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A SIMPLE 16-BIT MICROCOMPUTER UTILIZING THE 9900 CPU.(U)
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A SIMPLE 16-BIT MICROCOMPUTER UTILIZING THE 9900 CPU

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Guidance and Control Directorate
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8 December 1978

U.S. ARMY MISSILE RESEARCH AND DEVELOPMENT COMMAND

Redstone Arsenal, Alabama 35809

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The development of the large scale integrated circuit and its application in computers has resulted in a virtual explosion in data processing capabilities. These capabilities are being integrated into many existing and planned missile systems to provide increased accuracy, reliability, and maintainability at low cost. This report presents the design of a one board computer based on the 16-bit TMS 9900 CPU chip. Emphasis is placed on the simplicity, low cost, small size, and relatively high throughput rate of the computer.

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CONTENTS

I. INTRODUCTION

With the advent of the microprocessor, a virtual explosion in data processing capability has taken place. The US Army Missile Research and Development Command (MIRADCOM) is investigating the tremendous capabilities of these devices in the areas of rocket/missile guidance and fire control.

This report describes the development of a small, inexpensive microprocessor system designed to investigate the capabilities of one of the newer 16-bit machines (TMS 9900). Although the system was designed to investigate video tracking/correlation algorithms, this small system could easily handle many small computing tasks such as missile sequencing, simple guidance tasks, automatic testing, etc. With more extensive memory and input/output (I/O), this computer could handle many complex functions such as real-time video tracking, missile guidance and control, and rocket/gun fire control.

The main advantages to be gained by using microprocessors are:

a) Capability — Many functions desirable in missile and fire control systems can be implemented (practically speaking) only through the use of microprocessors.

b) Flexibility/Modularity — A common microprocessor module could serve as the autopilot for many different missile families.

c) Cost Effective — The system described in this report could have been procured 8 years ago for approximately $10K in commercial quantities (although it would have been approximately three times as large and required approximately four times as much power). The system described here was designed, hand made, and checked out at a total cost of less than $5K. Texas Instruments has recently introduced a similar system at a cost of $450.

II. TMS 9900 FEATURES

The TMS 9900 single chip central processing unit (CPU) is a logical choice for applications involving moderately high throughput and arithmetic processing. Key features include:

a) Sixteen-bit instruction word.

b) Instruction set reminiscent of many minicomputers (including multiply and divide).

c) Direct addressing capability of 65K-bytes.

d) Memory-to-memory architecture.

e) Separate memory, I/O, and interrupt buss structures.

f) Sixteen general purpose, memory resident registers.

g) Sixteen vectored, prioritized interrupts (1 nonmaskable).

The 9900 uses a flexible memory-to-memory architecture. There are only essentially three registers internal to the CPU: the status register (ST), the workspace pointer (WP), and the program counter (PC). The other sixteen general purpose registers (R0-R15) are actually words in memory. The WP is the address of the first register (R0) and the other 15 are the next 15 contiguous words of memory. One advantage of this approach is that a context switch is made by switching only three registers (the ST, WP, and PC). A single instruction accomplishes such a switch. Instructions in this architecture can be memory-to-memory or memory-to-register. Provisions are provided for indirect addressing and automatic incrementing of registers.

Two unique software features of the 9900 are the user defined external functions and the extended operations (XOP) instructions. The user can decode the external functions to provide certain user defined operations. The XOP instructions are vectors to user written subroutines with the added benefit of parameter passing. The return from the XOP is accomplished in a single instruction.

As with many microprocessors, a monitor program is available from the manufacturer of the 9900. Called TIBUG, the monitor can perform many simple tasks such as memory inspect/change, find hex strings, set breakpoints, perform hexadecimal arithmetic, etc. Perhaps of greater value, however, is the ability of the user to use many of the I/O utilities contained in the monitor. This monitor was used in the system described here and served well as a hardware/software troubleshooting aid. Interested persons should consult Texas Instruments' "TM 990/100M Microcomputer Users Guide," dated August 1977.

III. CPU BOARD DESIGN

The microprocessor system was constructed on a single TM 990/512 prototype board as shown in Figure 1. The CPU circuitry is shown in Appendix A, Figure A-1, Sheet 1. The CPU chip (U18) requires power supplies of +5, -5, and +12 V. In addition, a 12-V, 4-phase, nonoverlapping clock is required. The clock voltages are supplied by U17. In the prototype system, a 0.1-μf capacitor was substituted for a 48-MHz crystal due to long component lead times. The LC tank circuit was adjusted to produce a 3.00-MHz output to the CPU.

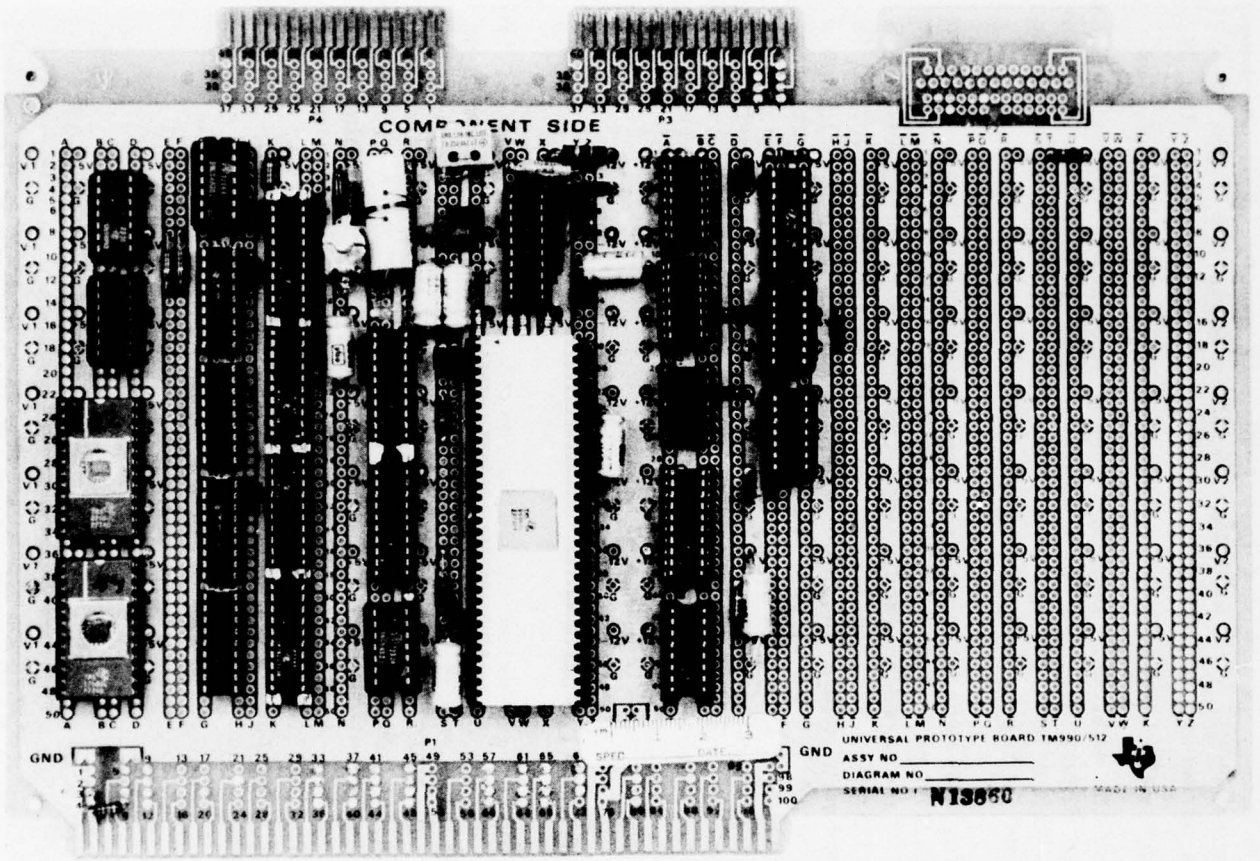


Figure 1. Board layout on a TM 990/512 prototype board.

All CPU busses are buffered to allow future expansion. Figure A-1, Sheets 2, 3, and 8 are detailed schematics of the buffers. 74S241 tristate noninverting buffers were used to provide high drive capability at high speed.

System memory is divided into read only memory (ROM) and random access memory (RAM). The 2K bytes of ROM contain the TIBUG monitor and reside at memory and addresses 0000_{16} through $07FF_{16}$. The 2K bytes of RAM reside at memory addresses $F800_{16}$ through $07FF_{16}$ as required by the monitor. Detailed schematics of the ROM and RAM can be found in Figure A-1, Sheets 5 and 6, respectively. The decoding circuits which decode the address lines for the memory select function can be found in Figure A-1, Sheet 4.

I/O for the present prototype was limited to a single RS-232C full duplex I/O port and an 8 input interrupt system. These were the only I/O ports mechanized, since the only peripheral available at this writing is an intelligent terminal. More extensive I/O is easy to implement since the 9900 supports memory mapped I/O, has a serial hardware I/O port, and has hardware to support direct memory access (DMA) data transfers. I/O through the built-in serial port [called the communications register unit or (CRU)] is especially easy since Texas Instruments supplies LSI chips which perform either serial (TMS 9902) or parallel (TMS 9901) I/O between the CRU and the outside world.

IV. SYSTEM EXPANSION

System expansion should be considered in the areas of I/O and memory expansion. I/O expansion should be directed towards an 8-bit parallel port which is IEEE-488 buss compatible and/or a 16-bit DMA port. The IEEE-488 buss would allow interfacing to many measuring instruments and computers containing 488 buss I/O. A 16-bit DMA port would allow storage of high speed data such as real-time digitizing of video scenes. Additional memory should be considered since the 2K bytes provided in the prototype is not adequate for most purposes. One circuit card the size of the TM 990/512 card can easily hold 32K bytes of memory and should be adequate for most purposes.

Appendix A. SYSTEM SCHEMATIC AND BOARD LAYOUT

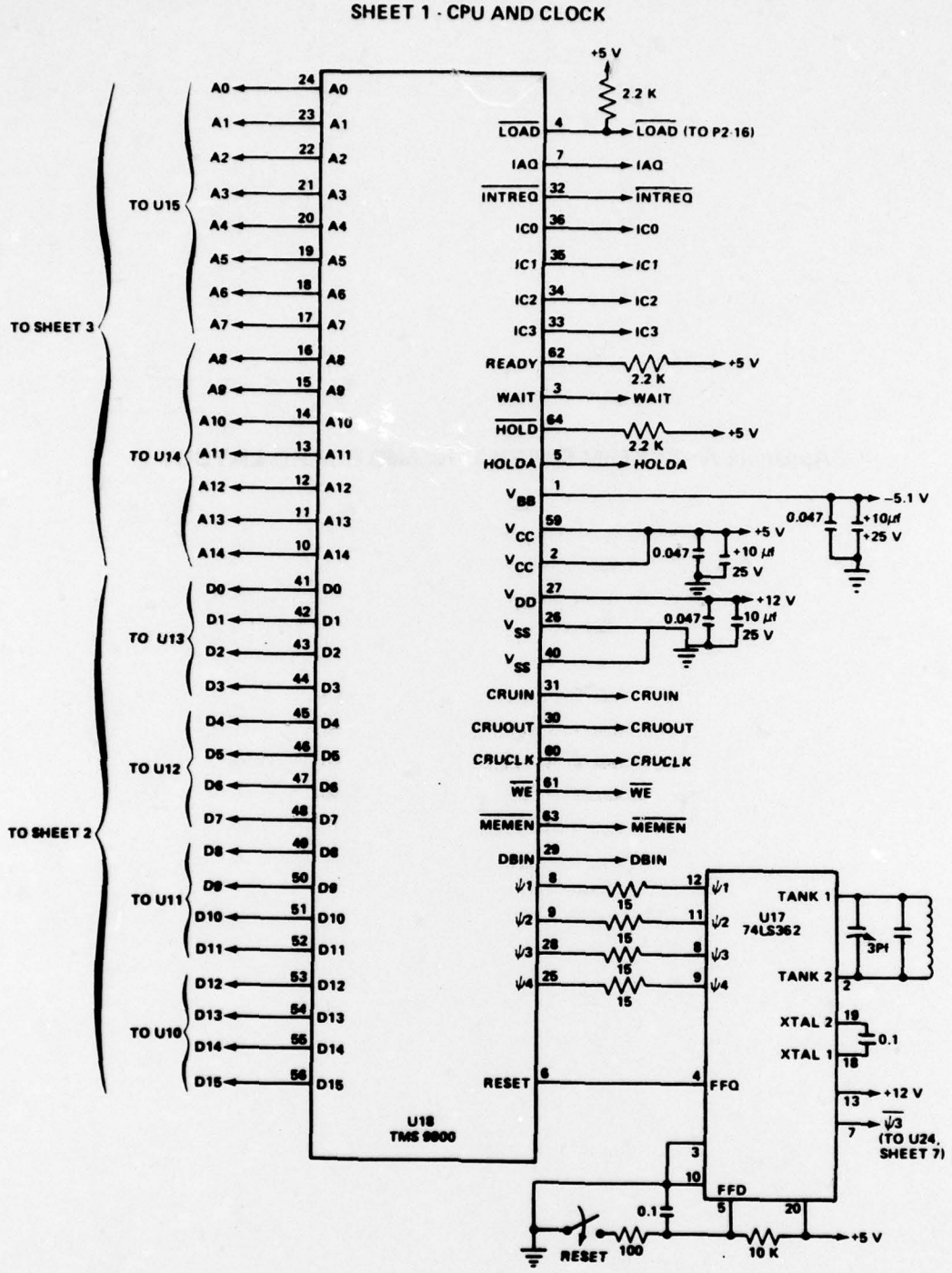


Figure A-1. TMS 9900 system schematic.

SHEET 2 – DATA BUSS BUFFERS

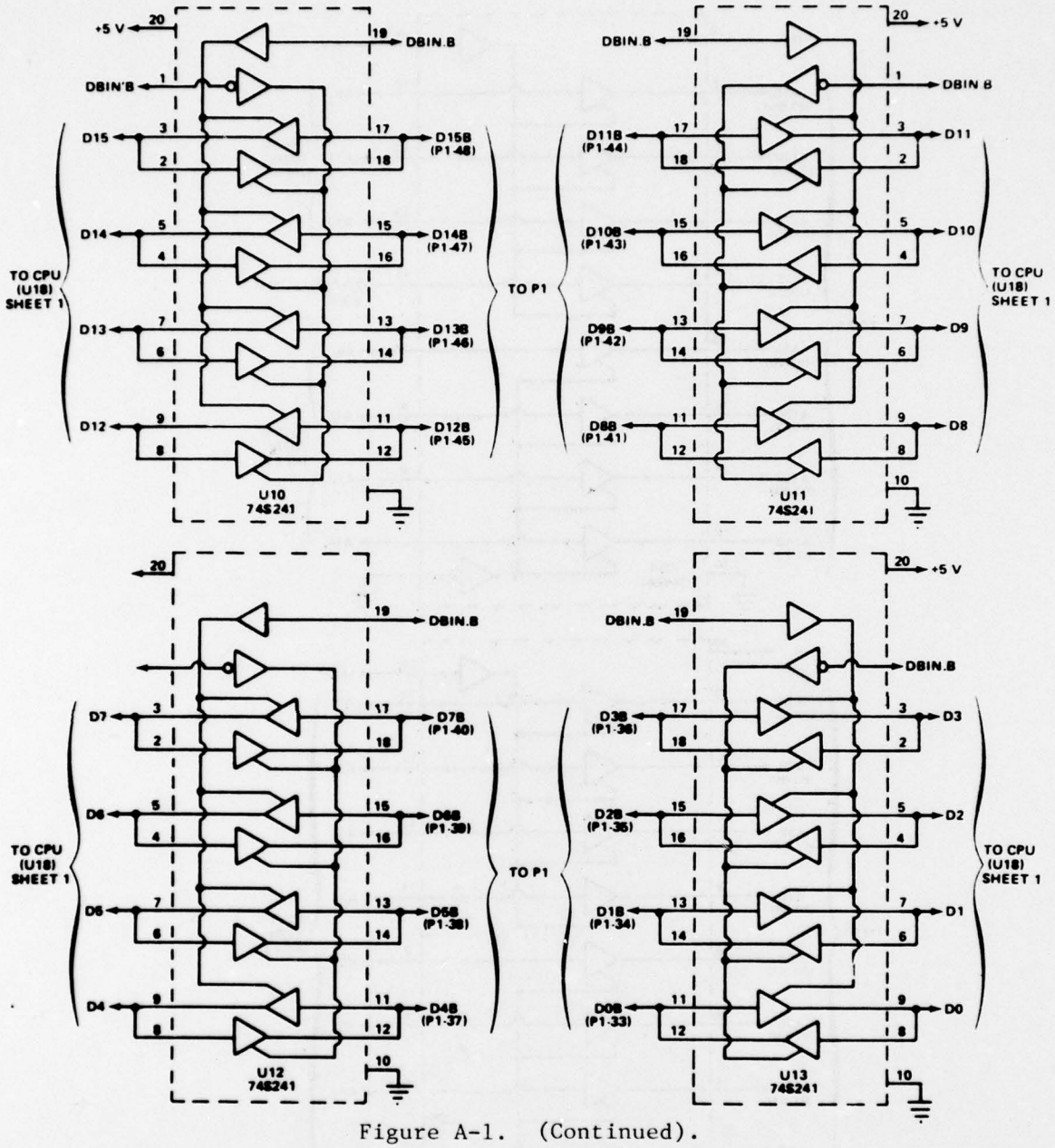


Figure A-1. (Continued).

SHEET 3 – ADDRESS BUFFERS

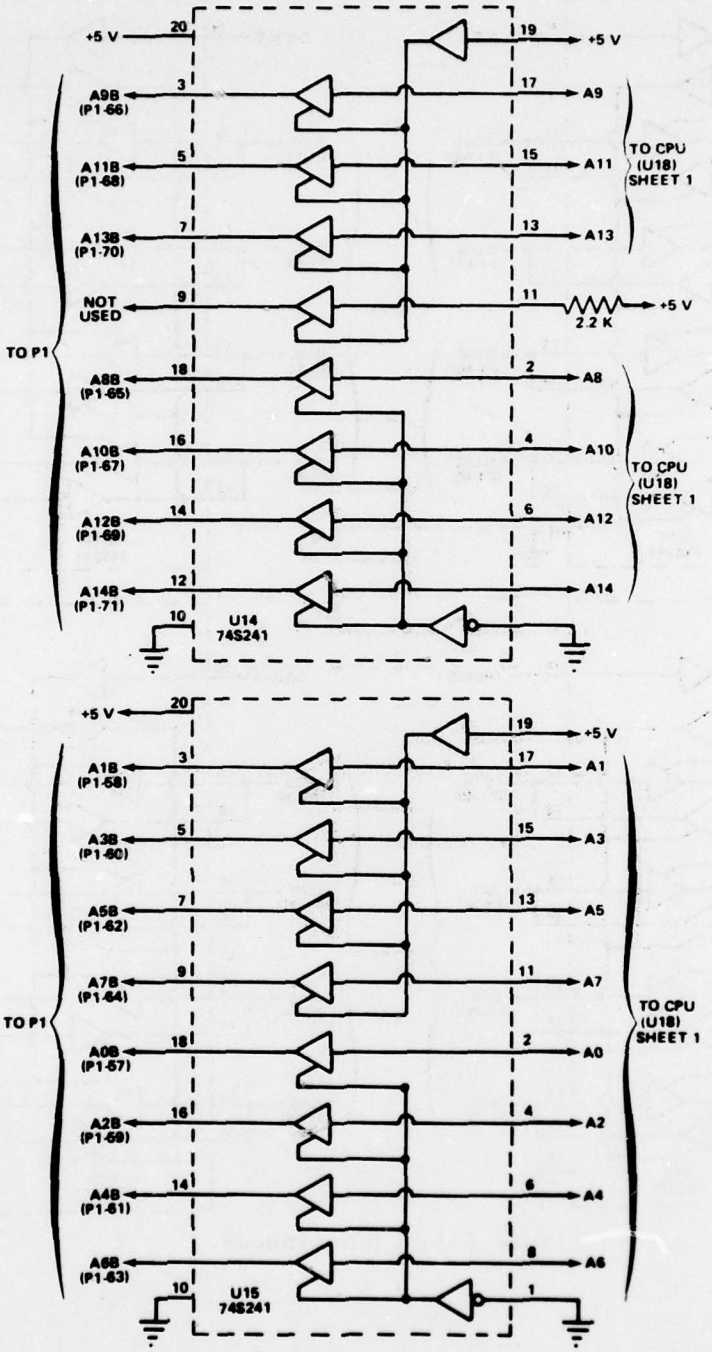
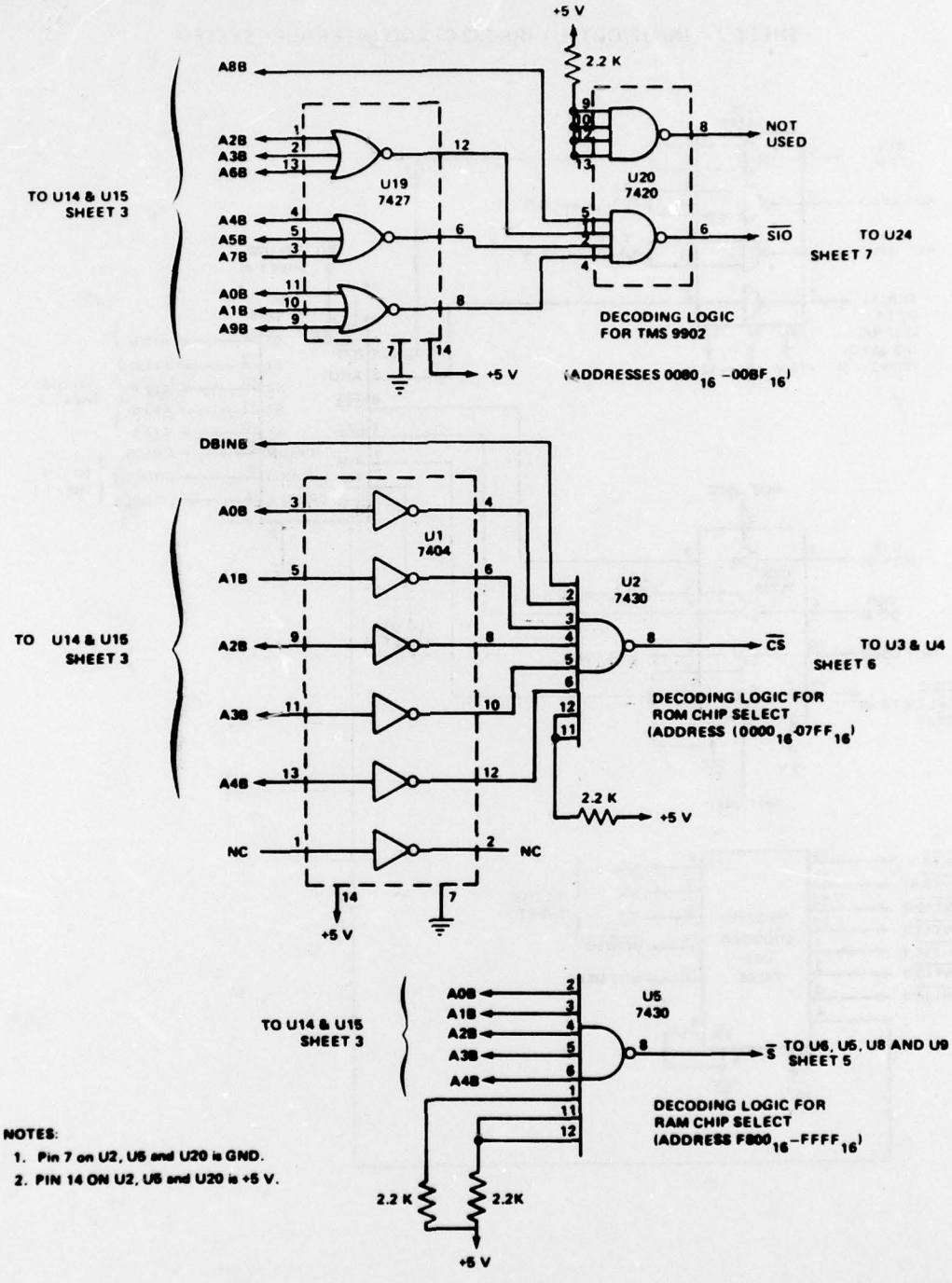


Figure A-1. (Continued).

SHEET 4– MEMORY AND I/O DECODERS



NOTES:

1. Pin 7 on U2, U5 and U20 is GND.
2. PIN 14 ON U2, U5 and U20 is +5 V.

Figure A-1. (Continued).

SHEET 7 – INPUT/OUTPUT (RS-232 C) AND INTERRUPT SYSTEM

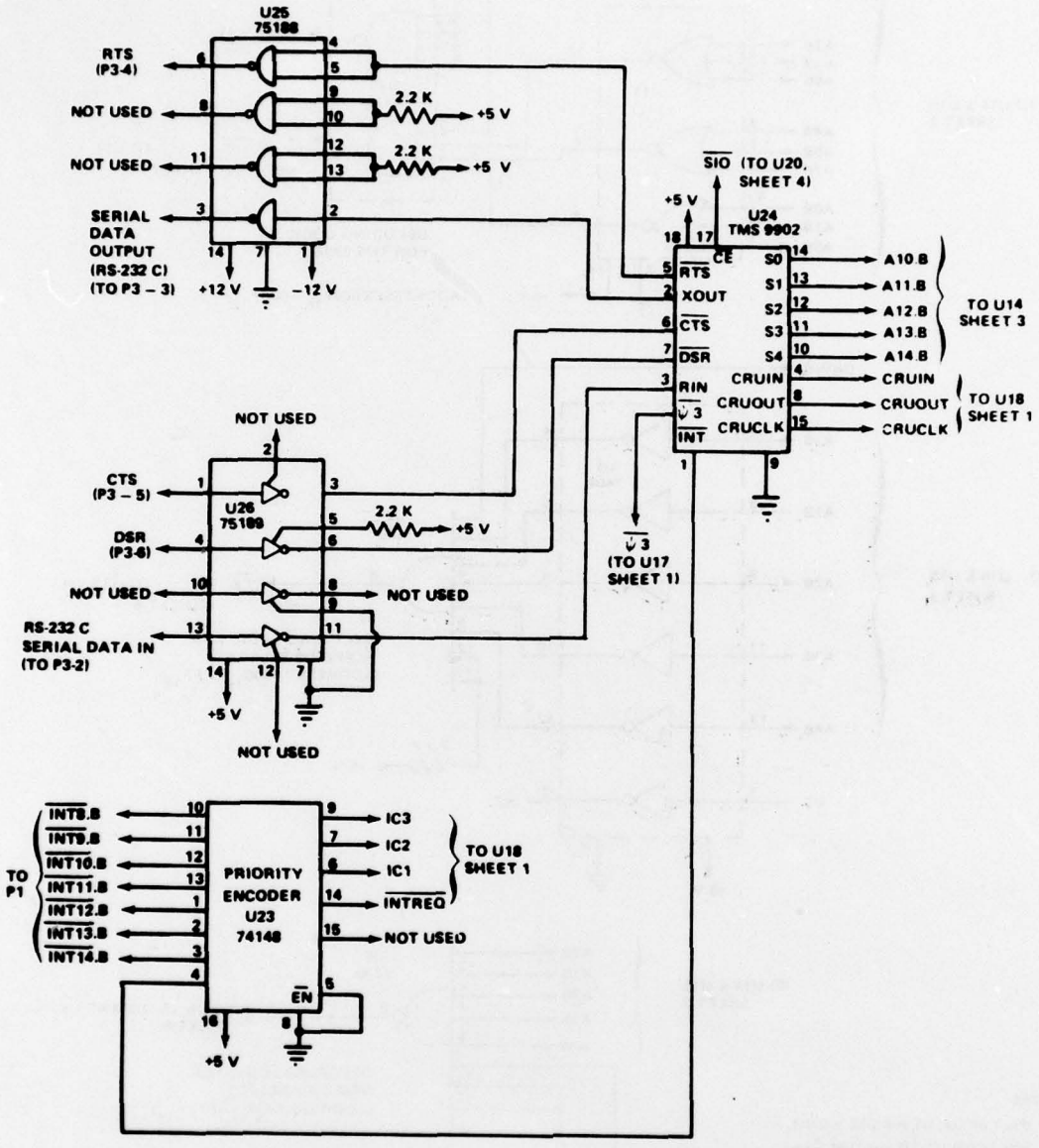


Figure A-1. (Continued).

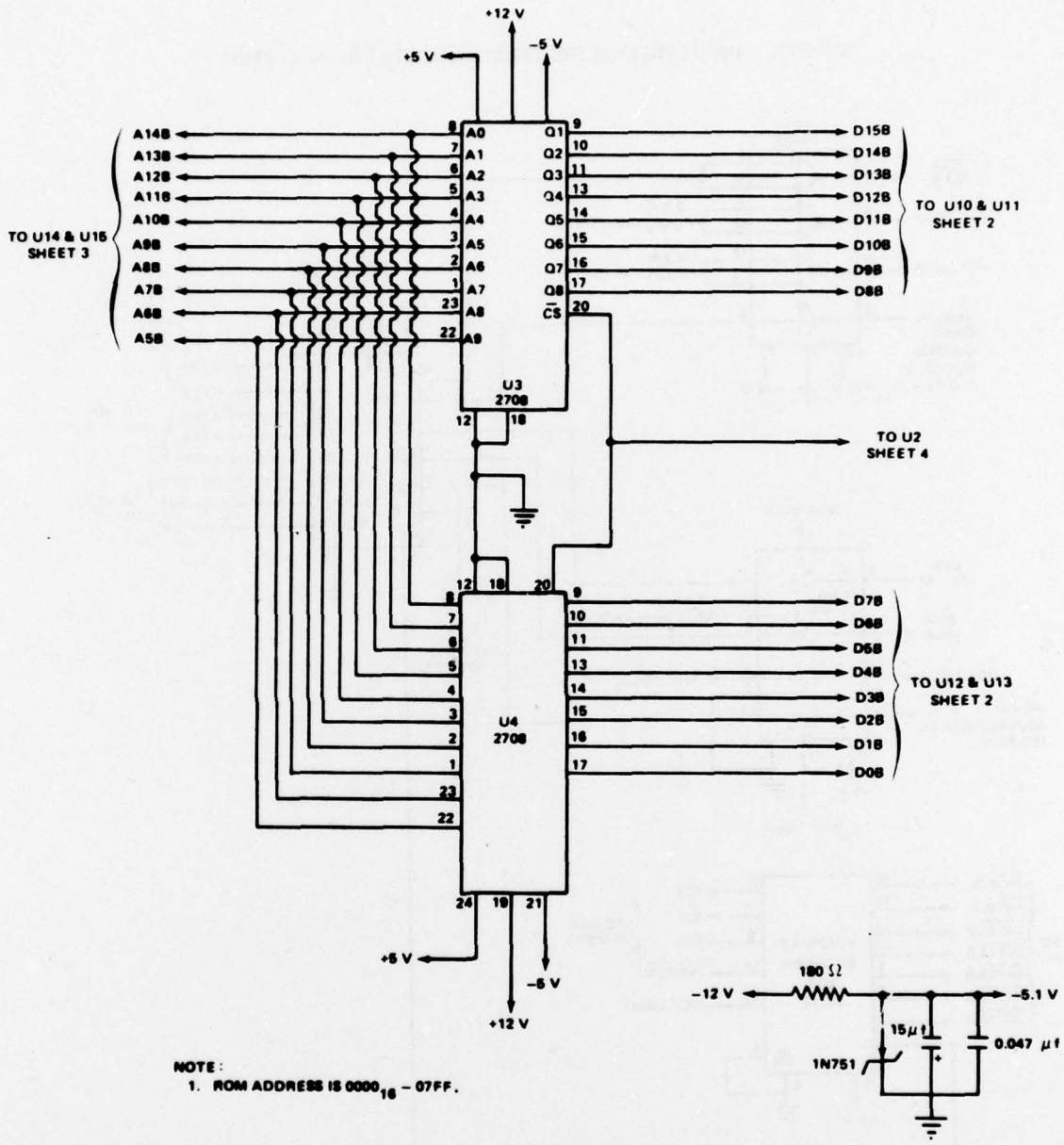
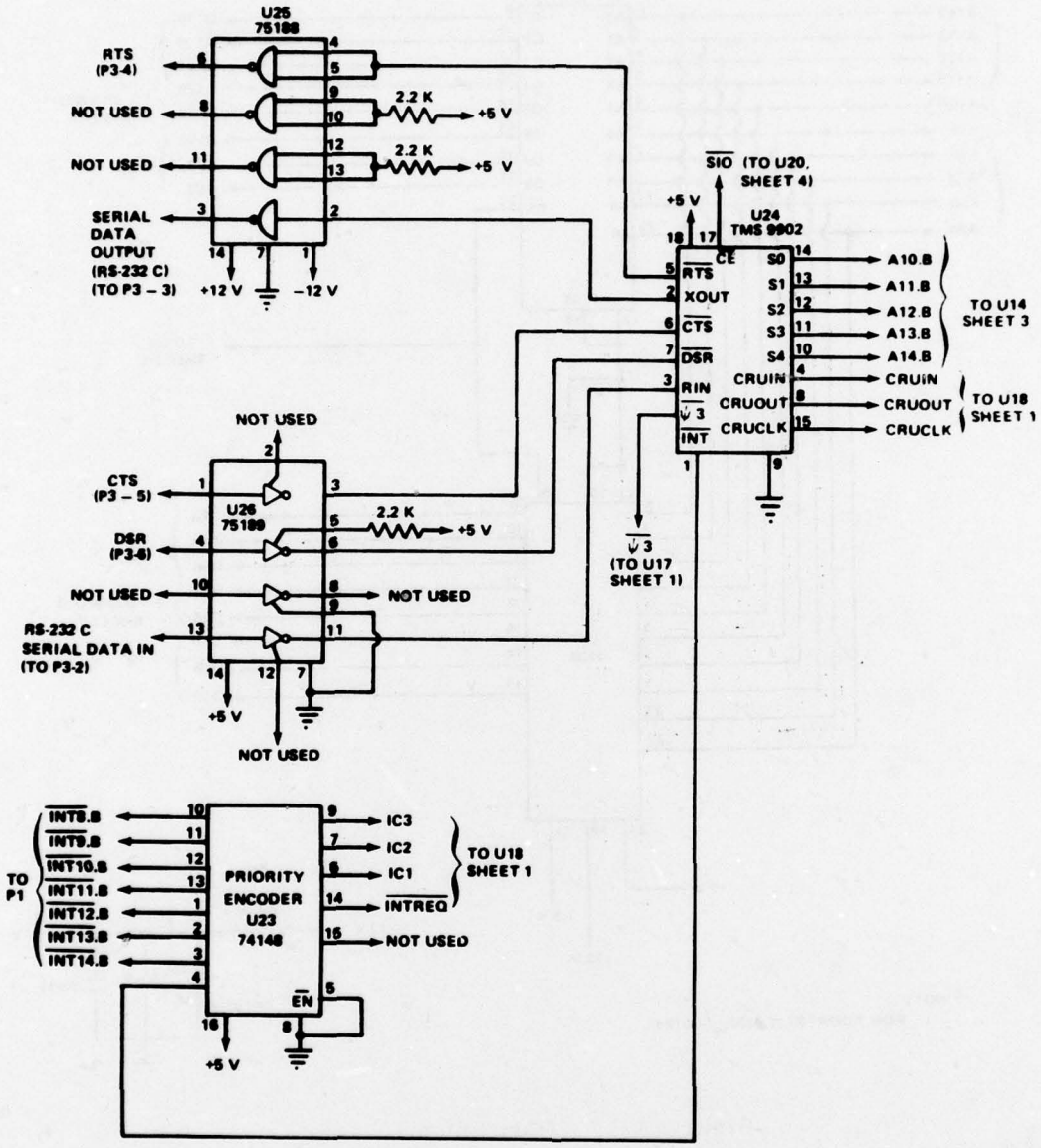


Figure A-1. (Continued).

SHEET 7 – INPUT/OUTPUT (RS-232 C) AND INTERRUPT SYSTEM



SHEET 8 – CONTROL LINE BUFFERS

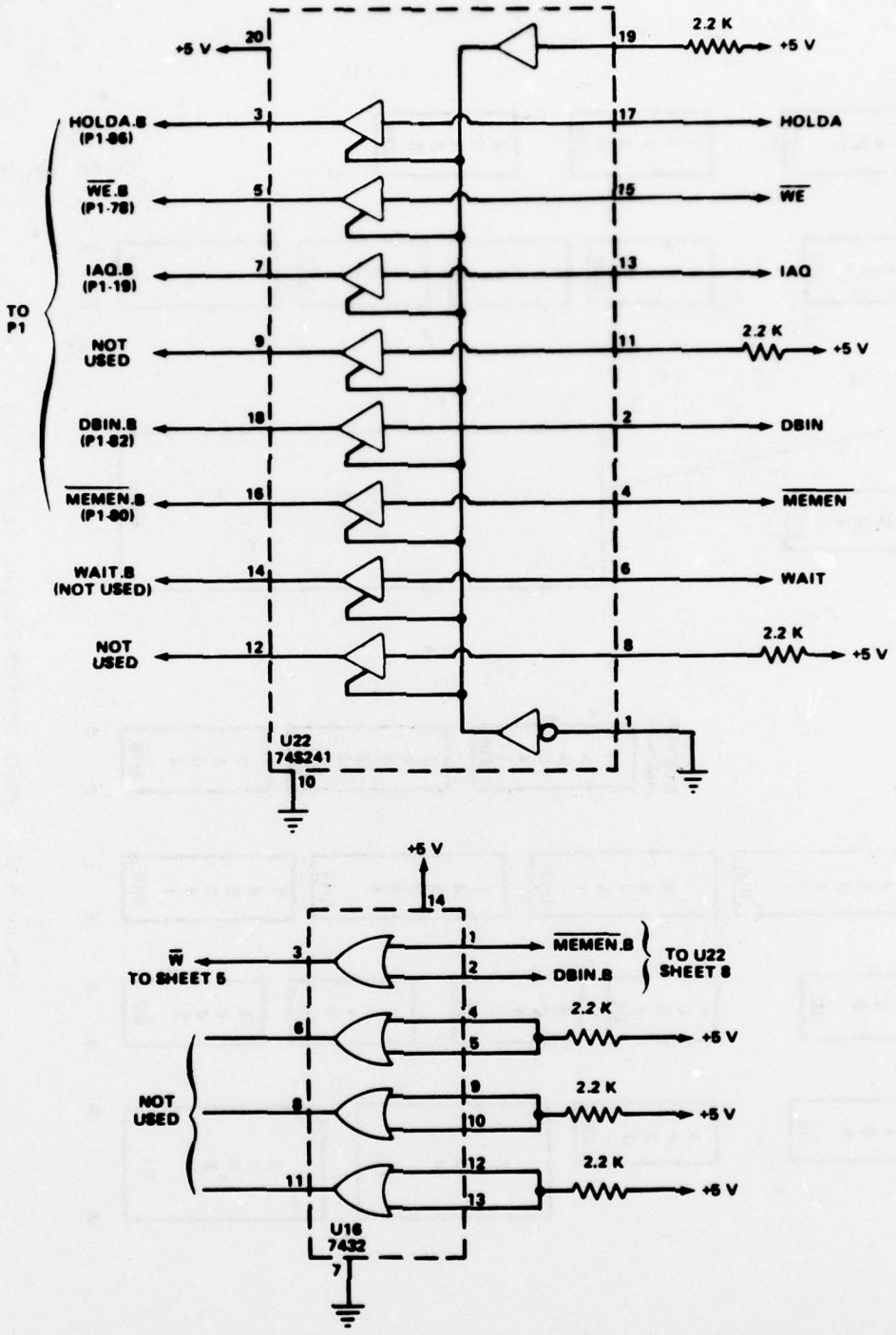


Figure A-1. (Concluded).

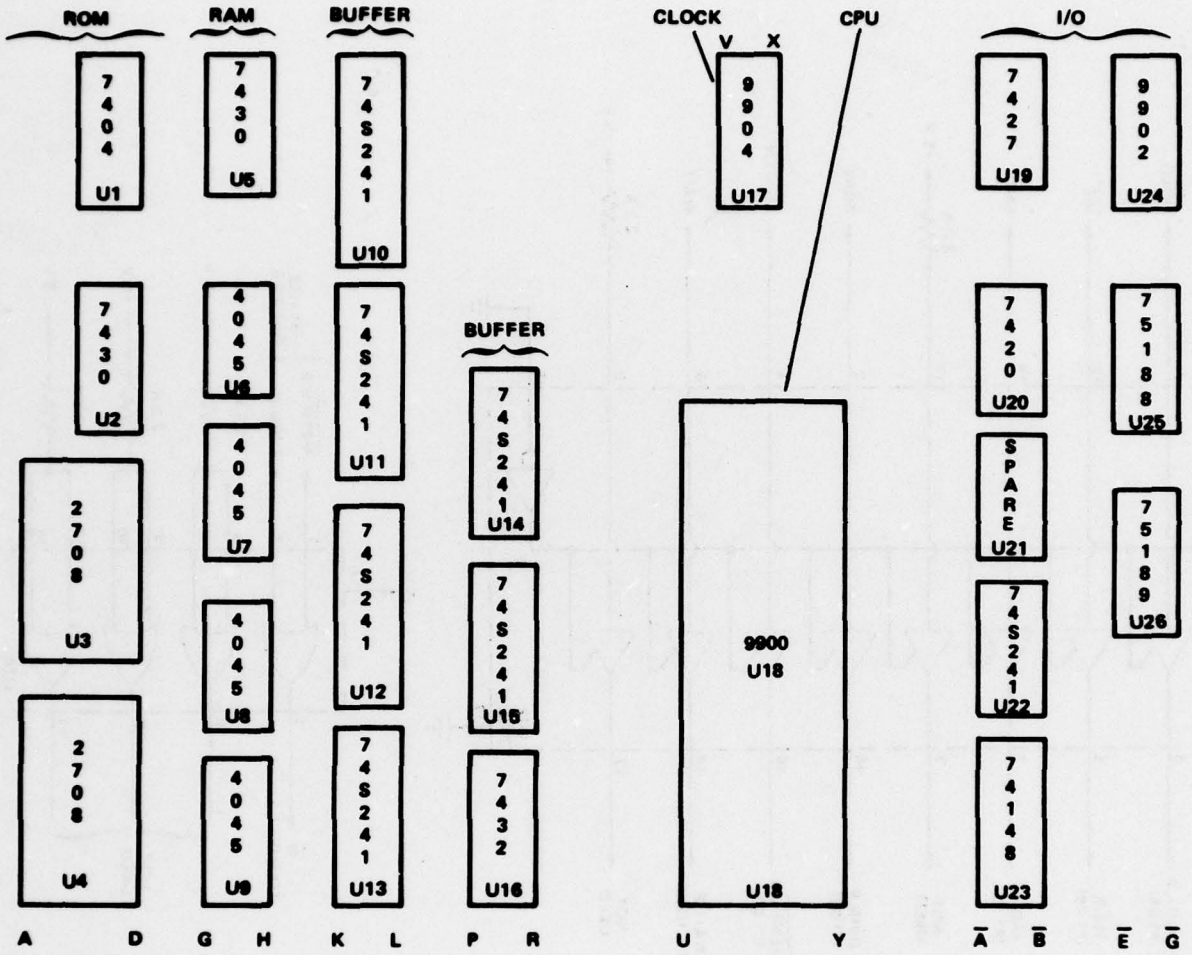


Figure A-2. 9900 system layout (top view).

Appendix B. PIN FUNCTION TABLES

TABLE B-1. PIN ASSIGNMENTS, CONNECTOR P1

Pin	Signal	Pin	Signal
33	DOB	63	A6
34	D1B	64	A7
35	D2B	65	A8
36	D3B	66	A9
37	D4B	67	A10
38	D5B	68	A11
39	D6B	69	A12
40	D7B	70	A13
41	D8B	71	A14
42	D9B	5	$\overline{\text{INT8}}$
43	D10B	7	$\overline{\text{INT10}}$
44	D11B	8	$\overline{\text{INT9}}$
45	D12B	9	$\overline{\text{INT12}}$
46	D13B	10	$\overline{\text{INT11}}$
47	D14B	11	$\overline{\text{INT14}}$
48	D15B	12	$\overline{\text{INT13}}$
57	A0	19	IAQ.B
58	A1	78	$\overline{\text{WE.B}}$
59	A2	80	MEMEN.B
60	A3	82	DBIN.B
61	A4	86	HOLDA.B
62	A5		

TABLE B-2. PIN ASSIGNMENTS, CONNECTOR P2

Pin	Signal
2	RS-232 Data In (RCV)
3	RS-232 Data Out (XMT)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
16	Load (to U18, Pin 4)

TABLE B-3. PIN ASSIGNMENTS, CONNECTOR P3

Pin	Signal
1	GND
2	RS-232 Data In (RCV)
3	RS-232 Data Out (XMT)
4	Ready to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	GND

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