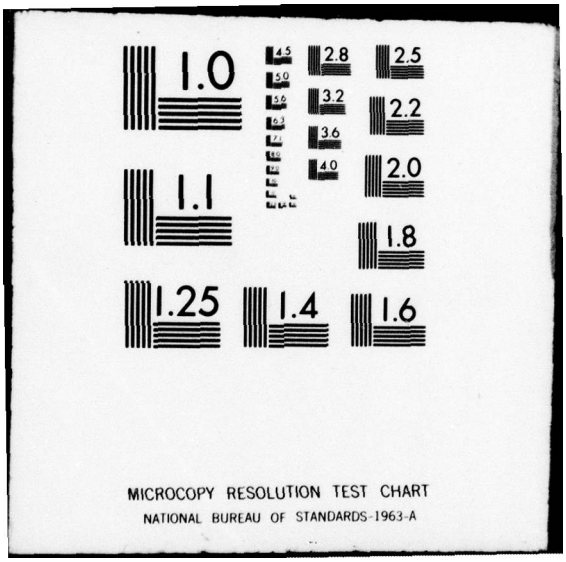
AD-A065 890 HONEYWELL INC ST PETERSBURG FL AVIONICS DIV F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TAPE CHIP --ETC(U)
FEB 79 W R RODRIGUES DE MIRANDA DAAB07-77-C-0526
UNCLASSIFIED DELET-TR-77-0526-4 NL

END
DATE FILMED
5-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

LEVEL II

Research and Development Technical Report
DELET-TR-77-0526-4

MANUFACTURING METHODS AND TECHNOLOGY FOR TAPE CHIP CARRIER

William R. Rodrigues de Miranda
Honeywell Inc.
St. Petersburg, Florida 33733

February 1979

Quarterly Report for Period Ending 30 June 1978

PREPARED FOR

Electronics Technology and Devices Laboratory

ERADCOM
US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

CONTRACT NO. DAAB07-77-C-0526
HONEYWELL INC.
ST. PETERSBURG, FLORIDA 33733

NOTICES

Disclaimers

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (WHEN DATA ENTERED)

(19) **REPORT DOCUMENTATION PAGE**

READ INSTRUCTIONS BEFORE COMPLETING FORM

(18) 1. REPORT NUMBER: DELET-TR-77-0526-4

2. GOVT ACCESSION NO

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (AND SUBTITLE): Manufacturing Methods and Technology Engineering for Tape Chip Carrier,

(9) 5. TYPE OF REPORT & PERIOD COVERED: Quarterly Report, 1 Apr - 30 Jun 78,

6. PERFORMING ORG. REPORT NUMBER

(10) 7. AUTHOR(S): William R. Rodrigues de Miranda

(15) 8. CONTRACT OR GRANT NUMBER(S): DAAB07-77-C-0526

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Honeywell Inc., Avionics Division
13350 US Highway 19
St. Petersburg, FL 33733

(16) 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: IL762705AH94 C2 200 (17)

11. CONTROLLING OFFICE NAME AND ADDRESS
ERADCOM
ATTN: DELET-IT
Fort Monmouth, NJ 07703

(11) 12. REPORT DATE: Feb 79

13. NUMBER OF PAGES: 33

14. MONITORING AGENCY NAME AND ADDRESS (IF DIFFERENT FROM CONTROLLING OFFICE)

(12) 82p.

15. SECURITY CLASS. (OF THIS REPORT): Unclassified

15A. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (OF THIS REPORT)

Approved for Public Release - Distribution Unlimited

17. DISTRIBUTION STATEMENT (OF THE ABSTRACT ENTERED IN BLOCK 20, IF DIFFERENT FROM REPORT)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

Tape Chip Carrier
Hybrid Microcircuit
Film Carrier
Inner Lead Bonding
Outer Lead Bonding
Automatic Feed Mechanism
Material Handling System
Automatic Assembly Line

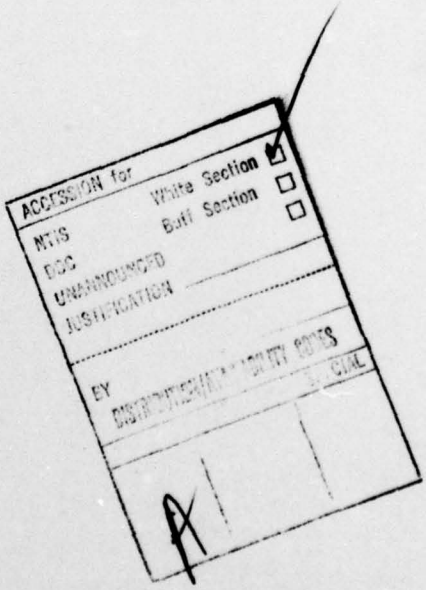
20. ABSTRACT (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

This report describes the work performed during the fourth quarter of a 26-month contract. The contract is aimed at establishing and demonstrating the feasibility of an automated assembly line for hybrid microcircuits using tape chip carrier technology for semiconductor devices whenever practical. The automated line will also make use of automatic substrate handling equipment to move partially assembled devices in and out of magazines.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED 393 215
SECURITY CLASSIFICATION OF THIS PAGE (WHEN DATA ENTERED)

TABLE OF CONTENTS



LIST OF ILLUSTRATIONS

INTRODUCTION

The purpose of this program is to demonstrate the concept of an automated assembly line for hybrid microcircuits, through the establishment of techniques for tape carrier mounting of semiconductor chips, burn-in and testing of these chips on tape and their placement into representative hybrid circuits. The Tape Chip Carrier (TCC) system permits mounting of semiconductor chips on reels of sprocketed film. The system is an established means of automating the interconnection of individually packaged semiconductor chip devices. It has been adapted to the fabrication of hybrid microcircuits used in the manufacture of certain commercial computers. The Army is interested in utilizing the tape carrier mounting technology for the manufacture of hybrid microcircuits for military electronic applications when advantageous for economic reasons or desirable from the viewpoint of increased reliability. Its overall adaptation to the hybrid program. The automated assembly line will make use of an automatic feed mechanism at each process step, and magazines to transport substrates and partially assembled circuits between process points.

This is the fourth quarterly report on the MM&T program. Honeywell is pleased to report continued good progress as the first of the Material Handling Systems are nearing completion.

SECTION 1

MATERIAL HANDLING SYSTEM

The Material Handling System is taking shape with extensive work on several of the components of the system. Most effort during this reporting period was expended on the Air Substrate Handling System for the Weltek Model 44 printer and the Furnace On-Loader to be attached to the Lindberg Firing furnace. Progress on the other system components has been mostly made in the areas of design and detail drafting and will be discussed further below.

The following is a status summary of these and other components of the Material Handling System.

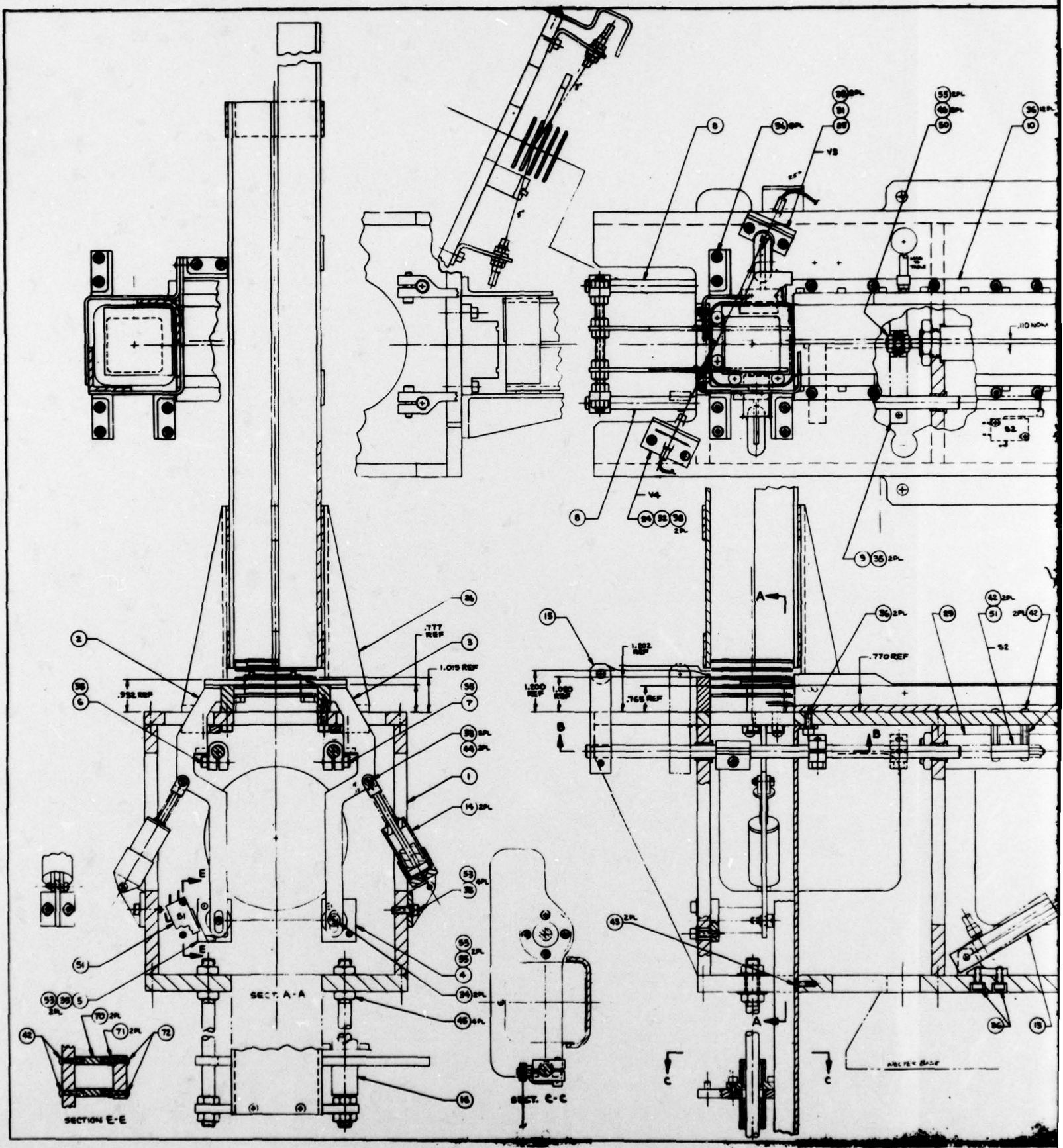
1. The Mechanical Substrate Handling System was completed during the previous reporting period and is described in the August 1978 report.

2. The Air Substrate Handling System is nearing completion with all parts fabricated. The air and relay logic systems are being assembled. During this reporting period some problems with the system were experienced during the debugging stage. These problems required redesign and rebuilding of certain components of the system. The parts involved were the air slide track which experienced an oscillation in air flow causing in turn the substrate to vibrate against the vertical track guides. This oscillation which was not observed in work with the proof model track was determined to be caused by the type of flow regulating valve used on this system.

   Another difficulty ensued in the stopping mechanism which captures the substrate at the end of the slide for positioning over the vacuum hold-down orifices. This system must be precisely balanced in order to prevent the substrate from bouncing back into the track. Extensive experimentation was required and some redesign and rebuilding in order to have this system work satisfactorily and consistently.

   Figure 1 shows an assembly drawing of the Substrate Handling System. Figure 2 shows a detail drawing of the air slide table and stopper mechanism. Figure 3 shows the operation of the lifter table and substrate snugging mechanism. And finally, Figure 4 shows the magazine index mechanism.

3. Furnace On-Loader. The Furnace On-Loader was completed during this reporting period and underwent checkout, debugging and some redesign and rebuild. Finally it was married to the Lindberg Model S-B Furnace.


SECT. A-A
SECT. C-C
SECTION E-E
.777 REF
1.019 REF
.952 REF
.770 REF
.765 REF
1.892 REF
1.000 REF
1.000 REF
.110 NOM
VB
V4
A
B
C
E

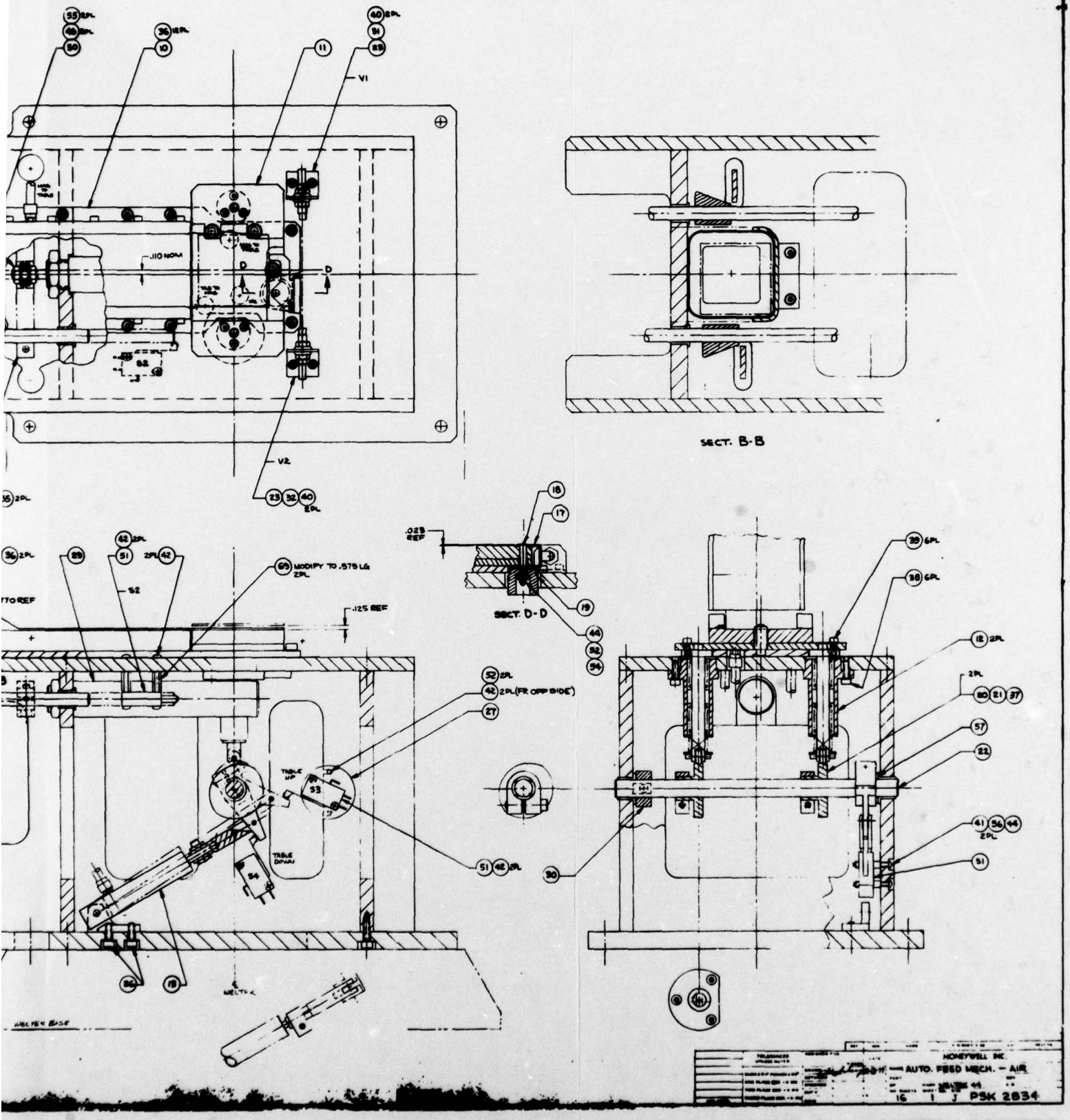
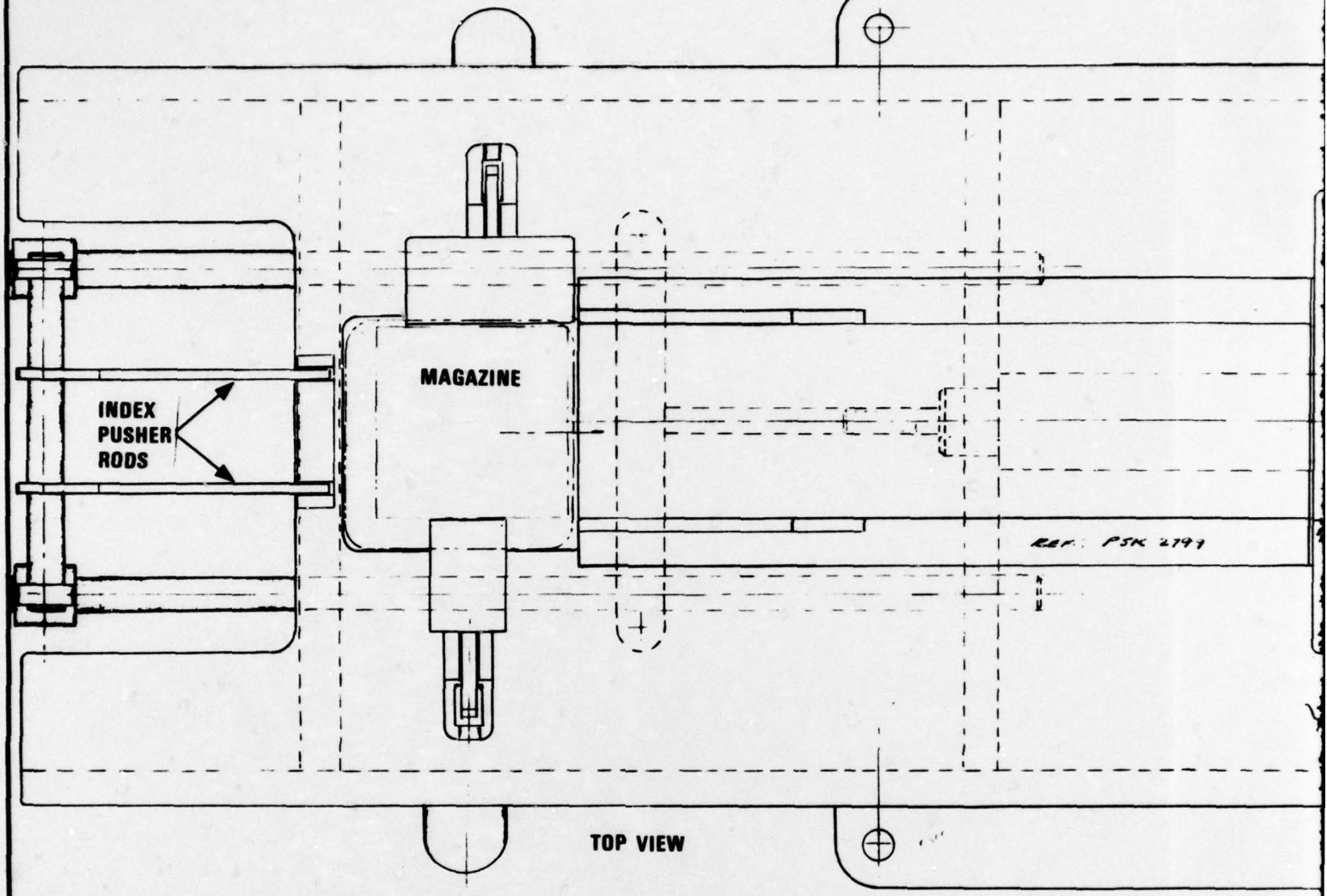
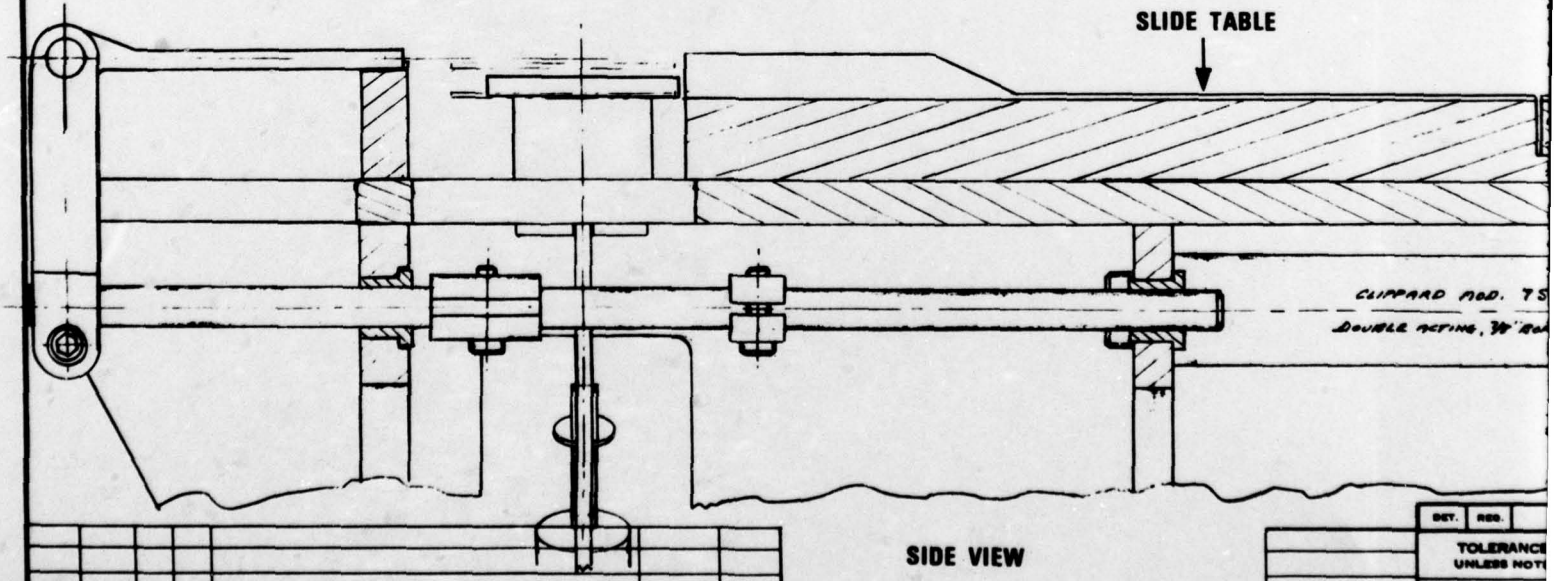


FIGURE 1. ASSEMBLY DRAWING OF AIR SUBSTRATE HANDLING SYSTEM

CAUTION: READ ALL NOTES & SPECS. REMOVE UNNECESSARY SHARP EDGES. SCREWS, SPRINGS & DOWELS TO SUIT. MARK TOOL NO. ON CASES MARK CASE NO., CASE NO.



TOP VIEW



SIDE VIEW

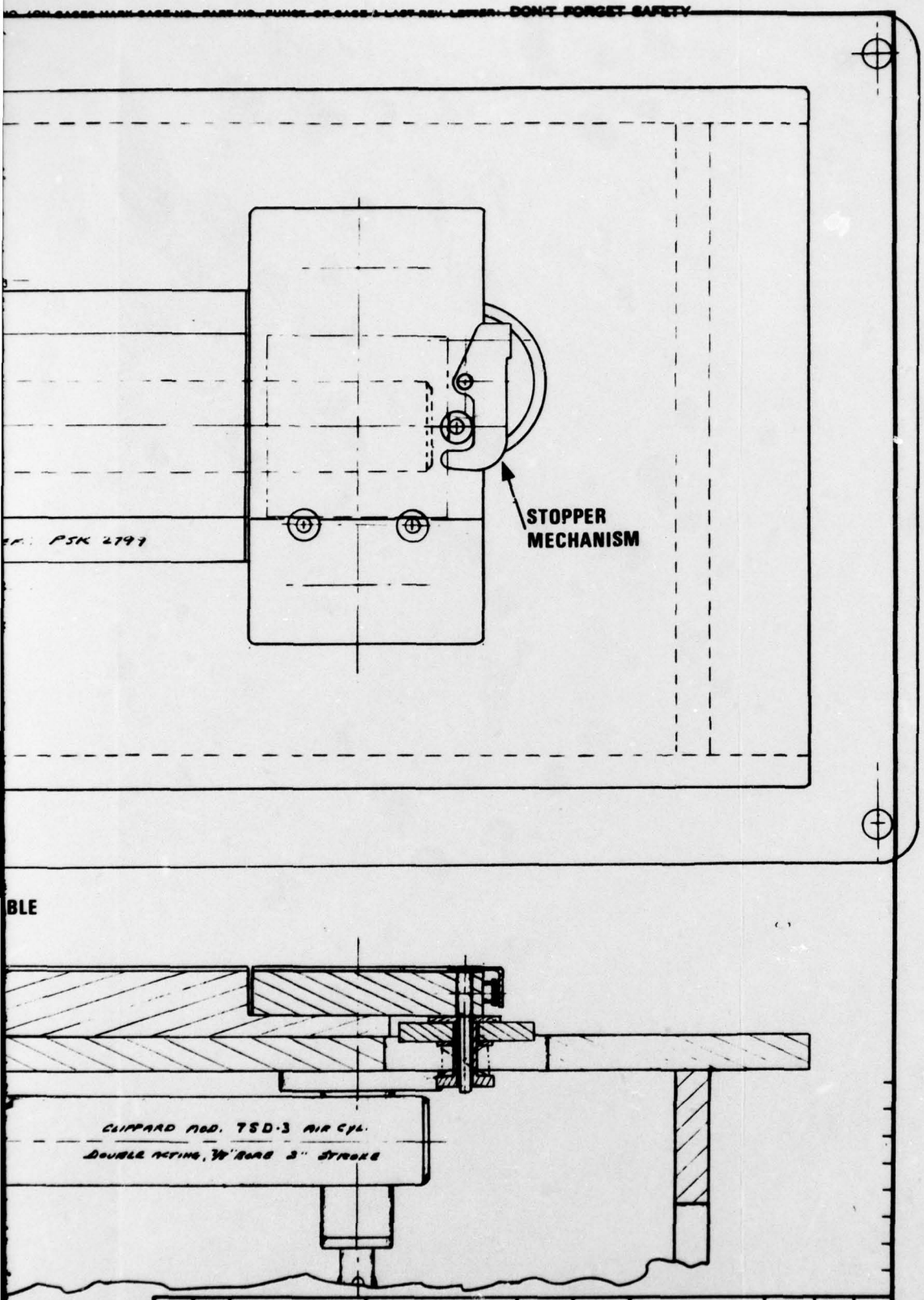
Ref: PSK 2799

SYM.	DATE	ENG.	C.C.	REVISIONS	DRAWN	E.O. NO.

DEC.	FRAC.
TOLERANCE UNLESS NOTE	
MACH ± 1° FORMA	
ONE PLACE DEC. ±	
TWO PLACE DEC. ±	
THREE PLACE DEC	

REF. DWGS.

CHG. NO.



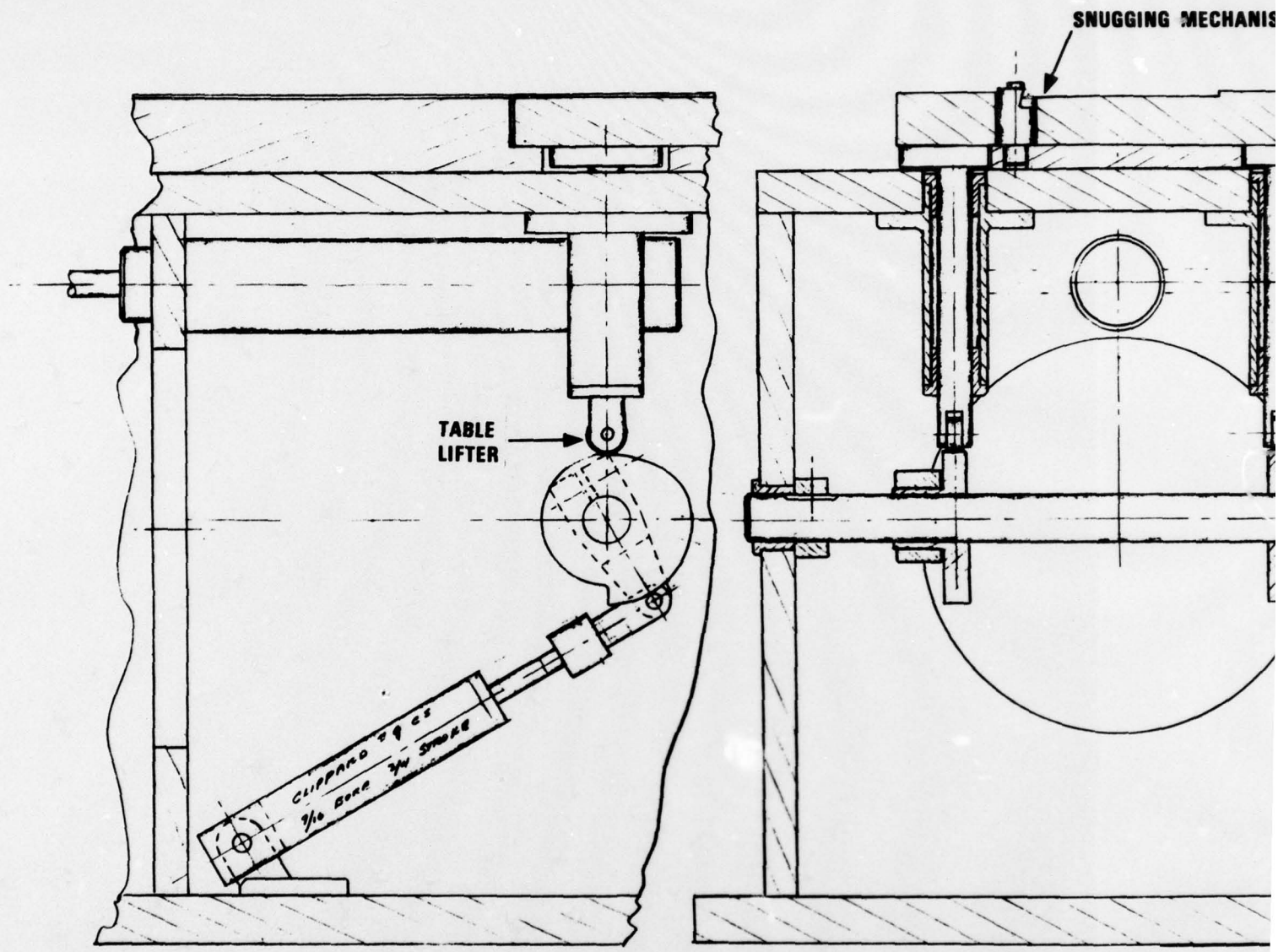
DET.	REQ.	NAME	FINISHED SIZE	MAT'L	HEAT TR.	MAT'L USED	WT. OR FT.	UNIT PRICE	TOTAL

TOLERANCES UNLESS NOTED	DESIGNED FOR PIECES	DATE	Honeywell
MACH ∠ ±1° FORMED ∠ ±2°	DRAWN DAVIDSON	11-2-77	NAME SUBSTRATE FEED MECHANISM, AIR
ONE PLACE DEC. = ±.030	DETAILED		PART TSD INSTR.
TWO PLACE DEC. = ±.010	CHECKED		OP. MACH. E.O.
THREE PLACE DEC. = ±.005	SUP'V.		NO. SHEETS 4 SHEET NO. 1 SIZE C PSK-
REF. DWGS.	ENG. G.C.		

CHG. NO. TOOLM 2 SIN. CHG. TO

FIGURE 2. SLIDE TABLE AND STOPPER MECHANISM

CAUTION: READ ALL NOTES & SPECS. REMOVE UNNECESSARY SHARP EDGES. SCREWS, SPRINGS & DOWELS TO SUIT. MARK TOOL NO. (ON GAGES MARK GAGE NO., PART NO., FUN



QTY.	DATE	ENG.	E.O.	REVISIONS	DRAWN	E. O. NO.

DEC.	FRS.	
TOLERANCES UNLESS NOTED		
MACH ∠ ±1° FORMED ∠ ±		
ONE PLACE DEC. = ±		
TWO PLACE DEC. = ±		
THREE PLACE DEC. = ±		

REF. DWGS.

CHG. NO.

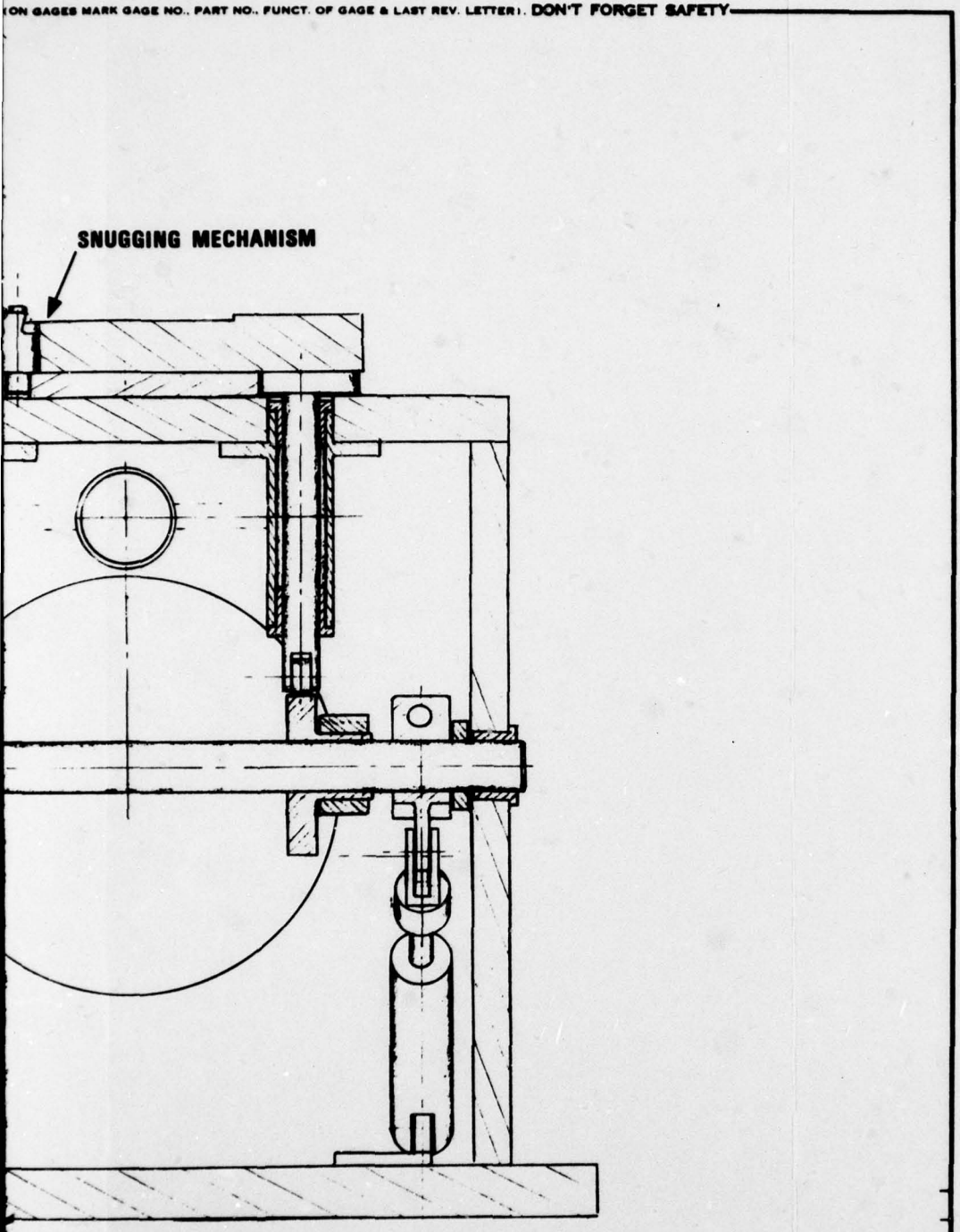
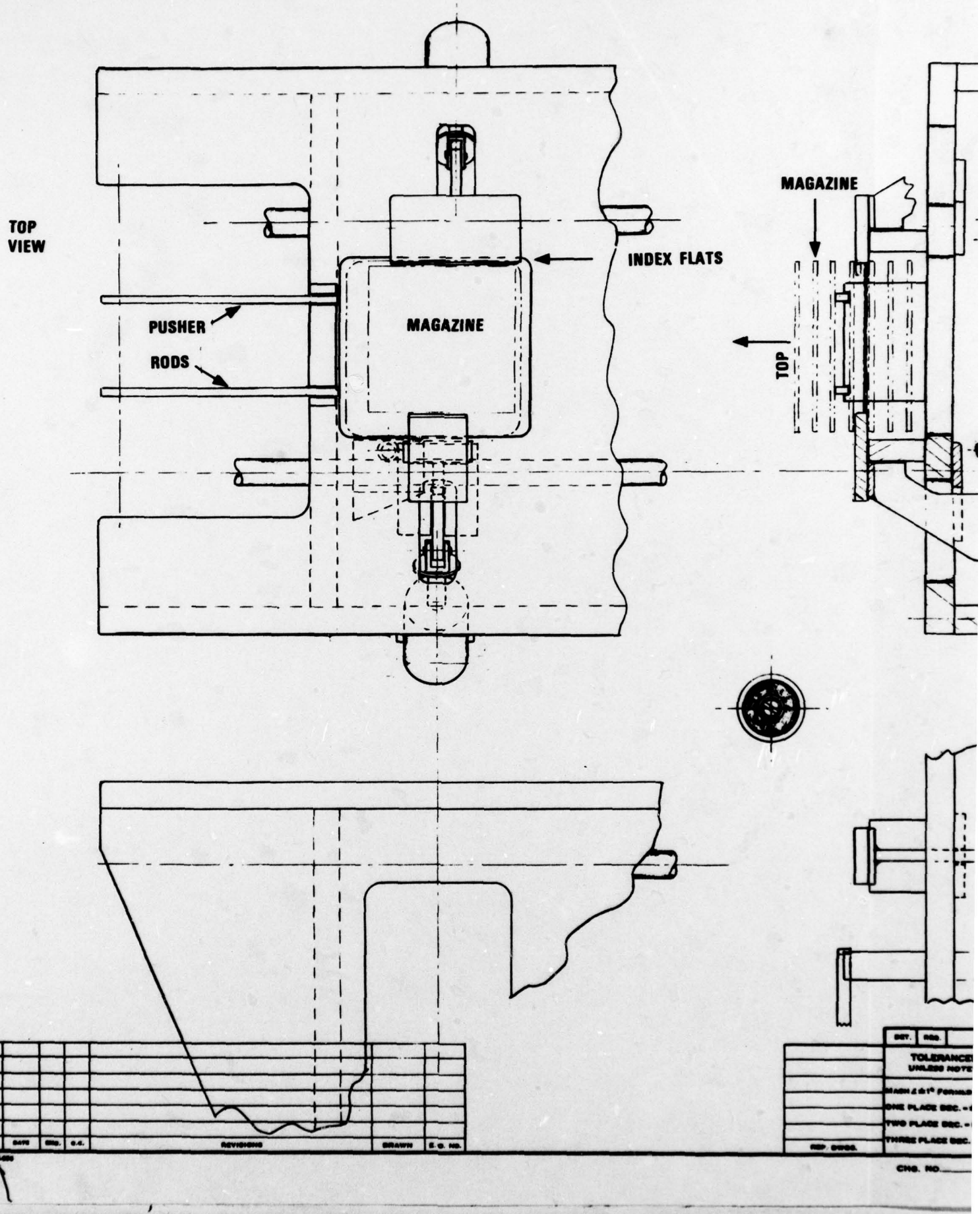


FIGURE 3. LIFTER TABLE AND SNUGGING MECHANISM

CAUTION: READ ALL NOTES & SPECS. REMOVE UNNECESSARY SHARP EDGES. SCREWS, SPRINGS & DOWELS TO SUIT. MARK TOOL NO. (ON GAGES MARK GAGE NO., PART NO.,



QTY.	DATE	ENG.	C.C.	REVISIONS	DRAWN	E.O. NO.

DIST. | RDS

TOLERANCE
UNLESS NOTE

ONE PLACE DEC. =
TWO PLACE DEC. =
THREE PLACE DEC.

REF. DWGS.

CNS. NO.

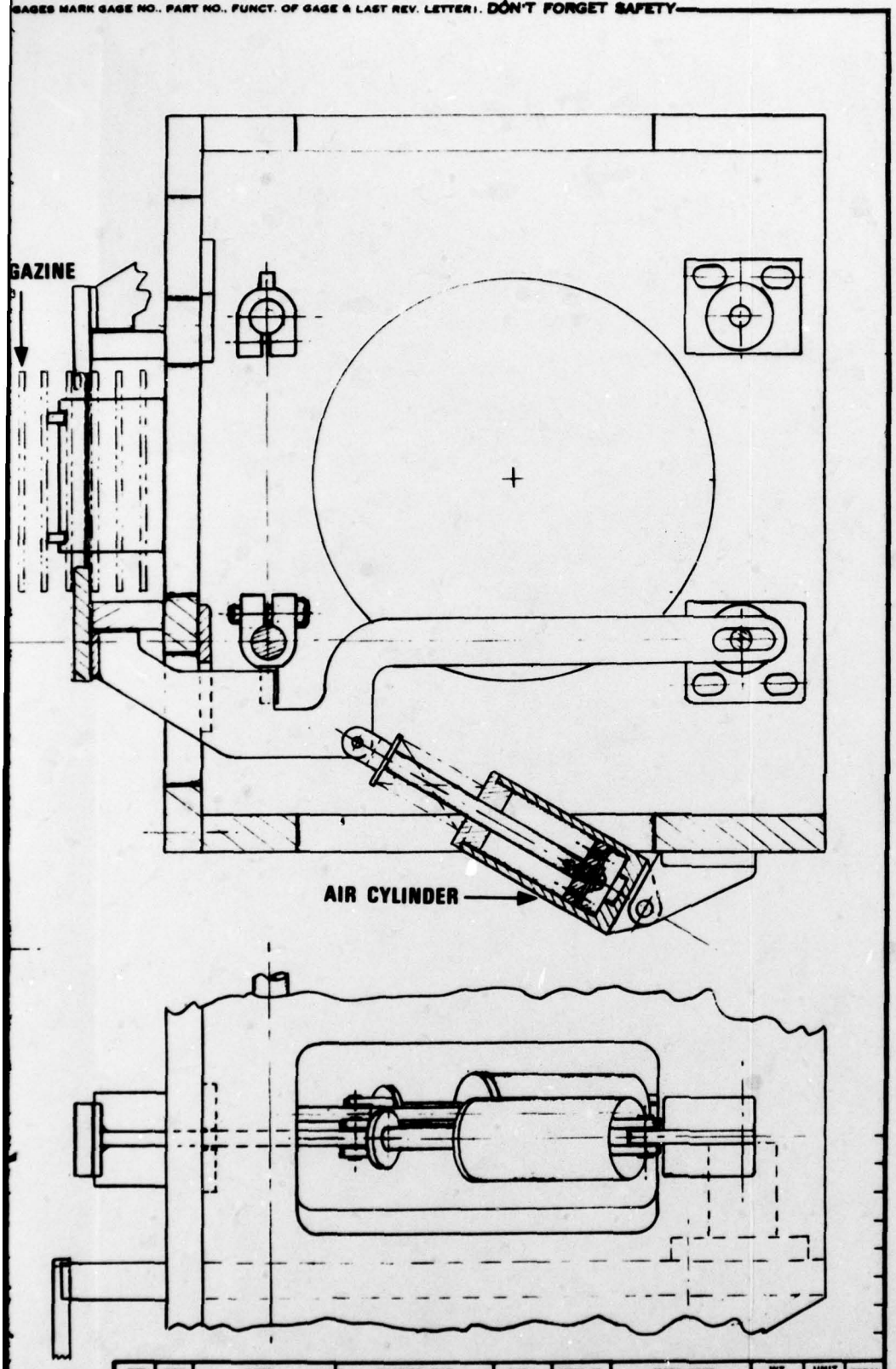


FIGURE 4. MAGAZINE INDEXING MECHANISM SYSTEM

Figure 5 shows an overall view of the system during check-out in the laboratory, prior to attachment of relays and controls. Figure 6 shows the system viewed from the rear. Note the extended magazine retrieval system and the fresh magazine waiting stack. The belt loading mechanism is shown in Figure 7. A detail of the index mechanism is shown in Figure 8. This mechanism works much like the escapement of a watch using the magazine separator ribs and a set of guide pins driven in and out by air. The magazine is fed through vertically by gravity action on its own weight. Figure 9 shows the system after mounting on the Lindberg Furnace complete with electrical and pneumatic control box. Figure 10 shows the substrate accumulator and belt placement mechanism. The same mechanism with the row spacing switch in the foreground is shown in Figure 11.

4. The Furnace Off Loader design has been completed. Ninety percent of the components have been machined and assembly of the system has been started.

5. The approach to the Dryer System has been altered significantly for the sake of simplicity and economy. Instead of taking the substrates out of the magazine and placing them on the dryer belt, a special oven will be designed and constructed which will hold eight magazines. The substrates will be dried in the oven while still in the magazines. At less than one-half hour drying time this approach will meet or exceed the required printing speed of 750 substrates per hour.

6. Browne On-Loader. Design is 10 percent complete, fabrication has not been started.

7. Browne Off-Loader. Design is 10 percent complete, fabrication has not been started.

8. Solder Reflow On-Loader. Design is 10 percent complete, fabrication has not been started.

9. Solder Reflow Off-Loader. Design is 10 percent complete, fabrication has not been started.

10. Automatic Wire Bonder will be supplied with an automatic substrate handling system through modification of the Welteck mechanical feed system.

NOTE: All work on the Material Handling System was temporarily suspended at the end of this reporting period pending approval of additional contract funding.

A7805 36

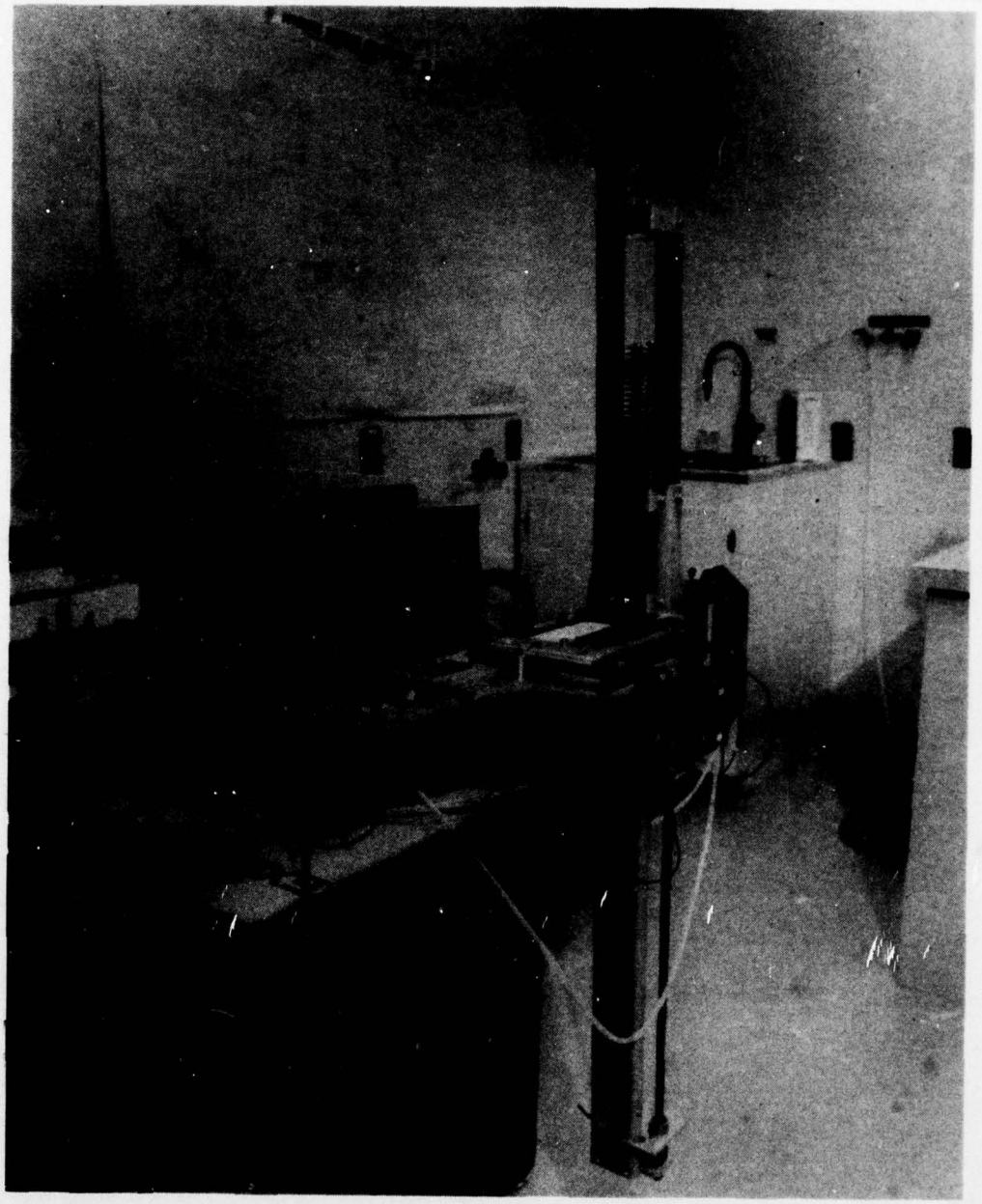


FIGURE 5. FURNACE ON-LOADER - OVERALL VIEW

A7805

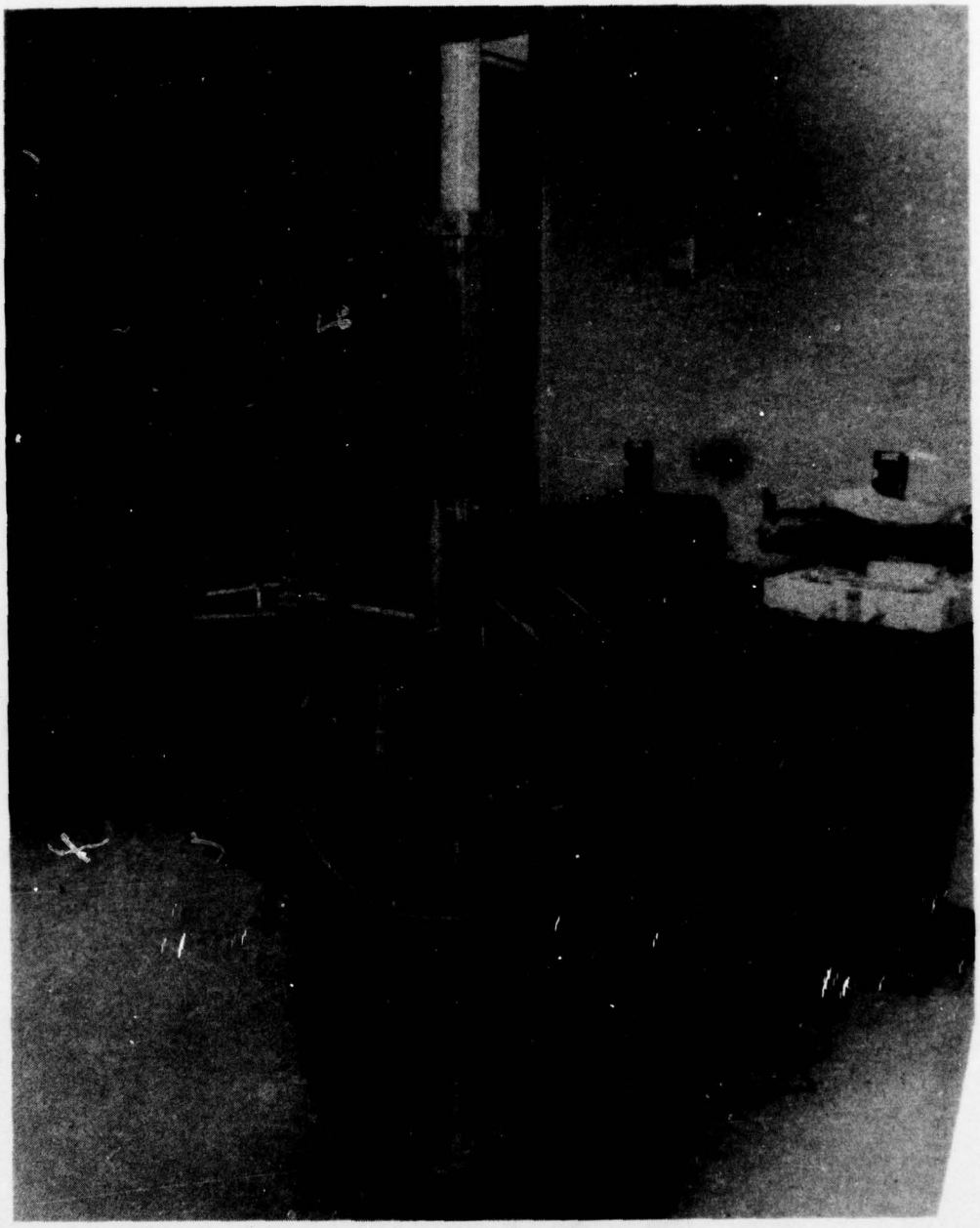


FIGURE 6. FURNACE ON-LOADER - REAR VIEW

A7805-38

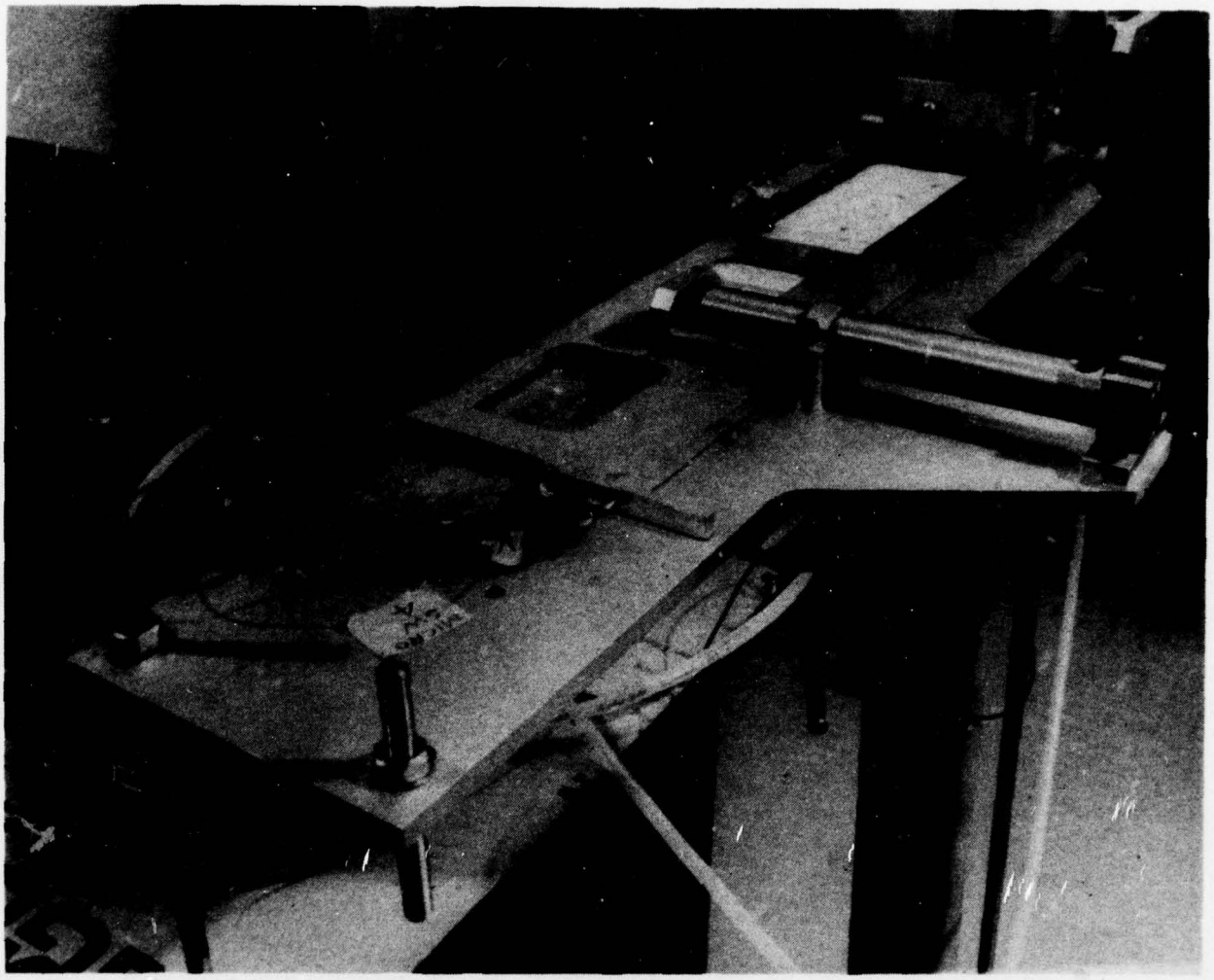


FIGURE 7. FURNACE ON-LOADER - BELT LOADING MECHANISM

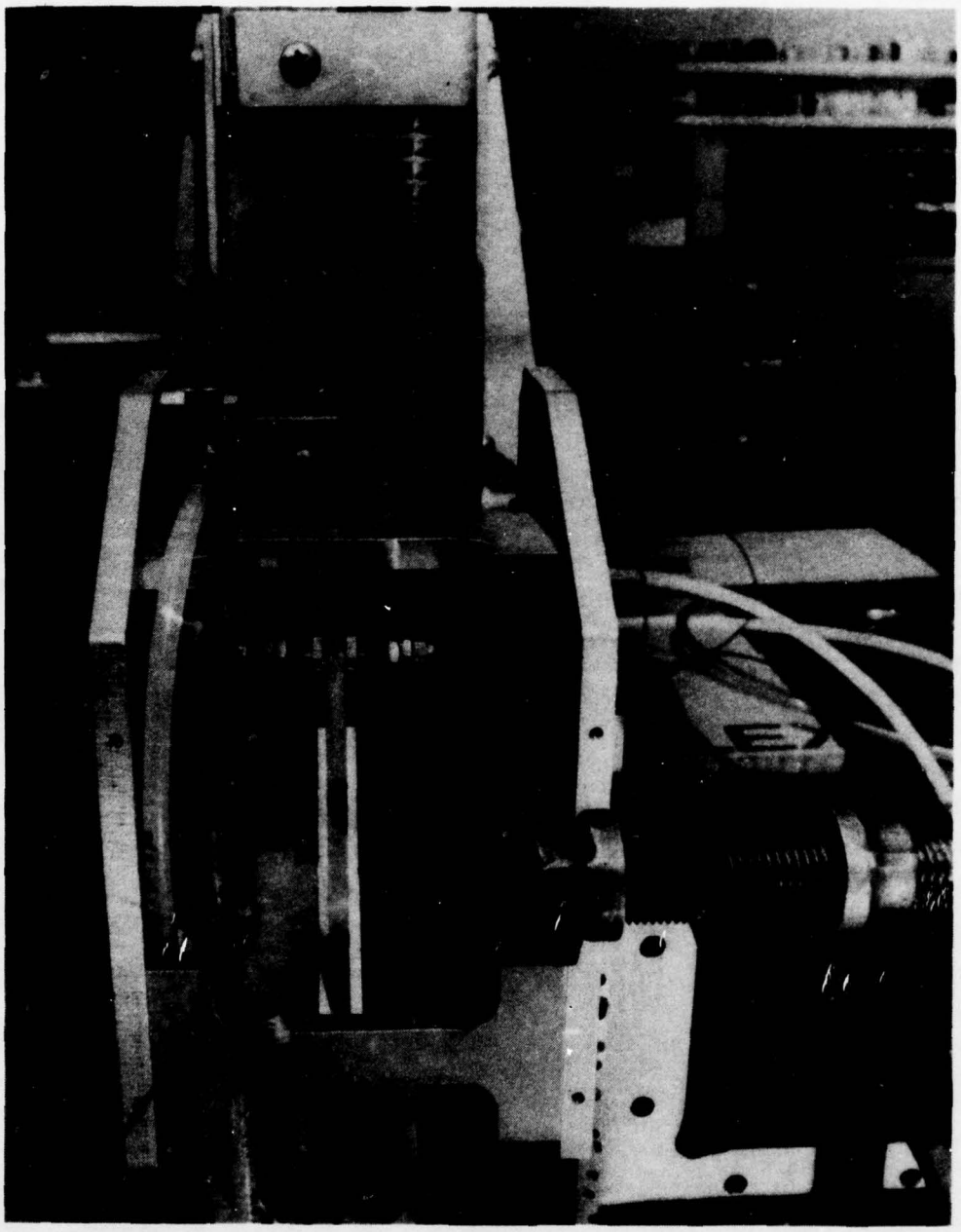


FIGURE 8. FURNACE ON-LOADER - INDEX MECHANISM

A7806-089

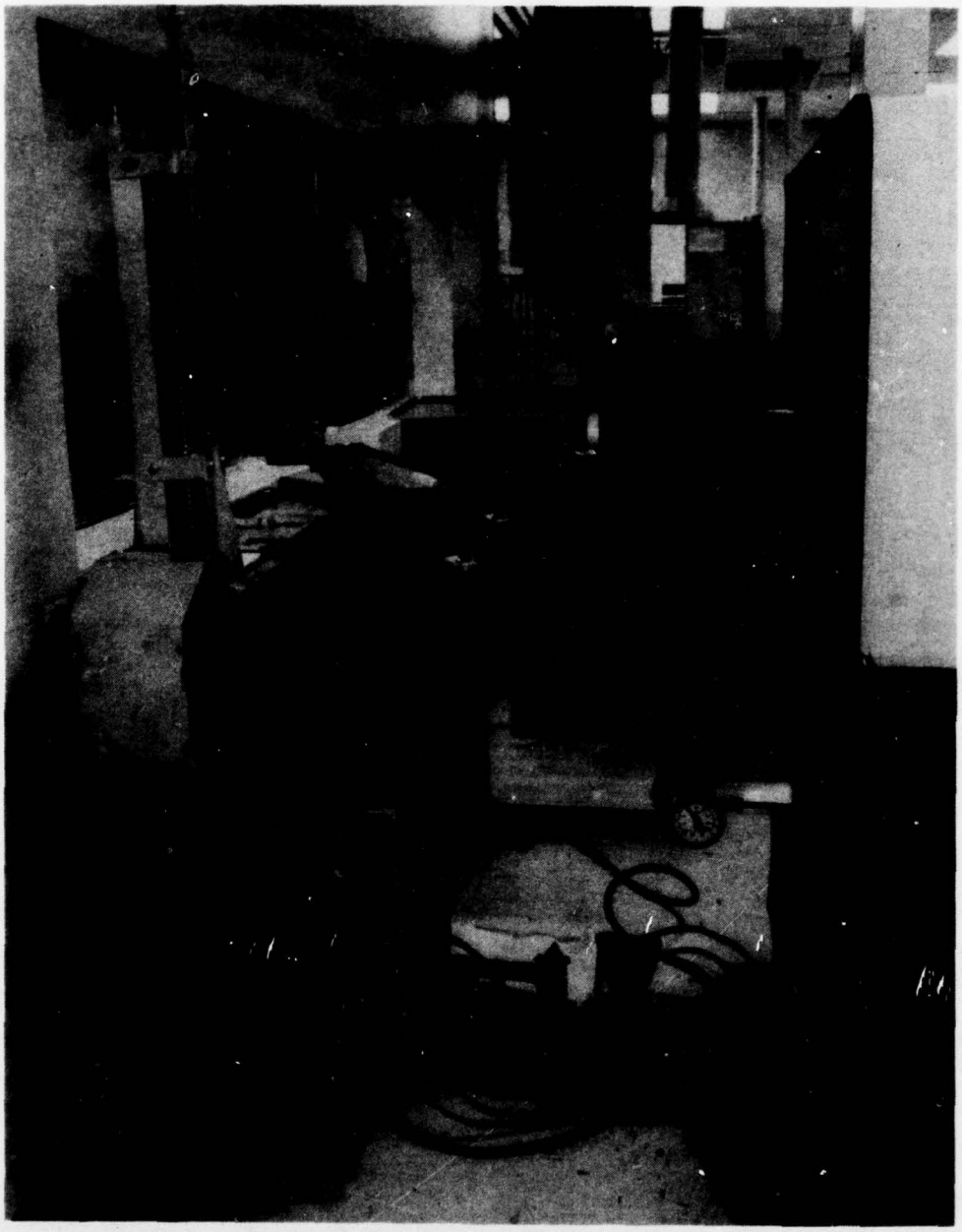


FIGURE 9. FURNACE ON-LOADER MOUNTED ON LINDBERG MODEL S-B FURNACE

A7806-087

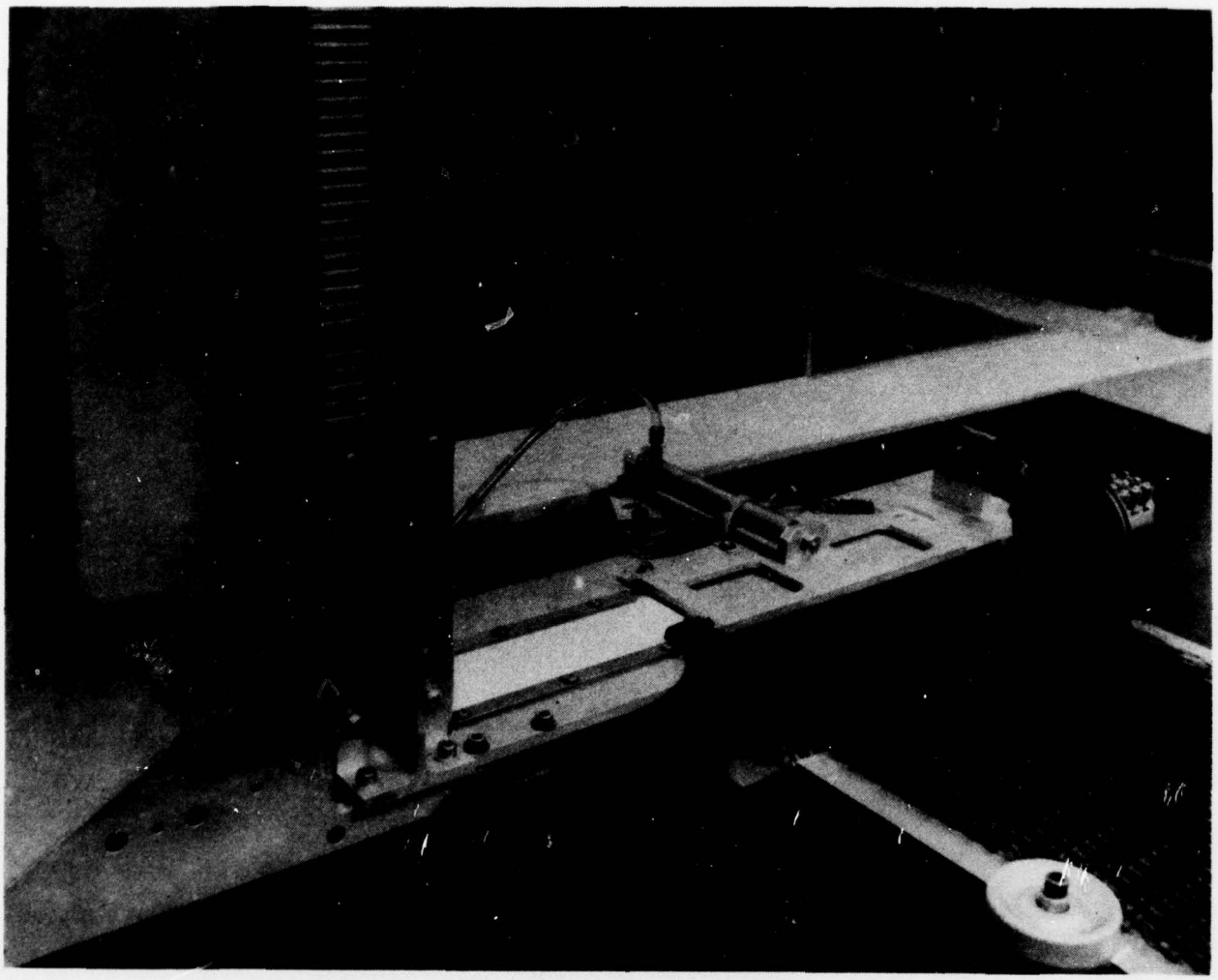


FIGURE 10. FURNACE ON-LOADER WITH SUBSTRATE ACCUMULATOR

A7806-088

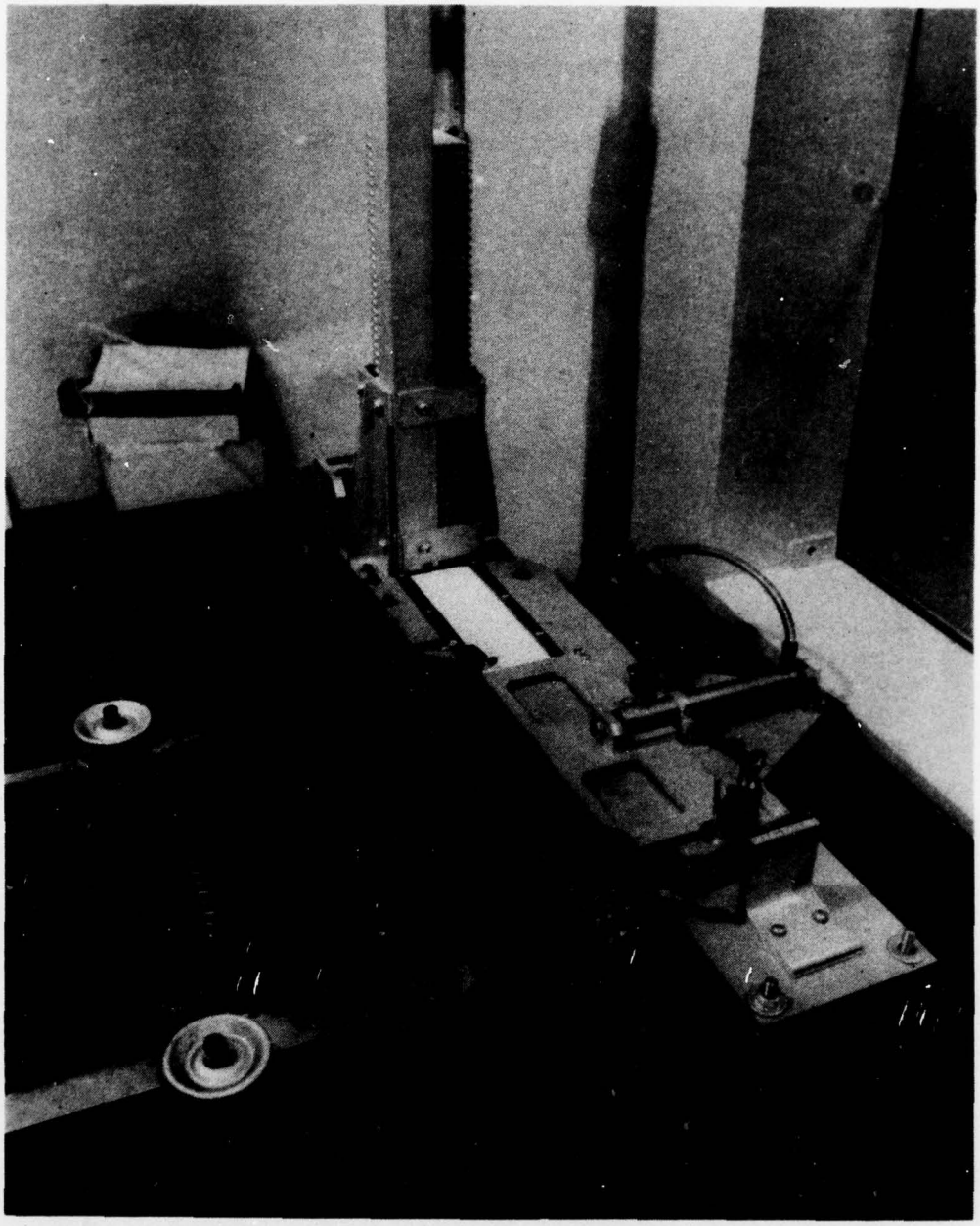


FIGURE 11. FURNACE ON-LOADER WITH ROW SPACING SWITCH

SECTION 2

BURN-IN SYSTEM

The burn-in tank design is complete and has been released to the machine shop for fabrication. Manufacturing of the tank is in the initial stages. Fabrication of the PC board mounting tray has been started and several piece parts have been completed.

The PC boards (P/N 34031328) have been built and delivered to Honeywell. Figure 12 shows a photograph of this PC board. The POGO pins will be inserted in the square array of small holes around the larger central holes. Additional interconnect runs are on the other side of the board.

The pump and filter to be used are on hand as they were previously used on the ERADCOM R&D Program (DAAB07-77-C-2708). A special T and valve connection to this system will be built.

The temperature controller was delivered to Honeywell as well (see Figure 13). This unit is similar to the one used on the above program and has worked very satisfactory.

Summarizing, the following major system components have been built or delivered and are ready for assembly.

1. PC Boards, P/N 3403128
2. Temperature Controller, Fenwal P/N 40-704011-425
3. Heater Pads for Tank
4. Relays and Housing
5. Tank Insulation

NOTE: All work on the Burn-In System was temporarily suspended at the end of this reporting period, pending approval of additional contract funding.

A7811-133

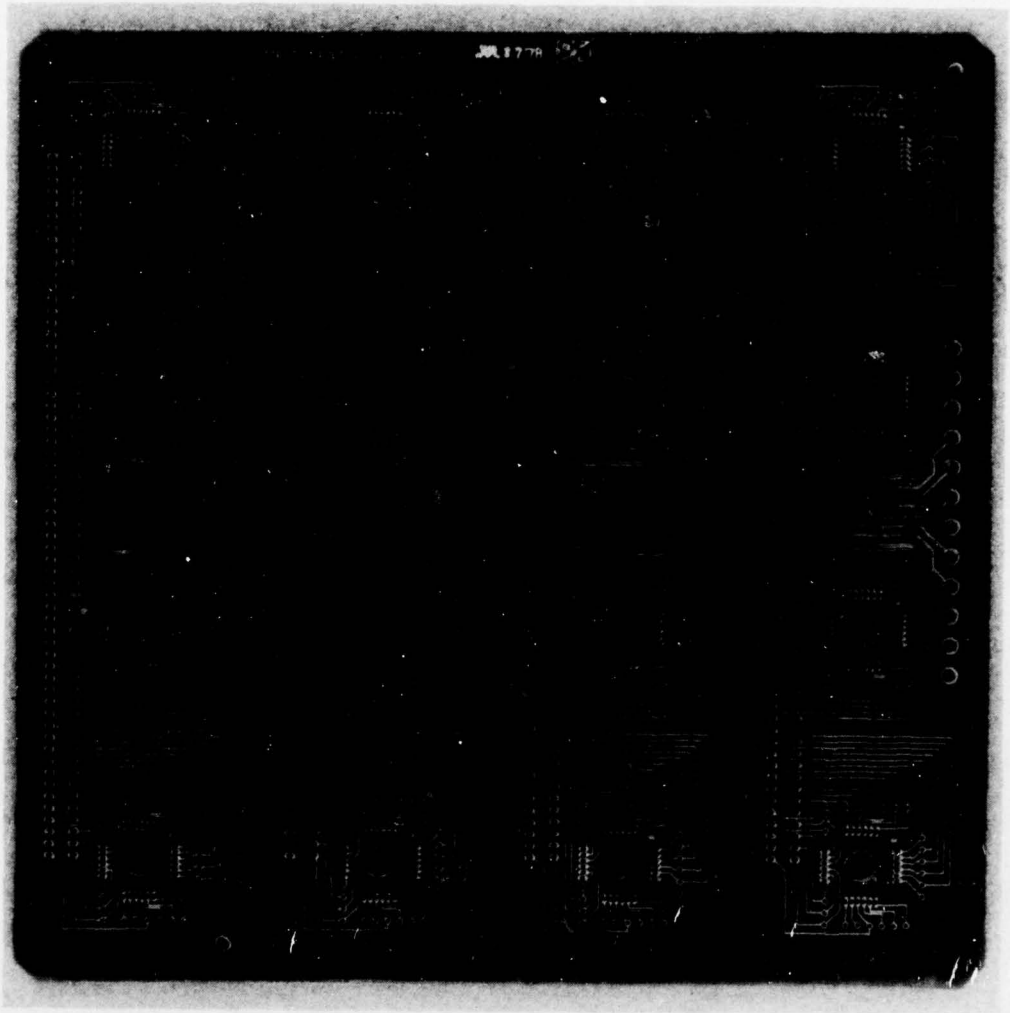


FIGURE 12. PC BOARD FOR BURN-IN SYSTEM

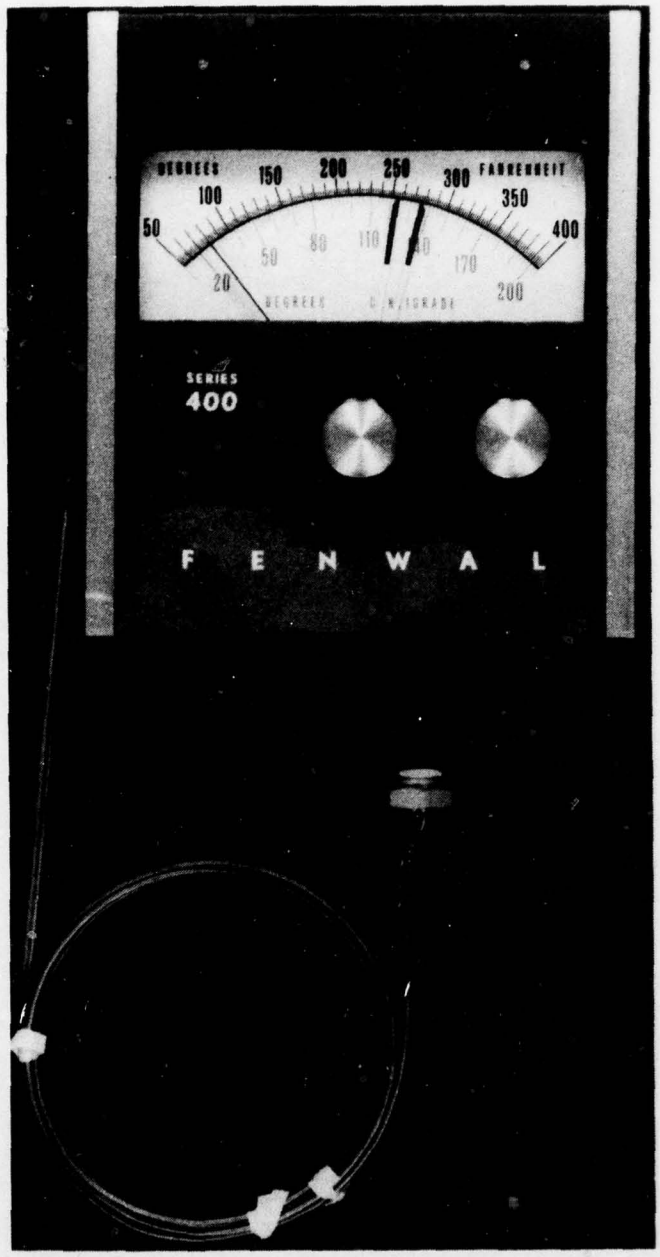


FIGURE 13. BURN-IN TANK TEMPERATURE CONTROLLER

SECTION 3

ENGINEERING SAMPLES

I. FIRST SUBMISSION

A. ELECTRONIC COMMUTATOR (34030402)

Five electrically and visually acceptable devices were shipped during a previous reporting period.

B. RANDOM ACCESS MEMORY (34030405)

Five electrically and visually acceptable devices were shipped during a previous reporting period.

C. MINILASER COUNTER (34030411)

Five electrically and visually acceptable devices were shipped during a previous reporting period.

D. SINCGARS DISCRIMINATOR (34030408)

Five electrically and visually acceptable devices were shipped during the previous reporting period.

E. CRYSTAL OSCILLATOR (34030417)

Five Oscillators have been successfully trimmed and tested and meet all specifications. Final testing with the Temperature Controller was successfully completed and the devices were shipped early in this reporting period. No further samples of this device type will be built during the remainder of this program per agreement with the ERADCOM Technical Director and the Procurement Specialist.

The test reports are contained in Appendix I of this report.

F. TEMPERATURE CONTROLLER (34030415)

Five Temperature Controllers have been successfully trimmed and tested and meet all specifications. Final testing with the Crystal Oscillator was successfully completed and the devices were shipped early during this reporting period.

The test reports for the Temperature Controller are contained in Appendix II of this report.

As with the Crystal Oscillator no further samples of this device type will be built during the remainder of this program.

II. SECOND SUBMISSION

A. ELECTRONIC COMMUTATOR (34030402)

Assembly of the Electronic Commutator samples is complete and the devices are in final test. Shipment is expected on or before the scheduled date (see Figure 14).

Several problems were experienced during assembly. The bump mask for the CD4051 chip contained an error which needed to be corrected. A new mask is on order, but will not arrive in time to be used on these samples.

Several significant milestones were reached during the assembly and test of these devices. Successful wafer bumping of CMOS wafers was accomplished. About 600 CMOS chips were successfully inner lead bonded to tape. Electrical testing of these chips on tape produced yields in the 80-90 percent range. This is the first time that CMOS devices have been successfully bumped and tested.

B. RANDOM ACCESS MEMORY (34030405)

The Random Access Memory (RAM) samples experienced several serious problems which have effected completion and delivery. A major problem was encountered when, early during this reporting period, it was discovered that the wafer manufacturer (Synertek Inc.) had shipped wafers with a redesigned chip (SY 2114/2082Z) rather than SY2114 used in the first engineering samples. This switch was made without notification to Honeywell and delivery was made several months after the wafers were ordered. Furthermore, the vendor destroyed masks and tooling so that new SY2114 wafers could not be built.

It was decided to keep the wafers with the 2082Z configuration chips. New matching tape, bump masks and thermodes were designed and ordered. After the redesigned lead frames and masks were received and matched to the 2082Z wafers it was discovered that several of the bump locations on the mask did not match the bonding pads on the chip. After checking back with Synertek, who had supplied the pad location data, they admitted an error was made in presenting the location data. A trip is planned to Synertek early during the next reporting period in order to obtain correct pad location data, as well as to discuss how such problems can be avoided in the future. Since once more new masks and tape have to be ordered, additional delays in the delivery of the RAM devices may be expected. Tentative estimates place delivery schedules in the October - November time frame (see Figure 15).

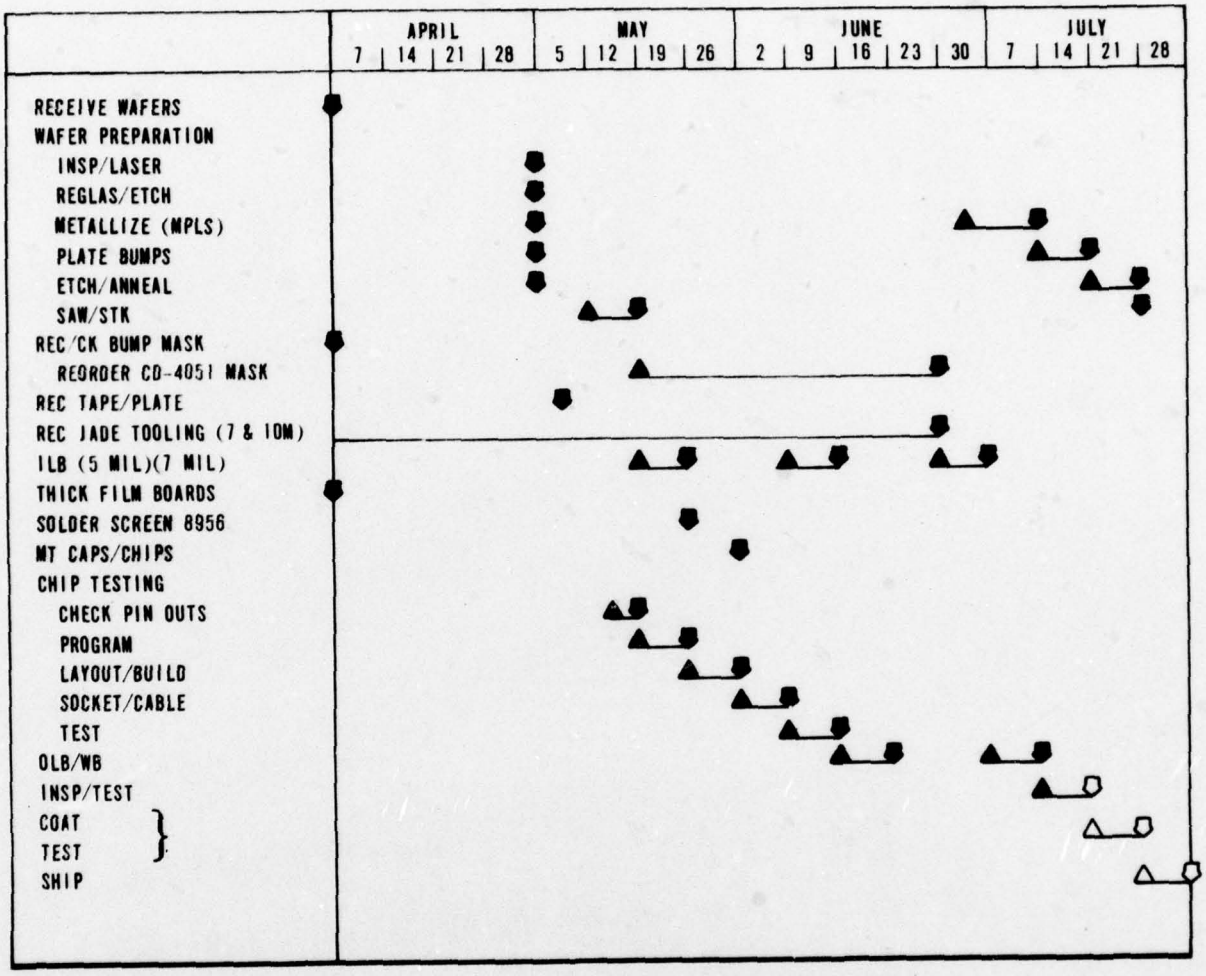


FIGURE 14. ELECTRONIC COMMUTATOR SCHEDULE

1278 828

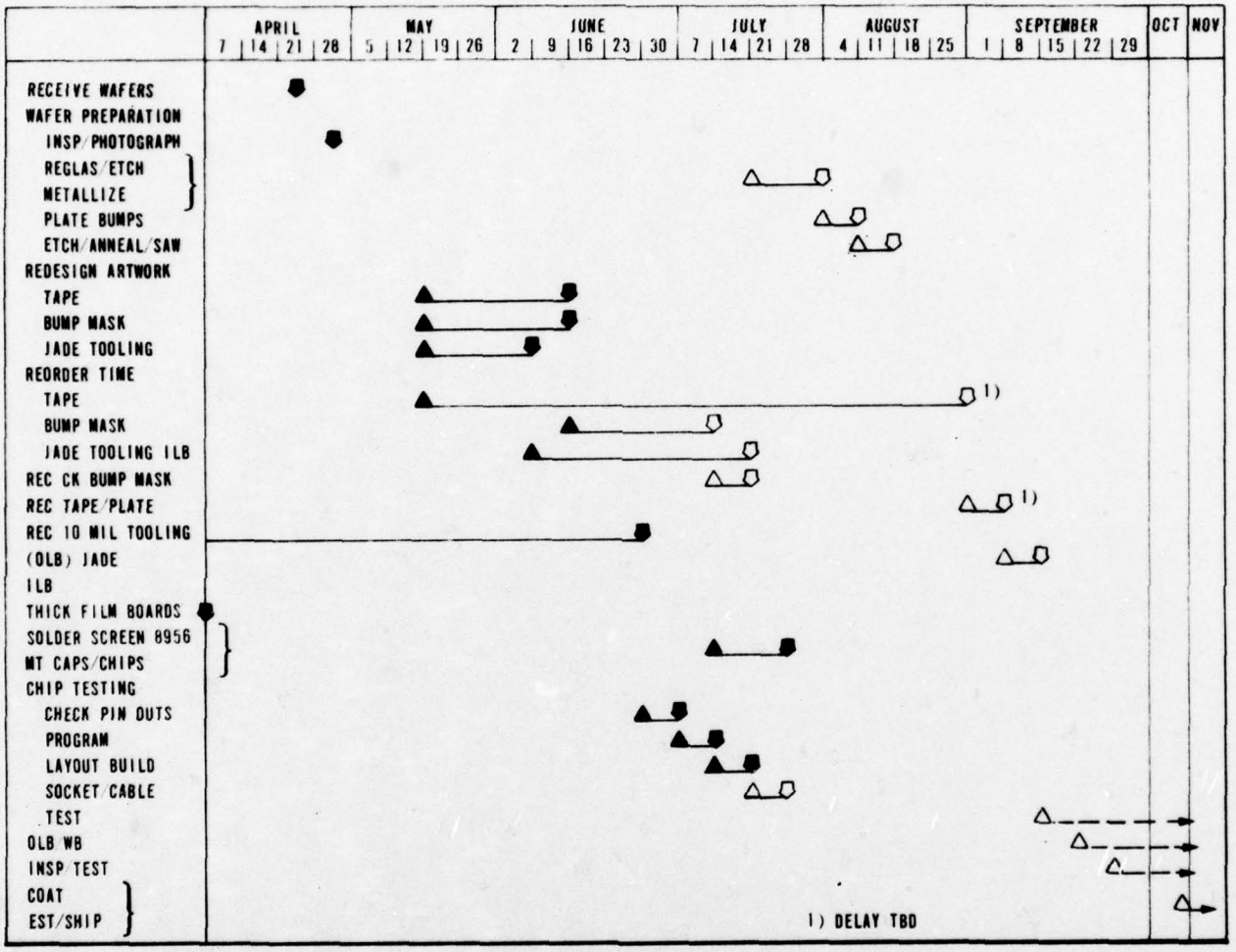


FIGURE 15. RAM SCHEDULE

C. MINILASER RANGEFINDER COUNTER (34030411)

Assembly of the Minilaser Rangefinder Counter devices is complete and the devices are in final test at the end of this reporting period. Shipment is expected early in the next reporting period (see Figure 16). During this period bumping of the following wafer types was accomplished: 54LS04, 54LS08, 54LS51, 54LS74, 54LS112, 54LS157 and 54LS160. Approximately 1000 chips total of these types were inner lead bonded and electrically tested on tape with yields ranging from 80-95 percent. Figure 17 shows a 54LS74 chip inner lead bonded on tape and after electrical testing.

D. SINCGARS DISCRIMINATOR (34030408)

Ten Discriminator samples completed assembly and testing during this reporting period, ahead of schedule (see Figure 18). Five visually acceptable and operational devices were shipped on 6 July 1978. This shipment marks a significant milestone in this program, as it includes the first TAB'ed* devices in this contract. Included in this shipment were serial numbers 101, 103, 105, 109 and 110, which met all specifications. Figure 19 shows a photograph of two completed SINCGARS Discriminator hybrids still attached on one substrate, but prescribed in preparation of snapping (separation). In addition to the electrically in-spec devices serial number 102 was shipped as a display sample. This device was operational, but with a slightly below spec output voltage at the center frequency. All other assembled devices were operational as well. During this reporting period both TC1125 and CA3130 (CMOS) wafers were bumped. Approximately 260 chips were inner lead bonded and tested on tape.

Appendix III includes the test reports for the five shipped devices identified by serial numbers.

*tape automatic bonded

1278-12B

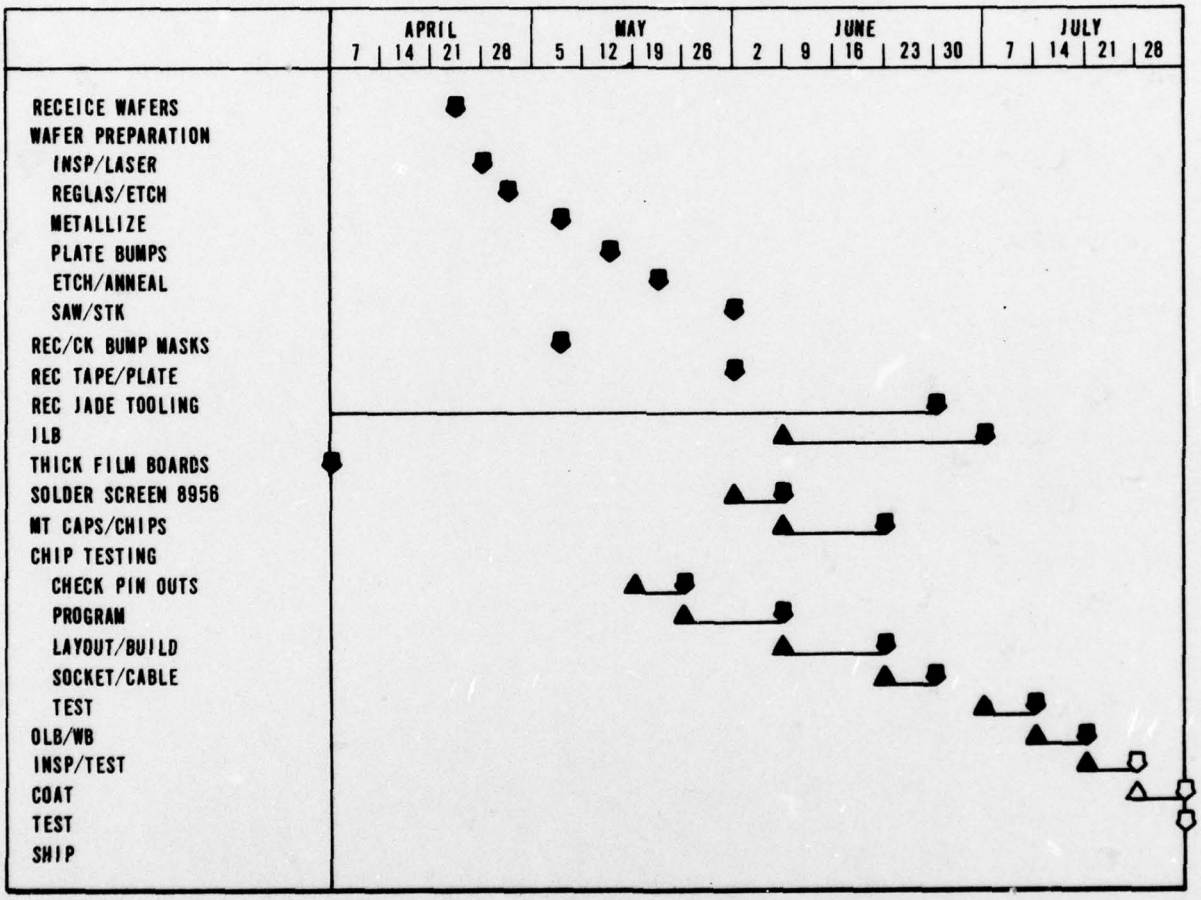


FIGURE 16. MINI-LASER COUNTER SCHEDULE

A7806-085

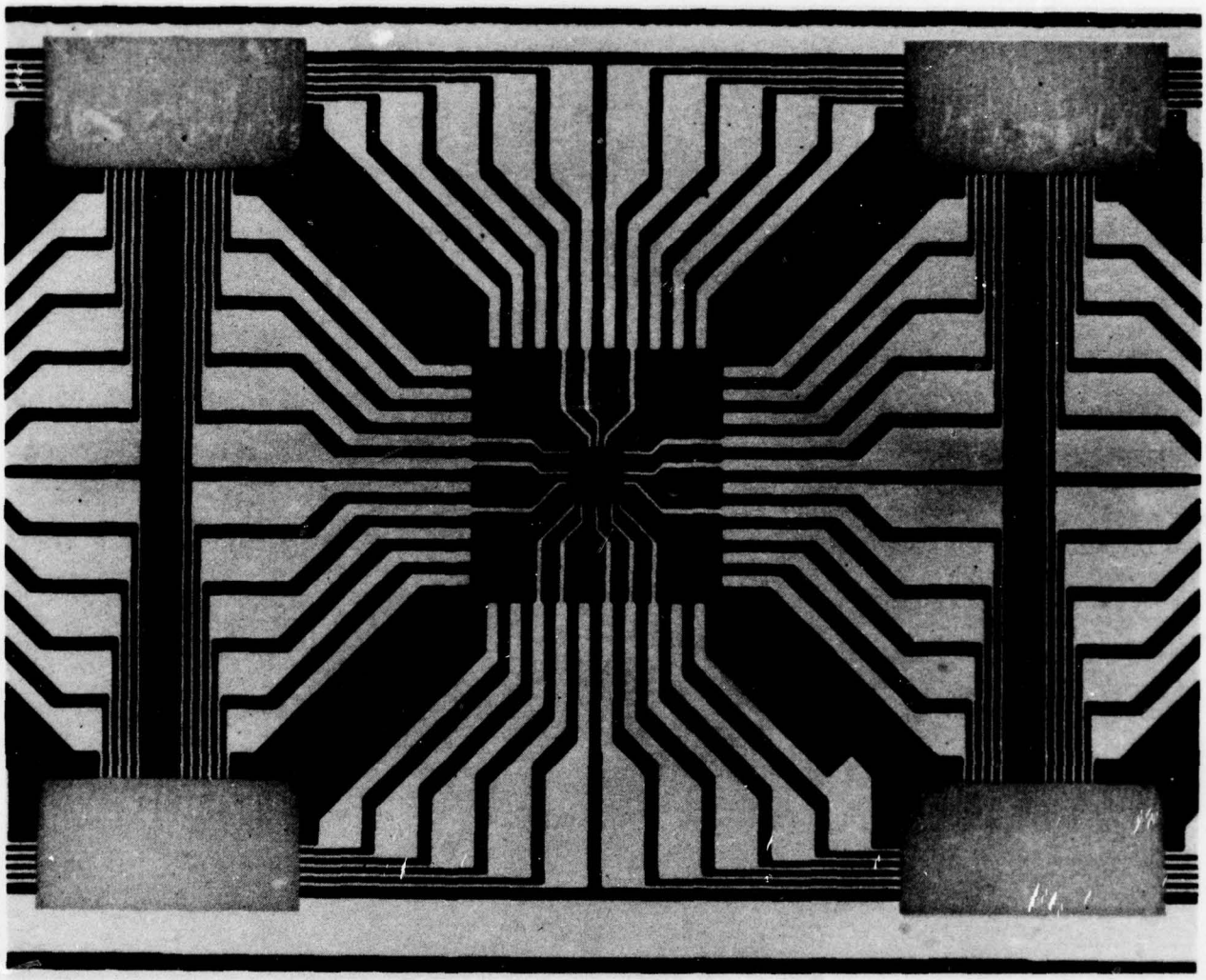


FIGURE 17. 54LS74 CHIP ON TAPE AFTER ELECTRICAL TEST

1278-078

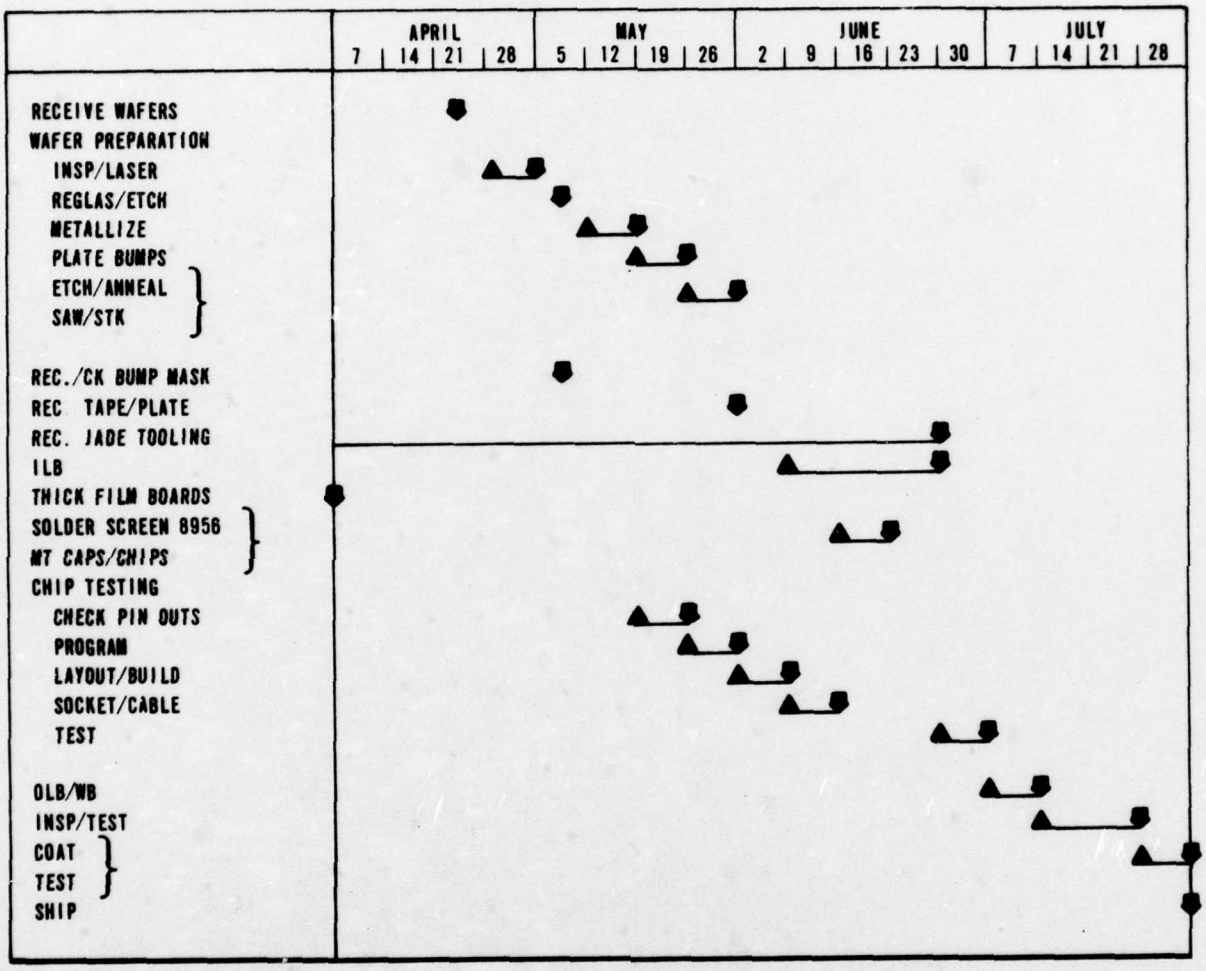


FIGURE 18. SINCGARS DISCRIMINATOR SCHEDULE

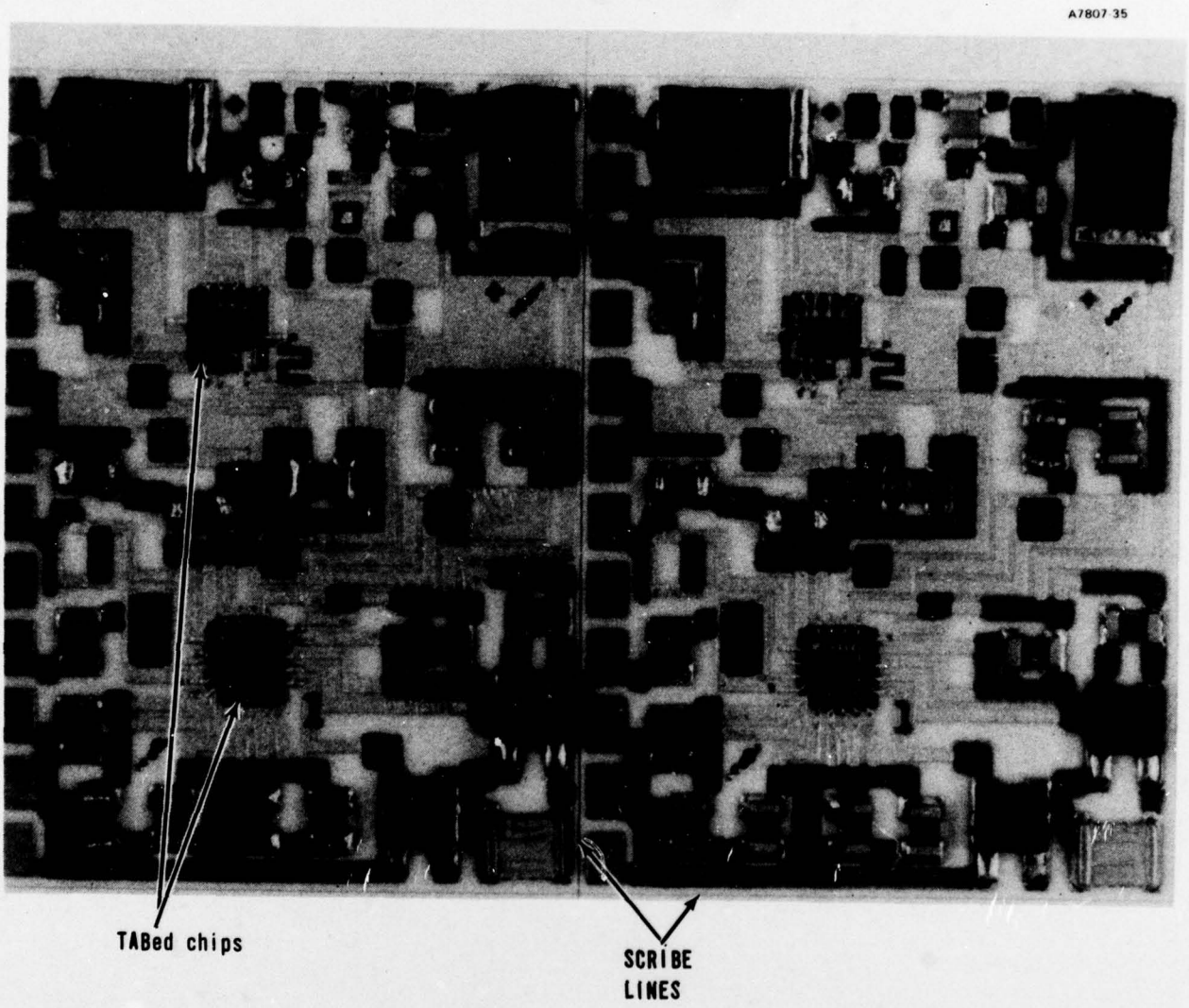


FIGURE 19. SINCGARS DISCRIMINATOR AFTER FINAL TEST
(TWO-UP)

SECTION 4

CONCLUSIONS

During this reporting period good progress continued in most areas of the program. The first Engineering Samples of the Crystal Oscillator and Temperature Controller circuits have been shipped. Also shipped were the first TAB'ed* devices, namely the Second Submission Samples of the SINCGARS Discriminator. Progress in assembling the TAB version of the Commutator and the Minilaser Counter is good. The RAM experienced a major problem in that new tape and masks had to be ordered twice due to an unannounced switch in device layout and further errors in pad location data. At the end of this reporting period all effort on the Material Handling System and the Burn-In System was temporarily suspended, pending a request for additional funding.

*tape automatic bonded

SECTION 5

PLANS FOR THE NEXT REPORTING PERIOD

During the next reporting period Second Engineering Samples of the Electronic Commutator and Minilaser Counter devices will be assembled, tested and shipped. A trip will be made to Synertek to obtain correct pad location data and to explore better ways to extract and transfer this data without possibility of error. Tape and bump masks for the RAM will be reordered and a new schedule will be established. Preparatory work for the build and assembly of the Confirmatory Samples will be initiated. Discussion and negotiations in order to obtain additional contract funding will continue.

SECTION 6

PUBLICATIONS

1. The following paper was presented at the 1978 (28th) Electronics Components Conference and published in its Proceedings on April 24, 1978 in Anaheim, CA: "Lead Forming and Outer Lead Bond Pattern Design for Tape Bonded Hybrids", by William R. Rodrigues de Miranda, and Dr. Rudolph G. Oswald of Honeywell Inc., and Don Brown of the Jade Corporation.

2. The following paper was presented at the Symposium on Plastic Encapsulated/Polymer Sealed Semiconductor Devices for Army Equipment and published in its Proceedings on May 10, 1978 at Fort Monmouth NJ: "Automated Tape Carrier Bonding for Hybrids" by Dr. Rudolph G. Oswald, William R. Rodrigues de Miranda and James M. Montante.

Appendix I

Universal Report No. _____ Originator's Report No. Oscillator -001

Revision _____

REPORT OF TEST ON Crystal Oscillator - First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal Report No. _____ Originator's Report No. Oscillator - 001

Revision _____

REPORT OF TEST ON Crystal Oscillator - First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

	Date	Signature	
Test Initiated	5/10/78		
Test Completed	5/11/78		
Report Written By	5/12/78	S. Jones: S. Jones	
Technician			
Test Engineer		S. Jones	
Supervisor	5/12/78	W. Miranda: John R. Miranda	
Supervisor			
Government Repr. (if applicable)			
Final Release	5/12/78		

1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ERADCOM under Contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the specifications listed in paragraph 1.3.2.

1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3.

Equipment Used	Model #	HI ID #	Last Calibrated	Due for Calibration
Ambitrol Twin Power Supply	TW-5005	CG1804-40	9/6/77	9/6/78
Ambitrol Twin Power Supply	TW-5005	CG1804-37	11/4/77	11/4/78
Fluke Digital Multimeter	8600A	CG13567	12/6/77	7/6/78
Fluke Digital Counter-Timer	1952A	CG12097	11/16/77	5/16/78
General Radio Decade Resistor	1434-M	X-289	11/14/77	11/14/79
Exact Signal Generator	124	CG12041	1/10/78	1/10/79

NOTE: The power supply output levels were set with the aid of the Fluke Digital Multimeter.

1.3 Test Procedure

1.3.1 Functional Trim

The functional trim procedure and trim results are contained in Appendix A, for Serial Numbers 7, 8, 11, 14 and 15.

1.3.2 Acceptance Test Specifications

The Crystal Oscillator (D34030418) shall be acceptance tested in conjunction with the Temperature Controller (D34030415). Refer to Test Report Number Controller -001 for further details.

The Temperature Controller/Crystal Oscillator circuit shall exhibit a frequency change of less than $\pm$ 20 parts per million over the temperature range of -40°C to +75°C at center frequency.

1.4 Test Data

The five engineering samples being delivered passed the tests specified in paragraph 1.3.2. Test Data sheets which contain the test results for Serial Numbers 7, 8, 11, 14 and 15 are attached.

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 7

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 7

Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

13,960	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,234	21,937,509
Freq. @ -40°C	Freq. @ 40°C
21,937,320	21,937,521
Freq. @ -30°C	Freq. @ 50°C
21,937,371	21,937,520
Freq. @ -20°C	Freq. @ 60°C
21,937,444	21,937,473
Freq. @ 0°C	Freq. @ 70°C
21,937,499	21,937,426
Freq. @ 20°C	Freq. @ 75°C

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 8

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 8

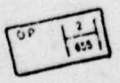
Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

14,420	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,290	21,937,505
Freq. @ -40°C	Freq. @ 40°C
21,937,353	21,937,506
Freq. @ -30°C	Freq. @ 50°C
21,937,395	21,937,507
Freq. @ -20°C	Freq. @ 60°C
21,937,468	21,937,476
Freq. @ 0°C	Freq. @ 70°C
21,937,499	21,937,430
Freq. @ 20°C	Freq. @ 75°C



TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 11

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 11

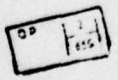
Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

1,875	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,432 Freq. @ -40°C	21,937,440 Freq. @ 40°C
21,937,529 Freq. @ -30°C	21,937,401 Freq. @ 50°C
21,937,578 Freq. @ -20°C	21,937,357 Freq. @ 60°C
21,937,559 Freq. @ 0°C	21,937,335 Freq. @ 70°C
21,937,499 Freq. @ 20°C	21,937,338 Freq. @ 75°C



TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 14

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 14

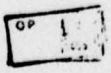
Date of Test 5-10-78

1. Center Frequency Adjust at Room Ambient

13,850	21,937,494
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,301 Freq. @ -40°C	21,937,503 Freq. @ 40°C
21,937,353 Freq. @ -30°C	21,937,500 Freq. @ 50°C
21,937,388 Freq. @ -20°C	21,937,485 Freq. @ 60°C
21,937,444 Freq. @ 0°C	21,937,434 Freq. @ 70°C
21,937,494 Freq. @ 20°C	21,937,384 Freq. @ 75°C



TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 15

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 15

Date of Test 5-10-78

1. Center Frequency Adjust at Room Ambient

14,236	21,937,500
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,401	21,937,506
Freq. @ -40°C	Freq. @ 40°C
21,937,425	21,937,509
Freq. @ -30°C	Freq. @ 50°C
21,937,447	21,937,500
Freq. @ -20°C	Freq. @ 60°C
21,937,470	21,937,461
Freq. @ 0°C	Freq. @ 70°C
21,937,500	21,937,425
Freq. @ 20°C	Freq. @ 75°C

APPENDIX A

CRYSTAL OSCILLATOR NETWORK ADJUSTMENT AND TRIM PROCEDURE

1. Digital Deviation

Object: Adjust U2 voltage level such that TPI difference voltage, corresponding to logic 0 and 1 inputs at the E_{DIG} interconnect (Pin 3) equals 1.250 V $\pm$ 0.002V

Conditions:
a) Regulated 9V $\pm$ .001V across 9V interconnect (Pin 8) and ground.
b) DVM across TPI interconnect (Pin 4) and ground.
c) 25K ohm potentiometer across Fadj (Pin 7) and ground.
d) 3.5V across E_{COMP} interconnect (Pin 6) and ground.
e) E_{CNTRL} (Pin 2) = E_{ANLG} (Pin 5) = 0V (interconnects at ground potential.
f) E_{DIG} (Pin 3) = 5V

Trim Procedure:

1.1 Connect 9.000 $\pm$ 0.001 Vdc Power Supply to the 9V and GND jacks on the trim test box.

1.2 Connect 5.000 $\pm$ 0.005 Vdc Power Supply to the 5V and GND jacks on the trim test box.

1.3 Connect 3.500 $\pm$ 0.005 Vdc Power Supply to the 3.5V and GND jacks on the trim test box.

1.4 Connect a General Radio, Model 1434-M or equivalent, decade resistor box to the 25K POT HI and LO jacks on the trim test box.

1.5 Connect the DVM to the DVM HI and LO jacks on the trim test box.

1.6 Set the test select switch on the trim test box to postion 2.

1.7 Adjust the decade resistor for a reading of 4.000 $\pm$ 0.001 Vdc on the DVM.

1.8 Set the test select switch on the trim test box to position 3.

1.9 Trim R14 or R15 as follows:

If DVM $<$ 2.749 Vdc, trim R14
If DVM $>$ 2.751 Vdc, trim R15

2. Analog Center Frequency

Object: Adjust U1 voltage level such that TP1 difference voltage, corresponding to logic 0 and 1 inputs at the E_{CNTRL} (Pin 2) interconnect, equals 0.625 ± 0.002V.

Conditions:
a) Regulated 9V ± .001V across 9V interconnect (Pin 8) and ground.
b) DVM across TP1 interconnect (Pin 4) and ground.
c) 25K ohm potentiometer across Fadj (Pin 7) and ground.
d) 3.5V across E_{COMP} interconnect and ground.
e) E_{ANLG} (Pin 5) = E_{DIG} = 0V (ground potential).
f) E_{CNTRL} (Pin 2) = 5V.

Trim Procedures

2.1 Set the test select switch on the trim test box to position 4.

2.2 Adjust the decade resistor for a reading of 4.125 ± 0.001 Vdc on the DVM.

2.3 Set the test select switch on the trim test box to position 5.

2.4 Trim R12 or R13 as follows:

If DVM < 3.499 Vdc, trim R13
If DVM > 3.501 Vdc, trim R12

3. Analog Deviation

Object: Adjust R1 summing resistor such that analog voltage gain at U3 equals 1.0 ± 5%.

Conditions:
a) Regulated 9V ± .001V across 9V interconnect (Pin 8) and ground.
b) DVM (AC/DC) across TP1 interconnect (Pin 4) and ground.
c) 25K ohm potentiometer across Fadj (Pin 7) and ground.
d) 3.5V across E_{COMP} interconnect and ground.
e) E_{CNTRL} (Pin 2) = 5V
f) E_{ANLG} (Pin 5) = E_{DIG} (Pin 3) = 0V (ground potential).

Trim Procedure:

3.1 Set the test select switch on the trim test box to position 6.

3.2 Adjust the decade resistor for a reading of 3.500 ± 0.001 Vdc on the DVM.

3.3 Set the test select switch on the trim test box to position 7.

3.4 Connect a 1.00 + 0.02 Vrms, 1KHz, signal generator to the 1 KHz HI and LO jacks on the trim test box.

3.5 Trim R1 to obtain a reading of 1.00 ± 0.02 Vrms on the DVM.

4. Compensation Grain

Object: Adjust R2 summing resistor such that temperature compensation voltage gain at U3 equals Fx/Fs volts, where Fx is the nominal frequency of the assigned crystal and Fs is the nominal frequency of the crystal from which the standard cubic correction function was derived. Fs = 19.88 MHz for compensation DGF resistor values in TCVCXO Schematic ES-C-215261.

Conditions:
a) Regulated 9V ± .001V across 9V interconnect (Pin 8) and ground.
b) DVM (AC/DC) across TPI interconnect (Pin 4) and ground.
c) 25K ohm potentiometer across Fadj (Pin 7) and ground.
d) E_{CNTRL} (Pin 2) = 5V.
e) E_{DIG} (Pin 3) = E_{ANLG} (Pin 5) = 0V (ground potential)
f) E_{COMP} = 3.5Vdc

Trim Procedure:

4.1 Set the test select switch on the trim test box to position 8.

4.2 Adjust the decade resistor for a reading of 3.500 ± 0.001 Vdc on the DVM.

4.3 Set the test select switch on the trim test box to position 9.

4.4 Trim R2 to obtain Fx/Fs ± 0.02 Vrms on the DVM.

4.5 Disconnect the signal generator from the 1KHz HI and LO jacks on the trim test box.

5. F/V Linearization

Object: Adjust linearization DFG segment gains to linearize VCXO frequency/voltage tuning characteristic for a slope of 500Hz/V.

Conditions:
a) Regulated 9V ± .001V across 9V interconnect (Pin 8) and ground.
b) 25K ohm potentiometer across Fadj (Pin 7) and ground.
c) 1K ohm load and frequency counter across RF (Pin 9) and ground.
d) Crystal connected across Pin 14 and 16.
e) DVM at E_O (term. 6, U4) and at TPI (Pin 4).

Trim Procedure:

5.1 Set the test select switch on the trim test box to position 10.

5.2 Adjust the decade resistor for a reading of 1.500 ± 0.001 Vdc on the DVM.

5.3 Set the test select switch on the trim test box to position 11.

5.4 Trim R7 or R10 as follows:

If DVM $>$ 1.001 Vdc, trim R7
If DVM $<$ 0.999 Vdc, trim R10

5.5 Connect digital counter to FREQ OUT jacks on the trim test box and record the frequency (F_{REF}).

5.6 Set the test select switch on the trim test box to position 10.

5.7 Adjust the decade resistor for a reading of 3.500 $\pm$ 0.001 Vdc on the DVM.

5.8 Set the test select switch on the trim test box to position 11 and note frequency F_1.

5.9 Trim R5 or R8 as follows:

If $(F_1 - F_{REF}) <$ 998 Hz, trim R5
If $(F_1 - F_{REF}) >$ 1002 Hz, trim R8

5.10 Set the test select switch on the trim test box to position 10.

5.11 Adjust the decade resistor for a reading of 5.500 $\pm$ 0.001 Vdc on the DVM.

5.12 Set the test select switch on the trim test box to position 11 and note frequency F_2.

If $(F_2 - F_{REF}) <$ 1998 Hz, trim R4
If $(F_2 - F_{REF}) >$ 2002 Hz, trim R9

TABLE I - FUNCTIONAL TRIM RESULTS

S/N	Digital Deviation 2.750±0.001Vdc	Analog Center Frequency 3.500±0.001Vdc	Analog Deviation 1.00±0.02Vrms	Comp. Gain 1.10±0.02Vrms	F/V Linearization 1.000±0.001Vdc 500Hz/V
7	2.750	3.499	0.984	1.10	1.000Vdc F_{REF} 21,936,399 F_1 21,937,397 F_2 21,938,399
8	2.750	3.500	0.994	1.11	1.001 Vdc F_{REF} 21,936,495 F_1 21,937,496 F_2 21,938,496
11	2.750	3.501	0.993	1.10	1.000Vdc F_{REF} 21,936,678 F_1 21,937,679 F_2 21,938,679
14	2.751	3.501	0.989	1.10	1.000Vdc F_{REF} 21,936,552 F_1 21,937,552 F_2 21,938,552
15	2.750	3.501	0.990	1.10	1.001Vdc F_{REF} 21,936,403 F_1 21,937,401 F_2 21,938,402

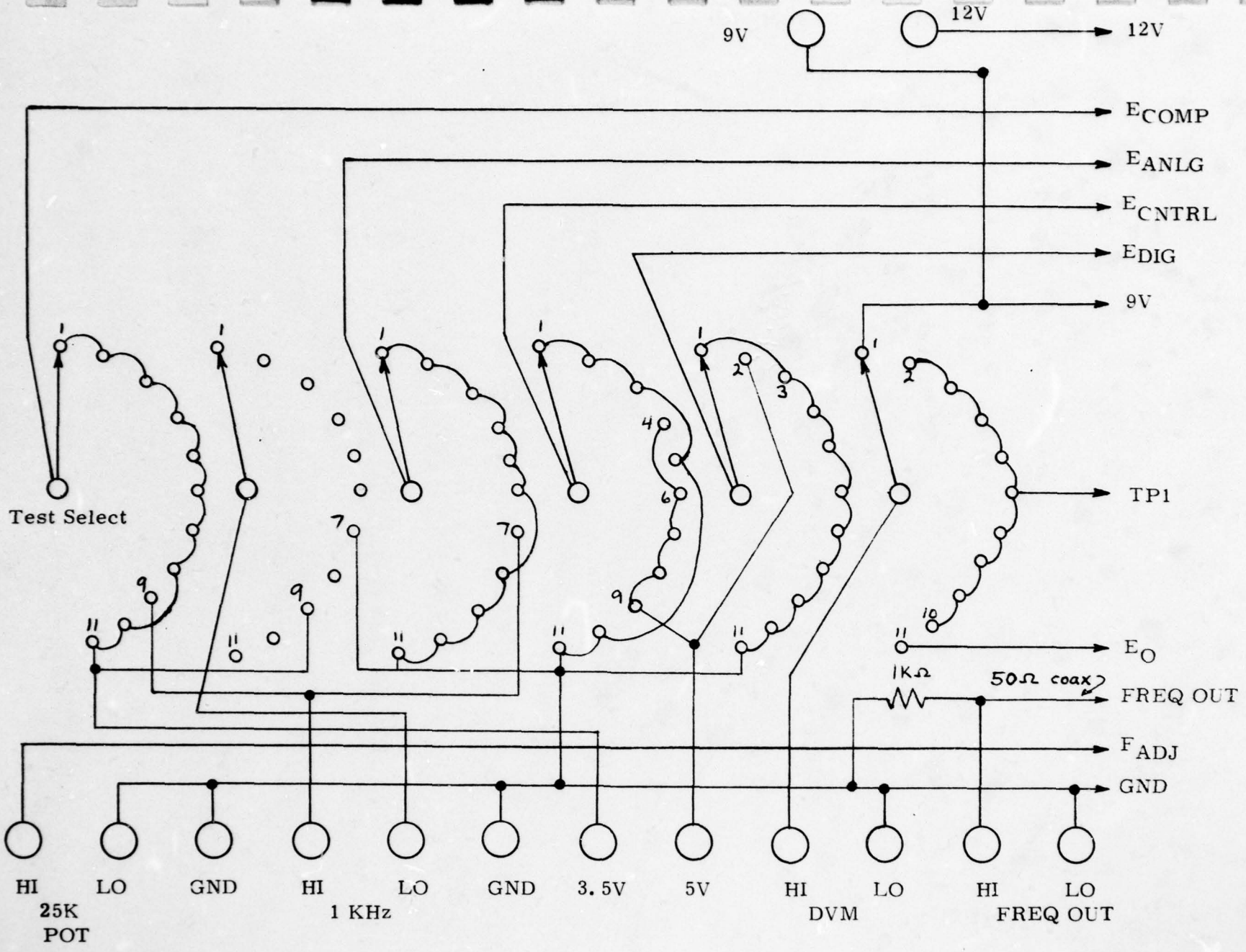


FIGURE 1 - SCHEMATIC TRIM TEST BOX

Appendix II

Universal
Report No. _____

Originator's
Report No. Controller-001

Revision _____

REPORT OF TEST ON Temperature Controller-First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal
Report No. _____

Originator's
Report No. Controller-001

Revision _____

REPORT OF TEST ON Temperature Controller-First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

	Date	Signature	
Test Initiated	5/10/78		
Test Completed	5/11/78		
Report Written By	5/12/78	S. Jones: S Jones/ilbw	
Technician			
Test Engineer		S. Jones ilbw	
Supervisor	5/12/78	W. Miranda Wm R. Miranda	
Supervisor			
Government Repr. (if applicable)			
Final Release	5/12/78		

1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ERADCOM under Contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the specifications listed in paragraph 1.3.2.

1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3.

Equipment Used	Model#	HI ID#	Last Calibrated	Due for Calibration
Ambitrol Twin Power Supply	TW-5005	CG1804-40	9/6/77	9/6/78
Ambitrol Twin Power Supply	TW-5005	CG1804-37	11/4/77	11/4/78
Fluke Digital Multimeter	8600A	CG13567	12/6/77	7/6/78
Fluke Digital Counter-Timer	1952A	CG12097	11/16/77	5/16/78
General Radio Decade Resistor	1434-M	X-289	11/14/77	11/14/79
Exact Signal Generator	124	CG12041	1/10/78	1/10/79

NOTE: The power supply output levels were set with the aid of the Fluke Digital Multimeter.

1.3 Test Procedure

1.3.1 Functional Trim

The functional trim procedure and trim results are contained in Appendix A, for Serial Numbers 7, 8, 11, 14 and 15.

1.3.2 Acceptance Test Specifications

The Temperature Controller (D34030415) shall be acceptance tested in conjunction with the Crystal Oscillator (D34030418). Refer to Test Report Number, Oscillator-001 for further details.

The Temperature Controller/Crystal Oscillator circuit shall exhibit a frequency change of less than $\pm$ 20 ppm over the temperature range of $-40^{o}C$ to $+75^{o}C$, at center frequency.

1.4 Test Data

The five engineering samples being delivered passed the tests specified in paragraph 1.3.2. Test data sheets which contain the test results for Serial Numbers 7, 8, 11, 14 and 15 are attached.

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 15

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 15

Date of Test 5-10-78

1. Center Frequency Adjust at Room Ambient

14,236	21,937,500
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,401 Freq. @ -40°C	21,937,506 Freq. @ 40°C
21,937,425 Freq. @ -30°C	21,937,509 Freq. @ 50°C
21,937,447 Freq. @ -20°C	21,937,500 Freq. @ 60°C
21,937,470 Freq. @ 0°C	21,937,461 Freq. @ 70°C
21,937,500 Freq. @ 20°C	21,937,425 Freq. @ 75°C

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 14

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 14

Date of Test 5-10-78

1. Center Frequency Adjust at Room Ambient

13,850	21,937,494
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,301 Freq. @ -40°C	21,937,503 Freq. @ 40°C
21,937,353 Freq. @ -30°C	21,937,500 Freq. @ 50°C
21,937,388 Freq. @ -20°C	21,937,485 Freq. @ 60°C
21,937,444 Freq. @ 0°C	21,937,434 Freq. @ 70°C
21,937,494 Freq. @ 20°C	21,937,384 Freq. @ 75°C

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 11

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 11

Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

1,875	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,432 Freq. @ -40°C	21,937,440 Freq. @ 40°C
21,937,529 Freq. @ -30°C	21,937,401 Freq. @ 50°C
21,937,578 Freq. @ -20°C	21,937,357 Freq. @ 60°C
21,937,559 Freq. @ 0°C	21,937,335 Freq. @ 70°C
21,937,499 Freq. @ 20°C	21,937,338 Freq. @ 75°C

TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 8

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 8

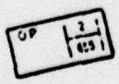
Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

14,420	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,290	21,937,505
Freq. @ -40°C	Freq. @ 40°C
21,937,353	21,937,506
Freq. @ -30°C	Freq. @ 50°C
21,937,395	21,937,507
Freq. @ -20°C	Freq. @ 60°C
21,937,468	21,937,476
Freq. @ 0°C	Freq. @ 70°C
21,937,499	21,937,430
Freq. @ 20°C	Freq. @ 75°C



TEMPERATURE CONTROLLER
P/N 34030415-001
S/N 7

CRYSTAL OSCILLATOR
P/N 34030418-001
S/N 7

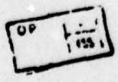
Date of Test 5-11-78

1. Center Frequency Adjust at Room Ambient

13,960	21,937,499
Resistance Value (ohms)	Frequency (Hz)

2. Frequency/Temperature Stability

21,937,234	21,937,509
Freq. @ -40°C	Freq. @ 40°C
21,937,320	21,937,521
Freq. @ -30°C	Freq. @ 50°C
21,937,371	21,937,520
Freq. @ -20°C	Freq. @ 60°C
21,937,444	21,937,473
Freq. @ 0°C	Freq. @ 70°C
21,937,499	21,937,426
Freq. @ 20°C	Freq. @ 75°C



TEMPERATURE CONTROLLER NETWORK ADJUSTMENT AND TRIM PROCEDURE

1. 9V Regulator

Object: Adjust regulator output to 9.000V ± 0.002V

Conditions: a) 12V power supply across 12V (Pin 13) interconnect and ground.
b) DVM across 9V (Pin 8) interconnect and ground.

Trim Procedure:

1.1 Connect 12.000 ± 0.010Vdc Power Supply to the 12V and GND jacks on the trim test box.

1.2 Connect DVM to the DVM HI/LO jacks on the trim test box.

1.3 Set ISO GND switch on the trim test box to the OFF position.

1.4 Set TEST SELECT switch on the trim test box to position 4.

1.5 Trim R21 or R22 as follows:

If DVM < 8.998V, trim R22
If DVM > 9.002V, trim R21

2. Thermometer Gain

Object: Adjust R2 or R1 summing resistors such that the gain for the voltage across CR1 equals 10 ± 5%.

Conditions: a) 12V power supply across 12V (pin 13) interconnect and ground.
b) DVM (ac) at E_1 (term 6, U1) and across CR1.
c) Audio signal generator in series with 5K ohm resistor across CR1.

Trim Procedure

2.1 Connect Signal Generator to the DVM HI and GND jacks on the trim test box.

2.2 Set TEST SELECT switch on the trim test box to position 1.

2.3 Set level of 1 KHz signal to 0.490 ± 0.015 Vdc offset and 60 ± 10 mVac at junction CR1/R2.

2.4 Trim R1 or R2 for a gain of 10 as follows:

If gain > 10 trim R2
If gain < 10 trim R1

3. Thermometer Reference

Object: Adjust R4 or R5 divider resistors such that E1 (term 6, U1) equals 4.355 V ± 0.005 V d.c. at 26.2°C. To correct for temperature difference between actual microcircuit temperature and 26°C use the formula E_1 corrected = 4.355V + 0.021 (TA-26.2°C) where TA is measured temperature of the microcircuit and 0.021 is the thermometer sensitivity in V/°C.

Conditions: a) 12V power supply across 12V (Pin 13) interconnect and ground.

b) DVM (dc) at E_1 (term 6, U1)

Trim Procedure:

3.1 Disconnect the Signal Generator from the 1 KHz HI/LO jacks on the trim test box.

3.2 Measure substrate temperature.

3.3 Trim R4 or R5 as follows:

If DVM > (E_1 corrected +0.005V), trim R4
If DVM < (E_1 corrected -0.005V), trim R5

4. Compensation DFG Curve Rotation

Object: Adjust R15, R16 divider resistors to set voltage across R16 equal to 4.355V such that the standard (design center) correction curve may be linearly rotated at the 26°C reference temperature.

Conditions: a) 12V power supply across 12V (Pin 13) interconnect and ground.

b) Branches containing R13 and R14 are open.

c) DVM across R16.

Trim Procedure:

4.1 Set TEST SELECT switch on the trim test box to position 3.

4.2 Trim R15 or R16 as follows:

If DVM > 4.357V, trim R15
If DVM < 4.353V, trim R16

5. Compensating Curve Selection

Object: Select a compensating curve (described by a set of R13 and R14 values) from a family of rotated curves, by matching the frequency difference between upper and lower turning points (UTP-LTP) obtained from a corrected F/T curve of the assigned crystal unit.

Condition: a) F/T curve for crystal unit obtained in test set with crystal load capacitance at 20pF.

b) Available family of F/T curves previously generated by rotation of the standard curve (R13 = R14 = 10K) using various combinations of R13 and R14 with crystal oscillator maintained at constant room temperature.

Trim Procedure:

Correct for circuit F/T contribution by multiplying the crystal F/T curve (UTP-LTP) difference with Fs/Fx, where Fx is the nominal frequency of the assigned crystal and Fs is the nominal frequency of the crystal from which the standard cubic correction function was derived (Fs = 19.88 MHz). (A near linear repeatable clockwise rotation of the crystal F/T characteristic is produced by the positive TC of the crystal load capacitance).

Select a curve (set of R13 and R14 values) which will provide a frequency change equal to the corrected crystal F/T curve (UTP-LTP) difference from Table I.

TABLE I

Hz	R13	R14
141	10K	40K
153	10K	35K
167	10K	30K
189	10K	25K
214	10K	20K
246	10K	15K
293	10K	10K
342	15K	10K
377	20K	10K
408	25K	10K
432	30K	10K
452	35K	10K
469	40K	10K

6. Compensating Curve Adjustment

Object: Adjust R13 or R14 such as to provide the required rotated compensating F/T curve.

Conditions: a) DVM (ohms) or resistance bridge across R13 or R14.
b) Branches containing R13 and R14 are open.

Trim Procedure:

6.1 Disconnect Power Supply from the 12V and GND jacks on the trim test box.

6.2 Connect DVM LO lead to the ISO GND jack on the trim test box.

6.3 Set the ISO GND switch on the trim test box to the ON position.

6.4 Set TEST SELECT switch on the trim test box to position 5 and trim R13 to the value selected in paragraph 5 (±5 percent).

6.5 Set TEST SELECT switch on the trim test box to position 6 and trim R14 to the value selected in paragraph 5 (±5 percent).

6.6 Return to production to close branches containing R13 and R14.

TABLE I - FUNCTIONAL TRIM RESULTS

S/N	9V REG 9.000±0.001Vdc	Ther. Gain 10±5%		Ther. Ref. E_1 corrected ±0.005 Vdc	DFG Rotation 4.355±0.002Vdc	Comp Curve Adjustment	
		Input Vac	Output Vac			R13 KΩ	R14 KΩ
7	8.999	0.06135	0.6132	4.313@24°C	4.355	10	15.3
8	9.000	0.06074	0.6077	4.308@23.9°C	4.356	10	19.5
11	8.999	0.06268	0.6269	4.314@24.2°C	4.356	10	17.1
14	9.000	0.06033	0.6034	4.307@23.9°C	4.357	10	20.8
15	9.001	0.06114	0.6118	4.306@23.8°C	4.356	10	23.7

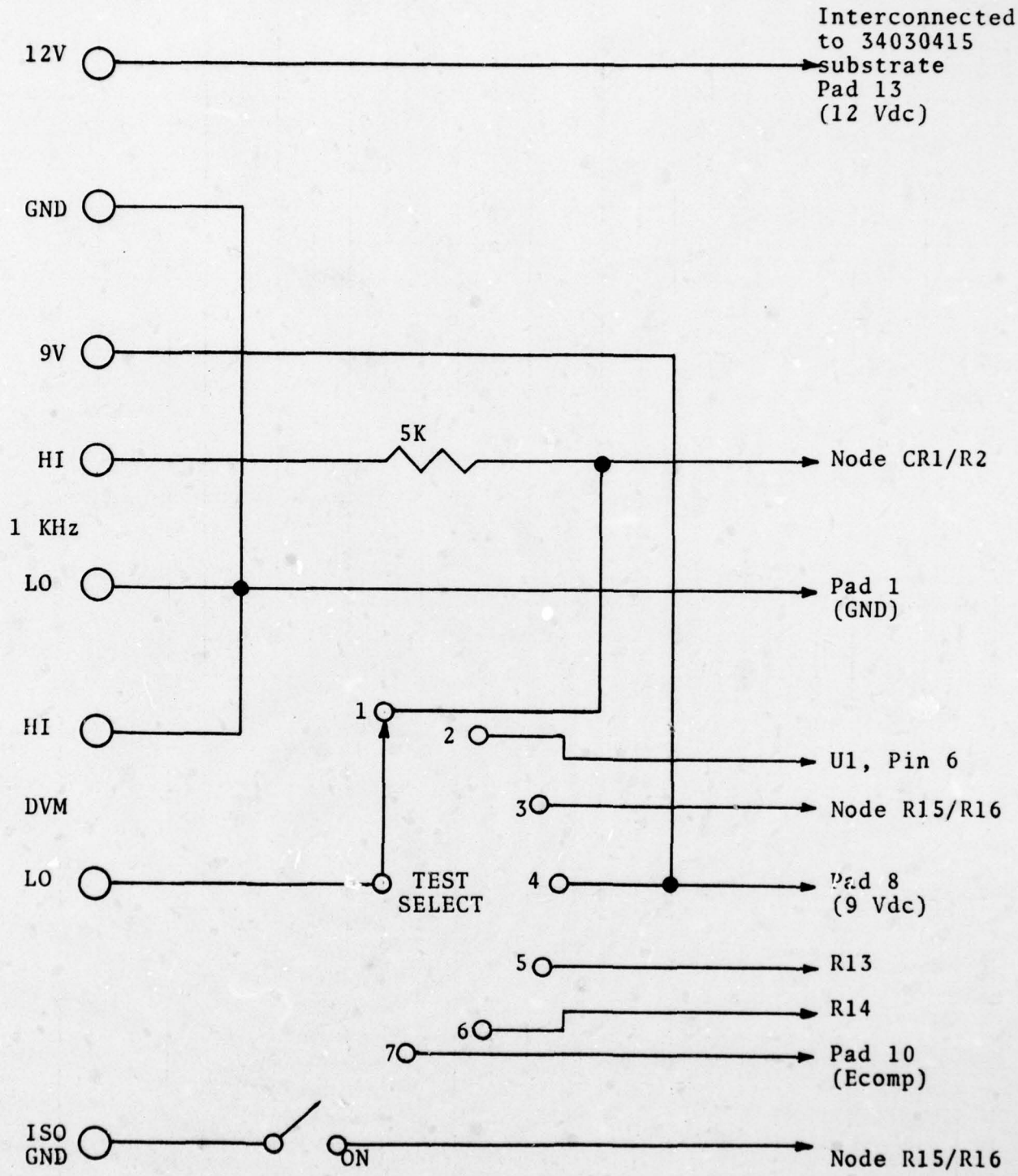


FIGURE 1. - TRIM TEST BOX SCHEMATIC

Appendix III

Universal
Report No. _____

Originator's
Report No. Discriminator -002

Revision _____

REPORT OF TEST ON SINCGARS Discriminator - Second Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal
Report No. _____

Originator's
Report No. Discriminator -002

Revision _____

REPORT OF TEST ON SINCGARS Discriminator - Second Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

	Date	Signature	
Test Initiated	6/30/78		
Test Completed	7/3/78		
Report Written By	7/3/78	S. Jones S Jones/ahn	
Technician			
Test Engineer			
Supervisor	7/3/78	W. Miranda	
Supervisor			
Government Repr. (if applicable)			
Final Release	7/3/78		

1.1 Reason for Test

Acceptance tests were performed on the second lot of engineering samples to be delivered to ERADCOM under Contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the specifications listed in paragraphs 1.3.2.1 through 1.3.2.6.

1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3. The Discriminator Manual Test Fixture is a special piece of test equipment built by Honeywell. This test fixture contains the switch and circuitry required to perform the tests specified in paragraph 1.3.2. Figure 1 shows the schematic of this fixture.

Equipment Used	Model #	HI ID #	Last Calibrated	Due for Calibration
Hewlett Packard Synthesized Signal Generator	8660B	30496	11/16/77	9/16/78
Hewlett Packard Modulation Section	86632A	30497	11/16/77	9/16/78
Hewlett Packard IF Section	86601A	30498	11/16/77	9/16/78
Tektronix Oscilloscope	475	CG12001	6/27/78	1/27/79
Fluke Digital Multimeter	8600A	CG13567	12/6/77	7/6/78
Ambitrol Twin Power Supply	TW5005	CG1804-37	11/4/77	11/4/78
Hewlett Packard Distortion Analyzer	334A	30727	9/28/77	1/28/79
Exact Signal Generator	124	CG12042	1/9/78	1/9/79
Discriminator Test Fixture	N/A	N/A	N/A	N/A

NOTE: The power supply output level was set with the aid of the Fluke Digital Multimeter.

1.3 Test Procedure

1.3.1 Test Circuit

The test configuration for conducting the tests specified in paragraph 1.3.2 is illustrated in Figure 1.

1.3.2 Electrical Requirements

1.3.2.1 Audio Output Voltage

With the HP 8660 and associated equipment set up for 1KHz modulation, 300 uV IF output and a deviation of 5 KHz, the audio output at pins 1 to 2/3 shall be greater than 40 mV.

1.3.2.2 Total Harmonic Distortion

With the HP 8660 and associated equipment set up for 1 KHz modulation, 300 uV IF output and a deviation of 8 KHz, the total harmonic distortion of the audio output at pins 1 to 2/3 shall be less than 5 percent.

1.3.2.3 Audio Output Due to Decrease of IF Input

With the same input conditions as specified in paragraph 1.3.2.2, decrease the IF input until the amplitude of the audio output (pins 1 to 2/3) decreases by 3 dB. The IF input shall be less than 200 uV as read on the meter located on the RF Section of the HP 8660.

1.3.2.4 Audio Output Due to Decreasing AGC

With the HP 8660 and associated equipment set up for 1 KHz modulation, 32 mV IF output and a deviation of 8 KHz, adjust the AGC control on the Discriminator test fixture (see Figure 1) counterclockwise until the amplitude of the audio output decreases by 3 dB. The voltage at pin 7 shall be greater than 2.5 Vdc.

1.3.2.5 Input Current

With the same input conditions as specified in paragraph 1.3.2.2, the current into pins 5 and 6 shall be less than 7.5 mA.

1.3.2.6 Output Filter Bandpass

With the same input conditions as specified in paragraph 1.3.2.2 except that an external oscillator is used for modulation (Exact 124), measure the upper and lower 3dB frequency limits of the Discriminator output. The lower limit shall be less than 5 Hz and the upper limit shall be greater than 25kHz. The Discriminator output at 100KHz modulation shall not be more than -24dB down from the output with 1KHz modulation.

1.4 Test Data

The five engineering samples being delivered passed all functional tests. Test data sheets which contain the test results for Serial Numbers 101, 103, 105, 109 and 110.

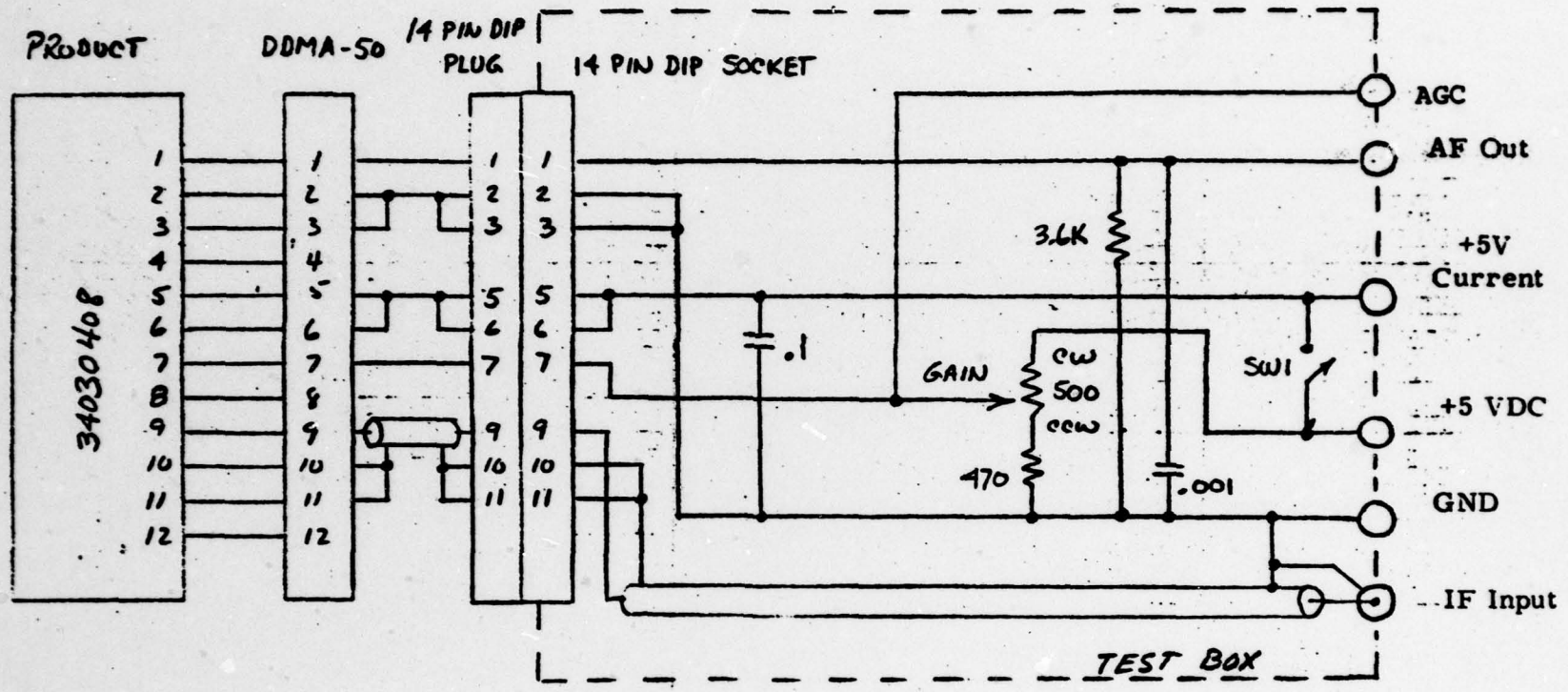


FIGURE 1 - DISCRIMINATOR TEST FIXTURE

DISCRIMINATOR
P/N 34030408-001

S/N 101
Date 7-2-78 after coating

1. Audio Output Voltage

54MV
> 40mV

2. Total Harmonic Distortion

0.38%
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

80 μV
IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.428 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

4.005 mA
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

2.8 Hz.
< 5Hz

(b) Upper -3dB Frequency

31 KHz
> 25 kHz

(c) At 100kHz

-21 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 103 after coating
Date 7-2-78

1. Audio Output Voltage

45 mV
> 40mV

2. Total Harmonic Distortion

0.3 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

65 μV
IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.674 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

3.983 mA
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.1 Hz
< 5Hz

(b) Upper -3dB Frequency

29 kHz
> 25 kHz

(c) At 100kHz

-20.6 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 105 after coating
Date 7-2-78

1. Audio Output Voltage

48 mV
> 40mV

2. Total Harmonic Distortion

0.32 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

85 µV
IF Input Voltage < 200µV

4. Audio Output -3dB (due to decreasing AGC control)

3.701 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

3.647 mA.
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

2.8 hz
< 5Hz

(b) Upper -3dB Frequency

29.4 khz
> 25 kHz

(c) At 100kHz

-20 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 109 after coating
Date 6/30/78

1. Audio Output Voltage

61 MV
> 40mV

2. Total Harmonic Distortion

0.36 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

35 µV
IF Input Voltage < 200µV

4. Audio Output -3dB (due to decreasing AGC control)

3.400 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

3.828 ma
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.0 hz
< 5Hz

(b) Upper -3dB Frequency

32.5 khz
> 25 kHz

(c) At 100kHz

-20.1 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 110 after cooling
Date 6/30/78

1. Audio Output Voltage

52 MV
> 40mV

2. Total Harmonic Distortion

0.45 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

75 μV
IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.364 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

4.025 ma
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

2.9 hz
< 5Hz

(b) Upper -3dB Frequency

31.2 Khz
> 25 kHz

(c) At 100kHz

-20.0 dB
-24dB max.

DISTRIBUTION LIST

Office of Defense Research & Engineering
Communications and Electronics
Room 3D1037
Washington, DC 20330 — 1

Director
US Army Production Equipment Agency
ATTN: Mr. C. McBurney
Rock Island Arsenal
Rock Island, IL 61201 — 1

Advisory Group on Electron Devices
201 Varick Street, 9th Floor
New York, NY 10014 — 2

Chief, Research & Development
ATTN: Director of Developments
Department of the Army
Washington, DC 20310 — 1

Commander
US Army Research Office
ATTN: DRXRO-IP
PO Box 12211
Research Triangle Park, NC 27709 — 1

Commander
US Army Missile Command
Redstone Scientific Info Center
ATTN: Chief, Document Section
Redstone Arsenal, AL 35809 — 1

US Army Missile Command
ATTN: DRSMI-RGP (Mr. Victor Ruwe)
Redstone Arsenal, AL 35805 — 1

Commander
Department of the Navy, Elex 05143A
ATTN: A.H. Young
Electronics System Command
Washington, DC 20360 — 1

Chief
Naval Ship Systems Command
Department of the Navy
ATTN: Code 681A2b, Mr. L. Gumina
Room 3329
Washington, DC — 1

Commander
US Naval Air Development Center
ATTN: Library
Johnsville, Warminster, PA 18974 — 2

Commander
Naval Ocean Systems Command
ATTN: Mr. Richard Gamble
San Diego, CA 92152 — 1

Commander
Rome Air Development Center
Griffiss Air Force Base
ATTN: (EMERR) Mr. L. Gubbins
Rome, NY 13440 — 1

Commander
Air Force Materials Laboratory
ATTN: MATE (Ms. E. Torrance)
Electronic Branch
Wright-Patterson Air Force Base
Dayton, Ohio 45433 — 1

AFAL (AVTA)
Electronic Technology Division
ATTN: Mr. Robert D. Larson, Chief
Advanced Electronics Devices Branch
Wright-Patterson Air Force Base
Dayton, Ohio 45433 — 1

NASA Scientific & Tech
Information Facility
PO Box 8757
Baltimore/Washington Int'l Airport
Baltimore, MD 21240 — 2

National Aeronautics & Space Administration
George C. Marshall Space Flight Center
ATTN: R-QUAL-FP (Mr. Leon C. Hamiter)
Huntsville, AL 35812 — 1

NASA Manned Space Craft Center
Reliability and Flight Safety Division
ATTN: Library
Houston, TX 77002 — 1

Alpha Industries, Inc.
20 Sylvan Road
Woburn, MA 08101 — 1

Amelco Semiconductor
PO Box 1030
Mountain View, CA 94042 — 1

Bell Laboratories
Whippany Road
ATTN: Tech Reports Center
WH5E-227
Whippany, NJ 07981 — 1

Philco Ford
ATTN: Mr. D. Heiden
Landsdale, PA — 1

General Instrument Corp
Semiconductor Products Group
600 West John Street
Hicksville, Long Island, NY 11802 — 1

Hughes Aircraft Corporation
ATTN: Mr. D. Hartman
Bldg. 100 MSA788
PO Box 90515
Los Angeles, CA 90009 — 1

Hughes Aircraft Company
Microelectronics Laboratory
500 Superior Avenue
Newport Beach, CA 92663 — 1

Honeywell Inc.
Semiconductor Products
2747 Fourth Avenue
Minneapolis, MN 55408 — 1

Harris Semiconductor
PO Box 883
Melbourne, FL 32901 — 1

IBM
Components Division
ATTN: Mr. Al Kran
East Fishkill, Rt. 52
Hopewell Junction, NY 12533 — 1

KSC Semiconductor Corp
ATTN: Mr. S. Cudletz, President
KSC Way (Katrina Road)
Chelmsford, MA 01824 — 1

Arthur D. Little
Acorn Park
ATTN: Dr. H. Rudenberg 15/206
Cambridge, MA 02140 — 1

Motorola, Inc.
ATTN: Mr. J. LaRue
5005 East McDowell Road
Phoenix, AZ 85008 — 1

Dr. Robert H. Rediker
Massachusetts Institute of Technology
Building 13-3050
Cambridge, MA 02139 — 1

Microwave Associates
ATTN: Dr. F. Brand
Burlington, MA 01803 — 1

Rockwell International
Collins Radio Group
ATTN: Dr. Cheng Wen
MS 406-246
Dallas, TX 75207 — 1

DISTRIBUTION LIST

Defense Documentation Center
ATTN: DDC-TCA
Cameron Station (Bldg 5)
Alexandria, VA 22314
(2)

Defense Communications Agency
Technical Library Center
Code 205 (P.A. Tolovi)
Washington, DC 20305
(1)

Director
National Security Agency
ATTN: TDL
Fort George G. Meade, MD 20755
(1)

Director, Defense Nuclear Agency
ATTN: Technical Library
Washington, DC 20305
(1)

Code 123, Tech Library
DCA Defense Comm Engring Ctr
1860 Wiehle Ave
Reston, VA 22090
(1)

Office of Naval Research
Code 427
Arlington, VA 22217
(1)

Naval Ships Engineering Ctr
Code 6157D
Prince Georges Center
Hyattsville, MD 20782
(1)

GIDEP Engineering & Support Dept.
TE Section
PO Box 398
Norco, CA 91760
(1)

Director
Naval Research Laboratory
ATTN: Code 2627
Washington, DC 20375
(1)

Commander
Naval Electronics Lab Center
ATTN: Library
San Diego, CA 92152
(1)

Cdr, Naval Surface Weapons Ctr
White Oak Laboratory
ATTN: Library Code WX-21
Silver Spring, MD 20910
(1)

Commandant, Marine Corps
HQ. US Marine Corps
ATTN: Code LMC
Washington, DC 20380
(1)

HQ, US Marine Corps
ATTN: Code INTS
Washington, DC 20380
(1)

Command, Control & Comm Div
Development Center
Marine Corps Devel & Educ Cmd
Quantico, VA 22134
(1)

Rome Air Development Center
ATTN: Documents Library (TILD)
Griffiss AFB, NY 13441
(1)

AFGL/SULL
S-29
HAFB, MA 01731

HQ, Air Force Systems Command
ATTN: DLCA
Andrews AFB
Washington, DC 20331
(1)

Deputy for Science & Technology
Ofc, Assist Sec Army (R&D)
Washington, DC 20310
(1)

Distribution List

Northrop Corporation Laboratories
ATTN: Library 320-61
3401 West Broadway
Hawthorne, CA 90250 — 1

Rockwell International
Corporation Science Center
Thousand Oaks, CA — 1

Raytheon Company
Semiconductor Operation
ATTN: Mr. S. Weinsner
350 Ellis Street
Mountain View, CA 94040 — 1

Raytheon Company
ATTN: Dr. S.F. Paik
130 Second Avenue
Waltham, MA 02154 — 1

Sanders Associates, Inc.
ATTN: Microwave Department
95 Canal Street
Nashua, NH 03060 — 1

TRW Semiconductor Inc.
ATTN: Mr. B. Lindgren
14520 Aviation Blvd
Lawndale, CA 90260 — 1

Texas Instruments
ATTN: Technical Reports Service
PO Box 5936, MS 105
Dallas, TX 75222 — 1

Commander
US Army Electronics R&D Command
Fort Monmouth, NJ 07703

DELEW-D	1
DELET-I	3
DELET-IT	9
DELET-P	1
DELSD-L (Tech Library)	1
DELSD-D	1
DELET-D	1
DELSD-L-S-2 cys	2

US Army Materiel Systems
Analysis Acts
ATTN: DRXSY-MP
Aberdeen Proving Ground, MD 21005 — 1


DATE
ILME