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JAN 79 J KULPINSKI, T SIMONSEN, R PASKOWSKY F30602-77-C-0153
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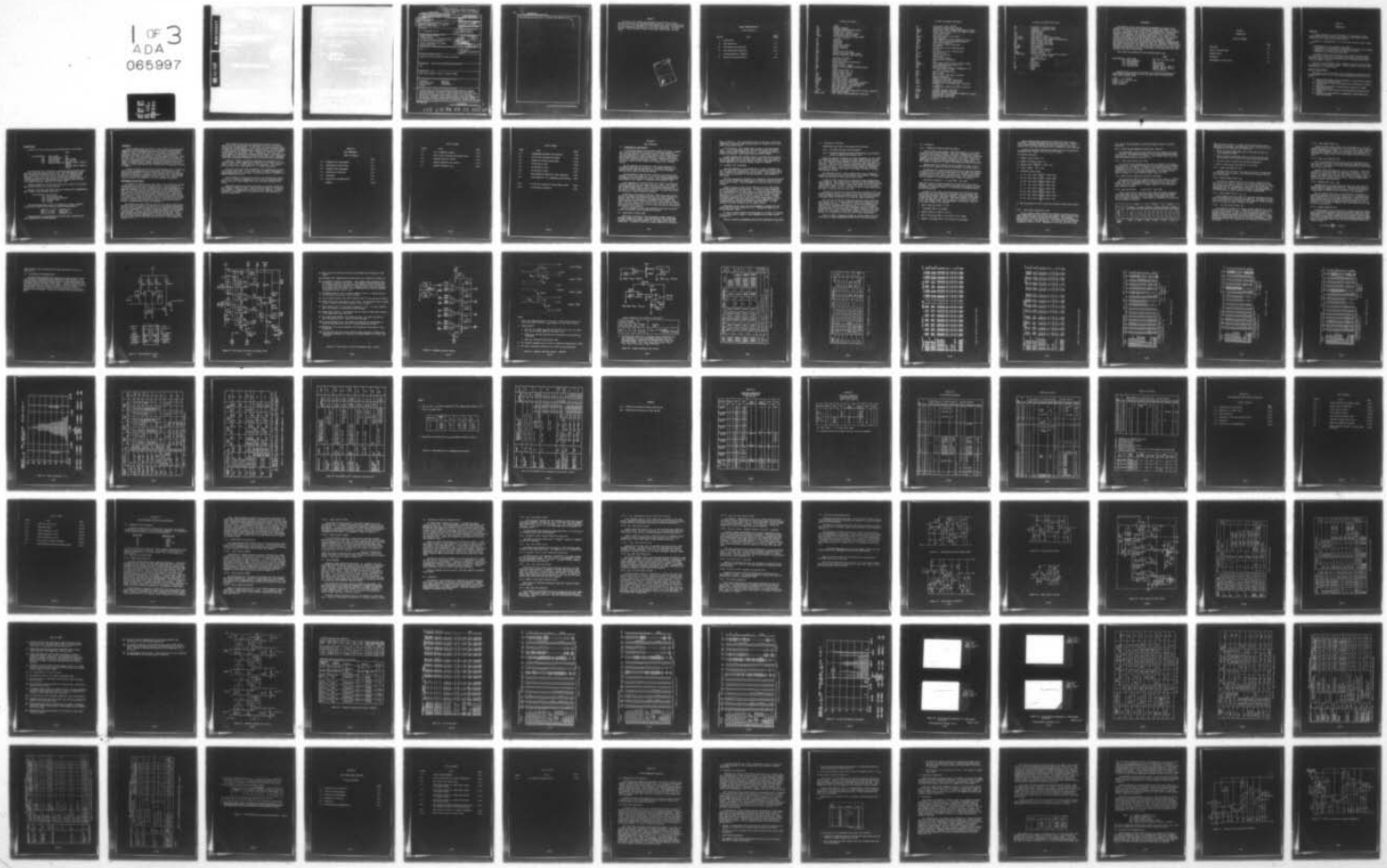

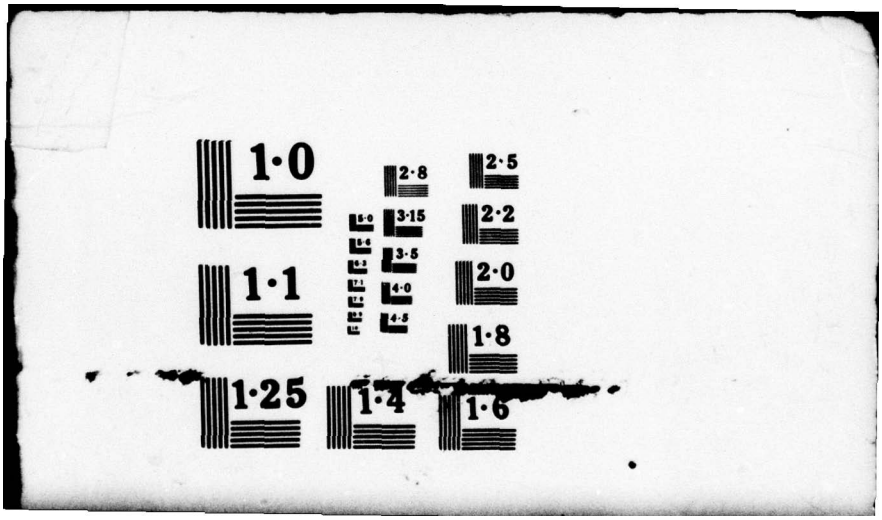
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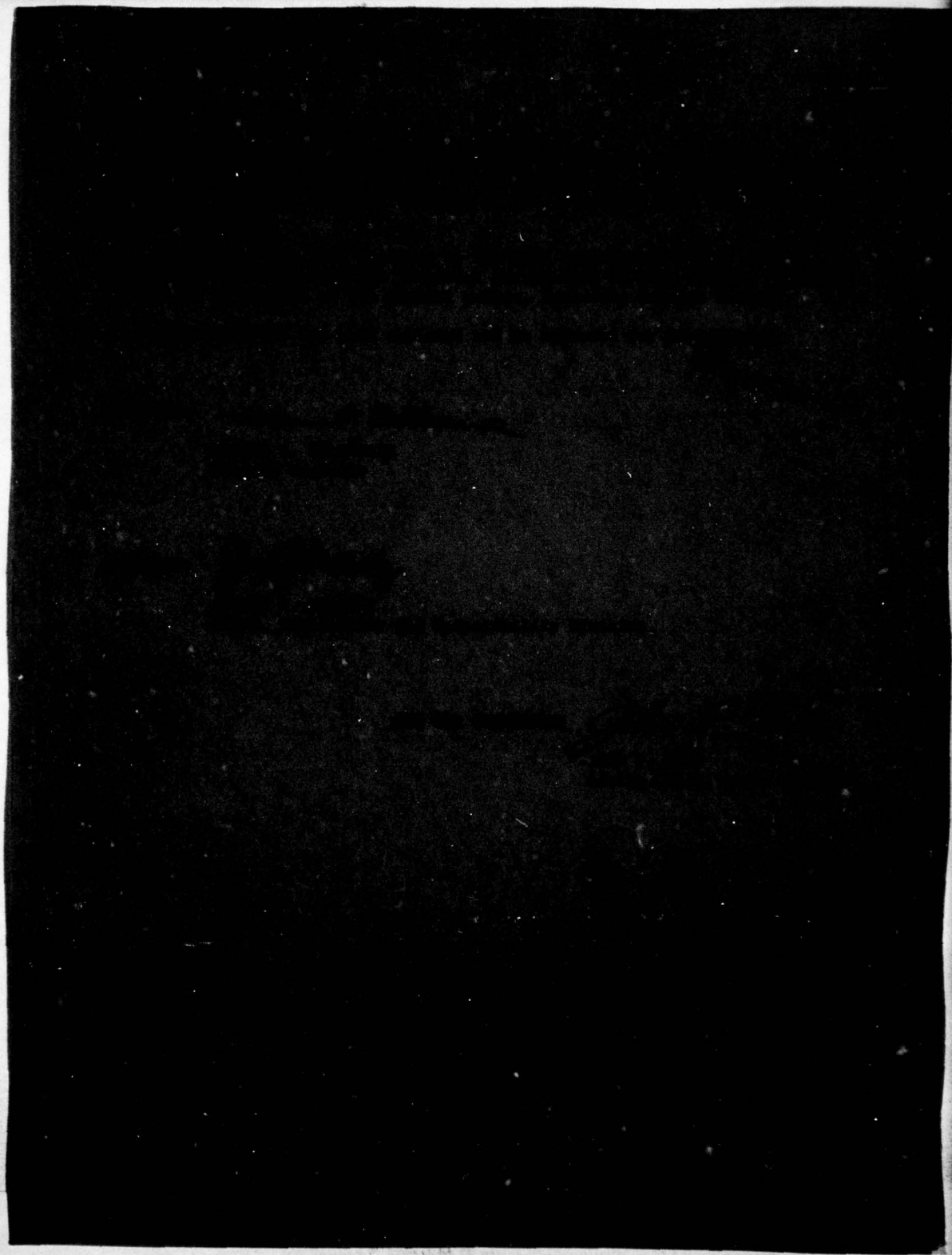

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the work performed by General Electric, Ordnance Systems pertaining to the electrical characterization and specification of linear microcircuits. The period of report is July 1977 to July 1978. Characterization was performed on five generic classes of parts and nineteen device types. The generic classes covered are quad op amps, quad comparators, D/A converters, Bi-FET op amps and negative regulators. Software programs were developed for automatic testing on a Tektronix 3263 automatic test system.

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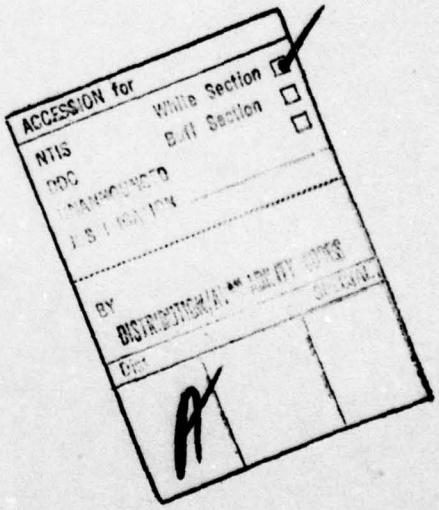
PREFACE

The work on this project was performed by the Electronic Circuits Engineering Operation and Components Engineering Unit. Project responsibility was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals who made significant contributions to this report were Messrs. Theodore Simonsen, Richard Paskowsky, Donald Van Alstyne, Herbert Labb, and Jerry Yaple.



LINEAR CHARACTERIZATION

List of Sections

Acronyms and Symbols

A	Ampere
A/D	Analog to Digital
AIA	Aerospace Industries Association
AMD	Advanced Micro Devices
A_{VC}	Voltage gain, collector output
A_{VE}	Voltage gain, emitter output
$A_{VS}(\pm)$	Open loop voltage gain (single-ended, 0 to +, 0 to 5)
BW	Bandwidth
CM	Common mode
cm	Centimeter
CMR	Common mode rejection
CS	Channel Separation
D/A	Digital to Analog
dB	Decibel
DCR	Direct Current Resistance
DESC	Defense Electronics Supply Center
$\frac{dI}{dt}$	Reference amplifier input slew rate
DOD	Department of Defense
DUT	Device Under Test
EIA	Electronic Industries Association
E_o	Output voltage
GE	General Electric Company
GEOS	General Electric Company, Ordnance Systems
GND	Ground
I^+	Supply current from + V_s
I^-	Supply current from - V_s
$+I_{CC}$	Positive supply current
$-I_{CC}$	Negative supply current
ICs	Integrated Circuits
$I_{FS}(I_o)$	Full scale current, true output
$I_{FS}(\overline{I_o})$	Full scale current, complement
I_{FSR1}	Full scale output current range, condition 1
$+I_{IB}$	Input bias current, non-inverting input
$-I_{IB}$	Input bias current, inverting input
I_{IH}	High level input current
I_{IL}	Low level input current
I_{FSC}	Change in full scale current due to voltage compliance
I_{IO}	Input offset current
$\Delta I_{IO}/\ \Delta T$	Input offset current/temperature coefficient

Acronyms and Symbols (Continued)

I_o	True current output (DAC-08)
$\overline{I}_o$	Complement current output (DAC-08)
$I_{OS(+)}$	Output short circuit current (for positive output)
$I_{OS(-)}$	Output short circuit current (for negative output)
I_{SCD}	Standby current drain
I_L	Load current (/107)
$I_{ZS}(I_o)$	Zero scale current, true output
JAN	Joint Army Navy
JC-41	JEDEC Committee on Linear Integrated Circuits
JEDEC	Joint Electron Devices Engineering Council
LSI	Large Scale Integration
LTPD	Lot Tolerance Percent Defectives
mA	Milliampere
MPCAG	Military Parts Control Advisory Group
mV	Millivolt
NL	Non-linearity (error), positive bits
$N_{i(BB)}$	Broadband noise
N_o	Output noise voltage
$N_{i(PC)}$	Popcorn noise
OS	(GE) Ordnance Systems
P_D	Quiescent power dissipation
pk	peak
+PSRR	Power Supply Rejection Ratio, positive supply
PSSIFS + 1	Power supply sensitivity from + V_s
QPL	Qualified Product List
q/kT	Charge/(Boltzman's constant) (Temperature, °K) q/kT = 25 mV at 25°C
RADC	Rome Air Development Center
S/N	Serial number
SR(+)	Slew rate (max $\Delta V_o/\Delta t$), positive
T_A	Ambient temperature
TC	Temperature coefficient
t_{PHL}	Propagation delay time, high-to-low
t_{PLH}	Propagation delay time, low-to-high
t_{RLHC}	Response time - low-to-high level - collector output
t_{RHLC}	Response time - high-to-low level - collector output
$TR(t_r)$	Transient response, rise time
TR(OS)	Transient response, overshoot
t_s	Settling time of step response to specified accuracy
t_{SLH}	Settling time, low-to-high
t_{SHL}	Settling time, high-to-low
RTN	Return

T^2L	Transistor - transistor logic
T^2L	Transistor - transistor logic
$\overline{V}$	Complement of V
V_{cc}	Supply voltage
V_{IN}	Input voltage
V_{IO}	Input offset voltage
V_{IO} ADJ(+)	Adjustment for input offset voltage
$\Delta V_{IO}/\Delta T$	Input offset voltage temperature coefficient
V_{OL}	Output Voltage, Low Level
V_{OH}	Output Voltage, High Level
V_{OP}	Output voltage swing (peak)
$V_{R\ LINE}$	Line regulation
$V_{R\ LOAD}$	Load regulation
V_{RTH}	Thermal voltage regulation
$+V_S$	Positive supply voltage
V_{START}	Voltage start-up
$\Delta V_{TH}/\Delta V_{CL}$	Change in threshold voltage due to change in control voltage (timer).
$\overline{X}$	Data mean of X
°C	Degrees centigrade
u	Micro
uF	Microfarad
uV	Microvolt
us	Microsecond
Δ	Delta
σ	Sigma

EVALUATION

The objective of this work effort was to characterize selected linear integrated circuit devices and to generate MIL-M-38510 slash sheets for the devices. The characterization effort includes determination of test parameters and limits, assessment of device anomalies, development of test procedures compatible with automatic test systems, generation of burn-in and life test circuits, and preparation of rough draft slash sheets. As a result of earlier studies, specification and test philosophies were fairly well established, and working relationships with the IC industry were developed. Device selection for new slash sheets was based upon various committee recommendations. Test parameters and limits were based upon JEDEC JC41 committee recommendations, data from a representative test sample, and laboratory evaluation. Test circuits developed were evaluated in the laboratory and on a Tektronix S-3260 Test System. The entire characterization process is negotiated at the committee level, from proposed slash sheet to dated issue.

Slash sheets were generated for the following device types:

		TYPES
MIL-M-38510/110	Quad Op Amps	124, 148, 149, 4136 & 4156
/112	Quad Comparators	139
/113	D/A Converters	DAC08 & DOC08A
/114	BiFET Op Amps	155, 156 & 157
/115	Neg Regulators	120H-05, 120H-12, 120H-15, 120H-24, 120K-05, 120K-12, 120K-15, 120K-24

General Electric has done an excellent job in resolving differences of opinion between manufacturers and users and expeditiously preparing draft slash sheets for RADC review.

Thomas L. Dellecave

THOMAS L. DELLECAVE
Project Engineer

SECTION I

INTRODUCTION

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SECTION I

INTRODUCTION

Objectives

The major objective of this work effort is to characterize certain linear integrated circuit devices for inclusion in MIL-M-38510 ("General Specification for Microcircuits") slash sheets.

Generally, "characterization" of a device type includes several related tasks:

* determination of test parameters and limits
* development of test procedures, compatible with automatic test systems
* generation of detailed burn-in and life test circuits
* preparation of a rough draft slash sheet

A secondary objective of this effort is to provide follow-up support for maintaining existing linear MIL-M-38510 slash sheets to current status, including support to Rome Air Development Center for manufacturer qualification and related activities.

All of the characterization effort performed is guided by the fundamental objectives of the JAN 38510 program - namely quality, reliability, interchangeability, and standardization.

Scope of Applied Effort

The specific tasks were planned for this program in a meeting with Rome Air Development Center in July, 1977, when the following efforts were identified:

(1) Develop slash sheets for Quad Comparators, D/A Converters, Negative Regulators and BiFET Op Amps.
(2) Provide support to RADC on development of a slash sheet for Analog Switches.
(3) Assess pending changes to existing slash sheets and recommend appropriate action.
(4) Support RADC in the evaluation of manufacturer qualification submittals.
(5) Interface with manufacturers as appropriate; attend JEDEC JC-41 committee meetings.

Program Status

A total of 15 device types have been characterized in this effort:

		TYPE
MIL-M-38510/110	Quad Op Amps	124
/112	Quad Comparators	139
/113	D/A Converters	DAC08, DAC08A
/114	BiFET Op Amps	155, 156, 157
/115	Negative Regulators	120H-05, 120H-12, 120H-15, 120H-24
		120K-05, 120K-12, 120K-15, 120K-24

The /110 effort was a follow-on to a previous characterization effort; this slash sheet was issued on May 28, 1978. The Quad Comparator slash sheet is complete and ready for issue in mid-1978. The remaining three slash sheets (/113, /114, /115) are not yet finalized, awaiting JC-41 response to unresolved problems with the devices and/or specifications. It is anticipated that all of the problems will be resolved before the next JC-41 committee meeting, scheduled for October, 1978.

Ordnance Systems has also provided consultation to RADC on the development of MIL-M-38510/111 for Analog Switches.

Changes to existing slash sheets have been assessed and recommendations made to RADC on the following slash sheets:

MIL-M-38510/110	Quad Op Amps
/107	Positive Regulators
/104	Line Drivers and Receivers
/109	Precision Timers
/101	Op Amps

The following meetings of the JC-41 Committee on Linear Integrated Circuits were attended by the Ordnance Systems Program Manager:

August 23, 24, 1977	Sunnyvale, Cal.
March 7, 8, 1978	Dallas, Tex.
June 21, 22, 1978	Washington, D.C.

Characterization and specification activities were coordinated with device manufacturers at these meetings.

Background

Ordnance Systems began this effort in July of 1977, having previously completed a related characterization program in 38510 linears (Contract F30602-76-C-0345, Report RADC-TR-78-22). Philosophies for establishing parameters, limits, and test circuits were fairly well established in meetings of the JEDEC JC-41 Committee on Linear Integrated Circuits. These meetings, held at four month intervals (approximately), were attended by all of the major manufacturers of integrated circuits with one or two exceptions. Representatives from RADC, the Defense Electronics Supply Center (DESC), and General Electric Ordnance Systems were present at all of the meetings. Working relationships were developed with key personnel from each IC company.

In order to improve the efficiency of the meetings, and to increase the rate at which new specifications are developed, sub-committees or task groups were established for several generic families, such as op amps/comparators, D/A converters, regulators, and analog switches. These meetings were held to determine recommended parameters, limits, test circuits, and burn-in circuits to be presented to the full committee for approval.

Development of Slash Sheets

A procedure for developing new slash sheets to MIL-M-38510 has evolved through negotiations among all concerned parties. Device selection is influenced by user need, which is determined both by the marketplace and by organized committess, such as the Military Parts Control Group (MPCAG) at DESC, the G12 Solid State EIA Device Committee, and the Microelectronics Projects Group of the Electronics Systems Committee of AIA. These recommendations are balanced with manufacturer recommendations obtained via the JC-41 committee. Devices having high useage, multiple application potential in military systems, proven performance, and two or more sources are given priority. Single-source devices are acceptable, especially for hybrid devices, although multiple sources are preferred.

The industry data sheet forms the basis for the military specification. Typically, such data sheets do not specify all of the necessary parameters over the military temperature range and over the common-mode voltage range. The JC-41 subcommittee, or the device originating company, usually prepares a proposed spec. Ideally, the device manufacturers would like to have these proposed specs incorporated without further consideration. However, RADC and General Electric experiences in this current program have shown that all of the proposed specs have been deficient, and are unsuitable for issuance "as is".

Data provides another base for determining parameters and limits. Devices for test are purchased from distributors, are also obtained from manufacturers via RADC request. In some cases, the industry-donated sample is tested by a single manufacturer on a volunteer basis. The entire sample is tested further on a Tektronix S3263 Automatic Test System at GE Ordnance Systems Electronic Test Center. Data obtained at -55°C, +25°C, and +125°C ambient is statistically analyzed and reproduced in histogram format. Recommended limits are compared to the statistical sample data. Parameter limits which are grossly inconsistent with the data are readily identified.

Additions, changes, and alternate approaches are discussed at the committee level. Device anomalies are identified in lab bench tests, often using a curve tracer. Failure modes are also identified. User caution notes are added to the specification if it is deemed appropriate.

Burn-in circuits are usually recommended by the manufacturer and evaluated by RADC and/or GEOS. At this time, there is apparent disagreement among manufacturers as to the merits of reverse-bias burn-in vs. dynamic and maximum dissipation burn-in.

Device schematics are presently included in MIL-M-38510 slash sheets. A recent JC-41 committee recommendation is to delete the schematics and to replace them with a block diagram which shows the basic elements of the device.

Rough-draft copies of the final slash sheet are prepared at GEOS and are forwarded to RADC for review. DESC distributes copies of this spec for final comments, to manufacturers and users for final comments. Following assessment of the comments by all concerned parties, DESC prepares and issues the slash sheet.

SECTION II

QUAD COMPARATOR

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SECTION II

QUAD COMPARATOR

2.1 Background and Introduction

In interfacing between low level analog signals and digital systems there are many applications which make use of voltage comparators. Zero crossing detectors, level/window detectors, pulse height detectors and pulse generators are popular application circuits of comparators. Quad voltage comparators have some additional advantage where circuit density and low power dissipation is required. Because of pin-out restrictions, offset voltage trimming and strobing are not available options.

The 139 comparator was chosen for linear characterization and MIL-M-38510 slash sheet action because it is popular among users, is multiple sourced from many manufacturers and has good performance characteristics useful for many applications.

The MIL-M-38510/112 specification originated from National Semiconductor's LM139 data sheets and a JC-41 joint industry recommendation of parameters, test conditions and limits. These recommendations were then modified by the results of characterization studies at GEOS.

A new ingredient for characterization was tried out by having all interested manufacturers ship typical devices to RADC. RADC unbranded and serialized these devices. This mixed industry sample was then sent to AMD (Advanced Micro Devices) a supplier who volunteered to test the devices to their standard factory test tape. The data and devices were then sent to GEOS via RADC for analysis.

In addition to reviewing the AMD data, GEOS built a test fixture and wrote a program for testing the device on its S-3260 automatic test system. While the S-3260 adapter and program were being developed, several devices were analyzed on a Tektronix 577 curve tracer. The curve tracer was useful in observing how each of the standard parameters (V_{IO}, $\pm$ I_{IB} etc.) changed over a range of test condition voltage. Device trends and anomalies found with the curve tracer are useful in developing the automatic test procedures.

The test program and slash sheet generation were done in parallel so that any problems could be exposed and resolved.

2.2 Description of Device Type

Device type 01 consists of four independent voltage comparators sharing a common power source. Low power operation over a wide range of supply voltage is possible because of the current source biasing scheme used. A schematic circuit of a single comparator in the quad is

shown in Figure 2-1. PNP transistors are used in the input so that each comparator's common mode range includes ground for single as well as dual supply voltage applications.

The differential input voltage range is equal to the power supply range. In low voltage applications, the input can exceed the positive supply voltage without damaging the device. If large negative input excursions are possible, diode clamp protection should be added.

An open collector NPN transistor output is provided with the device. This permits compatibility with many logic systems. Also the outputs of several comparators can be tied together for output OR'ing applications. In most applications an external pull-up resistor is required.

2.3 Automatic Test Development

From past experience it was decided that, in order to maximize the data base from which characteristic limits and conditions could be specified, automatic test procedures would be developed. A test program and an adapter card were developed for the GEOS Tektronix S-3260 Automatic IC Test System.

Since the standard test parameters for comparators have been previously defined in MIL-M-38510/103 minimum effort was required to define the necessary types of tests. Limits recommended by JC-41 were used for initial testing.

Figure 2-2 shows the test circuit schematic for the S-3260 adapter and the MIL-M-38510/112 specification. Any one of the four comparators can be programmed into the test circuit. A forcing voltage V_A applied to the inverting input of the nulling amplifier causes the comparator device under test (D.U.T.) to drive its output to the same voltage. Frequency compensation is provided by the .047 uf capacitor at the D.U.T. output. All standby comparators have a positive 1V bias voltage applied to their inverting inputs. This forces base drive to each comparator's output transistor and thus defines its standby mode output state. For test purposes this tends to maximize the I_{cc} supply current.

Measurement of the static front end parameters is permitted by the 1000:1 gain relationship between the D.U.T. differential input and the nulling amplifier output.

In order to permit response time measurements to be made, the features of the circuit shown in Figure 2-3 were combined with the basic circuit of Figure 2-2.

Table 2-1 shows the programming conditions and equations for the tests.

2.4 Tabulation of Test Data

Measurements were taken on two sample lots as follows:

Lot 1 - 32 LM139's procured from distributors

Lot 2 - 99 LM139's supplied by several manufacturers and initially tested by Advanced Micro Devices, Inc.

Table 2-2 shows the conditions and limits programmed into the S-3260 for testing the devices. A typical data output sheet is shown in Table 2-3. The astericks indicate parameter values that exceed the limits of Table 2-2. Tables 2-4, 2-5 and 2-6 are statistical data summaries of lot 2 for 25°C, -55°C and 125°C, excluding devices supplied by manufacturer "X" (code identifier). Group "X" was excluded because the individual data sheets of these devices showed a much higher incidence of failures than the other devices.

The objective of each of these summaries was to get a comparison between the statistical data and the initial (JC-41) limits. Estimated limits were used when no other specification existed.

A figure of merit calculation was performed on each parameter-data-limit condition. This figure of merit indicates how many standard deviations (Sigma, σ) exists between the data mean $\bar{X}$ and the low and high JC-41 specification limits. Since in a normal distribution 99.7% of the data points will be within $\bar{X} \pm 3\sigma$, the figure of merit is one indication of how tight or loose the initial limits are.

In practice a few "way-out" data points have a big effect on σ and therefore figure of merit. To counteract this effect high and low reject limits (determined by judgement) were included. Any data points beyond the reject limits were not used in the mean and sigma calculations.

The first data reductions yielded many figures of merit which were high (greater than 5). Certain parameter limits were tightened and the data reduction was rerun. Tables 2-4, 2-5 and 2-6 were generated with revised limits; histograms were generated for all of the data groups. Limit bars were drawn on each of the histograms, such as in Figure 2-4. The perspective of a data histogram with limits is superior to any other method. For the purpose of this report, however, the statistical summaries are a condensed way to show the data-to-limit relationships.

Table 2-7 gives a comparison between the catalog limits, the JC-41 limits and the limits recommended by GEOS for the /112 specification.

2.5 Discussion

2.5.1 Comparison of AMD and GEOS Test Results

Since 99 devices were tested at both AMD and GEOS it is of interest to know how well the data compares. There are fundamental differences between the data formats and some of the tests. The AMD data is organized in a matrix of test columns and serial number rows so that variations in parameter values between different devices can be checked. GEOS's data sheet format in Table 2-3 shows all parameters for a single device. Several tables were generated to display data comparisons from both sources.

Appendix Table A2-1 compares the AMD and GEOS data taken on S/N 1. How well the data compares is relative and depends on certain criteria.

At GEOS and other facilities which manufacture or test Navy Standard Electronic Modules, correlation measurements per MIL-M-28787 are required to demonstrate that data taken on one tester are traceable to the specification and the data of other correlated testers. MIL-M-28787 requires that for parameter tolerances greater than or equal to 3 percent:

Correlation tolerance = ± .11 (max limit - min limit)

Using this criteria the AMD and GEOS data correlate with only a few exceptions. Table A2-2 shows an overall evaluation of the devices in terms of good/bad or pass/fail criteria. For the front end parameters agreement was fairly good.

Besides the data format differences between the GEOS and AMD test results there are also differences in parameter types, parameter limits and histogram groupings. AMD type parameters, not tested at GEOS, were ± Swing and V_{IO} at zero common mode. GEOS type parameters, not tested at AMD, were V_{IO} drift, I_{IO} drift, ± I_{IB} at 5 V, ± I_{IO} at 5 V, CMR, I_{cc} at 30 V and response times. The AMD parameter limits differ from the JC-41 limits in Table 2-7 as follows:

1. V_{IO} at $-55 \leq T_A \leq 125°C$ = ± 9 mV
2. ± I_{IB} upper limit = 10 nA (max)
3. I_{CEX} at $-55 \leq T_A \leq 125°C$ = 0.5 uA
4. V_{OL} at $-55 \leq T_A \leq 125°C$, 1 KΩ and 5V = 0.5 V (max)
5. I_{SINK} at $-55 \leq T_A \leq 125°C$, 1 KΩ and 5V = 5.7 mA (min)

Both the AMD and GEOS individual data sheets have limit failures identified. Although histograms exist for both data sources. These can not be compared directly because the GEOS data includes all four comparators in a quad, while the AMD data has a histogram for each comparator.

A review of the GEOS individual data sheets gave the following yield information with respect to the initial JC-41 limits.

G.E. Results (per quad)

1. Number of parts tested = 99

2. Number of defective parts = 19

3. Overall yield = $\frac{99 - 19}{99}$ x 100% = 81%

4. % Fail = 100% - 81% = 19%

5. Individual vendor yields

   a) C1 - C10 yield = $\frac{10 - 2}{10}$ x 100% = 80%

   b) P3 - P10 yield = $\frac{8 - 0}{8}$ x 100% = 100%

   c) X2 - X10 yield = $\frac{10 - 8}{10}$ x 100% = 20%

   d) U1 - U11 yield = $\frac{11 - 2}{11}$ x 100% = 82%

   e) J1 - J10 yield = $\frac{10 - 1}{10}$ x 100% = 90%

   f) S1 - S65 yield = $\frac{14 - 3}{14}$ x 100% = 79%

   g) G7 - G24 yield = $\frac{18 - 1}{18}$ x 100% = 94.4%

   h) R1 - R20 yield = $\frac{20 - 3}{20}$ x 100% = 85%

6. With the exception of the X parts most failures involved bias current.

2.5.2 Input Offset Voltage V_{IO} (± CM)

As the parameter symbol suggests this parameter is measured over the input common mode range, which is from the negative supply, usually ground, and to within 2 volts of the positive power supply. The histograms, summaries and data sheets indicate the ± 5 mV limits to be well chosen for the four 25°C tests. The same tests at -55°C and 125°C had initial JC-41 recommended limits of ± 8 mV. Examination of the data shows that limits

of ± 7 mV are very reasonable; 3.69 was the figure of merit of the worst condition.

2.5.3 Offset Voltage Temperature Sensitivity $\Delta V_{IO}/\Delta T$

Most measurements were very much better than the proposed JC-41 limits of ± 30 uV/°C. The theoretical $\Delta V_{IO}/\Delta T$ for a simple differential input stage would be 3.3 uV/°C x 5 = 16.5 uV/°C. With revised units of ±25 uV/°C, the worst observed figure of merit was 5.74.

2.5.4 Input Offset Current I_{IO} (± CM)

For $25 \leq T_A \leq 125$°C applications the JC-41 I_{IO} limits of ± 25 nA are very reasonable. Although the data shows that I_{IO} increases with decreasing temperature the JC-41 limits of ± 100 nA at -55°C are not justified. With a compromise value of ± 75 nA, the yield on this -55°C value is much better than that with ± 25 nA at the higher temperatures. The revised ± 75 nA limits correspond to a worst observed figure of merit of 7.52.

2.5.5 Offset Current Temperature Sensitivity $\Delta I_{IO}/\Delta T$

With cold drift limits of ± 400 pA/°C and hot drift limits of ± 300pA/°C the summarized data minimum figures of merit are 5.96 and 5.30 respectively. The JC-41 recommended limits were ± 600 pA/°C and ± 300 pA/°C for cold and hot drift respectively. A figure of merit of 8.96 would result with ± 600 pA/°C limits.

2.5.6 Input Bias Current $+I_{IB}$ (± CM), $-I_{IB}$ (± CM)

From a yield criteria, the bias current tests are the most difficult. Since these tests over the common mode range, supply voltage and temperature have the most failures, it is of interest to see where they occur and if a pattern is observable. Shown below is a tabulation of I_{IB} failures for the different conditions.

$+V_{cc}$	CM	25°C				-55°C				125°C			
		$+I_{IB}$		$-I_{IB}$		$+I_{IB}$		$-I_{IB}$		$+I_{IB}$		$-I_{IB}$	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
30V	+	1	7	1	4	0	6	0	0	0	9	0	10
30V	-	18	0	18	0	0	0	0	0	3	0	5	0
5V	+	0	0	1	1	0	1	0	1	0	0	0	2
5V	-	2	0	4	0	0	1	1	0	0	0	1	0
Limits (nA)		-100	-1	-100	-1	-200	-1	-200	-1	-100	-1	-100	-1

These failures are based on a sample size of 396 (99 quads) and are supported by histograms. Some observations seen from this table, the histograms and the individual data sheets are:

1. The 30 V negative common mode tests at 25°C have the most low limit magnitude failures.

2. The 30 V positive common mode tests at 25°C have the most high limit failures, some of which are wrong polarity bias currents.

3. The bias currents increase with decreasing temperature.

4. Most 5 V bias current failures occur at 30 V also.

2.5.7 Common Mode Rejection CMR

The CMR limits of 76 and 70 dB limit at 30 V and 5 V respectively are reasonable for the device. Most observed CMR failures also had V_{IO} (+ CM) failures.

2.5.8 Output Leakage Current I_{CEX}

The specified leakage current of 0.1 μA max at $-55°C \leq T_A \leq 25°C$ and 1.0 uA at $T_A = 125°C$ is reasonable for the device based on the data. Most devices had a measured I_{CEX} of "-5 nA", which really means that their values were less than the measurement resolution of the test system. Although the user, in general, has little need for this leakage quality, the specification is a good indicator of surface contamination.

2.5.9 Input Leakage Current + I_{IL}, I_{IL}

Input leakage current was added as a specified requirement after the S-3260 characterization testing had been completed. The purpose of this test is to verify that the differential input breakdown voltage is greater than 34 volts when the supply voltage is 36 volts.

2.5.10 Low Level Output Voltage V_{OL}

The saturation voltage of the device's output transistors is an important interface characteristic. S-3260 data was taken at 4 mA and 6 mA of output sink current. In order to have low saturation voltage at a specified level of sink current, the output transistor's require a combination of adequate base drive and low saturation resistance. The tests verified the specification for 4 mA and 6 mA drive requirements. It was subsequently decided that changing the 6 mA condition to 8 mA would be more useful.

2.5.11 Power Supply Current I_{cc}

Having low power supply current over a wide range of V_{cc} is an important characteristic of this device. All of the data is well inside the specified maximum current limits. It was decided that a liberal specification on this parameter is justified because the user's benefit of a milliampere of supply current is not worth taking a possible future yield loss.

2.5.12 Open Loop Voltage Gain AVS

Most of the measured gains were better than the specification by a factor of from two to ten. In all cases where gain magnitude failures were observed, the comparator had other front end failures in some combination of V_{IO}, I_{IO} and I_{IB}.

Negative gains were observed in 10 out of 396 devices. There were asterisk (*) on the data sheets for visability as failures. All of the devices with negative gain also had other front end failures. Consequently, any devices that would have been rejected for negative gain were rejected for other parameter failures first. Transient thermal effects cause the negative gain phenomenon.

2.5.13 Response Time t_{RLH} , t_{RHL}

Response time for the low-to-high and high-to-low transitions are the most important dynamic characteristics. Although these tests are usually done on a sampled bench set up basis, it was felt that getting a large volume of automatic tester data would be very worthwhile.

The test results showed that at five millivolts of overdrive the comparators performed very much better than the JC-41 recommended limit. This is especially true for the t_{RHL} response time. Testing and specifying response time at 50 millivolts of overdrive was done so that the user has more information for applications having greater than 5 mV of overdrive. With the GEOS recommended limits, data figures of merit from 4 to 8.7 were calculated.

2.5.14 Channel Separation (CS)

It was decided not to add provisions for channel separation testing to the S-3260 adapter because it would have resulted in many more relays being added to it. Manual test data was taken on several devices using a Tektronix 577 curve tracer, modified for CS testing as shown in Figure 2-4. The ΔV change in V_{IO} used in calculating channel separation varied between 0 and 0.2 millivolts. With this data the minimum observed calculation results in

$$CS = 20 \log \frac{30000}{0.2} = 103 \text{ dB}$$

This is better than the proposed 80 dB (min) spec limit by 23 dB or a factor of 14.

2.6 Conclusions and Recommendations

The preceeding paragraphs have discussed the characterization effort and properties of the proposed MIL-M-38510/112-01 quad comparator. For obvious economic reasons the complete portfolio of device data sheets and histograms cannot be included in this report. A device specification has been written using the results of this study. A 200 page report on the 139 characterization data was submitted to RADC and the I.C. vendors in February 1978. The report contains 99 device data sheets, 9 statistical sumaries and 90 histograms. Copies may be obtained by contacting GEOS or RADC.

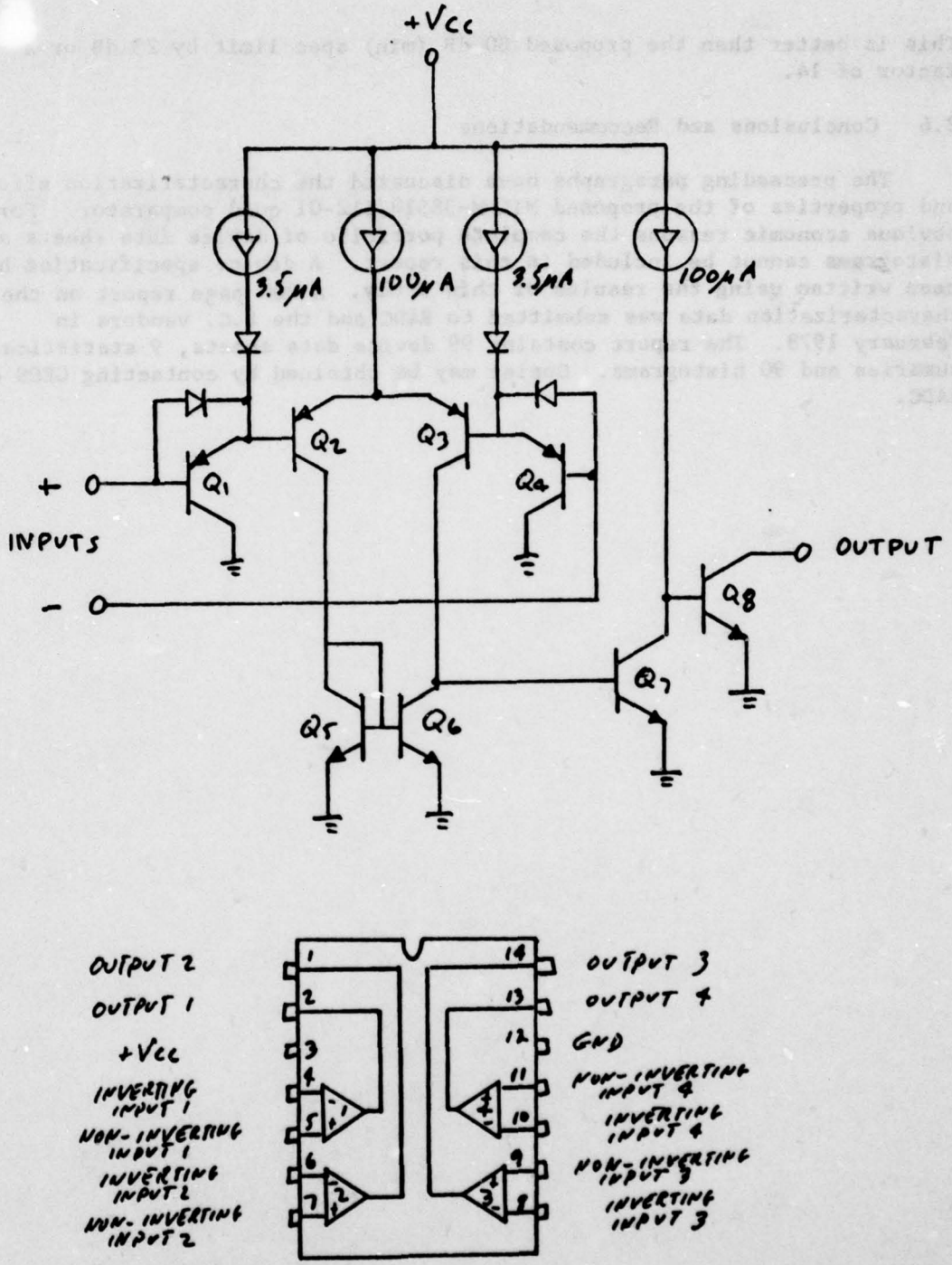


Figure 2-1 LM139 schematic circuit.

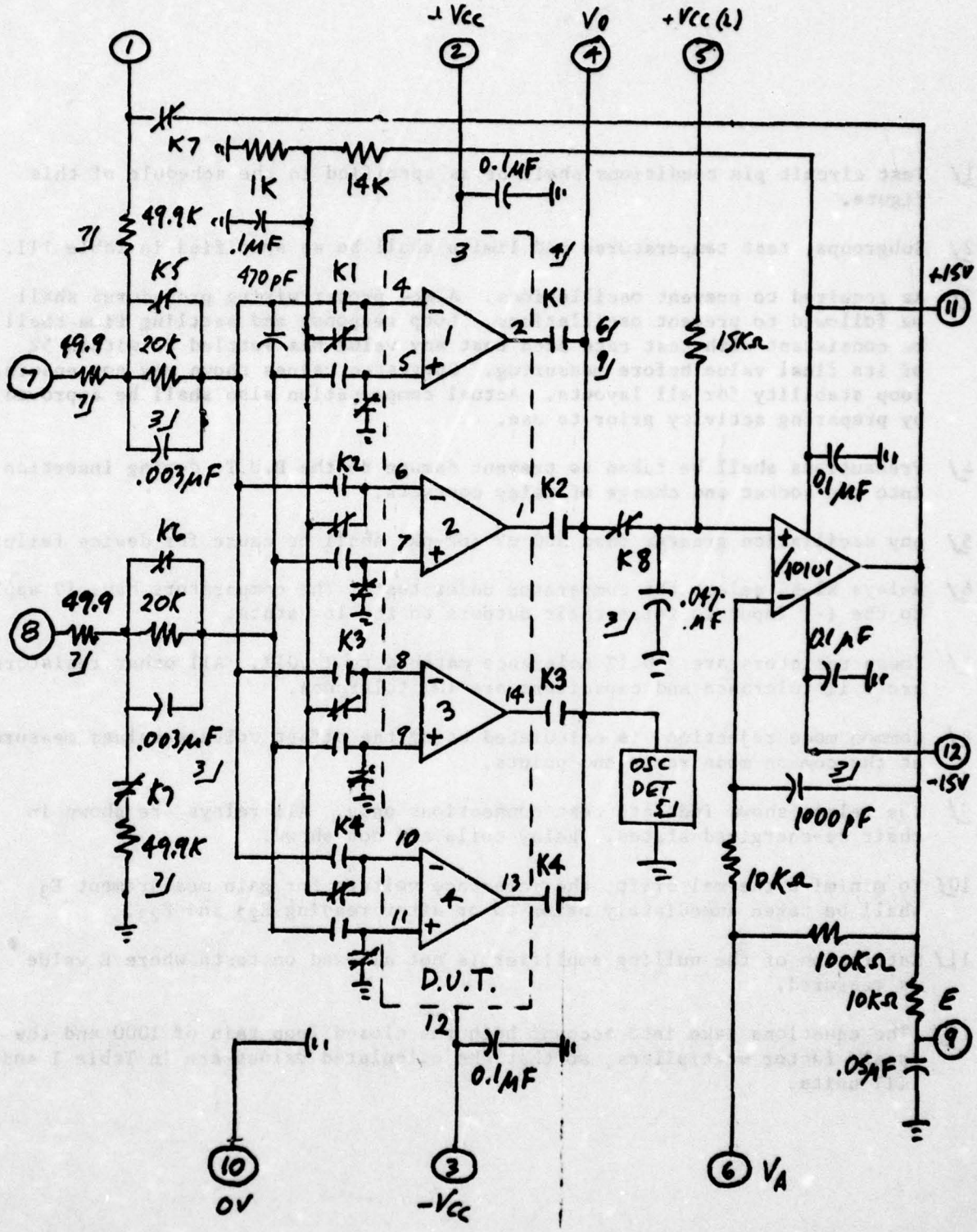


Figure 2-2 Test circuit for static and dynamic tests.

1/ Test circuit pin conditions shall be as specified in the schedule of this figure.

2/ Subgroups, test temperatures and limits shall be as specified in Table III.

3/ As required to prevent oscillations. Also, proper wiring procedures shall be followed to prevent oscillations. Loop response and settling time shall be consistant with test rate such that any value has settled to within 5% of its final value before measuring. Suggested values shown may not ensure loop stability for all layouts. Actual compensation also shall be approved by preparing activity prior to use.

4/ Precautions shall be taken to prevent damage to the D.U.T. during insertion into the socket and change of relay contacts.

5/ Any oscillation greater than 300 mV (pk-pk) shall be cause for device failure.

6/ Relays K1-K4 select the comparator under test. The comparators have 1V applied to the (-) input to force their outputs to the low state.

7/ These resistors are ± 0.1% tolerance matched to ± .01%. All other resistors are ± 1% tolerance and capacitors are 10% tolerance.

8/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

9/ The relays shown indicate test connections only. All relays are shown in their de-energized states. Relay coils are not shown.

10/ To minimize thermal drift, the reference voltage for gain measurement E_3 shall be taken immediately prior to or after reading E_{22} and E_{23}.

11/ Saturation of the nulling amplifier is not allowed on tests where E value is measured.

12/ The equations take into account both the closed loop gain of 1000 and the scale factor multipliers, so that the calculated values are in Table I and III units.

Figure 2-2 Test circuit for static and dynamic tests (cont'd.)

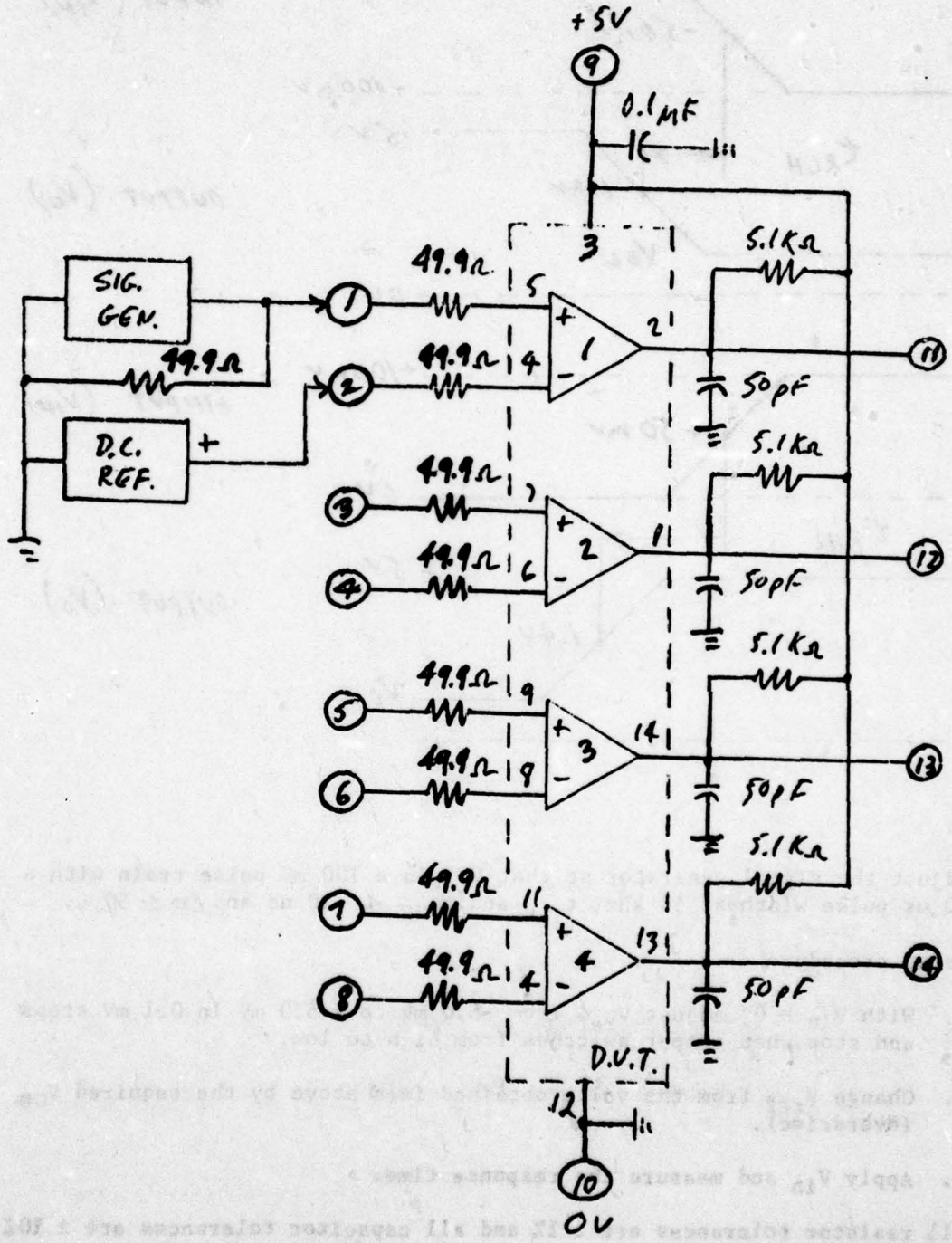
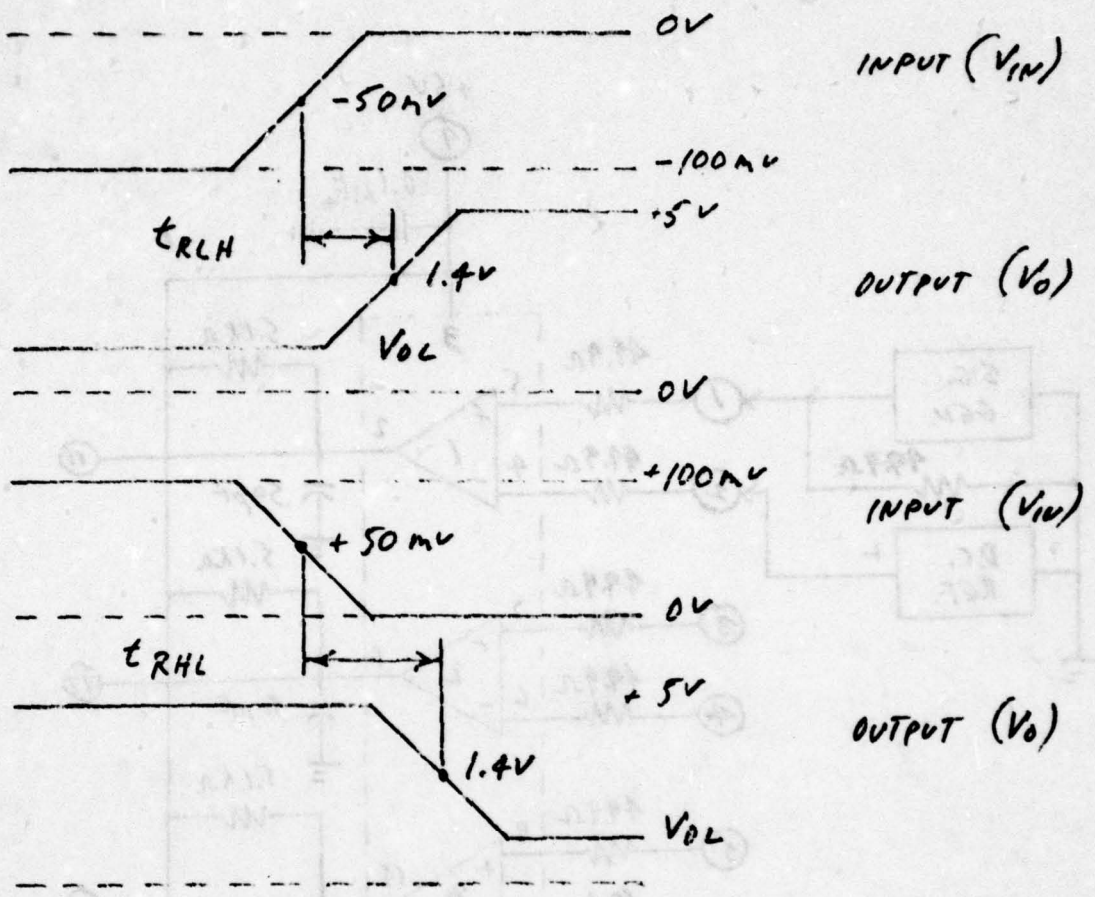


Figure 2-3 Response time test circuit.



NOTES:

1. Adjust the signal generator so that V_{in} is a 100 mV pulse train with a 10 μs pulse width at 50 kHz, t_{TLH} and $t_{THL} \leq$ 10 ns and $Z_O \approx 50\Omega$.

2. Setup procedure

   a. With V_{in} = 0, adjust V_{ref} from -5.0 mV to + 5.0 mV in 0.1 mV steps and stop when output switches from high to low.

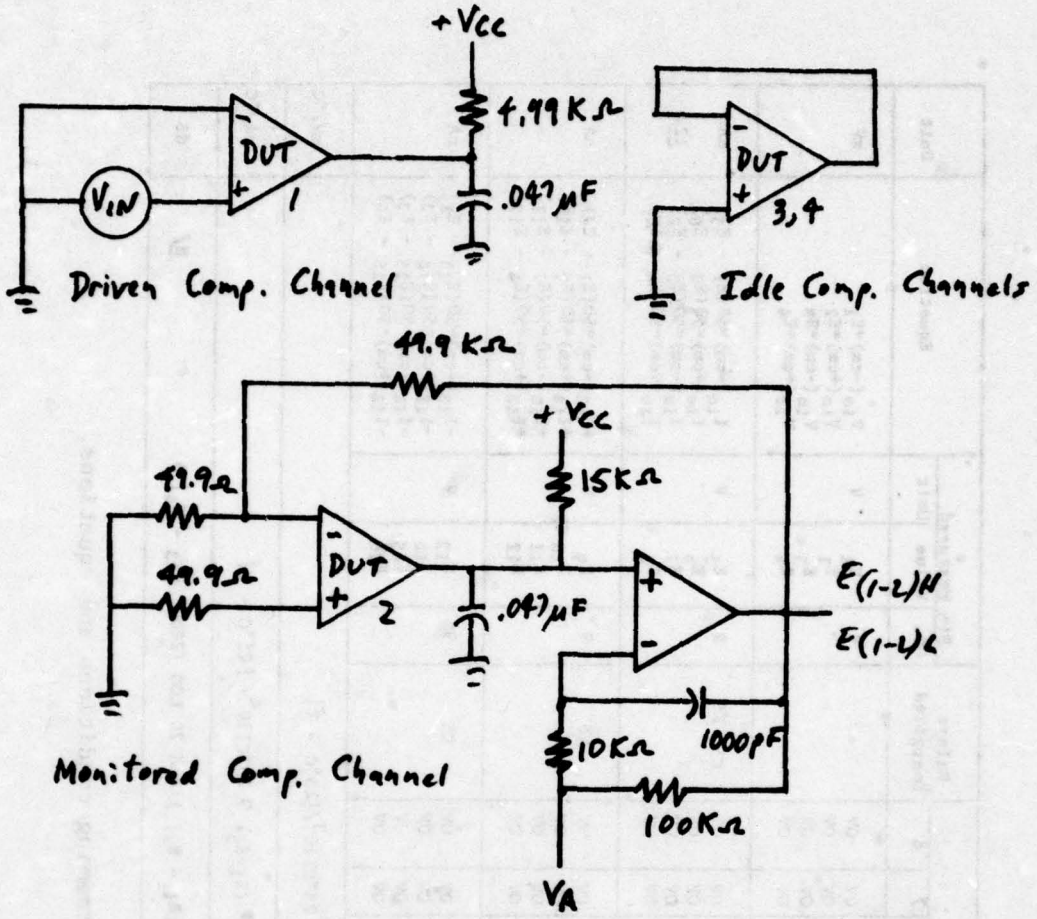
   b. Change V_{ref} from the value obtained in(a) above by the required V_{OD} (overdrive).

   c. Apply V_{in} and measure the response time.

3. All resistor tolerances are ± 1% and all capacitor tolerances are ± 10%.

4. The output capacitance includes scope, probe and jig capacitance.

Figure 2-3 Response time test circuit. (cont'd.)



Channel separation test condition & equations[1/]

Applied Voltages				Measure (V)	Equation (dB)
$+V_{cc}$ (V)	$-V_{cc}$ (V)	V_{in} (V)	V_A (V)		
+30	0	+ 1	15	$E_{(1-2)H}$	$CS_{1-2} = 20 \log \frac{30000}{E_{(1-2)H} - E_{(1-2)L}}$
+30	0	- 1	15	$E_{(1-2)L}$	

1/ The above table shows how to determine channel separation CS_{1-2} with comparator 1 as the driven channel and comp. 2 as the monitored channel. Repeat for all combinations of driven and monitored channels (i.e. CS_{1-3}, CS_{1-4}, CS_{2-1}, CS_{2-3}, CS_{2-4}, CS_{3-1}, CS_{3-2}, CS_{3-4}, CS_{4-1}, CS_{4-2}, and CS_{4-3})

Figure 2-4. Channel separation test circuit.

Parameter Symbol	Programmable Adapter Pins 1/								Relays Energized	Pin Measured			Equation	Unit
	1	2	3	4	5	6	7	8		No.	Value	Unit		
V_{io}(-cm)	-	30V	0V	-	30V	15V	0V	0V	-	9	E_1	V	V_{io}(-cm)=E_1	mV
V_{io}(+cm)	-	2V	-28V	-	2V	-13V	0V	0V			E_2		V_{io}(+cm)=E_2	
V_{io}(-cm)	-	5V	0V	-	5V	1.4V	0V	0V			E_3		V_{io}(-cm)=E_3	
V_{io}(+cm)	-	2V	- 3V	-	2V	-1.0	0V	0V			E_4		V_{io}(+cm)=E_4	
I_{io}(-cm)	-	30V	0V	-	30V	15V	0V	0V	K5, K6	9	E_5	V	I_{io}(-cm)=50(E_1 - E_5)	nA
I_{io}(+cm)	-	2V	-28V	-	2V	-13V	0V	0V			E_6		I_{io}(+cm)=50(E_2 - E_6)	
I_{io}(-cm)	-	5V	0V	-	5V	1.4V	0V	0V			E_7		I_{io}(-cm)=50(E_3 - E_7)	12/
I_{io}(+cm)	-	2V	- 3V	-	2V	-1.0V	0V	0V			E_8		I_{io}(+cm)=50(E_4 - E_8)	
$+I_{iB}$(-cm)	-	30V	0	-	30V	15V	0V	0V	K6	9	E_9	V	$+I_{iB}$(-cm)=50(E_1 - E_9)	nA
$+I_{iB}$(+cm)	-	2V	-28V	-	2V	-13V	0V	0V			E_{10}		$+I_{iB}$(+cm)=50(E_2 - E_{10})	
$+I_{iB}$(-cm)	-	5V	0V	-	5V	1.4V	0V	0V			E_{11}		$+I_{iB}$(-cm)=50(E_7 - E_{11})	
$+I_{iB}$(+cm)	-	2V	- 3V	-	2V	-1.0	0V	0V			E_{12}		$+I_{iB}$(+cm)=50(E_4 - E_{12})	
$-I_{iB}$(-cm)	-	30V	0	-	30V	15V	0V	0V	K5	9	E_{13}	V	$-I_{iB}$(-cm)=50(E_{13} - E_1)	nA
$-I_{iB}$(+cm)	-	2V	-28V	-	2V	-13V	0V	0V			E_{14}		$-I_{iB}$(+cm)=50(E_{14} - E_2)	
$-I_{iB}$(-cm)	-	5V	0V	-	5V	1.4V	0V	0V			E_{15}		$-I_{iB}$(-cm)=50(E_{15} - E_3)	
$-I_{iB}$(+cm)	-	2V	- 3V	-	2V	-1.0V	0V	0V			E_{16}		$-I_{iB}$(+cm)=50(E_{16} - E_4)	
$\Delta V_{io}/\Delta T$		Calculate (E_1 @ T - E_1 @ 25°C)10^3/|25°C - T|												mV/°C
$\Delta I_{io}/\Delta T$		Calculate ((E_1 - E_5) @ T - (E_1-E_5) @ 25°C)10^6/ |25°C - T|												pA/°C
CMR		Calculate 20 LOG (28000/|E_1 - E_2|) and 20 LOG (2400/ |E_3 - E_4|) 8/												dB

Table 2-1 Programming conditions and equations.

Parameter Symbol	Programmable Adapter Pins 1/								Relays Energized	Pin Measured			Equation	Unit
	1	2	3	4	5	6	7	8		No.	Value	Unit		
I_{CEX}	-15V	30V	0V	30V	0V	0V	0V	0V	K7, K8	4	I_{17}	mA	$I_{CEX} = I_{17}$	mA
$+I_{iL}$	-	36V	0V	-	0V	0V	0V	34V	K7, K8	8	I_{18}	nA	$+I_{iL} = I_{18}$	nA
$-I_{iL}$	-	36V	0V	-	0V	0V	34V	0V	K7, K8	7	I_{19}	nA	$-I_{iL} = I_{19}$	
V_{OL}	15V 15V	4.5V 4.5V	0V 0V	4mA 8mA	0V 0V	0V 0V	0V 0V	0V 0V	K7, K8	4	E_{20} E_{21}	V	$V_{OL} = E_{20}$ $V_{OL} = E_{21}$	V
I_{cc}	15V 15V	5V 30V	0V 0V	- -	0V 0V	0V 0V	0V 0V	0V 0V	K7, K8	2	I_{22} I_{23}	mA	$I_{cc} = I_{22}$ $I_{cc} = I_{23}$	mA
A_{VS}	-	15V	0V	-	15V	11V	0V	0V	-	9	E_{24}	V	$A_V = \frac{10}{E_{25} - E_{24}}$	V/mV
	-	15V	0V	-	15V	1V	0V	0V	-	9	E_{25}	V		

Table 2-i Programming conditions and equations. (cont'd.)

20 SEP 77 12:48:40 PARAMETER	INPUT CONDITIONS P1	P2	P3	P4	P5	P6	RELAYS CLOSED	TEST COND	LO-SS	HI-SS	TEST LIMITS LO 25	HI 25	LO125	HI125	UNITS
VIO(-CM) AT 30V	0.00	30.0	0.00	0.00	30.0	15.0	000	E(1)	-8.00	8.00	-5.00	5.00	-8.00	8.00	MV
VIO(+CM) AT 30V	0.00	2.00	-28.0	0.00	2.00	-13.0	000	E(2)	-8.00	8.00	-5.00	5.00	-8.00	8.00	MV
VIO(-CM) AT 5V	0.00	5.00	0.00	0.00	5.00	1.40	000	E(3)	-8.00	8.00	-5.00	5.00	-8.00	8.00	MV
VIO(+CM) AT 5V	0.00	2.00	-3.00	0.00	2.00	-1.00	000	E(4)	-8.00	8.00	-5.00	5.00	-8.00	8.00	MV
D-VIO/D-T FROM 25 OC								E(24)	-30.0	30.0			-30.0	30.0	UV/OC
IIO(-CM) AT 30V	0.00	30.0	0.00	0.00	30.0	15.0	060	E(5)	-100.	100.	-25.0	25.0	-25.0	25.0	NA
IIO(+CM) AT 30V	0.00	2.00	-28.0	0.00	2.00	-13.0	060	E(6)	-100.	100.	-25.0	25.0	-25.0	25.0	NA
IIO(-CM) AT 5V	0.00	5.00	0.00	0.00	5.00	1.40	060	E(7)	-100.	100.	-25.0	25.0	-25.0	25.0	NA
IIO(+CM) AT 5V	0.00	2.00	-3.00	0.00	2.00	-1.00	060	E(8)	-100.	100.	-25.0	25.0	-25.0	25.0	NA
D-IIO/D-T FROM 25 OC								E(25)	-600.	600.			-300.	300.	PA/OC
IIB(+)(-CM) AT 30V	0.00	30.0	0.00	0.00	30.0	15.0	040	E(9)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(+)(+CM) AT 30V	0.00	2.00	-28.0	0.00	2.00	-13.0	040	E(10)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(+)(-CM) AT 5V	0.00	5.00	0.00	0.00	5.00	1.40	040	E(11)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(+)(+CM) AT 5V	0.00	2.00	-3.00	0.00	2.00	-1.00	040	E(12)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(-)(-CM) AT 30V	0.00	30.0	0.00	0.00	30.0	15.0	020	E(13)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(-)(+CM) AT 30V	0.00	2.00	-28.0	0.00	2.00	-13.0	020	E(14)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(-)(-CM) AT 5V	0.00	5.00	0.00	0.00	5.00	1.40	020	E(15)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
IIB(-)(+CM) AT 5V	0.00	2.00	-3.00	0.00	2.00	-1.00	020	E(16)	-300.	-1.00	-100.	-1.00	-100.	-1.00	NA
CMR AT 30V	0.00	0.00	0.00	0.00	0.00	0.00	000	E(26)	76.0	0.00	76.0	0.00	76.0	0.00	dB
CMR AT 5V	0.00	0.00	0.00	0.00	0.00	0.00	000	E(27)	70.0	0.00	70.0	0.00	70.0	0.00	dB
ICEX	-15.0	30.0	0.00	30.0	0.00	0.00	300	E(17)	0.00	100.M	0.00	100.M	0.00	1.00	UA
VOL AT 4MA	15.0	4.50	0.00	4.00	0.00	0.00	300	E(18)	0.00	700.M	0.00	400.M	0.00	700.M	V
VOL AT 6MA	15.0	4.50	0.00	6.00	0.00	0.00	300	E(19)	0.00	1.00	0.00	1.00	0.00	1.00	V
ICC AT PS = 5V, 0V	15.0	5.00	0.00	0.00	0.00	0.00	300	E(20)	0.00	4.00	0.00	2.00	0.00	2.00	MA
ICC AT PS = 30V, 0V	15.0	30.0	0.00	0.00	0.00	0.00	300	E(21)	0.00	5.00	0.00	3.00	0.00	3.00	MA
AV	0.00	15.0	0.00	0.00	15.0	1.00	000	E(23)	25.0	0.00	50.0	0.00	25.0	0.00	V/MV
URLH WITH VOD=5MV	0.00	5.00	0.00	0.00	0.00	0.00	700	E(28)	0.00	5.00	0.00	5.00	0.00	5.00	US
URLH WITH VOD=100MV	0.00	5.00	0.00	0.00	0.00	0.00	700	E(29)	0.00	5.00	0.00	5.00	0.00	5.00	US
URHL WITH VOD=5MV	0.00	5.00	0.00	0.00	0.00	0.00	700	E(30)	0.00	5.00	0.00	5.00	0.00	5.00	US
URHL WITH VOD=100MV	0.00	5.00	0.00	0.00	0.00	0.00	700	E(31)	0.00	5.00	0.00	5.00	0.00	5.00	US

Table 2-2 LM139 test conditions and limits.

DEVICE TYPE: 139 ; S/N: 101 ; DATE CODE: 729 ; 06 OCT 77 16:22:03

PARAMETER	25 DEG C CMPAR1	CMPAR2	CMPAR3	CMPAR4	-55 DEG C CMPAR1	CMPAR2	CMPAR3	CMPAR4	125 DEG C CMPAR1	CMPAR2	CMPAR3	CMPAR4	UNITS
VIO(-CM) AT 30V	-1.10	-1.21	-950.M	528.M	-1.04	-1.12	-628.M	458.M	-1.25	-1.38	-1.46	670.M	MV
VIO(+CM) AT 30V	-1.09	-1.11	-1.70	16.0M	-1.07	-1.04	-1.30	-20.9M	-1.18	-1.17	-2.33	628.M	MV
VIO(-CM) AT 5V	-1.22	-1.07	-1.12	640.M	-1.17	-980.M	-790.M	585.M	-1.33	-1.17	-1.63	823.M	MV
VIO(+CM) AT 5V	-1.17	-1.00	-1.24	603.M	-1.14	-960.M	-880.M	512.M	-1.28	-1.10	-1.72	828.M	MV
D-VIO/D-T FROM 25 OC					-750.M	-1.25	-4.03	869.M	-1.45	-1.60	-5.15	1.42	UV/OC
IIO(-CM) AT 30V	4.25	1.00	-18.8	-35.6 *	1.50	750.M	-3.48	-49.3	1.00	2.00	1.75	-4.25	NA
IIO(+CM) AT 30V	1.50	500.M	-20.5	653. *	-750.M	750.M	-3.00	651. *	-500.M	500.M	250.M	-1.02	NA
IIO(-CM) AT 5V	500.M	-1.25	-21.0	-162. *	-1.50	1.00	-3.50	-191. *	1.00	0.00	1.50	-3.67	NA
IIO(+CM) AT 5V	2.25	250.M	-21.7	683. *	-1.00	-500.M	-3.75	578. *	1.50	250.M	250.M	-3.32	NA
D-IIO/D-T FROM 25 OC					34.4	3.13	-191.	172.	-32.5	10.0	205.	314. *	PA/OC
IIB(+)(-CM) AT 30V	-23.9	-24.2	-47.5	-96.6	-26.4	-28.2	-32.1	-90.1	-17.5	-15.3	-18.0	-23.0	NA
IIB(+)(+CM) AT 30V	-12.3	-12.8	-35.2	653. *	-14.5	-14.5	-18.5	651. *	-8.50	-8.50	-8.75	-10.3	NA
IIB(+)(-CM) AT 5V	-23.8	-23.1	-43.8	-188. *	-28.2	-25.8	-29.9	-209.	-14.5	-16.5	-14.3	-18.9	NA
IIB(+)(+CM) AT 5V	-20.2	-18.6	-40.1	668. *	-24.7	-23.2	-26.1	541. *	-12.3	-15.2	-13.0	-15.6	NA
IIB(-)(-CM) AT 30V	-27.5	-26.0	-27.8	-57.0	-29.5	-29.2	-28.6	-39.7	-18.5	-18.8	-17.5	-19.0	NA
IIB(-)(+CM) AT 30V	-13.7	-13.0	-15.0	-37.5	-14.3	-15.3	-15.0	-20.5	-8.50	-9.00	-8.25	-9.75	NA
IIB(-)(-CM) AT 5V	-24.0	-22.5	-25.5	-46.8	-25.5	-27.2	-27.5	-36.5	-16.5	-16.0	-16.7	-17.9	NA
IIB(-)(+CM) AT 5V	-22.3	-21.7	-21.7	-44.5	-25.0	-24.2	-25.0	-33.6	-15.0	-14.2	-15.0	-16.3	NA
CMR AT 30V	129.	108.	91.4	94.8	119.	112.	92.4	95.3	113.	103.	90.3	116.	dB
CMR AT 5V	94.5	90.7	86.0	96.2	98.1	102.	88.5	90.4	94.5	90.1	88.0	113.	dB
ICEX	1.45 *	1.37 *	10.2 *	10.2 *	-5.00M	-5.00M	7.80 *	8.60 *	-5.00M	-5.00M	-5.00M	-5.00M	UA
VOL AT 4MA	200.M	204.M	203.M	201.M	175.M	174.M	176.M	169.M	273.M	275.M	275.M	271.M	V
VOL AT 6MA	283.M	283.M	283.M	281.M	245.M	245.M	248.M	240.M	384.M	385.M	381.M	377.M	V
ICC AT PS = 5V, 0V	768.M	764.M	761.M	761.M	906.M	911.M	903.M	907.M	523.M	522.M	520.M	516.M	MA
ICC AT PS = 30V, 0V	931.M	924.M	922.M	921.M	1.08	1.08	1.08	1.08	643.M	642.M	638.M	636.M	MA
AV	667.	250.	400.	225.	667.	286.	200.	213.	1.00K	154.	333.	200.	V/MV
tRLH WITH VOD=5MV	1.45	1.39	1.51	1.50	1.24	1.19	1.22	1.22	2.09	1.94	2.03	1.97	US
tRLH WITH VOD=50MV	335.M	335.M	335.M	345.M	315.M	315.M	310.M	315.M	405.M	405.M	405.M	405.M	US
tRHL WITH VOD=5MV	800.M	840.M	815.M	860.M	670.M	660.M	695.M	685.M	1.21	1.14	1.20	1.24	US
tRHL WITH VOD=50MV	345.M	335.M	335.M	355.M	305.M	300.M	305.M	305.M	440.M	455.M	445.M	445.M	US

Table 2-3 Typical LM139 data output sheet.

STATISTICAL DATA FOR LM139 SERIALIZED PARTS AT 25 DEG C 06 DEC 77 15:58:29 REVISED LIMITS EXCL. X-SERIES PARTS

PARAMETER	LOW VALUE 2	HIGH VALUE 2	MEAN $\bar{X}$ 3	SIGMA σ 3	SAMPLE SIZE 2	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM 4/ 2	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 4/	UNITS
VIO(-CM) AT 30V	-4.49	4.62	356.M	1.42	352	95.2	99.1	0.00	-5.00	-10.0	3.77	0.00	5.00	10.0	3.27	MV
VIO(+CM) AT 30V	-4.34	4.18	46.8M	1.34	352	95.7	98.9	0.00	-5.00	-10.0	3.76	0.00	5.00	10.0	3.69	MV
VIO(-CM) AT 5V	-4.03	4.43	288.M	1.33	352	94.9	99.1	0.00	-5.00	-10.0	3.96	0.00	5.00	10.0	3.53	MV
VIO(+CM) AT 5V	-4.01	4.32	237.M	1.29	352	95.2	99.1	0.00	-5.00	-10.0	4.05	0.00	5.00	10.0	3.48	MV
D-VIO/D-T FROM -55 C	-12.7	12.4	380.M	3.28	352	95.5	98.6	0.00	-25.0	-60.0	(1.73)	0.00	25.0	60.0	(7.5)	UV/OC
IIO(-CM) AT 30V	-135.	183.	-238.M	13.8	352	98.9	99.1	568.M	-25.0	-200.	1.79	568.M	25.0	200.	1.82	NA
IIO(+CM) AT 30V	-131.	24.5	-820.M	7.82	350	98.0	98.9	284.M	-25.0	-200.	3.09	568.M	25.0	200.	3.30	NA
IIO(-CM) AT 5V	-134.	115.	-829.M	10.8	352	99.1	99.4	284.M	-25.0	-200.	2.24	284.M	25.0	200.	2.39	NA
IIO(+CM) AT 5V	-135.	135.	-596.M	11.2	352	99.4	99.4	284.M	-25.0	-200.	2.19	284.M	25.0	200.	2.29	NA
D-IIO/D-T FROM -55 C	-332.	553.	1.77	66.8	350	94.9	96.9	284.M	-400.	-1.20K	(4.0)	568.M	400.	1.20K	(5.98)	PA/OC
IIB(+)(-CM) AT 30V	-228.	-11.2	-43.2	21.7	352	96.9	99.4	568.M	-100.	-400.	2.61	0.00	-1.00	-10.0M	1.94	NA
IIB(+)(+CM) AT 30V	-175.	-2.75	-25.1	16.4	349	97.4	99.1	284.M	-100.	-400.	4.58	852.M	-1.00	-10.0M	1.47	NA
IIB(+)(-CM) AT 5V	-213.	-9.50	-38.5	19.6	352	98.3	99.7	284.M	-100.	-400.	3.13	0.00	-1.00	-10.0M	1.91	NA
IIB(+)(+CM) AT 5V	-204.	-7.35	-34.1	18.7	352	98.0	99.7	284.M	-100.	-400.	3.51	0.00	-1.00	-10.0M	1.77	NA
IIB(-)(-CM) AT 30V	-244.	-11.8	-45.6	26.0	352	98.3	98.9	1.42	-100.	-400.	2.10	0.00	-1.00	-10.0M	1.72	NA
IIB(-)(+CM) AT 30V	-172.	-3.20	-24.7	16.1	352	97.7	99.7	284.M	-100.	-400.	4.68	0.00	-1.00	-10.0M	3.47	NA
IIB(-)(-CM) AT 5V	-179.	-9.60	-38.6	18.5	352	96.0	99.7	284.M	-100.	-400.	3.31	0.00	-1.00	-10.0M	2.03	NA
IIB(-)(+CM) AT 5V	-144.	-7.75	-34.6	17.2	352	96.6	99.7	284.M	-100.	-400.	3.79	0.00	-1.00	-10.0M	1.95	NA
CMR AT 30V	85.2	143.	99.6	8.08	352	96.3	98.0	0.00	76.0	65.0	2.92	----	----	300.	----	dB
CMR AT 5V	78.1	160.	92.8	10.4	352	95.2	98.3	0.00	70.0	65.0	2.19	----	----	300.	----	dB
ICEX	-5.00M	241.M	-1.75M	23.5M	345	96.0	96.3	----	----	-10.0M	----	(3.13)	100.M	300.M	4.33	UA
VOL AT 4MA	184.M	409.M	249.M	45.5M	352	94.0	98.9	----	----	100.M	----	568.M	400.M	1.00	3.33	V
VOL AT 6MA	263.M	587.M	360.M	65.2M	352	94.0	98.9	----	----	100.M	----	0.00	600.M	1.00	3.69	V
ICC AT PS = 5V, 0V	592.M	1.54	988.M	280.M	352	100.	100.	----	----	0.00	----	0.00	2.00	10.0	3.61	MA
ICC AT PS = 30V, 0V	736.M	1.87	1.25	338.M	352	100.	100.	----	----	0.00	----	0.00	3.00	10.0	5.19	MA
AV	37.0	1.00K	248.	155.	352	96.0	98.9	284.M	50.0	1.00	1.28	----	----	900.K	----	V/MV
tRLH WITH VOD=5MV	1.25	3.77	2.06	678.M	342	90.6	97.2	----	----	5.00M	----	0.00	5.00	10.0	4.33	US
tRLH WITH VOD=50MV	315.M	665.M	415.M	95.9M	352	92.3	100.	----	----	5.00M	----	0.00	800.M	10.0	4.01	US
tRHL WITH VOD=5MV	615.M	1.43	1.02	250.M	342	97.2	97.2	----	----	5.00M	----	0.00	2.50	10.0	(1.92)	US
tRHL WITH VOD=50MV	255.M	500.M	386.M	59.1M	352	99.4	100.	----	----	5.00M	----	0.00	800.M	10.0	(7.00)	US

1/ = EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

3/ ○ FIGURE OF MERIT GREATER THAN 5 OR LESS THAN 1

3/ ○ % FAIL GREATER THAN 3 %

4/ FIGURE OF MERIT DEFINITIONS

$$\text{LO-FM} = \frac{\bar{X} - \text{LOW LIMIT}}{\sigma}$$

$$\text{HI-FM} = \frac{\text{HIGH LIMIT} - \bar{X}}{\sigma}$$

Table 2-4 LM139 data at 25°C.

STATISTICAL DATA FOR LM139 SERIALIZED PARTS AT -55 DEG C

REVISED LIMITS EXCL. Y-SERIES PARTS

PARAMETER	LOW VALUE	HIGH VALUE	MEAN $\bar{X}$	SIGMA σ	SAMPLE SIZE	X IN 2 SIGMA	X IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM 4/	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 4/	UNITS
	s	s	s	s	s						s				s	
VIO(-CM) AT 30V	-4.98	4.07	325.M	1.35	352	95.2	99.4	0.00	-7.00	-10.0	5.41	0.00	7.00	10.0	4.95	MV
VIO(+CM) AT 30V	-5.21	3.62	-26.8M	1.28	352	95.7	99.4	0.00	-7.00	-10.0	5.44	0.00	7.00	10.0	5.43	MV
VIO(-CM) AT 5V	-4.65	3.89	231.M	1.26	352	95.5	99.4	0.00	-7.00	-10.0	5.70	0.00	7.00	10.0	5.73	MV
VIO(+CM) AT 5V	-4.72	3.76	165.M	1.22	352	95.7	99.4	0.00	-7.00	-10.0	5.89	0.00	7.00	10.0	5.90	MV
IIO(-CM) AT 30V	-47.5	43.8	-542.M	9.90	352	93.8	96.9	0.00	-75.0	-200.	7.55	0.00	75.0	200.	7.45	NA
IIO(+CM) AT 30V	-27.5	72.5	-445.M	6.39	350	94.9	98.0	0.00	-75.0	-200.	11.2	568.M	75.0	200.	11.3	NA
IIO(-CM) AT 5V	-41.0	39.8	-1.09	8.83	352	93.8	96.9	0.00	-75.0	-200.	8.12	0.00	75.0	200.	8.01	NA
IIO(+CM) AT 5V	-35.7	86.4	-429.M	9.29	352	95.2	97.7	0.00	-75.0	-200.	8.01	284.M	75.0	200.	8.15	NA
IIB(+)(-CM) AT 30V	-158.	-13.7	-49.3	24.2	352	95.5	99.1	0.00	-200.	-400.	4.72	0.00	-1.00	-10.0M	1.99	NA
IIB(+)(+CM) AT 30V	-87.5	-3.90	-29.2	17.1	348	96.6	98.9	0.00	-200.	-400.	10.0	1.14	-1.00	-10.0M	1.65	NA
IIB(+)(-CM) AT 5V	-141.	-11.3	-44.8	22.3	352	96.3	98.9	0.00	-200.	-400.	6.92	0.00	-1.00	-10.0M	1.96	NA
IIB(+)(+CM) AT 5V	-124.	-8.50	-39.7	20.7	351	96.3	99.1	0.00	-200.	-400.	7.73	284.M	-1.00	-10.0M	1.87	NA
IIB(-)(-CM) AT 30V	-135.	-14.2	-50.1	24.1	352	95.7	99.1	0.00	-200.	-400.	6.33	0.00	-1.00	-10.0M	2.04	NA
IIB(-)(+CM) AT 30V	-72.2	-3.75	-28.8	16.5	352	97.7	100.	0.00	-200.	-400.	10.4	0.00	-1.00	-10.0M	1.68	NA
IIB(-)(-CM) AT 5V	-121.	-11.8	-44.6	21.2	352	95.5	99.4	0.00	-200.	-400.	6.98	0.00	-1.00	-10.0M	2.05	NA
IIB(-)(+CM) AT 5V	-108.	-9.25	-40.3	20.0	352	95.2	99.7	0.00	-200.	-400.	7.50	0.00	-1.00	-10.0M	1.96	NA
CMR AT 30V	85.9	145.	99.0	7.60	352	95.7	98.6	0.00	76.0	65.0	3.02	----	----	300.	----	dB
CMR AT 5V	79.1	160.	91.9	10.9	352	96.9	98.9	0.00	70.0	65.0	2.02	----	----	300.	----	dB
ICEX	-5.00M	269.M	-1.50M	25.4M	339	94.6	94.6	----	----	10.0M	----	5.11	100.M	300.M	3.99	UA
VOL AT 4MA	135.M	339.M	211.M	38.4M	352	94.0	99.1	----	----	100.M	----	0.00	600.M	1.00	10.1	V
VOL AT 6MA	221.M	485.M	305.M	54.9M	352	94.0	99.1	----	----	100.M	----	0.00	1.00	1.00	12.7	V
ICC AT PS = 5V, 0V	694.M	1.72	1.14	300.M	352	100.	100.	----	----	0.00	----	0.00	4.00	10.0	9.53	MA
ICC AT PS = 30V, 0V	869.M	2.07	1.43	360.M	352	100.	100.	----	----	0.00	----	0.00	5.00	10.0	9.93	MA
AV	47.6	1.00K	254.	166.	352	96.6	98.0	0.00	25.0	1.00	1.37	----	----	900.K	----	V/MV
tRLH WITH VOD=5MV	1.03	3.14	1.71	564.M	347	92.6	98.6	----	----	5.00M	----	0.00	5.00	10.0	5.8	US
tRLH WITH VOD=50MV	295.M	610.M	381.M	84.7M	352	92.9	100.	----	----	5.00M	----	0.00	800.M	10.0	4.95	US
tRHL WITH VOD=5MV	485.M	1.20	836.M	212.M	347	98.6	98.6	----	----	5.00M	----	0.00	2.50	10.0	7.85	US
tRHL WITH VOD=50MV	230.M	430.M	336.M	53.2M	352	98.9	100.	----	----	5.00M	----	0.00	800.M	10.0	8.75	US

1/ s EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

2/ ○ FIGURE OF MERIT GREATER THAN 5 OR LESS THAN 1

3/ ○ % FAIL GREATER THAN 3%

4/ FIGURE OF MERIT DEFINITIONS

$$\text{LO-FM} = \frac{\bar{X} - \text{LOW LIMIT}}{\sigma}$$

$$\text{HI-FM} = \frac{\text{HIGH LIMIT} - \bar{X}}{\sigma}$$

Table 2-5 LM139 data at -55°C.

STATISTICAL DATA FOR LM139 SERIALIZED PARTS AT 125 DEG C 04 DEC 77 16:33:50 REVISED LIMITS EXCL X-SERIES PARTS

PARAMETER	LOW VALUE x	HIGH VALUE x	MEAN $\bar{x}$ x	SIGMA σ x	SAMPLE SIZE x	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM 4/ x	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 4/ x	UNITS
VIO(-CM) AT 30V	-7.36	5.53	363.M	1.71	352	94.3	99.1	284.M	-7.00	-10.0	4.31	0.00	7.00	10.0	3.86	MV
VIO(+CM) AT 30V	-4.48	5.18	172.M	1.56	352	94.6	99.1	0.00	-7.00	-10.0	4.60	0.00	7.00	10.0	4.38	MV
VIO(-CM) AT 5V	-4.76	5.36	362.M	1.56	352	94.6	99.1	0.00	-7.00	-10.0	4.72	0.00	7.00	10.0	4.25	MV
VIO(+CM) AT 5V	-4.63	5.26	359.M	1.51	352	94.6	99.1	0.00	-7.00	-10.0	4.89	0.00	7.00	10.0	4.41	MV
D-VIO/D-T FROM 25 OC	-28.3	21.2	250.M	4.32	351	95.7	98.6	568.M	-25.0	-60.0	3.5	0.00	25.0	60.0	5.7	UV/OC
IIO(-CM) AT 30V	-27.7	51.4	-85.5M	4.49	352	96.6	98.9	284.M	-25.0	-200.	5.5	284.M	25.0	200.	6.5	NA
IIO(+CM) AT 30V	-6.25	7.98	-447.M	1.57	351	95.5	98.3	284.M	-25.0	-200.	15.9	0.00	25.0	200.	16.0	NA
IIO(-CM) AT 5V	-13.5	10.6	-498.M	2.74	352	93.8	98.3	0.00	-25.0	-200.	7.3	0.00	25.0	200.	7.3	NA
IIO(+CM) AT 5V	-11.8	9.95	-440.M	2.31	352	95.2	98.0	0.00	-25.0	-200.	10.4	0.00	25.0	200.	11.0	NA
D-IIO/D-T FROM 25 OC	-590.	479.	2.98	56.1	350	95.5	98.3	568.M	-300.	-1.20K	4.1	568.M	300.	1.20K	5.3	PA/OC
IIB(+)(-CM) AT 30V	-209.	-7.50	-32.9	19.4	352	98.3	99.1	852.M	-100.	-400.	3.47	0.00	-1.00	-10.0M	1.65	NA
IIB(+)(+CM) AT 30V	-48.0	-1.18	-17.2	10.6	351	97.7	100.	0.00	-100.	-400.	7.7	284.M	-1.00	-10.0M	1.54	NA
IIB(+)(-CM) AT 5V	-67.9	-4.87	-27.1	13.0	352	97.2	99.7	0.00	-100.	-400.	5.6	0.00	-1.00	-10.0M	2.00	NA
IIB(+)(+CM) AT 5V	-58.2	-4.00	-23.8	12.3	352	97.2	100.	0.00	-100.	-400.	6.1	0.00	-1.00	-10.0M	1.85	NA
IIB(-)(-CM) AT 30V	-219.	-7.25	-35.7	22.1	352	97.7	98.9	1.42	-100.	-400.	2.91	0.00	-1.00	-10.0M	1.57	NA
IIB(-)(+CM) AT 30V	-46.7	-1.25	-16.8	10.4	350	96.9	99.7	0.00	-100.	-400.	7.9	568.M	-1.00	-10.0M	1.52	NA
IIB(-)(-CM) AT 5V	-61.9	-6.00	-27.1	12.8	352	96.9	100.	0.00	-100.	-400.	5.7	0.00	-1.00	-10.0M	2.04	NA
IIB(-)(+CM) AT 5V	-57.2	-4.50	-24.0	12.2	352	97.2	100.	0.00	-100.	-400.	6.0	0.00	-1.00	-10.0M	1.89	NA
CMR AT 30V	72.8	135.	101.	8.98	352	94.0	98.0	284.M	76.0	65.0	2.73	-----	----	300.	-----	dB
CMR AT 5V	75.0	212.	92.5	14.0	352	97.7	98.3	0.00	70.0	65.0	1.60	-----	----	300.	-----	dB
ICEX	-5.00M	550.M	1.34M	34.7M	349	98.3	98.6	-----	-----	-10.0M	------	852.M	1.00	5.00	27.	UA
VOL AT 4MA	247.M	585.M	352.M	63.8M	352	94.6	98.9	-----	-----	100.M	------	0.00	600.M	1.00	3.89	V
VOL AT 6MA	349.M	870.M	513.M	98.7M	352	95.2	98.9	-----	-----	100.M	------	0.00	1.00	1.00	4.94	V
ICC AT PS = 5V, 0V	411.M	1.14	687.M	221.M	352	98.6	100.	-----	-----	0.00	------	0.00	2.00	10.0	5.9	MA
ICC AT PS = 30V, 0V	523.M	1.41	885.M	270.M	352	100.	100.	-----	-----	0.00	------	0.00	3.00	10.0	7.0	MA
AV	9.25	1.54K	230.	185.	352	95.2	97.7	1.14	25.0	1.00	1.11	-----	----	900.K	-----	V/MV
tRLH WITH VOD=5MV	1.68	5.30	2.92	1.02	334	87.2	100.	-----	-----	5.00M	------	0.00	7.00	10.0	4.02	US
tRLH WITH VOD=50MV	355.M	840.M	509.M	131.M	352	92.6	100.	-----	-----	5.00M	------	0.00	1.00	10.0	3.75	US
tRHL WITH VOD=5MV	895.M	2.01	1.45	340.M	336	95.5	95.5	-----	-----	5.00M	------	0.00	3.00	10.0	4.57	US
tRHL WITH VOD=50MV	335.M	655.M	512.M	76.2M	352	98.9	100.	-----	-----	5.00M	------	0.00	1.00	10.0	4.41	US

1/ # EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

2/ ○ FIGURE OF MERIT GREATER THAN 5 OR LESS THAN 1

3/ ○ % FAIL GREATER THAN 3 %

4/ FIGURE OF MERIT DEFINITIONS

$$\text{LO-FM} = \frac{\bar{x} - \text{LOW LIMIT}}{\sigma}$$

$$\text{HI-FM} = \frac{\text{HIGH LIMIT} - \bar{x}}{\sigma}$$

Table 2-6 LM139 data at 125°C.

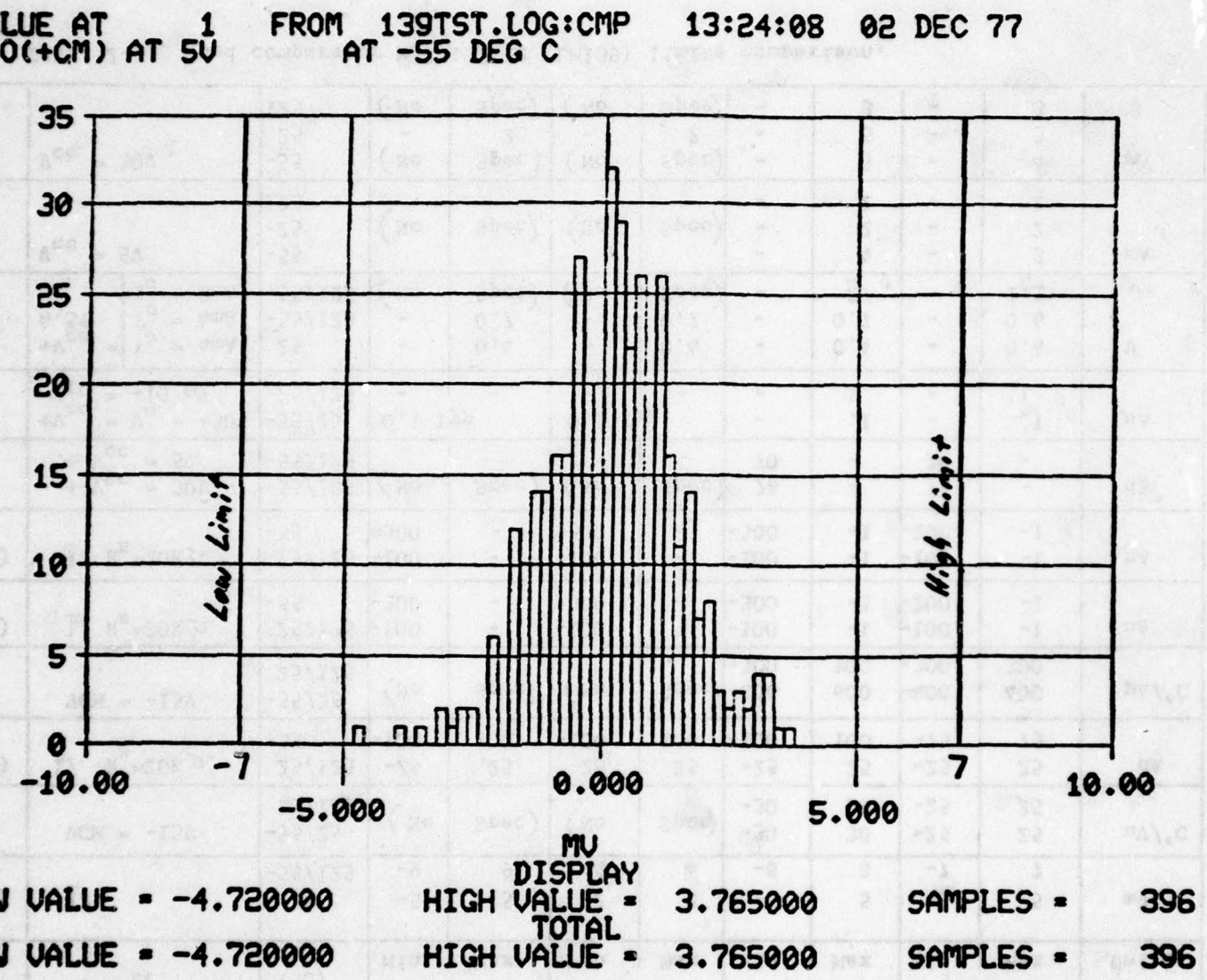


Figure 2-5 Typical histogram of V_{io}.

Parameter Symbol	Conditions $5V < +V_{cc} < 30V$	T_A (°C)	LM139 Cat. Min	LM139 Cat. Max	LM139A Cat. Min	LM139A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /112 Min	GEOS /112 Max	Units
V_{IO} (±CM)	1/	25	-5	5	-2	2	-5	5	-5	5	mV
		-55/125	-9	9	-4	4	-8	8	-7	7	
$\Delta V_{IO}/\Delta T$	VCM = -15V	-55/25	(No	Spec)	(No	Spec)	-30	30	-25	25	uV/°C
		25/125					-30	30	-25	25	
I_{IO} (±CM)	1/ R_s=20KΩ	25/125	-25	25	-25	25	-25	25	-25	25	nA
		-55	-100	100	-100	100	-100	100	-75	75	
$\Delta I_{IO}/\Delta T$	VCM = -15V	-55/25	(No	Spec)	(No	Spec)	-600	600	-400	400	pA/°C
		25/125					-300	300	-300	300	
$+I_{IB}$ (±CM)	1/ R_s=20KΩ	25/125	-100	-	-100	-	-100	-1	-100	-1	nA
		-55	-300	-	-300	-	-300	-1	-200	-1	
$-I_{IB}$ (±CM)	1/ R_s=20KΩ	25/125	-100	-	-100	-	-100	-1	-100	-1	nA
		-55	-300	-	-300	-	-300	-1	-200	-1	
CMR	+ V_{cc} = 30V	-55/125	(No	Spec)	(No	Spec)	76	-	76	-	dB
	+ V_{cc} = 5V	-55/125					70	-	70	-	
I_{CEX}	$+V_{cc}$ = V_O = +30V	-55/25	0.1 Typ		0.1 Typ		-	.1	-	.1	µA
	V_{ID} = -15 mV	25/125	-	-	-	-	-	1	-	1	
V_{OL}	$+V_{cc}$ = 4.5V, I_O = 4mA	25	-	0.4	-	0.4	-	0.4	-	0.4	V
	I_O = 4mA	-55/125	-	0.7	-	0.7	-	0.7	-	0.6	
	I_O = 8mA	-55/125	(No	Spec)	(No	Spec)	-	2/	-	1.5	
I_{ec}	V_{cc} = 5V	-55					-	4	-	3	mA
		25	(No	Spec)	(No	Spec)	-	2	-	2	
		125					-	2	-	2	
	V_{cc} = 30V	-55	(No	Spec)	(No	Spec)	-	5	-	4	mA
		25	-	2	-	2	-	3	-	3	
		125	(No	Spec)	(No	Spec)	-	3	-	3	

Table 2-7. Quad comparator M38510/112 (LM139) limits comparison.

Parameter Symbol	Conditions 5V < + V_{cc} < 30V	T_A (°C)	LM139 Cat. Min	LM139 Cat. Max	LM139A Cat. Min	LM139A Cat. Max	JC-41 Rec. Min	JC-41 Rec. Max	GEOS /112 Min	GEOS /112 Max	Units
$+I_{iL}$	+ V_{cc} = 36V V_{+I} = 34V, V_{-I} = 0V	-55/125		3/		3/	No Spec		0	500	nA
$-I_{iL}$	+ V_{cc} = 36V V_{+I} = 0V, V_{-I} = 34V	-55/125		3/		3/	No Spec		0	500	nA
A_{vs}	+ V_{cc} = 15V RL = 15 KΩ	25 -55/125	(200 typ) (No Spec)		50 (No Spec)	-	50 25	-	50 25	-	V/mV
CS	+ V_{cc} = 30 V	25	(No Spec)		(No Spec)		(No Spec)		80	-	dB
t_{RLH}	+ V_{cc} = 5V, RL = 5.1K, V_{OD}= 5 mV	-55/25 125	1.3 typ @ 25°C		1.3 typ @ 25°C		- @ 25°C	5	- -	5 7	µs
	V_{OD}= 50mV	-55/25 125	(No Spec)		(No Spec)		(No Spec)		- -	0.8 1.0	
t_{RHL}	+ V_{cc} = 5V, RL = 5.1KΩ, V_{OD}= 5 mV	-55/25 125	1.3 typ @ 25°C		1.3 typ @ 25°C		- @ 25°C	5	- -	2.5 3	µs
	V_{OD}= 50mV	-55/25 125	(No Spec)		(No Spec)		(No Spec)		- -	0.8 1.0	

Notes:
1/ V_{IO}, I_{IO} and $\pm I_{IB}$ are measured at $+V_{cc}$ = 30V and 5V with an input range from ground to 2V below V_{cc}.
2/ JC-41 specified a V_{OL} condition of 1.5 V at which $I_{OL(min)}$ - 8 mA @ 25°C and 6mA @-55/125°C.
3/ Differential input voltage is specified at 36V for the LM139 and V+ for the LM139A.

Table 2-7. Quad comparator M38510/112 (LM139) comparison. (cont'd.)

Characteristic	Symbol	Conditions 5 V < + V_{cc} < 30 V (Paragraph 3.4 and Figure 4 unless otherwise indicated)		Limits Min	Limits Max	Units
Input offset voltage	V_{io} (±CM)	1/	T_A = 25°C	-5	5	mV
			-55°C ≤ T_A ≤ 125°C	-7	7	
Input offset Voltage Temperature Sensitivity	$\frac{\Delta V_{io}}{\Delta T}$	ΔT_A from -55°C to + 25°C		-25	25	μV/°C
		ΔT_A from +25°C to + 125°C		-25	25	
Input offset current	I_{io} (± CM)	1/ R_s = 20 KΩ	25°C ≤ T_A ≤ 125°C	-25	25	nA
			T_A = -55°C	-75	75	
Input offset current temperature sensitivity	$\frac{\Delta I_{io}}{\Delta T}$	T_A from -55°C to + 25°C		-400	400	pA/°C
		T_A from +25°C to + 125°C		-300	300	
Input bias current	$+I_{iB}$ (±CM)	1/ R_s = 20 KΩ	25°C ≤ T_A ≤ 125°C	-100	-1	nA
			T_A = -55°C	-200	-1	
	$-I_{iB}$ (±CM)	1/ R_s = 20 KΩ	25°C ≤ T_A ≤ 125°C	-100	-1	nA
			T_A = -55°C	-200	-1	
Input Voltage Common Mode Rejection	CMR	2/	+ V_{cc} = 30 V	76	-	dB
			+ V_{cc} = 5 V	70	-	
Output Leakage	I_{CEX}	+ V_{cc} = V_o = + 30 V	- 55°C ≤ T_A ≤ 25°C	-	0.1	μA
			25°C < T_A ≤ 125°C	-	1.0	

Table 2-8 MIL-M-38510/112-01 recommended specifications.

NOTES:

1. V_{iO}, I_{iO} and $\pm I_{iB}$ shall be measured at the common mode extremes at 30 V and 5 V as shown below:

Condition	Common Mode	$+ V_{cc}$	$- V_{cc}$	V_{in}	V_O
1	(-CM)	30 V	0 V	OV	15 V
2	(+CM)	2 V	-28 V	OV	-13 V
3	(-CM)	5 V	0 V	OV	1.4 V
4	(+CM)	2 V	- 3 V	OV	-1.0 V

2. CMR shall be calculated from V_{iO} measurements defined in note 1/.

Table 2-8 MIL-M-38510/112-01 recommended specification.

Table 2-8 MIL-M-38510/112-01 recommended specifications. (cont'd.)

Characteristic	Symbol	Conditions 5 V $\leq +V_{cc} \leq$ 30 V (Paragraph 3.4 and Figure 4 unless otherwise indicated)	Limits Min	Limits Max	Units
Input leakage current	$+I_{IL}$	$+V_{cc}$ = 36 V, V_{+I} = 34 V, V_{-I} = 0V	0	500	nA
	$-I_{IL}$	$+V_{cc}$ = 36 V, V_{+I} = 0V, V_{-I} = 34 V	0	500	
Low level output Voltage	V_{OL}	$+V_{cc}$ = 4.5 V, I_o = 4 mA, T_A 25°C	-	0.4	V
		I_o = 4 mA, T_A 125°C	-	0.6	
		I_o = mA, - 55°C $\leq T_A \leq$ 125°C	-	1.5	
Power Supply Current	I_{cc}	V_{ID} = 15 mV, $+V_{cc}$ = 5 V, T_A = -55°C	-	3	mA
		T_A = 25°C	-	2	
		T_A = 125°C	-	2	
		$+V_{cc}$ = 30 V, T_A = -55°C	-	4	
		T_A = 25°C	-	3	
		T_A = 125°C	-	3	
Open loop Voltage Gain	A_{VS}	$+V_{cc}$ = 15 V, R_L = 15 KΩ, T_A = 25°C	50	-	V/mV
		1V $\leq$ V0 $\leq$ 11V, - 55°C $\leq T_A \leq$ 125°C	25	-	
Channel Separation	CS	$+V_{cc}$ = 30 V, T_A = 25°C Fig. 9	80	-	dB
Response Time - low to high level	t_{RLH}	$+V_{cc}$ = 5 V, V_{OD} = 5 mV, V_{in} = 100 mV, R_L = 5.1 KΩ, - 55 $\leq T_A \leq$ 25°C	-	5	μs
		T_A = 125°C	-	7	
		V_{OD} = 50 mV, - 55 $\leq T_A \leq$ 25°C	-	0.8	
		T_A = 125°C	-	1.0	
Response time - high to low level	t_{RHL}	$+V_{cc}$ = 5 V, V_{OD} = 5 mV, V_{in} = 100 mV, R_L = 5.1 KΩ, - 55 $\leq T_A \leq$ 25°C	-	2.5	μs
		T_A = 125°C	-	3	
		V_{OD} = 50 mV, - 55 $\leq T_A \leq$ 25°C	-	0.8	
		T_A = 125°C	-	1.0	

APPENDIX

A2-1 LM139 Data Correlation Between GEOS and AMD

A2-2 LM139 Device Evaluation per GEOS and AMD

TABLE A2-1

LM139 DATA CORRELATION
BETWEEN GEOS AND AMD
S/N 1 @ 25°C

Parameter	Comp.	GEOS	AMD	Spec Limits	Corr.* Limits	Units	Corr.
V_{io} (-CM)	1	.785	1.42	± 5	± 1.1	mV	Yes
@ 30 V	2	-1.43	-1.08				"
	3	1.55	2.02				"
	4	1.61	1.51				"
V_{io} (+CM)	1	.834	1.19				"
@ 30 V	2	-.995	-1.05				"
	3	1.30	1.60				"
	4	1.40	1.11				"
V_{io} (-CM)	1	1.02	1.17				"
@ 5 V	2	-.720	-.71				"
	3	1.32	1.49				"
	4	1.79	1.80				"
V_{io} (+CM)	1	.960	1.11				"
@ 5 V	2	-.670	-.64				"
	3	1.21	1.35				"
	4	1.74	1.72	± 5	± 1.1	mV	"
$+I_{IB}$ (-CM)	1	-45.5	-34.0	-100/-1	±11	nA	No
@ 30 V	2	-48.7	-31.0				No
	3	-36.5	-29.0				Yes
	4	-45.7	-33.0				No
$+I_{IB}$ (+CM)	1	-27.8	-26				Yes
@ 30 V	2	-28.1	-25				"
	3	-25.5	-23				"
	4	-29.0	-26	-100/-1	±11	nA	"
I_{OS} (-CM)	1	1.00	-1.00	± 25	± 5.5	nA	"
@ 30 V	2	-.75	0				"
	3	3.00	-3.00				"
	4	-4.50	0				"
I_{OS} (+CM)	1	-1.12	-1.00				"
@ 30 V	2	-1.25	0				"
	3	1.25	-3.00				"
	4	-1.50	0	± 25	± 5.5	nA	"
I_{cc} @ 5V	All	.72	0.67	2 (max)	± .22	nA	"
V_{OL}	1	.197	-	.4	± .44	V	2
@ 4 mA	2	.190	-	.4	± .44		
V_{cc} = 4.5 V	3	.187	-	.4	± .44		
	4	.187	-	.4	± .44	V	

TABLE A2-1

LM139 DATA CORRELATION
BETWEEN GEOS AND AMD
S/N 1 @ 25°C (cont'd.)

Parameter	Comp.	GEOS	AMD	Spec Limits	Corr.* Limits	Units	Corr. 2
V_{OL} @ 1K, V_{cc} = 5 V	1	-	.31	.5	± .055	V	2
	2	-	.31	.5	± .055		
	3	-	.29	.5	± .055		
	4	-	.29	.5	± .055		
V_{OL} @ 6 mA V_{cc} = 4.5 V	1	.277	-	1.0	± .11		
	2	.272	-	1.0	± .11		
	3	.265	-	1.0	± .11		
	4	.264	-	1.0	± .11	V	2

1/ Corr. limit = ± .11 x spec. limit range.

2/ Correlation cannot be checked since the tests are different.

TABLE A2-2

LM 139 DEVICE EVALUATION

Mfr. Code	S/N	GEOS Results of S-3260 Testing				AMD Test Results			
		Good	Bad	Parameter	Notes	Good	Bad	Parameter	Notes
C1	1	x		$-I_{IB}$(-CM)	1/	x			
C2	2	x				x			
C4	4		x	$+I_{IB}$(+CM)	2/	x			
C5	5	x					x		
C6	6	x				x			
C7	7		x	$-I_{IB}$(-CM)	3/	x			
C8	8	x				x			
C9	9	x				x			
C10	10	x				x			
P3	11	x					x	I_{IO}(+CM)	
P4	12	x				x			
P5	13	x				x			
P6	14	x				x			
P7	15	x				x			
P8	16	x				x			
P9	17	x				x			
P10	18	x				x			
X2	19		x	V_{IO}(+CM)	3,4,5/		x	V_{IO}(+CM)	5/
X3	20		x	V_{IO}(+CM)	3,4,5/		x	I_{IB}	2,5/
X4	21		x	V_{IO}(+CM)	3,4,5/		x	V_{IO}(+CM)	5/
X6	22	x		$-I_{IB}$(-CM)	1/		x	V_{IO}(+CM)	5/
X7	23	x		AV	6/	x			
X8	24		x	V_{IO}(+CM)	3,5/		x	V_{IO}(+CM)	5/
X9	25		x	V_{IO}(+CM)	3,4,5/		x	V_{IO}(+CM)	5/
X10	26		x	V_{IO}(+CM)	3,5,6/		x	$+I_{IB}$(-CM)	5/
X11	27		x	V_{IO}(+CM)	3,4,5,6		x	V_{IO}(+CM)	5/
X13	28		x	V_{IO}(+CM)	3,5,6		x	V_{IO}(+CM)	5/
U1	29		x	V_{IO}(+CM)	4,5,6		x	$-I_{IB}$(+CM)	3,5/
U2	30	x					x	I_{IO}	3,5/
U3	31	x					x	I_{IO}	5/
U4	32	x					x	I_{IO}	5/
U5	33		x	$-I_{IB}$(+CM)	2,4/		x	I_{IO}	4/
U6	34	x				x			
U7	35	x				x		V_{OL}	4/
U8	36	x				x			
U9	37	x					x	$+I_{IB}$(+CM)	3/
U10	38	x				x			
U11	39	x					x	$-I_{IB}$(+CM)	2,4/
J1	40	x				x			
J2	41	x				x		V_{OL}	4/

TABLE A2-2 (Cont'd)

Mfr. Code	S/N	GEOS Results of S-3260 Testing				AMD Test Results			
		Good	Bad	Parameter	Notes	Good	Bad	Parameter	Notes
J3	42	x					x	$-I_{IB}(-CM)$	3/
J4	43	x					x	I_{IB}	5,2/
J5	44		x	I_{CEX}	4/		x	I_{CEX}	
J6	45	x		V_{OL}	1/		x	I_{IB}	2/
J7	46	x				x			
J8	47	x		$I_{IO}(-CM)$	1/		x	$-I_{IB}(-CM)$	3/
J9	48	x				x			
J10	49	x				x			
S1	50	x				x			
S9	51	x		$I_{IB}(+)$, $I_{IB}(-)$	1/	x			
J26	52	x				x			
S33	53		x	I_{IO}, I_{IB}	3,4,5/	x			
S34	54	x				x			
S35	55		x	$I_{IB}(+)$ (+CM)	2,4/	x			
S44	56	x				x			
S45	57	x				x			
S49	58	x				x			
S65	59	x				x			
S71	60	x				x			
S77	61	x				x			
S84	62	x					x	V_{IO}, I_{IB}	5/
S102	63	x				x			
S115	64	x				x			
G7	65	x				x			
G8	66	x				x			
G9	67	x				x			
G10	68	x					x	$-I_{IB}$ (+CM)	2/
G11	69	x					x	V_{SAT} @ 125°C	7/
G12	70	x		t_{RLH}	1/		x	V_{SAT}	
G13	71	x		t_{RLH}	1/		x	V_{SAT}	
G14	72	x					x	V_{SAT}	
G15	73	x					x	V_{SAT}	
G16	74	x					x	V_{SAT}	
G17	75	x					x	V_{SAT}	
G18	76	x					x	V_{SAT}	7/
G19	77	x				x			
G20	78	x					x	V_{SAT}	7/
G21	79	x					x	V_{SAT}	
G22	80	x					x	V_{SAT}	
G23	81	x					x	V_{SAT}	7/
G24	82		x	$+I_{IB}$ (+CM)	2,4/		x	$+I_{IB}$ (+CM)	
R1	83		x	$-I_{IB}(-CM)$	3/	x			

TABLE A2-2 (Cont'd)

Mfr. Code	S/N	GEOS Results of S-3260 Testing				AMD Test Results			
		Good	Bad	Parameter	Notes	Good	Bad	Parameter	Notes
R2	84		x	$+I_{IB}$(-CM)	3/	x			
R3	85		x	$+I_{CEX}$	4/	x			
R5	86	x				x			
R6	87	x				x			
R7	88	x					x	$-I_{IB}$(-CM)	3,4,5/
R8	89	x				x			
R10	90	x				x			
R11	91	x				x			
R12	92	x				x			
R13	93	x					x	$-I_{IB}$	3/
R14	94	x				x			
R15	95	x				x			
R16	96	x				x			
R17	97	x				x			
R18	98	x				x			
R19	99	x				x			
R20	100	x				x			

1/ Parameter is slightly out of spec.
2/ Wrong polarity bias current
3/ Low limit failure
4/ High limit failure
5/ Multiple parameter failures
6/ Wrong polarity gain
7/ There is a difference in V_{OL} test criteria between the GEOS and AMD tests as shown below

V_{cc} = 4.5 V (GEOS) V_{cc} = 5 V (AMD)		GEOS		AMD	
		Lo Limit	Hi limit	Lo limit	Hi limit
V_{OL} @ 4 mA	@ 25°C	-	.4	-	-
V_{OL} @ 4 mA	-55°C < T_A <125°C	-	.7	-	-
V_{OL} @ 6 mA	-55°C < T_A <125°C	-	1.0	-	-
V_{OL} @ R_L=1K	-55°C < T_A <125°C	-	-	-0.2 -0.2	.5

SECTION III

QUAD OPERATIONAL AMPLIFIER MIL-M-38510/110

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SECTION III

QUAD OPERATIONAL AMPLIFIER MIL-M-38510/110

3.1 Background and Introduction

An earlier technical report, RADC-TR-78-22, described the characterization effort and results on quad operational amplifiers. MIL-M-38510/110 is the military specification on the following devices:

Device type	Commerical type
01	LM148
02	LM149
03	4741, 4156
04	4136
05	LM124

At the time this earlier report was written, complete characterization data on device type 05 was not available. The purpose of this section is to update the information in the earlier report, with the main emphasis on device type 05.

3.2 Description of Device Types

3.2.1 General Characterisitics

All quad op amps possess certain common characteristics. The individual amplifiers are similar to single operational amplifiers, except that, because of pin out restrictions, external compensation and offset voltage adjustment are not available options. All have a differential input stage in order to provide high gain for differential signals and much lower gain for common-mode signals. These two inputs are called inverting (-) and non-inverting (+) for their polarity with respect to the output signal. Different techniques are used in the design of these front ends, depending on the electrical parameters to be enhanced. Low input offset voltage, low bias currents, high gain, high input impednance and high common mode rejection are the main desired input characteristics. A level-shifting stage which provides further gain couples the signal to the output. Internal frequency compensation is generally applied to the in-between, level-shifting stage. The output stage almost always is in the form of a complementary emitter follower to provide a single-ended, low-impedance, output signal.

Current limiting is generally incorporated in the output stage so that shorts to ground do not damage the op amp. Protection for shorts to either supply voltage also exists but can not be guaranteed over the full temperature range because the 175°C maximum junction temperature will be exceeded.

Since, from an application point of view, op amps are generally connected with external negative feedback to establish a precision gain, frequency compensation must be applied for stability reasons. Each gain stage of an op amp has an associated break frequency at which the gain rolls off from its DC value. An accompanying phase shift of 45° occurs at the break frequency. This increases to 90° at ten times the break frequency. If the sum of the stage phase shifts equals 180° before the loop gain magnitude has been rolled-off to unity or 0 db, the amplifier will oscillate. An internal frequency compensation capacitor connected across a gain stage provides a Miller effect capacitance to roll the gain off at 20 db/decade. In this way the gain is reduced before the stage phase shifts can render the system unstable.

3.2.2 Unique Device Characteristics

The following devices were chosen early in the characterization effort to be candidate types for the /110 specification. These selections were based on JC-41 recommendations, user anticipated need and enough difference in a major parameter to warrant another device type category.

3.2.2.1 Device type 01 (LM148)

This device is a general purpose op amp with characteristics similar to the /101-01 (741). NPN transistors are used in the input stage. This yields positive polarity input bias current. Its offset voltage specification is worse than its single counterpart (i.e., +6 mV versus ±4 mV over the military temperature range, $-55°C \leq T_A \leq 125°C$). The only parameter where this quad op amp is better than its single counterpart is in supply current (i.e., 4.5 mA for 4 op amps versus 4.2 mA for one op amp at -55°C). A few picofarads of internal compensation capacitance gives the device a specified transient response rise time of one microsecond (maximum). A schematic of one op amp in the device is shown in figure 3-1.

3.2.2.2 Device type 02 (LM149)

The characteristics of this device are identical with type 01 except for frequency compensation. Instead of conventional unity gain compensation, this op amp is compensated for a minimum closed-loop gain of 5. Thus the bandwidth is extended by a factor of five at the expense of unity gain stability.

3.2.2.3 Device type 03 (4156/4741)

Figure 3-2 shows device type 03. It has a PNP differential input and, consequently, negative polarity bias current. At the expense of power supply current, type 03 has a faster transient response and lower noise specs than type 01.

3.2.2.4 Device type 04 (4136)

Device type 04 is very similar to the type 03 except for its non-standard pin out. In general its specifications are more liberal than for the type 03. It is one of the oldest quad op amps and, consequently, has many vendors. By specifying this device in /110, existing user applications are better protected than they would be otherwise. This device is not recommended for new design. The schematic is shown in figure 3-3.

3.2.2.5 Device type 05 (LM124)

All the previously mentioned op amps require dual power supplies. Device type 05, on the other hand, is meant to operate from a single supply. Its main advantage is in low power and single power applications. The input stage is designed with PNP transistors thus permitting the common mode range to include ground. The output stage has a 50 uA pull-down current source so that it can swing to ground for light loads. Dual supply operation is possible; however, since the output is a class B configuration crossover distortion will be present.

Where TTL interfacing is needed this device can be used with a pull-down resistor. Unlike a TTL output, the output of this device is much stronger on sourcing than sinking current. Device type 05 is shown in figure 3-4.

3.3 Test Procedures

Unlike the other operational amplifiers - 01 through - 04 in the MIL-M-38510/110 specification, device type 05 was designed for single power supply operation. It also has important applications in driving digital loads. For these reasons several parameters in the specification are unique to device type 05. Figure 3-5 shows the test circuit for quad op amp static tests. Table 3-1 shows how the test circuit is programmed for most tests. In order to perform the V_{OL} output voltage tests with a current source it was necessary to add relay K11. The only other change specifically added for device type 05 testing is the 10 KΩ load and relay K9. Except for these changes, the test procedure is the same as described in the previous quad operational amplifier report.

The S-3260 quad op amp test fixture was modified accordingly. The major change made to the S-3260 test program was to compare the measured data to the specification limits and then print an asterisk for each "out of spec" parameter. Without this feature it is very time consuming to locate paramter failures. Thirty-two (32) devices or 128 op amps were tested on GEOS's Tektronix S-3263 test system.

Transient response testing was done on a few samples on a bench test basis. Figure 3-6 illustrates the procedure for transient response testing.

3.4 Tabulation of Data and Characteristics

32 devices from 4 vendors were tested. A typical data sheet is shown in Table 3-2. The time required to take these measurements over temperature and print out the results was under four minutes per device. The data was also logged into a file so that a statistical analysis could be done on all the devices in the group. Tables 3-3, 3-4 and 3-5 are statistical summary sheets which were generated to show how well the data fits the specified limits. Most of the column headings are self explanatory. Low and high figures of merit were calculated to determine how many standard deviations (σ, sigma) exist between the data mean and the low and high parameter limits.

Since in a normal distribution 99.7% of the data is within $\pm 3\sigma$, each figure of merit is a good indicator of how loose or tight the data is with respect to the specified limits. It was arbitrarily decided that if the figures of merit were greater than 5 or less than 1 some corrective action to the test conditions or limits should be considered. Observations showed that a few "way-out" failed data values tend to degrade sigma and consequently the figure of merit also. High and low reject limits were added to exclude "grossly out-of-spec" data from the statistical calculations.

Although the statistical summaries are a good economical way to show the data to limit relationships, they are not as comprehensive as individual histograms for each parameter - temperature combination. Consequently, histograms were generated to help assess where the parameter limits should be established. A typical histogram is shown in figure 3-7. Proposed limits were added later on to each of the S-3260 histograms.

Table 3-6 compares the worst case $\bar{X} \pm 3\sigma$ limits against the specification limits.

3.5 Discussion

The purpose of this discussion is to describe the characterization study results with regard to the device electrical parameters. Emphasis is on device type 05 since the other types were discussed in technical report RADC-TR-78-22. In general, the data values and the final adjusted specification limits are in good agreement. Additional comments on a parameter by parameter basis follow:

3.5.1 V_{iO}, Input Offset Voltage

It was originally intended that this parameter be tested and specified under four conditions, such that for + V_{cc} = 5 and 30 V, the input common mode range be from - V_{cc} at OV to 2V below + V_{cc}. Test results showed that with V_{cc} = 5 V and V_{cm} = + .5 V, the limits would have to be doubled for acceptable yields.

By reducing the upper common mode range limit from + .5V to OV at V_{cc} = 5V, consistant limits could be maintained.

3.5.2 $\Delta V_{iO}/\Delta T$, Offset Voltage Temperature Sensitivity

With most of the data values within ± 20 μV/°C, limits of ± 30 μV/°C are safe and reasonable.

3.5.3 I_{iO}, Input Offset Current

The lowest yield condition for I_{iO} occurs at -55°C with high supply voltage and high common mode input. The comments of 3.5.1 also apply here.

3.5.4 $\Delta I_{iO}/\Delta T$, Offset Current Temperature Sensitivity

As with $\Delta V_{iO}/\Delta T$, this parameter is specified at low supply voltage and low common mode voltage. The -55°C yield of this parameter is 96.1% with the recommended limits of ± 700 pA/°C. $\Delta I_{iO}/\Delta T$ failures commonly occurred with I_{iO} and I_{iB} failures.

3.5.5 $+I_{iB}$, $-I_{iB}$, Input Bias Current

Wrong polarity bias current caused occasional failures at the high common mode input condition. Breakdown of the PNP base collector input junction is suspected for those failures. Overall yield on bias current tests, were much better for device type 05 than type 01. The deleted low supply, high common mode condition mentioned in 3.5.1 had the most wrong polarity bias current failures for device type 05.

3.5.6 PSRR(+), Power Supply Rejection Ratio

Data values for PSRR were comfortably inside the ± 100 μ V/V specification limits.

3.5.7 CMR, Common Mode Rejection

This parameter is calculated from the V_{iO} change over the input common mode range. Consequently, there is a close relationship between V_{iO} and CMR failures. The worst condition at -55°C had a CMR yield of 94% against a 76 dB (min) limit.

3.5.8 $+I_{os}$, Output Short Circuit Current (for + output)

With a minimum limit of -70 mA, there were no failures on this parameter. Typically, the output short circuit current for sourcing is between 30 and 50 mA and the magnitude decreases with increasing temperature.

3.5.9 I_{cc}, Power Supply Current

Supply current was tested at V_{cc} = 5V and 30V during the S-3260 characterization tests. Since the low voltage I_{cc} is approximately 70% of the value at 30 V, only one test was deemed necessary for the specification.

Typical values of I_{cc} are 50 to 100% less than the recommended limits. No benefit is seen in tightening the limit because the one to 2 mA of margin would not help power supply loading estimates that much.

3.5.10 $+V_{OP}$, Output Voltage Swing

Maximum output voltage swing is generally well behaved with a tight histogram pattern. All observed failures were associated with multiple failures in other parameters. This is not too surprising since good V_{OP} performance is mainly a function of the output Darlington transistor stage.

3.5.11 A_{VS}, Open Loop Voltage Gain

Of all the parameter tested, A_{VS} data forms the worst histogram in terms of "bell shape" criteria. The effect of thermal feedback in conjunction with output loading and high open loop gain gives rise to a non linear input-output relationship. Wrong polarity gains were not uncommon. No devices failed A_{VS} without failing other front end tests as well. Although GEOS is in favor of deleting the 2KΩ load requirement, the vendors state that this condition is needed to verify output swing linearity.

3.5.12 V_{OL}, Low Level Output Voltage

Low level output voltage is a parameter one normally associates with digital circuits and not op amps. Since device type 05 is commonly interfaced to digital circuits, it is important to specify its drive capability for such applications. Three conditions of V_{OL} are specified. For TTL applications it is important to specify the drive current for V_{cc} (min) = 4.5 V and V_{OL} (max) = 0.4 V. Over the temperature range, the data indicates a maximum test current of only 2 uA can be specified and still have good yields. For higher current sinking applications with V_{cc} = 30 V, a 5 mA test current results in a typical V_{OL} of 1V. A 1.5 V (max) limit was specified. The third V_{OL} specification with a 10 KΩ load guarantees that the output current source is working. Data for this test shows that a 35 mV (max) limit is reasonable.

3.5.13 V_{OH}, High Level Output Voltage

The companion specification to V_{OL} is V_{OH}, which defines the high level output voltage. Device type 05, unlike a TTL output, is much stronger in a current sourcing mode, than a current sinking mode. Thus at 10 mA of source current with supply voltages of 30 V and 4.5 V, minimum V_{OH} levels of 27 V and 2.4 V respectively can be specified.

3.5.14 TR (tr), TR (os), Transient Response (risetime), (overshoot)

Transient response measurements were not made automatically on the S-3260 test system as were the previous parameters. Oscilloscope observations of several sample devices showed that transient response rise time and overshoot depend quite significantly on input common mode conditions. Thus in a standard single supply application, device type 05 is not as responsive to ground referenced signals as it is to pulse inputs riding on a D.C. bias. Waveforms to illustrate this are shown in figure 3-8. Transistor saturation effects cause the response to be slower with less overshoot.

After some consultation with device manufacturers, it was decided that since, in the usual case, op amp transient response is specified with the device in the linear mode, the same conditions should apply to a single supply op amp. Using this rationale, the /110 slash sheet is being proposed with the 50 mV pulse referenced to + 5 V.

3.5.15 SR (+) and SR (-), Slew Rate

Typical data indicates that the - 05 can slew at a rate of 0.5 V/μs. A minimum limit of 0.1 V/μs is considered reasonable for temperature and yield variations.

3.5.16 N1 (BB), N1 (PC), Broadband and Popcorn Noise

Broadband and popcorn noise was observed with a curve tracer on a small sample of devices. The observed maximums of 10 μVrms and 5 μVpk are conservatively inside the recommended limits.

3.5.17 CS, Channel Separation

Curve tracer observations on a few devices indicates that there is better than a 20 dB margin between the minimum limit of 80 dB and worst observed data. Channel separation is measured on a D.C. basis by the effect of a driven op amp on the offset voltage of the other monitored op amps. This D.C. method is easier to mechanize in an automatic tester than an equivalent A.C. method.

3.6 Conclusions and Recommendations

Thirty-two (32) device data sheets, three statistical summary sheets and 133 parameter/condition histograms were generated in order to determine typical device performance.

The results of the quad operational amplifier characterization effort show that the data, in general, supports the recommended limits proposed by JEDEC JC-41.

One area where the /110-05 specification differs from the original JC-41 recommendations is with regard to output current sourcing and sinking. The JC-41 specification measures the output sink and source currents with test conditions of + V_{CC} = 30 V and V_O = 15 V. The /110-05 specification forces test source and sink currents and then measures the output voltage to determine if V_{OH} (min) and V_{OL} (max) are in tolerance. How close the device output can get to the supply rails is not determined in the JC-41 test.

The quad op amp specification contain parameter limits and test conditions which best compromise user needs and vendor yields.

Table 3-7 shows the electrical specifications as incorporated in MIL-M-38510/110, dated 25 May 1978.

The bulk characterization data was issued in a bound report to representatives of the linear IC manufacturers on 6 July 1978. Copies of this data are available at RADC and GEOS.

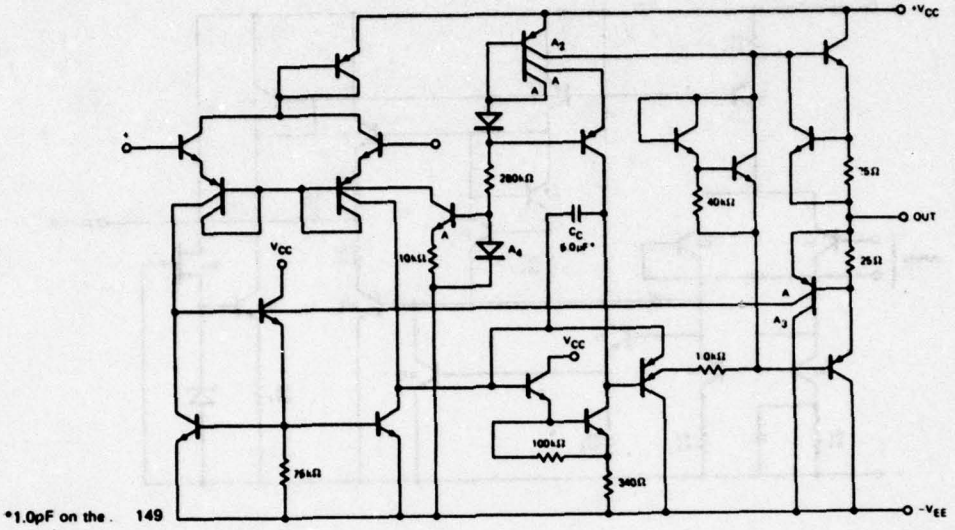


Figure 3-1. Device type 01 and 02 (LM148, LM149)

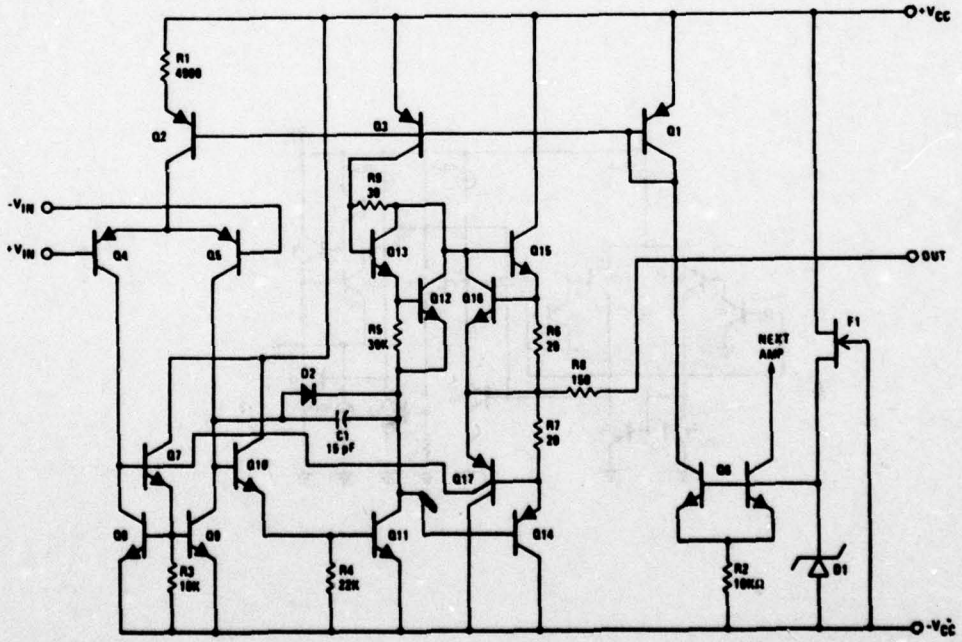


Figure 3-2. Device type 03 (4156/4741)

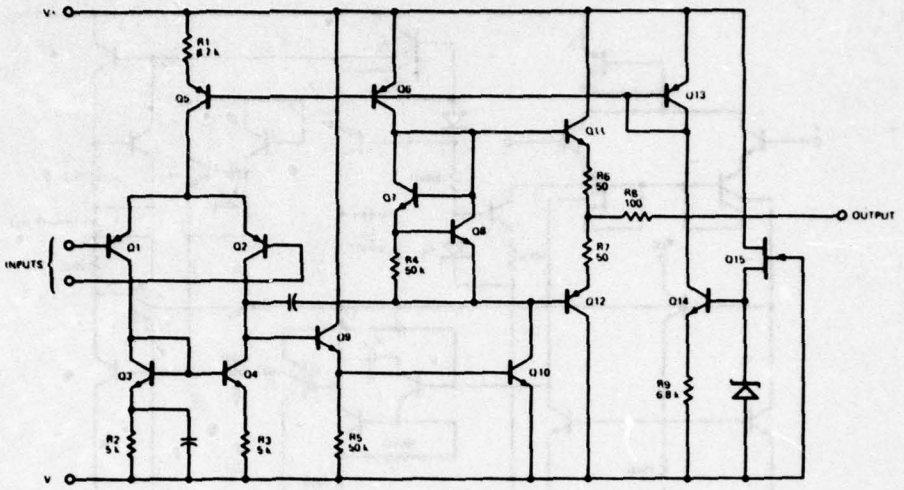


Figure 3-3. Device type 04 (4136)

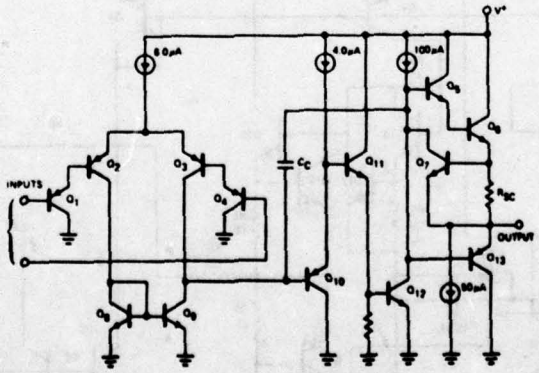


Figure 3-4. Device type 05 (LM 124)

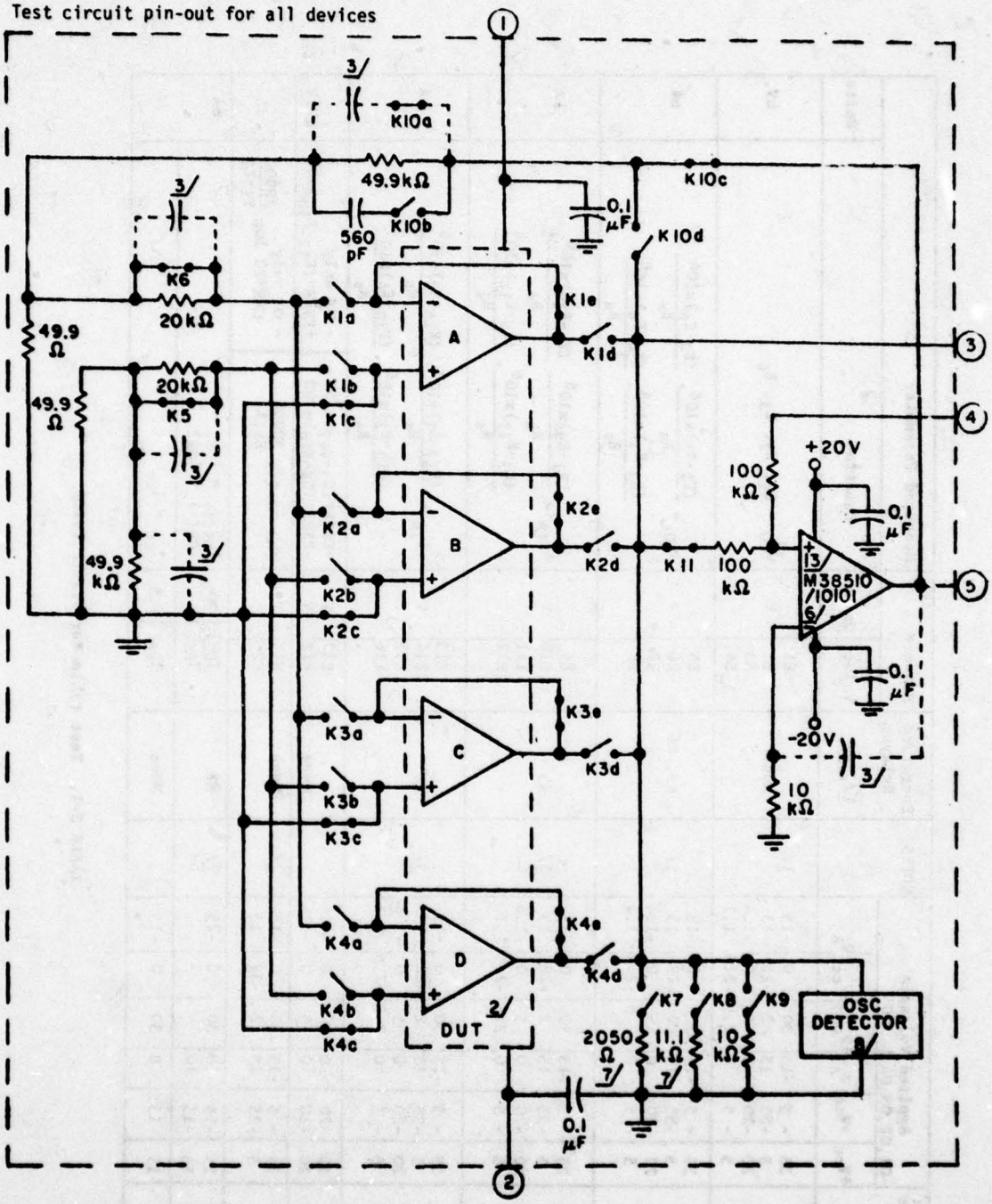


Figure 3-5. Test circuit for static tests.

Parameter Symbol	Applied Voltages -01,02,03,04			-05			NOTES	Energized Relays	Measure		Measured Parameter		
	$+V_{cc}$	$-V_{cc}$	V_A	$+V_{cc}$	$-V_{cc}$	V_A		1/, 6/	Value	Units	Equation		Units
V_{10}	35 5 20 5	- 5 -35 -20 - 5	-15 15 0 0	30 2 5 2.5	0 -28 0 -2.5	-15 13 -1.4 1.1	1/	None	E1 E2 E3 E4	V	$V_{10} = E_1, E_2, E_3, E_4$		mV
I_{10}	35 5 20 5	- 5 -35 -20 - 5	-15 15 0 0	30 2 5 2.5	0 -28 0 -2.5	-15 13 -1.4 1.1	5/	K5, K6	E5 E6 E7 E8	V	$I_{10} = \frac{(E1-E_5)\times10^6}{R_s}, \frac{(E_2-E_6)\times10^6}{R_s}, \frac{(E_3-E_7)\times10^6}{R_s}, \frac{(E_4-E_8)\times10^6}{R_s}$		nA
$+I_{IB}$	35 5 20 5	- 5 -35 -20 - 5	-15 15 0 0	30 2 5 2.5	0 -28 0 -2.5	-15 13 -1.4 1.1	3/	K5	E9 E10 E11 E12	V	$+I_{IB} = \frac{(E_1-E_9)\times10^6}{R_s}, \frac{(E_2-E_{10})\times10^6}{R_s}, \frac{(E_3-E_{11})\times10^6}{R_s}, \frac{(E_4-E_{12})\times10^6}{R_s}$		nA
$-I_{IB}$	35 5 20 5	- 5 -35 -20 - 5	-15 15 0 0	30 2 5 2.5	0 -28 0 -2.5	-15 13 -1.4 1.1	3/	K6	E13 E14 E15 E16	V	$-I_{IB} = \frac{(E_{13}-E_1)\times10^6}{R_s}, \frac{(E_{14}-E_2)\times10^6}{R_s}, \frac{(E_{15}-E_3)\times10^6}{R_s}, \frac{(E_{16}-E_4)\times10^6}{R_s}$		nA
+PSRR -PSRR	10 20	-20 -10	0 0	30 5	0 0	-1.4 -1.4		None	E17 E18	V V	+PSRR=$(E_3-E_{17})\times100$ -PSRR=$(E_3-E_{18})\times100$	- 05 only +PSRR=$(E_{17}-E_{18})\times40$	mV/V
CMR	35 5	- 5 -35	-15 15	30 2	0 -28	-15 13	2/	None	E1 E2	V	CMR=20 log $\frac{30000}{E_1-E_2}$	- 05 only CMR=20 log $\frac{28000}{E_1-E_2}$	dB
$I_{OS(+)}$ $I_{OS(-)}$	15 15	-15 -15	-10 10	30 -	0 -	-25 -	7/	K9	I_{OS1} I_{OS2}	mA	$I_{OS(+)} = I_{OS1}$ $I_{OS(-)} = I_{OS2}$		mA
I_{cc}	15	-15	0	30	0	-15		None	I_{cc}	mA	$I_{cc} = I_{cc}$		

TABLE 3-1. Test table for static tests.

Parameter Symbol	Applied Voltages -01,02,03,04			-05			NOTES	Energized Relays	Measure		Measured Parameter			
	$+V_{cc}$	$-V_{cc}$	V_A	$+V_{cc}$	$-V_{cc}$	V_A		1/, 6/	Value	Units	Equation			Units
+ V_{OP}	20	-20	-20	30	0	-30	R_L=	K8	$(E_o)_1$	V	+ V_{OP} = $(E_o)_1$			V
- V_{OP}	20	-20	20	-	-	-	10KΩ		$(E_o)_2$		- V_{OP} = $(E_o)_2$			
+ V_{OP}	-	-	-	5	0	- 5			$(E_o)_3$		+ V_{OP} = $(E_o)_3$			
+ V_{OP}	20	-20	-20	30	0	-30	R_L=	K7	$(E_o)_4$	V	+ V_{OP} = $(E_o)_4$			V
- V_{OP}	20	-20	20	-	-	-	2KΩ		$(E_o)_5$		- V_{OP} = $(E_o)_5$			
+ V_{OP}	-	-	-	5	0	- 5			$(E_o)_6$		+ V_{OP} = $(E_o)_6$			
A_{VS} (+)	20	-20	-15	-	-	-	R_L=	K8	E19	V	+ $A_{VS} = \frac{15}{E_3-E_{19}}$, - $A_{VS} = \frac{15}{E_{20}-E_3}$			V/mV
A_{VS} (-)	20	-20	-15	-	-	-	10KΩ		E20		9/			
A_{VS} (+)	20	-20	-15	-	-	-	R_L=	K7	E21	V	+ $A_{VS} = \frac{15}{E_3-E_{21}}$, - $A_{VS} = \frac{15}{E_{22}-E_3}$			V/mV
A_{VS} (-)	20	-20	-15	-	-	-	2KΩ		E22					
A_{VS} (+)	-	-	-	30	0	-26	R_L=	K8	E23	V	$A_{VS} = \frac{25}{E_{24}-E_{23}}$			V/mV
	-	-	-	30	0	- 1	10KΩ		E24					
A_{VS} (-)	-	-	-	30	0	-16	R_L=	K7	E25	V	$A_{VS} = \frac{15}{E_{26}-E_{25}}$			V/mV
	-	-	-	30	0	- 1	2KΩ		E26					
A_{VS}	5	- 5	- 2	5	0	- 3	R_L=	K8	E27	V	$A_{VS} = \frac{V_A}{E_{28}-E_{27}}$	01 - 04	ΔV_A = 4	V/mV
	5	- 5	2	5	0	- 1	10KΩ		E28			05	ΔV_A = 2	
A_{VS}	5	- 5	- 2	5	0	- 3	R_L=	K7	E29	V	$A_{VS} = \frac{V_A}{E_{30}-E_{29}}$	01 - 04	ΔV_A = 4	V/mV
	5	- 5	2	5	0	- 1	2KΩ		E30			05	ΔV_A = 2	
N_1 (BB)	20	-20	0	30	0	0		K10	$(E_o)_7$	mVrms	N_1 (BB) = $(E_o)_7$/1000			μVrms
N_1 (PC)	20	-20	0	30	0	0	12/	K5,K6,K10	$(E_o)_8$	mVpk	N_1 (PC) = $(E_o)_8$/1000			μVpk
V_{OL}	-	-	-	30	0	30	R_L=10K	K11,K9	$(E_o)_9$	mV	V_{OL} = $(E_o)_9$			mV
V_{OH}	-	-	-	30	0	-30	I_{OH}=10mA	K11	$(E_o)_{10}$	V	V_{OH} = $(E_o)_{10}$			V
V_{OL}	-	-	-	30	0	30	I_{OL}= 5mA		$(E_o)_{11}$		V_{OL} = $(E_o)_{11}$			
V_{OH}	-	-	-	4.5	0	- 5	I_{OH}=10mA		$(E_o)_{12}$		V_{OH} = $(E_o)_{12}$			
V_{OL}	-	-	-	4.5	0	5	I_{OL}=2mA		$(E_o)_{13}$		V_{OL} = $(E_o)_{13}$			

TABLE 3-1. Test table for static tests. (cont'd.)

TABLE 3-1 NOTES

1/ Selection of the op amp under test is made with relay contacts K1, K2, K3 and K4. Use the parameter table to determine which others need to be energized for a particular test.

2/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

3/ Stabilizing capacitors may be added as required if needed to prevent oscillation. Also, proper wiring procedures shall be followed to prevent oscillation. Loop response and setting time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.

4/ Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of switch positions (e.g. disable voltage supplies, current limits).

5/ Rs = 20 KΩ for -01, 02, 03, 04 and 05.

6/ All relays are shown in the normal de-energized state.

7/ Only one op amp at a time shall be tested with a short to ground for $t \leq 25$ ms.

8/ Any oscillation greater than 300 mV in amplitude (pk - pk) shall be cause for device failure.

9/ To minimize thermal drift, the reference voltage for gain measurement E3 shall be taken immediately prior to or after the reading corre sponding to device gain (E_{21}, E_{22}, E_{23} and E_{24}).

10/ All resistors are ±0.1% tolerance, capacitors are ± 10% tolerance.

11/ Adequate settling time shall be allowed such that each parameter has settled to 5% of its final value.

12/ Popcorn noise (E_0)8 shall be measured for 15 seconds. Breadboard noise (E_0)7 shall be measured with an RMS voltmeter with a bandwidth of 10 Hz to 5 kHz.

13/ Saturation of the nulling amplifier is not allowed on tests where E value is measured.

14/ The load resistors (2040 Ω and 11.1 K Ω) yield effective load resistances of 2 K Ω and 10 K Ω respectively.

15/ The equations take into account both the loop gain of 1000 and the scale factor multiplexer, so that the calculated value is in Table III units. Therefore, use measured value/units in the equations is i.e. E1 (volts).

16/ The programmable current source is used to exercise the drive capability of device type 05 for sourcing I_{OH} and sinking I_{OL}.

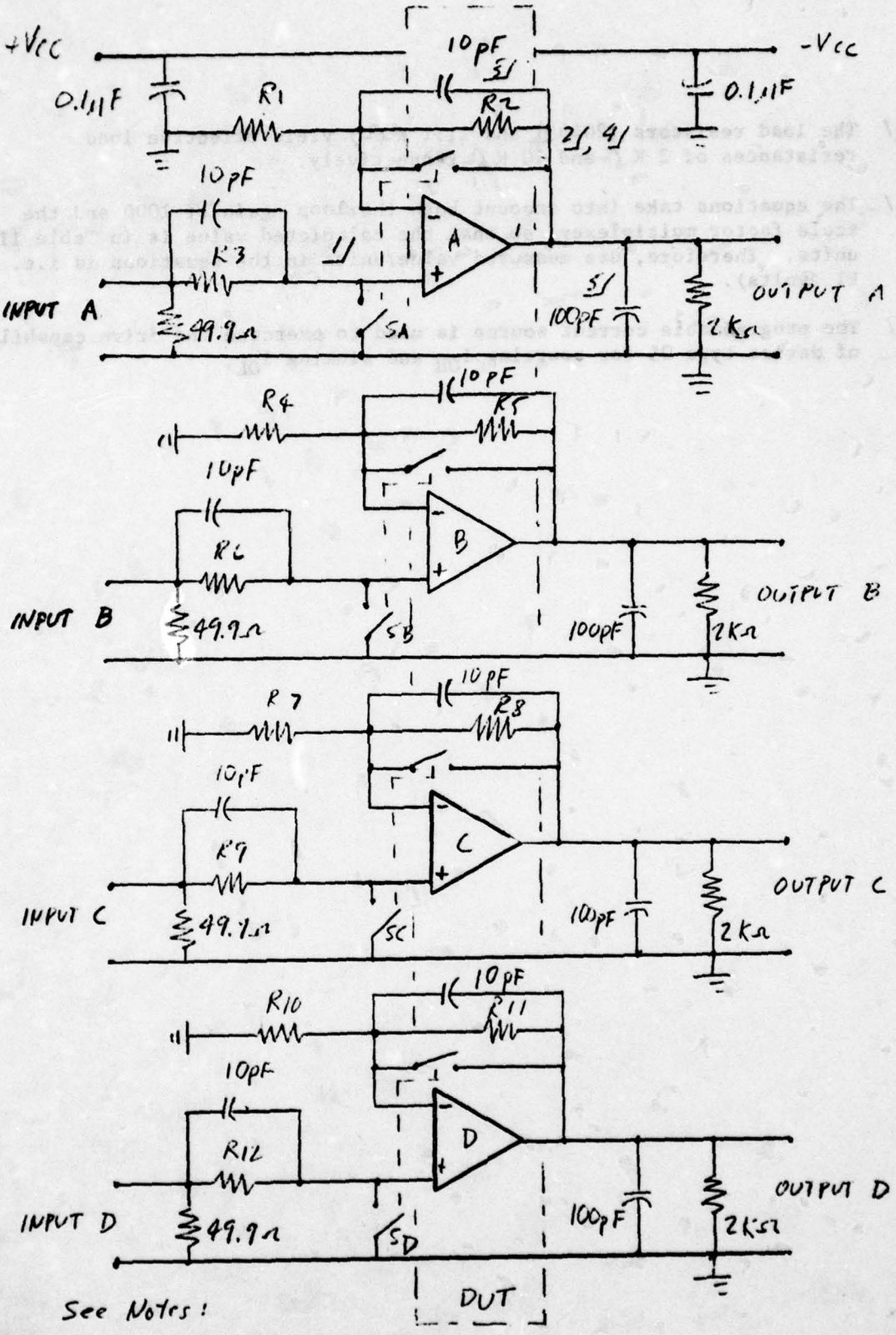


Figure 3-6. Transient response test circuit.

Transient response test conditions

Device Type	$+V_{cc}$ (V)	$-V_{cc}$ (V)	AV (V/V)	R1 (KΩ)	R2 (KΩ)	R3 (KΩ)	Pulse Generator Input	
							Rise Time Test	Slew Rate Test
-01,03,04	+20	-20	1	Open	10	10	+ 50 mV	-5V to +5V
-02	+20	-20	5	1	4.02	1	+ 50 mV	-1V to +1V
-05	+30	0	1	Open	10	10	+ 50 mV	+5V to +15V

Transient response parameters and equations

Parameter Symbol	Pulse Generator	Measure	Equation	Units
TR (tr)	+50 mV amplitude	Δt Waveform 1	TR (tr) = Δt	us
TR (os)	+50 mV amplitude	ΔV Waveform 1	TR (os) = $\frac{\Delta V}{Vo} \times 100$	%
SR (+) @ AV = 1	-5V to + 5V Step	ΔVo (+), Δt (+) Waveform 2	SR (+) = $\frac{\Delta Vo(+)}{\Delta t(+)}$	V/us
SR (-) @ AV = 1	+5V to + 5V Step	Δ Vo (-), Δt (-) Waveform 3	SR (-) = $\frac{\Delta Vo(-)}{\Delta t(-)}$	V/us
SR (+) @ AV = 5	-1V to + 1V Step	ΔVo (+), Δt (+) Waveform 2	SR (+) = $\frac{\Delta Vo(+)}{\Delta t(+)}$	V/us
SR (-) @ AV = 5	+1V to - 1V Step	ΔVo (-), Δt (-) Waveform 3	SR (-) = $\frac{\Delta Vo(-)}{\Delta t(-)}$	V/us
SR (+) @ AV = 1	+5V to + 15V Step	ΔVo (+), Δt (+) Waveform 2	SR (+) = $\frac{\Delta Vo(+)}{\Delta t(+)}$	V/us
SR (-) @ AV = 1	+15V to + 5V Step	ΔVo (-), Δt (-) Waveform 3	SR (-) = $\frac{\Delta Vo(-)}{\Delta t(-)}$	V/us

Figure 3-6. Transient response test circuit (cont'd).

DEVICE TYPE: 124 ; S/N: 177 ; DATE CODE: 0 ; 28 SEP 77 16:56:54

PARAMETER	25 DEG C				-55 DEG C				125 DEG C				UNITS
	OPAMP1	OPAMP2	OPAMP3	OPAMP4	OPAMP1	OPAMP2	OPAMP3	OPAMP4	OPAMP1	OPAMP2	OPAMP3	OPAMP4	
VIO AT 30, 0, -15	1.28	1.14	1.57	97.0M	995.M	1.13	1.44	-74.0M	1.63	1.28	1.85	82.0M	MV
D-VIO/D-T FROM 25 OC					3.56	62.5M	1.69	2.14	3.45	1.40	3.10	-150.M	UV/OC
VIO AT 2.0,-28.0,15	-80.5M	-401.M	64.5M	-1.49	-147.M	-168.M	163.M	-1.18	-79.0M	-641.M	44.7M	-1.85	MV
D-VIO/D-T FROM 25 OC					700.M	-2.91	-1.23	-3.88	115.M	-2.40	-199.M	-3.60	UV/OC
VIO AT 5, 0, -1.4	1.22	1.24	1.49	77.5M	980.M	1.23	1.38	-58.6M	1.43	1.37	1.78	77.0M	MV
D-VIO/D-T FROM 25 OC					3.01	187.M	1.44	1.70	2.70	1.25	2.85	-5.00M	UV/OC
VIO AT 2,-3, 1.6	-2.89	-2.90	-2.55	-3.95	-4.22	-3.95	-3.73	-6.95	-945.M	-1.09	-553.M	-2.20	MV
D-VIO/D-T FROM 25 OC					16.6	13.2	14.7	37.4 *	19.4	18.1	20.0	17.5	UV/OC
IIO AT 30, 0, -15	-1.00	-2.25	-5.25	6.54	-250.M	-2.25	-5.25	651. *	-500.M	-2.50	-4.50	-125.M	NA
D-IIO/D-T FROM 25 OC					-9.37	0.00	0.00	-8.06K*	5.00	-2.50	7.50	-66.7	PA/OC
IIO AT 2.0,-28.0,15	1.20	-125.M	-2.05	-21.0	1.22	-575.M	-2.65	-772. *	1.68	-50.0M	-1.19	2.00	NA
D-IIO/D-T FROM 25 OC					-312.M	5.63	7.50	9.38K*	4.00	750.M	8.55	230.	PA/OC
IIO AT 5, 0, -1.4	0.00	-1.25	-3.25	1.21	150.M	-1.00	-3.25	282. *	0.00	-1.25	-2.50	-275.M	NA
D-IIO/D-T FROM 25 OC					-1.88	-3.12	0.00	-3.51K*	0.00	0.00	7.50	-14.9	PA/OC
IIO AT 2,-3, 1.6	37.5 *	40.0 *	36.3 *	34.2 *	66.0	69.5	66.5	64.0	-11.3	-8.75	-13.5	-14.5	NA
D-IIO/D-T FROM 25 OC					-356.	-369.	-378.	-372.	-488.	-488.	-498.	-487.	PA/OC
IIB(+)AT 30, 0, -15	-44.0	-43.5	-48.8	-47.4	-33.5	-33.7	-39.0	-31.8	-56.8	-56.3	-60.0	-60.1	NA
IIB(+)AT 2.0,-28.0,15	-25.9	-25.5	-28.9	-27.5	-20.5	-21.0	-23.9	-10.5	-31.6	-31.2	-33.4	-33.0	NA
IIB(+)AT 5, 0, -1.4	-24.5	-24.7	-28.0	-27.2	-19.0	-19.5	-21.7	-16.8	-31.3	-30.2	-32.7	-32.8	NA
IIB(+)AT 2,-3, 1.6	74.7 *	80.0 *	72.3 *	68.2 *	131. *	138. *	132. *	128. *	-24.1	-18.5	-30.1	-29.7	NA
IIB(-)AT 30, 0, -15	-43.0	-41.1	-43.5	-54.1	-32.8	-31.1	-33.0	-651. *	-56.4	-54.2	-56.3	-60.4	NA
IIB(-)AT 2.0,-28.0,15	-27.0	-25.7	-26.3	-8.75	-21.9	-19.9	-20.9	772. *	-33.2	-31.7	-32.3	-35.0	NA
IIB(-)AT 5, 0, -1.4	-24.5	-23.5	-24.2	-27.2	-19.3	-18.3	-19.0	-275.	-30.8	-29.5	-30.8	-29.5	NA
IIB(-)AT 2,-3, 1.6	-111.	-119.	-107.	-101.	-194.	-204.	-195.	-195.	36.4 *	29.3 *	47.8 *	45.7 *	NA
PSRR(+)	12.2	14.8	13.6	14.9	10.4	12.2	10.8	12.9	15.4	18.8	16.6	18.7	UV/V
CMR1 AT VCM = 0-28V	86.9	85.9	86.0	85.5	89.4	87.2	87.4	88.7	84.9	83.9	84.2	83.8	DB
CMR2 AT VCM = 0-3V	57.3 *	57.2 *	57.4 *	57.4 *	55.2 *	55.3 *	55.4 *	52.8 *	61.8 *	61.7 *	62.2 *	62.4 *	DB
ICC AT VCC = +30V	-994.M	-995.M	-997.M	-1.00	-878.M	-880.M	-880.M	-880.M	-1.04	-1.03	-1.04	-1.04	MA
ICC AT VCC = +5V	-553.M	-552.M	-556.M	-554.M	-497.M	-496.M	-498.M	-495.M	-551.M	-550.M	-551.M	-549.M	MA
IOS(+)	-35.6	-38.8	-40.7	-33.8	-40.1	-44.0	-46.2	-43.9	-27.3	-29.4	-31.1	-29.9	MA
VOPP(+) PS=30V RL=10K	28.5	28.5	28.5	28.5	28.3	28.3	28.3	28.3	28.8	28.8	28.8	28.8	V
VOPP(+) PS=30V RL=2K	28.1	28.2	28.1	28.1	28.0	28.0	28.0	28.0	27.8	27.9	27.9	27.8	V
VOPP(+) PS=5V RL=10K	3.70	3.71	3.71	3.71	3.52	3.52	3.52	3.52	4.01	4.01	4.01	4.01	V
VOPP(+) PS=5V RL=2K	3.62	3.62	3.63	3.63	3.44	3.44	3.44	3.44	3.89	3.89	3.90	3.91	V
AVS(+) RL=10K	-625. *	-625. *	2.50K	758.	-167. *	-192. *	-417. *	57.9	-152. *	-179. *	-312. *	262.	V/MV
AVS(+) RL=2K	-58.8 *	-63.8 *	-68.2 *	-61.6 *	-69.8 *	-78.9 *	-83.3 *	1.10K	-50.0 *	-55.6 *	-57.7 *	-53.4 *	V/MV
AVS AT +-5V RL=10K	133.	200.	400.	154.	-400. *	80.0	200.	58.1	66.7	200.	66.7	129.	V/MV
AVS AT +-5V RL=2K	200.	200.	400.	200.	400.	400.	400.	54.8	100.	100.	100.	80.0	V/MV
VOL--PS=30V; RL=10K	17.7	20.5 *	20.2 *	19.3	19.2	20.4 *	20.3 *	20.8 *	18.2	21.7 *	21.3 *	22.3 *	MV
VOH--PS=30V	28.3	28.3	28.3	28.3	28.1	28.1	28.1	28.1	28.3	28.4	28.4	28.4	V
IOH-PS=30V/FORCE 25V	-36.6	-40.1	-42.4	-40.2	-40.9	-45.2	-47.4	-45.1	-28.1	-30.5	-32.5	-31.1	MA
VOL--PS=30V	907.M	901.M	901.M	903.M	955.M	952.M	952.M	953.M	861.M	856.M	856.M	859.M	V
IOL-PS=30V/FORCE 3V	23.0	22.7	23.3	23.8	21.8	21.4	21.9	22.6	20.9	20.7	21.1	21.2	MA
VOH--PS=4.5V	2.81	2.83	2.83	2.83	2.64	2.65	2.65	2.65	2.81	2.89	2.89	2.82	V
IOH-PS=4.5V/FORCE 2.4	-15.7	-16.8	-16.7	-16.0	-16.8	-17.9	-18.0	-17.2	-13.1	-14.0	-14.0	-13.3	MA
VOL--PS=4.5V	68.5M	75.5M	74.0M	71.0M	273.M	489.M*	395.M	374.M	72.5M	79.0M	78.0M	77.0M	V
IOL-PS=4.5V/FORCE 0.4	14.7	14.1	14.4	14.9	9.88	10.2	9.55	9.78	21.3	21.0	21.6	22.2	UA

Table 3-2. LM 124 Data Sheet.

STATISTICAL DATA FOR MIXED LOT LM124 AT -55 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM 2/ *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 2/ *	UNITS
VIO AT 30, 0, -15	-4.94	4.16	-93.7M	1.65	120	89.8	93.8	6.25	-7.00	-10.0	4.18	0.00	7.00	10.0	4.29	MV
VIO AT 2.0,-28.0,15	-5.64	7.11	-1.51	1.72	121	89.8	93.8	2.34	-7.00	-10.0	3.20	3.91	7.00	10.0	4.95	MV
VIO AT 5, 0, -1.4	-6.26	3.87	-120.M	1.67	124	93.8	95.3	3.13	-7.00	-10.0	4.12	0.00	7.00	10.0	4.27	MV
D-VIO/D-T FROM 25 OC	-20.6	25.6	-4.83M	5.33	128	95.3	96.1	0.00	-30.0	-50.0	1.63	0.00	30.0	50.0	5.63	UV/OC
VIO AT 2.5,-2.5,-1.1	-6.08	3.52	-334.M	1.57	123	92.2	95.3	1.56	-7.00	-10.0	4.26	2.34	7.00	10.0	4.69	MV
IIO AT 30, 0, -15	-30.1	117.	3.90	22.4	125	91.4	95.3	1.56	-90.0	-120.	4.19	3.13	90.0	120.	3.84	NA
IIO AT 2.0,-28.0,15	-99.2	30.0	-2.48	16.5	119	89.1	89.1	7.03	-90.0	-120.	5.31	781.M	90.0	120.	5.61	NA
IIO AT 5, 0, -1.4	-20.4	95.0	5.32	19.7	125	92.2	93.8	0.00	-90.0	-120.	4.85	3.91	90.0	120.	4.31	NA
D-IIO/D-T FROM 25 OC	-938.	800.	-37.3	185.	125	92.2	93.0	3.91	-700.	-1.00K	3.58	1.56	700.	1.00K	3.98	PA/OC
IIO AT 2.5,-2.5,-1.1	-15.5	40.8	1.73	7.77	127	94.5	97.7	0.00	-90.0	-120.	11.8	781.M	90.0	120.	11.4	NA
IIB(+)AT 30, 0, -15	-300.	-2.50	-48.0	29.7	120	97.7	97.7	2.34	-300.	-500.	8.49	4.69	-1.00	-5.00M	1.59	NA
IIB(+)AT 2.0,-28.0,15	-354.	-7.95	-28.8	32.7	118	97.7	97.7	2.34	-300.	-500.	8.30	6.25	-1.00	-5.00M	850.M	NA
IIB(+)AT 5, 0, -1.4	-60.1	-12.8	-29.2	11.0	120	85.9	93.8	0.00	-300.	-500.	24.6	6.25	-1.00	-5.00M	2.56	NA
IIB(+) AT +-2.5,-1.1	-56.6	-6.78	-23.6	10.4	122	86.7	98.4	0.00	-300.	-500.	26.5	4.69	-1.00	-5.00M	2.17	NA
IIB(-)AT 30, 0, -15	-408.	-18.2	-52.8	40.8	119	96.1	98.4	781.M	-300.	-500.	6.06	7.03	-1.00	-5.00M	1.27	NA
IIB(-)AT 2.0,-28.0,15	-383.	-2.50	-30.4	37.1	109	92.2	93.0	781.M	-300.	-500.	7.22	14.8	-1.00	-5.00M	794.M	NA
IIB(-)AT 5, 0, -1.4	-346.	-5.63	-38.2	43.7	127	96.9	97.7	2.34	-300.	-500.	5.99	0.00	-1.00	-5.00M	853.M	NA
IIB(-) AT +-2.5,-1.1	-348.	-2.50	-27.0	30.8	125	99.2	99.2	781.M	-300.	-500.	8.87	2.34	-1.00	-5.00M	844.M	NA
PSRR(+)	-18.8	122.	16.5	19.4	126	95.3	95.3	1.56	-100.	-200.	4.01	2.34	100.	200.	4.31	UV/V
CMR1 AT VCM = 0-28V	60.8	160.	87.0	11.2	128	95.3	98.4	6.25	76.0	60.0	976.M	----	----	500.	----	dB
CMR3 AT VCM = 0-2.5V	64.8	97.1	79.6	4.27	122	89.1	92.2	5.47	70.0	60.0	2.25	----	----	500.	----	dB
ICC AT VCC = +30V	-8.81	-462.M	-1.22	1.26	124	96.9	96.9	3.13	-4.00	-10.0	2.21	----	----	0.00	----	MA
ICC AT VCC = +5V	-1.09	-700.U	-611.M	241.M	128	96.1	100.	0.00	-2.50	-10.0	7.85	----	----	0.00	----	MA
IOS(+)	-69.3	-5.00M	-45.3	7.48	122	92.2	92.2	0.00	-70.0	-90.0	3.30	----	----	0.00	----	MA
VOPP(+) PS=30V RL=10K	24.9	28.4	28.3	315.M	121	93.8	93.8	6.25	27.0	20.0	3.97	----	----	30.0	----	V
VOPP(+) PS=30V RL=2K	24.5	28.1	27.9	328.M	120	93.0	93.0	7.03	26.0	20.0	5.71	----	----	30.0	----	V
VOPP(+) PS=5V RL=10K	3.42	3.54	3.48	34.1M	120	93.8	93.8	6.25	3.00	1.50	14.2	----	----	5.00	----	V
VOPP(+) PS=5V RL=2K	3.35	3.47	3.41	35.9M	120	93.8	93.8	6.25	3.00	1.50	11.4	----	----	5.00	----	V
AVS(+) RL=10K	1.61	9.00K	2.58K	3.30K	55	93.0	98.4	57.8	25.0	1.00	774.M	----	----	10.0K	----	V/MV
AVS(+) RL=2K	1.10	9.00K	4.51K	4.69K	12	100.	100.	94.5	25.0	1.00	955.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=10K	36.4	9.00K	1.38K	2.85K	117	89.1	100.	8.59	5.00	1.00	482.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=2K	23.5	9.00K	1.71K	3.23K	117	85.2	100.	8.59	5.00	1.00	527.M	----	----	10.0K	----	V/MV
VOL--PS=30V; RL=10K	1.00	40.1	18.5	7.58	125	93.8	97.7	----	----	0.00	----	4.69	30.0	50.0	1.52	MV
VOH--PS=30V	24.5	28.2	28.0	336.M	120	93.0	93.0	7.03	25.0	20.0	9.03	----	----	30.0	----	V
IOH-PS=30V/FORCE 25V	-53.6	-50.0M	-43.3	9.25	123	93.0	93.0	----	----	-100.	----	7.03	-10.0	0.00	3.60	MA
VOL--PS=30V	898.M	4.97	1.08	703.M	128	96.9	96.9	----	----	0.00	----	3.13	2.00	5.00	1.31	V
IOL-PS=30V/FORCE 3V	100.M	39.9	20.1	8.31	121	91.4	97.7	4.69	5.00	0.00	1.82	----	----	40.0	----	MA
VOH--PS=4.5V	2.53	2.76	2.64	62.4M	120	93.8	93.8	6.25	2.40	1.50	3.78	----	----	4.50	----	V
IOH-PS=4.5V/FORCE 2.4	-19.0	-50.0M	-15.6	3.50	125	93.8	93.8	----	----	-30.0	----	6.25	-10.0	0.00	1.59	MA
VOL--PS=4.5V	22.3M	675.M	357.M	290.M	124	96.9	96.9	----	----	0.00	----	50.0	400.M	1.50	149.M	V
IOL-PS=4.5V/FORCE 0.4	765.M	36.4	10.6	7.69	121	95.3	98.4	45.3	8.00	0.00	341.M	----	----	50.0	----	UA

1/ * EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

2/ LO-FM = $\frac{\bar{X} - \text{LOW LIMIT}}{\sigma}$; HI-FM = $\frac{\text{HIGH LIMIT} - \bar{X}}{\sigma}$

Table 3-3. LM 124 Statistics at -55°C.

STATISTICAL DATA FOR MIXED LOT LM124 AT 25 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM $\frac{\bar{X}-LL}{\sigma}$ *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM $\frac{HL-\bar{X}}{\sigma}$ *	UNITS
VIO AT 30, 0, -15	-5.57	4.05	-73.8M	1.79	124	93.0	96.1	3.91	-5.00	-10.0	2.75	0.00	5.00	10.0	2.83	MV
VIO AT 2.0,-28.0,15	-6.11	1.65	-1.79	1.64	123	93.0	96.1	3.91	-5.00	-10.0	1.96	2.34	5.00	10.0	4.15	MV
VIO AT 5, 0, -1.4	-9.92	3.80	-200.M	1.94	125	94.5	96.1	4.69	-5.00	-10.0	2.47	0.00	5.00	10.0	2.68	MV
VIO AT 2.5,-2.5,-1.1	-4.32	3.36	-305.M	1.58	126	93.8	98.4	1.56	-5.00	-10.0	2.97	0.00	5.00	10.0	3.35	MV
IIO AT 30, 0, -15	-25.6	40.3	-1.12	8.92	125	90.6	96.9	1.56	-30.0	-120.	3.24	1.56	30.0	120.	3.49	NA
IIO AT 2.0,-28.0,15	-12.0	25.2	1.13	6.38	126	90.6	97.7	781.M	-30.0	-120.	4.88	781.M	30.0	120.	4.52	NA
IIO AT 5, 0, -1.4	-20.3	41.3	-264.M	6.76	124	90.6	96.1	0.00	-30.0	-120.	4.40	3.91	30.0	120.	4.48	NA
IIO AT 2.5,-2.5,-1.1	-15.8	35.0	1.92	6.32	128	92.2	99.2	0.00	-30.0	-120.	4.90	781.M	30.0	120.	4.44	NA
IIB(+)AT 30, 0, -15	-134.	-23.8	-51.9	21.0	122	92.2	95.3	2.34	-150.	-500.	4.48	2.34	-1.00	-5.00M	2.43	NA
IIB(+)AT 2.0,-28.0,15	-70.7	-4.65	-27.9	13.8	122	91.4	96.9	1.56	-150.	-500.	8.84	3.13	-1.00	-5.00M	1.95	NA
IIB(+)AT 5, 0, -1.4	-76.7	-14.7	-32.9	12.0	122	89.1	93.8	0.00	-150.	-500.	9.75	4.69	-1.00	-5.00M	2.65	NA
IIB(+) AT +-2.5,-1.1	-62.2	-1.50	-26.7	11.0	126	89.8	98.4	0.00	-150.	-500.	11.7	1.56	-1.00	-5.00M	2.34	NA
IIB(-)AT 30, 0, -15	-376.	-21.0	-53.5	35.8	123	96.9	98.4	781.M	-150.	-500.	2.69	3.91	-1.00	-5.00M	1.46	NA
IIB(-)AT 2.0,-28.0,15	-369.	-2.25	-31.6	34.2	125	99.2	99.2	781.M	-150.	-500.	3.46	2.34	-1.00	-5.00M	894.M	NA
IIB(-)AT 5, 0, -1.4	-357.	-14.5	-39.3	44.3	127	96.9	98.4	2.34	-150.	-500.	2.50	781.M	-1.00	-5.00M	865.M	NA
IIB(-) AT +-2.5,-1.1	-72.2	-10.0	-28.1	10.8	126	93.8	97.7	0.00	-150.	-500.	11.3	1.56	-1.00	-5.00M	2.52	NA
PSRR(+)	-22.0	48.6	15.6	7.94	127	96.1	96.1	0.00	-100.	-200.	14.6	781.M	100.	200.	10.6	UV/V
CMR1 AT VCM = 0-28V	65.8	160.	85.6	8.66	128	94.5	98.4	1.61	76.0	60.0	1.11	----	----	500.	----	dB
CMR3 AT VCM = 0-2.5V	71.2	89.9	78.0	2.68	122	91.4	94.5	4.69	70.0	60.0	2.99	----	----	500.	----	dB
ICC AT VCC = +30V	-8.43	-515.M	-1.33	1.16	128	96.9	96.9	3.13	-3.00	-10.0	1.44	----	----	0.00	----	MA
ICC AT VCC = +5V	-1.20	-2.90M	-682.M	252.M	128	94.5	100.	0.00	-2.00	-10.0	4.24	----	----	0.00	----	MA
IOS(+)	-62.4	-5.00M	-40.6	6.77	126	95.3	95.3	0.00	-70.0	-90.0	4.35	----	----	0.00	----	MA
VOPP(+) PS=30V RL=10K	26.2	28.5	28.4	214.M	122	94.5	94.5	5.47	27.0	20.0	6.60	----	----	30.0	----	V
VOPP(+) PS=30V RL=2K	25.6	28.4	27.9	267.M	123	95.3	95.3	4.69	26.0	20.0	7.30	----	----	30.0	----	V
VOPP(+) PS=5V RL=10K	3.57	3.72	3.64	44.5M	123	96.1	96.1	3.91	3.00	1.50	14.5	----	----	5.00	----	V
VOPP(+) PS=5V RL=2K	3.48	3.63	3.56	44.0M	124	96.9	96.9	3.13	3.00	1.50	12.7	----	----	5.00	----	V
AVS(+) RL=10K	1.90	9.00K	2.81K	3.25K	57	96.1	99.2	58.6	50.0	1.00	848.M	----	----	10.0K	----	V/MV
AVS(+) RL=2K	1.12	9.00K	3.05K	4.46K	9	100.	100.	96.9	50.0	1.00	672.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=10K	45.1	9.00K	1.49K	3.04K	115	87.5	100.	10.2	10.0	1.00	487.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=2K	44.4	9.00K	1.80K	3.28K	113	85.2	100.	11.7	10.0	1.00	546.M	----	----	10.0K	----	V/MV
VOL--PS=30V; RL=10K	2.10	41.2	18.0	6.99	128	96.1	99.2	----	----	0.00	----	2.34	30.0	50.0	1.71	MV
VOH--PS=30V	25.7	28.3	28.2	235.M	123	95.3	95.3	3.91	25.0	20.0	13.4	----	----	30.0	----	V
IOH-PS=30V/FORCE 25V	-49.9	-22.5	-40.0	5.11	123	93.0	95.3	----	----	-100.	----	3.91	-10.0	0.00	5.87	MA
VOL--PS=30V	864.M	1.41	915.M	48.4M	128	99.2	99.2	----	----	0.00	----	0.00	2.00	5.00	22.4	V
IOL-PS=30V/FORCE 3V	11.2	36.6	20.9	6.58	125	96.1	97.7	1.56	5.00	0.00	2.42	----	----	40.0	----	MA
VOH--PS=4.5V	2.57	2.89	2.75	71.6M	124	95.3	96.9	3.13	2.40	1.50	4.93	----	----	4.50	----	V
IOH-PS=4.5V/FORCE 2.4	-21.0	-50.0M	-16.5	3.32	126	96.9	96.9	----	----	-30.0	----	3.13	-10.0	0.00	1.95	MA
VOL--PS=4.5V	22.7M	571.M	246.M	231.M	128	100.	100.	----	----	0.00	----	37.5	400.M	1.50	669.M	V
IOL-PS=4.5V/FORCE 0.4	3.76	44.6	15.2	8.80	127	94.5	96.9	24.2	8.00	0.00	816.M	----	----	50.0	----	UA

// * EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ 2/ LO-FM = $\frac{\bar{X} - LOW\ LIMIT}{\sigma}$; HI-FM = $\frac{HIGH\ LIMIT - \bar{X}}{\sigma}$

Table 3-4. LM 124 Statistics at 25°C.

STATISTICAL DATA FOR MIXED LOT LM124 AT 125 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM 2/ *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 2/ *	UNITS
VIO AT 30, 0, -15	-9.99	3.54	-366.M	2.26	125	94.5	96.9	3.13	-7.00	-10.0	2.93	0.00	7.00	10.0	3.26	MV
VIO AT 2.0,-28.0,15	-7.57	640.M	-2.36	1.98	123	93.8	96.1	2.34	-7.00	-10.0	2.34	2.34	7.00	10.0	4.73	MV
VIO AT 5, 0, -1.4	-6.10	3.50	-267.M	2.02	128	95.3	100.	0.00	-7.00	-10.0	3.33	0.00	7.00	10.0	3.59	MV
D-VIO/D-T FROM 25 OC	-18.6	6.80	-2.05	5.00	124	92.2	95.3	0.00	-30.0	-50.0	5.59	3.13	30.0	50.0	6.41	UV/OC
VIO AT 2.5,-2.5,-1.1	-5.01	2.89	-526.M	1.86	126	95.3	98.4	1.56	-7.00	-10.0	3.48	0.00	7.00	10.0	4.05	MV
IIO AT 30, 0, -15	-19.5	32.5	-131.M	7.32	124	88.3	96.1	1.56	-30.0	-120.	4.08	2.34	30.0	120.	4.12	NA
IIO AT 2.0,-28.0,15	-8.25	21.0	1.81	4.02	126	92.2	97.7	781.M	-30.0	-120.	7.92	781.M	30.0	120.	7.02	NA
IIO AT 5, 0, -1.4	-21.7	34.0	-471.M	6.09	126	93.0	96.9	781.M	-30.0	-120.	4.85	1.56	30.0	120.	5.00	NA
D-IIO/D-T FROM 25 OC	-320.	120.	-1.47	56.3	125	92.2	95.3	2.34	-350.	-1.00K	6.19	0.00	350.	1.00K	6.25	PA/OC
IIO AT 2.5,-2.5,-1.1	-15.5	26.0	3.73	6.04	127	93.0	97.7	781.M	-30.0	-120.	5.59	0.00	30.0	120.	4.35	NA
IIB(+)AT 30, 0, -15	-180.	-25.8	-58.6	28.4	122	92.2	94.5	4.69	-150.	-500.	3.22	2.34	-1.00	-5.00M	2.03	NA
IIB(+)AT 2.0,-28.0,15	-63.0	-3.25	-28.2	14.2	122	91.4	98.4	1.56	-150.	-500.	8.60	3.13	-1.00	-5.00M	1.92	NA
IIB(+)AT 5, 0, -1.4	-96.4	-16.8	-37.2	15.7	126	93.8	96.1	781.M	-150.	-500.	7.17	781.M	-1.00	-5.00M	2.30	NA
IIB(+) AT +-2.5,-1.1	-77.1	-7.45	-27.9	13.6	126	92.2	96.9	781.M	-150.	-500.	9.00	781.M	-1.00	-5.00M	1.98	NA
IIB(-)AT 30, 0, -15	-338.	-24.2	-61.7	38.4	124	95.3	96.9	3.13	-150.	-500.	2.30	3.13	-1.00	-5.00M	1.58	NA
IIB(-)AT 2.0,-28.0,15	-344.	-2.50	-32.3	31.9	125	99.2	99.2	781.M	-150.	-500.	3.69	2.34	-1.00	-5.00M	983.M	NA
IIB(-)AT 5, 0, -1.4	-350.	-16.3	-38.0	31.6	127	97.7	98.4	781.M	-150.	-500.	3.54	781.M	-1.00	-5.00M	1.17	NA
IIB(-) AT +-2.5,-1.1	-86.5	-6.40	-32.6	14.1	126	94.5	97.7	0.00	-150.	-500.	8.34	1.56	-1.00	-5.00M	2.24	NA
PSRR(+)	-37.4	62.0	19.1	10.2	127	94.5	95.3	0.00	-100.	-200.	11.7	781.M	100.	200.	7.96	UV/V
CMR1 AT VCM = 0-28V	65.5	160.	84.1	8.66	128	96.9	98.4	4.69	76.0	60.0	936.M	----	----	500.	----	dB
CMR3 AT VCM = 0-2.5V	68.3	95.9	77.6	4.15	126	93.0	96.9	3.13	70.0	60.0	1.83	----	----	500.	----	dB
ICC AT VCC = +30V	-7.68	-518.M	-1.35	1.05	128	96.9	96.9	3.13	-3.00	-10.0	1.57	----	----	0.00	----	MA
ICC AT VCC = +5V	-1.19	-388.M	-722.M	219.M	128	91.4	100.	0.00	-2.00	-10.0	5.84	----	----	0.00	----	MA
IOS(+)	-52.5	-5.00M	-31.7	5.78	126	95.3	95.3	0.00	-70.0	-90.0	6.62	----	----	0.00	----	MA
VOPP(+) PS=30V RL=10K	22.4	28.8	28.6	579.M	124	95.3	96.1	3.91	27.0	20.0	2.80	----	----	30.0	----	V
VOPP(+) PS=30V RL=2K	22.1	28.2	27.8	626.M	124	95.3	96.1	4.69	26.0	20.0	2.85	----	----	30.0	----	V
VOPP(+) PS=5V RL=10K	3.81	4.01	3.91	61.3M	124	96.9	96.9	3.13	3.00	1.50	14.9	----	----	5.00	----	V
VOPP(+) PS=5V RL=2K	3.71	3.91	3.81	62.3M	124	96.9	96.9	3.13	3.00	1.50	13.0	----	----	5.00	----	V
AVS(+) RL=10K	1.40	9.00K	977.	1.88K	70	94.5	95.3	50.8	25.0	1.00	506.M	----	----	10.0K	----	V/MV
AVS(+) RL=2K	1.15	9.00K	4.64K	4.68K	8	100.	100.	94.5	25.0	1.00	986.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=10K	30.8	9.00K	872.	2.35K	121	92.2	92.2	4.69	5.00	1.00	369.M	----	----	10.0K	----	V/MV
AVS AT +-5V RL=2K	33.3	9.00K	1.07K	2.63K	123	90.6	90.6	3.91	5.00	1.00	407.M	----	----	10.0K	----	V/MV
VOL--PS=30V; RL=10K	3.60	42.8	19.6	7.04	128	95.3	99.2	----	----	0.00	----	10.2	30.0	50.0	1.47	MV
VOH--PS=30V	22.1	28.6	28.2	603.M	124	95.3	96.1	3.91	25.0	20.0	5.26	----	----	30.0	----	V
IOH-PS=30V/FORCE 25V	-41.5	-19.4	-31.6	4.30	121	92.2	94.5	----	----	-100.	----	5.47	-10.0	0.00	5.01	MA
VOL--PS=30V	798.M	1.22	863.M	38.4M	128	99.2	99.2	----	----	0.00	----	0.00	2.00	5.00	29.7	V
IOL-PS=30V/FORCE 3V	11.1	29.2	16.6	3.53	125	93.8	96.1	1.56	5.00	0.00	3.29	----	----	40.0	----	MA
VOH--PS=4.5V	2.24	3.07	2.79	188.M	124	89.8	96.9	9.38	2.40	1.50	2.08	----	----	4.50	----	V
IOH-PS=4.5V/FORCE 2.4	-21.0	-50.0M	-14.7	3.75	126	96.9	96.9	----	----	-30.0	----	7.03	-10.0	0.00	1.25	MA
VOL--PS=4.5V	23.9M	438.M	137.M	119.M	128	89.1	100.	----	----	0.00	----	3.13	400.M	1.50	2.21	V
IOL-PS=4.5V/FORCE 0.4	4.16	49.8	22.8	12.1	120	90.6	98.4	3.13	8.00	0.00	1.23	----	----	50.0	----	UA

1/ * EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ 2/ LO-FM = $\frac{\bar{X} - \text{LOW LIMIT}}{\sigma}$; HI-FM = $\frac{\text{HIGH LIMIT} - \bar{X}}{\sigma}$

Table 3-5. LM 124 Statistics at 125°C.

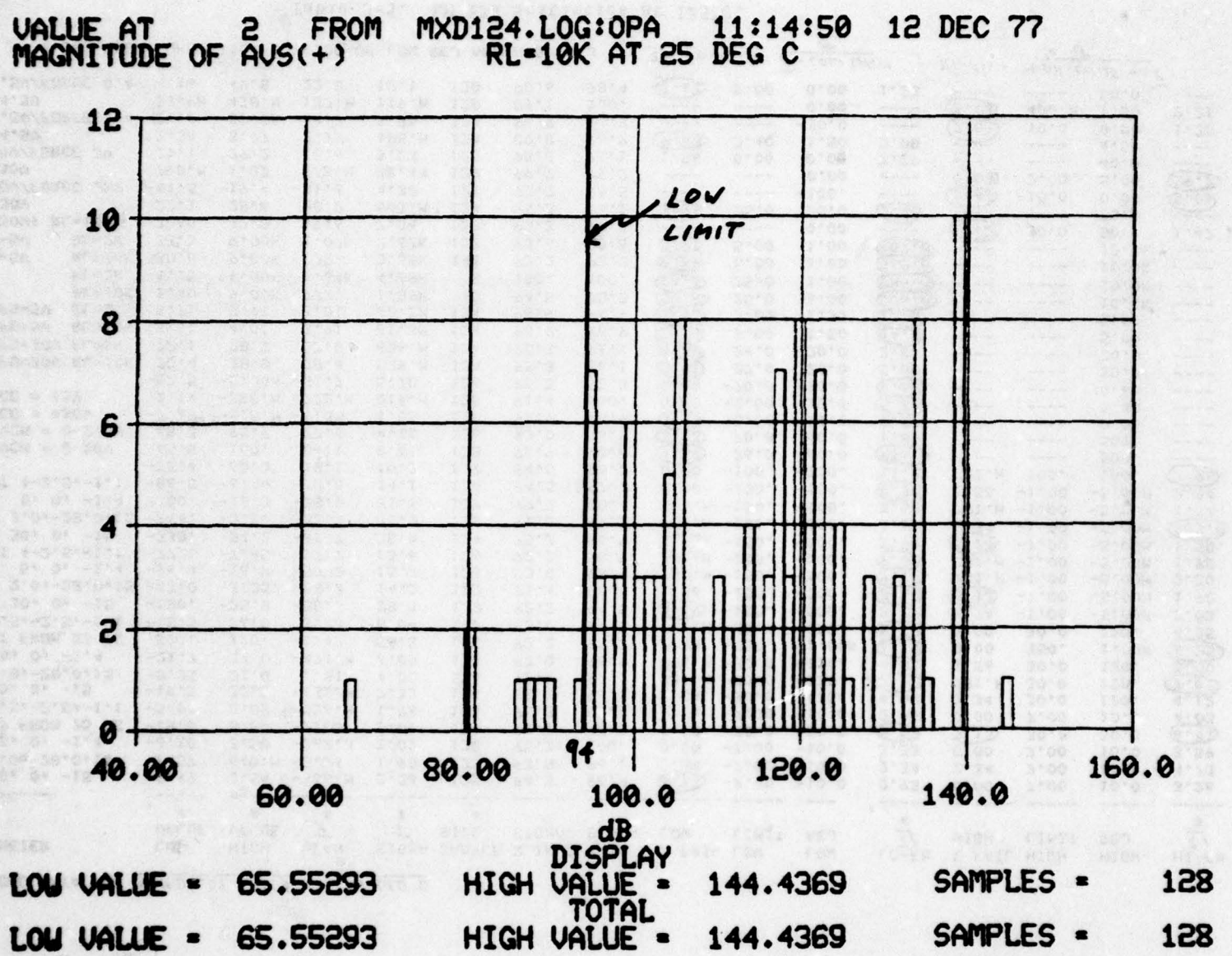
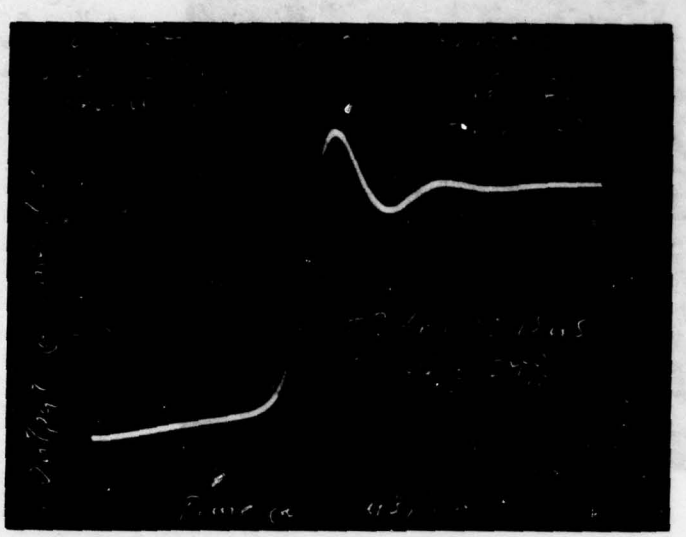
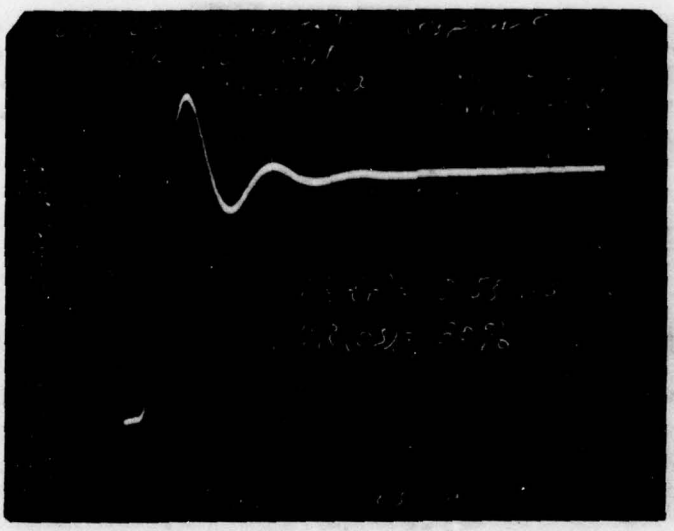


Figure 3-7. LM 124 Gain Magnitude Histogram.



+ V_{cc} = 25 V
- V_{cc} = 0V
TR(tr) = 0.75 us
TR(os) = 24%

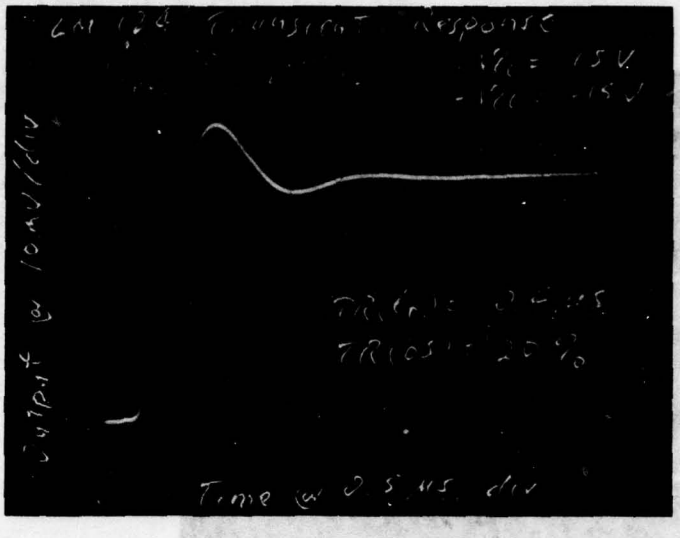


+ V_{cc} = 25 V
- V_{cc} = - 1V
TR(tr) = 0.55 us
TR(os) = 30%

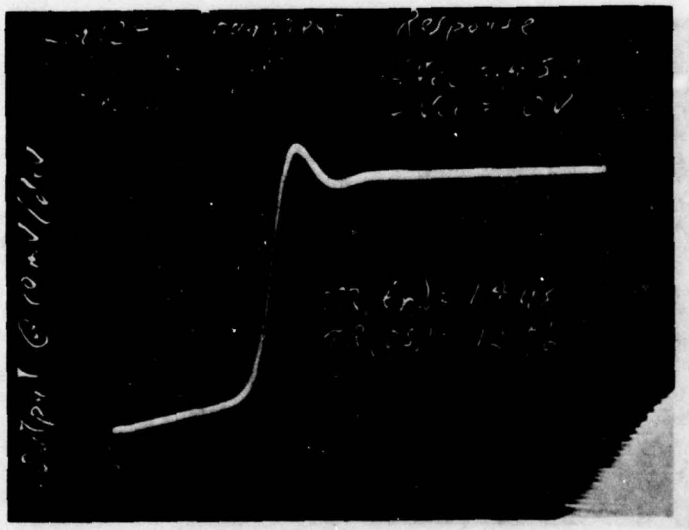
Figure 3-8. LM 124 Transient Response* v.s. Power Supply Conditions.

(sheet 1 of 2)

* Pulse generator risetime = 30 ns



$+ V_{cc}$ = 15 V
$- V_{cc}$ = -15 V
TR(tr) = 0.4 us
TR(os) = 20%



$+ V_{cc}$ = 4.5 V
$- V_{cc}$ = 0V
TR(tr) = 1.4 us
TR(os) = 12%

Figure 3-8. LM 124 Transient Response* v.s. Power Supply Conditions.

(sheet 2 of 2)

*** Pulse generator risetime = 30 ns**

Parameter Symbol	Conditions $5V \leq +V_{cc} \leq 30V$	T_A °C	LM124 Cat Min	LM124 Cat Max	JC-41 Rec Min	JC-41 Rec Max	Worst Data $\bar{X} \pm 3\sigma$ Min	Worst Data $\bar{X} \pm 3\sigma$ Max	GEOS /110-05 Min	GEOS /110-05 Max	Units
V_{10}	1/	25	-5	5	-5	5	-6.02	5.62	-5	5	mV
		-55/125	-7	7	-7	7	-7.15	6.41	-7	7	
$\Delta V_{10}/\Delta T$	$+V_{cc}$ = 5V, V_{cm} = -2.5V	-55/25	(No Spec)		-30	30	-20.82	11.16	-30	30	$\mu V/°C$
		25/125			-30	30	-17.05	12.95	-30	30	
I_{10}	1/ R_S = 20 KΩ	25/125	-30	30	-30	30	-27.88	25.64	-30	30	nA
		-55	-100	100	-90	90	-63.3	71.1	-75	75	
$\Delta I_{10}/\Delta T$	$+V_{cc}$ = 5V V_{cm} = 2.5V	-55/25	(No Spec)		-700	700	-592.3	517.7	-700	700	pA/°C
		25/125			-600	600	-170.4	167.4	-400	400	
$+I_{1B}$	1/ R_S = 20 KΩ	25/125	-	150	-150	-1	-143.8	26.6	-150	-1	nA
		-55	-	300	-300	-1	-126.9	69.3	-300	-1	
$-I_{1B}$	1/ R_S = 20 KΩ	25/125	-	150	-150	-1	-176.9	53.5	-150	-1	nA
		-55	-	300	-300	-1	-175.2	69.6	-300	-1	
+ PSRR	$+V_{cc}$ = 20 V	-55/125	65dB	-	-100	100	-41.7	74.7	-100	100	$\mu V/V$
CMR	28 V Common Mode Range	-55/125	65	-	76	-	53.4	120.6	76	-	dB
I_{OS} (+)	V_{cc} = 30 V	-55/125	-	60	-	70	-67.74	-22.86	-70	-	mA
I_{cc}	V_{cc} = 30 V	-55	-	-	-	4	-2.56	5	-	4	mA
		25	-	3	-	3	-2.32	4.81	-	3	
		125	-	-	-	3	-1.8	4.5	-	3	

Table 3-6. Device type -05 limits comparison

Parameter Symbol	Conditions $5V \leq +V_{cc} \leq 30V$	T_A °C	LM124 Cat Min	LM124 Cat Max	JC-41 Rec Min	JC-41 Rec Max	Worst Data $\bar{X} \pm 3$ Min	Worst Data $\bar{X} \pm 3$ Max	GEOS /110-05 Min	GEOS /110-05 Max	Units
$+V_{OP}$	V_{cc}=30V R_C=10KΩ	-55/125	27	-	27	-	26.86	30.34	+27	-	V
	R_C= 2KΩ	-55/125	26	-	26	-	25.92	29.68	+26	-	
A_{VS}(+)	V_{cc}=30V R_C=10KΩ	25	50	-	50	-	-6490	12560	50	-	V/mV
	2KΩ	-55/125	25	-	25	-	-4663	6617	25	-	
A_{VS}	V_{cc}= 5V R_C=10KΩ	25	(No Spec)		10	-	-7630	10610	10	-	V/mV
	2KΩ	-55/125			10	-	-6820	8960	10	-	
V_{OL}	30V, 10KΩ	-55/125	-	.02	-	.02	-.004	.041	-	.035	V
	30V, 3mA	-55/125	-	-	(No Spec)		-2.16	3.19	-	1.5	
	4.5V, 2uA	-55/125	-	-			-.513	1.23	-	0.4	
V_{OH}	30V, 10mA	-55/125	(No Spec)		(No Spec)		26.39	30.01	27	-	V
	4.5V, 10mA	-55/125					2.23	3.35	2.4	-	
TR (tr)	V_{cc} = 30V, C_F = 10pf, V_{in} = 50 mV	-55/125	(No Spec)		-	1	(.75 typ)		-	1.0	µS
TR (OS)		-55/125	(No Spec)		-	40	(24% typ)		-	40	%
SR(+), SR(-)	V_{cc}=30V, C_F=10pf, V_{in} = 10V	-55/125	(No Spec)		0.1	-	(0.5 typ)		0.1	-	V/uS
N_i (BB)	V_{cc} = 30V, R_S = 50Ω	25	(No Spec)		-	15	(10 max typ)		-	15	μV_{rms}
N_i (PC)	V_{cc} = 30V, R_S = 20 KΩ	25	(No Spec)		-	50	(5 max typ)		-	50	μV_{pk}
CS	V_{cc} = 30V	25	(No Spec)		80	-	(100 min typ)		80	-	dB

Table 3-6. Device type -05 limits comparison (cont'd.)

TABLE I. Electrical performance characteristics.

Characteristics	Symbol	Conditions (unless otherwise specified, requirements of 3.4 and figure 6 shall apply).		Device types 01,02 Limits Min	01,02 Limits Max	03 Limits Min	03 Limits Max	04 Limits Min	04 Limits Max	05 Limits Min	05 Limits Max	Units
Input offset voltage	V_{IO}	1/	T_A = 25°C	-5	5	-3	3	-5	5	-5	+5	mV
			-55°C ≤ T_A ≤ 125°C	-6	6	-5	5	-6	6	-7	+7	
Input offset voltage temperature sensitivity	$\Delta V_{IO}/\Delta T$		ΔT_A from -55°C to 25°C	-25	25	-20	20	-25	25	-30	+30	µV/°C
			ΔT_A from 25°C to 125°C	-25	25	-20	20	-25	25	-30	+30	
Input offset current	I_{IO}	1/	25°C ≤ T_A ≤ 125°C	-25	25	-30	30	-75	75	-30	+30	nA
		R_S = 20 kΩ	T_A = -55°C	-75	75	-75	75	-150	150	-75	+75	
Input offset current temperature sensitivity	$\Delta I_{IO}/\Delta T$		ΔT_A from -55°C to 25°C	-400	400	-500	500	-1000	1000	-700	700	pA/°C
			ΔT_A from 25°C to 125°C	-200	200	-200	200	-500	500	-400	400	
Input bias current	$+I_{IB}$	1/	25°C ≤ T_A ≤ 125°C	0.1	.00	-200	-1	-250	-1	-150	-1	nA
		R_S = 20 kΩ	T_A = -55°C	0.1	325	-325	-1	-400	-1	-300	-1	
	$-I_{IB}$	1/	25°C ≤ T_A ≤ 125°C	0.1	100	-200	-1	-250	-1	-150	-1	nA
		R_S = 20 kΩ	T_A = -55°C	0.1	325	-325	-1	-400	-1	-300	-1	
Power supply rejection ratio	+PSRR	Device types 01 through 04: $+V_{CC}$ = 10 V and $-V_{CC}$ = -20 V; device type 05: $+V_{CC}$ = 20 V		-100	100	-100	100	-100	100	-100	100	µV/V
	-PSRR	$+V_{CC}$ = 20V and $-V_{CC}$ = -10 V (Device types 01 through 04 only)		-100	100	-100	100	-100	100	---	---	µV/V
Input voltage common mode rejection	CMR	2/ Common mode range { 30 V for types 01-04; 28 V for type 05		76	---	76	---	76	---	76	---	dB
Output short circuit current (for positive output)	$I_{OS(+)}$	3/ (Only one amplifier shorted to ground at one time) t ≤ 25 ms For types 01-04: $\pm V_{CC}$ = ±15 V For type 05: $+V_{CC}$ = 30 V.		-55	---	-80	---	-80	---	-70	---	mA
Output short circuit current (for negative output)	$I_{OS(-)}$			---	55	---	80	---	80	---	---	mA

See notes at end of table.

TABLE 3-7. MIL-M-38510/110 electrical specifications.

TABLE I. Electrical performance characteristics -Continued.

Characteristics	Symbol	Conditions (Unless otherwise specified, requirements of 3.4 and figure 6 shall apply)		Device types 01,02 Limits Min	01,02 Limits Max	03 Limits Min	03 Limits Max	04 Limits Min	04 Limits Max	05 Limits Min	05 Limits Max	Units
Supply current	I_{CC} 4/	For types 01-04: $+V_{CC} = \pm 15V$	T_A = -55°C	---	4.5	---	9	---	13	---	4	mA
			T_A = 25°C	---	3.6	---	7	---	11	---	3	
		For type 05: $+V_{CC}$ = 30 V	T_A = 125°C	---	3.6	---	7	---	11	---	3	
Maximum output voltage swing	$+V_{OP}$	For types 01-04, $\pm V_{CC} = \pm 20V$	R_L = 10 kΩ	+16	---	+16	---	+16	---	+27	---	V
		For type 05, $+V_{CC}$ = +30 V	R_L = 2 kΩ	+15	---	+15	---	+15	---	+26	---	V
	$-V_{OP}$	$\pm V_{CC} = \pm 20$ V	R_L = 10 kΩ	---	-16	---	-16	---	-16	---	---	V
			R_L = 2 kΩ	---	-15	---	-15	---	-15	---	---	V
Single ended open	$A_{VS(+)}$ and $A_{VS(-)}$	R_L = 10 kΩ For types 01-04: $\pm V_O = \pm 15$ V For type 05: V_O = 1 to 26 V	T_A = 25°C	50	---	50	---	50	---	50	---	V/mV
			-55°C ≤ T_A ≤ 125°C	25	---	25	---	25	---	25	---	
		R_L = 2 kΩ For types 01-04: $\pm V_O = \pm 15$ V For type 05: V_O = 1 to 16 V	T_A = 25°C	50	---	50	---	50	---	50	---	
			-55°C ≤ T_A ≤ 125°C	25	---	25	---	25	---	25	---	
Loop voltage gain	A_{VS}	R_L = 10 kΩ and 2 kΩ For types 01-04: $\pm V_{CC} = \pm 5$ V, $V_O = \pm 2$ V	T_A = 25°C	10	---	10	---	10	---	10	---	
		For type 05: $+V_{CC}$ = + 5 V, V_O = 1 to 3 V	-55°C ≤ T_A ≤ 125°C	10	---	10	---	10	---	10	---	
Low level output voltage	V_{OL}	+ V_{CC} = 30 V, R_L = 10 kΩ		---	---	---	---	---	---	---	35	mV
		$+V_{CC}$ = 30 V, I_{OL} = 5 mA		---	---	---	---	---	---	---	1.5	V
		$+V_{CC}$ = 4.5 V, I_{OL} = 2 µA		---	---	---	---	---	---	---	0.4	

See notes at end of table.

TABLE 3-7. MIL-M-38510/110 electrical specifications. (cont'd.)

TABLE I. Electrical performance characteristics.-Continued.

Characteristics	Symbol	Conditions (Unless otherwise specified, requirements of 3.4 and figure 6 shall apply)		Device types 01,02 Limits Min	01,02 Limits Max	03 Limits Min	03 Limits Max	04 Limits Min	04 Limits Max	05 Limits Min	05 Limits Max	Units
High level output voltage	V_{OH}	$+V_{CC}$ = 30 V, I_{OH} = 10 mA		---	---	---	---	---	---	27	---	V
		$+V_{CC}$ = 4.5 V, I_{OH} = 10 mA		---	---	---	---	---	---	2.4	---	
Transient response	TR(tr)	5/ Figure 8; V_{IN} = 50 mV; $\pm V_{CC}$ = ±20V for types 01 - 04; V_{CC} = +30 V for type 05	A_V = 1	---	1.0	---	---	---	0.3	---	1.0	µs
			A_V = 5	---	1.0	---	0.2	---	---	---	---	
	TR(OS)		Overshoot	---	25	---	35	---	40	---	40	%
Slew rate	SR(+) and SR(-)	Figure 8; V_{IN} = 50 mV; $\pm V_{CC}$ = ±20 V for types 01 - 04; V_{CC} = +30 V for type 05	A_V = 1	0.2	---	---	---	0.6	---	1.0	---	V/µs
			A_V = 5	0.8	---	0.8	---	---	---	---	---	
Noise (broadband)	NI(BB)	T_A = 25°C, R_S = 50Ω		---	15	---	5	---	5	---	15	µVrms
Noise (popcorn)	NI(PC)	T_A = 25°C, R_S = 20 kΩ		---	40	---	50	---	50	---	50	µVpeak
Channel separation	CS	T_A = 25°C (Figure 7)		80	---	80	---	80	---	80	---	dB

See notes

TABLE 3-7. MIL-M-38510/110 electrical specifications. (cont'd.)

1/ Device types 01-04 shall be tested at V_{CM} = 0, +15 V and -15 V with $\pm V_{CC}$ = ±20 V; and at V_{CM} = 0 V and -2.5 V with $\pm V_{CC}$ = ±5 V. Device type 05 shall be tested at V_{CM} = 13 V and -15 V with $+V_{CC}$ = 30 V and $-V_{CC}$ = 0; and at V_{CM} = 0 and 2.5 V with $+V_{CC}$ = 5 V and $-V_{CC}$ = 0.

2/ CMR is determined by measuring input offset voltage as follows:

Offset voltage condition	Device types						Units
	01 - 04			05			
	$+V_{CC}$	$-V_{CC}$	V_O	$+V_{CC}$	$-V_{CC}$	V_O	
1	35	-5	15	30	0	15	V
2	5	-35	-15	2	-28	-13	V

3/ Continuous limits will be considerably lower and apply for $-55°C \leq T_A \leq 25°C$.

4/ I_{CC} limits are the total for all four amplifiers at no load, connected as grounded followers.

5/ Device type 05 transient response is specified with the input pulse referenced to 5 V. For applications purposes the device may be operated with the input referenced to ground, however, saturation effects will cause the response time to increase by approximately 50 percent.

TABLE 3-7. MIL-M-38510/110 electrical specifications. (cont'd).

SECTION IV

Bi-FET OPERATIONAL AMPLIFIER

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SECTION IV

Bi-FET OPERATIONAL AMPLIFIER

4.1 Background and Introduction

Bi-FET operational amplifiers represent a new class of devices in the evolution towards perfecting the ideal op amp. As the name of the process implies, Bi-FET op amps combine bipolar and J-FET transistors on a monolithic integrated circuit. This marriage of technologies combines standard bipolar linear processing with ion implantation. The op amp parameters which are enhanced by the Bi-FET process are high input impedance, low output impedance, wide bandwidth, high slew rates and low noise. Since the debut of Bi-FET op amps, users have been interested in incorporating them into new designs.

A review of linear device applications in military systems as well as a priority list of the JC-41 Committee were key reasons to characterize Bi-FET op amps for MIL-M-38510 procurement.

4.2 Device Type Description

A typical schematic circuit of a Bi-FET op amp is shown in Figure 4-1. Matched J-FET transistors are used for the differential input gain stage, the input current source loads and the offset adjustment control. The drain outputs of the input J-FETS feed a bipolar transistor differential stage. Signal conversion from differential to single ended is made at the collector of Q8. Since current sources exist at both the source and drain terminals of the input J-FETS, some mechanism must also exist to deal with the excess common mode current which is sourced from Q1, but not sunk by J10 and J11. Common mode feedback from the differential bipolar stage current source to the source terminals of J1 and J2 solves this problem.

With J-FET input transistors the op amp bias currents + I_{iB}, and - I_{iB} are much smaller than is possible with bipolar transistors. Since these currents are leakage currents, they are temperature sensitive and approximately double for every 10°C increase in temperature. Low noise and good high frequency response are other benefits of the J-FET front end transistors. The single ended output signal from Q8 and its J3 current source load is further amplified by the class B output stage. This output stage is a little unusual in that a J-FET, J5, complements the other bipolar output transistors. This design configuration eliminates the need for a PNP output current sinking transistor. The output J-FET also improves the stability of the op amp in driving large capacitive loads.

A Bi-FET op amp with bias current compensation is shown in Figure 4-2. This design technique is used to maintain low bias currents at elevated temperatures.

4.3 Automatic Test Development

Developing the tests for the Bi-FET op amps was done in a manner similar to previous quad op amp characterizations. A test program and an adapter card were developed in order to enable testing with GEOS' Tektronix S-3260 automatic IC test system. While the program and adapter were being developed several devices were analyzed on a Tektronix 577 curve tracer. This manual test phase is good for discovering anomalies and possible automatic tester problems. During the early characterization phase, GEOS had a requirement to production test several types of op amps for a military system. For economic considerations it was decided to build a universal op amp tester which could be programmed to test 741's, LM108A's and the LF155 series Bi-FETS.

Only limited success was achieved with the programmable tester. Although all 741 type and most Bi-FET static parameters could be tested, the Bi-FET configuration was not stable in the test modes for I_{IO} and + I_{IB}. In these modes 5 megohm resistors are switched in to the op amp inputs, so that the low (picoamp) bias currents can make a measurable effect on the offset voltage. The complexity of the test adapter prevented any simple circuit "fixes" from working. Bench observations of a tightly configured "breadboard" test circuit showed that the length and location of the non-inverting input wiring determined whether the circuit would be stable, oscillate or be sensitive to 60 Hz pickup.

An antenna wire on the non-inverting input, depending on its placement, could yield a mix of sustained oscillations and 60 Hz pickup as well. The sensitivity to these disturbances was much less severe on the inverting input, and also when the 5 MΩ resistor(s) was (were) shorted out. Capacitance added from the non-inverting input to ground is also helpful in stabilizing the test circuit. Using the information from these observations a second adapter was built. This new adapter was built with the following characteristics:

1. The D.U.T. (device under test) socket and all associated components were designed on an artwork for an etched copper printer circuit board.

2. The D.U.T. (+) and (-) input runs to their connections were made as short as possible.

3. Relay cans were grounded.

4. The component side of the board and much of the run side of the board were left as copper ground planes.

5. After the component lead holes were drilled, all ungrounded holes had copper removed with a fluted drill bit.

6. De-coupling capacitors were added as close as possible to the I.C. V_{cc}'s.

A test circuit is shown in Figure 4-3.

This circuit is very similar to the standard op amp test circuit for bipolar devices. One major difference is that with relay K8, the bias current measurement resistors can be programmed for 5 MΩ or 100 KΩ. This feature is required in measuring Bi-FET bias current over the 25°C - 125°C temperature range, since its magnitude can increase by a factor of 1000.

Devices were submitted by six I.C. manufacturers to form an industry test sample. Unfortunately, there are enough difference in the devices to prevent all the devices from being pooled into a single statistical test group for all parameters.

Shown below is a schedule of the test groups, device types and quantities.

Test Group	Type	Vendors	Qty.
1	155	F, S	24
2	156	F, S, A	24
3	157	S, A, N	24
4	155A	N	19
5	156A	N	20
6	157A		0
7	155A	P	20
8	156A	P	19
9	157A	P	20
10	355	T	9
		TOTAL	179

The rationale for the designated test groups are as follows:

1. Between the commercial type 155, 156 and 157 devices there are differences in supply current and slew rate.

2. The A subscript parts have tighter front end tolerances that their non-A counterparts.

3. One vendor (P) employs a bias current compensation scheme to give improved front end characteristics. Statistically pooling this data with that of the other vendor sources may obscure the details of each group.

4. The 355 group is only guaranteed for the 0 - 70°C commercial temperature range.

4.4 Tabulation of Test Data

While this report was being written, the automatic testing of the sample population of Bi-FET op amps was proceeding. The test data format is similar to that presented for the quad op amps and quad comparators in this report (individual data sheets, statistical data summaries, and histograms).

With the Bi-FET op amps, emphasis is placed on the input bias currents of the devices. Typical curves of bias current vs. common mode voltage are shown in Figure 4-4, 4-5, 4-6 and4-7. Correlation between curve tracer and automatic tester data is shown in Figure 4-8. How temperature effects bias current is shown in Figure 4-9.

4.5 Discussion

The purported improvement of Bi-FET op amps over conventional bipolar IC op amps is in input bias current. The degree of improvement must be qualified, however, since under certain conditions of either common mode voltage range or temperature or both, Bi-FET bias currents may be larger than bipolar device bias currents. With Bi-FET devices, + I_{iB} and - I_{iB} are gate leakage currents of the front end J-FETS. The curves of Figure 4-4 through 4-8 show how bias current varies with common mode voltage for different devices and power supply conditions. It can be seen that each of the curves is similar to a diode p-n junction volt - ampere characteristic turned up side down.

The orientation of a p-n junction with the same volt - ampere characteristic as in the observed figures is with the cathode end on the bottom and the anode end on top. Thus reverse junction current would be in the positive direction on the curve. The "zener - shape" breakdown at the negative common mode voltage extreme is actually the point where the J-FET P-n junction is forward biased. This is, of course, a forbidden zone to operate a J-FET and occurs for negative common mode voltage within two volts of the negative supply rack. Inspection of the device schematic confirms this, since the source terminal of the J-FET is elevated by three p-n junction drops from - V_{cc}.

The common mode reverse bias voltage range to the right of the forward bias knee is the most desirable operating range for low bias current. With $\pm V_{cc} = \pm 20$ V and a common mode voltage range from $V_{CM} = -15V$ to $V_{CM} = +5V$, bias current increases only slightly. Diffusion characteristics, geometry and minority concentration determine the amount of reverse current. Reverse voltage only effects the current indirectly by increasing the effective depletion layer thickness of the junction. For further increases in positive common mode voltage, the junction is technically operating in the multiplication range. In other words the minority carriers that comprise the reverse current have sufficient energy to break additional valence bonds and thus multiply the generation of hole-election pairs.

In a normal p-n junction avalanche breakdown eventually occurs. When this happens the current increases at an infinite rate with voltage and the well known "zener clamp" voltage has been reached. Because there is resistance in series with the J-FET P-N junction avalanche breakdown does not occur. However, the bias current that flows will be limited by the supply voltage levels, the series resistance and the junction breakdown characteristics. In practice this current could be a thousand times the current at zero common mode voltage.

In order to provide the user with information on bias current vs common mode voltage behavior as well as to guarantee it, the MIL-M-38510/114 slash sheet specifies bias current at four voltage conditions as follows:

Condition	$\pm V_{cc}$	V_{cm}	I_{iB} @ T = 25°C (min)	(max)
1	± 20V	- 15V	-100pA	100 pA
2	± 20V	0V	-100pA	100 pA
3	± 20V	+ 15V	-100pA	2000 pA
4	± 15V	+ 10V	-100pA	300 pA

Test condition 1 is a check to determine that at the negative common mode voltage limit the J-FET inputs are not forward biased. Test condition 2 indicates the normal zero common mode voltage leakage current. It is also the base line for delta I_{iB} measurements. The breakdown characteristics of the device are tested in condition 3 at the positive common mode voltage limit.

This will always represent the worst case maximum input bias current condition. In many user applications with ± 15V supplies, test condition 4 represents the maximum input bias current of the device. The reason for the non-zero minimum limit is that one of the popular suppliers of the Bi-FET op amps employs a bias current compensation scheme, which can yield "wrong polarity" bias current. In this scheme collector current of a bipolar transistor is designed to trim out the J-FET gate current that flows. Figure 4.2 shows how bias current compensation modifies the basic J-FET front end.

As observed at the Bi-FET input terminals, only the difference current between the J-FET and bipolar devices shows. Figure 4-5 shows an over-compensated bias current characteristic of a typical device with bias current compensation.

Ambient temperature is another important condition which effects bias current. This is so because the leakage current of the devices approximately double for each 10°C rise in temperature. Figure 4-9 illustrates how the worst case limits of the devices increase with temperature. It should be observed that the slash sheet specification on bias current is with regard to junction temperature conditions.

The reason for T_j measurements is that in automatic production testing, the devices are processed at a high through-put rate and their junction temperatures have not had time to stabilize at some delta above the ambient. If the bias current limits were specified as T_A, a wait time of from three to four minutes would be required. Figure 4-10 shows the effect of warm-up time on bias current. Not only would this add significantly to the cost of testing, but the limits would have to take into account the package thermal resistance, device type, and the power supply conditions according to the relationship $T_j = T_A + 2\ V_{cc}\ I_{cc}\ \theta_{jA}$.

where
T_j = Junction temperature in °C
T_A = Ambient temperature in °C
V_{cc} = Power supply voltage
I_{cc} = Worst case power supply current
θ_{jA} = Package thermal resistance (junction - ambient)

The user can expect the operating bias current to be from three to four times the value corresponding to the stated junction temperature value.

4.6 Conclusions and Recommendations

Characterization of the Bi-FET op amps is not complete at the time of this writing (September 1978). The recommendations of the JC-41 Committee as modified by GEOS with regard to bias current are submitted as a tentative specification. When the testing of an industry wide sample of over 100 parts has been completed, comparisons will be made between the statistical data and the JC-41 limits to confirm or modify those limits as required.

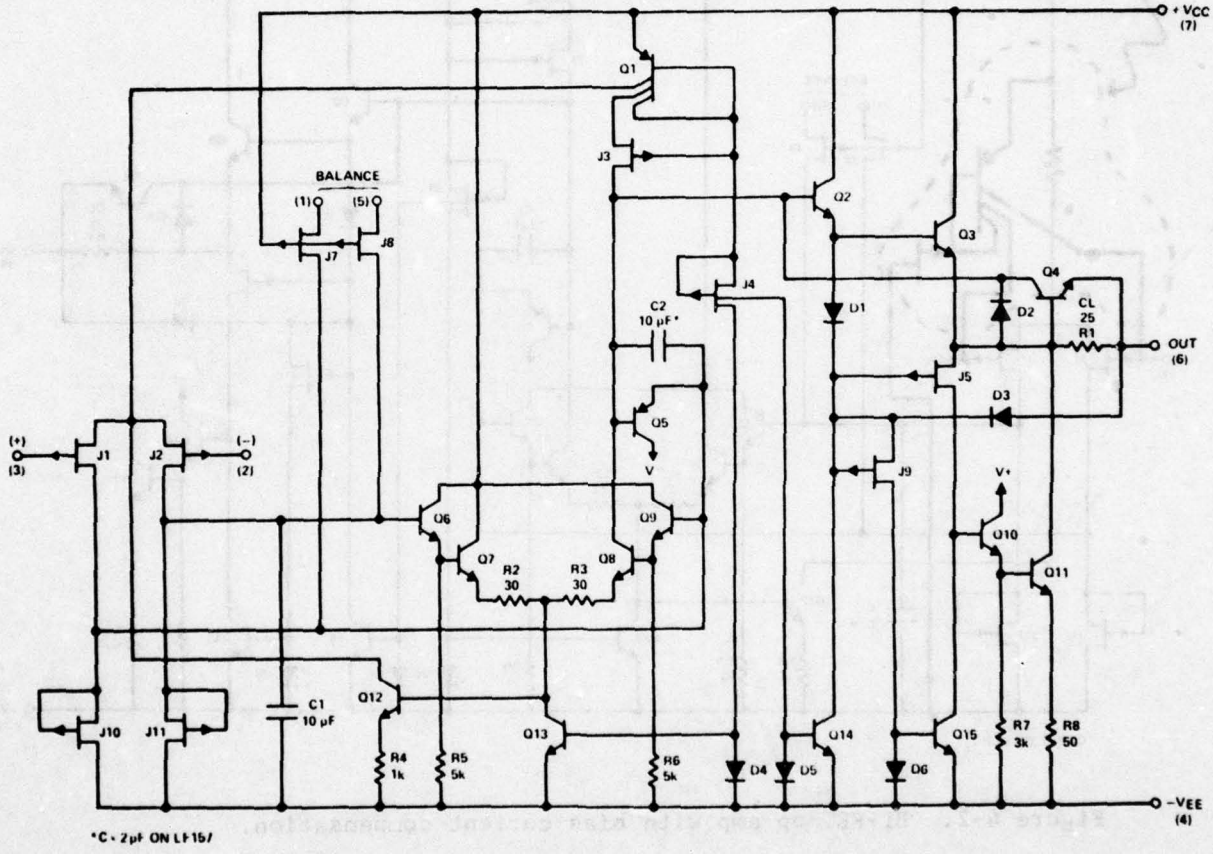


Figure 4-1. Typical Bi-FET op amp (LF155/156/157).

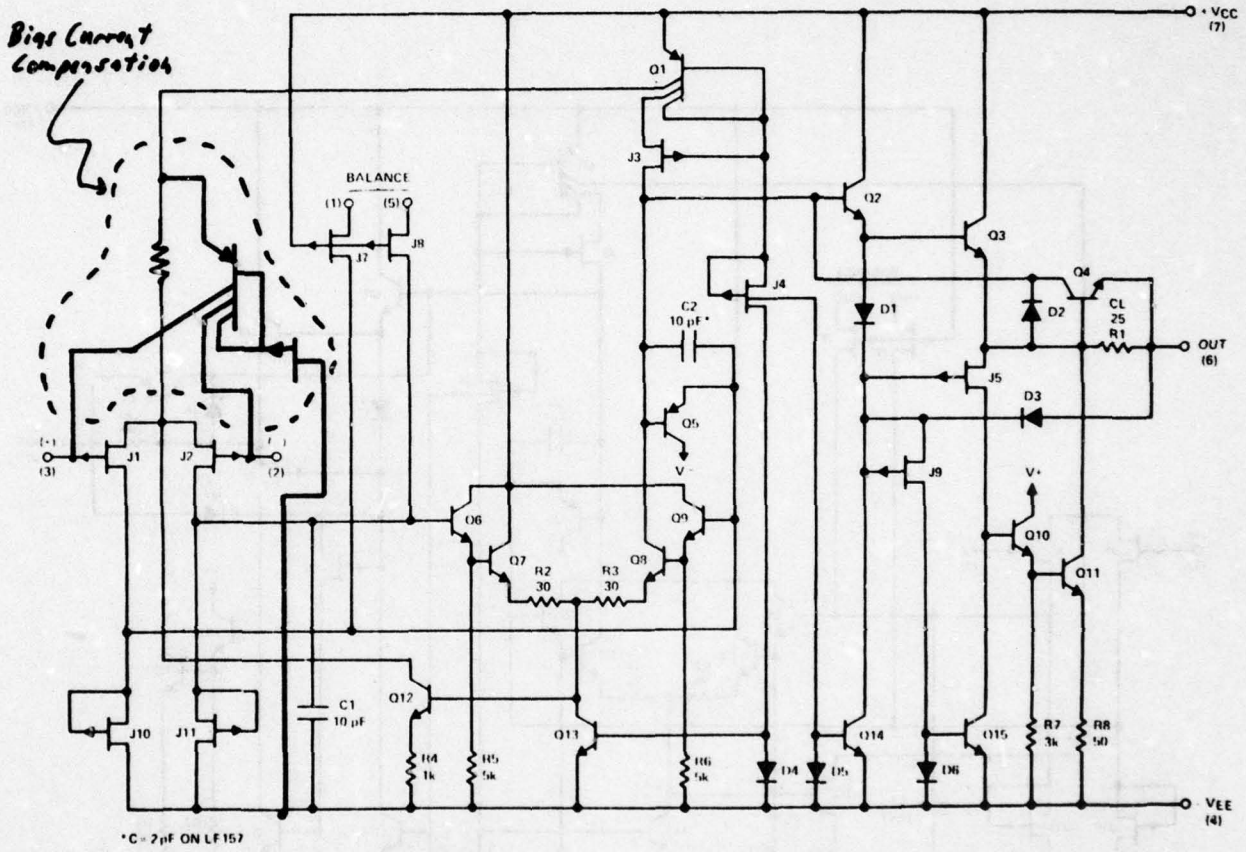
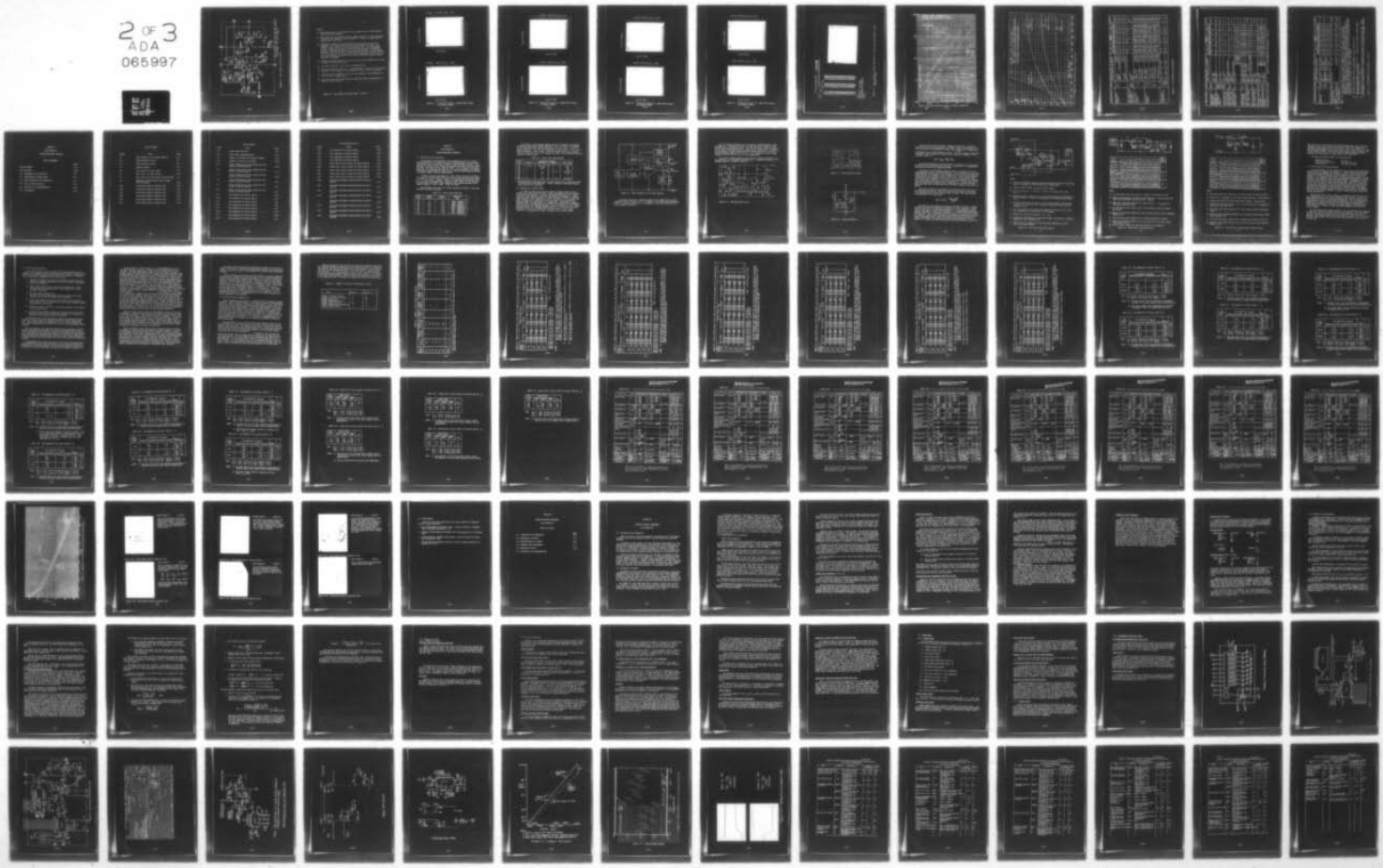
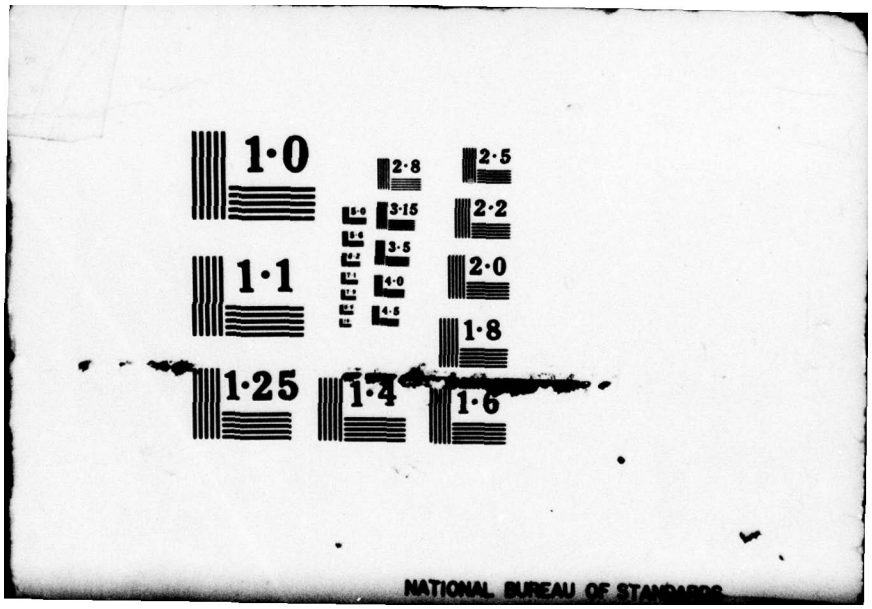


Figure 4-2. Bi-FET op amp with bias current compensation.

AD-A065 997 GENERAL ELECTRIC CO PITTSFIELD MASS ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF LINEAR INTEGRATED CIRCUITS,(U)
JAN 79 J KULPINSKI, T SIMONSEN, R PASKOWSKY F30602-77-C-0153
UNCLASSIFIED RADC-TR-78-275 NL

2 OF 3
ADA
065997




1·0
1·1
1·25
2·8
3·15
3·5
4·0
4·5
1·4
2·5
2·2
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1·8
1·6
NATIONAL BUREAU OF STANDARDS

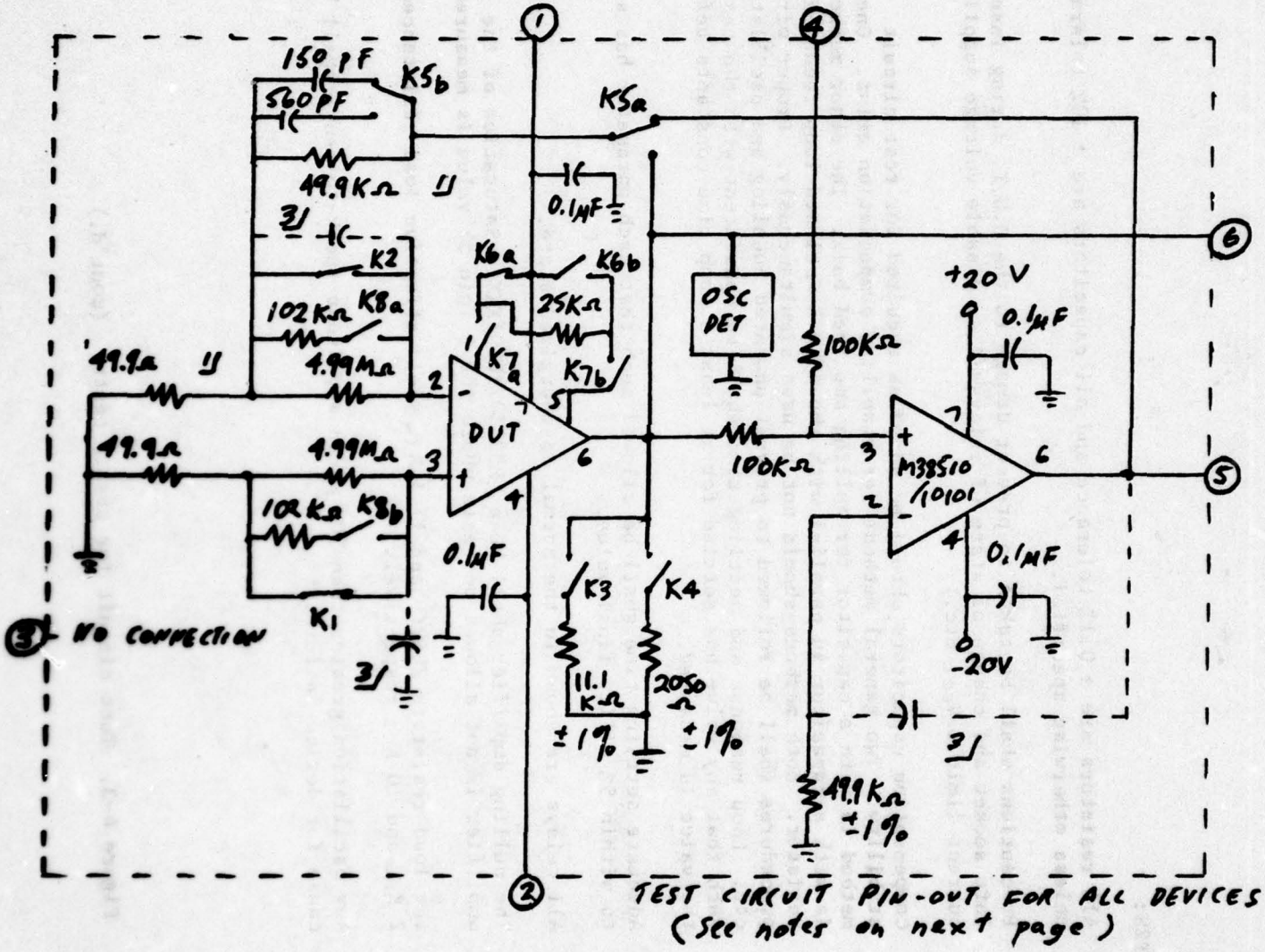


Figure 4-3. Test circuit for static tests.

NOTES:

1/ All resistors are ± 0.1% tolerance and all capacitors are ± 10% tolerance unless otherwise specified.

2/ Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit ± V_{CC}, etc.)

3/ Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feed back. The other method is with a capacitor in parallel with the 49.9 KΩ closed loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.

4/ Adequate settling time shall be allowed such that each parameter has settled to within 5% of its final value.

5/ All relays are shown in the normal de-energized state.

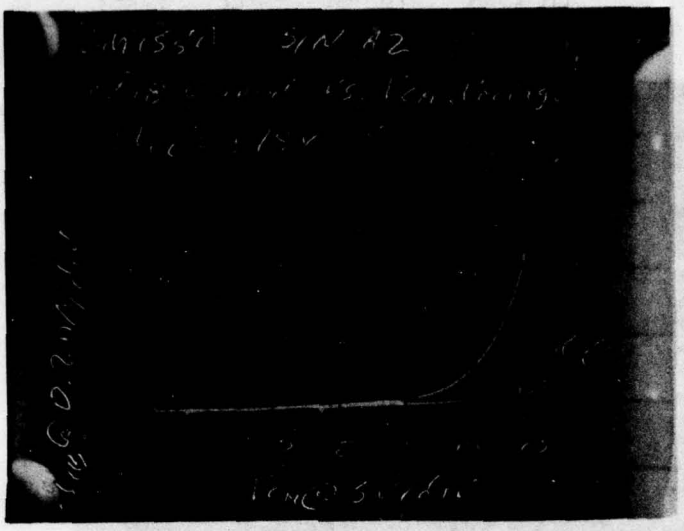
6/ The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (pin 5) value is measured.

7/ The load resistors 2050Ω and 11.1 KΩ yield effective load resistances of 2 KΩ and 10 KΩ respectively.

8/ Any oscillation greater than 300 mV in amplitude (peak-to-peak) shall be a cause for device failure.

Figure 4-3. Test circuit for static tests. (cont'd.)

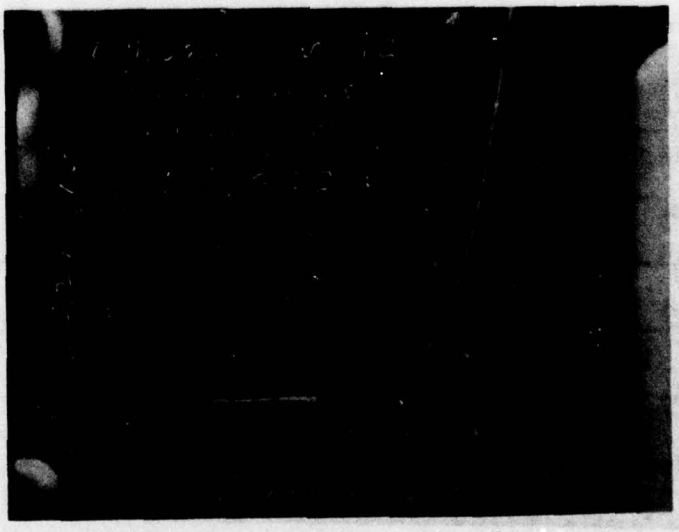
LM 155A S/N A2 @ ± V_{cc} = ± 15V



+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5V/div

LM 155A S/N A2 @ ± V_{cc} = ± 20V

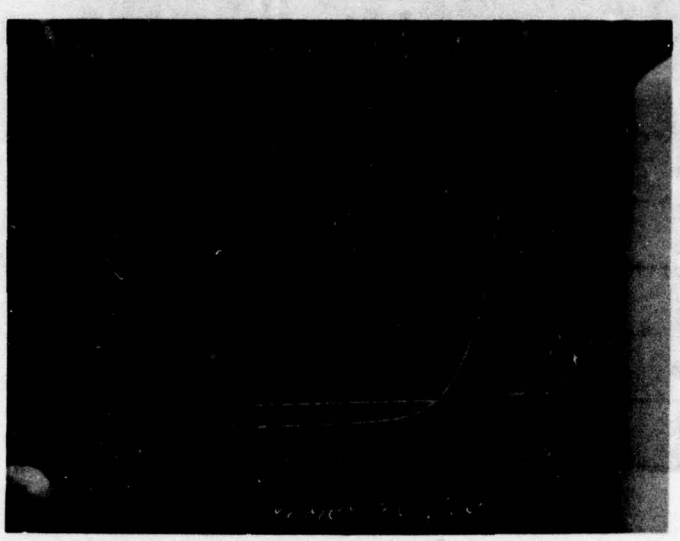


+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5V/div

Figure 4-4. Bi-FET bias current vs common mode voltage and supply voltage.

LM 155A S/N B2 @ ± V_{cc} = ± 15V



+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5 V/div

LM 155A S/N B2 @ ± V_{cc} = ± 20V

+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5 V/div

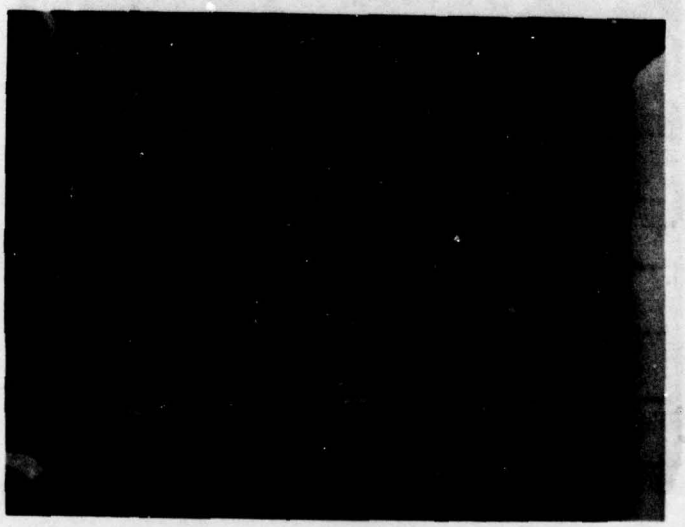
Figure 4-5. Bi-FET bias current vs. common mode voltage and supply voltage.

LM 155 S/N C2 @ ± V_{cc} = ± 15V

+ I_{iB} @ 0.2 nA/div

V_{cm} @ 5 V/div

LM 155 S/N C2 @ ± V_{cc} = ± 20V



+ I_{iB} @ 0.2 nA/div

V_{cm} @ 5 V/div

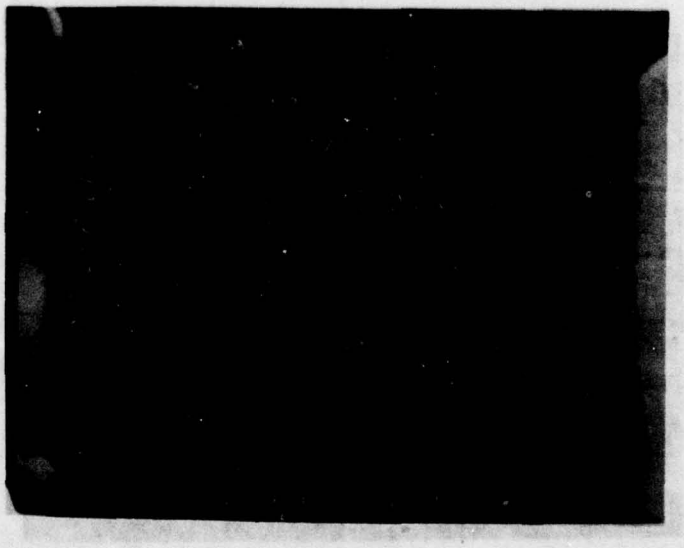
Figure 4-6. Bi-FET bias current vs. common mode voltage and supply voltage.

LM 157 S/N K2 @ ± V_{cc} = ± 15V

+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5 V/div

LM 157 S/N K2 @ ± V_{cc} = ± 20V



+ I_{IB} @ 0.2 nA/div

V_{cm} @ 5 V/div

Figure 4-7. Bi-FET bias current vs. common mode voltage and supply voltage.

0 DEVICES HAVE BEEN TESTED, 0 DEVICES PASSED
0 DEVICES FAILED

30 AUG 78 10:02:16PASSED THE SOCKET BOARD KEYING TEST

REL-V VOLTAGE = 10.24

VCM	PIIB	NIIB
-15.00	5.407M	13.29M
-14.00	15.26M	16.36M
-13.00	16.67M	17.50M
-12.00	17.71M	18.53M
-11.00	19.23M	18.77M
-10.00	21.36M	20.94M
-9.000	21.43M	21.32M
-8.000	21.67M	22.17M
-7.000	24.05M	23.94M
-6.000	25.72M	24.49M
-5.000	25.41M	24.74M
-4.000	26.21M	25.71M
-3.000	27.56M	27.76M
-2.000	29.12M	29.27M
-1.000	29.73M	30.29M
0.000	33.10M	32.46M
1.000	35.77M	36.10M
2.000	40.47M	40.75M
3.000	48.68M	49.98M
4.000	60.67M	61.63M
5.000	75.48M	76.79M
6.000	101.4M	101.5M
7.000	136.1M	136.9M
8.000	122.7M	184.3M
9.000	249.3M	250.7M
10.00	343.0M	341.3M
11.00	462.8M	462.1M
12.00	626.1M	625.0M
13.00	840.6M	840.2M
14.00	1.122	1.119
15.00	1.483	1.482

PASSED

TEST RUNTIME= 107.6 SECONDS

THIS DATA WAS RUN AT 10:05:04 ON

30 AUG 78

Figure 4-8. Test correlation between Tektronix 577 curve tracer and Tektronix S-3260 automatic tester.

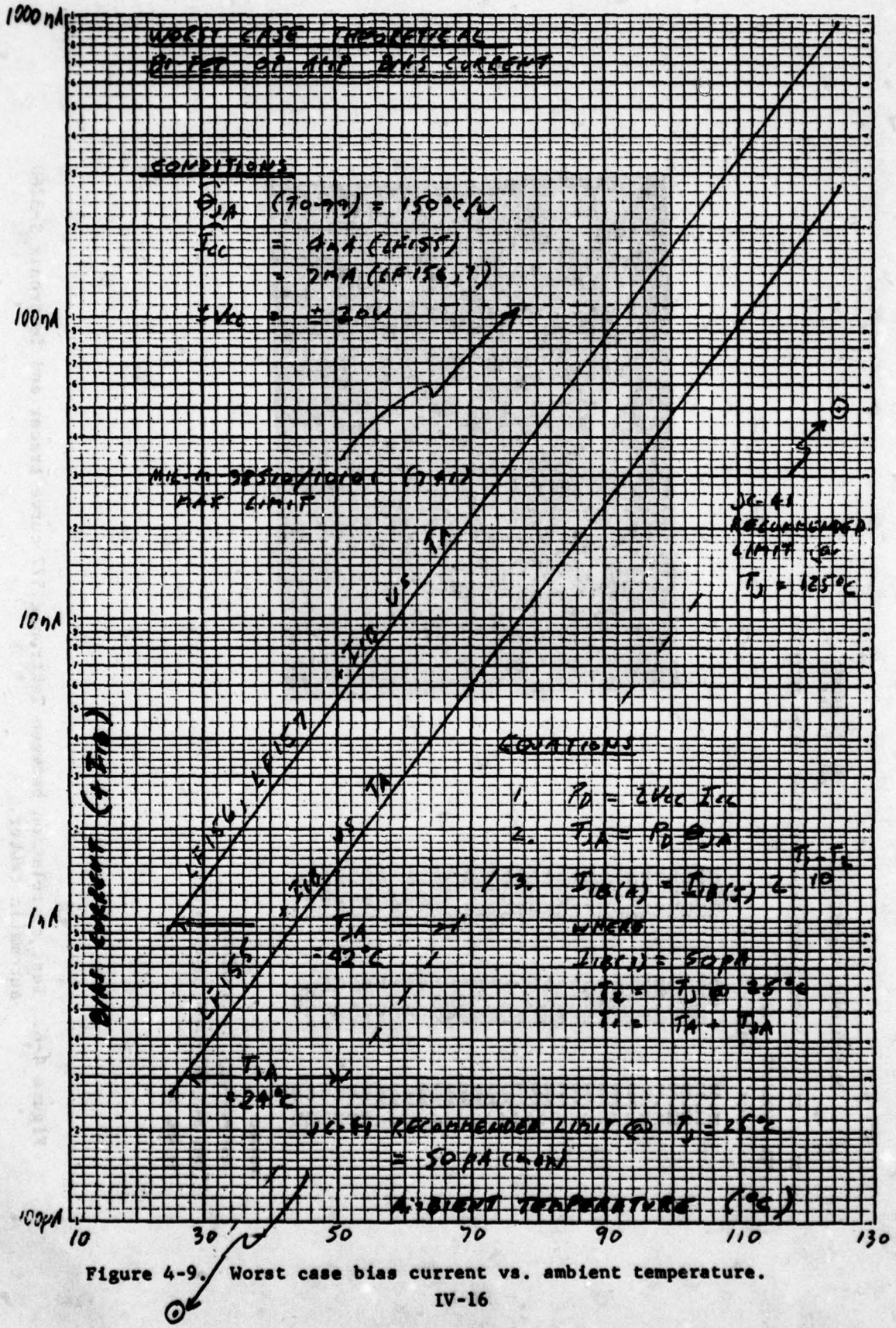


Figure 4-9. Worst case bias current vs. ambient temperature.

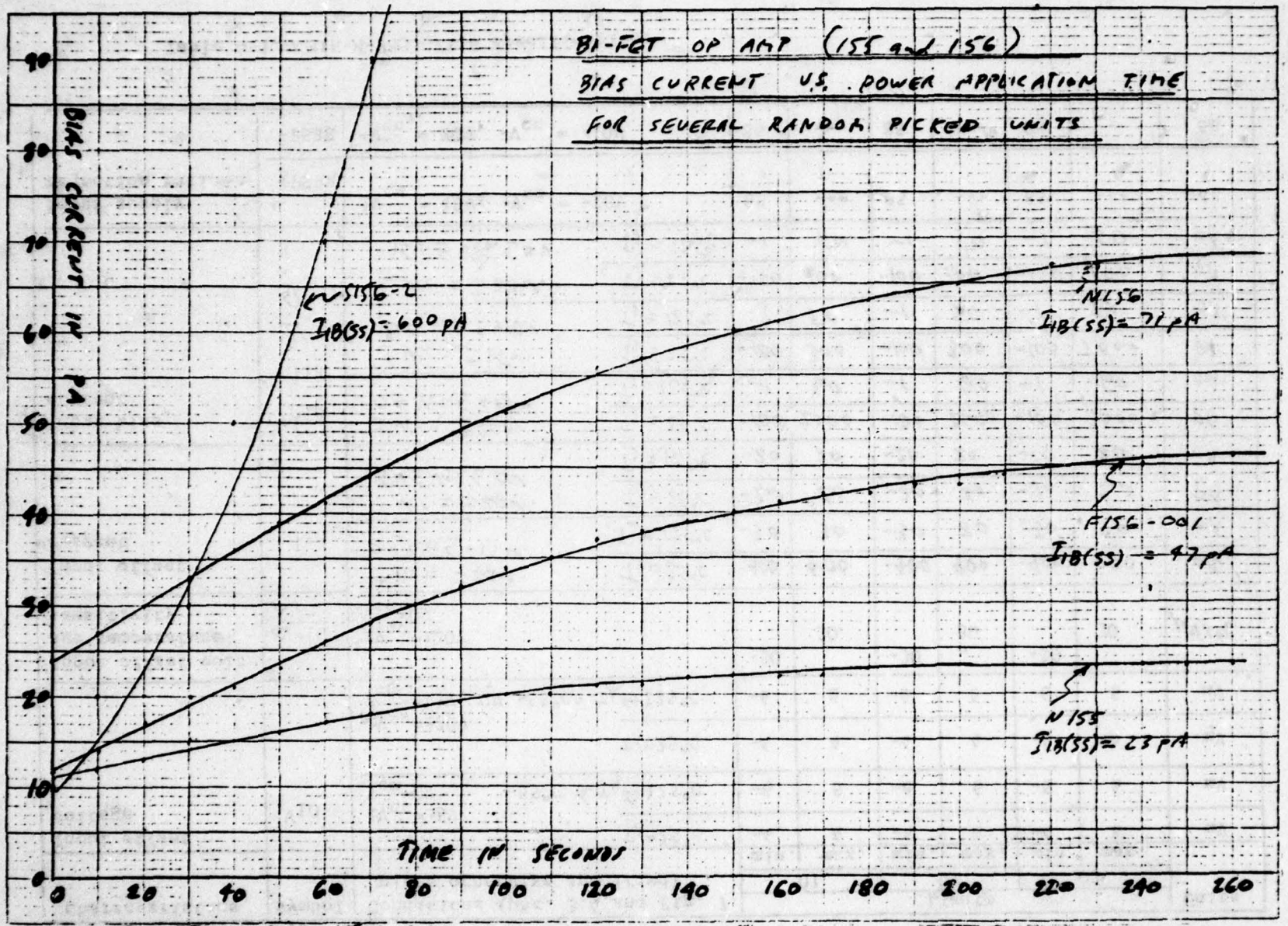


Figure 4-10. Typical bias current vs. warm-up time.

Characteristics	Symbol	Conditions (par. 3.4 and Fig. 7 unless otherwise specified)		Limits						Units
				01		02		03		
				min.	max.	min.	max.	min	max.	
Input offset voltage	V_{IO}		T_A=25°C	-4	4	-4	4	-4	4	mV
		$\pm V_{cc}$=±5V, V_{cm}=0V	-55°C ≤ T_A ≤+125°C	-6	6	-6	6	-6	6	mV
		$\pm V_{cc}$=±20V, V_{cm}=±15V, 0V	T_A=25°C	-4	4	-4	4	-4	4	mV
			-55°C ≤ T_A ≤+125°C	-6	6	-6	6	-6	6	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{cc}$=±20V, V_{cm}=0V		-30	30	-30	30	-30	30	µV/°C
Input offset current	I_{IO}	$\pm V_{cc}$ = ±20V, 0 ≤ V_{cm} ≤ +15V	T_J = 25°C	-400	400	-400	400	-400	400	pA
			T_J = 125°C	-30	30	-30	30	-30	30	nA
		$\pm V_{cc}$ = ±20V, -15V ≤ V_{cm} ≤ 0V	T_J = 25°C	-20	20	-20	20	-20	20	pA
			T_J = 125°C	-20	20	-20	20	-20	20	nA
Input bias current	$+I_{IB}$, $-I_{IB}$ 1/, 5/	$\pm V_{cc}$ = ±20V, 0 ≤ V_{cm} ≤ +15V	T_J = 25°C	-100	2000	-100	2000	-100	2000	pA
			T_J = 125°C	-1	60	-1	60	-1	60	nA
		$\pm V_{cc}$ = ±15V, 0 ≤ V_{cm} ≤ +10V	T_J = 25°C	-100	300	-100	300	-100	700	pA
			T_J = 125°C	-1	50	-1	50	-1	50	nA
		$\pm V_{cc}$ = ±20V, -15V ≤ V_{cm} ≤ 0V	T_J = 25°C	-100	100	-100	100	-100	100	pA
			T_J = 125°C	-1	50	-1	50	-1	50	nA
Power supply rejection ratio	+PSRR	$+V_{cc}$ = 10V, $-V_{cc}$ = -20V		85	---	85	---	85	---	dB
	-PSRR	$+V_{cc}$ = 20V, $-V_{cc}$ = -10V		85	---	85	---	85	---	dB

Table 4-1. MIL-M-38510/114 specification.

Characteristics	Symbol	Conditions (par. 3.4 and Fig. 7 unless otherwise specified)		Limits						Units
				01		02		03		
				min.	max.	min.	max.	min.	max.	
Input voltage common mode rejection 2/	CMR	$\pm V_{cc}$ = 20V V_{IN} = ±15V		85	---	85	---	85	---	dB
Adjustment for input offset voltage	V_{IO} ADJ(+)	$\pm V_{cc}$ = 20V		+8	---	+8	---	+8	---	mV
	V_{IO} ADJ(-)	$\pm V_{cc}$ = 20V		---	-8	---	-8	---	-8	mV
Output short circuit current (for positive output) 3/	$I_{OS}(+)$	$\pm V_{cc}$ = ±15V t ≤ 25 mS (Short circuit to ground)		-60	---	-60	---	-60	---	mA
Output short circuit current (for negative output) 3/	$I_{OS}(-)$	$\pm V_{cc}$ = ±15V t ≤ 25 mS (Short circuit to ground)		---	60	---	60	---	60	mA
Supply current	I_{cc}	$\pm V_{cc}$ = ±15V	T_A = -55°C	---	6	---	11	---	11	mA
			T_A = +25°C	---	4	---	7	---	7	
			T_A = +125°C	---	4	---	7	---	7	
Output Voltage swing (maximum)	V_{OP}	$\pm V_{cc}$ = 20V, R_L = 10 KΩ		±16	---	±16	---	±16	---	V
		$\pm V_{cc}$ = 20V, R_L = 2 KΩ		±15	---	±15	---	±15	---	
Open loop voltage gain (single ended) 4/	$A_{vs}(\pm)$	$\pm V_{cc}$ = 20V R_L=2 KΩ V_{OUT} = ±15V	T_A = 25°C	50	---	50	---	50	---	V/mV
			-55°C ≤ T_A ≤ +125°C	25	---	25	---	25	---	
Open loop voltage gain (single ended) 4/	A_{vs}	$\pm V_{cc}$ = 5V R_L = 2 KΩ V_{OUT} = ± 2V		10	---	10	---	10	---	V/mV
Transient response Rise time	$TR_{(tr)}$	$\pm V_{cc}$ = ±15V R_L = 2 KΩ C_L = 100 pf see Figure 8	AV=1	---	300	---	200	---	---	ns
			AV=5	---	---	---	---	---	400	
Transient response Overshoot	$TR_{(os)}$		AV=1	---	40	---	40	---	---	%
			AV=5	---	---	---	---	---	25	

See footnotes at end of table.

Table 4-1. MIL-M-38510/114 specification. (cont'd.)

Characteristics	Symbol	Conditions (par. 3.4 and Fig. 7 unless otherwise specified)	Limits						Units
			01		02		03		
			min.	max.	min.	max.	min.	max.	
Slew rate	SR(+) and SR(-)	V_{IN} = ±5V; AV = 1; See Fig. 8; 25°C ≤ T_A ≤ 125°C	2	---	7.5	---	---	---	V/us
		V_{IN} = ±5V; AV = 1; See Fig. 8; T_A = -55°C	1	---	5	---	---	---	V/us
		V_{IN} = ±5V; AV = 5; See Fig. 8; 25°C ≤ T_A ≤ 125°C	---	---	---	---	30	---	V/us
		V_{IN} = ±5V; AV = 5; See Fig. 8; T_A = -55°C	---	---	---	---	20	---	V/us
Noise (referred to input) Broadband	N_I(BB)	±V_{cc} = 20 V; T_A = 25°C	---	10	---	10	---	10	uV_{rms}
Noise (referrred to input) Popcorn	N_I(PC)	T_A = 25°C	---	40	---	40	---	40	uV_{pk}

NOTES: 1/ Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 msec after power is first applied to the device for test. Measurement at T_A = -55°C is not necessary since expected values are too small for typical test systems.

2/ CMR shall be calculated from V_{IO} measurements at V_{CM} = +15V and -15V.

3/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175°C$.

4/ Open loop gain is not guaranteed to be linear or positve over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

Table 4-1. MIL-M-38510/114 specification. (cont'd.)

SECTION V

MIL-M-38510/115

VOLTAGE REGULATORS, NEGATIVE

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SECTION V

MIL-M-38510/115

VOLTAGE REGULATORS, NEGATIVE

5.1 Background and Introduction

The acceptance and popularity of the Integrated Circuit (+ 5 volt) Voltage Regulator has prompted the design and manufacture of both positive and negative fixed output three-terminal voltage regulator families. The families of positive fixed output voltage regulators chosen for MIL-M-38510/107A were the LM140K, LM141H, 7800 and 78M00. It was decided by the manufacturers, the government and GEOS that as a natural outgrowth, the negative fixed output voltage regulator specification should include regulators from the LM120K, LM120H, 7900 and 79M00 families.

A survey of power requirements for linear devices and data converters (i.e. A/D and D/A converters) indicates that all such devices require either ± 15 VDC or ± 12 VDC. A similar survey of microprocessors indicated a need for a - 5 VDC voltage regulator. Therefore, GEOS agrees with the decision to characterize and specify fixed negative output voltage regulators with output voltages of -5VDC, -12VDC, -15VDC and -24Vdc.

The following table shows the voltage regulators included in this specification from these families:

TABLE 5.1: Device Types Specified

Device Type	Output Voltage, V	Output Current, A	Commercial Type
01	- 5	- 0.5	79M05, LM120H-5.0
02	-12	- 0.5	79M12, LM120H-12
03	-15	- 0.5	79M15, LM120H-15
04	-24	- 0.5	79M24, LM120H-24
05	- 5	- 1.0	7905 , LM120K-5.0
06	-12	- 1.0	7912 , LM120K-12
07	-15	- 1.0	7915 , LM120K-15
08	-24	- 1.0	7924 , LM120K-24

As a result of the observed design similarity throughout the families of positive fixed output voltage regulators, and in an effort to economize on the characterization effort small sample sizes were used. For the 1.0 ampere regulators, the -5VDC and -24VDC devices were obtained. For the 1/2 ampere regulators, -5VDC, -12VDC, -15VDC and -24VDC devices were obtained. The total quantities of the test samples indicated in the following table were supplied to GEOS by RADC.

TABLE 5.2: Device Types Characterized

Device Type	Quantity of Devices			
	Vendor A	Date Codes	Vendor B	Date Codes
01	4 + 4*	704, 806	4	642
02	4	626	2	712
03	-	-	2	516
04	-	-	4 + 3*	543, 632
05	4	648	3	619
06	-	-	-	-
07	-	-	-	-
08	4	725	3 + 2*	628, 816

* GEOS purchased 4 additional units of device type 01 and 3 additional units of device type 04 for evaluation. Vendor B shipped 2 additional units of device type 08 for evaluation.

5.2 Description of Device Types

The 7900 and LM120 three-terminal negative voltage regulators have designs with enough similarity that a common specification can be developed to describe both families. Although some design differences exist, both negative voltage families contain the same functional elements. A general block diagram of these regulators is shown in Figure 5.1. The voltage regulator consists of a) a start-up circuit to ensure that the device is rapidly brought into regulation, b) a temperature - compensated voltage reference, plus a current source to eliminate the effect of the unregulated input voltage on the reference voltage, c) an error amplifier, d) a current limiting circuit, e) a thermal shutdown circuit, f) a safe operating area protection circuit, g) a series pass transistor and h) laser trimmed resistors to factory-set the output voltage and peak output current.

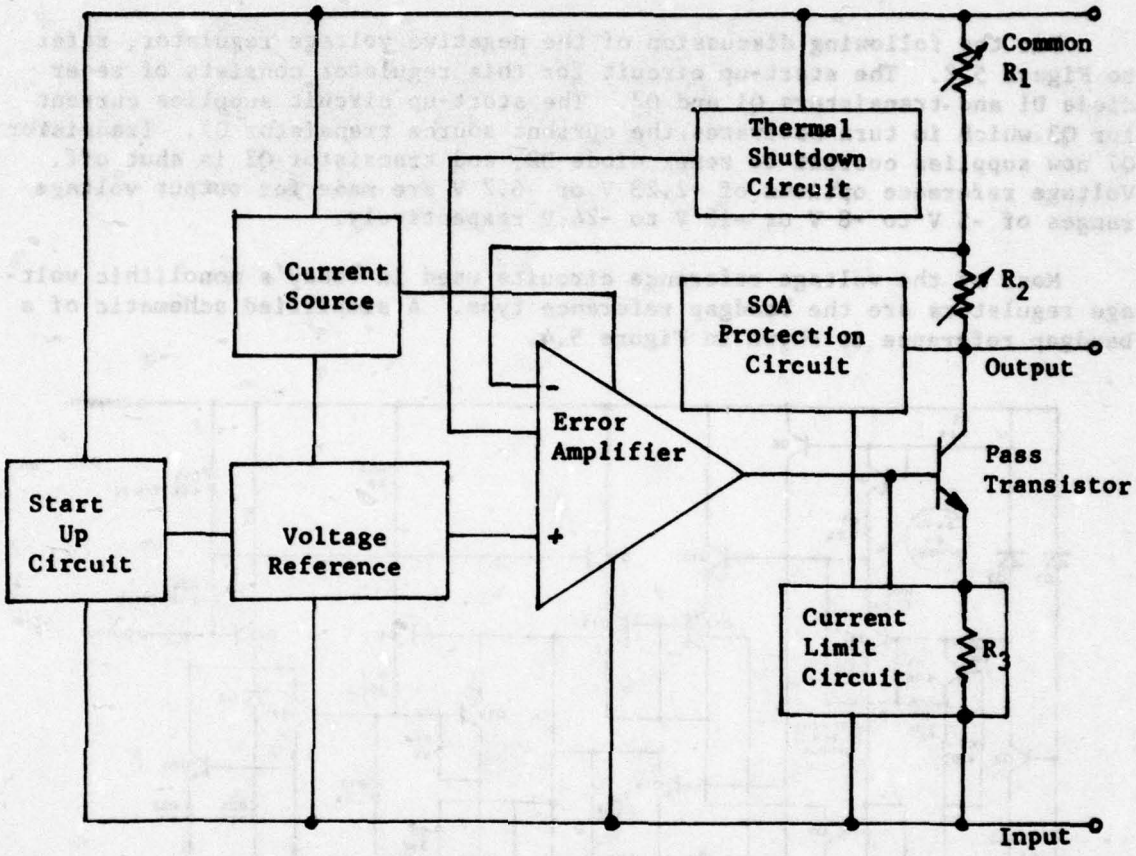


Figure 5.1. Block diagram of the voltage regulator

A detailed discussion of regulator theory can be found in any of the references listed in section 5.6. A schematic of the 7900 series equivalent circuit is shown in Figure 5.2 and a schematic of the LM120 equivalent circuit is shown in Figure 5.3.

For the following discussion of the negative voltage regulator, refer to Figure 5.2. The start-up circuit for this regulator consists of zener diode D1 and transistors Q1 and Q2. The start-up circuit supplies current for Q3 which in turn activates the current source transistor Q7. Transistor Q7 now supplies current to zener diode D2, and transistor Q2 is shut off. Voltage reference options of -2.23 V or -6.2 V are made for output voltage ranges of -5 V to -8 V or -12 V to -24 V respectively.

Most of the voltage reference circuits used in today's monolithic voltage regulators are the bandgap reference type. A simplified schematic of a bandgap reference is shown in Figure 5.4.

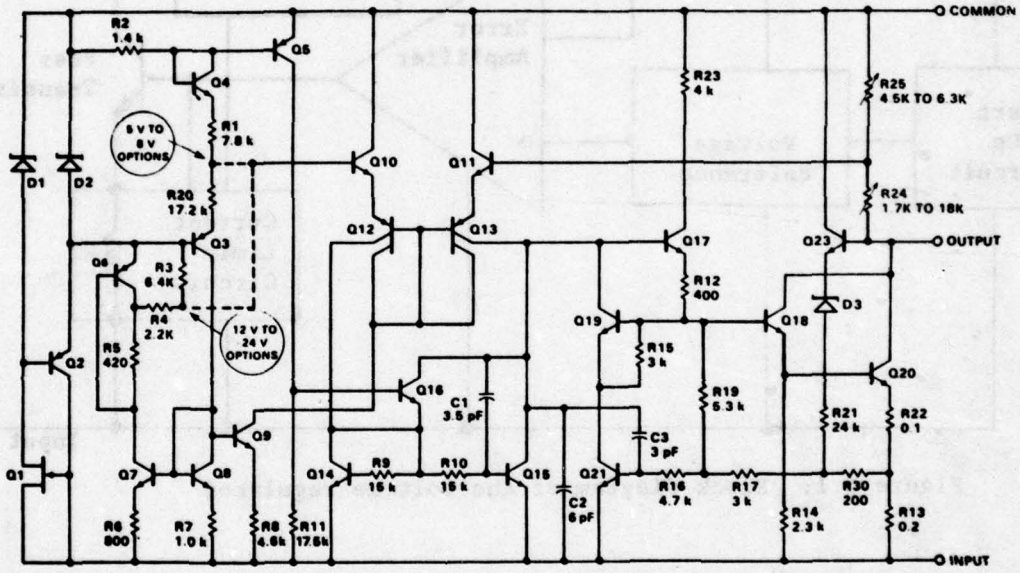


Figure 5.2. 7900 Equivalent circuit

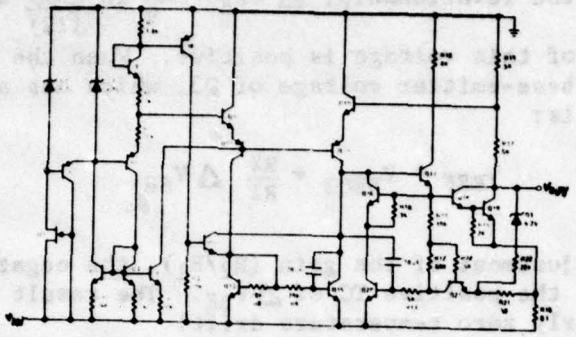


Figure 5.3. LM120 Equivalent circuit

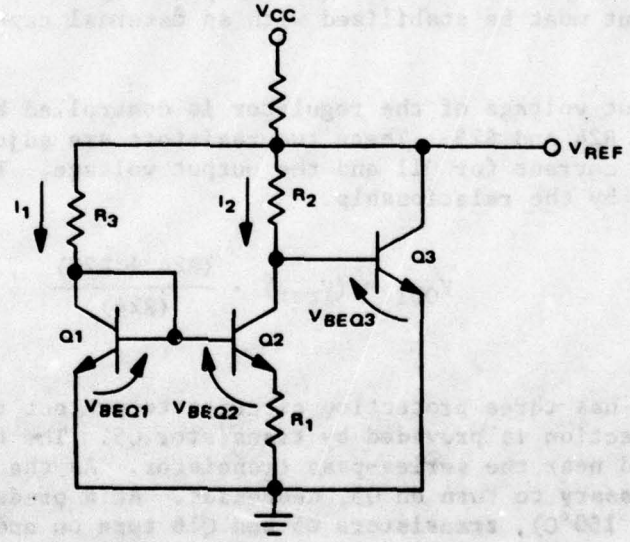


Figure 5.4. Bandgap reference

In this circuit, two monolithic transistors operating at different collector current densities develop a voltage, ΔV_{BE}, at the emitter of Q2. This voltage has the relationship: $\Delta V_{BE} = \frac{KT}{q} \ln \frac{(I1)}{(I2)}$ and the temperature coefficient (TC) of this voltage is positive. When the voltage is amplified and added to the base-emitter voltage of Q3, which has a negative TC, the resultant output is:

$$V_{REF} = V_{BEQ3} + \frac{R2}{R1} \Delta V_{BE}.$$

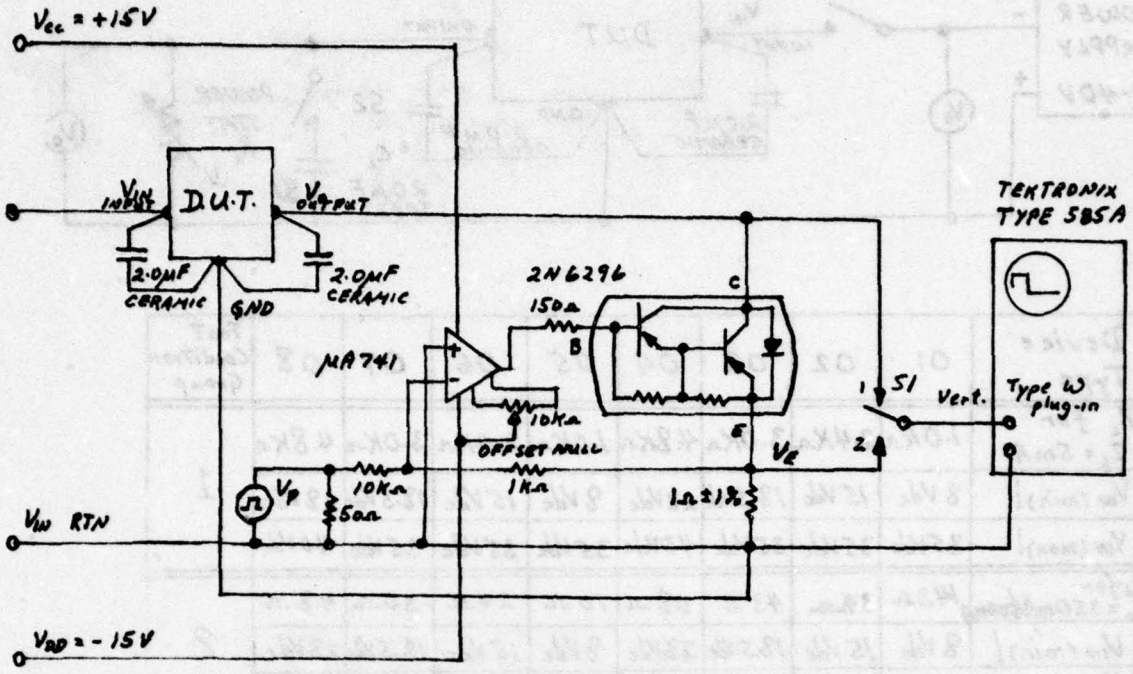
By proper adjustment of the gain (R_2/R_1), the negative TC of V_{BEQ3} can be made to cancel the positive TC of ΔV_{BE}. The result is a voltage reference that has nearly zero temperature drift.

In Figure 5.2, the bandgap reference voltage is coupled to the non-inverting input (Q10) of the error amplifier. The error amplifier consisting of transistors Q10 through Q13 also receives its bias from the voltage reference circuit via transistor, Q9 and resistor R8. Output voltage feedback is coupled from the feedback network of R24 & R25 to the inverting input (Q11) of the error amplifier. The output of the error amplifier is coupled to the series-pass transistor Q20 via transistors Q17, Q18 and resistor R12. Since the series-pass transistor Q20 is operating in an emitter follower mode the output must be stabilized with an external capacitor from output to ground.

The output voltage of the regulator is controlled by the ratio of the two resistors R24 and R25. These two resistors are adjusted to optimize both the bias current for Q11 and the output voltage. The output voltage is determined by the relationship:

$$V_{OUT} = (V_{ref}) \cdot \frac{(R24 + R25)}{(R24)}$$

The 7900 has three protection circuits to protect the device. Thermal overload protection is provided by transistor Q5. The transistor is physically located near the series-pass transistor. As the temperature rises, the V_{BE}, necessary to turn on Q5, decreases. At a predetermined temperature (greater than 150°C), transistors Q5 and Q16 turn on and the current to Q17 is turned off. Short circuit protection is provided by detecting the current flow through resistor R13. When the voltage drop across R13 rises sufficiently, transistors Q19 and Q21 will turn on and the current to Q17 is turned off. Finally, the safe operating area protection circuit, made up of



NOTES:

1/ Adjust the frequency, amplitude and pulse width of the pulse voltage (V_p) equal to 200 pps, 1.0 volts and 100 usec, respectively.

2/ Apply an input voltage, $V_{in(min)} \leq V_{in} \leq V_{in(max)}$.

3/ Set S1 to position 2. With $V_p = 0$, adjust the offset null so that $V_E = 0$.

4/ Adjust the pulse voltage (V_p) so that the voltage pulse (V_E) measured on the oscilloscope, is equal to the magnitude of the desired load current (I_L).

5/ Set the oscilloscope time base to view the 100 us pulse. Set the type W plug-in for a vertical input attenuator setting of 2 mV/cm and the display for A-V_c.

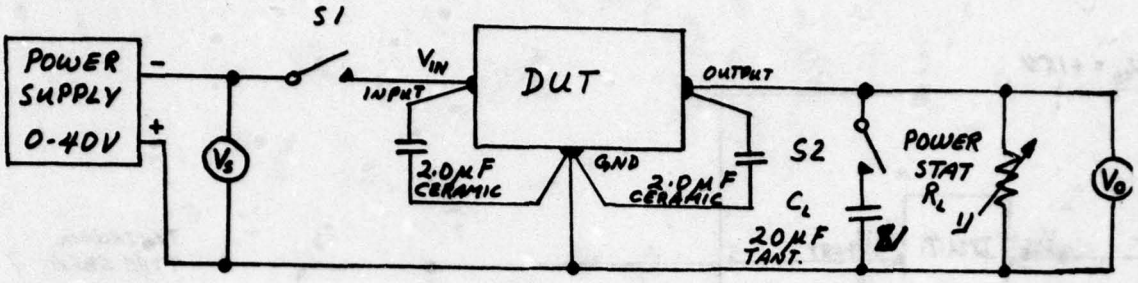
6/ Set S1 to position 1 and adjust the comparison voltage (V_c) for a zero volt reading 50 usec from the start of the sweep.

7/ Measure and record the voltage V_c. ($V_o = -V_c$).

8/ Observe the oscilloscope for any unusual spikes, oscillations, overshoot, undershoot, droop, blooming, etc.

9/ Repeat setps 4/ through 8/ for each specified combination of load current and input voltage.

Figure 5.5. Test Circuit for Static Tests.



Device Type	01	02	03	04	05	06	07	08	Test Condition Group
R_L for I_L = 5mA	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	35Vdc	35Vdc	35Vdc	40Vdc	35Vdc	35Vdc	35Vdc	40Vdc	
R_L for I_L = 350mA/500mA	14.3Ω	34Ω	43Ω	68Ω	10Ω	24Ω	30Ω	48Ω	2
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	25Vdc	32Vdc	35Vdc	40Vdc	25Vdc	32Vdc	35Vdc	40Vdc	
R_L for $I_L = I_{L(max)}$	10Ω	24Ω	30Ω	48Ω	5Ω	12Ω	15Ω	24Ω	3
$\|V_{IN(min)}\|$	8 Vdc	15Vdc	18.5Vdc	28Vdc	8 Vdc	15Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	20Vdc	27Vdc	30 Vdc	38 Vdc	20Vdc	27Vdc	30Vdc	38 Vdc	

NOTES:

1/ For each device type, adjust R_L for a typical load current of 5 mA.

2/ Adjust $V_s = -|V_{in(min)}|$ for the device type under test. Close switch S1 and observe that the proper voltage is at V_o. Open S1.

3/ Repeat the conditions defined in 1/ and 2/ with $V_s = -|V_{in(max)}|$ for each device type under test.

4/ For each device type, adjust R_L for a load current of 350 mA or 500 mA per Group 2.

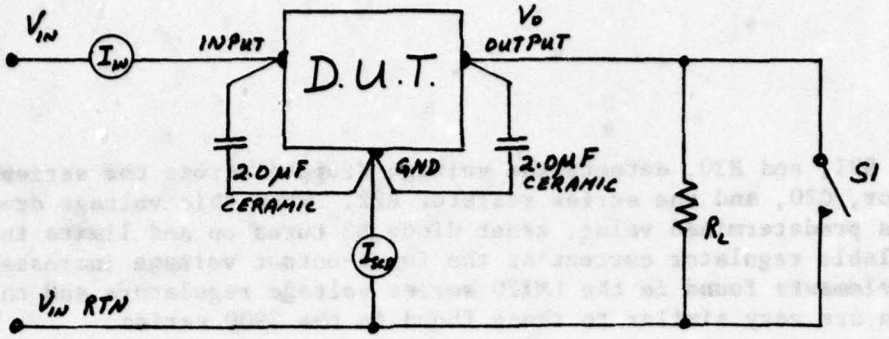
5/ Repeat the conditions defined in 2/ and 3/ with the load current conditions defined in 4/.

6/ For each device type, adjust R_L for a typical maximum load current.

7/ Repeat the conditions defined in 2/ and 3/ with the load current conditions defined in 6/.

8/ With S2 closed, repeat the conditions defined in 1/ through 7/.

Figure 5.6. Test circuit for start-up test.



Device Type	01	02	03	04	05	06	07	08	Test Condition Group
R_L for I_L = 5mA	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	35Vdc	35Vdc	35Vdc	40Vdc	35Vdc	35Vdc	35Vdc	40Vdc	
R_L for I_L = 350mA/500mA	14.3Ω	34Ω	43Ω	68Ω	10Ω	24Ω	30Ω	48Ω	2
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	25Vdc	32Vdc	35Vdc	40Vdc	25Vdc	32Vdc	35Vdc	40Vdc	
R_L for $I_L = I_{L(max)}$	10Ω	24Ω	30Ω	48Ω	5Ω	12Ω	15Ω	24Ω	3
$\|V_{IN(min)}\|$	8 Vdc	15Vdc	18.5Vdc	28Vdc	8 Vdc	15Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	20Vdc	27Vdc	30 Vdc	38Vdc	20Vdc	27Vdc	30Vdc	38 Vdc	

NOTES:

1/ For each device type, adjust R_L for a load current of 5 mA per Group 1.

2/ Adjust $V_{in} = -|V_{in(min)}|$ for the device type under test. Close switch S1.

3/ Measure and record the output short circuit current. ($I_{os}=I_{in}-I_{scd}$)

4/ Repeat the conditions defined in 1/, 2/ and 3/ with $V_{in} = -|V_{in(max)}|$ for each device type under test.

5/ For each device type, adjust R_2 for a load current of 350 or 500 mA per Group 2.

6/ Repeat the test conditions defined in 2/, 3/ and 4/ with the load conditions defined in 5/.

7/ For each device type, adjust R_L for a maximum load current per Group 3.

8/ Repeat the conditions defined in 2/, 3/ and 4/ with the load conditions defined in 7/.

Figure 5.7. Test circuit for output short circuit current.

Q23, D3, R21, and R30, detects the voltage dropped across the series pass transistor, Q20, and the series resistor R22. When this voltage drop exceeds a predetermined value, zener diode D3 turns on and limits the maximum available regulator current as the input-output voltage increases. The circuit elements found in the LM120 series voltage regulators and their operation are very similar to those found in the 7900 series.

The major protective elements in this design are:

Thermal shutdown	- Q8, Q13
Short circuit protection	- Q16, Q20, Q21, R16
SOA protection	- D3, R20, R21, R16

5.3 Test Circuits and Test Procedures

The test circuits and test procedures used during the characterization study are shown in Figures 5.5 through 5.7. These circuits are bench type setups using non-automatic test equipment; however, equivalents of these circuits are readily programmed into an automatic tester. In order to achieve ± 1 mV accuracy for the output voltage (V_{out}) measurements, nulling techniques were employed using the voltage comparator available in the Type W plug-in of the Tektronix Type 585A oscilloscope. Measurements of both the load current and the output voltage were made using this nulling technique. The two sockets used for the acceptance of both the T03 cases and the T039 cases were wired in parallel and the regulator input and output capacitors were soldered to the terminals on the T03 socket. The measurement probe was connected directly to either the precision one ohm resistor leads or the DUT socket terminals in order to ensure accurate current and voltage measurements.

The start-up test, shown in Figure 5.6, measures start-up under all of the extreme combinations of input voltage and load currents. The test is also performed with a 20 uF capacitor shunting the load to simulate distributed capacitors found in most system applications. The load resistance is obtained from a precision power resistor decade box and is preselected before power is applied to the DUT. The power supply is adjustable from 0 to 40 volts and is capable of supplying several amperes at any adjusted output voltage.

For the Output Short Circuit Test (Fig. 5.7), the ammeters were connected to read input current and standby current simultaneously. This was done to eliminate the meter resistance from the output circuit when the short is applied. The recorded value was the short circuit current ($I_{os} = I_{in} - I_{scd}$). The power supply used for this test is the same unit that is used in the startup test.

5.4 Device Characterization

The initial effort, prior to receipt of the characterization device samples, was to generate a base line specification similar in format to the one used for positive regulators based upon the JC41 Committee recommendations. Additional recommendations were later made to

a) tighten the standby current drain and standby current drain line regulation parameter requirements because the tighter requirements can be met by vendors

b) delete output short circuit current with minimum input voltage applied because the maximum input voltage condition is a more stringent requirement

c) move the ripple rejection test frequency to 2400 Hz because many military systems derive power from full wave rectified 3-phase 400 Hz generators

d) delete line voltage and load current transient tests because the large capacitors at the regulator input and output terminals negates the validity of these tests

e) delete the thermal coefficient tests because designs do not depend on this parameter and

f) incorporate the thermal transient test because this test is both a measure of quality of the chip bond to the case and a meansure of the device low frequency rejection capability.

A preliminary copy of the specification electrical peformance characteristics for device types 01 through 08 is shown in Tables 5.28 through 5.35. Test tables contain the recommendations of the JC41 Committee and also reflect recommendations arrived at as a result of device anomaly investigations.

The JC41 Committee also reported possible start-up problems on certain devices; GEOS evaluation therefore also included stringent start-up tests. Most of the remaining work effort on negative voltage regulators was devoted to the evaluation of device anomalies; such as, a) start-up and output short circuit current under different input voltage and load current conditions, b) emitter-follower type oscillations and c) hot socket insertion/ extraction failures.

A programmable test circuit was built to allow device testing as originally defined in the base line specification and to allow for additional investigation of device anomalies. The test circuit schematics and the test procedures for each test performed are shown and discussed in section 5.3.

Data was taken in a bench type set up at room temperature on all of the devices listed in Table 5.2, except for those devices shown with an asterisk. These data measurements began with the evaluation of output voltage (V_{out}) and output short circuit current (I_{os}) under different input voltage and load current conditions. Data taken on device types 01, 02, 03, 04, 05 and 08 has been tabulated in Tables 5.5 through 5.27. These tables show the calculated mean values of data taken on device type samples for specified conditions. In addition, the tables show the minimum and maximum values and their percentage below and above the corresponding mean values. The results show that the values are all well within the limits shown in Tables 5.28 through 5.35. However, data was taken only at room temperature (i.e. 25°C ± 5°C). A summary of the device failures and problems is shown in Table 5.3 and Table 5.4. The significant failures include device failures resulting from hot socket insertion/extraction and output short circuit current testing Additionally six of sixteen units dropped out of regulation in such a way that the output voltage began to track the input voltage. Outputs as high as -11.8 volts were observed from the -5.0 volt regulator and as high as -28 volts were observed from the -24 volt regulator. Data was taken on the three device type 05 failures to show when the devices stopped regulating as the input voltage and the output load current were simultaneously varied. Figure 5.8 shows the threshold level at which three devices go out of regulation versus input voltage and load current. Below and to the left of the curve the output voltage was within specification. Above and to the right of the curve the output voltage magnitude increased as the input voltage magnitude increased.

The output short circuit current failures shown in Table 5.3 were all catastrophic. Several of these devices were delidded and photos were taken of the destroyed devices. These photos are shown in Figures 5.9b and 5.9c. In each case, the pass transistor of the device was destroyed. An examination of Table 5.3, Table 5.4 and Tables 5.23 through 5.27 shows that a) these failures occurred primarily to device type 04 from vendor B and that b) in general, power dissipation during the output short circuit condition for all units was far in excess of the capability of a TO-39 case. Power dissipation was generally in excess of five watts.

Start-up problems on the other hand were observed chiefly in devices from vendor A. These problems were observed in device types 01, 05 and 08 as the magnitude of the input voltage was increased. For device type 01, the problem was observed when the magnitude of the input voltage was greater than 20-25 volts. For device type 05 and 08, the problem was observed when the magnitude of the input voltage was greater than 30-35 volts. Since devices could be started at voltages lower than those mentioned above, it was possible to first start the device sample and then increase the input voltage beyond the point where start up problems occur. Data tabulation in Table 5.5 through 5.27 was obtained in this manner, when necessary.

Hot socket insertion/extraction problems were observed in five device samples from vendor A. After experiencing these failures, this practice was stopped. The failure mode of the regulators was a partial short from input to output.

Emitter-follower type oscillations were observed on several regulators when the output terminals were decoupled with a 1.0 uF ceramic capacitor at various load conditions. However, the addition of an extra 1.0 uF ceramic capacitor eliminated these oscillations. Vendors of both the LM120 series regulators and the 7900 series regulators recommended different stabilizing capacitors at the output terminals of the two regulator types. Spec sheets for the 7900 series recommended either a 1 uF ceramic or a 1 uF solid tantalum capacitor at the output terminals of the regulator. Spec sheets for the LM120 series recommended either a 1 uF solid tantalum or a 25 uF aluminum electrolitic at the output terminals of the regulator The JC41 Committee has agreed on a recommendation of a 2.0 uF solid tantalum at the output terminals of the regulator.

5.5 Conclusions and Recommendations

Several anomalies were observed in characterization of negative voltage regulators. These anomalies appear to be related and should be investigated further in order to determine a satisfactory resolution. By far, one of the most serious failure modes observed during these investigations is the one in which the output voltage begins to track the input voltage. This anomaly occurs when the load currents at the output terminals of the regulator are less than 5 mA. Since these currents are not specified for negative regulators, this anomaly will not be picked up during test. A failure mode of this type could result in multiple system failures if overvoltage protection is not designed into the system. It is, therefore, recommended that the specification contain a caution note to indicate the possible existance of this failure mode.

The output short circuit current failure mode generally results in the total destruction of the pass transistor; and thus, an open circuit results between input and output. This failure mode results in system shut down but does not cause multiple system failures because of an over-voltage condition. The desired test time for testing this parameter is five seconds; however, this would make the costs prohibitive,

In addition, this test and the output peak current test are stress tests and should not be performed last in a test sequence. The JC41 Committee has recommended that these tests be performed prior to the start-up test, which will be performed last in the test sequence. The JC41 Committee will also recommend an adequate start-up test. In order to eliminate excessive heating of the device under test, the switch, used to initiate start-up, should be operated at a 2% duty cycle.

Ordnance Systems is of the opinion that the device anomalies associated with negative regulators contradict the MIL-M-38510 objective of reliability. The industry none-the-less has experienced a great demand for these devices, including military system applications, and reportedly few complaints have been received. It is also necessary to point out that the device problems uncovered during this characterization have not been verified by the industry at the time of this writing. Further evidence and negotiation is required at the committee level to determine the appropriate final corrective action.

TABLE 5.3. Summary of Failures and Problems by Vendor

Test	Vendor A	Vendor B
Number of Induced Failures	1	1
Number of Hot Socket Failures	5	N/A
Number failed V_{out}	2	4
Number destroyed during I_{os}	-	6
Number failed Start-up	12	1
Number dropped out of regulation	2	4
Number units oscillate	3	4

TABLE 5.4. Summary of test failures and problems.

Device Type	Total Tested	Number of Induced Failures	Number of Hot Socket Failures	Number Failed V_{out}	Number Destroyed During I_{os}	Number Failed Start-up	Number Dropped out Regulation	Number Oscil-lating	Number Passed Spec.
01	12*	2	4/ 4	-	-	7	-	-	3
02	6	-	N/A	-	1	-	-	1	5
03	2	-	N/A	-	-	-	-	-	2
04	7*	-	N/A	-	5	-	-	-	0
05	7	-	1/7	4	-	3	4	5	2
08	9	-	N/A	2	-	3	2	1	8
TOTAL	43	2	5	6	6	13	6	7	20

* Four of device type 01 and three of device type 04 units were checked for start-up failures and output short circuit current failures only.

Table 5.5. Output voltage (V_{out}) versus input voltage (V_{in}) and load current (I_L) for device type 01. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Value	Unit
	I_L = 5 mA	I_L = 50 mA	I_L = 350 mA	I_L = 500 mA		
- 8V	-5.011 (- .95%)	-5.007 (- .95%)	-5.007 (- .97%)	-5.005 (-1.49%)	Min	Volts
	-4.964	-4.959	-4.959	-4.931	Mean	
	-4.904 (+1.21%)	-4.890 (+1.39%)	-4.875 (+1.72%)	-4.851 (+1.63%)	Max	
-10V	-5.011 (- .91%)	-5.011 (- .97%)	-5.009 (-1.15%)	-5.006 (-1.47%)	Min	
	-4.966	-4.963	-4.952	-4.934	Mean	
	-4.905 (+1.23%)	-4.893 (+1.41%)	-4.877 (+1.51%)	-4.855 (+1.59%)	Max	
-20V	-5.014 (- .84%)	-5.016 (- .97%)	-5.015 (-1.25%)	-5.006 (-1.29%)	Min	
	-4.972	-4.968	-4.953	-4.942	Mean	
	-4.905 (+1.34%)	-4.905 (+1.27%)	-4.888 (+1.31%)	-4.862 (+1.63%)	Max	
-35V	-5.020 (- .86%)	-5.020 (- .99%)	-5.017 (- .64%)		Min	
	-4.977	-4.971	-4.985 2/	N/A 3/	Mean	
	-4.920 (+1.15%)	-4.906 (+1.3%)	-4.968 (+ .34%)		Max	

Min value of V_{out} for all readings = -5.020 Volts
Mean value of V_{out} for all readings = -4.959 Volts
Max value of V_{out} for all readings = -4.851 Volts

Spec: $-5.25V \leq V_{out} \leq -4.75V$

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value, based on six device samples from two manufacturers, of the output voltage, b) the maximum output voltage and the percentage above the mean and c) the minimum output voltage and the percentage below the mean.

2/ Only three samples continued to regulate the output voltage with V_i = -35V and I_L = 350 mA. This is an unspecified condition.

3/ None of the six samples continued to regulate the output voltage with V_i = -35V and I_L = 500mA. This is an unspecified condition.

TABLE 5-6. Output voltage (V_{out}) versus input voltage (V_{in}) and load current (I_L) for device type 02. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Value	Unit
	I_L = 5 mA	I_L = 50 mA	I_L = 350 mA	I_L = 500 mA		
-15V	-12.100 (- .85%)	-12.100 (- .92%)	-12.100 (-1.11%)	-12.070 (- .91%)	Min	Volts
	-11.998	-11.990	-11.967	-11.962	Mean	
	-11.872 (+1.05%)	-11.865 (+1.04%)	-11.825 (+1.18%)	-11.820 (+1.18%)	Max	
-17V	-12.110 (- .92%)	-12.100 (- .90%)	-12.100 (-1.08%)	-12.075 (- .90%)	Min	
	-12.000	-11.993	-11.971	-11.968	Mean	
	-11.875 (+1.04%)	-11.867 (+1.05%)	-11.837 (+1.12%)	-11.825 (+1.19%)	Max	
-27V	-12.110 (- .93%)	-12.110 (- .96%)	-12.110 (-1.12%)	-12.080 (- .90%)	Min	
	-11.998	-11.995	-11.976	-11.972	Mean	
	-11.877 (+1.01%)	-11.868 (+1.06%)	-11.840 (+1.13%)	-11.830 (+1.18%)	Max	
-32V	-12.110 (- .92%)	-12.110 (- .93%)	-1.2110 (-1.09%)	-12.080 (-1.06%)	Min	
	-11.999	-11.998	-11.979	-11.953	Mean	
	-11.875 (+1.04%)	-11.868 (+1.08%)	-11.840 (+1.16%)	-11.830 (+1.03%)	Max	
-35V	-12.115 (- .96%)	-12.110 (- .93%)	-12.110 (-1.06%)	-12.080 (-1.36%)	Min	
	-12.000	-11.999	-11.983	-11.918	Mean	
	-11.875 (+1.04%)	-11.870 (+1.07%)	-11.842 (+1.17%)	-11.795 (+1.03%)	Max	

Min value of V_{out} for all readings = -12.115 volts Spec. -12.6 V $\leq V_{out} \leq$ -11.4 V
Mean value of V_{out} for all readings = -11.981 volts
Max value of V_{out} for all readings = -11.820 volts

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value based on six device samples from two manufacturers, of the output voltage, b) the maximum output voltage and the percentage above mean and c) the minimum output voltage and the percentage below the mean.

Table 5.7. Output voltage (V_{out}) versus input voltage (V_{in}) and load current (I_L) for device type 03. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Value	Unit
	I_L = 5 mA	I_L = 50 mA	I_L = 350 mA	I_L = 500 mA		
-18.5V	-14.500 (- .09%)	-14.505 (- .09%)	-14.470 (- .09%)	-14.520 (- .24%)	Min	Volts
	-14.488	-14.492	-14.458	-14.485	Mean	
	-14.475 (+ .09%)	-14.478 (+ .09%)	-14.445 (+ .09%)	-14.450 (+ .24%)	Max	
-20V	-14.500 (- .10%)	-14.510 (- .01%)	-14.475 (- .12%)	-14.530 (- .24%)	Min	
	-14.485	-14.494	-14.458	-14.495	Mean	
	-14.470 (+ .10%)	-14.478 (+ .01%)	-14.440 (+ .12%)	-14.460 (+ .24%)	Max	
-30V	-14.502 (- .11%)	-14.515 (- .12%)	-14.485 (- .12%)	-14.535 (- .24%)	Min	
	-14.486	-14.498	-14.468	-14.500	Mean	
	-14.470 (+ .11%)	-14.480 (+ .12%)	-14.450 (+ .12%)	-14.465 (+ .24%)	Max	
-35V	-14.505 (- .10%)	-14.515 (- .12%)	-14.495 (- .12%)	-14.530 (- .23%)	Min	
	-14.490	-14.498	-14.478	-14.496	Mean	
	-14.475 (+ .10%)	-14.480 (+ .12%)	-14.460 (+ .12%)	-14.462 (+ .23%)	Max	

Min value of V_{out} for all readings = -14.515 Volts
Mean value of V_{out} for all readings = -14.486 Volts
Max value of V_{out} for all readings = -14.440 Volts

Spec. $-15.75V \leq V_{out} \leq -14.25V$

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value, based on two device samples from one manufacturer, of the output voltage, b) the maximum output voltage and the percentage above the mean and c) the minimum output voltage and the percentage below the mean.

TABLE 5.8. Output voltage (V_{out}) versus input voltage (V_{in}) and load current (I_L) for device type 04. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Value	Unit
	I_L = 5 mA	I_L = 50 mA	I_L = 350 mA	I_L = 500 mA		
-28V	-23.648 (-1.15%)	-23.643 (-1.17%)	-23.610 (-1.14%)	-23.590 (-1.07%)	Min	Volts
	-23.377	-23.370	-23.343	-23.341	Mean	
	-23.260 (+ .50%)	-23.255 (+ .50%)	-23.240 (+ .44%)	-23.245 (+ .41%)	Max	
-30V	-23.650 (-1.17%)	-23.645 (-1.15%)	-23.611 (-1.15%)	-23.595 (-1.07%)	Min	
	-23.376	-23.373	-23.343	-23.346	Mean	
	-23.255 (+ .52%)	-23.258 (+ .49%)	-23.235 (+ .46%)	-23.245 (+ .45%)	Max	
-38V	-23.655 (-1.18%)	-23.650 (-1.18%)	-23.622 (-1.17%)	-23.605 (-1.08%)	Min	
	-23.380	-23.375	-23.250	-23.352	Mean	
	-23.265 (+ .49%)	-23.258 (+ .50%)	-23.238 (+ .48%)	-23.245 (+ .46%)	Max	
-40V	-23.655 (-1.18%)	-23.650 (-1.07%)	-23.622 (-1.16%)	-23.610 (-1.11%)	Min	
	-23.379	-23.400	-23.352	-23.351	Mean	
	-23.260 (+ .51%)	-23.262 (+ .59%)	-23.238 (+ .49%)	-23.240 (+ .48%)	Max	

Min value of V_{out} for all readings = -23.655 Volts
Mean value of V_{out} for all readings = -23.357 Volts
Max value of V_{out} for all readings = -23.235 Volts

Spec. -25.20V V_{out} -22.80V

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value, based on four device samples from one manufacturer, of the output voltage, b) the maximum output voltage and the percentage above the mean and c) the minimum output voltage and the percentage below the mean.

TABLE 5.9. Output voltage V_{out} versus input voltage (V_{in}) and load current (I_L) for device type 05. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Values	Unit
	I_L = 5 mA	I_L = 100 mA	I_L = 350 mA	I_L = 1.0 A		
- 8V	-5.115 (- .85%)	-5.116 (- .97%)	-5.104 (- .96%)	-5.072 (- .93%)	Min	Volts
	-5.072	-5.067	-5.055	-5.026	Mean	
	-5.024 (+ .94%)	-5.018 (+ .97%)	-5.009 (+ .97%)	-4.984 (+ .83%)	Max	
-10V	-5.116 (- .83%)	-5.119 (- .98%)	-5.106 (- .95%)	-5.074 (- .90%)	Min	
	-5.074	-5.069	-5.058	-5.029	Mean	
	-5.025 (+ .96%)	-5.021 (+ .95%)	-5.011 (+ .93%)	-4.986 (+ .85%)	Max	
-20V	-5.122 (- .85%)	-5.123 (- .96%)	-5.111 (- .95%)	-5.081 (- .91%)	Min	
	-5.079	-5.075	-5.063	-5.035	Mean	
	-5.030 (+ .96%)	-5.026 (+ .96%)	-5.015 (+ .95%)	-4.990 (+ .89%)	Max	
-35V	-5.054 (- .21%)	-5.054 (- .25%)	-5.042 (- .22%)	-5.018 (- .25%)	Min	
	-5.044 2/	-5.041 3/	-5.031 3/	-5.005 3/	Mean	
	-5.033 (+ .21%)	-5.029 (+ .24%)	-5.021 (+ .20%)	-4.993 (+ .24%)	Max	

Min value of V_{out} for all readings = -5.123 Volts
Mean value of V_{out} for all readings = -5.055 Volts
Max value of V_{out} for all readings = -4.985 Volts

Spec. $-5.25V \leq V_{out} \leq -4.75V$

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value based on six device samples from two manufacturers, of the output voltage b) the maximum output voltage and the percentage above the mean and c) the minimum output voltage and the percentage below the mean.

2/ Only two samples continued to regulate the output voltage.

3/ Only three samples continued to regulate the output voltage.

TABLE 5.10. Output voltage (V_{out}) versus input voltage (V_{in}) and load current (I_L) for device type 08. 1/

Input Voltage (V_{in})	Output Voltage (V_{out})				V_{out} Value	Unit
	I_L = 5 mA	I_L = 100 mA	I_L = 500 mA	I_L = 1.0 A		
-28V	-24.540 (-1.80%)	-24.572 (-1.93%)	-24.565 (-1.99%)	-24.550 (-2.03%)	Min	Volts
	-24.106	-24.106	-24.087	-24.062	Mean	
	-23.650 (+1.89%)	-23.625 (+1.99%)	-23.600 (+2.02%)	-23.545 (+2.15%)	Max	
-30V	-24.545 (-1.82%)	-24.570 (-1.93%)	-24.565 (-2.14%)	-24.550 (-2.02%)	Min	
	-24.107	-24.104	-24.094	-24.064	Mean	
	-23.640 (+1.94%)	-23.620 (+2.01%)	-23.608 (+2.02%)	-23.560 (+2.09%)	Max	
-38V	-24.550 (-1.77%)	-24.570 (-1.93%)	-24.570 (-1.87%)	-24.545 (-1.98%)	Min	
	-24.123 2/	-24.106	-24.119	-24.068	Mean	
	-23.645 (+1.98%)	-23.635 (+1.95%)	-23.610 (+2.11%)	-23.570 (+2.07%)	Max	
-40V	-24.550 (-1.77%)	-24.565 (-1.90%)	-24.565 (-1.85%)	-24.540 (-1.97%)	Min	
	-24.124 2/	-24.107	-24.119	-24.066	Mean	
	-23.645 (+1.98%)	-23.640 (+1.94%)	-23.610 (+2.11%)	-23.555 (+2.12%)	Max	

Min value of V_{out} for all readings = -24.572 Volts
Mean value of V_{out} for all readings = -24.099 Volts
Max value of V_{out} for all readings = -23.545 Volts

Spec. $-25.20V \leqslant V_{out} \leqslant -22.80V$

NOTES: 1/ For each indicated input voltage (V_{in}) and load current (I_L), the elements of the matrix show a) the mean value based on eight device samples from two manufacturers, of the output voltage, b) the maximum output voltage and the percentage above the mean and c) the minimum output voltage and the percentage below the mean.

2/ Only seven samples continued to regulate the output voltage.

TABLE 5.11. Line Regulation for Device Type 01. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-35V \leq V_{in} \leq -8V$	$-25V \leq V_{in} \leq -8V$		
50 mA	+ 7	+ 5	Min	mV
	+ 12.5	+ 9.5	Mean	
	+ 17	+ 15	Max	
350 mA	- 56	+ 5	Min	
	- 17 2/	+ 10.6	Mean	
	+ 10	+ 20	Max	

Spec. (I_L = 50 mA; $-35V \leq V_{in} \leq -8V$) V_{RLINE} = ± 150 mV
(I_L = 350 mA; $-25V \leq V_{in} \leq -8V$) V_{RLINE} = ± 50 mV

Notes: 1/ The mean value of the line regulation measurements is based on six device samples from two manufacturers.

2/ Only three samples from one manufacturer continued to regulate. This is an unspecified condition.

TABLE 5.12. Line Regulation for Device Type 02. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-35 \leq V_{in} \leq -15V$	$-32V \leq V_{in} \leq -15V$		
50 mA	+ 3	+ 0	Min	mV
	+ 8.8	+ 8	Mean	
	+ 15	+ 15	Max	
350 mA	+ 3	+ 1	Min	
	+ 15.8	+ 12.7	Mean	
	+ 30	+ 25	Max	

Spec. (I_L = 50 mA; $-35V \leq V_{in} \leq -15V$) V_{RLINE} = ± 360 mV
(I_L = 350 mA; $-32V \leq V_{in} \leq -15V$) V_{RLINE} = ± 120 mV

Notes: 1/ The mean value of the line regulation measurements is based on six device samples from two manufacturers.

TABLE 5.13. Line Regulation for Device Type 03. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-35V \leq V_{in} \leq -18.5V$	$-30V \leq V_{in} \leq -18.5V$		
50 mA	+ 2	+ 2	Min	mV
	+ 6	+ 6	Mean	
	+ 10	+ 10	Max	
350 mA	+ 15	+ 5	Min	
	+ 20	+ 10	Mean	
	+ 25	+ 15	Max	

Spec. (I_L = 350 mA; $-35V \leq V_{in} \leq -15.5V$) V_{RLINE} = ± 150 mV

Notes: 1/ The mean value of the line regulation measurements is based on two device samples from one manufacturer.

TABLE 5.14: Line Regulator for Device Type 04. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-40V \leq V_{in} \leq -28V$	$-40K \leq V_{in} \leq -28V$		
50 mA	- 6	0	Min	mV
	+ 3.75	+ 3.75	Mean	
	+ 7	+ 7	Max	
350 mA	- 2	- 2	Min	
	+ 8.25	+ 6.5	Mean	
	+ 20	+ 13	Max	

Spec. (I_L = 50 mA; $-40V \leq V_{in} \leq -28V$) V_{RLINE} = ± 720 mV
(I_L = 350 mA; $-38V \leq V_{in} \leq -28V$) V_{RLINE} = ± 240 mV

Notes: 1/ The mean value of the line regulation measurements is based on four device samples from one manufacturer.

TABLE 5.15. Line Regulation for Device Type 05. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-35V \leq V_{in} \leq -8V$	$-20V \leq V_{in} \leq -8V$		
100 mA	+ 9	+ 4	Min	mV
	+ 10.3 2/	+ 7.5	Mean	
	+ 12	+ 9	Max	
350 mA	+ 10	+ 6	Min	
	+ 12 2/	+ 7.7	Mean	
	+ 14	+ 10	Max	

Spec. (I_L = .1A; $-35V \leq V_{in} \leq -8V$) V_{RLINE} = ± 150 mA
(I_L = .5A; $-25V \leq V_{in} \leq -8V$) V_{RLINE} = ± 150 mA

Notes: 1/ The mean value of the line regulation measurements is based on six device samples from two manufacturers.

2/ Only three samples from one manufacturer continued to regulate at V_{in} = -35V.

TABLE 5.16. Line Regulation for Device Type 08. 1/

Load Current (I_L)	Line Regulation (V_{RLINE})		ΔV_{out} Value	Unit
	$-40V \leq V_{in} \leq -28V$	$-38V \leq V_{in} \leq -28V$		
100 mA	- 20	- 15	Min	mV
	+ 1.0	- .25	Mean	
	+ 15	+ 10	Max	
500 mA	- 7	- 5	Min	
	+ 7.1	+ 6.25	Mean	
	+ 22	+ 15	Max	

Spec. (I_L = 100 mA; $-40V \leq V_{in} \leq -28V$) V_{RLINE} = ± 720 mV
(I_L = 500 mA; $-38V \leq V_{in} \leq -28V$) V_{RLINE} = ± 240 mV

Note: 1/ The mean value of the line regulation measurements is based on eight device samples from two manufacturers.

TABLE 5.17. Load Regulation for Device Type 01. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Values	Unit
	5 mA ≤ I_L ≤ 500 mA	5 mA ≤ I_L ≤ 50 mA		
-10V	- 50	- 12	Min	mV
	- 32.3	- 3.5	Mean	
	- 5	+ 1	Max	
-35V	N/A 2/	- 14	Min	
		- 6.5	Mean	
		- 0	Max	

Spec. (V_{in} = -10V; 5 mA ≤ I_L ≤ 500 mA) V_{RLOAD} = ± 100 mV
(V_{in} = -35V; 5 mA ≤ I_L ≤ 50 mA) V_{RLOAD} = ± 150 mV

Notes: 1/ The mean value of the load regulation measurements is based on six device samples from two manufacturers.

2/ None of the device samples continued to operate. This is an unspecified condition. Three samples from one manufacturer continued to regulate with V_{in} = -35V and 5 mA ≤ I_L ≤ 350 mA. The mean ΔV_{out} for these conditions was -16.7 mV.

TABLE 5.18. Load Regulation for Device Type 02. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Values	Unit
	5 mA ≤ I_L ≤ 500 mA	5 mA ≤ I_L ≤ 50 mA		
- 17V	- 50	- 12	Min	mV
	- 32.2	- 6.7	Mean	
	- 15	- 1	Max	
- 35V	- 235	- 10	Min	
	- 82	- 7	Mean	
	- 35	+ 10	Max	

Spec. (V_{in} = - 17V; 5 mA ≤ I_L ≤ 500 mA) V_{RLOAD} = ± 240 mV
(V_{in} = - 35V; 5 mA ≤ I_L ≤ 50 mA) V_{RLOAD} = ± 360 mV

Note: 1/ The mean value of the load regulation measurements is based on six device samples from two manufacturers.

TABLE 5.19. Load Regulation for Device Type 03. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Values	Units
	5 mA $\leq I_L \leq$ 500 mA	5 mA $\leq I_L \leq$ 50 mA		
- 18.5 V	- 25	+ 3	Min	mV
	- 2.5	+ 4	Mean	
	+ 20	+ 5	Max	
- 35 V	+ 5	- 13	Min	
	+ 7.5	+ 6	Mean	
	+ 10	+ 25	Max	

Spec. (V_{in} = - 20V; 5 mA $\leq I_L \leq$ 500 mA) V_{RLOAD} = ± 300 mV
(V_{in} = - 35V; 5 mA $\leq I_L \leq$ 50 mA) V_{RLOAD} = ± 450 mV

NOTE: 1/ The mean value of the load regulation measurements is based on two device samples from one manufacturer.

TABLE 5.20. Load Regulation for Device Type 04. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Values	Units
	5 mA $\leq I_L \leq$ 500 mA	5 mA $\leq I_L \leq$ 50 mA		
- 30 V	- 70	- 10	Min	mV
	- 36.3	- 3	Mean	
	- 2	+ 3	Max	
- 40 V	- 45	- 8	Min	
	- 28	- 4.75	Mean	
	- 12	+ 12	Max	

Spec. (V_{in} = -30V; 5 mA $\leq I_L \leq$ 500 mA) V_{RLOAD} = ± 480 mV
(V_{in} = -40V; 5 mA $\leq I_L \leq$ 50 mA) V_{RLOAD} = ± 720 mV

NOTES: 1/ The mean value of the load regulation measurements is based on four device types from one manufacturer.

TABLE 5.21. Load Regulation for Device Type 05. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Value	Unit
	5 mA ≤ I_L ≤ 1.0 A	5 mA ≤ I_L ≤ 100 mA		
- 10 V	- 13 - 4.3 + 3	- 53 - 45 - 38	Min Mean Max	mV ↓
- 35 V	- 13 - 8.5 2/ - 4	- 49 - 44.5 2/ - 40	Min Mean Max	

Spec. (V_{in} = -10V; 5 mA ≤ I_L ≤ 1.0 A) V_{RLOAD} = ± 100 mV
(V_{in} = -35V; 5 mA ≤ I_L ≤ 100mA) V_{RLOAD} = ± 150 mV

NOTES: 1/ The mean value of the load regulation measurements is based on six device samples from two manufacturers.

2/ Only two device samples continued to regulate with V_{in} = -35V, I_L = 5 mA

TABLE 5.22. Load Regulation for Device Type 08. 1/

Input Voltage (V_{in})	Load Regulation (V_{RLOAD})		ΔV_{out} Value	Unit
	5 mA ≤ I_L ≤ 1.0 A	5 mA ≤ I_L ≤ 100 mA		
- 30V	- 80 - 42.5 + 25	- 15 - 0.5 + 25	Min Mean Max	mV ↓
- 40V	- 90 - 45 2/ + 20	- 10 - 2.8 2/ + 15	Min Mean Max	

Spec. (V_{in} = -30V; 5 mA ≤ I_L ≤ 1.0 A) V_{RLOAD} = 480 mV
(V_{in} = -40V; 5 mA ≤ I_L ≤ 100mA) V_{RLOAD} = 720 mV

NOTES: 1/ The mean value of the load regulation measurements is based on eight device samples from two manufacturers.

2/ One device sample failed to regulate with V_{in} = -40 V, I_L = 5 mV.

TABLE 5.23. Output Short Circuit Current for Device Type 01. 1/

Input Voltage (V_{in})	Output Short Circuit Current (I_{os})			Unit
	min	mean	max	
- 10 V	600	650	740	mA
- 25 V	310	362	440	↓
- 35 V	1.2	146	300	↓

Spec. (V_{in} = - 10 V) 10 mA $\leq I_{os} \leq$ 2.00 A
(V_{in} = - 25 V) 10 mA $\leq I_{os} \leq$ 1.50 A
(V_{in} = - 35 V) 10 mA $\leq I_{os} \leq$ 1.00 A

NOTE: 1/ The mean value of the output short circuit current measurements is based on six device samples from two manufacturers.

TABLE 5.24. Output Short Circuit Current for Device Type 02. 1/

Input Voltage (V_{in})	Output Short Circuit Current (I_{os})			Unit
	min	mean	max	
- 17 V	560	679	780	mA
- 32 V	210	432 2/	560	↓
- 35 V	150	384 2/	480	↓

Spec. (V_{in} = - 17 V) 10 mA $\leq I_{os} \leq$ 1.75 A
(V_{in} = - 32 V) 10 mA $\leq I_{os} \leq$ 1.50 A
(V_{in} = - 35 V) 10 mA $\leq I_{os} \leq$ 1.00 A

NOTES: 1/ The mean value of the output short circuit current measurements is based on six device samples from two manufacturers.

2/ One unit failed after the initial test measurement.

TABLE 5.25. Output Short Circuit Current for Device Type 03. 1/

Input Voltage (V_{in})	Output Short Circuit Current (I_{os})			Unit
	min	mean	max	
- 20 V	540	555	570	mA
- 27 V	350	355	360	↓
- 35 V	4	4	4	↓

Spec. (V_{in} = -20 V) 10 mA $\leq I_{os} \leq$ 1.75
(V_{in} = -35 V) 10 mA $\leq I_{os} \leq$ 1.00

NOTE: 1/ The mean value of the output short circuit current measurements is based on two device samples from one manufacturer.

TABLE 5.26. Output Short Circuit Current for Device Type 05. 1/

Input Voltage (V_{in})	Output Short Circuit Current (I_{os})			Unit
	min	mean	max	
- 10 V	1.0	1.1	1.25	A
- 25 V	.3	0.37	.4	A
- 35 V	2.5	2.75	3.2	mA

Spec. (V_{in} = - 10V) 20 mA $\leq I_{os} \leq$ 4.00 A
(V_{in} = - 25V) 20 mA $\leq I_{os} \leq$ 3.00 A
(V_{in} = - 35V) 20 mA $\leq I_{os} \leq$ 2.00 A

NOTE: 1/ The mean value of the output short circuit current measurements is based on three samples from one vendor.

TABLE 5.27. Output Short Circuit Current for Device Type 08. 1/

Input Voltage (V_{in})	Output Short Circuit Current (I_{os})			Unit
	min	mean	max	
- 30 V	13	696	1100	mA
- 38 V	2.9	469	800	mA
- 40 V	2.8	420	750	mA

Spec. (V_{in} = - 30V) 20 mA $\leq I_{os} \leq$ 2.50 A
(V_{in} = - 38V) 20 mA $\leq I_{os} \leq$ 2.00 A
(V_{in} = - 40V) 20 mA $\leq I_{os} \leq$ 2.00 A

NOTE: 1/ The mean value of the output short circuit current is based on nine device samples from two manufacturers.

TABLE 5-28. Electrical performance characteristics for device type 01

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -8 V	I_L = 5 mA, 0.5 A		-5.25	-4.75	V
		V_{IN} = -20 V	I_L = 5 mA, 0.5 A		-5.25	-4.75	V
		V_{IN} = -35 V	I_L = 5 mA, 50 mA		-5.25	-4.75	V
		V_{IN} = -10 V	I_L = 5 mA	T_A = 150°C	-5.30	-4.70	V
Line regulation	V_{RLINE}	-35 V $\leq V_{IN} \leq$ -8 V	I_L = 50 mA		-150	150	mV
		-25 V $\leq V_{IN} \leq$ -8 V	I_L = 350 mA		-50	50	mV
Load regulation	V_{RLOAD}	V_{IN} = -10 V	5 mA $\leq I_L \leq$ 500 mA		-100	100	mV
		V_{IN} = -35 V	5 mA $\leq I_L \leq$ 50 mA		-150	150	mV
Standby current drain	I_{SCD}	V_{IN} = -10 V	I_L = 5 mA		0.1	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.1	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-35 V $\leq V_{IN} \leq$ -8 V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -10 V	5 mA $\leq I_L \leq$ 500 mA		-0.5	0.5	mA
Output short circuit current	I_{OS}						A
		V_{IN} = -25 V			0.01	1.50	A
		V_{IN} = -35 V			0.01	1.00	A
Peak output current	I_{pk}	V_{IN} = -8 V, forced ΔV_{OUT} = 0.48 V		See figure 9	0.5	2.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -10 V e_i = 1 V_{rms} @ f = 2400 Hz	I_L = 125 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -10 V	I_L = 50 mA	See figure 11 T_A = 25°C	-	150	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -15V	I_L = 500 mA	T_A = 25°C	-50	+50	mV
Voltage Startup	V_{START}	V_{IN} = -20 V	I_L = 500 mA	See figure 14	-5.25	-4.75	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -10 V	I_L = 5mA	See figure 12 T_A = 25°C	-	30.0	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -10 V	I_L = 50mA ΔI_L = 200mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-29. Electrical performance characteristics for device type 02

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -15 V	I_L = 5 mA, 0.5 A		-12.60	-11.40	V
		V_{IN} = -27 V	I_L = 5 mA, 0.5 A		-12.60	-11.40	V
		V_{IN} = -35 V	I_L = 5 mA, 50 mA		-12.60	-11.40	V
		V_{IN} = -17 V	I_L = 5 mA	T_A = 150°C	-12.72	-11.28	V
Line regulation	V_{RLINE}	-35V ≤ V_{IN} ≤ -15 V	I_L = 50 mA		-360	360	mV
		-32 V ≤ V_{IN} ≤ -15 V	I_L = 350 mA		-120	120	mV
Load regulation	V_{RLOAD}	V_{IN} = -17 V	5 mA ≤ I_L ≤ 500mA		-240	240	mV
		V_{IN} = -35 V	5mA ≤ I_L ≤ 50 mA		-360	360	mV
Standby current drain	I_{SCD}	V_{IN} = -17 V	I_L = 5 mA		0.1	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.1	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-35 V ≤ V_{IN} ≤ -15 V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -17 V	5 mA ≤ I_L ≤ 500mA		-0.5	0.5	mA
Output short circuit current	I_{OS}						A
		V_{IN} = -25 V			0.01	1.50	A
		V_{IN} = -35 V			0.01	1.00	A
Peak output current	I_{pk}	V_{IN} = -15 V, forced ΔV_{OUT} = 1.13 V		See figure 9	0.5	2.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -17 V e_i = 1 V_{rms} f = 2400 Hz	I_L = 125 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -17 V	I_L = 50 mA	See figure 11 T_A = 25°C	-	250	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -22V	I_L = 500mA	T_A = 25°C	-120	120	mV
Voltage Start up	V_{START}	V_{IN} = -28V	I_L = 500 mA	See figure 14	-12.60	-11.40	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -17V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -17V	I_L = 50mA ΔI_L = 200mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-30. Electrical performance characteristics for device type 03

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -18.5 V	I_L = 5 mA, 0.5 A		-15.75	-14.25	V
		V_{IN} = -30 V	I_L = 5 mA, 0.5 A		-15.75	-14.25	V
		V_{IN} = -35 V	I_L = 5 mA, 50 mA		-15.75	-14.25	V
		V_{IN} = -20 V	I_L = 5 mA	T_A = 150°C	-15.90	-14.10	V
Line regulation	V_{RLINE}	-35V ≤ V_{IN} ≤ -18.5V	I_L = 350 mA		-150	150	mV
Load regulation	V_{RLOAD}	V_{IN} = -20 V	5 mA ≤ I_L ≤ 500mA		-300	300	mV
		V_{IN} = -35 V	5mA ≤ I_L ≤ 50 mA		-450	450	mV
Standby current drain	I_{SCD}	V_{IN} = -20 V	I_L = 5 mA		0.1	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.1	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-35 V ≤ V_{IN} ≤ -18.5V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -20 V	5mA ≤ I_L ≤ 500mA		-0.5	0.5	mA
Output short circuit current	I_{OS}	V_{IN} = -25V			0.01	1.50	A
		V_{IN} = -35 V			0.01	1.00	A
Peak output current	I_{pk}	V_{IN} = -18.5 V; forced ΔV_{OUT} = 1.93 V		See figure 9	0.5	2.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -20 V; e_i = 1 V_{rms}; @ f = 2400 Hz	I_L = 125 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -20 V	I_L = 50 mA	See figure 11 T_A = 25°C	-	300	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -25V	I_L = 500mA	T_A = 25°C	-150	150	mV
Voltage Start up	V_{START}	V_{IN} = -30V	I_L = 500mA	See figure 14	-15.75	-14.25	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -20V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -20V	I_L = 50mA, ΔI_L = 200mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-31. Electrical performance characteristics for device type 04

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -28 V	I_L = 5 mA, 0.5 A		-25.20	-22.80	V
		V_{IN} = -38 V	I_L = 5 mA, 0.5 A		-25.20	-22.80	V
		V_{IN} = -40 V	I_L = 5 mA, 50 mA		-25.20	-22.80	V
		V_{IN} = -30 V	I_L = 5 mA	T_A = 150°C	-25.44	-22.56	V
Line regulation	V_{RLINE}	-40V ≤ V_{IN} ≤ -28V	I_L = 50 mA		-720	720	mV
		-38V ≤ V_{IN} ≤ -28V	I_L = 350 mA		-240	240	mV
Load regulation	V_{RLOAD}	V_{IN} = -30 V	5 mA ≤ I_L ≤ 500mA		-480	480	mV
		V_{IN} = -40 V	5 mA ≤ I_L ≤ 50mA		-720	720	mV
Standby current drain	I_{SCD}	V_{IN} = -30 V	I_L = 5 mA		0.1	4.0	mA
		V_{IN} = -40 V	I_L = 5 mA		0.1	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-40V ≤ V_{IN} ≤ -28V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -30 V	5 mA ≤ I_L ≤ 500mA		-0.5	0.5	mA
Output short circuit current	I_{OS}	V_{IN} = -30 V			0.01	1.25	A
		V_{IN} = -40 V			0.01	1.00	A
Peak output current	I_{pk}	V_{IN} = -28 V; forced ΔV_{OUT} = 2.28 V		See figure 9	0.5	2.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -30 V e_i = 1 V_{rms} @ f = 2400Hz	I_L = 125 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -30 V	I_L = 50 mA	See figure 11 T_A = 25°C	-	500	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -34V	I_L = 500mA	T_A = 25°C	-240	240	mV
Voltage Start up	V_{START}	V_{IN} = -38V	I_L = 500mA	See figure 14	-25.20	-22.80	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -30V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -30V	I_L = 50mA ΔI_L = 200mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-32. Electrical performance characteristics for device type 05

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -8 V	I_L = 5 mA, 1.0 A		-5.25	-4.75	V
		V_{IN} = -20 V	I_L = 5 mA, 1.0 A		-5.25	-4.75	V
		V_{IN} = -35 V	I_L = 5 mA, 0.1 A		-5.25	-4.25	V
		V_{IN} = -10 V	I_L = 5 mA	T_A = 150°C	-5.30	-4.70	V
Line regulation	V_{RLINE}	-35V ≤ V_{IN} ≤ -8 V	I_L = 0.1 A		-150	150	mV
		-25V ≤ V_{IN} ≤ -8 V	I_L = 0.5 A		-75	75	mV
Load regulation	V_{RLOAD}	V_{IN} = -10 V	5mA ≤ I_L ≤ 1.0A		-100	100	mV
		V_{IN} = -35 V	5mA ≤ I_L ≤ 0.1A		-150	150	mV
Standby current drain	I_{SCD}	V_{IN} = -10 V	I_L = 5 mA		0.5	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.5	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-35 V ≤ V_{IN} ≤ -8V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -10 V	5mA ≤ I_L ≤ 1.0A		-0.5	0.6	mA
Output short circuit current	I_{OS}	V_{IN} = -25 V			0.02	3.50	A
		V_{IN} = -35 V			0.02	2.00	A
Peak output current	I_{pk}	V_{IN} = -8 V; forced ΔV_{OUT} = 0.08 V		See figure 9	1.0	4.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -10 V e_i = 1 V_{rms} f = 2400Hz	I_L = 350 mA	See figure 10 meter BW 30 Hz to 10 kHz	54	-	dB
Thermal Regulation	V_{RTH}	V_{IN} = -15V	I_L = 1.0A	T_A = 25°C	-50	50	mV
Output noise voltage	N_O	V_{IN} = -10V	I_L = 0.1A		-	125	μV_{rms}
Voltage Startup	V_{START}	V_{IN} = -20V	I_L = 100mAmp	See figure 14	-5.25	-4.75	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -10 V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -10V	I_L = 100mA ΔI_L = 400mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-33. Electrical performance characteristics for device type 06

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -15 V	I_L = 5 mA, 1.0 A		-12.60	-11.40	V
		V_{IN} = -27 V	I_L = 5 mA, 1.0 A		-12.60	-11.40	V
		V_{IN} = -35 V	I_L = 5 mA, 0.1 A		-12.60	-11.40	V
		V_{IN} = -17 V	I_L = 5 mA	T_A = 150°C	-12.72	-11.40	V
Line regulation	V_{RLINE}	-35V ≤ V_{IN} ≤ -15V	I_L = 0.1 A		-360	360	mV
		-32 V ≤ V_{IN} ≤ -15V	I_L = 0.5 A		-120	120	mV
Load regulation	V_{RLOAD}	V_{IN} = -17 V	6mA ≤ I_L ≤ 1.0A		-240	240	mV
		V_{IN} = -35 V	5mA ≤ I_L ≤ 0.1A		-360	360	mV
Standby current drain	I_{SCD}	V_{IN} = -17 V	I_L = 5 mA		0.5	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.5	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-32 V ≤ V_{IN} ≤ -15V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -17 V	5mA ≤ I_L ≤ 1.0A		-0.5	0.5	mA
Output short circuit current	I_{OS}						
		V_{IN} = -32 V			0.02	3.50	A
		V_{IN} = -35 V			0.02	2.00	A
Peak output current	I_{pk}	V_{IN} = -15 V; forced ΔV_{OUT} = 1.13 V		See figure 9	1.0	4.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -17 V, e_i = 1 V_{rms} @ f = 2400Hz	I_L = 350 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -17 V	I_L = 0.1 A	See figure 11 T_A = 25°C	-	250	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -22V	I_L = 1.0 A	T_A = 25°C	-120	120	mV
Voltage Start up	V_{START}	V_{IN} = -28 V	I_L = 1.0 A	See figure 14	-12.60	-11.40	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -17V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -17V	I_L = 100mA, ΔI_L = 400mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-34. Electrical performance characteristics for device type 07

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -18.5 V	I_L = 5 mA, 1.0 A		-15.25	-14.25	V
		V_{IN} = -30 V	I_L = 5 mA, 1.0 A		-15.25	-14.25	V
		V_{IN} = -35 V	I_L = 5 mA, 0.1 A		-15.75	-14.25	V
		V_{IN} = -20 V	I_L = 5 mA	T_A = 150°C	-15.90	-14.10	V
Line regulation	V_{RLINE}	-35 V ≤ V_{IN} ≤ -18.5 V	I_L = 0.5 A		-150	150	mV
Load regulation	V_{RLOAD}	V_{IN} = -20 V	5 mA ≤ I_L ≤ 1.0 A		-300	300	mV
		V_{IN} = -35 V	5 mA ≤ I_L ≤ 0.1 A		-450	450	mV
Standby current drain	I_{SCD}	V_{IN} = -20 V	I_L = 5 mA		0.5	3.0	mA
		V_{IN} = -35 V	I_L = 5 mA		0.5	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-35 V ≤ V_{IN} ≤ -18.5 V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -20 V	5 mA ≤ I_L ≤ 1.0 A		-0.5	0.5	mA
Output short circuit current	I_{OS}	V_{IN} = -20 V			0.02	3.50	A
		V_{IN} = -35 V			0.02	2.00	A
Peak output current	I_{pk}	V_{IN} = -18.5 V; forced ΔV_{OUT} = 1.43 V		See figure 9	1.0	4.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -20 V e_i = 1 V_{rms} @ f = 2400 Hz	I_L = 350 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -20 V	I_L = 0.1 A	See figure 11 T_A = 25°C	-	300	μV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -25V	I_L = 1.0A	T_A = 25°C	-150	150	mV
Voltage Start up	V_{START}	V_{IN} = -30V	I_L = 1.0A	See figure 14	-15.75	-14.25	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -20 V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -20V	I_L = 100mA ΔI_L = 400mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

TABLE 5-35. Electrical performance characteristics for device type 08

Characteristics	Symbol	Conditions (figure 8 unless otherwise specified)			Limits		Units
		Input voltage	Load current	Other	Min	Max	
Output voltage	V_{OUT}	V_{IN} = -28 V	I_L = 5 mA, 1.0 A		-25.20	-22.80	V
		V_{IN} = -38 V	I_L = 5 mA, 1.0 A		-25.20	-22.80	V
		V_{IN} = -40 V	I_L = 5 mA, 0.1 A		-25.20	-22.80	V
		V_{IN} = -30 V	I_L = 5 mA	T_A = 150°C	-25.44	-22.56	V
Line regulation	V_{RLINE}	-40 V ≤ V_{IN} ≤ -28 V	I_L = 0.1 A		-200	200	mV
		-38 V ≤ V_{IN} ≤ -28 V	I_L = 0.5 A		-100	100	mV
Load regulation	V_{RLOAD}	V_{IN} = -30 V	5 mA ≤ I_L ≤ 1.0A		-100	100	mV
		V_{IN} = -40 V	5 mA ≤ I_L ≤ 0.1A		-200	200	mV
Standby current drain	I_{SCD}	V_{IN} = -30 V	I_L = 5 mA		0.5	3.0	mA
		V_{IN} = -40 V	I_L = 5 mA		0.5	4.0	mA
Standby current drain change (versus line voltage)	ΔI_{SCD} (line)	-40 V ≤ V_{IN} ≤ -28 V	I_L = 5 mA		-1.0	1.0	mA
Standby current drain change (versus load current)	ΔI_{SCD} (load)	V_{IN} = -30 V	5mA ≤ I_L ≤ 1.0A		-0.5	0.5	mA
Output short circuit current	I_{OS}	V_{IN} = -30 V			0.02	3.00	A
		V_{IN} = -40 V			0.02	2.00	A
Peak output current	I_{pk}	V_{IN} = -28 V; forced ΔV_{OUT} = 2.28 V		See figure 9	1.0	4.0	A
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -30 V e_i = 1 V_{rms} @ f = 2400Hz	I_L = 350 mA	See figure 10 meter BW 10 Hz to 10 kHz	54	-	dB
Output noise voltage	N_o	V_{IN} = -30 V	I_L = 0.1 A	See figure 11 T_A = 25°C	-	500	mV_{rms}
Thermal Regulation	V_{RTH}	V_{IN} = -34V	I_L = 1.0A	T_A = 25°C	-240	240	mV
Voltage Startup	V_{START}	V_{IN} = -38V	I_L = 1.0A	See figure 14	-25.20	-22.80	V
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -30V	I_L = 5mA	See figure 12 T_A = 25°C	-	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -30V	I_L = 100mA ΔI_L = 400mA	See figure 13 T_A = 25°C	-	2.5	mV/mA

NOTE: All tests performed at T_A = 125°C may, at the manufacturer's option, be performed at T_A = 150°C. Specifications for T_A = 125°C shall then apply at T_A = 150°C.

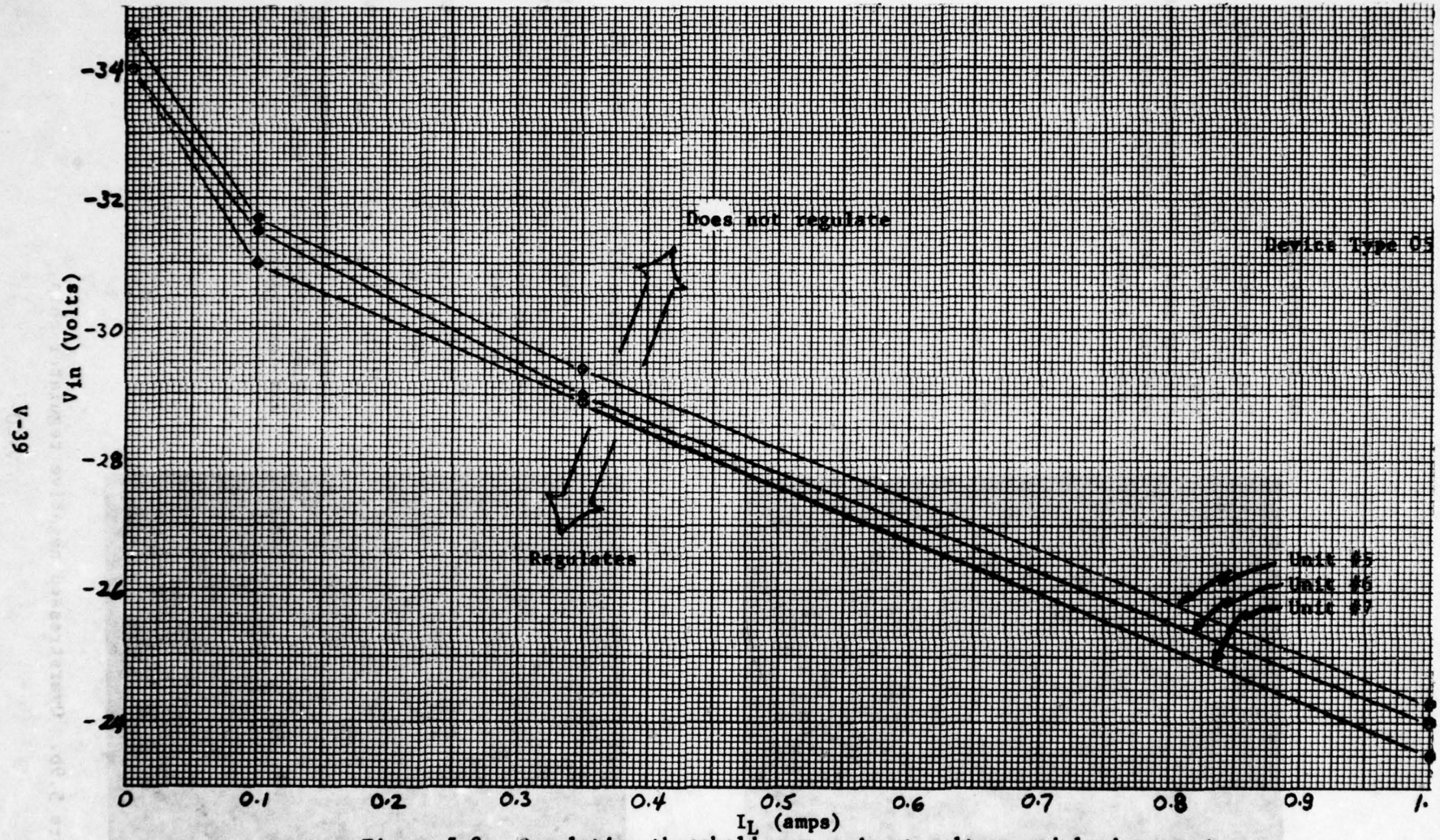
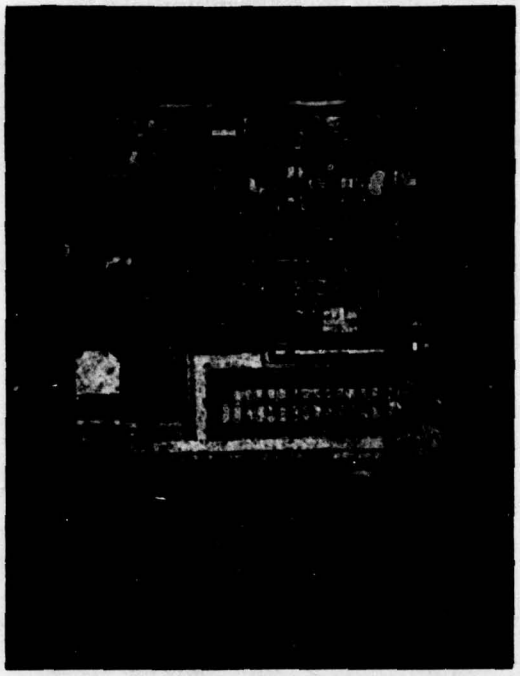


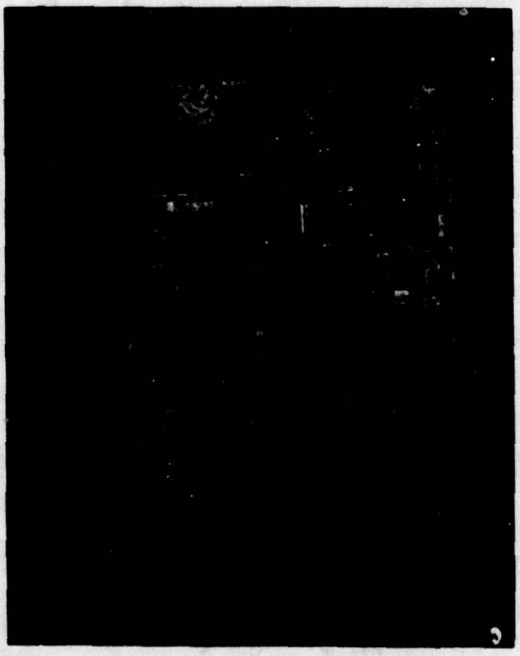
Figure 5.8. Regulation threshold versus input voltage and load current.



Device Type 01 Unit #4

Unit was destroyed by incorrectly connecting the device to the curve tracer test circuit. Incorrect adapter used. The photograph shows evidence of being overstressed in several areas.

Figure 5.9a. Overstressed negative regulator chip.



Device Type 02 Unit #1

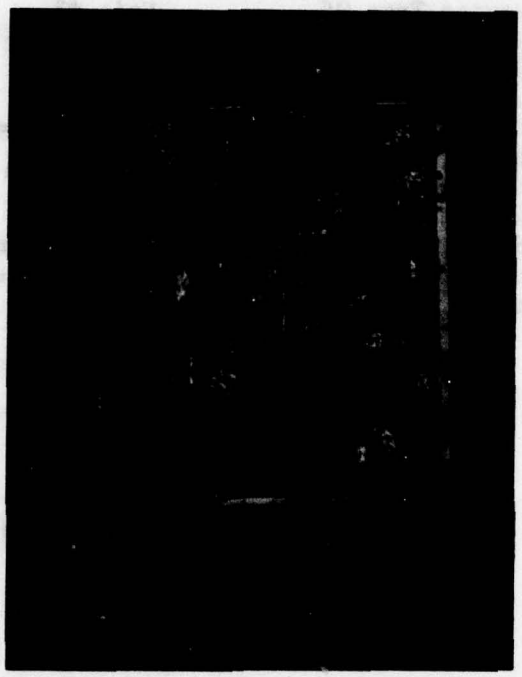
The unit showed no anomalies during the output voltage tests. Unit was destroyed during the output short circuit test.

With V_{in} = -17, I_{OS} = 670 mA
and P_D = 11.4W

With V_{in} = -32V, I_{OS} = 210 mA

During the latter measurement, the current dropped to 0 mA. The unit was destroyed.

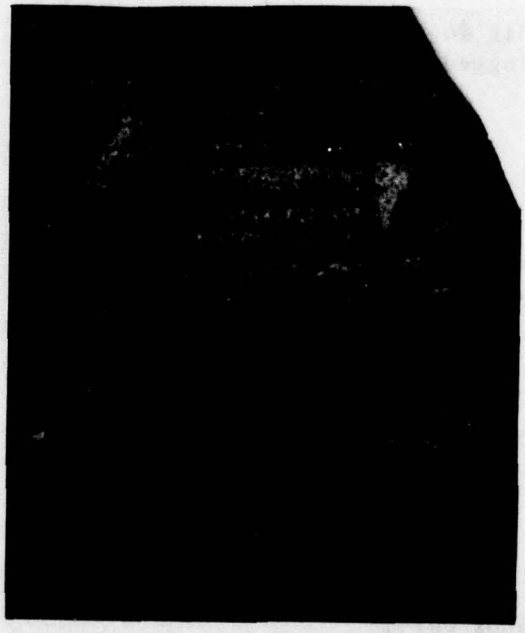
Figure 5.9b. Overstressed negative regulator chip.



Device Type 04 Unit #2

Unit failed during output short circuit test. Short circuit current I_{OS} was greater than 250 mA at V_{in} = -30V. Power dissipation was 7.5 Watts in a T05 case. Evidence of insufficient current fold-back.

Figure 5.9c. Overstressed negative regulator chip.



Device Type 08 Unit #1

Unit oscillates during initial testing. Developed an input to output short circuit while loaded. Eventually (matter of seconds), output opened.

Figure 5.9d. Overstressed negative regulator chip.

Device Type 05 Unit #2

Unit #2 started motorboating at the output when $|V_i| > 24.5V$ and I_L = 5.0 mA. Low level oscillations were observed during the test interval (i.e., 98%) when the load current was zero. Device failed while checking for the maximum load current that will degrade the output voltage to -4.75V.

Figure 5.9e. Overstressed negative regulator chip.

Device Type 05 Unit #4

Unit #4 failed after the device was plugged into a hot socket.

Figure 5.9f. Overstressed negative regulator chip.

5.6 Bibliography

Below are listed some works which have topics devoted to integrated circuit voltage regulators.

1. The Voltage Regulator Handbook; John D. Spencer and Dale E. Pippenger, Texas Instruments Corporation, 1977

2. National Voltage Regulator Handbook; Nello Sevaslopoulos et al, National, 1975.

3. Voltage Regulator Handbook; Andy Adamian, Fairchild Camera and Instrument Corporation, 1978.

4. Voltage Regulator Handbook, Theory and Practice; Henry Wurzburg et al, Motorola Inc, 1976.

SECTION VI

DIGITAL-TO-ANALOG CONVERTERS

MIL-M-38510/113

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SECTION VI

DIGITAL-TO-ANALOG CONVERTERS

MIL-M-38510/113

6.1 Introduction and Background

Since the advent of the microprocessor, the growth rate of the digital-to-analog converter and analog-to-digital converter market has increased markedly.

In response to that growth, the first characterization effort of a JAN 38510 digital-to-analog converter has been initiated. The DAC-08 device was selected for characterization because it meets the criteria of popularity, low cost (it is monolithic), multiple-sourcing, and quality of design. It was originally introduced by Precision Monolithics, Inc. and has become one of the most popular 8-bit digital-to-analog converters on the market today.

Initially, proposed specifications for the DAC08, the DAC08A, and the 1508 were received from the JC-41 Committee. As the characterization effort evolved, emphasis shifted to the DAC08, which has superior performance for at least three parameters ... namely, voltage compliance, settling time, and supply current. In order to include the needs of most users, both a standard version of the DAC08 (0.19% non-linearity) and the higher precision DAC08A (0.1% non-linearity) have been specified in the proposed slash sheet.

6.2 Description of Device

The DAC08 is an 8-bit monolithic multiplying D/A Converter, having dual complementary current outputs. The outputs have a large voltage compliance range of + 18V to -10V, and a full scale current of 2 mA. It is used with an external reference, which may be either positive or negative; however, in the true sense of the word, it is not a multiplying DAC that can be used with an AC reference directly (without biasing or additional external circuitry).

The DAC08 is a very high speed device, having a maximum settling time of 135 nsec to ± 1/2 LSB. The device can interface directly with various logic families by appropriate pin programming of the adjustable logic input threshold. Supply voltages can range from ± 4.5V to ± 18V.

A functional diagram of the device is shown in Figure 6.1, along with typical external connections. With $V_{REF}(-)$ grounded and $V_{REF}(+)$ tied to 10 VDC through a 5K ohm resistor, a 2.0 mA current flows into $V_{REF}(+)$. That current then flows through the reference transistor and reference 1K ohm resistor which sets the base voltage at the reference transistor and at all the other current sink transistors. The MSB current sink sinks 1 mA. The second bit current sink sinks 1/2 mA; the current level decreases by a factor of 1/2 with each succeeding current sink due to the R-2R ladder configuration. The LSB current sink sinks 8 uA. The current switches only steer the current from either of the two output pins. The degree of insensitivity of the current sinks and switches to voltage variations at the outputs is termed high output compliance.

6.3 Characterization of the DAC-08

Static Test Parameters

Table 6-1 shows the electrical performance limits that were recommended by the JC-41 Committee for MIL-M-38510/113. Unless otherwise specified, all tests are performed with the supply voltage at ±15V and I_{REF} set to 2.00 mA (10V/5KΩ), and over the temperature range of -55°C to +125°C.

Supply current from both supplies is measured only with all input bits high. With proper device operation, the supply current is not dependent on the digital input word. GEOS checked supply current with all input bits low to verify no dependence.

The Full Scale Current is the sink current into output I_o with all bits high, or at output $\overline{I_o}$ with all bits low. This test indicates to the user the gain error of the device over the temperature range.

The Zero Scale Current is the sink current into either I_o with all bits low, or into $\overline{I_o}$ with all bits high. This test indicates to the user the offset error of the device over the temperature range. Power supply sensitivity is checked for $+V_s$ from 4.5 V to 5.5 V and from 12 V to 18 V with $-V_s$ at -18V and for $-V_s$ from -4.5 V to -5.5V and from -12V to -18V with $+V_s$ at +18V during full scale current operation. This test checks the variation in full scale current into both the I_o and $\overline{I_o}$ outputs due to power supply variations.

The Output Current Range test indicates to the user the level of full scale current the device can sink with a low negative supply level.

The Reference Bias Current test measures the bias current into the grounded input of the voltage-to-current converter section of the device and checks for excessive leakage.

The High Level Input Current test checks leakage current at each of the digital inputs, and the Low Level Input Current test checks base current at each of the digital inputs.

Voltage compliance at both of the outputs is checked during full scale operation. This test verifies that only a small change in full scale current results when voltages of +18V and -10V are forced at the output. The full scale current is checked both to an absolute limit and a delta limit from +18V to -10V.

Linearity error is checked in several forms. The positive bit errors are summed and checked to a limit. The negative bit errors are summed and checked to a limit. The difference of these two sums are checked to assure sufficient freedom from bit interaction (see section for a further discussion of this subject). A worst case linearity error is calculated by summing the absolute values of the positive and negative bit errors and the difference of the sums (which is a measure of bit interaction).

Monotonicity is checked to assure the user that the transfer characteristics (output current vs. digital input) never reverses in slope (i.e. - never changes in the wrong direction). The device manufacturers claim that it is only necessary to check the major carry points because this is the most likely transition point to encounter such a failure. GEOS data tends to substantiate that claim.

The Output Symmetry test assures a good match between I_o and $\overline{I}_o$ full scale output currents.

The Full Scale Current Temperature Coefficient Check calculates the variation in full scale current due to a variation in temperature. This test gives the user the temperature coefficient of the gain error including the offset error. If zero scale current temperature coefficient was also calculated, then offset error TC and gain error TC could be separated out of out of the Full Scale Current Temperature Coefficient data.

Dynamic Test Parameters (25°C only)

The Propagation Delay Test measures the time it takes for the output to respond to an all-bits-high to all-bits-low transition and to an all-bits-low to all-bits-high transition. These measurements are made from the 50% point of input to the 50% point of the output.

The Settling Time Test measures the response time between the 50% point of the input transition (all-bits-high to all-bits-low or all-bits-low to all-bits-high) and the point at which the output settles to within 4 microamperes (one half of a least significant bit) of the final value. For a 500 Ω load resistor 4 microamperes corresponds to 2 millivolts.

Static Test Circuit

Figure 6-2 shows the static test circuit recommended by the JC-41 Committee. Although it is not readily apparent how the voltage compliance test is performed using this circuit, it appears that the following technique is used: (1) SW6 is set to the I_{out} position, (2) + 18 V is applied to I_{out} with SW1 and SW2 open, (3) the current drawn into I_{out} is measured with SW5 closed for 18 V compliance and with SW5 open for -10 V compliance.

The static test circuit shown in Figure 6-3 was used and may be more suitable for bench testing when a problem arises. The + 18 V voltage compliance test is performed by setting pin 15 to + 18 V and setting pin 13 to 35 V and pin 14 to 0V (i.e - set the op-amp supply voltage to V + = 35 V and V - = 0V). Offset due to the finite common mode rejection ratio of the op-amp and other offset errors are calibrated out by opening K3a and measuring the voltage at pin 24 with the reference DAC set to zero. The contribution of gain error associated with the .01% resistor tolerance is not a significant factor and does not contribute to the errors in the linearity tests. The 16 bit DAC is linear to .003% so that its error contribution to the linearity measurement is not significant.

At a recent meeting of the JC-41 D/A converter subcommittee this test circuit was criticized for:

(1) use of .01% resistors which degrade the accuracy of the 16 bit reference DAC and

(2) use of a voltage output reference DAC instead of a current output reference DAC.

The answer to (1) is that the .01% resistors only contribute gain error except during the compliance test when an offset error is generated (which is calibrated out). In any case, linearity error is certainly not degraded.

The answer to (2) is that a current output reference DAC could be used and such a variation would be quite acceptable.

Settling Time and Propagation Delay Test Circuit

Figure 6.4 shows the settling time and propagation delay test circuit recommended by the JC-41 Committee. The two diodes (Schottky, although not so identified) connected in opposite directions provide clamping to avoid saturation of the oscilloscope preamplifier. V_{ADJ} provides bias through Q1 to determine the clamp level. When the settling time to be measured is for the low-to-high transition of the input, the output goes from 0V to -0.67V without any bias. V_{ADJ} biases the output so that the settling level is at 0V instead of -0.67 V. Therefore, with V_{ADJ} at 2.6 V, settling time due to the

low-to-high input transition is measured. When the settling time due to the high-to-low transition is measured, V_{ADJ} is set to + 0.6 V which sets the emitter at 0 V.

This circuit seems to have several unnecessary parts. Q1, D3 and R2 could be eliminated and the V_{ADJ} simply applied to R1 where Q1 was connected. One potential problem with this circuit is the high parasitic capacitance at V_{out}. This circuit was used with non-Schottky diodes with poor results. While awaiting delivery of the Schottky diodes another test circuit specified in the PMI data sheet was built with non-Schottky diodes. The results were better, but were not acceptable until the Schottky diodes were installed.

Figure 6-5 shows the Settling Time and Propagation Delay Circuit that yielded the best results. The major advantage of this circuit is the lower parasitic capacitance made possible by the addition of Q1. Q2 isolates the clamping node from the scope probe capacitance.

The 0.1 uf bypass capacitor at V_L should be a BX ceramic and be as close as possible to RL. The Schottky diode GEOS used was a Motorola MBD501.

The key to measuring 100 nsec settling time is avoid saturation of the oscilloscope preamp. This can be accomplished in two ways. One way is to use a sampling preamp such as a Tektronix 3S1 and to advance the delay vernier to read the settling time. Since the sampling preamp only samples what is displayed, saturation of the preamp is avoided by not displaying that level. Another way to avoid saturation of the preamp is to use a differential comparator preamp such as the Tektronix 7A13, which, at the 1 mv./div. sensitivity, will not saturate until the signal exceeds ± 800 millivolts. GEOS used the former approach.

Slew Rate Test Circuit

Reference Amplifier Input Slew Rate is the measure of the maximum rate of change of the output current. Figure 6-6 shows the Slew Rate Test Circuit recommended by the JC-41 Committee. With all bits high, the reference current is stepped from 0 mA to 2 mA while V_{out} is monitored with an oscilloscope. The test is repeated with all bits low while monitoring V_{out}. This test circuit operated properly using a voltage source with a 50Ω source impedance, 50Ω coax and a 50Ω terminator. The 15 pf capacitor at pin 16 is a compensation capacitor for the op-amp (used as a voltage-to-current converter). The fast slew rate that is achieved in this configuration would not be obtained in the fast settling configuration. The compensation capacitor is selected according to the user's need (fast slew rate or fast settling time).

Comments on Test Parameters

Laboratory evaluation of the DAC08 revealed no apparent anomalies with the device. The test parameters recommended by the JC-41 Committee are adequate, although two additional parameters are recommended by Ordnance Systems. The first is a test for V_{LC}, a logic control signal that permits interfacing with several types of logic control. This should be a 100% test, since it checks the functional operation of the device. A second test recommended is that of output glitching. Ordnance Systems has not tested glitching in this initial effort, but it is recommended for follow-on action. Due to the difficulty of performing the test, it should be a sample or qualification test to establish some form of control for this characteristic. The JC-41 Committee has been informed of these recommendations; the vendors do not presently test for these parameters in their own facilities, but would consider a test circuit proposal for the V_{LC} test. (This will be developed by Signetics for consideration by all.) They would prefer to have the glitch test done during device characterization, and not have a test for it in the JAN spec. However, they do recognize the need to have some form of control for new vendors, or for device redesigns.

Devices Used For Testing

Devices used for testing were obtained by two methods: (1) a request for 10 devices from each manufacturer was made by RADC, this group being identified as the "industry sample"; (2) small quantities were purchased through standard Ordnance System procurement procedures from distributors, this group being identified as the "purchased sample".

Industry sample

DAC08		1508	
Signetics	20 devices	AMD	10 devices
AMD	10	Datel	15
Datel	15	PMI	20
Fairchild	13		45
PMI	20		
	78		

Late arrivals

Motorola	10	Motorola	10
National	10		55
	98		

Purchased sample (GEOS and RADC)

DAC08		1508	
Signetics	13 devices	Signetics	3
AMD	8	Fairchild	3
Fairchild	3	PMI	3
PMI	13	Motorola	3
	37		12

The industry sample was first tested by Signetics, who volunteered to do the testing at their facility, using their standard factory test program (Signetics also chairs the JC-41 Subcommittee on Data Converters). The "late arrivals" identified above were not included in the Signetics test group.

Ordnance Systems tested two groups of devices... 33 devices from the purchased sample, and five devices from the industry sample. Data sheets which have a "manufacturer code" heading of "XXXX" are from the industry sample; all others are from the purchased sample. There is no correlation between the serial numbers in the two test groups, since each were assigned at different companies at different times.

Static data was taken on 49 samples. The static data includes a linearity plot of all 256 points for both the I_o and $\bar{I}_o$ outputs at three temperatures (294 linearity plots). Bench data on at least 15 devices was also taken for all dynamic tests.

6.4 Automatic Test Development

Software was developed for the Tektronix S-3263 Test System to provide for automatic test of the DAC-08. All the static tests recommended by the JC-41 Committee plus some additional static tests were included in the software development.

General Static Testing

Figure 6-3 shows the test circuit for the static tests performed on the on the S-3263. Unless otherwise specified pin 11 is connected to + 15 Vdc, pin 12 is connected to -15 Vdc, K3b is switched to ground, K1 is switched to the MN2001, K3a is closed, K4 is switched to ground, pin 15 is grounded, pin 13 is connected to + 15 Vdc, pin 14 is connected to - 15 Vdc and pin 10 is grounded.

A calibration program is always run at the start of testing to assure proper adjustment of zero and full scale outputs levels of the reference DAC. Potentiometers are adjusted, when necessary, to provide negligible gain and offset error.

The test begins with positive and negative supply currents being checked with all bits high and all bits low.

An offset measurement is then performed with K3a open and K4 switched to the reference DAC with its inputs set to all zeros. The offset is subtracted out to improve measurement accuracy when necessary.

Full scale current out of I_o and $\overline{I_o}$ is measured using the reference DAC at its calibrated full scale setting. Offset correction is performed on the result.

A second offset measurement is performed with K4 switched to ground.

Zero scale current out of I_o and $\overline{I_o}$ is then measured with K4 switched to ground. Offset correction (using the second offset measurement) is also performed on the result.

Power supply sensitivity tests are run as described in section 6.1.

An offset measurement at pin 26 with K3 open is performed in preparation for the output current range test which uses + 30V and -5V power supplies for OA1.

The Output Current Range Test is then performed with a -5V negative supply while using a +15V reference. The same test is repeated with a -7V negative supply while using a +25V reference. The measurement is made on output pin 26 with +30V and -5V power supplies on OA1. Both outputs of the DAC-08 are checked.

The Reference Bias Current of the op-amp which is internal to the DAC-08 is measured at pin 10. The tester forces 0V and measures the current.

High Level Input Current, which is leakage current, is measured for each digital input. Low Level Input Current, which is base current, is also measured for each digital input.

Another pair of offset measurements at pin 24 are performed with K3 open and the reference DAC set at zero. These measurements are made with +18V and -10V common mode voltages at OA1 which are used for the voltage compliance tests.

The +18V Compliance Test is performed on both outputs by setting pin 15 to +18V and measuring full scale current. The -10V Compliance Test is performed similarly with pin 15 at -10V.

Linearity and Monotonicity Testing

For measuring DAC-08 linearity error the S-3263 compares the linearity of a reference DAC with the linearity of the DAC under test. This test measures relative bit weight difference (RBWD). Referring to Figure , one can see that the difference in bit weights is linearly related to the significance of the bits. For perfect linearity and no offset error, the relative bit weight difference is linearly related to how significant that bit is and is due to the difference in gains. Any error from this linear relationship is, therefore, due to linearity error, assuming an insignificant linearity error for the reference DAC.

Two basic techniques for measuring linearity error are utilized. The first technique checks only the weight of each bit and proceeds to show that there is no bit weight interaction.

The question that now arises is what assurance does one have that there is no bit weight interaction. That is, when one activates one bit alone and determines its weight that same bit may have a slightly different weight when any or all other bits are activated. The converter industry tries to answer this question by summing the positive and negative deviations and comparing it to the deviation with all bits activated. The all bits "on" state mathematically forces the difference in positive and negative bit weight deviations to zero. The difference between the summed positive and negative deviations is a measure of the bit weight interactions. This approach assumes no cancellation effects in the all bits "on" state. That is, one bit weight may rise due to one interaction while another bit may drop due to another interaction, so that a worse case linearity error can occur only for a certain bit combination. The only way to check for that phenomenon is to check each digital word, which is our second approach.

The technique for checking linearity at each digital word is as follows:

1. As in the first technique, establish a theoretical straight line between all bits "on" and all bits "off". Since the reference DAC will be used, all measurements will be relative to the reference DAC.

2. All digital word values will then be predicted by on-line calculations and errors relative to the theoretical straight line determined.

The all bits "on" state is used to establish the theoretical straight line because the gain and adjustments are usually performed by the user for that condition. Therefore, any argument that it is not the best straight line is purely academic.

The offset errors are also a concern. The offsets of the DAC under test, the reference DAC and the op amps are simply measured all at once and subtracted out of each measurement as part of the data manipulation in software.

The basic steps used in the S-3263 software to accomplish the first technique are as follows:

1. Set the device under test (D.U.T.) to all bits "off" and the reference DAC to all bits "off" and measure the combined offset (V_{COS}).

2. Set the D.U.T. to all bits "on" and the reference DAC to the 8 most significant bits "on" and determine the full scale difference (FSD) by subtracting V_{COS} from the measured value (V_{error}) and dividing by 100,000 ohms (20 x 5,000 ohms).

$$I_{FSD} = \frac{V_{error_T} - V_{COS}}{100,000 \text{ ohms}} \quad \text{amps}$$

3. Set the D.U.T. and reference DAC to all bits "off" except the most significant bit (MSB). Subtract V_{COS} from the measured value (V_{error}) and divide by 100,000 ohms.

$$I_{RBWD_1} = \frac{V_{error_1} - V_{COS}}{100,000 \text{ ohms}}$$

4. The linearity error is calculated as follows:

$$NL_1 = \frac{I_{RBWD_1} - \left(\frac{256}{255} \times \frac{1}{2} \times I_{FSD}\right)}{I_{FS}}$$

5. Repeat steps 3 and 4 with the second most significant bit and replace $(1/2)^1$ with $(1/2)^2$.

6. Repeat 5 for the other N^{th} bits using the appropriate $(1/2)^N$ factor.

7. To check for worst case linearity error

$$\Sigma NL^+ = 0 \pm .19\% \quad \text{(for DAC-08 only)}$$
$$\Sigma NL^- = 0 \pm .19\% \quad \text{(for DAC-08 only)}$$

8. To assure an insignificant amount of bit interaction

$$\Delta \Sigma NL = |\Sigma NL^+| - |\Sigma NL^-| = 0 \pm .05\% \text{ (for DAC-08 only)}$$

9. For the case where bit interaction is near the limit, a tighter bit weight error limitation is required as follows:

$$|\Sigma NL^+| - |\Delta \Sigma NL| = 0 \pm .19\% \text{ (for DAC-08 only)}$$
$$|\Sigma NL^-| - |\Delta \Sigma NL| = 0 \pm .19\% \text{ (for DAC-08 only)}$$

The next approach checks every digital word using the following steps:

1. Determine V_{COS} and I_{FSD} as before.

2. Step the D.U.T. from 00000001 to 11111110 and calculate the non-linearity at each digital word. For example, for the 00000011 input the non-linearity is given by

$$NL_3 = \frac{\left(\frac{V_{error} - V_{COS}}{100{,}000 \text{ ohms}}\right)\left(\frac{3 \times I_{FSD}}{256}\right)}{I_{FS}} = 0 \pm .19\% \quad \text{(for DAC-08 only)}$$

where I_{FS} is the full scale current out of the D.U.T. and is 2 mA. Of course, this is only the non-linearity relative to the reference DAC, but, since its linearity is .003% or better, the difference is not that significant. This test should also check for monotonicity at each point. The monotonicity calculation going from 00000010 to 00000011 is

$$\% \text{ Change} = \frac{V_{error_3} - V_{error_2} - V_{COS}}{100{,}000\ I_{FS}} = 0 \text{ to } 0.8\% \text{ (2 LSB)}$$

The converter industry uses the bit interaction check to substantiate checking only the major carries for monotonicity. The data from every point will determine the validity of their approach.

As for the way of presenting the linearity data, a horizontal plot of the non-linearity of 255 points provides a good visual profile of the DAC performance. This plot also indicates if there is any monotonicity problem. A sample plot of the data points is shown in Figure 6-8.

6.5 Evaluation of Data

6.5.1 Dynamic Test Data

Settling Time and Propagation Delay Data

Table 6-1 lists the bench data taken on devices from five manufacturers. All vendors except for vendor H had little or no problems with meeting the 135 nanosecond settling times. The vendor H devices also exhibited a 20 mV dip near the settling area of the curve which increased their total settling time for T_{SHL}.

The same test circuit was used to make propagation delay measurements. Table 6-3 shows that all the vendors' devices checked had prop delays in the range of 30-50 nsec, except for the vendor H device which was close to the 60 nsec limit. The typical settling time waveforms, shown in Figure 6-9, exhibit typical propagation delays for both transitions.

Slew Rate

Using the slew rate test circuit shown in Figure 6-6, slew rate data was taken on 13 devices from the purchased sample, and 5 devices from the industry sample. All of the data exceeded the minimum value of 1.5 mA/nsec. The data is tabulated in Table 6-4.

6.5.2 Static Test Data

Table 6-5 is a statistical tabulation of the static test data at three temperatures on all 33 samples tested by using wide reject limits. Table 6-6 uses the reject limits proposed by the JC41 Committee to present the statistical data.

Supply Currents

The positive and negative power supply current data indicates that the JC-41 limits are wide enough to avoid nuisance failures.

Full Scale and Zero Scale Current

The full scale current and zero scale current limits are wide enough to avoid unnecessary failures. The mean full scale current was 1.99 mA, which tends to support setting the acceptable range at 1.99 ± .05 mA as proposed.

Power Supply Sensitivity from + V_S and from - V_S

All the power supply sensitivity limits were acceptable. A wider range is justified for the 12 V to 18 V variation than for the 4.5 V to 5.5 V variation, as is already specified.

Output Current Range

Some problems were encountered meeting the limits specified by the JC-41 Committee. The IFSR1 limit of 2.1 mA min. was only a problem for one vendor's devices. The IFSR2 limit of 4.2 mA min. was not realistic for $-V_S$ = -7.0V. Not one device could meet it. The JC-41 D/A converter subcommittee has recently suggested setting $-V_S$ to -12 V instead of -7 V. This new setting has not been specifically tried, but earlier bench tests have indicated that changing $-V_S$ to -8 V or more will allow most devices to meet the 4.2 mA min; therefore, $-V_S$ = -12 V should leave a comfortable margin.

Reference Bias Current

The limits recommended by the JC-41 Committee allow for 0.1 uA of current reversal. This reversal would be caused by approximately 1 uA of leakage current which may be due to surface contamination. The data taken by both Signetics and GEOS indicated no reversal of measured current. GEOS does not see the need for allowing for bias current reversal and would rather be rejecting devices that exhibited bias current reversal. The other end of the limit (-3.0 uA) does not present any problems.

High and Low Level Input Currents

The JC-41 Committee recommended limits for the high level input current (which is really leakage current) only specifies a maximum which is at 10 uA.

The Signetics data does not look sensitive enough to draw any conclusions from. The GEOS data varied from a maximum of + .04 uA to a minimum of - .002 uA. Therefore, GEOS recommends a maximum limit of 1 uA and a minimum limit of - 0.1 uA. The - 0.1 uA allows for leakage current in the test fixture.

The low level input current limit of - 10 uA (minimum) leaves a comfortable margin to avoid nuisance failures. A maximum limit of zero could be provided for the detection of excessive leakage current, but this is already provided by the high level input current test.

Full Scale Current at + 18 V Compliance and - 10 V Compliance

No problems were encountered with the compliance tests. The limits recommended by JC-41 are reasonable and should not lead to nuisance failures.

Change in F.S. Current Due to Voltage Compliance

The 4 uA (1/2 LSB) limit at - 55°C set by the JC-41 Committee for the change in full scale current due to voltage compliance is not easily achieved. In fact, Vendor H exhibits almost ten times that amount. Only Vendor E has no problem meeting the 4 uA limit. In order to avoid poor yields, an 8 uA (1 LSB) limit should be used at -55°C. One manufacturer will still be unable to achieve this limit unless he improves his design. The other five manufacturers should have no problems.

Linearity

Because linearity is the most important characteristic of the DAC-08 a great amount of effort was expended to determine validity of the measurement assumptions and the actual linearity of the devices.

The question concerning bit interaction was "Is the difference of the sum of the positive and the sum of the negative bit errors a conservative measure of bit interaction?" The answer seems to be yes. The worst case linearity was estimated by adding the absolute value of the difference (described above) to the sum of the positive bit errors (to get the positive worst case linearity) and to the sum of the negative bit errors (to get the negative worst case linearity). Comparing these worst case linearities with the actual linearity errors obtained by measuring all 256 digital words, one must conclude the worst case linearity was always considerably worse than the actual linearity error. That is, the bit interaction was never worse than that observed with all bits on.

As for the linearity of the devices, the worst linearity always occurred at -55°C. The positive and negative bit errors exceeded 0.19% only occasionally at -55°C. The Positive and Negative Bit Error Difference (Bit Interaction) had a mean of-0.045% and a standard deviation of 0.003% to 0.004% and rarely exceeded the .05% limit. Positive Relative Accuracy and Negative Relative Accuracy, which is the worst case linearity mentioned earlier, exceeded 0.19% for many devices. In most cases, exceeding this limit did not indicate an actual linearity error greater than 0.19%.

Other notable characteristics that were observed are that the sum of the negative bit errors was almost always larger than sum of the positive bit errors and the actual linearity plots exceeded the sum of the positive bit errors only slightly and rarely exceeded the sum of the negative bit errors.

The data taken by Signetics does not calculate worst case linearity as described earlier, but calculates a worst case word which is the same as the sum of the bit errors (positive and negative).

Monotonicity

The linearity data of all 256 digital words substantiates the industry position that worst case monotonicity (differential linearity) occurs at the major carry points. The largest amount of differential linearity is generally exhibited at the most significant carry or the second most significant carry.

The monotonicity of a converter is guaranteed by establishing a linearity within ± 1/2 of a least significant bit. Therefore, as expected, no problems were encountered with the 16 uA limit to assure monotonicity.

Output Symmetry

The output symmetry of the I_o and $\overline{I}_o$ outputs was well below the 8 uA limit specified.

Full Scale Current Temperature Coefficient

Although Full Scale Current Temperature Coefficient was not specifically included in the static test software program (due to an oversight), some spot checks of this limit indicate no problem at all. The worst TC observed was about 25 PPM/°C (or about half the specified limit of 50 PPM/°C).

Comparison of GEOS and Signetics Static Test Data

An attempt was made to correlate GEOS and Signetics Static Test Data for five randomly selected devices. Table 6-7 tabulates both sets of data. In some cases, such as the Output Current Range Tests, no data was taken by Signetics.

The power supply currents correlate very well. I_{FS}, I_{ZS} and power supply sensitivities correlate poorly. I_{REF} correlates fairly well. High Level Input Current was difficult to correlate due to the low resolution of the Signetics data. Low Level Input Current correlated very well. The voltage compliance is measured by Signetics as a current change due to output voltage changes of 0 to + 18 V and 0 to - 10 V. Therefore, the difference in those measurements should correlate to the change resulting from a 18V to -10 V change as measured by GEOS. In fact, the correlation was very poor. Fair to good correlation was obtained for most of the bit errors except for an obvious difference in sign. The sum of the positive and negative bit errors measured by Signetics correlated fairly well with the GEOS data. The correlation for the difference between positive and negative bit error summations was very poor. The Signetics data was not even close to the limit, while the GEOS data was very close to the limit.

Comparison of GEOS and Signetics Dynamic Test Data

Table 6-8 tabulates GEOS and Signetics data on the same devices. The settling time test data shows fair correlation. The t_{PLH} propagation delay data correlates very well, while the t_{PHL} data correlates poorly. The Reference Amplifier Slew Rate data correlates very poorly. One reason for such disappointing correlation may be the difference in test circuits used. For example, all the GEOS test set-ups used R_L = 1 K ohm, while the Signetics' test set-ups used R_L = 200Ω (settling time), R_L = 50Ω (prop delay) and R_L = 100Ω (slew rate). The R_L used by GEOS was proposed by the JC-41 Committee.

6.6 Conclusions

6.6.1 Static Tests

The following static tests and their limits are acceptable as recommended by the JC-41 D/A Converter Subcommittee (described in Table 6-1):

1. Supply current from + V_s
2. Supply current from - V_s
3. Full scale current
4. Zero scale current
5. Power supply sensitivity from + V_s
6. Power supply sensitivity from - V_s
7. Low level input current
8. Full scale current at + 18 V compliance
9. Full scale current at - 10 V compliance
10. Positive bit errors (NL+)
11. Negative bit errors (NL-)
12. Monotonicity
13. Output symmetry
14. Full scale current temperature coefficient

Output Current Range

The IFSR2 limit of 4.2 mA min is not realistic with - V_s = -7.0V. However, with -V_s = -12V the limit will present no problem with normal devices.

Reference Bias Current

GEOS recommends no bias reversal be allowed by the reject limits. All data measurements indicated no need to accept such devices which may indicate excessive surface contamination. Therefore, reference bias current limits should be from -3.0 uA to 0 uA.

High Level Input Currents

Since this is really leakage current and GEOS data indicated maximum of + .04 uA, the maximum limit should be reduced to + 2 uA to avoid accepting devices with excessive surface contamination. Since the lowest level measured was -.002 uA, GEOS recommends a minimum limit of - 0.01 uA so as to allow for possible leakage current in the test fixture. Therefore, the High Level Input Current limits should be + 2 uA to -0.01 uA instead of the + 10 uA to 0 uA recommended by the JC-41 Committee.

Change in F.S. Current Due to Voltage Compliance

GEOS data on this parameter indicates the need to increase the limit at -55°C from 4 uA to 8 uA to avoid yield problems.

Positive and Negative Bit Error Difference

All measurements taken by GEOS have a mean value of about -0.04% and a standard deviation of 0.003% to 0.004%. Looking at Table 6-5 one sees that the Signetics data was not even close to the GEOS data. Since the GEOS data exhibits this mean of -.04% and the expected mean is zero, it may be that the GEOS data is erroneous. On the other hand, a bias in the bit interaction (inherent in the device design) is also possible. It is recommended that additional effort be applied in order to identify the reason for the bias.

Positive and Negative Relative Accuracy

The positive/negative relative accuracy is calculated by adding the difference of the summations of the positive and negative bit errors to the positive/negative bit error summation. Since the positive and negative bit error difference data is questionable, it is impossible to draw any conclusions on the validity of this measurement or the need for it. If the GEOS data is erroneous and the Signetics data is valid, the positive and negative relative accuracy would be very close to the positive and negative bit error summations. On the other hand, if the GEOS data is valid and the Signetics data is erroneous, it appears that this parameter is simply a super conservative estimate of the worst-case linearity error.

6.6.2 Dynamic Tests

Using the Settling Time and Propagation Delay Test Circuit shown in Figure 6-5, the maximum limit settling time of 135 nsec and the maximum limit for propagation delay of 60 nsec are acceptable. Checking both $\overline{I_o}$ as well as I_o for these two tests is recommended in spite of the fact that equal or faster times were observed at $\overline{I_o}$. The slew rate limit of 1.5 mA/usec is also acceptable when tested according to Figure 6-6, but a slew rate check in both the on and off direction is recommended.

6.6.3 Recommended Additional Tests

Zero Scale Current Temperature Coefficient

If the data taken for the zero scale current test at the three temperatures was used to calculate the zero scale current temperature coefficient, the user would be able to calculate the worst case gain and offset temperature coefficient. Since this does not mean an additional test and it may have some value to the user, it is recommended by GEOS.

Output Glitch

Output glitches are caused by unequal turn-on/turn-off times in D/A converter switches. For example, when going from an input word of 10000000 to an input work of 01111111, an intermediate state of 00000000 or 11111111 is possible depending on the mismatch in response time of the switches. Ordnance Systems has not tested glitching in this initial effort, but it is recommended for follow-on action. Due to the difficulty of performing the test, it should be a sample or qualification test to establish some form of control for this characteristic.

Logic Level Control Input

The logic level control input, labeled V_{cc}, controls the input threshold of the switches so that direct inputs from various digital logic families can be used. The test of this control input should be a 100% test since it checks functional operation of the device.

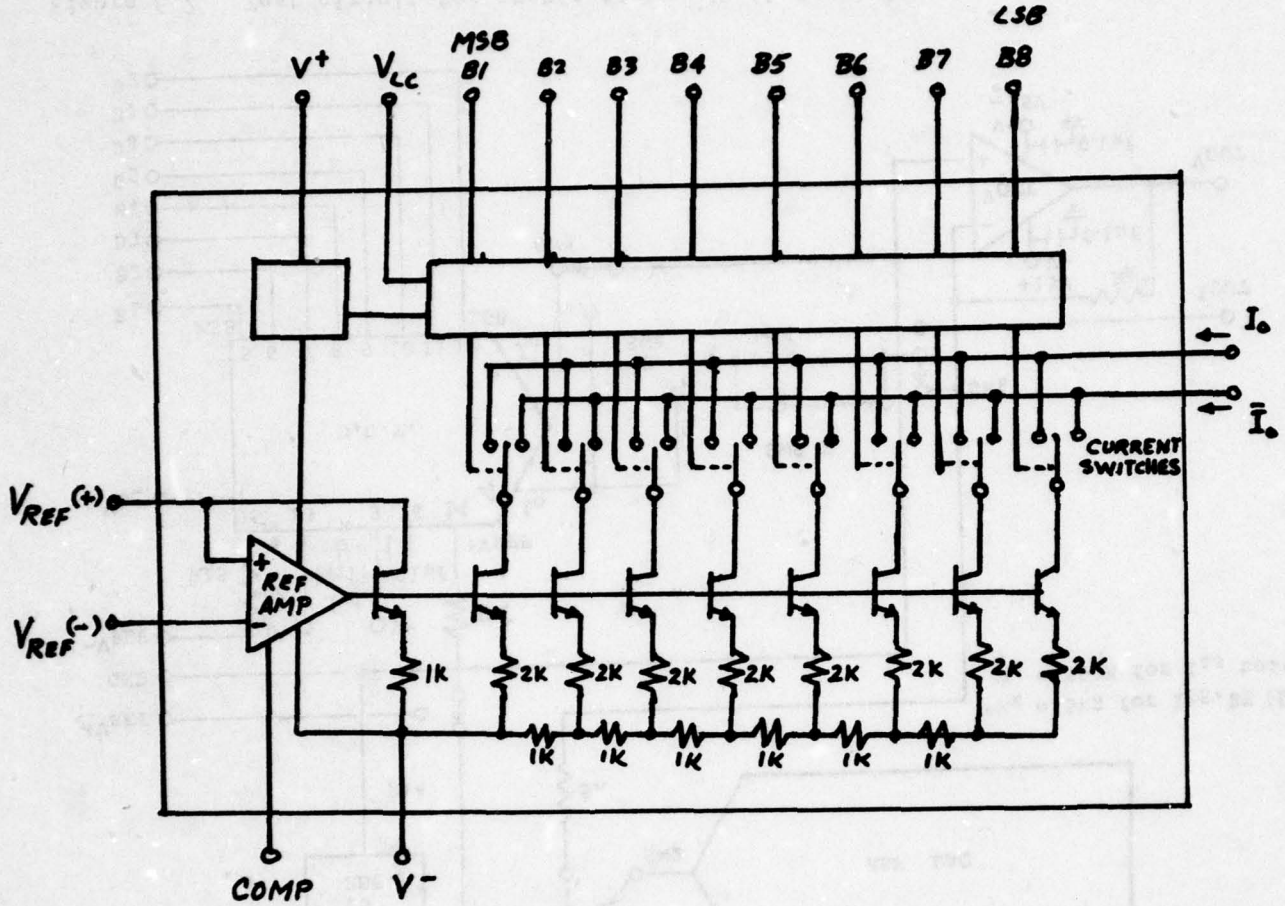


FIGURE 6-1 FUNCTIONAL BLOCK DIAGRAM

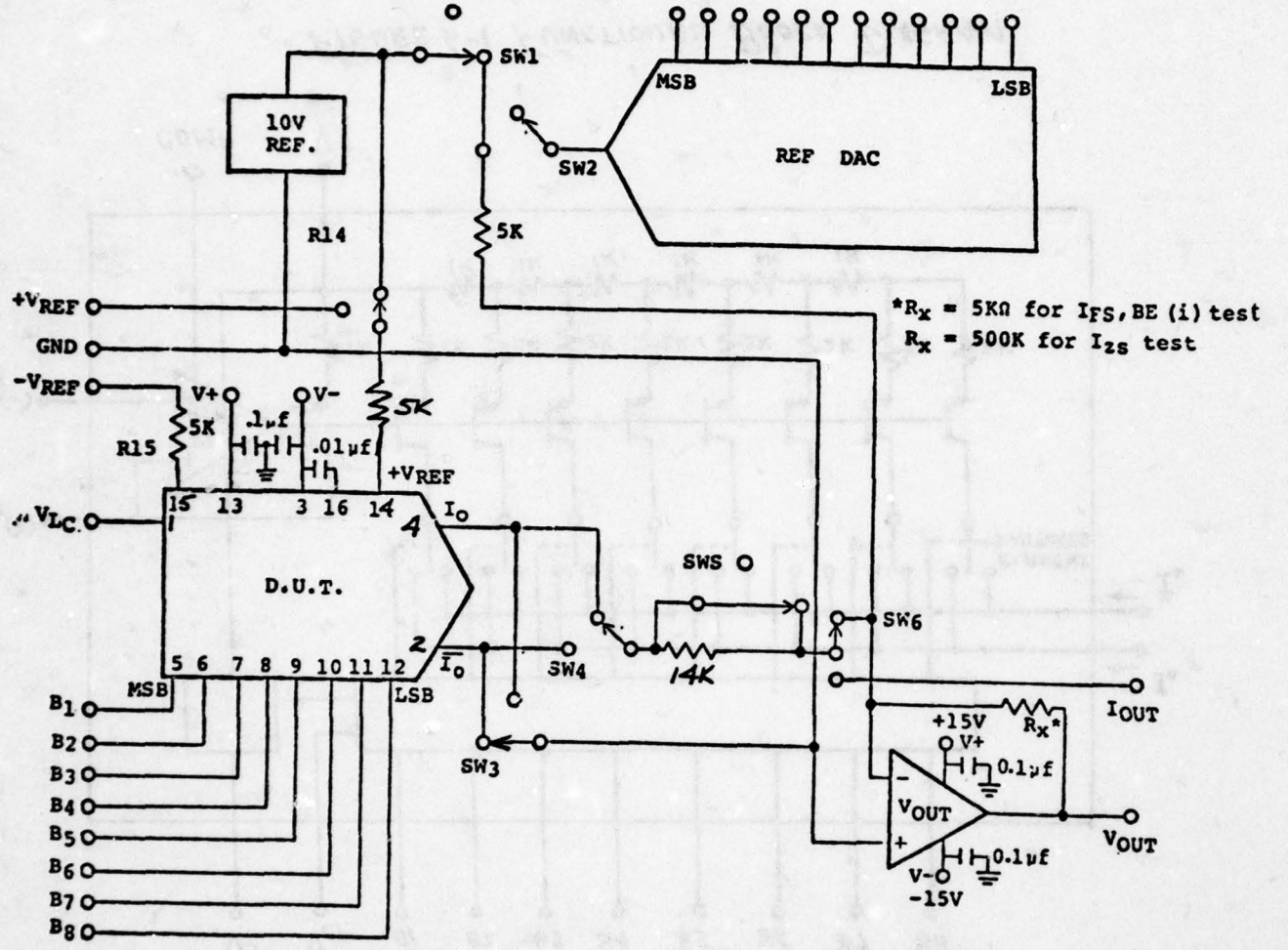


Figure 6.2. Test circuit for static tests, JC-41 Committee.

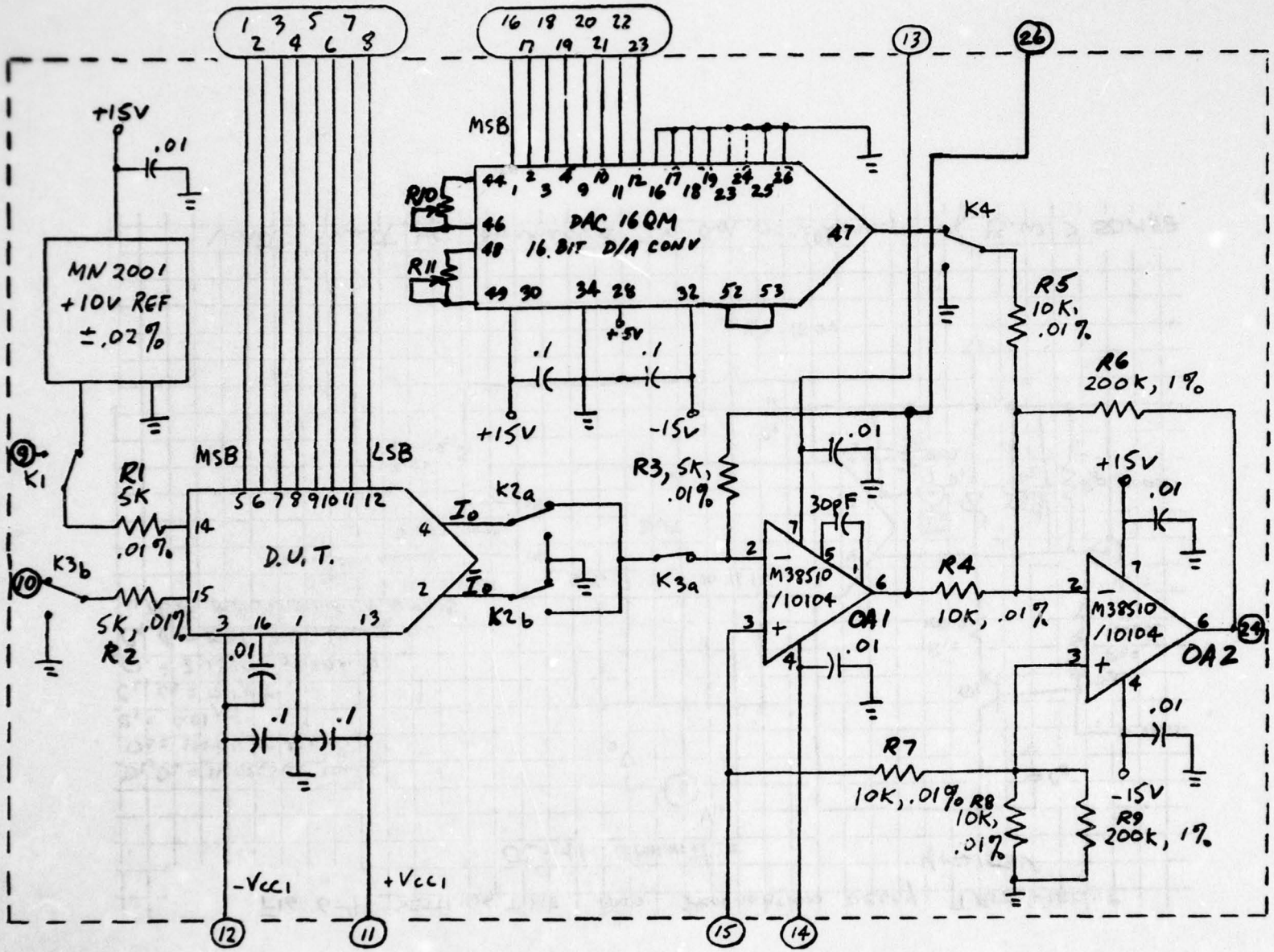
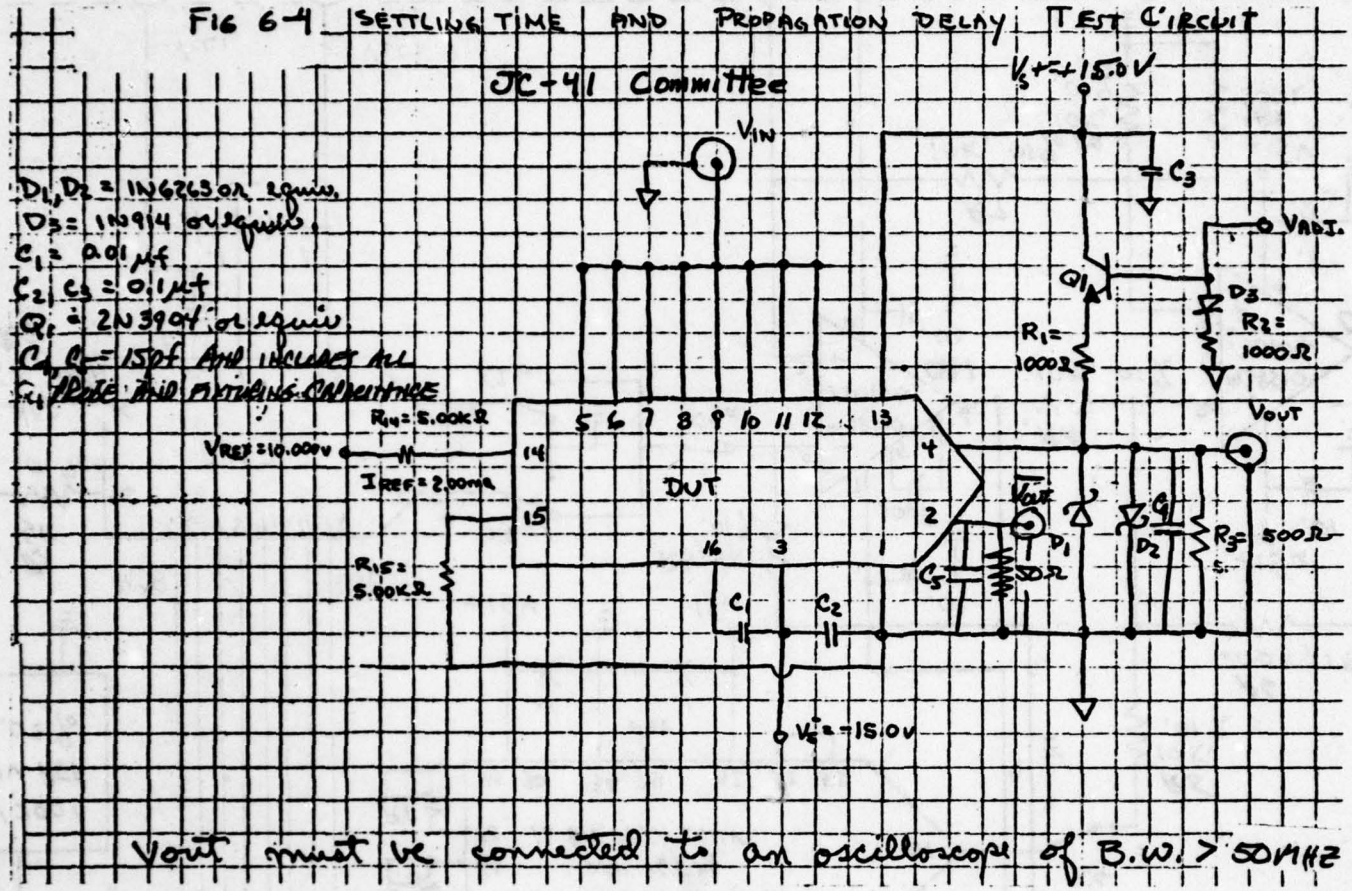


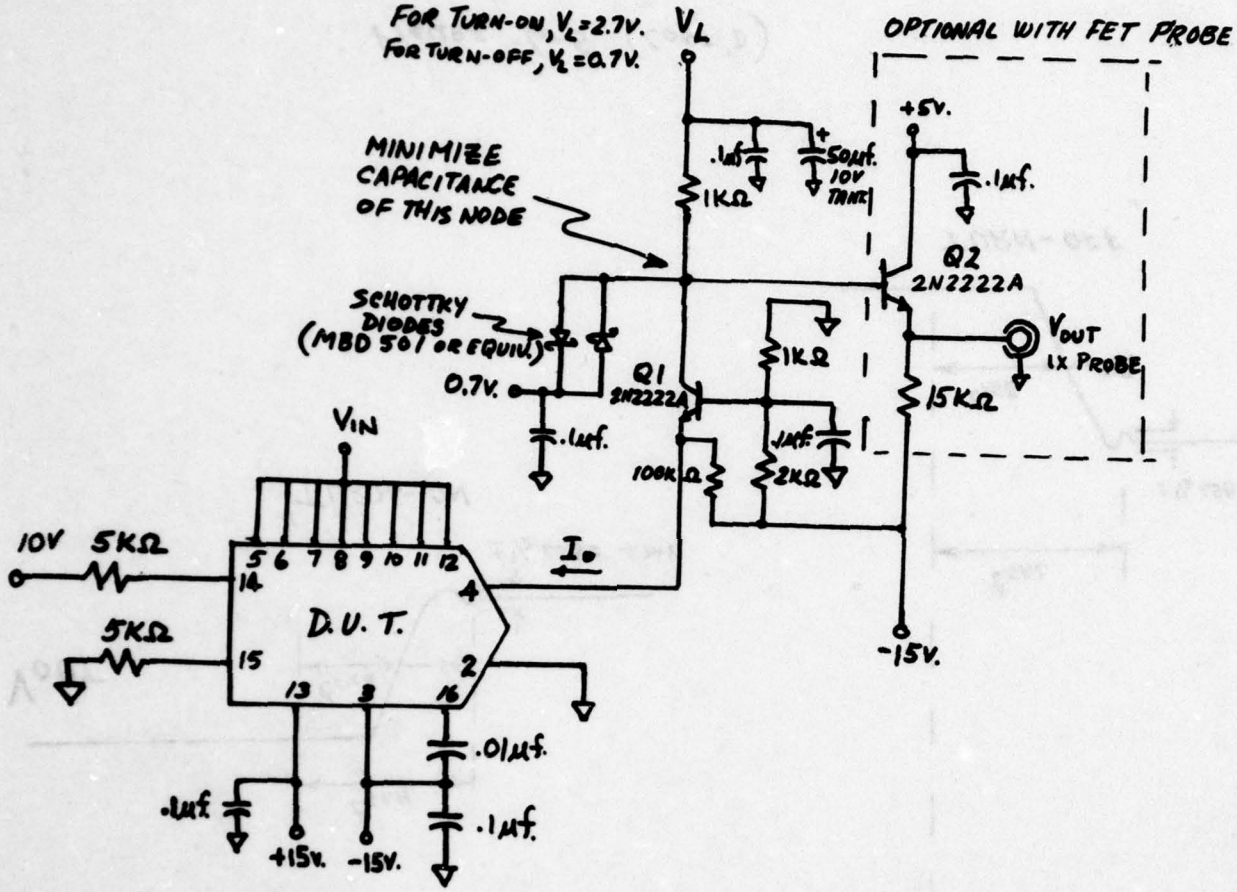
Figure 6-3 Test circuit for static tests, GEOS

FIG 6-4 SETTLING TIME AND PROPAGATION DELAY TEST CIRCUIT

JC-41 Committee



Vout must be connected to an oscilloscope of B.W. > 50MHz



NOTES: 1. USE OSCILLOSCOPE WITH 50 MHZ MINIMUM BANDWIDTH.
2. SATURATION OF PREAMP SHOULD BE AVOIDED.

FIGURE 6-5 SETTLING TIME AND PROPAGATION TIME

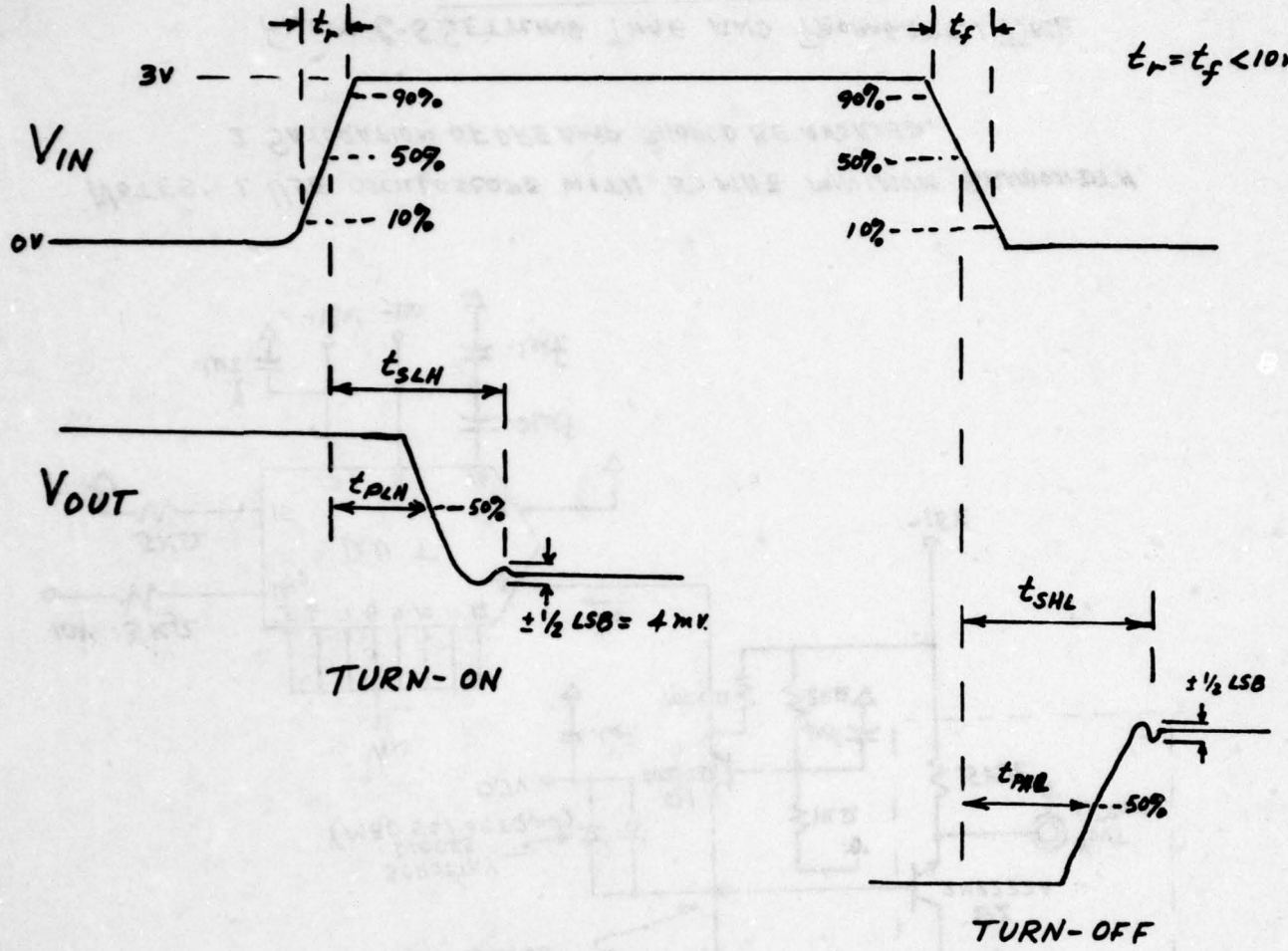


FIGURE 6-5 (CONT'D)

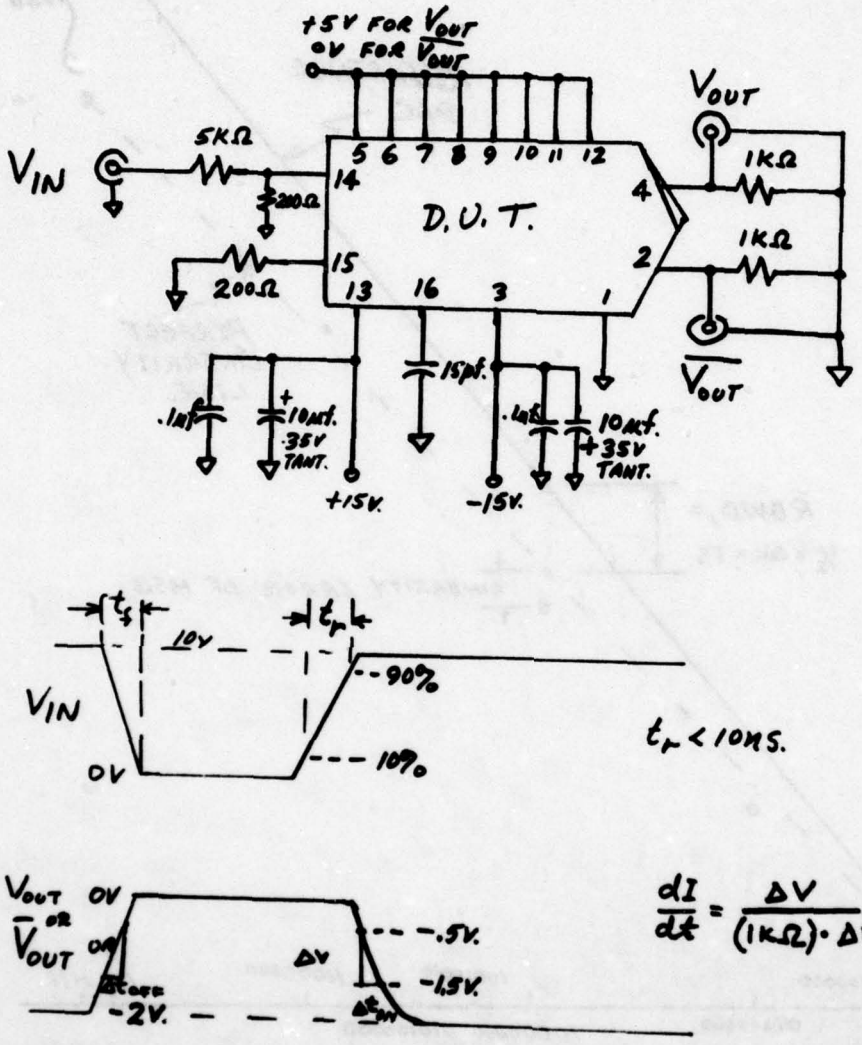
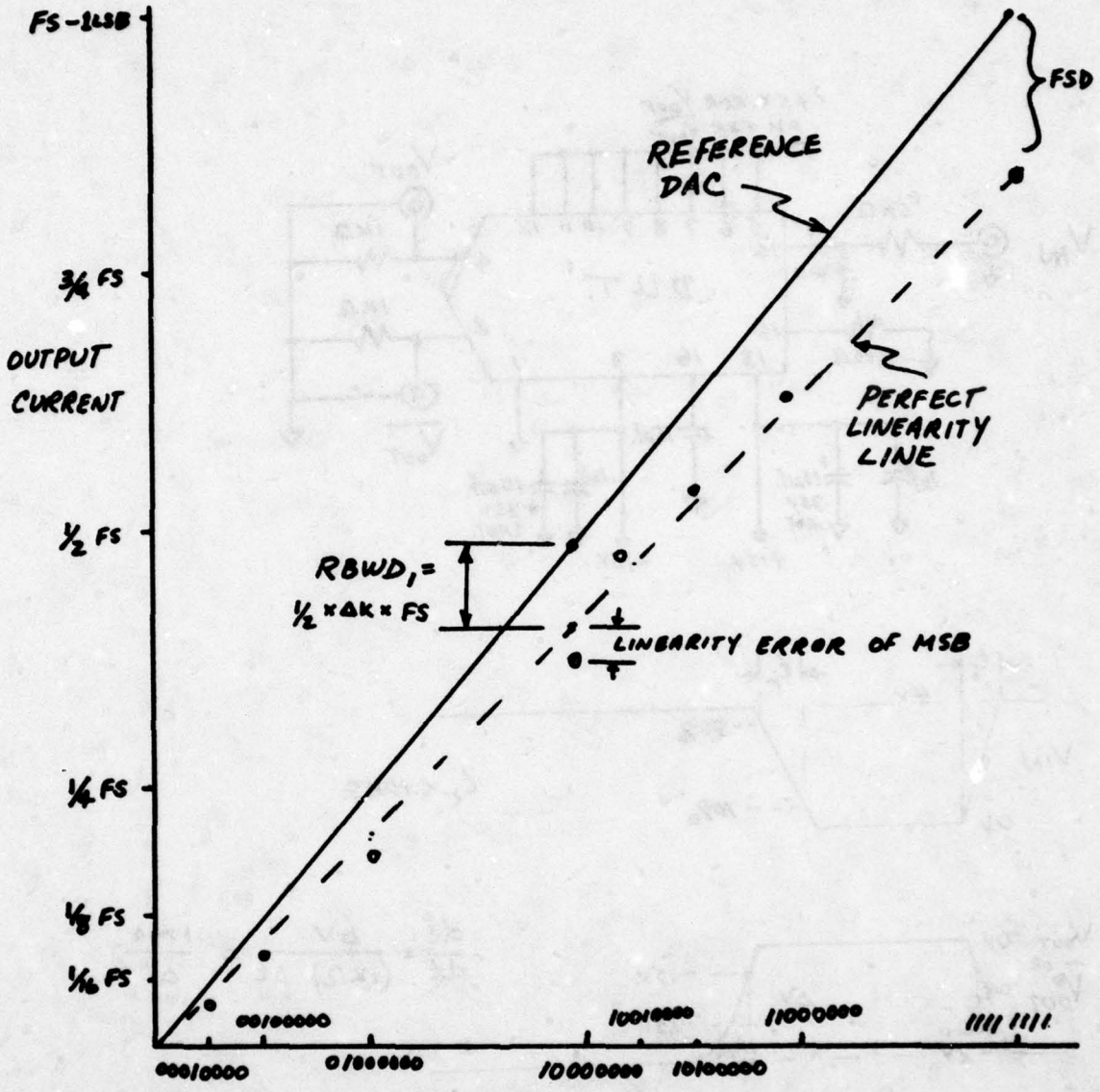


FIGURE 6-6 SLEW RATE



NOTES:

1. RBWD IS RELATIVE BIT WEIGHT DIFFERENCE.
2. ΔK IS THE GAIN DIFFERENCE BETWEEN REFERENCE AND D.U.T.
3. DATA POINTS FROM THE D.U.T. ARE SHOWN AS CIRCLES.

FIGURE 6-7 - LINEARITY MEASUREMENT

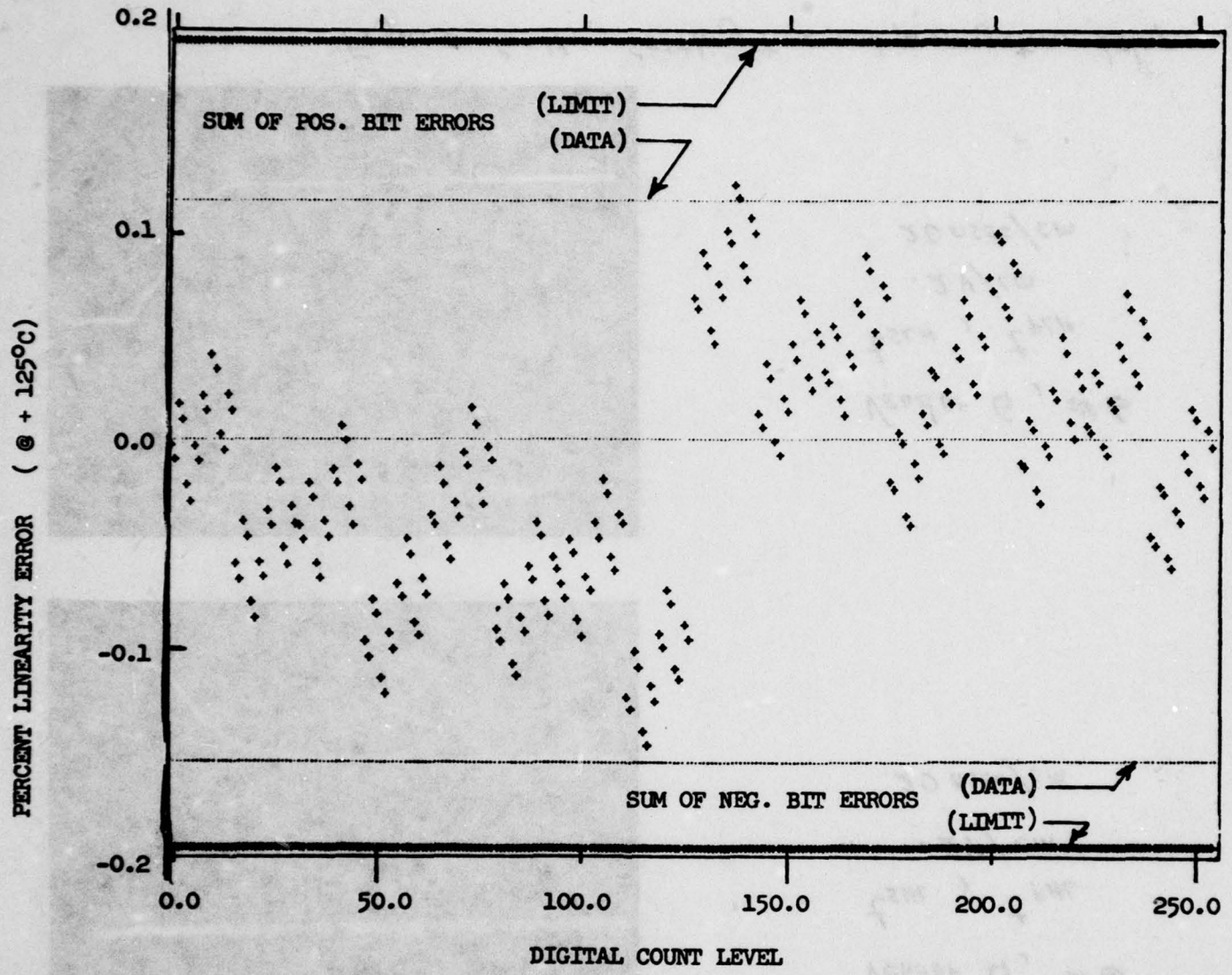
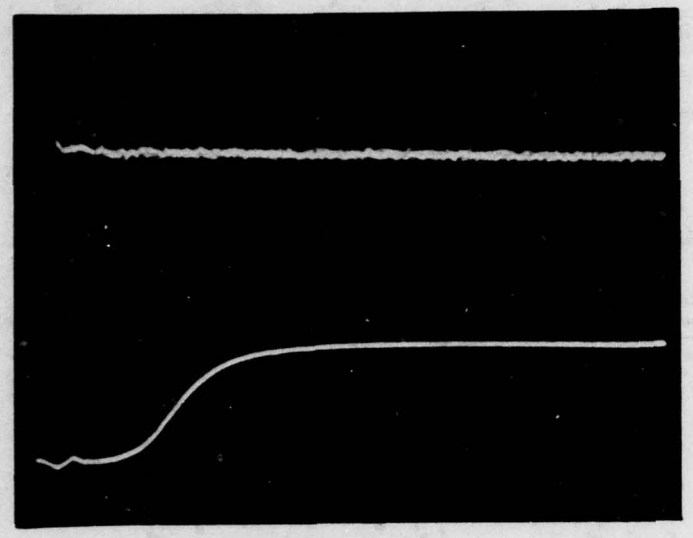


Figure 6-8. DAC08 D/A Converter Linearity/Bit-Weight-Interaction Plot.

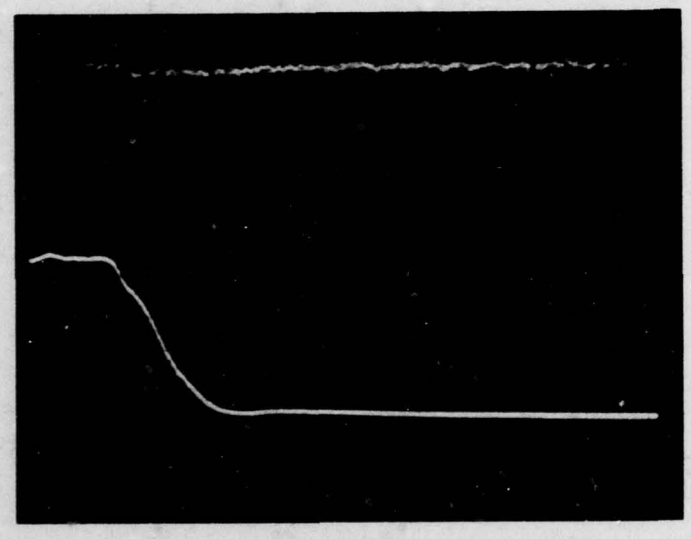


Vendor G, #6

t_{SHL} , t_{PHL}

.2V/cm

20 nsec/cm



Vendor G , #6

t_{SLH} , t_{PLH}

.2V/cm

20nsec/cm

Figure 6-11 Settling time and propagation delay

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 01)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS MIN	LIMITS MAX	UNITS
Supply Current From +VS	I+	All input Bits High	0.4	3.8	mA
Supply Current From -VS	I-	All input Bits High	-7.8	-0.8	mA
Full Scale Current	IFS	All input Bits High, 2/ Measure I_O All input Bits Low, Measure $\overline{I}_O$	1.94	2.04	mA
Zero Scale Current	IZS	All input Bits Low, Measure I_O All input Bits High, Measure $\overline{I}_O$	-2.0	+2.0	uA
Power Supply Sensitivity From +VS	PSSIFS+1	+VS=+4.5V to +5.5V, -VS =-18V All input Bits high, Measure I_O All input Bits Low, Measure $\overline{I}_O$	-4.0	+4.0	uA
	PSSIFS+2	+VS=+12V to +18V, -VS= -18V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	-8.0	+8.0	uA
Power Supply Sensitivity From -VS	PSSIFS-1	+VS = +18V, -VS = -12V to -18V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	-8.0	+8.0	uA
	PSSIFS-2	+VS=18V, -VS=-4.5V to -5.5V R14 = R15 = 10.000KΩ All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	-2.0	+2.0	uA
Output Current Range	IFSR1	-VS=-5.0V, VREF=+15V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	2.1		mA
	IFSR2	-VS = -7.0V, VREF = +25V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	4.2		mA
Reference Bias Current	IREF-	All input Bits Low	-3.0	+0.1	uA
High Level Input Current	IIH	All input Bits VIN = +18V, Each input measured separately		10	uA
Low Level Input Current	IIL	All input Bits VIN = -10V, Each input measured separately	-10.		uA

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 01)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS		UNITS
			MIN	MAX	
Full Scale Current at +18V Compliance	IFS+	$VI_O = \overline{VI}_O = +18V$ All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	1.90	2.08	mA
Full Scale Current at -10V Compliance	IFS-	$VI_O = \overline{VI}_O = -10V$ All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	1.90	2.08	mA
Change in full scale current due to voltage compliance	ΔIFSC	VI_O = +18V to -10V, Measure I_O $\overline{VI}_O$ = +18V to -10V, Measure $\overline{I}_O$	-4.0	+4.0	uA
Positive Bit Errors	ΣNL+	(Σ Positive Bit Errors)/IFS, Measure I_O and $\overline{I}_O$ 3/		0.19	%
Negative Bit Errors	ΣNL-	(Σ Negative Bit Errors)/IFS, Measure I_O and $\overline{I}_O$ 3/	-0.19		%
Positive & Negative Bit Error Difference	$\Delta\Sigma$NL	$\lvert\Sigma NL+\rvert - \lvert\Sigma NL-\rvert$	-0.05	+0.05	%
Positive Relative Accuracy	NL+	$\lvert\Sigma NL+\rvert + \lvert\Delta\Sigma NL\rvert$		0.19	%
Negative Relative Accuracy	NL-	$\lvert\Sigma NL-\rvert + \lvert\Delta\Sigma NL\rvert$		0.19	%
Monotonicity	Δ(i)	$(I_{on} - I_{on-1}) \geq 0$ at each major carry point. 4/ Measure I_O and $\overline{I}_O$	0	16.	uA
Output Symmetry	ΔIFS	IFS - $\overline{IFS}$	-8.0	+8.0	uA
Full scale current Temp. Coefficient	TC(IFS)	Measure Io and $\overline{I}_O$	-50.	+50.	ppm/°C
Propagation Delay time, High-To-Low level	tpHL	Fig. 2, all bits switched simultaneously, Measure $\overline{V}_O$	6	60	nS
Propagation Delay time, Low-To-High level	tpLH	Fig. 2, all bits switched simultaneously, Measure $\overline{V}_O$	6	60	nS
Reference amplifier input slew rate	dI/dt	Fig. 3	1.5		mA/uS
Settling Time, High-To-Low Level	tsHL	Fig. 2, output within 1/2 LSB of Final Value of I_O	10	135	nS
Settling Time, Low-To-High Level	tsLH	Fig. 2, output within 1/2 LSB of final value of I_O	10	135	nS

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 02.)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS MIN	LIMITS MAX	UNITS
Supply Current From +VS	I+	All input Bits High	0.4	3.8	mA
Supply Current From -VS	I-	All input Bits High	-7.8	-0.8	mA
Full Scale Current	IFS	All input Bits High, 2/ Measure I_O All input Bits Low, Measure $\overline{I_O}$	+1.984	+2.000	mA
Zero Scale Current	IZS	All input Bits Low, Measure I_O All input Bits High, Measure $\overline{I_O}$	-1.0	+1.0	uA
Power Supply Sensitivity From +VS	PSSIFS+1	+VS=+4.5V to +5.5V, -VS = 18V All input Bits high, Measure I_O All input Bits Low, Measure $\overline{I_O}$	-4.0	+4.0	uA
	PSS$\overline{IFS}$+2	+VS=+12V to +18V, -VS= -18V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I_O}$	-8.0	+8.0	uA
Power Supply Sensitivity From -VS	PSSIFS-1	+VS = +18V, -VS = -12V to -18V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I_O}$	-8.0	+8.0	uA
	PSS$\overline{IFS}$-2	+VS=18V, -VS=-4.5V to -5.5V, R14 = R15 = 10.000KΩ All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I_O}$	-2.0V	+2.0	uA
Output Current Range	IFSR1	-VS=-5.0V, VREF=+15V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I_O}$	2.1		mA
	IFSR2	-VS = -7.0V, VREF = +25V All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I_O}$	4.2		mA
Reference Bias Current	IREF-	All input Bits Low	-3.0	+0.1	uA
High Level Input Current	IIH	All input Bits VIN = +18V, Each input measured separately		10	uA
Low Level Input Current	IIL	All input Bits VIN = -10V, Each input measured separately	-10		uA

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 02.)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS MIN	LIMITS MAX	UNIT
Full Scale Current at +18V Compliance	IFS+	$VI_O = \overline{VI}_O = +18V$ All input Bits High, Measure I_O All input Bits Low, Measure $\overline{I}_O$	1.90	2.08	mA
Full Scale Current at -10V Compliance	IFS-	$VI_O = \overline{VI}_O = -10V$ All input Bits High, Measure I_O All input Bits Low, Measure I_O	1.90	2.08	mA
Change in full scale current due to voltage compliance	ΔIFSC	VI_O = +18V to -10V, Measure I_O $\overline{VI}_O$ = +18V to -10V, Measure $\overline{I}_O$	-4.0	+4.0	uA
Positive Bit Errors	ΣNL+	(Σ Positive Bit Errors)/IFS, Measure I_O and $\overline{I}_O$ 3/		0.1	%
Negative Bit Errors	ΣNL-	(Σ Negative Bit Errors)/IFS, Measure I_O and $\overline{I}_O$ 3/	-0.1		%
Positive & Negative Bit Error Difference	$\Delta\Sigma$NL	$\lvert\Sigma NL+\rvert - \lvert\Sigma NL-\rvert$	-0.03	+0.03	%
Positive Relative Accuracy	NL+	$\lvert\Sigma NL+\rvert + \lvert\Delta\Sigma NL\rvert$		0.10	%
Negative Relative Accuracy	NL-	$\lvert\Sigma NL-\rvert + \lvert\Delta\Sigma NL\rvert$		0.10	%
Monotonicity	Δ(i)	$(I_{on} - I_{on-1}) > 0$ at each major carry point. 4/ Measure I_O and $\overline{I}_O$	0	16	uA
Output Symmetry	ΔIFS	$IFS - \overline{IFS}$	-4.0	+4.0	uA
Full scale current Temp. Coefficient	TC(IFS)	Measure I_O and $\overline{I}_O$	-50.	+50.	ppm/°C
Propagation Delay time, High-To-Low level	tpHL	Fig. 2, all bits switched simultaneously, Measure $\overline{V}_O$	6	60	nS
Propagation Delay time, Low-To-High level	tpLH	Fig. 2, all bits switched simultaneously, Measure $\overline{V}_O$	6	60	nS
Reference amplifier input slew rate	dI/dt	Fig. 3	1.5		mA/uS
Settling Time, High-To-Low Level	tsHL	Fig. 2, output within 1/2 LSB of Final Value of I_O	10	135	nS
Settling Time, Low-To-High Level	tsLH	Fig. 2, output within 1/2 LSB of final value of I_O	10	135	nS

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 03)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS MIN	LIMITS MAX	UNITS
Supply Current From +VS	I+	All input Bits Low	0.4	22.0	mA
Supply Current From -VS	I-	All input Bits Low	-13.0	-0.8	mA
Full Scale Current	IFS	All input Bits High, 2/ Measure I_O	1.9	2.1	mA
Zero Scale Current	IZS	All input Bits Low, Measure I_O	-4.0	+4.0	uA
Power Supply Sensitivity From +VS	PSSIFS+	+VS=+4.5V to +5.5V, -VS=-16.5V All input Bits High, Measure I_O	-4.0	+4.0	uA
Power Supply Sensitivity From -VS	PSSIFS-1	+VS=+5.0V, -VS=-13.5 to -16.5V All input Bits High, Measure I_O	-8.1	+8.1	uA
	PSSIFS-2	+VS=+5.0V, -VS=-4.5V to -5.5V All input Bits High, Measure I_O	-2.7	+2.7	uA
Output Current Range	IFSR1	-VS=-5.0V, VREF=+1.5V All input Bits High, Measure I_O	2.1		mA
	IFSR2	-VS=-7.0V, VREF=+2.5V All input Bits High, Measure I_O	4.2		mA
Reference Bias Current	IREF-	All input Bits Low	-3.0	+0.1	uA
High Level Input current	IIH	All input Bits VIN = +5.5V, Each input measured separately		40.	uA
Low Level Input Current	IIL	All input Bits VIN = 0V, Each input measured separately	-800		uA
Full Scale Current at +.5V Compliance	IFS+	VI_O = +0.5V All input Bits High, Measure I_O	1.8	2.2	mA
Full Scale Current at -5.0V Compliance	IFS-	VI_O = -5.0V All input Bits High, Measure I_O, Pin 1 open	1.8	2.2	mA
Change in full scale current due to voltage compliance	ΔIFSC	VI_O =+.5V to -5.0V, Measure I_O	-4.0	+4.0	uA
Positive Bit Errors	≤NL+	(≤Positive Bit Errors)/IFS Measure I_O 3/		0.19	%
Negative Bit Errors	≤NL-	(≤Negative Bit Errors)/IFS Measure I_O 3/	-0.19		%

TABLE 6-I ELECTRICAL PERFORMANCE CHARACTERISTICS (DEVICE TYPE 03)

JC-41 COMMITTEE RECOMMENDATIONS

TEST	SYMBOL	CONDITIONS 1/	LIMITS MIN	LIMITS MAX	UNITS
Positive & Negative Bit Error Difference	$\Delta \pm$NL	$\lvert \pm$NL+$\rvert$ - $\lvert \pm$NL-$\rvert$	-0.05	+0.05	%
Positive Relative Accuracy	NL+	$\lvert \pm$NL+$\rvert$ + $\lvert \Delta \pm$NL$\rvert$		0.19	%
Negative Relative Accuracy	NL-	$\lvert \pm$NL-$\rvert$ + $\lvert \Delta \pm$NL$\rvert$		0.19	%
Monotonicity	Δ(i)	$(I_{on} - I_{on-1}) \geq 0$ at each major carry point. 4/ Measure I_o	0	16	uA
Full Scale current Temp. Coefficient	TC(IFS)	Measure I_o Bits High	-50.	+50.	ppm/°C
Propagation Delay time, High-To-Low level	tpHL	Fig. 2, all bits switched simultaneously,	6	100	nS
Propagation Delay time, Low-To-High level	tpLH	Fig. 2, all bits switched simultaneously,	6	100	nS
Reference Amplifier Output slew rate	dI/dt	Fig. 3	1.0		mA/uS
Settling Time, High-To-Low level	tsHL	Fig. 2, output within 1/2 LSB of final value of I_o	10	600	nS
Settling Time, Low-To-High level	tsLH	Fig. 2, output within 1/2 LSB of final value of I_o	10	600	nS

AD-A065 997 GENERAL ELECTRIC CO PITTSFIELD MASS ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF LINEAR INTEGRATED CIRCUITS,(U)
JAN 79 J KULPINSKI, T SIMONSEN, R PASKOWSKY F30602-77-C-0153
UNCLASSIFIED RADC-TR-78-275 NL

3 OF 3
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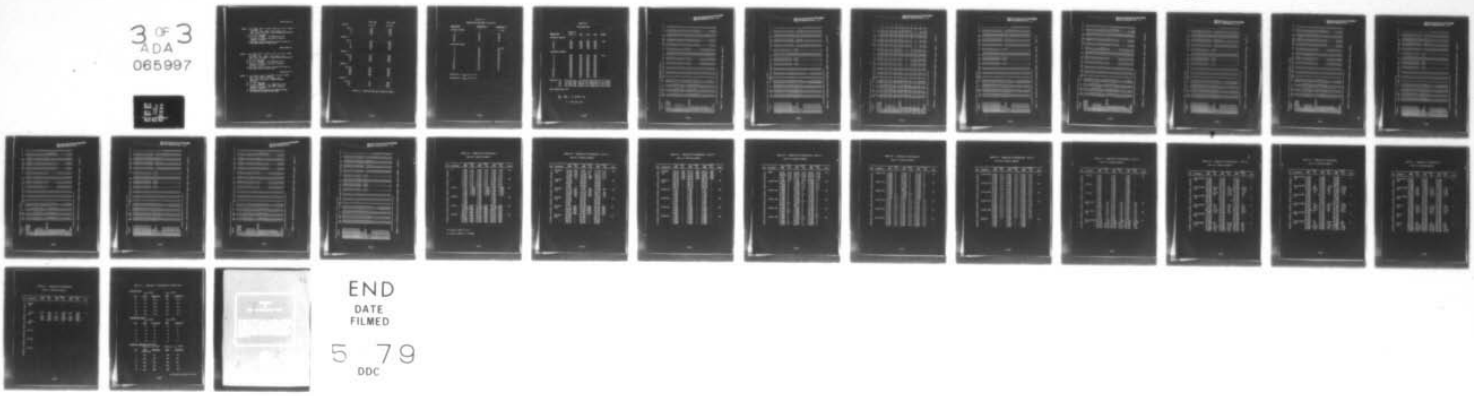

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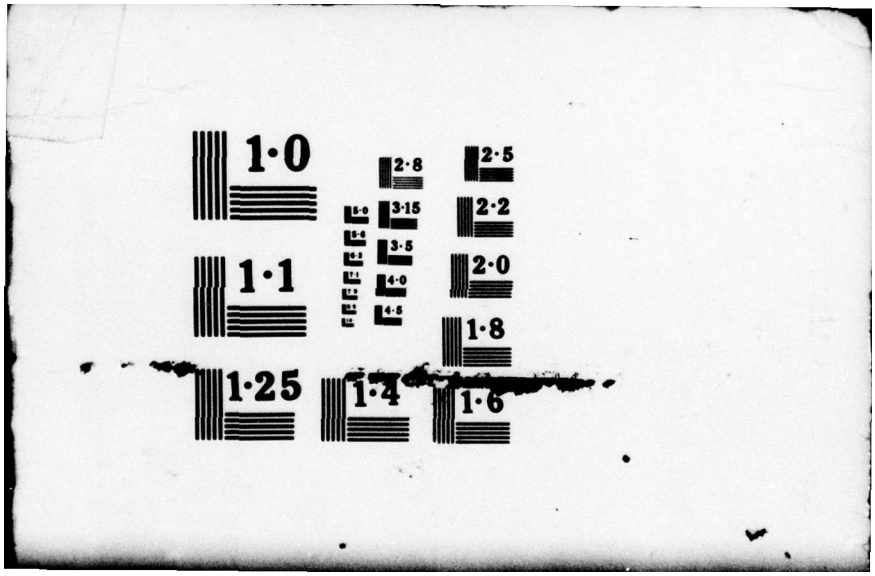
1·0
1·1
1·25
1·4
1·6
1·8
2·0
2·2
2·5
2·8
3·15
3·5
4·0
4·5

(Device Type 01)

NOTES: 1/ VS = ±15V, VREF = +10.000 ± .001V, R14 = R15 = 5.0000 ± .0005KΩ, VLC = VIO = $\overline{VI_O}$ = -VREF = 0.0V, V_{HIGH} = 2.0V, V_{LOW} = 0.8V, and Figure 1, unless otherwise specified.

2/ T_A = 25°C test only.

3/ Bit Error = $\left[\frac{2.000mA}{2^N} - (I_N - I_{ZS})\right]$; where IFS is adjusted to (1.992mA + IZS) and N = Positive integers 1 through 8.

4/ The output either increases or remains the same for each 1LSB increase of input code.

(DEVICE TYPE 02)

NOTES: 1/ VS = ±15V, VREF = +10.000 ± .001V, R14 = R15 = 5.0000 ± .0005KΩ, VLC = VIO = $\overline{VI_O}$ = -VREF = 0.0V, V_{HIGH} = 2.0V, V_{LOW} = 0.8V, and Figure 1, unless otherwise specified.

2/ T_A = 25°C test only.

3/ Bit Error = $\left[\frac{2.000mA}{2^N} - (I_N - I_{ZS})\right]$ where IFS is adjusted to (1.992mA + IZS) and N = Positive integers 1 through 8.

4/ The output either increases or remains the same for each 1LSB increase of input code.

(DEVICE TYPE 03)

NOTES: 1/ +VS = +5.0V, -VS = -15.0V, VREF = +10.000 ± .001V, R14 = R15 = 5.0000 ± .0005KΩ, VLC = VIO = -VREF = 0.0V, V_{HIGH} = 2.0V V_{LOW} = 0.8V, and Figure 1, unless otherwise specified.

2/ T_A = 25°C test only.

3/ Bit Error = $\left[\frac{2.000mA}{2^N} - (I_N - I_{ZS})\right]$; Where IFS is adjusted to (1.992mA + IZS) and N = positive integers 1 through 8.

4/ The output either increases or remains the same for each 1LSB increase of input code.

	t_{SLH} (ON)	t_{SHL} (OFF)
Vendor F	(n sec.)	(n sec.)
S/N 2	120	126
3	123	116
4	124	192
5	120	118
Vendor G		
S/N 6	110	100
7	112	110
8	114	110
9	120	120
10	112	112
Vendor E		
S/N 11	110	100
12	110	100
13	110	103
14	100	103
Vendor H		
S/N 101	165	160
102	165	160
103	165	160
104	165	160
105	160	155
Vendor A		
S/N 19	93	100
20	94	105
21	95	105

Table 6-2. Settling Time Data (taken by GEOS).

Table 6-3

PROPAGATION TIME TEST OF DAC 08's

Device S/N	Condition 1	Condition 2
Industry Sample		
1	35	44
24	41	42
35	50	56
47	33	42
70	34	41
Purchased Sample		
1	35	42
3	38	40
4	38	44
5	39	43
6	30	38
7	29	39
8	34	38
9	42	48
10	35	40
15	31	34
25	29	32
26	32	31
27	34	37

Condition 1 = t_{PLH}, V_L = 2.7 V

Condition 2 = t_{PHL}, V_L = 0.7 V

TABLE 6-4

SLEW RATE DATA

Device S/N	Condition (1)	(2)	(3)	(4)	Units
(Industry Sample)	t	t	t	t	
1	225	235	250	260	nsec
24	300	300	300	305	
35	490	500	480	500	
47	225	230	230	225	
70	330	335	330	350	
(Purchased Sample)					
1	400	405	395	400	nsec
3	370	375	365	380	
4	460	480	440	470	
5	455	455	465	470	
6	290	295	295	300	
7	265	275	280	295	
8	295	285	295	295	
9	350	355	340	355	
10	290	295	280	290	
15	235	240	220	230	
25	220	225	215	205	
26	245	240	230	245	
27	255	245	250	260	

Condition (1) all bits low, low-to-high transition at the output
(2) all bits high, low-to-high transition at the output
(3) all bits low, high-to-low transition at the output
(4) all bits high, high-to-low transition at the output

Room temperature only

$$\frac{dI}{dt} = \frac{1mA}{t} = 1.5 \text{ mA/usec. min}$$

$$t = 667 \text{ nsec. max}$$

STATISTICAL DATA FOR MIXED LOT DAC08 AT -55 DEG C (WIDE REJECT LIMITS)

PARAMETER	LOW VALUE #	HIGH VALUE #	MEAN #	SIGMA #	SAMPLE SIZE #	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM #	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM #	UNITS
I+(ALL BITS HIGH)	1.63	3.29	2.46	559.M	33	100.	100.	0.00	400.M	-1.00K	3.70	0.00	3.80	1.00K	2.39	MA
I+(ALL BITS LOW)	1.64	3.30	2.47	555.M	33	100.	100.	0.00	400.M	-1.00K	3.73	0.00	3.80	1.00K	2.39	MA
I-(ALL BITS HIGH)	-7.13	-5.51	-6.31	551.M	33	100.	100.	0.00	-7.80	-1.00K	2.71	0.00	-800.M	1.00K	9.99	MA
I-(ALL BITS LOW)	-7.13	-5.53	-6.30	542.M	33	100.	100.	0.00	-7.80	-1.00K	2.76	0.00	-800.M	1.00K	10.2	MA
IFS(I+)	1.98	2.01	1.99	6.10M	33	93.9	100.	0.00	1.94	-1.00K	8.88	0.00	2.04	1.00K	7.51	MA
IFS(I-)	1.98	2.01	1.99	6.02M	33	93.9	100.	0.00	1.94	-1.00K	9.01	0.00	2.04	1.00K	7.61	MA
IZS(I+)	-12.5M	1.62	94.6M	320.M	33	93.9	97.0	0.00	-2.00	-1.00K	6.55	0.00	2.00	1.00K	5.96	UA
IZS(I-)	-13.0M	58.0M	5.92M	14.4M	33	93.9	97.0	0.00	-2.00	-1.00K	139.	0.00	2.00	1.00K	139.	UA
PSSIFS+1(I+)	-50.1M	40.0M	-3.24M	22.7M	33	93.9	100.	0.00	-4.00	-1.00K	176.	0.00	4.00	1.00K	176.	UA
PSSIFS+1(I-)	-50.1M	50.1M	-4.42M	27.5M	33	100.	100.	0.00	-4.00	-1.00K	145.	0.00	4.00	1.00K	145.	UA
PSSIFS+2(I+)	-50.1M	40.0M	-3.24M	22.7M	33	93.9	100.	0.00	-8.00	-1.00K	352.	0.00	8.00	1.00K	353.	UA
PSSIFS+2(I-)	-50.1M	50.1M	-4.42M	27.5M	33	100.	100.	0.00	-8.00	-1.00K	290.	0.00	8.00	1.00K	291.	UA
PSSIFS-1(I+)	-37.3	583.M	-1.21	6.49	33	97.0	97.0	3.03	-8.00	-1.00K	1.05	0.00	8.00	1.00K	1.42	UA
PSSIFS-1(I-)	-34.1	558.M	-1.12	5.92	33	97.0	97.0	3.03	-8.00	-1.00K	1.16	0.00	8.00	1.00K	1.54	UA
PSSIFS-2(I+)	-2.17	38.2M	-395.M	512.M	33	93.9	97.0	3.03	-2.00	-1.00K	3.14	0.00	2.00	1.00K	4.68	UA
PSSIFS-2(I-)	-1.27	12.6M	-300.M	274.M	33	93.9	97.0	0.00	-2.00	-1.00K	6.21	0.00	2.00	1.00K	8.41	UA
IFSR1(I+)	1.22	2.97	2.52	646.M	33	97.0	100.	27.3	2.10	-1.00K	644.M	0.00	5.80	1.00K	5.09	MA
IFSR1(I-)	1.65	2.97	2.71	401.M	33	90.9	100.	15.2	2.10	-1.00K	1.51	0.00	5.80	1.00K	7.71	MA
IFSR2(I+)	1.03	4.04	3.29	1.02	33	93.9	100.	100.	4.20	-1.00K	-895.M	0.00	5.80	1.00K	2.47	MA
IFSR2(I-)	2.85	4.07	3.73	386.M	33	93.9	100.	100.	4.20	-1.00K	-1.23	0.00	5.80	1.00K	5.37	MA
IREF-(ALL BITS LOW)	-2.56	-372.M	-927.M	540.M	33	93.9	97.0	0.00	-3.00	-1.00K	3.84	0.00	100.M	1.00K	1.90	UA
IREF-(ALL BITS HIGH)	-2.56	-366.M	-926.M	539.M	33	93.9	97.0	0.00	-3.00	-1.00K	3.85	0.00	100.M	1.00K	1.90	UA
IIH(BIT#1)	-1.65M	78.2M	7.02M	14.2M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	705.	UA
IIH(BIT#2)	-1.00M	27.1M	4.62M	5.60M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	1.79K	UA
IIH(BIT#3)	-1.10M	19.7M	4.25M	4.48M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	2.23K	UA
IIH(BIT#4)	-400.U	9.60M	3.85M	3.00M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	3.33K	UA
IIH(BIT#5)	-1.20M	212.M	14.3M	42.4M	33	93.9	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	235.	UA
IIH(BIT#6)	-200.U	2.14	86.4M	382.M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	25.9	UA
IIH(BIT#7)	-200.U	401.M	16.7M	69.0M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	145.	UA
IIH(BIT#8)	-1.10M	15.4	471.M	2.69	33	97.0	97.0	----	----	-1.00K	----	3.03	10.0	1.00K	3.56	UA
IIL(BIT#1)	-17.7	-1.55	-2.99	2.88	33	97.0	97.0	3.03	-10.0	-1.00K	2.43	----	----	1.00K	----	UA
IIL(BIT#2)	-16.3	-1.43	-2.88	2.61	33	97.0	97.0	3.03	-10.0	-1.00K	2.73	----	----	1.00K	----	UA
IIL(BIT#3)	-19.5	-1.48	-3.07	3.16	33	97.0	97.0	3.03	-10.0	-1.00K	2.20	----	----	1.00K	----	UA
IIL(BIT#4)	-16.4	-1.32	-2.98	2.70	33	97.0	97.0	3.03	-10.0	-1.00K	2.60	----	----	1.00K	----	UA
IIL(BIT#5)	-15.0	-1.45	-2.99	2.38	33	97.0	97.0	3.03	-10.0	-1.00K	2.94	----	----	1.00K	----	UA
IIL(BIT#6)	-15.3	-1.38	-3.05	2.52	33	97.0	97.0	3.03	-10.0	-1.00K	2.76	----	----	1.00K	----	UA
IIL(BIT#7)	-17.2	-1.42	-3.12	2.79	33	97.0	97.0	3.03	-10.0	-1.00K	2.47	----	----	1.00K	----	UA
IIL(BIT#8)	-278.	-1.45	-11.9	47.9	33	97.0	97.0	9.09	-10.0	-1.00K	-39.4M	----	----	1.00K	----	UA
IFS+(I+)	1.98	2.04	2.00	15.2M	33	97.0	100.	0.00	1.85	-1.00K	10.2	0.00	2.08	1.00K	4.97	MA
IFS+(I-)	1.98	2.04	2.00	15.2M	33	97.0	100.	0.00	1.85	-1.00K	10.2	0.00	2.08	1.00K	4.94	MA
IFS-(I+)	1.95	2.00	1.99	9.77M	33	97.0	97.0	0.00	1.85	-1.00K	14.5	0.00	2.08	1.00K	9.05	MA
IFS-(I-)	1.95	2.00	1.99	9.27M	33	97.0	97.0	0.00	1.85	-1.00K	15.3	0.00	2.08	1.00K	9.53	MA
DELTA IFS(I+)	3.11	45.2	13.2	13.6	33	97.0	100.	0.00	-4.00	-1.00K	1.27	57.6	4.00	1.00K	-677.M	UA
DELTA IFS(I-)	2.82	45.3	13.1	13.6	33	97.0	100.	0.00	-4.00	-1.00K	1.26	57.6	4.00	1.00K	-670.M	UA

EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits).

STATISTICAL DATA FOR MIXED LOT DAC08 AT -55 DEG C (CONTINUED)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT#1)(I+)	-264.M	86.3M	-72.1M	82.3M	33	97.0	100.	6.06	-190.M	-1.00K	1.43	0.00	190.M	1.00K	3.18	%
ERROR(BIT#1)(I-)	-275.M	85.4M	-82.3M	86.6M	33	93.9	100.	6.06	-190.M	-1.00K	1.24	0.00	190.M	1.00K	3.15	%
ERROR(BIT#2)(I+)	-111.M	87.6M	-17.7M	53.4M	33	100.	100.	0.00	-190.M	-1.00K	3.23	0.00	190.M	1.00K	3.89	%
ERROR(BIT#2)(I-)	-105.M	95.1M	-15.0M	51.4M	33	97.0	100.	0.00	-190.M	-1.00K	3.40	0.00	190.M	1.00K	3.99	%
ERROR(BIT#3)(I+)	-112.M	82.3M	582.U	44.5M	33	97.0	100.	0.00	-190.M	-1.00K	4.28	0.00	190.M	1.00K	4.26	%
ERROR(BIT#3)(I-)	-75.3M	90.2M	5.88M	40.0M	33	93.9	100.	0.00	-190.M	-1.00K	4.89	0.00	190.M	1.00K	4.60	%
ERROR(BIT#4)(I+)	-34.0M	67.4M	12.5M	24.6M	33	97.0	100.	0.00	-190.M	-1.00K	8.24	0.00	190.M	1.00K	7.22	%
ERROR(BIT#4)(I-)	-33.7M	68.8M	11.2M	23.8M	33	97.0	100.	0.00	-190.M	-1.00K	8.47	0.00	190.M	1.00K	7.53	%
ERROR(BIT#5)(I+)	-30.8M	60.6M	9.60M	18.7M	33	93.9	100.	0.00	-190.M	-1.00K	10.7	0.00	190.M	1.00K	9.66	%
ERROR(BIT#5)(I-)	-19.5M	71.9M	10.4M	19.0M	33	97.0	97.0	0.00	-190.M	-1.00K	10.5	0.00	190.M	1.00K	9.44	%
ERROR(BIT#6)(I+)	-50.2M	40.6M	998.U	24.0M	33	97.0	100.	0.00	-190.M	-1.00K	7.97	0.00	190.M	1.00K	7.88	%
ERROR(BIT#6)(I-)	-50.2M	71.1M	2.21M	26.6M	33	97.0	100.	0.00	-190.M	-1.00K	7.23	0.00	190.M	1.00K	7.07	%
ERROR(BIT#7)(I+)	-8.43M	45.5M	16.1M	12.1M	33	93.9	100.	0.00	-190.M	-1.00K	17.0	0.00	190.M	1.00K	14.4	%
ERROR(BIT#7)(I-)	-7.90M	47.5M	16.7M	11.8M	33	93.9	100.	0.00	-190.M	-1.00K	17.5	0.00	190.M	1.00K	14.7	%
ERROR(BIT#8)(I+)	-20.2M	31.7M	6.45M	13.0M	33	97.0	100.	0.00	-190.M	-1.00K	15.1	0.00	190.M	1.00K	14.2	%
ERROR(BIT#8)(I-)	-90.0M	54.0M	7.11M	21.6M	33	93.9	97.0	0.00	-190.M	-1.00K	9.11	0.00	190.M	1.00K	8.46	%
SUM NL+(I+)	42.1M	221.M	108.M	42.7M	33	93.9	100.	----	----	-1.00K	----	6.06	190.M	1.00K	1.92	%
SUM NL+(I-)	40.1M	244.M	111.M	48.0M	33	93.9	100.	----	----	-1.00K	----	9.09	190.M	1.00K	1.65	%
SUM NL-(I+)	-268.M	-83.8M	-151.M	42.9M	33	93.9	100.	12.1	-190.M	-1.00K	903.M	----	----	1.00K	----	%
SUM NL-(I-)	-285.M	-84.8M	-155.M	47.6M	33	93.9	100.	18.2	-190.M	-1.00K	741.M	----	----	1.00K	----	%
DELTA SUM NL(I+)	-52.4M	-22.8M	-43.5M	4.81M	33	97.0	97.0	6.06	-50.0M	-1.00K	1.35	0.00	50.0M	1.00K	19.5	%
DELTA SUM NL(I-)	-46.4M	-38.9M	-43.8M	1.69M	33	97.0	100.	0.00	-50.0M	-1.00K	3.67	0.00	50.0M	1.00K	55.4	%
NL+(I+)	83.8M	268.M	151.M	42.9M	33	93.9	100.	----	----	-1.00K	----	12.1	190.M	1.00K	903.M	%
NL+(I-)	84.8M	285.M	155.M	47.6M	33	93.9	100.	----	----	-1.00K	----	18.2	190.M	1.00K	741.M	%
NL-(I+)	125.M	315.M	195.M	43.6M	33	93.9	100.	----	----	-1.00K	----	54.5	190.M	1.00K	-110.M	%
NL-(I-)	127.M	327.M	199.M	47.3M	33	93.9	100.	----	----	-1.00K	----	51.5	190.M	1.00K	-180.M	%
DELTA I(1)(I+)	4.03	17.9	10.3	3.28	33	97.0	100.	----	----	-1.00K	----	9.03	16.0	1.00K	1.75	UA
DELTA I(1)(I-)	3.97	18.4	10.6	3.45	33	93.9	100.	----	----	-1.00K	----	6.06	16.0	1.00K	1.55	UA
DELTA I(2)(I+)	5.78	12.8	9.31	1.81	33	100.	100.	----	----	-1.00K	----	0.00	16.0	1.00K	3.70	UA
DELTA I(2)(I-)	5.94	13.3	9.40	1.94	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	3.40	UA
DELTA I(3)(I+)	6.01	13.5	8.82	1.42	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	5.05	UA
DELTA I(3)(I-)	6.12	11.3	8.75	1.21	33	90.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	6.00	UA
DELTA I(4)(I+)	6.70	9.67	8.26	550.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	14.1	UA
DELTA I(4)(I-)	6.52	11.3	8.35	762.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	10.0	UA
DELTA I(5)(I+)	7.17	9.01	8.09	347.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	22.8	UA
DELTA I(5)(I-)	5.32	8.79	8.13	580.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	13.6	UA
DELTA I(6)(I+)	6.90	10.2	8.24	752.M	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	10.3	UA
DELTA I(6)(I-)	6.26	10.2	8.25	834.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	9.30	UA
DELTA I(7)(I+)	7.19	8.61	7.63	344.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	24.3	UA
DELTA I(7)(I-)	5.85	9.06	7.63	481.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	17.4	UA
DELTA I(8)(I+)	7.12	8.23	7.69	259.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	32.0	UA
DELTA I(8)(I-)	6.75	9.61	7.68	433.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	19.2	UA
DELTA IFS	-2.66	2.57	28.0M	942.M	33	93.9	100.	0.00	-8.00	-1.00K	8.52	0.00	8.00	1.00K	8.46	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +25 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
I+(ALL BITS HIGH)	1.60	3.43	2.45	525.M	33	100.	100.	0.00	400.M	-1.00K	3.91	0.00	3.80	1.00K	2.57	MA
I+(ALL BITS LOW)	1.61	3.44	2.46	521.M	33	100.	100.	0.00	400.M	-1.00K	3.96	0.00	3.80	1.00K	2.57	MA
I-(ALL BITS HIGH)	-7.28	-5.51	-6.31	522.M	33	100.	100.	0.00	-7.80	-1.00K	2.86	0.00	-800.M	1.00K	10.6	MA
I-(ALL BITS LOW)	-7.28	-5.53	-6.29	504.M	33	100.	100.	0.00	-7.80	-1.00K	2.99	0.00	-800.M	1.00K	10.9	MA
IFS(I+)	1.98	2.01	2.00	5.40M	33	93.9	100.	0.00	1.94	-1.00K	10.2	0.00	2.04	1.00K	8.33	MA
IFS(I-)	1.98	2.01	2.00	5.39M	33	93.9	100.	0.00	1.94	-1.00K	10.2	0.00	2.04	1.00K	8.33	MA
IZS(I+)	-7.00M	119.M	24.0M	39.9M	33	90.9	100.	0.00	-2.00	-1.00K	50.7	0.00	2.00	1.00K	49.5	UA
IZS(I-)	-11.5M	127.M	24.2M	41.3M	33	93.9	100.	0.00	-2.00	-1.00K	49.0	0.00	2.00	1.00K	47.8	UA
PSSIFS+1(I+)	-75.0M	45.2M	-16.4M	29.4M	33	97.0	100.	0.00	-4.00	-1.00K	135.	0.00	4.00	1.00K	137.	UA
PSSIFS+1(I-)	-70.1M	40.0M	-8.93M	23.4M	33	93.9	100.	0.00	-4.00	-1.00K	171.	0.00	4.00	1.00K	171.	UA
PSSIFS+2(I+)	-75.0M	45.2M	-16.4M	29.4M	33	97.0	100.	0.00	-8.00	-1.00K	271.	0.00	8.00	1.00K	272.	UA
PSSIFS+2(I-)	-70.1M	40.0M	-8.93M	23.4M	33	93.9	100.	0.00	-8.00	-1.00K	342.	0.00	8.00	1.00K	342.	UA
PSSIFS-1(I+)	-950.M	14.9M	-194.M	160.M	33	97.0	97.0	0.00	-8.00	-1.00K	48.7	0.00	8.00	1.00K	51.2	UA
PSSIFS-1(I-)	-1.05	80.1M	-215.M	176.M	33	97.0	97.0	0.00	-8.00	-1.00K	44.2	0.00	8.00	1.00K	46.6	UA
PSSIFS-2(I+)	-2.27	-80.1M	-389.M	507.M	33	93.9	93.9	6.06	-2.00	-1.00K	3.18	0.00	2.00	1.00K	4.71	UA
PSSIFS-2(I-)	-1.41	-130.M	-323.M	293.M	33	93.9	93.9	0.00	-2.00	-1.00K	5.72	0.00	2.00	1.00K	7.92	UA
IFSR1(I+)	948.M	2.94	2.65	592.M	33	87.9	100.	15.2	2.10	-1.00K	925.M	0.00	5.80	1.00K	5.33	MA
IFSR1(I-)	1.25	2.94	2.73	475.M	33	87.9	97.0	12.1	2.10	-1.00K	1.32	0.00	5.80	1.00K	6.46	MA
IFSR2(I+)	1.79	4.05	3.52	785.M	33	93.9	100.	100.	4.20	-1.00K	-862.M	0.00	5.80	1.00K	2.90	MA
IFSR2(I-)	2.36	4.04	3.73	498.M	33	90.9	100.	100.	4.20	-1.00K	-936.M	0.00	5.80	1.00K	4.15	MA
IREF-(ALL BITS LOW)	-2.49	-426.M	-1.01	545.M	33	93.9	100.	0.00	-3.00	-1.00K	3.65	0.00	100.M	1.00K	2.05	UA
IREF-(ALL BITS HIGH)	-2.49	-423.M	-1.01	545.M	33	93.9	100.	0.00	-3.00	-1.00K	3.64	0.00	100.M	1.00K	2.04	UA
IIH(BIT#1)	-1.65M	10.5M	3.69M	4.18M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	2.39K	UA
IIH(BIT#2)	-1.80M	9.65M	3.32M	3.94M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	2.53K	UA
IIH(BIT#3)	-1.75M	14.0M	3.40M	4.01M	33	97.0	100.	----	----	-1.00K	----	0.00	10.0	1.00K	2.49K	UA
IIH(BIT#4)	-1.30M	9.30M	3.43M	3.33M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	3.00K	UA
IIH(BIT#5)	-450.U	9.50M	3.41M	3.21M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	3.11K	UA
IIH(BIT#6)	-1.20M	9.35M	3.44M	3.26M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	3.06K	UA
IIH(BIT#7)	-1.00M	9.30M	3.25M	3.44M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	2.91K	UA
IIH(BIT#8)	-1.10M	63.7M	5.08M	11.1M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	903.	UA
IIL(BIT#1)	-7.13	-1.75	-2.95	1.20	33	97.0	97.0	0.00	-10.0	-1.00K	5.88	----	----	1.00K	----	UA
IIL(BIT#2)	-5.97	-1.68	-2.83	1.05	33	97.0	100.	0.00	-10.0	-1.00K	6.81	----	----	1.00K	----	UA
IIL(BIT#3)	-6.62	-1.71	-2.96	1.17	33	97.0	97.0	0.00	-10.0	-1.00K	6.03	----	----	1.00K	----	UA
IIL(BIT#4)	-7.19	-1.56	-2.92	1.24	33	97.0	97.0	0.00	-10.0	-1.00K	5.72	----	----	1.00K	----	UA
IIL(BIT#5)	-6.39	-1.72	-2.98	1.13	33	97.0	97.0	0.00	-10.0	-1.00K	6.21	----	----	1.00K	----	UA
IIL(BIT#6)	-7.64	-1.56	-2.95	1.30	33	97.0	97.0	0.00	-10.0	-1.00K	5.41	----	----	1.00K	----	UA
IIL(BIT#7)	-7.26	-1.62	-3.02	1.20	33	97.0	97.0	0.00	-10.0	-1.00K	5.80	----	----	1.00K	----	UA
IIL(BIT#8)	-149.	-1.69	-7.49	25.4	33	97.0	97.0	3.03	-10.0	-1.00K	98.5M	----	----	1.00K	----	UA
IFS+(I+)	1.98	2.02	2.00	10.2M	33	93.9	100.	0.00	1.85	-1.00K	14.9	0.00	2.08	1.00K	7.76	MA
IFS+(I-)	1.98	2.02	2.00	10.2M	33	93.9	100.	0.00	1.85	-1.00K	14.9	0.00	2.08	1.00K	7.74	MA
IFS-(I+)	1.98	2.00	1.99	5.36M	33	93.9	97.0	0.00	1.85	-1.00K	26.8	0.00	2.08	1.00K	16.1	MA
IFS-(I-)	1.98	2.01	1.99	5.36M	33	93.9	100.	0.00	1.85	-1.00K	26.8	0.00	2.08	1.00K	16.1	MA
DELTA IFSC(I+)	1.75	26.5	7.35	7.62	33	97.0	100.	0.00	-4.00	-1.00K	1.49	30.3	4.00	1.00K	-440.M	UA
DELTA IFSC(I-)	1.73	26.7	7.41	7.73	33	97.0	100.	0.00	-4.00	-1.00K	1.48	30.3	4.00	1.00K	-441.M	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +25 DEG C (CONTINUED)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT01)(I+)	-166.M	72.7M	-45.2M	65.8M	33	100.	100.	0.00	-190.M	-1.00K	2.20	0.00	190.M	1.00K	3.57	%
ERROR(BIT01)(I-)	-171.M	53.6M	-48.8M	62.4M	33	100.	100.	0.00	-190.M	-1.00K	2.26	0.00	190.M	1.00K	3.82	%
ERROR(BIT02)(I+)	-83.9M	56.4M	-13.3M	41.0M	33	100.	100.	0.00	-190.M	-1.00K	4.31	0.00	190.M	1.00K	4.96	%
ERROR(BIT02)(I-)	-79.3M	53.2M	-12.8M	40.0M	33	100.	100.	0.00	-190.M	-1.00K	4.43	0.00	190.M	1.00K	5.07	%
ERROR(BIT03)(I+)	-63.6M	57.3M	5.23M	31.4M	33	97.0	100.	0.00	-190.M	-1.00K	6.22	0.00	190.M	1.00K	5.88	%
ERROR(BIT03)(I-)	-47.1M	58.7M	6.90M	29.7M	33	100.	100.	0.00	-190.M	-1.00K	6.62	0.00	190.M	1.00K	6.16	%
ERROR(BIT04)(I+)	-42.5M	38.5M	-1.00M	20.8M	33	100.	100.	0.00	-190.M	-1.00K	9.08	0.00	190.M	1.00K	9.17	%
ERROR(BIT04)(I-)	-43.4M	39.1M	-1.15M	21.1M	33	97.0	100.	0.00	-190.M	-1.00K	8.96	0.00	190.M	1.00K	9.07	%
ERROR(BIT05)(I+)	-25.6M	38.0M	3.21M	15.1M	33	97.0	100.	0.00	-190.M	-1.00K	12.8	0.00	190.M	1.00K	12.3	%
ERROR(BIT05)(I-)	-21.2M	39.8M	3.70M	15.3M	33	97.0	100.	0.00	-190.M	-1.00K	12.7	0.00	190.M	1.00K	12.2	%
ERROR(BIT06)(I+)	-56.5M	30.3M	-4.69M	22.1M	33	97.0	100.	0.00	-190.M	-1.00K	8.37	0.00	190.M	1.00K	8.79	%
ERROR(BIT06)(I-)	-56.1M	30.8M	-4.22M	22.2M	33	97.0	100.	0.00	-190.M	-1.00K	8.39	0.00	190.M	1.00K	8.77	%
ERROR(BIT07)(I+)	-9.88M	43.6M	12.3M	12.6M	33	97.0	100.	0.00	-190.M	-1.00K	16.1	0.00	190.M	1.00K	14.1	%
ERROR(BIT07)(I-)	-9.93M	44.1M	12.6M	12.5M	33	97.0	100.	0.00	-190.M	-1.00K	16.2	0.00	190.M	1.00K	14.2	%
ERROR(BIT08)(I+)	-27.2M	28.3M	-1.08M	12.6M	33	93.9	100.	0.00	-190.M	-1.00K	15.0	0.00	190.M	1.00K	15.2	%
ERROR(BIT08)(I-)	-67.0M	45.5M	141.U	17.3M	33	93.9	97.0	0.00	-190.M	-1.00K	11.0	0.00	190.M	1.00K	10.9	%
SUM NL+(I+)	27.1M	140.M	77.9M	27.8M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	4.03	%
SUM NL+(I-)	28.4M	137.M	76.9M	27.0M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	4.19	%
SUM NL-(I+)	-183.M	-72.0M	-122.M	27.1M	33	93.9	100.	0.00	-190.M	-1.00K	2.50	----	----	1.00K	----	%
SUM NL-(I-)	-180.M	-72.4M	-121.M	25.9M	33	93.9	100.	0.00	-190.M	-1.00K	2.68	----	----	1.00K	----	%
DELTA SUM NL(I+)	-47.6M	-39.4M	-44.5M	2.10M	33	97.0	100.	0.00	-50.0M	-1.00K	2.62	0.00	50.0M	1.00K	45.0	%
DELTA SUM NL(I-)	-52.4M	-37.4M	-43.7M	3.10M	33	90.9	100.	3.03	-50.0M	-1.00K	2.04	0.00	50.0M	1.00K	30.2	%
NL+(I+)	72.0M	183.M	122.M	27.1M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	2.50	%
NL+(I-)	72.4M	180.M	121.M	25.9M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	2.68	%
NL-(I+)	117.M	228.M	167.M	26.5M	33	97.0	100.	----	----	-1.00K	----	18.2	190.M	1.00K	873.M	%
NL-(I-)	116.M	224.M	164.M	25.2M	33	97.0	100.	----	----	-1.00K	----	18.2	190.M	1.00K	1.02	%
DELTA I(1)(I+)	4.59	14.0	9.18	2.62	33	100.	100.	----	----	-1.00K	----	0.00	16.0	1.00K	2.60	UA
DELTA I(1)(I-)	5.21	14.2	9.31	2.69	33	100.	100.	----	----	-1.00K	----	0.00	16.0	1.00K	2.69	UA
DELTA I(2)(I+)	6.06	11.8	8.59	1.29	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	5.73	UA
DELTA I(2)(I-)	6.37	11.9	8.65	1.29	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	5.68	UA
DELTA I(3)(I+)	5.78	9.80	7.99	1.04	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	7.72	UA
DELTA I(3)(I-)	5.83	9.83	8.00	1.00	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	8.00	UA
DELTA I(4)(I+)	7.14	9.35	8.07	461.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	17.2	UA
DELTA I(4)(I-)	7.26	9.65	8.11	505.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	15.6	UA
DELTA I(5)(I+)	6.76	8.56	7.89	336.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	24.1	UA
DELTA I(5)(I-)	6.58	8.61	7.92	504.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	16.0	UA
DELTA I(6)(I+)	6.77	10.2	8.13	778.M	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	10.1	UA
DELTA I(6)(I-)	6.76	10.1	8.16	807.M	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	9.72	UA
DELTA I(7)(I+)	7.12	8.58	7.55	313.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	27.0	UA
DELTA I(7)(I-)	6.37	8.94	7.58	391.M	33	93.9	93.9	----	----	-1.00K	----	0.00	16.0	1.00K	21.5	UA
DELTA I(8)(I+)	7.26	8.36	7.84	253.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	32.3	UA
DELTA I(8)(I-)	6.92	9.16	7.82	346.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	23.7	UA
DELTA IFS	-1.08	450.M	-21.7M	313.M	33	93.9	97.0	0.00	-8.00	-1.00K	25.5	0.00	8.00	1.00K	25.6	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +125 DEG C

PARAMETER	LOW VALUE #	HIGH VALUE #	MEAN #	SIGMA #	SAMPLE SIZE #	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM #	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM #	UNITS
I+(ALL BITS HIGH)	1.44	3.45	2.32	541.M	33	93.9	100.	0.00	400.M	-1.00K	3.55	0.00	3.80	1.00K	2.73	MA
I+(ALL BITS LOW)	1.46	3.47	2.33	540.M	33	93.9	100.	0.00	400.M	-1.00K	3.57	0.00	3.80	1.00K	2.72	MA
I-(ALL BITS HIGH)	-7.31	-5.36	-6.19	541.M	33	93.9	100.	0.00	-7.80	-1.00K	2.98	0.00	-800.M	1.00K	9.95	MA
I-(ALL BITS LOW)	-7.31	-5.37	-6.17	529.M	33	93.9	100.	0.00	-7.80	-1.00K	3.07	0.00	-800.M	1.00K	10.2	MA
IFS(I+)	1.98	2.01	1.99	5.28M	33	93.9	100.	0.00	1.94	-1.00K	10.2	0.00	2.04	1.00K	8.71	MA
IFS(I-)	1.98	2.01	1.99	5.26M	33	93.9	100.	0.00	1.94	-1.00K	10.3	0.00	2.04	1.00K	8.75	MA
IZS(I+)	14.5M	544.M	136.M	160.M	33	90.9	100.	0.00	-2.00	-1.00K	13.4	0.00	2.00	1.00K	11.7	UA
IZS(I-)	9.50M	356.M	93.9M	111.M	33	90.9	100.	0.00	-2.00	-1.00K	18.9	0.00	2.00	1.00K	17.2	UA
PSSIFS+1(I+)	-115.M	44.9M	-35.8M	34.1M	33	93.9	100.	0.00	-4.00	-1.00K	116.	0.00	4.00	1.00K	118.	UA
PSSIFS+1(I-)	-140.M	20.0M	-41.1M	42.2M	33	93.9	100.	0.00	-4.00	-1.00K	93.7	0.00	4.00	1.00K	95.7	UA
PSSIFS+2(I+)	-115.M	44.9M	-35.8M	34.1M	33	93.9	100.	0.00	-8.00	-1.00K	233.	0.00	8.00	1.00K	235.	UA
PSSIFS+2(I-)	-140.M	20.0M	-41.1M	42.2M	33	93.9	100.	0.00	-8.00	-1.00K	188.	0.00	8.00	1.00K	190.	UA
PSSIFS-1(I+)	-440.M	-60.1M	-244.M	99.4M	33	100.	100.	0.00	-8.00	-1.00K	78.0	0.00	8.00	1.00K	82.9	UA
PSSIFS-1(I-)	-455.M	-100.M	-266.M	101.M	33	100.	100.	0.00	-8.00	-1.00K	76.6	0.00	8.00	1.00K	81.9	UA
PSSIFS-2(I+)	-45.5	-120.M	-4.91	12.3	33	90.9	97.0	18.2	-2.00	-1.00K	-237.M	0.00	2.00	1.00K	562.M	UA
PSSIFS-2(I-)	-59.9	-130.M	-5.17	14.0	33	90.9	97.0	12.1	-2.00	-1.00K	-226.M	0.00	2.00	1.00K	512.M	UA
IFSR1(I+)	668.M	4.02	2.66	914.M	33	97.0	100.	27.3	2.10	-1.00K	617.M	0.00	5.80	1.00K	3.43	MA
IFSR1(I-)	811.M	4.05	2.84	882.M	33	97.0	100.	21.2	2.10	-1.00K	841.M	0.00	5.80	1.00K	3.35	MA
IFSR2(I+)	1.40	3.97	2.83	918.M	33	100.	100.	100.	4.20	-1.00K	-1.50	0.00	5.80	1.00K	3.24	MA
IFSR2(I-)	1.81	4.04	3.24	720.M	33	100.	100.	100.	4.20	-1.00K	-1.33	0.00	5.80	1.00K	3.56	MA
IREF-(ALL BITS LOW)	-2.22	-306.M	-993.M	512.M	33	97.0	100.	0.00	-3.00	-1.00K	3.92	0.00	100.M	1.00K	2.13	UA
IREF-(ALL BITS HIGH)	-2.23	-297.M	-992.M	516.M	33	97.0	100.	0.00	-3.00	-1.00K	3.89	0.00	100.M	1.00K	2.12	UA
IIH(BIT01)	1.70M	25.8M	12.2M	7.22M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.38K	UA
IIH(BIT02)	1.55M	23.8M	12.2M	7.42M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.35K	UA
IIH(BIT03)	1.70M	28.3M	12.6M	8.15M	33	100.	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.23K	UA
IIH(BIT04)	1.20M	29.1M	12.5M	8.25M	33	97.0	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.21K	UA
IIH(BIT05)	550.U	30.9M	12.1M	8.14M	33	93.9	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.23K	UA
IIH(BIT06)	900.U	75.4M	14.1M	13.9M	33	97.0	97.0	----	----	-1.00K	----	0.00	10.0	1.00K	721.	UA
IIH(BIT07)	1.05M	37.5M	13.3M	9.46M	33	93.9	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.06K	UA
IIH(BIT08)	800.U	30.2M	12.0M	7.72M	33	97.0	100.	----	----	-1.00K	----	0.00	10.0	1.00K	1.29K	UA
IIL(BIT01)	-6.01	-1.80	-3.05	1.12	33	97.0	100.	0.00	-10.0	-1.00K	6.19	----	----	1.00K	----	UA
IIL(BIT02)	-5.20	-1.70	-2.91	1.01	33	97.0	100.	0.00	-10.0	-1.00K	7.03	----	----	1.00K	----	UA
IIL(BIT03)	-5.65	-1.77	-3.03	1.09	33	97.0	100.	0.00	-10.0	-1.00K	6.39	----	----	1.00K	----	UA
IIL(BIT04)	-6.09	-1.66	-3.00	1.15	33	97.0	100.	0.00	-10.0	-1.00K	6.11	----	----	1.00K	----	UA
IIL(BIT05)	-5.34	-1.77	-3.05	1.06	33	97.0	100.	0.00	-10.0	-1.00K	6.55	----	----	1.00K	----	UA
IIL(BIT06)	-6.33	-1.64	-3.00	1.18	33	97.0	100.	0.00	-10.0	-1.00K	5.94	----	----	1.00K	----	UA
IIL(BIT07)	-6.03	-1.74	-3.05	1.10	33	97.0	100.	0.00	-10.0	-1.00K	6.31	----	----	1.00K	----	UA
IIL(BIT08)	-65.9	-1.71	-5.03	11.0	33	97.0	97.0	3.03	-10.0	-1.00K	452.M	----	----	1.00K	----	UA
IFS+(I+)	1.98	2.01	2.00	8.12M	33	97.0	100.	0.00	1.85	-1.00K	18.2	0.00	2.08	1.00K	10.1	MA
IFS+(I-)	1.98	2.01	2.00	8.13M	33	97.0	100.	0.00	1.85	-1.00K	18.2	0.00	2.08	1.00K	10.1	MA
IFS-(I+)	1.98	2.00	1.99	5.22M	33	90.9	100.	0.00	1.85	-1.00K	27.4	0.00	2.08	1.00K	16.7	MA
IFS-(I-)	1.98	2.01	1.99	5.20M	33	93.9	100.	0.00	1.85	-1.00K	27.4	0.00	2.08	1.00K	16.8	MA
DELTA IFSC(I+)	1.48	16.7	5.10	4.66	33	97.0	100.	0.00	-4.00	-1.00K	1.95	30.3	4.00	1.00K	-236.M	UA
DELTA IFSC(I-)	1.41	16.9	5.12	4.76	33	97.0	100.	0.00	-4.00	-1.00K	1.92	30.3	4.00	1.00K	-236.M	UA

EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +125 DEG C (CONTINUED)

PARAMETER	LOW VALUE #	HIGH VALUE #	MEAN *	SIGMA *	SAMPLE SIZE #	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT#1)(I+)	-157.M	84.8M	-30.6M	58.1M	33	97.0	100.	0.00	-190.M	-1.00K	2.74	0.00	190.M	1.00K	3.80	%
ERROR(BIT#1)(I-)	-160.M	81.8M	-32.2M	57.1M	33	97.0	100.	0.00	-190.M	-1.00K	2.76	0.00	190.M	1.00K	3.89	%
ERROR(BIT#2)(I+)	-77.4M	45.3M	-10.4M	33.6M	33	100.	100.	0.00	-190.M	-1.00K	5.34	0.00	190.M	1.00K	5.96	%
ERROR(BIT#2)(I-)	-73.4M	46.2M	-10.5M	33.2M	33	100.	100.	0.00	-190.M	-1.00K	5.40	0.00	190.M	1.00K	6.04	%
ERROR(BIT#3)(I+)	-51.2M	63.2M	7.41M	31.0M	33	100.	100.	0.00	-190.M	-1.00K	6.37	0.00	190.M	1.00K	5.89	%
ERROR(BIT#3)(I-)	-40.3M	69.7M	8.08M	30.2M	33	100.	100.	0.00	-190.M	-1.00K	6.56	0.00	190.M	1.00K	6.02	%
ERROR(BIT#4)(I+)	-55.8M	29.1M	-8.21M	22.4M	33	97.0	100.	0.00	-190.M	-1.00K	8.10	0.00	190.M	1.00K	8.83	%
ERROR(BIT#4)(I-)	-55.5M	29.3M	-7.86M	22.7M	33	97.0	100.	0.00	-190.M	-1.00K	8.04	0.00	190.M	1.00K	8.73	%
ERROR(BIT#5)(I+)	-23.5M	34.7M	-1.10M	15.3M	33	93.9	100.	0.00	-190.M	-1.00K	12.3	0.00	190.M	1.00K	12.5	%
ERROR(BIT#5)(I-)	-23.2M	38.0M	-551.U	15.6M	33	97.0	100.	0.00	-190.M	-1.00K	12.1	0.00	190.M	1.00K	12.2	%
ERROR(BIT#6)(I+)	-60.6M	25.4M	-7.55M	21.8M	33	97.0	100.	0.00	-190.M	-1.00K	8.36	0.00	190.M	1.00K	9.05	%
ERROR(BIT#6)(I-)	-58.6M	25.6M	-7.06M	21.4M	33	97.0	100.	0.00	-190.M	-1.00K	8.53	0.00	190.M	1.00K	9.19	%
ERROR(BIT#7)(I+)	-9.21M	46.3M	11.5M	14.5M	33	90.9	100.	0.00	-190.M	-1.00K	13.9	0.00	190.M	1.00K	12.3	%
ERROR(BIT#7)(I-)	-7.16M	46.6M	11.9M	14.7M	33	90.9	100.	0.00	-190.M	-1.00K	13.8	0.00	190.M	1.00K	12.2	%
ERROR(BIT#8)(I+)	-33.6M	30.8M	-5.52M	14.5M	33	97.0	100.	0.00	-190.M	-1.00K	12.7	0.00	190.M	1.00K	13.5	%
ERROR(BIT#8)(I-)	-53.5M	47.5M	-4.42M	16.9M	33	93.9	97.0	0.00	-190.M	-1.00K	11.0	0.00	190.M	1.00K	11.5	%
SUM NL+(I+)	13.7M	123.M	70.8M	25.6M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	4.66	%
SUM NL+(I-)	13.3M	118.M	71.3M	24.6M	33	97.0	100.	----	----	-1.00K	----	0.00	190.M	1.00K	4.83	%
SUM NL-(I+)	-168.M	-56.5M	-115.M	24.7M	33	93.9	100.	0.00	-190.M	-1.00K	3.02	----	----	1.00K	----	%
SUM NL-(I-)	-160.M	-56.5M	-114.M	24.3M	33	97.0	100.	0.00	-190.M	-1.00K	3.13	----	----	1.00K	----	%
DELTA SUM NL(I+)	-51.8M	-38.3M	-44.5M	2.93M	33	90.9	100.	6.06	-50.0M	-1.00K	1.88	0.00	50.0M	1.00K	32.2	%
DELTA SUM NL(I-)	-48.6M	-36.6M	-42.6M	2.76M	33	90.9	100.	0.00	-50.0M	-1.00K	2.67	0.00	50.0M	1.00K	33.6	%
NL+(I+)	56.5M	168.M	115.M	24.7M	33	93.9	100.	----	----	-1.00K	----	0.00	190.M	1.00K	3.02	%
NL+(I-)	56.5M	160.M	114.M	24.3M	33	97.0	100.	----	----	-1.00K	----	0.00	190.M	1.00K	3.13	%
NL-(I+)	99.4M	213.M	160.M	24.3M	33	93.9	100.	----	----	-1.00K	----	6.06	190.M	1.00K	1.25	%
NL-(I-)	99.7M	201.M	157.M	24.4M	33	97.0	100.	----	----	-1.00K	----	9.09	190.M	1.00K	1.37	%
DELTA I(1)(I+)	4.02	13.7	8.60	2.33	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	3.18	UA
DELTA I(1)(I-)	4.23	13.7	8.67	2.27	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	3.24	UA
DELTA I(2)(I+)	5.72	11.3	8.20	1.17	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	6.69	UA
DELTA I(2)(I-)	6.00	11.3	8.23	1.16	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	6.69	UA
DELTA I(3)(I+)	4.91	9.86	7.57	1.19	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	7.11	UA
DELTA I(3)(I-)	5.19	10.0	7.58	1.16	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	7.27	UA
DELTA I(4)(I+)	6.93	9.31	7.97	469.M	33	90.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	17.1	UA
DELTA I(4)(I-)	7.00	9.31	7.99	490.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	16.4	UA
DELTA I(5)(I+)	6.64	8.48	7.82	356.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	23.0	UA
DELTA I(5)(I-)	5.82	8.49	7.83	480.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	17.0	UA
DELTA I(6)(I+)	6.67	10.1	8.09	855.M	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	9.26	UA
DELTA I(6)(I-)	6.93	10.0	8.10	858.M	33	93.9	100.	----	----	-1.00K	----	0.00	16.0	1.00K	9.20	UA
DELTA I(7)(I+)	7.02	8.51	7.48	316.M	33	97.0	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	26.9	UA
DELTA I(7)(I-)	6.64	8.89	7.49	368.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	23.1	UA
DELTA I(8)(I+)	7.18	8.51	7.92	298.M	33	97.0	100.	----	----	-1.00K	----	0.00	16.0	1.00K	27.1	UA
DELTA I(8)(I-)	6.87	8.88	7.90	338.M	33	93.9	97.0	----	----	-1.00K	----	0.00	16.0	1.00K	23.9	UA
DELTA IFS	-555.M	505.M	57.3M	215.M	33	93.9	100.	0.00	-8.00	-1.00K	37.5	0.00	8.00	1.00K	37.0	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-5. Statistical data for purchased sample (wide reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT -55 DEG C (TIGHT REJECT LIMITS)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
I+(ALL BITS HIGH)	1.63	3.29	2.46	559.M	33	100.	100.	0.00	400.M	400.M	3.70	0.00	3.80	3.80	2.39	MA
I+(ALL BITS LOW)	1.64	3.30	2.47	555.M	33	100.	100.	0.00	400.M	400.M	3.73	0.00	3.80	3.80	2.39	MA
I-(ALL BITS HIGH)	-7.13	-5.51	-6.31	551.M	33	100.	100.	0.00	-7.80	-7.80	2.71	0.00	-800.M	-800.M	9.99	MA
I-(ALL BITS LOW)	-7.13	-5.53	-6.30	542.M	33	100.	100.	0.00	-7.80	-7.80	2.76	0.00	-800.M	-800.M	10.2	MA
IFS(I+)	1.98	2.01	1.99	6.10M	33	93.9	100.	0.00	1.94	1.94	8.88	0.00	2.04	2.04	7.51	MA
IFS(I-)	1.98	2.01	1.99	6.02M	33	93.9	100.	0.00	1.94	1.94	9.01	0.00	2.04	2.04	7.61	MA
IZS(I+)	-12.5M	1.62	94.6M	320.M	33	93.9	97.0	0.00	-2.00	-2.00	6.55	0.00	2.00	2.00	5.96	UA
IZS(I-)	-13.0M	58.0M	5.92M	14.4M	33	93.9	97.0	0.00	-2.00	-2.00	139.	0.00	2.00	2.00	139.	UA
PSSIFS+1(I+)	-50.1M	40.0M	-3.24M	22.7M	33	93.9	100.	0.00	-4.00	-4.00	176.	0.00	4.00	4.00	176.	UA
PSSIFS+1(I-)	-50.1M	50.1M	-4.42M	27.5M	33	100.	100.	0.00	-4.00	-4.00	145.	0.00	4.00	4.00	145.	UA
PSSIFS+2(I+)	-50.1M	40.0M	-3.24M	22.7M	33	93.9	100.	0.00	-8.00	-8.00	352.	0.00	8.00	8.00	353.	UA
PSSIFS+2(I-)	-50.1M	50.1M	-4.42M	27.5M	33	100.	100.	0.00	-8.00	-8.00	290.	0.00	8.00	8.00	291.	UA
PSSIFS-1(I+)	-550.M	583.M	-75.9M	205.M	32	90.9	93.9	3.03	-8.00	-8.00	38.6	0.00	8.00	8.00	39.4	UA
PSSIFS-1(I-)	-445.M	558.M	-85.6M	198.M	32	93.9	93.9	3.03	-8.00	-8.00	40.1	0.00	8.00	8.00	40.9	UA
PSSIFS-2(I+)	-1.78	38.2M	-340.M	406.M	32	87.9	93.9	3.03	-2.00	-2.00	4.09	0.00	2.00	2.00	5.76	UA
PSSIFS-2(I-)	-1.27	12.6M	-300.M	274.M	33	93.9	97.0	0.00	-2.00	-2.00	6.21	0.00	2.00	2.00	8.41	UA
IFSR1(I+)	2.23	2.97	2.89	154.M	24	69.7	69.7	27.3	2.10	2.10	5.15	0.00	5.80	5.80	18.9	MA
IFSR1(I-)	2.39	2.97	2.86	160.M	28	78.8	84.8	15.2	2.10	2.10	4.76	0.00	5.80	5.80	18.4	MA
IREF-(ALL BITS LOW)	-2.56	-372.M	-927.M	540.M	33	93.9	97.0	0.00	-3.00	-3.00	3.84	0.00	100.M	100.M	1.90	UA
IREF-(ALL BITS HIGH)	-2.56	-366.M	-926.M	539.M	33	93.9	97.0	0.00	-3.00	-3.00	3.85	0.00	100.M	100.M	1.90	UA
IIH(BIT01)	-1.65M	78.2M	7.02M	14.2M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	705.	UA
IIH(BIT02)	-1.00M	27.1M	4.62M	5.60M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	1.79K	UA
IIH(BIT03)	-1.10M	19.7M	4.25M	4.48M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	2.23K	UA
IIH(BIT04)	-400.U	9.60M	3.85M	3.00M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	3.33K	UA
IIH(BIT05)	-1.20M	212.M	14.3M	42.4M	33	93.9	97.0	----	----	-10.0	----	0.00	10.0	10.0	235.	UA
IIH(BIT06)	-200.U	2.14	86.4M	382.M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	25.9	UA
IIH(BIT07)	-200.U	401.M	16.7M	69.0M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	145.	UA
IIH(BIT08)	-1.10M	9.60M	4.08M	3.52M	32	97.0	97.0	----	----	-10.0	----	3.03	10.0	10.0	2.84K	UA
IIL(BIT01)	-7.33	-1.55	-2.53	1.17	32	93.9	93.9	3.03	-10.0	-10.0	6.37	----	----	10.0	----	UA
IIL(BIT02)	-5.89	-1.43	-2.45	983.M	32	93.9	93.9	3.03	-10.0	-10.0	7.68	----	----	10.0	----	UA
IIL(BIT03)	-6.85	-1.48	-2.56	1.12	32	93.9	93.9	3.03	-10.0	-10.0	6.67	----	----	10.0	----	UA
IIL(BIT04)	-7.49	-1.32	-2.56	1.22	32	93.9	93.9	3.03	-10.0	-10.0	6.08	----	----	10.0	----	UA
IIL(BIT05)	-6.47	-1.45	-2.61	1.05	32	93.9	93.9	3.03	-10.0	-10.0	7.04	----	----	10.0	----	UA
IIL(BIT06)	-7.95	-1.38	-2.67	1.26	32	93.9	93.9	3.03	-10.0	-10.0	5.80	----	----	10.0	----	UA
IIL(BIT07)	-7.45	-1.42	-2.69	1.19	32	93.9	93.9	3.03	-10.0	-10.0	6.15	----	----	10.0	----	UA
IIL(BIT08)	-8.34	-1.45	-2.72	1.39	30	87.9	87.9	9.09	-10.0	-10.0	5.23	----	----	10.0	----	UA
IFS+(I+)	1.98	2.04	2.00	15.2M	33	97.0	100.	0.00	1.85	1.85	10.2	0.00	2.08	2.08	4.97	MA
IFS+(I-)	1.98	2.04	2.00	15.2M	33	97.0	100.	0.00	1.85	1.85	10.2	0.00	2.08	2.08	4.94	MA
IFS-(I+)	1.95	2.00	1.99	9.77M	33	97.0	97.0	0.00	1.85	1.85	14.5	0.00	2.08	2.08	9.05	MA
IFS-(I-)	1.95	2.00	1.99	9.27M	33	97.0	97.0	0.00	1.85	1.85	15.3	0.00	2.08	2.08	9.53	MA
DELTA IFSC(I+)	3.11	3.93	3.62	292.M	14	45.5	51.5	0.00	-4.00	-4.00	26.1	57.6	4.00	4.00	1.30	UA
DELTA IFSC(I-)	2.82	3.98	3.47	416.M	14	45.5	60.6	0.00	-4.00	-4.00	17.9	57.6	4.00	4.00	1.28	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits).

STATISTICAL DATA FOR MIXED LOT DAC08 AT -55 DEG C (CONTINUED)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT#1)(I+)	-180.M	86.3M	-62.0M	73.6M	31	93.9	100.	6.06	-190.M	-190.M	1.74	0.00	190.M	190.M	3.43	%
ERROR(BIT#1)(I-)	-186.M	85.4M	-69.9M	73.4M	31	90.9	100.	6.06	-190.M	-190.M	1.64	0.00	190.M	190.M	3.54	%
ERROR(BIT#2)(I+)	-111.M	87.6M	-17.7M	53.4M	33	100.	100.	0.00	-190.M	-190.M	3.23	0.00	190.M	190.M	3.89	%
ERROR(BIT#2)(I-)	-105.M	95.1M	-15.0M	51.4M	33	97.0	100.	0.00	-190.M	-190.M	3.40	0.00	190.M	190.M	3.99	%
ERROR(BIT#3)(I+)	-112.M	82.3M	582.U	44.5M	33	97.0	100.	0.00	-190.M	-190.M	4.28	0.00	190.M	190.M	4.26	%
ERROR(BIT#3)(I-)	-75.3M	90.2M	5.88M	40.0M	33	93.9	100.	0.00	-190.M	-190.M	4.89	0.00	190.M	190.M	4.60	%
ERROR(BIT#4)(I+)	-34.0M	67.4M	12.5M	24.6M	33	97.0	100.	0.00	-190.M	-190.M	8.24	0.00	190.M	190.M	7.22	%
ERROR(BIT#4)(I-)	-33.7M	68.8M	11.2M	23.8M	33	97.0	100.	0.00	-190.M	-190.M	8.47	0.00	190.M	190.M	7.53	%
ERROR(BIT#5)(I+)	-30.8M	60.6M	9.60M	18.7M	33	93.9	100.	0.00	-190.M	-190.M	10.7	0.00	190.M	190.M	9.66	%
ERROR(BIT#5)(I-)	-19.5M	71.9M	10.4M	19.0M	33	97.0	97.0	0.00	-190.M	-190.M	10.5	0.00	190.M	190.M	9.44	%
ERROR(BIT#6)(I+)	-50.2M	40.6M	998.U	24.0M	33	97.0	100.	0.00	-190.M	-190.M	7.97	0.00	190.M	190.M	7.88	%
ERROR(BIT#6)(I-)	-50.2M	71.1M	2.21M	26.6M	33	97.0	100.	0.00	-190.M	-190.M	7.23	0.00	190.M	190.M	7.07	%
ERROR(BIT#7)(I+)	-8.43M	45.5M	16.1M	12.1M	33	93.9	100.	0.00	-190.M	-190.M	17.0	0.00	190.M	190.M	14.4	%
ERROR(BIT#7)(I-)	-7.90M	47.5M	16.7M	11.8M	33	93.9	100.	0.00	-190.M	-190.M	17.5	0.00	190.M	190.M	14.7	%
ERROR(BIT#8)(I+)	-20.2M	31.7M	6.45M	13.0M	33	97.0	100.	0.00	-190.M	-190.M	15.1	0.00	190.M	190.M	14.2	%
ERROR(BIT#8)(I-)	-90.0M	54.0M	7.11M	21.6M	33	93.9	97.0	0.00	-190.M	-190.M	9.11	0.00	190.M	190.M	8.46	%
SUM NL+(I+)	42.1M	171.M	101.M	34.5M	31	90.9	97.0	----	----	0.00	----	6.06	190.M	190.M	2.58	%
SUM NL+(I-)	40.1M	160.M	99.6M	32.5M	30	90.9	93.9	----	----	0.00	----	9.09	190.M	190.M	2.78	%
SUM NL-(I+)	-185.M	-83.8M	-140.M	30.8M	29	87.9	93.9	12.1	-190.M	-190.M	1.62	----	----	0.00	----	%
SUM NL-(I-)	-188.M	-84.8M	-138.M	28.1M	27	84.8	90.9	18.2	-190.M	-190.M	1.86	----	----	0.00	----	%
DELTA SUM NL(I+)	-49.8M	-22.8M	-43.0M	4.50M	31	93.9	97.0	6.06	-50.0M	-50.0M	1.55	0.00	50.0M	50.0M	20.7	%
DELTA SUM NL(I-)	-46.4M	-38.9M	-43.8M	1.69M	33	97.0	100.	0.00	-50.0M	-50.0M	3.67	0.00	50.0M	50.0M	55.4	%
NL+(I+)	83.8M	185.M	140.M	30.8M	29	87.9	93.9	----	----	0.00	----	12.1	190.M	190.M	1.62	%
NL+(I-)	84.8M	188.M	138.M	28.1M	27	84.8	90.9	----	----	0.00	----	18.2	190.M	190.M	1.86	%
NL-(I+)	125.M	189.M	160.M	24.8M	15	66.7	87.9	----	----	0.00	----	54.5	190.M	190.M	1.21	%
NL-(I-)	127.M	184.M	163.M	19.7M	16	63.6	75.8	----	----	0.00	----	51.5	190.M	190.M	1.37	%
DELTA I(1)(I+)	4.03	14.9	10.0	3.02	32	97.0	100.	----	----	0.00	----	3.03	16.0	16.0	1.98	UA
DELTA I(1)(I-)	3.97	14.7	10.2	2.92	31	90.9	100.	----	----	0.00	----	6.06	16.0	16.0	2.00	UA
DELTA I(2)(I+)	5.78	12.8	9.31	1.81	33	100.	100.	----	----	0.00	----	0.00	16.0	16.0	3.70	UA
DELTA I(2)(I-)	5.94	13.3	9.40	1.94	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	3.40	UA
DELTA I(3)(I+)	6.01	13.5	8.82	1.42	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	5.05	UA
DELTA I(3)(I-)	6.12	11.3	8.75	1.21	33	90.9	100.	----	----	0.00	----	0.00	16.0	16.0	6.00	UA
DELTA I(4)(I+)	6.70	9.67	8.26	550.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	14.1	UA
DELTA I(4)(I-)	6.52	11.3	8.35	762.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	10.0	UA
DELTA I(5)(I+)	7.17	9.01	8.09	347.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	22.8	UA
DELTA I(5)(I-)	5.32	8.79	8.13	580.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	13.6	UA
DELTA I(6)(I+)	6.90	10.2	8.24	752.M	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	10.3	UA
DELTA I(6)(I-)	6.26	10.2	8.25	834.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	9.30	UA
DELTA I(7)(I+)	7.19	8.61	7.63	344.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	24.3	UA
DELTA I(7)(I-)	5.85	9.06	7.63	481.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	17.4	UA
DELTA I(8)(I+)	7.12	8.23	7.69	259.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	32.0	UA
DELTA I(8)(I-)	6.75	9.61	7.68	433.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	19.2	UA
DELTA IFS	-2.66	2.57	28.0M	942.M	33	93.9	100.	0.00	-8.00	-8.00	8.52	0.00	8.00	8.00	8.46	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +25 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
I+(ALL BITS HIGH)	1.60	3.43	2.45	525.M	33	100.	100.	0.00	400.M	400.M	3.91	0.00	3.80	3.80	2.57	MA
I+(ALL BITS LOW)	1.61	3.44	2.46	521.M	33	100.	100.	0.00	400.M	400.M	3.96	0.00	3.80	3.80	2.57	MA
I-(ALL BITS HIGH)	-7.28	-5.51	-6.31	522.M	33	100.	100.	0.00	-7.80	-7.80	2.86	0.00	-800.M	-800.M	10.6	MA
I-(ALL BITS LOW)	-7.28	-5.53	-6.29	504.M	33	100.	100.	0.00	-7.80	-7.80	2.99	0.00	-800.M	-800.M	10.9	MA
IFS(I+)	1.98	2.01	2.00	5.40M	33	93.9	100.	0.00	1.94	1.94	10.2	0.00	2.04	2.04	8.33	MA
IFS(I-)	1.98	2.01	2.00	5.39M	33	93.9	100.	0.00	1.94	1.94	10.2	0.00	2.04	2.04	8.33	MA
IZS(I+)	-7.00M	119.M	24.0M	39.9M	33	90.9	100.	0.00	-2.00	-2.00	50.7	0.00	2.00	2.00	49.5	UA
IZS(I-)	-11.5M	127.M	24.2M	41.3M	33	93.9	100.	0.00	-2.00	-2.00	49.0	0.00	2.00	2.00	47.8	UA
PSSIFS+1(I+)	-75.0M	45.2M	-16.4M	29.4M	33	97.0	100.	0.00	-4.00	-4.00	135.	0.00	4.00	4.00	137.	UA
PSSIFS+1(I-)	-70.1M	40.0M	-8.93M	23.4M	33	93.9	100.	0.00	-4.00	-4.00	171.	0.00	4.00	4.00	171.	UA
PSSIFS+2(I+)	-75.0M	45.2M	-16.4M	29.4M	33	97.0	100.	0.00	-8.00	-8.00	271.	0.00	8.00	8.00	272.	UA
PSSIFS+2(I-)	-70.1M	40.0M	-8.93M	23.4M	33	93.9	100.	0.00	-8.00	-8.00	342.	0.00	8.00	8.00	342.	UA
PSSIFS-1(I+)	-950.M	14.9M	-194.M	160.M	33	97.0	97.0	0.00	-8.00	-8.00	48.7	0.00	8.00	8.00	51.2	UA
PSSIFS-1(I-)	-1.05	80.1M	-215.M	176.M	33	97.0	97.0	0.00	-8.00	-8.00	44.2	0.00	8.00	8.00	46.6	UA
PSSIFS-2(I+)	-1.36	-80.1M	-276.M	236.M	31	87.9	90.9	6.06	-2.00	-2.00	7.31	0.00	2.00	2.00	9.65	UA
PSSIFS-2(I-)	-1.41	-130.M	-323.M	293.M	33	93.9	93.9	0.00	-2.00	-2.00	5.72	0.00	2.00	2.00	7.92	UA
IFSR1(I+)	2.52	2.94	2.89	98.3M	28	78.8	81.8	15.2	2.10	2.10	8.01	0.00	5.80	5.80	29.6	MA
IFSR1(I-)	2.25	2.94	2.90	130.M	29	84.8	84.8	12.1	2.10	2.10	6.11	0.00	5.80	5.80	22.3	MA
IREF-(ALL BITS LOW)	-2.49	-426.M	-1.01	545.M	33	93.9	100.	0.00	-3.00	-3.00	3.65	0.00	100.M	100.M	2.05	UA
IREF-(ALL BITS HIGH)	-2.49	-423.M	-1.01	545.M	33	93.9	100.	0.00	-3.00	-3.00	3.64	0.00	100.M	100.M	2.04	UA
IIH(BIT01)	-1.65M	10.5M	3.69M	4.18M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	2.39K	UA
IIH(BIT02)	-1.80M	9.65M	3.32M	3.94M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	2.53K	UA
IIH(BIT03)	-1.75M	14.0M	3.40M	4.01M	33	97.0	100.	----	----	-10.0	----	0.00	10.0	10.0	2.49K	UA
IIH(BIT04)	-1.30M	9.30M	3.43M	3.33M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	3.00K	UA
IIH(BIT05)	-450.U	9.50M	3.41M	3.21M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	3.11K	UA
IIH(BIT06)	-1.20M	9.35M	3.44M	3.26M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	3.06K	UA
IIH(BIT07)	-1.00M	9.30M	3.25M	3.44M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	2.91K	UA
IIH(BIT08)	-1.10M	63.7M	5.08M	11.1M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	903.	UA
IIL(BIT01)	-7.13	-1.75	-2.95	1.20	33	97.0	97.0	0.00	-10.0	-10.0	5.88	----	----	10.0	----	UA
IIL(BIT02)	-5.97	-1.68	-2.83	1.05	33	97.0	100.	0.00	-10.0	-10.0	6.81	----	----	10.0	----	UA
IIL(BIT03)	-6.62	-1.71	-2.96	1.17	33	97.0	97.0	0.00	-10.0	-10.0	6.03	----	----	10.0	----	UA
IIL(BIT04)	-7.19	-1.56	-2.92	1.24	33	97.0	97.0	0.00	-10.0	-10.0	5.72	----	----	10.0	----	UA
IIL(BIT05)	-6.39	-1.72	-2.98	1.13	33	97.0	97.0	0.00	-10.0	-10.0	6.21	----	----	10.0	----	UA
IIL(BIT06)	-7.64	-1.56	-2.95	1.30	33	97.0	97.0	0.00	-10.0	-10.0	5.41	----	----	10.0	----	UA
IIL(BIT07)	-7.26	-1.62	-3.02	1.20	33	97.0	97.0	0.00	-10.0	-10.0	5.80	----	----	10.0	----	UA
IIL(BIT08)	-8.18	-1.69	-3.07	1.40	32	93.9	93.9	3.03	-10.0	-10.0	4.96	----	----	10.0	----	UA
IFS+(I+)	1.98	2.02	2.00	10.2M	33	93.9	100.	0.00	1.85	1.85	14.9	0.00	2.08	2.08	7.76	MA
IFS+(I-)	1.98	2.02	2.00	10.2M	33	93.9	100.	0.00	1.85	1.85	14.9	0.00	2.08	2.08	7.74	MA
IFS-(I+)	1.98	2.00	1.99	5.36M	33	93.9	97.0	0.00	1.85	1.85	26.8	0.00	2.08	2.08	16.1	MA
IFS-(I-)	1.98	2.01	1.99	5.36M	33	93.9	100.	0.00	1.85	1.85	26.8	0.00	2.08	2.08	16.1	MA
DELTA IFSC(I+)	1.75	3.19	2.56	428.M	23	69.7	69.7	0.00	-4.00	-4.00	15.3	30.3	4.00	4.00	3.37	UA
DELTA IFSC(I-)	1.73	3.22	2.55	468.M	23	69.7	69.7	0.00	-4.00	-4.00	14.0	30.3	4.00	4.00	3.10	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +25 DEG C (CONTINUED)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT01)(I+)	-166.M	72.7M	-45.2M	65.8M	33	100.	100.	0.00	-190.M	-190.M	2.20	0.00	190.M	190.M	3.57	%
ERROR(BIT01)(I-)	-171.M	53.6M	-48.8M	62.4M	33	100.	100.	0.00	-190.M	-190.M	2.26	0.00	190.M	190.M	3.82	%
ERROR(BIT02)(I+)	-83.9M	56.4M	-13.3M	41.0M	33	100.	100.	0.00	-190.M	-190.M	4.31	0.00	190.M	190.M	4.96	%
ERROR(BIT02)(I-)	-79.3M	53.2M	-12.8M	40.0M	33	100.	100.	0.00	-190.M	-190.M	4.43	0.00	190.M	190.M	5.07	%
ERROR(BIT03)(I+)	-63.6M	57.3M	5.23M	31.4M	33	97.0	100.	0.00	-190.M	-190.M	6.22	0.00	190.M	190.M	5.88	%
ERROR(BIT03)(I-)	-47.1M	58.7M	6.90M	29.7M	33	100.	100.	0.00	-190.M	-190.M	6.62	0.00	190.M	190.M	6.16	%
ERROR(BIT04)(I+)	-42.5M	38.5M	-1.00M	20.8M	33	100.	100.	0.00	-190.M	-190.M	9.08	0.00	190.M	190.M	9.17	%
ERROR(BIT04)(I-)	-43.4M	39.1M	-1.15M	21.1M	33	97.0	100.	0.00	-190.M	-190.M	8.96	0.00	190.M	190.M	9.07	%
ERROR(BIT05)(I+)	-25.6M	38.0M	3.21M	15.1M	33	97.0	100.	0.00	-190.M	-190.M	12.8	0.00	190.M	190.M	12.3	%
ERROR(BIT05)(I-)	-21.2M	39.8M	3.70M	15.3M	33	97.0	100.	0.00	-190.M	-190.M	12.7	0.00	190.M	190.M	12.2	%
ERROR(BIT06)(I+)	-56.5M	30.3M	-4.69M	22.1M	33	97.0	100.	0.00	-190.M	-190.M	8.37	0.00	190.M	190.M	8.79	%
ERROR(BIT06)(I-)	-56.1M	30.8M	-4.22M	22.2M	33	97.0	100.	0.00	-190.M	-190.M	8.39	0.00	190.M	190.M	8.77	%
ERROR(BIT07)(I+)	-9.88M	43.6M	12.3M	12.6M	33	97.0	100.	0.00	-190.M	-190.M	16.1	0.00	190.M	190.M	14.1	%
ERROR(BIT07)(I-)	-9.93M	44.1M	12.6M	12.5M	33	97.0	100.	0.00	-190.M	-190.M	16.2	0.00	190.M	190.M	14.2	%
ERROR(BIT08)(I+)	-27.2M	28.3M	-1.08M	12.6M	33	93.9	100.	0.00	-190.M	-190.M	15.0	0.00	190.M	190.M	15.2	%
ERROR(BIT08)(I-)	-67.0M	45.5M	141.U	17.3M	33	93.9	97.0	0.00	-190.M	-190.M	11.0	0.00	190.M	190.M	10.9	%
SUM NL+(I+)	27.1M	140.M	77.9M	27.8M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	4.03	%
SUM NL+(I-)	28.4M	137.M	76.9M	27.0M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	4.19	%
SUM NL-(I+)	-183.M	-72.0M	-122.M	27.1M	33	93.9	100.	0.00	-190.M	-190.M	2.50	----	----	0.00	----	%
SUM NL-(I-)	-180.M	-72.4M	-121.M	25.9M	33	93.9	100.	0.00	-190.M	-190.M	2.68	----	----	0.00	----	%
DELTA SUM NL(I+)	-47.6M	-39.4M	-44.5M	2.10M	33	97.0	100.	0.00	-50.0M	-50.0M	2.62	0.00	50.0M	50.0M	45.0	%
DELTA SUM NL(I-)	-50.0M	-37.4M	-43.4M	2.72M	32	87.9	97.0	3.03	-50.0M	-50.0M	2.42	0.00	50.0M	50.0M	34.3	%
NL+(I+)	72.0M	183.M	122.M	27.1M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	2.50	%
NL+(I-)	72.4M	180.M	121.M	25.9M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	2.68	%
NL-(I+)	117.M	189.M	158.M	19.4M	27	84.8	93.9	----	----	0.00	----	18.2	190.M	190.M	1.64	%
NL-(I-)	116.M	185.M	156.M	18.5M	27	84.8	93.9	----	----	0.00	----	18.2	190.M	190.M	1.85	%
DELTA I(1)(I+)	4.59	14.0	9.18	2.62	33	100.	100.	----	----	0.00	----	0.00	16.0	16.0	2.60	UA
DELTA I(1)(I-)	5.21	14.2	9.31	2.48	33	100.	100.	----	----	0.00	----	0.00	16.0	16.0	2.69	UA
DELTA I(2)(I+)	6.06	11.8	8.59	1.29	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	5.73	UA
DELTA I(2)(I-)	6.37	11.9	8.65	1.29	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	5.68	UA
DELTA I(3)(I+)	5.78	9.80	7.99	1.04	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	7.72	UA
DELTA I(3)(I-)	5.83	9.83	8.00	1.00	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	8.00	UA
DELTA I(4)(I+)	7.14	9.35	8.07	461.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	17.2	UA
DELTA I(4)(I-)	7.26	9.65	8.11	505.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	15.6	UA
DELTA I(5)(I+)	6.76	8.56	7.89	336.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	24.1	UA
DELTA I(5)(I-)	5.58	8.61	7.92	504.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	16.0	UA
DELTA I(6)(I+)	6.77	10.2	8.13	778.M	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	10.1	UA
DELTA I(6)(I-)	6.76	10.1	8.16	807.M	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	9.72	UA
DELTA I(7)(I+)	7.12	8.58	7.55	313.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	27.0	UA
DELTA I(7)(I-)	6.37	8.94	7.58	391.M	33	93.9	93.9	----	----	0.00	----	0.00	16.0	16.0	21.5	UA
DELTA I(8)(I+)	7.26	8.36	7.84	253.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	32.3	UA
DELTA I(8)(I-)	6.92	9.16	7.82	346.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	23.7	UA
DELTA IFS	-1.08	450.M	-21.7M	313.M	33	93.9	97.0	0.00	-8.00	-8.00	25.5	0.00	8.00	8.00	25.6	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +125 DEG C

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
I+(ALL BITS HIGH)	1.44	3.45	2.32	541.M	33	93.9	100.	0.00	400.M	400.M	3.55	0.00	3.80	3.80	2.73	MA
I+(ALL BITS LOW)	1.46	3.47	2.33	540.M	33	93.9	100.	0.00	400.M	400.M	3.57	0.00	3.80	3.80	2.72	MA
I-(ALL BITS HIGH)	-7.31	-5.36	-6.19	541.M	33	93.9	100.	0.00	-7.80	-7.80	2.98	0.00	-800.M	-800.M	9.95	MA
I-(ALL BITS LOW)	-7.31	-5.37	-6.17	529.M	33	93.9	100.	0.00	-7.80	-7.80	3.07	0.00	-800.M	-800.M	10.2	MA
IFS(I+)	1.98	2.01	1.99	5.28M	33	93.9	100.	0.00	1.94	1.94	10.2	0.00	2.04	2.04	8.71	MA
IFS(I-)	1.98	2.01	1.99	5.26M	33	93.9	100.	0.00	1.94	1.94	10.3	0.00	2.04	2.04	8.75	MA
IZS(I+)	14.5M	544.M	136.M	160.M	33	90.9	100.	0.00	-2.00	-2.00	13.4	0.00	2.00	2.00	11.7	UA
IZS(I-)	9.50M	356.M	93.9M	111.M	33	90.9	100.	0.00	-2.00	-2.00	18.9	0.00	2.00	2.00	17.2	UA
PSSIFS+1(I+)	-115.M	44.9M	-35.8M	34.1M	33	93.9	100.	0.00	-4.00	-4.00	116.	0.00	4.00	4.00	118.	UA
PSSIFS+1(I-)	-140.M	20.0M	-41.1M	42.2M	33	93.9	100.	0.00	-4.00	-4.00	93.7	0.00	4.00	4.00	95.7	UA
PSSIFS+2(I+)	-115.M	44.9M	-35.8M	34.1M	33	93.9	100.	0.00	-8.00	-8.00	233.	0.00	8.00	8.00	235.	UA
PSSIFS+2(I-)	-140.M	20.0M	-41.1M	42.2M	33	93.9	100.	0.00	-8.00	-8.00	188.	0.00	8.00	8.00	190.	UA
PSSIFS-1(I+)	-440.M	-60.1M	-244.M	99.4M	33	100.	100.	0.00	-8.00	-8.00	78.0	0.00	8.00	8.00	82.9	UA
PSSIFS-1(I-)	-455.M	-100.M	-266.M	101.M	33	100.	100.	0.00	-8.00	-8.00	76.6	0.00	8.00	8.00	81.9	UA
PSSIFS-2(I+)	-1.70	-120.M	-470.M	398.M	27	75.8	78.8	18.2	-2.00	-2.00	3.83	0.00	2.00	2.00	6.22	UA
PSSIFS-2(I-)	-1.13	-130.M	-415.M	248.M	29	81.8	87.9	12.1	-2.00	-2.00	6.40	0.00	2.00	2.00	9.76	UA
IFSR1(I+)	2.56	4.02	3.14	448.M	24	72.7	78.8	27.3	2.10	2.10	2.33	0.00	5.80	5.80	5.92	MA
IFSR1(I-)	2.41	4.05	3.20	543.M	26	78.8	87.9	21.2	2.10	2.10	2.03	0.00	5.80	5.80	4.78	MA
IREF-(ALL BITS LOW)	-2.22	-306.M	-993.M	512.M	33	97.0	100.	0.00	-3.00	-3.00	3.92	0.00	100.M	100.M	2.13	UA
IREF-(ALL BITS HIGH)	-2.23	-297.M	-992.M	516.M	33	97.0	100.	0.00	-3.00	-3.00	3.89	0.00	100.M	100.M	2.12	UA
IIH(BIT#1)	1.70M	25.8M	12.2M	7.22M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	1.38K	UA
IIH(BIT#2)	1.55M	23.8M	12.2M	7.42M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	1.35K	UA
IIH(BIT#3)	1.70M	28.3M	12.6M	8.15M	33	100.	100.	----	----	-10.0	----	0.00	10.0	10.0	1.23K	UA
IIH(BIT#4)	1.20M	29.1M	12.5M	8.25M	33	97.0	100.	----	----	-10.0	----	0.00	10.0	10.0	1.21K	UA
IIH(BIT#5)	550.U	30.9M	12.1M	8.14M	33	93.9	100.	----	----	-10.0	----	0.00	10.0	10.0	1.23K	UA
IIH(BIT#6)	900.U	75.4M	14.1M	13.9M	33	97.0	97.0	----	----	-10.0	----	0.00	10.0	10.0	721.	UA
IIH(BIT#7)	1.05M	37.5M	13.3M	9.46M	33	93.9	100.	----	----	-10.0	----	0.00	10.0	10.0	1.06K	UA
IIH(BIT#8)	800.U	30.2M	12.0M	7.72M	33	97.0	100.	----	----	-10.0	----	0.00	10.0	10.0	1.29K	UA
IIL(BIT#1)	-6.01	-1.80	-3.05	1.12	33	97.0	100.	0.00	-10.0	-10.0	6.19	----	----	10.0	----	UA
IIL(BIT#2)	-5.20	-1.70	-2.91	1.01	33	97.0	100.	0.00	-10.0	-10.0	7.03	----	----	10.0	----	UA
IIL(BIT#3)	-5.65	-1.77	-3.03	1.09	33	97.0	100.	0.00	-10.0	-10.0	6.39	----	----	10.0	----	UA
IIL(BIT#4)	-6.09	-1.66	-3.00	1.15	33	97.0	100.	0.00	-10.0	-10.0	6.11	----	----	10.0	----	UA
IIL(BIT#5)	-5.34	-1.77	-3.05	1.06	33	97.0	100.	0.00	-10.0	-10.0	6.55	----	----	10.0	----	UA
IIL(BIT#6)	-6.33	-1.64	-3.00	1.18	33	97.0	100.	0.00	-10.0	-10.0	5.94	----	----	10.0	----	UA
IIL(BIT#7)	-6.03	-1.74	-3.05	1.10	33	97.0	100.	0.00	-10.0	-10.0	6.31	----	----	10.0	----	UA
IIL(BIT#8)	-6.93	-1.71	-3.13	1.30	32	93.9	97.0	3.03	-10.0	-10.0	5.28	----	----	10.0	----	UA
IFS+(I+)	1.98	2.01	2.00	8.12M	33	97.0	100.	0.00	1.85	1.85	18.2	0.00	2.08	2.08	10.1	MA
IFS+(I-)	1.98	2.01	2.00	8.13M	33	97.0	100.	0.00	1.85	1.85	18.2	0.00	2.08	2.08	10.1	MA
IFS-(I+)	1.98	2.00	1.99	5.22M	33	90.9	100.	0.00	1.85	1.85	27.4	0.00	2.08	2.08	16.7	MA
IFS-(I-)	1.98	2.01	1.99	5.20M	33	93.9	100.	0.00	1.85	1.85	27.4	0.00	2.08	2.08	16.8	MA
DELTA IFSC(I+)	1.48	2.97	2.17	398.M	23	66.7	69.7	0.00	-4.00	-4.00	15.5	30.3	4.00	4.00	4.59	UA
DELTA IFSC(I-)	1.41	2.72	2.13	404.M	23	69.7	69.7	0.00	-4.00	-4.00	15.2	30.3	4.00	4.00	4.62	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits). (cont'd.)

STATISTICAL DATA FOR MIXED LOT DAC08 AT +125 DEG C (CONTINUED)

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN *	SIGMA *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW	LOW LIMIT	LOW REJ	LO-FM *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM *	UNITS
ERROR(BIT01)(I+)	-157.M	84.8M	-30.6M	58.1M	33	97.0	100.	0.00	-190.M	-190.M	2.74	0.00	190.M	190.M	3.80	%
ERROR(BIT01)(I-)	-160.M	81.8M	-32.2M	57.1M	33	97.0	100.	0.00	-190.M	-190.M	2.76	0.00	190.M	190.M	3.89	%
ERROR(BIT02)(I+)	-77.4M	45.3M	-10.4M	33.6M	33	100.	100.	0.00	-190.M	-190.M	5.34	0.00	190.M	190.M	5.96	%
ERROR(BIT02)(I-)	-73.4M	46.2M	-10.5M	33.2M	33	100.	100.	0.00	-190.M	-190.M	5.40	0.00	190.M	190.M	6.04	%
ERROR(BIT03)(I+)	-51.2M	63.2M	7.41M	31.0M	33	100.	100.	0.00	-190.M	-190.M	6.37	0.00	190.M	190.M	5.89	%
ERROR(BIT03)(I-)	-40.3M	60.7M	8.08M	30.2M	33	100.	100.	0.00	-190.M	-190.M	6.56	0.00	190.M	190.M	6.02	%
ERROR(BIT04)(I+)	-55.8M	29.1M	-8.21M	22.4M	33	97.0	100.	0.00	-190.M	-190.M	8.10	0.00	190.M	190.M	8.83	%
ERROR(BIT04)(I-)	-55.5M	29.3M	-7.86M	22.7M	33	97.0	100.	0.00	-190.M	-190.M	8.04	0.00	190.M	190.M	8.73	%
ERROR(BIT05)(I+)	-23.5M	34.7M	-1.10M	15.3M	33	93.9	100.	0.00	-190.M	-190.M	12.3	0.00	190.M	190.M	12.5	%
ERROR(BIT05)(I-)	-23.2M	38.0M	-551.U	15.6M	33	97.0	100.	0.00	-190.M	-190.M	12.1	0.00	190.M	190.M	12.2	%
ERROR(BIT06)(I+)	-60.6M	25.4M	-7.55M	21.8M	33	97.0	100.	0.00	-190.M	-190.M	8.36	0.00	190.M	190.M	9.05	%
ERROR(BIT06)(I-)	-58.6M	25.6M	-7.06M	21.4M	33	97.0	100.	0.00	-190.M	-190.M	8.53	0.00	190.M	190.M	9.19	%
ERROR(BIT07)(I+)	-9.21M	46.3M	11.5M	14.5M	33	90.9	100.	0.00	-190.M	-190.M	13.9	0.00	190.M	190.M	12.3	%
ERROR(BIT07)(I-)	-7.16M	46.6M	11.9M	14.7M	33	90.9	100.	0.00	-190.M	-190.M	13.8	0.00	190.M	190.M	12.2	%
ERROR(BIT08)(I+)	-33.6M	30.8M	-5.52M	14.5M	33	97.0	100.	0.00	-190.M	-190.M	12.7	0.00	190.M	190.M	13.5	%
ERROR(BIT08)(I-)	-53.5M	47.5M	-4.42M	16.9M	33	93.9	97.0	0.00	-190.M	-190.M	11.0	0.00	190.M	190.M	11.5	%
SUM NL+(I+)	13.7M	123.M	70.8M	25.6M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	4.66	%
SUM NL+(I-)	13.3M	118.M	71.3M	24.6M	33	97.0	100.	----	----	0.00	----	0.00	190.M	190.M	4.83	%
SUM NL-(I+)	-168.M	-56.5M	-115.M	24.7M	33	93.9	100.	0.00	-190.M	-190.M	3.02	----	----	0.00	----	%
SUM NL-(I-)	-160.M	-56.5M	-114.M	24.3M	33	97.0	100.	0.00	-190.M	-190.M	3.13	----	----	0.00	----	%
DELTA SUM NL(I+)	-48.6M	-38.3M	-44.0M	2.35M	31	87.9	93.9	6.06	-50.0M	-50.0M	2.54	0.00	50.0M	50.0M	40.0	%
DELTA SUM NL(I-)	-48.6M	-36.6M	-42.6M	2.76M	33	90.9	100.	0.00	-50.0M	-50.0M	2.67	0.00	50.0M	50.0M	33.6	%
NL+(I+)	56.5M	168.M	115.M	24.7M	33	93.9	100.	----	----	0.00	----	0.00	190.M	190.M	3.02	%
NL+(I-)	56.5M	160.M	114.M	24.3M	33	97.0	100.	----	----	0.00	----	0.00	190.M	190.M	3.13	%
NL-(I+)	99.4M	188.M	157.M	21.9M	31	93.9	100.	----	----	0.00	----	6.06	190.M	190.M	1.51	%
NL-(I-)	99.7M	184.M	153.M	22.0M	30	93.9	100.	----	----	0.00	----	9.09	190.M	190.M	1.69	%
DELTA I(1)(I+)	4.02	13.7	8.60	2.33	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	3.18	UA
DELTA I(1)(I-)	4.23	13.7	8.67	2.27	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	3.24	UA
DELTA I(2)(I+)	5.72	11.3	8.20	1.17	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	6.69	UA
DELTA I(2)(I-)	6.00	11.3	8.23	1.16	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	6.69	UA
DELTA I(3)(I+)	4.91	9.86	7.57	1.19	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	7.11	UA
DELTA I(3)(I-)	5.19	10.0	7.58	1.16	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	7.27	UA
DELTA I(4)(I+)	6.93	9.31	7.97	469.M	33	90.9	100.	----	----	0.00	----	0.00	16.0	16.0	17.1	UA
DELTA I(4)(I-)	7.00	9.31	7.99	490.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	16.4	UA
DELTA I(5)(I+)	6.64	8.48	7.82	356.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	23.0	UA
DELTA I(5)(I-)	5.82	8.49	7.83	480.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	17.0	UA
DELTA I(6)(I+)	6.67	10.1	8.09	855.M	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	9.26	UA
DELTA I(6)(I-)	6.93	10.0	8.10	858.M	33	93.9	100.	----	----	0.00	----	0.00	16.0	16.0	9.20	UA
DELTA I(7)(I+)	7.02	8.51	7.48	316.M	33	97.0	97.0	----	----	0.00	----	0.00	16.0	16.0	26.9	UA
DELTA I(7)(I-)	6.64	8.89	7.49	368.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	23.1	UA
DELTA I(8)(I+)	7.18	8.51	7.92	298.M	33	97.0	100.	----	----	0.00	----	0.00	16.0	16.0	27.1	UA
DELTA I(8)(I-)	6.87	8.88	7.90	338.M	33	93.9	97.0	----	----	0.00	----	0.00	16.0	16.0	23.9	UA
DELTA IFS	-555.M	505.M	57.3M	215.M	33	93.9	100.	0.00	-8.00	-8.00	37.5	0.00	8.00	8.00	37.0	UA

* EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ

Table 6-6. Statistical data for purchased sample (tight reject limits). (cont'd.)

TABLE 6-7. Comparison of GE/Signetics

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Units
1	I+	3.280	3.27	3.320	3.35	3.240	3.28	mA
24		2.075	2.02	2.000	1.97	1.810	1.79	
35		1.555	1.55	1.455	1.47	1.290	1.31	
47		2.430	2.49	2.525	2.42	2.170	2.15	
70		2.095	2.05	2.120	2.13	1.985	2.00	
1	I-	-7.125	-7.17	-7.185	-7.24	-7.100	-7.17	mA
24		-5.930	-5.94	-5.870	-5.89	-5.690	-5.72	
35		-5.445	-5.50	-5.365	-5.43	-5.210	-5.27	
47		-6.365	-6.39	-6.280	-6.30	-6.025	-6.05	
70		-5.960	-5.97	-6.000	-6.04	-5.890	-5.93	
1	IFS(I_O)	1.994	1.9828	1.995	1.9825	1.992	1.9802	mA
24		1.995	1.9824	1.996	1.9828	1.995	1.9819	
35		1.996	1.9869	1.999	1.9878	1.998	1.9878	
47		1.988	1.9782	1.987	1.9690	1.985	1.9745	
70		1.988	1.9761	1.990	1.9777	1.989	1.9781	
1	IFS($\bar{I}_O$)	1.994	-	1.994	-	1.991	-	mA
24		1.994	-	1.996	-	1.995	-	
35		1.996	-	1.999	-	1.998	-	
47		1.988	-	1.987	-	1.985	-	
70		1.988	-	1.991	-	1.989	-	
1	IZS(I_O)	26.00M	-200M	97.50M	-510M	353.5M	-210M	uA
24		-1.000M	-220M	8.000M	-600M	82.50M	-390M	
35		-500.0u	-210M	30.00M	-590M	190.0M	-170M	
47		62.00M	-160M	158.5M	-440M	399.0M	-130M	
70		109.5M	-200M	81.00M	-530M	452.0M	-470M	
1	IZS($\bar{I}_O$)	26.00M	-190M	105.5M	-500M	325.5M	-260M	uA
24		-500.0u	-210M	10.50M	-590M	50.50M	-550M	
35		4.000M	-210M	22.00M	-570M	120.0M	-470M	
47		64.50M	-150M	157.0M	-440M	369.0M	-190M	
70		22.50M	-190M	81.50M	-520M	230.0M	-360M	

*M = milli (-200M = -0.2)

*u = micro (-500.0 u = -0.0005)

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	PSSIFS+1	-24.91M	-10M	0.000	0.02	-70.08M	0.06	uA
24	(I_O)	-19.79M	-20M	25.15M	0.0	-15.13M	0.02	
35		10.01M	+10M	-24.91M	0.0	-30.04M	0.03	
47		-49.83M	+50M	-50.06M	-60M	-100.1M	0.11	
70		0.000	0.0	-15.13M	-10M	-50.06M	0.04	
1	PSSIFS+1	34.92M	-	-20.02M	-	5.122M	-	uA
24	($\overline{I}_O$)	20.02M	-	-40.05M	-	-80.09M	-	
35		-20.02M	-	-20.02M	-	-84.98M	-	
47		0.000	-	-50.06M	-	-99.88M	-	
70		0.000	-	-40.05M	-	-149.9M	-	
1	PSSIFS+2	-24.91M	-40M	0.000	-30M	-70.08M	10M	uA
24	(I_O)	-19.79M	-30M	25.15M	-30M	-15.13M	0	
35		10.01M	-40M	-24.91M	-10M	-30.04M	10M	
47		-49.83M	-20M	-50.06M	+10M	-100.1M	50M	
70		0.000	-40M	-15.13M	-20M	-50.06M	10M	
1	PSSIFS+2	34.92M	-	-20.02M	-	5.122M	-	uA
24	($\overline{I}_O$)	20.02M	-	-40.05M	-	-80.09M	-	
35		-20.02M	-	-20.02M	-	-84.98M	-	
47		0.000	-	-50.06M	-	-99.88M	-	
70		0.000	-	-40.05M	-	-149.9M	-	
1	PSSIFS-1	-74.97M	+90M	-114.8M	+120M	-115.0M	200M	uA
24	(I_O)	-100.1M	+60M	-70.08M	+120M	-84.98M	190M	
35		-99.88M	+20M	-60.07M	+100M	-125.0M	150M	
47		250.1M	-40M	99.88M	+50M	50.06M	130M	
70		-150.2M	+140M	-64.96M	+170M	-149.9M	250M	
1	PSSIFS-1	-79.86M	-	-64.96M	-	-145.1M	-	uA
24	($\overline{I}_O$)	-80.09M	-	-84.98M	-	-140.2M	-	
35		-60.07M	-	-94.99M	-	-160.0M	-	
47		300.1M	-	149.9M	-	50.06M	-	
70		-149.9M	-	-180.0M	-	-149.9M	-	

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameters	T_A = -55°C GEOS	Sig	T_A = +25°C GEOS	Sig	T_A = +125°C GEOS	Sig	Unit
1	PSSIFS-2	-295.0M	270M	-255.2M	280M	-285.0M	360M	uA
24	(I_o)	-129.9M	140M	-175.1M	200M	-655.0M	290M	
35		-329.9M	120M	-315.0M	160M	-4.865*	240M	
47		-150.2M	110M	-200.0M	170M	-600.0M	260M	
70		-299.9M	220M	-300.1M	280M	-450.1M	370M	
1	PSSIFS-2	-335.0M	-	-270.1M	-	-295.0M	-	uA
24	($\bar{I}_o$)	-129.9M	-	-165.1M	-	-585.1M	-	
35		-220.0M	-	-280.1M	-	-3.190*	-	
47		-100.1M	-	-149.9M	-	-349.9M	-	
70		-250.1M	-	-299.9M	-	-400.0M	-	
1	IFSR1(I_o)	2.110	-	2.880	-	2.730	-	mA
24		2.930	-	2.930	-	2.640	-	
35		1.610*	-	1.730*	-	1.370*	-	
47		2.890	-	2.870	-	1.766*	-	
70		1.636*	-	2.680	-	2.016*	-	
1	IFSR1($\bar{I}_o$)	2.750	-	2.930	-	2.910	-	mA
24		2.930	-	2.930	-	2.660	-	
35		2.029*	-	2.070*	-	1.628*	-	
47		2.910	-	2.900	-	2.290	-	
70		2.240	-	2.860	-	2.310	-	
1	IFSR2(I_o)	1.915*	-	3.780*	-	3.450*	-	mA
24		4.010*	-	4.020*	-	2.210*	-	
35		2.460*	-	2.290*	-	2.040*	-	
47		4.030*	-	3.680*	-	1.775*	-	
70		2.004*	-	2.100*	-	1.838*	-	
1	IFSR2($\bar{I}_o$)	3.690*	-	4.020*	-	4.020*	-	mA
24		4.010*	-	4.020*	-	2.530*	-	
35		3.320*	-	2.970*	-	2.460*	-	
47		4.020*	-	4.030*	-	2.920*	-	
70		3.280*	-	3.340*	-	2.740*	-	

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	IREF-	-1.875	-2.21	-1.980	-2.34	-1.915	-2.25	uA
24		-383.0M	-0.74	-452.5M	-0.83	-492.5M	-0.85	
35		-452.0M	-0.81	-492.5M	-0.86	-484.0M	-0.86	
47		-1.965	-2.31	-1.925	-2.27	-1.570	-1.90	
70		-1.120	-1.47	-1.150	-1.50	-965.0M	-1.31	
1	IIH(Bit #1)	9.200M	-0.1	3.650M	-0.1	20.10M	0	uA
24		950.0u	0	6.750M	-0.1	6.000M	-0.1	
35		7.650M	0	4.700M	-0.1	3.750M	-0.1	
47		7.050M	0	-1.050M	-0.1	13.15M	-0.1	
70		9.200M	0	-300.0u	-0.1	15.05M	-0.1	
1	IIH(Bit #2)	7.900M	0	5.050M	0	16.95M	0	uA
24		3.150M	0	7.400M	0	4.950M	0	
35		8.150M	0	3.950M	-0.1	4.250M	0	
47		7.650M	0	-700.0u	0	11.65M	0	
70		9.500M	0	-1.350M	0	13.50M	0	
1	IIH(Bit #3)	6.700M	0	6.350M	0	16.70M	0	uA
24		4.700M	0	8.150M	-0.1	4.300M	0	
35		8.950M	+0.1	2.900M	0	11.50M	0	
47		8.400M	0	400.0u	0	11.25M	0	
70		9.200M	0	900.0u	0	11.50M	0	
1	IIH(Bit #4)	5.650M	0	7.550M	0	15.50M	0	uA
24		6.150M	+0.1	9.000M	0	3.500M	0	
35		9.300M	+0.1	1.700M	0	10.55M	0	
47		9.050M	0	2.900M	0	10.10M	0	
70		8.350M	0	-1.850M	0	10.45M	+0.1	
1	IIH(Bit #5)	4.850M	0	8.350M	-0.1	13.25M	0	uA
24		7.250M	0	9.450M	-0.1	2.950M	0	
35		9.350M	0	900.0u	0	12.25M	0	
47		9.400M	-0.1	4.600M	0	8.400M	0	
70		7.150M	0	-50.0u	-0.1	9.650M	0	

TABLE 6-7. Comparison of GE/Signetics

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	Sig	T_A = +25°C GEOS	Sig	T_A = +125°C GEOS	Sig	Unit
1	IIH(Bit #6)	4.250M	0	9.050M	0	11.35M	0	uA
24		8.100M	0	9.550M	0	2.450M	0	
35		8.800M	0	-50.00u	0	13.90M	0	
47		9.350M	0	5.950M	0	8.250M	0	
70		6.100M	0	400.0u	0	8.850M	0	
1	IIH(Bit #7)	3.600M	0	9.200M	0	10.30M	0	uA
24		8.850M	0	8.800M	0	2.250M	-0.1	
35		7.900M	0	-1.150M	0	14.50M	0	
47		8.300M	0	7.000M	0	7.750M	0	
70		5.200M	0	200.0u	0	8.750M	0	
1	IIH(Bit #8)	3.200M	0	9.500M	0	9.250M	0	uA
24		9.400M	0	7.800M	-0.1	2.150M	0	
35		6.700M	-0.1	-1.300M	-0.1	14.80M	0	
47		7.400M	-0.1	8.000M	0	8.900M	0	
70		4.500M	-0.1	250.0u	-0.1	6.700M	0	
1	IIL(Bit #1)	-4.705	-4.3	-5.195	-4.9	-5.245	-5.0	uA
24		-1.305	-1.4	-1.565	-1.6	-1.690	-1.7	
35		-1.480	-1.6	-1.580	-1.7	-1.575	-1.7	
47		-4.050	-4.0	-4.270	-4.0	-3.950	-3.6	
70		-2.810	-2.8	-3.050	-3.0	-2.720	-2.7	
1	IIL(Bit #2)	-4.170	-3.9	-4.600	-4.3	-4.595	-4.4	uA
24		-1.365	-1.5	-1.610	-1.7	-1.715	-1.7	
35		-1.455	-1.7	-1.575	-1.7	-1.600	-1.7	
47		-3.655	-3.7	-3.905	-3.7	-3.625	-3.4	
70		-2.645	-2.7	-2.840	-2.8	-2.515	-2.5	
1	IIL(Bit #3)	-4.350	-4.1	-4.730	-4.4	-4.670	-4.4	uA
24		-1.385	-1.5	-1.615	-1.6	-1.700	-1.7	
35		-1.540	-1.8	-1.630	-1.8	-1.655	-1.8	
47		-4.180	-4.2	-4.340	-4.1	-4.000	-3.7	
70		-2.795	-2.8	-2.980	-3.0	-2.600	-2.6	

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	IIL(Bit #4)	-4.285	-4.0	-4.655	-4.4	-4.635	-4.4	uA
24		-1.385	-1.5	-1.625	-1.7	-1.725	-1.8	
35		-1.585	-1.8	-1.660	-1.8	-1.645	-1.8	
47		-3.945	-3.9	-4.130	-3.9	-3.835	-3.6	
70		-2.700	-2.7	-2.860	-2.9	-2.550	-2.6	
1	IIL(Bit #5)	-4.450	-4.1	-4.830	-4.5	-4.775	-4.5	uA
24		-1.345	-1.4	-1.590	-1.6	-1.700	-1.7	
35		-1.555	-1.7	-1.670	-1.8	-1.700	-1.8	
47		-4.370	-4.3	-4.515	-4.2	-4.045	-3.8	
70		-2.930	-2.9	-3.120	-3.1	-2.745	-2.7	
1	IIL(Bit #6)	-4.420	-4.1	-4.820	-4.6	-4.765	-4.6	uA
24		-1.400	-1.5	-1.645	-1.7	-1.730	-1.8	
35		-1.545	-1.8	-1.630	-1.8	-1.670	-1.8	
47		-4.205	-4.2	-4.350	-4.1	-3.915	-3.7	
70		-3.015	-3.0	-3.145	-3.2	-2.765	-2.8	
1	IIL(Bit #7)	-4.305	-4.1	-4.695	-4.5	-4.680	-4.5	uA
24		-1.330	-1.4	-1.610	-1.7	-1.740	-1.8	
35		-1.490	-1.7	-1.620	-1.8	-1.645	-1.8	
47		-4.230	-4.2	-4.385	-4.2	-3.935	-3.7	
70		-2.900	-2.9	-3.100	-3.1	-2.725	-2.7	
1	IIL(Bit #8)	-4.840	-4.5	-5.400	-5.1	-5.450	-5.2	
24		-1.445	-1.5	-1.660	-1.7	-1.775	-1.8	
35		-1.720	-1.9	-1.805	-2.0	-1.825	-1.9	
47		-4.200	-4.1	-4.445	-4.3	-4.070	-3.8	
70		-2.980	-3.0	-3.285	-3.3	-2.940	-2.9	
1	IFS+(I_O)	1.997	-	1.996	-	1.993	-	mA
24		1.996	-	1.997	-	1.995	-	
35		2.001	-	2.001	-	2.000	-	
47		1.991	-	1.989	-	1.986	-	
70		1.991	-	1.992	-	1.990	-	

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Units
1	IFS+($\bar{I}_O$)	1.996	-	1.996	-	1.992	-	mA
24		1.996	-	1.997	-	1.995	-	
35		2.001	-	2.001	-	2.001	-	
47		1.992	-	1.989	-	1.986	-	
70		1.991	-	1.992	-	1.990	-	
1	IFS-(I_O)	1.993	-	1.994	-	1.991	-	
24		1.994	-	1.995	-	1.994	-	
35		1.995	-	1.998	-	1.997	-	
47		1.987	-	1.986	-	1.984	-	
70		1.986	-	1.989	-	1.988	-	
1	IFS-($\bar{I}_O$)	1.992	-	1.993	-	1.991	-	
24		1.993	-	1.995	-	1.994	-	
35		1.995	-	1.998	-	1.997	-	
47		1.987	-	1.986	-	1.984	-	
70		1.987	-	1.989	-	1.988	-	
1	Delta IFSC	3.934	.28	2.243	-.29	1.749	-.41	uA
24	(I_O)	2.499	.13	1.713	-.36	1.552	-.28	
35		5.893*	.23	3.566	-.24	2.648	-.17	
47		4.739*	.11	2.862	-.33	1.956	-.14	
70		4.343*	.58	2.754	-.01	2.247	-.01	
1	Delta IFSC	3.964	.23	2.257	-.34	1.694	-.37	uA
24	($\bar{I}_O$)	2.544	.13	1.753	-.43	1.507	-.33	
35		5.901*	.23	3.543	-.28	2.707	-.18	
47		4.774*	.1	2.862	-.4	2.007	-.45	
70		4.233*	.53	2.689	-.04	2.347	-.12	
1	Error(Bit#1)	-45.11M	22M	-25.65M	4.5M	-14.12M	-6.0M	%
24	(I_O)	-22.97M	1.5M	-4.198M	-19.5M	15.88M	-35.5M	
35		11.56M	-32.5M	26.32M	-47M	35.94M	-58M	
47		-89.07M	70.5M	-49.95M	36.5M	-37.45M	22M	
70		-54.23M	34.5M	-32.45M	9.5M	-22.41M	9.5M	

TABLE 6-7. Comparison of GE/Signetics (cont'd.)

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	Error(Bit#1)	-55.70M	-	-36.30M	-	-26.34M	-	%
24	($\overline{I_O}$)	-4.526M	-	2.843M	-	19.55M	-	
35		12.84M	-	28.57M	-	37.77M	-	
47		-81.24M	-	-47.88M	-	-37.43M	-	
70		-51.47M	-	-27.52M	-	-15.64M	-	
1	Error(Bit#2)	-50.60M	36.5M	-45.77M	33M	-45.20M	33.5M	%
24	(I_O)	-30.95M	18M	-30.73M	18.5M	-30.92M	20.5M	
35		-18.98M	7M	-16.45M	2.5M	-14.67M	3.5M	
47		1.310M	-16.5M	-11.81M	-3.5M	-17.05M	5M	
70		10.54M	-22M	12.97M	-24.5M	11.78M	18M	
1	Error(Bit#2)	-60.08M	-	-53.21M	-	-52.17M	-	%
24	($\overline{I_O}$)	-36.22M	-	-30.64M	-	-31.05M	-	
35		-14.58M	-	-12.18M	-	-11.18M	-	
47		-18.50M	-	-19.06M	-	-21.20M	-	
70		13.11M	-	14.93M	-	15.61M	-	
1	Error(Bit#3)	23.29M	-34M	13.80M	-23M	6.927M	-15M	%
24	(I_O)	-1.601M	-7M	-5.421M	-2M	-9.693M	2.5M	
35		-16.12M	7.5M	-19.92M	11M	-22.07M	14M	
47		-20.66M	11.5M	-21.81M	11M	-22.72M	13.5M	
70		-2.980M	-5.5M	-10.05M	2.5M	-16.39M	11M	
1	Error(Bit#3)	24.87M	-	14.70M	-	6.362M	-	%
24	($\overline{I_O}$)	-7.693M	-	7.042M	-	-10.10M	-	
35		-15.72M	-	-18.77M	-	-20.78M	-	
47		-19.32M	-	-21.38M	-	-21.90M	-	
70		-2.009M	-	-8.437M	-	-13.51M	-	
1	Error(Bit#4)	15.09M	-23M	11.85M	-20.5M	10.64M	-16M	%
24	(I_O)	-13.42M	7M	-15.44M	8.5M	-18.56M	13M	
35		-25.93M	19.5M	-29.89M	23M	-32.57M	27M	
47		-4.106M	-3M	-7.308M	-1.5M	-8.174M	2M	
70		-9.262M	3M	-17.26M	11M	-22.50M	19M	

TABLE 6-7. Comparison of GE/Signetics

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	Error(Bit#4)	17.02M	-	13.88M	-	10.26M	-	%
24	($\overline{I}_O$)	-14.81M	-	-15.04M	-	-17.72M	-	
35		-25.50M	-	-29.32M	-	-31.20M	-	
47		7.048M	-	-1.782M	-	-5.243M	-	
70		-8.939M	-	-16.23M	-	-20.81M	-	
1	Error(Bit#5)	6.706M	-6M	3.631M	-3.5M	376.0u	-1.5M	%
24	(I_O)	30.00M	-29M	30.97M	-32M	32.17M	-31.5M	
35		12.52M	-12.5M	15.95M	-16M	16.04M	-16.5M	
47		7.166M	-5M	2.034M	-1M	-1.403M	1.5M	
70		5.594M	-3	967.8u	-1M	-1.671M	2.5M	
1	Error(Bit#5)	7.584M	-	4.070M	-	560.7u	-	%
24	($\overline{I}_O$)	30.18M	-	32.07M	-	31.56M	-	
35		13.55M	-	17.06M	-	17.92M	-	
47		5.146M	-	820.2u	-	-2.155M	-	
70		5.301M	-	1.583M	-	-197.9u	-	
1	Error(Bit#6)	-26.42M	27M	-30.52M	30.5M	-33.12M	32.5M	%
24	(I_O)	-8.926M	8.5M	-14.75M	15M	-17.48M	17.5M	
35		-18.21M	18M	-22.27M	22M	-25.33M	25.5M	
47		-14.34M	14.5M	-16.75M	18M	-18.51M	19M	
70		19.02M	-17M	14.52M	14M	11.03M	-18.5M	
1	Error(Bit#6)	-25.84M	-	-29.97M	-	-32.71M	-	%
24	($\overline{I}_O$)	-10.62M	-	-14.83M	-	-16.77M	-	
35		-17.65M	-	-21.58M	-	-24.35M	-	
47		-15.12M	-	-17.95M	-	-19.38M	-	
70		18.62M	-	15.02M	-	12.66M	-	
1	Error(Bit#2)	24.25M	-24M	24.12M	-24.5M	29.76M	-30M	%
24	(I_O)	-6.618M	7M	-10.71M	11M	-13.08M	12M	
35		1.277M	-1.5M	-2.103M	2.5M	-3.480M	1.5M	
47		35.51M	-35.5M	30.84M	-31M	33.10M	-33.5M	
70		-6.726M	7.5M	-7.276M	7M	-1.122M	-3.5M	

TABLE 6-7. Comparison of GE/Signetics

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	Error(Bit#7)	25.05M	-	23.79M	-	29.63M	-	%
24	($\overline{I_O}$)	-6.774M	-	-10.34M	-	-12.46M	-	
35		1.107M	-	-1.871M	-	-3.327M	-	
47		34.40M	-	31.50M	-	32.14M	-	
70		-6.798M	-	-7.184M	-	-395.2u	-	
1	Error(Bit#8)	4.940M	-4.5M	3.149M	-2.0M	3.772M	-4.5M	%
24	(I_O)	11.78M	-12M	5.205M	-5.0M	317.5u	-1.5M	
35		10.72M	-11M	5.103M	-5.0M	1.576M	-3.0M	
47		42.47M	-45M	35.76M	-36.5M	33.72M	-34.5M	
70		2.900M	-2.5M	-2.420M	2.0M	-2.095M	-1.0M	
1	Error(Bit#8)	20.65M	-	19.61M	-	19.60M	-	%
24	($\overline{I_O}$)	7.918M	-	827.3u	-	-4.487M	-	
35		1.831M	-	-3.987M	-	-7.569M	-	
47		44.72M	-	36.61M	-	33.24M	-	
70		-8.931M	-	-14.54	-	-14.55M	-	
1	Sum NL+	74.27M	90M	56.55M	71.5M	51.48M	675M	%
24	(I_O)	41.78M	43.5M	36.18M	56.5M	48.37M	67M	
35		36.08M	56M	47.37M	65.5M	53.55M	73.5M	
47		86.45M	99.5M	68.63M	69M	66.82M	70.5M	
70		38.06M	49M	28.45M	38.5M	22.81M	40M	
1	Sum NL+	95.18M	-	76.05M	-	66.42M	-	%
24	($\overline{I_O}$)	38.10M	-	35.74M	-	51.12M	-	
35		29.32M	-	45.63M	-	55.69M	-	
47		91.31M	-	68.94M	-	65.38M	-	
70		37.03M	-	31.53M	-	28.27M	-	
1	Sum NL-	-122.1M	-89M	-101.9M	-72M	-92.43M	-67M	%
24	(I_O)	-84.48M	-46.5M	-81.24M	-55.5M	-89.73M	-66M	
35		-79.24M	-53.5M	-90.63M	-65.5M	-98.12M	-75M	
47		-128.2M	-101.5M	-107.6M	-69.5M	-105.3M	-68.5M	
70		-73.20M	-47M	-69.45M	36.5M	-66.19M	-39.5M	

TABLE 6-7. Comparison of GE/Signetics

Data on 5 industry samples

S/N	Parameter	T_A = -55°C GEOS	T_A = -55°C Sig	T_A = +25°C GEOS	T_A = +25°C Sig	T_A = +125°C GEOS	T_A = +125°C Sig	Unit
1	Sum NL-		-		-		-	%
24	($\overline{I_O}$)		-		-		-	
35								
47								
70								
1	Sum NL	-.048	.001	-.045	-.0005	-.041	.0005	%
24	(I_O)	-	.002	-	.001	-	.001	
35		-.043	.0025	-.043	.000	-.045	.0015	
47		-.042	-.002	-.039	-.0005	-.039	.002	
70		-.035	+.0002	-.041	+.002	-.043	.0005	
1	Sum NL		-		-		-	
24	($\overline{I_O}$)		-		-		-	
35								
47								
70								
1	NL+(I_O)		-		-		-	
24								
35								
47								
70								
1	NL+($\overline{I_O}$)		-		-		-	
24								
35								
47								
70								
1	NL-(I_O)		-		-		-	
24								
35								
47								
70								

TABLE 6-7. Comparison of GEOS/Signetics Dynamic Data

Settling Time

	t_{SLH} (nsec)		t_{SHL} (nsec)	
S/N	GEOS	Signetics	GEOS	Signetics
76	100	86.8	110	83.2
30	107	122.8	110	83.2
63	110	86.8	106	90.4
66	104	86.8	104	79.6
68	104	76.0	107	90.4

Propagation Delay

	t_{PLH} (nsec)		t_{PHL} (nsec)	
S/N	GEOS	Signetics	GEOS	Signetics
1	35	31	44	15
24	41	32	42	14
35	50	43	56	36
47	33	29	42	5
70	34	33	41	13

Reference Amplifier Slew Rate

	Δt_{ON} (L - H) (nsec)		Δt_{OFF} (H - L) (nsec)	
S/N	GEOS (bits high)	Signetics	GEOS	Signetics
1	236	127	260	68
24	300	223	305	119
35	500	362	500	185
47	230	125	225	73
70	335	202	350	98

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