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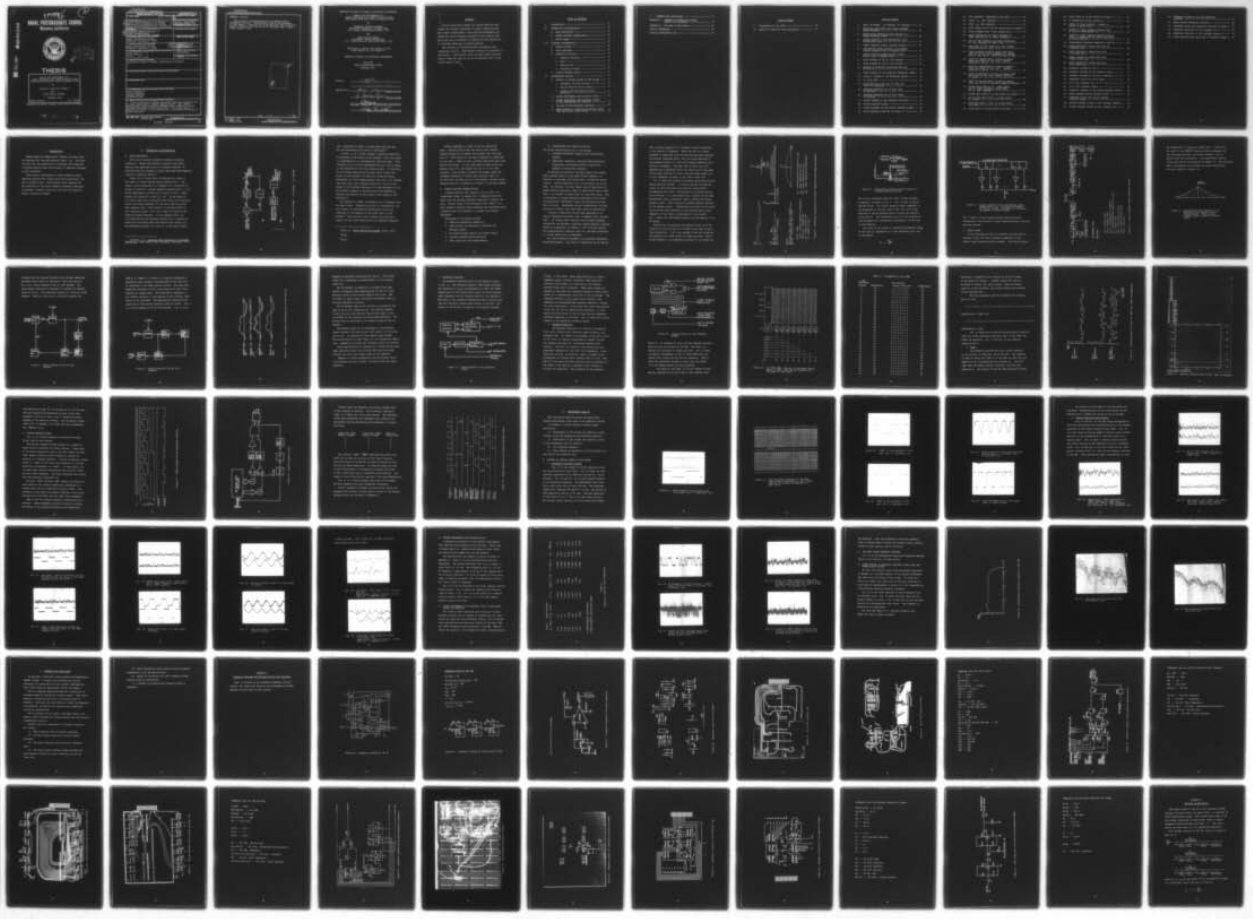

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THESIS

DESIGN AND PERFORMANCE OF A
SPREAD SPECTRUM DATA COMMUNICATIONS SYSTEM
USING DELTA MODULATION WITH A DITHERED CLOCK

by

Evangelos Vassilios Pappas

and

James Harvey Hoffman

December 1978

Thesis Advisor: G.A. Myers

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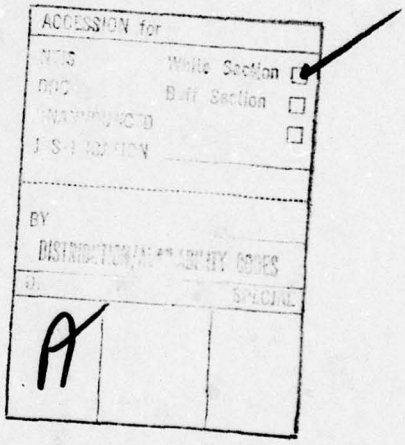
The circuitry incorporates small and medium scale integrated circuits. Experimental results are presented in some detail. Good quality voice and music were recovered using a fixed bit rate as low as 10 kbits/sec and a clock dither range of 40%.



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Design and Performance of a Spread Spectrum Data Communications System Using Delta Modulation with a Dithered Clock

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ABSTRACT

Digital modulation schemes and spread spectrum techniques are of major importance in modern communications. This thesis investigates a delta modulation/demodulation scheme and direct sequence spreading of the digital data. The clock rate is dithered to enhance the low probability of intercept advantage of spread spectrum.

The circuitry incorporates small and medium scale integrated circuits. Experimental results are presented in some detail. Good quality voice and music were recovered using a fixed bit rate as low as 10 kbits/sec and a clock dither range of 40%.

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TABLES OF SYMBOLS AND ABBREVIATIONS

AJ	-	anti jam
LPI	-	low probability of intercept
ΔM	-	delta modulation
x(t)	-	band limited analog input to delta modulator
L(t)	-	binary pulses from delta modulator
τ	-	pulse width
T	-	period
e(t)	-	error waveform
y(t)	-	delta modulator integrator output
$\pm V$	-	delta modulator step size
SS	-	spread spectrum
DS	-	direct sequence
PN	-	pseudo-noise
RF	-	radio frequency
PRM	-	phase reversal modulation
FSK	-	frequency shift keying
FSR	-	feedback shift register
L	-	length of maximal length sequence
n	-	number of shift register stages
ACF	-	autocorrelation function
CCF	-	cross correlation function
MF	-	matched filter
BW_{RF}	-	transmitted bandwidth
PG	-	processing gain

R	-	information rate
PROM	-	programmable read only memory
ROM	-	read only memory
VCO	-	voltage controlled oscillator
IC	-	integrated circuit
TTL	-	transistor transistor logic
CVSD	-	continuously variable slope delta modulator
$\hat{x}(t)$	-	an approximation to x(t)
LPF	-	low pass filter
d(t)	-	digital data
BJT	-	bipolar junction transistor
S_o	-	"ZERO" sequence
S_1	-	"ONE" sequence
V_{ref}	-	voltage comparator reference voltage
DMF	-	digital matched filter
S/N, SNR	-	signal to noise ratio
V_s	-	signal voltage RMS
V_N	-	noise voltage RMS
PC	-	printed circuit

I. INTRODUCTION

Spread spectrum communication systems are being used and designed for many applications [Refs. 1-4]. The anti-jam (AJ) and low probability of intercept (LPI) features of spread spectrum make the military an important developer of this technique.

This project investigates a direct sequence spread spectrum communication system using delta modulation (ΔM) and a dithered clock. The dithered clock enhances the LPI qualities of the direct sequence spreading technique. ΔM provides a simple, relatively low data rate analog to digital conversion scheme.

II. THEORETICAL CONSIDERATIONS

A. DELTA MODULATION

ΔM is one of several methods of analog to digital conversion. Rather than sending a digital code representing some amplitude value of a sampled waveform, ΔM functions describe changes in signal amplitude from sampling instant to sampling instant.[1]

Linear ΔM in a basic form is described by figure 1. The input is a band limited analog waveform x(t). The output of this modulator is a waveform L(t) consisting of pulses of duration τ seconds spaced T seconds apart ($\tau \leq T$) having amplitude of either plus or minus V volts. These pulses are clocked at a rate $F_c = 1/T$. If the slope of the input signal x(t) is positive then while this condition exists the output waveform L(t) has more positive pulses than negative ones. The situation is reversed when x(t) has a negative slope. For a D.C. input the positive and negative pulses alternate. In the feedback path, L(t) is integrated and the resulting waveform y(t) consists of steps which oscillate about the analog input signal x(t). The difference between x(t) and y(t) is the error signal

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[1]Silahaki, R.M., Adaptive Delta Modulation in Hardware Realization, MSEE Thesis, NPGS, Monterey, Californai, 1977.

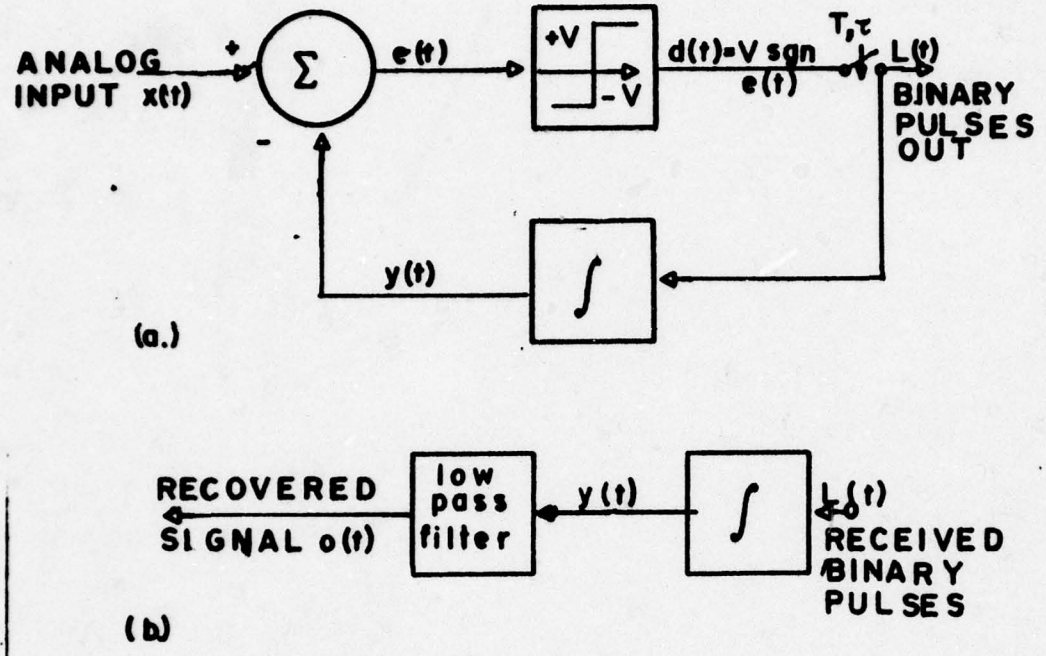

Figure 1. Basic ΔM scheme: (a) encoder, (b) decoder

e(t), quantized to limits ±V which means the sign and not the magnitude of the error is quantized.[2]

If $e(t) \geq 0$ at a clock instant, a positive pulse will be produced at the output of the encoder. When this pulse is integrated y(t) is increased by a positive step. This increase in y(t) will be subtracted from x(t) and a change in the magnitude of the error signal occurs. If the error has not become negative by the next clock instant the output of the encoder will again be a positive pulse. Eventually y(t) will become greater than x(t); e(t) becomes less than zero, and a negative pulse will occur at the output of the encoder resulting in a step decrease in y(t). The encoder attempts to minimize the error waveform by varying the polarity of the pulses at the output of the modulator.[3]

The decoder in linear ΔM consists of an integrator and low pass filter. Assuming no errors in transmission, the L(t) signal is recovered and integrated to give y(t), identical to the feedback to the error point in the encoder.[4] The low pass filter removes the step-like quality of y(t) that results from the sampling frequency.

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[2]Steel, R., Delta Modulation Systems, Wiley, 1975.

[3]Steel,

[4]Steel,

Several problems in linear ΔM can be identified. Slope overload occurs when the analog input changes between samples by an amount much greater than the step size ±V. This occurs if the input frequency or amplitude is too great. There is also a minimum amplitude input that the ΔM can follow. If the input peak to peak values are smaller than $|\pm V|$, the output will be as if x(t) were constant. Many methods to expand the dynamic range and frequency response of ΔM have been explored [Ref. 9]. In this work, we make use of a continuously variable slope algorithm which is considered in detail in the next chapter.

B. SPREAD SPECTRUM COMMUNICATIONS

A spread spectrum (SS) system is one in which the transmitted signal is spread over a frequency band much wider than the minimum bandwidth required to transmit the data. Various types of SS techniques exist [Refs. 1-4]. This research involves direct sequence (DS) spreading using a pseudo-noise (PN) sequence to increase the system's bandwidth.

Advantages of SS systems include

1) Selective addressing capability
2) Code division multiplexing is possible for multiple access
3) Low density power spectra for signal hiding
4) Inherent message privacy/security
5) High resolution range measurements

6) Interference and jamming rejection.

Two prime disadvantages exist in SS systems.

1) Increased bandwidth compared with conventional systems

2) Additional complexity including code generators, correlators and synchronization circuits not needed in conventional systems.

DS systems are presently the most popular SS systems. These systems employ a high speed binary sequence, in addition to the basic data being sent, to modulate the RF carrier. Carrier modulation can, in principle, be of any form. In practice, the most common type of modulation is phase-reversal modulation (PRM) or phase-shift keying (FSK) with $\pm \pi/2$ radians of phase shift for each data pulse. PRM is equivalent to double-sideband suppressed carrier amplitude modulation (AM-DSB/SC) where the modulating voltage has two levels. Suppressed carrier transmissions are more difficult to detect than some other forms of modulations.

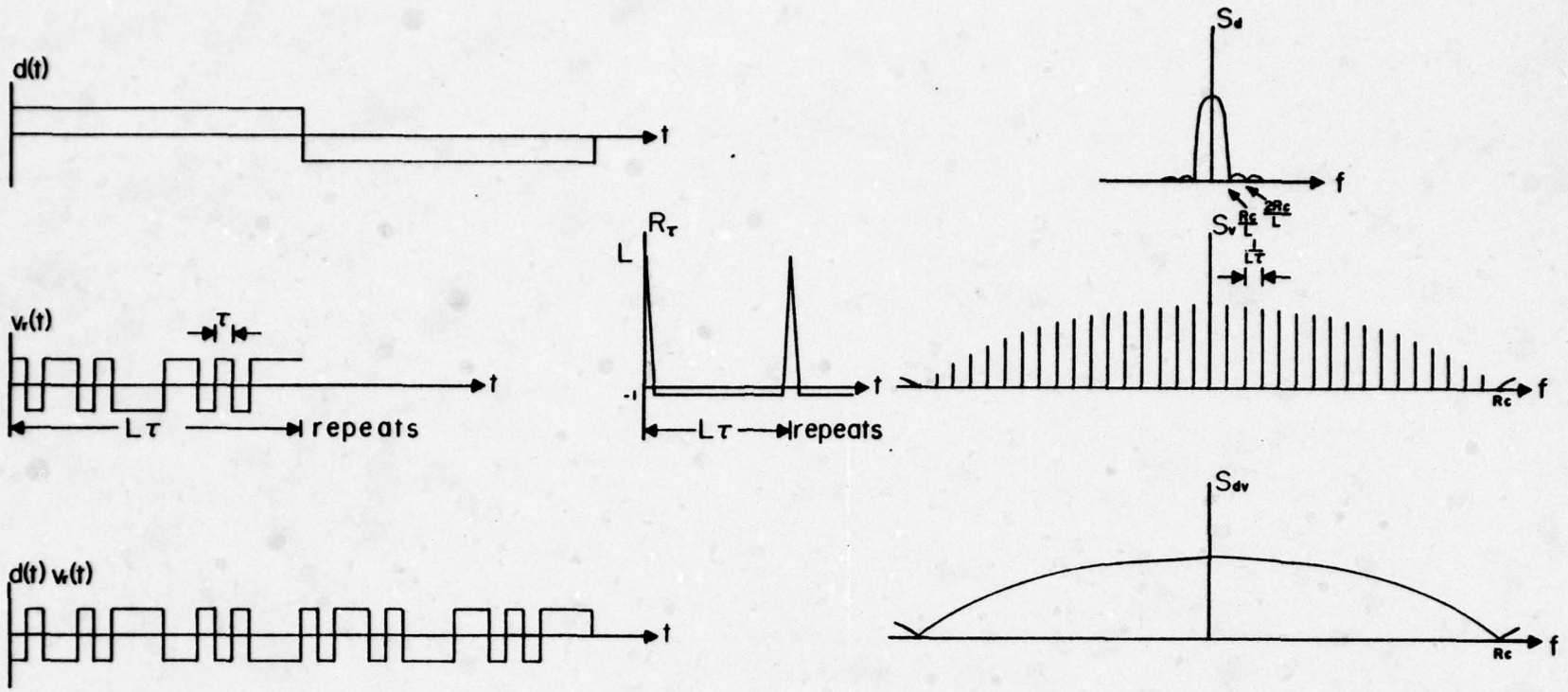
A method of generating binary code sequences to be used as spreading functions, uses a feedback shift register (FSR). An n-stage shift register with suitable feedback connections can generate a periodic binary sequence (maximal-length or m-sequence) of length $L = 2^n-1$ bits per period. The autocorrelation function (ACF) of a periodic m-sequence is a sharp spike with no sidelobes.

The radio frequency bandwidth in DS systems determines system performance. The result of modulating an RF carrier

with a direct sequence is to produce a signal translated to the carrier's frequency. Since the ACF of a direct sequence is known and since the ACF and the power spectrum are Fourier transform pairs, then the power spectrum of the produced signal is a $(\sin x/x)^2$ shape centered at the carrier's frequency. The main lobe of this $(\sin x/x)^2$ spectrum has a bandwidth twice the clock rate of the modulating code, from null to null, and side lobes whose null to null bandwidth is equal to the code's clock rate.

Fig. 2 shows the different waveforms associated with DS spread spectrum systems. In the SS receiver the desired signal is received along with additive uncorrelated interference and noise. This mixture of received signals is correlated, i.e., multiplied with a replica of the same pseudorandom code (m-sequence) used to spread the wanted message signal. This correlation process permits recovery of the message signal. Interference and noise do not correlate with the code generated in the receiver and so this component of the input is suppressed in the receiver. Fig. 3 shows the relationship between various spectra in an SS system.

Another way of obtaining the desired signal in an SS receiver is with the use of a matched filter (MF) to provide correlation. A MF is an optimum filter for detecting the presence of a known signal in additive noise. Thus a filter matched to an m-sequence provides at its output the



d(t): data

$v_r(t)$: direct sequence (m-sequence)

$d(t)v_r(t)$: spread data

R_c: code's clock rate

L: length of code

R_τ: autocorrelation function of $v_v(t)$

S_d: power spectrum of d(t)

S_v: power spectrum of $v_r(t)$

S_{dv}: power spectrum of spread data

Figure 2. Waveforms associated with direct sequence spread spectrum systems

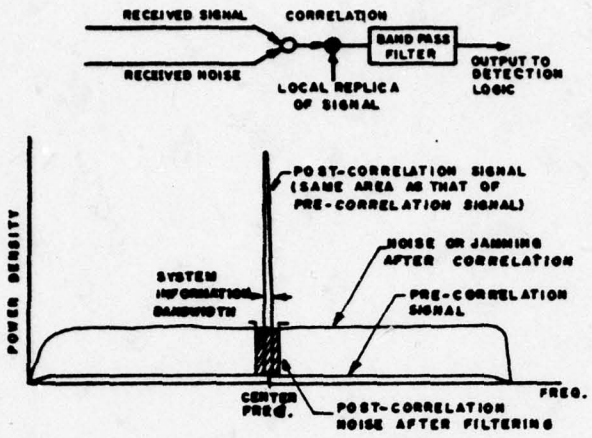


Figure 3. Relationship between various spectra in a spread spectrum system.

ACF of this m-sequence when the input is that periodic m-sequence, as shown in Fig. 2. Fig. 4 shows a digital matched filter. All direct sequence signal bandwidth is the bandwidth of the main lobe of the $(\sin x/x)^2$ power spectrum of the DS waveform which is twice the system's clock rate R_c. The information rate R is the minimum bit rate necessary for satisfactory reproduction of the data at the receiver.

The ratio of the spread or transmitted bandwidth (BW_{RF}) to the rate of information R is the processing gain (PG) of the system.

$$PG = \frac{BW_{RF}}{R}$$

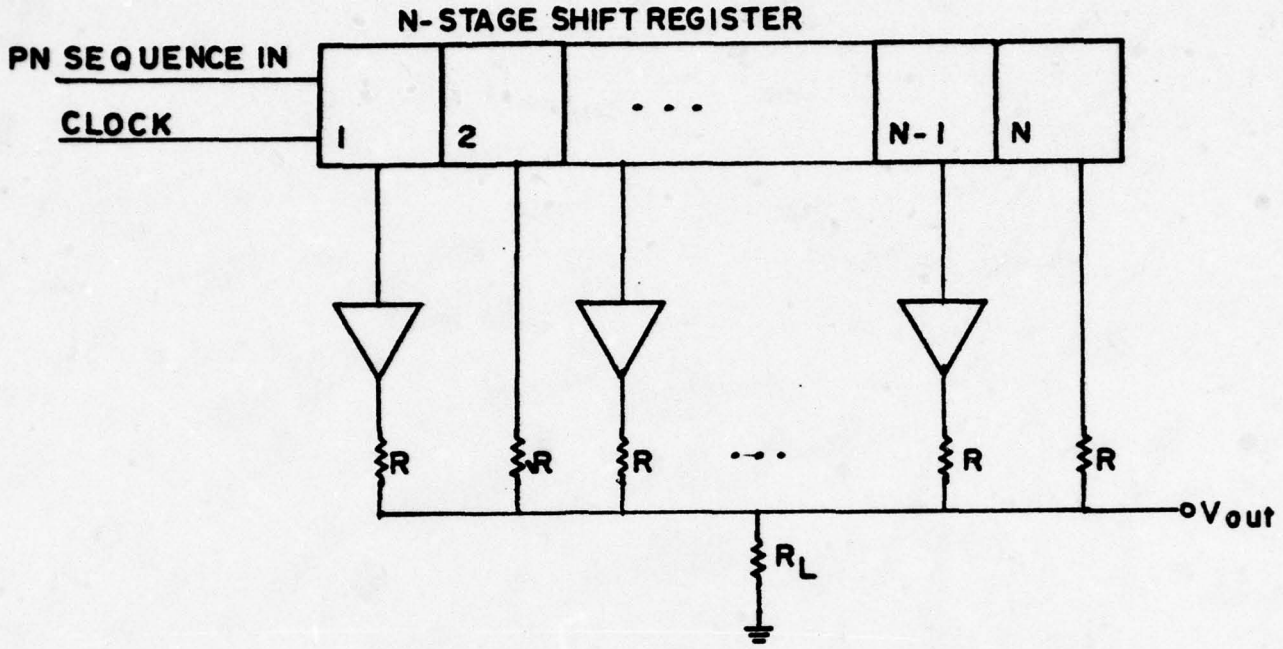
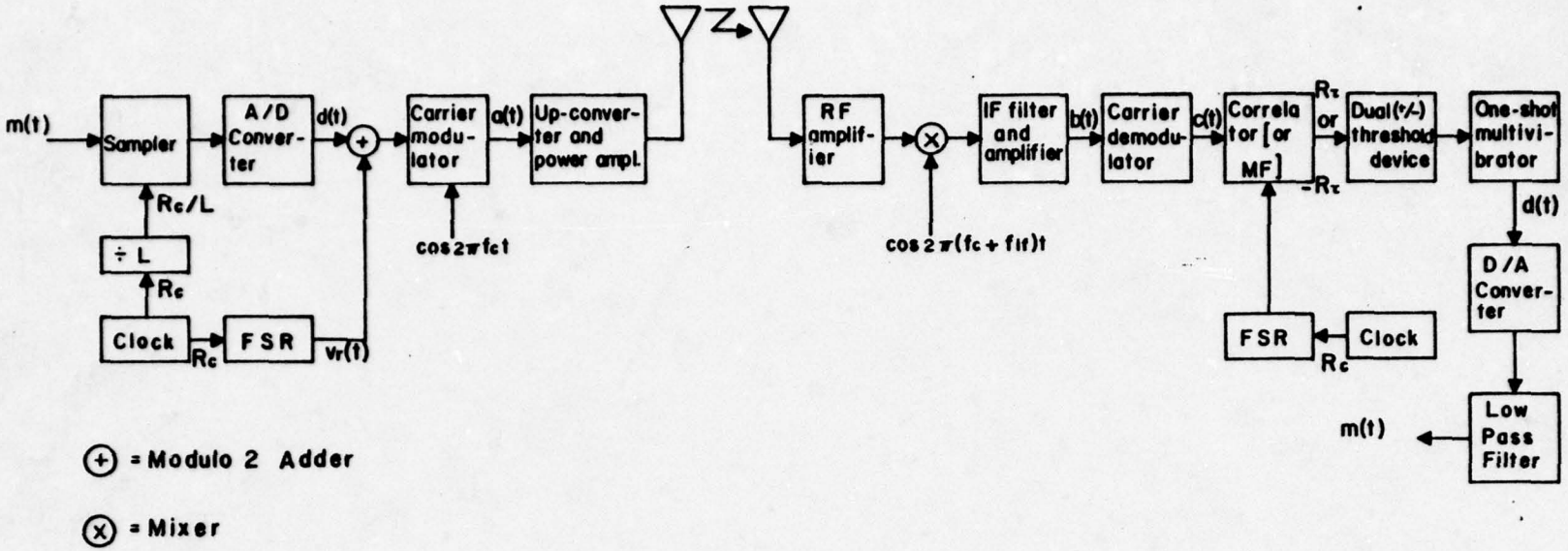


Figure 4. Digital matched filter realization using tapped delay line. Inverters correspond to "zeros" stored, the absence of inverters correspond to "ones" stored.

Fig. 5 shows a direct sequence spread spectrum system. Transmitter's and receiver's clocks synchronization circuitry has been omitted.

C. CLOCK DITHER

It was hypothesized that by dithering the data and PN sequence clocks the clock frequency components in the spread signal spectrum would be masked. This should reduce



$m(t)$ = analog input

$d(t)$ = digital data

$v_r(t)$ = m-sequence of length L

R_τ = autocorrelation function of $v_r(t)$

R_c = clock rate

$a(t) = d(t)v_r(t)\cos 2\pi f_c t$

$b(t) = d(t)v_r(t)\cos 2\pi f_{IF} t$

$c(t) = d(t)v_r(t)$

Figure 5. Direct sequence spread spectrum system

the probability of intercept (enhace LPI). Intuitively the nulls in the $(\frac{\sin x}{x})^2$ spectrum should disappear and the side lobes and main lobe blend together. Fig. 6 demonstrates this hypothesis. The experimental results verify this notion as discussed in Chapter IV. The circuitry used to accomplish clock dither and system performance are also treated in Chapter IV.

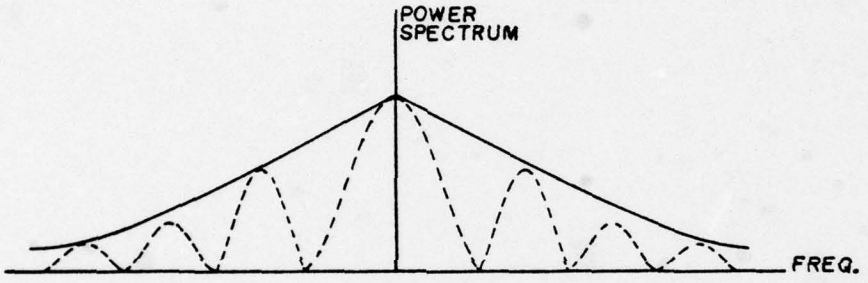


Figure 6. Hypothesized power spectra of the spread digital sequence with a dithered clock. Power spectra without dither is shown in dotted lines.

III. HARDWARE IMPLEMENTATION

A. OVERALL SYSTEM

Figure 7 is a block diagram of the entire spread spectrum system design. On the transmitter side a ΔM, through logic circuitry, enables one of two 32 bit spreading sequences from a read only memory (ROM). A voltage controlled oscillator (VCO) dithered by a modulating voltage drives the PN sequence output by the ROM. A divide-by-32 counter network clocks the ΔM. On the receiver side, a 32 stage digital matched filter consisting of cascaded serial-in-parallel-out shift registers correlates the two input sequences. The summed output of the shift registers is applied to a threshold detector, appropriate logic, and a D-flip flop. The flip flop output is applied to a ΔM decoder, and the decoded analog output is filtered and amplified to drive a speaker. For the purposes of this project the receiver and transmitter are connected to the same clock.

B. DELTA MODULATOR

The ΔM used in this project consists of an integrated circuit (IC), the Motorola XC 3418 Codec (encoder-decoder). The single IC combines the encoder and decoder functions. Rather than providing bipolar pulses, the output of this IC is a plus voltage for data "ONE" and ground for data "ZERO", which is compatible with TTL integrated circuits.

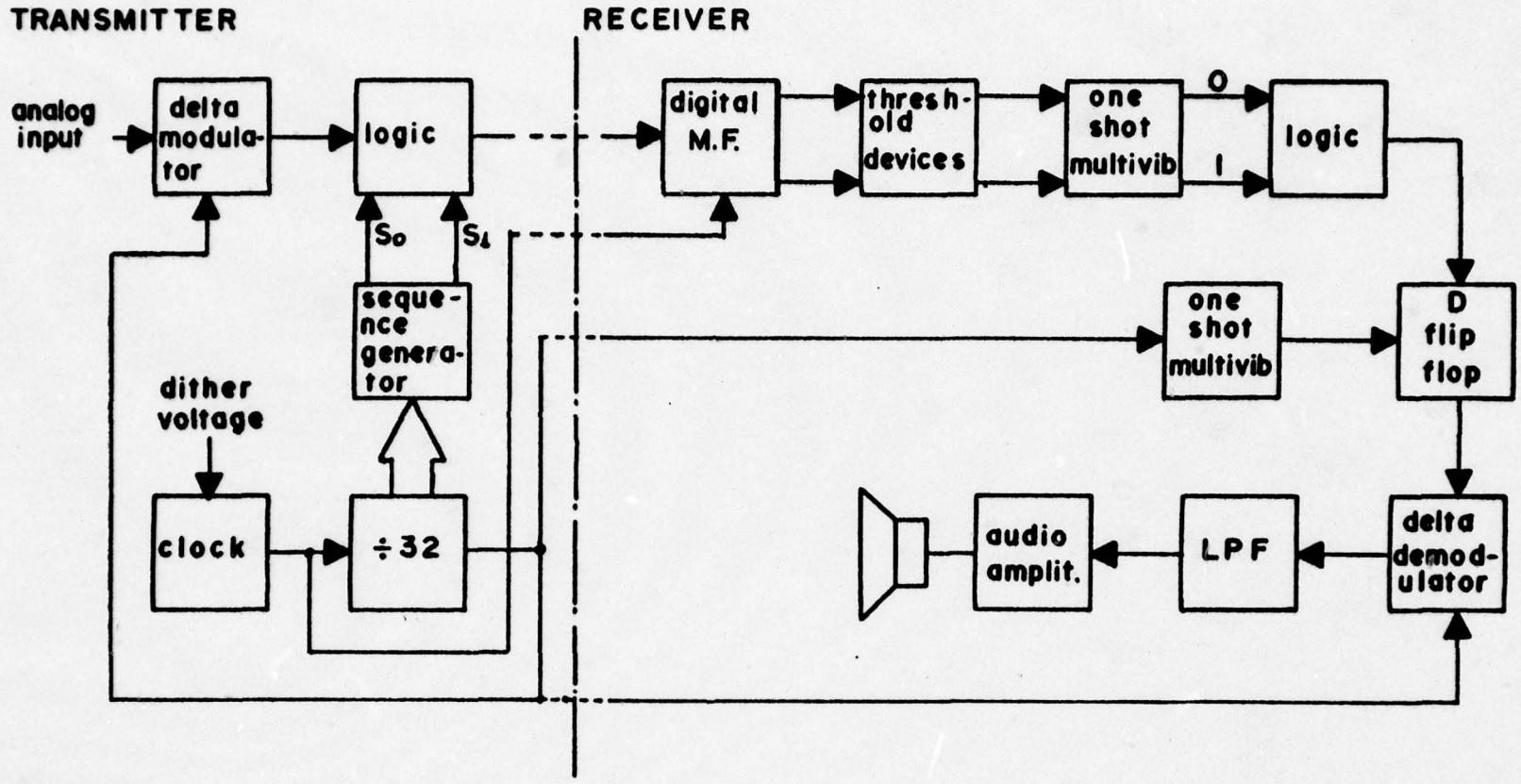


Figure 7. Spread spectrum communications system with ΔM and a dithered clock

A sample and hold network following the voltage comparator provides output pulses of duration T (the clock period). Fig. 8 is a block diagram of the XC 3418 encoder. The level detect algorithm is designed to increase the dynamic range of the IC. The algorithm consists of a four-bit shift register. When all four bits in the shift register are

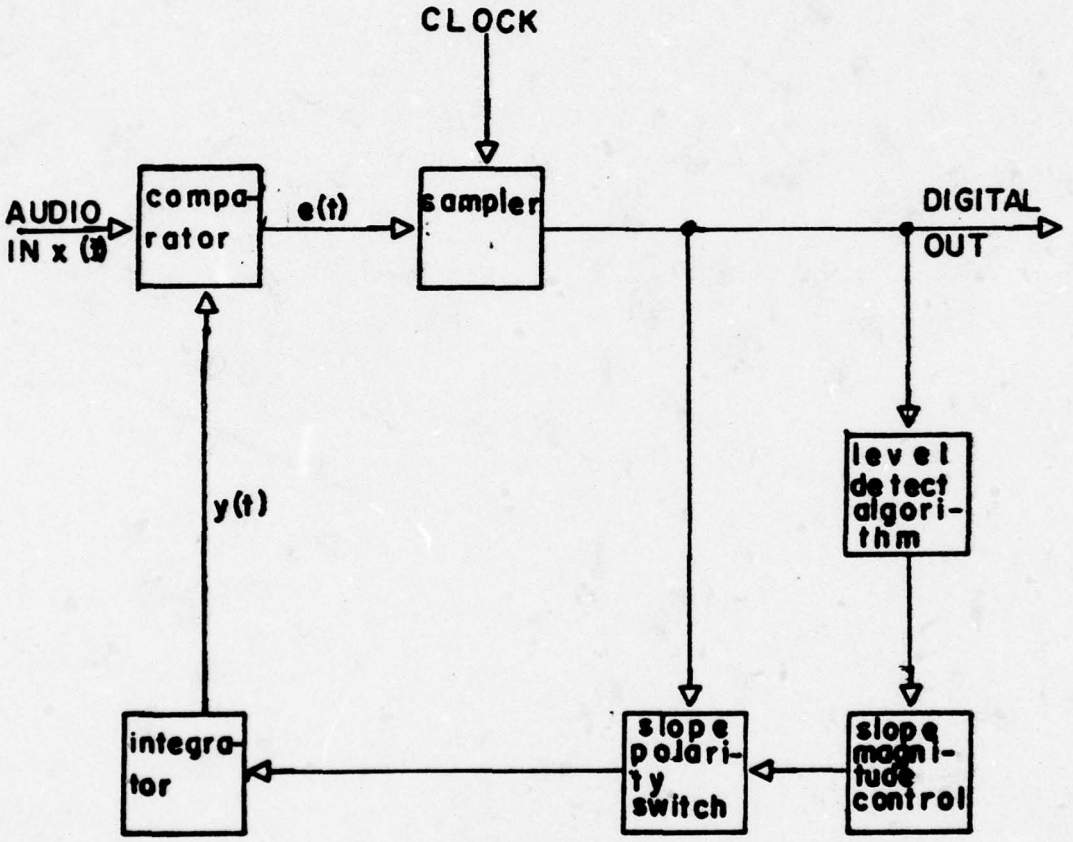


Figure 8. Block diagram of the XC 3418 encoder.

"ONE's" or "ZERO's", a result of a rapidly increasing or decreasing input voltage, the magnitude of the step size is increased at the slope polarity switch. The step size magnitude increases at each clock pulse until this "coincidence" no longer holds. The algorithm is repeated in the decoder allowing a close replica of the original input signal to be recovered. The manufacturer describes this algorithm as continuously variable slope ΔM (CVSD). Fig. 9 is a block diagram of the XC 3418 decoder. Fig. 10 is an

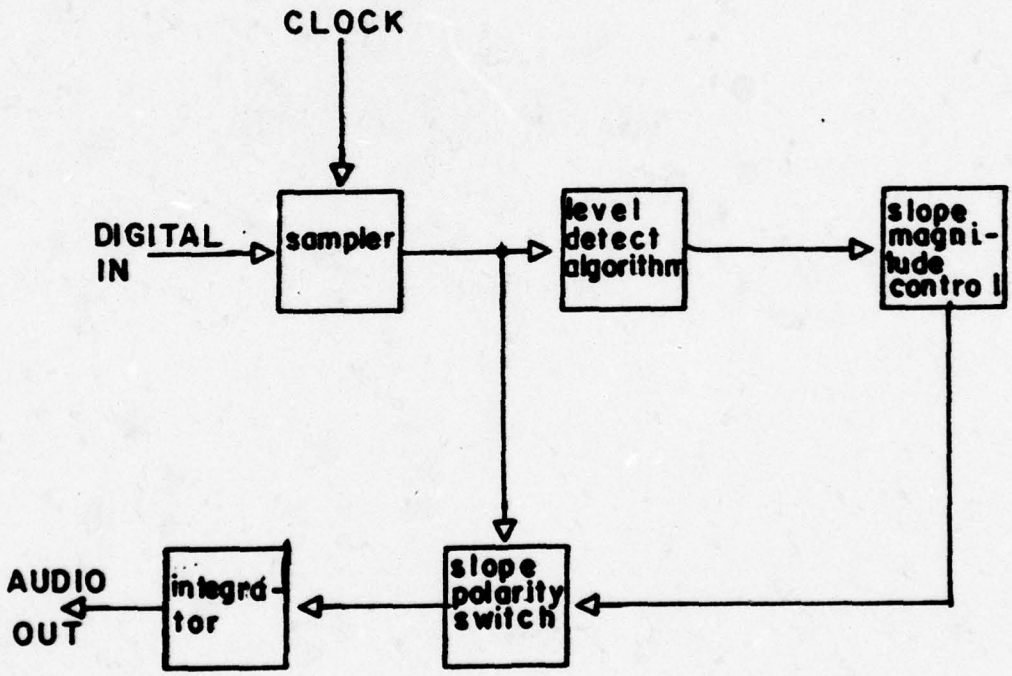


Figure 9. Block diagram of the XC 3418 decoder.

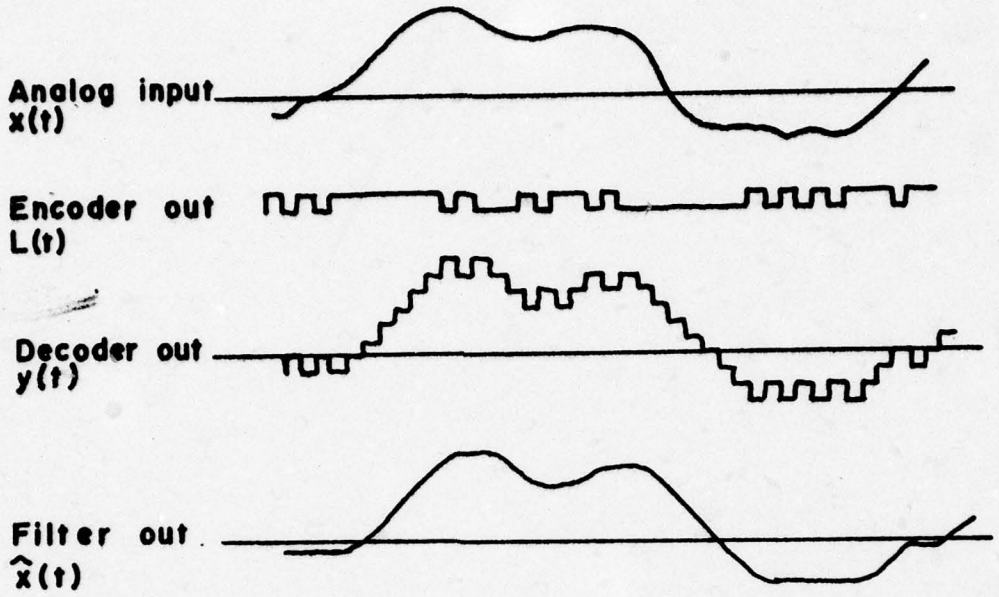


Figure 10. Example of waveform associated with the XC 3418 ΔM

example of waveforms associated with the IC. The filter output $\hat{x}(t)$ represents an approximation to the original input $x(t)$.

The ΔM encoder is clocked by a dithered clock that varies in frequency from approximately 20 kHz to 24 kHz. New data occurs on the falling edge of the clock. The ΔM output is used to gate the proper PN sequence code in the data spreading circuitry.

The ΔM decoder used in the receiver is clocked by the same clock as the transmitter ΔM. The digital matched filter circuitry provides the digital data input to the ΔM decoder at the required +5V and ground potentials. The digital data is converted to an analog voltage by the ΔM decoder.

The analog output of the ΔM decoder in the receiver passes through a low pass filter (LPF) which is a six-pole active LPF. It consists of three second order stages. The active device for each stage is a 741 operational amplifier. Appendix B provides the transfer function of the LPF.

Audio amplification is achieved by a single LM 380 audio power amplifier which also provides the tone and volume controls for this last output stage of the receiver.

Appendix A contains schematics and the printed circuit foil patterns for the ΔM codec, low pass filter and audio amplifier.

C. SPREADING CIRCUITRY

The bandwidth spreading part of the system is shown in Fig. 11. The sequence generator continuously produces the sequences S_1 and S_o corresponding to "ONE" and "ZERO" respectively of the digital data output of the ΔM encoder. These sequences and the incoming data d(t) are applied to AND gates in the sequence distributing logic circuitry and then the resulting outputs pass through an OR gate. The output of the OR gate is applied to the digital matched

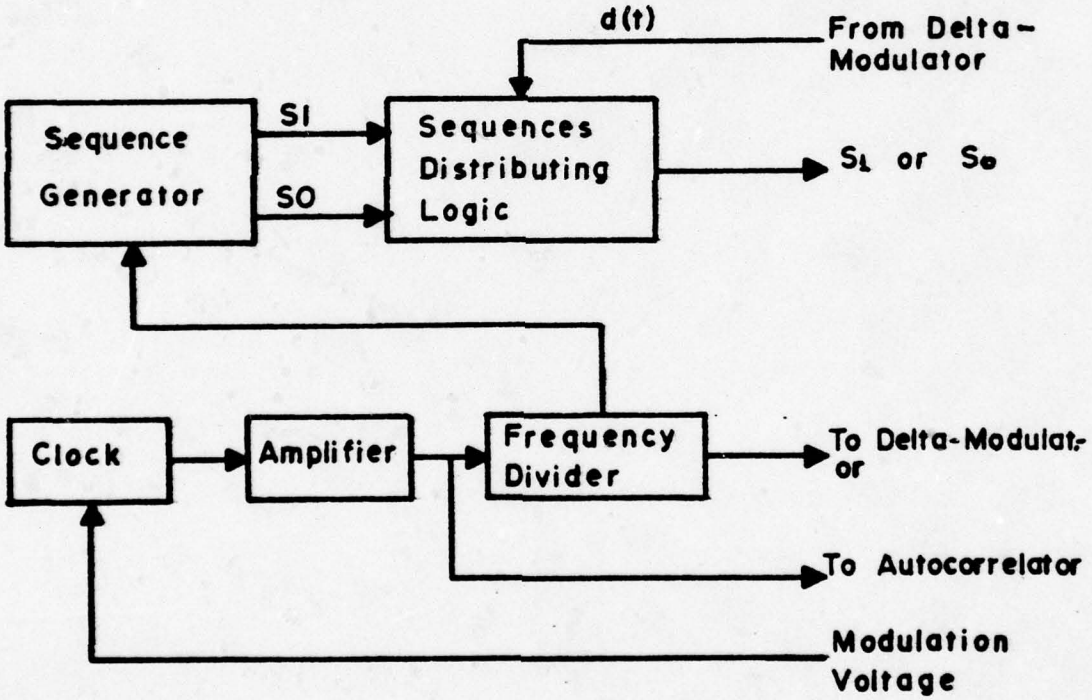


Figure 11. Block diagram of the spreading system.

filter. A VCO output, after amplification by a single feedback bipolar junction transistor (BJT) amplifier provides clock pulses at a high rate to the digital matched filter shift registers. These clock pulses are applied to the modulo-32 frequency divider to obtain clock pulses of a comparatively slow rate to the ΔM encoder. The frequency divider, a five stage binary counter, also addresses the programmable ROM sequence generator, through its five output ports. During each slow clock pulse period to the ΔM, the 32-bit sequences are generated. In this manner synchronization of the ΔM codec and the bandwidth spreading sequences is achieved. Fig. 12 shows the circuit diagram of the bandwidth spreading system.

1. Sequence Generator

The sequence generator is a 256-bit (32 words by eight bits) fusible-link, Schottky, open-collector, programmable ROM. Its memory is programmed to provide on each of the first six outputs m-sequences of length 31 which are normally produced by a five-stage feedback shift register. The last two outputs of the ROM provide the complement sequences of the first two m-sequences. Since there are 32 words, an extra bit (zero) is added to the m-sequences to increase their lengths from 31 to 32. The ROM is of the open-collector type and pull-up resistors of the order of 500 Ohms are connected to the outputs to retrieve the sequences. The spreading of the incoming

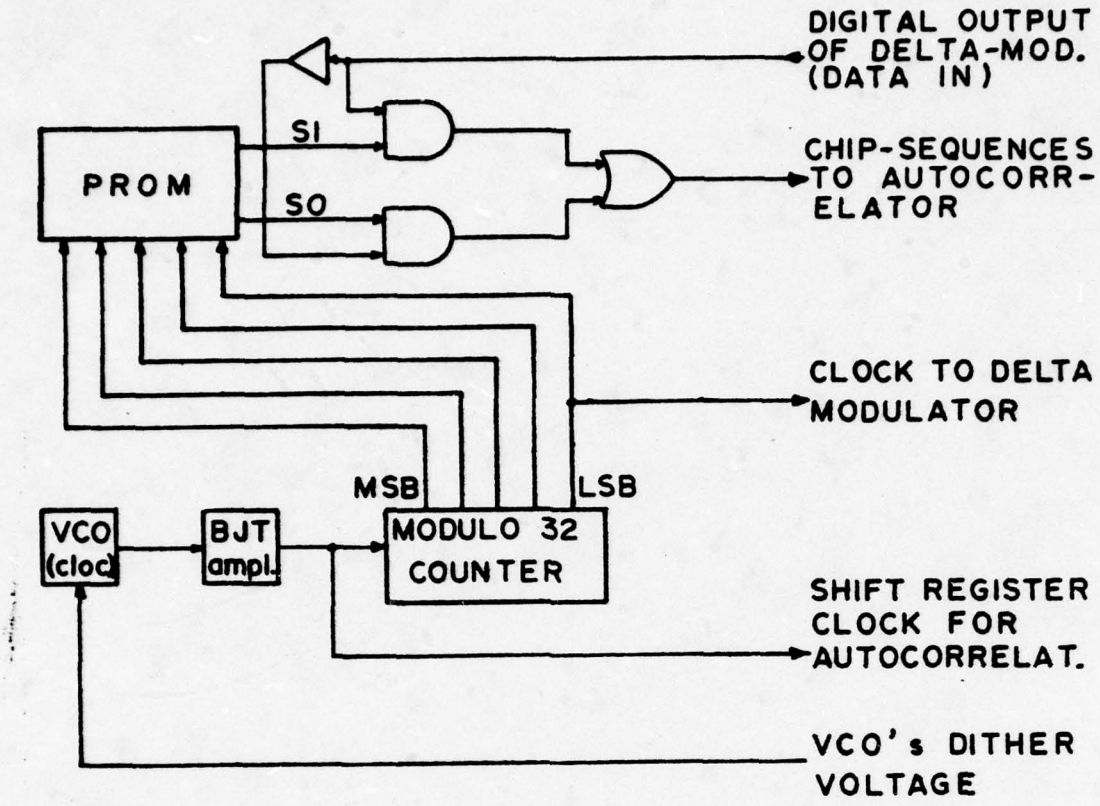


Figure 12. Circuit diagram of the spreading system.

data d(t), is achieved by using the chip sequence emerging from the last two outputs of the ROM. The other six outputs are available to change the code. Fig. 13 shows the general arrangement of the TI 74188 PROM used, the stored logic levels and the pull-up resistors. Table I shows the procedure followed to store into the PROM's 32 x 8 bit memory matrix the chip sequences.

The words at the eight (01 to 08) outputs of the ROM are selected by the five (ADA to ADE) address lines

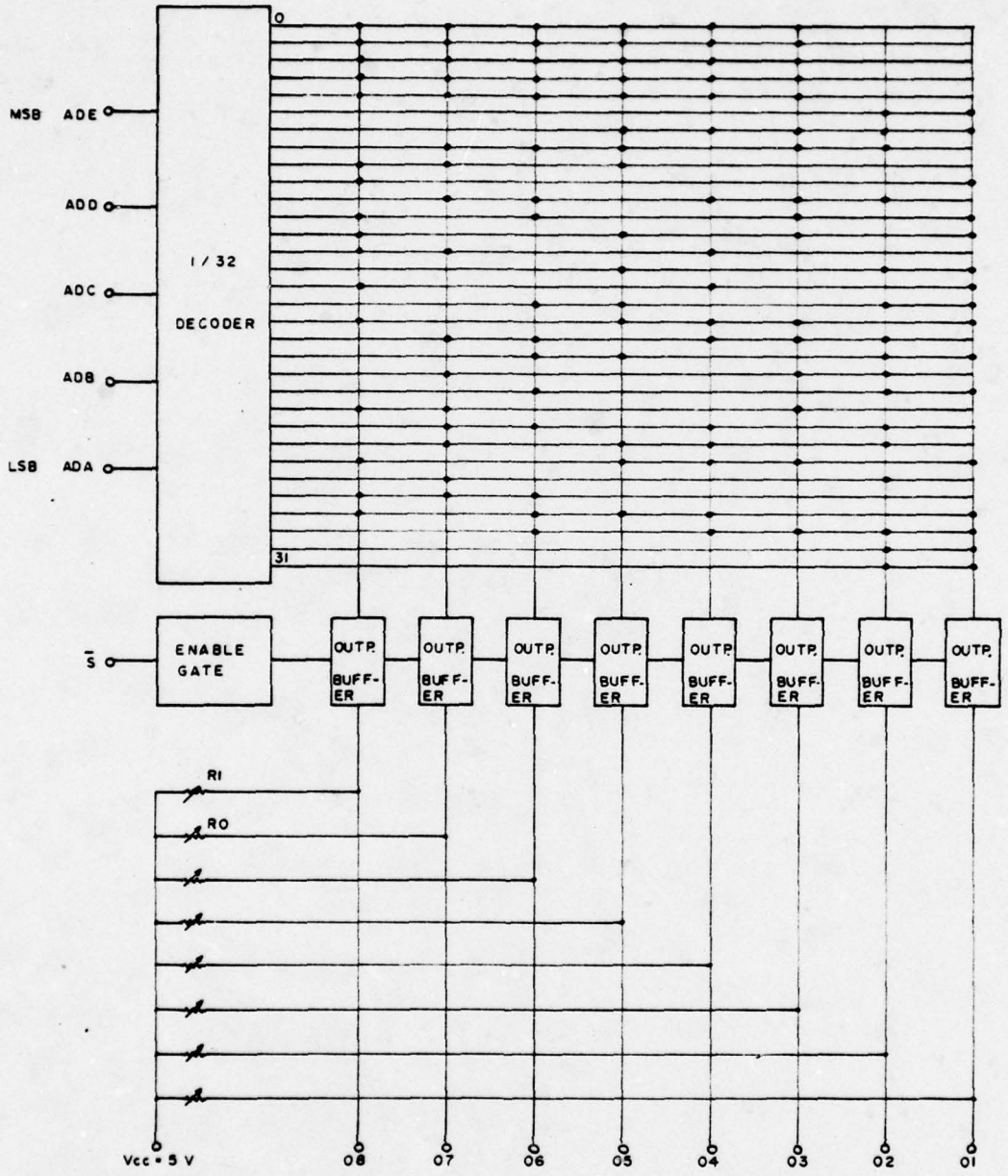


Figure 13. TI 74188 PROM. The dot in the memory matrix means a "high" level and the absence of a dot means a "low" level.

Table I: Programming of the PROM

Row Addressed		Data Stored	
Decimal	Hexadecimal	Binary (high,low)	Hexadecimal
0	00	1 1 1 1 1 1 0 0	FC
1	01	1 1 1 1 1 1 0 0	FC
2	02	1 1 1 1 1 1 0 0	FC
3	03	1 1 1 1 1 1 0 0	FC
4	04	1 1 1 1 1 1 0 0	FC
5	05	0 0 0 0 0 0 1 1	OB
6	06	0 0 0 1 1 1 1 1	1F
7	07	0 1 1 1 0 1 1 0	7G
8	08	1 1 0 1 0 0 0 0	DO
9	09	1 0 0 0 0 0 0 1	81
10	OA	0 1 1 0 1 1 1 0	6E
11	OB	1 0 1 0 0 1 0 1	A5
12	OC	1 0 0 1 0 1 0 1	95
13	OD	1 1 0 0 1 0 0 0	C8
14	OE	0 0 0 1 0 0 1 1	13
15	OF	1 0 0 0 1 0 0 1	89
16	10	0 0 1 1 0 0 1 1	33
17	11	1 0 0 1 1 1 0 1	9D
18	12	0 1 1 0 1 1 1 0	6E
19	13	0 0 1 1 0 0 1 1	33
20	14	0 1 0 0 0 1 1 0	46
21	15	0 0 1 0 0 0 1 1	23
22	16	1 1 0 0 0 1 0 0	C4
23	17	0 1 1 0 1 0 1 0	6A
24	18	0 1 0 1 1 0 1 0	5A
25	19	1 0 0 1 1 1 0 1	9D
26	1A	0 1 0 0 0 0 1 0	42
27	1B	1 1 1 0 0 0 0 0	EO
28	1C	1 0 1 1 1 0 0 1	B9
29	1D	0 0 1 0 1 1 1 1	2F
30	1E	0 0 0 0 0 0 1 1	03
31	1F	0 0 0 0 0 0 1 1	03

activated in sequence by the outputs of the five stages of the modulo 32 counter. A memory enable ($\overline{S}$) input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

The chip sequences used for spreading the incoming data d(t) are:

1 1 1 1 1 0 0 1 1 0 1 0 0 1 0 0 0 0 1 0 1 0 1 1 1 0 1 1 0 0 0 0

representing a "ZERO" and

1 1 1 1 1 0 0 0 1 1 0 1 1 1 0 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0 0 0

representing a "ONE".

Fig. 14 shows the calculated autocorrelation functions (ACF) and cross-correlation function (CCF) of the "ONE" and "ZERO" PN sequences. Fig. 15 and Fig. 16 are computer generated ACF's.

2. Logic

The sequence distributing logic circuit consists of an inverter, an AND gate, and an OR gate. One inverter is used to invert the "ZERO's" of the data so that they are ANDed with the corresponding chip sequence S_o. Also the "ONE" data are ANDed (without inverting) with the chip sequence S_1. The outputs of the two AND gates pass through

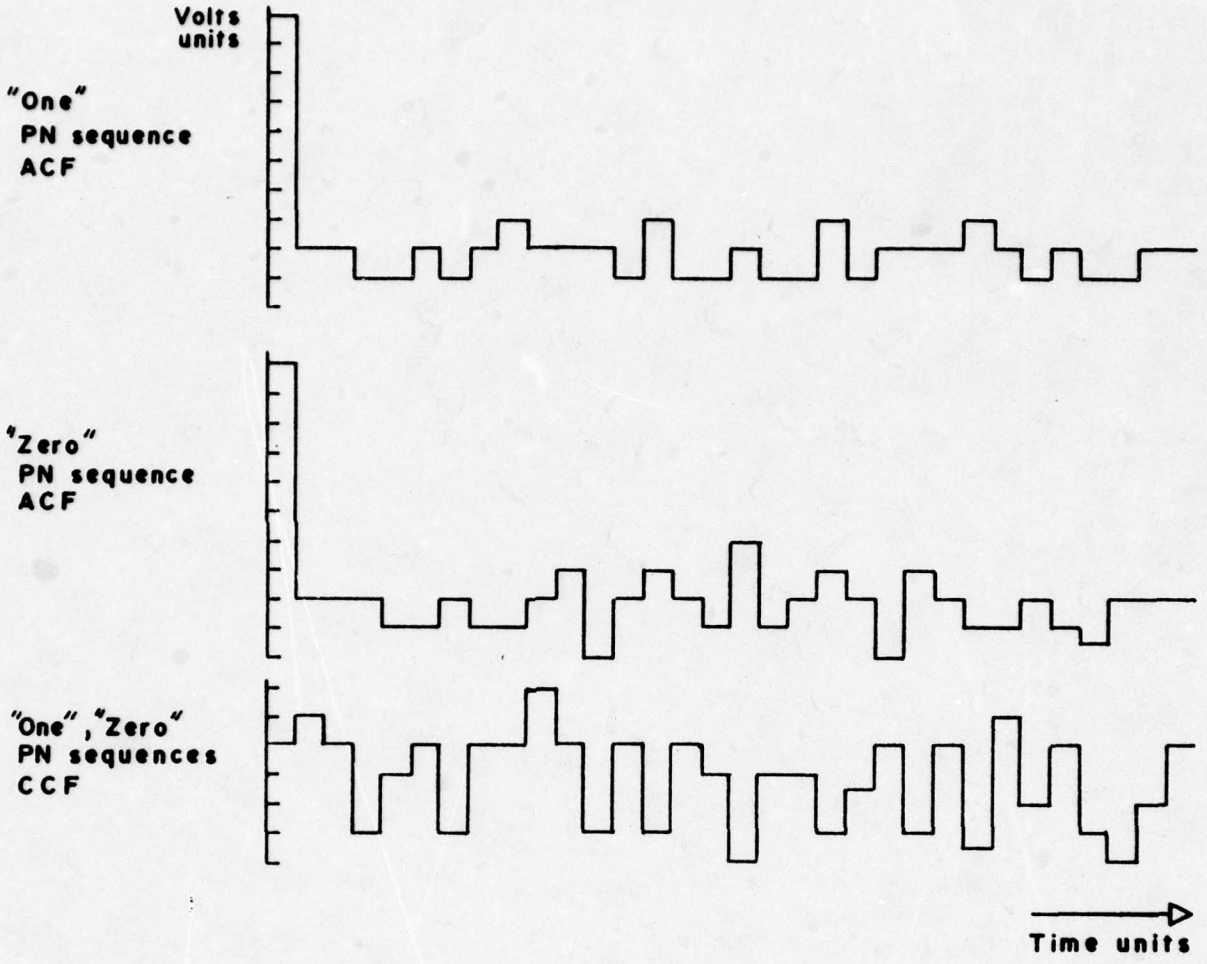


Figure 14. Calculated ACF's and CCF of "ONE" and "ZERO" PN sequences

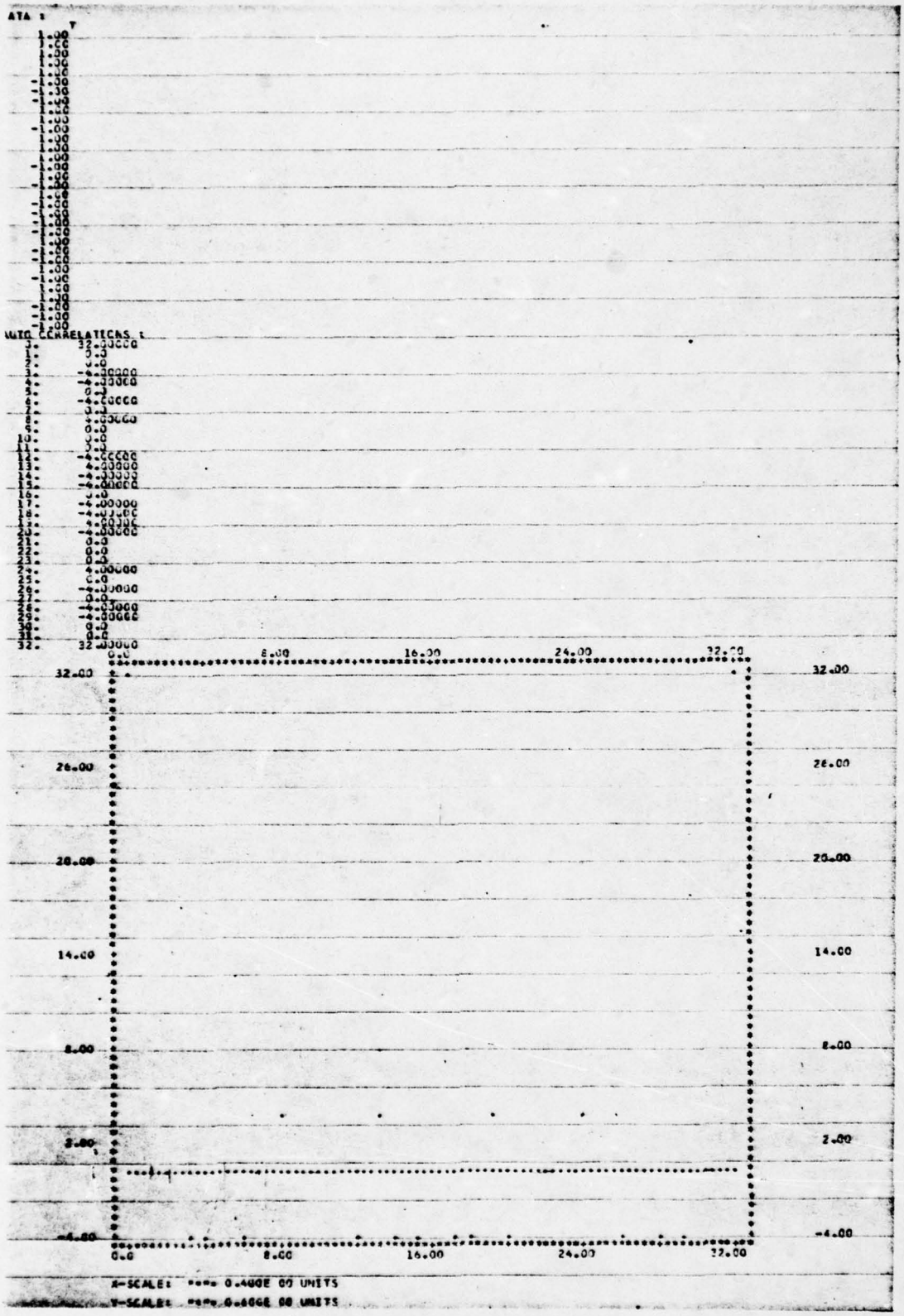


Figure 15. Computer generated ACF of data "ONE" PN sequence

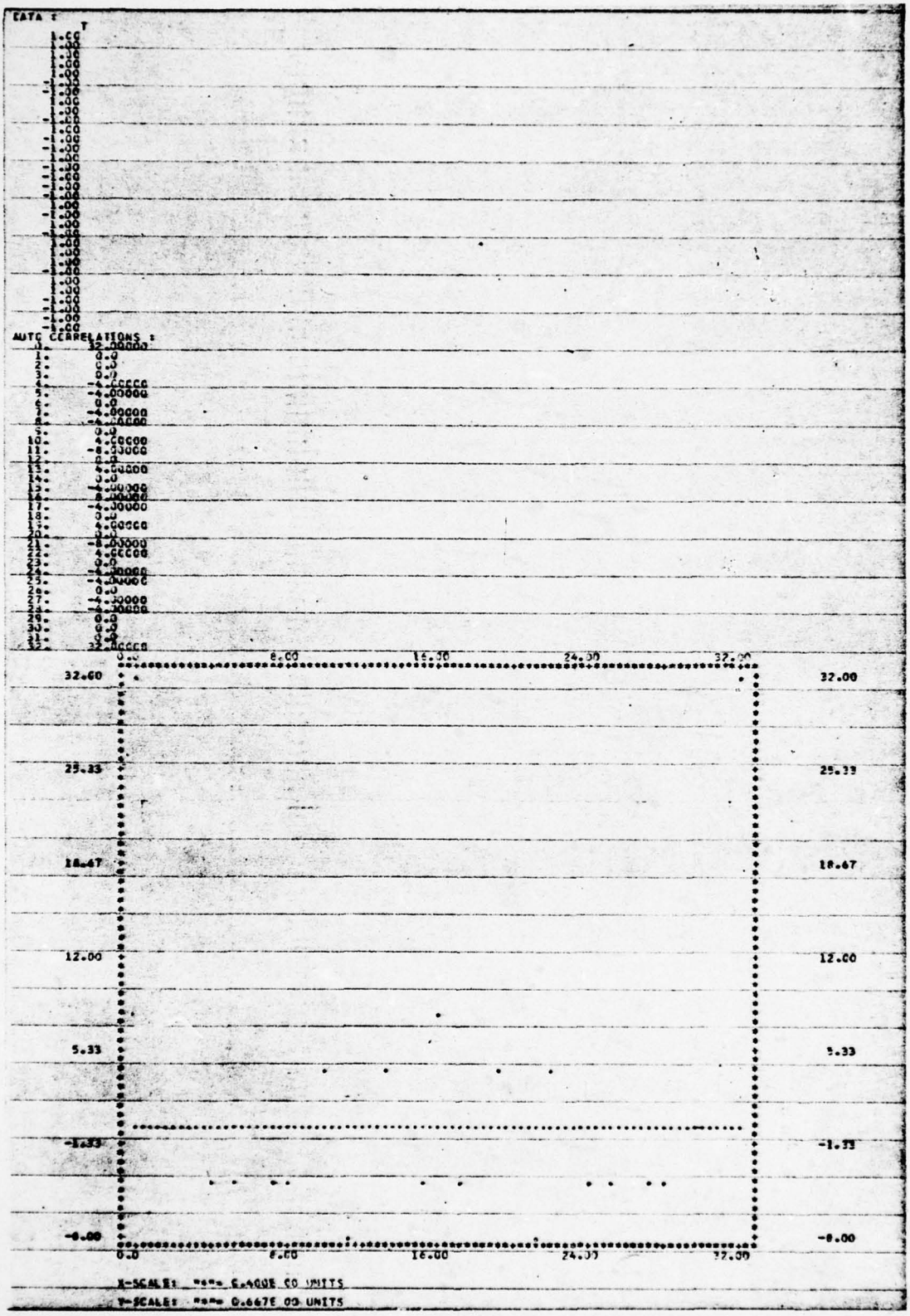


Figure 16. Computer generated ACF of data "ZERO" PN sequence

an OR gate to provide a continuous serial output of the spread data.

3. System Clock

The clock of the system is an LM566 VCO. The frequency of the VCO is a linear function of a control voltage, referred to as the modulating or dither voltage. The clock center frequency is determined by an external resistor and capacitor. The BJT amplifier amplifies the clock pulses to a peak voltage of 8V.

4. Frequency Divider

The frequency divider consists of two cascaded four-bit, up/down, binary, synchronous counters (DM 74193's). The counter outputs change state after the low-to-high transition of the clock. Each counter individually counts up to 16 different states. When the first counter is in state 15 ($1\ 1\ 1\ 1_2$) and in the count-up mode, a clock pulse (carry) will change the counters state to state zero ($0\ 0\ 0\ 0_2$) on the rising edge and simultaneously clock the following counter through the appropriate count-up terminal. By using the four outputs of the first counter and the first output of the second counter, a modulo 32 counter is constructed. This counter addresses the 32 rows of the memory matrix of the ROM in sequence, and its output provides the slow clock to the ΔM codec.

For a clock rate out of the BJT amplifier of 704 kHz, the ΔM is clocked at 704 kHz/32 = 22 kHz and thus the bit rate out of the ΔM is 22 k bits/second. The

time duration of each bit of the data d(t) is 45.45 μsec. The time required for generation of each 32 bit chip sequence is the 45.45 μsec. Fig. 17 shows the timing diagram of the modulo-32 counter. The ΔM digital output (data d(t)) is assumed to be "ONE" and the coresponding chip sequence is S_1.

D. DIGITAL MATCHED FILTER

Fig. 18 is a block diagram of the digital matched filter used in this project.

The digital matched filters consist of a simple 32 stage serial-in parallel-out shift register. Each stage of the shift register is tied to the data "ZERO" and data "ONE" summing junction either through an inverter or directly to a summing resistor. A direct connection corresponds to a "ONE" of the input chip sequence; an inverter connection corresponds to a "ZERO". In this manner, one 32 stage shift register suffices for both the data "ZERO" and data "ONE" sequences. The shift registers are clocked from the modulated (dithered) VCO.

The data "ZERO" and data "ONE" summing junctions provide inputs to two voltage comparators referenced to a voltage level set by a resistive voltage divider. The threshold is set above the highest sidelobe in the cross-correlation of the "ONE" and the "ZERO" data sequences.

Each of the two outputs triggers a monostable multivibrator. These components provide latitude in shaping the widths of the pulses delivered by the comparators.

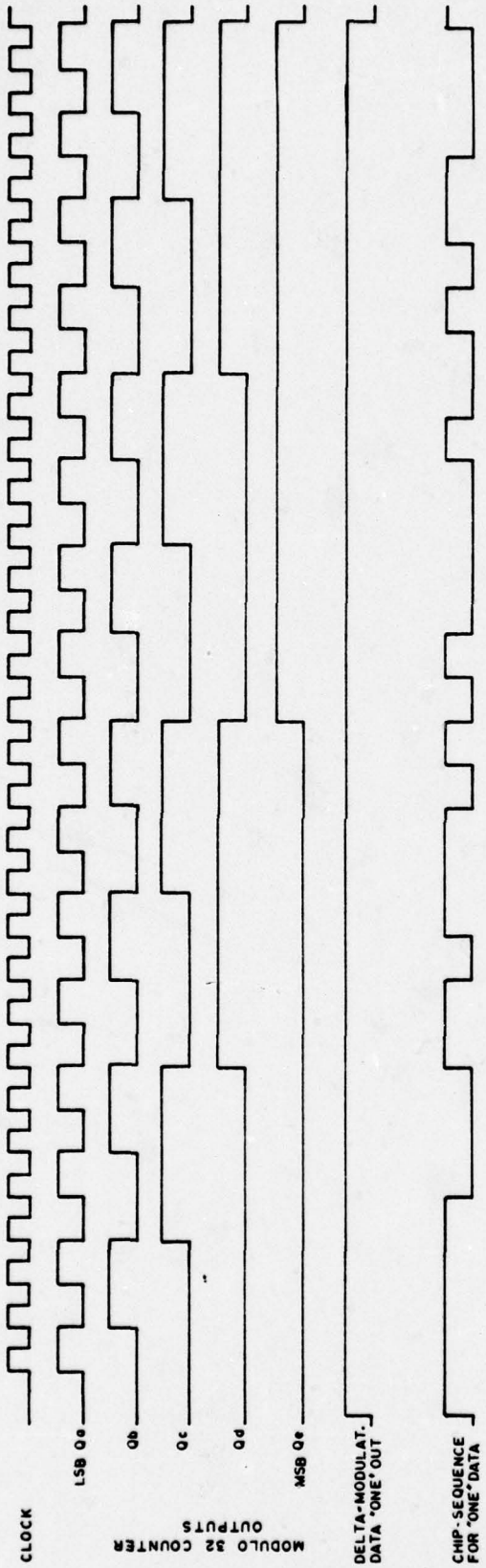


Figure 17. Timing diagram of the spreading circuitry

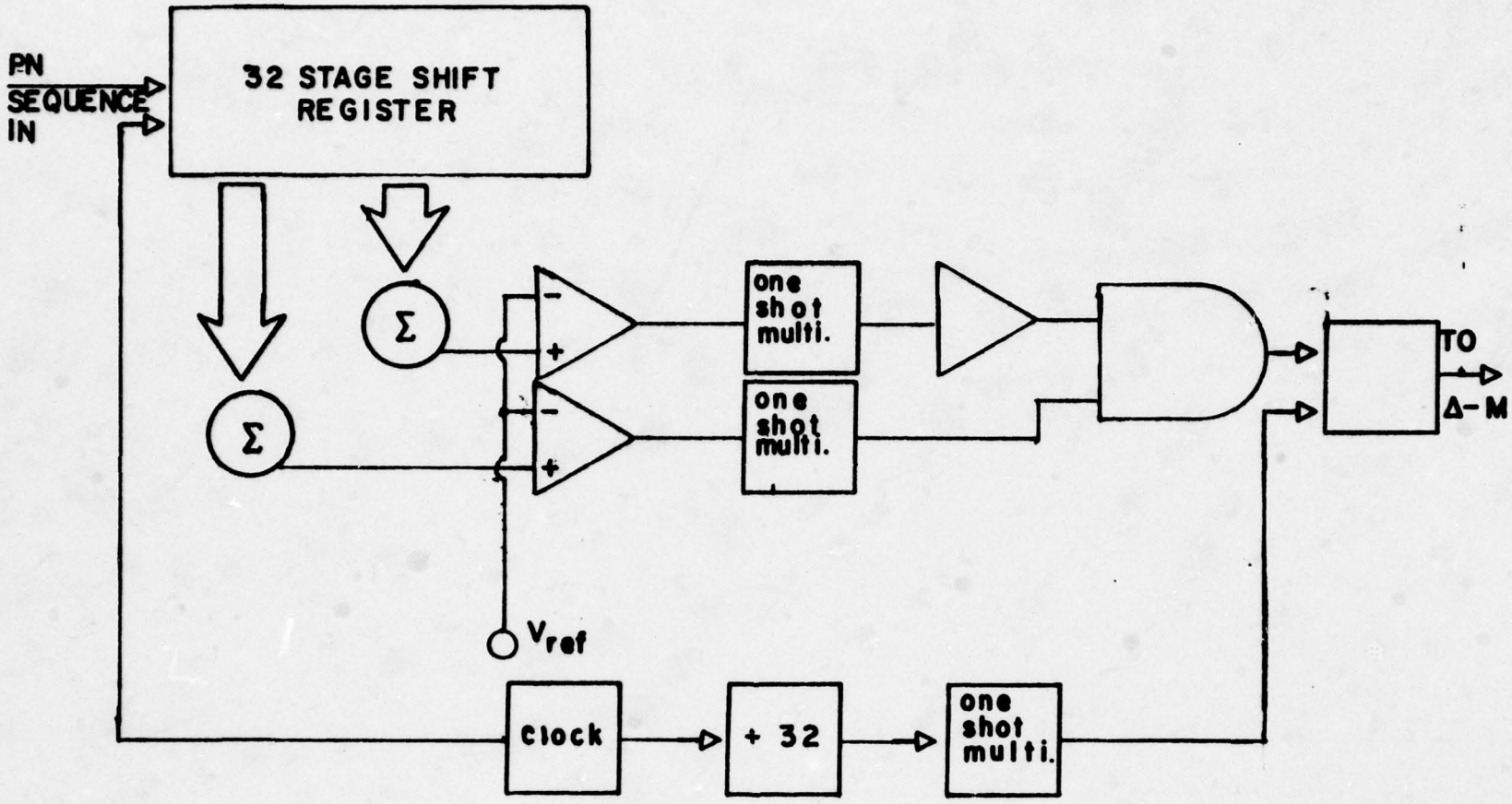


Figure 18. Digital matched filter

Digital logic is necessary to provide a proper input to the receiver ΔM decoder. The ΔM decoder requires a "ONE" or a "ZERO" for a full clock period. The following truth table determines the necessary logic function for the pulses from the monostable multivibrators to a delay flip-flop.

Pulse from "ONE" Schmitt trigger	Pulse from "ZERO" Schmitt trigger	Input to D-flip-flop
0	0	0
0	1	0
1	0	1
1	1	0

The function ("ONE") "$\overline{\text{ZERO}}$" describes the above truth table and is used as the input to the delay flip-flop. The D-flip-flop is clocked by the same divide-by-32 clock driving the delta modulators. To properly apply the data to the D-flip-flop it is necessary to shorten the width of this clock pulse using a monostable multivibrator. The output of the D-flip-flop is applied to the delta-demodulator.

Fig. 19 is a timing diagram which uses as an example the data sequence from the transmitter ΔM encoder.

Circuit schematic diagrams, printed circuit board foil patterns and pictures of bread board circuits of the digital matched filter are provided in Appendix A.

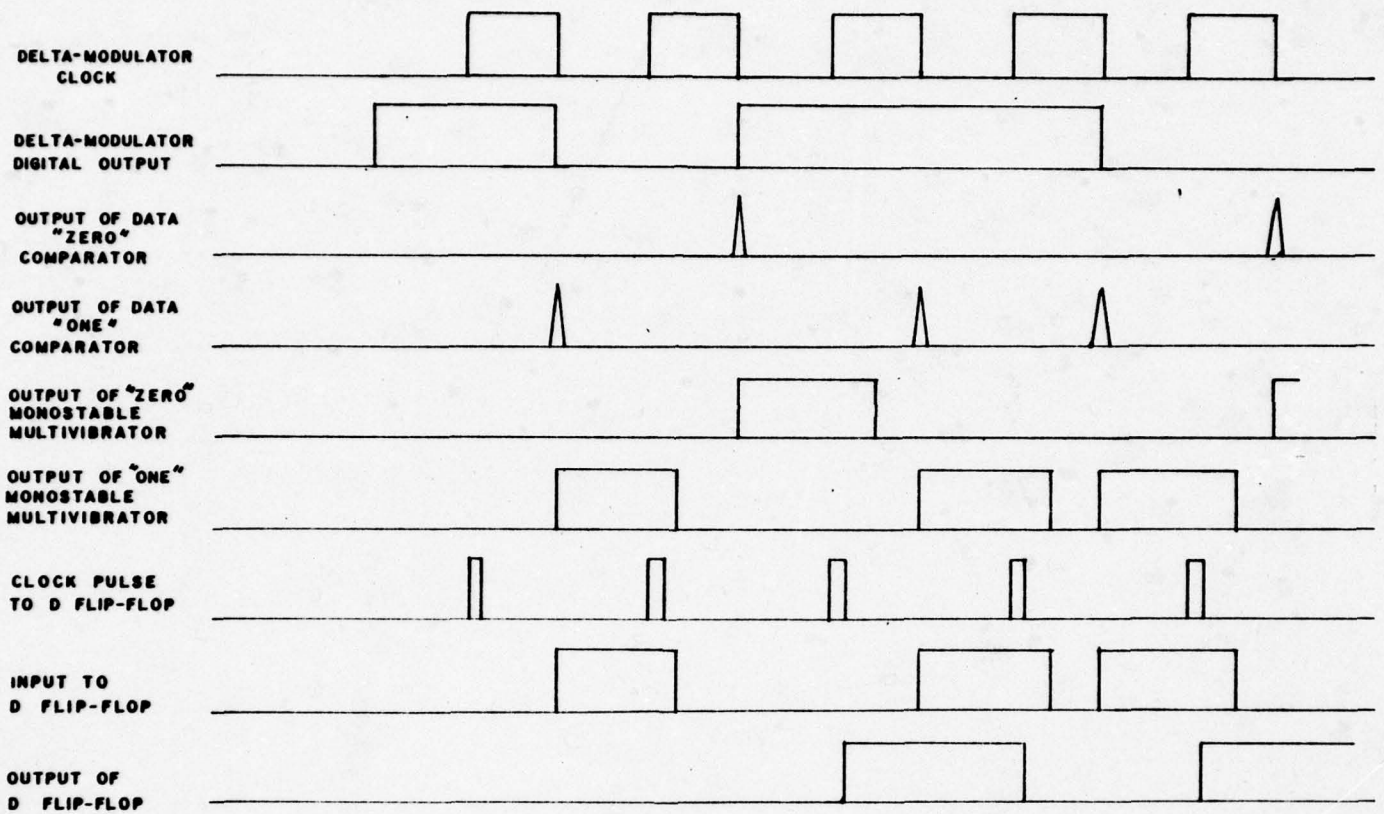


Figure 19. Timing diagram for the digital matched filter

IV. EXPERIMENTAL RESULTS

Once the spread spectrum system was operational several experimental areas were to be checked as listed:

(1) Outputs of various stages to ensure proper functioning.

(2) Performance of the system with additive, white, Gaussian noise and comparison with predicted behavior.

(3) Performance of the system with separate clocks in the transmitter and the receiver.

(4) LPF frequency response.

(5) Power spectra of spreading circuitry output with and without the dithered clock.

A. OUTPUTS AT VARIOUS STAGES IN THE SYSTEM

1. Spreading Circuitry Outputs

Fig. 20 is the output of the BJT amplifier clock and the divide-by-32 slow clock. Fig. 21 shows the chip sequences generated by the PROM and recorded by a brush reocrder. Fig. 22 and Fig. 23 are oscilloscope displays of the spreading sequences. The photographs were taken with a fast clock rate of about 800 kHz. The sequences repeat with frequency 800 kHz/32 = 25 kHz. The period of each sequence S_1 and S_o is 40 μsec. The peak amplitude of each chip is 4.6 V. Fig. 24 is the clock from the BJT without dither and Fig. 25 is the clock with dither.

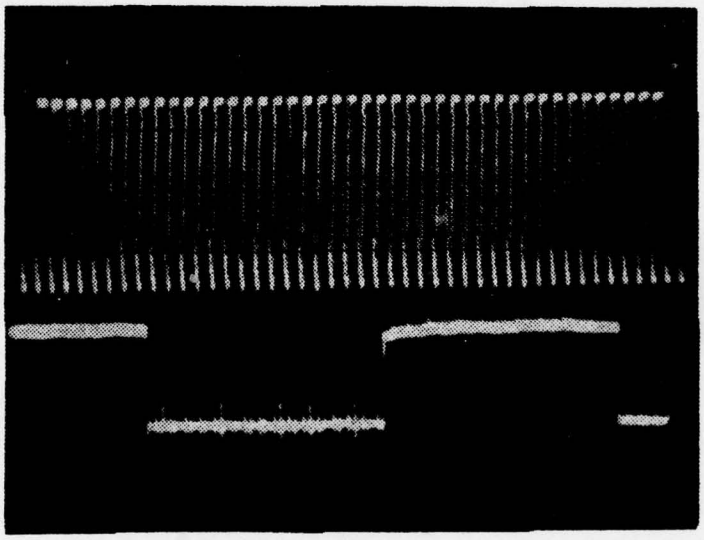


Figure 20. Shift register clock and ΔM clock
2 volt/vert. div., 5 μsec/horiz. dif.

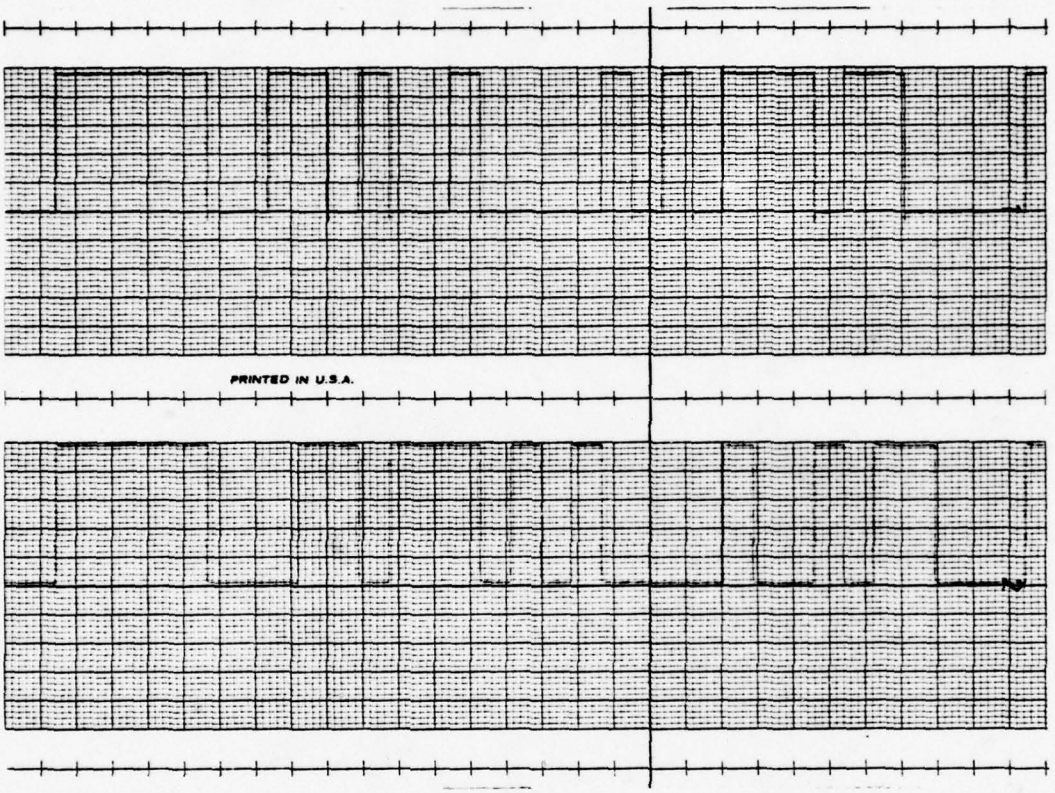


Figure 21. Chip sequences generated by the PROM Upper trace corresponds to a data "zero" and the lower trace corresponds to a data "one"

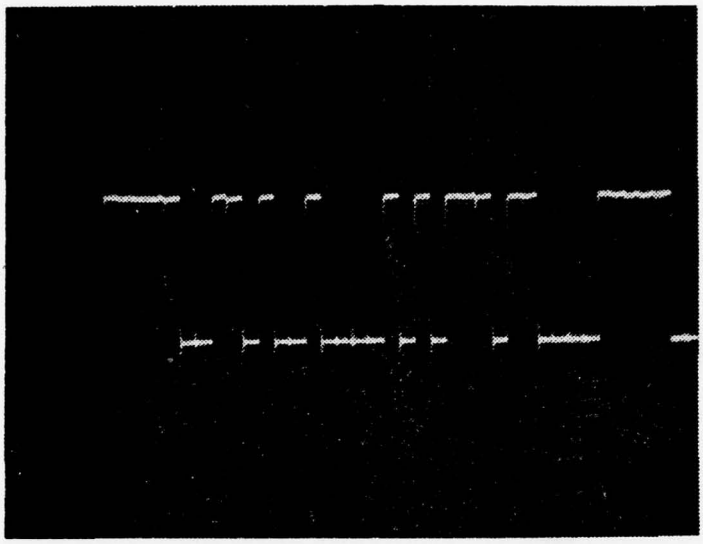


Figure 22. "ZERO" S_o chip sequence 2 volt/ vert. div., 5 μsec/Horiz, div.

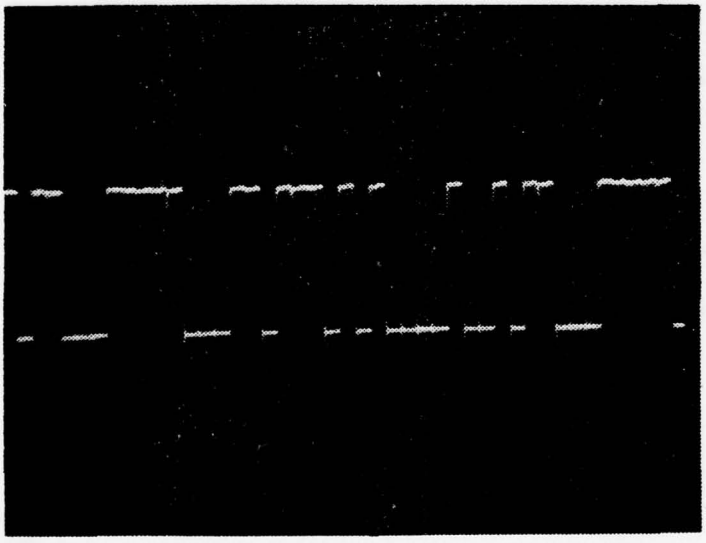


Fig. 23. "ONE" S_1 chip sequence 2 volt/ vert. div., 5 μsec/Horiz. div.

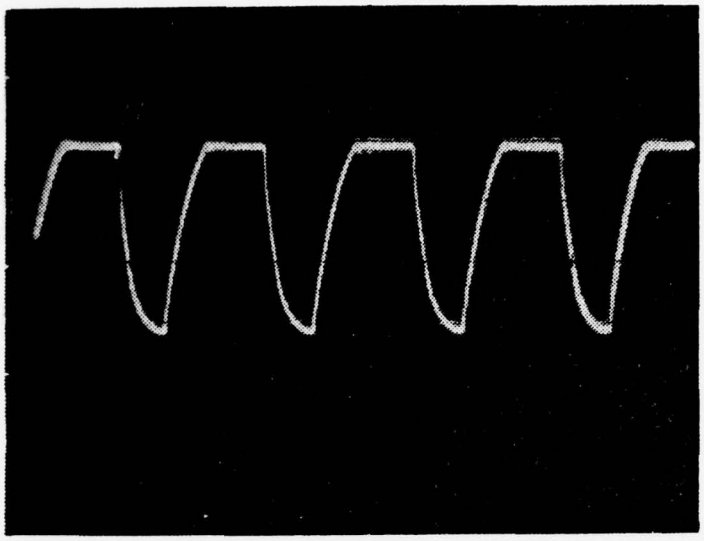


Fig. 24. Clock pulses out of the BJT amplifier without dither, 2 volt/vert. div., 0.5 μsec/Hor. div.

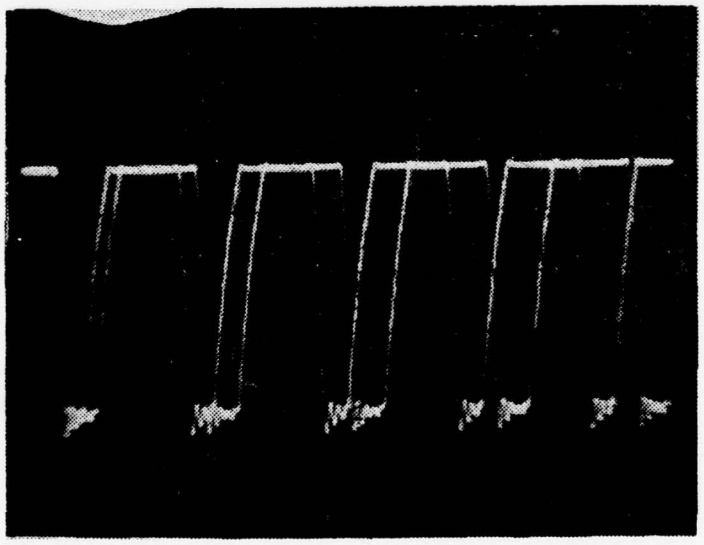


Fig. 25. Clock dithered with a 4 kHz square wave, 5 V peak to peak.

No pictures of the output of the ΔM encoder are available. Synchronization of the oscilloscope was not possible with a random data output of the ΔM encoder.

2. Digital Matched Filter Outputs

Fig. 26 and Fig. 27 are dual trace photographs of the cross correlations and autocorrelations at the summing junctions of the digital matched filter (DMF). Fig. 28 is a dual trace of the two summing junctions with a square wave out of the transmitting ΔM (resulting from a D.C. analog input). Fig. 29 shows a summing junction output with music applied to the transmitting ΔM and a dithered clock. Fig. 30 and Fig. 31 are dual traces of the transmitter ΔM output with D.C. input and the summing junctions of the DMF. Note correlation peaks corresponding to data

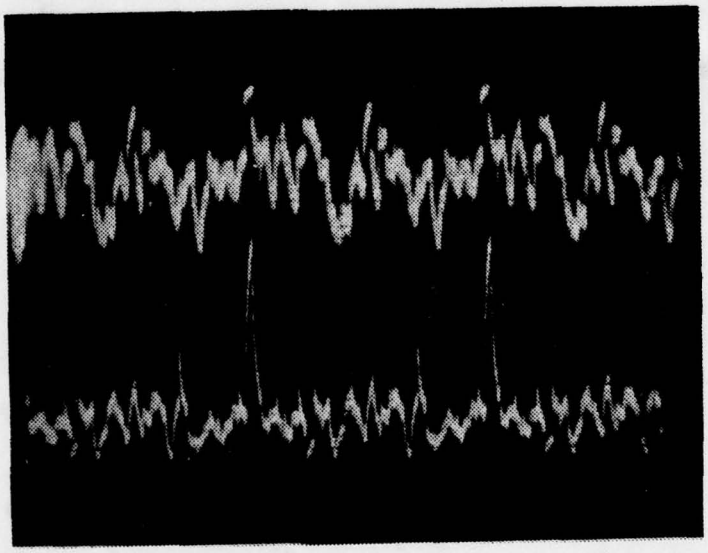


Fig. 26. Upper trace: cross correlation of "ZERO" sequence on "ONE" taps.
Low trace: ACF of "ZERO" sequence.
0.5 volt/Vert. div. 10 μsec/Horiz. div.

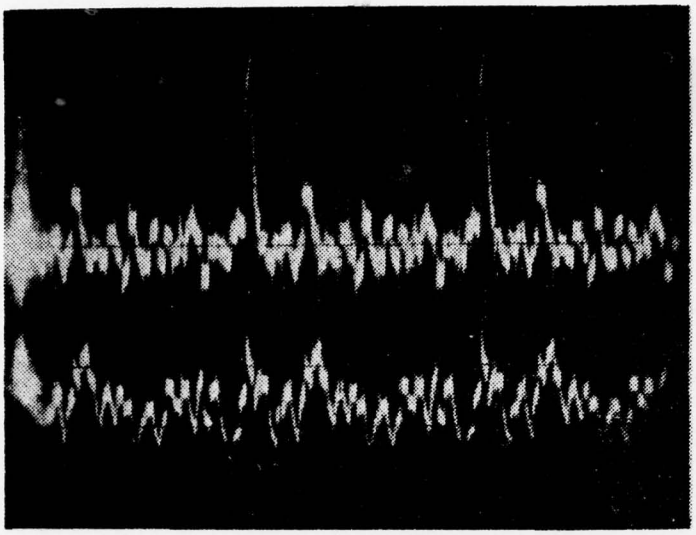


Fig. 27. ACF of "ONE" sequence and cross correlation of "ONE" sequence on "ZERO" taps.

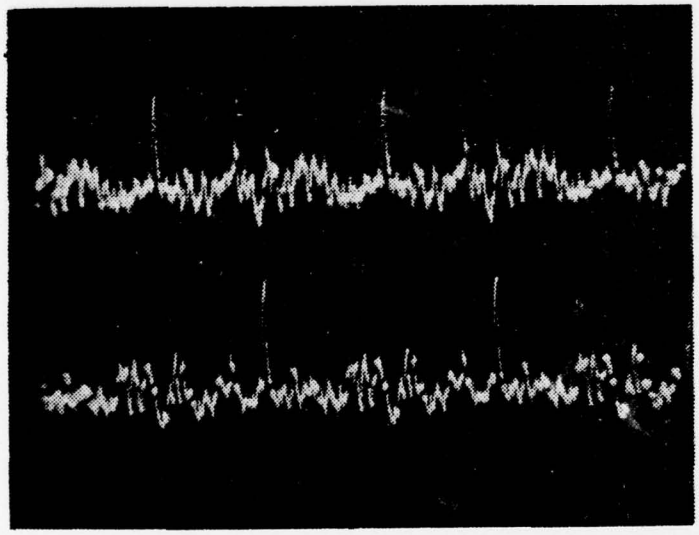


Fig. 28. Dual trace of the "ZERO" (low trace) and "ONE" (upper trace) summing junctions, with DC input to ΔM

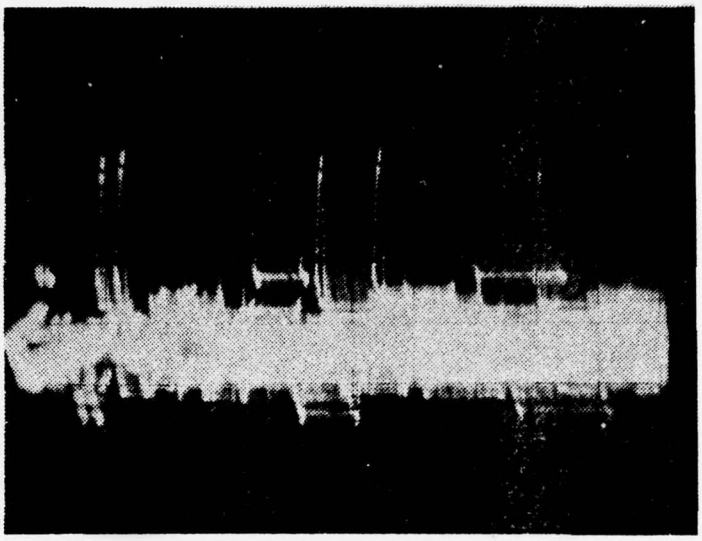


Fig. 29. "ZERO" summing junction output with music into the ΔM and clock dithered by a square wave of 4 kHz and 6 V amplitude peak to peak

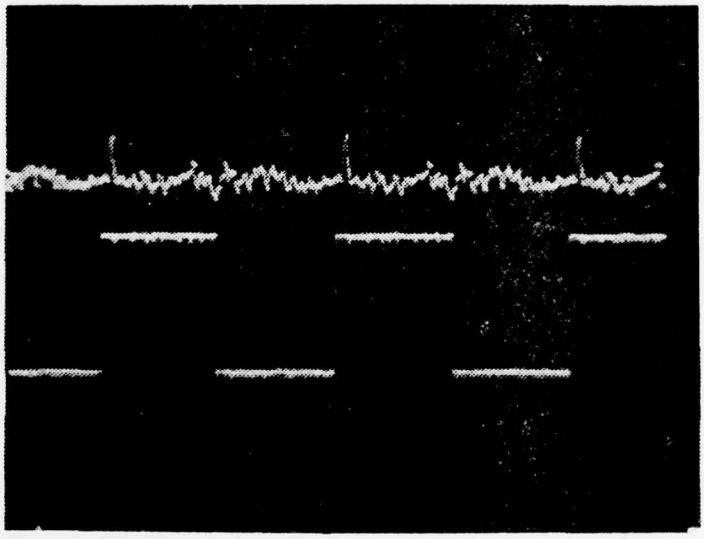


Fig. 30. Low trace: Output of transmitter's ΔM with DC analog input and output of the "ZERO" summing juntion of the MF

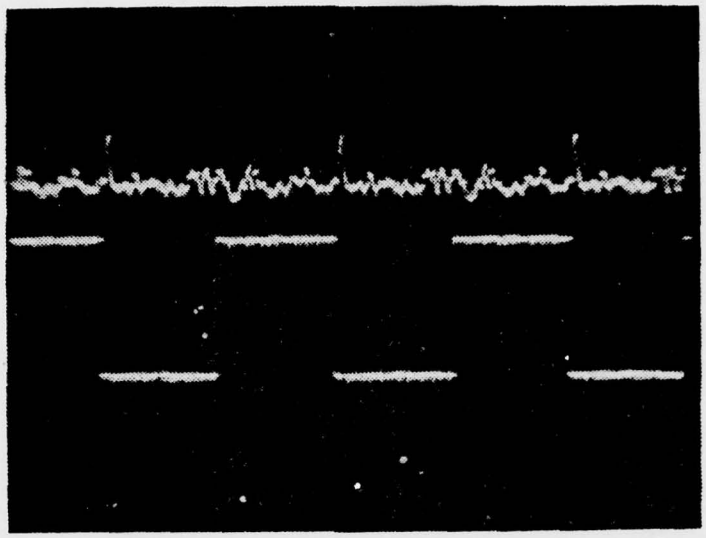


Fig. 31. Output of transmitter's ΔM with DC analog input and output of the "ZERO" summing junction of the MF

"ONE" and "ZERO". Fig. 32 and Fig. 33 are similar dual traces showing the summing junction output with the receiver ΔM decoder input signal.

3. Outputs of the Receiver ΔM Decoder

Fig. 34 is a dual trace of the DMF summing junctions with a square wave applied to the transmitter ΔM encoder and Fig. 35 shows the square wave applied to the transmitter and the final waveform output of the receiver after the LPF. Fig. 36 is a dual trace of a 600 Hz input sine wave and the filter output, and Fig. 37 shows input and output for

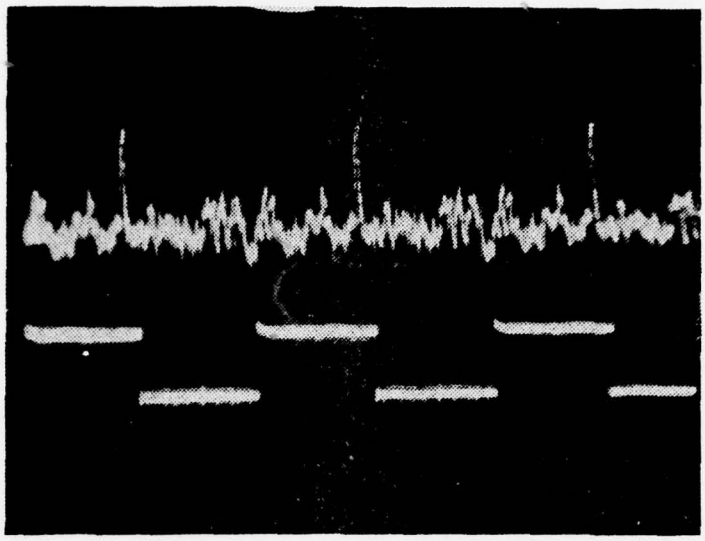


Fig. 32. Low trace: input to receivers ΔM with DC analog input and output of the "ONE" summing junction of the MF

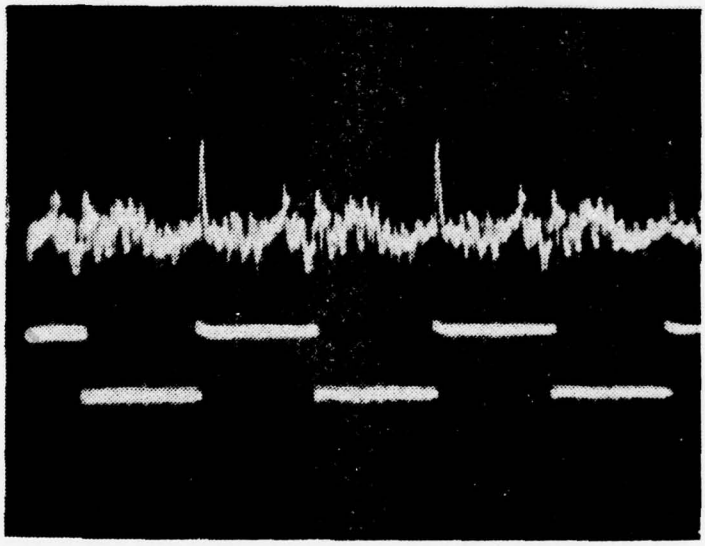


Fig. 33. Input to the receiver's ΔM with DC analog input and output of the "ZERO" summing junction

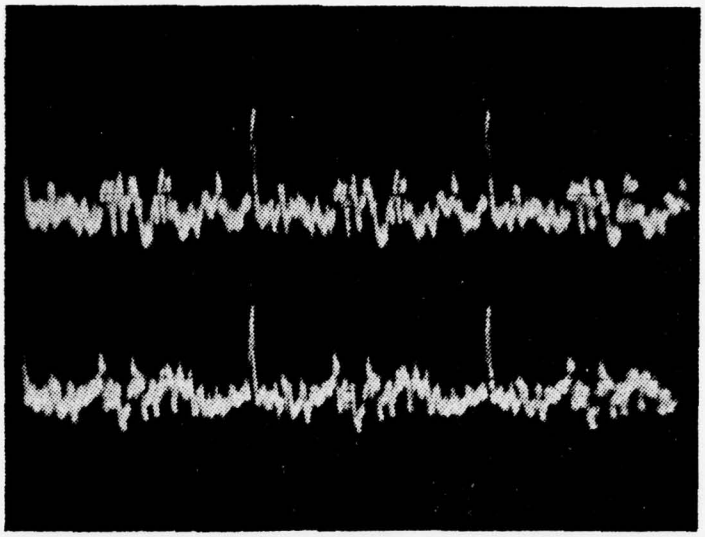


Fig. 34. Square wave input to ΔM. Lower trace: ACF of "ZERO" sequence; upper trace: ACF of "ONE" sequence.

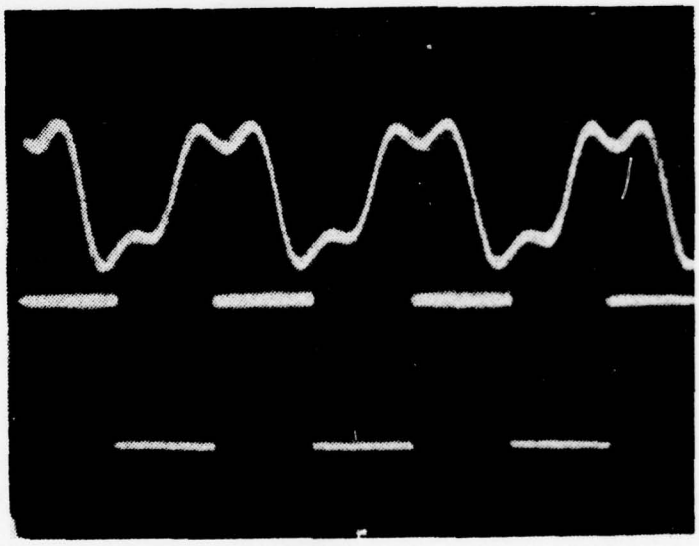


Fig. 35. Square wave input to ΔM and output of filter

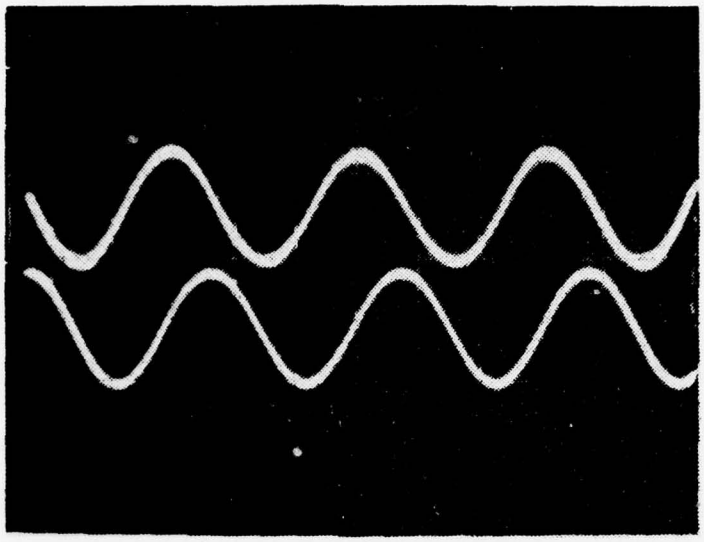


Fig. 36. 600 Hz sine wave input to ΔM and output of filter

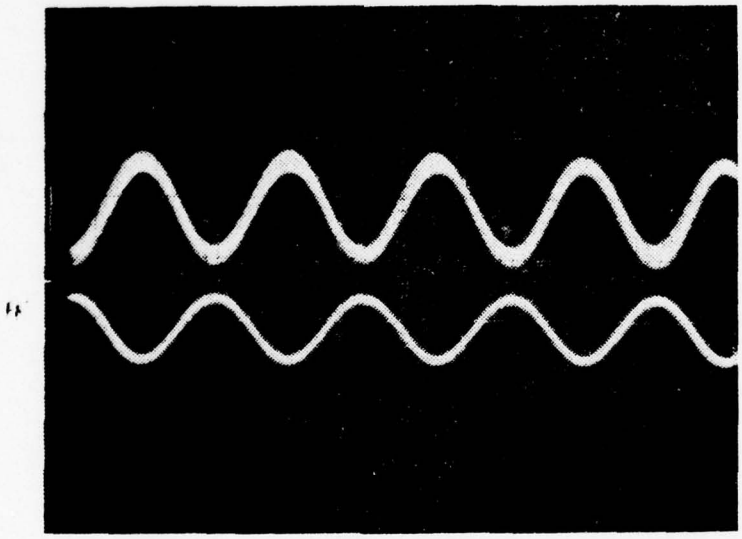


Fig. 37. Sine wave input (2 kHz) to ΔM and output of filter

a 2kHz sine wave. Fig. 38 and Fig. 39 show voice and music system input and output.

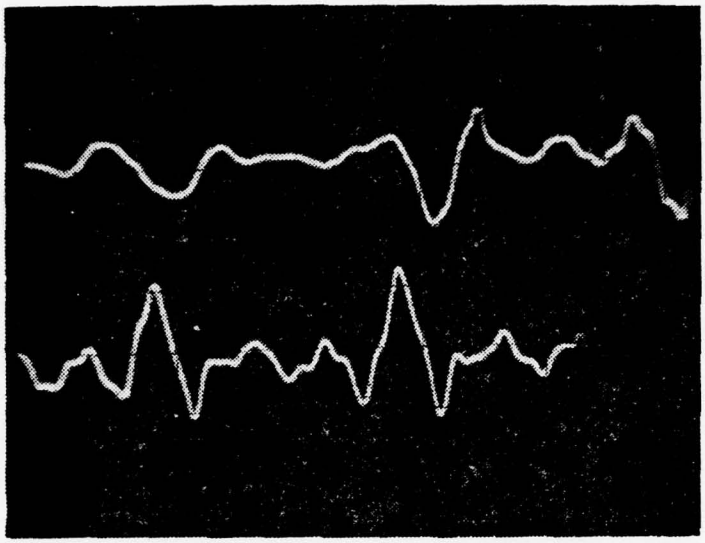


Fig. 38. Low trace: Voice input to ΔM 0.5 volt/ vert div.
Upper trace: Output of filter 2 volt/ vert div. 2 msec/Hor. div.

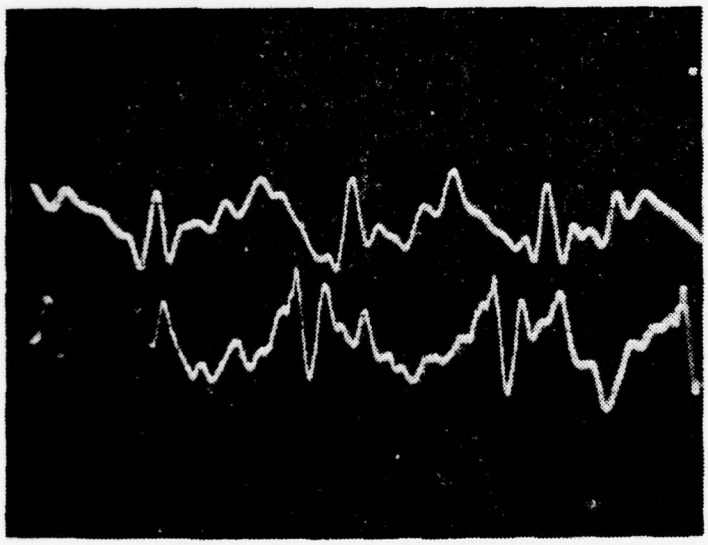


Fig. 39. Low trace: Music input to ΔM and 1 volt/vert. div.
Upper trace: Output of filter 5 volt/ vert div. 2 msec/Hor. div.

B. SYSTEM PERFORMANCE WITH ADDITIVE NOISE

A subjective evaluation of the system's performance with additive white, Gaussian noise was made. Noise from a General Radio Co., Random Noise Generator type 1390-B was amplified and summed with the PN sequence.

The amplification and summing circuitry is shown in Appendix A. Table II is the resulting data from this experiment. The system functioned well up to a signal to noise ratio of -4.5 dB. The processing gain of a 32 bit PN sequence is approximtely 15 dB and if one assumes digital circuitry requires 8 to 12 dB of signal-to-noise ratio (SNR) to function properly, then the experimental results are close to what is expected.

Fig. 40 is the PN sequence at the noise summing junction without noise. Fig. 41 shows the sequence plus noise at a SNR of about -1 dB. Fig. 42 is the output of a summing junction without noise and Fig. 43 is the same summing junction output with noise.

C. SYSTEM PERFORMANCE WITH SEPARATE CLOCKS IN THE TRANSMITTER AND RECEIVER

The receiver shift registers were driven by a signal generator square wave to attempt to synchronize the transmitter and receiver using different clocks. The ΔM decoder clock was derived from ORing the outputs of the data "ONE" and "ZERO" monostable multivibrators in the DMF. When no dither was applied to the transmitter clock, synchronization

Signal	Signal plus Noise					
V_s Volts	V_s+V_n Volts	$V_s^2 = S$	$(V_s+V_n)^2 = S+N$	$N = (S+N) - S$	S/N	[S/N] db
0.46	0.5	0.2116	0.25	0.0384	5.51	7.4
0.46	0.6	0.2116	0.36	0.1484	1.423	1.53
0.46	0.7	0.2116	0.49	0.2784	0.76	-1.19
0.46	0.75*	0.2116	0.5625	0.3509	0.603	-2.19
0.46	0.80	0.2116	0.64	0.4284	0.494	-3.06
0.46	0.85	0.2116	0.7225	0.5109	0.4142	-3.83
0.46	0.90**	0.2116	0.81	0.5984	0.3536	-4.515

* Reset threshold, signal audible

** Reset threshold, signal barely audible

TABLE II

Results of additive noise experiment

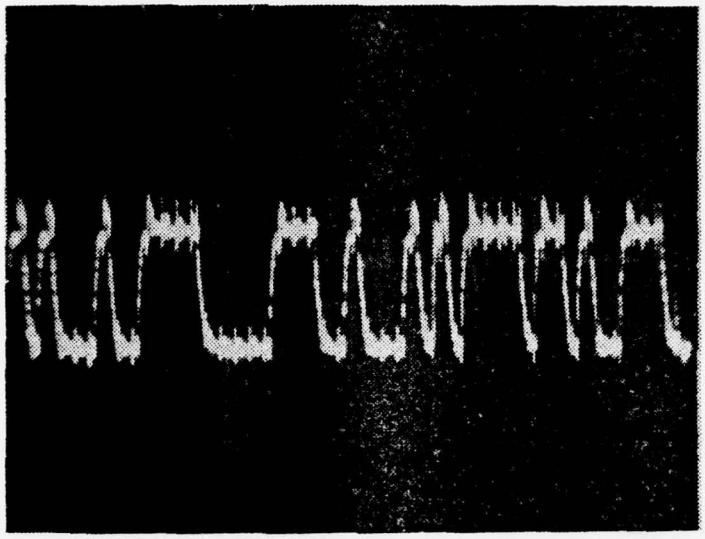


Fig. 40 PN sequences at noise junction. Signal level 0.46 volts RMS 0.5 volt/vert. div. 5 μsec/Hor. div.

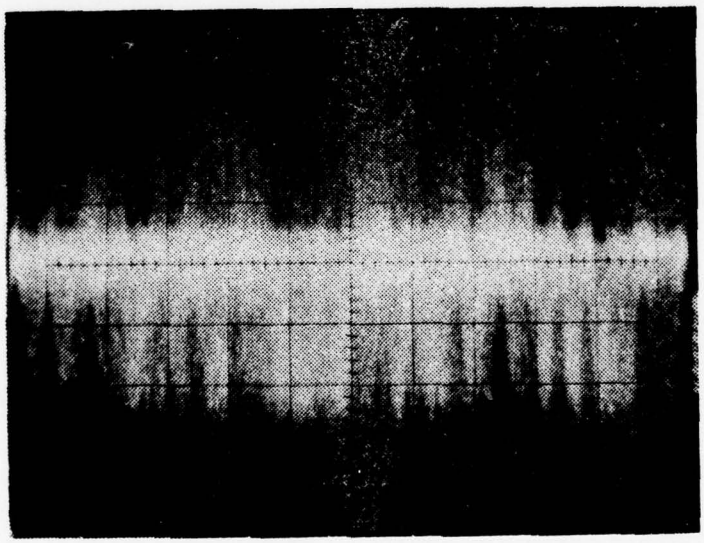


Fig. 41 Output of noise junction signal plus noise level 0.7 volt RMS, signal is buried in white noise.

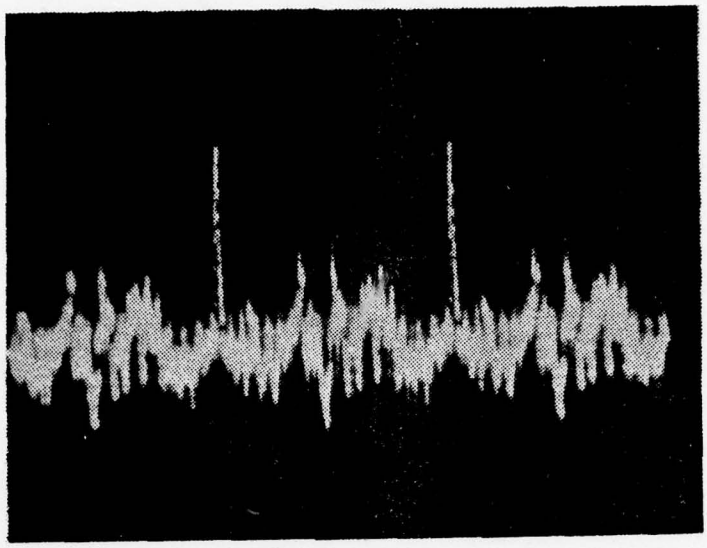


Fig. 42 Output of "ZERO" summing junction with DC input to transmitter ΔM. Signal level to noise junction 0.46 volts RMS 0.5 volt/ Vert. div. 20 μsec/Hor. div.

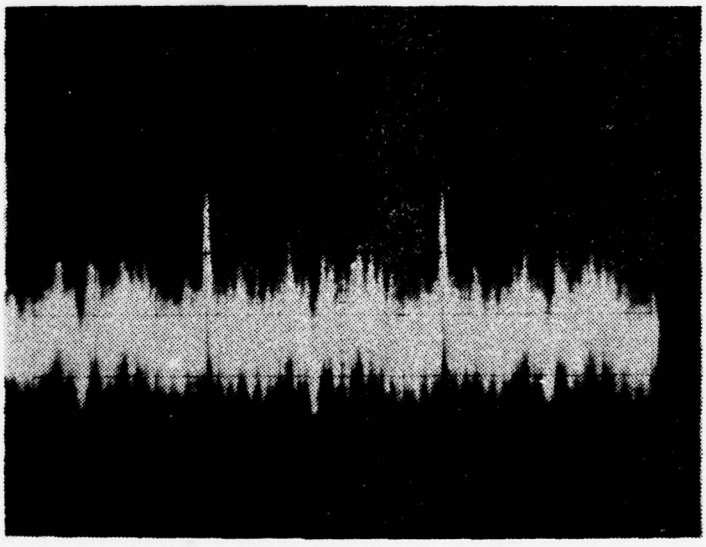


Fig. 43 Output of "ZERO" summing junction with DC input to transmitter ΔM signal plus noise at noise junction.

was possible. Once the transmitter clock was dithered, with no attempt made to dither the receiver clock, audible output of poor quality could be achieved.

D. LOW PASS FILTER FREQUENCY RESPONSE

Fig. 44 is the experimental amplitude frequency response curve of the six-pole, low pass filter.

E. POWER SPECTRA OF SPREADING CIRCUITRY OUTPUT WITH AND WITHOUT CLOCK DITHER

To test the original clock dither hypothesis mentioned in Chapter II, the power spectra of the spread PN sequence was taken with and without clock dither. To allow this data to be taken, the clock rate of the fast clock had to be reduced by approximately a factor of 10 for compatability with available spectrum analysis equipment.

Fig. 45 is the power spectrum of the PN sequence with no dithered clock. Fig. 46 shows the power spectrum with a small amount of dither. Fig. 47 and Fig. 48 are the power spectra with progressively more dither. Data appears to agree with the hypothesis.

The data was taken with a Spectral Dynamics Corp. Model 360 Digital Signal Processor.

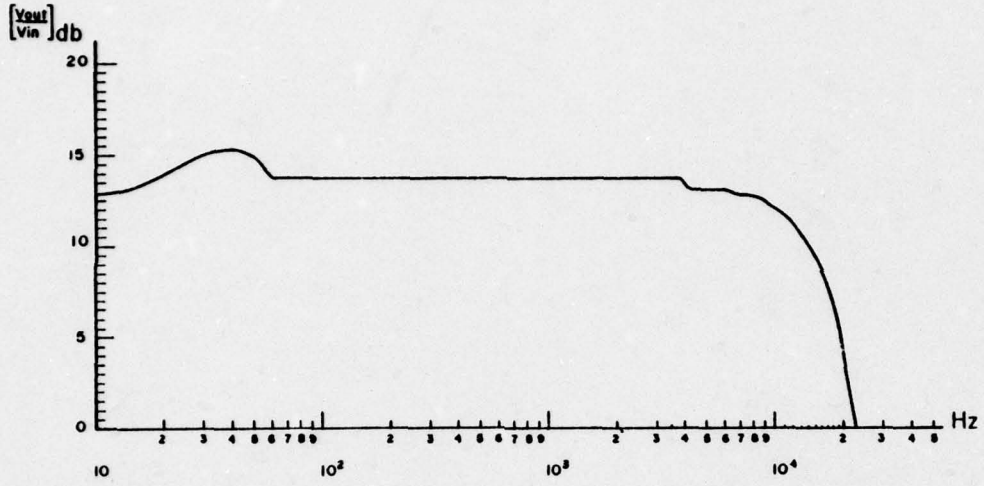


Figure 44. Experimental ferquency response of the LPF

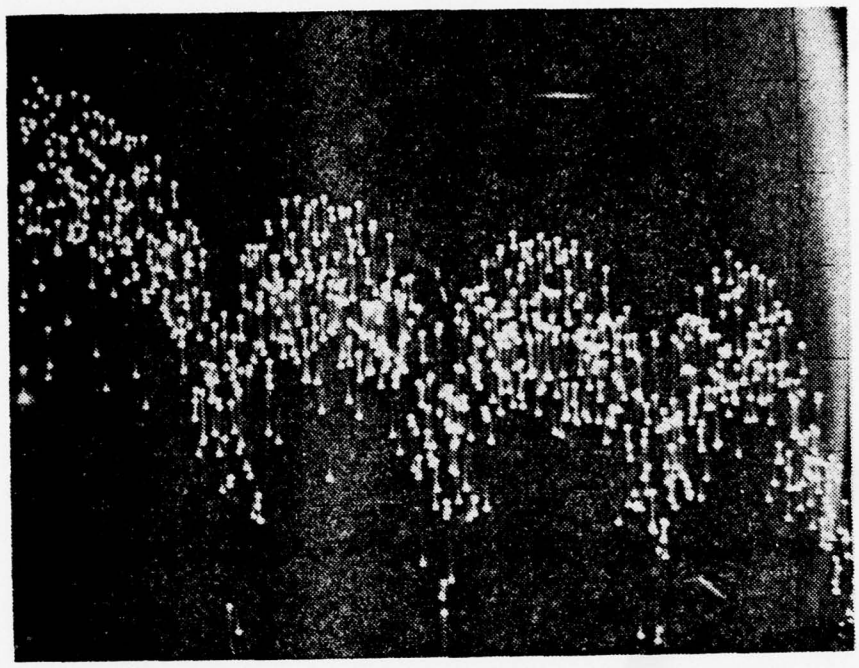


Fig. 45 Lower spectrum of spread data with no dithering clock

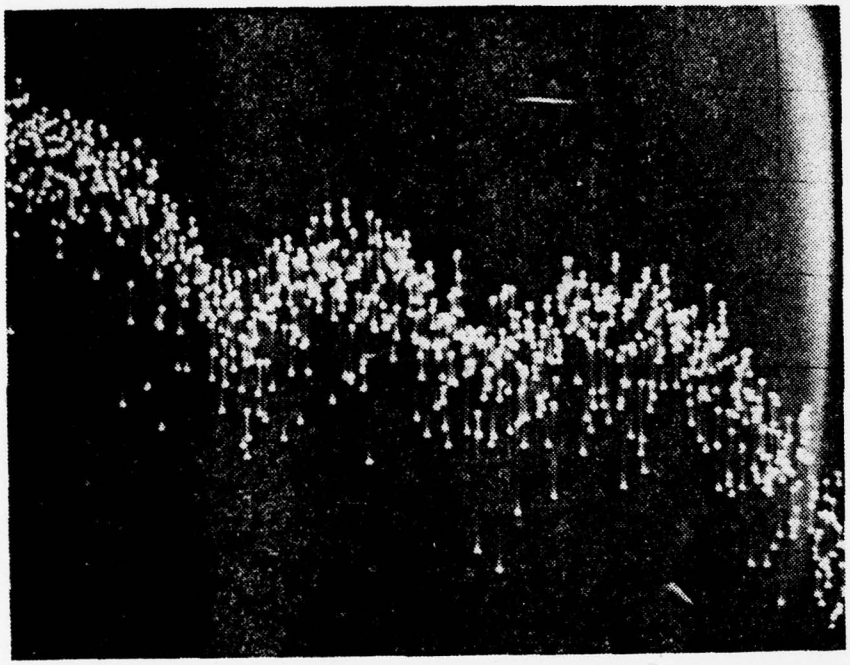


Fig. 46 Power spectrum of spread data with low dither rate

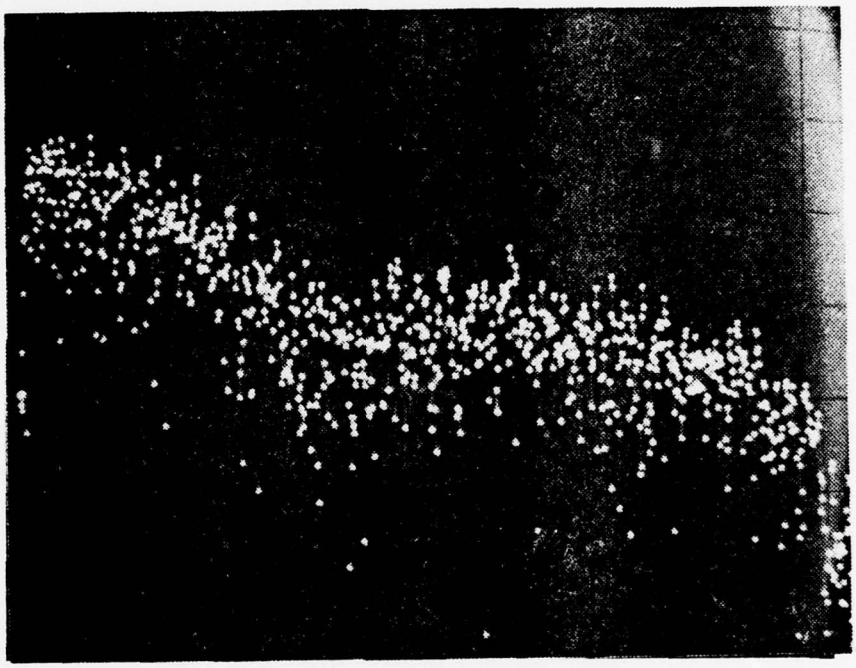


Fig. 47 Power spectrum of spread data with higher dither rate

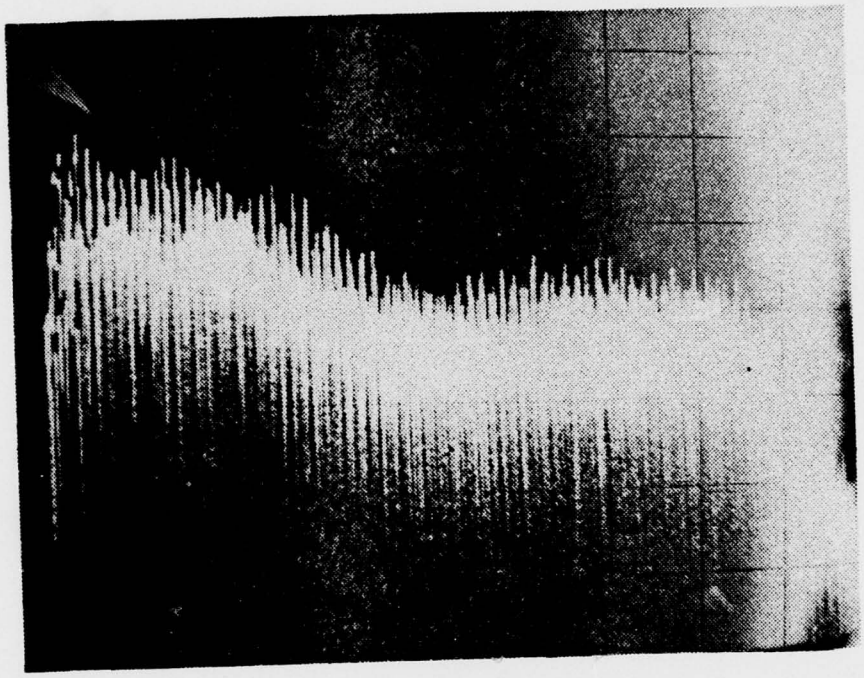


Fig. 48 Power spectrum of spread data with high dither rate

V. COMMENTS AND CONCLUSIONS

ΔM provides a relatively simple modulation/demodulation (MODEM) scheme. A single ΔM IC provides A/D and D/A conversion for good quality voice or music reproduction. Clock dither does not appreciably affect this MODEM.

Use of a sequence generating ROM and a digital MF is a simple method of recovering a spread signal. Some noise immunity is obtained even with a relatively short PN sequence. Dithering the clock does not affect the despreading operation, as long as the receiver and transmitter clocks are synchronized.

Use of printed circuit boards, shielded chassis, and coaxial cables improved the system greatly over the original breadboarded circuits.

Several areas for improvement or further evaluation are listed:

(1) Power supplies could be better regulated.

(2) The DMF voltage comparator could be better designed.

(3) The audio amplifier design could be improved upon.

(4) The input analog waveform should be amplitude and frequency limited to allow a reduction in the ΔM clock rate.

(5) Error correcting coding could be used for better performance in low SNR applications.

(6) Design of the system for radio frequency transmission would be interesting.

(7) A method of synchronizing dithered clocks is necessary.

APPENDIX A

Schematic Diagrams and Printed Circuit Foil Patterns

Figs. 49 through 65 are schematic diagrams, printed circuit (PC) board foil patterns and photographs of bread-boarded circuits used in this project.

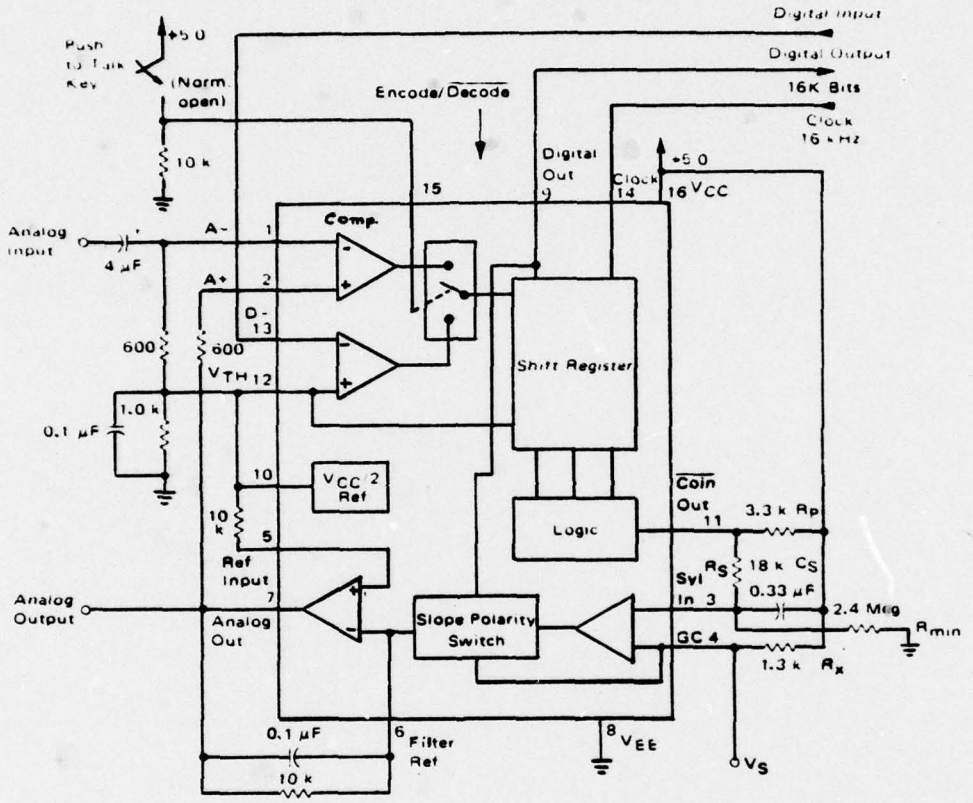


Figure 49. Schematic diagram of the ΔM

Component List for the LPF

OP AMPS - 741

$R_{11}, R_{22}, R_{21}, R_{22}, R_{31}, R_{32}$ - 10K

R_{13}, R_{23}, R_{33} - 39K

R_{14} - 2.7K

R_{24} - 22K

R_{34} - 56K

C - 10μ

$C_{11}, C_{12}, C_{21}, C_{31}$ - 0.0082μ

C_{22}, C_{32} - 0.012μ

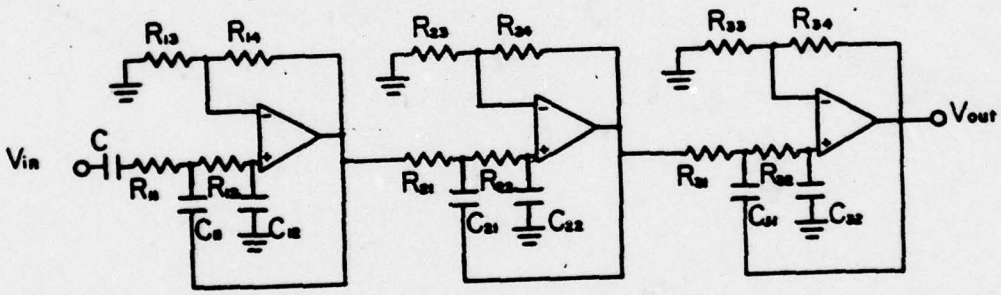


Figure 50. Schematic diagram of the low pass filter

pins 3,4,5,7,10,11,12 are grounded

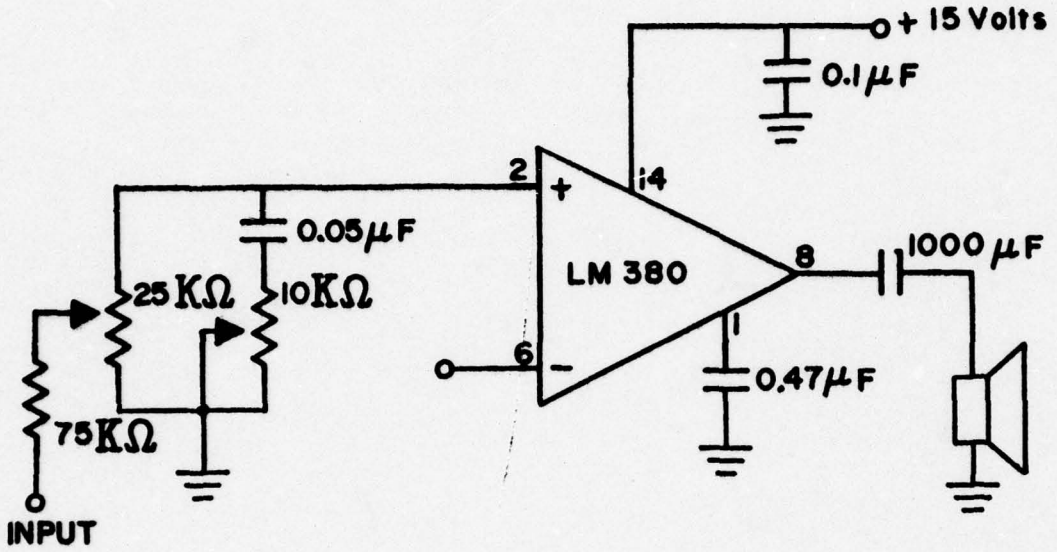


Figure 51. Schematic diagram of the audio amplifier

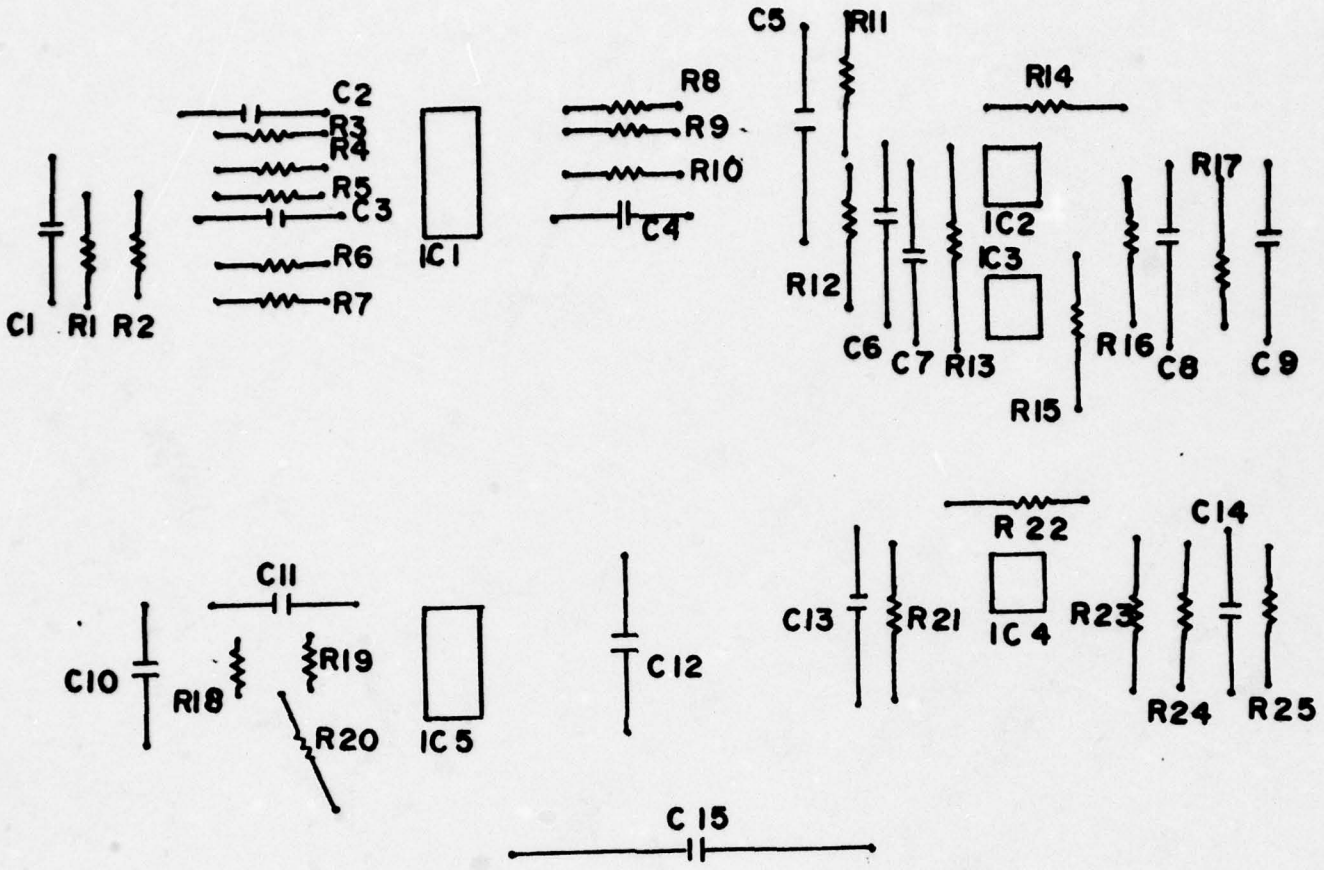


Figure 52. Component layout for ΔM PC board

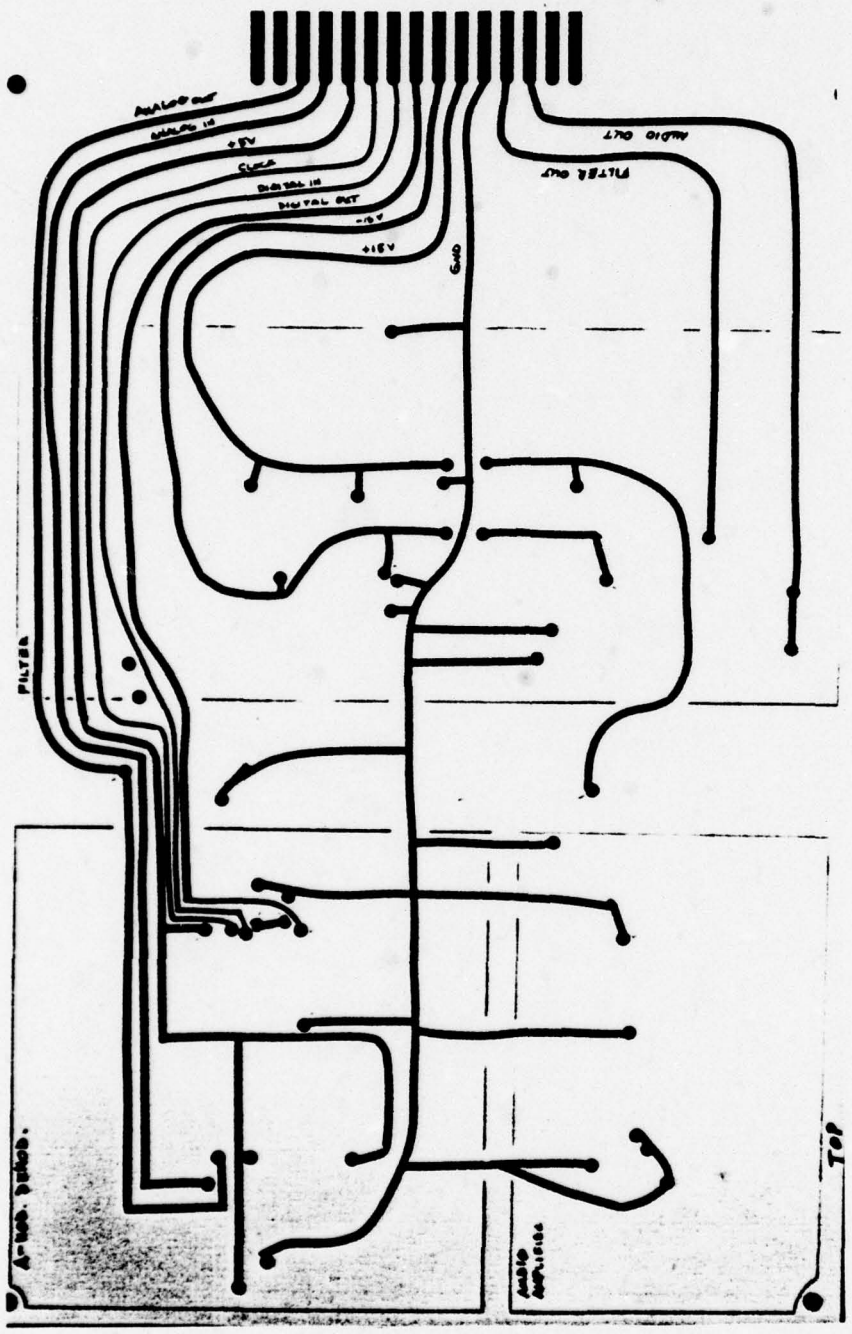


Figure 53. ΔM PC foil pattern, top

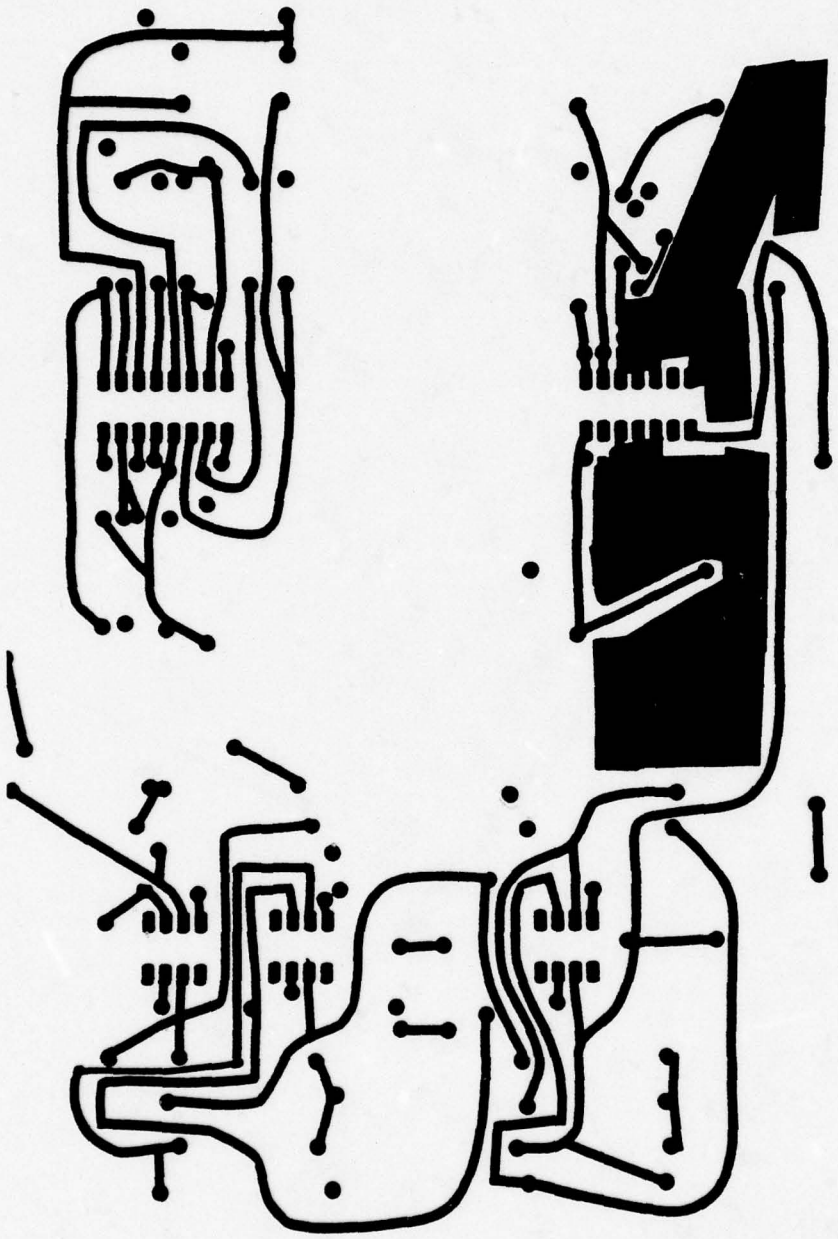


Figure 54. ΔM PC foil pattern, bottom

Component List for ΔM PC Board

C1 - 0.33 μ
C2 - 4 μ
C3,C4,C12 - 0.1 μ
C5 - 10 μ
C6,C7,C8,C14 - 0.0082 μ
C9,C13 - 0.012 μ
C10 - 0.05 μ
C11 - 0.47 μ
C15 - 1000 μ

IC1 - XC 3418 (ΔM)
IC2-IC4 - 741 (OP AMP.)
IC5 - LM 380 (Audio Amp.)

R1 - 2.4M
R2 - 18K
R3,R8 - 600 Ohm
R4 - 1.3K
R5,R6,R9,R11,R16,R17,R23,R24 - 10K
R7 - 3.3K
R10 - 1K
R12 - 5.1K
R13,R15,R21 - 39K
R14 - 5.7K
R18 - 10K POT
R19 - 25K POT
R20 - 75K
R22 - 22K
R25 - 56K

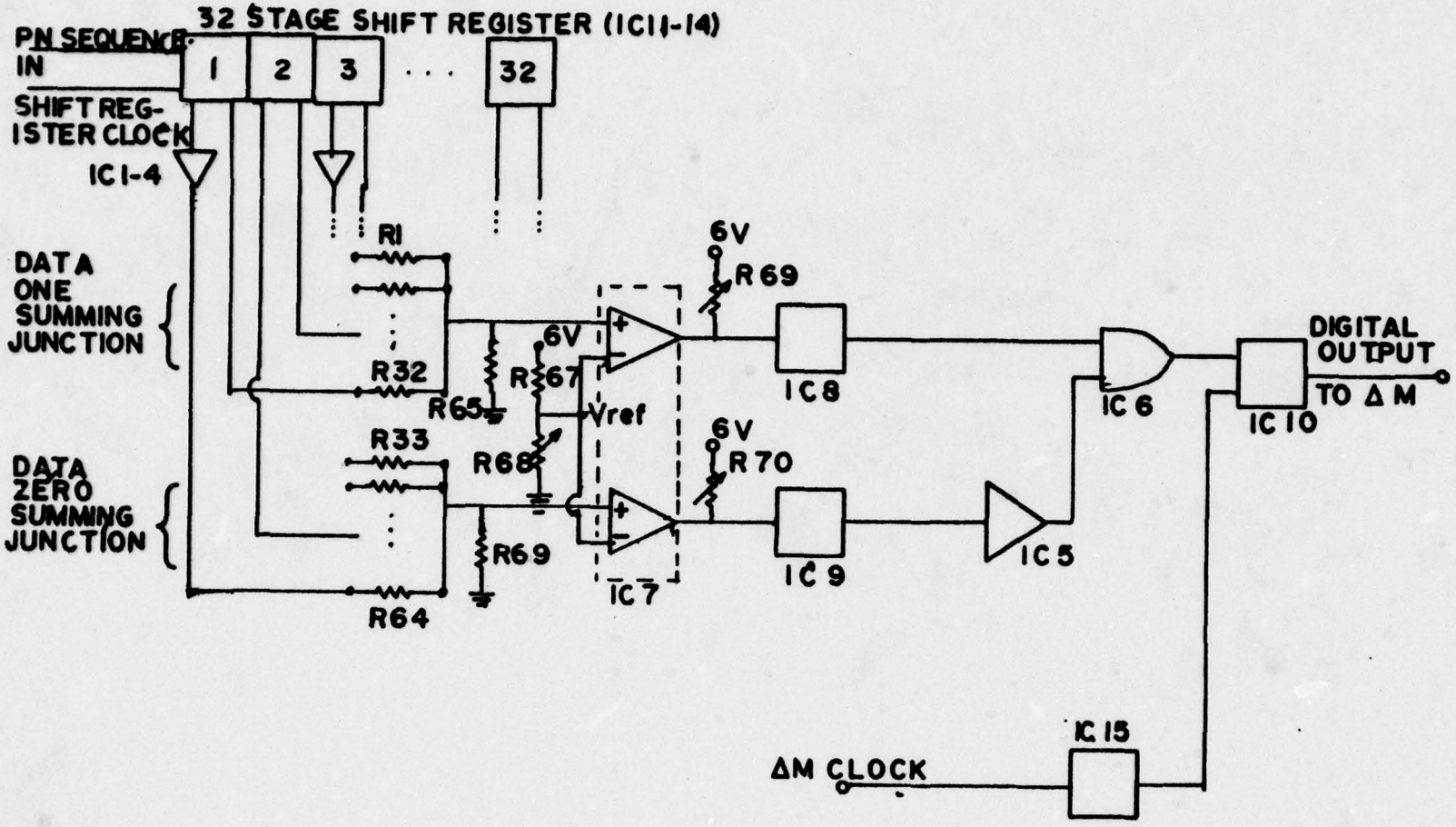


Figure 55. Schematic diagram of the digital matched filter

Component List for Digital Matched Filter Schematic

R1 - R64 - 200 K

R65,R66 - 100K

R67 - 75K

R68 - 100 K POT

R69,R70 - 10K POT

IC1-IC5 - DM 7404 (Inverter)

IC6 - DM 7408 - (AND-gate)

IC7 - LM 319 (Dual Comparator)

IC8,IC9,IC15 - LM 74121 (Monostable Multivibrator)

IC10 - DM 7474 (D-Flip Flop)

IC11-IC14 - DM 74164 (Shift Register)

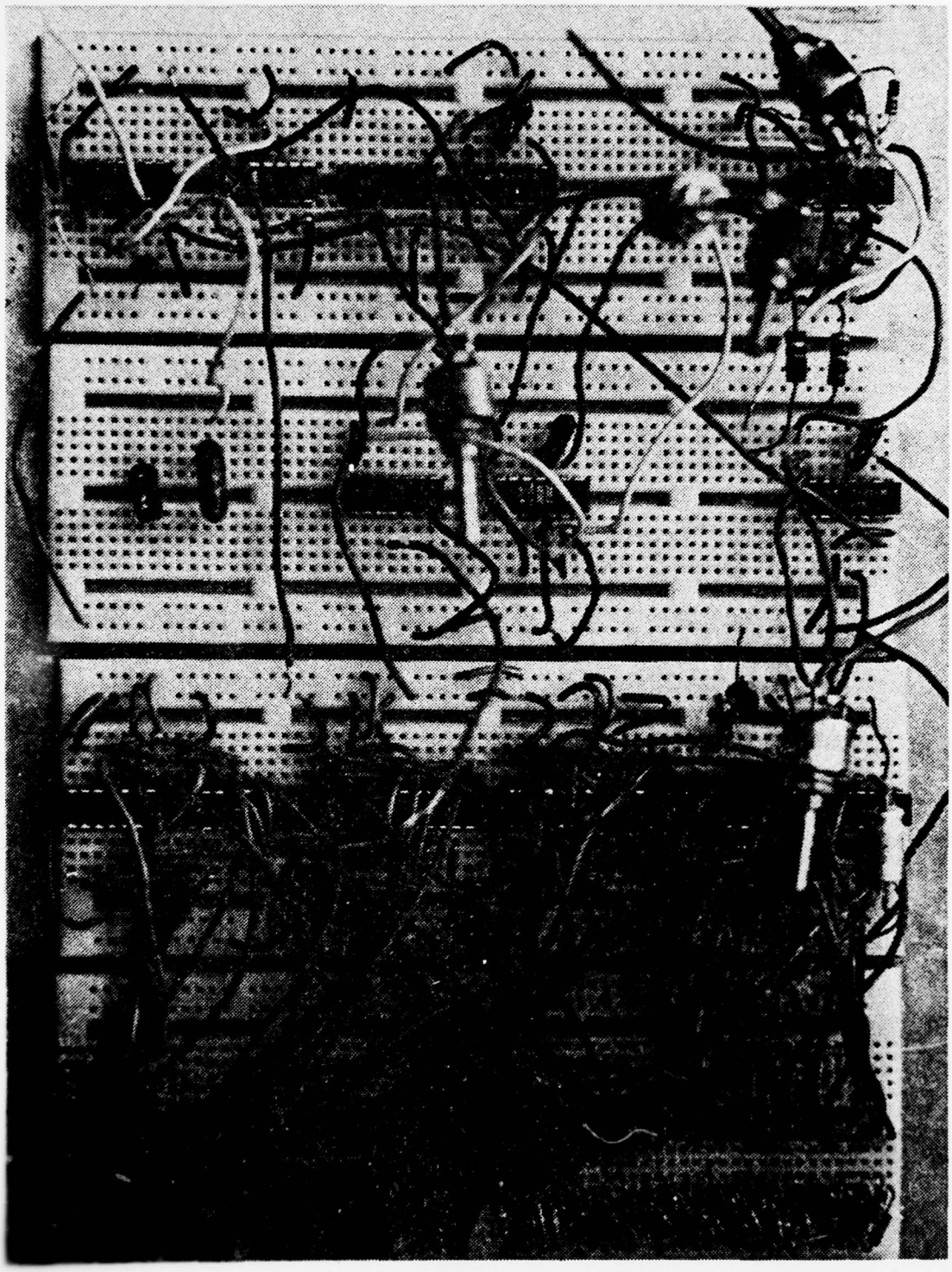


Figure 56. Bread boarded digital matched filter

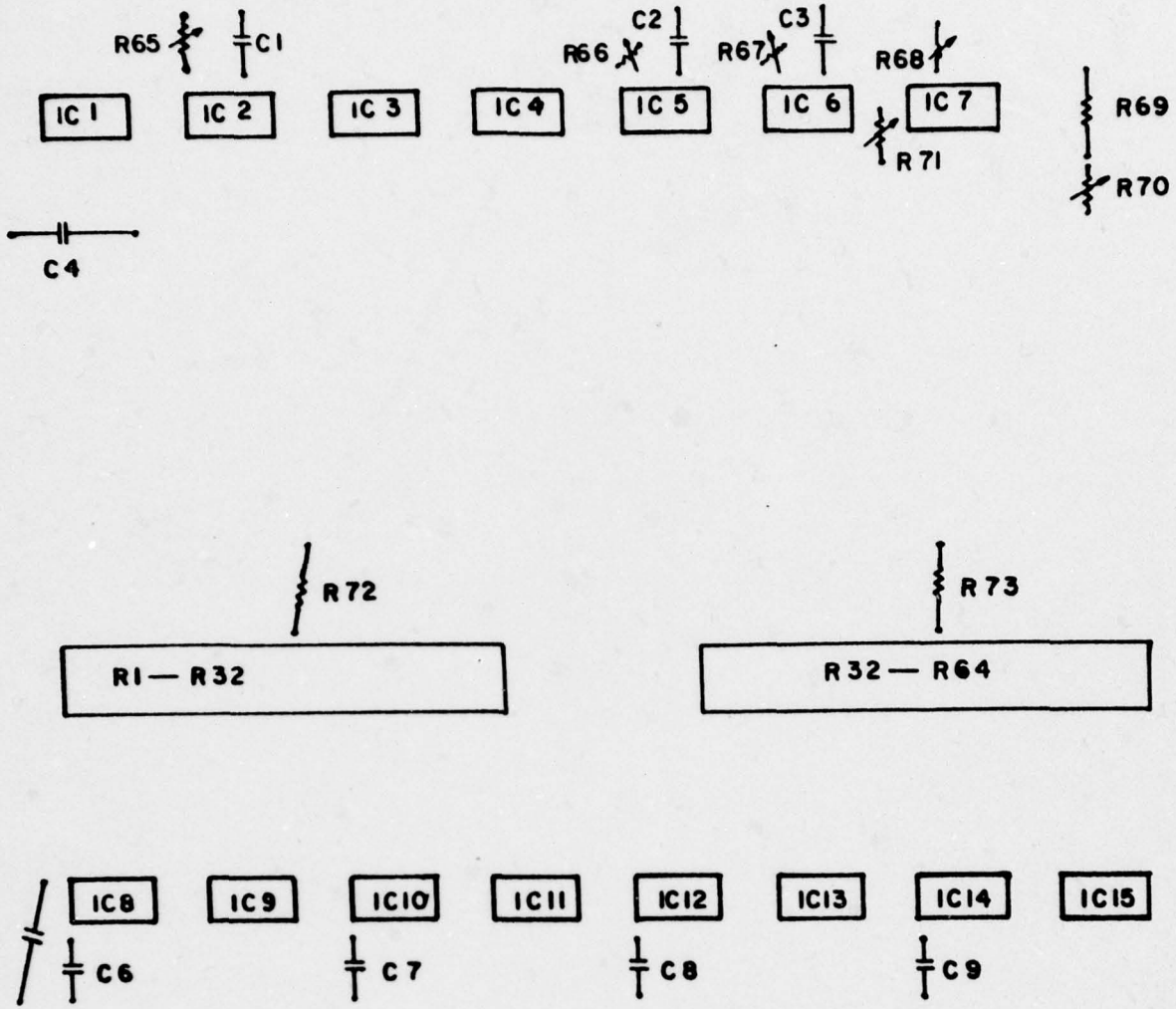


Figure 57. Component layout for digital matched filter PC board

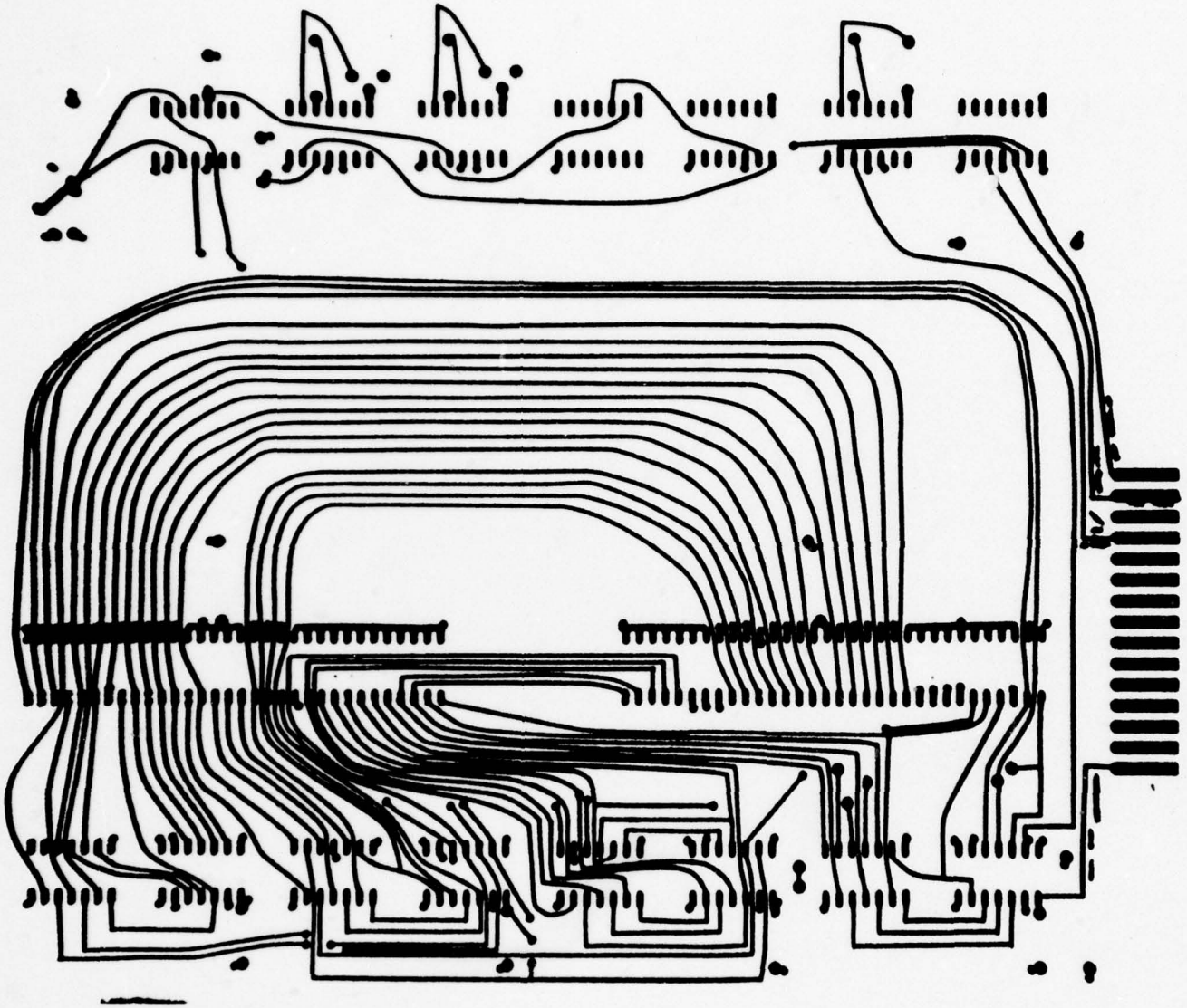


Figure 58. Digital matched filter PC foil pattern, bottom

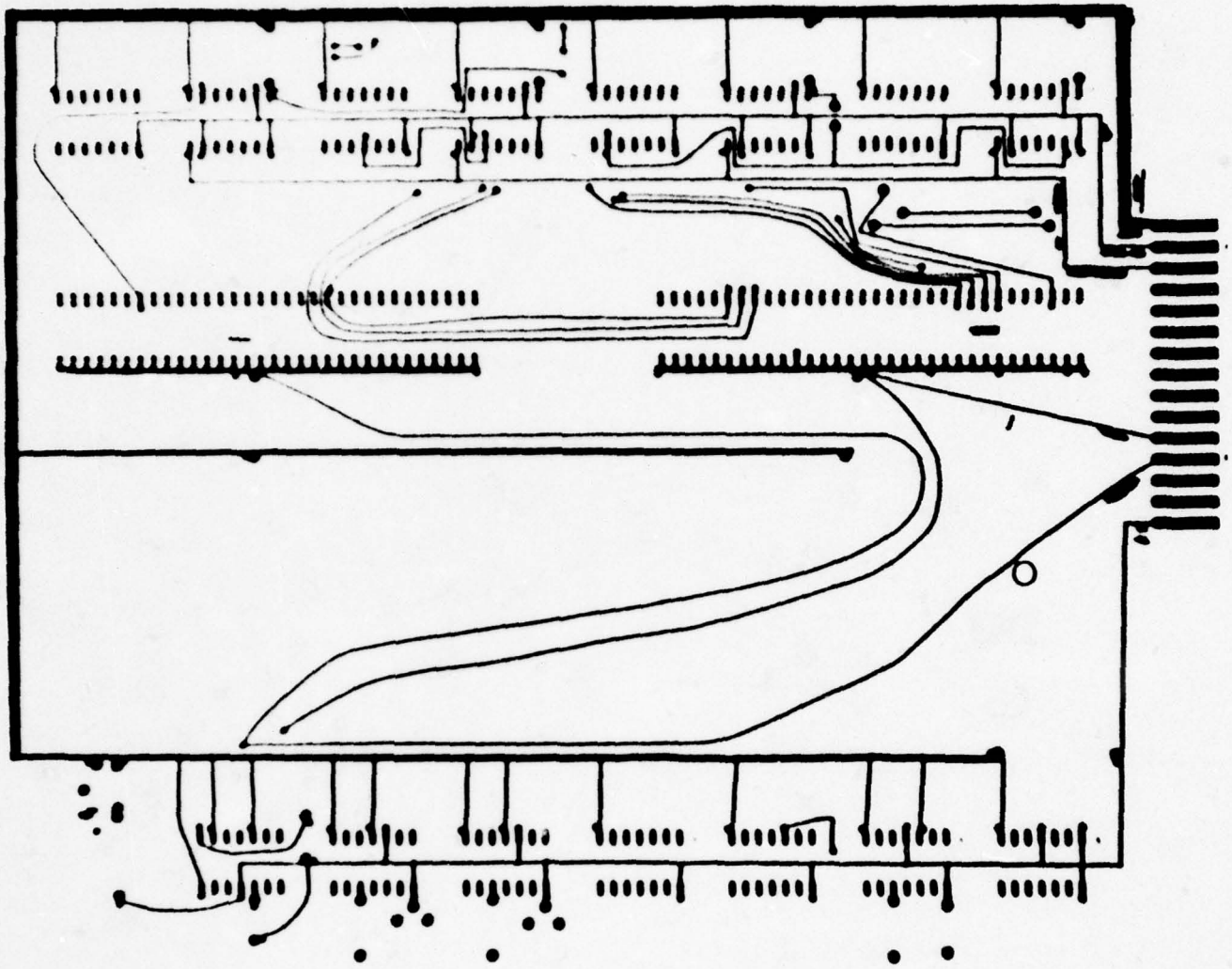


Figure 59. Digital matched filter PC foil pattern, top

Component List for DMF PC Board

R1-R64 - 200K

R65,R68,R71 - 10 K POT

R66,R67 - 50 K POT

R69,R72,R73 - 100K

R70 - 100 K POT

C1-C3 - 0.001 μ

C4,C5 - 5 μ

C6-C9 - 0.003 μ

IC1 - DM 7474 (D-Flip Flop)

IC2,IC5,IC6 - DM 74121 (Monostable Multivibrator)

IC3 - DM 7408 (AND-gate)

IC4,IC9,IC11,IC13,IC15 - DM 7404 (Inverter)

IC7 - LM 319 (Dual Comparator)

IC8,IC10,IC12,IC14 - DM 74164 (Shift Register)

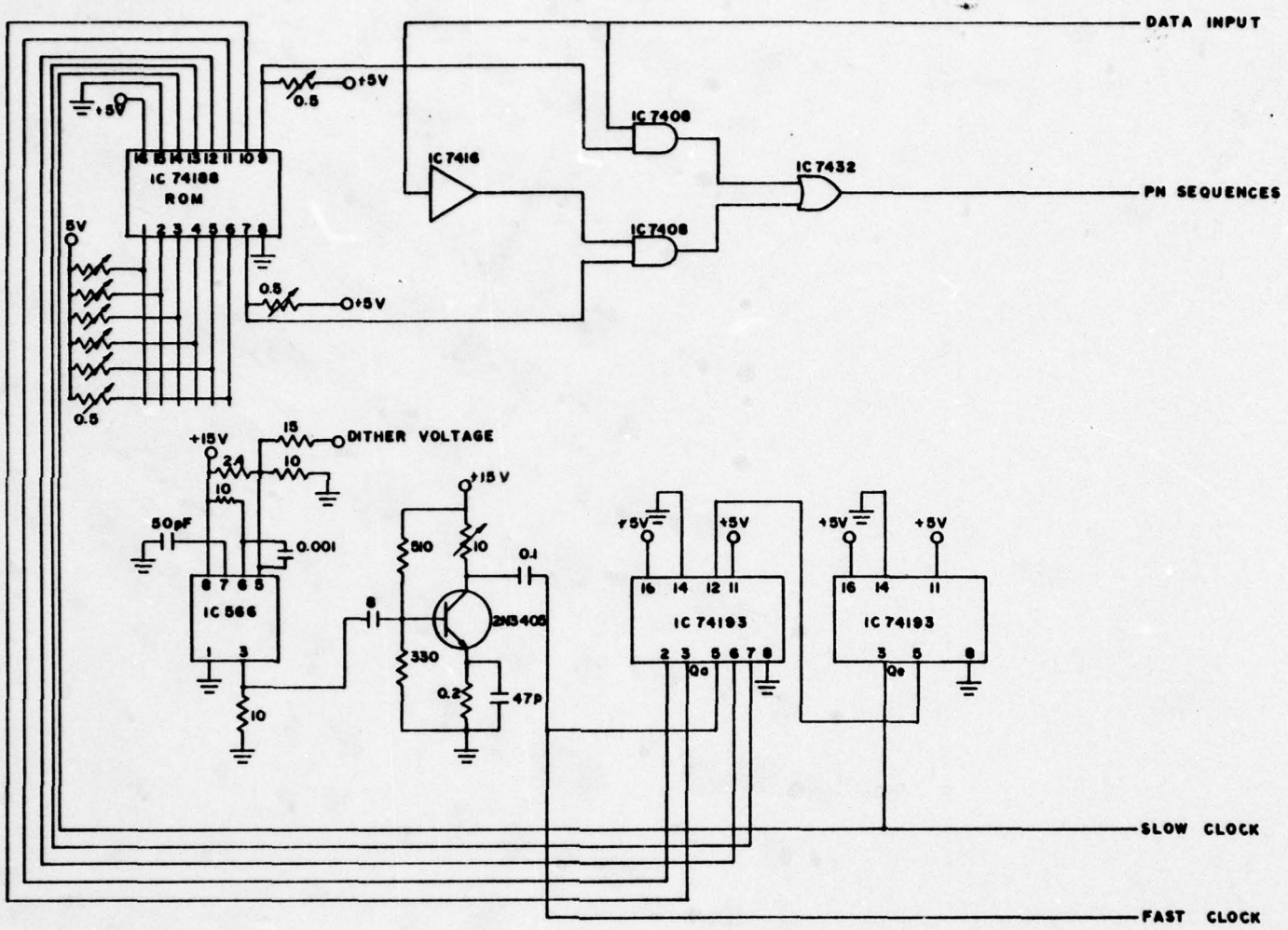


Figure 60. Schematic diagram of the data spreading circuitry

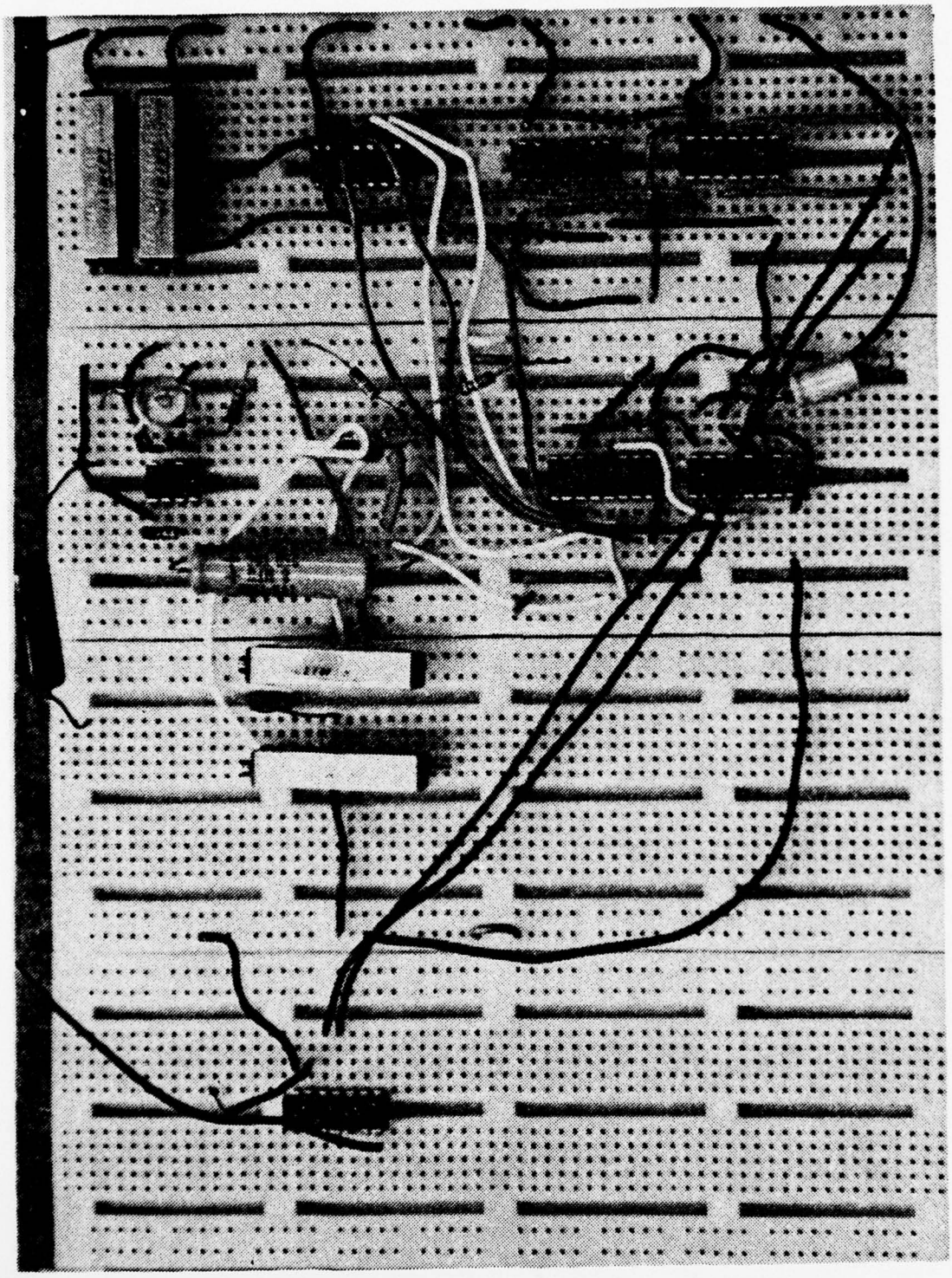


Figure 61. Bread boarded spreading circuitry

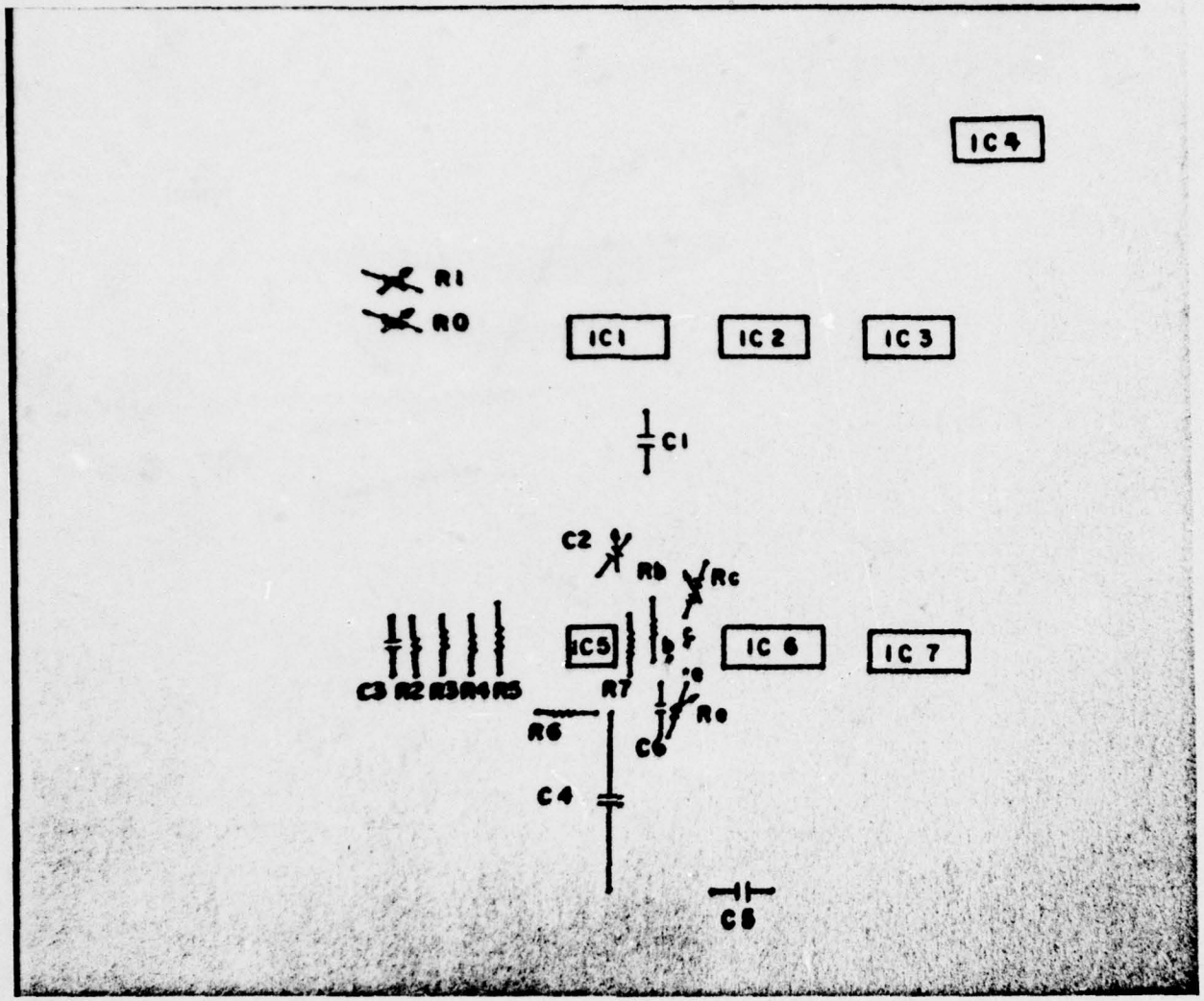


Figure 62. Component layout for spreading circuitry PC board

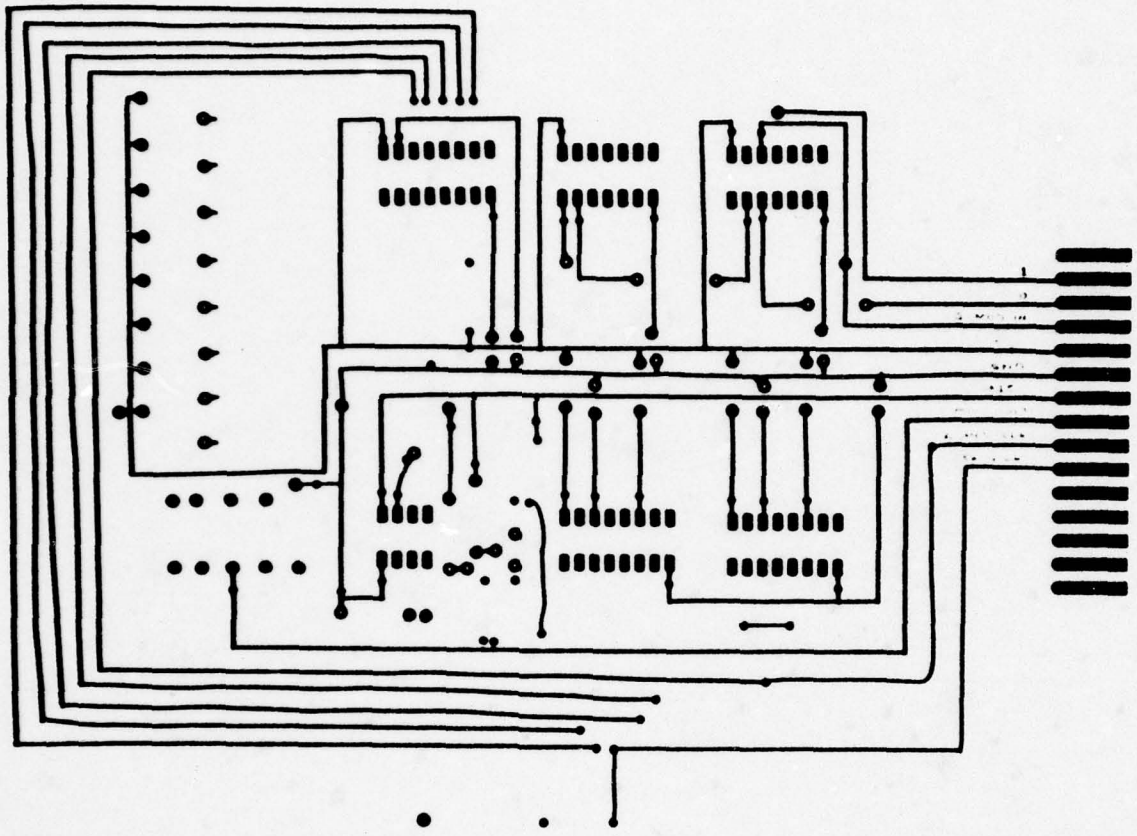


Figure 63. Spreading circuitry PC foil pattern, top

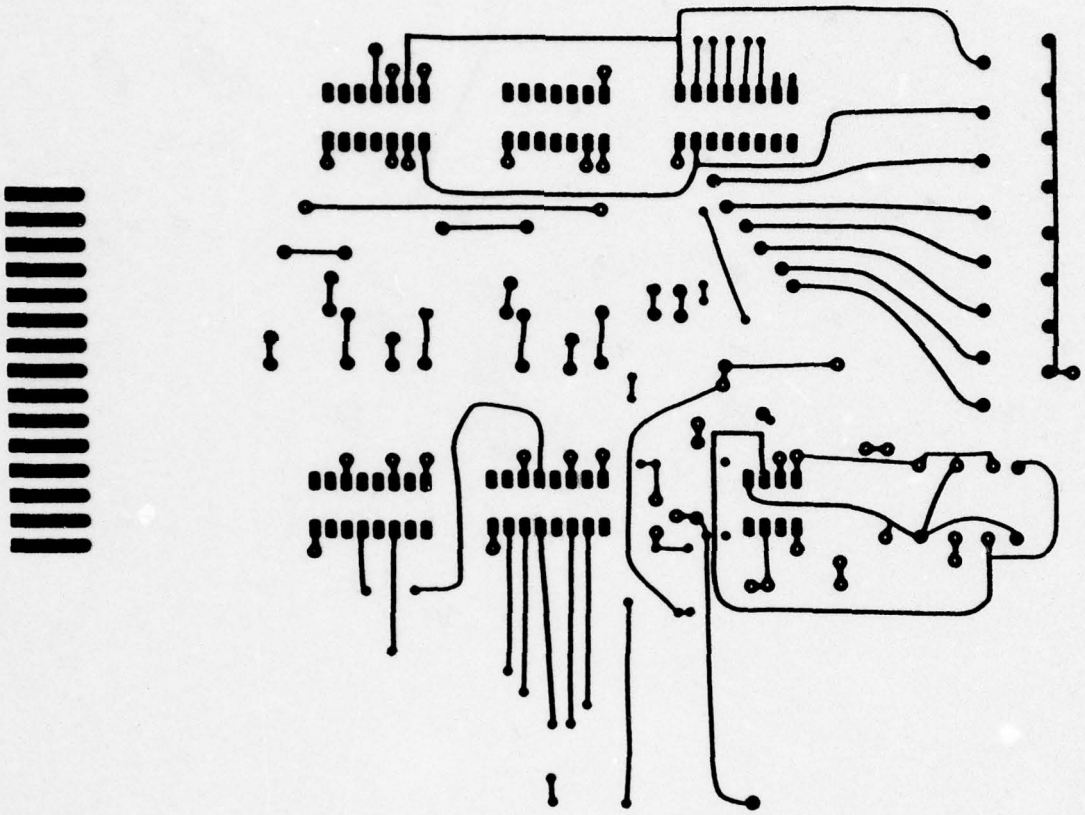


Figure 64. Spreading circuitry PC foil pattern, bottom

Component List for Sequence Generator PC Board

R0,R1,Rc,Re - 10 K POT

R2,R5,R6 - 10 K

R3 - 1.5 K

R4 - 2.4 K

R7 - 330 K

Rb - 510 K

C1 - 0.47 μ

C2 - 50 p variable capacitor

C3 - 0.001 μ

C4 - 8 μ

C5 - 0.1 μ

C6 - 47p

IC1 - SN 74188 (ROM)

IC2 - DM 7416 (Inverter)

IC3 - DM 7408 (AND-gate)

IC4 - DM 7432 (OR-gate)

IC5 - LM 566 (VCO)

IC6,IC7 - DM 74193 (Binary Counter)

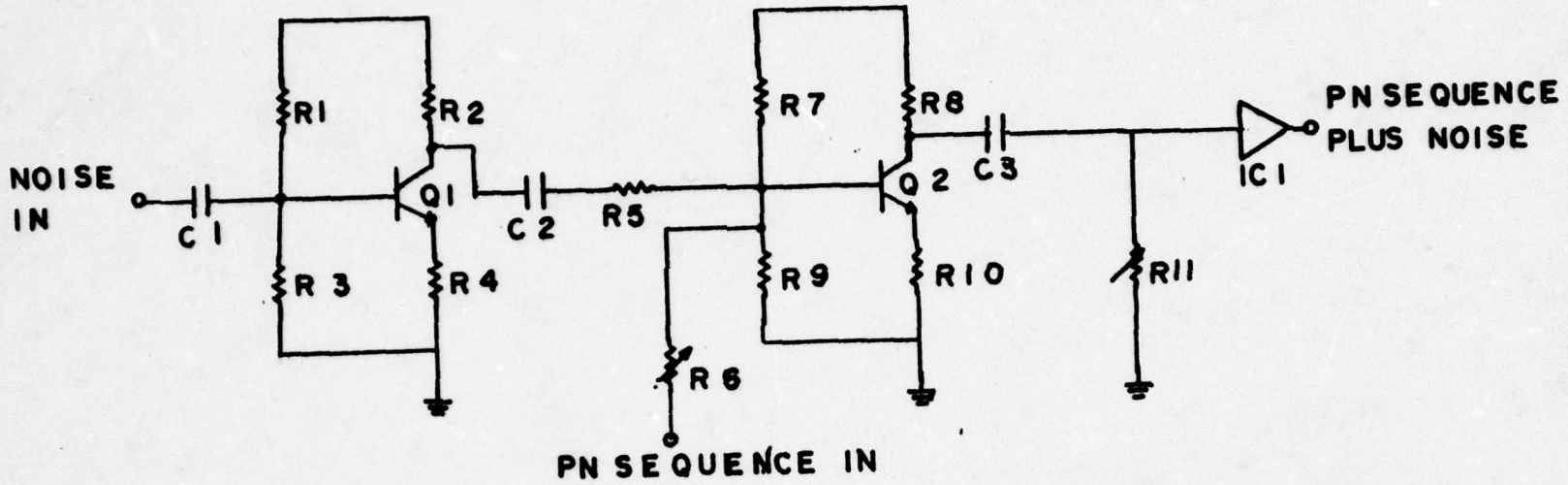


Figure 65. Noise amplifier and noise plus PN sequence summer

Component List for Noise Amplifier and Summer

R1,R7 - 510 K

R2,R8 - 1.8K

R3,R9 - 330 K

R4,R10 - 200 Ohms

R5 - 10 K

R6 - 1 M POT

R11 - 10 K POT

C1 - 8 μ

C2,C3 - 0.47μ

Q1,Q2 - 2N3405

IC1 - DM 7404 (Inverter)

APPENDIX B

LOW PASS FILTER DESIGN

The analog output of the ΔM in the receiver's passes through a six-pole active low pass filter. It consists of three second-order stages. Each second order stage is of the voltage controlled voltage source (VCVS) or equal-component-value Sallen-Key type [Ref. 5]. The active device for each stage is a 741 operational amplifier.

The transfer function of the LPF (refer to figure 50, page 74) is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{k_1}{R_{11}C_{11}R_{12}C_{12}}}{s^2 + [\frac{1}{R_{12}C_{11}} + \frac{1}{R_{11}C_{11}} + (1-k_1)\frac{1}{R_{12}C_{12}}]s + \frac{1}{R_{11}C_{11}R_{12}C_{12}}} \cdot$$

$$\frac{\frac{k_2}{R_{21}C_{21}R_{22}C_{22}}}{s^2 + [\frac{1}{R_{22}C_{21}} + \frac{1}{R_{21}C_{21}} + (1-k_2)\frac{1}{R_{22}C_{22}}]s + \frac{1}{R_{21}C_{21}R_{22}C_{22}}} \cdot$$

$$\frac{\frac{k_3}{R_{31}C_{31}R_{33}C_{33}}}{s^2 + [\frac{1}{R_{32}C_{31}} + \frac{1}{R_{31}C_{31}} + (1-k_3)\frac{1}{R_{32}C_{32}}]s + \frac{1}{R_{31}C_{31}R_{32}C_{33}}}$$

where k_1, k_2, k_3 are the gains of the corresponding stages. In a Sallen-Key circuit the gain is given by

$$k_i = 1 + \frac{R_{i4}}{R_{i3}} \cdot$$

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