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RELIABILITY STUDY OF HIGH EFFICIENCY GAAS IMPATT DEVICES.(U)
JAN 79 J L HEATON F30602-76-C-0409

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Final Technical Report
January 1979

RELIABILITY STUDY OF HIGH EFFICIENCY GaAs IMPATT DEVICES

Microwave Associates, Incorporated

Dr. John L. Heaton

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The reliability of low-high-low profile gallium arsenide IMPATT diodes has been studied. The devices were fabricated from vapor phase grown epitaxial gallium arsenide using sputtered platinum Schottky junctions and plated heat sink construction. Various screening methods have been evaluated for use in burn-in, and 75°C case DC burn-in at rated power dissipation selected as the best compromise. Long-term operation tests have established a minimum MTBF at 90% confidence of 41,000 hours. RF storage step stress tests have revealed a potential failure mechanism involving separation of the metallization layers.

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An improved metallization system has been established eliminating this mechanism. Various additional tests have demonstrated the immunity of these IMPATTs to damage from on-off switching transients, load mismatch, and bias voltage transients.

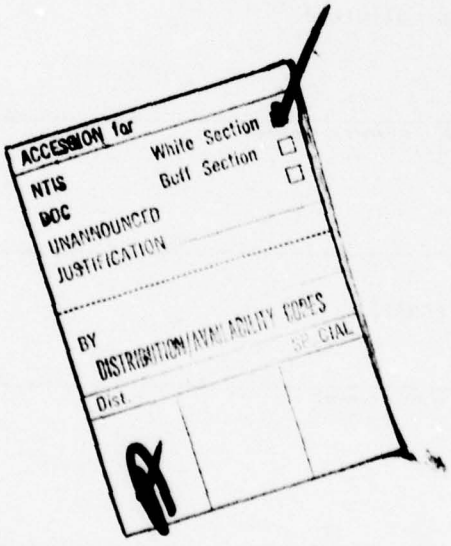


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EVALUATION

This report describes a study of the reliability of high efficiency gallium arsenide IMPATT diodes. From the results of the study it can be concluded that properly screened diodes in a good circuit are capable of reliable performance. A major cause of failure in the study was due to separation of metallization layers and this limited the information from high temperature accelerated testing. The problem was corrected and was shown by test that the design changes were effective. No changes were observed in the Schottky contact or doping profile during the accelerated tests. This work supports the objectives of TPO-5, "C^3 Systems Availability," and the associated project 2338, "Assurance Technology for Electronics." These show as an objective that failure mechanism studies are required on gallium arsenide devices such as IMPATT diodes. The results of this study will be used in the reliability prediction for these types of devices in MIL-HDBK-217, "Reliability Prediction of Electronic Equipment," and in reliability specifications for these devices. Additional effort is planned to investigate the effects of high power pulsed operation of GaAs IMPATT devices.



JOHN F. CARROLL
Project Engineer

1.0 INTRODUCTION

1.1 Program Summary

The concept of solid state reliability is of extreme importance to systems designers, particularly in the field of telecommunications. Because of the limited life of traveling-wave tubes, solid state replacements of assumed superior life expectancy are being sought for use as transmitter output stages, particularly in remote locations. High efficiency design, Read profile gallium arsenide IMPATTs presently represent the highest power output commercially available solid state microwave sources, and with conversion efficiencies in excess of 20%, are an attractive TWT replacement. However, before Read IMPATTs find extensive use in remote equipment or military systems where highest reliability is required, an assessment of the reliability of present devices is required. It was the purpose of this program to provide this needed reliability information.

The program was divided into four distinct phases as follows:

1) Early failure region screening where DC, AC, and RF burn-in as well as HTRB were examined for effectiveness in early failure region screening.

2) Accelerated stress testing where RF burn-in and high temperature storage step stress tests were carried out for MTTF (mean time to failure) determination.

3) Long-term testing where twenty (20) diodes were operated under worst case use conditions for in excess of 5000 hours for MTBF (mean time between failure) determination.

4) Special testing involving pulsed burn-out, switching transient, corosion resistance and tuning induced failure tests.

All devices tested were L-H-L (low-high-low) doping profile type platinum Schottky barrier units of Microwave Associates' manufacture.

1.2 General Theory of Failure Analysis

The typical failure rate versus time curve for a component population is composed of three regions (Figure 1-1). These regions are the infant mortality or freak failure region, the useful life region and wearout failure region. This type of behavior is typical for all semiconductor devices. An additional failure mode can occur during the useful life and is catastrophic in nature. This failure mode is not related to the inherent processes involved in the device manufacture but to the effects of transient phenomena on a high field device. These failures are a result of diode-circuit interactions and cannot be studied by the conventional approaches used for reliability studies.

For the typical failure rate-time distribution for semiconductor devices (Figure 1-1), it is instructive to inquire as to what is to be accomplished in reliability testing and procedures developed for the different areas of the failure rate curve. The freak failure or infant mortality region is characterized by a failure rate that decreases with time as faulty devices are removed from the population. It is the purpose of this period to remove sufficient defective devices to reduce the failure rate to an acceptable level during the useful-life region. The procedures which are utilized must therefore enhance the infant mortality rate so as to minimize the useful-life failure rate by eliminating any defective devices during this infant mortality period.

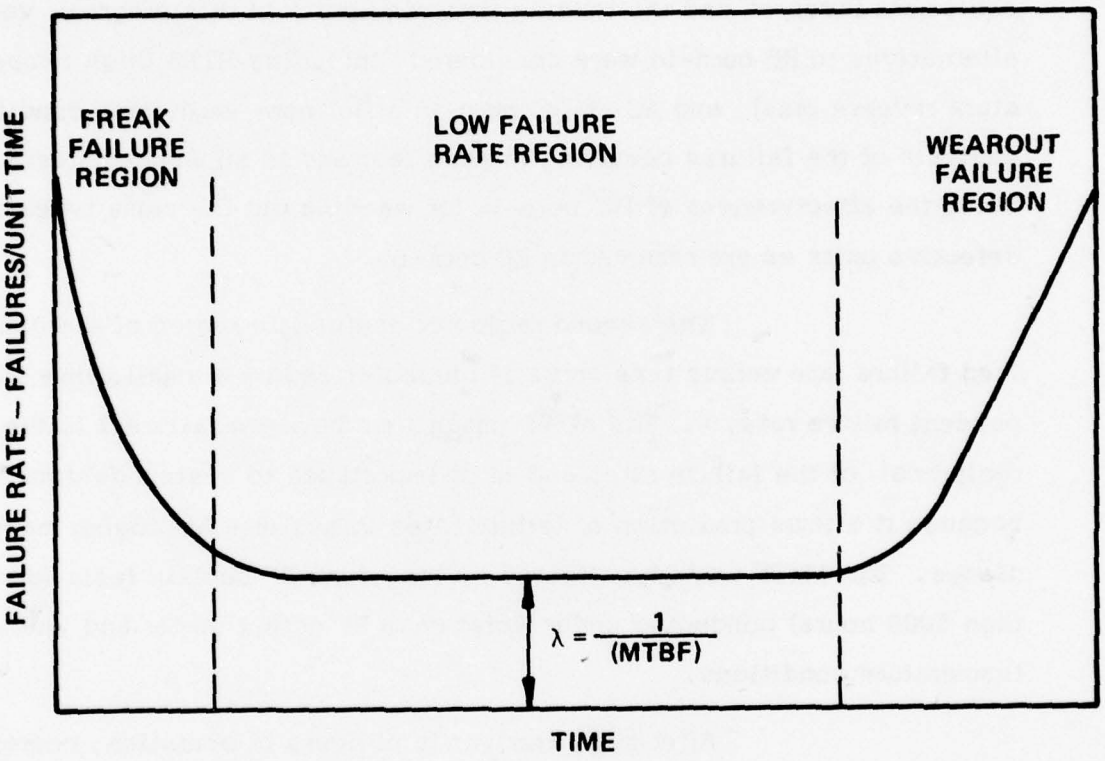


FIGURE 1-1. GENERALIZED FAILURE RATE VERSUS TIME CHARACTERISTICS

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Some sort of burn-in screening process is normally used to remove weak devices from the population, and reduce the failure rate to an acceptable level. Generally, operation of devices under increased stress conditions (RF burn-in) is employed as a screening test. However, as a production technique, RF burn-in is costly because of the equipment involved and the loading time required. In this program, various alternatives to RF burn-in were considered, including HTRB (high temperature reverse bias), and AC or DC burn-in under non-oscillating conditions. Analysis of the failures occurring in each test and in subsequent tests indicated the effectiveness of DC burn-in for weeding out the same types of defective units as are removed in RF burn-in.

The second region or useful-life region of the generalized failure rate versus time curve is characterized by a small, time independent failure rate, λ. The MTBF (mean time between failures) is the reciprocal of the failure rate, and is of importance to system designers because it allows prediction of failure rates in systems employing many diodes. The MTBF was investigated by long-term RF burn-in tests (greater than 5000 hours) conducted under worst case RF output power and junction temperature conditions.

After many thousands of hours of operation, components enter the wearout failure region of the failure rate versus time characteristics, where the failure rate is no longer constant but begins to increase with time. This region is normally investigated by using accelerated aging life tests of the step stress or constant stress type.

1.2.1 MTBF Determination

Diode MTBF determination is concerned with measurement of the failure rate of units surviving early failure screening. This portion of the failure rate versus time curve is characterized by a constant failure rate, λ, where:

$$\text{MTBF} = 1 / \lambda \tag{1}$$

The rate of failure is time independent in this region, leading to an exponential probability of survival given by [1] .

$$P_s = e^{-\lambda t} \tag{2}$$

where

P_s = probability of component will survive to time, t, (hours)

λ = the failure rate (failures per hour)

Causes of failure in this region are not due to wearout mechanisms such as contact metallization movement, but are of the "freak" variety, such as loosening of the contact wire or failure of the chip bond. Such failures are most difficult to identify because of the normally low observed failure rates.

MTBF is determined by operating a group of units under normal conditions and measuring the observed failure rate. Then

$$\text{MTBF} = \frac{\text{Number of unit hours of operation}}{\text{Number of failures}} \tag{3}$$

The lower confidence limit estimate for the MTBF is computed as follows:

$$L = \frac{2R\bar{m}}{\chi^2_{2R,\,(\alpha/2)}} \qquad (4)$$

where

L = lowest value that the MTBF could assume with confidence level α

R = number of devices which have failed

α = the confidence level

$\bar{m}$ = estimate of the MTBF from Equation (3)

$\chi^2_{2R,(\alpha/2)}$ = value of Chi square statistic for 2R degrees of freedom, and probability level $\alpha/2$

It should be noted that those failure mechanisms responsible for determining the MTBF may not be accelerated by temperature increase. Hence to be completely valid, MTBF measurements are normally conducted under normal operation conditions, and may require several years of test time to produce a significant number of failures. Only in tests involving very large samples can meaningful MTBF data be developed in short times.

1.2.2 Wearout Failure

In the wearout failure region of the failure rate versus time curve, the failure rate is no longer constant, but begins to increase as failure due to long-term degradation mechanisms become more likely than the random failures of the middle-life region.

The average time to wearout failure is often described by the Eyring-Arrhenius rate law:

$$t_m = \exp\left\{\left[\frac{\Delta H}{k T} + C\right]\right\} \quad (5)$$

or

$$\log t_m = \frac{\Delta H}{k T} + C$$

where

ΔH = the activation energy for the process

k = Boltzmann's constant

C = design constant factor

T = device active region temperature, ^{o}K

The factor, C, reflects variation from unit to unit in device manufacture or the effect of stress other than temperature. If, for a large number of units, temperature is held constant, and C is assumed to be normally distributed among units, then the time to failure is log normally distributed. Such a condition has been found to empirically describe most semiconductor failure distributions [2, 3].

In order to determine the activation energy for a process, t_m must be determined experimentally for several different average active region temperatures. This technique is the so called "constant stress" method, (see Figure 1-2), and involves operating a set of devices at a fixed temperature and recording the time to failure for each unit. The test must be repeated for at least two stress levels. Alternatively, the step stress method may be used where the devices are subjected to stress

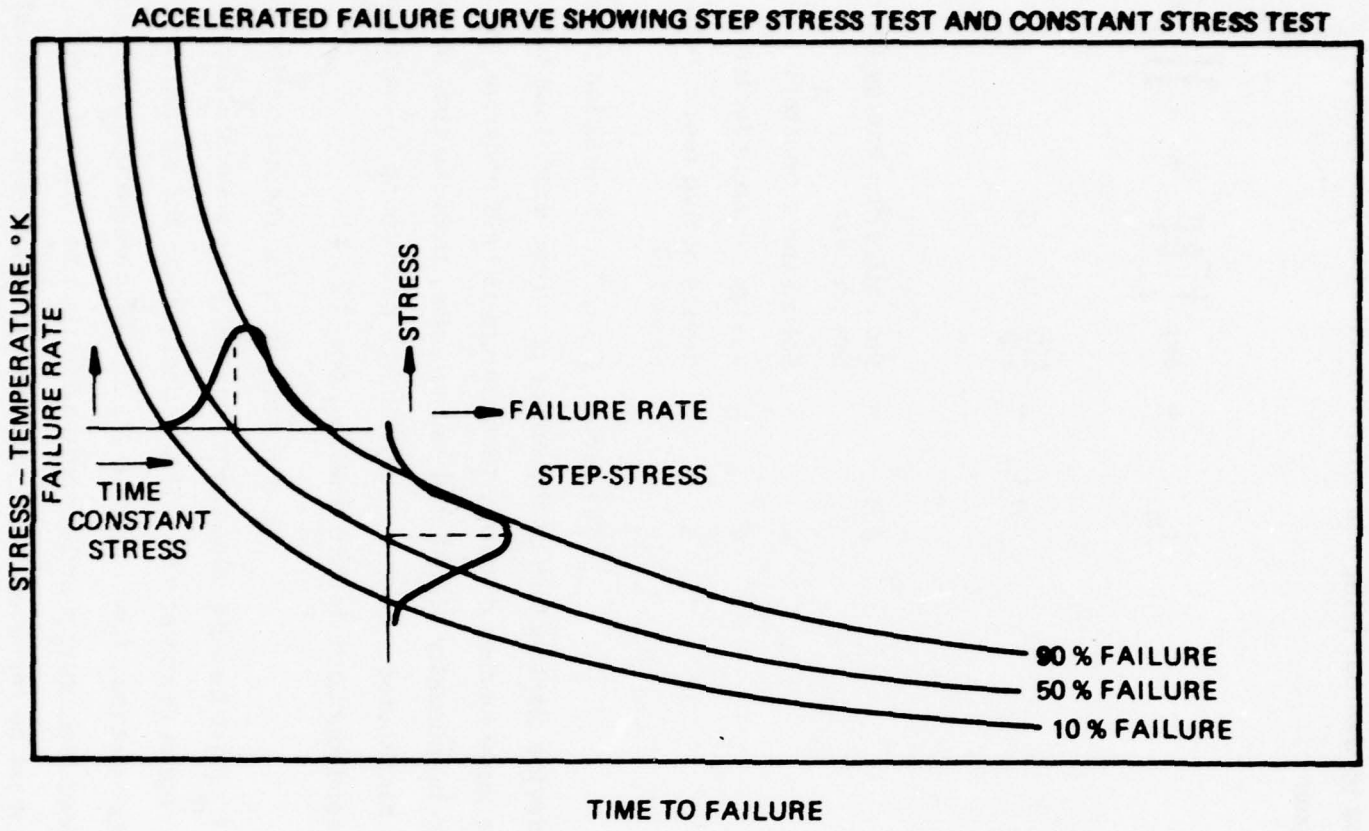


FIGURE 1-2. ACCELERATED FAILURE RATE CURVE SHOWING STEP STRESS AND CONSTANT STRESS TESTS.

which is repeatedly increased in constant increments after a fixed time interval, until all devices fail. Here, the test is repeated using time intervals of at least two different lengths. All devices failing within a given time interval are considered to have failed at the end of the interval in question. As shown in Figure 1-2, either the constant stress or step-stress technique may be used to generate the Arrhenius accelerated failure curve.

One danger associated with the use of the Arrhenius equation concerns the existence of two or more failure mechanisms. In some cases, certain mechanisms such as melting of contact metallization may be effective only at elevated temperature. Attempts to accelerate those mechanisms responsible for wearout failure under normal conditions may initiate failure due to a second mechanism which completely masks operation of the primary cause of failure. In order to eliminate this problem, several quick step stress tests can be run initially in order to find the maximum usable temperature before excitation of additional failure mechanisms.

1.3 Long-Term Failure Mechanisms in GaAs Read IMPATTs

In the case of platinum Schottky Read IMPATT diodes, penetration of platinum Schottky barrier metallization into the gallium arsenide active region has been cited as a primary cause of long-term diode degradation [4, 5]. Because such motion in effect changes the doping peak location and height, dramatic changes in diode operating performance are expected. If the platinum layer is not excessively thick (less than 200 Å), reaction will stop before much change in diode performance has occurred due to the exhaustion of unreacted platinum.

In the case of thin platinum layers (a few hundred angstroms), a second degradation mechanism can occur. This mechanism involves penetration of gold from the final metallization layer through the

platinum by diffusion or surface migration. Such penetration leads to acceptor formation and net donor density reduction in the heavily doped spike region of L-H-L IMPATTs. Calviello, et al [6] have reported that tantalum forms an effective diffusion barrier for gold and is stable to 400°C on gallium arsenide. It was feared that some gold diffusion could still occur in pure tantalum films via the grain boundary interfaces, and that a further measure of protection could be obtained by incorporating nitrogen at the tantalum grain boundaries, preventing gold diffusion via this mechanism. Accordingly, the devices investigated in this program used two tantalum gold diffusion barrier layers; the second was reactively sputtered in a nitrogen argon atmosphere.

2.0 DEVICE FABRICATION AND TEST

2.1 Device Fabrication

The devices investigated in this program were Schottky barrier junction L-H-L doping profile gallium arsenide IMPATT diodes. The required epitaxial gallium arsenide layers were prepared using the $AsCl_3$, G_a, H_2 vapor phases synthesis system, with H_2S/H_2 doping gas. The L-H-L doping profile (see Figure 2-1) was used, with a heavily doped peak region of maximum doping 2.5×10^{17} carries/cc, width at half height of 0.07 microns, and peak location of 0.35 to 0.45 microns from the surface. The drift region was doped at 5.5×10^{15} carriers/cc and was 5.5 microns in thickness.

A Schottky-barrier was formed by sputtering a 200 Å layer of platinum on the epitaxial surface and was followed by sequentially sputtered layers of tantalum (4000 Å) and gold (2000 Å). The last 2000 Å of tantalum was reactively sputtered in nitrogen-argon. A post sputtering sintering step was performed to produce complete reaction of the platinum with the gallium arsenide, preventing apparent motion of the junction during operation due to conversion of gallium arsenide to platinum arsenide. The tantalum layers form a gold diffusion barrier. Gold diffusion can occur along grain boundary interfaces in pure tantalum, but is inhibited if nitrogen is incorporated at the grain boundaries.

Chips (see Figure 2-2) were fabricated using a standard plated heat sink (PHS) process. Mesas of 10 mil diameter and 2 mils height resulted, on 25 mil square gold pads of 2.5 mil thickness. The chips were mounted in threaded stud (80 mil outside diameter ceramic) microwave diode packages using 80% gold, 20% tin eutectic solder preforms (285° melting point). The mesas were contacted by crossed 1/4 mil by 5 mil pure gold ribbons.

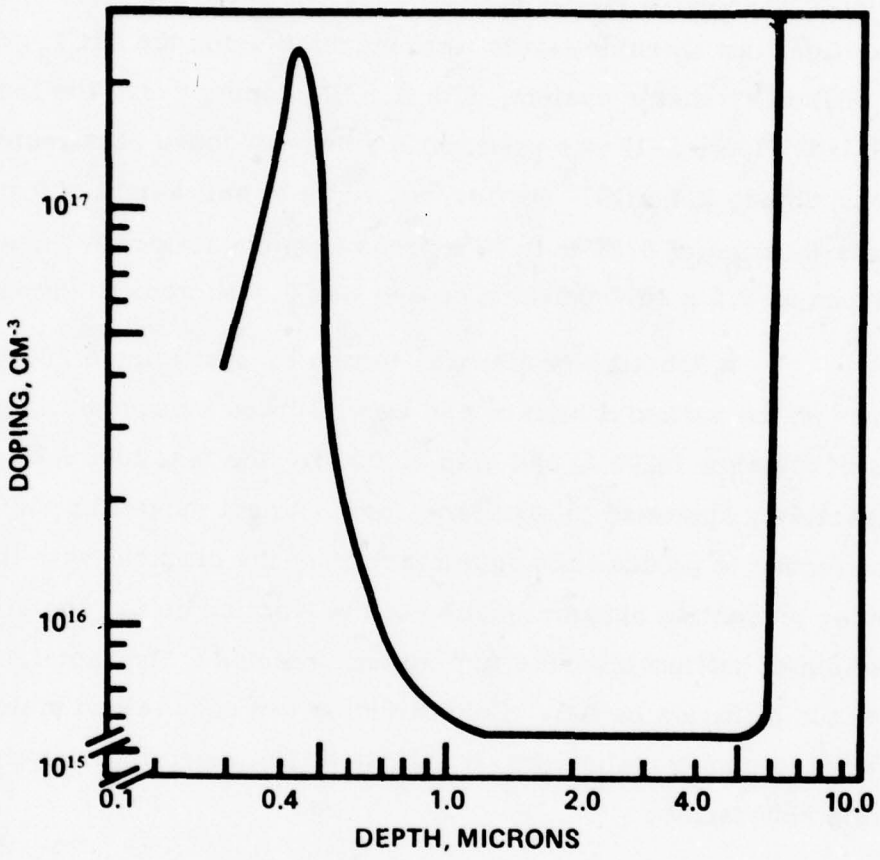


FIGURE 2-1. LHL IMPATT DOPING PROFILE

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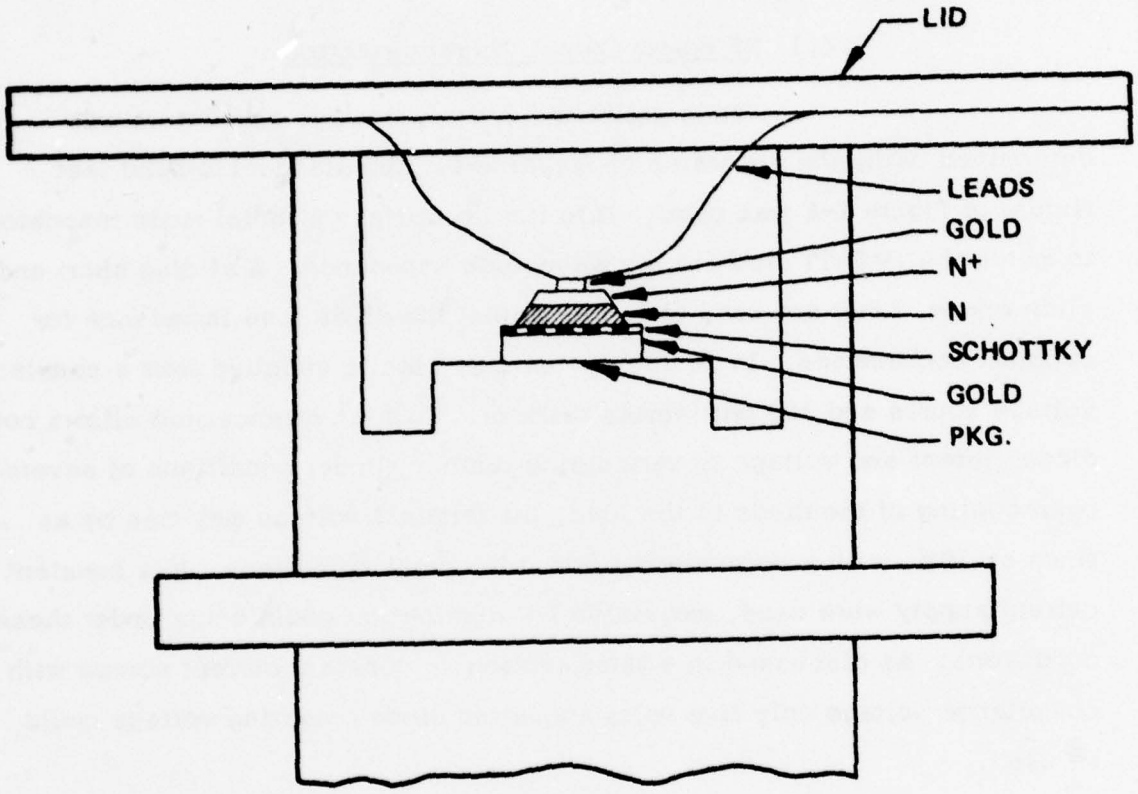


FIGURE 2-2. IMPATT DIODE MOUNTED IN PACKAGE

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Packaged devices were etched to capacitance specification (25% area reduction) using an electrolytic potassium hydroxide etch. Only the epitaxial layer is removed by this etch, producing a gap around the mesa circumference (etch gap). A cross sectional chip is shown in Figure 2-3.

2.2 Device Test

2.2.1 RF Power Output Characterization

Diode performance as microwave oscillators was determined using the apparatus of Figure 2-4. The standard X-band test fixture of Figure 2-5 was used. This fixture utilizes a radial mode resonator to match the IMPATT diode to the waveguide impedance. A sliding short and slide screw tuner are used to further adjust the diode load impedance for optimum performance. In device evaluation, bias is supplied from a constant voltage source and 100 ohm series resistor. Such an arrangement allows both diode current and voltage to vary during tuning. Under conditions of severe overcoupling of the diode to the load, the terminal voltage may rise by as much as 20%, with a corresponding drop in operating current. If a constant current supply were used, excessive DC dissipation could occur under these conditions. As discussed in a later section, a constant current source with compliance voltage only five volts above the diode operating voltage could be used.

2.3 Thermal Resistance Measurement

Device junction temperature under operation, T_J is usually expressed in terms of the device thermal resistance as follows:

$$T_J = T_C + \theta_J \left(P_{in} - P_{out} \right) \qquad (7)$$

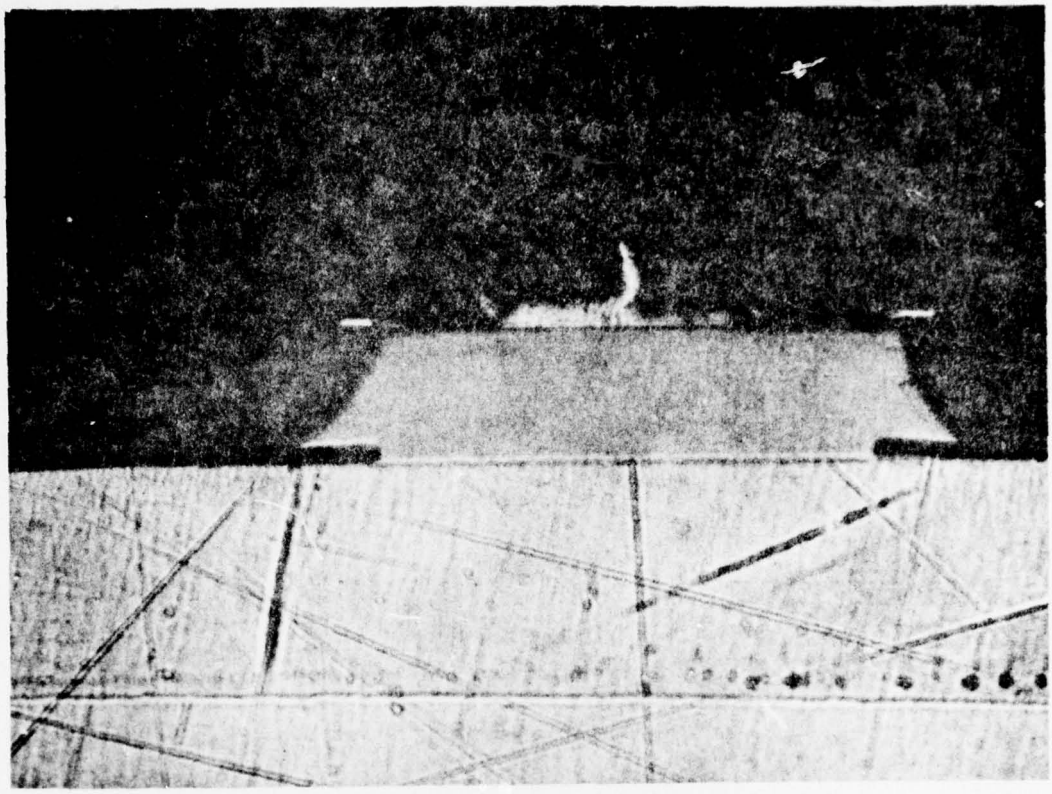


FIGURE 2-3. CROSS SECTION OF TYPICAL IMPATT CHIP SHOWING THE STRUCTURE FORMED BY IN PACKAGE ETCHING 200X

D-16493

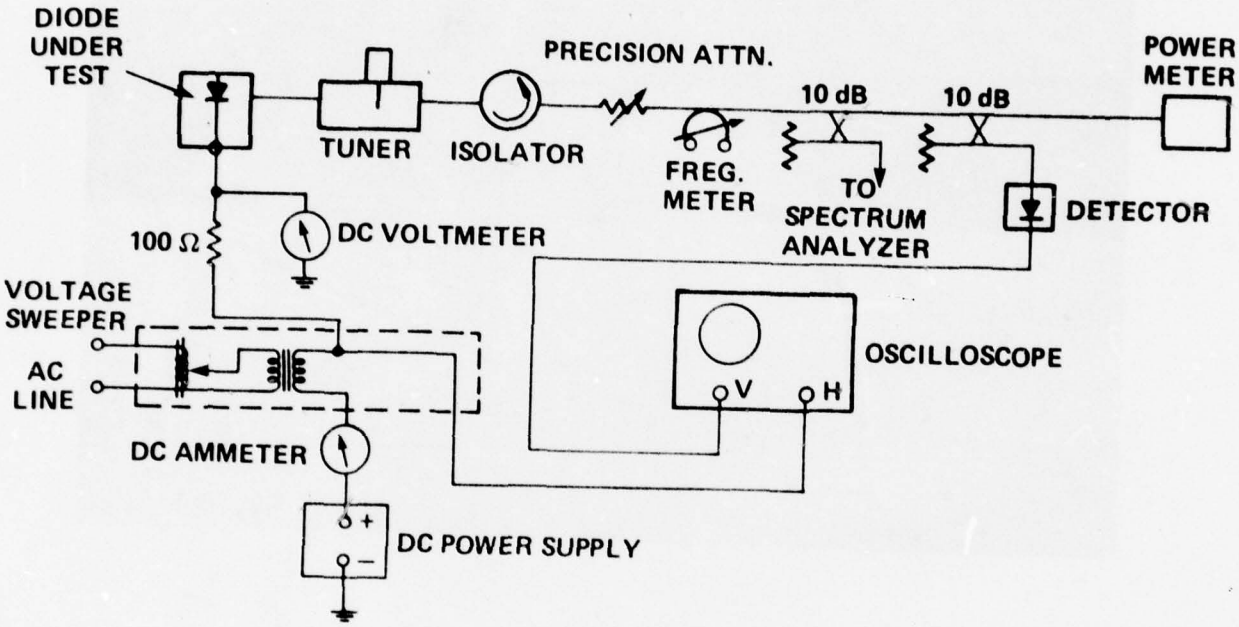


FIGURE 2-4. APPARATUS USED TO DETERMINE IMPATT DIODE DC AND rf PARAMETERS

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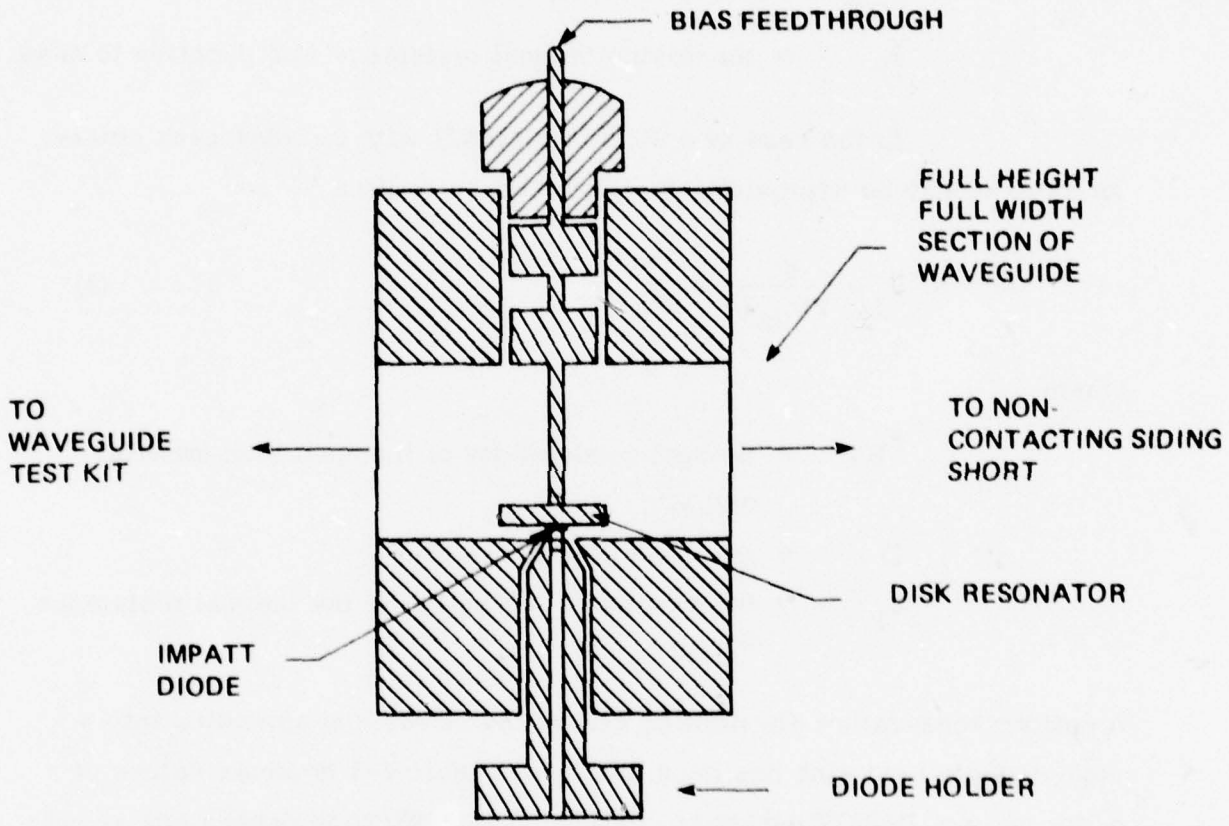


FIGURE 2-5. STANDARD X-BAND IMPATT DIODE TEST CAVITY

D-14015

where

T_C = the device case temperature, ^oC

T_J = the device junction temperature, ^oC

P_{in} = the DC input power to the device

P_{out} = the RF output power from the device

θ_J = the device thermal resistance from junction to case.

In the case of a Schottky IMPATT with circular mesa cross-section, θ_J may be approximately calculated as follows [6]:

$$\theta_J = \frac{2}{\pi K_{HS} D} + \theta_P \qquad (8)$$

where

K_{HS} = thermal conductivity of the heat sink material W/cm^oC

D = the mesa diameters, cm

θ_P = the package contribution to the thermal resistance, $^oC/W$

A uniform temperature distribution across the mesa, and spreading into a semi-infinite heat sink has been assumed. Table 2-1 presents values of θ_P for various IMPATT packages, estimated from package dimensions assuming one dimensional heat flow in cylindrical geometry [7]. Eq. (8) is plotted in Figure 2-6, including a package contribution of $2.1^oC/W$ (ODS 111 package). The thermal resistance as calculated from equation (8) represents an ideal minimum, since no provision has been made for non-ideal bonding.

Microwave Associates Package Style	Heat Sink Type	Ceramic OD mil	Ceramic Height mil	Pkg Thermal Resistance °C/W
30	0.062 in dia stud	80	61	3.2
111	3-48 threaded stud	80	30	2.0
118	3-48 threaded stud	50	19	3.2
138	3-48 threaded stud	30	12	2.8
141	3-48 threaded stud	124	45	0.3

TABLE 2-1

APPROXIMATE PACKAGE CONTRIBUTION TO IMPATT DIODE THERMAL RESISTANCE

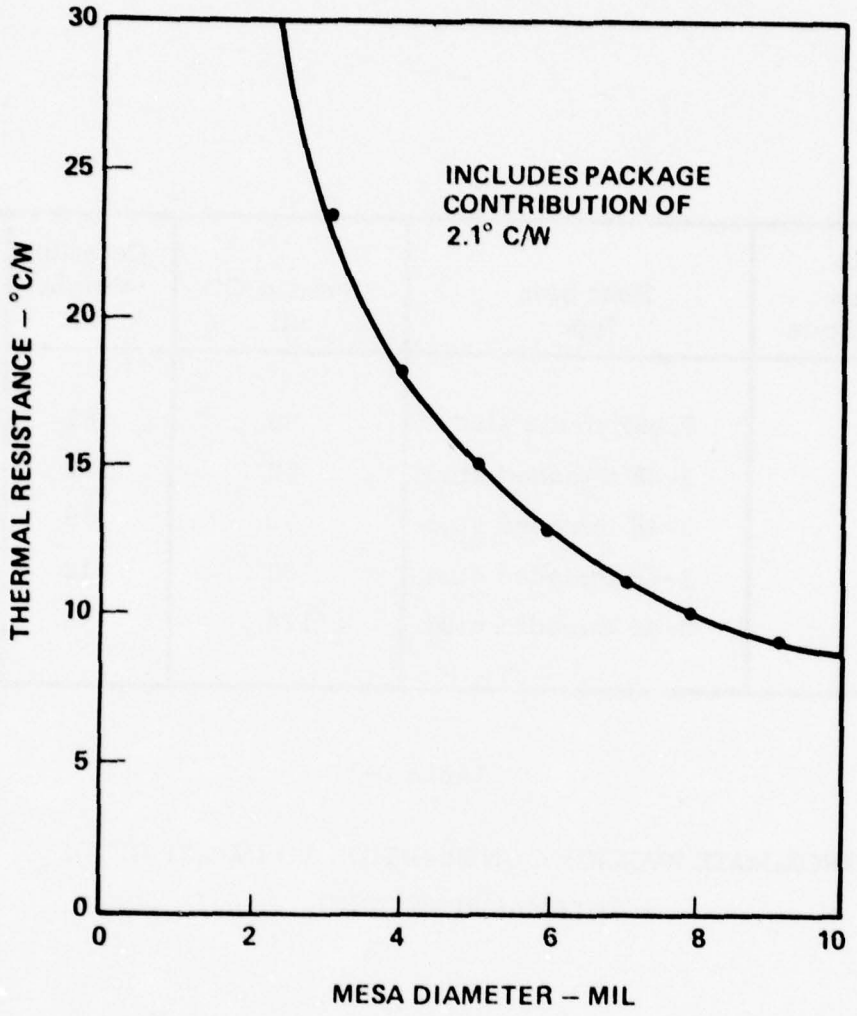


FIGURE 2-6. CALCULATED SCHOTTKY IMPATT THERMAL RESISTANCE (JUNCTION TO CASE) VERSUS MESA DIAMETER

D-14018

The thermal resistance measurement method used at Microwave Associates involves the temperature dependence of the breakdown voltage [8].

$$V_b (T_J) = K_T \ (T_j - T_C) \ + \ V_{bo} \tag{9}$$

where

T_J = junction temperature, ^oC

T_C = initial junction temperature (equal to case temperature), ^oC

V_{bo} = breakdown voltage at $T_J = T_C$

K_T = temperature coefficient of the breakdown voltage, $(V/^oC)$

The circuit of Figure 2-7 is used. The diode under test is placed in a test fixture and biased at normal operating power input. Oscillations are suppressed by use of graphite load material in the diode mount. A negative going pulse of 1 microsecond duration is introduced across the diode and the amplitude adjusted until the diode peak pulse current as read on the current probe is equal to the DC current read on the ammeter. The pulse voltage required at the diode is then subtracted from the applied DC voltage to give a breakdown voltage value, measured with the junction at normal operating temperature. Because the pulse duration is much less than the chip thermal time constant, negligible cooling occurs. Using Eq. (9), a value for T_J and thus θ may be calculated if K_T is known. K_T may be measured by removing DC bias and applying external heat to the diode, while observing the pulsed breakdown voltage, using the circuit at Figure 2-7. In practice, several V_B versus T_C data points are measured for a few sample diodes from a given wafer

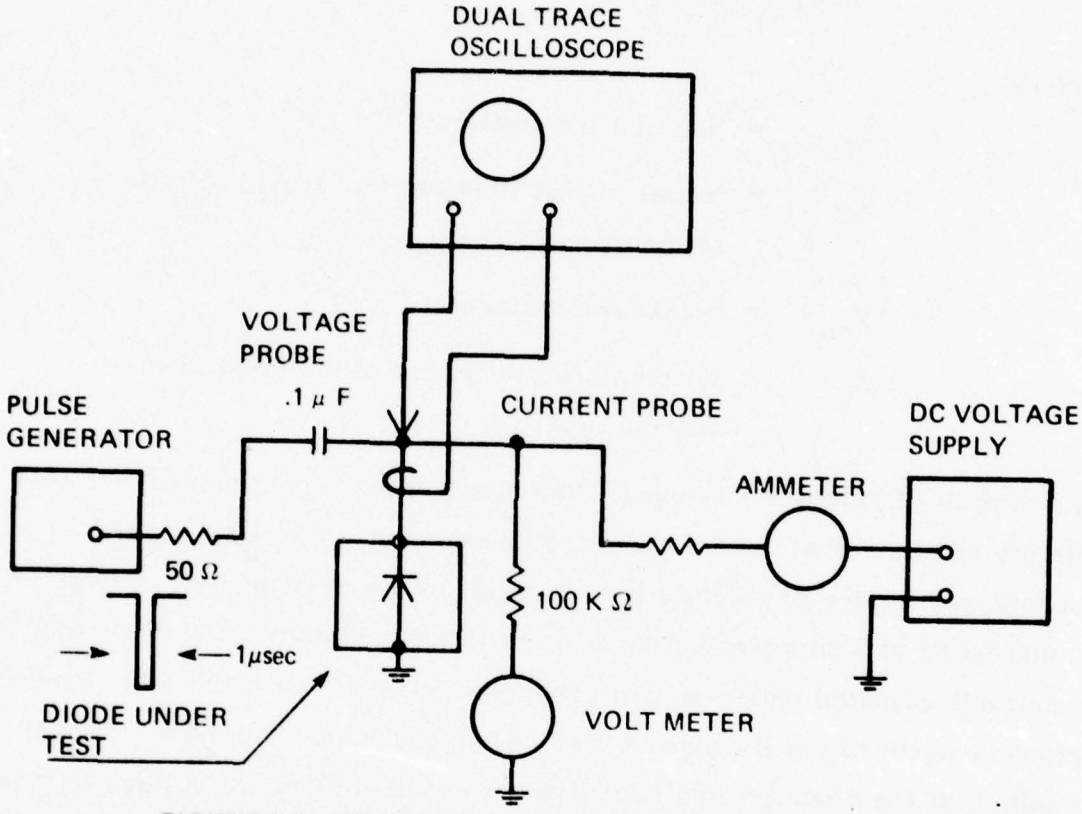


FIGURE 2-7. EQUIPMENT USED IN IMPATT THERMAL RESISTANCE MEASUREMENT

D-14019A

and K_T determined from a best fit line drawn on a V_T versus T plot. The value of K_T obtained is then used to characterize the thermal resistance of other diodes from the wafer.

$$\theta_J = \left[\frac{V_b - V_{bo}}{K_T} - T_{co} + T_C \right] \frac{1}{V_{DC} I_{DC}} \qquad (10)$$

where

V_b = breakdown voltage measured under operating conditions using 1 microsecond pulses, volts

V_{bo} = breakdown voltage measured with DC voltage turned off, using 1 microsecond pulse, volts

T_C = diode case temperature during operation, ^oC

V_{DC} = diode operating voltage, volts

I_{DC} = diode operating current, amperes

K_T = temperature coefficient of the breakdown voltage, volts/^oC

T_{co} = diode case temperature with DC voltage turned off, when V_{bo} was measured, volts

2.4 Device Characteristics

The general performance characteristics of the devices investigated in this program are as follows:

Breakdown Voltage (V_B):	21	to	26	volts
Zero Bias Capacitance (C_{TO}:	11.5	to	16	pF
Power Output (P_o):	2.3	to	3.3	watts
Operating Voltage (V_O):	43	to	53	volts
Operating Current (I_O):	275	to	385	mA

Operating Frequency (f_o)	:	8.3	to 9.5	GHz
Conversion Efficiency (η)	:	16	to 22	%
Thermal Resistance (θ)	:	9	to 12	$^{o}C/W$

3.0 EARLY FAILURE REGION TESTING

3.1 Introduction

The early failure region testing was intended to accomplish the following: 1) establish an effective burn-in screening technique, and 2) determine the time required using the indicated technique for diode parameters to stabilize. The following testing techniques were investigated:

1) High temperature reverse bias (HTRB) at 175°C and 80% of breakdown

2) 60 Hz AC burn-in at 100 mA peak forward current, 125°C, and 80% of breakdown peak reverse voltage

3) DC burn-in at 75°C case temperature and 15 to 15.5 watts of DC dissipation in the reverse direction

4) RF burn-in in the oscillating condition at rated output power and 75°C diode case temperature

Each burn-in was carried out for 168 hours. Failure was determined by RF testing following each screening, with a power drop of 2 dB or more considered a failure. The effectiveness of these burn-in screens was determined by passing groups of 20 devices sequentially through the tests. Devices failing in a later screen indicated that previous screens had been ineffective in removing defective diodes from the population. For example, of 17 diodes surviving AC burn-in, 8 were placed on DC burn-in and 4 failures resulted. The remaining 9 were placed on RF burn-in with 2 failures resulting.

Before entering the testing sequence, devices were preconditioned with a 24 hour DC burn-in, Military Standard 750 temperature cycling, constant acceleration and hermetic seal tests, and characterized as to breakdown voltage, zero bias capacitance, power output, efficiency and thermal resistance.

The complete early testing sequence is detailed in Figure 3-1.

3.2 Life Test Apparatus

The equipment used to perform the various early failure region tests is identical to that used in the long-term and step stress tests. This equipment will now be described.

3.2.1 DC Burn-In Apparatus

Figure 3-2 pictures the electrical circuit of the DC burn-in rack. A 50 diode rack was constructed. Each diode was mounted in a 1/4 - 28 threaded copper holder and screwed into a water cooled brass plate. Only diodes in case style 111 (3-48 threaded base) were used. Cooling or heating of the circulating coolant was provided by a Lauda model K2/R circulating bath. Contact to the diode caps was made using commercially available spring loaded probes with 1/8 inch diameter tips, (Pogo probe). Each diode was biased through a circuit breaker and 120 ohm adjustable series resistor. A 33 ohm fixed resistor was located as close as possible to the diode cap and served to suppress oscillation in the bias line. Individual diode current and voltage metering was provided.

3.2.2 RF Burn-In Equipment

Two twenty-position RF burn-in kits were contructed. The electrical circuit of one position appears in Figure 3-3.

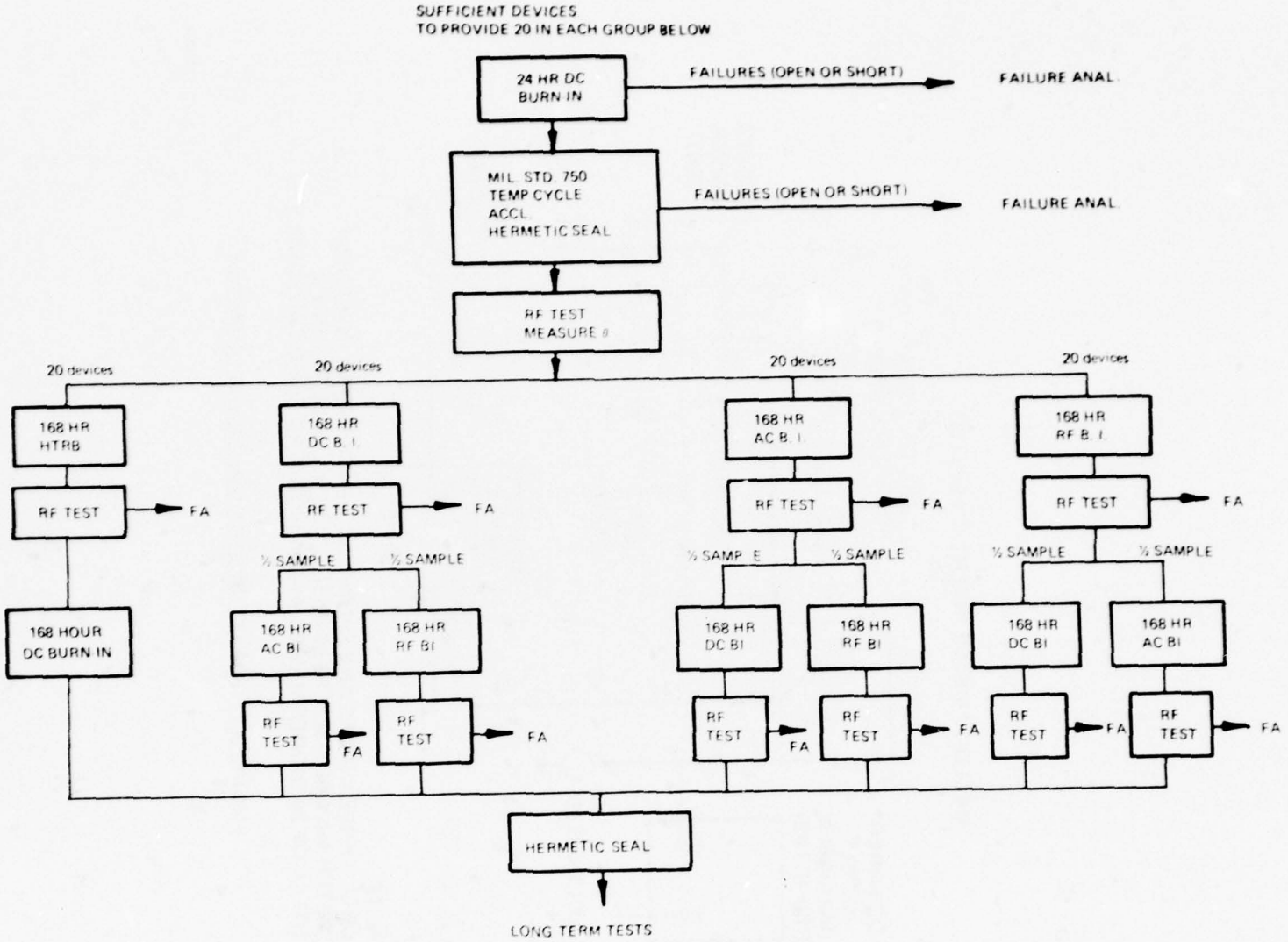
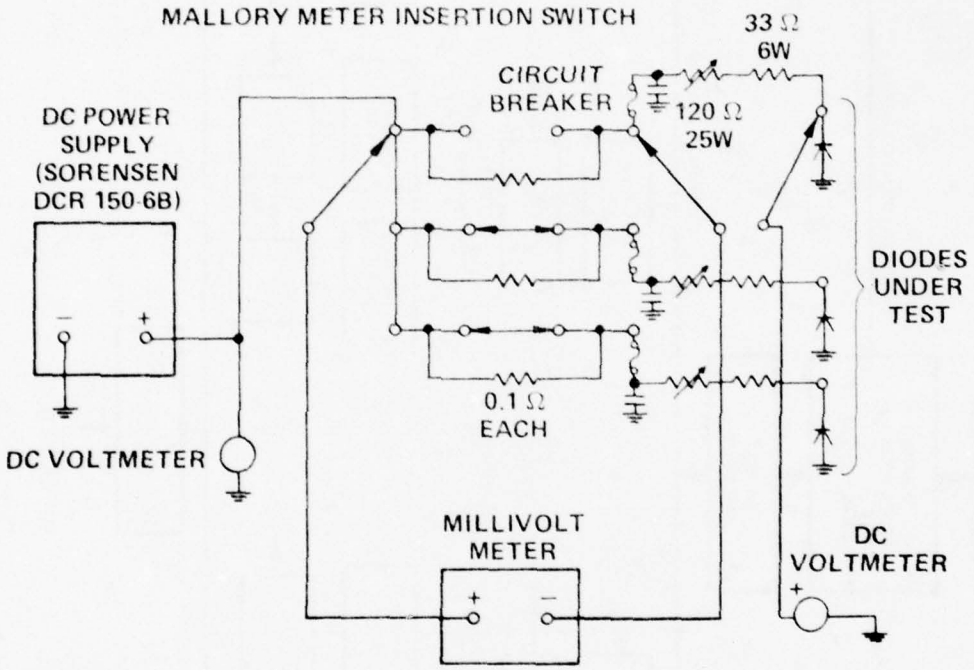


FIGURE 3-1. EARLY FAILURE REGION TESTING SEQUENCE



NOTE:
ONLY THREE DIODES ARE SHOWN, BUT EACH METER INSERTION SWITCH MAY BE USED TO MONITOR UP TO 12 DIODES, AND A TOTAL OF 50 DIODES MAY BE ACCOMMODATED SIMULTANEOUSLY.

FIGURE 3-2. IMPATT DIODE DC BURN-IN EQUIPMENT

D-11503A

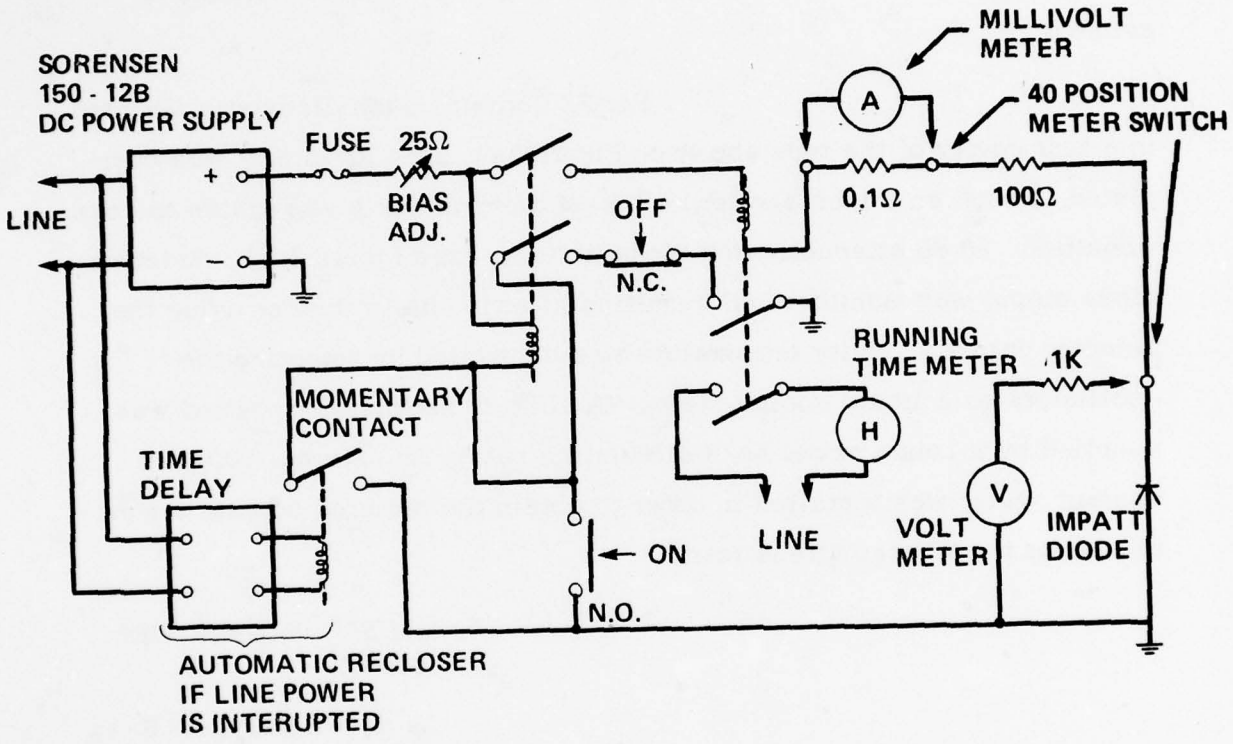


FIGURE 3-3. CIRCUIT DIAGRAM OF ONE SECTION OF 20 SECTION IMPATT DIODE RF BURN-IN APPARATUS

D-12335A

Each position contains a running time clock, adjustable series resistance bias control, and sensing relays. If the diode should fail either open or short, the running time meter is stopped. In addition, each diode is connected in series with a 0.1 ohm, 1% resistor for current monitoring, without breaking the circuit for ammeter insertion. Thus, a switching transient which could cause failure in heavily over-stressed diodes is avoided.

For RF burn-in, each diode was mounted in a test cavity of the type shown in Figure 3-4. The RF circuit was completed through an 8 inch section of WR-90 waveguide, a waveguide to coax transition, 20 dB attenuator and diode detector (see Figure 3-5). Relative diode output was monitored on a multipoint strip chart recorder using the detector output. Cavity temperature was controlled by mounting the oscillators on a liquid cooled plate. Cooling or heating as required was supplied by a Lauda model Ke/R circulating bath. An external 500 watt coolant heater was installed in order to obtain the required coolant temperatures for the RF step stress tests.

3.2.2.1 Current Regulator Bias Supply

As shown in Figure 3-3, bias current was supplied to the IMPATTs through series resistors. Total bias line resistance was about 100 ohms following adjustments.

A current regulator would have greatly improved the overall conversion efficiency from power supply output to RF, by reducing the bias path voltage drop and would more nearly simulate the actual use bias condition. Because 40 regulators were needed, a commercial integrated circuit unit was investigated. A simple regulator circuit (shown in Figure 3-6) was designed and tested, using a 2.5 watt

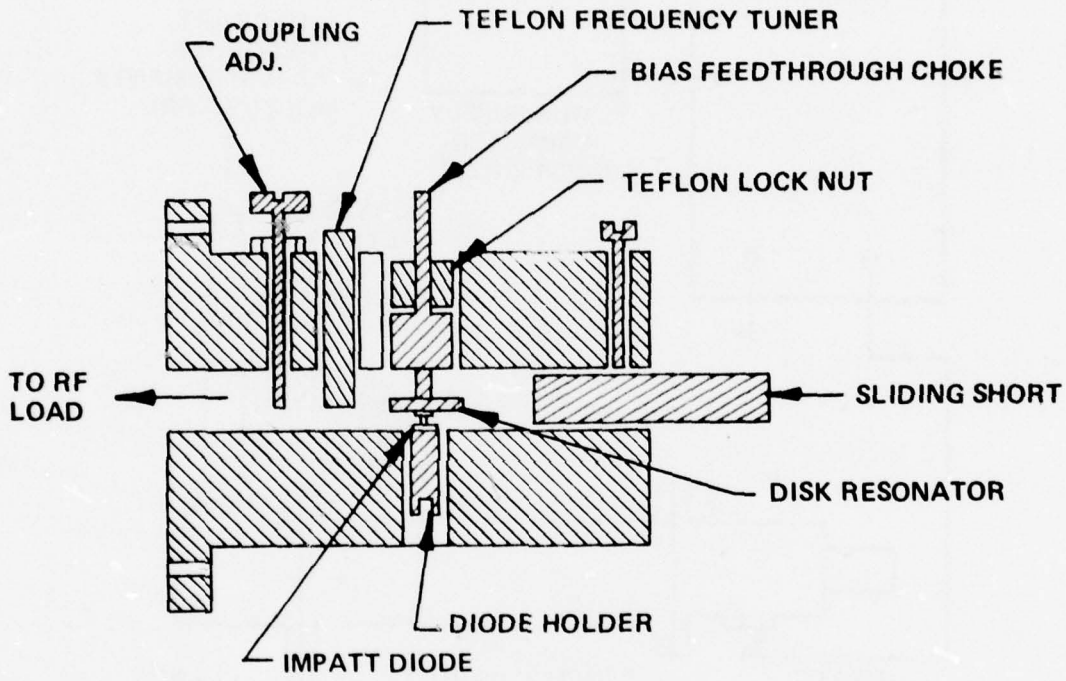


FIGURE 3-4. IMPATT OSCILLATOR FOR USE IN RF BURN-IN APPARATUS

D-14014A

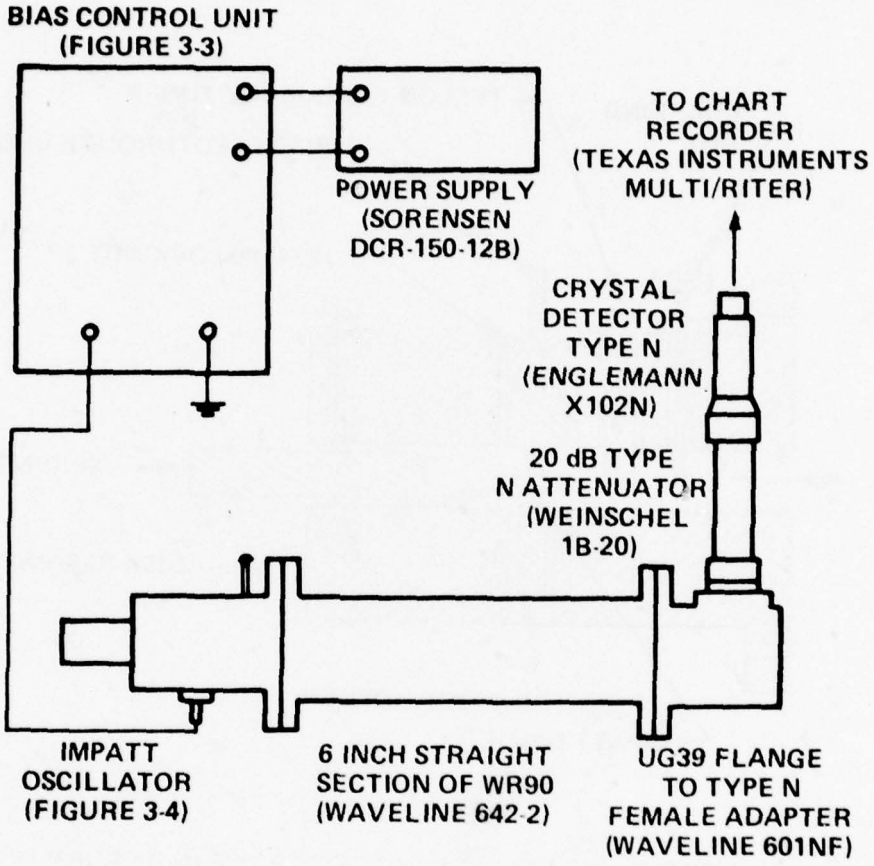
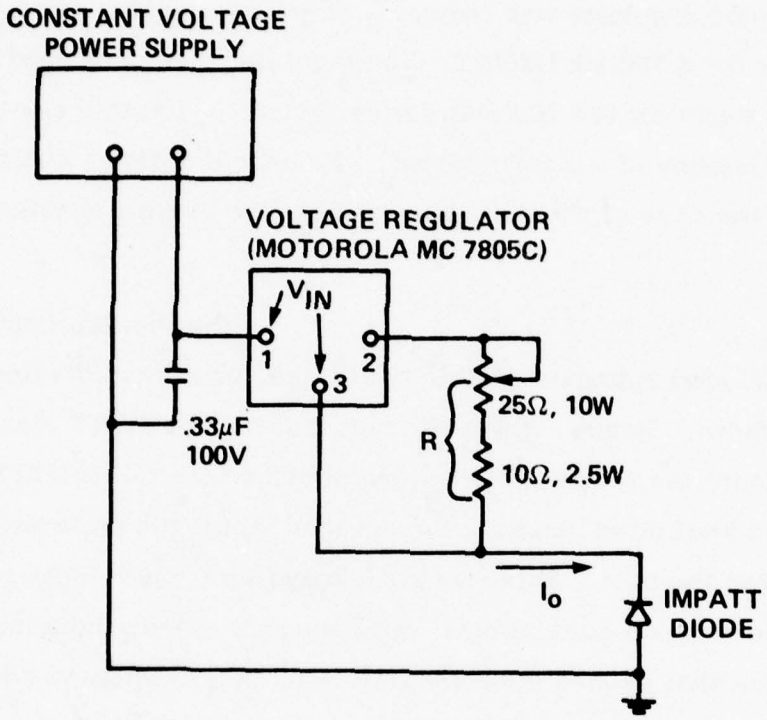


FIGURE 3-5. RF SECTION OF IMPATT RF BURN-IN OR RF STEP STRESS APPARATUS

D-16485



MC 7805C SPECIFICATIONS

$I_o = \frac{5}{R}$

V_{IN} = 7.0 VOLTS MIN, 35 VOLTS MAX

P_D = 15 WATTS AT 25°C

FIGURE 3-6. PROPOSED IMPATT BIAS CURRENT REGULATOR

D-16484

diode mounted in one of the RF burn-in test cavities. The regulator consisted of a commercially available integrated circuit voltage regulator operated in the constant current mode. A minimum operating voltage drop of 7 volts across the regulator was required, which was equivalent to a 23 ohm series resistor for a 300 mA IMPATT. The regulator then consumed 2.1 watts, compared to 9 watts for the 100 ohm series resistor. Using the regulator, the overall efficiency of a 3 watt output, 20% efficient diode would be cut to 17.5%. In the case of the 100 ohm resistor, the overall efficiency was 12.5%.

The regulator chosen (MC7850C) included automatic current, voltage, or excess dissipation overload shutdown. Hence, it was thought that if the IMPATT diode failed to a short circuit, the regulator, when subjected to the full IMPATT operating voltage, would shut down, and not be damaged, until the protective relay circuits removed the bias. This was not always the case. Some regulators did not shut down to an open circuit, but became shorted, inducing a power supply transient that caused other regulators to shut down, and damaging IMPATTs under test. The regulators were also sensitive to bias circuit oscillations that often occurred if an IMPATT was mistuned. For these reasons, the regulator circuit was abandoned in favor of the 133 ohm series resistor circuit.

3.2.3 AC Burn-In and HTRB Apparatus

AC burn-in was conducted by simply applying line voltage to the IMPATTs through a step-down transformer and 1000 ohm series resistors. Units were mounted in an oven to obtain the required test temperature.

HTRB tests were conducted using the same equipment but with the AC power supply replaced with a DC power supply.

3.3 Early Failure Region Test Results

One-hundred, forty-eight devices were passed through the early failure region tests. Table 3-1 summarizes the resulting failure distribution.

In general, HTRB and AC burn-in proved to be ineffective as early failure screening methods in that diodes surviving HTRB or AC burn-in failed in a subsequent DC or RF burn-in. DC and RF burn-in were of equal value because similar percentages of devices surviving DC or RF burn-in failed in subsequent RF burn-in. Because of the equipment simplification involved, DC burn-in is the recommended early failure region screen.

Diode parameter change occurring during the 168 hour DC burn-in is summarized in Table 3-2. The only significant change seen was a slight increase in breakdown voltage. This change is consistent with behavior expected if the 200 Å platinum layer had not been completely reacted during the sintering step. Parameter stabilization as shown in Figure 3-7 usually was complete within 4 days.

Diode failure occurring in the early failure region testing was found to be due to inevitable manufacturing defects such as incomplete solder melting, chip damage from contact with the bonding tool, or mesa surface contamination. Figure 3-8 shows an example of failure due to contact of the bonding tool with the mesa edge. The bonding tool used consists of a thick wall tube with an inside diameter 2 mils larger than the mesa diameter. The ring-like impression in the PHS pad indicates the point contact of the bonding tool inside the diameter. As happened here, the tool was not centered properly and damaged the mesa. In many cases, failure appeared to occur because of the formation of a highly conducting channel along the mesa surface. Such failure is characterized by a plume

Test (each 168 hours)	Failures (%)	Subsequent Test	Subsequent Failures (%)
HTRB ($175^{\circ}C$, 80% of V_B)	0	DC Burn-in	11
AC BURN-IN ($125^{\circ}C$, 100 mA peak forward, 80% V_B reverse)	0	DC Burn-in	50
		RF Burn-in	22
DC BURN-IN ($75^{\circ}C$, 15 W Dissipation)	18.4	AC Burn-in	0
		RF Burn-in	12
RF BURN-IN ($75^{\circ}C$, 12.5 W Dissipation)	15	AC Burn-in	0
		DC Burn-in	12.5

TABLE 3-1 RESULTS OF EARLY FAILURE REGION TESTING

PARAMETER	INITIAL VALUE	FINAL VALUE
Breakdown Voltage (1 mA)	24.45 volts	25.18 volts
Capacitance at Zero Bias	14.06 pF	14.13 pF
Output Power (maximum)	2.99 Watts	2.89 Watts
Frequency of Maximum Output	8736 MHz	8785 MHz
Operating Voltage at Maximum Output	51.95 volts	51.29 volts
Operating Current at Maximum Output	300.8 μA	306.3 μA
Conversion Efficiency at Maximum Output	19.3 %	18.5 %

TABLE 3-2 EFFECT OF 168 HOUR DC BURN-IN ON AVERAGE IMPATT DC AND RF PARAMETERS

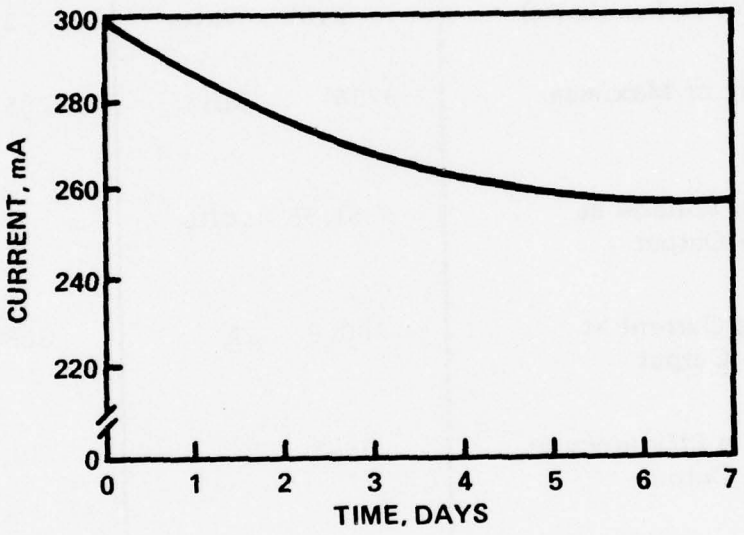


FIGURE 3-7. VARIATION OF IMPATT CURRENT VS TIME DURING DC BURN-IN USING CONSTANT VOLTAGE SOURCE AND 100 OHM SERIES RESISTOR

D-16519

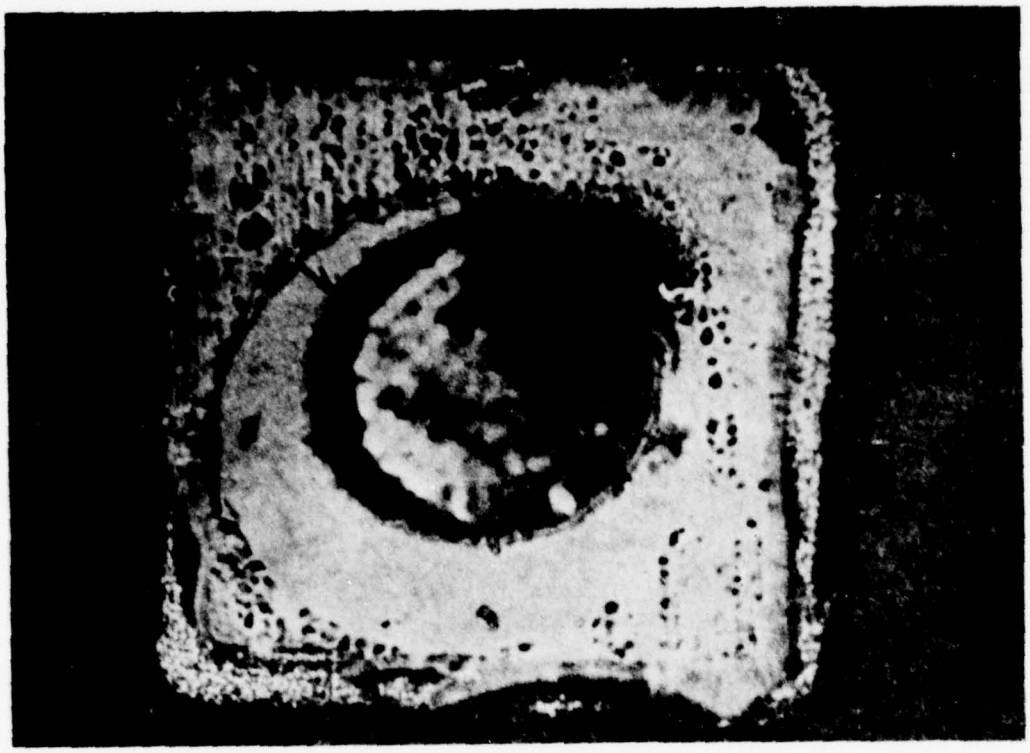


FIGURE 3-8. PHOTOMICROGRAPH OF A DIODE THAT FAILED DUE TO CONTACT OF THE BONDING TOOL WITH THE MESA 100X

D-16491

or trail of evaporated gallium arsenide on the plated heat sink pad (see Figure 3-9). SEM examination revealed the badly cracked and deformed mesa surface shown in Figure 3-10. Such failures are probably due to surface contamination of the mesa because of incomplete cleaning following in-package etching. Exact identification of the cause of failure is difficult in many of these failures because of extensive chip damage.

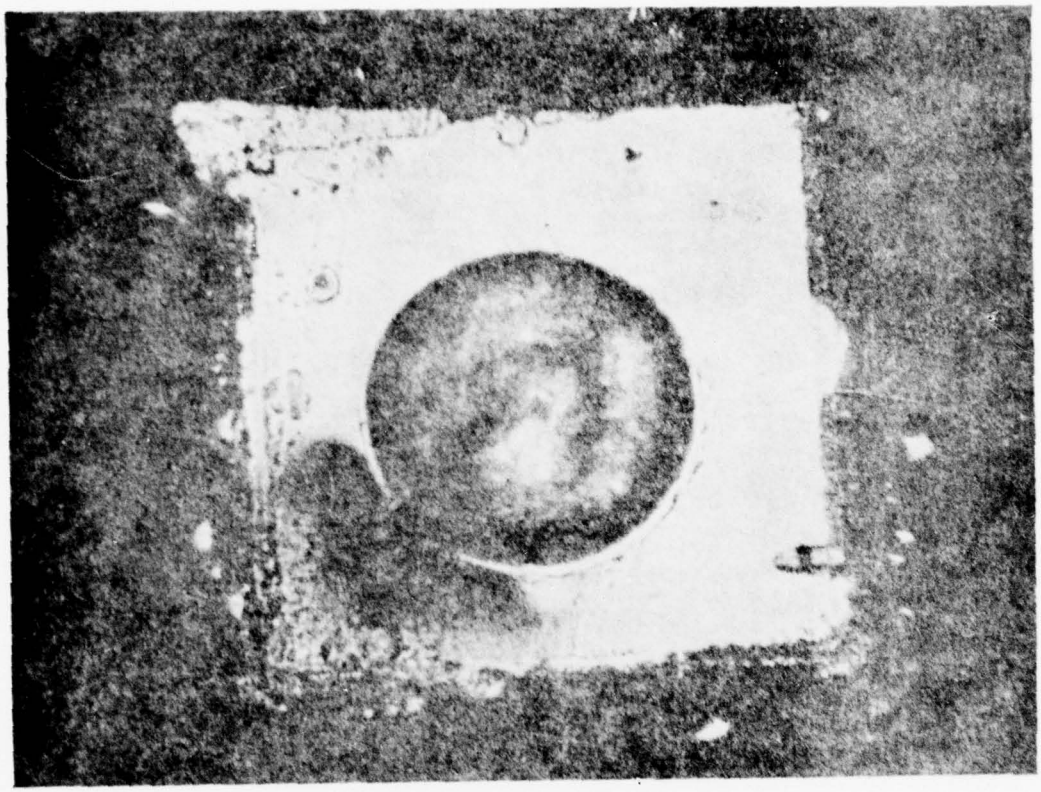


FIGURE 3-9. PHOTOMICROGRAPH OF A DEVICE FOLLOWING FAILURE DURING 168 HOUR DC BURN-IN (100X)

D-16492

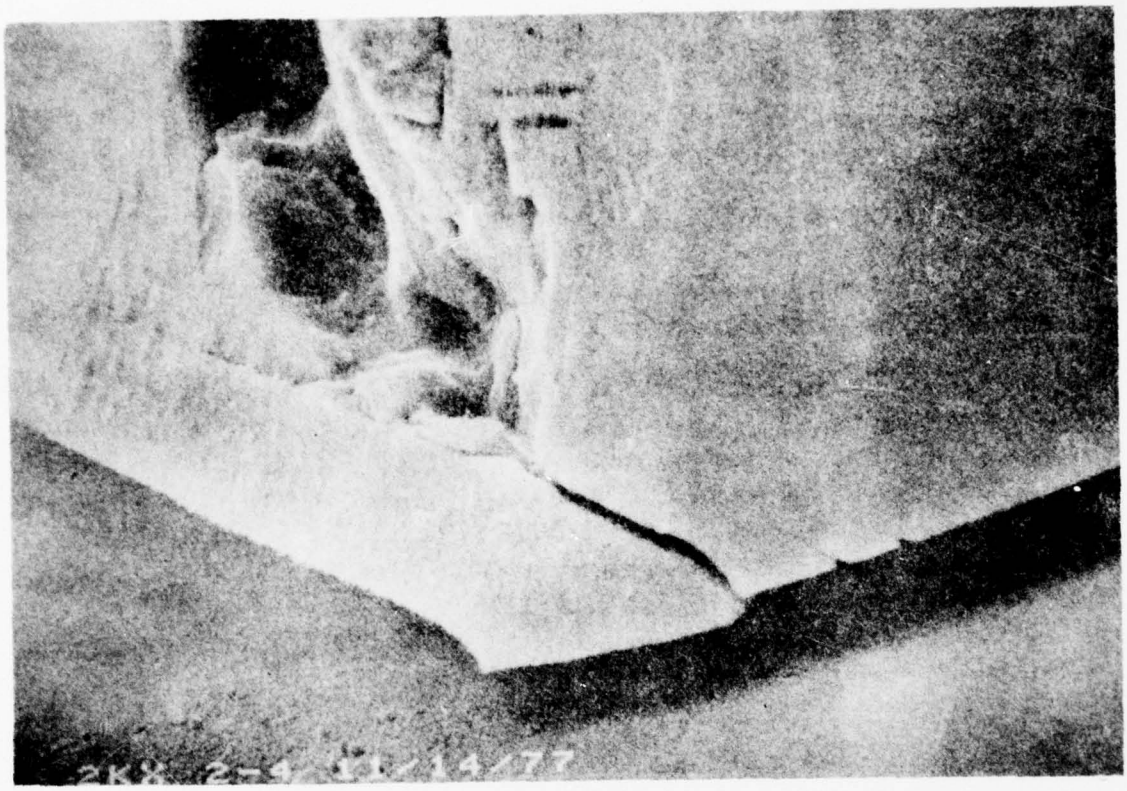


FIGURE 3-10. SEM PHOTOGRAPH OF A DEVICE FOLLOWING FAILURE DURING 168 HOUR DC BURN-IN

D-16490

4.0 ACCELERATED STRESS TESTS

The long term and accelerated stress testing sequence is summarized in Figure 4-1. Before entering this testing sequence, devices were pre-conditioned with 168 hour DC burn-in at 75°C case temperature and 15 watts of input power dissipation followed by Military Standard 750 hermetic seal tests (conditions 1071H and 1071E). Each device was characterized as to DC and RF parameters in the standard test cavity and again in the burn-in cavity. A doping profile was measured on each device. On finished devices only the peak region can be profiled before device breakdown occurs.

4.1 RF Burn-In Step Stress Testing

RF step stress tests were conducted using 40 devices, 20 each in 24 hour and 168 hour period tests. Device thermal resistance was carefully measured, allowing accurate determination of the junction temperature at failure for each diode. The IMPATTs were mounted in individual oscillators and power output was continuously monitored using a strip chart recorder. Initially, each device was biased at rated output power (2 watts minimum) with 70°C diode case temperature. Following each 10°C case temperature step, cavity tuning was adjusted to maintain maximum output, but input DC power was not changed. Devices degrading in output by more than 2 dB during the step as well as open and shorted devices were considered failures.

4.1.1 Twenty-four Hour Period RF Step Stress Test

This test was conducted using the current regulator circuits described previously to supply bias to the diodes. Some problems were encountered in the test in that diode operating points shifted with increasing temperature, requiring retuning of the oscillator cavities at each step. Retuning for maximum power was always accompanied by decrease in current resulting in a lower than desired junction temperature step. Attempts to increase operating current by adjusting the voltage compliance of the

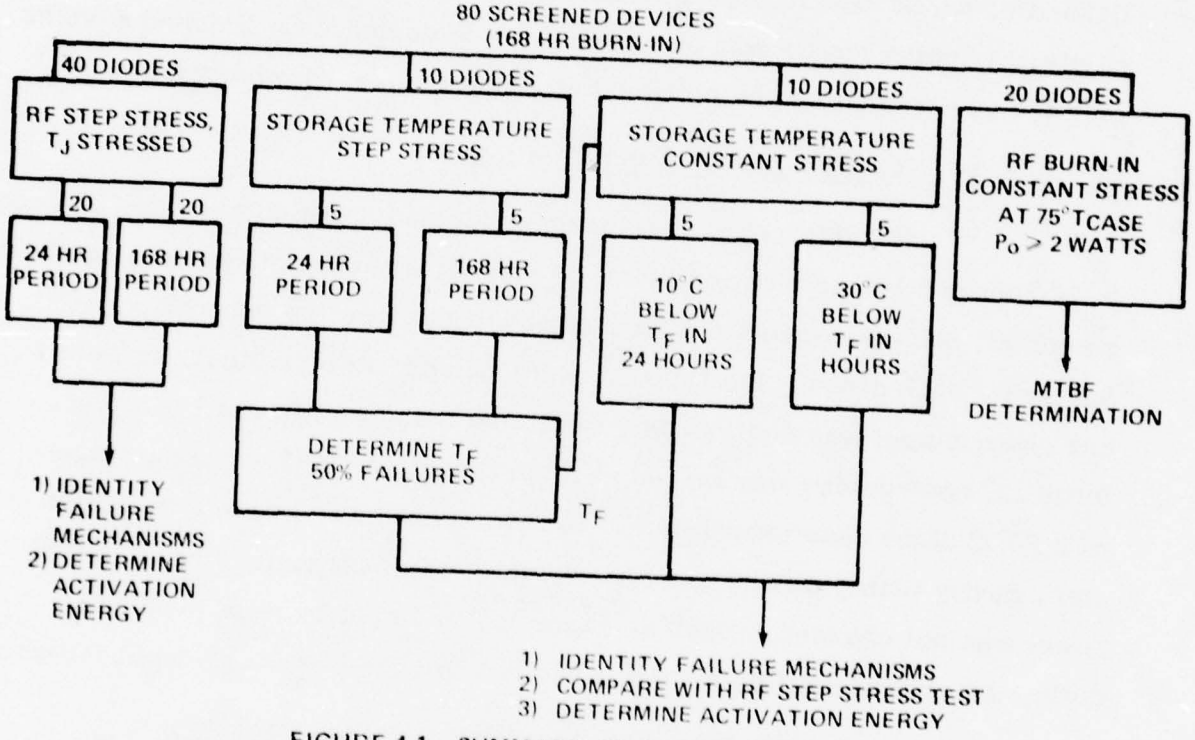


FIGURE 4-1. SUMMARY OF LONG TERM AND ACCELERATED STRESS TESTS

D-14022

current regulators resulted in the diodes falling out of oscillation. In the last two steps, some diodes were deliberately detuned to increase their junction temperatures. Even at 130°C diode case temperature, half of the units were capable of over two watts output. During step #11, coolant at 130°C, five devices failed simultaneously. Their junction temperatures ranged from 269°C to 280°C. It was discovered that all five of the current regulators involved had also failed. There was no way of determining if failing IMPATTs resulted in regulator failure or failing regulators caused IMPATT failure. Because only five diodes had survived, the test was terminated and data analysis was based on the performance of the other 15 devices. Surviving diodes were retested and the results are compared with original data in Table 4-1. One device, Lot 6 #12, exhibited significant performance degradation, droppings from 17% efficiency to 13%, while other devices reproduced essentially the original readings. The devices were reprofiled and in general exhibited shifts in peak position toward the surface of about 0.04 micron. The device that degraded in efficiency was not a typical in this respect. All diodes showed a slight increase in capacitance and breakdown voltage. In retesting the devices, the circuit and bias conditions were adjusted for maximum efficiency.

4.1.2 One Hundred Sixty Eight Hour Period RF Step Stress Test

A similar RF step stress test was conducted using a one week period. For this test the troublesome current regulators were replaced with 75 ohm series resistors. The test was started with 20 devices, each producing at least 2 watts of output power. The diodes were allowed to operate for three days at a 62°C coolant temperature as equipment was checked out. For the first step, a coolant temperature of 82°C was used. Six diodes failed in this step. Only one additional diode failed in the subsequent two steps.

TABLE 4-1

DIODE PARAMETER CHANGE OCCURING DURING 24 HOUR PERIOD

RF STEP STRESS TEST

DIODE		V_B VOLTS	C_{TO} pF	P_o W	f_o GHz	V_o VOLTS	I_o mA	η %
4-4	INITIAL	21.4	12.7	2.8	8.64	47.0	360	16.5
	FINAL	22.2	13.2	2.15	9.50	46.6	360	15.4
6-9	INITIAL	23.3	11.5	2.95	9.22	51.0	325	17.9
	FINAL	26.1	15.3	2.8	8.60	55.2	330	15.4
6-10	INITIAL	24.4	12.1	3.00	9.29	51.9	290	19.9
	FINAL	25.5	15.1	3.05	8.50	51.6	340	17.4
6-12	INITIAL	24.7	12.0	2.95	8.50	52.4	340	16.6
	FINAL	25.3	14.5	2.35	8.50	53.4	340	12.9
6-15	INITIAL	22.2	11.9	2.90	8.65	47.5	340	18.6
	FINAL	23.1	14.5	2.60	8.78	47.4	333	16.5

Because of the annual plant shutdown at Microwave Associates, all experiments were shut off on 29 July 1977. Prior to shut down, the 168 hour period RF step stress test had completed step 5 with a coolant temperature of 133°C. Nine diodes of the original twenty were surviving at this point. Junction temperatures of surviving diodes ranged from 257 to 295°C.

Before shutting the RF step stress experiment off, the kit was cooled to the first step coolant temperature (62°C), and each surviving diode was returned in an effort to repeat the original readings. The diodes had been returned at each step to ensure continued operation at maximum output power. In general, original power output was duplicated, but at reduced operating current. Breakdown voltage had increased, and in the case of one diode removed for further testing, the zero bias capacitance had increased. This diode was reprofiled, and the results appear in Figure 4-2. A slight narrowing of the peak is evident.

Following the two week plant shutdown, the diodes on the RF burn-in kit were connected to a curve tracer for breakdown measurement without removing them from the cavity oscillators. Diodes in positions 2 and 13 were found to be shorted, although they had operated properly when the kit had been cooled at 62°C before shutdown. Because of these unexplained failures, the results for these two diodes were not used in data analysis.

The final step in the 168 hour period test was conducted at a coolant temperature of 145°C, with diode junction temperatures ranging from 258°C to 315°C. Six diodes survived the final step, and were removed from the apparatus and completely characterized. Initial and final test data for these diodes appears in Table 4-2. In every case, diode performance had improved as compared with the initial data with respect to efficiency. Breakdown voltage had increased, zero bias capacitance slightly increased, operating voltage increased, and operating current decreased. In addition,

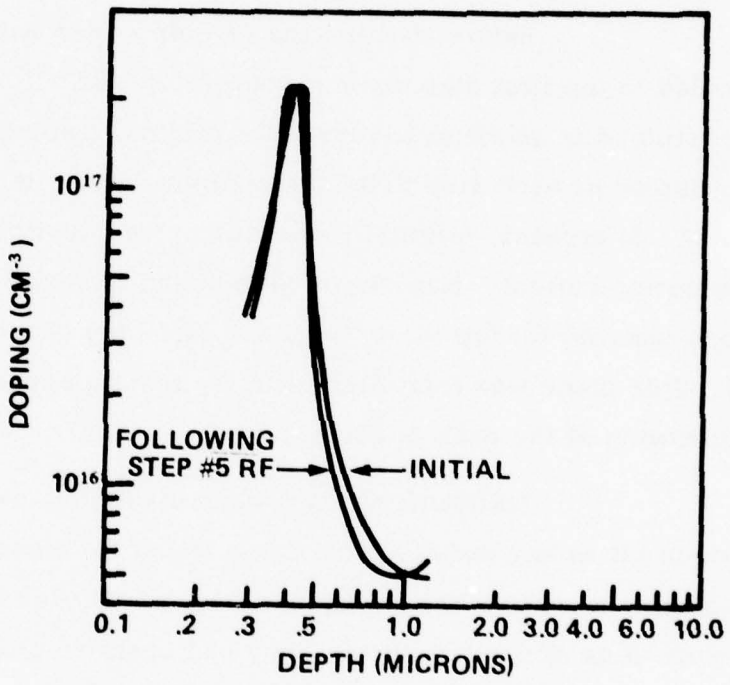


FIGURE 4-2. DOPING PROFILE OF DIODE 2-6 BEFORE AND AFTER 5 WEEKS OF RF STEP STRESS TESTING AT A MAXIMUM JUNCTION TEMPERATURE OF 265° C.

D-16520

TABLE 4-2

DIODE PARAMETER CHANGE OCCURING DURING 168 HOUR PERIOD

RF STEP STRESS TEST

DIODE		V_B VOLTS	C_{TO} pF	P_o W	f_o GHz	V_o VOLTS	I_o mA	η %
2-6	INITIAL	21.3	12.0	3.0	9.3	47.4	340	18.5
	FINAL	29	12.7	3.0	8.74	58.8	269	19.0
2-19	INITIAL	24.2	12.2	2.75	9.26	54.0	300	17.0
	FINAL	28	14.9	3.7	8.62	55.4	323	20.7
3-12	INITIAL	22.0	12.3	3.0	8.42	48.8	385	16.0
	FINAL	30	14.8	3.3	8.64	60.7	296	18.4
3-19	INITIAL	22.1	11.9	3.0	8.49	48.6	360	17.1
	FINAL	28	13.9	3.0	8.75	59.1	242	21
3-20	INITIAL	21.9	12.3	2.85	9.30	49.4	328	17.6
	FINAL	27	13.8	3.1	9.34	56.2	255	21.6
3-23	INITIAL	22.3	12.1	3.0	8.44	49.5	360	16.9
	FINAL	27	15.1	3.1	9.28	55.2	277	20.3

the diodes were much more prone to oscillate in the bias circuit than before RF step stress. A bias line filter consisitng of a series RF choke was of some help in reducing oscillations, and was used in testing the last two devices (lot 2, #20 and #23).

Surviving devices were also reprofiled, and in general exhibited a slight reduction in peak height (from 2.8 to 2.3 x 10^{17} cc^{-1}) and half width (from 0.08 to 0.06 micron) (see Figure 4-3). In some cases, peak position had shifted toward the surface by as much as 0.06 micron.

4.1.3 Failure Analysis of Devices Failing During RF Step Stress Tests

All devices failing in the RF step stress tests failed to a short circuit condition, with the exception of device 6-12 which dropped in output power and efficiency. Examinations of failing units revealed essentially the same conditions as had been seen in the case of the early failure region device failures. That is, formation of a highly conducting surface layer or channel, resulting in severe mesa damage and evaporation of gallium arsenide onto the PHS pad (See Figure 4-4). A closer examination with a scanning electron microscope revealed a circumferential step in the platinum-tantalum top metallization layers, closely following the mesa outline. As seen in the scanning electron microscope photograph of Figure 4-5, the step does in some cases extend into the etch gap where elevated metal fragments could short the diode. This crack could be due to thermal expansion coefficient mismatch between the gold and tantalum layers. The region along the mesa circumference would be exposed to the largest temperature gradient and would crack first releaving the stress. Interpretation in terms of an activation energy is tenuous, because once cracking takes place, failure will not necessarily follow. Indeed, devices surviving the step stress test (315°C junction for 168 hours) have exhibited circumferential cracking.

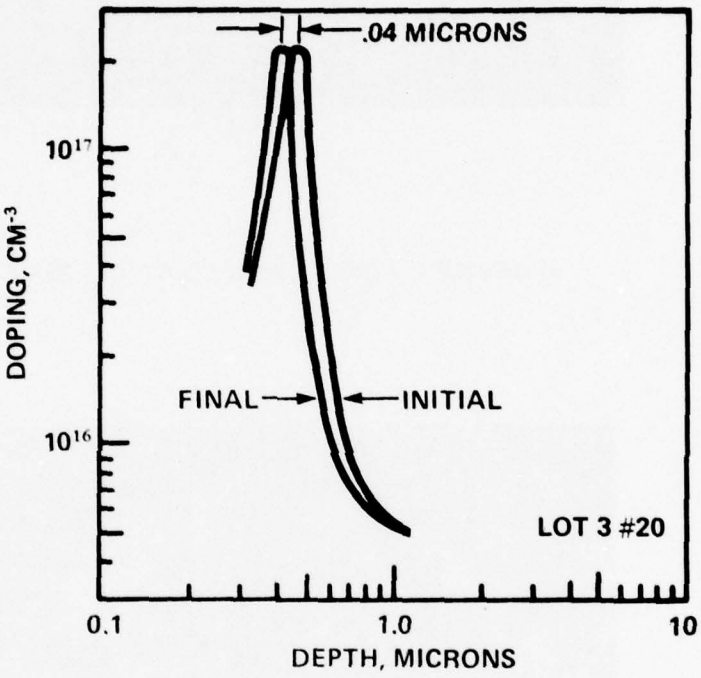
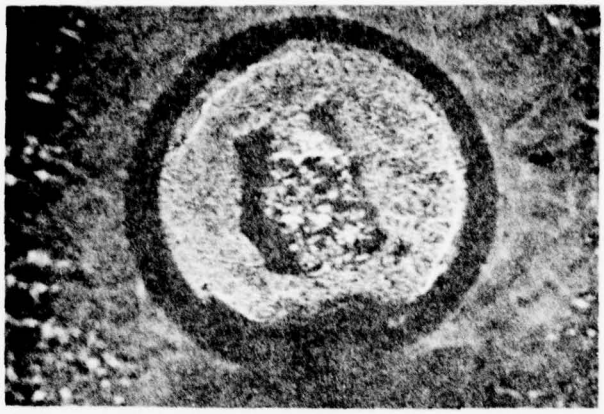
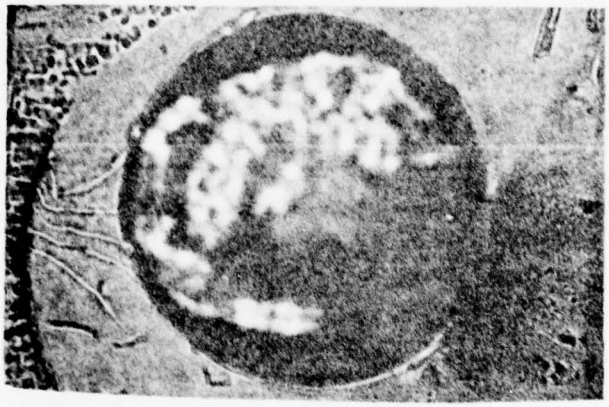


FIGURE 4-3. COMPARISON OF DEVICE DOPING PROFILE BEFORE AND AFTER 168 HOUR RF STEP STRESS AT 315°C MAXIMUM JUNCTION TEMPERATURE

D-16521



a) DEVICE 2-7 (200X), FAILED AT T_J = 237°C



b) DEVICE 4-18 (200X), FAILED AT T_J = 272°C

FIGURE 4-4. TWO DEVICES FOLLOWING FAILURE DURING RF STEP STRESS TESTING

D-16513

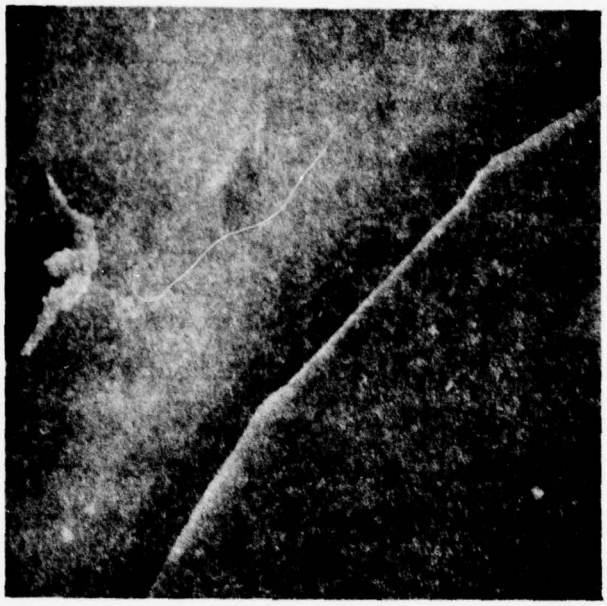


FIGURE 4-5. SEM PHOTOGRAPH OF A DEVICE FOLLOWING FAILURE DURING RF STEP STRESS TESTING (800X)

D-16543

In order to determine if cracking occured during RF step stress or during device initial operation, devices failing in the first 17 hours of burn-in were examined for circumferential metallization cracking. In about 30% of the cases, cracks were found, indicating that cracking was occuring very early in the operation life of the devices. Figure 4-6 shows one of these devices following gallium arsenide removal through etching. The shape of the crack is clearly seen. Blackened areas in the pad metallization are due to heat generated during burn-out.

Some deterioration in the back contact metallization was observed for devices failing in the 168 hour RF step stress test. Figure 4-7 depicts this condition. Apparent change in metal appearance is no doublt due to continued sintering of the back contact during operation. The circular pattern is probably the result of different sintering rates due to radial temperature gradients across the back contact.

Two devices that had survived the 168 hour RF step stress test at 315 and 242°C maximum junction temperature were cross sectioned and examined using the SEM X-ray spectrometer.

Analysis at 1 micron from the interface into the gallium arsenide, indicated zero detectable gold concentration. The probe diameter was 1 micron. This result indicates that the tantalum blocking layer was effective in preventing penetration of gold into the active region. The X-ray spectra at three locations and the cross section for one of these devices appear in Figure 4-8.

4.1.4 RF Step Stress Results

The results of the RF burn-in step stress tests appear in Figures 4-9, 4-10 and 4-11. Junction temperature at failure versus cumulative failures have been plotted on probability paper, and in the 168 hour test an initial point not lying on the normal distribution characteristic



FIGURE 4-6. PHOTOMICROGRAPH OF A DEVICE THAT FAILED DURING INITIAL BURN-IN. THE GALLIUM ARSENIDE MESA HAS BEEN ETCHED AWAY TO REVEAL THE CRACKING IN THE METALLIZATION.

D-16517

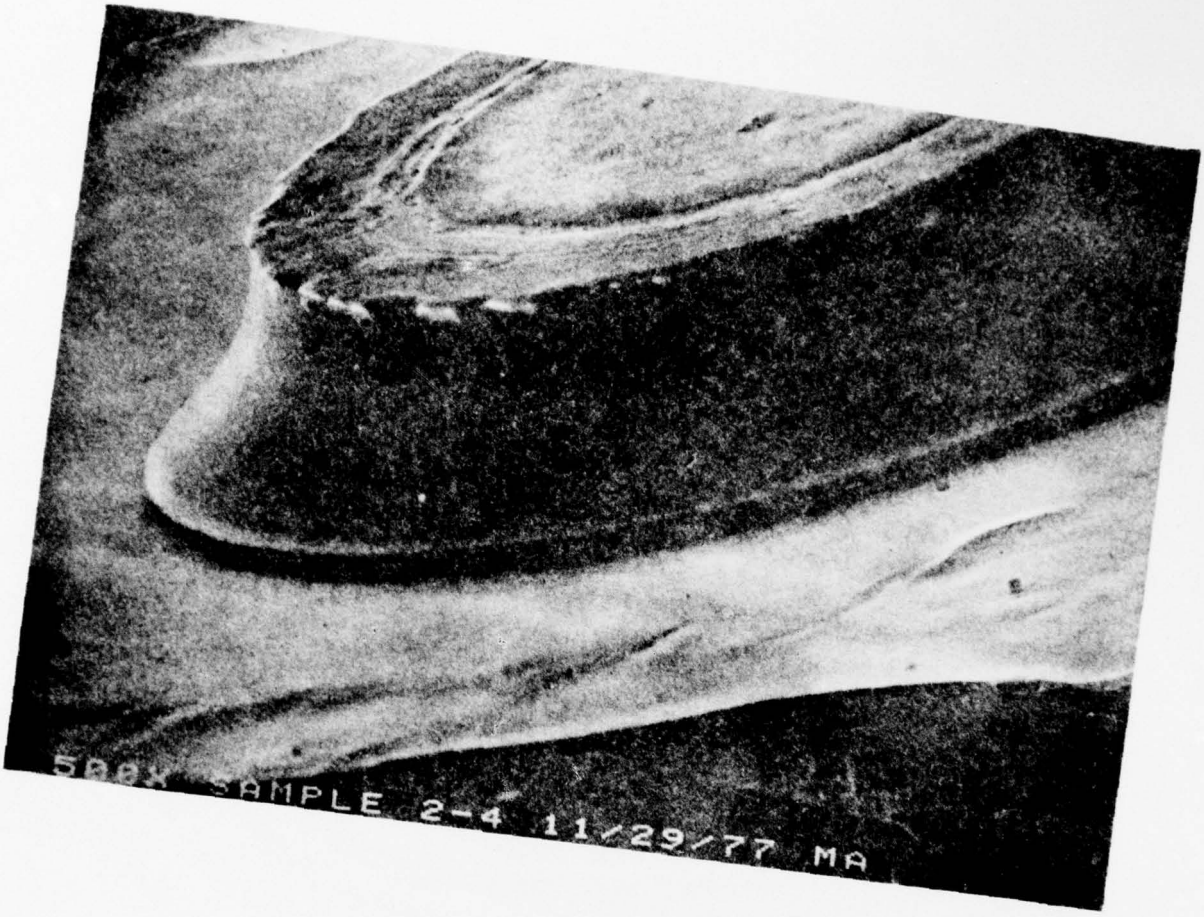


FIGURE 4-7. DEVICE 2-4 FOLLOWING 168 HOUR RF STEP STRESS AT 270°C MAXIMUM JUNCTION TEMPERATURE (500X)

D-16516

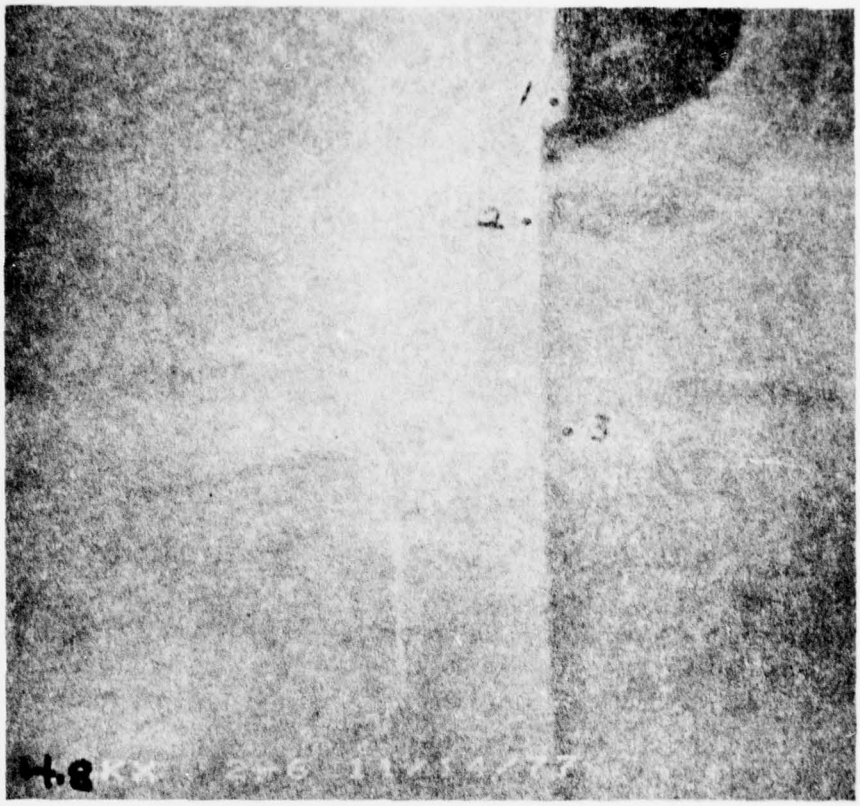
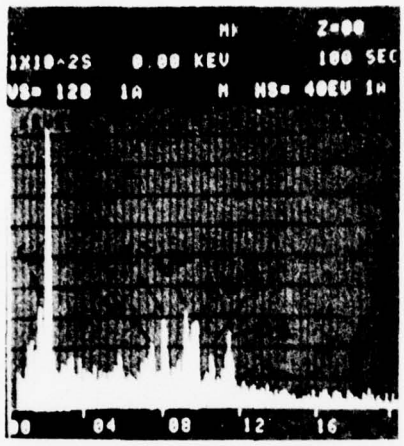
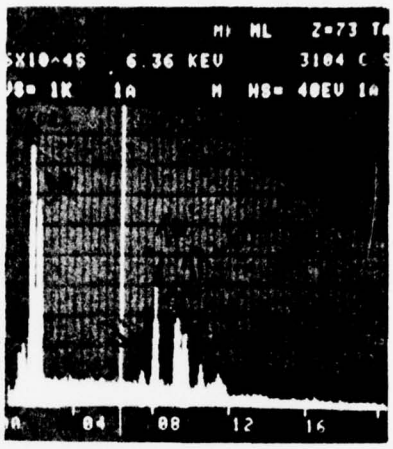


FIGURE 4-8 (a). CROSS SECTION OF DEVICE 2-6 AFTER 168 HOURS RF STEP STRESS TESTING AT A MAXIUM JUNCTION TEMPERATURE OF 315°C. INDICATED POINTS WERE EXAMINED WITH ELECTRON BEAM MICROPROBE ANALYSIS

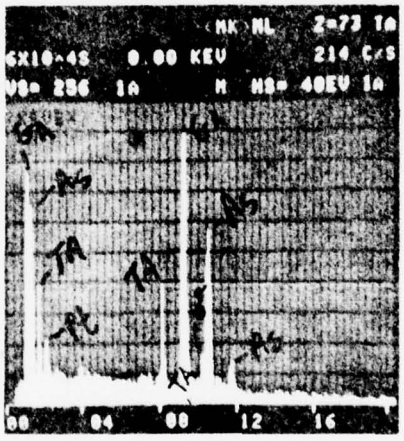
D-16531



POSITION 1



POSITION 2



POSITION 3

FIGURE 4-8 (b). X-RAY SPECTRA OBTAINED FROM THE DEVICE OF FIGURE 4-7

D-16533

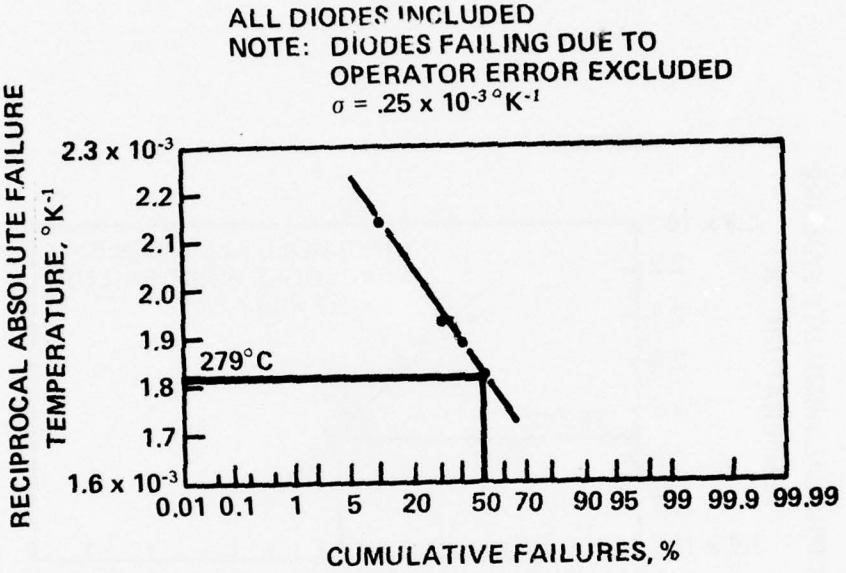


FIGURE 4-9. RECIPROCAL ABSOLUTE FAILURE TEMPERATURE VS CUMULATIVE FAILURES RF STEP STRESS – 25 HOUR PERIOD

D-16522

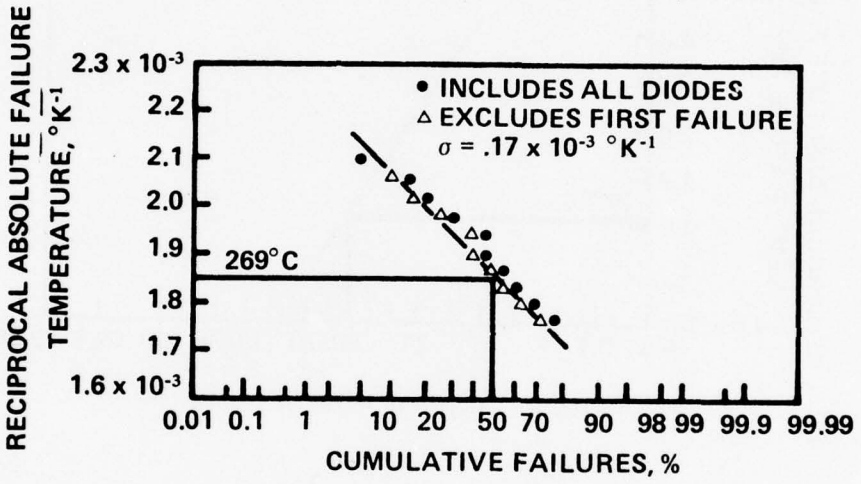


FIGURE 4-10. RECIPROCAL ABSOLUTE FAILURE TEMPERATURE VERSUS CUMULATIVE FAILURES RF STEP STRESS TEST – 168 HOUR PERIOD

D-16523

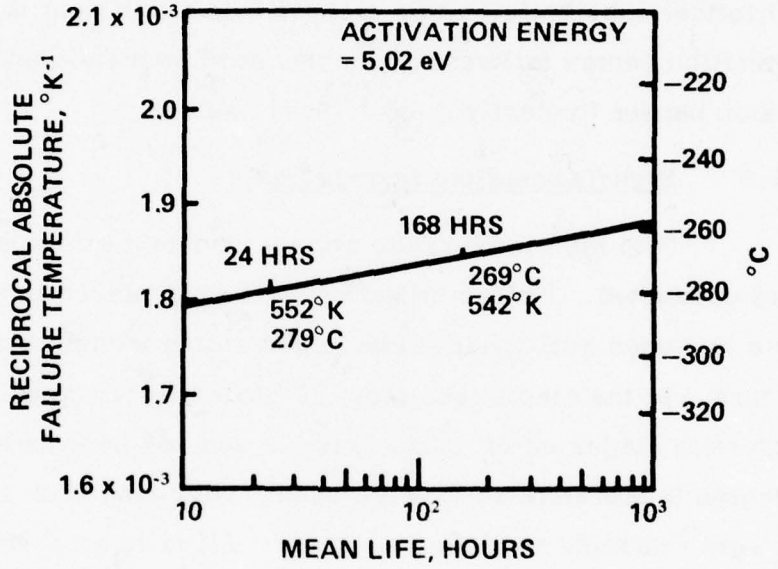


FIGURE 4-11. ACTIVE REGION TEMPERATURE VERSUS MEAN LIFE FOR MA46033 LHL IMPATT RESULTS OF RF STEP STRESS TESTS

D-16524

(straight line on probability paper) has been discarded as an early failure. Mean junction temperatures at failure of 279°C and 269°C were obtained for the 24 hour and 168 hour tests respectively. Because circumferential cracking of the top PHS pad layer is felt to be the responsible failure mechanism, and because once cracking takes place, relieving the stress, subsequent failure may not be accelerated by temperature, the regression curve obtained from the RF step stress test (Figure 4-11) should be interpreted with caution. The unusually large activation energy for this process (5.02 ev) further substantiates this claim. It is significant to note that no lower activation energy failure mechanisms such as metal penetration through the diffusion barrier (typically 2 ev) [7] were seen.

4.2 High Temperature Storage Tests

Both high temperature storage constant stress and step stress tests were conducted. Characterized devices were placed in a graphite holder in a hydrogen atmosphere furnace and stored without bias for the required time. In the step stress test, 20 diodes total, grouped in two lots of 10 each were subjected to testing with 24 and 168 hour periods respectively. Twenty degree temperature steps were used. Following each step, diode V_B and C_{TO} were measured with a curve tracer. All failures observed were to a shorted condition.

Constant stress tests were also conducted at temperatures of 200, 230, and 250°C. Each test involved 6 devices. Failure analysis revealed the condition shown in Figures 4-12 and 4-13, where a peeling and separation of the tantalum, tantalum nitride layer from the sputtered gold has occured. Evidently, shorting has taken place when the height of the wrinkle has filled the etch gap.

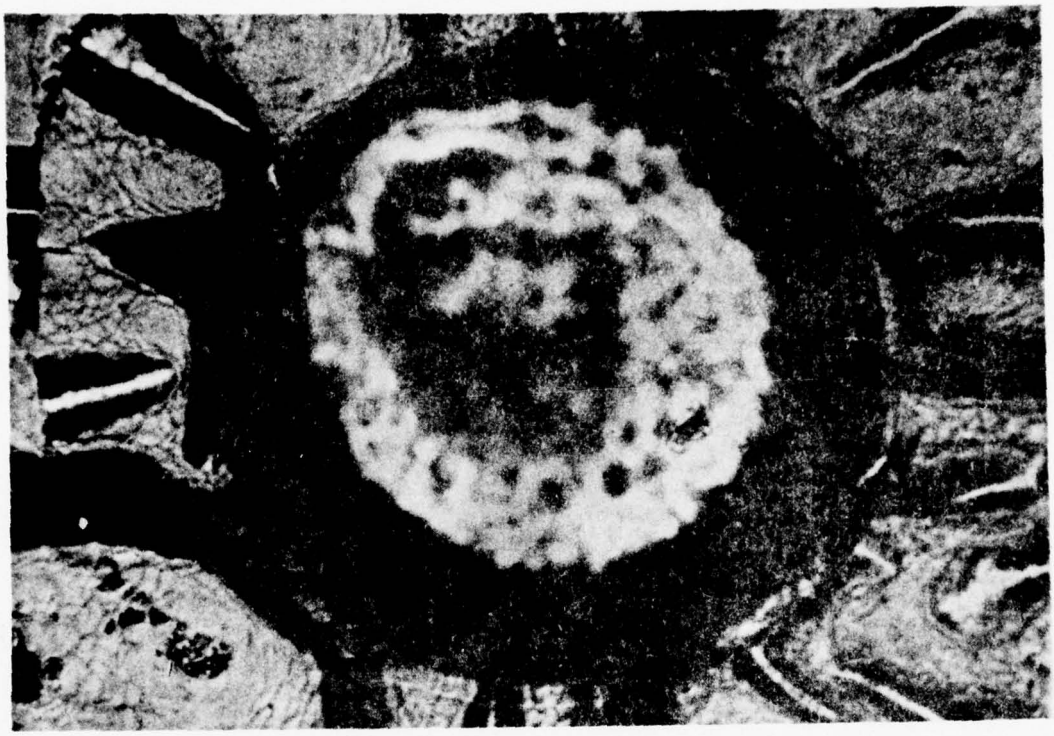


FIGURE 4-12. DEVICE 3-2 FOLLOWING 168 HOUR HIGH TEMPERATURE STORAGE STEP STRESS TEST AT A MAXIMUM TEMPERATURE AT 200°C (200X)

D-16515

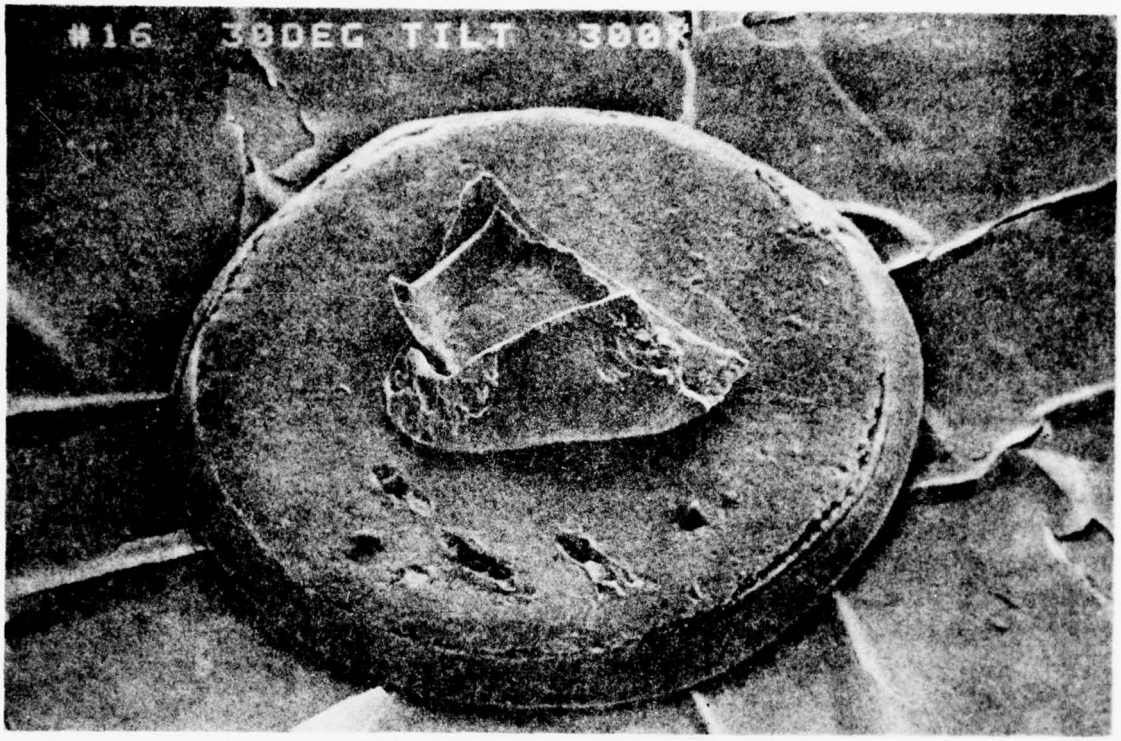


FIGURE 4-13. DEVICE 3-7 FOLLOWING 168 HOUR HIGH TEMPERATURE STORAGE STEP STRESS TEST AT 260°C MAXIMUM. DEVICE FAILED IN FINAL RF TEST.

D-16514

It was suspected that the metal separation was caused by a combination of poor adhesion between the sputtered gold and tantalum layers and a mismatch in metal thermal expansion coefficients. In order to improve adhesion, a 2000 Å layer of platinum was added between the gold and tantalum in several recent wafers. Five devices from such a wafer have presently survived 720 hours of storage at 250°C without failure. One device was opened and examined after 17 days at 250°C and showed no sign of metallization peeling (see Figure 4-14). Twenty devices from a second wafer have survived 168 hour DC burn-in with no change in operating parameters. RF performance was generally as good as that of devices from the same wafer with the former metallization method.

Reciprocal failure temperature versus percent cumulative failures from the strorage temperature stress data appears in Figure 4-15. An Arrhenius equation plot of MTTF versus storage temperature appears in Figure 4-16. The results of two constant stress tests at 200 and 230°C are also included. The data from the 250°C constant stress test is questionable since the diodes were checked for failure only once a week.

It must be stressed at this point that the data of Figure 4-13 must not be misinterpreted as device mean life versus junction temperature. In light of the failure mechanism discovered, this interpretation is not valid because in operation, the PHS pad is much cooler than the junction. Again following initial cracking, metallization lifting and subsequent diode failure probably is not accelerated according to the Eyring Arrhenius rate equation. Extrapolation of the curve of Figure 4-16 is therefore not justified.

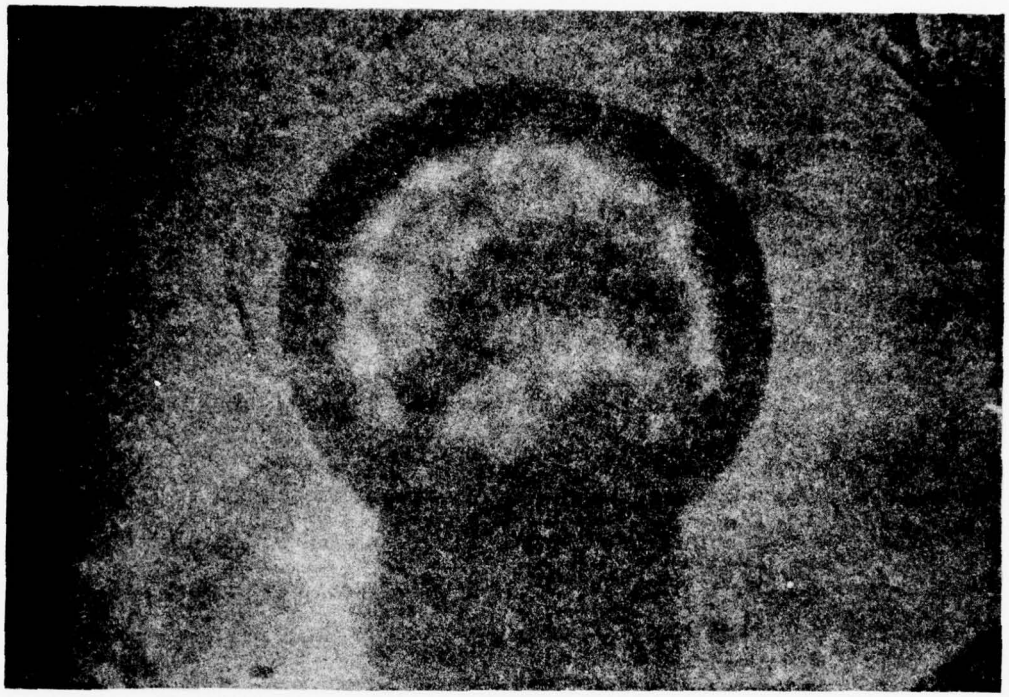


FIGURE 4-14. DEVICE WITH IMPROVED METALLIZATION FOLLOWING 17 DAYS STORAGE AT 250°C (200X)

D-16518

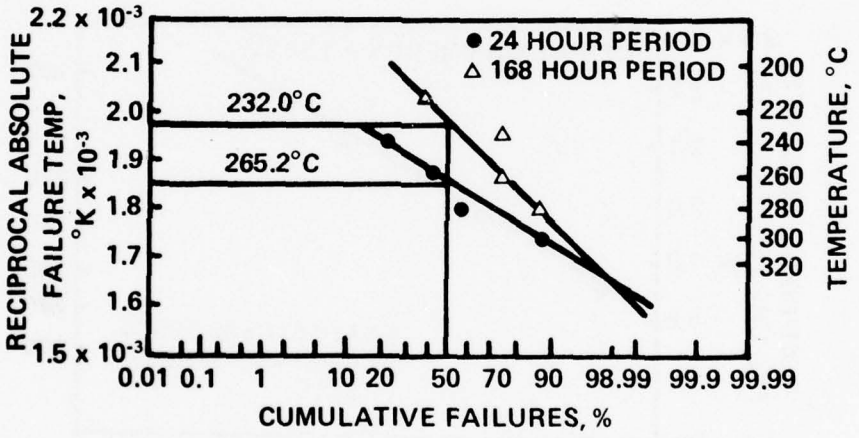


FIGURE 4-15. RECIPROCAL END OF INTERVAL TEMPERATURE VS CUMULATIVE FAILURES, 24 AND 168 HOUR STORAGE TEMPERATURE STEP STRESS RESULTS

D-16526

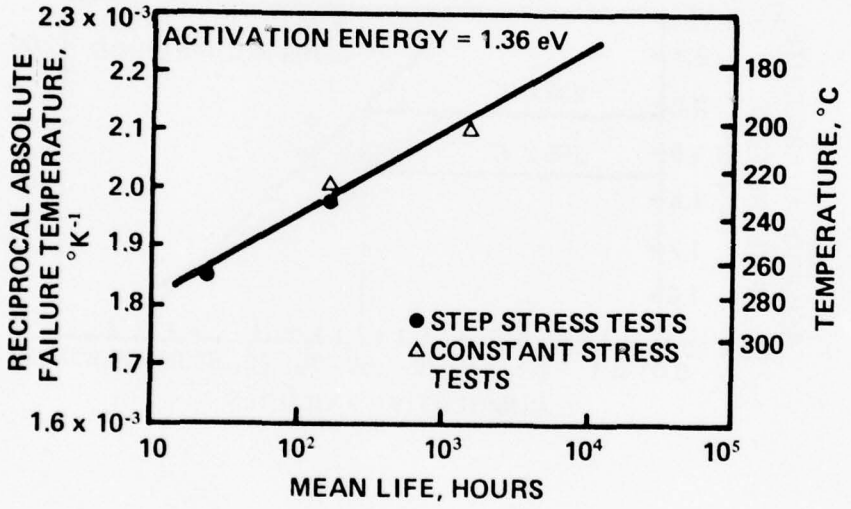


FIGURE 4-16. ACTIVE REGION TEMPERATURE VS MEAN LIFE RESULTS OF STORAGE TEMPERATURE STEP STRESS AND CONSTANT STRESS TESTS.

D-16525

5.0 LONG-TERM RF BURN-IN

5.1 Test Description

Two long-term RF burn-in tests were conducted, involving a total of twenty-four (24) devices. Because the 20 position RF burn-in rack was being used in the RF step stress tests, a test was conducted using a four-diode rack before the long-term test on the 20 position rack could be started. Both the four position and 20 position racks used the RF burn-in oscillator cavities previously described, together with control circuitry identical to that used in the RF step stress tests. Bias was supplied through 100 ohm series resistors from a constant voltage source. Some bias adjustment was possible to compensate for individual diode breakdown voltage differences, since the 100 ohms consisted of a 75 ohm fixed resistor and 25 ohm potentiometer.

Devices used in these tests had previously been screened with a 168 hour DC burn-in at 75°C case temperature and gross and fine leak tests. Thermal resistance and RF performance data were recorded before placing the units on test. Each device was again characterized after loading into an RF burn-in cavity.

5.1.1 Twenty (20) Diode Test

For the twenty (20) diode long-term test, the device temperature was controlled with a circulating liquid (ethylene glycol and water, 50%). The coolant temperature was set at 44°C, placing the diode cases at sixty-seven (67) to 76°C and the junctions at 182 to 260°C (because of varying thermal resistance). Diodes from wafer 2448-1 were used. Output power was continuously monitored by a multipoint strip chart recorder and diode detector, and has been recorded absolutely at bi-weekly intervals by replacing the diode detector with an RF power meter.

Output power varied from 2.15 watts to 2.9 watts. A summary of diode operating conditions for this test appears in Table 5-1.

5.1.2 Four (4) Diode Test

This equipment was identical to that used for the twenty (20) position test except that forced air cooling was used, placing the body cavity temperature at 40 to 47°C. In this apparatus, the diode cases were not accessable. The junction temperatures were estimated from the cavity temperatures by including 1/2°C/W for the thermal resistance from oscillator case to diode case.

Two watt output diodes from wafer 2449-1 were used in this test and operated at 52 to 56 volts, and 298 to 348 mA, with estimated junction temperatures of 194 to 230°C. Details of the test conditions used appear in Table 5-2.

5.2 Long-Term RF Burn-In Test Results

5.2.1 Twenty (20) Position Test Kit Results

The twenty (20) position long-term RF burn-in test has been operating for a total of 5500 hours (107,000 total unit hours of operation). Three diodes have failed during the test and have been replaced. The first failure occurred after 1478 hours when the device in position 9 failed to a short circuit. This device was operating at 260°C junction temperature, the highest junction temperature of any diode on the board.

Two additional devices failed simultaneously after 3498 hours, during a period when remodelling was being performed in the vacinity of the burn-in rack. It is theorized that the rack was unplugged and reconnected quickly before the time delay relay protective

POSITION NUMBER	V_o (Volts)	I_o (mA)	P_o (mW)	θ ($^oC/W$)	T_J (^oC)
1	48.5	290	2300	14.3	255
2	44.0	365	2600	12.1	242
3	46.0	300	2350	12.8	216
4	45.5	345	2700	12.2	238
5	48.5	305	2500	9.9	188
6	46.0	345	2500	12.2	233
7	46.0	340	2900	11.6	222
8	45.5	350	2200	11.3	225
9	47.0	325	2150	13.9	260
10	44.0	355	2450	11.6	227
11	46.5	340	2800	10 4	213
12	41.5	380	2000	9.2	203
13	49.0	300	2750	9.3	184
14	39.5	382	2150	8.5	186
15	45.0	360	2500	10.4	217
16	46.5	335	2400	9.0	193
17	46.0	343	2300	9.2	193
18	48.0	320	2150	9.7	198
19	49.5	300	2550	9.2	182
20	42.0	390	2200	11.0	229

TABLE 5-1 INITIAL OPERATING CONDITIONS FOR LONG-TERM RF BURN-IN TEST, WAFER 2448-1, 20 POSITION TEST KIT

WAFER NUMBER	POSITION NUMBER	V_o (Volts)	I_o (mA)	P_o (mW)	θ ($^oC/W$)	T_J (^oC)
2449-1	11	52.1	302	2200	9.8	194
	12	55.5	348	1700	8.7	212.5
	13	51.9	298	2550	10.8	201
	14	55.5	301	2040	11.6	230

TABLE 5-2 INITIAL OPERATING CONDITIONS FOR FOUR POSITION RF BURN-IN TEST

circuits had time to react. In this case, the power supply turn-on transient would be applied directly to the diodes under test. Because of the questionable conditions at failure, these two failures are not included in data for MTBF determination.

The device failing at 1478 hours (diode 9-11) has been submitted to failure analysis. A SEM micrograph of the diode appears in Figure 5-1. No cracking or peeling of the PHS (plated heat sink) pad metallization is evident, nor is deterioration of the back contact seen. A conducting channel has formed, apparently within the interior of the device, as a burn mark can be seen in the back contact metallization removed from the edge.

Very little change has occurred in diode operating parameters during the life test. A slight increase in operating voltage and decrease in operating current has occurred, with output power remaining essentially unchanged. Data recorded in the RF burn-in cavities at the start of the test and at the 5000 hour point appears in Table 5-3. The devices have not been removed for more complete characterization. Some variability in this data can be attributed to small adjustments made in the cavity tuning during the test. Occasionally, it was found that one of the diodes had switched modes and the power output had dropped with an accompanying change in operating voltage and current. In these cases, a slight adjustment of the teflon tuning screw was sufficient to regain the original conditions of operation. However, output frequency could have changed slightly as it was not monitored during RF burn-in.

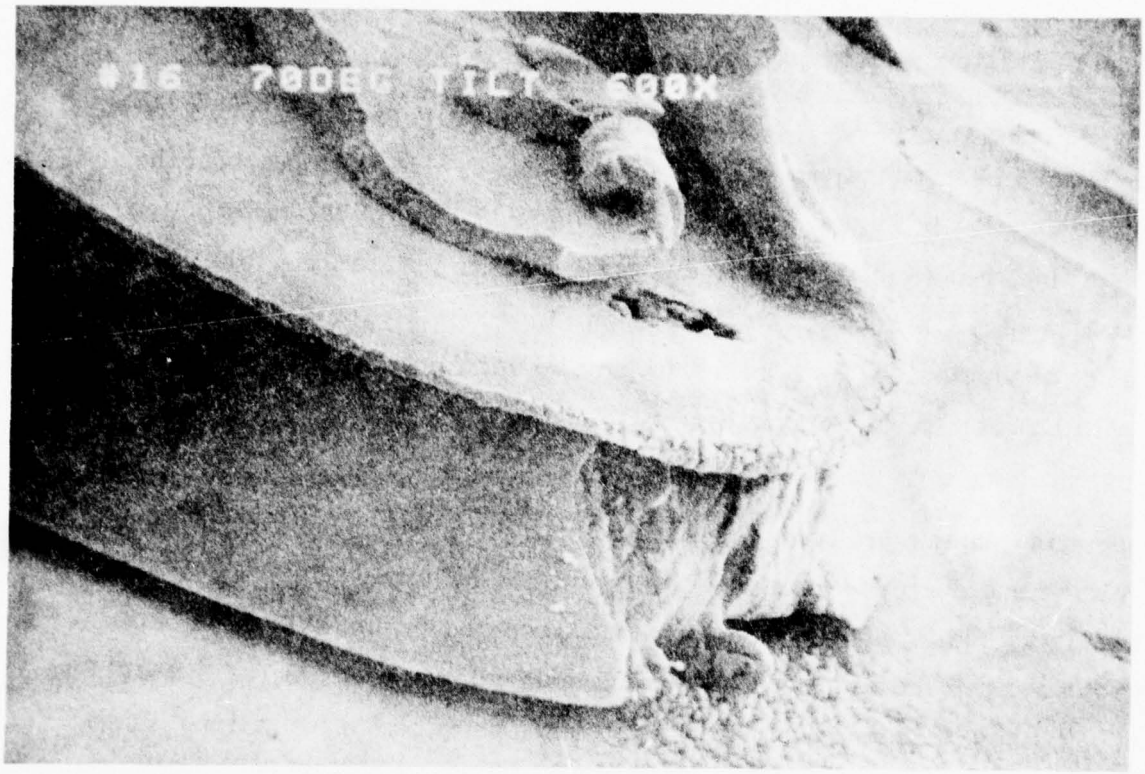


FIGURE 5-1. DEVICE 9-11 FOLLOWING FAILURE AFTER 1478 HOURS OF OPERATION ON LONG TERM RF BUILT-IN WITH T_J = 260°C

D-16532

HOURS AT FAILURE	POSITION NUMBER	V_o, Volts		I_o, mA		P_o, mW	
		INITIAL	FINAL	INITIAL	FINAL	INITIAL	FINAL
	1	48.5	51.0	290	280	2300	2350
	2	44.0	47.6	365	315	2600	2300
	3	46.0	46.7	300	300	2350	2200
	4	45.5	48.5	345	310	2700	2750
	5	48.5	51.7	305	268	2500	2250
	6	46.0	50.2	345	290	2500	2460
3948	7	46.0	47.2	340	321	2900	2770
	8	45.5	47.4	350	325	2200	2100
1478	9	47.0	48.4	325	317	2150	2150
	9 Reloaded	51.5	51.6	260	300	1600	2150
	10	44.0	48.6	355	300	2450	2000
	11	46.5	48.1	340	320	2800	2900
	12	41.5	43.9	380	350	2000	2000
	13	49.0	50 5	300	285	2750	2900
	14	39.5	43.0	382	345	2150	2300
	15	45.0	51.2	360	275	2500	2480
	16	46.5	48.1	335	315	2400	2250
	17	46.0	49.2	343	300	2300	2400
3948	18	48.0	49.3	320	300	2150	2150
	19	49.5	49.9	300	220	2550	2550
	20	42.0	46.2	390	350	2200	2400

TABLE 5-3 DIODE OPERATING PARAMETER CHANGE DURING 5000 HOUR RF BURN-IN TEST, WAFER 2448-1

5.2.2 Results From the Four Position RF Burn-In Test

During lthis test, four devices from lot 2449-1 survived 3900 hours of operation (15,500 total unit hours) without failure. Following the test, the devices were completely characterized (see Table 5-4) and doping profiles were remeasured. The profiles were essentially unchanged. The initial and final test data presented in Table 5-4 were measured in the standard test cavity, not in the individual burn-in test cavities, and, because of the use of a precision sliding short a higher initial power was obtained in the standard test cavity (compare Table 5-2).

5.3 Device MTBF Determination

In total, the long-term RF tests have accumulated 122,500 unit hours of operation with one failure. At the 90% confidence limit, the MTBF for devices of this type is no less than 41000 hours. As the long-term RF burn-in test continues to accumulate unit hours of operation without additional failures, this estimate will increase.

POSITION NUMBER	CONDITION	V_B (Volts)	C_{T0} (pF)	V_o (Volts)	I_o (mA)	P_o (mW)	f_o (GHz)
11	Initial	22.1	11.5	52.4	280	2300	8.38
	Final	23.4	11.8	51.3	258	2200	8.45
12	Initial	22.5	12.0	51.6	300	2500	8.34
	Final	23.4	12.2	50.2	308	2500	8.40
13	Initial	22.4	13.4	56.5	300	2300	8.31
	Final	23.8	13.9	55.3	298	2300	8.34
14	Initial	24.2	14.1	55.6	345	2300	8.30
	Final	26.2	14.5	55.8	292	2300	8.38

TABLE 5-4 DIODE RF AND DC CHARACTERISTICS BEFORE AND AFTER 3900 HOUR RF BURN-IN TEST, WAFER 2449-1

6.0 SPECIAL TESTS

6.1 Test Description

The special testing sequence is summarized in (Figure 6-1) with the exception of the corrosion resistance test, these experiments were conducted using units that had been passed through DC burn-in for 168 hours, gross and fine hermeticity tests, and RF and DC characterization.

6.1.1 Transient Overstress Test (Pulsed Burn-Out)

Transient overstress tests were conducted by applying pulsed bias current to devices from a fast rise, low duty cycle 50 Ohm output impedance pulse generator. A 200 nsec, 100 Hz repetition rate pulse was used, to avoid device heating. Five devices mounted in the waveguide test cavity were stressed to failure by increasing the pulse voltage, while monitoring pulsed output power. Five units were similarly tested but with worst case RF mismatch (short circuit load). An additional ten units were pulsed to failure, but in a non-oscillating condition. Oscillations were suppressed by installing sections of waveguide filled with graphite plungers on either side of the waveguide diode mount.

6.1.2 Switching Transient Test

On off power cycling was used to investigate the ability of the devices to withstand switching transients. The circuit of (Figure 6-2) was employed. No special precautions were taken to eliminate switching transients other than use of low inductance resistors in the bias network. An automatic timer was used to turn the system on and off every two minutes. The diodes were mounted in cavity oscillators of the type previously described. Each oscillator output was monitored through an attenuator by a diode detector driving one channel of a multi-point recorder.

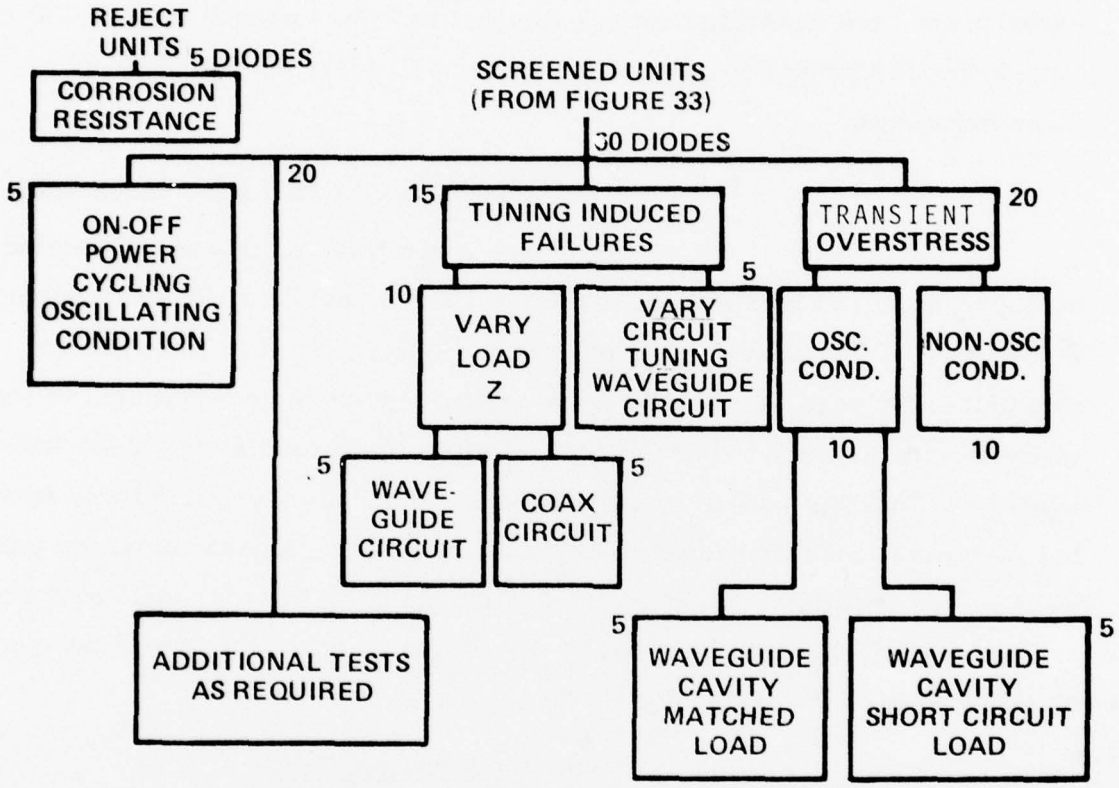


FIGURE 6-1. SUMMARY OF SPECIAL TESTS

D-14021A

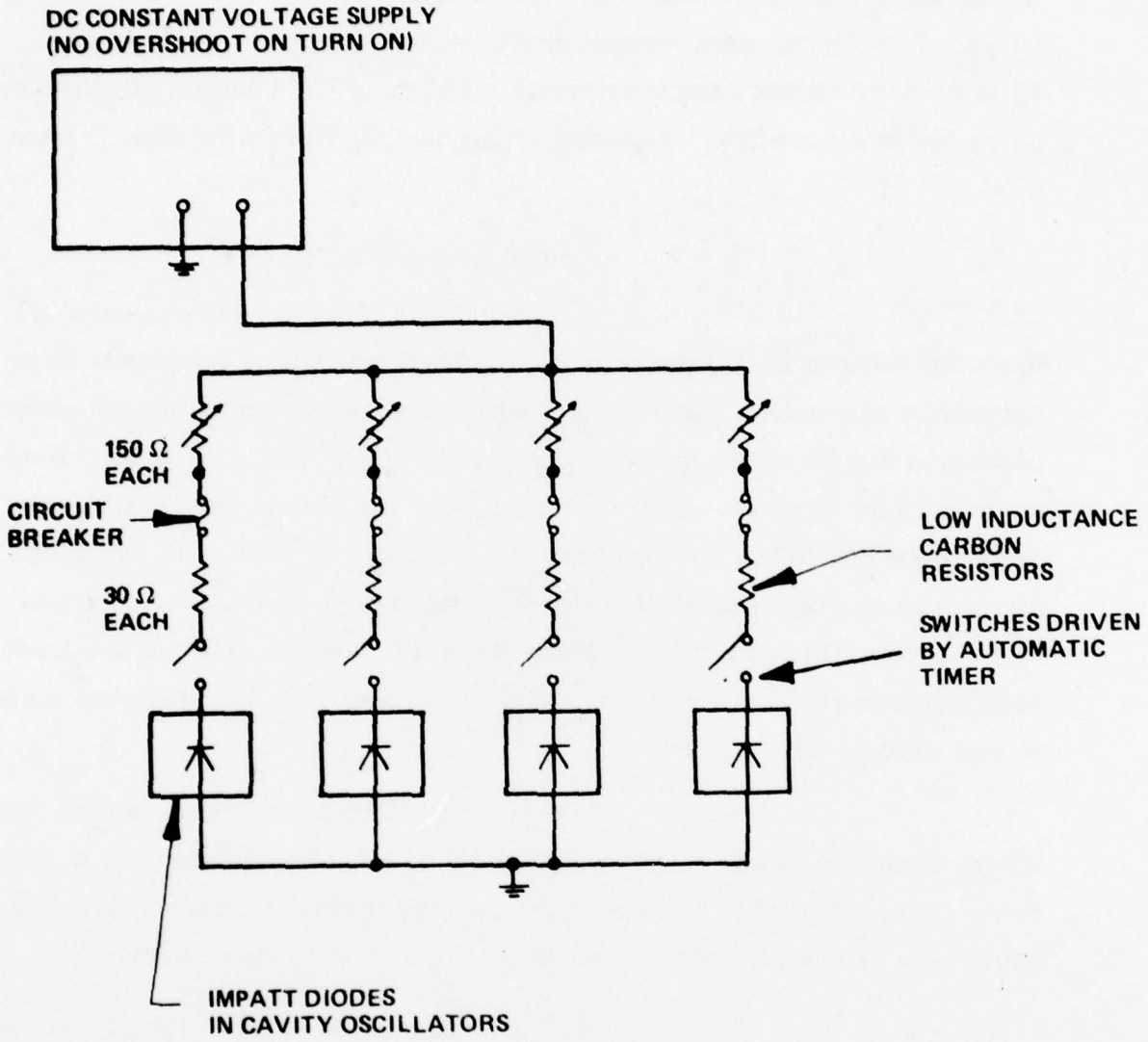


FIGURE 6-2. EQUIPMENT USED IN IMPATT DIODE SWITCHING TRANSIENT STUDY

D-14016A

In this way, the time of failure or change in output power could be determined. Five diodes were tested, in this manner, and were operated at 39 to 41°C oscillator case temperature, (182 to 196°C junction temperature) using forced air cooling. Two watt output devices from wafer 2448-1 were used.

6.1.3 Tuning Induced Failure Test

Tuning induced failures were analyzed by operating devices at full power in the standard test cavity connected to an adjustable mismatch. The system used involved a waveguide switch which connected the oscillator either to the usual test kit or to a precision attenuator and sliding short. After tuning up the diode, the switch was thrown (with power off) to the sliding short and attenuator position. By reducing attenuation in steps and sliding the short through at least one half of the guide wavelength at each attenuator setting, the device could be presented with increasingly severe mismatches of all phases. Five diodes were tested in this experiment.

In a second tuning induced failure test, five diodes operating at full power in the waveguide cavity were detuned to zero power using the sliding short which formed the test cavity back wall. The cavity was connected to the standard test line for this experiment.

6.1.4 Corrosion Resistance Test

Five electrical reject devices were passed through MIL-STD-750, Method 1041.1 Salt Atmosphere Test. A 35°C 24 hour testing cycle was used. No discoloration or deterioration of the package plating occurred.

6.2 Test Results

The results of the special testing program (except corrosion resistance) are summarized in Table 6-1. More detailed descriptions of the test results follow.

6.2.1 Transient Overstress Test

In the pulsed burn-out tests (see Tables 6-2 and 6-3) a 200 nanosecond, 100 Hz pulse of variable amplitude and 50 ohm output impedance was applied to the diode under test. In the first test, the devices were operated in the standard waveguide test cavity and first adjusted for maximum pulsed output power. The duty cycle was increased to 10% for this test. Then duty was decreased to 2×10^{-5} and the voltage increased until diode failure resulted. In general, from 1.0 to 1.6 A at 62 to 74 volts were required. When failure occurred, the diode impedance suddendly dropped, resulting in a drop in voltage and increase in current. If the bias pulse was immediately removed at the first sign of this condition, the device could be saved and did not become a DC short, (devices 8-6 and 8-7). If the high current condition was allowed to persist, a DC short always resulted. Similar results were obtained when a short circuit load was used instead of the waveguide test kit (matched load). Because the diodes were not generating power at failure, this result is understandable.

Somewhat higher failure voltages (62 to 80 volts) were observed when oscillations were suppressed by using a graphite loaded test fixture (see Table 6-3). This would indicate that some oscillations were occurring in the previous tests, although no output power was seen.

TEST DESCRIPTION	INITIAL NO. DEVICES	FINAL NO. DEVICES	AVERAGE FAILURE CONDITIONS
I On/Off Cycling, Oscillating Condition: 85,000 Cycles, 50°C Diode Case Temp.	5	5	No Failures
II Tuning Induced Failures:			
A. Short Circuit Load at Full Output	5	5	No Failures
B. Vary Circuit Tuning from Full Output to Zero Output	5	5	No Failures
III Transient Overstress Pulse to Failure (100 nsec pulse, 50 ohm impedance)			
A. Oscillating Condition	10	0	66 V, 1.4 A Peak
B. Non-Oscillating Condition	10	0	70 V, 1.35 A Peak

TABLE 6-1 SUMMARY OF SPECIAL TEST RESULTS

DEVICE DEVICE	P_o, Peak (Watts)	V_o, Peak (Volts)	I_o, Peak (mA)	f_o (GHz)	COMMENT
PART 1: MATCHED LOAD THROUGHOUT					
8-3	3.1	45	920	11.35	
	0	70	1000	---	Failed Shorted
8-5	2.25	40	900	11.3	
	0	64	1600	---	Failed Shorted
8-6	2.8	45	680	11.55	
	0	62	1600	---	Recovered
8-7	2.75	47	640	11.3	
	0	68	1300	---	Recovered
8-8	2.95	43	680	11.15	
	0	74	1400	---	Failed Shorted
PART 2: SHORT CIRCUIT LOAD DURING BURN-OUT TEST					
8-9	2.45	40	800	11.45	
	0	60	1500	---	Failed Shorted
8-10	2.75	47	640	11.35	
	0	70	1300	---	Failed Shorted
8-11	2.75	54	700	10.75	
	0	70	1400	---	Failed Shorted
8-12	2.80	54	630	10.9	
	0	60	1400	---	Failed Shorted
8-13	2.55	45	630	11.5	
	0	60	1600	---	Recovered

TABLE 6-2 TRANSIENT OVERSTRESS TEST SUMMARY, WAVEGUIDE OSCILLATOR -- LOT 2448-1

AD-A067 223 MICROWAVE ASSOCIATES INC BURLINGTON MASS F/G 9/1
RELIABILITY STUDY OF HIGH EFFICIENCY GAAS IMPATT DEVICES.(U)
JAN 79 J L HEATON F30602-76-C-0409
UNCLASSIFIED RADC-TR-78-203 NL

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DEVICE	V_{peak}	I_{peak}	COMMENT
8-14	66	1250	Moving graphite load caused Failure - Short
8-15	90	1600	Failure - Short
8-16	80	1600	Failure - Short
7-10	64	1250	Recovered
7-11	62	1200	Failure - Short

TABLE 6-3 TRANSIENT OVERSTRESS TEST SUMMARY
OSCILLATIONS SUPPRESSED, LOT 2448-1

6.2.2 Switching Transient Test

The switching transient test operated with a two minute on and two minute off cycle for 5500 hours without device failure or significant change in operating parameters. The test was powered from the same power supply used for the four position long-term RF burn-in experiment. When this power supply malfunctioned, the devices in the switching transient test were destroyed also. Initial and final test data taken with the devices in the switching transient apparatus appears in Table 6-4. During the course of the test, the apparatus was moved twice necessitating complete shutdown of the test. The test was again shut down following the annual vacation plant closing at Microwave Associates. Following each restarting, it was necessary to readjust cavity tuning, probably because of jaring and slight motion of the adjustments during the move. Upon turn-on, the power supply was reset to the original value. Because of this moving, some variability in the data taken during the test would be expected.

6.2.3 Tuning Induced Failure Test

The tuning induced failure test results are summarized in Table 6-5. Two (2) tests were conducted involving six (6) devices operated in the standard waveguide test circuit. In the first test, the diodes, operating at full output power, were detuned to minimum power using the waveguide sliding short which forms the cavity back wall. No failures occurred.

In the second test, the oscillator containing the diode was connected to a waveguide switch. One output port lead to the usual test kit while the other was connected to a precision attenuator and sliding short. After adjusting diode tuning for maximum output

DIODE	V_o, Volts		I_o, mA		P_o, mW	
	INITIAL	FINAL	INITIAL	FINAL	INITIAL	FINAL
1	46.6	43.8	325	290	2000	1950
2	51.1	54.5	290	260	1750	1850
3	50.4	47.6	335	278	2000	2250
4	48.7	49.2	315	253	2050	2050
5	50.7	53.4	305	248	2200	2500

TABLE 6-4 INITIAL AND FINAL OPERATING PARAMETERS FOR RF BURN-IN SWITCHING TRANSIENT TEST, LOT 2448-1

DIODE	INITIAL			WITH SHORT CIRCUIT LOAD		COMMENT
	V_o (Volts)	I_o (mA)	P_o (mW)	V_o (Volts)	I_o (mA)	
8-3	44.9	345	3000	43.1	363	Pass
8-5	45.6	379	2950	44.7	383	Pass
8-6	48.3	323	2850	47.8	329	Pass
8-7	49.9	323	2900	49.0	332	Pass
8-8	48.6	360	3500	45.7	370	Pass

NOTE: Operating parameters with short circuit load were recorded with the sliding short set for minimum DC voltage across the diode under test

TABLE 6-5 RESULTS OF TUNING INDUCED FAILURE TEST USING SHORT CIRCUIT LOAD

while connected to the waveguide test kit, the bias was turned off and the waveguide switch thrown to the second position. With bias reapplied, the short was moved through one-half of a guide wavelength while the attenuation was reduced in steps. No diode failures occurred even with 0 dB attenuation.

During these tests, bias was supplied from a constant voltage source and 100 ohm series resistor. It was felt that had bias been supplied by a current regulator, the probability of diode failure would have been higher. Accordingly, the short circuit load test was repeated with bias supplied from a current regulator. The power supply voltage into the regulator was fixed at 58.4 volts, while the diode operating voltage was 47.4 volts. The regularor circuit (see Figure 3-6) maintains a constant five volt differential, resulting in a 6 volt compliance voltage.

Similar test results were obtained using the current regulator to supply diode bias. That is, no failure resulted in five devices examined. Diode operating voltage dropped from about 47 volts to 42 volts when the short circuit load was connected.

7.0 CONCLUSION

A comprehensive reliability study of platinum Schottky low-high-low structure gallium arsenide IMPATTs has been carried out. Early failure region tests indicated DC burn-in at normal input power dissipation to be the best choice as an early failure screen. Long term RF burn-in tests have been established, a minimum MTBF of 40,000 hours for diodes operated at 14 watts dissipation and 70°C case temperature. Average device junction temperature was 215°C. Device failure on high temperature storage has been attributed to separation of the top metallization layers. This mechanism may invalidate the RF step stress Arrhenius rate law. Penetration of gold into the active region was not a cause of failure and no change in doping profile occurred during RF step stress. Special testing has demonstrated the immunity of these low-high-low IMPATTs to damage from on - off switching or load mismatch.

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