AD-A067 980 RCA ADVANCED TECHNOLOGY LABS CAMDEN N J F/G 9/5
RADIATION HARDENED CMOS/SOS CODE GENERATOR FOR SPACE APPLICATIO--ETC(U)
OCT 78 J I PRIDGEN, H W KAISER N00014-75-C-0709

UNCLASSIFIED NL

1 OF 2
AD
A067980

(12) LEVEL II

RADIATION HARDENED CMOS/SOS CODE GENERATOR FOR SPACE APPLICATIONS

Final Report November 1976 - May 1978

October 1978

AD A067980

Distribution Unlimited

This research was sponsored by the Defense Nuclear Agency under Subtask TD033.

DDC
RECEIVED
MAY 1 1979
A

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

Prepared for

Director
Naval Research Laboratory
4555 Overlook Avenue, SW
Washington, DC 20375

DDC FILE COPY

Prepared by

Advanced Technology Laboratories
Government Systems Division
RCA
Camden, NJ 08102

79 04 27 002

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Navy position, unless so designated by other authorized documents.

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) (6) Radiation Hardened CMOS/SOS Code Generator for Space Applications.	(9) 5. TYPE OF REPORT & PERIOD COVERED Final rept. November 1976 - May 1978
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) (10) J. I. Pridgen, H. W. Kaiser	(15) 8. CONTRACT OR GRANT NUMBER(s) N00014-75-C-0709
9. PERFORMING ORGANIZATION NAME AND ADDRESS Advanced Technology Laboratories Government Systems Division RCA, Camden, N.J. 08102	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Subtask TD033
11. CONTROLLING OFFICE NAME AND ADDRESS (11) Director Naval Research Laboratory 4555 Overlook Ave., SW, Washington, DC 20375	12. REPORT DATE October 1978
	13. NUMBER OF PAGES 98
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (12) 108p.	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Distribution unlimited.

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

This research was sponsored by the Defense Nuclear Agency under Subtask TD033.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Radiation hardened LSI
LSI arrays
Code generator
CMOS/SOS LSI technology
GPS baseband generator

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The primary objective of this program was to design, fabricate, and test a radiation hardened LSI code generator array suitable for use in the NAVSTAR Global Positioning System (GPS). The LSI array developed is a mask programmable custom cell CMOS/SOS array which was fabricated using both standard processing and radiation hardened processing.

→ (over)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

405 561

LB

Designated TCS102, this array contains two 12-stage pseudorandom sequence generators and a 12-stage synchronous counter along with associated control logic.

The Precision (P) Code Generator in the GPS operates with a fixed 10.23-MHz clock. The radiation hardness objectives for this development effort were a total dose hardness of 10^6 rads(Si), with a minimum transient upset level of 2×10^{10} rads(Si)/s, with a goal of 10^{11} rads(Si)/s. Extensive computer simulations were made to predict circuit performance over the full range of total dose radiation and ambient temperature to +125°C. Design techniques ~~employed~~ used to obtain high speed include the elimination of long signal paths, the retiming of all control signals on the array, optimizing device widths for maximum speed, and designing all devices with a channel length of 6.25 μm. Radiation hardening techniques ~~employed~~ included: clamped channels on P transistors, elimination of transmission gates from the design, use of gated diodes for the input protection, and the restriction of stacked devices to a maximum of three. The TCS102 was processed using the RCA Solid State Technology Center radiation hardened gate oxide process. The design was initially verified by processing the masks with the standard I^2(N/N) process.

Following the radiation hardening processing and subsequent device and array characterization tests, the arrays were radiation tested by NRL. The tested parts met or exceeded the minimum hardness levels established by NRL for the parts.

The analysis of the code generator array indicated a worst-case speed problem in meeting the 10.23-MHz requirement at a temperature of 125°C. However, performance results showed a loss in speed less than the worst-case prediction for both temperature and radiation effects.

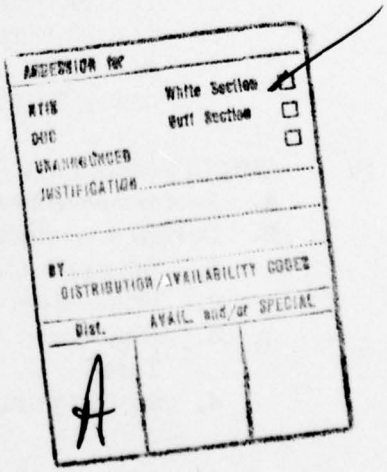
Testing of the array at the NRL cobalt 60 facility showed correct operation of the code generator after 10^6 rads(Si) with about a 15% decrease in speed. Some arrays were functional after 3×10^6 rads(Si), but at reduced speed. Transient upset tests performed at NRL using a 40-MeV LINAC showed an upset level near 10^{11} rads(Si)/s for a 50-ns pulse and 6 to 8×10^{10} rads(Si)/s for a longer 1-μm pulse. This testing demonstrates the megarad hardness and high transient upset level of the TCS102 code generator array. The combination of radiation hardened processing results in hardened CMOS/SOS LSI arrays capable of operation at 10 to 20 MHz.

FOREWORD AND ACKNOWLEDGMENT

This program was administered under the direction of Dr. L. J. Palkuti, technical program director, Naval Research Laboratory, Washington, DC. The authors gratefully acknowledge the suggestions and the assistance provided by Dr. Palkuti, who also personally supervised the testing of parts under radiation.

The authors wish to acknowledge the assistance of H. Borkan, J. Fabula, D. Woo, and S. Policastro, of the RCA Solid State Technology Center (SSTC) in Somerville, NJ, in developing the silicon gate radiation hardened process used on this program. All parts fabricated on this program were processed by SSTC.

The authors also wish to acknowledge the contribution of W. A. Boyd, who was responsible for all the digitizing and checkplotting of the custom-design cells and the array.



79 04 27 002

TABLE OF CONTENTS

Section		Page
I	INTRODUCTION	1
II	SYSTEM CONSIDERATIONS	4
III	ARRAY PARTITION AND INTERFACE	7
	A. General	7
	B. XA Code Generator	7
	1. Code Generator Structure	7
	2. Serial Register Extension	12
	3. State Decode Logic	12
	4. Clock and Control Logic	12
	C. XB Code Generator	17
	1. Code Generator Structure	17
	2. State Decode Logic	17
	3. Clock and Control Logic	17
	D. Synchronous Counter	19
	1. Counter Structure	19
	2. Counter Output Register	22
	3. Count Decode Logic	22
	4. Counter Input Logic	22
	E. Mask Programmable Options Used	24
	1. TCS102A	24
	2. TCS102B	24
	F. Input/Output Summary	28
	1. TCS102 Inputs	28
	2. TCS102 Outputs	29
	3. Packaging	30
	4. Power Requirements	30
IV	CIRCUIT DESIGN AND SIMULATION	33
	A. Performance Requirements	33
	B. Design Techniques Employed to Meet Requirements	34
	1. Substrate Clamps on Stacked P Transistors	34
	2. Elimination of Transmission Gates	36
	3. Limiting of Stacked Devices to a Maximum of Three	36
	4. Speed Optimization at the End of Total Dose	37

TABLE OF CONTENTS (Continued)

Section		Page
	C. Simulation of Critical Circuits	37
	1. Circuit Models Used in Simulation	38
	2. Code Generator Stage	40
	3. Clock Control Logic and Driver	45
	4. Counter Stage	47
	5. Output Driver	48
	6. Input Register Setup	49
	7. Use of Circuit Simulation Results	49
	D. Predicted Speed Performance	50
	E. Input Protection	51
V	RADIATION HARDENED PROCESS	55
	A. Standard CMOS/SOS I^2(N/N) Process	55
	B. Radiation-Hardened CMOS/SOS Process	57
VI	ARRAY PERFORMANCE	61
	A. Room-Temperature Preradiation Characterization	61
	1. Maximum Speed of the Code Generator	62
	2. Output Propagation Delay	63
	3. Output Rise and Fall Times	67
	4. Power Dissipation	67
	5. Input Clock Waveform Requirements	72
	6. Input Setup Times	72
	B. Performance Over Temperature	73
	1. Maximum Speed of the Code Generator	73
	2. Output Propagation Delays	74
	3. Power Dissipation	74
	C. Radiation Performance	76
	1. Total Dose Testing	76
	2. Transient-Radiation Upset	79
VII	TEST DEVICES	80
	A. Input Protection Gated Diodes	80
	B. Inverters	82
	C. NOR Gate	82
	D. Memory Element	82
VIII	CONCLUSIONS AND RECOMMENDATIONS	84
IX	REFERENCES	86
	APPENDIX	87

LIST OF ILLUSTRATIONS

Figure		Page
1-1	Microphotograph of radiation hardened code generator array TCS102	2
2-1	P code generator	5
3-1	TCS102 code generator	8
3-2	Two equivalent forms for a pseudorandom sequence generator	10
3-3	XA code generator	11
3-4	Phase adjustment timing	14
3-5	X1 code generator timing	15
3-6	X2 code generator timing	16
3-7	XB code generator	18
3-8	Epoch counter	20
3-9	Logic diagram of a counter stage	21
3-10	TCS102A sequence generators	25
3-11	TCS102B sequence generators	27
4-1	Two-input NOR showing clamps to P device channel	35
4-2	R-CAP Model of N transistor used in simulating radiation transient effects	40
4-3	Register circuit investigated in transient analysis	42
4-4	Register simulation with transient radiation pulse at time of clocking	43
4-5	Register simulation with a long transient radiation pulse	44
4-6	XA sequence generator clock driver	45
4-7	XA clock control logic	46
4-8	Pulse-forming circuit	47
4-9	TCS102 input protection	53
4-10	Input pad with arc gap protection	54
5-1	Cross-sectional view of I^2(N/N) CMOS/SOS silicon-gate process	56
5-2	Single-epi double-implant substrate preparation	58
5-3	P+ gate CMOS/SOS radiation hardened process	60
6-1	TCS102B code generator speed vs. operating voltage	63
6-2	Delay path for XA, XB, XA1-XA12 and XA EPOCH outputs	63

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
6-3	Delay path for CNT1-CNT12 outputs	64
6-4	Clock to XA output delay TCS102B code generator	66
6-5	Clock to XB output delay TCS102B code generator	66
6-6	Clock to XA output delay	67
6-7	XA output rise and fall times vs. load	68
6-8	TCS102B leakage current vs. V_{DD} voltage	68
6-9	TCS102 10-volt leakage current distribution measured at room temperature	69
6-10	TCS102B power dissipation	70
6-11	Maximum code generator speed vs. temperature	74
6-12	TCS102B leakage current increase with temperatures	76
6-13	Performance curves for the code generator	77
6-14	The threshold between acceptable operation and transient upset for the code generator as a function of the irradiation pulse width	78
7-1	TCS102 test devices	81

LIST OF TABLES

Table		Page
3-1	Counter Initialization Steps	23
3-2	TCS102A and TCS102B Mask Programmable Options Used	26
3-3	TCS102 Package Pin Identification for 40-Lead DIP	31
3-4	TCS102 Package Pin Identification for 48-Lead LHP	32
4-1	Parameters Used in R-CAP Simulation	38
4-2	Postradiation Parameters Used in Simulation Comparison	39
4-3	Ten-Volt Propagation Delay Comparison Using Different Sets of Device Parameters	39
4-4	Simulated Performance of Code Generator Register at 10 V	41
4-5	Simulated Performance of Code Generator Exclusive-OR at 10 V	41
4-6	Logic Voltages Observed in Radiation Transient Simulation of Register	42
4-7	Predicted 10-V XA Clock Driver Performance	45
4-8	10V Simulated Delay to XA CLK Control Output	47
4-9	10-V Simulated Delays in Counter Logic	48
4-10	10-V Simulated Delays in Counter Output Register	48
4-11	Simulated Performance of Output Drivers at 10 V with a 15-pF Load	49
4-12	Simulated Input Register Setup Times	49
4-13	Maximum Internal 10-V Path Delays for TCS102	51
4-14	Simulated 10-V Setup and Output Delay Times for TCS102	52
6-1	TCS102B Chips Used in Characterization Tests	61
6-2	TCS102B Maximum Room-Temperature Clock Frequency (V_{DD} = 10 V)	62
6-3	TCS102B Maximum Room-Temperature Clock Frequency (V_{DD} = 5 V)	62
6-4	Clock to Output Signal Propagation Delay at 10 V	64
6-5	Five-Volt Output Propagation Delay for Lot S1739	65
6-6	Dynamic Power Dissipation for TCS102B Code Generator	70
6-7	TCS102B Power Dissipation with Counter only Being Operated	71
6-8	TCS102B Input Clock Duty Cycle	72
6-9	TCS102B Clock Maximum Transition Time	73
6-10	Ten-Volt Clock-to-Output Delay as a Function of Temperature	75
6-11	Ten-Volt Dynamic Power Increase with Temperature for TCS102B Producing Both XA and XB Codes	75
7-1	TCS102X Test Inverters	82
7-2	Memory Element Bias Conditions at Time of Radiation Pulse	83

Section I

INTRODUCTION

The primary objective of this program was to design, fabricate, and test a radiation hardened LSI code generator array suitable for use in the NAVSTAR Global Positioning System (GPS). The LSI array developed (Fig. 1-1) is a mask programmable custom cell CMOS/SOS array which was fabricated using both standard processing and radiation hardened processing.

The code generator array, designated TCS102, is designed for use in the precision (P) code generation baseband subsystem in the NAVSTAR GPS. The TCS102 contains two 12-stage pseudorandom sequence generators and a 12-stage synchronous counter along with associated control logic. Metal masks were generated for each of the two versions used in the P coder, designated the TCS102A and TCS102B. All arrays fabricated and tested under this contract have been of the TCS102B type. A third metal mask, not generated on this program but considered in the design, will allow the array to produce the C/A code required by the GPS.

The design goal was to meet the dual objectives of high speed and radiation hardness. The code generator array in the P coder operates with a fixed 10.23-MHz clock. The radiation hardness objectives for this development effort were a total dose (gamma) hardness of 10^6 rads(Si) and a minimum transient upset level of 2×10^{10} rads(Si)/s, with a goal of 10^{11} rads(Si)/s. Extensive computer simulations were made to predict circuit performance over the full range of total dose radiation and ambient temperature to +125°C. Design techniques employed to obtain high speed include the elimination of long signal paths, the retiming of all control signals on the array, optimizing device widths for maximum speed, and designing all devices with a channel length of 6.25 μm (0.25 mil). Radiation hardening design techniques employed included clamped channels on P transistors, the elimination of transmission gates from the design, gated diodes for the input protection, and the restriction of stacked devices to a maximum of three. The TCS102 was processed using the RCA Solid State Technology Center (SSTC) radiation hardened gate oxide process. The design was initially verified by processing the masks with the standard I^2(N/N) process.

Following the radiation hardening processing and subsequent device and array characterization tests, the arrays were radiation tested by NRL. The tested parts met or exceeded the minimum hardness levels established by NRL for the parts.

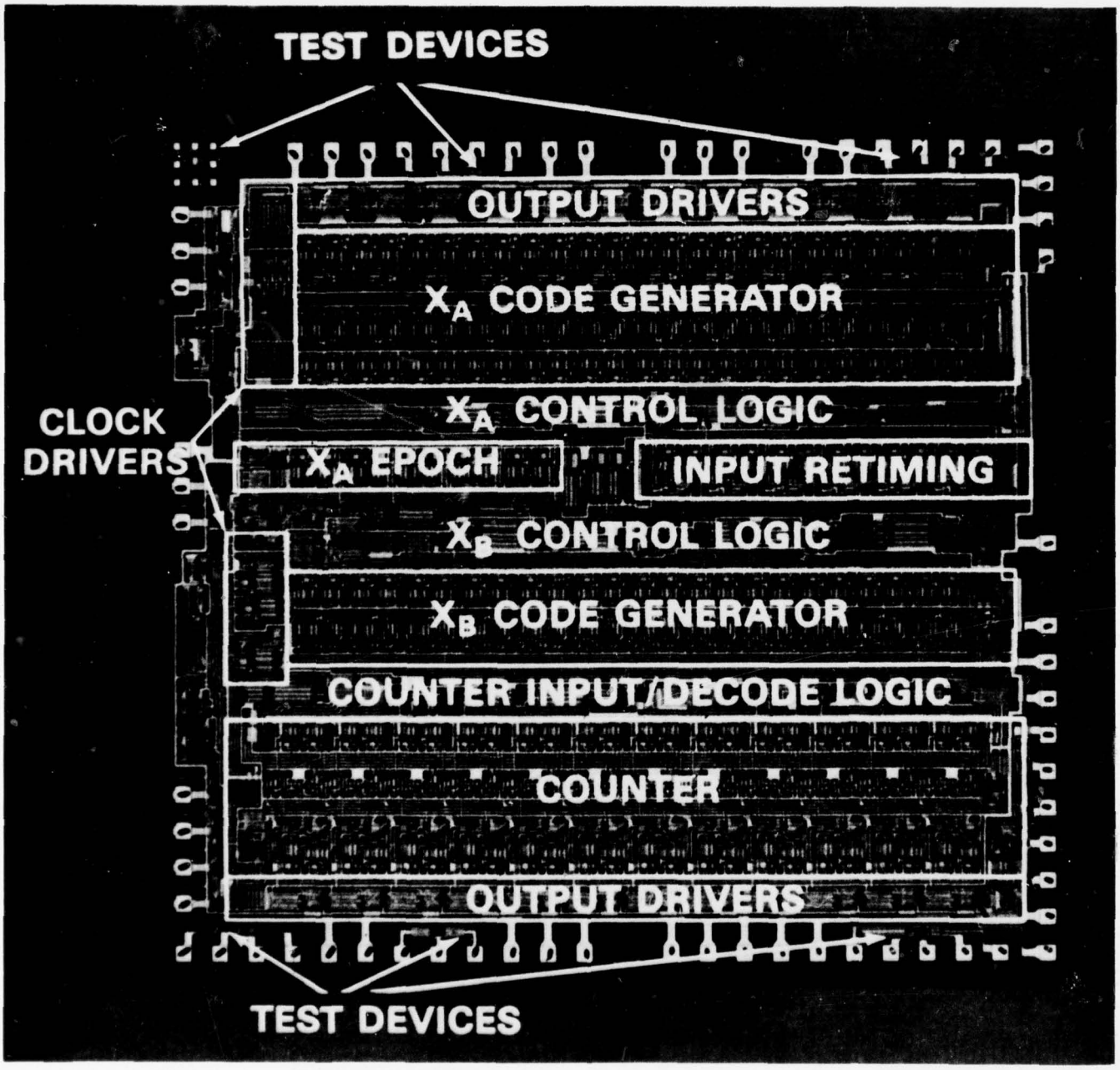


Fig. 1-1. Microphotograph of radiation hardened code generator array TCS102.

In the following sections the array partitioning, circuit design, performance predictions from circuit simulations, and actual array performance for both the standard and hardened processes are discussed in detail.

Since it is not the intent of this report to explore the detailed system operation of the GPS, only sufficient system descriptions will be provided to clarify the chip operation or to help establish an overall design baseline and philosophy.

Section II

SYSTEM CONSIDERATIONS

The TCS102 radiation hardened code generator array is designed for use in the precision navigation (P) code baseband subsystem of the NAVSTAR GPS system. The P code is produced at a 10.23-megabit rate with a period of exactly one week. Since the entire precision code generator (Fig. 2-1) is too complex to be included on a single LSI array, the precision code generation logic has been partitioned into five LSI arrays:

1) PX1 code generator
2) PX2 code generator
3) Z counter
4) Phase adjust logic
5) Tap register.

The PX1 and PX2 code generators each produce a pseudorandom sequence 1.5 s long. The Z counter is advanced by one count every 1.5 s, with a count of 403,200 required for a complete week. The phase adjust logic generates the reset signals required to adjust or update the precision code logic. The tap register varies the delay between the PX1 and PX2 sequences to enable more than one unique sequence to be produced.

The TCS102 code generator is designed to produce either the PX1 (TCS102A) or the PX2 (TCS102B) sequence, depending on the metallization mask used. Both the PX1 and PX2 sequences require two 12-bit pseudorandom sequence generators and a 12-bit counter. All the logic required by either the PX1 or the PX2 code generators is included on the TCS102 array; hence, the one design is used for two arrays in the baseband subsystem, the particular array being specified by the metal mask. A third variation of the metal mask will result in an array producing the command/acquisition (C/A) code required elsewhere in the baseband subsystem.

The TCS102 is the first CMOS/SOS LSI array to be designed for the GPS baseband subsystem. Specific interface requirements between the individual LSI arrays in the baseband subsystem had not been previously established, and, therefore, the TCS102 is designed for ease of interface with the future design of the remaining chips. Output signals from the TCS102 are made available as early as possible to allow more time to perform the logical functions on the remaining peripheral arrays. All signals which may be of use to the remaining logic are brought out of the TCS102 array.

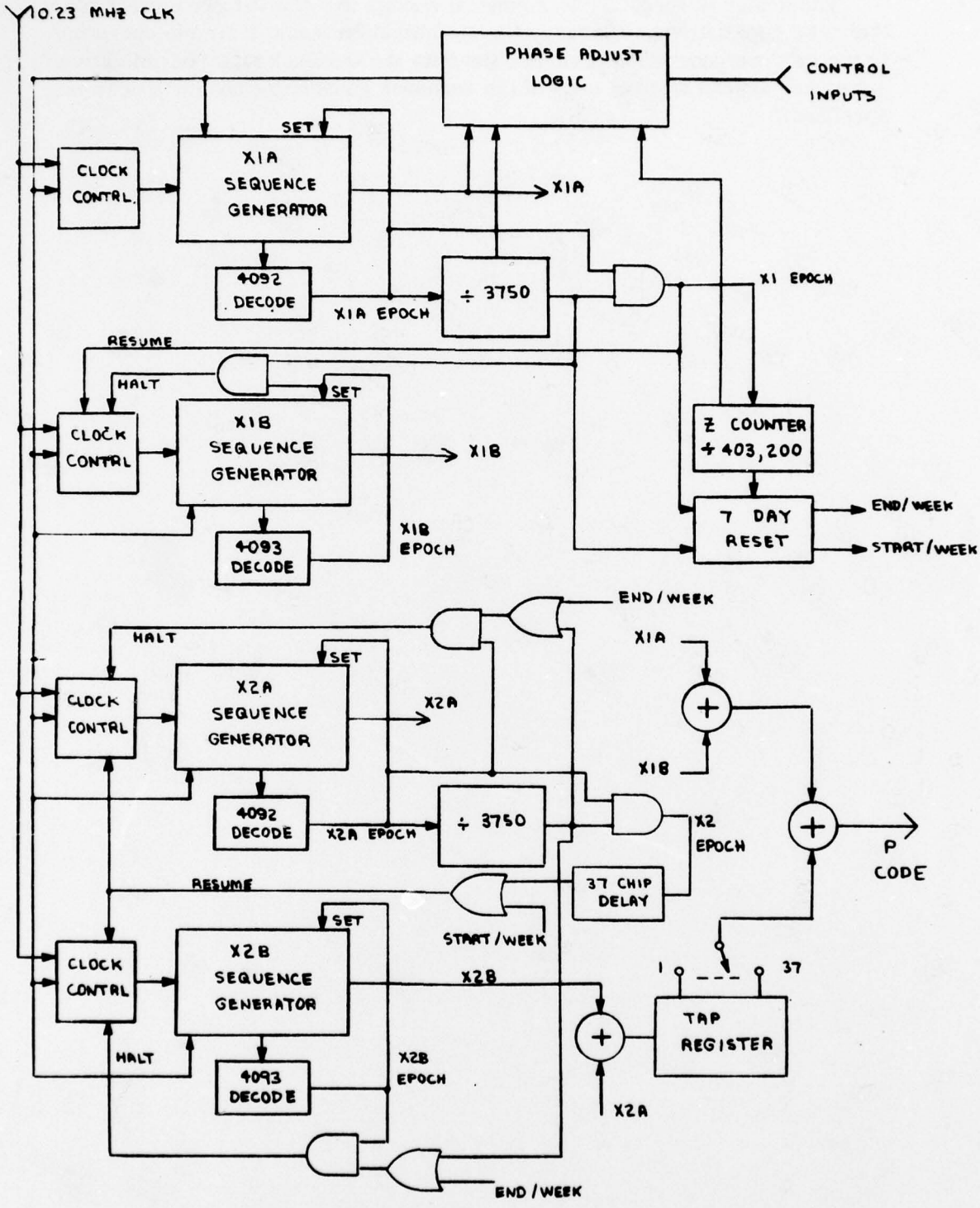


Fig. 2-1. P code generator.

The design of the TCS102 is general enough to allow it to be used in other than GPS applications. Changing the metallization mask (a simple operation in the artwork generation program) permits the feedback taps, initialization state, and decode state of each of the sequence generators and counter to be specified.

Section III

ARRAY PARTITION AND INTERFACE

A. GENERAL

There are three basic functional elements on the TCS102 array. The first is the XA sequence generator, a 12-stage pseudorandom sequence generator. The second functional unit is the XB sequence generator, another 12-stage pseudorandom sequence generator. The third functional unit is a 12-stage synchronous counter. In addition, there is control and clock logic associated with each of these functional units. The TCS102 code generator chip measures 5.13 mm by 4.80 mm (202 mils by 189 mils) and contains a total of 2660 transistors.

Design and operation of the two sequence generators and the counter are described below, followed by a summary of the mask programmable options implemented. The TCS102 array has a total of 40 input/output signals and has been packaged in a 40-pin dual-in-line package (DIP). Included is a summary of all the array input and output signals.

B. XA CODE GENERATOR

The XA code generator portion of the TCS102 array consists of a 12-stage pseudorandom sequence generator, a 12-stage serial shift register, state decode logic, and clock control logic as shown in Fig. 3-1. The pseudorandom sequence is produced by the sequence generator. The output of the sequence generator is clocked through the 12-stage serial register. Array outputs are taken at 12 contiguous stages of the sequence generator and serial register, as well as at the final register output. Thus, an output sequence is available with various delays. The state decode logic provides an output, XA $EPOCH_{out}$, when the sequence generator is in a preprogrammed state. The clock control logic gates the clock to the sequence generator and serial register ON or OFF, depending on control inputs to the array.

1. Code Generator Structure

Pseudorandom sequence generators can be designed in either of two equivalent forms. In the first form, a shift register is used with the outputs of selected stages being exclusive-ORed and fed back to the input as shown in

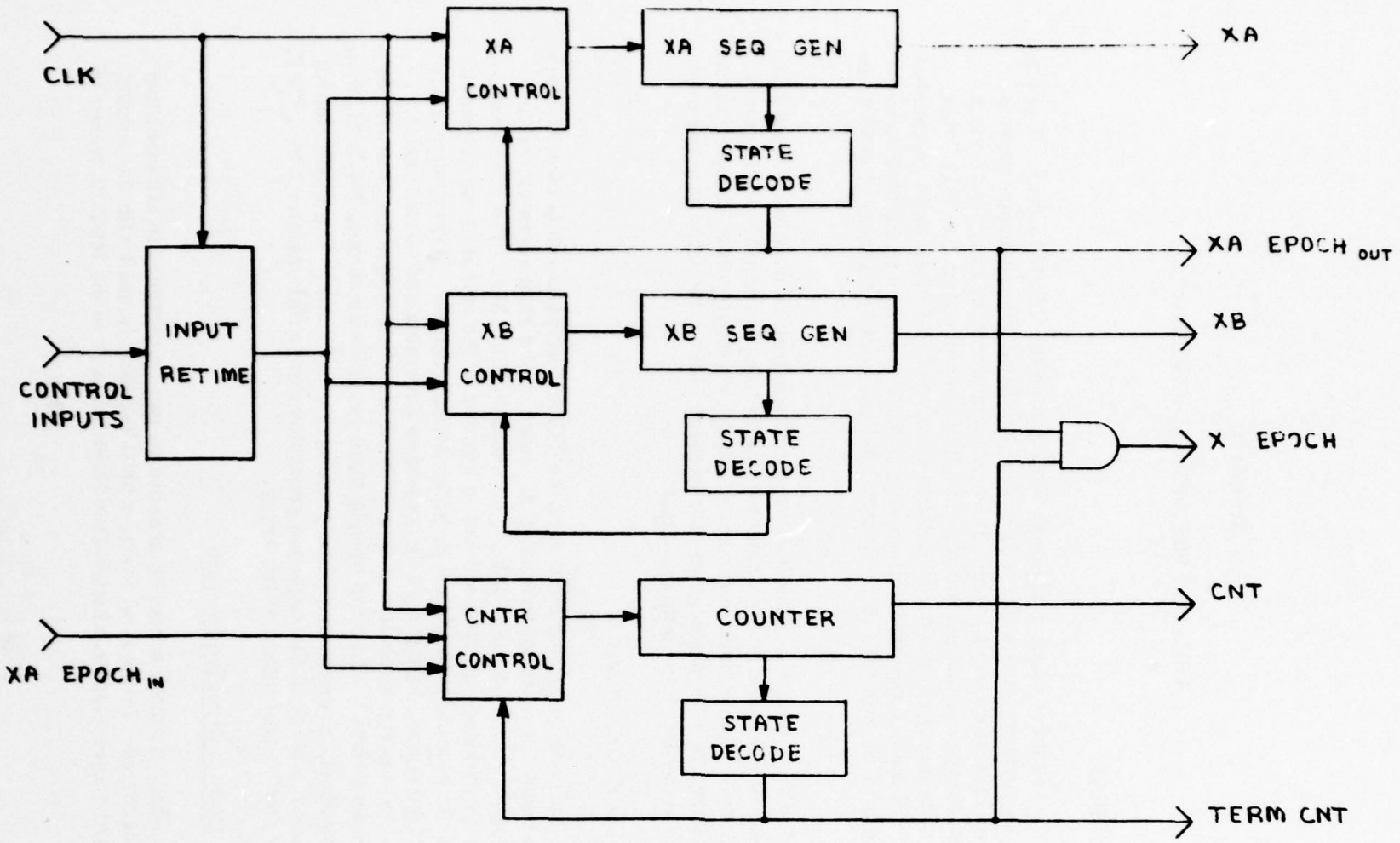


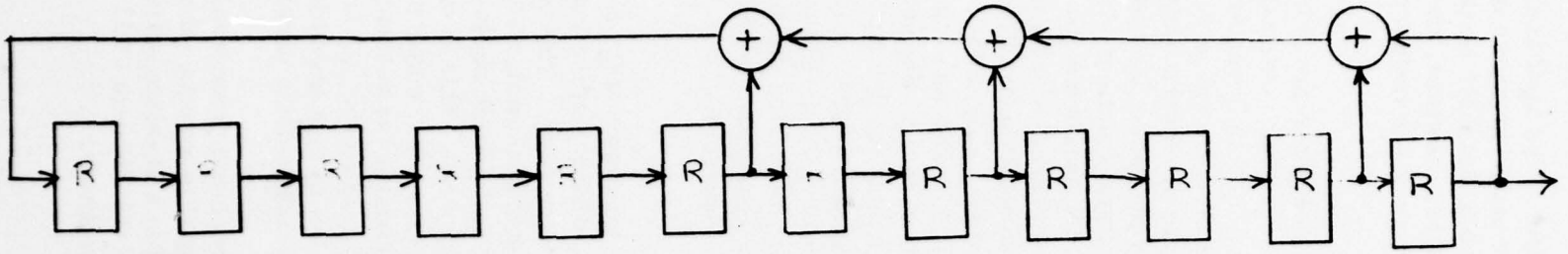
Fig. 3-1. TCS102 code generator.

Fig. 3-2a. In the second form, the shift register output is fed back to exclusive-OR gates located between selected successive register stages as shown in Fig. 3-2b. The two sequence generators can be designed such that their respective output sequences cannot be distinguished from each other. However, the state vectors, as defined by the contents of the register stages at one instant of time, will be different.

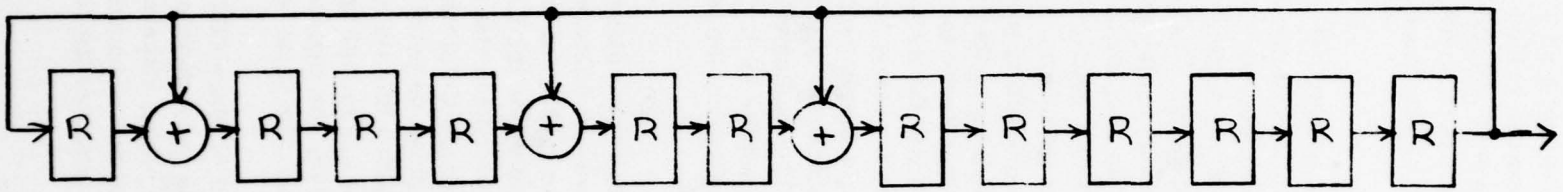
The choice of which of the two forms of sequence generator to implement is guided by two considerations: 1) the maximum clock frequency obtainable, and 2) the ease of implementing code programmability. In both forms for complete programmability a register and an exclusive-OR are required at each sequence generator stage. The programmability feature provides a means to bypass or disable those exclusive-ORs not required by the particular code being implemented. In this respect, neither configuration offers a distinct advantage in terms of size, device count, or programmability. The maximum speed for the sequence generator of Fig. 3-2a is limited by the propagation delay through the exclusive-ORs generating the register input. If the code requires more than several feedback taps, this delay quickly adds up using successive exclusive-ORs. Any scheme to reduce the serial delay by using an exclusive-OR tree will complicate the design and will still result in several exclusive-ORs in series. The sequence generator of Fig. 3-2b avoids the delay problem by having, at most, a single exclusive-OR between register stages. The only penalty paid in this scheme is the increased internal loading on the sequence generator output. The loading effects are minimized by increasing the size of the transistor gate widths in the register output. Hence, in order to obtain the maximum operating speed, the sequence generator configuration of Fig. 3-2b is used.

Each of the twelve stages of the XA sequence generator (Fig. 3-3) consists of an exclusive-OR followed by a register stage, with one of the inputs to the exclusive-OR being the output of the previous register stage. This input is tied to ground (logic 0) for the first stage of the sequence generator. The second input to the exclusive-OR is tied to ground (logic 0) if no feedback tap is desired, or to the output of stage CG12 when a feedback tap is desired. This is one of the programmable features included in the metal mask design. The output of the exclusive-OR is loaded into its associated register whenever the sequence generator clock makes a low to high transition provided the load control LA is low. Whenever LA is high, the register is initialized on a low to high transition of clock. The initialization state is determined by the programmable metal options.

The output of stage CG12 (Fig. 3-3) is the undelayed pseudorandom sequence produced by the sequence generator. This signal is brought out of the array as the XA-4 output and also serves as the input to a 12-stage serial register on the chip. The states of sequence generator stages CG9 through CG11 are also brought out of the array as XA-1 through XA-3, respectively.



a. Sequence generator configuration 1.



b. Sequence generator configuration 2.

Fig. 3-2. Two equivalent forms for a pseudorandom sequence generator.

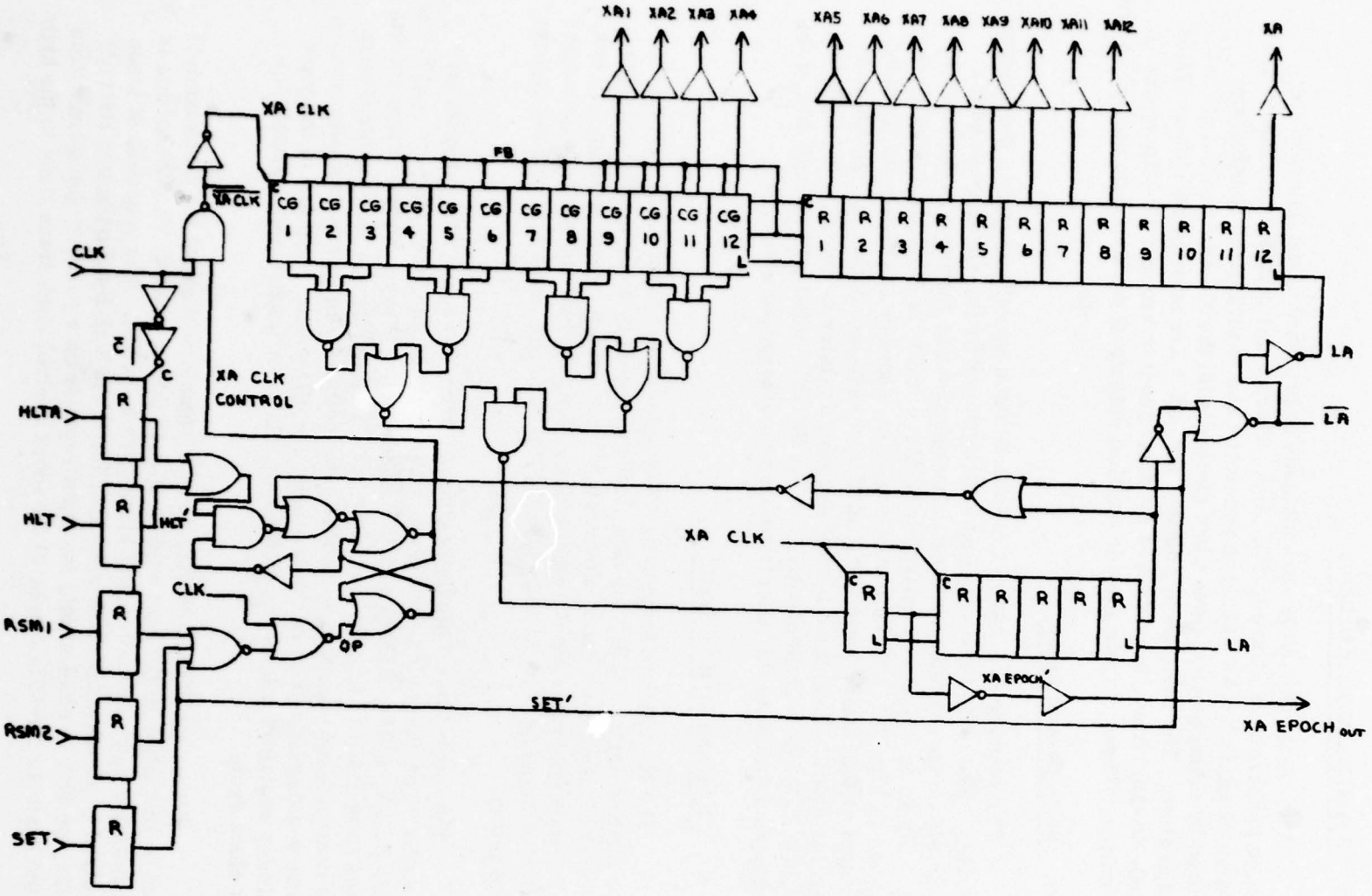


Fig. 3-3. XA code generator.

2. Serial Register Extension

A 12-stage shift register extension is provided at the output of the sequence generator as shown in Fig. 3-3. This serial register is clocked by the same clock as the XA sequence generator and is initialized to the state specified by metal mask options when clocked with the XA load control LA in the high state. The contents of stages 1 through 8 are brought off chip as XA-5 through XA-12. Also, the output of the final stage is brought off chip as the XA code output. These outputs provide parallel outputs of the sequence earlier in time.

3. State Decode Logic

The state decode logic is used to detect a specified state in the sequence generator. The state to be detected is determined by the metal mask which selects either the register state or its complement as the input to the decode logic. These 12 inputs are ANDed using three levels of NAND and NOR gates as shown in Fig. 3-3. To maintain maximum speed in a synchronous system, the output of the decode logic is retimed by a register clocked by the XA code generator clock. The output of this retiming register is brought off chip on the XA EPOCH output. Consequently, the XA EPOCH output will be high during the clock period following the detected state in the sequence generator.

4. Clock and Control Logic

The XA clock is formed by ANDing the array input clock with the XA clock control signal. When the clock control signal is high, the XA code generator is clocked at the input clock rate. When the clock control signal is low, the XA code generator clock remains low. This enables the XA code generator portion of the chip to be halted while the XB code generator and counter remain in operation.

The clock control signal is obtained from the output of a latch formed by a pair of crosscoupled NOR gates. The state of this latch is controlled by the HLT, HLTA, RSM1, RSM2, and SET inputs to the array. Each of these control inputs is retimed by an input register prior to reaching the clock control latch. The control input signals are clocked into the input register continually on each positive-going transition of the basic 10.23-MHz clock. The use of the input retiming registers allows the control signals to be latched and available for a full clock cycle.

Either the RSM1, RSM2, or SET signals will cause the clock control latch to transition to the high state if it is in the low state. This transition is not initiated until the basic input clock goes back low. The sequence of steps involved in starting the code generator is: 1) the high level on either RSM1, RSM2, or SET is clocked into the input register on a positive-going transition of the basic 10.23-MHz clock; 2) the clock control latch transitions to the high

state following the next negative-going transition of the basic clock; and 3) the first clocking of the XA sequence generator and serial extension register occurs on the next positive-going transition of the basic clock. If the clock control latch is already in the high state, it is not affected by the RSM1, RSM2, or SET inputs.

The HLT or HLTA inputs are used to stop the XA clock by transitioning the clock control latch to the low state. The transition to a low state can occur only during the sixth clock period following the decode state in the XA sequence generator. This is accomplished by ANDing the HLT or HLTA signals with the XA EPOCH delayed by an additional five clock periods of delay. The XA EPOCH is already delayed from the time of the decode state by one clock period. The HLT and HLTA inputs are both retimed on the chip. As a result, the clocking of the XA code generator is halted if either the HLT input or HLTA input is high at the positive transition of the basic clock following the fifth clock period after a high state decode logic state. At all other times the signal on HLT or HLTB will have no effect on the XA code generator.

The XA code generator is initialized to the state specified by the mask programming whenever the load control LA is in the high state at the time of a positive transition of the XA clock. A high level on LA is obtained in one of two ways: 1) as the result of a high level on the SET input to the chip, or 2) as the result of the state decode on the chip.

The SET input to the array is used to initialize the XA sequence generator. Whenever a high level is stored in the SET input register, the load control LA is high. The input register delays the initialization by one clock period from the application of the SET input. As described previously, the SET input initiates code generation if the clock control has been in the off state. The sequence generator will not proceed to the second bit in the sequence until the output of the SET input register returns to the low state.

The LA control signal is also high during the sixth clock period following the detection of the decode state in the XA sequence generator. Consequently, the output sequence continues for six bits after the decode state and is then initialized to the first bit of the sequence. The ability to detect a specified code generator state with the subsequent restart provides a simple method to program the code sequence to any desired length. When responding to an HLT or HLTA control signal, the code is stopped in the final bit of its sequence with LA in the high state. The register stages responsible for delaying the state decode are clocked by the XA clock rather than by the basic array clock. Thus, LA remains high and the XA sequence generator is initialized to the first bit of the sequence when clocking resumes.

Figure 3-4 shows the timing associated with the SET command. The timing diagrams of Fig. 3-5 and 3-6 show typical timing relationships in the TC102 array.

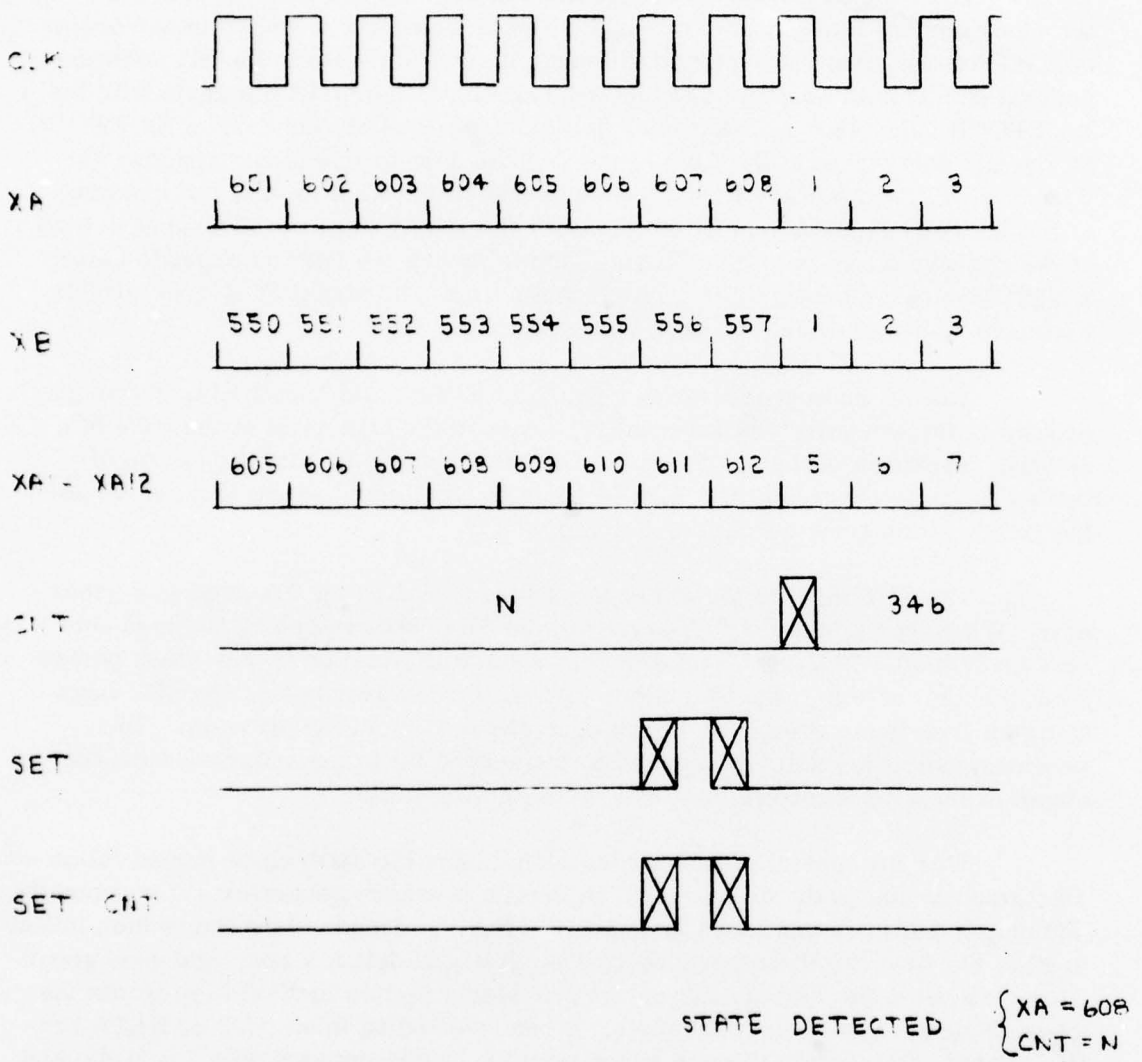


Fig. 3-4. Phase adjustment timing.

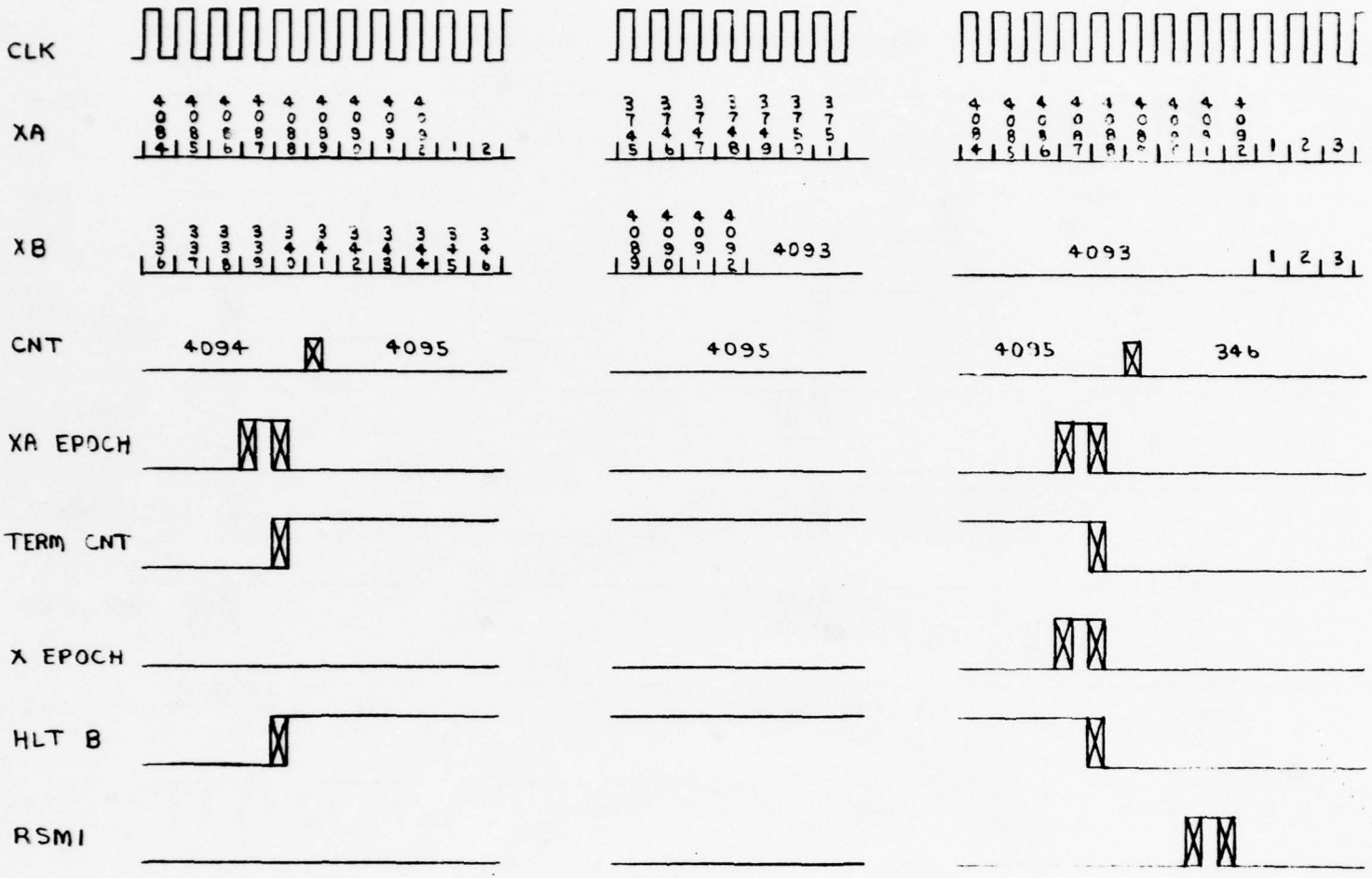


Fig. 3-5. X1 code generator timing.

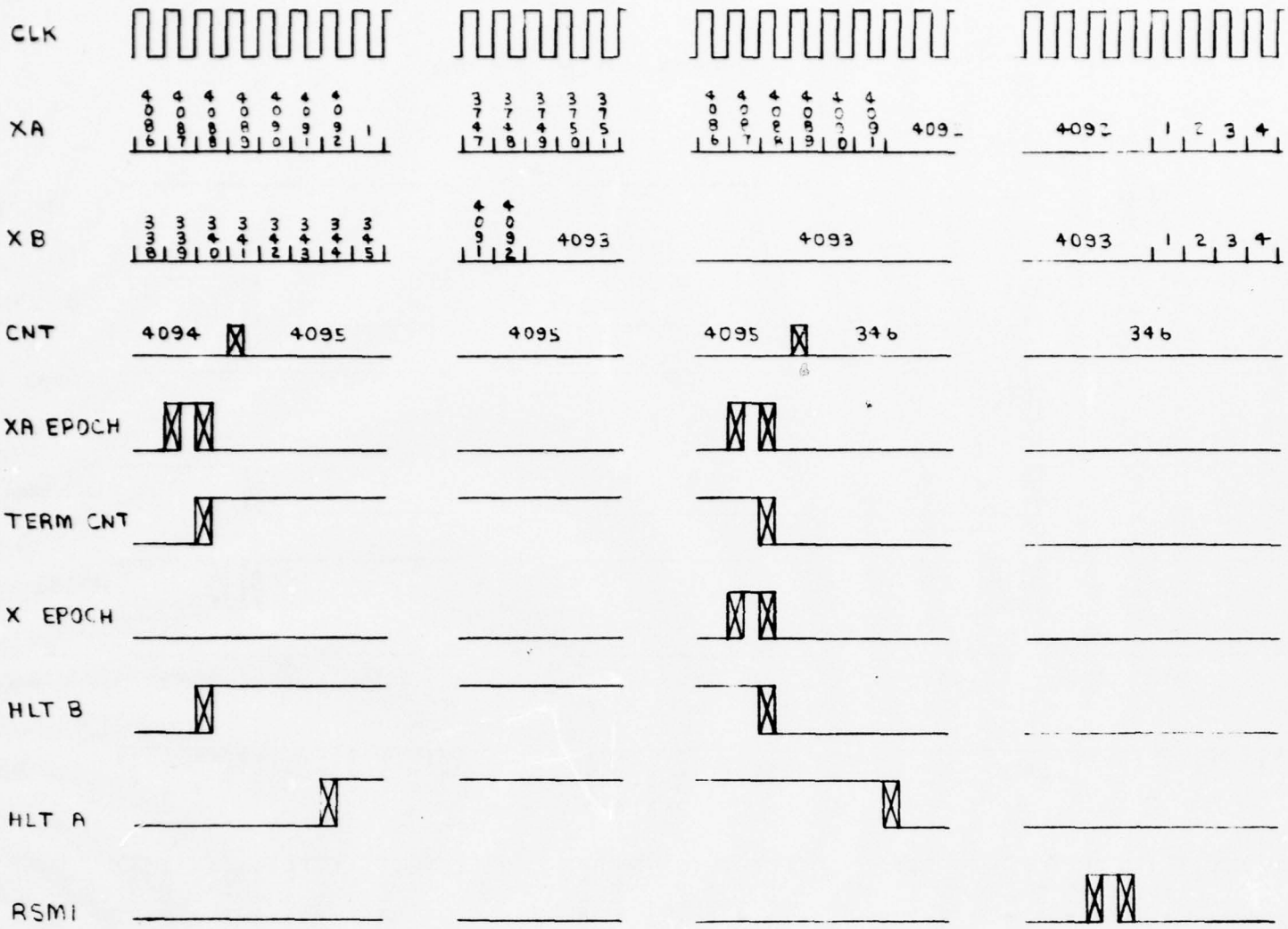


Fig. 3-6. X2 code generator timing.

C. XB CODE GENERATOR

The XB code generator portion of the TCS102 array consists of a 12-stage pseudorandom sequence generator, state decode logic, and clock control logic, shown in detail in Fig. 3-7. The output of the final stage of the sequence generator is brought out of the chip as the XB code. The structure and operation of the XB code generator are similar to those of the XA code generator. The following discussion of the XB code generator will emphasize the features in which the two code generators differ.

1. Code Generator Structure

The sequence generator in the XB code generator has the same structure as the XA sequence generator, namely, exclusive-OR gates at the input to each register stage with the output of the final stage being fed back to selected stages. The mask programmable features in each sequence generator stage are: 1) the presence or absence of feedback from the output stage, 2) the state the register is to assume when initialized, and 3) the input of either the register state or its complement to the state decode logic.

All signal transitions in the XB sequence generator occur on the positive-going transition of the XB clock. The sequence generator is initialized to its starting point whenever the load control LB is high. The output of the final stage of the sequence generator is brought off chip as the XB code without any additional delay.

2. State Decode Logic

The state decode logic detects the presence of the sequence generator state specified by the programmable metal option. Whenever the sequence generator is in this state, the state decode is high. For all other sequence generator states, the state decode is low. The state decode is retimed prior to its use in the control logic to avoid a speed limitation problem.

3. Clock and Control Logic

The XB clock is formed by ANDing the array input clock with the XB clock control signal as shown in Fig. 3-7. When the clock control signal is high, the XB clock is the same as the array input clock. When the clock control signal is low, the XB clock is halted in its low state and the XB code generator is not clocked. This enables the XB code generator to be halted even though other sections of the array continue to be clocked.

As is the case with the XA code generator, the clock control signal is obtained as the output of a latch formed by a pair of crosscoupled NOR gates. The clock control for the XB code generator responds to the HLT, HLTB, RSM1, RSM2, and SET inputs to the array. HLTB is the only one of these

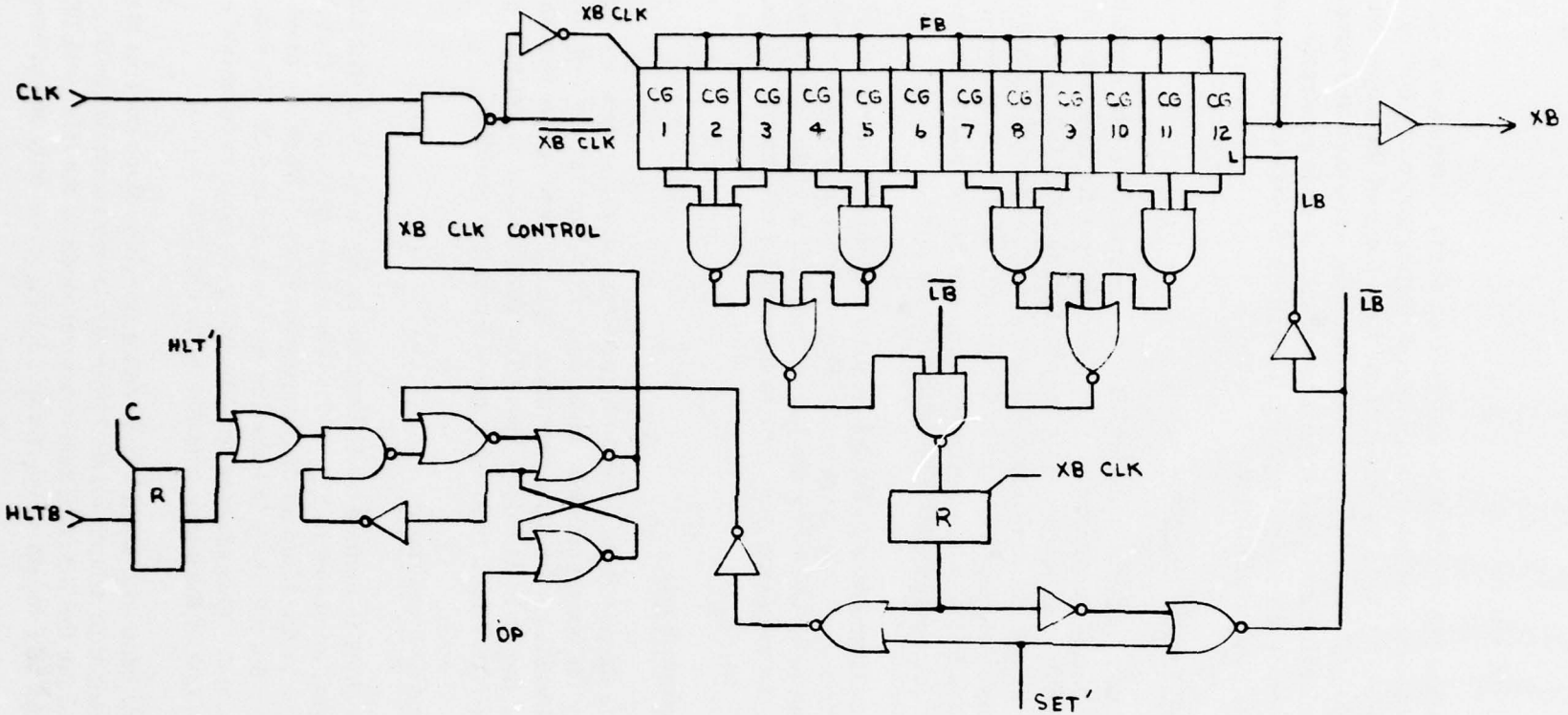


Fig. 3-7. XB code generator.

control signals which is not shared with the XA code generator. All of the control signals are retimed on the array.

The same signal which sets the XA clock control signal to the high state also sets the XB clock control signal to the high state. The XB code generator responds to the SET, RSM1, and RSM2 input signals in the same manner as the XA code generator.

Either the HLT or HLTB signal is used to stop the clocking of the XB code generator. The clock control latch transitions to its low state if either the HLT input or HLTB input is high when the decode state is detected and clocked into its retiming register. The HLT input will cause both the XA and XB code generators to stop sequence generation. Only the XB code generator responds to the HLTB input. The XB sequence generator is stopped in the state following the state decode state when halted.

The XB code generator is initialized whenever a clocking occurs with the load control LB high. A high level on LB will occur when a high level is clocked into the SET input retiming register. This provides the external means of initializing the XB code generator at any time. The XB code generator remains in its initial state until after SET goes low. The second condition under which LB will be high is during the clock period following the decode state. Hence, the XB sequence continues for one bit beyond the decode state, at which point initialization to the first bit of the sequence occurs. Thus, the XB sequence length can be adjusted to any desired length by the selection of the decode state and the initial state using the programmability options. The XB code generator will always be in its final state when halted by the clock control logic. Whenever operation resumes, the output will begin with the first bit of the sequence.

The timing diagrams of Fig. 3-4 through 3-6 show the timing relationships in the control and clocking of the XB code generator.

D. SYNCHRONOUS COUNTER

The third functional area on the TCS102 array is the 12-stage synchronous counter shown in Fig. 3-8. The counter portion of the array consists of the counter stages, an output register, count decode logic, and input control logic. The counter is described in more detail in the following sections.

1. Counter Structure

Operation of the counter is best explained by examining the operation of a single counter stage shown in Fig. 3-9. The count is stored in a master-slave D-type register which is clocked by the count control logic output, CLK C. Whenever load control LC is low, the input to the register is formed by the exclusive-OR of the register output with the CE_I signal obtained from the next

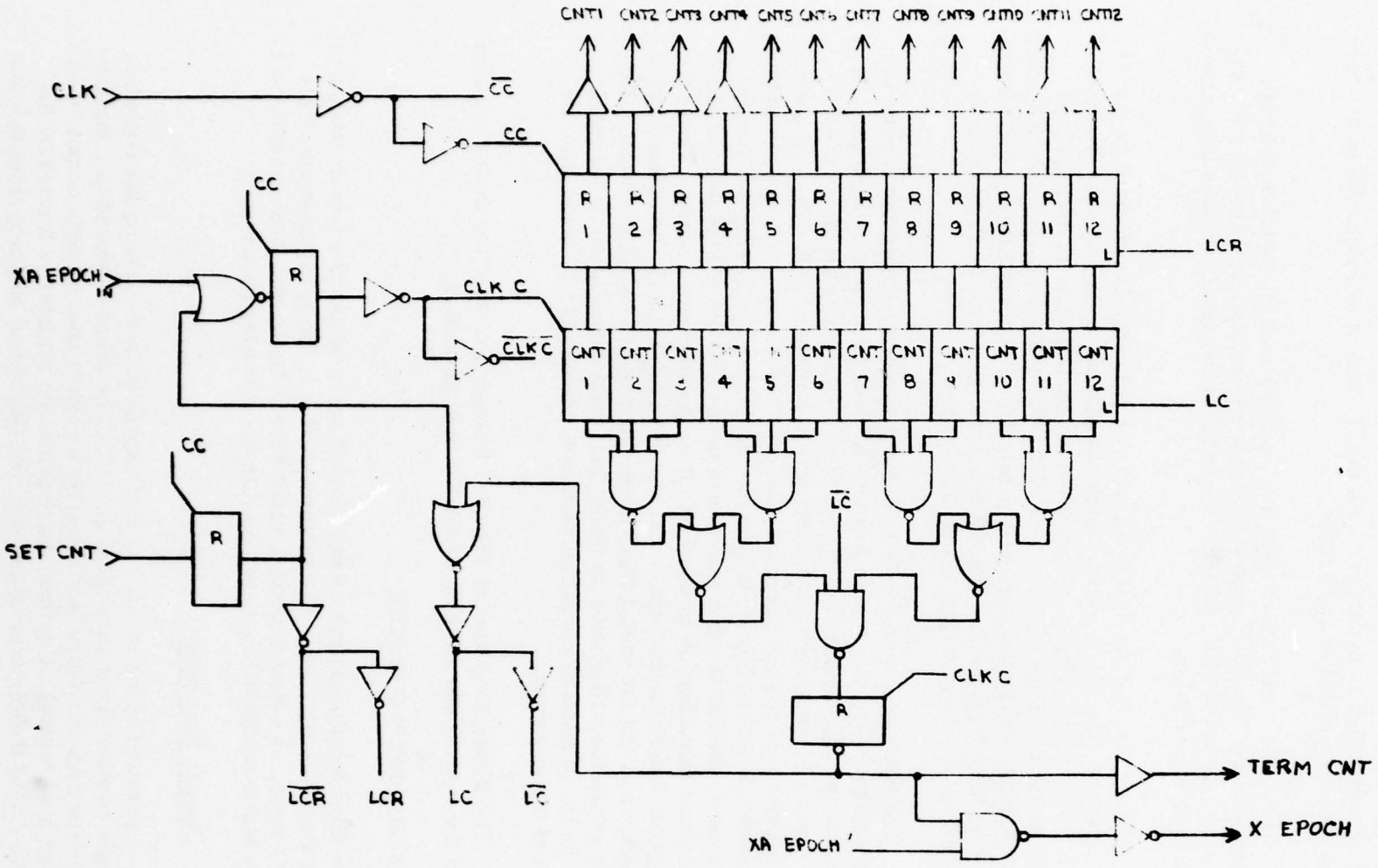


Fig. 3-8. Epoch counter.

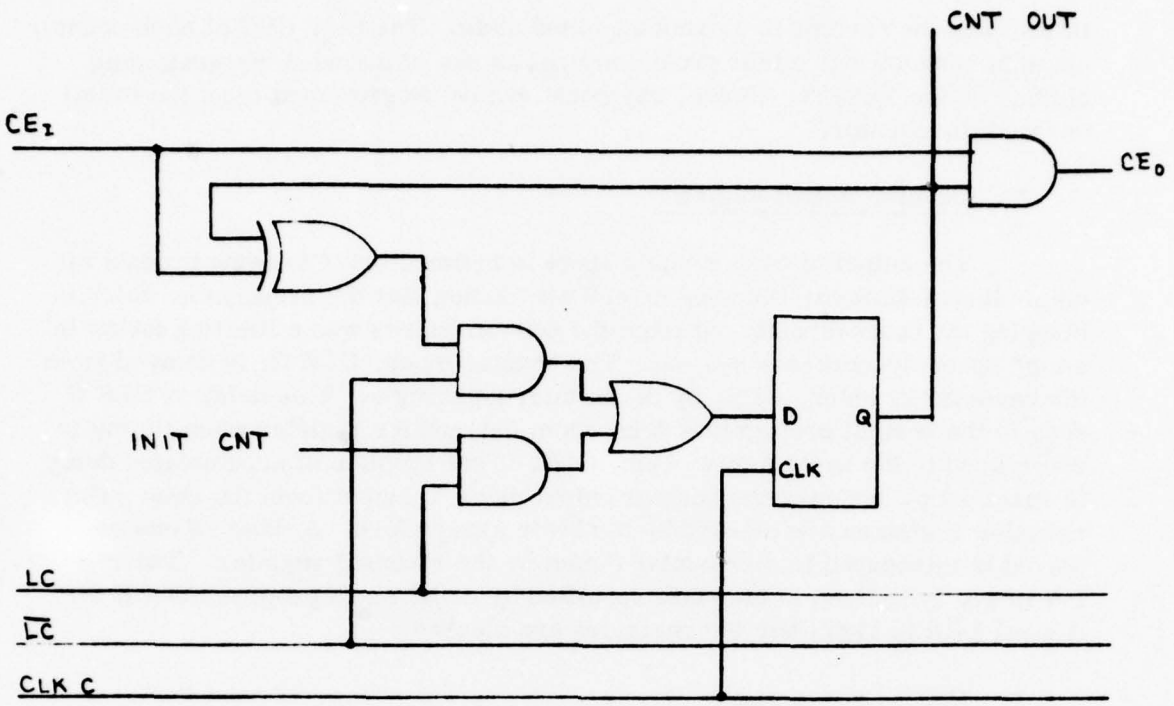


Fig. 3-9. Logic diagram of a counter stage.

less significant stage. Thus, when CE_I is low, the input to the register is the same as its output, and no change in counter state occurs upon clocking. On the other hand, when CE_I is high, the input to the register is the complement of the register output, resulting in the register changing state upon clocking. The count enable signal CE_O for the next more significant counter stage is formed by ANDing CE_I with the register output. At the least significant stage CE_I is always high, causing the least significant bit of the count to change state on each clocking of the counter. The CE_I of subsequent counter stages is high only when all less significant bits of the count are high (logic 1).

Unlike a ripple counter where the carry propagates from the least to more significant stage when clocked, all stages of the TCS102 counter will change state simultaneously when clocked. This reduces to a minimum the time delay from the application of the count command to the obtainment of a valid output count. However, sufficient time must be allowed for the count enable signal to propagate the full length of the counter prior to the next count command. Thus, the TCS102 counter is best suited to the counting of infrequently occurring events where a fast update of the count is required. In a particular application, the counter can count the XA EPOCH signals produced by the XA code generator and maintain a valid count at all times in a synchronous system being clocked at 10 to 20 MHz.

Whenever the control LC in Fig. 3-9 is high, INIT CNT is loaded into the register on the positive transition of CLK C. This provides the means of

initializing the counter to a predetermined state. The INIT CNT of each counter stage is connected to either ground or V_{DD} as one of the mask programming options on the TCS102. Hence, any count can be programmed in as the initial count of the counter.

2. Counter Output Register

The output of each counter stage is retimed prior to being brought off chip. It was discovered during circuit simulation that the propagation delay in bringing the count directly out from the counter stages was a limiting factor in a high speed synchronous system. The counter clock, CLK C, is delayed from the basic array clock, CLK, by the counter input logic. This delay in CLK C adds to the normal propagation delay from the counter register when timing is referenced to the basic array clock, CLK. This problem of accumulated delay is resolved by retiming the counter output prior to output from the chip. The retiming registers are clocked by the basic array clock. A delay of one clock period is introduced in the counter output by the retiming register. The registers are initialized to the state specified by metal mask programming if the control LCR is high when the registers are clocked.

3. Count Decode Logic

The count decode logic is used to detect the maximum or all 1's count in the counter. The count decode performs the AND operation on the outputs of the 12 counter stages using three levels of logic as shown in Fig. 3-8. The output of these gates is retimed by a register clocked by CLK C. To compensate for the presence of this register, the complement of the least significant counter stage output must be used as the input to the count decode. The output of the count decode register is brought off chip as TERM CNT, and is ANDed with XA $EPOCH_{out}$ to produce X EPOCH, another array output. TERM CNT is high when the counter is at its maximum count. Since the TERM CNT output is not retimed by the basic clock, it will precede the count by one period of the basic clock when both are observed on the array outputs.

4. Counter Input Logic

The counter input logic generates the counter clock, CLK C, and the load controls, LC and LCR. The pulses to be counted are applied to the XA EPOCH input and are retimed by a register clocked by the basic array clock as shown in Fig. 3-8. The output of this register is the clock for the synchronous counter. The net effect of this arrangement is that the XA EPOCH input is sampled each time the basic 10.23-MHz clock, CLK, makes a positive-going transition. Whenever a high level is sampled on the input and the previous input sample was low, the counter is advanced by one count. A series of high samples in a row will advance the counter by only one count. The high sample is counted only if it is immediately preceded by a low sample. Hence, the maximum possible count rate is half the basic clock frequency.

The counter could be used to count asynchronous pulses with arbitrary width applied to the XA EPOCH input and to provide the output count in synchronous form. In this case, to assure no missed counts, each pulse must be at least a basic clock period wide. The same width requirement exists for the low between successive pulses.

The SET CNT input is used to initialize the counter to its mask programmed initial state. Like the other control inputs to the TCS102 array, the SET CNT input is retimed by an input register clocked by CLK. A high level on the output of the SET CNT register produces: 1) a high level on the LC control to the counter stages, 2) a high level on the LCR control to the counter output registers, and 3) a high level on the input to the register producing CLK C. The counter and the counter output registers will be initialized on the next positive transition of CLK. The counter will not properly initialize if the XA EPOCH input is high when SET CNT is received. In this situation, the counter is being given conflicting instructions to both count and initialize. The counter will not count an XA EPOCH pulse until the third CLK transition after the SET CNT is received. Table 3-1 summarizes the initialization procedure using SET CNT.

TABLE 3-1. COUNTER INITIALIZATION STEPS

CLK Transition #	Action
1	SET CNT loading into input register setting up LC and LCR, XA $EPOCH_{in}$ low.
2	Counter and count register initialized.
3	No action.
4	First counting of XA EPOCH input can occur.

The counter will also initialize itself following the maximum count of 4095. The TERM CNT output of the count decode logic will cause the LC control to go to the high state. The next time an XA EPOCH input is received, the counter is initialized. Unlike the external initialization using SET CNT, the output registers are not directly initialized. This internal initialization permits the counter to be recycled after every N counts up to the maximum of 4096. N is fixed by the mask programming of the initial counter state.

E. MASK PROGRAMMABLE OPTIONS USED

Under this contract, metal masks were produced for two different versions of the TCS102 and have been designated as the TCS102A and the TCS102B. All parts fabricated and tested under this contract have used the TCS102B metal mask. The mask programmable options used on both of these metal masks will be described in this section.

1. TCS102A

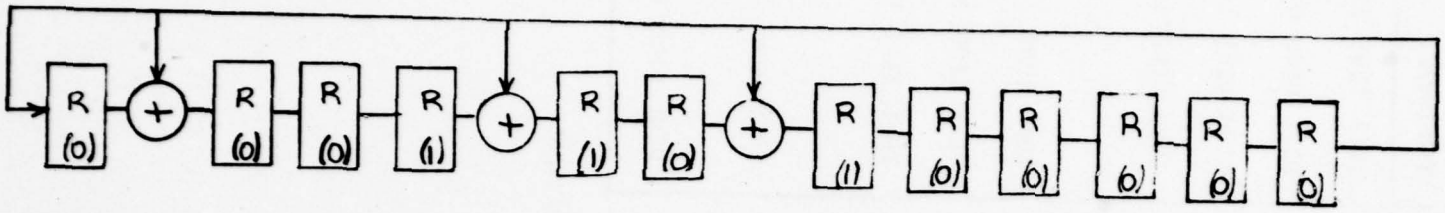
The feedback tap locations and initial state for the XA and XB sequence generators on the TCS102A chip are shown in Fig. 3-10. Without any shortening of sequence length, the sequence produced by each of these sequence generators will be 4095 bits in length. The XA state decode logic looks for the state 0011 0000 1001 in the XA sequence generator reading left to right in Fig. 3-10. When coupled with the initial state of 0001 1010 0000, this decode state causes the output sequence of the XA sequence generator to be shortened to 4092 bits. The final three bits of the sequence are omitted. In similar fashion, the XB state decode logic looks for the state 0111 0111 1111, which results in the XB sequence being shortened to 4093 bits by omitting the final two bits. The serial register in the XA code generator is initialized to the first 12 bits of the XA sequence, namely, 0001 0010 0100, reading from input to output. Table 3-2 summarizes the mask programmable options used.

The counter is programmed to initialize to a count of 346 during initialization. This initial count, when coupled with the maximum count of 4095, gives a counter which recycles every 3750 counts. If the XA $EPOCH_{out}$ is connected to XA $EPOCH_{in}$, the counter will recycle and an X EPOCH will be produced once every 15,345,000 cycles of the basic clock, CLK.

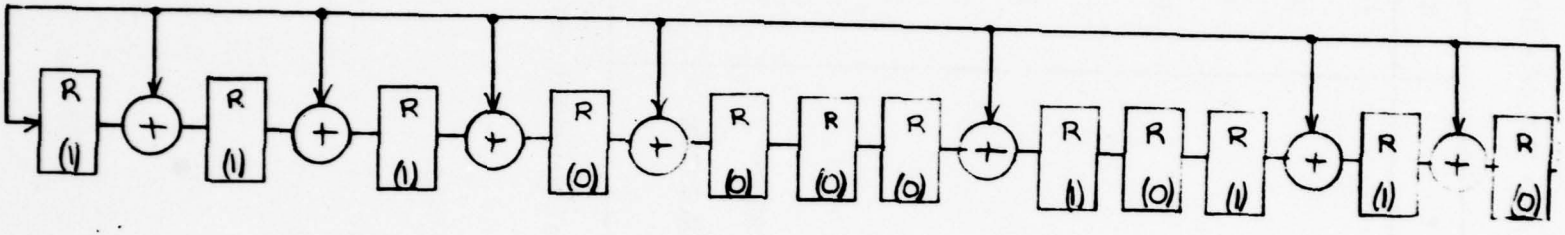
2. TCS102B

The feedback tap locations and initial state for the XA and XB sequence generators on the TCS102B array are shown in Fig. 3-11. These feedback taps normally will give a sequence 4095 bits long. However, the combination of initial states and decode states results in the XA sequence being shortened to 4092 bits and the XB sequence being shortened to 4093 bits. The final three bits of the XA sequence are omitted, while the final two bits of the XB sequence are omitted. Although the sequence lengths for the TCS102A and TCS102B are the same, the actual sequences are different. The program options for the TCS102B are summarized in Table 3-2.

The programming of the counter on the TCS102B is the same as on the TCS102A. The counter is initialized to a count of 346 which, when combined with the maximum count of 4095, produces a full cycle of the counter every 3750 counts.



a. XA sequence generator.



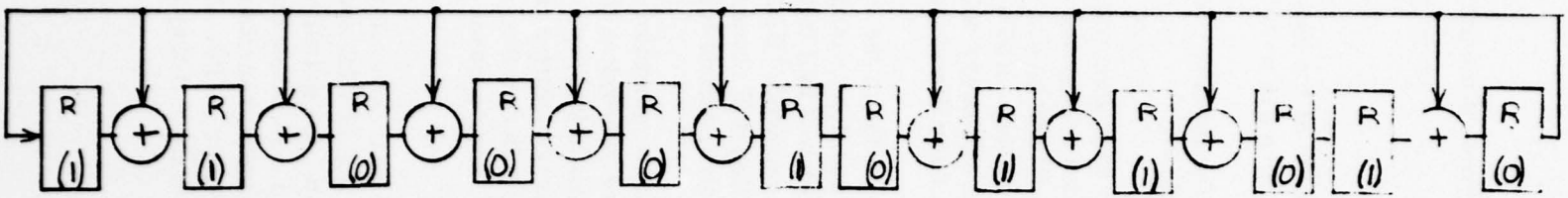
b. XB sequence generator.

Fig. 3-10. TCS102A sequence generators. Initial state shown in parentheses.

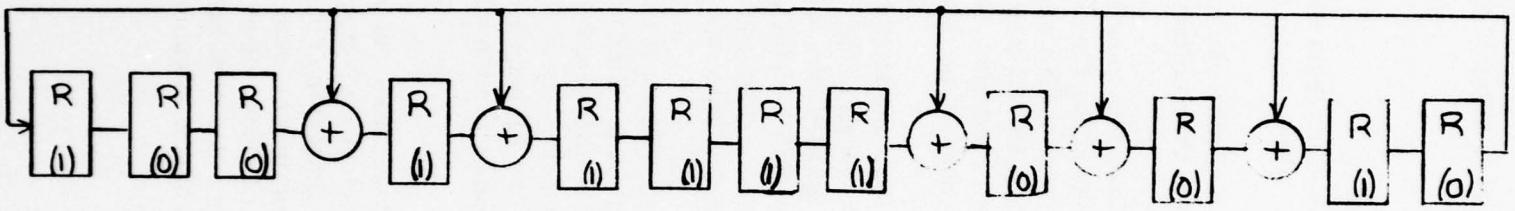
TABLE 3-2. TCS102A AND TCS102B MASK PROGRAMMABLE OPTIONS USED

	TCS102A	TCS102B
XA FEEDBACK TAPS	1100 1010 0000	1111 1101 1101
XA DECODE STATE	0011 0000 1001	0111 0100 0110
XA INITIAL STATE	0001 1010 0000	1100 0101 1010
XA REGISTER INITIAL	0001 0010 0100	1010 0100 1001
XB FEEDBACK TAPS	1111 1001 0011	1001 1000 1110
XB DECODE STATE	0111 0111 1111	0111 1100 1000
XB INITIAL STATE	1110 0001 0110	1001 1111 0010
COUNTER INITIAL STATE*	0001 0101 1010	0001 0101 1010
COUNTER OUTPUT REGISTER INITIAL STATE*	0001 0101 1010	0001 0101 1010

*Most significant bit to least significant bit reading left to right.



a. XA sequence generator.



b. XB sequence generator.

Fig. 3-11. TCS102B sequence generators. Initial state shown in parentheses.

F. INPUT/OUTPUT SUMMARY

Operation of the TCS102 array is described here in terms of the array inputs and outputs.

1. TCS102 Inputs

The TCS102 has nine inputs controlling the operation of the two sequence generators and counter. These inputs and their control action are as follows:

CLK - This is the basic clock signal supplied to the TCS102. All operations are synchronized to the positive transition of this clock.

HLTA - When low, this input has no effect on the code generator operation. If this input is high at the time of the clock transition generating the final bit in the XA sequence, the XA sequence generator will halt in this final state until either an RSM1, or RSM2, or SET signal is received. HLTA has no effect on the XB sequence generator. Halting of operation will occur only on the final bit of the XA sequence, as determined by the XA state decode logic.

HLTB - When low, this input has no effect on operation of the code generator. If this input is high at the time of the clock transition generating the final bit in the XB sequence, the XB sequence generator will halt in this final state until either an RSM1, RSM2, or SET signal is received. HLTB has no effect on the XA sequence generator. Halting of operation will occur only on the final bit of the XB sequence as determined by the XB state decode logic.

HLT - When low, this input has no effect on the code generator operation. If this input is high at the time of the clock transition generating the final bit of the XA sequence, the XA sequence generator will halt in this final state. Also, if this input is high at the time of the clock transition generating the final bit of the XB sequence, the XB sequence generator will halt in this final state. Hence, the HLT input can be used to stop the operation of both sequence generators on the TCS102.

RSM1 - When low, this input has no effect on the code generator operation. If this input is high at the time of a positive transition of CLK and if either the XA or XB sequence generator is halted in its final state, the halted sequence generator will begin operation by going to the first bit of the sequence on the next positive transition of clock. Both the XA and XB sequence generators continue producing their codes until halted by HLT, HLTA, or HLTB. A high level on the RSM1 input has no effect on the sequence generators if they are already producing code.

RSM2 - This input has the same effect on TCS102 operation as the RSM1 input.

SET - When low, this input has no effect on the code generator operation. If this input is high at the time of a positive transition of CLK, both the XA and XB sequence generators go to their initial state on the next positive transition of clock. They remain in their initial state until the second positive transition of CLK after SET returns to its low state. Both sequence generators then continue to produce code.

XA EPOCH$_{in}$ - This is the input signal to the counter. The XA EPOCH$_{in}$ is sampled on each positive transition of CLK. The count is advanced each time the sampled value is high, provided the previous sampled value was low. Successive high samples without intervening low samples will add only one to the count. The new count appears on the counter output after the positive CLK transition following the transition on which the high input level was first observed.

SET CNT - This input has no effect when it is low. If it is high at the time of a positive transition of CLK, the counter is initialized to its initial count on the next positive transition of CLK. As long as the SET CNT is high, counting of the XA EPOCH$_{in}$ pulses is disabled. To properly set the counter, the XA EPOCH$_{in}$ must be low at the time of the first high sampling of the SET CNT. A high on the XA EPOCH$_{in}$ will not be counted until the second sampling with SET CNT low.

2. TCS102 Outputs

The 29 outputs of the TCS102 array are as follows:

XA - This is the output of the XA sequence generator.

XB - This is the output of the XB sequence generator.

XA1 - XA12 - These are XA sequence outputs which are advanced in time from the XA output. XA1 is 15 bits earlier in the sequence than XA, XA2 is 14 bits earlier, continuing until XA12 which is 4 bits earlier than XA.

XA EPOCH$_{out}$ - The XA EPOCH$_{out}$ is high during only one bit of the XA sequence as decoded by the state detect logic. As programmed, this output is high during the 4087th bit of the 4092-bit XA sequence.

CNT1 - CNT12 - These are the 12 bits of the counter output, with CNT1 being the least significant bit and CNT12 being the most significant bit.

TERM OUT - This output goes high one CLK period before the counter reaches its final count of 4095. It remains high until one CLK period prior to the counter output returning to the initial count.

X EPOCH - This output is formed by ANDing the XA EPOCH$_{out}$ with the TERM CNT. Consequently, X EPOCH will be high only during the 4087th bit of the XA sequence occurring when the counter is at 4095.

3. Packaging

The TCS102 arrays are packaged in two different packages. The TCS102-1 uses a 40-lead dual-in-line package (DIP) while the TCS102-2 uses a 48-pin leadless hermetic package (LHP). The list of package pin identifications is given in Table 3-3 for the DIP and in Table 3-4 for the LHP.

4. Power Requirements

Power is supplied to the TCS102 array through the ground and V_{DD} input pins. The TCS102 can operate over a wide range of voltages from 4 to 15 V. The maximum clock rate achievable increases as the operating voltage increases.

The output signals swing over the full voltage range from ground for a logic "0" to V_{DD} for a logic "1". The input signal voltage swing should also be over the full range from ground to V_{DD}.

TABLE 3-3. TCS102 PACKAGE PIN IDENTIFICATION FOR 40-LEAD DIP

Package Pin #	Signal Name	I/O		Package Pin #	Signal Name	I/O
1	V_{DD}			21	HLT	I
2	XA EPOCH$_{OUT}$	O		22	SET	I
3	XA-4	O		23	SET CNT	I
4	XA	O		24	XA EPOCH$_{IN}$	I
5	XA-3	O		25	CLK	I
6	XA-2	O		26	CNT-12	O
7	XA-1	O		27	CNT-11	O
8	XA-12	O		28	CNT-10	O
9	XA-11	O		29	CNT-9	O
10	XA-10	O		30	CNT-8	O
11	XA-9	O		31	CNT-7	O
12	XA-8	O		32	CNT-6	O
13	XA-7	O		33	CNT-5	O
14	XA-6	O		34	CNT-4	O
15	XA-5	O		35	CNT-3	O
16	HLTB	I		36	CNT-2	O
17	RSM1	I		37	CNT-1	O
18	RSM2	I		38	X EPOCH	O
19	GND			39	TERM CNT	O
20	HLTA	I		40	XB	O

TABLE 3-4. TCS102 PACKAGE PIN IDENTIFICATION FOR 48-LEAD LHP

Package Pin #	Signal Name	I/O	Package Pin #	Signal Name	I/O
1	V_{DD}		25	SET	I
2	XA EPOCH$_{OUT}$	O	26	SET CNT	I
3	XA-4	O	27	XA EPOCH$_{IN}$	I
4	XA	O	28	CLK	I
5	XA-3	O	29	N.C.	
6	N.C.		30	N.C.	
7	XA-2	O	31	N.C.	
8	XA-1	O	32	CNT-12	O
9	XA-12	O	33	CNT-11	O
10	XA-11	O	34	CNT-10	O
11	XA-10	O	35	CNT-9	O
12	XA-9	O	36	CNT-8	O
13	XA-8	O	37	CNT-7	O
14	XA-7	O	38	CNT-6	O
15	XA-6	O	39	CNT-5	O
16	XA-5	O	40	CNT-4	O
17	N.C.		41	CNT-3	O
18	N.C.		42	N.C.	
19	HLTB	I	43	CNT-2	O
20	RSM1	I	44	CNT-1	O
21	RSM2	I	45	N.C.	
22	GND		46	X EPOCH	O
23	HLTA	I	47	TERM CNT	O
24	HLT	I	48	XB	O

Section IV

CIRCUIT DESIGN AND SIMULATION

In the custom cell approach, which was chosen for the design of the TCS102 code generator LSI array, each cell is specifically designed to perform its function in the array. This approach allows both the array size and performance to be optimized, as well as permitting the mask programming option to be incorporated. In addition, custom design of the cells allows techniques to be employed that enhance the radiation hardness of the chip. Design techniques employed in the TCS102 are described in the following material.

A. PERFORMANCE REQUIREMENTS

The TCS102 code generator is designed to be a low-power, high-speed pseudorandom-sequence generator capable of operating in the radiation environment found in a satellite application.

This array is designed to generate pseudorandom sequences at a rate greater than 20 megabits per second at room temperature and no accumulated radiation dose. More specific is the requirement that the chip operate with a clock frequency of 10.23 MHz over the full temperature range of $-55^{o}C$ to $125^{o}C$ and over the full range of radiation exposure. As in any CMOS design, the maximum speed of operation decreases with increasing temperature. Thus, an ambient temperature of $125^{o}C$ constitutes the worst-case temperature.

The speed requirement applies to the propagation delays on the signal outputs and to the setup times on the signal inputs. It is assumed that the chip is operating in a synchronous system where all signal changes occur on the positive-going clock transition. At 20 MHz this means that the sum of any output propagation delay and the corresponding input setup time must be less than the 50-ns clock period. At 10 MHz this translates into a 100-ns limit on any possible chip-to-chip delays. Hence, in evaluating the speed of the code generator, both the internal inherent speed limitation and the chip-to-chip signal propagation must be considered.

The TCS102 is designed to operate within its performance limits over accumulated gamma radiation dose up to 10^{6} rads(Si). Thus, the array must be designed to handle the threshold shifts, leakage current increases, and mobility decreases associated with this level of gamma radiation exposure. To meet this degree of radiation hardness requires that special circuit design techniques be employed and that special processing using a hardened oxide be employed.

The TCS102 is also designed to withstand a gamma radiation transient pulse. The design objective is no upset or failure of the code generator for transient pulses up to 2×10^{10} rads(Si)/s with a goal of 10^{11} rads(Si)/s. The transient upset requirement is considered in the design of the logic. A radiation transient pulse causes photocurrent generation which can lead to an upset if the circuit design does not compensate for the increased current.

B. DESIGN TECHNIQUES EMPLOYED TO MEET REQUIREMENTS

1. Substrate Clamps on Stacked P Transistors

It has been established that CMOS/SOS transistors suffer degradation in in the form of parameter shifts when irradiated.[1,2] The most significant parameter degradation is the shift in threshold voltage. This threshold voltage shift is highly dependent on the gate-to-substrate bias during radiation exposure. The P transistor threshold voltage becomes more negative, with the maximum shift occurring if the transistor gate is positive with respect to the substrate during radiation exposure. To avoid this worst-case bias condition, the substrates of some P-channel transistors are clamped to the V_{DD} voltage.

In inverters and NAND gates, the source of the P transistor will be connected to V_{DD}. The source-to-substrate diode will be forward biased, preventing the substrate from dropping more than about 0.7 V below V_{DD}. Hence, no design modification is required for these gates to avoid positive P-channel bias. However, NOR gates and compound gates with series P transistors will have P transistors whose source is not connected to V_{DD}. Under certain conditions, the source of these transistors may drift as low as ground with resulting positive bias between gate and substrate. This condition will be avoided if the channel regions of these P-devices are connected to V_{DD}.

On the TCS102, this problem is solved by bringing the channel region out the end of the transistor and connecting it to V_{DD} as shown in Fig. 4-1. To obtain an ohmic contact requires that the N- substrate be brought out to an N+ implant region. The N+ region then connects to V_{DD}, effectively clamping the substrate. This technique was used on all stacked P transistors. Since the channel region has high resistivity (estimated at 10,000 ohms per square), transistors with widths greater than 4 or 5 mils were clamped at both ends.

Although the substrate clamps improve the radiation hardness of the circuits, a slight penalty is paid in device packing density and circuit speed. The area required for a NOR gate, for example, is increased by that of the substrate clamp region and its V_{DD} contact. The speed penalty results from the increased gate capacitance arising from the polysilicon extension into the clamp region. However, the hardness gained more than offsets these penalties when

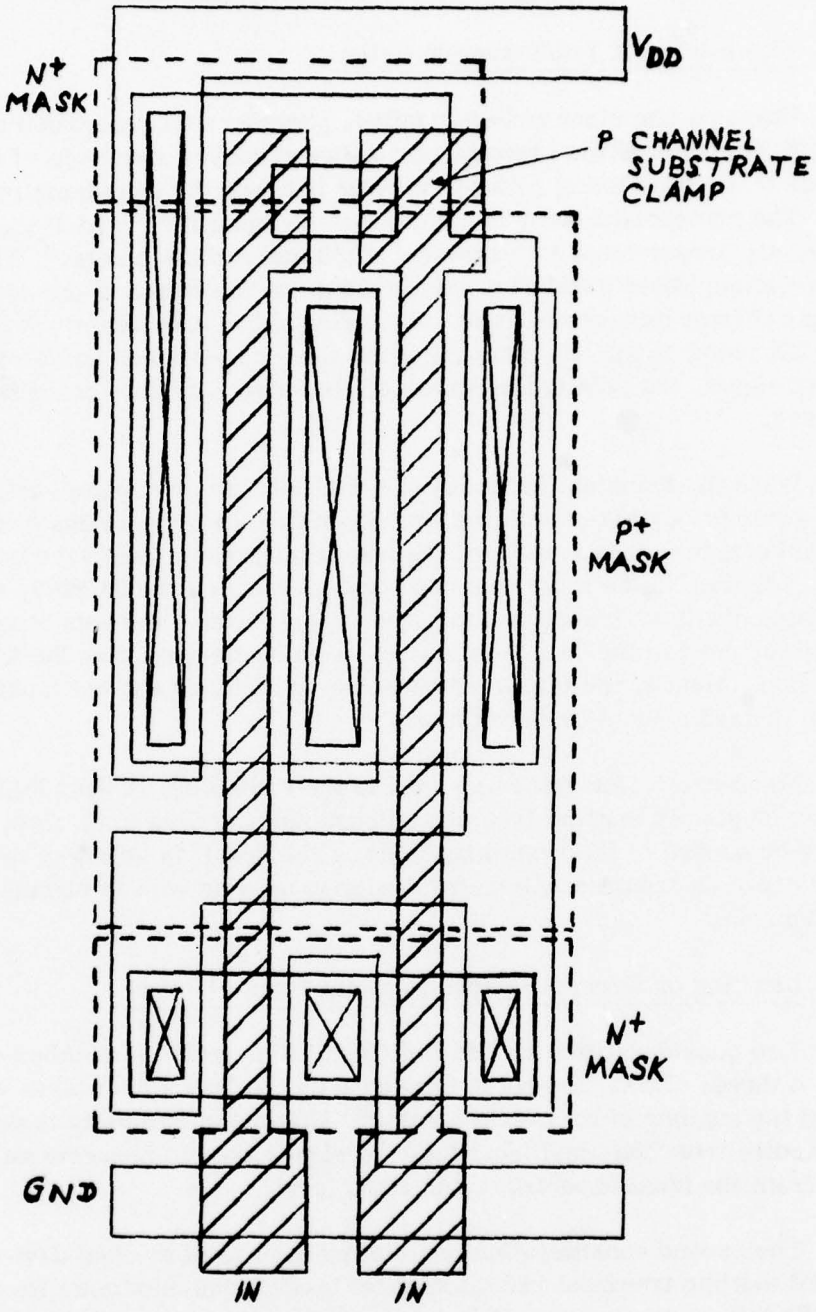


Fig. 4-1. Two-input NOR showing clamps to P device channel.

postradiation performance is examined. Substrate clamps were not used on the stacked N transistors since previous results[2] had shown that they are not as effective in reducing the N transistor leakage as originally anticipated.

2. Elimination of Transmission Gates

During a transient radiation pulse, photocurrent generation occurs in a CMOS/SOS device. This photocurrent between source and drain of the MOS transistor is modeled using a shunt resistor between the transistor source and drain.[3] The photoconductance is assumed to be equal for N and P channels, and to be directly proportional to transistor width and radiation rate.[3] The photoconductance manifests itself as a noise voltage on the output of any logic gate. This noise voltage causes the logic "0" to rise above ground and the logic "1" level to fall below V_{DD}. By comparing the radiation-induced noise voltage on the output signal, the relative hardness of alternate candidate circuits can be determined.

When the transient hardness of a multiplexer or register using transmission gates is compared with the equivalent functional logic designed without transmission gates, it is found that the non-transmission gate version is harder.[2] Since the register is the most common logic element on the TCS102, all registers were designed without transmission gates. Fortunately, the non-transmission gate register used in the TCS102 requires no more devices than the transmission gate version. Hence, the improved hardness is obtained without making any sacrifice in device count or array size.

No transmission gates are used in the remaining TCS102 logic. The transmission gate is suspect from a hardness point of view and, also, none proved to be needed in the remaining logic. The result is an array design without the potentially troublesome transmission gate at no cost in circuit complexity or performance.

3. Limiting of Stacked Devices to a Maximum of Three

Two considerations lead to limiting of the maximum number of stacked devices to three. First, the noise immunity on the inputs decreases with the increase in the number of logic gate inputs.[2] This noise immunity is defined as that departure from the ideal input logic level required to generate an equal departure from the ideal expected output logic level.

The second consideration restricting the use of stacked devices is the requirement that the transient radiation upset level at the maximum feasible value. The NAND gate is more susceptible to upset when all inputs are high, while the NOR gate is most susceptible when all inputs are low. The use of speed-optimized device sizing causes the transient radiation upset level for NAND and NOR gate to go down when the number of inputs is increased. A more complete analysis of the radiation transient upset levels of the NAND and NOR gates may be found in Reference 2.

4. Speed Optimization at the End of Total Dose

The speed of SOS circuits is lower after radiation accumulation than before radiation exposure. When designing to meet a speed requirement over a specified total dose accumulation range, circuit speed performance is optimized at the maximum total radiation dose level. This guarantees the highest possible speed under the worst-case radiation conditions.

The speed optimization at the end of total dose is achieved by using a ratio of 1.8 to 2.0 for the channel widths between P and N devices. If optimized for preradiation performance, this ratio would be nearer 1.5. The P devices are made larger than normal relative to the N devices to compensate for the high P and low N threshold after radiation exposure. Under these conditions, the output rise and fall times are equal.

The device size requirements for speed optimization and radiation transient performance are in conflict. Radiation transient performance is optimized if the photoconductances of the P and N devices are more nearly equal. The difference in the ON resistance of the N and P transistors enters into the calculation of device size ratio for photoconductance compensation. The result is a slightly above unity ratio between P and N channel widths. This ratio in device sizes results in a slower circuit, particularly after the threshold shift of total dose accumulation. The TCS102 is designed using the 1.8-to-2.0 ratio range for speed optimization, rather than using a lower ratio for maximum photocurrent compensation.

C. SIMULATION OF CRITICAL CIRCUITS

The logic circuits used in the TCS102 code generator array were simulated using R-CAP (RCA Circuit Analysis Program) to predict performance under various conditions of radiation and temperature. Specifically, the expected propagation delay of each circuit element at 10 V was determined under the following conditions:

Preradiation at 25°C

Preradiation at 125°C

After 10^6 rads(Si) at 25°C

After 10^6 rads(Si) at 125°C.

Additional simulations were used to investigate the radiation transient performance of critical circuits.

1. Circuit Models Used in Simulation

The R-CAP program allows the user to specify a wide range of circuit design and process parameters in creating the computer model of the circuit to be simulated. Separate models are developed for the total dose and radiation transient simulations as described below.

a. RCA-P Model for Total Dose Simulation

Radiation exposure causes a shift in transistor threshold voltages and a decrease in the device mobility. R-CAP simulations are made using modified threshold and mobility parameters to account for the radiation-induced device degradation. A difficulty in this approach is the dependence of the parameter shift upon the gate bias during radiation. For example, an N transistor irradiated when biased ON will have a different threshold shift from the same transistor when irradiated in the OFF state. Table 4-1 provides a list of device parameters used in the simulations.

A comparison was made between several sets of postradiation device parameters using a register with output driver as the test case. The parameter values are given in Table 4-2 with the propagation delay results provided in Table 4-3. The propagation delay variation is less than 10% between the three cases, Case C having the shortest delay. Case A represents the parameter shift with 0-V bias on the transistor gates during radiation exposure. Case B represents the parameter shift with a 10-V bias. Case C, the intermediary case used throughout the simulations, should more closely approach the parameter shift under dynamic operating conditions.

TABLE 4-1. PARAMETERS USED IN R-CAP SIMULATION

		Preradiation	10^6 Rads(Si)
N Threshold	V	1.5	1.0
P Threshold	V	-1.5	-2.5
N Mobility	$\frac{cm^2}{V\text{-}s}$	400	300
P Mobility	$\frac{cm^2}{V\text{-}s}$	250	220
Oxide Thickness	$\mathring{A}$	850	850
Channel Acceptor Density	cm^{-3}	$3x10^{15}$	$3x10^{15}$
Channel Donor Density	cm^{-3}	$3x10^{15}$	$3x10^{15}$
Channel Length	mils	0.25	0.25

TABLE 4-2. POSTRADIATION PARAMETERS USED IN SIMULATION COMPARISON

		Case A 0-V Bias	Case B 10-V Bias	Case C
N Threshold	V	2.5	0.5	1.0
P Threshold	V	-2.5	-3.5	-2.5
N Mobility	$\frac{cm^2}{V-s}$	380	280	300
P Mobility	$\frac{cm^2}{V-s}$	210	230	220

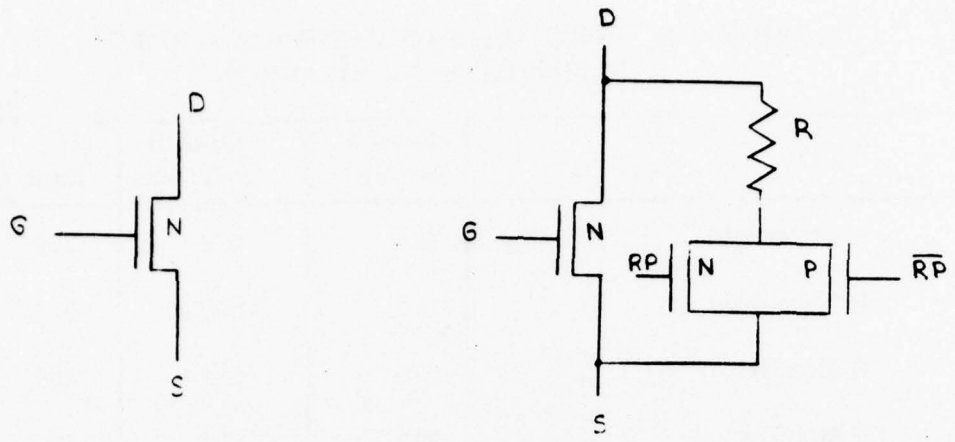
TABLE 4-3. TEN-VOLT PROPAGATION DELAY COMPARISON USING DIFFERENT SETS OF DEVICE PARAMETERS

	Case A	Case B	Case C
Delay Positive Transition (ns)	57	57	54
Delay Negative Transition (ns)	43	44	40

b. R-CAP Model for Radiation Transient Simulation

The radiation-induced photocurrent in an SOS transistor is modeled by placing a shunt conductance between the transistor source and drain.[3] The value of this conductance is directly proportional to the transistor's channel width and, also, directly proportional to the radiation rate. The photoconductances of the N channel and P channel devices are generally assumed to be equal. The factor relating the radiation rate to the shunt conductance is not accurately known. The transient upset simulations on the code generator were made using a factor of 1×10^{-15} mho/ {[mil] [rad(Si)/s]} obtained from curves on test device performance.[4] Although the exact upset level cannot be predicted due to uncertainties in the shunt conductance factor, the results do provide approximate upset levels and will uncover any circuits particularly susceptible to upset.

The clock period of the code generator (approximately 100 ns) is of the same order of magnitude as the length of the radiation pulse. It is a requirement that the code generator continue to function during the radiation pulse without losing code synchronization and without missing a single bit in its output. For modeling the transient effects a transmission gate is placed in series with the shunt resistance in the R-CAP model as shown in Fig. 4-2. The transmission gate is turned ON during the simulated radiation pulse, placing the resistance R in shunt with the transistor. Before and after the radiation pulse the



a. N transistor.

b. N transistor model for transient radiation.

Fig. 4-2. R-CAP model of N transistor used in simulating radiation transient effects.

transmission gate is turned OFF, leaving the transistor free of the shunt resistance. The resistive and capacitive effects of the transmission gate on the simulation are minimized by using a 0.01-mil channel length and a 20-mil channel width in the model. Radiation pulse width and timing effects were investigated by varying the ON time of the transmission gate. The models for the N and P transistors use the same combination of shunt resistance controlled by a transmission gate.

2. Code Generator Stage

Each code generator stage contains a static register and an exclusive-OR which were separately simulated. When evaluating the performance of the register at the different radiation levels and temperature, the clock driver was included in the simulation model to provide clock signals with the expected rise time, fall time, and skew. The complemented clock signal precedes clock in time. The register simulation yields two numbers needed for speed analysis: 1) the setup time of the register, and 2) the clock to output delay of the register. The simulation results are presented in Table 4-4 for the different radiation levels and temperatures. In cases where the delay is data-dependent, the larger value is given.

The signal propagation delays through the exclusive-OR obtained from the R-CAP simulations are presented in Table 4-5. The propagation delay is defined as the elapsed time between the 50% point on the input signal transition and the 50% point on the output signal transition. The output loading in all simulations is the maximum loading seen by the simulated logic in the array. Using the maximum loading and the worst-case transition enables a more accurate prediction to be made of the worst-case signal path.

TABLE 4-4. SIMULATED PERFORMANCE OF CODE GENERATOR REGISTER AT 10 V

Temperature (°C)	Radiation Level (rads(Si))	Setup Time (ns)	Delay To Output* (ns)
25	0	19	17
125	0	25	25
25	10^6	24	26
125	10^6	34	38

*Delay to output measured from 50% point of $\overline{\text{Clock}}$.

TABLE 4-5. SIMULATED PERFORMANCE OF CODE GENERATOR EXCLUSIVE-OR AT 10 V

Temperature (°C)	Radiation Level (rads(Si))	Delay (ns)
25	0	15
125	0	19
25	10^6	18
125	10^6	23

The same logic is used in the master and slave portions of the register stage. Consequently, half of a register stage (Fig. 4-3) was simulated in the radiation transient behavior investigation. Included in the simulation is the logic generating the clock C and $\overline{C}$ signals. This clock logic is included to obtain the degraded clock signal during a radiation pulse. Also included in the simulation is an inverter on the input data line to provide a degraded data input. Simulation runs were made using shunt resistances corresponding to 1×10^{10}, 5×10^{10}, and 1×10^{11} rads(Si)/s radiation rates.

During the radiation pulse the logic "0" voltages rise above ground and the logic "1" voltages fall below V_{DD} (10 V in the simulation). Since the device sizes were chosen to optimize speed rather than for photoconductance compensation, the signals collapsed toward 6 V rather than 5 V at the maximum radiation rate. Optimum photoconductance compensation would require a lower (closer to unity) ratio of p to n transistor channel widths. Table 4-6 gives the approximate logic "0" and logic "1" voltages observed for an inverted output in the simulations

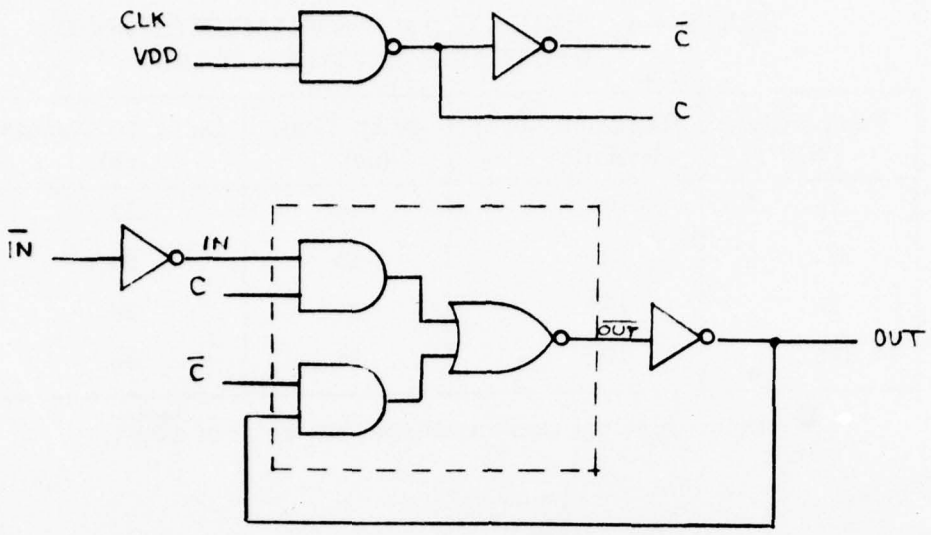


Fig. 4-3. Register circuit investigated in transient analysis.

TABLE 4-6. LOGIC VOLTAGES OBSERVED IN RADIATION TRANSIENT SIMULATION OF REGISTER

Radiation Rate (rads(Si)/s)	Logic 0 (V)	Logic 1 (V)
0	0	10
1×10^{10}	1.0	9.5
5×10^{10}	4.2	7.7
1×10^{11}	5.2	6.8

conducted for the register. Figure 4-4 shows the register simulation run for a 75-ns-wide transient pulse at 5×10^{10} rads(Si)/s. The logic continues to function during the radiation pulse simulation without loss in speed. The reduced signal drive is offset by the similarly reduced signal swing.

The simulated effect of a long transient radiation pulse on the register circuit of Fig. 4-3 is shown in Fig. 4-5. A possible logic failure is indicated when clock C is low, IN is low, and OUT is high. Output OUT drifts to the midpoint of its logic swing before the clock begins to change state. This confirms that the worst-case condition for the register stage is when a logic "0" is on the input and a logic "1" is being stored. The same simulation when made for a radiation rate of 1×10^{10} rads(Si)/s showed no upset problem.

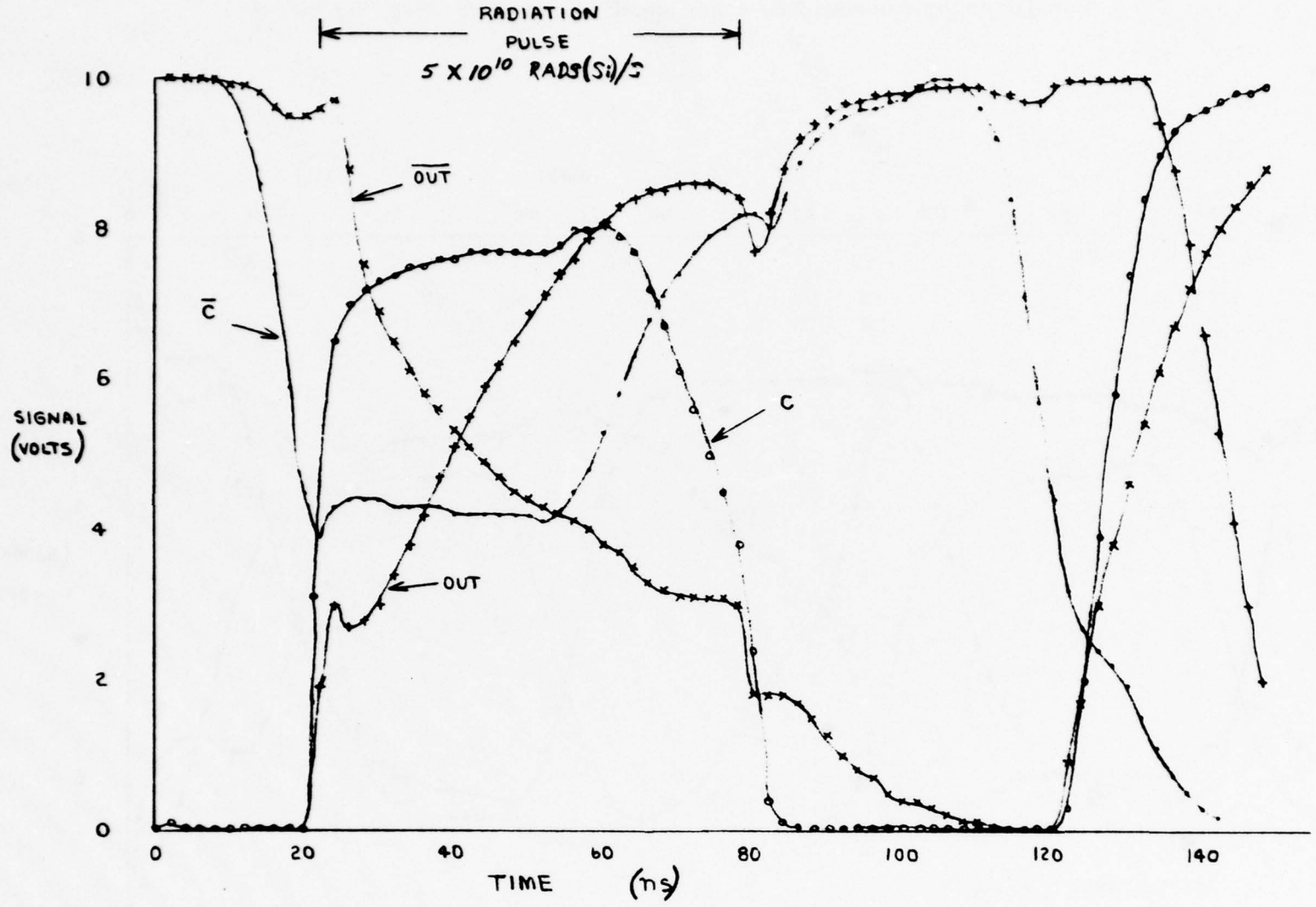


Fig. 4-4. Register simulation with transient radiation pulse at time of clocking.

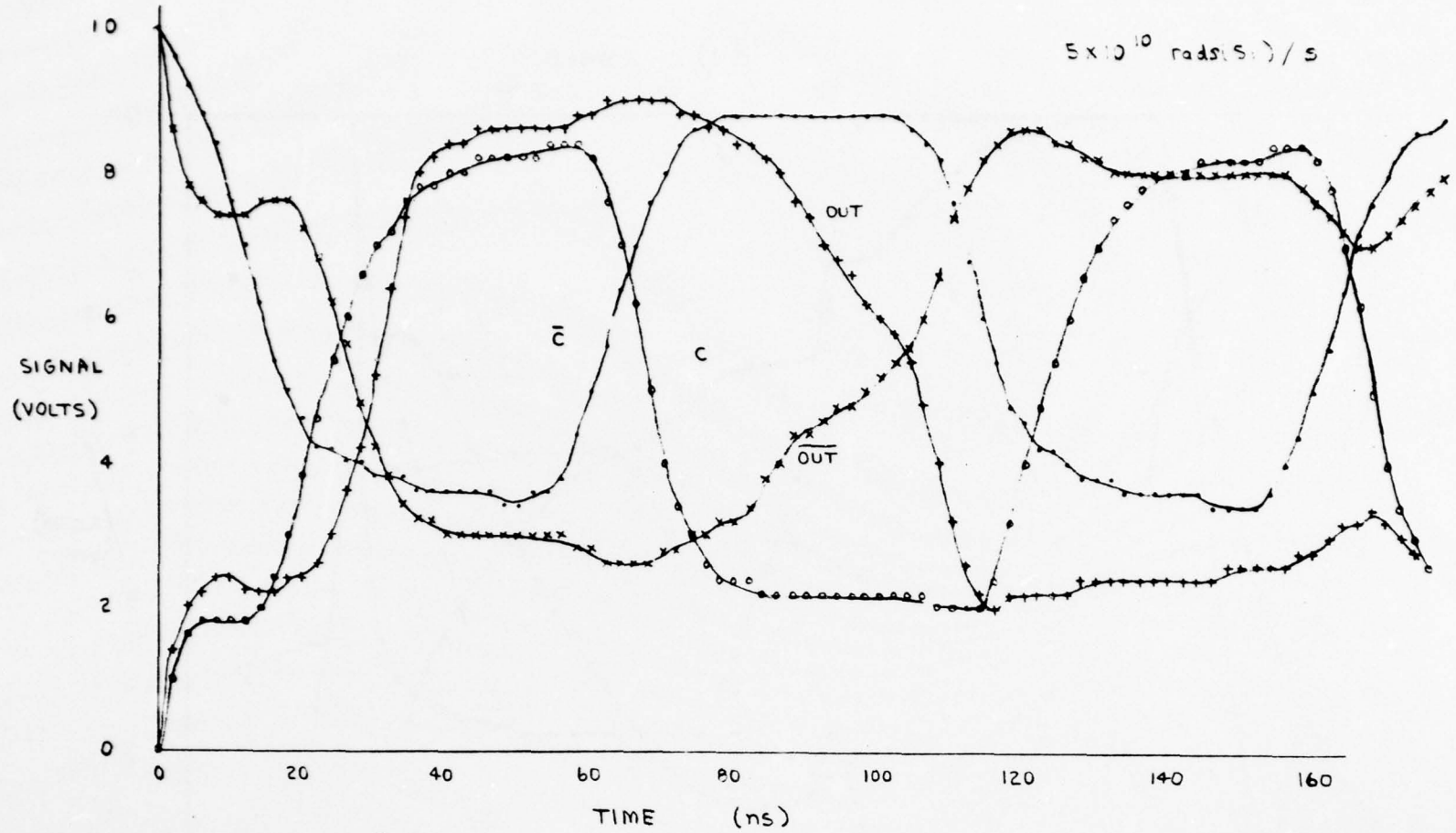


Fig. 4-5. Register simulation with a long transient radiation pulse.

3. Clock Control Logic and Driver

The clock control logic and clock driver involve critical timing considerations in the design and performance of the code generator. Since the loading is greater on the XA clock circuit, it was simulated instead of the XB clock circuit. Once a design was established for the XA clock logic, the same design was used for the XB clock logic.

Each phase of the XA clock drives a capacitive load of 17 pF. The XA clock driver, shown schematically in Fig. 4-6, uses 44-mil-wide transistors in the NAND gate, and 40-mil P and 20-mil N transistors in the inverter. Simulation results for the clock driver are given in Table 4-7. The simulations were run with the array input clock having rise and fall times of 12 ns.

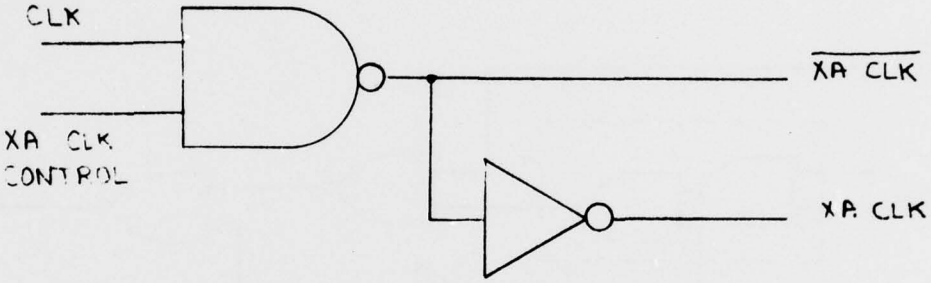


Fig. 4-6. XA sequence generator clock driver.

TABLE 4-7. PREDICTED 10-V XA CLOCK DRIVER PERFORMANCE

Temperature (°C)	Radiation Level (rads(Si))	Delay To $\overline{\text{XA CLK}}$ (ns)	Delay To XA CLK (ns)	XA CLK Rise Time (ns)	XA CLK Fall Time (ns)
25	0	7	13	7	9
125	0	10	17	11	13
25	10^6	8	16	9	11
125	10^6	11	22	14	16

The clock control logic is shown in Fig. 4-7 with simulation propagation delays on several paths being given in Table 4-8. Once the clock control logic has turned the XA clock off, the clock control must be able to respond to a resume or set control to reinitiate the clock. Before the feedback scheme disabling the halt control shown in Fig. 4-7 was designed, a scheme using the pulse-generating circuit of Fig. 4-8 was considered. This circuit was suspect under a radiation pulse and, hence, was subjected to radiation-transient simulation. The circuit failed to produce the desired output signal during a radiation pulse at the 5×10^{10} level and was eliminated from further consideration. No circuits depending on the use of race conditions for signal generation are used on the TCS102 array.

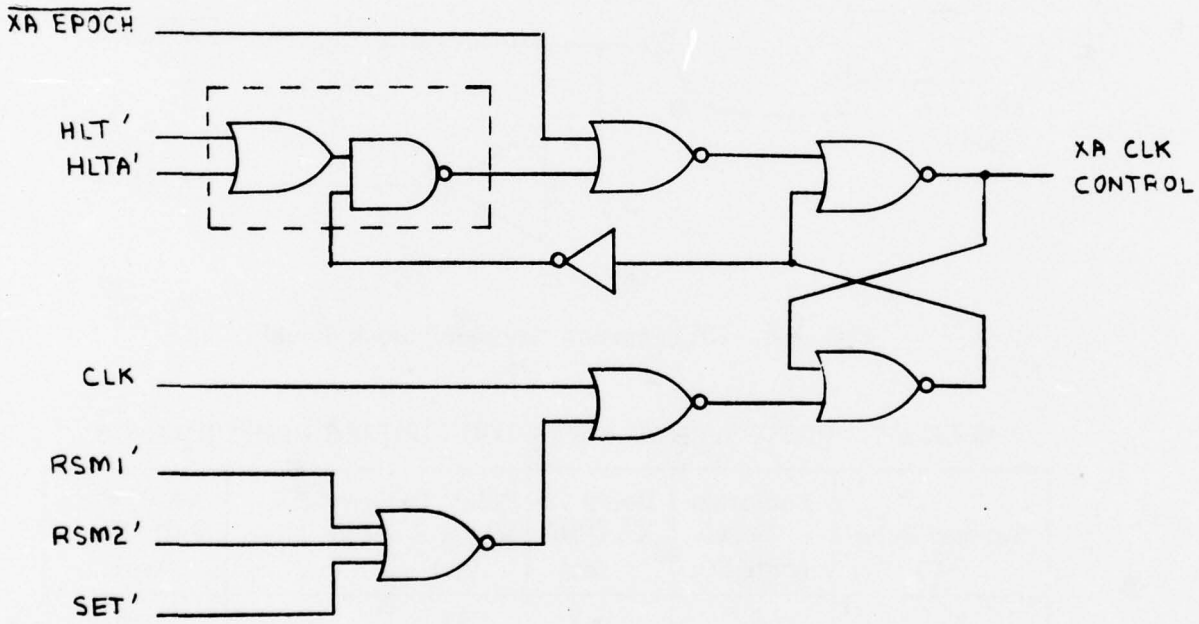


Fig. 4-7. XA clock control logic.

TABLE 4-8. 10-V SIMULATED DELAY TO XA CLK CONTROL OUTPUT

Temperature (°C)	Radiation Level (rads (Si))	Input Signal Delay (ns)			
		HLT' HLTA'	$\overline{\text{XA EPOCH}}$	RSM1' RSM2' SET'	CLK
25	0	26	17	33	25
125	0	36	24	45	35
25	10^6	32	22	43	34
125	10^6	46	32	60	48

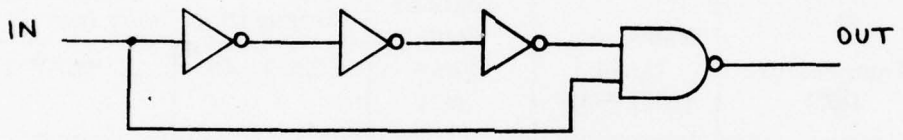


Fig. 4-8. Pulse-forming circuit.

4. Counter Stage

The delay associated with the counter is the sum of delays from three contributing circuits:

a) The delay from the array input clock, CLK, to the buffered on-chip clock, CC.

b) The delay from CC to the counter clock CLKC.

c) The delay from CLKC to the $\overline{\text{CNT}}$ output of an individual counter stage.

The simulated delay results are given in Table 4-9. The delay on the $\overline{\text{CNT}}$ output of the counter makes it necessary to retime the counter output prior to coming off-chip if system speed is to be maintained. The signal propagation delays in the counter retiming register are given in Table 4-10.

TABLE 4-9. 10-V SIMULATED DELAYS IN COUNTER LOGIC

Temperature (°C)	Radiation Level (rads(Si))	Propagation Delay (ns)			
		CLK To CC	CC To CLKC	CLKC To $\overline{CNT}$	CLK To $\overline{CNT}$
25	0	13	15	21	49
125	0	16	21	30	67
25	10^6	14	20	27	61
125	10^6	20	29	40	89

TABLE 4-10. 10-V SIMULATED DELAYS IN COUNTER OUTPUT REGISTER

Temperature (°C)	Radiation Level (rads(Si))	Register Setup Time (ns)	Propagation Delay (ns)	
			CLK To CC	CC To OUT
25	0	19	13	17
125	0	25	26	24
25	10^6	24	14	23
125	10^6	34	20	33

5. Output Driver

The output driver must be capable of driving the larger capacitive loads seen off-chip. In the absence of an output loading specification, the device sizes in the final driver stage were chosen to handle anticipated loads up to 50 pF without serious degradation in either the output rise and fall times or the propagation delay through the output buffer. All the output drivers on the code generator chip use a 25-mil-wide P transistor and a 13.7-mil-wide N transistor in the output inverter.

All the output drivers consist of two inverters in series except for the counter output, which uses a single inverter. The first of the two inverters is intermediary in size between the internal logic and the final inverter. This scaling of device sizes avoids excessive loading on the logic by the output driver.

All the code outputs use an inverter with a 6-mil P transistor and a 3.3-mil N transistor to drive the final output inverter. The intermediary device size step in the counter output is provided by using larger device sizes in the counter register output.

The two types of output drivers were simulated with a 15-pF load on the output. The results are given in Table 4-11.

TABLE 4-11. SIMULATED PERFORMANCE OF OUTPUT DRIVERS AT 10 V WITH A 15-pF LOAD

Temperature (°C)	Radiation Level (rads(Si))	Propagation Delay (ns)		Rise Time (ns)	Fall Time (ns)
		Single Inverter	Double Inverter		
25	0	8	17	12	12
125	0	12	24	17	18
25	10^6	10	22	14	15
125	10^6	14	32	22	22

6. Input Register Setup

As part of the design techniques employed to maintain maximum system speed, all the control inputs are latched into input registers. The setup time is defined as the delay from the data input until the master portion of the register is in the correct state, including its feedback inverter. Since the internal array clock is delayed from the system clock, the effective setup time is smaller. This setup time is the minimum time interval between an input data change and the positive clock transition for reliable clocking in of the data. The input setup times are given in Table 4-12. Input rise and fall times of 15 ns were used in the simulation.

TABLE 4-12. SIMULATED INPUT REGISTER SETUP TIMES

Temperature (°C)	Radiation Level (rads(Si))	Setup Time (ns)	Delay CLK to $\overline{CC}$ (ns)	Effective Setup Time (ns)
25	0	15	7	8
125	0	21	9	12
25	10^6	22	8	14
125	10^6	28	10	18

7. Use of Circuit Simulation Results

The results of the individual circuit simulations were combined to provide the estimated operational speed discussed in Sec. IV.D.

D. PREDICTED SPEED PERFORMANCE

The results of the circuit simulations described above can be combined to make a prediction of the maximum code generator speed. It should be noted that these maximum speed predictions are somewhat pessimistic since worst-case delays are used for all the circuit elements. Circuits used in more than one location were always simulated using the maximum loading case. The delay through most circuits showed some dependence on the direction of signal transition. For example, the delay may be greater when an output makes a low to high transition than it is for the high to low signal transition. In each case the larger number is used without determining whether it is a real possibility. Hence, the propagation delays are an upper bound on the anticipated actual delays.

In determining the internal speed limitation of the array several potential maximum length paths were investigated, with the delays on the four longest paths being given in Table 4-13. These four paths are:

1) The path beginning with the application of clock CC to the register generating CLKC in the counter, through the clocking of the synchronous counter stages, and to the setup of the counter output registers.

2) The path from the application of either XA CLK or XB CLK to the respective sequence generator register, to the generation of the feedback signal, through the exclusive-OR, and to the setup of the code generator register.

3) The path through the sequence generator clock driver, to the output of the epoch delay register, through the clock control logic, and finally back to the clock driver to disable the next clocking.

4) The path consisting of the output delay of the sequence generator register, through the state decode logic, and to the setup of the state decode retiming register.

The maximum clock frequencies before failure as predicted by the internal chip delay paths are:

1) 18.2 MHz at 25°C and 0 rad(Si)

2) 13.0 MHz at 125°C and 0 rad(Si)

3) 13.0 MHz at 25°C and 10^6 rads(Si)

These speed predictions are about 20% lower than the actual measured speed of the radiation-hardened units, reflecting the worst-case nature of the speed prediction.

TABLE 4-13. MAXIMUM INTERNAL 10-V PATH DELAYS FOR TCS102

Temperature (ns)	Radiation Dose (rads(Si))	Delays on Maximum Length Paths (ns)			
		1. Counter	2. XA/XB Generation	3. Clock Halt	4. CG Decode
25	0	55	51	50	55
125	0	76	69	71	77
25	10^6	71	68	66	77
125	10^6	103	95	95	110

The second part of the speed analysis is an examination of the required set-up times on the array inputs and the delay until signals appear on the array outputs. The results of this analysis are given in Table 4-14. The setup time is measured from the 50% point of the input signal transition to the 50% point of the positive-going transition of clock CLK. The output delay is measured from the 50% point of the positive-going CLK transition to the 50% point on the output signal transition with a load of 15 pF.

If it is assumed that the largest output delay when coupled with the largest setup time will define the maximum system speed of the TCS102 array, the following maximum clock frequencies are obtained:

1) 14.3 MHz at 25°C and 0 rad(Si)

2) 10.2 MHz at 125°C and 0 rad(Si)

3) 10.4 MHz at 25°C and 10^6 rads(Si)

The results discussed in Sec. V indicate that the actual performance is better than the predicted, with a greater than 10-MHz operating rate achieved over the full range of temperature and radiation exposure.

E. INPUT PROTECTION

It is necessary to provide protection on the inputs to MOS arrays to prevent damage from static charge. The MOS transistor has an extremely high input impedance which can lead to a breakdown in the gate oxide if a discharge path is not provided for the static charge buildup that can be present on the input during handling. The commonly used input protection on previous nonhardened

TABLE 4-14. SIMULATED 10-V SETUP AND OUTPUT DELAY TIMES FOR TCS102

Signal Name	Type	Setup or Output Delay (ns)			
		0 rad(Si)		10^6 rads(Si)	
		25°C	125°C	25°C	125°C
XA1 - XA12	Out	41	59	56	81
XA	Out	41	59	56	81
XB	Out	41	59	56	81
XA EPOCH	Out	41	59	56	81
X EPOCH	Out	41	59	56	81
CNT1 - CNT12	Out	38	52	47	67
TERM CNT	Out	62	86	82	119
SET	In	8	12	14	18
HLT, HLTA, HLTB	In	8	12	14	18
RSM1, RSM2	In	8	12	14	18
SET CNT	In	8	12	14	18
XA EPOCH	In				

CMOS/SOS arrays used Zener diodes in the protection network. However, Zener diodes produced by the radiation-hardening process are soft. An input protection scheme using gated diodes, arc gaps, and series resistors has been developed by RCA which is compatible with the radiation-hardening process.[5]

The input protection scheme used on the TCS102 is shown schematically in Fig. 4-9. The 45° sawtooth interdigitated arc gap with a 0.8-mil separation shown in Fig. 4-10 provides a breakdown path to ground at higher voltages. The initial voltage for a 1.6-mil arc gap has been measured to be 250 to 275 V.[5]

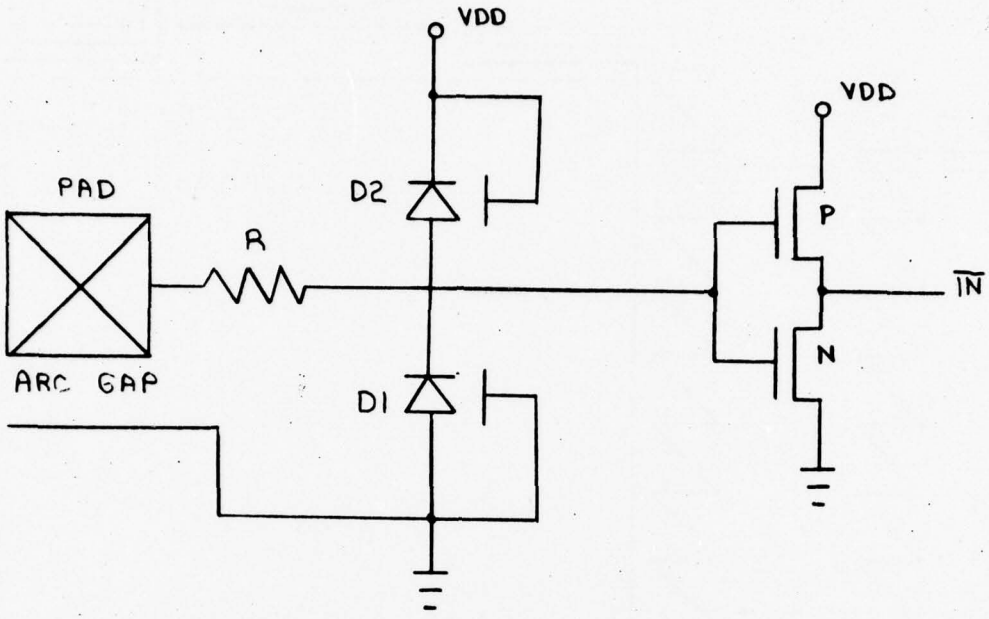


Fig. 4-9. TCS102 input protection.

The selection of the series resistors requires a compromise between speed and input protection. Increasing the resistance provides greater protection but results in a large RC time constant on the input. The TCS102 uses a P+ resistor of approximately three squares. At 60 ohms per square, the resistance is 180 ohms.

The gated diodes are closed-geometry devices with a polysilicon gate shielding the region between the P+ and N+ terminals during the source/drain implant. The result is either a P+PN+ or a P+NN+ diode. One diode is connected between the input and V_{DD} so that it will conduct if the input voltage exceeds V_{DD} by more than a diode drop. The second diode, connected between the input and ground, will become forward biased if the input goes below ground by more than a diode drop. Connected between V_{DD} and ground is another gated diode which is forward biased if ground exceeds the V_{DD} voltage. Device leakage throughout the array will limit any static voltage between ground and V_{DD}. This combination of diodes and leakage prevents the buildup of static charge on any array input.

The final element in the input protection is the use of closed-geometry devices for all transistors with gates that are driven from off the chip. Tests have shown that closed-geometry devices can handle larger gate voltages than normal open-geometry devices without being damaged.[5]

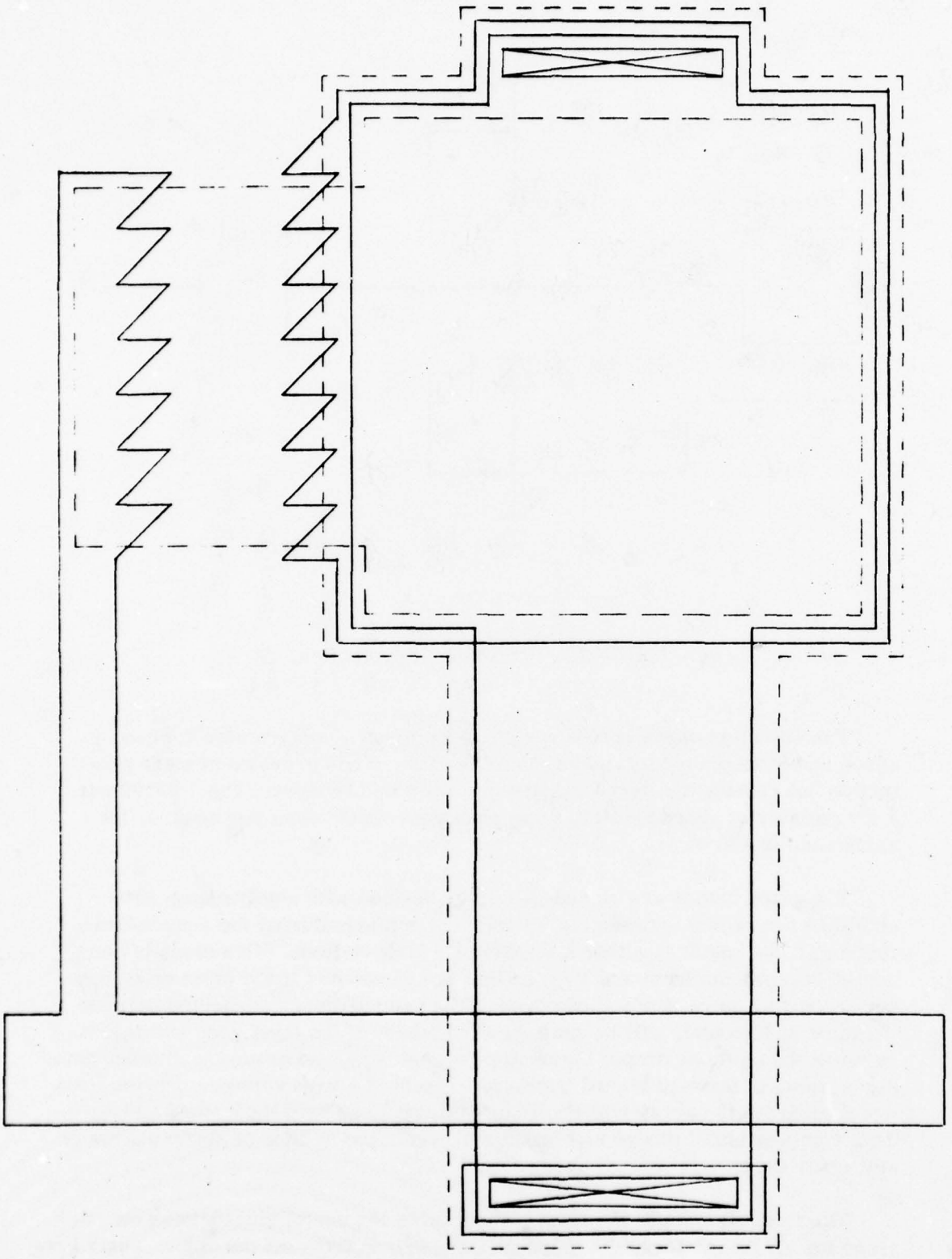


Fig. 4-10. Input pad with arc gap protection.

Section V

RADIATION HARDENED PROCESS

During the code generator contract, the TCS102 arrays were processed using two different CMOS/SOS processes: a standard nonhardened process, and a radiation-hardened process. Both of these processing runs were conducted at the RCA SSTC facility at Somerville, NJ.

The standard process was used initially to verify the design integrity of the array while providing a baseline datum for the later hardened process runs. The standard process was I^2(N/N) and is an ion-implanted procedure that results in a deep-depletion N device and a normal enhancement P device. Both the I^2(N/N) and radiation-hardened processes are described in the following material.

A. STANDARD CMOS/SOS I^2(N/N) PROCESS

Figure 5-1 outlines the processing steps being used in the fabrication of random-logic silicon-gate CMOS/SOS arrays at the RCA SSTC. The five-mask process outlined is perhaps the simplest self-aligned Si-gate process for producing complementary structures that could be envisioned. It has been well documented in the past, and is presented here briefly only because it forms the base from which modifications have been made to improve radiation tolerance.

To begin, a 0.6-μm layer of intrinsic silicon is epitaxially deposited on the specially prepared ($1\bar{1}02$) surface of a sapphire wafer. The silicon is doped N-type by ion implantation. The first mask is then used to define the islands which will be used for forming both the N type and P type transistors. A thermal oxide (the channel oxide) is then grown on both islands. This is the only thermal oxidation step at the island edge, and this fact is largely responsible for the high reliability exhibited by devices so produced. This oxidation is followed immediately by the deposition of 0.6 μm of polycrystalline silicon. This poly is used for the gate electrode and for interconnect tunnels.

A layer of boron-doped glass is then deposited onto the polysilicon and is photolithographically defined into the desired pattern (mask 2). This doped glass is then used as the diffusion source to selectively dope the intrinsic poly. The glass is then removed and poly etched. The boron-doped poly resists attack by the anisotropic etches used, while the intrinsic poly does not. This results in the poly geometry being diffusion defined, rather than etch-rate and undercutting limited, and allows fine control of the poly width.

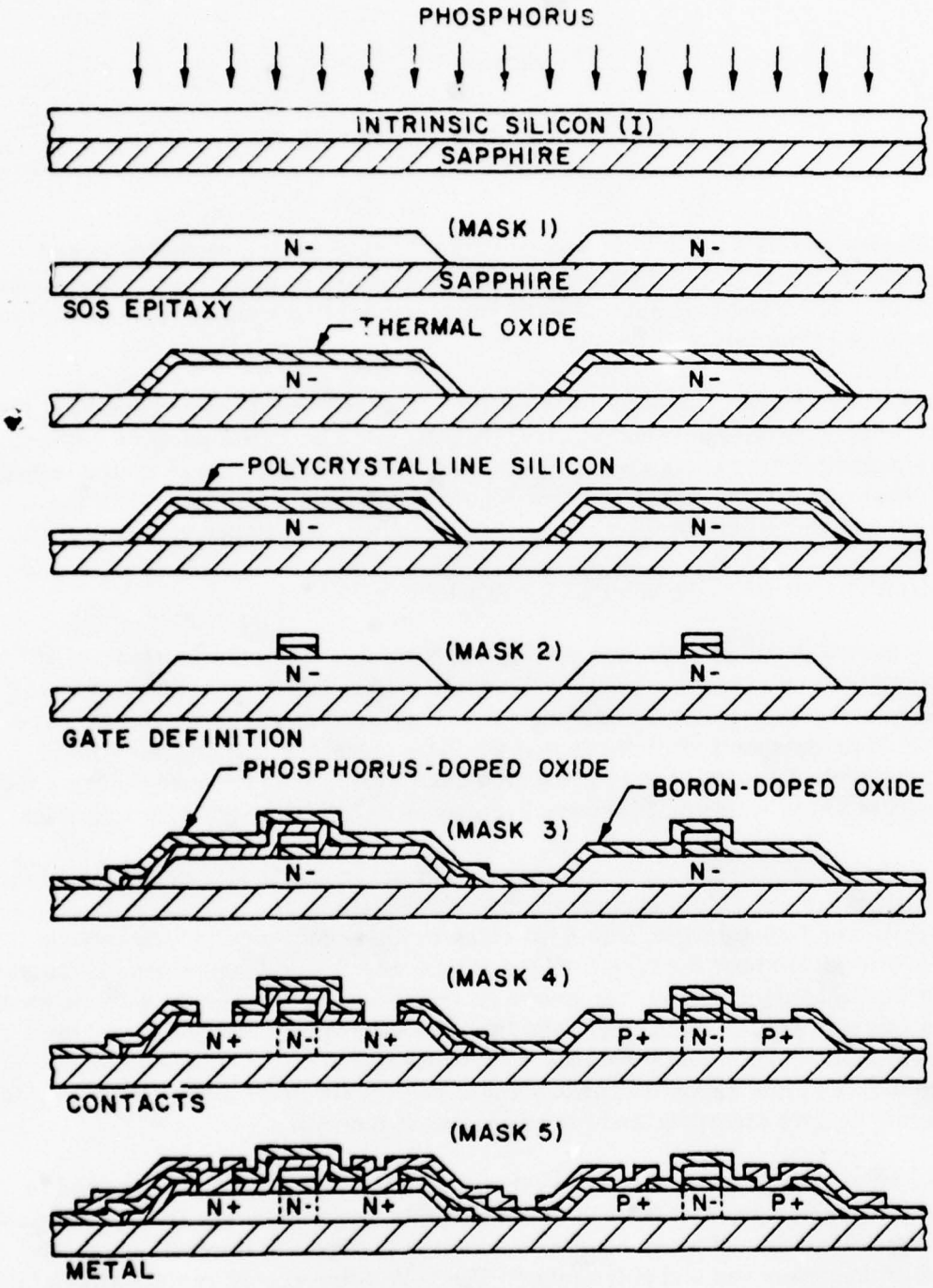


Fig. 5-1. Cross-sectional view of I^2(N/N) CMOS/SOS silicon-gate process.

The poly is then used as an etch mask to clear oxide out of the source-drain electrodes of both transistors. A phosphorus-doped oxide is deposited. This oxide serves as the diffusion source for the source-drain (S-D) doping of the N-type transistor. The phosphorus glass is then defined using mask 3. A deposition of boron-doped glass together with an updoped capping (field) oxide then follows. A single high-temperature diffusion (1050°C) simultaneously dopes the S-D of both the P type and N type transistors. The poly-gate masks the channel region from this diffusion.

The rest of the processing is quite standard. Contacts are opened with mask 4. Aluminum is deposited and defined with mask 5. The final device structure is a deep-depletion N+N-N+ transistor and an enhancement-mode P+N-P+ transistor. The epi thickness, and the substrate doping and channel oxide thickness are set to maintain matched threshold voltages (1.0 V). The deep-depletion transistor is held off by the work function difference between the P+ polysilicon and the silicon.

B. RADIATION-HARDENED CMOS/SOS PROCESS

Figure 5-2 shows some of the changes required to increase the radiation tolerance of the standard CMOS/SOS technology. While the deep-depletion technology has proven manufacturable for standard circuits, it does not offer the degrees of freedom desired when dealing with various oxidation technologies or varying pre-rad thresholds in order to achieve the desired magnitude in total dose. Thus, the first change is to go to a full enhancement-mode structure. The epitaxial silicon is still intrinsic but is reduced to 0.5 μm. The first mask is again used to define islands for both transistors, but now it is used before ion implantation. Photoresist is used as a mask to selectively dope the N- and P-islands by ion implantation. This technique gives an independent variable to adjust threshold voltages. Note also that when the island is defined before the implantation is done, some dopant gradation occurs at the island edges, causing the (111) edge transistor to have a higher threshold than it would have if the sequence is reversed. This aids the radiation tolerance of the N transistor by keeping the edge transistor OFF. Note also that if this same process sequence were used in the standard deep-depletion technology, it would turn the edge device ON!

The preradiation threshold voltages are offset since the N threshold will decrease with dose while the P threshold will increase with dose. Somewhere near the middle of the dose specification, the thresholds are matched and circuit performance is optimized. At this point, the N threshold voltage change usually turns around and starts increasing, while the P threshold keeps monotonically increasing. Since the k factor starts to degrade here, speed degradation becomes serious. In order to minimize this speed degradation, the doping of the N-type channel is kept as low as possible. The work-function difference of the P+ gate structure aids in this regard. Proper choice of implant profiles, along with good quality epitaxy and proper thermal history, keeps the back-channel-leakage problem under control.

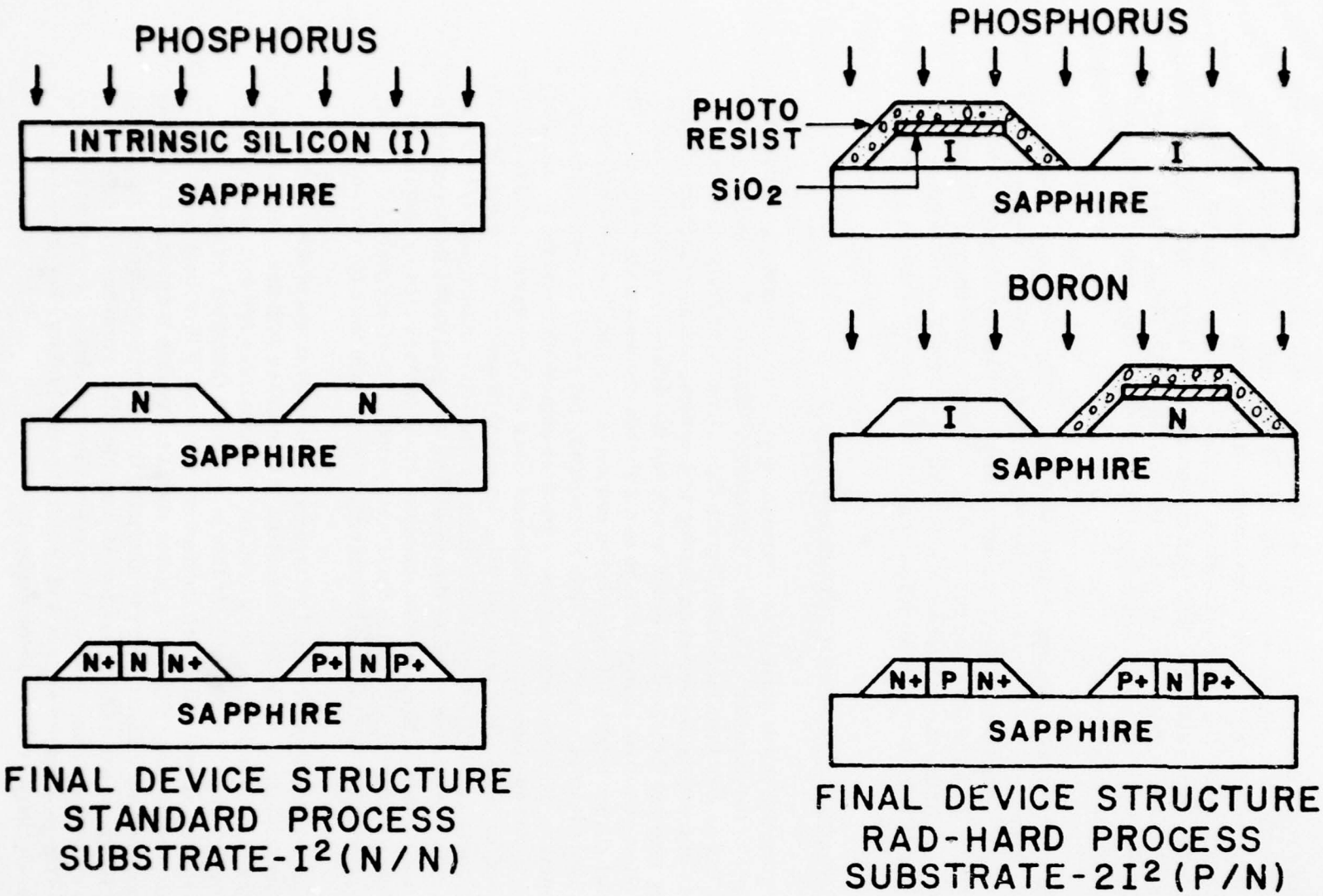


Fig. 5-2. Single-epi double-implant substrate preparation.

The continuation of the process is shown in Fig. 5-3. The channel oxide used on the radiation-tolerant process is chosen to maximize hardness while minimizing back-channel leakage. Initially the 1000°C dry unannealed oxide was used since RCA has considerable experience with it on metal-gate bulk-silicon hardening programs. However, this oxide continued to show about two orders of magnitude worse back-channel leakage than lower-temperature oxides. The final oxide of choice was grown in pyrogenically derived steam at 925°C. The water-vapor percentage is adjusted to control oxidation rate, with a 700 Å oxide being grown in 90 minutes. In-situ anneals in dry O_2 and N_2 (900°C) follow, to establish and control the interface state density.

The polysilicon is deposited doped. It is P type, and is deposited at about 850°C by the pyrolysis of SiN_4 and B_2H_6. The poly, being heavily doped, cannot be defined by the conventional anisotropic etches. Rather, it is etched by plasma or by HF/HNO_3 wet etch. Since the sources and drains will be implanted, there is no need to do the self-aligned oxide etch, and the channel oxide is left intact. This aids in maintaining a reasonable gate rupture voltage when using the thinner (700 Å) channel oxide. Since the poly is doped in-situ to avoid high-temperature processing after the hardened channel oxide is grown, the self-limiting etch characteristics of the anisotropic etch usually used in this step are lost. When resorting to plasma etching of the poly, one must be careful to avoid introducing instabilities or degrading the channel oxide hardness. Finally, the polysilicon etch procedures result in a more abrupt poly step, and careful attention must be paid to the metal deposition and etch steps to ensure step coverage.

Figure 5-3 shows how the processing is completed without any additional high-temperature steps. Ion implantation is substituted for the doped oxide diffusion normally used for the S-D diffusion. Contacts are opened and non-E-gun/non-sputtered clean aluminum is deposited and etched. A low-temperature glassivation overcoat completes the passivation.

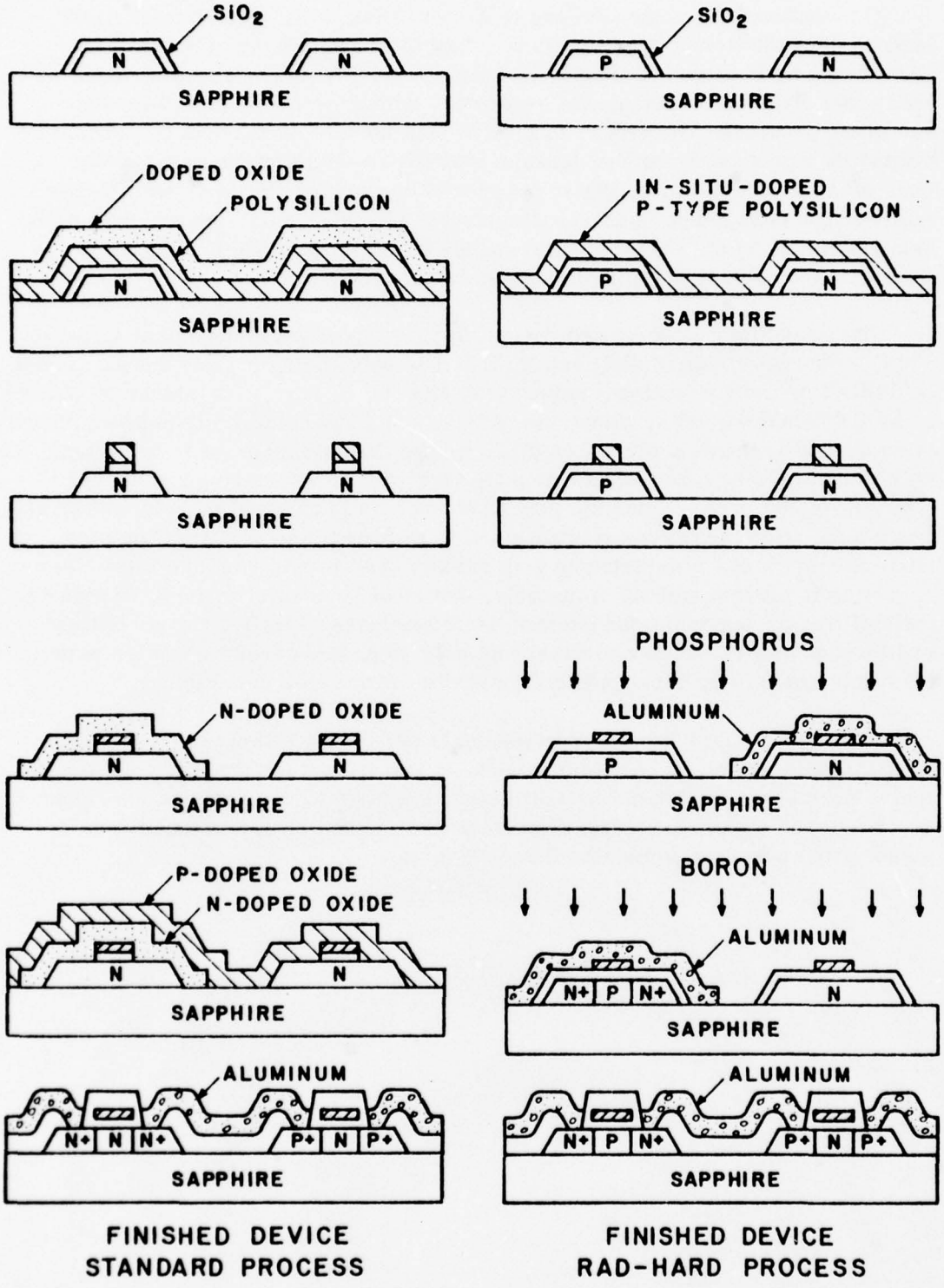


Fig. 5-3. P+ gate CMOS/SOS radiation hardened process.

Section VI

ARRAY PERFORMANCE

The results of characterization tests conducted on TCS102B arrays from several process runs are presented in this section. All of the chips passed the low-speed functional test at 5 and 10 V prior to packaging and characterization. The tested units, process lot number, and the process used are summarized in Table 6-1.

TABLE 6-1. TCS102B CHIPS USED IN CHARACTERIZATION TESTS

Number of Chips	Lot Numbers	Process
11	S1613	Standard $2I^2$(NP/N)
7	S1623	Dry Oxide, P+ Gate
6	S1739	Rad. Hard., Pyro. Oxide, N+ Gate
16	S1855	Rad. Hard., Pyro. Oxide, P+ Gate

The standard process units (lot S1613) and the dry oxide units (lot S1623) constitute the nonhardened units. The radiation-hardened process with N+ gates was used for lot S1739 while P+ gates were used for lot S1855. The N+ gate units failed to meet the radiation specifications. The radiation test results for the P+ gate units, which met the hardness requirements, are described in Sec. VI. C. below. Some of the arrays have been subjected to high temperature and radiation testing in addition to the room-temperature characterization. The characterization results are also compared with the computer simulation predictions.

A. ROOM-TEMPERATURE PRERADIATION CHARACTERIZATION

Chips from each of four process runs were subjected to room-temperature testing to determine the TCS102B speed, power, and signal characteristics. These samples enable a comparison to be made between different processes and process runs. Room-temperature characterization results are described in Sec. VI. B.

1. Maximum Speed of the Code Generator

The maximum speed before failure was measured by monitoring the XA and XB code outputs as the clock frequency is increased. The XA EPOCH out is used as the SYNC pulse to the oscilloscope. The XA code repeats synchronously with the XA EPOCH, while the XB code repeats every 4093/4092 XA EPOCHs. By monitoring the waveforms any failure in either XA, XB or the XA EPOCH will be detected. A failure in either of the two sequence generators will result in one of these outputs being bad.

The maximum code generator clock frequency while operating at 10 V is given in Table 6-2. All chips exceeded the simulated maximum frequency of 18.2 MHz except two chips from lot S1855. As is expected, the fastest units are those processed using the standard process. The maximum clock frequency at 5 V is given in Table 6-3. Most units, when tested at 5 V, met the 10 V speed specification. The maximum clock frequency as a function of operating voltage for a typical chip from lot S1613 is shown in Fig. 6-1.

TABLE 6-2. TCS102B MAXIMUM ROOM-TEMPERATURE CLOCK FREQUENCY (V_{DD} = 10 V)

Lot Number	Number Units Tested	Average Maximum Frequency (MHz)	Lowest Maximum Frequency (MHz)
S1613	10	28.4	27.2
S1623	5	27.8	27.0
S1739	6	24.2	21.1
S1855	16	21.1	16.6

TABLE 6-3. TCS102B MAXIMUM ROOM-TEMPERATURE CLOCK FREQUENCY (V_{DD} = 5 V)

Lot Number	Number Units Tested	Average Maximum Frequency (MHz)	Lowest Maximum Frequency (MHz)
S1613	10	14.0	12.7
S1623	5	11.1	10.7
S1739	6	11.0	10.6
S1855	16	9.6	6.8

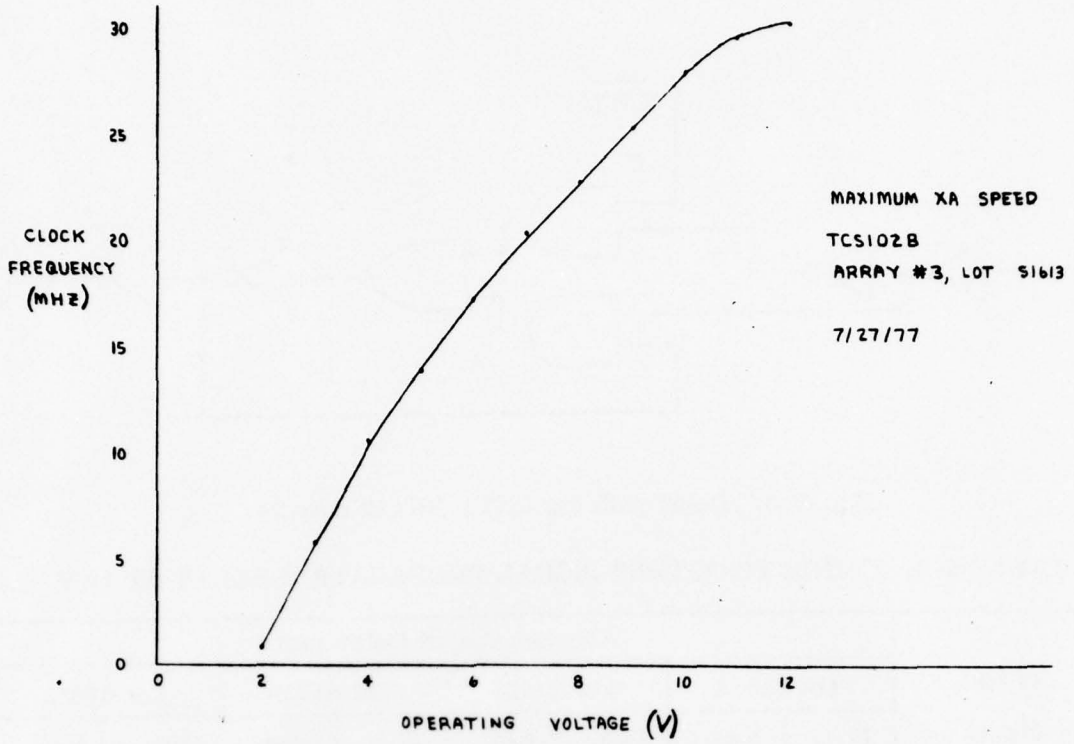


Fig. 6-1. TCS102B code generator speed vs. operating voltage.

2. Output Propagation Delay

The signal propagation delay between the clock input to the TCS102B and various outputs was measured. This output delay is defined as the elapsed time between the 50% point on a positive-going clock transition and the 50% point on the resulting output transition. Included in this path is the delay through the on-chip clock buffer, the output time of a register, and the delay through the output buffer (Fig. 6-2 and 6-3). The results, given in Table 6-4, are for 10 V operation with the outputs lightly loaded (3-5 pF).

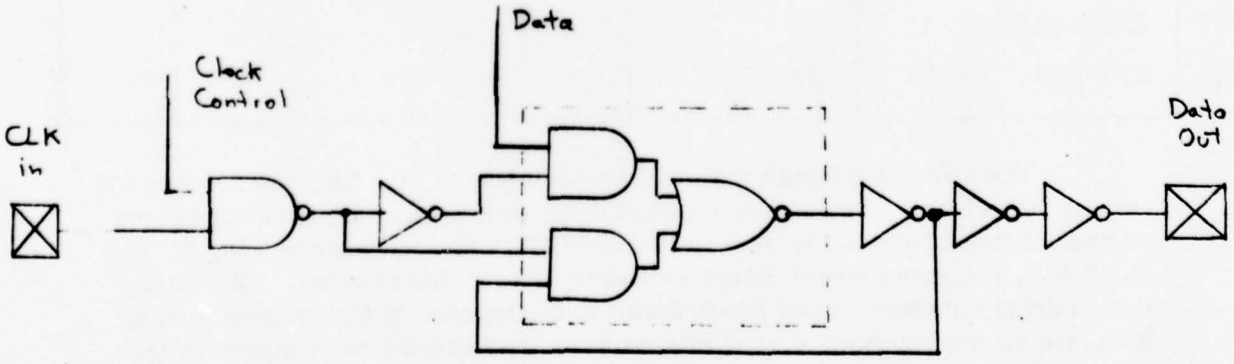


Fig. 6-2. Delay path for XA, XB, XA1-XA12 and XA EPOCH outputs.

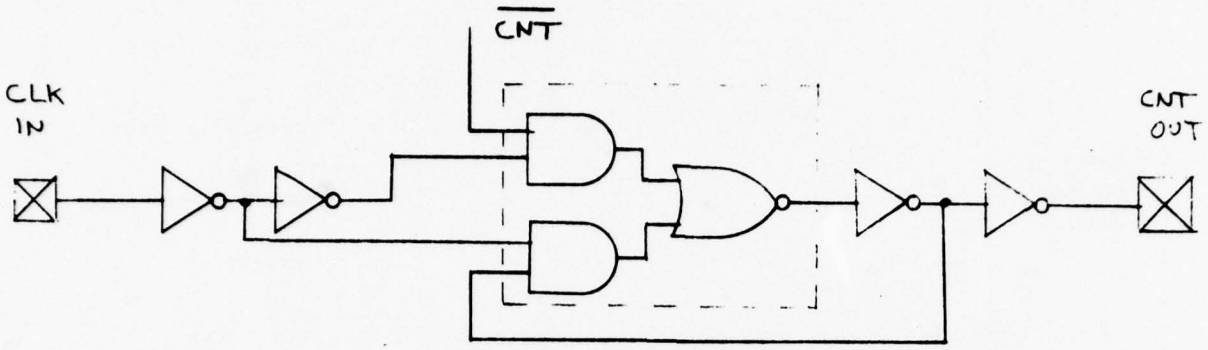


Fig. 6-3. Delay path for CNT1-CNT12 outputs.

TABLE 6-4. CLOCK TO OUTPUT SIGNAL PROPAGATION DELAY AT 10 V

Output Signal	Average Output Delay (ns)							
	Lot S1613		Lot S1623		Lot S1739		Lot S1855	
	Pos. Trans.	Neg. Trans.	Pos. Trans.	Neg. Trans.	Pos. Trans.	Neg. Trans.	Pos. Trans.	Neg. Trans.
XA1-XA3	31.0	26.6	31.9	27.8	42.9	39.4	41.7	40.9
XA4	38.0	34.6	39.6	37.1	48.8	46.5	49.8	49.1
XA5-XA12	27.4	22.5	29.3	24.3	38.5	34.2	38.1	35.7
XA	28.0	22.8	29.6	24.3	38.8	34.5	38.6	36.2
XB	35.5	31.7	38.0	35.1	42.2	39.3	43.6	43.5
CNT1-CNT12	25.3	26.6	24.2	29.2	33.2	36.0	30.0	35.5
XA EPOCH	30.3	27.9	31.0	30.7	42.8	40.2	-	-
TERM CNT	42	40	-	-	-	-	-	-
XEPOCH	32	33	-	-	-	-	-	-

The simulated output delay on the XA1-XA12, XA, XB, and XA EPOCH outputs was 41 ns. The measured output delay is less than the simulated 41 ns on each of these outputs for lots S1613 and S1623. The two slower lots, S1739 and S1855, had some output delays exceeding the simulated value. The variation in delay between outputs is attributed to differences in the internal loading. XA4, the slowest output, is used internally as the feedback to 10 stages in the XA sequence generator. The next slowest of these outputs, XB, is used as the feedback to five stages in the XB sequence generator. The XA1-XA3 outputs

have more resistance in the signal path than the XA5-XA12 outputs. Although the logic and output driver sizes are the same on these outputs, the loading and layout variations are responsible for a 25% variation in output delays.

The measured delays on the CNT1-CNT12 outputs are all less than the simulated value of 38 ns. All the counter outputs are identical in design and layout and, hence, little variation in delay exists between the individual outputs. The count output circuit uses one less inverter in the output driver than is used by the code output driver. There are six gate delays on each code output path and five gate delays on each count output path.

The TERM CNT and X EPOCH are infrequently occurring signals, making delay measurements on these outputs difficult. The 47-ns TERM CNT delay measurement on lot S1613 is 32 percent lower than the simulated value of 62 ns. If the lot-to-lot variation remains the same as on the other outputs, the TERM CNT delay is within the simulated delay for all four lots. The X EPOCH delay of 33 ns is approximately the same as the various code output delays.

Clock to output signal propagation delays at 5 V are given in Table 6-5 for lot S1739. Corresponding measurements on lot S1855 were not taken. Similar delays would be expected.

TABLE 6-5. FIVE-VOLT OUTPUT PROPAGATION DELAY FOR LOT S1739

Output Signal	Average Output Delay (ns)	
	Positive Transition	Negative Transition
XA1-XA3	74.2	65.0
XA4	91.2	84.0
XA5-XA12	65.8	55.1
XA	66.4	56.0
XB	82.4	77.2
CNT1-CNT12	50.8	60.4
XA EPOCH	66.4	64.4

The propagation delay is a function of the output load. Figures 6-4 through 6-6 show the propagation delay on XA and XB outputs as a function of the capacitive load for lots S1613 and S1623. These curves show that the output delay of the code generator increases by approximately 0.2 ns for each additional picofarad of output loading.

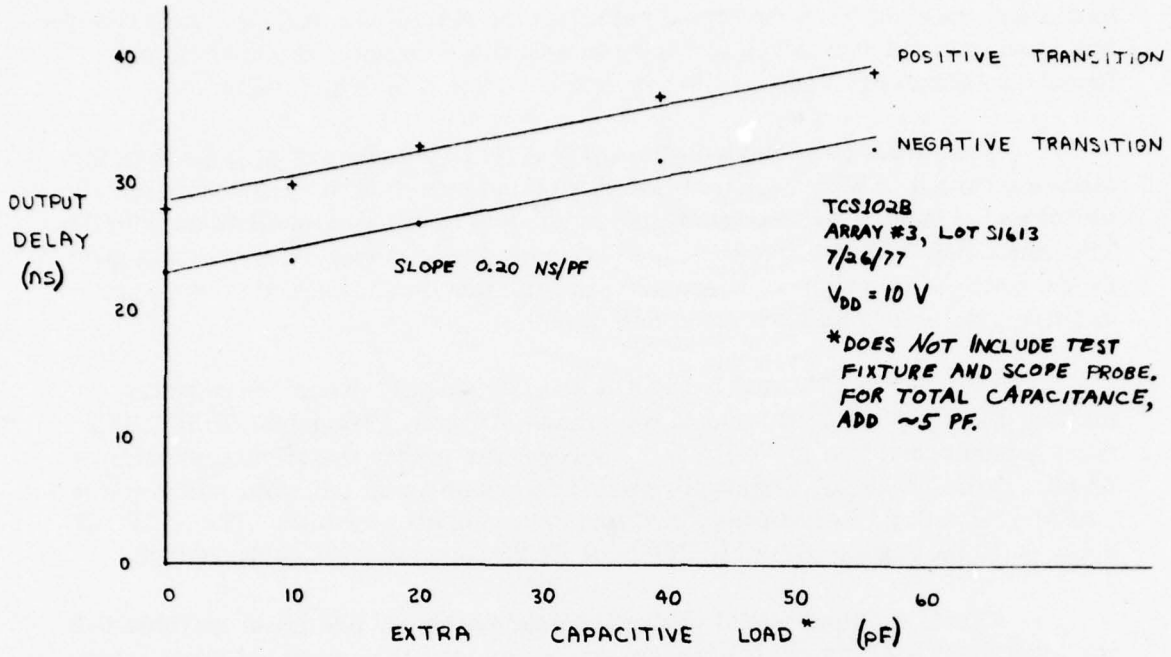


Fig. 6-4. Clock to XA output delay of the TCS102B code generator.

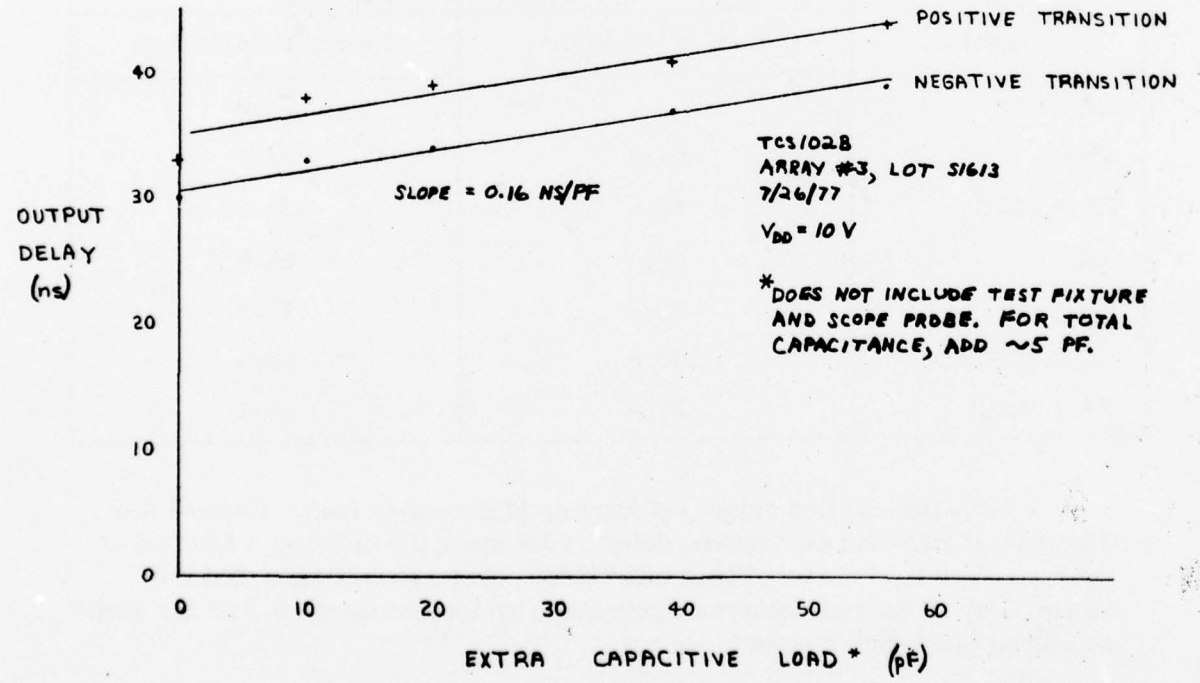


Fig. 6-5. Clock to XB output delay of the TCS102B code generator.

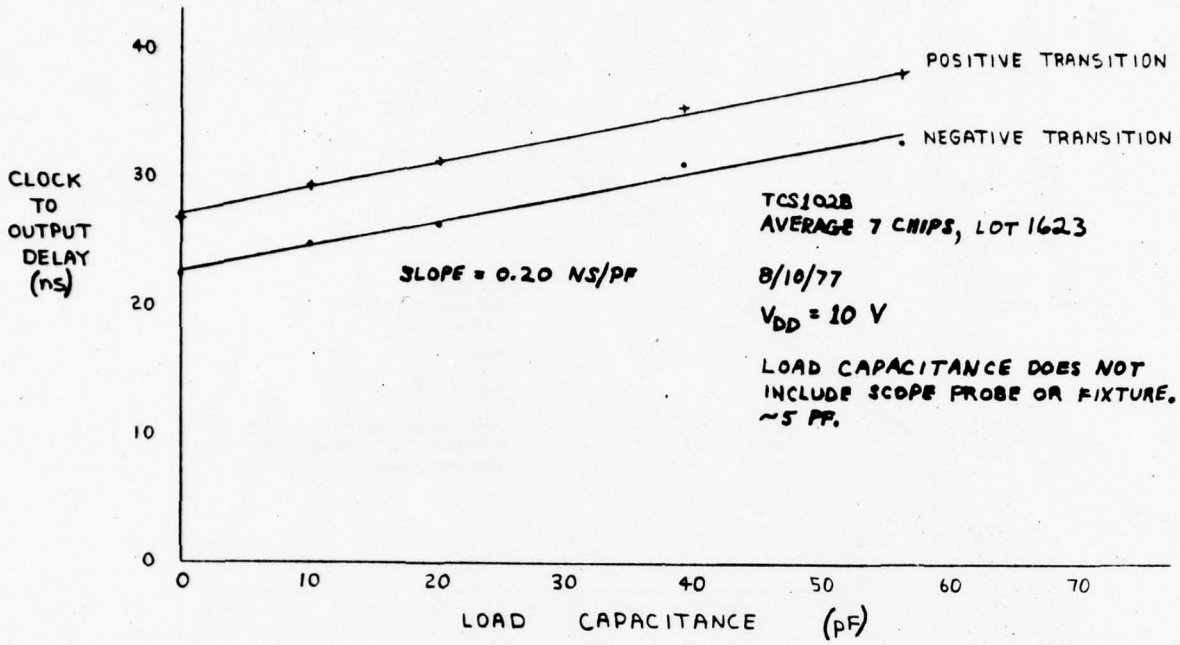


Fig. 6-6. Clock to XA output delay.

3. Output Rise and Fall Times

The XA output rise and fall time as a function of the capacitive load is plotted in Fig. 6-7 for arrays from lot S1623 operating at 10 V. Since each output driver uses a 13.7-mil N transistor and a 25-mil P transistor, the output rise and fall times are approximately the same for the other code generator outputs. The rise and fall times increase by approximately 0.4 ns for each picofarad of load.

4. Power Dissipation

The power dissipation of a CMOS/SOS array can be broken down into two components, the static power which is independent of operating speed and the dynamic power which increases linearly with operating speed. The TCS102 is designed with no logic circuits which dissipate static power. Hence, the only static power dissipation on the TCS102 is that resulting from device leakage current.

A plot of leakage current as a function of the power supply voltage is given in Fig. 6-8. The leakage current was measured at the V_{DD} input to the array. The distribution of 10-V leakage currents for the different process runs is given in Fig. 6-9. In cases where the leakage depended on the state of the code generator, the larger value was chosen.

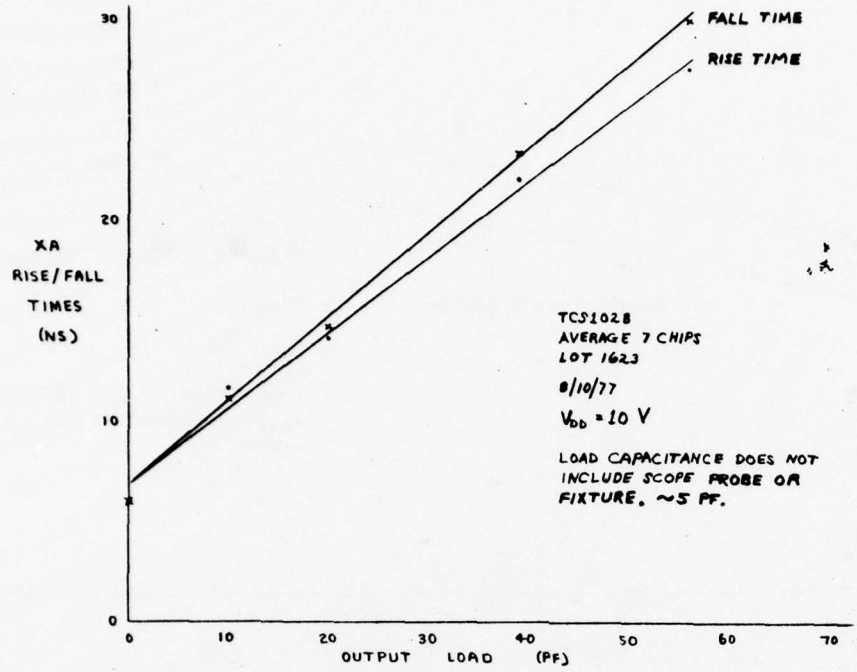


Fig. 6-7. XA output rise and fall times vs. load.

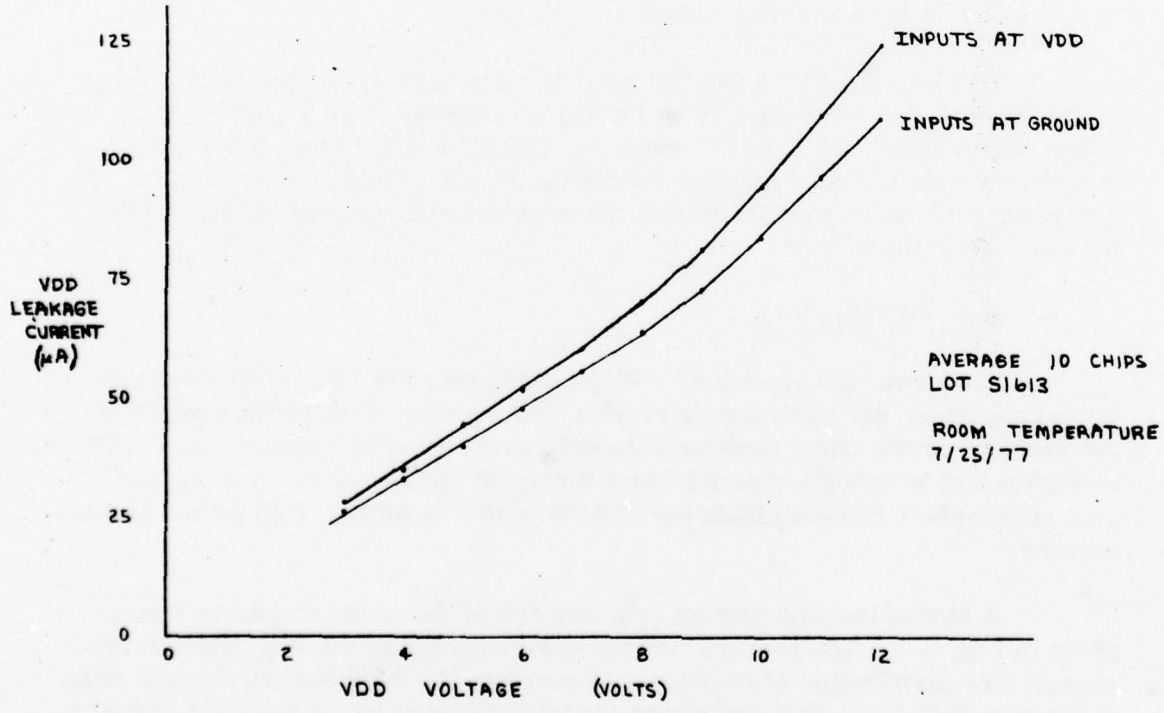


Fig. 6-8. TCS102B leakage current vs. V_{DD} voltage.

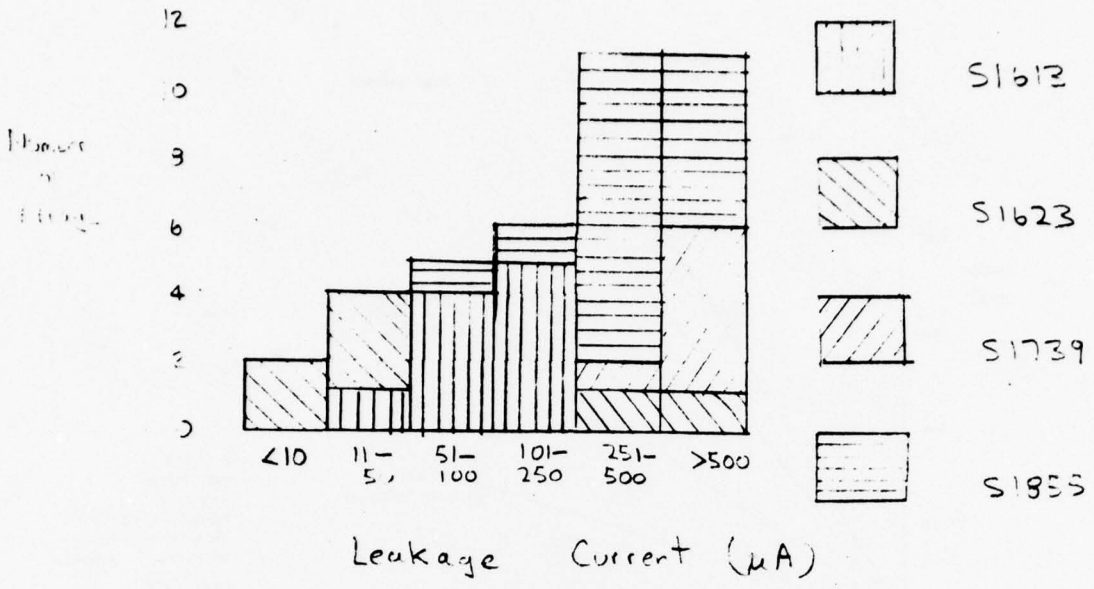


Fig. 6-9. TCS102 10-volt leakage current distribution measured at room temperature.

The TCS102B dynamic power dissipation was measured under several operating conditions with the outputs either unloaded or lightly loaded. Figure 6-10 is a plot of the power dissipation as a function of the clock frequency. The TCS102B was operated with the XA $EPOCH_{out}$ connected to the XA $EPOCH_{in}$. In the "no-code-being-generated" case the clock is turned OFF to both the XA and XB sequence generators. The remaining curves are for the cases where: 1) the XA sequence only is being generated; 2) the XB sequence only is being generated; or 3) both XA and XB sequences are being generated. The dynamic power increases linearly with frequency and, hence, can be specified by the slope of the power versus frequency curve as given in Table 6-6. The TCS102 requires between 156 and 227 mW of power when producing both sequences at a 10 megabits/s rate while operating at 10 V. At 5 V, only 33 to 44 mW are required for the 10 megabits/s code rate.

The dynamic power data taken with selective portions of the TCS102B turned OFF allows the power dissipation in separate sections of the array to be determined. For example, the 10-V power dissipation for arrays from lot S1613 operating at 10 MHz can be broken down as follows:

1) 43 mW in those portions always clocked such as the input retiming registers and counter output registers.
2) 48 mW in the XB sequence generator producing XB.
3) 122 mW in the XA sequence generator producing XA.

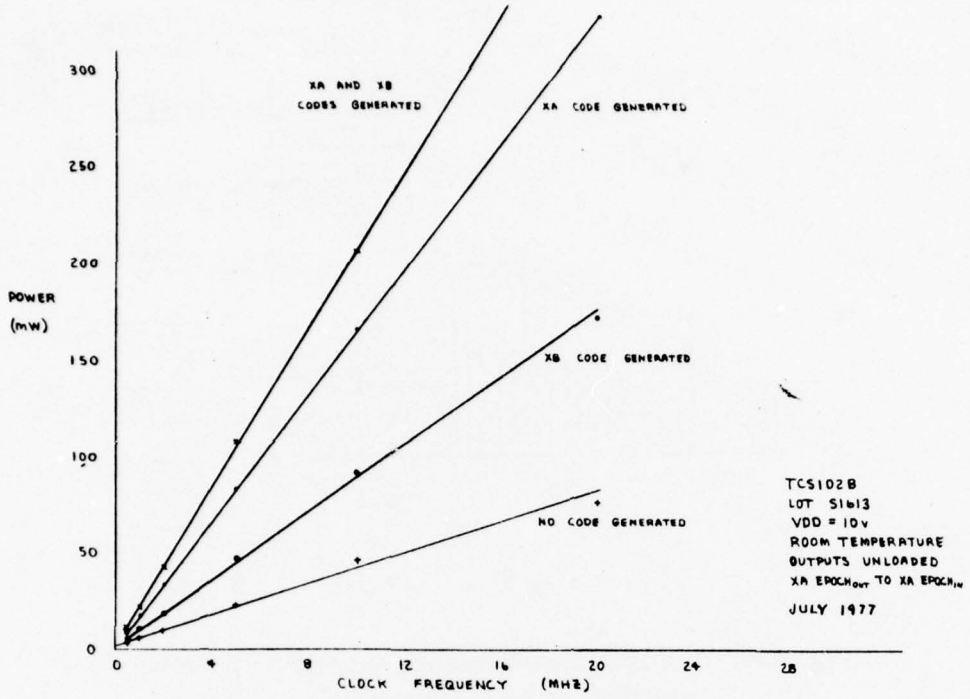


Fig. 6-10. TCS102B power dissipation.

TABLE 6-6. DYNAMIC POWER DISSIPATION FOR TCS102B CODE GENERATOR

Lot #	Voltage (volts)	Dynamic Power (mW/MHz)			
		No. Code	XA Only	XB Only	XA and XB
S1613	10	4.3	16.5	9.1	21
S1623	10				15.6
S1739	10	4.4	17.8	9.8	22.7
S1855	10	4.2	17.1	9.5	22
S1613	5				4.3
S1623	5				3.3
S1739	5				4.2
S1855	5				4.4

The larger power dissipation for the XA sequence generator is primarily due to the 12-stage serial register extension, the additional output drivers for XA1-XA12, and the registers used in the XA EPOCH logic. The counter contributes less than a milliwatt of power to the total when the counter output register power is excluded. The counter is clocked only once for every 4092 periods of the input clock.

An estimate of the anticipated dynamic power dissipation was made by determining the internal array capacitances based upon the array layout. The capacitances obtained are 130 pF on circuit nodes changing at the clock rate and 210 pF on nodes changing at the data rate. A capacitance of 4 pF was assumed on each output, 14 of which change state at the data rate. The array dynamic power can be predicted from:

$$P = C_{clock} V^2 f + 1/4\ C_{data} V^2 f + 1/4\ C_{out} V^2 f.$$

Substituting the capacitance estimates into this equation yields 19.6 mW per megahertz, well within the measured range of power dissipation.

The power dissipation in the counter was measured when counting at half the clock frequency. During these measurements neither the XA nor the XB code was being produced. The slopes of the dynamic power curves obtained are given in Table 6-7.

TABLE 6-7. TCS102B POWER DISSIPATION WITH COUNTER ONLY BEING OPERATED

Lot #	Voltage (V)	Dynamic Power (mW/MHz)
S1613	10	7.2
S1623	10	5.5
S1613	5	1.5
S1623	5	1.2

5. Input Clock Waveform Requirements

The minimum width clock pulse to which the TCS102B will respond was measured for a typical chip from lot S1613, with the results given in Table 6-8. The width of the clock pulse was measured between the 50% points on the clock waveform. The minimum width of the high portion of the pulse was 12 ns at 10 V and 32 ns at 5 V. The minimum width of the low portion was even less. These results indicate considerable tolerance to variations in clock duty cycle.

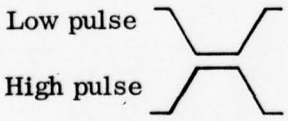
TABLE 6-8. TCS102B INPUT CLOCK DUTY CYCLE

Voltage (V)	Pulse Type	Pulse Width (ns)	Rise Time (ns)	Fall Time (ns)
10	Low	9	4.5	4.5
10	High	12	4.5	4.5
5	Low	16	5	5
5	High	32	5	5

NOTES:

Minimum pulse width at which the chip operates.

Measured on chip #3 operating at 10.23 MHz.



The maximum rise and fall times on the input clock without a failure are given in Table 6-9 for chips from lots S1613 and S1623. None of the chips with input clock rise or fall times less than 2 μs at 10 V failed.

6. Input Setup Times

Each of the control inputs is retimed by a register on the code generator array. Hence, the parameters of interest on these inputs are the setup and hold times. The control signal rise and fall times do not matter so long as the correct level is established at the time that the clock makes its positive-going transition. The setup time is defined as the time the input must be present prior to the positive clock transition. The hold time is the minimum time the input must remain unchanged following the positive clock transition. Measured values from lot S1613 yielded a setup time of 4 ns and a hold time of 7 ns. This

TABLE 6-9. TCS102B CLOCK MAXIMUM TRANSITION TIME

Array No.	Maximum Rise Time (μs)	Maximum Fall Time (μs)
1	3.2	8
2	2.8	8
3	5.2	21
4	2.0	8
5	2.8	8
6	5.0	21
12	9	26
13	9	23
14	10	31
15	8	13
16	7	28
18	9	20

NOTES:

Measured between 0 and 100% points on the ramp.

Clock rate is 5 kHz.

defines a range of time around the positive clock transition during which the inputs are to remain constant if ambiguous results are to be avoided.

B. PERFORMANCE OVER TEMPERATURE

Three chips from lot S1613 were tested over the temperature range from 25°C to 125°C, with the results being presented here.

1. Maximum Speed of the Code Generator

A plot of the 10-volt maximum speed for the three TCS102B chips from lot S1613 as a function of temperature is given in Fig. 6-11. The decrease in speed is linear with increasing temperature. At 125°C the internal speed is approximately 14 percent lower than the speed at 25°C. This speed decrease is less than the predicted speed decrease of 28.5 percent between 25°C and 125°C.

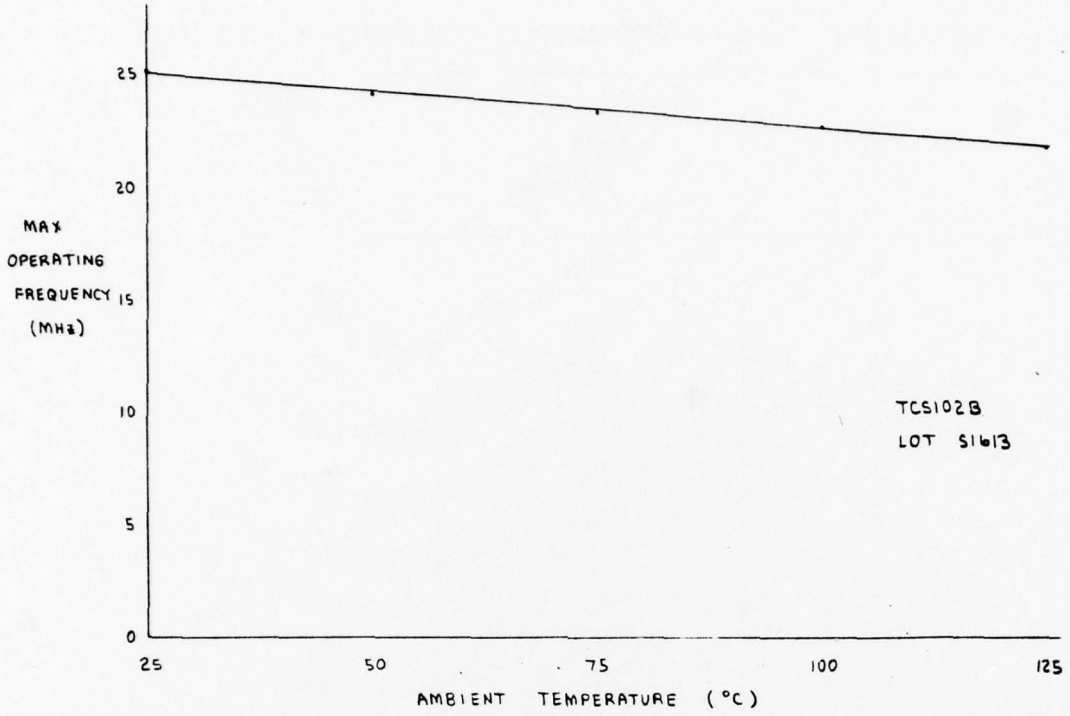


Fig. 6-11. Maximum code generator speed vs. temperature.

2. Output Propagation Delays

Output signal propagation delay as a function of temperature is given in Table 6-10 for selected outputs. The higher initial room temperature values are attributed to the additional loading and signal cable length required to access the chip in the temperature chamber. The percentage increase in delay at 125°C over 25°C ranged from 13 to 23 percent, less than predicted by the simulations. The percentage increase will be closer to the predicted if the test setup effects are eliminated by subtracting approximately 10 to 14 ns from all values.

3. Power Dissipation

Both the leakage power and the dynamic power increase at elevated temperatures. The dynamic power increase with temperature is relatively small, as indicated by the results presented in Table 6-11. The leakage current increase with temperature is more dramatic, as shown in Fig. 6-12. The leakage current at 125°C is greater than the 25°C leakage current by a factor of 100.

TABLE 6-10. TEN-VOLT CLOCK-TO-OUTPUT DELAY AS A FUNCTION OF TEMPERATURE

Output Signal	Transition	Clock-to-Output Delay (ns)				
		25°C	50°C	75°C	95°C	125°C
XA	Positive	39.5	41.8	42.5	44	45.2
	Negative	36.7	37.5	39.2	40	41.5
XB	Positive	46	48.2	51	51.7	54.7
	Negative	45.5	47.8	49.3	49.5	51.8
XA-4	Positive	52.2	53.3	57	57.2	61.0
	Negative	50.3	52.2	54.5	54.8	58.7
CNT1, CNT2	Positive	32.8	34.3	36.9	38.2	40.1
	Negative	37.7	38.9	41.8	44.0	46.3

TABLE 6-11. TEN-VOLT DYNAMIC POWER INCREASE WITH TEMPERATURE FOR TCS102B PRODUCING BOTH XA AND XB CODES

Temperature (°C)	Dynamic Power (mW/MHz)
25	22.4
50	23.1
75	23.3
95	23.5
125	24.9

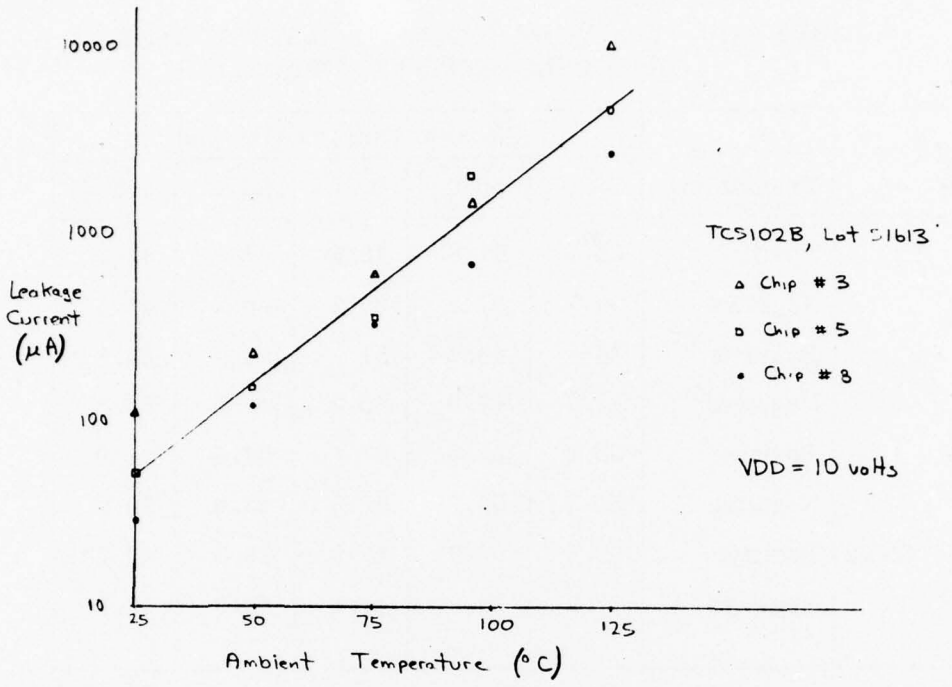


Fig. 6-12. TCS102B leakage current increase with temperatures.

C. RADIATION PERFORMANCE

Code generator arrays from the radiation hardened lot S1855 were subjected to total dose and transient radiation testing at NRL. Additional information on the radiation performance of the TCS102 is provided in the Appendix.

1. Total Dose Testing

The total-dose gamma radiation effects on the code generator array were evaluated by exposing the devices at a dose rate of 10^6 rads(Si) per hour using the NRL cobalt 60 facility. The chips were operated at 100 kHz during the irradiation with the XA, XB and CNT outputs being monitored. At intermediate radiation levels the arrays were removed from the cobalt 60 source and tested for speed and functionality. The functionality test entailed exercising the array through its complete functional test pattern using the NRL-EH-4500 computer-controlled test system. The performance characterization was completed within 30 minutes of removal of the arrays from the cobalt 60 source. This testing was in addition to an immediate functionality test given the part upon removal from the source.

The observed effects of radiation exposure were the reduction in the code generator maximum frequency of operation and an increase in the array leakage current. The reduction in speed as a function of accumulated radiation dose is shown in Fig. 6-13. The decrease in maximum operating speed was

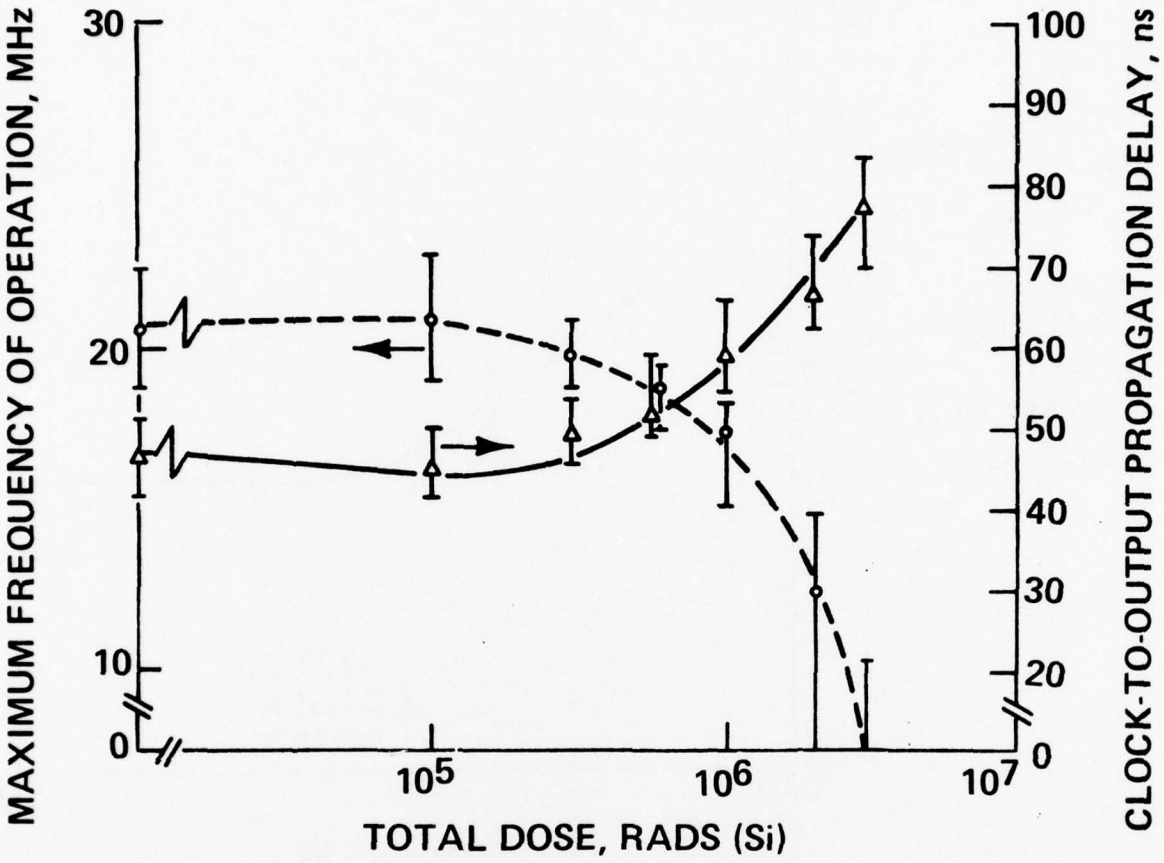


Fig. 6-13. Performance curves for the code generator.

approximately 15% over a megarad as compared with the prediction of 29% from the simulation. Possible explanations for the discrepancy in speed degradation are the lower N and P transistor threshold voltage after radiation, a smaller decrease in device mobility and the less than worst case conditions of dynamic operation during irradiation. Radiation testing of the test transistors on the TCS102 showed an N threshold of 0 volts for a 10 volt bias and a threshold of 2 volts for a 0 volt bias after 10^6 rads. Corresponding thresholds for the P transistor were -2.5 volts for 0 volt bias and -2.2 volts for -10 volt bias. These thresholds are lower than those used in the simulation and, consequently, should yield a higher postradiation speed. Dynamic operation of the array results in the individual transistors being in the worst case bias only part of the time. Hence, parameter shifts are less than the maximum as the effects of the two bias conditions average out. This effect was demonstrated by the one array irradiated with a dc bias which decreased in speed by 27% at a megarad. The clock to output delay showed the same degradation with radiation exposure as the maximum code generator speed.

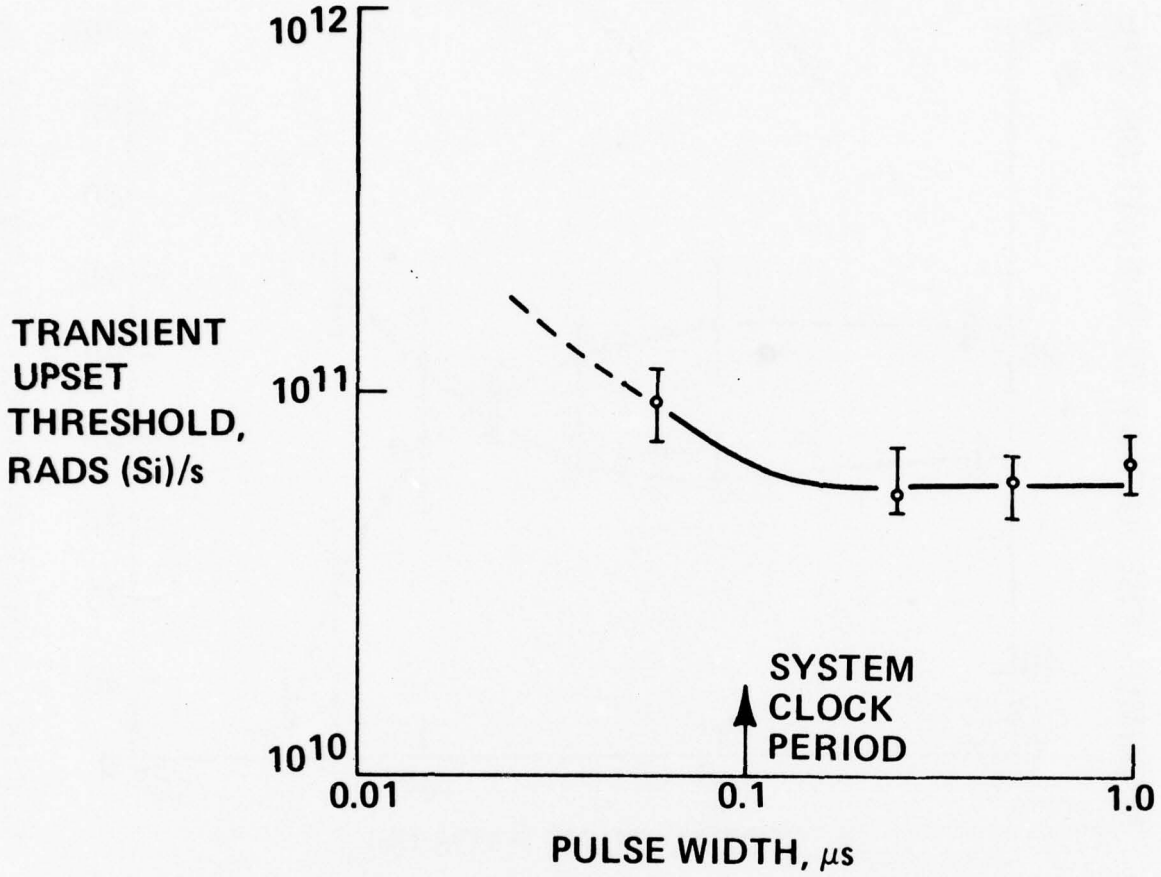


Fig. 6-14. The threshold between acceptable operation and transient upset for the code generator as a function of the irradiation pulse width.

The leakage current for the dynamically operated units increased from 200 to 400 μA before irradiation to 0.5 to 1.4 mA after 10^6 rads (Si). The increase occurred before 10^5 rads(Si) of exposure. This indicates that the N transistors did not go depletion. The one chip tested with a dc bias had leakage current increasing to 19 mA after a megarad, indicating that the N devices may have gone depletion.

All the dynamically operated chips were fully functional at a megarad and exceeded the 10 megabit speed requirement. Some units were tested out to 3×10^6 rads(Si) without functional failure, although speed began to drop off significantly above a megarad. All the units tested at this time came from a single process run (S1855).

2. Transient-Radiation Upset

The transient upset threshold for the code generator was measured at NRL using the 40 MeV LINAC with 50 ns to 1 μs electron pulses. The array was operated at 10 MHz during the transient-radiation test with initial synchronization of the pseudorandom sequence obtained using the SET input. The delay from the SET pulse to the irradiation pulse was about 1 μs. Both of the code outputs and several of the counter states were monitored. Any upset is detected by comparing the actual output with the known correct output following the radiation pulse. Any upset in the array will appear as an error on an output within 24 clock periods (2.4 μs).

The transient upset threshold was measured as a function of irradiation pulse width with the results being given in Fig. 6-14. For 50-ns pulses the transient upset threshold is near 10^{11} rads(Si)/s. For longer pulses the upset threshold is in the 6 to 8×10^{10} rads(Si)/s range. During the longer pulses the array must undergo several clockings with corresponding register state changes during the radiation pulse. These tests show that the code generator meets the 2×10^{10} rads(Si)/s minimum upset level requirement and approaches the 10^{11} rads(Si)/s goal.

Section VII

TEST DEVICES

Six test devices with pads for optional bondout are included on the TCS102 array, namely:

1) Pair of input protection gated diodes
2) Inverter without substrate clamp
3) Inverter with substrate clamp on P transistor
4) Inverter with short channel length (0.2 mil instead of 0.25 mil)
5) NOR gate with P transistor substrate clamp
6) Memory element consisting of half a normal register stage.

The TCS102 is packaged in a 28-pin package and is designated the TCS102X when these six devices are bonded out. These test devices are used to obtain characterization data on individual devices. In particular, the inverters provide a means to determine device threshold shift, leakage current increase, and mobility decrease as a function of radiation exposure. The test devices are described below.

A. INPUT PROTECTION GATED DIODES

The gated diode test device consists of two gated diodes identical in design to the input protection diodes used on each code generator input. Figure 7-1 shows schematically the gated diodes along with the package pin numbers on the TCS102X. The diode D1 is a P+PN+ diode formed by implanting the P+ and N+ regions into the original P island using the polysilicon gate as a shield. Closed-geometry layout is used to obtain a diode free of any edge effects. The PN+ diode junction has a length of 290 μm. The diode D2 is a P+NN+ diode formed in similar fashion beginning with N material. The P+N diode junction has a length of 290 μm. The diode pair is used in the input protection with the anode of D1 connected to ground and the cathode of D2 connected to V_{DD}. The input signal is connected to the common point.

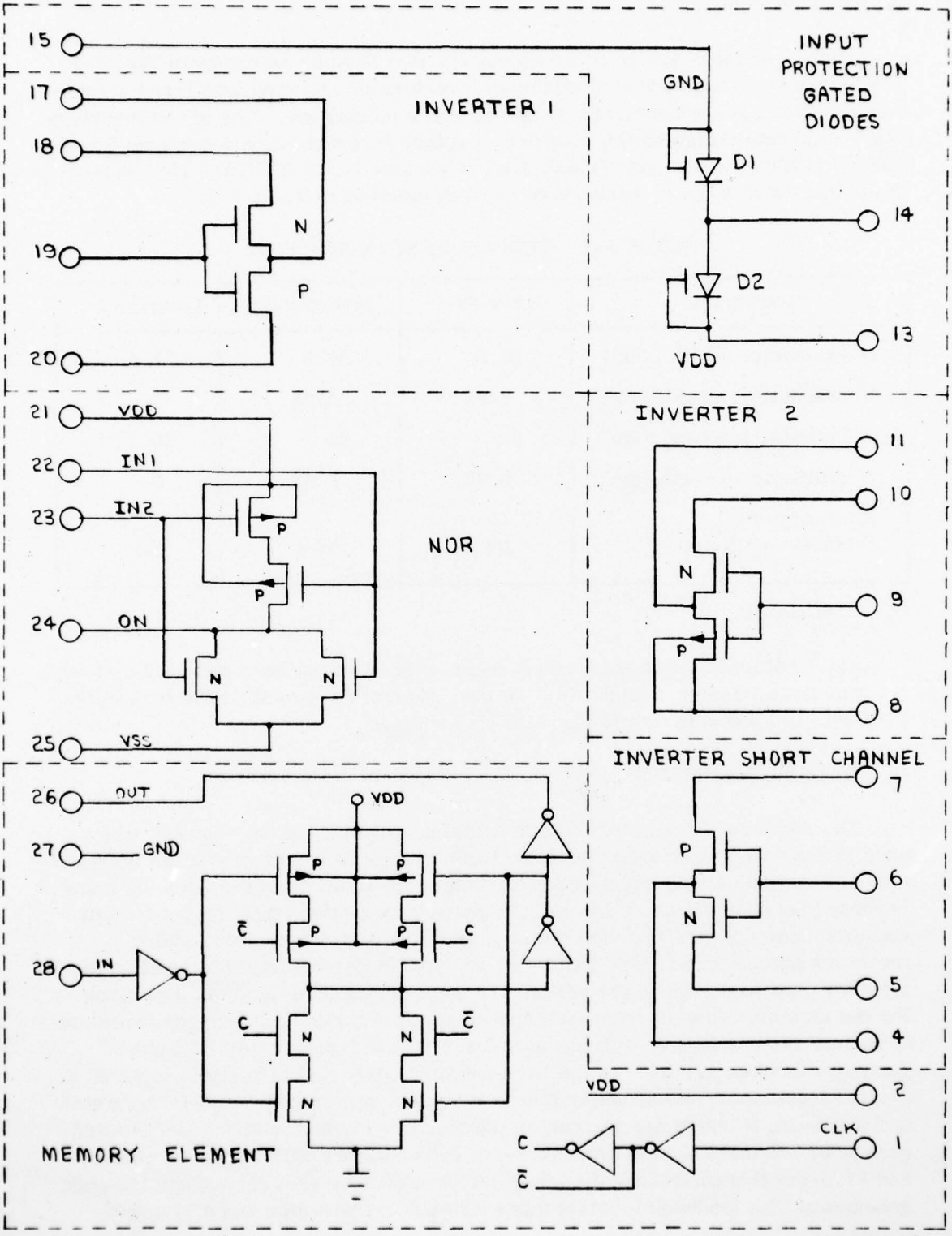


Fig. 7-1. TCS102 test devices.

B. INVERTERS

Three inverters are included among the test devices as shown in Fig. 7-1. These inverters can be tested either as inverters or as individual P and N transistors since each source, drain, and gate are bonded out. One of the inverters has a substrate clamp on the P device. Another inverter has a 5-μm gate length instead of the 6.25-μm gate length used elsewhere on the TCS102. The sizes of the transistors in the test inverters are summarized in Table 7-1.

TABLE 7-1. TCS102X TEST INVERTERS

Parameter	Inverter 1	Inverter 2	Inverter 3
N Transistor Width (μm)	27.5	27.5	27.5
N Transistor Length (μm)	6.25	6.25	5
P Transistor Width (μm)	55	55	55
P Transistor Length (μm)	6.25	6.25	5
Presence of P Substrate Clamp	No	Yes	No

C. NOR GATE

The NOR gate is designed with 250-μm-wide P transistors and 62.5-μm-wide N transistors. The gate length is 6.25 μm. Each of the two P transistors in the NOR has its substrate tied to the NOR V_{DD} voltage.

D. MEMORY ELEMENT

The memory element test device contains half of a typical register stage used in the code generator. The same basic circuit is used for both the master and slave portions of a typical register stage, the polarity of the clocking being reversed between the two portions. To provide maximum isolation between the memory logic and the input and output pins of the test device, four buffer inverters are provided (Fig. 7-1). One of these buffer inverters is used on the memory data input, while two others are used to generate the $\overline{\text{clock}}$ and clock for the memory element from the supplied clock signal. Each of these inverters is formed from a 130-μm P transistor and a 65-μm N transistor. Closed-geometry devices are used in the two inverters connected directly to input pins. A closed-geometry output buffer inverter consisting of a 642.5-μm P transistor and a 345-μm N transistor is used on the memory element output. The clocked gate in the memory element has 52.5-μm P transistors with substrate clamps and 27.5-μm N transistors, the same device widths as used throughout the code generator. The feedback inverter has a 150-μm P transistor and a 75-μm N transistor.

No input protection is provided in the memory element or in any other of the test devices. Consequently, care should be taken to avoid static charge on the input pins, since such charge could damage the gate oxide.

The memory element is specifically designed for testing the effects of a radiation transient on data stored in a memory element. Either a "1" or a "0" may be stored in the memory element, with an upset occurring if the stored bit changes as a result of a transient radiation pulse. Table 7-2 gives the biasing conditions at the time of the radiation pulse for both cases.

The storing of a "0" in the memory element requires the following steps:

1) Make CLK (pin 1) high and IN (pin 28) low. This enters the "0" into the memory element.

2) Return CLK to the low state. This isolates the memory element from further signal changes on the IN input.

3) Return IN to the high state. This creates the situation where the input and stored signal have opposite polarity, thus increasing the probability of upset.

The storing of a "1" in the memory element follows a similar sequence of steps:

1) Make CLK high and IN high.

2) Return CLK to the low state.

3) Return IN to the low state.

Table 7-2. MEMORY ELEMENT BIAS CONDITIONS AT TIME OF RADIATION PULSE

Pin No.	Pin Name	Input/Output	"0" Stored	"1" Stored
1	CLK	Input	0 V	0 V
2	V_{DD}	Input	10 V	10 V
26	OUT	Output	0 V	10 V
27	GND	Input	0 V	0 V
28	IN	Input	10 V	0 V

Section VIII

CONCLUSIONS AND RECOMMENDATIONS

The TCS102B version of the code generator LSI array was successfully fabricated, with all the logic performing as planned. The TCS102B generates the X2 code in the NAVSTAR GPS baseband subsystem. The TCS102A, for which a metal mask was generated, and the TCS102C, for which a metal mask was not generated, are two more LSI arrays in the GPS baseband system. The TCS102 is the first radiation-hardened CMOS/SOS LSI array designed for the NAVSTAR GPS baseband subsystem and, hence, can serve as the first of a family of arrays for performing the P and C/A code generation functions.

The analysis of the code generator array indicated a worst-case speed problem in meeting the 10.23-MHz requirement at a temperature of 125°C after a megarad total dose. However, performance results showed a loss in speed less than the worst-case prediction for both temperature and radiation effects. Two suggested approaches for improving the worst-case speed are:

1) Screen the parts during testing to eliminate slow parts which may not meet the speed requirements.

2) Create a new polysilicon gate mask with a drawn channel length of 5 μm rather than the 6.25 μm used. This will both increase the K factor by about 20 percent and reduce the gate capacitance. Both effects reduce gate delay and, hence, increase circuit speed.

The P-channel substrate clamps used to prevent back bias on the P transistors during irradiation are designed for the double epi process, with separate masks being used to define the N and P islands. An alternate clamping scheme is available for use with a single-epi process if both level 4 (N+) and level 9 (P+) masks are generated. Since this alternative clamping technique requires less layout area and results in lower gate capacitance, it should be considered in the design of future radiation-hardened CMOS/SOS arrays. Both clamping schemes have proved successful in eliminating excessive threshold shifts in the P transistor during irradiation.

Testing of the TCS102B at the NRL cobalt 60 facility showed operation of the code generator at 10^6 rads(Si) with about a 15 percent decrease in speed.

Some arrays were functional at 3×10^6 rads(Si), but at reduced speed. Transient upset tests performed at NRL using a 40-MeV LINAC showed an upset level near 10^{11} rads(Si)/s for a 50-ns pulse and 6 to 8 x 10^{10} rads(Si)/s for a longer 1-μm pulse. This testing demonstrates the megarad hardness and high transient upset level of the TCS102 code generator array. The combination of radiation-hardened design techniques and radiation-hardened processing results in hardened CMOS/SOS LSI arrays capable of operation at 10 to 20 MHz.

Section IX

REFERENCES

1. L. J. Palkuti et al., "Analysis of the radiation response of CMOS circuits," 1974 GOMAC Digest, June 1974, p. 88.

2. R. L. Pryor and A. Feller, Radiation-Hardened CMOS/SOS Standard Cell Circuits, Interim Report, NRL Contract N00014-75-C-0709, January 1977.

3. D. H. Phillips, "Silicon-on-sapphire device photoconduction predictions," IEEE Trans. on Nuclear Science, vol. NS-21, p. 217, December 1974.

   D. H. Phillips, "CMOS/SOS NAND gate sapphire photocurrent compensation," IEEE Trans. on Nuclear Science, vol. NS-22, p. 2617, December 1975.

4. W. F. Heagerty and H. W. Kaiser, Radiation Hardened MOS/SOS Analog-to-Digital Conversion Technology for Phase I, AFAL-TR-78-23, March 1978.

5. S. H. Cohen and G. K. Caswell, "An improved input protection circuit for CMOS/SOS arrays," IEEE Trans. on Electron Devices, vol. ED-25, p. 926, August 1978.

6. L. J. Palkuti, H. W. Kaiser, J. I. Pridgen, and B. J. Wilson, "Ultra-high upset, megarad-hard Si-gate CMOS/SOS code generator," IEEE Trans. on Nuclear Science, vol. NS-25, pp. 1181-1185, December 1978.

AD-A067 980 RCA ADVANCED TECHNOLOGY LABS CAMDEN N J F/6 9/5
RADIATION HARDENED CMOS/SOS CODE GENERATOR FOR SPACE APPLICATIO--ETC(U)
OCT 78 J I PRIDGEN, H W KAISER N00014-75-C-0709

UNCLASSIFIED NL

2 OF 2
AD
A067980

END
DATE
FILMED
6-79
DDC

Appendix

ULTRA-HIGH UPSET, MEGARAD-HARD SI-GATE CMOS/SOS CODE GENERATOR

(Reprinted from IEEE Transactions on Nuclear Science, vol. NS-25, pp. 1181-1186, December 1978)

IEEE Transactions on Nuclear Science, Vol.NS-25, No.6, December 1978

ULTRA-HIGH UPSET, MEGARAD-HARD SI-GATE CMOS/SOS CODE GENERATOR*

L. J. Palkuti, H. W. Kaiser, J. I. Pridgen, and B. J. Wilson

Abstract

A high-speed, radiation-hard code generator LSI array has been developed and fabricated. A unique design approach combined with hard silicon-gate CMOS/ SOS processing has resulted in an ultra-high transient-upset threshold ($\sim 10^{11}$ rads/s for 50 ns pulse width) and megarad total-dose hardness. This paper describes the design as well as characterizes the electrical, radiation and temperature capabilities of this device. Even with modified design and the radiation-hard process, the code generator achieves better than 20 megabit per second operation. The measured 25°C and 125°C clock-to-output propagation delays are 46 and 52 ns respectively prior to radiation exposure. The measured clock-to-output propagation delay after 10^6 rads (si) is 55 ns. These results demonstrate Si-gate CMOS/SOS as a successful radiation-hard LSI technology.

Introduction

The benefits of low-power, high speed and radiation-hardness required for space applications can be realized using Si-gate CMOS/SOS technology in LSI-arrays. Typical LSI candidates requiring these benefits are sequence generators frequently used in spacecraft components for security, jam-resistant, and time keeping applications. As an example, the baseband subsystem from a navigation satellite application is shown in block diagram form in Figure 1. This subsystem produces a 10.23 megabit per second precision (P) navigation code using an atomic frequency standard with the appropriate accuracy. The PX1 and PX2 code generators each produce a one and one-half second long pseudo-random sequence which are then combined, with appropriate relative delay, to form the seven-day long P code. The tap register varies the delay of the X2 sequence enabling one of thirty-two unique sequences to be formed. The Z counter is advanced every 1.5 seconds with a count of 403,200 required for a complete week. Monitoring, control and initialization of the sequence is provided through the phase adjustment logic subject to externally provided control signals. This paper discusses a mask programmable radiation-hard code generator, designated the TCS102, that generates the pseudorandom sequences in the precision navigation baseband subsystem.

Array Description

There are three basic functional elements on the TCS102 array. The first two elements, designated the X_A and X_B code generators, are twelve-stage pseudo-random sequence generators. Each sequence generator consists of twelve master-slave register stages with the output of the final stage being fed back to exclusive-OR gates located between selected successive register stages. The specific sequence generated is selected by using a metal mask option to locate the feedback taps. The third element of the array is a twelve-stage synchronous counter. In addition, control and clock logic associated with each of these elements is included on the array. The TCS102 is 5.13 by 4.80 mm (202 mil x 189 mil) in size and contains a total of 2660 transistors. A photomicrograph of the TCS102B (the specific metal mask option described in this paper) is shown in Figure 2. Test devices designed to aid device characterization and lot-sampling tests are included along the chip periphery.

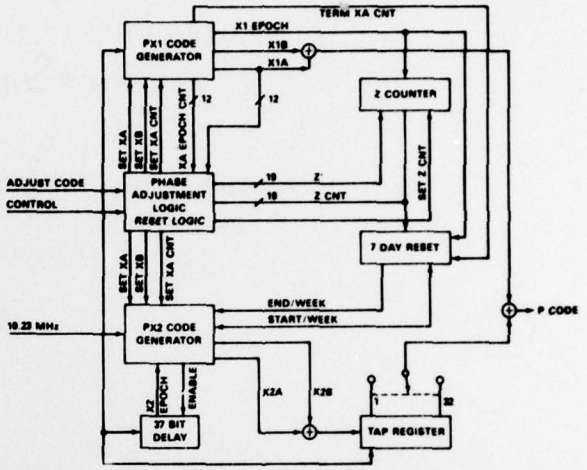


Figure 1. A block diagram of a precision navigation baseband subsystem.

The X_A code generator portion of the TCS102 array consists of a twelve-stage pseudorandom sequence generator, a twelve-stage serial shift register, state-decode logic and clock-control logic (Figure 2). The pseudorandom sequence produced by the programmable sequence generator is clocked through the twelve-stage serial register. Buffered array outputs are taken at twelve successive stages of the sequence generator and serial register as well as at the final register output to provide sequence outputs shifted in time. The state-decode logic gives an epoch output whenever the sequence generator reaches a preprogrammed state. The clock-control logic is used to halt or resume X_A sequence generation depending on control inputs to the array. The X_A sequence can be externally initialized by the SET input pulse. Specifically, the X_A code for the TCS102B is generated by the polynomial $X^{12} + X^{11} + X^{10} + X^9 + X^8 + X^7 + X^5 + X^4 + X^3 + X + 1$. The sequence length is shortened to 4092 bits from the natural 4095 bits by resetting the sequence generator with the epoch signal. The generation of the X_B code is similar to that of the X_A code.

The synchronous counter on the TCS102 generates 1.5 second timing pulse (if operated at a 10.23 MHz clock rate) by counting the epoch pulses of the X_A code generator. Unlike a ripple counter where the carry propagates from the last to most significant stage when clocked, all stages of the TCS102 counter will change state simultaneously when clocked. In this manner, a valid count is maintained at all times in a synchronous system operating in the 10-20 MHz range. Although designed to count the epoch pulses generated by the X_A code generator, the connection of the X_A epoch to the counter input is external to the chip. This allows independent operation of the X_A code generator and the counter and facilitates testing of the array.

Palkuti and Wilson are with the Naval Research Laboratory, Washington, D.C. 20375; Kaiser and Pridgen are with RCA Corp., Camden, N.J. 08102.

*Work was supported by DNA under Subtask TD033.

U.S. government work not protected by U.S. copyright.

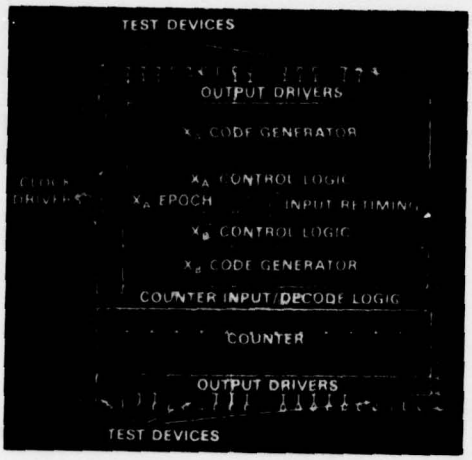


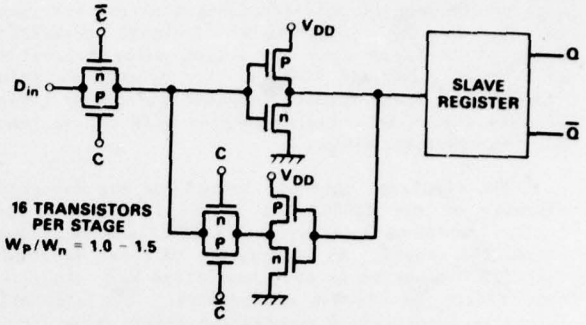
Figure 2. Photomicrograph of TCS102B code generator showing the functional elements of the custom array.

Array Design and Simulation

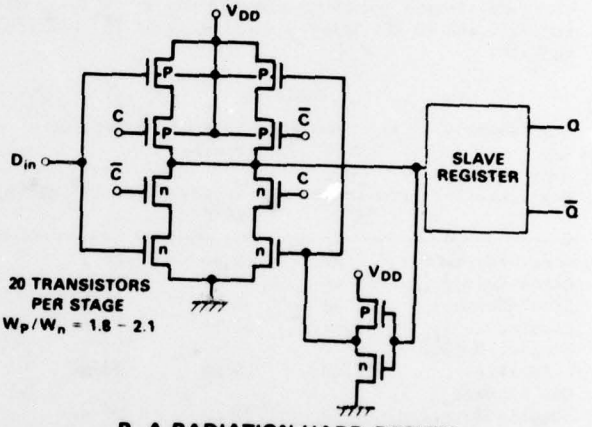
A handcrafted-custom approach rather than the standard-cell approach[1] was used to design the TCS102 array because the logic in the array is inherently repetitive rather than random, and because a mask programmable feature was desired. In addition, the custom approach allows the most freedom to optimize both electrical performance and radiation hardness. The design procedure that was followed entailed optimizing logic and circuit design to assure a high level of tolerance to transient-radiation induced circuit upset, while minimizing the effect on circuit performance of the expected total-dose induced parameter changes.[2] Consideration was given to total-dose induced threshold voltage changes (including transient annealing effects), mobility degradation, increases in subthreshold leakage of n-channel transistors and minimizing the irradiation-bias dependence of transistor parameter changes. For LSI arrays, it is most important to minimize this irradiation-bias dependence to make meaningful irradiation testing and simulations possible. Reasonable simulation and experiments, to date, make predictions of the worst-case bias condition virtually impossible.

Specific design rules included (1) elimination of circuit options that were more sensitive to upset than a 3-input NAND, (2) the bodies of stacked p-channel transistors were clamped to the positive power supply, (3) transmission gates were not used, (4) stacked transistors of the same polarity were limited to three and (5) the p-channel transistor widths in inverters were increased from a typical W_p/W_n ratio of 1.5 to about 2.0.

As an example, a standard-design master-slave static register stage, shown in Figure 3A, is contrasted with a radiation-hard register stage, Figure 3B, where some of the above rules were incorporated. The standard-design register is sensitive to radiation induced n-channel currents in the transmission gate, TG, (next to the D_{in} terminal) when this TG is in the OFF state. If D_{in} is changed to a logic "1" after a logic "0" is entered into the master, leakage through the transmission gate will tend to cause D_{in} to fall below the logic "1" level and the signal on the master inverter to rise above the logic "0" level. This effect, when coupled with the reduced noise immunity from radiation-induced parameter shifts, can eventually lead to failure in either the register or the D_{in} driving source. In contrast, the radiation-hard register stage uses no transmission gates and provides isolation between the D_{in} signal and the stored data.



A. STANDARD DESIGN



B. A RADIATION-HARD DESIGN

Figure 3. A comparison between the standard and a modified design for the register stages.

Extensive transient analysis using the R-CAP[3] computer simulation program was utilized to obtain an optimum design. These simulations were used to evaluate array speed capability, temperature performance and radiation sensitivity. Both total-dose and transient radiation performance was investigated. Model parameters utilized in the simulations are listed in Table I.

TABLE I

Transistor Parameters Used in Simulations

Parameter	N OV Bias	N +10V Bias	P OV Bias	P -10V Bias
V_T (pre) [V]	1.5		-1.5	
K' (pre) [$\mu A/V^2$]	5.0		3.35	
V_T (10^6rad) [V]	2.5	0.5	-3.5	-2.5
K'/K'_0 (10^6rad)	0.95	0.70	0.85	0.92

To study the effect on circuit performance of the bias conditions during irradiation, the propagation delay of the register stage followed by an output driver was determined by computer simulations using each of the sets of post-irradiation parameters given in Table I. The results showed a signal propagation delay of 54-57 ns when the output makes a positive going transition and 40-43 ns for a negative going transition. These results indicate the insensitivity of this design to irradiation-bias effects, at least for the speed parameter.

The simulated internal delays for the important elements of the TCS102 are listed in Table II for typical, worst-case temperature (125°C) and total-dose irradiation cases. An examination of these data show that 125°C temperature and irradiation have about the same effect on circuit performance. The simulated values also indicate a significant design margin from the maximum 100 ns delay allowable at 10 MHz operation. The predictions of maximum code generator speed using worst-case parameters are 18 MHz at 25°C, 13 MHz at 125°C and 13 MHz after a total-dose of 10^6 rad (Si) at 25°C.

Table II

Summary of the Simulated Internal Delays of TCS102 Sub-circuits

Sub-circuit	Pre-irrad. 25°C	Pre-irrad. 125°C	After 10^6 rad(Si)
Code Generator	17 ns	25 ns	26 ns
Clock Driver	13 ns	17 ns	16 ns
Clock Control	25 ns	35 ns	34 ns
Counter Logic	49 ns	67 ns	61 ns
Counter Output Register	17 ns	24 ns	23 ns
Out Drivers (Double inverter)	17 ns	24 ns	22 ns

Critical circuits such as the register stage were analyzed to study their transient-upset behavior. Sapphire photoconduction was assumed to dominate the transient response and a conductivity factor of 1×10^{-15} mho (mil-rad/s) based on test device performance[4] was assumed. A typical simulation result from the transient-upset analysis is shown in Figure 4. These data show that proper circuit operation is maintained at the simulation level with about a 25 percent degradation in the output level during the irradiation pulse. The simulations predicted 5- and 7-volt logic levels at 10^{11} rad/s indicating the proximity to upset. Although the exact upset levels are not necessarily predicted due to uncertainties in input parameters, these results are useful in uncovering circuits particularly susceptible to upset.

Array Processing

The circuits were processed using a radiation-hard, self-aligned, Si-gate CMOS/SOS process.[7] The n- and p-transistor islands were separately ion implanted, i.e., a single-epitaxial, full enhancement process. The gate oxide was a 925°C pyrogenic oxide that was annealed in oxygen and nitrogen at the same temperature. The gate-oxide thicknesses ranged from 700 to 850 Å. The P^+ polysilicon gates are boron doped during deposition. The sources and drains are separately ion-implanted (an addition mask is used to shield P^+ areas during phosphorous implantation) and the dopants are activated at 850°C. RF heated Al metalisation is used. A low-temperature glassivation overcoat completes the passivation.

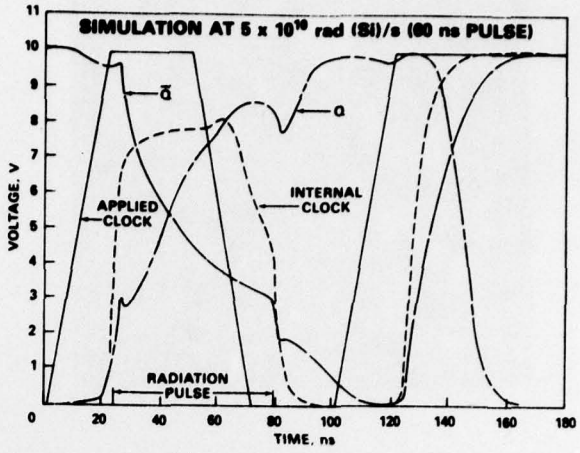


Figure 4. Simulated performance of the register circuit to a transient radiation pulse.

The array design rules allowed 0.25 mil polysilicon gate lengths and 0.4 mil minimum metal linewidth with 0.3 mil minimum spacing. Other design and layout rules are outlined in reference 6. Array input protection is provided by a closed-geometry gated diode, resistor and arc-gap that is compatible with the radiation-hard process.[7]

TABLE III

Transistor Parameters Measured on TCS102B Test Devices

	N OV Bias	N +10V Bias	P OV Bias	P -10V Bias	P +10V Bias
V_T (pre), [V]	2.0			-1.0	
K' (pre), [$\mu A/V^2$]	6.0			3.7	
V_T (10^6rad), [V]	2.0	0.0	-2.5	-2.2	-6.5
K'/K'_0	0.95	0.65	0.90	0.95	0.70

Test transistors on the TCS102 array were used to evaluate the performance of the radiation-hard process. These devices were exposed to cobalt 60 irradiation at various bias conditions. The transistor parameters before and after 10^6 rad (Si) are listed in Table III. These measured parameters are similar to the parameters used in the simulations except perhaps a slightly larger threshold voltage shift for the n-channel transistors. The large change in the p-transistor threshold observed under positive bias indicates the need for substrate clamps. Radiation-induced back-channel leakage of about 1 μA/mil was observed on some wafers and less than 0.01 μA/mil was observed on other wafers. All n-transistors exhibited some degree of edge-transistor leakage that was especially pronounced during positive irradiation bias.

Electrical Evaluation

TCS102 arrays were evaluated from both radiation-hard process and conventional process lots. Functional performance for the arrays was obtained from 3.5 to 10 volts for the hard process and 2.5 to 10 volts for the standard process. Higher voltage operation is possible but was not attempted. Measurements

of maximum array speed were performed by monitoring the X_A and X_B code outputs as the frequency was increased. Maximum frequency of operation as a function of operating voltage is shown in Figure 5 for typical arrays. For the radiation-hard process, the maximum operating frequency ranged from 18-26 MHz and 8-12 MHz for 10 and 5 volt operation, respectively. For the standard process, the maximum frequency range was 27 to 28 MHz at 10 volt operation. These data indicate that a modest (10 to 20%) performance reduction can be expected between the standard and radiation-hard processes. Note that the maximum operating frequency is an internal parameter and hence is independent of output loading. The simulations predicted a maximum operating frequency that was lower than generally observed (Figure 5). These results are expected, since the simulations used worst-case assumptions. In addition, the transistor mobilities assumed in the simulations were generally lower than experimentally observed.

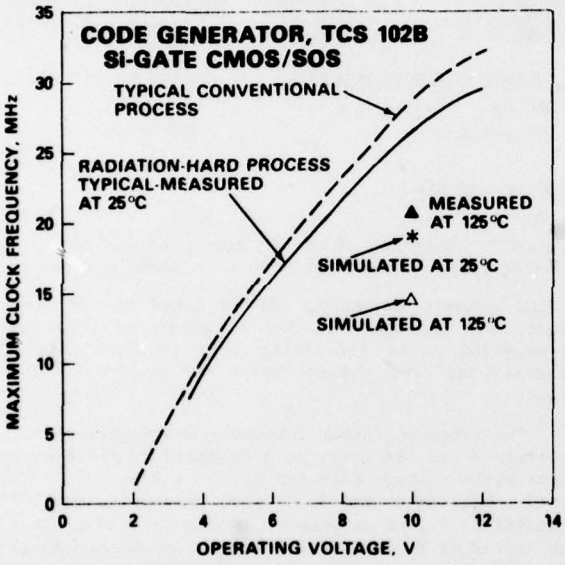


Figure 5. Performance of the code generator array as a function of operating voltage.

Measured signal propagation delays ranged between 45 and 50 ns (at 10V) for the clock input to code output path. Again, these values were slightly lower than the simulated values. The devices fabricated by the standard process had clock-to-output delays ranging from 37 to 43 ns. Propagation delays of 56 to 77 ns were measured for these arrays at 5 volts. Measurements made on the input clock requirements indicated considerable tolerance of the array to variations in clock duty cycle. Measurement of propagation delays as a function of output loading were made. The slope of this characteristic was measured as 0.2 ns per pF up to 60 pF.

Standby or leakage currents for the arrays were found to vary from array to array. The distribution of maximum leakage currents peaked near 200 μA (10 volt) for the devices fabricated by the radiation-hard process. The lot produced by the conventional process had lower (~ 80 μA) average leakage. The 10 volt dynamic power was found to depend linearly on frequency at 22 mW/MHz.

Measurement of array performance over temperature showed that the maximum speed of the arrays was reduced by about 15-20 percent from the room temperature speed at 125°C. The simulation predicted a larger decrease in speed (about 30 percent) than the decrease experimentally observed (see Figure 5). Standby current increased by a factor of 100 over the room temperature values at 125°C. The dynamic power of the arrays increased to 250 mW (10 V and 10 MHz) at 125°C as compared with 220 mW at room temperature.

Total-Dose Effects

Ionizing total-dose effects on the code generator were evaluated by exposing the devices at the NRL cobalt 60 facility at a dose rate of 10^6 rad (Si) per hour. Since in the actual applications the code is continually generated without interruption, the arrays were clocked at 100 KHz during radiation exposure. A portable measurement box was used so that a limited functional test, the maximum frequency of operation and the standby current could be measured immediately after the removal of the devices from the irradiation source. The NRL-EH-4500 computer-controlled test system was then utilized to completely characterize the arrays including a full functional test and measurement of propagation delays at all outputs. In all cases, the arrays were completely characterized within 30 minutes after irradiation. Correlations between the EH 4500 tester and the portable test box indicated negligible annealing in all parameters except the array leakage. Typically, about 20 percent annealing in the standby current was observed during the measurement intervals.

The effect of total-dose irradiation on the TCS-102 array is primarily a reduction in the maximum frequency of operation and an increase in the standby current. The reduction in array performance as a function of irradiation dose is shown in Figure 6. The decrease in maximum operating frequency and increase in propagation delay was about 15 percent after 10^6 rad (Si). The simulated results, similar to those obtained for the temperature sensitivity, predicted more degradation than was observed. These data show that significant margin is available at 10 MHz at 10^6 rad (Si). Initial failures in some arrays were observed at 2×10^6 rad (Si). Some arrays were functional after an irradiation dose of 3×10^6 rad (Si). The leakage current increased from 100-500 μA before irradiation to about 1 mA at 10^6 rad (Si) as shown in Figure 7. The increase in leakage resulted primarily from island-edge-effects and to a lesser extent to back-channel leakage because similar increases in radiation-induced leakage current were observed for arrays taken from wafers where the test transistors showed no back-channel leakage.

Transient-Radiation Upset

The transient upset threshold for the array was measured using the 40 MeV LINAC with 50 ns to 1 μs electron pulses. Dosimetry was performed for each pulse by 4-1/8 inch TLD dosimeters. The electron pulse shape of the LINAC was monitored using a PIN diode. The array was operated at the nominal 10 MHz clock rate with the radiation pulse synchronized to the SET pulse (start of code generators). The delay between the irradiation pulse and the SET pulse was usually adjusted to about 1 μs. Several counter outputs were monitored during and after the irradiation pulse on dual-beam oscilloscopes. Since the SET pulse started the array in a known state, observation of the code generator outputs for only a limited number (about 25) of clock cycles was needed to determine if an upset in any internal register occurred.

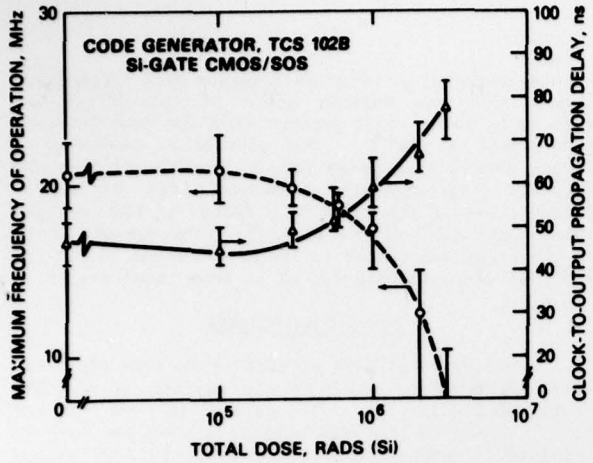


Figure 6. Performance curves for the code generator. The irradiations were conducted in a cobalt 60 source at a dose rate of 10^6 rad (Si) per hour. The effect of total dose on maximum frequency is given by the dashed curve while the solid line shows the total dose effects on the propagation delay. Output loading for both propagation delay and maximum frequency measurements was between 20-25 pF.

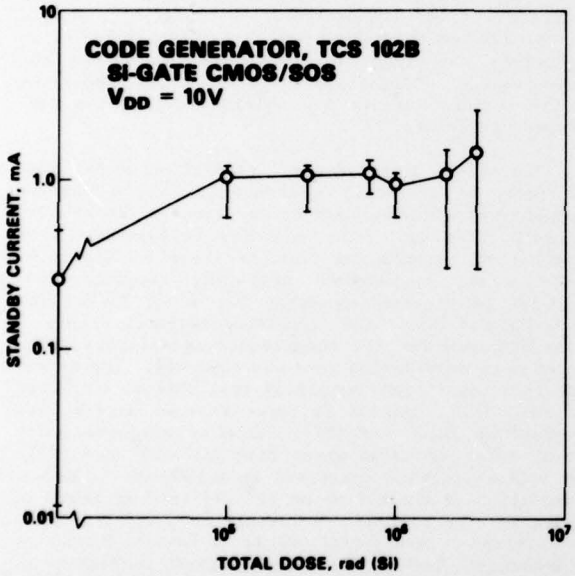


Figure 7. The irradiation induced leakage current as a function of the irradiation dose. The error bars indicate both the variation with the condition of measurement and variability among the devices tested.

To illustrate the transient behavior of the code generator, actual output data near the upset threshold is shown in Figure 8. The center trace shows the proper X_A-code output after the application of the set pulse. The top trace shows the X_A output during and after a 1 μs irradiation pulse. By comparing the top and center traces, it is clear that the proper X_A code is maintained during and after the irradiation pulse. The modification to the logic levels during the radiation pulse is in agreement with the simulations. It should be noted that the proper code output was maintained during irradiation even though the array power supply current increased to 200 mA (10 times the

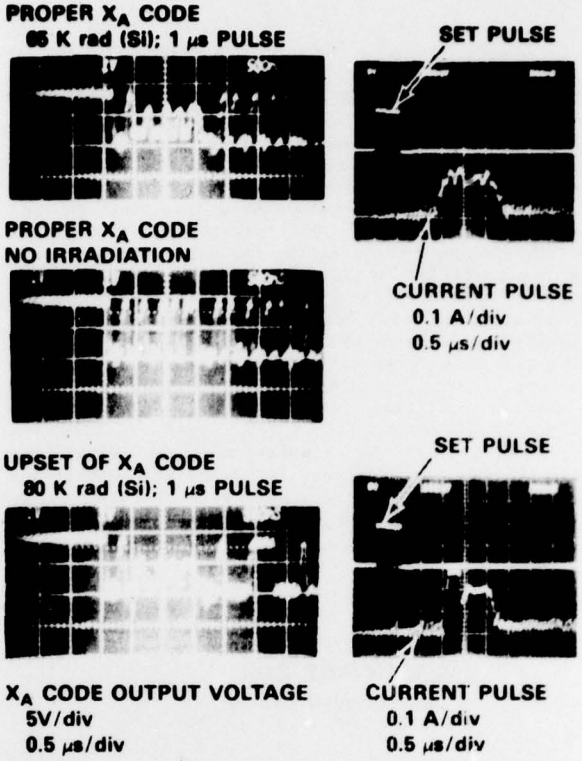


Figure 8. Response of the X_A output of the code generator when irradiated with 1 s LINAC pulses.

normal dynamic current). As is noted on the lower trace, the improper X_A code is generated after the irradiation pulse indicating that in this case an internal register changed state during the irradiation.

The transient error threshold was experimentally determined for the array as a function of irradiation-pulse width. These data are given in Figure 9. The array exhibited a transient-upset threshold near 10^{11} rads (Si)/s for 50 ns pulses. The error bars indicate the spread of four different samples tested. A slight decrease in upset threshold for longer pulses was observed due to the variation of dynamic noise immunity with pulse width.[2] Proper circuit operation was verified in these tests by irradiating the device with different input commands to verify that proper logic operation was maintained. No upset was observed from large threshold shifts (maximum dose 8×10^4 rads in 1 μs).

Conclusions

It has been demonstrated that the Si-gate CMOS/SOS technology can be used to fabricate high-performance radiation-hard large-scale integrated circuits. The performance achieved by the TCS102 code generator is summarized in Table IV. These results were achieved by combining modified designs and processes. It was demonstrated that to achieve the full potential of the radiation-hard CMOS/SOS process, care must be exercised in the design not to compromise either the transient or total dose hardness. In addition, the design procedures outlined also eliminate significant irradiation-bias dependent differences in the radiation response. The approach is, therefore, useful in

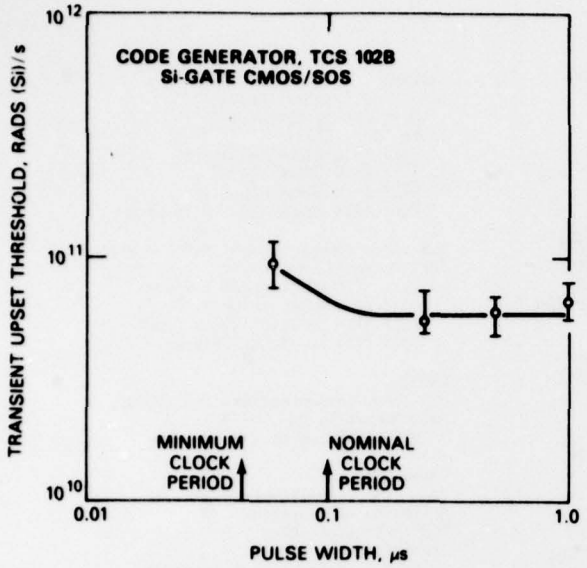


Figure 9. The threshold between acceptable operation and transient upset for the code generator as a function of the irradiation pulse width. These data were taken with the code generator operating at the nominal (10 MHz) clock rate during irradiation.

establishing reasonable irradiation-test procedures for the qualification of radiation-hard circuits. The approaches outlined can lead to custom LSI devices with near nominal performance after 10^6 rad(Si) and achieve error-free operation in excess of 5×10^{10} rad (Si)/s. These arrays can be fabricated without significant compromise to both circuit density and performance.

Acknowledgements

The authors would like to thank G. P. Nelson for providing the EH-4500 tester propagation-delay program, and R. Hevey for contributions to irradiation testing. The work of J. J. Fabula in device processing is also acknowledged.

References

1. A. Feller, S. Ozga and T. Lombardi, CAD VLSI Design Techniques and Microprocessor Application, ISSCC Digest of Technical Papers, pp. 212-213 (Feb 1978).
2. L.J. Palkuti and R. Pryor, "Radiation-Hard Standard Cell Circuits," IEEE Trans. on NS-23, pp. 1715-1719, Dec. 1976.
3. C.B. Davis and M.I. Payne, "The R-CAP Program - An Integrated Circuit Simulator," RCA Engineer, June 1975.
4. D.H. Phillips, "SOS Device Photoconductivity Prediction," IEEE Trans. on NS-22, Dec 1975; also, W. Heagerty, private communication.
5. J.J. Fabula, D.S. Woo, and S.G. Policastro, "Radiation tolerant Si-Gate CMOS/SOS Processing," SOS Workshop, Vail, Col., Sept. 1977.
6. "Manufacturing Methods for Silicon Devices on Insulating Substrate," AFML Report AFML-Report AFML-IR-516-3(2), Jan. 1974.
7. S. Cohen, G. Caswell, "Improved Input Protection Circuit CMOS/SOS Arrays," IEEE Trans on ED, Sept. 1978.

TABLE IV

Summary of Typical Characteristics of the Code Generator

Technology	P^+ Si-gate, CMOS/SOS radiation-hard process
Die size	4.83 x 5.13 mm (190 x 202 mils)
Devices	2660
Maximum clock rate	25 MHz @ 10 volts
Active current	20 mA @ 10 MHz
Standby current	0.3 mA @ 10 volts
Radiation parameters transient upset	$0.8\text{-}1.0 \times 10^{11}$ Rad (Si)/s (50 ns) $6\text{-}8 \times 10^{10}$ Rad (Si)/s (1 μs)
Total dose	10^6 Rad (Si)

Assistant to the Secretary of Defense
Atomic Energy
Washington, DC 20301
01CY ATTN Executive Assistant

Defense Communication Engineer Center
1860 Wiehle Avenue
Reston, VA 22090
01CY ATTN Code R720 C Stansberry
01CY ATTN Code R410

Defense Documentation Center
Cameron Station
Alexandria, VA 22314
12CY ATTN DD

Commander
Defense Electronic Supply Center
1507 Wilmington Pike
Dayton, OH 45401
(Thru DSA for CNWDI)
01CY ATTN DESC-ECS

Director
Defense Intelligence Agency
Washington, DC 20301
01CY ATTN DB-4C
01CY ATTN DT-1B

Director
Defense Nuclear Agency
Washington, DC 20305
03CY ATTN TITL
01CY ATTN RAEV
01CY ATTN TISI Archives

Commander
Field Command
Defense Nuclear Agency
Kirtland AFB, NM 87115
01CY ATTN FCPR

Joint Chiefs of Staff
Washington, DC 20301
01CY ATTN J-3 WWMCCS Evaluation Office

Chief
Livermore Division Fld Command DNA
Department of Defense
Lawrence Livermore Laboratory
P.O. Box 808
Livermore, CA 94550
01CY ATTN FCPRL

Commander
U.S. Army Nuclear & Chemical Agency
7500 Backlick Road
Building 2073
Springfield, VA 22150
01CY ATTN Library

Commander
U.S. Army Test and Evaluation Comd.
Aberdeen Proving Ground, MD 21005
01CY ATTN DRSTE-EL
01CY ATTN DRSTE-FA

Director
U.S. Army TRADOC Systems Analysis Act.
White Sands Missile Range, NM 88002
01CY ATTN ATAA-TFC O Miller

Commander
U.S. Army Training and Doctrine Comd.
Fort Monroe, VA 23651
01CY ATTN ATORI-OP-SW

National Communications System
Office of the Manager
Department of Defense
Washington, DC 20305
01CY ATTN NCS-TS C Bodson

Director
National Security Agency
Department of Defense
Fort George G. Meade, MD 20755
01CY ATTN R-52 O Van Gunten

Under Secy of Def for Rsch & Engrg
Department of Defense
Washington, DC 20301
01CY ATTN Strategic & Space Space Systems (OS)
01CY ATTN AE

Director
BMD Advanced Technology Center
Huntsville Office
Department of the Army
P.O. Box 1500
Huntsville, AL 35807
01CY ATTN ATC-O F Hoke
01CY ATTN ATC-T

Commander
Fort Huachuca
Department of the Army
Fort Huachuca, AZ 85613
01CY ATTN Tech. Ref. Div.

Commander
Harry Diamond Laboratories
Department of the Army
2800 Powder Mill Road
Adelphi, MD 20783
(CNWDI-Inner Envelope:
ATTN: DEFLHD-RBH)
01CY ATTN DELHD-N-RBG
01CY ATTN DELHD-N-RBA J Rosado
01CY ATTN DELHD-N-NP
01CY ATTN DELHD-N-EMA J Miletta
01CY ATTN J Thompkins
01CY ATTN DELHD-N-RBH J McGarrity
01CY ATTN DELHD-N-EM Chief Lab 1000

Commander
Redstone Scientific Information Ctr.
U.S. Army R&D Command
Redstone Arsenal, AL 35809
01CY ATTN DRDMI-TBD

Project Manager
XM-1 Tank System
Department of the Army
28150 Dequindre
Warren, MI 48092
01CY ATTN DRCPM-GCM-SW

Commander
Naval Air Systems Command
Washington, DC 21360
01CY ATTN Air 5324K
01CY ATTN Air 350F
01CY ATTN Air 310

Commanding Officer
Naval Avionics Facility
21st and Arlington Avenue
Indianapolis, IN 46218
01CY ATTN Branch 942 D Repass

Command
U.S. Army Armament Research & Development Command
Dover, NJ 07801
01CY ATTN DRDAR-TSS No. 59
01CY ATTN DRDAR-LCA-PO
01CY ATTN DRDAR-LCN-F
01CY ATTN DRDAR-TSI-E A Grinoch

U.S. Army Communications R&D Command
Fort Monmouth, NJ 07703
01CY ATTN DRSEL-NL-RO R Brown
01CY ATTN DRSEL-TL-MD MR Gaule
01CY ATTN DRSEL-CT-HDK A Cohen
01CY ATTN DELET-IR E Hunter

Chief
U.S. Army Communications Sys. Agency
Fort Monmouth, NJ 07703
01CY ATTN COM-RD-T

Commander
U.S. Army Intelligence & Sec CMD
Arlington Hall Station
4000 Arlington Blvd.
Arlington, VA 22212
01CY ATTN IARDA-OS R Burkhardt

Commander
U.S. Army Material & Mechanics Rsch Ctr
Watertown, MA 02172
(Address CNWDI: ATTN: Document Control for:)
01CY ATTN DRXMR-HH J Dignam

Commander
U.S. Army Missile Material Readiness Cmd
Redstone Arsenal, AL 35809
01CY ATTN Hawk Project Officer DRCPM-HAER

Commander
U.S. Army Missile R&D Command
Redstone Arsenal, AL 35809
01CY ATTN DRCPM-PE-EA W Wagner

Commander
U.S. Army Mobility Equip. R&D Cmd
Fort Belvoir, VA 22060
(CNWDI to Army Mat Dev & Readiness Command)
01CY ATTN DRDME-E J Bond Jr.

Commander
U.S. Army Night Vision Laboratory
Fort Belvoir, VA 22060
01CY ATTN DRSEL-NV-SD J Carter
01CY ATTN DRSEL-NV-SD A Parker

Commander
Naval Electronic Systems Command
Washington, DC 30260
01CY ATTN PME 117-21
01CY ATTN Code 50451
01CY ATTN Navelex 51024 C Watkins

Commanding Officer
Naval Intelligence Support Ctr.
4301 Suitland Road, Bldg. 5
Washington, DC 20390
01CY ATTN NISC Library

Commander
Naval Ocean Systems Center
San Diego, CA 92152
01CY ATTN Code 4471 (Tech Lib)

Superintendent (Code 1424)
Naval Postgraduate School
Monterey, CA 93940
01CY ATTN Code 0142 Library

Director
Naval Research Laboratory
Washington, DC 20375
01CY ATTN Code 5210 J Davey
01CY ATTN Code 4104
30CY ATTN Code 5216 L Palkuti
01CY ATTN Code 6624 J Ritter
01CY ATTN Code 2627
01CY ATTN Code 6601 E Wolicki

Commander
Naval Ship Engineering Center
Washington, DC 20362
01CY ATTN Code 617402

Officer-in-Charge
Naval Surface Weapons Center
White Oak, Silver Spring, MD 20910
01CY ATTN Code F30 130-108
01CY ATTN Code F31

Commander
Naval Surface Weapons Center
Dahlgren Laboratory
Dahlgren, VA 22448
01CY ATTN DG-50 W Holt

Commanding Officer
Naval Weapons Evaluation Facility
Kirtland Air Force Base
Albuquerque, NM 87117
01CY ATTN Code AT-6

Commanding Officer
Nuclear Weapons TNG Center Pacific
Department of the Navy
Naval Air Station, North Island
San Diego, CA 92135
01CY ATTN Code 32

Director
Strategic Systems Project Office
Department of the Navy
Washington, DC 20376
01CY ATTN NSP-230 D Gold
01CY ATTN NSP-2701 J Pitsenberger
01CY ATTN NSP-27334 B Hahn

Commander
Aeronautical Systems Division, AFSC
Wright-Patterson AFB, OH 45433
01CY ATTN ASD-YH-EX Mr. Sunkes
01CY ATTN ENACC R Fish
01CY ATTN ASD/ENESS P Marth

Air Force Avionics Laboratory
Wright-Patterson AFB, OH 43433
01CY ATTN POE-2 J Wise

Air Force Avionics Laboratory
Wright-Patterson AFB, OH 45433
01CY ATTN DHE-2
01CY ATTN DH LTC McKenzie

Air Force Materials Laboratory
Wright-Patterson AFB, OH 45433
01CY ATTN LTE

Headquarters
Air Force Systems Command
Andrews AFB
Washington, DC 20334
01CY ATTN DLCA

Air Force Technical Applications Center
Patrick AFB, FL 32925
01CY ATTN TFS M Schneider

Air Force Weapons Laboratory
Kirtland AFB, NM 87117
01CY ATTN ELP TREE SECTION
01CY ATTN R Maier
01CY ATTN EL C Baum
01CY ATTN SUL
01CY ATTN J Mullis

Commander
BMD Systems Command
Department of the Army
P.O. Box 1500
Huntsville, AL 35807
01CY ATTN BMDSC-HEN

Commander
Naval Sea Systems Command
Washington, DC 20362
01CY ATTN SEA-04531

Headquarters
Electronic Systems Division/IN
Department of the Air Force
Hanscom AFB, MA 01731
01CY ATTN INDC/21

Headquarters
Electronic Systems Division, AFSC
Hanscom AFB, MA 01731
01CY ATTN DRI E Doherty

Commander
Foreign Technology Division, AFSC
Wright-Patterson AFB, OH 45433
01CY ATTN ETDP B Ballard

Commander
Rome Air Development Center, AFSC
Griffiss AFB, NY 13441
(Desires No CNWDI)
01CY ATTN RADC/RBRP C Lane
01CY ATTN RBRAC I Krulac

Commander
Rome Air Development Center, AFSC
Hanscom AFB, MA 01731
01CY ATTN ESE A Kahan

Space & Missile Systems Organization/MN
Air Force Systems Command
Norton AFB, CA 92409
(Minuteman)
01CY ATTN MNNG
01CY ATTN MNNH

Space & Missile Systems Organization/RS
Air Force Systems Command
Post Office Box 92960
Worldway Postal Center
Los Angeles, CA 90009
(Reentry Systems)
01CY ATTN RSMG Capt. Collier
01CY ATTN RSMA Lt. D Higgins

Space & Missile Systems Organization/SK
Air Force Systems Command
Post Office Box 92960
Worldway Postal Center
Los Angeles, CA 90009
(Space Comm Systems)
01CY ATTN SKF P Stadler

Space & Missile System Organization/YA
Air Force Systems Command
Post Office Box 92960
Worldway Postal Center
Los Angeles, CA 90009
01CY ATTN YAS

Strategic Air Command/XPES
Offutt AFB, NB 68113
01CY ATTN XPES M Carra
01CY ATTN NRI-STINFO Library

Director (INWS)
3416th Technical Training Squadron (ATC)
Air Training Command
Department of the Air Force
Kirtland AFB, NM 87115
01CY ATTN TTV

Department of Energy
Albuquerque Operations Office
P.O. Box 5400
Albuquerque, NM 87115
01CY ATTN DOC CON FOR WSSB/OSD R Shay

University of California
Lawrence Livermore Laboratory
P.O. Box 808
Livermore, CA 94550
01CY ATTN DOC CON for Technical Information Dept.
01CY ATTN DOC CON for L-156 R Kalibjian
01CY ATTN DOC CON for L-545 D Meeker (Class L-477)

Office of Military Application
Department of Energy
Washington, DC 20545
01CY ATTN DOC CON for Classified Library

Sandia Laboratories
P.O. Box 5800
Albuquerque, NM 87115
01CY ATTN DOC CON for J Hood
01CY ATTN DOC CON for F Coppage
01CY ATTN DOC CON for R Gregory

Central Intelligence Agency
ATTN: RD/SI, RM 5G48, HQ Bldg.
Washington, DC 20505
01CY ATTN RD/SI RM 5G48 HQ Bldg.

Department of Transportation
Federal Aviation Administration
Headquarters Sec Div. ASE-300
800 Independence Avenue, SW
Washington, DC 20591
01CY ATTN ARD-350

Aeroject Electro-Systems Co.
Div. of Aerojet-General Corp.
P.O. Box 296, 1100 W Hollyvale Drive
Azusa, CA 91702
01CY ATTN SV/8711/70

Aerospace Corp.
P.O. Box 92957
Los Angeles, CA 90009
01CY ATTN W Willis
01CY ATTN V Josephson
01CY ATTN J Reinheimer
01CY ATTN R Crolius
01CY ATTN S Bower
01CY ATTN I Garfunkel

AVCO Research & Systems Group
201 Lowell Street
Wilmington, MA 01887
01CY ATTN W Broding

Battelle Memorial Institute
505 King Avenue
Columbus, OH 43201
01CY ATTN D Hamman
01CY ATTN R Blazek

BDM Corp.
P.O. Box 9274
Albuquerque International
Albuquerque, NM 87119
01CY ATTN D Alexander
01CY ATTN Marketing

Bendix Corp.
Communication Division
E Joppa Road
Baltimore, MD 21204
01CY ATTN Document Control

Bendix Corp.
Research Laboratories Division
Bendix Center
Southfield, MI 48075
01CY ATTN M Frank

Boeing Co.
P.0. Box 3707
Seattle, WA 98124
01CY ATTN 8K-38
01CY ATTN H Wicklein
01CY ATTN R Caldwell

Booz-Allen and Hamilton, Inc.
776 Shrewsbury Avenue
Tinton Falls, NJ 07724
01CY ATTN R Chrisner

Brown Engineering Company, Inc.
Cummings Research Park
Huntsville, AL 35807
01CY ATTN J McSwain

Burroughs Corp.
Federal and Special Systems Group
Central Ave. and Route 252
P.O. Box 517
Paoli, PA 19301
01CY ATTN Product Eval. Lab.

California Institute of Technology
Jet Propulsion Lab
4800 Oak Grove Drive
Pasadena, CA 91103
01CY ATTN A Stanley
01CY ATTN J Bryden

Charles Stark Draper Lab, Inc.
555 Technology Square
Cambridge, MA 02139
01CY ATTN R Haltmaier
01CY ATTN P Kelly

Computer Sciences Corp.
1400 San Mateo Blvd. SE
Albuquerque, NM 87108
01CY ATTN A Schiff

Cutler-Hammer, Inc.
AIL Division
COMAC Road
Deer Park, NY 11729
01CY ATTN Central Tech. Files
A Anthony

Dikewood Industries, Inc.
1009 Bradbury Drive, SE
Albuquerque, NM 87106
01CY ATTN L Davis

E-Systems, Inc.
ECI Division
P.O. Box 12248
St. Petersburg, FL 33733
01CY ATTN R. French

E-Systems, Inc.
Greenville Division
P.O. Box 1056
Greenville, TX 75401
01CY ATTN Division Library

Effects Technology, Inc.
5383 Hollister Avenue
Santa Barbara, CA 93111
01CY ATTN E. Steele

Ex-Cal, Inc.
First National Bldg. E
Suite 1516
Albuquerque, NM 87108
01CY ATTN R Dickhaut

Fairchild Camera and Instrument Corp.
464 Ellis Street
Mountain View, CA 94040
01CY ATTN SEC CON for D Myers

Fairchild Industries, Inc.
Sherman Fairchild Technology Center
20301 Century Blvd.
Germantown, MD 20767
01CY ATTN B Patton

University of Florida
ATTN: Security Officer
P.O. Box 284
Gainesville, FL 32601
01CY ATTN H Sisler

Ford Aerospace & Communications Corp.
Ford & Jamboree Roads
Newport Beach, CA 92663
01CY ATTN Tech Infor Services
01CY ATTN K Attinger
01CY ATTN E Poncelet, Jr.

Ford Aerospace & Communications Corp.
3939 Fabian Way
Palo Alto, CA 94303
01CY ATTN D McMorrow MS G30
01CY ATTN E Hahn MS X22
01CY ATTN Technical Library

Franklin Institute
20th Street and Parkway
Philadelphia, PA 19103
01CY ATTN R Thompson

Garrett Corp.
P.O. Box 92248, 9851 Sepulveda Blvd.
Los Angeles, CA 90009
01CY ATTN Dept 93-9 Weir

General Electric Co.
Space Division
Valley Forge Space Center
P.O. Box 8555
Philadelphia, PA 19101
01CY ATTN J Peden VFSC, 4230M
01CY ATTN D Tasca
01CY ATTN L Chasen
01CY ATTN L Sivo
01CY ATTN J Andrews
01CY ATTN D Long
01CY ATTN L Jeffers

General Electric Co.
Re-Entry & Environmental Systems Div.
P.O. Box 7722
3198 Chestnut Street
Philadelphia, PA 19101
01CY ATTN J Palcheesky, Jr.
01CY ATTN W Patterson
01CY ATTN Tech. Lab.
01CY ATTN R Benedict

General Electric Co.
Ordnance Systems
100 Plastics Avenue
Pittsfield, MA 01201
01CY ATTN J Reidl

General Electric Co.
Aircraft Engine Business Group
Evendale Plant, Int. Hwy. 75 S
Cincinnati, OH 45215
01CY ATTN R Hellen

General Electric Co.
Aerospace Electronics Systems
French Road
Utica, NY 13503
01CY ATTN C Hewison

General Electric Co.-Tempo
Center for Advanced Studies
816 State Street (P O Drawer QQ)
Santa Barbara, CA 93102
01CY ATTN M Espig
01CY ATTN R Rutherford
01CY ATTN W McNamara
01CY ATTN DASIAC

General Research Corp.
Santa Barbara Division
P.O. Box 6770
Santa Barbara, CA 93111
01CY ATTN Technical Information Office

Georgia Institute of Technology
Office of Contract Administration
ATTN: RSCH Security Coordinator
Atlanta, GA 30332
01CY ATTN Res. & Sec. Coord. for H Denny

Goodyear Aerospace Corp.
Arizona Division
Litchfield Park, AZ 85340
01CY ATTN Security Control Station

GTE Sylvania, Inc.
Electronics Systems GRP-Eastern Div.
77 A Street
Needham, MA 02194
01CY ATTN C Thornhill Librarian
01CY ATTN L Blaisdell

Harris Corp.
Electronics Systems Division
P.O. Box 37
Melbourne, FL 32901
01CY ATTN C Davis
01CY ATTN W Abare

Harris Corp.
Harris Semiconductor Division
P.O. Box 883
Melbourne, FL 32901
01CY ATTN MNGR Linear Eng.
01CY ATTN MNGR Bipolar Digital Eng.

Hazeltine Corp.
Pulaski Road
Greenlawn, NY 11740
01CY ATTN Tech. Info Ctr M Watte

Honeywell, Inc.
Avionics Division
13350 U.S. Highway 19, N
St. Petersburg, FL 33733
01CY ATTN MS 725-5

Hughes Aircraft Co.
Centinela and Teale
Culver City, CA 90230
01CY ATTN CTDC 6/E110
01CY ATTN D Binder
01CY ATTN J Singletary
01CY ATTN K Walker

Hughes Aircraft Co.
El Segundo Site
P.O. Box 92919
Los Angeles, CA 90009
01CY ATTN E Smith M S A620

IBM Corp.
Route 17C
Owego, NY 13827
01CY ATTN Electromagnetic Compatibility
01CY ATTN Mono Memory Systems

Institute for Defense Analyses
400 Army-Navy Drive
Arlington, VA 22202
01CY ATTN Tech. Info. Services

General Electric Co.-Tempo
Alexandria Office
Huntington Building, Suite 300
2560 Huntington Avenue
Alexandria, VA 22303
01CY ATTN DASIAC

GTE Sylvania, Inc.
189 B Street
Needham Heights, MA 02194
01CY ATTN J Waldron
01CY ATTN P Fredrickson

International Tel & Telegraph Corp.
500 Washington Avenue
Nutley, NJ 07110
01CY ATTN Dept. 608

Ion Physics Corp.
S Bedford Street
Burlington, MA 01803
01CY ATTN R Evans

IRT Corp.
P.O. Box 81087
San Diego, CA 02138
01CY ATTN MDC
01CY ATTN Physics Division
01CY ATTN R Mertz
01CY ATTN Systems Effects Division

Jaycor
205 S Whiting Street, Suite 500
Alexandria, VA 22304
01CY ATTN R Sullivan

Johns Hopkins University
Applied Physics Lab.
Johns Hopkins Road
Laurel, MD 20810
01CY ATTN P Partridge

Kaman Sciences Corp.
P.O. Box 7463
Colorado Springs, CO 80933
01CY ATTN Dir Science & Technology Div
01CY ATTN J Lubell
01CY ATTN W Ware
01CY ATTN President
01CY ATTN W Rich

Litton Systems, Inc.
Guidance & Control Systems Division
5500 Canoga Avenue
Woodland Hills, CA 91364
01CY ATTN J Retzler
01CY ATTN V Ashby

Lockheed Missiles & Space Co., Inc.
P.O. Box 504
Sunnyvale, CA 94086
01CY ATTN L Rossi
01CY ATTN B Kimura
01CY ATTN E Smith
01CY ATTN D Wolfhard

Lockheed Missiles and Space Co., Inc.
3251 Hanover Street
Palo Alto, CA 94304
01CY ATTN Reports Library

M.I.T. Lincoln Lab
P.O. Box 73
Lexington, MA 02173
01CY ATTN Library A-082

Martin Marietta Corp.
Orlando Division
P.O. Box 5837
Orlando, FL 32805
01CY ATTN TIC/MP-30

Martin Marietta Corp.
Denver Division
P.O. Box 179
Denver, CO 80201
01CY ATTN Research Library
01CY ATTN P Kase

McDonnell Douglas Corp.
P.O. Box 516
St. Louis, MO 63166
01CY ATTN T Ender
01CY ATTN Library

McDonnell Douglas Corp.
5301 Bolsa Avenue
Huntington Beach, CA 92647
01CY ATTN P Albrecht

Mission Research Corp.
P.O. Drawer 719
Santa Barbara, CA 93102
01CY ATTN M Van Blaricum

Mission Research Corp.
EM System Applications Division
1400 San Mateo Blvd., SE Suite A
Albuquerque, NM 87108
01CY ATTN David E. Merewether

Mission Research Corp. - San Diego
P.O. Box 1209
La Jolla, CA 92038
(Victor A J Van Lint)
01CY ATTN V Van Lint
01CY ATTN J Raymond

National Academy of Sciences
ATTN: Committee on Atmospheric Sciences
2101 Constitution Avenue, NW
Washington, DC 20418
10CY ATTN R Shane

University of New Mexico
Electrical Engineering & Computer Science Dept.
Albuquerque, NM 87131
01CY ATTN Harold Southward

Northrop Corp.
Northrop Research & Technology Ctr.
1 Research Park
Palos Verdes Peninsula, CA 90274
01CY ATTN J Srour

Northrop Corp.
Northrop Research and Technology Ctr.
3401 W Broadway
Hawthorne, CA 90250
(Desires only 1 copy of CNWDI Mat)
01CY ATTN J Srour
01CY ATTN O Curtis, Jr.

Northrop Corp.
Electronic Division
2301 W 120th Street
Hawthorne, CA 92050
01CY ATTN D Strobel

University of Oklahoma
Research Institute
1808 Newton Drive
Norman, OK 73069
01CY ATTN R Wood

Palisades Inst. for Rsch. Services, Inc.
201 Varick Street
New York, NY 10014
01CY ATTN Secretary

Physics International Co.
2700 Merced Street
San Leandro, CA 94577
01CY ATTN Division 6000
01CY ATTN J Shea

Power Conversion Technology, Inc.
11588 Sorrento Valley Road
San Diego, CA 92121
01CY ATTN V Fargo

R & D Associates
P.O. Box 9695
Marina Del Rey, CA 90291
01CY ATTN C MacDonald
01CY ATTN S Rogers
01CY ATTN W Karzas

Rand Corp.
1700 Main Street
Santa Monica, CA 90406
01CY ATTN C Crain

Raytheon Co.
Hartwell Road
Bedford, MA 01730
01CY ATTN G Joshi

Raytheon Co.
528 Boston Post Road
Sudbury, MA 01776
01CY ATTN H Flescher

RCA Corp.
Government Systems Division
Astro Electronics
P.O. Box 800, Locust Corner
East Windsor Township
Princeton, NJ 08540
01CY ATTN G Brucker

RCA Corp.
David Sarnoff Research Center
P.O. Box 432
Princeton, NJ 08540
01CY ATTN Office N103
01CY ATTN Security Dept. L Minich

Rensselaer Polytechnic Institute
P.O. Box 965
Troy, NJ 12181
01CY ATTN R Gutmann (Unclas only)

Research Triangle Institute
P.O. Box 12194
Research Triangle Park, NC 27709
(All Corres. ATTN: Sec. Office)
01CY ATTN Eng. Div. Mayrant Simons, Jr.

Rockwell International Corp.
P.O. Box 3105
Anaheim, CA 92803
01CY ATTN James E. Bell HA10
01CY ATTN N Rudie
01CY ATTN K Hull

Rockwell International Corp.
Space Division
12214 South Lakewood Boulevard
Downey, CA 90241
01CY ATTN D Stevens
01CY ATTN TIC D/41-092 AJ01

Rockwell International Corp.
815 Lapham Street
El Segundo, CA 90245
01CY ATTN T B Yates
01CY ATTN TIC BA08

Rockwell International Corp..
Collins Divisions
400 Collins Road NE
Cedar Rapids, IA 52406
01CY ATTN TIC 106-216
01CY ATTN Alan A Langenfeld

Sanders Associates, Inc.
95 Canal Street
Nashua, NH 03060
01CY ATTN L Brodeur
01CY ATTN M Aitel

Science Applications, Inc.
P.O. Box 2351
LaJolla, CA 92038
01CY ATTN J Beyster
01CY ATTN L Scott

Science Applications, Inc.
Huntsville Division
2109 W Clinton Avenue
Suite 700
Huntsville, AL 35805
01CY ATTN N Byrn

Science Applications, Inc.
8400 Westpark Drive
McLean, VA 22101
01CY ATTN W Chadsey

Singer Co.
Data Systems
150 Totowa Road
Wayne, NJ 07470
01CY ATTN Tech. Info Center

Sperry Rand Corp.
Sperry Microwave Electronics
P.O. Box 4648
Clearwater, FL 33518
01CY ATTN Engineering Laboratory

Sperry Rand Corp.
Sperry Division
Marcus Avenue
Great Neck, NY 11020
01CY ATTN P Maraffino
01CY ATTN C Craig
01CY ATTN R Viola

Sperry Rand Corp.
Sperry Flight Systems
P.O. Box 21111
Phoenix, AZ 85036
01CY ATTN D Andrew Schow

Spire Corp.
P.O. Box D
Bedford, MA 01730
01CY ATTN Roger G Little

SRI International
333 Ravenswood Avenue
Menlo Park, CA 94025
01CY ATTN P Dolan

Sundstrand Corp.
4751 Harrison Avenue
Rockford, IL 61101
01CY ATTN Research Department

Tetra Tech, Inc.
1911 Fort Myer Drive
Arlington, VA 22209
01CY ATTN T Simpson

Texas Instruments, Inc.
P.O. Box 6015
Dallas, TX 75265
01CY ATTN D Manus

TRW Defense & Space Sys. Group
One Space Park
Redondo Beach, CA 90278
01CY ATTN H Holloway
02CY ATTN R Plebuch
02CY ATTN O Adams
01CY ATTN A Narevsky
01CY ATTN Technical Information Ctr.
01CY ATTN Vulnerability & Hardness
Laboratory
01CY ATTN R Webb

TRW Defense & Space Sys. Group
San Bernardino Operations
P.O. Box 1310
San Bernardino, CA 92402
01CY ATTN R Kitter
01CY ATTN F Fay

TRW Systems and Energy
P.O. Box 368
Clearfield, UT 84015
01CY ATTN R Mathews

Vought Corp.
P.O. Box 225907
Dallas, TX 75265
(Formerly LTV Aerospace Corp.)
01CY ATTN R Tomme
01CY ATTN Library

Westinghouse Electric Corp.
Defense and Electronic Systems Ctr.
P.O. Box 1693
Baltimore-Washington Intl. Airport
Baltimore, MD 21203
01CY ATTN MS 3330