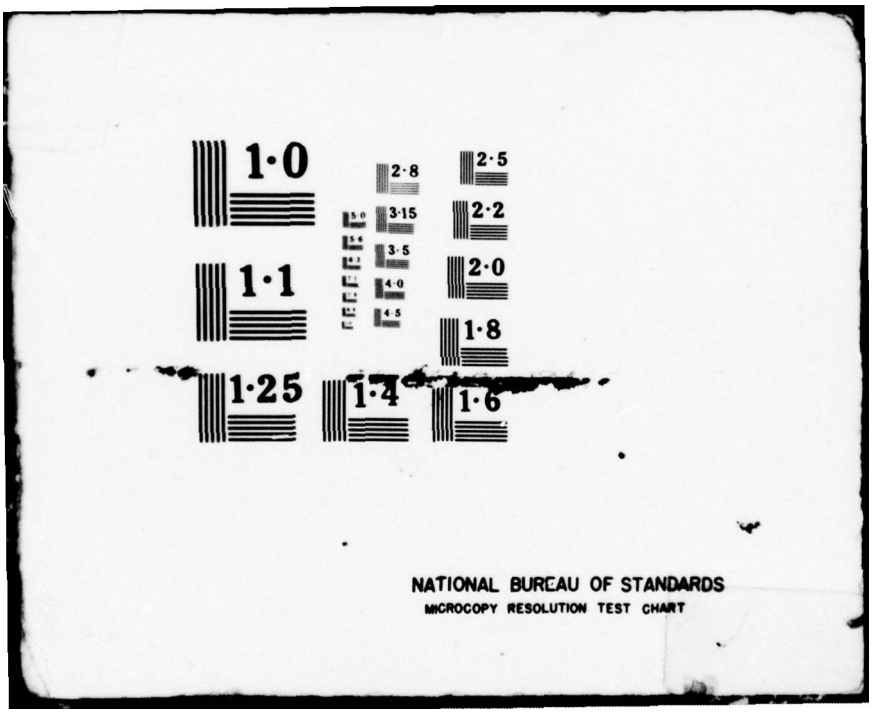
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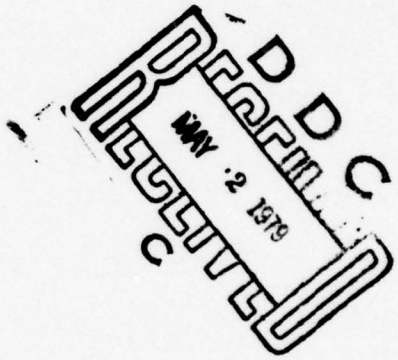
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by

Larry G. Meiners

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Capacitance-voltage measurements over a wide frequency range and surface photovoltage measurements were made on GaAs and InP MIS diodes. In GaAs, the surface potential could only be varied about 0.4 eV about a point 0.8-0.9 eV below the conduction band. In contrast, InP displayed a considerably smaller surface state density and the p-type material could be inverted.

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ABSTRACT OF DISSERTATION

DIELECTRIC-SEMICONDUCTOR INTERFACES OF

GALLIUM ARSENIDE AND INDIUM PHOSPHIDE

This thesis reports an experimental investigation of the properties of insulator-semiconductor structures formed using the semiconductors InP and GaAs in conjunction with a number of dielectrics. The insulators studied on GaAs were the native oxide formed by anodization, sputtered-silicon nitride, and pyrolytically-deposited silicon nitride. The investigation of InP was limited to the study of pyrolytically deposited silicon dioxide layers. Capacitance-voltage (C-V) measurements over a wide frequency range and surface photovoltage measurements on metal-insulator-semiconductor (MIS) diodes formed from these structures were used to determine the bulk doping, surface potential variation, and interface state density of the semiconductor.

The data on GaAs indicate that on n-type substrates the Fermi level at the surface is pinned at a point 0.8 - 0.9 eV below the conduction band minimum (CBM). Surface potential variations of only $\sim$ 0.4 V are possible around this position. Results on p-type material were in agreement except that the zero bias position of the Fermi level at the surface was 0.7 - 0.8 below the CBM. Accumulations of neither electrons nor holes were observed on the GaAs samples for surface electric field magnitudes to to 16^6 V/cm. A minimum surface state density of 2×10^{12} cm^{-2} eV^{-1} was calculated near the zero bias position with values greater than 10^{14} cm^{-2} eV^{-1} as the band edges were approached.

Data on the n-type InP samples indicate that the surface is near flatband with zero applied gate bias. With applied electric fields of

$\pm 10^6$ V/cm the surface could be modulated from accumulation into or nearly into inversion. The surface state density rose from 6×10^{11} cm^{-2} eV^{-1} at a point 0.6 eV below the CBM to 2×10^{12} cm^{-2} eV^{-1} at flatband. Data on the p-type samples indicated that the surface is near inversion with zero gate bias. The surface could be fully inverted with positive gate bias; however, the surface did not reach flatband with negative gate bias. This apparent discrepancy between the data on the n- and p-type material was not fully resolved.

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TABLE OF CONTENTS

		Page
ABSTRACT		iii
LIST OF TABLES		vii
LIST OF FIGURES		viii
Chapter 1.	INTRODUCTION	1
Chapter 2.	THEORETICAL BACKGROUND	4
	2.1 Surface Capacitance	6
	2.2 Surface States	15
	2.3 Surface Conductance	18
	2.4 Surface Photovoltage	20
	2.5 References	26
Chapter 3.	LITERATURE REVIEW	38
	3.1 Gallium Arsenide	39
	3.2 Indium Phosphide	46
	3.3 References	47
Chapter 4.	EXPERIMENTAL PROCEDURE	50
	4.1 Sample Preparation	50
	4.1.1 Sputtering	50
	4.1.2 Anodization	53
	4.1.3 Pyrolysis	53
	4.1.4 Sample Contacts	54
	4.2 Measurement Techniques	55
	4.2.1 Quasistatic Capacitance Measurement	55
	4.2.2 Small Signal Capacitance	56
	4.2.3 Surface Photovoltage Measurements	58
	4.3 References	60

Page

Chapter 5. DATA AND ANALYSIS. 69
5.1 C-V Measurements on n-type GaAs 69
5.1.1 Quasistatic and 1 MHz C-V Measurements . . . 71
5.1.2 High-Frequency C-V Measurements. 71
5.1.3 Comparison of Surface State Model with Experiment 74
5.1.4 Impurity Density from Deep-Depletion Capacitance. 76
5.2 C-V Measurements on p-type GaAs 80
5.3 C-V Measurements on n-type InP. 82
5.3.1 Frequency Dispersion in the Dielectric . . . 83
5.3.2 Impurity Density from Deep-Depletion Measurements 84
5.3.3 Surface State Density. 85
5.4 C-V Measurements on p-type InP. 88
5.5 Surface Photovoltage Measurements on GaAs 92
5.6 Surface Photovoltage Measurements on InP. 95
5.7 References. 96

Chapter 6. CONCLUSIONS. 128
6.1 Gallium Arsenide. 129
6.2 Indium Phosphide. 130
6.3 Suggestions for Further Work. 131
6.4 References. 132

ACKNOWLEDGMENTS 133

LIST OF TABLES

Table		Page
5.1	Surface potential vs. gate bias for anodized n-GaAs. . . .	73
5.2	Calculated surface parameters for n-InP at 300°K	85
5.3	Calculated surface parameters for n-InP at 85°K.	87
5.4	Calculated surface parameters for p-InP at 300°K	89
5.5	Surface potential variations calculated from quasistatic data (p-InP)	91

LIST OF FIGURES

Figure		Page
2.1	Energy band diagram for a depleted n-type semiconductor. . . .	27
2.2	Energy band diagram for an n-type semiconductor in accumulation	28
2.3	Surface charge vs. surface potential for n = 10^{15} cm^{-3} GaAs at 300°K.	29
2.4	Differential space-charge capacitance vs. surface potential for n = 10^{15} cm^{-3} GaAs at 300°K.	30
2.5	Total capacitance vs. applied voltage for an MIS device on an n-type semiconductor	31
2.6	Equivalent circuit for the MIS device including the effects of surface states.	32
2.7	Surface conductance vs. surface potential for n = 10^{15} cm^{-3} GaAs at 300°K.	33
2.8	Excess carrier density vs. excess generation rate for GaAs . .	34
2.9	Energy band diagram of an n-type semiconductor with illumination	35
2.10	Surface photovoltage (Δv_s) vs. excess carrier density for n = 10^{15} cm^{-3} GaAs at 300°K.	36
2.11	Surface photovoltage (Δv_s) vs. excess carrier density for n = 10^{15} cm^{-3} GaAs at 300°K.	37
4.1	Ion beam sputtering system	61
4.2	Auger electron spectrum of sputtered-silicon nitride layer . .	62
4.3	Quasistatic capacitance measurement circuit.	63
4.4	Small signal capacitance measuring circuit	64
4.5	Stripline jig.	65
4.6	Schematic diagram of stripline circuit	66
4.7	C-V measurements from 10 Hz to 150 Hz on a GaAs Schottky diode	67
4.8	Circuit for surface photovoltage measurement	68

Figure		Page
5.1	C-V characteristic of a sputtered-silicon oxide on n-type GaAs MIS device T = 300°K	97
5.2	I-V characteristic of a sputtered-silicon oxide on n-type GaAs MIS device	98
5.3	C-V characteristic of a sputtered-silicon nitride on n-type GaAs MIS device	99
5.4	Frequency dispersion in the C-V characteristics of a sputtered-silicon nitride on n-type GaAs MIS device.	100
5.5	C-V characteristics of an n-type GaAs MIS device with a dielectric formed by anodization at a current density of 8 $\mu A/cm^2$ to 80 V	101
5.6	C-V characteristics of a sputtered-silicon nitride on n-type GaAs MIS device measured from 100 Hz to 150 Hz. . . .	102
5.7	C-V characteristic of a pyrolytic-silicon nitride on n-type GaAs MIS device measured from DC to 150 Hz.	103
5.8	C-V data for an MIS device constructed using n-type GaAs with a dielectric formed by anodization at a current density of 8 $\mu A/cm^2$ to 5 V	104
5.9	Low frequency C-V data for the device of Figure 5.8.	105
5.10	Deep-depletion capacitance vs. gate bias for the device of Figure 5.8	106
5.11	C-V characteristics of an anodized n-type GaAs MIS device measured with fast sweep rates.	107
5.12	Deep-depletion capacitance vs. gate bias for the device of Figure 5.11.	108
5.13	C-V characteristics of an anodized p-type GaAs MIS device measured from DC to 150 MHz	109
5.14	Deep-depletion capacitance vs. gate bias for the device of Figure 5.13.	110
5.15	Surface state density of GaAs.	111
5.16	C-V characteristics of a pyrolytic-silicon oxide on n-type InP MIS device measured from DC to 450 MHz.	112

Figure		Page
5.17	C-V characteristics of a pyrolytic-silicon oxide on n-type, InP MIS device with and without illumination, T = 85°K	113
5.18	C-V characteristics of a pyrolytic-silicon oxide on n-type InP MIS device measured with sweep rates of 100 m V/S and 400 V/S, T = 300°K	114
5.19	Deep-depletion capacitance vs. gate bias for the device of Figure 5.18.	115
5.20	Deep-depletion capacitance vs. gate bias for the device of Figure 5.17.	116
5.21	Surface state density of n-type InP coated with silicon oxide.	117
5.22	C-V data for a pyrolytic-silicon oxide on p-type InP MIS device measured from DC to 1 MHz; T = 300°K.	118
5.23	1 MHz C-V curve for the device of Figure 5.22 measured with a gate bias sweep rate of 600 V/S	119
5.24	C-V data taken from DC to 1 MHz on a p-type InP silicon oxide MIS device; T = 77°K	120
5.25	Depletion-capacitance vs. gate voltage for the device of Figure 5.24	121
5.26	Surface photovoltage vs. gate bias for a thermally-oxidized n-type silicon MIS device	122
5.27	C-V characteristic for the device of Figure 5.26	123
5.28	Surface photovoltage vs. gate bias for an anodized n-type GaAs MIS device	124
5.29	C-V characteristic for the device of Figure 5.28	125
5.30	Energy band diagram for an MIS device with charge-trapping in the insulator.	126
5.31	Surface photovoltage vs. gate bias for a pyrolytic-silicon oxide on n-type InP MIS device	127

CHAPTER 1

INTRODUCTION

An enormous amount of theoretical and experimental work has been published on metal-insulator semiconductor (MIS) structures which employ thermally-oxidized silicon. The technology of these devices has reached a level of perfection which permits the formation of insulator-semiconductor interfaces in which essentially no extraneous charge trapping mechanisms are present. The understanding of such structures has reached a level which permits the design and large-scale technological applications of MIS transistors and MIS integrated circuit. Although several other semiconductors appear to be superior to silicon for certain MIS applications such as microwave logic and signal processing, the understanding of the surface properties of the alternative semiconductors is in a primitive state. The dielectrics that have been tried on such semiconductors always have exhibited larger amounts of charge-trapping at the interface and greater frequency dispersion of the insulator than that attainable on silicon. In fact, the surface properties are, in many cases, so poor that comparison between experiment and the theoretical models developed for silicon can be very difficult and often confusing. An example of this confusion is the present controversy concerning the amount of surface potential modulation possible on GaAs-dielectric interfaces. An obvious need exists to examine, in detail, the results of measurements and analysis applied to semiconductors other than silicon, to compare the characteristic aspects of surfaces produced with our present technology to those of ideal surfaces and those obtained on silicon MIS structures.

This dissertation reports the results of an experimental investigation made of the surfaces of the semiconductors, gallium arsenide and indium phosphide, which have been coated with a thin dielectric layer. These materials were chosen because (at least as far as bulk properties are concerned) both have the potential advantages desired for field-effect transistors (FETs). The electron mobilities are high and the band-gaps are large enough to assure that the semiconductors remain extrinsic at normal operating temperatures.

A goal of this work has been to establish quantitatively the surface carrier concentrations that may be produced on these materials. The conclusions reached have been based primarily on capacitance-voltage (C-V) measurements made on MIS structures. The underlying constraints for comparing theory with experiment have been examined on these III-V semiconductors. The present work is unique in that a comprehensive series of C-V measurements has been made on each device tested, and comparison between theory and experiment has been made by insisting that any proposed model be simultaneously consistent with several different types of capacitance measurement. A result of this work has been the realization that the interfacial charge of the III-V semiconductors can respond at much higher frequencies than those corresponding to silicon surfaces. Consequently, much of the published work (especially that on GaAs) which reports only relatively low frequency measurements (1 MHz or less) contains significant errors of interpretation. Also it appears that previously reported anomalous results obtained on InP surfaces can be

explained and that the surface charge densities are higher than those previously reported.

CHAPTER 2

THEORETICAL BACKGROUND

The purpose of this Chapter is to describe the mathematical model necessary for understanding the remainder of the thesis. This model is based on a solution of Poisson's equation for the space charge region at the semiconductor surface. An analytical expression can be obtained for the surface electric field in a semiconductor as a function of the total potential drop across the surface region. From this expression equations may be derived for the parametric variations of the surface capacitance and the total surface charge. These calculated quantities can be compared with experimental measurements. The surface conductivity and surface photovoltage may also be calculated although these must be obtained by numerical techniques. Such calculations will also be discussed; they must be included in order to understand several previously published papers on GaAs as well as results described in this thesis.

Space charge regions can extend to significant depths (10 - 10,000Å depending on the impurity doping density) in semiconductors. This is due to the fact that the mobile charge density is lower than that in metals by a factor of 10^5 to 10^{10} for doping densities of 10^{14} to 10^{19} cm^{-3}. The ability of the mobile charge to screen the interior of the semiconductor from external electric fields increases with increasing charge density. Once one admits the possibility of a space charge region in a semiconductor, it follows that an electric field exists within and an electric potential exists across the space charge layer. If the value of this potential can be determined experimentally then for non-degenerate semiconductors

the use of the Boltzmann distribution function allows calculation of the carrier densities in the space charge region.

Consider the case of a parallel plate capacitor composed of a metal-insulator-semiconductor (MIS) sandwich. Ideally, when an electric potential is applied between the metal and the semiconductor, the component of the electric displacement vector perpendicular to the surface is continuous across the semiconductor-dielectric boundary. If the displacement vector is continuous, then the electric field within the semiconductor is uniquely related to the field in the insulator. As will be shown the surface electric field can then be uniquely related to such experimentally-measurable quantities as the surface capacitance and surface conductivity by the solution of Poisson's equation. Thus the relationships between applied voltage, surface capacitance, and carrier density are all calculable.

However, the condition of continuity of electric displacement is found to apply only for very specially prepared semiconductor-insulator interfaces. It is much more common for the electric displacement to be discontinuous because of the presence of charges trapped at the interface between the semiconductor and insulator. In addition, the magnitude and polarity of this charge will be a function of the surface electric field. It will no longer be the case that each charge applied to the metal gate attracts a mobile charge of opposite sign in the semiconductor bulk. Interpretation of surface capacitance and surface conductivity measurements thus becomes considerably more complicated if interfacial charging mechanisms are present.

2.1 Surface Capacitance

Consider the situation in which an electric field is applied perpendicularly to a semiconductor surface by a metal plate which does not quite touch the semiconductor. For this device no current will flow at equilibrium although alternating currents may be sustained. For the present time it is assumed that charge may exist only in bulk states and not at the semiconductor surface. From Gauss' law we know that the charge will redistribute itself until at equilibrium, all of the electric field lines will be terminated on charges in the vicinity of the surface. If this were not the case, the non-zero field within the bulk of the crystal would cause a steady state flow of current and this would redistribute the charge until the point was reached where no current flowed.

We wish now to solve Poisson's equation for the potential distribution within the semiconductor for a fixed external electric field. Consider the band picture of an n-type semiconductor surface as shown in Fig. 2.1. The potential energy plot is for a surface in which electrons are depleted from the surface. In this diagram E_c is the conduction band energy minimum in the bulk, E_v is the bulk valence band energy maximum, E_F is the Fermi energy, E_i is the Fermi energy for the intrinsic material, V is the electrostatic potential within the semiconductor, and ϕ_B the difference between E_i and E_F deep in the crystal is called the bulk potential.

When the static electric field is directed away from the semiconductor (negative charge on the metal plate), a positive space charge will be produced in the semiconductor. This can be either the fixed charge of the

ionized donor impurities, or that of the mobile valence band holes. This is the situation in Fig. 2.1 in which the energy bands bend up at the surface. The electrostatic potential at the surface (V_s) is, by convention, negative in this case. If the electric field is directed toward the surface (positive charge on the metal plate) then the space charge will consist of conduction band electrons. For this situation the bands bend downward as shown in Fig. 2.2 and the surface potential (V_s) is by convention positive.

It is usually adequate to consider analytically the case of non-degenerate carrier distributions (particles spaced far enough apart so as to be noninteracting) for the electrons and holes. This allows the use of Maxwell-Boltzmann statistics in calculating the mobile carrier densities. This formalism is described by the equation

$$\frac{D_1}{D_2} = \frac{e^{-E_1/kT}}{e^{-E_2/kT}} \tag{2.1}$$

where $D_{1,2}$ and $E_{1,2}$ represent the density and energy respectively of identical particles at two separate points in the crystal. In the present case the carrier densities are given by

$$n(x) = n_B \exp(qV(x)/kT) \tag{2.2}$$

and

$$p(x) = p_B \exp(-qV(x)/kT)$$

where n_B and p_B are the bulk electron and hole densities respectively, and $V(x)$ is defined to be zero in the bulk material. As a further constraint the electron and hole densities are related by the mass action law, viz.,

$$n_B p_B = n_i^2 \tag{2.3}$$

where n_i is the carrier concentration in undoped or intrinsic material. The assumption is made that all impurities remain ionized. This will be the case for shallow impurity levels at room temperature. The volume charge density within the semiconductor is then given by

$$\rho = (- n + p + N_{Di} - N_{Ai}) \tag{2.4}$$

where N_{Di} and N_{Ai} are the ionized donor and acceptor densities respectively. The one-dimensional Poisson equation

$$\frac{d^2V}{dx^2} = - \rho/\epsilon_s \tag{2.5}$$

must be solved for the above charge distribution with the boundary conditions that

$$V|_{x=0} = V_s \quad \text{and} \quad V|_{x=\infty} = 0 \tag{2.6}$$

Since $\frac{d^2V}{dx^2} = 0$ far into the bulk, from Eqs. (2.4) and (2.5) one has the result that

$$\begin{aligned} p_B - n_B + N_{Di} - N_{Ai} = 0 \quad \text{or,} \\ N_{Di} - N_{Ai} = n_B - p_B \end{aligned} \tag{2.7}$$

The charge density can then be written as

$$\rho = (n_B\, e^{qV/kT} + p_B\, e^{-qV/kT} + n_B - p_B) \tag{2.8}$$

or

$$\rho = [n_B(1 - e^{qV/kT}) - p_B(1 - e^{-qV/kT})]$$

Then

$$\frac{d^2V}{dx^2} = \frac{q}{\varepsilon_s}\left[p_B(1 - e^{-qV/kT}) - n_B(1 + e^{qV/kT})\right] \tag{2.9}$$

Use of the integrating factor $\frac{dV}{dx}$ within Eq. (2.9) leads to

$$\int_x^\infty \frac{d^2V}{dx^2}\frac{dV}{dx}\,dx = \frac{q}{\varepsilon_s}\int_x^\infty \left[p_B(1 - e^{-qV/kT}) - n_B(1 + e^{qV/kT})\right]\frac{dV}{dx}\,dx \tag{2.10}$$

which reduces to

$$\frac{1}{2}\left(\frac{dV}{dx}\right)^2\Bigg|_x^\infty = \frac{q}{\varepsilon_s}\int_V^0 \left[p_B\,(1 - e^{-qV/kT}) - n_B\,(1 + e^{qV/kT})\right]dV \tag{2.11}$$

Integration of this expression gives the electric field,

$$E = -\frac{dV}{dx} = \pm\left[\frac{2kT}{\varepsilon_s}\right]^{1/2}\left[p_B\,(e^{-qV/kT} + qV/kT - 1) + n_B\,(e^{qV/kT} - qV/kT - 1)\right]^{1/2} \tag{2.12}$$

where the positive sign is taken for $V_s<0$ ($\vec{E}$ points away from surface), and the negative sign is taken for $V_s>0$. The total charge per unit area in the surface region is given by Gauss' law

$$Q_s = \varepsilon_s E_s \tag{2.13}$$

where the electric field at the surface is

$$E_S = -\left.\frac{dV}{dx}\right|_{x\,=\,0} \tag{2.14}$$

or,

$$Q_s = \pm(2\varepsilon_s kT)^{1/2}\left[p_B(e^{-qV_s/kT} + qV_s/kT - 1) + n_B\,(e^{qV_s/kT} - qV_s/kT - 1)\right]^{1/2} \tag{2.15}$$

where the positive sign applies when $V_s<0$ and vice versa. One can define a differential capacitance per unit area of the semiconductor surface C_D and a bit of algebra gives

$$C_D \equiv \frac{\partial Q_s}{\partial V_s} = \left[\frac{q^2 \varepsilon_s}{2kT} \right]^{1/2} \frac{\left| p_B(1 - e^{-qV_s/kT}) + n_B (e^{qV_s/kT} - 1) \right|}{\left[p_B (e^{-qV_s/kT} + qV_s/kT - 1) + n_B (e^{qV_s/kT} - qV_s/kT - 1) \right]^{1/2}} \tag{2.16}$$

All of the above results apply to either n-type material or p-type material.

The reader can see at this point that the differential capacitance for a particular semiconductor is a function only of the impurity doping, temperature, and surface potential. Thus an experimental measurement of the parametric variations of the differential capacitance of the space charge layer of such an ideal semiconductor allows a determination of the corresponding variations of the surface potential. One can then calculate the total surface charge, carrier densities, and electric field, and avoid the far more difficult experimental problem of measuring these quantities directly.

A plot of Q_s as a function of surface potential is shown for 10^{15} n-GaAs in Fig. 2.3. This also illustrates the terminology in common use. Positive values of V_s correspond to an excess of surface electrons called accumulation. Negative values of V_s, up to the value of the Fermi level, in intrinsic material, correspond to the situation in which electrons are driven away from the surface; consequently the electric field terminates

on the ionized donors. This is termed the depletion regime. Further changes in the gate voltage which make the hole density at the surface equal to the electron density in the bulk lead to weak surface inversion. More negative values of V_s produce a larger density of surface holes. Such a surface layer of carriers whose sign is opposite to that of the charge carriers in the bulk is called an inversion layer. A plot of the differential capacitance calculated from Eq. (2.16) for this same material is shown in Fig. 2.4. As expected this curve rises steeply when the surface density of carriers becomes larger than the bulk value.

A question not yet touched upon here is the condition under which Eq. (2.16) corresponds to a physically-measurable capacitance. In a very general sense the space charge capacitance is the equivalent circuit element which represents the flow of charge carriers in the surface region in response to an external electric field. In an AC applied field this current must decay to zero in a time interval much smaller than the inverse of the AC frequency. Currents which are in phase with the applied AC field may be described as a conductive component. Equation (2.16) holds only if the conductive component of the current can be ignored. The frequency at which this occurs depends on the material type and the surface electric field.

Equation (2.16) for the differential capacitance gives essentially a low frequency curve because equilibrium statistics were used for the carrier populations. In the accumulation regime for the material described in Fig. 2.4 a space charge perturbation should come to equilibrium in a

time τ_o of the order of $\tau_o = \varepsilon_s \rho$ which for $10^{15}/cm^3$ n-GaAs is approximately 10^{-12} sec. This capacitance should then remain constant for all practical measurement frequencies. A depleted n-type surface can be approximated by assuming that the electrons are totally absent from a slab extending to a depth w from the surface. The space charge then consists only of the ionized donor impurities which have a volume density N_D. The thickness of this layer may be obtained from the requirement that $Q_{sc} = N_D w$ using Eq. (2.15) to obtain the total space charge Q_{sc}. Fluctuations in charge that result from small changes in surface potential then occur in a narrow region at depth w from the surface. Since this charge is in good communication with the semiconductor bulk, equilibrium should be restored in a time interval of the same order as the bulk relaxation time.

In inversion the situation is quite different. Hofstein and Warfield[1] and Heiman[2] have treated this problem and find that normally the largest source of minority carriers for the inversion layer is generation of carriers within the depletion region. The generation rate (g) of electron hole pairs in the depletion layer is given by

$$g = \frac{n_i}{2\tau} \tag{2.17}$$

where τ is the minority carrier lifetime. From a very general point of view one would expect that the inversion layer would come to equilibrium when the total elapsed time multiplied by the carrier generation rate was equal to the bulk impurity doping. Thus equilibrium is expected when

$$t = \frac{N_D}{g} = \tau \frac{N_D}{n_i} \tag{2.18}$$

For GaAs at 300°K, $n_i = 1.94 \times 10^6/cm^3$, and $\tau \simeq 10^{-9}$ sec. Thus for $N_D = 10^{16}\ cm^{-3}$, $t \simeq 10$ sec.

This time is quite long and thus the assumption of equilibrium statistics for the minority carriers is in general not valid. Attention must therefore be paid to the frequency response of the space charge layer. Among the first things one might wish to calculate is the capacitance in the limit of high frequencies. Rigorously the approach that would be taken is to repeat the earlier described calculations assuming that the minority carriers are not able to respond to the frequency of the measurement voltage.[3] However, a good approximation can be obtained[4] by taking the high frequency capacitance to be constant in the inversion region at the value obtained when the surface potential is equal to twice the bulk potential ($-2\phi_B/q$). This treatment is more than satisfactory for the purposes of the present discussion.

A somewhat different type of surface capacitance measurement can be made in which the surface is quickly pulsed into depletion. In this case the minority carrier terms can be neglected in Eqs. (2.12), (2.15), and (2.16). Since the terms due to majority carrier accumulation can be neglected also, the result for n-type material is then

$$E_s = \mp \left[\frac{2qn_B}{\varepsilon_s}\right]^{1/2} \left[- V_s - \frac{kT}{q}\right]^{1/2} \tag{2.19}$$

$$Q_s = \pm (2\varepsilon_s n_B q)^{1/2} [- V_s - kT/q]^{1/2} \tag{2.20}$$

$$C_D = \left[\frac{q\varepsilon_s n_B}{2}\right]^{1/2} [- V_s - kT/q]^{-1/2} \tag{2.21}$$

The above equations comprise what is called the depletion approximation; they apply in either of two cases: the first is the above mentioned one produced with pulsed gate bias, and the second is the one which would be created if the minority carriers were transported away from the surface to the metal gate electrode, if the metal electrode were in direct contact with the semiconductor. The resulting structure is called a Schottky[5] barrier or metal-semiconductor junction. The approximation for the minimum in the high frequency capacitance can be obtained from Eq. (2.21) upon the substitution of $\phi_B = kT\ell n(n_B/n_i)$ for V_s. Recall that the basis for this approximation is that the space charge capacitance measured at high frequency saturates at a minimum value given when $V_s = 2\phi_B/q$. This leads to

$$C_D\Big|_{min}^{HF} \cong \left[\frac{4\epsilon_s kT\ell n(n_B/n_i)}{q^2 n_B}\right]^{1/2} \tag{2.22}$$

The discussion so far has centered around only the differential capacitance of the semiconductor space charge layer. In an actual measurement the capacitance of the dielectric region between the metal electrode and the semiconductor must also be considered. In practice the dielectric employed is not usually air but rather a thin insulating layer formed on the semiconductor surface. For the present, this dielectric will be considered to be linear and nondispersive so that the capacitance of the resulting structure will be

$$C_m = \frac{C_i C_D}{C_i + C_D} \tag{2.23}$$

where C_m is the measured capacitance and C_i is the capacitance of the dielectric layer given by

$$C_i = \frac{\varepsilon_i}{d} \tag{2.24}$$

where ε_i and d are the dielectric constant and thickness of the insulator respectively. The electric field in the insulator is related to the electric field in the semiconductor by Gauss' law

$$\varepsilon_i E_i = \varepsilon_s E_s \tag{2.25}$$

and the voltage drop across the insulator is

$$V_i = E_i d = \frac{\varepsilon_s}{\varepsilon_i} E_s d \tag{2.26}$$

The total voltage drop across the MIS structure is then

$$V_g = V_i + V_s \tag{2.27}$$

The gate bias-dependent capacitance of an MIS structure constructed with the semiconductor of Fig. 2.3 would then appear as shown in Fig. 2.5.

2.2 Surface States

The previous treatment of the fields and charges within the semiconductor ignored the effects of charge which may be trapped at the interface between the insulator and the semiconductor. In practice these cannot be ignored and may, in some instances, dominate the measurements made on MIS devices. The surface of a semiconductor can be assumed to contain energy states not present in the bulk material. These may be related to the

discontinuity of the crystal lattice or to defects and impurities localized upon it. The corresponding energy levels can be charged or discharged as a function of the measurement frequency and bias voltage. An equivalent circuit for an MIS device which includes the effect of surface charging is shown in Fig. 2.6. where C_{ss} represents a frequency and surface potential dependent capacitor related to the surface states. From a qualitative point of view one would expect the time constants for surface charging to be a function of the surface potential. The trapping rate of the surface states should be proportional to the product of the surface carrier concentration and the number of surface traps.

The total amount of charge trapped at the semiconductor-insulator interface can be determined experimentally by comparing the measured C-V characteristics to those predicted by the equations previously developed. The technique first used for doing this, proposed by Terman,[6] consists of comparing the high frequency capacitance curve to that predicted by theory. In order for this technique to be valid, the experimenter must first determine the measurement frequency which is high enough so that the surface states no longer respond and, therefore, the corresponding surface state capacitance is zero.

In order to apply Terman's method the insulator capacitance and the semiconductor doping must be determined accurately. An accurate determination of C_i requires biasing the surface by the applied potential such that $C_{sc} + C_{ss} >> C_i$. The measured capacitance is then equal to C_i, and the capacitance of the space charge layer can be determined as a function of the gate voltage from Eq. (2.23). This procedure allows calculation of

the corresponding surface potential V_s from Eq. (2.16) and semiconductor space charge Q_{sc} from Eq. (2.15) if the impurity doping and temperature are known. Since $V_g = V_i + V_s$ the voltage across the insulator can be determined as well as the total charge (Q_T)

$$Q_T = V_i C_i = Q_{sc} + Q_{ss} \tag{2.28}$$

Thus

$$Q_{ss} = (V_g - V_s)C_i - Q_{sc} \tag{2.29}$$

The derivative of the surface state charge with respect to surface potential is commonly called the surface state density N_{ss}, i.e.,

$$N_{ss} = \frac{1}{q} \frac{\partial Q_{ss}}{\partial V_s} \tag{2.30}$$

This method yields the number per eV per cm^2 of all surface states except those which respond more slowly than the frequency of the gate bias sweep.

A different technique for measuring the same quantity, first proposed by Berglund[7] consists of measuring the capacitance at a very low frequency. The measured capacitance is

$$C_m = \frac{dQ_T}{dV_g} \tag{2.31}$$

Recall that

$$dQ_T = C_i dV_i \tag{2.32}$$

so that

$$C_m = C_i \frac{dV_i}{dV_g} \tag{2.33}$$

Using

$$dV_g = dV_i + dV_s \tag{2.34}$$

then

$$C_m = C_i[1 - \frac{dV_s}{dV_g}] \tag{2.35}$$

or

$$\frac{dV_s}{dV_g} = 1 - C_m/C_i \tag{2.36}$$

This equation can be integrated to give

$$V_s(V_g) = \int_{-\infty}^{V_g}[1 - C_m/C_i]dV_g + \Delta \tag{2.37}$$

where Δ is an additive constant. The change in surface potential between any two values of gate voltage can be determined by integrating the area between 1 and C_m/C_i on a normalized C-V curve. The constant Δ, must be determined by a separate measurement which gives the surface potential unambiguously for at least one value of gate voltage or alternatively the carrier density must be determined accurately. Once the surface potential vs. gate voltage relationship is known, then the surface state density can be determined from Eq. (2.30) in the same way as that used in the Terman method described earlier.

2.3 Surface Conductance

The change in conductance which occurs at a semiconductor surface in response to a change in surface potential may be calculated using a minor extension of the formalism developed for the space charge capacitance. The quantity of interest is that defined by the equation

$$\Delta\sigma = q(\mu_e \Delta n + \mu_n \Delta p) \tag{2.38}$$

where $\Delta\sigma$ is the change in conductance in mhos, μ_e and μ_n are the electron and hole mobilities respectively, and Δn and Δp are the deviations in the total numbers of electrons and holes from their bulk values. These are defined by

$$\Delta n = \int_0^\infty (n - n_B)\, dx \qquad \text{and,} \tag{2.39}$$

$$\Delta p = \int_0^\infty (p - p_B)\, dx \tag{2.40}$$

The conductance change, $\Delta\sigma$, is that which would be measured by attaching leads to a square sample and the units are commonly expressed as mhos/square or mhos/ . With the substitution of Eqs. (2.2) and (2.12) into Eq. (2.39) it becomes

$$\Delta n = \left[\frac{\epsilon_s}{2kT}\right]^{1/2} \int_{V_s}^{0} \frac{n_B(1 - e^{qV/kT})dV}{\left[p_B(e^{-qV/kT} + qV/kT - 1) + n_B(e^{qV/kT} - qV/kT - 1)\right]^{1/2}} \tag{2.41}$$

Substitution of Eqs. (2.2) and (2.12) into Eq. (2.40) yields

$$\Delta p = \left[\frac{\epsilon_s}{2kT}\right]^{1/2} \int_{V_s}^{0} \frac{p_B(e^{-qV/kT} - 1)dV}{\left[p_B(e^{-qV/kT} + qV/kT - 1) + n_B(e^{qV/kT} - qV/kT - 1)\right]^{1/2}} \tag{2.42}$$

In all probability neither of these integrals has an analytical solution; however, they may be evaluated numerically quite simply. The result of this computation for 10^{15} cm^{-3} n - GaAs at 300°K assuming $\mu_e = 6000$ cm^2 V^{-1} s^{-1} and $\mu_h = 400$ cm^2 V^{-1} s^{-1} is shown in Fig. 2.7.

The surface conductance passes through zero for two values of surface potential. As expected it has a zero crossing when $V_s = 0$, and also crosses zero in the inversion region. A useful feature of this effect is the minimum in conductance which occurs for one unique value of surface potential. If a minimum in conductance can be obtained experimentally, then this gives a reference point for determining the value of the surface potential for one value of the applied bias. Comparison of the calculated vs. experimental conductance curves then allows the determination of the surface potential values that are achievable.

2.4 Surface Photovoltage

Imagine a structure which consists of a slab of n-type semiconducting material on the back side of which has been placed a metal layer which provides an ohmic contact. On the front side is placed either a semitransparent metal layer which provides a blocking contact or an insulating dielectric layer on which there is deposited a metal layer. Assume that radiation which penetrates the metal contact, the dielectric layer, and enters the semiconductor has a wavelength which corresponds to an energy greater than that of the fundamental bandgap of the semiconductor. The radiation induces electronic transitions from the valence band to the conduction band producing electron-hole pairs which are separated by the electric field associated with the surface potential. This charge separation gives rise to a voltage which is a function of various parameters of the excitation process and the material parameters. This voltage is defined as the surface photovoltage.

Once generated, the excess carriers will recombine with an effective lifetime, τ, and will be transported through diffusion and drift processes

to other regions of the semiconductor. If an electric field is initially present in the surface region (caused, for instance, by fixed charges attached to the surface of the semiconductor), then the electrons and holes will drift in opposite directions after generation. If, for example, fixed negative charges are present on the surface, then the electrons will move toward the interior. If steady state illumination is maintained, then a population of holes will be maintained next to the fixed negative charge at the surface. This charge has the effect of reducing the electric field within the semiconductor and also the total potential between the front and back contact. In the limit of high illumination levels one can imagine the potential initially present across the sample due to the fixed negative surface charge to be reduced to zero when the surface hole population is equal to the fixed surface charge population. The above qualitative description is the basis of the surface photovoltage effect. Illumination of the front surface of a semiconducting sample reduces the initial value of surface potential and from this reduction inferences about the value of the surface potential may be made. In the discussion to follow an estimate will be made of the excess surface carrier densities to be expected for various light intensities and the surface photovoltage will be calculated for the corresponding range of excess carrier densities.

The rate of change of the carrier density $(\frac{\partial n}{\partial t})$ in a semiconductor is described precisely by the continuity equation

$$\frac{\partial n}{\partial t} = (G-\gamma) + g_E + \frac{1}{q} \nabla \cdot J_n \qquad (2.43)$$

This equilibrium expression states the requirement that $\partial n/\partial t$ be equal to the thermal generation rate (G) of carriers less the recombination rate (γ)

plus the generation rate of excess carriers (g_E) (caused, for example, by optical absorption) plus the net current flow ($\frac{1}{q} \nabla \cdot J_n$) into the region. At thermal equilibrium $\frac{\partial n}{\partial t} = g_E = \frac{1}{q} \nabla \cdot J_n = 0$ so that

$$G = \gamma \tag{2.44}$$

Two simplifying assumptions will be made. The first is that the thermal generation rate (G) is unaffected by excess carrier densities. The second is that the recombination rate is directly proportional to the product of the electron (n) and hole (p) densities. This can be expressed as

$$\gamma = G\left(\frac{np}{n_i^2}\right) \tag{2.45}$$

where (n_i) is the electron density in intrinsic material. Equation (2.43) can therefore be written as

$$\frac{\partial n}{\partial t} = G \frac{n_i^2 - np}{n_i^2} + g_E \tag{2.46}$$

for the condition in which no current is flowing into the region. Since overall charge neutrality must be maintained when a sample is illuminated, equal numbers of excess electrons (n_e) and holes (p_e) will be generated. Thus

$$n = n_o + n_e \tag{2.47}$$

$$p = p_o + p_e = p_o + n_e \tag{2.48}$$

where n_o and p_o represent the thermal equilibrium electron and hole densities, respectively. Equation (2.46) becomes

$$\frac{\partial n}{\partial t} = G\left[\frac{n_i^2 - (n_o + n_e)(p_o + p_e)}{n_i^2}\right] + g_E \qquad (2.49)$$

At steady state $\partial n/\partial t = 0$ and this expression becomes

$$G\, n_e^2 + G\, n_e(n_o + p_o) - n_i^2\, g_E = 0 \qquad (2.50)$$

which has the solution

$$n_e = 2\left(\frac{g_E}{G}\right)\left(\frac{n_i^2}{n_o + p_o}\right)\left[1 + \left[1 + 4\left(\frac{g_E}{G}\right)\left(\frac{n_i}{n_o + p_o}\right)^2\right]^{1/2}\right]^{-1} \qquad (2.51)$$

Using a value for G of 527 $cm^{-3}\ s^{-1}$ [8] Eq. (2.51) was evaluated for several carrier concentrations and the results are plotted in Fig. 2.8. Also shown are the illumination levels required to provide a given generation rate of excess carriers using 0.6 μm (He-Ne) laser radiation incident on GaAs. They were roughly estimated by assuming that all of the incident photons are absorbed in a distance equal to the inverse absorption coefficient (α). Using a value for α of 10^5 cm^{-1} at 0.6 μm (2.6 eV)[9] in GaAs and the equation $g_E = J\alpha$ where J is the incident radiation intensity, the values shown in Fig. 2.8 were obtained.

The solution of the space charge equation that was obtained in Section 2.1 was derived using the assumption of thermal equilibrium throughout the sample. When the semiconductor surface is illuminated, several simplifying assumptions must be made before a solution can be obtained. The first is that with continuous illumination a steady state condition is reached in which the diffusion current of either type of carrier is zero and requires that the surface recombination of electrons and holes be negligible. This assumption permits the definition of a quasi Fermi level

for electrons (F_n) and for holes (F_p) as shown in Fig. 2.9. These quantities are defined in terms of the steady state densities of electrons (n^*) and holes (p^*) in the bulk during illumination. Thus

$$n_B^* = n_B \, e^{q(F_n - E_F)/kT} \tag{2.52}$$

$$p_B^* = p_B \, e^{q(E_F - F_p)/kT} \tag{2.53}$$

In the space charge region the charge densities are given by

$$n^* = n_B \, e^{q(V^* + F_n - E_F)/kT} \tag{2.54}$$

$$p^* = p_B \, e^{q(-V^* - F_p + E_F)/kT} \tag{2.55}$$

Following Eq. (2.8) the charge density introduced in Poisson's equation can then be written as

$$\rho = (-n^* + p^* + n_B^* - p_B^*) \tag{2.56}$$

$$\rho = (-n_B^* \, e^{qV^*/kT} + p_B \, e^{-qV^*/kT} + n_B^* - p_B^*) \tag{2.57}$$

which is seen to be of exactly the same form as Eq. (2.8) if each term representing a quantity with illumination is replaced by its thermal equilibrium value. The total surface charge density calculated from a solution of Poisson's equation is then of the same form as Eq. (2.15) and is given by

$$Q_s^* = \pm(2\varepsilon_s kT)^{1/2} \left[p_B^* \left(e^{-qV_s/kT} + \frac{qV_s^*}{kT} - 1 \right) + n_B^* \left(e^{qV_s^*/kT} - qV_s^*/kT - 1 \right) \right]^{1/2} \tag{2.58}$$

In order to obtain a solution for the dependence of the surface potential

on illumination, an additional assumption is made that the charge trapped in surface states does not change during the illumination period. If this is the case, then from Gauss' law the total space charge in the semiconductor does not change after illumination and

$$Q_{sc}(n_B, p_B, V_s) = Q_{sc}(n_B^*, p_B^*, V_s^*) \tag{2.59}$$

It was assumed that the optical generation created equal numbers (n_e) of excess electrons and holes, and that the nonequilibrium electron and hole densities were given by

$$\begin{aligned} n_B^* &= n_B + n_e \\ p_B^* &= p_B + n_e \end{aligned} \tag{2.60}$$

Equation (2.59) was then solved numerically for V_s^* and the surface photovoltage (ΔV_s) was calculated from

$$\Delta V_s = V_s - V_s^* \tag{2.61}$$

This solution was obtained for 10^{15} cm^{-3} and 10^{17} cm^{-3} GaAs as a function of n_e for a number of initial values of surface potential. A monotonic increase in surface photovoltage with increasing illumination is observed in Figs. 2.9 and 2.10 which saturates at the initial value of surface potential. If the surface is initially inverted a dramatic change in the shape of the curves is obtained. This is because essentially no change in surface potential is obtained until sufficient carriers are generated to neutralize the surface inversion layer.

A typical measurement would consist of operation on a vertical line drawn through a specified value of excess carrier density. The surface potential would then be varied by the application of a bias to the gate of the MIS capacitor. The surface photovoltage thereby resulting could be determined from the intersections of this vertical line with the surface photovoltage curves.

2.5 References

1. S. R. Hofstein and G. Warfield, Solid-State Electron., 8, 321(1965).
2. F. P. Heiman, IEEE Trans. on Electron Devices ED-14, 781(1967).
3. A. Goetzberger, E. Klairmann and M. Schulz, CRC Critical Reviews in Solid-State Sciences, 6, 1(1976).
4. S. M. Sze, Physics of Semiconductor Devices, p. 436, Wiley-Interscience, New York, 1969.
5. W. Schottky, Natarwiss., 26, 843(1938).
6. L. M. Terman, Solid-State Electron., 5, 285(1962).
7. C. N. Berglund, IEEE Trans. on Electron Devices, ED-13, 701(1966).
8. C. Hilsum, Progress in Semiconductors, 9, 137(1965).
9. J. I. Pankove, Optical Processes in Semiconductors, p. 53, Prentice-Hall, Inc., Englewood Cliffs, N.J.

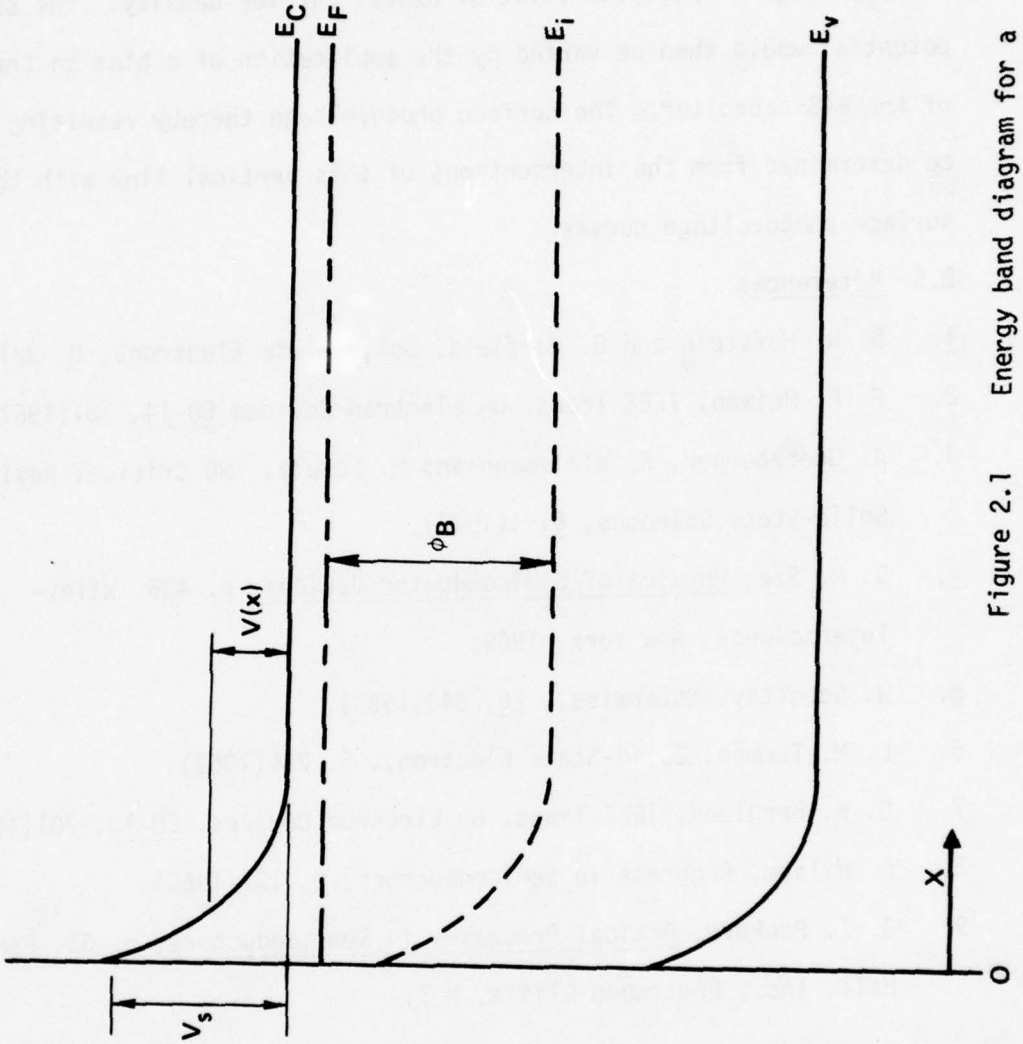


Figure 2.1 Energy band diagram for a depleted n-type semiconductor

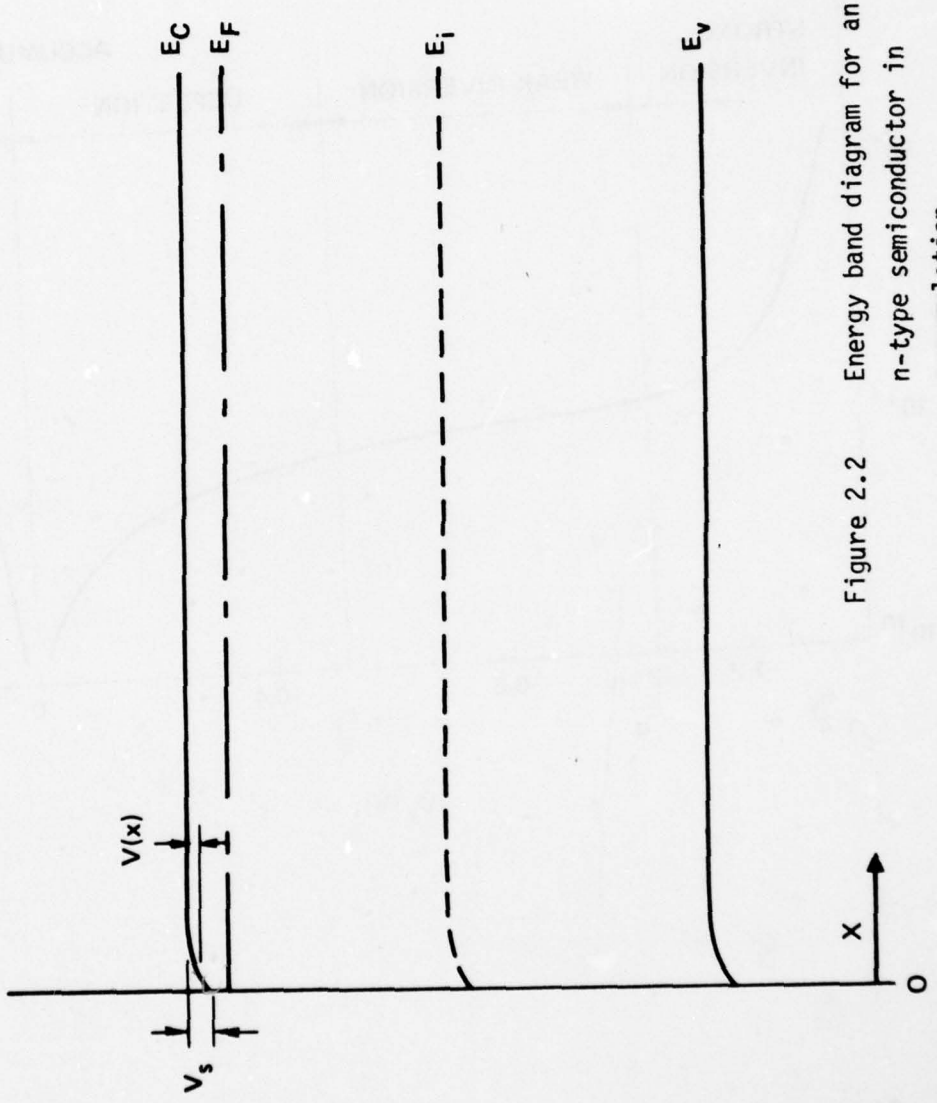


Figure 2.2 Energy band diagram for an n-type semiconductor in accumulation

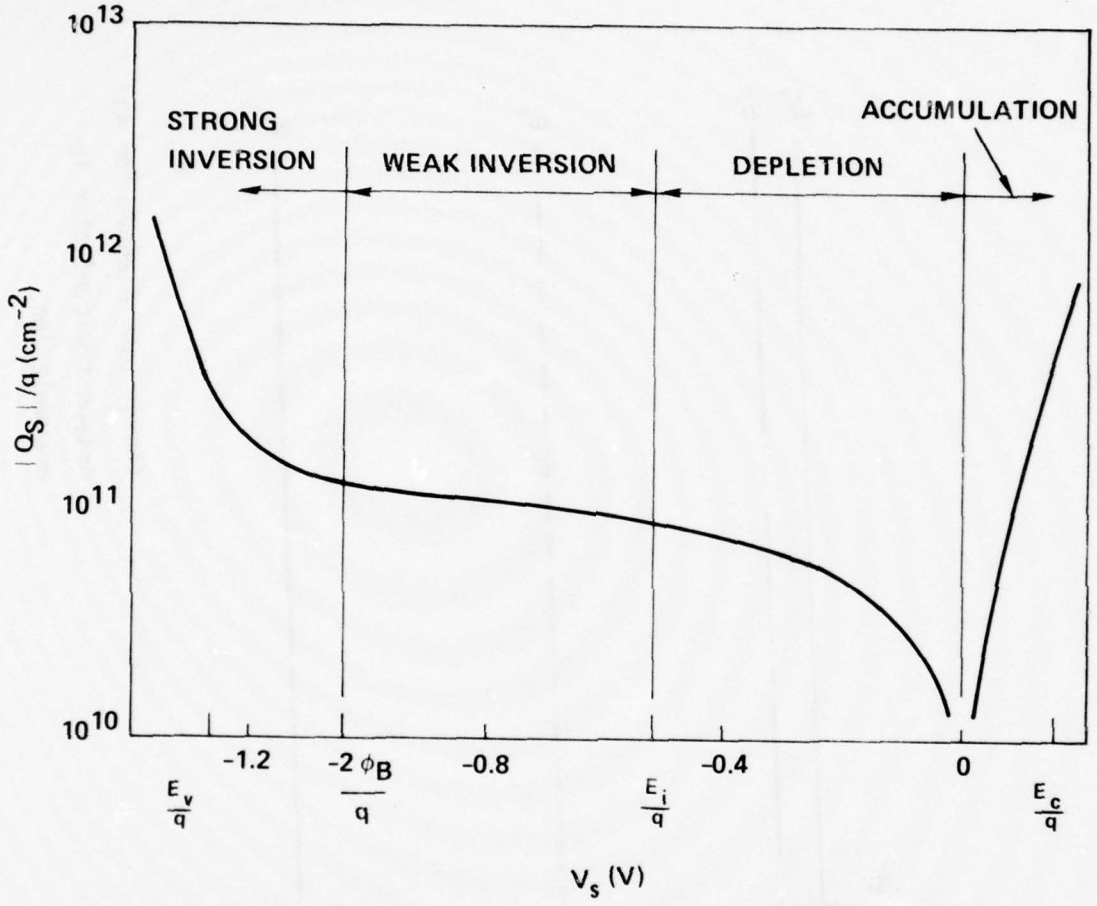


Figure 2.3 Surface charge vs surface potential for $n = 10^{15}$ cm^{-3} GaAs at 300°K; ϕ_B is the energy corresponding to the bulk potential; E_v, E_i, and E_c are, respectively, the peak of the valence band, the intrinsic Fermi level, and the minimum of the conduction band.

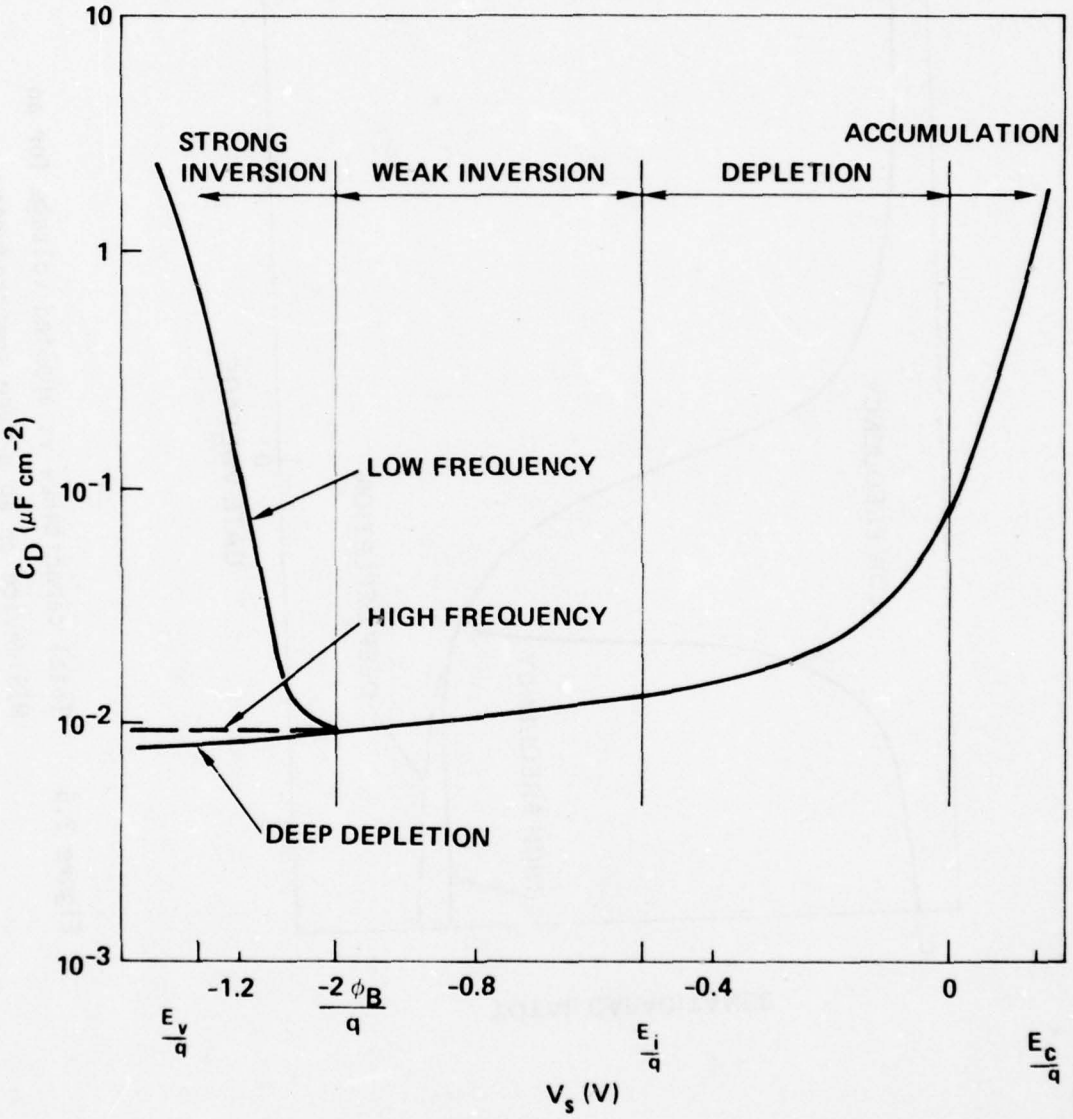


Figure 2.4 Differential space charge capacitance vs surface potential for $n = 10^{15}$ cm^{-3} GaAs at 300°K; ϕ_B is the energy corresponding to the bulk potential; E_v, E_i and E_c are, respectively, the peak of the valence band, the intrinsic Fermi level, and the minimum of the conduction band.

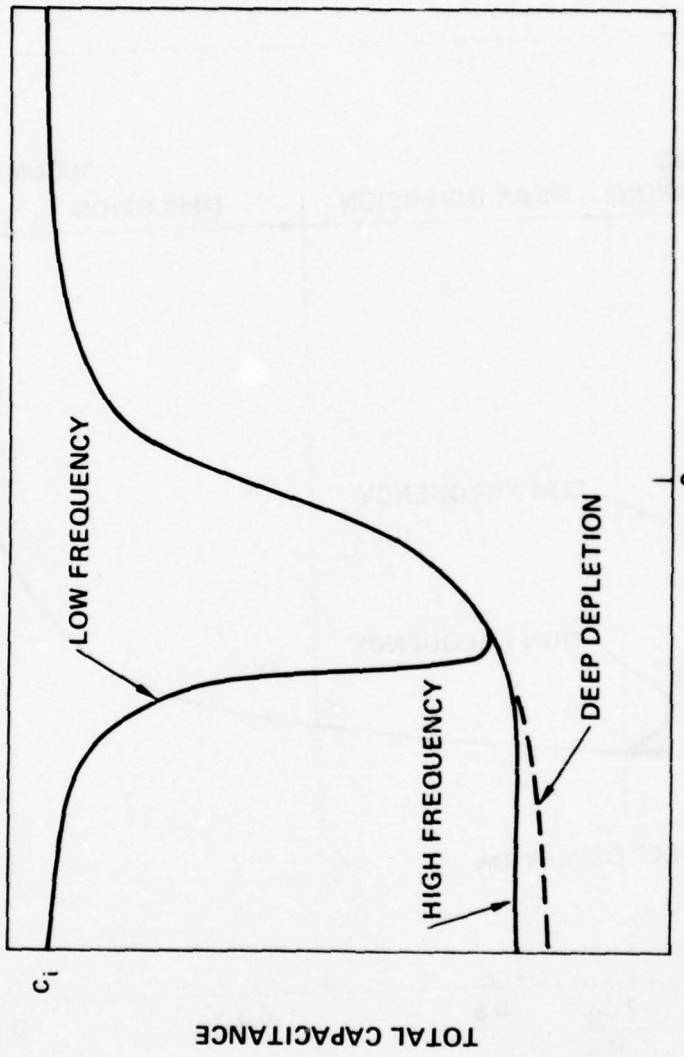


Figure 2.5 Total capacitance vs applied voltage for an MIS device on an n-type semiconductor.

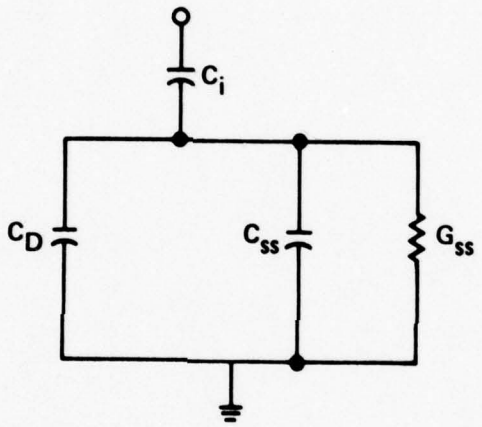


Figure 2.6 Equivalent circuit for the MIS device including the effects of surface states; C_D is the depletion capacitance, C_i is the capacitance corresponding to the insulating layer, C_{ss} is the capacitance due to surface states, and G_{ss} is the parallel conductance.

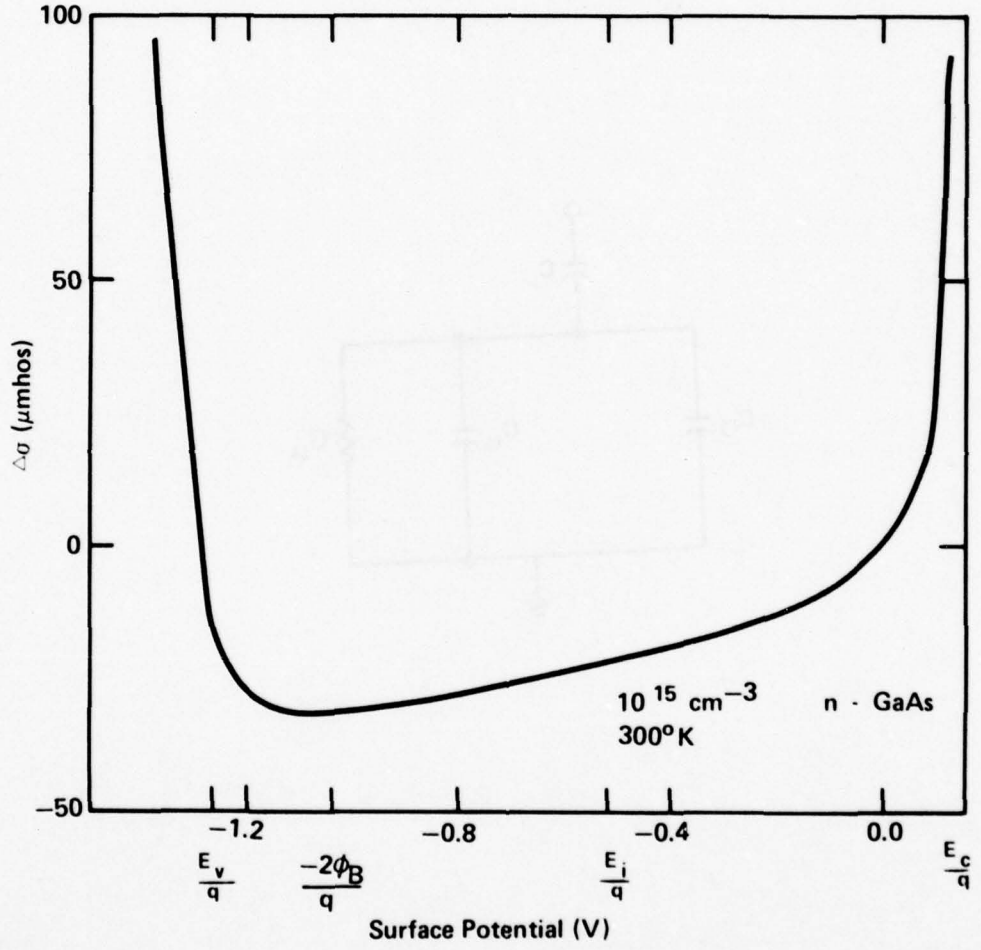


Figure 2.7 Surface conductance vs surface potential for $n = 10^{15}$ cm^{-3} GaAs at 300°K; ϕ_B is the energy corresponding to the bulk potential; E_V, E_i and E_C are, respectively, the peak of the valence band, the intrinsic Fermi level, and the minimum of the conduction band.

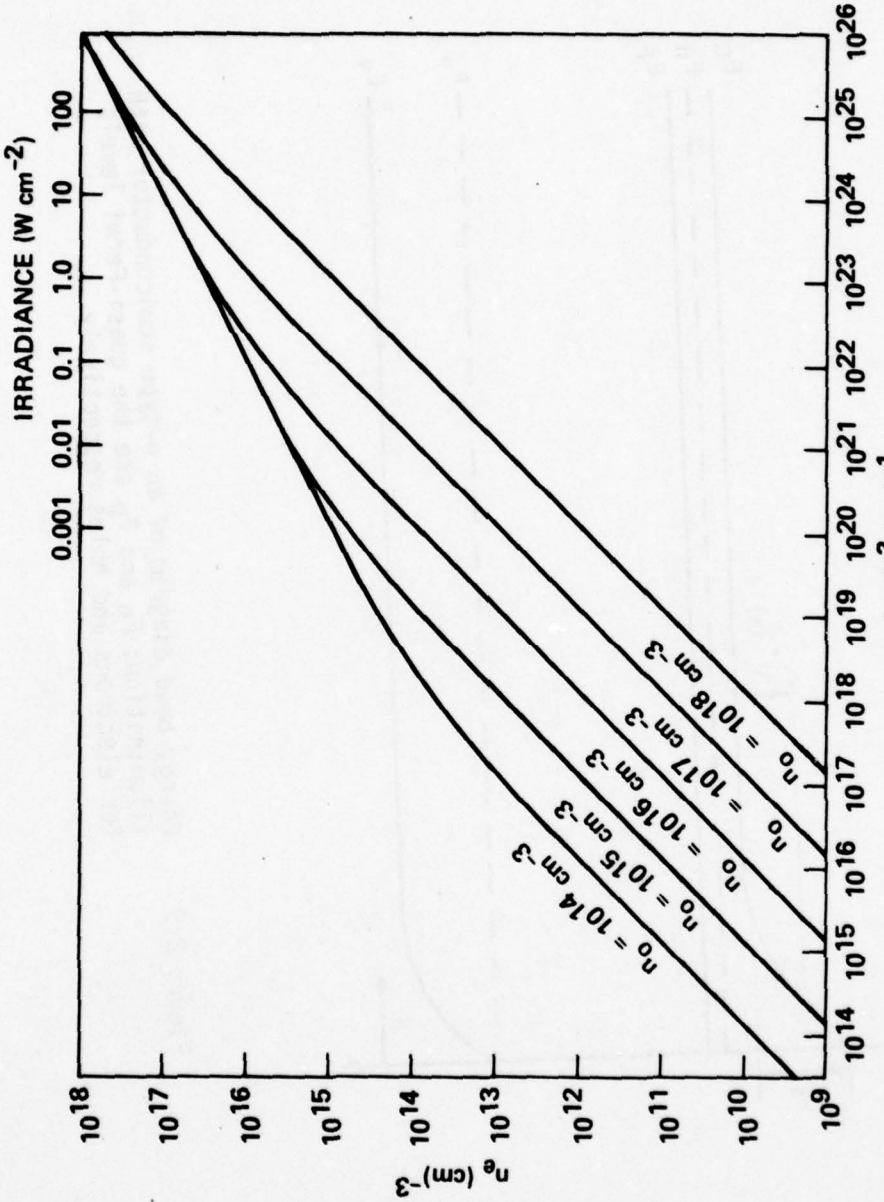


Figure 2.8 Excess carrier density vs excess generation rate for GaAs

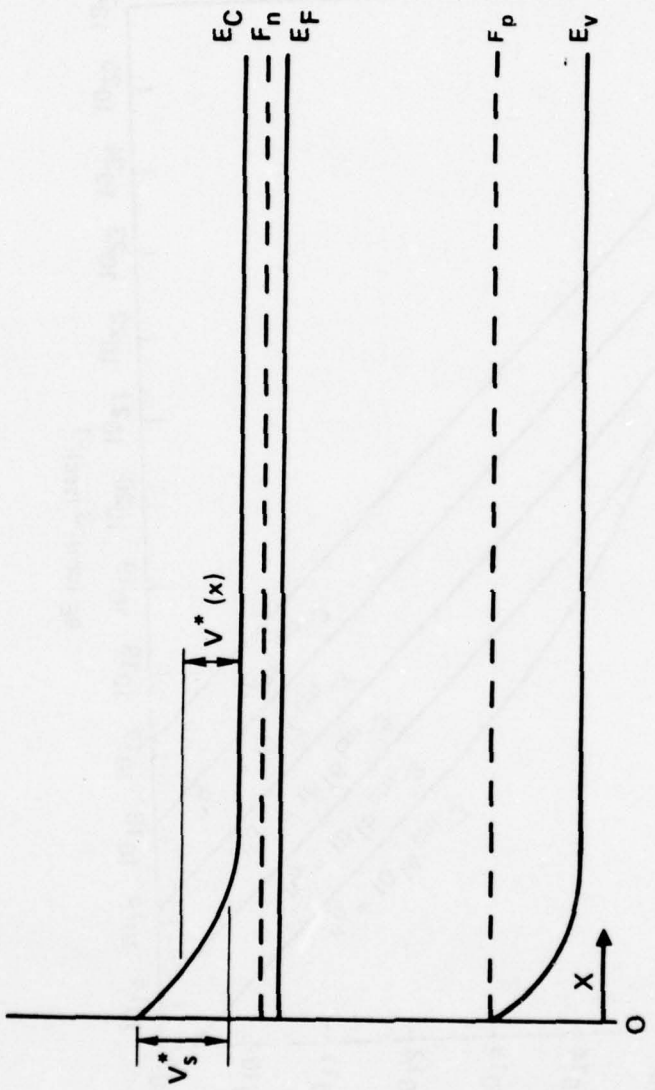


Figure 2.9 Energy band diagram of an n-type semiconductor with illumination; F_n and F_p are the quasi-Fermi levels for electrons and holes respectively.

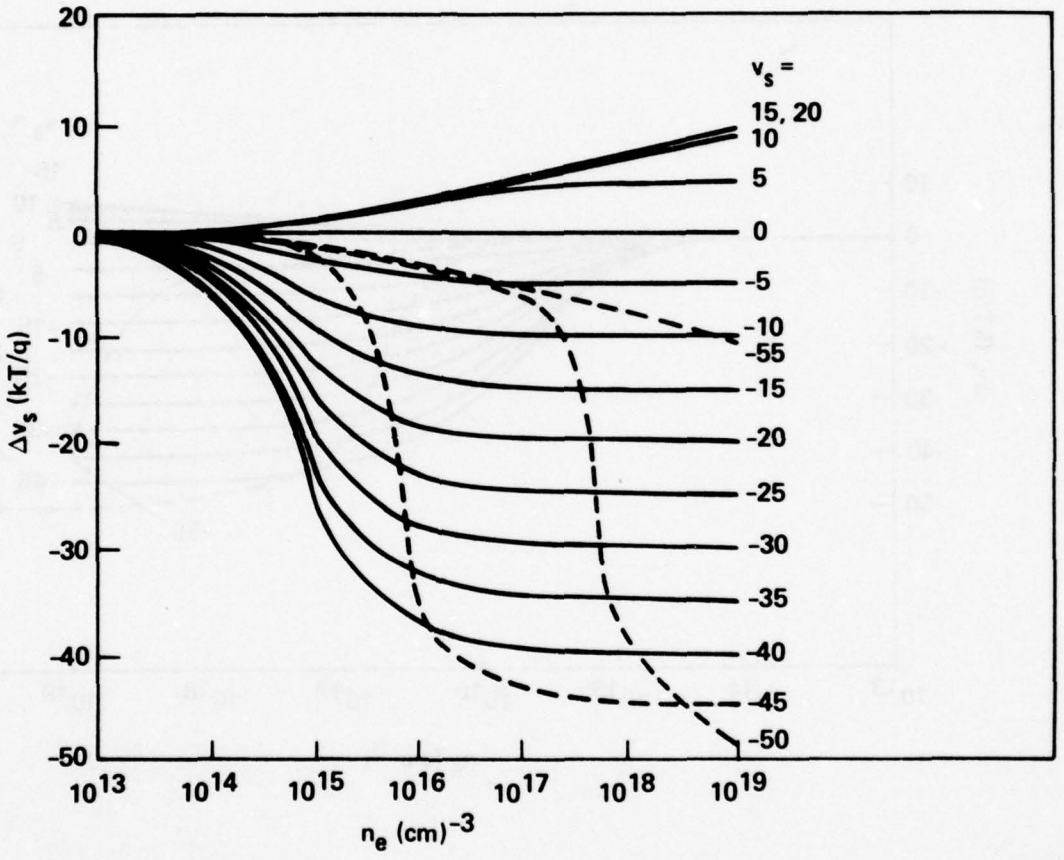


Figure 2.10 Surface photovoltage (Δv_S) vs excess carrier density for n = 10^{15} cm^{-3} GaAs at 300°K; v_s represents the surface potential in reduced units (kT/q) with no illumination; the dashed lines indicate that the surface is inverted for that value of surface potential.

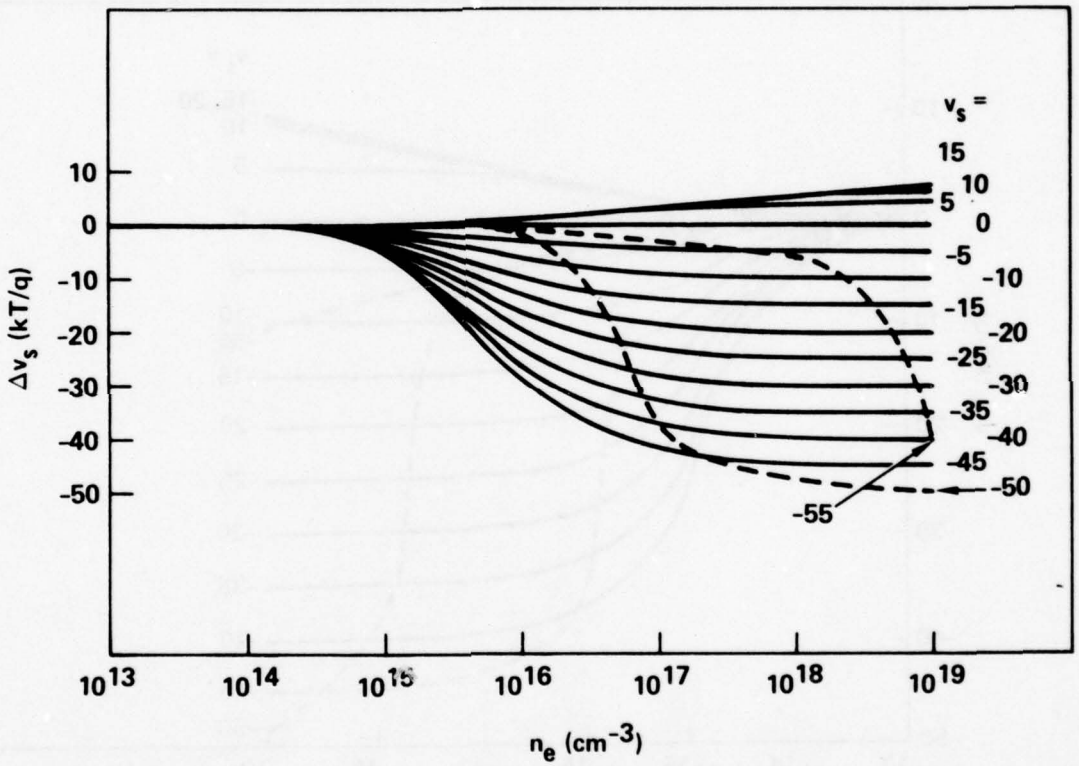


Figure 2.11 Surface photovoltage (Δv_s) vs excess carrier density for n = 10^{17} cm^{-3} GaAs at 300°K; v_s represents the surface potential in reduced units (kT/q) with no illumination; the dashed lines indicate that the surface is inverted for that value of surface potential.

CHAPTER 3

LITERATURE REVIEW

This review will discuss the published data relevant to the surface electrical properties of GaAs and InP. The basic models for treating the surface space charge region of a semiconductor have been most thoroughly tested on silicon, and a vast body of theoretical and experimental work exists on this material. The most recent comprehensive review paper on this subject by Goetzberger *et al*[1] contains a thorough discussion of the most recent data on silicon-silicon dioxide interfaces and a comprehensive bibliography of the MIS measurement technique. Literature is included in the present review only when it bears directly on the nature of the surface potential and surface carrier densities on samples which were measured outside the ultra-high vacuum system. This restriction is somewhat arbitrary but was made in the interest of keeping the subject manageable. Some justification for it can be made on the basis of concentrating on those surfaces which could reasonably be expected to exist in a technologically useful device. Therefore most of the work on surfaces prepared in ultra-high vacuum has been omitted. This includes much work on photoemission and contact potential difference measurements.

In the reported literature saturation of the C-V data with either positive or negative gate bias has been almost universally assumed to indicate the presence of either surface accumulation or inversion, depending, of course, on the carrier type of the material and the polarity of the gate bias. However, such interpretation of the data can lead to serious errors. In the following Chapter it should be remembered that when the words

accumulation and inversion are encountered, they are quoted from the work being cited.

3.1 Gallium Arsenide

The most intensively studied III-V semiconductor is GaAs. Many devices have been constructed from this material and its present and potential usefulness are largely responsible for ongoing investigations made on this material. The successful development of the Gunn diode, the junction LED and laser, and the Schottky barrier FET have all prompted an intensive effort on the growth and characterization of GaAs. Still lacking, however, is a consensus as to the nature of the surface of GaAs and the manner in which this surface is changed when it is coated with dielectric materials.

Gerlach[2] performed surface conductivity measurements on n-GaAs (0.16 Ω-cm) at room temperature using a metal gate electrode and an unnamed dielectric spacer placed on one side of the sample to induce surface potential changes in the semiconductor. He found a monotonically increasing surface conductivity as the voltage on the gate electrode of a sample etched in a $H_2SO_4/H_2O/H_2O_2$ (3:1:1) solution was increased from negative to positive. He interpreted this as evidence of strong accumulation but, of course, an alternate explanation would be a depletion layer of decreasing width as the gate voltage was increased. He did not observe a conductance minimum so was not able to obtain a determination of the surface potential. In a similar device which used mylar as a dielectric spacer and $HF/HNO_3/H_2O$ (1:3:2) for the etchant Pilkuhn[3] observed a minimum in conductance as the gate voltage was swept at ∿ 0.8 Hz. The total conductance change observed was 7×10^{-8} m /

when ideally the total change should have been $1x10^{-4}$ m / . This result indicates that the surface potential variations obtained were very small and the surface was pinned. Flinn and Briggs[4] performed surface photovoltage and conductance measurements on $\sim 3x10^{15}/cm^3$ n- and p-type single crystal GaAs in a configuration employing transparent metal gates and polythene dielectric spacers on both faces of a 0.02 cm-thick semiconducting filament. They observed that any DC voltage step applied to the field electrode produced a conductance change which decayed to zero in less than a second, and from this concluded that for sufficiently long times all of the induced-charge was trapped in surface states with a density greater than 10^{12} cm^{-2}. They were not able to obtain saturated photovoltage measurements on either n- or p-type material and concluded that for n-type material the zero bias surface potential, V_{so}, is < -0.5 V and on p-type material $V_{so} > 0.15$ V.

Hall and White[5] reported the first data on GaAs coated with a dielectric material. By pyrolytically-depositing silicon dioxide on GaAs at 730°C they were able to produce an MIS device whose capacitance could be changed by an applied gate voltage. They presented capacitance voltage data taken at a single frequency (1 MHz) and concluded therefrom that the surface state density was $\sim 1x10^{12}$ cm^{-2} eV^{-1} on both p- and n-type material and that the surface potential might be modulated over the full bandgap. This conclusion, of course, might have been more justifiable if the measurements had been taken at a number of frequencies in order to see if surface states were responding at the measurement frequency. Sato[6] has reported measurements taken on evaporated silicon monoxide and pyrolytically-deposited silicon dioxide (tetraethoxysilane process at 600-800°C) layers on $2x10^{16}/cm^3$ n-GaAs

substrates. The data he reported indicates however, the presence of a large leakage current through the dielectric layer; which precluded balancing the capacitance bridge for positive bias voltages. It is therefore difficult to draw conclusions from his data about the properties of the surface measured.

Foster and Swartz[7] constructed Si_3N_4-GaAs MIS devices by pyrolytically-depositing Si_3N_4 using a silane-ammonia process with deposition temperatures in the range 650-750°C. They report C-V measurements on $n = 4x10^{16}$ cm^{-3} and $p = 1.4x10^{17}$ cm^{-3} specimens in the frequency range from 5 kHz to 1.5 MHz. They observed monotonically decreasing curves as the frequency was increased up to 1.5 MHz indicative of a surface state density in the 10^{12}-10^{13} eV^{-1} range. They suggested that a frequency of 1.5 MHz was sufficiently high to "freeze out" the fast states but did not present any confirmatory experimental data. By the application of electric fields of $\sim 1.5x10^6$ V/cm they were able to obtain C-V curves on p-type material which they interpreted as the achievement of an accumulation layer. Electric field values of $2\text{-}3x10^6$ V/cm were necessary to reach flatband on the n-type samples.

Kern and White[8] measured the 1 MHz C-V characteristics of pyrolytically-deposited SiO_2 layers on n- and p-type GaAs substrates. Their data are impossible to analyze in a quantitative fashion because their C-V measurements do not accurately give the value of oxide capacitance, and also there is no way of determining whether their measurements were at a high enough frequency to prevent a response due to surface states.

Valahas *et al*[9] measured the photoconductance and surface photovoltage on n- and p-type GaAs prepared with a variety of surface treatments and employing semitransparent metal gates with mylar dielectric spacers on both sides of the sample. They were not able to obtain a surface conductance minimum so the surface potentials could not be determined. However, by measuring the decay in the photoconductive signal they estimated the capture cross-section for surface states to be 1×10^{-16} cm^2 for n-type material and 5×10^{-14} cm^2 for p-type material. They placed the energy position of this state at 0.70 eV below E_c in n-type material and 0.62 eV below E_c in p-type material. They obtained a positive photovoltage signal on n-type samples indicating a depleted surface but did not obtain saturation of the photovoltage. Cooper *et al*[10] attempted to construct a model for C-V and G-V data on pyrolytically-deposited Si_3N_4 on p-GaAs with not a great deal of success. Their data was all taken at 100 kHz; this frequency is not high enough to obtain high-frequency behavior and therefore they could not calculate the surface potential from their measurements.

Ito and Saki[11] reported the presence of an inversion layer on an MIS transistor constructed on a p-GaAs substrate using a two-layer dielectric of pyrolytically-deposited SiO_2 and Al_2O_3. Their data were taken on a curve tracer which was essentially a pulsed measurement. They derived a field effect mobility of the carriers of 2240 cm^2/V-sec.

Klose *et al*[12] investigated pyrolytically-deposited Si_3N_4 layers on n-GaAs by C-V and photocapacitance measurements. From C-V measurements at 10 MHz they infer a minimum surface state density of $\sim 2 \times 10^{12}$ cm^{-2} and the existence of both inversion and accumulation layers. Miyazaki *et al*[13]

formed MIS structures employing Al_2O_3 made by oxidation of tri-iso-butyl-aluminum at 450°C, Si_3N_4 made by ammonolysis of silane at 700°C, and SiO_2 formed by pyrolysis of tetraethoxysilane at 700°C and with a microwave glow discharge of tetraethoxysilane at 400°C. The surface state densities determined from C-V measurements at 1 MHz gave minimum values of $\sim 10^{11}$ cm^{-2} eV^{-1} for p-type samples on the best devices. They presented no evidence that 1 MHz was a high enough measurement frequency to justify application of the Terman analysis.

Hasegawa *et al*[14] were the first to report electrical measurements on the anodically-formed native oxide of GaAs. Anodization was done in a solution of 1 part 3% aqueous tartaric acid mixed with two to four parts of propylene glycol. For the MIS devices made on p-type material they reported minimum surface state densities of $2x10^{11}$ cm^{-2} eV^{-1} based on C-V measurements at 1 MHz and use of the Terman method in analyzing the data. Annealing at 300° for 6 hours was claimed to improve the properties of the interface by reducing the hysteresis and frequency dispersion in the C-V curves. They concluded from their data that both accumulation and inversion layers could be produced on p-type material.

Bayraktaroglu *et al*[15] reported FET structures using an anodized dielectric on a p-GaAs substrate. They concluded that the transistor action observed took place because of the existence of an inversion layer of electrons on the surface. Unfortunately they did not give the dimensions of the device structure so that the carrier mobility cannot be calculated, and the type of carrier (electron or hole) responsible for charge transport cannot be determined. Stannard *et al*[16] performed microwave magnetoconductance

measurements on anodized n-GaAs MOS capacitors in the attempt to measure the surface carrier mobilities. Their data seems inconclusive but was interpreted as indicating a carrier mobility of 100 $cm^2\ V^{-1}\ sec^{-1}$ in an accumulation layer of electrons. Shimano *et al*[17] applied the saturated photovoltage technique to the study of anodized n-GaAs MOS capacitors and reported a surface potential shift from -0.6 V to -0.2 V with the application of electric fields of $\sim \pm 10^6$ V/cm. This result implies that no accumulation of either electrons or holes was observed since $V_s > 0$ for electron accumulation and $V_s < -1.2$ V for hole accumulation.

A number of authors [18, 19, 20, 21, 22, 23, 24] have published results on GaAs MOS devices produced by forming the oxide layer anodically in an oxygen plasma discharge. The possible advantage of such a technique is the elimination of the electrolyte from the anodization process with the potential contamination resulting from its use. The interpretation of the electrical measurements on such devices is still open to controversy. Only Chang and co-workers claim results (attainment of accumulation and inversion and surface state densities $\sim 5 \times 10^{10}\ cm^{-2}$) which are significantly different from those obtained with aqueous anodization. Their conclusions are based on the measurement of the capacitance of MOS devices at a single frequency (1 MHz). Thus additional measurements over a wide frequency range need to be performed to bear out their conclusions. Bagratishvili *et al*[25] reported Ge_3N_4 layers deposited on n-GaAs substrates at 300-350°C. The Ge_3N_4 was formed by the nitridization of germanium with hydrazine vapor at 650°C. They constructed MIS capacitors and measured capacitance as a function of voltage from DC to 30 MHz.

However, their C-V measurements suggest that the surface potential of their MIS devices does not reach zero (flatband); the surfaces are always either depleted or (possibly) inverted.

Several other authors[26, 27, 28, 29, 30] have reported depletion mode MIS FETs using native oxides (both thermal and anodic) and deposited $Si_xO_yN_z$ dielectrics. Their data shows that the region under the gate electrode can be depleted of carriers when the devices were tested with a pulsed gate bias. The field effect mobilities quoted (1000-3000 $cm^2\ V^{-1}\ s^{-1}$) indicate that the conduction process is definitely due to the electrons. Zeisse *et al*[31] measured the frequency response of MIS capacitors on n-GaAs employing SiO_2, $Si_xO_yN_z$, and anodized dielectrics. They observed a frequency dispersion in the C-V curves all the way to 1 MHz and could not obtain the absolute value of surface potential. From the quasistatic data the range of surface potential variation was determined to be $\sim$ 25 kT (0.6 V). The surface state density was found to be 2×10^{12} to $10^{14}\ cm^{-2}\ eV^{-1}$.

Kohn and Hartnagel[32] have reported the temperature dependence and frequency dispersion of n- and p-type GaAs MOS capacitors. They observed a gradual flattening of the C-V curves with decreasing temperature; this follows the same trend as that observed if the frequency is raised. They concluded that this behavior was anomalous; however, a possible interpretation of their data is that the observed capacitance variation is due almost entirely to surface states and that the effect of lowering the temperature or raising the frequency is to "freeze out" or reduce the contribution of the surface states to the measured capacitance.

3.2 Indium Phosphide

Only very recently has InP substrate material of sufficient purity become available for the measurement of the surface properties. Wilmsen[33] reported I-V measurements and C-V measurements at 1 MHz on n-type InP MOS capacitors with dielectric layers formed by anodization in aqueous 0.1 N KOH and by rf-sputtering of SiO_2. The anodized layers were found to conduct a substantial amount of DC current while the sputtered layers pinned the surface potential (no field-effect modulation possible); therefore, a two-layer dielectric sandwich was used with the anodized layer next to the semiconductor. The C-V data indicated that the surface could be modulated from accumulation into depletion with a zero bias surface charge of -5×10^{11} e/cm^2 and a surface state density of $\sim 10^{11}$ cm^{-2} eV^{-1}. Lile and Collins[34] reported a somewhat improved electrolyte used for anodization which consisted of a 1% by weight solution of sodium salicylate in ethyl alcohol. This increased the dielectric resistivity to over 10^{13} Ω-cm. C-V measurements at 1 MHz again indicated that the surface could be modulated from accumulation into depletion. Messick[35] reported on pyrolytically-deposited SiO_2 layers formed at 300°C on n-InP substrates. Except for the fact that the dielectric resistivity was increased to $> 10^{15}$ Ω-cm and the breakdown strength was improved, his results were essentially the same as those of Lile and Collins.[34] Roberts *et al*[36] have reported I-V and C-V measurements on MIS capacitors using a dielectric formed by the deposition of successive monomolecular layers of either cadmium stearate or cadmium arachidate. Their results differ from those of earlier investigations in that they

observed the capacitance measured at 30 Hz to rise toward the value of the insulator capacitance with increasingly negative gate bias. This would indicate the presence of an inversion layer at the surface. Fritzsche[37] reported that the addition of HCℓ to the SiO_2 chemical vapor deposition process reduced the amount of charge trapping at low frequencies. In addition he reported C-V measurements with pulsed bias on n-InP samples, which allowed measurement of the deep depletion capacitance. This data allowed accurate determination of the impurity density directly under the capacitor plate and permitted calculation of a theoretical high frequency capacitance curve that could be compared with experiment. In this manner he concluded that the surface potential variation was restricted to $50\ mV > V_S > -600\ mV$ which implies that inversion was not reached on the n-type material.

3.3 References

1. A. Goetzberger, E. Klausmann and M. Schulz, CRC Critical Reviews in Solid-State Sciences, 6, 1(1976).
2. D. Gerlich, J. Appl. Phys., 33, 1815(1962).
3. M. H. Pilkuhn, J. Phys. Chem. Solids, 25, 141(1964).
4. I. Flinn and M. Briggs, Surf. Sci., 2, 136(1964).
5. R. Hall and J. P. White, Solid-State Electron., 8, 221(1965).
6. Y. Sato, Japan. J. Appl. Phys., 7, 595(1968).
7. J. E. Foster and J. M. Swartz, J. Electrochem. Soc., 117, 1410(1970).
8. W. Kern and J. P. White, RCA Review, 31, 771(1970).

9. T. M. Valahas, J. S. Sochanski, and H. C. Gatos, Surf. Sci., 26, 41(1971).

10. J. A. Cooper, E. R. Ward, and R. J. Schwartz, Solid-State Electron., 15, 1219(1972).

11. T. Ito and Y. Sakai, Solid-State Electron., 17, 751(1974).

12. H. Klose, Y. Maronchuk, and O. Senoshenko, Phys. Stat. Sol., (a) 21, 659(1974).

13. T. Miyazaki, N. Nakamura, A. Doi, and T. Tokuyama, Japan. J. Appl. Phys., Suppl. 2, Pt. 2, 441(1974).

14. H. Hasegawa, K. E. Forward, and H. L. Hartnegel, Appl. Phys. Lett., 12, 53(1976).

15. B. Bayraktaroglu, E. Kohn, and H. L. Hartnagel, Electron. Lett., 12, 53(1976).

16. J. L. Stannard, T. A. Kennedy, and B. D. McCombe, J. Vac. Sci. Technol., 13, 869(1976).

17. A. Shimano, A. Moritani, and J. Nakai, Japan. J. Appl. Phys., 15, 939(1976).

18. R. P. H. Chang and A. K. Sinha, Appl. Phys. Lett., 29, 57(1976).

19. R. L. Kauffman, L. C. Feldman, J. M. Poate, and R. P. H. Chang, Appl. Phys. Lett., 30, 319(1977).

20. C. C. Chang, R. P. H. Chang, and S. P. Musarka, J. Electrochem. Soc., 125, 481(1978).

21. R. P. H. Chang and J. J. Coleman, Appl. Phys. Lett., 32, 332(1978).

22. K. Yamasaki and T. Sugano, Proceedings of the 9th Conference on Solid State Devices, Tokyo, 1977.

23. F. Koshiga and T. Sugano, to be published in Thin Solid Films, Jan. 1979.

24. D. Fritzsche and G. Weimann, 2nd Symposium on Solid State Device Technology, March 8-10, 1977, Munster, German Federal Republic.

25. G. D. Bagratishvili, R. B. Dzhanelidze, N. I. Kurdiani, and O. V. Saksaganskii, Phys. Stat. Sol., (a) 36, 73(1976).

26. D. L. Lile, A. R. Clawson, and D. A. Collins, Appl. Phys. Lett., 29, 207(1976).

27. L. Messick, J. Appl. Phys., 47, 5474(1976).

28. A. Colquhoun, E. Kohn, and H. Hartnagel, IEEE Trans. on Electron Devices, ED-25, 375(1978).

29. H. Takagi, G. Kano, and I. Teramoto, IEEE Trans. on Electron Devices ED-25, 551(1978).

30. D. L. Lile, D. A. Collins, L. Messick, and A. R. Clawson, Appl. Phys. Lett., 32, 247(1978).

31. C. R. Zeisse, L. J. Messick, and D. L. Lile, J. Vac. Sci. Technol., 14, 957(1977).

32. E. Kohn and H. L. Hartnagel, Solid-State Electron., 21, 409(1978).

33. C. W. Wilmsen, CRC Critical Reviews in Solid State Sciences, 5, 313(1975).

34. D. L. Lile and D. A. Collins, Appl. Phys. Lett., 28, 554(1976).

35. L. Messick, J. Appl. Phys., 47, 4949(1976).

36. G. G. Roberts, K. P. Pande, and W. A. Barlow, Electron. Lett., 13, 581(1977).

37. D. Fritzsche, Electron. Lett., 14, 51(1978).

CHAPTER 4

EXPERIMENTAL PROCEDURE

The information provided in Chapter 3 indicates clearly the state of confusion prevailing at this time about the nature of the semiconductor-dielectric interfaces of GaAs and InP, particularly the surface potential and interface state densities of MIS structures. The experimental investigations described in Chapters 4 and 5 were made to provide information on these fundamental properties.

4.1 Sample Preparation

Three different techniques have been used to prepare the dielectric layers employed in this investigation. Two of the processes, sputtering and pyrolysis, produced deposited layers, and the third, anodization, produced a grown oxide layer on the GaAs substrates.

4.1.1 Sputtering

The apparatus used for fabricating the sputtered silicon oxide layers is shown schematically in Fig. 4.1. A neutralized ion beam was produced by a 10-cm diameter Kaufman-type source.[1] A bell jar pressure of 3×10^{-4} torr argon was required to sustain the discharge. The beam energy could be varied from 100 to 800 eV/ion with current densities from 0 to 2 mA/cm^2. The GaAs substrates used were Si-doped wafers ($n = 1 \times 10^{18}$ cm^{-3}) with either <100> or <111> orientation which were mounted on a moveable platform to facilitate predeposition cleaning. In position A (Fig. 4.1), the beam incident on the quartz target sputtered away its top layer in the pre-cleaning step; these sputtered particles were shielded from the substrate. In position B, the substrate was cleaned using a reduced energy ion beam

(100 eV, 0.2 mA/cm^2) for about 5 min. being mindful of possible sputter damage discussed below. Actual sputter deposition of silicon oxide took place in position C; the angles and positions of the substrate were designed to provide reasonably uniform coverage while keeping the substrate out of the incident ion beam path. Using 500 eV argon ions with a density of 1 mA/cm^2, the deposition rate was 30 Å/min. Means were provided for heating the substrates, however doing so generally produced inferior results.

The adherence and abrasion resistance of the SiO_x films was very good as long as the substrates were sputter-etched prior to the dielectric deposition. If the deposition was performed directly on a chemically-etched GaAs substrate, the adhesion was poor. Similar results were obtained when very low (<50 ev) ion energies were used during cleaning. A deleterious result of the use of the ion beam for substrate cleaning was the increased surface damage produced by progressively larger ion energies. With an incident ion energy of 300 eV sufficient surface damage was produced that no modulation of the space charge capacitance could be observed.

The dielectric layers prepared initially, using the 10 cm diameter ion source, were conductive (resistivity 10^{10} - 10^{12} Ω cm); a second generation sputtering system was constructed using a 2.5 cm diameter source and employing all quartz fixtures for mounting the target and substrate because it had been assumed that stray argon ions were sputtering metallic atoms off the stainless steel fixtures and introducing metallic impurities into the deposited layers. This has not been demonstrated causally; however, layers deposited in the redesigned sputtering system typically had resistivities in the 10^{14} - 10^{16} Ω cm range.

Sputtered silicon nitride layers were formed by reactive sputtering of a 99.999% pure polycrystalline silicon target in Linde UHP argon and nitrogen using the 2.5 cm diameter source. The best results were obtained when the gallium arsenide substrates were sputter-cleaned using nitrogen ions in the 80 - 200 eV energy range prior to deposition of the silicon nitride. The accelerating potential used during deposition was 500 V with an ion current density of 1 mA/cm^2. The partial pressures during deposition were $1x10^{-4}$ of argon and $3x10^{-4}$ torr of nitrogen. A background pressure of at least $3x10^{-4}$ torr nitrogen was necessary in order to get high resistivity layers. The sputtering rate was, of course, reduced when nitrogen was introduced into the vacuum system, and a partial pressure of $1x10^{-4}$ torr argon was required in order to obtain deposits. This is accounted for by the reduced mass of the nitrogen atoms which reduced the sputtering yield.[2] The vacuum system was equipped with a liquid nitrogen cold trap and the background pressure was $5x10^{-7}$ torr.

Post-deposition annealing of the sputtered silicon nitride dielectrics did not improve their electrical properties. Auger electron spectroscopy (AES) of the silicon nitride layers revealed that oxygen contamination was present in all the layers studied. A typical spectrum is shown in Fig. 4.2 which was obtained after sputter etching for 3 minutes in xenon at 1 KV with a current density of 100 $\mu A/cm^2$. The oxygen definitely appears to be in the silicon nitride layers and is not just the adsorbed surface oxygen. Also there is an increased concentration of oxygen near the GaAs surface.

4.1.2 Anodization

The anodized oxides were formed at room temperature using low current anodization (8 $\mu A/cm^2$) in an 0.03 M aqueous solution of ammonium dihydrogen phosphate ($NH_4H_2PO_4$). Anodization was performed at constant current up to the maximum voltage. The sample was then taken out of the bath, washed in 18 MΩ resistivity water, and dried in air at room temperature. A variety of pre-anodization cleaning procedures were tried but none seemed to affect the electrical properties of the completed devices. It was necessary to use a neoprene O-ring seal between the top surface of the substrate and the anodizing bath in order to prevent the electrolyte from reaching either the edges or back of the sample. Imperfections in the crystal surface such as scratches or imperfectly cleaved edges short-out the growing anodic layer in much the same manner as they would short-out a p-n junction. In order to do the anodization at low current densities these imperfections were insulated from the electrolyte.

The anodic oxides were annealed at 400°C for 20 minutes in a mixture of 10% hydrogen and 90% helium prior to making any measurements. When this step was omitted, the devices exhibited such a large amount of short term drift and hysteresis in the C-V characteristics that no analysis of the data was possible.

4.1.3 Pyrolysis

The dielectrics formed by chemical vapor deposition (SiO_2, Si_3N_4) were deposited in a water-cooled quartz reactor through which passed a mixture consisting of 0.016% SiH_4, 0.32% O_2 and 99.52% N_2 at 300°C for the SiO_2 deposition and 0.1% SiH_4, 1.5% NH_3 and 98.4% N_2 at 600°C for the

Si_3N_4 deposition.[3,4] The gases were mixed in a stainless steel chamber prior to entering the reactor, and the substrate was placed on a graphite block in which a heater and a thermocouple had been placed for temperature control.

4.1.4 Sample Contacts

The ohmic contact to the n-GaAs was made by first evaporating a 2000Å layer of gold-germanium (88%-12%) eutectic on the back side of the sample and following this with an evaporation of 1000Å of nickel. Annealing of this contact at 425°C for 2 minutes in a gas mixture of 95% N_2 - 5% H_2 was sufficient to form a low resistance contact. Contacts for the sputtered samples were formed prior to film deposition since high temperature annealing seemed to degrade the sputtered layers. The contacts on the anodized and pyrolytically-deposited layers were deposited after the dielectric formation. Contacts to the p-type GaAs samples were prepared by soldering an alloy of 80% In - 20% Cd to the wafer and annealing in the same manner as for the n-type material.

Ohmic contact to n-type InP may be made with indium solder - no annealing is required. Preparation of contacts to p-type material is considerably more difficult. Nothing that was tried produced a truly low resistance ohmic contact. A low temperature silver solder consisting of 5% Ag, 16.6% Zn, and 78.4% Cd reproducibly gave ohmic contacts although they did not have a particularly low resistance. In general, the contact resistance continued to decrease as the annealing time and temperature were increased. However, the surfaces of the InP substrates suffered from thermal degradation at temperatures much above 400°C. A typical

treatment was at 300°C for 10 minutes in a gas mixture of 95% N_2 - 5% H_2. The metal gate contacts were formed by evaporating aluminum through a metal mask.

Contacts to the gate electrode were made using conductive epoxy (Dupont 5504A) and 0.001-inch diameter gold wire. At measurement frequencies above 1 MHz, this wire was kept short ($\sim$ 2 mm) to minimize the series inductance. Samples for the high frequency measurements had back contacts made by soldering the device with indium to a silver ribbon 0.005-inch thick and 1 mm wide. It was generally necessary to thin the devices to $\sim$ 125 μm or less to reduce the series resistance when making measurements above 1 MHz. This was done by mounting the sample on a stainless-steel polishing jig and grinding with a 5 μm alumina slurry on a plate-glass polishing lap.

4.2 Measurement Techniques

4.2.1 Quasistatic Capacitance Measurement

The most satisfactory method of obtaining low frequency capacitance data is the quasistatic or linear ramp technique devised by Kuhn.[5] In the circuit shown in Fig. 4.3, a linear voltage ramp (usually the output of a triangular waveform generator) is applied to the gate of an MOS device whose back contact is connected to the input of a high impedance operational amplifier (Princeton Applied Research Model 135 electrometer). The output of the amplifier is

$$V_o(t) = - RC \frac{dV}{dt} \tag{4.1}$$

which for a linearly-changing input signal is

$$V_o = \mp \alpha RC \tag{4.2}$$

The amplifier and X-Y recorder used to plot the data were calibrated with a standard capacitor prior to each measurement and a plot of capacitance vs. voltage was obtained directly. The theory for obtaining the surface state density of an MOS device from a low frequency capacitance measurement developed by Berglund[6] holds only if the surface states which respond at the bias sweep rate also respond to the capacitance measurement frequency. In practice it is difficult to make AC capacitance measurements at frequencies much lower than $\sim$ 5 Hz, and the quasistatic method neatly avoids this problem by sweeping the bias voltage and making the capacitance measurement at the same frequency. Typically the measurements reported herein were made with a sweep rate of 100 mV/sec.

4.2.2 Small Signal Capacitance

The small signal differential capacitance measurements with swept bias were made using a PAR Model 124 lock-in amplifier in conjunction with a PAR Model 181 current amplifier. This circuit, shown in Fig. 4.4 was used to measure the small signal parameters in the frequency region from 10 to 10^5 Hz. The lock-in amplifier has an internal oscillator with an adjustable output, and this was used as the voltage generator. Measurements could easily be made with the lock-in amplifier using a 10 mV rms signal on the MIS device. This was determined to be in the linear region of small signal behavior, and the same signal level was used at all frequencies. The PAR 124 amplifier rejected the essentially static voltage provided by the ramp generator so that the lock-in output was proportional to only the sinusoidal current through the MIS device.

Measurements in the frequency range 10 - 10^5 Hz were sometimes made using a General Radio (GR) Model 1621 capacitance bridge. This was used because some devices were too conductive to permit measurement with the lock-in amplifier system and also for calibration of the other measuring instruments. Measurements with the bridge could be accurately made only when the applied voltage at the device was at least 50 mV, and this level was used at all frequencies.

Measurements at 1 MHz were made using a Boonton Model 72BD capacitance meter which applies a 3 mV rms signal to the device under test. Above this frequency the devices were mounted on a stripline jig and measured with a GR Model 1602-B UHF admittance meter. The stripline circuit was constructed from a ceramic wafer[7] which had been precoated with a layer of chromium followed by a layer of gold. The pattern, shown in Fig. 4.5 was etched in the conductor on one side of the wafer. The line width was chosen such that a 50 Ω line impedance was maintained to the device under test and additional bonding pads were formed on the conductor for connection of a ceramic chip coupling capacitor and bias resistor. A schematic diagram of the completed circuit is shown in Fig. 4.6. The measurements with the admittance meter were corrected for the error caused by the finite length of transmission line between the meter and device. This correction is given by

$$Y_D = Y_o \frac{G_m + j(B_m - Y_o \tan \beta d)}{(Y_o + B_m \tan \beta d) - jG_m \tan \beta d} \qquad (4.3)$$

where Y_D is the admittance of the MIS device, Y_o is the characteristic line impedance (in this case 0.02 mho), G_m is the measured conductance, B_m is the measured susceptance, and βd is the length of the transmission line

between the meter and the device, given as a fraction of a wavelength. In practice the line length was determined electrically by leaving an open circuit on the end of the test jig (so that $Y_D = 0$) and measuring G_m and B_m. It can be seen from Eq. (4.3) that a solution is obtained only when

$$G_m = 0 \tag{4.4}$$

and

$$\beta d = \tan^{-1}(B_m/Y_o) \tag{4.5}$$

The device admittance determined in the aforementioned manner was modeled by a series resistance-capacitance circuit and this value of capacitance is claimed to be the device capacitance.

As evidence that this is actually the case, in Fig. 4.7 are presented C-V data which were taken on a gold-GaAs Schottky diode. Measurements at 10 Hz, 1 MHz, and 150 MHz are seen to be in excellent agreement and lend credence to the supposition that the capacitance was being measured accurately by the different procedures.

4.2.3 Surface Photovoltage Measurements

The basic technique used in making the photovoltage measurements was to keep the sample in the dark most of the time and allow light to strike it for only very short periods. An Ithaco Model 382A light beam chopper was modified to give a 1% duty cycle and was used with repetition rates from 1 - 60 Hz. The incident radiation was supplied from either a 4 mW He-Ne laser (6320Å) or a high pressure mercury-xenon arc lamp.

MIS samples were prepared with 200 Å-thick semitransparent nickel gates on top of the dielectric. A small area contact to the nickel gate was made with 0.001-inch diameter gold wire and conductive epoxy. Ohmic contact to

the GaAs samples was made using the Au-Ge-Ni recipe previously described while contact to the n-type InP samples was made with indium solder.

A problem encountered in these measurements was finding a high impedance preamplifier which would permit variation of the DC voltage across the MIS sample. The sample-amplifier configuration forms an RC circuit whose time constant must be larger than the time required for the sample to reach equilibrium after application of a light pulse. Since the capacitance of the test device was of the order 100 pF this required an amplifier with an input impedance of $\sim 10^8\ \Omega$. The circuit shown in Fig. 4.8 was constructed to have an input resistance of $\sim 10^8\ \Omega$ and an input capacitance of ~ 3 pF. The static current through the MIS device was measured with an electrometer to insure that the voltage drop across the bias resistor was negligible.

The MIS device, in a photovoltage measurement, can be represented by a voltage generator in series with the oxide capacitance. The voltage within the MIS device is therefore attenuated at the amplifier input terminals by any input capacitance of the amplifier. This error was corrected by calibrating the preamplifier circuit for each device that was measured. First the oxide capacitance was determined and then a square-wave generator in series with a fixed capacitor of the same value as the oxide capacitance was connected across the input terminals of the amplifier. The gain of the amplifier was then adjusted to give output pulses with peak heights equal to the pulse heights supplied by the signal generator. A PAR 160 boxcar integrator was used as a sample and hold circuit to measure the peak pulse height from the preamplifier and the output was displayed as a function of bias voltage on an X-Y recorder.

4.3 References

1. P. D. Reader and H. R. Kaufman, J. Vac. Sci. Technol., 12, 1344(1975).
2. L. I. Maissel and R. Gland, Handbook of Thin Film Technology, McGraw Hill, 1970.
3. L. Messick, J. Appl. Phys., 47, 5474(1976).
4. L. Messick, J. Appl. Phys., 47, 4949(1976).
5. M. Kuhn, Solid-State Electron., 13, 873(1970).
6. C. N. Berglund, IEEE Trans. on Electron Devices, ED-13, 701(1966).
7. Tek-Wave Inc., 3 Delaware Dr., New Hyde Park, N.Y. 11040, Model 15-2513-1210.

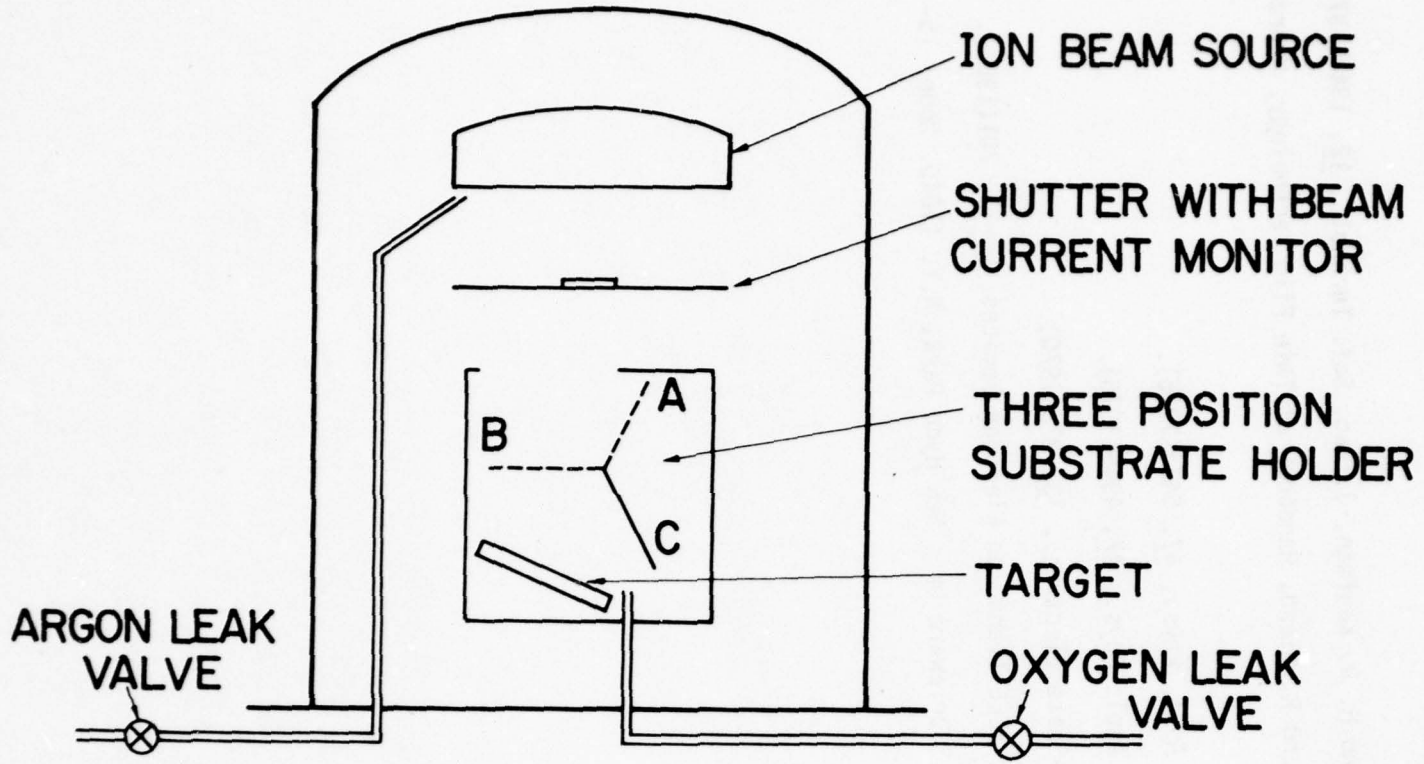


Figure 4.1 Ion beam sputtering system

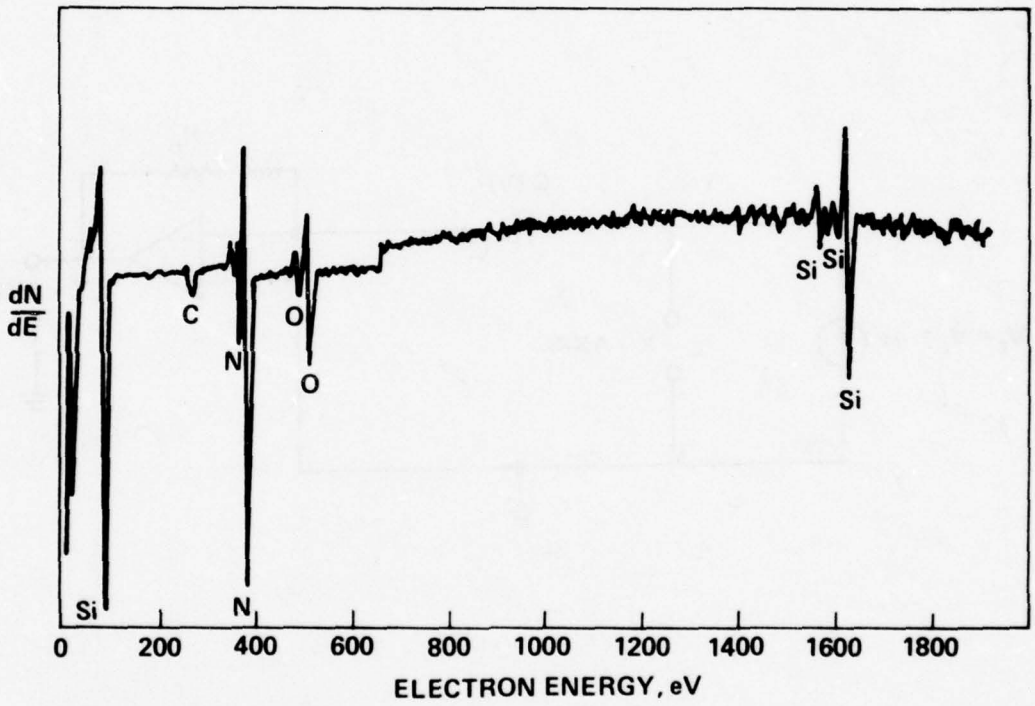


Figure 4.2 Auger electron spectrum of sputtered silicon nitride layer

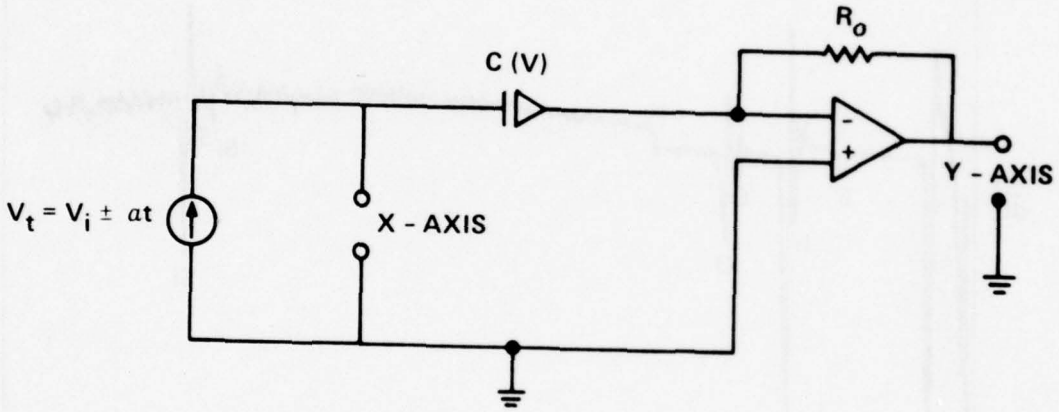


Figure 4.3 Quasistatic capacitance measurement circuit

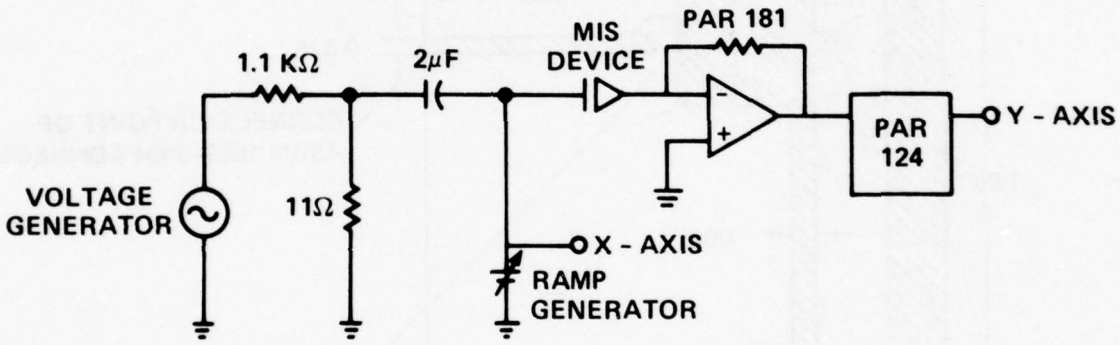


Figure 4.4 Small signal capacitance measuring circuit

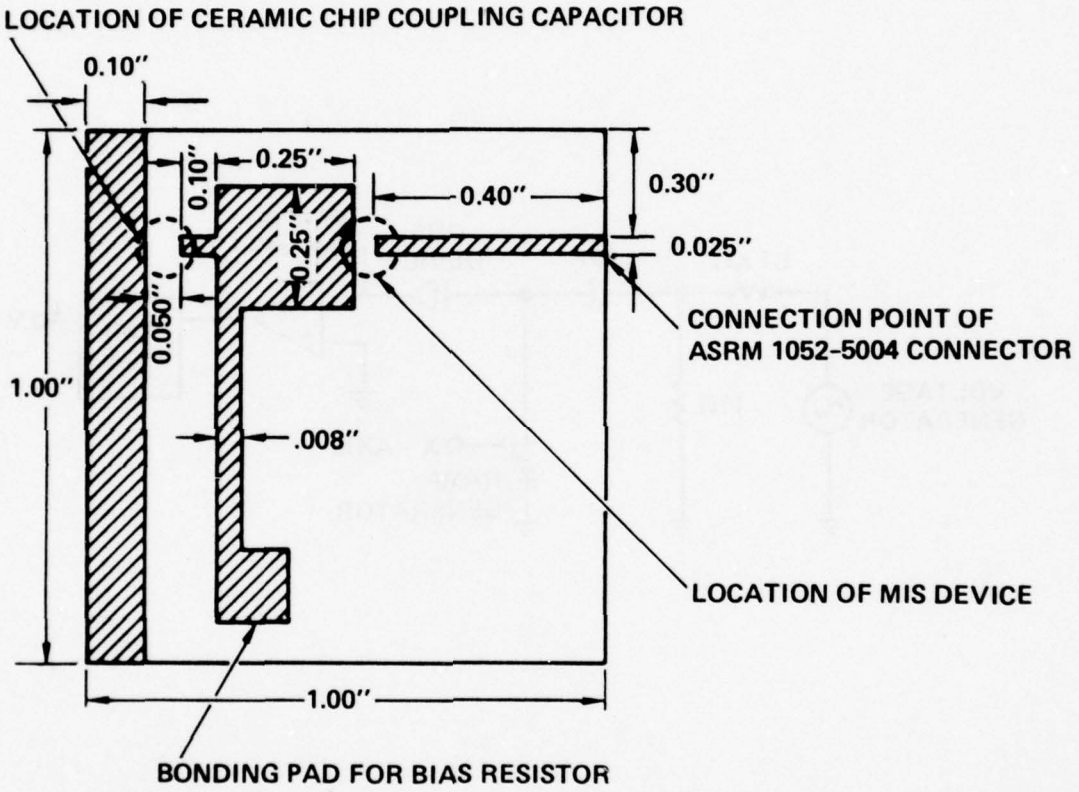


Figure 4.5 Stripline jig

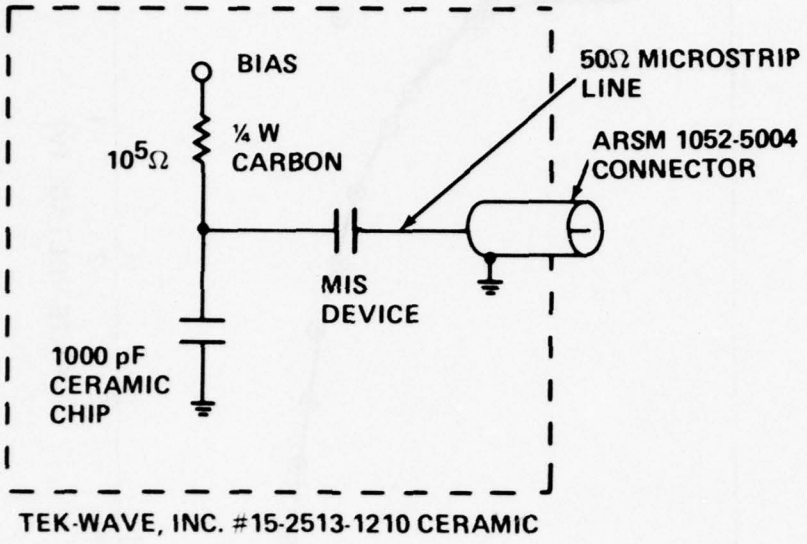


Figure 4.6 Schematic diagram of stripline circuit

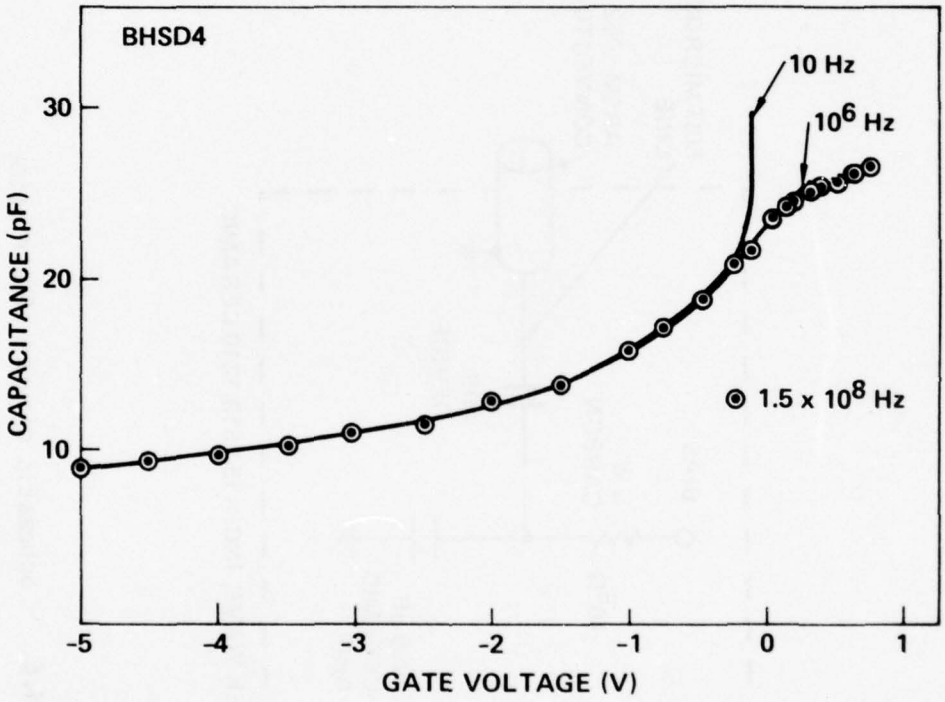


Figure 4.7 C-V measurements from 10 Hz to 150 MHz on a GaAs Schottky diode

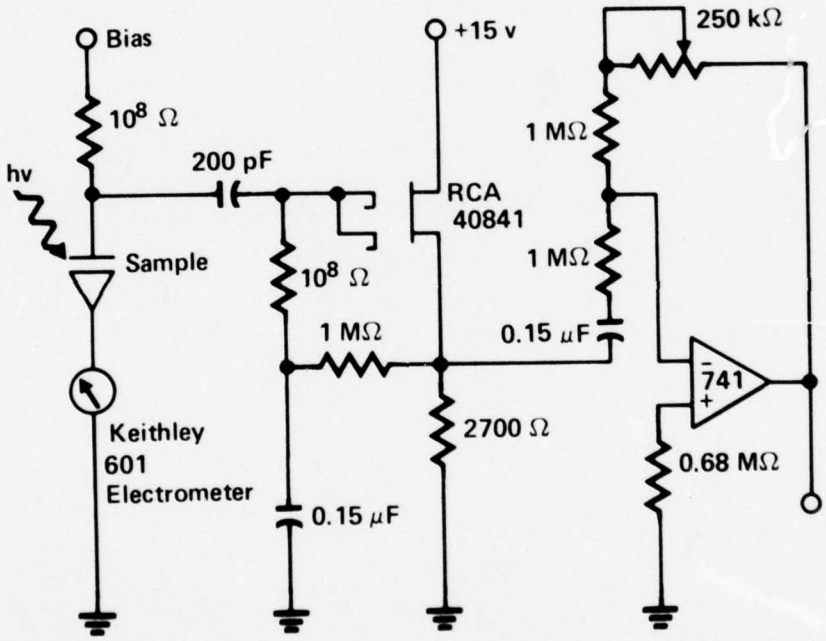


Figure 4.8 Circuit for surface photovoltage measurement

CHAPTER 5

DATA AND ANALYSIS

In this Chapter the results of the electrical measurements and the surface photovoltage measurements are presented for the various dielectric layers investigated experimentally on GaAs and InP. The data are presented in chronological order so that the reader can follow the arguments that have led to the present understanding of the nature of these surfaces.

5.1 C-V Measurements on n-type GaAs

Preliminary data obtained on the sputtered SiO_2 and Si_3N_4 dielectric MIS structures were taken at a measurement frequency of 1 MHz on a Boonton 72B capacitance meter. This somewhat arbitrary choice of frequency has been made in several capacitance measuring instruments in response to a need to do routine C-V measurements on silicon MOS devices. It is an often confirmed experimental observation that the surface states present on high-quality thermally-oxidized Si-SiO_2 interfaces cannot follow (do not respond to) frequencies of the order of 1 MHz or higher.

Figure 5.1 is a plot of the C-V measurement on an Al-silicon oxide - GaAs MIS structure with the dielectric formed by sputtering quartz using the 10 cm diameter ion beam source. Hall measurements made on the semiconducting material indicated a carrier concentration of 1.1×10^{18} cm^{-3}. The C-V curve exhibits the characteristic shape of a high-frequency measurement on an n-type Si-SiO_2 device. However, if the capacitance (with 15 V bias) is taken to be the oxide capacitance and the capacitance with -15 V bias is taken to be the high-frequency minimum capacitance, then the calculation of the minimum space charge capacitance from Eq. (2.23) and determination of

the carrier concentration from Eq. (2.22) yields a value of 2.5×10^{17} cm^{-3} for the carrier density in disagreement with the Hall value. The current voltage measurements on the same device are shown in Fig. 5.2 and indicate a large current (for an MIS device) with both forward and reverse voltages on the gate. The current which flows with reverse bias may prevent the inversion layer from forming in the same manner as in the Schottky barrier device discussed in Chapter 2. If it does, then the high-frequency capacitance curve would never saturate at a minimum value but would continue to decrease with increasing negative voltage as shown in Fig. 2.5. This lack of saturation was assumed to be the reason for the large discrepancy in the values of carrier concentration obtained from Hall measurements and from C-V measurements.

A typical C-V curve taken at 1 MHz on a device constructed using a sputtered silicon nitride dielectric layer on n-GaAs is shown in Fig. 5.3. Calculation of the substrate carrier concentration using the C-V data and the capacitance minimum yields a value of 1.55×10^{16} cm^{-3} compared with the value of 1.18×10^{16} cm^{-3} obtained from the Hall measurements. If this data is taken to represent a high-frequency curve (i.e., surface states no longer respond to the measurement frequency), then the semiconductor reaches the flatband condition with approximately 13 V bias and larger voltages produce an increasingly accumulated surface.

A number of silicon nitride on n-GaAs samples were prepared under different sputtering conditions and the samples were routinely evaluated using the 1 MHz C-V measurement. By introducing substrate bias and using various sample cleaning procedures it was possible to obtain C-V data in

which it appeared that the polarity and magnitude of the charge stored at the insulator-semiconductor interface could be altered. However, judging from the C-V data the surface properties were not improved.

5.1.1 Quasistatic and 1 MHz C-V Measurements

Subsequently it became possible to make the C-V measurements using the quasistatic technique and the lock-in amplifier. Some of the first data taken on a sputtered sample are shown in Fig. 5.4. In it are data taken at 1 kHz and 10 kHz in addition to 1 MHz data. Several troubling questions immediately arose. It seemed that by choosing a specific measurement frequency almost any type of C-V curve desired could be obtained. An apparent inconsistency was the almost flat curve obtained at low frequency and the large capacitance variation seen in the 1 MHz curve. A Berglund analysis of the low-frequency curve (i.e., integration of the area between the value of oxide capacitance and the C-V curve to obtain the change in surface potential) would indicate a negligible change in surface potential with gate bias changes of ± 15 V. Since the 1 MHz data indicates a change in surface potential of almost 1 V, these two sets of data would be inconsistent if the 1 MHz data were truly at a frequency such that surface states no longer responded.

5.1.2 High-Frequency C-V Measurements

In order to determine the upper limit of the frequency response it became necessary to measure the C-V characteristics at significantly higher frequencies, and the circuit, shown in Fig. 4.5, using microstripline was constructed. The first MIS device on which the high-frequency measurements were made utilized an anodized dielectric. This

was motivated, in part, by the high leakage of the sputtered dielectrics which prevented useful quasistatic measurements, and an analytical cross-check of the high- and low-frequency experimental measurements was desired. The measurements taken over the full frequency range are shown in Fig. 5.5.

The surface potential vs. gate-voltage relationship, shown in Table 5.1, was obtained from the quasistatic C-V curve assuming that the surface reaches inversion with -10 V gate bias. The high-frequency data was analyzed by taking the maximum value of the capacitance measured at 100 Hz with the room lights on as the oxide capacitance and the minimum value of capacitance measured at 150 MHz as the high-frequency minimum. The minimum space charge capacitance was calculated from Eq. (2.23) and the carrier concentration was obtained from Eq. (2.22). Using these parameters the high-frequency device capacitance was calculated as a function of surface potential using Eq. (2.16) and the capacitance values were plotted in Fig. 5.5 using the gate voltage vs. surface potential relationship obtained from the quasistatic data. Reasonably good agreement is obtained between the experimental and calculated high-frequency curves indicating that the quasistatic and high-frequency data are substantially in agreement. The total surface potential excursion indicated is approximately 16 kT/q (0.41 V).

Subsequently the same measurements were performed on a pyrolytically-deposited silicon nitride dielectric on GaAs and on a sputtered silicon nitride layer and the data are shown in Figs. 5.6 and 5.7. The data are qualitatively similar for all three samples. The only significant difference lies in the frequency response in the intermediate ranges. It can be seen that for the two silicon nitride-GaAs interfaces the surface states are responding at 1 MHz.

Table 5.1

Surface potential vs. gate bias for anodized n-GaAs.

V_v(v)	C_m(pF)	v_s(kT/q)
-8	152.3	-50
-7	152.3	-50
-6	152.3	-50
-5	150.3	-49.75
-4	148.3	-48.98
-3	143.0	-47.30
-2	145.5	-45.25
-1	146.8	-43.70
0	147.0	-42.35
1	147.5	-41.05
2	147.5	-39.83
3	147.5	-38.62
4	146.8	-37.31
5	148.0	-36.07
6	149.0	-35.11
7	150.5	-34.46
8	151.0	-34.07
9	151.8	-33.84
10	152.0	-33.74

5.1.3 Comparison of Surface State Model with Experiment

A physical model for the surface state capacitance has been developed by Nicollian and Goetzberger[1] based on the concept of discrete interfacial energy states located within the fundamental bandgap of a semiconductor. The probability of electron or hole capture in these states can be represented by either a capture probability, (C_n, C_p), or a capture cross-section, (σ_n, σ_p). These quantities are related by the expression

$$C_{n,p} = \bar{v}\sigma_{n,p} \tag{5.1}$$

where $\bar{v}$ is the average thermal speed of the mobile carriers ($\bar{v} \sim 10^7$ cm/S at room temperature). For a continuous distribution of energy states (N_{ss}) they expressed the surface state admittance as

$$Y_{ss} = G_{ss} + j\omega C_{ss} = q\frac{N_{ss}}{2\tau}\ln(1+\omega^2\tau^2) + jq\frac{N_{ss}}{\tau}\arctan(\omega\tau) \tag{5.2}$$

where $\tau = 1/C_n n_{so}$; n_{so} is the surface electron concentration ($n_{so} = n_B e^{qV_s/kT}$). Therefore $C_{ss} = q\frac{N_{ss}}{\omega\tau}\arctan(\omega\tau)$. Since all the quantities in this equation except C_n are either known or can be estimated; the capture probability of the interface states can be evaluated:

$$C_n = \frac{\omega C_{ss}}{qN_{ss}\, n_{so}\arctan(\omega\tau)} \tag{5.3}$$

For this example the capacitance measured at 10^4 Hz with 10 V bias for the device of Fig. 5.5 will be used. N_{ss} was obtained from the quasistatic measurement and was determined to be 1.13×10^{14} cm^{-2} eV^{-1}. For the moment it will be assumed that $\omega\tau$ is large so that $\arctan(\omega\tau) \simeq 1.57$. The surface state capacitance can be calculated from the expression

$$C_{ss} = (1/C_T - 1/C_i)^{-1} - C_D \tag{5.4}$$

where C_D is obtained from the measurement at 150 MHz. Using the values C_i = 146 pF, C(150 MHz, 10 V) = 47.5 pF, C(10^4 Hz, 10 V) = 137 pF, and V_S = -0.87 V

$$C_D = (1/47.5 - 1/146)^{-1} = 70.41 \text{ pF} \tag{5.5}$$

$$C_{ss}(10^4 \text{ Hz}, 10 \text{ V}) = 21.52 \text{ pF} \tag{5.6}$$

The result is that $C_n = 1.60\text{x}10^{-4}$ m^3 s^{-1} and that $\sigma_n = 1.60\text{x}10^{-5}$ cm^2. The expression arctan ($\omega\tau$) is therefore equal to 1.42 so that the original estimate of 1.57 is close enough. This calculation gives an enormous value for the capture cross-section (σ_n). By comparison Nicollian and Goetzberger obtained values from 10^{-15} - 10^{-16} cm^2 on silicon MIS devices. One might be able to explain away a factor of 10 difference for the two different materials but a factor of 10^{10} clearly suggests an error in the selection of the parameter values in Eq. (5.2). The term most likely to be in error is the surface carrier concentration that was calculated using the value of surface potential obtained from Table 5.1. Since n_{so} varies exponentially with the surface potential a relatively small error in V_S could lead to a very large error in n_{so}. It will be recalled from Eq. (2.37) that analysis of the quasistatic data yields the surface potential only to within an additive constant. The constant must be determined from an absolute evaluation of the surface potential for at least one value of gate voltage or by an accurate determination of the semiconductor impurity doping level. The value of the constant used for Table 5.1 was obtained by assuming that the device was inverted with -10 V gate bias. This choice was made because

of the saturation of the capacitance with negative gate bias in a manner very similar to the ideal theoretical curve shown in Fig. 2.5.

Two possible means for determining the surface potential are the saturated photovoltage measurement discussed in Section 2.4 and deep-depletion capacitance measurements as discussed in Section 2.1. Experimental photovoltage results on InP and GaAs will be discussed subsequently.

5.1.4 Impurity Density from Deep-Depletion Capacitance

One technique which can be used for obtaining deep-depletion capacitance measurements and hence the impurity doping density is to first prepare very thin insulating layers on n-GaAs. The motivation for doing this is as follows: the large bandgap of gallium arsenide and resultant low intrinsic carrier density lead one to expect small generation recombination currents in the surface depletion region.[2] Since the generation of minority carriers in the depletion region is a primary source of holes for the surface inversion layer, a low value of insulator leakage current would be required in order to sweep away the minority carriers under the gate and thus prevent an inversion layer from forming. If an insulator could be formed such that this condition were satisfied, then deep-depletion might be obtained under static conditions and from the deep-depletion capacitance measurements the doping could be obtained. It should be pointed out that a Hall measurement of the impurity doping level was not satisfactory for use in analyzing the C-V data. Variations in the doping level by factors of 2 or 3 were common on wafers only 5 mm square. The volume of semiconductor sampled using a Hall measurement is greater by a factor of 10^5 than the volume sampled using capacitance technique. It is suggested that the Hall measurements average out the doping non-uniformities.

In order to see if the inversion layer could be prevented from forming by using a thin insulator, a sample was anodized and annealed using the same techniques previously described except this time the oxide growth was stopped when the voltage across the dielectric reached 5 V. The sample was processed in an MIS configuration and C-V measurements were made as previously described; the results are shown in Fig. 5.8. Data taken at 150 MHz coincides with the 1 MHz data. Data taken at lower frequencies with small positive bias voltages are shown in Fig. 5.9. From this data the oxide capacitance was taken to be 120 pF. The high-frequency data in the deep depletion regime was corrected for the effect of the series oxide capacitance and is shown in a typical plot, usually made on Schottky barriers in Fig. 5.10. A good fit to a straight line is obtained so that the slope can be considered proportional to the semiconductor doping. From Eq. (2.21) this is seen to be

$$N_d = \frac{V_1 - V_2}{(1/C_D)^2_1 - (1/C_D)^2_2}\left[\frac{2}{q\epsilon_s A^2}\right] \tag{5.7}$$

By assuming the validity of the depletion approximation, the surface potential as given by Eq. (2.21) can be calculated as a function of gate bias and is indicated at several points in Fig. 5.8. The surface potential with zero gate bias is $V_s = -0.79$ V. Definite inflection points are present on the high-frequency curve; a rather abrupt change in slope occurs at $V_s = -1.10$ V and a gradual change in slope occurs at $V_s = -0.79$ V. If these singularities are associated with charge trapping states at the semiconductor surface, then the energy position of these states is given by $E_T = E_c - E_f - qV_s$.

The trapping states would then be located 0.83 and 1.15 eV below the conduction band edge. If one takes the usual approximation[3] that the onset of strong inversion occurs for

$$V_s = -2(kT/q)\ \ell n(N_d/n_i) \tag{5.8}$$

then inversion is expected for $V_s = -1.25$ V. The trap level at 1.15 eV below the conduction band edge might therefore prevent the surface from reaching inversion.

In order to ascertain if this was indeed the case, a second MIS device, made from the same wafer as that characterized by Fig. 5.5, was measured in the following manner: the usual C-V measurements using the quasistatic technique and small signal techniques at 10^2 and 10^6 Hz were made; additional measurements were made at 10^6 Hz using sweep frequencies of 0.15 Hz and 6 Hz. These measurements are shown in Fig. 5.11. The capacitance of the depletion layer was calculated using the equation

$$C_D = (1/C_m - 1/C_{ox})^{-1} \tag{5.9}$$

where C_m is the capacitance measured with a negative going sweep. The voltage drop across the depletion layer can be determined to within an additive constant by the equation

$$V_s + C = \frac{C_{ox}\, V_g}{C_{ox} + 2C_D} \tag{5.10}$$

where C is a constant term. This is just a simple voltage divider equation; the reader is reminded that C_D is a differential capacitance; the factor 2 arises because the voltage in the depletion layer is a quadratic function of distance and

$$\frac{Q_{sc}}{V_s} = 2C_D \tag{5.11}$$

where Q_{sc} is the charge in the semiconductor depletion layer. Implicit in Eq. (5.10) is the assumption that the charge in surface states doesn't change as the deep-depletion curve is traversed. The depletion layer capacitance for the device of Fig. 5.11 was calculated from Eq. (5.9) and this result was plotted vs. the voltage obtained from Eq. (5.10). This is shown in Fig. 5.12. Two persuasive arguments indicate that this curve represents the actual C-V relationship for the depletion layer only: the first is that a quite good fit to a straight line is obtained on the Schottky plot, and the second is that measurements using bias sweep frequencies of 0.15 Hz and 6 Hz give identical results. This implies that the bias sweep rate is fast enough to trace out the true depletion curve. The doping density then is calculated from Eq. (5.7) to be 7.32×10^{15} cm^{-3}.

If the point of onset of strong inversion is calculated using Eq. (5.8), then this value of surface potential can be inserted into Eq. (2.21) to give the minimum value of C_D for equilibrium bias conditions. Equation (2.23) then gives the result that the high-frequency minimum in capacitance should occur at a measured capacitance of 47.3 pF in Fig. 5.11. With -9 V bias this point occurs between the curves taken with negative and positive sweep directions for measurements taken at 1 MHz with a bias sweep rate of 100 mV/sec. If this result is taken at face value, then it implies that inversion is reached as the bias sweeps from positive to negative. When the bias ramp changes direction, the effect of the acceptor-like trap 1.15 eV below the conduction band is observed as the surface moves quickly away from inversion. At equilibrium the charge would be fixed at the trap location instead of occurring as mobile holes.

5.2 C-V Measurements on p-Type GaAs

One possible way of resolving the question of whether or not n-type GaAs MIS structures actually reach inversion would be to repeat the C-V measurements on p-type material. If the p-type material were to show evidence of surface accumulation, then inversion would be expected to occur on the n-type material. This argument rests on the assumption that the surface properties of n- and p-type material are essentially the same. This would not be unreasonable since for a typical doping density of $10^{17}/cm^3$ only about one in ten million surface lattice sites is occupied by an impurity atom. It would then be expected that the surface properties would still be dominated by the intrinsic surface atoms and the adsorbed or chemically-bonded surface interlayer material rather than the impurity atoms.

An anodically-prepared dielectric was formed on a Cd-doped, $p = 2.3x10^{17}\ cm^{-3}$, <100>-oriented GaAs wafer which was then annealed and mounted in the manner described in Chapter 4 except for the use of a soldered indium-cadmium (80%-20%) back contact. The measurements were performed in the same manner as previously described and the results are shown in Fig. 5.13. The devices all exhibited a counter-clockwise hysteresis, however, only the negative going sweep is shown for clarity. A large frequency dispersion in the dielectric constant of the oxide appears to occur between 10 Hz and the quasistatic data. The analysis of the quasistatic data was accomplished using a different value of oxide capacitance than that used for the high frequency data. Integration

of the area below a horizontal line drawn through C_{ox} and the experimental curve for the quasistatic data as described by Berglund[4] yields a total change in surface potential of 0.45 volt. The carrier concentration for this device was determined from a deep-depletion curve taken with a sweep rate of 400 V/sec. The doping density was calculated from the plot of the measured deep-depletion capacitance (C_m) vs. gate voltage (V_g) shown in Fig. 5.14 using the method of van Gelder and Nicollian.[5] Using the equation

$$N_A = 2(q\varepsilon_s \, d(A/C_m)^2/dV_g))^{-1} \tag{5.12}$$

where N_A is the doping density, q is the electronic charge, ε_s is the semiconductor dielectric constant, and A is the device area, a doping density of $N_A = 2.3\text{x}10^{17}$ cm^{-3} is obtained. Knowledge of the doping density allows calculation of the surface potential from the high-frequency capacitance curve measured at 150 MHz using the depletion approximation, i.e.,

$$V_s = \frac{kT}{q} + \frac{q\varepsilon_s \, N_A A^2}{2 \, C_D^2} \tag{5.13}$$

where k is Boltzmann's constant, T is the temperature in degree Kelvin, and C_D is the semiconductor space charge capacitance computed from Eq. (5.9). The result is that $V_s(V_g = 10V) = 0.83$ V, $V_s(V_g = -10$ V$) = 0.37$ V and V_s $(V_g = 0) = 0.59$ V. The total surface potential excursion is 0.46 V in good agreement with the value of 0.45 V obtained from the quasistatic measurements. The minimum value of the surface state density for this sample was determined to be $3\text{x}10^{12}$ cm^{-2} eV^{-1}. The Fermi level at the surface is located 0.68 eV above the valence band maximum (VBM) with $V_g = 0$. This compares to the value of 0.46 eV that was found for anodized n-type material.

Although not in good quantitative agreement, these values are consistent with the trends observed in Fermi level pinning on GaAs as determined by Spicer *et al* from photoemission measurements.[6] After 10^9 Langmuir oxygen exposure they found that the Fermi level pinning positions on cleaved (110) GaAs to be 0.8 eV and 0.45 eV above the VBM for n- and p-type material respectively. This lack of close agreement is not surprising considering the vastly different histories of the devices being compared. However, it does support the notion that the surface pinning observed at low oxygen coverages on cleaved samples is also present on heavily oxidized surfaces.

The data in Fig. 5.13 strongly suggest that the p-GaAs surface anodized in the aforementioned manner does not reach accumulation. Coupled with previous arguments that the n-GaAs surface does not reach flatband or accumulation, the conclusions seem inescapable that the surfaces on both n- and p-material are pinned in the middle of the bandgap, that surface potential excursions of only $\sim$ 0.45 V are possible, and that neither accumulation nor inversion are reached with electric field values of less than 10^6 V/cm on either material.

A compilation of the results obtained for the surface-state density of GaAs is shown in Fig. 5.15. These curves serve to illustrate the previously stated conclusions that the Fermi level is pinned in the lower one-third of the bandgap and that enormously high surface-state densities are obtained as either band edge is approached.

5.3 C-V Measurements on n-Type InP

A series of electrical measurements were made on SiO_2-InP MIS samples with the aim of determining the nature of the interface. Figure 5.16

illustrates room temperature C-V data taken in the frequency range from DC to 450 MHz which is typical of that obtained on the n-type samples. The quasistatic curve has no minimum but rather shows a gradual increase as the gate voltage is increased from -10 V. Integration of the area under this curve in the manner proposed by Berglund[4] yields a total change in surface potential of 1.01 V. These devices exhibit a large amount of frequency dispersion with positive gate bias even beyond 150 MHz.

5.3.1 Frequency Dispersion in the Dielectric

An analysis of the data is not possible unless a conclusion can be reached as to whether the frequency dispersion is caused by the bulk properties of the insulator or by the interface states. This issue is important because if the dispersion is due to interface states, then the surface does not reach accumulation with positive gate bias. The data taken at 450 MHz indicate a surface that is still depleted with 10 V gate bias if the frequency dispersion is due to surface states. Seemingly a way to resolve this issue is to modulate the capacitance of the semiconductor space charge layer by illuminating the sample. Pierret and Sah[7,8] have examined this effect in detail; the model can be described in the following way: when greater than bandgap radiation is incident on the sample then electron-hole pairs are generated which increase its conductivity. At very high irradiation levels sufficient carriers will be generated to cause the semiconductor surface to be metallic in nature. When this occurs the space charge capacitance will be greatly increased, and the total measured capacitance is due only to the insulating layer.

The data in Fig. 5.17 were taken on a device which had a semitransparent nickel gate. A small tungsten lamp providing an irradiance of 200 $\mu W\ cm^{-2}$

on the sample did not increase the capacitance measured with large positive bias. A He-Ne laser (6320Å) was used in order to increase the irradiance to the order of 1 W cm^{-2}. This had the effect of producing flat C-V curves located at the capacitance value obtained with 10 V bias in the dark. This result strongly indicates that the observed frequency dispersion is due to the oxide and not to surface states in the semiconductor. Otherwise the high-frequency curves with large positive bias would have been lifted by the illumination. With this result in mind it would then seem that the proper way to analyze any particular high-frequency C-V curve taken on these samples is to assume the maximum capacitance at that frequency to be equal to the oxide capacitance.

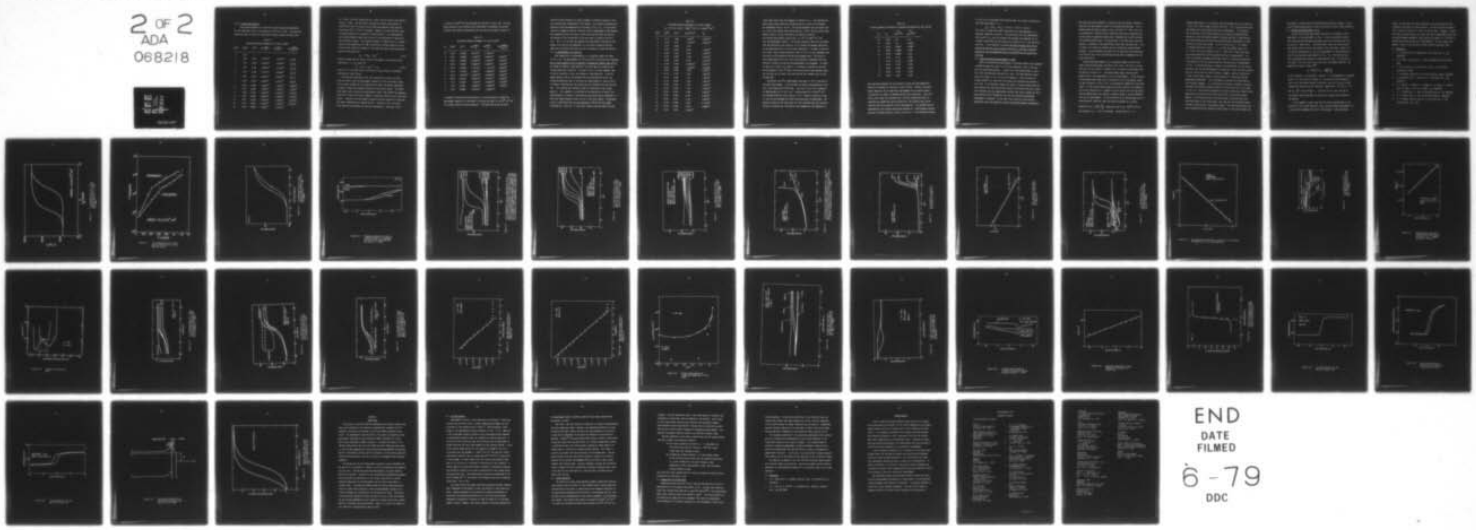
5.3.2 Impurity Density from Deep-Depletion Measurements

The next parameter requiring determination is the bulk doping level. The doping variations observed on the GaAs substrate material indicate that again the most satisfactory way of measuring the doping would be from a C-V measurement made on the MIS device being analyzed. Figure 5.18 illustrates a deep-depletion measurement made at 1 MHz with a gate voltage sweep rate of 400 V/S. A Schottky-type plot of the data is shown in Fig. 5.19 from which a doping level of 2.08×10^{16} cm^{-3} was calculated using Eq. (5.12). The minimum space charge capacitance expected for this doping level was determined from Eq. (2.22) and the total capacitance was calculated from Eq. (2.23). This value for the minimum high-frequency capacitance is shown as a dashed line in Fig. 5.18. This agrees very well with the measured minimum at 10^6 Hz using a sweep rate of 100 mV/S and implies that the surface potential is modulable over the full bandgap from accumulation to inversion.

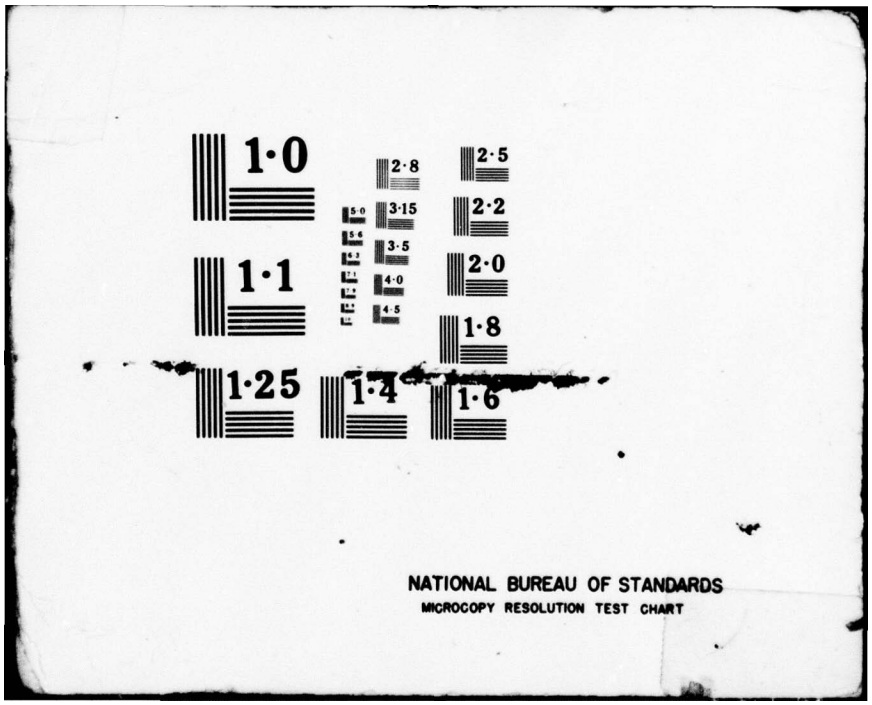
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5.3.3 Surface State Density

The surface potential as a function of gate voltage was determined for the 1 MHz data in Fig. 5.18 using Eqs. (2.23) and (2.16). The resulting values are given in Table 5.2 along with the space charge calculated from

Table 5.2

Calculated Surface Parameters for n-InP at 300°K.

V_g(V)	C_m(pF)	V_s(V)	$Q_{sc}(\frac{coul.}{m^2})$	$Q_T(\frac{coul.}{m^2})$	$N_{ss}(\frac{states}{cm^2\ eV})$
7	9.32	-			
6	9.30	0.241	-1.42×10^{-2}	-1.67×10^{-3}	$Q_{sc}>Q_T$
5	9.28	0.186	-4.96×10^{-3}	-1.40×10^{-3}	$Q_{sc}>Q_T$
4	9.24	0.140	-1.99×10^{-3}	-1.12×10^{-3}	$Q_{sc}>Q_T$
3	9.18	0.106	-1.01×10^{-3}	-8.39×10^{-4}	$Q_{sc}>Q_T$
2	9.08	0.073	-4.83×10^{-4}	-5.56×10^{-4}	$Q_{sc}>Q_T$
1	8.90	0.034	-1.59×10^{-4}	-2.8×10^{-4}	$Q_{sc}>Q_T$
0	8.60	-0.005	1.86×10^{-5}	1.45×10^{-6}	1.58×10^{12}
-1	8.18	-0.054	1.50×10^{-4}	2.74×10^{-4}	1.14×10^{12}
-2	7.60	-0.132	2.75×10^{-4}	5.42×10^{-4}	7.47×10^{11}
-3	7.04	-0.246	3.96×10^{-4}	7.99×10^{-4}	4.14×10^{11}
-4	6.52	-0.414	5.26×10^{-4}	1.04×10^{-3}	3.47×10^{11}
-5	6.10	-0.614	6.47×10^{-4}	1.27×10^{-3}	4.57×10^{11}
-6	5.80	-0.803	7.44×10^{-4}	1.51×10^{-3}	-

Eq. (2.20), the total charge from Eq. (2.28), and the surface state density from Eq. (2.30). The data imply a minimum in surface state density of 3.5×10^{11} cm^{-2} eV^{-1} at a point 0.4 eV below the conduction band edge and values near 10^{12} $c,^{-2}$ eV^{-1} at flatband. However, for more positive values of surface potential an unphysical situation results. The semiconductor space charge becomes larger than the sum of the semiconductor charge plus the interfacial charge. This apparent paradox is probably due to a nonzero surface state capacitance at 1 MHz with positive surface potential values. If the surface states do respond at 1 MHz then the space charge capacitance that was calculated from

$$C_D = (1/C_m - 1/C_i)^{-1} \tag{5.14}$$

would be larger than the actual value by the amount of the surface state capacitance, i.e., C_D should be

$$C_D = (1/C_m - 1/C_i)^{-1} - C_{ss} \tag{5.15}$$

Use of Eq. (5.14) would lead to artificially large values of calculated semiconductor space charge.

Two possible experiments exist for resolving this issue, the first being to simply raise the measurement frequency so that the surface states can no longer respond and the second being to lower the sample temperature in order to lower the frequency response of the surface charge. The admittance meter used to perform the measurements above 1 MHz lacked the necessary precision to resolve the small changes in capacitance which occur in this bias region. Therefore, the measurement frequency was kept constant at 1 MHz and the sample temperature was lowered to 85°K. The data of Fig. 5.17 were first analyzed to determine the carrier concentration. Using Eq. (2.22)

a value of 7.0×10^{15} cm^{-3} was obtained from the plot in Fig. 5.20. The data were analyzed in the previously described manner to determine the surface potential and surface state density and the results are shown in Table 5.3.

Table 5.3

Calculated Surface Parameters for n-InP at 85°K.

V_g	C_m(pF)	V_s(V)	$Q_{sc}(\frac{coul.}{m^2})$	$Q_T(\frac{coul.}{m^2})$	$N_{ss}(\frac{states}{cm^2\ eV})$
10	118.8	0.07969	-16.6×10^{-2}	-2.179×10^{-3}	-
9	118.5	0.04449	-1.136×10^{-3}	-1.967×10^{-3}	-2.39×10^{13}
8	118.2	0.03586	-5.874×10^{-4}	-1.749×10^{-3}	5.51×10^{12}
7	118.0	0.03121	-4.090×10^{-4}	-1.530×10^{-3}	2.28×10^{13}
6	117.8	0.02789	-3.141×10^{-4}	-1.311×10^{-3}	5.96×10^{12}
5	116.3	0.01494	-1.00×10^{-4}	-1.095×10^{-3}	4.87×10^{12}
4	113.0	6.64×10^{-6}	-2.832×10^{-8}	-8.784×10^{-3}	3.94×10^{12}
3	106.0	-0.02377	6.468×10^{-5}	-6.64×10^{-4}	5.32×10^{11}
2	90.5	-0.1288	1.118×10^{-4}	-4.675×10^{-4}	1.93×10^{10}
1	74.3	-0.4562	3.296×10^{-4}	-3.198×10^{-4}	1.59×10^{10}
0	64.5	-0.8965	4.637×10^{-4}	-1.969×10^{-4}	-

A steadily rising surface state density is calculated which is below the measurement capability in the middle of the gap and peaks at 2.3×10^{13} cm^{-2} eV^{-1} for slightly positive surface potential. The decreasing values for more

positive surface potential are again probably an artifact caused by a non-zero surface-state capacitance in this region. The surface state densities obtained at the two temperatures are plotted in Fig. 5.21. If the surface states are assumed to possess a physical reality independent of the measurement temperature then the actual surface state density would be given by the maximum of the intersection of the two curves as shown by the solid line. This is to say that the apparent low-state density observed in the middle of the gap at low temperature is an artifact caused by the bias sweep rate not being sufficiently low for the sample to reach equilibrium.

5.4 C-V Measurements on p-Type InP

Room temperature C-V measurements on a p-InP/SiO_2 sample are shown in Fig. 5.22. The measurements at 10^5 Hz and 10^6 Hz coincide which indicates that a high-frequency curve is obtained at frequencies greater than 10^5 Hz. An attempt to measure a deep-depletion curve was made by increasing the voltage sweep rate to 600 V/S. The data of Fig. 5.23 show, however, that it was not possible to place the specimen in deep depletion. Since the sample doping could not be obtained from the deep-depletion curve, the following method was used to calculate the doping density: data on the n-InP samples indicated that the surface was near flatband with zero applied bias. This implies that inversion should be achievable on the p-type material. This argument is reinforced by the observation of nearly flat high-frequency C-V curves in the positive bias region and by the manner in which the lower frequency curves rise up in this bias region. The maximum value of capacitance that could be measured at 10^6 Hz with the sample irradiated at a level of $\sim$ 1 W cm^2 with a He-Ne laser was taken to be the

Table 5.4

Calculated surface parameters for p-InP at 300°K.

C_{ox} = 16.7 pF, Area = 1.08×10^{-3} cm^2, p = 5.85×10^{16} cm^{-3}.

V_g(V)	C_m(pF)	V_s(v)	Q_{ss}(coul/m^2)	N_{ss}
10	13.75	1.036	3.4×10^{-5}	9.42×10^{11}
9	13.78	0.971	1.32×10^{-4}	6.87×10^{12}
8	13.79	0.958	2.75	∞
7	13.79	0.958	4.305	1.32×10^{13}
6	13.80	0.951	5.874	4.54×10^{12}
5	13.82	0.932	7.165	6.91×10^{12}
4	13.85	0.919	8.604	2.54×10^{12}
3	13.89	0.888	9.866×10^{-4}	8.62×10^{11}
2	13.97	0.821	1.079×10^{-3}	2.52×10^{12}
1	14.02	0.790	1.204	8.75×10^{11}
0	14.13	0.725	1.279	1.86×10^{12}
-1	14.18	0.686	1.411	1.89×10^{12}
-2	14.25	0.648	1.526	2.36×10^{12}
-3	14.30	0.616	1.647	1.88×10^{12}
-4	14.37	0.578	1.761	3.36×10^{12}
-5	14.42	0.554	1.890	4.65×10^{12}
-6	14.45	0.536	2.024	4.65×10^{12}
-7	14.48	0.518	2.158	4.65×10^{12}
-8	14.52	0.500	2.292	5.31×10^{12}
-9	14.55	0.484	2.428	8.88×10^{12}
-10	14.57	0.474	2.56×10^{-3}	-

oxide capacitance using the arguments of Section 5.3.1. The semiconductor space charge capacitance was calculated from Eq. (2.23) and the doping was determined from Eq. (2.22). The surface potential was calculated from Eq. (2.16), the surface state charge from Eq. (2.29), and the surface state density from Eq. (2.30); the results are shown in Table 5.4. The surface state density varies from $\sim 9 \times 10^{11}$ to 8×10^{12} cm^{-2} eV^{-1} over the measurement interval. The surface potential shift was calculated from the quasistatic data using Eq. (2.37) taking the maximum capacitance on the quasistatic plot to be the oxide capacitance. As shown in Table 5.5 this gives a total surface potential shift of 0.14 V in poor agreement with the value of 0.56 obtained from the high-frequency data. The value of oxide capacitance used in Eq. (2.51) was adjusted to determine the value required in order to bring the two measurements into agreement. As shown in Table 5.5 a value of C_{ox} that is $\sim$ 2% larger is required to give the surface potential shift of 0.56 V calculated from the high frequency data. One can then say, at least, that the high and low frequency data are not inconsistent.

Quasistatic and 10^6 Hz measurements were made at 77°K in the dark on the same p-type sample. It was possible to obtain a deep-depletion curve with a bias sweep rate of 600 V/sec. The curve in Fig. 5.24 is shown on a Schottky-type plot in Fig. 5.25. A doping density of 2.67×10^{16} cm^{-3} was obtained from this plot using Eq. (5.12). Before an analysis of the C-V data can be performed the oxide capacitance must be determined. The previous results on the SiO_2 layers on n-InP indicated that the insulator dielectric constant was a function of both temperature and frequency so

Table 5.5

Surface potential variations calculated from quasistatic data (p-InP)

V_g	C_m	ΔV_s C_{ox}=18.25	ΔV_s C_{ox}=18.64
-10	18.25	0.0	0.0
-8	18.25	0.0	0.0419
-6	18.20	0.0027	0.0864
-4	18.05	0.0208	0.146
-2	17.80	0.0647	0.231
0	17.80	0.117	0.324
2	18.12	0.138	0.386
4	18.22	0.140	0.432
6	18.25	0.142	0.474
8	18.25	0.142	0.516
10	18.25	0.142	0.557

that one would probably not be justified in using the room temperature dielectric constants for analysis of the 77°K data. Further, the experimental apparatus used to make these measurements did not permit sample illumination as a means of determining the oxide capacitance. Since the data on the n-type InP indicated that a surface accumulation layer of electrons was formed with positive gate bias, this implies that surface inversion should be possible on the p-type material. The minimum value of semiconductor space charge capacitance expected in a high-frequency measurement was calculated from Eq. (2.22) to be 43.7 pF. If the measured minimum

in Fig. 5.24 is associated with inversion then this allows calculation of the oxide capacitance, i.e.,

$$C_{ox} = (1/C_m - 1/C_{sc}) = (1/13.5 - 1/43.7) = 19.5 \text{ pF}$$

This value is larger than the DC capacitance at room temperature -- a seemingly unphysical situation. This would imply that the experimental value used for C_{sc} did not represent the minimum value expected for an inverted surface and that the surface was actually still in the depletion condition. It was therefore concluded that the available data did not justify the choice of any particular value of C_{ox} and that a detailed analysis of the low-temperature data on p-type InP was not possible at this time.

5.5 Surface Photovoltage Measurements on GaAs

Before the photovoltage measurements on the GaAs samples were attempted a thermally-grown SiO_2 layer on silicon was measured to see if the apparatus was performing properly. Figure 5.26 is the photovoltage vs. gate bias curve obtained using the Hg-Xe arc lamp. The high-frequency capacitance curve shown in Fig. 5.27 was also measured. From this data the surface potential vs. gate bias relationship was obtained and plotted in Fig. 5.26. In the depletion region the values of surface photovoltage are only slightly less than the surface potential calculated from the C-V data. This indicates that the semiconductor surface very nearly reaches the flat-band condition with illumination and that the saturated photovoltage measurement is obtained. As the Fermi level position at the surface approaches either band edge the surface photovoltage becomes considerably

less than the surface potential, indicating that the surface irradiation level was not high enough to obtain the saturated photovoltage. This is expected from the results shown in Figs. 2.10 and 2.11, which show that an accumulated or inverted surface requires excess carrier densities one or more orders of magnitude higher than a depleted one in order to obtain the saturated photovoltage. Of significance is the fact that a polarity reversal is obtained in the photovoltage signal near zero gate bias. This is taken to be conclusive evidence that the surface has passed through flatband. It was therefore concluded that the apparatus was working properly and that the C-V and photovoltage results were in agreement for the SiO_2-Si MIS device.

Photovoltage measurements on an n-type GaAs sample on which a 60 V anodic oxide had been grown are shown in Fig. 5.28. The 100 Hz C-V characteristic for this device is shown in Fig. 5.29 which is consistent with the results of Section 5.1. The photovoltage signal saturates with negative bias in the same manner as the C-V measurements. A zero crossing of the photovoltage signal was not obtained on any of the samples tested for gate voltages as large as 40 V on approximately 1000Å-thick insulating layers. If the surface photovoltage and surface potential are assumed to be directly proportional, as seemed to be the case for the Si-SiO_2 sample, then the photovoltage data indicate a greater change in surface potential than the C-V measurements. If the flattening of the photovoltage curve is associated with inversion, then that would correspond to a surface potential of $V_s = 2 \frac{kT}{q} \ell n \frac{N_d}{n_i}$. Using the value of $N_d = 4 \times 10^{16}$ cm^{-3} for this material $V_s = -1.23$ V is obtained. Assuming that $V_s = k x$

(photovoltage) where k is a constant, then the maximum value of V_s would be - 0.25 V for a total change of 0.98 V (38 kT/q). This is greater than twice the change (0.4 V) calculated from the C-V measurements. An alternative way of looking at this situation would be to choose the proportionality constant so that the surface potential obtained from the C-V data matches the surface potential obtained from the photovoltage measurements at some arbitrary value of gate voltage. If this is done at V_g = - 10 V where V_s obtained from the C-V data is - 1.1 V, then the maximum value of V_s is - 0.23 V for a total change of 0.87 V. Again this is more than twice the surface potential excursion deduced from the C-V measurements. The ratio of maximum to minimum photovoltage signal is 4.85 while the maximum to minimum ratio for the surface potential obtained from C-V measurements is 1.48. If the photovoltage is assumed to be proportional to the surface potential then the two measurements are consistent in that they both indicate that the surface does not reach flatband. However, they are inconsistent in that a much larger change in surface potential is predicted from the photovoltage experiment. This discrepancy can perhaps be rationalized by the following argument. If a large positive voltage is present on the gate electrode, the potential energy diagram for the electrons will be as shown in Fig. 5.30. The electrons generated by incident light would normally drift away from the surface while the holes would stay in the surface region. However, if the electrons have sufficient energy to penetrate the oxide beyond the depth of the fixed charge, then they will be accelerated toward the metal electrode until they become trapped. Thus both the electrons and holes produced by optical generation would remain in the surface region and

the change in surface potential observed would be greatly reduced. A zero value of photovoltage would not then be indicative of zero surface potential.

5.6 Photovoltage Measurements on InP

Surface photovoltage measurements were made on InP samples in the same manner as the measurements on GaAs. It was not possible to obtain fully-saturated photovoltage measurements with the 4 mW He-Ne laser that was used as a light source. The photovoltage signal was always reduced when neutral density filters were placed in the light beam. Figure 5.31 illustrates photovoltage vs. gate bias measurements on the same device as used in the capacitance measurements of Fig. 5.18. With positive gate bias the photovoltage saturates at approximately 10 mV. The polarity of the signal is of the correct sign to be due to the Dember potential, the magnitude of which is given by[9]

$$V_D = \frac{kT}{q} \frac{b - 1}{b + 1} \ln 1 + \frac{(b+1)\ \Delta n}{bn_o + p_o}$$

In this equation, k is Boltzmann's constant, T is the temperature in degrees Kelvin, q is the electronic charge, b is the electron-to-hole mobility ratio, Δn is the surface excess of electrons, and n_o and p_o are the equilibrium bulk electron and hole densities, respectively. For InP $b = 7$ so that $V_D \simeq \frac{kT}{q} = 26$ mV for $\frac{\Delta n}{n_o} = 1$. Thus the lack of a zero crossing of the surface photovoltage does not necessarily indicate that flatband is not reached.

If the argument is again used that the surface photovoltage is proportional to the surface potential, then the photovoltage measurements are in qualitative agreement with the C-V measurements. Both experiments

support the view that the surface potential can be modulated from near flatband to the onset of strong inversion. No really convincing explanation is given for why this is so for InP and not GaAs. However, it seems that fewer spurious effects are likely with the C-V measurements than with the photovoltage measurements simply because the sample is in the dark at thermal equilibrium during the C-V measurements. For this reason more weight is given to the conclusions drawn from the capacitance data.

5.7 References

1. E. H. Nicollian and A. Goetzberger, Bell System Tech. J., 46, 1055(1967).
2. R. A. Smith, *Semiconductors*, p. 290, Cambridge University Press, 1959.
3. S. M. Sze, *Physics of Semiconductor Devices*, p. 436, Wiley-Interscience, 1969.
4. C. N. Berglund, IEEE Trans. on Electron Devices, ED-13, 701(1966).
5. W. van Gelder and E. H. Nicollian, J. Electrochem. Soc., 118, 138(1971).
6. W. E. Spicer, I. Lindau, P. E. Gregory, C. M. Garner, P. Pianetta, and P. W. Chye, J. Vac. Sci. Technol., 13, 780(1976).
7. R. F. Pierret and C. T. Sah, Solid-State Electron., 13, 269(1970).
8. R. F. Pierret and C. T. Sah, Solid-State Electron., 289(1970).
9. J. I. Pankove, *Optical Processes in Semiconductors*, p. 320, Prentice-Hall, Inc., 1971.

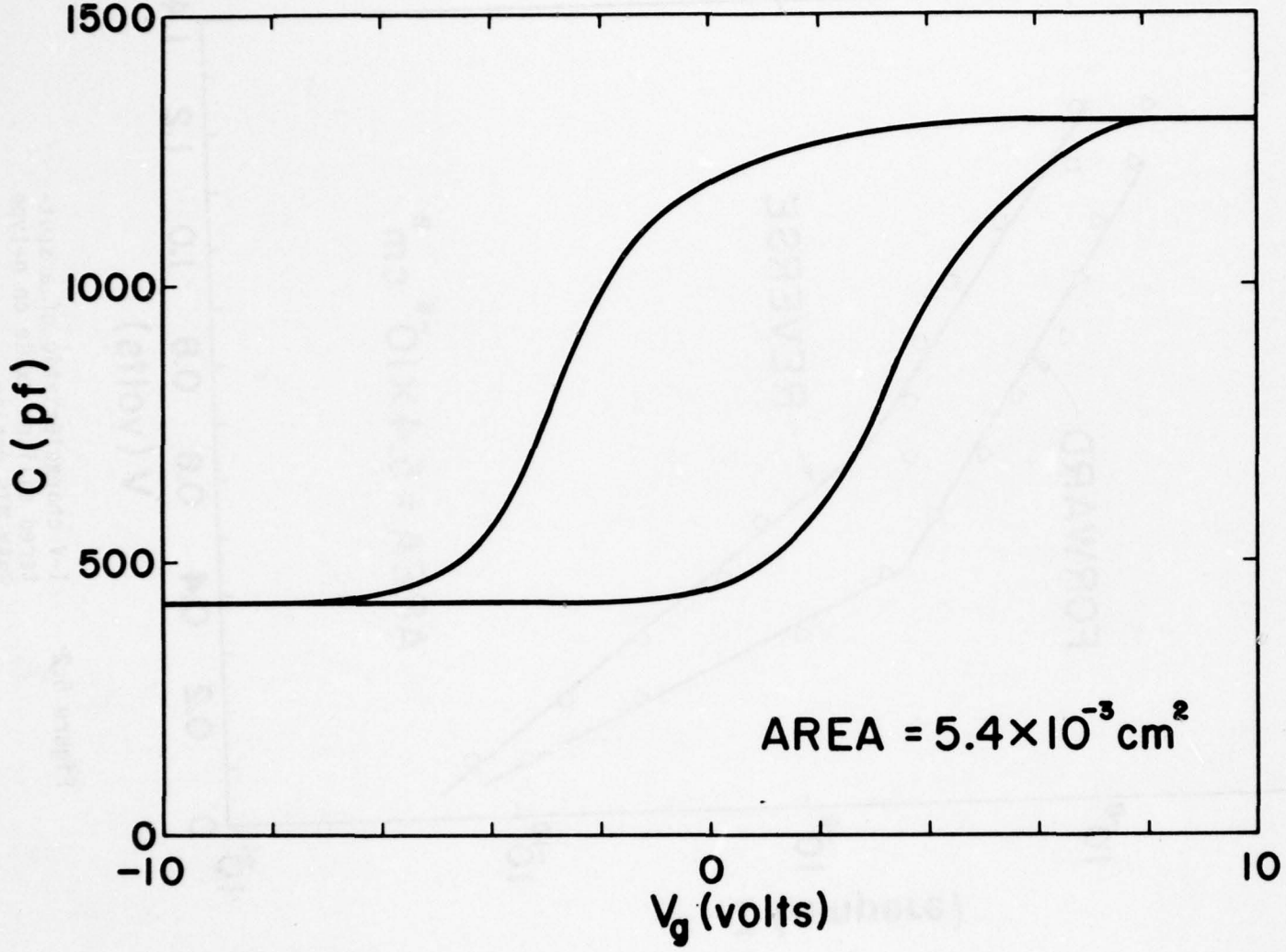


Figure 5.1 C-V characteristic of a sputtered silicon oxide on n-type GaAs MIS device; f = 1 MHz, T = 300°K.

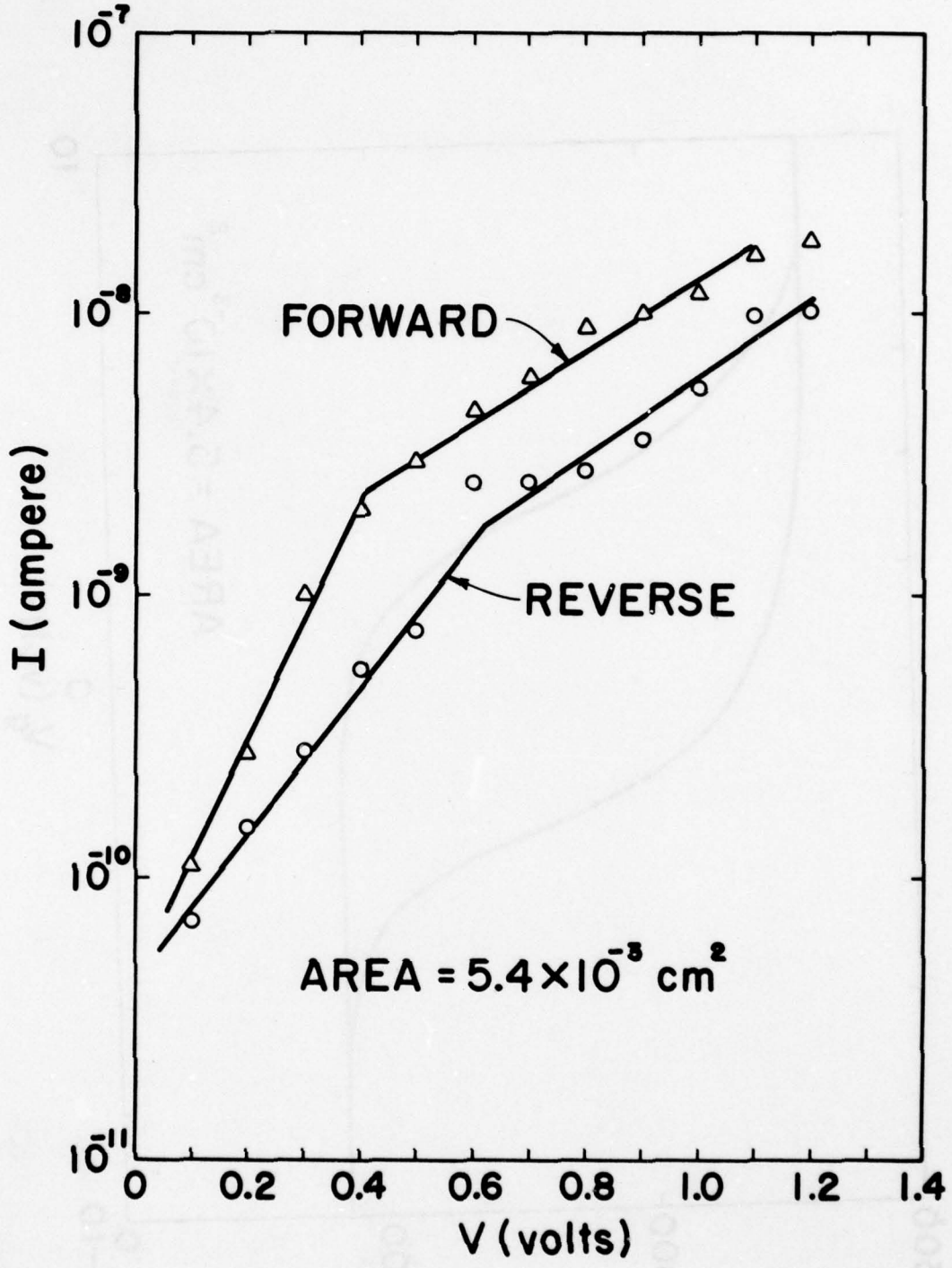


Figure 5.2 I-V characteristic of a sputtered silicon oxide on n-type GaAs MIS device.

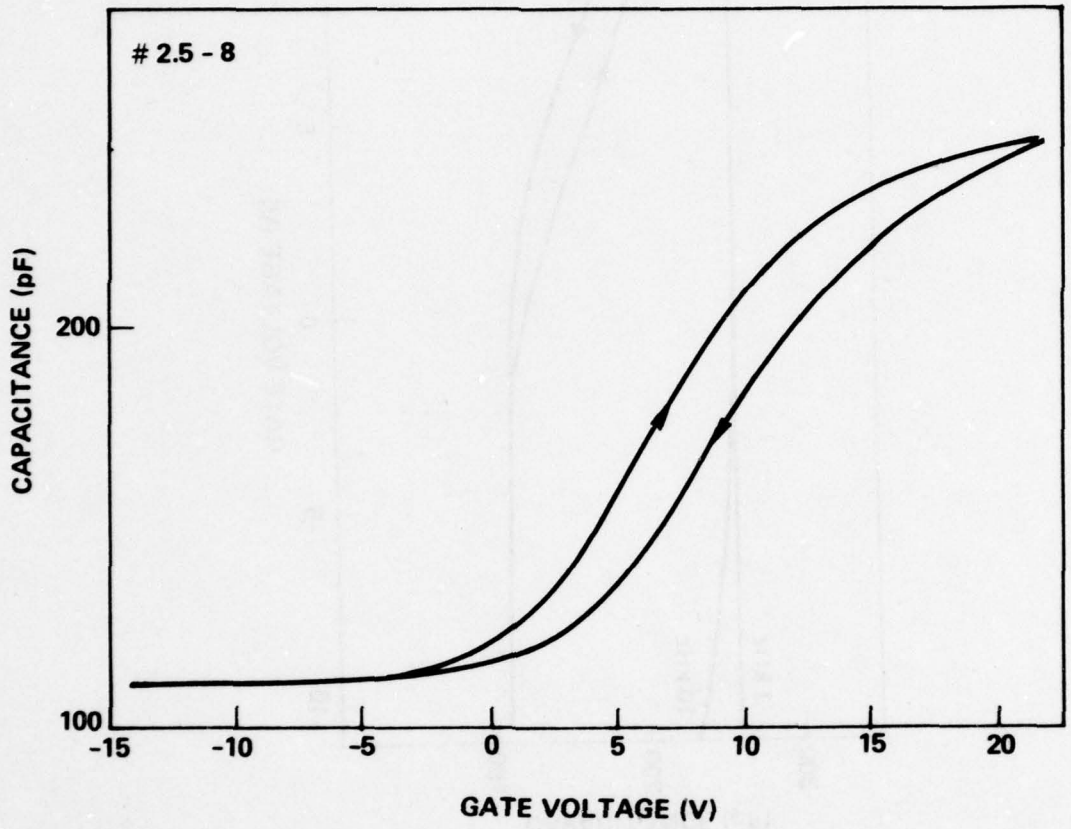


Figure 5.3 C-V characteristic of a sputtered silicon nitride on n-type GaAs MIS device; f = 1 MHz, T = 300°K.

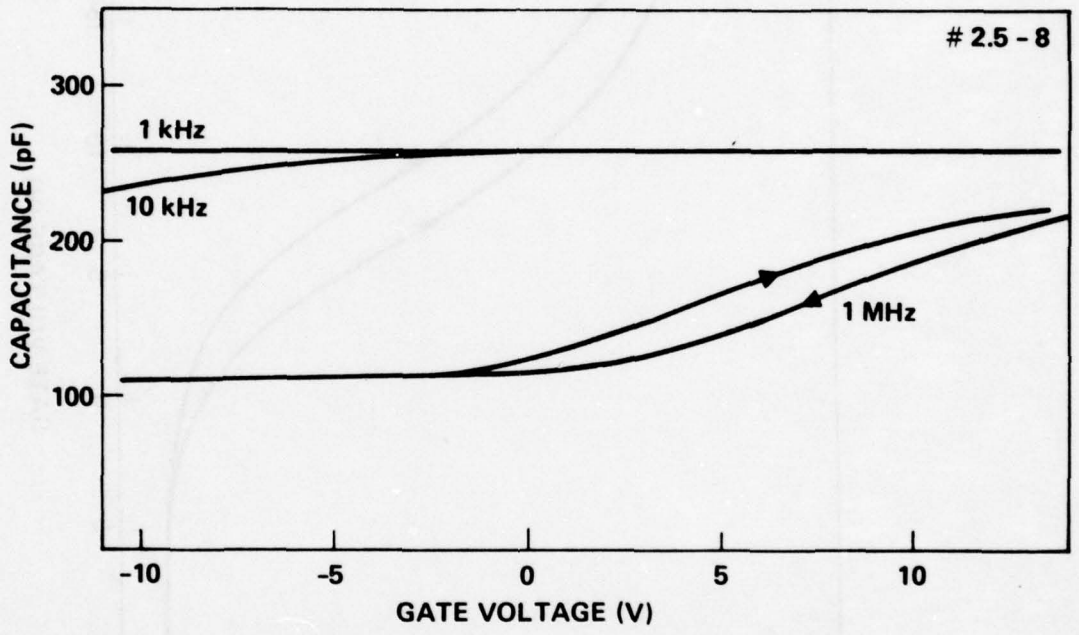


Figure 5.4 Frequency dispersion in the C-V characteristics of a sputtered silicon nitride on n-type GaAs MIS device; T = 300°K.

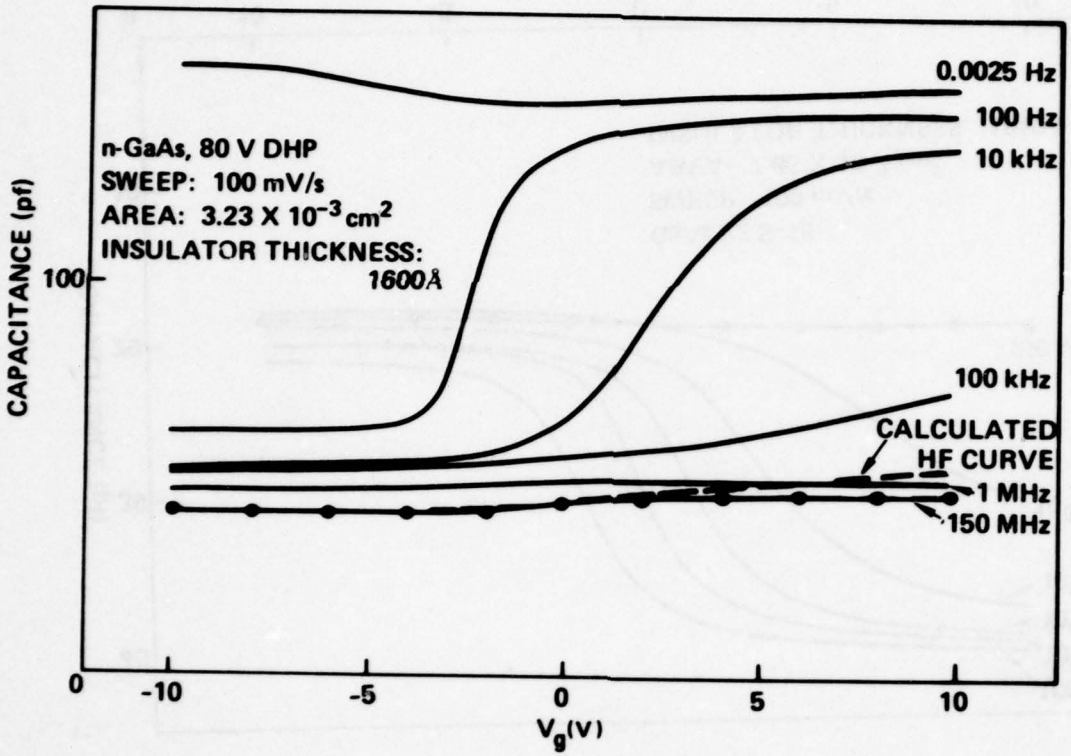


Figure 5.5 C-V characteristics of an n-type GaAs MIS device with a dielectric formed by anodization at a current density of 8 $\mu A/cm^2$ to 80 V in a 0.03 M aqueous solution of ammonium dihydrogen phosphate; measured from DC to 150 MHz at 300°K; also shown is the calculated high frequency curve represented by the dashed line.

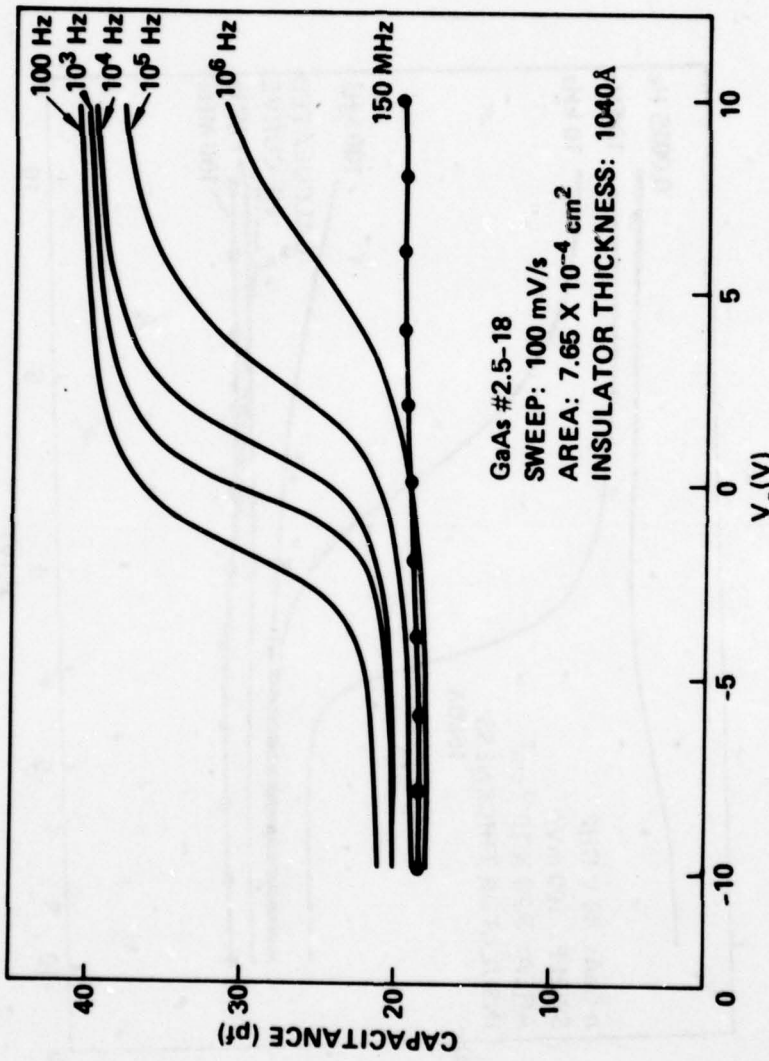


Figure 5.6 C-V characteristics of a sputtered silicon nitride on n-type GaAs MIS device measured from 100 Hz to 150 MHz; T = 300°K.

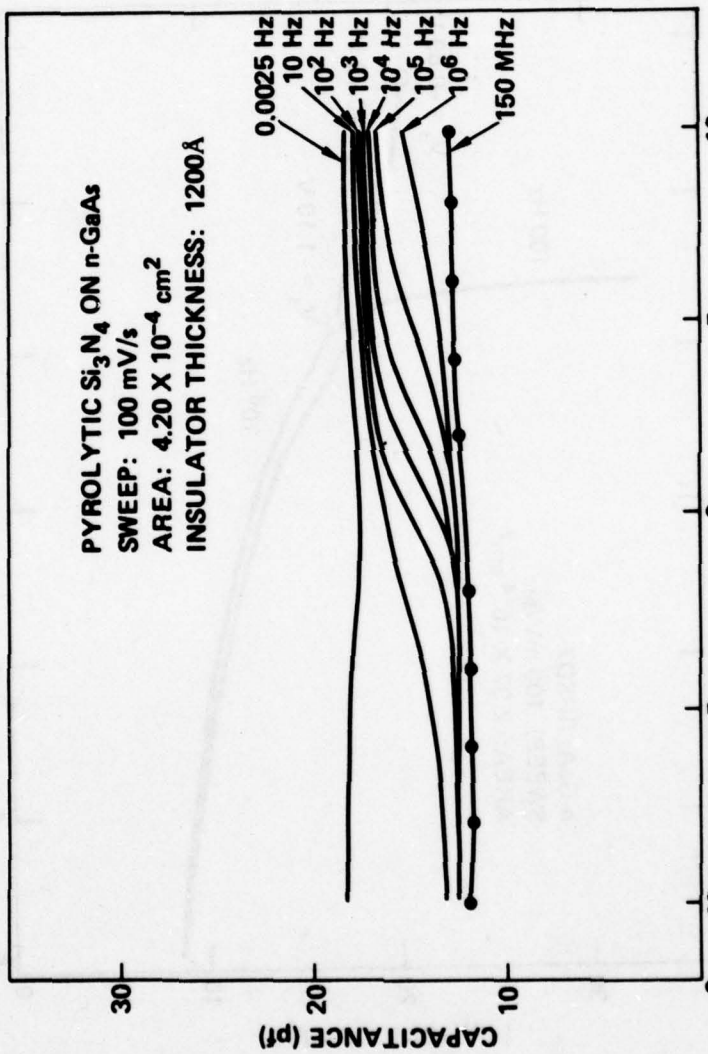


Figure 5.7 C-V characteristic of a pyrolytic silicon nitride on n-type GaAs MIS device measured from DC to 150 MHz; T = 300°K.

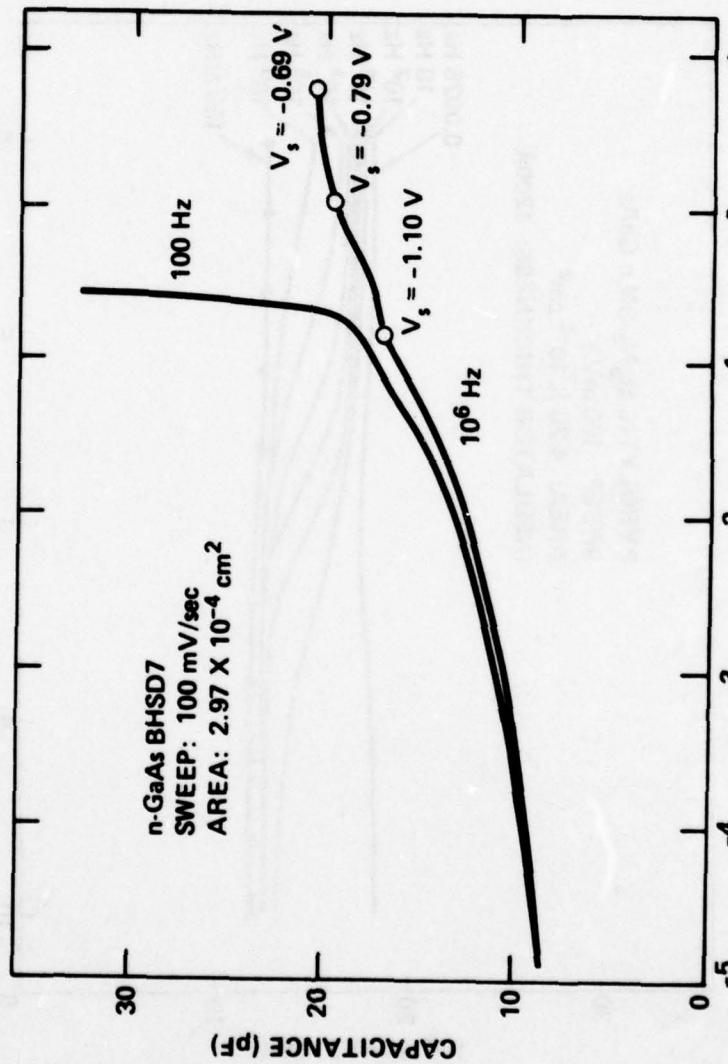


Figure 5.8 C-V data for an MIS device constructed using n-type GaAs with a dielectric formed by anodization at a current density of 8 $\mu A/cm^{-2}$ to 5 V in a 0.03 M aqueous solution of ammonium dihydrogen phosphate; T = 300°K.

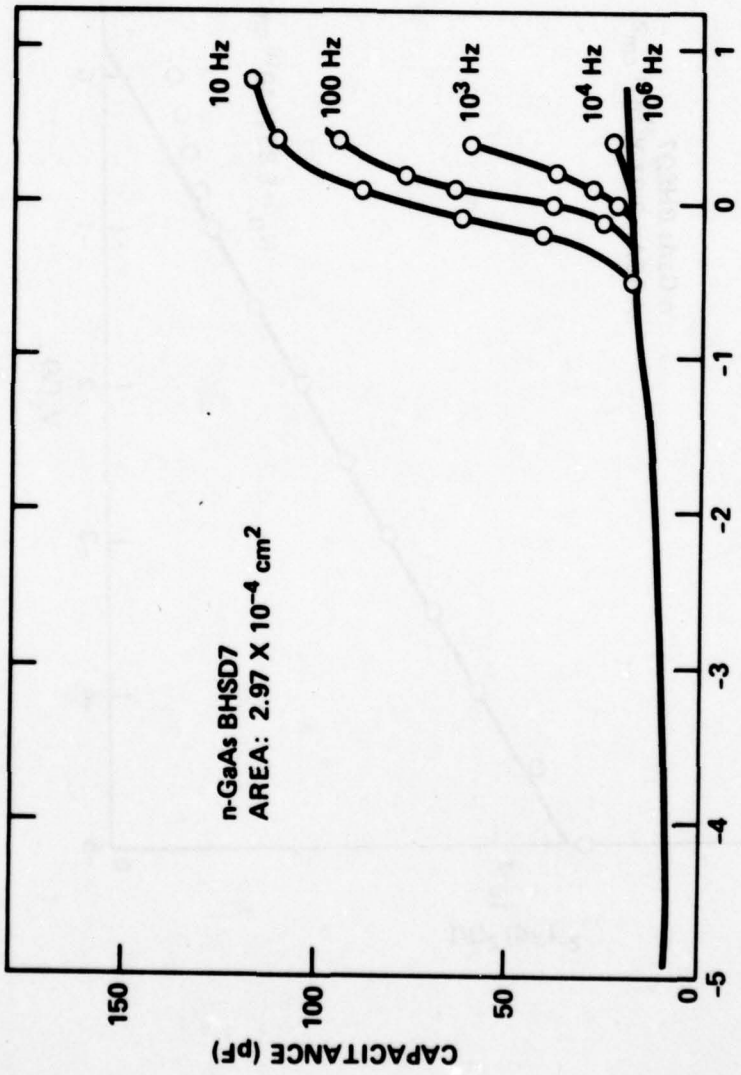


Figure 5.9 Low frequency C-V data for the device of Figure 5.8.

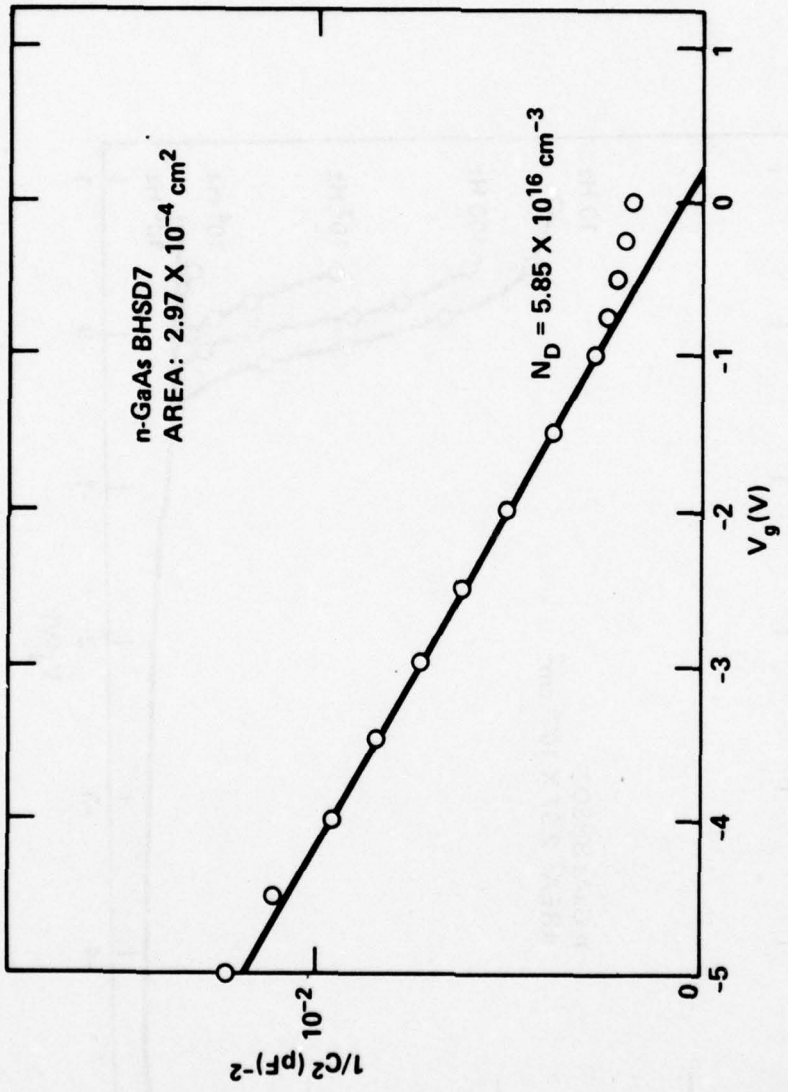


Figure 5.10 Deep depletion capacitance vs gate bias for the device of Figure 5.8.

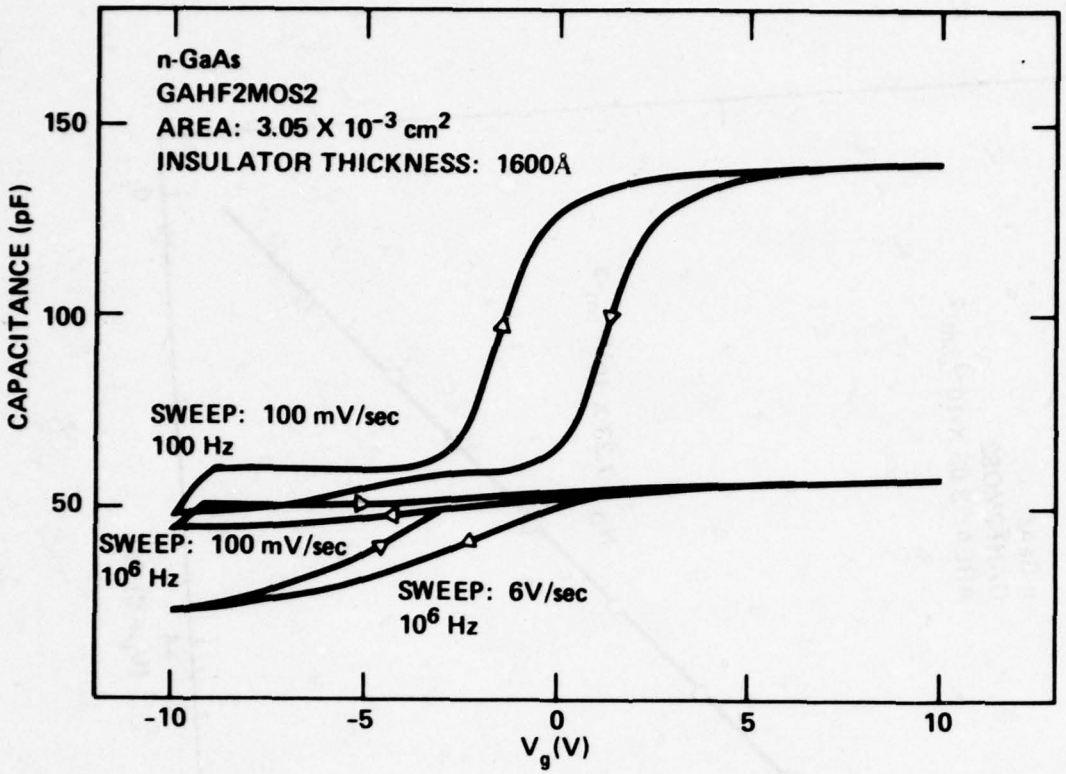


Figure 5.11 C-V characteristics of an anodized n-type GaAs MIS device measured with fast sweep rates; T = 300°K.

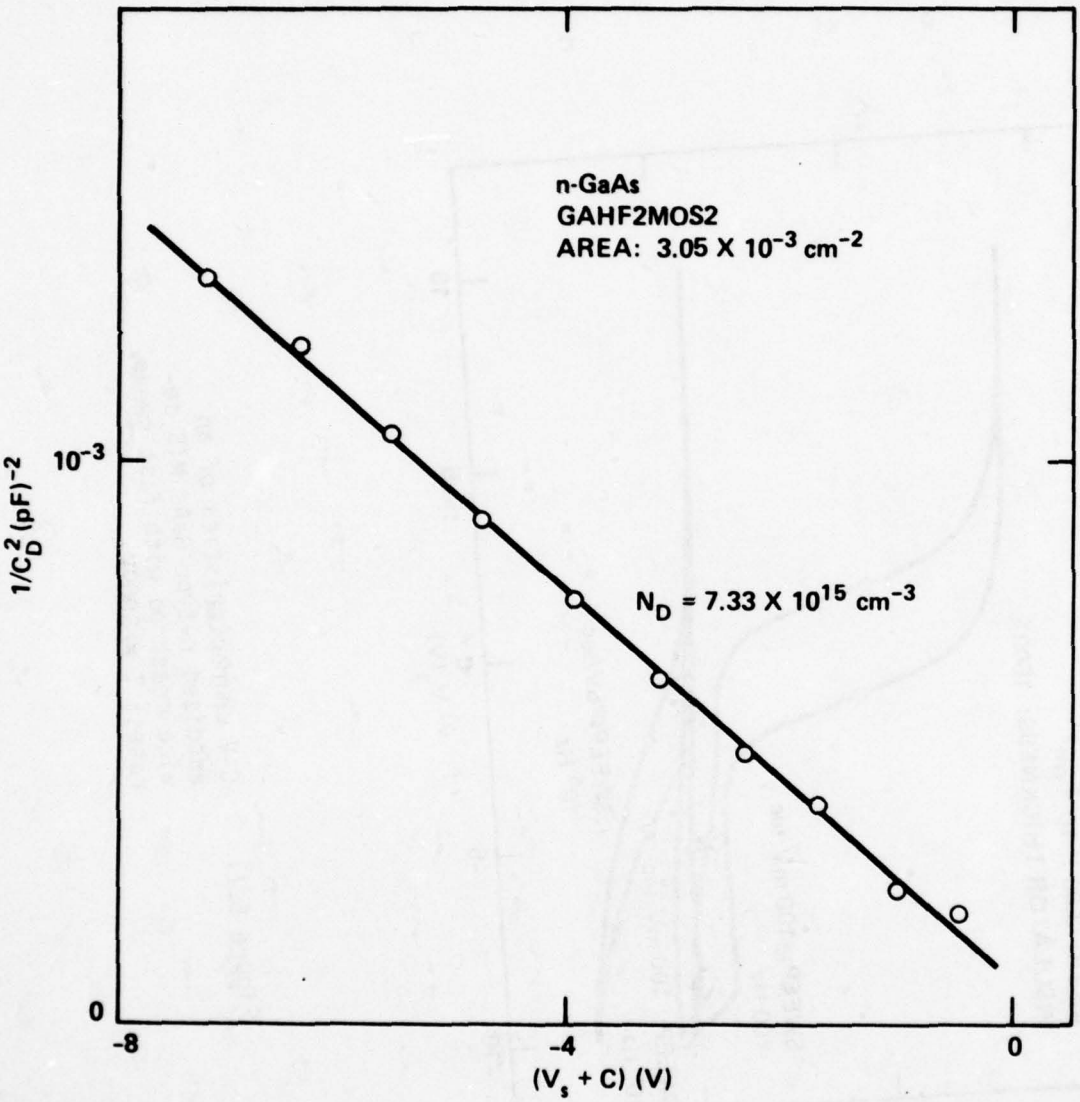


Figure 5.12 Deep depletion capacitance vs gate bias for the device of Figure 5.11; C is a constant term.

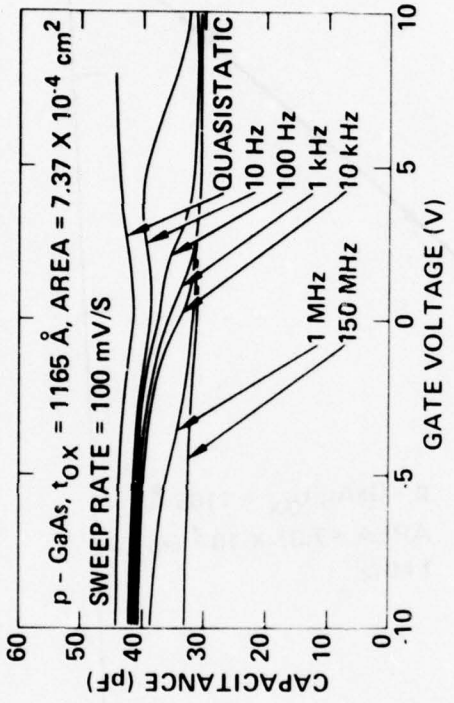


Figure 5.13 C-V characterics of an anodized p-type GaAs MIS device measured from DC to 150 MHz; T = 300°K.

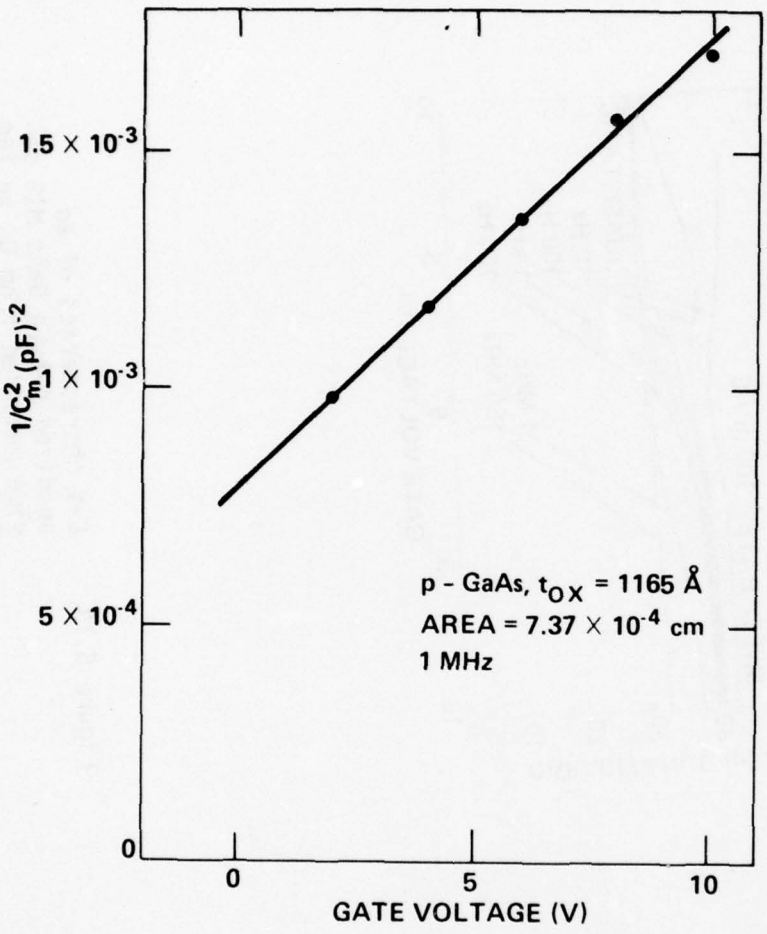


Figure 5.14 Deep depletion capacitance vs gate bias for the device of Figure 5.13; T = 300°K, sweep rate = 400 V/S.

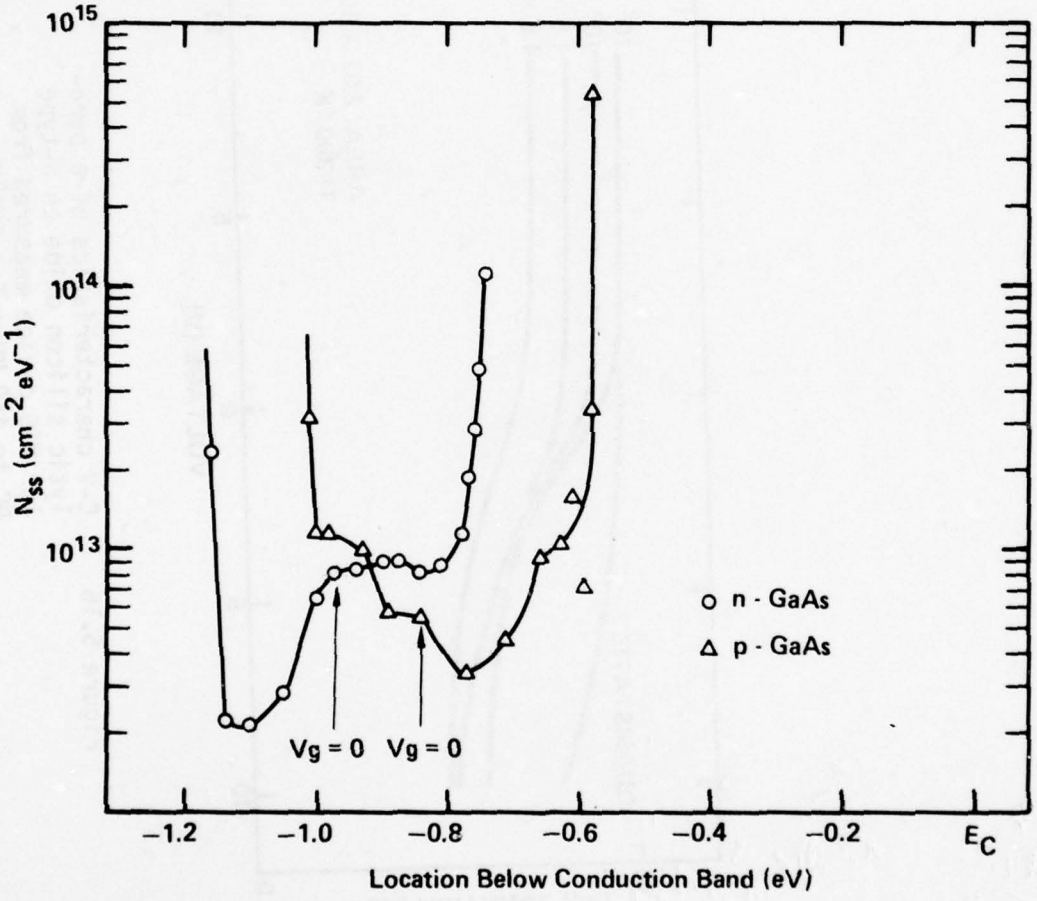


Figure 5.15 Surface state density of GaAs.

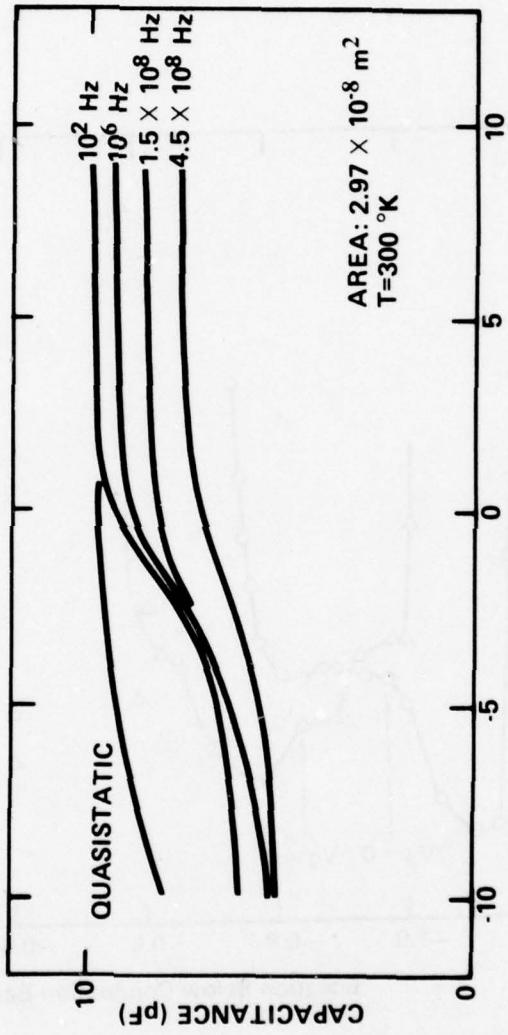


Figure 5.16 C-V characteristics of a pyrolytic silicon oxide on n-type InP MIS device measured from DC to 450 MHz; T = 300°K.

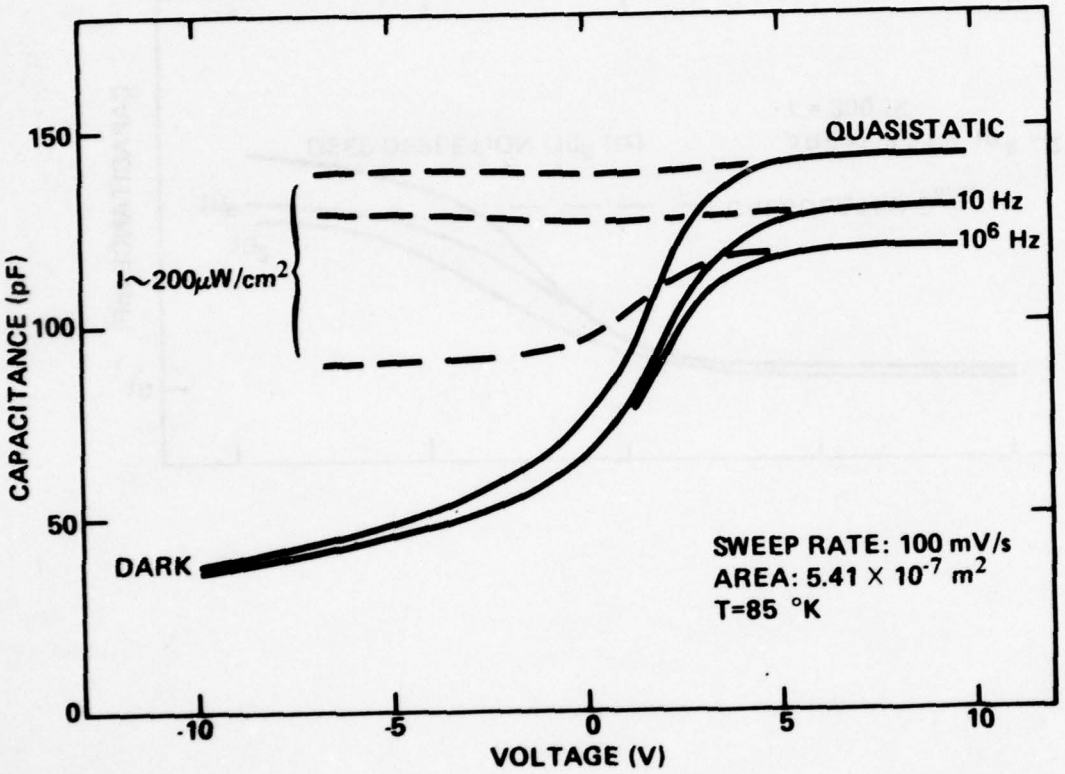


Figure 5.17 C-V characterics of a pyrolytic silicon oxide on n-type InP MIS device with and without illumination; T = 85°K.

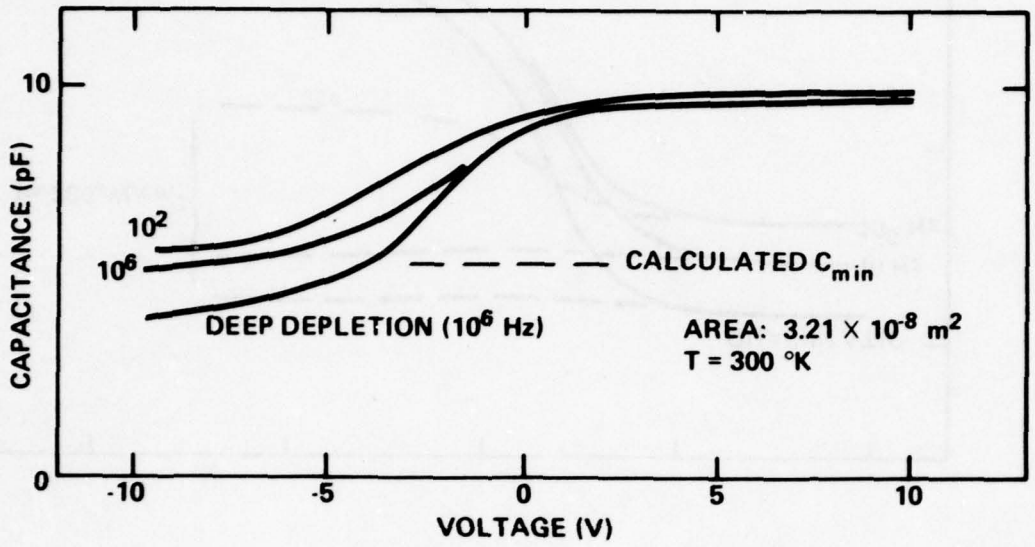


Figure 5.18 C-V characteristics of a pyrolytic silicon oxide on n-type InP MIS device measured with sweep rates of 100 mV/S and 400 V/S; T = 300°K.

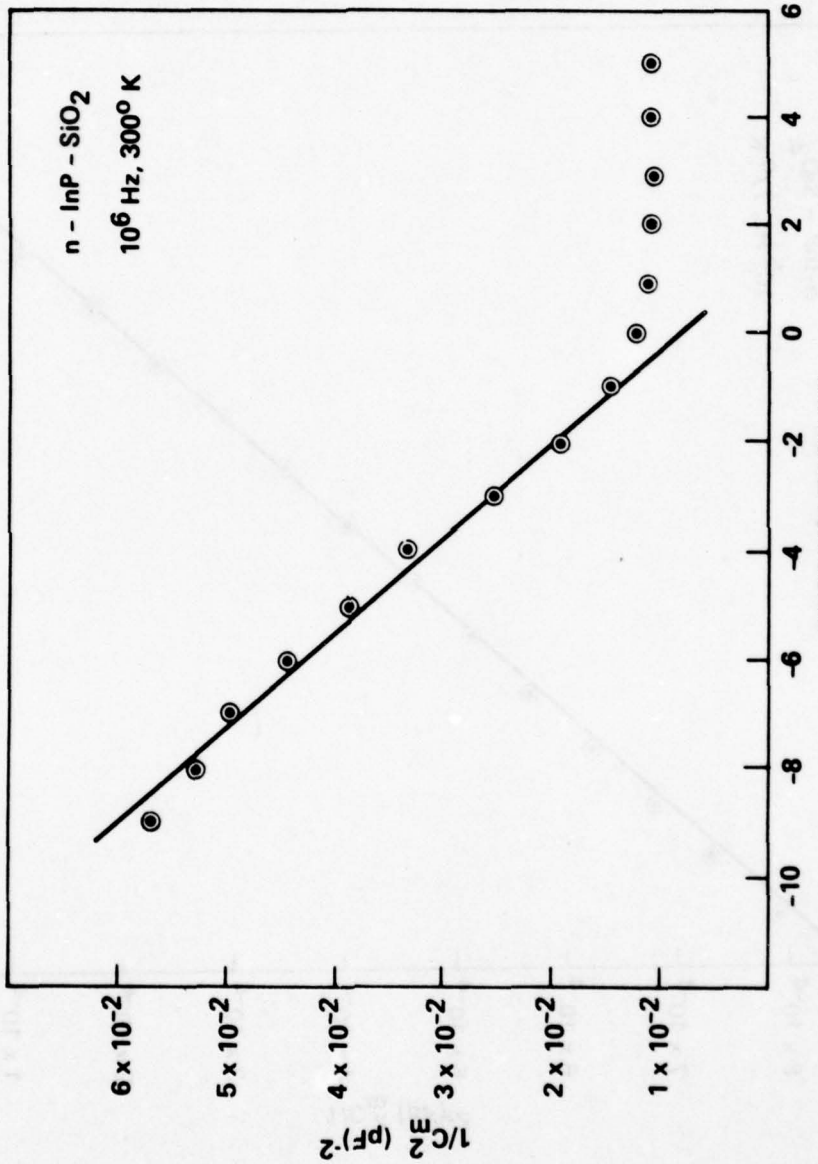


Figure 5.19 Deep depletion capacitance vs gate bias for the device of Figure 5.18.

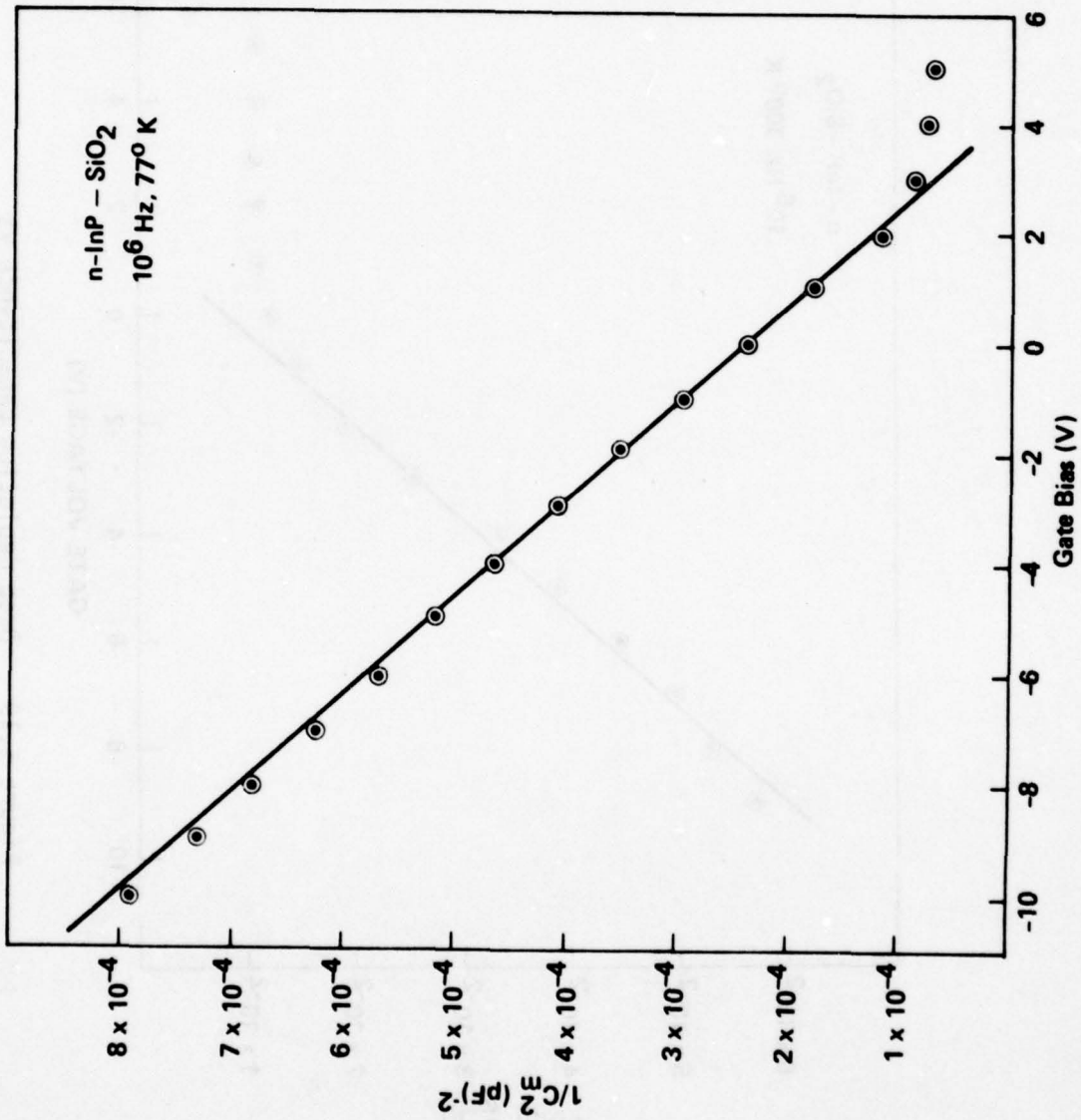


Figure 5.20 Deep depletion capacitance vs gate bias for the device of Figure 5.17.

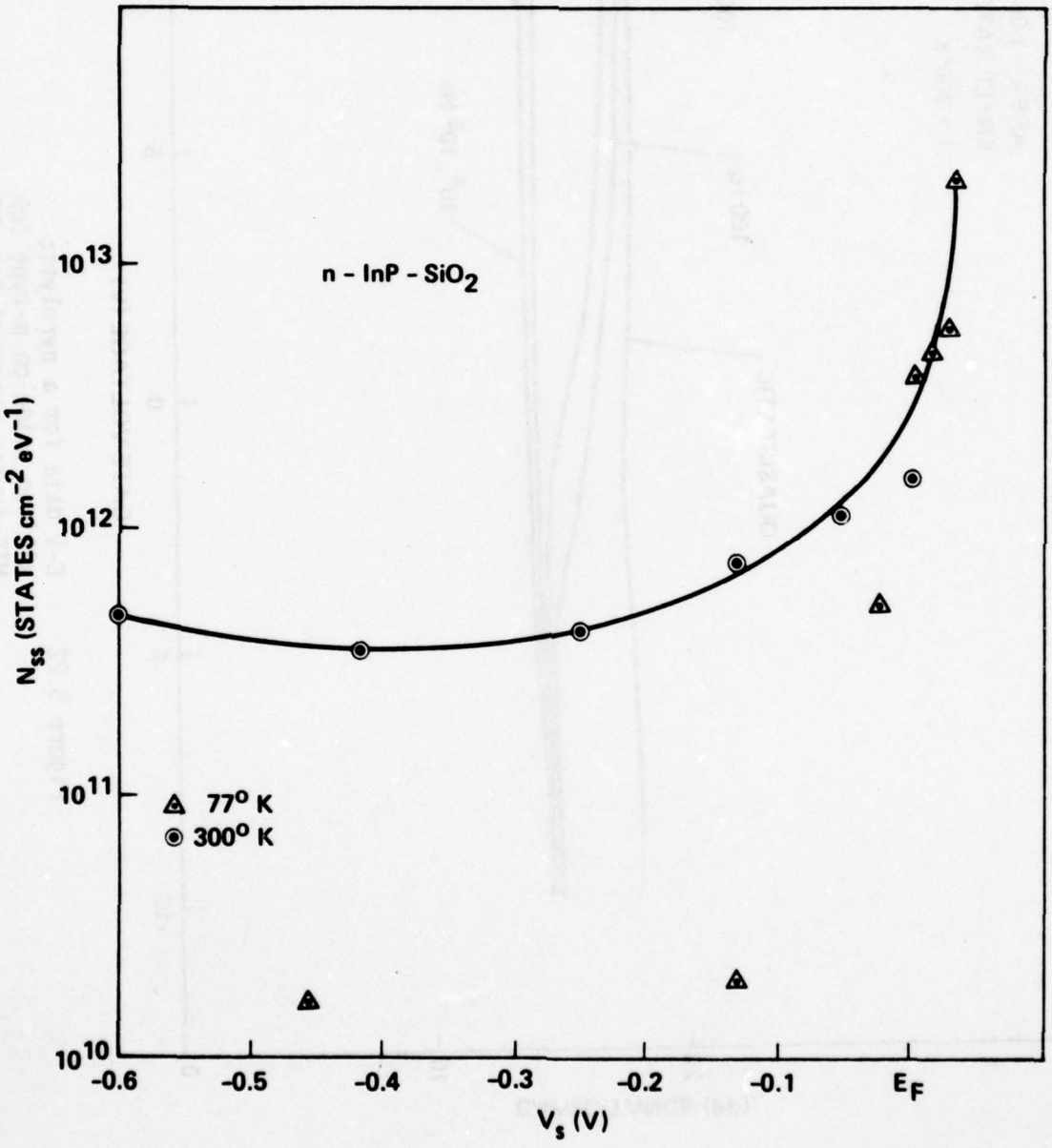


Figure 5.21 Surface state density of n-type InP coated with silicon oxide.

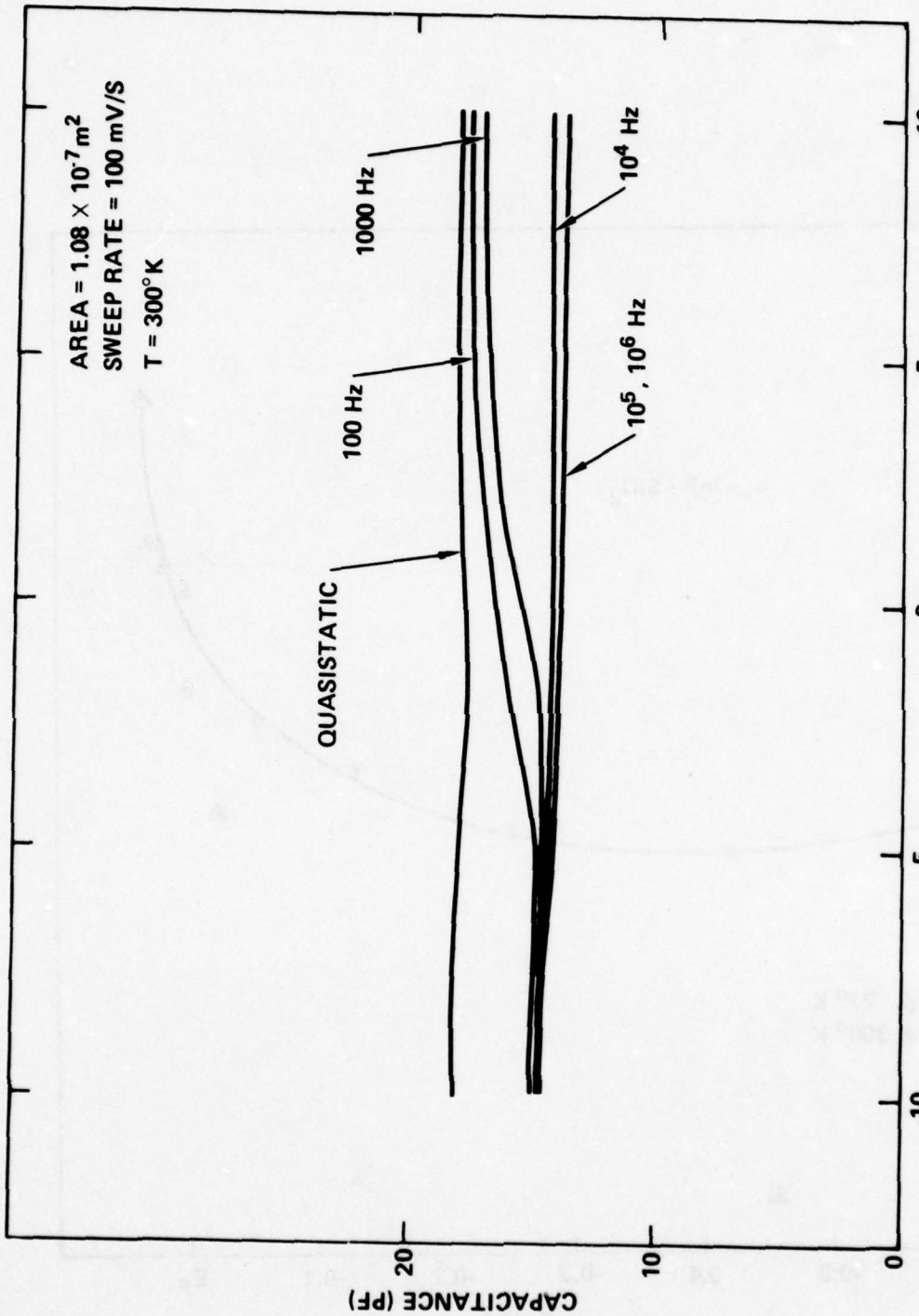


Figure 5.22 C-V data for a pyrolytic silicon oxide on p-type InP MIS device measured from DC to 1 MHz; T = 300°K.

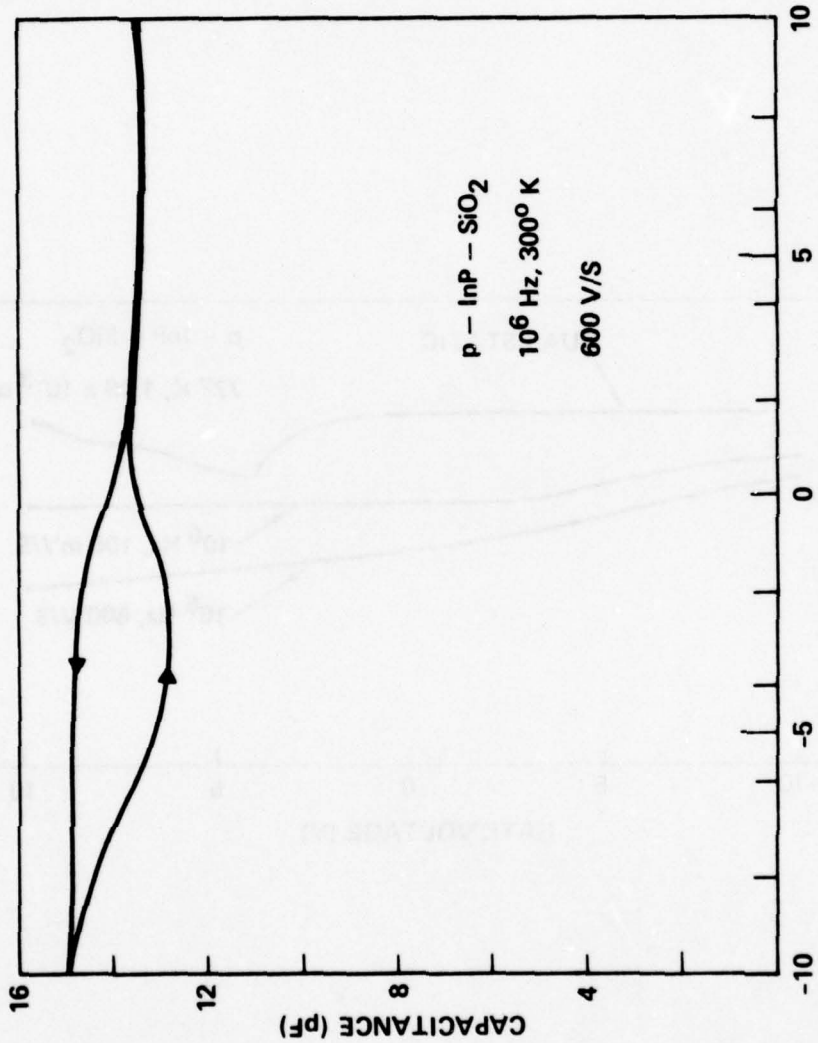


Figure 5.23 1 MHz C-V curve for the device of Fig. 5.22 measured with a gate bias sweep rate of 600 V/S.

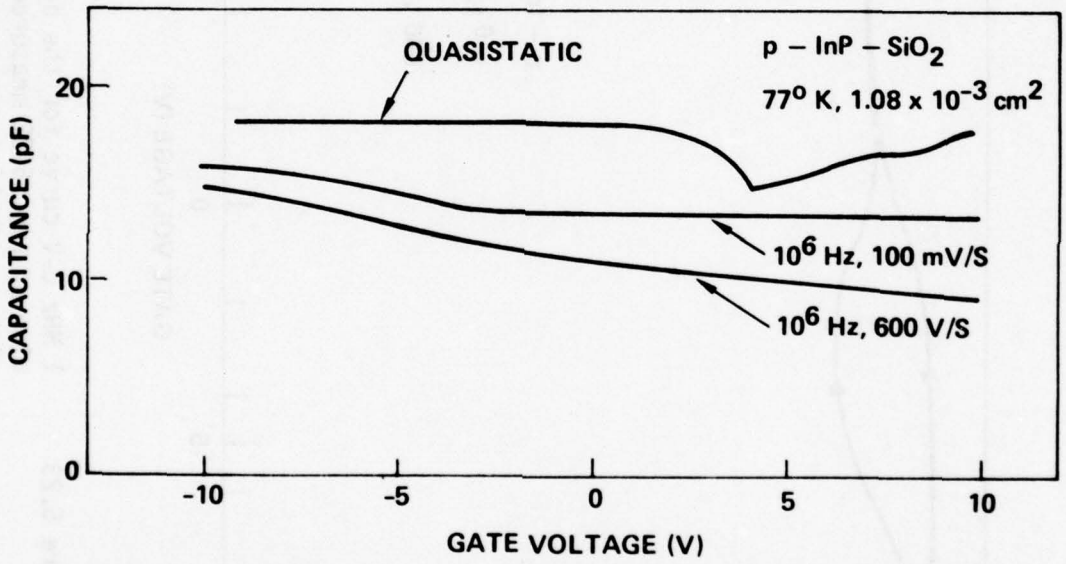


Figure 5.24 C-V data taken from DC to 1 MHz on a p-type InP-silicon oxide MIS device; T = 77°K.

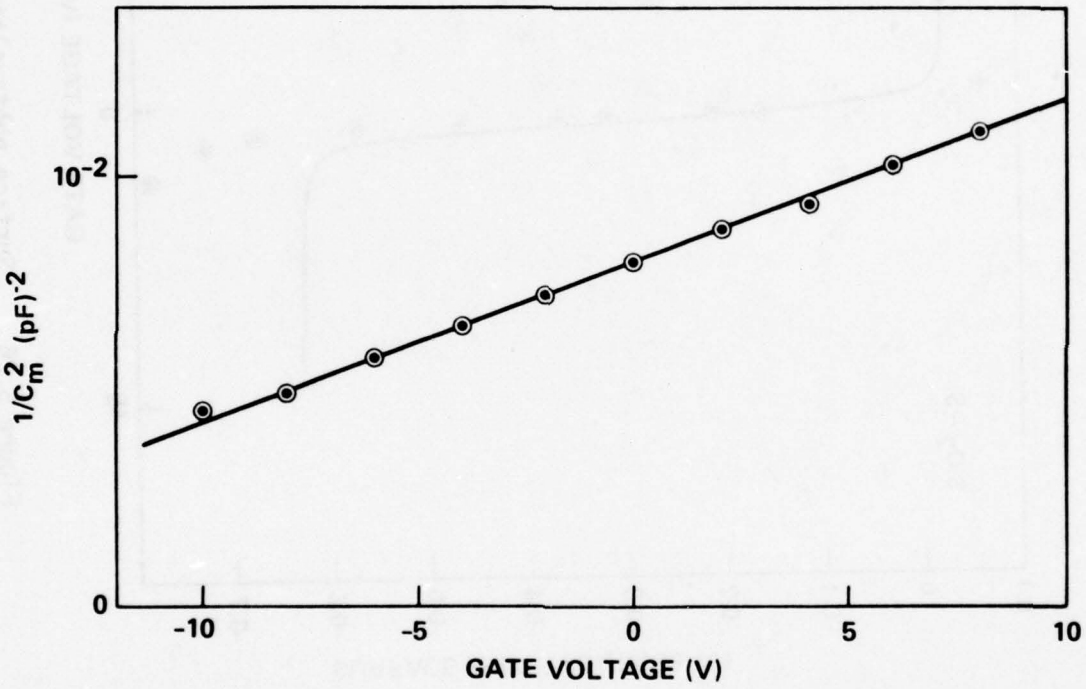


Figure 5.25 Depletion capacitance vs gate voltage for the device of Figure 5.24.

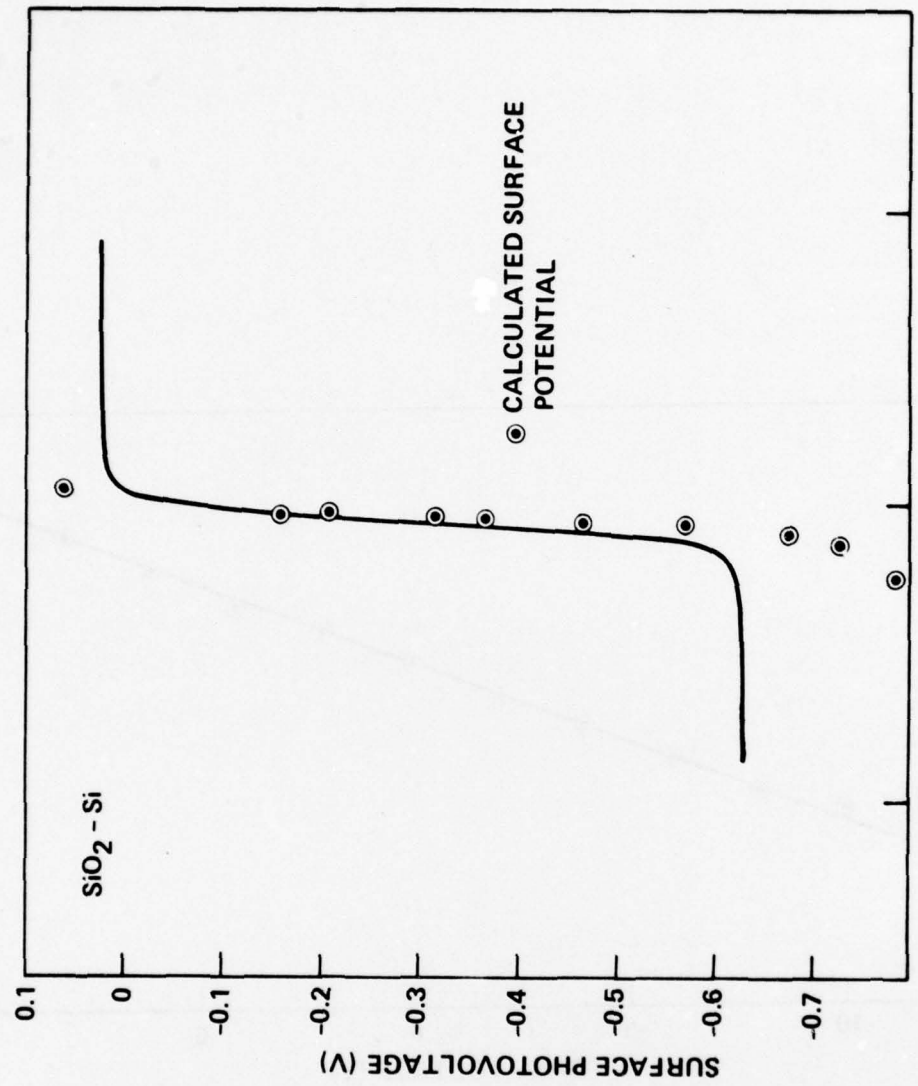


Figure 5.26 Surface photovoltage vs gate bias for a thermally oxidized n-type silicon MIS device.

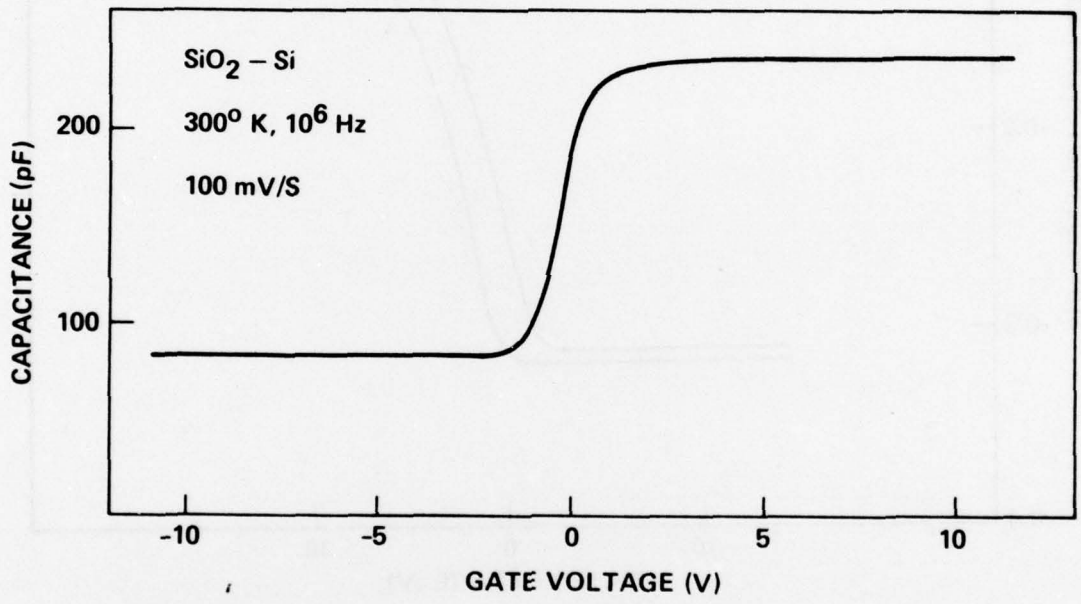


Figure 5.27 C-V characteristic for the device of Figure 5.26.

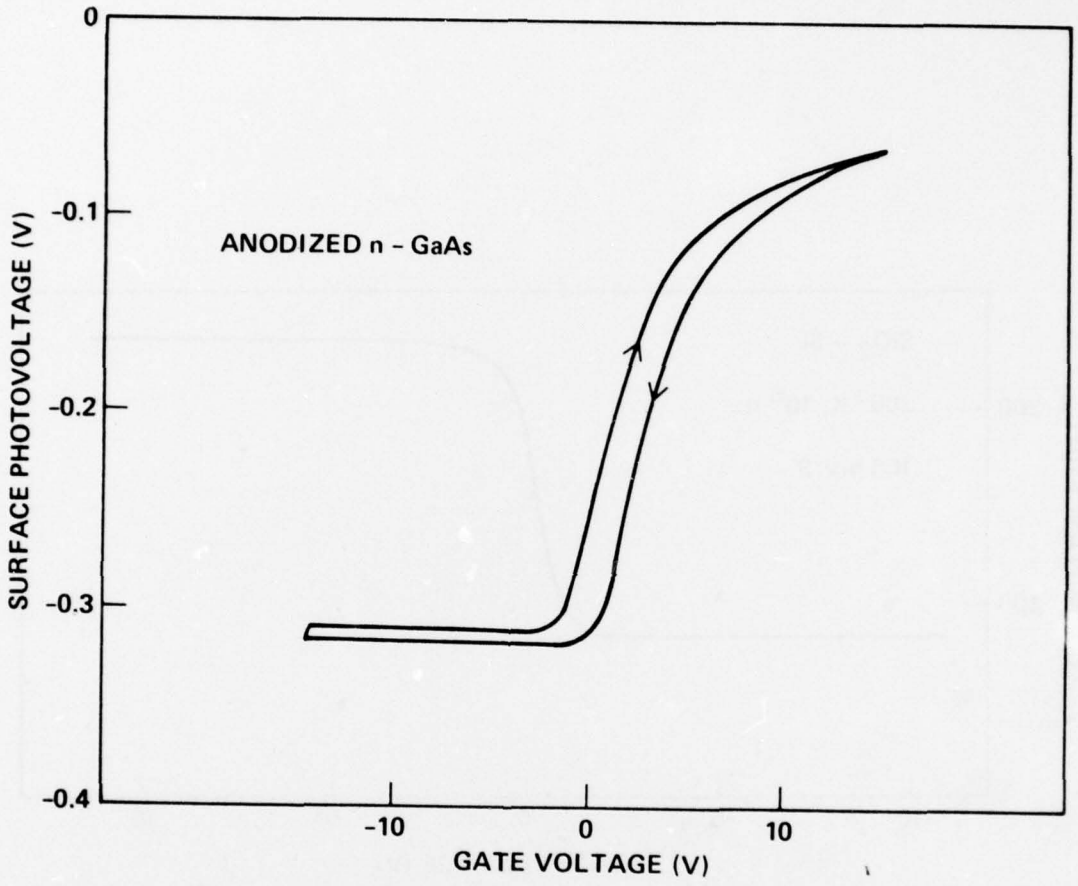


Figure 5.28 Surface photovoltage vs gate bias for an anodized n-type GaAs MIS device.

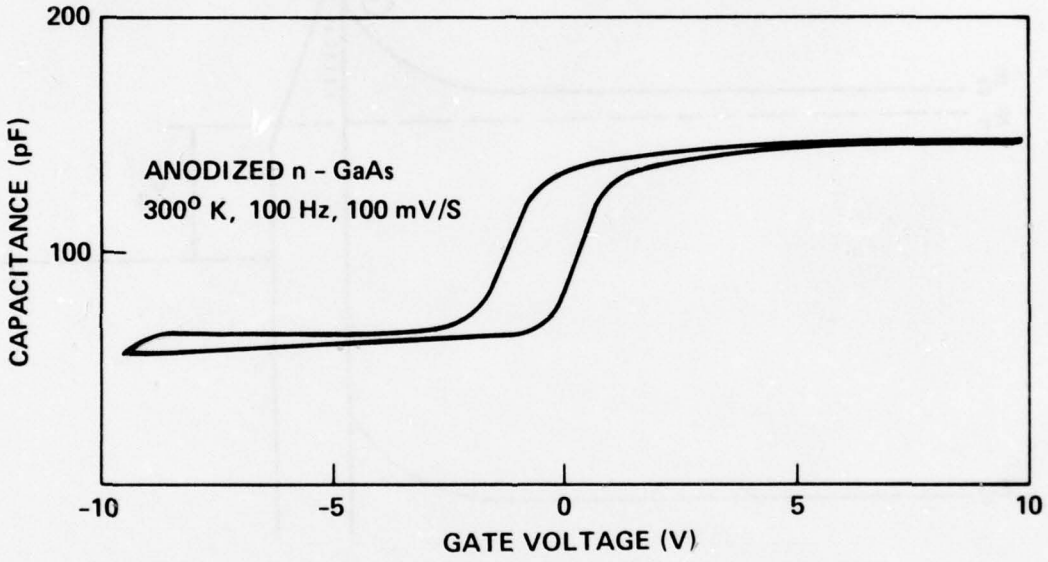


Figure 5.29 C-V characteristic for the device of Figure 5.28.

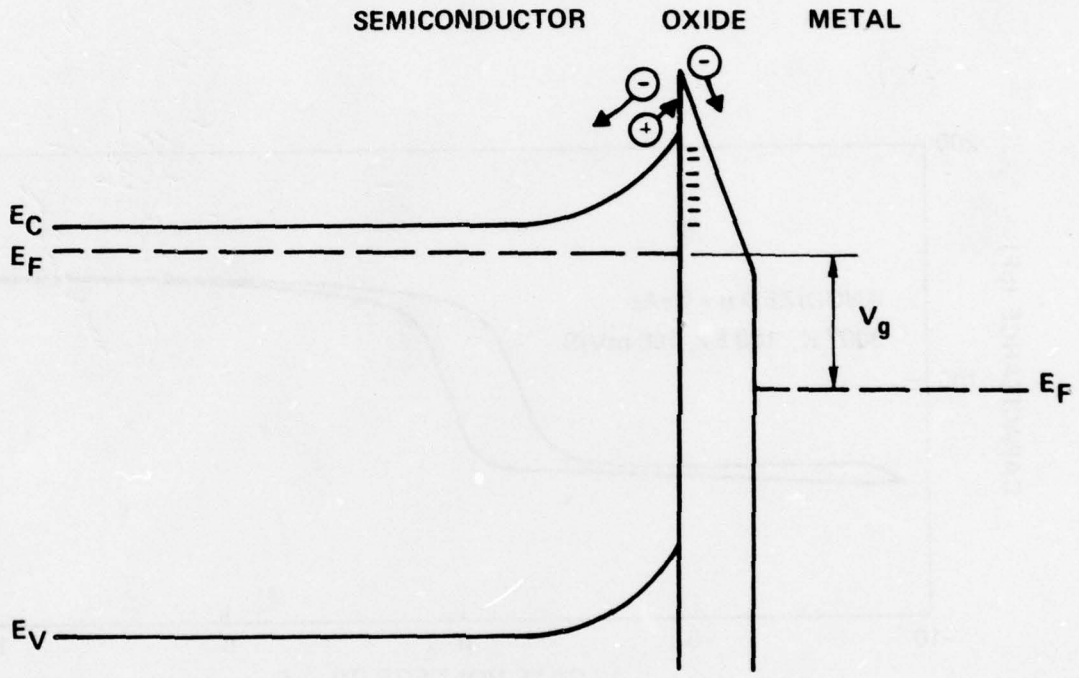


Figure 5.30 Energy band diagram for an MIS device with charge trapping in the insulator.

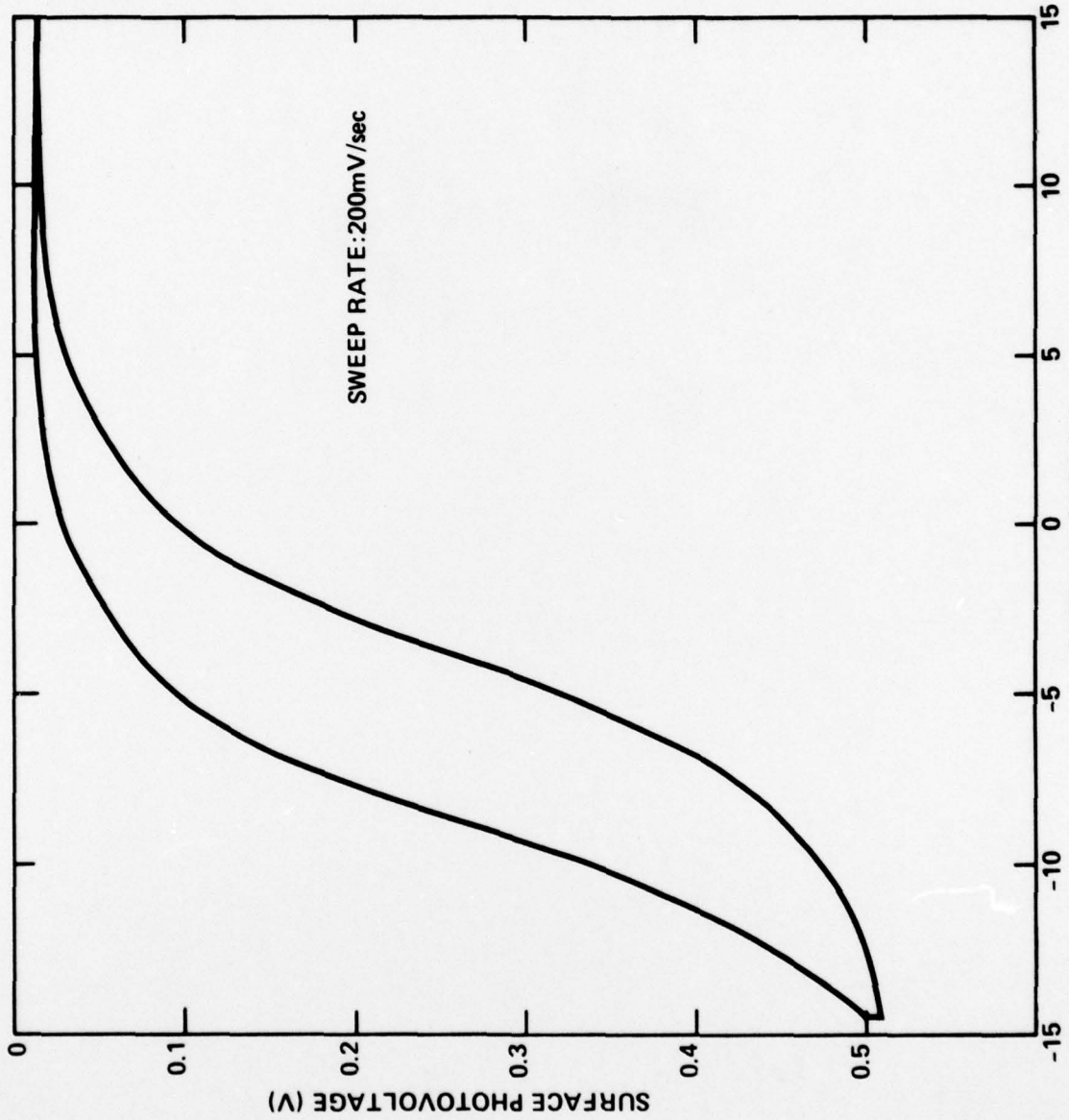


Figure 5.31 Surface photovoltage vs gate bias for a pyrolytic silicon oxide on n-type InP MIS device.

CHAPTER 6

CONCLUSIONS

The principal scientific question addressed by this thesis concerns the nature and properties of the dielectric-semiconductor interface of III-V compounds, specifically the degree to which the surface potential can be varied. The experimental data described in this thesis rely heavily on the experimental techniques and the analytical models developed for silicon metal-oxide-semiconductor (MOS) structures. A comparative study of III-V compound semiconductor MIS and silicon MOS structures employing capacitance vs. gate voltage augmented by surface photovoltage measurements and Schottky barrier investigations provide specific information on the surface potential, interface state densities, and their relation to fundamental band structure parameters.

The appropriate choice of measurement conditions usually permitted the MIS devices to be operated in a manner such that the depletion approximation could be used. From the deep depletion measurements the sample impurity density was obtained. Insertion of this experimentally-determined parameter into the analytical expressions for the surface capacitance and charge permitted comparison of the experimental and calculated capacitance vs. voltage curves. Discrepancies between these two results were explained in terms of a model which postulates a gate voltage dependent charge at the interface between the semiconductor and the dielectric layer. The quality of the interfaces measured has been discussed in terms of the total amount and the voltage dependence of this charge and in terms of the total surface potential variations that were observed. Ideally, of course, the amount of this interfacial charge would be equal to zero.

6.1 Gallium Arsenide

Measurements on both n- and p-type GaAs are consistent in that they indicate that the Fermi level is pinned somewhat below midgap and that variations in the surface electric field of $\pm 10^6$ V/cm produce a total change in the semiconductor surface potential of only $\sim$ 0.4 V. Both the n- and p-type GaAs surfaces studied in this investigation have remained in the depleted condition under all conditions of applied gate bias. A corollary to this result has been the realization that accumulations of neither electrons nor holes were observed on the surfaces studied. A plot of the surface state density for this material as shown in Fig. 5.15 illustrates that the minimum is $\sim 2\times10^{12}$ cm^{-2} eV^{-1} and that the surface state density rapidly rises to values above 10^{14} cm^{-2} eV^{-1} on each side of the minimum. At these large values the surface state density loses much of its utility as an indicator of the quality of the interface. A simpler model for the gallium arsenide interface is obtained by assuming the interfacial charge to be directly proportional to the voltage across the insulating layer. The proportionally constant was determined to be 3×10^{11} charges cm^{-2} V^{-1} and showed little change as the bias voltage was varied from - 10 V to 10 V.

The above results have added significance because the major features were independent of the manner in which the dielectric layers were prepared. Samples prepared by such drastically different procedures as anodization and sputtering differed only in that the surface states responded at frequencies in excess of 1 MHz for nearly all of the GaAs samples studied. However, the surface potential variations deduced from

C-V measurements made at 150 MHz agreed well with those obtained from quasistatic C-V data.

The result, that the interfacial properties of dielectric-semiconductor structures employing anodic, pyrolytic and sputtered dielectrics are substantially the same, clearly indicates that the properties are intrinsic to GaAs and not dependent on the specific properties of the dielectric employed. Workers[1] who have studied GaAs surfaces cleaved in ultra-high vacuum have found that the Fermi level, on a freshly-cleaved GaAs surface, is unpinned but that less than monolayer coverage by either metallic or oxygen atoms is sufficient to produce surface pinning. This result is certainly consistent with the conclusions of the present work. The suggestion seems to be that the surface pinning is caused by an intrinsic property of the surface rearrangement which occurs when a GaAs surface combines with foreign atoms. One must therefore conclude that dielectric layers, produced using the conventional techniques discussed above, offer little hope for the realization of a GaAs-insulator interface with no Fermi level pinning.

6.2 Indium Phosphide

The results on n-type indium phosphide samples coated with pyrolytic SiO_2 indicate that the surface is near flatband with no applied gate bias. Interpretation of the data is complicated by the frequency dispersion of the capacitance observed with the dielectrics investigated thus far, preventing a precise determination of the surface parameters in the accumulation region. The surface state density increased from 4×10^{11} cm^{-2} eV^{-1} at a point 0.6 eV below the conduction band edge to 2×10^{12} cm^{-2} eV^{-1} at

flatband. The data obtained on both p- and n-type material indicates that accumulation of electrons could be produced at the surface. The C-V data on the n-type samples indicate that inversion was achievable; however, data obtained on the p-type material indicate that for practically attainable electric fields neither flatband nor accumulation were reached. This apparent discrepancy obviously needs to be resolved by further study.

The data presented in this thesis indicate that the InP surface differs from that of GaAs in two important respects:

(a) the surface potential variation of $\sim$ 1 V obtainable for InP with surface electric fields of $\pm 10^6$ V/CM is much larger than that observed on GaAs;

(b) although the surface potential is to some degree pinned by the surface electron traps near the conduction band edge, it is near flatband for zero gate voltage at room-temperature on the n-type material rather than the midgap-pinning observed on GaAs.

Thus relatively small applied electric fields are needed to produce surface accumulations of electrons in InP.

6.3 Suggestions for Further Work

Seemingly the most fruitful area of study for MIS devices on the III-V semiconductors at the present time centers on InP. The fact that inversion layers have already been observed on p-type MIS devices[2] is very encouraging. These layers obviously need to be studied in detail. The carrier mobilities and densities are among the first parameters that need to be determined. This information is of especial importance to the development of FETs using

the MIS approach. If the carrier mobilities in the inversion layer are significantly higher than those observed on silicon, then MIS integrated circuits which operate at higher frequencies may be feasible. Undoubtedly quantum transport effects will be observable in these layers which should provide additional information on the conduction band structure of InP.

The frequency dispersion in the capacitance measurements with positive gate bias prevented the determination of the surface parameters in the accumulation region on the n-type InP samples. This problem might be avoided by conducting measurements on metal-oxide-metal capacitors with dielectrics formed under the same conditions as those on simultaneously-prepared MIS structures. In this way it may be possible to better separate those effects due to the dielectric and those due to the interfacial charge.

The question of whether or not the n-InP MIS structures may be biased into inversion needs to be resolved. Conclusive evidence of this would be observation of gate modulable conduction in an inversion layer on an n-type substrate.

6.4 References

1. W. E. Spicer and P. E. Gregory, CRC Crit. Rev., Solid-State Sci., 5, 231(1975).

2. D. L. Lile, D. A. Collins, L. G. Meiners and L. Messick, Electron. Lett., 14, 657(1978).

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