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LIGHT EMITTING DIODES FOR FIBER OPTIC COMMUNICATIONS.(U)

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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING
PROGRAM QUARTERLY TECHNICAL REPORT

Contract Number DAAB07-76-C-8135

LIGHT EMITTING DIODES FOR FIBER OPTIC COMMUNICATIONS

Prepared By:

LASER DIODE LABORATORIES, INC.
205 Forrest Street
Metuchen, New Jersey 08840

Fifth Quarterly Report
for the Period 1 October 1977 to 31 December 1977

Approved for public release; distribution unlimited.

Placed By:

U. S. Army Electronic Research and Development Command
Fort Monmouth, N. J. 07703

MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING PROGRAM QUARTERLY TECHNICAL REPORT

(5)

Contract Number (15) DAAB07-76-C-8135

(6) LIGHT EMITTING DIODES FOR FIBER OPTIC COMMUNICATIONS.

(12) 35 p.

Prepared by:

(10) Albert Gennaro
Product Development Manager

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205 Forrest Street
Metuchen, New Jersey 08840

(11) 1977

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for the Period 1 October 1977 to 31 December 1977,

This project has been accomplished as part of the Army Manufacturing and Technology Program, which has as its objective the timely establishment of manufacturing processes techniques or equipment to insure the efficient production of current or future programs.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design and fabrication of high speed etched-well light emitting diodes for fiber optic communications is discussed with regard to materials synthesis via LPE, wafer fabrication, and device assembly in a manufacturing environment.

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SECTION I

INTRODUCTION

The primary objective of this Manufacturing Methods and Technology Engineering Program is twofold. First, the manufacturing methods and techniques necessary for the volume production of the light emitting diode for use in fiber optic communications as outlined in Specification SCS-511 must be developed and implemented to insure the highest degree of device quality and reliability at a reasonable cost. Secondly, verification of device performance and quality for LED's produced in a volume manufacturing environment must be carried out by means of rigorous testing and evaluation in accordance with SCS-511 in order to demonstrate the technical adequacy of the manufacturing methods developed under this contract.

The major objective for the fifth quarter of the program include completion of 2000 hour life testing, delivery of second engineering samples from the completed life test group, establishment of an alternative fiber as a result of a request for change, start of re-design of the zinc diffusion furnace, and process change in the photolithography procedure.

SECTION II

MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING

2.1 Wafer Processing for Etched Well Light Emitting Diode Chip Fabrication.

By increasing the thickness of the 'n' blocking layer, it has been possible to allow room for the zinc diffusion without washing out the current confining contact dot. Lot Bur-B-48 was processed in this manner and has produced good results. Table 1 contains sample data on Lot Bur-B-48. Of particular significance is the uniformity of the forward voltage, a direct result of the zinc diffusion process. Included in the table for comparison is data on a non diffused lot, Lot But-B-20, which was processed early in the program. Although the diffusion process has yielded good results, run to run consistency is not good. In order to improve the run consistency and achieve predictability, the system is being re-designed. The most critical step in the process is the inner ampoule-ball sealing at the start of the process. At present this is accomplished in the hot furnace practically out of visual range and at best is a sometime successful step. This fault will be corrected by providing a sliding furnace which can be moved over the inner ampoule area after the seal has been completed and checked visually. The sliding furnace allows the seal to be made before the heating process begins, and by the same token by removing the furnace from the

TABLE 1. Forward Voltage, V_f.

DATE TIME		V_f (volts) @ 20 ma	V_f (volts) @ 100 ma										
1		1.40	1.70										
2		1.41	1.72										
3		1.43	1.70		LOT BUR-B-48								
4		1.40	1.70										
5		1.42	1.71										
6		1.40	1.70										
7		1.40	1.70										
8		1.42	1.72										
9		1.42	1.73										
10		1.42	1.73										
1		2.60	4.00										
2		2.50	3.60										
3		2.50	3.60										
4		2.60	3.90		LOT BUT-B-20								
5		2.60	3.90										
6		2.80	3.90										
7		2.50	4.00										
8		2.80	3.90										
9		2.80	3.90										
10		3.00	4.00										
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diffusion area, allows the inner ampoule to cool before breaking the seal. Figure 1 illustrates this technique. In addition, a dry box will be attached to the system to allow loading the system under low humidity and low contamination conditions, while providing a safe work environment.

A process change has been made in the photolithographic technique to protect resist coated wafers during handling. The resist protective coating (RPC) process is as follows:

> Dissolve 16.2 gr of polyvinyl alcohol in 2700 ml of DI water at 45° ± 5°C. Add 300 ml of isopropyl alcohol containing 0.3 gr of glyceryl monostearate and 1.5 gr of triton X-100. The solution is mixed well and filtered. Standard photo-resist procedures are used to resist coat the wafer. The RPC is spun on to cover the resist and then baked for 20 minutes at 100°C. Standard techniques are used to align and expose the coated wafer. The RPC is removed by a room temperature soak in water for 10 minutes. The wafer can now be developed.

The very thin RPC coating serves to protect the resist during insertion and removal of the wafer with respect to the hinged mask set. Improved pattern definition, fewer pin holes, and minimum tearing are the results of the use of the RPC coating. A peristaltic pump has replaced the conventional plastic impeller type pump

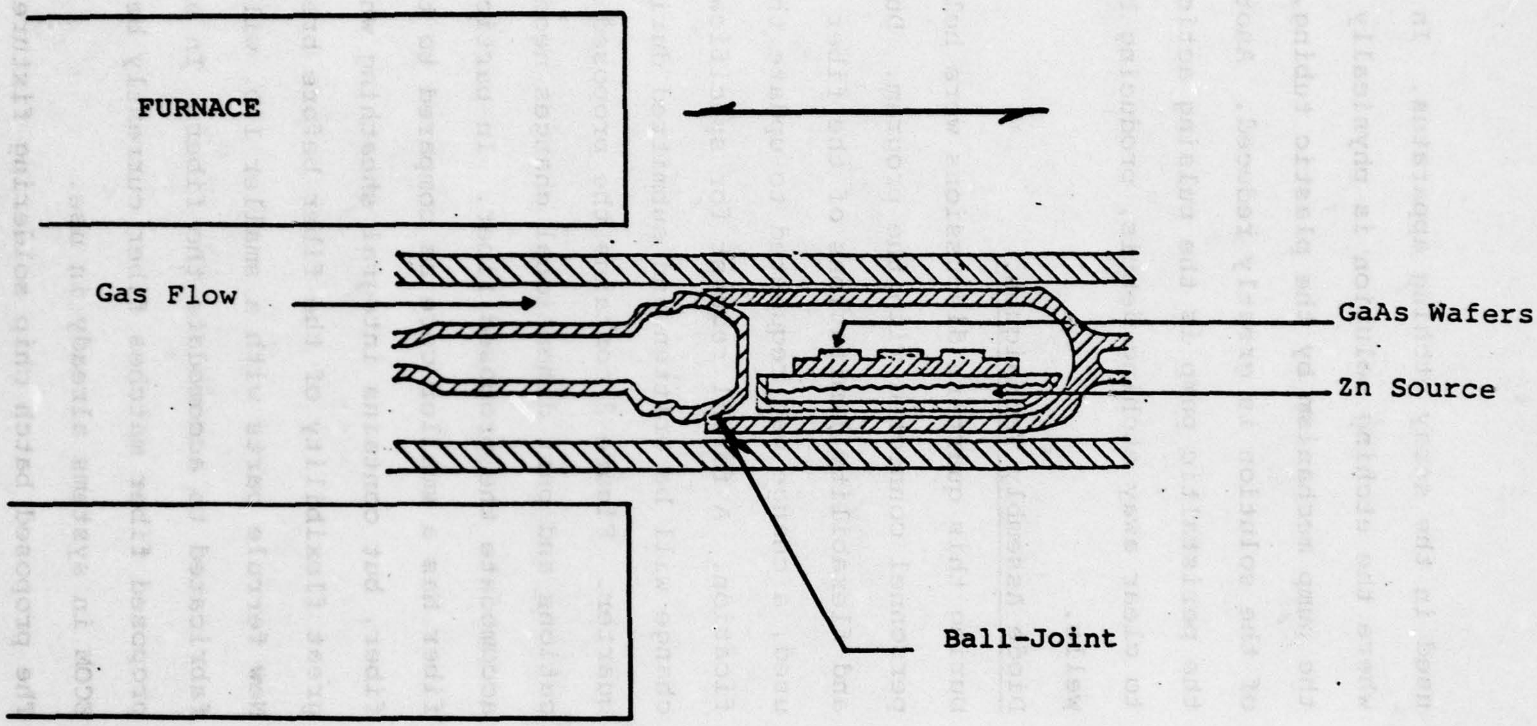


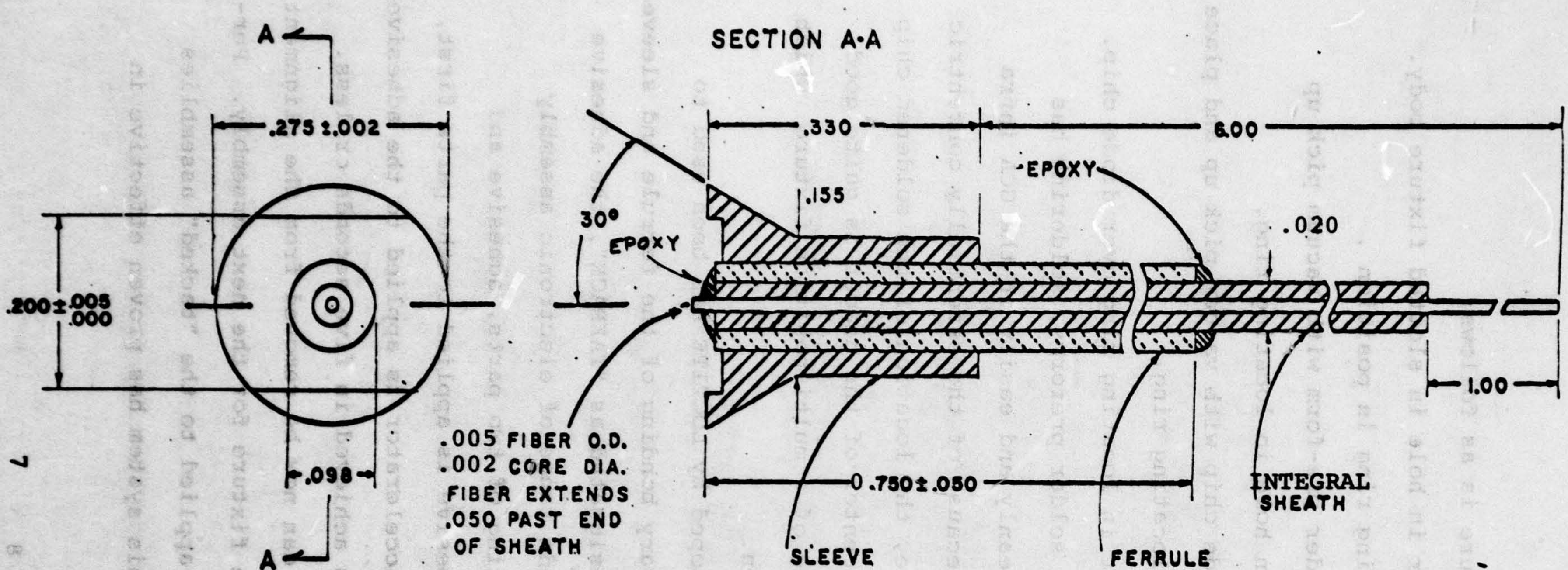
Figure 1. Sliding Diffusion Furnace.

used in the spray etching apparatus. In this pump, where the etching solution is physically isolated from the pump mechanism by the plastic tubing, contamination of the solution is greatly reduced. Another feature of the peristaltic pump is the pulsing action which helps to clear away etching debris, producing better defined wells.

2.3 Diode Assembly Techniques.

During this quarter, discussions were held with ECOM personnel connected with the program. Due to fabrication, and flexability limitations of the fiber currently being used, a change was requested to update the fiber specification. A formal request for specification and program change will be written and submitted during the next quarter. Figure 2 contains the proposed fiber specifications and part dimensional changes necessary to accomodate the proposed fiber. In particular, this fiber has a smaller core as compared to the current fiber, but contains integral sheathing which allows great flexibility of the fiber before breakage occurs. New ferrule parts with a smaller I.D. will need to be fabricated to accomodate the fiber. In addition, the proposed fiber matches fiber currently being used by ECOM in systems already in use.

The proposed batch chip soldering fixture was implemented in the form of a two position fixture for test purposes. Figure 3 shows the fixture body, locating ring, and weight in the disassembled configuration. The procedure



FIBER CHARACTERISTICS

CHARACTERISTICS	MIN.	MAX.	UNIT
ATTENUATION (AT λP) (8200Å)	–	50	db/km
CORE DIAMETER	–	62.5	um
CLADDING DIAMETER	125	–	um.
PROTECTIVE JACKET DIAMETER	500	–	mm
NUMERICAL APERTURE (N.A.)	–	0.3	–
TENSILE STRENGTH	50	–	NEWTONS
BENDING RADIUS	5	–	mm

LDT 177 FIBER ASSEMBLY

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Figure 2. LED Fiber-Ferrule Assembly with Support Sleeve.

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for loading the fixture is as follows:

1. Place header in hole in slotted fixture body.
2. Place locating ring in position .
3. Pick up solder pre-form with vacuum pick up and place in hole in locating ring.
4. Pick up diode chip with vacuum pick up and place in hole in locating ring.
5. Place weight in locating ring over diode chip.

Using 60-40 lead-tin solder preforms, soldering has been accomplished cleanly and easily in the GCA infra red belt furnace. Because of the essentially concentric design of the fixture, the location of the soldered chip with respect to the center of the header is quite good. Figure 4 is a drawing of a multi-position fixture which is under construction.

A new adhesive developed by LOCTITE has been used to effect a fast temporary bonding of the ferrule and sleeve during assembly. Designated as "TAKPACK", the adhesive is designed for a wide range of electronic assembly operations. Consisting of two parts, adhesive and accelerator, the adhesive is applied to the parts first, and then a drop of accelerator is applied to the adhesive. Handling strength is achieved in five seconds or less. The bonded assembly can now be removed from the alignment fixture, freeing the fixture for the next assembly. Permanent epoxy can be applied to the "tacked" assemblies at a later time. This system has proven effective in

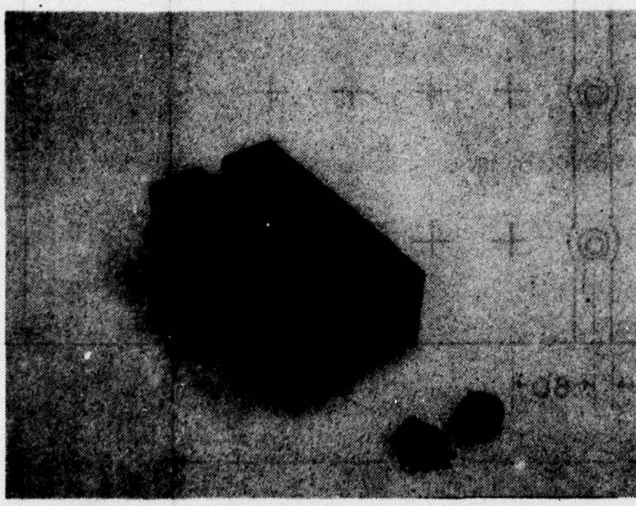

Figure 3. Chip Soldering Fixture.

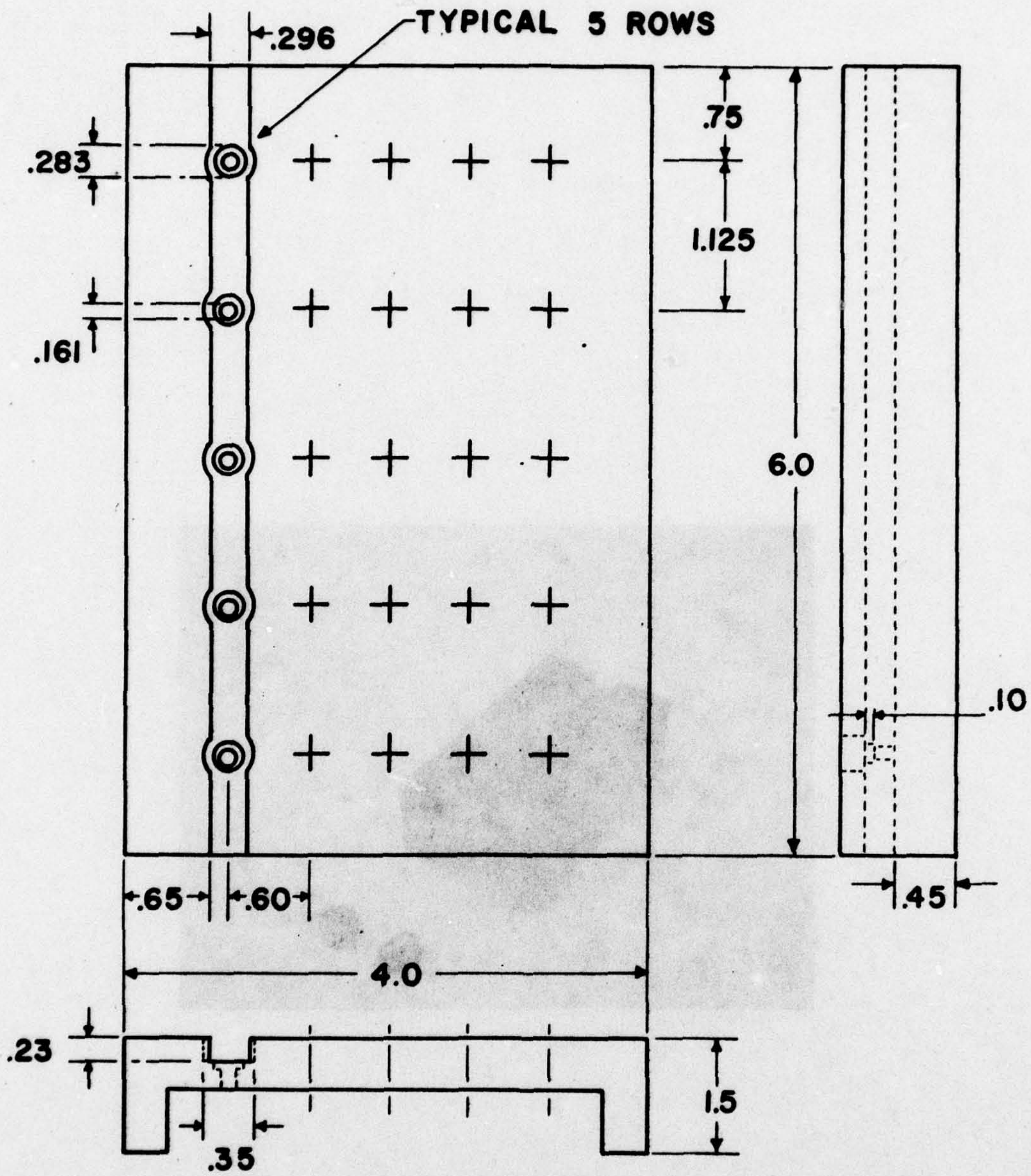

Fig.4 LDL-11 SOLDERING FIXTURE

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increasing the thru-put at the assembly operation.

2.4 Device Evaluation and Testing.

2.4.1 Device Evaluation.

Table 2 contains data on lot Bur-B-42, which has completed 2176 hours of life testing, and will be supplied as the second engineering sample. Figure 5 is an actual chart recorder plot of small signal Dynamic Linearity. The diode has a 1 MHZ signal applied and detected by a PIN diode. The signal from the PIN diode is fed to a Hewlet Packard Spectrum Analyser. In slow scan mode the spectrum analyser is output to the chart recorder producing the plot in Figure 5. This plot is representative of the lot. As an added check on linearity, Figure 6 is a "static linearity" plot. What is illustrated here, is, that the thermal characteristics of the device are very good, and little distortion or fall off is introduced to the device under high dissipation static conditions. The curve as recorded is a very good approximation to a straight line, an indication of good linearity. Figure 7 is the circuit diagram for use in the small signal dynamic linearity measurement. C_{IN} and R_L are chosen to meet the input impedance of 50 Ω, and bandwidth of 1 MHZ and up. The circuit permits driving LED's with combined D.C. and A.C. modulation, and is capable of highly linear operation. Figure 8 is a chart recording of rise and fall time. The light output trace shows rise and fall times on the order of 15 ns, which is typical for this lot. Figure 9 is the test circuit used for this measurement. R_x and R_s suppress parasitic oscillation due to negative resistance in the emitter follower. Values will be between 10 Ω and 100 Ω. C_s may be inserted for speed up and has a value between 2 to 20 pf. C_p should be 0.1 μf or greater, and be non inductive. Current through the LED is determined by -V, R_E, and V_R. In operation the circuit switches the main current from one transistor to the other effectively turning the LED on and off. Rise and fall times for the circuit are in the 5 ns region. A Tektronix CT-1 current probe is used to monitor the current.

2.5 Test Equipment.

2.5.1 Life Testing.

During this quarter, 2000 hour life was completed on Lot Bur-B-42. These devices were constructed with standard parts which comply with the SCS-511 dimensional outline. Table 3 lists data at the start of life, at the first down period of 176 hours, and at the end of life testing. The end of life testing data meets the requirements of SCS-511 in that the power output at 2176 hours has not decreased from the 0 hour reading by more than 5%. The second engineering sample will be supplied from this life test group.

TABLE 2. Second Engineering Samples - Lot BUR-B-42

	P_O (mw) @ 100 ma	λp (nm)	V_f (volts) @ 20 ma	V_f (volts) @ 100 ma	V_R (volts) @ 10 μa	Linearity - db
DATE						
TIME						
#						
1	.550	820	1.43	1.70	6.0	35
2	.530	815	1.41	1.72	3.5	36
3	.560	805	1.40	1.70	3.5	37
4	.580	825	1.42	1.72	6.0	35
5	.500	830	1.42	1.75	5.5	38
6	.670	828	1.40	1.70	4.5	37
7	.490	818	1.41	1.72	3.0	36
8	.520	830	1.41	1.70	5.5	35
9	.540	805	1.40	1.71	4.0	37
10	.480	810	1.42	1.71	3.0	38
11	.480	820	1.43	1.73	3.8	39
12	.490	825	1.40	1.70	4.6	36
13	.540	820	1.41	1.71	5.5	38
14	.510	817	1.42	1.73	5.0	37
15	.560	815	1.40	1.70	4.5	36
16	.570	820	1.40	1.70	6.0	36
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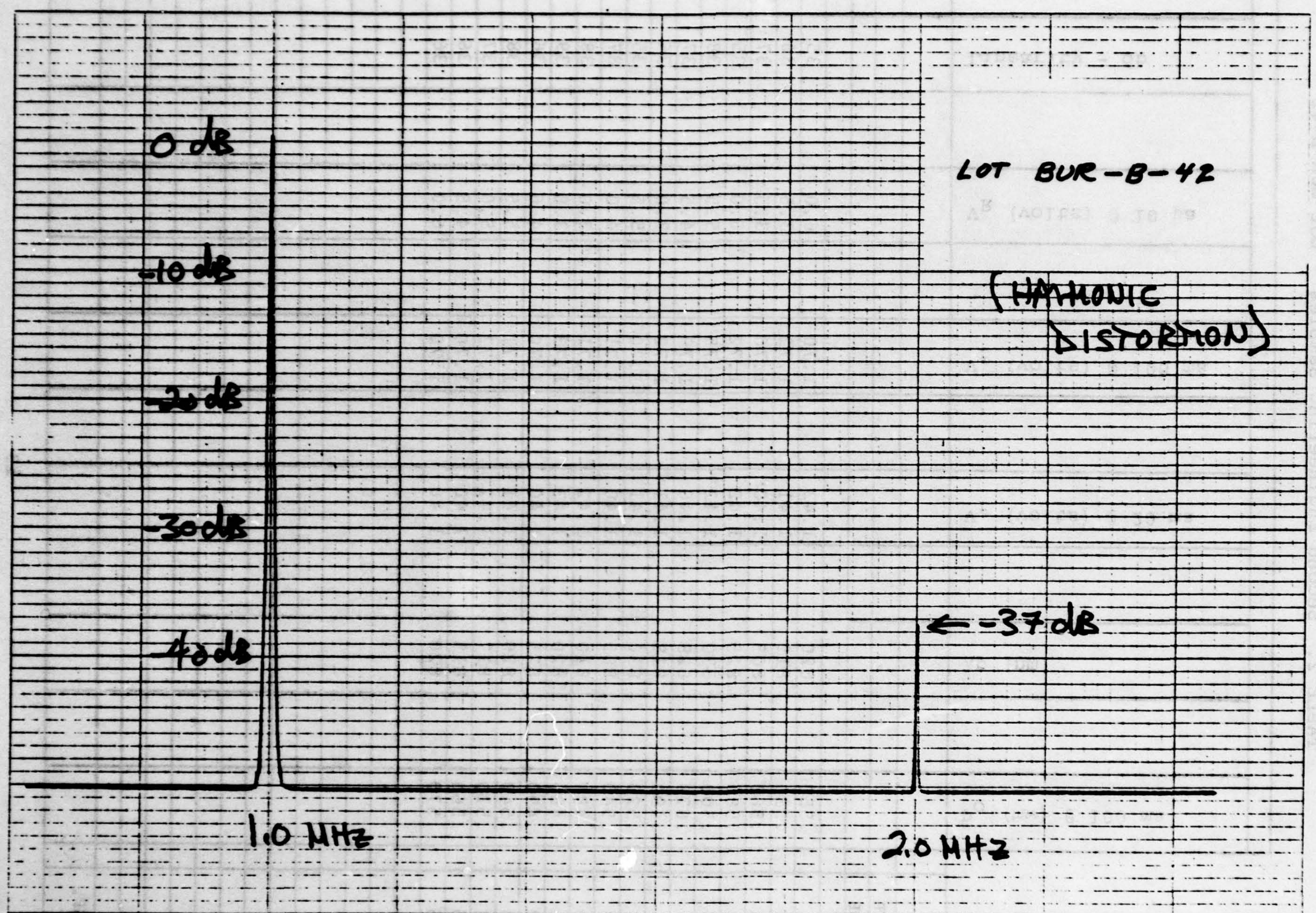


Figure 5. Linearity (Small Signal Dynamic).

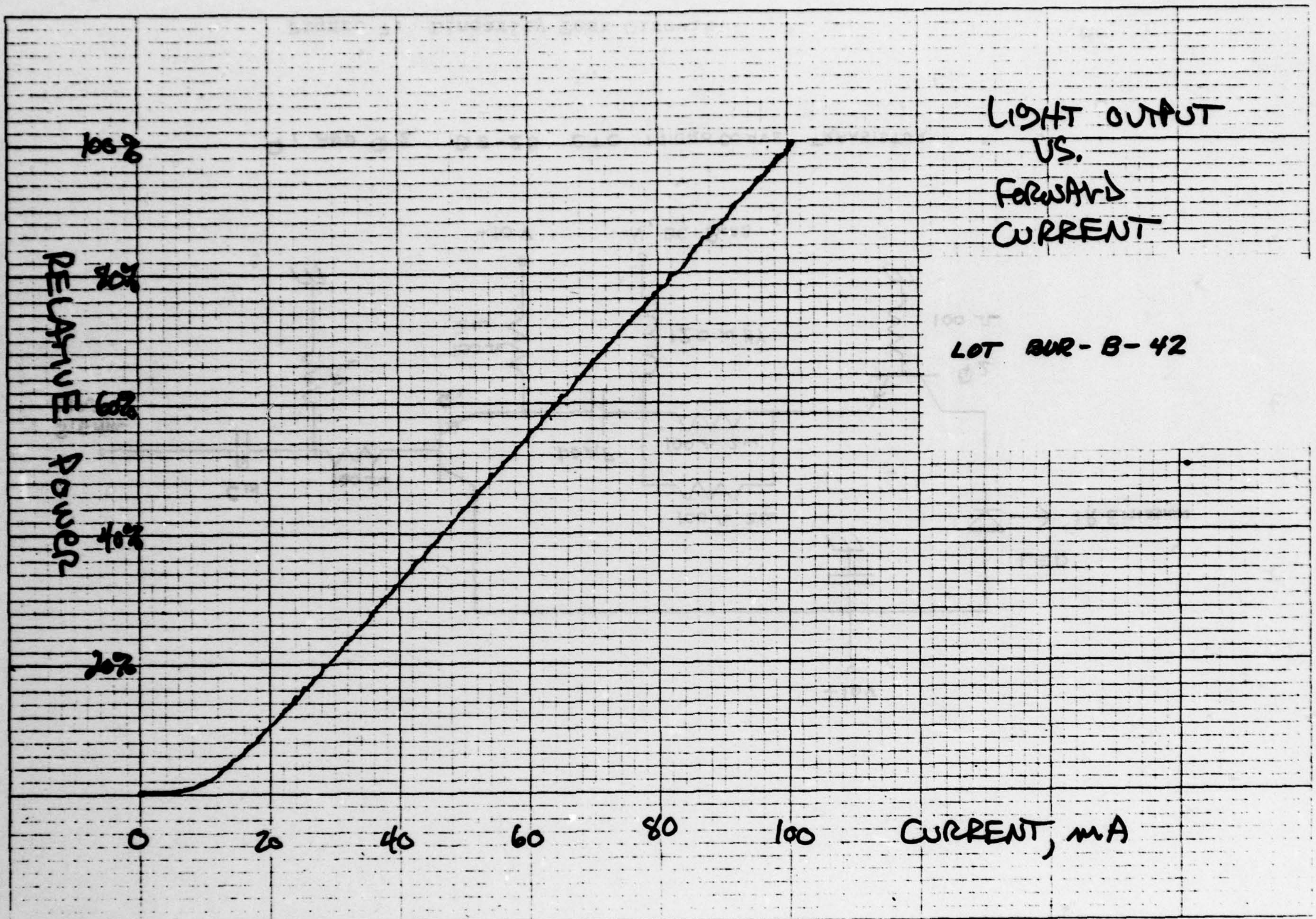
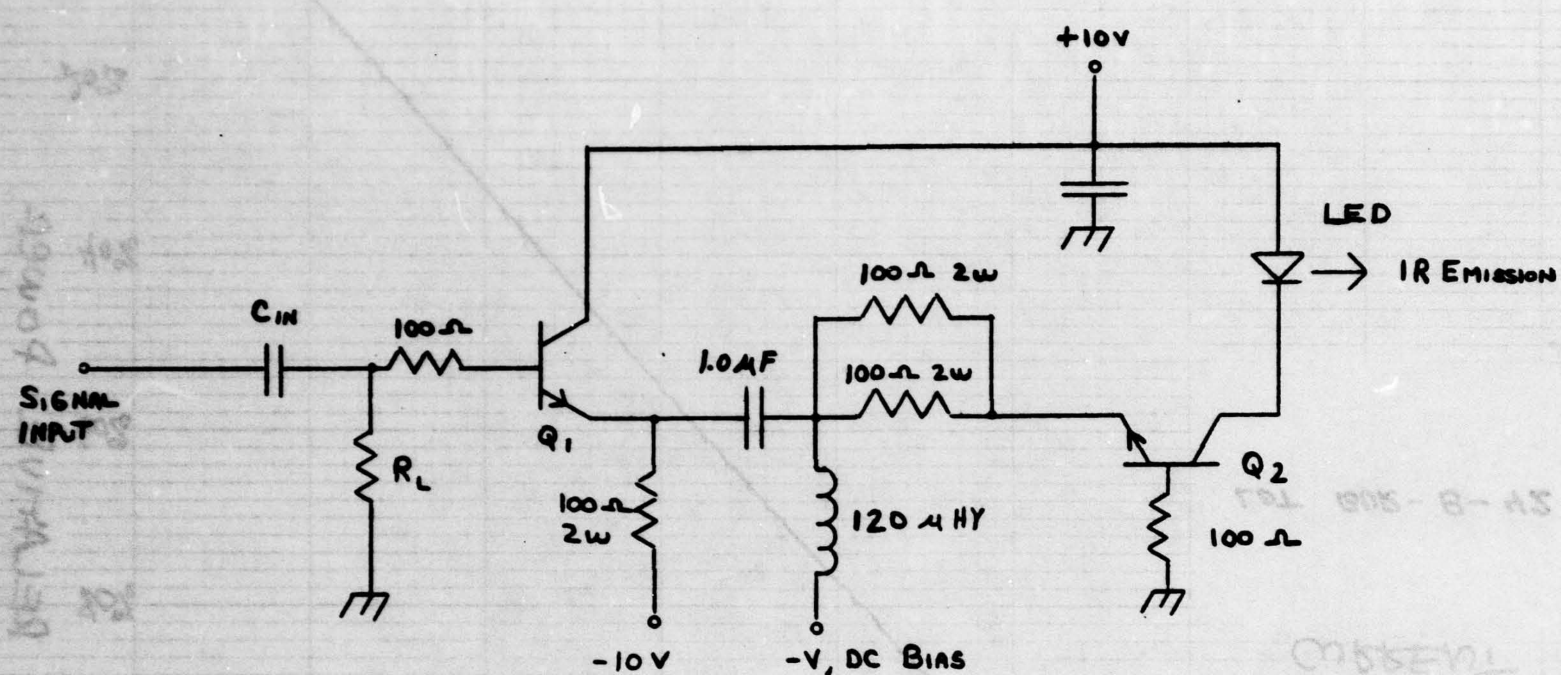


Figure 6. Linearity (Static).



Q1 AND Q2 D3-28 CTC MICROWAVE TRANSISTOR

Figure 7. Linearity Test Circuit.

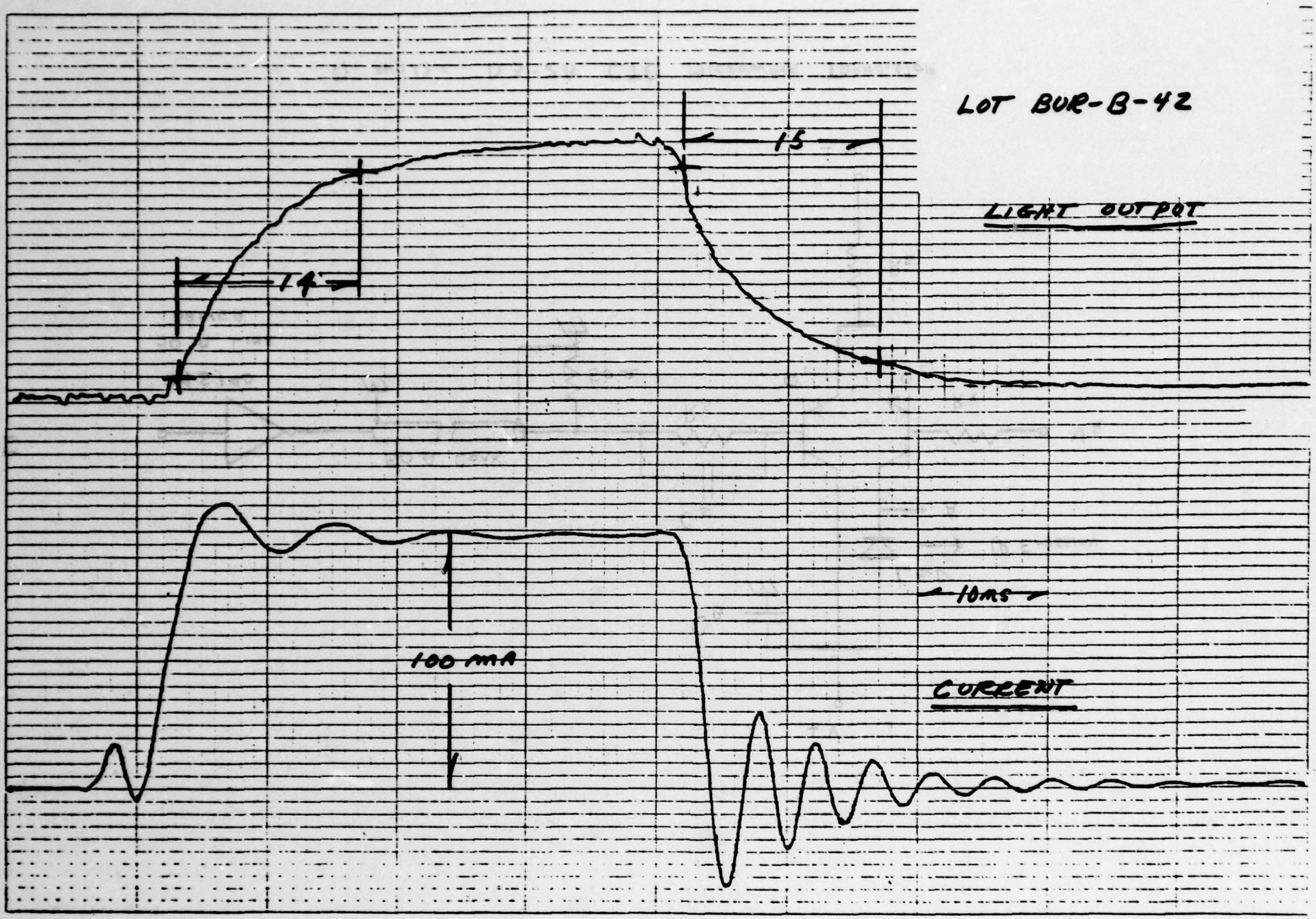


Figure 8, Rise and Fall Time,

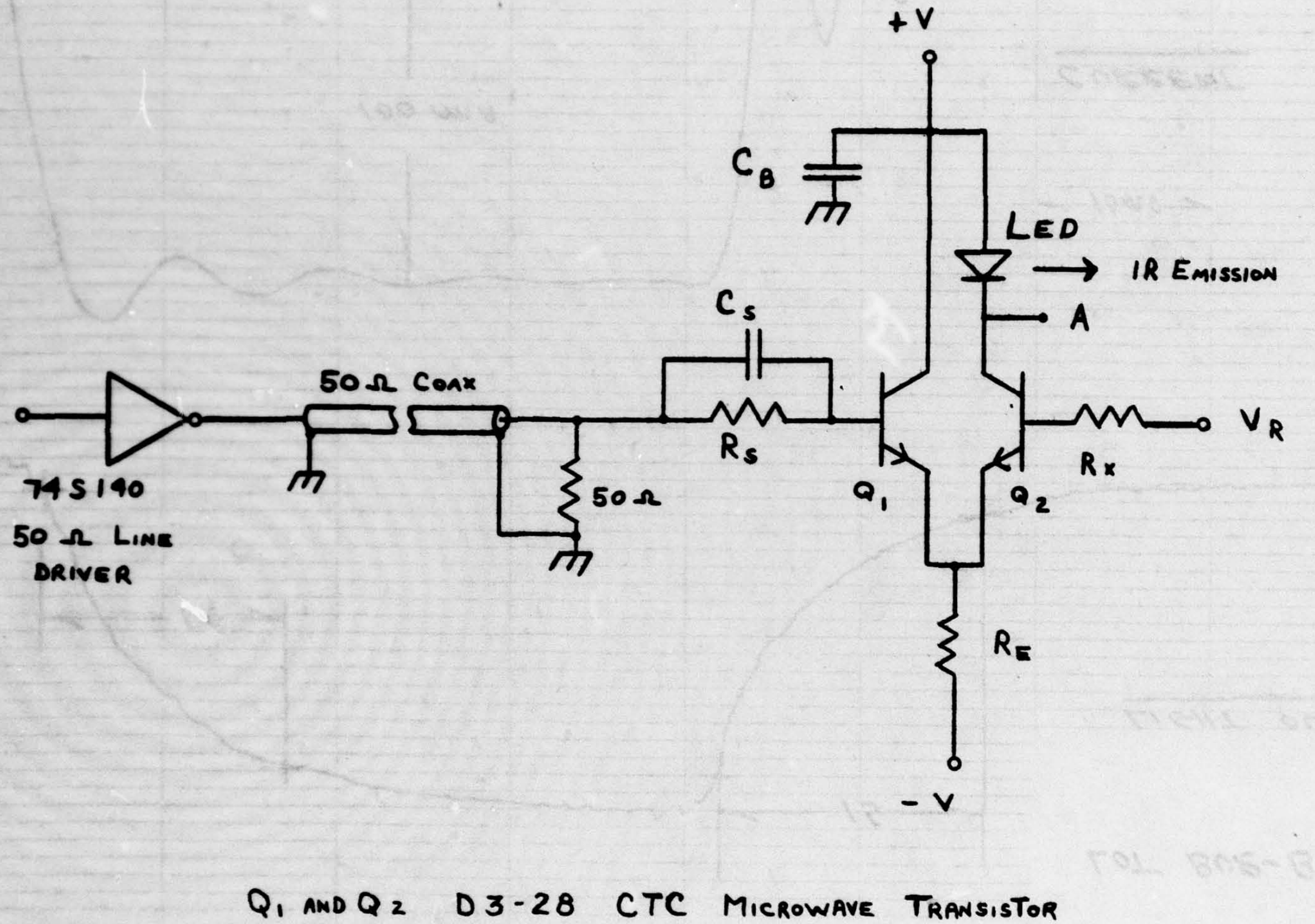


Figure 9. Rise and Fall Time Test Circuit.

TABLE 3. Lot BUR-B-42 2000 Hour Life.

		Po (mw) @ 100 ma T = 0 hrs.		Po (mw) @ 100 ma T = 176 hrs.		P0 (mw) @ 100 ma T = 2176 hrs.							
DATE TIME													
1		.550		.550		.550							
2		.540		.535		.530							
3		.575		.560		.560							
4		.585		.585		.580							
5		.520		.510		.500							
6		.685		.675		.670							
7		.510		.510		.490							
8		.530		.525		.520							
9		.540		.540		.540							
10		.500		.490		.480							
11		.505		.490		.480							
12		.510		.500		.490							
13		.540		.540		.540							
14		.510		.510		.510							
15		.575		.560		.560							
16		.570		.570		.570							
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SECTION III

SUMMARY AND CONCLUSIONS

During the fifth quarter, 2000 hour life testing was successfully completed. Sixteen units from the life test group were delivered as second engineering samples. Re-design of the zinc diffusion furnace to obtain repeatability from run to run was begun. Photo resist protective coating was included in the process to prevent scratching and tearing of the resist during handling. Plans for the next quarter include formal specification proposal for the new fiber, and construction of third engineering samples with the new fiber.

APPENDIX A

Engineering Man-Hour Utilization for the Fifth Quarter of the Program.

	5th Qtr.	Cumulative
R. B. Gill	28 Hrs.	28 Hrs.
A. Gennaro	217 Hrs.	813 Hrs.
M. Lai	178 Hrs.	265 Hrs.
T. E. Stockton	-	472 Hrs.
R. E. Albano	-	248 Hrs.
Manufacturing Personnel	1084 Hrs.	2504 Hrs.

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