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FLEET RELIABILITY ASSESSMENT PROGRAM. VOLUME 6. AN/UYK-20 COMPU--ETC(U)
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VOLUME 6

FINAL REPORT

FLEET RELIABILITY ASSESSMENT PROGRAM

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AN/UYK-20 COMPUTER, DIGITAL DATA, COMBAT SYSTEM

NAVAL OCEANS SYSTEM CENTER SAN DIEGO, CALIFORNIA

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VOLUME 6

(9) FINAL REPORT.

(6) FLEET RELIABILITY
ASSESSMENT PROGRAM.

Volume 6.

AN/UYK-20
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NAVAL OCEANS SYSTEM CENTER
SAN DIEGO, CALIFORNIA

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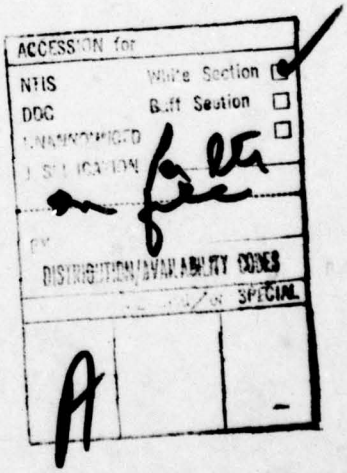
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i to vi	0
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FLEET RELIABILITY ASSESSMENT PROGRAM

DEPARTMENT OF THE NAVY

NAVAL ELECTRONIC SYSTEMS COMMAND

PREPARED UNDER THE DIRECTION OF

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TABLE OF CONTENTS

CONTENTS	PREPARED BY	PAGE
VOLUME 1 GENERAL PROGRAM REPORT	NAVWPNSUPPCEN CRANE	1-1
VOLUME 2 AN/SSR-1 EQUIPMENT REPORT	NAVWPNSUPPCEN CRANE	2-1
VOLUME 3 AN/WSC-3 EQUIPMENT REPORT	NAVELEXSYSENGCEN VALLEJO	3-1
VOLUME 4 AN/URC-85 EQUIPMENT REPORT	NESTED PATUXENT RIVER	4-1
VOLUME 5 AN/URC-62 EQUIPMENT REPORT	NAVWPNSUPPCEN CRANE	5-1
VOLUME 6 AN/UYK-20 EQUIPMENT REPORT	NOSC SAN DIEGO	6-1
VOLUME 7 APPENDICES	NAVWPNSUPPCEN CRANE	7-1

A	FRAP TEAM MEMBERS
B	SAMPLING MATRIX
C	DATA CODING
D	DATA ANALYSIS
E	LOGISTICS MODEL
F	GLOSSARY OF TERMS

TABLE OF CONTENTS

VOLUME 6 AN/UYK-20 EQUIPMENT REPORT

SECTION		PAGE
I	INTRODUCTION	6-1
II	RESULTS	6-2
	2-1 DATA PROCESSING SET, AN/UYK-20	6-2
	2-2 RESULTS SUMMARY	6-2
III	SYSTEM DESCRIPTION	6-3
	3-1 GENERAL	6-3
	3-2 MISSION DESCRIPTION	6-3
	3-3 SYSTEM DESCRIPTION	6-3
	3-4 RELIABILITY REQUIREMENTS	6-5
	3-5 MAINTAINABILITY REQUIREMENTS	6-5
	3-6 MAINTENANCE PHILOSOPHY	6-5
	3-7 PLANNED DEPLOYMENT	6-5
IV	RELIABILITY MODEL	6-6
	4-1 BACKGROUND	6-6
	4-2 RELIABILITY MODEL	6-6
V	PROBLEMS	6-16
	5-1 OPERATIONAL	6-16
	5-2 HARDWARE PROBLEM LIST	6-17
	5-3 TIMING	6-18
VI	CORRECTIVE ACTION	6-19
	6-1 RETROFIT	6-19
	6-2 TIMING/LOADING	6-19
	6-3 COOLING	6-19
	6-4 CABLE CLAMPS	6-19
	6-5 MEMORY ARRAY BOARD	6-19
	6-6 CONTROL AND DATA BOARDS	6-19
	6-7 CLOCK CARD	6-19
	6-8 PARTS	6-19
VII	COST BENEFITS	6-20
	7-1 MAINTENANCE	6-20
VIII	SPECIFICATION REQUIREMENTS	6-22
	8-1 RELIABILITY SPECIFICATIONS	6-22
	8-2 MAINTAINABILITY SPECIFICATIONS	6-22
	8-3 AVAILABILITY SPECIFICATION	6-23
	8-4 TEMPERATURE SPECIFICATIONS	6-23
IX	FLEET DATA ANALYSIS	6-24
	9-1 DATA COLLECTION	6-24
	9-2 COMPUTER RUN	6-24
	9-3 SUMMARY OF COMPUTER ANALYSIS	6-24

TABLE OF CONTENTS (Cont.)

SECTION		PAGE
X	DEPOT DATA ANALYSIS	6-45
	10-1 BACKGROUND	6-45
	10-2 RETURNED PARTS IDENTIFICATION	6-45
	10-3 VERIFICATION RATIO	6-45
	10-4 STRUCTURED ANALYSIS	6-46

TABLES

		PAGE
6-2.1	Results for AN/UYK-20	6-2
6-4.1	Reliability Model Elements	6-9 - 6-15
6-9.1	Summary of Computer Analysis	6-44
6-10.1	Failed Parts List	6-48
6-10.2	P.C.B. Analysis NOSC DPS	6-49
6-10.3	P.C.B. Analysis Fleet DPS	6-50

SECTION I INTRODUCTION

1-1 COMBAT SYSTEM PROCESSOR.

The AN/UYK-20(V) Combat System Processor, hereafter referred to as the Data Processing Set (DPS), is a 16 bit general purpose militarized digital computer which has been procured as a standard minicomputer for Naval Combat Systems applications.

SECTION II RESULTS

2-1 DATA PROCESSING SET, AN/UYK-20.

A total of 17 sample equipments on 18 sample platforms were monitored for approximately a nine month period (June 1976 through March 1977) utilizing the 3M system with a limited amount of additional data for the sample equipment. The total operating time of the sample equipment was 34,427 hours in a total calendar time of 91,824 hours (a duty cycle of .375). During this period, a total of 20 system operational failures were encountered on the sample equipment. Of those failures, it is estimated that 18 were equipment failures.

2-1 RESULTS SUMMARY

TABLE 6-2.1

Parameter	Specified	Predicted @50°C	Predicted @30°C	Operational Ship	Operational Lab	Equipment Ship
MTBF	2000	304	2066	1721	1586	2008
90% Confidence Level						
Upper Limit				2370		3012
Lower Limit				1270		1406
Verification Ratio				.857		
MTTR (OP)	0.25			49.3	0.68	
90% Confidence Level						
Upper Limit				99.2		
Lower Limit				0.00		
Down Time				248.5		
Availability						
Inherent	.999875	.999178	.999879	0.972316	.999329	.976178
Operational (Sample Obseration)				0.971339		

2-1.1 COMPLIANCE.

The system meets the MTBF requirement of 2000 hours with the 90% confidence level upper limit value of 2370 hours (Table 6-9.1).

2-1.2 RELIABILITY PREDICTIONS. Two reliability predictions were calculated: one for 50°C and one for 30°C ambient intake air temperature. The adjustment results in part from the Arrhenius relationship which projects a doubling of chemical reaction rates for a 10°C rise in temperature. This results in a commensurate change in failure rates for semiconductor and other types of devices dominated by failure mechanisms that are chemical in nature. Exercising the "rule of thumb" alone would result in MTBF prediction of 1216 hours i.e., 20°C reduction results in four times improvement (304 X 4).

SECTION III SYSTEM DESCRIPTION

3.1 GENERAL. The AN/UYK-20(V) are being procured from Sperry Univac Defense Systems under Contract N00039-73-D-0432. The data sets are design to meet a variety of processing requirements for Naval Shipboard, land-based, and submarine combat systems.

3.2 MISSION DESCRIPTION. The AN/UYK-20(V) DPS are general purpose minicomputers in a ruggedized format suitable for use in control, data processing, and combat systems applications aboard all classes of ships and submarines and at land-based installations. Among the projected tasks for the data sets is the tuning, operation, and control of telecommunications equipment. The data sets will be used with input/output devices such as teletype machines and will be interfaced to other equipments as required.

3.3 SYSTEM DESCRIPTION. The AN/UYK-20(V) DPS consists of a single enclosure. The cabinet is designated CY-7445/UYK-20(V) for the 400 Hz version or CY-7446/UYK-20X(V) for the 60 Hz version.

3.3.1 DPS SECTIONS. The data set breaks down into five sections which are:

Equipment Cabinet

CY-7445/UYK-20(V) (400 Hz version)
CY-7446/UYK-20(V) (60 Hz version)

Control Monitor

C-9674/UYK-20(V) (400 Hz version)
C-9675/UYK-20X(V) (60 Hz version)

Memory Chassis C-9531/(V)/UYK-20(V) or C-9670(V)/UYK-20X(V)

(2ea) Memory Control Board - (included above)
(2ea) Memory Data Board - (included above)
(1-8ea) Core Memory Unit - MU-604/UYK-20(V) or MU-632/UYK-20(V)

Processor - Verifier Unit

CP-1188(V)/UYK-20(V) (400 Hz version)
CP-1189(V)/UYK-20X(V) (60 Hz version)

Program Kit, Micro Memory MK-1723(V)/UYK-20(V)
Register, Computer, Single MU-633/UYK-20(V)
Register, Computer, Dual MU-634/UYK-20(V)

3.3.2 INTERFACE KITS. There are 16 slots allotted to input/output interfaces. The interface kits contain either two (serial type) or four cards (parallel type). The DPS I/O slots are subdivided into four sets of four slots each. A set may contain either one or two serial kits or one parallel kit.

(1) Interface Kit, Slow, MK 1693/UYK-20(V). (Parallel, -15V)
(2) Interface Kit, Fast, Negative, MK 1694/UYK-20(V). (Parallel, -3V)

(3) Interface Kit, Fast, Positive, MK 1695/UYK-20(V). (Parallel, +3.5V).
(4) Interface Kit, Serial Communications, Synchronous MK 1718/UYK-20(V).
(5) Interface Kit, Serial Synchronous MK 1719/UYK-20(V). (MIL-STD 188C, Sync).
(6) Interface Kit, Fast Serial, MK 1720/UYK-20(V). (NTDS Serial).
(7) Interface Kit, Serial Asynchronous MK 1721/UYK-20(V). (MIL-STD-188C, Async)/(RS-232C, Async)
(8) Interface Kit, Serial Communications Asynchronous MK 1722/UYK-20(V).
(9) Interface Kit, Parallel Peripheral Input Channel (Nomenclature not available).
(10) Interface Kit, VACALES Serial MK1806/UYK-20(V).

Power Supply Chassis (one only, depending on power source available)

115 Vac, 3 phase delta, 400 Hz: PP-7032/UYK-20(V)
208 Vac, 3 phase wye, 400 Hz: PP-7107/UYK-20(V)
115 Vac, single phase, 400 Hz: PP-7108/UYK-20(V)
115 Vac, 3 phase delta, 60 Hz: PP-7109/UYK-20X(V)
208 Vac, 3 phase wye, 60 Hz: PP-7110/UYK-20X(V)
115 Vac, single phase, 60 Hz: PP-7111/UYK-20X(V)

3.3.3 DATA PROCESSING SET. The AN/UYK-20(V) DPS is a modular, medium-scale, general purpose digital data processing device using a micro-programmed control structure. The microprogram consists of microinstructions and control data stored in read-only memory (ROM). The DPS operates from a stored program of macroinstructions read from main memory to perform arithmetic operations, solve real-time problems, control other equipment, and perform a variety of other data processing operations. It performs two's complement integer arithmetic using signed numbers. Its logic construction is parallel. The basic word length is 16 bits which may be handled as 8-bit bytes (such as ASCII character codes), as 16-bit words, or as double-length 32-bit words. It has memory addressing capability of up to 65K 16-bit words which may be treated as groups of pages for relative (virtual) addressing. The memory cycle time is 750 nanoseconds. The DPS communicates with peripheral equipment through an I/O controller containing up to 16 channels, which may be parallel or serial channels or a mixture of both. It has an interrupt structure, dependent on priority assignments, which permits interruption of the normal of the normal program sequence to perform special functions. It allocates a portion of micro-memory for a user-defined microprogram. It has a real-time clock and a monitor clock which operate either from an internal oscillator or from an external clock input. A Math Pac option adds a square root, floating point, trigonometric, hyperbolic, and double-precision multiply and divide capability.

It can operate from either 400 Hz or 60 Hz (-20X(V) version) on a variety of standard voltages in either single or three phase configurations. The AN/UYK-20(V) is intended to be a system building block and as such will interface to input/output devices such as teletype machines, to mass memory devices such as magnetic disc or tape units, and to digital controlled devices such as printers, plotters, or radio sets. User interaction with the DPS will be, primarily, through one or more of these external devices.

3.4 RELIABILITY REQUIREMENTS. The AN/UYK-20(V) Data Processing Set is to have, according to specification ELEX-C-135, a specified MTBF of 2,000 hours.

3.5 MAINTAINABILITY REQUIREMENTS. The AN/UYK-20(V) is a modular assembly. Primary organizational level maintenance will be by replacement of printed circuit cards. Mean Time to repair is specified as 15 minutes with maximum maintenance time at the 95% confidence level specified to be 120 minutes. Mission utilization is expected to be upwards of 90%.

3.6 MAINTENANCE PHILOSOPHY. The AN/UYK-20(V) is repaired on the organizational level with the aid of a built-in diagnostic program which will sectionalize a problem to, typically, a three card area. Immediate repair action is effected by replacement of all three cards. At some later time when the DPS is not being utilized, the pulled cards are re-inserted into the DPS to isolate which is the defective card. If the identified card is one of those judged to be economical to repair, it will be returned to the vendor for depot level maintenance. No intermediate level maintenance is planned at this time. If the identified card is not judged economical to repair, it will be discarded. No repair of cards is planned at the organizational level.

3.7 PLANNED DEPLOYMENT. DMI (Defense Marketing Intelligence) reports over 800 in-service by mid 1976 and a follow-on-production on a modification of the original contract as of March 1977 of several hundred per year for two years. The system is to be used in MK 68 gun fire control systems, ESM systems such as the AN/WRL-6, and in the Marine Air Traffic Control and Landing System (MATCALS). The unit uses the CMS-2 (Compiler Monitor System - 2nd generation) language which is the Navy's standard high level tactical language.

SECTION IV - RELIABILITY MODEL

4-1 BACKGROUND

4-1.1 SYSTEM DESCRIPTION - The AN/UYK-20(V) Data Processing Set (DPS) is a ruggedized general purpose medium sized minicomputer suitable for a variety of data processing tasks. The AN/UYK-20(V) occurs in two primary variants, the 400Hz powered AN/UYK-20(V) and the 60Hz powered AN/UYK-20X(V). The Power Supply, memories, general register and the interface groups allow options at the modular level. The AN/UYK-20 is of modular construction and each O-Level replaceable module is divided into Line Replaceable Units (LRU). The AN/UYK-20 provides for memory options of up to 64K memory which is contained on eight Memory Array Boards (MAB), physically located inside the Memory Control module. Each MAB contains 8K words. The AN/UYK-20 contains interfacing options for parallel input, output I/O channels, or serial channels (total of sixteen channels maximum). I/O subgroups are received with the equipment as a kit and are serviced on a replaceable card basis. One of the cards has options selected by moveable straps. Because the setting of straps does not affect the likelihood of failure, these options are shown as a single block.

4-2 THE RELIABILITY MODEL

4-2.1 BLOCK DIAGRAM MODEL - Figure 6-4.1 is a series reliability block diagram of the AN/UYK-20(V). Because of the versatility of the equipment, a generalized mission has been developed. Since operating modes are unspecified, any channel failure must be considered a system failure. Detailed block diagrams for the blocks depicted in 6-4.1 are available from the FRAP Lead Field Activity (LFA). These become quite complex because of the nature of construction of a digital computer. Table 6-4.1 provides a list of the following module information:

(1) Reliability Block Number
(2) Nomenclature
(3) Reference Designation
(4) Manufacturers Stock Number
(5) Failure Rate (per million hours)
(6) Number Used

4-2.2 THE FORM OF THE MODEL - As discussed above, the AN/UYK-20 is a series model with respect to the major blocks (Figure 6-4.1). The model is based on MIL-HDBK-217B prediction and failure rates were furnished by the contractor. Series reliability is calculated by equation 1 and 2 below:

$$R(TOT) = EXP(-LT) \qquad (1)$$

where $L = L(1) + L(2) + \ldots\ldots\ldots + L(n)$ (2)

the failure rates L(N) can be added because an exponential distribution is assumed.

The Control-Monitor Group is made up of indicator lights and switches, but its function in system maintenance is so vital that it has been included in the overall reliability series string. Although failure of an indicator will not result in an immediate system outage; it will delay system repair because the indicator must be repaired before system trouble shooting can continue. From a reliability standpoint, the requirement to repair the indicator before the next failed item can be repaired/replaced is equivalent to a normal fail/fix cycle. The Power Supply (see Figure 6-4.1) is a single modular line replaceable unit. Although six different options exist, three of these (Parts List Designators 5-7, see Table 6-4.1) are useable only on the AN/UYK-20 (V) and three (Parts List Designators 8-10) are useable only on the AN/UYK-20X(V). This defines three different power supply options for each of the two system frequency options. The Processor-Verifier (see Figure 6-4.1) is the heart of the DPS hardware. It contains the data shuffling, computational, instruction decoding, and general overall cycle-control circuitry. The entire remainder of the system can be viewed as supporting this section. It is here that user instructions are converted into strings of system instructions that accomplish some task, such as addition. From here instructions go to memory to call up program steps and to recall and store data bits. When the user interacts with the computer, it is this section that "converses" with him. The memory control module also depicted in Figure 6-4, buffers data to and from the Memory Array Boards and fetches and stores data on command from the Processor-Unifier.

RELIABILITY BLOCK DIAGRAM
for the AN/UYK-20 (V)
(Modular Level)

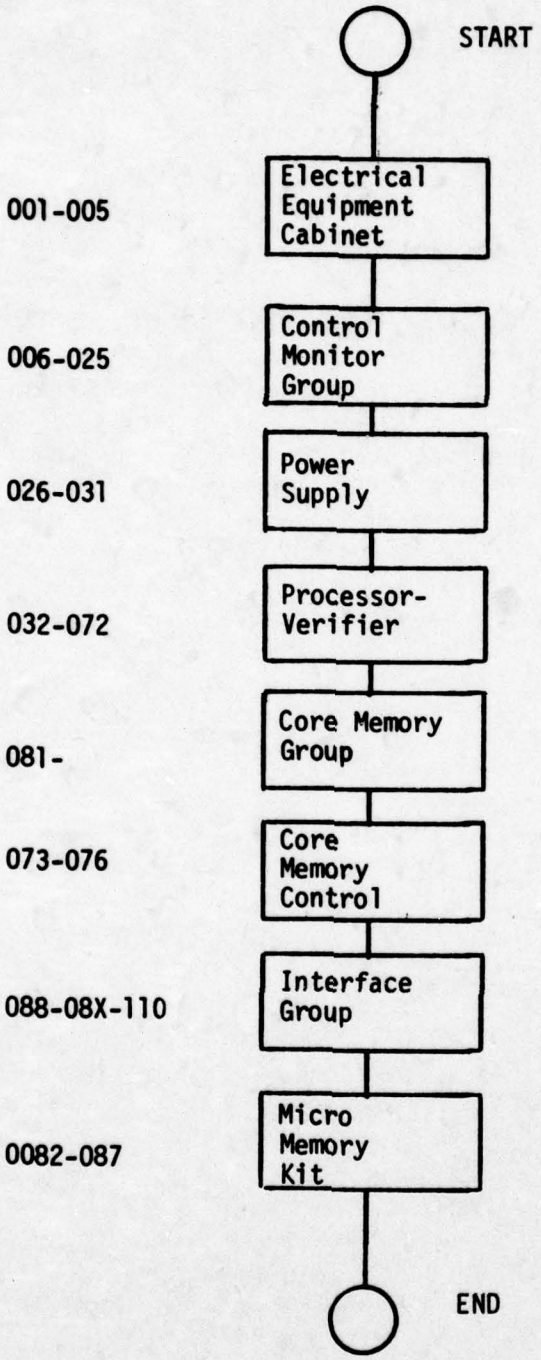


Figure 6-4.1

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE $X10^{-6}$	NUMBER USED
001	1A4	Filter Assy	7101950-00	.3376	
002	1A6	Elec. Comp. Assy.	7126335-00	.0008	1
003	1A3	Resister Assy	7128008-00	.0105	1
004	1W5	Power Cable Assy	7133925-00	.2400	1
005	1B1	Fan Assy	7133943-00	10.0	1
006	3A	Panel Assy	M3901915-80		
007	-	-	7904735-20/23		
008	-	-	7904289-12/14		
009	-	-	MS24656		
010	-	-	MS24655		
011	-	-	7904733		
012	-	-	790429-00		
013	-	-	7101817-00		
014	3A2FL1	Choke Assy	7134945-00		
015	-	-	Ms27418-1A		
016	-	-	MS17322-10		
017	-	-	7904277		
018	-	-	7904278		
019	-	-	MS24655		

Table 6-4.1

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE X10^{-6}	NUMBER USED
020	-	-	900125-16		
021	-	-	7904466		
022	-	-	4911632		
023	-	-	910486-20		
024	-	-	7101913		
025	-	-	DPDT Switch		
026	5	P.S. 115V, 400Hz, 3P	7101840-00	110	1
027	6	P.S. 208V, 400Hz, 3P	7101995-00	110	1
028	7	P.S. 115V, 400Hz, 1P	7101875-00	110	1
029	8	P.S. 115V, 60Hz, 3P	7101880-00	110	1
030	9	P.S. 208V, 60Hz, 3P	7101990-00	110	1
031	10	P.S. 115V, 60Hz, 1P	7101885-00	110	1
032	-	M. Reg	7092200-01	12.5	1
033	11A7	2-BIT Mult	7126125-01	17.2	2
034	11A9	Shift Matrix	7125500-01	14.2	2
035	11A12	SFT Matrix Input	7126130-01	11.3	1
036	11A13	SFT Matrix CTL	7126137	11.3	1
037	11A14	MON CLK CTL	7126160-01	11.7	1
038	11A15	Mem Bank Sel	7126206-01	7.54	1

TABLE 6-4.1 (cont.)

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE $X10^{-6}$	NUMBER USED
039	11A19	I/O Data Drv	7126150-01	17.7	1
040	11A20	I/O Index Logic	7125306-01	29.4	4
041	11B6	NDRO	7126147-01	37.3	1
042	11B7	Micro CTL	7125275-01		
043	11B8	Branch CTL	7092195-01	12.6	1
044	11B9	ALU CTL II	7125416-01 7125415-01	6.35	1
045	11B10	ALU CTL	70902181		
046	11B11	ALU	7092175-01	15.3	4
047	11B15	S/D Xfer	7125290-01	10.5	1
048	11B16	Clock	7125960-01	10.2	1
049	11B17	Micro-CTL 15	7126191-01		
050	11B18	I/O PRI-CTL	7126181-01	11.7	1
051	11B19	Int Store	7126186-01	13.5	1
052	11B20	I/O Priority	7126175-01	9.36	1
053	11B21	Translator	7126171-01	17.9	1
054	11B23	20MHz Osc	7126100-01	22.4	1
055	11C5	Special MEM Int'f.	7126155-01	10.7	2
056	11C9	Page REG	7125405-01	48.4	1
057	11C10	MEM CTL	7125666-01	13.4	1
058	11C13	Instr Reg	7215240-01	12.3	1

Table 6-4.1 (cont.)

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE $X10^{-6}$	NUMBER USED
059	11C15	Pt Stat Reg	7125380-01	18.4	2
060	11C17	Emulate CTL I	7125236-01	12.2	1
061	11C18	Emulate CTL II	7125386-01		
062	11C19	Jump + IA	7126166-01	13.5	1
063	11C22	Power Int	7125925-01		
064	-	Repeat CTL	Wiring/Straps		
065	11B1	Axial Fan Assy	-		
066	-	P-BKP7-M Addr Reg	-		
067	-	PWR Int, MACLR, Mode	-		
068	-	XLTR CTL & TMG	MS3120E14-5P		
069	-	Register (Single)	-		
070	-	Not assigned	-		
071	-	Not assigned	-		
072	11W8	DMA Cable Assy	-		
073	14B1	Axial Fan	-		
074	14C1	Fixed Cap	7903001-33		
075	-	Not assigned	904862-15 7134919-00		

Table 6-4.1 (cont.)

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE X10^{-6}	NUMBER USED
076	-	Not assigned	1N2816B		
077	14A1R1	Fixed Resister	RER60F1GR5M		
078	-	Not assigned	-		
079	14A5	CTL Data BRD	-		
080	14A6	Mem Data BRD	-		
081	13	Mem Array BRD	7128082-00	15.4	8
082	24A11	Multiply CTL/Math Pac	-		
083	24B5	M Mem I	7125128-01	99.6	1
084	24XX	NRDO & Cordic	7136611-00	37.3	1
085	24B2	Diag ROM	7125136-01	85.1	1
086	24C12	Emulation CTL	7125157-01	40.1	1
087	24A11	M Mem II			
088	16A1	Fast Serial Drv			
089	16A2	Fast Serial Rcvr			
090	17A1	Serial Sync			
091	17A2	Serial Sync			
092	-	Not assigned			

Table 6-4.1 (cont.)

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE X10^{-6}	NUMBER USED
093	18A1	Serial Asynch Rcvr	713327-01	64.0	1
094	18A3	Serial Async Drvr	7133231-01	65.9	1
095	-	Not assigned			
096	19A3	Serial Comm Dvr	7150352-01	52.6	1
097	19A2	Serial Comm Rcvr	7119430-01	34.8	1
098	-	Not assigned			
099	20A1	Async Comm Drvr			
100	20A3	Async Comm Rcvr			
101	-	Not assigned			
102	21A1	-15V Slow Type I	7119395-01	31.7	2
103	21A2	-15V Slow Type II	7119405-01	38.1	1
104	21A3	-15V Slow Type III	7119401-01	47.8	1
105	22A1	-3V Fast Type I	7119380-01	21.6	2
106	22A3	-3V Fast Type II	7119385-01	32.9	1
107	22A4	-3V Fast Type III	7119390-01	30.6	1
108	23A1	+3V Fast Type I			
109	23A3	+3V Fast Type II			
110	23A4	+3V Fast Type III			
111					
112					

Table 6-4.1 (cont.)

REL BLOCK	REF DESIGN	NOMENCLATURE	MFG P/N	FAILURE RATE X10^{-6}	NUMBER USED
113					
114	24A4	-			
115	-	Jumper Plug			

Table 6-4.1 (cont.)

SECTION V PROBLEMS

Preceding the FRAP Program by several months an excellent problem solving program was initiated. In December 1975 a Test Analyze, and FIX (TAAF) Program was established to assess and if necessary, improve the DPS. The objective of the TAAF Program was to investigate all failures to determine if reliability problem existed, and if necessary generate appropriate corrective action recommendations. The test was conducted using four DPS's. Each processor was configured differently to assure that the majority of all DPS ordering options were included in the test. The test was conducted in a high-temperature (50°C, 50 percent relative humidity) environment with all maintenance actions strictly controlled. Test software was loaded into each computer and allowed to run continuously throughout the entire test period of at least 3000 hours per DPS. All deviations from normal operation were recorded and investigated until the problem was isolated. The test was initiated on 17 December 1975, and with the exception of a 10 day shutdown period over the holidays, the test ran continuously until 1 June 1976, for a total of 14,305 cumulative test hours. During this test period eight critical/solid failures occurred, and numerous noncritical failures occurred. It should be noted that no design modifications were made during the test period, with the exception of a redesigned master clock module which was installed after 9,200 hours of testing. The reliability improved steadily after the first 4000 hours of testing from 600 hours to 1788 hours MTBF.

The improvements as the result of TAAF are obvious when compared to the results reported in a "Thermal Analysis Test Report - AN/UYK-20" conducted in September 1975 by NOSC (formerly NELC) which states in paragraph 2.1 "The AN/UYK-20 computer, with its door closed, and not mounted in a cabinet, operated satisfactorly (though not in a reliability sense) in both the 25°C, 50 percent relative humidity and the 50°C, 30 percent relative humidity ambient environments:. This report further states under conclusions in Item 4, " Use of 74 family of devices is marginal and borders on being unacceptable at a 50°C external ambient,..." and in Item 6, "If 54 family TTL devices were used exclusively in the UYK-20, the probability of thermal problems ....would be greatly reduced".

5-1 OPERATIONAL

5-1.1 HEAT. Early shipboard installation of the DPS resulted in overheating indications and intermittent malfunctions. In most every installation the DPS was placed in a rack which impeded the air flow. This raised the internal temperatures in the box and caused thermal problems with the semiconductor devices. One CV reported on a Ship's Maintenance Action Form (2-KILO) "Program faults due to inadequate ventilation xxx extended present ventilation to directly above equipment". They recognized the problem and did something to improve the cooling. An LPH also commented about the heat problem"...most probable cause is physical placement of unit. Heat is exhausted from unit and this hot exhaust is immediately directed back to the AN/UYK-20 by the TT-624 being mounted only 6 inches away". As can be seen overheating in most cases was caused by incorrect installation in racks which blocked DPS exhaust ports. The proper installation of the DPS has reduced the overheat problem.

If this could have been anticipated the specification could have been written more realistically. Specifications for future systems using semiconductor devices should certainly consider factors that influence internal cabinet temperatures.

5-1.2 POWER. Some sensitivity of DPS to transients on ship power grids has been reported causing intermittent program failures. These reports were for DPS's with 60 cycle, 110 VAC power supplies. The carrier found that by paralleling two generators on one power grid, that intermittent program stops were eliminated. The Electronics Maintenance Officer on the carrier was of the opinion that if these were 3 phase, 400 cycle power supplies in the DPS they would not be as sensitive to power grid transients since the 400 cycle power is more free of tranients. A NESEC field crew has since monitored the power grids and found voltage and transients within the requirements of MIL-E-16400 and MIL-STD-1399. Also, according to the Project Office, the primary cause of program failures due to power transients has been improper programming of the DPS Power Fault Interrupt by the users.

5-1.3 PARTS. Long repair time appears to be a problem on some ships. In some cases, long repair times seem to be a function of how difficult it is to obtain parts from ship's supply. Sometimes even the obtaining of the necessary authorization signatures can take several hours to a full days time. Then it can take several hours for the supply personnel to identify and locate the part. The prospect of these possible difficulties are sufficient to cause a 24 hour delay in the actual initiation of the procedure to obtain replacement parts. One LPH reported on a form 2 KILO ". . . Poor Cosal support . . .", early in the FRAP reporting period.

5-1.4 TROUBLESHOOTING. The usual time to checkout a DPS using diagnostic software is under five minutes. Actual time required to run all diagnostics now being used with the system is in excess of one hour, including preparation time. As a rule, however, all diagnostics are not run unless unusual problems develop. According to users, typical time to troubleshoot and repair is only one-half hour.

DIAGNOSTIC TEST TIMES REPORTED

MICRO	1 minute
CP Central Processor	1 minute
CP Logic	20 seconds
I/O	
Parallel	2 minutes*
NTDS Serial	2 minutes*
Common	1 minute**

* Total 40 minute preparation, loading of test, removal of I/O cables, and installation of jumpers in typical applications.

** Total of 30 minutes including preparation and loading of diagnostics is typical, according to users.

5-1.5 TRAINING. Maintenance training and transfer schedules of personnel need to be reviewed so as not to remove trained DPS men from ships without replacement. One ship reported on a form 2 KILO " . . . technical training appears to be inadequate - most individuals appear confused in relation to overall system operation and how the AN/UYK-20 fits in the total system . . .".

5-2 HARDWARE PROBLEM LIST. Section IX lists several items under Problem Area, Table

5-2.1 MEMORY ARRAY BOARDS. One area identified was cracked cores on the Memory Array Board (MAB) and often on spare boards. Most of the breakage seemed to be occuring in shipping.

5-2.2 CABLES. Initially, cables were not sufficiently secured and several cases of cable damage and one cable fire was reported during the FRAP monitoring period.

5-2.3 RESISTORS, PCB. Resistors popped loose from PCB and one case of a cracked resistor was reported from improper installation of resistors. This was observed on a MAB and on one Micro Memory I PCB.

5-2.4 LOGIC, PCB. Failure of logic resulted from a short between board buss caused by incorrect installation of IC on the PCB.

5-2.5 PCB LIST. Figure 6-10.1 is a composite list of modules returned to the contractor and to the Technical Support Activity (TSA). No defect was found for four of the items. Failed components are listed, the majority of which were integrated circuits. Some items such as the cracked core and broken resistor duplicate items on the Problem List in Section IX.

5-3 TIMING

Symptoms of master clock problems were reported early in the AN/UYK-20 program but the cause was not detected and resolved until the TAAF progam as noted above.

SECTION VI CORRECTIVE ACTION

Some one hundred Class I Engineering Change Proposals (ECP) had been generated for the AN/UYK-20 as of March 1977, approximately forty of these during the FRAP monitoring period.

6-1 RETROFIT. The contractor completed Retrofit 1 and 2 on the DPSs at NOSC by December 1976 and aboard ships on an as-available basis. The retrofit included many of the ECP proposed over the last year.

6-2 TIMING/LOADING. Some of these ECPs include improvement in I/O control pulse width variance by one magnitude (from 15% to 1.5%) (optional), I/O Interrupt priority acknowledgements, clock performance pulse, timing accuracy and load distribution of circuit gates. A worst case analysis of gate load distribution was done by UNIVAC in the spring of 1976. This pointed up the fact that many gates were overloaded under worst case conditions. The UNIVAC representative, however, in presenting this study insisted that worst case conditions seldom occurred. However, changes to decrease gate loading were implemented in Retrofit I and II and further changes are being considered.

6-3 COOLING. Early in the FRAP monitoring period, (July 1976) a very comprehensive report was received from the USS GUAM and the USS CONSTELLATION discussing DPS overheating problems (5-1.1). As a result, poor ventilation of some DPS installations was quickly noted and corrected and subsequent installations were revised. A better internal ventilating fan was also installed in the DPSs by the contractor early in the AN/UYK-20 program.

6-4 CABLE CLAMPS. Cable clamps have been installed to correct cable abrasion problems which caused cable shorts and computer replacement such as is listed in Section IX under Problem Areas.

6-5 MEMORY ARRAY BOARD. In Section V cracked cores on Memory Array printed circuit boards was listed as a problem. A new shipping case was designed for the card. This eliminated breakage during shipping which seemed to be the major problem. Also, stiffeners have been added to the boards to make the board more rugged and to improve connector alignment.

6-6 CONTROL AND DATA BOARDS. Control and data boards also have stiffeners installed.

6-7 CLOCK CARD. A new clock card was checked out by the TAAF Program and released to the field. Further improvements are noted in paragraph 6-2, Timing/Loading.

6-8 PARTS. A longer burn-in of 1000 hours is being specified for the new DPS. This will cull out parts that fail during the early life of the equipment.

SECTION VII COST BENEFIT

Early detection of operational hardware problems has affected early correction at the cost of the contractor. Many of the ECPs discussed in Section VI have been implemented at no cost to the government.

7-1 MAINTENANCE. Early correction has resulted in lower maintenance costs immediately and for the total life cycle of the system.

7-1. MTBF. One of the dramatic indicators of improvement in the rise of the MTBF during the period monitored by FRAP, from 313 hours as of December 1976 to 1721 hours at the end of the monitoring period. It should be noted that the December MTBF was arrived at without the benefit of the operating time of nonreporting DPS in the sample.

7-1.2 MODULES. A decrease was noted in the monthly average quantity of suspected failed modules which were returned during the last two months as compared to the quantity returned during the first six months. As a result, module costs averaged twenty percent less for the last two months of the monitoring period.

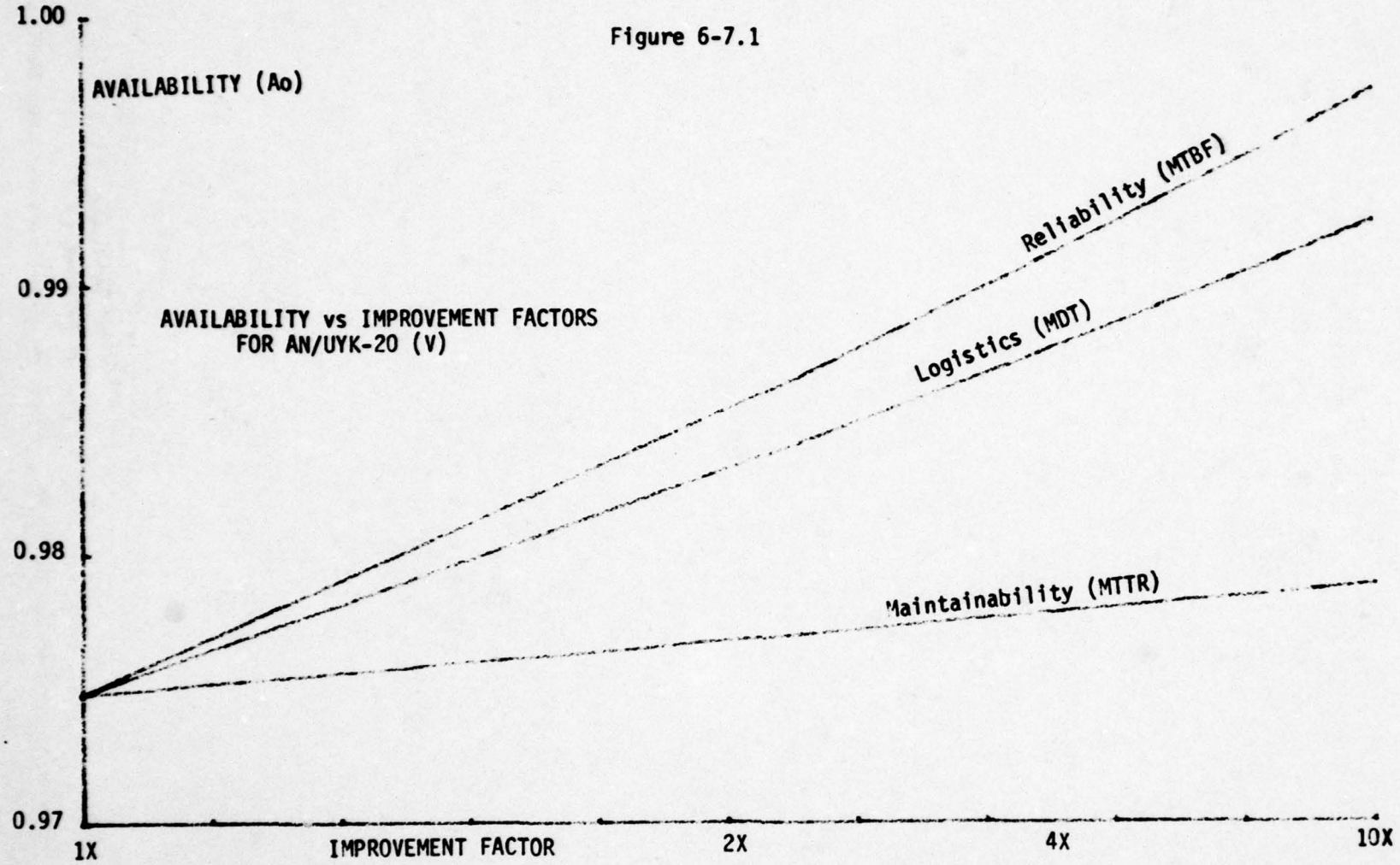
7-1.3 TRAINING. Training or actual retraining could be a needed program. As the DPS approaches the 2000 hours MTBF, it requires less and less attention. As a result the technician loses his knowledge of the equipment through non-use. An active preventive maintenance program will help to keep the technician knowledgeable and preventive maintenance needs to be emphasized as some technicians have the philosophy "If it works leave it alone".

7-1.4 WATER COOLING. In the consideration of the Arrhenius rule-of-thumb noted in Section II, water cooling may offer an effective way to control the temperature of air within the DPS and to improve the reliability. By lowering the temperature 10°C the MTBF could be theoretically doubled. UNIVAC originally provided the design of a water cooled heat exchanger and a cost/benefit analysis could show an advantage to water cooling the DPS. On the other hand, some authorities insist water cooling is not effective since "chilled" water temperature can exceed 40°C.

7-1.5 INTEGRATED CIRCUIT TYPE. Originally TTL Type 74 Integrated Circuits (IC), operating temperature range 0°C to 70°C, were used exclusively in the DPS. A more general use of Type 54 IC (some are used in selected circuits) operating temperature range -65°C to 125°C would reduce the failure rate and improve the availability as suggested by Figure 6-7.1.

7-1.6 PASSIVE COMPONENTS. Changing resistors and capacitors one level from M to P level would also increase the availability of the DPS. Cost studies could show this as a desirable change.

Figure 6-7.1


1.00
AVAILABILITY (Ao)
0.99
AVAILABILITY vs IMPROVEMENT FACTORS
FOR AN/UYK-20 (V)
0.98
0.97
Reliability (MTBF)
Logistics (MDT)
Maintainability (MTTR)
1X
IMPROVEMENT FACTOR
2X
4X
10X

SECTION VIII SPECIFICATION REQUIREMENTS

Specification requirements are stated in the Contract Specification EXEC-C-135 dated 27 November 1972.

8-1 RELIABILITY SPECIFICATIONS

8-1.1 RELIABILITY. The specification states in paragraph 3.3 "---the maximum configuration computer shall be 2000 hours specified MTBF minimum..." Two reliability predictions were calculated by the contractor. One at 50°C resulting in 304 hours MTBF and one at 30°C resulting in 2066 hours MTBF. Operating temperature range requirements are discussed in this Section, paragraph 8-4.

8-1.2 RELIABILITY DEMONSTRATION TEST. In paragraph 4.5.1.1.1 the specification states "The reliability requirements of 3.3 shall be demonstrated on the maximum configuration computer as specified in 3.1.2 for the production computers in accordance with the following test level C of MIL-STD-781 modified as follows:

Test time	-4600 operate hours
Failures allowed	-3
Producer's risk	-L = 0.2
Consumer's risk	-S = 0.3
Discrimination ratio	-2.07
Temperature cycling	- per para 4.4.1e
On off cycling	- per para 4.4.1e

Operating tests of 4.6.1 shall be conducted continuously throughout reliability testing. With all these exceptions this ceases to be a standard MIL-STD-781 test. The follow-on contract specifies T.P. 29 and a vibration test.

8-1.3 BURN-IN-TEST. In paragraph 4.6.7 the specification states"...with equipment at full power and with its cooling system in normal operation, for 48 hours continuously under the conditions of temperature cycling between 0° and 50°C. The cycle shall be as follows:

a. 4 hours and 0°C
b. 2 hours transition from 0°C to 50°C
c. 4 hours at 50°C
d. 2 hours transition from 50°C to 0°C

Cycle is to be repeated four times. This Burn-In-Test was too short to catch all infant mortality failures. The 1000 hour Burn-In-Test for the follow-on contract will accomplish what this short test failed to do and provide a better product.

8-2 MAINTAINABILITY SPECIFICATIONS

8-2.1 MAINTAINABILITY. The specification states in paragraph 3.4.1.1 "The maximum configuration of the computer shall have a specified mean corrective maintenance time (M ct) of 15 minutes and a specified maximum corrective maintenance time (Mmax) of 120 minutes at a 95 percent confidence level when repair is accomplished by replacement of line replacable item (LRI) and chassis mounted components

(this includes electronic, electro-mechanical, and mechanical parts). The system mean corrective maintenance time includes localization, isolation, disassembly, interchange, reassembly, alignment, and checkout of all maintenance tasks".

8-2.2 LRI-CORRECTIVE MAINTENANCE. Paragraph 3.4.1.2 of the specification states "...Mct for the piece part repair of the repairable LRI - shall be 6 minutes.

8-2.3 QUALITATIVE MAINTAINABILITY REQUIREMENT. The specification states in paragraph 3.4.1.4 "Access panels and doors which must be opened for maintenance or inspeciton more often than monthly shall have a minimum time to open at 30 seconds". It appears that this should read no more than 30 seconds or a maximum of 30 seconds.

8-2.4 DIAGNOSTIC CAPABILITY. The specification states in paragraph 3.4.5.2 "The diagnostic program shall isolate 95 percent of all detectable, active logic element failures to not more than three printed circuit card modules".

8-3 AVAILABILITY SPECIFICATION

8-3.1 AVAILABILITY. The specification states in paragraph 3.3.3.1, a, (1) "Equipment availability for performance within this specification not less than MTBF/MTBF+Mean-Time-To-Repair (MTTR)} specified in 3.3 and 3.4.

8-3.2 MISSION TIME FACTOR. The specification states in paragraph 3.3.3.1,(4) "Mission time factors and equipment utilization: at least 90 percent utilization during a six months cruise". The system to date cannot meet this requirement unless every LRU is supported with approximately two spares each. However, no risk factor to duty cycle requirement is specified.

8-4 TEMPERATURE SPECIFICATIONS

8-4.1 REQUIREMENTS. Paragraph 3.1.3 of the contract specification requires that the computer shall conform to the operating temperature conditions of Class 4 of MIL-E-16400 and the nonoperating temperature conditions of MIL-E-16400, and shall be air cooled using ambient air within the operating temperature specified.

8-4.2 SPECIFICATIONS. MIL-E-16400 Class 4 temperature ranges (ambient) for sheltered controlled environments (ship or shore) operating are 0 to 50^{o}C and nonoperating -62 to +71^{o}C.

SECTION IX - FLEET DATA ANALYSIS

9-1 DATA COLLECTION

9-1.1 Data in the FRAP field study was collected by interview with operating and maintenance personnel and by mail in the form of copies of 3M OPNAV 4790/2K forms returned using pre-addressed envelopes. To allow use of parametric analysis, FRAP instructed sample platforms to include Elapsed Time Meter (ETM) readings with each submission. Numerical data was encoded, keypunched, and statistically reduced using electronic digital computers. Data from interview, narrative comments on the 3M forms, and information from failure analysis was used by FRAP reliability engineers to correlate, interpret and, sometimes, correct data submitted by the Fleet.

9-2 COMPUTER RUN

9-2.1 RMA ANALYSIS. These analysis and the computer output are described in Appendices C and D. Basically the outputs consist of:

(1) Graphs showing:

a. The fit of best fitting probability distribution to FRAP observed times.

b. The fit of other distributions tired. These are given for system and WRA time-to-failure, repair time and system down time.

(2) Tabulation of observed data for time-to-failure, repair, and down time.

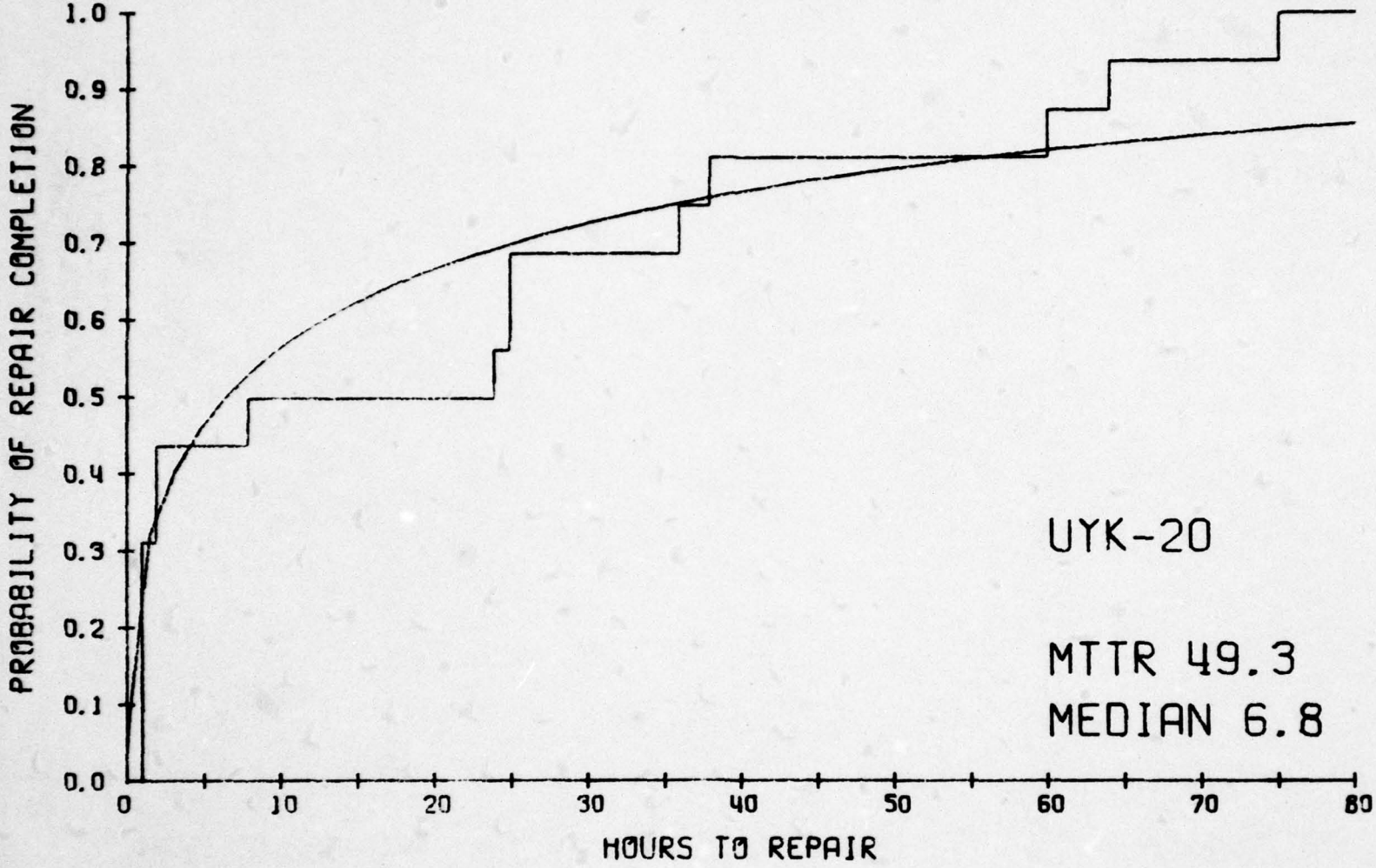
(3) Observed frequency distribution and associated goodness of fit tests and confidence limits for the above parameters.

(4) Confidence intervals on the O-level parts which failed.

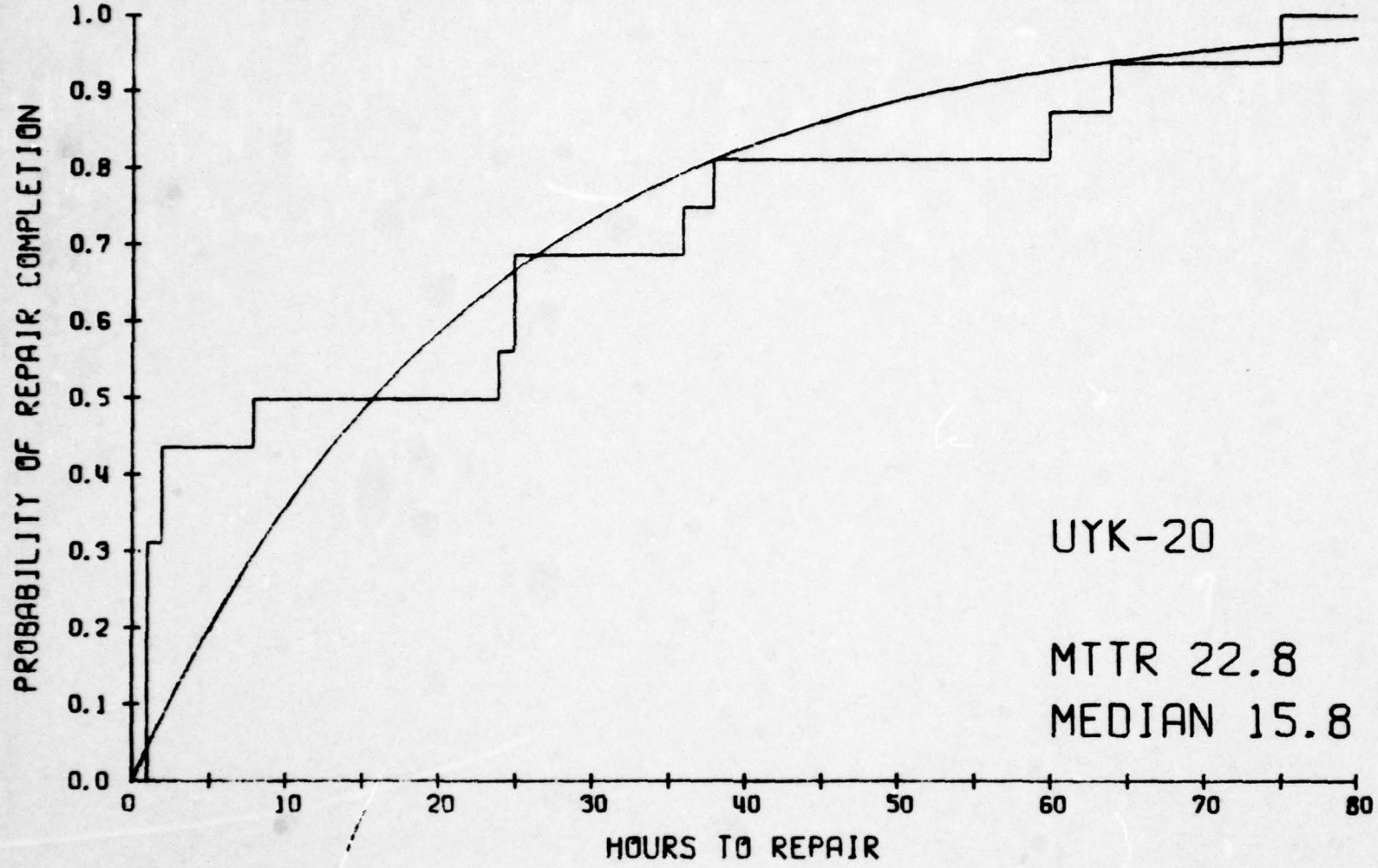
(5) Summaries of 2K forms where problems were detected in either failures or repair time.

(6) Values for inherent and observed (predicted operational) availability.

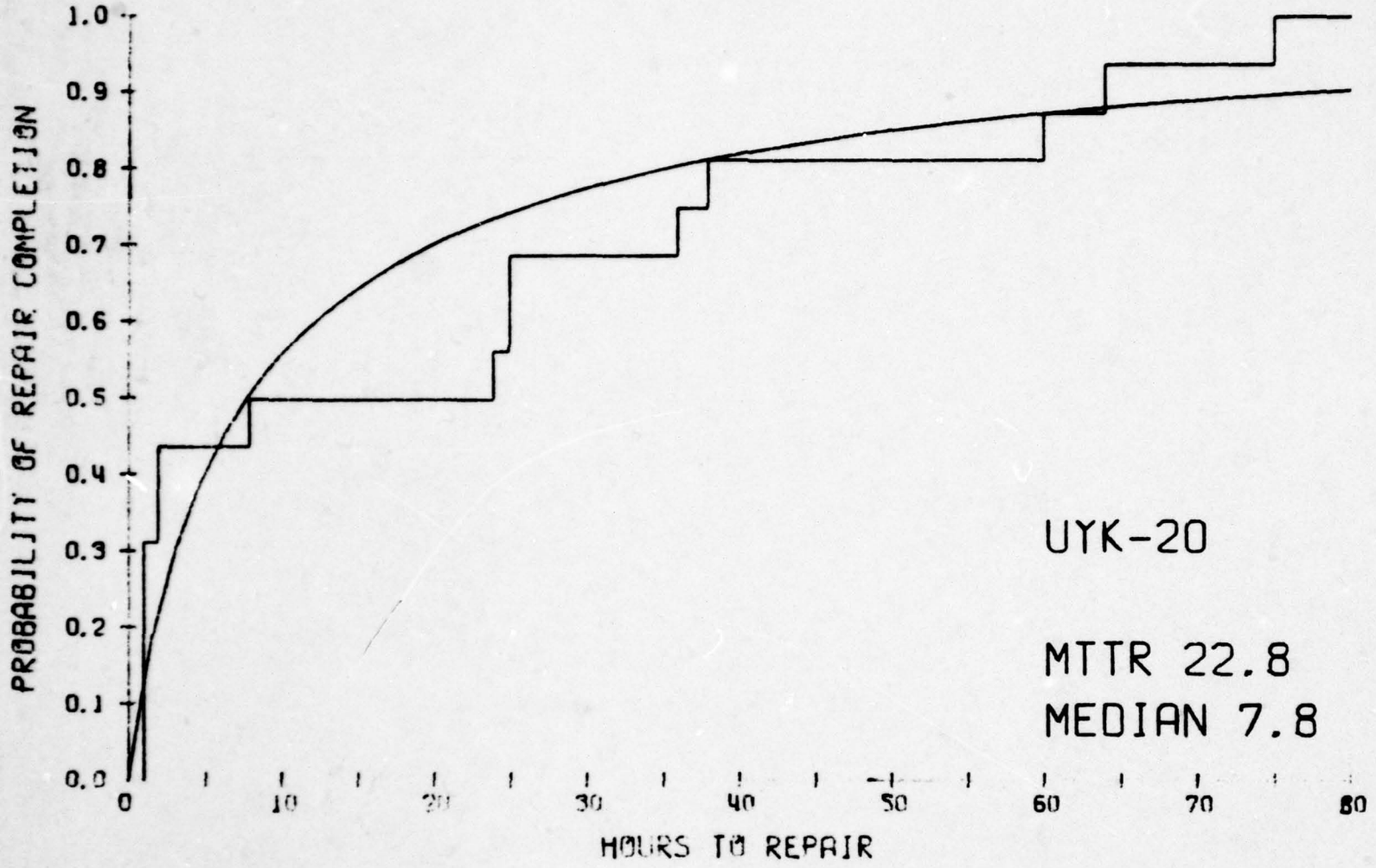
CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
WEIBULL PROBABILITY DISTRIBUTION FOR TIME TO REPAIR



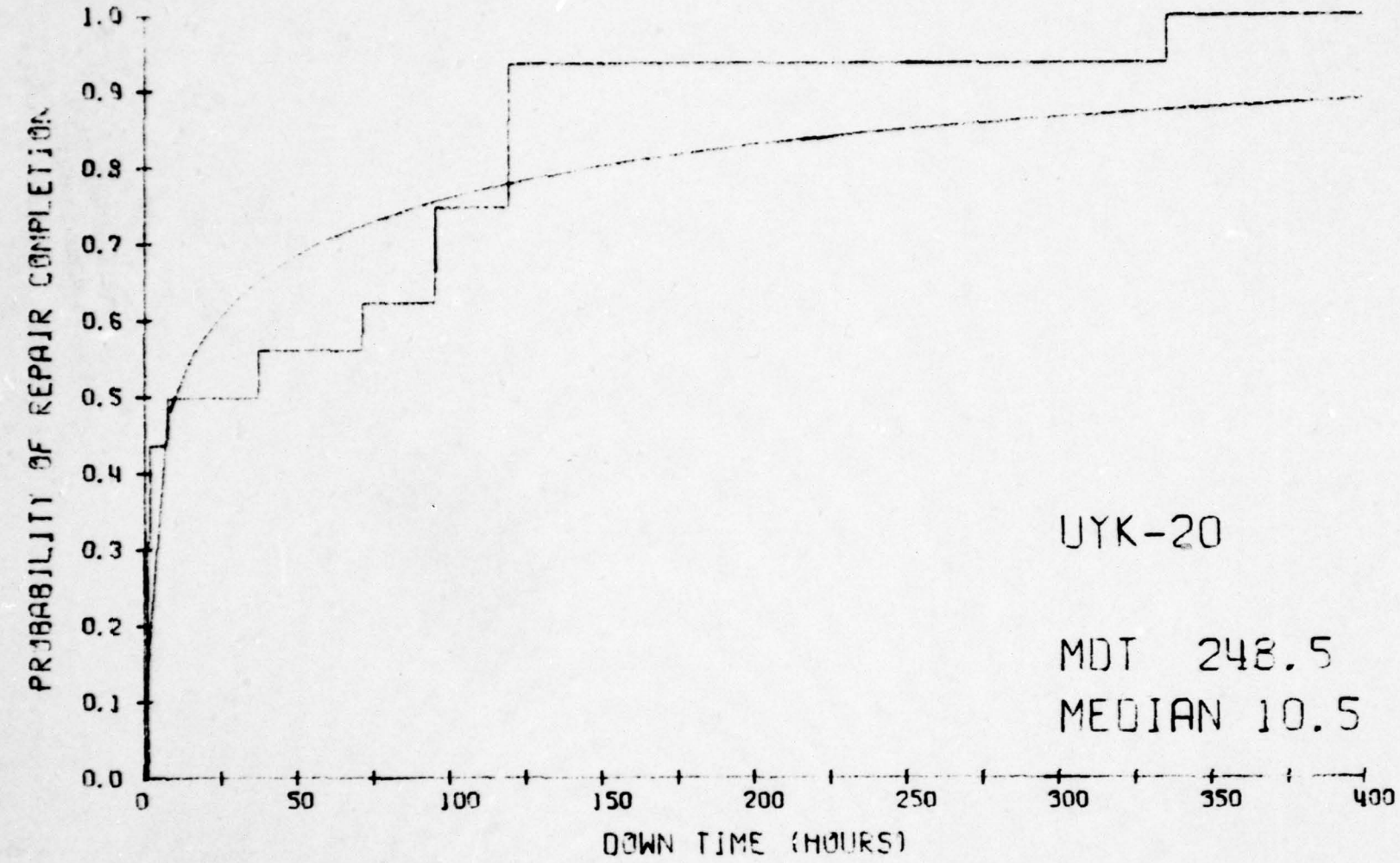
CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
EXPONENTIAL PROBABILITY DISTRIBUTION FOR TIME TO REPAIR



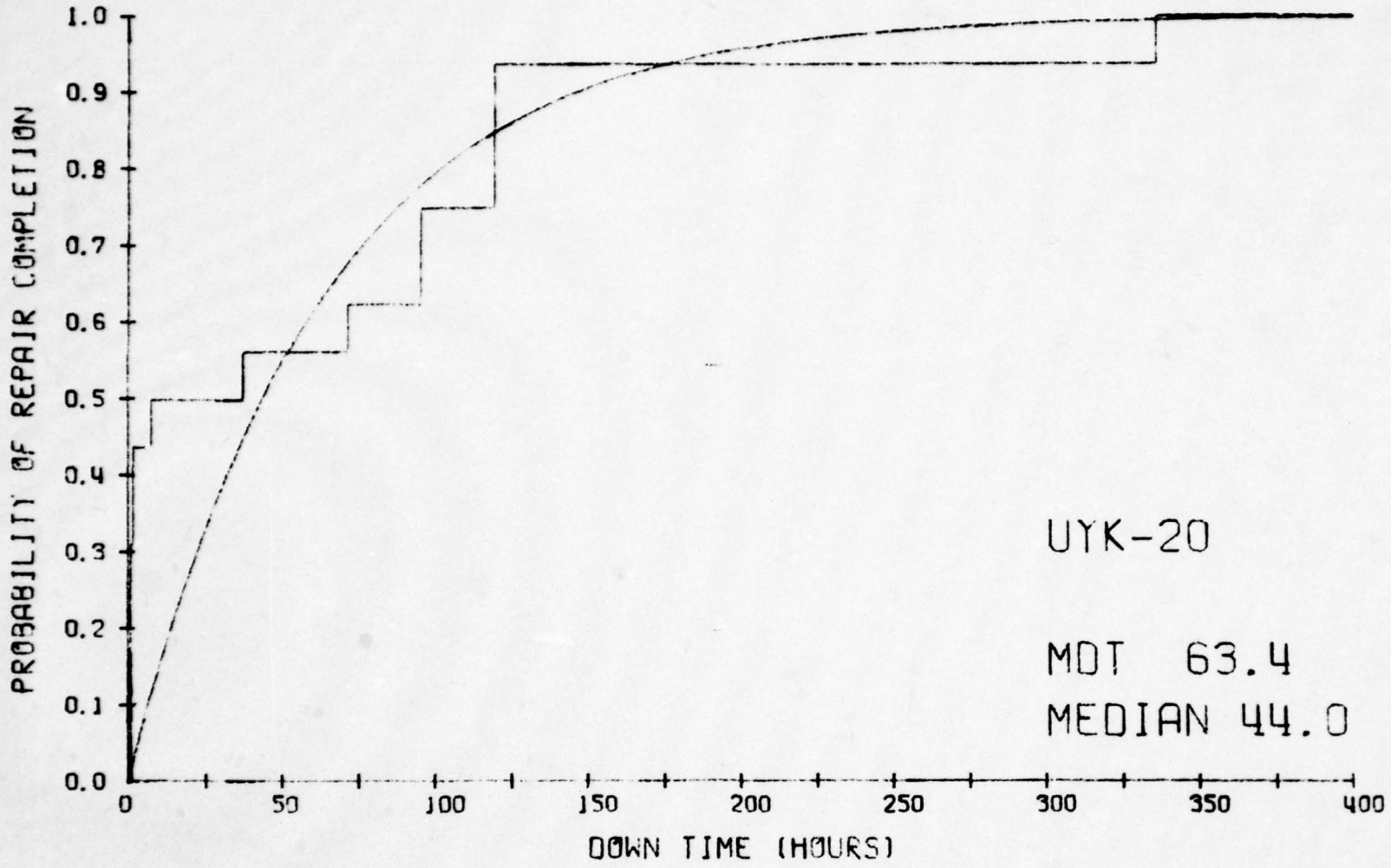
CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
LOGNORMAL PROBABILITY DISTRIBUTION FOR TIME TO REPAIR



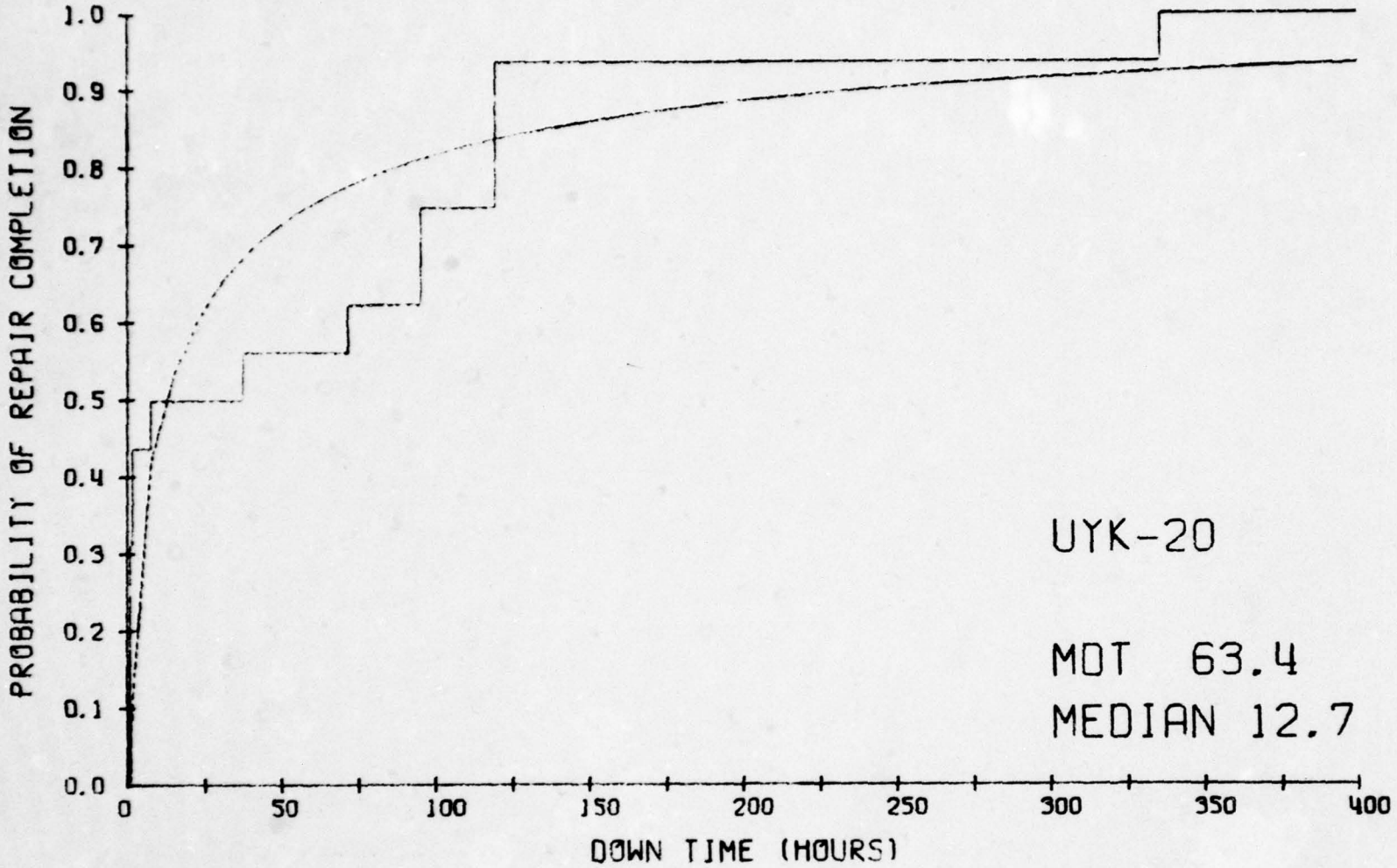
CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
WEIBULL PROBABILITY DISTRIBUTION FOR DOWN TIME



CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
EXPONENTIAL PROBABILITY DISTRIBUTION FOR DOWN TIME



CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
LOGNORMAL PROBABILITY DISTRIBUTION FOR DOWN TIME



FLEET MAINTAINABILITY ASSESSMENT DATA

WRA	OL1	OL2	OL3	DISCOVERY DATE	COMPLETION DATE	DOWN TIME (HRS)	REPAIR TIME (HRS)	SYS	UIC
1	8	4	51	6239	6244	120.0	24.0	3	03364
1	81	0	0	6307	6307	2.0	2.0	3	03364
1	48	0	0	6342	6345	72.0	25.0	3	03364
1	81	0	0	6359	6359	1.0	1.0	3	03365
1	81	0	0	6232	6232	1.0	1.0	3	04668
1	53	0	0	6305	6305	1.0	1.0	3	04668
1	88	0	0	7012	7012	1.0	1.0	3	04668
1	999	0	0	7084	7084	1.0	1.0	3	04668
1	999	0	0	6251	6251	0.0	0.0	3	05139
				NO REPAIR TIME FOR THE ABOVE RECORD					
1	62	0	0	7068	7069	38.0	38.0	3	05154
1	37	81	6	7034	7034	2.0	2.0	3	07178
1	82	0	0	6322	6322	0.0	0.0	3	20001
				NO REPAIR TIME FOR THE ABOVE RECORD					
1	81	0	0	7044	7044	0.0	0.0	3	20001
				NO REPAIR TIME FOR THE ABOVE RECORD					
1	999	0	0	7054	7054	0.0	0.0	3	20001
				NO REPAIR TIME FOR THE ABOVE RECORD					
1	999	0	0	6253	6253	8.0	8.0	3	20044
1	999	0	0	6204	6218	336.0	36.0	3	20122
1	81	0	0	6236	6236	0.0	0.0	3	20122
				NO REPAIR TIME FOR THE ABOVE RECORD					
1	81	0	0	7016	7021	120.0	25.0	3	20122
1	81	81	81	7014	7019	120.0	60.0	3	52702
1	54	62	46	6267	6271	96.0	75.0	3	52702
1	93	94	96	7014	7018	96.0	64.0	3	52702

MAINTAINABILITY (REPAIR TIME)

UYK-20 SYSTEM LEVEL

REPAIR TIME	FREQUENCY	CUM FREQUENCY	NPF	LOGNORMAL	MAX DIFFERENCE
1.0	5.	5.0	.294	.124	.170
2.0	2.	7.0	.412	.222	.190
8.0	1.	8.0	.471	.506	.094
24.0	1.	9.0	.529	.736	.266
25.0	2.	11.0	.647	.744	.215
36.0	1.	12.0	.706	.805	.158
38.0	1.	13.0	.765	.814	.108
60.0	1.	14.0	.824	.875	.110
64.0	1.	15.0	.882	.882	.058
75.0	1.	16.0	.941	.899	.043

TOTAL REPAIR HOURS = 364.0 NUMBER OF REPAIRS = 16. OBSERVED REPAIR RATE/HR = .4396E-01

DISTRIBUTION DETERMINATION

MEAN OF LN'S = 2.05 STD DEV OF LN'S = 1.78

K-S CRITICAL VALUE (.10, 16.) = .195 MAX DIFF CALC = .266 IS GREATER THAN THE CRITICAL VALUE

THEREFORE THE LOGNORMAL DISTRIBUTION CANNOT BE ASSUMED

REPAIR TIME	FREQUENCY	CUM FREQUENCY	NPF	EXPONENTIAL	MAX DIFFERENCE
1.0	5.	5.	.294	.043	.251
2.0	2.	7.	.412	.084	.328
8.0	1.	8.	.471	.296	.174
24.0	1.	9.	.529	.652	.181
25.0	2.	11.	.647	.667	.137
36.0	1.	12.	.706	.795	.147
38.0	1.	13.	.765	.812	.106
60.0	1.	14.	.824	.928	.164
64.0	1.	15.	.882	.940	.116
75.0	1.	16.	.941	.963	.081

TOTAL REPAIR HOURS = 364.0 NUMBER OF REPAIRS = 16. OBSERVED REPAIR RATE/HR = .4396E-01

DISTRIBUTION DETERMINATION

K-S CRITICAL VALUE (.10, 16.) = .236 MAX DIFF CALC = .328 IS GREATER THAN THE CRITICAL VALUE

THEREFORE THE EXPONENTIAL DISTRIBUTION CANNOT BE ASSUMED

WEIBULL DISTRIBUTION ASSUMED, ESTIMATED PARAMETERS ARE ALPHA = .32198E+00 BETA = .40999E+00

EST MEDIAN = 6.769 EST MEAN = 49.326 90 PER CENT LCL ON MEAN = 0.000 90 PER CENT UCL ON MEAN = 99.200

SPECIFIED MTTR = .25 HOURS LOWER CONF LIM 0.00 IS LESS THAN MTTR, THUS THE EQUIPMENT MEETS THE SPECIFICATIONS

MAINTAINABILITY (DOWN TIME)

UYK-20 SYSTEM LEVEL

DOWN TIME	FREQUENCY	CUM FREQUENCY	NPF	LOGNORMAL	MAX DIFFERENCE
1.0	5.	5.0	.294	.132	.162
2.0	2.	7.0	.412	.208	.204
8.0	1.	8.0	.471	.419	.051
38.0	1.	9.0	.529	.685	.214
72.0	1.	10.0	.588	.777	.248
96.0	2.	12.0	.706	.813	.225
120.0	3.	15.0	.882	.838	.132
336.0	1.	16.0	.941	.925	.043

TOTAL DOWN TIME (TDT) = 1015.0 NUMBER OF REPAIRS (NR) = 16. OBSERVED DOWN TIME/REPAIR (TDT/NR) = 63.44

DISTRIBUTION DETERMINATION

MEAN OF LN'S = 2.54 STD DEV OF LN'S = 2.27

K-S CRITICAL VALUE (.10, 16,) = .195 MAX DIFF CALC = .248 IS GREATER THAN THE CRITICAL VALUE

THEREFORE THE LOGNORMAL DISTRIBUTION CANNOT BE ASSUMED

DOWN TIME	FREQUENCY	CUM FREQUENCY	NPF	EXPONENTIAL	MAX DIFFERENCE
1.0	5.	5.	.294	.016	.278
2.0	2.	7.	.412	.031	.381
8.0	1.	8.	.471	.118	.352
38.0	1.	9.	.529	.451	.079
72.0	1.	10.	.588	.679	.149
96.0	2.	12.	.706	.780	.192
120.0	3.	15.	.882	.849	.143
336.0	1.	16.	.941	.995	.113

TOTAL DOWN TIME (TDT) = 1015.0 NUMBER OF REPAIRS (NR) = 16. OBSERVED DOWN TIME/REPAIR (TDT/NR) = 63.44

DISTRIBUTION DETERMINATION

K-S CRITICAL VALUE (.10, 16,) = .236 MAX DIFF CALC = .381 IS GREATER THAN THE CRITICAL VALUE

THEREFORE THE EXPONENTIAL DISTRIBUTION CANNOT BE ASSUMED

WEIBULL DISTRIBUTION ASSUMED, ESTIMATED PARAMETERS ARE ALPHA = .34199E+00 BETA = .31115E+00

EST MEDIAN = 10.500 EST MEAN = 248.478 90 PER CENT LCL ON MEAN = 0.000 90 PER CENT UCL ON MEAN = 665.533

MAINTAINABILITY (REPAIR TIME)

UYK-20 O-LEVEL SUMMARY

WRA	O-LEVEL BLOCK NO.	O-LEVEL NOMENCLATURE	NUMBER REPAIRS	LOWER 90 CONF LIM	UPPER 90 CONF LIM	SPEC MTTR	OBSERVED REPAIR TIMES LOW	MEAN	HIGH	MAINT PROBLEM
1	4 1W5	CABLE ASSBLY	1.	NO CONF LIMITS		.3	24.0	24.00	24.0	
1	6 3A1CB1	CKT BREAKER	1.	NO CONF LIMITS		.3	2.0	2.00	2.0	
1	8 3A1D55	LED INDICATOR	1.	NO CONF LIMITS		.3	24.0	24.00	24.0	
1	37 11A14	MON CLK CTL	1.	NO CONF LIMITS		.3	2.0	2.00	2.0	
1	46 11B11	ALU	1.	NO CONF LIMITS		.3	75.0	75.00	75.0	
1	48 11B16	CLOCK	1.	NO CONF LIMITS		.3	25.0	25.00	25.0	
1	51 11B19	INT STORE	1.	NO CONF LIMITS		.3	24.0	24.00	24.0	
1	53 11B21	TRANSLATOR	1.	NO CONF LIMITS		.3	1.0	1.00	1.0	
1	54 11B23	20 MHZ OSC	1.	NO CONF LIMITS		.3	75.0	75.00	75.0	
1	62 11C19	JUMP AND IA	2.	18.75	152.00	.3	38.0	56.50	75.0	YES
1	81 13	MEM ARRAY BRD	8.	3.15	21.64	.3	1.0	26.38	60.0	YES
1	88 16A1	MK-1720 DVR	1.	NO CONF LIMITS		.3	1.0	1.00	1.0	
1	93 18A1	MK-1721 RCVR	1.	NO CONF LIMITS		.3	64.0	64.00	64.0	
1	94 18A2	JUMPER PLUG	1.	NO CONF LIMITS		.3	64.0	64.00	64.0	
1	96 19A1	MK-1718 DVR	1.	NO CONF LIMITS		.3	64.0	64.00	64.0	
1	999		3.	.93	46.85	.3	1.0	15.00	36.0	YES

MAINTAINABILITY (REPAIR TIME)

2K SUMMARY FOR UYK-20 PROBLEM AREAS

JCN	SYSTEM	WRA	D-L	D-L	D-L	SYSTEM SYMPTON	DIAGNOSTIC	RESULTS
03364DE11M003	3	1	81	0	0	NO 60	MICRO	R+R MAB
03365	3	1	81	0	0	PROG, FAULT	SCOMP DI	ARPL MEM ARA4 BOARD
0466800000000	3	1	81	0	0			R+R MAB
0466800000000	3	1	999	0	0	SHRT P-CHO		
05139DE010362	3	1	999	0	0	BAD CHNL		R+R I/O-NG R+R CPU
05154DC010381	3	1	62	0	0	NO LOAD		R+R BOOTS CARD
07178DE013018	3	1	37	81	6	PBM STPS	ETM JA	M TERMINATED
20001DE02A393	3	1	81	0	0		000000	R+R MAB
20001DE02A394	3	1	999	0	0	OVR HEATING	000000	NOT GIVEN
20044DC010170	3	1	999	0	0		DIAL 1	R R CARD 6B
20122DE011621	3	1	999	0	0	FAILD LGIC	SMOKE	R R COMPUTER
20122DE011635	3	1	81	0	0	PGM FAULT	000333	R+R MAB
20122DE01	3	1	81	0	0	LOCKUP	MICRO-D	R+R MAB
52702DE01A703	3	1	81	81	81	HI DUST+DIR	T	ALSO R+R PCB 39A33
52702DE01A598	3	1	54	62	46	EXH TEMP 35	CO-SCOPE	ALSO R+R R043

RMA SUMMARY UYK-20 EXC SYSTEM LEVEL

TTF DISTRIBUTION IS EXPONENTIAL WITH MEAN = 1721.30

DT DISTRIBUTION IS WEIBULL WITH ALPHA = .34200 AND BETA = .31120 MEAN = 248.48

RT DISTRIBUTION IS WEIBULL WITH ALPHA = .32200 AND BETA = .41000 MEAN = 49.33

INHERENT AVAILABILITY = MTBF/(MTBF+MTTR)

MEAN TIME TO FAILURE = 1721.30

MEAN REPAIR TIME = 49.33

INHERENT AVAILABILITY = .9721

OBSERVED AVAILABILITY (SIMULATION OF RATIOS TTF/(TTF+DT))

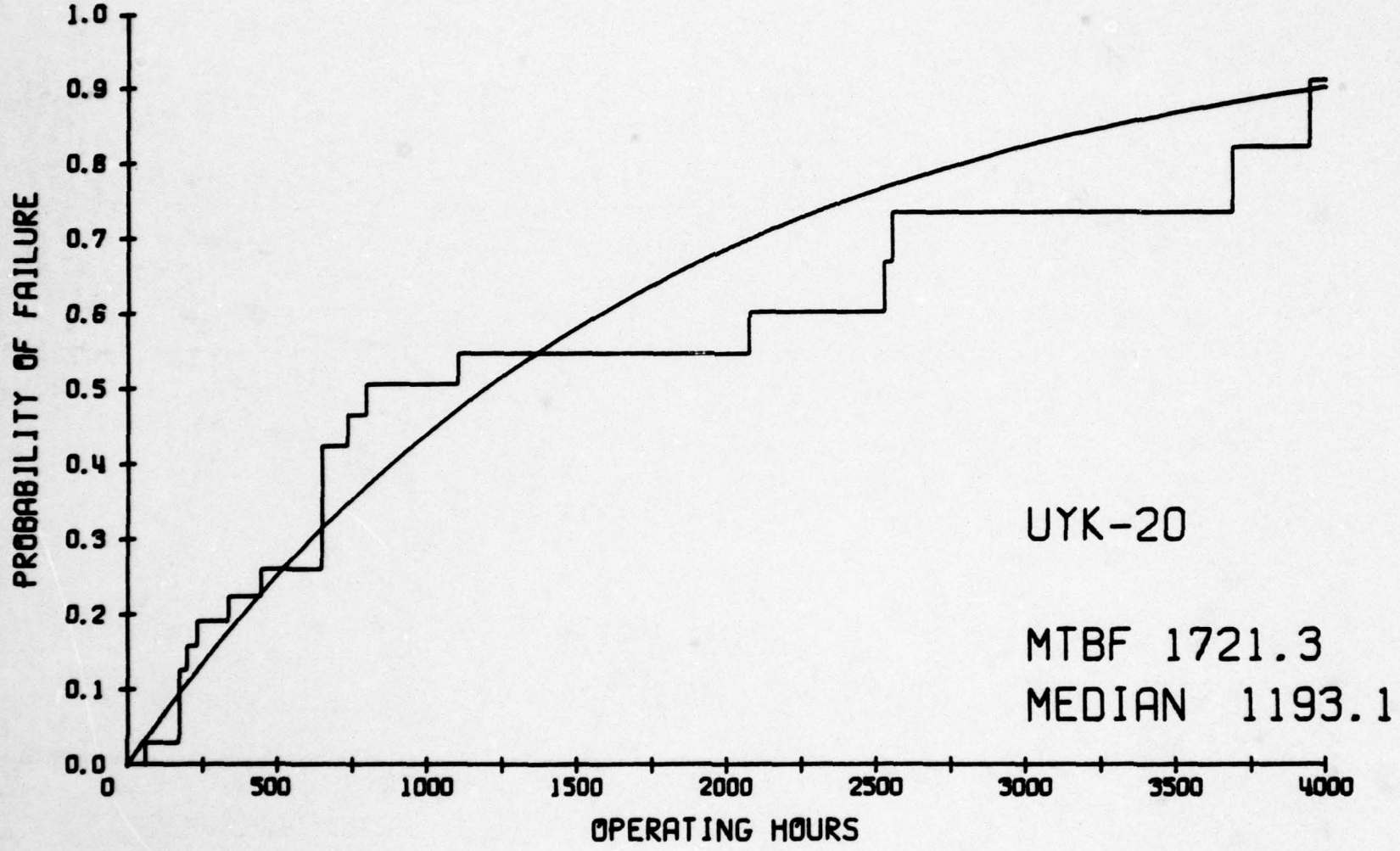
90 PERCENT LCL ON INDIVIDUALS = .6029

90 PERCENT UCL ON INDIVIDUALS = .9966

MEAN = .8932

MEDIAN = .9829

CUMULATIVE OBSERVED DISTRIBUTION VERSUS THEORETICAL
EXPONENTIAL PROBABILITY DISTRIBUTION FOR TIME TO FAILURE



FLEET RELIABILITY ASSESSMENT DATA

MTYP	DATE		NRA	OL1	OL2	OL3	ETM	ETM1	ETM2	OPERATE	DUTY	TTF	SYS	UIC	SHIP NAME	HULL NO
0	6170	0	0	0	0	0	3304.0	0.0	0.0	0.0	0.000	0.0	3	33641	CONSTELLATION	CVA 64
8	6232	6232	0	0	0	0	0.0	3618.0	3618.0	314.0	.211	314.0	3	33641		
3	6239	6244	1	8	4	51	3648.0	3643.0	3648.0	339.0	.191	339.0	3	33641		
4	7039	7039	0	0	0	0	0.0	5081.0	5081.0	1772.0	.316	1433.0	3	33641		
0	6170	0	0	0	0	0	3115.0	0.0	0.0	0.0	0.000	0.0	3	33642	CONSTELLATION	CVA 64
8	6256	6256	0	0	0	0	0.0	3595.0	3595.0	480.0	.233	480.0	3	33642		
3	6307	6307	1	81	0	0	0.0	3852.0	3852.0	737.0	.224	737.0	3	33642		
3	6342	6345	1	48	0	0	0.0	4028.0	4028.0	913.0	.217	176.0	3	33642		
4	7039	7039	0	0	0	0	0.0	4350.0	4350.0	1235.0	.220	322.0	3	33642		
0	6170	0	0	0	0	0	4647.0	0.0	0.0	0.0	0.000	0.0	3	33651	ENTERPRISE	CVN 65
4	7073	7073	0	0	0	0	0.0	6832.0	6832.0	2185.0	.340	2185.0	3	33651		
0	6170	0	0	0	0	0	8616.0	0.0	0.0	0.0	0.000	0.0	3	33652	ENTERPRISE	CVN 65
3	6359	6359	1	81	0	0	0.0	1174.0	1176.0	2558.0	.564	2558.0	3	33652		
4	7073	7073	0	0	0	0	0.0	2935.0	2935.0	4317.0	.671	1759.0	3	33652		
0	6159	0	0	0	0	0	5280.0	0.0	0.0	0.0	0.000	0.0	3	46680	ADAMS,CHARLES	DDG 2
3	6232	6232	1	81	0	0	0.0	5933.0	5933.0	653.0	.373	653.0	3	46680		
3	6305	6305	1	53	0	0	0.0	6586.0	6586.0	1306.0	.373	653.0	3	46680		
3	7012	7012	1	88	0	0	0.0	7239.0	7239.0	1959.0	.374	653.0	3	46680		
3	7084	7084	1	999	0	0	0.0	7892.0	7892.0	2612.0	.375	653.0	3	46680		
4	7084	7084	0	0	0	0	0.0	7893.0	7893.0	2613.0	.375	1.0	3	46680		
0	6153	0	0	0	0	0	97.0	0.0	0.0	0.0	0.000	0.0	3	50580	PLUNGER	SSN 595
4	7019	7019	0	0	0	0	0.0	496.8	496.8	399.8	.072	399.8	3	50580		
0	6112	0	0	0	0	0	69.0	0.0	0.0	0.0	0.000	0.0	3	51100	ABRAHAM LINCOL	SSBN602
4	7057	7057	0	0	0	0	0.0	98.0	98.0	29.0	.004	29.0	3	51100		
0	6136	0	0	0	0	0	109.0	0.0	0.0	0.0	0.000	0.0	3	51160	ETHAN ALLEN	SSBN608
4	7069	7069	0	0	0	0	0.0	650.0	650.0	541.0	.076	541.0	3	51160		
NO INITIAL RECORD-FIRST RECORD USED																
4	7057	7057	0	0	0	0	1400.0	1400.0	1400.0	0.0	0.000	0.0	3	51170	SAM HOUSTON	SSBN609
0	6230	0	0	0	0	0	285.0	0.0	0.0	0.0	0.000	0.0	3	51390	PUFFER	SSN 652
6	6251	6251	1	999	0	0	0.0	485.0	485.0	200.0	.397	200.0	3	51390		
NO INITIAL RECORD-FIRST RECORD USED																
4	7087	7087	0	0	0	0	1510.0	1510.0	1510.0	0.0	0.000	0.0	3	51450	SEA DEVIL	SSN 664
0	6221	0	0	0	0	0	56.0	0.0	0.0	0.0	0.000	0.0	3	51480	HAWKBILL	SSN 666
8	6258	6258	0	0	0	0	0.0	642.0	642.0	586.0	.660	586.0	3	51480		
4	7053	7053	0	0	0	0	0.0	3185.0	3185.0	3129.0	.662	3129.0	3	51480		
0	6159	0	0	0	0	0	1599.0	0.0	0.0	0.0	0.000	0.0	3	51520	FINBACK	SSN 670
NO INITIAL RECORD-FIRST RECORD USED																
3	7068	7069	1	62	0	0	3780.0	3780.0	3780.0	0.0	0.000	0.0	3	51540	FLYING FISH	SSN 673
0	6188	0	0	0	0	0	873.4	0.0	0.0	0.0	0.000	0.0	3	71780	GUAM	LPH 9
0	6317	0	0	0	0	0	419.0	0.0	0.0	0.0	0.000	0.0	3	71781	GUAM	LPH 9
3	7034	7034	1	37	81	6	1219.0	1219.0	1219.0	800.0	.407	800.0	3	71781		
0	6155	0	0	0	0	0	302.0	0.0	0.0	0.0	0.000	0.0	3	200011	WHITNEY,MOUNT	LCC 20
8	6175	6175	0	0	0	0	0.0	338.0	338.0	36.0	.075	36.0	3	200011		
4	7081	7081	0	0	0	0	0.0	475.0	475.0	173.0	.025	173.0	3	200011		
0	6155	0	0	0	0	0	3812.1	0.0	0.0	0.0	0.000	0.0	3	200012	WHITNEY,MOUNT	LCC 20
8	6175	6175	0	0	0	0	0.0	4263.0	4263.0	450.9	.939	450.9	3	200012		
3	6322	6322	1	82	0	0	0.0	7760.1	7760.1	3948.0	.985	3948.0	3	200012		
3	7044	7044	1	81	0	0	0.0	9840.0	9840.0	6027.9	.989	2079.9	3	200012		
3	7054	7054	1	999	0	0	0.0	76.0	76.0	6263.9	.989	236.0	3	200012		
4	7081	7081	0	0	0	0	0.0	715.0	715.0	6902.9	.988	639.0	3	200012		

FLEET RELIABILITY ASSESSMENT DATA

MTYP	DATE		#RA	OL1	OL2	OL3	ETM	ETM1	ETM2	OPERATE	DUTY	TTF	SYS	UIC	SHIP NAME	HULL NO
0	6159	0	0	0	0	0	125.3	0.0	0.0	0.0	0.000	0.0	3	200440	BATFISH	SSN 681
3	6253	6253	1	999	0	0	0.0	301.5	301.5	176.2	.078	176.2	3	200440		
0	6182	0	0	0	0	0	552.0	0.0	0.0	0.0	0.000	0.0	3	201220	KANSAS CITY	AOR 3
3	6204	6218	1	999	0	0	0.0	726.0	744.0	174.0	.201	174.0	3	201220		
6	6236	6236	1	81	0	0	0.0	803.0	846.0	233.0	.180	59.0	3	201220		
3	7016	7021	1	81	0	0	0.0	3376.0	3486.0	2763.0	.564	2530.0	3	201220		
8	7040	7040	0	0	0	0	0.0	4118.0	4118.0	3395.0	.634	632.0	3	201220		
4	7080	7080	0	0	0	0	0.0	4908.0	4908.0	4185.0	.663	1422.0	3	201220		
0	6155	0	0	0	0	0	786.0	0.0	0.0	0.0	0.000	0.0	3	527021	DANIELS,JOSEPH	CG 27
3	7014	7019	1	81	81	81	4475.0	4475.0	4505.0	3689.0	.671	3689.0	3	527021		
0	6155	0	0	0	0	0	854.0	0.0	0.0	0.0	0.000	0.0	3	527022	DANIELS,JOSEPH	CG 27
0	6221	0	0	0	0	0	955.0	0.0	0.0	0.0	0.000	0.0	3	527023	DANIELS,JOSEPH	CG 27
3	6267	6271	1	54	62	46	1404.0	1404.0	1490.0	449.0	.374	449.0	3	527023		
3	7014	7018	1	93	94	96	2598.0	2598.0	2604.0	1557.0	.400	1108.0	3	527023		
4	7081	7081	0	0	0	0	0.0	3127.0	3127.0	2080.0	.385	523.0	3	527023		

R E L I A B I L I T Y

UYK-20 SYSTEM LEVEL

TIME TO FAIL	NO. FAILURES	NO. CENSORED	SURVIVORS	CPDF	EXPONENTIAL	MAX DIFFERENCE
1.0		1.				
29.0		1.				
59.0	1.		31.	.031	.034	.002
173.0		1.				
174.0	1.		29.	.064	.096	.065
176.0	1.		28.	.096	.097	.034
176.2	1.		27.	.128	.097	.031
200.0	1.		26.	.160	.110	.051
236.0	1.		25.	.193	.128	.065
322.0		1.				
339.0	1.		23.	.226	.179	.048
399.8		1.				
449.0	1.		21.	.262	.230	.032
523.0		1.				
541.0		1.				
639.0		1.				
653.0	4.		17.	.426	.316	.110
737.0	1.		13.	.467	.348	.118
800.0	1.		12.	.508	.372	.136
1108.0	1.		11.	.549	.475	.074
1422.0		1.				
1433.0		1.				
1759.0		1.				
2079.9	1.		7.	.605	.701	.153
2185.0		1.				
2530.0	1.		5.	.671	.770	.165
2558.0	1.		4.	.737	.774	.103
3129.0		1.				
3689.0	1.		2.	.824	.883	.146
3948.0	1.		1.	.912	.899	.075

R E L I A B I L I T Y

UYK-20 SYSTEM LEVEL

EQUIPMENT OPERATING HOURS (O.H.) = 34426.9 CALENDAR HOURS(C.H.) = 91824.0 DUTY CYCLE (O.H./C.H.) = .375

NUMBER OF FAILURES = 20. OBSERVED FAILURE RATE/O.H. = .58094E-03

DISTRIBUTION DETERMINATION,

K-S CRITICAL VALUE (.10,20.) = .212

MAX DIFF CALC = .165, IS LESS THAN CRITICAL VALUE THEREFORE THE EXPONENTIAL DISTRIBUTION IS ASSUMED

FOR THE ASSUMED DISTRIBUTION

EST. MEAN = 1721.345, EST. MEDIAN = 1193.145, 90 PER CENT LCL FOR MEAN = 1273.2, 90 PER CENT UCL FOR MEAN = 2370.142

90 PERCENT UCL 2370.14 IS GREATER THAN 2000.00 HOURS, THEREFORE THE EQUIPMENT MEETS THE SPECIFICATIONS

R E L I A B I L I T Y

UYK-20 O-LEVEL SUMMARY

WRA	O-LEVEL BLOCK	O-LEVEL NO.	O-LEVEL NOMENCLATURE	NUMBER FAILURES	LOWER 90 CONF LIM	MEAN	UPPER 90 CONF LIM	SPEC MTBF	OBSERVED FAILURE TIMES LOW	OBSERVED FAILURE TIMES HIGH	RELIAB PROBLEM
1	4	1A5	CABLE ASSBLY	1.	8850,74	34426,90	326754,94	41667,00	339,00	339,00	NO
1	6	3A1CB1	CKT BREAKER	1.	8850,74	34426,90	326754,94	665,00	800,00	800,00	NO
1	8	3A1D55	LED INDICATOR	1.	8850,74	34426,90	326754,94	1000000,00	339,00	339,00	YES
1	37	11A14	MON CLK CTL	1.	8850,74	34426,90	326754,94	852,00	800,00	800,00	NO
1	46	11B11	ALU	1.	8850,74	34426,90	326754,94	2609,00	449,00	449,00	NO
1	48	11B16	CLOCK	1.	8850,74	34426,90	326754,94	980,00	913,00	913,00	NO
1	51	11B19	INT STORE	1.	8850,74	34426,90	326754,94	1477,00	339,00	339,00	NO
1	53	11B21	TRANSLATOR	1.	8850,74	34426,90	326754,94	557,00	1306,00	1306,00	NO
1	54	11B23	20 MHZ OSC	1.	8850,74	34426,90	326754,94	446,00	449,00	449,00	NO
1	62	11C19	JUMP AND IA	1.	8850,74	34426,90	326754,94	742,00	449,00	449,00	NO
1	81	13	MEM ARRAY BRD	10.	2234,55	3442,69	5533,71	521,00	233,00	6027,90	NO
1	82	24A11	MATH PAC	1.	8850,74	34426,90	326754,94	848,00	3948,00	3948,00	NO
1	88	16A1	MK-1720 DVR	1.	8850,74	34426,90	326754,94	190,00	1959,00	1959,00	NO
1	93	18A1	MK-1721 RCVR	1.	8850,74	34426,90	326754,94	156,00	1557,00	1557,00	NO
1	94	18A2	JUMPER PLUG	1.	8850,74	34426,90	326754,94	152,00	1557,00	1557,00	NO
1	96	19A1	MK-1718 DVR	1.	8850,74	34426,90	326754,94	156,00	1557,00	1557,00	NO
1	999			5.	3711,92	6885,38	14152,36	1000000,00	174,00	6263,90	YES

R E L I A B I L I T Y

2K SUMMARY FOR UYK-20 PROBLEM AREAS

JCN	SYSTEM	WRA	D-L	J-L	D-L	SYSTEM SYMPTON	DIAGNOSTIC	RESULTS
03364DE020015	3	1	8	4	51	VISUAL,R BR	K	R+R CRD 7125128
04668D000000	3	1	999	0	0	SHRT P-CHO		
05139DE010362	3	1	999	0	0	BAD CHNL		R+R I/O-NG R+R CPU
20001DE02A394	3	1	999	0	0	OVR HEATING	000000	NOT GIVEN
20044DC010170	3	1	999	0	0		DIAL 1	R R CARD 6B
20122DE011621	3	1	999	0	0	FAILD LGIC	SMOKE	R R COMPUTER

9-3 SUMMARY OF COMPUTER ANALYSIS.

TABLE 6-9.1

Parameter	AN/UYK-20
MTBF	1721 Hours
Not Greater Than	2370 Hours
Not Less Than	1273 Hours
Failures Observed	20
Verification Ratio	0.857
Est. Equipment MTBF	2008 Hours
Not Greater Than	3012 Hours
MTTR	49.3
Operational Availability	.971399

9-3.1 PARAMETERS. Statistical estimates of MTBF and MTTR are given above with appropriate confidence limits calculated at the 90% level.

9-3.2 PROBLEMS IDENTIFIED. No significant problems were identified as a result of computer analysis.

9-3.3 MAINTAINABILITY. The AN/UYK-20 time-to-repair data is not an acceptable fit to the expected Log-normal probability distribution. Neither is the data an acceptable fit to an exponential probability distribution. According to Lillefors K-S criteria, the best fit to the data is a Weibull distribution having a mean (MTTR) of 49.3 hours and a median of 6.7 hours. This means that one would expect a repair to require 49.3 hours on the average, while there is a 50/50 chance that repair can be completed in 6.7 hours or less.

SECTION X - DEPOT DATA ANALYSIS

10-1 BACKGROUND.

10-1.1 RETURNED PARTS REPAIR. The AN/UYK-20 Data Processing Set (DPS) is manufactured by Sperry-Univac, Defense Systems Division, Clearwater, Florida. Depot level repair for DPS modules has been established at the manufacturing plant with parts failure analysis being done by Sperry-Univac, Defense Systems, St. Paul, Minnesota.

10-2 RETURNED PARTS IDENTIFICATION. A problem developed at the supply depot level with parts becoming separated from their ships Maintenance Action Form (2 Kilo) when returned from ships to the Designated Turn-In Points (DIP) for ultimate delivery to the contractor/repair depot. Six of the eleven modules (Table 6-10.1) received by Univac had no maintenance form with them.

10-2.1 PROBLEM ASSISTANCE. The Fleet Repairable Assistance Agent (FRAA) Oakland office was informed of the problem. This office suggested they include in their presentations to ship's crews, information concerning the FRAP program to stress the importance of placing the 2K form in the packing case with the failed module. Their information was that if the 2K form was enclosed with the packing slip on the outside of the container, it would be discarded by the warehouseman at the Supply Depot/Designated Turn-In Point.

10-3 VERIFICATION RATIO. To assist in problem isolation, a verification factor for each 95% + significant module was calculated using:

$$Vf = (N1 + N2/2)/N$$

where N1 = Number of failures confirmed at depot
N2 = Number of non-confirmed failures
N = N1 + N2 = Total number of failures reported by fleet

This equation states that there is an even chance that a non-confirmed failure did malfunction in the fleet but the cause was not discovered at depot level repair. This is perhaps somewhat harsh on the depot test facility, but depot tests open air, room temperature, no vibration affairs, usually on simulation jigs. A verification ratio of 0.85-0.90 (20-30% unconfirmed) is considered average. The possible values range from 0.50 for no confirmations to 1.00 for all returns confirmed as failures. Some types of possible problems that will result in low verification ratios are: Errors in tech manuals, BITE design faults, misapplications, thermal or vibration problems, and correlation problems between module test jigs and actual system operating conditions.

10-3.1 RETURNED MODULE ANALYSIS. Contractor data (Figure 6-10.1) recorded a total of thirteen modules received from FRAP ships. Ten of these modules were found to be defective as confirmed failures.

$$Vf = (10 + 4/2)/14$$

$$= 12.0/14 = 0.857$$

Also: $\theta E = \theta I / Vf$

where: θE = Equip. θ

θI = Inher. θ = 1721

$$\theta E = \frac{1721}{.857} = 2008 \text{ hours}$$

10-4 STRUCTURED ANALYSIS. FRAP has developed a failure ranking technique useful for locating field problems as evidenced by their module return rates. This method takes into account both the numbers of each module used in a system and the complexity of each module. A problem is evidenced by an observed return rate which is significantly larger than the expected return rate. To measure this significance, a Poisson Test of Means is used. The results of this test are expressed in percent and represent the probability that the observed return rates and the expected return rates are truely different, i.e., the resultant value approaches 100% significance if the two rates differ by more than the random error of sampling can account for. In FRAP, 95% significance was chosen as the trigger point for follow-up study.

10-4.1 LABORATORY RETURNED PARTS. A large data base of AN/UYK-20 experience exists at the Naval Ocean Systems Center (NOSC), formerly known as Naval Electronics Laboratory Center (NELC). This data base includes all available failure/malfunction reports (FMR) from the Univac representative and the NOSC maintenance personnel for the period March 1974 to 24 May 1977. The data includes input from 61 AN/UYK Data Processing Sets (DPS) of which 30 were still on board as of June 1977. An analysis was run on three cables and twenty-six PCBs and listed in Table 6-10.2. Column descriptions of as follows:

Col 1: Part number of Printed Circuit Board (PCB)
Col 2: Total number of type of PCB in the Data Processing Set (DPS)
Col 3: Total operating hours of populations
Col 4: N -Failures experienced for this PCB from Table 3
Col 5: Failure rate of PCB = $\frac{\text{Col 4} \times 10^6}{\text{Col 2} \times \text{Col 3}}$
Col 6: NB total DPS failures experienced (major)
Col 7: A Predicted failure rate of the PCB from Relia. Stress Analysis AN/UYK-20 Digital Computer, Univac, Apr 1976
Col 8: B Predicted failure rate for DPS (same source as Col 7)
Col 9: # Spares required for 95% (probability of completing mission) from Figure viii-2-7, Spare Parts Required, from the Maintainability Design Criteria Handbook for Designers of the Shipboard Electronic Equipment, NAVSHIPS 94324, March 1965.
Col 10: Confidence, or probability that the considered part will fail NA times or more. Calculated using Poisson Structured Analysis Program on a HP-65 calculator. If this figure is greater than .95, a problem exists with this item.

A preliminary inspection of Table 6-10.2, column 4, indicates nine items had four or more failures which possibly indicates a problem. However, a comparison of column 4 and 9 shows seven items exceeded their spares allowance and that items 8 and 11 are not critical but item twenty-four with one failure is critical. Column 10 verified these observations with the seven items having values of .95 or greater.

10-4.2 FLEET RETURNED PARTS. Table 6-10.3 lists the analysis results for fleet data which was available at the cutoff date of 22 July 1977. A look at Table 6-10.3 (Column 10) indicates items 1, 2, 4, 7, 12, 16 and 17 are possible problems with a factor of .91 or greater (col 10) and they have also used or exceeded their spares allowance (Col 4 vs. Col 9). However, only items 1, 2 and 7 have equaled or exceeded .95 in Column 10.

FAILED PARTS LIST - FRAP

PART NUMBER	SERIAL NO.	DESCRIPTION	FMR NO.	FAIL RATE	COMMENT
7150354-00	013	Power Supply	C97219	4/23/76	Shorted driver transistors
7128082-00	1407	MAB	C73958	6/6/76	No defect found.
7128082-00	599	MAB	C73959	6/6/76	Cracked core.
7150326-01	055	PCA - 56P	C73960	None	P1 Connector broken. No functional failure.
7092175-01	2480	PCA - 56P	D31125	6/26/76	U2 internal short.
7126166-01	620	PCA - 56P	D31126	None	U4 defective.
7126125-01	621	PCA - 56P	D31144	None	U8 defective.
7125311-01	592	PCA - 56P	D52403	None	U3 defective.
7125136-01	527	PCA - 56P	D52404	None	No defect found.
7125306-01	1117	PCA - 56P	D52402	None	Solder Bridge, evident handling damage.
7128082-00	607	MAB	L07938	12/25/76	Not failure analyzed.
7125128-01	069	PCA - 56P	0E120013	8/30/76	Broken resistor.
7150420-01	601	PCA - 56P	0E120015	8/31/76	No defect found.
7092175-01	4053	PCA - 56P	L07969	None	No defect found.

TABLE 6-10.1

TABLE 6-10.2

PRINTED CIRCUIT BOARD ANALYSIS
ANALYSIS NOSC DPS

PCB P/N	PCB DPS	TOT OP HRS	N_A	F/R EXPR	N_B	A	B	#	P(F N_A)
7092157	4	154,705	3	4.85	254	15.33	3289	6	.17
7092185	3	"	8	17.2	"	13.91	"	5	.99
7092200	1	"	4	25.8	"	12.60	"	2	.98
7101824	2	"	6	19.4	"	26.31	"	6	.98
7119380	2	"	1	3.23	"	21.63	"	5	.18
7119395	2	"	56	181.0	"	31.76	"	7	1.00
7119405	1	"	12	77.5	"	38.14	"	5	1.00
7125157	1	"	4	25.8	"	40.09	"	5	.69
7125236	1	"	1	6.46	"	12.19	"	2	.42
7125240	1	"	1	6.46	"	12.28	"	2	.42
7124306	4	"	4	6.46	"	24.48	"	9	.09
7125380	2	"	1	3.23	"	18.45	"	4	.25
7125405	1	"	1	6.46	"	48.40	"	5	.23
7125926	1	"	3	19.4	"	4.157	"	1	1.00
7126125	2	"	1	3.23	"	17.25	"	4	.26
7126155	2	"	1	3.23	"	10.79	"	3	.22
7126160	1	"	1	6.46	"	11.74	"	2	.44
7126181	1	"	1	6.46	"	11.74	"	2	.44
7126200	1	"	1	6.46	"	22.41	"	3	.21
7126265	1	"	1	6.46	"	15.63	"	2	.33
*7126339	1	"	1	6.46	"	1.684	"	1	.89
7128082	8	"	23	18.2	"	153.5	"	75	.01
7133227	1	"	2	12.9	"	64.02	"	7	.41
*7133909	1	"	1	6.46	"	.4452	"	0	.97
7134994	2	"	5	16.3	"	51.40	"	9	.63
7136295	1	"	1	6.46	"	11.31	"	3	.45
7150320	1	"	2	12.9	"	10.20	"	2	.81
*7150338	1	"	1	6.46	"	2.14	"	2	.86
7150395	1	154,705	1	6.46	254	29.72	3289	4	.12

* Cable Assembly

TABLE 6-10.3

PRINTED CIRCUIT BOARD ANALYSIS
FLEET DPS

PCB P/N	PCB DPS	TOT OP HRS	N_A	F/R EXPR	N_B	A	B	#	P(F N_A)
7092175	4	35,487	2	14.89	20	15.33	3289	2	.95
7092195	1	"	1	28.17	"	12.62	"	1	.99
7101826	1	"	1	28.17	"	-	"	-	-
7101985	1	"	1	28.17	"	15.09	"	1	.91
7119380	2	"	1	14.89	"	21.63	"	2	.77
7119385	1	"	1	28.17	"	32.97	"	1	.82
7119395	2	"	3	42.26	"	31.76	"	2	.99
7119405	1	"	1	28.17	"	38.14	"	1	.79
7125128	1	"	1	28.17	"	85.05	"	2	.60
7125306	4	"	2	14.89	"	29.47	"	3	.84
7126125	2	"	1	14.89	"	17.25	"	3	.81
7126166	1	"	1	28.17	"	13.47	"	1	.92
7126200	1	"	1	28.17	"	22.40	"	1	.87
7128182	8	"	11	38.74	"	153.5	"	23	.87
7136225	1	"	1	28.17	"	-	"	-	-
7136295	1	"	1	28.17	"	11.31	"	1	.93
7150320	1	"	1	28.17	"	10.20	"	1	.94
7150420	1	35,487	1	28.17	20	-	3289	-	-

NOTE: DPS FAILURES (2K FORMS): 20
REPORTED OPERATING HOURS: 34,427
MTBF = 34,427/20 = 1721