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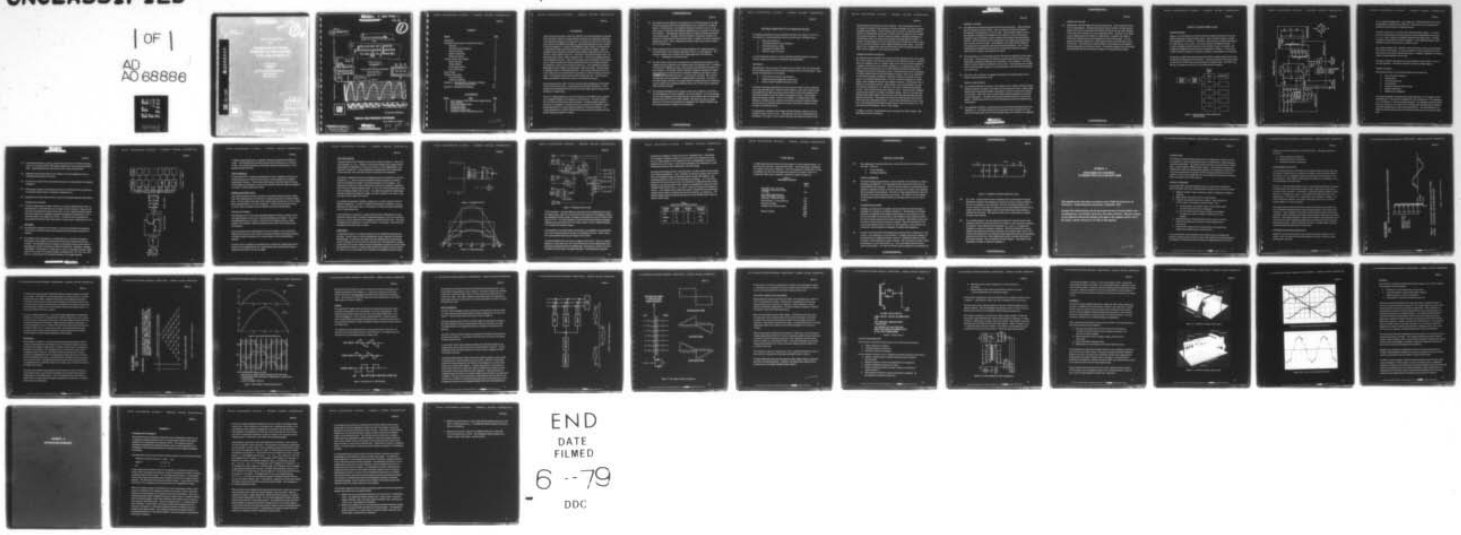

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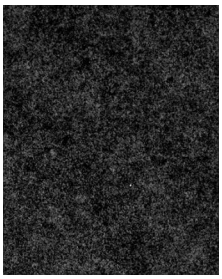

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FOR

(6) # APPLICATION OF A PRECISE CONTINUOUS POWER AMPLIFIER TO THE SQS-26 SONAR ~~(U)~~.

GENERAL MOTORS CORPORATION

Under Contract

~~333-LR-163-1~~ ? Per Navsea

NAVAL SHIP SYSTEMS COMMAND

CODE PMS 387-3

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BACKGROUND

Under Contract 333-LR-163-1 with Code PMS 387 of the Naval Ship Systems Command, Delco Electronics Division of General Motors Corporation is studying the application of a proprietary technique for the generation of precision sine wave power to the transducer drivers of the SQS-26 sonar system. The detailed description of this converter is given in Appendix A. In general, the technique accepts 3-phase, 60 Hz power into a conventional rectifier that produces positive and negative dc voltages. These dc voltages are then switched at the desired output frequency (generally 400 Hz) to produce the "center" portion of the wave. This center is 60 electrical degrees wide. On either side of the center is added a staircase wave. This wave is ascending one side and descending on the other. Since in a three-phase system each phase is 120 degrees apart, 3 center switches and 2 staircase generators plus a set of 6-phase selectors are sufficient to create all of the required waveforms. This organization produces a lightweight converter capable of driving loads of any power factor. Its performance is essentially that of a three-phase alternator. The harmonic distortion in the converter output can be any value desired by the addition or deletion of steps in the staircases. The 60-degree center portion remains fixed in any case. The actual step widths and heights are selected by means of an optimization program.

The precision sine wave power converter has been under development at Delco Electronics for the last two years. Breadboards have been built and operated. These indicate that the techniques described above provide a highly effective means for the generation of 3-phase power.

The use of 3-phase generators to drive the transducer of the SQS-26 sonar appeared to be a possible extension to the application of the converter. The high frequency limit of 4 kHz for the thyristors used was suitable. The phase delays required to beam form as computed on a geometric basis for each layer of the transducer could be approximated by two 3-phase generators offset by 60 electrical degrees. The relative phasing layer-to-layer could be derived from these same generators as long as fixed depression angles were chosen.

(C) After discussion with PMS 387 and examination of the DATOM manuals for the SQS-26 it became apparent that these simplifications are not acceptable for the SQS-26 system. In the first place, the transducer phasing for each layer is not on a geometric basis, but has been experimentally determined so as to generate the required beam patterns. This phasing is further modified to change the transmit beamwidth in the various modes. Secondly, the beam steering is continuously variable in depression to accommodate the bottom bounce mode. In addition, the beam is stabilized against ship motion. This is essential in the BB/TK mode so as to keep the target in the 8.5 degree beam.

(U) These requirements have ruled out the direct application of a 3-phase generator to the sonar problem. The techniques developed, however, are still applicable. The principal attribute of the converter that remains applicable is the following:

- Insensitivity to load power factor.

(C) The power factor of the load on a sonar driver is controlled by the impedance of the transducer and the impedance of the radiation load at the transducer face. In addition, numerous fault conditions can exist, such as open or shorted cables and broken ceramic elements. The radiation load is a function of transducer location with respect to the active area of the array and can be further modified by local faults, such as ~~inoperative~~ inoperative elements within the array. It is safe to say, therefore, that the driver can experience any load impedance, including negative real values. The object of the driver design, therefore, is to operate under all conditions within the voltage and current ratings of the components within the driver and to protect those components under all other conditions.

(U) The techniques developed for the 3-phase converter have produced a circuit that is not only insensitive to the load impedance, but is also bilateral. In the case of negative real load impedances the acoustic energy at the transducer base is rectified and placed on the dc bus for use by other elements. This power flow has no harmful effects on the driver and is limited by the magnitude of the negative impedance and the internal (generator) impedance of the transducer.

DESIRABLE CHARACTERISTICS OF TRANSDUCER DRIVERS

The following attributes have been considered desirable in the design of a driver for the elements of a large transmitting array such as that used in the SQS-26 sonar:

- High overall efficiency
- Controlled generator source impedance
- Controlled harmonic content
- Compatible with digital logic
- Minimum weight and volume.

As in any engineering program, the above attributes should be attained at minimum cost and complexity and maximum reliability and maintainability.

EFFICIENCY

High efficiency in the conversion of the ship's service 3-phase, 440 volt, 60 Hz power into the signals required to drive the sonar transducers has several advantages. These include the minimization of the following:

- Total load on the ship service alternators
- Weight of the power supply and cooling system
- Volume of power supplies and system cooling.

It should be noted that minimization of the total load on the ship's service generators may be less desirable than a reduction of load transients, and in some cases the base load supplied by low efficiency devices such as Class B vacuum tube amplifiers can reduce the magnitude of the load change on the generator system. When weighed against the savings in weight, volume, and reliability, it is apparent that a high-efficiency solid state device is required to provide the necessary transducer signals and that other more desirable means can be used to alleviate the transient loads on the ship's ac distribution system.

The generation of transducer drive signals with high efficiency requires the use of switches in place of linear circuits. This generates waveforms containing step discontinuities. The steps, in turn, generate harmonics that must be controlled in the

interface between the amplifier and the transducer. Since the equivalent circuit of the transducer contains a shunt capacitor at its input terminals, this control requires intelligent circuit design. If shunt tuning is used, each step in the driving waveform produces an instantaneous current that is limited only by the generator source impedance at that same instant. Since the instant in question is during the switching of a semiconductor device, the actual source impedance becomes difficult to define. In practice, the autotransformer used to step-up the driver voltage can be made to saturate, but this again introduces a poorly defined nonlinearity in the circuit. From this point of view, it appears that some series inductance must be introduced between the driver and the transducer to limit these peak currents.

GENERATOR SOURCE IMPEDANCE

By "generator source impedance" is meant the internal impedance of the driver amplifier at each instant of time during the generation of the selected waveform. In general, this source impedance can be a constant voltage source with zero internal impedance, a constant current source with an infinite impedance, or a constant power source. In either of these cases there has to be a careful distinction between the steady state impedance levels and the instantaneous values. Assuming that the driver is operating in a highly efficient mode by using semiconductor switches, there can be a difference in the waveform generator impedance, depending on whether the switches are open, closed, or in transition between states. In order to define the operation of a driver system, these impedances should be fully defined at all times. Unfortunately, this is difficult to do in practical circuits. Many circuits, such as SCR parallel inverters, are forced to commutate the "on" SCR to the "off" state by external energy storage circuits. This is done during the peak voltage of a cycle. Thus the source impedance becomes poorly defined at an instant of maximum voltage. This can, and often does, generate large voltage spikes as the load current flows through instantaneously large generator impedances. These spikes can exceed the voltage ratings of the semiconductor and cause unpredictable failures. Any practical switching circuit must, therefore, limit impedance discontinuities to those times at which the current is low. For well-behaved load impedances, this is at zero voltage.

In addition, current or voltage limiting must be included in the driver design. This also affects the source impedance.

HARMONIC CONTENT

(C) Any highly efficient switched signal generator produces harmonics. These harmonics have two effects on the sonar system. Both are related to forcing the transducer and transducer tuning elements to act as a filter. The first effect relates to the impracticability of predicting the impedance of the transducer at all of the harmonic frequencies under all possible acoustic radiation load impedances and operating frequencies. This becomes particularly troublesome as the range of operating frequencies of modern sonars increases. The probability is very high that the transducer will accept power at frequencies other than the desired frequencies. This, in turn, complicates the already difficult task given to the transducer designer in limiting peak velocities, voltages, and heating to safe values.

(C) The second effect is on the harmonic content of the acoustic radiations from the transducer array. These harmonics fall within the operating frequencies of other sonars, fathometers, underwater telephones and, particularly, active torpedoes. The present status of acoustic radiations underwater is one of chaos. Future systems will certainly have to control harmonic radiations to avoid interference with other systems operating in the same area.

(U) Any driver must, therefore, be capable of generating its waveforms under the constraint of specified harmonic levels.

DIGITAL COMPATIBILITY

(U) In the proposed approach the inputs to the transducer driver module include the desired transmit waveform, the phase of this signal, and the output power level. Ideally, these signals should be generated digitally and supplied to the driver module either serially or in parallel. This would allow the relative phases between elements to be set prior to each transmission. Coincident with the phase information would be a power level setting. Following this would be the actual transmission waveform as required by the sonar system.

(U) The advantages of digitally controlled devices are well known and therefore will not be repeated here. The important thing is that the approach used to generate the transducer drive signal should interface with the digital inputs with a minimum of complexity.

WEIGHT AND VOLUME

(C) High efficiency and low weight and volume go hand in hand. This is particularly true in the cooling required. Assuming an electrical output of 150 kw, the input required would be 167 kw for a driver that is 90% efficient and 250 kw for one of 60% efficiency. 17 kw of heat can be rejected a lot more easily than 100 kw. The other area in which a major weight saving can be made is in transformers. In general, the weight of 60 Hz power transformers can well dominate the overall system weight. For this reason, the minimum weight driver would operate directly across the ship's service 440-volt line. Delco Electronics' system utilizes an autotransformer that handles a small percentage of the sonar system power. Transformer weight in the Delco system will be less than 25% of the transformer weight for conventional sonar systems.

CONCEPT OF SONAR POWER SYSTEM

SYSTEM SUMMARY

Figure 1 is a block diagram of the Delco Electronics design concept which meets the general performance concepts outlined above. These concepts are shown in simplified schematic form in Figure 2. The 440-volt service power is rectified and filtered by D_1 through D_6, and L_f and C_f to provide a positive and negative dc supply. T_1 is used to establish a system neutral to reduce rectifier voltage, if necessary, and to handle the unbalanced current required by amplifiers 1 through N. N could be up to 200, but further subdivision for system redundancy would probably be incorporated.

Q_1 and Q_2 are high voltage switches with shunt diodes to handle reverse current flow. Drivers are incorporated with the switches. These would probably be optically coupled to allow the use of NPN units in both the positive and negative legs. The output of Q_1 and Q_2 is a square wave across T_2 at the desired sonar frequency.

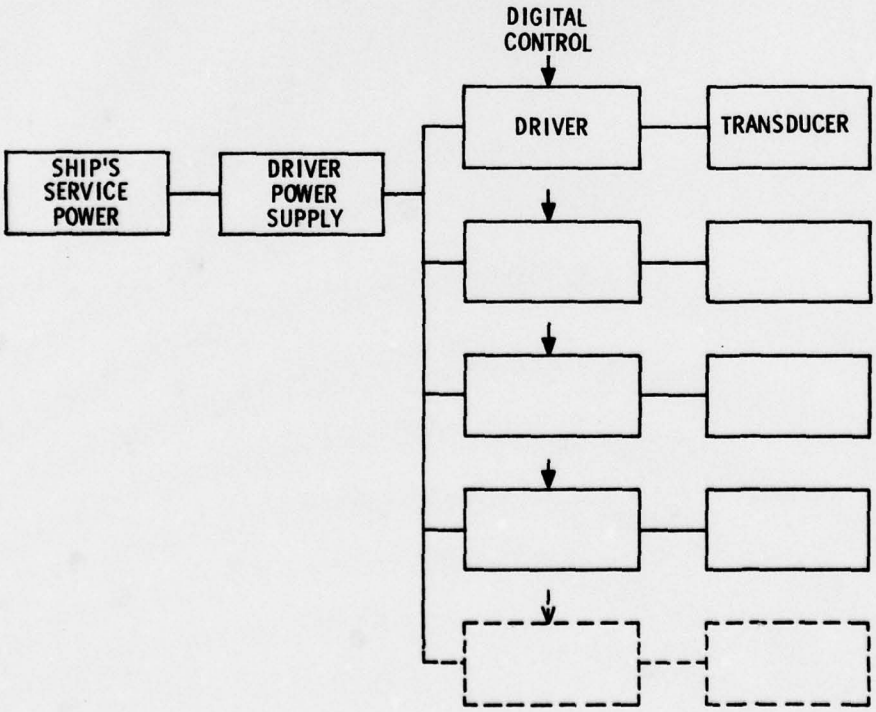


Figure 1 Block Diagram of Delco Electronics Design Concept

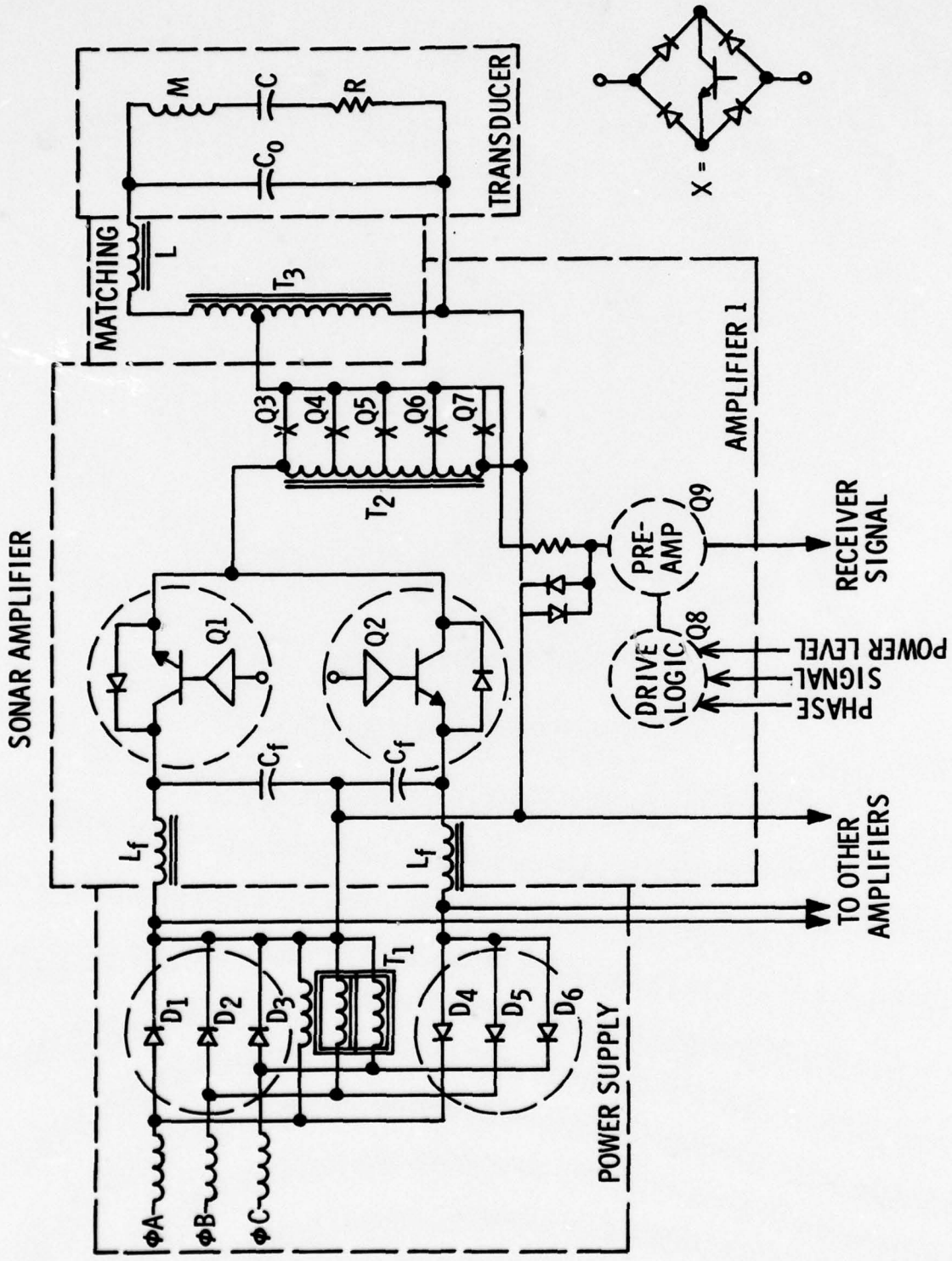


Figure 2 Sonar Amplifier

T_2 is a tapped autotransformer. Q_3 through Q_7 are bilateral switches that connect the appropriate transformer tap to the load. These switches are all referenced to neutral and can be driven by conventional drivers.

The load is made up of T_3 to achieve the required operating voltage. L is used to provide current limiting to the high frequency transients generated by the switches. C_o, M, C, and R represent a simplified transducer equivalent circuit. As shown, no attempt has been made to tune the transducer. Either additional series or shunt inductance would be incorporated in a realistic circuit.

Q_8 contains the digital logic required to drive the switches, and Q_9 is the preamplifier for the received signal. A resistor and diodes are shown as the device to limit input voltage to the receiver during transmission. In addition, blanking of the receiver would be incorporated into the drive logic.

Not shown in Figure 2 are means for current limiting the driver output in case of a low load impedance. This will be included in the final conceptual design.

DESIGN FEATURES

The principal features of the conceptual design as shown above are:

- Very low internal impedance
- High efficiency
- Controlled harmonics
- All solid state
- Suitable for MSI and hybrid circuits
- Modular construction
- Digital logic compatibility.

The internal impedance of the generator is determined by the "on" resistance of the semiconductors. This typically is exhibited by a fixed voltage drop. The impedances of L_f are offset by C_f for the switching transients. The impedance during the switching of Q_3 through Q_7 can be kept low by overlapping the switching times by approximately the expected turn or time of the following device. The self inductance of T_2 limits the current during the short interval when two switches are closed at the same time.

(U) The switching between Q_1 and Q_2 must be done so that one is "off" before the other comes "on" so that the positive and negative supplies are never connected simultaneously. Bypass diodes prevent open circuit at zero voltage across the load.

(U) Additional study is being directed to the problem of current sensing and its use in controlling the operation of the circuit.

(U) The efficiency is about 90% as determined by losses in the semiconductos and magnetic components.

(U) The harmonic content of the waveform can be set to any desired level by the selection of waveforms and the number of switches on transformer T_2.

(U) Discussion of the other features will be covered in the detailed description that follows.

POWER SUPPLY SYSTEM

(C) The power supply shown in Figure 3 consists of a dual band EMI attenuation filter, an interconnected Y autotransformer and a rectifier-dc filter assembly. Energy for the sonar will be supplied by the ship's service 440 v, 60 Hz, 3-phase distribution system. The power supply will be designed to energize 200 amplifiers simultaneously, with a total power input to the transducers of 150 kw. During this mode of operation the sonar system will require 167 kw input power at a power factor of approximately 0.95.

Input Filter

(U) The input filter is divided into two sections: one section provides 100 db attenuation from 14 kHz to 10 GHz; the other section attenuates lower harmonics created by the rectifier.

(U) The rectifier can be considered as a commutating device, and there is therefore a discontinuity in the loading of the power lines which results in distorted 60 Hz line currents. The resulting waveform consists of a fundamental sine wave upon which we superimposed a number of harmonics of different frequencies, magnitudes, and phase relationships. All harmonics of orders $(6a \pm 1)$, where a is any positive integer, appear in the ac line current of the 6-phase rectifier, including the 5th, 7th, 11th, 13th, 17th, 19th, etc., which are the odd nontriplen harmonics of the supply frequency.

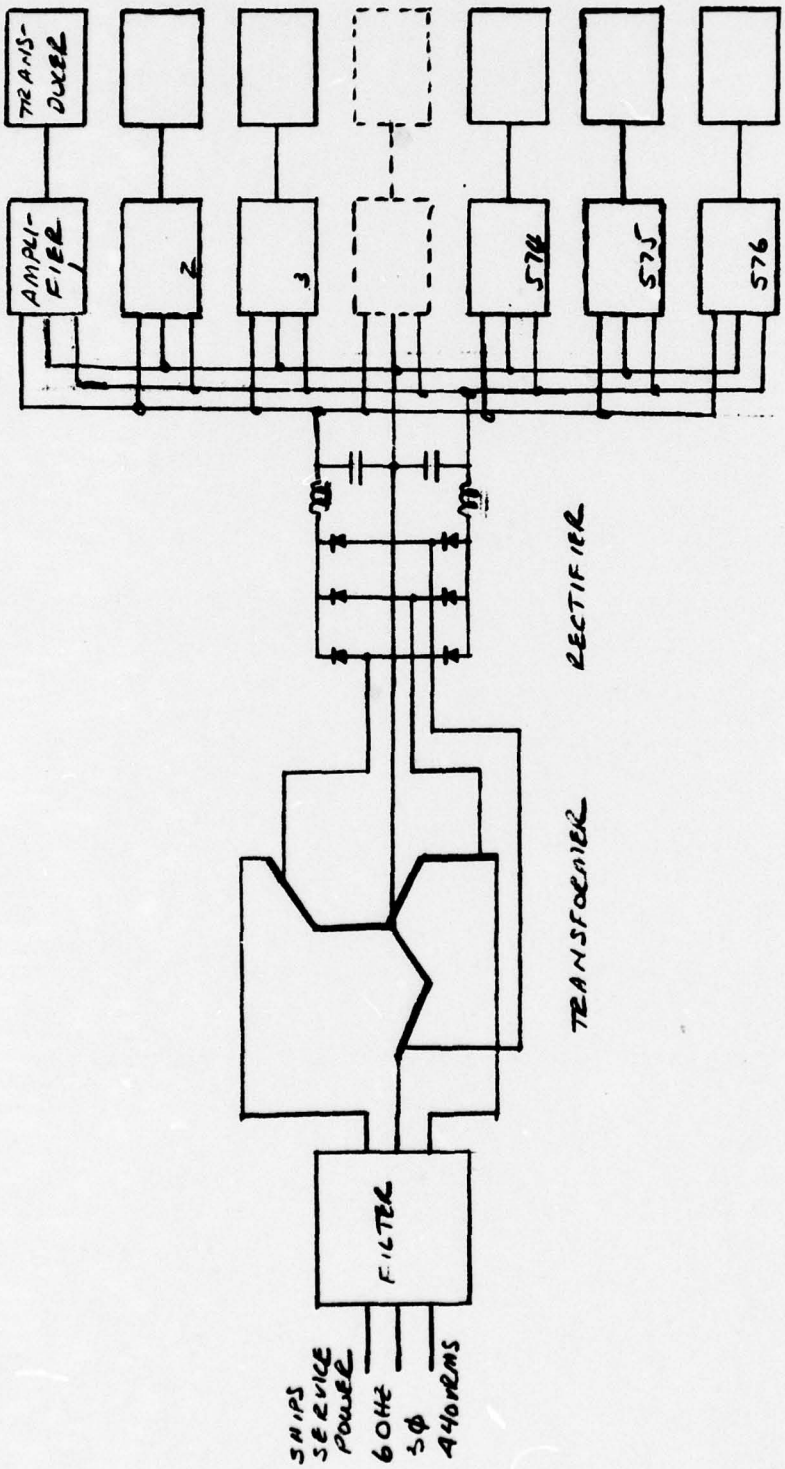


Figure 3 Sonar Power Supply System

A 3-phase interconnected filter is designed to attenuate frequencies from 300 Hz to 14 kHz. A second EMI power line filter provides 100 db attenuation from 15 kHz to 10 GHz. The combined attenuation of both filters reduces all interference to levels specified by MIL-STD-461A.

Power Transformer

An interconnected Y or zigzag autotransformer is used to establish a neutral for the rectifier system and to reduce the line voltage to a level suitable for the amplifier semiconductor switches. Current tends to flow equally in the three legs of the transformer despite load imbalances, and the interconnection offers the minimum impedance to the flow of a single-phase fault current.

Rectifier and dc Filter Circuit

Two 3-phase single-way rectifier circuits are connected in series across the voltage taps of the autotransformer to provide the dc voltage required by the transducer amplifiers. The total ripple at the output of the rectifier diodes across each of the dc voltage lines is approximately 11.3% prior to filtering. A simple inductor-capacitor filter is used to reduce the ripple to the level defined in the system specifications.

DRIVER ELECTRONICS

The transducer driver circuit uses saturating transistor switches to generate a stepwise approximation to a sine wave, whereby high efficiency is achieved. The use of saturating switches also results in a very low source impedance which is closely coupled to the transducer, thereby providing accurate control of the voltage across the transducer.

The incremental nature of the proposed drive circuit enables it to be controlled by digital logic circuits and could result in an attractive interface with a digital computer. A parallel interface is proposed, but a serial interface can be provided easily if required.

The drive circuit is designed to be powered from a balanced dc voltage supply derived directly from the shipboard 440 volt, 3-phase system and to provide three levels of transducer drive power from this dc supply.

Power Switch Circuit

The power section of the transducer drive circuit is shown in Figure 4. Each of the seven switches, S_1 to S_7, consists of a saturating transistor and a bridge rectifier which enables the transistor to control the current in a circuit independently of the direction of current flow. This arrangement is necessitated by the variable power factor of the load, but it also allows full wave utilization of the transistors.

The different voltage levels used in the stepped waveform are obtained from the auto-transformer, T_1, which is switched alternately between the positive and negative halves of the balanced dc supply at the desired transducer drive frequency. The transformer provides four output voltage levels which form a geometric progression with a ratio of 0.6 between adjacent levels. For any one of three chosen power levels, only two adjacent voltage levels are used. As a result of the geometric relationship, the three waveforms are identical in shape, as shown in Figure 5, and result in relative power levels of 100%, 36% and 13%.

T_2 provides the necessary transducer voltage and L is used to limit the current at harmonic frequencies. In order to minimize the dissipation in switches S_1 and S_2 when they are in the active region, it is desirable to correct the nominal load power factor to approximate unity.

In the event that it is necessary to change the power factor compensation to accommodate the desired range of transducer operating frequencies, one or more switches, such as S_7, may be employed to add impedance in parallel with the load. The tuning impedance may be connected to a tap on the inductor, if necessary, to lower the voltage applied to the switch when it is open.

Logic Circuit

As indicated in Figure 5, the stepped waveform cycle is divided into ten equal time intervals. Figure 6 shows the logic mechanization chosen to generate the required timing signals. An eight-bit shift register that gets feedback from the fourth stage is used to generate the five-bit times of a half-cycle and a flip-flop (which is complemented each time the shift register recycles) determines the polarity of the half-cycles. By presetting the flip-flop to a chosen initial polarity and setting a one into a chosen bit of the five active shift register bits, the phase of the stepped wave can be varied

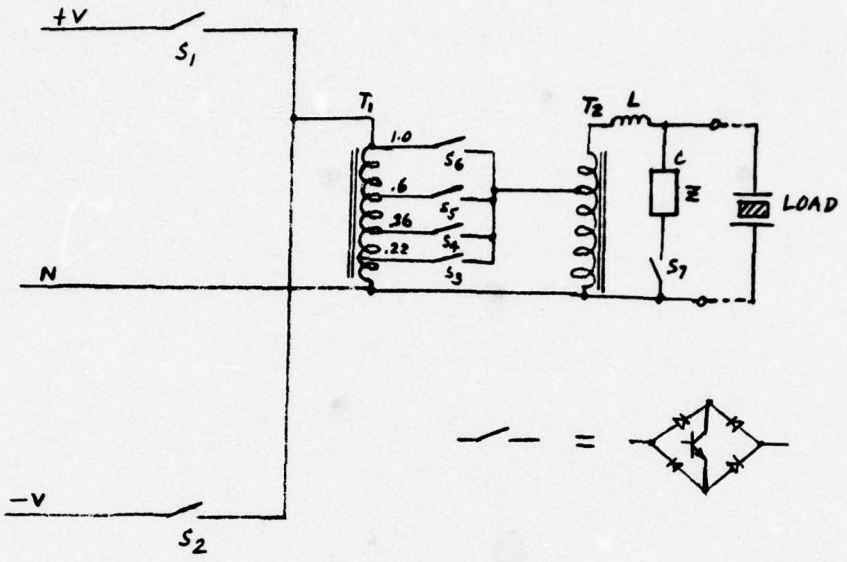


Figure 4 Transducer Driver

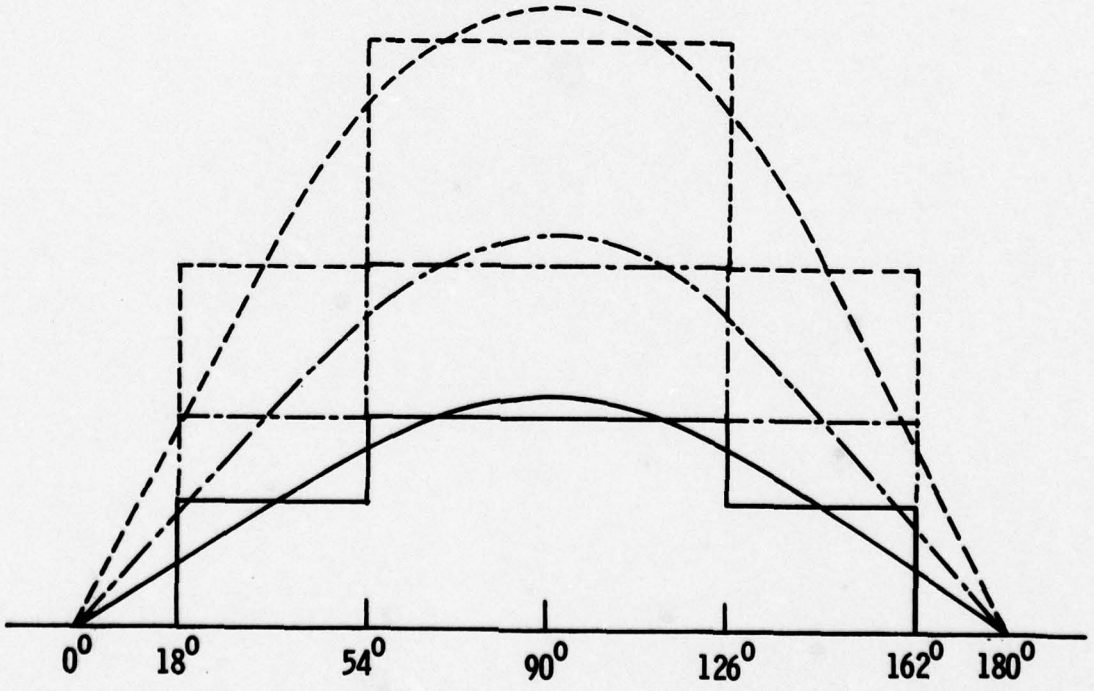


Figure 5 Driving Waveforms

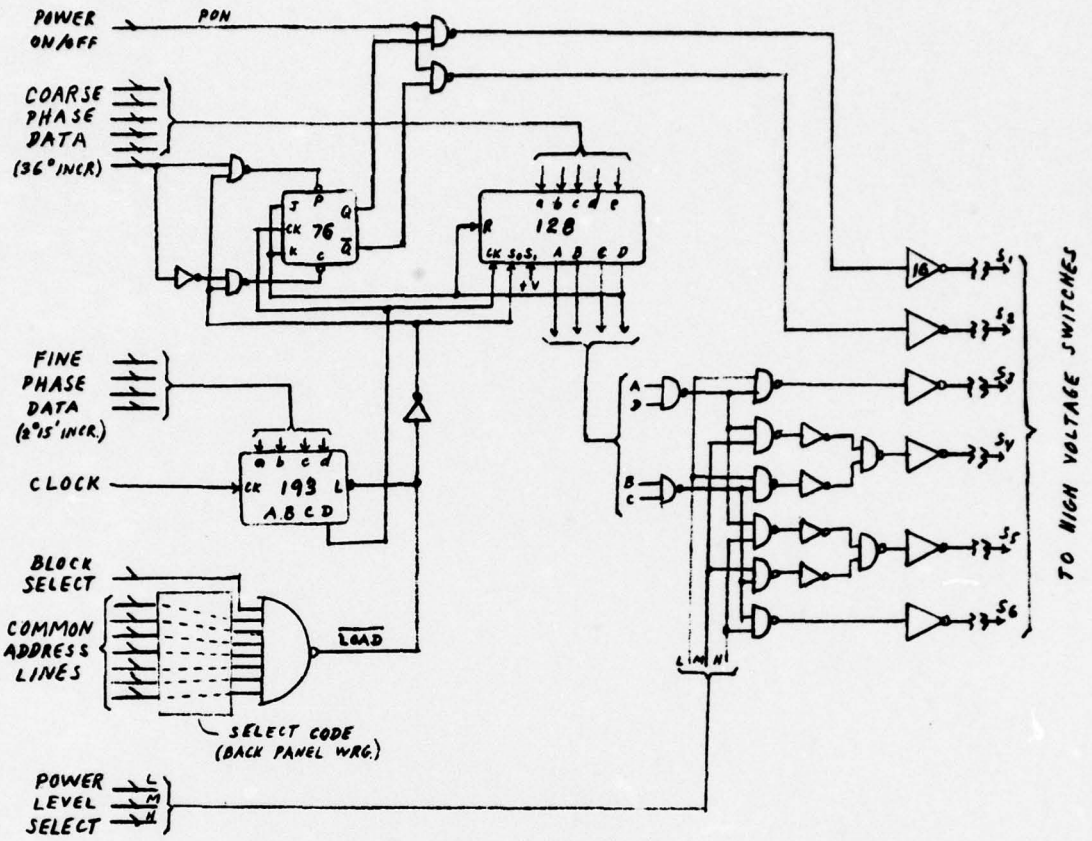


Figure 6 Transducer Driver Logic

in 36° increments. The shift register is driven by the most significant bit of a four-bit timing counter, which is in turn driven by clock common to all transducer drivers. By presetting the binary counter, the phase of the stepped wave can be varied in increments of 2° 15'. The clock frequency is 160 times the desired transducer operating frequency and can be varied over a wide range, either to select a desired frequency or to modulate the transducer signal.

The presetting of the desired phase into the logic is accomplished in parallel fashion over a set of data lines that are common to all transducer drivers. There is also a set of seven address lines that are common to all circuits.

The BLOCK SELECT line is common to a group of 128 circuits. When a true signal appears on a block select line, one of the 128 circuits in the corresponding group is selected by the unique wiring of its address gate, and causes its circuits to be set in accordance with the states of the phase data lines. With appropriate cabling and

interfacing the transducer circuits can be set at a megaHertz rate. Alternatively, at the expense of additional hardware, the phase data can be transferred in serial form to a buffer register in each transducer circuit and subsequently transferred in parallel in the local circuits. In this case the transducer can be operating in a prior setting while the data is being transferred for the next setting.

This phase data loading operation, described above, can also be used to prevent operation of selected transducers. (Note: The power on/off line is common to all circuits.) This is accomplished simply by loading all zeroes into their shift registers, thus preventing operation of any of the four switches S_3 through S_6. S_1 or S_2 will be pulsed once but cannot remain on due to the transformer coupling in the logic outputs. Selection of one of three levels of power output is accomplished by means of the three POWER LEVEL SELECT lines L, M, and H, which are common to all transducer circuits. A true signal on one of these three lines is combined with the decoded shift register states to select an adjacent pair of the four switches, S_3 through S_6. The functions performed by the selected switches for the three possible power levels are shown in Table I below.

Table I
SELECTION OF POWER LEVELS

POWER LEVEL	FIRST STEP	SECOND STEP	RELATIVE POWER
Low	S_3	S_4	13-1/2%
Medium	S_4	S_5	36%
High	S_5	S_6	100%

SYSTEM WEIGHT

A rough estimate has been made of the total weight of a 150 kw amplifier system. As shown in Table II the total is approximately 5000 lb. The largest single component is the 3-phase, 60 Hz power transformer. Since this transformer provides only a moderate stepdown from 440 volts and handles only unbalanced currents to neutral it is considerably lighter than a comparable conventional 3-phase transformer.

Table II
COMPONENT WEIGHTS

	Weight (lb)
EMI/EMC Power Line Filter. Attenuation: 100 db from 14 kHz to 10 GHz	500
Three-Phase Interconnected Filter for Rectifier Generated Harmonics. 300 Hz to 14 kHz	500
Interconnected Y autotransformer	1500
Rectifier Assembly	250
Amplifiers and Timing Circuits	1728
	4478
External Cabling	500
	4978

PROPOSED FUTURE WORK

(U) The continuation of the study effort under contract 333-LR-163-1 will concentrate on two areas. These are:

- Circuit Definition
- Transducer Matching.

CIRCUIT DEFINITION

(U) The detailed design requirements for a driver amplifier will be defined as a result of discussions with PMS 387. It is anticipated that the design will be tailored for the present SQS-26 (CX) transducer. This will allow the selection of semiconductors and magnetic components necessary to provide a specified drive voltage to the transducer and its associated tuning networks. This will be a paper design sufficient to show the feasibility of the approach described in the report. The details of current limiting for the switches and the interface between the transducer and the receiver will be included.

TRANSDUCER MATCHING

(C) Designing a transducer driver amplifier without consideration of the problems of matching it to a transducer is obviously impractical. The problems of controlling the phase and amplitude of the radiated sound pressure at each element in a large array is tied equally to the performance of the transducer and its associated driver. In order to limit the inertial forces within the transducer, some positive control over the velocity of the head and tail masses is required. Since the beam pattern of the array can be defined in terms of velocity as well as pressure, velocity control can provide well controlled patterns independent of radiation load impedances.

(U) In order to study the effect of the stepped input waveform from a voltage source on the velocity of the radiating face of the transducer, a computer simulation is planned. At the present time a simplified equivalent circuit for a longitudinal radiator as shown in Figure 7 is being analyzed by Laplace methods. The circuit shown includes a series tuning inductor L_s and a shunt inductor L_p. The circuit shown has been solved in terms of the operator S for input current and current through the loop containing Lm,

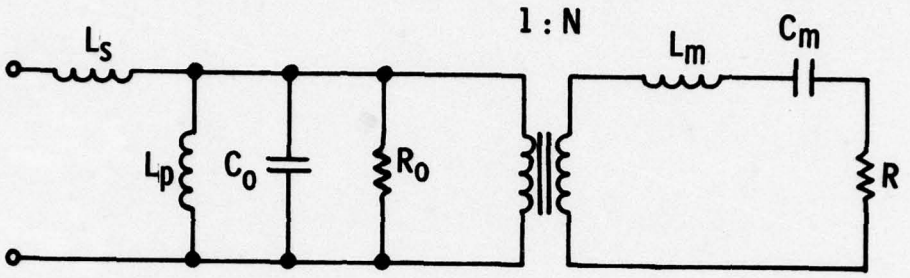


Figure 7 Simplified Transducer Equivalent Circuit

(U) Cm, and R. Typical values for these components will be selected based on typical SQS-26 (CX) transducer and radiation load impedances and the transient response of the circuit computed for a unit step input. Once the time domain response of the circuit is known to a unit step, the response to any selected stepped waveform may be readily calculated by the addition of the unit step solution with proper attention to amplitude and time delay. This approach allows one to examine both the transient and steady state solutions.

(C) It is presently planned to take the steady state solution for current (velocity) in the mechanical loop of the circuit and use this as an input to a Delco Electronics optimization program. This would select the best values of L_s and L_p to minimize the variations in velocity as a function of frequency. This will be repeated for various radiation load impedances and under constraints on the allowable input current. The result of this analysis will be an optimized tuning arrangement based on the limitations imposed by the model used. More sophisticated models, including radial effects in the ceramic elements, could be utilized in the same analysis. A description of the optimization technique is included as Appendix B.

APPENDIX A

DEVELOPMENT OF A CONVERTER TO PRODUCE PRECISION SINE WAVE POWER

This appendix is the main body of a technical report (TR69-52) prepared by AC Electronics - Defense Research Laboratories in September 1969.

Recently Delco Radio Division and AC Electronics Division of General Motors were consolidated into a new division called Delco Electronics Division. This fact accounts for the difference between the headings of the pages in this appendix and the rest of this report, and the references to AC-DRL in this appendix.

INTRODUCTION

New methods for generating three-phase sine-wave voltages from dc power sources is the subject of a recent comprehensive study at AC Electronics - Defense Research Laboratories (AC-DRL). The primary objective has been to develop dc link, variable speed, constant frequency (VSCF) system concepts. The numerous techniques and insights which evolved are presently being applied to the development of various electrical power systems that are competitive with existing mechanical and electrical systems in terms of size, weight and cost while providing the reliability and maintainability commensurate with static systems.

CONCEPT GUIDELINES

The AC-DRL VSCF concept development program was based upon the following general guidelines which were established after thorough review of existing concepts:

1. Whenever possible, reduce transformer weight by adding semi-conductor switches.
2. Make transformers perform dual or triple functions.
3. Construct the waveform from line-to-neutral. This technique has a direct impact on transformer and filter weight, since
   a) An inherent four-wire system results, thus avoiding creation of a load neutral with a power transformer.
   b) All of the third harmonic and its multiples are cancelled in summing line-to-neutral voltages to produce line-to-line voltages.
4. Maximize the power switched directly from the source to the load. Directly by-passing any transformers reduces weight and cuts power losses.
5. Condition the remaining power through switches and transformers, thereby performing harmonic content reduction.

It was reasoned that if these guidelines were followed, many of the undesirable features of existing systems could be avoided. This approach has provided significant new insight into waveform construction and system organization which result in an

impressive reduction in weight of dc link VSCF systems. The weight reduction results from:

A. Unique Transformer Utilization
B. Optimized Waveform Construction
C. Advanced Commutation Techniques.

TRANSFORMER UTILIZATION

If it is assumed that power is available from a 3-phase rectifier such that equal plus-and-minus dc voltages relative to neutral are available, then the simplest method of converting dc to ac is to generate a square wave and filter out all harmonics of the basic frequency. Filter weight in this approach is prohibitive, thus leading to a stair-step approximation to the sine wave.

Basically, a stair-step approximation must be accomplished by adding and subtracting various selected level voltage steps or square waves in appropriate order and time duration to yield a sine wave. Conceptually, the indicated algebraic addition requires the use of n transformers, where n is the number of voltage levels used in the approximation. Practically, the n transformers can be reduced to utilizing n different transformer primaries, each with an appropriate turns ratio, to yield the desired voltage in a common secondary.

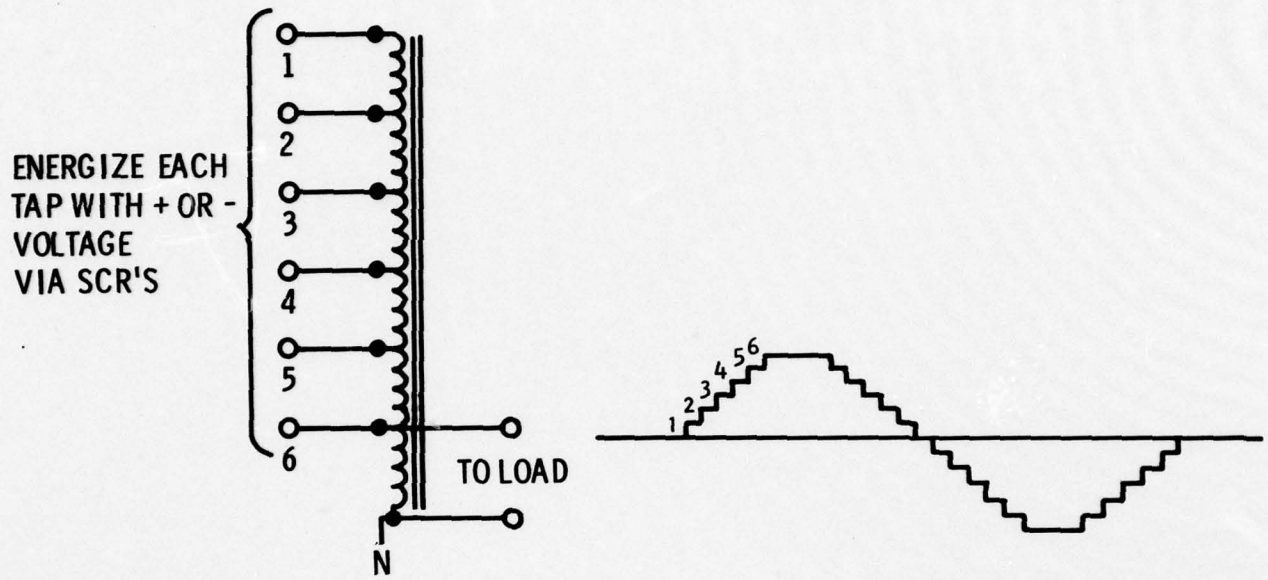
The weight saving motivation behind such sharing of the transformer secondary has led to the logical evolutionary step of using an autotransformer in the manner shown in Figure 1. When compared to three-phase inverters using summing transformers, substitution of the autotransformer results in approximately a 40% transformer weight reduction. This unique transformer utilization was evolved by following guidelines one and two and was the first significant weight reduction achieved during the conceptual development program. Further transformer and other component weight reductions resulted through optimized waveform construction.

OPTIMIZED WAVEFORM CONSTRUCTION

Adoption of a stair-step approach to wave construction raises a question as to the number, level, and duration of the steps necessary to produce a wave that closely approximates a sine wave.

AC-DRL PROGRAM :

STEP 1 REPLACE FULL TRANSFORMERS WITH SINGLE AUTOTRANSFORMER



PENALTY: EACH SCR MUST PROVIDE UP TO FULL LOAD CURRENT

SAVINGS: APPROXIMATELY 40% TRANSFORMER WEIGHT

Figure 1 Autotransformer Concept

To answer these questions the AC-DRL Optimization Computer Program was applied to the studies. One instruction in the program was to minimize the line-to-line total harmonic distortion (THD). Assumed as variables in the optimization calculation were both the values which the line-to-neutral voltage level could take and the times at which the line-to-neutral driving function could assume each of these voltage values. The optimization computer study was thus made consistent with guideline three: construct the waveform from line-to-neutral.

The set of solutions obtained for n equal one to eight voltage levels is summarized in Figure 2. The number 1.0 represents the maximum voltage value in any step and the other numbers are fractions of this value. The small numbers provide the timing (in electrical degrees) for each level. When this firing diagram is translated into waveform diagrams, the line-to-neutral (LTN) and line-to-line (LTL) waveforms are as shown in Figure 3 for n equal to seven steps. By constructing the optimized three-phase line-to-neutral waveforms shown in Figure 4 (again for seven steps), valuable insight into VSCF system organization can be obtained.

Observations

With reference to Figure 4, an observation which has significant impact is that the center sixty degree portion of each half cycle is constant at the maximum value (independent of the number of steps chosen). Further, each half-cycle is comprised of three equal time intervals. For convenience they are referred to as Left, Center, and Right portions of the wave. The Left portion has the property that it always increases (in magnitude) from zero to the maximum voltage; this is true in both the positive and negative half cycles. As indicated above, the Center portion is constant at the maximum value. The Right portion has the property that it always decreases (in magnitude) from the maximum voltage to zero; again, this is true for both positive and negative half-cycles.

The final critical insight is that during the Center portion of a cycle in one phase of a three-phase system, one of the other two phases is in its Left portion and the remaining phase is in the Right portion. Also at any instant of time, these Left and Right portions are always the same polarity and opposite to the polarity of the Center portion of the remaining phase.

AC-DRL PROGRAM

STEP2 COMPUTER OPTIMIZATION PROGRAMS

QUESTION ASKED: IF ARE WILLING TO USE n VOLTAGE LEVELS (TAPS ON THE AUTOTRANSFORMER), WHAT SHOULD THOSE LEVELS BE, AND AT WHAT TIMES* SHOULD THEY BE SWITCHED IN TO MINIMIZE LINE-TO-LINE TOTAL HARMONIC DISTORTION?

n	Voltage Levels (fraction of maximum) and Firing Angles
1	1.0
2	$.58_{21.3^\circ}$ 1.0_{60°
3	$.36_{14^\circ}$ $.65_{34.2^\circ}$ 1.0_{60°
4	$.30_{10.6^\circ}$ $.56_{25.2^\circ}$ $.74_{41.1^\circ}$ 1.0_{60°
5	$.25_{8.4^\circ}$ $.49_{20.1^\circ}$ $.67_{32.4^\circ}$ $.79_{45.2^\circ}$ 1.0_{60°
6	$.20_{7.3^\circ}$ $.40_{16.6^\circ}$ $.58_{26.7^\circ}$ $.71_{37.2^\circ}$ $.80_{48^\circ}$ 1.0_{60°
7	$.17_{6.6^\circ}$ $.36_{14.4^\circ}$ $.52_{23.1^\circ}$ $.65_{31.7^\circ}$ $.75_{40.7^\circ}$ $.81_{49.9^\circ}$ 1.0_{60°
8	$.15_{5.7^\circ}$ $.32_{12.6^\circ}$ $.47_{20.1^\circ}$ $.60_{27.7^\circ}$ $.70_{35.4^\circ}$ $.78_{43.2^\circ}$ $.83_{51.5^\circ}$ 1.0_{60°

*This variable is not used in other methods

Figure 2 Voltage Levels and Firing Diagram

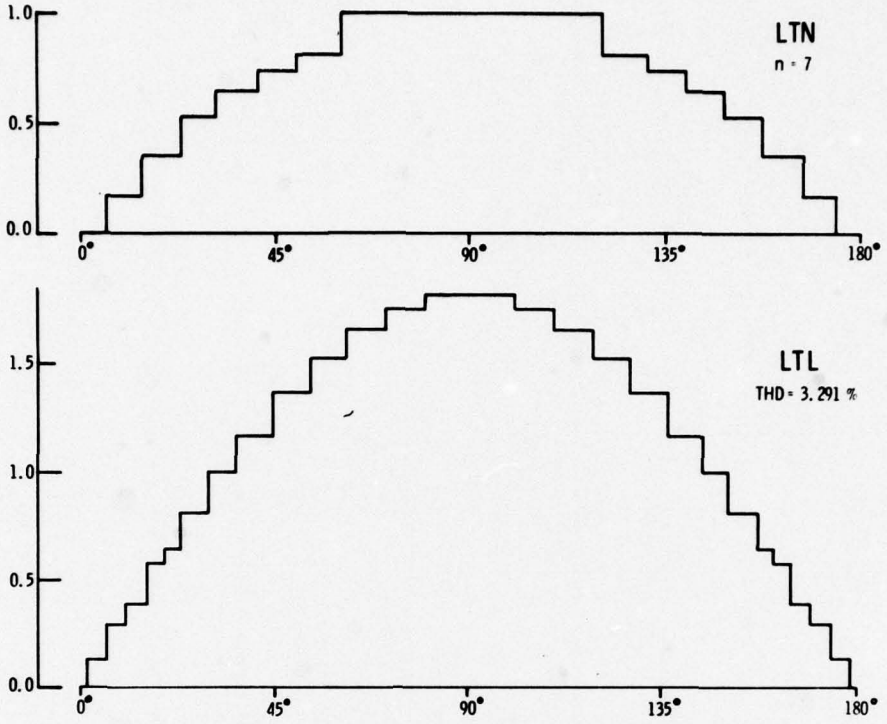
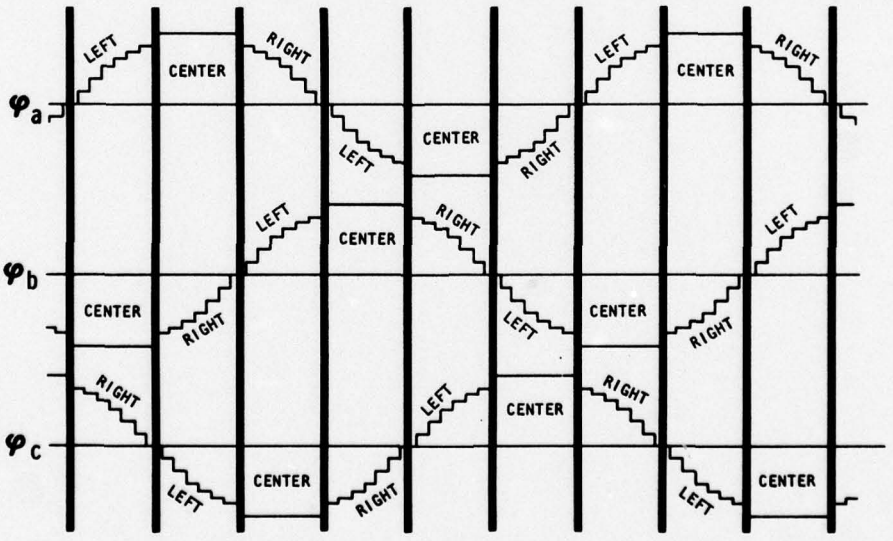


Figure 3 Seven Step Optimized Waveform



WITHIN THE MARKED 60° INTERVALS, WE HAVE

1. ONE PHASE WITH "CENTER", OTHER TWO PHASES ARE "LEFT" AND "RIGHT"
2. "LEFT" AND "RIGHT" PHASES ARE ALWAYS OF SAME POLARITY, AND OPPOSITE TO "CENTER" POLARITY
3. POLARITIES ALTERNATE EVERY 60°.

Figure 4 Three-Phase LTN Optimized Waveform

When the above observations are used to construct the waveforms obtained by time sequencing between the three phases (i.e., Center ϕ_a to Center ϕ_b to Center ϕ_c), periodic waveforms with three times the frequency of the desired output frequency result. The waveforms for such Left, Right and Center sequencing in a basic 400 Hz output system are shown in Figure 5.

Analysis

The observed 60° constant Center portion has such important implications relative to system implementation that it was decided to verify this mathematically. The mathematical verification shows that the line-to-line voltage [defined g(t)] can be constructed exactly by a line-to-neutral voltage [defined f(t)] that has the same period as g(t) and has the following interesting property: one third of a half cycle of f(t) is specified arbitrarily, and the remaining two thirds of the half cycle are derived according to g(t).

The mathematical proof substantiates the computer optimization of the wave, and clears the way to set the Center portion, quite arbitrarily, to a constant value, and then select the Left and Right portions according to g(t).

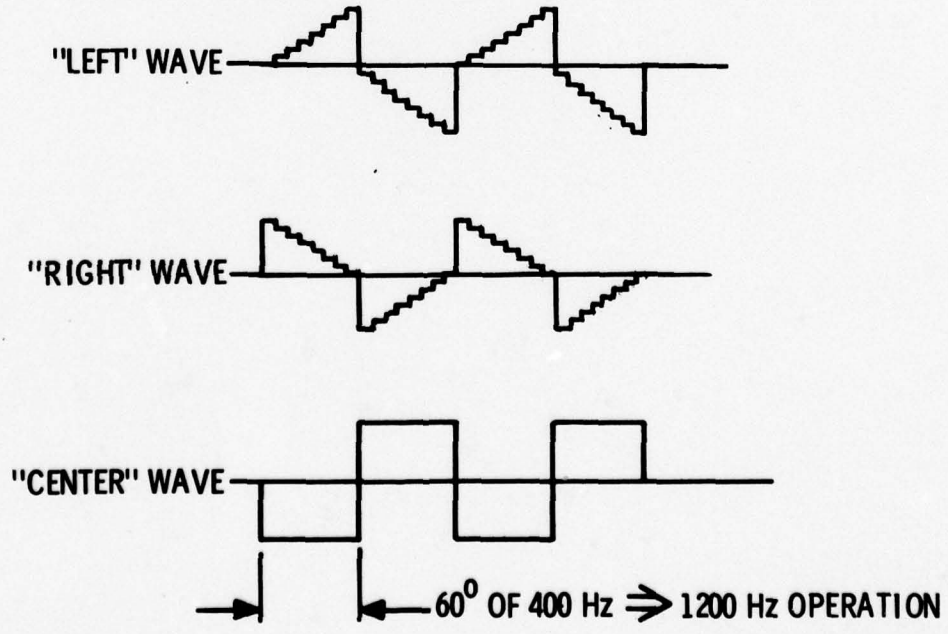


Figure 5 Waveforms for a 400 Hz System

The mathematical analysis also shows that if g(t) has the property that g(t) = -g(-t) (a sine wave has this property), then so will f(t). From this it follows that the Right portion when viewed from right to left, will be the same as the Left portion when viewed left to right. This result validates an assumption made in the optimization program that the line-to-neutral wave is the same in going from 0^{o} to 90^{o} as in going from 180^{o} back to 90^{o}.

System Organization

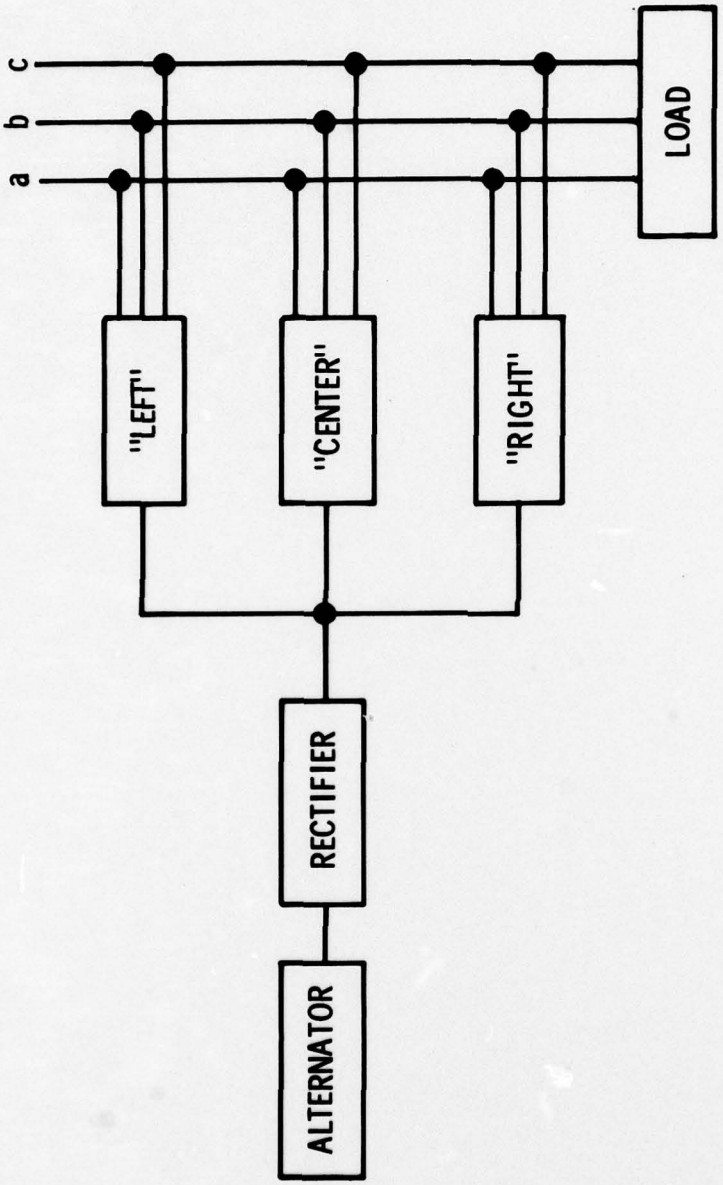
The Left, Center and Right concept coupled with the observations cited above leads to a logical system which utilizes separate modules to generate the "sub-waves" of Figure 5. The basic VSCF system structure is shown in Figure 6.

Each wave generator feeds its line-to-neutral voltage into each phase according to the timing indicated in Figure 4 (each generator feeds only one phase at a time). The phase selection is accomplished by means of switches at the output of each generator.

The Center module is simply a square wave generator operating at three times the desired power frequency. The generator feeds directly to the load via the phasing switches mentioned above.

The indicated Center module operation satisfies the fourth basic guideline of the program which was to maximize the power switched directly to the load. With the organization shown the Center module is the "power section" supplying over 60% of the power to the load.

The Left and Right modules comply with the fifth program guideline, using switches and transformer to reduce waveform harmonic content. Since the Left and Right waves are of the same polarity at any instant of time (Figure 5), a common transformer can be used for both modules. A simple method uses an autotransformer which is fed at the top by a square wave equal in amplitude but of opposite polarity to the Center wave (at three times the power frequency). Taps and switches are arranged along the transformer to provide voltage levels according to the optimization of Figure 2. The Left wave is generated by commutating the switches (SCR's) from bottom to the top (Figure 7) during the positive half cycle of the driving square wave and again from bottom to the top during the negative half cycle of the square wave.



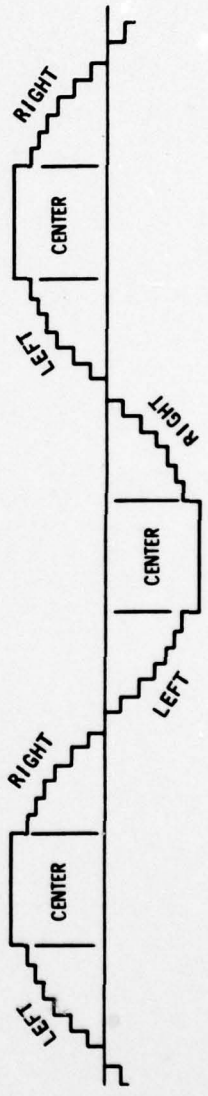


Figure 6 VSCF System Organization

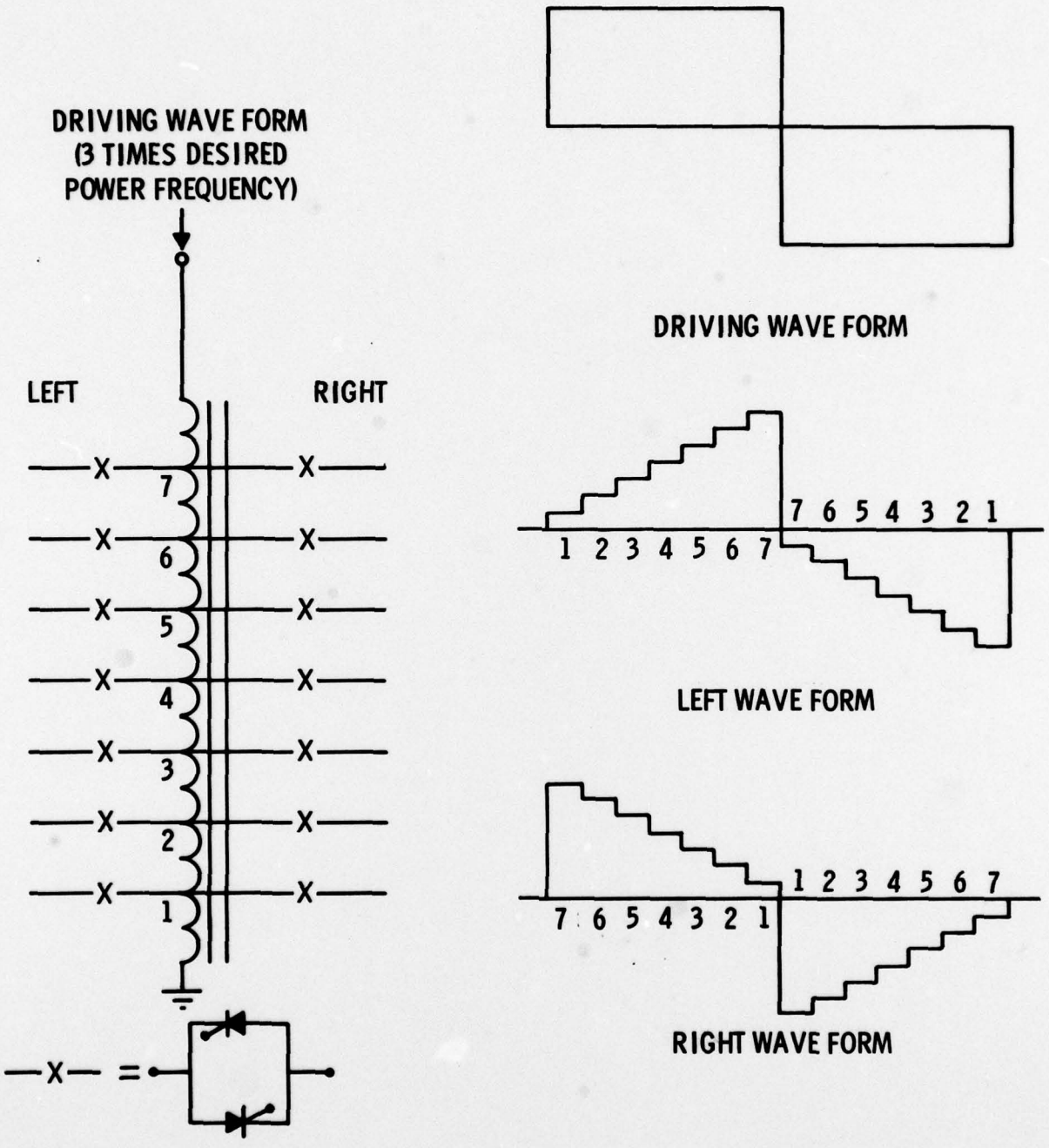


Figure 7 Left, Right Waveform Generation

The dwell time at each step is programmed according to the firing angles of Figure 2. The Right wave is generated in the same manner only the commutation of levels starts at the top and goes down to the bottom during each half cycle.

ADVANCED COMMUTATION TECHNIQUES

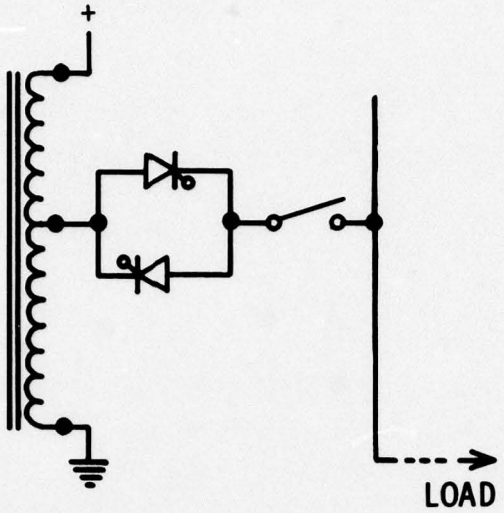
Having adopted the system organization described, the remaining major problem is that of commutating the switches. Usually this is accomplished by using energy storing elements such as inductors or capacitors. Such an approach, however, suffers an appreciable weight penalty. AC-DRL has devised a transistor commutating method to reduce the weight requirements.

SCR's can switch high currents at high voltages. The SCR is turned on by means of a gate signal, but can only be turned off by reverse current flow or starvation. Transistors can control relatively high currents but at low voltages, and can be turned on or off by means of the base drive signal. AC-DRL uses the power switching capabilities of SCR's and transistors to their best advantages in our new circuit concepts.

There are transistors available that will handle up to 250 amps, but at relatively low voltages (approximately 100 volts). The new commutation scheme utilizes transistors in parallel to yield the required system short circuit capability, and incorporates them in a scheme for commutating the SCR's, which takes advantage of the multiple voltage levels available in the system to keep the voltage across the transistors at a maximum of 40 volts.

The transistor is used as a "flying switch," that is, injected (or flown) to the appropriate level for turning off the conducting switch (SCR) shown in Figure 8.

Tradeoff studies have shown that this approach yields a lighter weight configuration than other commutation schemes. Therefore, the flying-switch method has been selected for use in AC-DRL breadboard VSCF systems.



"FLYING" SERIES-SWITCH

INJECT SWITCH IN PATH OF CONDUCTING SCR.

THIS PROVIDES COMMUTATION BY "STARVATION".

THIS METHOD USES TWO SWITCHES, WHICH ARE USED FOR ALTERNATE TAPS OF THE AUTO-TRANSFORMER.

Figure 8 "Flying" Switch

CONCEPT MECHANIZATION

The three key concept VSCF advances which were evolved during the program:

- Unique transformer utilization
- Optimized waveform construction
- Advanced commutation techniques

can be combined to provide a circuit configuration having the following characteristics:

1. Lighter in weight than any competing solid state system which has been disclosed.
2. Relatively simple in concept and straightforward in organization.
3. Capable of handling low power-factor loads.
4. Requires relatively few basic switches to produce a low harmonic-content waveform.
5. Will benefit from advances in power semiconductor packaging, and developments in large-scale integration.

6. Relatively easy to achieve redundancy for critical elements in the system.
7. Highly flexible in that similar mechanization schemes can be used in various applications over wide power ranges.

The particular mechanization which was decided upon for breadboard testing is shown in Figure 9. A 400 Hz power output to the load is assumed for the circuit shown.

The main power Center operates directly into the load, switching among the three phases at 1200 Hz. The Left and Right wave generators share a common autotransformer which is driven by an independent 1200 Hz square wave generator.

The transistor switches at A and B are the "flying" series-switches. To describe their action, assume that the level-5 SCR's and switch B are conducting. To change to level-4, simply remove the gates on the level-5 SCR's, open switch B, and simultaneously gate on the SCR's at level-4 and close switch A. Then, to change to level-3, remove the gates on the level-4 SCR's, open switch A, and simultaneously gate on the SCR's at level-3 and close switch B. Note at this last step that switch b

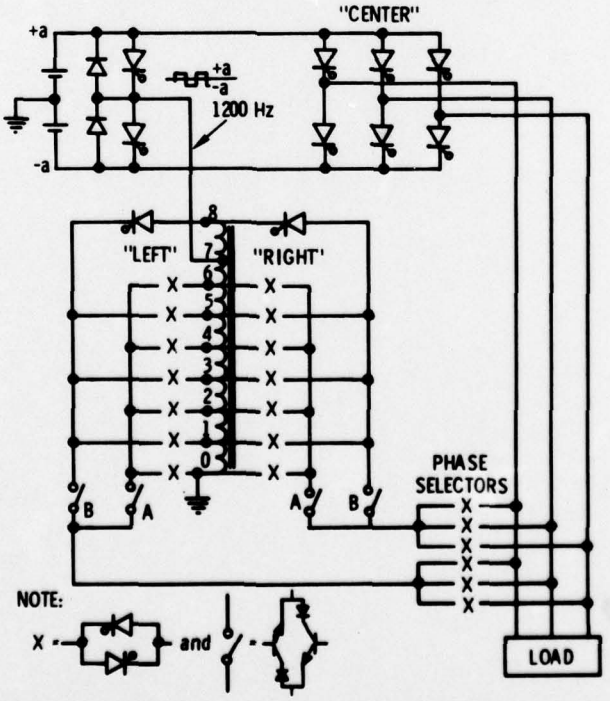


Figure 9 AC-DRL Breadboard VSCF Configuration

"moved down the ladder" to level-3. In this way switches A and B, respectively, control alternate SCR's in the ladder. The commutating switches, operating in series with the phase switches, provide the required increasing and decreasing step voltages to the load. Positive commutation of the power Center SCR's is also provided via transistor switch B and the step-up voltage action between autotransformer terminals 7 and 8.

Breadboard

To test the concepts presented above and to validate the VSCF system organization selected, a breadboard of the circuit shown in Figure 9 was constructed. Figures 10 and 11 show two views of the power system which contains all of the elements shown in the circuit diagram plus the SCR gate driving elements. The gate drives use photon coupled devices to isolate the logic from the power system. The logic network is not shown but is of standard design and configuration.

After construction and checkout of the various sub-circuits, the following functional tests were performed on the breadboard:

a) Generate three-phase line-to-neutral and line-to-line voltages in accordance with the selected computer designed waveshape for 28 step line-to-neutral voltages.
b) Supply three-phase power to lagging, leading, and unity power factor loads.
c) Supply three-phase unbalanced loads.
d) Supply power for line starting of three-phase induction motors.

The breadboard performed all the required functions, thus verifying the predictions made for the new AC-DRL concepts. During the preliminary tests the breadboard produced 5 kva into a resistance load, energized 0.5 power factor lagging and 0.2 leading power factor loads, supplied power to one-phase or two-phase loads to demonstrate the capability to energize unbalanced loads, and successfully line started 2.4 hp induction motors with ±50 volts dc input voltage.

Figure 12 shows the line-to-neutral and line-to-line voltage waveforms obtained from the system. The waveshapes are shown with no filtering and have a total harmonic content of approximately 6.5% and 3.3%, respectively.

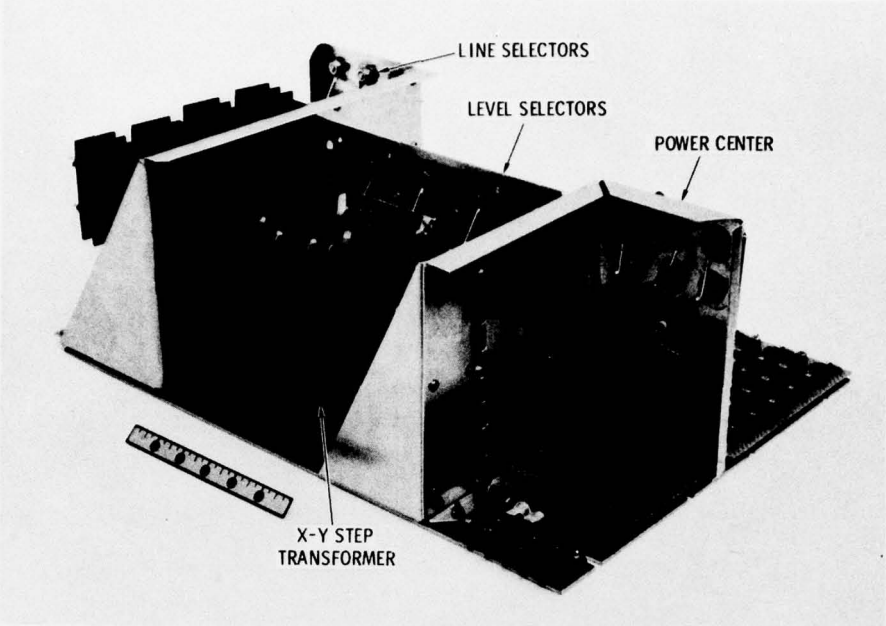


Figure 10 AC-DRL's Converter (Front View)

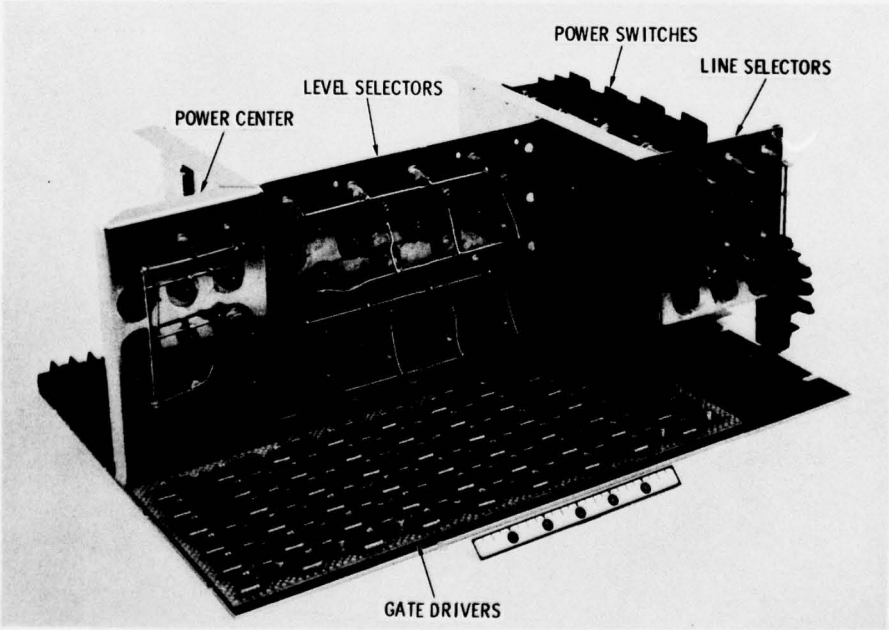


Figure 11 AC-DRL's Converter (Rear View)

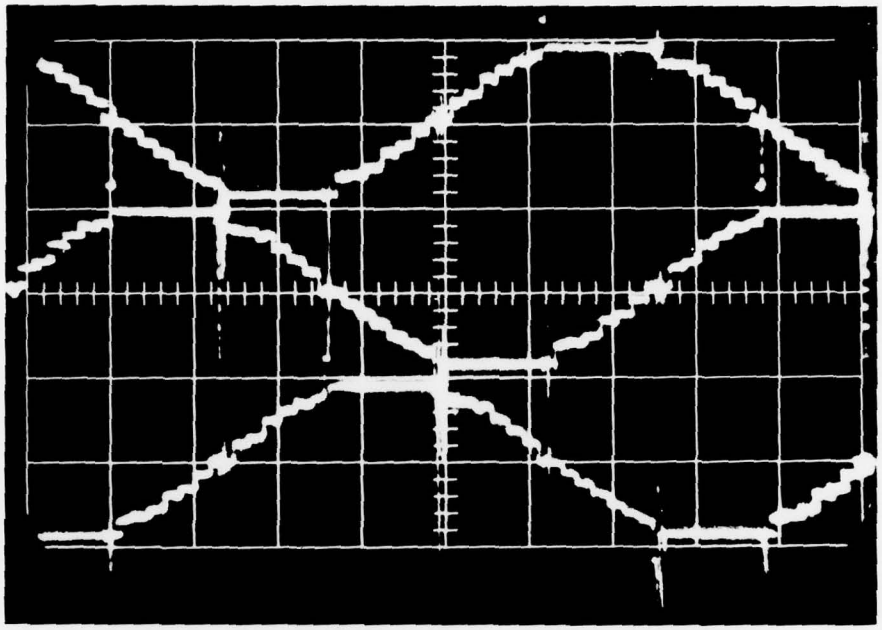


Figure 12a Line-to-Neutral Unfiltered Waveforms

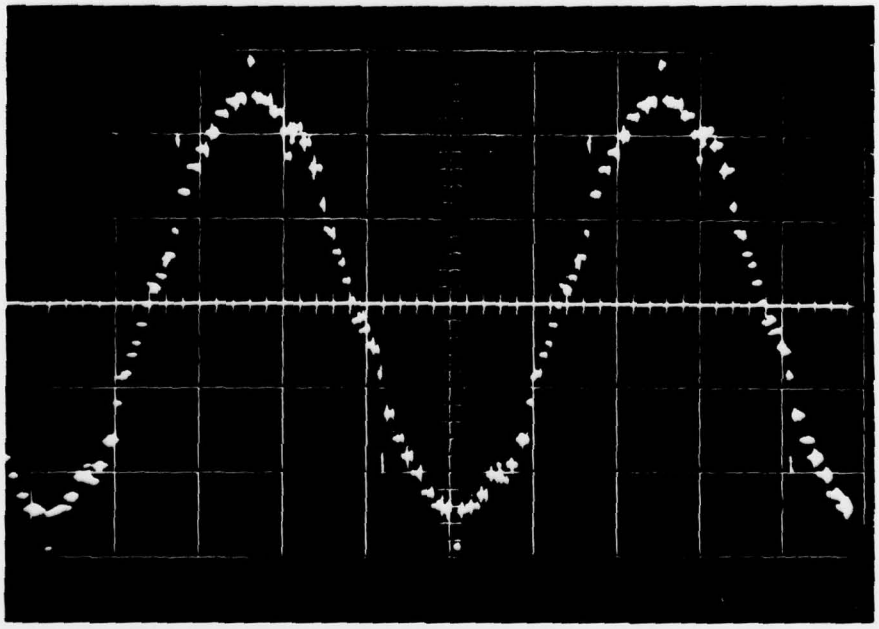


Figure 12b Line-to-Line Unfiltered Waveform

SUMMARY

The AC-DRL dc link VSCF conceptual development program, has, to date, resulted in the advances summarized below:

- Utilization of an autotransformer in step forming
- "Left-Center-Right" concept enables higher frequency (1200 Hz) operation of the autotransformer
- "Flying Switch" commutation eliminates capacitors.

The above innovations individually and collectively result in significant weight reductions of critical VSCF system components. The unique method of forming a sine-wave approximation minimizes output filter requirements. These indicated conceptual advances have been verified mathematically as well as experimentally and then functionally tested in a breadboard system. The testing has established that combined transformer weight savings of 90% over the full summing transformer approach are realizable through autotransformer operation at three times the basic VSCF power frequency. Further, the test results establish that, as a first approximation, harmonic content of the output waveform is not a function of transformer weight but the number of switches and transformer voltage taps used in the circuit. The utility of the transistor commutation approach has also been established.

The concepts that have been presented herein are the subject of a continuing in-house development program at AC-DRL. The breadboard system described is being upgraded to higher and higher power levels and being subjected to comprehensive testing to assure accurate knowledge of component stresses and substantiate performance under various transient and unbalanced load conditions.

Detailed circuit analysis and optimization studies are being pursued which have already revealed additional insights that may make it possible to reduce the number of power components as well as simplify the required system logic.

AC-DRL's in-house program is directed toward developing a family of power conditioners extending to the 100 kw range. In order to achieve this goal, considerable emphasis is being put on the system approach which necessarily requires detailed study of the various applications for such power conditioners. These system studies are being performed concurrently with the analytical and breadboard efforts such that a maximum of interchange between the technical groups involved is realized.

APPENDIX B

OPTIMIZATION TECHNIQUES

APPENDIX B

OPTIMIZATION TECHNIQUES

Delco Electronics has developed a multivariable direct optimization program for use on engineering design problems that are too complicated for solution by the indirect methods such as differential and variational calculus. The experience gained in developing and applying the optimization program will be directly applicable to the development of the optimization algorithm in the Phase II armor design and optimization package.

The optimization program uses the direct evaluation method to solve the general problem:

maximize the objective function $F = f(X_1, \ldots, X_n)$

subject to $a_i \leq X_i \leq b_i$

for $i = 1, \ldots, n$

A direct optimization method searches for the maximum of the objective function by a series of direct evaluations of the function, using the resulting data to pattern the search for improved values of the function. To use the optimization program, a mathematical model of the system being studied must be available in the form of a computer analysis program. The model must fit the general problem as stated – it must express a single value which is to be maximized as a function of some set of independent variables.

There is no absolute measure of the efficiency of a direct optimization method. Qualitatively, the efficiency of any method is increased if the number of direct evaluations required to find the maximum of the objective function can be decreased. Since many engineering programs take a significant amount of computer time for a single evaluation, using the analysis program as few times as possible can decrease the cost of performing a computer optimization study. The basic technique used is a "continous improvement" technique. In most cases, the continuous improvement technique will find a direction of increasing F (in the above equation) with fewer evaluations than are required by the gradient methods. The continuous improvement technique avoids the scaling problem inherent to the gradient methods, and is not sensitive to discontinuities in the objective function.

In the armor weight minimization problem there are two types of optimization which must be done – either separately or at the same time, depending upon whether or not a minimum level of protection is specified for all sections of the armored surface. The distribution of probabilities for protection of the various portions of the surface will involve an exploration algorithm of a type very similar to the one used in the developed program. Its function is described in the following paragraph.

The exploration routine uses a finite step exploration to determine if, and in what direction, the objective function increases. The procedure to be described is performed for each variable, in order, while all other variables are held at their basepoint value. The result of the exploration routine is a vector $\overline{V}$ which indicates for each variable the direction of increasing F. The procedure for each variable is as follows: An evaluation of F is performed at the point $(X_1, \ldots, X_i - \Delta_i, \ldots, X_n)$, where Δ_i is the step size assigned to the i^{th} variable. If F increases, the i^{th} element of $\overline{V}$ becomes -1. If there is no increase at the negative step point, then F is evaluated at the point $(X_1, \ldots X_i + \Delta_i, \ldots, X_n)$. If F increases here, the i^{th} element of $\overline{V}$ becomes +1. If F increases for either a negative or a positive step, the i^{th} basepoint value is changed to the value which produced the increase. If neither step produced an increase in F, the i^{th} element of $\overline{V}$ becomes zero, and the values of F at each step tried are stored for future use, if required. An example vector $\overline{V}$ for a five variable problem $\overline{V} = (+1, 0, -1, +1, 0)$, shows that the objective function increased for positive steps on the first and fourth variables, that F increased for a negative step on the third variable, and that no increase was found for the second and fifth variables. The completion of $\overline{V}$ ends the exploration routine.

When a direction of increasing objective function has been found, a search for the maximum along that vector is made by a special Fibonacci search technique. When the maximum is reached, another exploration is performed and the sequence is continued until no further improvement is found. For the armor optimization problem, the algorithm will be written for a minimization search. The optimization program will incorporate methods of assuring that the selected optimum is not on a resolution ridge (a location where the finite step exploration method is unable to detect an existing direction of objective function improvement). The application of gradient techniques has been shown to be an effective method of following a resolution ridge.

If a minimum level of protection is specified for the entire surface of the armored combat vehicle, then the optimization problem becomes much simpler, because the distribution of protection effectiveness need not be done. In this case, the optimization problems are all of the type specified to adjust the surface geometry for minimum weight, as described previously. This problem involves a search for a minimum weight where each independent variable (variables to describe the surface geometry) can vary only between certain selected limits (such as upper and lower limits for the angle of rotation of a plate about a specified axis). This problem is ideal for a Fibonacci search, or a lattice search if a step size has been defined for changes in the independent variables.

It is understood that this contract effort is the first attempt to develop an automated design approach to the problem of minimum weight armor design. To simplify the desired approach it is recommended that the practice of defining a minimum protection level for the entire armored surface be adopted. The optimization procedure to be developed would, in that case, be more efficient in terms of computer time than if the minimum protection were not defined. It is expected that the direct optimization approach will be more effective than methods that spend computer time in calculating approximation functions so that more exotic optimization procedures can be applied. The experience which Delco Electronics has gained in the direct optimization method will be useful in coordinating the analysis and optimization portions of the design optimization package, and will lessen the time required to develop the specific optimization routine to be written specially for this problem.

The following examples illustrate engineering design problems to which the optimization program has already been successfully applied:

1. Optimize the armor penetrating capabilities of the AP round of a VRFWS application. The independent design variables were: weapon caliber, projectile length-to-diameter ratio, penetrator length-to-diameter ratio, projectile subcaliber ratio, and propellant web thickness.
2. Minimize the weight of an air-to-air gun system (including ammunition weight) to give the required flight and effectiveness characteristics. The independent design variables were: weapon caliber, projectile length-to-diameter ratio, barrel length, and propellant web thickness.

3. Optimize the performance of a roller-type feed and chamber system for a six-barrel, rotating machine gun. Ten independent design variables were used to define the mechanism.

4. Minimize the harmonic content of the stepped waveform in a solid-state aircraft auxiliary power system. The independent design variables were number of steps, step voltage, and step duration.