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Final Technical Report
March 1979

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LSI/MICROPROCESSOR RELIABILITY PREDICTION MODEL DEVELOPMENT

IITRI/Reliability Analysis Center

H.C. Rickers

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This report presents updated reliability prediction models for LSI, microprocessor and memory devices for inclusion in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment."

The models proposed in this study possess all those qualities common to practical reliability assessment techniques. The expressions are relatively simple and allow for consideration of evolving fabrication techniques, or emerging technologies, through the modification of temperature dependency and

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associated temperature factors. The factors exhibit the appropriate discriminations against the device design and usage attributes which contribute to known failure mechanisms. Additionally, each of the models demonstrate reasonable accuracy over the total range of parameters considered in these techniques.

PREFACE

This final report was prepared by IIT Research Institute, Chicago, Il. for the Rome Air Development Center, Griffiss AFB, New York, under Contract F30602-77-C-0223. The RADC technical monitor for this program was Mr. Peter F. Mannc (RBRM). This report covers the work performed from October 1977 to November 1978.

The principal investigator for this project was Mr. H. C. Rickers with valuable assistance provided by Mr. T. E. Turner, Mr. D. B. Nicholls, Mr. S. J. Flint, Mrs. C. A. Proctor, Mr. S. Kus and Dr. F. C. Bock. Data collection efforts for this program were coordinated by Mr. M. R. Klein, assisted by Mr. I. L. Krulac.

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EVALUATION

The objective of this effort was to evaluate and update the monolithic failure rate prediction models in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment." Major emphasis was placed on microprocessors and complex memory devices.

As a result of this program, models were developed which retained the same general form and theory of the existing models. The base failure rate still consists of a temperature dependent device failure rate contribution and a mechanical device failure rate contribution. The modifying factors, such as for temperature and environment, only apply to their appropriate portion. The following are some of the major changes or additions:

a. A voltage derating stress factor has been added.

b. The contribution to the failure rate for package related defects is now based on package type as well as the number of pins. The package complexity failure rate (C_3) is added to the mechanical device failure rate contribution (C_2). Flat pack factors may be applied to carrier packages for which unique C_3 values have not yet been determined.

c. The temperature acceleration factor is a function of the impact of temperature on the failure rate for particular technology and values are presented for 11 technologies over a range of temperatures.

d. A ROM and PROM programming technique factor has been added to account for small differences observed in the available data depending on how the devices were programmed.

e. A method for estimating junction temperatures has been included. Typical temperatures for the various environments along with some typical values of junction-to-case thermal resistances are provided. Again, flat pack factors may be used for carrier packages.

The learning factor which is present in the existing MIL-HDBK-217C model, is not treated in this report since the data analyzed was predominantly on mature devices and did not permit quantitative evaluation. This factor will have to be assessed prior to inclusion of the new model in MIL-HDBK-217C.

The quality factor for plastic encapsulated devices is now 35 which, at first glance, appears to be considerably more tolerant than in the existing models. However, the effect of plastic encapsulation is now also reflected in the base failure rate by the temperature acceleration factor and the junction-to-case thermal resistance. The data in this study was limited in both the scope of applications reflected and the operating duration, although a large number of device hours of data was available. The majority of the plastic data came from either limited-duration, ground benign applications with carefully controlled environments or from accelerated tests at higher temperatures where the effects of moisture were masked or reduced. Therefore, it was impossible to assess failure rate versus time for moisture related

Section 1

INTRODUCTION

1.1 Purpose

The purpose of this study was to develop the failure rate prediction methodology which can be employed in the reliability assessment of complex and new technology microcircuits with the major emphasis placed upon memories, microprocessors and their support devices. The study involved an evaluation of the current failure rate prediction models as presented in MIL-HDBK-217B, the identification of those factors most closely correlated with complex microcircuit reliability, and the development of new prediction models which afford reasonably accurate estimates of device reliability.

1.2 Background

The failure rate and mean time between failure (MTBF) prediction capabilities are essential in the development and maintenance of reliable electronic equipments. Predictions performed during the design phase yield early estimates of the anticipated equipment reliability which provide a quantitative basis for performing design trade-off analyses, reliability growth monitoring, and life cycle cost studies. Current microcircuit reliability prediction techniques, such as those presented in MIL-HDBK-217B, afford reasonably accurate predictions for a variety of device technologies over the low-and-medium-complexity range. However, the rapid evolution of microcircuit technologies has introduced complex device configurations which are beyond the intended scope of present methods. The extensive use of these complex and new technology devices in both military and commercial electronic systems, combined with the importance of an early estimate of expected reliability, has created an urgent need for a relatively simple but accurate method of predicting their reliability.

Several prediction models addressing complex devices have been proposed in the past several years. Most of these methods are based on transfer techniques which attempt to extend the model variables and factors for simple devices to complex device models. Other models have been based on the physical attributes and characteristics of the circuit elements and require detailed knowledge of the device design parameters. However, none of these proposed models addresses the entire spectrum of technologies or device configurations, or adequately reflects the introduction of new processes, device configurations or technology evolution.

The complex microcircuit failure rate prediction methodology should afford the optimal consideration of those qualities common to practical reliability assessment techniques including:

- a relatively uncomplicated approach which is easy to use and does not require intimate knowledge of device characteristics beyond readily available information;

- the appropriate discrimination against device design and usage attributes which contribute to known failure mechanisms;

- a dynamic, flexible expression, which, through simple modification, allows for the evaluation of newly emerging technology devices;

- reasonable accuracy over the total range of all parameters considered in the technique.

This report describes the approach, results and conclusions of the study and includes the proposed complex microcircuit reliability prediction models to update Sections 2.1.3 and 2.1.4 of MIL-HDBK-217B.

Section 2

DATA COLLECTION

The validity of failure rate prediction models can only be assessed through a comparison of predictions and actual reliability experiences. Likewise, the modification of current prediction models or the development of new prediction techniques should be based upon reliability data. These types of modeling activities require extensive reliability data resources since models derived from limited data will reflect the characteristics of only that information.

Since the IIT Research Institute/Reliability Analysis Center (RAC) regularly pursues the collection of microcircuit device reliability data as part of its normal data solicitation activities, substantial data resources had already been accumulated for LSI devices prior to the beginning of this study. The requirement for vast quantities of reliability data for model development necessitated the initiation of a data collection effort to supplement the existing information. This data collection effort included a literature search for published information in journals, technical reports, handbooks, etc., and a survey of commercial, industrial and government organizations for complex microcircuit reliability data.

2.1 Literature Review

A comprehensive literature review was performed to identify all published information which is relevant to the reliability of complex microcircuits. Literature sources searched in addition to the RAC automated library information retrieval system include the National Technical Information Service (NTIS), the Defense Documentation Center (DDC), and the Government Industry Data Exchange Program (GIDEP).

The emphasis in the literature review was directed toward the identification of references dealing specifically with complex microcircuit reliability characteristics and prediction. Reliability prediction references were examined to determine the deficiencies of current prediction methods and to evaluate the merit of proposed prediction model revisions. Other reports were extremely useful in providing supplemental information, particularly in the areas of component construction, testing, and failure mode and mechanisms.

2.2 Data Survey

An extensive reliability data collection effort was required to provide the additional data resources for the model development activities. Numerous potential data sources were identified by the results of a RAC Microprocessor Reliability Survey which was conducted in the winter of 1977. The survey presented a series of questions designed to determine the extent to which microprocessors and complex microcircuits were being employed in new equipment designs and the experiences which had been accumulated with these devices. The survey forms were sent to over 3,000 commercial, industrial and government

organizations. Over 225 of the survey respondents indicated that they were utilizing complex microcircuits in equipment designs. Each of these organizations was contacted to acquire its complex microcircuit reliability experiences. Discussions with individuals within these organizations resulted in references to other potential data sources. A letter was also circulated by Mr. D.F. Barber, Chief, Reliability Branch, Reliability and Compatibility Division, Rome Air Development Center, to a group of large-volume complex microcircuit users, indicating the importance of this program and requesting their participation. Additional requests were forwarded to all complex microcircuit manufacturers to obtain device construction and test information. In total, slightly over 300 organizations were contacted in the data collection effort.

Approximately 20% of the organizations contacted during the data collection effort submitted information to RAC. A primary concern of the majority of contributors was the proprietary nature of the information and the desire to remain anonymous. For this reason, none of the data contributors in this study will be identified.

The types of information collected include life test, accelerated life test, screening, burn-in, reliability demonstration, field experience, device characterization and device malfunction data. These data encompass all LSI microcircuits including RAMs, ROMs, PROMs, EPROMs, shift registers, random logic LSI, microprocessors and their peripherals.

The collected data and related documentation were reviewed for completeness and detail. Only the data presenting adequate descriptions of the major concerns including device constructional features, screening procedure employed, application stresses and test or operating conditions were considered in this study.

While the scope of this study was limited to the development of prediction models for LSI Digital and Memory devices, to avoid any discrepancies which might possibly have resulted from the differences in prediction model formats of the existing SSI/MSI Digital, Linear device equations and the newly proposed equations, RAC extended the proposed model formats to consider all microcircuit devices. The appropriate model parameters for SSI/MSI Digital and Linear devices were developed utilizing the existing data resources in the RAC automated data file system. The proposed models for these device families and evaluations of these proposed models are presented in Appendix 2.

A summary of the operational part hours employed in this study is presented by device type, technology, package type and data source in Table 1.

TABLE 1: SUMMARY OF OPERATIONAL DATA BY DEVICE TYPE
(In Millions of Device Hours)

Device Type	Technology	VENDOR		USER	
		Plastic	Hermetic	Plastic	Hermetic
RAM and Shift Register	Bipolar	13	51	97	1678
	MOS	17	66	238	3287
ROM and PROM	Bipolar	8	39	889	205
	MOS	2	21	241	44
Digital MSI/LSI (≤ 50 Gates)	Bipolar	1	3	324	82
	MOS	2	7	663	1163
Digital MSI (12-50 Gates)	Bipolar	--	--	3813	316
	MOS	--	--	277	13
Digital SSI (1-12 Gates)	Bipolar	--	--	6464	654
	MOS	--	--	321	22
Linear		22	71	972	10277

Section 3

DATA ANALYSIS AND STATISTICAL MODELING TECHNIQUES

The development of a viable prediction methodology for complex microcircuits involves identifying and quantifying all significant reliability parameters and factors from an in-depth evaluation and analysis of accumulated reliability experience data and information. This section outlines the approaches, conventions, and assumptions utilized in the data analysis and the techniques employed in the prediction model development.

3.1 Data Analysis

All data items received during the data collection efforts were reviewed for completeness of detail and examined for any inherent biases. Any data submittal which displayed obvious biases was not considered in this study. Those reports lacking sufficient detail were not considered until the necessary additional information was acquired.

A prerequisite to the data summarization was the identification of all of the parameters and factors which would influence component reliability. The RAC automated reliability data system is presently organized according to a set of detailed descriptors which characterize both device attributes and test or operating conditions. These descriptors formed the basis for potential data summarization parameters. Additional factors were identified to complement the existing set through a review of periodic literature dealing with complex microcircuit reliability and alternative reliability prediction techniques. The descriptor complement which was selected allowed for the maximum number of variables to be quantified so that the analysis procedures can identify those which are truly significant.

Each of the data submittals was summarized by recording the appropriate value of each of the descriptor parameters. These summarized data records were then entered into a computer file for subsequent analysis.

Failure Rate Calculation. The dependent variable in each of the data records is the device failure rate which is the parameter calculated in reliability predictions. Failure rates are typically expressed as the number of failures per unit time (usually per 10^6 hours) or as percentage failures per unit time (usually 10^3 hours). The failure rate, expressed in failures/10^6 hours, is calculated by dividing the total number of failures by the total millions of device hours. This single factor, referred to as the point estimate failure rate, does not completely characterize the reliability of a given device population.

In this study, point estimate and the 60% Chi-square confidence interval failure rates were calculated for each of the data records. The Chi-square statistic is used to identify a confidence interval around the point estimate failure rate. The 60% confidence interval is comprised of the lower-20% confidence and upper-80% confidence level points. A 60% confidence interval is that range of values around the estimate that would, with a 60% probability,

include the actual mean of an infinite sample of the device tested. These failure values are calculated as follows:

$$\text{Lower-20\% confidence point} = \frac{X^2\ (\alpha - 1,\ 2r)}{2T}$$

$$\text{Point estimate} = \frac{r}{T}$$

$$\text{Upper-80\% confidence point} = \frac{X^2\ (\alpha,\ 2r + 2)}{2T}$$

where:

r is the number of degrees of freedom equal to the number of failures

T is the total number of device hours (in millions of hours)

$X^2(\alpha)$ is the Chi-square value for the particular confidence level based on the number of degrees of freedom (determined from Chi-square Tables).

The use of the 60% confidence interval and point estimate failure rates provides a convenient method for weighting the various data records during model development analysis. The significance of the data record increases as the confidence interval points approach the point estimate value. In the model development analysis these points would appear as three records with identical parameter values exhibiting similar failure rates, as opposed to three records with identical parameter values exhibiting divergent failure rates. Only the upper-80% confidence level failure rate was calculated for those data records with zero failures.

3.2 Statistical Modeling Techniques

In order to identify and evaluate the relationships between the various reliability considerations which are defined by the data, various statistical analysis techniques were employed. The techniques which were applicable to the derivation of the reliability prediction model are briefly reviewed in the following paragraphs.

Stepwise Multiple Linear Regression Analysis. The stepwise multiple linear regression analysis routine assumes a preliminary model of the form:

$$Y' = b_o + b_1X_1 + b_2X_2 + \ldots b_iX_i$$

where Y' is the resultant dependent variable; X_1, $X_2 \ldots X_i$ are the independent variables which are thought to influence the value of Y'; and b_1, $b_2 \ldots b_i$ are the coefficients which will be found by the regression.

To perform a regression, a number of data points, each consisting of a known Y and its corresponding X variables, are required. A proper regression also requires that the X variables be nearly independent and that there are many more data points than X variables.

The regression technique first computes a correlation matrix comparing all the X variables to one another as well as to the observed Y. This matrix serves to identify any nonindependent X variables (except those which are a function of two or more other X variables) and also computes the relative correlation of the Y variable to each of the X variables.

The analysis orders the X variables according to their relative correlation with the Y variable. Considering the first X variable and the Y variable, b_o and b_1 are computed such that the sum of the squares of $(Y-Y')$ will be a minimum. The second X variable is then considered in the computation of b_o, b_1 and b_2 such that the sum of the squares of $(Y-Y')$ will again be minimum.

If the improvement in the estimate afforded by the inclusion of this second variable is significant with respect to a given confidence level, the variable is accepted as part of the model and the regression continues by considering a third variable.

If considering the second variable does not result in a significant improvement, the model remains:

$$Y = b_o + b_1 X_1$$

Whenever a new variable is included in the fitted model, all previously included variables are retested for significance, given that the new variable is in the model.

The regression continues until all of the significant X variables have been identified and their corresponding b coefficients have been calculated.

Several measures of the "goodness of fit" of the model to the observed data are generally available for a regression model[1]. A review of the more important of these measures is presented below.

<u>R^2 - Multiple Correlation Coefficient</u>. This is probably the single most useful "goodness of fit" measure. The R^2 value is the ratio of the sum of the squares of the variance explained by the regression to the sum of the squares of the variance in the observed data. An R^2 value of 100% is the ideal result.

---

[1] N. Draper and H. Smith, Applied Regression Analysis (John Wiley & Sons, Inc., 1966.)

Critical F. The critical F is the value from the F table corresponding to the degrees of freedom of the model and the difference between the number of data points and the number of b coefficients. This number may be used to test the significance of each variable as it is considered for addition to or deletion from the model. The calculated F value for a regression is the quotient of the mean square due to residual variation. If the calculated F value is greater than the critical F value at the given significance level, it can be said that the last variable does not equal zero with a confidence of $1 - \alpha$, where α is the level of significance.

Estimated Standard Error of b_i. The estimated standard error of each b_i is the square root of the estimate variance. This value may be used to establish confidence intervals around the respective b_i's.

Standard Error of Estimate(S) The standard error of estimate is the square root of the residual mean square (the estimate of the variance about the regression). A small S value indicates a good fit, providing there are few repeats and many degrees of freedom for the error remaining.

Residuals. A residual is the difference between the observed and calculated Y values for each data point (Y_i-Y_i'). The residual may be plotted vs. one of the variables in order to evaluate patterns or trends. This may lead to the identification of new variables or transformations of current variables.

Fisher "F" Test. The complexities associated with the characteristics of microcircuits make it impractical to consider every possible variable when attempting to model the reliability of a device. As a result, the variables to be included are constrained to those which will have the most significant impact upon the reliability. The F-test technique can be employed to determine if any significant variables have been neglected. This may be accomplished by segregating the data resources into groups with the same set of significant variables. Applying the F-test to each of these groups will determine if there is sufficient statistical evidence to conclude that a data point, or a set of data points, come from a population with a mean which is not the same as the rest of the data. While a few outliers may be expected, an additional variable should be sought if a large percentage of any group is found to be divergent.

Curve Fit Analysis Technique. A series of curve fit programs are available for establishing the mathematical relationship between dependent and independent variable pairs in a given data set. These techniques provide a least squares curve fit of the data points to various types of expressions, including linear, exponential, power, and hyperbolic functions. The output of these programs express the dependent variable (Y) in terms of the independent variable (X) and two coefficients (A,B). In addition to the values of the coefficients A and B, the output provides an index of determination for each function which represents the "goodness-of-fit" of the expression to the data points.

3.3 General Modeling Procedure

The approach utilized in the development of the model format combined the relationships, as suggested by the data analyses and the literature, with the

statistical analysis techniques and data resources. The basic methodology employed in the model development is illustrated in a simplified form in Figure 1. The techniques represented in Figure 1 can be briefly explained as follows:

Identify Possible Variables. As previously indicated, the variables considered in the analysis were identified during the data collection activities based upon the parameters suggested by the RAC data system and the literature.

Data Quality Control and Confidence Evaluation. The data quality control was established in the data collection activities. Only unbiased data which identified all variables of concern in this study program were considered. The confidence for each data point was evaluated using Chi-square techniques. These confidence intervals were employed as figure of merit when evaluating each data point's impact during the subsequent statistical analyses.

Correlation Analysis. To perform a proper regression analysis, all of the selected variables must have a low interdependence. The regression program employed in this study offered a correlation coefficient matrix as a preliminary option in the regression. This matrix indicated the degree to which each variable was related to the others. Those variable pairs which exhibited high correlation coefficients were reviewed to either combine the variables or eliminate one of the variables from the regression. The coefficients of each variable with the failure rate variable suggested which parameters had the greatest impact upon reliability.

Stepwise Multiple Regression Analysis. This technique has been described in Section 3.2. The objective is to compute the coefficients of the assumed form of the model in a least squares fit to the data employing only those variables which are significant to a given confidence level. The limitation of the technique is the presumption of the model form. The regression does not suggest the optimal form of the model but rather computes the coefficients for the standard additive form. Multiplicative or other model forms can only be achieved by transforming variables in the regression.

"Good Fit" Tests. The "goodness-of-fit" techniques including residual analysis, standard error, R^2 and F-test were employed to determine if the models were realistic with respect to the data. These tests identified the need for additional variables and suggested which of the variables should be transformed to result in better model fit to the data.

Model Validation. The validation process consisted of tests at extreme and nominal parameter values. Predictions were made using the models for values of the parameters which are beyond the ranges found in the data. While there were not any data for comparison with the predictions, they were used to reveal any combination of values for which the prediction "blew up" or predicted a failure rate which was theoretically inconsistent or intuitively wrong. Predictions were also made for a set of data, not employed in the model development, to determine if the models accurately reflected the reliability of data other than that used to develop model parameters.

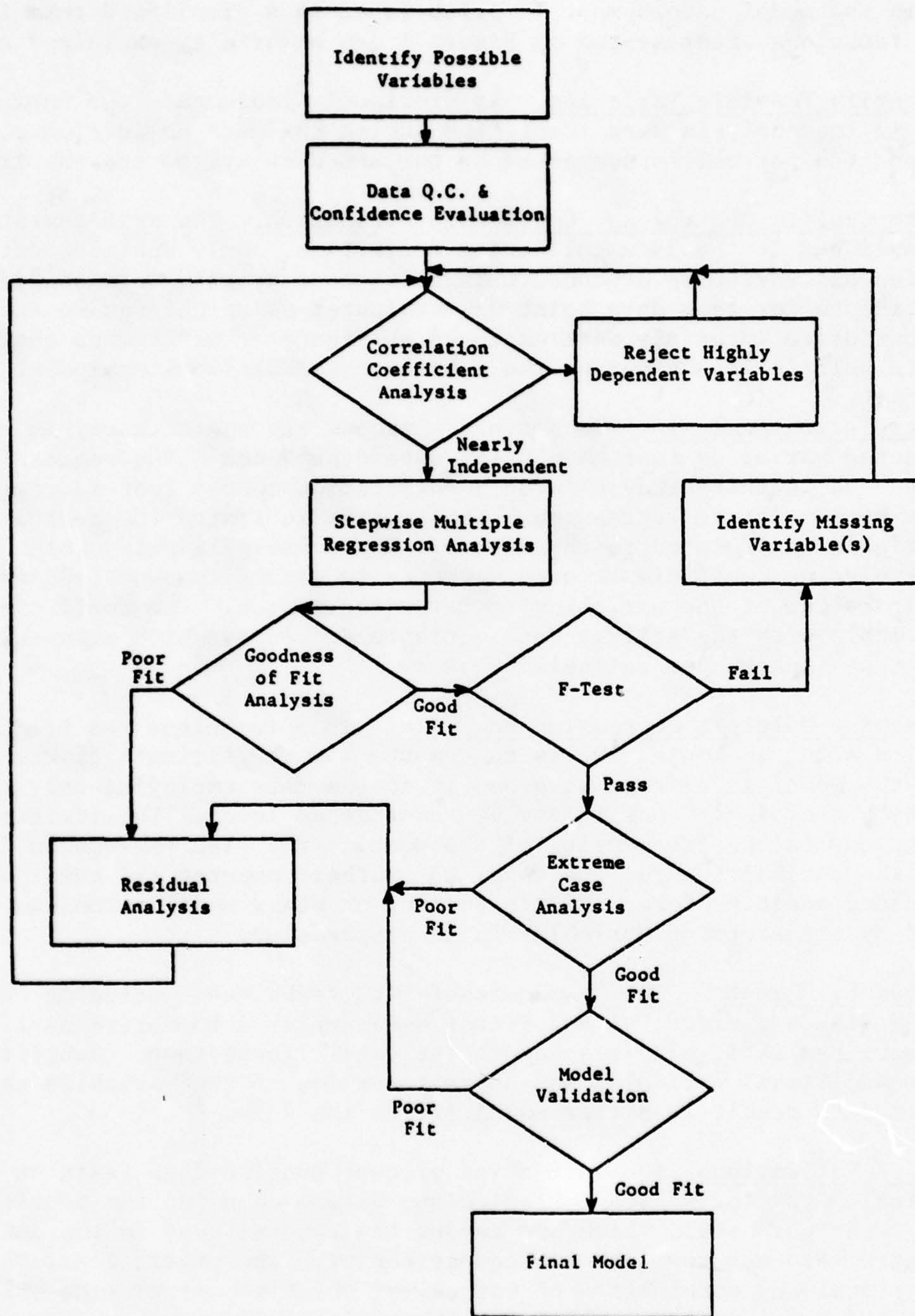


Figure 1: Prediction Model Approach Methodology.

Section 4

PREDICTION MODEL DEVELOPMENT

In formulating the proposed technical approach, it was essential to identify those critical factors associated with complex microcircuits which would ultimately impact the reliability of these devices. The variables which were given consideration include:

Device Technology
- Fabrication Techniques
- Fabrication Process Maturity
- Failure Mode Experience

Device Complexity
- Elements Employed in the Implementation of LSI Circuit Functions
- Electrical Functions Performed by Various Elements

Package Configuration and Complexity

Effectiveness of Screening Techniques

Operating Temperature and Environment

Software/Firmware Attributes

Application Considerations and Requirements

The development of a prediction model(s) requires the evaluation of the contributions resulting from each of these factors and the integration of their collective effects into a manageable expression that can be applied by reliability engineers without intimate knowledge of material properties, device physics or process techniques. Several possible modeling approaches were reviewed and considered, each of which had definite merit but were also subject to limiting constraints. The approach pursued in this study endeavored to utilize the available reliability experiences, established reliability conventions, and the information presented in the literature censoring conflicting or discrepant information. This section outlines the analysis performed in the determination of the various prediction model factors.

4.1 General Modeling Concepts

Historically, reliability prediction models have varied in complexity from a single point estimate failure rate value for an entire component family to elaborate expressions reflecting the contributions of the various physical and operational attributes of each component.

One of the earliest prediction techniques for microelectronic devices, presented in MIL-HDBK-217A, prescribed a single average failure rate value for the generic category of all monolithic integrated circuits. This single

failure rate value approach, while extremely simple, did not offer any sensitivity to the factors which influence component reliability. However, it should be realized that this model represented the results of the first serious effort to characterize the reliability of an emerging technology at a time when actual reliability experiences were extremely limited.

The microcircuit reliability prediction model evolved into a more elaborate expression in the RADC Reliability Notebook, Volume II, which was published in 1967. The failure rate model presented in this notebook consisted of a temperature-dependent base failure rate and a series of multiplicative modifying factors. These factors reflected the effects of component complexity, package configuration, application environment and component quality. The modifying factors which were included in this model, as well as the values which these factors assumed, were determined empirically from an analysis of the existing reliability information.

The base failure rate in this model was derived from an extension of the Arrhenius Model which had been used in conjunction with discrete semiconductor component reliability models. This base failure rate was intended to represent the most optimistic failure rate that the highest quality grade microcircuits might achieve under zero stress conditions. This base failure rate was then multiplied by the various adjustment factors related to part type, complexity, manufacturing method, quality grade, application stress and environment to arrive at a failure rate which was representative of a specific service.

The values which the adjustment factors assumed for various cases were derived from the analysis of reliability experiences. Since analyses of malfunctions experienced in microcircuit devices revealed that the majority of failures at that time were related to oxide step or contact cut problems, the complexity factor in this model was based upon the number of oxide steps and contact cuts in the device.

Reliability experiences also indicated a relationship between the amount of control and reliability emphasis applied during device production and the ultimate component reliability. This relationship is reflected in the quality factor which modifies the base failure rate according to the level of reliability screening. In a similar fashion, the relationships and dependence upon package configuration and operating environment are reflected in the appropriate adjustment factors.

The application of this modeling technique was limited to double or triple diffused silicon planar devices. It is based upon the assumptions that: (1) all infant mortality defects have been eliminated; (2) only conventional manufacturing processes and techniques have been employed; and (3) devices are operated within the prescribed operating limits.

This modeling approach, while more sensitive to critical reliability factors than previous techniques and certainly appropriate at the time, was still limited in terms of valid applications. The data employed in the derivation of the model parameters was extremely limited and reflected the problems associated with immature vintages of select technologies. The predictions

generated using this model were only considered valid for small-scale complexity with an end-of-life requirement not exceeding 20,000 hours. The ultimate limitation of this technique was that it did not incorporate any capability to extend the parameters to include devices of increased complexity or devices manufactured using new technologies.

A revision of MIL-HDBK-217A was developed to provide more accurate reliability prediction models for parts included in the "A" version and to extend the coverage to newer parts. This revision was first presented as a proposed MIL-HDBK-217B dated July 1973. The prediction technique presented in this revision employed an "additive model concept" consisting of two failure rate components; one due to time degradation causes which are accelerated by temperature and electrical bias, and a second due to mechanical and environmental causes.

The format of this proposed model reflected the reliability experiences which had been observed since the previous modeling attempts. This model attempted to demonstrate the influence of the various physical constituents of the devices which were identified as being critical to component reliability.

The total failure rate in this technique is actually comprised of the failure rate contributions of each of the device constituents. The failure rate contributions were determined according to the physical characteristics of the constituents such as: metallization area, diffusion area, chip area, crossover area, gate oxide area, number of interconnects, interconnect material, bond type, number of bonds, etc. Actual values for the model parameters for these various factors were determined using physics-of-failure techniques scaled by field data.

The failure rate contribution factors for the device constitutents are modified by the appropriate quality, temperature and environmental factors to determine the temperature and mechanical failure rates and ultimately the total device failure rate.

This proposed technique differed from all previous methods in that it presented individual models for various categories of device technology (Bipolar, MOS), device complexity (SSI/MSI, LSI), and a device function (Linear, Digital). This format allowed for the consideration of the parameters which were critical in each of these categories.

Unfortunately this elaborate technique suffered from two major deficiencies: first, using the model required extensive familiarity with the fabrication of the device, such as device materials and geometries, which is often difficult to ascertain, and, second, it is assumed that the temperature dependency exhibited in all categories (for all failure mechanisms) were identical. The assumption of identical temperature dependency implies that the failure mode distributions exhibited in each technology are similar. Analysis of the failure mode distributions for the various technologies indicates that the validity of this assumption is somewhat questionable.

Alternate approaches designed to simplify application and remedy the shortcomings of the proposed 217B technique without compromising the accuracy

of the predictions were considered in the development of the accepted version of MIL-HDBK-217B dated September 1974, which remains as the government authorized methodology covering this class of devices.

The accepted 217B technique presents a series of models for Bipolar and MOS microcircuit devices for four major classes: Digital (SSI/MSI), Linear, Digital (LSI), and Memories. Each of these classifications adopted the "additive model concept" as suggested in the 1973 proposed version. However, the number of modifying factors was significantly reduced.

All of the factors included in the proposed 217B version which were derived from the physical characteristics of the devices have been combined into a pair of complexity factors for the 217B handbook. The values for the small- and medium-scale complexity factors were determined from the mathematical relationships established from the analysis of empirical data. The large-scale complexity factors were established from the extrapolation of small- and medium-scale device relationships.

Two sets of temperature acceleration factors are included in the 217B prediction technique to reflect the variations in experienced failure mode distributions and associated temperature dependencies for the different technologies. The accepted 217B prediction technique also includes a learning factor which is intended to account for the impact of an immature technology and design, or process changes upon the ultimate component reliability.

The MIL-HDBK-217B prediction model affords reasonably accurate reliability predictions for a variety of device technologies, over a substantial complexity range, requiring only minimal familiarity with component attributes. However, the rapid evolution of microcircuit technologies has introduced a breed of devices which are beyond the intended scope of the 217B prediction model. Unfortunately, a simple extension of previous reliability knowledge and methods is not always practical for these devices, nor does it always yield predictions which are representative of actual device reliability.

The modeling approach pursued in this study combined the statistical analysis of reliability data with the relationships suggested in the literature and previous reliability modeling techniques, while attempting to afford the optimal consideration of those qualities common to practical reliability assessment techniques including:

- reasonable accuracy
- uncomplicated approach
- dynamic, flexible expression
- appropriate discrimination against unreliable conditions.

Since complex microcircuits, especially microprocessors and their support chips, are frequently configured essentially as a computer system, it is necessary to incorporate the reliability characteristics which result from the system-related considerations into the overall reliability assessment of the devices.

An appreciation for the critical parameters involved in the reliability assessment of complex microprocessor type systems can be derived from the consideration of the types of failures which would be exhibited by such a configuration. These failures can be grossly categorized as being attributable to hardware/device, software/firmware or application considerations. Similarly, the failure rate of a complex microcircuit can be expressed as a function of the failure rates for these individual system parameters:

$$\lambda_P = F(\lambda_S, \lambda_D, \lambda_A)$$

where:

λ_P is the complex device failure rate

λ_S is the failure rate for software/firmware attributes

λ_D is the hardware/device failure rate

λ_A is the failure rate for application considerations.

The failure rate contributions of each of these categories will be influenced by the disposition of a series of factors which are illustrated in Figure 2. In order to develop mathematical expressions which accurately characterize the reliability of LSI microcircuits, it is necessary to investigate how the variations of the individual factors actually influence device reliability.

The major portion of the complex microcircuit failure rate is related to the hardware considerations or to the inherent device reliability. The device failure rate, as suggested by previous models, is a function of the device characteristics and operational stresses. The device failure rate model form assumed at the onset of this study was similar to that of the existing MIL-HDBK-217B models:

$$\lambda_P = \lambda_T + \lambda_M$$

where:

λ_P is the device failure rate

λ_T is the temperature dependent device failure rate contribution

λ_M is the mechanical device failure rate contribution.

This model form is based upon accepted theoretical concepts and has demonstrated reasonable accuracy in small- and medium-scale integrated circuit reliability predictions. The factors which constitute the thermal and mechanical failure rates, as well as the appropriate weighting of their relative contributions to the total failure rate, were determined by the analyses of the extensive reliability data resources accumulated during this study. The types of analyses and their results are the subject of Sections 4.2 through 4.6.

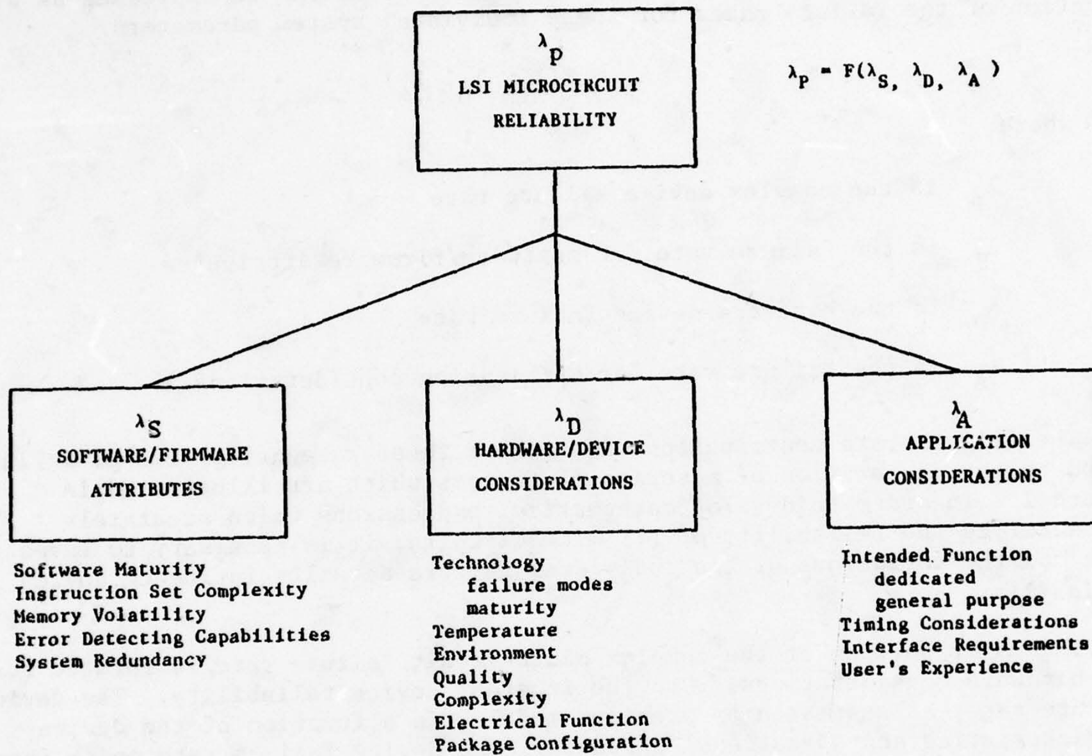


Figure 2: LSI Microcircuit Reliability Considerations.

The modeling of the application and software/firmware attributes presents a problem since many of these considerations cannot easily be expressed in terms of numerical values. In addition, the definitions of many of the factors involved are not universally accepted and thus introduce variations in interpretation and usage. While these software/firmware and application considerations do not apply to all complex devices, their impact on certain devices and device configurations suggests their inclusion in the reliability models for these components. The types of analyses and the results of these analyses are presented in Section 4.7.

4.2 Temperature Factors

A microcircuit's physical characteristics and fundamental principles of operation are defined by the device technology. The basic design and fabrication techniques employed in the implementation of different technologies result in a dramatic variation in the physical geometries, constituent materials and electrical characteristics of the fundmental device elements. Since the failures experienced in microcircuits can be directly related to the physical characteristics and limitations of the materials and techniques employed in the implementation of those devices, it is the device technology which inevitably has a major influence on microcircuit reliability.

The malfunction experiences within the different types of microcircuits are invaluable in defining the constituent failure mode distributions characteristic of each of the various device technologies. The failure mechanisms associated with each of the failure modes, as well as the stresses which activate these mechanisms, have been identified in the literature dealing with microcircuit physics-of-failure.

The data collection efforts in this study have provided an extensive amount of device malfunction data. The malfunction information was summarized by segregating the experienced defects into two categories: technology-related and package-related. These classifications are based upon the assumption that the experienced package-related defects for a given package configuration will be independent of the technology of the device contained within. However, an analysis of the technology-related defects revealed that experienced failure mode distributions for a given technology varied according to the packge configuration. Accordingly, the technology-related defects were summarized for each technology into hermetic and nonhermetic package categories. The resulting defect distributions are presented in Table 2 for Bipolar technologies in hermetic packages; Table 3 for Bipolar technologies in nonhermetic packages; Table 4 for MOS technologies in hermetic packages; and Table 5 for MOS technologies in nonhermetic packages. The percentage values in each column in these figures represent the normalized distribution of defects within that column.

The technology-related defect categories presented in Tables 2 through 5 can be grossly classified as being attributable to thermal or mechanical stresses. Temperature is generally considered to be the primary activating

TABLE 2. NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS FOR BIPOLAR DEVICES IN HERMETIC PACKAGES

Defect Category	TTL*	LTTL	STTL	LSTTL	ECL	I^2L
Surface Defects	15%	23%	25%	34%	13%	
Bulk Defects	6	5	3	2	1	
Oxide Defects	19	27	19	19	46	
Diffusion Defects	14	21	12	12	16	
Metallization Defects	46	24	41	33	24	
Malfunction Reports	278	107	79	41	324	**

TABLE 3. NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS FOR BIPOLAR DEVICES IN NONHERMETIC PACKAGES

Defect Category	TTL*	LTTL	STTL	LSTTL	ECL	I^2L
Surface Defects	22%	33%	32%	43%	19%	
Bulk Defects	8	4	2	3	3	
Oxide Defects	16	18	19	19	37	
Diffusion Defects	12	16	12	8	9	
Metallization Defects	42	29	35	27	32	
Malfunction Reports	83	57	59	37	108	**

* TTL includes all TTL families not otherwise mentioned.
** Insufficient data available to determine the distributions.

TABLE 4. NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS FOR MOS DEVICES IN HERMETIC PACKAGES

Defect Category	PMOS	NMOS	CMOS	MNOS
Surface Defects	35%	42%	52%	43%
Bulk Defects	1	3	1	---
Oxide Defects	25	26	18	33
Diffusion Defects	12	5	3	5
Metallization Defects	27	24	26	19
Malfunction Reports	148	72	142	21

TABLE 5. NORMALIZED DISTRIBUTIONS OF EXPERIENCED TECHNOLOGY-RELATED MALFUNCTIONS FOR MOS DEVICES IN NONHERMETIC PACKAGES

Defect Category	PMOS	NMOS	CMOS	MNOS
Surface Defects	61%	70%	74%	---
Bulk Defects	1	2	---	---
Oxide Defects	12	12	10	---
Diffusion Defects	8	4	1	---
Metallization Defects	18	12	15	---
Malfunction Reports	90	51	73	*

*Insufficient data to determine distribution.

stress since it has the most pronounced effect upon a substantial number of failure mechanisms experienced in microcircuit devices.

Several models have been developed to characterize failure mechanism temperature dependence and to provide an approximation of the relationship between stress (electrical and thermal), time, and failure rate. These models are typically intended to characterize individual failure mechanisms. However, failures in any given microcircuit population are seldom attributable to any single failure mechanism. This condition introduces difficulty in attempting to apply the established mathematical relationships in the modeling of microcircuit failure rate temperature dependence.

The approach pursued in this study involved the empirical determination of failure rate temperature dependence using actual reliability experiences at various temperature levels.

To facilitate the determination of failure rate temperature dependence for the various technologies, the reliability data for the technology-package categories, as presented in Tables 2 through 5, were combined according to the similarity in the defect distributions for the categories. For example, the defect distributions for plastic encapsulated TTL and hermetically packaged STTL (in Tables 2 and 3) are extremely similar. Therefore, the reliability data for these two technology-package categories (along with other categories) were merged together to form a more significant data resource for the determination of a temperature factor.

These resulting data sets were employed in the temperature factor determination. Initially, groups of entries with similar parameters and different temperature stresses were identified in each data set. These points served as the basis for an initial estimate of the impact of temperature variation on device failure rate. Preliminary temperature factor values were calculated using curve-fitting techniques on the various reliability data for the different technology-package categories. These initial calculations provided gross estimates of the temperature factors for each data entry to be employed in the subsequent analyses to determine other model parameter values.

The temperature factor analysis, like the analyses of all of the factors, involved an iterative process. The initial temperature factor values were recalculated after values had been determined for all other model parameters. The new values were utilized to recalculate values for other model parameters, and so on. The process was stopped when the highest index of determination had been achieved. The resulting temperature factor values for the various technology-package categories are presented in Tables 2.1.5-3 through 2.1.5-12 of the proposed model in Section 5.

An analysis of the CMOS technology data revealed that a second stress variable, other than temperature, had a significant influence upon device failure rate. A review of the literature confirmed this observation and suggested the use of a model which combines both temperature and voltage as life accelerating stresses. An analysis of the CMOS reliability data, supported by the findings reported in the literature, resulted in the introduction of a voltage stress derating factor which is employed as a direct multiplier of the

temperature factor.

The value of this parameter is set equal to 1.0 for any technology except for CMOS devices where the maximum recommended operating supply voltage is greater than 12 volts. The expressions for this factor reflect the reliability improvement which can be realized by derating the supply voltage for CMOS devices.

The approaches pursued in modeling failure rate temperature dependence in this study offer many benefits, including model flexibility. The temperature factors for various technology-package categories can be easily modified to accommodate the changing characteristics of evolving technologies. Emerging technologies may also be assigned slightly pessimistic temperature dependency values, initially, and realistic values when the technology becomes established.

4.3 Device Complexity Factors

The need for a reliability prediction technique specifically dedicated to complex microcircuits indicates that device complexity should be a primary consideration in the reliability model development. All previous modeling approaches (except 217A) have employed some type of device complexity factors. These factors have been based upon assorted device attributes including the physical characteristics of the device fabrication, number of oxide steps and contact cuts, number of active components, or device density.

The reliability consequences resulting from increased component densities have already been established and documented in the literature and in many study programs. For devices implemented using a given fabrication technique, any increase in chip density is accompanied by a reduction in the circuit element geometries. The smaller geometries place a greater emphasis on the tolerances required during the fabrication processes and also reduce the effectiveness of visual inspection techniques as a method of detecting surface defects and imperfections. The reduced width and spacing of metallization runs increase the susceptibility to bridging shorts and/or open metallization conditions. Smaller junction geometries also increase the criticality of fabrication processes and lower the characteristic breakdown voltages. In general, increased component density diminishes component reliability.

The fabrication techniques employed in the implementation of various device technologies inevitably become the limiting constraints of the achievable component densities and, therefore, device complexities. Some of the major discrepancies for complex devices in previous prediction models resulted from the derivation of complexity factors based upon current fabrication techniques. The predicted failure rates for the complex devices were extremely high because their implementation was "pushing the limits of the technology."

New technologies and fabrication techniques are constantly emerging offering greater component density capabilities without the degree of reliability decrement as invisioned with prior technologies. Techniques such as the self-aligning silicon gate process (introduced in NMOS devices) increased achievable densities, improved device performance, and enhanced device reli-

ability. The adaptation of this process to other MOS technologies produced similar benefits. The introduction of dual-level metallization, polysilicon intraconnection system, and many other innovative designs further increased the achievable device densities, pushing the technology limitations further outward.

The key to the derivation of realistic complexity factors for reliability prediction models is the determination of an indicator which accurately characterizes the device complexity. The bit complexity for memory devices would appear to be an obvious indicator of the complexity of these devices. However, a closer examination revealed subtleties associated with memory device complexity which merited consideration.

The monolithic memory devices can be grossly classified as either Random Access Memories (RAMs) or Read-Only Memories (ROMs). The ROM family consists of devices whose memory patterns are fixed and are not altered during normal operation. The RAM devices' memory patterns, on the other hand, are typically altered during normal operation. Obviously, the vastly different operational modes indicate that the circuitry required for the implementation of RAMs and ROMs varies dramatically. Additional complexity-sensitive attributes were identified within the RAM and ROM families.

The primary distinction in both the RAM and ROM families was based upon the technology--Bipolar or MOS. Similar devices implemented in Bipolar or MOS technologies require different numbers of functional elements and silicon real estate. An additional distinction was made in the MOS RAM family for static and dynamic operatonal modes. The memory matrix element for a static MOS RAM typically employs six to eight transistors and operates on a type of "flip-flop" principle. The dynamic memory cell typically employs four transistors and relies on parasitic capacitances to retain memory information. While the dynamic cells require periodic refresh to retain information, they offer lower power dissipation, lower element stresses, and require less silicon real estate than their static counterparts.

It is fairly obvious from an examination of the functional and circuit differences that a single set of complexity factors would not adequately characterize all of these memory configurations. Therefore, separate complexity factor sets were developed for Biplar RAMs, MOS static RAMs, MOS dynamic RAMs, Bipolar ROMs and MOS ROMs. The complexity factors utilized the device bit complexity as the complexity index.

The existing MIL-HDBK-217B prediction models employ two complexity factors, C_1 and C_2, to reflect the impact of device complexity. The C_1 factor represents the contribution of complexity to the temperature-dependent portion of the device failure rate. The C_2 factor represents the complexity contribution to the mechanical portion of the failure rate. This convention is valid since the technology-related defects, previously discussed, are manifested by both thermal and mechanical stresses.

The complexity values, C_1 and C_2, were derived in a fashion similar to the temperature factor values. To begin the analysis an initial assumption of $C_1 = 2C_2$ was made. The iterative process provided values of C_1 and C_2 for

various device complexities. A curve-fitting technique was employed to determine the forms of the C_1 and C_2 expressions. The newly calculated values were then subjected to additional modification in subsequent analyses until a reasonable index of determination was achieved. The coefficients for C_1 and C_2 derived from the regression analyses were incorporated into the complexity value expressions. These coefficients provide the appropriate weighting of the thermal and mechanical contributions to the technology failure rate.

The analysis of the ROM family data suggested that an additional factor was required to reflect the failures which were unique to the Programmable Read-Only Memories (PROMs). These devices are basically ROMs which are programmed by the device user. The PROM devices exhibit the same technology-related defects as their ROM counterparts, but also exhibit defects associated specifically with the PROM programming techniques.

Information was acquired from ROM and PROM manufacturers to compare the complexities associated with these devices. The data received indicated that the complexity differences between ROMs and PROMs were negligible for both bipolar and MOS devices. The only appreciable difference was the method in which the program was implemented.

A review of the literature suggested two possible types of failures associated with the PROM programming techniques; the loss of a programmed bit, and an undesired programming of a bit. An analysis of available PROM reliability data did not reveal any instances of a nonprogrammed bit location becoming programmed. Therefore, to simplify the model this failure mode was ignored. The bit loss failure mode includes fusible link growback, the recovery of shorted junctions, and charge leakage. Some of these types of failures have been observed in the experiences with PROM devices. The probability of occurrence for this type of failure is based upon the number of programmed elements, the type of programmed element, temperature, and device quality. An attempt to model the PROM programming technique based upon these factors would require an extensive reliability data base and would result in an extremely complicated mathematical expression.

To provide a simple estimate of the PROM programming technique failure rate contribution, an additional factor was developed for ROM and PROM devices. The values for this factor were derived from programming element failure experiences and are based on the assumption of 50% of the device bits being programmed. The values for the various programming techniques and the equations for determining these values are presented in Table 2.1.5-22 in Section 5.

The derivation of complexity factors for random logic LSI devices was somewhat more difficult. There is no unique, readily identifiable indicator of device complexity for this family of devices. Analyses were performed to determine the correlation between device complexity and various device attributes. The only reasonable correlation to device complexity was exhibited by a gate count estimator. The gate count estimators for the various devices were determined from the logic diagrams for the circuit functions. Where the logic diagrams were unavailable, transistor counts were employed with several conversion conventions to determine an approximate device gate count.

Random logic device functions were also partitioned into smaller complexity functions for which gate counts would be determined. The gate count for the entire device was then calculated by summing the approximations for the smaller function components. The derivation of C_1 and C_2 factors was performed in the same manner as the memory devices with a distinction between the Bipolar and MOS random logic devices.

To simplify the predictions for microprocessor devices, the manufacturers were contacted to determine gate count approximations. These values are listed, for many of the currently available microprocessors, in Table 2.1.5-26 in Section 5. Accompanying the microprocessor gate counts in Table 2.1.5-26 are a series of conventions for approximating the gate complexities for other random logic devices.

4.4 Quality Factors

All previous modeling techniques have assumed that the devices have been implemented utilizing a mature technology and that all infant mortality failures have been eliminated. In practice, infant mortality failures are minimized by subjecting the devices to some form of 100%-screening beyond the manufacturer's normal quality control practices. The device quality, in all previous modeling techniques, has been based upon the device procurement quality grade or the screening program to which the devices had been subjected.

In this study the same device quality grades are utilized. An initial analysis in this program employed the values directly from MIL-HDBK-217B for each of the quality factors. The values for each of the factors were modified according to the coefficients of the regression analyses. The resulting quality factors, presented in Tables 2.1.5-1 in Section 5, are extremely similar to higher-quality grades of the existing model. For the proposed quality factors a comparison of Class S to Class C would indicate an improvement factor of 16 to 1. The same comparison in the existing model would result in a 16 to 1 improvement.

The obvious discrepancy between the existing and proposed model quality factors is the value for Class D, commerical, off-the-shelf devices. The existing model presents two quality factors for this grade; a factor of 150 for hermetic devices, and a factor of 300 for nonhermetic devices. The proposed model distinguishes between hermetic and nonhermetic reliability in the temperature and package factors in addition to different quality factors. The proposed quality factors of 17.5 for hermetic and 35 for nonhermetic commercial devices are significantly lower than those presented in the present models.

This dramatic difference in quality factors between the existing and proposed models for commercial devices may be explained by considering the nature of the data used in deriving these factors in this study. The commercial device data employed in this study reflect the impact of recent advances and improvements in both technology and package fabrication. This is especially true for nonhermetic devices, where new plastics have resulted in im-

proved device quality. In addition, most of the commercial device data is from applications in non-hostile environments such as Ground, Fixed and Ground, Benign where the environmental and temperature stresses are minimal.

4.5 Package Factors

Integrated circuit packages are responsible for providing both protection from hostile environments and electrical connections for the device chip. The two primary reliability concerns related to device packages are the package hermeticity and interconnect wire integrity. The materials used in the fabrication of the various integrated circuit package types ultimately influence the package reliability characteristics. Consideration of the various package configuration attributes is essential in the derivation of prediction model package factors.

The package attributes which are considered to impact reliability include: package material, seal material and perimeter, number of interconnects, interconnect material, type of wirebonds and number of package leads. Due to the interdependencies among the package attributes, many of these variables can be combined and simplified.

For all practical purposes, the number of interconnects can be assumed to equal the number of package leads in LSI packages. The package material, seal material, and even the lead "frame" material and lead egress will be extremely interdependent. For example, a ceramic dual-in-line package typically employs a sandwich structure consisting of a kovar alloy lead frame, between an alumina base and lid, sealed with some type of solder glass with the lead egress through the glass seal. A ceramic/metal dual-in-line package typically employs a different set of constituents. These include: an alumina base, a thin-film conductor system with brazed leads, a kovar lid, and a solder seal to establish hermeticity. This grouping of package attributes according to typical package configuration interdependencies forms the most logical definition of microcircuit package classifications to be used in failure mode distribution analyses.

Based upon an analysis of integrated circuit package construction, five major package categories were developed. These categories include: Hermetic DIPs with solder or weld seals; Hermetic DIPs with glass seals; Nonhermetic DIPs; Flatpacks; and Metal Cans. The package failure mode information collected in this study is summarized for these package categories in Table 6.

The failure modes experienced in each package category, as well as their frequency of occurrence, will depend upon the physical characteristics of the package and the types of stresses experienced. The package failure modes are almost exclusively manifested by mechanical stresses. Therefore, the package complexity factors were developed as a contributor to the mechanical portion of the device failure rate.

The initial assumption was made that the package failure rate accounted for 40% of the total device failure rate. The number of functional pins (pins having electrical connections) was used as the index of package complexity. The relationships between package complexity and device failure rate were developed for each of the five package categories. These expressions, along

TABLE 6. NORMALIZED DISTRIBUTIONS OF EXPERIENCED PACKAGE-RELATED MALFUNCTIONS FOR VARIOUS PACKAGE CATEGORIES

Defect Category	Hermetic DIPS[1]	Hermetic DIPS[2]	Nonhermetic DIPS	Hermetic Flatpacks	Hermetic Cans
Wirebond & Die Attach Bond Defects	49%	15%	70%	39%	56%
Interconnect Wire Defects	5	8	29	7	10
Hermeticity & Lead Defects	46	77	1	54	34
Malfunction Reports	174	266	87	134	71

[1]Hermetic DIPs employing solder or weld seals

[2]Hermetic DIPs employing glass seals

with the package complexity values, are presented in Table 2.1.5-23 in Section 5.

4.6 Application Environment Factors

The primary activating stresses for integrated circuit failure modes are thermal or mechanical in nature. The thermal stress failure rate dependency is reflected in the prediction model temperature factor. Since the mechanical stresses are derived from environmental conditions, the mechanical failure rate dependency is reflected in the prediction model application environment factor.

The proposed models have adapted the environment categories, as presented in the existing MIL-HDBK-217B, with the additional distinction between the fighter and transport airborne environments. In the initial analyses the existing MIL-HDBK-217B application environment factors were utilized. However, subsequent modeling activities resulted in the modification of the parameter values. The application environment factors for the proposed models, which are presented in Table 2.1.5-2 in Section 5, are fairly similar to the existing values with the exception of the Ground, Benign, and Space, Flight values.

Since the available Space, Flight application environment data were extremely limited, the value for these two factors was derived based excusively upon Ground, Benign data. The data in the Ground, Benign category was largely commerical grade or class B-2 grade devices employed in computer systems. It is possible that a commercial Ground, Benign environment is more hostile or severe than a military Ground, Benign environment. Unfortunately, the data analyzed in this category were inconclusive in distinguishing between military and commercial Ground, Benign environments.

Application environment factors for categories where insufficient data were available were calculated using ratios based upon the existing MIL-HDBK-217B values.

4.7 Software/Firmware and Application Considerations

Since many complex microcircuits, especially microprocessors and their support devices, are frequently configured as a computer system, it is necessary to incorporate the reliability characteristics which result from system-related considerations into the overall reliability assessment of the devices. The literature review and the results of the RAC Microprocessor Reliability Survey (both previously discussed in Section 2.0) were employed as the sources for the identification of potential application and software/firmware reliability factors. These parameters, which are illustrated in Figure 2, are presented again for emphasis:

Software/Firmware Attributes

- Software Maturity
- Instruction Set Complexity
- Memory Volatility
- Error Detecting Capabilities
- System Redundancy

Application Considerations

- Intended Function
  - dedicated
  - general purpose
- Timing Considerations
- Interface Requirements
- User's Experience.

The survey results indicated that these factors constitute a significant percentage of the problems encountered with complex microcircuits during the system design and development phases. However, the frequency of these problems occurring in actual field usage was dramatically less than initially experienced. While the hardware reliability characteristics are considered to closely approximate the actual experienced device reliability, for most complex microcircuits, it is worthwhile to determine how some of these parameters influence the overall reliability of a particular group of complex devices, namely microprocessors.

One of the more obvious microprocessor reliability concerns is the software reliability. There are a large number of models which deal with the determination of software reliability. In an extremely simplified form, software reliability can be related to its complexity and maturity. Software maturity reflects the consequences of a learning process. As the software is used repeatedly, the "bugs" or the inherent defects are identified and corrected. Obviously, as the software complexity increases, the time required for debugging increases.

With microprocessor devices the software complexity can be related to the size of the device's instruction set. The software maturity is a function of the extent to which the software has been used. Microprocessor software which is "pirated" from existing computer systems will be more mature, and therefore more reliable, than similar software developed solely for that microprocessor.

From this discussion it would appear that a software reliability factor could readily be developed, for each microprocessor device, based upon instruction set maturity and complexity. Unfortunately, deriving such a software reliability factor would be extremely difficult. First, the software maturity is a rather abstract variable which could not easily be translated into a numerical value for a mathematical expression. Secondly, the software reliability would also be application dependent. That is, various applications may utilize different portions of the entire instruction set. (This dedicated vs. general-purpose function factor will be discussed in detail in later paragraphs.) As a result, the software reliability must be determined for microprocessors on an individual basis according to the intended application.

The other software/firmware attributes, including memory volatility, error detection capabilities, and system redundancy, are all factors which must be given consideration during system reliability determinations. These parameters can only be evaluated when considering the interaction of many components and cannot therefore be adequately addressed within a device reliability model.

Microprocessor timing considerations should be addressed at two levels. The timing sequences are critical to the proper transfer of data throughout the microprocessor system. Even slight timing deviations in the system could create discrepancies which could be difficult to detect. These problems must be considered at the system level through the use of parity checks and fault detection schemes.

The timing considerations can also be addressed at the component level (through its influence on the device power dissipation). Increasing clock frequency increases device power dissipation, resulting in increased junction temperatures and decreased reliability.

Interfacing logic is an important aspect of microprocessor systems. A microprocessor possesses its own internal characteristics which cannot be modified by the device user. External devices, such as I/O devices, program storage units, transducers, etc., each have their own characteristics. To enable the processor to control and process data associated with external devices, it is necessary to properly code and synchronize the system elements. This is primarily achieved through the use of hardware, such as latches, decoders, encoders, or converters, which translate the signals from one system element into usable signals for a second system element. Once the basic physical and electrical compatibility has been achieved between the system elements, a second level of integration may be achieved through software implementation.

The microprocessor manufacturers have recognized that interface logic is essential in the implementation of a microprocessor system. Accordingly, these manufacturers offer "part families" consisting of the most frequently used microprocessor peripherals. Reliability concerns resulting from interfacing considerations must also be considered at the system level since these aspects cannot be adequately reflected in device reliability predictions.

The application consideration which is thought to have the most dramatic impact upon device reliability is the intended function. Intuitively, a device performing a dedicated function would be more reliable than the same device in a general-purpose application. The underlying basis for this assumption, as well as the essence for all software/firmware and application reliability considerations, is device TESTABILITY.

It is generally accepted that as the number of functional elements required to implement a circuit increases, the time and the sophistication of the techniques to completely test the device increase dramatically. Considering all of the possible functional permutations for a single microprocessor, it would be totally impractical to completely test each device.

Complex devices employed in dedicated function applications, where only a small percentage of the devices' total capabilities are being utilized, can be tested more thoroughly than devices intended for general purpose applications. The comprehensive device testing would increase the probability of failure detection during early life, thus improving useful-lifetime reliability of the device population.

An effort was made in this study to derive a mathematical expression relating the intended application complexity to reliability. Unfortunately, several obstacles were encountered in this activity. First, the definitions of dedicated and general-purpose applications have never been universally accepted, introducing many problems in interpreting user data inputs. Secondly, most reliability data currently available on microprocessor devices do not indicate the software employed nor the details of the application or functions performed. However, it is recommended that this type of information be recorded and carefully scrutinized, in future efforts, to determine the relationship between functional application and complex device reliability.

Section 5

PROPOSED MEMORY AND LSI MODELS

This section presents the proposed reliability prediction models and supporting information for memory and random logic LSI monolithic microcircuits. These recommended revisions to the existing MIL-HDBK-217B models are the result of the analyses performed on the extensive data base compiled during this study. The format and paragraph numbering scheme presented in this section was selected to be consistent with MIL-HDBK-217B.

2.1.3 Monolithic Bipolar and MOS Random Logic LSI and Microprocessor Devices (equal to or greater than 100 gates)

$$\lambda_P = \pi_Q \left\{ C_1 \pi_T \pi_V + (C_2 + C_3)\pi_E \right\}$$

where:

λ_P is the device failure rate in $F/10^6$ Hours

π_Q is the quality factor, Table 2.1.5-1

π_T is the temperature acceleration factor, based on technology (Table 2.1.5-3) and is found in Tables 2.1.5-4 thru 2.1.5-12

π_V is the voltage derating stress factor, Table 2.1.5-13

π_E is the application environment factor, Table 2.1.5-2

C_1 and C_2 are device complexity failure rates based upon gate count and are found in Tables 2.1.5-17 and 2.1.5-18 (See Tables 2.1.5-24 thru 2.1.5-26 for gate count determination guidelines)

C_3 is the package complexity failure rate, Table 2.1.5-23

2.1.4 Monolithic MOS And Bipolar Memories

2.1.4.1 Random Access Memories (RAMs)

$$\lambda_p = \pi_Q \left\{ C_1 \pi_T \pi_V + (C_2 + C_3)\, \pi_E \right\}$$

where:

λ_p is the device failure rate in F/10^6 Hours

π_Q is the quality factor, Table 2.1.5-1

π_T is the temperature acceleration factor, based on technology (Table 2.1.5-3), and is found in Tables 2.1.5-4 thru 2.1.5-12

π_V is the voltage derating stress factor, Table 2.1.5-13

π_E is the application environment factor, Table 2.1.5-2

C_1 and C_2 are the device complexity failure rates based upon bit count and are found in Tables 2.1.5-19 and 2.1.5-20

C_3 is the package complexity failure rate, Table 2.1.5-23

2.1.4.2 Read-Only Memories (ROMs) And Programmable Read-Only Meomories (PROMs)

$$\lambda_p = \pi_Q \left\{ C_1 \pi_T \pi_V \pi_{PT} + (C_2 + C_3)\, \pi_E \right\}$$

where:

λ_p is the device failure rate in F/10^6 Hours

π_Q is the quality factor, Table 2.1.5-1

π_T is the temperature acceleration factor, based on technology (Table 2.1.5-3), and is found in Tables 2.1.5-4 thru 2.1.5-12

π_V is the voltage derating stress factor, Table 2.1.5-13

π_{PT} is the ROM and PROM programming technique factor, Table 2.1.5-22

π_E is the application environment factor, Table 2.1.5-2

C_1 and C_2 are the device complexity failure rates based upon bit count and are found in Table 2.1.5-21

C_3 is the package complexity failure rate, Table 2.1.5-23

2.1.5 Figures and Tables For the Monolithic Model Parameters

This section presents the tables and figures for quantifying the parameters of the failure rate models in Sections 2.1.1 through 2.1.4 for the various monolithic microelectronic device types. The tables are presented first, and then the figures.

TABLE 2.1.5-1: π_Q, QUALITY FACTORS

Quality Level	Description	π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements.	0.5
B	Procured in full accordance with MIL-M-38510, Class B requirements.	1.0
B-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with the electrical requirements of MIL-M-38510 slash sheet or vendor or contractor electrical parameters. The device must be qualified to requirements of MIL-STD-883, Method 5005, Class B. No waivers are allowed.	3.0
B-2	Procured to vendor's equivalent of screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with vendor's electrical parameters. Vendor waives certain requirements of MIL-STD-883, Method 5004, Class B.	6.5
C	Procured in full accordance with MIL-M-38510, Class C requirements.	8.0
C-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class C and in accordance with the electrical requirements of MIL-M-38510 slash sheet or vendor or contractor electrical specification. The device must be qualified to requirements of MIL-STD-883, Method 5005, Class C. No waivers are allowed.	13.0
D	Commercial (or non-mil standard) part, hermetically sealed, with no screening beyond the manufacturer's regular quality assurance practices.	17.5
D-1	Commercial (or non-mil standard) part, packaged or sealed with organic materials (e.g., epoxy, silicone or phenolic).	35.0

TABLE 2.1.5-2. π_E, APPLICATION ENVIRONMENT FACTORS

	Environment	π_E
G_B	Ground, Benign	1.0
S_F	Space, Flight	1.0
G_F	Ground, Fixed	2.5
A_{IT}	Airborne, Inhabited, Transport	3.5
G_M	Ground, Mobile	4.0
N_S	Naval, Sheltered	4.0
A_{UT}	Airborne, Uninhabited, Transport	4.0
N_U	Naval, Unsheltered	5.0
A_{IF}	Airborne, Inhabited, Fighter	7.0
A_{UF}	Airborne, Uninhabited, Fighter	8.0
M_L	Missile, Launch	10.0

TABLE 2.1.5-3. TECHNOLOGY TEMPERATURE FACTOR TABLES

Technology	Package Type	π_T Table Number
TTL*	Hermetic	2.1.5-4
	Nonhermetic	2.1.5-5
LTTL	Hermetic	2.1.5-5
	Nonhermetic	2.1.5-6
STTL	Hermetic	2.1.5-5
	Nonhermetic	2.1.5-6
LSTTL	Hermetic	2.1.5-6
	Nonhermetic	2.1.5-7
ECL	Hermetic	2.1.5-4
	Nonhermetic	2.1.5-5
I^2L	Hermetic	2.1.5-8
	Nonhermetic	2.1.5-11
PMOS	Hermetic	2.1.5-6
	Nonhermetic	2.1.5-10
NMOS	Hermetic	2.1.5-7
	Nonhermetic	2.1.5-11
MNOS	Hermetic	2.1.5-8
	Nonhermetic	2.1.5-11
CMOS	Hermetic	2.1.5-9
	Nonhermetic	2.1.5-12
LINEAR	Hermetic	2.1.5-9
	Nonhermetic	2.1.5-12

*TTL includes all TTL families not otherwise mentioned.

JUNCTION TEMPERATURE ESTIMATE

T_J, the worst case junction temperature in ^oC, shall be estimated by the following expressions:

$$T_J = T_C + \theta_{JC} P_{Max}$$

$$T_C = T_A + T_R$$

where:

- T_C is the case temperature in ^oC
- T_A is the ambient temperature in ^oC
- T_R is the system (or board) temperature rise above the ambient in ^oC
- θ_{JC} is the junction-to-case thermal resistance for a device soldered into a printed circuit board (^oC/watt)
- P_{Max} is the device maximum power dissipation (watts) from the appropriate specification. If a value for P_{Max} is not available, use a value contained in a specification for the closest equivalent device.

When specific values for θ_{JC} cannot be obtained, the following approximations shall be employed:

θ_{JC}, Junction-to-Case Thermal Resistance (^oC/Watt)

Package Type	Number of Package Pins	
	$\leq$22 pins	>22 pins
Hermetic DIPs[1]	30	25
Nonhermetic DIPs	125	100
Hermetic Flatpacks[1]	30	25
Hermetic Cans[1]	30	--

[1] For packages with epoxy or glass die attach use $\theta_{JC} = 125^oC$/Watt.

ENVIRONMENTAL TYPICAL TEMPERATURES

When specific values for environmental temperatures cannot be obtained, the following approximations shall be employed:

Environment	Typical Temperature (^{o}C)		
	Ambient, T_A	Rise Above T_A, T_R	Case, T_C
G_B	30	10	40
S_F	30	20	50
G_F	50	15	65
G_{FS}[1]	70	20	90
A_{IT}	55	20	75
G_M	55	15	70
G_{MS}[1]	70	20	90
N_S	60	15	75
A_{UT}	70	35	105
N_U	75	20	95
A_{IF}	55	20	75
A_{UF}	70	35	105
M_L	55	15	70

[1]Applications with solar radiation

TABLE 2.1.5-4. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	0.35	77	1.0	103	2.5
27	0.11	53	0.38	79	1.1	105	2.7
29	0.12	55	0.42	81	1.2	110	3.2
31	0.14	57	0.45	83	1.3	115	3.7
33	0.15	59	0.49	85	1.4	120	4.3
35	0.17	61	0.54	87	1.5	125	5.0
37	0.18	63	0.58	89	1.6	135	6.6
39	0.20	65	0.63	91	1.7	145	8.7
41	0.22	67	0.68	93	1.8	150	9.9
43	0.24	69	0.74	95	1.9	155	11.
45	0.27	71	0.80	97	2.1	165	14.
47	0.29	73	0.87	99	2.2	175	18.
49	0.32	75	0.93	101	2.4		

TABLE 2.1.5-5. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	0.41	77	1.4	103	3.8
27	0.11	53	0.45	79	1.5	105	4.1
29	0.13	55	0.50	81	1.6	110	4.9
31	0.14	57	0.55	83	1.7	115	5.8
33	0.16	59	0.60	85	1.9	120	6.9
35	0.18	61	0.66	87	2.0	125	8.1
37	0.20	63	0.72	89	2.2	135	11.
39	0.22	65	0.79	91	2.4	145	15.
41	0.24	67	0.87	93	2.6	150	18.
43	0.27	69	0.95	95	2.8	155	20.
45	0.30	71	1.0	97	3.0	165	27.
47	0.33	73	1.1	99	3.3	175	35.
49	0.37	75	1.2	101	3.5		

TABLE 2.1.5-6. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	0.48	77	1.8	103	5.6
27	0.11	53	0.53	79	2.0	105	6.1
29	0.13	55	0.59	81	2.2	110	7.5
31	0.15	57	0.66	83	2.4	115	9.1
33	0.17	59	0.73	85	2.6	120	11.
35	0.19	61	0.81	87	2.9	125	13.
37	0.21	63	0.90	89	3.1	135	19.
39	0.24	65	1.0	91	3.4	145	27.
41	0.27	67	1.1	93	3.7	150	31.
43	0.30	69	1.2	95	4.0	155	37.
45	0.34	71	1.4	97	4.4	165	50.
47	0.38	73	1.5	99	4.8	175	67.
49	0.43	75	1.6	101	5.2		

TABLE 2.1.5-7. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	0.56	77	2.4	103	8.4
27	0.12	53	0.63	79	2.7	105	9.2
29	0.13	55	0.71	81	3.0	110	12.
31	0.15	57	0.80	83	3.3	115	14.
33	0.18	59	0.89	85	3.6	120	18.
35	0.20	61	1.0	87	4.0	125	22.
37	0.23	63	1.1	89	4.4	135	32.
39	0.26	65	1.3	91	4.8	145	46.
41	0.30	67	1.4	93	5.3	150	56.
43	0.34	69	1.6	95	5.8	155	66.
45	0.38	71	1.8	97	6.4	165	93.
47	0.44	73	1.9	99	7.0	175	129.
49	0.49	75	2.2	101	7.7		

TABLE 2.1.5-8. π_T VS. JUNCTION TEMPERATURE

T_J (°C)	π_{TI}	T_J (°C)	π_{TI}	T_J (°C)	π_{TI}	T_J (°C)	π_{TI}
25	0.10	51	0.65	77	3.2	103	13.
27	0.12	53	0.74	79	3.6	105	14.
29	0.14	55	0.85	81	4.0	110	18.
31	0.16	57	0.96	83	4.5	115	22.
33	0.18	59	1.1	85	5.0	120	28.
35	0.21	61	1.2	87	5.6	125	35.
37	0.25	63	1.4	89	6.2	135	54.
39	0.29	65	1.6	91	6.9	145	81.
41	0.33	67	1.8	93	7.6	150	99.
43	0.38	69	2.0	95	8.5	155	120.
45	0.43	71	2.3	97	9.4	165	173.
47	0.50	73	2.5	99	10.	175	247.
49	0.57	75	2.9	101	11.		

TABLE 2.1.5-9. π_T VS. JUNCTION TEMPERATURE

T_J (°C)	π_{TI}	T_J (°C)	π_{TI}	T_J (°C)	π_{TI}	T_J (°C)	π_{TI}
25	0.10	51	0.76	77	4.3	103	19.
27	0.12	53	0.88	79	4.8	105	21.
29	0.14	55	1.0	81	5.5	110	27.
31	0.17	57	1.2	83	6.1	115	35.
33	0.19	59	1.3	85	6.9	120	45.
35	0.23	61	1.5	87	7.8	125	57.
37	0.27	63	1.7	89	8.7	135	91.
39	0.31	65	2.0	91	9.8	145	142.
41	0.36	67	2.3	93	11.	150	175.
43	0.42	69	2.6	95	12.	155	216.
45	0.49	71	2.9	97	14.	165	323.
47	0.57	73	3.3	99	15.	175	473.
49	0.61	75	3.8	101	17.		

TABLE 2.1.5-10. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{TI}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	0.89	77	5.7	103	28
27	0.12	53	1.0	79	6.5	105	32
29	0.14	55	1.2	81	7.4	110	42
31	0.17	57	1.4	83	8.4	115	55
33	0.20	59	1.6	85	9.6	120	72
35	0.24	61	1.9	87	11.	125	93
37	0.29	63	2.2	89	12.	135	154
39	0.34	65	2.5	91	14.	145	248
41	0.40	67	2.9	93	16.	150	311
43	0.47	69	3.3	95	18.	155	390
45	0.55	71	3.8	97	20.	165	600
47	0.65	73	4.4	99	23.	175	908
49	0.76	75	5.0	101	25.		

TABLE 2.1.5-11. π_T VS. JUNCTION TEMPERATURE

$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}	$T_J(^oC)$	π_{T1}
25	0.10	51	1.2	77	10	103	63
27	0.12	53	1.5	79	12	105	72
29	0.15	55	1.7	81	14	110	100
31	0.19	57	2.0	83	16	115	136
33	0.23	59	2.4	85	18	120	184
35	0.28	61	2.9	87	21	125	248
37	0.33	63	3.4	89	25	135	439
39	0.40	65	4.0	91	28	145	756
41	0.49	67	4.7	93	32	150	982
43	0.59	69	5.5	95	37	155	1269
45	0.71	71	6.4	97	43	165	2081
47	0.85	73	7.5	99	49	175	3337
49	1.0	75	8.7	101	57		

TABLE 2.1.5-12. π_T VS. JUNCTION TEMPERATURE

T_J (°C)	π_{T1}	T_J (°C)	π_{T1}	T_J (°C)	π_{T1}	T_J (°C)	π_{T1}
25	0.10	51	1.7	77	18.	103	142.
27	0.13	53	2.0	79	22.	105	165.
29	0.16	55	2.5	81	25.	110	236.
31	0.20	57	3.0	83	30.	115	335.
33	0.25	59	3.6	85	35.	120	472.
35	0.31	61	4.4	87	42.	125	659.
37	0.39	63	5.2	89	49.	135	1252.
39	0.48	65	6.3	91	57.	145	2308.
41	0.60	67	7.5	93	67.	150	3099.
43	0.73	69	9.0	95	78.	155	4134.
45	0.90	71	11.	97	91.	165	7210.
47	1.1	73	13.	99	106.	175	12,267.
49	1.4	75	15.	101	123.		

TABLE 2.1.5-13. π_V, VOLTAGE DERATING STRESS FACTOR

Technology	π_V
CMOS, V_{DD} = 5 volts	1.0
CMOS, 12 volts $\leq V_{DD} \leq$ 15.5 volts	Equation 1 (below)
CMOS, 18 volts $\leq V_{DD} \leq$ 20 volts	Equation 2 (below)
All technologies other than CMOS	1.0

V_{DD} is the maximum recommended operating supply voltage

Equation 1: For maximum recommended operating supply voltage between 12 and 15.5 volts.

$$\pi_V = 0.110\, e^X$$

where:

$$X = \frac{0.168\, Vs\, (T_J + 273)}{298}$$

Equation 2: For maximum recommended operating supply voltage between 18 and 20 volts.

$$\pi_V = 0.068\, e^X$$

where:

$$X = \frac{0.135\, Vs\, (T_J + 273)}{298}$$

Vs is the operating supply voltage in actual application
T_J is the device worst case junction temperature (°C)
e is the natural logarithm base, 2.71828

TABLE 2.1.5-17. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR BIPOLAR RANDOM LOGIC LSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
100	0.015	0.0012	850	0.045	0.0021	3400	0.091	0.0031
150	0.019	0.0013	900	0.046	0.0021	3600	0.093	0.0031
200	0.022	0.0014	950	0.048	0.0022	3800	0.096	0.0032
250	0.024	0.0015	1000	0.049	0.0022	4000	0.098	0.0032
300	0.027	0.0016	1200	0.053	0.0023	4250	0.101	0.0033
350	0.029	0.0016	1400	0.058	0.0024	4500	0.104	0.0033
400	0.031	0.0017	1600	0.062	0.0025	4750	0.107	0.0034
450	0.033	0.0018	1800	0.066	0.0026	5000	0.110	0.0034
500	0.034	0.0018	2000	0.069	0.0027	5500	0.116	0.0035
550	0.036	0.0019	2200	0.073	0.0027	6000	0.121	0.0036
600	0.038	0.0019	2400	0.076	0.0028	6500	0.126	0.0037
650	0.039	0.0019	2600	0.079	0.0029	7000	0.131	0.0038
700	0.041	0.0020	2800	0.082	0.0029	7500	0.135	0.0039
750	0.042	0.0020	3000	0.085	0.0030			
800	0.044	0.0021	3200	0.088	0.0030			

Tabulated values are determined by the following equations:

$$C_1 = 1.48 \times 10^{-3} (N_G)^{0.506}$$

$$C_2 = 3.20 \times 10^{-4} (N_G)^{0.279}$$

where N_G is the number of gates.

TABLE 2.1.5-18. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR MOS RANDOM LOGIC LSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	Gates	C_1	C_2	No. Gates	C_1	C_2
100	0.011	0.0007	850	0.026	0.0012	3400	0.045	0.0016
150	0.013	0.0008	900	0.027	0.0012	3600	0.046	0.0016
200	0.015	0.0008	950	0.027	0.0012	3800	0.047	0.0016
250	0.016	0.0009	1000	0.028	0.0012	4000	0.048	0.0016
300	0.017	0.0009	1200	0.030	0.0013	4250	0.049	0.0017
350	0.018	0.0009	1400	0.032	0.0013	4500	0.051	0.0017
400	0.019	0.0010	1600	0.033	0.0013	4750	0.052	0.0017
450	0.020	0.0010	1800	0.035	0.0014	5000	0.053	0.0017
500	0.021	0.0010	2000	0.037	0.0014	5500	0.055	0.0018
550	0.022	0.0010	2200	0.038	0.0014	6000	0.057	0.0018
600	0.023	0.0011	2400	0.039	0.0015	6500	0.059	0.0018
650	0.023	0.0011	2600	0.041	0.0015	7000	0.060	0.0019
700	0.024	0.0011	2800	0.042	0.0015	7500	0.062	0.0019
750	0.025	0.0011	3000	0.043	0.0015			
800	0.025	0.0011	3200	0.044	0.0016			

Tabulated values are determined by the following equations:

$$C_1 = 1.75 \times 10^{-3} \, (N_G)^{0.400}$$

$$C_2 = 2.52 \times 10^{-4} \, (N_G)^{0.226}$$

where N_G is the number of gates.

Note: This table applies to both static and dynamic operation devices.

TABLE 2.1.5-19. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR BIPOLAR RAMs IN FAILURES PER 10^6 HOURS

Bit Complexity	C_1	C_2
16	0.011	0.0002
32	0.016	0.0003
64	0.024	0.0004
128	0.036	0.0006
256	0.054	0.0009
320	0.061	0.0010
512	0.080	0.0013
576	0.086	0.0014
1024	0.119	0.0019
2048	0.178	0.0027
2560	0.202	0.0031
4096	0.265	0.0040
8192	0.395	0.0059
9216	0.423	0.0063
16,384	0.589	0.0086

Tabulated values are determined by the following equations:

$$C_1 = 2.2 \times 10^{-3} (B)^{0.576}$$

$$C_2 = 4.0 \times 10^{-5} (B)^{0.554}$$

where B is the number of bits ($\leq$ 16,384)

TABLE 2.1.5-20. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR MOS RAMS IN FAILURE PER 10^6 HOURS

	Dynamic		Static	
Bit Complexity	C_1	C_2	C_1	C_2
16	0.003	0.00015	0.004	0.00022
32	0.004	0.00023	0.006	0.00033
64	0.006	0.00034	0.009	0.0005
128	0.010	0.0005	0.014	0.0008
256	0.015	0.0008	0.022	0.0012
320	0.017	0.0009	0.026	0.0013
512	0.022	0.0012	0.035	0.0018
1024	0.034	0.0017	0.055	0.0027
2048	0.052	0.0026	0.087	0.0042
2560	0.060	0.0030	0.101	0.0048
4096	0.080	0.0039	0.137	0.0063
8192	0.122	0.0058	0.216	0.0097
9216	0.131	0.0063	0.233	0.0104
16,384	0.186	0.0088	0.339	0.015
32,768	0.284	0.013	0.533	0.022
65,536	0.434	0.020	0.838	0.034

Tabulated values are determined by the following equations:

Dynamic RAMs $C_1 = 5.0 \times 10^{-4}(B)^{0.610}$ $C_2 = 3.0 \times 10^{-5}(B)^{0.585}$

Static RAMS $C_1 = 6.0 \times 10^{-4}(B)^{0.653}$ $C_2 = 4.0 \times 10^{-5}(B)^{0.609}$

where B is the number of bits ($\leq 65,536$)

TABLE 2.1.5-21. C_1 AND C_2 DEVICE COMPLEXITY FAILURE RATES FOR ROMs AND PROMs IN FAILURES PER 10^6 HOURS

	Bipolar		MOS	
Bit Complexity	C_1	C_2	C_1	C_2
16	0.0026	0.00013	0.0039	0.00020
32	0.0034	0.00017	0.0052	0.00026
64	0.0044	0.00022	0.0070	0.00035
128	0.0058	0.00028	0.0094	0.00046
256	0.0076	0.00037	0.013	0.00060
320	0.0083	0.0004	0.014	0.00066
512	0.010	0.0005	0.017	0.0008
1024	0.013	0.0006	0.023	0.0010
2048	0.017	0.0008	0.031	0.0014
2560	0.018	0.0009	0.034	0.0015
4096	0.022	0.0010	0.041	0.0018
8192	0.029	0.0014	0.055	0.0024
9216	0.030	0.0014	0.058	0.0025
16,384	0.038	0.0018	0.074	0.0032
32,768	0.050	0.0023	0.100	0.0042
65,536	0.065	0.0030	0.134	0.0055

Tabulated values are determined from the following equations:

Bipolar $C_1 = 8.8 \times 10^{-4}(B)^{0.388}$ $C_2 = 4.5 \times 10^{-5}(B)^{0.378}$

MOS $C_1 = 1.2 \times 10^{-3}(B)^{0.425}$ $C_2 = 6.6 \times 10^{-5}(B)^{0.399}$

where B is the number of bits ($\leq$ 65,536)

TABLE 2.1.5-22. π_{PT}, ROM AND PROM PROGRAMMING TECHNIQUE FACTORS

Device Type	Technology	Programming Technique	π_{PT}
ROM	Bipolar	Metal Mask	1.0
	MOS	Metal Mask	1.0
PROM	Bipolar	NiCr or TiW Links	Equation 1 (below)
		Polysilicon Links	1.0
		Shorted Junction (AIM)	1.0
	MOS	UV and Electrically Erasable	Equation 2 (below)

Equation 1: For Bipolar PROMs utilizing NiCr or TiW Links:

$$\pi_{PT} = 0.985 + 9.5 \times 10^{-5}(B)$$

where B is the number of bits.

Equation 2: For MOS PROMs, both UV and Electrically Erasable:

$$\pi_{PT} = 0.950 + 7.5 \times 10^{-5}(B)$$

where B is the number of bits.

TABLE 2.1.5-23. C_3, PACKAGE COMPLEXITY FAILURE RATES IN FAILURES PER 10^6 HOURS

	Package Type				
Number Of Functional Pins	Hermetic DIPs with Solder or Weld Seal	Hermetic DIPS with Glass Seal	Nonhermetic DIPS	Hermetic Flatpacks	Hermetic Cans
3	--	--	--	--	0.0003
4	--	--	--	0.0004	0.0005
6	0.0019	0.0013	0.0018	0.0008	0.0011
8	0.0026	0.0021	0.0026	0.0013	0.0020
10	0.0034	0.0029	0.0034	0.0020	0.0031
12	0.0041	0.0038	0.0043	0.0028	0.0044
14	0.0048	0.0048	0.0051	0.0037	0.0060
16	0.0056	0.0059	0.0061	0.0047	0.0079
18	0.0064	0.0071	0.0070	0.0058	--
22	0.008	0.010	0.009	0.008	--
24	0.009	0.011	0.010	0.010	--
28	0.010	0.014	0.012	--	--
36	0.013	0.020	0.016	--	--
40	0.015	0.024	0.019	--	--
64	0.025	0.048	0.033	--	--

The tabulated values are determined by the following equations:

Hermetic DIPS with solder or weld seals $C_3 = 2.8 \times 10^{-4}(N_p)^{1.08}$

Hermetic DIPS with glass seals $C_3 = 9.0 \times 10^{-5}(N_p)^{1.51}$

Nonhermetic DIPS $C_3 = 2.0 \times 10^{-4}(N_p)^{1.23}$

Hermetic Flatpacks $C_3 = 3.0 \times 10^{-5}(N_p)^{1.82}$

Hermetic Cans $C_3 = 3.0 \times 10^{-5}(N_p)^{2.01}$

where:

N_p is the number of functional package Pins.

TABLE 2.1.5-26: GATE COUNT FOR MICROPROCESSOR INTEGRATED CIRCUITS

Commercial Type	M38510/ XXXXX	Technology	Number Of Gates	Complexity Factors C_1	C_2
1802A	47001	CMOS	1375	0.032	0.0013
2901A	44001	LSTTL	537	0.036	0.0018
3850	N/A	NMOS	3530	0.046	0.0016
3851	N/A	NMOS	1623	0.034	0.0013
6800	40001	NMOS	1300	0.031	0.0013
8080A	42001	NMOS	1100	0.029	0.0012
8085	N/A	NMOS	2067	0.037	0.0014
9900	46001	IIL	3100	0.086	0.0030
10800	N/A	ECL	350	0.029	0.0016
Z-80	N/A	NMOS	2833	0.042	0.0015

General Guidelines for Random Logic LSI Gate Count Determination

1. Using vendors logic diagram, count the number of logic gates. For devices employing flip-flops use the following estimates:

   T-Type and D-Type - 6 gates
   RS-Type and JK-Type - 8 gates

2. Where logic diagram is unavailable use device transistor count to determine gate counts using the following approximations:

   Bipolar: No. Transistors ÷ 2.5
   CMOS: No. Transistors ÷ 3.75
   Other MOS: No. Transistors ÷ 3.0

Section 6

EVALUATION OF PROPOSED MODELS

Prior to the preliminary model development activities, several sets of field experience data entries were segregated from the complex microcircuit reliability data resources. These data entries were not employed during the model development, as they were intended to be used in the model validation activities to demonstrate that the proposed models are accurate for data points other than those employed in the model development. The data points were selected to represent a majority of the possible model parameter conditions.

The data entries are presented, along with observed and predicted failure rate values, by the following categories:

Table 7. Bipolar RAM and Shift Register Data

Table 8. MOS Dynamic RAM and Shift Register Data

Table 9. MOS Static RAM and Shift Register Data

Table 10. ROM and PROM Data

Table 11. Ramdom Logic LSI Data.

The data entries in each of the Tables present a summary of the model parameter conditions, the total number of device hours and failures, and the 60% Chi-square confidence interval and point estimate failure rates, and predicted failure rate values calculated using MIL-HDBK-217B (including Notice II, dated 17 March 1978) and the proposed models.

In addition to the tabulated data, the correlation between the observed failure rates and the predicted failures calculated using MIL-HDBK-217B and the proposed models are presented graphically for each of the data sets in Figures 3 through 12.

In each of the observed vs. MIL-HDBK-217B predicted failure rate graphs, the data points are almost exclusively situated in the predicted-greater-than-observed failure rate regions. This condition indicated that the failure rate predictions calculated using MIL-HDBK-217B are generally pessimistic with respect to actual experiences. It should be noted that the MIL-HDBK-217B predictions were calculated using the modified complexity factor values as presented in Notice II. Predictions calculated employing the complexity factors presented in Notice I resulted in even more pessimistic values.

The graphs presenting the proposed model predicted vs. observed failure rates illustrate extremely good correlation in each case. The test entries in each of the data sets are positioned directly on or very close to the predicted-equal-to-observed failure rate lines, demonstrating extremely good model accuracy.

TABLE 7. BIPOLAR RAM AND SHIFT REGISTER DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_j (°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	TTL	16	Flat Pack	16	55	C-1	AIF	4.240	3	0.36	0.71	1.30	0.82	0.51
2	LTTL	16	PL-DIP	16	50	D-1	GB	16.800	11	0.49	0.65	0.88	0.66	0.46
3	TTL	64	PL-DIP	16	55	D-1	GB	4.450	3	0.34	0.67	1.24	1.83	0.65
4	STTL	64	PL-DIP	16	55	D-1	GB	34.756	14	0.31	0.40	0.52	1.83	0.72
5	TTL	256	Flat Pack	16	40	B-1	GF	23.391	1	0.01	0.04	0.13	0.08	0.08
6	TTL	256	C-DIP	16	45	B-1	GF	5.142	1	0.04	0.19	0.58	0.09	0.10
7	ECL	256	C-DIP	16	55	D	GB	55.000	8	0.10	0.15	0.21	5.34	0.52
8	TTL	1024	Flat Pack	16	70	B-2	GF	0.744	2	1.11	2.69	5.75	0.78	0.70

*Predictions Using Notice II Dated 17 March 1978.

TABLE 8. MOS DYNAMIC RAM AND SHIFT REGISTER DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_j (°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	PMOS	50	CAN	10	35	S	SF	1.963	0	--	--	0.82	0.01	0.01
2	PMOS	128	CAN	8	35	B-1	GF	2.761	0	--	--	0.58	0.06	0.03
3	PMOS	320	CM-DIP	16	60	D	GB	16.486	7	0.29	0.42	0.62	8.97	0.34
4	PMOS	1024	CAN	8	50	B-1	NS	16.354	2	0.05	0.12	0.26	0.75	0.09
5	NMOS	2048	PL-DIP	16	55	D-1	GB	2.290	1	0.10	0.44	1.31	37.92	3.40
6	PMOS	2048	C-DIP	14	65	D	AIF	4.851	9	1.33	1.86	2.58	59.93	1.82
7	NMOS	4096	CM-DIP	16	60	D	GB	3.110	4	0.74	1.29	2.16	42.27	1.50
8	NMOS	4096	CM-DIP	22	60	D	GB	100.000	174	1.63	1.74	1.87	42.27	1.54

*Predictions Using Notice II Dated 17 March 1978.

TABLE 9. MOS STATIC RAM AND SHIFT REGISTER DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_j(°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	PMOS	256	CM-DIP	16	45	B-1	NS	2.600	0	--	--	0.62	0.28	0.10
2	PMOS	320	C-DIP	16	55	D	GF	114.011	52	0.40	0.46	0.53	7.41	0.58
3	NMOS	1024	C-DIP	16	40	B-1	GB	29.670	6	0.13	0.20	0.31	0.14	0.07
4	NMOS	1024	C-DIP	16	40	D	GB	61.510	26	0.35	0.42	0.51	4.33	0.42
5	NMOS	1024	S-DIP	16	40	D	GB	1.168	0	--	--	1.38	8.66	1.17
6	NMOS	1024	S-DIP	16	40	D	GF	4.480	4	0.51	0.89	1.50	14.42	1.64
7	PMOS	2048	C-DIP	18	65	C-1	AIF	3.850	8	1.45	2.08	2.96	35.96	2.16
8	NMOS	4096	E-DIP	22	60	D	GB	85.440	594	6.71	6.95	7.20	82.29	13.00

*Predictions Using Notice II Dated 17 March 1978.

TABLE 10. ROM AND PROM DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_j(°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	ECL NiCr PROM	16	PL-DIP	14	45	D-1	GB	8.800	1	0.03	0.11	0.34	0.28	0.21
2	STTL ROM	1024	CM-DIP	16	50	B-2	GB	50.500	4	0.05	0.08	0.13	0.08	0.07
3	STTL PolySi PROM	1024	S-DIP	16	65	D-1	GB	0.537	0	--	--	3.00	4.24	0.69
4	TTL AIM/NiCr PROM	2048	CM-DIP	16	60	B-2	GB	7.933	3	0.19	0.38	0.70	0.18	0.11
5	PMOS UV PROM	2048	CM-DIP	24	60	D	GF	1.678	2	0.49	1.19	2.55	8.79	0.92
6	PMOS ROM	2560	C-DIP	24	50	D	GB	8.243	2	0.10	0.24	0.52	4.37	0.49
7	NMOS UV PROM	8192	CM-DIP	24	50	D	GB	2.800	1	0.08	0.36	1.07	8.81	1.00
8	STTL ROM	9216	CM-DIP	24	55	B-1	GM	1.131	0	--	--	1.42	0.73	0.17

*Predictions Using Notice II Dated 17 March 1978

TABLE 11. RANDOM LOGIC LSI DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Gate Complexity	Package	No. Pins	T_j(°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	LSTTL	108	E-DIP	20	45	D-1	GB	2.160	0	--	--	0.75	3.86	0.54
2	TTL	138	C-DIP	16	50	B-1	GF	1.130	1	0.20	0.88	1.42	0.18	0.07
3	NMOS	350	CM-DIP	40	50	D	GB	1.110	1	0.20	0.90	2.70	9.43	0.45
4	P-MNOS	525	CM-DIP	40	45	D	GF	17.900	22	1.00	1.23	1.50	13.11	0.87
5	PMOS	560	CM-DIP	16	50	D	GF	17.500	13	0.57	0.74	0.94	17.40	0.47
6	NMOS	1100	CM-DIP	40	55	D	GF	1.400	2	0.59	1.43	3.06	34.65	1.07
7	NMOS	1300	CM-DIP	40	55	D	GB	6.600	3	0.23	0.45	0.84	36.09	0.67
8	PMOS	2000	E-DIP	16	55	D-1	GB	19.800	28	1.19	1.41	1.69	144.60	1.82

*Predictions Using Notice II Dated 17 March 1978.

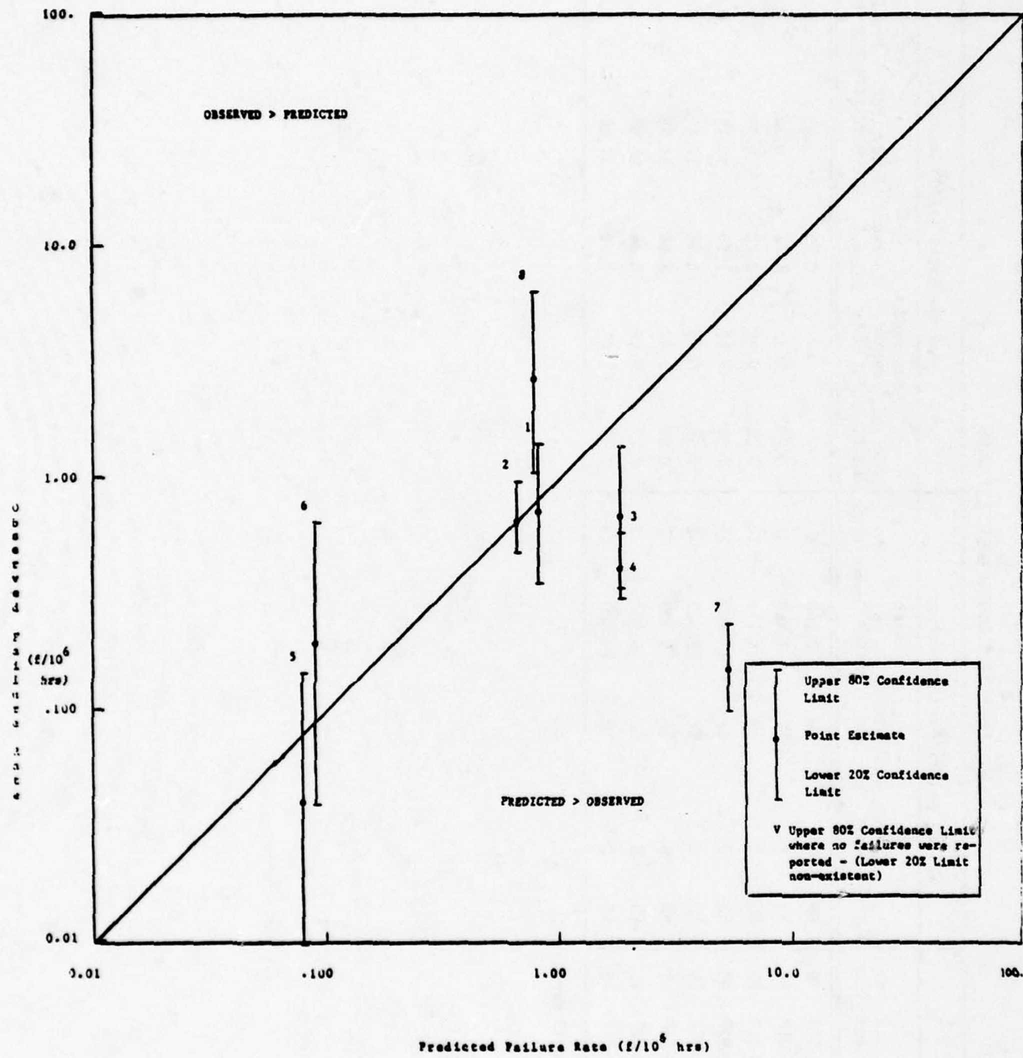


Figure 3: Bipolar RAM and Shift Register Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates

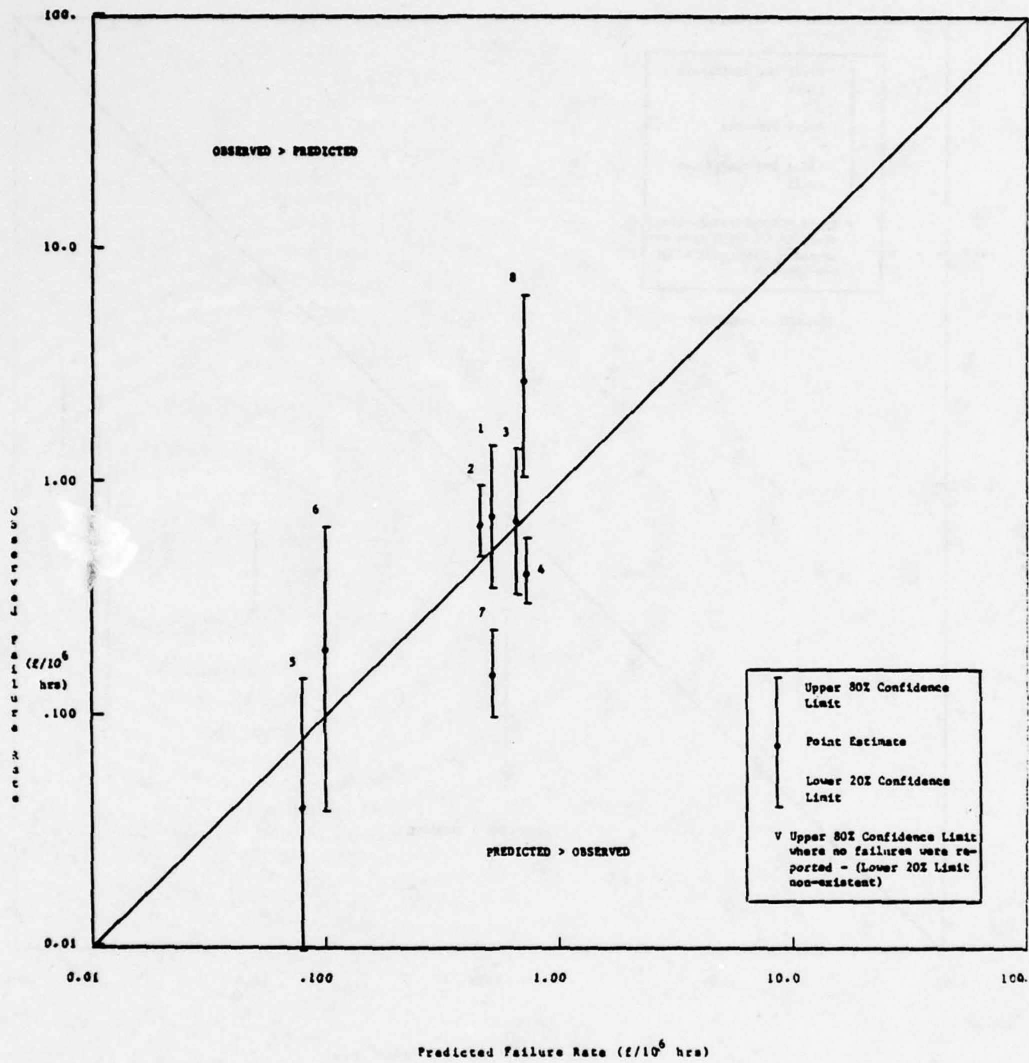


Figure 4: Bipolar RAM and Shift Register Observed Failure Rates vs. Proposed Model Predicted Failure Rates

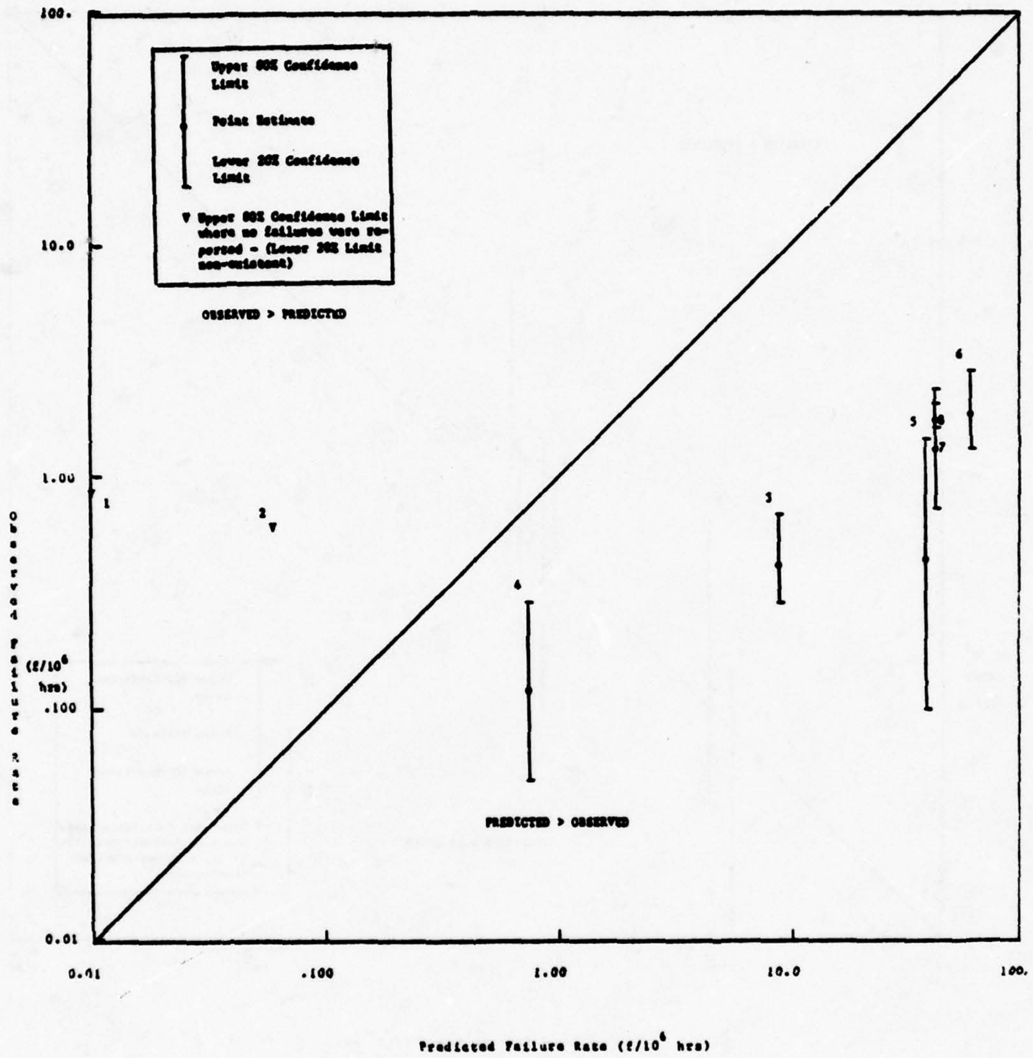


Figure 5: MOS Dynamic RAM and Shift Register Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates

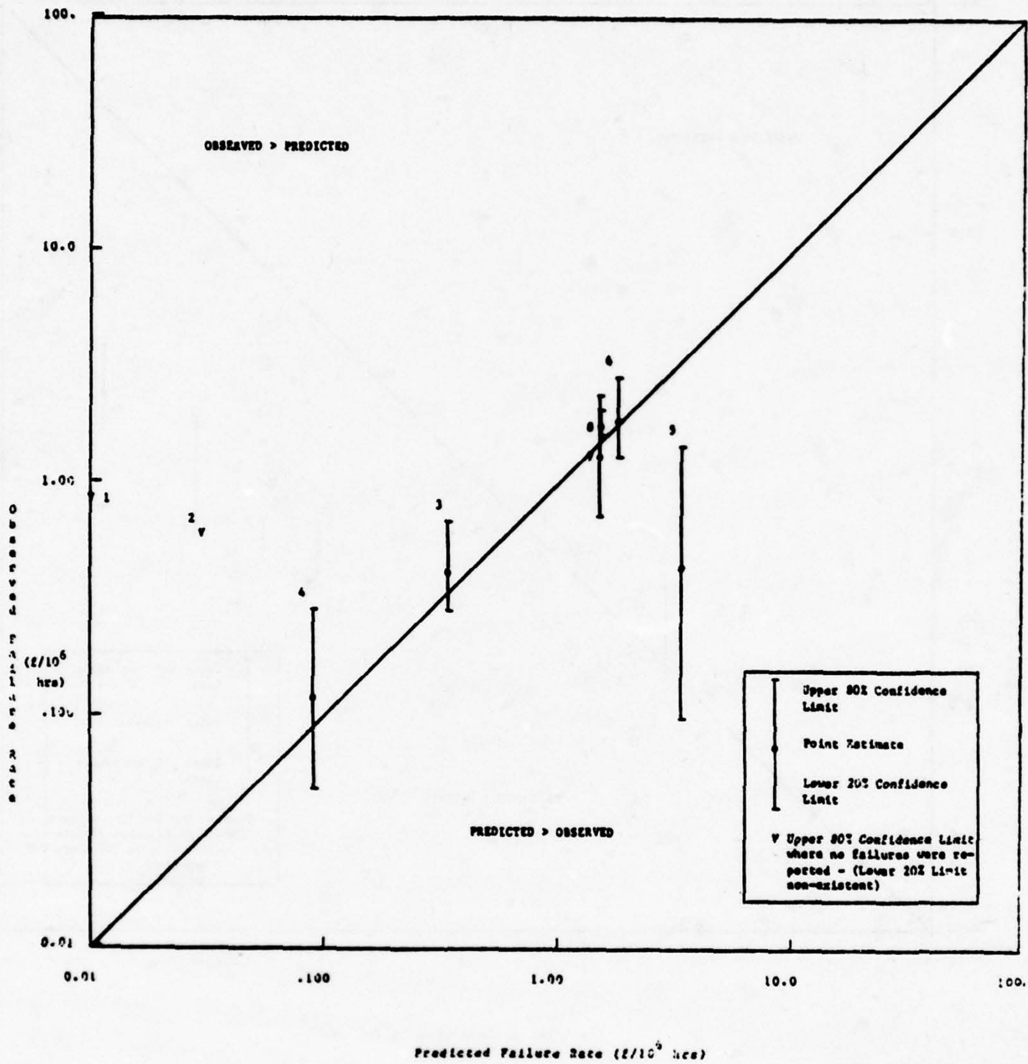


Figure 6: MOS Dynamic RAM and Shift Register Observed Failure Rates vs. Proposed Model Predicted Failure Rates

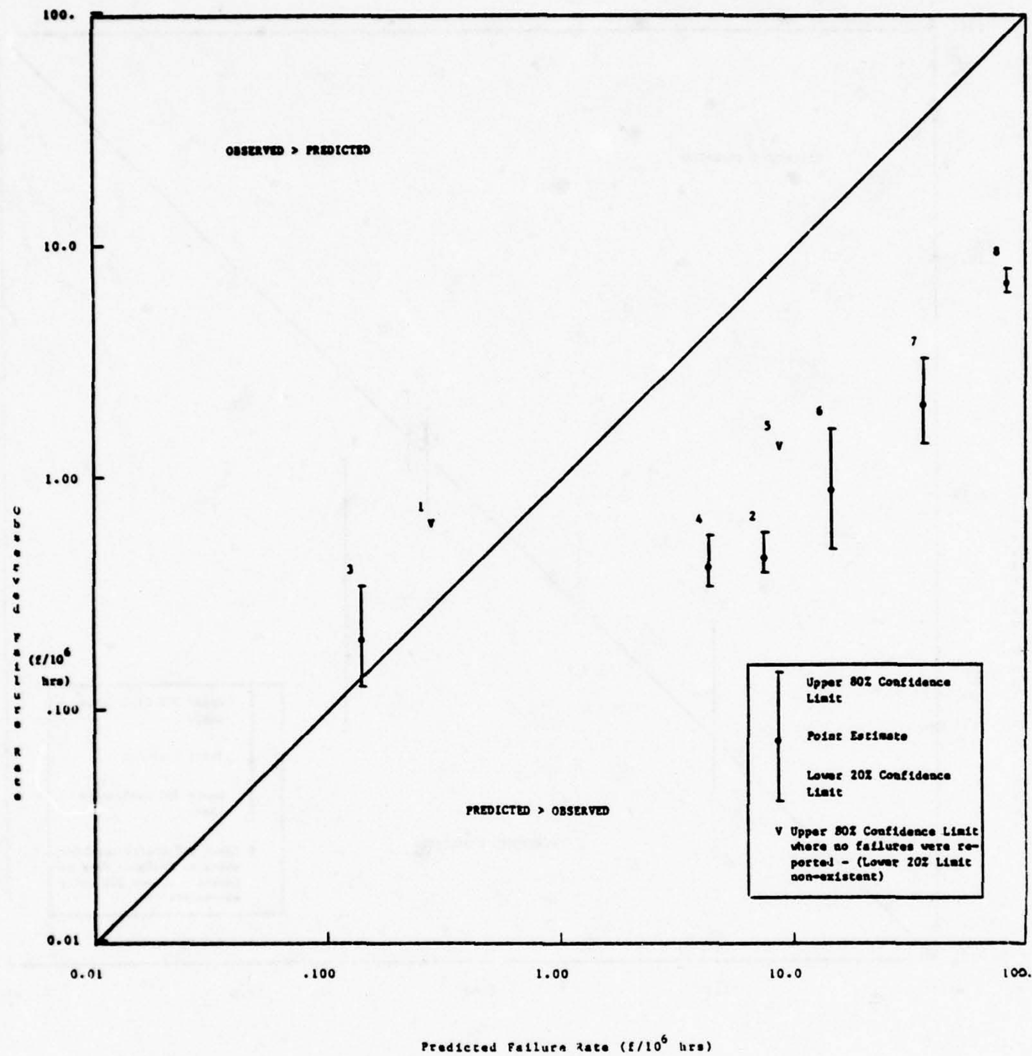


Figure 7: MOS Static RAM and Shift Register Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates

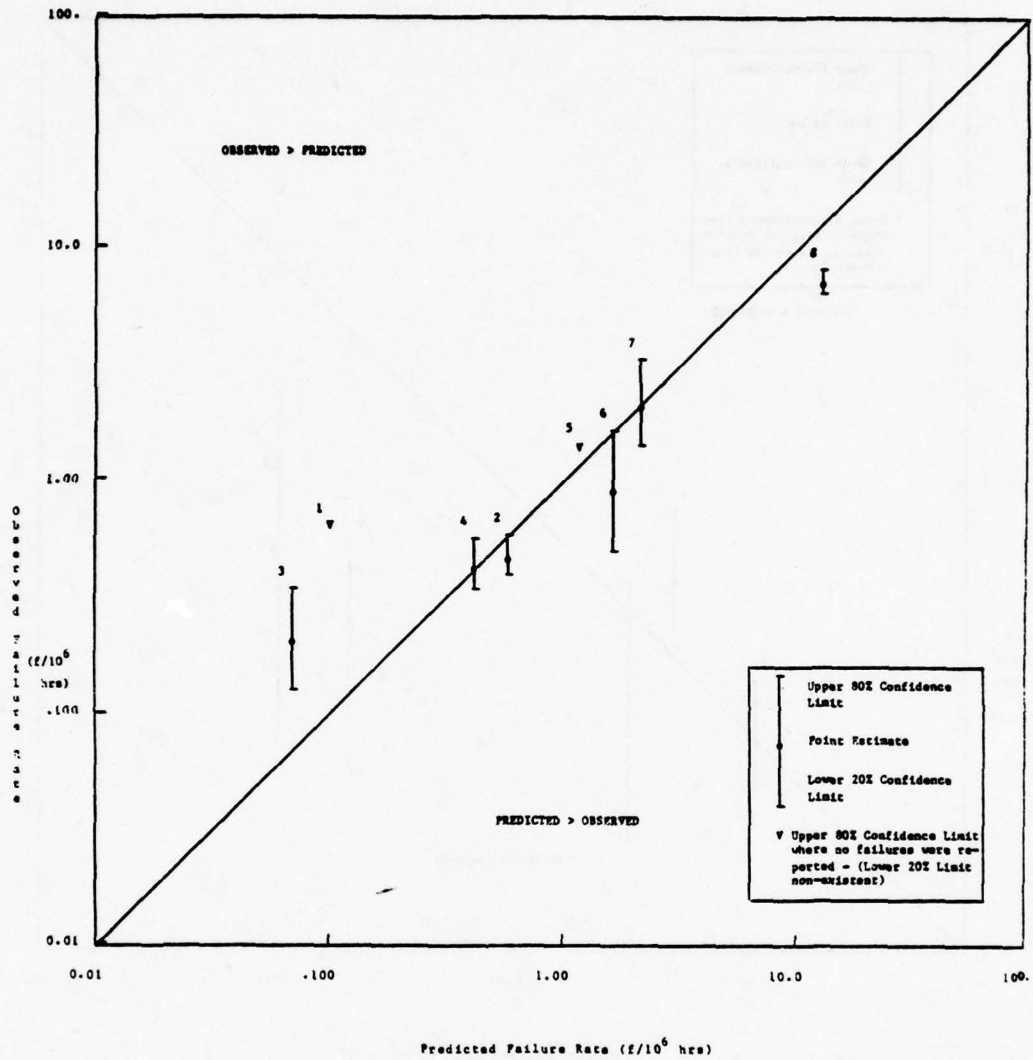


Figure 8: MOS Static RAM and Shift Register Observed Failure Rates vs. Proposed Model Predicted Failure Rates

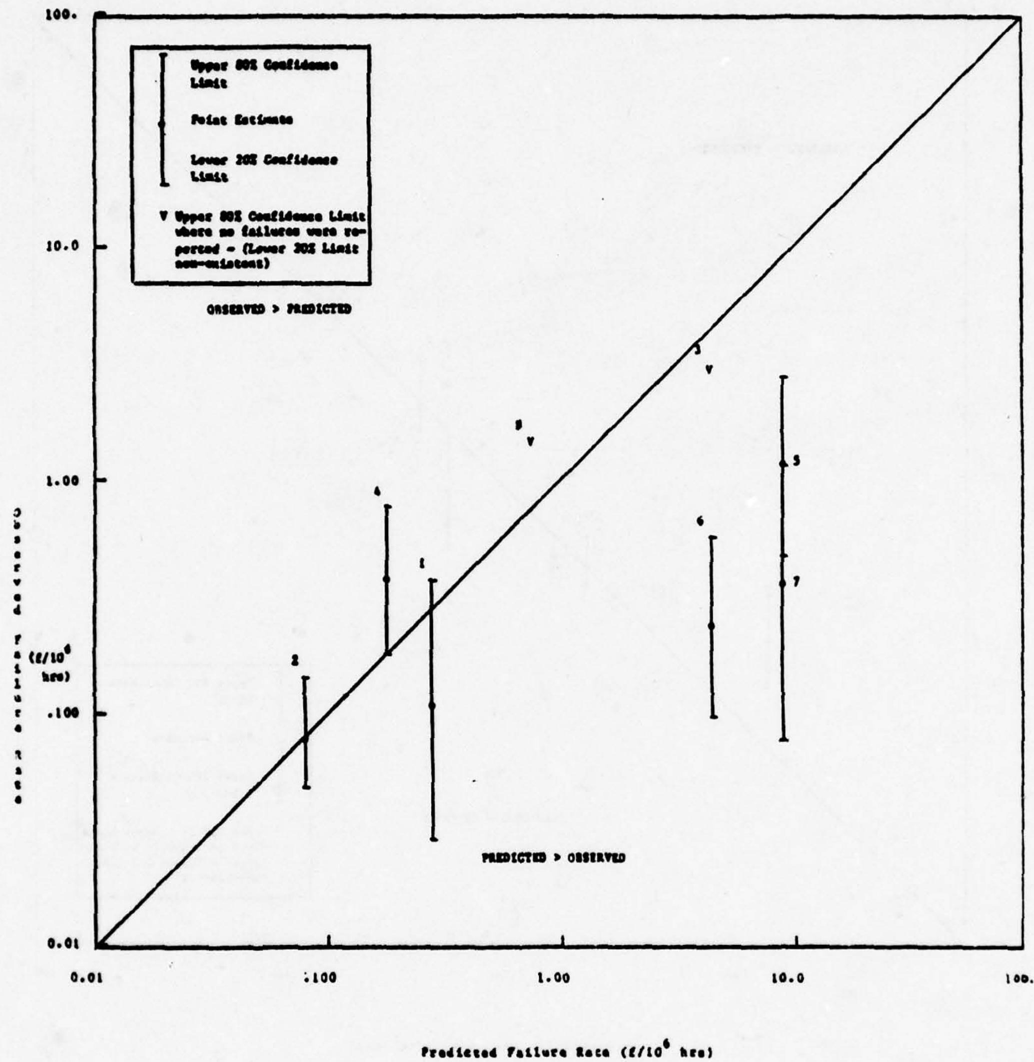


Figure 9: ROM and PROM Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates

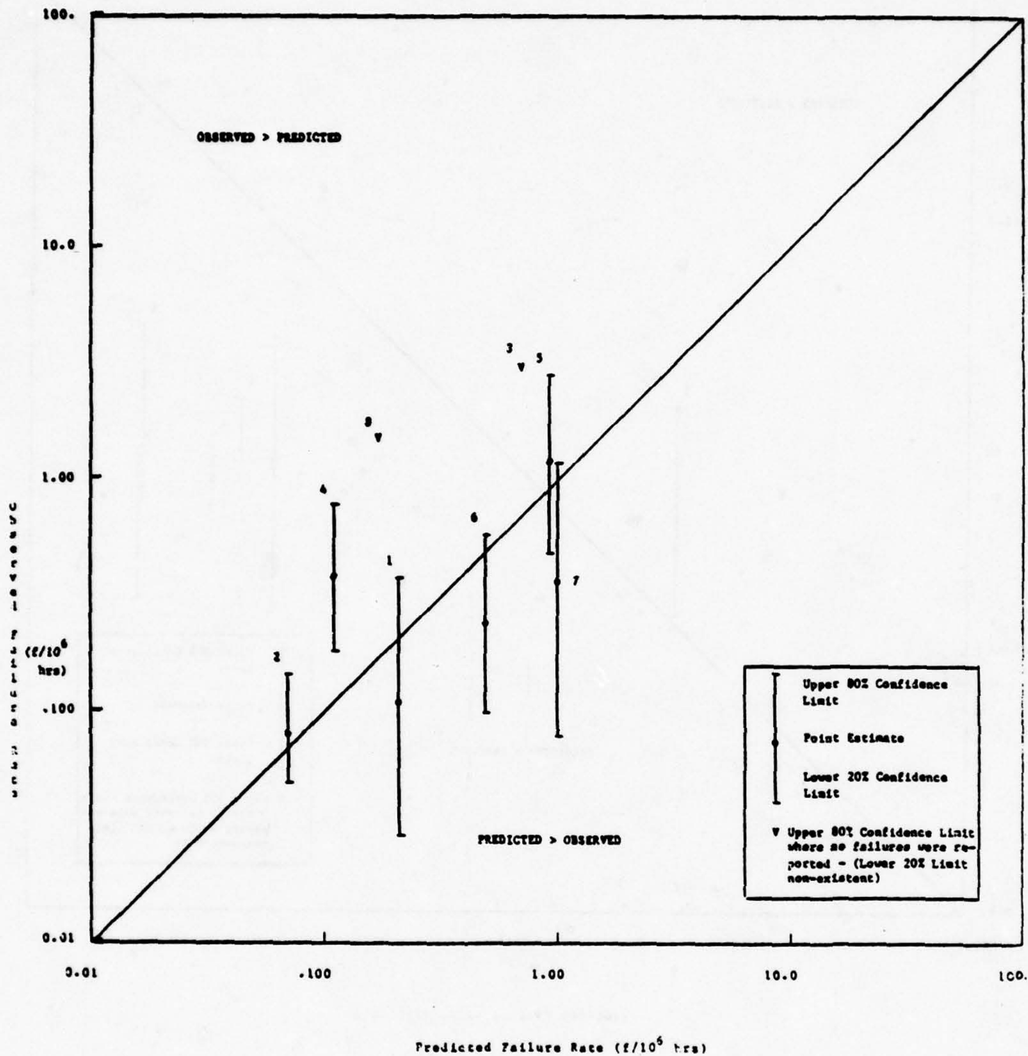


Figure 10: ROM and PROM Observed Failure Rates vs. Proposed Model Predicted Failure Rates

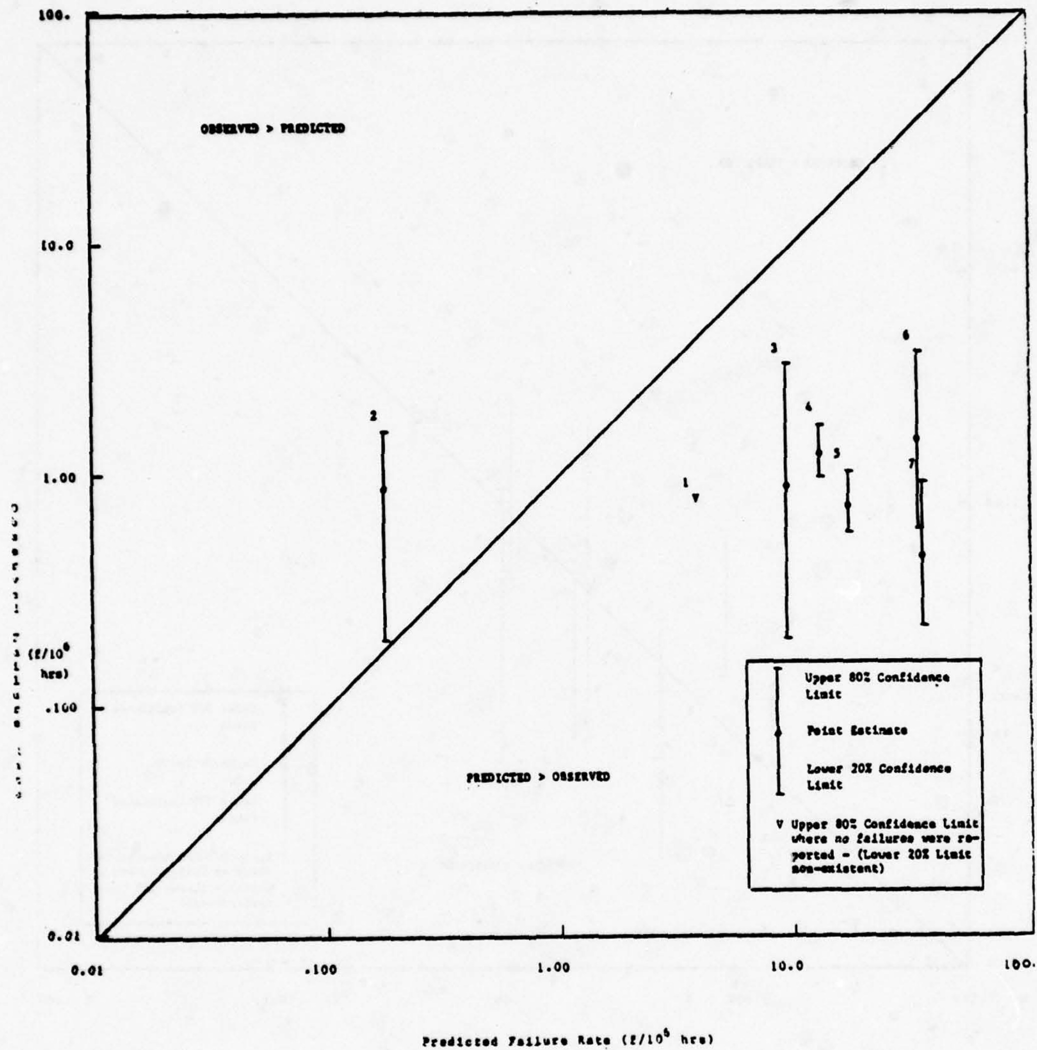


Figure 11: Random Logic LSI Device Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates

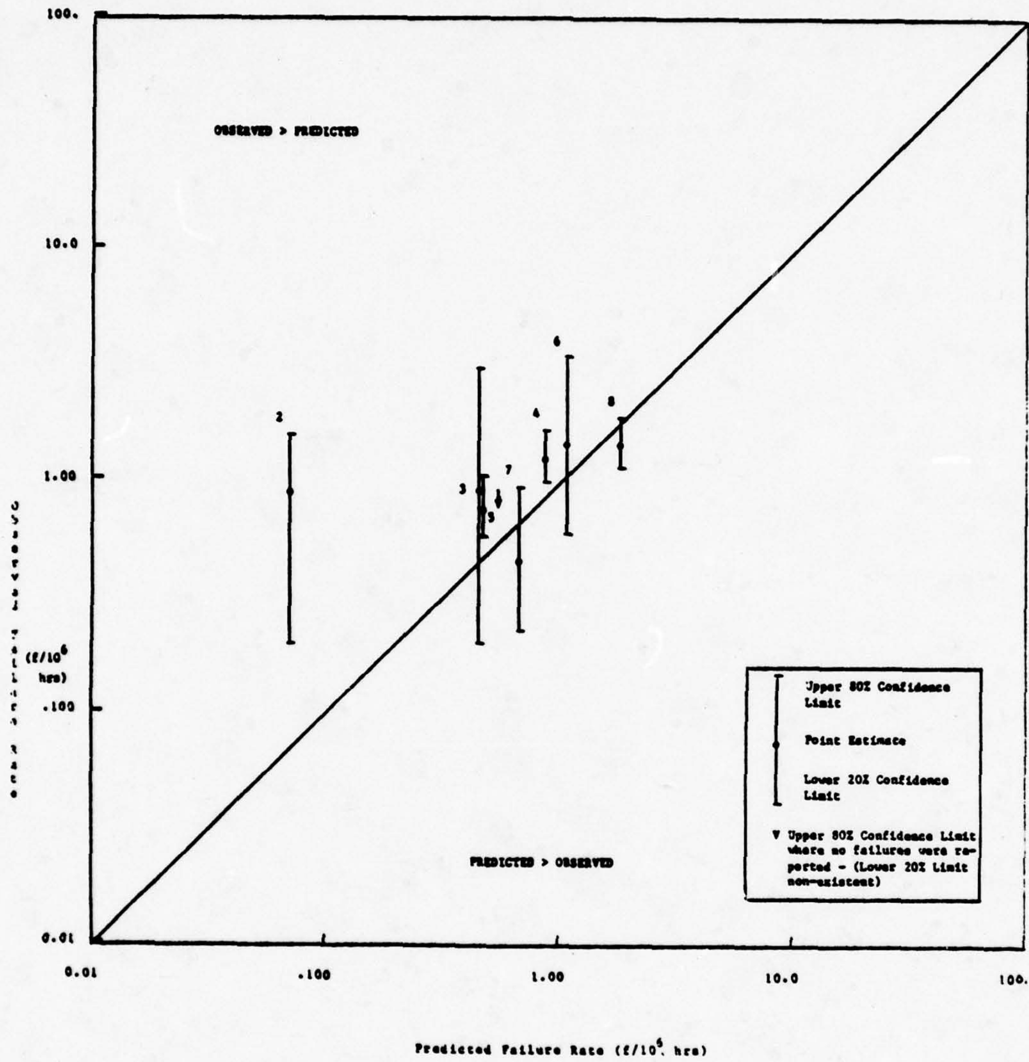


Figure 12: Random Logic LSI Device Observed Failure Rates vs. Proposed Model Predicted Failure Rates

Section 7

CONCLUSIONS AND RECOMMENDATIONS

A comparison of the failure rate predictions calculated using MIL-HDBK-217B, Notice II, and actual observed failure rates for LSI random logic and memory devices did not indicate a reasonable correlation between these values. An analysis of the 217B models revealed that the degree of correlation was attributable to the generic consolidation of model parameters, which ultimately reduced model sensitivity to several critical reliability factors. It was found that the model accuracy could be greatly improved, without substantially increasing model complexity, by dividing each of the generic parameters into a set of more detailed parameters, thereby more adequately reflecting the variation of the reliability sensitive attributes within each parameter.

The major model revisions included:

- Development of complexity factors for:
  - Bipolar RAMs and Shift Registers
  - MOS Dynamic RAMs and Shift Registers
  - MOS Static RAMs and Shift Registers
  - Bipolar ROMs and PROMs
  - MOS ROMs and PROMs
  - Bipolar Random Logic LSI
  - MOS Random Logic LSI.
- Development of temperature factors for each device technology, in both hermetic and nonhermetic packages.
- Introduction of an additive package failure rate factor based upon package type and number of functional package pins.
- Introduction of a voltage derating stress factor for CMOS devices with maximum recommended operating supply voltage greater than 12 volts.
- Introduction of a ROM and PROM programming technique factor to reflect the influence of the programming mechanism employed in these devices.

- Modification of device quality factors.

- Modification of application environment factors.

The models proposed in this study possess all those qualities common to practical reliability assessment techniques. The expressions are relatively simple and allow for consideration of evolving fabrication techniques, or emerging technologies, through the modification of the temperature factors. The factors exhibit the appropriate discriminations against the device design and usage attributes which contribute to known failure mechanisms. Additionally, each of the models, as illustrated in Section 6, demonstrates reasonable accuracy over the total range of parameters considered in these techniques.

Appendix 1

PROPOSED MODEL SAMPLE CALCULATIONS

APPENDIX 1

PROPOSED MODEL SAMPLE CALCULATIONS

EXAMPLE ONE

Description: An 8192 bit N-channel MOS UV-EPROM in a Ground, Fixed application, junction temperature of 55°C, procured to vendor equivalent B-2 quality level, in a ceramic/metal DIP, 24 pin.

From Section 2.1.4.2:

$$\lambda_P = \pi_Q \left\{ C_1 \pi_T \pi_V \pi_{PT} + (C_2 + C_3)\pi_E \right\}$$

Table 2.1.5-1 Quality Level B-2; $\pi_Q = 6.5$

Table 2.1.5-2 Ground, Fixed Environment; $\pi_E = 2.5$

Table 2.1.5-3 NMOS, Hermetic Package; corresponding to π_T Table 2.1.5-7; $\pi_T = 0.71$

Table 2.1.5-13 $\pi_V = 1.0$

Table 2.1.5-21 8192 bits; $C_1 = 0.055$, $C_2 = 0.0024$

Table 2.1.5-22 from equation 2 $\pi_{PT} = 1.56$

Table 2.1.5-23 24 pin Hermetic DIP solder seal; $C_3 = 0.009$

$$\lambda_p = 6.5 \left\{ (0.055)0.71(1.0)(1.56) + (0.0024 + 0.009)2.5 \right\}$$

$$\lambda_p = 6.5 \left\{ 0.061 + 0.029 \right\}$$

$$\lambda_p = 0.59/10^6 \text{ hours.}$$

EXAMPLE TWO

Description: Device type M38510/01801 is being used in an airborne inhabited, transport environment at 55°C ambient temperature. The device is procured as quality level B-2 and has been in continuous production. The device is in a hermetic C-DIP package.

The type number shows that the device is included in MIL-M-38510, described in slash sheet 18, type 01. The device is fabricated using TTL digital bipolar technology.

Table 2.1.5-25 shows a 100 gate complexity for this device. Since the device complexity is equal to 100 gates, the random logic LSI digital model in Section 2.1.3 applies. The failure rate equation is:

$$\lambda_p = \pi_Q \left\{ C_1 \pi_T \pi_V + (C_2 + C_3) \pi_E \right\}$$

Table 2.1.5-1 Quality Level B-2; $\pi_Q = 6.5$

Table 2.1.5-2 Airborne, Inhabited, Transport Environment, $\pi_E = 4.0$

Table 2.1.5-3 TTL, Hermetic Package; corresponding to π_T Table 2.1.54

$T_A = 55^oC$

$T_C = T_A + T_R = 55 + 20 = 75^oC$

$T_J = T_C + \Theta_{JC} P_{max} = 75 + 30(0.77) = 98^oC$

from Table 2.1.5-4; $\pi_T = 2.2$

Table 2.1.5-13 $\pi_V = 1.0$

Table 2.1.5-17 100 gate complexity; $C_1 = 0.015$, $C_2 = 0.0012$

Table 2.1.5-23 16 pin hermetic DIP, glass seal; $C_3 = 0.0059$

$$\lambda_p = 6.5 \left\{ (0.015)2.2(1.0) + (0.0012 + 0.0059)4.0 \right\}$$

$$\lambda_p = 6.5 \left\{ 0.033 + 0.028 \right\}$$

$$\lambda_p = 0.40/10^6 \text{ hrs.}$$

Appendix 2

PROPOSED SSI/MSI DIGITAL AND LINEAR MODELS

2.1.1 Monolithic Bipolar and MOS Digital SSI/MSI Devices (less than 100 gates).

$$\lambda_P = \pi_Q \left\{ C_1 \pi_T \pi_V + (C_2 + C_3)\pi_E \right\}$$

where:

λ_P is the device failure rate in $F/10^6$ Hours

π_Q is the quality factor, Table 2.1.5-1

π_T is the temperature acceleration factor, based on technology (Table 2.1.5-3) and is found in Tables 2.1.5-4 thru 2.1.5-12

π_V is the voltage derating stress factor, Table 2.1.5-13

π_E is the application environment factor, Table 2.1.5-2

C_1 & C_2 are the circuit complexity failure rates based upon gate count and are found in Tables 2.1.5-14 and 2.1.5-15. (See Tables 2.1.5-24 and 2.1.5-25 for gate count determination)

C_3 is the package complexity failure rate, Table 2.1.5-23.

2.1.2 Monolithic Bipolar and MOS Linear Devices

$$\lambda_P = \pi_Q \left\{C_1 \pi_T \pi_V + (C_2 + C_3)\pi_E\right\}$$

where:

λ_P is the device failure rate in $F/10^6$ Hours

π_Q is the quality factor, Table 2.1.5-1

π_T is the temperature acceleration factor, based on technology (Table 2.1.5-3) and is found in Tables 2.1.5-4 thru 2.1.5-12

π_V is the voltage derating stress factor, Table 2.1.5-13

π_E is the application environment factor, Table 2.1.5-2

C_1 & C_2 are circuit complexity failure rates based upon transistor count and are found in Table 2.1.5-16

C_3 is the package complexity failure rate, Table 2.1.5-23.

TABLE 2.1.5-14. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR BIPOLAR SSI/MSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
1	0.0007	0.0002	22	0.0056	0.0007	44	0.0089	0.0009
2	0.0012	0.0003	24	0.0060	0.0007	46	0.0091	0.0009
4	0.0019	0.0004	26	0.0063	0.0007	48	0.0094	0.0009
6	0.0024	0.0004	28	0.0066	0.0007	50	0.0097	0.0009
8	0.0029	0.0005	30	0.0069	0.0008	55	0.0103	0.0009
10	0.0034	0.0005	32	0.0072	0.0008	60	0.0109	0.0010
12	0.0038	0.0005	34	0.0075	0.0008	65	0.0115	0.0010
14	0.0042	0.0006	36	0.0078	0.0008	70	0.012	0.0010
16	0.0046	0.0006	38	0.0081	0.0008	80	0.013	0.0011
18	0.0050	0.0006	40	0.0083	0.0008	90	0.014	0.0011
20	0.0053	0.0007	42	0.0086	0.0009	99	0.015	0.0012

Tabulated values are derived from the following equations:

$$C_1 = 7.48 \times 10^{-4} (N_G)^{0.654}$$

$$C_2 = 2.19 \times 10^{-4} (N_G)^{0.364}$$

where N_G is the number of gates.

TABLE 2.1.5-15. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR MOS SSI/MSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
1	0.0022	0.0003	22	0.0065	0.0005	44	0.0084	0.0006
2	0.0028	0.0004	24	0.0067	0.0005	46	0.0085	0.0006
4	0.0036	0.0004	26	0.0069	0.0006	48	0.0086	0.0006
6	0.0041	0.0004	28	0.0071	0.0006	50	0.0088	0.0006
8	0.0046	0.0005	30	0.0073	0.0006	55	0.0091	0.0006
10	0.0049	0.0005	32	0.0075	0.0006	60	0.0094	0.0006
12	0.0053	0.0005	34	0.0076	0.0006	65	0.0096	0.0007
14	0.0057	0.0005	36	0.0078	0.0006	70	0.010	0.0007
16	0.0058	0.0005	38	0.0080	0.0006	80	0.010	0.0007
18	0.0061	0.0005	40	0.0081	0.0006	90	0.011	0.0007
20	0.0063	0.0005	42	0.0082	0.0006	99	0.011	0.0007

Tabulated values are derived from the following equations:

$$C_1 = 2.17 \times 10^{-3} (N_G)^{0.357}$$

$$C_2 = 3.11 \times 10^{-4} (N_G)^{0.178}$$

where N_G is the number of gates.

TABLE 2.1.5-16. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR LINEAR DEVICES IN FAILURES PER 10^6 HOURS

No. Trans.	C_1	C_2	No. Trans.	C_1	C_2	No. Trans.	C_1	C_2
4	0.0046	0.0017	64	0.040	0.0074	148	0.077	0.0116
8	0.0079	0.0024	68	0.042	0.0076	156	0.081	0.0119
12	0.011	0.0030	72	0.044	0.0079	164	0.084	0.0122
16	0.014	0.0035	76	0.046	0.0081	172	0.087	0.0126
20	0.016	0.0040	80	0.048	0.0083	180	0.090	0.0129
24	0.019	0.0044	84	0.050	0.0086	188	0.093	0.0132
28	0.021	0.0048	88	0.052	0.0088	196	0.096	0.0135
32	0.023	0.0051	92	0.053	0.0090	204	0.099	0.0138
36	0.026	0.0054	96	0.055	0.0092	220	0.105	0.0143
40	0.028	0.0058	100	0.057	0.0094	236	0.111	0.0149
44	0.030	0.0061	108	0.061	0.0098	252	0.117	0.0154
48	0.032	0.0063	116	0.064	0.0102	268	0.123	0.0159
52	0.034	0.0066	124	0.067	0.0105	284	0.129	0.0164
56	0.036	0.0069	132	0.071	0.0109	300	0.134	0.0169
60	0.038	0.0072	140	0.074	0.0113			

The tabulated values are derived from the following equations:

$$C_1 = 1.57 \times 10^{-3} (N_T)^{0.780}$$

$$C_2 = 8.00 \times 10^{-4} (N_T)^{0.535}$$

where N_T is the number of transistors.

DIGITAL SSI/MSI DATA

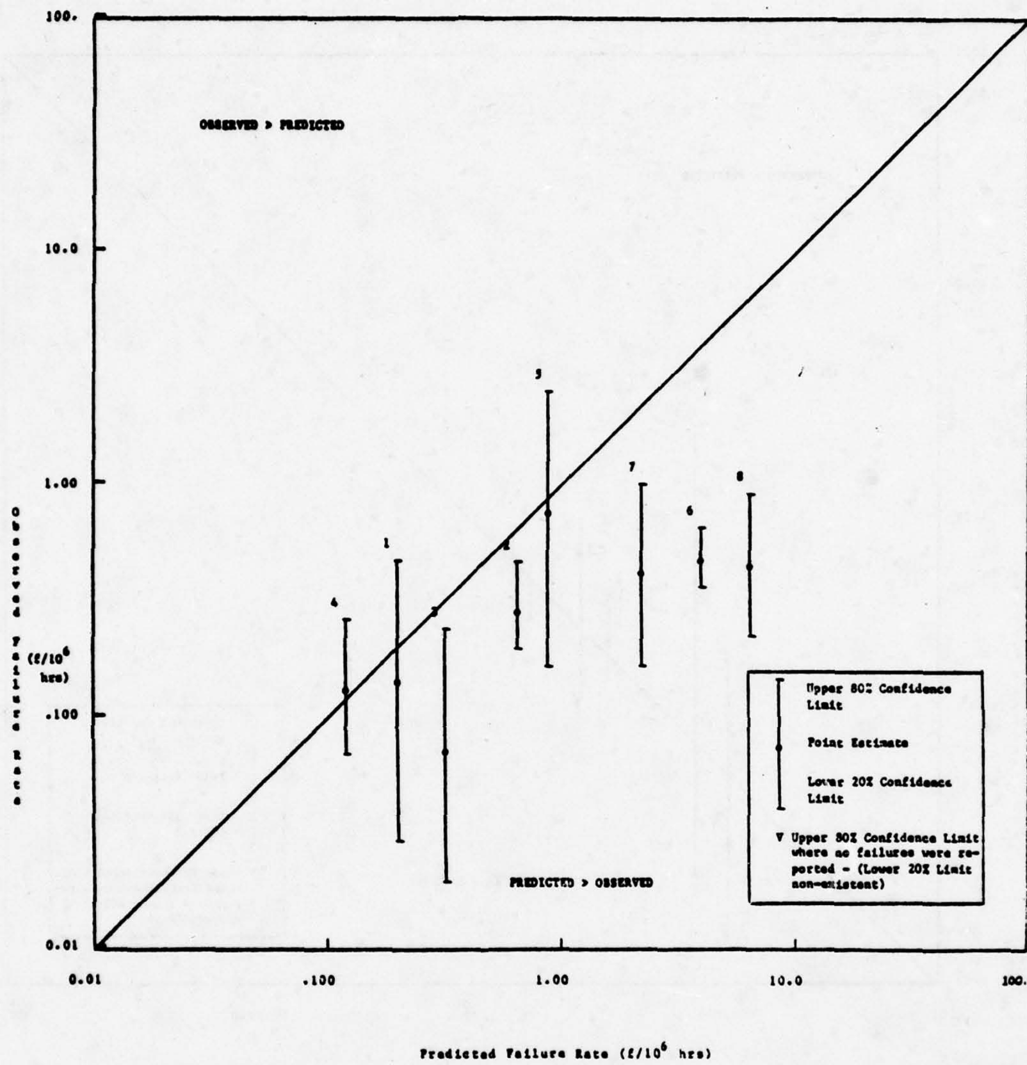
Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Gate Complexity	Package	No. Pins	T_j (°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	TTL	2	C-DIP	12	27	B-2	NS	6.940	1	0.03	0.14	0.43	0.20	0.11
2	CMOS	3	E-DIP	14	40	D	GB	28.568	8	0.20	0.28	0.42	0.65	0.26
3	TTL	6	FPK.	12	60	B-2	AIT	13.400	1	0.02	0.07	0.22	0.32	0.08
4	LTTL	12	C-DIP	12	51	B-2	GF	23.077	3	0.07	0.13	0.24	0.12	0.08
5	ECL	16	C-DIP	14	42	D	GB	1.340	1	0.17	0.75	2.23	0.88	0.11
6	TTL	20	E-DIP	14	40	D	GF	36.400	17	0.37	0.47	0.59	3.95	0.56
7	PMOS	26	PL-DIP	16	41	D	GB	4.713	2	0.17	0.42	0.91	2.22	0.34
8	CMOS	79	PL-DIP	16	48	D	GB	6.630	3	0.23	0.45	0.83	6.47	0.66

*Predictions Using Notice II Dated 17 March 1978.

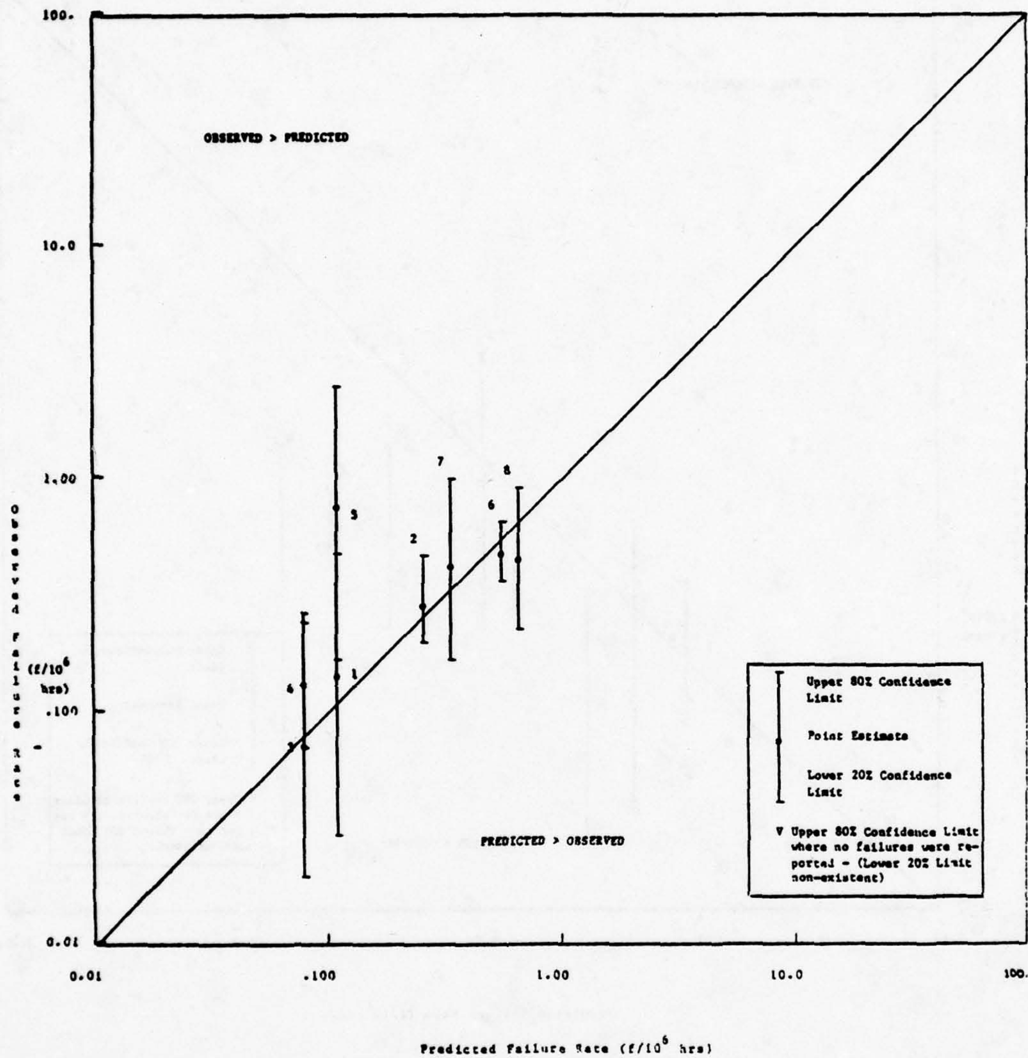
LINEAR DEVICE DATA

Device Description				Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Number Of Transistors	Package	No. Pins	T_j (°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	4	FPK	6	50	S	GB	422.300	1	0.0005	0.0024	0.0071	0.0024	0.0029
2	5	FPK	8	43	S	GB	1159.500	6	0.0034	0.0052	0.0078	0.0022	0.0028
3	11	CAN	10	67	D	GB	7.591	2	0.11	0.26	0.56	1.82	0.51
4	19	CAN	3	65	D	GB	26.427	15	0.44	0.57	0.73	2.38	0.63
5	22	CAN	6	51	D	GB	388.093	88	0.21	0.23	0.25	1.21	0.33
6	24	C-DIP	14	44	B-2	GF	7.811	5	0.40	0.64	1.01	0.18	0.21
7	34	C-DIP	12	35	D	GM	3.632	1	0.06	0.28	0.82	11.10	0.74
8	40	CAN	8	69	B-2	GB	42.414	10	0.17	0.24	0.32	0.35	0.52

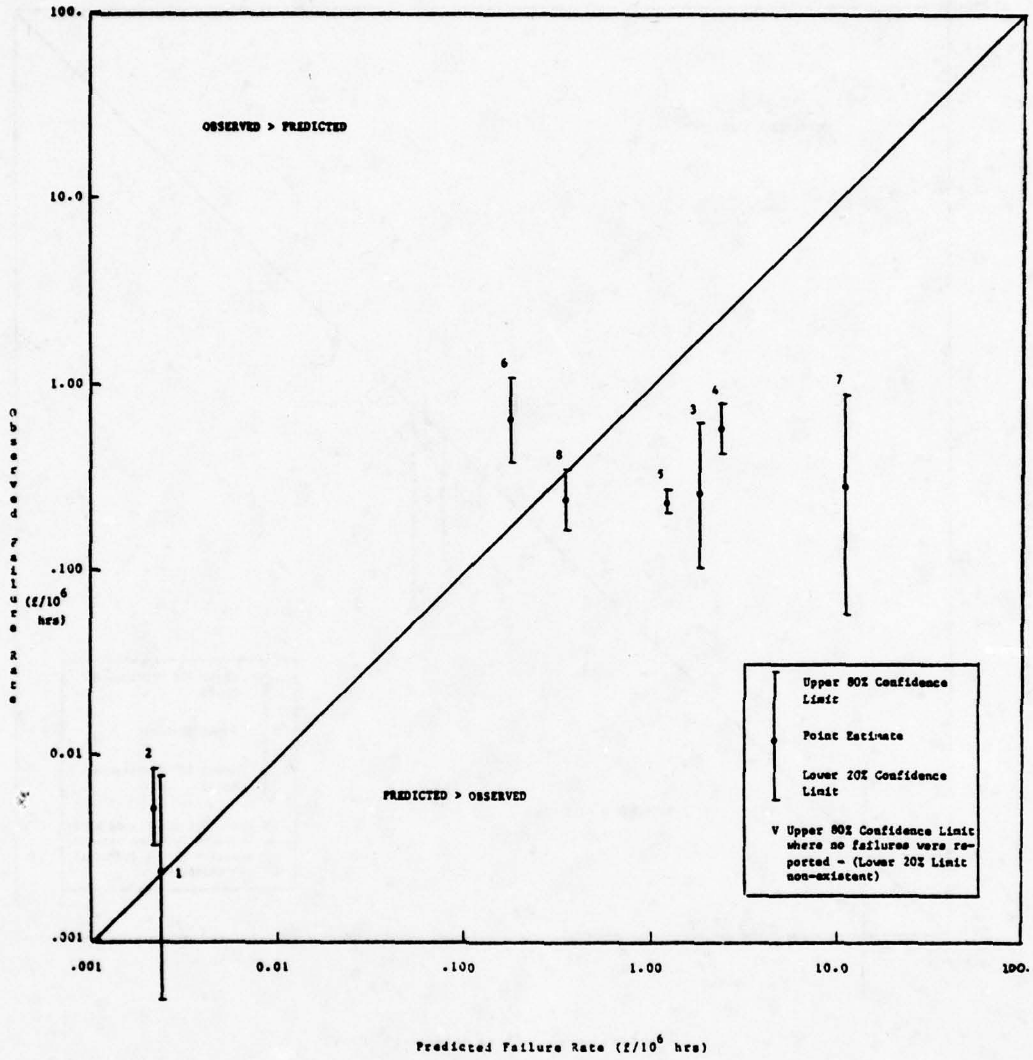
*Predictions Using Notice II Dated 17 March 1978.



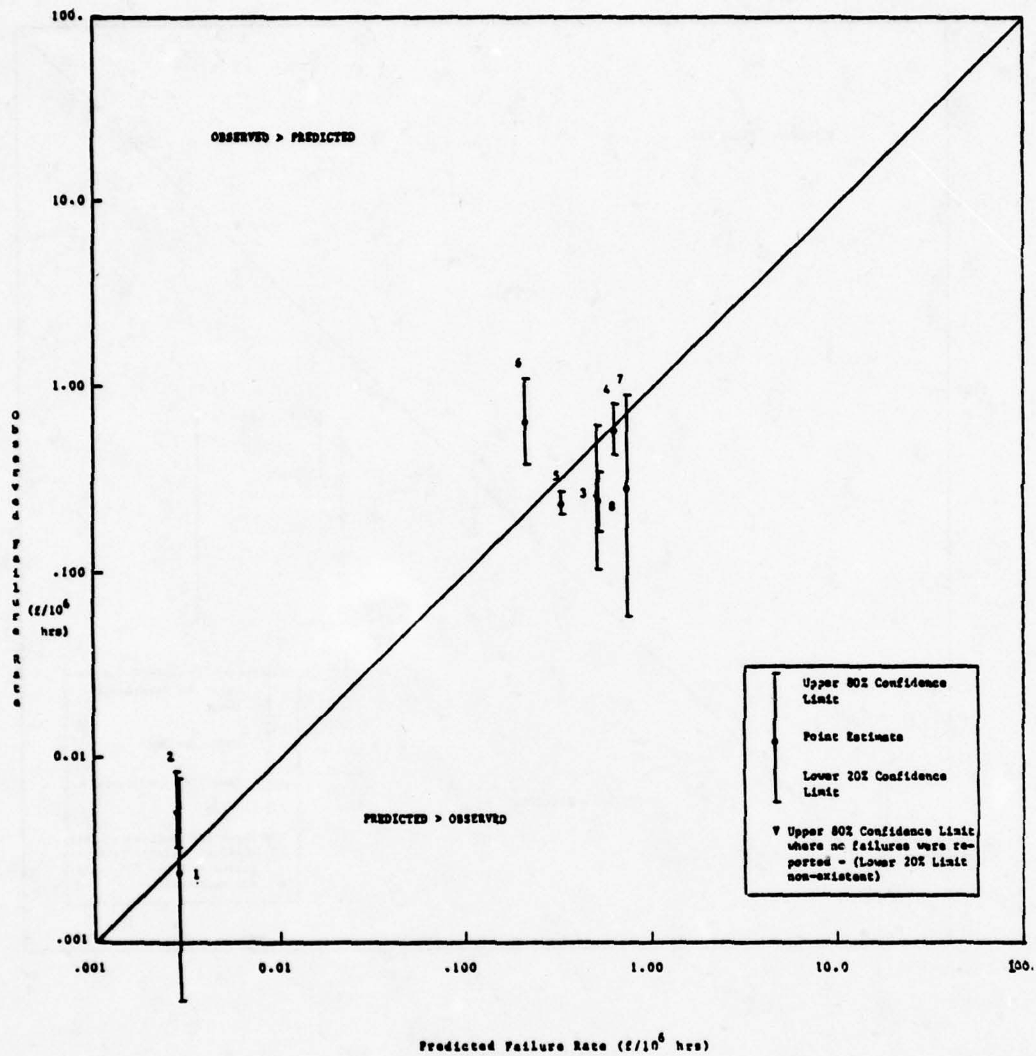
SSI/MSI Digital Device Observed Failure Rates vs. MIL-HDBK-217B Predicted Failure Rates



SSI/MSI Digital Device Observed Failure Rates vs. Proposed Model Predicted Failure Rates



Linear Device Observed Failure Rates vs. MIL-HDBK-217B
Predicted Failure Rates



Linear Device Observed Failure Rates vs. Proposed Model Predicted Failure Rates

Appendix 3

COMPLEXITY VALUE TABLES FOR
MIL-M-38510 DEVICE TYPES

TABLE 2.1.5-24. GATE, BIT & TRANSISTOR COUNT FOR COMMERCIAL TYPE INTEGRATED CIRCUITS AND CROSS-REFERENCE TO MIL-M-38510 TYPE

Commercial Type	M38510/ XXXXX	No. Trans.
LINEAR		
710	10301	9
711	10302	18
723	10201	20
741	10101	23
747	10102	46
DTL		No. Gates
930	03001	2
932	03101	2
933	03105	2
935	03002	6
936	03003	6
940	03002	6
944	03102	2
945	03301	8
946	03004	4
948	03302	8
950	03303	8
951	03201	6
957	03103	4
958	03104	4
962	03005	3
CMOS		
4000A	05201	3
4001A	05202	4
4002A	05203	2
4006A	05701	109
4007A	05301	3
4008A	05401	58
4009A	05501	6
4010A	05502	6
4011A	05001	6
4012A	05002	5
4013A	05101	24
4014A	05702	55
4015A	05703	58
4017A	05601	47
4018A	05602	57
4019A	05302	12
4020A	05603	132

Commercial Type	M38510/ XXXXX	No. Gates
CMOS		
4021A	05704	55
4022A	05604	39
4023A	05003	3
4024A	05605	81
4025A	05204	3
4027A	05102	30
4030A	05303	4
4031A	05705	263
4041A	05505	12
4049A	05503	6
NMOS RAM		No. BITS
4050	23501	4096
CMOS		No. Gates
4050A	05504	6
TTL		
5400	00104	4
5401	00107	4
5402	00401	4
5403	00109	4
5404	00105	6
5405	00108	6
5406	00801	6
5407	00803	6
5408	01601	4
5409	01602	4
5410	00103	3
5412	00106	3
5413	15101	2
5414	15102	6
5416	00802	6
5417	00804	6
5420	00102	2
5423	00402	2
5425	00403	2
5426	00805	4
5427	00404	3
5430	00101	1

TABLE 2.1.5-24. GATE, BIT & TRANSISTOR COUNT FOR COMMERCIAL TYPE INTEGRATED CIRCUITS AND CROSS-REFERENCE TO MIL-M-38510 TYPE (CONT'D)

Commercial Type	M38510/ XXXXX	No. Gates
TTL		
5437	00302	4
5438	00303	4
5440	00301	2
5442	01001	18
5443	01002	18
5444	01003	18
5445	01004	18
5446	01006	44
5447	01007	44
5448	01008	37
5449	01009	34
5450	00501	6
5451	00502	6
5453	00503	5
5454	00504	5
5470	00206	11
5472	00201	8
5473	00202	16
5474	00205	12
5475	01501	24
5476	00204	16
5477	01502	24
5479	00207	12
5482	00601	21
5483	00602	36
5485	15001	31
5486	00701	4
5490	01307	15
5492	01301	26
5493	01302	25
5495	00901	37
5496	00902	39
BIPOLAR PROM		No. BITS
5531	23001	256
LINEAR		No. Trans.
7831	10406	60
7832	10407	60

Commercial Type	M38510/ XXXXX	No. Gates
TTL		
8250	15204	15
8251	15205	18
8252	15206	18
DTL		
9093	03304	16
TTL		
9300	15901	40
9301	15206	18
9304	00603	22
9308*	01503	56
9309	01404	16
9311*	15201	25
9312	01402	17
9314	01504	26
9317	15802	46
9321	15801	18
9322	01405	19
9324	15002	32
9328	15902	72
9334	16001	59
9338	15701	98
9341*	01101	63
9342	01102	19
9382	00601	21
9383	00602	36
9601	01204	8
9602	01205	14
LINEAR		No. Trans.
9614	10403	40
9615	10404	35
ECL		No. Gates
10501	06001	4
10502	06002	4
10505	06003	3
10506	06004	3

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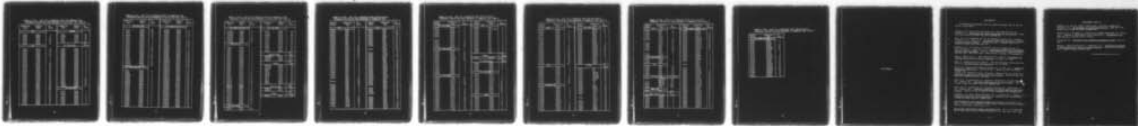

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TABLE 2.1.5-24. GATE, BIT & TRANSISTOR COUNT FOR COMMERCIAL TYPE INTEGRATED CIRCUITS AND CROSS-REFERENCE TO MIL-M-38510 TYPE (CONT'D)

Commercial Type	M38510/ XXXXX	No. Gates	Commercial Type	M38510/ XXXXX	No. Trans.
ECL			LINEAR		
10507	06005	3	55107	10401	29
10509	06006	2	55108	10402	25
10531	06101	24	55113	10405	46
10535	06104	24	55114	10403	40
10576	06103	42	55115	10404	35
10631	06102	24			No. Gates
TTL			TTL HIGH SPEED		
54107	00203	16	54H00	02304	4
54116*	01503	56	54H01	02306	4
54121	01201	8	54H04	02305	6
54122	01202	10	54H08	15501	4
54123	01203	20	54H10	02303	3
54125	15301	4	54H11	15502	3
54126	15302	4	54H20	02302	2
54132	15103	4	54H21	15503	2
54145	01005	18	54H22	02307	2
54150*	01401	26	54H30	02301	1
54151	01406	17	54H40	02401	2
54153	01403	16	54H50	04001	6
54154*	15201	25	54H51	04002	6
54155	15202	15	54H53	04003	5
54156	15203	15	54H54	04004	5
54157	01405	19	54H55	04005	3
54160	01303	60	54H72	02201	8
54161	01306	57	54H73	02202	16
54162	01305	60	54H74	02203	12
54163	01304	58	54H76	02204	16
54164	00903	36	54H101	02205	10
54165	00904	62	54H103	02206	12
54170	01801	100	TTL LOW POWER		
54174	01701	36			
54175	01702	24	54L00	02004	4
54180	01901	14	54L01	02006	4
54181*	01101	63	54L02	02701	4
54182	01102	19	54L03	02006	4
54192	01308	50	54L04	02005	6
54193	01309	48	54L10	02003	3
54194	00905	47	54L20	02002	2
54195	00906	41	54L30	02001	1

TABLE 2.1.5-24. GATE, BIT & TRANSISTOR COUNT FOR COMMERCIAL TYPE INTEGRATED CIRCUITS AND CROSS-REFERENCE TO MIL-M-38510 TYPE (CONT'D)

Commercial Type	M38510/ XXXXX	No. Gates
TTL LOW POWER		
54L42	02901	18
54L43	02902	18
54L44	02903	18
54L46	02904	44
54L47	02905	44
54L51	04101	6
54L54	04102	5
54L55	04103	3
54L71	02101	8
54L72	02102	8
54L73	02103	14
54L74	02105	12
54L78	02104	16
54L86	02601	4
54L90	02501	15
54L93	02502	25
54L95	02801	37
54L121	04201	8
54L122	04202	10
54L164	02802	36
54L193	02503	48
LOW POWER SCHOTTKY TTL		
9LS51	30401	6
9LS54	30402	5
54LS00	30001	4
54LS02	30301	4
54LS03	30002	4
54LS04	30003	6
54LS05	30004	6
54LS08	31004	4
54LS10	30005	3
54LS11	31001	3
54LS12	30006	3
54LS13	31301	2
54LS14	31002	6
54LS15	31002	3
54LS20	30007	2
54LS21	31003	2
54LS22	30008	2
54LS27	30302	3
54LS30	30009	1
54LS32	30501	4
54LS37	30202	4
LOW POWER SCHOTTKY TTL		
54LS38	30203	4
54LS40	30201	2
54LS42	30703	18
54LS47	30704	44
54LS51	30401	6
54LS54	30402	5
54LS73	30101	16
54LS74	30102	12
54LS75	31601	24
54LS83A	31201	36
54LS85	31101	31
54LS86	30502	4
54LS90	31501	15
54LS93	31502	25
54LS95	30603	37
54LS96	30604	39
54LS107	30108	16
54LS109	30109	16
54LS112	30103	16
54LS113	30104	16
54LS114	30105	16
54LS123	31401	20
54LS132	31303	4
54LS138	30701	16
54LS139	30702	18
54LS151	30901	17
54LS153	30902	16
54LS157	30903	19
54LS158	30904	15
54LS160	31503	60
54LS161	31504	57
54LS164	30605	36
54LS168	31505	63
54LS169	31506	60
54LS174	30106	36
54LS175	30107	24
54LS181*	30801	63
54LS192	31507	50
54LS193	31508	48
54LS194	30601	47
54LS195	30602	41
54LS221	31402	16
54LS251	30905	17
54LS253	30908	16

TABLE 2.1.5-24. GATE, BIT & TRANSISTOR COUNT FOR COMMERCIAL TYPE INTEGRATED CIRCUITS AND CROSS-REFERENCE TO MIL-M-38510 TYPE (CONT'D)

Commercial Type	M38510/ XXXX	No. Gates
LOW POWER SCHOTTKY TTL		
54LS257	30906	15
54LS258	30907	15
54LS266	30303	4
54LS279	31602	8
54LS283	31202	36
54LS295	30606	48
54LS395	30607	48
SCHOTTKY TTL		
54S00	07001	4
54S02	07301	4
54S03	07002	4
54S04	07003	6
54S05	07004	6
54S10	07005	3
54S11	08001	3
54S15	08002	3
54S20	07006	2
54S22	07007	2
54S30	07008	1
54S40	07201	2
54S51	07401	6
54S64	07402	5
54S65	07403	5
54S74	07101	12
54S85	08201	31
54S86	07501	4
54S112	07102	16
54S113	07103	16
54S114	07104	16
54S133	07009	1
54S134	07010	1
54S135	07502	8
54S140	08101	2
54S151	07901	17
54S153	07902	16
54S157	07903	15
54S158	07904	15
54S174	07105	36
54S175	07106	24
54S251	07905	17
54S257	07906	15
54S258	07907	15
TTL LOW POWER		
76L42A	02906	18
76L70	02805	36

Commercial Type	M38510/ XXXXX	No. Gates
TTL LOW POWER		
93L00	02804	40
93L01	02907	18
93L08*	04502	60
93L09	04601	16
93L10	02504	38
93L12	04602	17
93L14	04501	30
93L16	02505	58
93L18	04301	24
93L22	04603	19
93L24	04401	27
93L28	02803	72
BIPOLAR PROM		No. BITS
HYPROM512	20101	512
IM5603A	20201	1024
IM5623	20202	1024
LINEAR		No. Trans.
LH2101A	10105	42
LH2108A	10106	58
LM101A	10103	21
LM102	10601	19
LM106	10303	13
LM108A	10104	29
LM109	10701	19
LM110	10602	19
LM111	10304	23
LM118	10107	36
LM723	10201	20
BIPOLAR PROM		No. BITS
MCM5303	20101	512
MCM5304	20102	512
LINEAR		No. Trans.
MH0026	03501	18

TABLE 2.1.5-25. GATE, BIT & TRANSISTOR COUNT FOR MIL-M-38510 INTEGRATED CIRCUITS AND CROSS-REFERENCE TO COMMERCIAL TYPE

M38510/ XXXXX	Commercial Type	No. Gates	M38510/ XXXXX	Commercial Type	No. Gates
TTL			TTL		
00101	5430	1	01001	5442	18
00102	5420	2	01002	5443	18
00103	5410	3	01003	5444	18
00104	5400	4	01004	5445	18
00105	5404	6	01005	54145	18
00106	5412	3	01006	5446	44
00107	5401	4	01007	5447	44
00108	5405	6	01008	5448	37
00109	5403	4	01009	5449	34
00201	5472	10	01101*	54181	63
00202	5473	20		9341	63
00203	54107	20	01102	54182	19
00204	5476	20		9342	19
00205	5474	12	01201	54121	8
00206	5470	11	01202	54122	10
00207	5479	12	01203	54123	20
00301	5440	2	01204	9601	8
00302	5437	4	01205	9602	14
00303	5438	4	01301	5492	26
00401	5402	4	01302	5493	25
00402	5423	2	01303	54160	60
00403	5425	2	01304	54163	58
00404	5427	3	01305	54162	60
00501	5450	6	01306	54161	57
00502	5451	6	01307	5490	15
00503	5453	5	01308	54192	50
00504	5454	5	30109	54193	48
00601	5482	21	01401*	54150	26
	9382	21	01402	9312	17
00602	5483	36	01403	54153	16
	9383	36	01404	9309	16
00603	9304	22	01405	9322	19
00701	5486	4		54157	19
00801	5406	6	01406	54151	17
00802	5416	6	01501	5475	24
00803	5407	6	01502	5477	24
00804	5417	6	01503*	9308	56
00805	5426	4		54116	56
00901	5495	37	01504	9314	26
00902	5496	39	01601	5408	4
00903	54164	36	01602	5409	4
00904	54165	62	01701	54174	36
00905	54194	47	01702	54175	24
00906	54195	41	01801	54170	100
			01901	54180	14

TABLE 2.1.5-25. GATE, BIT & TRANSISTOR COUNT FOR MIL-M-38510 INTEGRATED CIRCUITS AND CROSS-REFERENCE TO COMMERCIAL TYPE (CONT'D)

M38510/ XXXXX	Commercial Type	No. Gates
TTL LOW POWER		
02001	54L30	1
02002	54L20	2
02003	54L10	3
02004	54L00	4
02005	54L04	6
02006	54L01	4
	54L03	4
02101	54L71	8
02102	54L72	8
02103	54L73	14
02104	54L78	16
02105	54L74	12
TTL HIGH SPEED		
02201	54H72	8
02202	54H73	16
02203	54H74	12
02204	54H76	16
02205	54H101	10
02206	54H103	12
02301	54H30	1
02302	54H20	2
02303	54H10	3
02304	54H00	4
02305	54H04	6
02306	54H01	4
02307	54H22	2
02401	54H40	2
TTL LOW POWER		
02501	54L90	15
02502	54L93	25
02503	54L193	48
02504	93L10	38
02505	93L16	58
02601	54L86	4
02701	54L02	4
02801	54L95	37
02802	54L164	36
02803	93L28	72
02804	93L00	40
02805	76L70	36
02901	54L42	18
02902	54L43	18
02903	54L44	18
02904	54L46	44
02905	54L47	44
02906	76L42A	18
02907	93L01	18

M38510/ XXXXX	Commercial Type	No. Gates
DTL		
03001	930	2
03002	935 & 940	6
03003	936	6
03004	946	4
03005	962	3
03101	932	2
03102	944	2
03103	957	4
03104	958	4
03105	933	2
03201	951	6
03301	945	8
03302	948	8
03303	950	8
03304	9093	16
LINEAR		No. Trans
03501	MH0026	18
TTL HIGH SPEED		No. Gates
04001	54H50	6
04002	54H51	6
04003	54H53	5
04004	54H54	5
04005	54H55	3
TTL LOW POWER		
04101	54L51	6
04102	54L54	5
04103	54L55	3
04201	54L121	8
04202	54L122	10
04301	93L18	24
04401	93L24	27
04501	93L14	30
04502*	93L08	60
04601	93L09	16
04602	93L12	17
04603	93L22	19
CMOS		
05001	4011A	6
05002	4012A	5
05003	4023A	3
05101	4013A	24
05102	4027A	30
05201	4000A	3
05202	4001A	4
05203	4002A	2

TABLE 2.1.5-25. GATE, BIT & TRANSISTOR COUNT FOR MIL-M-38510 INTEGRATED CIRCUITS AND CROSS-REFERENCE TO COMMERCIAL TYPE (CONT'D)

M38510/ XXXXX	Commercial Type	No. Gates
CMOS		
05204	4025A	3
05301	4007A	3
05302	4019A	12
05303	4030A	4
05401	4008A	58
05501	4009A	6
05502	4010A	6
05503	4049A	6
05504	4050A	6
05505	4041A	12
05601	4017A	47
05602	4018A	57
05603	4020A	132
05604	4022A	39
05605	4024A	81
05701	4006A	109
05702	4014A	55
05703	4015A	58
05704	4021A	55
05705	4031A	263
ECL		
06001	10501	4
06002	10502	4
06003	10505	3
06004	10506	3
06005	10507	3
06006	10509	2
06101	10531	24
06102	10631	24
06103	10576	42
06104	10535	24
SCHOTTKY TTL		
07001	54S00	4
07002	54S03	4
07003	54S04	6
07004	54S05	6
07005	54S10	3
07006	54S20	2
07007	54S22	2
07008	54S30	1
07009	54S133	1
07010	54S134	1
07101	54S74	12
07102	54S112	16
07103	54S113	16
07104	54S114	16

M38510/ XXXXX	Commercial Type	No. Gates
SCHOTTKY TTL		
07105	54S174	36
07106	54S175	24
07201	54S40	2
07301	54S02	4
07401	54S51	6
07402	54S64	5
07403	54S65	5
07501	54S86	4
07502	54S135	8
07901	54S151	17
07902	54S153	16
07903	54S157	15
07904	54S158	15
07905	54S251	17
07906	54S257	15
07907	54S258	15
08001	54S11	3
08002	54S15	3
08101	54S140	2
08201	54S85	31
LINEAR		No. Trans.
10101	741	23
10102	747	46
10103	LM101A	21
10104	LM108A	29
10105	LH2101A	42
10106	LH2108A	58
10107	LM118	36
10201	723	20
10301	710	9
10302	711	18
10303	LM106	13
10304	LM111	23
10401	55107	29
10402	55108	25
10403	9614	40
	55114	40
10404	9615	35
	55115	35
10405	55113	46
10406	7831	60
10407	7832	60
10601	LM102	19
10602	LM110	19
10701	LM109	19

TABLE 2.1.5-25. GATE, BIT & TRANSISTOR COUNT FOR MIL-M-38510 INTEGRATED CIRCUITS AND CROSS-REFERENCE TO COMMERCIAL TYPE (CONT'D)

M38510/ XXXXX	Commercial Type	No. Gates
TTL		
15001	5485	31
15002	9324	32
15101	5413	2
15102	5414	6
15103	54132	4
15201*	54154	25
	9311	25
15202	54155	15
15203	54156	15
15204	8250	15
15205	8251	18
15206	8252	18
	9301	18
15301	54125	4
15302	54126	4
TTL HIGH SPEED		
15501	54H08	4
15502	54H11	3
15503	54H21	2
TTL		
15701	9338	98
15801	9321	18
15802	9317	46
15901	9300	40
15902	9328	72
16001	9334	59
BIPOLAR PROM		No. Bits
20101	HYPROM512	512
	MCM5303	512
20102	MCM5304	512
20201	IM5603A	1024
20202	IM5623	1024
23001	5531	256
NMOS RAM		
23501	4050	4096
LOW POWER SCHOTTKY TTL		No. Gates
30001	54LS00	4
30002	54LS03	4
30003	54LS04	6
30004	54LS05	6
30005	54LS10	3
30006	54LS12	3
30007	54LS20	2

M38510/ XXXXX	Commercial Type	No. Gates
LOW POWER SCHOTTKY TTL		
30008	54LS22	2
30009	54LS30	1
30101	54LS73	16
30102	54LS74	12
30103	54LS112	16
30104	54LS113	16
30105	54LS114	16
30106	54LS174	36
30107	54LS175	24
30108	54LS107	20
30109	54LS109	16
30201	54LS40	2
30202	54LS37	4
30203	54LS38	4
30301	54LS02	4
30302	54LS27	3
30303	54LS266	4
30401	9LS51	6
	54LS51	6
30402	9LS54	5
	54LS54	5
30501	54LS32	4
30502	54LS86	4
30601	54LS194	47
30602	54LS195	41
30603	54LS95	37
30604	54LS96	39
30605	54LS164	36
30606	54LS295	48
30607	54LS395	48
30701	54LS138	16
30702	54LS139	18
30703	54LS42	18
30704	54LS47	44
30801*	54LS181	63
30901	54LS151	14
30902	54LS153	16
30903	54LS157	15
30904	54LS158	15
30905	54LS251	17
30906	54LS257	15
30907	54LS258	15
30908	54LS253	16
31001	54LS11	3

TABLE 2.1.5-25. GATE, BIT & TRANSISTOR COUNT FOR MIL-M-38510 INTEGRATED CIRCUITS AND CROSS-REFERENCE TO COMMERCIAL TYPE (CONT'D)

M38510/ XXXXX	Commercial Type	No. Gates
LOW POWER SCHOTTKY TTL		
31002	54LS15	3
31003	54LS21	2
31004	54LS08	4
31101	54LS85	31
31201	54LS83A	36
31202	54LS283	36
31301	54LS13	2
31302	54LS14	6
31303	54LS132	4
31401	54LS123	20
31402	54LS221	16
31501	54LS90	15
31502	54LS93	25
31503	54LS160	60
31504	54LS161	57
31505	54LS168	63
31506	54LS169	60
31507	54LS192	50
31508	54LS193	48
31601	54LS75	24
31602	54LS279	8

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