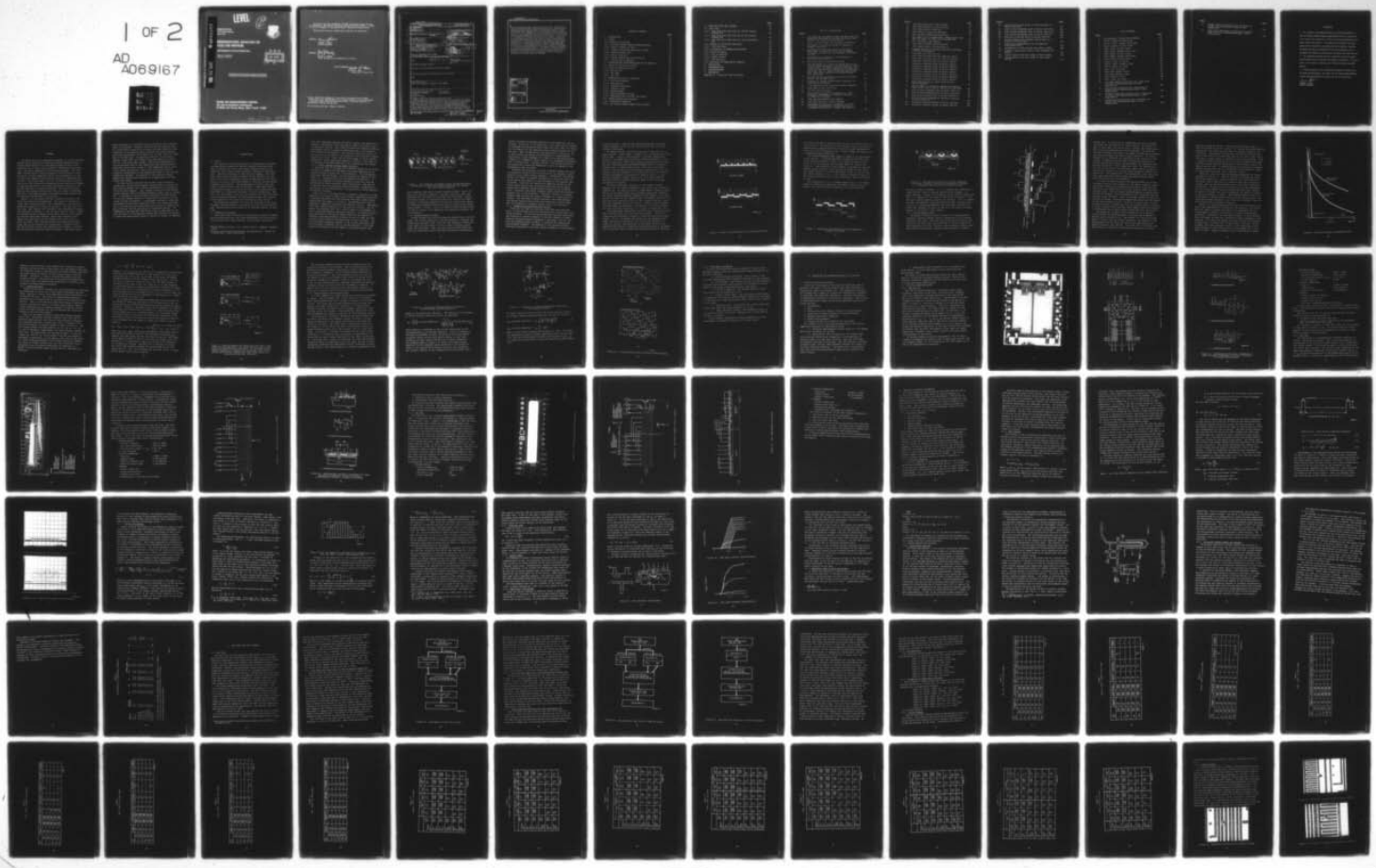
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DEGRADATION ANALYSIS OF CCD/CID DEVICES

RADC-TR-79-58
Final Technical Report
April 1979

DEGRADATION ANALYSIS OF CCD/CID DEVICES

WESTINGHOUSE ELECTRIC CORPORATION

John W. Dzimianski
Gerald M. Borsuk

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The growing use of Charge-Coupled Devices (CCD's) in systems for analog signal processing has generated a need to develop information on degradation mechanisms that affect CCD devices due to their structure and operation. The effort reported on in this report describes an experimental study of factors which influence the degradation of parameters and performance of analog charge coupled devices using accelerated stress techniques. Measured parameters included charge transfer efficiency, dark current density, Cont'd)

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full well capacity, dynamic range, and insertion loss. Test cells of a surface channel device and a buried channel device were temperature bias stressed for 1000 hours with parametric measurements taken at 0, 168, 500 and 1000 hours. Dynamic and d.c. stresses were applied to separate test cells at 125°C and 200°C. Electrical parameters of the devices were measured at room temperature with the precaution taken to cool the devices to room temperature before electrical stress was removed. The test results indicated that a basic trend towards increased dark current and decreased charge transfer efficiency in the p-surface channel CCD's can be attributed to an increase in interface state density. Also, dynamic stressing of the surface channel devices tends to degrade parameters faster than d.c. stressing. A decrease in charge transfer efficiency at 200°C stress for the buried channel devices is tentatively attributed to an increase in bulk trap density. Catastrophic failures of initially unscreened devices during temperature bias life tests indicated that a MIL-STD-883, Method 1015 burn-in screen would have been effective in removing the early failures from the population of unscreened devices. Tabulated test data and curves are presented.

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EVALUATION

1. This contract investigated the physics of failure mechanisms in bulk and surface channel charge coupled devices (CCD's), and was the first study of the reliability of CCD's utilizing accelerated environmental stress test methods. Its purpose was to identify and study unique failure mechanisms associated with CCD technology, determine the degree and cause of degradation of key CCD parameters, and to recommend test methods to evaluate lots and remove unreliable devices.

2. The information derived from this study will be used to update specifications and test methods (MIL-M-38510, MIL-STD-883). This will result in the ability to procure more reliable CCD and related MOS devices.

3. A paper presented at the International Symposium on Application of Charge Coupled Devices, San Diego, CA, Oct 1978 provided feedback to users and manufacturers on the key results of the contract.

Carmine J. Salvo

CARMINE J. SALVO
Project Engineer

SUMMARY

The objective of the "Degradation Analysis of CCD/CID Devices" program was to determine reliability problems associated with charge-coupled device (CCD) and charge-injection device (CID) technology due to their unique method of construction and operation. The study consisted of three distinct phases. The first phase involved device selection based on the structure of each device for a given technology family, the availability and cost of sufficient numbers of devices, and the device complexity and function. The second phase involved a detailed study of typical devices and the planning of experiments using accelerated stresses to identify potential factors whose degradation might be an important indicator of device reliability. The third and final phase of the program involved long term life tests to establish the casual relationship between the selected stress applied and the long term reliability of the devices.

Section 1 of the report provides a general overview of the CCD device structure and operation. The choice of devices for study, their characteristics, and a discussion of the electrical parameters measured is covered in section 2. The long term life test plan, test results, and analysis of the experimental results are presented in section 3. For the long term life tests, groups of 44-stage surface p-channel analog shift register CCD's (SCCD) and 455/910-stage bulk n-channel analog shift register CCD's (BCCD) were subjected to dc and dynamic electrical stress at 125°C and 200°C. The 44-stage devices were unscreened Westinghouse 7004 serial-in/serial-out 4-phase shift registers, while the 455/910-stage devices were commercially available. Fairchild CCD-321 serial-in/serial-out shift registers. The sample group

sizes consisted of 10 devices each for the SCCD's and 7 devices each for the BCCD's. However, each BCCD had two separate 455-bit analog shift registers on a single chip and, therefore, provided data on two separate shift registers per device package. Electrical measurements were taken at 0, 25, 168, 500, and 1,000 hours of stress time. An additional 500 hours of stress was applied to the 125°C dc n-channel BCCD test group for a total time of 1,500 hours under stress. Electrical measurements of the devices were made at room temperature with the precaution taken that devices were cooled to room temperature before electrical stress was removed. Also, initial and final sets of parametric measurements on the samples were made at low and high temperature extremes. As required in the contract, package ambient gas analysis was performed on a sample basis for each device type tested.

The test results indicated that a basic trend toward increased dark current and decreased charge transfer efficiency in the p-surface channel CCD's can be attributed to an increase in interface state density. Also, dynamic stressing of the surface channel devices tends to degrade parameters faster than dc stressing. A decrease in charge transfer efficiency at 200°C stress for the bulk channel devices is tentatively attributed to an increase in bulk trap density. Catastraphic failures of initially unscreened devices during temperature bias life tests indicated that a 168 hour burn-in screen would be effective in removing the early failures from the population of unscreened devices. Recommendation was made that additional study be undertaken to define the nature of the physical process that degrades CCD devices at 200°C when operational levels of electrical stress are applied.

1. INTRODUCTION

1.1 SCOPE

The objective of this program was to determine by analytical and experimental methods reliability problems associated with charge coupled device (CCD) and charge injection device (CID) technology due to their unique method of construction and operation. The study consisted of three distinct phases. The first phase involved device selection based on the structure of each device for a given technology family and applications, the availability and cost of sufficient numbers of devices, and the device complexity and function. The second phase involved a detailed study of typical devices and the planning of experiments using accelerated stresses to identify potential factors whose degradation might be an important indicator of device reliability. The third and final phase of the program involved long term life tests to statistically establish any relationship between the selected stress applied and the long term reliability of the devices.

The selection of devices for study, by direction of the work statement, gave preference to analog devices over digital devices. Also, imaging devices were ruled out as candidate devices in this study.

1.2 GENERAL CCD OVERVIEW

Since 1969, when the conceptual breakthrough needed for making CCD structures occurred, very rapid development and use of CCD devices has occurred. Many technical journal papers and books[1,2]

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[1]Charge Transfer Devices - C.H. Sequin and M.F. Tompsett, Academic Press.

[2]Charge-Coupled Devices; Technology and Application - Edited by R. Melen and D. Buss, IEEE Press.

have been published covering CCD theory, design, and application. However, information on CCD degradation modes and failure rates is generally lacking. This study initiated and funded by Rome Air Development Center is aimed at aleviating some of the dearth of CCD reliability information. The following pages of section 1.2 will provide an overview of the operational and structural characteristics of CCD's. There are two basic types of CCD's, surface channel CCD (SCCD) and buried channel CCD (BCCD). Also there is a variation on the BCCD referred to as a peristaltic CCD (PCCD).

1.2.1 Surface Channel Charge-Coupled Devices

The first type of CCD made was a surface channel device (SCCD). The SCCD is composed of overlapping electrodes deposited on an insulator which is grown over a semiconductor. The overlapping electrodes form and define a row of adjacent MOS capacitors (see figure 1). Conventionally, the semiconductor is silicon n- or p-type, the insulator is usually thermally grown SiO_2, and the electrodes are made from metal and/or polysilicon. The SCCD is a depletion mode CCD since the electrical charge, transported at the surface of the semiconductor, is confined to a region depleted of majority carriers.

Thus for an n- (p)-type silicon, a negative (positive) voltage applied to the gates at time t_o will create a depletion region and a confining potential well for the hole (electron) charge packet representing the signal. At time t_o, the potential well will be depleted of thermally generated free minority carrier. Subsequently, with time, thermal generation of the minority carriers, near or within the potential well, will collect within a 10 nanometer region of the semiconductor insulator interface. To prevent significant alteration of the signal charge packet by the addition of thermally generated minority carriers, we have to limit the time a signal charge packet is confined under a given electrode. The time confinement possible depends on the thermal generation rate or the thermal relaxation time of the MOS capacitor. With good quality bulk material and low number of interface states, the

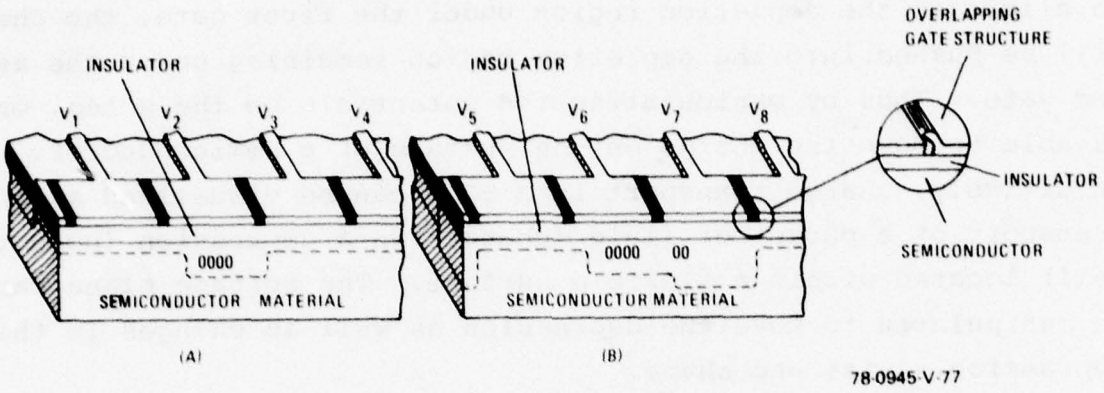


Figure 1. CCD Formed by Overlapping Gates and MOS Capacitors Defined by the Gates (A) During Integration and Storage, (B) During Charge Transfer

MOS relaxation time can be several hundred seconds. Hence, for short time intervals compared to the MOS relaxation time, the potential well can serve as a storage site for charge. However, the charge stored in any potential well will have to be transferred to a different potential well before a significant amount of thermally generated minority carriers are added to the signal charge packet. Clearly, a CCD is a dynamic charge storage device and charge transfer is an important and necessary ingredient for its operation.

1.2.2 Charge Transfer in SCCD

Charge transfer in a SCCD is caused by manipulating, with the gates, the surface potential of the semiconductor. Consider two gates which overlap in such a way that the depletion regions produced under each gate merge to form a single depletion region under the electrodes. Thus, any free charge located under one gate will distribute itself uniformily throughout the depletion

region, provided the surface potential in the depletion area is uniform. Similarly, if the potential on the first gate is changed to eliminate the depletion region under the first gate, the charge will be pushed into the depletion region remaining under the second gate. Thus by manipulating the potentials on the gates, one is able to move the charge on the surface of a semiconductor. Intuitively, charge transport in a SCCD can be visualized as the transport of a packet of fluid (charge) in a depression (potential well) located within a flexible surface. The surface plane can be manipulated to move the depression as well as changes in the depression's size and shape.

Extending the principle of charge transport between two gates to a periodic structure with many gates, we can transport charge packets across longer surface channels. Furthermore, with proper design, the number of packets transferred at any given time can be as many as the number of cells contained in the periodic gate structure. Each cell will permit the temporary storage of the charge packet and provide isolation between the stored charge packet and neighboring charge packets located in the different cells. Moreover, the charge transport within each cell should be possible only in one direction. Generally, the use of diffused channel stops confines the charge transport to a narrow and long channel. The electrode clocking structure, the clock phasing, and channel doping profile along the direction of charge transport are designed to transport charge only in one direction.

1.2.3 Transfer Electrode Structure in SCCD

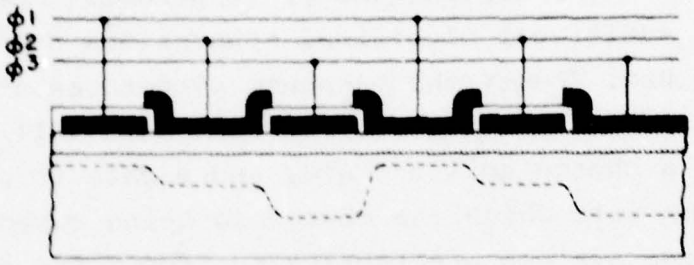
There are two types of electrode structures used with the SCCD, a nondirectional electrode structure and a directional electrode structure. In CCD with nondirectional electrode structures, the direction of charge transport in the SCCD channel is determined by the pulse-clocking sequence on the gates; that is, forward and backward charge transport is possible by changing the gate-clocking sequence. The geometry of CCD with directional electrode structures is such that charge transport is only possible

in one direction. Changing the clocking waveforms to promote charge transport in the reverse direction will not yield good transfer performance.

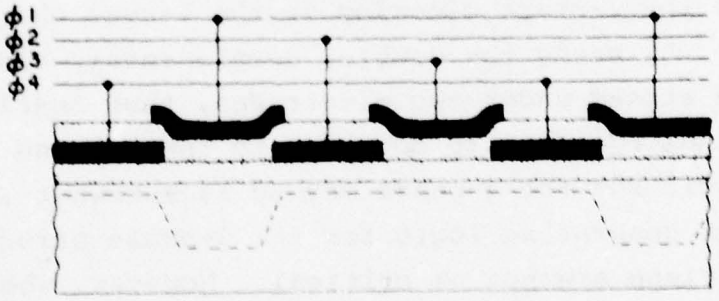
The nondirectional electrodes currently in use are 3- or 4-phase systems. Large number of phases (i.e., electrodes per cell) can be used. However, topologically, it becomes impractical, because of the additional electrical connections needed to form the gate structure. Fewer than 3-phase structures are not possible with nondirectional electrodes because each cell requires a blocking gate, a charge holding gate, and a gate to provide a depletion region into which the charge is being moved. The 3- or 4-phase electrode systems are fabricated from metal and/or polysilicon overlapping electrodes as is shown in figure 2. The clocking sequence normally employed is called push clocking characterized by a clocking sequence where at any given time, two phases are enabled.

The most significant advantages of the 4-phase clocking approach over the 3-phase clocking is the larger charge handling capabilities. By using the double, complementary clocking scheme, charge can be stored under two electrodes, thus nearly doubling the charge handling capacity compared to the 3-phase. The clock generation logic for the 4-phase method is somewhat less difficult than the clock generating logic for the 3-phase structure. Also, the clock overlaps are not as critical. However, when a 3-phase clocking scheme is employed, it is possible to fabricate smaller CCD cells with three gates per cell versus four gates per cell.

CCD's which have directional electrodes have the charge transport direction built into the electrode geometry. One or two clocks may be sufficient to operate a SCCD with directional electrodes. In a 2- or 1-phase gate structure, the depletion well under each gate is profiled so that the surface potential is higher at one end. The potential of the charge stored in the depletion well does not exceed the surface potential at the higher end of the well, hence an effective directional stop is obtained.



(a) THREE - PHASE



(b) FOUR - PHASE

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Figure 2. Three- and Four-Phase CCD Electrode Structures

The charge confined in the profiled CCD well can only be moved in one direction. The profiling of the potential well of an SCCD is possible with stepped-electrode structures or with implanted regions to provide a potential step. Figure 3 shows the geometry of a stepped-electrode structure.

The stepped potential well, shown in figure 4, is produced by an ion implant. A 1-phase operation is possible with the electrode structures shown in figure 3 or 4 when one phase is connected to an ac potential and the other phase is clocked (see figure 5). The potential on the dc phase is adjusted so that the highest potential level of the dc phase is equal or lower than the lowest potential of the clocked phase in the off states. And the lowest potential level of the dc phase is higher or equal to the highest potential level of the clocked well during the clock on time.

The advantages of a 1- or 2-phase system over a 3- or 4-phase system is smaller cell dimension and simpler clocking required. However, the charge handling capability is reduced with the

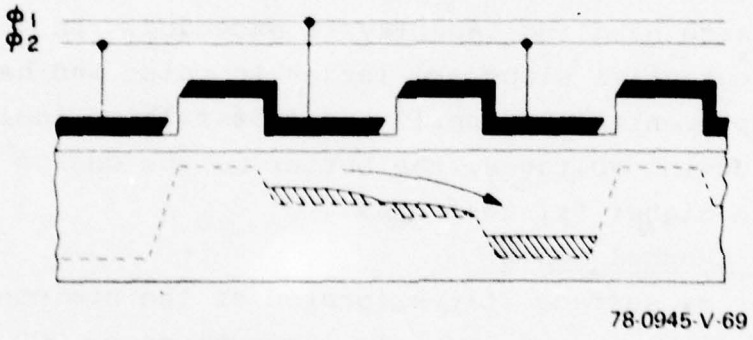


Figure 3. Two-Phase CCD Electrode Structure Employing Stepped Electrodes

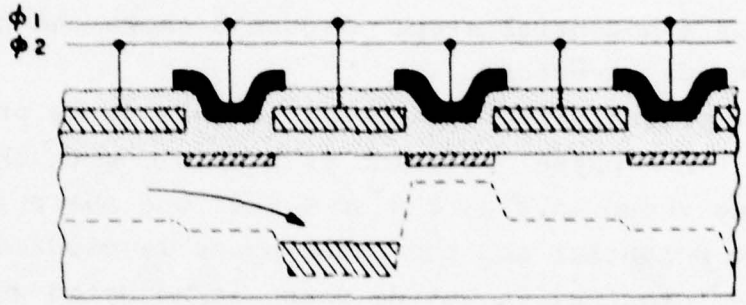


Figure 4. Two-Phase CCD Electrode Structure Employing Electrodes Connected in Pairs and an Implant to Produce a Potential Step Yielding a Profiled CCD Well

decreasing number of phases. In 3- or 4-phase gate structures, a larger dynamic range is possible than with the uniphase or 2-phase approach. Because of the smaller charge handling capability, the 1- or 2-phase SCCD is prone to back spills of charge, if the CCD well's charge handling capacity is exceeded. In 4- or 3-phase systems, the potential stops are larger in value and hence more effective in preventing backspill and crosstalk. Finally, the higher the clocking voltages, the better is the charge transport because of the higher fringe fields.

1.2.4 Buried Channel CCD's

The number of surface states located at the semiconductor-insulator interface imposes certain limitations on CCD transfer efficiency and noise. The traps and scattering occurring at the surface of an SCCD reduce the efficiency of charge transfer between adjacent CCD wells. Moreover, the scattering centers reduce the mobility and hence the charge transfer speed in a surface

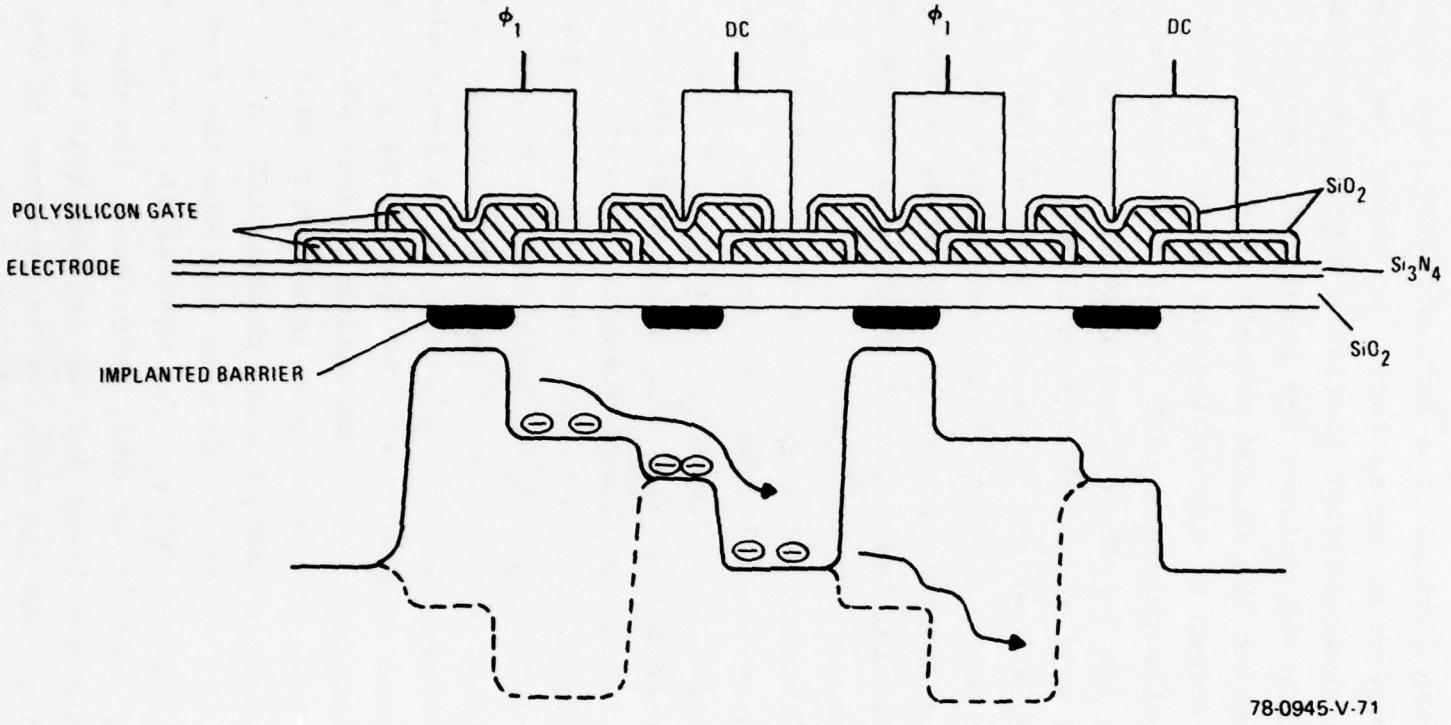


Figure 5. Cross Section Illustrating the Mechanism of One-Phase CCD Clocking

channel CCD. To eliminate the undesirable interaction between the charge and the surface of a semiconductor, the channel in BCCD is moved away from the surface. Locating the charge transport inside the semiconductor (buried channel) increases the carrier's mobility and reduces the number of trapping and scattering sites with which the charge signals interact. The buried channel CCD is formed by ion implanting in the silicon to form a layer of opposite polarity than the bulk silicon material. Reverse biasing the junction formed between the implanted layer and the silicon will form a depletion layer. By fabricating a CCD gate structure over the implanted layer similar to the gate structure of an SCCD, we form the charge transport channel of a buried CCD. The manipulation of the potential on the gates will form moving potential wells inside the buried channel within which the charge will be transported.

A further dividend realized with buried channel CCD is the increased fringing field influencing the charge transport inside the buried channel. An increased fringing field occurs because the charge is transported in a channel located farther from the clocking gates. With increased distances between clocking gates and the CCD channel, the gate screening effect decreases and the fringing field increases. Also, with larger amounts of charge in the buried channel, interaction between the surface and the charge in the buried channel occurs. Clearly, it is desirable to move the buried channel farther away from the clocking gates to realize a larger fringing field, and the buried channel should be profiled to accommodate more charge without interaction with the surface.

The peristalic or deep, buried channel CCD is a modified buried channel CCD which attempts to overcome the drawbacks of shallow buried channel CCD's. The channel in a PCCD is located about 5 μm away from the Si-SiO_2 interface. The channel is confined between the epi layer and the silicon bulk material of opposite polarity than the epi. As in the case of the BCCD, the PCCD channel is formed by reverse biasing the epi-Si junction

forming a depletion channel. The electrode structure used in a PCCD is the same as one for a BCCD. To increase the charge handling capability of the PCCD, the epi layer is graded in impurity concentration. The gradient in impurity concentration is such that most of the charge is located near (but not at) the Si-SiO_2 interface while a small amount is located at the Si-epi boundary. Such a charge distribution profile in a PCCD offers several advantages. Increased charge handling capability is obtained by confining the charge near the gate. To understand why the high rate of transfer between adjacent PCCD wells is maintained, even though the charge is stored near the gates, let us examine figure 6.

Basically, there are three mechanisms responsible for charge transport in CCD's; i.e., thermal diffusion, self-induced drift, and fringe field drift. Figure 6 shows a curve describing the fractional charge remaining in a potential well as a function of transfer time and the region where each of the above mechanisms is dominant. In general, self-induced drift will be responsible for the initial charge fraction transported with either thermal diffusion or fringe field drift determining the speed of transfer of the last fraction of charge. Self-induced drift arises from the gradient of mobile charge carriers in the potential well. The fractional charge remaining Q_r as a function of transfer time for self-induced drift is shown in figure 6.

Clearly, in the beginning self-induced drift and thermal diffusion are responsible for transporting 99 percent of the charge. When the amount of charge remaining to be transported has decreased below 1 percent, the effects of fringe fields becomes pronounced. Therefore, for high speed transfer, a high-fringing field is needed for the last 1 percent of charge remaining in the CCD well. In a PCCD, the charge fills the CCD well from the epi-Si interface to an area close to the Si-SiO_2 interface. During transfer, the first portion of charge to be transferred is the charge nearest to the clocking gate, a region where the fringe field is small. However, because of the large amount of charge

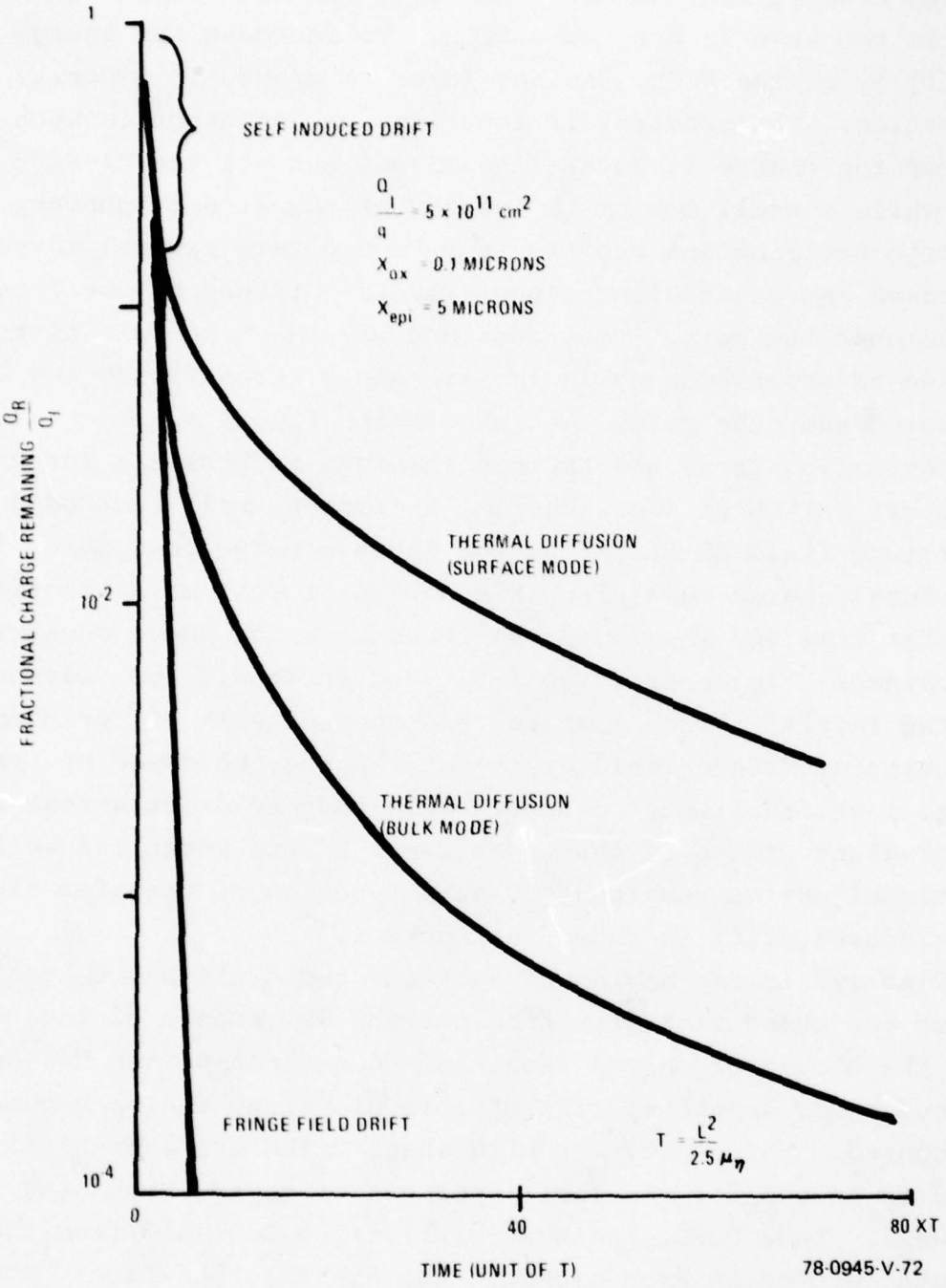


Figure 6. Functional Charge vs Normalized Time

present in the PCCD well, self-induced drift fields and thermal diffusion moves the bulk of the charge into the adjacent PCCD well. The remaining charge in the PCCD well is located farther away from the gates, hence the effect of the fringing field is more pronounced. Therefore, it also is transferred quickly into the adjacent CCD well. The profiling of the impurity concentration of the epi layer has improved the performance of the BCCD and increased its charge handling capacity.

1.2.5 Charge Injection

Signal charge can be injected into CCD electrically or optically. The absorption of silicon is in the visible wavelength spectrum. Hence, a packet of charge can be photoelectrically generated in an illuminated CCD well. The amount of charge photoelectrically generated will be proportional to the photon flux directed at the CCD well. Thus, a CCD area array into which charge is photoelectrically injected can serve as a visible image sensor. However, in most applications, an electrical signal is available and the amount of charge injected into the CCD register has to be controlled by the electrical signal.

There are two basic methods of electrical charge injection into a CCD. The dynamic current injection (DCI) mode and the potential equilibration (PE) mode are the principal techniques for injecting electrical signals into a CCD. A profile of an SCCD with different injection schemes is shown in figure 7. The CCD clocking phases are designated by $\phi 1$, $\phi 2$, and $\phi 3$. ID, G1, G2, and IS represent, respectively, the input diffusion diode, the first gate, the second gate, and the input signal. In the DCI (figure 7a), the ID, G1, and G2 nodes of the CCD are biased to correspond, respectively, to the source, gate, and virtual drain of a metal oxide semiconductor field effect transistor (MOSFET). The amount of charge injected (q_s) into the G2 CCD well can be calculated from the equation describing the operation of a MOSFET in the saturation region and the time (τ) available for injection.

$$q_s = \tau \mu \frac{W}{L_G} \frac{C_{ox}}{2} (V_G - V_T - V_{ID})^2 \quad (1)$$

where μ, W, L_G, C_{ox}, V_G, V_T, and V_{ID} are, respectively, the surface mobility, the channel width of G1, the length of G1, the oxide capacitance per unit area, the voltage on the gate, the MOSFET threshold voltage, and the voltage on the input diode. For the DCI mode of operation, shown in figure 7a, the input signal is connected to the input diode (ID); however, it is also possible to control the amount of charge q_s injected by connecting the input signal to the gate G1 and supplying the proper dc potential to ID. When the input signal is changed from ID to G1 in the DCI mode, the injected signal will be the complement or 180 degrees out of phase with the signal injected at ID.

In the potential equilibration method (see figures 7b and 7c), the amount of charge q_s injected in the CCD holding well (G2) is determined by the differences between the surface potentials under G1 and G2. Typically, the input diode (ID) is pulsed on to overfill with charge the holding well G2 and well G1. When the input diode (ID) is pulsed off (i.e., reverse biased), all the excess charge in wells G1 and G2 is drained until the surface potential of the free charge in well G2 is equal to the barrier potential under G1. It can be shown that the amount of charge q_s retained in G2 is equal to

$$q_s = (V_{G2} - V_{G1} \pm \Delta V_{TH}) A_{G2} C_{ox} = V_{in} C_2; \begin{cases} A_{G2} C_{ox} = C_2 = \text{input cap. of G2} \\ V_{in} = V_{G2} - V_{G1} \pm \Delta V_{TH} \end{cases} \quad (2)$$

where V_{G2}, V_{G1}, ΔV_{TH}, and A_{G2} are, respectively, the dynamic input on gate G2, the voltage on gate G1, the threshold variations ΔV_{TH} between the input gates, and the gate area of gate G2. The signal can be applied either to the G1 or G2 gate (see figure 7b or 7c). Generally, it is preferred to apply the signal to G2 and keep G1 at a constant dc voltage. Placing G1 at a constant dc voltage will offer some shielding between the pulsed diode ID and the signal gate G2. Also, by increasing the area size of G2, a larger signal dynamic range can be achieved.

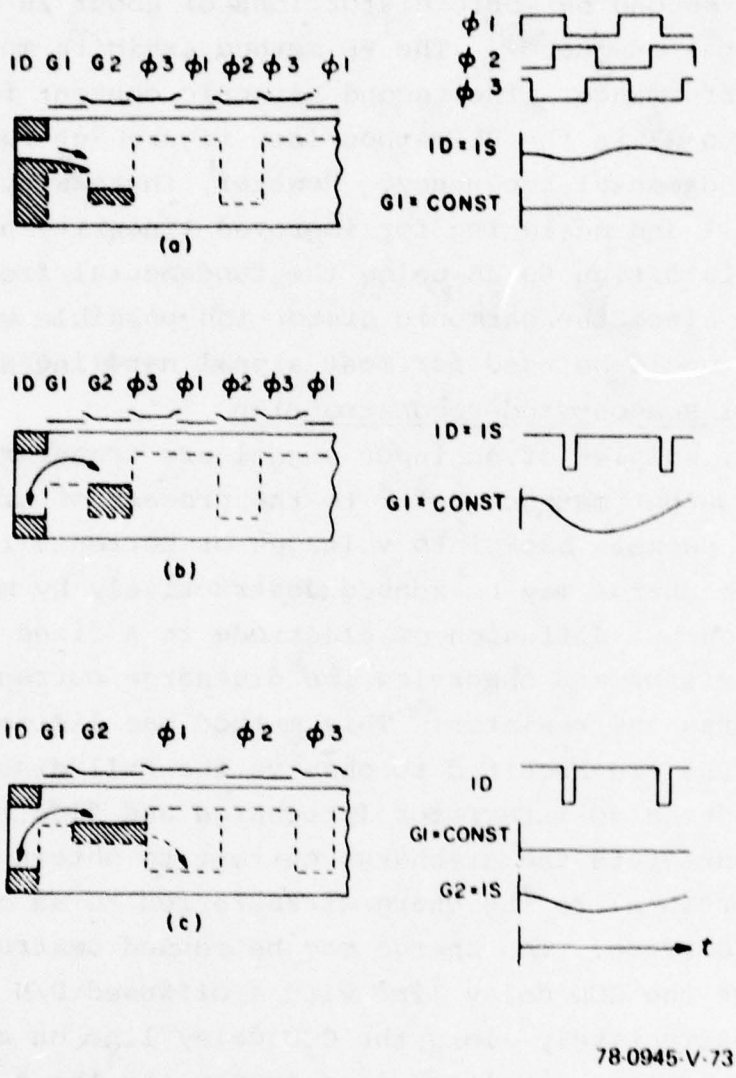


Figure 7. Various Schemes for Charge Injection into a CCD (The waveforms applied to the electrodes are shown on the right: (a) dynamic current injection, (b) potential equilibration method with a pulsed well electrode, and (c) improved equilibration method with input signal applied to enlarged holding well electrode)

One difference between the DCI and the PE method is in the injection linearity of each scheme. The DCI method produces unsatisfactory second harmonic distortions of about 20 percent of the fundamental frequency. The PE method exhibits much better linearity performance. The second harmonic content for the signal applied to G2 in the PE method (see figure 7c) can be 46 dB below the fundamental frequency. However, increasing the size of the G2 well and designing for improved linearity have achieved a harmonic distortion 60 dB below the fundamental frequency. It appears that since the harmonic distortion possible with PE is very low, PE would be used for most signal handling applications.

1.2.6 Signal Readout and Reconstruction

In a CCD, samples of an input signal are transferred as packets of charge. Output methods refer to the process of translating these charge packets back into voltages or currents in an external circuit. The charge may be sensed destructively by merely connecting the output diffusion or electrode to a fixed voltage through a resistor and observing the discharge current as a voltage drop acorss the resistor. This method has limitations since wide bandwidths are required to observe the full discharge current.

The gated-charge integrator (precharge and float) method can be used to integrate the discharge current to obtain a voltage change proportional to the charge transferred to an output diffusion or electrode. The charge may be sensed destructively at the output of the CCD delay line with a diffused P/N junction or sensed nondestructively along the CCD delay line on a gate electrode. In practice, a voltage is measured and the signal charge calculated. To illustrate this calculation a gated-charge integrator will be used to sense destructively the charge at the end of a CCD delay line. Figure 8 illustrates the basic gated-charge integrator which is constructed on the CCD chip, and the off-chip operational amplifier and sample/hold circuit to provide a signal reconstruction. The output signal is a voltage v_s measured at the

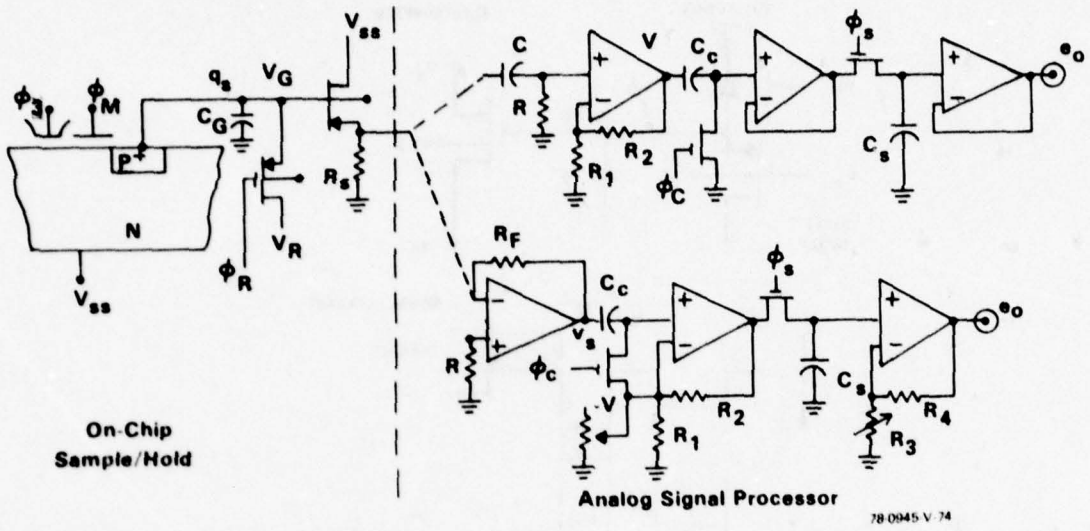


Figure 8. Current and Voltage Sensing Circuits for Signal Readout and Reconstruction

output of the operational amplifier. The charge q_s is calculated at the P/N junction detection node by the equation,

$$q_s = \frac{C_G V_s}{g_m R_F} \text{ (current amplifier)} = \frac{C_G V_s}{\frac{R_2}{R_1}\left(\frac{g_m R_s}{1+g_m R_s}\right)} \text{ (Voltage amplifier)} \quad (3)$$

which requires a knowledge of the on-chip capacitance C_G and transconductance g_m of the MOS amplifier. Figure 9 illustrates the basic "pre-charge on float" operation of the gated-charge integrator output circuit with the pre-charge or reset performed by the reset switch followed by a floating operation. The sequence shown in figure 9 is called "correlated double sampling" and the complete timing operation is illustrated in figure 10 for typical SI/SO (serial in/serial out) operation. The transfer function at low frequencies for a SI/SO CCD (also

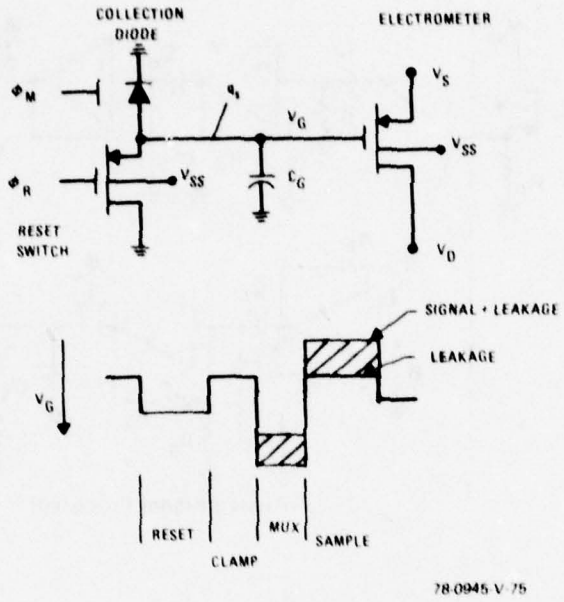


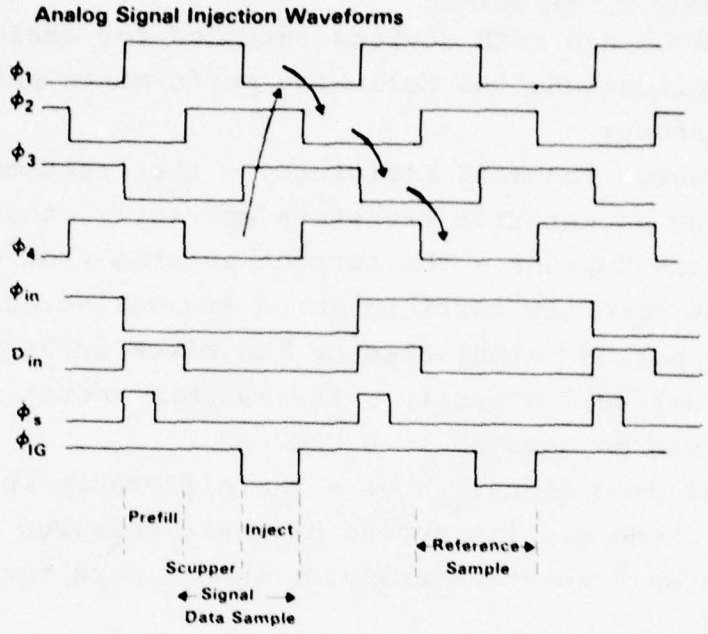
Figure 9. Schematic of Output Gated-Charge Integrator or "Pre-Charge and Float"

for PI/SO (parallel in/serial out) CCD) may be written neglecting transfer loss by combining equations (2) and (3) to yield

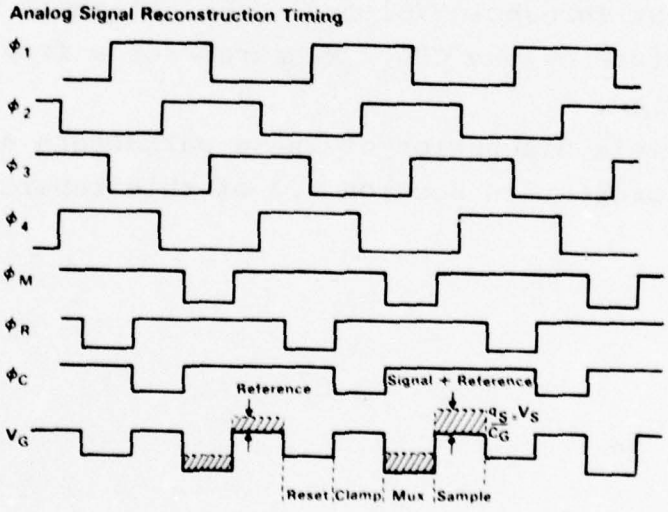
$$e_{out} \text{ (voltage amplifier)} = V_{in} \frac{C_2}{C_G} \left(\frac{g_m R_s}{1 + g_m R_s} \right) \frac{R_2 G}{R_1} \qquad (4)$$

$$e_{out} \text{ (current amplifier)} = V_{in} \frac{C_2}{C_G} g_m R_F G$$

where G is the gain following the preamplifier stage. We notice the dependence on input-to-output capacitance ratio and g_m; however, with the voltage amplifier mode, the selection $g_m R_s >> 1$ can densitize the variation of open loop gain with g_m and temperature.



(a)



(b)

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Figure 10. SI/SO Operation with Correlated Double Sampling

1.2.7 Performance Parameters

For both SCCD and BCCD devices intended for analog signal processing applications the following performance parameters are the most important:

a. Charge Transfer Efficiency - the fraction of the original charge packet that transfers correctly at each transfer.

b. Dark Current - the current arising from the thermally generated free minority carriers which are collected in a well during a time period established by the clock cycle.

c. Full Well Capacity - the maximum amount of signal charge which can be handled by a CCD.

d. Dynamic Signal Range - the difference in dB between a fundamental tone and its second harmonic measured at the output of the device by a spectrum analyzer when a pure tone is applied to the input.

e. Insertion Loss - the attenuation a signal experience between the input and output terminals of a CCD.

f. Input Threshold Voltage - the threshold voltage of the input structure of the CCD. Measured for a fixed value of G_1 as G_2 is varied.

A more complete discussion of these parameters and their measurement is present in section 2.3 of this report.

2. EVALUATION AND CHARACTERIZATION OF CCD DEVICES

2.1 CHOICE OF DEVICES FOR STUDY

During the first phase of the program a survey was made to determine the types of CCD/CID devices that were available for degradation study as of January 1977. The commercial literature was reviewed and a number of vendors were contacted by telephone to supplement the published information. Also the availability of Westinghouse in-house CCD devices was considered. The criteria for selecting device types for the study was based upon the following factors:

- o Availability
- o Cost
- o Surface and buried channel devices to be represented
- o Preference of analog devices over digital devices
- o Moderate functional complexity
- o Hermetically packaged
- o Imaging devices not considered for this study.

As a result of the first phase deliberations, three device types were selected for experimental study:

a. Fairchild Semiconductor CCD-321 which is a "n"-channel BCCD serial in-serial out (SI/SO).

b. Westinghouse 7004 CCD which is a "p"-channel SCCD shift-register device with a capability for multiplexing 20 parallel inputs into the shift register. Only the SI/SO mode of operation was used in the study. The 7004 chip was originally developed under contract number N00014-75-C-0283 in a study for the Naval Research Laboratory. The chips used in this program were fabricated with Westinghouse funds and were surplus from other studies.

c. Westinghouse 7007 CCD which is an "n"-channel PCCD SI/SO device. It is an experimental device developed with Westinghouse funds.

The choice of these three devices covers the major generic types of CCD devices, excluding imaging devices. They are of a moderate functional complexity, but yet useful in a broad range of signal processing applications.

2.2 PHYSICAL CHARACTERIZATION

2.2.1 The CCD 321

The CCD 321 device consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock, and output port allowing the device to be used as two 455- or one 910-bit analog delay line. A photograph of the chip is shown in figure 11, and a circuit diagram of the device is shown in figure 12. Each shift register is folded back seven times with an N+ corner diffusion. Figure 13 illustrates the semiconductor structure. The input structure consists of two gates and a diode as shown in figure 13A. In operation, ϕ_S is clocked to sample the input signal applied at V_I. V_R is a dc reference potential, and the charge injected is approximately proportional to $V_R - V_I$. ϕ_S and V_R are surface channel gates for good linearity, while the rest of the device is buried channel. An N+ floating diffusion diode between ϕ_S and V_R is used to increase the junction capacitance in the input structure for purposes of matching the nonlinear contribution in the input and output capacitors to produce a more linear voltage-to-voltage transfer characteristic of the device.

To minimize external clocking requirements, the CCD shift register is designed to operate in the 1½ phase mode so that only one transport phase, $\phi 1$, is clocked while the other phase, V_2, is set at an intermediate dc potential.

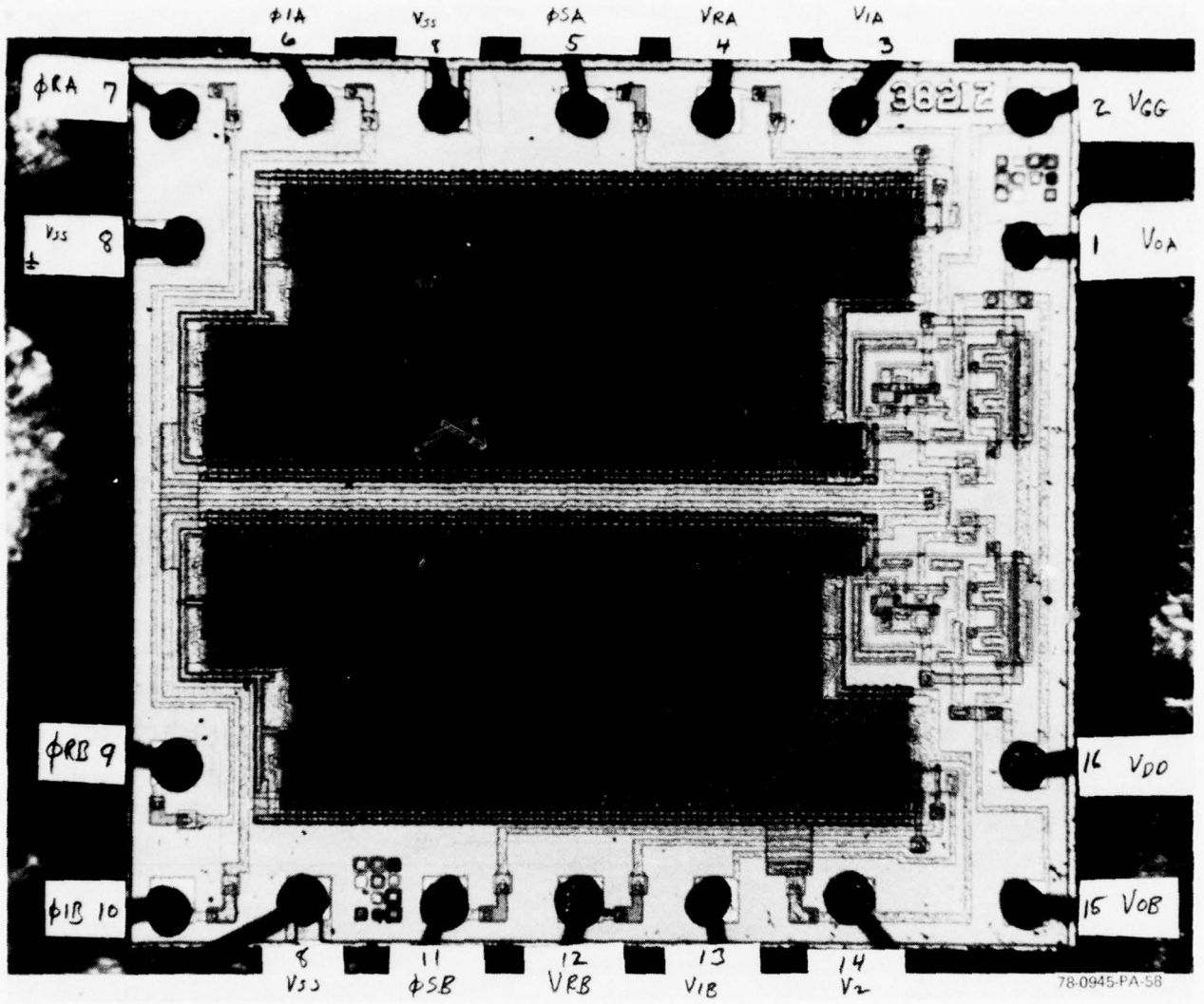
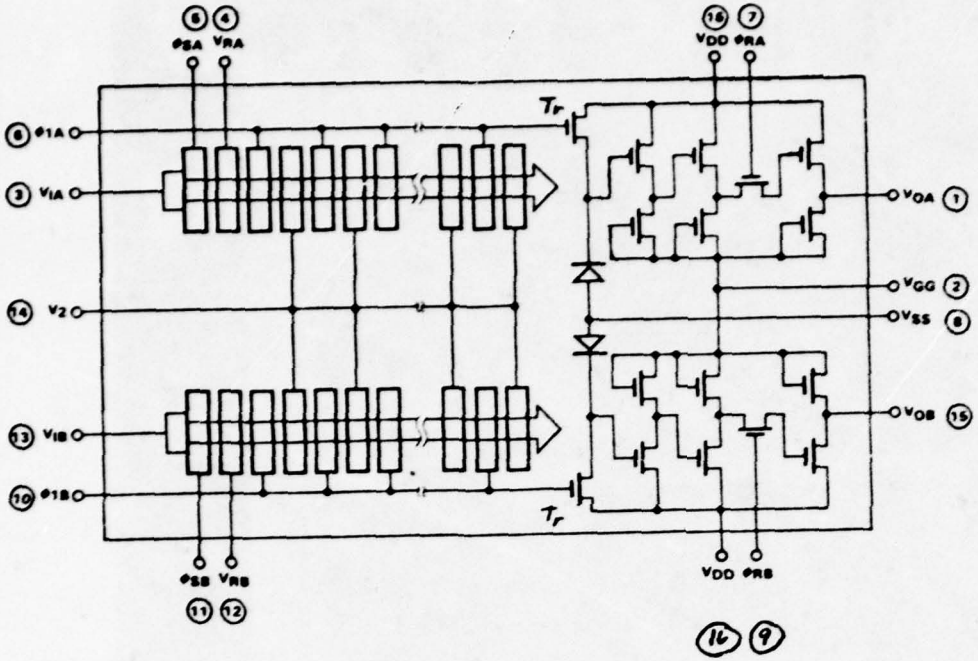


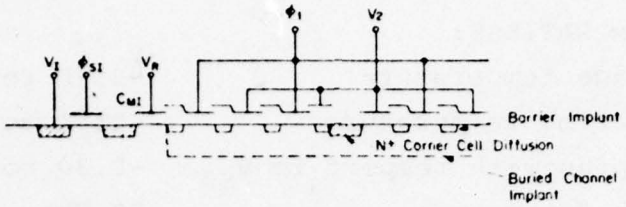
Figure 11. Chip Photo of CCD 321 Device



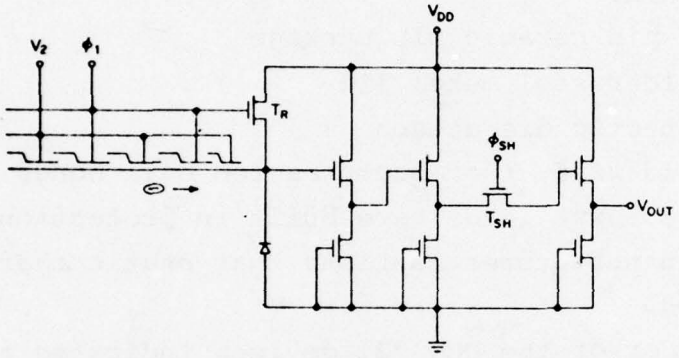
PIN NAMES	
Φ_{1A}-Φ_{1B}	Analog Shift Register Transport Clocks
Φ_{SA}-Φ_{SB}	Input Sampling Clocks
Φ_{RA}-Φ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA}-V_{IB}	Analog Inputs
V_{RA}-V_{RB}	Analog Reference Inputs
V_{OA}-V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

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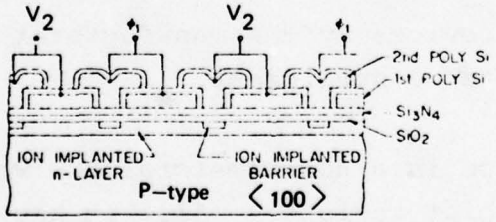
Figure 12. CCD 321 Circuit Diagram



A – SCHEMATIC OF INPUT STRUCTURE



B – SCHEMATIC OF OUTPUT STRUCTURE



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C – 1 1/2 PHASE CCD STRUCTURE

Figure 13. Semiconductor Structure: A-Schematic of Input Structure; B-Schematic of Output Structure; C-1½ Phase CCD Structure

- o MAXIMUM RATINGS:
  - Storage temperature -25°C to 100°C
  - Operating temperature -25°C to 55°C
  - All pins with respect to V_{SS} -0.3v to 20v
  - Clock frequency 20 MHz
- o PHYSICAL DIMENSIONS:
  - Chip size 2.07mm x 1.94mm
  - Channel width 50 micrometers
  - Width of each CCD gate 13 micrometers
- o PACKAGE:
  - 16 pin ceramic DIL package
  - Solder seal metal lid
  - Eutectic die attach
  - Gold wire, thermocompression ball bonds

All gate input leads have built in protection to static voltages. The manufacturer cautions that static charge buildup should be minimized.

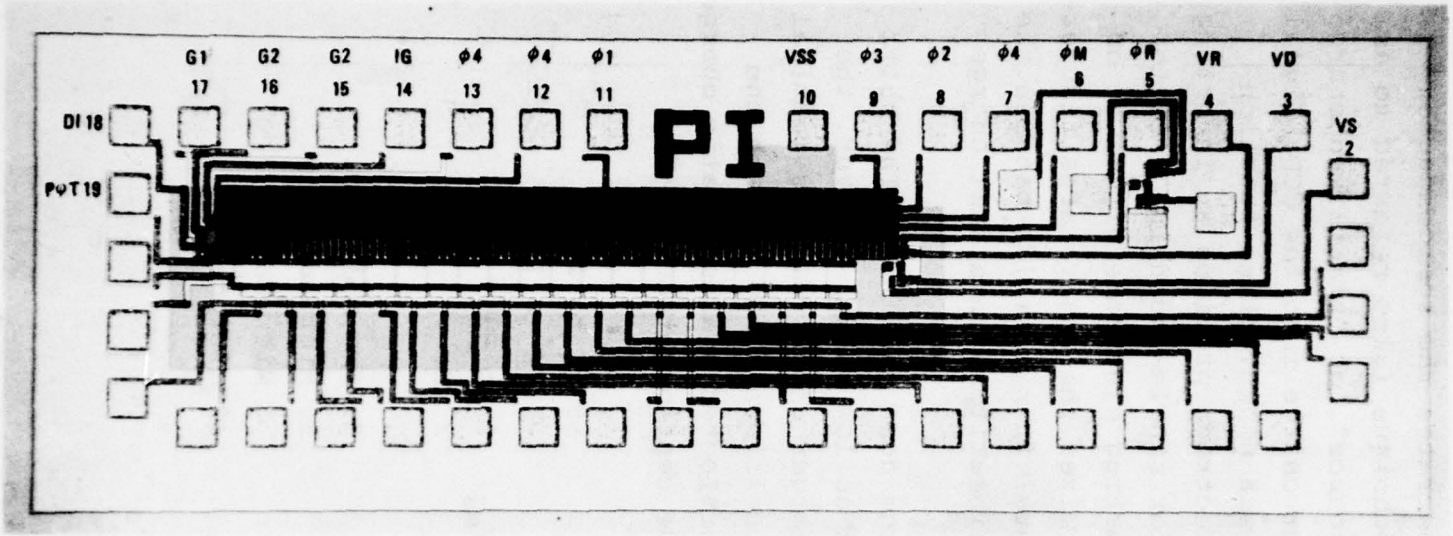
The vendor of the CCD 321 devices indicated that the manufacturer screen for the consisted of:

- o 100 percent fine and gross leak test
- o Electrical tests to verify that devices met parameters spec in manufacturers data sheet.

Of 3 groups of 7 devices of this type, there were no failures in 1000 hours of stress testing. The stress screen or burn-in applied to these devices by the manufacturer to weed out early failures appears to be sufficient.

2.2.2 The 7004

The 7004 device is a noncommercial CCD which consists of a 44-bit, 4-phase shift register. Also it has the capability of multiplexing 20 low data rate signal channels into a higher data rate output channel. The device was used as a serial-in/serial-out (SI/SO) shift register. The parallel input capability of the chip was disabled by connecting the parallel transfer gate P_T to V_{ss} and by not bringing out to the package pins any of the 20 parallel input. Figure 14 is a photograph of the 7004 chip with



PIN NAMES

DI	INPUT DIODE
G1	ANALOG REFERENCE INPUT
G2	ANALOG SIGNAL INPUT
IG	INPUT SAMPLING CLOCK
φ1, φ2, φ3, φ4	SHIFT REGISTER 4φTRANSPORT CLOCKS
φM	OUTPUT SAMPLING CLOCK
VR	RESET VOLTAGE
φR	RESET SWITCH GATE
VS	OUTPUT TRANSISTOR SOURCE
VD	OUTPUT TRANSISTOR DRAIN
VSS	SUBSTRATE GROUND
PφT	PARALLEL TRANSFER GATE

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Figure 14. 7004 Chip With Bonding Pad Labeled

bonding pad leads labeled. A circuit diagram of the device is shown in figure 15. Figure 16 illustrates the semiconductor structure. The "fill-and-spill" technique (also referred to as "potential equalibration", "clock source", or "stabilized charge injected" method) was used to inject charge into the CCD. Signal applied to the G1 electrode provides a noninverting function while a signal applied to the G2 electrode provides an inverting function. The preferred approach for single-ended input is to insert the signal on the G2 or inverting electrode with a dc or reference voltage on G1. This minimizes the active area fluctuations of G2 capacitance due to lateral fringe fields between the electrodes and thereby reduces nonlinearities in signal charge injection.

A 4-phase clock propagates charge down the line. The shift register will operate with voltages as low as 8V; however, the transfer efficiency improves with larger clock voltages (nominal 20V) due to the increase in electric fringe field beneath the electrodes. All of the gates are protected against static charge with a series resistance/zener diode configuration.

- o MAXIMUM RATINGS:
  - Storage tempeature -55°C to 200°C
  - Operating temperature -55°C to 125°C
  - All pins with respect to V_{ss} 0 to -35V
  - Clock frequency 2 MHz
- o PHYSICAL DIMENSIONS:
  - Chip size 3.76mm x 1.32mm
  - Channel width 50 Micrometers
  - Width of transfer gates 8 Micrometers
  - Width of storage gates 12 Micrometers
- o PACKAGE:
  - 40 pin ceramic DIL
  - Solder seal metal lid
  - Eutectic die attach
  - Aluminum wire, ultrasonic wire bonding

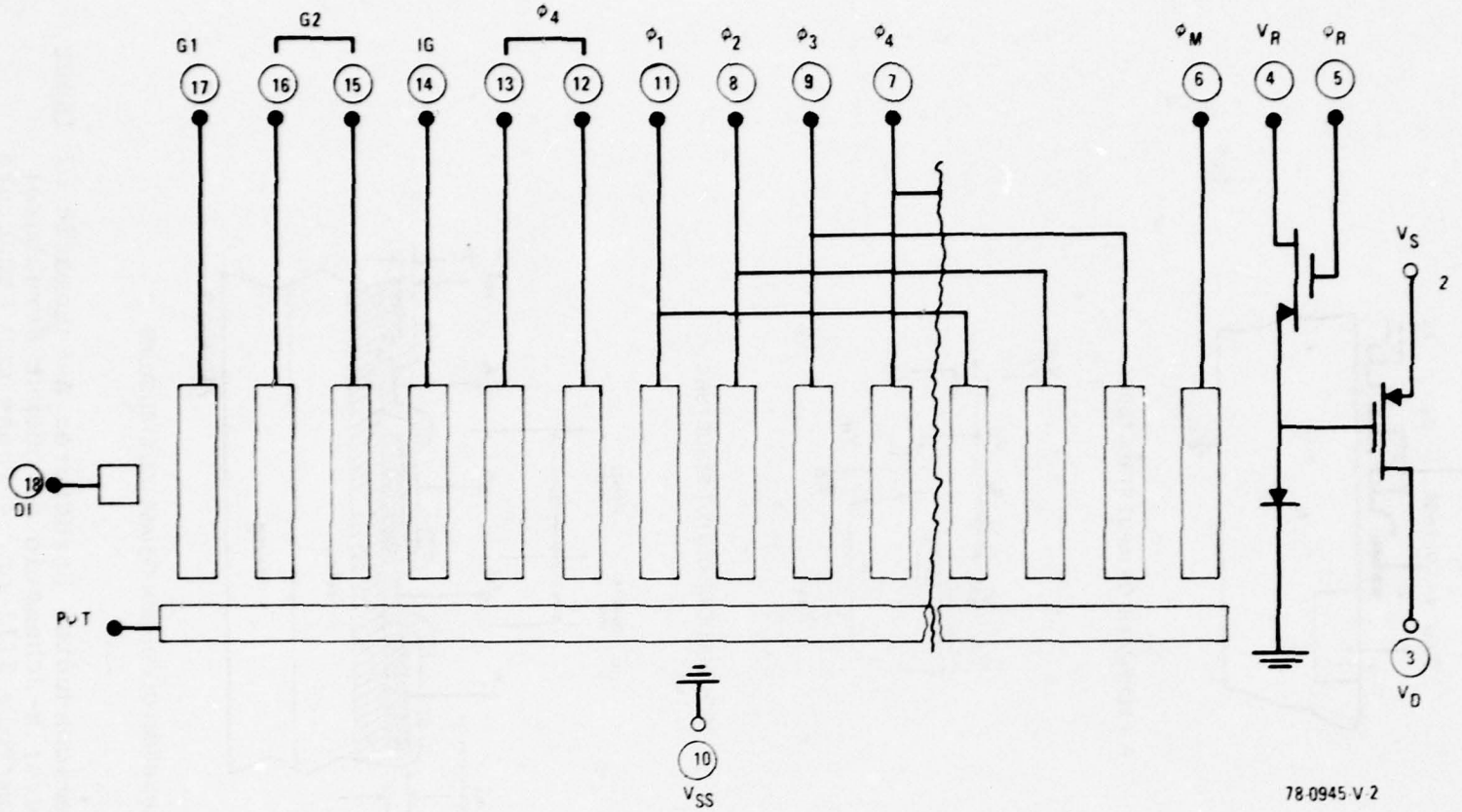
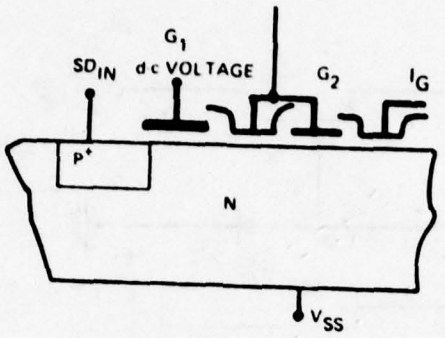
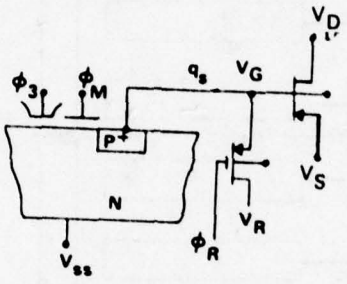


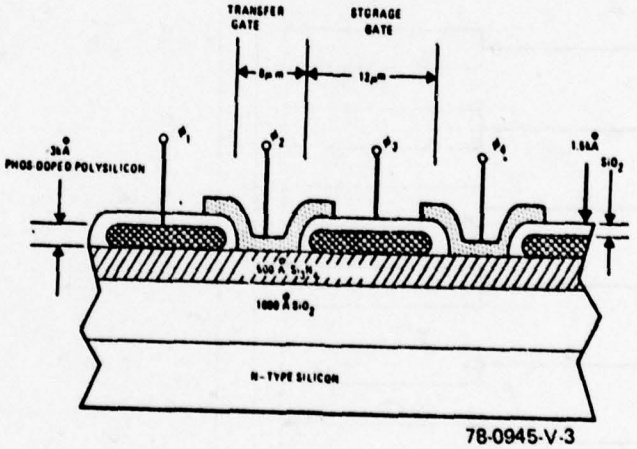
Figure 15. 7004 Shift Register Circuit Diagram



A – SCHEMATIC OF INPUT STRUCTURE



B – SCHEMATIC OF OUTPUT STRUCTURE



C – ALUMINUM/POLYSILICON 4 PHASE CCD STRUCTURE

Figure 16. Semiconductor Structure: A-Schematic of Input Structure; B-Schematic of Output Structure; C-Aluminum/Poly Silicon, 4-Phase CCD Structure

The initial screen for the 7004 devices consisted of:

- o Electrical test to verify operation
- o 100 percent fine and gross leak test

No screening was used to detect and remove early failures from the population of devices. The desire was to observe the early-failure fallout and obtain an indication of stress time required to remove these devices from the population.

2.2.3 The 7007

The 7007 device is a 76 stage experimental 4 phase n-channel PCCD. In operation the charge is contrained to a channel within an n-epitaxial layer. Figure 17 is a photograph of the 7007 chip with the active pads labeled as to function and package pin. Figure 18 shows the circuit diagram of the device and figure 19 illustrates the semiconductor structure. A coplaner electrode structure is used with a polysilicon gate and an overlapping gate of aluminum with each gate 7 micrometers wide. The dual dielectric between the gates and silicon consists of thermal silicon dioxide plus a layer of silicon nitride. The n-epitaxial layer is 3.5 micrometers thick. The input circuit consists of an input diode plus two gates, G_1 and G_2. In this study and in use up to frequencies of 10 MHz the "fill-and-spill" (potential equilibration) technique is used to inject charge into the CCD. Above 10 MHz the pulsed diffusion mode or diode injection technique is used. The output circuit consists of a charge integrater circuit using depletion mode MOS transistor. There is no protection built-in to protect the chip from static voltages. Therefore this chip is susceptable to static damage.

- o MAXIMUM RATINGS:
  - Storage temperature: $-55^{o}C$ to $200^{o}C$
  - Operating temperature: $-55^{o}C$ to $125^{o}C$
  - All pins to V_{ss}: 30V
  - Clock frequency: 85 MHz

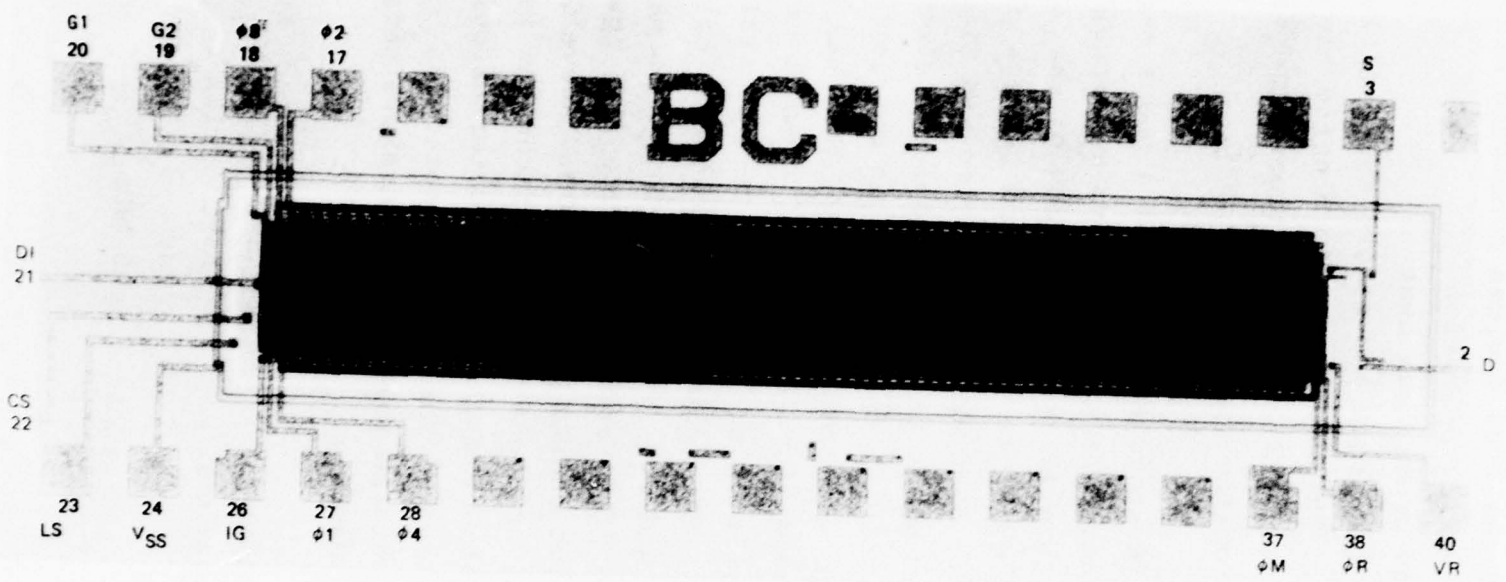


Figure 17. 7007 Chip with Active Pads Labeled

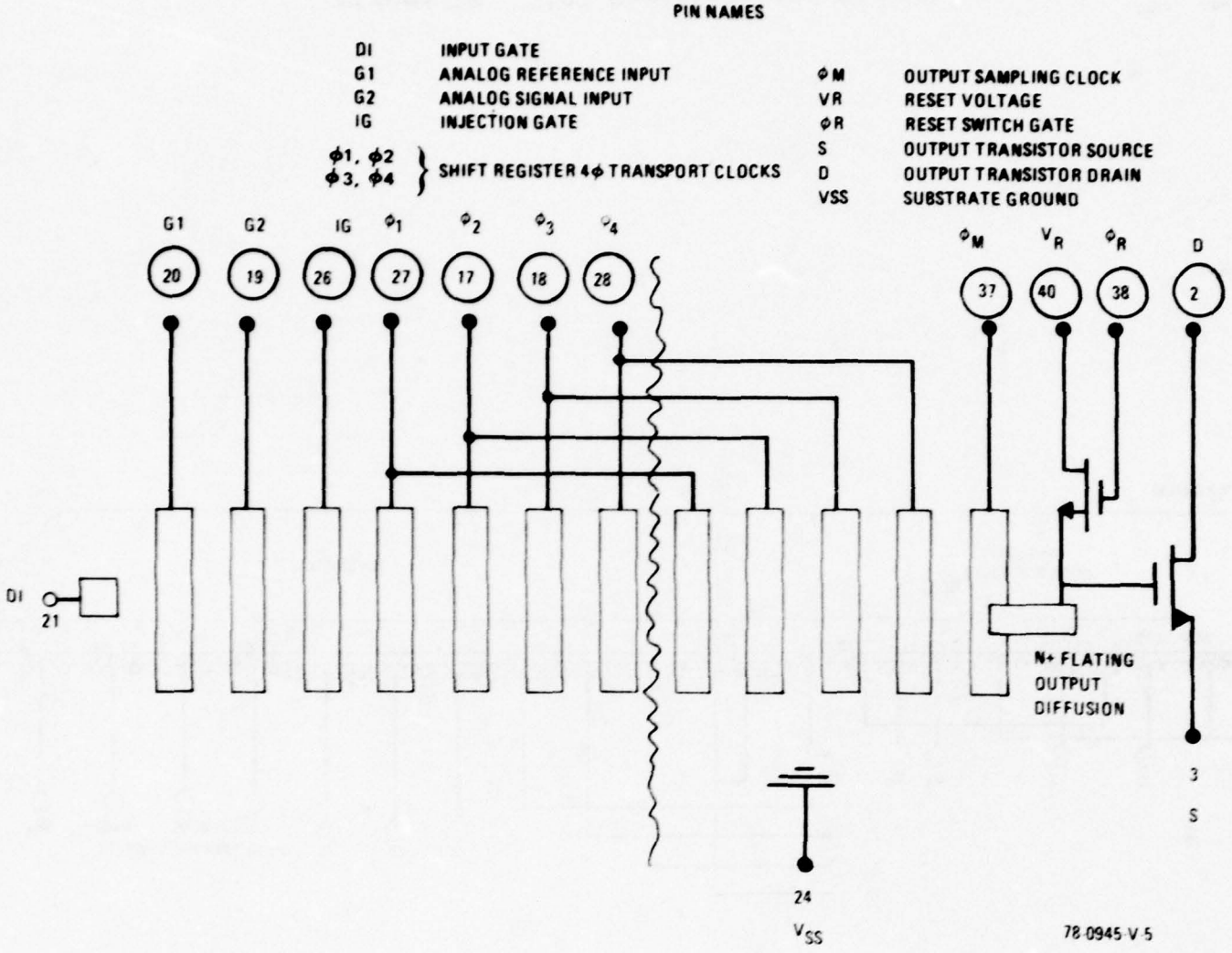


Figure 18. 7007 Shift Register Circuit Diagram

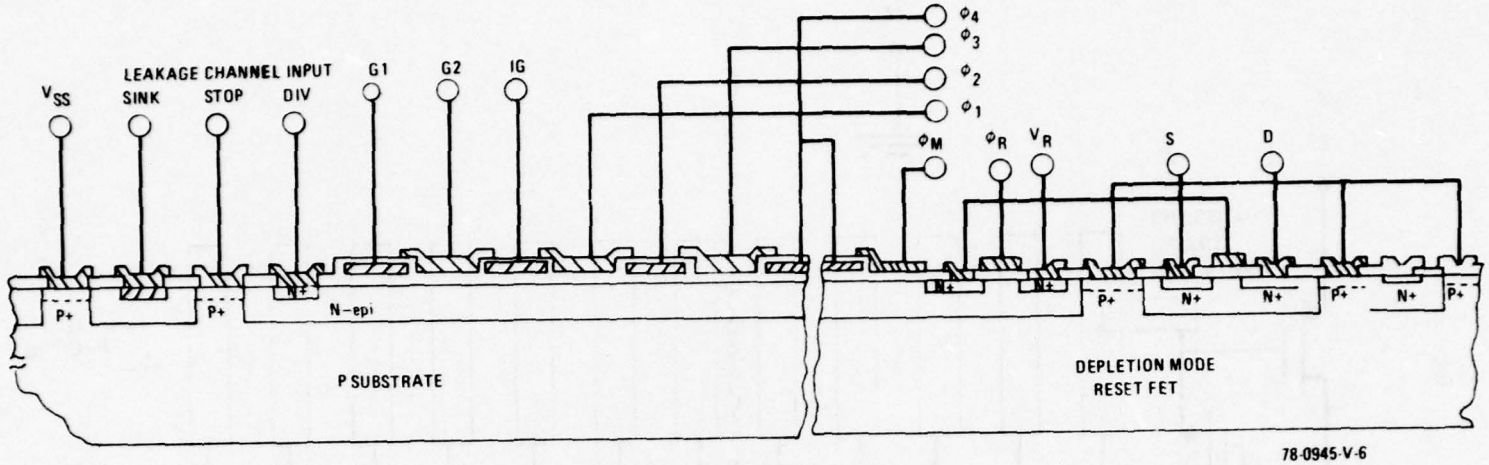


Figure 19. 7007 Semiconductor Structure

- o PHYSICAL DIMENSIONS:
  - Chip size 3.59mm x 1.34mm
  - Channel width 246 micrometers
  - Width of each gate 7 micrometers
- o PACKAGE:
  - 40 Pin ceramic DIL
  - Solder steel metal lid
  - Eutectic die attach
  - Aluminum wire, ultrasonic wire bonding

The initial screening for the 7007 devices consisted of:

- o Electrical test to verify operations
- o Open/short test on all gates and diodes
- o Fine and gross leak test

No screening was used to detect and remove early failures from the population of devices. The desire was to observe the early-failure fallout and obtain an indication of stress time required to remove these devices from the population.

It must be emphasized that the 7007 CCD is an experiemental device rather than a mature product and is currently still under development.

2.3 MEASURED ELECTRICAL PARAMETERS

The second phase of the program was concerned with the choice of electrical parameters that should be used to measure for characterizing device operation and degradation; setting up the appropriate test equipment to measure the desired parameters, and then verifying the desired measurements on typical samples of each device type. This section discusses the electrical parameters listed below that were selected for measurement during the long-term life tests part of the program.

- o Full Well Capacity
- o Dark Current
- o Transfer Efficiency
- o Insertion Loss
- o Dynamic Range
- o Input Structure Threshold Voltage
- o Open/short test on gates and diodes

Measurements were made at 1 MHz with CCD exercisers that provided all the pulse and voltages needed to operate the device under test. The 7004 and 7007 device exercisers had the capability to reverse clock phases so as to change the direction of charge transfer in the CCD for direct dark current measurement. In order to be able to measure the CCD properties at temperature extremes, the driver circuits in the exerciser had sufficient capability to operate the CCD over a 1 foot length of shielded cable at 1 MHz, which permitted the device under test to be located inside a controlled temperature chamber. The circuit used for making the measurements are shown in Appendix A.

2.3.1 Full Well Capacity

Full well capacity is the maximum amount of signal charge which can be handled by a charge-coupled device. It is dependent on the physical geometry of the CCD and also, to some extent, on the magnitude of the applied clock voltages and their temporal relationship; i.e., in a 4-phase system, "drop clock" yields less signal handling capacity than "push clock".

Full well capacity was measured as the maximum output voltage difference between empty charge packets, when charge injection was cut off, and the largest charge packet the CCD would transfer when the output was saturated. The timing and magnitude of the applied pulse voltages were kept constant for all measurements to assured reproducible and comparable results. The measurement approach did not differentiate whether the input structure, CCD shift register, or the output circuit saturation was the controlling processes. However, this measurement approach is believed to be valid as far as indicating charge/degradation in full well capacity of the CCD device, even though the "full well" measurement may not represent full charge capacity of the CCD shift register if the input or output structures were the limiting elements. It has the value of being simple, applicable in the same way to all the devices, and measures the actual saturated output of a device.

2.3.2 Dark Current

Dark current is the accumulation of additional carriers in potential wells from generation recombination centers found both in the bulk and at the silicon-silicon dioxide interface. The three major sources of dark current are thermal generation at the SiO_2-Si interface, thermal generation in the depleted bulk, and thermal generation in the nondepleted bulk within a diffusion length of the depletion region. This latter source is small compared to the former sources. The dark current density (or leakage current) can then be expressed as

$$I_D = I_S + I_B \tag{5}$$

$$= \tfrac{1}{2}\pi kTqN_i \bar{V}_{th} \sigma_S N_{ss} + \tfrac{1}{2}qN_i \sigma_B \bar{V}_{th} X_d N_t$$

where σ_S and σ_B are the capture cross section of surface and bulk traps respectively. N_{SS} and N_t are the surface and bulk trap densities, x_d is the depletion width and $\bar{V}_{th}$ is the thermal velocity of carriers. Surface trapping states are distributed

uniformly across the bandgap and distributed in emission time constants. Bulk trapping states, in contrast are discrete and located within $\pm$0.1eV of the middle of the bandgap. The intrinsic carrier concentration, Ni, varies with temperature as $e^{-Eg/kT}$ where Eg is the bandgap and is 1.12 eV for silicon at room temperature. As a result, the dark current possesses a strong temperature dependence and goes up by a factor of 2 for every 10^{o} C increase in temperature. The dark current degrades stored information with increasing time causing a nonuniform noise distribution in system applications in which the CCD clocks are not operating continuously or signals take different paths through the device to the output. In the case of continuous clocking the increased dark current reduces dynamic range.

The measurement of dark current for the 7004 and 7007 device was made by measuring the difference in reset current flowing to the charge collection node at the CCD output with the shift register running first in the forward direction, and then in the reverse direction, with no charge being injected by the input structure. Using this procedure, the charge packets will be empty except for dark current. In the forward clock direction the dark current is delivered to the collection diode, while in the reverse clock direction the dark current is swept away from the collection diode and therefore, only the current due to the output amplifier itself is present. The difference between forward and reverse clocking is the actual dark current.

The dark current is normally reported as a dark current per cm^2 of active CCD area which serves as a common denominator for the comparison of CCD structures of different sizes and number of stages. The calculation of dark current density, J_D is:

$$J_D = \frac{I_F - I_R}{A_T} \qquad (6)$$

where: I_F is the current measured for the forward clock direction.

I_R is the current measured for the reverse clock direction.

A_T is the total active area of the CCD charge transport channel at the silicon surface.

For the 7004 PI device:

$$A_T = 8.94 \times 10^{-4} \text{ sq cm} \tag{7}$$

For the 7007 device:

$$A_T = 5.3 \times 10^{-3} \text{ sq. cm} \tag{8}$$

The CCD-321 device was not amenable to the direct measurement of dark current as in the case of 7004 and 7007 devices because the charge transfer direction is built into the structure. Also, the charge collection node at the output of the CCD was not available independently of other circuitry. The dark current measurement was made for the CCD-321 by first stopping the clock with one phase high for a period of time to collect the dark current charge. After a suitable integration period the charge pockets were then clocked at high speed to the output. The output waveform contains the signal voltage both with and without the leakage current integration. The voltage difference (Δv) between the siganl voltage with and without integration is due to the dark current. Figure 20 illustrates the dark current integration waveform for the times used for measurement. For read-out times short compared to integration time; i.e., 10:1, the dark current is related to the voltage difference by:

$$J_D = \frac{Q_{FW} \dfrac{\Delta V}{V_{FW}}}{\tau_i \quad A_{T.}} \tag{9}$$

where: Q_{FW} = Full well charge = $1.1 \times 10^6 q$ (q = electron charge)

V_{FW} = Full Well CCD output voltage

τ_i = Average integration time

ΔV = Voltage difference (see text)

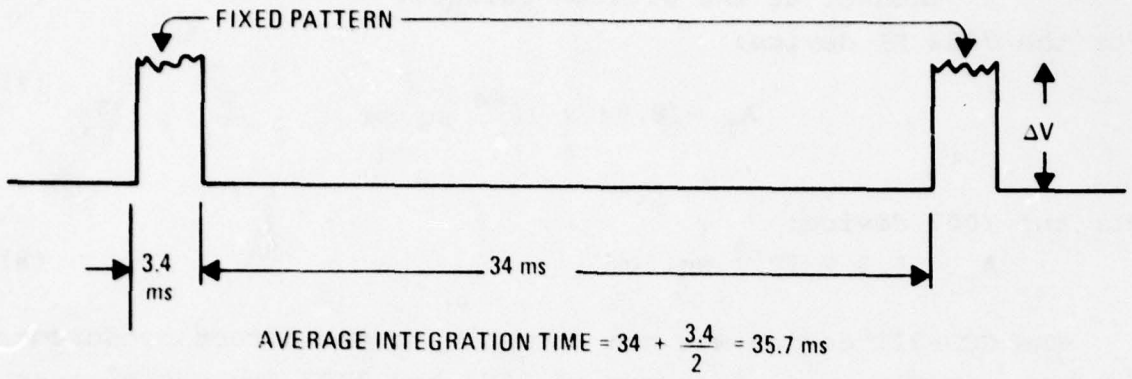


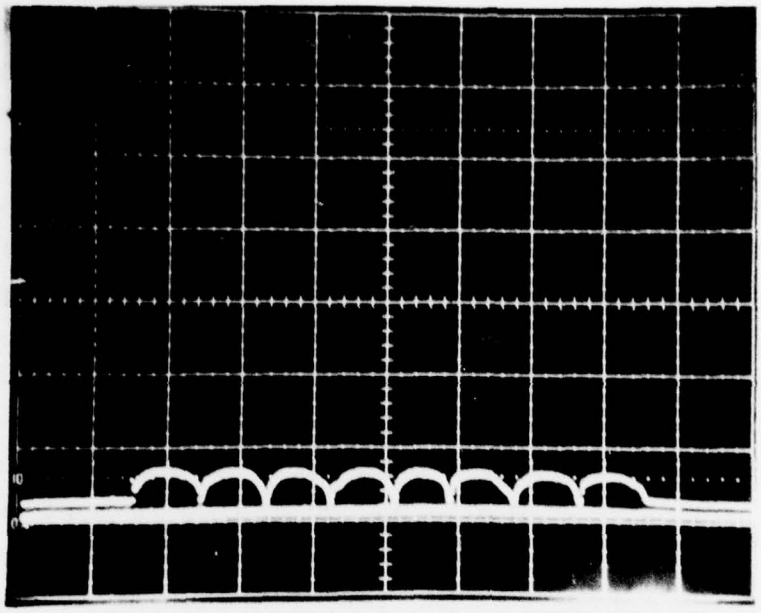
Figure 20. (U) Dark Current Integration Waveform

$$A_{T_1} = 1.3 \times 10^{-5} \text{ sq. cm (one well)} \tag{10}$$

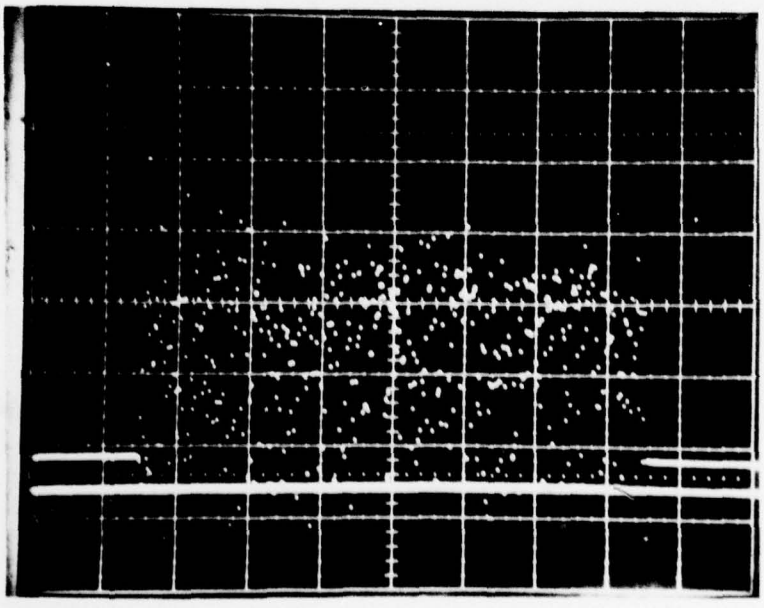
$$J_D = \frac{(1.1 \times 10^{6} \times 1.6 \times 10^{-19}) \frac{\Delta V}{VFW}}{35.7 \times 10^{-3} \times 1.3 \times 10^{-5}} \tag{11}$$

$$J_D = 379 \times 10^{-9} \frac{\Delta V}{V_{FW}} \quad \text{A/ sq. cm} \tag{12}$$

Photographs of the integrated dark current for two devices are shown in figure 21. Device in figure 21A has a relatively low level of dark current. The cusps appear to be the result of the corner turns in the shift register structure. Figure 21B shows a device where the dark current level varied dramatically from bit to bit as can be seen by the scattering of data (where each dot represents an individual bit). The variations in dark current shown in figure 21 illustrate what is generally known as the "fixed pattern." These two examples represent the extremes of dark current level found in a 25-device



A. Dark Current Pattern for CCD 321-5B (Vertical Scale 0.2v/Cm)



B. Dark Current Pattern for CCD 321-12B (Vertical Scale 0.5v/cm)

78-0945-PA-8

Figure 21. (U) Dark Current Readout by Integration

lot purchased for this program. For purposes of comparison during life test instead of photographing the dark noise pattern each time, an average dark current voltage level measurement was made directly from the oscilloscope screen.

2.3.3 Transfer Efficiency

Charge transfer efficiency (or its complement, charge transfer inefficiency) is an important measure of device performance for analog signal processing. Transfer inefficiency is due to the trapping of charge at either the SiO_2-Si interface or within the depleted bulk. A degradation in charge transfer efficiency can result from the introduction of defects and/or a change in the fixed charge density. The former mechanism is manifested by an increase in interface or bulk trap density and/or a decrease in minority carrier mobility. The latter mechanism is manifested by the trapping of electrons or holes in the oxide near the oxide-nitride interface necessitating a change in operating voltages for optimum performance (This situation is undesirable from a user's viewpoint). The effect of charge transfer inefficiency on the transfer function characteristics of the serial-in/serial-out analog sampled data CCD's is given by the expression:

$$\left| \frac{A_{out}}{A_{in}} \right| = \frac{g_m R_s}{1+g_m R_s} \left(\frac{C_{in}}{C_{out}} \right) \left(\frac{\mu^2}{1 + \epsilon^2 - 2\epsilon \cos (2\pi f/f_c)} \right)^{N/2} \frac{\mathrm{SIN}\ (2\pi k)}{2\pi k}$$

$$k < 1 \qquad (13)$$

where g_m is the transconductance of the output electrometer, R_s is the output electrometer source resistance, C_{in} is the effective input capacitance, and C_{out} is the output capacitance of the reversed bias readout diffusion. The term η is the charge transfer efficiency while ϵ is the charge transfer inefficiency defined as $\epsilon = (1-\eta)$. The term f is the input signal frequency, fc is the clock frequency N is the number of CCD stages and k is the ratio of signal output aperture to clock period.

Charge Transfer Efficiency (CTE) measurements are most readily performed by use of a two-level signal: high charge = one, low charge = Fat Zero (FZ). Typically, the signal is repetitive, consisting of a block of M-ONE's followed by a block of P - Fat Zero's. M should be large enough so that the last several ONE's all have the same amplitude - typically, M = 8 to 16. P should be large enough that, for the case of a true zero signal charge, only leakage charge at the device temperature remains in the CCD channel.

For computational purposes, the inefficiency factor ϵ is usually calculated where: CTE = $1 - \epsilon$, and ϵ has been defined in the literature[3] as

$$\epsilon = \frac{\Delta Q}{Q_{sig} - Q_{FZ}} \tag{14}$$

where ΔQ is the net charge lost from a large charge pocket, Q_{sig} is the signal charge, and Q_{FZ} is the continuously introduced background (or bias) charge of fat zero (FZ). A method[4] of measuring the inefficiency parameter ϵ is illustrated in figure 22 which shows a train of uniform signal charges in the midst of a long series of fat zeros. ΔT is the difference between the signal charge and the fat zero charge. The differences $\Delta 1$, $\Delta 2$, $\Delta 3$ etc., are the amounts of charge missing from the first, second, third, etc., pulses in the train; and $\Delta' 1$, $\Delta' 2$, $\Delta' 3$, etc., are the amounts of charge in excess of the fat zero charge which emerge in the first, second, third, etc., pulses trailing the pulse train. The normalized total loss in the leading edge (L_L) is defined by

$$L_L = \frac{1}{\Delta T} \sum_i \Delta i \tag{15}$$

and the normalized total less in the trainling edge (L_T) is defined by

$$L_T = \frac{1}{\Delta T} \sum_i \Delta i' \tag{16}$$

[3] C. N. Berglund, IEEE trans. SC-6, pgs. 391 - 394 (Dec. 1971)
[4] R. W. Brodersen, D. D. Buss, A. F. Tasch, Jr., IEEE Trns. Ed-22 pg. 40-6, (Feb 1975)

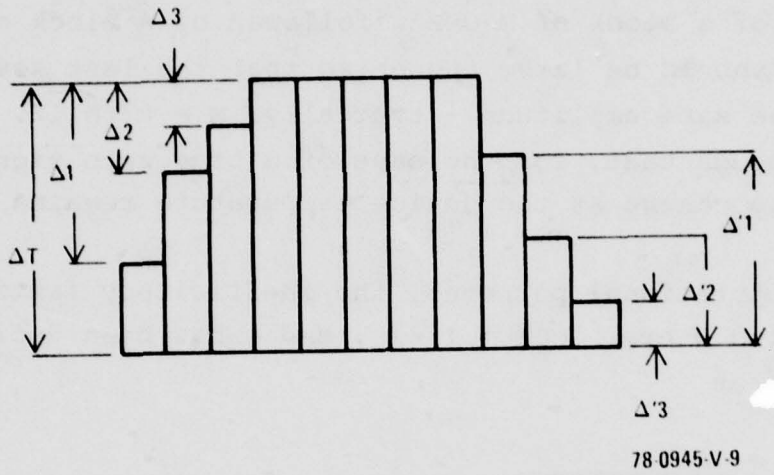


Figure 22.(U) The output of a CCD which has a proportional loss when the input is eight clock periods long

Analysis of the operation of a CCD considering only proportional loss has shown that the loss in a given leading-edge pulse is equal in amplitude to the corresponding trailing pulse; i.e., $\Delta 1 = \Delta' 1$, $\Delta 2 = \Delta' 2$, $\Delta i = \Delta' i$. For our case, where the output is taken from an output diode, which is a destructive output, an expression for the individual pulses is

$$\Delta i = \Delta' i = 1 - \epsilon - \sum_{k=0}^{i-1} \binom{N-k-2}{k} e^k (1-\epsilon)^N \qquad (17)$$

where N is the number of transfers and $\binom{i}{j}$ is a binomial coefficient. This expression has the computational advantage that there is only one term to determine $\Delta 1$ or $\Delta' 1$, etc. Brodersen[4]; et al, indicated that utilizing the above relationship

$$L_L = L_T = \frac{(N-1)\epsilon}{1-\epsilon} \qquad (18)$$

or

$$\epsilon = \frac{L_L}{N - 1 + L_L} = \frac{L_T}{N - 1 + L_L} \qquad (19)$$

which is independent of signal amplitude. This expression provides a simple means of calculating transfer inefficiency or CTE which is $1 - \epsilon$. When fixed and nonlinear losses are considered in addition to proportional loss, they give rise to a nonsymmetric-looking output from equal amplitude pulse train at the inputs. Since the amount of charge is conserved $L_L = L_T$, but in general $\Delta i \neq \Delta' i$. Also the emission of charge in this situation after the trailing edge of the pulse train is usually relatively slow and it takes many pulses for the charge to be reemitted. Because of the possibility of this situation, transfer efficiency is most accurately determined by measuring the amount of charge missing from the leading pulses of the output.

Transfer efficiency was measured at 0 percent and 10 percent fat zero (FZ) levels for the CCD 321 and 7004 devices. As fixed loss is eliminated by a sufficiently large FZ, the variation of transfer efficiency at 0 percent FZ provides an indication of changes in charge trapping levels even though the 10 percent FZ level measurements of CTE may show no change. Transfer efficiency measurements on the 7007 device were made at 25 percent FZ level. The performance at 0 percent FZ of the particular group of samples used was not representative of their class of devices.

A useful variation of transfer efficiency (inefficiency) measurement is the "double pulse technique"[5,6], where transfer efficiency is measured as a function of time between pulses without bias charge. A burst of charge pockets is input to the CCD to fill traps. The initial burst is followed by a variable delay time, t, during which no charge is input to the CCD. If the characteristic emission time τ of certain traps satisfies $\tau < t$, these traps may emit their trapped electrons. The empty traps

[5] J. E. Carnes & W. F. Kosonocky, Appl. Phys. Lett. Vol. 20, pgs. 261-263 (April, 1972)

[6] N. S. Saks, IEEE Transactions on Nuclear Science, Vol. NS-24, N6, pgs. 2153-2157 (Dec. 1977)

then capture electrons from the first signal pocket following the delay time. A plot of the loss vs time between bursts from the double pulse measurements provides information from which electron emission rates and electron trap creation rates for defects created by stress testing, can be calculated.

2.3.4 Insertion Loss

Insertion loss is the measure of signal power loss between the input and output of a CCD. From equation 20, the insertion loss in dB is given by the ubiquitous relationship:

$$dB = 20 \log \frac{A_{out}}{A_{in}} \qquad (20)$$

for a specified input frequency, clock frequency and value of k in equation (13).

Insertion loss was measured experimentally using a Hewlett-Packard Model 1417 spectrum analyzer with a test signal of known power level. Measurements were made at a nominal 50 ohm impedance level, a clock frequency of 1 MHz, and a test signal of 225 KHz.

2.3.5 Dynamic Range

The cummulative effects of decreased charge handling capacity, increased dark current, and nonlinear distortion due to degraded input injection or signal recovery can be directly measured as a dynamic range value. Experimentally, dynamic range was measured as the difference, in dB, between the fundamental tone output of the CCD and its second harmonic when the second harmonic power equaled the rms noise power out of the device. These measurements were made using a spectrum analyzer. The spectral content of the noise was predominantly white with little contribution to total noise power due to 1/f noise for both types of CCD's tested.

The measurements were made at a nominal 50 ohm impedance level, a clock frequency of 1 MHz, and a test signal of 225 KHz.

2.3.6 Input Threshold Voltage

There are several methods to launch or inject a quantity of charge which is linearily related to an input analog voltage as discussed in section 1.2.5. The best method to inject charge into a CCD is the so-called "fill-and-spill" technique in which

the injected charge is related linearly to the difference in voltage on the two gate electrodes G_1 and G_2, as shown in figure 23. If the two gate electrodes G_1 and G_2 are fabricated in an identical manner so their threshold voltages are very closely matched, then the charge injected is invariant with threshold variations from device to device. The basic principle is to fill a well under the G_2 electrode with excess charge and let it spill out backwards (scuppering) until the remaining charge is determined by the difference between the voltages and threshold voltages of G_1 and G_2.

$$q_s = C_2 \, (V_{G2} - V_{G1} \pm \Delta V_{th}) \tag{21}$$

where C_2 is the effective storage capacitance (i.e., determined by the "effective" G_2 electrode area) and ΔV_{th} is the difference in threshold voltages between the G_1 and G_2 electrodes.

Figures 24 and 25 illustrate the input transfer characteristic of the 7004 and 7007 CCD devices for a single-ended input.

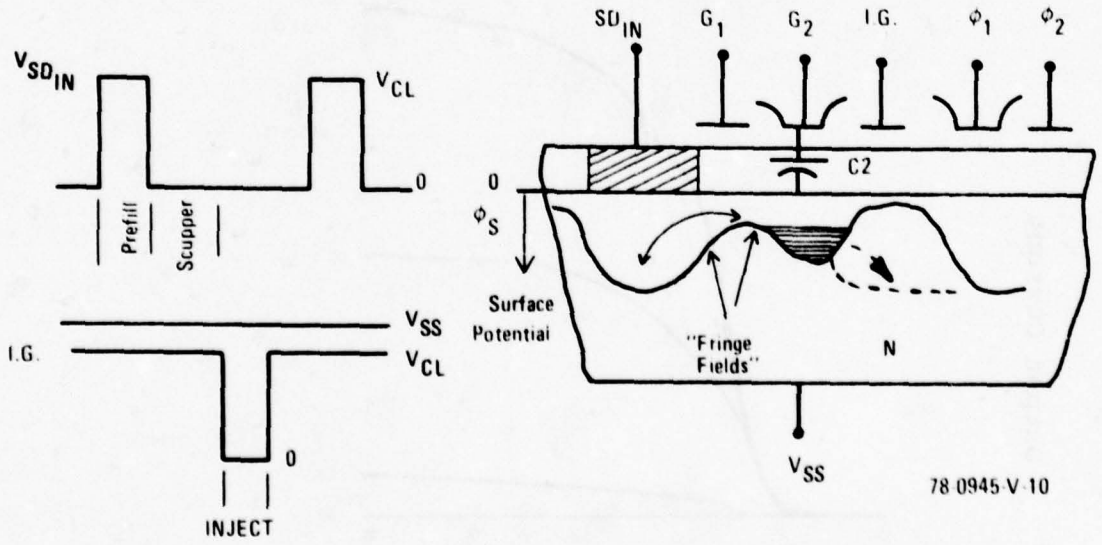


Figure 23. Fill and Spill Input Method

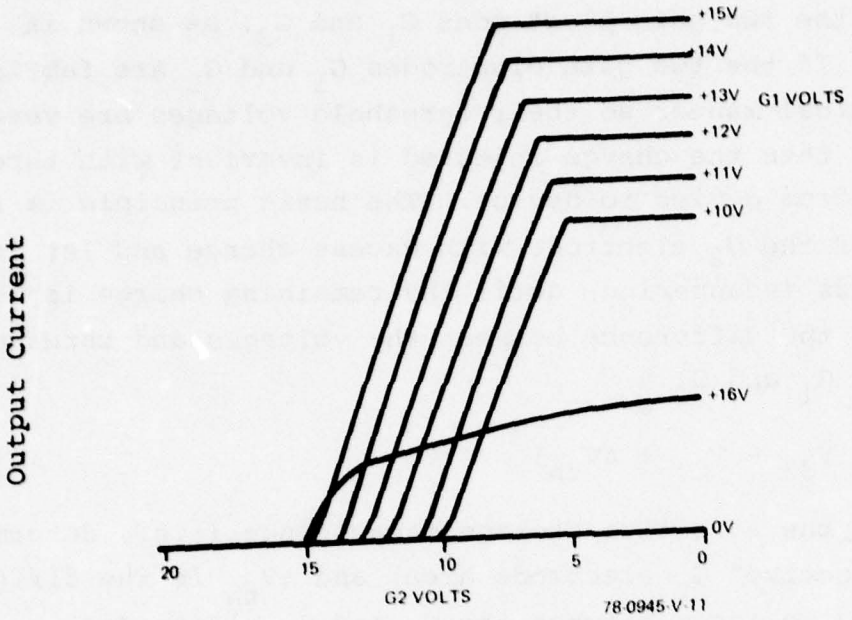


Figure 24. 7004 Input Transfer Characteristics

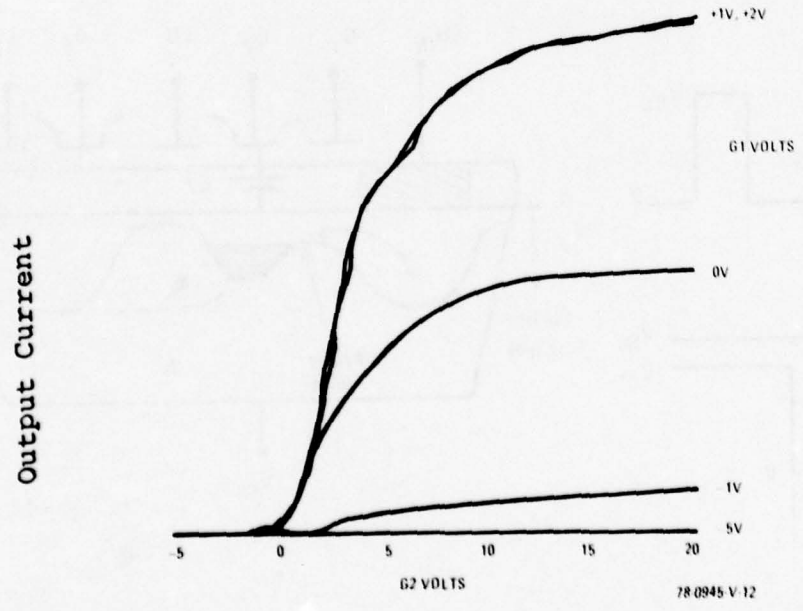


Figure 25. 7007 Input Transfer Characteristics

These characteristics were taken by fixing G_1 at a series of fixed voltages and varying G_2 over a range of voltages. The output of the CCD was used to drive the Y-axis of an X-Y recorder through a Keithley Model 610C Electrometer, while the variable G_2 voltage was used to drive the X-axis.

The intercept on the X-axis at which point the output starts to rise for a given fixed G_1 as G_2 is varied was used as a measure of the input threshold voltage. For the 7004 devices, a G_1 = 15V was used to establish a common reference for determining the threshold voltage (a straight line extrapolation was used to establish the intercept on the X-axis, thus avoiding the curvature of the characteristics close to cut-off). For the 7007 devices a G_1 = 1 volt was used to establish threshold value.

Displacement in the threshold voltage indicates the effects of charge buildup or decay in the dielectric of the input structure. Threshold changes reflect possible changes in charge handling capacity of a CCD and in distortion of the input transfer characteristics of a device.

Measurements of input transfer voltages of the CCD 321 devices were not made, as the circuitry on the chip was not amenable to direct measurement of the CCD output independent of the output stage circuitry on the chip.

2.3.7 Open/Short Test on Gates and Diodes

To verify the integrity of the dielectric under the CCD gates and the diode junctions, a open/short verification was made utilizing a Tektronix-type 575 curve tracer. The measurements were made with the vertical current sensitivity set at 0.01 ma/div and horizontal voltage set at 10 volts. Connections were:

CCD 321
Pin #8 = o.v.
All other pins (one at a time) to +10V.

7004

Pin #10 = ov.

Pins# 2 thru 9 and 11 thru 19 (one at a time) to - 10 V.

7007

Pin #24 = ov.

Pins#2, 3, 21, 40 (one at a time) to +10 V.

Also

Pin#24 = ov.

Pins#17, 18, 19, 20, 26, 27, 28, 37, 38 (one at a time) to - 10 V.

An indication of current of a fraction of one division was considered to represent defective dielectric for a gate structure or a leaky diode for a diode structure.

2.4 PACKAGE AMBIENT GAS ANALYSIS

2.4.1 Measurement Approach

The "mass spectrometer" is the general analytical instrument used for making a total analysis of gases in a semiconductor package. Water vapor, which is the constitutent of greatest concern, is also one of the most difficult gases to determine quantitatively. The scope of the problem has been reviewed recently at the ARPA/NBS Workshop on "Moisture Measurement Technology for Hermetic Semiconductor Devices", held March 22-23, 1978, at the National Bureau of Standards, Gaithersburg, Maryland. Specific problem areas include extraction of all the moisture from the package, incomplete and nonreproducible transport of water molecules through the spectrometer inlet system and interaction of water vapor with the ion source filament and/or impurities on surfaces in the source region. Various experimental techniques have been evolved to minimize these difficulties. For example the inlet system can be heated above 100^{o}C to improve the efficiency and reproducibility of water molecule transport through the inlet system. Comparison of measurements made by a number of mass spectrometers in some of the technical papers presented at the ARPA/NBS Workshop indicated that even with the various steps

taken to alleviate the experimental problems, measurements on ostensibly identical gas samples could produce wide variations in measured moisture content.

The problem of accurate and reproducible determination of the moisture content of hermetically sealed packages has been studied at the Westinghouse Research and Development Center. As a result of this study, a method of mass spectrometric moisture analysis has been developed by Carlson and Morgan[7]. Moisture is cryogenically concentrated and quantitatively converted to another gas, such as acetylene. The synthesized secondary gas can then be determined by routine gas mass spectrometric techniques with the advantage that it is not subject to the anomalies associated with the direct measurement of water vapor. The accuracy and reproducibility of the acetylene conversion method has been verified by analyzing nitrogen samples of known moisture content as determined by an Alnor Dewpoint Meter and by measuring the water content of hydrated salts of known water content when the water was driven off in a small furnace.

The essential features of the system used for moisture and total gas analysis of hermetic CCD devices for this program are shown in figure 26. The device is held in a mechanical stainless steel housing equipped with temperature monitoring and heating. The package is punctured by means of a needle attached to a valve stem. Calcium carbide is enclosed in a stainless steel tube which has provisions for both heating and cooling. Valves provide the various required pumping options. The system is miniaturized to facilitate the transfer of moisture from the device to the trap. The system is attached directly to the inlet system of the 21-104 Dupont mass spectrometer and its associated inlet pumping system is used to evacuate the drive and trap.

Preconditioning of the system for device analysis includes pumping and baking at 125°C for ½ - 1 hour, based on background

[7] G. L. Carlson and W. R. Morgan, Applied Spectroscopy, 31 nl, pp. 48-49 (Jan/Feb, 1977).

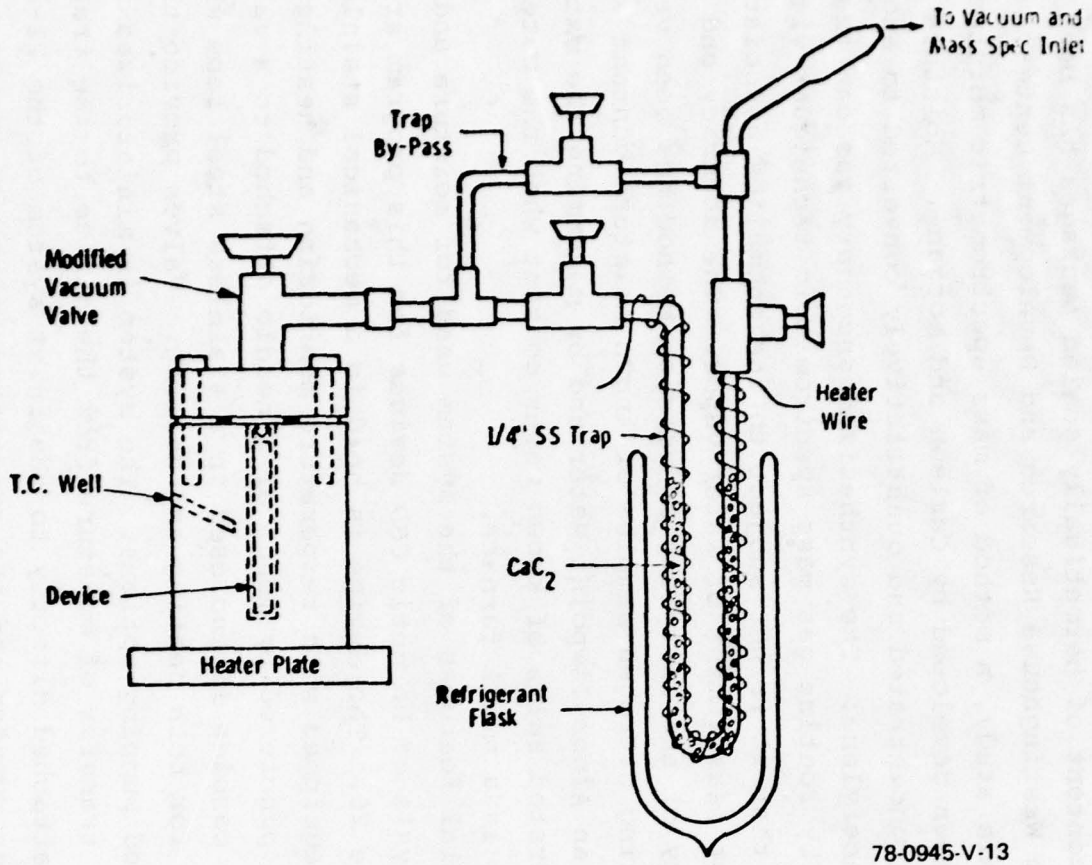


Figure 26. Trapping system for concentration and conversion of water to acetylene

monitoring. Prior to puncture of the package, the CaC_2 trap is cooled with liquid nitrogen. The device is punctured and the gas partitioned as to condensables at liquid nitrogen temperature. The condensables are retained in the trap and the noncondensables are measured as to quantity, are mass spectrometrically analyzed, and are pumped away. The trap is then warmed to 100°C for release of the gases and conversion of the moisture to acetylene. This fraction is measured, analyzed, and combined with the results of the noncondensable fraction to provide a total analysis. The calculations for water determinations allow for its conversion to acetylene, wherein one mole of water reacts to form 0.5 mole of acetylene.

2.4.2 CCD Device Package Sample Gas Analysis

The program required the package ambient gas analysis of samples of each device type and lot selected prior to application of any environmental stress. The samples of 7004 surface channel CCD device and 7007 peristaltic CCD devices were assembled each as an individual lot. The CCD321 buried channel CCD devices were purchased as a single lot. Two devices of each type were randomly selected from the samples available, subjected to a helium fine and a gross leak test to verify their hermeticity and sent to the Westinghouse R&D Center in Pittsburgh, Pennsylvania for gas analysis in which conversion of water vapor to acetylene was utilized.

In addition to the above samples, four additional samples were submitted for gas analysis to explore the effect of a high temperature polyimide die attach on the gas ambient in a semiconductor package. Polyimide die attach was considered as a possible means of preparing test samples in the second phase of the program but was ruled out because of outgasing uncertainties. Two samples labeled 5025-3311E-3-Eu and 5025-3311E-C3-Eu utilized eutectic die attach and gold wire thermocompression wire bonding. The other two samples, 5025-3311-C2 and 5025-2180-A4 utilized a polyimide die attach and aluminum ultrasonic wire bonding.

The specifice experimental procedure applied to the packages is as follows:

The package is placed in the sample holder and heated to 125°C under vacuum for 12 to 15 hours. This ensures a clean, dry environment in which the package will be opened. The package and holder are then held under vacuum and without pumping for two hours to check for system leaks, background interference, and possible package leaks. Showing no signs of leaks or contaminants, the package is opened using a special high vacuum valve which has had the valve seat removed and the valve stem fitted with a piece of sharpened and hardened drill rod. The drill rod punctures the package using the pressure provided by the valve drive.

The fill gas and internal contaminants are then passed through a liquid-nitrogen cold trap which contains CaC_2. The trap retains the moisture and the other impurities, while the fill gas passes on into the mass spectrometer for analysis. The package remains exposed to the cold trap for several hours to ensure the complete transfer of moisture to the trap. The trap is then isolated and heated to 125°C, causing the H_2O to react with the CaC_2. The resulting C_2H_2 is analyzed and used to determine the moisture content of the fill gas.

The results of the gas analysis is tabulated in table 1. These values are derived from a computer program which takes the raw mass spectrograph readings and calculates the constitutents by volume percent. Water vapor ranged from a low of 0.06 percent (600PPM) to a high of 0.51 percent (5100PPM). Samples 5025-3311-C2 and 5025-2180-A4, which utilized a high temperature polyimide die attach, indicated that sufficient organic matter was released from this die attach to produce a 1.5 percent gaseous hydrocarbon level in the package. It may be noted that one package, 5025-2180-A4 must have had a fine leak as evidenced by the presence of helium, oxygen and argon in the package. This leak probably was so small that the package passed the helium fine leak

test; however, an alternate possibility is that leak was of an intermittant nature.

Hydrogen is the major impurity found in the packages. The source of the hydrogen is not fully understood and should be further investigated. Potential sources of the hydrogen include the degassing of parts, decomposition of organics and the reaction of water in the formation of metallic oxides. Most analysis of packages by other laboratories have not included the measurement of hydrogen. Further studies to fully define the source (s) of hydrogen are recommended.

TABLE 1

GAS ANALYSIS OF ELECTRONIC PACKAGES

Sample ID	Total Gas Cm^3-torr	VOLUME OR MOLE%								
		H_2	CH_4	N_2	CO_2	H_2O (b)	O_2	Ar	He	HC (c)
321DC-1	15.7	5.32	0.29	92.94	1.21	0.07	-	-	-	0.15
321DC-12	15.7	2.26	0.15	97.10	0.33	0.09	-	-	-	0.06
7004-2685-A6	20.2	3.50	0.28	95.68	0.30	0.23	-	-	-	-
7004-2685-B6	24.9	6.76	2.23	90.07	0.32	0.51	-	-	-	0.10
7007-3425-7-15	21.7	3.67	0.26	95.83	0.11	0.06	-	-	-	0.07
7007-3425-7-8	23.3	2.75	0.38	96.15	0.27	0.35	-	-	-	0.10
5025-3311E-3-EU	19.2	3.36	0.18	95.54	0.76	0.16	-	-	-	-
5025-3311E-C3-EU	19.2	4.21	0.03	93.86	-	(a)	1.77	0.13	-	-
5025-3311-C2	18.1	3.96	0.82	90.45	2.97	0.30	-	-	-	1.5
5025-2180-A4	19.2	2.81	1.24	89.94	1.41	0.28	2.02	0.31	0.50	1.5

(a) No H_2O reported due to system leak following gas analysis. Leak accounts for O_2 in analysis.

(b) Minimum water detection limit is 0.02% which is equivalent to 4×10^{-6} grams.

(c) HC is hydrocarbons including C_2H_4 and acetone.

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3. LONG TERM LIFE TEST PROGRAM

3.1 TEST PLAN

The test plan for the long term (1000 hours) life test program evolved from the preliminary stress testing of a few representative components of the three device types selected for study. Initially, high temperature storage, high temperature dynamic stress, and high temperature bias stress life test conditions were considered. However, the preliminary tests indicated that high temperature storage was ineffective as a stress condition for producing degradation in CCD devices. Considering this fact along with the limitations imposed by component cost and test man-hours, high temperature storage was dropped as a stress condition for long term life tests. High temperature dynamic stress life and high temperature bias stress life were the test conditions used.

The stress temperatures chosen were 125^{o}C and 200^{o}C. The 125^{o}C temperature represents a MIL-STD test temperature and therefore is of interest as a bench mark. The 200^{o}C temperature was an estimate of where considerable acceleration of failure mechanisms can be expected without destroying the test samples in short order. This temperature is well above any expected operational temperature of the CCD's being studied. The CCD-321 has a 55^{o}C upper operational temperature limit and 100^{o}C storage temperature limit as specified by the manufacturer. The 7004 and 7007 are functional up to and at 125^{o}C.

The bias voltage stress test used applied 20* volts dc stress to all MIS gate structures and reverse bias at 20 volts to all appropriate p-n junctions. Dynamic voltages applied under stress

*(dc stress on CCD321 initially was started at 6V and then increased to 20V.)

testing was identical to the dynamic voltage used at room temperature for base line testing, 18 volt square wave levels for 7004 and 7007 devices and 16 volt square wave levels for CCD321.

The electrical stresses were applied to each device through a "load buffer". Series current limiting resistors of 3000 ohms were placed in each active stressing voltage lead to the device. In the eventuality that a component fails while under test by developing a short circuit, the series resistors in that device's lines prevents the voltage stress from being removed from the other components connected to the same voltage bus. Thus, the failure of one or several devices could not invalidate the life test on the other components being stressed. The clock rate for all devices under dynamic stress test was 1.0 MHz.

3.1.1 Long Term Life Test Plan for CCD-321 Buried Channel CCD

The long term life test plan for the CCD-321 is shown in figure 27. Three groups of seven devices were formed. One test cell of seven devices was subjected to dynamic stress at 125°C. A second group was subjected to dc bias stress at 125°C. The third group was subjected to dc bias stress at 200°C. Electrical measurements were taken initially and after 24, 168, 500, and 1000 hours of life stress time. Devices were cooled down to room temperature with electrical stress applied before they were removed from the temperature chamber for electrical testing at room temperature. In addition to the electrical measurements at the indicated times, an operational check was made at approximately 320, 670, and 840 hour points to determine whether a device had failed. This procedure required the cooling of the test chamber down to room temperature with electrical stress applied, and then measuring full cell capacity and transfer efficiency to verify that a device was functional. A complete set of parametric measurements were not taken at the check points. The object of this procedure was to reduce the time interval for detection of device failure.

The life test on the 125°C dc bias test cell of 7 devices was extended to a total of 1500 hours. This group initially was

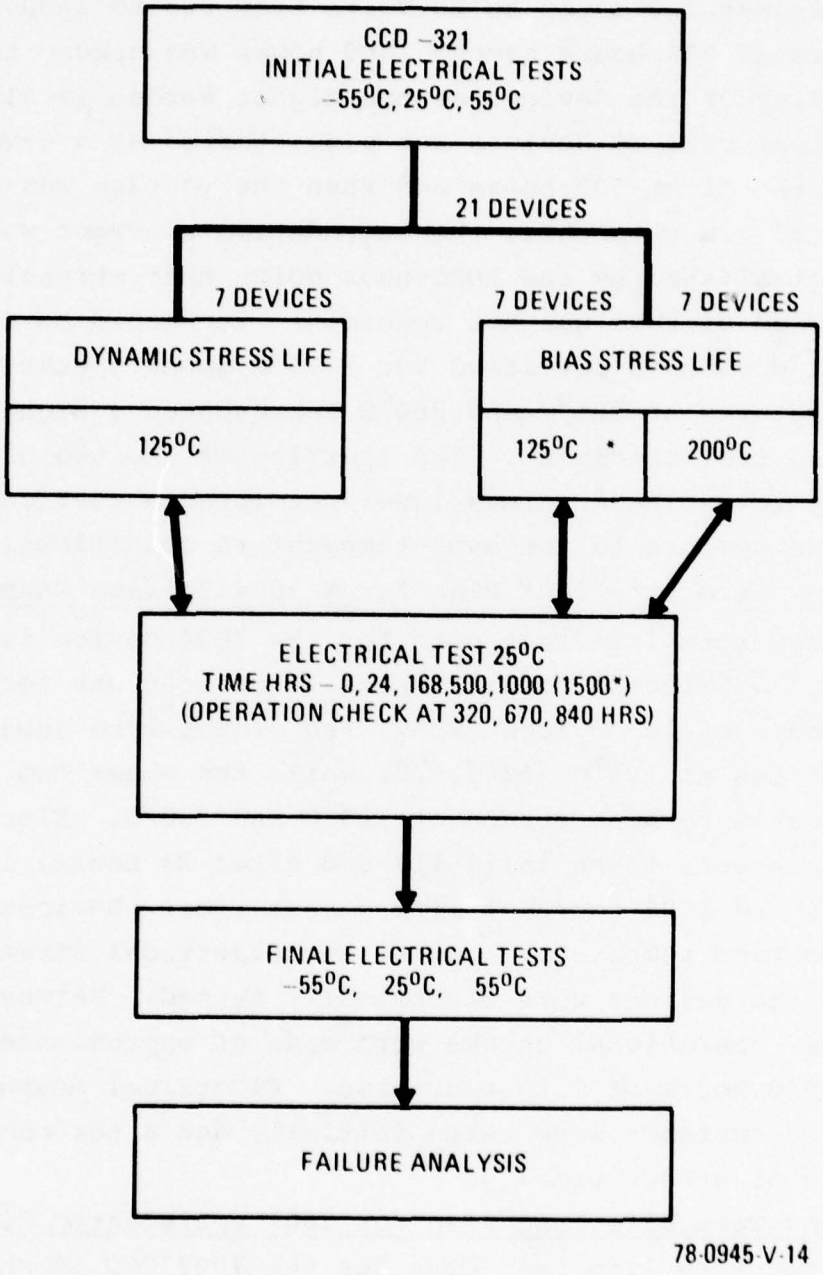


Figure 27. Long Term Life Plan for CCD-321

started at a 6-volt stress level for the first 863 hours and then the voltage was increased to 20 volts from 863 to 1500 hours. The additional 500 hours beyond 1000 hours was needed to verify the stability of the devices at the higher stress level. The 200°C dc test cell of devices was also started at a 6-volt stress level for the first 500 hours and then the voltage was increased to 20 volts. In this case, the degradation behavior was sufficiently established by the 1000-hour point that stressing for a longer period of time was not required. It should be noted that the CCD321 device is specified for a 55°C upper operating limit. The temperatures of 125°C and 200°C represented a significantly accelerated test condition. The starting of the two groups at a relatively low voltage stress level permitted a cautious evaluation of the devices to the over-temperature conditions.

3.1.2 Long Term Life Test Plan for W 7004 Surface Channel CCD

The long term life test plan for the 7004 device is shown in figure 28. A selected population of 40 devices was formed into 4 test groups of 10 devices each. Two groups were subjected to dynamic stress at 125°C and 200°C, while the other two groups were subjected to bias stress at 125°C and 200°C. Electrical measurements were taken initially and after 24 hours, 168 hours, 500 hours, and 1000 hours of life stress time. Devices were cooled down to room temperature before the electrical stress was removed and the devices were electrically tested. Between electrical test times, operational checks were made at approximately 320, 670, and 840 hours of life test time. Electrical measurements at temperature extremes were taken initially and after completion of 1000 hours of stress time.

3.1.3 Long Term Life Test Plan for 7007 Peristaltic CCD

The long term life test plan for the 7007 CCD is shown in figure 29. Only one test cell of 10 devices was used as the initial tests on the available devices disclosed that the majority of these devices had electrical defects and therefore were considered not suitable for life testing under accelerated stress

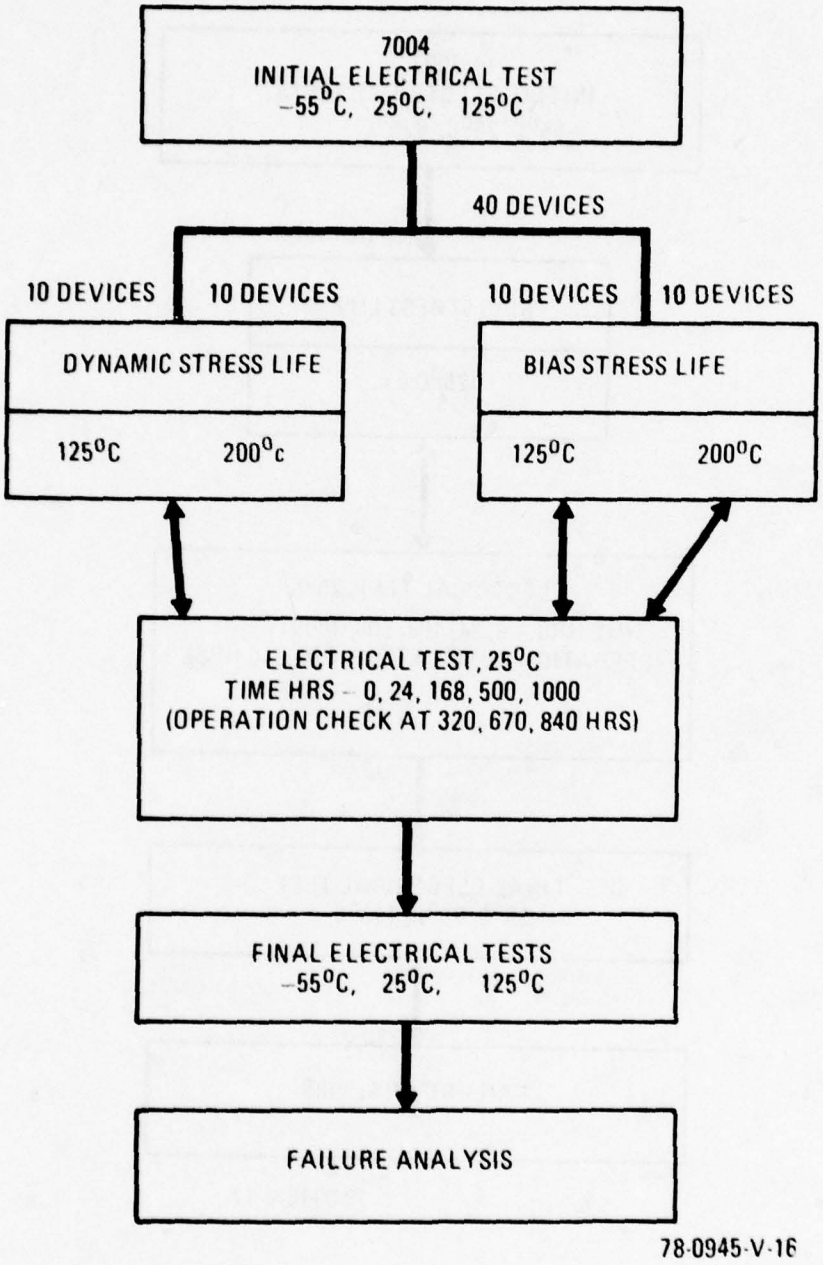


Figure 28. Long Term Life Test Plan for 7004 CCD Device

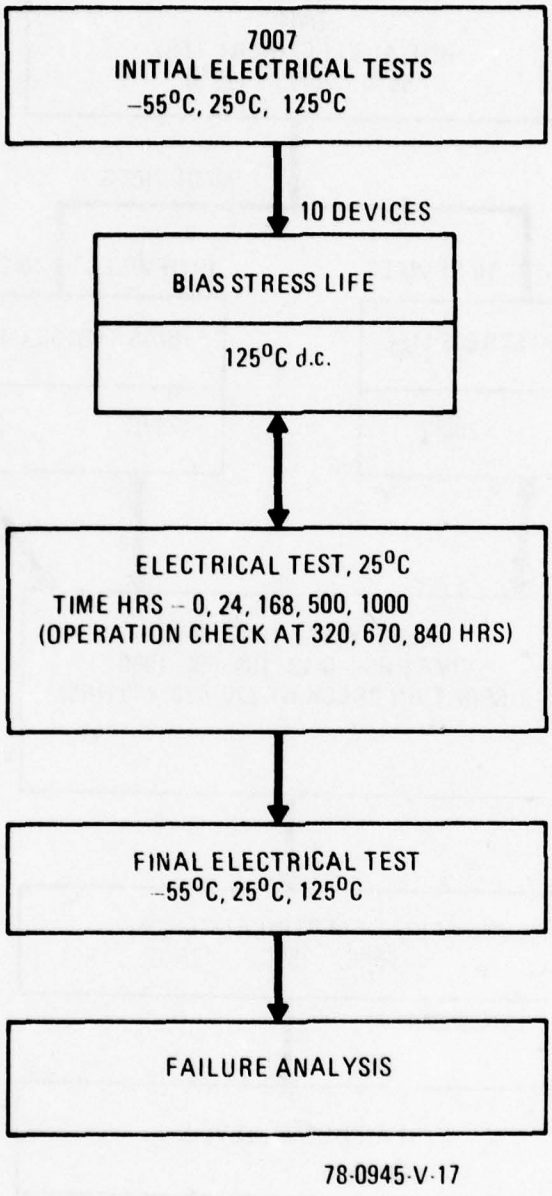


Figure 29. Long Term Life Test Plan for 7007 CCD Device

conditions. The one test cell was subjected to dc stress at 125°C. Electrical measurements were taken initially and after 24 hours, 168 hours; 500 hours, and 1000 hours of stress time. Between electrical test times, operational checks were made at approximately 320, 670, and 840 hours of test time. In all cases, the devices were cooled down to room temperature before the electrical stress was removed, and the devices were electrically tested. Electrical measurements at temperature extremes were taken initially and after completion of 1000 hours of stress test time.

3.2 SUMMARY OF ELECTRICAL TEST DATA

The electrical test data represented two different series of measurements. The standard room temperature measurements were made in a test socket mounted on the CCD exerciser PC board. All the life test data was taken using this configuration. The initial and final measurements at temperature extremes were taken on a teflon insulated extension cable (about 10 inches in length) which plugged into the test socket mounted on the CCD exerciser PC board and extended through a door port into a temperature chamber so that the test socket on end of the extension cable was several inches inside the test chamber and away from any walls. There were some small discrepancies between the measurements on the exerciser board and measurements on the extension cable. As a result, room temperature measurements were taken in the temperature chamber in addition to the high and low temperature measurements. Two independent sets of measurements were thus made and are presented in section 3.2.1 and 3.2.2. Each test point represents the mean and standard deviation of the measurements taken for each test group. Initially this represented a sample size of ten 7004 and 7007 devices and seven CCD321 devices. However, as stressing progressed and some devices fell out due to catastrophic failure, the sample size represented the actual number of surviving devices. The general criteria used was once a device failed it was considered a failure from that point on even though it may have recovered under additional stress. In

the case of the 7007 devices, the entire group failed after the initial 24 hours of stress. The tabulated data represents the mean and standard deviation of devices that provided measurable parameters. The values for the 7007 device beyond the initial reading are included for general information.

3.2.1 Life Test Data

The following tables present the summary of the mean and standard deviation of all the data for the test groups life tested.

Table 2, CCD321, 125°C, dc, Test Group
Table 3, CCD321, 125°C, dynamic, Test Group
Table 4, CCD321, 200°C, dc, Test Group
Table 5, 7004, 125°C, dc, Test Group
Table 6, 7004, 125°C, dynamic, Test Group
Table 7, 7004, 200°C, dc, Test Group
Table 8, 7004, 200°C, dynamic, Test Group
Table 9, 7007, 125°C, dc, Test Group

3.2.2 Parameters at Temperature Extremes

The following 8 tables present the summary of the mean and standard deviation of initial and final data taken at room temperature and at temperature extremes.

Table 10, CCD321, 125°C, dc, (-55, 25, 55°C)
Table 11, CCD321, 125°C, dynamic, (-55, 25, 55°C)
Table 12, CCD321, 200°C, dc, (-55, 25, 55°C)
Table 13, 7004, 125°C, dc, (-55, 25, 125°C)
Table 14, 7004, 125°C, dynamic, (-55, 25, 125°C)
Table 15, 7004, 200°C, dc, (-55, 25, 125°C)
Table 16, 7004, 200°C, dynamic, (-55, 25, 125°C)
Table 17, 7007, 125°C, dc, (-55, 25, 125°C)

3.3 FAILURE ANALYSIS

3.3.1 CCD321 Devices

None of the CCD321 devices failed catastrophically during the life tests. This clearly indicated that the manufacturer's screen effectively removed all early failures from the group of 21 devices stressed in the study. Degradation of transfer

TABLE 2

CCD 321, 125°C, dc TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0 % F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range $(f_1 - 2f_1)$ dB	Cumulative % Failure
0	(mean)	1.83	0.9990	0.9999	37	−13.7	47.3	0
	(S.D.)	0.13	0.0002	0.0000	25	0.5	1.3	
24	(mean)	1.81	0.9990	0.9999	31	−13.8	--	0
	(S.D.)	0.16	0.0002	0.0000	21	0.6		
168	(mean)	1.78	0.9989	0.9999	35	−13.7	--	0
	(S.D.)	0.22	0.0002	0.0000	25	2.1		
500	(mean)	1.81	0.9988	0.9999	34	−13.0	--	0
	(S.D.)	0.13	0.0002	0.0000	23	2.3		
1000	(mean)	1.82	0.9989	0.9998	37	−12.7	--	0
	(S.D.)	0.13	0.0001	0.0000	23	0.6		
1500	(mean)	1.84	0.9987	0.9998	44	−11.6	53.1	0
	(S.D.)	0.13	0.0002	0.0001	32	1.0	2.1	

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TABLE 3

CCD321, 125°C, DYNAMIC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0% F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range ($f_1 - 2f_1$) dB	Cumulative % Failure
0	(mean)	1.78	0.9991	0.9999	73	–13.6	47.6	
	(S.D.)	0.14	0.0002	0.0000	64	0.5	1.2	0
24	(mean)	1.78	0.9989	0.9999	71	–13.9	–	
	(S.D.)	0.13	0.0001	0.0000	68	0.4		0
168	(mean)	1.78	0.9988	0.9999	86	–12.4	–	
	(S.D.)	0.14	0.0003	0.0000	74	1.3		0
500	(mean)	1.80	0.9988	0.9999	68	–12.1	–	
	(S.D.)	0.15	0.0001	0.0000	65	1.3		0
1000	(mean)	1.78	0.9989	0.9999	67	–12.1	51.5	
	(S.D.)	0.14	0.0001	0.0000	61	1.2	0.9	0

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TABLE 4

CCD321, 200°C, DC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0 % F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range $(f_1 - 2f_1)$ dB	Cumulative % Failure
0	(mean)	1.75	0.9991	0.9999	34	-13.7	45.0	
	(S.D.)	0.20	0.0002	0.0000	16	0.5	3.1	0
24	(mean)	1.81	0.9989	0.9999	40	-13.8	–	
	(S.D.)	0.15	0.0002	0.0000	20	0.4		0
168	(mean)	1.85	0.9988	0.9999	36	-13.4	–	
	(S.D.)	0.16	0.0002	0.0000	18	2.8		0
500	(mean)	1.83	0.9988	0.9999	44	-13.4	–	
	(S.D.)	0.15	0.0002	0.0000	23	2.6		0
1000	(mean)	1.94	0.9953	0.9968	47	-31.2	47.2 (Annealed)	
	(S.D.)	0.13	0.0006	0.0004	20	5.0	3.6	0

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TABLE 5

7004, 125°C, DC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0% F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range $(f_1 - 2f_1)$ dB	G2 Threshold V (G1 = 15V	Cumulative % Failures
0	(mean)	0.66	0.9971	0.9988	119	-25.9	43.0	149	
	(S.D.)	0.14	0.0012	0.0006	234	1.3	1.3	0.2	0
24	(mean)	0.51	0.9986	0.9994	93	-31.1	--	14.7	
	(S.D.)	0.14	0.0005	0.0003	179	1.7	--	0.2	0
168	(mean)	0.46	0.9985	0.9995	45	-28.9	--	14.7	
	(S.D.)	0.13	0.0004	0.0001	65	2.5	--	0.2	30
500	(mean)	0.63	0.9983	0.9993	79	-24.2	--	14.8	
	(S.D.)	0.13	0.0006	0.0003	43	2.1	--	0.3	40
1000	(mean)	0.58	0.9983	0.9994	80	-29.0	40.2	14.9	
	(S.D.)	0.08	0.0005	0.0003	40	1.4	1.7	0.1	40

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TABLE 6

7004, 125°C, DYNAMIC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0% F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range (f_1-2f_1) dB	G2 Threshold V (G1 = 15V)	Cumulative % Failures
0	(mean)	0.59	0.9990	0.9995	30	-26.1	44	15.6	
	(S.D.)	0.09	0.0005	0.0006	9	2.1	1.9	0.6	0
24	(mean)	0.63	0.9984	0.9992	416	-29.5	--	14.7	
	(S.D.)	0.09	0.0006	0.0006	749	1.9	--	0.2	0
168	(mean)	0.56	0.9986	0.9990	2550	-27.6	--	14.7	
	(S.D.)	0.17	0.0007	0.0011	4631	2.9	--	0.1	10
500	(mean)	0.51	0.9977	0.9990	2897	-26.4	--	14.8	
	(S.D.)	0.13	0.0026	0.0012	5089	2.2	--	0.2	10
1000	(mean)	0.61	0.9979	0.9989	1825	-25.7	45	14.7	
	(S.D.)	0.11	0.0010	0.0009	2893	1.4	3.7	0.3	10

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TABLE 7

7004, 200°C, DC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0 % F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range (f_1-2f_1) dB	G2 Threshold V (G1 = 15V)	Cumulative % Failures
0	(mean)	0.57	0.9984	0.9994	55	−26.1	43.7	15.6	
	(S.D.)	0.11	0.0007	0.0005	45	1.7	3.9	0.2	0
24	(mean)	0.43	0.9976	0.9986	63	−32.9	–	14.6	
	(S.D.)	0.16	0.0015	0.0008	87	3.2	–	0.1	0
168	(mean)	0.56	0.9969	0.9988	59	−27.7	–	14.7	
	(S.D.)	0.13	0.0020	0.0009	62	1.8	–	0.1	0
500	(mean)	0.56	0.9972	0.9987	81	−26.2	–	14.7	
	(S.D.)	0.11	0.0016	0.0008	65	1.9	–	0.2	0
1000	(mean)	0.57	0.9966	0.9984	122	−26.4	39.6	14.8	
	(S.D.)	0.11	0.0018	0.0011	94	1.8	5.1	0.1	0

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TABLE 8

7004, 200°C, DYNAMIC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 0 % F.Z.	Transfer Efficiency 10% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range $(f_1 - 2f_1)$ dB	G2 Threshold V (G1 = 15V)	Cumulative % Failure
0	(mean)	0.58	0.9990	0.9997	44	-25.6	44.2	15.5	
	(S.D.)	0.11	0.0003	0.0001	35	1.1	1.3	0.2	0
24	(mean)	0.54	0.9971	0.9985	20	-34.3	–	14.8	
	(S.D.)	0.09	0.0014	0.0005	30	4.5	–	0.2	40
168	(mean)	0.70	0.9982	0.9991	425	-25.2	–	–	
	(S.D.)	0.11	0.0005	0.0003	503	1.6	–	–	50
500	(mean)	0.62	0.9974	0.9985	194	-25.0	–	15.0	
	(S.D.)	0.12	0.0009	0.0008	175	1.2	–	0.2	50
1000	(mean)	0.59	0.9970	0.9982	204	-26.8	44.6	15.0	
	(S.D.)	0.08	0.0014	0.0013	121	3.0	0.9	0.2	50

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TABLE 9

7007, 125°C, DC TEST GROUP

Time Hours		$V_{Full\ Well}$ Volts	Transfer Efficiency 25% F.Z.	Dark Current nA/cm^2	Insertion Loss dB, f_1 = 225 kHz	Dynamic Range ($f_1 - 2f_1$) dB	G2 Threshold (G1 = 1V)	Cumulative % Failures
0	(mean)	2.13	0.9903	604	-14.3	35.1	1.1	
	(S.D.)	0.67	0.0060	1113	6.4	5.7	1.1	0
24	(mean)	0.63	0.9903	472	-27.7	31.7	2.4	
	(S.D.)	0.35	0.0037	698	6.9	6.4	0.9	–
168	(mean)	1.4	0.9915	917	-21.4	31.6	2.4	
	(S.D.)	0.8	0.0037	1597	7.5	4.4	1.1	–
500	(mean)	0.36	0.9890	811	-28.2	26.2	2.24	
	(S.D.)	0.05	0.0035	1667	6.3	3.0	1.2	–
1000	(mean)	0.35	0.9872	373	-31.8	21.4	2.12	
	(S.D.)	0.07	0.0038	258	6.6	3.9	1.2	–

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TABLE 10

CCD321, 125°C, DC GROUP

		Time = 0 Hrs			Time = 1500 Hrs		
		−55°C	25°C	55°C	−55°C	25°C	55°C
$V_{Full\ Well}$ Volts	(mean)	1.78	1.77	1.76	1.79	1.83	1.81
	(S.D.)	0.17	0.14	0.13	0.19	0.13	0.13
Trans. Eff. 0% F.Z.	(Mean)	0.9989	0.9994	0.9992	0.9988	0.9989	0.9990
	(S.D.)	0.0004	0.0002	0.0002	0.0005	0.0004	0.0002
Trans. Eff. 10% F.Z.	(Mean)	0.9999	0.9999	0.9998	0.9998	0.9998	0.9997
	(S.D.)	0.0000	0.0000	0.0000	0.0001	0.0001	0.0001
Dark Current nA/cm^2	(Mean)	< 1	35	230	< 1	36	221
	(S.D.)	–	19	85	–	22	98
Insertion Loss dB	(Mean)	−14.5	−14.1	−14.1	−12.5	−11.9	−11.8
	(S.D.)	0.5	0.3	0.3	1.5	1.0	1.1
Dynamic Range dB	(Mean)	45.9	44.9	46.1	48.3	49.8	51
	(S.D.)	0.6	4.7	0.5	2.9	3.5	3.9

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TABLE 11

CCD321, 125°C, DYNAMIC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		−55°C	25°C	55°C	−55°C	25°C	55°C
$V_{Full\ Well}$ Volts	(Mean)	1.72	1.74	1.74	1.72	1.77	1.74
	(S.D.)	0.23	0.16	0.17	0.22	0.17	0.15
Trans. Eff. 0% F.Z.	(Mean)	0.9989	0.9992	0.9992	0.9988	0.9986	0.9989
	(S.D.)	0.0004	0.0004	0.0002	0.0003	0.0005	0.0004
Trans. Eff. 10% F.Z.	(Mean)	0.9999	0.9999	0.9998	0.9999	0.9999	0.9998
	(S.D.)	0.0000	0.0000	0.0001	0.0000	0.0000	0.0001
Dark Current nA/cm^2	(Mean)	< 1	63	260	< 1	61	264
	(S.D.)	–	56	76	–	57	84
Insertion Loss dB	(Mean)	−14.4	−14.0	−14.0	−11.7	−11.6	−11.1
	(S.D.)	0.6	0.0	0.0	1.1	1.1	1.1
Dynamic Range dB	(Mean)	46.0	45.9	46.1	51.0	52.2	51.9
	(S.D.)	0.6	1.3	0.3	2.9	2.2	1.6

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TABLE 12

CCD321, 200°C, DC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		−55°C	25°C	55°C	−55°C	25°C	55°C
$V_{Full\ Well}$ Volts	(Mean)	1.75	1.74	1.69	1.95	1.94	1.93
	(S.D.)	0.18	0.15	0.16	0.16	0.13	0.13
Trans. Eff. 0% F.Z.	(Mean)	0.9989	0.9993	0.9992	0.9957	0.9955	0.9956
	(S.D.)	0.0004	0.0003	0.0003	0.0007	0.0004	0.0005
Trans. Eff. 10% F.Z.	(Mean)	0.9999	0.9999	0.9998	0.9971	0.9968	0.9969
	(S.D.)	0.0000	0.0000	0.0001	0.0006	0.0004	0.0004
Dark Current nA/cm^2	(Mean)	< 1	33	235	< 1	48	331
	(S.D.)	–	13	94	–	18	80
Insertion Loss dB	(Mean)	−14.4	−14.0	−14.0	−31.3	−31.1	−31.2
	(S.D.)	0.7	0.4	0.4	5.3	5.2	5.1
Dynamic Range dB	(Mean)	46.0	44.8	45.9	46.5	45.8	45.1
	(S.D.)	0.9	4.0	0.9	1.9	1.4	1.3

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TABLE 13

7004, 125°C DC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		−55°C	25°C	125°C	−55°C	25°C	125°C
$V_{Full\ Well}$ Volts	(mean)	0.87	0.66	0.47	0.82	0.62	0.44
	(S.D.)	0.17	0.14	0.11	0.14	0.10	0.09
Trans. Eff. 0% F.Z.	(mean)	0.9971	0.9971	0.9983	0.9974	0.9972	0.9984
	(S.D.)	0.0014	0.0012	0.0009	0.0009	0.0009	0.0007
Trans. Eff. 10% F.Z.	(mean)	0.9988	0.9988	0.9991	0.9988	0.9987	0.9991
	(S.D.)	0.0006	0.0006	0.0005	0.0006	0.0005	0.0005
Dark Current nA/cm^2	(mean)	145	147	25,984	38.0	78	32,103
	(S.D.)	169	227	8,528	50.2	42	9,418
Insertion Loss dB	(mean)	−24.0	−25.9	−28.3	−23.7	−26	−28.2
	(S.D.)	1.3	1.3	1.6	1.3	1.6	1.2
Dynamic Range dB	(mean)	38.8	43	45.5	41.3	43.2	45.8
	(S.D.)	2.9	1.3	1.3	5.3	1.0	2.3
Threshold Input Gates	(mean)	14.8	14.9	15.0	14.6	14.8	14.8
	(S.D.)	0.3	0.2	0.2	0.1	0.3	0.2

78-0945-T-29

TABLE 14

7004, 125°C DYNAMIC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		-55°C	25°C	125°C	-55°C	25°C	125°C
$V_{Full\ Well}$ Volts	(mean)	0.88	0.67	0.47	0.75	0.63	0.44
	(S.D.)	0.16	0.14	0.10	0.27	0.16	0.10
Trans. Eff. 0% F.Z.	(mean)	0.9962	0.9964	0.9977	0.9975	0.9968	0.9980
	(S.D.)	0.0027	0.0011	0.0015	0.0011	0.0014	0.0012
Trans. Eff. 10% F.Z.	(mean)	0.9983	0.9982	0.9982	0.9984	0.9983	0.9986
	(S.D.)	0.0010	0.0011	0.0016	0.0008	0.0010	0.0014
Dark Current nA/cm^2	(mean)	17.2	31	25,548	2087	2177	33,781
	(S.D.)	15.2	17	5,480	3533	3496	7,601
Insertion Loss dB	(mean)	-23.8	-26	-28.7	-23.9	-25.9	-28.2
	(S.D.)	1.5	1.7	1.7	1.9	1.7	1.4
Dynamic Range dB	(mean)	40.8	44.4	46.1	42.7	43.9	45.9
	(S.D.)	4.2	2.3	1.7	4.4	4.3	4.4
Threshold Input Gate	(mean)	14.7	14.8	15.1	14.7	14.7	14.8
	(S.D.)	0.2	0.2	0.4	0.3	0.3	0.2

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TABLE 15

7004, 200°C DYNAMIC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		−55°C	25°C	125°C	−55°C	25°	125°C
$V_{Full\ Well}$ Volts	(mean)	0.88	0.67	0.46	0.73	0.63	0.42
	(S.D.)	0.18	0.15	0.10	0.20	0.11	0.07
Trans. Eff. 0% F.Z.	(mean)	0.9973	0.9965	0.9982	0.9969	0.9962	0.9976
	(S.D.)	0.0012	0.0023	0.0009	0.0026	0.0020	0.0011
Trans. Eff. 10% F.Z.	(mean)	0.9986	0.9986	0.9991	0.9978	0.9979	0.9985
	(S.D.)	0.0008	0.0005	0.0005	0.0027	0.0014	0.0007
Dark Current nA/cm^2	(mean)	59.5	81.3	28412	94.4	200	43,375
	(S.D.)	76.9	98.3	8924	112.2	153	8158
Insertion Loss dB	(mean)	−23.7	−25.8	−28.3	−23.6	−26.1	−28.7
	(S.D.)	1.1	1.4	1.6	0.7	0.6	1.0
Dynamic Range	(mean)	40	43.9	45.8	46.0	35.4	44.2
	(S.D.)	2	0.9	1.1	2.4	2.9	4.6
Threshold Input Gates	(mean)	14.7	14.9	15.0	14.8	15.0	14.9
	(S.D.)	0.3	0.2	0.2	0.3	0.2	0.2

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TABLE 16

7004, 200°C, DC GROUP

		Time = 0 Hrs			Time = 1000 Hrs			
		-55°C	25°C	125°C	-55°C	25°C	125°C	Units
$V_{Full\ Well}$	(mean)	0.85	0.65	0.45	0.85	0.67	0.41	Volts
	(S.D.)	0.16	0.14	0.11	0.19	0.16	0.09	S.D.
Trans. Eff. 0% F.Z.	(mean)	0.9951	0.9962	0.9978	0.9956	0.9953	0.9996	%
	(S.D.)	0.0045	0.0017	0.0011	0.0025	0.0023	0.0015	S.D.
Trans. Eff. 10% F.Z.	(mean)	0.9982	0.9982	0.9988	0.9977	0.9998	0.9984	%
	(S.D.)	0.0009	0.0010	0.0009	0.0011	0.0012	0.0017	S.D.
Dark Current nA/cm^2	(mean)	75.5	85.8	26,833	67.2	136.3	52,125	nA/cm^2
	(S.D.)	130	110	8,341	68.5	120.5	23,034	S.D.
Insertion Loss dB	(mean)	-26.3	-26.3	-29	-24.4	-26.4	-28.7	dB
	(S.D.)	5.5	1.8	1.6	1.8	1.8	1.3	S.D.
Dynamic Range dB	(mean)	38.7	43.8	45.4	40.5	41.8	43.6	dB
	(S.D.)	6.6	4.2	2.3	4.0	3.7	5.3	S.D.
Threshold Input Gates	(mean)	14.7	14.9	14.9	14.5	14.8	14.8	Volts
	(S.D.)	0.2	0.1	0.2	0.1	0.1	0.1	S.D.

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TABLE 17

7007, 125°C, DC GROUP

		Time = 0 Hrs			Time = 1000 Hrs		
		−55°C	25°C	125°C	−55°C	25°C	125°C
$V_{Full\ Well}$ Volts	(mean)	2.30	1.85	1.46	0.85	0.55	0.50
	(S.D.)	0.83	0.77	0.71	0.7	0.19	0.40
Trans. Eff. 25% F.Z.	(mean)	0.9944	0.9144	0.9941	0.9924	0.9921	0.9930
	(S.D.)	0.0009	0.0013	0.0010	0.0012	0.0023	0.0024
Dark Current nA/cm^2	(mean)	61,572	94,887	106,793	33,165	6,083	60,255
	(S.D.)	83,708	70,785	48,120	12,995	12,995	68,551
Insertion Loss dB	(mean)	−15.2	−17.8	−20.9	−30.8	−32.2	−28.5
	(S.D.)	4.5	3.9	3.8	10.0	8.8	10.1
Dynamic Range dB	(mean)	35.7	33.6	38.7	23.1	23.2	22.7
	(S.D.)	4.9	4.4	2.2	7.0	7.0	8.5
Threshold Input Gates (G1 = 1V)	(mean)	−1.5	−2.4	−1.5	−2.3	−1.35	−1.8
	(S.D.)	0.8	0.7	0.6	0.2	0.96	1.2

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efficiency of devices stressed at 200°C is discussed in section 3.4.

3.3.2 7004PI Devices

Ten devices failed out of a total of 40 devices life tested in 4 test groups of 10 devices each. All but one of the failed devices recovered under a 24-hour bake at 125°C with pins shorted. Stressing of these devices was continued for a total of 1000 hours; however, they were counted as failures and their data was not included in the cumulative results. Deliding and microscopic examination of the 10 failed devices disclosed that all failed because of a dielectric defect at a point between a metal line and the underlying silicon substrate or polysilicon gate. The nine devices that recovered, cleared the fault by melting away the aluminum metallization around the dielectric pinhole defect. Figures 30 thru 38 are photographs of the failures taken at 400X. The tenth device which did not recover, suffered a fused-open input diode lead. It appeared that a dielectric fault at the point where the metal line crossed over an isolation junction was responsible for the fault. Figure 38 is a micrograph of the

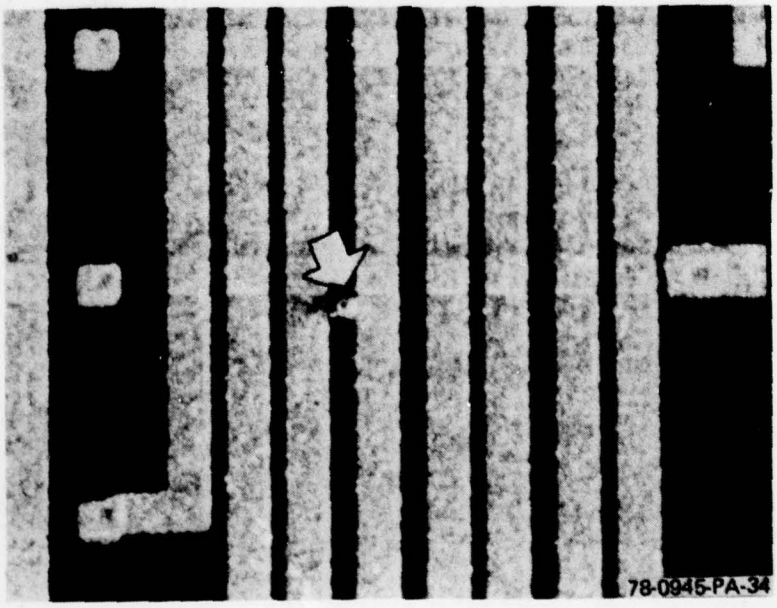


Figure 30. Dielectric Puncture Point on Device 7004-B7

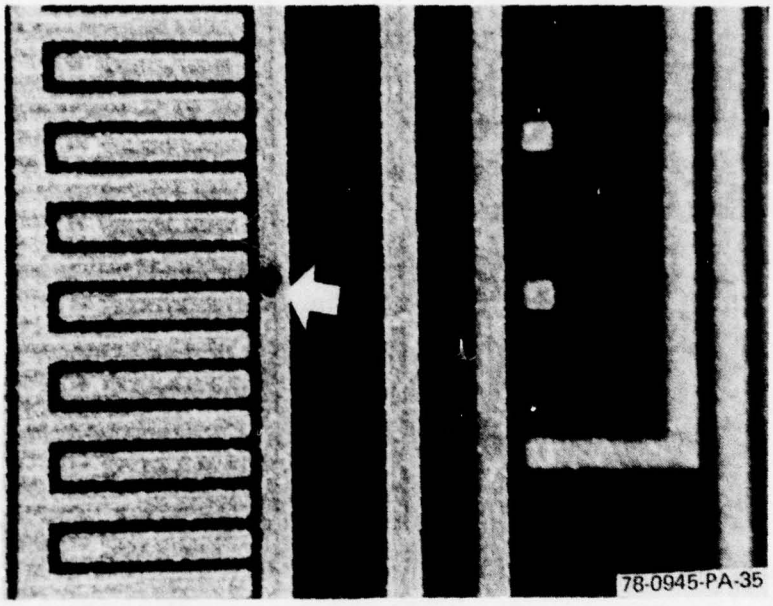


Figure 31. Dielectric Puncture Point on Device 7004-C1

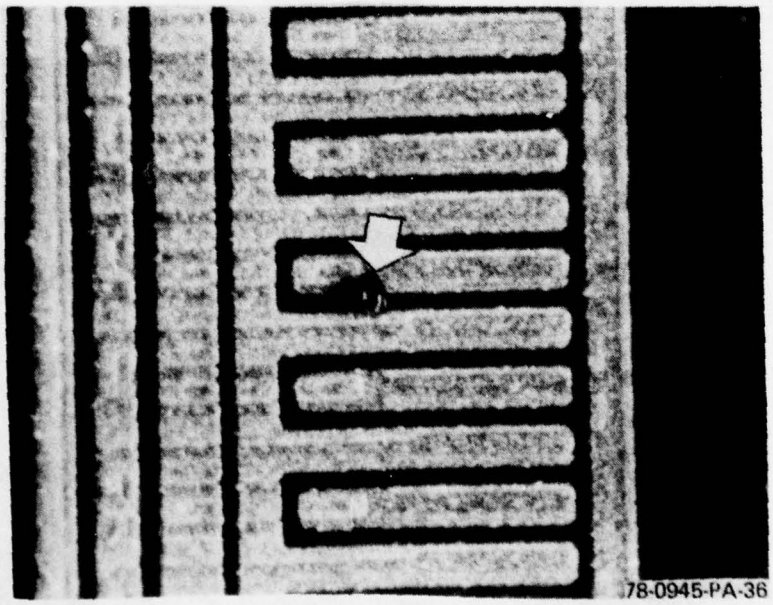
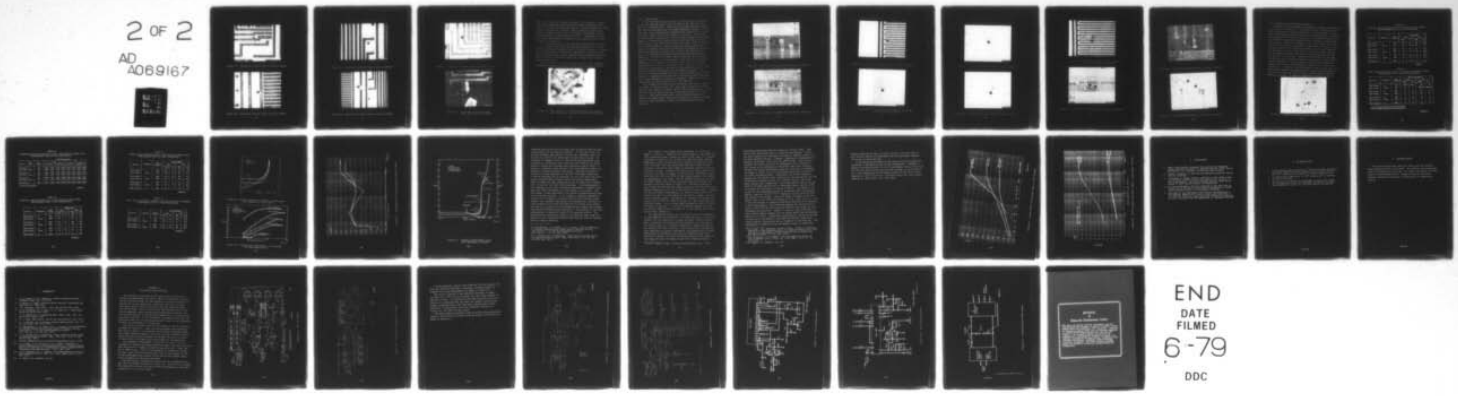


Figure 32. Dielectric Puncture Point on Device 7004-B15

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DEGRADATION ANALYSIS OF CCD/CID DEVICES.(U)
APR 79 J W DZIMIANSKI, G M BORSUK F30602-77-C-0037
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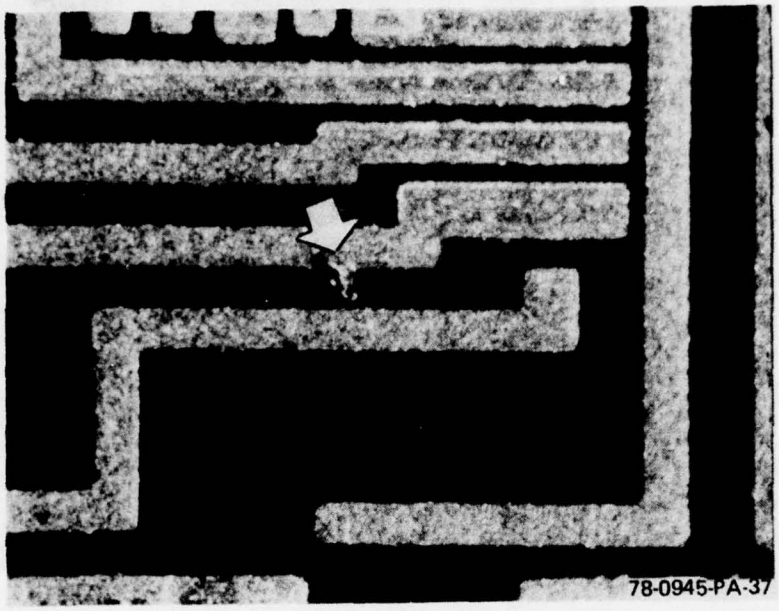


Figure 33. Dielectric Puncture Point on Device 7004-B5

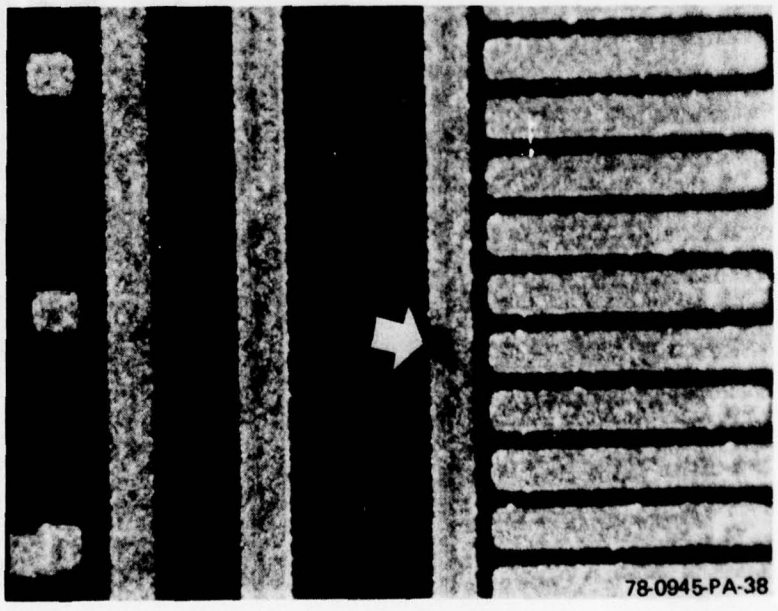


Figure 34. Dielectric Puncture Point on Device 7004-C3

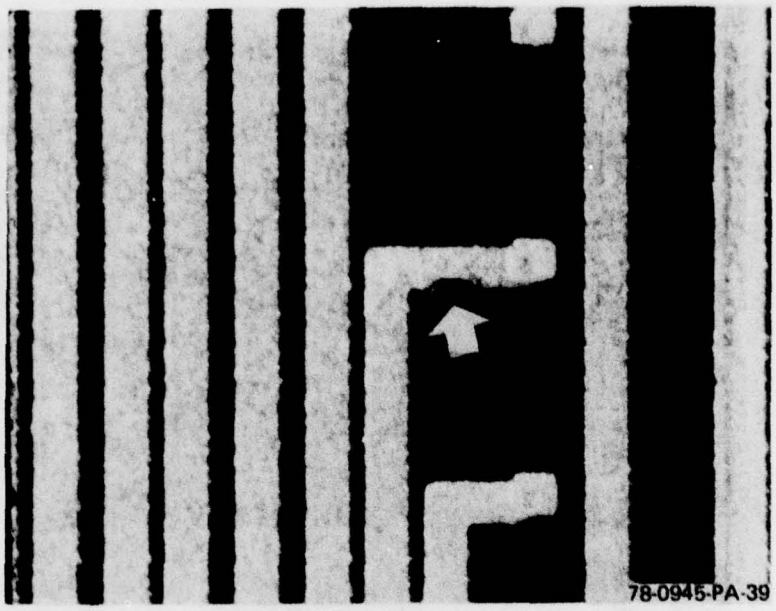


Figure 35. Dielectric Puncture Point on Device 7004-B11

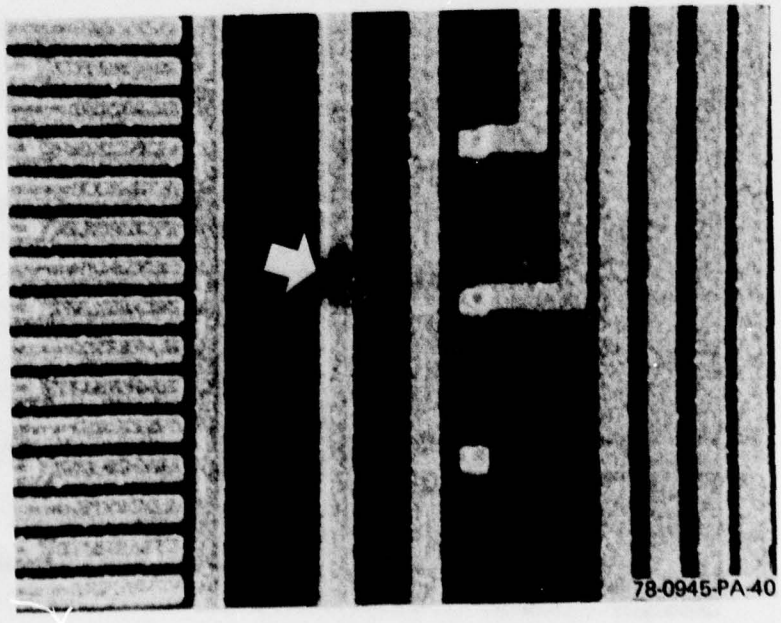


Figure 36. Dielectric Puncture Point on Device 7004-B14

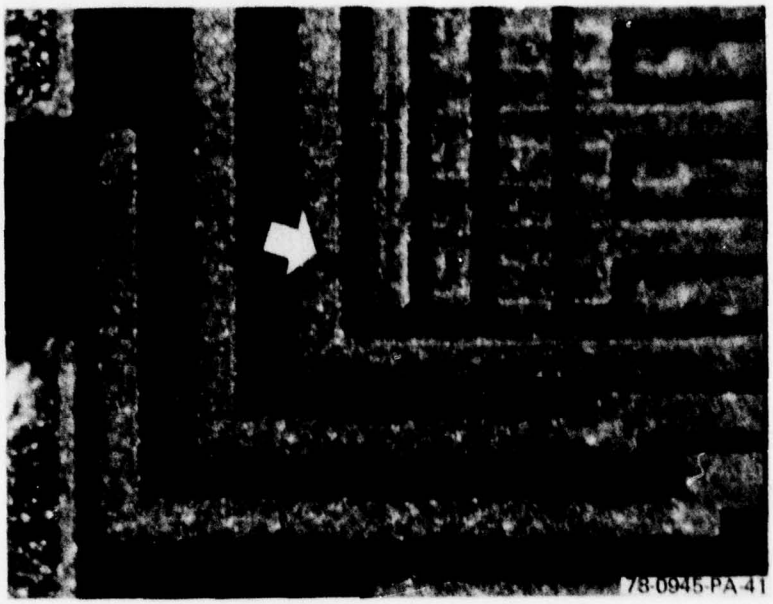


Figure 37. Dielectric Puncture Point on Device 7004-C2

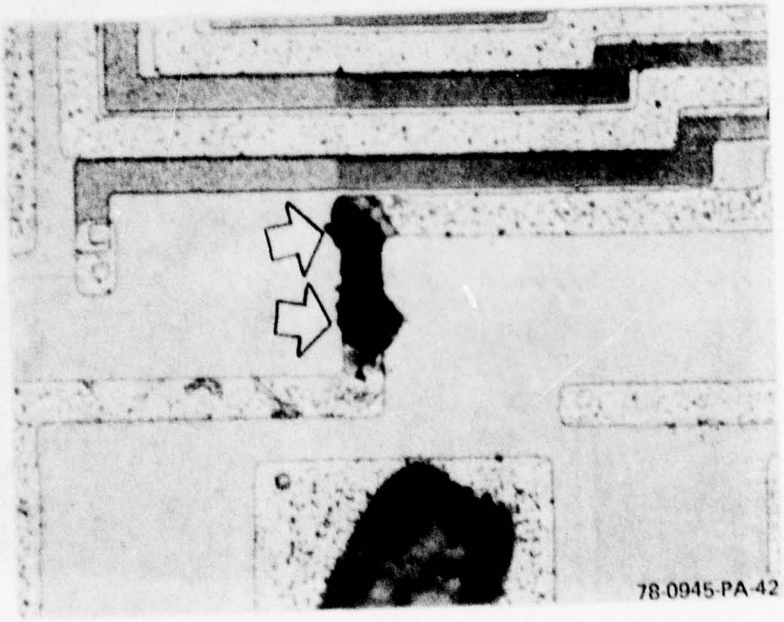


Figure 38. Fused Open Section of Input Diode Lead on Device 7004-A16

area. The silox overcoat was stripped off the chip by etching and then an aluminum etch was used to remove the metallization line in an effort to expose the defect. The fused aluminum, which reacted with the SiO_2, formed a mass of material that was not readily etchable in the fault area without completely removing the surrounding SiO_2 and defect evidence. A scanning electron microscopic photograph at 10,000X of the vicinity of the defect is shown in figure 39.

It is reasonably clear from the above information that dielectric defects occuring in the fabrication process of the 10 failed devices were responsible for the device failures. All but one failure occurred in the first 168 hours of stress testing which indicates that a normal 168-hour burn-in screen would have been effective in removing almost all of those early failures from the population.

The two groups of devices stressed at 200°C also exhibited parametric degradation similar to the CCD321 devices at 200°C.



Figure 39. SEM (10,000X) of Dielectric Defect Area Causing Input Diode Lead on Device 7004-A16 to Fuse Open

3.3.3 7007 Devices

Of the ten 7007 devices tested, five devices were functional at all the test and check points at time 0, 24, 168, 320, 500, 670, 840, and 1000 hours. These five functional devices however, did indicate that some sort of problem existed by virtue of the full well (V_{FW}) voltage being substantially lower at all measurement times after the initial reading at time zero. At the end of 1000 hours of stress, all 10 devices were delided and analyzed. However, self-healing permitted some of the devices to recover sufficiently to be functional at the test times. Five of the devices showed evidence of being damaged by voltage overstress (static discharge), four devices indicated breakdown at dielectric point defects, and one device had a silicon epi defect at the edge of an isolation diffusion which broke down the isolation junction. In view of the above observations and the fact that V_{FW} and "insertion loss" measurements indicated significant degradation of the working 7007 devices after the first 24-hour stress period, it must be concluded that all the devices were failures at this point. The lack of input protection on the 7007 device makes it very sensitive to overvoltage failure. Also, no burn-in screen was used to remove early failures from the population of samples, which came from a process lot that apparently had a high incidence of dielectric pinholes. These two factors invalidated the test results on the 7007 devices.

Micrographs of the ten devices indicating the failure points are shown in figures 40 thru 49. The oxide overcoat and metallization was etched off device 7007-6-5 and an SEM picture, figure 50, was taken at 2500X locating the puncture point in the dielectric. This chip showed both a high voltage breakdown path (which came first) and a dielectric puncture at a dielectric weak point in close proximity to where the high voltage breakdown occurred.



Figure 40. High Voltage Breakdown Path on Device 7007-7-9

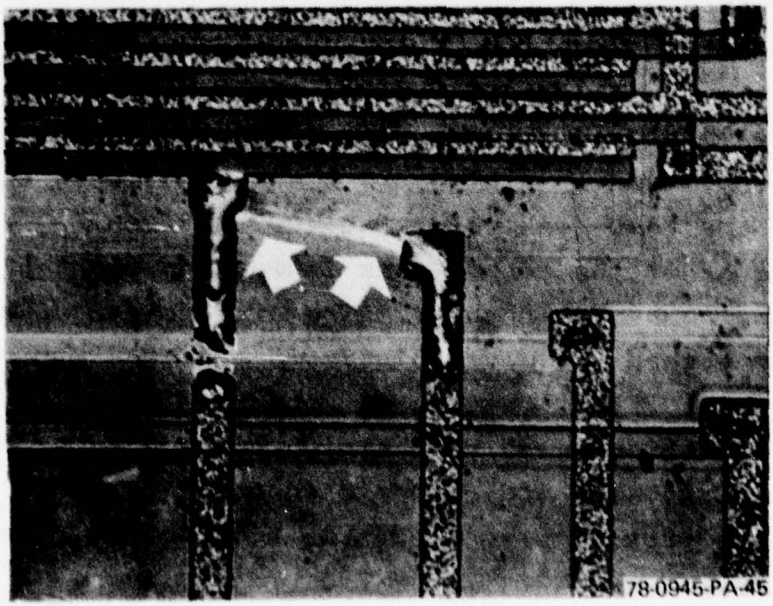


Figure 41. High Voltage Breakdown Path on Device 7007-6-14

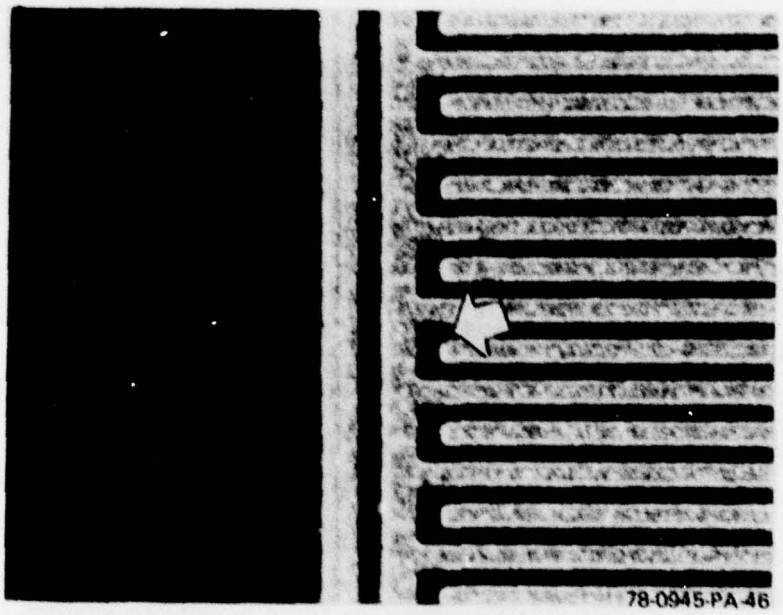


Figure 42. Dielectric Puncture Point on Device 7007-6-12

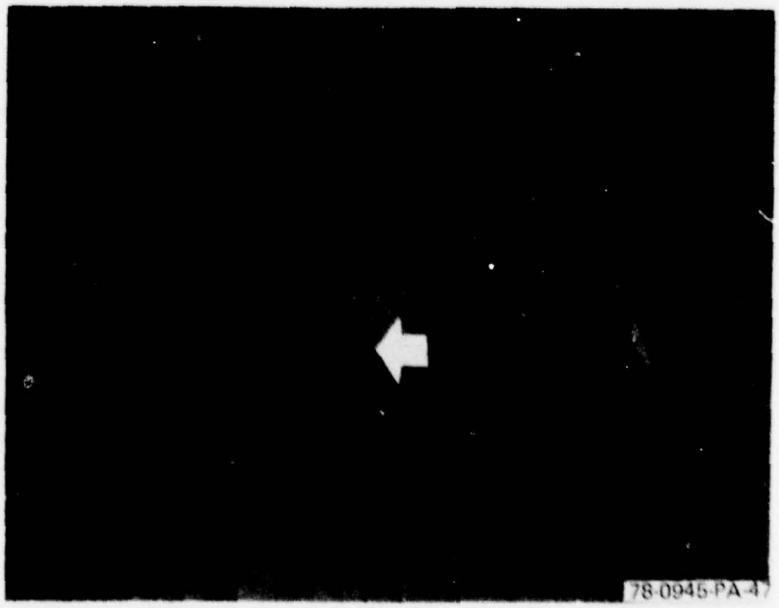


Figure 43. Silicon Defect Breakdown at Isolation Junction on Device 7007-6-3

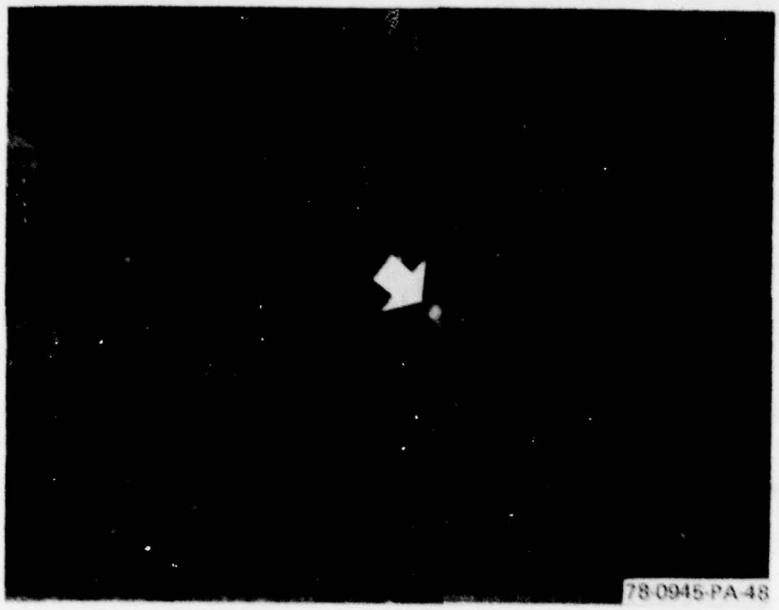


Figure 44. Dielectric Puncture Points on Device 7007-8-6

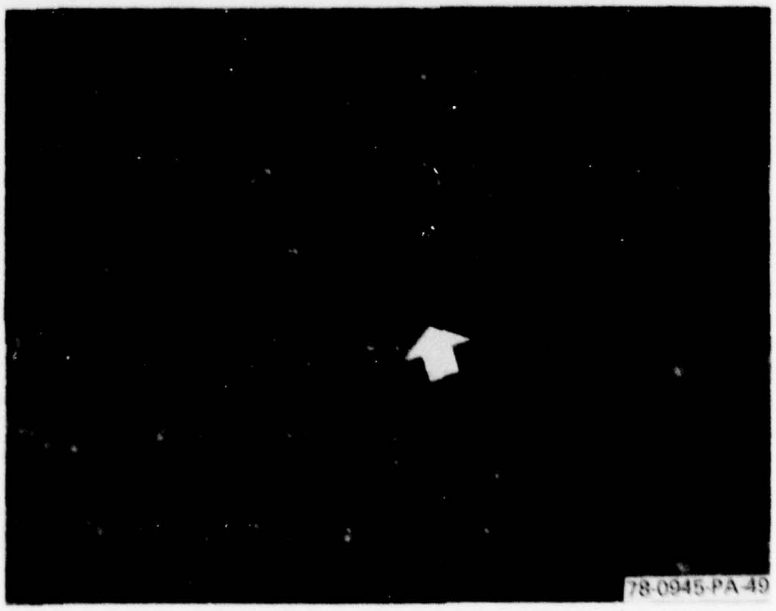


Figure 45. Dielectric Puncture Points on Device 7007-8-2

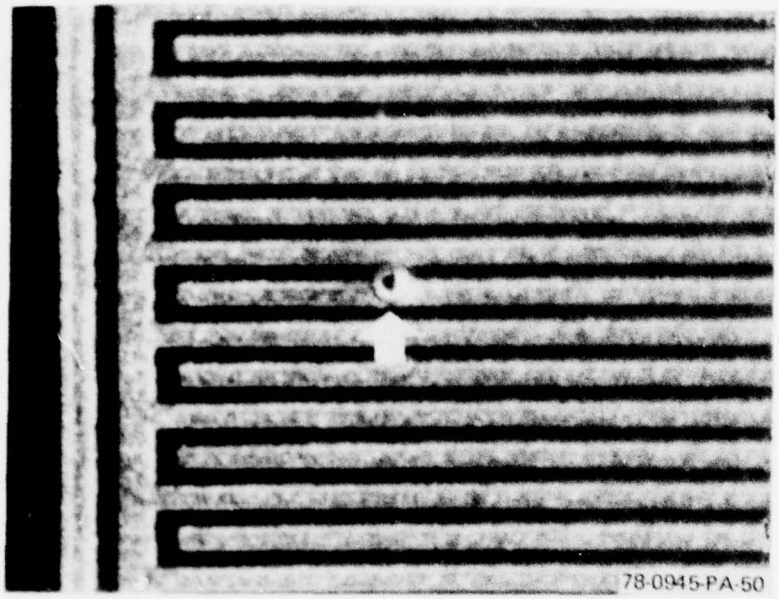


Figure 46. Dielectric Puncture Point to Gate Electrode on Device 7007-6-30

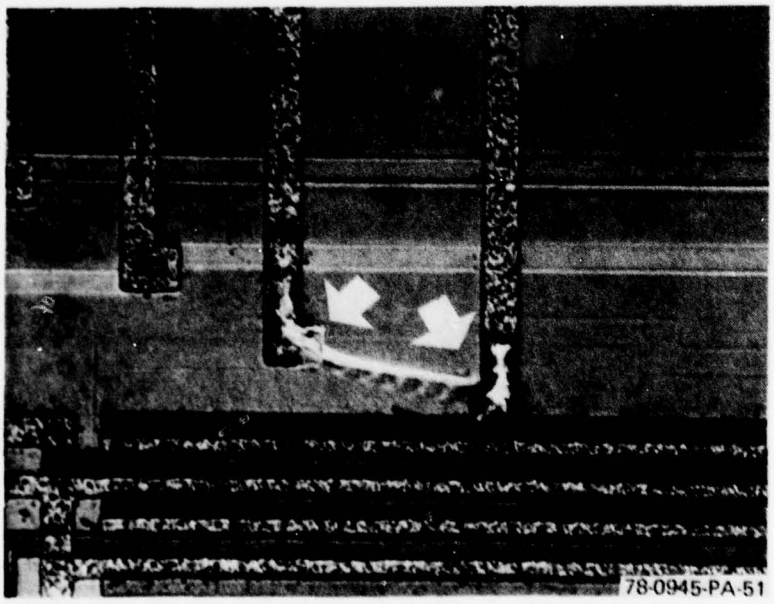


Figure 47. High Voltage Breakdown Path on Device 7007-6-28

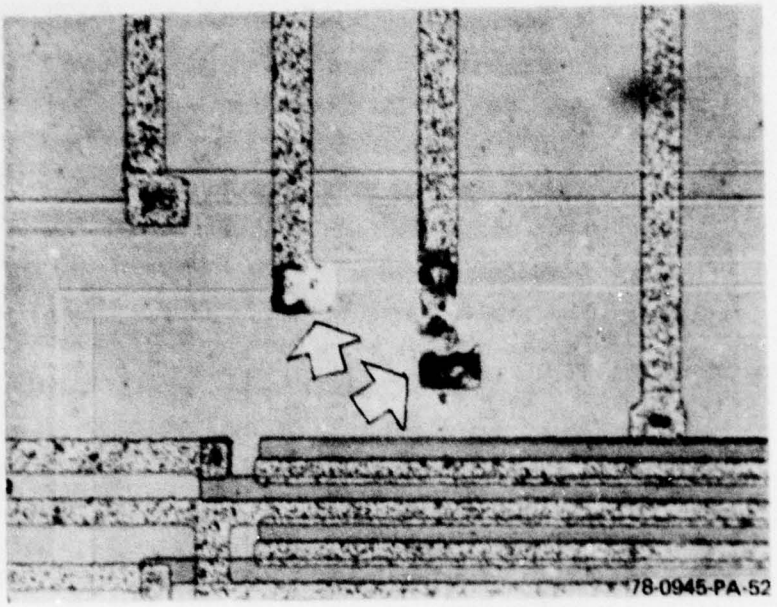


Figure 48. High Voltage Breakdown Path on Device 7007-12-32



Figure 49. High Voltage Breakdown Path on Device 7007-6-5

3.4 DISCUSSION OF EXPERIMENTAL RESULTS

A summary of the test data is presented in tables 18 through 23 and figures 51 through 54. Each data value in the tables represents the mean and standard deviation of 10 measurements (10 devices) per category for the SCCD's and 14 measurements (7 devices) per category for the BCCD's. The g_m of the output transistor for the SCCD's was measured initially and at the end of stress testing, and was essentially unchanged. The output amplifier of the BCCD was not available for separate measurement of its g_m. Referring to table 18, no significant change in full well capacity was observed for either the SCCD's or the BCCD's under stress testing except the BCCD 200°C dc test group showed an increase in capacity of 11 percent. Tables 19 and 20 give the test data results for dark current and transfer efficiency for the various stress categories. The data shows a uniform trend towards increased dark current with temperature stress for all SCCD test categories. A constant ratio difference of the initial and final measurements between the dynamic and dc stress SCCD categories can also be determined from the data with the dynamic category always the larger. A possible explanation is that for the dc



Figure 50. Dielectric Puncture Point on Device 7007-6-5

TABLE 18

FULL WELL VOLTAGE VARIATION OVER 1,000 HOURS OF STRESS
(MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Full Well Voltage			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.66	0.14	0.58	0.08
SCCD P-Channel	dynamic	125°C	0.59	0.09	0.61	0.11
SCCD P-Channel	dc	200°C	0.57	0.11	0.57	0.11
SCCD P-Channel	dynamic	200°C	0.58	0.11	0.59	0.08
BCCD N-Channel	dc	125°C	1.83	0.13	1.84	0.13
BCCD N-Channel	dynamic	125°C	1.78	0.14	1.78	0.14
BCCD N-Channel	dc	200°C	1.75	0.14	1.94	0.13

78-0789-TA-1

TABLE 19

DARK CURRENT VARIATION OVER 1,000 HOURS OF STRESS TESTING
(MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Dark Current nA/Square Cm			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	118/31*	234/11*	80	40
SCCD P-Channel	dynamic	125°C	30	9	1825/194*	2893/138**
SCCD P-Channel	dc	200°C	55	45	122	94
SCCD P-Channel	dynamic	200°C	44	35	204	121
BCCD N-Channel	dc	125°C	37	25	44	32
BCCD N-Channel	dynamic	125°C	73	64	67	61
BCCD N-Channel	dc	200°C	34	16	47	20

*Data with all sample values/data with two of ten samples deleted.
**Data with all sample values/data with three of ten samples deleted.

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TABLE 20

TRANSFER EFFICIENCY VARIATION OVER 1,000 HOURS OF STRESS TIME (MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Transfer Efficiency per Transfer							
			Initial				Final			
			0% F.Z.		10% F.Z.		0% F.Z.		10% F.Z.	
			Mean	S.D.	Mean	S.D.	Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.9986	0.0005	0.9994	0.0003	0.9983	0.0005	0.9994	0.0003
SCCD P-Channel	dynamic	125°C	0.9990	0.0005	0.9995	0.0006	0.9979	0.0010	0.9993*	0.0003*
SCCD P-Channel	dc	200°C	0.9984	0.0007	0.9994	0.0005	0.9966	0.0018	0.9984	0.0011
SCCD P-Channel	dynamic	200°C	0.9990	0.0003	0.9997	0.0001	0.9970	0.0014	0.9982	0.0013
BCCD N-Channel	dc	125°C	0.9990	0.0002	0.9999	0.0000	0.9987	0.0002	0.9999	0.0001
BCCD N-Channel	dynamic	125°C	0.9991	0.0002	0.9999	0.0000	0.9989	0.0001	0.9999	0.0000
BCCD N-Channel	dc	200°C	0.9991	0.0002	0.9999	0.0000	0.9953	0.0006	0.9968	0.0004

*Data with three of ten samples deleted

78-0789-TA-3

TABLE 21

INSERTION LOSS VARIATION OVER 1,000 HOURS OF STRESS TIME (MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Insertion Loss dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	-25.9	1.3	-29.0	1.4
SCCD P-Channel	dynamic	125°C	-26.1	2.1	-25.7	1.4
SCCD P-Channel	dc	200°C	-26.1	1.7	-26.4	1.8
SCCD P-Channel	dynamic	200°C	-25.6	1.1	-26.8	3.0
BCCD N-Channel	dc	125°C	-13.7	0.5	-11.6	1.0
BCCD N-Channel	dynamic	125°C	-13.6	0.5	-12.1	1.2
BCCD N-Channel	dc	200°C	-13.7	0.5	-31.2	5.0

78-0789-TA-4

TABLE 22

DYNAMIC RANGE VARIATION OVER 1,000 HOURS OF STRESS TIME
(MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Dynamic Range dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	43.0	1.3	40.2	1.7
SCCD P-Channel	dynamic	125°C	44.0	1.9	45.0	3.7
SCCD P-Channel	dc	200°C	43.7	3.9	39.6	5.1
SCCD P-Channel	dynamic	200°C	44.2	1.3	44.6	0.9
BCCD N-Channel	dc	125°C	47.3	1.3	53.1	2.1
BCCD N-Channel	dynamic	125°C	47.6	1.2	51.5	0.9
BCCD N-Channel	dc	200°C	45.0	3.1	27.0	5.0

78-0789-TA-5

TABLE 23

INPUT GATE "THRESHOLD" VOLTAGES FOR THE SCCD TEST CATEGORIES
(MEASUREMENTS MADE AT ROOM TEMPERATURE)

Device Type	Voltage Stress	Stress Temperature	Gate Threshold (volts)			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	14.9	0.2	14.9	0.1
SCCD P-Channel	dynamic	125°C	15.6	0.6	14.7	0.3
SCCD P-Channel	dc	200°C	15.6	0.2	15.0	0.2
SCCD P-Channel	dynamic	200°C	15.6	0.2	14.8	0.1

78-0789-TA-6

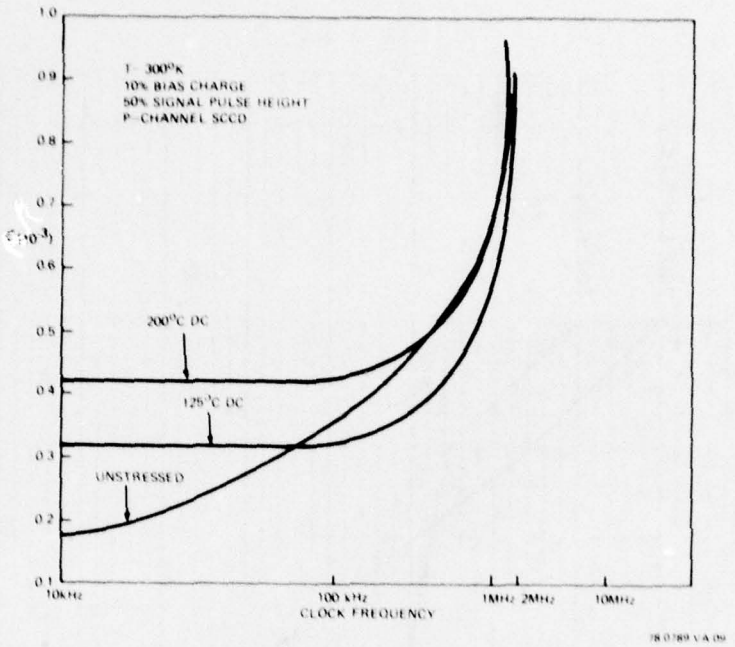


Figure 51. Surface Channel CCD Transfer Inefficiency as a Function of Clock Rate

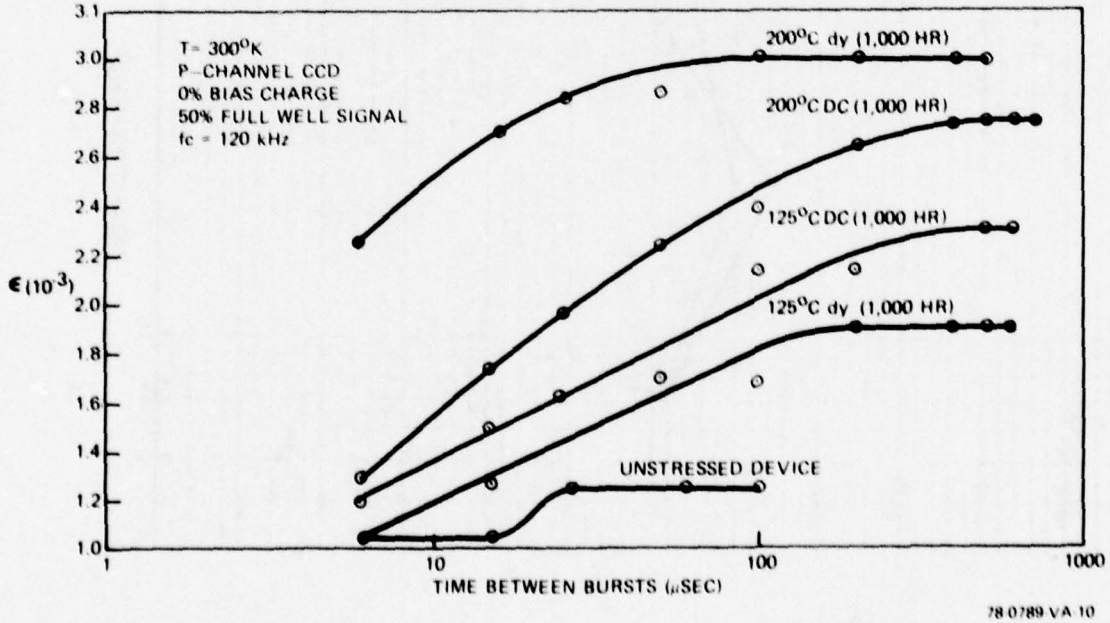


Figure 52. Double Pulse Measurements for Stressed and Unstressed SCCD's

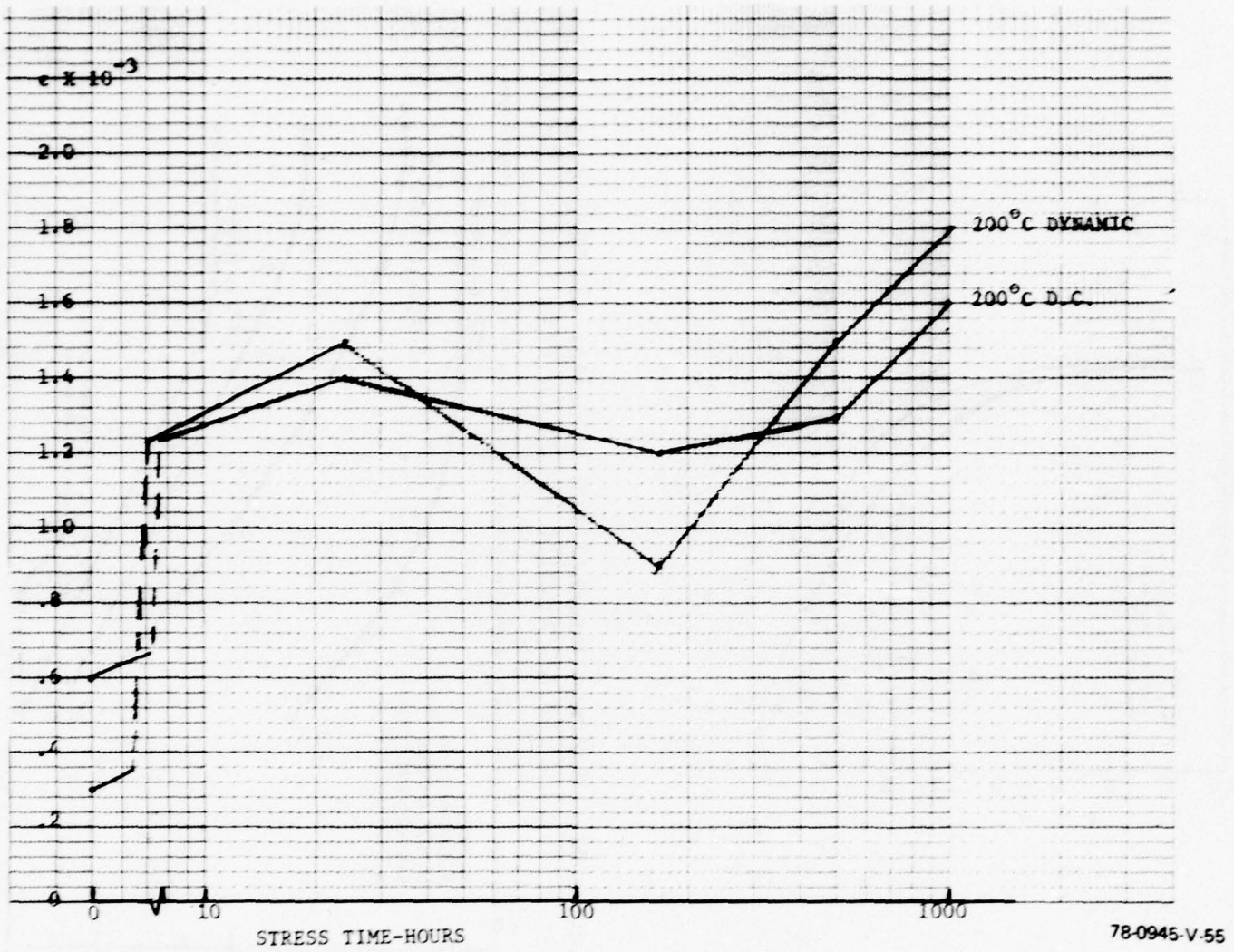


Figure 53. Degradation of 7004 Devices with Time at 200°C

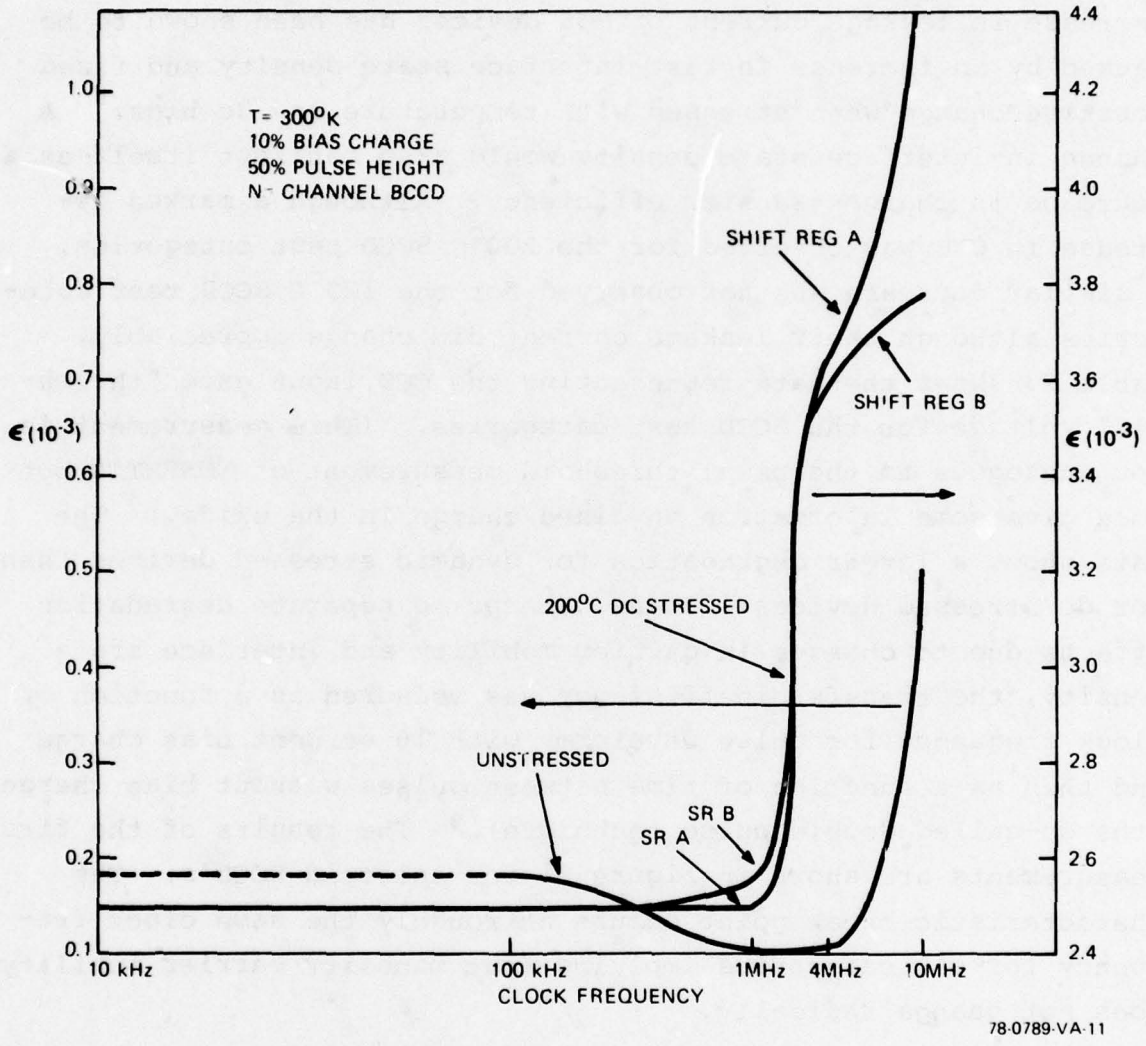


Figure 54. Transfer Inefficiency versus Clock Frequency for BCCD's

stressed devices the entire voltage drop occurred across the gate oxide because the surface was inverted. On the other hand, the devices stressed with dynamic voltages had a depleted region at the silicon surface over which some voltage drop occurred. An increase in leakage current of MOS devices has been shown to be caused by an increase in fast interface state density and fixed positive charge when stressed with temperature and dc bias.[8] A change in interface state density would also manifest itself as a decrease in charge transfer efficiency. Although a marked decrease in CTE was observed for the 200°C SCCD test categories, a similar decrease was not observed for the 125°C SCCD test categories although their leakage current did change appreciably. Table 23 shows the data representing the CCD input gate "threshold" voltage for the SCCD test categories. (This measurement is not analogous to the usual threshold measurement of MOSFET's but does give some information on fixed charge in the oxide.) The data shows a larger degradation for dynamic stressed devices than for dc stressed devices. In an attempt to separate degradation effects due to changes in carrier mobility and interface state density, the transfer inefficiency was measured as a function of clock frequency for pulse waveforms with 10 percent bias charge and then as a function of time between pulses without bias charge (the so-called double pulse technique).[9] The results of the first measurements are shown in figure 51 for selected SCCD's. The characteristic break point occurs at roughly the same clock frequency for all categories implying that minority carrier mobility does not change radically.

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[8] A. Geotzberger, A.D. Lopez, & A. J. Strain, "On the Formation of Surface States During Stress Aging of Thermal Si-SiO_2 Interfaces," J. of the Electrochemical Society, Vol. 120, No. 1 p. 90, Jan. 1973.

[9] J. E. Carnes & W. F. Kosonocky, "Fast Interface State Losses in Charge-Coupled Devices," Appl. Phys Lett., Vol. 20, pp 261-263, Apr. 1972.

The results of the double pulse experiment for SCCD's are shown in figure 52. Comparison of these graphs for the 200°C and 125°C categories show a change in slope on the order of ~2 which represents a factor of two increase in interface state density. Comparison of the initial and final transfer efficiency for the 125°C and 200°C test categories show that this factor of two increase in interface state density reasonably explains the difference in values. Although the factor of two also causes a proportional increase in leakage current which is reasonably consistent with the 125°C and 200°C dc SCCD stress results, the factor of approximately four change for the leakage current in the 125°C and 200°C dynamic SCCD stress categories cannot be readily explained by the data shown in figure 52. The data in tables 20 and 21 show that neither the dynamic range nor the insertion loss changed dramatically for any of the SCCD test categories. Although the CTE did change substantially for 200°C stressed SCCD's, the devices are only 44 stages which is too short to impact insertion loss and dynamic range. Degradation of transfer efficiency with stress time at 200°C is shown in figure 53. The curves show two distinct trends. First, a very rapid degradation within 24 hours of stress is apparent. A period of stability appears to exist for several hundred hours followed by a trend toward rapid degradation after ~800 hours.

The experimental results for the BCCD do not lend themselves to easy physical interpretation. Although the device is a buried channel CCD, the data given in table 20 shows a marked improvement in transfer efficiency with the addition of a bias charge. The devices use an n+ floating diffusion for making several corner turns in the shift register. This corner turn technique has been replaced by clocked electrodes by the manufacturer in later generations of the device type with the reported result that excellent transfer efficiency is achieved without bias charge.[10] The reason for poor CTE appears then to be caused by barrier

[10]Private Communication, Fairchild Semiconductor Corp., 1978.

modulation associated with the floating n+ corner-turns. This effect also causes poor CTE in bucket brigade devices. Unlike the SCCD, there is no consistent increase in leakage current for the BCCD stressed devices. However, a substantial degradation in transfer efficiency occurred in the 200^{0}C group. This loss in transfer efficiency could not be compensated by an increase in bias charge or by increasing or decreasing the clock voltages. Transfer efficiency measurements made as a function of frequency are shown in figure 54 for an unstressed device and the mean of all 200^{o}C stressed devices. Differences are clearly apparent between the two 455-bit shift registers on the same device for the 200-degree dc results as well as a general shift of the break point toward lower frequencies. The double pulse results for the 200^{o}C dc stressed devices and an unstressed device and the 125^{o}C dc devices are presented in figures 55 and 56. The shape of the curves for the unstressed device is consistent with measurements made by others of BCCD's[11,12,13] implying a single level of mid-gap electron trap states. Figure 55 shows the slope of the analogous line in the 125^{o}C test groups is ~0.4. This ratio is ~3.75. If the differences in slope are attributed entirely to an increase in bulk trap density, the difference between the transfer efficiency of the 125^{o}C dc test group and 200^{o}C dc test group are very reasonably rationalized. However, a similar ratio difference in dark current density between the two groups would also be expected which did not occur. Traps which predominately contribute to dark current are in the middle of the band gap whereas traps which cause transfer inefficiency may be elsewhere in the band gap. The degradation in insertion loss and dynamic range for sinusoidal

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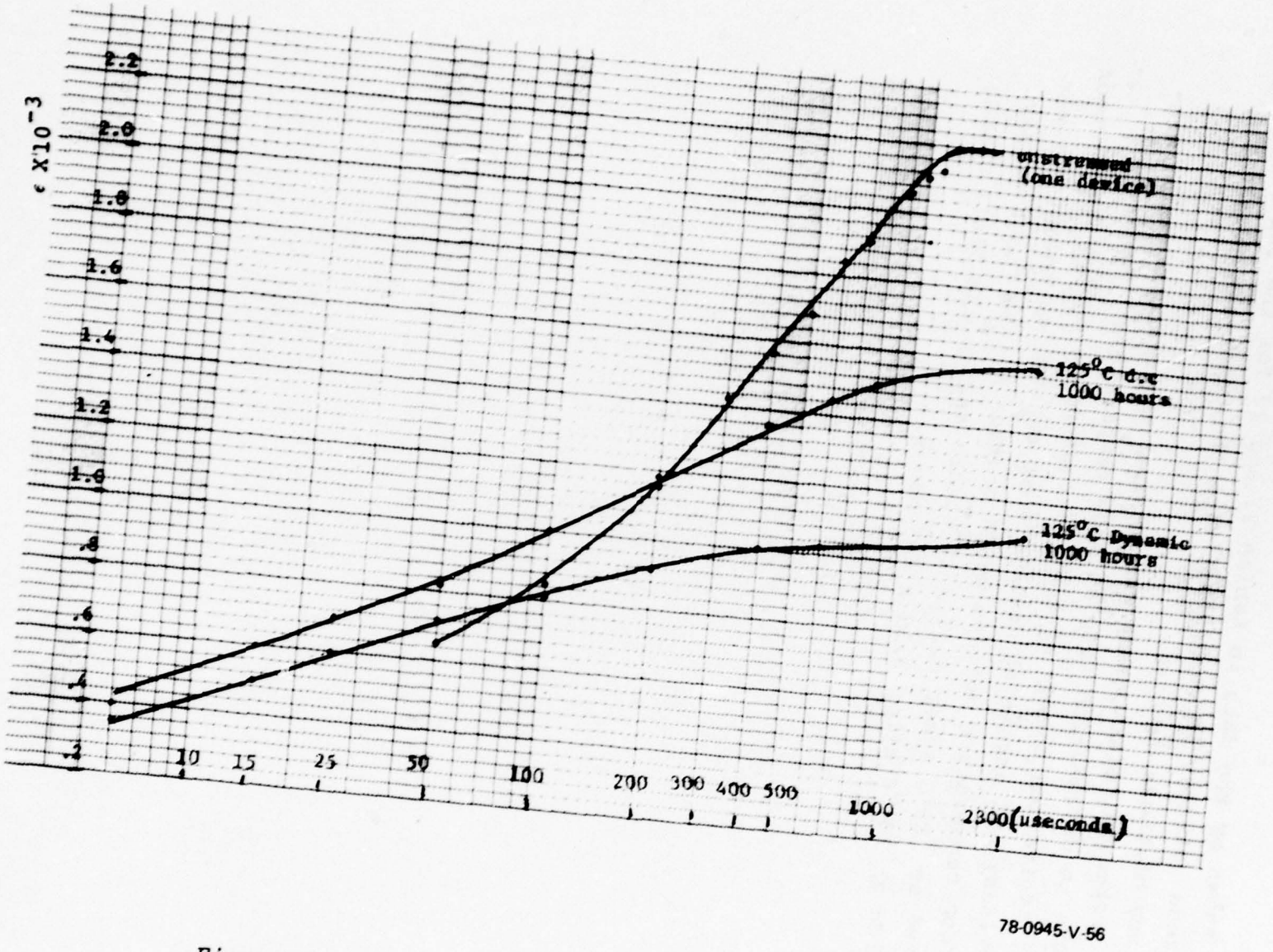
[11] N.S. Saks, J.M. Killiany, and W.D. Baker, "Effects of Neutron Radiation on the Characteristics of a Buried Channel CCD at 80 K and 295 K," Proceedings on Charge Coupled Device Technology and Applications, p. 110, Dec. 1976

[12] R.W. Brodersen & S.P. Emmons, "The Measurement of Noise in Buried Channel CCD's," Proc. Int. Conf. Appl. CCD's, p. 331, Oct. 1975.

[13] C. Sequin & M. Tompsett, op. cit.

signals shown by the data in tables 21 and 22 for the 200°C dc BCCD stress category is consistent with the decreased transfer efficiency of these devices.

An Arrhenius relationship can be used to relate stressed measurements to degradation rate at room temperature. Assuming a thermal activation energy of 1 eV (a reasonable choice for silicon MOS devices) and screening devices that succumb to infant mortality, room temperature devices would degrade to the final values measured at 125°C after 8.54×10^4 hours and to the final values measured at 200°C after 5.13×10^5 hours.



78-0945-V-56

Figure 55. CCD321 Double Pulse Data (Mean of Test Groups)

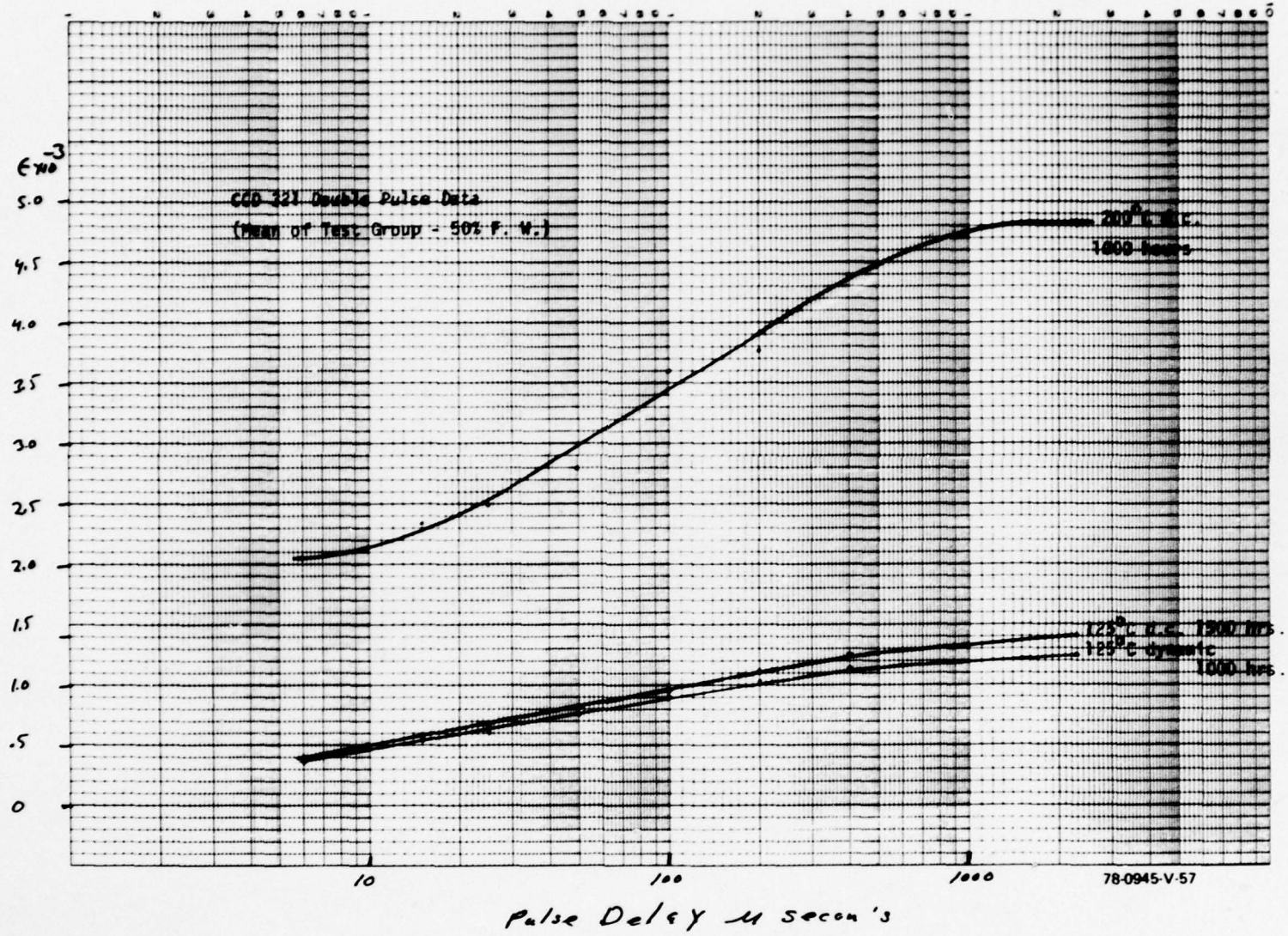


Figure 56. CCD321 Double Pulse Data (Mean of Test Group - 50% FW)

4. CONCLUSIONS

1. Basic trend towards increased dark current and decreased charge transfer efficiency in the SCCD devices (7004) can be attributed to an increase in interface state density.
2. Dynamic stressing of SCCD devices degrades parameters faster than dc stressing.
3. A decrease in charge transfer efficiency under 200°C stress for the BCCD (CCD321) can be attributed to an increase in bulk trap density. Why this increase does not cause an increase in dark current density is unexplained.
4. All the catastrophic failures observed in the 7004 SCCD devices were of the early failure type attributable to fabrication related faults (i.e, dielectric pinholes).
5. Test data on the unscreened 7004 devices indicated that a MIL-STD-883, Method 1015.1 Burn-In Test, Test Condition D at 125°C for 168 hours would have been effective in removing the early failures from the population of unscreened devices.

5. RECOMMENDATIONS

1. A 100 percent burn-in screen at 125°C with dynamic stress for 168 hours should be used to remove early failures from any CCD device population intended for reliable applications.
2. An operational temperature of 125°C should not be exceeded for any CCD device.
3. Additional study should be undertaken to define the nature of the physical process that degrades CCD devices at 200°C when operational levels of electrical stress are applied.

6. ACKNOWLEDGEMENT

The authors thank Merle Hoxie for making the many measurements associated with this program. The authors also acknowledge useful discussions held with Drs. M.H. White, Don Lampe, and Nate Bluzer of Westinghouse and Dr. Joseph Killiany of the Naval Research Laboratory concerning interpretation of experimental results.

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4. R. W. Brodersen, D. D. Bass & A. F. Tasch, Jr., IEEE Trans., ED-22, pp 40-46 (Feb. 1975)
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10. Private Communication, Fairchild Semiconductor Corp., 1978.
11. N. S. Saks, J. M. Killiany, & W. D. Baker, "Effects of Neutron Radiation on the Characteristics of a Buried Channel CCD at 80 K and 295 K," Proceedings on Charge Coupled Device Technology and Applications," p.110, Dec. 1976.
12. R. W. Brodersen & S. P. Emmons, "The Measurement of Noise in Buried Channel CCD's," Proc. Int. Conf. Appl. CCD's, p.331, Oct. 1975.
13. C. Sequin & M. Tompsett, op.cit.

APPENDIX A
ELECTRICAL TEST CIRCUITRY

As indicated in the body of the report all the electrical parametric measurements were made on the CCD's utilizing exerciser circuits which provided all the required dc and pulse voltage to operate the device under test. Two basic exerciser circuits were used, one for the CCD 321 device and the other for 7004 and 7007 devices. Also to ensure fail safe excitation for life stress pruposes a power system was provided which floated a 28-volt storage battery on the dc power supply bus to the exercisers and stress circuits. If utility power interruption occurred, the batteries took over and maintained normal stress circuit operation without any interruption or transients.

The circuit diagram of the "CCD 321 module" (CCD 321 exerciser) is shown in figure A-1. This unit was purchased from Fairchild. The "CCD 321 module" is a printed circuit board containing input and output signal processing circuitry, and the required clocking signal sources and bias voltages to exercise the CCD 321 device. A single 20-25 volt power source was needed for its operation.

For parametric measurements on the CCD 321 device, it was necessary to disable the output amplifier sample and hold circuitry. This was done on an adapter socket by connecting pin 7 (ϕRA) and pin 9 (ϕRB) to V_{DD}. Also it was necessary to measure the output at pins 1 and 15 of the device rather than at the outputs of the on the board amplifiers because of the modification these amplifiers introduced to the pulse waveforms.

The dark current integration circuit used in conjunction with the "CCD 321 module" is shown in figure A-2. This circuit provides the integration control for dark current measurements as described in section 2.3.2 of this report.

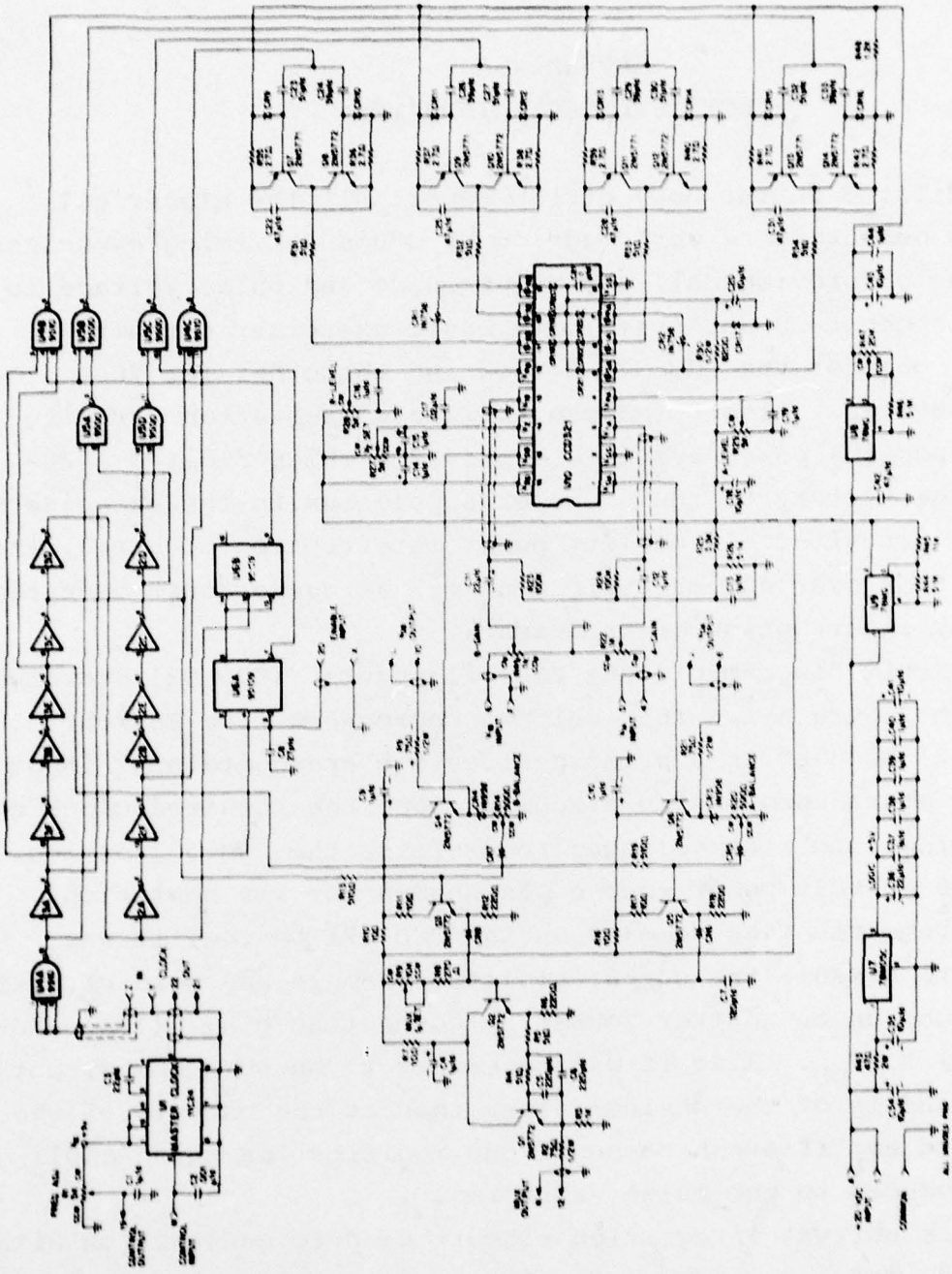
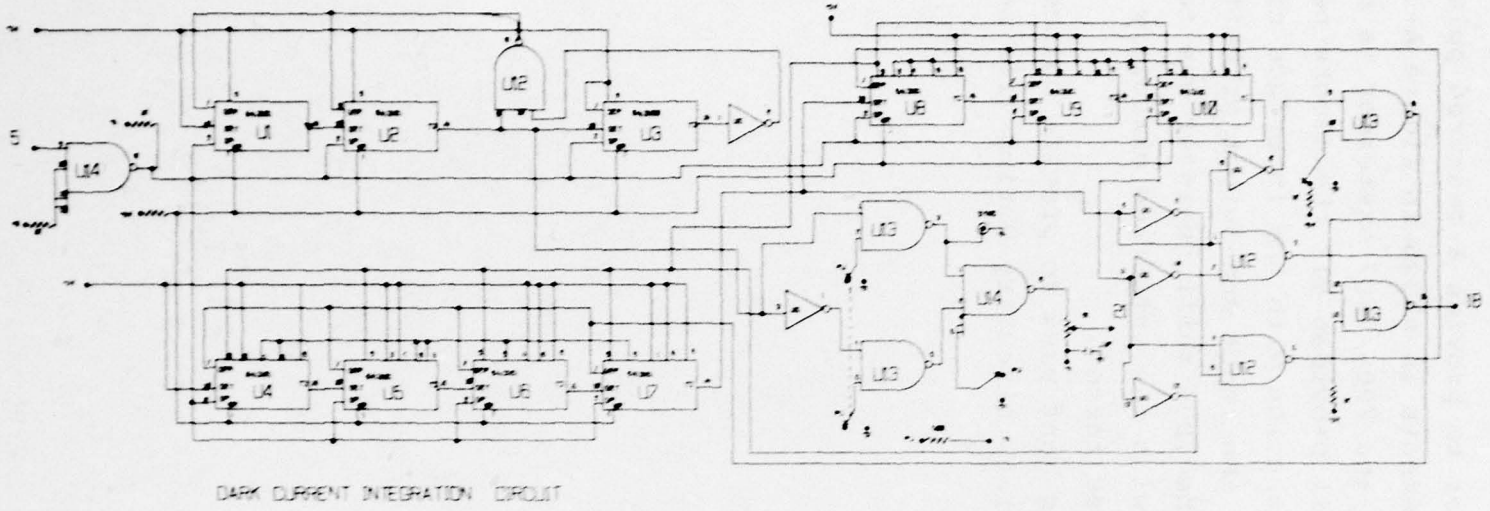


Figure A-1. CCD 321 Module



DARK CURRENT INTEGRATION CIRCUIT

U1, 2, 4, 5, 6, 7, 8, 9, 10	74LS161
U3	74LS160
U11	74LS04
U12, 13	74LS00
U14	74LS20

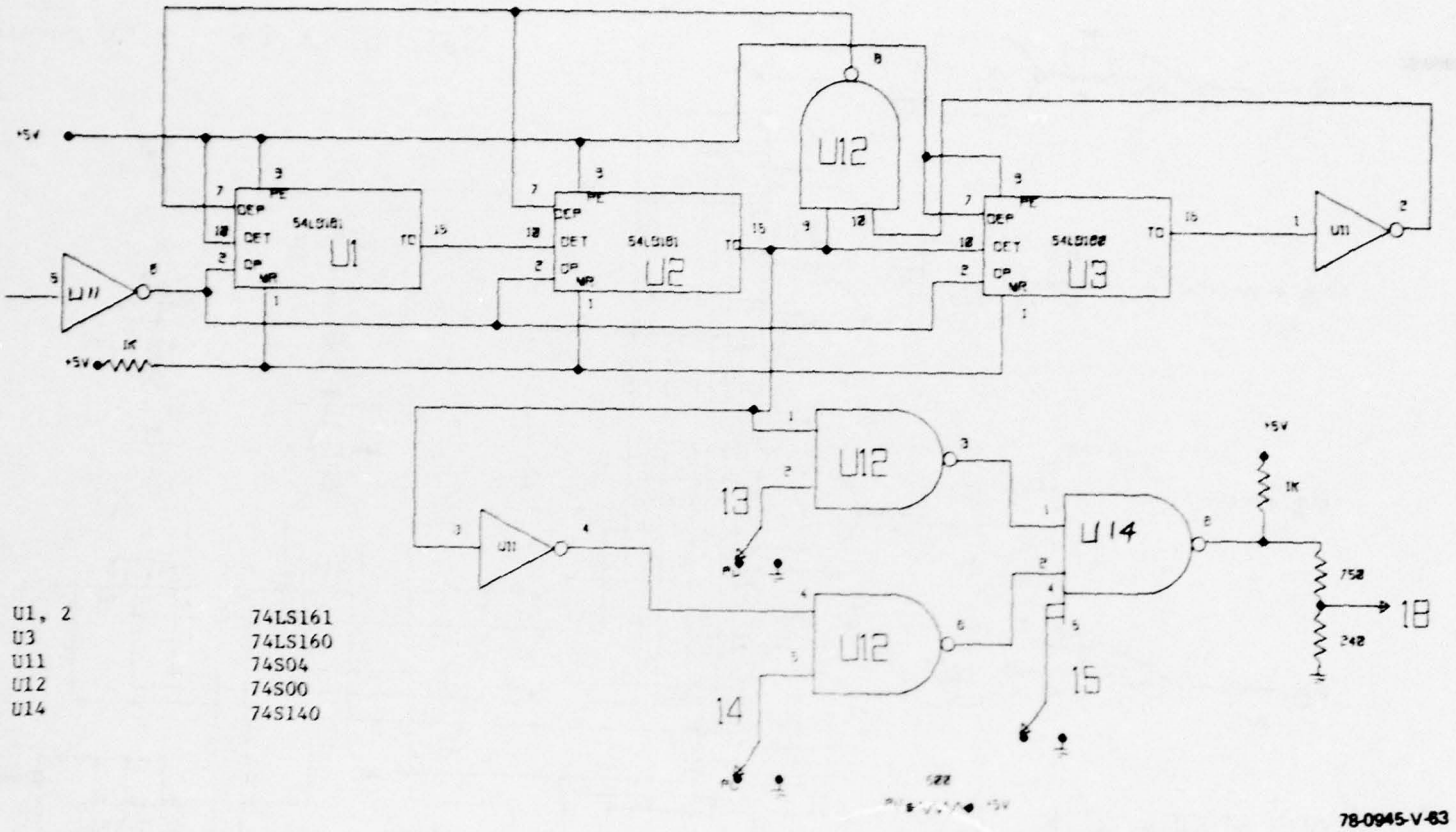
78-0845-V-42

Figure A-2. Dark Current Integration Circuit

A clock generator circuit used with the "CCD 321 module" and with the 7004/7007 exerciser to provide a measured pulse for transfer efficiency measurements is shown in figure A-3.

The circuit diagram of the 7004/7007 exerciser is shown in figure A-4. This circuit provides all the clocks needed to operate a 4ϕ CCD. In conjunction with the interface circuit in figure A-5, which provides the input and output circuitry and proper interconnections, the 7004 shift register was tested. Similarly, in conjunction with the interface circuitry in figure A-6, the 7007 CCD was tested.

The power supply arrangement used to provide uninterruptable power to the electrical stress circuitry during life testing is shown in figure A-7.



U1, 2	74LS161
U3	74LS160
U11	74S04
U12	74S00
U14	74S140

Figure A-3. Clock Generator for Transfer Efficiency Measurements

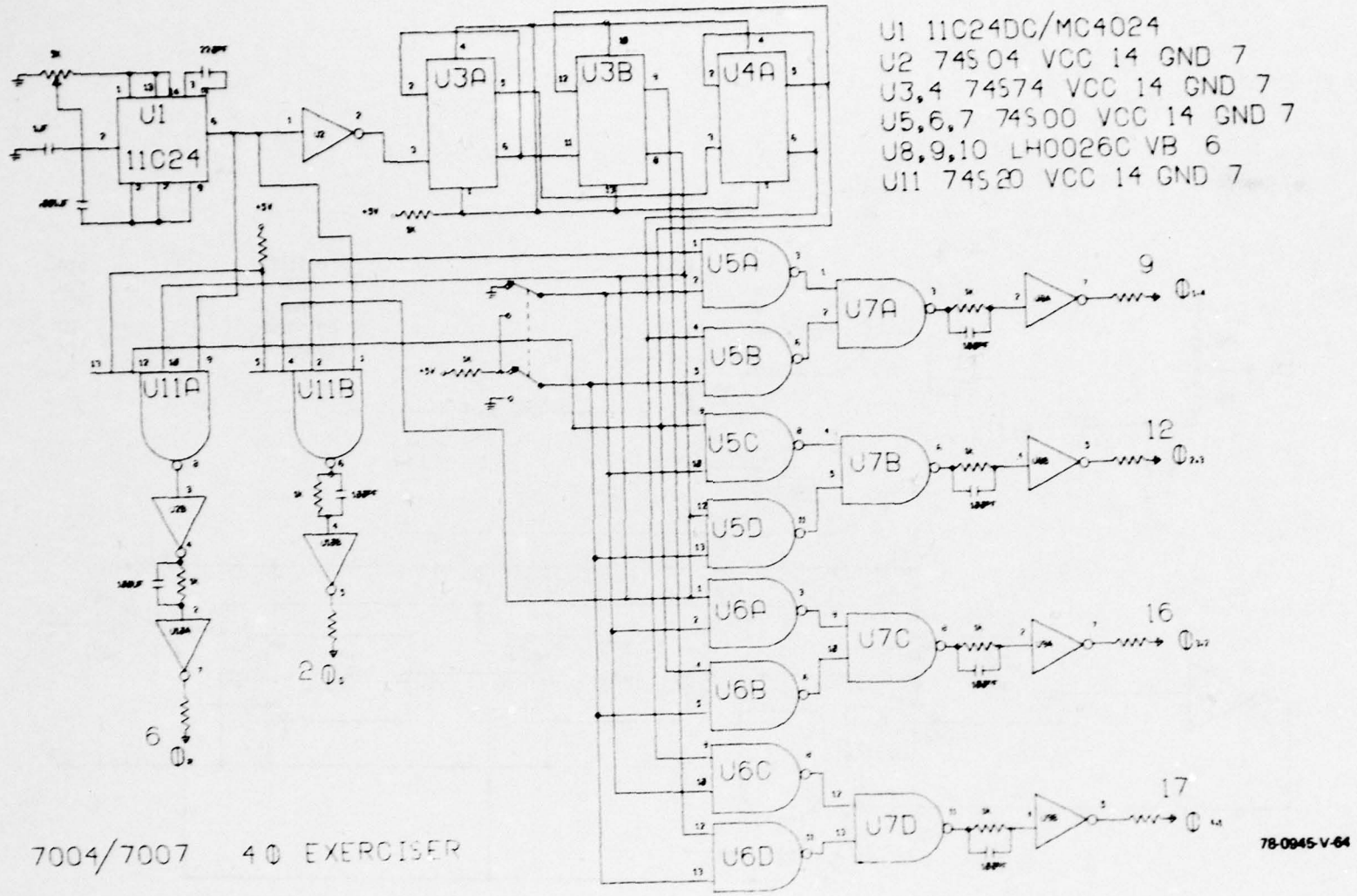


Figure A-4. 7004/7007 4φ Exerciser

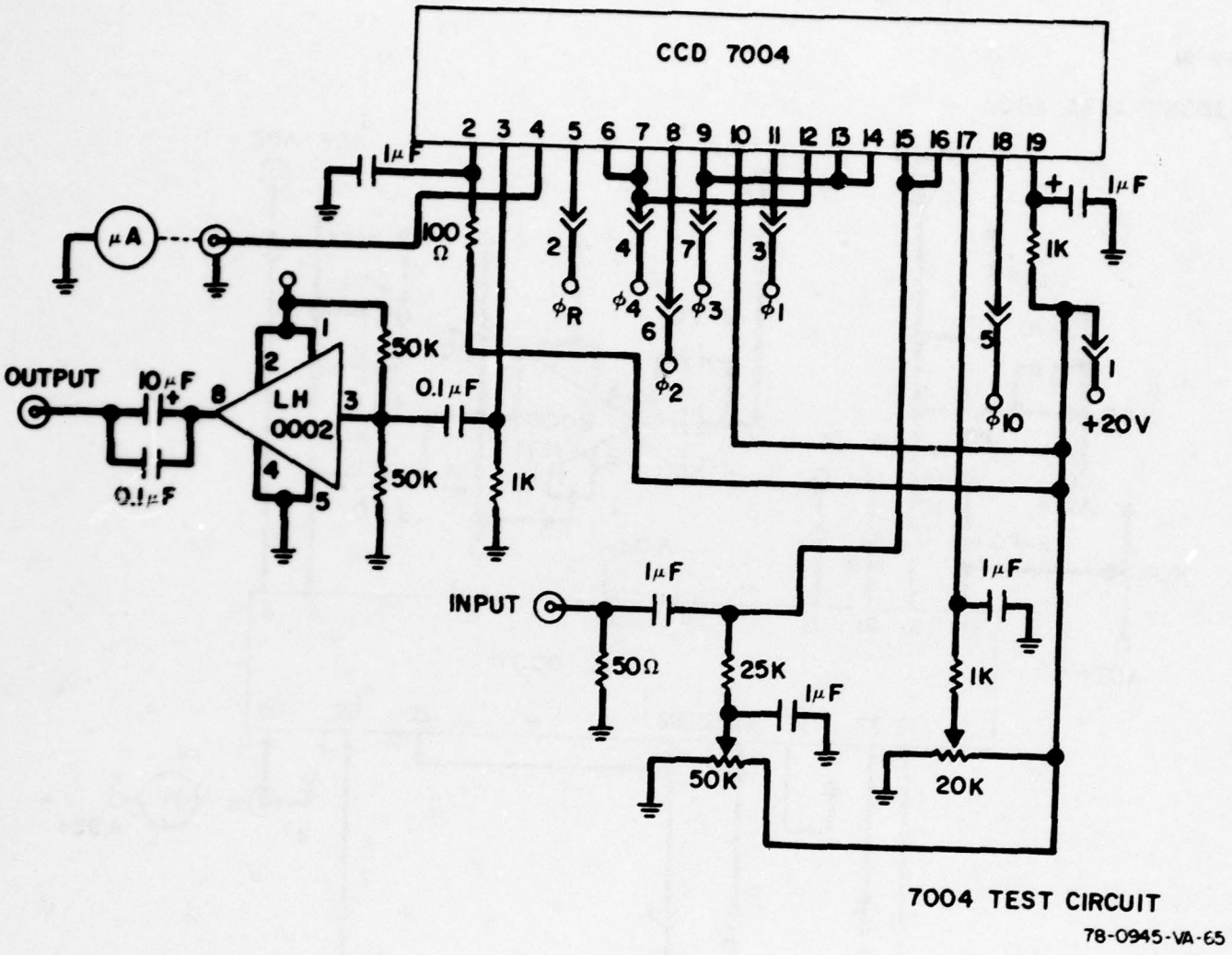
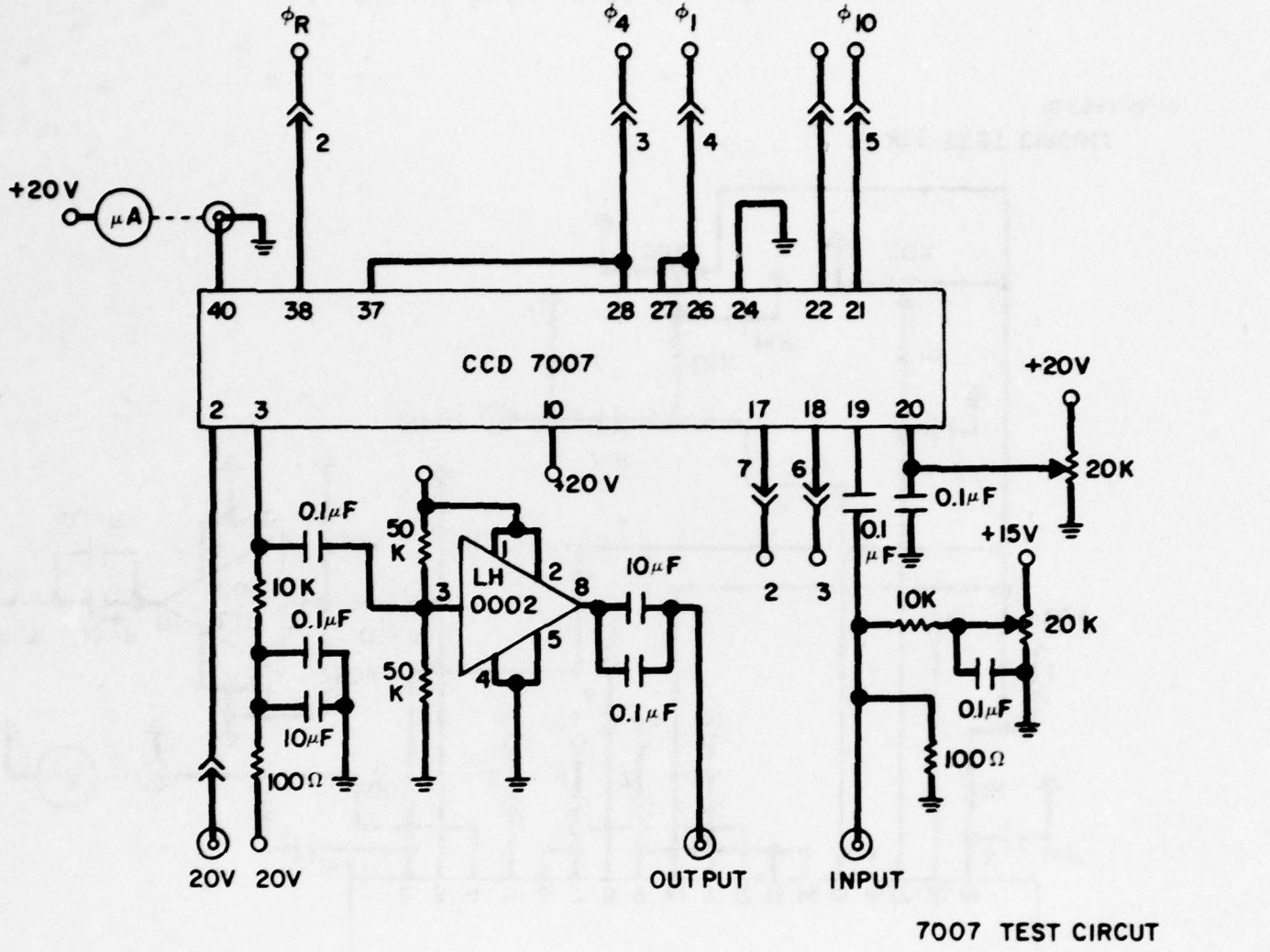


Figure A-5. 7004 Interface Board



7007 TEST CIRCUT

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Figure A-6. 7007 Interface Board

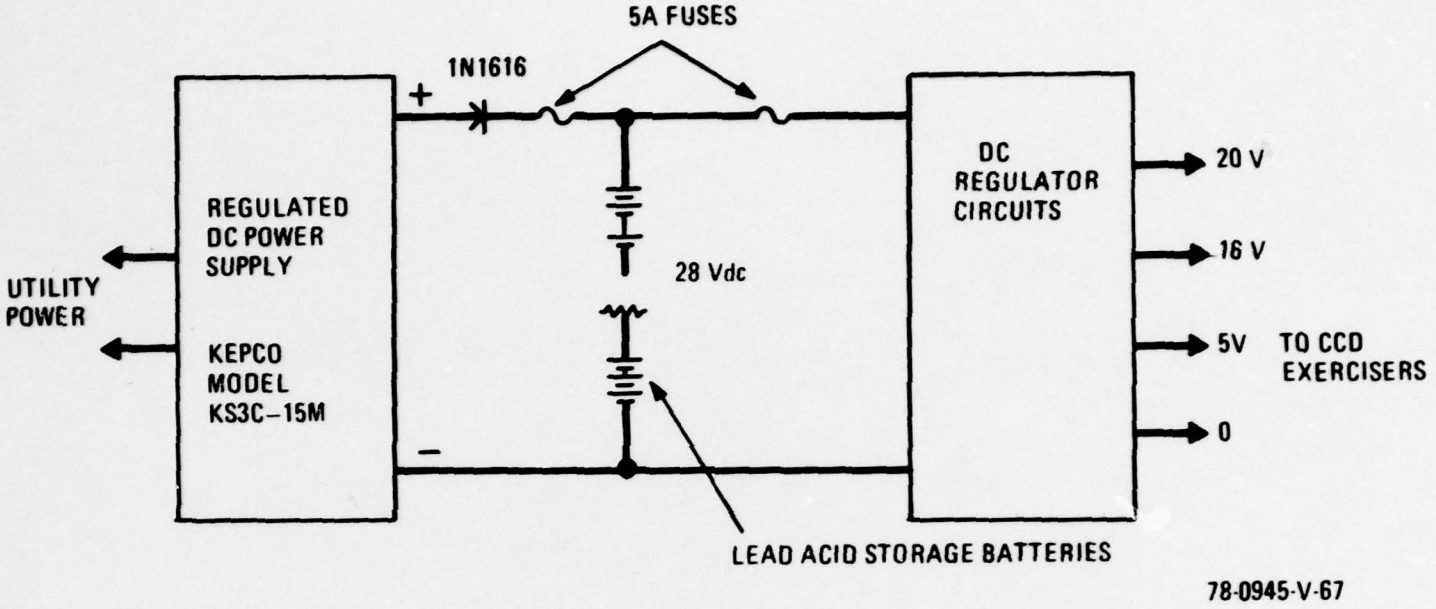


Figure A-7. Uninterruptable Power Source

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