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DYNAMIC PROPERTIES OF INTERFACE STATES IN MOS-STRUCTURES

Final Technical Report

LEVEL II

by

A. Goetzberger and E. Klausmann

January 1979

EUROPEAN RESEARCH OFFICE

United States Army

London England

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GRANT NUMBER DA-ERO-78-G-031

Fraunhofer-Institut für Angewandte Festkörperphysik
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Errata

Page 9

(a) The expression $\frac{t_1}{2.52}$ in eq (7) has to be replaced by $2.52 \cdot t_1$.

(b) The expression $\frac{d\ \sigma(E_o)}{dE}$ in eq (10) has to be replaced by

$$\frac{d \ln \sigma(E_o)}{dE} .$$

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This is the second annual technical report of a three years research program.

Within this project details of the dynamic properties of impurities implanted into the interface of MOS structures are investigated. Interface state density, trapping time constants and capture cross sections are measured.

The CC-DLTS-method (Constant Capacitance Deep Level Transient Spectroscopy)

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is a valuable means to tackle the topical problems, especially because it requires less measuring time than competing methods. The presently used evaluation method is over-simplified and yields occasionally misleading results. This was revealed by an experimental check with the conductance method. An improved evaluation procedure is suggested.

The conductance method was applied to the measurement of Cs-implanted and non-implanted MOS structures of n- and p-type Si. The two n-type samples behave similarly: the interface state density increases and the capture cross section decreases towards the conduction band edge. These properties appear to a greater extent with the Cs-implanted sample.

With the p-type samples the limits of the conductance methods are encountered. These limits are discussed. The few data which could be obtained from the implanted sample do not yet permit an unequivocal and final comment.

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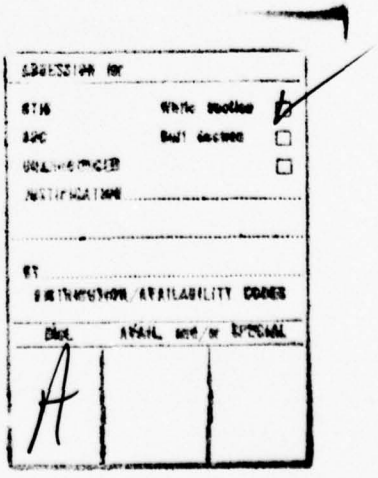

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I. The CC-DLTS-Method and the Conductance Method

Introduction

The conduction method is generally considered as the standard procedure for analysing the interface state properties of MOS structures. This method has been used to obtain the most reliable results about the energy distribution of interface state densities and capture cross sections in wide energy ranges. The biggest drawback is seen in the great time consumption and the necessity to operate the measuring equipment with permanent concentration.

Recently a strong competitor to the conduction method arose in the CC-DLTS-method (Constant Capacitance Deep Level Spectroscopy). The most striking advantage is the short measuring run time (about ten times faster than the conduction method) and the semi-automatic operation which only needs occasional supervision.

It seems therefore necessary to us to compare the two methods and their results obtained with possibly the same sample. We anticipate thereby to assess the reliability of the two methods. If differences are found they may be caused by

- shortcomings of the technical set-ups
- a too strongly simplified or incorrect mathematical evaluation of the measuring results and finally
- an inadequate physical model used to describe the interface states.

In the following it will be shown that at the time being the most serious imperfection originates in the mathematical evaluation procedure of the CC-DLTS-method.

The conduction method is already comprehensively covered in the literature /1, 2/. As nothing else has to be added in this report, another description is unnecessary. Only new results will be reported.

The first two articles about the CC-DLTS-method are pending publication /3, 4/ and are not yet available. Because of this, and as they were written in connection to the present contract they will be reproduced in the appendix.

In addition we will give further detailed information about both the method and the obtained results. In order to make the present report more understandable some repetitions of the papers cited above cannot be avoided.

The CC-DLTS-Method

With the CC-DLTS-method

- the density of interface states
- the capture cross sections and
- the energy level of these states

in MOS capacitors can be analysed. The method makes use of the time and temperature dependence of the electron (or the hole) emission from the interface states into the majority carrier band. The method is explained in Fig. 1a - d. First the states become occupied by electrons during a voltage pulse (20 µsec) into the accumulation regime. Then with the bias again in depletion the excess charges are thermally emitted (Fig. 1a). With the CC-DLTS-method the bias is controlled by a feedback circuit in such a way as to keep the hf-MOS-capacitance constant (Fig. 1b/c). Consequently the band bending also stays virtually constant during the emission and the evaluation is considerably facilitated.

The bias $V(t)$ is then measured at two different times t_1 and t_1^* ($= 2\,t_1$) and the difference $\delta V(t_1) = V(t_1) - V(t_1^*)$ (= correlation signal) is formed. By varying the temperature the emission rate is changed and the correlation signal becomes a maximum at an optimum temperature. The maximum occurs for each state of different energy and of different capture cross section at a different temperature (Fig. 1d). The correlation signal $V(t_1, T)$ is recorded in dependence of the temperature T with the gate times $t_1/2t_1$ as parameter.

With respect to the instrumentation the papers in the appendix may be consulted.

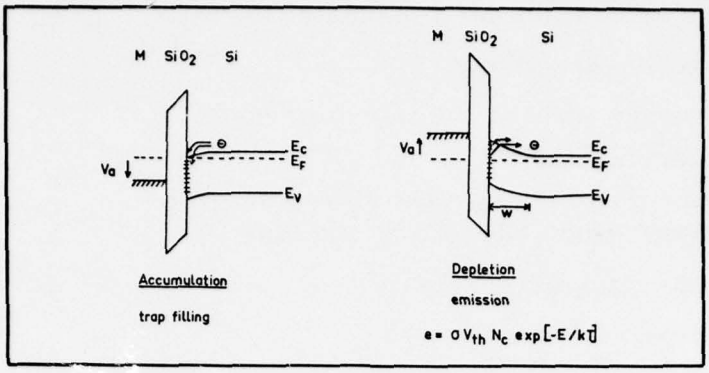
Quantitative Theory and Evaluation

In the two papers of the appendix it has been shown that the correlation signal is related to the pertinent physical quantities by

$$(1) \qquad \delta V(t_1, T) = \frac{A}{C_{ox}} \int_{Es}^{o} N_{ss}(E) \cdot \left[\exp\left(-\frac{t_1}{\tau(E)}\right) - \exp\left(-\frac{2t_1}{\tau(E)}\right) \right] dE$$

and

$$(2) \qquad \tau^{-1} = \sigma(E)\; v_{th}\; N_c\; e^{E/kT} \quad .$$



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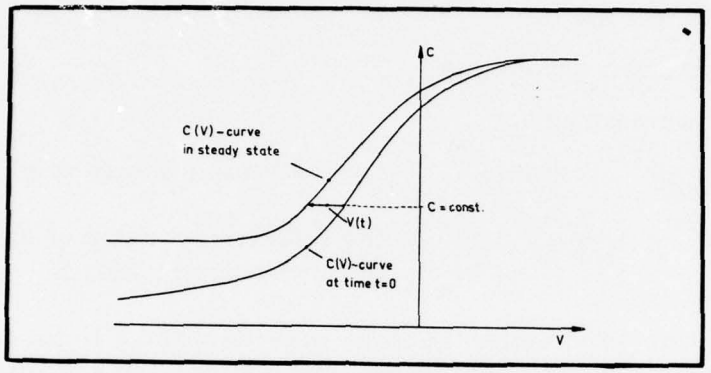

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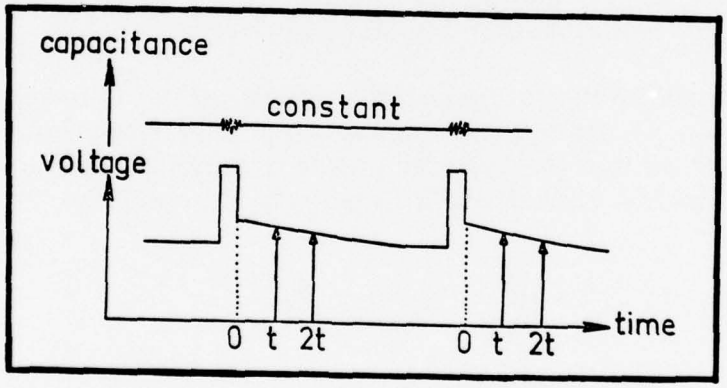

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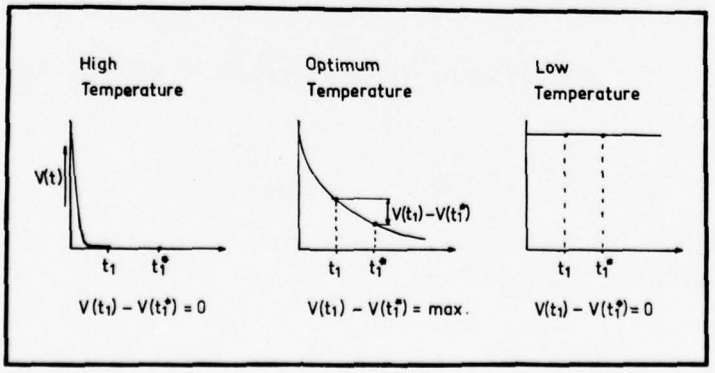


d

Fig. 1a - d Explanation of the CC-DLTS-Method

Here A is the area of the MOS capacitance,

C_{ox} the oxide capacitance

E the energy level of the interface state within the bandgap

E_s the energy of the deepest state still just charged and discharged by the bias V

$N_{ss}(E)$ the interface state density

$\sigma(E)$ the capture cross section

τ the response time of an interface state

t_1 the gate time

k the Boltzman constant

T the temperature

$v_{th} = 10^7 \cdot (\frac{T}{300})^{1/2}$ cm sec^{-1} the thermal velocity of electrons

$N_c = 2.8 \cdot 10^{19} \cdot (\frac{T}{300})^{3/2}$ cm^{-3} the effective density of states in the conduction band

In a first survey let us assume the capture cross sections to be constant and independent of the energy, and the response time τ of the interface states may be much larger than the gate time t_1. Then the integral (1) is independent of E_s which can be replaced by $-\infty$.

The weighting function in the integrand (= expression in the brackets) is sharply peaked (Fig. 2). Its halfwidth amounts to approximately $\pm$ 1.2 kT-units. On the condition that the interface state density $N_{ss}(E)$ does not change very much within the halfwidth range, the integral can be exactly calculated

$$\delta V(t_1, T) = \frac{kT}{q} \cdot \frac{A}{C_{ox}} \cdot N_{ss}(E_o) \cdot \ln 2 \qquad (3)$$

In this equation $N_{ss}(E)$ represents an averaged value of the interface state density in the vicinity of the maximum of the weighting function.

Somewhat arbitrarily the abscissa of the maximum is usually determined to be E_o:

$$E_o = kT \cdot \ln (\sigma v_{th} N_c \frac{t_1}{\ln 2}) \qquad (4)$$

This assignment can be more clearly interpreted: Transforming eq. (4) and a comparison with eq. (2) leads to

(5) $$\tau = \frac{t_1}{\ln 2} = 1.44\, t_1$$

This means: By selection of the gate times t_1 and $2t_1$ just these interface states are picked out which possess the response time τ .

Moreover it can be deduced from eq. (3): The energy interval in which the interface states mostly contributing to the correlation signal are located is given by

(6) $$\Delta E = kT \cdot \ln 2$$

Hence: In the validity regime of these approximations the weighting function of the integral (1) is replaced by a rectangular function that is shown in Fig. 2 by the obliquely hatched area.

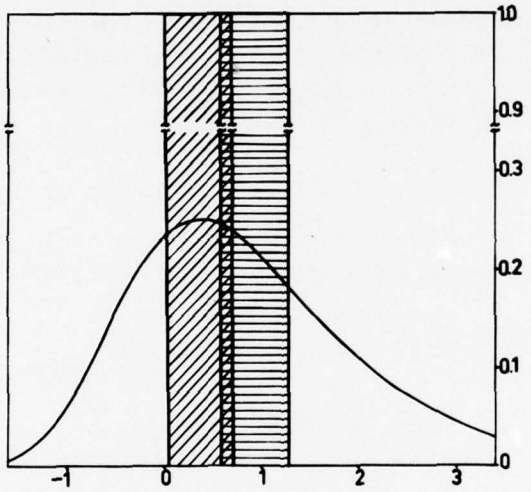


Fig. 2 Weighting Function $f(E) = \exp(-t/\tau(E)) - \exp(-2t/\tau(E))$
It is assumed that the capture cross sections are constant, especially that they do not depend on energy. The abscissa represents an energy axis in kT/q-units (it may include an additive constant). In special cases the correlation signal integral (eq. 1) can be performed explicitely (eqs. 3 and 10). This is equivalent to the fact that the weighting function may be replaced by the hatched approximations. The width of these functions is given by eq. (6): $\Delta E = kT \cdot \ln 2$.

An Improved Approximation

A more sophisticated consideration points out that the condition N_{ss} being constant over a limited energy range needs not to be rigorously observed. A linear relationship of $N_{ss}(E)$ on the energy may be permitted. In this case no more has to be done than to take the abscissa of the center of gravity of the weighting function for E_o instead of the maximum-abscissa.

A numerical computation shows that the eq. (4) and (5) have to be replaced by

$$E_o = kT \cdot \ln \left(\sigma(E_o) \cdot v_{th} \cdot N_c \cdot \frac{t_1}{2.52} \right) \tag{7}$$

and

$$\tau = 2.52\ t_1 \,. \tag{8}$$

When eq. (1) is applied in practice the assumption that σ has to be constant is greatly restrictive. This requirement can be replaced by a less severe condition. Only over a range of some kT/q-units in each interval the logarithmic derivation of σ should be constant:

$$\frac{d \ln \sigma}{dE} = \text{const} \tag{9}$$

With this all requirements for practical computation are virtually fulfilled.

Eq. (3) has only to be modified in

$$\delta V\,(t_1, T) = \frac{kT}{q} \frac{A}{C_{ox}} N_{ss}(E_o) \frac{\ln 2}{1 + kT \dfrac{d\,\sigma(E_o)}{dE}} \tag{10}$$

Evaluation Procedure

At least two correlation signals must be measured in dependence of temperature (usually in the interval from 50 K to 300 K) with two different gate times t_1 and t_2. Until now only the approximation (3) has been used for the evaluation. With this equation the interface state density $N_{ss}(E)$ can be extracted from the two correlation signals by

$$N_{ss}(E_o(t_i,\ T_i)) = \frac{C_{ox}}{qA \cdot \ln 2} \frac{q \cdot \delta V(t_i, T_i)}{kT_i} \tag{11}$$

where

$$i = 1,\ 2$$

If a certain value for N_{ss} has once been chosen and the temperatures T_1 and T_2 were determined in such a way that

$$N_{ss}(E_o(t_1, T_1)) = N_{ss}(E_o(t_2, T_2))$$

then the energy E_o and the capture cross section σ can be calculated by using eq. (5) or still better eq. (8).

(12) $$E_o = - kT_1 \frac{T_2}{\Delta T} \cdot \ln \left[\left(\frac{T_2}{T_1} \right)^2 \cdot \frac{\tau_1}{\tau_2} \right]$$

and

(13) $$\sigma(E_o) = \left[\frac{\tau_2 \cdot v_{th}(T_2) \cdot N_c(T_2)}{(\tau_1 \cdot v_{th}(T_1) \cdot N_c(T_1))^{T_1/T_2}} \right]^{\frac{T_2}{\Delta T}}$$

where $\Delta T = T_1 - T_2$.

These formulas are graphically represented in Fig. 3 and 4 with some typical values of the variables.

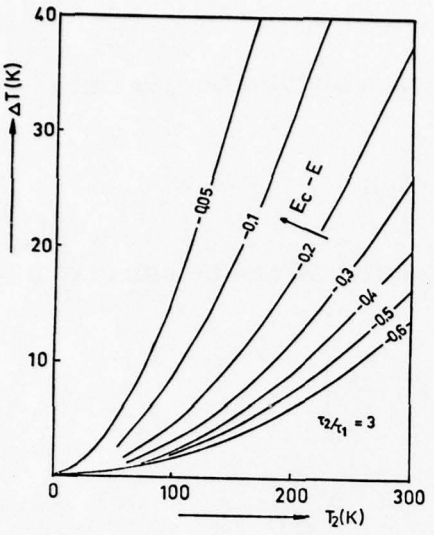
In the following we will show that this procedure for calculating E_o and is still defective because the energy dependence of is neglected. A generally applicable procedure is not yet tested. In the last paragraph of this chapter a proposal for such a procedure is given.

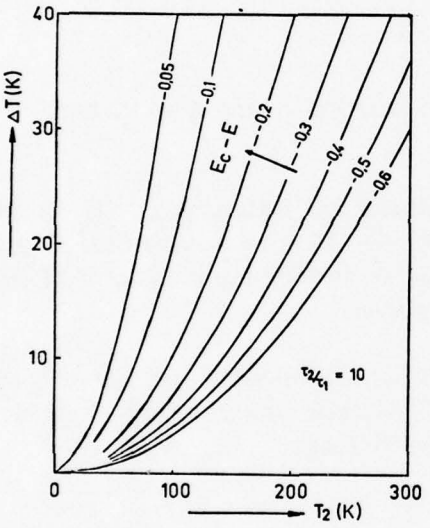
In order to compare at any rate the CC-DLTS-method with the conductance method the evaluation of the present CC-DLTS-data was merely empirically improved in particular cases by an individual fitting.

Experimental Results

In Fig. 5 to 7 measured readings and the evaluation results according to the quasistatic method the conductance method and the CC-DLTS-method are shown.

The measurements were carried out on three different MOS capacitors. They were prepared simultanously in the same process. Two of the samples (II and III) are even adjacent of the same Si-wafer. The wafers were thermally oxidized to an oxide thickness of 500 Å at a temperature of 950 °C. After the metallisation the wafers were annealed in an H_2-atmosphere at 400 °C for 30 min. The starting material was an epitaxy-(100)-Si-wafer with a resistivity of 4 ohm cm.





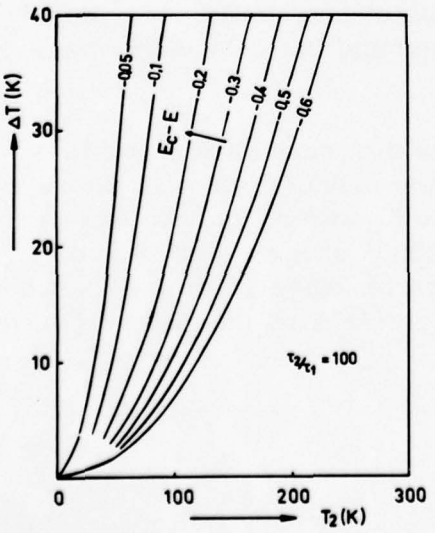


Fig. 3
Evaluation of eq. (12).
Correlation signals with different gate times t_1 , t_2 show apart from a certain change in magnitude a parallel displacement on the temperature axis. From this the energy and the capture cross section of the interface states which contribute mostly to the correlation signals at these temperatures can be determined.

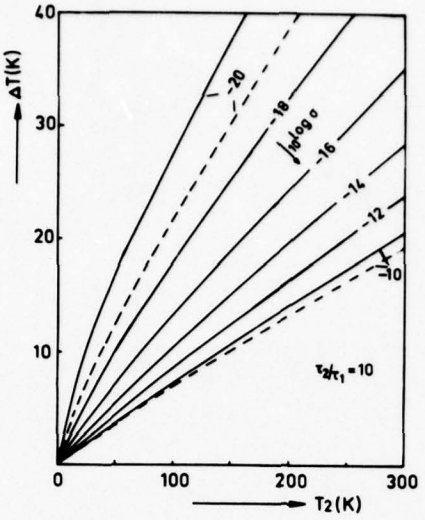


Fig. 4 Evaluation of eq. (13).
Cf. caption of Fig. 3. The full lines refer to a gate time of t_1 = 1 msec, the dashed lines refer to a gate time of 10 msec.

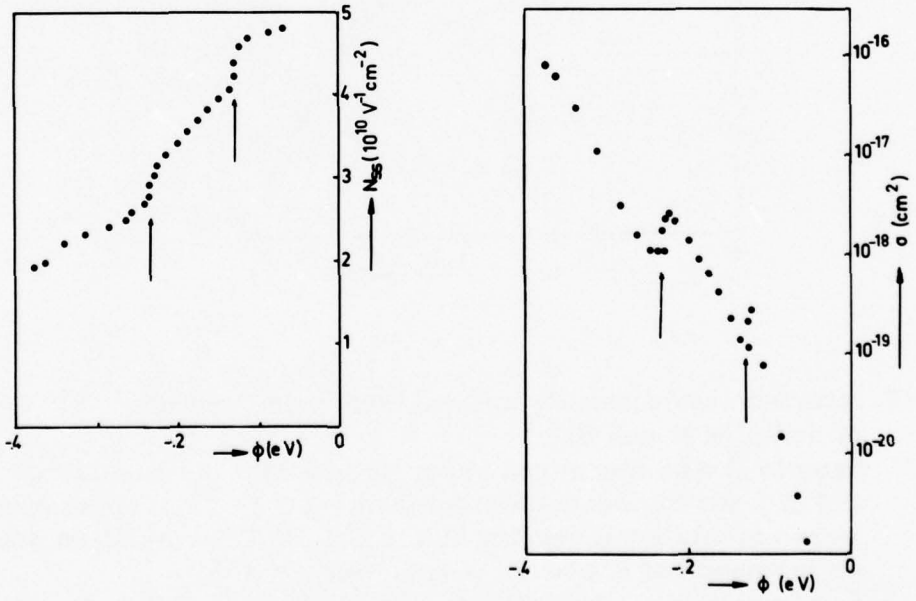


Fig. 5 Interface state density and capture cross section of sample I. The steps and peaks of these curves are artifacts caused by a too much simplified evaluation method.

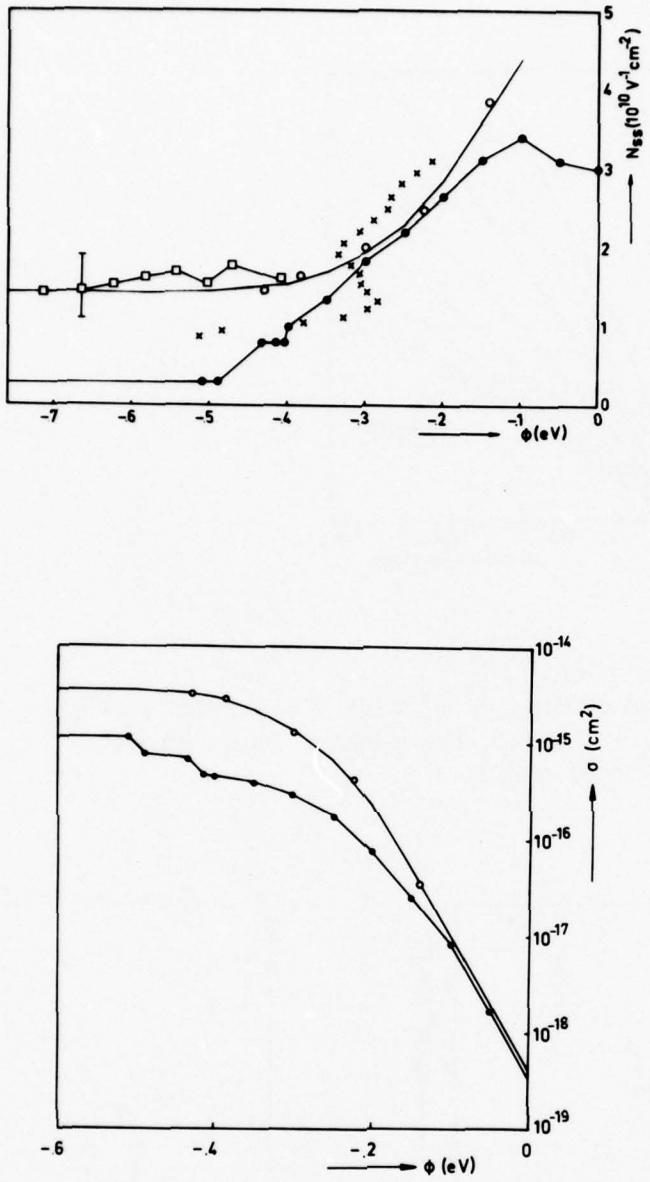


Fig. 6 Interface state density and capture cross section of samples II and III.
Sample II was measured according to both the quasistatic method (□□) and the conduction method (○○). The correlation signals were calculated according to the CC-DLTS-evaluation procedure so far used but it proved insufficient (××).
For lack of a mathematically well based evaluation we attempted empirically to reproduce the correlation signal by using polygonal traces for N_{ss} and σ. The optimum is surely not reached.
The results of the quasistatic measurement lie within the shown error margin for all three samples. This margin does not represent a scattering error but it means that all N_{ss}-values of each sample possess a constant additive error of this magnitude. The scattering error is smaller.

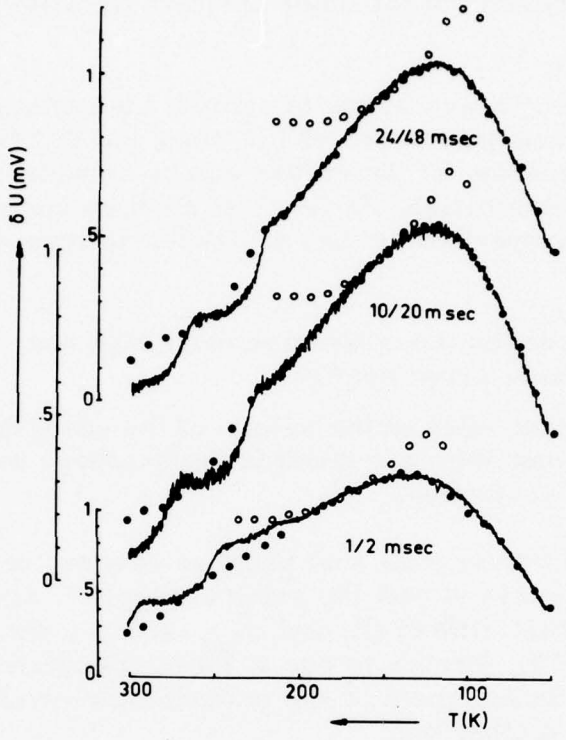


Fig. 7 Correlation signals of sample III.
The dots (• •) are calculated values (according to eq. (1)) as initial values the polygonal curves of Fig. 6 marked by the same dots were used for this purpose. The open circles (O O) are also calculated, the values of N_{ss} and σ were taken from the polygonal curve (Fig. 6) approximating the results of the conductance method.

Unfortunately the measurements could not be achieved with exactly the same sample as is desirable. Only the quasistatic method after Kuhn could be applied to all the samples. The result of only one sample is shown in Fig. 6a; the results of the other samples lie within the shown error margin.

The result of the CC-DLTS-evaluation of sample I according to the above described procedure (with gate times of 1/2 msec and 10/20 msec) can be seen in Fig. 5a/b. The shape of the curves can be considered to be typical for such an CC-DLTS-evaluation. At the first sight no contradiction arises to the interface state properties as they are received from the conduction method /2/:

- N_{ss}: an increase towards the conduction band edge and a relatively small error scatter
- σ : a nearly constant value in the middle of the bandgap and a pronounced decrease towards the bandedge with a large error scattering.

A more detailed inspection reveals that peculiar changes occur in both the N_{ss}-curve and the σ-curve at just the same energy (cf. arrows in Fig. 5a/b). This indicates that $d\ln\sigma/dE$ and N_{ss} are in a strong connection as it is stated by eq. (10). Errors of one of these magnitudes that may be caused by either the measurement or the mathematical evaluation result in similar errors of the other one.

Finally the CC-DLTS-method and the conductance method were cross-checked with the samples II and III.

The CC-DLTS-evaluation of sample III produced curves of untypical behaviour. Note for instance the retrograde portion of the N_{ss}-curve (Fig. 6). In this case the evaluation method must be made responsible for this peculiar behaviour. This shape is surely not an inherent property of the samples or an effect of the measuring errors. This can be seen by a slightly improved evaluation which shows a "normal" behaviour.

The conductance and capacitance measurements were performed in the frequency range between 500 Hz and 500 kHz and at temperatures between 140 K and 300 K. The results can also be seen in Fig. 6a and b.

To achieve a fair judgement we have to call to attention that the surface potential as received by the conduction method has an error of 1 - 2 kT/q-units. This error exerts an influence on the calculated value of the electron density and further on the capture cross section σ. Therefore the error of the capture cross section amounts to a factor of some e^1 to e^2, i.e. to a factor of about 5.

As we did not succeed in a straight-forward evaluation of the correlation signals we proceeded in the following way:

1. The values of $N_{ss}(E)$ and $\sigma(E)$ obtained by the conductance method (open circles in Fig. 6a/b) were used to calculate the correlation signals. In order to be able to use eq. (1) for this purpose the discrete values of N_{ss} and σ were interpolated by a smoothed polygonal trace, and outside the range where conductance measurements could be employed the polygonal trace was reasonably continued.

   In Fig. 7 the measured correlation signals and the computed ones (open circles) are shown.

2. By changing these polygonal traces in a suitable way we attempted to get a better approximation of the correlation signals. This could be accomplished to some degree (black dots in Fig. 7). It is difficult to assess, however, when the best possible approximation is reached. Nevertheless the measured and the computed correlation signals agree quite well in the temperature range up to about 220 K. The interface state density and the capture cross section of the region between -0.05 eV and -0.4 eV mainly contribute to the values in that temperature range. Just in this region the values measured by the conductance method agree sufficiently with the improved polygonal curves which were chosen for a better fitting with the correlation signals. We did not try hard to improve the approximation to the correlation signals in the higher temperature range. There the readings show a weak reproducibility (Fig. 8). This indicates that minority carriers are about to be generated. This is not implied in the present theory.

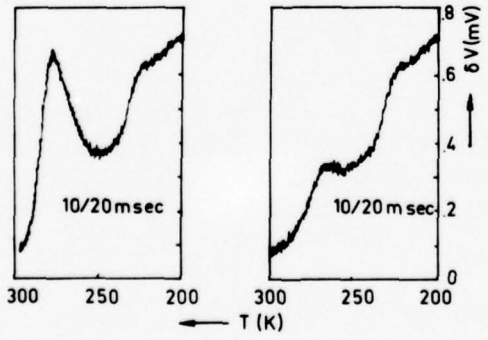


Fig. 8 Correlation signals in weak inversion.
The two correlation signals were obtained with the same adjustments of the measuring equipment. The interface states, which are situated in the energy gap in such a way that they can only be seen when the bias is in weak inversion, are responsible for these signals. It is supposed that the differences are due to the different previous treatments of the samples just before the measurement.

In conclusion it may be stated:

It is possible to achieve a reasonable agreement between the CC-DLTS-method and the conductance method. It is desirable to improve the CC-DLTS-data evaluation and to establish a sound error analysis.

Proposal for Improving the Evaluation Method

Several unsuccessful attempts revealed that in the course of any calculation one should avoid numerical differentiations like $d\sigma/dE$ or $d\ln\sigma/dE$. The errors accumulate too much by propagation.

In the following we suggest an iteration method in which no numerical differentiation is needed. The proposed derivation is still advantageous for another reason. Not only two but any quantity of correlating signals $V(t_i, T)$ with different gate times t_i can be taken into account without giving preference to any of these signals.

The procedure starts with eq. (7) and eq. (10). In order to obtain a deeper insight into the mathematical schema the names of the variables are changed in the following way

$$\begin{aligned} \delta V(t, T) &\rightarrow F(t, T) \\ E(t, T) &\rightarrow f(t, T) \\ N_{ss}(E) &\rightarrow u(f) \\ \sigma(E) &\rightarrow v(f) \\ \frac{d\ln\sigma(E)}{dE} &\rightarrow w(f) \end{aligned}$$

The functions $F(t_i, T)$, where $i = 1, 2 \ldots n$ and $n \geq 2$, are given by experiment over a sufficiently large interval of T. The functions $u(f)$ and $v(f)$, which are of physical significance, are unknown and have to be found. During the calculation the function $f(t, T)$ and $w(f)$ have to be considered also as unknown.

All these functions are connected by the following relations

$$F(t_i, T) = A \cdot T \cdot \frac{u(f(t_i, T))}{1 - BT\ w(f(t_i, T))} \qquad i = 1, 2, \ldots n \tag{14}$$

$$t_i^{-1} = C \cdot v\,(f(t_i, T)) \cdot T^2 \cdot \exp\left[f(t_i, T) / BT\right] \tag{15}$$

$$w(f) = \frac{d\ln v(f)}{df} \tag{16}$$

A, B, C are known constant values.

As an initialisation step one must make a reasonable assumption about the function w(f). Let us call this initial approximation $w_o(f)$.

1. Step: According to eq. (16) one calculates v(f) by

$$v(f) = k \cdot \exp\left[\int w_o(f)\right] df$$

where k is an integration constant.

2. Step: Any magnitude of f is chosen. Then one calculates T_i in such a way that according to eq. (15) the equations

$$t_i^{-1} = C \cdot v(f) \cdot T_i^2 \cdot \exp\left[f/BT_i\right]$$

are satisfied.

Note that in this case the relation

$$f \equiv f(t_1, T_1) = f(t_2, T_2) = \ldots$$

is fulfilled.

3. Step: The eqs. (14) in connection with

$$u_1(f) \equiv (f(t_1, T_1)) = u(f(t_2, T_2)) = \ldots$$

and

$$w_1(f) \equiv w(f(t_1, T_1)) = w(f(t_2, T_2)) = \ldots$$

are considered to be a system of conditional equations with the unknown quantities $u_1(f)$ and $w_1(f)$. This system must be solved.

If $n>2$ the system is overdetermined. The equations in excess can be used to improve the accuracy for instance by a least square fit. When repeating the steps 2 and 3 with different f one receives first approximation functions $u_1(f)$ and $w_1(f)$ for the unknown functions u(f) and w(f).

4. Step: Step 1 and the following ones are repeated with the new and probably improved values $w_1(f)$ *instead of* $w_o(f)$. If the procedure converges the iteration may be stopped.

The convergence and the suitable choice of the integration constant k have still to be investigated in detail.

II. Conductance Measurements on Implanted and Non-implanted MOS Structures

The conductance method is the most reliable method for measuring capture cross sections of MOS structures at the present state of the art. Because up to now only a few measurements of this kind have been performed, we first looked for an element to be implanted that could be used as a model to study the phenomena involved and which permitted a test of the investigation methods concerned.

We started out with cesium as implantation element. We picked this element because it exerts a clear effect on the Si-SiO_2 interface:

- Cesium accumulates in the interface during the oxidation process /5/ and it causes - like all alkali metals - a large flatband shift.

On the other hand cesium-implanted samples do not show effects which render the measurement and the evaluation difficult:

- The mobility of cesium in Si and SiO_2 is small at room temperature /6/ and all the more so at lower temperatures. Therefore the samples are insensitive to ion migration, i.e. they are stable and do not show hysteresis.

- So far cesium is assumed to have no states near the bandedges. This means there is no additional (resistivity) doping profile. Therefore the surface potential is easy to calculate and the energy levels of the interface states under investigation are unequivocably determinable. Especially with cesium we hardly find any difference of the surface potential if we calculate on the one hand from the low-frequency c-v-curve (by the Berglund-Integration) and on the other hand from the high-frequency c-v-curve (Fig. 9).

In a first measuring run we investigated pure (≈ non-implanted) MOS capacitors in order to be able to separate the intrinsic from the extrinsic properties induced by the implantation element.

Conduction Measurements on Pure (Non-implanted) Samples and the Limits of the Conduction Method

Previous experimental investigations confirmed the following statements of interface state properties:

1. The interface state density is at a minimum near the center of the bandgap and increases towards the bandedges.

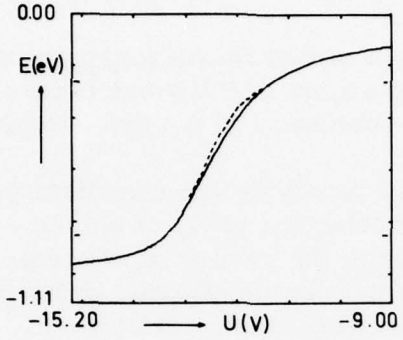


Fig. 9 Energy E (referred to the conduction-bandedge) of the interface states that contribute mostly when bias is set to the voltage U. The curves relate to the Cs-implanted n-type-MOS-capacitor. The initial data of the full line curve comes from the lf-c-v-curve by the Berglund-integration. The dashed curve was computed from the hf-c-v-curve. It is less important that the values of the two curves agree (error of the integration constant). Parallelism is more important. In the event of deviations a doping profile near the interface would be present or the frequency of the hf-measuring voltage was chosen too low. In this particular case the parallelism is quite good, the r.m.s. deviation amounts to only .5 kT/q-units.

2. The capture cross sections are constant in the center of the bandgap and decrease towards the majority carrier bandedge. This is mainly true for n-type-Si-samples. Until now the accuracy has been insufficient in the case of p-type-Si to verify the decrease of the capture cross sections without any doubt.

In the meantime the preparation technique has been improved; the interface state density has been clearly lowered. Therefore it was necessary to perform the same measurements on samples recently produced.

The results are nearly the same as stated in the foregoing rules (Fig. 10). But with the new samples the limitations of the conductance method become more conspicuous. This applies especially to p-type-samples.

The incurred limitations are given partly by the technical possibilities of the equipment and partly by - and this to a greater extend - the properties of the samples themselves. Although the causes of these particular properties are not yet fully understood, the circumstances under which these restrictions get important are reported in more detail here.

The conductance method is an accurate investigation of the frequency dispersion of the MOS capacitor admittance. The relaxation frequency is given (save a factor of magnitude close to 1) by

$$f_R \propto \sigma(E) \cdot v_{th}(T) \cdot N_c(T)\, e^{E/kT} \tag{17}$$

Here $\sigma(E)$ means the capture cross section

v_{th} the thermal velocity of electrons

N_c the effective density of states of the conduction band

E the energy of the investigated interface state

T the temperature.

Three causes limit the measurement and the evaluation:

- The technical set-up of the measuring equipment,
- the properties of the samples and
- the assumption about the model of the MOS structure.

Precise capacitance and conductance measurements are limited by being technically restricted to a frequency range from 10 Hz to 50 MHz. If the temperature is to be varied during the measurement and the sample is

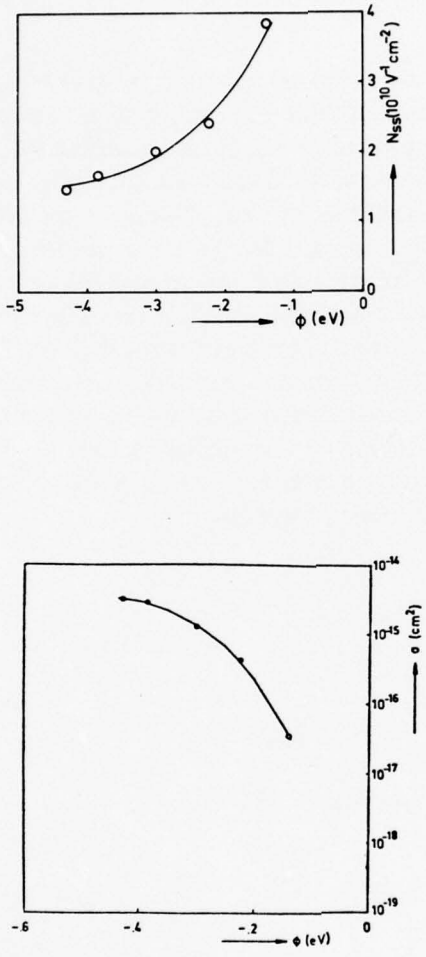


Fig. 10 Interface state density N_{ss} and capture cross section σ of an non-implanted n-type-MOS-capacitor. The points were obtained by the conductance measuring technique in the temperature range from 140 K to 300 K.
(The same values have already been given in Fig. 6.)

therefore inserted in a cryostat, the frequency range is further narrowed down by disturbances introduced by the electric cable leads.

The relaxation frequency must be shifted into a frequency range that is amenable to technical measurements. This can be done by a suitable adjustment of the bias voltage (or rather the surface potential) and the temperature. The temperature influences the relaxation frequency both by the temperature dependent level of the Fermi energy and by the exponent E/kT in eq. (17).

In Fig. 11a an equivalent circuit of an MOS capacitor is given in a first approximation. Only the total admittance of the circuit can be measured (Fig. 11c). In order to obtain the physically relevant quantities C_p and G_p the oxide capacitance must be deducted. This can be done best if the oxide capacitance C_{ox} is as large and the space charge capacitance C_{sc} is as small as possible. To keep C_{sc} small large band bending and low temperatures are favorable. On the other hand, in order to cover the full energy gap up to the majority carrier bandedge small band bending is necessary. This means measurements have to be performed near flatband point or in the accumulation region. By this circumstances contradictory conditions arise and a limit of the conductance method is reached: in this range the frequency dependent variations of the admittance $G_m + j\,C_m$ become small. The requirements with respect to the stability of the samples and the accuracy of the bridges rise sharply.

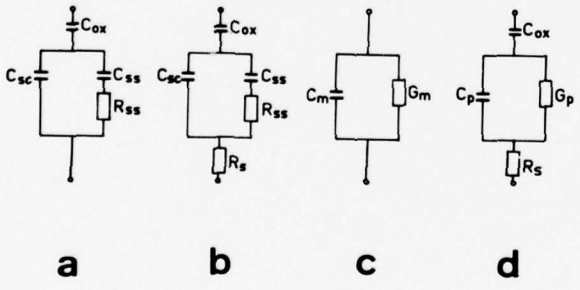


Fig. 11 Equivalent circuits of MOS capacitors.
C_{ox} = oxide capacitance, C_{sc} = space charge capacitance, C_{ss} = capacitance of the interface states, R_{ss} = resistance of the interface states, R_s = bulk resistance of the wafer

a) Greatly simplified equivalent circuit
b) Same as Fig. a, but the bulk resistance of the wafer is taken into consideration
c/d) Circuits by which some auxiliary quantities are defined.

Very often one cannot even approach this limitation due to the shortcoming of the equipment. The equivalent circuit in Fig. 11a is too much simplified. First one realises that the frequency dispersion is much greater than can be expected according to the simple equivalent circuit. Furthermore, one must take into account the bulk-resistivity of the wafer and the reactance of the back contact.

The broadening of the dispersion is explained by the "statistical model" /1/. According to this the broadening is a direct consequence of surface potential fluctuations which are caused by the random distribution of charged oxide traps and charged interface states. Because of the surface potential fluctuations interface states of a wider energy range and hence of a broader response time range are able to participate in the charging processes.

This relaxation broadening has always set a limit to the p-type-MOS-structures. At low temperatures the relaxation range is spread totally over the frequency band that can be covered by the capacitance bridges. Near the bandedges p-type samples could never be measured reliably.

The present p-type-samples can only be evaluated with serious reservations due to the shape of the G_p/ω-curves, even at room temperature (Fig. 12). The causes for their wide broadening have not yet been investigated.

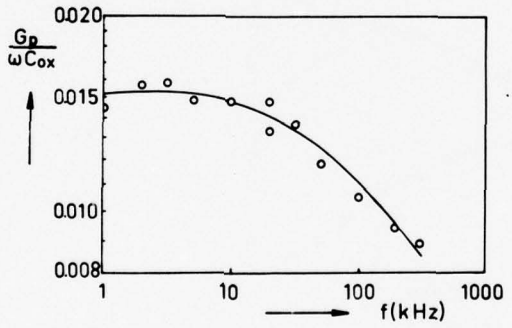


Fig. 12 The $G_p/\omega C_{ox}$ vs. frequency-curve of the non-implanted p-type-MOS-sample. The measurement was performed at a bias of -0.85 V and at room temperature. It is striking that the relaxation spreads over a wide frequency interval. Corresponding to the small capture cross section of this sample the relaxation frequency is low. Generally spoken it is possible to shift the relaxation frequency into a more favorable range by adjusting the bias. But then the differences between the hf- and the lf-capacitances become even smaller and an evaluation is impossible. At this particular bias we have a dispersion of the admittance of about $\Delta C_m \approx G_m/\omega \approx 0.1$ pF with $C_m \approx 38$ pF. All information about the interface states are contained in these small differences.

Capacitance measurements (without conductance measurements) can be executed in a more extended frequency range. With the particular sample of Fig. 12 we could not see another capacitance step (i.e. no other relaxation). With a relaxation frequency of about 3 kHz one obtains a capture cross section in the order of

$$\sigma = 3 \cdot 10^{-17}\ \mathrm{cm}^2$$

at an energy of 0.34 eV from the valence bandedge. The evaluation of the quasistatic method and of the G_p/ω-curve of Fig. 12 result in the same value

$$N_{ss} = 2 \cdot 10^{10}\ \mathrm{V}^{-1}\ \mathrm{cm}^{-2}\ .$$

Only the pronounced relaxation broadening and the relatively small capture cross section are striking, all the other properties of this sample look normal.

Often another difficulty arises in the intermediate region from depletion to accumulation. An additional electric loss can be observed. It is seen in the asymmetric shape of the $G_p/\omega C_{ox}$-curve (Fig. 13).

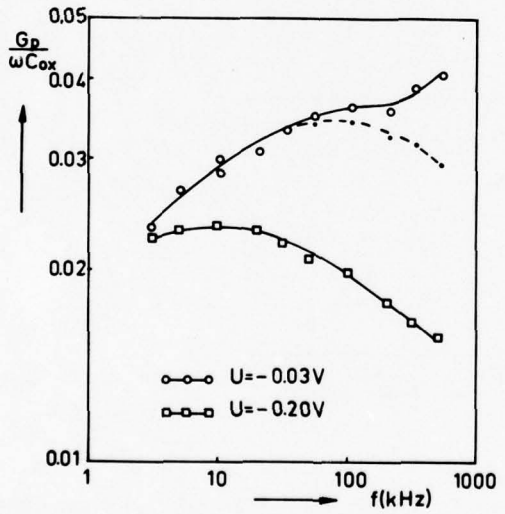


Fig. 13 G_p/ω-curves of the non-implanted n-type-MOS-sample at two different bias-voltages and at 140 K.
Measurements in depletion yield almost symmetrical bell-shaped curves which agree to the statistical model. With measurements, still in depletion but closer to accumulation, another loss can be observed. In particular cases this loss appears to be caused by a series resistance R_s (Fig. 9b). The dashed curve was obtained by taking a resistance of 3 ohm into account. A physical interpretation of this loss has not been found.

They are no more bell-shaped like the curves attributed to the normal interface states (cf./2/). The relaxation frequency of these peculiar losses lie far in the MHz-range. With the present experimental set-ups only the increase of the low frequency branch can be observed. In particular cases this increase can formally be ascribed to a series resistance (Fig. 11b). It seems obvious that this resistance and the bulk resistance of the wafer are identical. But this cannot be true: It is seen from Fig. 13 that the curve becomes symmetrical if we tentatively take a resistance of 3 ohm into account. The series resistance of the bulk (epitaxy-wafer), however, amounts only to 2 ohm at room temperature. At 140 K it may be neglected because of the greatly increasing mobility of the charge carriers.

Recently Morita et al. /7/ investigated such an additional loss in the frequency range between 1 MHz and 100 MHz at room temperature. They successfully covered the whole relaxation regime but were also unable to explain the effect.

MOS Structures Implanted with Cesium

In these experiments we used the same base material as in the experiments with the non-implanted samples. The implantation was performed after cleaning the wafer and before oxidation. The implantation energy was chosen to 60 kV and the doses to 10^{13} cm^{-2}. This corresponds to a projected range of 300 Å. The oxide was grown to a thickness of 1850 Å by a dry-wet-dry process. After the metallisation the samples were annealed in an H_2-atmosphere at 400 °C for 30 min. The results of the quasistatic method and the conductance method are shown in Fig. 14a/b.

Remarks about the reliability of the measurements: The results of the quasistatic measurements are given in Fig. 14a with error bars. The conductance measurements show in the G_p/ω-curves more pronounced asymmetry as is expected according to the statistical model. The high- and low-frequency branch of these curves can be fitted to different surface potential variances σ_g. This causes an uncertainty of about 20 % for the interface state density N_{ss}. The measurements at low temperatures down to 197 K - this corresponds to the measurement values in the neighbourhood of E = -0.2 eV - were difficult to obtain. To shift the relaxation frequency into the region of the capacitance bridges the measurements had to be performed in the proximity of the flatband point. The capacity dispersion amounts at this point to but ΔC_m = 0.2 pF at C_m = 33.5 pF. The dispersion losses are correspondingly small. For this reason the interface state density N_{ss} is uncertain at this point. The capture cross section determined from eq. (17), however, has the usual accuracy of 1/2 to 1 order of magnitude because the calculation of the surface potential (i.e. the energy level E) is independent of the dispersion and the relaxation frequency is relatively well defined.

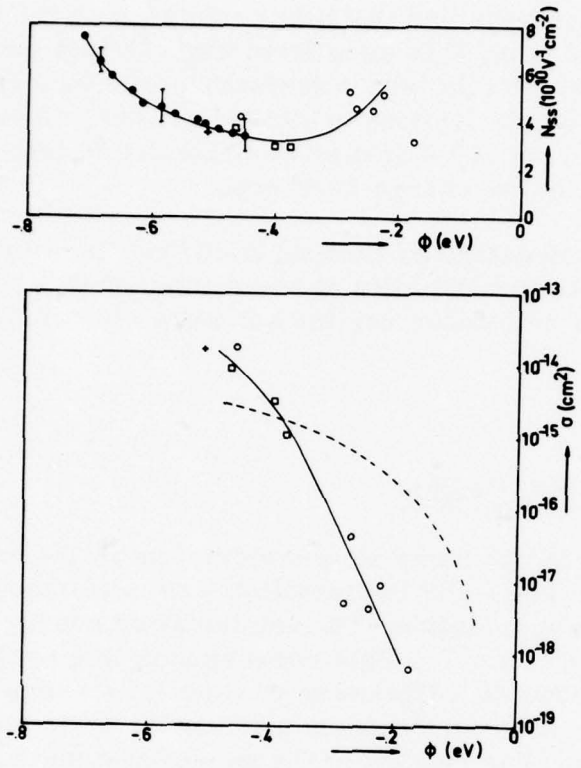


Fig. 14 Interface state density N_{ss} and capture cross section σ of a Cs-implanted n-type-MOS-capacitor.
The black dots represent the result of the quasi-static method. The other results come from the conductance method. Several capacitors on the same wafer were used. The measurements were performed with temperatures from 197 K to 300 K. The dashed curve is a result of an CC-DLTS-evaluation using a too much simplified approximation.

In Fig. 14b the functional dependence of the capture cross section as obtained by the CC-DLTS-method has been marked by a dashed line. But as has been discussed in Chap. I the presently used mathematical procedure to apply the CC-DLTS-method is wanting of improvements. It is too early to make a comparison.

The results of the Cs-implanted p-type sample are quite different from the non-implanted p-type structures. Conductance has been measured at 300 K at the frequency range from 500 Hz to 20 MHz and at 288 K in the narrowed down range from 500 Hz to 500 KHz. At 300 K we found two relaxations: one in the neighbourhood of about 2 KHz, the other at about 2 MHz. These two relaxations can be interpreted as two different states of the same energy but with different capture cross sections. The relaxation broadening can only roughly be estimated because the adjacent branches of the two maxima overlap and the correct shape of each of them cannot be seen. But it is perceivable that the broadening is smaller (σ_g = 2 ... 3.5) than that of the non-implanted sample (σ_g = 4).

The evaluation of the G_p/ω vs. f-curve together with the result of the quasistatic measurement is given in Fig. 15. We used the quasistatic measurement according to Kuhn (cf./2/). The frequency (1 MHz) which was used in this measurement to obtain the hf-c-v-curve is still within the relaxation regime. Therefore the computed values of N_{ss} are too small. It is reasonable that the sum of the interface state density obtained by the conductance method is somewhat greater than the result of the quasistatic measurement.

In Fig. 15 the capture cross sections are also shown. The large values (up to 10^{-11} cm^2) are striking. A pronounced decrease to the valence bandedge is seen.

On the other hand, these statements become questionable when being compared with the measurements at 288 K. At this temperature the conductance measurements were carried out between midgap and accumulation with frequencies between 500 Hz and 500 KHz. Here too, relaxation maxima are found at frequencies about 1 KHz and lower. Further a large increase of the losses are seen at the high frequency end. One must assume that the relaxations frequencies lie far in the MHz-range.

The low frequency relaxation can certainly be considered as an effect of minority carriers (electrons). This must be concluded from the dependence of these maxima on the surface potential. The maxima increase in height and become peaked the more the surface potential approaches weak inversion. The high frequency maxima cannot be measured. The steep increase of the losses indicate a concomitant increase of N_{ss} towards the valence-bandedge. One might also think of an increase (!) of the capture cross sections towards the valence-bandedge but this would be opposite to the findings at 300 K.

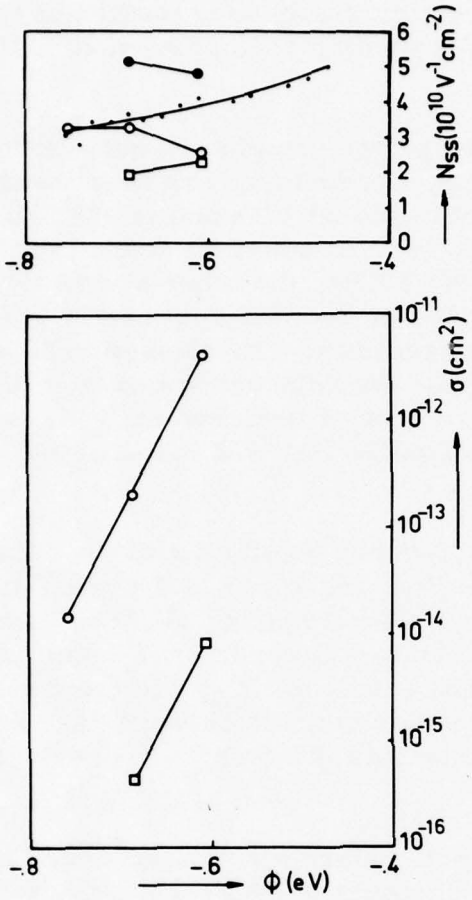


Fig. 15 Interface state density N_{ss} and capture cross section σ of a Cs-implanted p-type-MOS-capacitor. The small dots are the result of the quasistatic method. The hf-frequency (1 MHz) was certainly to low for this measurement. Therefore the shown values give only a lower limit.
The other points were measured by the conductance method at 300 K. This sample possesses two maxima of G_p/ω at the same surface potential. These maxima can be attributed to two different interface states at the same energy (circles, squares). Their sum is marked by large black dots.
Conductance measurements at 288 K, however, let appear these statements questionable.

Also a third possible interpretation is contradictory: The high frequency losses may be the same of unknown origin as those found by Morita et al. /7/. And the low frequency losses are minority carrier effects not only at 288 K but also at 300 K. In order to be able to interpret the measurements at 300 K one must assume that the capture cross sections for electrons are large. But this is in contrast to the foregoing measurements on n-type-structures.

In conclusion it can be stated:

1. An evaluation according to the statistical model is possible in the case of non-implanted and Cs-implanted n-type Si-MOS-structures. The capture cross section drops towards the conduction band edge. For the implanted sample the decrease is steeper and the capture cross sections are smaller. The implanted sample cannot be investigated as close to the bandedge as the non-implanted one because in consequence of the small capture cross sections the relaxation fall into frequency ranges which are unfavorable to bridge measurements.

2. Difficulties arise when p-type-Si-MOS-structures are measured by the conductance method. The origin of these difficulties are found in a small capture cross section (for holes) and a large dispersion broadening with the non-implanted sample. The measured data of the Cs-implanted sample cannot yet be discussed without encountering contradictions.

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Appendix A 1

The Physics of SiO_2 and Its Interfaces
Proceedings of the International Topical Conference
Yorktown Heights, New York
March 22 - 24, 1978
Editor: S. T. Pantelides

TRANSIENT CAPACITANCE MEASUREMENTS OF ELECTRONIC STATES AT THE SiO_2-Si INTERFACE

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ABSTRACT

Deep-level transient spectroscopy (DLTS) has been applied to measure the energy distribution and capture cross-section of electronic trapping centers at the Si-SiO_2 interface. The experimental and analytical techniques for DLTS analysis of interface states in MOS structures are summarized, and results from combined capacitance-voltage and DLTS measurements of a characteristic discrete level at the oxidized silicon surface are presented.

INTRODUCTION

The interface between thermally-grown SiO_2 and Si is generally found to possess a continuous distribution of electronic trapping centers which extends throughout the Si forbidden energy band, with the density monotonically increasing with energy toward the band edges from a minimum near midgap (1). The metal-oxide-semiconductor (MOS) structure has been extensively used to study these states. From conductance measurements on MOS capacitors (2,3) and charge transfer loss measurements on charge-coupled devices (4) it is found that the cross section for electron capture by fast surface states is constant over the midgap region, but decreases rapidly with energy near the Si conduction band. Deep-level transient spectroscopy (DLTS) (5) is an alternative technique for studying interface states which features high sensitivity and complements the above techniques for measuring dynamic interface properties in that it is not affected by surface potential fluctuations, which arise from the random spatial distribution of fixed positive charge in the oxide. In addition, the technique has been used to measure bulk defects introduced by ion implantation in the near-surface region of MOS structures (6). Here we summarize the experimental and analytical techniques for the DLTS analysis of interface states and present combined capacitance-voltage (C-V) and DLTS measurements of a characteristic discrete level at the Si-SiO_2 interface.

DLTS MEASUREMENTS ON MOS STRUCTURES

DLTS is a transient capacitance technique which was developed by Lang (5) to measure deep levels in bulk semiconductors. A block diagram of the apparatus is shown in Fig. 1. The

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measurement system consists of a capacitance bridge with fast transient response, a pulse generator for rapidly changing sample bias, a dual-gated signal integrator and X-Y recorder, and a variable temperature cryostat. For studying interface states in MOS structures, the system in Fig. 1 includes a feedback loop which maintains the capacitance of an MOS device at a constant value by varying the gate voltage. Thus, the monitored signal is a voltage transient. In the next section we show that the constant-capacitance DLTS, or CC-DLTS, technique offers significant advantages for the analysis of interface states in MOS structures.

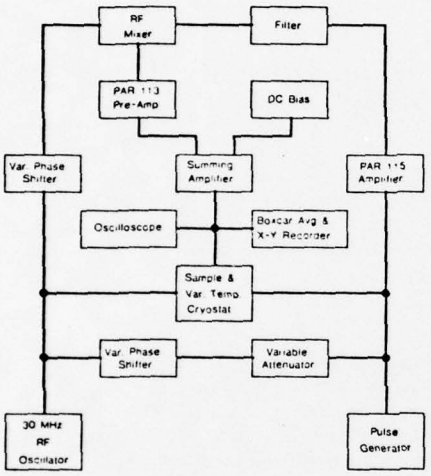

Fig. 1. Block diagram of apparatus for constant-capacitance DLTS (CC-DLTS) measurements of interface states in MOS structures.

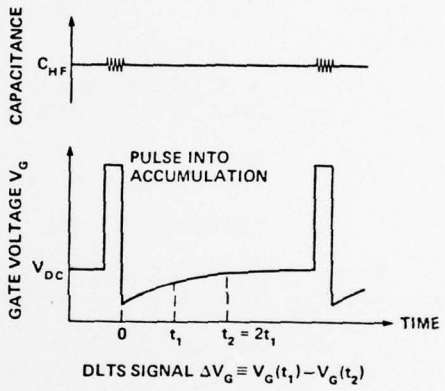

Fig. 2. Schematic diagrams of the capacitance variation and voltage transient in a CC-DLTS measurements.

The experimental procedure involves first biasing an MOS device into depletion. Superimposed on the dc bias is a charging pulse which drives the semiconductor surface into strong accumulation in order to populate the interface states with majority carriers. After a charging pulse, the gate voltage varies with time as the occupation of the interface states returns to its equilibrium distribution.

The voltage transient is schematically illustrated in Fig. 2. At low temperatures (<300 K) and short times (~1 msec) the transient arises from the emission of majority carriers and consists of a superposition of many exponentially decaying signals, since the interface traps are distributed in energy and hence emit their charge at different rates. With the DLTS technique these signals can be deconvolved. The CC-DLTS signal, ΔV_G, is obtained by forming the difference of the gate voltages measured at two delay times t_1 and t_2 after a charging pulse, as shown in Fig. 2. The signal is measured in a temperature scan, and good noise discrimination is obtained by time averaging over many cycles with a boxcar averager or on-line computer.

THEORY OF CONSTANT-CAPACITANCE DLTS MEASUREMENTS

For majority carrier emission from interface states, the CC-DLTS signal is readily shown to be proportional to the change with time of the net charge in interface states after a charging pulse.

Since the depletion capacitance of the semiconductor is held constant during the transient response, the change in gate voltage required to maintain a constant capacitance appears only across the oxide layer, and the emission signal ΔV_G is related to the net charge (per unit area) in interface states, Q_{is}, as follows:

$$\Delta V_G = (1/C_{ox})[Q_{is}(t_1) - Q_{is}(t_2)], \tag{1}$$

where C_{ox} is the oxide capacitance per unit area. The gate-voltage transient is thus linearly proportional to the difference in the net charge in interface states at the two delay times t_1 and t_2 after a charging pulse. This linear dependence obtains for all interface trap densities, and the proportionality factor is independent of substrate doping and temperature. By contrast, in DLTS transient-capacitance measurements with fixed gate voltages, linearity is lost at high interface-state densities, and the proportionality factor depends on substrate doping and varies with temperature.

For electron emission from a continuous distribution of interface traps, the CC-DLTS signal is

$$\Delta V_G = (1/C_{ox}) \int qN_{is}(E) \, [\exp(-t_1/\tau_n) - \exp(-t_2/\tau_n)] \, dE, \tag{2}$$

where τ_n is the electron emission time constant which from considerations of detailed balance may be expressed as

$$1/\tau_n = \sigma_n v_n N_c \exp(-E/kT). \tag{3}$$

The quantities appearing in the above equations are defined as follows: q is the electronic charge, $N_{is}(E)$ is the interface-state density at an energy E below the conduction-band minimum, σ_n is the capture cross-section for electrons, v_n is the mean thermal velocity for electrons, N_c is the effective density of states in the Si conduction band, k is the Boltzmann constant, and T is the absolute temperature. In Eq. (2) it is assumed that the traps are completely filled during a charging pulse. The exponential terms in the integrand of Eq. (2) form a function which for $t_2 = 2t_1$ is peaked at an energy $E_o = kT \, ln(\sigma_n v_n N_c t_1/ln2)$. For a constant capture cross-section this function is sharply peaked, and the integral can be solved by assuming that N_{is} varies slowly over an energy interval of order kT. We obtain

$$\Delta V_G = q \, kT \, ln2 \, N_{is}(E_o)/C_{ox}. \tag{4}$$

Thus, the emission signal, divided by temperature, is directly proportional to the interface-state density at the energy E_o. The energy interval over which interface traps contribute to the DLTS signal is $\Delta E = kT \, ln2$. Both the width of the interval, ΔE, and its location in energy, E_o, increase linearly with temperature. The energy resolution is therefore greatest at low temperatures where the sampled interval is closest to the conduction band and the interface-state density is expected to vary most rapidly. The larger energy intervals obtained at high temperatures provide enhanced sensitivity for detecting low densities of interface states which are typically found near midgap.

RESULTS AND DISCUSSION

CC-DLTS Spectra in an N-Type MOS Structure

Several qualitative features of CC-DLTS measurements on n-type MOS capacitors can be illustrated by examining Fig. 3. This figure shows DLTS spectra obtained with delay times t_1,t_2

= 1,2 msec for different fixed depletion capacitances and also one spectrum for t_1,t_2 = 10,20 msec. In n-type MOS capacitors, the DLTS signal arises from the emission of electrons from interface states in the upper half of the Si bandgap. Below room temperature the DLTS signal is independent of the device capacitance, provided that the capacitor is biased far enough into depletion so that under equilibrium conditions the Fermi level intersects the interface below the Si midgap. In this temperature regime the signal is dominated by majority carrier emission. The rapid drop in the emission signal at temperatures below ~130 K may arise from a dependence of the capture cross-section on energy near the Si conduction band. Above 300 K the DLTS signal is strongly dependent on the depletion capacitance and increases rapidly as the device is biased further into depletion. The peak at ~335 K and the sharp increase in the signal at higher temperatures occur when the capacitor is biased near inversion and is ascribed to the onset of minority carrier emission and capture processes at the interface.

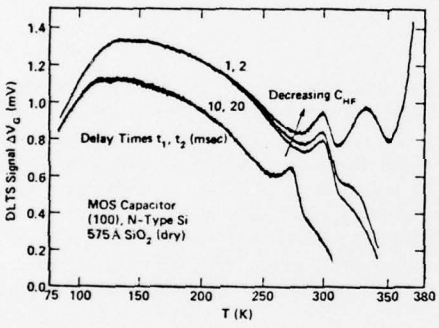

Fig. 3. CC-DLTS spectra for an n-type MOS capacitor for different bias conditions and delay times

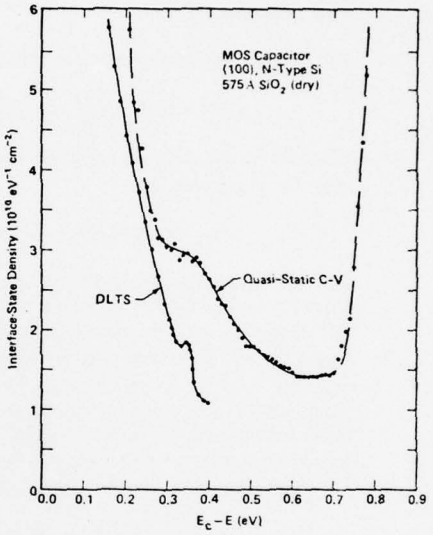

Fig. 4. Interface-state distributions for the capacitor of Fig. 3 obtained by the quasi-static C-V technique and from a DLTS analysis, with a constant capture cross-section of 10^{-18} cm^2.

The analysis presented in the last section is applicable over the region of the spectrum where the signal is dominated by electron emission and the capture cross-section can be assumed to be a constant. The interface-state distribution at midgap cannot be determined from DLTS data with the analysis presented here due to the onset of minority carrier effects at high temperatures. Also, contrary to a previous report (7), the analysis is not sufficient to determine the possible existence of a thermally activated capture cross-section. The emission spectra in Fig. 3 can be used to compute both σ_n and the energy scale for the interface-state distribution. The shift of the spectrum with delay time over the temperature range from ~130 K to room temperature is consistent with a capture cross-section that is constant or varies slowly with energy. The data can be adequately fitted with a σ_n of 10^{-18} cm^2. In Fig. 4 is shown the interface-state distribution obtained from the DLTS analysis. For comparison the

distribution as measured by the quasi-static C-V technique (8) is also shown. In both distributions the density increases with energy from midgap toward the Si conduction band. The peak at ~300 K in the DLTS spectrum in Fig. 3 corresponds to the shoulder in the C-V distribution.

A Characteristic Discrete Interface Level in a P-Type MOS Structure

Certain processing and testing procedures introduce discrete levels at the $Si-SiO_2$ interface. In clean, unimplanted MOS structures, discrete interface levels appear when the device is electrically biased at elevated temperatures (9). In particular, bias-temperature treatments produce a discrete level of high density at an energy between 0.35 and 0.4 eV above the valence-band maximum (9,10). We have observed a similar level in *unannealed* specimens of oxidized Si, *without* the use of bias-temperature treatments. This peak is located at E_V+0.35 (±0.01) eV and is readily removed by a low-temperature anneal (450 C).

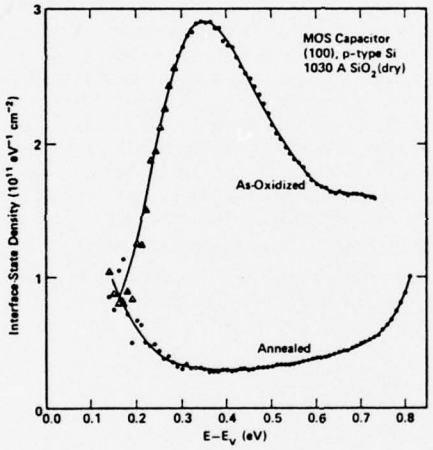

Fig. 5. Interface-state distributions in as-oxidized and annealed p-type MOS capacitors, as measured by the quasi-static C-V technique.

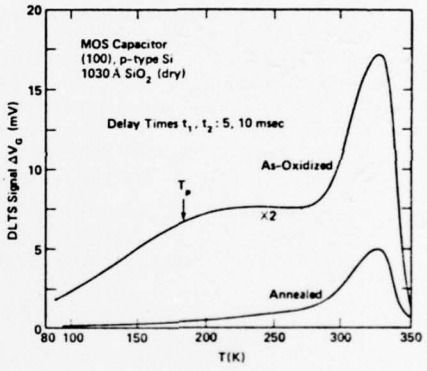

Fig. 6. CC-DLTS spectra for as-oxidized and annealed p-type MOS capacitors.

The interface-state distributions for both as-oxidized and annealed specimens, measured by the quasi-static C-V technique, are shown in Fig. 5. As-oxidized samples display a broad, prominent peak centered at E_V+0.35 eV. The full width of the peak at half maximum is approximately 0.3 eV, and the peak density is 2.9×10^{11} eV^{-1} cm^{-2}. In the annealed samples this peak is completely absent; remaining is the generally-observed continuum of interface states, with a minimum density near midgap of 3×10^{10} eV^{-1} cm^{-2}.

DLTS spectra for both as-oxidized and annealed specimens are shown in Fig. 6. Both spectra were recorded with the same delay times and fixed depletion capacitance. The only difference in preparation between the two specimens is a low-temperature, post-metallization anneal (450 C, 60 min, H_2/N_2). Both spectra display a large peak at ~330 K which we ascribe to combined majority and minority carrier processes. These peaks are not the DLTS signatures of the discrete level shown in Fig. 5, although the relative magnitudes of the peaks do reflect the

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difference in the interface-state densities of the two specimens. The broad interface-state peak is responsible for the large emission signal in the as-oxidized specimen at temperatures below ~300 K. Although the peak is associated with a discrete level, it must be treated as a continuous trap distribution in the DLTS analysis since its density varies slowly with energy on a scale of kT. In annealed specimens the hole emission signal is strongly attenuated due to the reduced density of the discrete interface level. The interface-state distribution (*vs* temperature) obtained from the emission spectrum for the as-oxidized specimen displays a peak at a temperature T_p; this temperature is noted on the emission spectrum in Fig. 6. The interface-state density at the peak is 2.5×10^{11} eV^{-1} cm^{-2}, in close agreement with the peak density as measured by the quasi-static C-V technique (Fig. 5). From the peak temperature the capture cross-section for holes is found to be approximately 7×10^{-15} cm^2.

DLTS emission spectra for an annealed specimen are shown in Fig. 7. The spectra were recorded with enhanced sensitivity and with two different pairs of delay times. Two features are clearly evident. First, the emission signal monotonically increases with temperature over the entire range, in marked contrast with results for electron emission from interface states in n-type MOS structures (Fig. 3). In MOS capacitors on p-type Si, the signal is due to hole emission from interface states near the Si valence band. However, the interface-state distribution which is obtained from the DLTS spectrum indicates that the density of states in the continuum increases with energy from the valence band toward midgap, in disagreement with results from quasi-static C-V measurements on annealed specimens (Fig. 5). This feature has been previously noted (11); it was suggested that the DLTS signal arises from hole emission from interface states in a conduction-band tail which extends into the lower half of the Si bandgap. The second feature pertains specifically to the discrete interface level. Even in the annealed specimens, a residual peak, superimposed on the continuum, is detectable in the DLTS emission spectra (Fig. 7). From the shift of the peak with delay time, the peak energy is found to be E_v+.34(+.15,-.08) eV. Further, we estimate that the density of discrete levels at the peak is ~6×10^8 eV^{-1} cm^{-2}. As is evident in Fig. 5, a residual peak with this density is not detectable by the quasi-static C-V technique. The minimum detectable interface-state density in the DLTS measurements presented in Fig. 7 is ~2×10^8 eV^{-1} cm^{-2}.

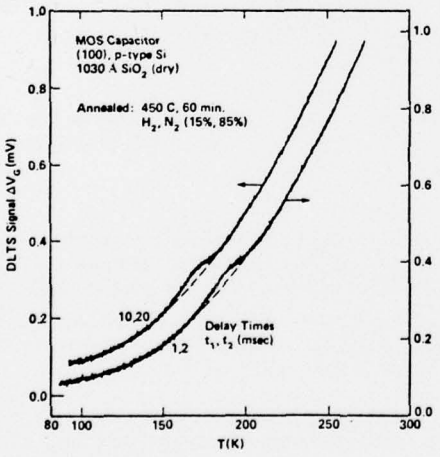

Fig. 7. CC-DLTS emission spectra, recorded on an expanded scale, for an annealed p-type MOS capacitor

We propose that the discrete interface level at E_v+0.35 eV is due to a characteristic defect at the Si-SiO_2 interface. Its presence in clean, as-prepared MOS structures and the effect of a

low-temperature anneal, as demonstrated here, as well as its response to bias-temperature treatment (9,10) support this identification. Additional information further suggests that this defect is a Si dangling bond. Recent theoretical studies by Laughlin, Joannopoulos, and Chadi (12) reveal that Si dangling bonds at the $Si-SiO_2$ interface introduce a discrete interface level in the lower half of the Si bandgap near midgap, while neither oxygen dangling bonds nor strained Si-O bonds (i.e., bond angle distortions) contribute discrete levels in the bandgap. Since the thermal oxidation process favors an excess of Si in the $Si-SiO_2$ transition layer (13), which has been experimentally observed (14), Si dangling bonds may be considered a characteristic defect of the thermally oxidized surface. Even an atomically abrupt interface may possess a surface density of dangling bonds due to the $Si-SiO_2$ lattice mismatch (15). Further, with electron spin resonance Si dangling bonds have been identified at the $Si-SiO_2$ interface in freshly oxidized wafers and in processed wafers after bias-temperature treatment (16). In the present study the surface density of discrete levels in as-oxidized specimens (Fig. 5) would correspond to $\sim 10^{11}$ cm^{-2} Si dangling bonds, or of the order of one dangling bond for every 10^4 surface atoms. These dangling bonds would be readily hydrogenated by a low-temperature anneal in a hydrogen-rich ambient; on a free Si surface this removes the discrete level from the Si bandgap (17). The surface density of discrete interface levels in the annealed specimens (Fig. 7) is estimated to be $<5 \times 10^7$ cm^{-2}.

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Appendix A 2

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Transient Capacitance Measurements of Interface States on the Intentionally Contaminated Si–SiO_2 Interface

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Abstract. The constant capacitance transient capacitance technique (CC–DLTS) was applied to analyse the effect of impurities on MOS interface states. The elements Cs, Pb, Xe were ion implanted prior to oxidation. Sodium was implanted directly into SiO_2 and drifted to the interface. The alkali ions cause a steep increase in the density of interface states near the conduction band edge. The other elements studied show little effect on the interface properties. The capture cross-section for electrons decreases strongly near the conduction band.

PACS: 73.40

We have studied the effect of impurities on density and properties of MOS interface states. The influence of impurities in semiconductor insulator interfaces is not well understood, but it is expected that impurities have a strong effect since in recent years the density of states in MOS interfaces could be markedly reduced by improvement of cleanliness standards.

Ion implantation was used to introduce the impurity into the MOS interface for the study using the same technique, as previously published [1]. Ion implantation makes it possible to select special types of elements with high purity and to incorporate these elements directly into the interface in a controlled manner by choosing the appropriate energy. In order to avoid radiation damage in the interface we implant the impurity under consideration before oxidation into the bare silicon surface with a well controlled dose of the order 10^{12}–$10^{14}\,cm^{-2}$. The silicon wafer is then oxidised thermally with standard technology to obtain approximately 1000 Å thin SiO_2 layers. It is known that during formation of the oxide from the implanted Si-layer, the impurity redistributes itself to establish an equilibrium with the interface. As indicated in the schematic drawing of Fig. 1, most impurities are gettered in the interface region. A concentration profile with peaks in the interface and at the surface is generally observed by secondary ion mass spectroscopy SIMS [1, 2].

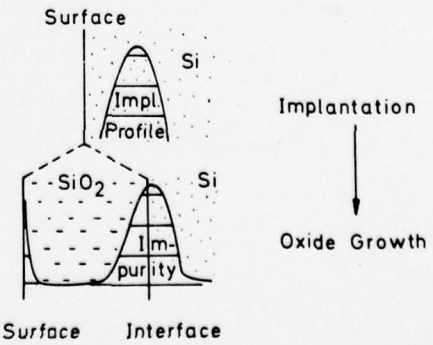

Fig. 1. Schematic drawing of the procedure to introduce an implanted impurity into the MOS interface

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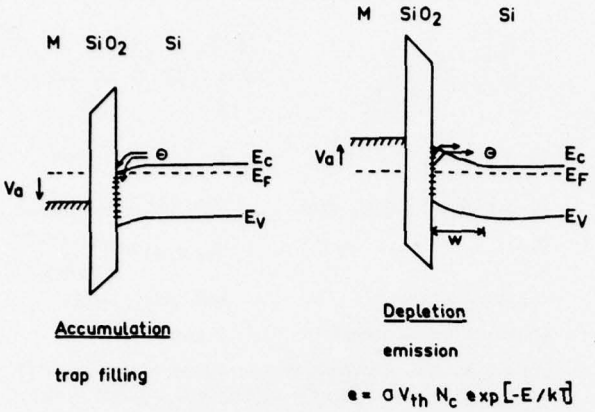

Fig. 2. Schematic drawing to illustrate the measurement principle of DLTS applied to an MOS structure

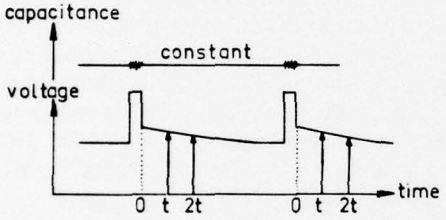

Fig. 3. Schematic drawing to explain the correlation procedure in the "Constant Capacitance Transient Spectroscopy" CC-DLTS

The new feature of the present paper is the application of the transient capacitance measurement technique DLTS to analyse the dynamic properties of MOS interface states in presence of impurities. The DLTS technique has been mainly used to measure bulk defects [3–5]. It has also been successfully applied to study MOS interface states in the case of state-of-the-art clean MOS interfaces [6–8]. The technique features high sensitivity and complements the conventional techniques, e.g. the quasistatic and conductance technique for measuring interface state properties, in that it is not affected by surface potential fluctuations which arise from the random spatial distribution of fixed positive charge in the oxide. The technique is therefore especially advantageous for measuring interface states at energies close to the band edge.

Details on the measurement technique and the evaluation analysis are given elsewhere [9]. Here we only explain the main details of the measurement procedure and evaluation. New results are shown for the interface state density distribution in presence of the alkali elements Cs and Na in the interface region. These elements are known to have a critical effect on the fixed interface charge. We could show that these impurities also have an effect on the fast interface state density close to the band edges. This region is not accessable to the conventional measurement techniques. Results for other contaminants, e.g. Pb and Xe, which mainly cause radiation damage are also shown. The experimental results are discussed in the light of theoretical models for MOS interface states.

DLTS-Measurement on MOS Structures

The measurement principle is explained in Figs. 2 and 3. During a 20 µs pulse the MOS capacitor is biased into accumulation to fill all interface traps with majority charge carriers, e.g. in our case electrons. During the pulse interval the bias voltage is adjusted so that the Fermi level in equilibrium is located in a midgap position. The change of the interface charge is monitored by measurement of the MOS capacitance. As indicated in Fig. 3, we use a feedback from the capacitance bridge to the bias power supply to maintain a constant capacitance. The relaxation of the interface charge is then monitored by the bias voltage. The change of the gate voltage required to maintain a constant capacitance appears only across the oxide layer. The interface charge change per unit area $\Delta Q_{ss}(t) = q\Delta N_{ss}$ which is proportional to the interface state density therefore is simply related to the observed gate voltage signal $\Delta V(t)$ by

$$\Delta V(t) = A\Delta Q_{ss}(t)/C_{0x}, \tag{1}$$

where C_{0x} is the oxide capacitance and A the capacitor metal gate area. It is assumed that during the pulse interval interface states emit the trapped charge by thermal emission [$\sim\exp(-t/\tau_e)$] with time constant

$$1/\tau_e = \sigma_n v_{th} N_C \exp(-E/kT), \tag{2}$$

where σ_n is the capture cross-section and v_{th} the thermal velocity of electrons, N_C the effective density of states in the conduction band, and E the energy depth of the interface state below the conduction band edge. As indicated in Fig. 3, the gate voltage V_G is sampled at two different delay times t_1 and $t_2 = 2t_1$ and the difference signal

$$\Delta V_G = V_G(t_1) - V_G(t_2) \tag{3}$$

is formed in the DLTS measurement. For electron emission from a continuous distribution of interface traps, we obtain for the DLTS signal ΔV_G from (1)–(3)

$$\Delta V_G = A/C_{0x} \int qN_{ss}(E) \cdot [\exp(-t_1/\tau_e) - \exp(-t_2/\tau_e)]\,dE. \tag{4}$$

For a constant or slowly varying capture cross-section and interface state density the integrand is sharply peaked at energy E_0 [6]

$$E_0 = kT \ln(\sigma_n v_{th} N_C t_1 / \ln 2) \tag{5}$$

and

$$\Delta V_G = kTA \ln 2 \, N_{ss}(E_0)/C_{0x}. \tag{6}$$

Thus, the emission signal divided by temperature is directly proportional to the interface state density at energy E_0. The energy interval over which interface traps contribute to the DLTS signal is $\Delta E = kT \ln 2$. Both, the width of the interval ΔE, and its location in energy E_0 increase linearly with temperature. The energy resolution is therefore greatest at low temperatures where the sampled interval is closest to the conduction band and where the interface state density and capture cross-section is expected to vary most rapidly. The larger energy intervals obtained at high temperatures provide enhanced sensitivity for detecting low densities of interface states which are typically found near midgap.

The capture cross-section is obtained from two or more temperature scans taken at different delay time constants t_1 and t_1' by using (5) and noting that the same density of states at a given E_0 is measured at two different temperatures T and T'. The analytical expression for the capture cross-section is

$$\sigma_n = (\ln 2 / t_1 V_{th} N_C)(t_1'/t_1)^{T'/(T-T')} \tag{7}$$

Equations (5) and (7) are used to analyse the experiment. A comparison of the DLTS-technique with the conventional conductance technique for the measurement of interface state densities is given in Fig. 4. In the conductance technique, the position of the Fermi level is used to probe the energy position of deep levels at the surface. Only those states which are within a few kT in the vicinity of the Fermi level contribute to the measured conductance signal.

The transition of charge carriers which is sensed in the conductance technique is marked by CT in Fig. 4a. Bulk levels are only measured at the cross-over with the Fermi level. This cross-over occurs in a narrow region because of the band bending. The conductance technique is therefore insensitive to bulk states.

The effect of potential fluctuations in the surface is indicated in Fig. 4b. In the conductance technique, the energy resolution is smeared out by the potential fluctuation. In the DLTS-technique, the emission time constant is measured. This time constant is only dependent on the local energy depth under the band edge for pure thermal emission and is independent of the position of the Fermi level. The total number of states in the space charge layer is measured independent of band bending and potential fluctuations. DLTS therefore is very sensitive also to bulk states. However the spectrum of the states is measured as a function of the emission time constant rather than energy. The energy dependence of the number of states and the capture cross-section can only be obtained by a deconvolution of the measured data. The comparison of the various properties is listed in Fig. 4.

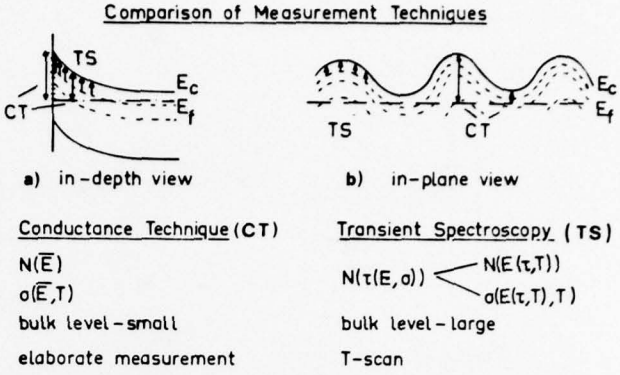

Fig. 4. Comparison of the conductance technique and CC-DLTS technique in the measurement of bulk and interface states in MOS structures

Experiment

The silicon samples (approx. 1 Ohm cm n-type epitaxial material on low resistivity substrate) were implanted before oxidation. The implantation was performed at room temperature at an angle of about 7° with respect to a low-index crystal orientation. The implantation energy was chosen to obtain a projected range of approx. 600 Å according to the LSS table computed by Johnson and Gibbons [10]. The SiO_2 film was grown under standard dry oxidation conditions at 1050 °C to a thickness of 600 to 1200 Å. For the elements under investigation Cs, Pb, Xe it was known from our earlier work where we have performed secondary ion mass spectroscopy SIMS that these imporities pile up at the interface during oxide growth.

For the case of sodium a shallow implantation into the oxide was performed to contaminate the MOS structure intentionally. Sodium can be drifted to and away from the interface at room temperature by applying a dc bias field. A flat band voltage shift from −6 V to −34 V was observed after 30 min drift with 10 V dc bias voltage.

The DLTS measurement system has been described elsewhere [4, 8, 9]. The only new feature in CC-DLTS is a feedback loop from the capacitance bridge to the

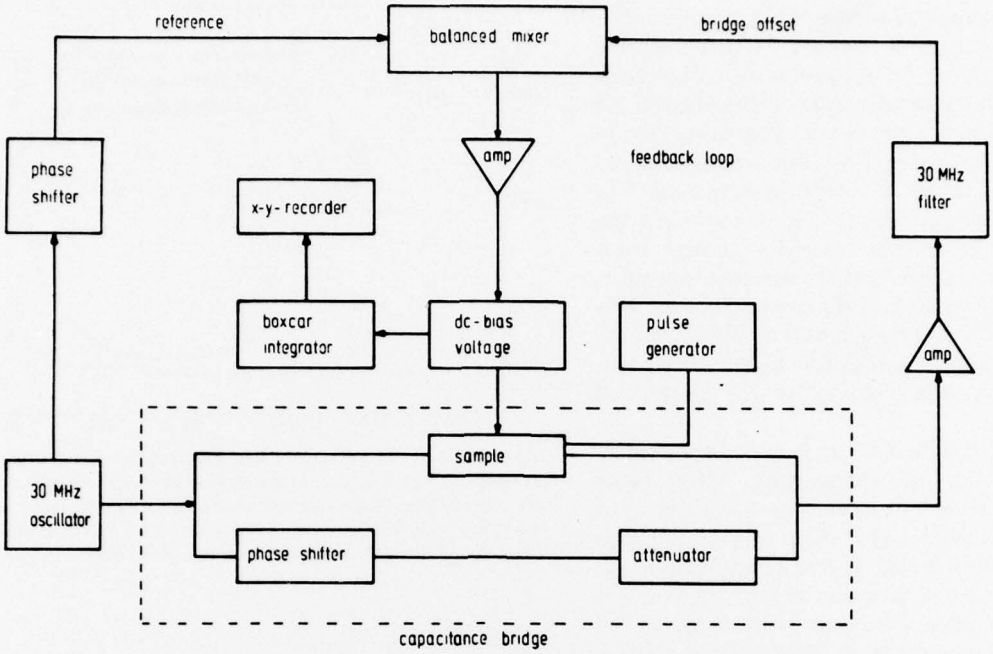

Fig. 5. Block diagram of the apparatus for the CC-DLTS measurement system which is used to analyse interface states

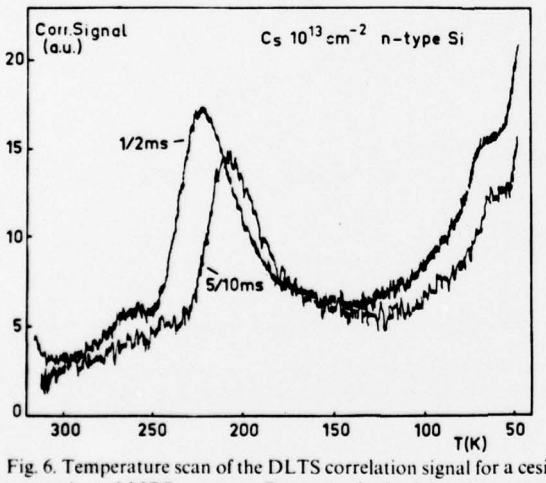

Fig. 6. Temperature scan of the DLTS correlation signal for a cesium contaminated MOS structure. Parameter is the delay time constant used in the DLTS technique

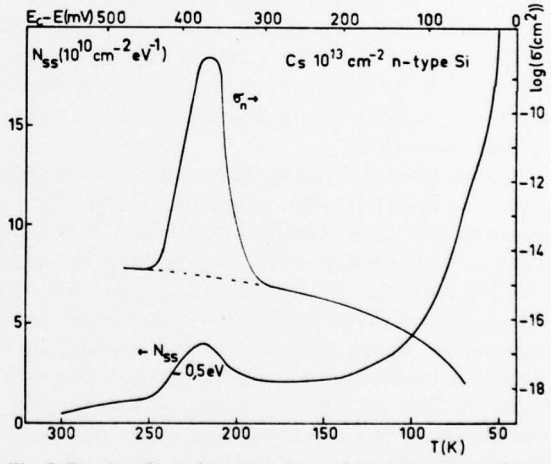

Fig. 7. Density of interface states N_{ss} and capture cross-section σ_n as evaluated from the measurement in Fig. 6 for a cesium contaminated MOS structure

dc voltage supply to maintain a constant capacitance of the MOS structure. The block diagram of the measurement system is shown in Fig. 5.

Results

A typical temperature scan of the DLTS signal for a Cs contaminated sample is shown in Fig. 6. Two temperature scans of the DLTS correlation signal taken with two pairs of sampling delay times 1/2 ms (i.e. 1 and 2 ms) and 5/10 ms were recorded. The cesium dose implanted into the bare silicon before oxidation was 10^{13} cm^{-2}. The shape of the observed signal vs. temperature is quite different to the shape observed in state-of-the-art clean samples [6, 9]. A steep increase of the signal is observed at low temperatures. A strong peak is superimposed at approx. 220 K.

In Fig. 7 the experimental curves of Fig. 6 are evaluated to obtain the density of interface states N_{ss} and the capture cross-section σ_n by using (6) and (7). The values N_{ss} and σ_n are plotted as a function of temperature. An approximate energy scale is obtained by using (5) and the continuous curve for σ_n. This scale is marked at the top of Fig. 7. It should be noted, however, that the peak at 220 K which also appears in the capture cross-section does not fit into the continuous energy scale. The energy position of the peak is evaluated to approx. 0.5 eV because of its high capture cross-section. This peak in the density of interface state at 220 K and the peak in the capture cross-section indicate that this state differs from the continuous background of states.

The background density of states is rather low around $10^{10}\,cm^{-2}\,eV^{-1}$ at high temperatures where states near midgap are observed and increases very steeply at low temperatures where states close to the band edge are observed. The increase at low temperatures and shallow energy depths is much steeper than it was observed in state-of-the-art clean MOS samples. The variation of the capture cross-section for the background of interface states (excluding the peak) is comparable to the observation in clean samples. In the midgap region the capture cross-section is of the order $10^{-15}\,cm^2$. At shallow energy depths $E_0 \sim 0.2$ eV the value of the capture cross-section drops to low values of the order of $10^{-18}\,cm^2$. The capture cross-section seems not to be affected by the cesium contamination. Only the density of states near the band edge is strongly increased.

The same general behavior of the number of interface states is observed after sodium contamination by implantation of a small dose $10^{13}\,cm^{-2}$ into the surface. The interface state density observed before drift (A) and after drift (B) of sodium ions away from the interface is shown in Fig. 8. The amount of positive sodium ion charge shifted from the interface to the surface is visible in the flat band voltage shift of the order of 28 V. A strong increase of the number of interface states is again observed when a large number of positive sodium ions is present at the interface. The background of states in the sample was quite high of the order $3 \times 10^{11}\,cm^{-2}\,eV^{-1}$. Because of the mobility of sodium ions in SiO_2 the density of states could not be measured at high temperatures (greater 150 K) under the bias conditions in the measurement. The observed result for sodium, however, is similar to the case of cesium which is stable up to high temperatures.

A result of lead implantation prior to oxidation is shown in Fig. 9. The density of states and the capture cross-section are shown as a function of the measurement temperature. Note the change in the scale for the

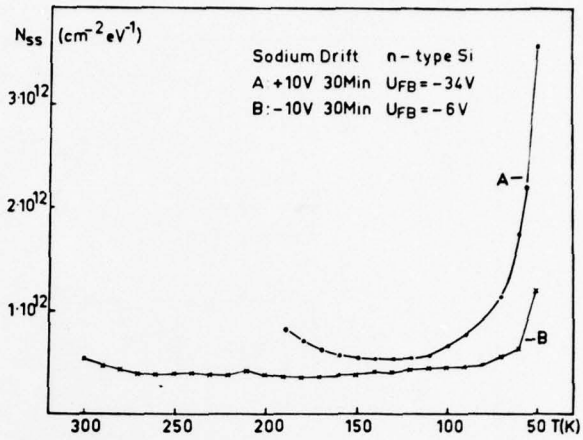

Fig. 8. Density of interface states obtained by the CC-DLTS measurement for a sodium contaminated MOS structure. Sodium ions were drifted to the interface (curve A) and to the metal gate (curve B) by a dc bias stress as shown in the insert. Values of the flat band voltage for each case are also shown in the insert

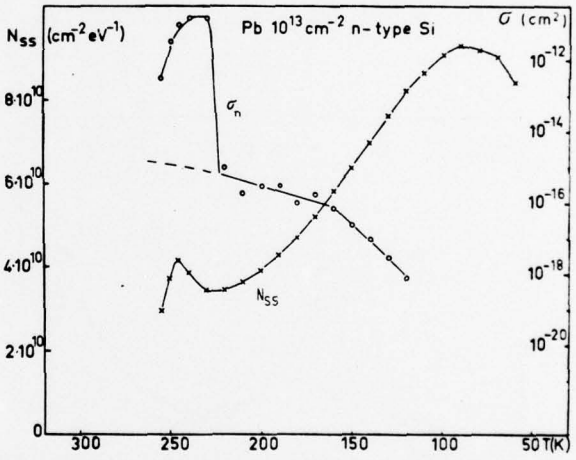

Fig. 9. Density of interface states N_{ss} and capture cross-section σ_n for a MOS structure implanted with lead prior to oxidation

N_{ss} value in comparison to cesium in Fig. 7! The increase in the number of states at low temperatures is much weaker than for cesium and comparable to the behavior in clean samples. A peak is observed at 240 K which appears in the density of states and the capture cross-section. The background of the capture cross-section for the continuum of interface states shows the same general behavior as was observed for cesium.

In order to study the effect of radiation damage we have implanted a noble gas ion (Xe) prior to oxidation. The sample preparation was not changed. The result is

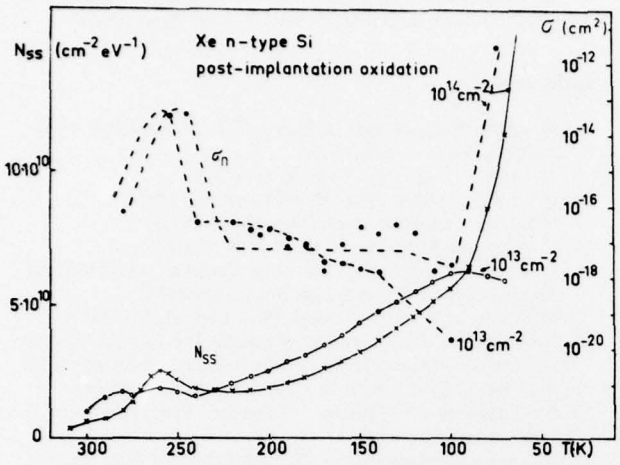

Fig. 10. Density of interface states N_{ss} and capture cross-section σ_n for a MOS structure implanted with Xe-ions prior to oxidation. The implanted doses are shown in the insert

shown in Fig. 10 for two implanted doses of $10^{13}\,cm^{-2}$ and $10^{14}\,cm^{-2}$. The observed result for the dose of $10^{13}\,cm^{-2}$ is similar to the behavior of lead. Peaks are observed in the density of states and capture cross-section around 250 K. The density of states shows a weak increase at low temperatures where states close to the conduction band edge are observed. The capture cross-section decreases to low values. For a high implanted dose $10^{14}\,cm^{-2}$, the density near midgap observed at high temperatures remains low, however, at shallow energies the density of interface states increases very steeply. This behavior seems similar to the behavior of cesium, however, the capture cross-section also shows a steep increase for the high Xe-dose. It is therefore assumed that a new type of level appears at high implanted doses.

Conclusions

The observed results demonstrate that CC-DLTS is very useful to study MOS interface states. The capture cross-section and the number of states are directly observed in a temperature scan of the DLTS correlation signal. The temperature variation can be interpreted as an energy scale. It has been shown earlier [6] that the variation of the capture cross-section is energy dependent. CC-DLTS is especially useful to study the energy region in the vicinity of the band edge. This region was not accessible by other techniques which use the Fermi level to probe the energy position because potential fluctuations smeared out the energy resolution.

Based on the presented CC-DLTS results in comparison with earlier measurements using the conductance technique [11] we arrive at the following conclusions on the influence of impurities in the MOS interface on *n*-type silicon:

- alkali ions increase the number of fast interface states in the energy region close to the conduction band edge
- the density of interface states in the midgap region is very little affected by impurities
- lead ions do not seriously affect the number of interface states up to doses of the order of $10^{13}\,cm^{-2}$ implanted prior to oxidation
- ion implantation prior to oxidation causes a damage level near midgap which appears as a peak in the CC-DLTS temperature scan, independent of the implanted type of ion. Tests with the conductance technique did not show this level. The peak is probably a bulk Si level in the vicinity of the interface because only the CC-DLTS technique is sensitive to bulk levels
- the capture cross-section is energy dependent [6]. The order of magnitude near midgap is $10^{-15}\,cm^2$. The value indicates a neutral trapping center. Near the band edge, the value of the capture cross-section drops to very low values of less than $10^{-18}\,cm^2$
- the emission rate from interface traps is purely temperature activated. This conclusion is a consequence of the observed quantitative agreement with results of the conductance technique
- tunneling to trap centers in the oxide can be excluded because tunneling would be temperature independent. It is therefore not visible in a temperature scan. Tunneling together with a temperature activation would lead to a discrepency with results of the conductance technique because in the evaluation of the CC-DLTS result only temperature activation has been taken into account. However, CC-DLTS and the conductance measurements are in accordance within the measurement error
- except in the discrete peaks observed around 240 K, all the interface states are of the same type. The observed variation in density and capture cross-section can be interpreted as a gradual property variation of the same type of state as a function of its energy position. Especially, a transition from one type of state to another can be excluded because two different capture cross-sections are never observed for states at the same energy position. A step in the capture cross-section would be observed if a transition from one type of state to a new type at a given energy is present
- the charge model [12] for the interpretation of interface states seems very unlikely. In the charge model, the free electron is bound to the positive charge center in the oxide similarly as to a donor center in bulk crystals. The charge model cannot account for the

capture cross-section near the band edge. For an attractive center, the capture cross-section for weakly bound electrons is expected to increase rather than to drop to low values as it is observed for bulk donor levels.

Theoretical models which are known at present cannot explain all the observed effects on interface states in MOS structures on *n*-type silicon. Since the number of states is related to the oxide charge, the charge center in the oxide and its coupling to the lattice (multiphonon emission) may dominate the trapping of electrons at the interface. Further experimental details are necessary to develop a theoretical model on firm grounds.

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