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FINAL REPORT AND OPERATION MANUAL FOR KA-BAND TRANSMITTER, KA-B--ETC(U)
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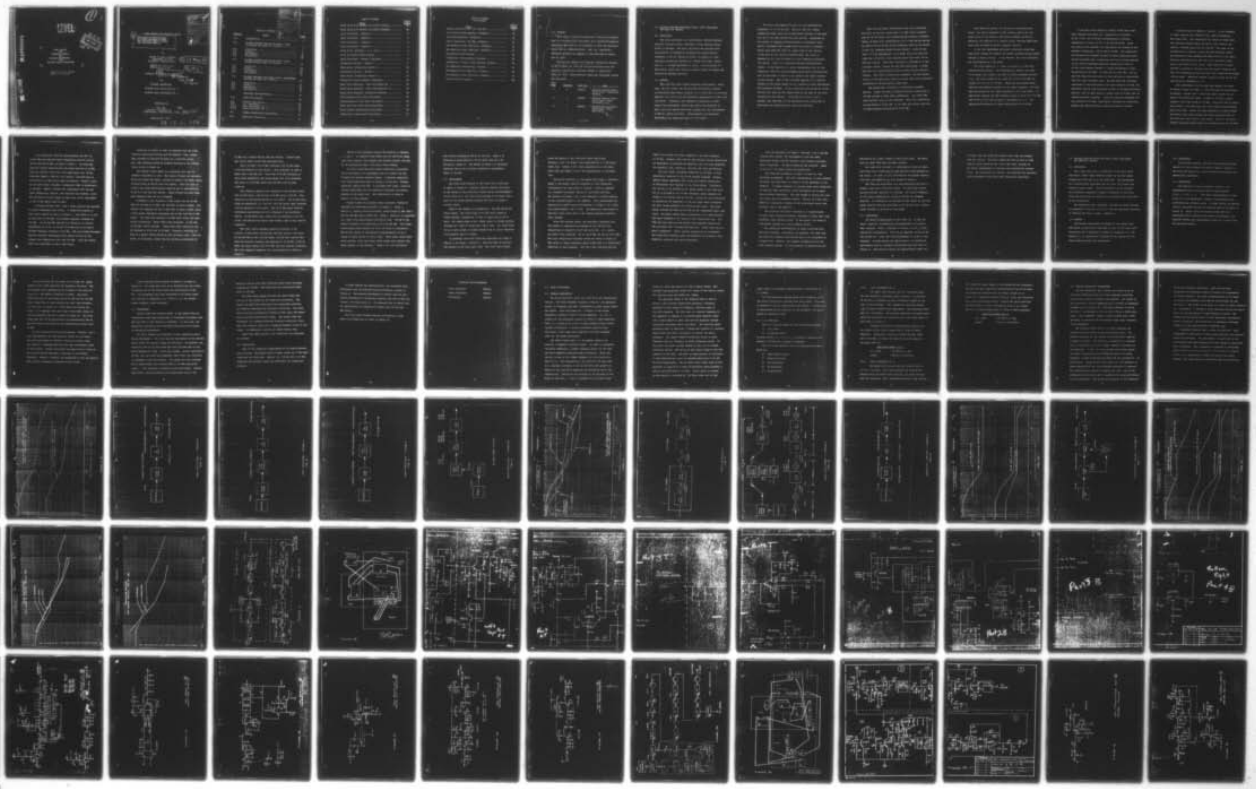

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FINAL REPORT
AND
OPERATION MANUAL
FOR
KA-BAND TRANSMITTER
AND
KA-BAND LOCAL OSCILLATORS

APPROVED FOR PUBLIC RELEASE
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(6) FINAL REPORT AND OPERATION MANUAL

**Final Report and Operation Manual
for KA-Band Transmitter, KA-Band
Local Oscillator Number 1, KA-Band
Local Oscillator Number 2,**

TO

OFFICE OF NAVAL RESEARCH
DEPARTMENT OF NAVY
ARLINGTON, VIRGINIA 22217

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FOR

KA-BAND TRANSMITTER

KA-BAND LOCAL OSCILLATOR NO. 1

KA-BAND LOCAL OSCILLATOR NO. 2

SUBMITTED BY:

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S/C 391195

February 28, 1975

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1.0 FORWARD

This report covers the objectives, history and development of a Ka-Band Local Oscillator and a Ka-Band Transmitter Exciter, as described in the Statement of Work and Specifications, RFP No. N0014-TS-R-0017. RDL, Inc. submitted a technical proposal in response to the above RFP on December 15, 1972.

Contract No. N00014-73-C-0394 was subsequently awarded to RDL on March 19, 1973 and the specifications were subsequently revised per Attachment Number 1, Dated September 14, 1973. Three hardware items were developed, tested and delivered:

Line Item	Quantity	Model No.	Item
1	1	M06K161	Ka-Band Varactor Multiplier Chain, Transmitter Exciter
2	1	M01K161	Ka-Band Varactor Multiplier Chain, Local Oscillator, and
3	1	M01K162	Ka-Band Varactor Multiplier Chain, Local Oscillator

2.0 Ka-BAND VARACTOR MULTIPLIER CHAIN, LOCAL OSCILLATOR RDL MODEL NO. M01K161

2.1 OBJECTIVES

The local oscillator is a solid-state, state-of-the-art, varactor multiplier chain, providing a high spectral purity output in Ka-Band. The local oscillator was designed with the objective of meeting or exceeding the specifications contained in RFP No. N00014-73-R-9917, Paragraph 4.2 (subsequently revised per Contract No. N00014-73-C-0394, Attachment No. 1, revised September 14, 1973). The provisions of MIL-E-16400 (Navy) were used as a general guide for design and fabrication wherever possible.

2.2 HISTORY

This unit has three highly stringent requirements: small size, low F.M. noise, and low spurious and harmonic outputs. In discussing these three criteria, it is shown that no practical approach will fully meet the electrical requirements of the local oscillator. Therefore, four methods of developing a clean signal were considered, showing the merits and downfalls of each, and which method would most closely meet the requirements of RFP No. N00014-73-R-0017. These methods and subsequent development are summarized again in this report.

The noise requirements for the L.O. are described by paragraph 4.2.1.5 of the RFP. The A.M. and F.M. single sideband-to-noise ratio are of particular interest in the band 20.0 Hz to 10.0 MHz removed from the carrier. Regardless of the scheme of frequency multiplication or processing, some general statements may be made about the effect of multiplication upon both A.M. and F.M. noise close to the carrier. In the case of F.M. single sideband noise, the noise is degraded by 20 x log (N) where N is the frequency multiplication factor. This is a limitation derived from modulation theory. In the case of A.M. noise, disregarding A.M. to P.M. conversion, the A.M. single sideband noise after multiplication will be less than or equal to the noise at the input relative to the carrier. This is due to either specific A.M. limiting schemes or the normal degree of A.M. limiting in most multipliers and frequency dividers. If the multiplier were perfectly linear, and the A.M. noise at the output would be the same as the input (relative to the carrier). Since the A.M. noise is not a problem, the remainder of this discussion will concentrate on techniques for minimizing F.M. noise and spurious.

There are two basic limitations which were considered. The first is the F.M. noise from a 5.0 MHz atomic standard, such as the HP 5061A, the intended system frequency standard. Figure 1A shows this characteristic at 5.0 MHz and multiplied by 7488 to the 37.44 GHz output frequency (this is the center of the L.O. frequency bands finally chosen). Since 20 log 7488 = 77.5 db degradation, it is shown that curve does not cross the -60 dB F.M. noise specification line until 700 Hz from the carrier. When this reference is followed by a high Q crystal filter, (Figure 1A) and then multiplied, it shows that the F.M. specification is met at about 150 Hz from the carrier. This curve, showing the reference, and the crystal filter is the best noise close to carrier that can be realized, regardless of the processing system used.

The second basic limitation is obtaining frequency agility. Figure 1B shows an HP5061A reference multiplied to 117 MHz through a Fluke 6160A synthesizer. The 6160A adds some residual noise to the reference. When this combination is multiplied to 37.44 GHz, it is worse than having only the 5.0 MHz reference multiplied to 37.44 GHz.

From these two points, the following conclusions were drawn: the atomic standard is the limiting factor for F.M. noise close to the carrier, the atomic standard can be improved by the addition of a crystal filter, and some additional noise must be added to obtain frequency agility.

In the four approaches presented, comparison noise data were shown (Figure 6) assuming the atomic standard was processed through a crystal filter. In all methods, the final multiplier was consolidated as a X80 block.

The first Method No. 1, shown in Figure 2, is the most straightforward method. The advantages of Method 1 are that it is cheap, very simple, and that it offers frequency agility (i.e., the Fluke 6160A may be tuned 116.75 to 117.25 MHz for outputs of 37.36 to 37.52 GHz). There are two problem areas: spurious and harmonics related to the imput frequency, and other spurious present at the input generated by the Fluke 6160A. Of particular interest are the frequency bands of 36.80 to 37.00 GHz and 37.90 to 38.10 GHz as shown in paragraph 4.2.1.4. The spurious and harmonics in these bands should be <-100 dB.

It was known from technical inquiry of NRL that there were actually only three L.O. frequencies of interest: 37.38, 37.44, and 37.50 GHz corresponding to receiver frequencies of 36.84, 36.90, 37.98 and 38.08 GHz. After the contract was awarded, the requirement was changed to two discrete frequencies: 36.06 and 36.12 GHz. For simplicity, we discussed the problems related to these frequencies only. Various proposed input frequencies and their related spurious in the -100 db forbidden bands are summarized in Table 1. In the first example (Method 1), these correspond to input frequencies of 116.8125, 117.0000 and 117.1875 GHz. We can see that there are from three to four spurious in these bands from the input frequency only. Through judicious filtering techniques in the multipliers, the spurs would be $\leq$-60 dB, but obtaining -100 dB from microwave filters is extremely difficult. However, none of these spurs is closer than 45.00 MHz from the related receiver frequency. Since the receiver bandwidth will be a maximum of $\pm$1 MHz, these spurs, although not technically meeting the specifications, would not present a problem.

A greater fault of Method 1, however, is the treatment of other spurious not related to the input generated by the Fluke 6160A. The frequencies and levels of these spurs are virtually unpredictable and may be very close to the carrier, although they would be <-80 db. The input to the X4 multiplier of Figure 2 cannot be made extremely narrow and therefore it was assumed that these close in F.M. spurs would be enhanced by 20 x log 320 = 50.1 dB (worst case), just as the close in F.M. noise. There would be an unpredictable multitude of spurious near the output frequency and near the abovementioned spurious that fall inside the forbidden -100 dB bands. Therefore, Method 1 would not meet any of the provisions of paragraph 4.2.1.4.

Some improvement could be made upon Method 1 by going to Method 2 shown in Figure 3. This utilizes the same scheme as Method 1, except that a "clean-up" phase locked VCXO is used at the multiplier input. A VCXO at 117 MHz is phase locked to the Fluke 6160A at 117 MHz. Since the VCXO is itself very stable, a low loop gain and a very narrow loop bandwidth may be utilized. Within the loop bandwidth of a phase locked oscillator, the output follows the noise characteristics of the reference +20 x log N to the output. However, the phase locked oscillator would follow the characteristics of the VCXO

outside the loop bandwidth. It was estimated that the 117 MHz VCXO would have greater spectral purity than the reference 200 Hz and greater from the carrier. Closer than 200 Hz from the carrier, the 20 x log N rule applies, and the spectrum would look like the reference multiplied to the output frequency. Three to four spurs of the input still occur in the -100 dB bands, but as previously noted, are never closer than 45.00 MHz from the receive frequency. The only advantage, therefore, of Method 2 is that it eliminates a lot of "clutter" from about 500 Hz and out from the carrier. Spurious occurring from the 6160A still remain from 500 Hz into the carrier. Method 2 is more costly than Method 1 because frequency agility of the source has been lost. A different VCXO must be employed for each desired output frequency.

Some of the advantages of Method 1 and 2 could be obtained by Method 3, as shown in Figure 4. This employs a 468 MHz VCO phase-locked to the Fluke 616A synthesizer. The advantage of this scheme is that it offers complete frequency mobility as with Method 1 and it attenuates the 117 MHz spurious at the output. As listed in Table 1, the number of possible spurs in the forbidden -100 dB bands has been reduced to only 1 or 2, depending on the L.O. frequency. These spurious would never be closer than 72.00 MHz from the receive frequency which is

better than the 45.00 MHz obtained in the other schemes. However, the loop bandwidth required for this VCO is much greater than for the VCXO of Figure 3 and would provide very little, if any, improvement in the noise and spurs generated by the Fluke 6160A in the region 20 Hz to 1 MHz from the carrier.

Through technical discussion with Fluke, it was learned that in order to predict the spurs from the Fluke 6160A, the exact frequency must be pinpointed. It had become obvious that the selection of the input frequency, and thus the multiplication scheme, is critical. It is known that spurs generated by the last digit that is dialed on the Fluke 6160A (i.e.,if the 1 MHz position is used, 1 MHz spurs will occur around the output frequency. Likewise, if the 1 KHz position is required, 1 KHz spurs will occur around the output frequency).

In the three methods proposed thus far, the input frequencies would be 116.81250, 117.00000 and 117.18750 MHz. The last digit required is in the 100 Hz digit. Therefore, 100 Hz spurs would occur surrounding the carrier, except in the 117.00000 MHz case which would be 1 MHz. The three schemes proposed thur far would provide virtually no reduction of the 100 Hz, 200 Hz, etc. spurious. It became evident that 117 MHz was not the best choice for the input frequency to the multiplier.

A X3 multiplier could be used preceding the X80, in which case the required input frequencies would be 155.75, 156.00 and 156.25 MHz, as shown in Table 1. We could see that the closest spurious from the 6160A would be at 10 KHz from the carrier, which has a big improvement over 100 Hz. Examining Method 1 used as a X3, however, revealed that no correction of 10 KHz spurs could be obtained. Method 2 could not be used either, because a fundamental VCXO is unrealistic at 156 MHz. Method 3 showed some improvement with the new input frequencies, however, the required loop bandwith, using the VCO had to be wide enough so that very little improvement in the 10 KHz spurs would be made.

It became obvious, then, that a fresh approach was required to obtain acceptable spur levels. A simplified diagram of this fourth method is shown in Figure 5. From Table 1, it can be seen that at 468 MHz, the minimum frequency increment is 250 KHz. If the 468 MHz applied to a divide by 15 circuit, frequencies of 31.15, 31.70 and 31.25 MHz will occur with a minimum frequency increment of 50 KHz. RDL had already developed digital countdown techniques which enable division by any integer from frequencies well over 500 MHz. Also very stable VCXO's are available in the 31 MHz region.

Referring to Figure 5, then, we proposed that the Fluke 6160A be eliminated entirely and the HP5061A, 5 MHz, cesium beam standard be utilized directly as a reference signal. The 5 MHz reference would be followed directly by the crystal filter shown in Figure 1B.

The crystal filter shown is a practical unit that is somewhat reasonable in cost. More exotic filters are available which can filter the atomic standard to nearly -150 dB/Hz signal-to-noise ratio at 100 Hz from the carrier. With this type of filter, the noise specification could be met at approximately 50 Hz to 75 Hz from the carrier. These filters are many times more expensive than the unit proposed.

In Method 4, the filtered 5.0 MHz signal and the 31 MHz VCXO are divided to 50 KHz, the smallest increment needed. The signals are compared and the 31 MHz VCXO is phase locked, using a very narrow loop which attenuates the 50 KHz from the 31 MHz signal. The loop also contains a 50 KHz notch filter for additional attenuation. Three VCXO's were proposed; 31.150 MHz, 31.200 MHz, and 31.250 MHz. (These were later reduced to two and changed to 30.05 and 30.10 MHz.) Frequency selection is done by a manual rotary switch at the oscillator unit. The F.M. noise, at this point, looks like the reference multiplied to

31 MHz out to about 400 Hz from the carrier. Farther away, the signal takes on the VCXO characteristic.

Thus, we have a 31.20 MHz reference with 50 KHz spurs <-130 dB relative to the carrier. This reference is used to phase lock a 468 MHz VCO. Since the 31.20 MHz reference is very large compared to the second phase lock loop bandwidth, the level of 31.20 MHz spurs near 468 MHz would be down <-140 dB.

The frequency spectrum now consists of the 468 MHz output with 50 KHz spurs <-106 dB and 31.20 MHz spurs <-140 dB. This spectrum is then multiplied X80 to the output. The 50 KHz spurs would be enhanced by 20 x log 80 = 38.1 dB (worst case) becoming <-68 dB relative to the output. The 31.20 MHz spurs would be attenuated significantly by the filtering of the multiplier stages. In the worst case, these will be enhanced by 38.1 dB to be <-102 dB and will never occur within 1 MHz of the receiver frequency.

The final output frequency spectrum consists of the carrier; 50 KHz spurs <-68 dB down from the carrier; two spurs of the 468 MHz in the -100 dB bands, <-60 dB down, and >72 MHz from the receiver frequency and spurious of 31.20 MHz, <-102 dB down, and never closer than 8.75 MHz from the receiver frequency. The final expected composite F.M. noise spectrum is shown in Figure 6.

Method 4 was considered clearly the superior to Methods 1, 2 and 3. It requires three VCXO's and an additional phase lock loop, however, this expense was weighted against the cost of the synthesizer used in the other three schemes.

The local oscillator has unusual mechanical constraints due to stringent size requirements and as a result was subdivided into several separate stages. A possible separation into three stages was shown in Figure 1 of the RFP. Through technical inquiry with NRL, it was known that Stage 1 could be further subdivided into two sections to minimize the drastic effects of the cable loss. This subdivision is shown in Figure 7 of the proposal.

Figure 8 shows the proposed local oscillator (Method 4) expanded and subdivided according to Figure 7. Stage 1, Section 1, contains three switchable, phase locked 31 MHz VCXO's and the 468 MHz phase locked VCO. Stage 1, Section 2 is separated by a cable with approximately 10.5 dB of loss. 200 mW at the input of Section 2 is amplified to 40 W at 468 MHz. This stage would require heat-sinking for 30 to 35 watts of dissipation. The 40 watt signal is attenuated to approximately 9 W by a length of cable having 6.5 dB of loss. These power levels were later revised, since the actual cable losses were smaller than those assumed in the proposal. Stage 2 is a X10 multiplier

and isolator generating 900 mW at 468 GHz. Stage 2 is followed by approximately 1 dB of cable loss and a X8 multiplier (Stage 3). The design of Stage 3 is extremely difficult due to the stringent mechanical requirements shown in the RFP.

2.3 DEVELOPMENT

The final block diagram of the first local oscillator is shown in Figure 17. Although numerous changes took place on the design of the individual blocks during the development of the first L.O., the final block diagram is virtually identical to the block diagram proposed and shown in Figure 8 of this report.

Many of the changes were mechanical. The RFP called for three stages: the first stage to be 100 cubic inches in volume maximum, followed by 70 feet of cable with 20 dB of loss; the second stage to be 5 cubic inches in volume maximum, followed by 2 feet of cable with 2 dB of loss; the third stage to be 3 cubic inches in volume maximum with no single dimension to be greater than 2.5 inches.

As proposed, the first stage was separated into Stage 1, Section 1 and Stage 1, Section 2. This was done to minimize the effects of the huge cable loss. The final cable losses

eased the design of the transistor power amplifiers. Sections 1 and 2 of Stage 1 were separated by a 7.3 dB final cable loss, Stages 1 and 2 were separated by a 4 dB final cable loss and Stages 2 and 3 were separated by a 1 dB cable loss.

During the contract, it was agreed that Stage 1, Section 2, Stage 2, and Stage 3 must be supplied in final mechanical configuration but that Stage 1, Section 1 would be supplied in a standard instrument cabinet to facilitate delivery. The designs of Stages 2 and 3 were modified to conform exactly to the available space in the pedestal. This necessitated the separation of the X4 and X2 multipliers, in Stage 3, by a cable with approximately 1 dB of loss. The mechanical constraints on Sections 2 and 3 were some of the largest problems affecting their designs.

After the contract award, the government requested that the number of frequencies be changed to two and that the frequencies be changed to 36.06 and 36.12 GHz. As a result, two VCXO's were required: one at 30.05 MHz and one at 30.01 MHz. The final frequencies and power levels are shown in Figure 17. The design of these switchable phase-locked VCXO's is essentially identical to that proposed. Both the 5 MHz reference and the

VCXO's are divided and phase compared at the same frequency of 50 KHz. However, this section went through several generations of development to optimize the amplifier gain and loop bandwidth for automatic lock, stability, spurious and noise performance.

The next block, the phase locked VCO at 450 MHz, is also essentially identical to the block diagram proposed. However, several design approaches were tried and several generations of development were required on the final design. Originally, the VCO was to be divided by 15, phase locked to the VCXO which was to be divided to the 50 KHz reference, phase compared and locked by an outside loop to the VCO. Difficulty was encountered in optimizing the bandwidths of the two loops which interacted and thus caused problems with stability and noise. The final design treated the VCXO and the VCO as two independent phase lock loops. The phase locked VCXO is multiplied via a comb generator and phase compared at the output in the conventional way. The VCXO has very high gain and narrow loop bandwidth whereas the VCO has wider loop bandwidth and less gain. These loops are now quite independent. Again, several generations of development were required to optimize gain and bandwidth for automatic lock, stability, spurious and noise performance.

With the separation of Stage 1, Sections 1 and 2 and the reduced cable losses, the development of the two power amplifiers became straight forward, using readily available power transisters. No hybrid combining was required. Refer to Figure 17 for power levels and frequencies.

The times ten multiplier in Stage 2 of the L.O. was developed as proposed. The final configuration is only slightly different from that shown in Figure 2 of the amendment to the proposal. It became necessary to provide right angle connectors at both the input and output of the multiplier and to mount the circulator vertically. This was needed to shorten the overall length and to accommodate cables. Cooling fins were also added as a precaution, because of the anticipated severe temperature rise in the pedestol.

The times ten multiplier consists of a lumped-element low pass input matching structure, matching a single chip, high breakdown, step recovery diode. At the output, the diode is transformer coupled to a 3-pole combine filter.

The mechanical configuration of Stage 3 provided more difficult problems. Originally, as proposed, the times four and times two frequency multipliers were to be integrated as a single unit. However, this became incompatible with the final pedestol design. It was necessary to separate the two

multipliers by a short length of semi-rigid cable. The power loss and added VSWR were overcome, however.

The times four utilizes an interdigital filter at input and output with a high quality step recovery diode embedded at the center. An idler is also provided for the second harmonic. Fins were also added as its only source of cooling.

The times two multiplier is a self-contained unit with a coaxial input and a waveguide output. An ultra high cutoff gallium arsenide variactor is utilized. The cutoff frequency of the output waveguide was raised to filter out unwanted spurious. An attenuation is provided at the output to turn the power from the 10-15 mW range down to as low as 1 mW. A waveguide isolator is provided at the output.

2.4 CONCLUSIONS

The major accomplishment of the first L.O. is that the power, spurious, switchability and mechanical configuration were achieved. Stage 1, Section 1, however, is not in final mechanical configuration. This was an important objective for the second L.O. Also, the noise performance is close to that proposed. A graph showing the specification, the predicted performance from the proposal and measured data are shown in Figure 14. The measured results are approximately equal to a

or better than the predicted results from 1-KHz and greater from the carrier. The major reason for this is that a 5 MHz crystal filter could not be used at the input, because it was highly susceptible to vibration and acoustically coupled noise. By eliminating this filter, the predicted and resultant noise performance would have been essentially equivalent.

3.0 Ka-BAND VARACTOR MULTIPLIER CHAIN, LOCAL OSCILLATOR RDL MODEL NO. M01K162

3.1 OBJECTIVES

This local oscillator is identical to the first local oscillator, model number M01K161 except for the two output frequencies which are 38.76 and 38.82 GHz. The requirement for a second local oscillator did not occur until after the initial contract award. Through amendment to the contract, the government requested a change in frequency of the first local oscillator and the additions of a second local oscillator at new frequencies.

The objectives were, therefore, the same as those outlined in paragraph 2.1 for the first L.O. with the additional objective of reducing the size of Stage 1, Section 1.

3.2 HISTORY

The history surrounding the design of the second local oscillator is essentially identical to that of the first local oscillator and is described in detail in paragraph 2.2. The second L.O. is functionally identical to the second with the only difference being the frequencies.

3.3 DEVELOPMENT

As mentioned earlier, the only new objective for the second L.O. was to reduce the size of Stage 1, Section 1. The first and second L.O.'s are otherwise electrically and mechanically equivalent.

3.4 CONCLUSIONS

The reduction in size of Stage 1, Section 1 was accomplished with a resultant size of approximately 8 3/4 x 3 3/8 x 6. The other accomplishments of the first L.O. were duplicated. However, the measured noise performance was slightly better. A graph showing the specifications, projected results and measured results are shown in Figure 15. Again, since the crystal filter had to be eliminated due to vibration and acoustic performance, the measured results were approximately equal to or better than the projected results.

A simplified diagram of Method 1 is shown in Figure 9 and is the straightforward method of direct multiplication. Thus, any F.M. noise or close in spurious from the Fluke 645A are enhanced by 57.7 dB = 20 x log 768. Since a broad band of frequencies is required, and the input must be moved arbitrarily, no bandlimiting circuits may be provided at the output of the Fluke 645A. Without the input frequency exactly determined, the location and amplitude of spurious from the Fluke 645A are virtually unpredictable. The amplitude of spurious, however, are guaranteed to be <-100 dB from the output. When multiplied by 768, the possible spurious *could* be as high as -42 dB relative to the output. Thus, we saw that Method 1 would not meet the requirements of paragraph 4.1.1.5.

The F.M. noise characteristics of the transmitter exciter (Method 1) are shown in Figure 10. The characteristics of the HP 5061A cesium beam reference are shown. The HP5061A translated to the output of the Fluke 645A are shown, and finally, the Fluke 645A multiplied to 37.4 GHz are shown. From the graph, it could be seen that Method 1 would not meet the noise requirements of paragraph 4.1.1.6 from 20 Hz to approximately 350 Hz. However, the system limitation, again as with the L.O. was shown to be the HP5061A reference.

However, it was learned, from technical inquiry of NRL, that it is desirable to obtain a small frequency increment of 2 Hz or less at the Ka-Band output. The smallest frequency increment available from the Fluke 645A is .01 Hz. If this were multiplied X 768 as with Method 1, the smallest frequency increment at the output would be 7.68 Hz, which is too great. Therefore, a second method was proposed. A simplified diagram of Method 2 is shown in Figure 11. A mixer has been added to translate the Fluke 645A directly to 284.375 to 300.000 MHz. A high level Schottky mixer would be used and the mixer spurious level for the minimum bandwidth required by paragraph 4.1.1.1 is anticipated to be <-100 dB. The mixer output is then multiplied X 128 to the output. Therefore, the spurious level for the narrow band case would be as high as - 100 dB + 43 dB = 57 dB. For the wideband case, the mixer spurious would be more numerous, whose level are not exactly known and may be substantially worse than -100 dB. However, for Method 1, the anticipated spur, level at the output was as bad as -42 dB and we believed that the spurs from Method 2 would be as good or better. Now the frequency increment is .01 Hz multiplied X 128 = 1.28 Hz at the output and the objective has been met.

The pump signal for the mixer is a 330 MHz VCO, phase locked to the 5 MHz reference for frequency coherence. The anticipated noise characteristics of Method 2 are shown in Figure 12. The HP5061A reference is shown. The noise characteristics of the Fluke 645A at 45 MHz and the 330 MHz phase locked VCO are both derived from the 5 MHz reference and are shown in Figure 12. Since these two signals are mixed, it is apparent that the noise of the mixer output is then multiplied X 128 and is shown in Figure 12. The noise would meet the -60 dB specification at approximately 800 Hz from the carrier and does not get substantially better until 10 KHz.

We thus drew the following conclusions. Methods 1 and 2 have approximately the same spurious levels at the output. The noise performance of Method 2 would be slightly worse than Method 1, although they have the same performance close to the carrier. Neither would meet the specification close to the carrier because the basic limitation is the HP5061A reference. Method 2, however, was preferred to meet the requirement of small frequency increments at the output.

A more detailed block diagram of Method 2 is shown in Figure 13. All components were to be designed with the intent of meeting all of the design goals and requirements of the RFP. The parameters that were considered to be design goals are outlined in paragraph 4.1.1.1 and 4.1.1.2, and concern output frequency range and power.

4.3 DEVELOPMENT

Shortly after the contract award, it was agreed that the transmitter would also be provided in a standard instrument case. This was done in the interest of delivery. In this case, the mechanical constraints were secondary and priority was placed on electrical performance.

Two major changes were required in the transmitter chain during development. The first was the development of the 330 MHz phase locked VCO used as a pump for the mixer. As proposed, the transistor VCO at 330 MHz would have been divided down to and phase compared at 5 MHz. Using this scheme, various combinations of VCO, loop gain and loop bandwidths were tried, but resulting in inadequate noise performance. The scheme was then replaced with a phase-locked 5th overtone VCXO at 110 MHz multiplied times 3. This resulted in improved noise performance. However, even better noise performance was accomplished using a fun-

damental VCXO at 110/3 MHz multiplied times three and phase compared at 110 MHz. The output was then multiplied times three to 330 MHz.

The other major change was that the third times four multiplier was changed to two times two multipliers. The change was made after difficulty was encountered achieving the combined bandwidth and conversion efficiency. The first double utilizes interdigital filters at both input and output and a multichip step recovery diode. The second times two multiplier is a crossed waveguide structure utilizing a very fast step recovery diode and a waveguide bandpass filter at the output. An additional isolator was added between them.

Apart from these changes, the transmitter was developed as proposed.

4.4 CONCLUSIONS

Most of the electrical requirements of the specifications were achieved. The design goals of power output and 2 GHz bandwidth were not fully met. However, 10 - 20 mW over a 1.6 GHz bandwidth was achieved, which was sufficient for system performance.

A graph showing the specifications, the projected noise performance and the measured noise performance is shown in Figure 16. The measured performance is better than the projected performance of frequencies greater than 200 Hz from the carrier, but worse close in. The measured data is better than the specification at frequencies greater than 400 Hz from the carrier.

The final block diagram showing configuration, power levels and frequencies is shown in Figure 28.

Local Oscillator	M06K161
Local Oscillator	M01K161
Transmitter	M01K162

5.0 LOCAL OSCILLATORS

5.1 GENERAL DESCRIPTION

The Local Oscillator units (LO 1 and LO 2) are functionally similar. The block diagrams (Figures 17 and 20) are identical except for frequency and small differences in power levels within the system. Local oscillator No. 1 (Figure 17 has switch selectable outputs of 36060 or 36120 megahertz. L.O. No. 2 (Figure 20) has selectable outputs at 38760 or 38820 megahertz. Each L.O. is made up of a pair of phase locked voltage control crystal oscillators, a voltage controlled coaxial cavity oscillator, a two stage power amplifier and three cascaded (X10, X4, X2) diode multipliers.

The VCXO's within each L.O. are phased locked to an external 5 megahertz reference signal. In order to accomplish the phase comparison, a common frequency factor for the VCXO and the 5 megahertz reference must be selected. Phase comparison is done at the common frequency of 50 Kilohertz for both L.O.'s. The frequencies of 30.5 and 30.1 for the first L.O. requires a division of 601 or 602 while the second L.O. VCXO's at 32.3 and 32.35 megahertz are divided by 646 or 647 respectively. Control of the counters is via switches on the panel of each unit. A pair of switches are utilized on the

first L.O. while the second L.O. has a single toggle. The switches simultaneously control D.C. power to the VCXO's, select the required count and proper R.F. output.

The amplified output of the selected VCXO is used to divide a step recovery diode which generates a frequency spectrum of lines spaced at frequency intervals equal to the VCXO frequency. The 15th line at a nominal frequency of 450 megahertz is applied to a balanced phase detector along with a small amount of power from the 450 megahertz voltage controlled transister cavity oscillator. The resulting phase detected output is amplified, filtered and coupled to a varactor diode within the cavity oscillator to control the cavity frequency. The signal feedback caused the cavity to shift frequency until no frequency or phase difference exists. At this point the error voltage reduces to zero and no further correction occurs. The cavity is then phase locked to the 15th harmonic of the VCXO. The power of approximately 10 milliwatts is then amplified by a pair of cascaded amplifiers to 10 and 25 watts respectively. The 25 watts (minus cable loss) at 450 megahertz is applied to a times 10 multiplier which produces a nominal 500 milliwatts at 4.5 GHz. Final output at Ka-Band is developed by a cascaded X4 - X2 which takes the 4.5 GHz

input signal and generates approximately 10 milliwatts of L.O. power.

An interconnection diagram along with schematics of all the active circuits are enclosed with this report. This data is supplied to aid in understanding the system. If difficulty is encountered during operation of the equipment, the matter should be referred to RDL.

5.2 L.O. OPERATION

The L.O.'s are provided with two functional switches:

1) D.C. Power
2) Frequency Select

To place either L.O. 1 or L.O. 2 in operation requires only external + 28 VDC and 5 megahertz reference.

The L.O.'s are packaged into five interconnected units which are:

1) Phase Lock Circuits
2) Power Amplifiers
3) X10 Multiplier
4) X4 Multiplier
5) X2 Multiplier

5.2.1 LOCAL OSCILLATOR No. 1

The phase lock circuits are all contained within the rack mountable instrument type enclosure. An external 28 VDC must be connected to power terminals located at the rear of the enclosure. The 5 megahertz reference channel input is also located on the back panel. The reference level must be 4 milliwatts. The external amplifiers and multipliers should be connected with cables having a loss value equal to that shown in Figure 17.

Frequency selection is designated as high or low and refers to the output frequencies of 36060 or 36120 megahertz. Selection is done by throwing the pair (both must be thrown) of toggle switches on the front panel of the phase lock box.

Input Requirement L.O. 1

D.C. Power	+ 28 VDC at 3.6 amp
Signal	5 MHz at 4 milliwatts

5.2.2 LOCAL OSCILLATOR NO. 2

The phase lock circuits are all housed within a 6 x 9 x 3 inch box. The inputs/outputs and controls all located along the bottom front section just below the heat sink fin structure. The 5 megahertz reference input and the

450 megahertz output appear on the designated BNC connectors. The external power amplifier and multipliers should be interconnected with cables having the losses called out on Figure 20. Frequency selection and D.C. power are controlled by a center-off toggle switch. Placing the switch position on either side of center, designation high or low causes the L.O. to output frequencies of 38760 or 38820 megahertz.

Input Requirement L.O. 2

D.C. Power	+ 28 VDC at 4.3 amp
Signal	5 MHz at 4 milliwatts

6.0 GENERAL DESCRIPTION TRANSMITTER

The NRL transmitter unit (Figure 28) is made up of an externally stabilized very low noise frequency translator followed by a chain of frequency multipliers. The inputs to the system are a fixed 5 megahertz and a variable 30 megahertz tuneable over a range of 7%. The output between 10 and 20 milliwatts is developed at 36.6 to 38.2 6 Hz by a X144 multiplier. The 5 megahertz signal is used to phase lock a VCXO operating at one-ninth the translation mixer input frequency of 330 megaherts.

The circuits within units 1, 2, and 3 generate the required low noise drive to the up connecter mixer. The primary reference for the system is the externally supplied 5 megahertz signal. The reference is applied to a cascaded pair of multipliers to give a higher frequency reference at 110 megahertz. A very low noise voltage controlled crystal oscillator operating in the fundamental mode at 36.666667 megahertz is used to develop the drive for the cascaded X3 - X3 multipliers. Output of the first times 3 at 110 megahertz is phase compared with the high frequency reference to generate the required error signals to control the VCXO. The filter parameters are carefully set to guarantee the noise performance of the transmitter. The second X3 multiplier at 330 megahertz

drives the frequency translator. Each unit has been assembled with multipole filters to prevent the propagation of signal spurious. The lower sideband output of the mixer at nominal 300 megahertz provides the drive signal for the multiplier. The output of the mixer is a very low level signal of 80 microwatts. A cascade of three amplifiers boosts the drive power for the multipliers to approximately 20 watts. The frequencies and nominal power at each functional interface is given in Figure 28. The transmitter is completely contained within a 19 inch rack mountable instrument case.

A component location plan is given in Figure 29. Each subassembly is coded with a number which identifies the location within the enclosure. The same number is called out on the block diagram and where appropriate on the schematic associated with the modules. The information is provided to facilitate understanding of the system and not for maintenance purposes. In the event frequencies or powers are not at the levels assigned, the units should be referred to RDL for correction.

6.1 OPERATION TRANSMITTER

The transmitter has no operational controls. A D.C. power switch located on the front panel provides a local on/off function. All inputs and outputs are located at the rear of the enclosure. Input signals are via BNC connectors; D.C. power on banana jacks while the RF outlet at Ka is WR28 waveguide.

To place the system on the air the following inputs and levels must be provided:

D.C. Power

1 +28 VDC at 2.5 amps

2 - 5 VDC at .019 amps

Signals

1 5 MHz at 4 mw into 50 Ω

2 30 MHz (nominal) at 4 mw into 50 Ω

3 Control, TTL levels

When the above inputs are supplied the transmitter is made fully operational by placing the D.C. power switch on.

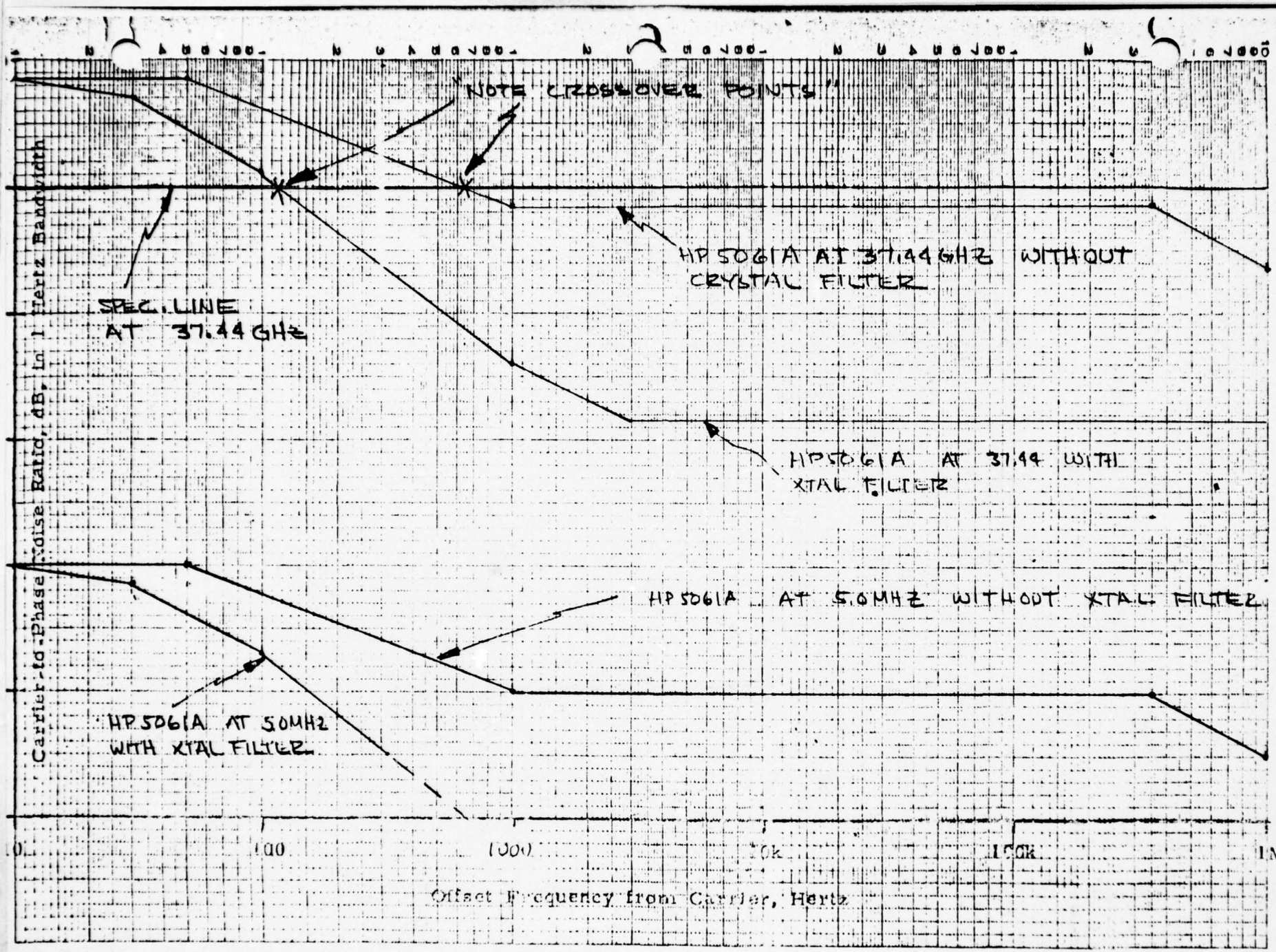

"NOTE CROSSOVER POINTS"
SPEC. LINE AT 37.44 GHz
HP 5061A AT 37.44 GHz WITHOUT CRYSTAL FILTER
HP5061A AT 37.44 WITH XTAL FILTER
HP 5061A AT 5.0MHz WITHOUT XTAL FILTER
HP 5061A AT 5.0MHz WITH XTAL FILTER
Carrier-to-Phase Noise Ratio, dB, in 1 Hertz Bandwidth
100
1000
10k
100k
1M
Offset Frequency from Carrier, Hertz

FIGURE 1A

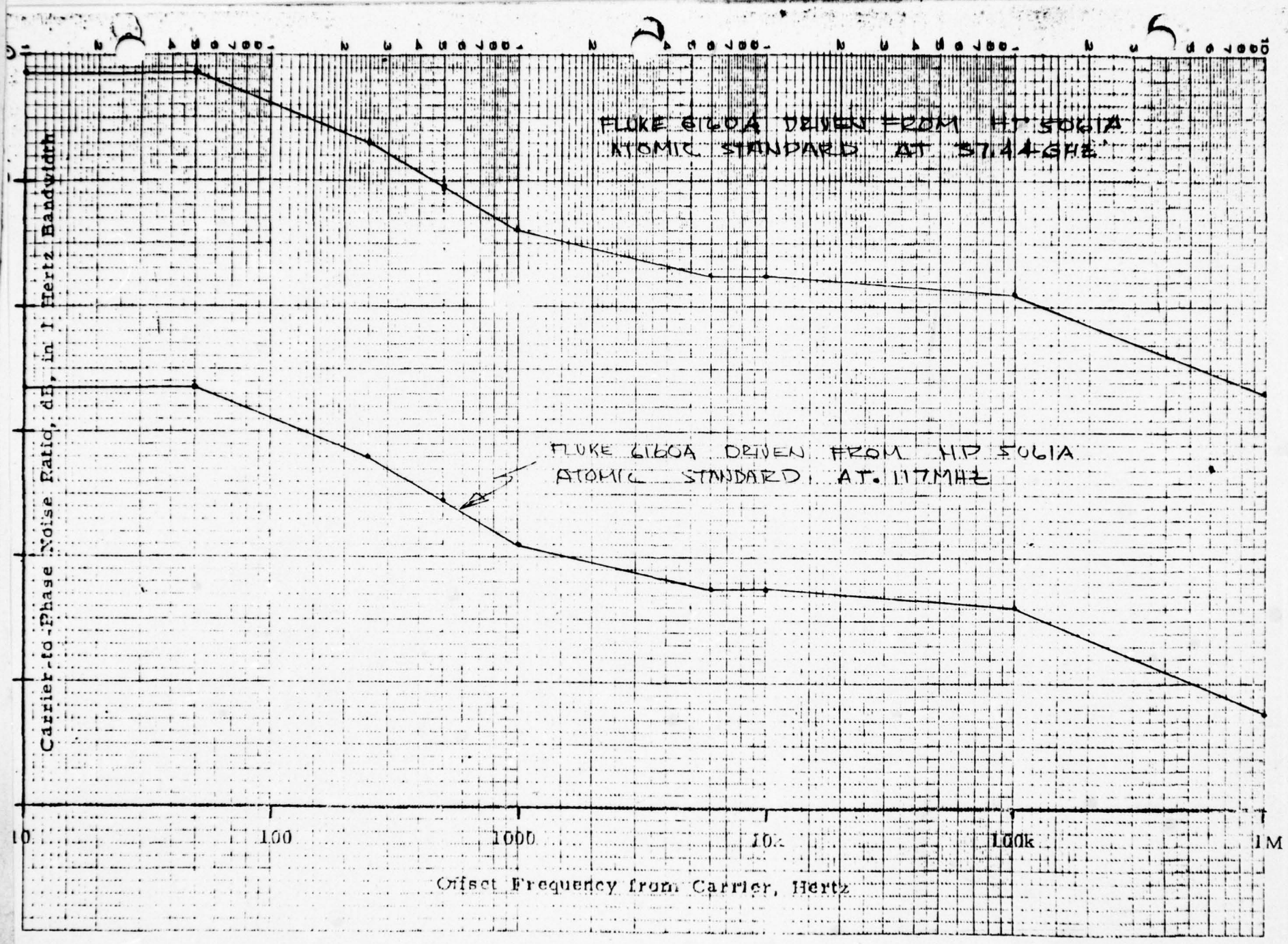

FLUKE 6160A DRIVEN FROM HP 5061A
ATOMIC STANDARD AT 5.44 GHz
FLUKE 6160A DRIVEN FROM HP 5061A
ATOMIC STANDARD AT 117MHz
Carrier-to-Phase Noise Ratio, dB, in 1 Hertz Bandwidth
10
100
1000
10k
100k
1M
Offset Frequency from Carrier, Hertz

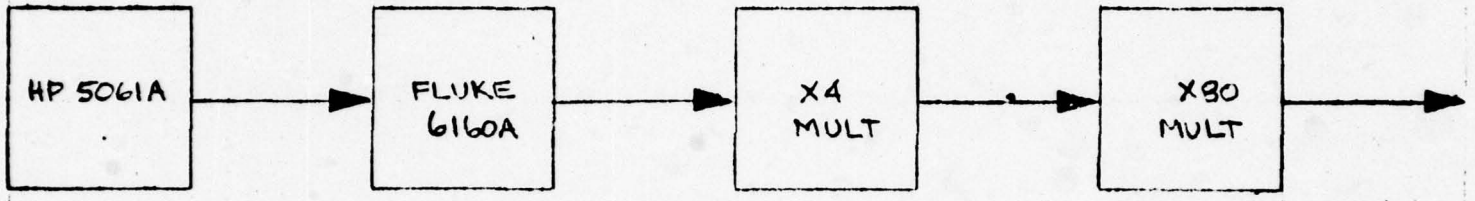
FIGURE 1 B

116.8125, 117.0000, 117.1875 MHZ

5 MHZ

467.25, 468.00, 468.75 MHZ

37.38, 37.44, 37.50 GHZ

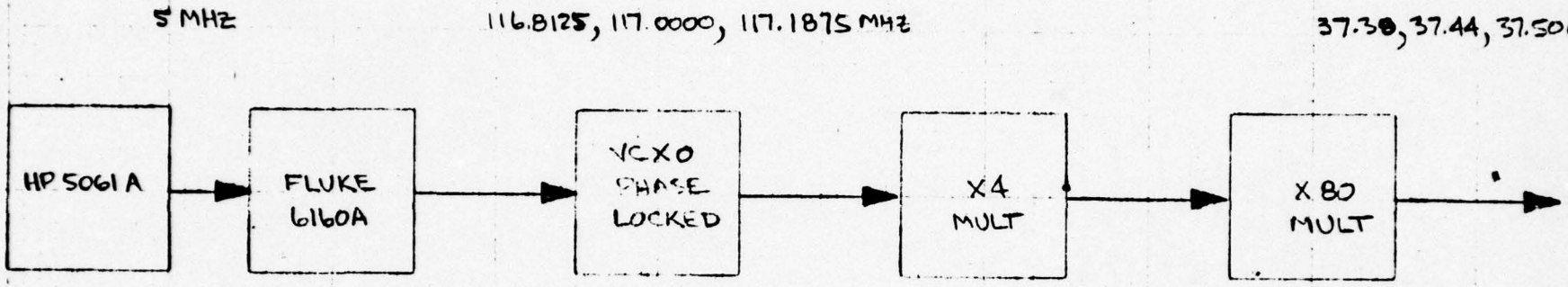


20 log 4 = 12.0 DB

20 log 80 = 38.1 DB

LOCAL OSCILLATOR – METHOD 1

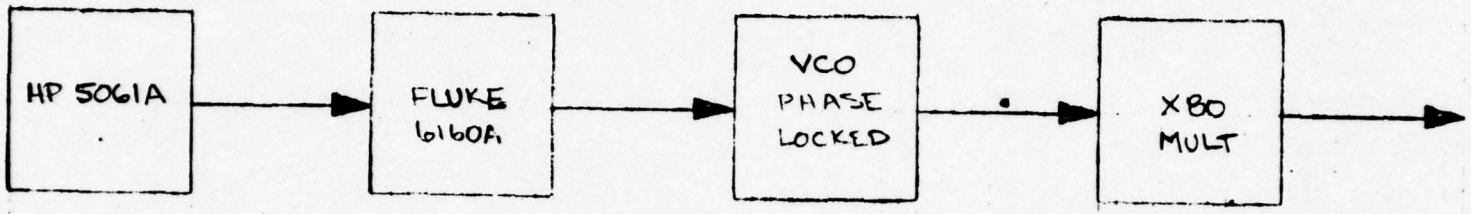
FIG. 2



LOCAL OSCILLATOR – METHOD 2

FIG. 3

116.8125, 117.00, 117.1875MHZ 467.25, 468.00, 468.75MHZ 37.38, 37.44, 37.50 GHZ

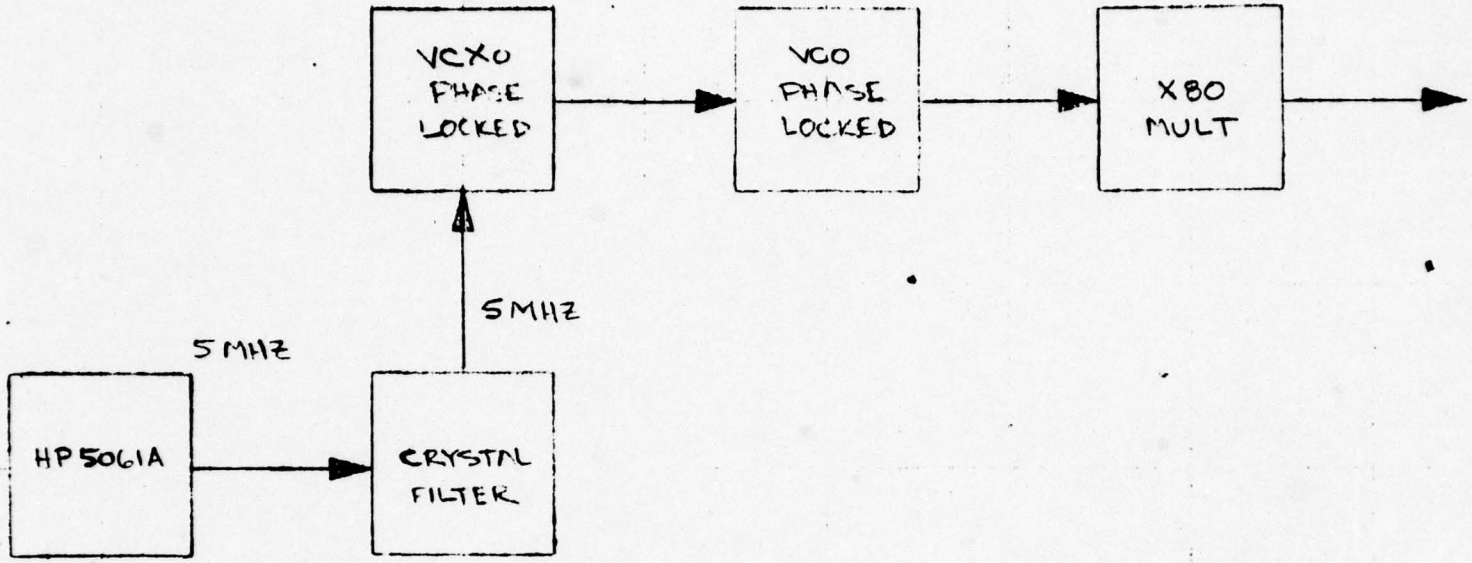


20 log 80 = 38.1 DB

LOCAL OSCILLATOR - METHOD 3

FIG. 4

31.15	467.25	37.38
31.20	468.00	37.44
31.25 MHz	468.75 MHz	37.50 GHz



20 log 7488 = 77.5 dB

LOCAL OSCILLATOR – METHOD 4

FIG. 5

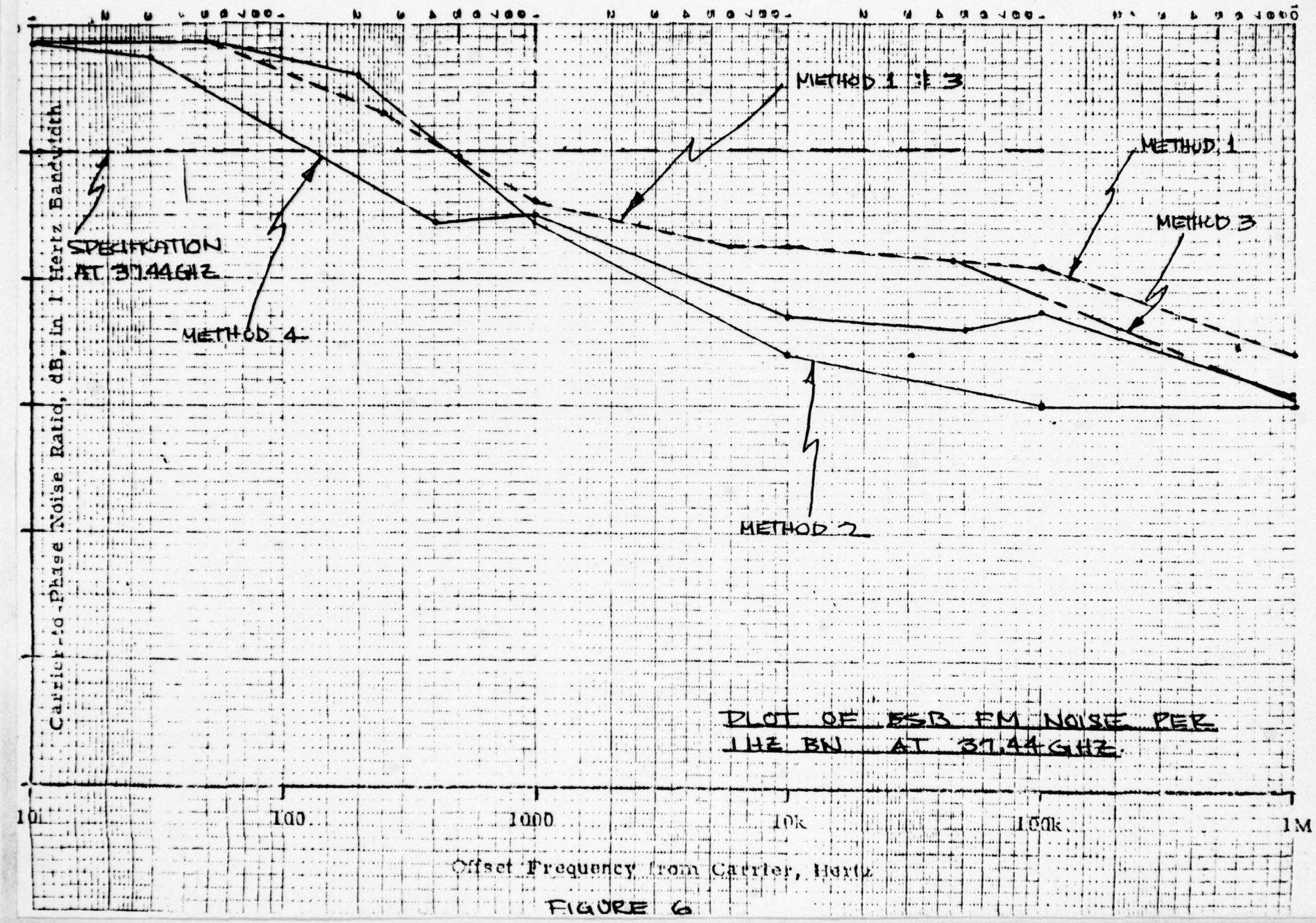
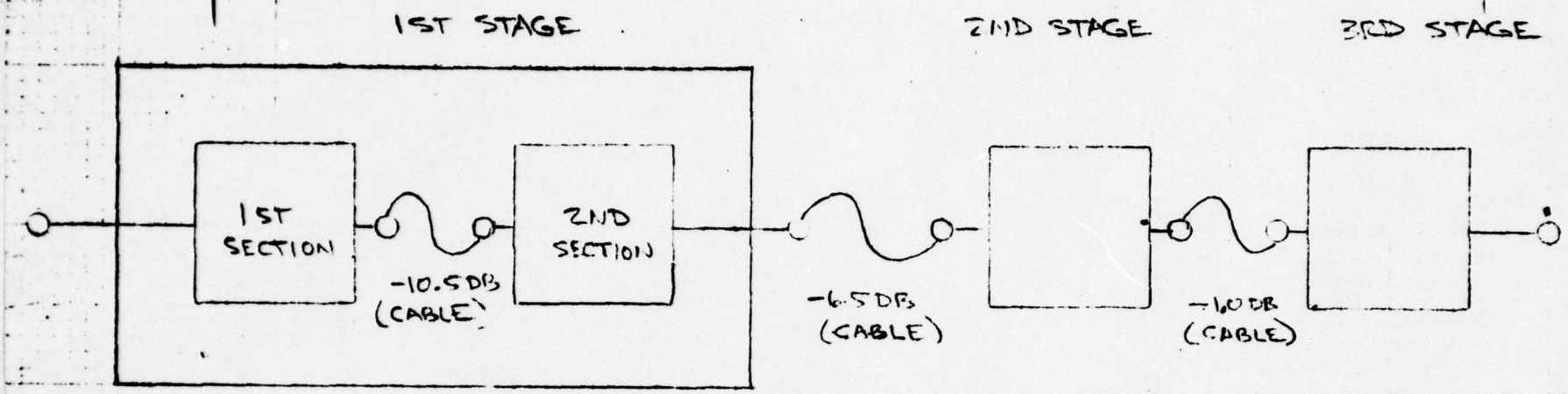
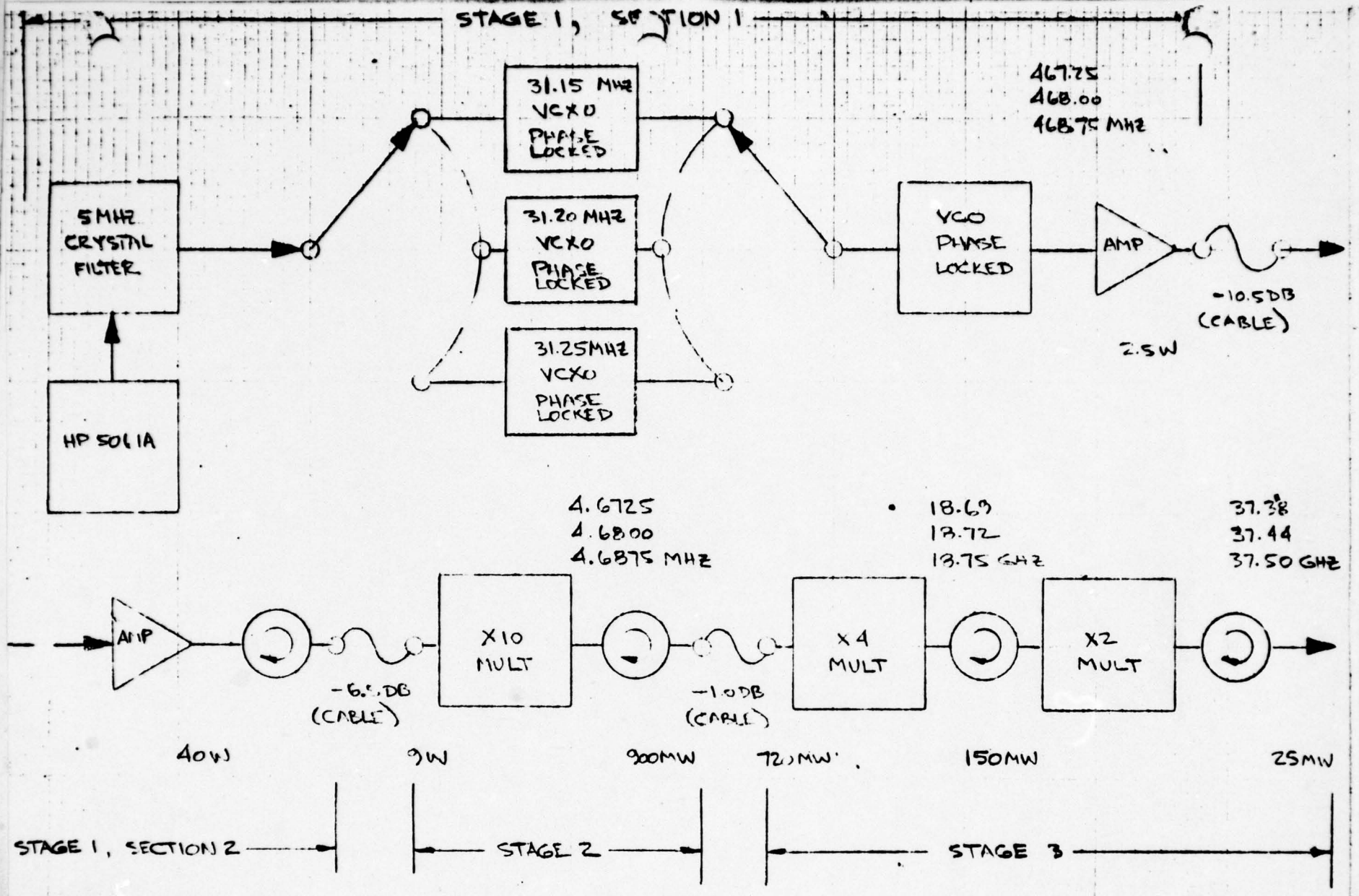


FIGURE 6



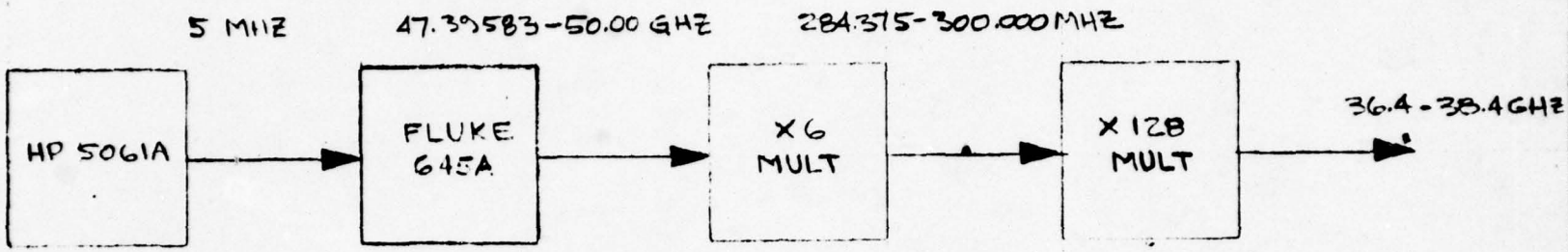
LOCAL OSCILLATOR

FIG. 7



LOCAL OSCILLATOR – METHOD 4

FIG. 8



$20 \log 10 = 20$ DB $\quad 20 \log 6 = 15.6$ DB $\quad 20 \log 128 = 42.2$ DB

TRANSMITTER EXCITER – METHOD 1

FIG. 9

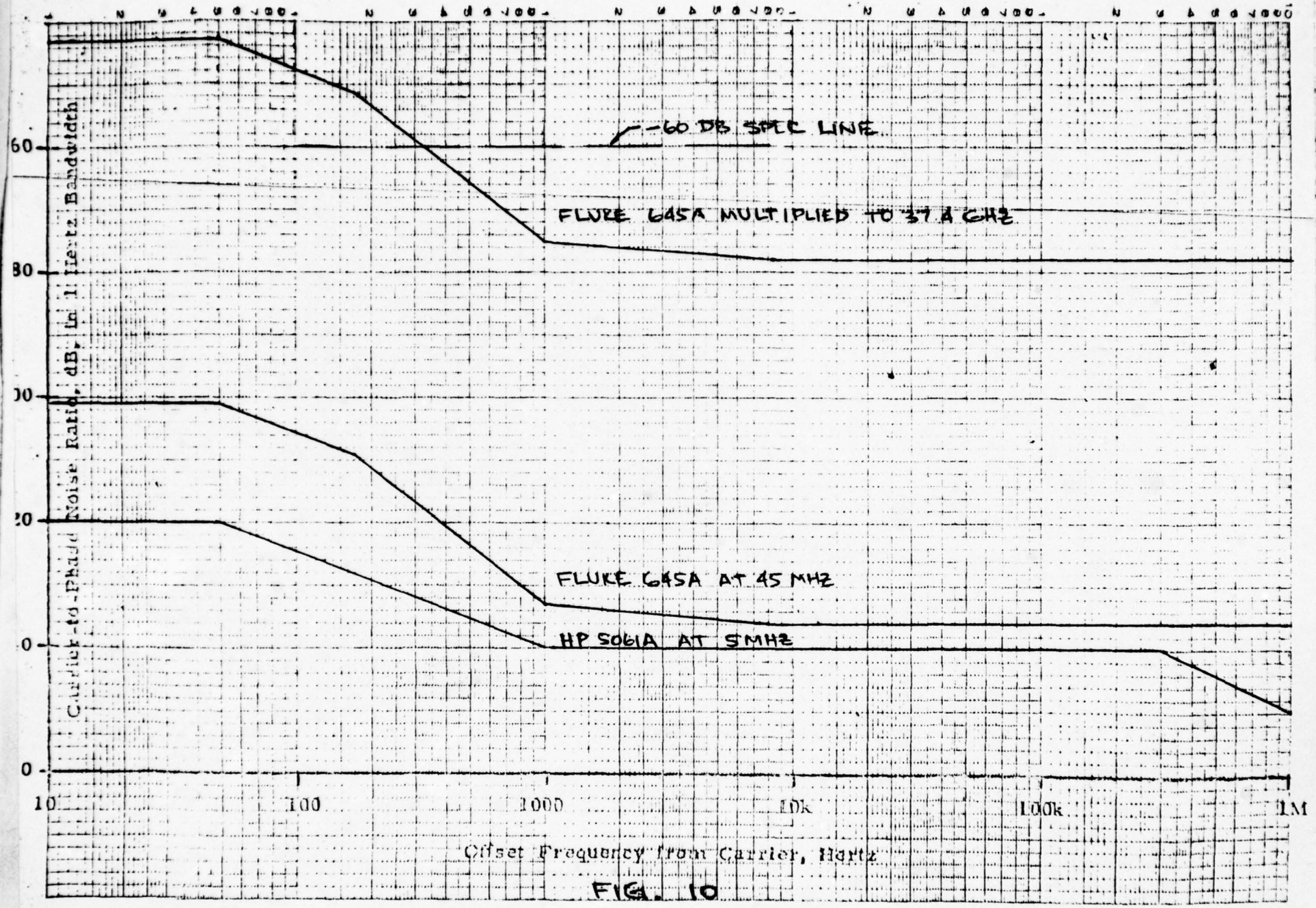
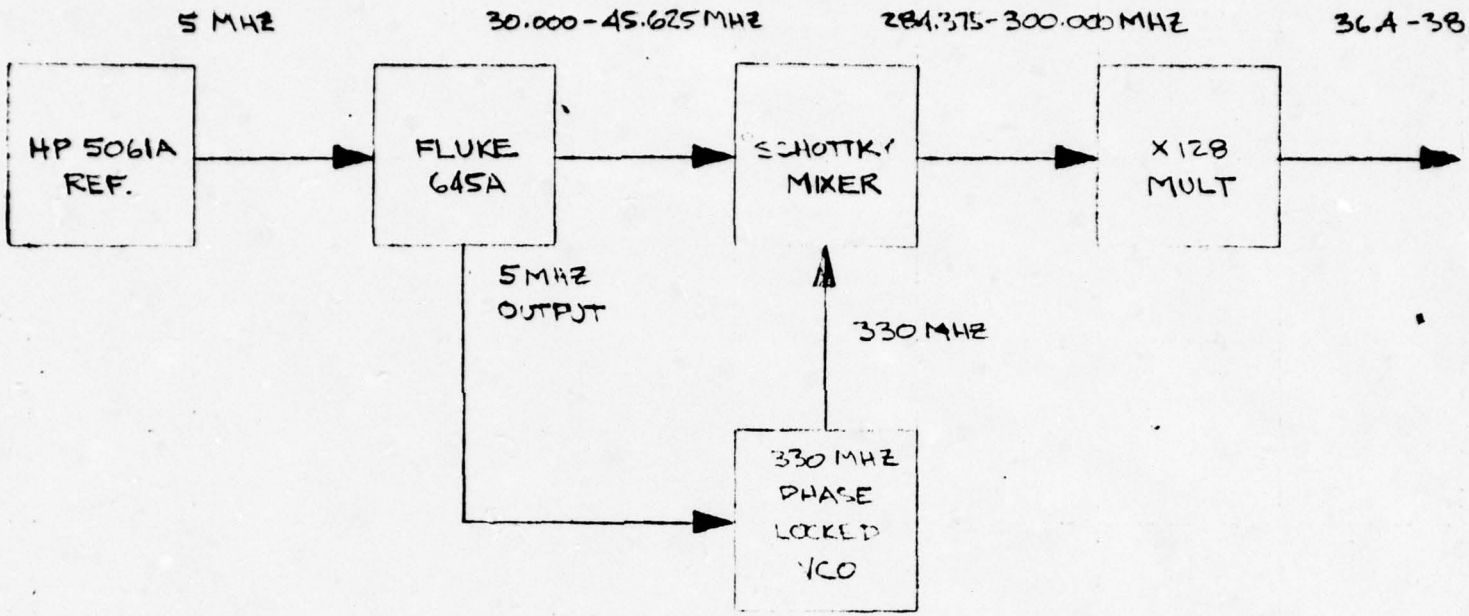


FIG. 10



TRANSMITTER EXCITER - METHOD 2

FIG. 11

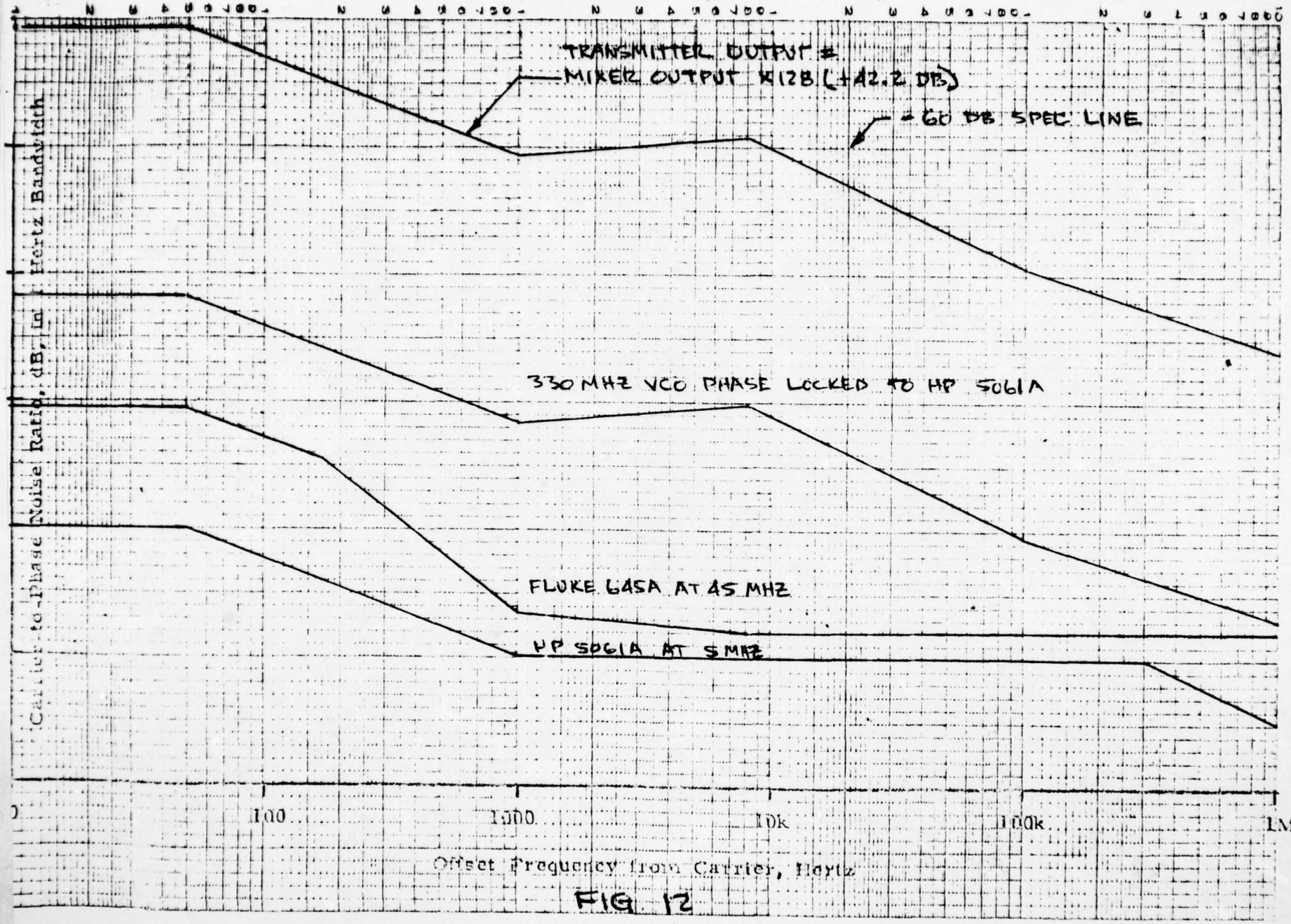
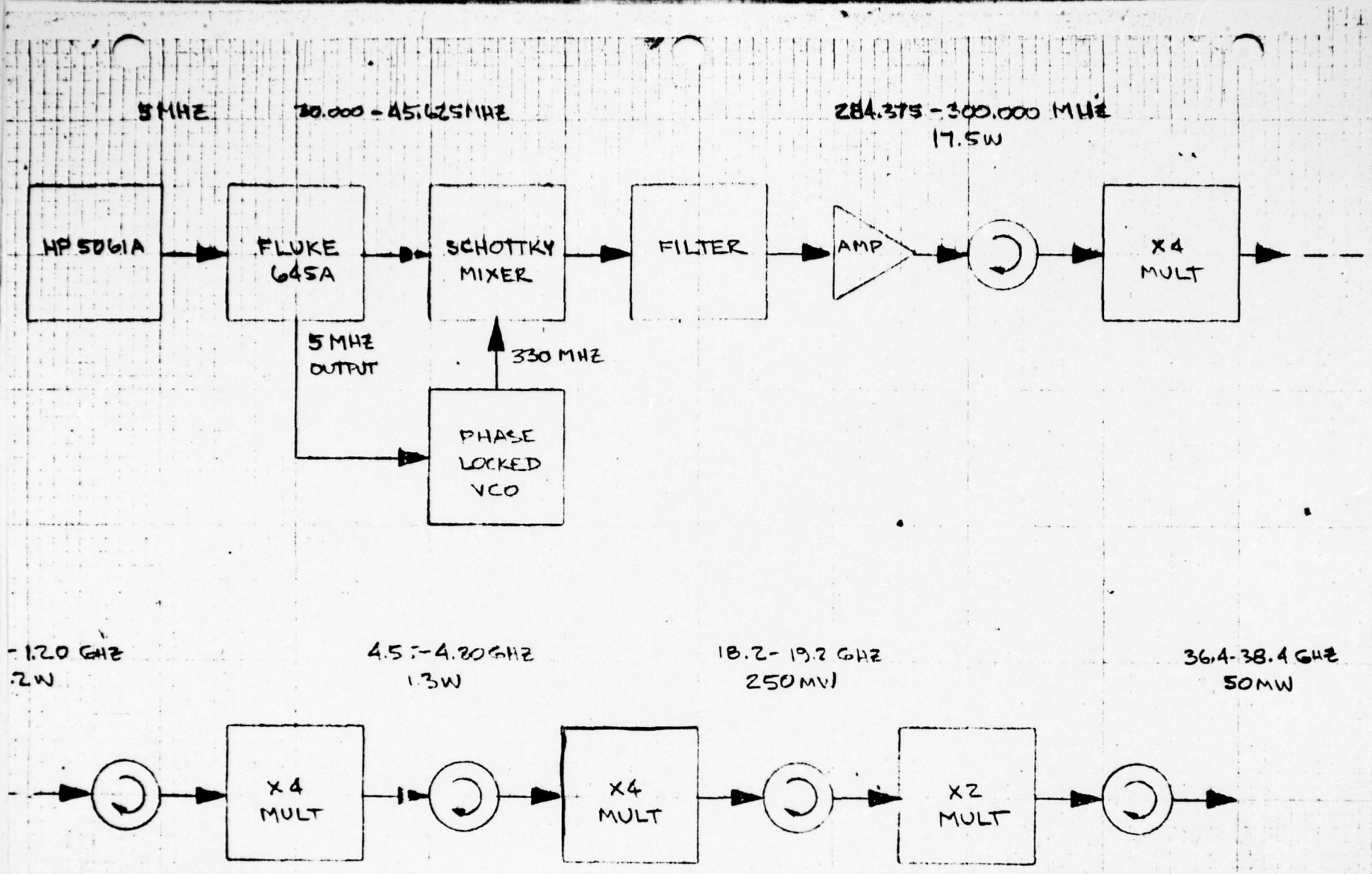


FIG 12



TRANSMITTER EXCITER - METHOD 2

FIG. 13

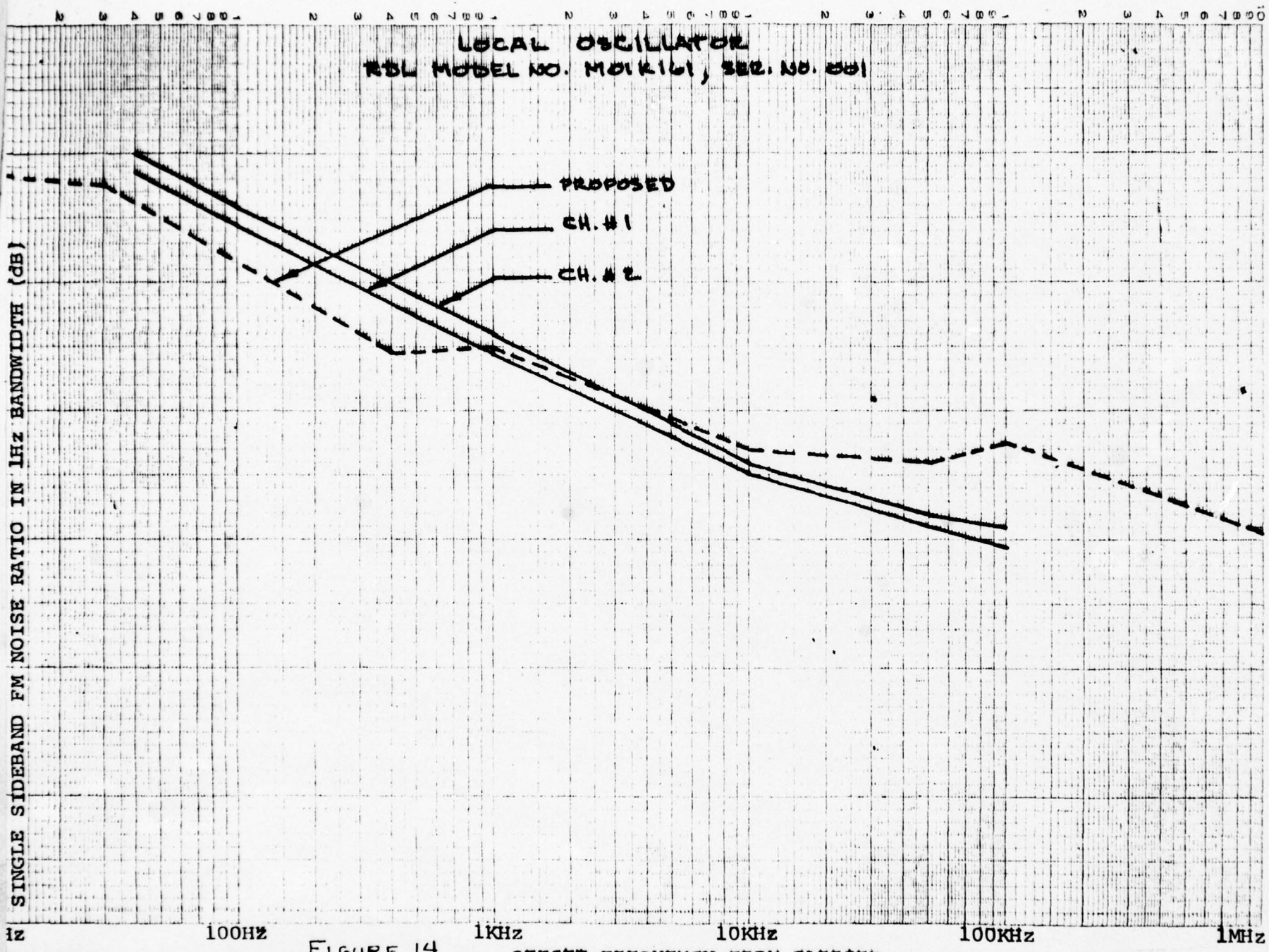


FIGURE 14

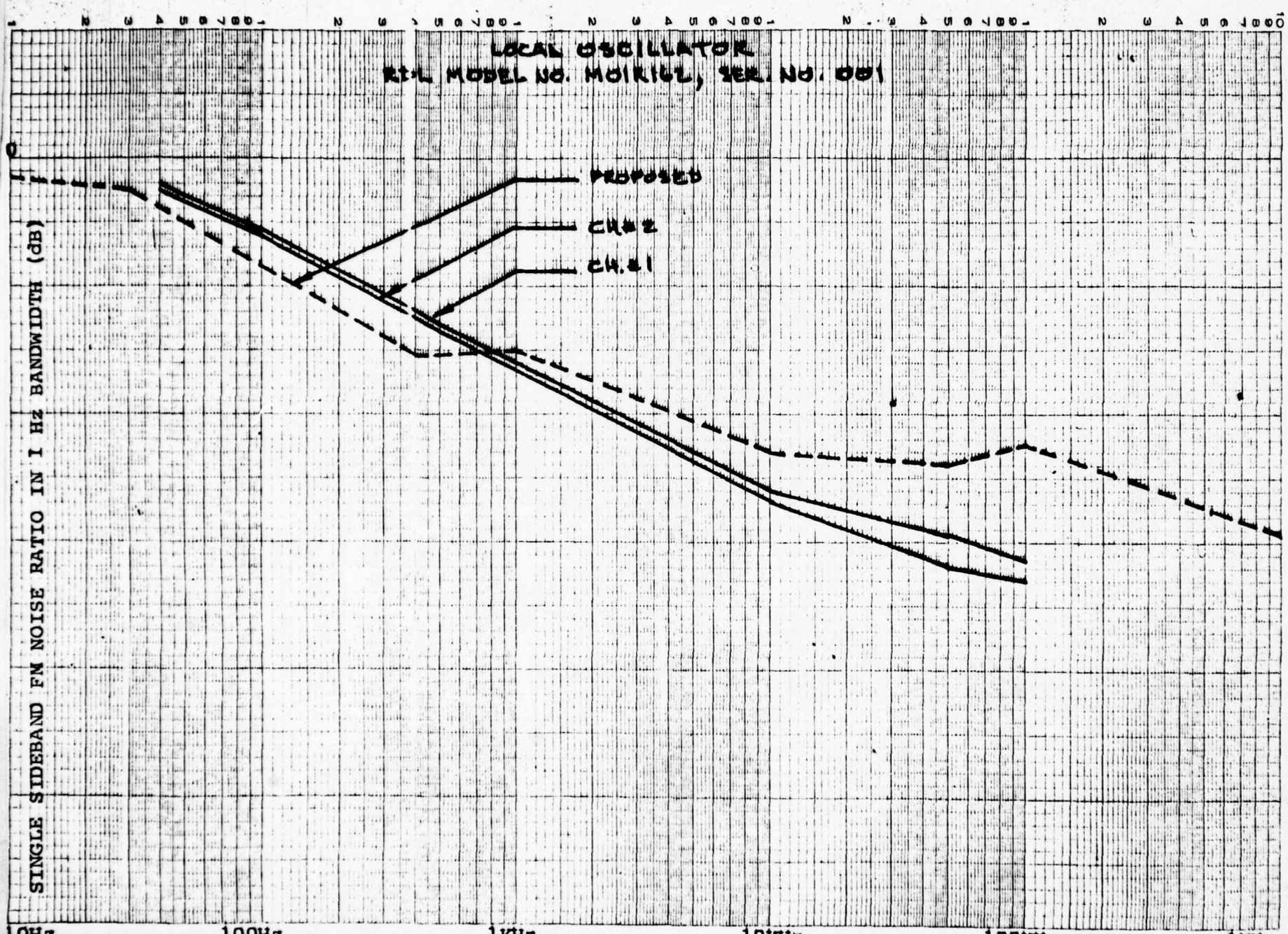


FIGURE 15

NO. 340-L510 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

EUGENE DIETZGEN CO.
MADE IN U. S. A.

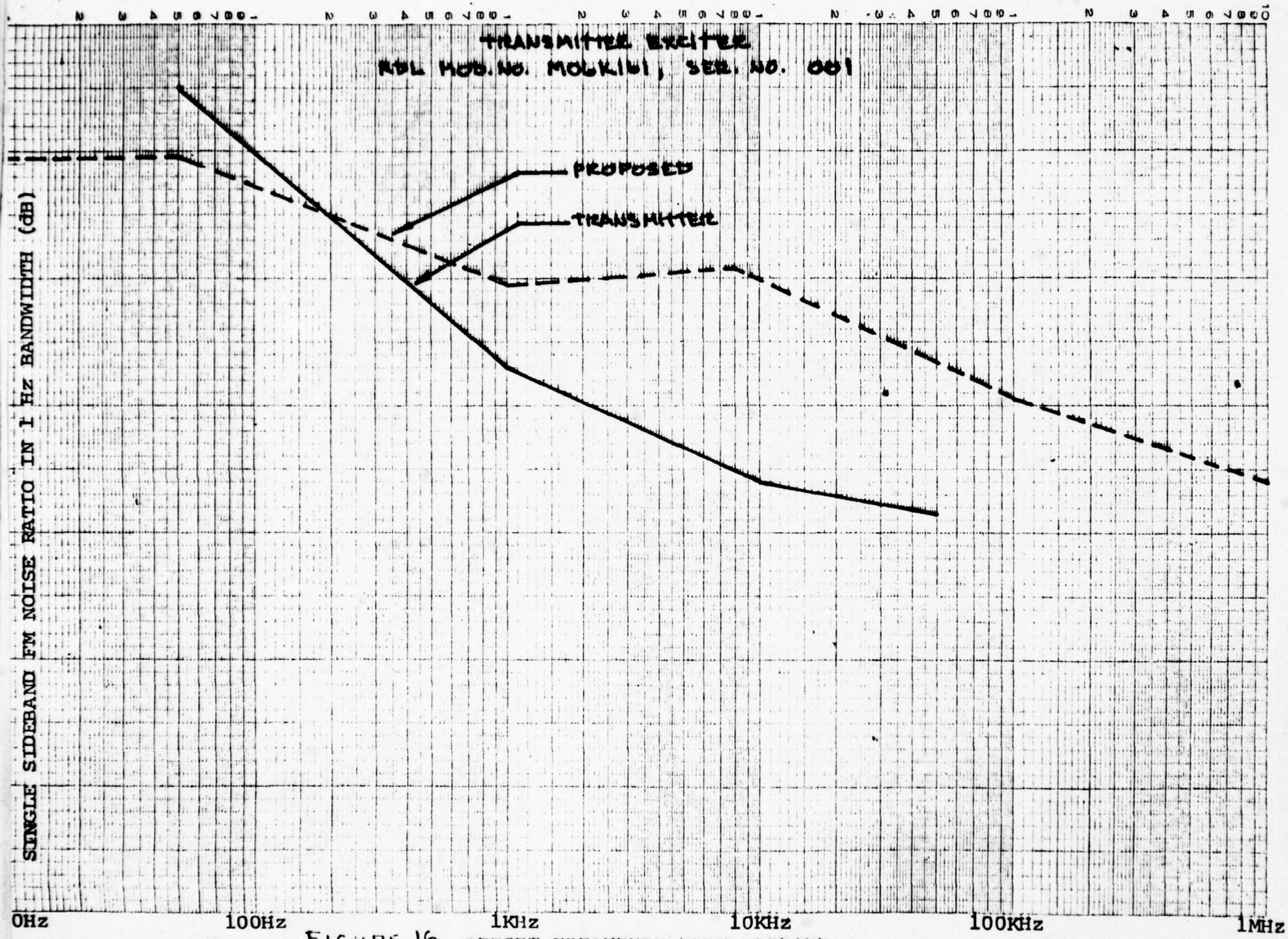


FIGURE 16

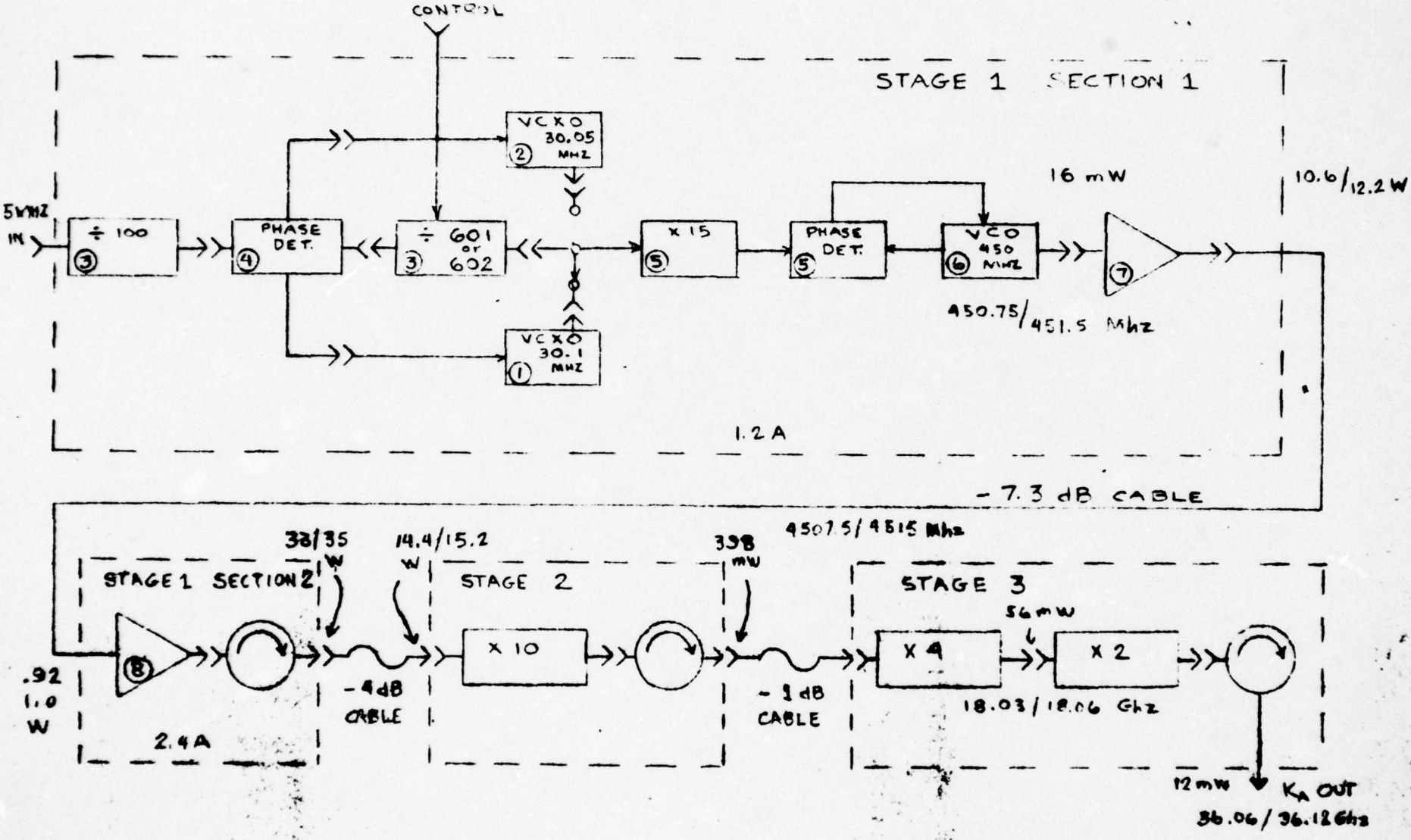
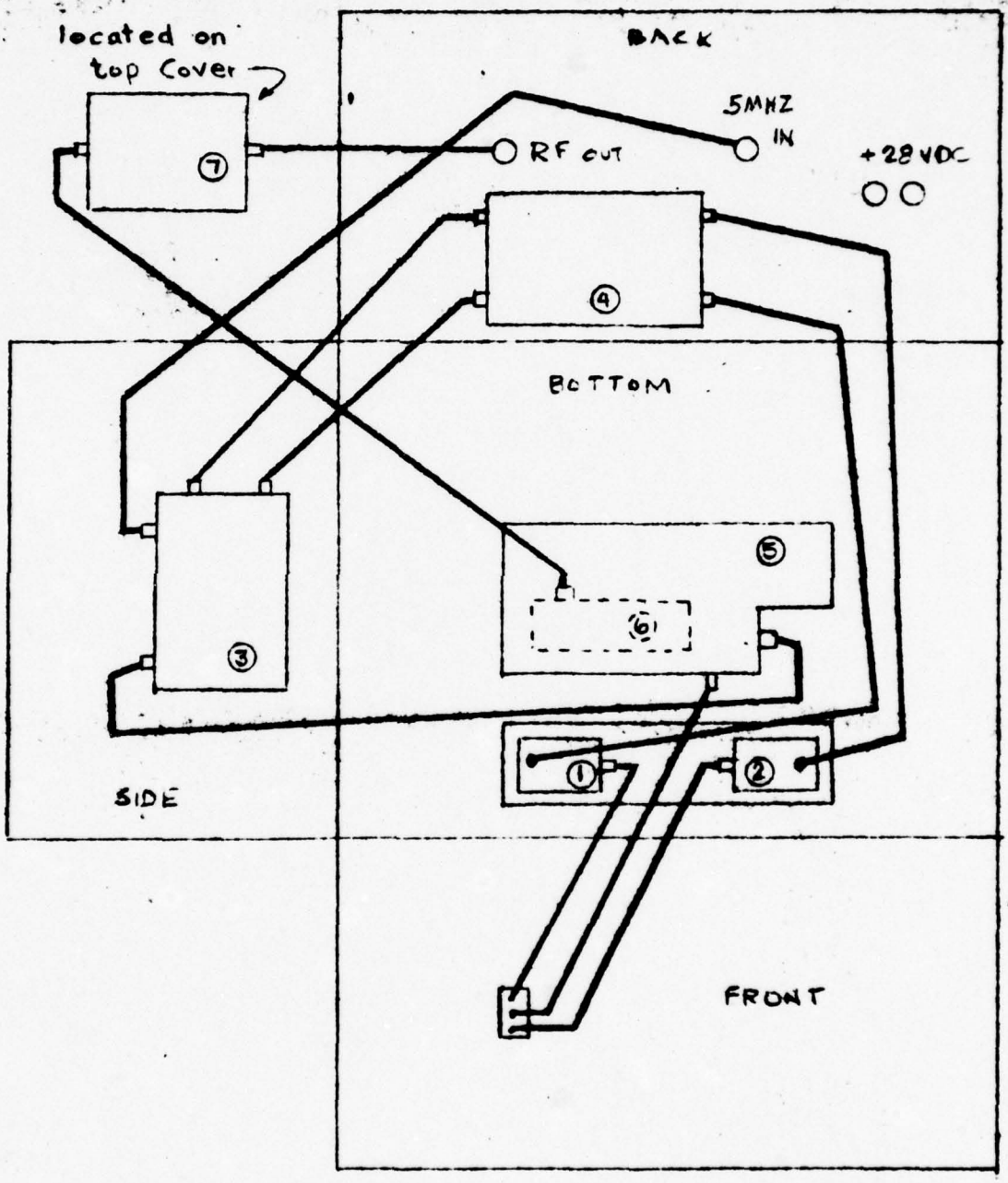


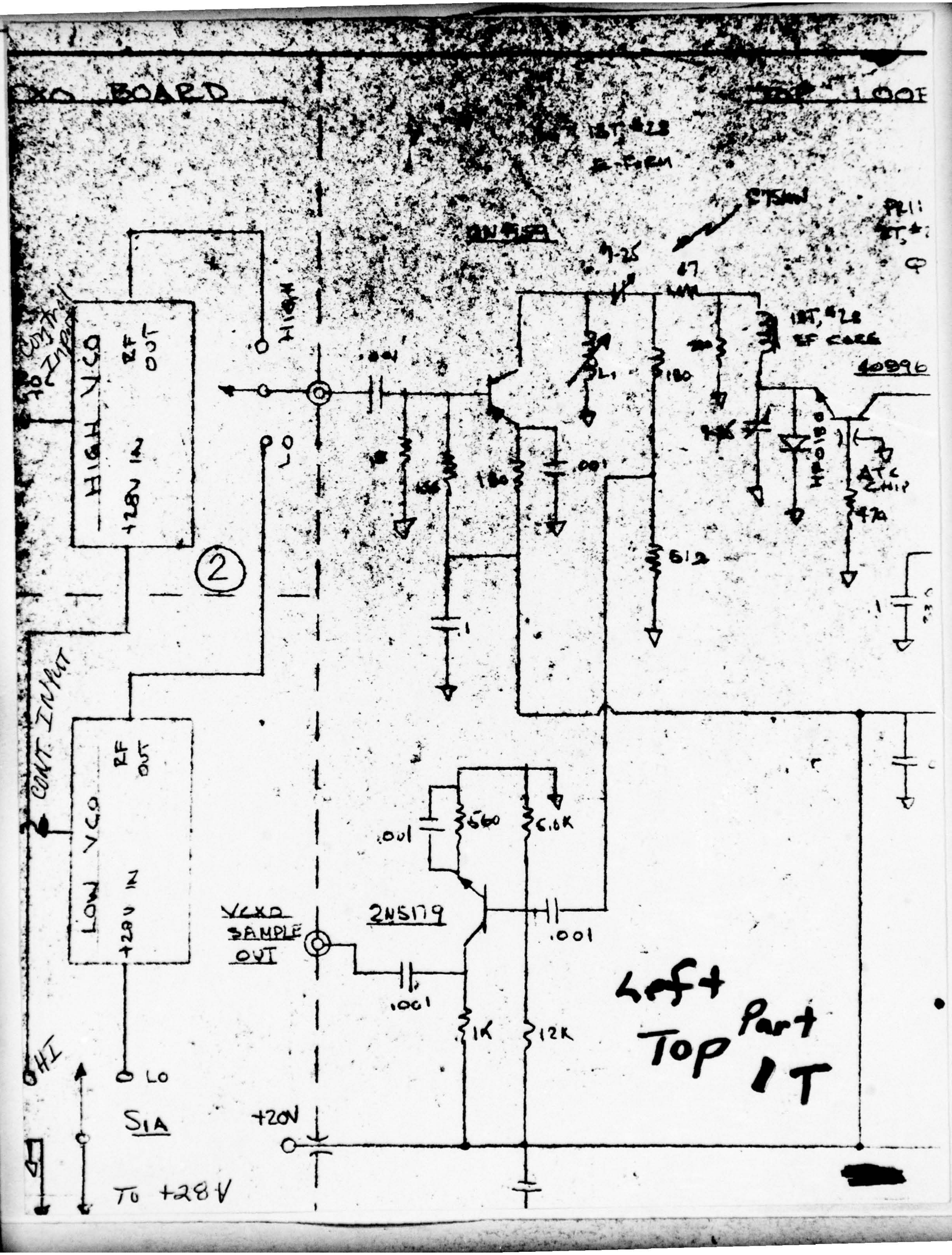
FIGURE 17

NRL 1ST L.O.

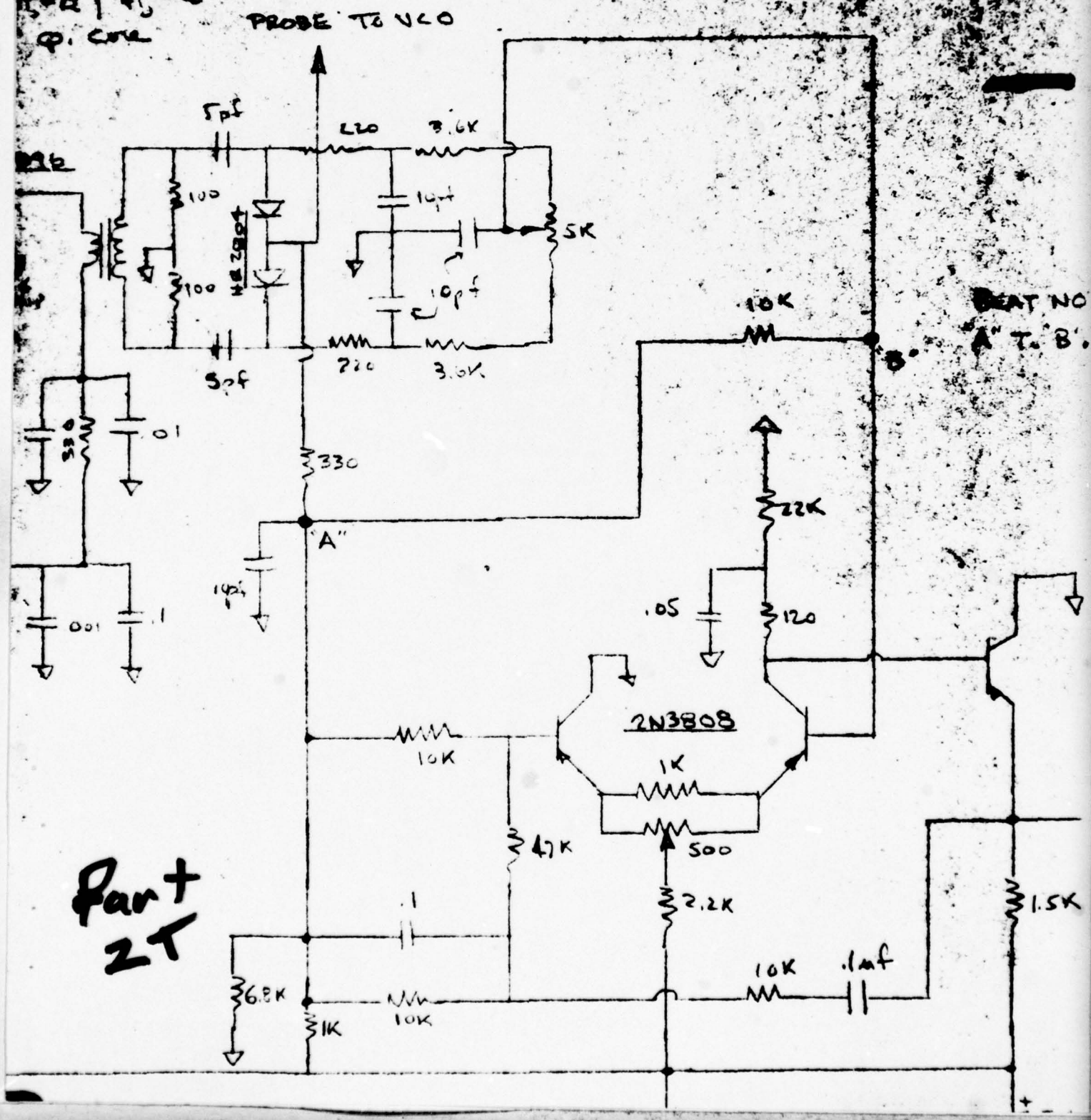


1 ST L.O.
STAGE 1 SECTION 1
(TOP VIEW)

FIGURE 18

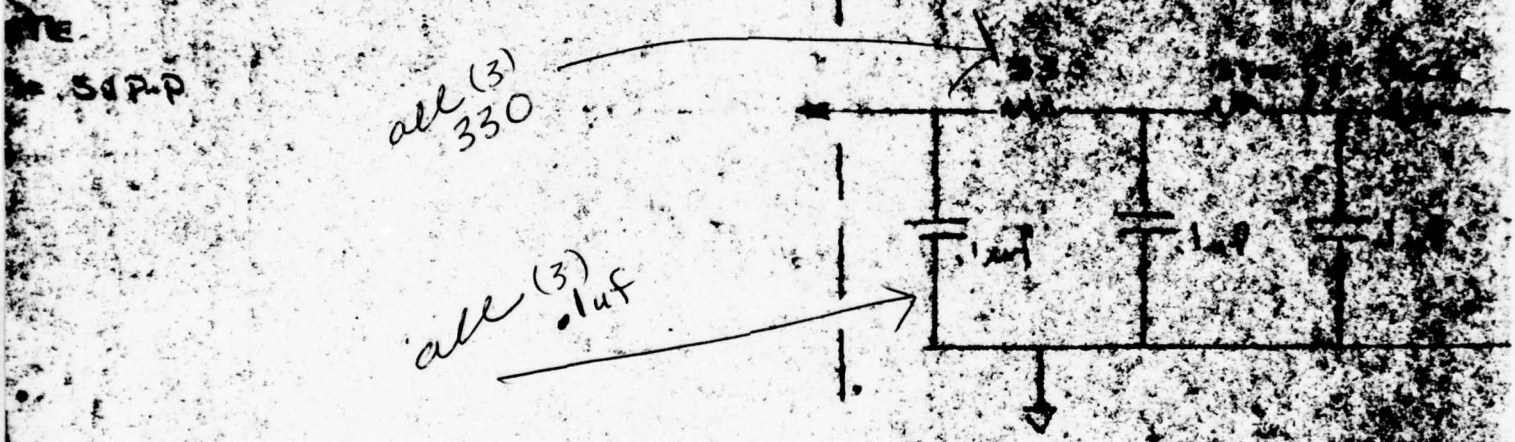

BOARD
HIGH VCO
RF OUT
+28V IN
Control Input
HIGH
LO
2
CONT INPUT
LOW VCO
RF OUT
+28V IN
VCXO SAMPLE OUT
2N5179
.001
560
1K
12K
+20V
HI
LO
S1A
To +28V
18T, #28 EF CORE
.001
180
512
.1
47
Left Top Part 1T

OP BOX

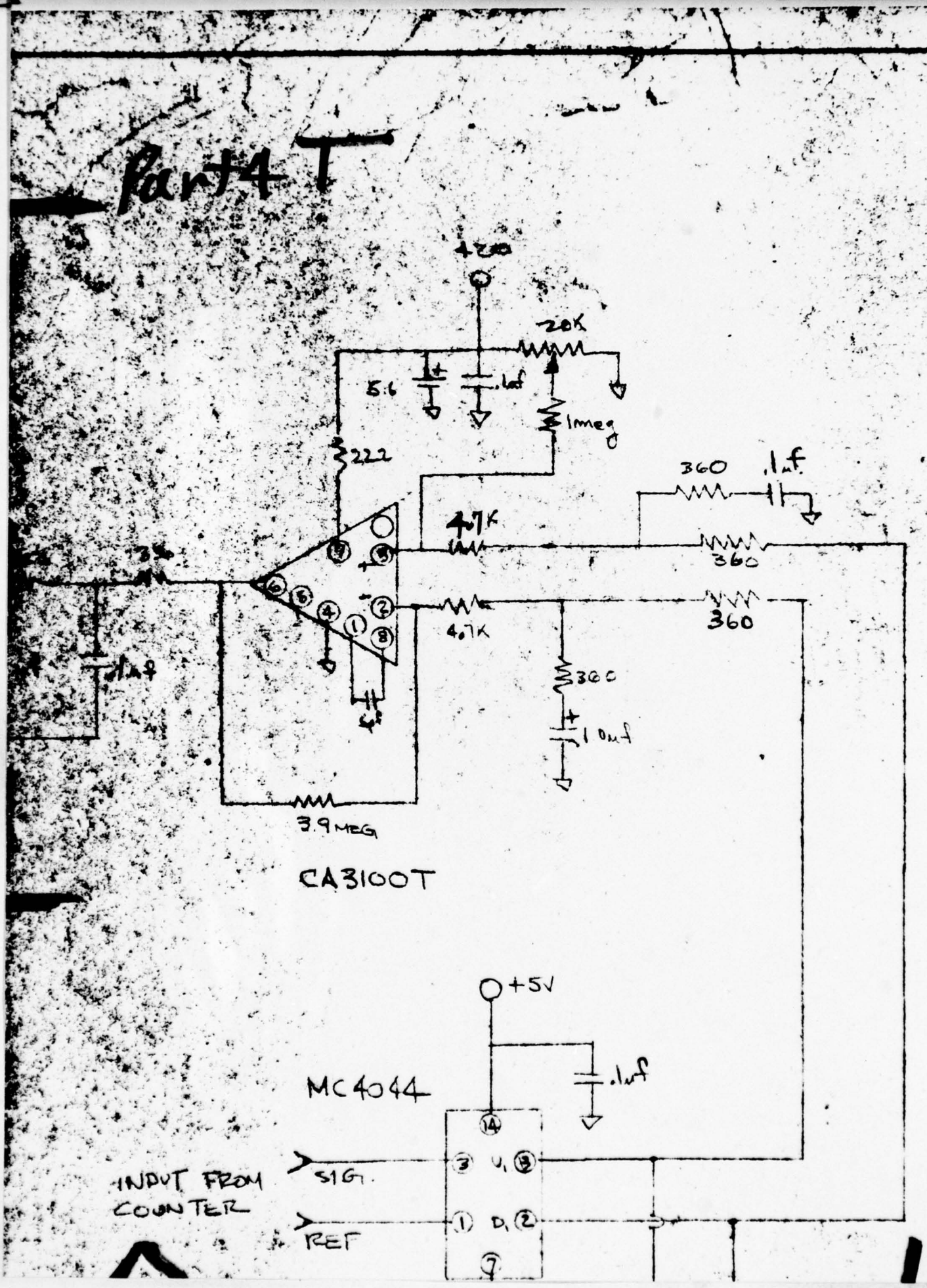

PROBE TO VCO
5pf
L20
3.6K
100
100
10pf
5K
10pf
5pf
220
3.0K
10K
BEAT NO
A" T. B'.
B'
330
22K
"A"
10pf
.05
120
2N3808
10K
1K
500
47K
2.2K
1.5K
.1
6.8K
1K
10K
10K
.1mf
Part 2T

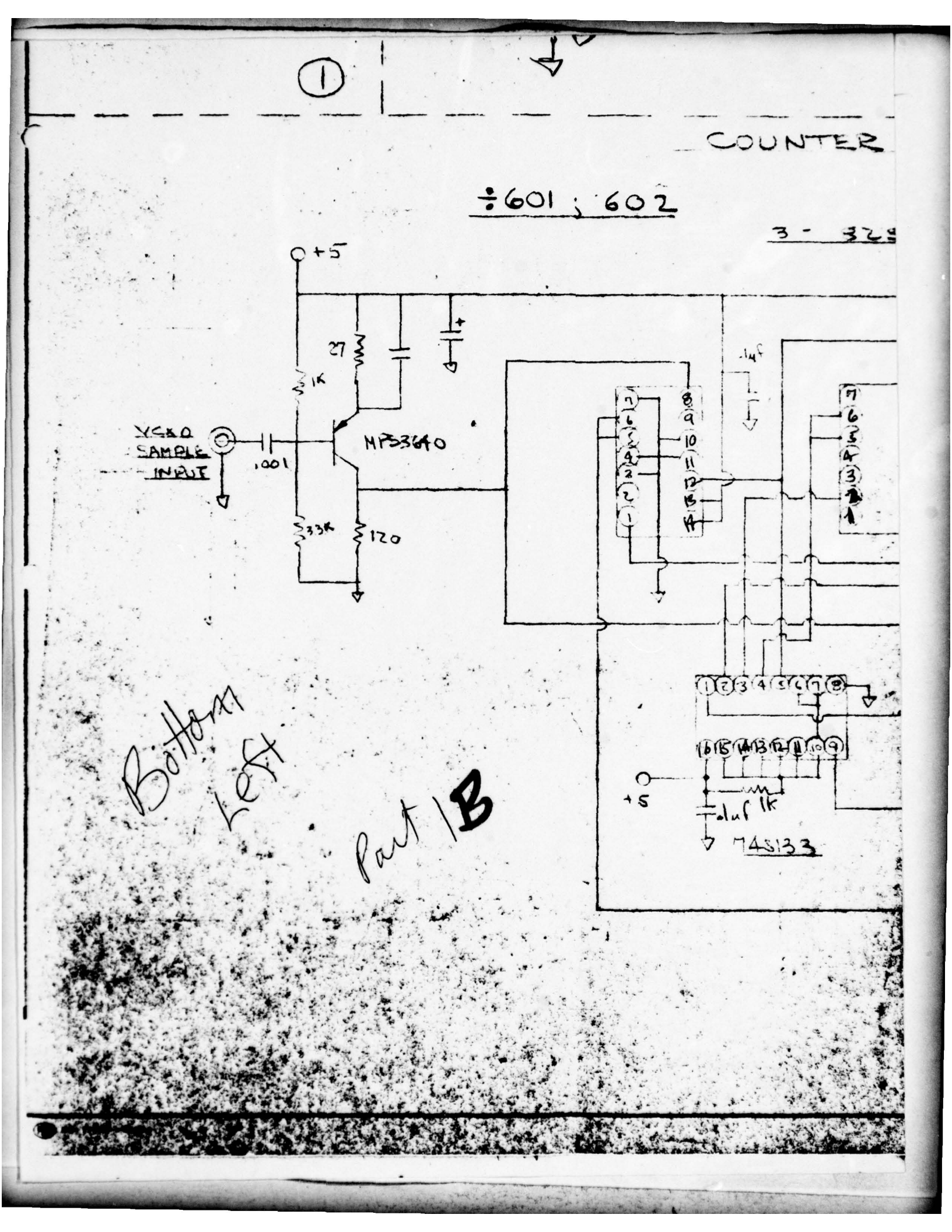
Part 3T

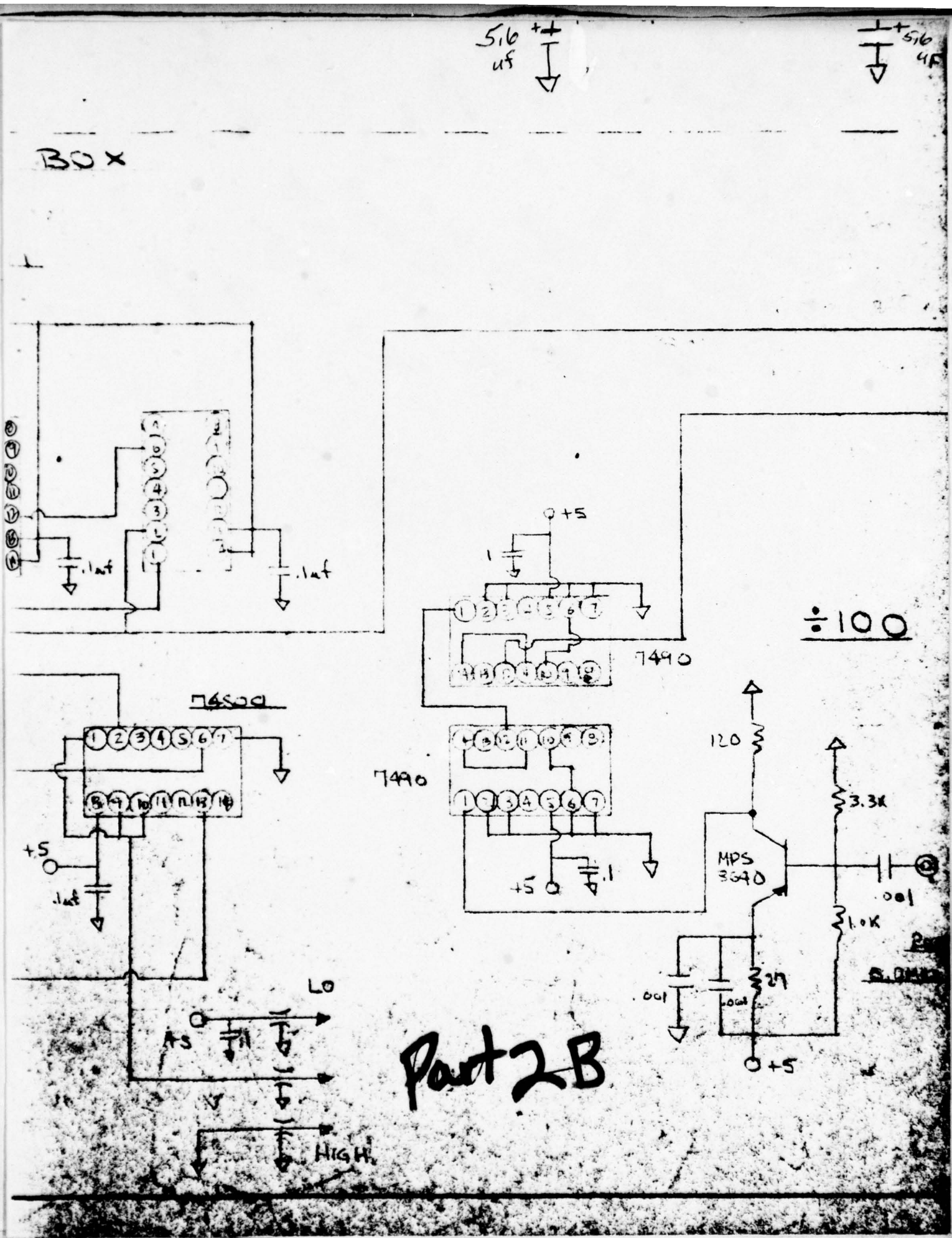
TO VCXO CONTROL INPUTS

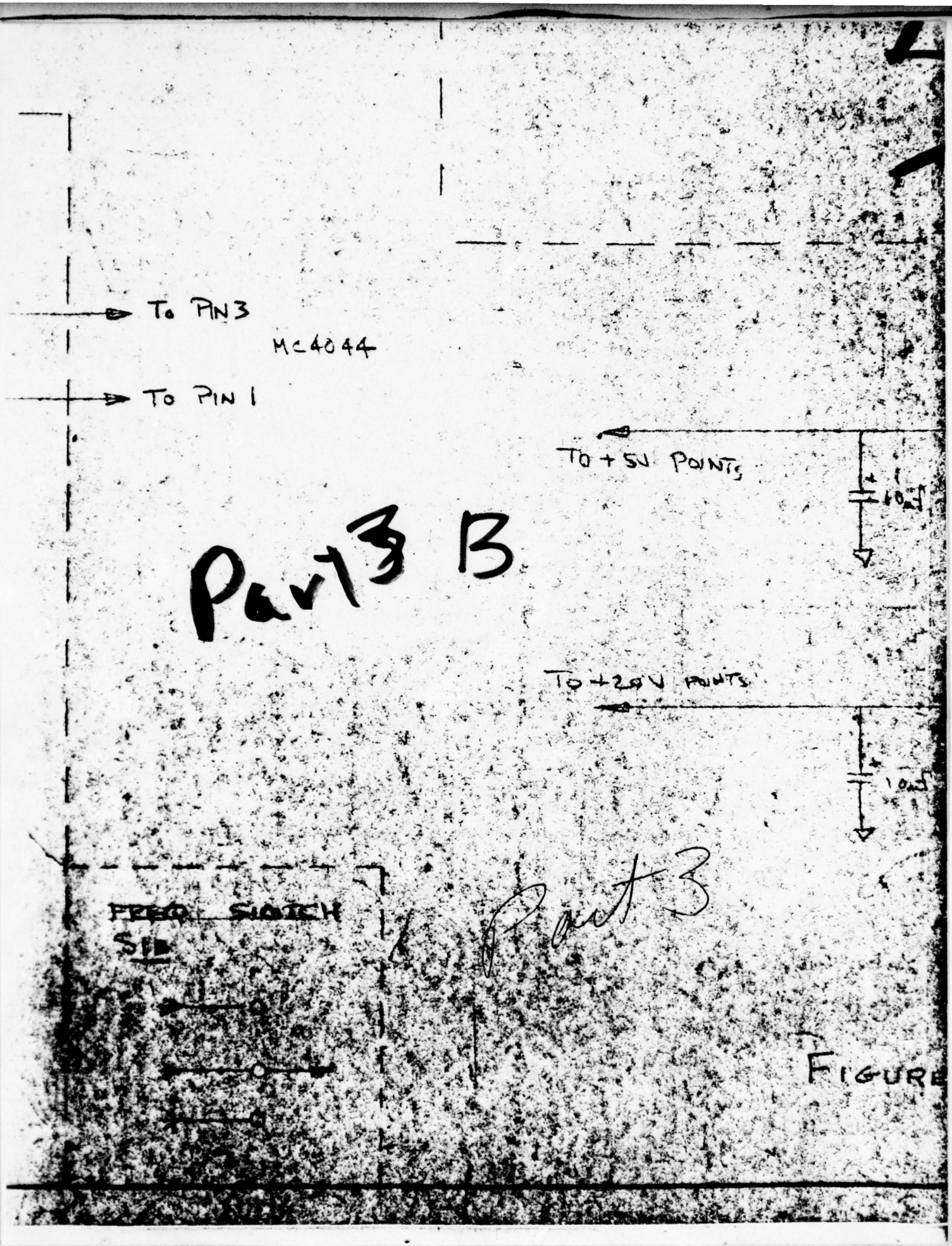


TO HI VCO

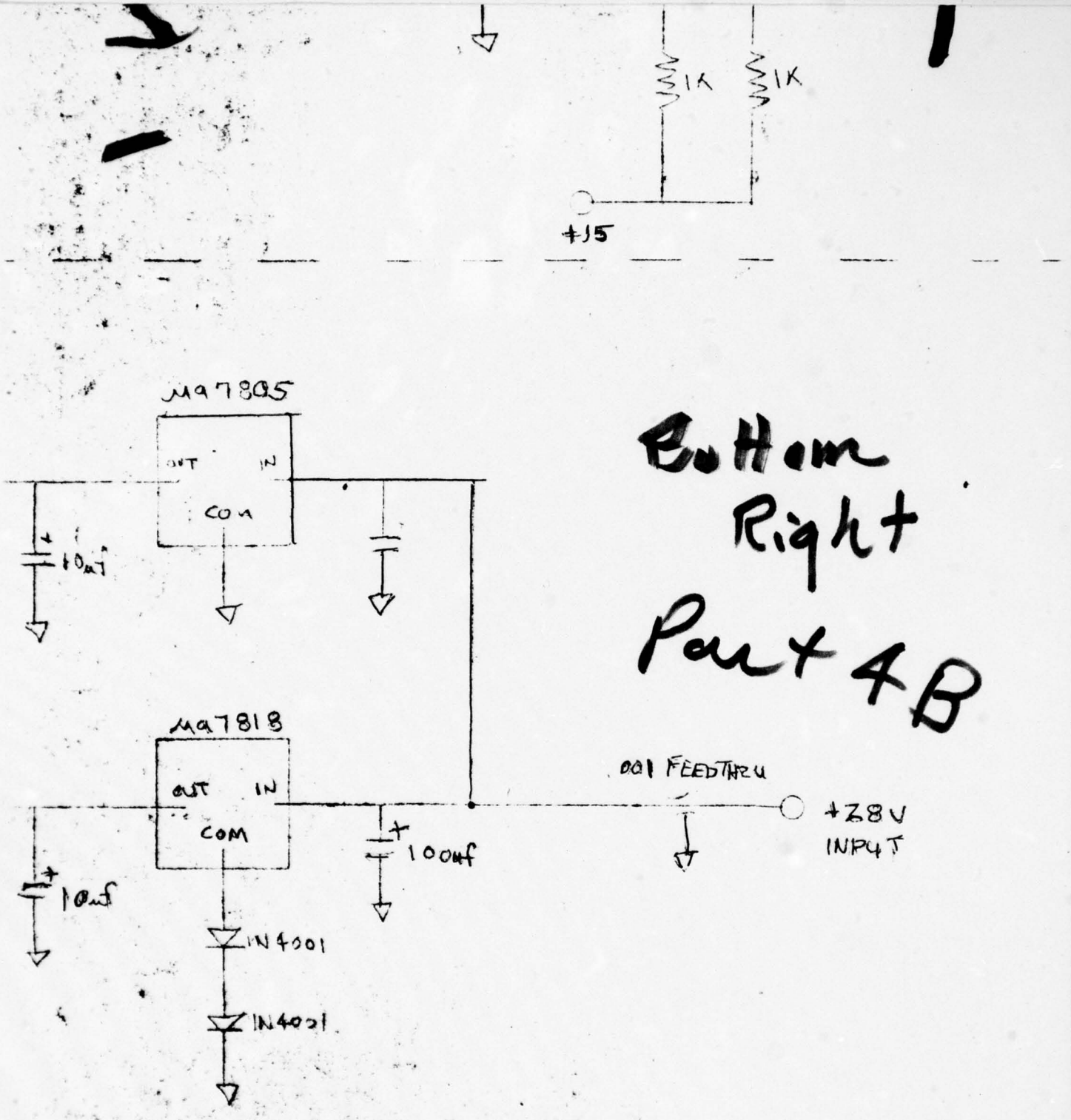

Part 4 T
+20
20K
5.6
.1uf
1meg
222
360
.1uf
4.7K
360
3.9
.1uf
4.7K
360
1 0uf
3.9 MEG
CA3100T
+5V
.1uf
MC4044
INPUT FROM COUNTER
SIG.
REF


1
COUNTER
÷601 ; 602
3 - 32
+5
27
1K
.1μF
XTAL
SAMPLE
INPUT
.001
MPS3640
33K
120
+5
.1μF
1K
74S133
Bottom
Left
Part 1B


5.6 uf
5.6 uF
BOX
.1uf
.1uf
+5
1
7490
÷100
7490
7490
120
3.3K
MPS 3640
.001
1.0K
.001
.001
27
+5
+5
.1
+5
.1uf
LO
HIGH
Part 2B


To PIN 3
MC4044
To PIN 1
To +5V POINTS
10μF
Part 3 B
To +20V POINTS
10μF
FREQ SWITCH
S1
Part 3

FIGURE



Bottom Right Part 4B

REVISIONS			NRL 1st L.O. PHASE LOCK UNIT		
NO.	DATE	BY			
1			UNITS 1, 2, 3 AND 4		
2					
3			DRAWN BY J.L	SCALE	MATERIAL
4			CHK'D	DATE	DRAWING NO.
5			TRACED	APP'D	

FIGURE 19

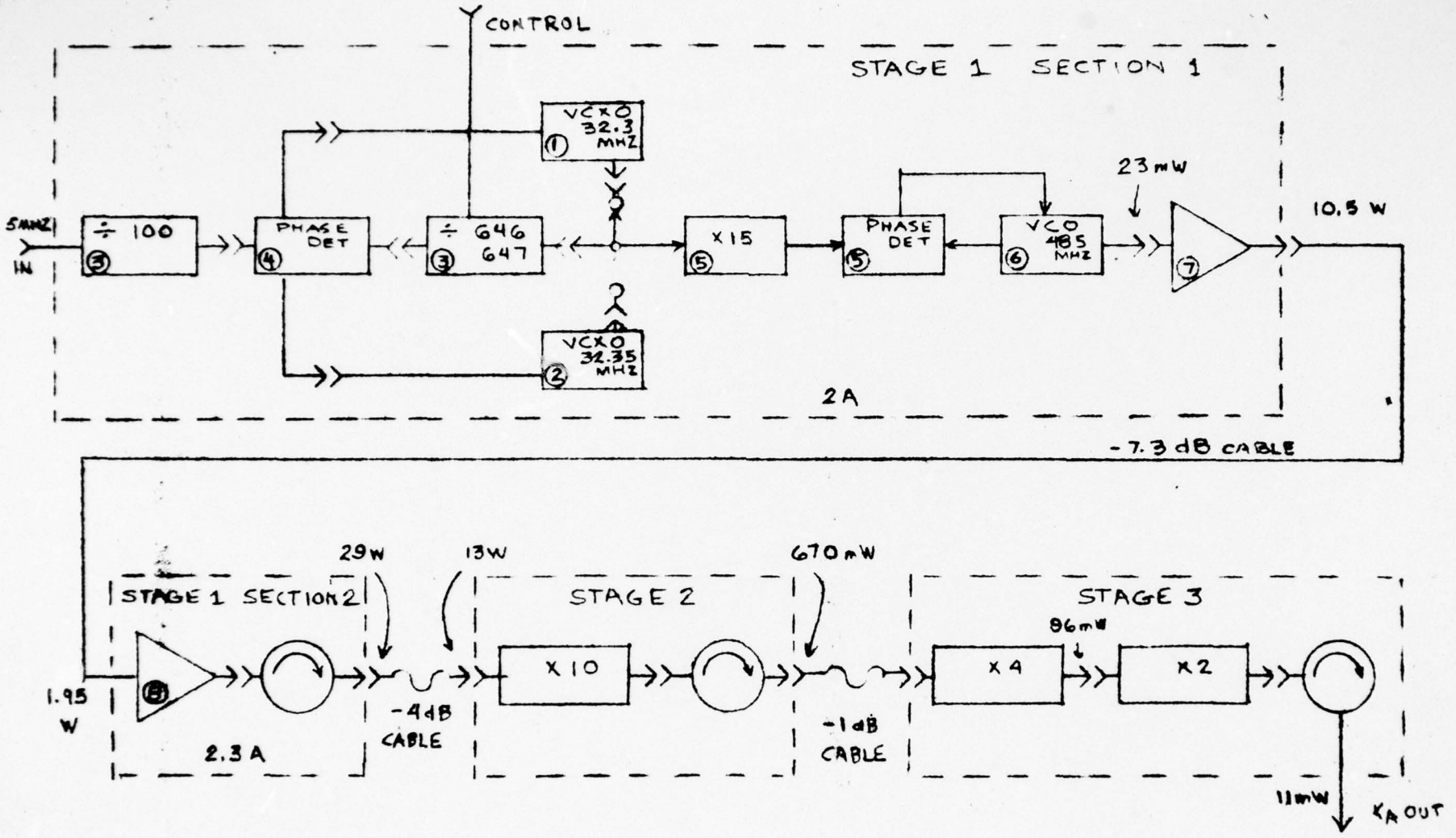
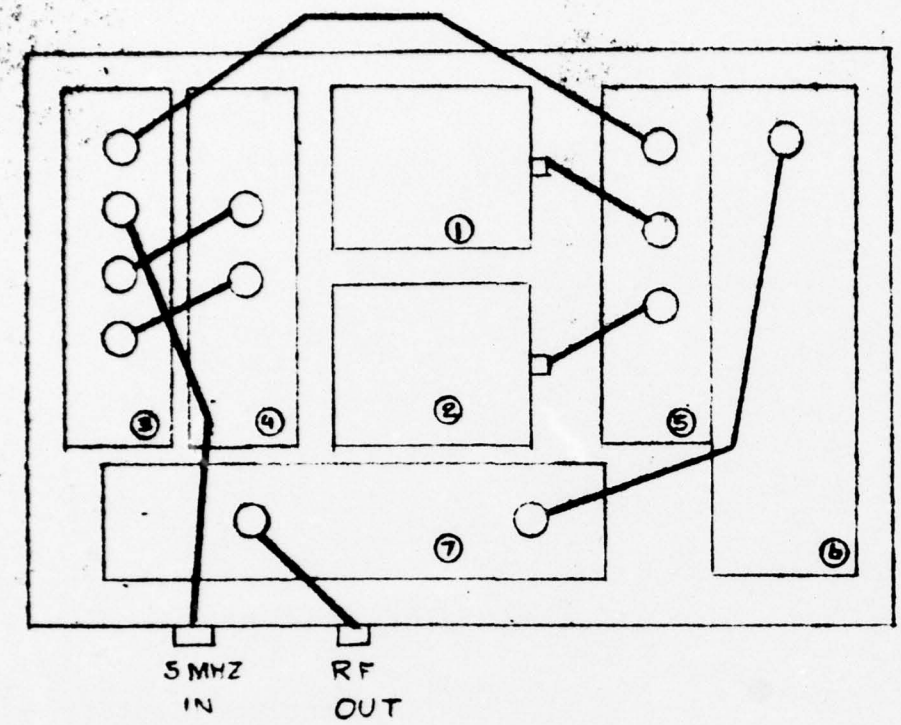


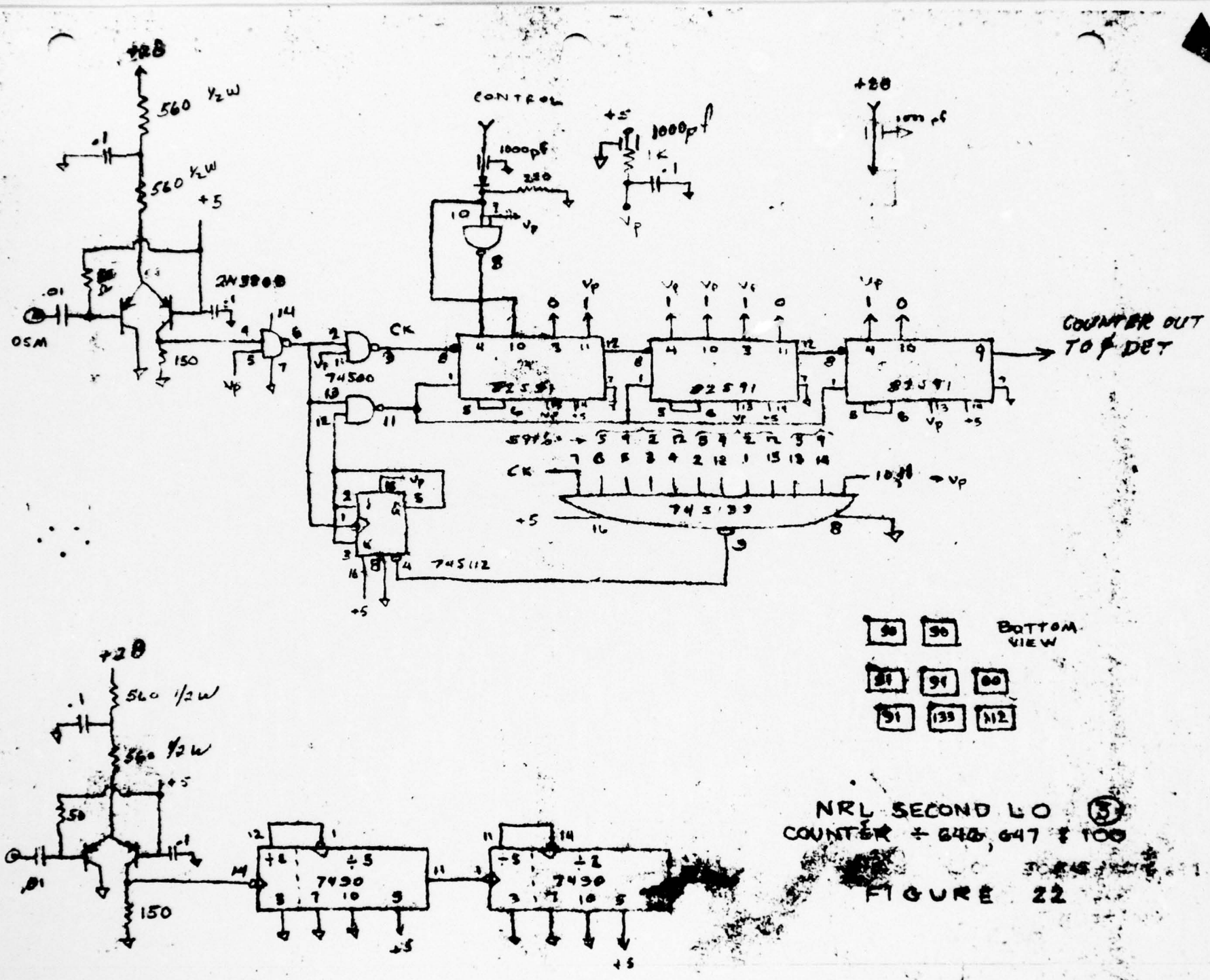
FIGURE 20

NRL 2ND LO



NRL 2ND LO
STAGE 1 SECTION 1
(BOTTOM VIEW)

FIGURE 21



NRL SECOND LO (3)
COUNTER ÷ 640, 647 & 100

FIGURE 22

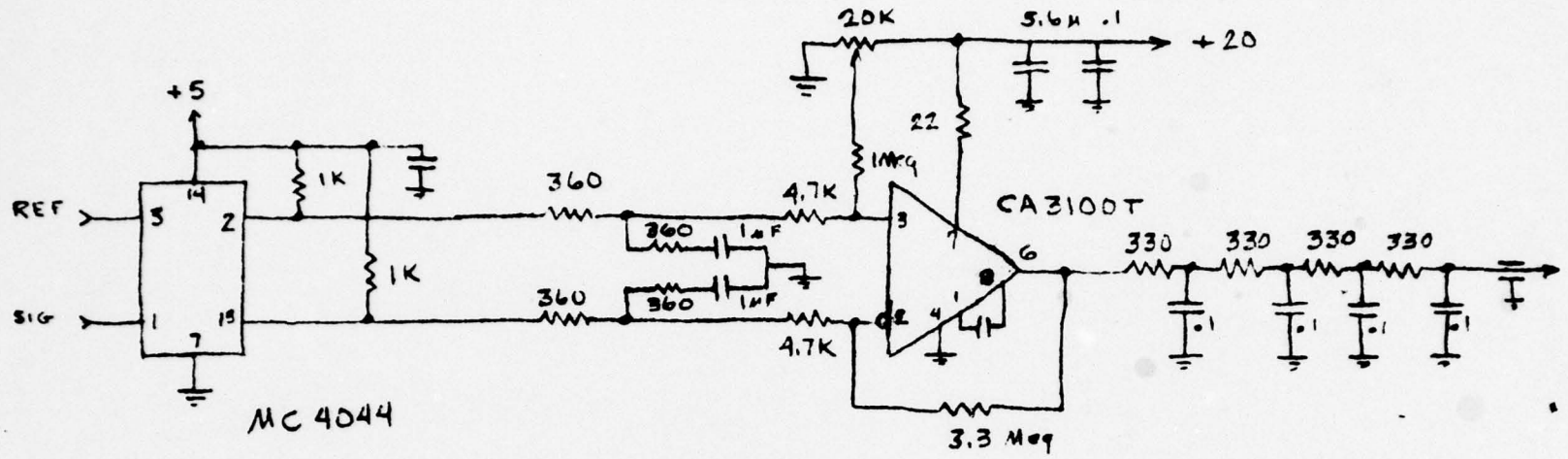


FIGURE 23

NRL SECOND LO (4)
50KHZ PHASE DETECTOR

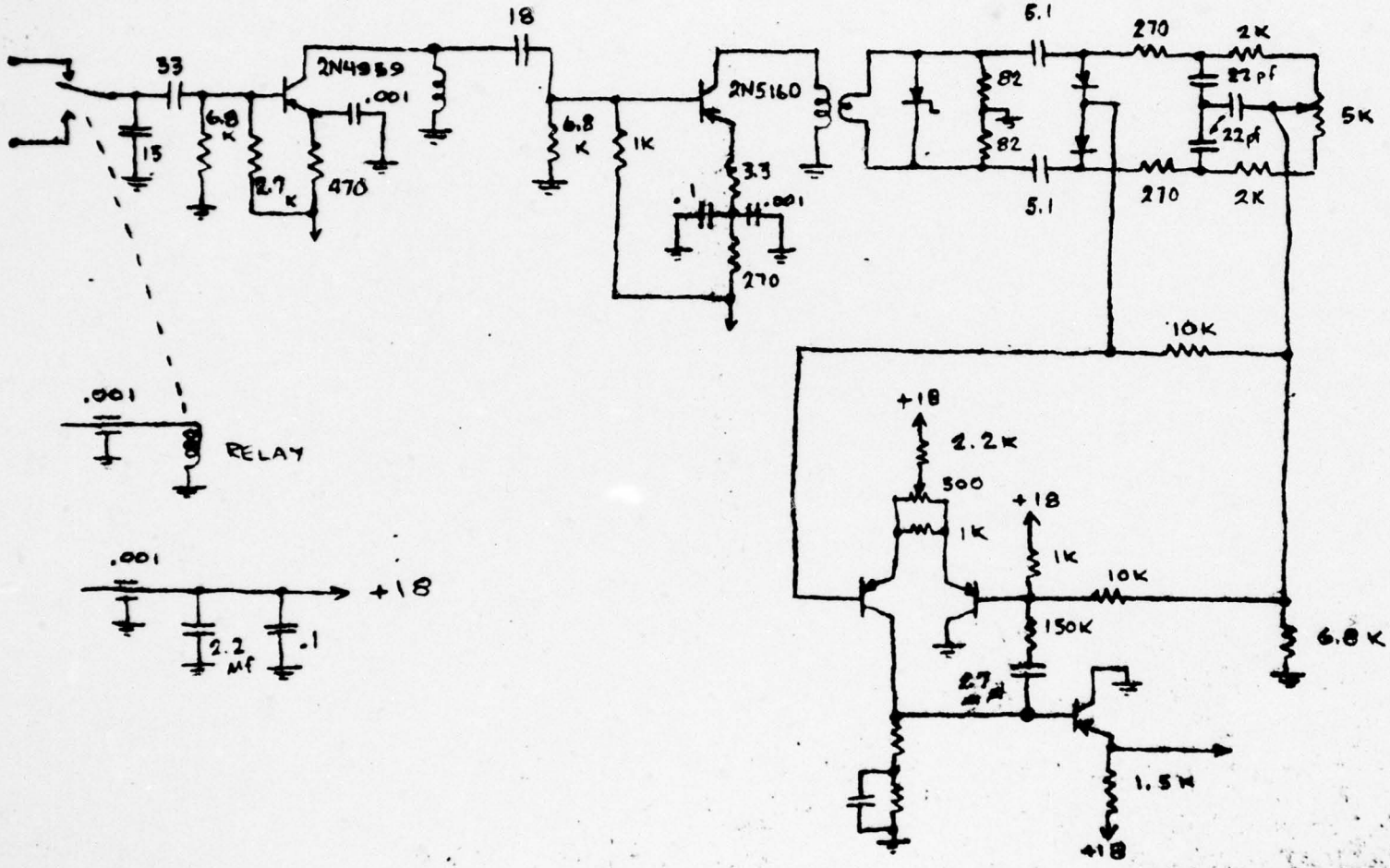


FIGURE 24

NRL RECORD 50
COMP BOARD & DETECTOR

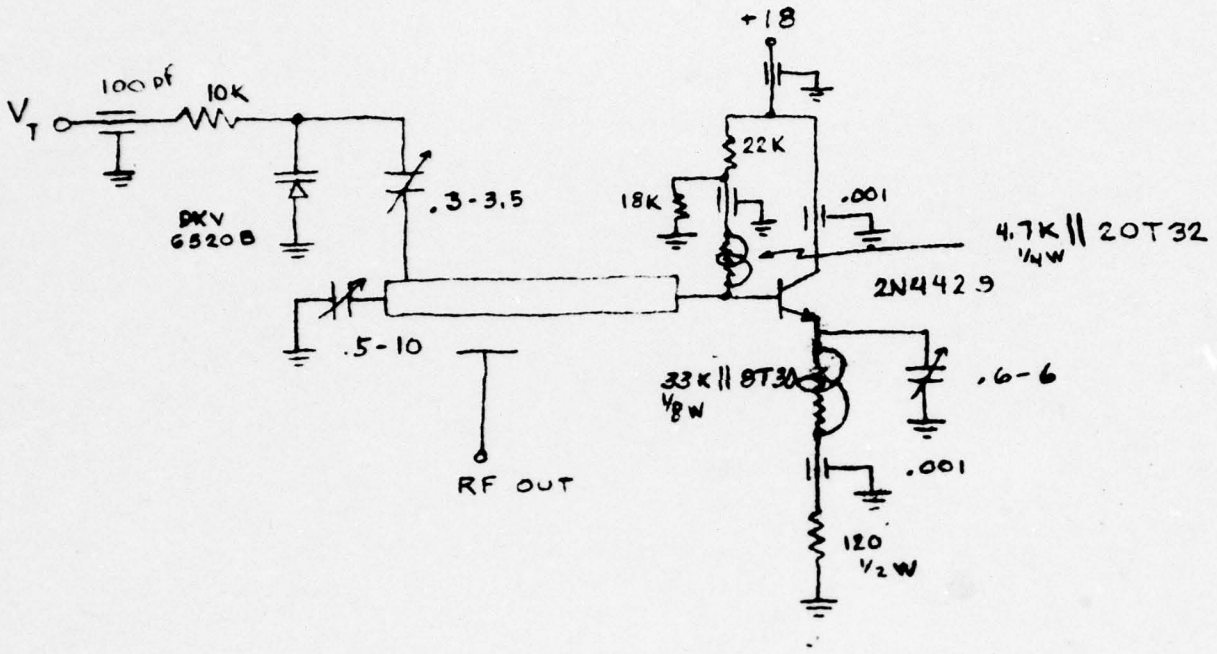
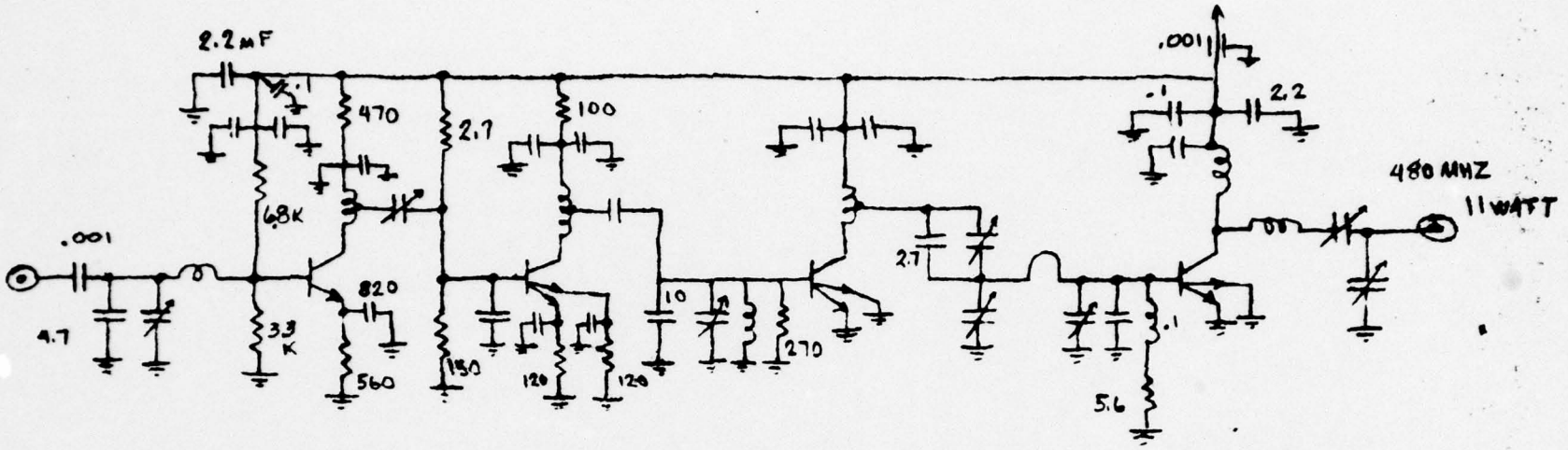


FIGURE 25

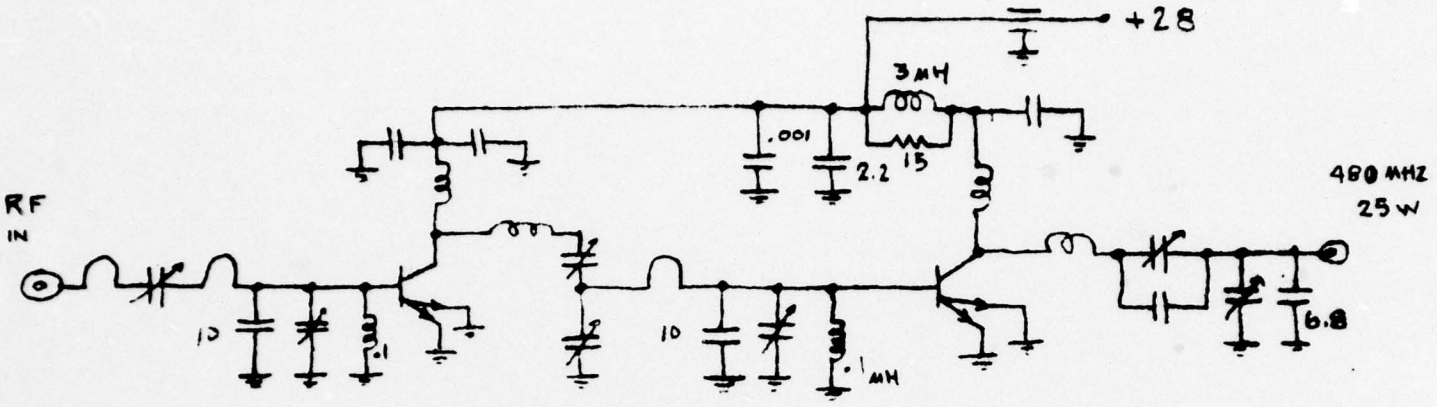
NRL SECOND LO (6)
480 MHZ CAVITY OSCILLATOR



ALL UNMARKED BYPASS 820 PF
ALL TRIMMERS 8. - 10 PF

FIGURE 26

NRL SECOND LO (7)
480 MHZ FIRST AMPLIFIER



C12-28

C25-28

FIGURE 27

NRL SECOND LO ⑧
480 MHZ POWER AMPLIFIER

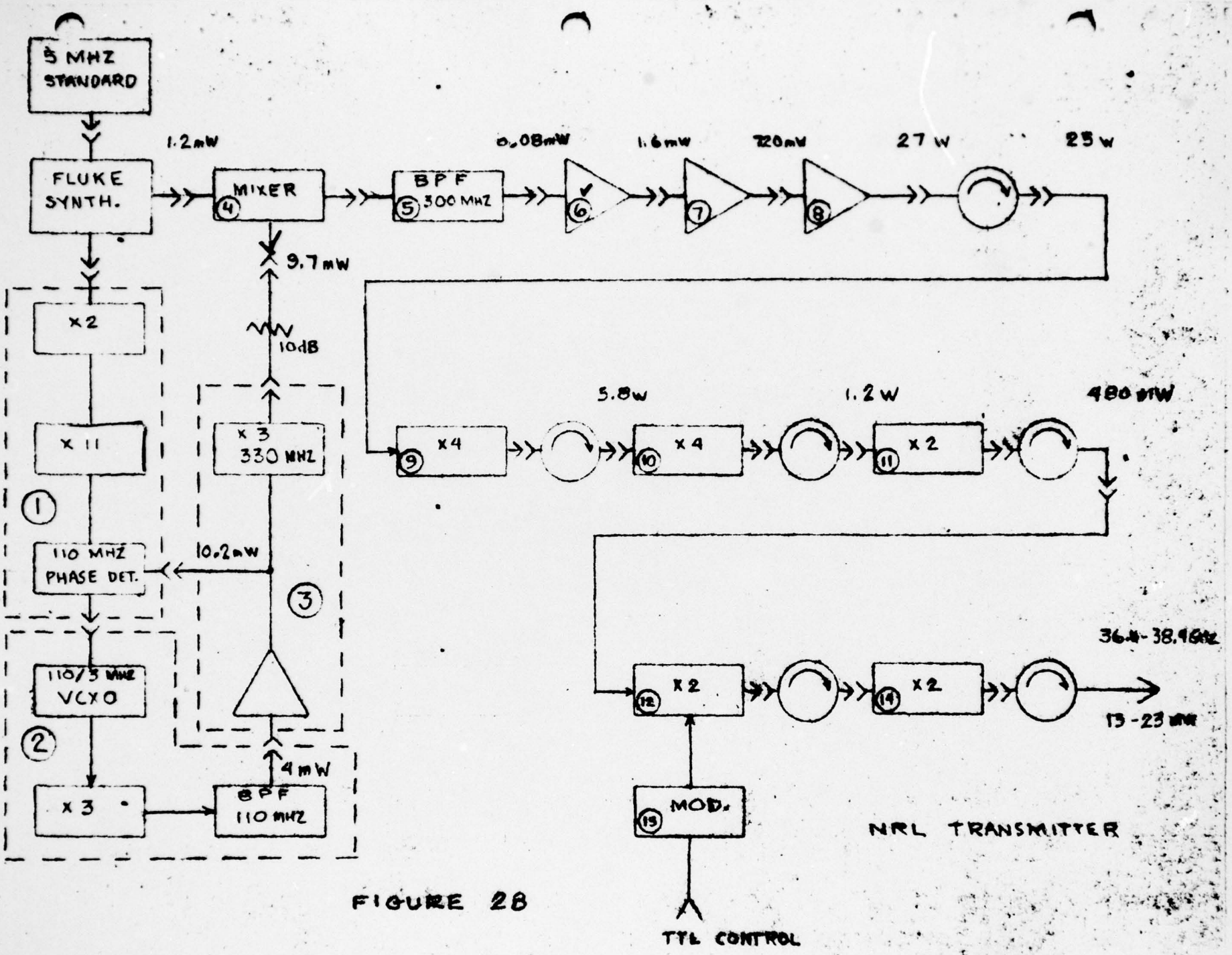
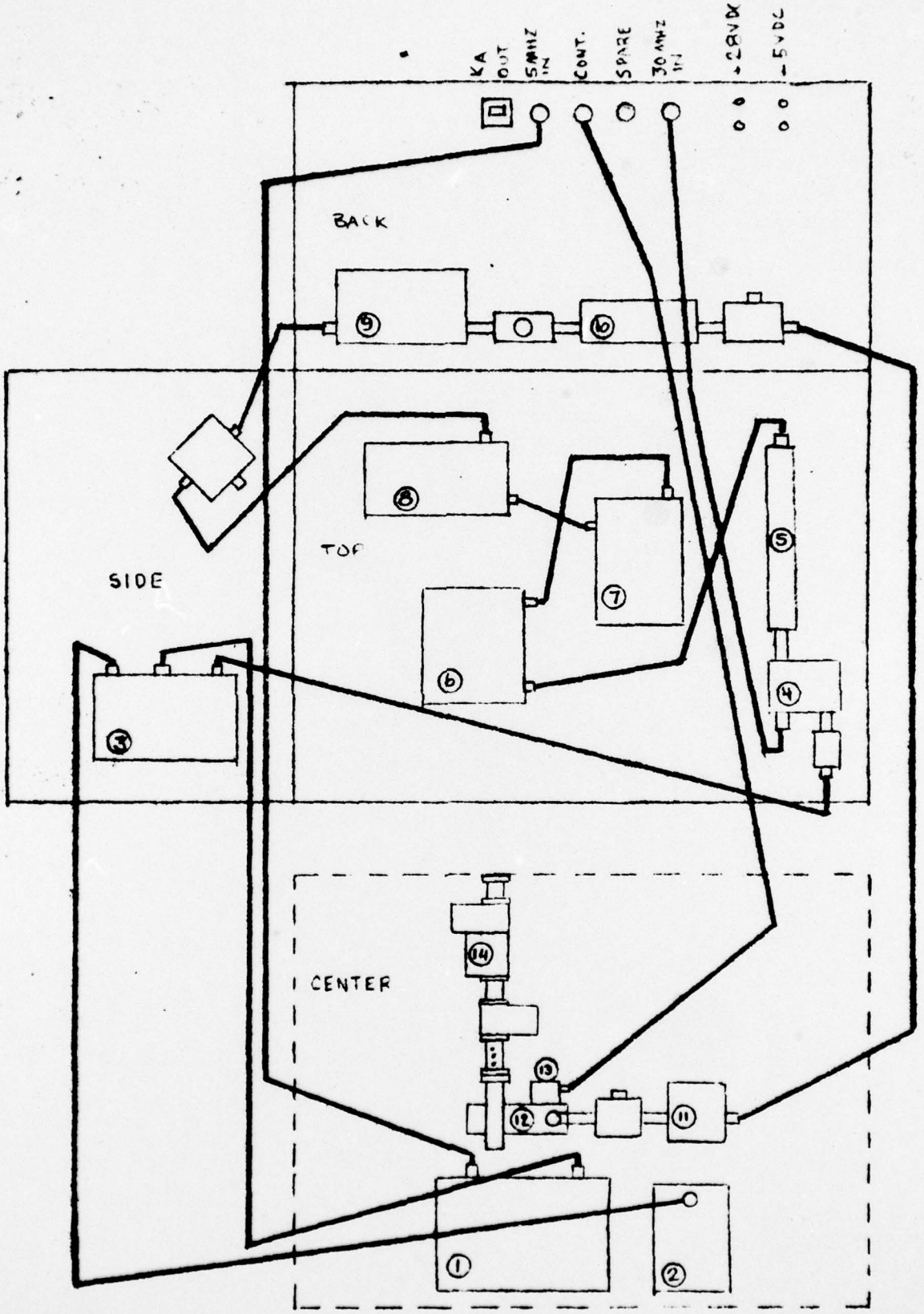

5 MHZ STANDARD
FLUKE SYNTH.
1.2mW
MIXER
4
BPF 300 MHZ
5
0.08mW
6
1.6mW
7
720mW
8
27 W
25 W
9.7mW
10dB
x2
x11
x3 330 MHZ
1
110 MHZ PHASE DET.
10.2mW
3
110/3 MHZ VCXO
2
4mW
x3
BPF 110 MHZ
5.8W
x4
9
x4
10
1.2W
x2
11
480 mW
x2
12
x2
14
36.4-38.4GHz
13-23 mW
MOD.
13
TTL CONTROL
NRL TRANSMITTER

FIGURE 28



NRL TRANSMITTER
(VIEWED FROM BOTTOM)

FIGURE 29

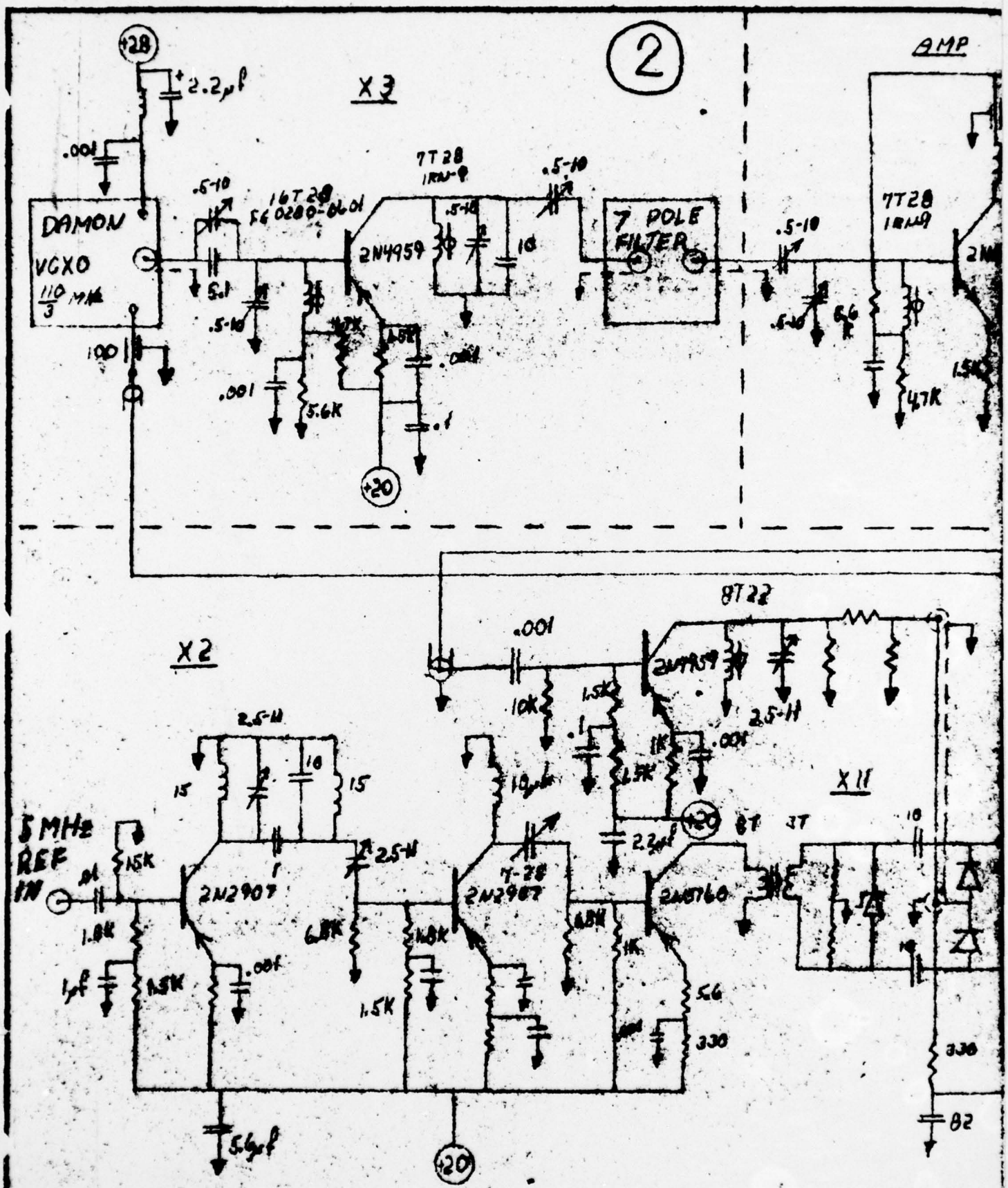
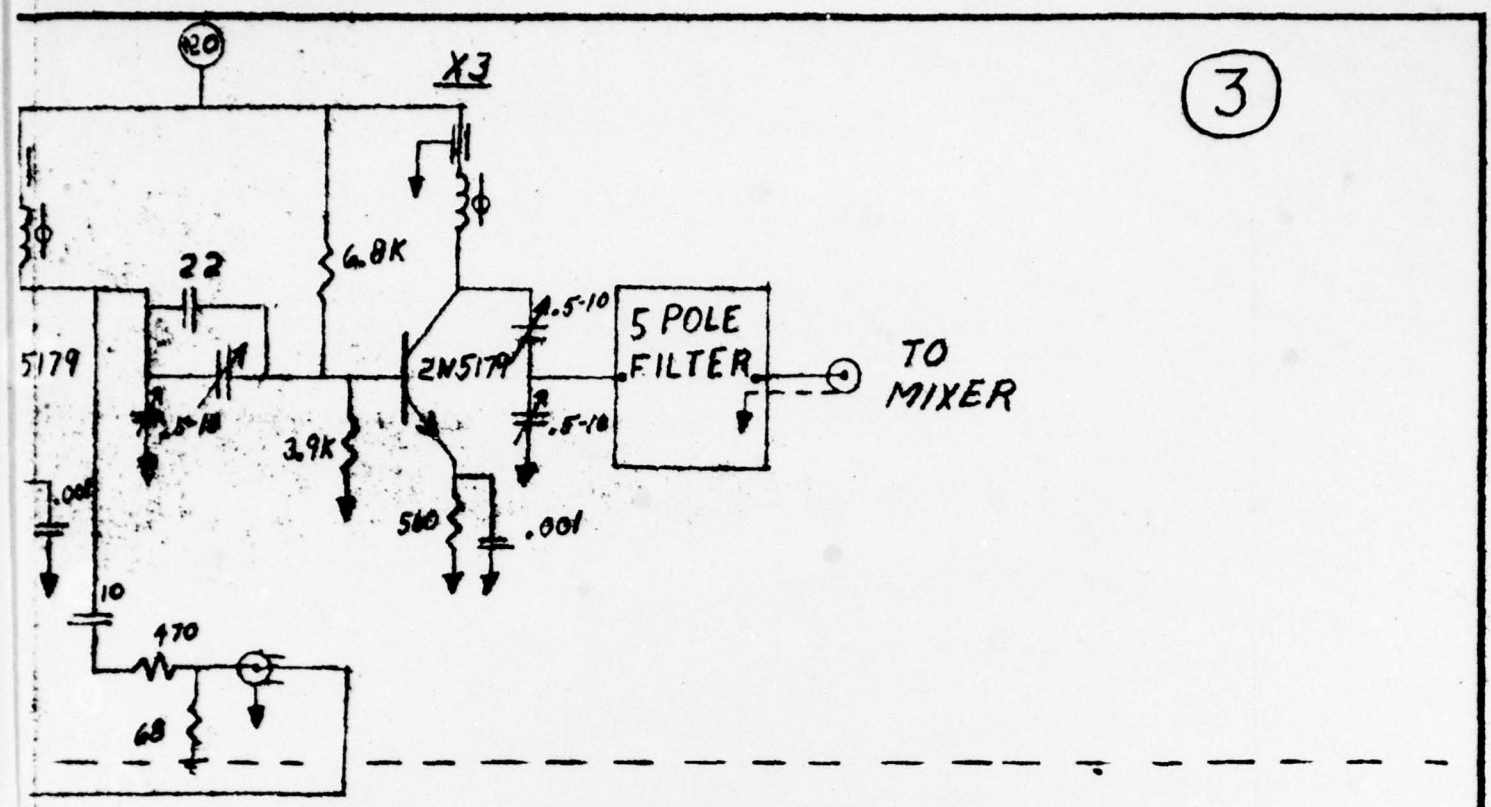
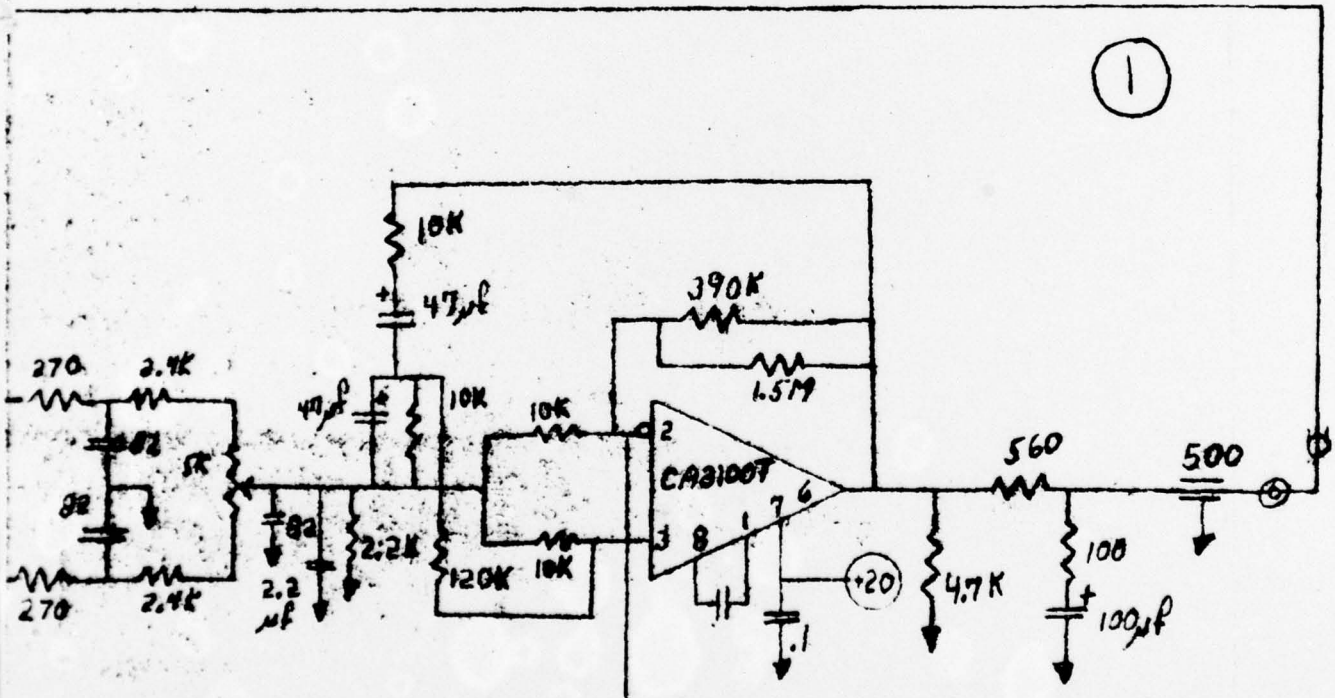


Figure 30 left





REVISIONS		
NO.	DATE	BY
1		
2		
3		
4		
5		

NRL TRANSMITTER, TRIPLER / PHASE DETECTOR

CIRCUITS ① ② AND ③

DRAWN BY G GLAUSER	SCALE —	MATERIAL
CHE'D	DATE 2-10-75	DRAWING NO
TRACED	APP'D	

FIGURE 30 right

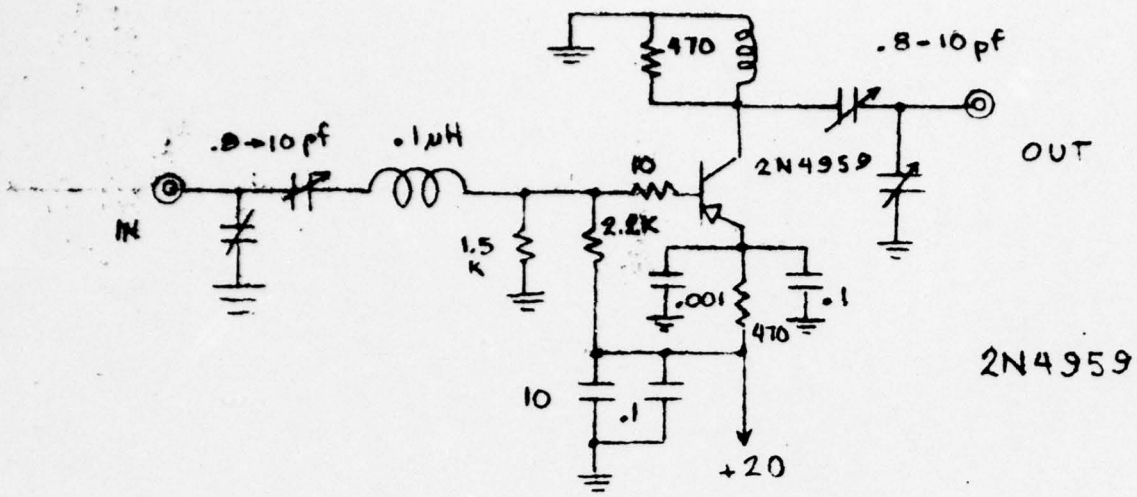
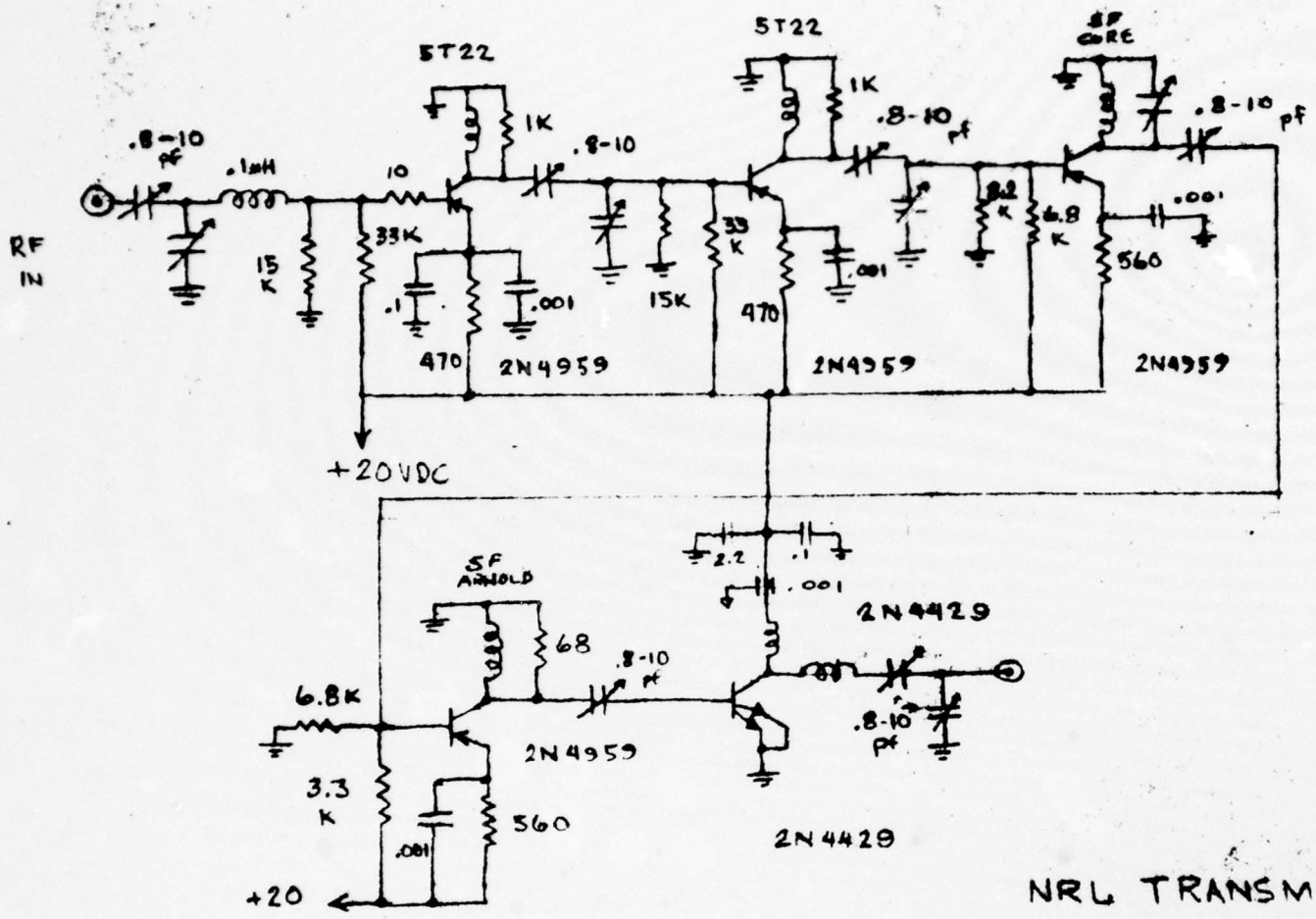


FIGURE 31

NRL TRANSMITTER UNIT (6)
300 MHZ PREAMP



NRL TRANSMITTER (7)

300 MHZ MAIN AMP

FIGURE 32

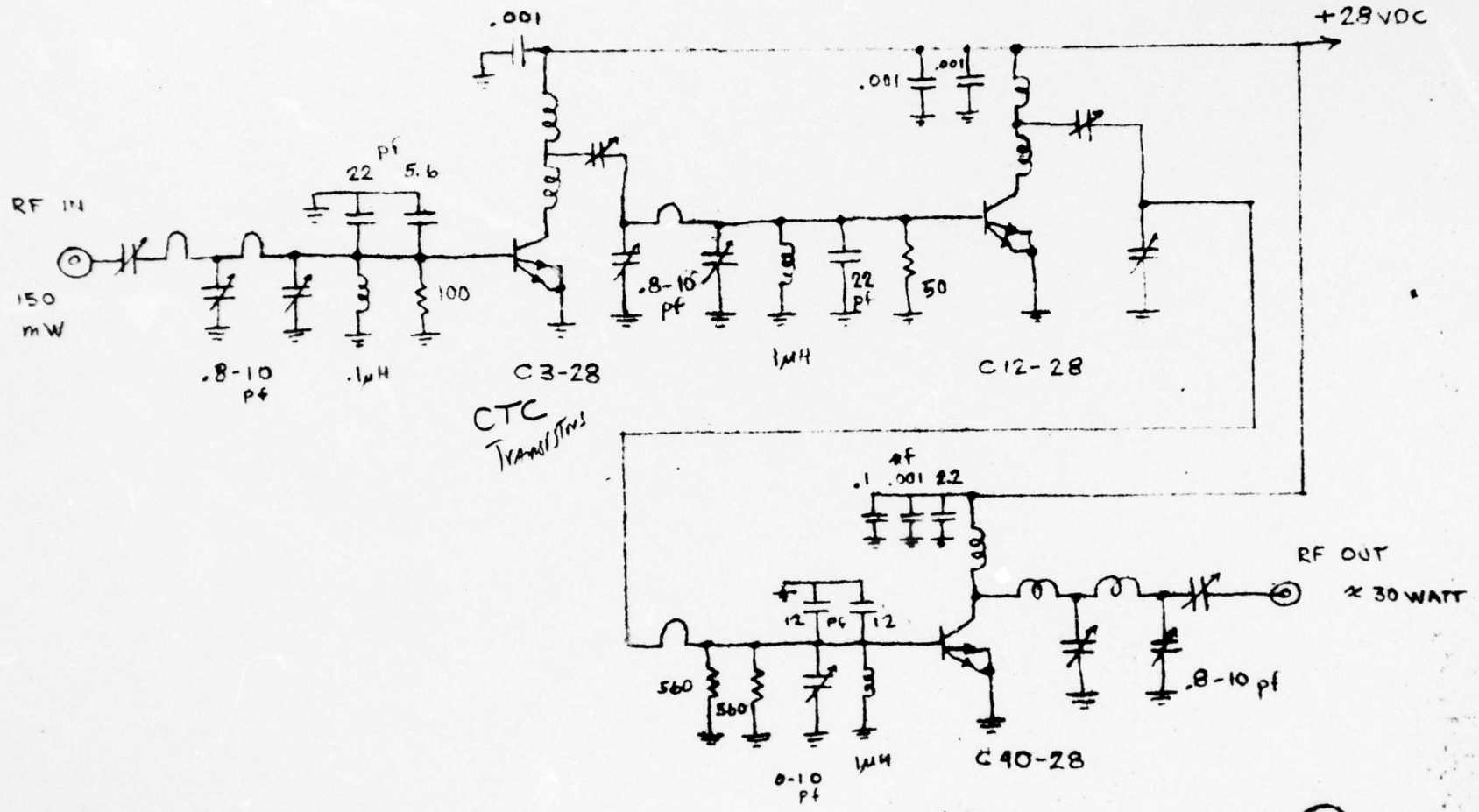


FIGURE 33

NRL TRANSMITTER
300 MHZ POWER AMP

(8)

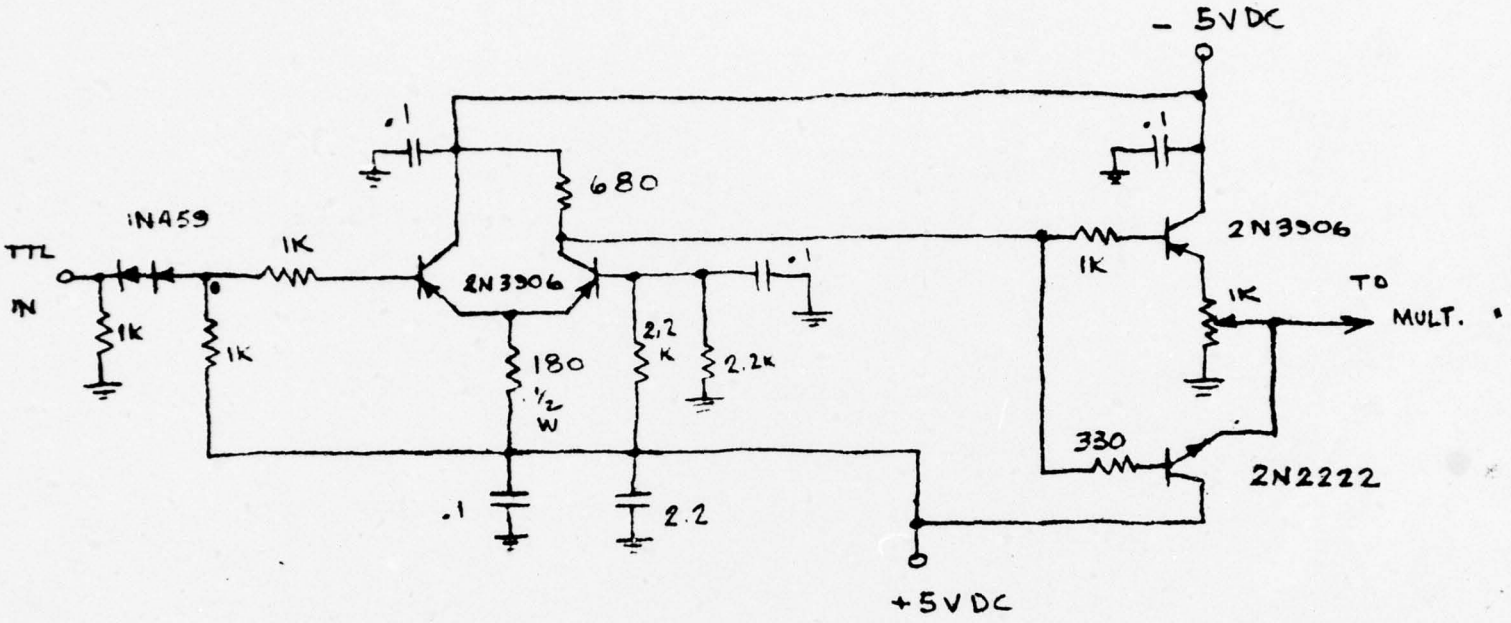


FIGURE 34

NRL TRANSMITTER (13)
CARRIER SWITCH