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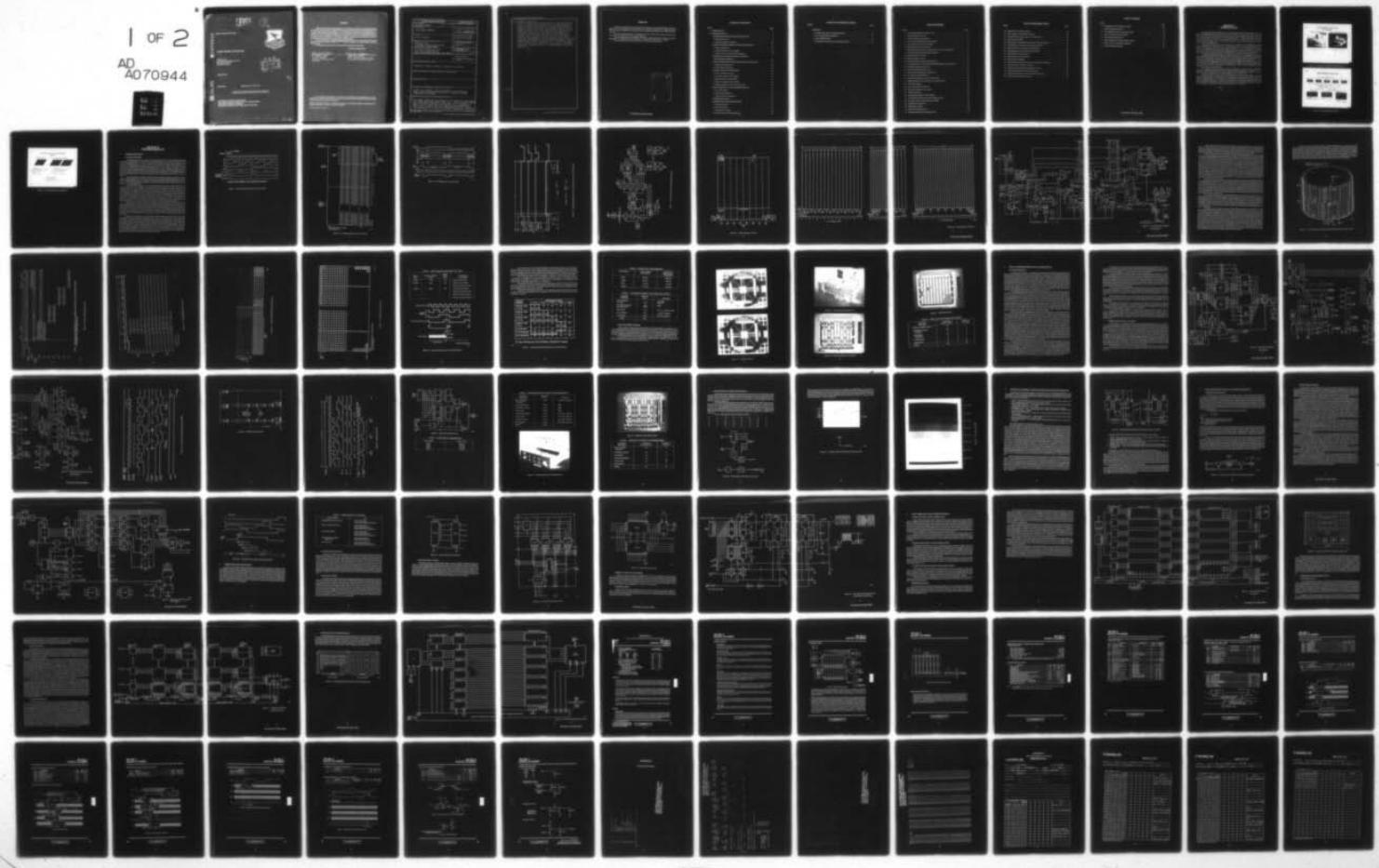

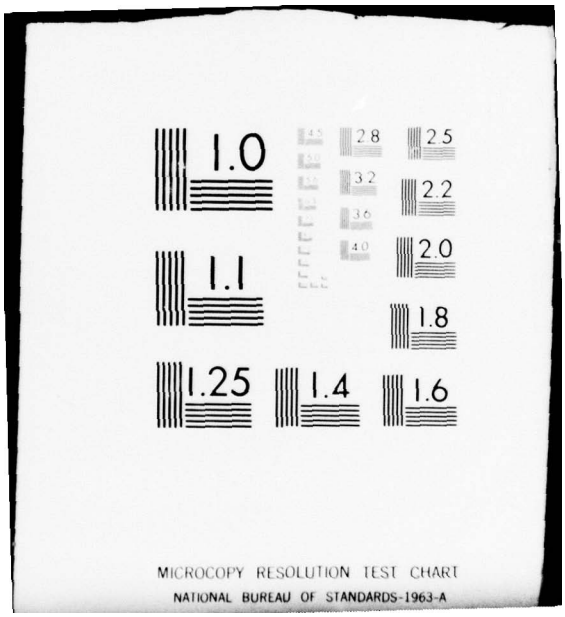
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VIDEO MEMORY MODULES

Motorola, Inc.
Government Electronics Division
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Final Report

September 1977 - May 1978

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This technical report has been reviewed and is approved for publication.

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This report summarizes the results of the exploratory development of a video frame store memory which can a) lower the sensor frame rate to provide increased A/J protection, and b) refresh a TV monitor at the normal rate while operating at reduced frame rates. Also, a similar unit for second-generation FLIR systems was investigated to a) freeze the display momentarily (continued)

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20. ABSTRACT (continued)
to give an observer additional time to search for details, and b) to improve system sensitivity for the detection of fixed or slowly moving objects by integrating successive frames of video as the image is displayed. This effort is being conducted in parallel with investigations at AFAL to develop a low-cost A/J video data link for advanced RPV's and guided missiles. This exploratory development was divided into two phases. The first phase was devoted to circuit design and module definition. The second phase involved the brassboard fabrication and testing of two prototype video memories for RPV bandwidth reduction systems employing 64K digital CCD memories for the primary frame store function. The primary goal was to realize the imaging system at a minimum of memory cost, size, weight and power dissipation through the use of a common modular packaging approach.

PREFACE

This report was prepared by the Engineering staff of the Government Electronics Division of Motorola, Inc. for the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, under Air Force Contract No. F33615-77-C-1142. The work was performed at Motorola, Inc. GED, Scottsdale, Arizona.

The work, performed between 1 September 1977 and 15 May 1978, was directed for the Air Force by Dr. R. A. Belt, Air Force Avionics Laboratory.

The following persons participated in the research, module fabrication, testing, or writing of this report: J. E. Greenwood, Dr. G. R. Kaelin, J. E. Bjornholt, D. Hall, and L. A. Hopper.

This technical report has been reviewed and is approved for publication.

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SECTION I
INTRODUCTION

This final report describes Motorola Inc. Government Electronics Division's efforts on a nine month developmental program of video memory systems. These investigations involved a video frame store memory for providing increased anti-jam (A/J) protection by lowering sensor frame rates, and a second-generation forward looking infrared sensor (FLIR) system to improve sensitivity by integrating successive frames of video. The critical design requirement of both systems was to minimize memory cost, size, weight and power dissipation to achieve a practical system for remotely piloted vehicle (RPV) or battlefield use.

This two-part developmental effort consisted of a circuit design and module definition phase followed by the brassboard fabrication of two prototype video memories for RPV bandwidth reduction systems. The program utilized 64k digital charge coupled device (CCD) memories for the primary frame store function along with large scale integrated (LSI) logic devices for minimizing control and input/output (I/O) functions. The modular packaging approach was applied to the two brassboard units so that each unique module might later be reduced to a high-density hybrid submodule.

A brassboard Frame Rate Buffer unit (FRB) was fabricated to 1) digitize the serial analog video output from a standard 525 line National Television Systems Committee (NTSC) compatible TV sensor into 512 samples/line at 6 bits per sample, 2) reformat the data into 8x8 pixel blocks for serial outputting, and 3) lower the video frame rate from the standard 30 frames/second to either 7½, 3¾ or 1⅞ frames/second. A brassboard Display Refresh Memory unit (DRM) was fabricated to perform the inverse function of the FRB. That is, it continuously updates a display monitor while simultaneously accepting frame rate reduced video data from the FRB. Figure 1 shows the two brassboard units with a summary of pertinent characteristics.

A Frame Freeze/Time Integration unit was also designed to 1) snatch a frame of video, digitize it, store it, and then read it out continuously through a digital-to-analog (D/A) converter to a standard 525 line NTSC compatible RS-170 format display, and 2) add together successive frames on a pixel-for-pixel basis while the sum is continuously displayed on a TV monitor.

These unit designs are partitioned into discrete functional modules. This modular packaging approach allows any unit to be fabricated around these basic functional blocks. Figure 2 shows the common modules defined for this program with a breakdown of module utilization for each unit. These functional building blocks can subsequently be reduced to a high density form of hybrids or full water LSI. Figure 3 illustrates a conceptual configuration of the Frame Rate Buffer and Display Refresh Memory if implemented with the high density functional modules.

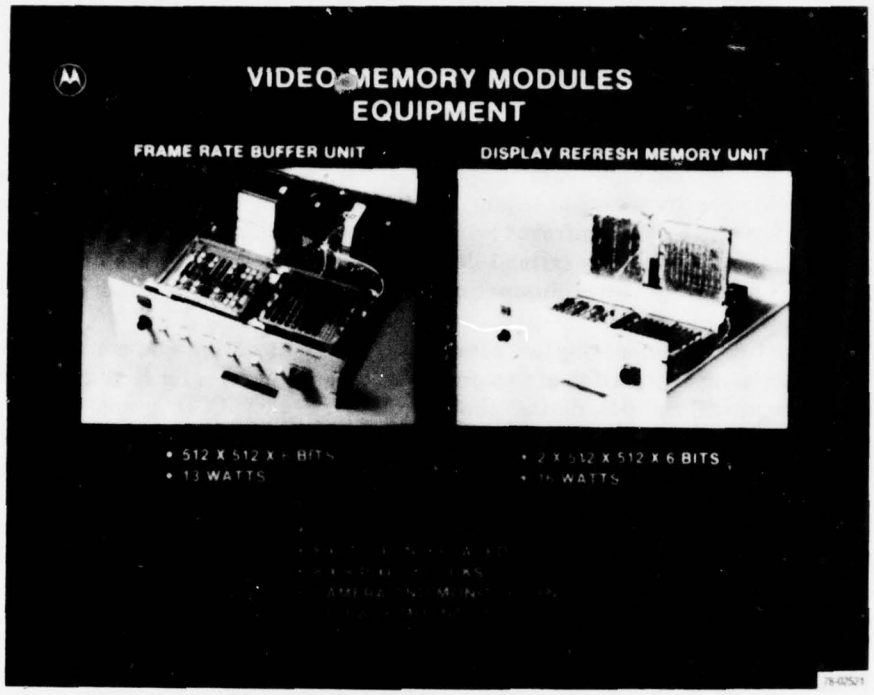


Figure 1. Video Memory Modules Brassboard Units

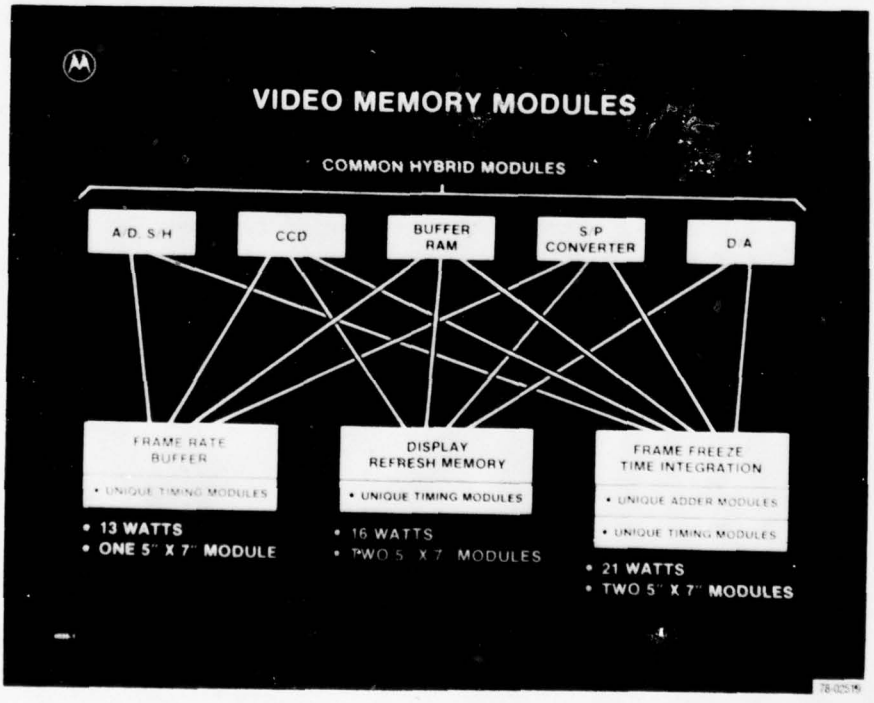


Figure 2. Common Module Definition

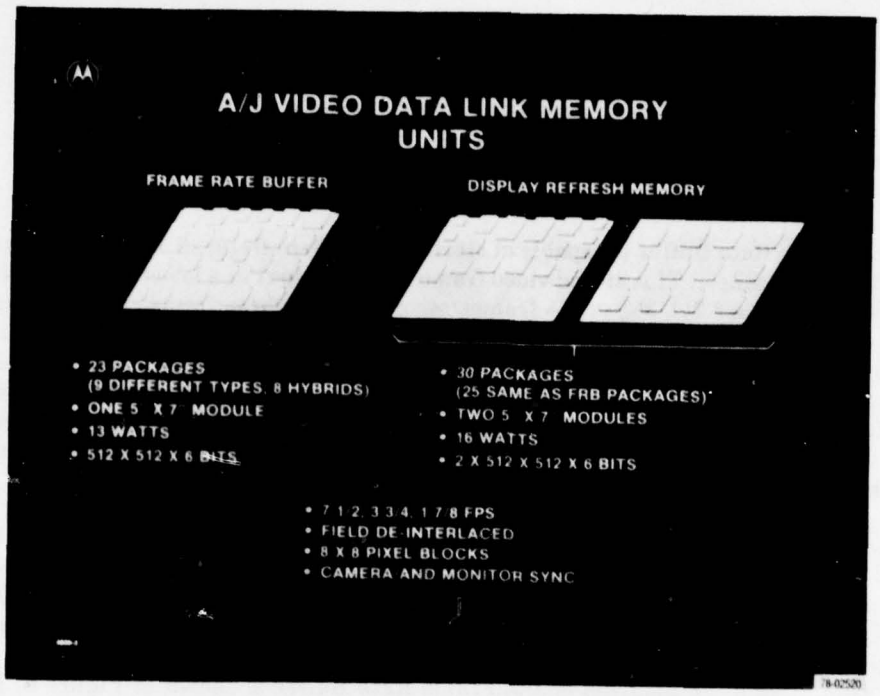


Figure 3. Conceptual Hybrid Configuration

SECTION II
PROGRAM RESULTS

1. FRAME RATE BUFFER

a. Technical Operation

The Frame Rate Buffer is capable of storing a complete frame of video from a standard 525 line NTSC compatible sensor. This stored video frame will be output at a lower rate from the standard 30 frames/second to either 7½, 3¾, or 1⅞ frames/second. These three frame rates correspond to the output of one complete frame of video every 4, 8, or 16 real time TV frames. This output frame, or active frame, is defined for each frame rate in Figure 4. Every active frame will consist of 512 pixels per horizontal line by 512 horizontal lines (256 lines from each field). The horizontal lines stored in each active frame are defined in Figure 5. The individual line numbers are Motorola designations but the relative timing of vertical drive, vertical blanking, and field index pulse are all NTSC standard. A timing diagram showing these signals and the location of the stored horizontal lines is given in Figure 6.

Every horizontal line consists of 512 active pixel elements which are stored in the CCD memory. These 512 pixels are taken from a horizontal line consisting of 640 total pixel time elements. The horizontal blanking, however, occupies 112 pixel time elements so that the 512 stored pixels represents ~97 percent of the remaining 528 active video pixel elements. Figure 7 defines the stored pixels from a given horizontal line.

A simplified block diagram of the Frame Rate Buffer is shown in Figure 8. The camera input goes through a video amplifier to set the proper gain and offset for the sample/hold (S/H) and A/D converter. The video is digitized into 6 bits per pixel of resolution and then changed from a 10-Mbps serial to a 2.5-Mbps four-bit parallel bus structure for storage in the CCDs. A master oscillator is included in the FRB to generate all internal timing signals and to generate proper synchronizing signals for the TV camera. Since the video from the camera is field oriented, the CCD memories will store the odd field data in the lower half of memory and the even field data in the upper half of memory. Two redundant buffer RAMs located at the CCD outputs are used to reformat the field oriented horizontal line data into 8 pixel x 8 pixel frame oriented data blocks. The buffer RAM output is converted back into a serial bit stream for outputting to the Display Refresh Memory.

The sequence by which a stored video frame is output is determined by pixel availability from the CCD memories. The output format of the FRB requires both odd and even field data, so a stored video frame cannot be output until the even field of that frame begins. Due to the serial nature of the CCD's, only certain portions of the stored frame are accessed during each rotation. The frame will, therefore, be output in vertical picture stripes with each stripe width being determined by the frame rate. Figure 9 shows the output sequence of a stored video frame for each required frame rate. A picture stripe will consequently take a complete real time TV field to be output from the Frame Rate Buffer.

A detailed block diagram of the Frame Rate Buffer is shown in Figure 10. The input video from the TV camera is digitized by a high-speed A/D converter. The 10-Msps A/D converter presently in the FRB is a combined monolithic/discrete module capable of outputting 6-bit parallel TTL data. All clock and interface circuitry around this S/H and A/D module are designed so that the Motorola proprietary 6-bit monolithic S/H and A/D may be added later. The digitized pixel output rate of the A/D is 10 Mbps. The maximum read/write data rate of the TI CCD's (part no. TMS 3064JL) is specified in the data sheet of Appendix A at 5 Mbps maximum. The input serial pixel rate of the A/D is, therefore, rate reduced through a serial to parallel converter to a four-bit parallel bus at a 2.5 Mbps pixel rate. This four-bit wide bus is the input to four CCDs at each bit per pixel for a total of 24 CCDs required to store a frame of video with this method of operation.

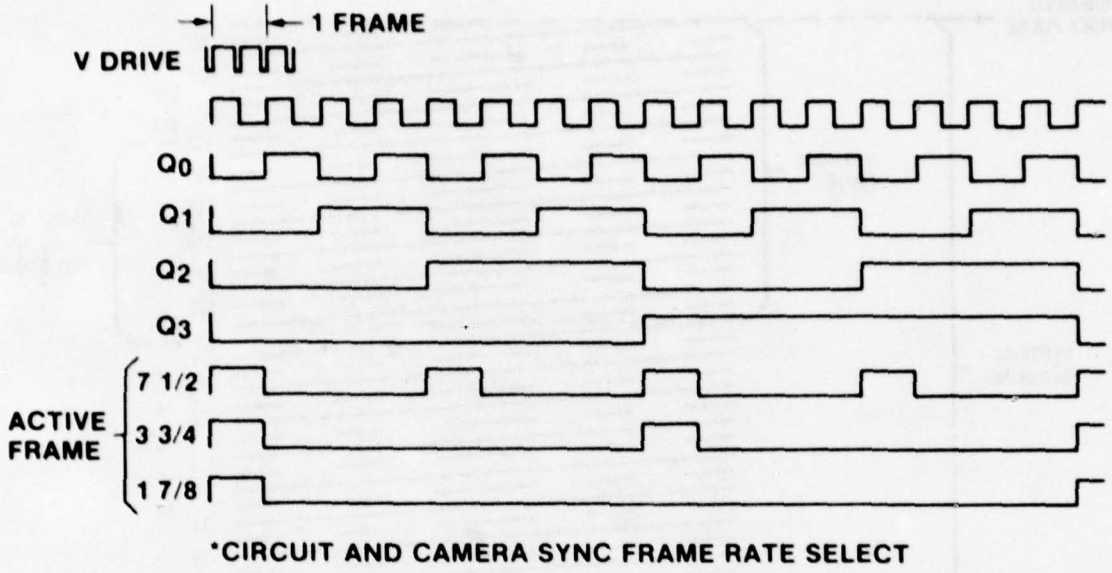


Figure 4. Active Frame Definition for all Frame Rates

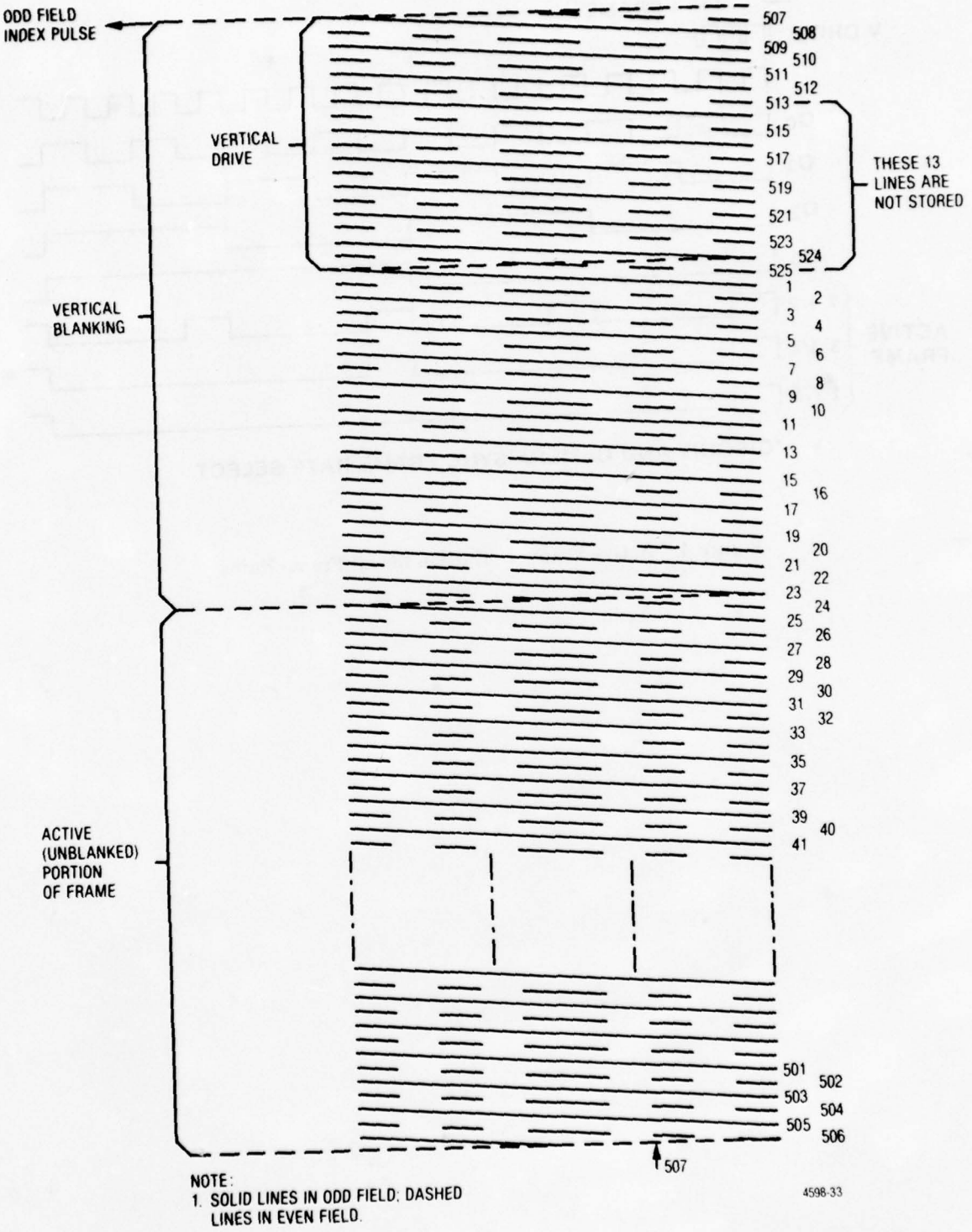


Figure 5. Line Number Definition for TV Frame

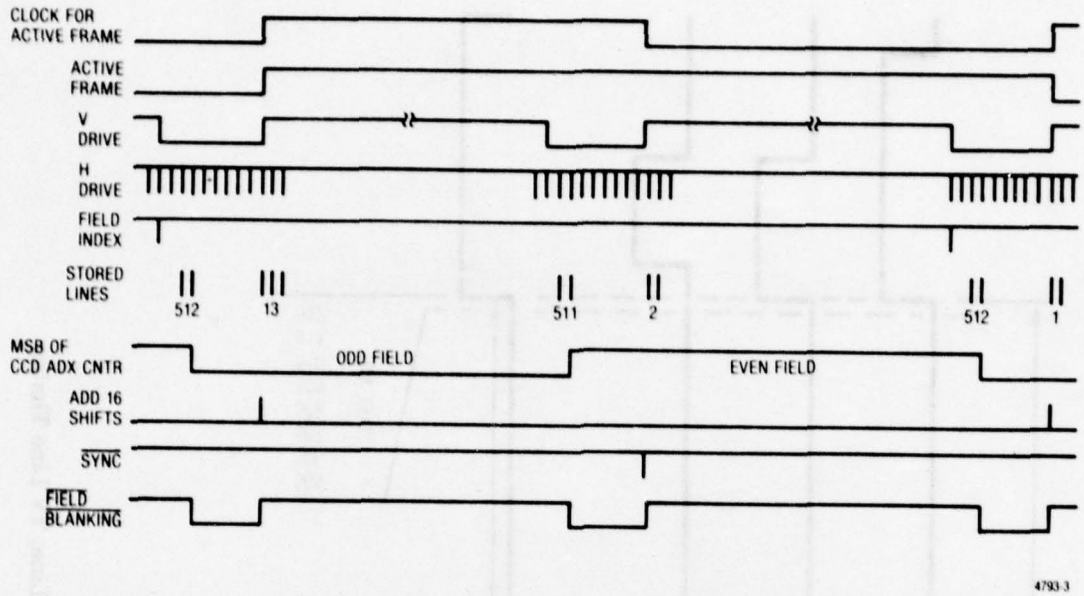
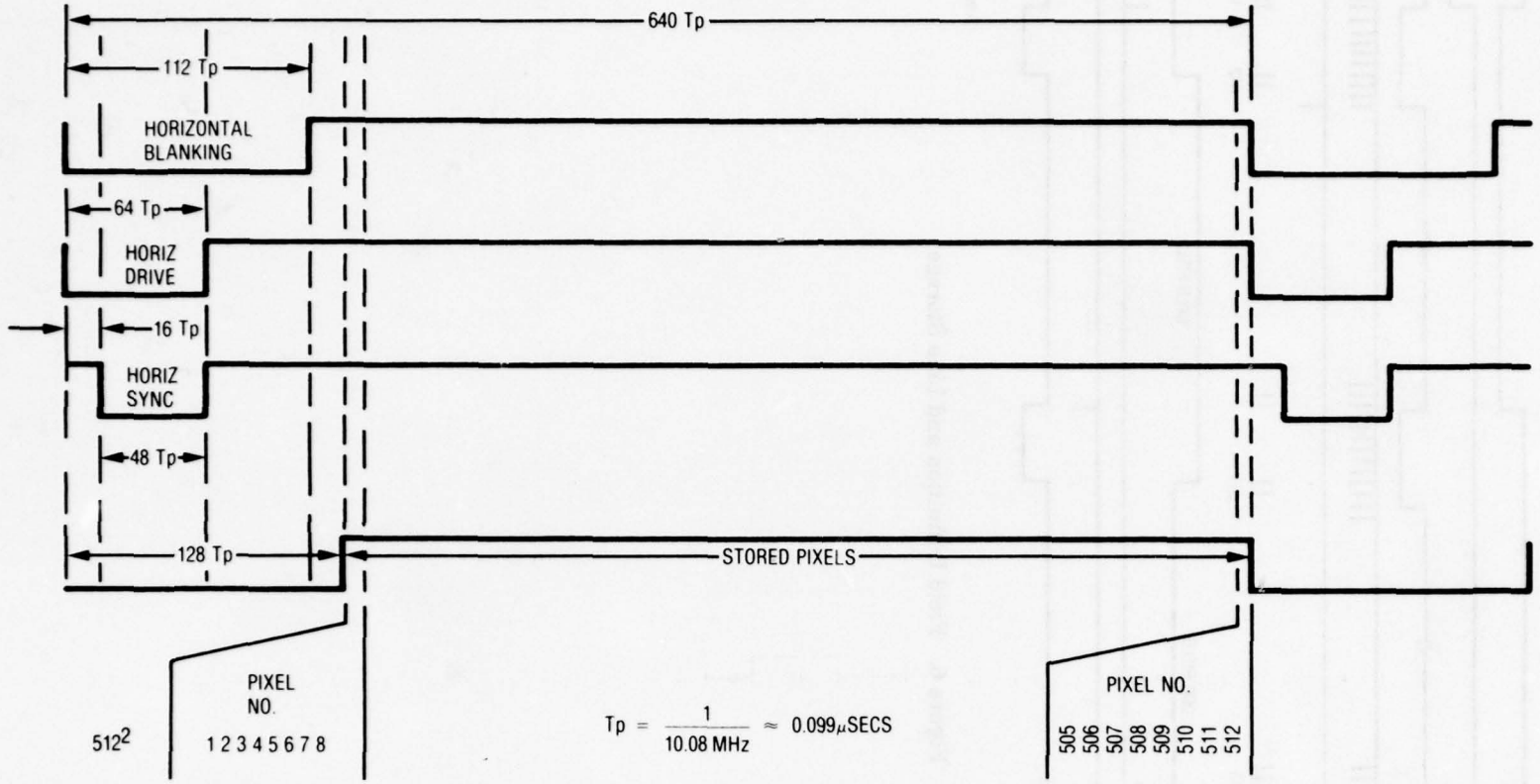


Figure 6. Field Definition and Line Storage



$$\text{HORIZONTAL LINE RATE} = \frac{10.08\ \text{MHz}}{640} = 15750\ \text{Hz}$$

Figure 7. Pixel Number Definition for a Horizontal TV Line; TV Line Timing

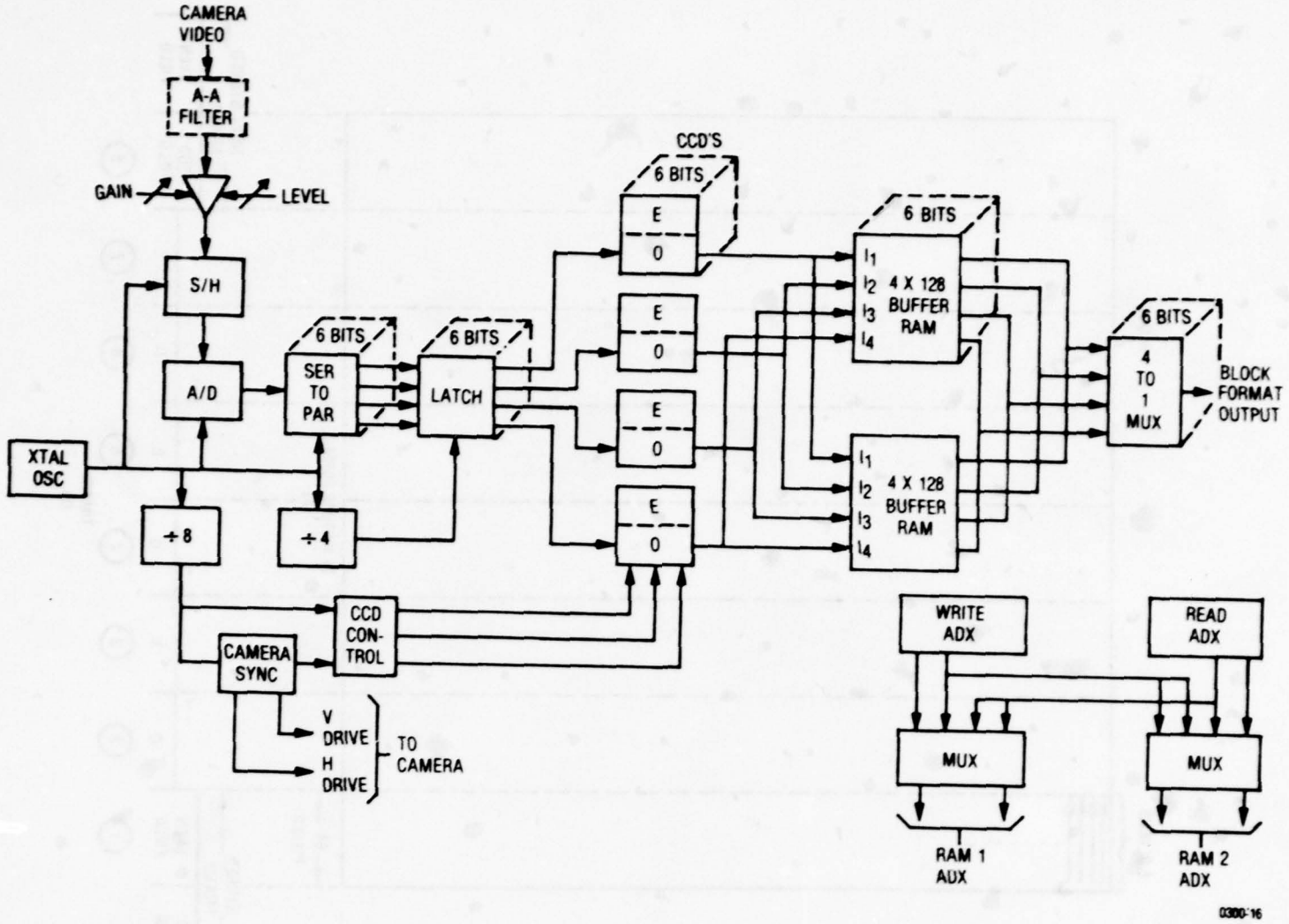


Figure 8. Frame Rate Buffer Simplified Block Diagram

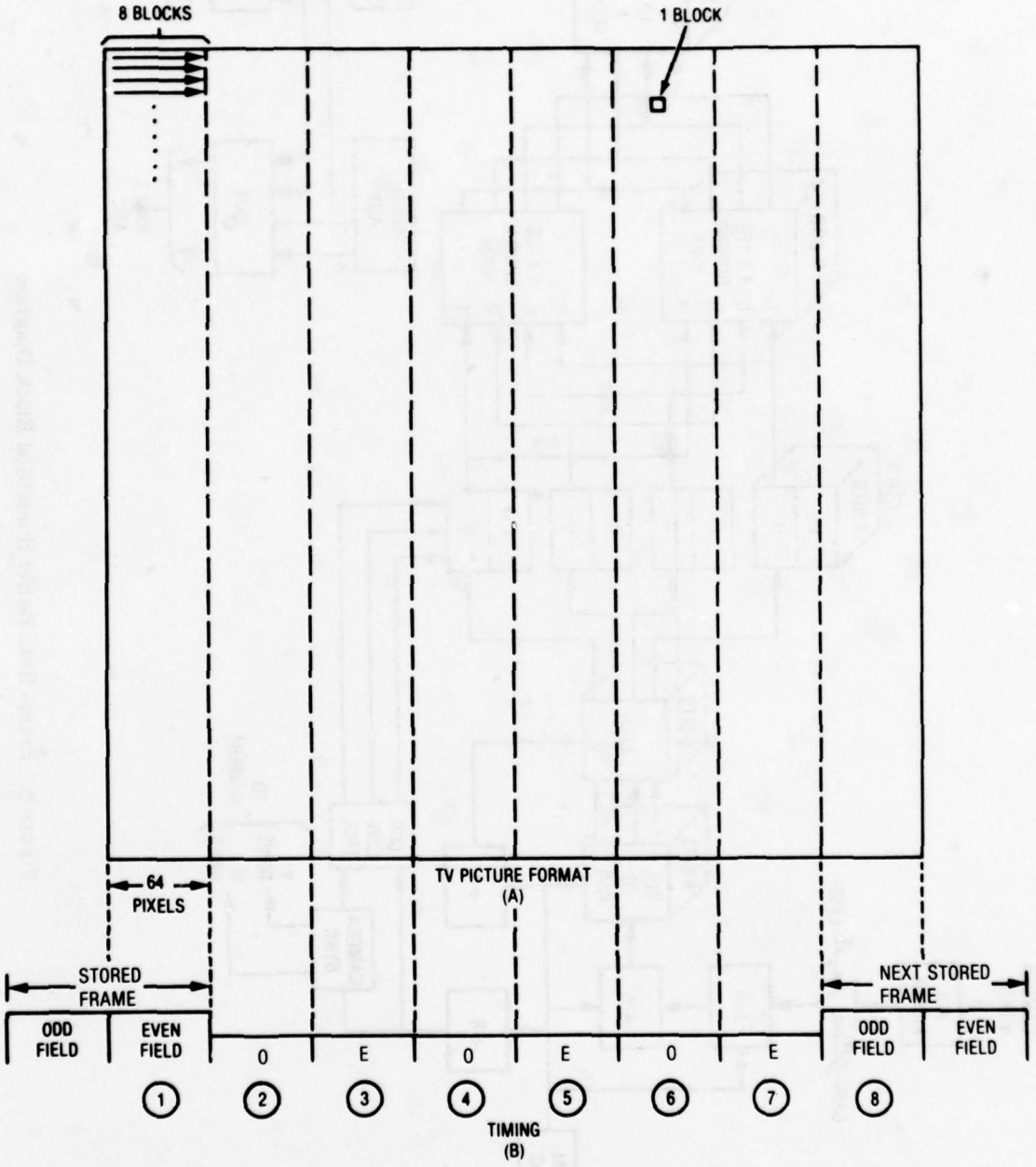
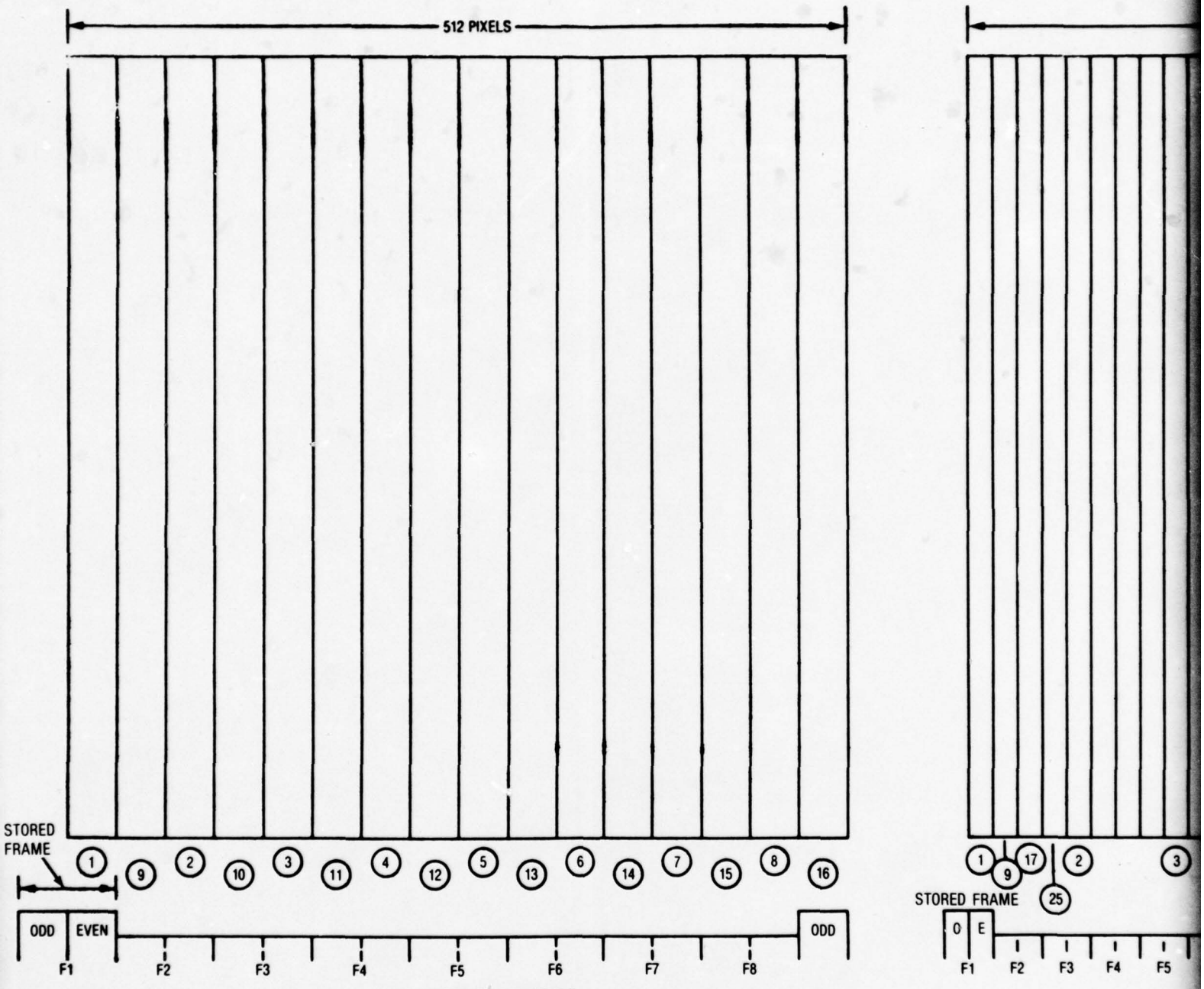


Figure 9a. Output Sequence of Picture



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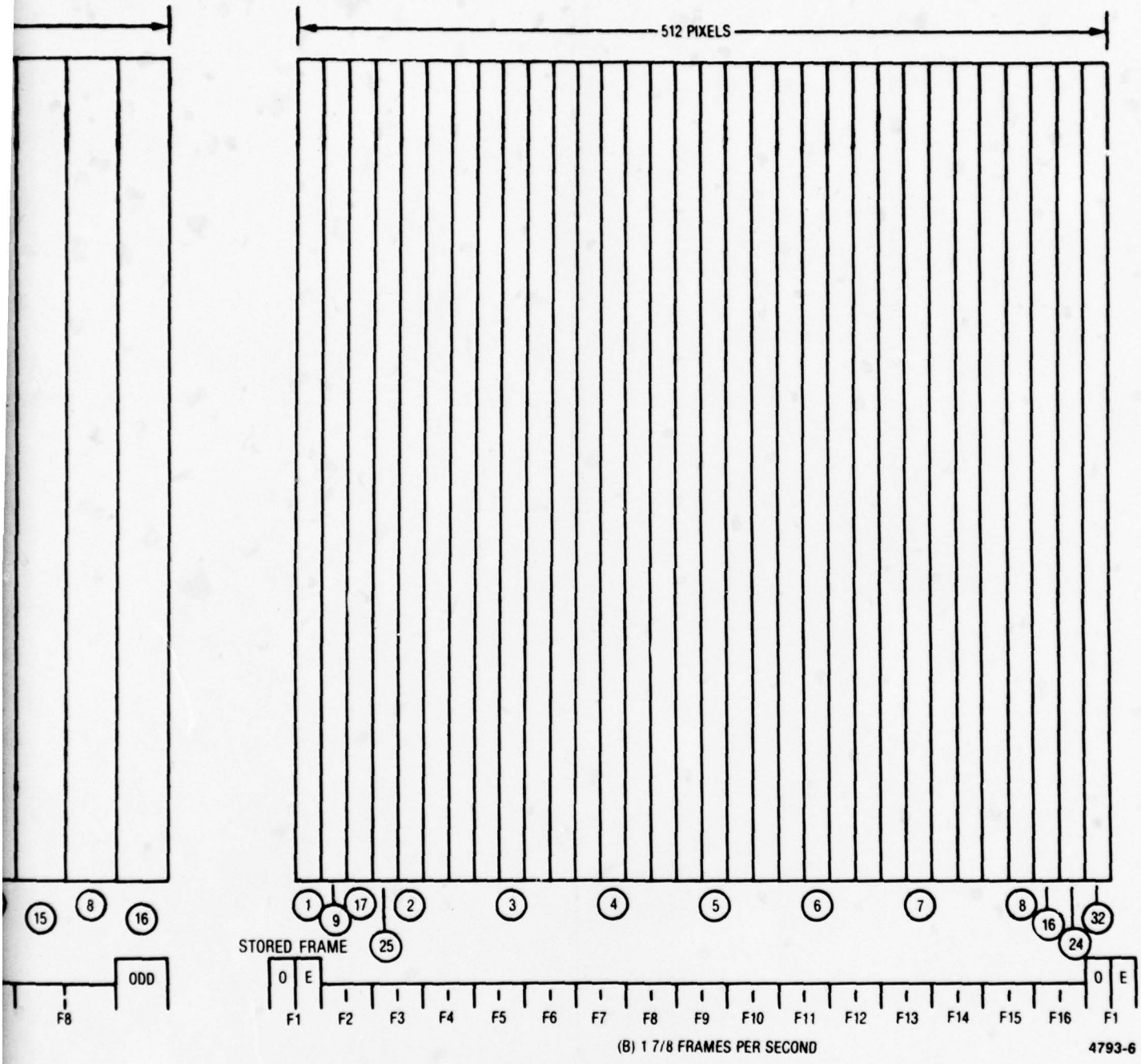

Figure 9b. Output Sequence of Picture

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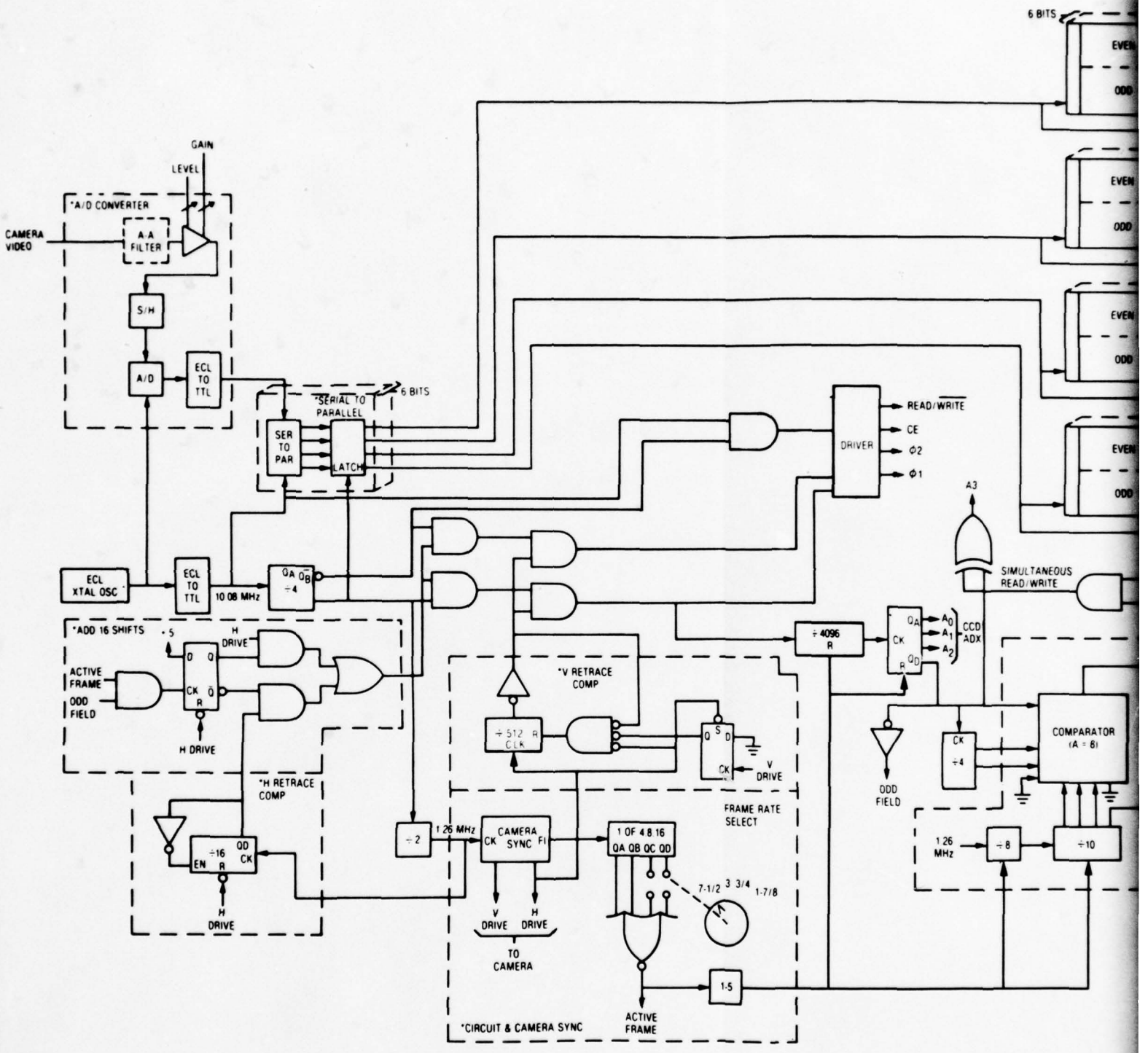
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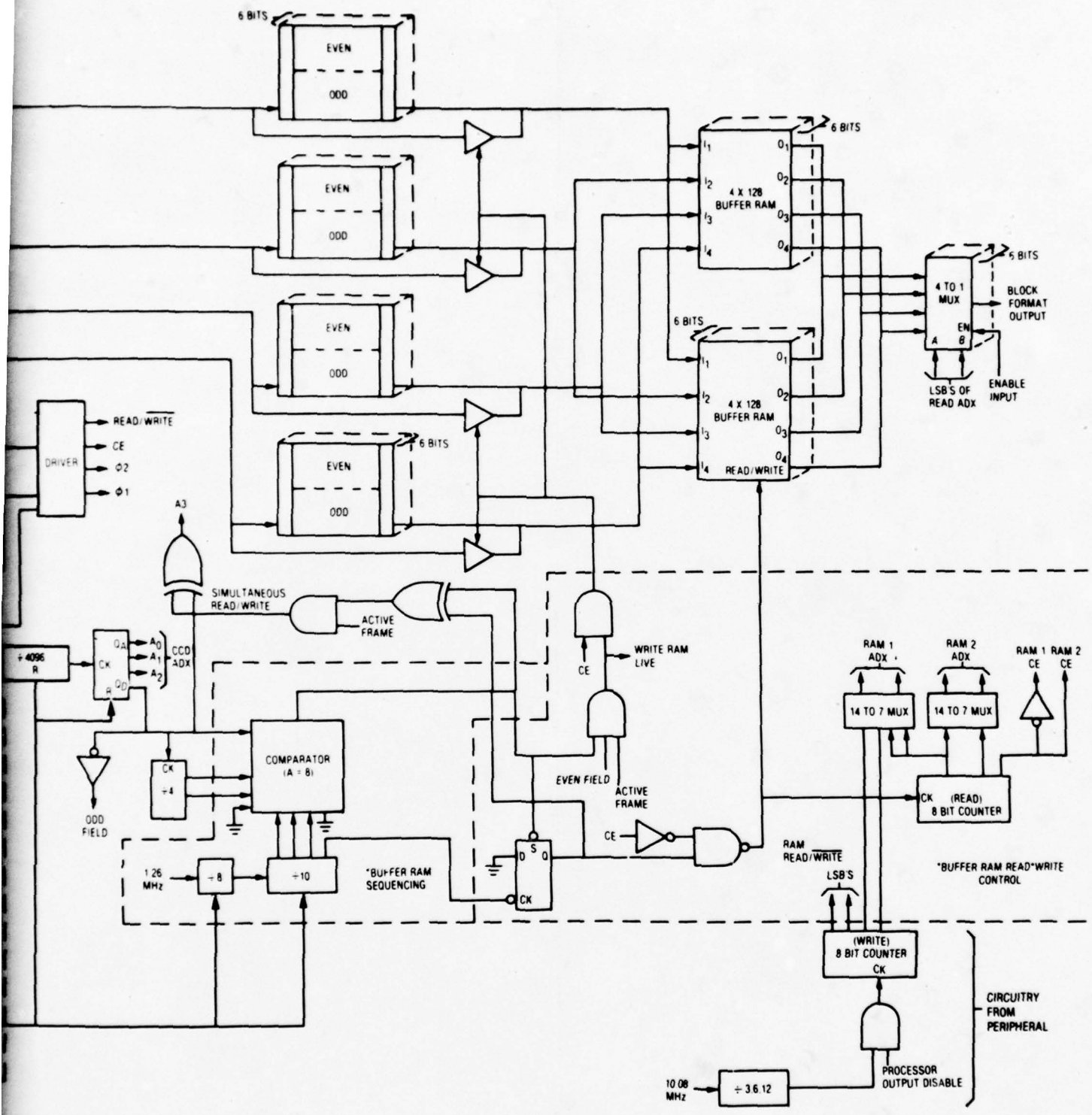

Figure 10. Frame Rate Buffer Detailed Block Diagram

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Each horizontal TV line has 512 pixel sampels, so a given CCD will have every fourth pixel stored in it (due to the four-bit-wide pixel bus) for a total of 128 pixels per line in a particular CCD. Also, since the data from the camera enters as an odd field followed by the even field, the CCD is segmented into odd and even field storage locations. The architecture for the CCD is shown in Figure 11. This figure represents only one of four identical CCDs required for each bit per pixel.

Once a complete frame of video has been stored in the frame store memory, it will be output in vertical picture stripes according to frame rate (see Figure 9). Since the FRB output must be frame oriented (interlaced odd and even field lines) 8x8 pixel blocks, the stored frame is not output until the even field of that frame. This means that the odd field of an active frame must be utilized to output the last vertical stripe of the previous stored frame. From a timing standpoint the odd field segment must be used to write data into the CCDs from the new active frame as well as output data from the odd and even fields of the old stored frame. These three operations (write new odd field data, read old odd field data, and read old even field data) occur at a 2.5 Mbps rate each, so this simultaneous manipulation would violate the 5 Mbps data throughput rate of the CCDs. To eliminate this, a data offset of 16 shifts, corresponding to one vertical picture stripe, was put in so that even field data from a stripe could be output from the CCDs to the buffer random access memory (RAM) prior to outputting odd field data to the buffer RAM. This would reduce the number of simultaneous manipulations to two for a 5 Mbps data rate. This shift is also shown in Figure 11. On a line by line basis, Figure 12 shows the CCD read and write operations required for storing and outputting one frame of video at the 7½ frames per second (FPS) rate.

The data read out of the CCDs is stored into redundant reformatting, or buffer RAMs. The two RAMs allow one of the RAMs to be written with CCD data while the other RAM is being read out to the Display Refresh Memory. After the CCD RAM is filled, the two RAMs switch functions. According to the timing sequence for data output, it takes only four real time TV horizontal line times to write a vertical picture stripe segment of 8 lines long into the buffer RAM since both odd and even field lines are available from the CCDs. This means that the DRM has four complete horizontal line times, or approximately 254 microseconds, to output 8 lines and 64 pixels per line of the given picture stripe segment. Figure 13 relates buffer RAM operation to the actual horizontal line timing for the first vertical stripe of a stored frame.

The reformatting function of the buffer RAM allows the data to be output in an 8 pixel x 8 pixel block format. The vertical stripe segment will be written into the RAM as 8 lines by 64 pixels, or eight 8x8 pixel blocks, in each buffer RAM. The buffer RAM architecture for the first eight blocks of the leftmost vertical picture stripe is shown in Figure 14. The data may then be read from the buffer and clocked through the output parallel-to-serial converter by supplying a seven-bit binary address to the RAM and a clock to the P/S converter. Adjacent eight-line pixel blocks are output from each vertical picture stripe in a top down manner. Figure 15 shows the actual 8x8 pixel block designations of an entire video frame.

The widest picture stripe to be output from the FRB is 64 pixels, as shown for the 7½ FPS rate in Figure 9(a). The buffer RAM is, therefore, capable of holding 64 pixels by 8 lines of data. At the 3¾ FPS rate, the picture stripe width is only 32 pixels, or four blocks, by 8 lines. In order to keep the controlling circuitry of the FRB to a minimum, the buffer RAM will always be loaded with a 64-pixel-wide stripe regardless of selected frame rate. It is, therefore, the job of the Display Refresh Memory to keep up with which data must be read from the buffer RAM. Table 1 defines what portion of the buffer RAM data must be read during each real time TV frame to load into the DRM at each of the three required frame rates. This table actually defines the addressing scheme from the DRM to retrieve the reduced frame rate data. The address from the DRM is actually the buffer RAM address of the FRB. There is an inherent delay in the RAM before data can be latched and clocked out of the parallel-to-serial converter at the output of the FRB. Figure 16 shows a timing diagram of the required signals, as well as how these signals are generated, and appropriate delay times for data output from the FRB. All signal lines are single ended TTL logical levels

There are two sync signals generated by the FRB. "FRAME SYNC" is a positive-going 500 nanosecond pulse output at the start of the transmission of a new active frame. From Figure 6, this pulse is sent prior to the first stored line of the even field of the real time TV frame because the first 8 blocks of the new stored frame are not available for output until this time (see Figure 9). A "BEGIN NEW PIXEL SET" pulse is used to signal the Display Refresh Memory that an output buffer RAM is loaded with 8 pixel blocks (8 lines x 64 pixels) and ready for output. This 100 nanosecond negative-going pulse is output every 4 horizontal line times or ≈254 microseconds. The DRM has this length of time to read the 8 pixel blocks from one buffer RAM. Both signals are TTL compatible.

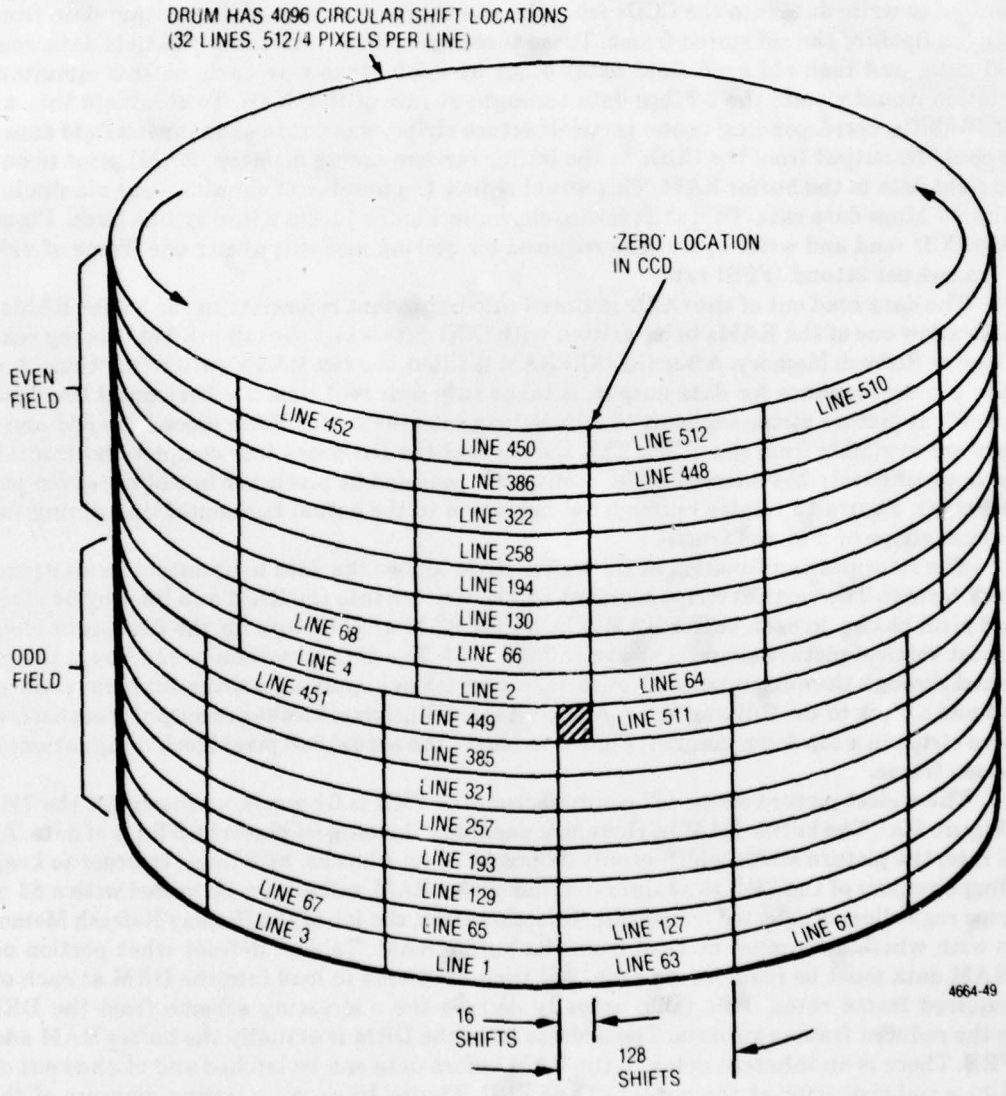
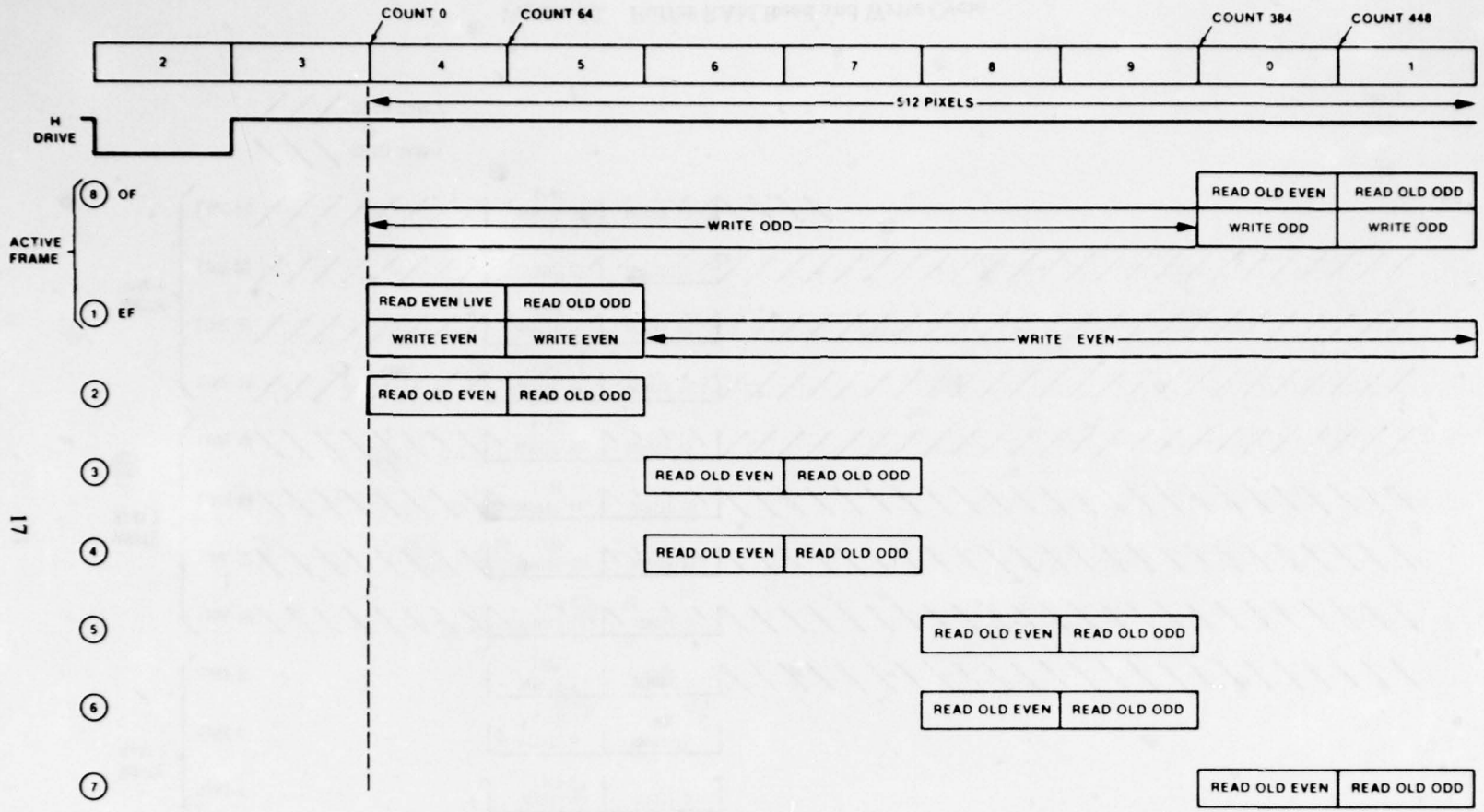


Figure 11. Line Organization in CCD Frame Rate Buffer Memory (Drum Concept)



NOTE: THIS SHOWS THE SEQUENCE FOR 7 1/2 FRAMES PER SECOND, BUT IS REPEATED (EXCEPT FOR WRITE) FOR LOWER FRAME RATES.

4793-9

Figure 12. Read/Write Sequencing for CCD

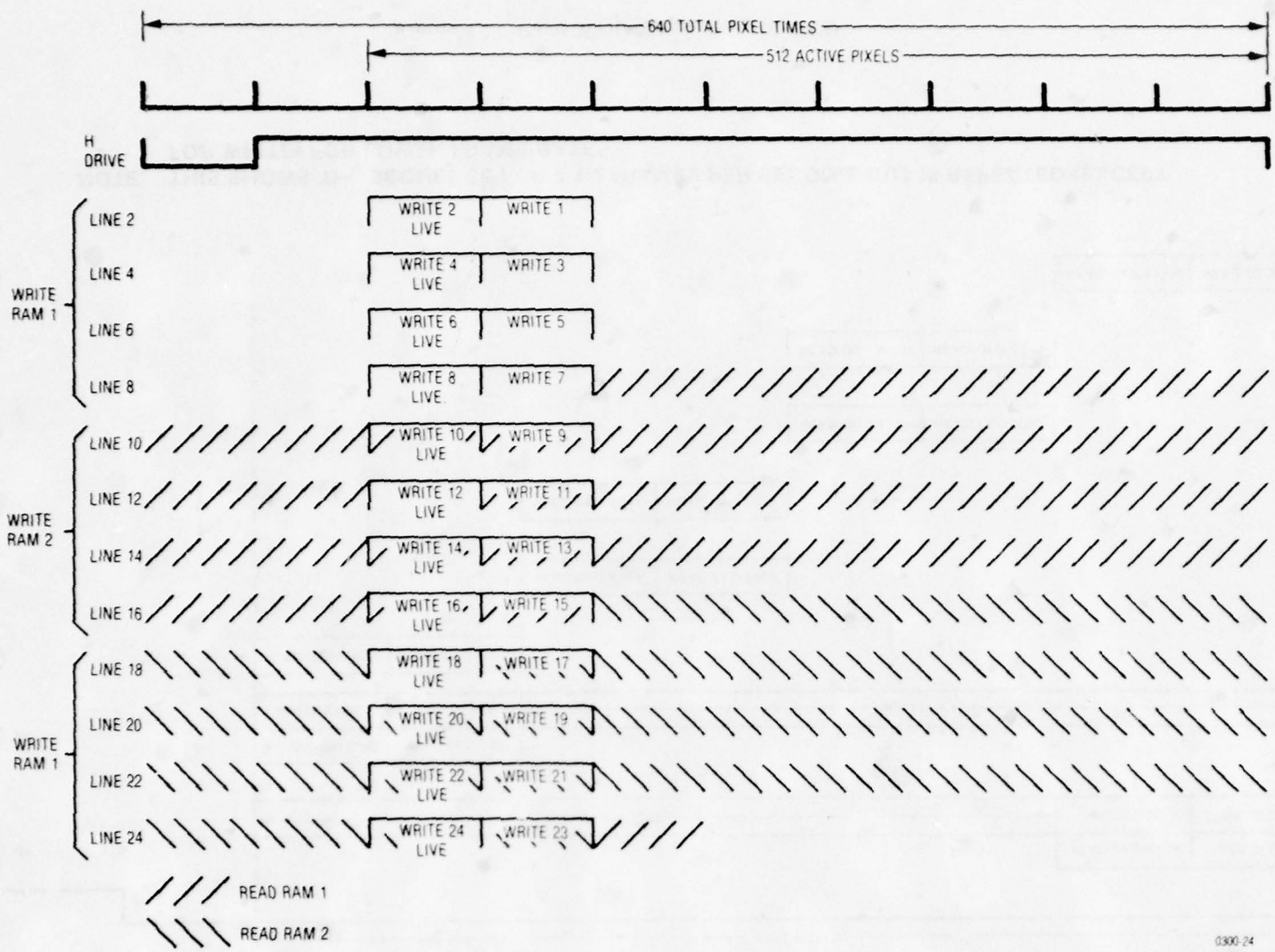


Figure 13. Buffer RAM Read and Write Cycle

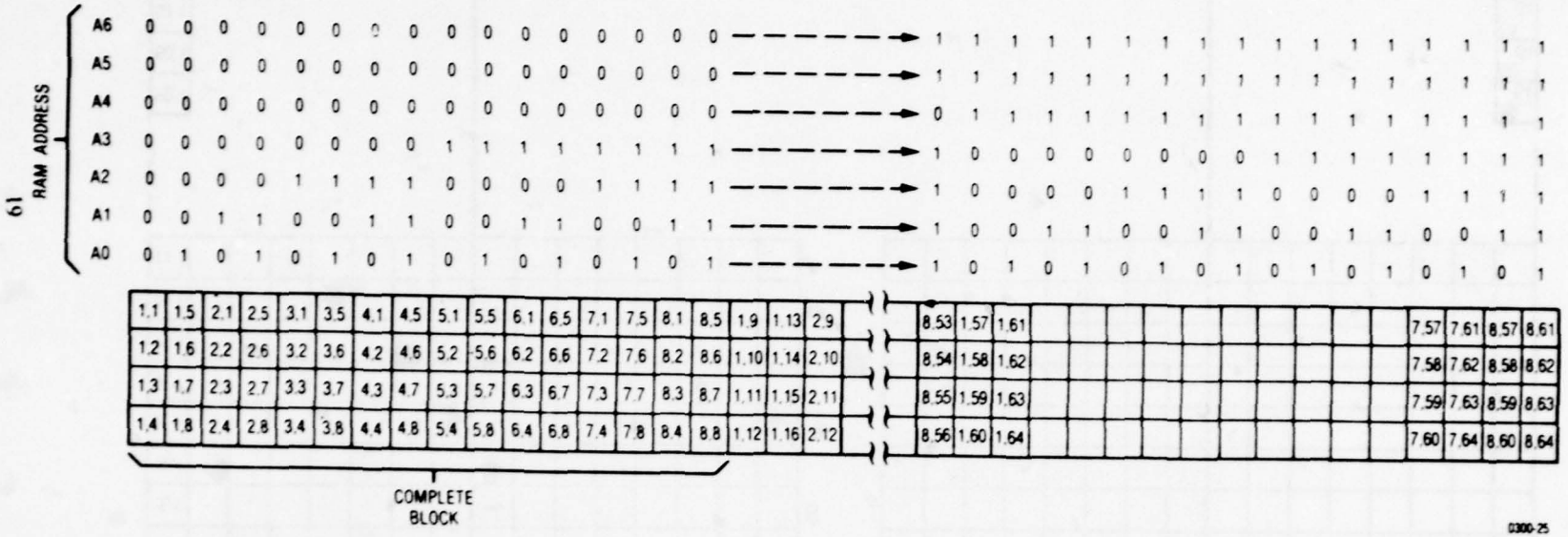


Figure 14. Output Buffer RAM Storage Architecture

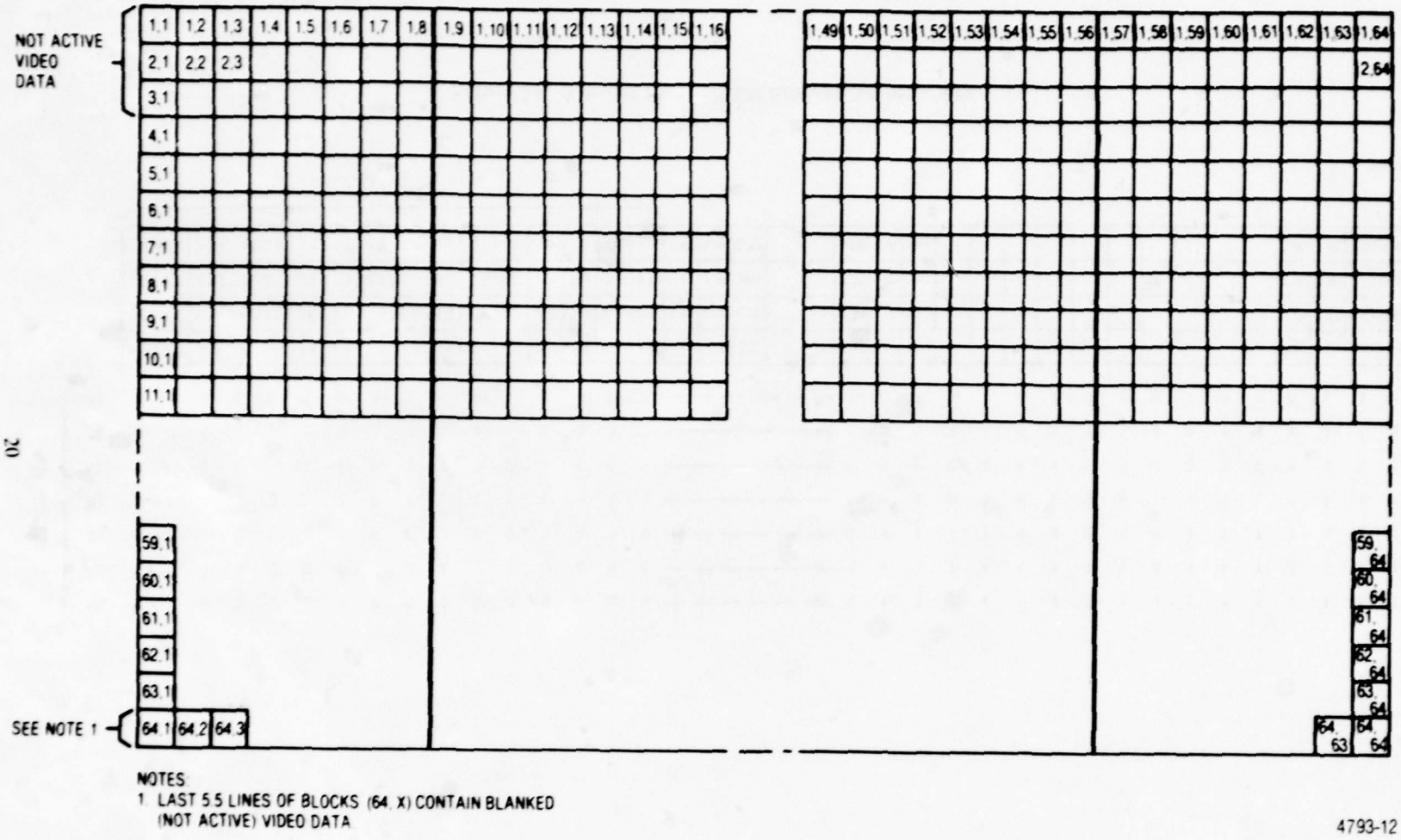


Figure 15. 8 x 8 Block Number Definition

TABLE 1. PIXEL SEQUENCE FROM FRB OUTPUT RAM

Frame Rate	Number of BEGIN Pulses	Pixels/ BEGIN Pulse	Pixel Sequence From RAM
7½ FPS	512	512	0-511 for all 4 frames
3¾ FPS	1024	256	0-255 for first 4 frames
			256-511 for second 4 frames
1⅞ FPS	2048	128	0-127 for first 4 frames
			128-255 for second 4 frames
			256-383 for third 4 frames
			384-511 for fourth 4 frames

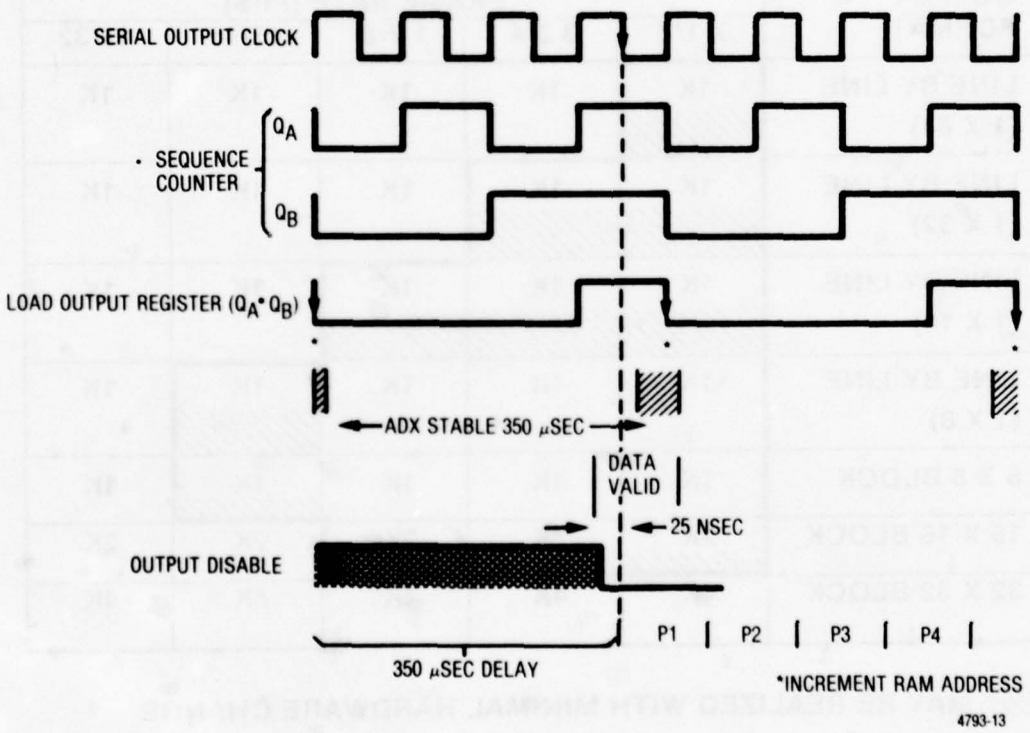


Figure 16. Output Timing Sequence of Frame Rate Buffer

The output format of the Frame Rate Buffer is an 8x8 block oriented, six-bit pixel serial data line. Figure 17 shows the current output scheme along with other block size outputs available as well as the possible line-by-line output modes. All line-by-line modes inside the dark line are available by simply changing the address scheme of the Display Refresh Memory. The larger block sizes and areas outside the dark line require significant hardware changes to be implemented in the FRB.

The Frame Rate Buffer unit was designed to operate over the temperature range of −29 degrees C to +49 degrees C. All parts except the CCDs and clock drivers are specified over the entire military temperature environment of −55 degrees C to +125 degrees C. The memories and clock drivers are specified at 0 degrees C to +70 degrees C.

The Frame Rate Buffer is powered by four modular power supplies. Table 2 lists each supply with its associated current output. These supplies are all short circuit and overvoltage protected. The input requirements are 115 Vac ± 10 percent, 50-400 Hz. Table 3 shows the technology and functional submodule power dissipation of the FRB.

Figure 18a shows a photograph of video data viewed directly from a TV camera to a monitor. Figure 18b shows a photograph of video through the AFAL brassboard video memory system and displayed on a monitor.

OUTPUT FORMAT	FRAME RATE (FPS)				
	7 1/2	3 3/4	1 7/8	15/16	15/32
LINE BY LINE (1 X 64)	1K	1K	1K	1K	1K
LINE BY LINE (1 X 32)	1K	1K	1K	1K	1K
LINE BY LINE (1 X 16)	1K	1K	1K	1K	1K
LINE BY LINE (1 X 8)	1K	1K	1K	1K	1K
8 X 8 BLOCK	1K	1K	1K	1K	1K
16 X 16 BLOCK	2K	2K	2K	2K	2K
32 X 32 BLOCK	4K	4K	4K	4K	4K

MAY BE REALIZED WITH MINIMAL HARDWARE CHANGE

4793-14

Figure 17. Buffer RAM Size (Per Bit Slice) for Frame Rate Buffer

TABLE 2. POWER SUPPLY REQUIREMENTS

Power Supply	Current Without A/D and S/H	Current With Hybrid/Discrete A/D and S/H
+5Vdc	860 mA	1000 mA
+12Vdc	550 mA	550 mA
−5Vdc	<10 mA	<10 mA
−12Vdc	<10 mA	460 mA

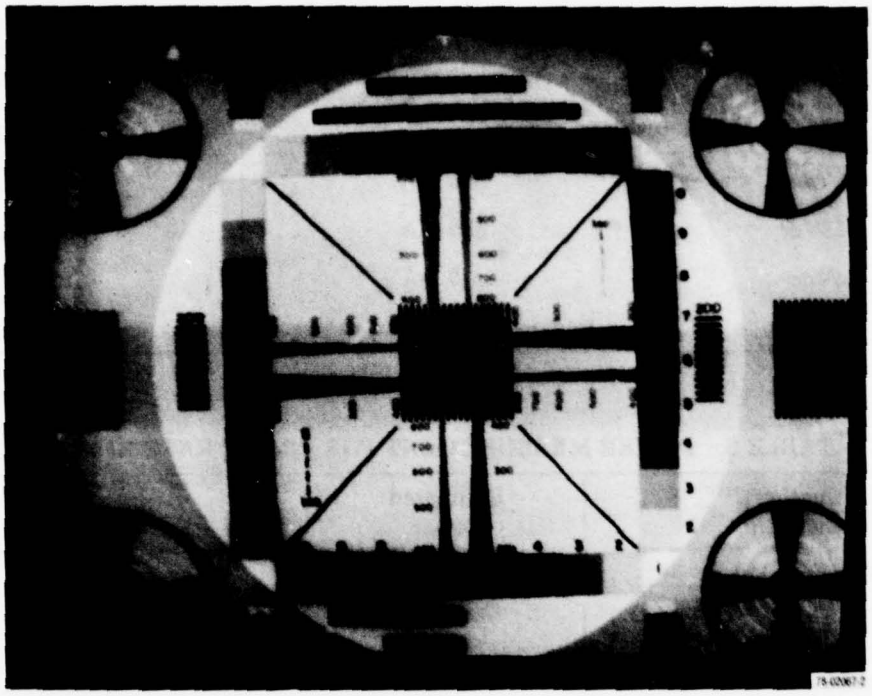
TABLE 3. POWER MEASUREMENT FOR FRAME RATE BUFFER

Functional Description	Estimated Power	Technology
Serial to parallel converter	1.5W	Low power Schottky
CCD Memory Devices and clock drivers	2.4W 3.0W	MOS
Buffer RAM	0.3W	Silicon on Sapphire MOS
Output Register	0.1W	Low power Schottky
Control Logic	3.5W	LS TTL and MOS
TOTAL	10.8W	

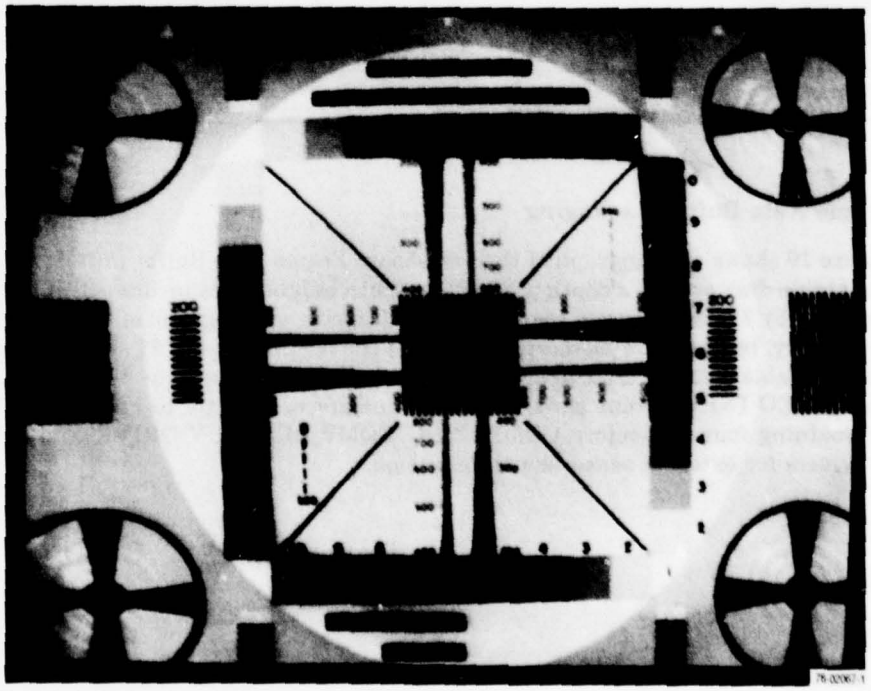
b. Frame Rate Buffer Packaging

Figure 19 shows a photograph of the brassboard Frame Rate Buffer unit. It is built in a 19 inch rack-mountable drawer with a depth of 29 inches and a height of 5½ inches. All of the electronics are housed on two 7 by 7 inch wirewrap boards. Figure 20 shows a photograph of the circuit board containing CCD memory, buffer RAM memory, and output converters. Figure 21 shows a photograph of the timing board. Table 4 shows a parts breakdown for the two Frame Rate Buffer circuit boards.

The VIDEO INPUT front panel connector interfaces directly to an RS-170, 75 Ω video source. The remaining four connectors, COMP SYNC, COMP BLANK, V DRIVE, and H DRIVE are 75 Ω source drivers for external sensor synchronization.



a.



b.

Figure 18. Video Data Displays

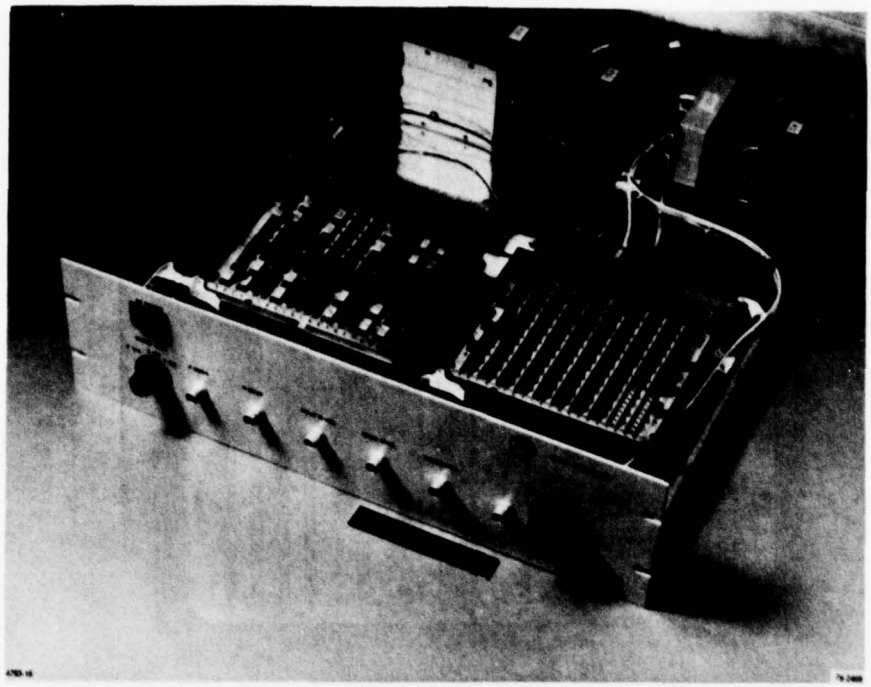


Figure 19. View of Frame Rate Buffer Unit

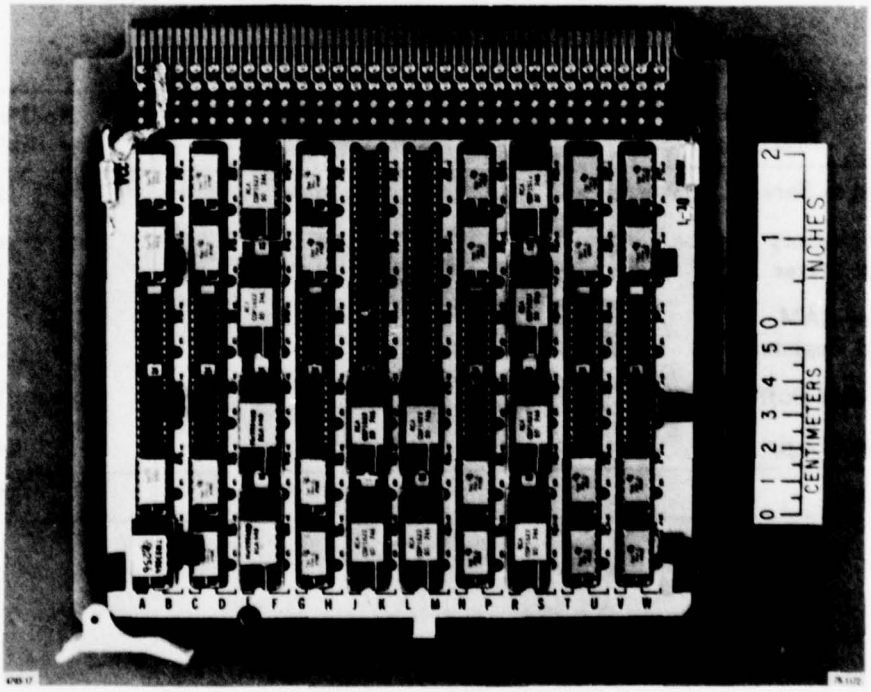


Figure 20. Frame Store Memory Circuit Board

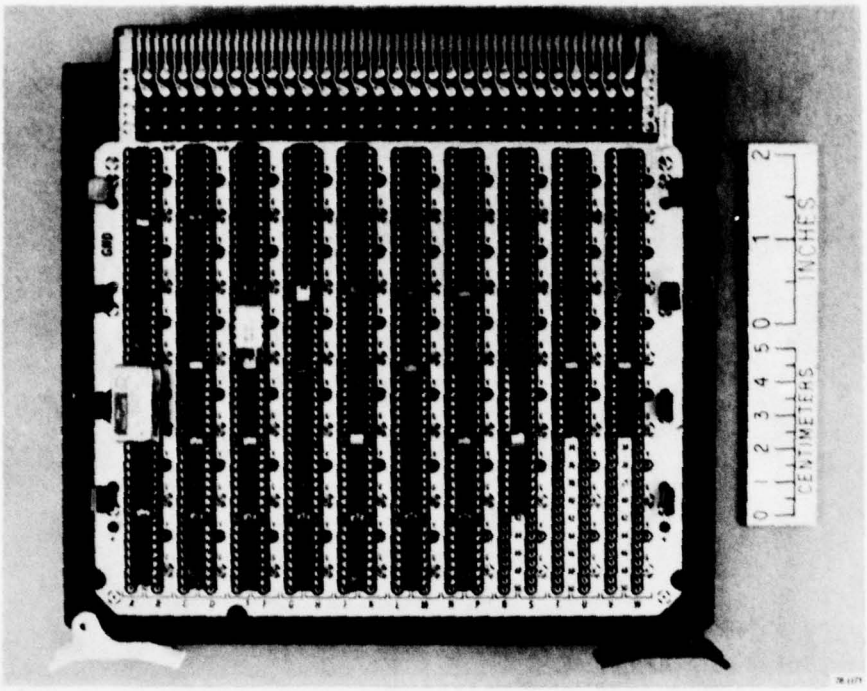


Figure 21. FRB Timing Board

TABLE 4. PARTS COUNT FOR FRAME RATE BUFFER

Functional Description	6 Bits/Pixel Functional Total	No. Parts at 1 Bit/Pixel
Serial to Parallel Converter	12	2
CCD Memory Devices	24	4
and Driver	6	1
Buffer RAM	12	2
and Register	6	1
Tri-State Buffer	6	1
Control Logic	44	44
TOTAL	110	55

2 DISPLAY REFRESH MEMORY DETAILED DESCRIPTION

a. Technical Operation

The Display Refresh Memory is capable of inputting and storing frame rate reduced video data while continuously refreshing an NTSC standard TV monitor at a 30 frame/second rate. The DRM essentially performs the reverse function of the Frame Rate Buffer. A simplified block diagram showing the major operational blocks in the DRM is shown in Figure 22. The serial input data is clocked through a serial-to-parallel converter and written into an input buffer RAM. The operation of outputting a full RAM of data from the FRB to the DRM is actually a copy function with each pixel from the FRB being transferred to its corresponding location in the DRM. This data is then stored in CCD memory for output. There are two complete frame memories in the FRB, and they operate in alternate modes. While one memory is being loaded with a slow scan video frame, the other is read out through a high speed D/A converter to a TV monitor. After the first memory is full, that memory is switched by the FRAME SYNC signal to be displayed on the monitor.

A detailed block diagram of the Display Refresh Memory unit is shown in Figure 23. Upon command of the BEGIN NEW PIXEL SET pulse, the six-bit pixel serial input data (from the FRB output) is clocked into a serial-to-four-wide parallel converter by the external serial data clock. The circuitry required for generating this external clock, along with the address lines to the FRB, are contained in the DRM but not considered part of it. The four input pixels are then written into an input buffer RAM. There are two redundant buffer RAMs that operate in alternate modes. While one RAM is being written with input data, the other is being read into the CCD frame store memory. This redundant RAM removes the complexity of trying to simultaneously read and write a single RAM. After one RAM has been loaded with input data, a RAM FULL pulse is generated and the two RAMs reverse functions. Each RAM, whether written with input data or read into the CCD memory, has four horizontal line times (254 microseconds) to complete its function. Figure 24 shows a timing diagram of the data input sequence along with associated start pulses.

The CCD memories are loaded with data from the buffer RAM in an architecture similar to that of the FRB. Since the digital CCD data is output directly to the D/A converter for display, this CCD data is arranged with adjacent line odd field data in the lower half of memory and adjacent line even field data in the upper half of memory. This architecture is shown in Figure 25. As in the FRB, there is one CCD for each of the four parallel data lines and 4 CCDs for each bit per pixel for a total of 24 CCDs in each of the two frame memories of the DRM. The four parallel CCDs are each loaded with every fourth pixel from a horizontal line, so each CCD will contain ¼ of a horizontal line, or 128 pixels. The shaded areas in the lines of Figure 24 represent the new data stored for the first vertical picture stripe of the output video frame at the 7½ FPS rate. This stripe is 64 pixels long (see Figure 9 (a)). One buffer RAM, therefore, contains 8 lines by 64 pixels of data. The first vertical picture stripe will be written into the CCD locations reserved for lines 1 through 8, and each of the four CCDs will be written with 16 pixels (64 pixels total). One buffer RAM will therefore store the designated 16 pixels of lines 1 through 8 into the CCDs. The second RAM will store the first 16 pixels of lines 9 through 16 into the four CCDs. This process will continue until the entire CCD memory has been filled from the RAMS with these 16 pixel wide segments. Each CCD will make eight complete revolutions for each vertical picture stripe output from the FRB. Since each stripe is sent during one entire real time TV field, the CCD will make these eight revolutions in each field.

The horizontal line data from the CCDs will then be output to the high speed D/A converter (DAC) in a sequential manner. Since the frame rates of 7½ FPS, 3¾ FPS and 1⅞ FPS correspond to receiving one complete active video frame every 4, 8 or 16 real time TV frames respectively, the CCD memory being displayed on the monitor will be read 4, 8 or 16 times. The Display Refresh Memory has its own internal master oscillator and TV sync generator so that the alternating between frame memories in the DRM results in flicker-free monitor operation. A sample timing diagram for reading digital CCD data and outputting it to the DAC is shown in Figure 26. The same serial output clock of the DRM output is used by the DAC since data is read out of the DRM on the negative-going edge of this clock and the DAC latches in new pixel data on the positive-going edge of this clock.

A high speed DAC is used to interface the 6-bit digital data from the DRM to the TV monitor. The DAC accepts a 6-bit, TTL compatible, 10 Mbps pixel along with composite sync and composite blanking to output standard RS-170 composite video. The output is buffered and capable of driving a 75 ohm load. A block diagram of the D/A converter is shown in Figure 27.

As shown in the block diagram, alternate pixels will be latched and presented to each DAC every 200 nanoseconds. The outputs of the DACs are then multiplexed so that every pixel is output. This dual latch/DAC approach was chosen to minimize power consumption and maximize speed performance as compared to the conventional DAC module and sample/hold circuitry. By using the two DACs and multiplexer, the analog output has a chance to settle since, if it were not settled when one DAC output was selected, it would settle during that sample. Using a sample and hold, however, if the DAC had not settled when sampled, the output would be wrong for the entire sample. So the two-DAC approach offers some significant advantages.

This converter has been designed, built and tested to operate satisfactorily over the temperature range −55 degrees C to +90 degrees C. The composite blanking signal will be used to output a black (all zero equivalent) video level during horizontal and vertical blanking intervals of the monitor. Composite sync will be summed into the output video to produce the standard RS-170 composite video.

The Display Refresh Memory will accept the line-by-line or different block-sized data formats shown in the inside portion of Figure 17 without internal DRM circuitry changes. The only change required is in the control/interface circuitry which addresses the Frame Rate Buffer's output buffer RAM.

The Display Refresh Memory unit was designed to operate over the specified temperature range of −29 degrees C to +49 degrees C. All parts except the CCDs and clock drivers are specified over the entire military temperature environment of −55 degrees C to +125 degrees C. The memories and clock drivers are specified at 0 degrees C to +70 degrees C.

The Display Refresh Memory is powered by four modular power supplies. Table 5 lists each supply with its associated drive current loads. All supplies are short circuit proof and overvoltage protected for maximum circuit protection. The input requirements to these supplies are 115Vac±10%, 50-400 Hz. Table 6 summarizes the technology and functional submodule power dissipation of the DRM. This power includes the interface circuitry that controls the FRB/DRM serial data interface.

b. Display Refresh Memory Packaging

Figure 28 shows a photograph of the brassboard Display Refresh Memory unit. It is built in a 19" rack-mountable drawer with a depth of 29 inches and a height of 5½ inches. The electronics are mounted on four 7x7 inch wirewrap boards with all control and interface signals connected through a 55-pin circular connector. Figure 29 shows the component layout of one of the two complete CCD frame store memories in the DRM. Table 7 shows a parts breakdown for the four DRM circuit boards.

There are four test points located on the front panel of the Display Refresh Memory. H DRIVE is a synchronizing signal for observing actual video output data. The SYNC signal is the FRAME SYNC pulse which designates the beginning of a new active frame of video to be output from the FRB. The LOAD RAM test point is the "BEGIN NEW PIXEL SET" signal from the FRB. This signal indicates that an FRB buffer RAM is full and ready to be output to the DRM. The RAM FULL test point is generated inside the DRM that indicates one FRB RAM has been transferred to the DRM input RAM and is ready to be written into the CCDs. All four of these signals are buffered so that unintentional grounding will not affect the operation of the DRM.

The composite sync and composite video signals are used for TV monitor or video tape recorder synchronization. Each of these signals is capable of driving a 75 ohm load and is short circuit protected.

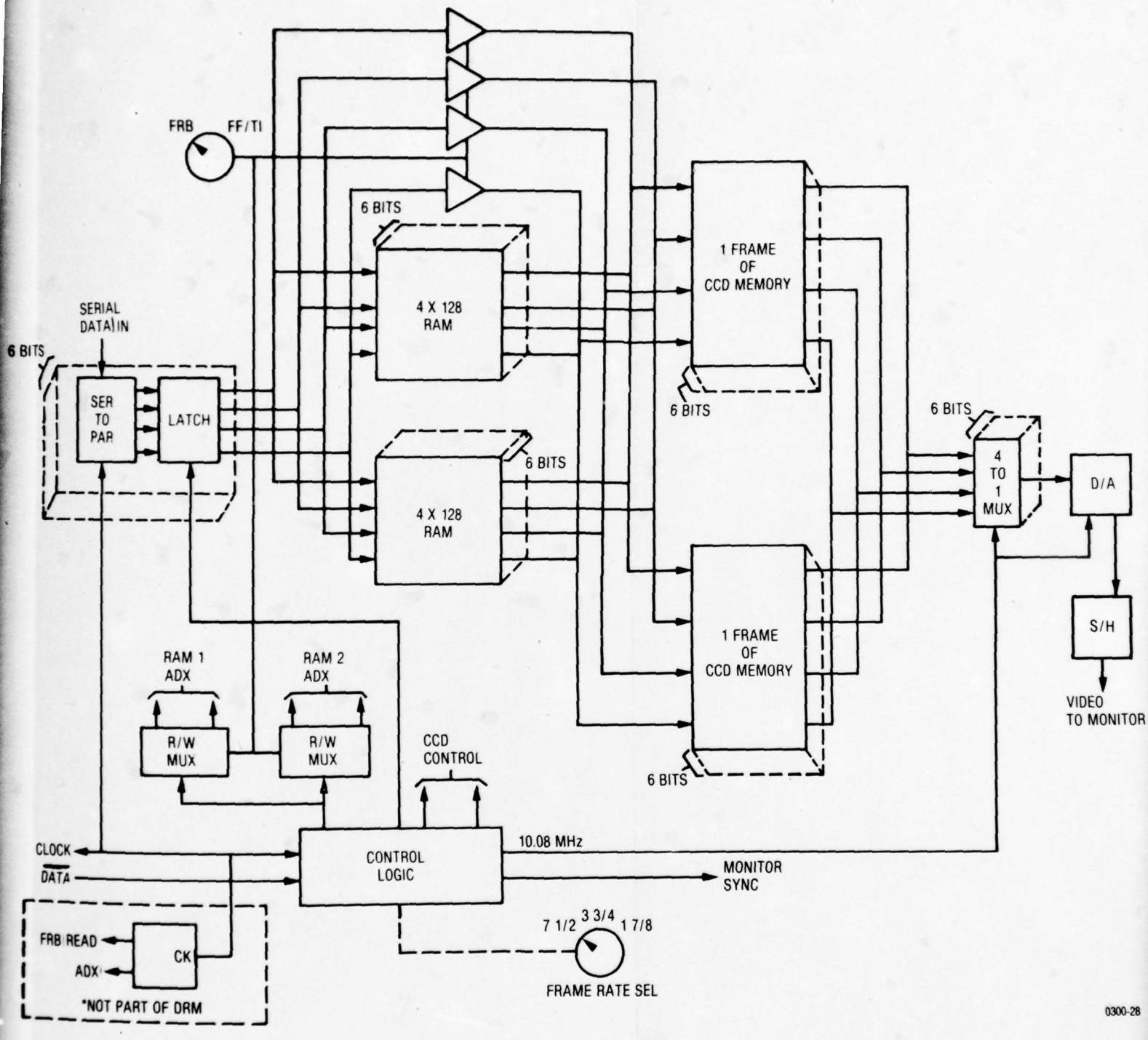


Figure 22. Display Refresh Memory Block Diagram

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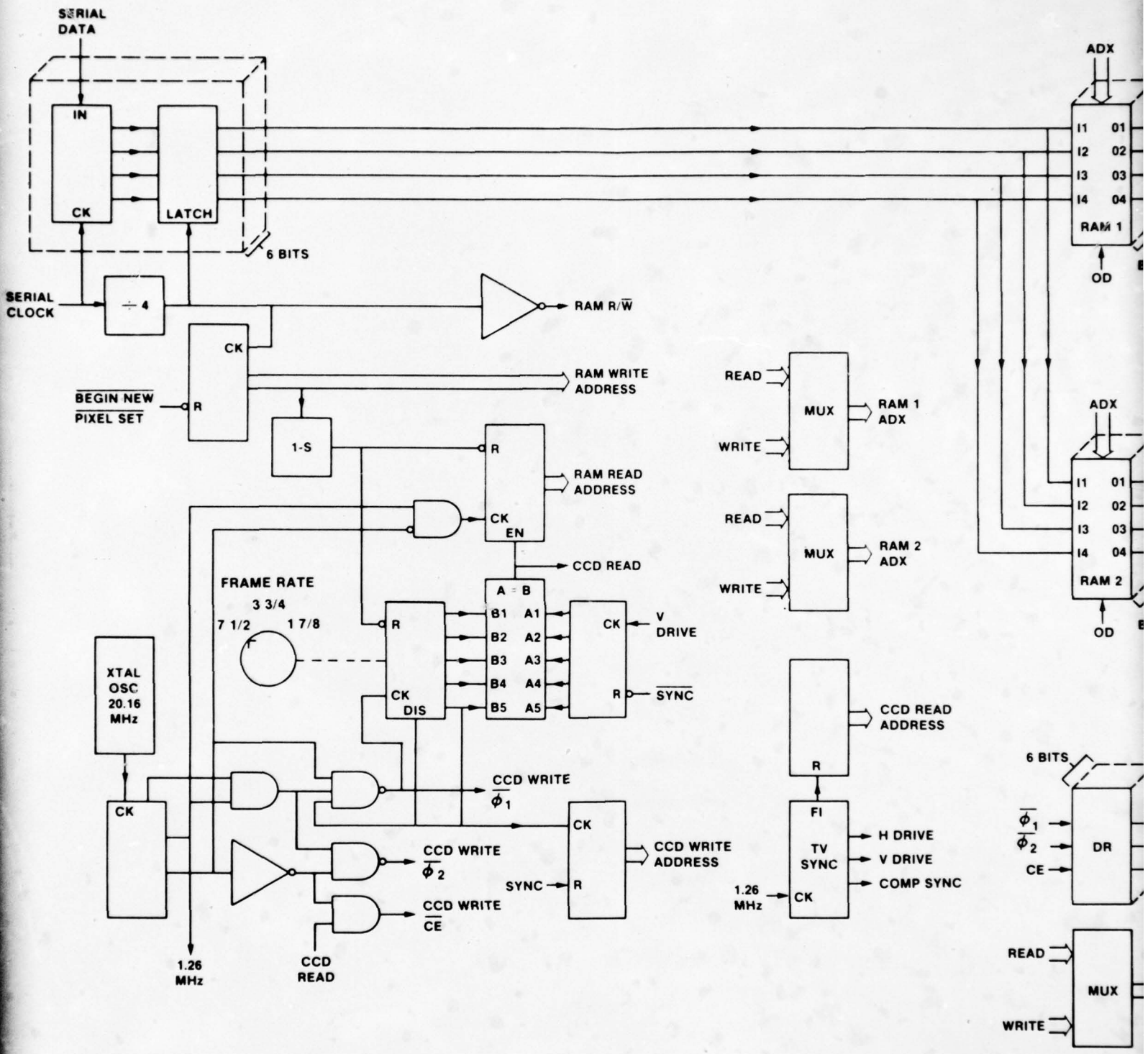
SERIAL DATA
IN
CK
LATCH
6 BITS
SERIAL CLOCK
÷ 4
RAM R/W
CK
BEGIN NEW PIXEL SET
R
RAM WRITE ADDRESS
1-S
R
RAM READ ADDRESS
CK EN
CCD READ
FRAME RATE
3 3/4
7 1/2
1 7/8
A = B
B1 A1
B2 A2
B3 A3
B4 A4
B5 A5
R
CK DIS
CK
V DRIVE
R
SYNC
XTAL OSC 20.16 MHz
CK
CCD WRITE $\overline{\phi_1}$
CCD WRITE $\overline{\phi_2}$
CCD WRITE $\overline{CE}$
CK
SYNC
R
CCD WRITE ADDRESS
1.26 MHz
CCD READ
READ
WRITE
MUX
RAM 1 ADX
READ
WRITE
MUX
RAM 2 ADX
R
CCD READ ADDRESS
FI
TV SYNC
CK
1.26 MHz
H DRIVE
V DRIVE
COMP SYNC
ADX
I1 01
I2 02
I3 03
I4 04
RAM 1
OD
ADX
I1 01
I2 02
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RAM 2
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CE
DR
READ
WRITE
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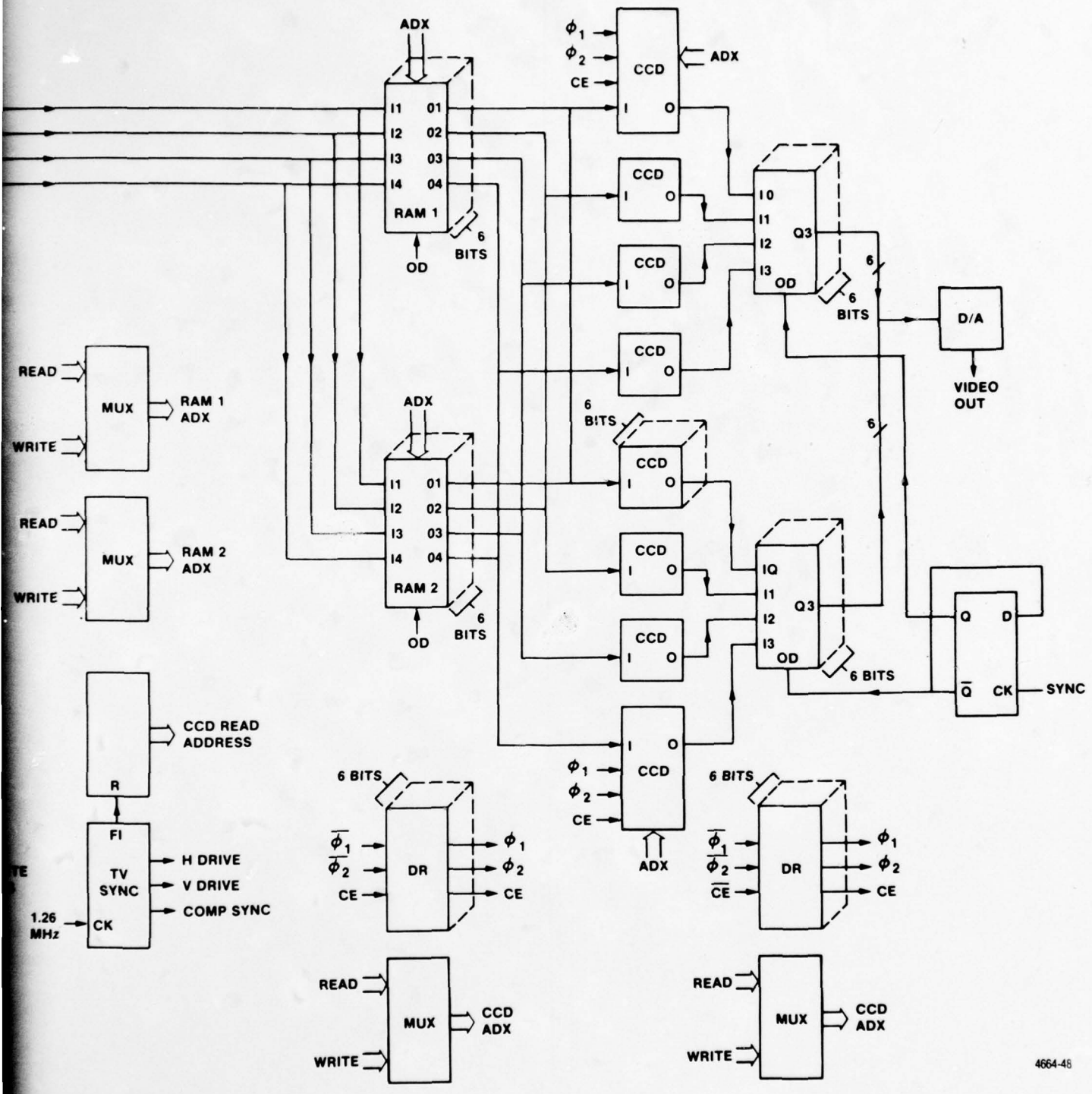

Figure 23. Detailed Block Diagram for Display Refresh Memory

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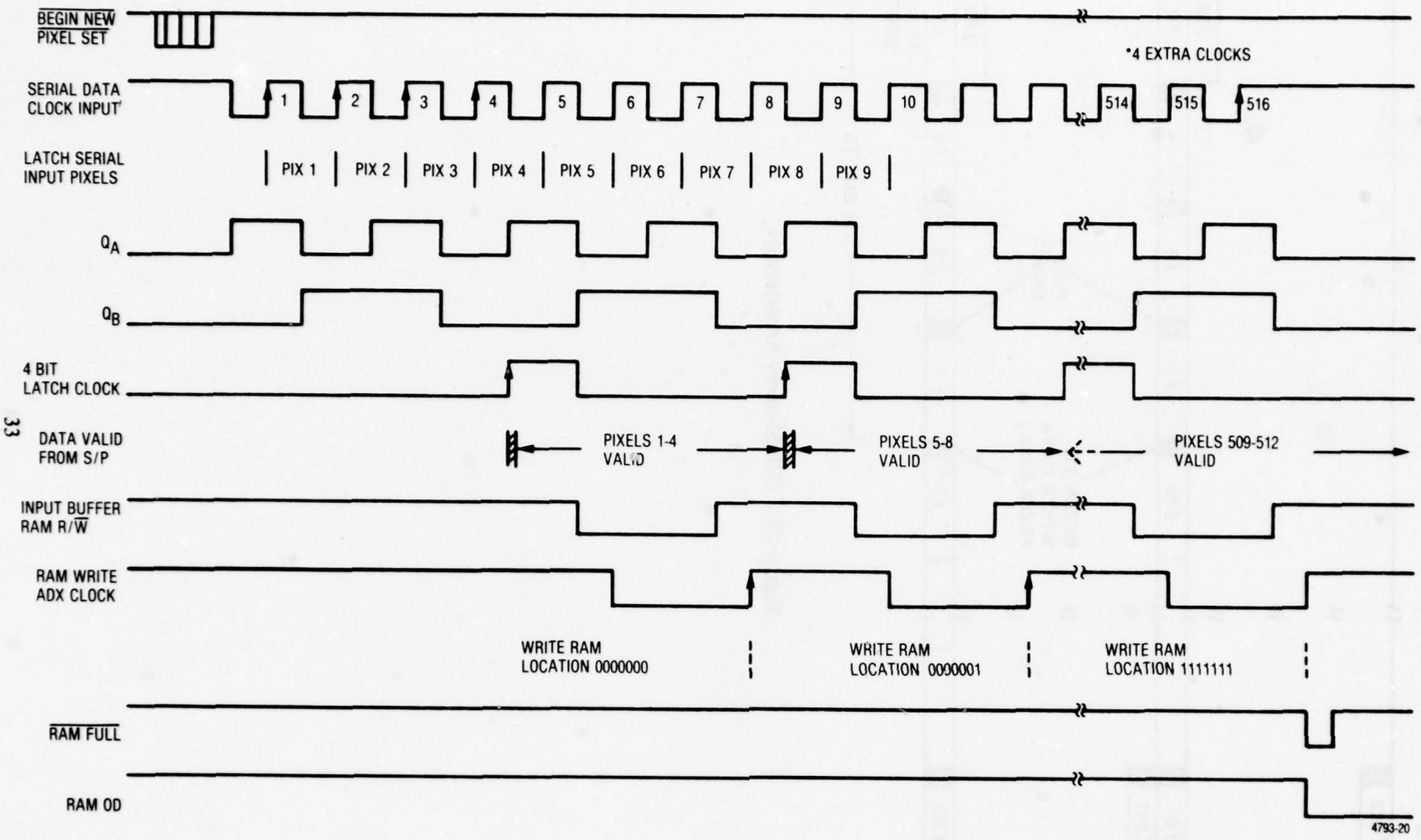

Figure 24. Serial Data Input Timing Sequence for DRM

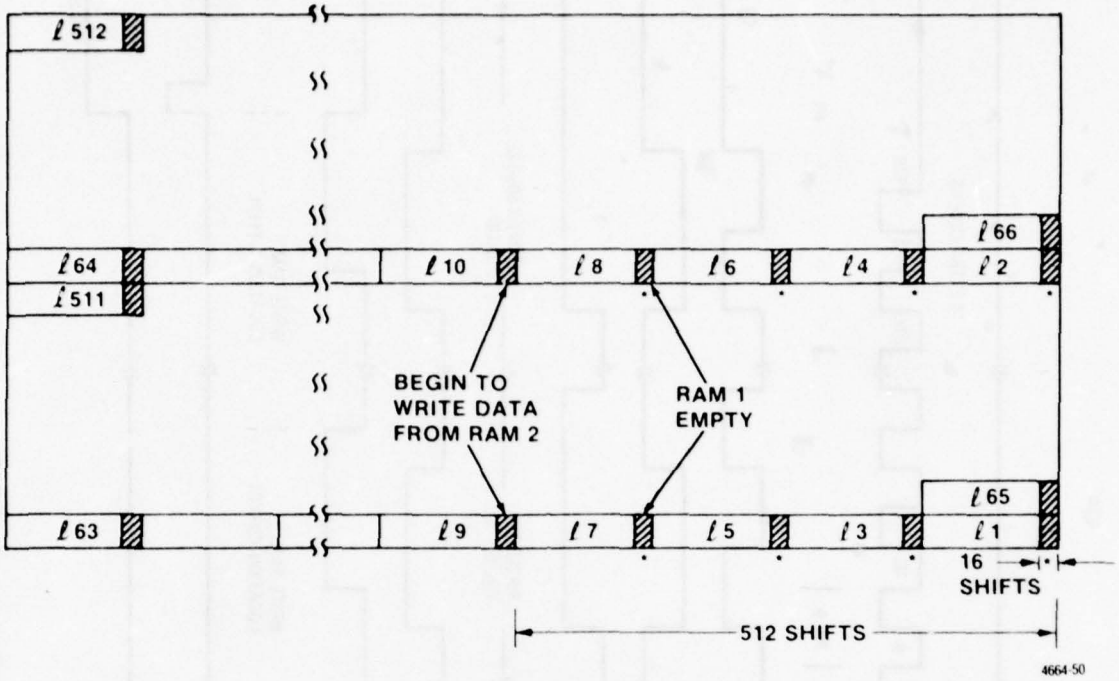

Figure 25. CCD Memory Architecture

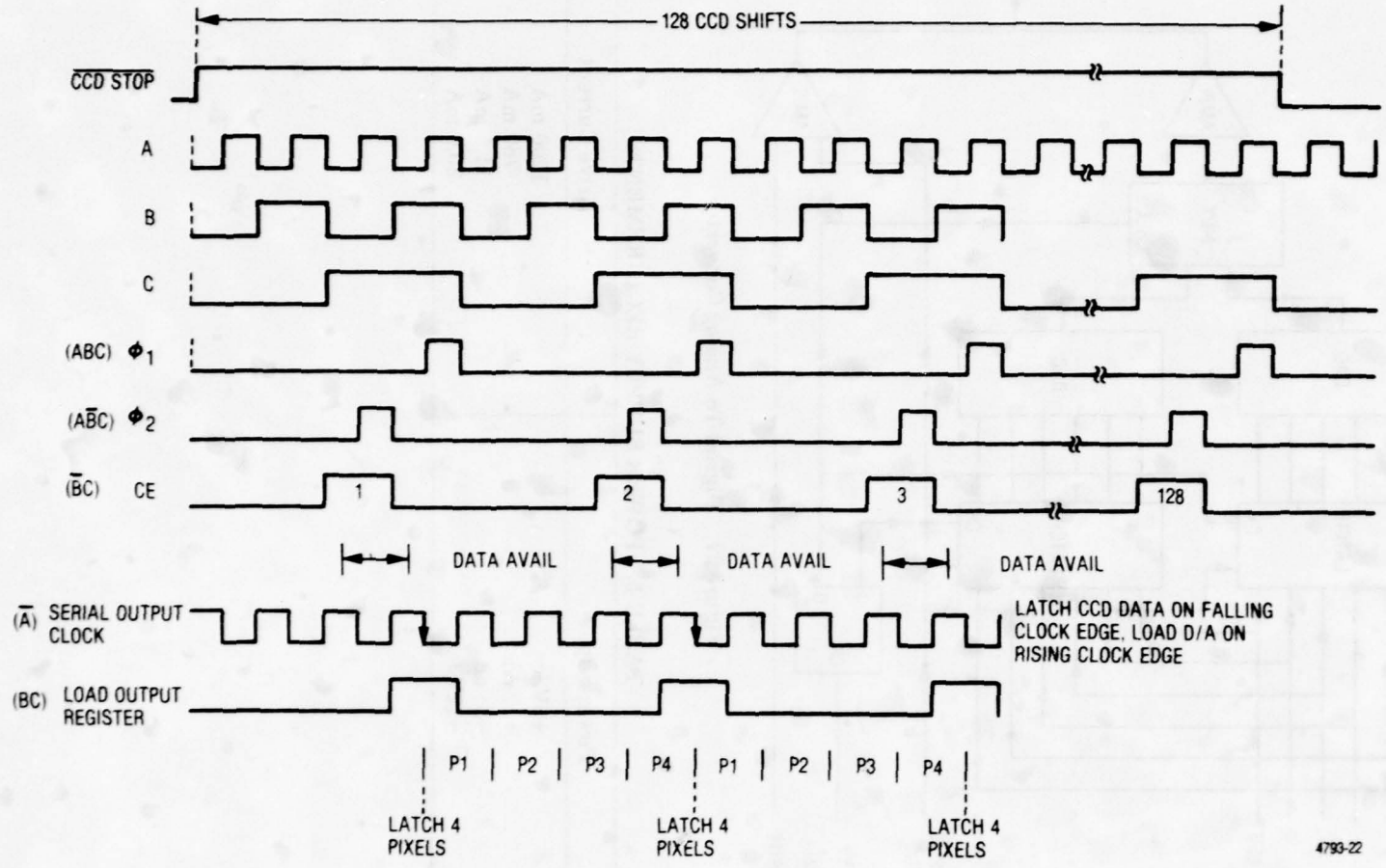

Figure 26. DRM Output Timing

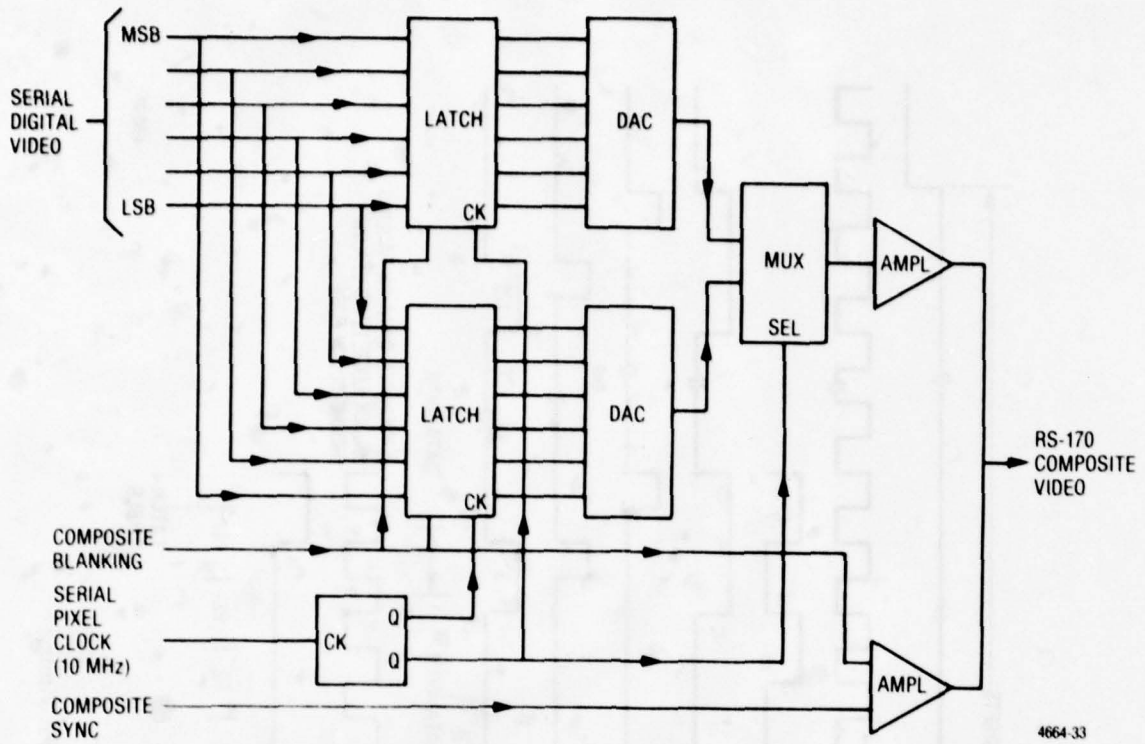

Figure 27. Digital-To-Analog Converter

TABLE 5. POWER SUPPLY REQUIREMENTS

Power Supply	Drive Current
+5Vdc	1200 mA
+12Vdc	780 mA
−5Vdc	11.5 mA
−12Vdc	30.0 mA

TABLE 6. POWER DISSIPATION FOR DISPLAY REFRESH MEMORY

Functional Description	Estimated Power	Technology
Serial-To-Parallel Converter	1.5 W	Low Power Schottky
Input Buffer RAM	0.3 W	MOS
CCD Memory Devices	4.8 W	MOS
Clock Drivers	6.0 W	MOS
Output Serial Register	0.2 W	Low Power Schottky
Control Logic	2.2 W	Low Power Schottky
Interface Circuitry	0.5 W	Low Power Schottky
D/A Converter	0.4 W	Low Power Schottky
TOTAL	15.9 W	

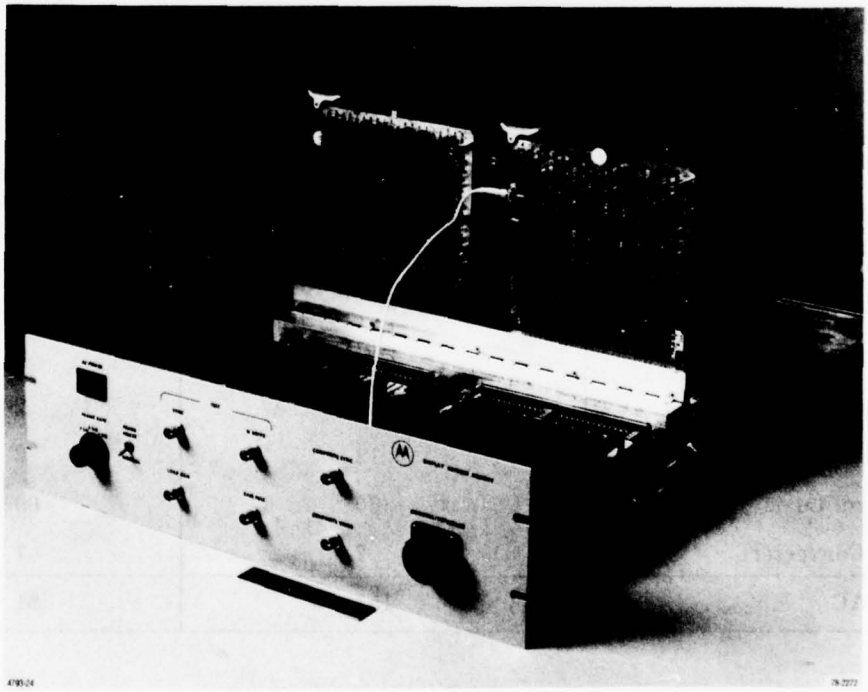

Figure 28. Display Refresh Memory Brassboard Unit

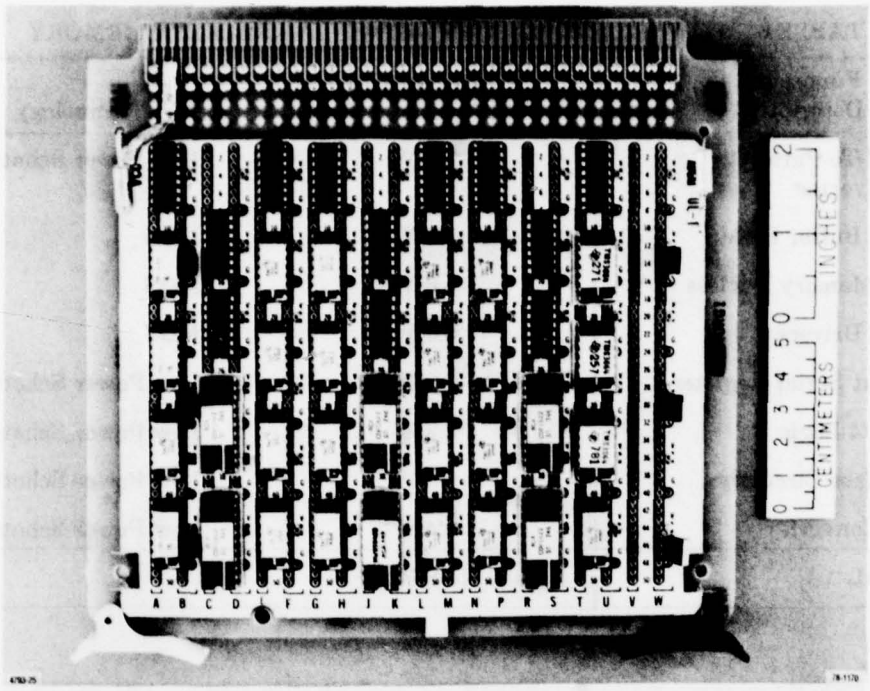

Figure 29. DRM Frame Store Memory Board

TABLE 7. PARTS COUNT FOR DISPLAY REFRESH MEMORY

Functional Description	6 Bits/Pixel Functional Total	No. Parts at 1 Bit/Pixel
Serial-To-Parallel Converter	12	2
CCD Memory Devices	48	8
Clock Drivers	12	2
Output Serial Register	12	2
Control Logic	60	60
D/A Converter	7	7
TOTAL	151	81

c. Self-Test Feature of Display Refresh Memory

The self-test feature generates an eight-level (3-bit) grey scale of 8 vertical stripes as seen on the TV monitor. This mode is selected by connecting the single test connector plug to the Control/ Interface connector located on the DRM front panel, and selecting a 7½ frame per second rate. The associated circuitry for the test pattern generator is located on board A3, and a block diagram of the test circuitry is shown in Figure 30.

The MM4320 TV Sync Generator is allowed to free-run, and a test SYNC signal is generated every fourth real-time TV frame. A three-bit binary counter is used to count the eight fields during these four frames such that one binary count is output throughout an entire field. These three counter bits are routed through the test connector plug back into the three most significant input data bits of the DRM. The three least significant bits are all logic "0" (grounded). A TEST BEGIN NEW PIXEL SET signal is generated every fourth horizontal line time from the MM4320 Sync Generator.

The TV picture pattern, then, will appear as follows:

0	0	0	0	1	1	1	1
0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

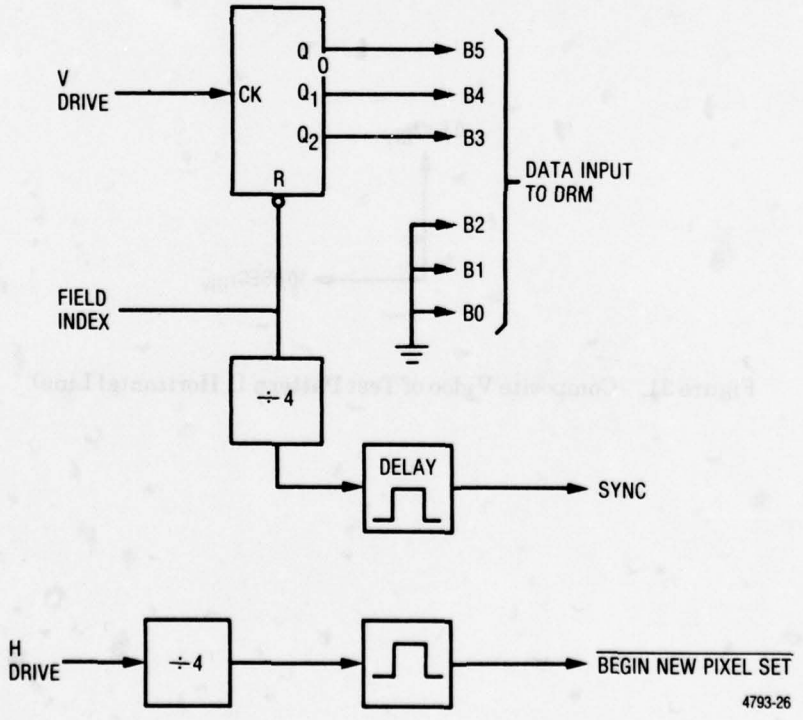

Figure 30. Block Diagram of Test Pattern Generator

This pattern may be shifted (rotated horizontally) by adjusting the TEST SYNC pot on board A3 so that the brightest stripe (111000) just appears at the left side of the picture followed by the darkest stripe. This will allow the DAC output to be observed as it reacts to this 'step' function. A picture of one horizontal line of the test feature exhibiting this mode is shown in Figure 31. A picture of this rotated test pattern is shown in Figure 32.

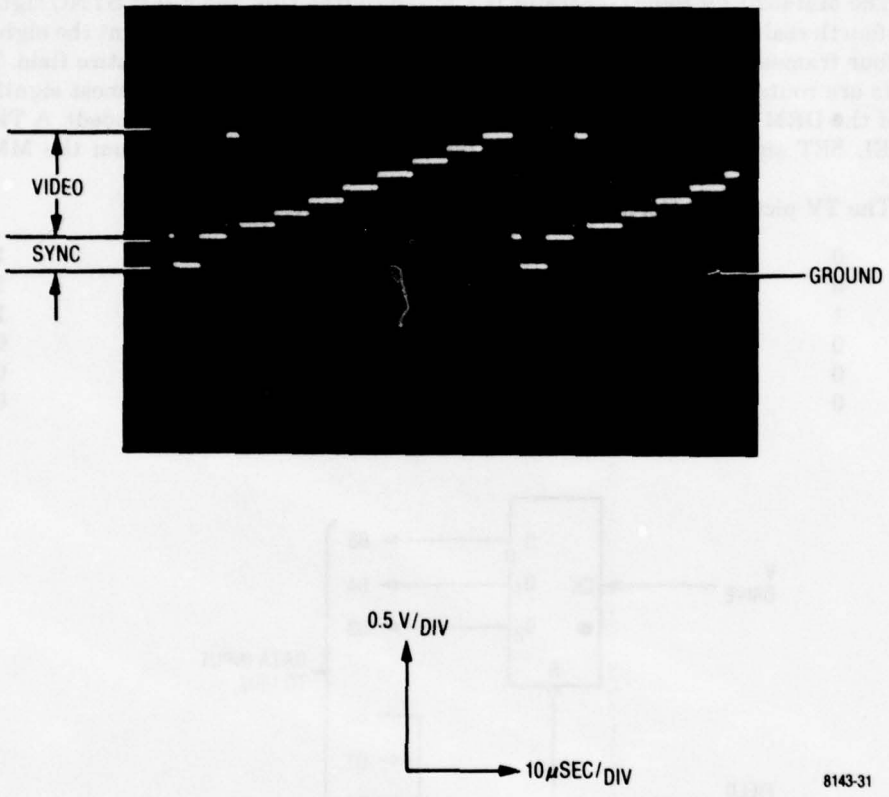

Figure 31. Composite Video of Test Pattern (1 Horizontal Line)

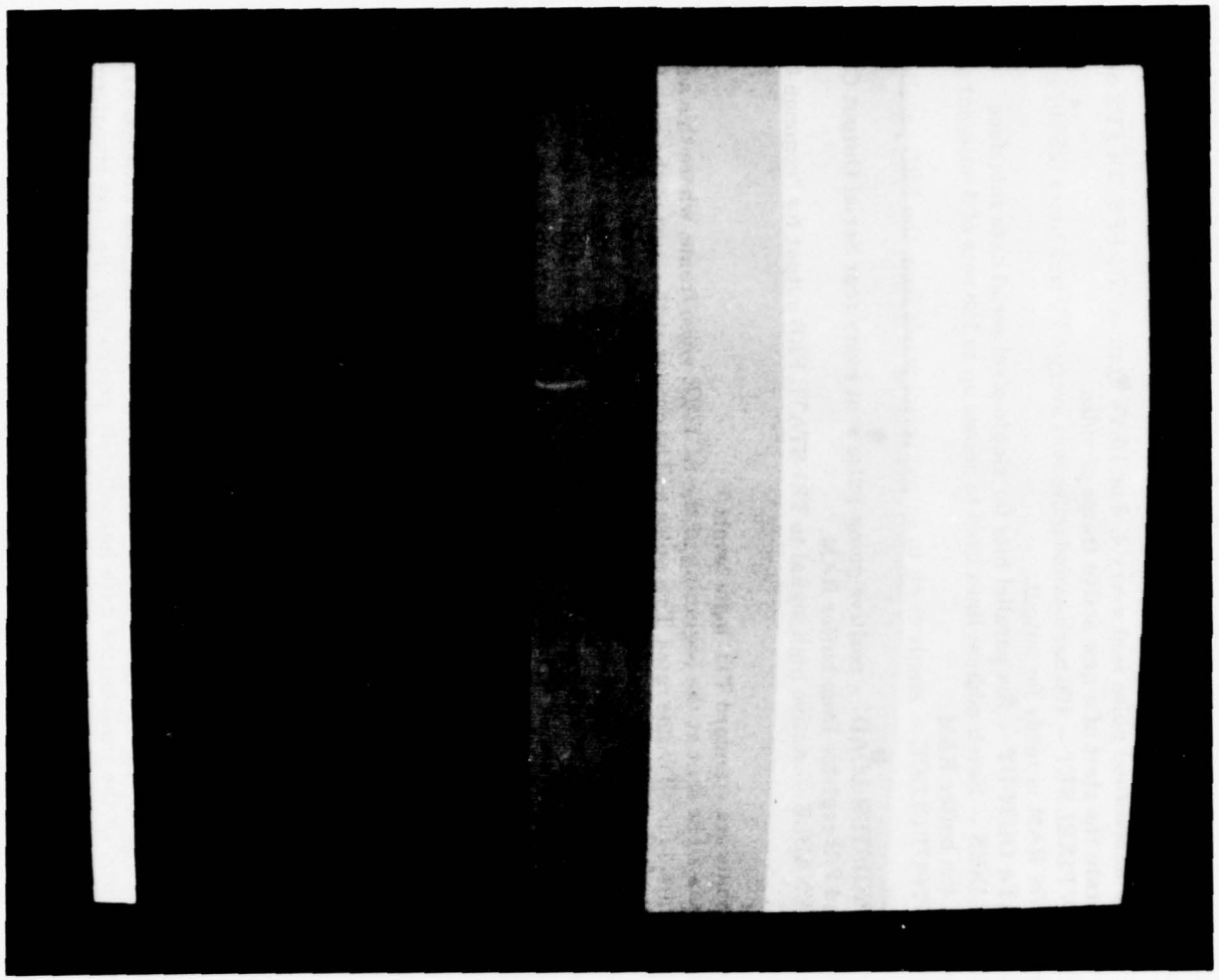

Figure 32. Test Video From DRM

3 EXTERNAL PROCESSOR CONTROL/INTERFACE FOR FRB-DRM OPERATION

The output of the Frame Rate Buffer unit and the input of the Display Refresh Memory unit are designed to allow a bandwidth compression transform processor to be operated between the two brassboard units. The Frame Rate Buffer has the following interface control signals which must be used or generated by the processor:

1. SYNC — 100 nanosecond pulse sent every 4, 8 or 16 TV frames (7½ FPS, 3¾ FPS or 1⅞ FPS) to indicate the start of a new active frame of video.
2. BEGIN NEW PIXEL SET — 100 nanosecond pulse sent every 4 TV line times (253.97 μs) to indicate buffer RAM is ready for output.
3. SERIAL DATA OUTPUT — Six parallel bits for single pixel serial data interface.
4. ADDRESS LINES — Seven address lines used to access up to 128 sets of 4 adjacent pixel groups from the buffer RAM.
5. SERIAL OUTPUT CLOCK — single clock to output serial pixels from the FRB parallel to serial register.
6. OUTPUT REGISTER LOAD — positive-going pulse sent every four Serial Output Clock pulses to load P/S register from buffer RAM.
7. TRISTATE ENABLE — Active high signal to TRI-STATE FRB output for "common bus" operation.

All of these signals are standard TTL logic levels.

The SYNC pulse will be sent at the beginning of the ACTIVE video frame, where this active frame is defined in Figure 4 for all frame rates. This pulse will be output at the start of the even field of the real time TV frame (see Figure 6) since the actual stored video is not available for output until that time. This is because the output data format is specified to be 8x8 frame-oriented blocks, and the stored frame is output in vertical picture stripes according to Figure 9. Each vertical stripe is divided into 64 equal sections, with each section (8 lines by 64 pixels for 7½ FPS) corresponding to one full output buffer RAM. Once a section is ready for output from a RAM, a BEGIN NEW PIXEL SET pulse is transmitted. From this point, the BW compression processor must remove the appropriate pixels (see Table 1) for processing during the next four horizontal line times ($\simeq$ 254 microseconds). These pixels may be removed from the FRB by appropriate RAM addressing, P/S register loading and clocking according to the timing diagram of Figure 16. This asynchronous "hand-shake" mode will allow the processor to perform operations at a continuous or gated rate of one pixel every 100 nanoseconds maximum. The processor may, therefore, extract data from the FRB with clock signals generated from either its own master oscillator or a clock supplied by the FRB. The only constraint is that each FRB buffer RAM, containing 8 lines by 64 pixels of data, must be completely processed before the next BEGIN NEW PIXEL SET pulse, or a maximum time of 254 microseconds. The TRISTATE ENABLE line is held low for normal data output from the FRB, and enabled high to allow "common bus" operation.

Figure 33 shows a block diagram of the processor interface to the FRB and DRM brassboard units. Since the compressed data is assumed to be transmitted over a data link, the FRAME SYNC signal is assumed to be part of the transmitted data immediately preceeding the first transformed data bit of the active video frame. This sync code must, therefore, be detected by the inverse processor to be output to the DRM. The serial data clock must be obtained from the link, and the BEGIN NEW PIXEL SET pulse must be output to the DRM after eight lines of a vertical picture stripe have been inverse processed. The ground processor may operate from a clock furnished by the DRM or from its own internal oscillator since the data input to the DRM may be asynchronous due to the "handshake" mode of operation.

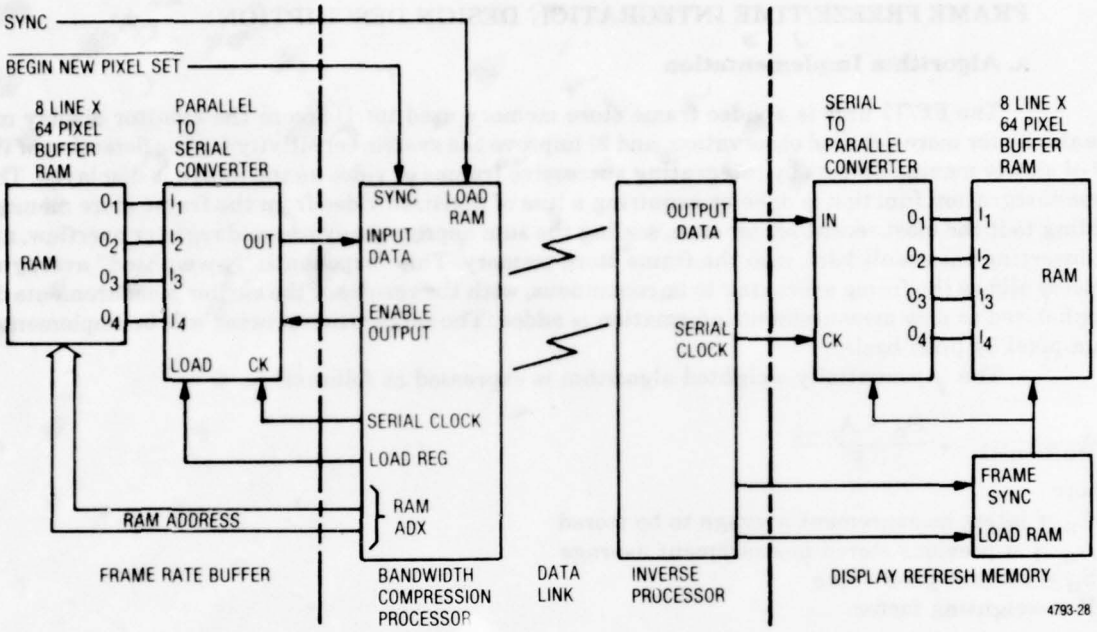

Figure 33. Block Diagram of Bandwidth Compression Processor Interface

The Display Refresh Memory needs the following interface control signals:

1. SYNC — 500 nanosecond pulse sent every 4, 8 or 16 TV frames (7½ FPS, 3¾ FPS or 1⅞ FPS) preceeding the first pixel of a new frame.
2. BEGIN NEW PIXEL SET — 100 nanosecond pulse sent every 4 TV line times ($\simeq$ 254 μs) to indicate a new eight lines of a vertical picture stripe.
3. SERIAL DATA — Six lines of data, corresponding to 6 bits for a single serial pixel.
4. DATA CLOCK — Input clock whose POSITIVE edge may be used to clock stable data into the DRM.

All signals are standard TTL logic levels and are diagrammed in Figure 33.

The SYNC signal is used to select the alternate CCD memory frame in the DRM, as well as reset the TV monitor's control sync to the upper left hand corner of the sweep. This allows the preceeding video frame to be displayed on the monitor and resets all controls for writing the next active video frame into the other CCD memory block. Following the SYNC pulse, there will be a total of 512 x 512 pixels (at 6 bits per pixel) inputted to the DRM to fill this other memory frame. There are 64 BEGIN NEW PIXEL SET pulses sent every field with the total number of these pulses being dependent on the frame rate, as shown in Table 1. The number of pixels to be taken from the inverse processor and then put into the DRM is also shown in that figure.

The serial data lines correspond to a single pixel (at 6 bits per pixel) to be stored in the DRM. The serial data stream is also accompanied by a data clock to strobe a given pixel into the DRM on its positive-going edge. The DRM accepts pixels at either a constant rate, or in bursts up to a maximum of one pixel every 100 nanoseconds. The only constraint is that the required number of pixels be input to the DRM in the 4 horizontal line times (254 μs).

4 FRAME FREEZE/TIME INTEGRATION DESIGN DESCRIPTION

a. Algorithm Implementation

The FF/TI unit is a video frame store memory used to: 1) freeze the monitor display momentarily for more detailed observation, and 2) improve the system sensitivity for the detection of fixed or slowly moving objects by integrating successive frames of video as the image is displayed. This time integration function is done by acquiring a line of digitized video from the frame store memory, adding to it the most recent sensor scan, scaling the sum appropriately to avoid register overflow, and re-inserting the result back into the frame store memory. This "exponentially-weighted" averaging process allows the frame averaging to be continuous, with the results of the earlier measurements de-emphasized as new measurement information is added. The integration process will be implemented on a pixel by pixel basis.

The exponentially-weighted algorithm is expressed as follows:

$$A_n = A_{n-1} + \frac{S_n - A_{n-1}}{F}$$

where

A_n = latest measurement average to be stored
A_{n-1} = previous stored measurement average
S_n = current pixel value
F = weighting factor

So the difference between the previous stored value and the current real time pixel value is scaled by F and then added to the previous stored value to obtain the new video sample value. From the equation a small value of F will cause the displayed video to respond quickly to changes in S_n. Larger values of F will cause the displayed video to adapt slowly to changes in S_n. The FF/TI is designed for F = 16 so that the divide will consist of a four-bit shift. A block diagram of the algorithm is shown in Figure 34.

With F = 16, a computer program was run to check the transient response of the algorithm to an input step function of a full scale pixel value (128) to a zero-value average measurement. This resultant steady-state average value was then processed with a zero-value pixel. The results are shown in Appendix B. These tabulated values, representing the actual video average measurement, indicate that no additional sign bit is needed for proper algorithm operation. Since these average measurements are conducted on a pixel by pixel basis, the entire algorithm must be implemented in one real time pixel increment. This means that the output video display, coming from the previous measurement sample, will essentially be one frame sample behind the real time averaged value.

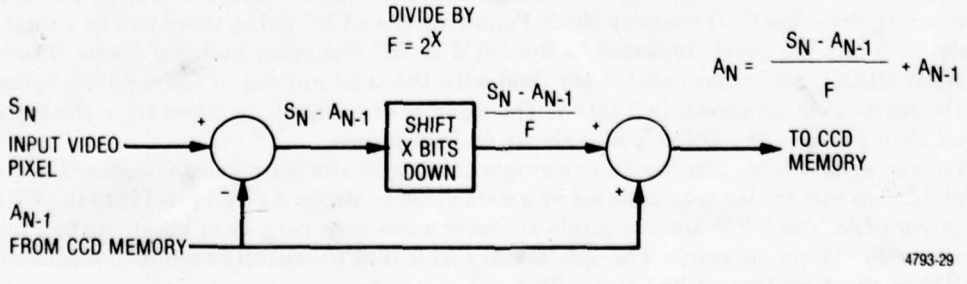

Figure 34. Implementation of Exponential Averaging Algorithm

b. FF/TI Design Description

Figure 35 shows a block diagram of the Frame Freeze/Time Integration unit. This is a complete system which may snatch a frame of video, digitize it, store it, and then read it out continuously through D/A converter to a standard 525 line NTSC compatible RS-170 format display. This unit may also add together successive frames on a pixel for pixel basis while the sum is continuously being updated on a TV monitor. These two unique functions, along with the normal mode of real time display of consecutive stored frames, are under pushbutton control of a display operator.

The design of the FF/TI unit makes extensive use of the frame store memory module of the two brassboard units. The input video from a TV camera is adjusted to proper operating levels by a video amplifier and then digitized to 6 bits per pixel through a high speed sample/hold and A/D converter. These serial pixels are then converted to a four-pixel-wide bus by a serial-to-parallel converter. A high speed adder is next used to perform one of two functions. Under a normal display, the input pixels are added to zero, and stored in the CCD memory unchanged from their original values. Since these pixels are input in a standard field organized frame, the CCDs are organized exactly as the Display Refresh Memory shown in Figure 24. At the same time an input pixel is written into the CCD memory, the previous value is read from the CCDs and displayed on a monitor through a D/A converter. Since both the TV camera and TV monitor receive the same synchronizing signal from the FF/TI unit, the relative sensor sweeps are located in exactly the same location. This completely synchronous operation reduces the complexity of the controlling hardware but means that the displayed video is exactly one frame behind the real time TV camera video.

If the Frame Freeze function is selected, the memory operates exactly the same way. A pixel is read from the CCD memory and output to the D/A converter for display. At the same time, that pixel is latched into a register and fed back to the input adder. In this mode, that feedback pixel is added to zero (the most recent input pixel from the camera is ignored) and then stored back into its same CCD location. This READ-MODIFY-WRITE operation causes the video in the CCD memory to retain its original value, and the monitor display will effectively be frozen with one frame of video. As soon as this function is removed, the most recent TV camera video frame will be stored in memory and displayed the following frame.

The Time Integration mode of operation is almost unchanged from the Frame Freeze mode. As a pixel is read out of the CCD memory, it is simultaneously displayed on the TV monitor. This pixel is also latched into the feedback register and presented to the input adder. This pixel is then subtracted from the most recent TV camera pixel from the A/D converter. This difference is next shifted down four bits (divided by 16), added to the present output pixel, and stored back into the CCD memory. This completes the integration algorithm of one pixel of video. The process is actually implemented on four parallel pixels, with a resolution of 10 bits per pixel (F = 16). The output video to the D/A converter will consist of the six most significant bits from a given pixel value.

Since four parallel pixels must be averaged in four real time pixel increments, the timing sequence is very critical. Figure 36 shows a sample timing diagram of the algorithm execution. The actual hardware operation will require careful scrutiny, but the diagram shows that, typically, enough time is available for the entire process.

The D/A converter to be used with the FF/TI unit is the same as that described for the Display Refresh Memory in paragraph 2a. The parts count for the Frame Freeze/Time Integration unit will be comparable to the Frame Rate Buffer unit except four more bit planes of CCD memory with associated drivers and output latches must be included. The power estimate for the FF/TI unit is expected to be about 15 watts. The push-button mode controls are clocked with the sync generator Field Index pulse so that a newly selected mode will begin with the next full video frame so that no glitches or blank spots will be detected on the monitor display.

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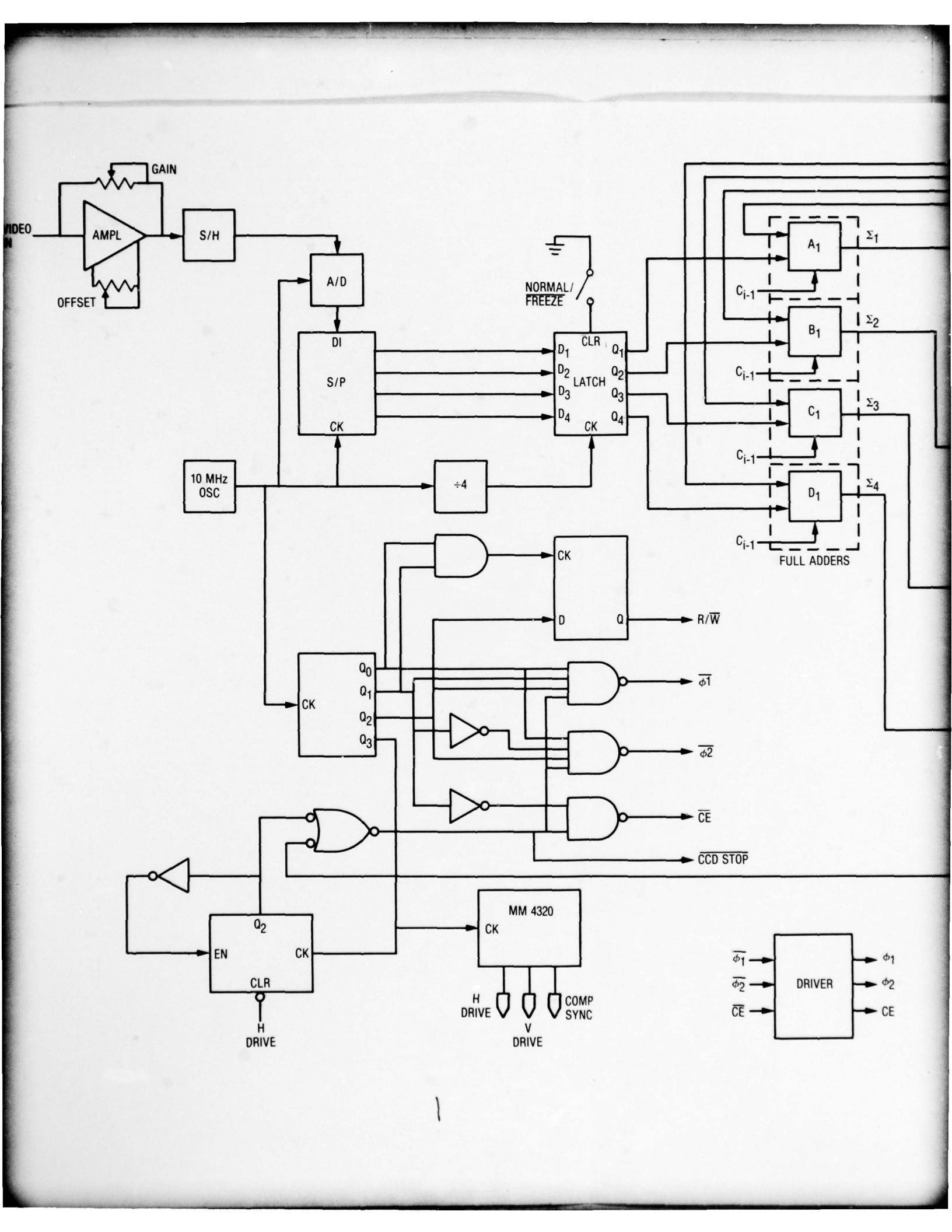
GAIN
AMPL
OFFSET
S/H
A/D
DI
S/P
CK
NORMAL/
FREEZE
CLR
D1
D2
D3
D4
LATCH
Q1
Q2
Q3
Q4
CK
A1
B1
C1
D1
Σ1
Σ2
Σ3
Σ4
Ci-1
FULL ADDERS
10 MHz
OSC
÷4
CK
D
Q
R/W
Q0
Q1
Q2
Q3
φ1
φ2
CE
CCD STOP
Q2
EN
CK
CLR
H
DRIVE
MM 4320
CK
H
DRIVE
V
DRIVE
COMP
SYNC
DRIVER
φ1
φ2
CE

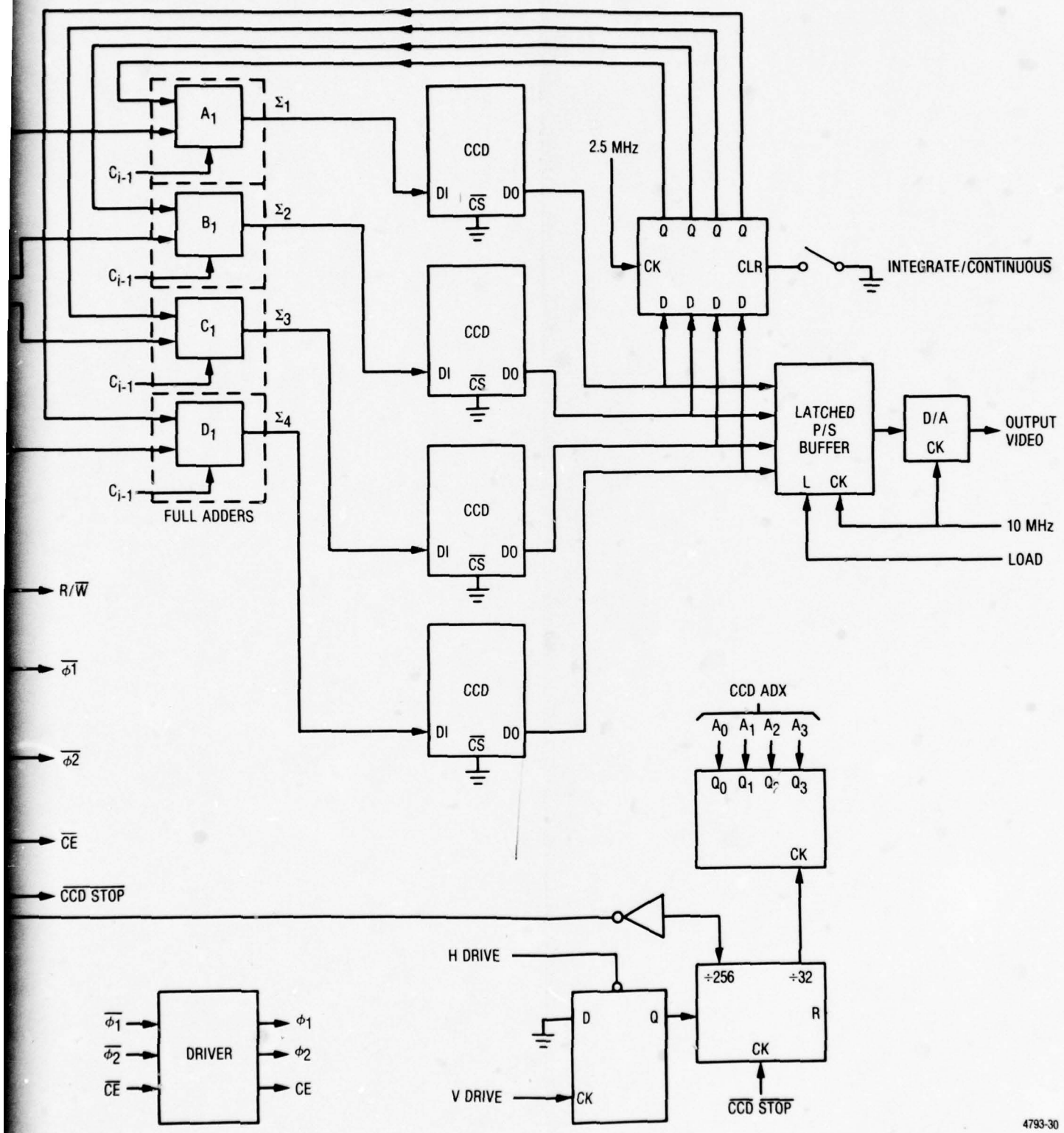

Figure 35. Frame Freeze/Time Integration Block Diagram

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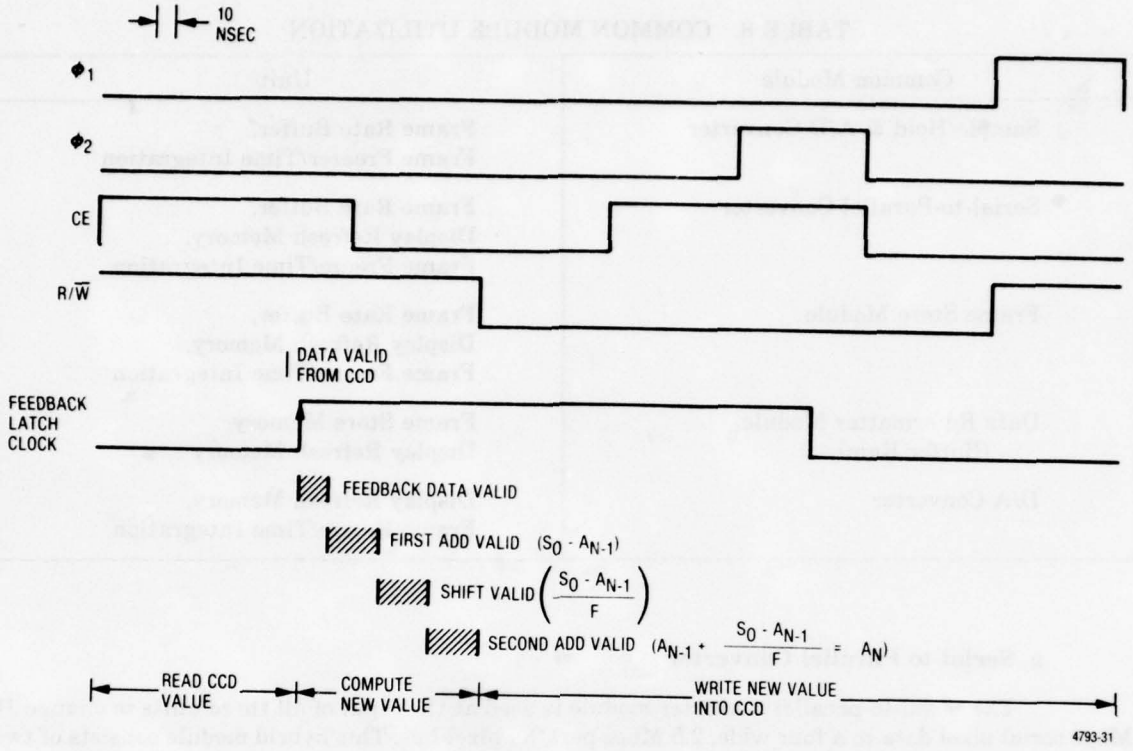

Figure 36. Timing Sequence for Algorithm Implementation

5 COMMON MODULE PARTITIONING

The Frame Rate Buffer, Display Refresh Memory and Frame Freeze/Time Integration units are designed to utilize common functional blocks. These blocks are implemented in discrete functional modules which perform identical operations in each unit. A list of the modules, along with the units which incorporate a particular module, is shown in Table 8. These modules are realized with discrete hardware so that one functional block is required for each bit per pixel (bit plane segmented). This modular packaging approach will allow each functional module to be reduced to a high density form (hybrid packaging or full wafer LSI). The following sections completely define each module with respect to function, data I/O format, and power supply/control interface. An approximate hybrid package size is listed for some of the modules.

TABLE 8. COMMON MODULE UTILIZATION

Common Module	Unit
Sample/Hold & A/D Converter	Frame Rate Buffer, Frame Freezer/Time Integration
Serial-to-Parallel Converter	Frame Rate Buffer, Display Refresh Memory, Frame Freeze/Time Integration
Frame Store Module	Frame Rate Buffer, Display Refresh Memory, Frame Freeze/Time Integration
Data Reformatter Module (Buffer Ram)	Frame Store Memory, Display Refresh Memory
D/A Converter	Display Refresh Memory, Frame Freeze/Time Integration

a. Serial to Parallel Converter

The serial-to-parallel converter module is used at the input of all three units to change 10 Mbps serial pixel data to a four wide, 2.5 Mbps parallel pixel bus. This hybrid module consists of two 54LS175 low power Schottky, positive edge-triggered latches, and one module is required for each bit per pixel of digitized video resolution. Figure 37 shows an interconnect of this module. Input data S1 is input to the first group of latches, and ripples through this register at the input clock rate. The input pixels are clocked through this serial shift register on the low to high transition of the clock. The LATCH signal is used to clock every four pixels in the serial register to the four wide output bus. The LATCH clock is made by simply dividing the input CLOCK by 4. The four output pixels are then stable for four input data time segments. The expected power dissipation of this module is typically 120 mW. The module itself will have only 9 output pins, with all inputs and outputs TTL compatible. Each input represents one half of a unit TTL load, and each output is capable of driving 10 unit TTL loads.

b. Frame Store Module

The frame store module consists of one bit plane of CCD memory with associated clock drivers and data latches. This module is also used in the FRB, DRM and FF/TI. Figure 38 shows the interconnect for this module. There are seven chips associated with the frame store module. Four 64K CCD memory devices, which correspond to one bit plane of memory in all three units are required. There is a MOS clock driver to interface the TTL phase clocks and chip enable to the CCDs. Also, an input/output data latch and output parallel-to-serial converter are contained in the module. These last two chips allow the memory outputs to be interfaced to the re-formatter module in the FRB or directly to the D/A converter in the DRM or FF/TI. All inputs represent one unit TTL load factor except the data input lines which represent 1½ unit loads. All inputs and outputs are TTL compatible. The power dissipation of this module is estimated to be about 1 watt. There are 26 output pins required for interfacing, and the hybrid size will be a 1 inch x 1 inch package.

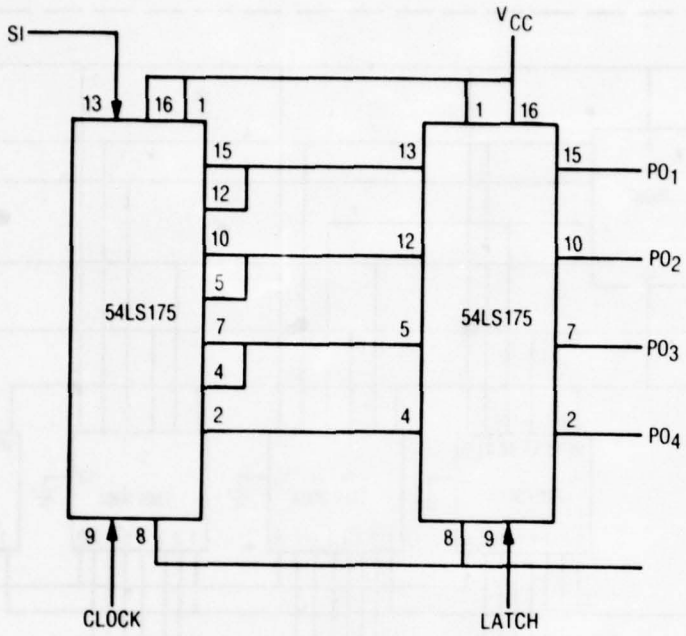

Figure 37. Serial/Parallel Converter Hybrid

c. Data Re-Formatter Module

The data re-formatter, or buffer RAM module is used in the FRB and DRM units for interlacing or de-interlacing field oriented horizontal video lines. This module consists of two 256x4-bit silicon-on-sapphire MOS RAMs and a low power Schottky Tristate parallel-to-serial converter. One of these modules is needed for each bit per pixel in each of the two brassboard units. The maximum read or write cycle time of the RAM is 400 nanoseconds, with the output serial data being available at 10 Mbps. Figure 39 shows the interconnect for the data re-formatter module. All inputs and outputs are TTL compatible. All control lines of the RAMs are brought out as part of the 34 I/O pins so that each RAM may be operated independently. The total power dissipation is about 225 mW.

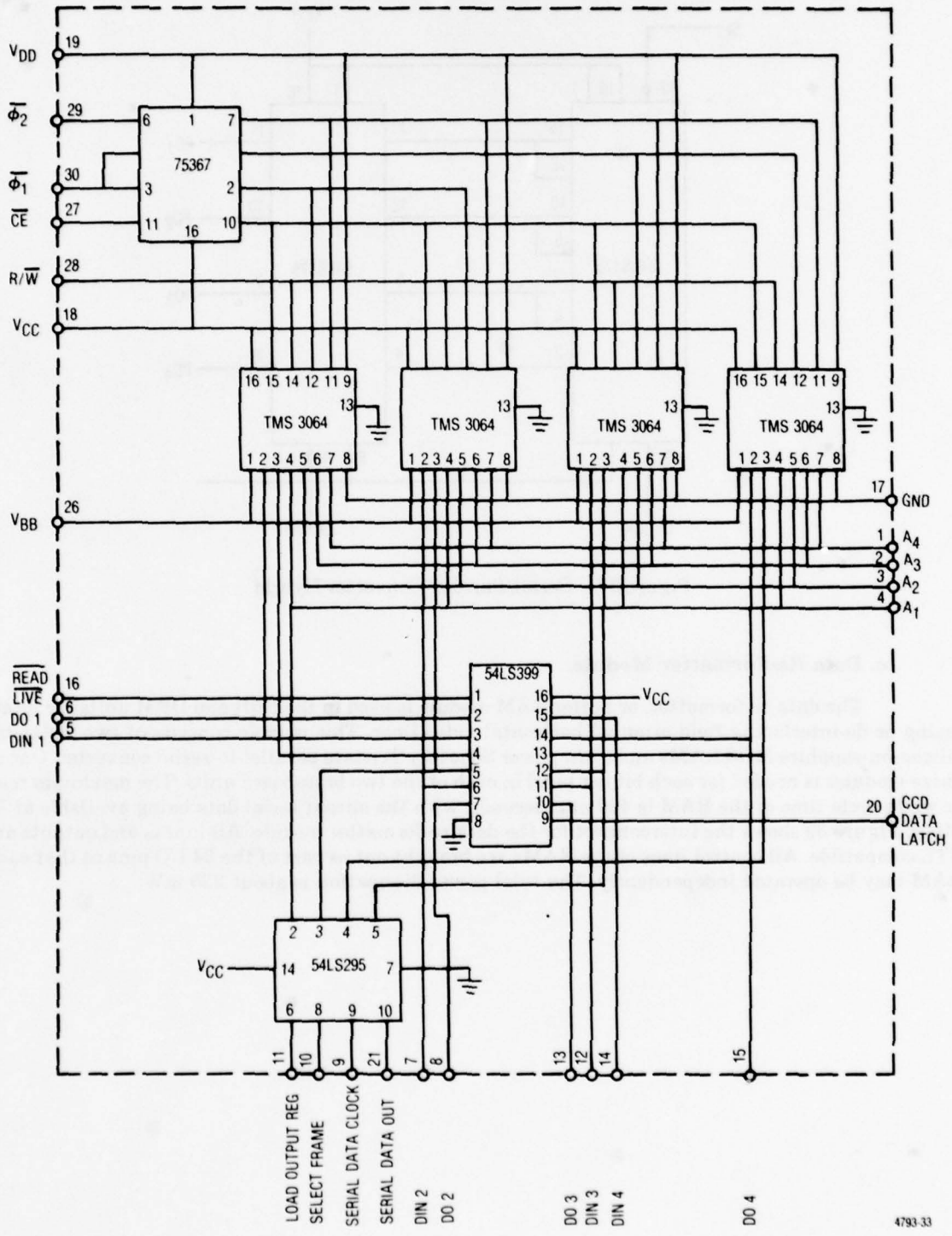

Figure 38. Frame Store Hybrid Interconnect

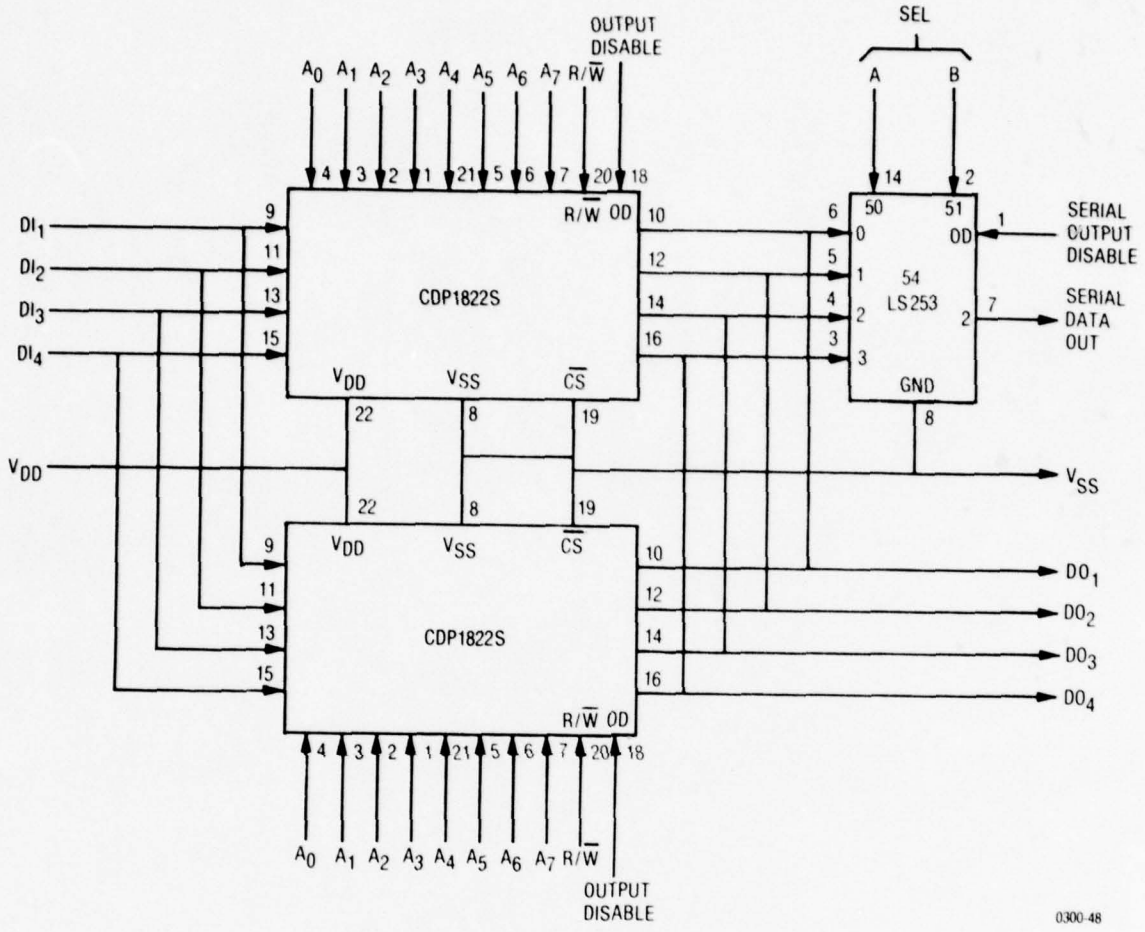

Figure 39. Data Reformatter Module

d. Digital to Analog Converter Module

The D/A converter is used with the DRM and FF/TI units. This module accepts up to 8 bits per pixel along with a serial pixel clock, composite sync and composite blanking to output standard RS-170 video. Figure 40 shows the schematic of the D/A converter. Each of the input timing signals presents a factor of 1 TTL unit load. The discrete output buffer is used as a summing amplifier and 75 ohm driver. There are only 15 interface pins to the module, and the total power dissipation is about 400 mW. This module will be packaged in a ½ inch x ½ inch flat pack.

e. Backplane Module

There will be a separate backplane module for each of the three units. Each module performs a similar function of unit synchronization and control, but each backplane module contains circuitry unique to its own particular unit. Each unit will utilize 3 backplane modules to accommodate the pinouts and power dissipation.

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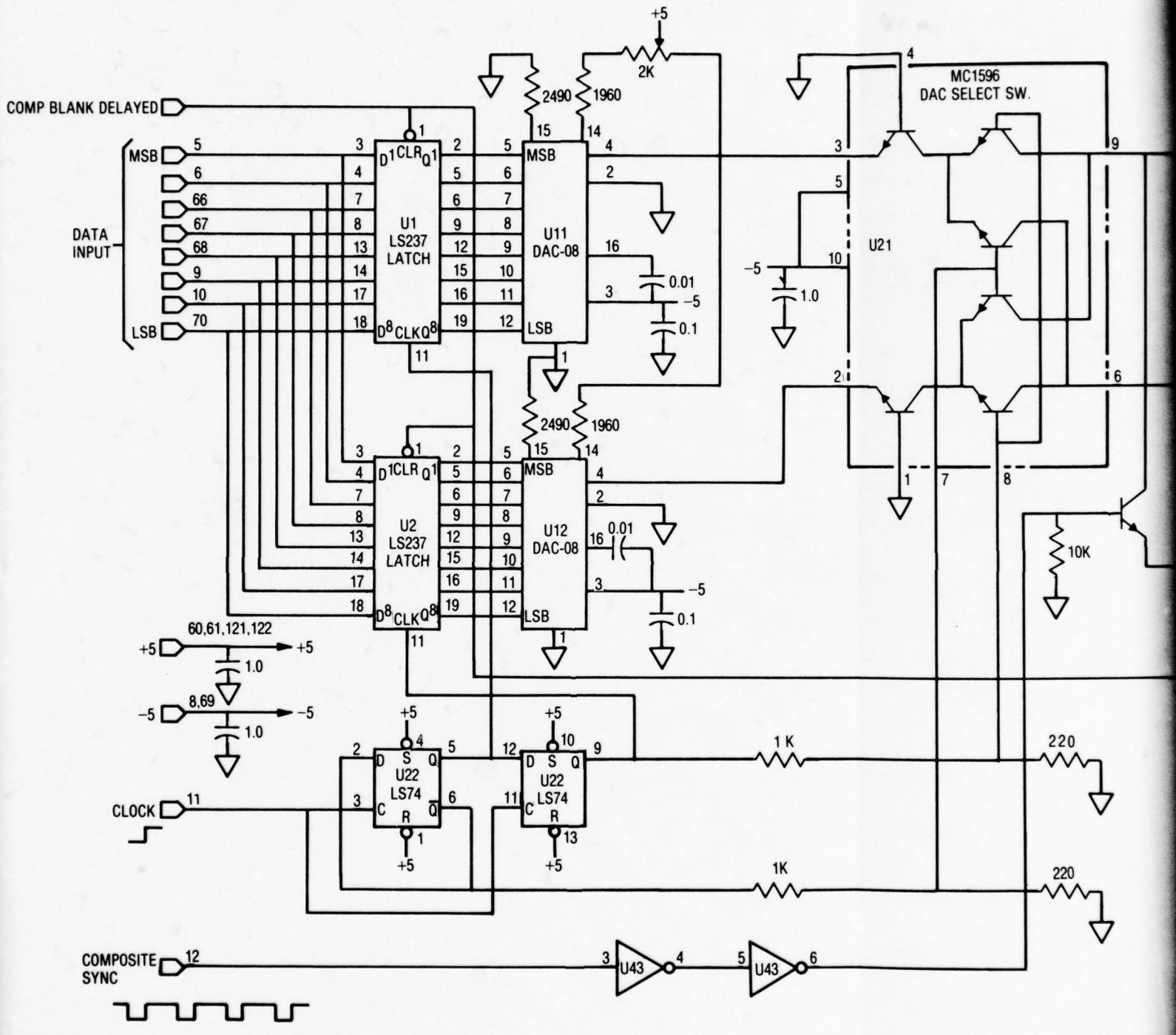
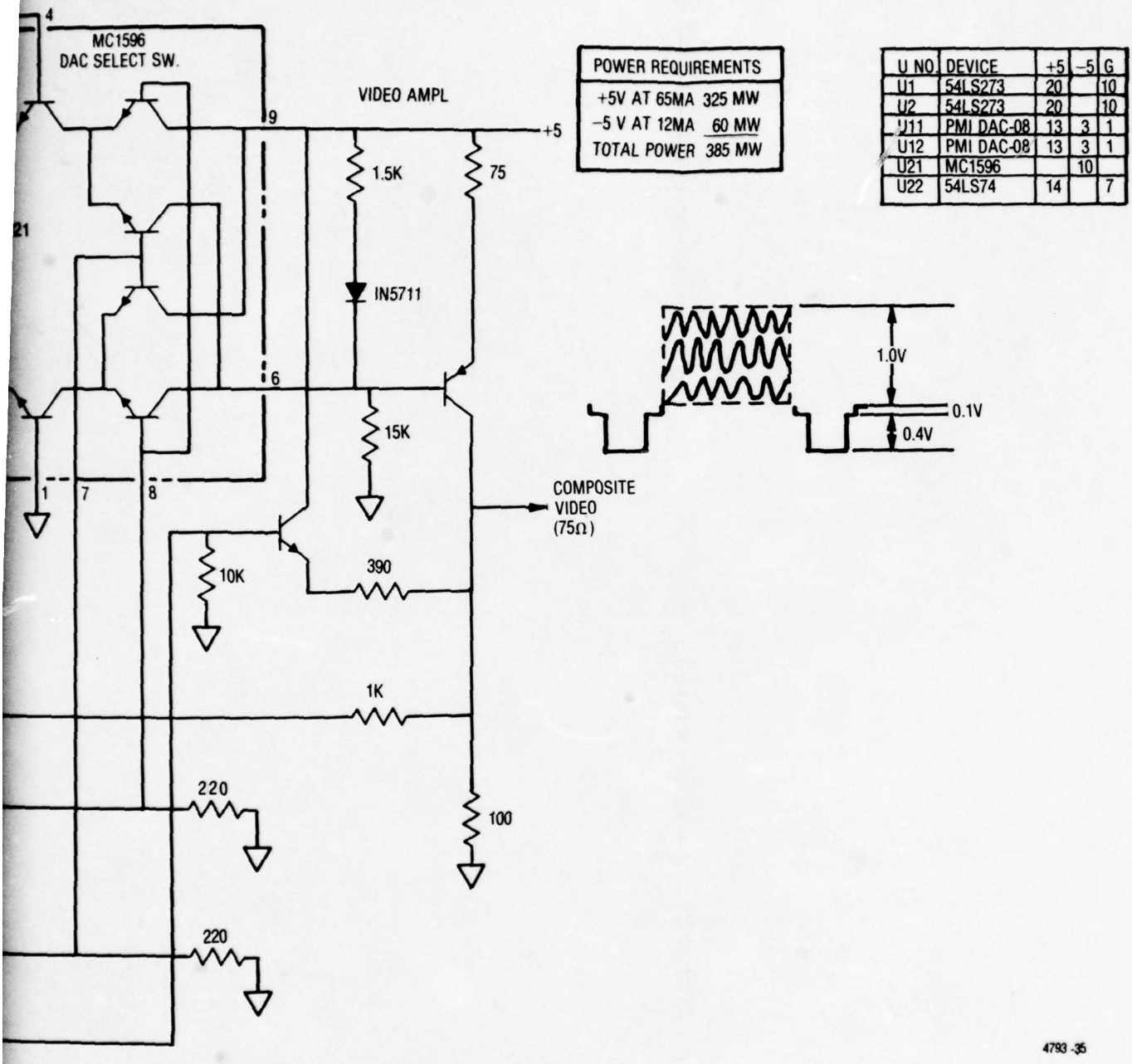

COMP BLANK DELAYED
DATA INPUT
MSB
LSB
U1 LS237 LATCH
U2 LS237 LATCH
U11 DAC-08
U12 DAC-08
2490
1960
2K
0.01
0.1
1.0
MC1596 DAC SELECT SW.
U21
10K
60,61,121,122
8,69
CLOCK
U22 LS74
1 K
220
1K
COMPOSITE SYNC
U43



POWER REQUIREMENTS
+5V AT 65MA 325 MW
−5 V AT 12MA 60 MW
TOTAL POWER 385 MW

U NO	DEVICE	+5	−5	G
U1	54LS273	20		10
U2	54LS273	20		10
U11	PMI DAC-08	13	3	1
U12	PMI DAC-08	13	3	1
U21	MC1596		10	
U22	54LS74	14		7

Figure 40. 8-Bit Digital-To-Analog Converter with Composite Video Output

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6 UNIT FABRICATION USING COMMON MODULES

a. Frame Rate Buffer Common Module Design

The Frame Rate Buffer may be implemented by interconnecting the previously defined common modules. A sample-hold and A/D converter are required to digitize the incoming video. A serial to parallel module is needed for each required bit per pixel. The output of this module is used as the input to the frame store module (CCD memory module). This output is connected to the input of the data re-formatter (buffer RAM) module to obtain the 8x8 block output sequence. The data re-formatter output is therefore the required FRB serial output data bus. All of these common modules are synchronized by three backplane modules. An interconnect diagram showing how these modules will be used is given in Figure 41. This diagram is shown for 6 bits per pixel.

The power dissipation of 13 watts including the A/D and S/H can be easily handled with a 5 x 7 inch multi-layer circuit board. A possible layout for the miniaturized Frame Rate Buffer unit is shown in Figure 42. The multi-layer board will contain a copper ground plane of sufficient thickness to spread the heat over the entire board area. The board rails then conduct the heat to the FRB enclosure.

b. Display Refresh Memory Common Module Design

The Display Refresh Memory may be implemented using the common modules. There will be a serial-to-parallel converter and data reformatter (buffer RAM) module required for each bit per pixel of resolution. Since there are two complete frames of CCD memory in the DRM, twice as many (12 total) frame store modules as were used in the FRB are required in the DRM. The two frame memories are wire-ored into the D/A converter module to output RS-170 video to a TV monitor. There are four unique backplane modules to synchronize the individual function modules. Figure 43 shows the interconnect required for a common module DRM.

The Display Refresh Memory modules will dissipate approximately 16 watts in the configuration shown. The modules may be housed on two 5 x 7 inch multilayer circuit boards as diagrammed in Figure 44. These two boards have a copper ground plane to distribute the heat over the entire board surface area.

c. Frame Freeze/Time Integration Common Module Design

The FF/TI unit requires only the serial-to-parallel converter, frame store, and D/A converter common modules for its construction. In addition to the two unique backplane modules, this unit also requires a unique adder module to implement the exponential averaging algorithm. This adder module is located between the input serial-to-parallel converter and the CCDs. Figure 45 shows a common module interconnect to implement the Frame Freeze/Time Integration system.

Based upon the power measurements of the Display Refresh Memory, the FF/TI unit is expected to require about 21 watts. The packaging for this system would require two or three 5 x 7 inch multilayer circuit boards.

7 TEMPERATURE DATA

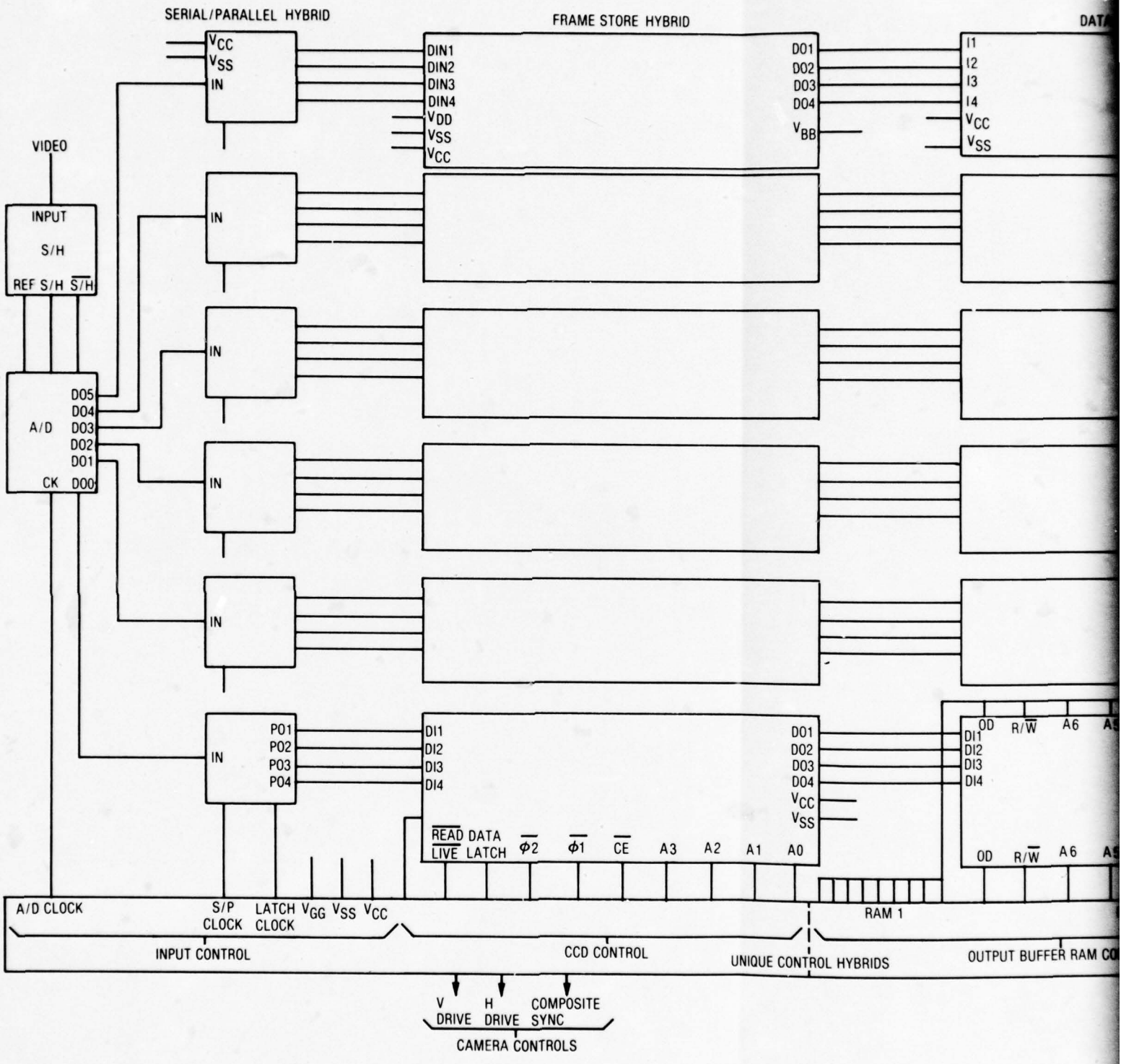
Prior to the award of the AFAL Video Memory Modules contract, Motorola conducted extensive temperature tests on a prototype 0.400 inch 64K CCD device from TI. The tests consisted of measuring power consumption, bit errors as a function of stop time, and bit errors as a function of shift rate. A special test fixture was fabricated to simulate the timing for the CCD that was later used in the AFAL brassboard units.

The first part tested exceeded the upper operating temperature limit by 15 degrees C (proper operation to +85 degrees C). Another test, attempting to determine if the CCD could operate at speeds greater than 5 MHz, could not be run since the MOS clock driver performance degraded due to the small shift clock widths. A second TI part was subjected to an abbreviated test, but operated comparably with the first device. It was concluded from these tests that the AFAL brassboard units would have no trouble operating at the contract design goal of +49 degrees C (TI specification states a lower limit of 0 degree C), and no bit errors were detected even with a pause time twice as great as the TI specification of 1 millisecond.

One very important operating peculiarity was noted during this preliminary CCD testing. It was observed under all temperature settings that the CCD operation was somewhat insensitive to various power supply settings. Even though the TI specification stated a tolerance of ± 10 percent, the actual voltages were varied ± 25 percent without producing bit errors. The sensitivity of the CCD device to high frequency transient noise on the power supply lines was most noticeable, however. For this reason the power supply lines were decoupled on every memory device for the AFAL brassboard units. This precaution was well worth its effort since no problems were encountered on either brassboard unit that could possibly be attributed to power supply glitches.

Upon completion of the video memory system hardware testing, the Frame Rate Buffer was temperature tested in a heat chamber to determine overall unit performance. An alternate dark-light vertical bar pattern was input to the FRB. The FRB output was run out of the chamber to the DRM (actual system configuration) so that the pattern and subsequent temperature-induced errors could be observed on a TV monitor.

In the exploratory temperature sweep, the FRB operated only to +50 degrees C before the output data became invalid (as observed on the monitor). The unit exhibited almost a step function response since the output, being good at one temperature, became totally unrecognizable with an incremental temperature increase. This symptom indicated that the problem did not lie with the CCDs, but rather with some externally generated timing signal. Further testing revealed extreme temperature-related delays from a CMOS counter. This part was replaced with a functionally compatible low power Schottky device, and the temperature test was rerun.


SERIAL/PARALLEL HYBRID
FRAME STORE HYBRID
VIDEO
INPUT
S/H
REF S/H S/H
A/D
CK
IN
DIN1
DIN2
DIN3
DIN4
VDD
VSS
VCC
DO1
DO2
DO3
DO4
VBB
I1
I2
I3
I4
PO1
PO2
PO3
PO4
DI1
DI2
DI3
DI4
READ DATA
LIVE LATCH
φ2
φ1
CE
A3
A2
A1
A0
OD
R/W
A6
RAM 1
A/D CLOCK
S/P CLOCK
LATCH CLOCK
VGG
INPUT CONTROL
CCD CONTROL
UNIQUE CONTROL HYBRIDS
OUTPUT BUFFER RAM CO
V DRIVE
H DRIVE
COMPOSITE SYNC
CAMERA CONTROLS

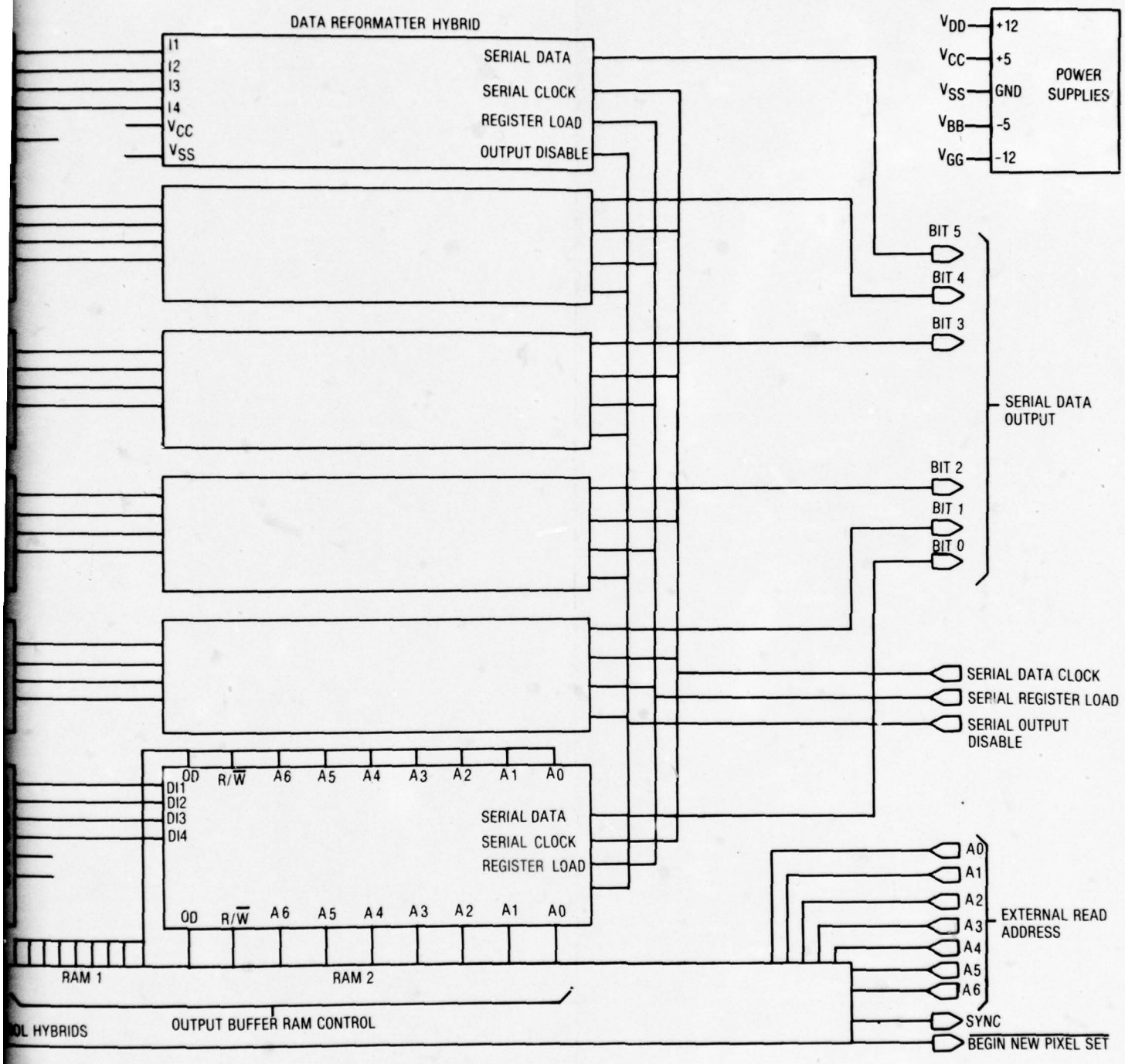


Figure 41. Frame Rate Buffer Hybrid Interconnect

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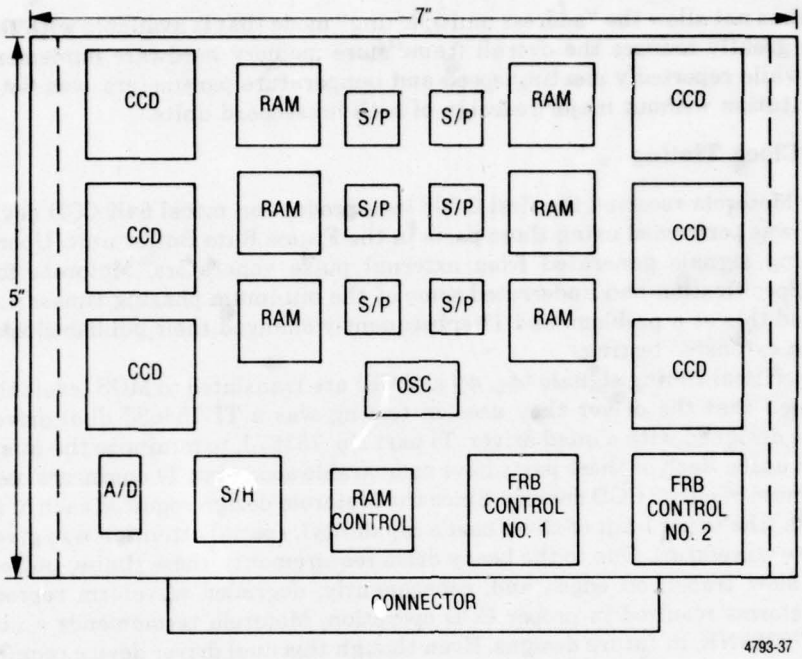


Figure 42. Frame Rate Buffer Miniaturized Package Concept

This second temperature test produced outstanding results. The FRB worked well to approximately +70 degrees C when a few short vertical bars began to appear. This effect is attributed to actual temperature-induced random CCD bit errors. The ambient temperature was then increased to +85 degrees C. At this temperature more lines were visible on the monitor, but the picture was still easily recognizable. At low temperatures, the FRB worked perfectly to about −25 degrees C when symmetric dots began occurring on the edges of the dark vertical bars. At −45 degrees C the black vertical bars began looking like punched paper tape, but video was not completely lost until a few degrees lower. In general, the FRB exhibited no bit errors over the temperature range −25 degrees C to +70 degrees C. Appendix C summarizes the temperature tests performed with the Frame Rate Buffer and includes some sketches to aid in visualizing the actual error effects observed on the monitor.

8 PROBLEMS AND RECOMMENDATIONS

a. CCD Parts Delivery

Texas Instruments is having its own problems with the 64K CCD device. Motorola received 0.400 inch prototype parts in July, 1977 for engineering evaluation with the standard 0.300 inch production parts to follow in November, 1977. The first production parts were not delivered until January and February, 1978 and then only ¾ of the order was filled. The AFAL brassboard testing illuminated some device sensitivities, and TI slipped all parts deliveries to May because of "timing difficulties." In June, TI stated there was a high speed-high temperature operating problem with the 0.300 inch production parts, and delivery of the full temperature devices was postponed until September, 1978.

Because of the delivery problems with the TI part, Motorola also investigated using a Fairchild 64K device, part number CCD464. The specifications for this part are given in Appendix D. Since two more shift clocks are required for this device's operation, more control circuitry is needed.

Also, Fairchild does not allow the "address multiplexing" mode that is available with the TI part. This operating mode greatly reduces the overall frame store memory hardware implementation, so the Fairchild part, while reportedly meeting speed and temperature parameters, was not considered an expedient substitution without major redesign of both brassboard units.

b. CCD Clock Timing

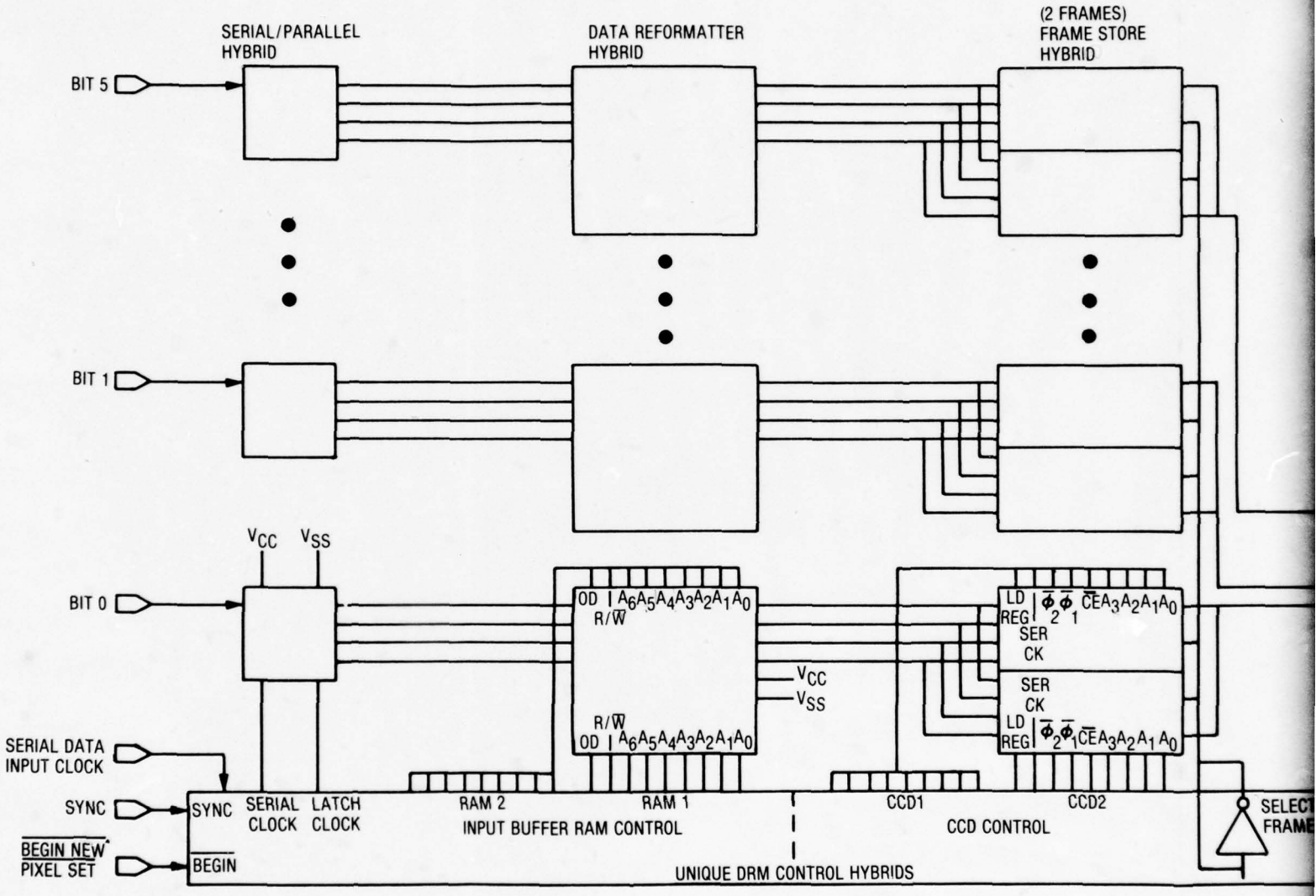
After Motorola received the first 0.300 inch production model 64K CCD devices, extensive troubleshooting was performed using these parts in the Frame Rate Buffer unit. Upon testing these parts with timing signals generated from external pulse generators, Motorola found that the preliminary TI Specification had underrated some of the minimum phasing times. A check with TI engineers verified this as a problem, and TI subsequently changed their published specification following their own extensive testing.

These critical timing signals ($\phi 1$, $\phi 2$ and CE) are translated to MOS levels through a clock driver. TI revealed that the driver they used in testing was a TI 75363J dual driver. The AFAL brassboards were designed with a quad driver, TI part No. 75367J, to minimize the number of devices in the fabricated units. Each of these parts have comparable specs, but TI engineers used their driver to power a maximum of only 3 CCD devices. Since the Motorola design required each of the 75367Js to drive 4 CCD parts (the upper limit of these part's capability), special attention was given to the MOS level timing pulse waveforms. Due to the heavy drive requirements, these timing pulses were seen to have relatively slow transition edges and, consequently, degraded waveform reproduction. Even though the waveforms resulted in proper CCD operation, Motorola recommends a new MOS clock driver, part No. 75363NE, in future designs. Even though this dual driver device requires more parts per frame store memory, the extended drive capability is expected to exhibit better waveform reproduction. TI also recommends this new driver for CCD MOS clock interfacing.

The CCD data rate used in the Frame Rate Buffer unit is the maximum 5 Mbps. This number is derived from a pixel clock rate synchronous with the TV sync generator, part No. MM4320D. With this part, there are 528 pixel times of actual unblanked video of which Motorola uses 512 in each horizontal line. If a phase-locked clock of slightly lower frequency were generated so that 512 pixel samples could be taken from the same unblanked line segment now containing 528 pixels, the CCD data rate could be lowered to 4.88 Mbps. Even though this operation would require more parts for the additional clock and PLL, extra time could be acquired to add a safety margin to the critical timing signals of the CCD devices. This observation is noted primarily as a suggestion for possible system improvement to extend the operating temperature of the unit. This analysis is prefaced by the fact that TI has not guaranteed the full temperature-maximum speed operation of the CCDs that have thus far been delivered to Motorola.

c. Synchronization Delay

The Frame Rate Buffer brassboard unit and the Display Refresh Memory brassboard unit each have an internal oscillator for clock generation and synchronization. The only sync signal common to both units is the Frame Sync pulse generated by the FRB to reset the DRM for the beginning of a new transmitted video frame. This pulse actually resets the TV monitor sync generator device inside the DRM so that output data begins to be displayed at the upper left hand corner of the monitor sweep. The two oscillators are not phase-locked, so they operate at slightly different frequencies. At the 7½ FPS rate, or a frame sync pulse sent every four real time TV frames, the two oscillators do not drift very far apart from each other. At the 1⅞ FPS rate, however, a frame sync is sent only once every 16 real time TV frames. In this instance, the two 20.16 MHZ oscillators do drift slightly apart in frequency. At this reduced frame rate, a slight horizontal line rippling effect can be noticed on the display monitor if, and only if, a stationary picture is viewed under high intensity and contrast level settings. The effect is not noticeable under normal viewing conditions and must be scrutinized under the above settings. The solution to this minor problem is to construct a phase-locked loop around the DRM sync generator device. This, or course, adds complexity to the circuitry, so is not recommended by Motorola since the symptoms are not severe enough to be noticed in actual operation.


SERIAL/PARALLEL HYBRID
DATA REFORMATTER HYBRID
(2 FRAMES) FRAME STORE HYBRID
BIT 5
BIT 1
BIT 0
V_{CC} V_{SS}
OD R/$\overline{W}$ $A_6A_5A_4A_3A_2A_1A_0$
LD REG
SER CK
$\overline{\Phi}_2$ $\overline{\Phi}_1$ $\overline{CE}$ $A_3A_2A_1A_0$
SERIAL DATA INPUT CLOCK
SYNC
BEGIN NEW PIXEL SET
SERIAL CLOCK
LATCH CLOCK
RAM 2
RAM 1
CCD1
CCD2
INPUT BUFFER RAM CONTROL
CCD CONTROL
UNIQUE DRM CONTROL HYBRIDS
SELECT FRAME

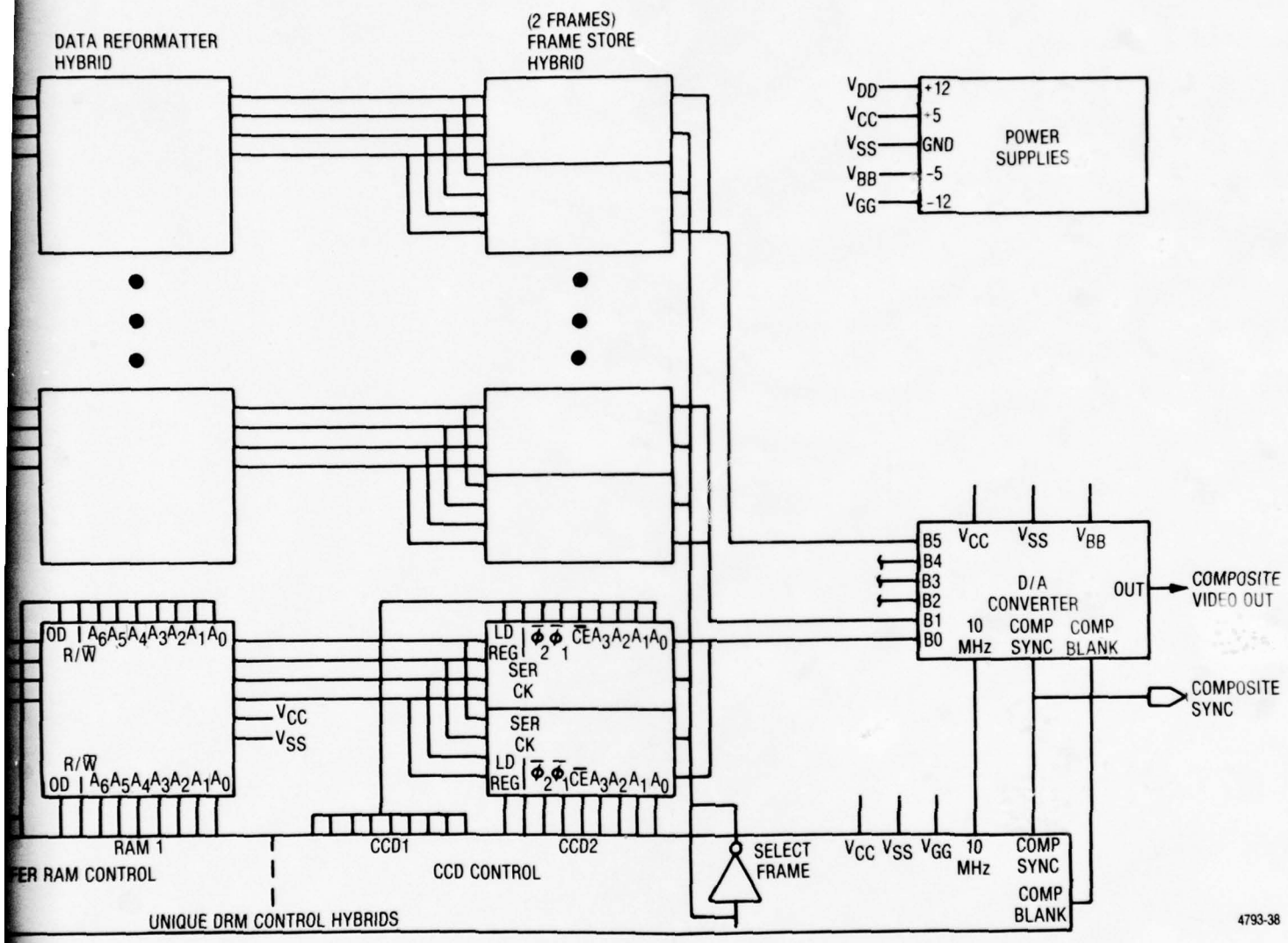


Figure 43. Display Refresh Memory Hybrid Interconnect

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d. Program Follow-on Recommendations

The brassboard frame rate reduction system built for the Air Force under this developmental contract has performed well under all test conditions. Motorola recommends a follow-on program in which the discrete function modules developed in this effort would be hybridized. A miniature frame rate reduction system for RPVs could then be constructed as the basis for an advanced A/J tactical video data link. The Video Memory Modules program has verified that present technology may be utilized to build a low-cost video memory unit for imaging system applications.

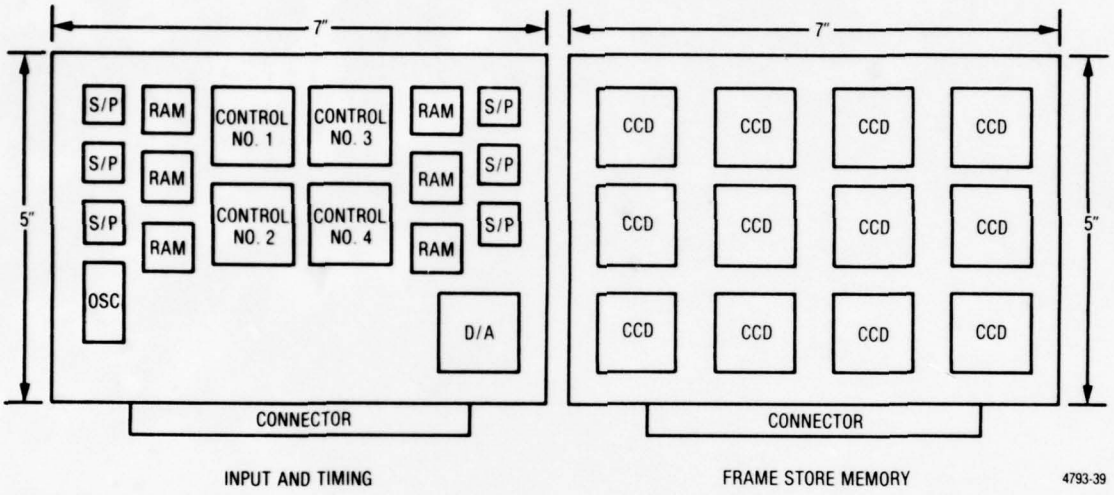

Figure 44. Display Refresh Memory Miniaturized Package Concept

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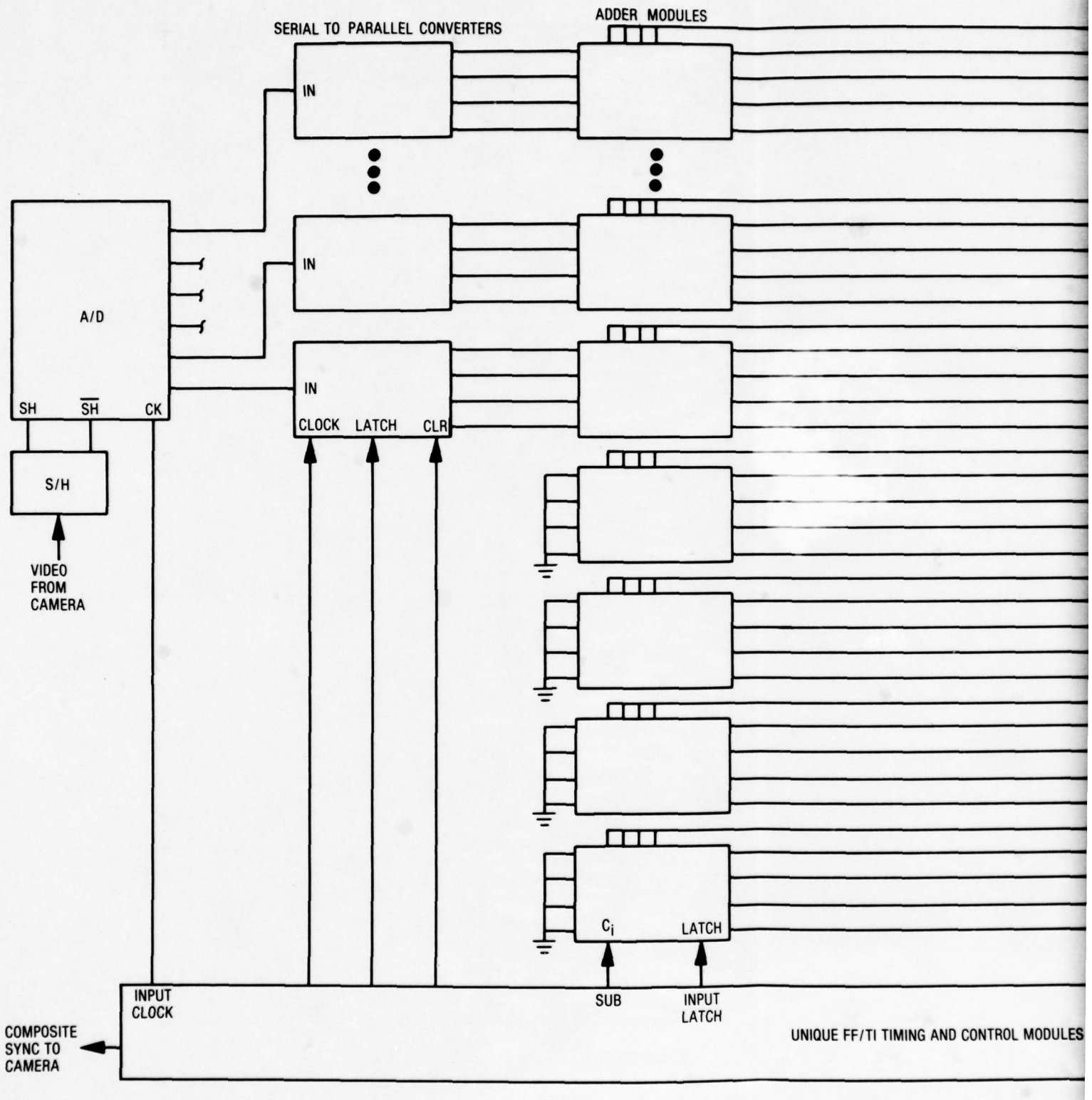
SERIAL TO PARALLEL CONVERTERS
ADDER MODULES
IN
IN
IN
A/D
SH
$\overline{SH}$
CK
CLOCK
LATCH
CLR
S/H
VIDEO FROM CAMERA
C_i
LATCH
SUB
INPUT LATCH
INPUT CLOCK
COMPOSITE SYNC TO CAMERA
UNIQUE FF/TI TIMING AND CONTROL MODULES

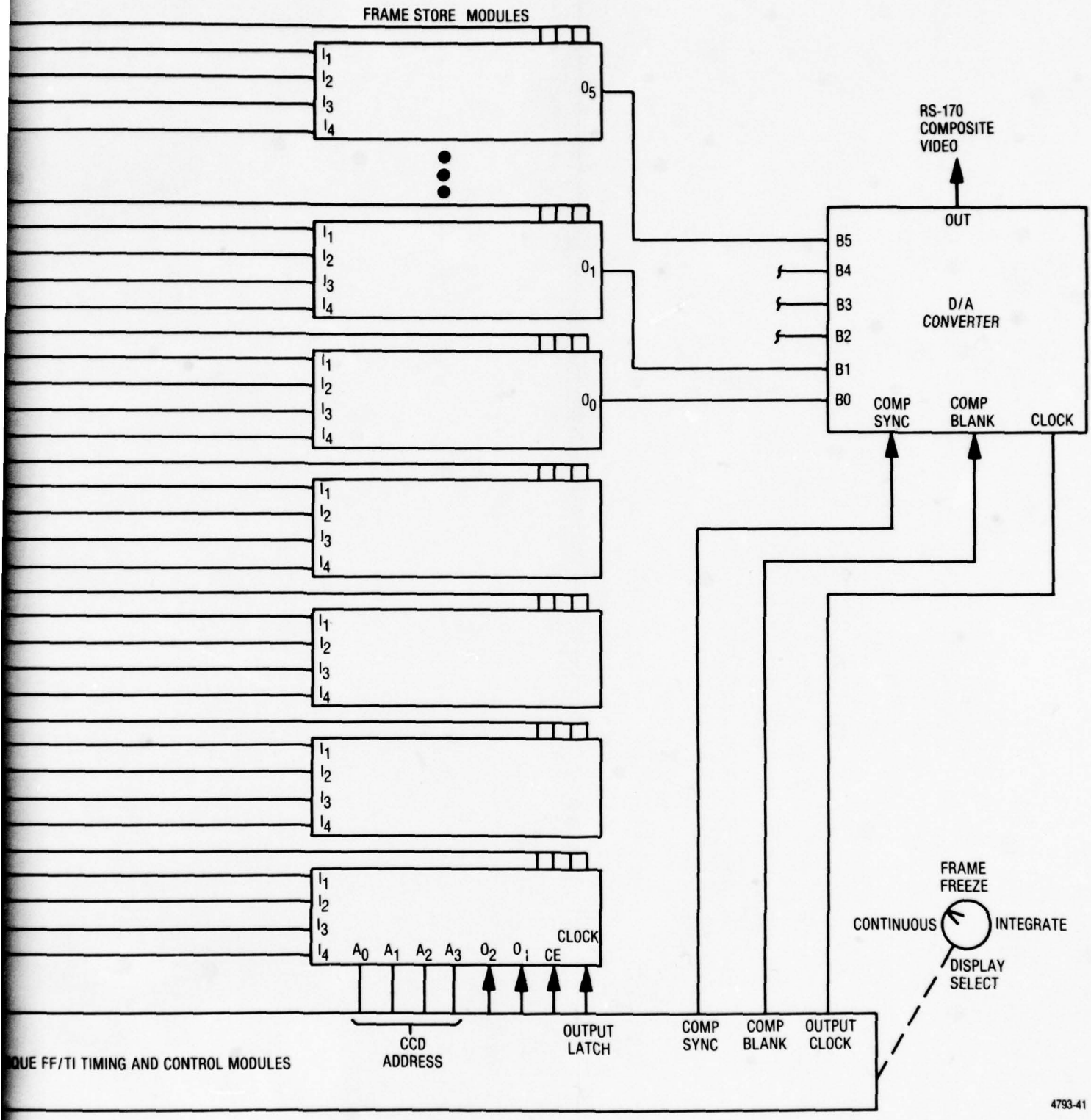

Figure 45. FF/TI Common Module Interconnect

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APPENDIX A

Texas Instruments TMS-3064JL 64K CDD Specification

MOS LSI

TMS 3064 JL
65,536-BIT CCD MEMORY

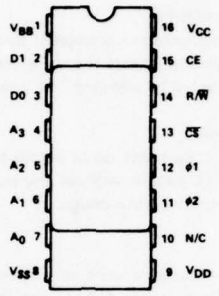
NOVEMBER 1977

- 65,536 x 1 Organization
  (16 Addressable 4096-Bit Loops)
- Performance:

LATENCY TIME AT 5 MHz (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
820 µs	200 ns	300 ns

- Full TTL Compatibility (No Pull-up Resistors Required) on All Inputs Except $\phi 1$, $\phi 2$, and Chip Enable
- Low Power Dissipation:
  280 mW Operating (Typical @ 5 MHz)
  25 mW Recirculating (Typical @ 1 MHz)
  <1 mW Standby (Typical)
- Two-Phase CCD Clocks
- N-Channel Silicon-Gate Technology
- 16-Pin, 300-Mil Dual-in-Line Package

16-PIN CERAMIC DUAL-IN-LINE PACKAGE



description

The TMS 3064 is a high-speed dynamic 65,536-bit CCD (charge-coupled device) block-addressable serial memory. It is organized as 65,536 one-bit words, in sixteen addressable blocks of 4096 bits each. N-channel silicon-gate technology with two levels of polysilicon is employed to optimize the speed/power/density trade-off. The TMS 3064 can operate at any frequency from 1 MHz to 5 MHz. This frequency range allows the system designer to match the memory speed to that of the rest of the system.

All inputs except the two clocks and chip enable are fully TTL-compatible and require no pull-up resistors. The low input capacitance of all the TTL inputs eliminates the need for specialized drivers on these inputs. When driven by Series 74 devices, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible output buffer is guaranteed to drive at least two Series 74 TTL gates. The TMS 3064 uses only two CCD clocks to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of the TMS 3064 is 280 mW active at the maximum frequency and <1 mW standby. To retain data only 25 mW (typical) is required, which includes the power consumed to refresh the content of the memory.

The TMS 3064 is offered in a 16-pin ceramic (JL suffix) dual-in-line package. The TMS 3064 is guaranteed for operation from 0°C to 70°C still-air ambient.

operation

Chip Select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the input and output circuits. The data input and data output terminals are enabled when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip-select input must be held high when chip enable goes high. A latch for the chip-select input has been provided on the chip to reduce overhead and simplify system design.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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operation (continued)

Chip Enable (CE)
An MOS level (12 V swing) input is required. All read, write, and read-modify-write operations take place when the chip-enable input is high. When the chip enable is low, the memory is in a low-power recirculate/standby mode and no read/write operations can take place.

Read/Write Select (R/$\overline{W}$)
The read or write operation is selected through the read/write (R/$\overline{W}$) input. A logic high on R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. The R/$\overline{W}$ terminal can be driven by standard TTL circuits without a pull-up resistor.

***Address* (A0 – A3)**
All addresses must be stable on or before the rising edge of the chip-enable pulse. All the address inputs can be driven from standard TTL circuits without any pull-up resistor. Address latches are provided on the chip in order to reduce overhead and simplify system design.

Data In (DI)
Data is written in during a write or read-modify-write cycle while the chip enable input is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. An on-chip latch is provided at the data-in terminal.

Data Out (DO)
The three-state output buffer provides direct TTL compatibility with a fan-out of at least two Series 74 TTL gates plus 100 pF stray capacitance. The TMS 3064 utilizes a latched data output to provide adequate time for data output to be valid, even at the minimum cycle time of 200 ns. If the chip is not selected, then the output will go into a high-impedance state with the rising edge of $\phi 2$ or chip enable, whichever occurs first. During a valid data cycle, chip enable first causes the output to go to a high impedance and then, a data delay time later, the output goes to a low impedance (logic one or zero). The data then remains latched until the next cycle.

Phase One ($\phi 1$) Clock, Phase Two ($\phi 2$) Clock
$\phi 1$ and $\phi 2$ are two-phase, non-overlapping clocks for driving the CCD SPS registers. The other five clocks required for operating these registers are generated on the chip to simplify system design. With each $\phi 1/\phi 2$ clock cycle, data are shifted forward by one bit position in each of the 16 registers, and one bit in each register is refreshed by a regenerator. $\phi 1$ and $\phi 2$ are high-level (12 V) clocks. NOTE: $\phi 1$ AND $\phi 2$ MUST NOT BE HIGH SIMULTANEOUSLY.

Minimum Clock Frequency (Refresh)
The CCD is a dynamic storage device and thus the stored data must be refreshed periodically to remain valid. In the TMS 3064, the maximum period for this refresh cycle is approximately four milliseconds. This corresponds to a minimum continuous clock frequency of 1 MHz.

Pause Time
Pause time is the maximum time that $\phi 1$ and $\phi 2$ clocks may be held low without loss of data. In the simplest case, pause time may be as long as 0.5 ms when preceded and followed by a minimum of 4096 clock cycles at a 5 MHz clock rate. If clocks are held low for a period longer than 0.5 ms, a flush operation must be performed before writing data into the memory.

Flush Operation
A flush operation consists of clocking $\phi 1$ and $\phi 2$ for a minimum of ten refresh cycles of 4096 clock cycles each. A flush operation is required when the memory is first powered up, and after each period of clock inactivity exceeding 0.5 ms.

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functional block diagram

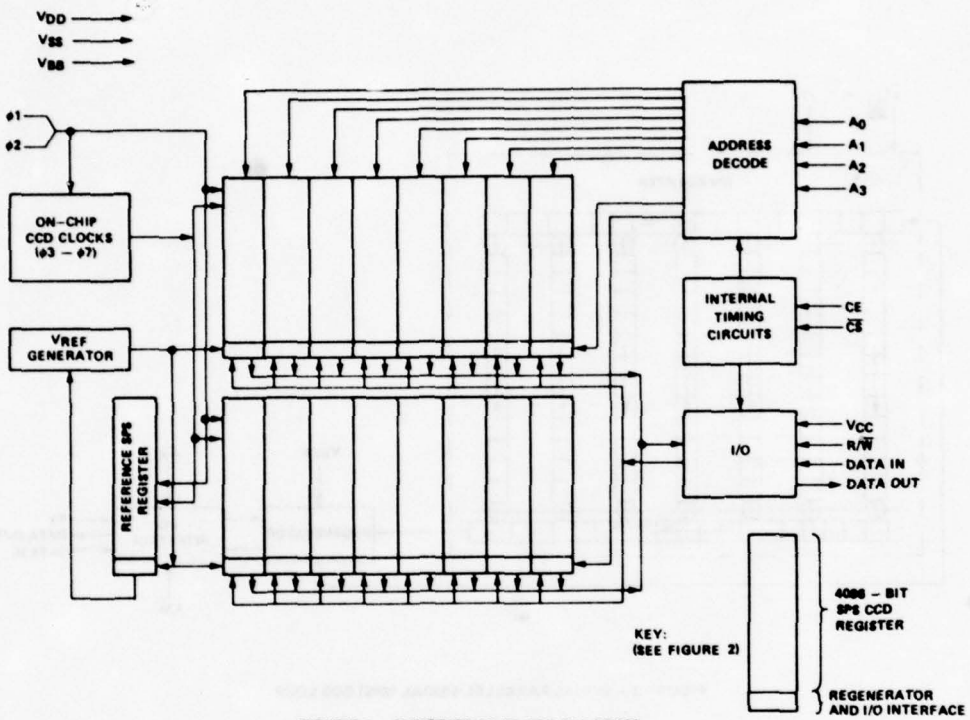

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

The TMS 3064 is internally organized as 16 addressable 4 Kb loops. Each loop consists of a 4096-bit serial-parallel-serial (SPS) CCD shift register for data storage, a regenerator for refreshing the data, and an I/O interface circuit for data transfer to and from the loop (see Figure 2). A 17th SPS register (non-addressable) is used in conjunction with a reference voltage generator circuit to generate a reference voltage compensated for leakage current that is used by the regenerators at each loop.

Although a total of seven different clocks are required to operate the SPS registers, only two simple, non-overlapping clocks must be supplied by the user; the other five are generated on the chip. These clocks recirculate and refresh the data storage in the loops. Within each loop, data is accessed serially by pulsing the CCD clocks, $\phi 1$ and $\phi 2$, until the desired bit is shifted to the output of the selected SPS register. At the register output, the data is refreshed by a regenerator and, in a read cycle or a recirculate cycle, is returned to the input of the register again. Data at the output of any regenerator is read by setting the appropriate address, setting $\overline{CS}$ low and R/$\overline{W}$ high, then pulsing CE high. Data output will be valid one data delay time following the rise of CE. For writing data into a particular loop, the address and data inputs are set, $\overline{CS}$ and R/$\overline{W}$ are set low, then CE is pulsed high. A given bit may be read and then modified in the same clock cycle by performing a read-modify-write (RMW) operation. This consists of first performing a read operation as described above, then while CE is still high, setting data input and pulsing R/$\overline{W}$ low. The RMW cycle may be used to interchange the contents of two TMS 3064's by connecting the data output of one to the data input of the other, and vice-versa.

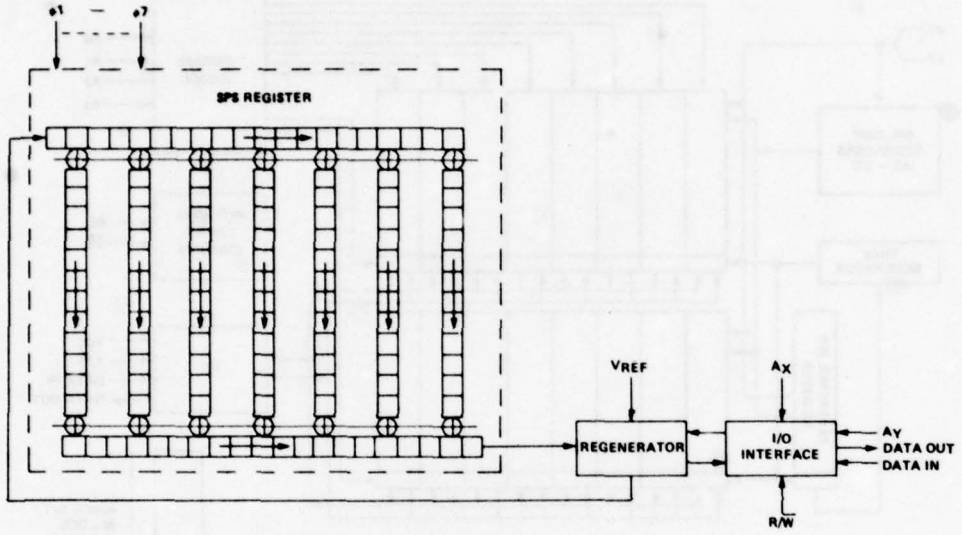

FIGURE 2 – SERIAL-PARALLEL-SERIAL (SPS) CCD LOOP

serial-parallel-serial (SPS) CCD loop

Each addressable block in the TMS 3064 contains 4096 bits of storage, organized as a serial-parallel-serial (SPS) shift register. Data is shifted into the SPS register along a 32-bit input serial register, is demultiplexed into 32 parallel 127-bit shift registers, and finally multiplexed into a 32-bit output serial register which shifts the data to a regenerator. The regenerator detects the small charge quantities being transferred and converts these charge levels to voltage levels which are compared with a reference voltage (V_{REF}). The output of the regenerator is a 0 V to 12 V digital signal which, during a read or recirculate cycle, drives the input gate of the CCD to refresh the stored data. Data transfer to and from the loop is controlled by an I/O interface circuit.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Output voltage (operating with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{DD}		11.4	12	12.6	V
Supply voltage, V_{SS}			0		V
Supply voltage, V_{BB}		−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable and clocks)		2.2		5.5	V
High-level chip enable input voltage, $V_{IH(CE)}$		V_{DD} −1.2		V_{DD} +1.2	V
High-level clock input voltage, $V_{IH(\phi1,\phi2)}$		V_{DD} −1		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable and clocks)		−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$		−0.6		0.6	V
Low-level clock input voltage, $V_{IL(\phi1,\phi2)}$ (see Note 2)		−0.6		0.6	V
Variable clock frequency, f_ϕ (see Note 3)	T_A = 0°C to 55°C	1		5	MHz
Fixed clock frequency, f_ϕ (see Note 3)	T_A = 0°C to 70°C	1		5	MHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 2. Interclock feedthrough transients outside this range are permitted at the $\phi1$, $\phi2$ inputs, provided the limits specified in Figure 9 are not exceeded.

3. Fixed clock limits apply when clock frequency is never changed otherwise variable frequency applies.

CCD

electrical characteristics over full range of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA	2.7		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA	V_{SS}		0.4	V
I_{OZ}	High-impedance state (off-state) output current	V_O = 0 to 5.5 V			1	μA
I_I	Input current (all inputs except chip enable and clocks)	V_I = 0 to 5.5 V			1	μA
$I_{I(CE)}$	Chip-enable input current	V_I = 0 to 13.2 V			1	μA
$I_{I(\phi1)}$	Clock one input current	V_I = 0 to 13.2 V, $V_{I(\phi2)}$ = 0V			1	μA
$I_{I(\phi2)}$	Clock two input current	V_I = 0 to 13.2 V, $V_{I(\phi1)}$ = 0V			1	μA
I_{CC}	Supply current from V_{CC}	I_O = 0, f MAX = 5 MHz			1	mA
I_{DD}	Peak transient supply current from V_{DD}			100	160	mA
I_{DD}	Supply current from V_{DD} with CE high	$V_{IH(CE)}$ = 13.2 V		7	10	mA
I_{DD}	Supply current from V_{DD} with CE low (standby)	$V_{IL(CE)}$ = 0.6 V			1	mA
$I_{DD(av)}$	Average supply current from V_{DD} during recirculate cycle	f MIN = 1 MHz		1.5	4	mA
		f MAX = 5 MHz		7	10	
$I_{DD(av)}$	Average supply current from V_{DD} during read cycle	f MIN = 1 MHz		4	6	mA
		f MAX = 5 MHz		18	23	
$I_{DD(av)}$	Average supply current from V_{DD} during write cycle	f MIN = 1 MHz		4	6	mA
		f MAX = 5 MHz		20	25	
$I_{DD(av)}$	Average supply current from V_{DD} during read-modify-write cycle	f MIN = 1 MHz		4	6	mA
		f MAX = 3.3 MHz		15	20	
$I_{BB(av)}$	Average supply current from V_{BB}	Recirculate: f MAX = 5 MHz		10	20	μA
		Read or write: f MAX = 5 MHz		12	30	
I_{BB}	Peak transient supply current from V_{BB}			40	60	mA

†All typical values are at T_A = 25°C.

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capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, T_A = 0°C to 70°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			10	pF
$C_{i(CE)}$	Input capacitance chip-enable input	$V_{I(CE)}$ = 0 to 13.2 V↑		15	pF
		$V_{I(CE)}$ = 13.2 to 0V↓		10	
$C_{i(\phi1)}$	Input capacitance phase-one clock input including interclock capacitance			160	pF
$C_{i(\phi2)}$	Input capacitance phase-two clock input including interclock capacitance			160	pF
$C_{i(\phi1,\phi2)}$	Interclock capacitance			60	pF
$C_{i(\overline{CS})}$	Input capacitance chip-select input			10	pF
$C_{i(DI)}$	Input capacitance data input			10	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			10	pF
C_o	Output capacitance			12	pF

$\phi1$, $\phi2$, and chip-enable timing requirements (see figure 3.)

	PARAMETER	MIN	MAX	UNIT
$t_{w(\phi1H)}$	Pulse width, $\phi1$ high	30		ns
$t_{w(\phi2H)}$	Pulse width, $\phi2$ high	40		ns
$t_{w(CEH)}$	Pulse width, CE high	80		ns
$t_{w(CEL)}$	Pulse width, CE low	50		ns
$t_{CEH,\phi2L}$	CE high to $\phi2$ low edge separation	90		ns
$t_{CEL,\phi1H}$	CE low to $\phi1$ high edge separation	30		ns
$t_{su(\phi1)}$	$\phi1$ setup time	−30		ns
$t_{\phi1L,\phi2H}$	$\phi1$-$\phi2$ pulse separation	25		ns
$t_{\phi2L,\phi1H}$	$\phi2$-$\phi1$ pulse separation	15		ns

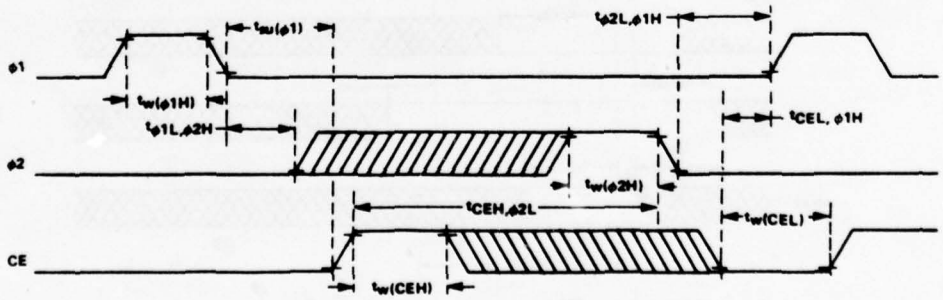

FIGURE 3 – $\phi1$, $\phi2$, AND CE TIMING

CCD

read cycle timing requirements (see figure 4)

	PARAMETER	MIN	MAX	UNIT
$t_{c(rd)}$	Read data cycle time	200	1000	ns
$t_{su(ad)}$	Address setup time	0		ns
$t_{su(CS)}$	Chip-select setup time	0		ns
$t_{su(rd)}$	Read setup time	0		ns
$t_{h(ad)}$	Address hold time	50		ns
$t_{h(CS)}$	Chip-select hold time	70		ns
$t_{h(rd)}$	Read hold time for read cycle	0		ns

data output switching characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PZX}	Delay time to data valid	See Figure 10		75	150	ns
*t_{PXZ}	Output disable time to end of data valid		0	2		ns

*t_{PXZ} commences with the rise of $\phi 2$ or $\overline{CE}$, whichever occurs first. If the rise of $\phi 2$ precedes the rise of $\overline{CE}$, then the limits of Figure 8 apply.

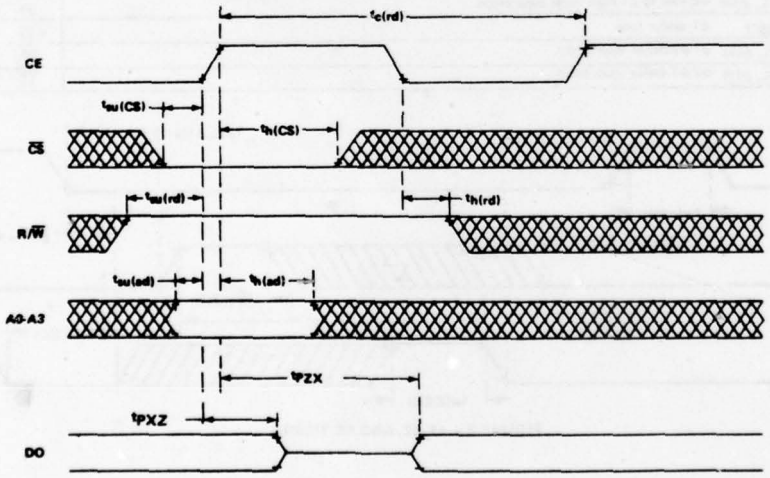

FIGURE 4 – READ CYCLE TIMING

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write cycle timing requirements (see figure 5)

	PARAMETER	MIN	MAX	UNIT
$t_{c(wr)}$	Write data cycle time	200	1000	ns
$t_{w(wr)}$	Write pulse width	50		ns
†$t_{su(da\text{-}wr)}$	Data setup time before fall of R/W	0		ns
$t_{su(wr)}$	Write setup time before fall of CE	80		ns
$t_{su(wr\text{-}\phi2)}$	Write setup time before fall of $\phi2$	55		ns
*$t_{h(da)}$	Data hold time after rise of CE	105		ns
$t_{h(wr)}$	Write hold time	70		ns
*$t_{h(da\text{-}wr)}$	Data hold time after fall of R/W	85		ns

†If R/W is low before CE goes high, then DI must be valid when CE goes high.
*$t_{h(da\text{-}wr)}$ applies if R/W goes low after CE is high; $t_{h(da)}$ applies otherwise.

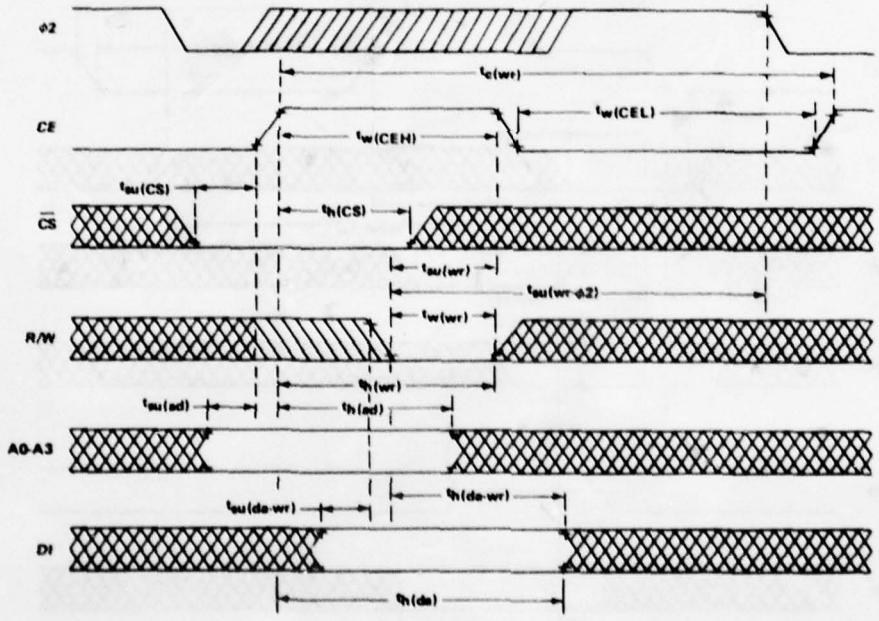

FIGURE 5 – WRITE CYCLE TIMING

CCD

read-modify-write cycle timing requirements (see figure 6)

	PARAMETER	MIN	MAX	UNIT
$t_{c(rmw)}$	Read-modify-write data cycle time	300	1000	ns
$t_{h(rmw)}$	Read hold time for RMW cycle	100		ns

(Other parameter values – same as listed for read and write cycles.)

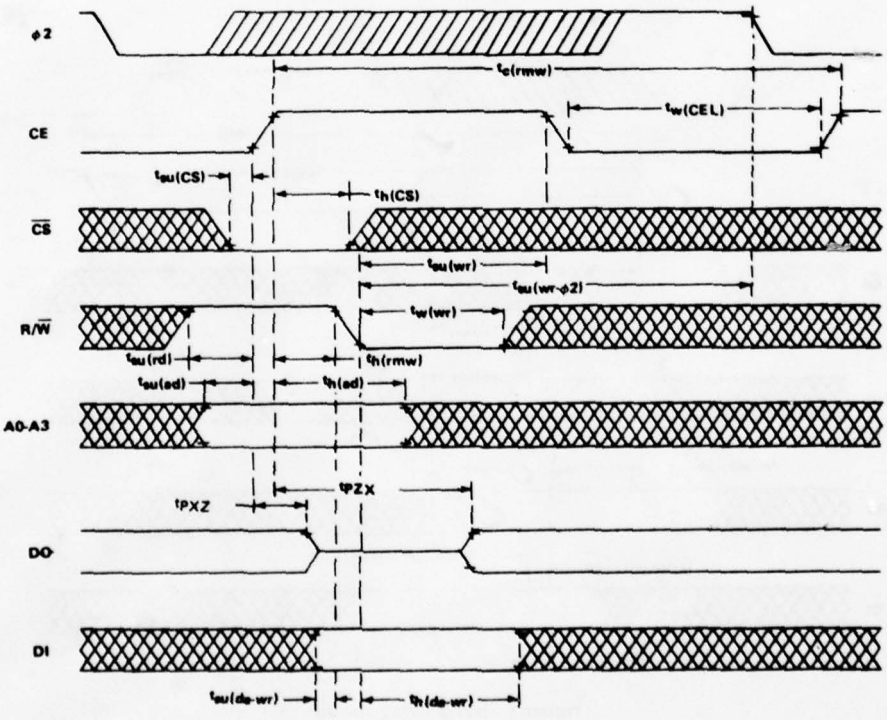

FIGURE 6 – READ-MODIFY-WRITE CYCLE TIMING

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chip-enable disabling output requirements when chip is not selected (see figure 7)

	PARAMETER	MIN	MAX	UNIT
$t_{su(CSH)}$	Chip disable setup time	0		ns
$t_{h(CSH)}$	Chip disable hold time	15		ns

(Other parameter values – same as read cycle timing.)

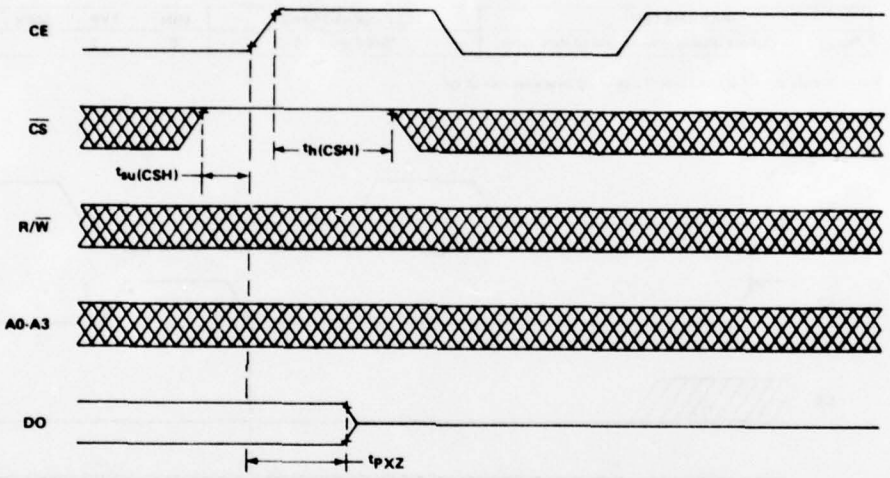

FIGURE 7 – CE DISABLING OUTPUT WHEN CHIP IS NOT SELECTED

recirculate cycle timing requirements (see figure 8)

	PARAMETER	MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time, recirculate	200	1000	ns

switching characteristics for $\phi 2$ disabling output (see figure 8)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
*t_{PXZ}	Output disable time to end of data valid	*See Figure 10	0	2		ns

*t_{PXZ} also applies during active cycle if rise of $\phi 2$ precedes rise of $\overline{CE}$.

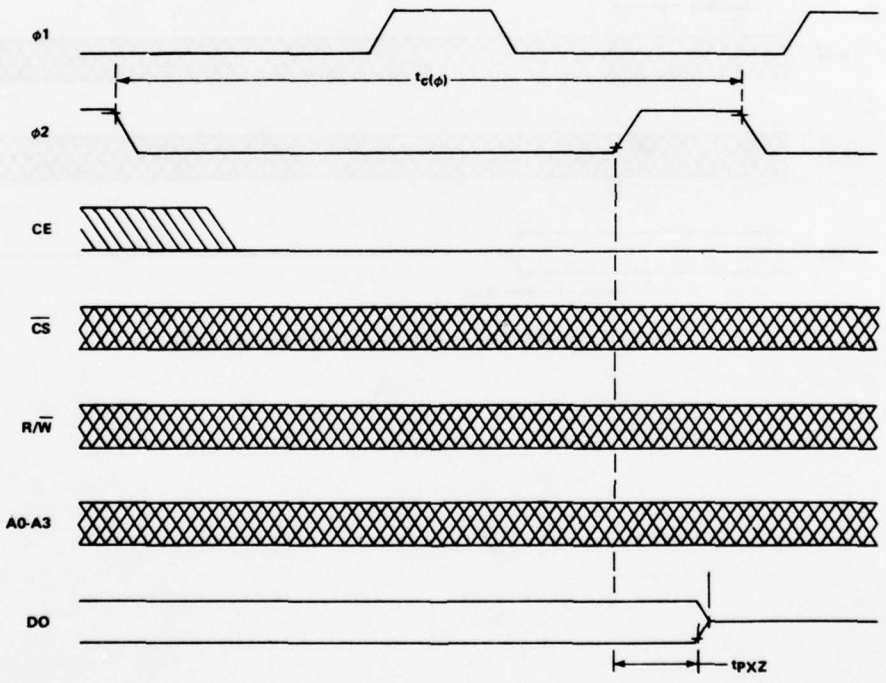

FIGURE 8 – $\phi 2$ DISABLING OUTPUT DURING RECIRCULATE CYCLE

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clock-to-clock transient feed-thru requirements

	PARAMETER		MIN	MAX	UNIT
$t_{FT(R)}$	Rising-clock transient feed-thru time			$\pm 0.5t_{r\phi}$	ns
$t_{FT(F)}$	Falling-clock transient feed-thru time			$\pm 0.5t_{f\phi}$	ns
$t_{wFT(R)}$	Rising-clock transient feed-thru pulse width			$1.5t_{r\phi}$	ns
$t_{wFT(F)}$	Falling-clock transient feed-thru pulse width			$1.5t_{f\phi}$	ns
$V_{FT(R)}$	Instantaneous transient feed-thru voltage resulting from rising clock	$V_{FT(R)+}$		2	V
		$V_{FT(R)-}$		−0.6	
$V_{FT(F)}$	Instantaneous transient feed-thru voltage resulting from falling clock	$V_{FT(F)+}$		0.6	V
		$V_{FT(F)-}$		−1.5	

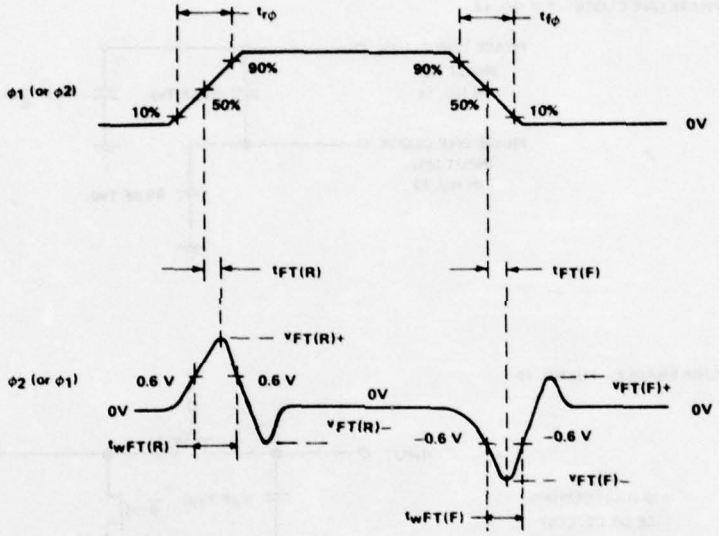
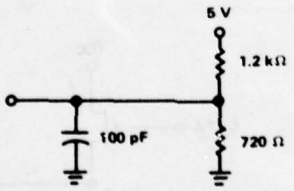


FIGURE 9 – CLOCK-TO-CLOCK TRANSIENT FEED-THRU REQUIREMENTS



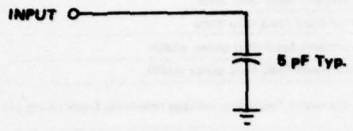
NOTE: RESISTOR VALUES ARE EQUIVALENT TO TWO SERIES 74 TTL LOADS.

FIGURE 10 – OUTPUT LOAD CIRCUIT

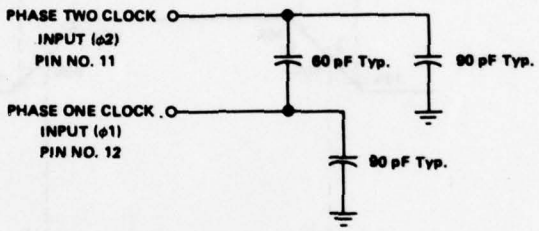
equivalent input/output circuits

(A) ALL TTL LEVEL INPUTS

INPUT	PIN NO.
DATA IN	2
A0 - A3	4-7
$\overline{CS}$	13
R/$\overline{W}$	14

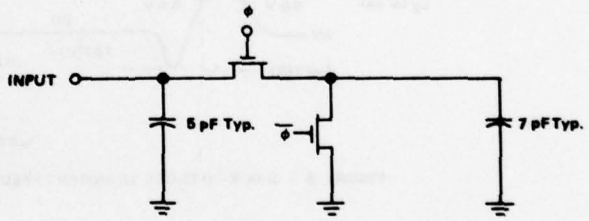


(B) PHASE TWO CLOCK -- PIN NO. 11
PHASE ONE CLOCK -- PIN NO. 12

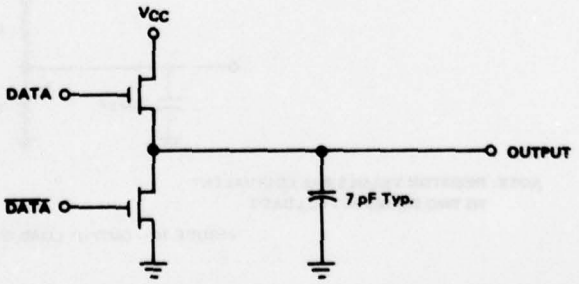


(C) CHIP ENABLE -- PIN NO. 15

ϕ IS HIGH DURING RISE OF CE. LOW DURING FALL OF CE



(D) DATA OUT -- PIN NO. 3



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APPENDIX B

FF/TI Algorithm Program

```
1.      C
2.      C       FFTI TEST PROGRAM
3.      C
4.
5.
6.
7.
8.
9.
10.
11.
12.
13.
14.          20
15.
16.
17.
18.          10
ABSOFT: END STATEMENT ENCOUNTERED BY COMPILER.
```

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NAME	TYPE	CLASS	HEX LOC	DEC WORDS
A	I	ARRAY	00000 V	128
N	I	SCALR	00083 V	1

NAME	TYPE	CLASS	HEX LOC	DEC WORDS
F	I	SCALR	00080 V	1
S	I	SCALR	00081 V	1

NAME	TYPE	CLASS	HEX LOC	DEC WORDS
J	I	SCALR	00082 V	1

LABEL	HEX LOC	LABEL	HEX LOC	LABEL	HEX LOC	LABEL	HEX LOC	LABEL	HEX LOC	LABEL	HEX LOC
10	00041	20	00024								

LOCAL VARIABLES (132 WORDS):

00000 A 00080 F 00081 S 00082 J 00083 N

BLANK COMMON (0 WORDS)

EXTERNAL SUBPROGRAMS REQUIRED:

F:IOR F:DC F:CC GRADTCL GINITIAL GIODATA GPRINT GSTOP

NUMBER OF ERROR MESSAGES: 1

NUMBER OF STATEMENTS DELETED: 0

HIGHEST ERROR SEVERITY: 0 (NO MAJOR ERRORS)

	DEC WORDS	HEX WORDS
GENERATED CODE:	71	00047
CONSTANTS:	0	00000
LOCAL VARIABLES:	132	00084
TEMPS:	0	00000
TOTAL PROGRAM:	203	000CB

```
LOAD (GO),(LMN,TERM)
IP1 ASSOCIATED.


  * * ALLOCATION SUMMARY * *

PROTECTION        LOCATION   PAGES

DATA (00)         A000       2
PROCEDURE (01)    A400       1
DCB (10)          A800       1
  SEV.=LEV.=

**********************************  SOC= 1480

  ********** PROTECTION TYPES **********
     00 DATA   01 PROCEDURE   10 STATIC
     --------  ------------   ---------
HIGH: A5F3        A655         A5FF
LOW : A000        A400         A800
SIZE:  5F4         256          800
```


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```
RUN (LMN,TEMP)
 STEP FULL SCALE
 A(0) = 0
 A(N) = 63
 A(N) = 122
 A(N) = 177
 A(N) = 228
 A(N) = 276
 A(N) = 321
 A(N) = 363
 A(N) = 403
 A(N) = 440
 A(N) = 475
 A(N) = 508
 A(N) = 539
 A(N) = 568
 A(N) = 595
 A(N) = 620
 A(N) = 644
 A(N) = 666
 A(N) = 687
 A(N) = 707
 A(N) = 725
 A(N) = 742
 A(N) = 758
 A(N) = 773
 A(N) = 787
 A(N) = 800
 A(N) = 813
 A(N) = 825
 A(N) = 836
 A(N) = 846
 A(N) = 856
 A(N) = 865
 A(N) = 873
 A(N) = 881
 A(N) = 888
 A(N) = 895
 A(N) = 902
 A(N) = 908
 A(N) = 914
 A(N) = 919
 A(N) = 924

 A(N) = 929    A(N) = 993    A(N) = 993    A(N) = 74     A(N) = 15     A(N) = 15
 A(N) = 933    A(N) = 993    A(N) = 993    A(N) = 74     A(N) = 15     A(N) = 15
 A(N) = 937    A(N) = 993    STEP TO ZERO  A(N) = 74     A(N) = 15     STEP TO ZERO
 A(N) = 941    A(N) = 993    A(N) = 931    A(N) = 66     A(N) = 15     *STOP* 0
 A(N) = 945    A(N) = 993    A(N) = 873    A(N) = 62     A(N) = 15
 A(N) = 948    A(N) = 993    A(N) = 819    A(N) = 59     A(N) = 15
 A(N) = 951    A(N) = 993    A(N) = 768    A(N) = 56     A(N) = 15
 A(N) = 954    A(N) = 993    A(N) = 720    A(N) = 53     A(N) = 15
 A(N) = 957    A(N) = 993    A(N) = 675    A(N) = 50     A(N) = 15
 A(N) = 960    A(N) = 993    A(N) = 633    A(N) = 47     A(N) = 15
 A(N) = 963    A(N) = 993    A(N) = 594    A(N) = 45     A(N) = 15
 A(N) = 965    A(N) = 993    A(N) = 557    A(N) = 43     A(N) = 15
 A(N) = 967    A(N) = 993    A(N) = 523    A(N) = 41     A(N) = 15
 A(N) = 969    A(N) = 993    A(N) = 491    A(N) = 39     A(N) = 15
 A(N) = 971    A(N) = 993    A(N) = 461    A(N) = 37     A(N) = 15
 A(N) = 973    A(N) = 993    A(N) = 433    A(N) = 35     A(N) = 15
 A(N) = 975    A(N) = 993    A(N) = 407    A(N) = 33     A(N) = 15
 A(N) = 977    A(N) = 993    A(N) = 381    A(N) = 31     A(N) = 15
 A(N) = 978    A(N) = 993    A(N) = 358    A(N) = 30     A(N) = 15
 A(N) = 979    A(N) = 993    A(N) = 336    A(N) = 29     A(N) = 15
 A(N) = 980    A(N) = 993    A(N) = 315    A(N) = 28     A(N) = 15
 A(N) = 981    A(N) = 993    A(N) = 296    A(N) = 27     A(N) = 15
 A(N) = 982    A(N) = 993    A(N) = 278    A(N) = 26     A(N) = 15
 A(N) = 983    A(N) = 993    A(N) = 261    A(N) = 25     A(N) = 15
 A(N) = 984    A(N) = 993    A(N) = 245    A(N) = 24     A(N) = 15
 A(N) = 985    A(N) = 993    A(N) = 230    A(N) = 23     A(N) = 15
 A(N) = 986    A(N) = 993    A(N) = 216    A(N) = 22     A(N) = 15
 A(N) = 987    A(N) = 993    A(N) = 203    A(N) = 21     A(N) = 15
 A(N) = 988    A(N) = 993    A(N) = 191    A(N) = 20     A(N) = 15
 A(N) = 989    A(N) = 993    A(N) = 180    A(N) = 19     A(N) = 15
 A(N) = 990    A(N) = 993    A(N) = 169    A(N) = 18     A(N) = 15
 A(N) = 991    A(N) = 994    A(N) = 159    A(N) = 17     A(N) = 15
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 A(N) = 993    A(N) = 993    A(N) = 88     A(N) = 15     A(N) = 15
 A(N) = 993    A(N) = 993    A(N) = 83     A(N) = 15     A(N) = 15
```

APPENDIX C

FRB Versus Temperature Test Results

TEMPERATURE CYCLE

MOTOROLA INC.
Government Electronics Division
SCOTTSDALE, ARIZONA

SHEET 1 OF WO 4645 DATE 7-13-78

PROJECT 2513-000 UNIT F.R. BUFFER MODEL N/A SERIAL E/M

OPERATOR ART HAWKINS OBSERVER LARRY HOPPER

SPECIFICATION VERBAL NO. OF CYCLES N/A

CYCLE RANGE _____ TO _____

RATE OF CHANGE MAX _____ ° _____ PER _____

MIN _____ ° _____ PER _____

REASON FOR TEST _____

REMARKS _____

°C

TIME	AMB 1	BUFFER 2	C.C.D. 3	BLUE BOARD 4	5	6	7	8	9	10	REMARKS
0900	24	46	30	25.5							Go to 31°C
0925	31	38	32	31							
0940	32	39	33	32							Increase gradually to 50°C
0945	35	41	36	35							
0950	36	43	37	36							
0955	39	46	39	39							
1000	40	47	40	40							
1005	43	50	44	43							
1010	47	53	47	46							
1013	50	56	50	50							Video O.K. at 49°C, broke up at 50°C amb.
1020	47	55	48	47							Normal video resumed
1025	49	56	50	49							Video broken up.
1035	49	56	50	49							" " "
1045	49	56	50	49							" " "
1055	49	56	50	49							" " "

MOTOROLA/GED E3081-01 3/71 CTL 734

MOTOROLA INC.
Government Electronics Division

TEMPERATURE CYCLE

SHEET 2 OF ___ CONTROL NO. 20 W.O. 4645 DATE 7-13-78

PROJECT 2513-000 UNIT F.R. Buffer MODEL N/A SERIAL N/A

All temps in °C

TIME	1 AIR	2 BUFFER	3 C.C.D.	BLUE 4 BOARD	5	6	7	8	9	10	REMARKS
1105	49	57	50	50							Video brcken up.
1117	49	57	50	50							Open Removed board
1320	29	36	33	32							Restart. Increase tc 50°C
1325	39	41	39	39							
1330	43	46	44	44							
1335	46	49	47	46							
1340	48	52	49	49							
1341	49	53	49	49							Video brcken up.
1345	51	54	51	51							Gc to 55°C
1350	56	60	57	57							Gc to 47°C
1355	47	52	49	48							
1356	47	51	48	47							Normal videc resumed
1400	47	50	48	47							Increase temp. gradually
1405	48	51	48	48							
1409	48	51	49	48							
1411	48.5	52	49	48.5							Video broken up.
1427	49	52	50	49							
1450	49	52	50	49							Open.
1600	29	34	31	29							Restart. Increase to 50°C
1605	40	41	40	39							
1610	48	50	48	48							
1612	49	52	50	49							Video broken up. Open.

MOTOROLA INC.
Government Electronics Division

TEMPERATURE CYCLE

SHEET 3 OF ___ CONTROL NO. 20 W.O. 4645 DATE 7-13-78

PROJECT 2513-000 UNIT F.R. Buffer MODEL N/A SERIAL N/A

All temps. in °C

	TIME	1 AIR	2 BUFFER	3 C.C.D.	4 BLUE BOARD	5	6	7	8	9	10	REMARKS
7/14	1040	26	39	33	29							Increase toward 50°C
	1045	36	37	36	35							
	1050	44	45	44	43							
	1053	48	51	44	47							
	1055	49	52	50	49							Video broken up.
	1100	50	53	51	51							" " "
	1105	51	54	52	51							" " "
	1110	46	51	48	47							" " "
	1111	46	50	47	47							Normal video resumed
	1125	47	49	47	47							
	1137	48	51	48	47							Open.
	1205	37	41	39	37							Increase toward 50°C
	1210	47	49	47	47							
	1214	49	51	50	49							Video broken up.
	1219	49	52	50	49							Open
	1220	34	48	45	44							Normal video resumed.
	1249	34	39	36	34							Increase toward 50°C
	1255	47	50	48	47							
	1259	49	52	50	49							Video broken up.
	1310	49	52	50	50							" " "
	1326	49	52	50	50							Open.
	1355	35	39	36	35							Increase toward 50°C

MOTOROLA INC.
Government Electronics Division

TEMPERATURE CYCLE

SHEET 4 OF ___ CONTROL NO. 20 W.O. 4645 DATE 7-14-78

PROJECT 2513-000 UNIT F.R. Buffer MODEL N/A SERIAL N/A

All temps. in °C

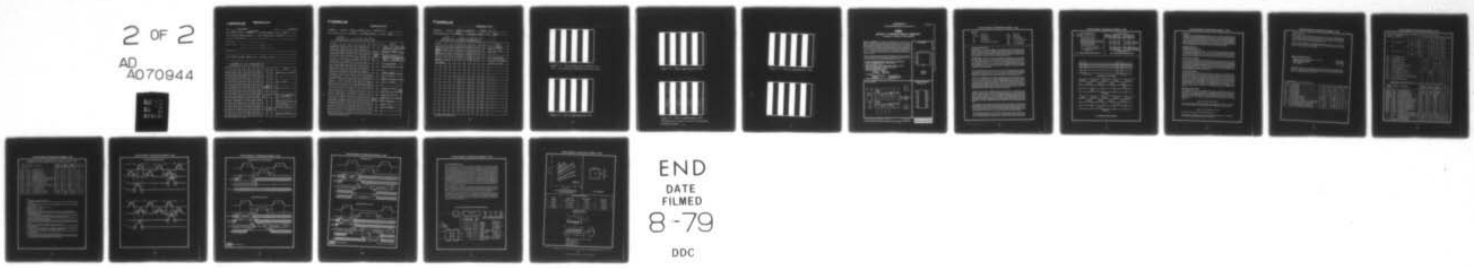
TIME	1 AIR	2 BUFFER	3 C.C.D.	4 BLUE BOARD	5	6	7	8	9	10	REMARKS
1400	40	41	40	40							
1405	46	47	46	46							
1410	48	49	48	48							
1414	50	51	50	50							Video broken up.
1418	50	52	51	50							End test.

MOTOROLA/GED K0154-02 7/78 CTL 734

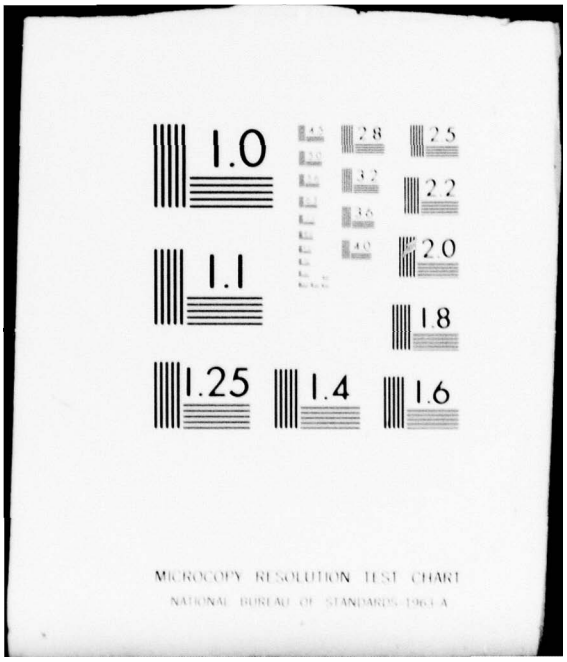
AD-A070 944 MOTOROLA INC SCOTTSDALE ARIZ GOVERNMENT ELECTRONICS DIV F/G 9/2
VIDEO MEMORY MODULES.(U)
FEB 79 L A HOPPER

UNCLASSIFIED F33615-77-C-1142
AFAL-TR-79-1003 NL

2 OF 2
AD A070944



END
DATE FILMED
8-79
DDC


1.0
1.1
1.25
1.4
1.6
2.8
2.5
3.2
2.2
3.6
2.0
4.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

MOTOROLA INC.
Government Electronics Division

TEMPERATURE CYCLE

SHEET 1 OF W.O. 4645 DATE 7-24-78

PROJECT 2513-000 UNIT ~~FRM~~ FRB MODEL Eng. model SERIAL n/a

OPERATOR Jim Thompson OBSERVER Forrest Seitz

SPECIFICATION Verbal NO. OF CYCLES

CYCLE RANGE TO

RATE OF CHANGE MAX 0 PER

MIN 0 PER

REASON FOR TEST

REMARKS 232 pound Aluminum Shaker plate

	Chamber Amb. air	Ram	41	CCO	4320	Pwr supply	Driver				
TIME	1 °C	2 °C	3 °C	4 °C	5 °C	6 °C	7 °C	8	9	10	REMARKS
1235	33	37	51	40	43	34	57				start go to 50°C
1240	43	43	57	46.5	47	45	62				
1245	44	46	59	49	51	46	65				
1250	46	49	62	51	54	48	67				go to 65°C
1255	58	55	67	58	54	55	73				
1300	58	58	73	63	64	57	77	-12.1	11.9 / 5.0	-5.0	go to 70°C
1305	64	63	73	67	68	62	82				
1310	64	67	81	70	72	64	85				go to 75°C a few ~~lines~~ dots occured
1320	70	73	87	76	78	70	91				go to 70°C
1325	66	72	87	74	77	69	90				go to 75°C
1330	72	75	89	78	79	73	92				Short vertical lines occuring in white Areas
1335	72	76	89	78	80	74	93				Lines getting Longer go to 80°C
1340	76	78	92	81	83	78	96	-12.1	11.9 / 5.0	-5.0	Lines 99% complete
1345	75	79	93	82	84	78	97				go to 90°C
1350	84	84	97	87	87	83	102				2nd + 3rd Line starting

MOTOROLA/GED E3081-01 3/71 CTL 734

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Government Electronics Division

TEMPERATURE CYCLE

SHEET 2 OF ___ CONTROL NO. 52 W.O. 4645- DATE 7-24-78

PROJECT 2513-000 UNIT ERB MODEL Eng model SERIAL n/a

TIME	1 (chamber ambient)	2 (Rum)	3 (41)	4 (LCD)	5 (4320)	6 (Env supply)	7 (Driver)	8 (table)	9	10	REMARKS
1355	83	76	100	90	90	84	104				Two more lines appearing in 3 of the Black Horiz Lines appearing every
1401	84	89	102	92	93	86	106				go to 95°c
1405	90	92	105	95	95	90	109	-18.1	+11.4 / +5.0	-5.0	40% correct, Timming prob
1410	90	93	107	97	97	91	111		+5.0		Video Breaking up Lines disappearing go to 50°c
1415	61	79	97	78	88	76	96				(CCD) 72.5°c video Partially Restored
1420	59	72	88	70	80	72	87				go to 37.8°c go to 20°c
1425	49	63	82	59	73	67	77				a few Random Errors remain
1430	34	51	74	45	66	58	65				
1435	32	43	65	39	58	53	58				Open Door
1450	33	32	64	47	57	53	67	53			a very few errors Remain go to 0°c
1455	+8	+8	50	30	41	35	48	42			(1457 All Random errors go)
1500	0	0	34	16	32	26	33	36			go to -28.9°c
1505	-17	-17	27	0	20	14	19	26			
1510	-19	-14	17	-8	10	6	10	18			go to -45.6°c
1515	-34	-34	7	-20	-2	-7	-1	7			Symetric errors at left and Blk
1520	-35	-36	0	-25	-8	-12	-4	1			go to -56.7°c
1525	-47	-48	-10	-35	-17	-23	-12	-9			starting to show symetrically
1528	-48	-48	-16	-39	-23	-27	-15	-15	-12.0 / 11.4 / +5.0	55°	video Breaking up
1535	-45	-45	-19	-39	-26	-29	-14	-18			go to -40°c
1540	-35	-35	-15	-32	-22	-25	-9	-21			go to -34.4°c
1545	-32	-32	-12	-28	-19	-24	-6	-22			
1550	-30	-30	-9	-25	-16	-23	-4	-23			

MOTOROLA INC.
Government Electronics Division

TEMPERATURE CYCLE

SHEET 3 OF ___ CONTROL NO. 52 W.O. 4645 DATE 7-24-78

PROJECT 2513-000 UNIT FRB MODEL Eng model SERIAL N/A

TIME	1 (Chamber Ambient / Ram)	2	3 (41)	4 (CCD)	5 (4320)	6 (pwr supply)	7 (Driver)	8 (Table)	9	10	REMARKS
1555	-30	-30	-8	-25	-15	-22	-3	-25			go to ~~-36.7~~ -28.9°C
1605 ~~1605~~	-25	-25	-4	-20	-12	-20	+0	-24			go to -23.3
1610 ~~1610~~	-20	-20	0	-16	-7	-16	+4	-23			
1615	-17	-17	2	-14	-5	-14	+6	-21			go to -17.8°C
1620	-15	-15	4	-11	-3	-12	8	-20			go to Amb vid-o Restored
1630	Amb										end test

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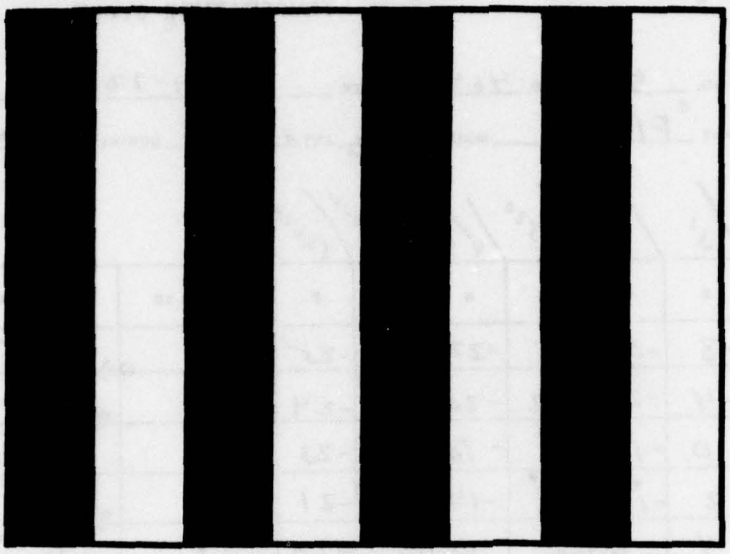


Figure 2-1. Test pattern seen on monitor at 25°C. The dark bars represent gray not black.

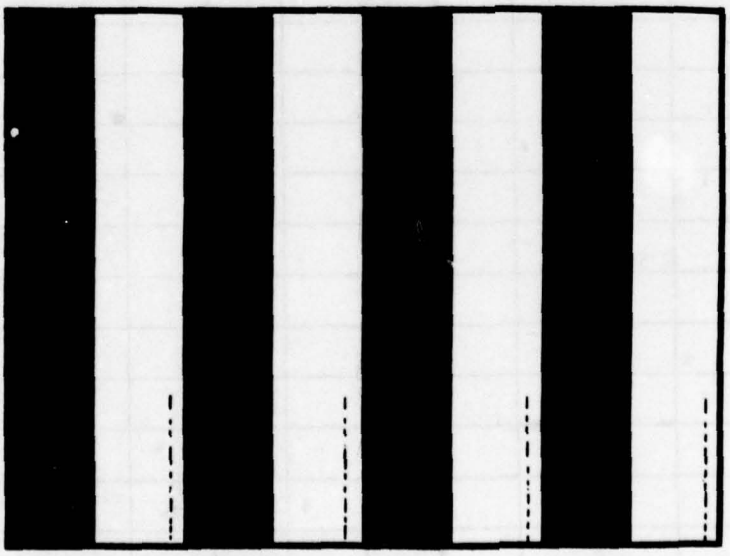


Figure 2-2. CCD at approximately 78°C.

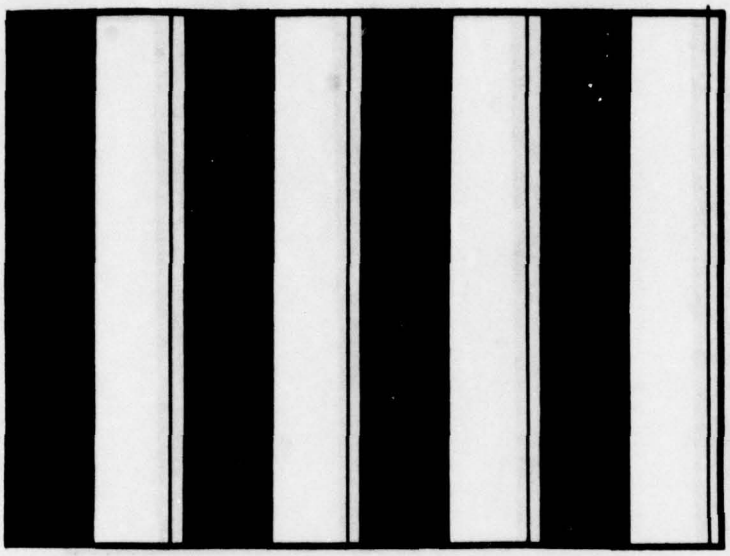


Figure 2-3. CCD at approximately 81°C.

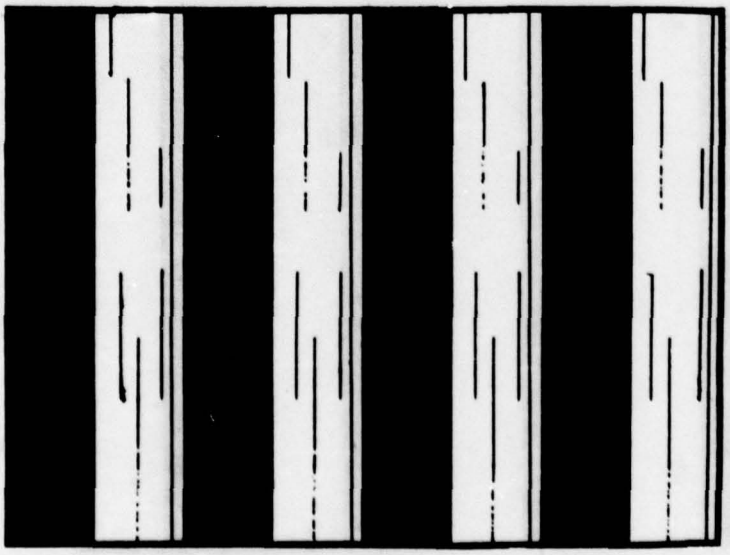


Figure 2-4. CCD at approximately 87°C. Different gray levels are not distinguished although present.

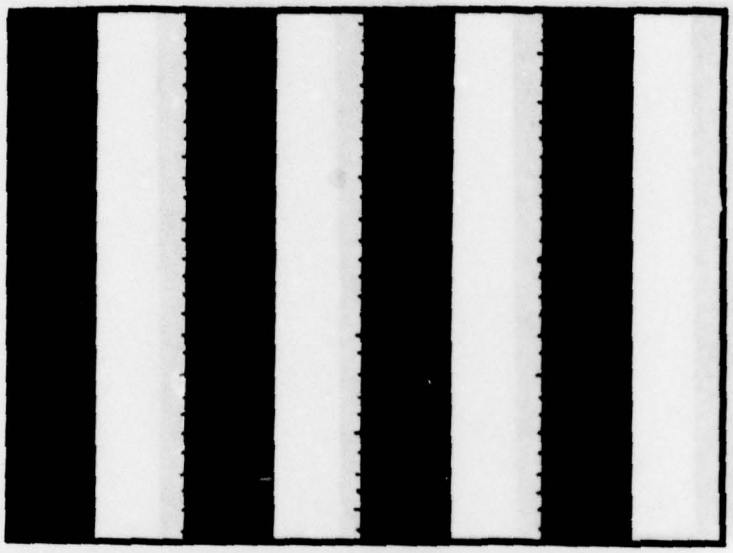
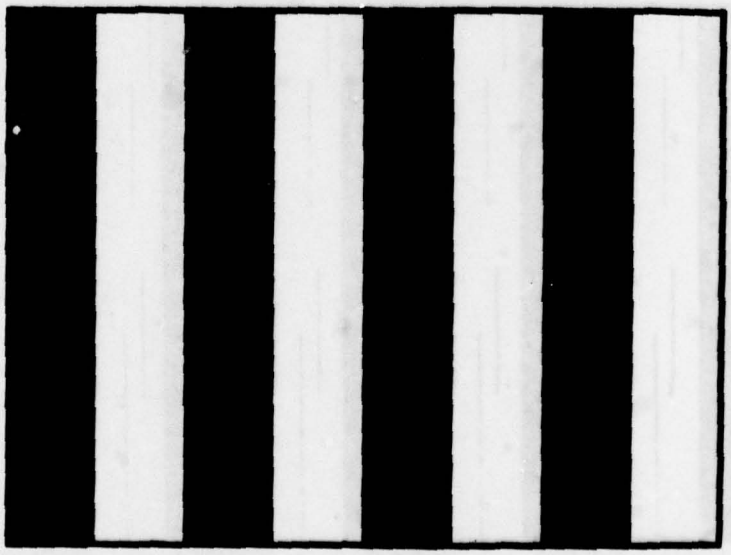


Figure 2-5. CCD at approximately -30°C.



APPENDIX D

Fairchild CCD464 64K CCD Specification

F464

65,536 X 1 DYNAMIC SERIAL MEMORY

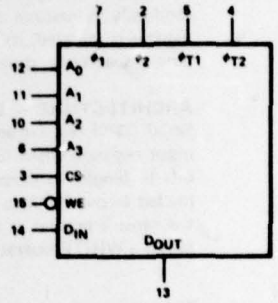
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION – The F464 is a 65,536-bit dynamic serial memory configured as 16 randomly accessible shift registers, each 4096 bits long. Each of these shift registers is designed utilizing Charge Coupled Device (CCD) techniques with the interlaced Serial-Parallel-Serial (SPS) register structure which features both low power and high density characteristics. The high density of the F464 is further enhanced through the use of an electrode-per-bit memory cell approach. The high density permits packaging the memory in a standard 16-pin (0.3"-wide) dual in-line package which allows the construction of highly dense memory systems using widely available automated testing and insertion equipment.

Furthermore, this buried-channel CCD memory is fabricated using Fairchild's double-poly n-channel Isoplanar process. This process allows the F464 to be a high performance, state-of-the-art memory circuit which is manufacturable in large volume.

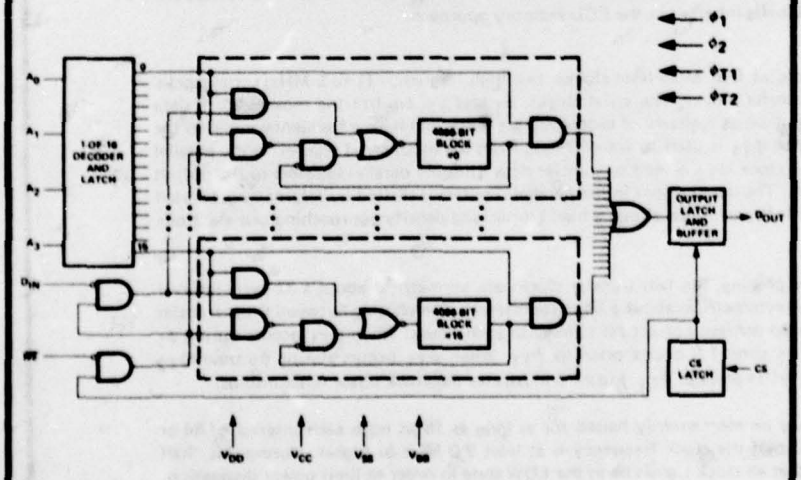
- **INDUSTRY STANDARD 16 PIN (0.3"-WIDE) DUAL IN-LINE PACKAGE.**
- **OPERATING FREQUENCY RANGE: 1 MHz TO 5 MHz.**
- **15 μs HALT TIME AT 2.0 MHz**
- **LOW CAPACITANCE TTL-COMPATIBLE INPUTS (EXCEPT CLOCKS).**
- **3-STATE, TTL-COMPATIBLE, LATCHED DATA OUTPUT.**
- **OUTPUT DRIVE CAPABILITY: 3.5 mA**
- **LOW CAPACITANCE 12 V CLOCKS:**
  - **ϕ_1 AND ϕ_2: 100 pF (TYP)**
  - **ϕ_{T1} AND ϕ_{T2}: 30 pF (TYP)**
- **LOW POWER**
  - **NORMAL OPERATION: <336 mW (MAX) @ f_{max}**
  - **STANDBY: <66 mW (MAX) @ f_{min}**
- **STANDARD POWER SUPPLIES (+12 V, +5 V, AND −5 V)**

LOGIC SYMBOL

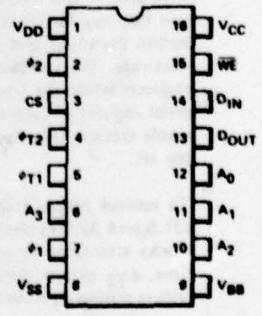


V_{DD} - PIN 1
V_{CC} - PIN 16
V_{SS} - PIN 8
V_{BB} - PIN 9

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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203-11-0005-087 15M

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

PIN NAMES

ϕ_1, ϕ_2	Serial Clocks	D_{IN}	Data Input
ϕ_{T1}, ϕ_{T2}	Transfer Clocks	D_{OUT}	Data Output
A_n	Address Inputs	V_{CC}	+5 V Power Supply
CS	Chip Select Input	V_{SS}	0 V Power Supply, GND
$\overline{WE}$	Write Enable Input (Active LOW)	V_{BB}	−5 V Power Supply
		V_{DD}	+12 V Power Supply

FUNCTIONAL DESCRIPTION

ORGANIZATION – The F464 is a 65,536 x 1 bit dynamic serial memory organized internally as 16 dynamic shift registers (or blocks) of 4096 bits each in length. These 16 shift register blocks are randomly accessible through four internally decoded Address inputs (A_0 – A_3). When a given register is selected, its input and output are internally connected (as needed) to the D_{IN} and D_{OUT} pins, respectively, thus permitting simultaneous read and write operations.

ARCHITECTURE – Each of the sixteen shift register blocks is implemented using a Serial-Parallel-Serial (SPS) register architecture. In this approach N data bits are sequentially shifted into a "serial" input register. When full, the entire N-bit word is shifted in parallel into N "parallel" registers of M bits in length, as illustrated in Figure 1. At the other end of this parallel register structure, bits are loaded in parallel into an N-bit serial output register. Bits in this register are then shifted out toward the sense amplifier at the output and are automatically recirculated back to the input serial register unless a WRITE operation is specified.

The primary advantages of this type of architecture include very high density, low power, and low clock capacitance. These features all result from the fact that in the SPS architecture the parallel registers which encompass most of the total storage capacity within each block are shifted at a considerably slower rate (f_{IN}/N) than the clock rate of the input or output serial registers (f_{IN}).

In actuality, each 4096-bit block of the F464 is implemented using an "interlaced" SPS structure in which each bit of the input serial register services two parallel registers rather than just one. The same is true for the output serial register. In addition, "electrode-per-bit" design techniques are used to reduce the effective cell size by minimizing the number of electrodes used to store each bit of information. These techniques obviously enhance the memory density considerably. The dimensions of the F464's interlaced SPS structure are 32-bit input and output serial registers and 64 parallel registers, each 63 bits in length. See Figure 2. These dimensions were chosen in order to optimize the power/density/latency tradeoffs inherent in the CCD memory approach.

CLOCKS – The F464 requires four MOS level clocks: two high frequency (1 to 5 MHz) serial clocks and two low frequency transfer clocks. The serial clocks, ϕ_1 and ϕ_2, control the movement of data within the input and output serial registers of each 4096-bit block and have a frequency equal to the data rate. The transfer clock ϕ_{T1} is used to transfer data from the input serial register to the parallel registers while the transfer clock ϕ_{T2} is used to transfer data from the parallel registers to the output serial register of each block. The data present in the parallel registers is shifted by internally generated ripple clocks. This ripple clock technique allows a high bit-packing density approaching one electrode per bit.

To achieve proper transfer phasing, the two transfer clocks are asymetrical about a 32-cycle interval (31.5 and 32.5 cycles) but symmetrical about a 64-cycle interval. The phasing between these transfer clocks alternates in order to achieve correct bit storage in each block. When ϕ_{T1} occurs during ϕ_1 time, ϕ_{T2} occurs during ϕ_2 time 1.5 cycles prior to ϕ_{T1}. When ϕ_{T1} occurs during ϕ_2 time, ϕ_{T2} occurs during ϕ_1 time 2.5 cycles prior to ϕ_{T1}. Figure 3 illustrates the clock phase relationships.

The clocking operation may be momentarily halted for as long as 15 μs once each interval of 64 or more clock cycles provided that the clock frequency is at least 2.0 MHz or higher. During this "halt time" it is recommended that all clock signals be in the LOW state in order to limit power dissipation.

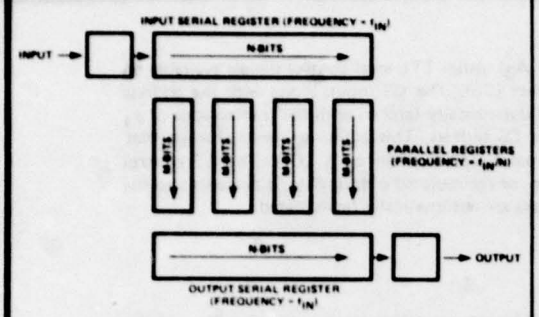


Fig. 1 SIMPLIFIED SPS EXAMPLE WITH N = 4

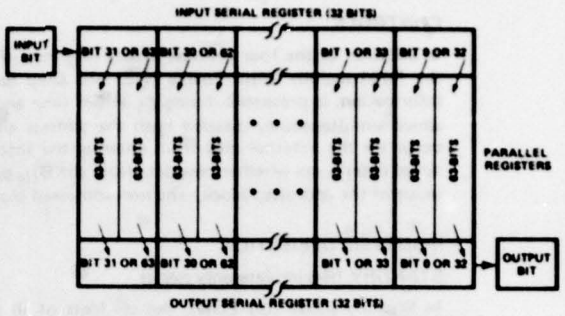
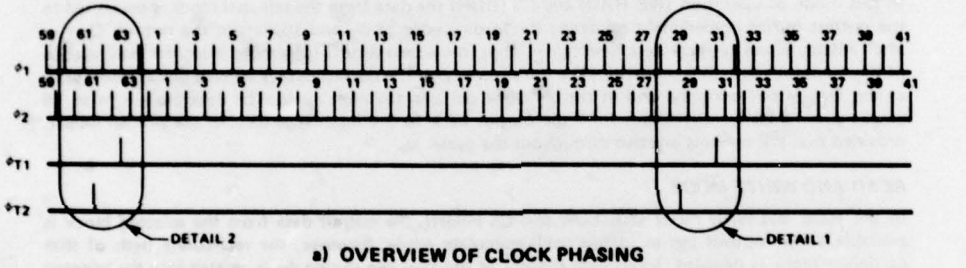
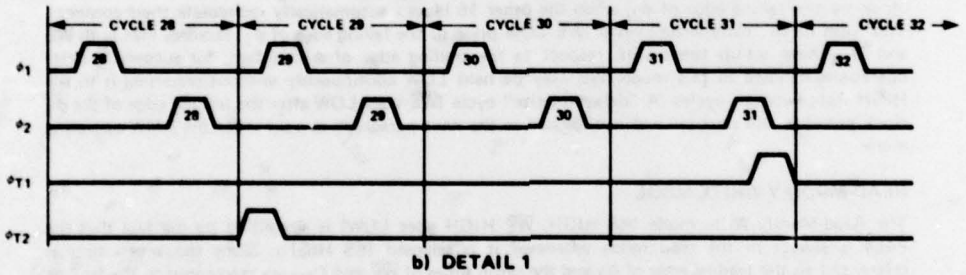


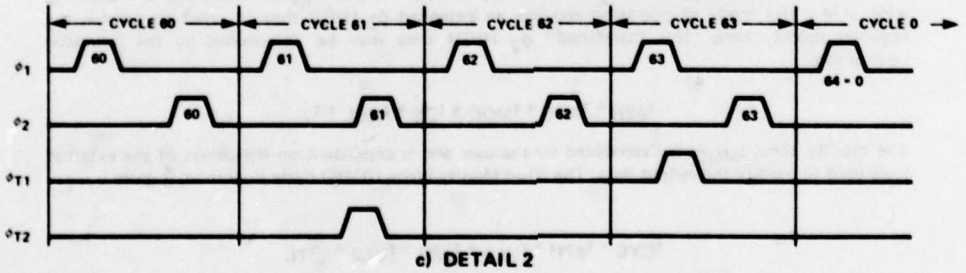
Fig. 2 INTERLACED SPS ARCHITECTURE



a) OVERVIEW OF CLOCK PHASING



b) DETAIL 1



c) DETAIL 2

Fig. 3 F464 CLOCK RELATIONSHIPS

CONTROLS

In addition to the four Address inputs (A_0 through A_3), other TTL level control signals available on the F464 include Write Enable ($\overline{WE}$) and Chip Select (CS). The CS input, along with the address information, is presented during ϕ_1 HIGH time and dynamically latched with the trailing edge of ϕ_1 which simultaneously disables both the address and CS buffers. This action prevents changes that occur on the external pins from entering the internal circuitry when ϕ_1 is LOW. The $\overline{WE}$ control signal determines whether new data from the D_{IN} pin, or recirculated output data, is presented to the input of the addressed block. The non-addressed blocks are automatically recirculated.

MODES OF OPERATION

STANDBY (Recirculate-only cycle)

In Standby mode (CS LOW), the contents of all 16 blocks are recirculated automatically, and the device disregards the $\overline{WE}$, Address, and D_{IN} inputs. The output latch goes into the high impedance state after the trailing edge of the ϕ_1 clock. Minimum power dissipation results when the device is operated in the recirculate mode with minimum ϕ_1 and ϕ_2 pulse widths at the lowest allowed frequency.

READ-RECIRCULATE MODE

In this mode of operation ($\overline{WE}$ HIGH and CS HIGH) the data from the selected block is presented to the output buffer immediately following the leading edge of ϕ_2 and appears at the output, D_{OUT}, after a delay equal to the access time t_{ACC}. Thus, the access time is referenced from the leading edge of the ϕ_2 pulse and is independent of the duration of ϕ_2. The output data is latched and remains valid at the D_{OUT} pin until the end of the ϕ_1 clock pulse in the next cycle. The data present in all 16 blocks automatically recirculates from the output back to the input regardless of the address inputs, provided that $\overline{WE}$ remains inactive throughout the cycle.

READ AND WRITE MODE

In the Read and Write mode ($\overline{WE}$ LOW and CS HIGH), the output data from the selected block is available at the output pin as in the read-recirculate mode; however, the recirculate path of that particular block is disabled. Input data present at the D_{IN} pin during ϕ_2 is written into the selected block by the falling edge of ϕ_2, while the other 15 blocks automatically recirculate their contents. This form of an "early-write" cycle ($\overline{WE}$ LOW prior to the falling edge of ϕ_1) requires that both $\overline{WE}$ and D_{IN} have set-up times with respect to the trailing edge of ϕ_1. In fact, for successive write operations handled in this mode, $\overline{WE}$ may be held LOW continuously without returning it to the HIGH state between cycles. A "delayed-write" cycle ($\overline{WE}$ goes LOW after the trailing edge of the ϕ_1 clock pulse) is also possible and is discussed in the next paragraph as a subset of the RMW operating mode.

READ-MODIFY-WRITE MODE

The Read-Modify-Write mode (CS HIGH, $\overline{WE}$ HIGH goes LOW) is simplified by the fact that the F464 is always in the read mode whenever it is selected (CS HIGH). Since the access time is referenced to the leading edge of ϕ_2 and the setup times of $\overline{WE}$ and D_{IN} are referenced to the trailing edge of ϕ_2, this mode of operation requires an extended ϕ_2 HIGH time in order to provide the required modify time. This "stretched" ϕ_2 HIGH time may be determined by the following relationship:

$$t_{\phi 2H} = t_{ACC} + t_{MOD} + t_{DS} + t_{WCL} + t_T$$

The modify time, t_{MOD}, is determined by the user and is dependent on the delays of the external logic used to modify the output data. The Read-Modify-Write (RMW) cycle time then, is given by:

$$t_{CYC} = t_{\phi 1H} + t_{UL1} + t_{\phi 2H} + t_{UL2} + 4t_{TC}$$

where $t_{\phi 2H}$ is the new "stretched" version of the ϕ_2 clock pulse.

If no modification of output data is required, then this operating mode reduces to a "delayed-write" mode in which D_{IN} and $\overline{WE}$ may occur after the ϕ_1 clock pulse.

MEMORY START-UP

When the F464 is initially powered up, the V_{BB} supply (i.e., the −5 volt supply) should be applied to the memory before and removed after the other supplies. This action results in greater protection against accidental violation of the voltage limits specified in the Absolute Maximum Ratings section and, in general, enhances the long term reliability of the memory.

In order to clear the memory of extraneous charge following power-up or after a clock stoppage of greater than 15 μs, the F464 must be clocked through a minimum of 20,000 clock cycles of any type before a valid memory cycle should be attempted.

ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	−0.5 V to +20 V
Operating Temperature (Ambient)	0°C to 55°C
Storage Temperature (Ambient)	−55°C to 150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC REQUIREMENTS: $T_A = 0°C$ to $55°C$ (See Note 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12	12.6	V	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{SS}	Supply Voltage	0	0	0	V	1
V_{BB}	Supply Voltage	−5.5	−5.0	−4.5	V	
V_{IHC}	Input HIGH Clock Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{ILC}	Input LOW Clock Voltage	−0.5		0.8	V	2
$\lvert\Delta V_{ILC}\rvert$	Voltage Differential Between Any Two Clock LOWS	0		0.8	V	2
V_{IH}	Input HIGH Voltage, all inputs except clocks	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage, all inputs except clocks	−0.5		0.8	V	

DC ELECTRICAL CHARACTERISTICS: Over Full Range of Voltage and Temperature (See Note 1)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current	Active	f_{min}		5	8	mA	3, 10
			f_{max}		15	25	mA	
		Standby	f_{min}		3	5	mA	
			f_{max}		12	19	mA	
I_{CC}	Average V_{CC} Current	Active	f_{min}		1.5	2.5	mA	3, 10
			f_{max}		2.5	4	mA	
		Standby	f_{min}		0.3	0.5	mA	
			f_{max}		1.2	2	mA	
I_{BB}	Average V_{BB} Current					100	μA	4
V_{OH}	Output HIGH Voltage			2.8			V	5
V_{OL}	Output LOW Voltage					0.4	V	6
I_{IN}	Input Leakage Current (any input)			−10		10	μA	7
I_{OUT}	Output Leakage Current			−10		10	μA	8
C_{IN1}	Input Capacitance, ϕ_1 and ϕ_2				100		pF	9
C_{IN2}	Input Capacitance, ϕ_{T1} and ϕ_{T2}				30		pF	9
C_{IN3}	Input Capacitance, $A_0 - A_3$, CS, $\overline{WE}$, and D_{IN}				5		pF	9
C_{OUT}	Output Capacitance, D_{OUT}				7		pF	9

RECOMMENDED CLOCKING CONDITIONS: Over Full Range of Voltage and Temperature (See Note 11)

IEEE SYMBOL	SYMBOL	PARAMETER	F464-2		F464-3		F464-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
TE1HE1L	$t_{\phi 1H}$	ϕ_1 HIGH Pulse Width	50	200	60	200	100	200	ns	10
TE2HE2L	$t_{\phi 2H}$	ϕ_2 HIGH Pulse Width	50	300	60	300	100	300	ns	10
TE1LE2H	t_{UL1}	ϕ_1 to ϕ_2 Underlap Time	30		45		100		ns	
TE2LE1H	t_{UL2}	ϕ_2 to ϕ_1 Underlap Time	30		45		100		ns	
TTHEL	t_{OV1}	ϕ_{T1} and (ϕ_1 or ϕ_2) Overlap Time	30		30		50		ns	
TEHTL	t_{OV2}	ϕ_{T2} and (ϕ_1 or ϕ_2) Overlap Time	20		30		50		ns	
TEHTH	t_{T1D}	(ϕ_1 or ϕ_2) to ϕ_{T1} Delay Time	0		0		0		ns	
TTLEH	t_{T1S}	ϕ_{T1} to (ϕ_1 or ϕ_2) Setup Time	0		0		0		ns	
TELTH	t_{T2D}	(ϕ_1 or ϕ_2) to ϕ_{T2} Delay Time	0		0		0		ns	
TTLEL	t_{T2S}	ϕ_{T2} to (ϕ_1 or ϕ_2) Setup Time	5		5		5		ns	
TELTL	t_{T1HD}	ϕ_{T1} Hold Time	20		30		50		ns	
–	t_T	Transition Time (Except Clocks)	3	50	3	50	3	50	ns	11
–	t_{TC}	Clock Transition Time (Rise and Fall)	10	50	10	50	10	50	ns	11,12
–	f	Operating Frequency	1.0	5.0	1.0	4.0	1.0	2.0	MHz	12
–	t_{HALT}	Halt Time @ 2 MHz		15		15		15	μs	17

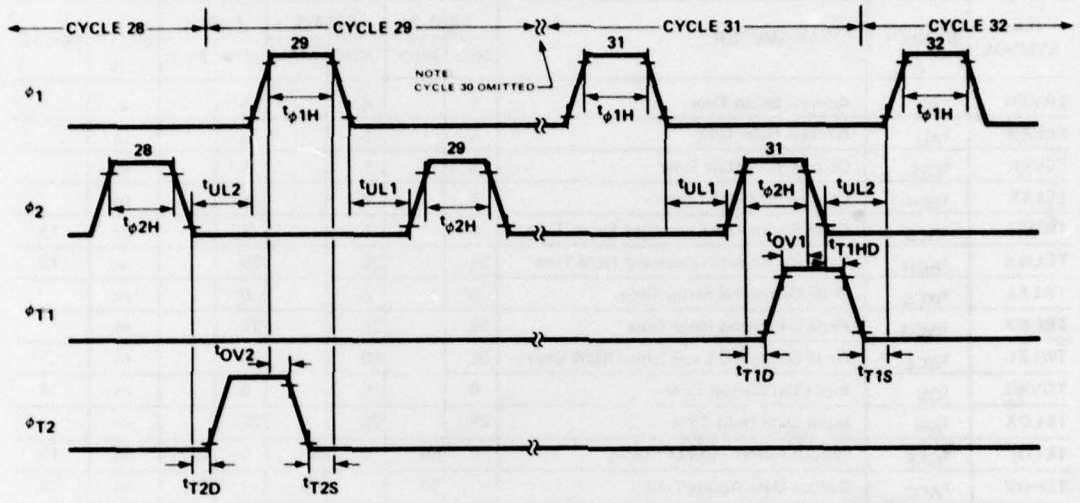
RECOMMENDED AC OPERATING CONDITIONS: Over Full Range of Voltage and Temperature

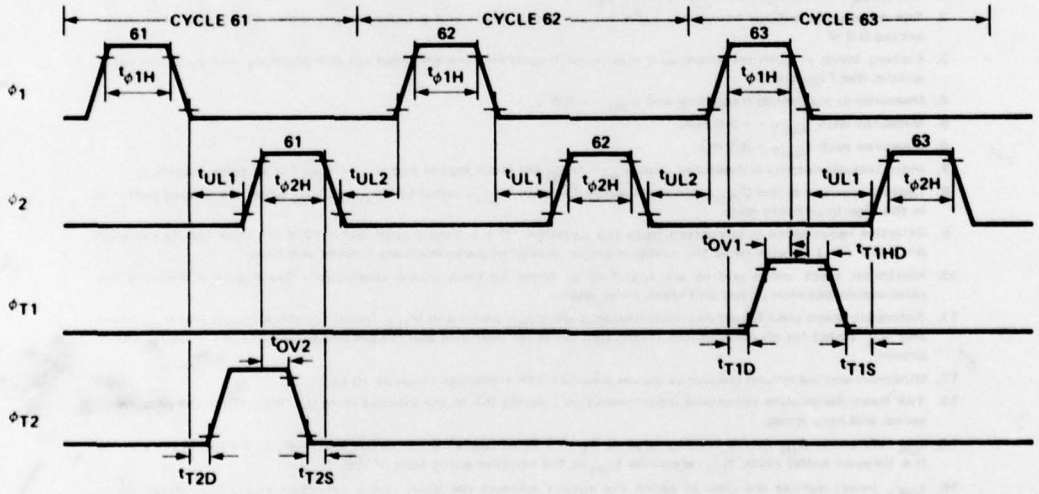
IEEE SYMBOL	SYMBOL	PARAMETER	F464-2		F464-3		F464-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
TAVEH	t_{AS}	Address Setup Time	5		5		5		ns	
TELAX	t_{AH}	Address Hold Time	5		5		5		ns	
TSVEH	t_{CSS}	Chip Select Setup Time	5		5		5		ns	
TELSX	t_{CSH}	Chip Select Hold Time	5		5		5		ns	
TWHEL	t_{RCS}	Read-Recirculate Command Setup Time	5		5		5		ns	13
TELWX	t_{RCH}	Read-Recirculate Command Hold Time	25		25		25		ns	13
TWLEL	t_{WCS}	Write Command Setup Time	0		0		0		ns	
TELWX	t_{WCH}	Write Command Hold Time	25		25		25		ns	
TWLEL	t_{WCL}	Write Command Lead Time (RMW Only)	60		60		60		ns	
TDVWL	t_{DS}	Input Data Setup Time	0		0		0		ns	14
TELDX	t_{DH}	Input Data Hold Time	25		25		25		ns	
TELQZ	t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	50	0	50	ns	15
TEHQV	t_{ACC}	Output Data Access Time		50		60		70	ns	16

NOTES:

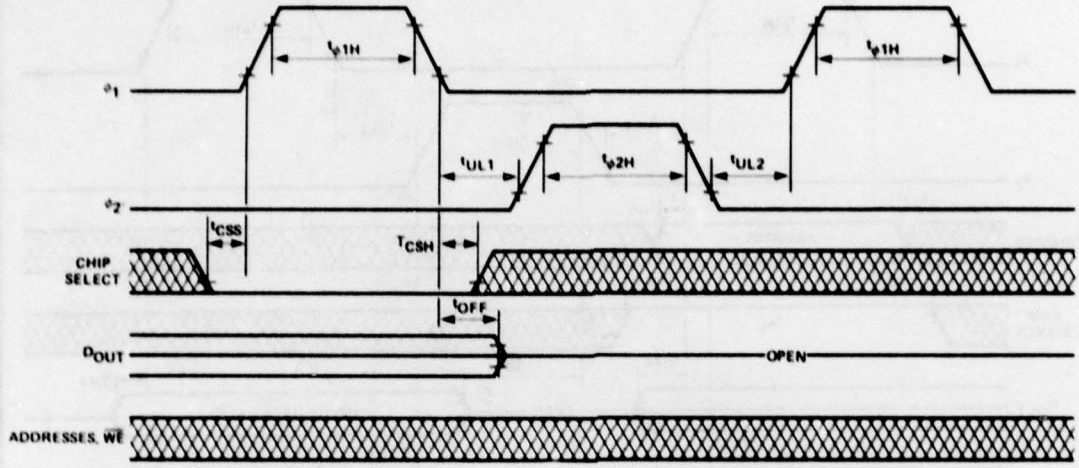
1. All voltages are measured with respect to V_{SS}.
2. The differential voltage between a LOW for any clock input and a LOW for any other clock input should not exceed 0.8 V.
3. Current levels at both minimum and maximum frequencies are specified for minimum ϕ_1 and ϕ_2 clock pulse widths. See Figure 4.
4. Measured at maximum frequency and $V_{BB} = -5.5$ V.
5. Measured with $I_{OUT} = -2.5$ mA.
6. Measured with $I_{OUT} = 3.5$ mA.
7. *Input leakage current is measured with* $V_{IN} = V_{DD}$ for clock inputs and $V_{IN} = V_{CC}$ for all other inputs.
8. Leakage current at the D_{OUT} pin is measured for both V_{OUT} equal to V_{CC} and V_{SS} when the output buffer is in the high impedance state.
9. Effective capacitance is calculated from the equation $C = I\,\Delta t/\Delta V$ with $\Delta V = 12$ V for clock inputs and with $\Delta V = 3$ V for TTL pins while the device is active. Measured parameters are current and time.
10. Maximum clock pulse widths are specified in order to limit power dissipation. See Figure 4 showing the relationship between power and clock pulse width.
11. Reference levels used for timing measurements are V_{IHC} (min) and V_{ILC} (max) for clock inputs and V_{IH} (min) and V_{IL} (max) for all other inputs. Transition times for both rise and fall are measured between these reference points.
12. Minimum and maximum frequency values assume clock transition times of 10 ns.
13. The Read-Recirculate command is performed by keeping $\overline{WE}$ in the inactive state (i.e. HIGH) for the prescribed set-up and hold times.
14. t_{DS} references D_{IN} to the trailing edge of ϕ_1 in a Read-(early) Write cycle. However, in a Read-Modify Write (i.e. delayed write) cycle, t_{DS} references D_{IN} to the negative-going edge of $\overline{WE}$.
15. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
16. Measured with a load equivalent to two TTL loads and 100 pF. See Fig. 5.
17. The clocking operation maybe momentarily halted for as long as 15 μs once each interval of 64 or more clock cycles provided that the clock frequency is at least 2.0 MHz or higher. During this "halt time" it is recommended that all clock signals be in the LOW state in order to limit power dissipation.

SERIAL AND TRANSFER CLOCKS

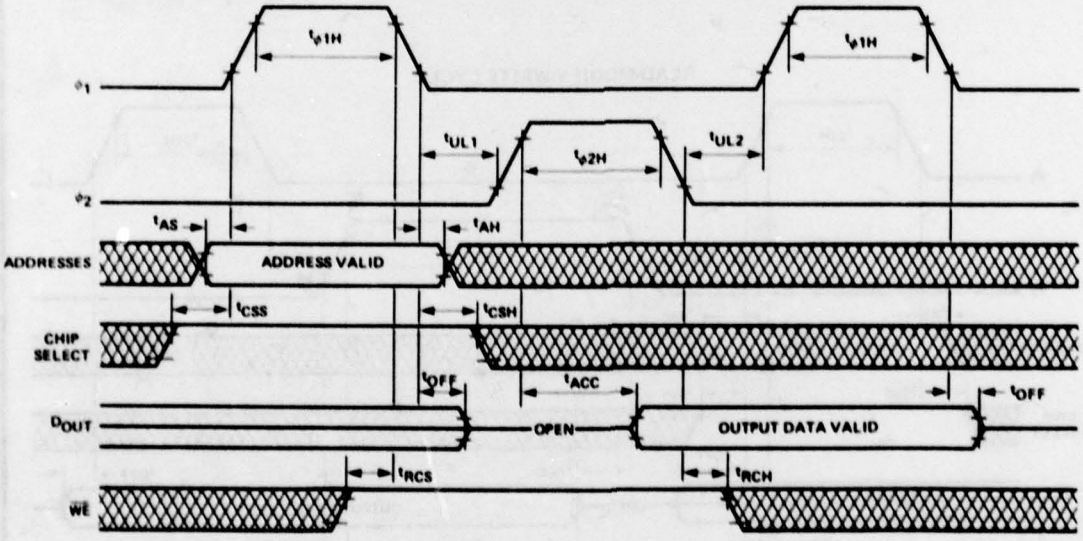




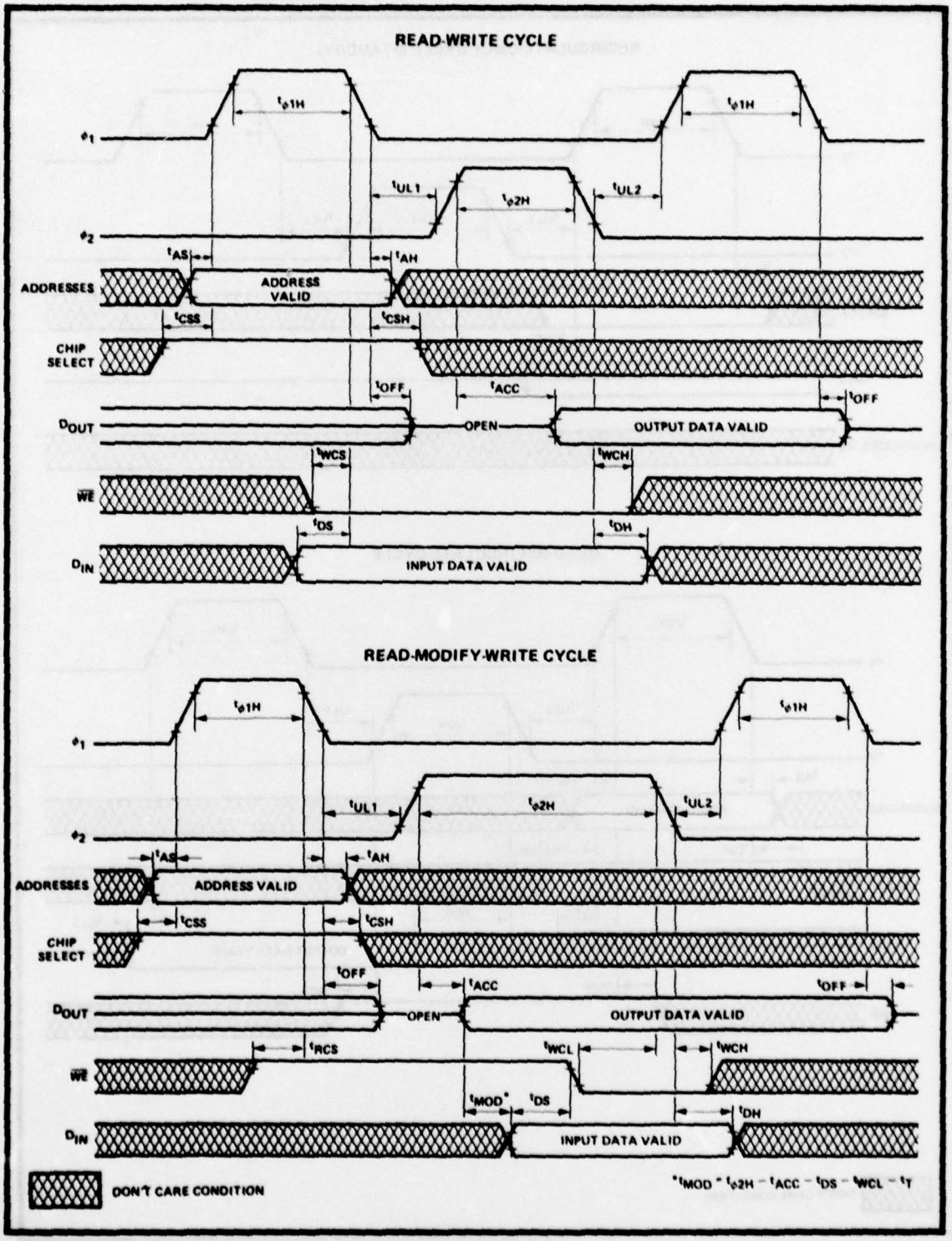
RECIRCULATE-ONLY CYCLE (STANDBY)



READ-RECIRCULATE-CYCLE



DON'T CARE CONDITION


READ-WRITE CYCLE
$t_{\phi 1H}$
ϕ_1
t_{UL1}
$t_{\phi 2H}$
t_{UL2}
ϕ_2
t_{AS}
t_{AH}
ADDRESSES
ADDRESS VALID
t_{CSS}
t_{CSH}
CHIP SELECT
t_{OFF}
t_{ACC}
D_{OUT}
OPEN
OUTPUT DATA VALID
t_{WCS}
t_{WCH}
$\overline{WE}$
t_{DS}
t_{DH}
D_{IN}
INPUT DATA VALID
READ-MODIFY-WRITE CYCLE
t_{RCS}
t_{WCL}
t_{MOD}*
DON'T CARE CONDITION
*$t_{MOD} = t_{\phi 2H} - t_{ACC} - t_{DS} - t_{WCL} - t_T$

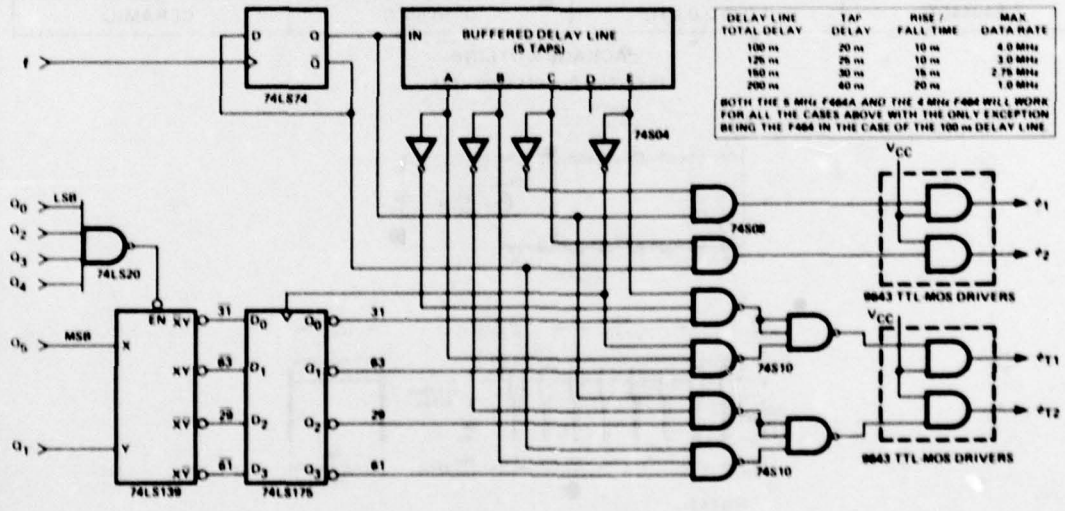
CLOCK GENERATION CIRCUIT –

The circuit shown below may be used to generate the four MOS-level clocks required of the F464 from a single master clock. In this circuit, the master clock frequency f, must be twice the desired data rate at the F464 output pin. Since the input clock frequency is "squared-up" with a divide-by-two flip-flop, the duty cycle of this clock is non-critical. A pulse edge at the input of the buffered delay line produces a sequence of delayed pulse edges from the A, B, C, D and E output taps. These delayed pulse edges are ANDed together to produce the required ϕ_1 and ϕ_2 clocks as well as the ϕ_{T1} and ϕ_{T2} transfer clocks. Since the transfer clocks occur in a symmetrical fashion every 64 clock cycles, a 6-bit, modulo 64 counter is required. The outputs of this 6-bit counter are decoded to enable the appropriate transfer clock gates at counts of 29, 31, 61 and 63. Thus, ϕ_{T1} is passed along to the clock drivers only during cycles 31 and 63, while ϕ_{T2} is gated through only during cycles 29 and 61. These four counts are easily decoded with only a 2-to-4 decoder and one 4-input NAND gate. The 6 bits of the modulo 64 counter comprise the 6 low order bits of the 12-bit, modulo 4096 loop counter. This counter is required to define address locations within each 4K block and will, in most cases, be already present in the system.

One major advantage of using a delay line is that since the clock pulses are generated from delayed edges, the pulse width in all cases is fixed and does not vary as a function of the input master frequency f. Thus minimum pulse widths are always generated regardless of cycle and data rates. This translates directly into lower power dissipation since I_{DD} is a function of clock pulse width.

The maximum clock rates for which this circuit will operate properly depends on the clock transition times (both rise and fall) at the output of the TTL-to-MOS drivers and, the delay between adjacent taps on the delay line. The maximum data rates possible for this circuit are given in the table. Faster and/or more efficient clock generation circuits may be realized by using different types of delay lines (e.g. more taps or unequal tap delays).

SERIAL AND TRANSFER CLOCK GENERATION CIRCUIT



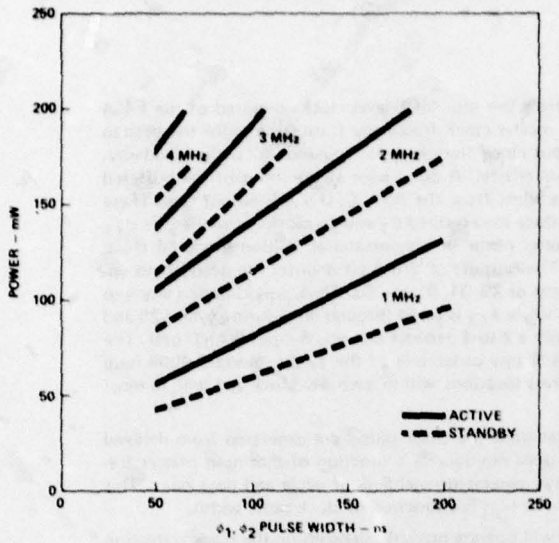


Fig. 4 TYPICAL POWER DEPENDENCE ON CLOCK PULSE WIDTH

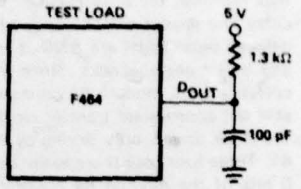


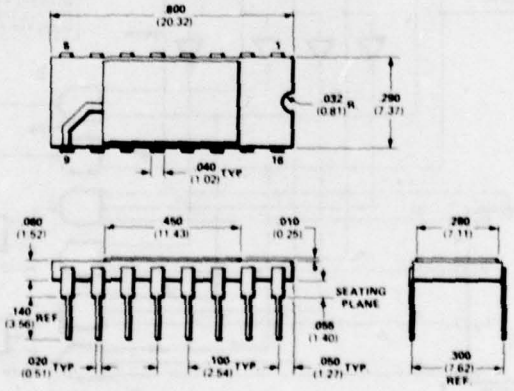
Fig. 5 TEST LOAD

ORDERING INFORMATION

PART NUMBER	OPERATING FREQUENCY RANGE	TEMPERATURE RANGE	PACKAGE (See Below)
F4642DC	1.0 to 5.0 MHz	0° to 55°C	CERAMIC
F4643DC	1.0 to 4.0 MHz	0° to 55°C	CERAMIC
F4644DC	1.0 to 2.0 MHz	0° to 55°C	CERAMIC

PACKAGE OUTLINE

16-Pin Side-Brazed Ceramic DIP



NOTES:
Dimensions in inches (bold), millimeters in parentheses.
Header body is black ceramic.
Lid is gold plated kovar.
Pin #9 is common to substrate.
Package is hermetic.
Package weight is 1.1 grams.

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.
Manufactured under one of the following U.S. Patents: 2981877; 3015048; 3064167; 3108359; 3117260; other patents pending.

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