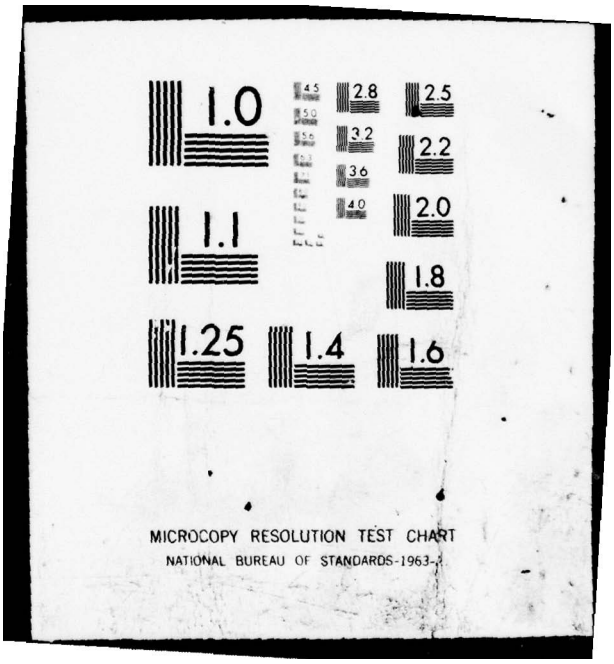
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TRUE-INTEGRATING ENVIRONMENTAL NOISE MONITOR AND SOUND EXPOSURE--ETC(U)
JUN 79 A J AVERBUCH, P D SCHOMER

UNCLASSIFIED CERL-TR-N-41-VOL-2 NL

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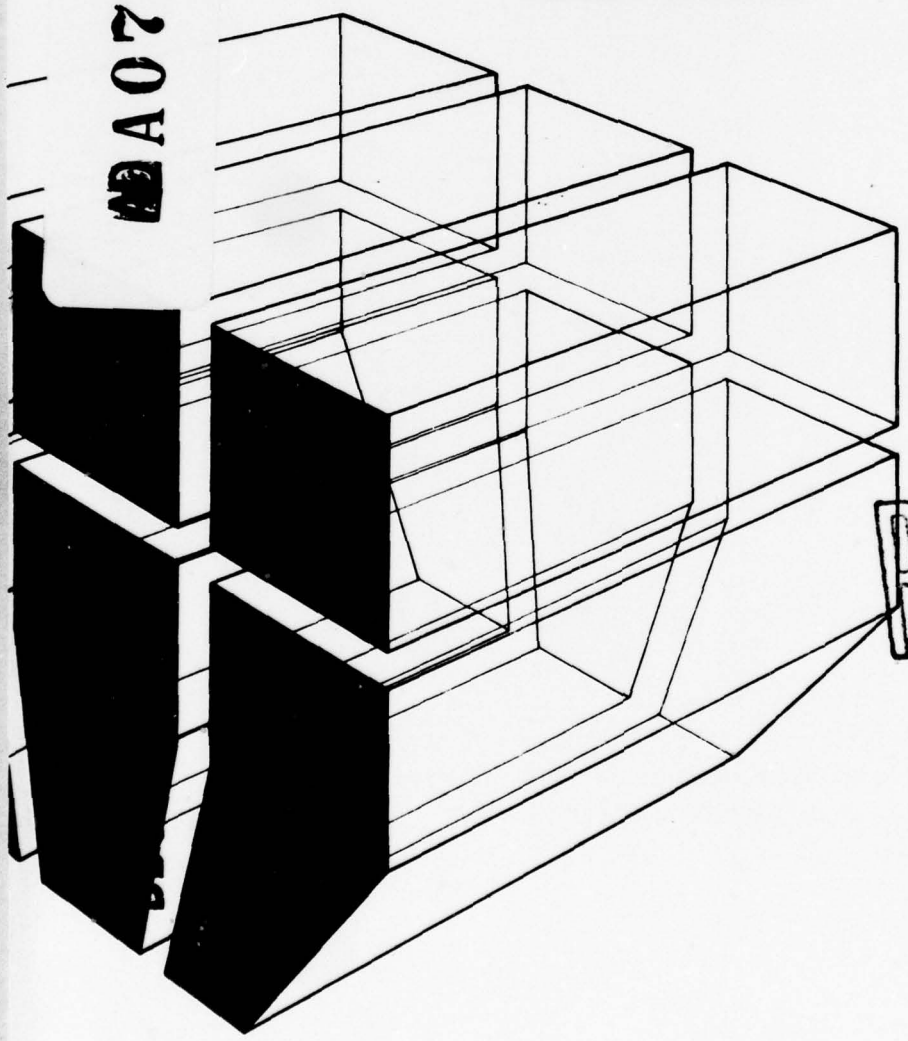
TECHNICAL REPORT N-41
June 1979
Prediction of the Noise Impact Within and Adjacent to Army Facilities

TRUE-INTEGRATING ENVIRONMENTAL NOISE MONITOR AND SOUND EXPOSURE LEVEL METER VOLUME II: WIRING AND PARTS LISTS, PARTS LAYOUTS, AND SCHEMATICS

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LEVEL II

ADGO 958



by
A. J. Averbuch
P. D. Schomer
M. W. Weisberg

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report provides the complete hardware construction of the CERL environmental noise monitor. Included are: (1) a task block diagram of the unit, (2) a parts list and diagram of the front panel, (3) a parts list and diagram of the power supply circuit, (4) a list of the back plane wiring, (5) parts list, layout, and schematics of the PC boards, and (6) wiring list for cables and connectors.

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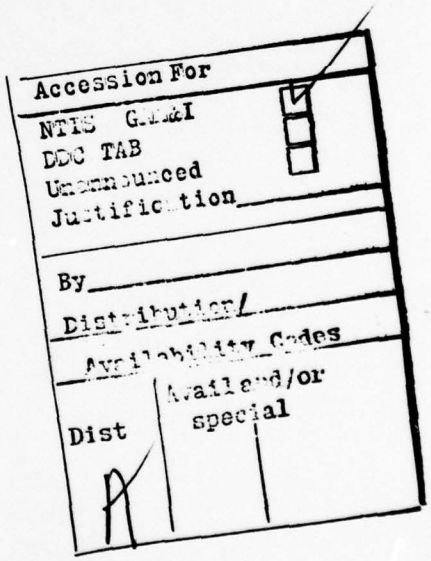
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FOREWORD

This research was conducted for the Directorate of Military Programs, Office of the Chief of Engineers (OCE), under Project 4A762720A896, "Environmental Quality for Construction and Operation of Military Facilities"; Task 03, "Pollution Control Technology"; Work Unit 001, "Prediction of the Noise Impact Within and Adjacent to Army Facilities." The QCR number is 1.03.011. Mr. F. P. Beck, DAEN-MPE-I, is the OCE Technical Monitor.

The work was performed by the Environmental Division (EN), U.S. Army Construction Engineering Research Laboratory (CERL). Dr. R. K. Jain is Chief of EN.

COL J. E. Hays is Commander and Director of CERL, and Dr. L. R. Shaffer is Technical Director.



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TRUE-INTEGRATING ENVIRONMENTAL
NOISE MONITOR AND SOUND-
EXPOSURE LEVEL METER
VOLUME II: MONITOR CONSTRUCTION --
PARTS, LAYOUT, AND SCHEMATICS

1 INTRODUCTION

Background

The Environmental Protection Agency (EPA) has recommended the day-night average level (L_{dn}) as the measure to use for assessing normal environmental noise, and the C-weighted day-night level (L_{Cdn}) as the measure for assessing impulsive noises (for example, from artillery, armor, sonic boom, etc.). Explicit in the EPA's recommendation is a requirement to directly integrate the instantaneous square of the sound pressure as a function of time. In a practical sense, this direct integration can be approximated for most continuous noise sources by integration the output of a root-mean-square (RMS) detector (for example, like the detector employed in the normal sound-level meter). However, in the case of highly impulsive noises, and especially for single events, the integration of an RMS detector output may yield erroneous results because the quantity found is the impulse response of the detector itself, rather than the true square of the pressure as a function of time.

The Construction Engineering Research Laboratory (CERL) has designed and constructed monitors for its own use and for the Federal EPA; in addition, CERL has studied the features of commercial noise monitors for the Federal EPA[1] and participated in the National Academy of Science efforts to define noise assessment procedures for Federal activities.[2] These studies have made apparent certain physical characteristics within the design of the monitor for measuring Army-specific noises (see Volume I).

---

1 P. D. Schomer and A. J. Averbuch, Analysis of Environmental Noise Monitors, Technical Report N-21/ADA040005 (U.S. Army Construction Engineering Research Laboratory [CERL], April 1977).

2 Guidelines for Preparing Environmental Impact Statements on Noise, Report of Working Group 69 on Environmental Impact of Noise, Committee on Hearing, Bioacoustics, and Biomechanics, Assembly of Behavioral and Social Sciences (National Research Council of the National Academy of Sciences, 1977).

Purpose

The purpose of this report is to describe the construction, and provide parts lists, layout, and schematics for the CERL environmental noise monitor.

Outline of Report

Chapter 2 provides a block diagram of the monitor. Chapter 3 provides a parts list and diagram of the front panel. Chapter 4 provides a parts list of the monitor's power supply circuit. Chapter 5 is a list of the monitor's back plane wiring components, and Chapter 6 provides a parts list, parts layout, and schematics for the PC Boards. Chapter 7 is a list of the monitor's cable and connector wiring.

2 BLOCK DIAGRAM OF MONITOR

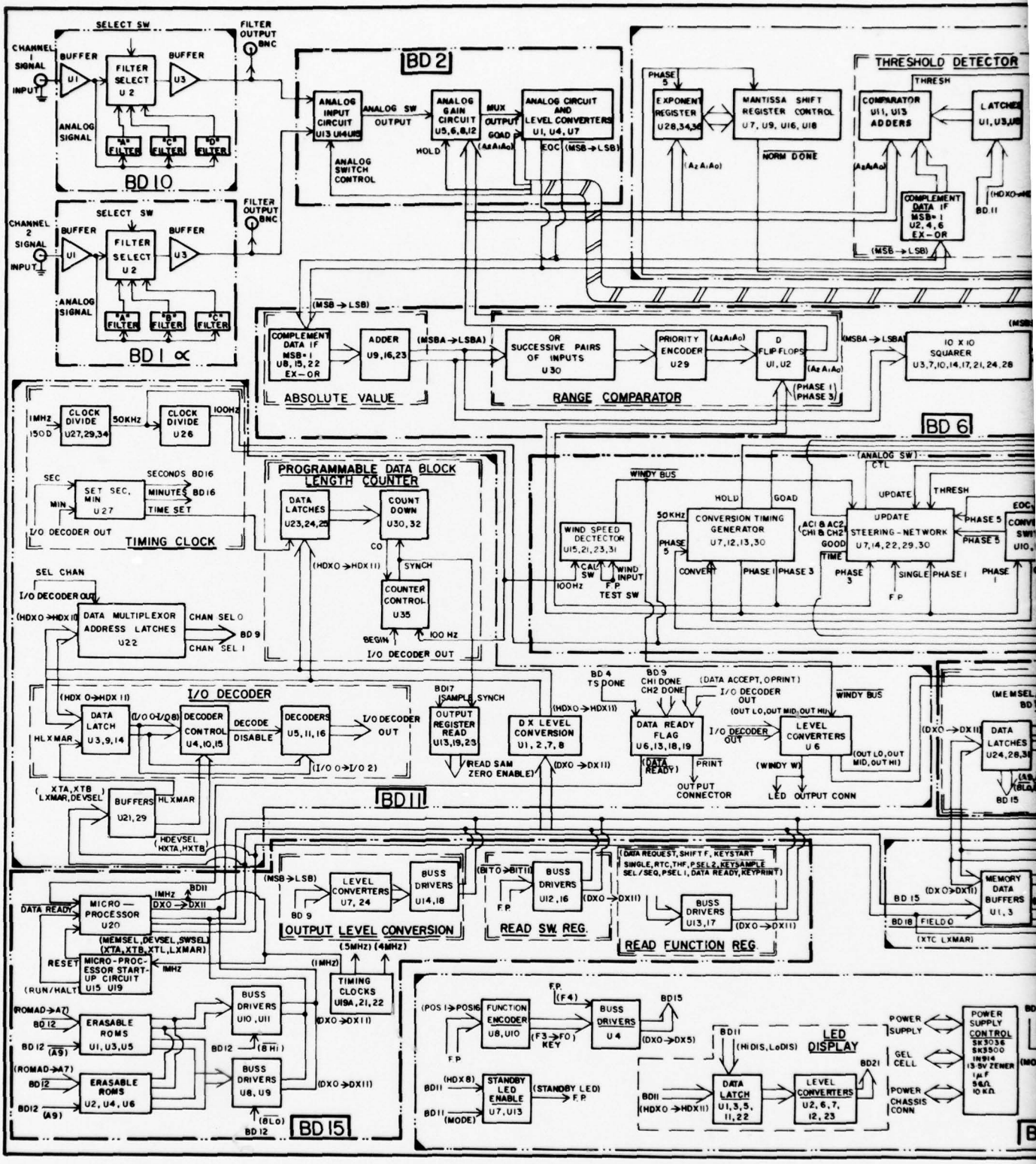
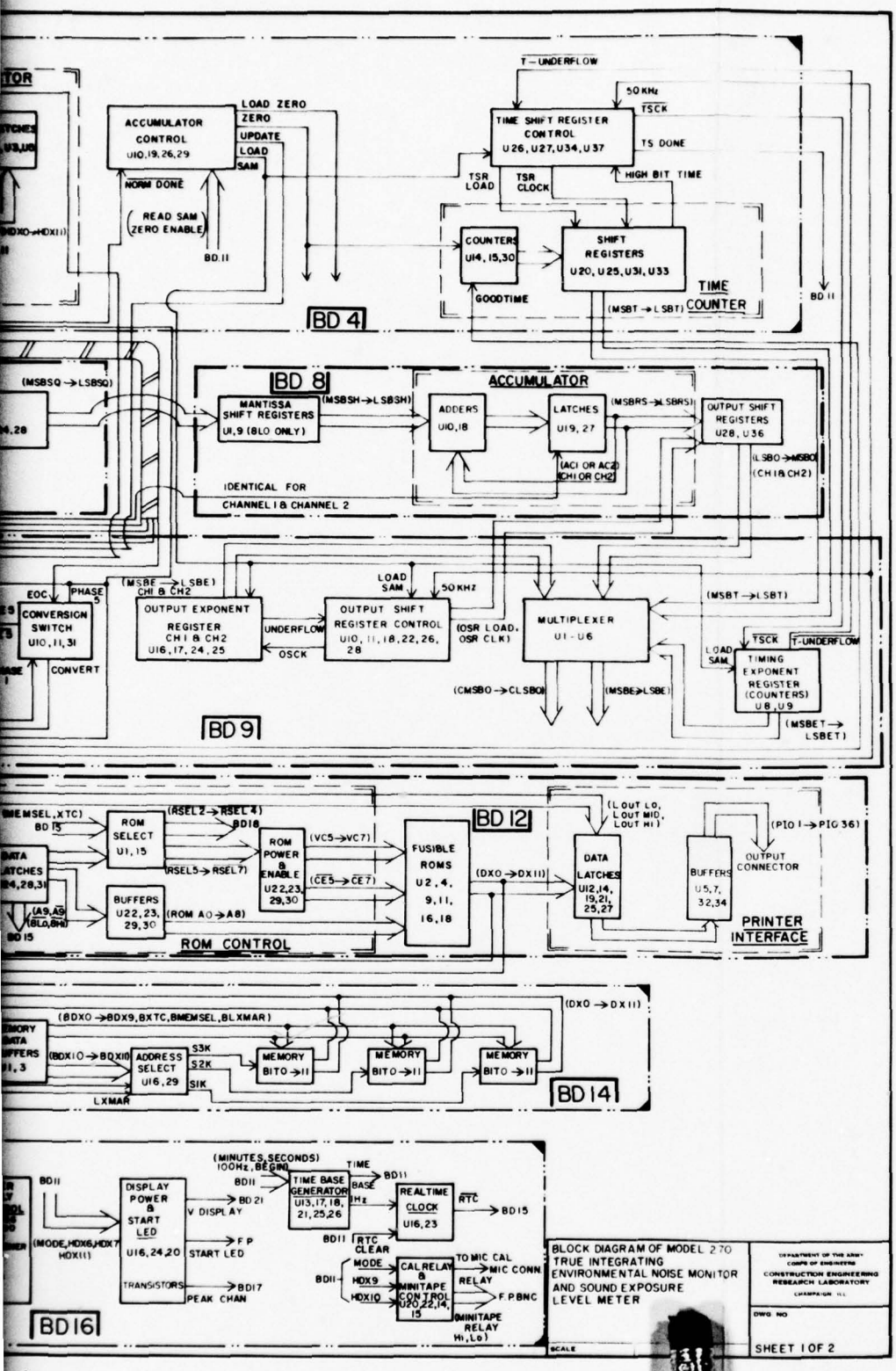


Figure 1. Block diagram of Model 270 true integrating environmental noise monitor and sound exposure level meter.


T-UNDERFLOW
50 KHz
TSCK
TS DONE
HIGH BIT TIME
TSR LOAD
TSR CLOCK
TIME SHIFT REGISTER CONTROL U26, U27, U34, U37
ACCUMULATOR CONTROL U10, 19, 26, 29
LOAD ZERO
ZERO
UPDATE
LOAD SAM
NORM DONE
READ SAM (ZERO ENABLE)
BD 11
COUNTERS U14, 15, 30
SHIFT REGISTERS U20, U25, U31, U33
GOODTIME
(MSBT → LSBT)
TIME COUNTER
BD 4
BD 8
ACCUMULATOR
MANTISSA SHIFT REGISTERS U1, 9 (8LO ONLY)
(MSBSH → LSBSH)
ADDERS U10, 18
LATCHES U19, 27
(MSBRS → LSBRS)
OUTPUT SHIFT REGISTERS U28, U36
(ACI OR ACZ) (CHI OR CH2)
(LSBO → MSBO) (CH1 & CH2)
IDENTICAL FOR CHANNEL 1 & CHANNEL 2
(MSBSQ → LSBSQ)
EOC
PHASE S
CONVERSION SWITCH U10, 11, 31
CONVERT
(MSBE → LSBE) CH1 & CH2
OUTPUT EXPONENT REGISTER CH1 & CH2 U16, 17, 24, 25
UNDERFLOW
OSCK
LOAD SAM
50 KHz
OUTPUT SHIFT REGISTER CONTROL U10, 11, 18, 22, 26, 28
(OSR LOAD, OSR CLK)
MULTIPLEXER U1 - U6
(MSBT → LSBT)
TSCK
T-UNDERFLOW
LOAD SAM
TIMING EXPONENT REGISTER (COUNTERS) U8, U9
(MSBET → LSBET)
(CMSBO → CLSBO)
(MSBE → LSBE)
BD 9
(BMEMSEL, XTC)
BD 15
ROM SELECT U1, 15
(RSEL2 → RSEL4)
BD 18
(RSEL5 → RSEL7)
ROM POWER & ENABLE U22, 23, 29, 30
(VC5 → VC7)
(CE5 → CE7)
BUFFERS U22, 23, 29, 30
(A9, A8) (BLO, BHI)
(ROM A0 → A8)
ROM CONTROL
FUSIBLE ROMS U2, 4, 9, 11, 16, 18
BD 12
(DX0 → DX11)
(L OUT LO, L OUT MID, L OUT HI)
DATA LATCHES U12, 14, 19, 21, 25, 27
BUFFERS U5, 7, 32, 34
(PIO 1 → PIO 36)
OUTPUT CONNECTOR
PRINTER INTERFACE
(BDX0 → BDX9, BXTC, BMEMSEL, BLXMAR)
(BDX10 → BDX10)
ADDRESS SELECT U16, 29
S3K
S2K
S1K
LXMAR
MEMORY BIT 0 → 11
BD 14
(MINUTES, SECONDS) 100Hz, BEGIN
TIME BASE GENERATOR U13, 17, 18, 21, 25, 26
TIME BASE 1Hz
REALTIME CLOCK U16, 23
RTC
RTC CLEAR
DISPLAY POWER & START LED U16, 24, 20
V DISPLAY
START LED
TRANSISTORS
PEAK CHAN
(MODE, HDX6, HDX7 HDX11)
MODE
HDX9
HDX10
CAL RELAY & MINITAPE CONTROL U20, 22, 14, 15
TO MIC CAL RELAY
MIC CONN
F.P. BNC
MINITAPE RELAY (Hi, Lo)
BD 16
BLOCK DIAGRAM OF MODEL 270 TRUE INTEGRATING ENVIRONMENTAL NOISE MONITOR AND SOUND EXPOSURE LEVEL METER
DEPARTMENT OF THE ARMY CORPS OF ENGINEERS CONSTRUCTION ENGINEERING RESEARCH LABORATORY CHAMPAIGN, ILL.
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SHEET 1 OF 2

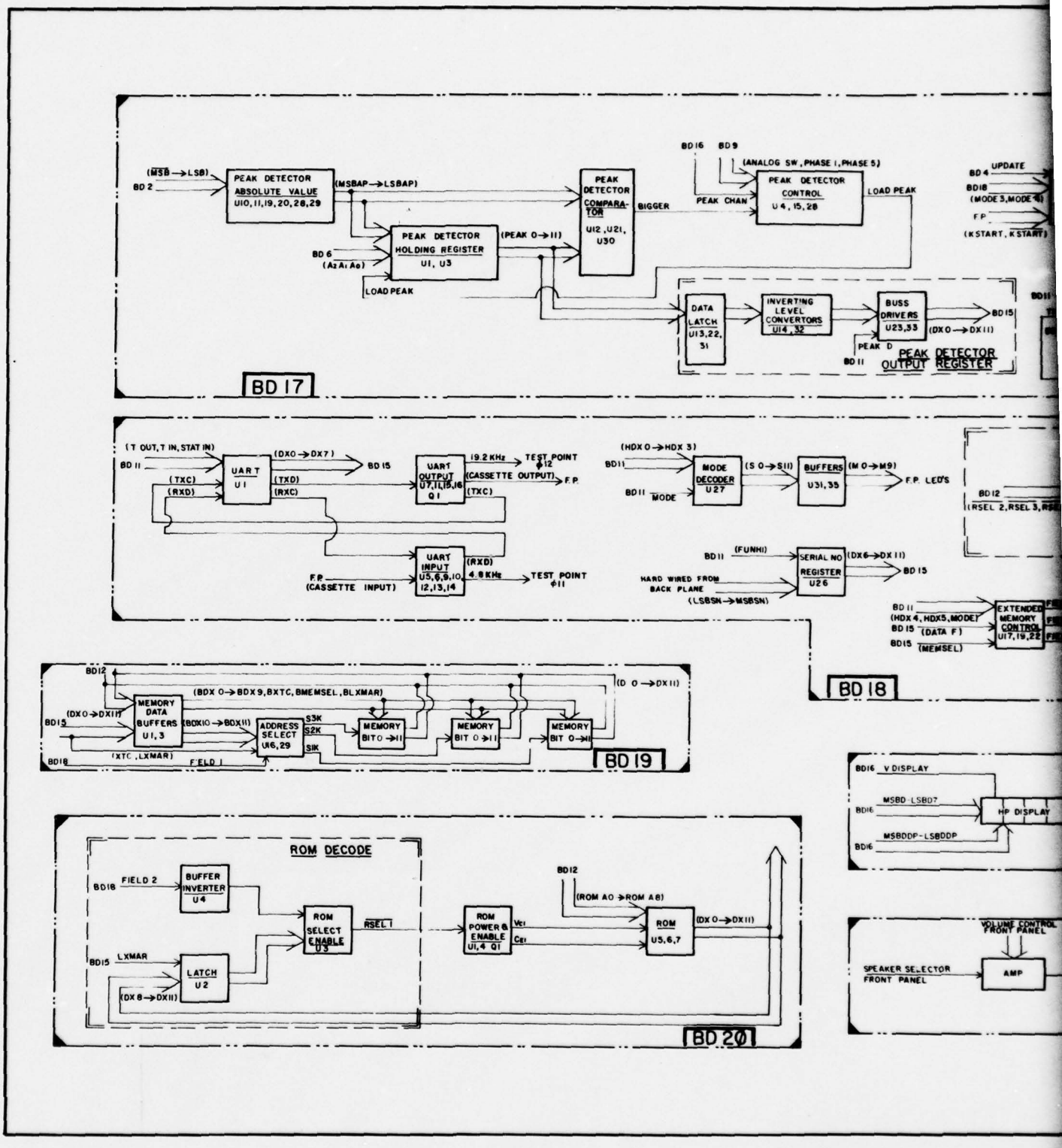
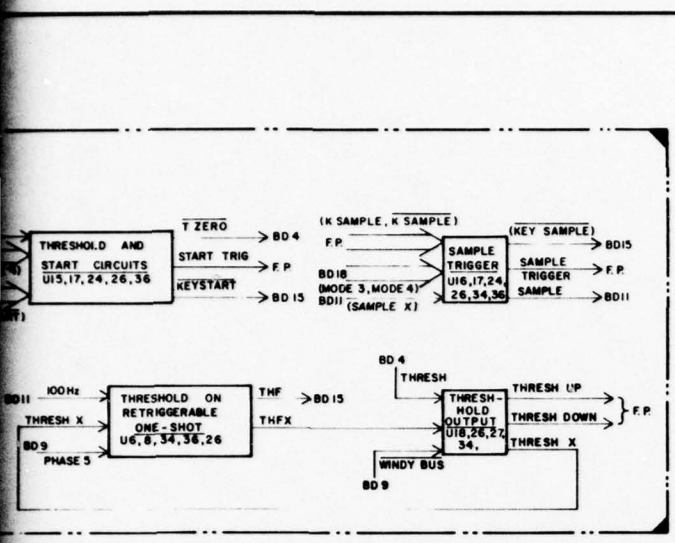
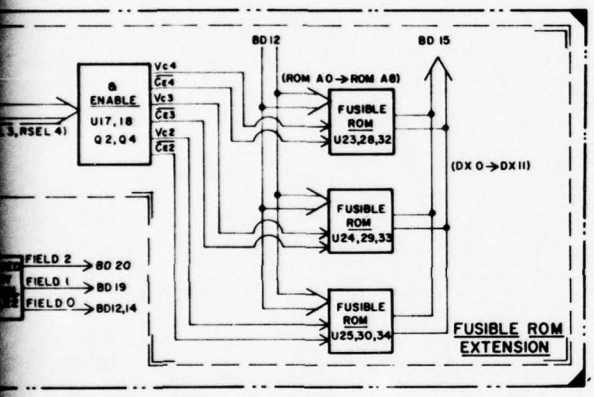


Figure 1. (cont'd).









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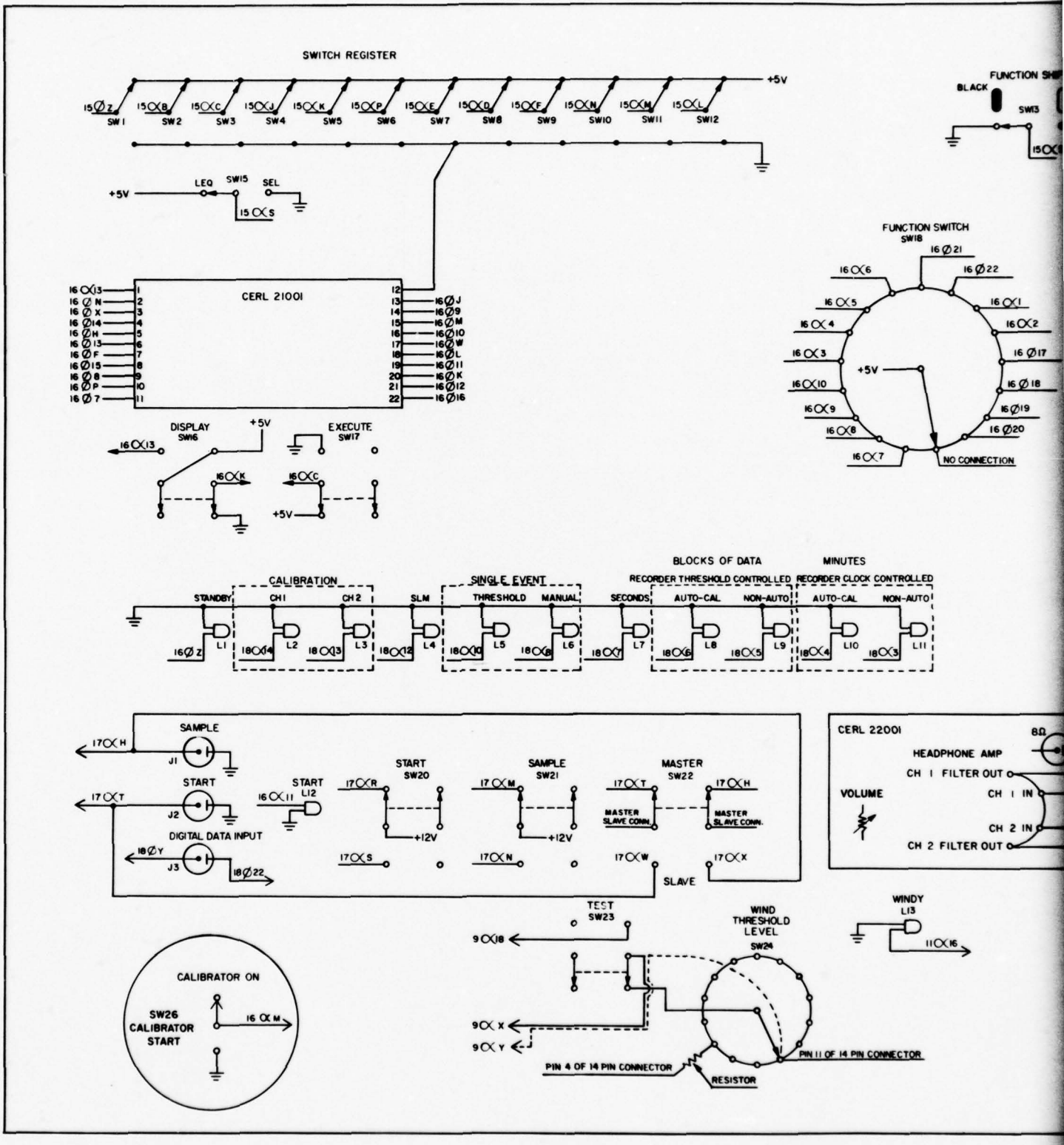
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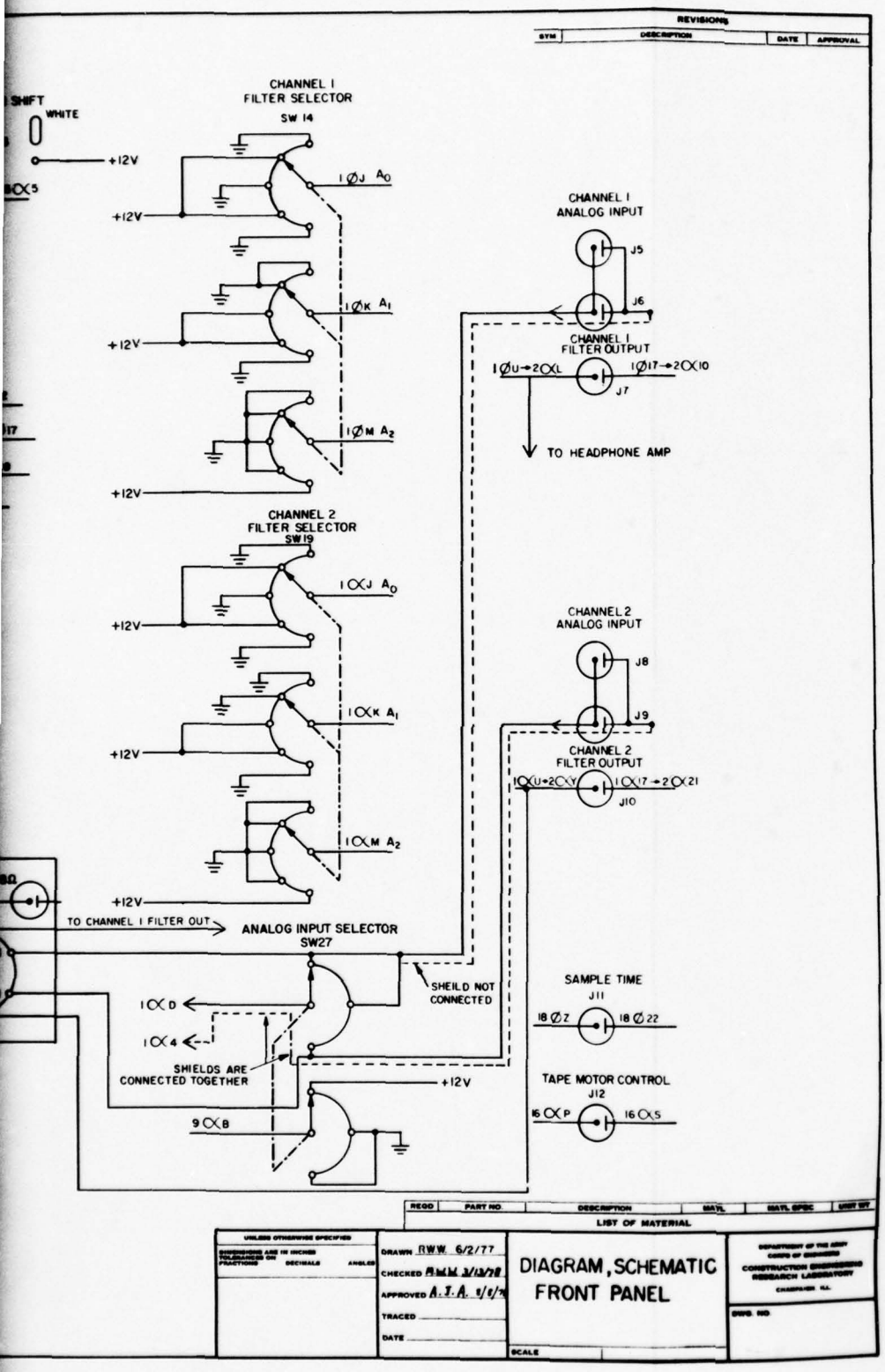
3 FRONT PANEL -- PARTS LIST AND SCHEMATIC

Table 1

Front Panel -- Parts List

Diagram Reference	Part Type and Manufacturer Number
SW1-SW13, SW15	SPDT switch ALCO MTE-106D
SW14, SW19, SW27	3 pole 2-5 pos non-shorting rotary switch CENTRALAB PSA-207
SW16, SW17, SW20, SW21, SW23	DPDT spring-loaded switch ALCO MTE-206R
SW18, SW24, SW26	non-shorting 2-17 pos rotary switch Mallory 32117J
SW22	DPDT switch ALCO MTE-206N
L1	yellow led Monsanto MV5352
L2-L13	red led Monsanto MV5752
J1, J2, J11	non-insulated BNC connector Amphenol 74868 UG-1094/U
J3, J5-J10	insulated BNC connector Amphenol 31-10
J12	Viking THORKOM TFR09-101P
CERL 21001	PC Board No. 21001 display
CERL 22001	PC Board No. 22001 headphone amp
R1	100 K potentiometer


SWITCH REGISTER
+5V
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
LEQ
SW15
SEL
CERL 21001
FUNCTION SWITCH
SW18
DISPLAY
SW16
EXECUTE
SW17
CALIBRATION
STANDBY
CH1
CH2
SLM
SINGLE EVENT
THRESHOLD
MANUAL
BLOCKS OF DATA
RECORDER THRESHOLD CONTROLLED
SECONDS
AUTO-CAL
NON-AUTO
MINUTES
RECORDER CLOCK CONTROLLED
SAMPLE
START
DIGITAL DATA INPUT
START SW20
SAMPLE SW21
MASTER SW22
MASTER SLAVE CONN.
SLAVE
CERL 22001
HEADPHONE AMP
VOLUME
CH 1 FILTER OUT
CH 1 IN
CH 2 IN
CH 2 FILTER OUT
TEST SW23
WIND THRESHOLD LEVEL SW24
WINDY L13
CALIBRATOR ON
SW26 CALIBRATOR START
PIN 4 OF 14 PIN CONNECTOR
PIN 11 OF 14 PIN CONNECTOR
RESISTOR
NO CONNECTION


REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
CHANNEL 1
FILTER SELECTOR
SW 14
WHITE
+12V
1ØJ A0
1ØK A1
1ØM A2
CHANNEL 1
ANALOG INPUT
J5
J6
CHANNEL 1
FILTER OUTPUT
1ØU→2ØL
1Ø17→2Ø10
J7
TO HEADPHONE AMP
CHANNEL 2
FILTER SELECTOR
SW19
1ØJ A0
1ØK A1
1ØM A2
CHANNEL 2
ANALOG INPUT
J8
J9
CHANNEL 2
FILTER OUTPUT
1ØU→2ØY
1Ø17→2Ø21
J10
TO CHANNEL 1 FILTER OUT
ANALOG INPUT SELECTOR
SW27
SHEILD NOT
CONNECTED
1Ø D
1Ø 4
SHIELDS ARE
CONNECTED TOGETHER
9Ø8
SAMPLE TIME
J11
18Ø7
18Ø22
TAPE MOTOR CONTROL
J12
16ØP
16Ø5
REQD
PART NO
DESCRIPTION
MATL
MATL SPEC
UNIT QTY
LIST OF MATERIAL
DRAWN RWW 6/2/77
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SCALE
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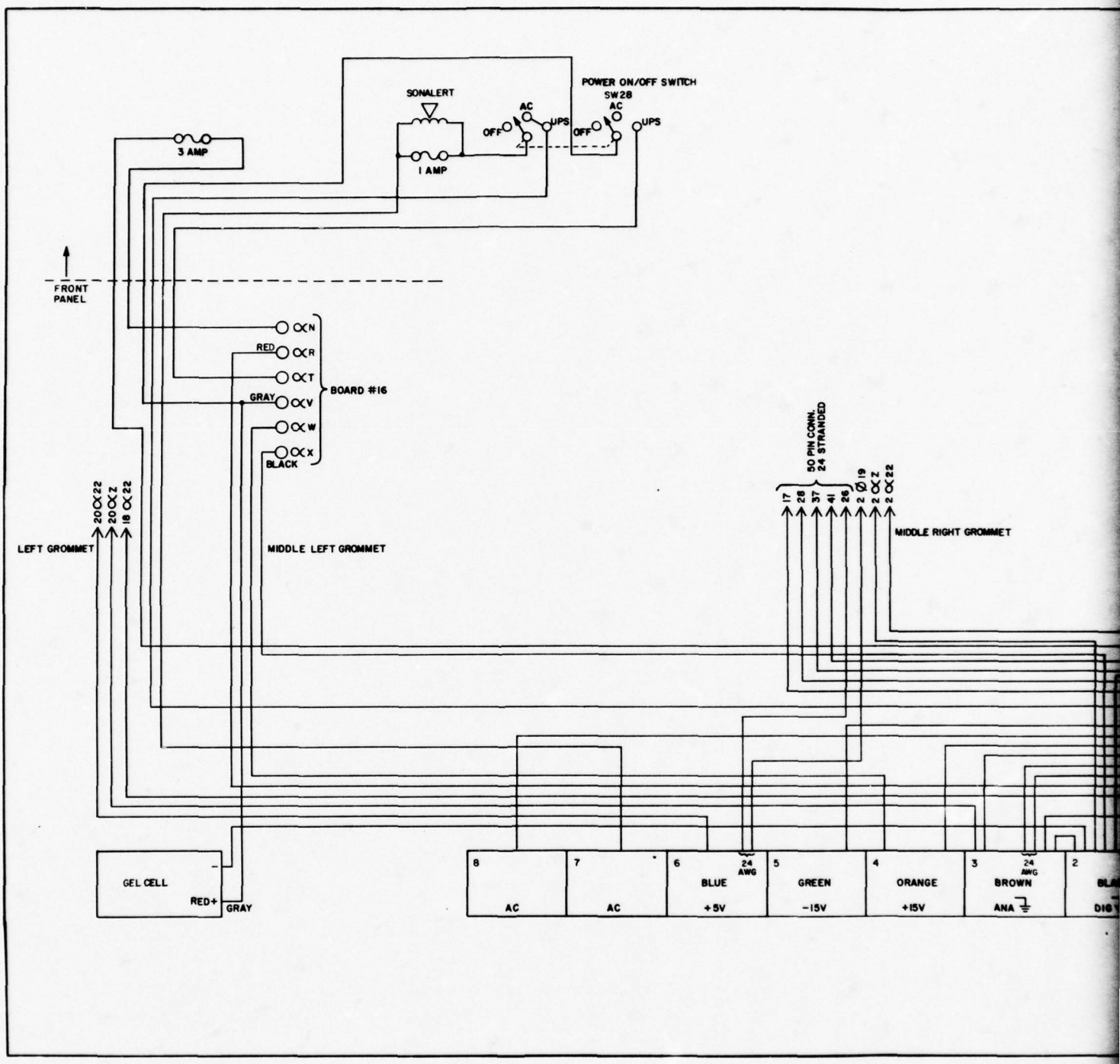
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4 POWER SUPPLY CIRCUIT--PARTS LIST AND SCHEMATIC

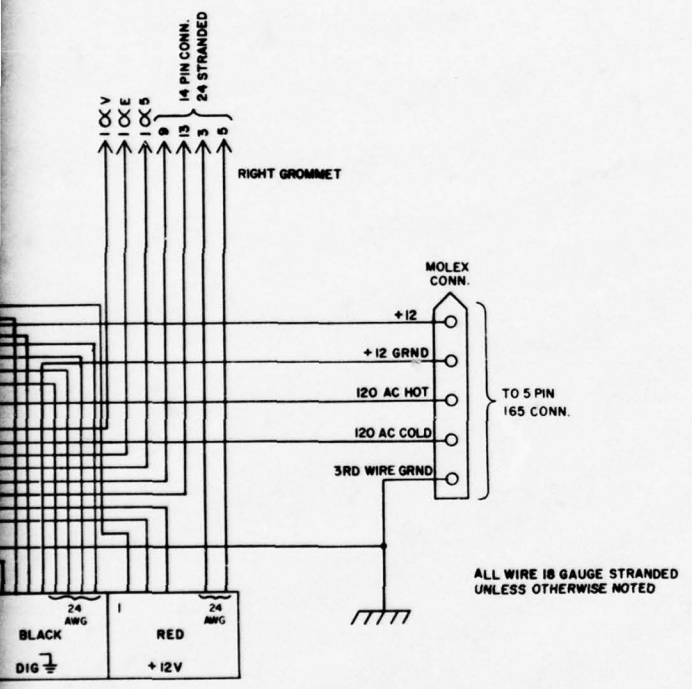
Table 2

Power Supply Circuit -- Parts List

Part Description	Part Number
Fuse holders--waterproof 20/A 250 V max	Littlefuse FHN 20G
1-amp fuse 125 V SLO-BLO	
3-amp fuse 125 V	
SW28 - 3 pol 2-5 pos non-shorting rotary switch	CENTRALAB PSA-207
Sonalert Electronic Signal 110-VAC pulsing 2900 Hz	Mallory SC110P
Rechargeable battery 12-V 5.0/AH lead acid	Gates 0800-0016
Uninterruptible power supply system	Semiconductor Circuits UPS12-2T3


SONALERT
POWER ON/OFF SWITCH
SW28
AC
OFF
UPS
3 AMP
1 AMP
FRONT PANEL
RED
GRAY
BLACK
BOARD #16
50 PIN CONN. 24 STRANDED
LEFT GROMMET
MIDDLE LEFT GROMMET
MIDDLE RIGHT GROMMET
GEL CELL
RED+
GRAY
AC
AC
BLUE
+5V
GREEN
-15V
ORANGE
+15V
BROWN
ANA
24 AWG

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



ITEM	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT QT

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED

DRAWN RWW 5/20/77

CHECKED [illegible] 5/23/78

APPROVED A.J.A. 5/16/78

TRACED

DATE

DIAGRAM, SCHEMATIC POWER SUPPLY WIRING

SCALE

DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

DWG. NO.

2

5 MONITOR BACK PLANE WIRING LIST

Each PC board in the monitor is divided into two halves, labeled "α" and "ϕ". Each half has 22 output pins on each side. One side's outputs are numbered 1 through 22; the others are labeled with 22 letters. Similarly, the back plane of the monitor chassis is divided into two halves, also labeled "α" and "ϕ". Therefore, the back plane consists of two rows of 44 pin connectors.

The wiring list shows the connections to be made between these 44 pin connectors. Some connections also have to be made to the power supply (PS), to the front panel (FP), and to the various chassis connectors. For more details on the connections to the power supply, front panel, and connectors, see the corresponding diagrams and lists.

To facilitate the wiring of the back plane, several busses were wired from the power supply. When a particular pin is to be wired to a buss, the name of the signal is given and the buss is designated by a dagger. The various busses are listed below in Table 3.

In the wiring list, an asterisk in the origin column means that the pin in question is the origin of that signal. The double dagger indicates that Board 8 has many signal pins which must be connected to ground.

Table 3

Wiring List for Power Supply Busses

Digital Ground

PS pin 2 → 2φA → ··· all boards φA ··· → 21 φA → PS
PS pin 2 → 2αZ → ··· all boards αZ ··· → 21 αZ → PS

+12 V

PS pin 1 → 2φ1 → 4φ1 → 6φ1 → 8Lo1φ1 → 8Hi1φ1 →
PS pin 1 → 2α22→ 4α22→ 6α22→ 8Lo1α22→ 8Hi1α22→

→ 8Lo2φ1 → 8Hi2φ1 → 9φ1 → 11φ1 → 16φ1 → 17φ1 → 18φ1 → PS
→ 8Lo2α22→ 8Hi2α22→ 9α22→ 11α22→ 16α22→ 17α22→ 18α22 → PS

+5 V

PS pin 6 → 2φ19 → 11φB → 12φ1 → 14φ1 → 15φ1 → 16φ2 → 17φ2 →
2φ19 → 11αY → 12α22→ 14α22→ 15α22→ 16α21→ 17α21→

→ 18φ2 → 19φ1 → 20φ1→ 21φ1 →
→ 18α21→ 19α22→ 20α22→21α22 →

Analog ground

PS pin 3 → 1α5 → 1φ5
1α5 → 2φZ

+15 V

PS pin 4 → 1αE → 1φE → 2φX

-15 V

PS pin 5 → 1αV → 1φV → 2φY

Board No. 2, Side ϕ

Pin	Signal Name	Origin	
1	+12	PS	†
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19	+5	PS	†
20			
21			
22			

Board No. 2, Side ϕ

Pin	Signal Name	Origin	
A	Digital Ground	PS	†
B	$\overline{\text{EOC}}$	*	9α20
C	$\overline{\text{MSB}}$	*	4ϕ19, 6ϕR, 17ϕC
D	MSB-1	*	4ϕZ, 6ϕN, 17ϕD
E	MSB-4	*	4ϕP, 6ϕC, 17ϕH
F	MSB-3	*	4ϕN, 6ϕB, 17ϕF
H	MSB-2	*	4ϕM, 6ϕM, 17ϕE
J	LSB+2	*	4ϕ4, 6ϕD, 17ϕL
K	LSB+3	*	4ϕ3, 6ϕK, 17ϕK
L	LSB+4	*	4ϕR, 6ϕL, 17ϕJ
M	LSB+1	*	4ϕ5, 6ϕE, 17ϕM
N	LSB	*	4ϕ6, 6ϕH, 17ϕN
P			
R			
S			
T	GOAD	9αM	
U			
V			
W			
X	+15 V	PS	1αE, 1ϕE
Y	-15 V	PS	1αV, 1ϕV
Z	Analog Ground	PS	1α5, 1ϕ5

Board No. 2, Side α

Pin	Signal Name	Origin
1		
2		
3		
4		
5		
6		
7		
8		
9		
10	Chan 1 input GND	1ϕ17
11		
12		
13		
14		
15		
16	Ch 1 filter bd GND	1ϕ11
17	Ch 2 filter bd GND	1α11
18		
19		
20		
21	Ch 2 input GND	1α17
22	+12V	PS †

Board No. 2, Side α

Pin	Signal Name	Origin	
A	A_2	6ϕF	4ϕX, 4αR, 17ϕ5
B	A_1	6ϕJ	4ϕY, 4αY, 17ϕ4
C	A_o	6ϕP	4ϕ20, 4αX, 17ϕ3
D			
E			
F			
H			
J	HOLD	9αP	
K	ANALOG SWITCH CONTROL	9α9	17ϕR
L	Ch 1 input (analog)	1ϕU	
M			
N			
P			
R			
S			
T			
U			
V			
W			
X			
Y	Ch 2 input (analog)	1αU	
Z	Digital Ground	PS	†

Board No. 4, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS †	
2			
3	LSB +3	2ϕK	6ϕK, 17ϕK
4	LSB +2	2ϕJ	6ϕD, 17ϕL
5	LSB +1	2ϕM	6ϕE, 17ϕM
6	LSB	2ϕN	6ϕH, 17ϕN
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19	$\overline{\text{MSB}}$	2ϕC	6ϕR, 17ϕC
20	A_0	6ϕP	4αX, 2αC, 17ϕ3
21	THRESH	*	9αU, 17αJ
22	HIGH BIT TIME	*	

Board No. 4, Side ϕ

Pin	Signal Name	Origin	
A	Digital Ground	PS †	
B	GOOD TIME	9αT	
C	HDX0	11ϕH	16αL, 18α16
D	HDX1	11ϕJ	16ϕ4, 18α17
E	HDX2	11ϕK	16ϕ6, 18α18
F	HDX3	11ϕL	16ϕ5, 18α19
H	HDX4	11ϕM	16ϕC, 18αK
J	HDX5	11ϕN	16ϕB, 18αJ
K	HDX6	11ϕP	16ϕD
L	HDX7	11ϕR	16ϕE
M	MSB-2	2ϕH	6ϕM, 17ϕE
N	MSB-3	2ϕF	6ϕB, 17ϕF
P	MSB-4	2ϕE	6ϕC, 17ϕH
R	LSB+4	2ϕL	6ϕL, 17ϕJ
S	THSET	11α1	
T	HDX8	11ϕS	16ϕT
U	HDX9	11ϕT	16ϕS
V	HDX10	11ϕU	16ϕV
W	HDX11	11ϕV	16ϕU
X	A_2	6ϕF	4αR, 2αA, 17ϕ5
Y	A_1	6ϕJ	4αY, 2αB, 17ϕ4
Z	MSB-1	2ϕD	6ϕN, 17ϕD

Board No. 4, Side α

Pin	Signal Name	Origin	
1	MSBT	*	9φV
2	MSBT-1	*	9φM
3	MSBT-2	*	9φZ
4	LSBT+2	*	9φ14
5			
6	$\overline{\text{TZERO}}$	17αD	
7			
8			
9			
10	T-UNDERFLOW	9φD	
11			
12			
13			
14			
15	$\overline{\text{TSCK}}$	*	9φ6
16			
17	SR LOAD	*	8Lo1φ4, 8Lo2φ4
18	UPDATE	*	9αN, 17αA
19	$\overline{\text{NORM DONE}}$	*	
20	READ SAM	11αL	
21	ZERO	*	8Lo1α20, 8Hi1α20, 8Hi2α20, 8Lo2α20, 17φU
22	+12	PS	†

Board No. 4, Side α

Pin	Signal Name	Origin	
A	LSBT+1	*	9αL
B	LSBT	*	9αC
C	LSBT-1	*	
D	50 kHz	11α11	9α10
E			
F	$\overline{\text{Norm Clock}}$	*	
H	1.8 MHz	*	
J	SR CLK	*	8Lo1φ5, 8Lo2φ5
K	TSR LOAD	*	
L	NORM REQ	*	
M	TSR CLOCK	*	
N	$\overline{\text{TS DONE}}$	*	11α13
P	$\overline{\text{CARRY OUT}}$	*	
R	A_2	6φF	4φX, 2αA, 17φ5
S	NORM DONE	*	
T	PHASE 5	9αR	17φT
U	LOAD ZERO	*	
V	ZERO ENABLE	11α20	
W	LOAD SAM	*	9φB
X	A_0	6φP	4φ20, 2αC, 17φ3
Y	A_1	6φJ	4φY, 2αB, 17φ4
Z	Digital ground	PS	†

Board No. 6, Side ϕ

Pin	Signal Name	Origin
1	+12	PS †
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		

Board No. 6, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	MSB-3	2ϕF	4ϕN, 17ϕF
C	MSB-4	2ϕE	4ϕP, 17ϕH
D	LSB+2	2ϕJ	4ϕ4, 17ϕL
E	LSB+1	2ϕM	4ϕ5, 17ϕM
F	A_2	*	4ϕX, 4αR, 2αA, 17ϕ5
H	LSB	2ϕN	4ϕ6, 17ϕN
J	A_1	*	4ϕY, 4αY, 2αB, 17ϕ4
K	LSB+3	2ϕK	4ϕ3, 17ϕK
L	LSB+4	2ϕL	4ϕR, 17ϕJ
M	MSB-2	4ϕH	4ϕM, 17ϕE
N	MSB-1	2ϕD	4ϕZ, 17ϕD
P	$\overline{A_0}$	*	4ϕ20, 4αX, 2αC, 17ϕ3
R	$\overline{MSB}$	2ϕC	4ϕ19, 17ϕC
S			
T	PHASE 1	9ϕ10	17ϕS
U	PHASE 3	9α1	
V			
W			
X			
Y			
Z			

Board No. 6, Side α

Pin	Signal Name	Origin	
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22	+12	PS	†

Board No. 6, Side α

Pin	Signal Name	Origin	
A			
B	MSBSQ+2	*	8Lo1αD, 8Lo2αD
C	MSBSQ+1	*	8Lo1αC, 8Lo2αC
D	MSBSQ	*	8Lo1αB, 8Lo2αB
E	MSBSQ-1	*	8Lo1φY, 8Lo2φY
F	MSBSQ-2	*	8Lo1φX, 8Lo2φX
H	MSBSQ-3	*	8Lo1φW, 8Lo2φW
J	MSBSQ-4	*	8Lo1φV, 8Lo2φV
K	MSBSQ-5	*	8Lo1φU, 8Lo2φU
L	MSBSQ-6	*	8Lo1φT, 8Lo2φT
M	MSBSQ-7	*	8Lo1φS, 8Lo2φS
N	MSBSQ-8	*	8Lo1φR, 8Lo2φR
P	LSBSQ+8	*	8Lo1φP, 8Lo2φP
R	LSBSQ+7	*	8Lo1φN, 8Lo2φN
S	LSBSQ+6	*	8Lo1φM, 8Lo2φM
T	LSBSQ+5	*	8Lo1φL, 8Lo2φL
U	LSBSQ+4	*	8Lo1φK, 8Lo2φK
V	LSBSQ+3	*	8Lo1φH, 8Lo2φH
W	LSBSQ+2	*	8Lo1φF, 8Lo2φF
X	LSBSQ+1	*	8Lo1φE, 8Lo2φE
Y	LSBSQ	*	8Lo1φD, 8Lo2φD
Z	Digital ground	PS	†

Board No. 8 Lol, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS	†
2	OSR CARRY IN	PS	††
3	SR CARRY IN	PS	††
4	SR LOAD	4α17	8Lo2ϕ4
5	SR CLK	4αJ	8Lo2ϕ5
6	OSR-4	*	
7	OSR-3	*	
8	OSR-2	*	
9	OSR-1	*	
10	OSR-8	*	
11	OSR-7	*	
12	OSR-6	*	
13	OSR-5	*	
14	OSR-12	*	
15	OSR-11	*	
16	OSR-10	*	
17	OSR-9	*	
18	OSR-16	*	
19	OSR-15	*	
20	OSR-14	*	
21	OSR-13	*	
22	OSR-20	*	

Board No. 8 Lol, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	OSR LOAD	9ϕ11	8Hi2ϕB, 8HilϕB, 8Lo2ϕB, 17ϕ18
C	OSR CLOCK Ch1	9ϕ12	8HilϕC
D	LSBSQ	6αY	8Lo2ϕD
E	LSBSQ+1	6αX	8Lo2ϕE
F	LSBSQ+2	6αW	8Lo2ϕF
H	LSBSQ+3	6αV	8Lo2ϕH
J	ADDER CARRY IN	PS	††
K	LSBSQ+4	6αU	8Lo2ϕK
L	LSBSQ+5	6αT	8Lo2ϕL
M	LSBSQ+6	6αS	8Lo2ϕM
N	LSBSQ+7	6αR	8Lo2ϕN
P	LSBSQ+8	6αP	8Lo2ϕP
R	MSBSQ-8	6αN	8Lo2ϕR
S	MSBSQ-7	6αM	8Lo2ϕS
T	MSBSQ-6	6αL	8Lo2ϕT
U	MSBSQ-5	6αK	8Lo2ϕU
V	MSBSQ-4	6αJ	8Lo2ϕV
W	MSBSQ-3	6αH	8Lo2ϕW
X	MSBSQ-2	6αF	8Lo2ϕX
Y	MSBSQ-1	6αE	8Lo2ϕY
Z			

Board No. 8 Lol, Side α

Pin	Signal Name	Origin	
1	OSR-19	*	
2	OSR-18	*	
3	OSR-17	*	
4	OSR-24	*	
5	OSR-23	*	
6	OSR-22	*	
7	OSR-21	*	
8	OSR-28	*	
9	OSR-27	*	
10	OSR-26	*	
11	OSR-25	*	
12	OSR-32	*	
13	OSR-31	*	
14	OSR-30	*	
15	OSR-29	*	
16	OSR-36 (OSR CARRY OUT)	*	8 Hilφ2
17	OSR-35	*	
18	OSR-34	*	
19	OSR-33	*	
20	ZERO	4α21	8 Hilα20, 8 Hi2α20, 8 Lo2α20, 17φU
21	AC1 (UPDATE)	9α12	8 Hilα21
22	+12 V	PS	†

Board No. 8 Lol, Side α

Pin	Signal Name	Origin	
A			
B	MSBSQ	6αD	8 Lo2αB
C	MSBSQ+1	6αC	8 Lo2αC
D	MSBSQ+2	6αB	8 Lo2αD
E	MSBSQ+3	PS	††
F	MSBSQ+4	PS	††
H	MSBSQ+5	PS	††
J	MSBSQ+6	PS	††
K	MSBSQ+7	PS	††
L	MSBSQ+8	PS	††
M	MSBSQ+9	PS	††
N	MSBSQ+10	PS	††
P	MSBSQ+11	PS	††
R	MSBSQ+12	PS	††
S	MSBSQ+13	PS	††
T	MSBSQ+14	PS	††
U	MSBSQ+15	PS	††
V	MSBSQ+16	PS	††
W	MSBSQ+17	PS	††
X	MSBSQ+18	PS	††
Y	ADDER CARRY OUT	*	8 HilφJ
Z	Digital ground	PS	†

Board No. 8 Hil, Side ϕ

Pin	Signal Name	Origin
1	+12 V	PS †
2	OSR-36	8Lolα16
3		
4		
5		
6	OSR-40	*
7	OSR-39	*
8	OSR-38	*
9	OSR-37	*
10	OSR-44	*
11	OSR-43	*
12	OSR-42	*
13	OSR-41	*
14	OSR-48	*
15	OSR-47	*
16	OSR-46	*
17	OSR-45	*
18	OSR-52	*
19	OSR-51	*
20	OSR-50	*
21	OSR-49	*
22	OSR-56	*

Board No. 8 Hil, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	OSR LOAD	9ϕ11	8 Hi2ϕB, 8 Lo2ϕB, 8 Lo1ϕB, 17ϕ18
C	OSR CLOCK Ch 1	9ϕ12	8 Lo1ϕC
D			
E			
F			
H			
J	ADDER CARRY OUT	8Lo1αY	
K			
L			
M			
N			
P			
R			
S			
T			
U			
V			
W			
X			
Y			
Z			

Board No. 8 Hil, Side α

Pin	Signal Name	Origin	
1	OSR-55	*	
2	OSR-54	*	
3	OSR-53	*	
4	OSR-60	*	
5	OSR-59	*	
6	OSR-58	*	
7	OSR-57	*	
8	OSR-64	*	
9	OSR-63	*	
10	OSR-62	*	
11	OSR-61	*	
12	LSBO+2 Ch 1	*	9φ16
13	LSBO+1 Ch 1	*	9αJ
14	LSBO Ch 1	*	9αE
15	OSR-65	*	
16	HIGH BIT Ch 1	*	9αA
17	MSBO Ch 1	*	9φT
18	MSBO-1 Ch 1	*	9φP
19	MSBO-2 Ch 1	*	9φX
20	ZERO	4α21	8 Lolα20, 8 Hi2α20, 8 Lo2α20, 17φU
21	AC 1 (UPDATE)	9α12	8 Lolα21
22	+12 V	PS	†

Board No. 8 Hil, Side α

Pin	Signal Name	Origin
A		
B		
C		
D		
F		
H		
H		
J		
K		
L		
M		
N		
P		
R		
S		
T		
U		
V		
W		
X		
Y	ADDER OVERFLOW	*
Z	Digital ground	PS †

Board No. 8 Lo2, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS	†
2	CARRY IN	PS	††
3	CARRY IN	PS	††
4	SR LOAD	4α17	8 Lolϕ4
5	SR CLK	4αJ	8 Lolϕ5
6	OSR-4	*	
7	OSR-3	*	
8	OSR-2	*	
9	OSR-1	*	
10	OSR-8	*	
11	OSR-7	*	
12	OSR-6	*	
13	OSR-5	*	
14	OSR-12	*	
15	OSR-11	*	
16	OSR-10	*	
17	OSR-9	*	
18	OSR-16	*	
19	OSR-15	*	
20	OSR-14	*	
21	OSR-13	*	
22	OSR-20	*	

Board No. 8 Lo2, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	OSR LOAD	9ϕ11	8Hi2ϕB, 8Hi1ϕB, 8Lo1ϕB, 17ϕ18
C	OSR CLOCK Ch 2	9ϕ13	8Hi2ϕC
D	LSBSQ	6αY	8Lo1ϕD
E	LSBSQ+1	6αX	8Lo1ϕE
F	LSBSQ+2	6αW	8Lo1ϕF
H	LSBSQ+3	6αV	8Lo1ϕH
J	ADDER CARRY IN	PS	††
K	LSBSQ+4	6αU	8Lo1ϕK
L	LSBSQ+5	6αT	8Lo1ϕL
M	LSBSQ+6	6αS	8Lo1ϕM
N	LSBSQ+7	6αR	8Lo1ϕN
P	LSBSQ+8	6αP	8Lo1ϕP
R	MSBSQ-8	6αN	8Lo1ϕR
S	MSBSQ-7	6αM	8Lo1ϕS
T	MSBSQ-6	6αL	8Lo1ϕT
U	MSBSQ-5	6αK	8Lo1ϕU
V	MSBSQ-4	6αJ	8Lo1ϕV
W	MSBSQ-3	6αH	8Lo1ϕW
X	MSBSQ-2	6αF	8Lo1ϕX
Y	MSBSQ-1	6αE	8Lo1ϕY
Z			

Board No. 8 Lo2, Side α

Pin	Signal Name	Origin	
1	OSR-19	*	
2	OSR-18	*	
3	OSR-17	*	
4	OSR-24	*	
5	OSR-23	*	
6	OSR-22	*	
7	OSR-21	*	
8	OSR-28	*	
9	OSR-27	*	
10	OSR-26	*	
11	OSR-25	*	
12	OSR-32	*	
13	OSR-31	*	
14	OSR-30	*	
15	OSR-29	*	
16	OSR-36(OSR CARRY OUT)	*	8Hi2φ2
17	OSR-35	*	
18	OSR-34	*	
19	OSR-33	*	
20	ZERO	4α21	8Lolα20, 8Hilα20, 8Hi2α20, 17φU
21	AC2 (UPDATE)	9αS	8Hi2α21
22	+12 V	PS	†

Board No. 8 Lo2, Side α

Pin	Signal Name	Origin	
A			
B	MSBSQ	6αD	8Lolα B
C	MSBSQ+1	6αC	8Lolα C
D	MSBSQ+2	6αB	8Lolα D
E	MSBSQ+3	PS	††
F	MSBSQ+4	PS	††
H	MSBSQ+5	PS	††
J	MSBSQ+6	PS	††
K	MSBSQ+7	PS	††
L	MSBSQ+8	PS	††
M	MSBSQ+9	PS	††
N	MSBSQ+10	PS	††
P	MSBSQ+11	PS	††
R	MSBSQ+12	PS	††
S	MSBSQ+13	PS	††
T	MSBSQ+14	PS	††
U	MSBSQ+15	PS	††
V	MSBSQ+16	PS	††
W	MSBSQ+17	PS	††
X	MSBSQ+18	PS	††
Y	ADDER CARRY OUT	*	8Hi2φJ
Z	Digital ground	PS	†

Board No. 8 Hi2, Side ϕ

Pin	Signal Name	Origin
1	+12 V	PS †
2	OSR-36	8Lo2α16
3		
4		
5		
6	OSR-40	*
7	OSR-39	*
8	OSR-38	*
9	OSR-37	*
10	OSR-44	*
11	OSR-43	*
12	OSR-42	*
13	OSR-41	*
14	OSR-48	*
15	OSR-47	*
16	OSR-46	*
17	OSR-45	*
18	OSR-52	*
19	OSR-51	*
20	OSR-50	*
21	OSR-49	*
22	OSR-56	*

Board No. 8 Hi2, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	OSR LOAD	9ϕ11	8Lo2ϕB, 8Hi1ϕB, 8Lo1ϕB, 17ϕ18
C	OSR LOAD Ch 2	9ϕ13	8Lo2ϕC
D			
E			
F			
H			
J	ADDER CARRY OUT	8Lo2αY	
K			
L			
M			
N			
P			
R			
S			
T			
U			
V			
W			
X			
Y			
Z			

Board No. 8 Hi2, Side α

Pin	Signal Name	Origin	
1	OSR-55	*	
2	OSR-54	*	
3	OSR-53	*	
4	OSR-60	*	
5	OSR-59	*	
6	OSR-58	*	
7	OSR-57	*	
8	OSR-64	*	
9	OSR-63	*	
10	OSR-62	*	
11	OSR-61	*	
12	LSBO+2 Ch 2	*	9φ15
13	LSBO+1 Ch 2	*	9αK
14	LSBO	*	9αD
15	OSR-65	*	
16	HIGH BIT Ch 2	*	9α2
17	MSBO Ch 2	*	9φU
18	MSBO-1 Ch 2	*	9φN
19	MSBO-2 Ch 2	*	9φY
20	ZERO	4α21	8Lo1α20, 8Hi1α20, 8Lo2α20, 17φU
21	AC2 (UPDATE)	9αS	8Lo2α21
22	+12 V	PS	†

Board No. 8 Hi2, Side α

Pin	Signal Name	Origin
A		
B		
C		
D		
E		
F		
H		
J		
K		
L		
M		
N		
P		
R		
S		
T		
U		
V		
W		
X		
Y	ADDER OVERFLOW	*
Z	Digital ground	PS †

Board No. 9, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS	†
2	UNDERFLOW Ch 1	*	
3			
4			
5			
6	TSCK	4α15	
7	OS DONE Ch 2	*	11α15
8	OS DONE Ch 1	*	11α14
9	MSB-5	*	15α21
10	PHASE 1	*	6ϕT, 17ϕS
11	OSR LOAD	*	8Hi2ϕB, 8Lo2ϕB, 8HilϕB, 8LolϕB, 17ϕ18
12	OSR CLOCK Ch 1	*	8HilϕC, 8LolϕC
13	OSR CLOCK Ch 2	*	8Hi2ϕC, 8Lo2ϕC
14	LSBOT+2	4α4	
15	LSBO+2 Ch 2	8Hi2α12	
16	LSBO+2 Ch 1	8Hilα12	
17	cLSB+2	*	15α18
18	CHAN SEL 0	11ϕ17	
19	CHAN SEL 1	11ϕ16	
20			
21			
22			

Board No. 9, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	LOAD SAM	4αW	
C	MSB-1	*	15α10
D	T-UNDERFLOW	*	4α10
E	UNDERFLOW Ch 2	*	
F	MSB	*	15α11
H	MSB-3	*	15α19
J	MSB-2	*	15α9
K	MSB-4	*	15α20
L			
M	MSBOT-1	4α2	
N	MSBO-1 Ch 2	8Hi2α18	
P	MSBO-1 Ch 1	8Hilα18	
R	LSB+4	*	15α14
S	LSB+5	*	15α15
T	MSBO Ch 1	8Hilα17	
U	MSBO Ch 2	8Hi2α17	
V	MSBOT	4α1	
W	LSB+3	*	15α13
X	MSBO-2 Ch 1	8Hilα19	
Y	MSBO-2 Ch 2	8Hi2α19	
Z	MSBT-2	4α3	

Board No. 9, Side α

Pin	Signal Name	Origin	
1	PHASE 3	*	6φU
2	HIGH BIT Ch 2	8Hi2α16	
3	OS ENABLE Ch 1	*	
4	OS ENABLE Ch 2	*	
5			
6			
7			
8			
9	ANALOG SW CONTROL	*	2αK, 17φR
10	50 kHz	11α11	4αD
11			
12	AC1	*	8Hi1α21, 8Lo1α21
13			
14			
15			
16			
17			
18	WIND TEST SWITCH	F.P. SW 23	
19	100 Hz	11αK	16α17, 17αL
20	EOC	2φB	
21	WINDY BUS	*	11αU, 9αV, 17αK, CONN.J14 PIN 2, F.P.
22	+12 V	PS	†

Board No. 9, Side α

Pin	Signal Name	Origin
A	HIGH BIT Ch 1	8Hi1α16
B	SINGLE	FP 15α8 SW 27
C	LSBOT	4αB
D	LSBO Ch 2	8Hi2α14
E	LSBO Ch 1	8Hi1α14
F	LSB	* 15α16
H	LSB+1	* 15α17
J	LSBO+1 Ch 1	8Hi1α13
K	LSBO+1 Ch 2	8Hi2α13
L	LSBOT+1	4αA
M	GOAD	* 2φT
N	UPDATE	4α18 17αA
P	HOLD	* 2αJ
R	PHASE 5	* 4αT, 17φT
S	AC2	* 8Hi2α21, 8Lo2α21
T	GOOD TIME	* 4φB
U	THRESH	4φ21 17αJ
V	WINDY BUS	9α21 11αU, 17αK, CONN.J14 PIN 2, F.P.
W	WIND INHIBIT	
X	WIND INPUT	FP SW 23
Y	SHIELD	CONNJ15 PIN 11 F.P. SW24
Z	Digital ground	PS †

Board No. 11, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS	†
2	DX0	15ϕ13	14ϕJ, 12ϕ22, 16αH, 17α13, 18ϕN, 19ϕJ, 20ϕJ
3	DX1	15ϕ11	14ϕL, 12ϕ21, 16αA, 17α12, 18ϕM, 19ϕL, 20ϕL
4	DX2	15ϕ9	14ϕM, 12ϕ20, 16αE, 17α11, 18ϕL, 19ϕM, 20ϕM
5	DX3	15ϕ12	14ϕN, 12ϕ19, 16αJ, 17α10, 18ϕK, 19ϕN, 20ϕN
6	DX4	15ϕ10	14ϕV, 12ϕ18, 16αD, 17α9, 18ϕJ, 19ϕV, 20ϕV
7	DX5	15ϕ8	14ϕX, 12ϕ17, 16αF, 17α8, 18ϕH, 19ϕX, 20ϕX
8	DEVSEL	51ϕ21	
9	1MHz	15ϕD	
10	DX11	15ϕ2	14αR, 12ϕU, 17α2, 18αD, 19αR, 20αR, 20ϕR
11	DX10	15ϕ4	14αP, 12ϕV, 17α3, 18αC, 19αP, 20αP, 20ϕS
12	DX8	15ϕ3	14αL, 12ϕX, 17α5, 18αA, 19αL, 20αL, 20ϕV
13	DX7	15ϕ5	14ϕZ, 12ϕY, 17α6, 18ϕE, 19ϕZ, 20ϕZ
14	DX6	15ϕ7	14ϕY, 12ϕZ, 17α7, 18ϕF, 19ϕY, 20ϕY
15	DX9	15ϕ6	14αN, 12ϕW, 17α4, 18αB, 19αN, 20αN, 20ϕT
16	Ch SEL 1	*	9ϕ19
17	Ch SEL 0	*	9ϕ18
18	SEL CHAN	11α7	
19	SPARE	*	
20	TIN	*	18ϕW
21	STATIN	*	18ϕX
22	SAMPLEX	*	17αP

Board No. 11, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	+5 V	PS	†
C	MINUTES	*	16α14
D	XTA	15ϕ20	
E	XTB	15ϕ18	
F	LXMAR	15ϕ19	14αM, 12ϕT, 19αM, 20αM, 20ϕP
H	HDX0	*	4ϕC, 16αL, 18α16
J	HDX1	*	4ϕD, 16ϕ4, 18α17
K	HDX2	*	4ϕE, 16ϕ6, 18α18
L	HDX3	*	4ϕF, 16ϕ5, 18α19
M	HDX4	*	4ϕH, 16ϕC, 18αK
N	HDX5	*	4ϕJ, 16ϕB, 18αJ
P	HDX6	*	4ϕK, 16ϕD
R	HDX7	*	4ϕL, 16ϕE
S	HDX8	*	4ϕT, 16ϕT
T	HDX9	*	4ϕU, 16ϕS
U	HDX10	*	4ϕV, 16ϕV
V	HDX11	*	4ϕW, 16ϕU
W	OUT HI	*	11α18
X	OUT LO	*	11αR
Y	T OUT	*	18ϕV
Z	SECONDS	*	16α16

Board No. 11, Side α

Pin	Signal Name	Origin	
1	THSET	*	4ϕS
2	SEC	*	
3	MODE	*	16ϕY, 18α15
4	DATA ACCEPT	*	
5	HIDIS	*	16ϕR
6	MIN	*	
7	SEL CHAN	*	11ϕ18
8	OUT MID	*	11αT
9	BEGIN	*	11α21, 16α18
10	FUN HI	*	16αB, 18αM
11	50 kHz	*	9α10, 4αD
12	TIME BASE	16α15	
13	TS DONE	4αN	
14	Ch 1 DONE	9ϕ8	
15	Ch 2 DONE	9ϕ7	
16	WINDY LED	FP LI3	
17	WINDY W	*	CONN. J13 PIN50
18	OUT HI	11ϕW	
19			
20	ZERO ENABLE	*	4αV
21	BEGIN	11α9	16α18
22	+12 V	PS	†

Board No. 11, Side α

Pin	Signal Name	Origin	
A	OPRINT	*	11αM
B	RTC CLEAR	*	16αY
C	LO DIS	*	16φ3
D	SW REG	*	15αH
E	PEAK D	*	17φ19
F	OUTPUT D	*	15α12
H	FUN LO	*	15αX
J	$\overline{CT}$	*	15φX
K	100 Hz	*	9α19, 16α17, 17αL
L	READ SAM	*	4α20
M	$\overline{OPRINT}$	11αA	
N	$\overline{PRINT}$	11αN	CONN. J13 PIN36
P	L OUT LO	*	12α1
R	OUT LO	11φX	
S	L OUT MID	*	12α8
T	$\overline{OUT\ MID}$	11α8	
U	$\overline{WINDY\ BUS}$	9α21	9αV, 17αK, CONN. J14 PIN2
V	$\overline{L\ OUT\ HI}$	*	12α15
W	$\overline{DATA\ READY}$	*	15α2
X	SAMPLE	17αF	
Y	+5 V	PS	†
Z	Digital ground	PS	†

Board No. 12, Side ϕ

Pin	Signal Name	Origin	
1	+5 V	PS	†
2	$\overline{8LO}$	*	15ϕJ
3	$\overline{8HI}$	*	15ϕL
4	A9	*	15ϕ14
5	$\overline{RSEL\ 4}$	*	18αE
6	$\overline{RSEL\ 3}$	*	18αF
7	$\overline{RSEL\ 2}$	*	18αH
8			
9			
10			
11			
12			
13			
14			
15			
16			
17	DX5	15ϕ8	14ϕX, 11ϕ7, 16αF, 17α8, 18ϕH, 19ϕX, 20ϕX
18	DX4	15ϕ10	14ϕV, 11ϕ6, 16αD, 17α9, 18ϕJ, 19ϕV, 20ϕV
19	DX3	15ϕ12	14ϕN, 11ϕ5, 16αJ, 17α10,18ϕK, 19ϕN, 20ϕN
20	DX2	15ϕ9	14ϕM, 11ϕ4, 16αE, 17α11,18ϕL, 19ϕM, 20ϕM
21	DX1	15ϕ11	14ϕL, 11ϕ3, 16αA, 17α12,19ϕM, 19ϕL, 20ϕL
22	DX0	15ϕ13	14ϕJ, 11ϕ2, 16αH, 17α13,18ϕN, 19ϕJ, 20ϕJ

Board No. 12, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	XTC	15ϕ17	14ϕK, 19ϕK, 20ϕK
C			
D	FIELD 0	18αY	14ϕW
E	A9	*	15ϕH
F	ROM A8	*	18ϕ21, 20ϕ20
H	ROM A7	*	15ϕV, 18ϕ20, 20ϕ19
J	ROM A6	*	15ϕU, 18ϕ19, 20ϕ18
K	ROM A5	*	15ϕT, 18ϕ18, 20ϕ17
L	ROM A4	*	15ϕS, 18ϕ17, 20ϕ16
M	ROM A3	*	15ϕR, 18ϕ16, 20ϕ15
N	ROM A2	*	15ϕP, 18ϕ15, 20ϕ14
P	ROM A1	*	15ϕN, 18ϕ14, 20ϕ13
R	ROM A0	*	15ϕM, 18ϕ13, 20ϕ12
S			
T	LXMAR	15ϕ19	14αM, 11ϕF, 19αM, 20αM, 20ϕP
U	DX11	15ϕ2	14αR, 11ϕ10,17α2, 18αD, 19αR, 20αR, 20ϕR
V	DX10	15ϕ4	14αP, 11ϕ11,17α3, 18αC, 19αP, 20αP, 20ϕS
W	DX9	15ϕ6	14αN, 11ϕ15,17α4, 18αB, 19αN, 20αN, 20ϕT
X	DX8	15ϕ3	14αL, 11ϕ12,17α5, 18αA, 19αL, 20αL, 20ϕV
Y	DX7	15ϕ5	14ϕZ, 11ϕ13,17α6, 18ϕE, 19ϕZ, 20ϕZ
Z	DX6	15ϕ7	14ϕY, 11ϕ14,17α7, 18ϕF, 19ϕY, 20ϕY

Board No. 12, Side α

Pin	Signal Name	Origin	
1	LOUT LO	11αP	
2	PIO 29	*	CONN J13 PIN 16
3	PIO 26	*	CONN J13 PIN 25
4	PIO 28	*	CONN J13 PIN 35
5	PIO 33	*	CONN J13 PIN 44
6	PIO 35	*	CONN J13 PIN 33
7	PIO 30	*	CONN J13 PIN 30
8	LOUT MID	11αS	
9	PIO 17	*	CONN J13 PIN 7
10	PIO 14	*	CONN J13 PIN 4
11	PIO 16	*	CONN J13 PIN 20
12	PIO 21	*	CONN J13 PIN 46
13	PIO 23	*	CONN J13 PIN 42
14	PIO 18	*	CONN J13 PIN 22
15	LOUT HI	11αV	
16	PIO 5	*	CONN J13 PIN 39
17	PIO 2	*	CONN J13 PIN 13
18	PIO 4	*	CONN J13 PIN 24
19	PIO 9	*	CONN J13 PIN 14
20	PIO 11	*	CONN J13 PIN 23
21	PIO 6	*	CONN J13 PIN 11
22	+5 V	PS	†

Board No. 12, Side α

Pin	Signal Name	Origin	
A			
B			
C			
D	PIO 32	*	CONN J13 PIN 21
E	PIO 36	*	CONN J13 PIN 31
F	PIO 34	*	CONN J13 PIN 6
H	PIO 25	*	CONN J13 PIN 5
J	PIO 27	*	CONN J13 PIN 1
K	PIO 31	*	CONN J13 PIN 10
L	PIO 20	*	CONN J13 PIN 18
M	PIO 24	*	CONN J13 PIN 49
N	PIO 22	*	CONN J13 PIN 40
P	PIO 13	*	CONN J13 PIN 9
R	PIO 15	*	CONN J13 PIN 2
S	PIO 19	*	CONN J13 PIN 27
T	PIO 8	*	CONN J13 PIN 3
U	PIO 12	*	CONN J13 PIN 43
V	PIO 10	*	CONN J13 PIN 12
W	PIO 1	*	CONN J13 PIN 34
X	PIO 3	*	CONN J13 PIN 45
Y	PIO 7	*	CONN J13 PIN 38
Z	Digital	PS	†

Board No. 14, Side ϕ

Pin	Signal Name	Origin
1	+5	PS †

Board No. 14, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B			
C			
D			
E			
F			
H			
J	DX0	15ϕ13	12ϕ22, 11ϕ2, 16αH, 17α13, 18ϕN, 19ϕJ, 20ϕJ
K	XTC	15ϕ17	12ϕB, 19ϕK, 20ϕK
L	DX1	15ϕ11	12ϕ21, 11ϕ3, 16αA, 17α12, 18ϕM, 19ϕL, 20ϕL
M	DX2	15ϕ9	12ϕ20, 11ϕ4, 16αE, 17α11, 18ϕL, 19ϕM, 20ϕM
N	DX3	15ϕ12	12ϕ19, 11ϕ5, 16αJ, 17α10, 18ϕK, 19ϕN, 20ϕN
P			
R			
S			
T			
U			
V	DX4	15ϕ10	12ϕ18, 11ϕ6, 16αD, 17α9, 18ϕJ, 19ϕV, 20ϕV
W	FIELD 0	18α4	12ϕD
X	DX5	15ϕ8	12ϕ17, 11ϕ7, 16αF, 17α8, 18ϕH, 19ϕX, 20ϕX
Y	DX6	15ϕ7	12ϕZ, 11ϕ14, 17α7, 18ϕF, 19ϕY, 20ϕY
Z	DX7	15ϕ5	12ϕY, 11ϕ13, 17α6, 18ϕE, 19ϕZ, 20ϕZ

Board No. 14, Side α

Pin	Signal Name	Origin
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22	+5	PS †

Board No. 14, Side α

Pin	Signal Name	Origin	
A			
B			
C			
D			
E			
F			
H			
J			
K			
L	DX8	15φ3	12φX, 11φ12, 17α5, 18αA, 19αL, 20αL, 20φV
M	LXMAR	15φ19	12φT, 11φF, 19αM, 20αM, 20φP
N	DX9	15φ6	12φW, 11φ15, 17α4, 18αB, 19αN, 20αN, 20φT
P	DX10	15φ4	12φV, 11φ11, 17α3, 18αC, 19αP, 20αP, 20φS
R	DX11	15φ2	12φU, 11φ10, 17α2, 18αD, 19αR, 20αR, 20φR
S			
T			
U			
V			
W			
X			
Y			
Z	Digital ground	PS	†

Board No. 15, Side ϕ

Pin	Signal Name	Origin	
1	+5 V	PS	†
2	DX11	*	14αR, 12ϕU, 11ϕ10, 17α2, 18αD, 19αR, 20αR, 20ϕR
3	DX8	*	14αL, 12ϕX, 11ϕ12, 17α5, 18αA, 19αL, 20αL, 20ϕV
4	DX10	*	14αP, 12ϕV, 11ϕ11, 17α3, 18αC, 19αP, 20αP, 20ϕS
5	DX7	*	14ϕZ, 12ϕY, 11ϕ13, 17α6, 18ϕE, 19ϕZ, 20ϕZ
6	DX9	*	14αN, 12ϕW, 11ϕ15, 17α4, 18αB, 19αN, 20αN, 20ϕT
7	DX6	*	14ϕY, 12ϕZ, 11ϕ14, 17α7, 18ϕF, 19ϕY, 20ϕY
8	DX5	*	14ϕX, 12ϕ17, 11ϕ7, 16αF, 17α8, 18ϕH, 19ϕX, 20ϕX
9	DX2	*	14ϕM, 12ϕ20, 11ϕ4, 16αE, 17α11, 18ϕL, 19ϕM, 20ϕM
10	DX4	*	14ϕV, 12ϕ18, 11ϕ6, 16αD, 17α9, 18ϕJ, 19ϕV, 20ϕV
11	DX1	*	14ϕL, 12ϕ21, 11ϕ3, 16αA, 17α12, 18ϕM, 19ϕL, 20ϕL
12	DX3	*	14ϕN, 12ϕ19, 11ϕ5, 16αJ, 17α10, 18ϕK, 19ϕN, 20ϕN
13	DX0	*	14ϕJ, 12ϕ22, 11ϕ2, 16αH, 17α13, 18ϕN, 19ϕJ, 20ϕJ
14	A9	12ϕ4	
15	FETCH	*	
16	.5MHz Clock Input	15ϕC	
17	XTC	*	14ϕK, 12ϕB, 19ϕK, 20ϕK
18	XTB	*	11ϕE
19	LXMAR	*	14αM, 12ϕT, 11ϕF, 19αM, 20αM, 20ϕP
20	XTA	*	11ϕD
21	DEVSEL	*	11ϕ8
22			

Board No. 15, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	4 MHz	*	
C	0.5 MHz	*	15ϕ16
D	1 MHz	*	11ϕ9
E	SKP	*	
F	$\overline{\text{CP}}$ REQUEST	PS(+5V)	to +5 supply
H	$\overline{\text{A9}}$	12ϕE	
J	$\overline{\text{8LO}}$	12ϕ2	
K	-9 V	PS	From separate 9v supply. Used only
L	$\overline{\text{8HI}}$	12ϕ3	if U1 thru U6 installed.
M	ROM A0	12ϕR	18ϕ13, 20ϕ12
N	ROM A1	12ϕP	18ϕ14, 20ϕ13
P	ROM A2	12ϕN	18ϕ15, 20ϕ14
R	ROM A3	12ϕM	18ϕ16, 20ϕ15
S	ROM A4	12ϕL	18ϕ17, 20ϕ16
T	ROM A5	12ϕK	18ϕ18, 20ϕ17
U	ROM A6	12ϕJ	18ϕ19, 20ϕ18
V	ROM A7	12ϕH	18ϕ20, 20ϕ19
W	$\overline{\text{SWSEL}}$	*	
X	$\overline{\text{C1}}$	11αJ	
Y	$\overline{\text{MEMSEL}}$	*	18α20
Z	$\overline{\text{BIT 0}}$	FP	
		SW 1	

Board No. 15, Side α

Pin	Signal Name	Origin
1	$\overline{\text{CPSEL}}$	*
2	$\overline{\text{DATA READY}}$	11αW
3	RTC	16αU
4	PSEL 2	CONN J13 PIN 47
5	SHIFT F	FP SW 13
6	$\overline{\text{DATA REQUEST}}$	CONN J13 PIN 15
7	$\overline{\text{KEY START}}$	17αU
8	SINGLE	FP SW 27 9αB
9	MSB-2	9ϕJ
10	MSB-1	9ϕC
11	MSB	9ϕF
12	OUTPUT D	11αF
13	LSB+3	9ϕW
14	LSB+4	9ϕR
15	LSB+5	9ϕS
16	LSB	9αF
17	LSB+1	9αH
18	LSB+2	9ϕ17
19	MSB-3	9ϕH
20	MSB-4	9ϕK
21	MSB-5	9ϕ9
22	+5 V	PS †

Board No. 15, Side α

Pin	Signal Name	Origin
A	DATA F	* 18αL
B	BIT 1	FP SW 2
C	BIT 2	FP SW 3
D	BIT 7	FP SW 8
E	BIT 6	FP SW 7
F	BIT 8	FP SW 9
H	SW REG	11αD
J	BIT 3	FP SW 4
K	BIT 4	FP SW 5
L	BIT 11	FP SW 12
M	BIT 10	FP SW 11
N	BIT 9	FP SW 10
P	BIT 5	FP SW 6
R	THF	17αV
S	SEL/LEQ	FP SW 15
T	PSEL 1	J13 PIN 8
U		
V	KEY PRINT	CONN J13 PIN 19
W	KEY SAMPLE	17αE
X	FUNLO	11αH
Y	+12 V	PS †
Z	Digital	PS †

Board No. 16, Side ϕ

Pin	Signal Name	Origin	
1	+12 V	PS	†
2	+5 V	PS	†
3	LODIS	11αC	
4	HDX1	11ϕJ	4ϕD, 18α17
5	HDX3	11ϕL	4ϕF, 18α19
6	HDX2	11ϕK	4ϕE, 18α18
7	MSBD-2	*	21-11
8	MSBD	*	21-9
9	LSBD+5	*	21-14
10	LSBD+7	*	21-16
11	LSBD+1	*	21-19
12	LSBD+3	*	21-21
13	MSBD-6	*	21-6
14	MSBD-4	*	21-4
15	$\overline{\text{MSBDDP}}$	*	21-8
16	$\overline{\text{LSBDDP}}$	*	21-22
17	POS 13	*	FP SW 18
18	POS 14	*	FP SW 18
19	POS 15	*	FP SW 18
20	POS 16	*	FP SW 18
21	POS 9	*	FP SW 18
22	POS 10	*	FP SW 18

Board No. 16, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	HDX5	11ϕN	4ϕJ, 18αJ
C	HDX4	11ϕM	4ϕH, 18αK
D	HDX6	11ϕP	4ϕK
E	HDX7	11ϕR	4ϕL
F	MSBD-7	*	21-7
H	MSBD-5	*	21-5
J	LSBD	*	21-13
K	LSBD+2	*	21-20
L	LSBD+4	*	21-18
M	LSBD+6	*	21-15
N	MSBD-3	*	21-2
P	MSBD-1	*	21-10
R	HI DIS	11α5	
S	HDX9	11ϕT	4ϕU
T	HDX8	11ϕS	4ϕT
U	HDX11	11ϕV	4ϕW
V	4DX10	11ϕU	4ϕV
W	$\overline{\text{LSBDDP+1}}$	*	21-17
X	$\overline{\text{MSBDDP-1}}$	*	21-3
Y	MODE	11α3	18α15
Z	STAND-BY LED	*	FP L1

Board No. 16, Side α

Pin	Signal Name	Origin	
1	POS 11	FP	
		SW 18	
2	POS 12	FP	
		SW 18	
3	POS 5	FP	
		SW 18	
4	POS 6	FP	
		SW 18	
5	POS 7	FP	
		SW 18	
6	POS 8	FP	
		SW 18	
7	POS 1	FP	
		SW 18	
8	POS 2	FP	
		SW 18	
9	POS 3	FP	
		SW 18	
10	POS 4	FP	
		SW 18	
11	START LED	*	FP
			L12
12	PEAK CHANNEL	*	17φP
13	V DISPLAY	*	FP
			SW 16, 21-1
14	MINUTES	11φC	
15	TIME BASE	*	11α12
16	SECONDS	11φZ	
17	100 Hz	11αK	9α19, 17αL
18	BEGIN	11α9	11α21
19			
20			
21	+5	PS	†
22	+12	PS	†

Board No. 16, Side α

Pin	Signal Name	Origin	
A	DX1	15φ11	14φL, 12φ21, 11φ3, 17α12, 18φM, 19φL, 20φL
B	FUNHI	11α10	18αM
C	F4	FP SW 17	
D	DX4	15φ10	14φV, 12φ18, 11φ6, 17α9, 18φJ, 19φV, 20φV
E	DX2	15φ9	14φM, 12φ20, 11φ4, 17α11, 18φL, 19φM, 20φM
F	DX5	15φ8	14φX, 12φ17, 11φ7, 17α8, 18φH, 19φX, 20φX
H	DX0	15φ13	14φJ, 12φ22, 11φ2, 17α13, 18φN, 19φJ, 20φJ
J	DX3	15φ12	14φN, 12φ19, 11φ5, 17α10 18φK, 19φN, 20φN
K	EXECUTE FUNCTION	*	FP SW 16
L	HDX0	11φH	4φC, 18α16
M	TO MIC CAL RELAY	*	CONN J15 PIN 2, FP SW 26
N	+12 V Ext Batt (Red No. 18 gauge)	CONN J16 PIN 1	
P	Minitape Relay Hi	*	FP J12
R	+12 V P.S. (Red No. 18)	PS	
S	Minitape Relay Lo	*	FP J12
T	On/off Switch (Red No. 18)	PS SW 28	
U	$\overline{\text{RTC}}$	*	15α3
V	+12 V Int. (Gray Batt. No. 18)	PS	
W	+15 V (Orange No. 18)	PS	
X	Ground from Ext.Batt. Digital P.S. (Black No. 18)	PS	
Y	RTC Clear	11αB	
Z	Digital ground	PS	†

Board No. 17, Side ϕ

Pin	Signal Name	Origin	
1	12 V	PS	†
2	5 V	PS	†
3	A_0	6ϕP	4ϕ20, 4αX, 2αC
4	A_1	6ϕJ	4ϕY, 4αY, 2αB
5	A_2	6ϕF	4ϕX, 4αR, 2αA
6	PEAK 11	*	
7	PEAK 10	*	
8	PEAK 9	*	
9	PEAK 8	*	
10	PEAK 7	*	
11	PEAK 6	*	
12	PEAK 5	*	
13	PEAK 4	*	
14	PEAK 3	*	
15	PEAK 2	*	
16	PEAK 1	*	
17	PEAK 0	*	
18	OSR LOAD	9ϕ11	8 Hi2ϕB, 8 Lo2ϕB, 8 HilϕB, 8 LolϕB
19	PEAK D	11αE	
20			
21			
22			

Board No. 17, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B			
C	$\overline{\text{MSB}}$	2ϕC	4ϕ19, 6ϕR
D	MSB-1	2ϕD	4ϕZ, 6ϕN
E	MSB-2	2ϕH	4ϕM, 6ϕM
F	MSB-3	2ϕF	4ϕN, 6ϕB
H	MSB-4	2ϕE	4ϕP, 6ϕC
J	LSB+4	2ϕL	4ϕR, 6ϕL
K	LSB+3	2ϕK	4ϕ3, 6ϕK
L	LSB+2	2ϕJ	4ϕ4, 6ϕD
M	LSB+1	2ϕM	4ϕ5, 6ϕE
N	LSB	2ϕN	4ϕ6, 6ϕH
P	PEAK CHAN	16α12	
R	ANALOG SWITCH	9α9	2αK
S	PHASE 1	9ϕ10	6ϕT
T	PHASE 5	9αR	4αT
U	ZERO	4α21	8 Lo1α20, 8 Hi1α20, 8 Hi2α20, 8 Lo2α20
V			
W			
X			
Y			
Z			

Board No. 17, Side α

Pin	Signal Name	Origin						
1								
2	DX11	15φ2	14αR,	12φU,	11φ10,	18αD,	19αR,	20αR, 20φR
3	DX10	15φ4	14αP,	12φV,	11φ11,	18αC,	19αP,	20αP, 20φS
4	DX9	15φ6	14αN,	12φW,	11φ15,	18αB,	19αN,	20αN, 20φT
5	DX8	15φ3	14αL,	12φX,	11φ12,	18αA,	19αL,	20αL, 20φV
6	DX7	15φ5	14φZ,	12φY,	11φ13,	18φE,	19φZ,	20φZ
7	DX6	15φ7	14φY,	12φZ,	11φ14,	18φF,	19φY,	20φY
8	DX5	15φ8	14φX,	12φ17,	11φ7,	16αF,	18φH,	19φX, 20φX
9	DX4	15φ10	14φV,	12φ18,	11φ6,	16αD,	18φJ,	19φV, 20φV
10	DX3	15φ12	14φN,	12φ19,	11φ5,	10αJ,	18φK,	19φN, 20φN
11	DX2	15φ9	14φM,	12φ20,	11φ4,	16αE,	18φL,	19φM, 20φM
12	DX1	15φ11	14φL,	12φ21,	11φ3,	16αA,	18φM,	19φL, 20φL
13	DX0	15φ13	14φJ,	12φ22,	11φ2,	16αH,	18φN,	19φJ, 20φJ
14								
15								
16								
17								
18								
19								
20								
21	+5	PS	†					
22	+12	PS	†					

Board No. 17, Side α

Pin	Signal Name	Origin	
A	UPDATE	4α18	9αN
B	MODE 3	18α9	
C	MODE 4	18α11	
D	T ZERO	*	4α6
E	KEY SAMPLE	*	15αW
F	SAMPLE	*	11αX
H	SAMPLE TRIG	*	FP SW 22, FP J1
J	THRESH	4φ21	9αU
K	WINDY BUS	9α21	11αU, 9αV
L	100 Hz	11αK	9α19, 16α17
M	K SAMPLE	*	FP SW 21
N	K SAMPLE	*	FP SW 21
P	SAMPLEX	11φ22	
R	K START	*	FP SW 20
S	K START	*	FP SW 20
T	START TRIG	*	FP J2, FP SW 22
U	KEY START	*	15α7
V	THF	*	15αR
W	THRESH UP	*	FP SW 22
X	THRESH DOWN	*	FP SW 22
Y			
Z	Digital ground	PS	†

Board No. 18, Side ϕ

Pin	Signal Name	Origin	
1	+12	PS	†
2	+5	PS	†
3	DX7 (RBR8)	*	
4	DX6 (RBR7)	*	
5	DX5 (RBR6)	*	
6	DX4 (RBR5)	*	
7	DX3 (RBR4)	*	
8	DX2 (RBR3)	*	
9	DX1 (RBR2)	*	
10	DX0 (RBR1)	*	
11	RXC	*	
12	19.2 kHz	*	
13	ROM A0	12ϕR	15ϕM, 20ϕ12
14	ROM A1	12ϕP	15ϕN, 20ϕ13
15	ROM A2	12ϕN	15ϕP, 20ϕ14
16	ROM A3	12ϕM	15ϕR, 20ϕ15
17	ROM A4	12ϕL	15ϕS, 20ϕ16
18	ROM A5	12ϕK	15ϕT, 20ϕ17
19	ROM A6	12ϕJ	15ϕU, 20ϕ18
20	ROM A7	12ϕH	15ϕV, 20ϕ19
21	ROM A8	12ϕF	20ϕ20
22			

Board No. 18, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B	Relay Coil (ground to activate)	*	
C	Relay Contact Hi	*	
D	Relay Contact Lo	*	
E	DX7 (TBR8)	15ϕ5	14ϕZ, 12ϕY, 11ϕ13, 17α6, 19ϕZ, 20ϕZ
F	DX6 (TBR7)	15ϕ7	14ϕY, 12ϕZ, 11ϕ14, 17α7, 19ϕY, 20ϕY
H	DX5 (TBR6)	15ϕ8	14ϕX, 12ϕ17, 11ϕ7, 16αF, 17α8, 19ϕX, 20ϕX
J	DX4 (TBR5)	15ϕ10	14ϕV, 12ϕ18, 11ϕ6, 16αD, 17α9, 19ϕV, 20ϕV
K	DX3 (TBR4)	15ϕ12	14ϕN, 12ϕ19, 11ϕ5, 16αJ, 17α10, 19ϕN, 20ϕN
L	DX2 (TBR3)	15ϕ9	14ϕM, 12ϕ20, 11ϕ4, 16αE, 17α11, 19ϕM, 20ϕM
M	DX1 (TBR2)	15ϕ11	14ϕL, 12ϕ21, 11ϕ3, 16αA, 17α12, 19ϕL, 20ϕL
N	DX0 (TBR1)	15ϕ13	14ϕJ, 12ϕ22, 11ϕ2, 16αH, 17α13, 19ϕJ, 20ϕJ
P	DR	*	
R	TBRE	*	
S	PE	*	
T	FE	*	
U	OE	*	
V	TOUT	11ϕY	
W	TIN	11ϕ20	
X	STATIN	11ϕ21	
Y	CASSETTE IN	FP J3	
Z	CASSETTE OUT	*	FP J11

Board No. 18, Side α

Pin	Signal Name	Origin	
1	M11	*	
2	M10	*	
3	M9	*	FP L11
4	M8	*	FP L10
5	M7	*	FP L9
6	M6	*	FP L8
7	M5	*	FP L7
8	M4	*	FP L6
9	MODE 3	*	17αB
10	M3	*	FP L5
11	MODE 4	*	17αC
12	M2	*	FP L4
13	M1	*	FP L3
14	M0	*	FP L2
15	MODE	11α3	16φY
16	HDX0	11φH	4φC, 16αL
17	HDX1	11φJ	4φD, 16φ4
18	HDX2	11φK	4φE, 16φ6
19	HDX3	11φL	4φF, 16φ5
20	MEMSEL	15φY	
21	+5 V	PS	†
22	+12 V	PS	†

Board No. 18, Side α

Pin	Signal Name	Origin	
A	DX8	15φ3	14αL, 12φX, 11φ12, 17α5, 19αL, 20αL, 20φV
B	DX9	15φ6	14αN, 12φW, 11φ15, 17α4, 19αN, 20αN, 20φT
C	DX10	15φ4	14αP, 12φV, 11φ11, 17α3, 19αP, 20αP, 20φS
D	DX11	15φ2	14αR, 12φU, 11φ10, 17α2, 19αR, 20αR, 20φR
E	$\overline{\text{RSEL 4}}$	12φ5	
F	$\overline{\text{RSEL 3}}$	12φ6	
H	$\overline{\text{RSEL 2}}$	12φ7	
J	HDX5	11φN	4φJ, 16φB
K	HDX4	11φM	4φH, 16φC
L	DATA F	15αA	
M	$\overline{\text{FUNHI}}$	11α10	16αB
N	$\overline{\text{LSBSN}}$	*	
P	$\overline{\text{LSBSN +1}}$	*	
R	$\overline{\text{LSBSN +2}}$	*	
S	$\overline{\text{MSBSN -2}}$	*	Serial number for each unit in one's complement binary (Same as stamped on front panel)
T	$\overline{\text{MSBSN -1}}$	*	
U	$\overline{\text{MSBSN}}$	*	
V	FIELD 3	*	
W	FIELD 2	*	20φW
X	FIELD 1	*	19φW
Y	FIELD 0	*	14φW, 12φD
Z	Digital ground	PS	†

Board No. 19, Side ϕ

Pin	Signal Name	Origin
1	+5	PS †
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		

Board No. 19, Side ϕ

Pin	Signal Name	Origin	
A	Digital ground	PS	†
B			
C			
D			
E			
F			
H			
J	DX0	15ϕ13	12ϕ22, 11ϕ2, 16αH, 17α13, 18ϕN, 20ϕJ
K	XTC	15ϕ17	12ϕB, 20ϕK
L	DX1	15ϕ11	12ϕ21, 11ϕ3, 16αA, 17α12, 18ϕM, 20ϕL
M	DX2	15ϕ9	12ϕ20, 11ϕ4, 16αE, 17α11, 18ϕL, 20ϕM
N	DX3	15ϕ12	12ϕ19, 11ϕ5, 16αJ, 17α10, 18ϕK, 20ϕN
P			
R			
S			
T			
U			
V	DX4	15ϕ10	12ϕ18, 11ϕ6, 16αD, 17α9, 18ϕJ, 20ϕV
W	FIELD 1	18αX	
X	DX5	15ϕ8	12ϕ17, 11ϕ7, 16αF, 17α8, 18ϕH, 20ϕX
Y	DX6	15ϕ7	12ϕZ, 11ϕ14, 17α7, 18ϕF, 20ϕY
Z	DX7	15ϕ5	12ϕY, 11ϕ13, 17α6, 18ϕE, 20ϕZ

Board No. 19, Side α

Pin	Signal Name	Origin
1		
2		
3		
4		
5		
6		
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8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22	+5	PS †

Board No. 19, Side α

Pin	Signal Name	Origin	
A			
B			
C			
D			
E			
F			
H			
J			
K			
L	DX8	15φ3	12φX, 11φ12, 17α5, 18αA, 20αL, 20φV
M	LXMAR	15φ19	12φT, 11φF, 20αM, 20φP
N	DX9	15φ6	12φW, 11φ15, 17α4, 18αB, 20αN, 20φT
P	DX10	15φ4	12φV, 11φ11, 17α3, 18αC, 20αP, 20φS
R	DX11	15φ2	12φU, 11φ10, 17α2, 18αD, 20αR, 20φR
S			
T			
U			
V			
W			
X			
Y			
Z	Digital ground	PS	†

Board No. 20, Side ϕ

Pin	Signal Name	Origin	
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12	ROM A0	12ϕR	15ϕM, 18ϕ13
13	ROM A1	12ϕP	15ϕN, 18ϕ14
14	ROM A2	12ϕN	15ϕP, 18ϕ15
15	ROM A3	12ϕM	15ϕR, 18ϕ16
16	ROM A4	12ϕL	15ϕS, 18ϕ17
17	ROM A5	12ϕK	15ϕT, 18ϕ18
18	ROM A6	12ϕJ	15ϕU, 18ϕ19
19	ROM A7	12ϕH	15ϕV, 18ϕ20
20	ROM A8	12ϕF	18ϕ21
21			
22			

Board No. 20, Side ϕ

Pin	Signal Name	Origin
A	Digital ground	PS
B		
C		
D		
E		
F		
H		
J	DX0	15ϕ13 14ϕJ, 12ϕ22, 11ϕ2, 16αH, 17α13, 19ϕJ, 18ϕN
K	XTC	15ϕ17 14ϕK, 19ϕK, 12ϕB
L	DX1	15ϕ11 14ϕL, 12ϕ21, 11ϕ3, 16αA, 17α12, 19ϕL, 18ϕM
M	DX2	15ϕ9 14ϕM, 12ϕ20, 11ϕ4, 16αE, 17α11, 19ϕM, 18ϕL
N	DX3	15ϕ12 14ϕN, 12ϕ19, 11ϕ5, 16αJ, 17α10, 19ϕN, 18ϕK
P	LXMAR	15ϕ19 14αM, 11ϕF, 19αM, 12ϕT, 20αM
R	DX11	15ϕ2 14αR, 12ϕU, 11ϕ10, 17α2, 19αR, 20αR, 18αD
S	DX10	15ϕ4 14αP, 12ϕV, 11ϕ11, 17α3, 19αP, 20αP, 18αC
T	DX9	15ϕ6 14αN, 12ϕW, 11ϕ15, 17α4, 19αN, 20αN, 18αB
U	DX8	15ϕ3 14αL, 12ϕX, 11ϕ12, 17α5, 19αL, 20αL, 18αA
V	DX4	15ϕ10 14ϕV, 12ϕ18, 11ϕ6, 16αD, 17α9, 19ϕV, 18ϕJ
W	FIELD 2	18ϕW
X	DX5	15ϕ8 14ϕX, 12ϕ17, 11ϕ7, 16αF, 17α8, 19ϕX, 18ϕH
Y	DX6	15ϕ7 14ϕY, 12ϕZ, 11ϕ14, 17α7, 19ϕY, 18ϕF
Z	DX7	15ϕ5 14ϕZ, 12ϕY, 11ϕ13, 17α6, 19ϕZ, 18ϕE

Board No. 20, Side α

Pin	Signal Name	Origin
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22	+5	PS †

Board No. 20, Side α

Pin	Signal Name	Origin	
A			
B			
C			
D			
E			
F			
H			
J			
K			
L	DX8	15φ3	12φX, 11φ12, 17α5, 18αA, 19αL, 14αL, 20φU
M	LXMAR	15φ19	12φT, 11φF, 19αM, 14αM, 20φP
N	DX9	15φ6	12φW, 11φ15, 17α4, 18αB, 19αN, 14αN, 20φT
P	DX10	15φ4	12φV, 11φ11, 17α3, 18αC, 19αP, 14αP, 20φS
R	DX11	15φ2	12φU, 11φ10, 17α2, 18αD, 19αR, 14αR, 20φR
S			
T			
U			
V			
W			
X			
Y			
Z	Digital ground	PS	†

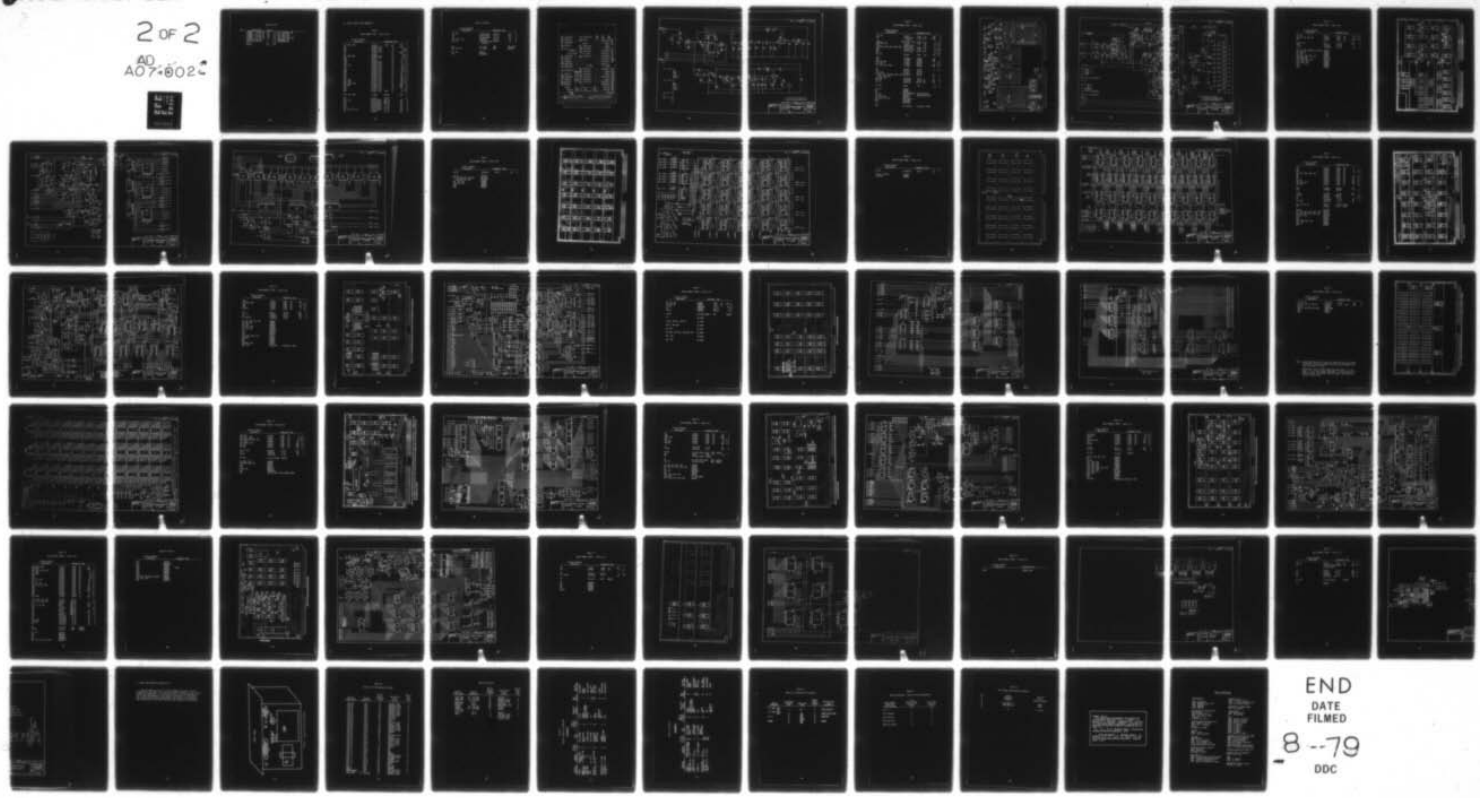
Board No. 21

Pin	Signal Name	Origin
1	VOISPLAY	16α13
2	MSBD-3	16ϕN
3	MSBDDP-1	16ϕX
4	MSBD-4	16ϕ14
5	MSBD-5	16ϕH
6	MSBD-6	16ϕ13
7	MSBD-7	16ϕF
8	MSBDDP	16ϕ15
9	MSBD	16ϕ8
10	MSBD-1	16ϕP
11	MSBD-2	16ϕ7
12		
13	LSBD	16ϕJ
14	LSBD+5	16ϕ9
15	LSBD+6	16ϕM
16	LSBD+7	16ϕ10
17	LSBDDP+1	16ϕW
18	LSBD+4	16ϕL
19	LSBD+1	16ϕ11
20	LSBD+2	16ϕK
21	LSBD+3	16ϕ12
22	LSBDDP	16ϕ16

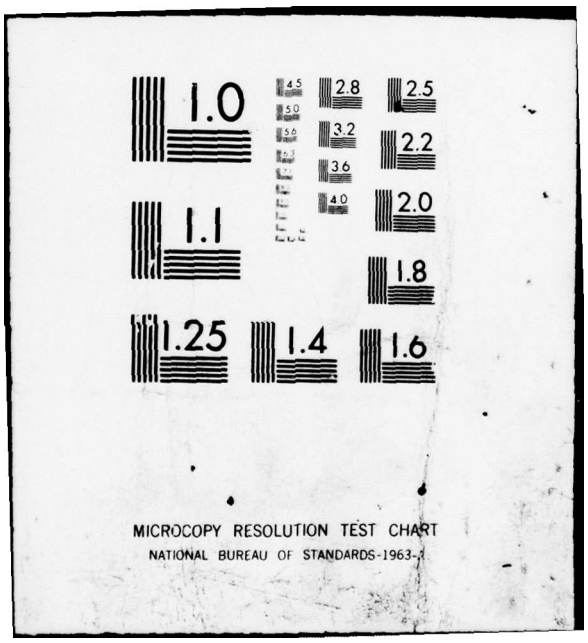
AD-A072 002 CONSTRUCTION ENGINEERING RESEARCH LAB (ARMY) CHAMPAIGN IL F/G 13/2
TRUE-INTEGRATING ENVIRONMENTAL NOISE MONITOR AND SOUND EXPOSURE--ETC(U)
JUN 79 A J AVERBUCH, P D SCHOMER

UNCLASSIFIED CERL-TR-N-41-VOL-2 NL

2 OF 2
AD A072002



END
DATE FILMED
8-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Board No. 22

Pin	Signal Name	Origin	
	CHANNEL 1 FILTER OUT	1φU	F.P. CH1 FILTEROUT BNC
	CHANNEL 1 FILTER IN	1φD	F.P. CH1 INPUT BNC
	CHANNEL 2 FILTER IN	1αD	F.P. CH2 INPUT BNC
	CHANNEL 2 FILTER OUT	1αU	F.P. CH2 FILTER OUT BNC
	Headphone Amp OUT +	*	F.P. HEADPHONE BNC
	Headphone Amp OUT -	*	F.P. HEADPHONE BNC
	12 V	P.S.	F.P.
	Ground	P.S.	F.P.

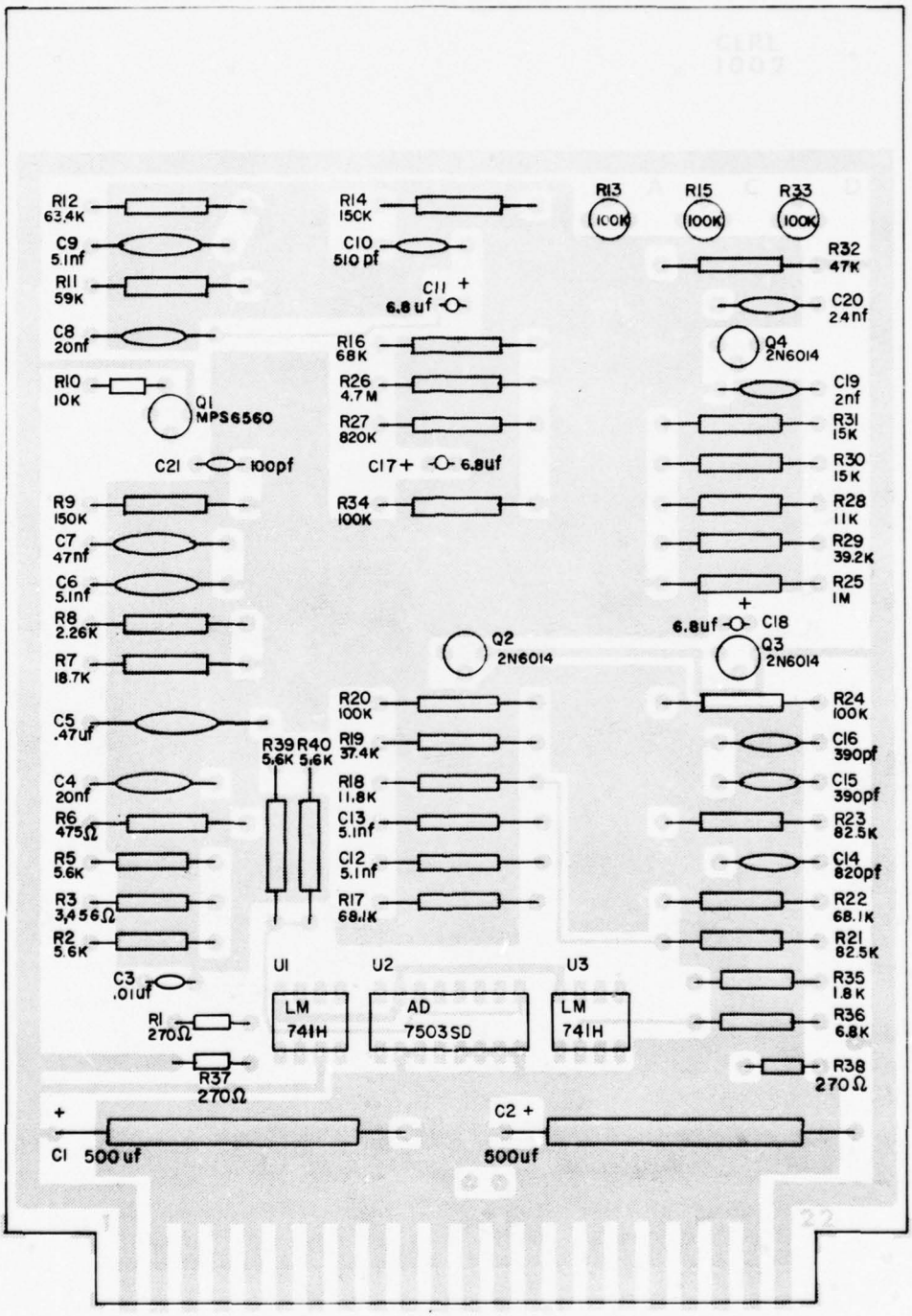
Table 4

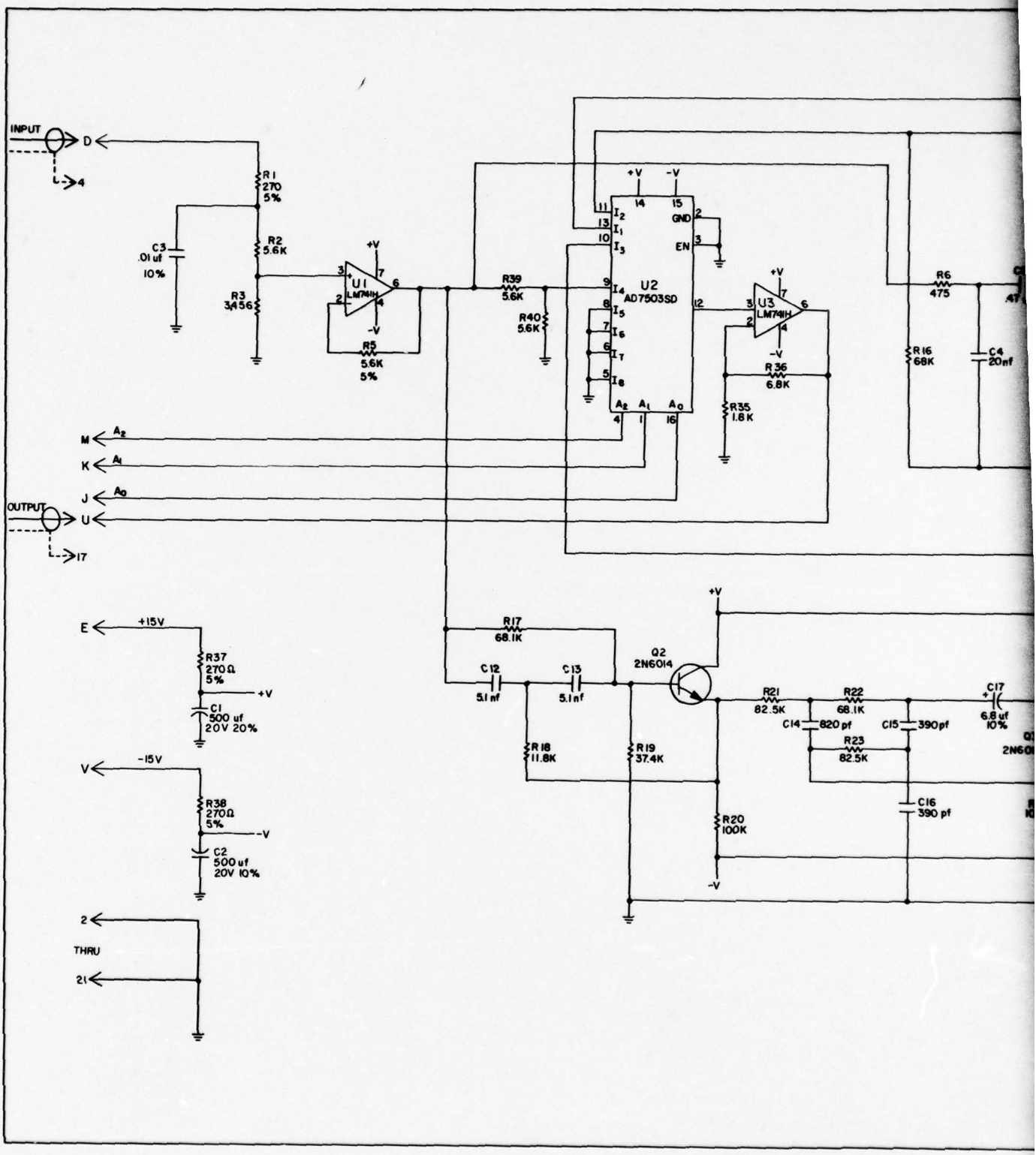
Board Number 1002 -- Parts List

Circuit Diagram Reference	Component Type			
R1, R37, R38	Carbon	1/4W	5%	270 Ω
R6	Carbon film		1%	475 Ω
R35	Carbon film		1%	1.8 K Ω
R8	Carbon film		1%	2.26K Ω
R3	Carbon film		1%	3456 Ω
R5	Carbon		5%	5.6 K Ω
R2, R39, R40	Carbon film		1%	5.6 K Ω
R36	Carbon film		1%	6.8 K Ω
R10	Carbon		5%	10 K Ω
R28	Carbon film		1%	11 K Ω
R18	Carbon film		1%	11.8 K Ω
R30, R31	Carbon film		1%	15 K Ω
R7	Carbon film		1%	18.7 K Ω
R19	Carbon film		1%	37.4 K Ω
R29	Carbon film		1%	39.2 K Ω
R32	Carbon film		1%	47 K Ω
R11	Carbon film		1%	59 K Ω
R12	Carbon film		1%	63.4 K Ω
R16	Carbon film		1%	68 K Ω
R17, R22	Carbon film		1%	68.1 K Ω
R21, R23	Carbon film		1%	82.5 K Ω
R20, R24, R34	Carbon film		1%	100 K Ω
R9, R14	Carbon film		1%	150 K Ω
R27	Carbon film		1%	820 K Ω
R25	Carbon film		1%	1 M Ω
R26	Carbon film	1/2W	1%	4.7 M Ω
R13, R15, R33	Trimmer	Cermet		100 K Ω
C21	Ceramic	100 pF		1 K V
C15, C16	Polystyrene	390 pF		63 V
C10	Polystyrene	510 pF		125 V
C14	Polystyrene	820 pF		63 V
C19	Polystyrene	2 nF		63 V
C20	Polystyrene	2.4 nF		63 V
C6, C9, C12, C13	Polystyrene	5.1 nF		63 V
C3	Ceramic	.01 nF		100 V

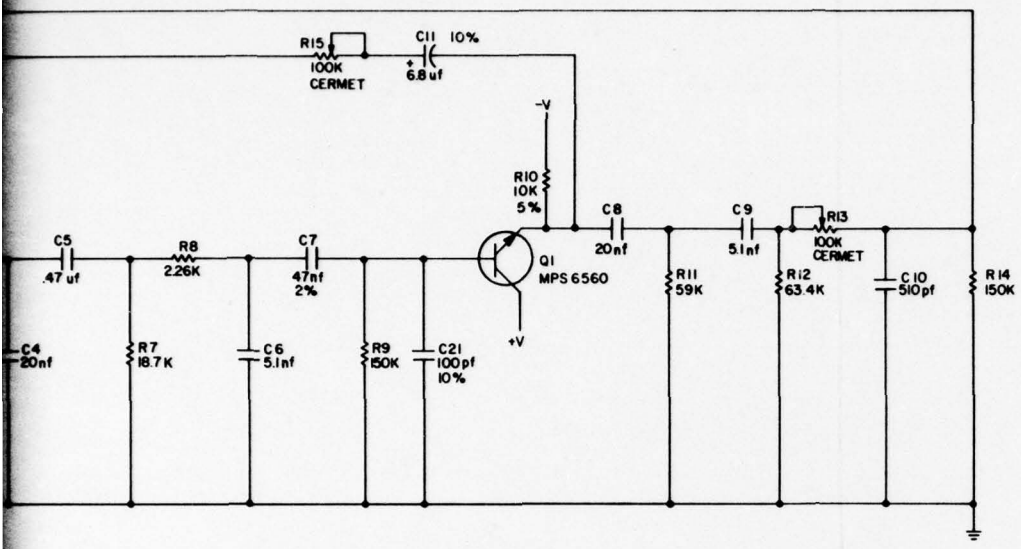
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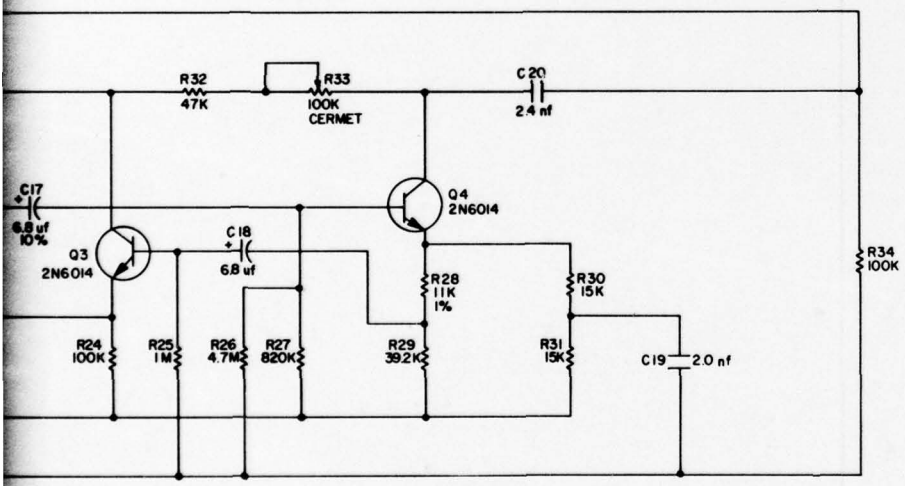
Circuit Diagram Reference	Component Type			
C4, C8	Polystyrene	20 nF	63	V
C7	Polystyrene	.047 uF	160	V
C5	Polystyrene	.47 uF	63	V
C11, C17, C18	Tantalum	6.8 uF	6	V
C1, C2	Aluminum Electrolytic	500 uF	25	V
Q1	Si Trans	NPN	MPS 6560	
Q2, Q3, Q4	Si Trans	NPN	2N6014	
U1, U3	LM741H			
U2	AD7503SD			


R12 63.4K
C9 5.1nf
R11 59K
C8 20nf
R10 10K
Q1 MPS6560
C21 100pf
R9 150K
C7 47nf
C6 5.1nf
R8 2.26K
R7 18.7K
C5 .47uf
C4 20nf
R6 475Ω
R5 5.6K
R3 3,456Ω
R2 5.6K
C3 .01uf
R1 270Ω
R37 270Ω
C1 + 500uf
R14 15CK
C10 510 pf
C11 + 6.8uf
R16 68K
R26 4.7M
R27 820K
C17 + 6.8uf
R34 100K
Q2 2N6014
R20 100K
R19 37.4K
R39 5.6K
R40 5.6K
R18 11.8K
C13 5.1nf
C12 5.1nf
R17 68.1K
U1
U2
U3
LM 741H
AD 7503SD
LM 741H
R13 100K
R15 100K
R33 100K
R32 47K
C20 24nf
Q4 2N6014
C19 2nf
R31 15K
R30 15K
R28 11K
R29 39.2K
R25 1M
+ 6.8uf C18
Q3 2N6014
R24 100K
C16 390pf
C15 390pf
R23 82.5K
C14 820pf
R22 68.1K
R21 82.5K
R35 1.8K
R36 6.8K
R38 270Ω
C2 + 500uf


INPUT
D
4
R1
270
5%
C3
.01 uf
10%
R2
5.6K
R3
3.456
U1
LM741H
+V
-V
R5
5.6K
5%
R39
5.6K
R40
5.6K
U2
AD7503SD
+V
-V
14
15
GND
EN
U3
LM741H
R36
6.8K
R35
1.8K
R6
475
R16
68K
C4
20nf
M
K
J
A2
A1
A0
OUTPUT
U
17
E
+15V
R37
270Ω
5%
C1
500 uf
20V 20%
V
-15V
R38
270Ω
5%
C2
500 uf
20V 10%
2
THRU
21
R17
68.1K
C12
5.1nf
C13
5.1nf
Q2
2N6014
R18
11.8K
R19
37.4K
R20
100K
R21
82.5K
R22
68.1K
C14
820 pf
C15
390pf
R23
82.5K
C16
390 pf
C17
6.8 uf
10%

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL





ALL RESISTORS 1% UNLESS OTHERWISE SPECIFIED

ALL CAPACITORS 1% UNLESS OTHERWISE SPECIFIED

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES

DRAWN R.W.W. 4/8/77
CHECKED M.W.W. 3/13/78
APPROVED A.J.A. 8/15/78
TRACED
DATE

DIAGRAM, SCHEMATIC P.C. BOARD

SCALE

DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

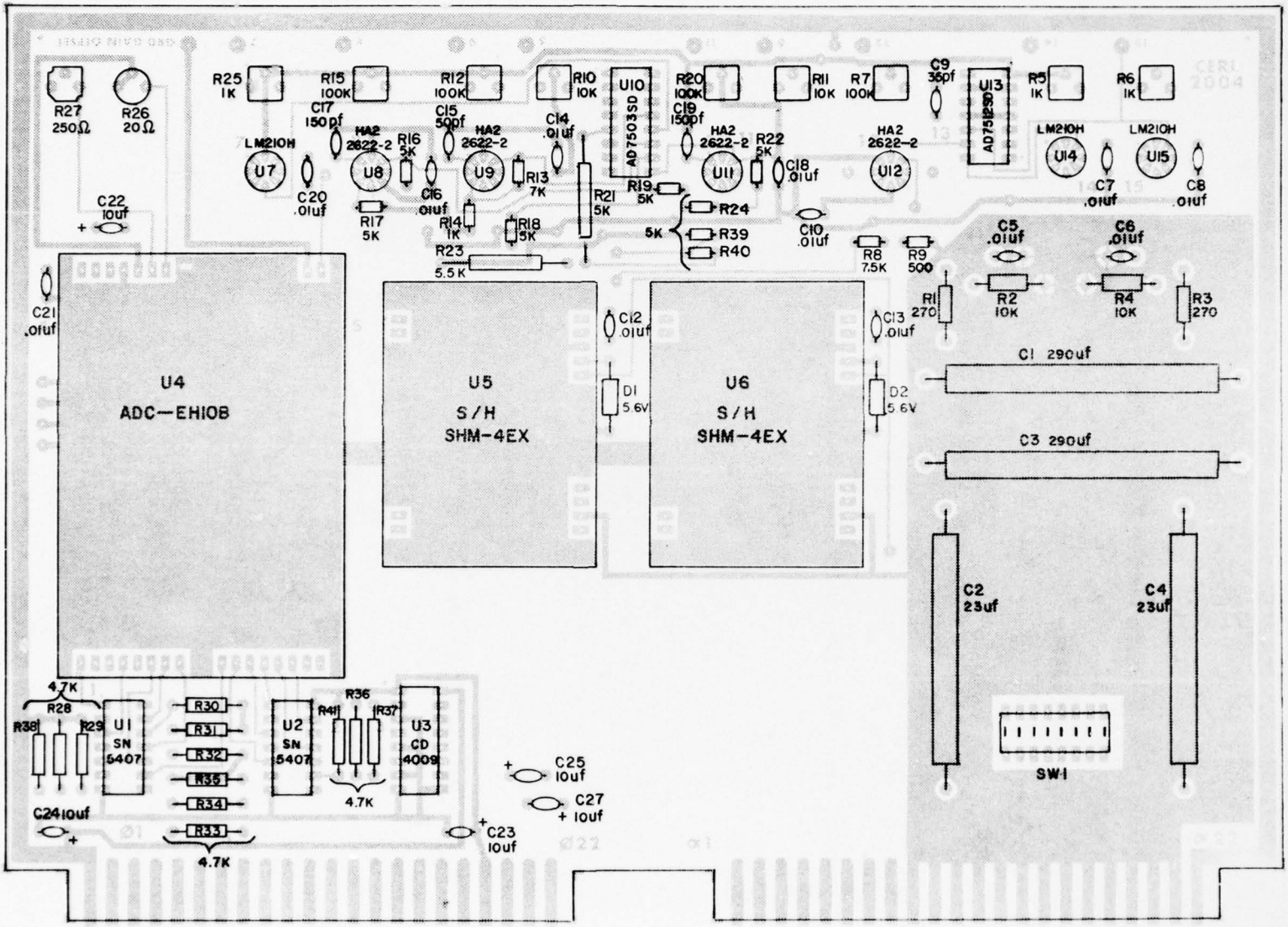
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1002

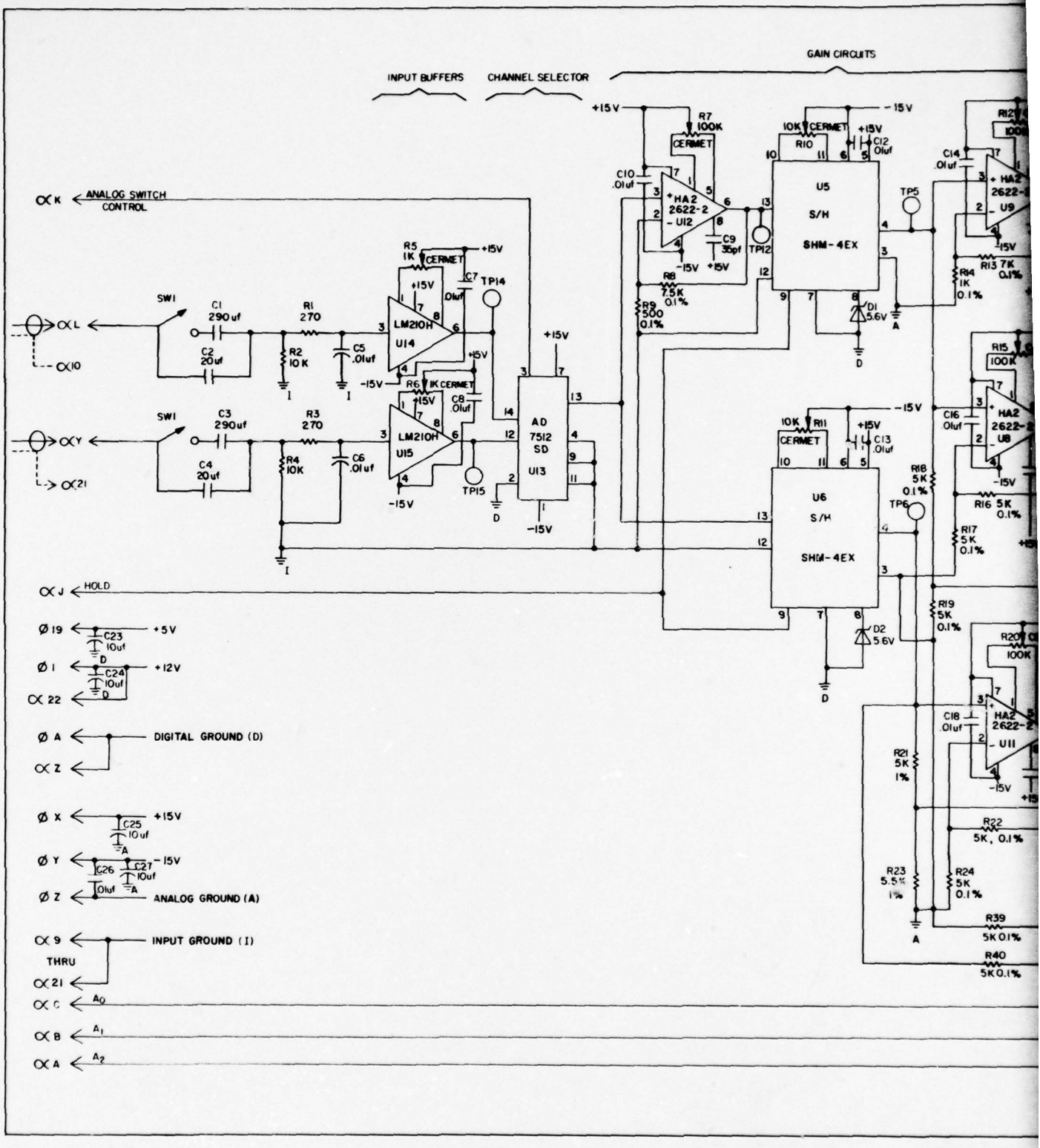
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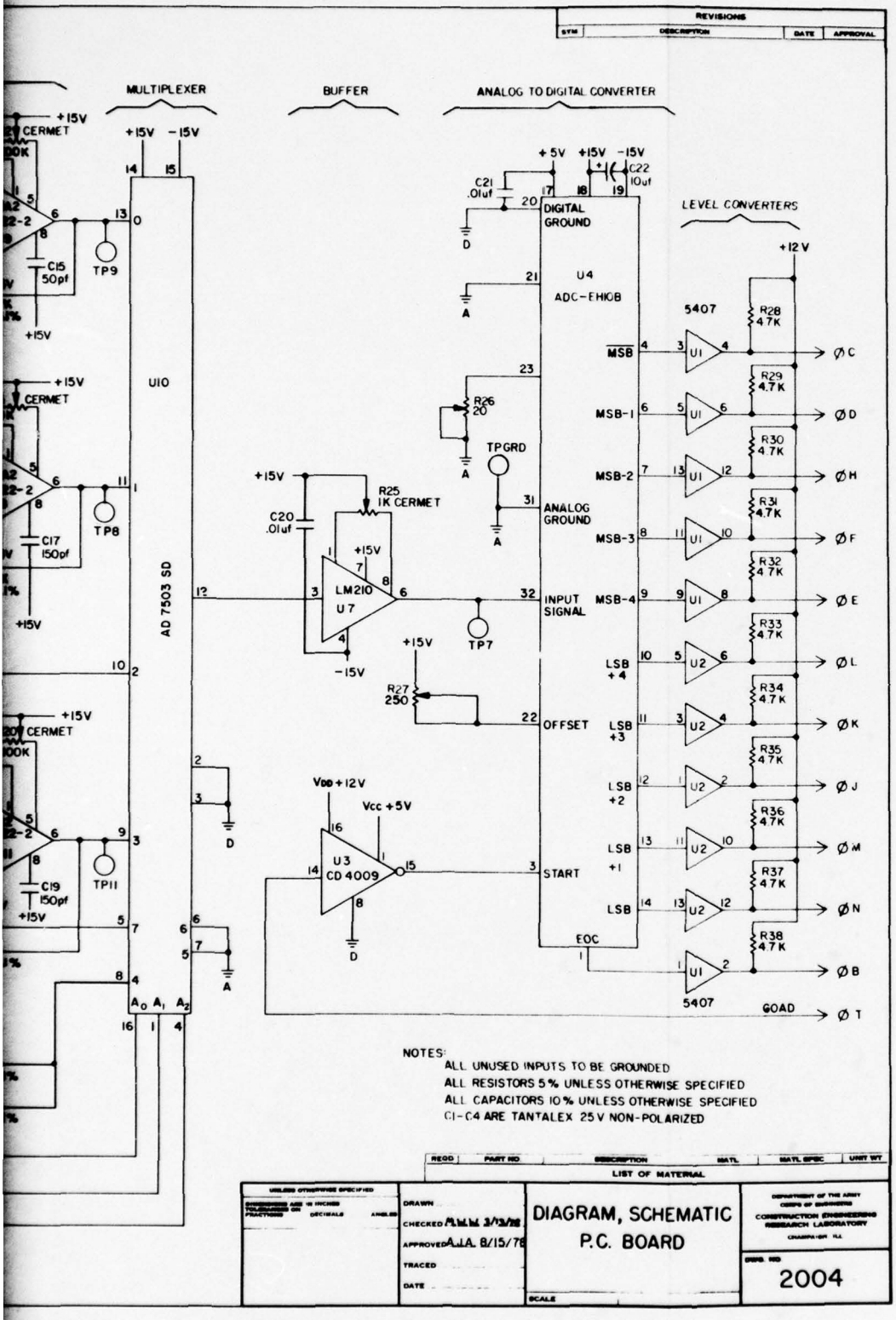
Table 5

Board Number 2004 -- Parts List

Circuit Diagram Reference	Component Type				
R1, R3	Carbon	1/4W	5%	270	Ω
R9	Bulk metal film	0.3W	0.1%	500	Ω
					Ω
R14	Bulk metal film	0.3W	0.1%	1	K Ω
R28-R38, R41	Carbon	1/4W	5%	4.7	K Ω
R21	Carbon film		1%	5	K Ω
R16-R19, R22, R24, R39, R40	Bulk metal	0.3W	0.1%	5	K Ω
R23	Carbon film	1/4W	1%	5.5	K Ω
R13	Bulk metal	0.3W	0.1%	7	K Ω
R8				7.5	K Ω
R2, R4	Carbon	1/4W	5%	10	K Ω
R26	Trimmer	Cermet		20	Ω
R27	Trimmer	Cermet		250	Ω
R5, R6, R25	Trimmer	Cermet		1	K Ω
R10, R11	Trimmer	Cermet		10	K Ω
R7, R12, R15, R20	Trimmer	Cermet		100	K Ω
C9	Ceramic	35 pF		1	K V
C15	Ceramic	50 pF			
C17, C19	Ceramic	150 pF			
C5-C8, C10, C12-C14, C16, C18 C20, C21, C26	Ceramic	.01 uF		100	V
C22-C25, C27	Tantalum	10 uF		35	V
C2, C4	Tantalum	20 uF	NP	25	V
C1, C3	Tantalum	290 uF	NP	25	V
D1, D2	Zener	1W		5.6	V
U1, U2	SN5407				
U3	CD4009				
U4	ADC-EH10B1-EX	A/D Converter			
U5, U6	SHM-4-EX	Sample and hold			
U7, U14, U15	LM210H				
U8, U9, U11, U12	HA2 2622-2				
U10	AD7503SD				
U13	AD7512SD				
SW1	Dip switch	8 station	SPST		


R27 250Ω
R26 20Ω
R25 1K
R15 100K
R12 100K
R10 10K
U10 AD7503SD
R20 100K
R11 10K
R7 100K
C9 36pf
U13 AD7528SD
R5 1K
R6 1K
LM210H U7
C17 150pf
HA2 2622-2 U8
R16 5K
C15 50pf
HA2 2622-2 U9
C14 .01uf
R13 7K
C19 150pf
HA2 2622-2 U11
R22 5K
C18 .01uf
HA2 2622-2 U12
LM210H U14
LM210H U15
C7 .01uf
C8 .01uf
C20 .01uf
C16 .01uf
R21 5K
R19 5K
R24
R39
R40
5K
C10 .01uf
C22 10uf
R17 5K
R14 1K
R18 5K
R23 5.5K
R8 7.5K
R9 500
C5 .01uf
C6 .01uf
C21 .01uf
U4 ADC—EH10B
U5 S/H SHM-4EX
U6 S/H SHM-4EX
C12 .01uf
D1 5.6V
D2 5.6V
C13 .01uf
R1 270
R2 10K
R4 10K
R3 270
C1 290uf
C3 290uf
C2 23uf
C4 23uf
SW1
4.7K
R28
R38
R29
U1 SN 5407
R30
R31
R32
R35
R34
R33
4.7K
U2 SN 5407
R36
R41
R37
4.7K
U3 CD 4009
C24 10uf
C25 10uf
C27 10uf
C23 10uf


INPUT BUFFERS
CHANNEL SELECTOR
GAIN CIRCUITS
ANALOG SWITCH CONTROL
HOLD
DIGITAL GROUND (D)
ANALOG GROUND (A)
INPUT GROUND (I)
THRU
+15V
-15V
+5V
+12V
SW1
C1 290uf
C2 20uf
C3 290uf
C4 20uf
R1 270
R2 10K
R3 270
R4 10K
C5 .01uf
C6 .01uf
LM210H U14
LM210H U15
R5 1K CERMET
R6 1K CERMET
C7 .01uf
C8 .01uf
TP14
TP15
AD 7512 SD U13
R7 100K CERMET
C10 .01uf
HA2 2622-2 U12
C9 35pf
TP12
U5 S/H SHM-4EX
R8 7.5K 0.1%
R9 500 0.1%
D1 5.6V
TP5
R10 10K CERMET
C12 .01uf
R11 10K CERMET
C13 .01uf
U6 S/H SHM-4EX
D2 5.6V
TP6
R18 5K 0.1%
R19 5K 0.1%
R21 5K 1%
R22 5K, 0.1%
R23 5.5K 1%
R24 5K 0.1%
R39 5K 0.1%
R40 5K 0.1%
R12 100K
C14 .01uf
HA2 2622-2 U9
R13 7K 0.1%
R14 1K 0.1%
R15 100K
C16 .01uf
HA2 2622-2 U8
R16 5K 0.1%
R17 5K 0.1%
R20 100K
C18 .01uf
HA2 2622-2 U11
C23 10uf
C24 10uf
C25 10uf
C26 .01uf
C27 10uf
αK
αL
αI0
αY
αY21
αJ
Ø19
Ø1
α22
ØA
αZ
ØX
ØY
ØZ
α9
THRU
α21
αC
αB
αA
A0
A1
A2



NOTES:

ALL UNUSED INPUTS TO BE GROUNDED
ALL RESISTORS 5% UNLESS OTHERWISE SPECIFIED
ALL CAPACITORS 10% UNLESS OTHERWISE SPECIFIED
C1-C4 ARE TANTALEX 25V NON-POLARIZED

LIST OF MATERIAL

REQD	PART NO	DESCRIPTION	MATL	MATL SPEC	UNIT WT

UNLESS OTHERWISE SPECIFIED

DRAWN

CHECKED A.L.A. 3/13/78

APPROVED A.L.A. 8/15/78

TRACED

DATE

SCALE

DIAGRAM, SCHEMATIC
P.C. BOARD

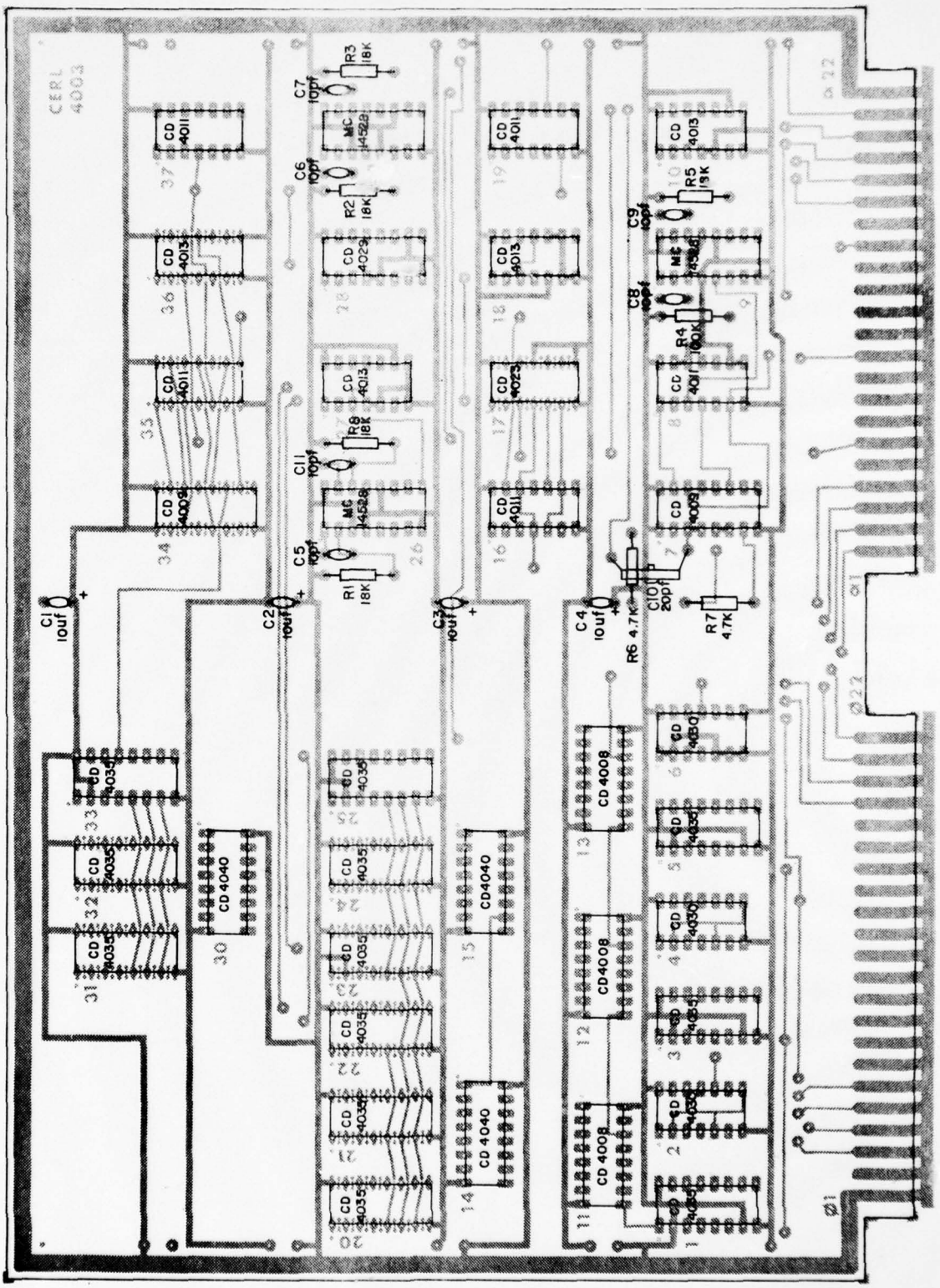
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

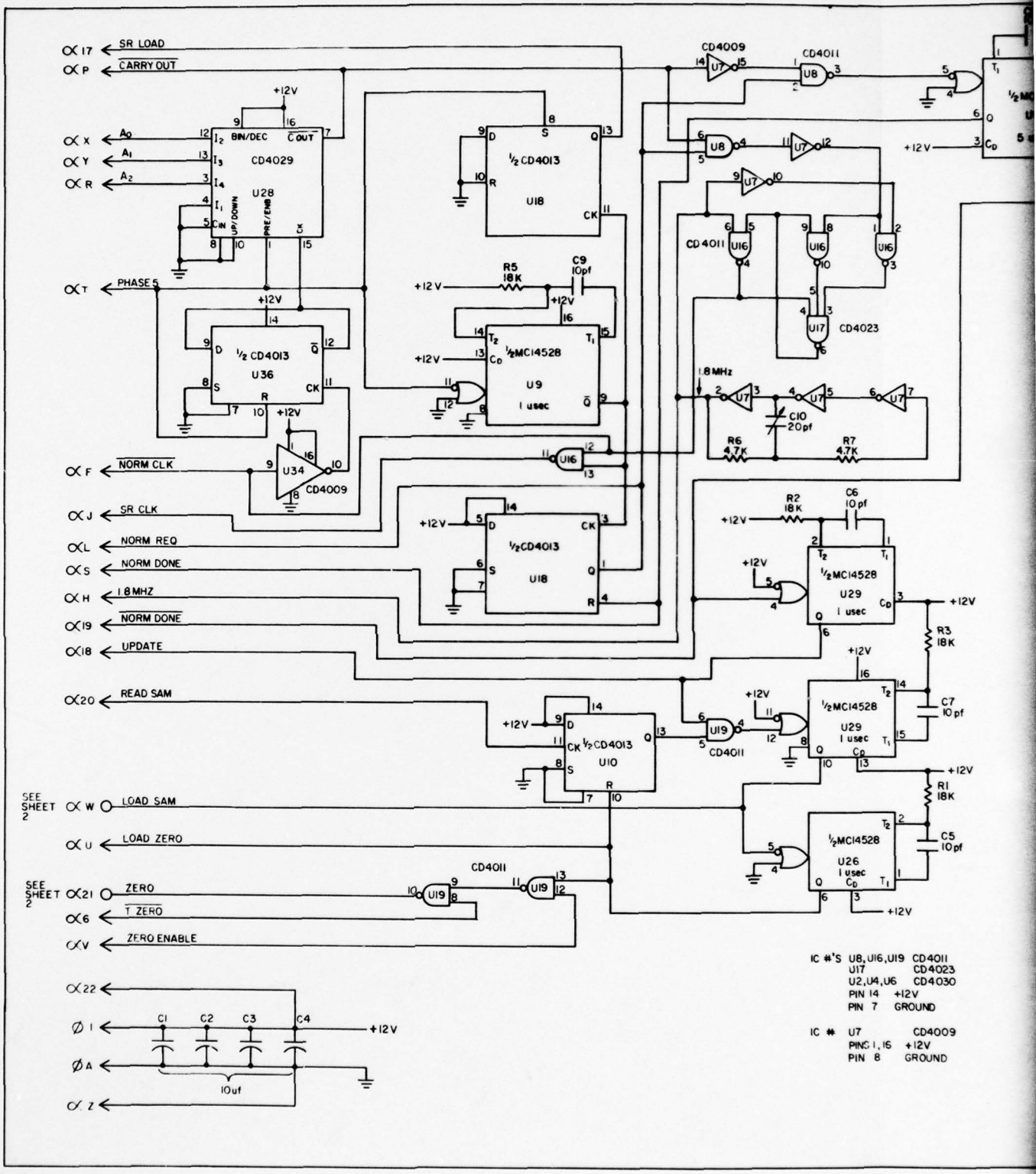
DRAWING NO.
2004

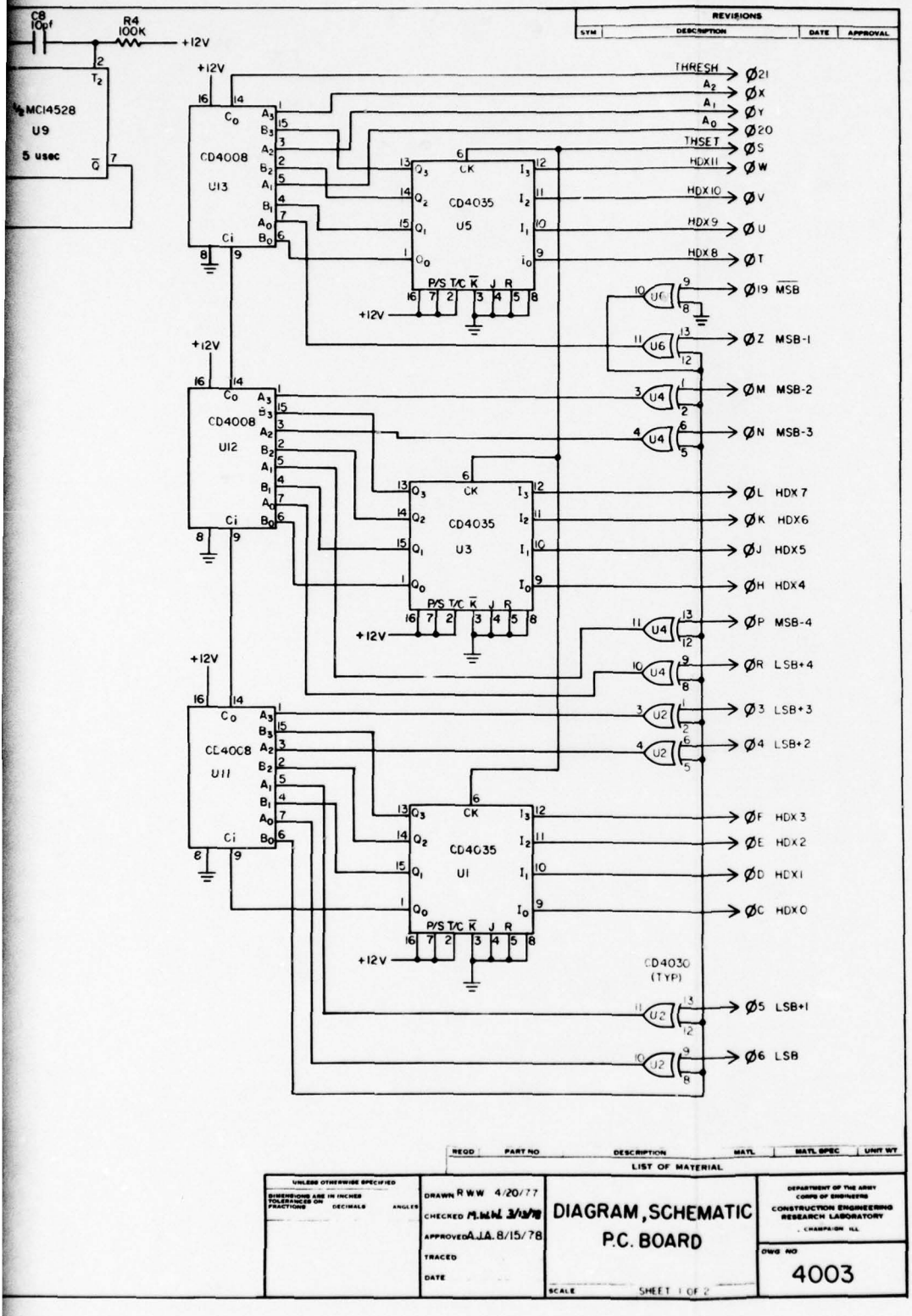
Table 6

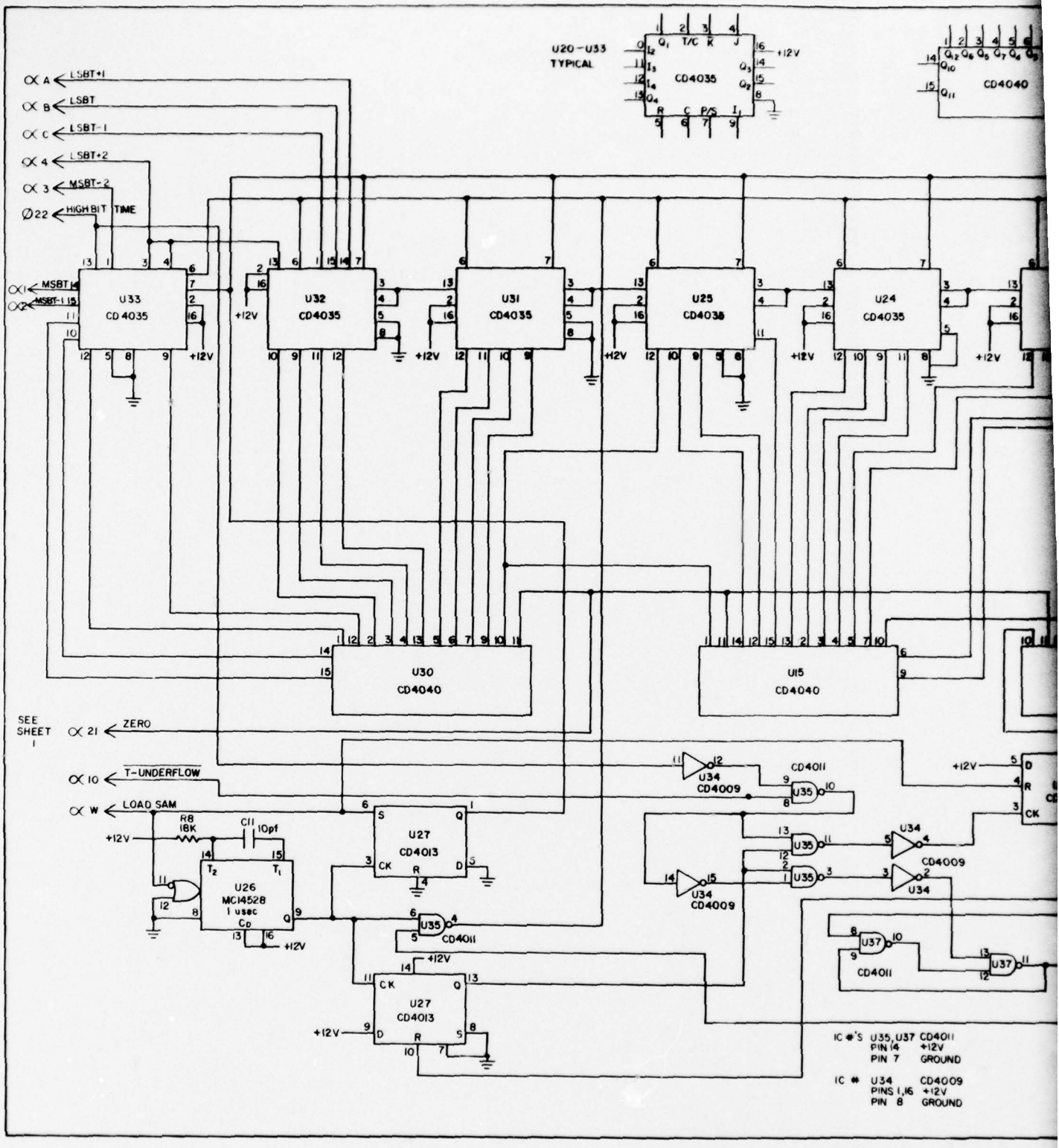
Board Number 4003 -- Parts List

Circuit Diagram Reference	Component Type				
R6, R7	Carbon	1/4W	5%	4.7	K Ω
R1, R2, R3, R5, R8	Carbon	1/4W	5%	18	K Ω
R4	Carbon	1/4W	5%	100	K Ω
C5-C9, C11	Mica	10 pF		500	V
C10	Trimmer	4-47 pF			
C1-C4	Tantalum	10 uF		35	V
U1, U3, U5, U20-U25, U31-U33	CD4035				
U2, U4, U6	CD4030				
U7, U34	CD4009				
U8, U16, U19, U35, U37	CD4011				
U9, U26, U29	MC14528				
U10, U18, U27, U36	CD4013				
U11, U12, U13	CD4008				
U14, U15, U30	CD4040				
U17	CD4023				
U28	CD4029				


CERL
4003
C1 10uf
C2 10uf
C3 10uf
C4 10uf
C5 10pf
C6 10pf
C7 10pf
C8 20pf
C9 20pf
C10 20pf
C11 10pf
R1 18K
R2 18K
R3 18K
R4 100K
R5 15K
R6 4.7K
R7 4.7K
R8 18K
CD 4011
CD 4013
CD 4029
CD 4023
CD 4008
CD 4030
CD 4035
CD 4040
MC 14528
Ø1
Ø2


SR LOAD
CARRY OUT
+12V
A0
A1
A2
BIN/DEC
COUT
CD4029
U28
UP/DOWN
PRE/ENB
CIN
CK
PHASE 5
½ CD4013
U36
R
S
CD4009
U34
NORM CLK
SR CLK
NORM REQ
NORM DONE
1.8MHZ
NORM DONE
UPDATE
READ SAM
LOAD SAM
LOAD ZERO
ZERO
T ZERO
ZERO ENABLE
SEE SHEET 2
½ CD4013
U18
½ CD4013
U10
½MC14528
U9
1 usec
R5 18K
C9 10pf
CD4011
U8
U7
U16
CD4023
U17
1.8MHz
C10 20pf
R6 4.7K
R7 4.7K
U19
R2 18K
C6 10pf
½MC14528
U29
1 usec
R3 18K
C7 10pf
R1 18K
C5 10pf
U26
C1
C2
C3
C4
10uf
IC #'S U8, U16, U19 CD4011
U17 CD4023
U2, U4, U6 CD4030
PIN 14 +12V
PIN 7 GROUND
IC # U7 CD4009
PINS 1, 16 +12V
PIN 8 GROUND


C8
100pf
R4
100K
+12V
½MC14528
U9
5 usec
T2
Q̄
REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
CD4008
U13
U12
U11
CD4035
U5
U3
U1
P/S T/C K̄ J R
THRESH
THSET
HDX11
HDX10
HDX9
HDX8
HDX7
HDX6
HDX5
HDX4
HDX3
HDX2
HDX1
HDX0
MSB
MSB-1
MSB-2
MSB-3
MSB-4
LSB+4
LSB+3
LSB+2
LSB+1
LSB
CD4030
(TYP)
REQD
PART NO
DESCRIPTION
MATL
MATL SPEC
UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS
DECIMALS
ANGLES
DRAWN R W W 4/20/77
CHECKED
APPROVED A.J.A. 8/15/78
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
SHEET 1 OF 2
DEPARTMENT OF THE ARMY
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CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN ILL.
DWG NO
4003


U20–U33
TYPICAL
CD4035
CD4040
∝ A LSBT+1
∝ B LSBT
∝ C LSBT-1
∝ 4 LSBT+2
∝ 3 MSBT-2
Ø22 HIGH BIT TIME
∝1 MSBT
∝2 MSBT-1
U33
CD4035
U32
CD4035
U31
CD4035
U25
CD4038
U24
CD4035
+12V
U30
CD4040
U15
CD4040
SEE SHEET 1
∝ 21 ZERO
∝ 10 T-UNDERFLOW
∝ W LOAD SAM
R8
18K
C11
10pf
U26
MC14528
1 usec
U27
CD4013
U34
CD4009
CD4011
U35
U37
IC #'S U35, U37 CD4011
PIN 14 +12V
PIN 7 GROUND
IC # U34 CD4009
PINS 1,16 +12V
PIN 8 GROUND

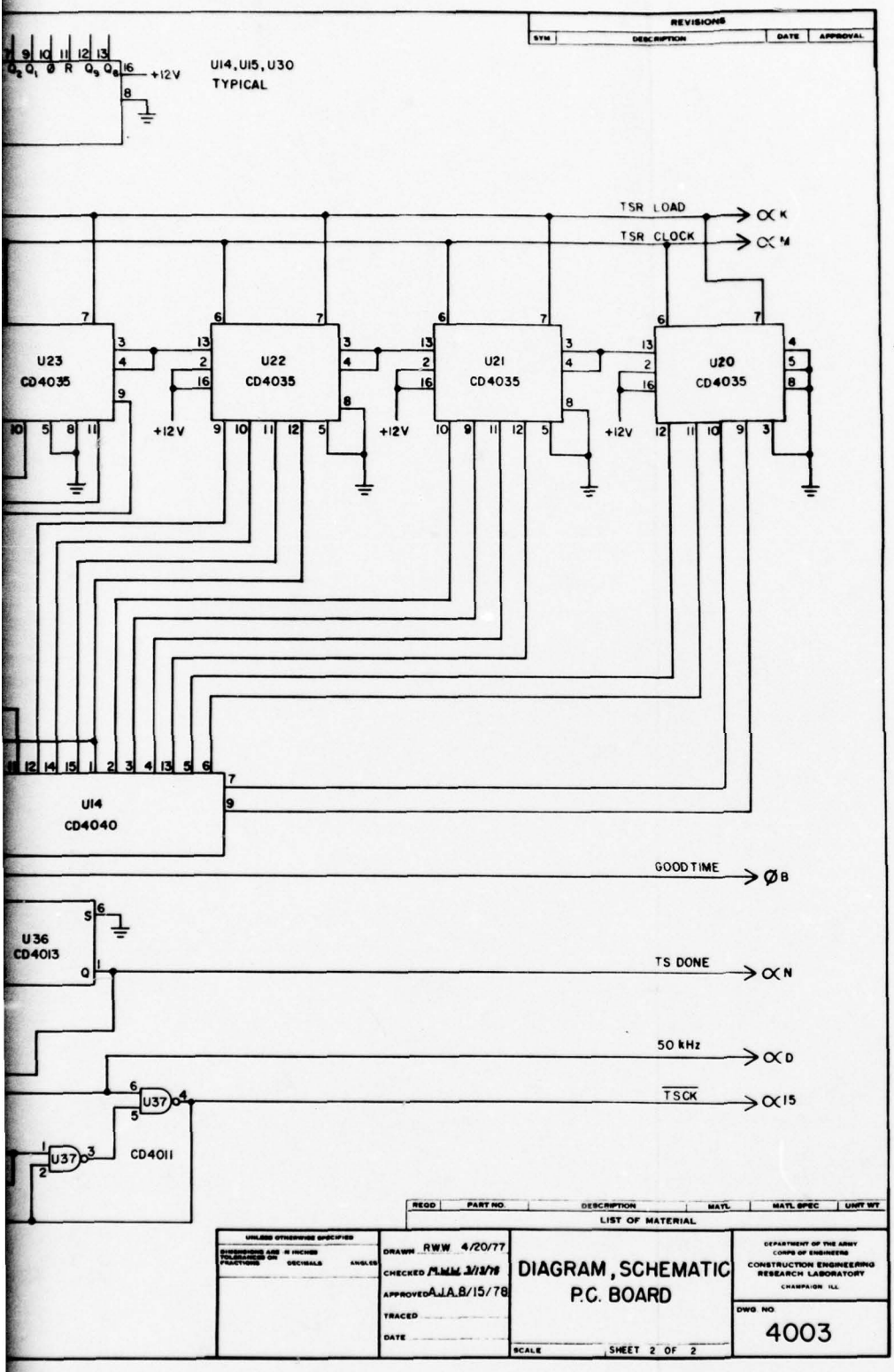
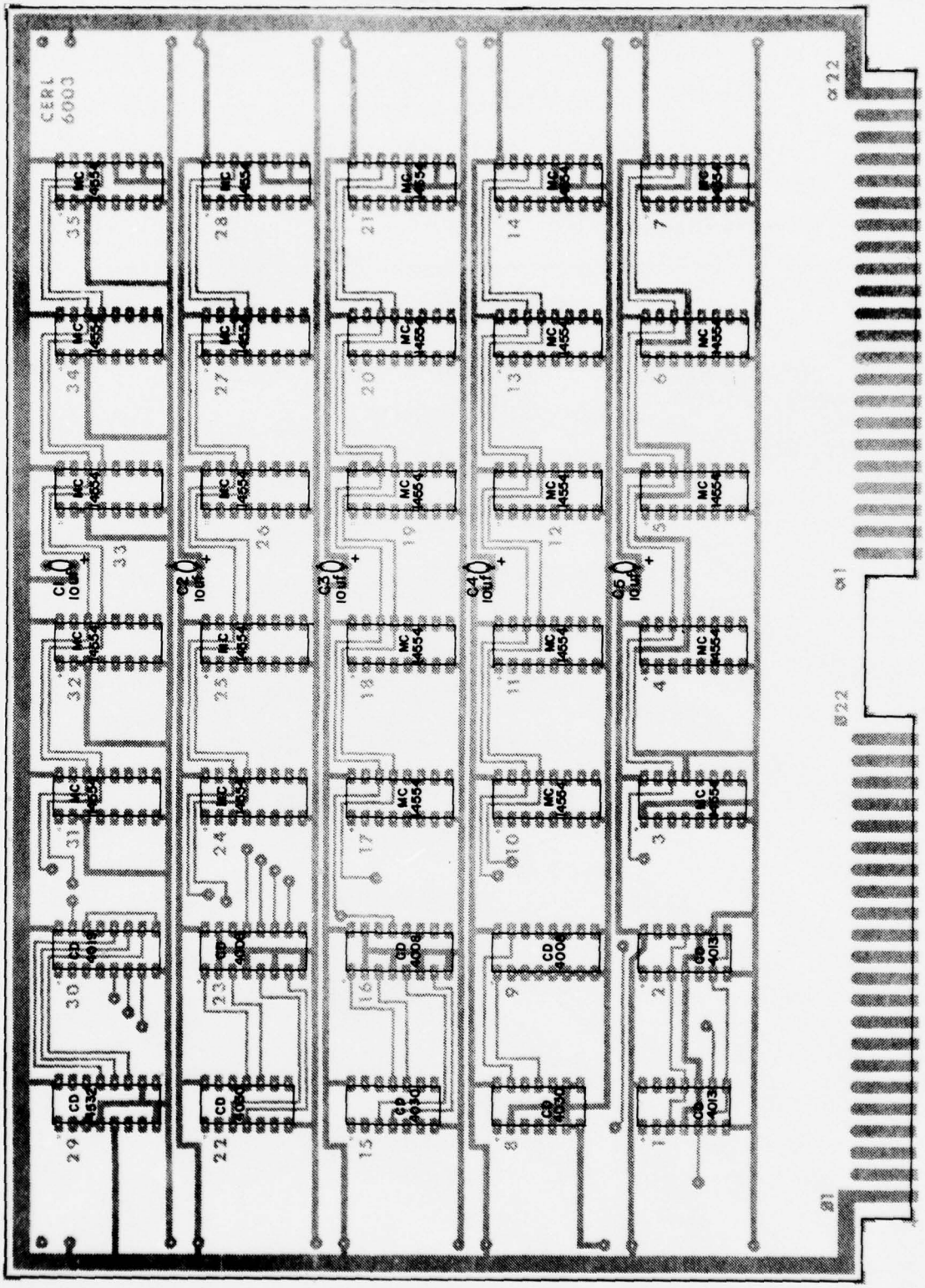
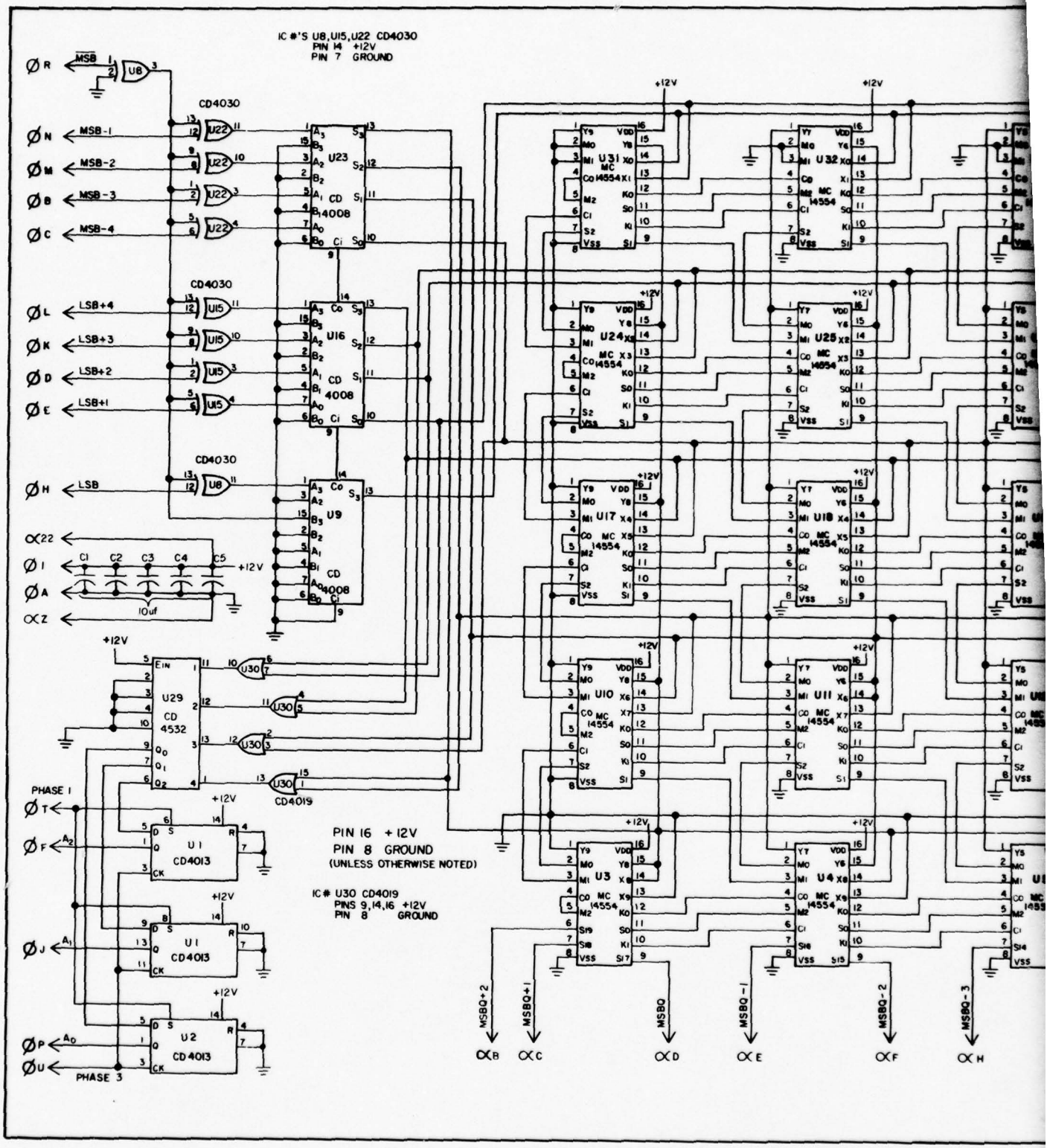

REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
U14, U15, U30
TYPICAL
+12V
TSR LOAD
TSR CLOCK
U23
CD4035
U22
CD4035
U21
CD4035
U20
CD4035
+12V
U14
CD4040
GOOD TIME
U36
CD4013
TS DONE
50 kHz
U37
CD4011
TSCK
REQD
PART NO.
DESCRIPTION
MATL
MATL SPEC
UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DRAWN RWW 4/20/77
CHECKED
APPROVED A.J.A. 8/15/78
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
SHEET 2 OF 2
DEPARTMENT OF THE ARMY
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CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN ILL.
DWG NO.
4003

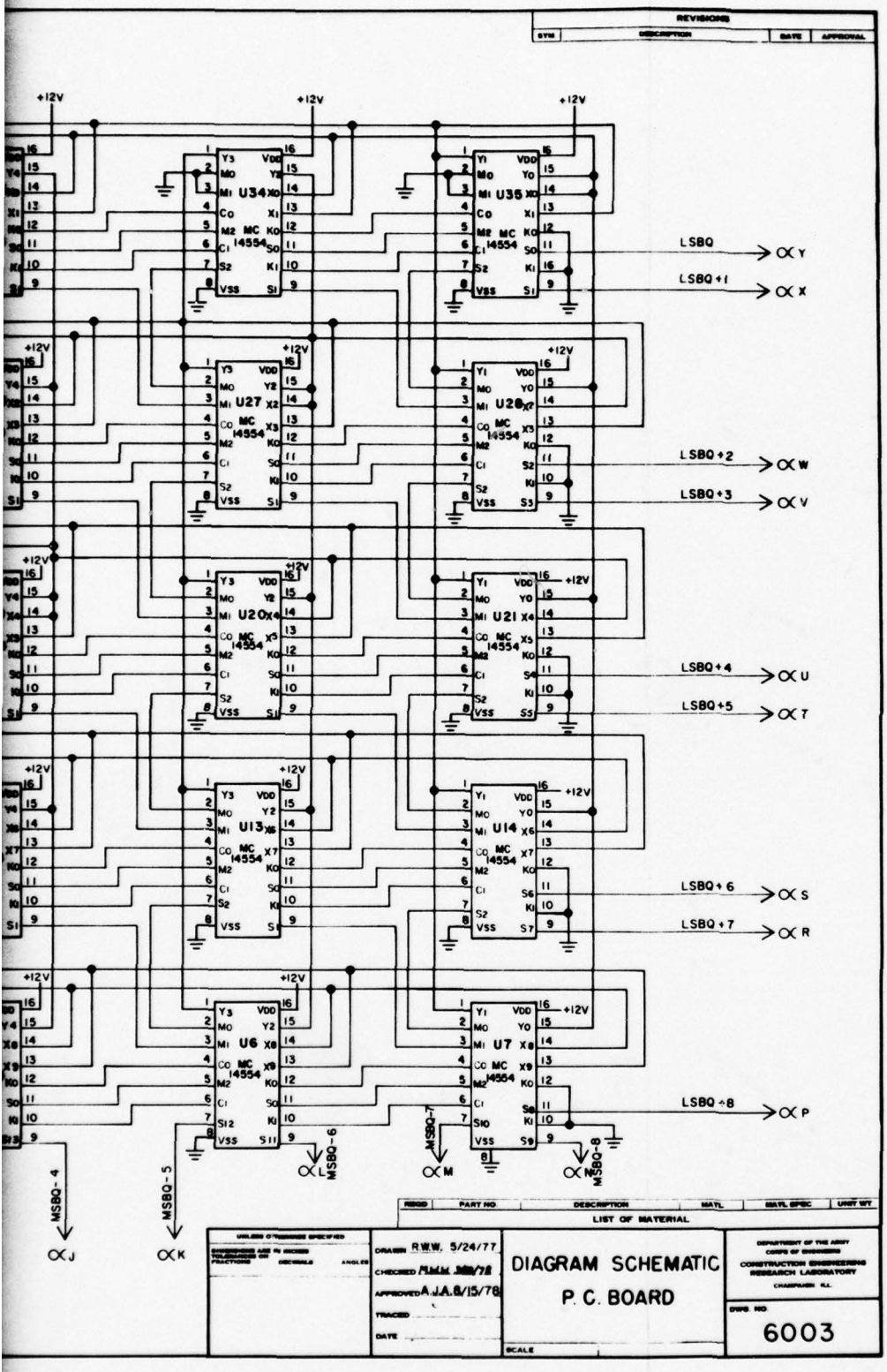
Table 7

Board Number 6003 -- Parts List

Circuit Diagram Reference	Component Type			
C1-C5	Tantalum	10 uF	35	V
U1, U2	CD 4013			
U3-U7, U10-U14, U17-U21	MC14554			
U24-U28, U31-U35	MC14554			
U8, U15, U22	CD4030			
U9, U16, U23	CD4008			
U29	CD4532			
U30	CD4019			


CERL
6003
MC 14554
CD 4008
CD 4013
C10 10uf
C20 10uf
C30 10uf
C40 10uf
C50 10uf
J22
J1


IC #'S U8, U15, U22 CD4030
PIN 14 +12V
PIN 7 GROUND
CD4030
MSB
MSB-1
MSB-2
MSB-3
MSB-4
LSB+4
LSB+3
LSB+2
LSB+1
LSB
U8
U22
U15
U23
U16
U9
CD 4008
+12V
C1 C2 C3 C4 C5
10uf
U29
CD 4532
U30
CD4019
PHASE 1
PHASE 3
U1
U2
CD4013
PIN 16 +12V
PIN 8 GROUND
(UNLESS OTHERWISE NOTED)
IC# U30 CD4019
PINS 9,14,16 +12V
PIN 8 GROUND
U31
U32
U24
U25
U17
U18
U10
U11
U3
U4
MC 14554
MSBQ+2
MSBQ+1
MSBQ
MSBQ-1
MSBQ-2
MSBQ-3


REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
+12V
U34
U35
U27
U28
U20
U21
U13
U14
U6
U7
14554
LSBQ
LSBQ+1
LSBQ+2
LSBQ+3
LSBQ+4
LSBQ+5
LSBQ+6
LSBQ+7
LSBQ+8
MSBQ-4
MSBQ-5
MSBQ-6
MSBQ-7
MSBQ-8
∝J
∝K
∝L
∝M
∝N
∝P
∝R
∝S
∝T
∝U
∝V
∝W
∝X
∝Y
REQD
PART NO.
DESCRIPTION
MATL
MATL SPEC
UNIT WT
LIST OF MATERIAL
DRAWN R.W.W. 5/24/77
CHECKED
APPROVED A.J.A. 8/15/78
TRACED
DATE
DIAGRAM SCHEMATIC
P. C. BOARD
SCALE
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN, ILL.
DWG NO.
6003

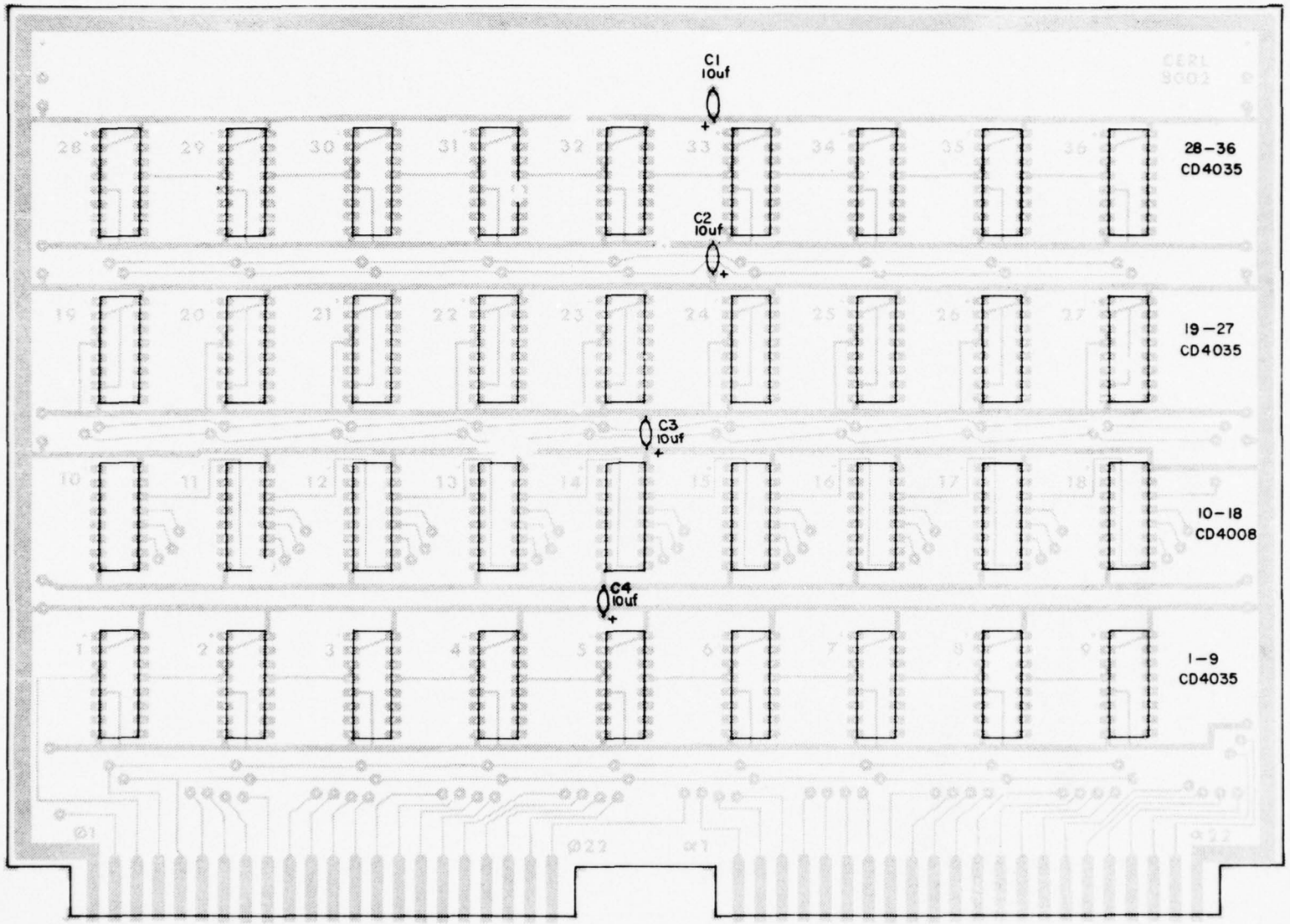
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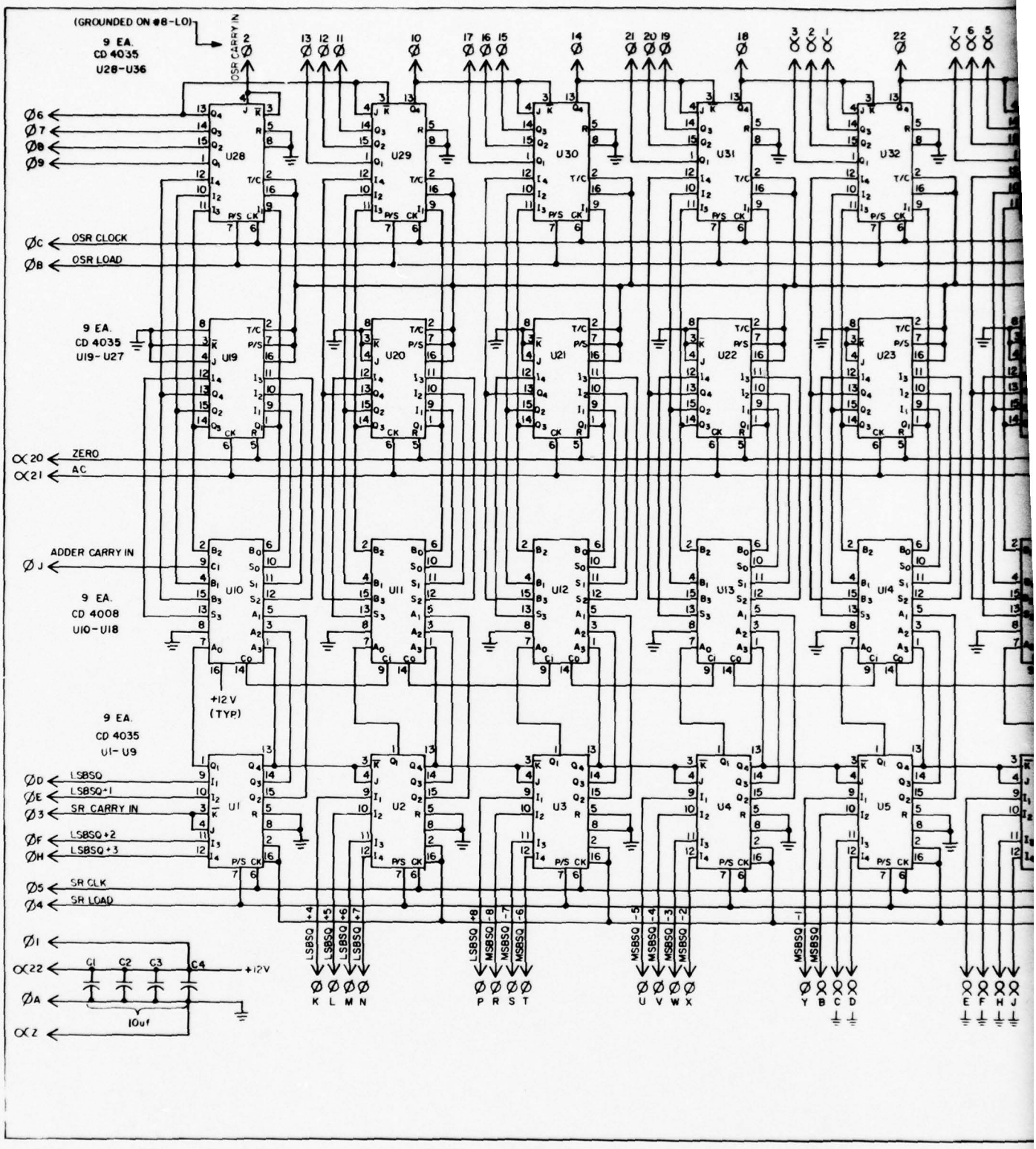
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Table 8

Board Number 8002 -- Parts List

Circuit Diagram Reference	Component Type			
C1-C4	Tantalum	10 uF	35	V
U1-U9, U19-U36	CD4035			
U10-U18	CD4008			


C1
10uf
C2
10uf
C3
10uf
C4
10uf
28-36
CD4035
19-27
CD4035
10-18
CD4008
1-9
CD4035


(GROUNDED ON #8-LO)
9 EA.
CD 4035
U28-U36
OSR CARRY IN
Ø6
Ø7
Ø8
Ø9
ØC
OSR CLOCK
ØB
OSR LOAD
9 EA.
CD 4035
U19-U27
∝20
ZERO
∝21
AC
ØJ
ADDER CARRY IN
9 EA.
CD 4008
U10-U18
+12 V
(TYP)
9 EA.
CD 4035
U1-U9
ØD
LSBSQ
ØE
LSBSQ+1
Ø3
SR CARRY IN
ØF
LSBSQ+2
ØH
LSBSQ+3
Ø5
SR CLK
Ø4
SR LOAD
Ø1
∝22
C1
C2
C3
C4
+12V
ØA
10uf
∝Z
LSBSQ +4
LSBSQ +5
LSBSQ +6
LSBSQ +7
Ø K L M N
LSBSQ +8
MSBSQ -8
MSBSQ -7
MSBSQ -6
Ø P R S T
MSBSQ -5
MSBSQ -4
MSBSQ -3
MSBSQ -2
Ø U V W X
MSBSQ -1
MSBSQ
Ø Y B C D
E F H J

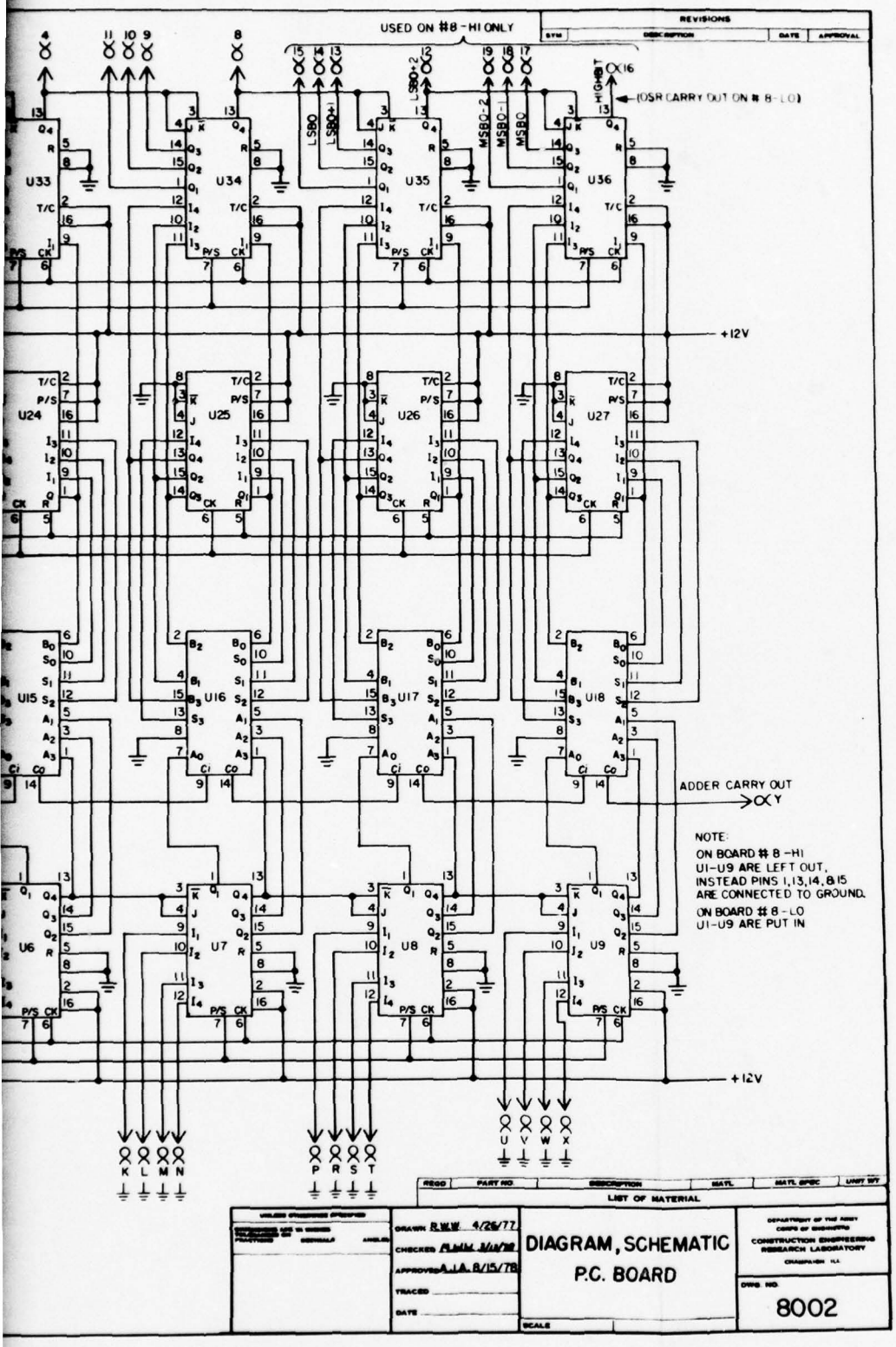
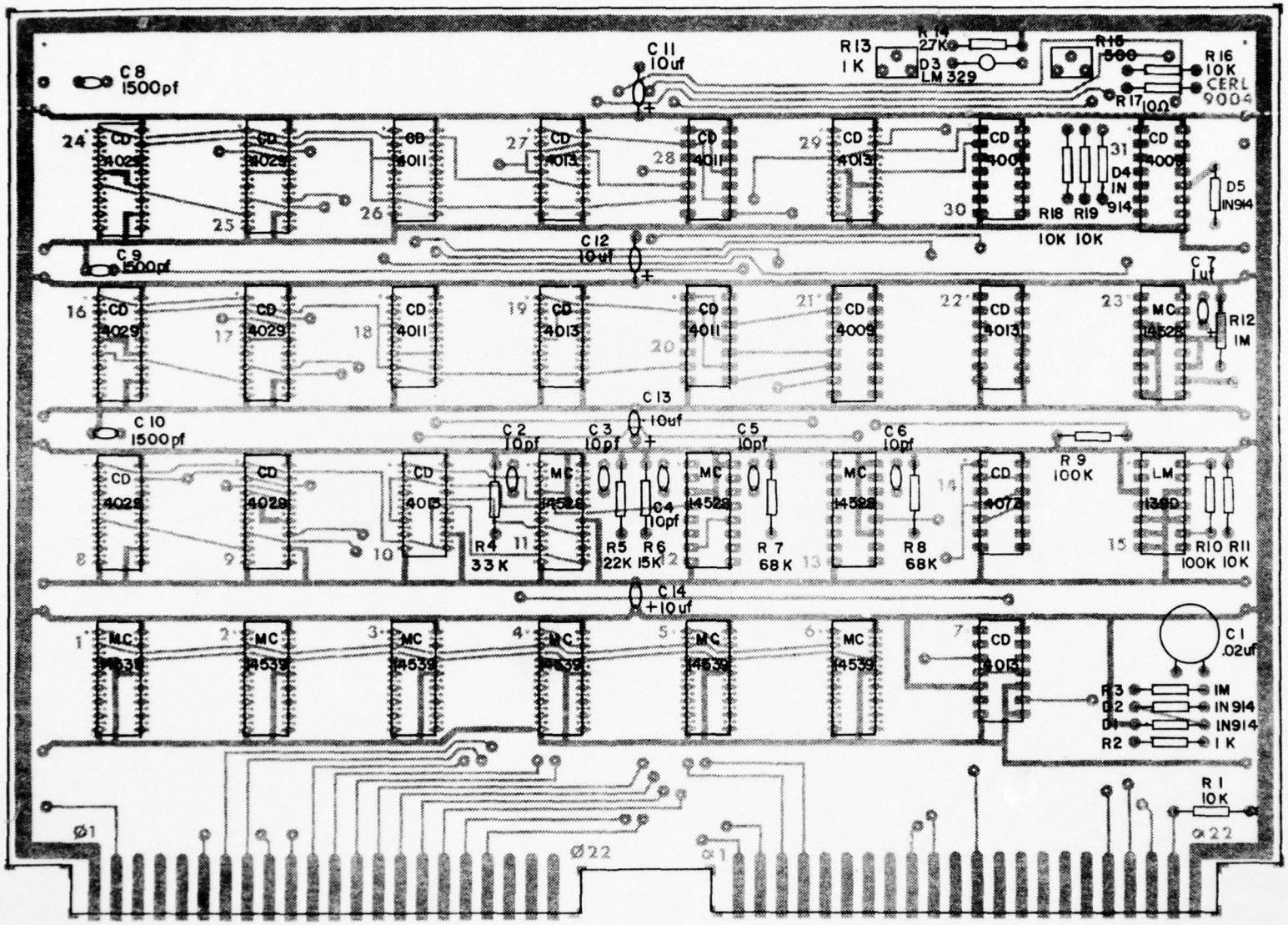

USED ON #8 - HI ONLY
REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
(OSR CARRY OUT ON # 8 - LO)
LSB0
LSB0+1
LSB0+2
MSB0-2
MSB0-1
MSB0
HIGHEST
+12V
ADDER CARRY OUT
NOTE:
ON BOARD # 8 - HI
U1-U9 ARE LEFT OUT,
INSTEAD PINS 1,13,14,8,15
ARE CONNECTED TO GROUND.
ON BOARD # 8 - LO
U1-U9 ARE PUT IN
K L M N
P R S T
U V W X
REQD
PART NO.
DESCRIPTION
MATL
MATL SPEC
UNIT QTY
LIST OF MATERIAL
DRAWN R.W.W. 4/26/77
CHECKED
APPROVED
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
DWG NO.
8002

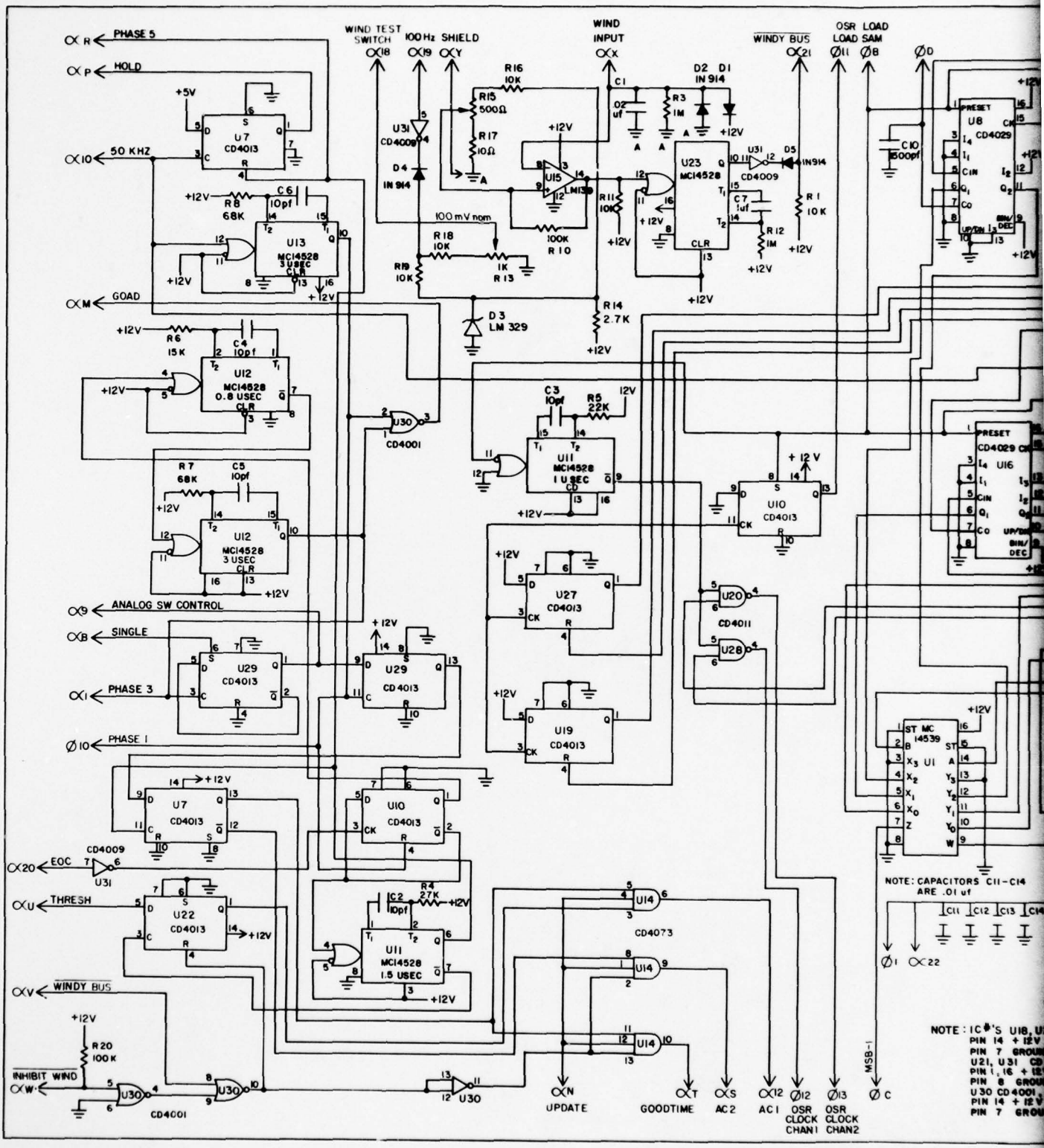
Table 9

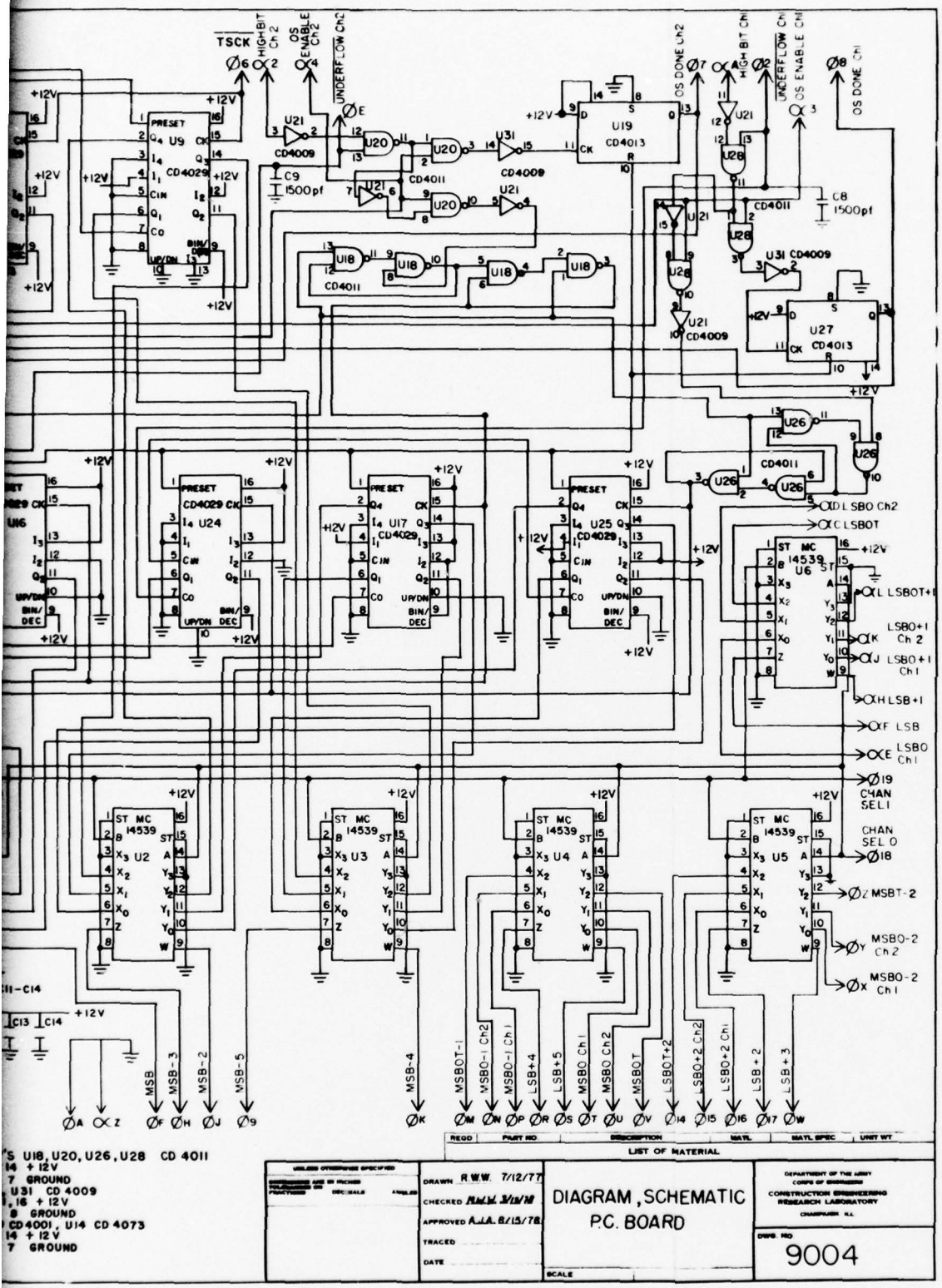
Board Number 9004 -- Parts List

Circuit Diagram Reference	Component Type			
R17	Carbon	1/4W	5%	10 Ω
R2	Carbon	1/4W	5%	1 K Ω
R14	Carbon	1/4W	5%	2.7 K Ω
R1, R11, R16, R18, R19	Carbon	1/4W	5%	
R6	Carbon	1/4W	5%	15 K Ω
R5	Carbon	1/4W	5%	22 K Ω
R4	Carbon	1/4W	5%	33 K Ω
R7, R8	Carbon	1/4W	5%	68 K Ω
R9, R10, R20	Carbon	1/4W	5%	100 K Ω
R3, R12	Carbon	1/4W	5%	1 M Ω
R15	Trimmer	Cermet		500 Ω
R13	Trimmer	Cermet		1 K Ω
C2-C6	Ceramic	10 pF		500 V
C8-C10	Ceramic	1500 pF		1 K V
C1	Ceramic	.02 uF		1 K V
C7	Tantalum	1 uF		35 V
C11-C14	Tantalum	10 uF		35 V
D1, D2, D4, D5	IN914B	Silicon Diode		
D3	LM329H	Zener 6.95V		
U1-U6	MC14539			
U7, U10, U19, U22, U27, U29	CD4013			
U8, U9, U16, U17, U24, U25	CD4029			
U11-U13, U23	MC14528			
U14	CD4073			
U15	LM139D			
U18, U20, U26, U28	CD4011			
U21, U31	CD4009			
U30	CD4001			



NOTE: C11–C14 ARE BYPASS CAPACITORS. R20 IS LOCATED ON REVERSE SIDE OF BOARD, 100 KΩ R9 IS USED TO TIE UNUSED INPUT INPUT OF U13 HIGH.


PHASE 5
HOLD
50 KHZ
GOAD
ANALOG SW CONTROL
SINGLE
PHASE 3
PHASE 1
EOC
THRESH
WINDY BUS
INHIBIT WIND
WIND TEST SWITCH
100 Hz SHIELD
WIND INPUT
WINDY BUS
OSR LOAD LOAD SAM
U7 CD4013
U8 CD4029
U10 CD4013
U11 MC14528 1 USEC
U12 MC14528 0.8 USEC
U12 MC14528 3 USEC
U13 MC14528 3 USEC CLR
U19 CD4013
U20 CD4011
U22 CD4013
U23 MC14528
U27 CD4013
U28 CD4011
U29 CD4013
U30 CD4001
U31 CD4009
U14 CD4073
ST MC 14539
D3 LM 329
D4 IN 914
D5 IN914
D2 D1 IN914
R15 500Ω
R16 10K
R17 10Ω
R18 10K
R19 10K
100K R10
1K R13
R14 2.7K
R1 10K
R3 1M
R4 27K
R5 22K
R6 15K
R7 68K
R8 68K
R11 10K
R12 1M
R20 100K
C1 .02 uf
C2 10pf
C3 10pf
C4 10pf
C5 10pf
C6 10pf
C7 1uf
C10 500pf
C11 C12 C13 C14
100 mV nom
+12V
+5V
NOTE: CAPACITORS C11-C14 ARE .01 uf
NOTE: IC #'S U18, U
PIN 14 + 12V
PIN 7 GROU
U21, U31 CD
PIN 1, 16 + 12
PIN 8 GROU
U30 CD 4001
PIN 14 + 12 V
PIN 7 GROU
MSB-1
UPDATE
GOODTIME
AC2
AC1
OSR CLOCK CHAN1
OSR CLOCK CHAN2



'S U18, U20, U26, U28 CD 4011
14 + 12V
7 GROUND
U31 CD 4009
16 + 12V
8 GROUND
CD4001, U14 CD 4073
14 + 12V
7 GROUND

REQD	PART NO	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

DRAWN R.W.W. 7/12/77
CHECKED R.W.W. 7/13/78
APPROVED A.J.A. 8/15/78
TRACED
DATE
SCALE

DIAGRAM, SCHEMATIC
P.C. BOARD

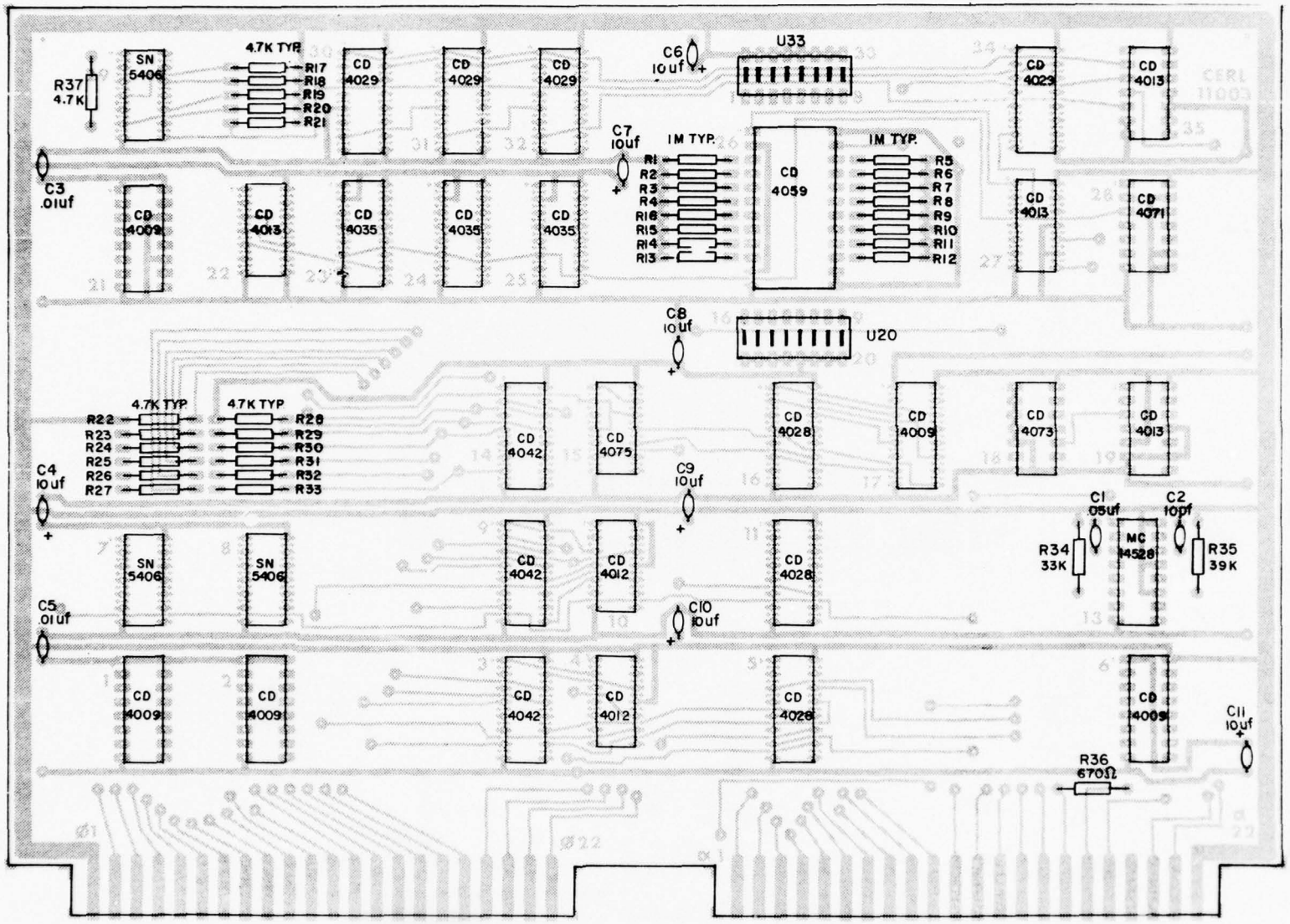
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

DWG NO
9004

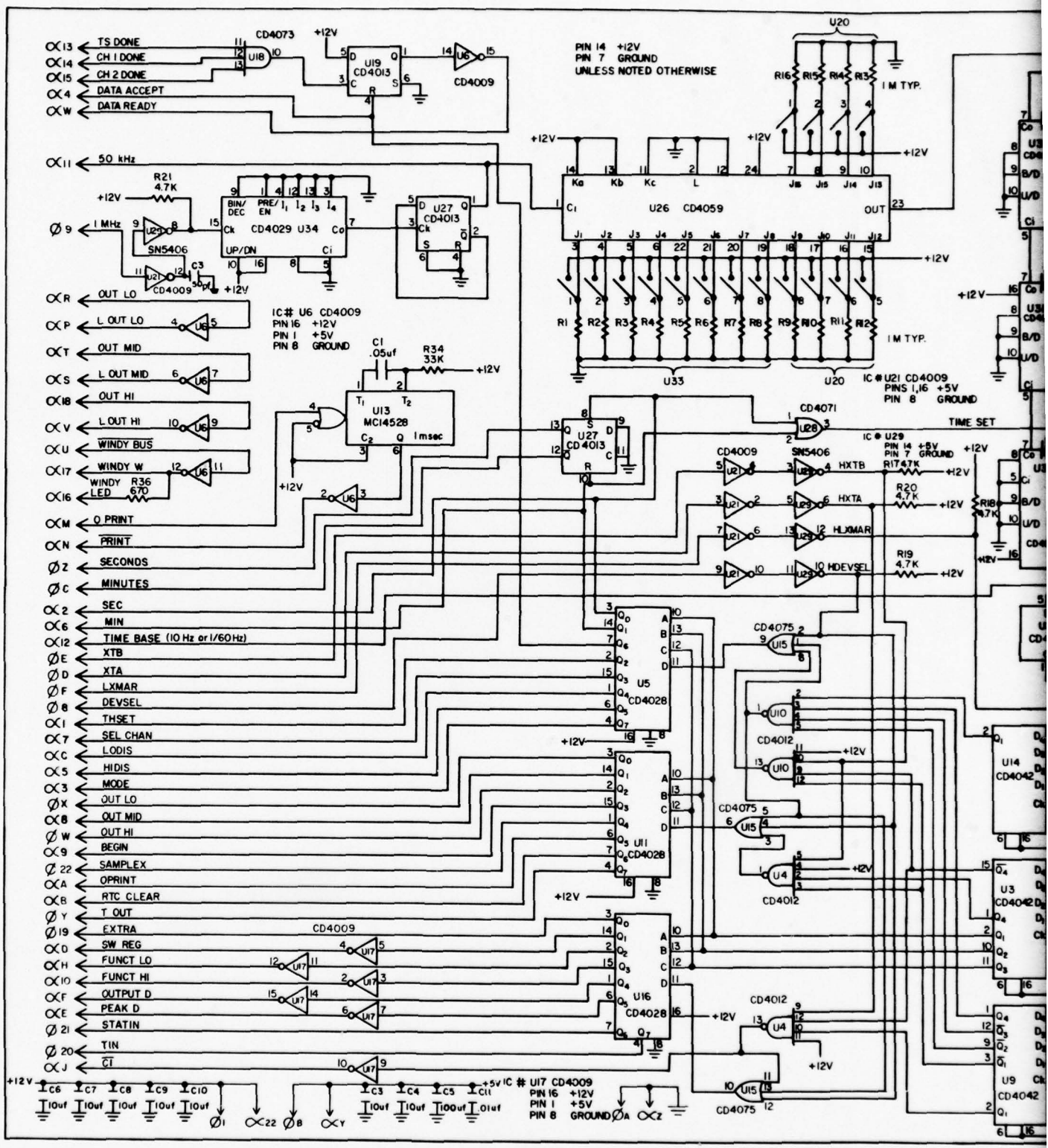
Table 10

Board Number 11003 -- Parts List

Circuit Diagram Reference	Component Type			
R36	Carbon	1/4W	5%	670 Ω
R17-R33, R37	Carbon	1/4W	5%	4.7 K Ω
R34	Carbon	1/4W	5%	33 K Ω
R35	Carbon	1/4W	5%	39 K Ω
R1-R16	Carbon	1/4W	5%	1 M Ω
C2	Mica	10 pF		500 V
C3, C5	Ceramic	.01 uF		100 V
C1	Ceramic	.05 uF		50 V
C4, C6-C11	Tantalum	10 uF		35 V
U1, U2, U6, U17, U21	CD4009			
U3, U9, U14	CD4042			
U4, U10	CD4012			
U5, U11, U16	CD4028			
U7, U8, U29	SN5406			
U13	MC14528			
U15	CD4075			
U18	CD4073			
U19, U22, U27, U35	CD4013			
U23-U25	CD4035			
U26	CD4059			
U28	CD4071			
U30-U32, U34	CD4029			
U20, U33	Dipswitch	8 Station	SPST	



NOTE: C3–C11 ARE BYPASS CAPACITORS. R37 IS USED TO THE UNUSED INPUT OF U29 HIGH.


TS DONE
CH 1 DONE
CH 2 DONE
DATA ACCEPT
DATA READY
50 kHz
1 MHz
OUT LO
L OUT LO
OUT MID
L OUT MID
OUT HI
L OUT HI
WINDY BUS
WINDY W
WINDY LED
Q PRINT
PRINT
SECONDS
MINUTES
SEC
MIN
TIME BASE (10 Hz or 1/60 Hz)
XTB
XTA
LXMAR
DEVSEL
THSET
SEL CHAN
LODIS
HIDIS
MODE
OUT LO
OUT MID
OUT HI
BEGIN
SAMPLEX
OPRINT
RTC CLEAR
T OUT
EXTRA
SW REG
FUNCT LO
FUNCT HI
OUTPUT D
PEAK D
STATIN
TIN
CI
CD4073
CD4009
CD4013
CD4029
CD4059
CD4028
CD4075
CD4012
CD4042
CD4071
SN5406
MC14528
U26 CD4059
U33
U20
HXTB
HXTA
HLXMAR
HDEVSEL
TIME SET
PIN 14 +12V
PIN 7 GROUND
UNLESS NOTED OTHERWISE
1 M TYP.
IC# U6 CD4009
PIN 16 +12V
PIN 1 +5V
PIN 8 GROUND
IC # U21 CD4009
PINS 1,16 +5V
PIN 8 GROUND
IC # U17 CD4009
PIN 16 +12V
PIN 1 +5V
PIN 8 GROUND
IC # U29
PIN 14 +5V
PIN 7 GROUND
R21 4.7K
R34 33K
R17 4.7K
R20 4.7K
R18 4.7K
R19 4.7K
R36 670
C1 .05uf
C3 30pf
C6 10uf
C7 10uf
C8 10uf
C9 10uf
C10 10uf
C3 10uf
C4 10uf
C5 100uf
C11 01uf
+12V
+5V

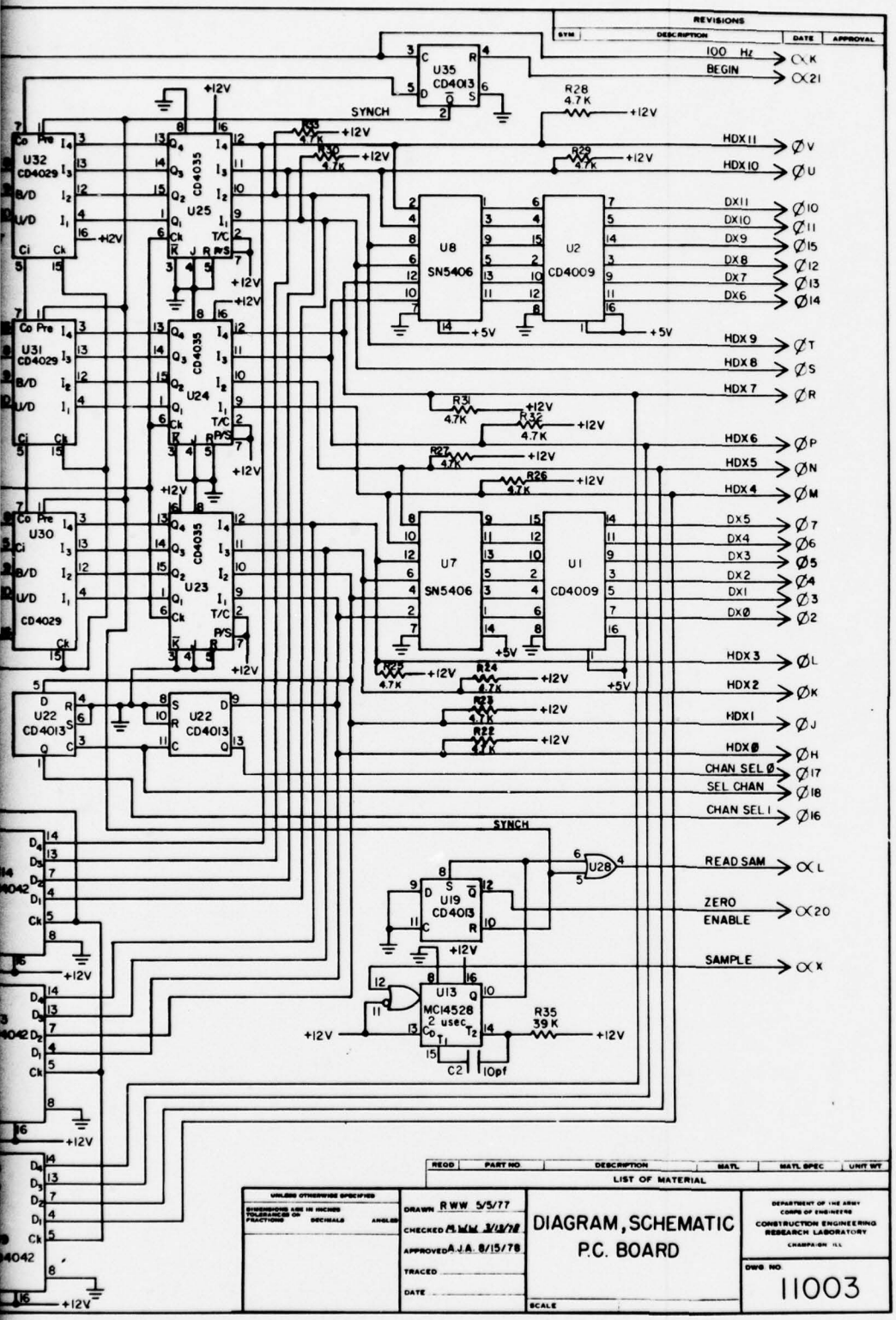
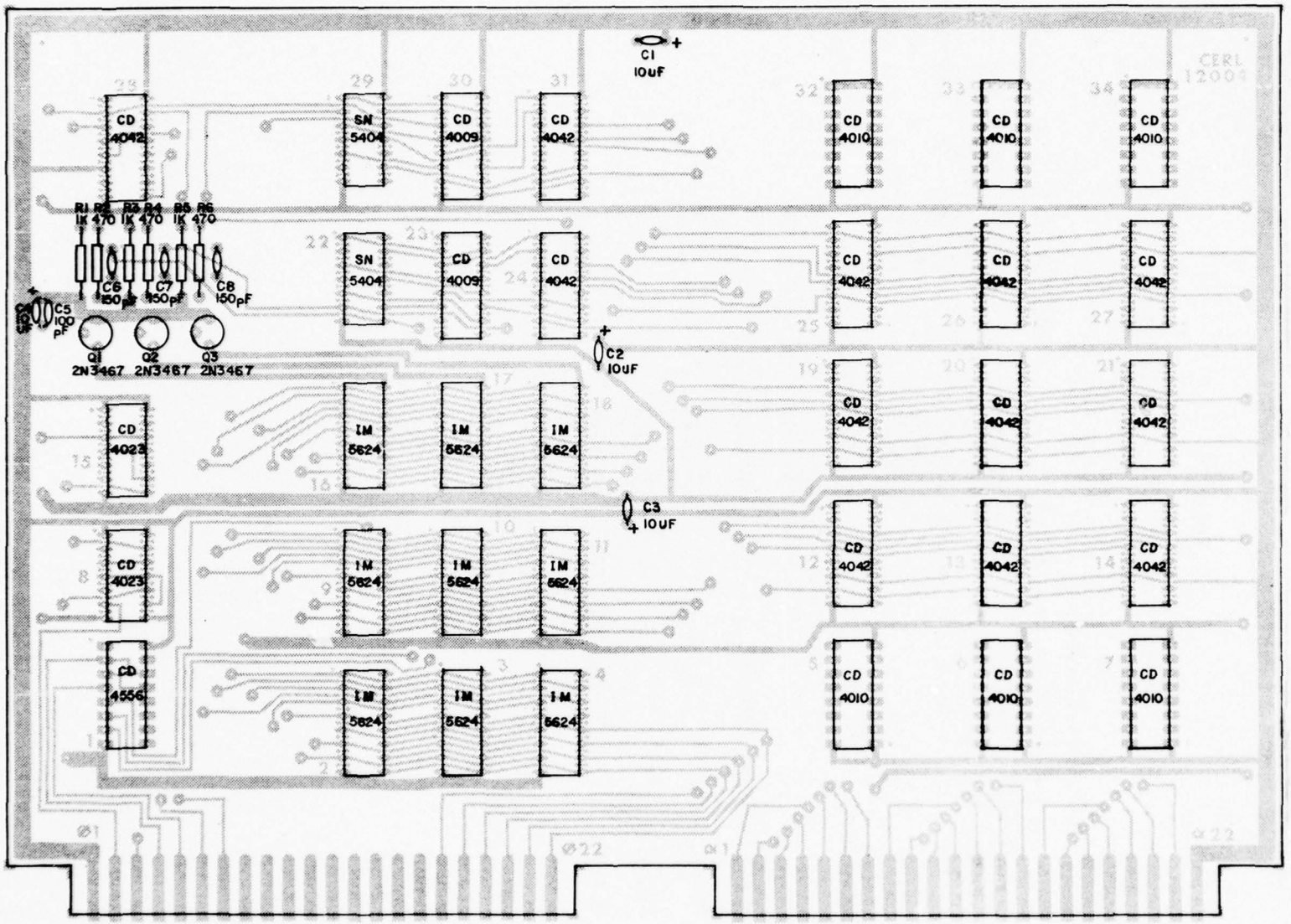

REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
U35 CD4013
100 Hz
BEGIN
SYNCH
+12V
R28 4.7K
R33 4.7K
R30 4.7K
R29 4.7K
U32 CD4029
U25 CD4035
HDX11
HDX10
U8 SN5406
U2 CD4009
DX11
DX10
DX9
DX8
DX7
DX6
+5V
U31 CD4029
U24 CD4035
HDX9
HDX8
HDX7
R31 4.7K
R32 4.7K
R27 4.7K
R26 4.7K
HDX6
HDX5
HDX4
U30 CD4029
U23 CD4035
U7 SN5406
U1 CD4009
DX5
DX4
DX3
DX2
DX1
DX0
R25 4.7K
R24 4.7K
R23 4.7K
R22 4.7K
HDX3
HDX2
HDX1
HDX0
U22 CD4013
CHAN SEL 0
SEL CHAN
CHAN SEL 1
U19 CD4013
U28
READ SAM
ZERO ENABLE
SAMPLE
U13 MC14528
2 usec
R35 39K
C21 10pf
REQD
PART NO.
DESCRIPTION
MATL
MATL SPEC
UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DRAWN RWW 5/5/77
CHECKED
APPROVED
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN ILL
DWG NO.
11003

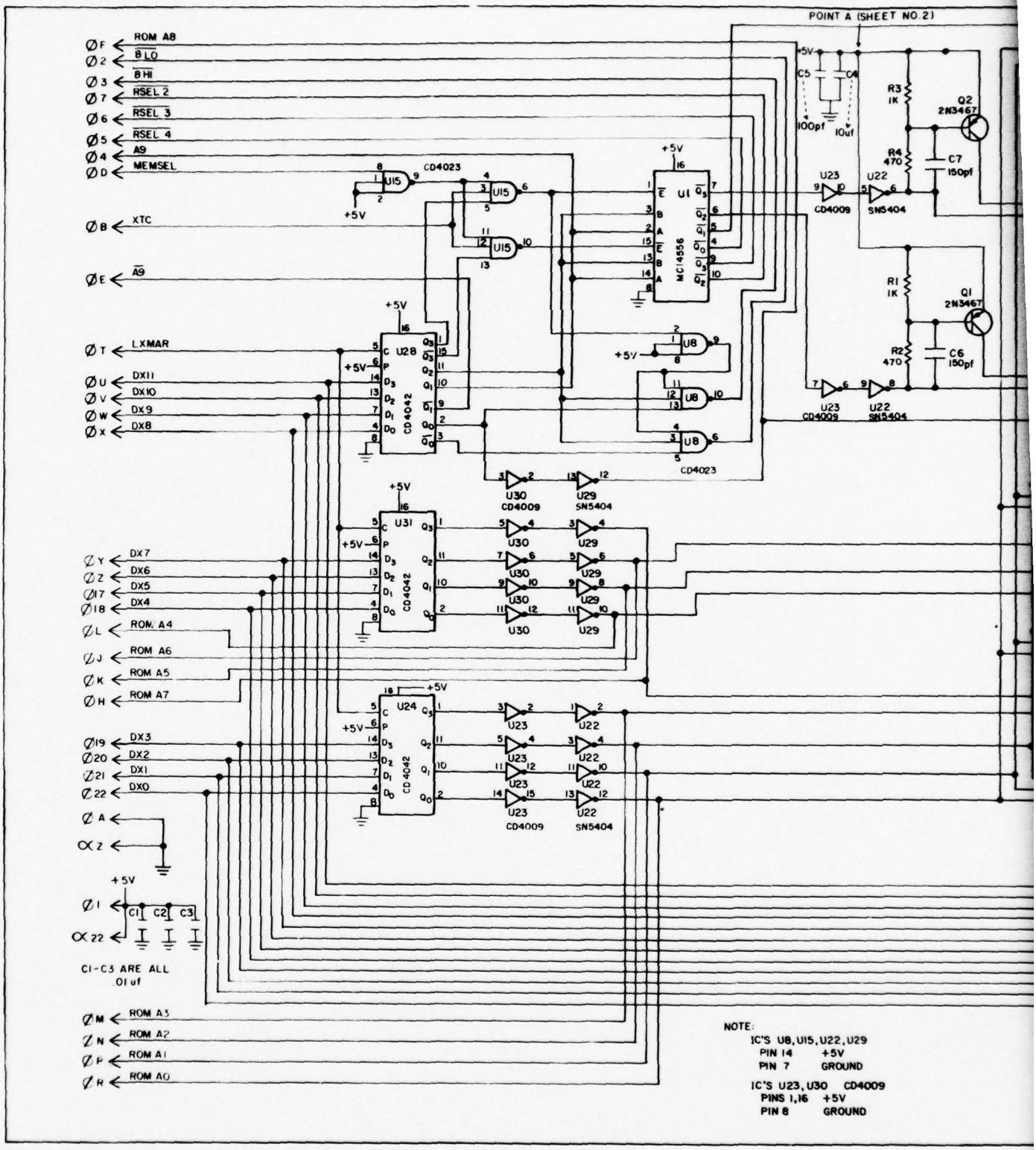
Table 11

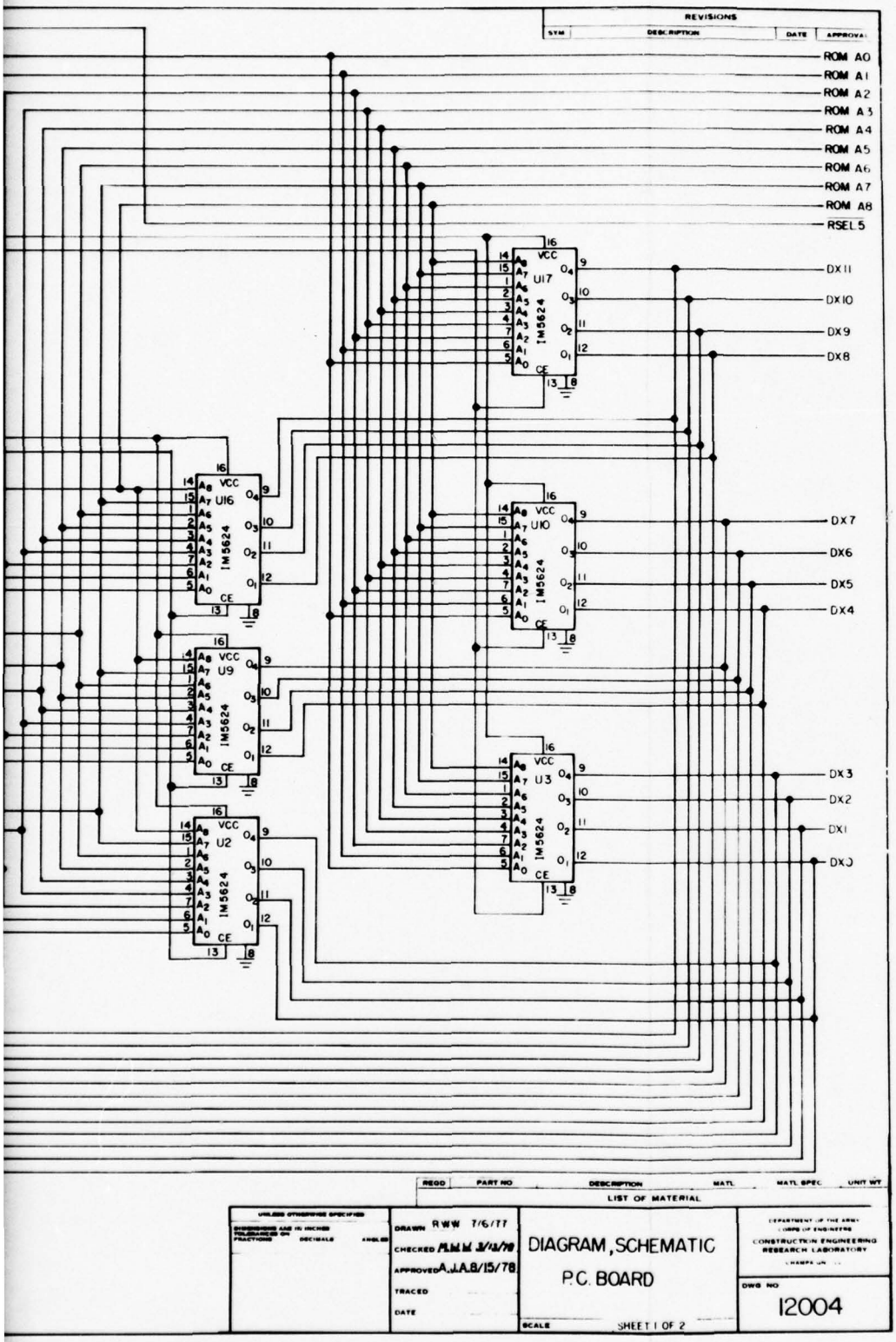
Board Number 12004 -- Parts List

Circuit Diagram Reference	Component Type			
R2, R4, R6	CARBON	1/4W	5%	470 Ω
R1, R3, R5	CARBON	1/4W	5%	1 KΩ
C1-C4	TANTALUM	10 uF		35 V
C5	CERAMIC	100 pF		1 KV
C6-C8	CERAMIC	150 pF		1 KV
Q1-Q3	SILICON TRANS.	PNP		2N3467
U1	CD 4556			
U2-U4, U9-U11, U16-U13	IM 5624			
U5-U7, U32-U34	CD 4010			
U8, U15	CD 4023			
U12-U14, U19-U21, U24-U28, U31	CD 4042			
U22, U29	SN 5404			
U23, U30	CD 4009			

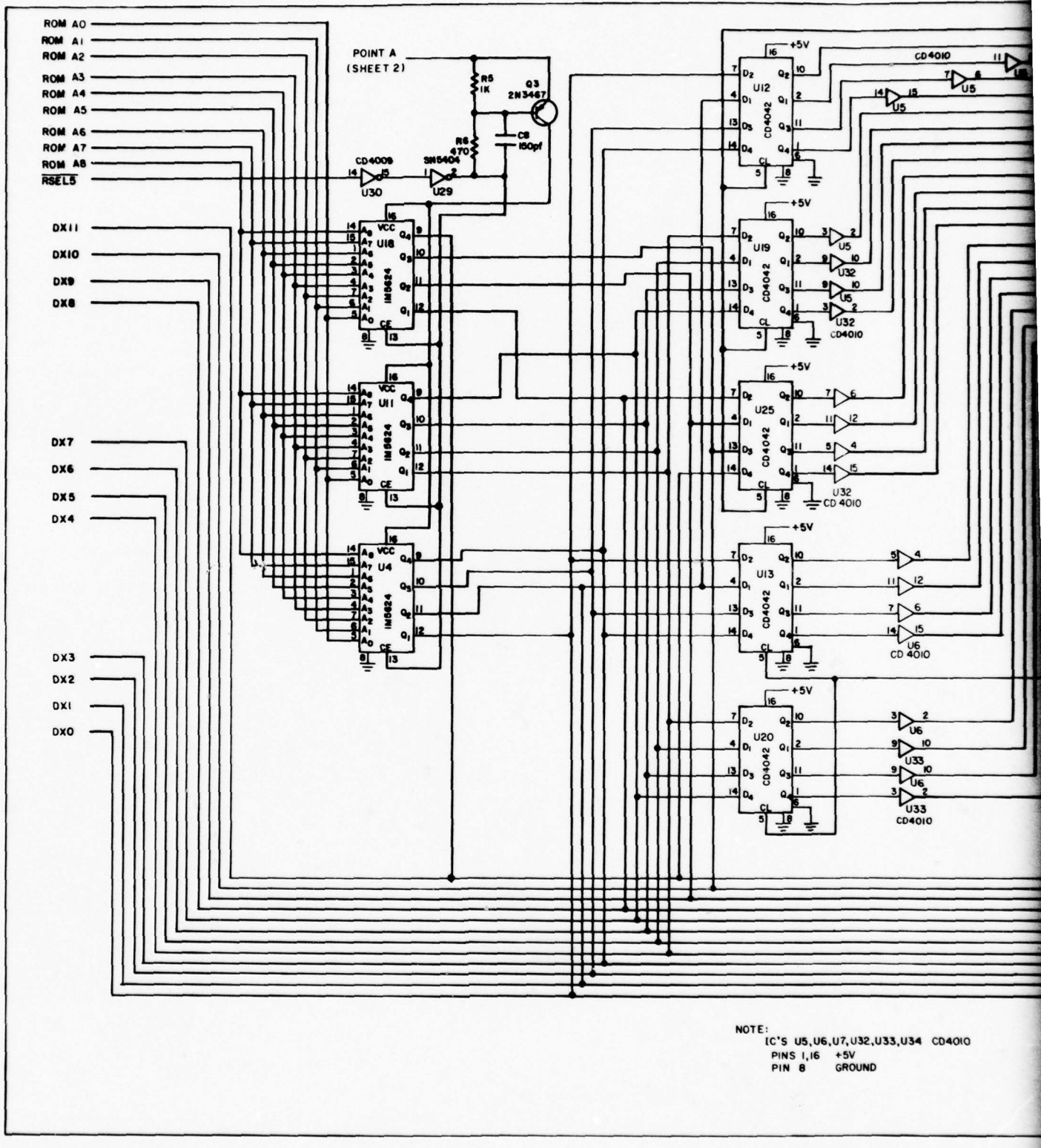


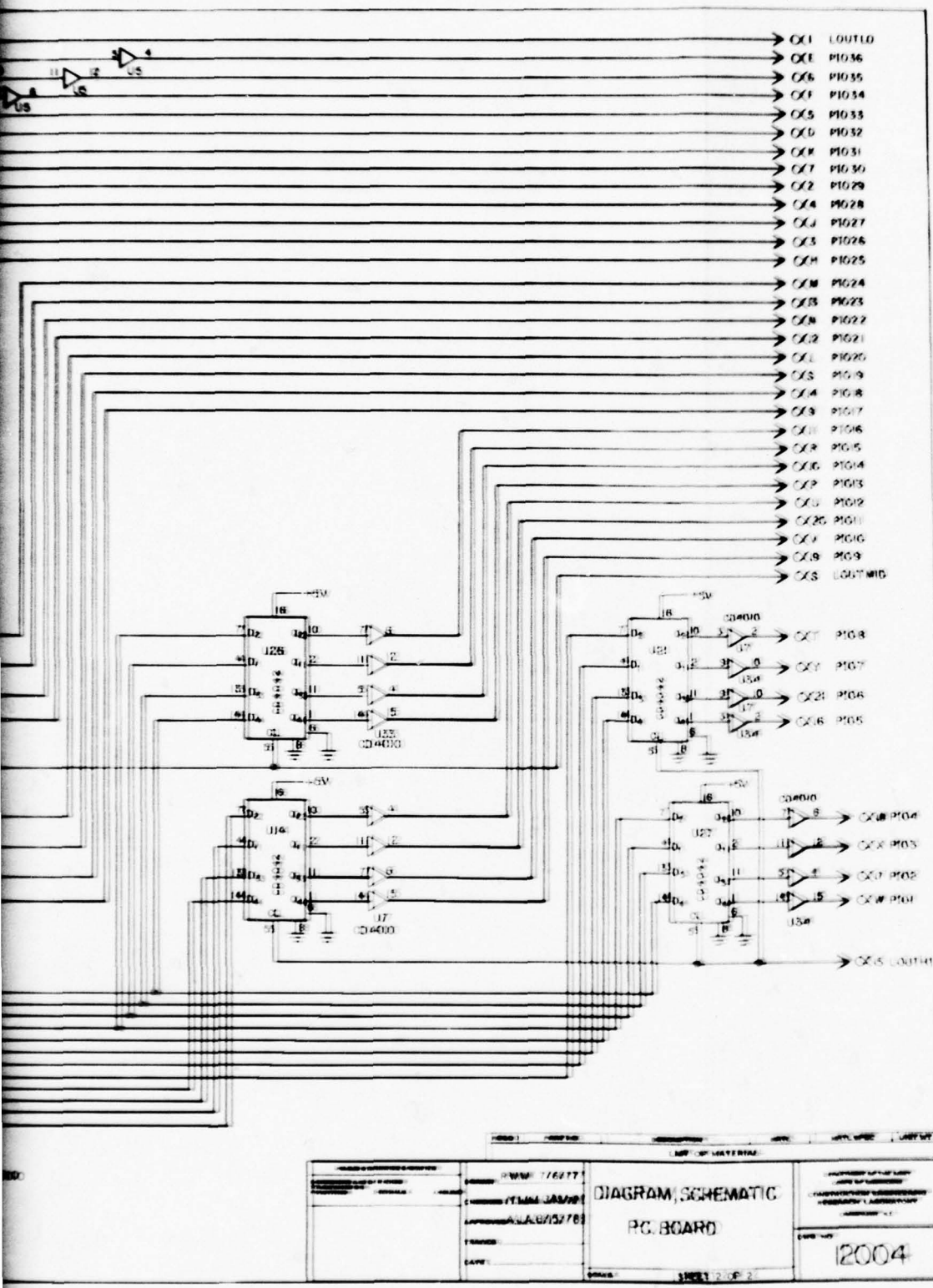
NOTE: C1–C5 ARE BYPASS CAPACITORS.


POINT A (SHEET NO. 2)
ØF ROM A8
Ø2 8 LO
Ø3 8 HI
Ø7 RSEL 2
Ø6 RSEL 3
Ø5 RSEL 4
Ø4 A9
ØD MEMSEL
ØB XTC
ØE A9
ØT LXMAR
ØU DX11
ØV DX10
ØW DX9
ØX DX8
ØY DX7
ØZ DX6
Ø17 DX5
Ø18 DX4
ØL ROM A4
ØJ ROM A6
ØK ROM A5
ØH ROM A7
Ø19 DX3
Ø20 DX2
Ø21 DX1
Ø22 DX0
Ø A
∝Z
Ø1
∝22
C1-C3 ARE ALL .01 uf
ØM ROM A3
ØN ROM A2
ØP ROM A1
ØR ROM A0
+5V
C5 100pf
C4 10uf
R3 1K
R4 470
C7 150pf
Q2 2N3467
R1 1K
R2 470
C6 150pf
Q1 2N3467
U15 CD4023
U1 MC14556
U23 CD4009
U22 SN5404
U28 CD4042
U8 CD4023
U30 CD4009
U29 SN5404
U31 CD4042
U24 CD4042
NOTE:
IC'S U8, U15, U22, U29
PIN 14 +5V
PIN 7 GROUND
IC'S U23, U30 CD4009
PINS 1,16 +5V
PIN 8 GROUND


REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
ROM A0
ROM A1
ROM A2
ROM A3
ROM A4
ROM A5
ROM A6
ROM A7
ROM A8
RSEL 5
U17
U16
U10
U9
U3
U2
IM5624
VCC
CE
DX11
DX10
DX9
DX8
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
REQD
PART NO
DESCRIPTION
MATL
MATL SPEC
UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS
DECIMALS
ANGLES
DRAWN RWW 7/6/77
CHECKED R.L.M 8/15/78
APPROVED A.J.A 8/15/78
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
SHEET 1 OF 2
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN
DWG NO
12004

2


ROM A0
ROM A1
ROM A2
ROM A3
ROM A4
ROM A5
ROM A6
ROM A7
ROM A8
RSEL5
POINT A
(SHEET 2)
R5
1K
Q3
2N3467
R6
470
C8
150pf
CD4009
U30
SN5404
U29
DX11
DX10
DX9
DX8
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
U18
U11
U4
IM5624
VCC
CE
U12
U19
U25
U13
U20
CD4042
+5V
CD4010
U5
U32
U6
U33
NOTE:
IC'S U5,U6,U7,U32,U33,U34 CD4010
PINS 1,16 +5V
PIN 8 GROUND



DIAGRAM, SCHEMATIC
P.C. BOARD

12004

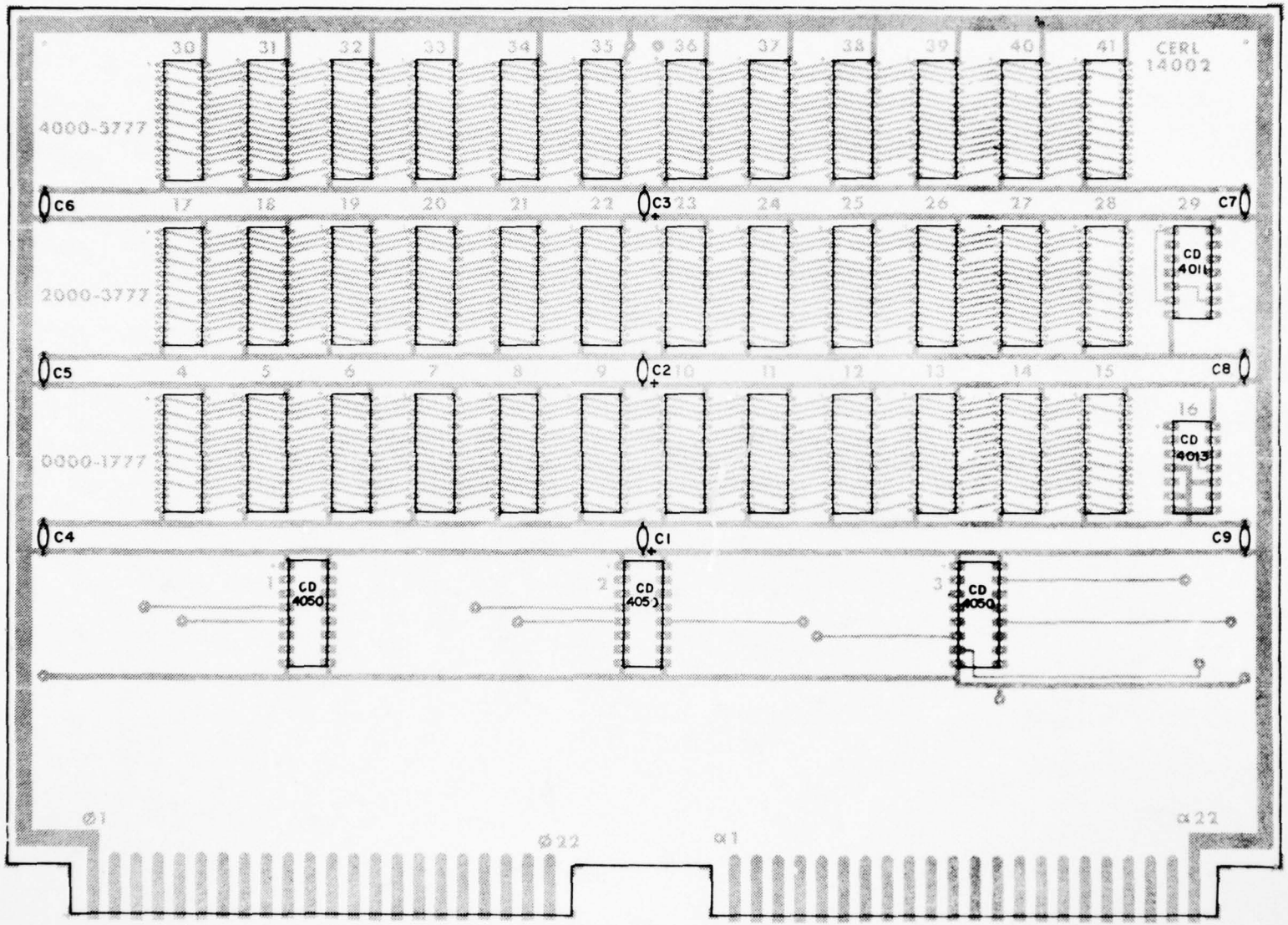
Table 12

Board Number 14002 -- Parts List

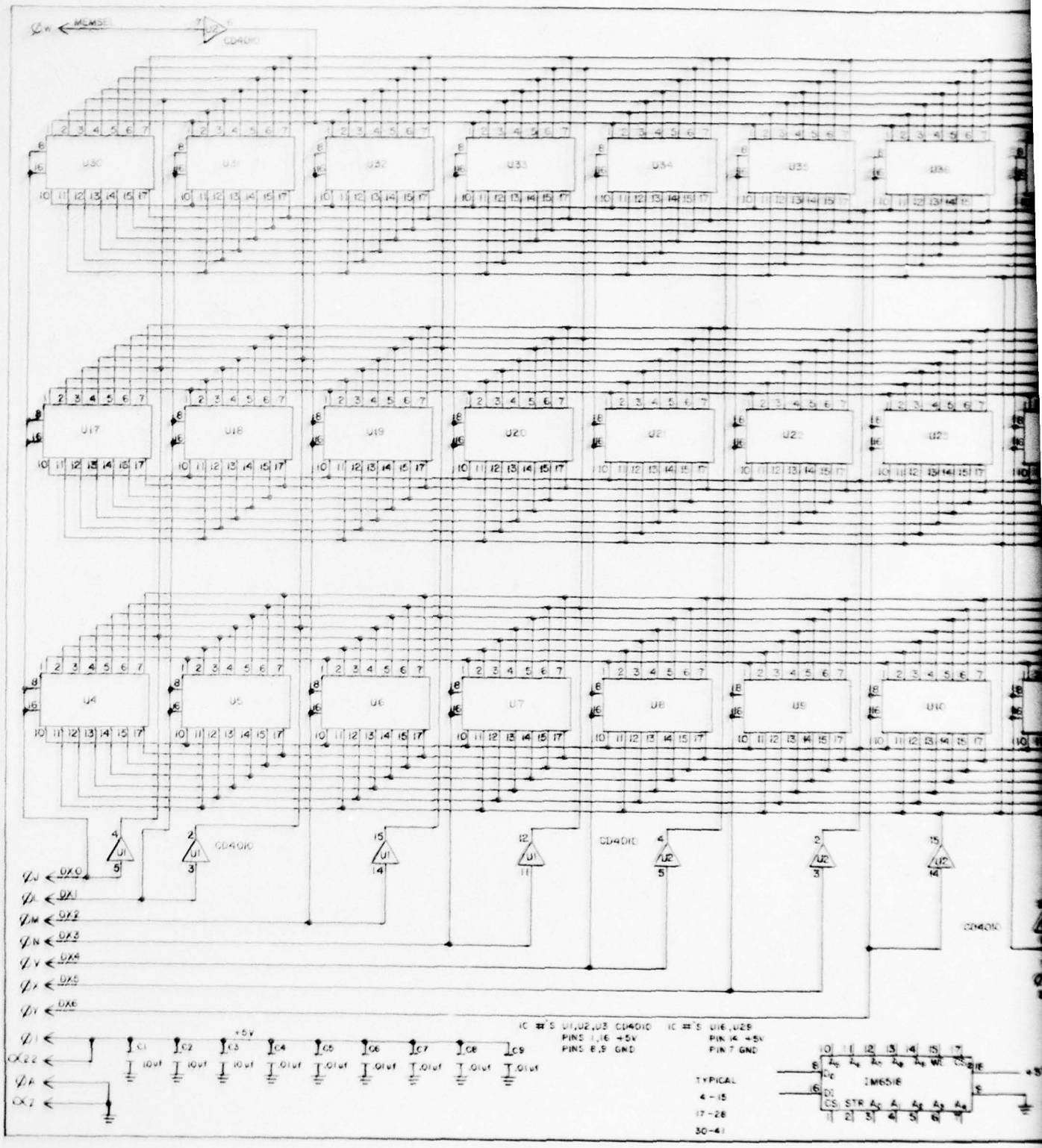
Circuit Diagram Reference	Component Type				
C1, C2, C3	Tantalum	10 uF		35	V
C4, C5, C6, C7, C8, C9	Ceramic	.01 uF	disc	100	V
U1-U3	CD4010				
U4-U15, U17-U28, U30-U41	IM6518IDN				
U16	CD4013				
U29	CD4011				

Note: Board 14002 has only 1U words of memory and has only U4-U15 installed. U17-28 and U30-41 must not be used unless less read only memory is used.

Board Slot 19 has a Board 14002 installed there. It can have 1, 2, or 3 kilo words installed. If less than 3 kilowords is used, the sockets with the lower U designations should be used first.



NOTE: C1 AND C2 ARE BYPASS CAPACITORS. EACH IS 10uf. U4–U15, U17–U28, U30–U41 ARE ALL IM6518.


MEMSEL
CD4010
U30
U31
U32
U33
U34
U35
U36
U17
U18
U19
U20
U21
U22
U23
U4
U5
U6
U7
U8
U9
U10
CD4010
CD4010
CD4010
DX0
DX1
DX2
DX3
DX4
DX5
DX6
+5V
C1 10uf
C2 10uf
C3 10uf
C4 .01uf
C5 .01uf
C6 .01uf
C7 .01uf
C8 .01uf
C9 .01uf
IC #'S U1,U2,U3 CD4010
PINS 1,16 +5V
PINS 8,9 GND
IC #'S U16,U29
PIN 14 +5V
PIN 7 GND
TYPICAL
4-15
17-28
30-41
IM6518
STR
CS
+5

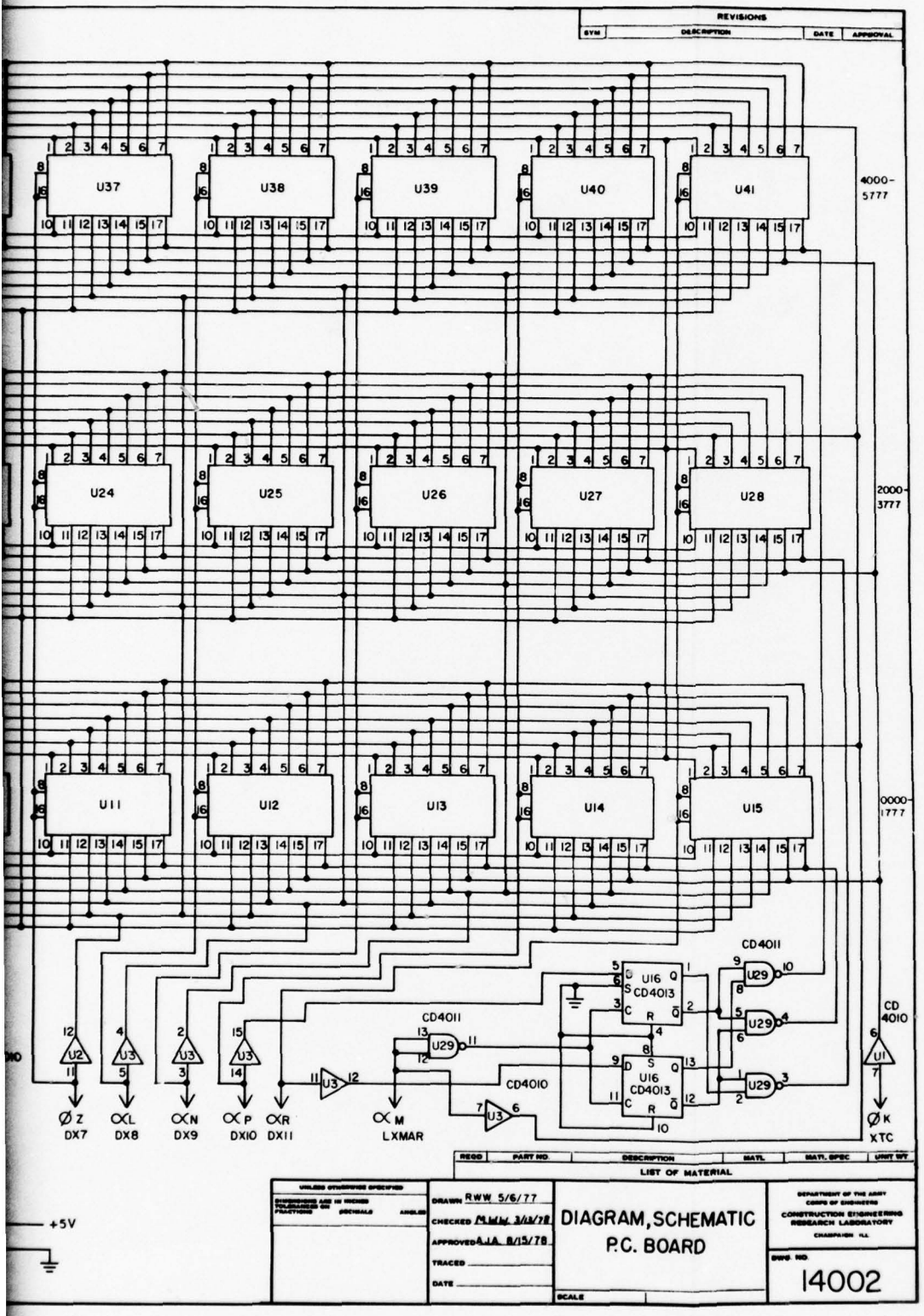
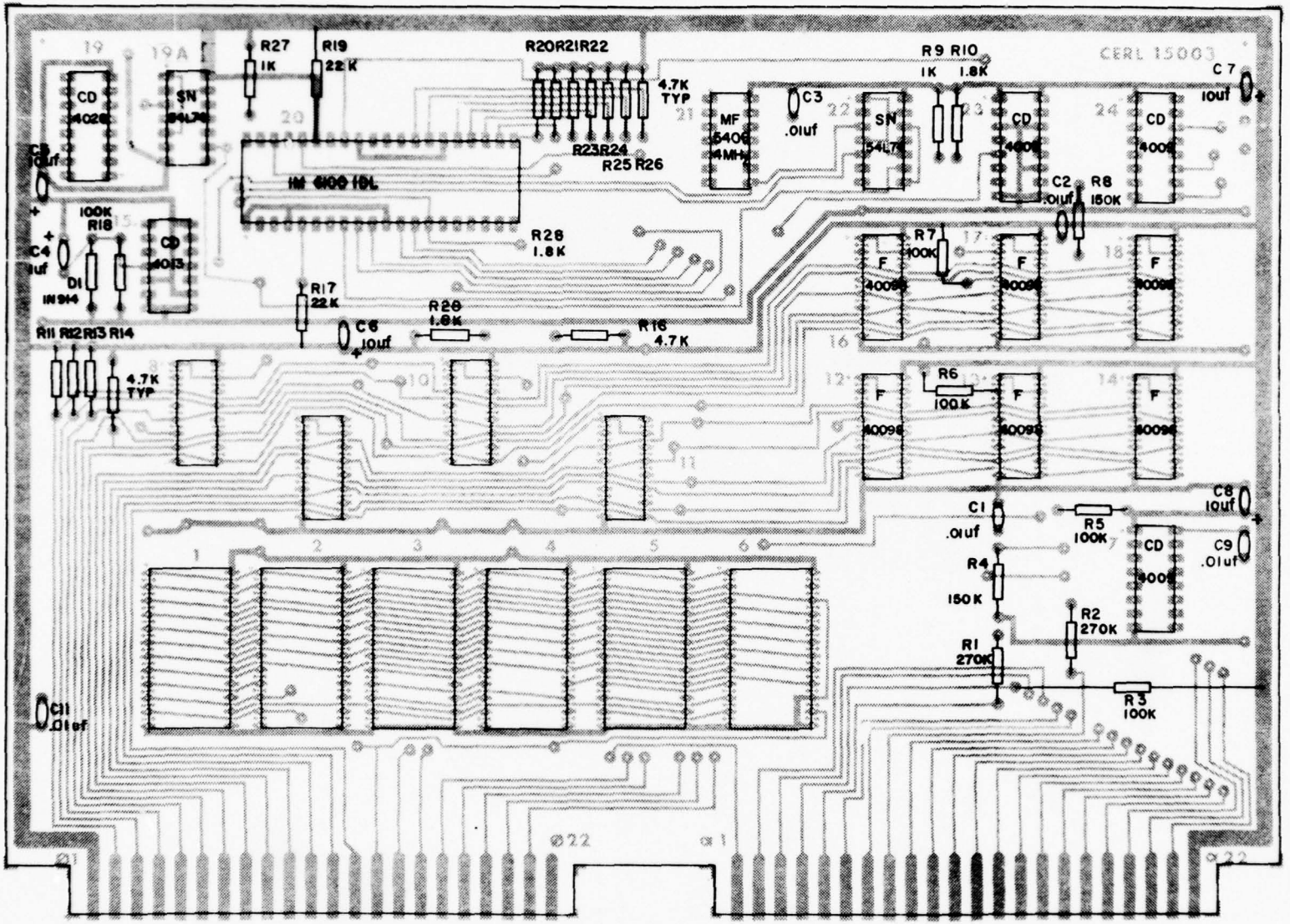

REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
U37
U38
U39
U40
U41
4000-
5777
U24
U25
U26
U27
U28
2000-
3777
U11
U12
U13
U14
U15
0000-
1777
CD4011
U16
CD4013
U29
CD4010
U1
U2
U3
ØZ
DX7
ØL
DX8
ØN
DX9
ØP
DX10
ØR
DX11
ØM
LXMAR
ØK
XTC
+5V
REQD
PART NO.
DESCRIPTION
MATL
MAT'L SPEC
UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS
DECIMALS
ANGLES
DRAWN RWW 5/6/77
CHECKED
APPROVED
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN ILL
DWG NO
14002

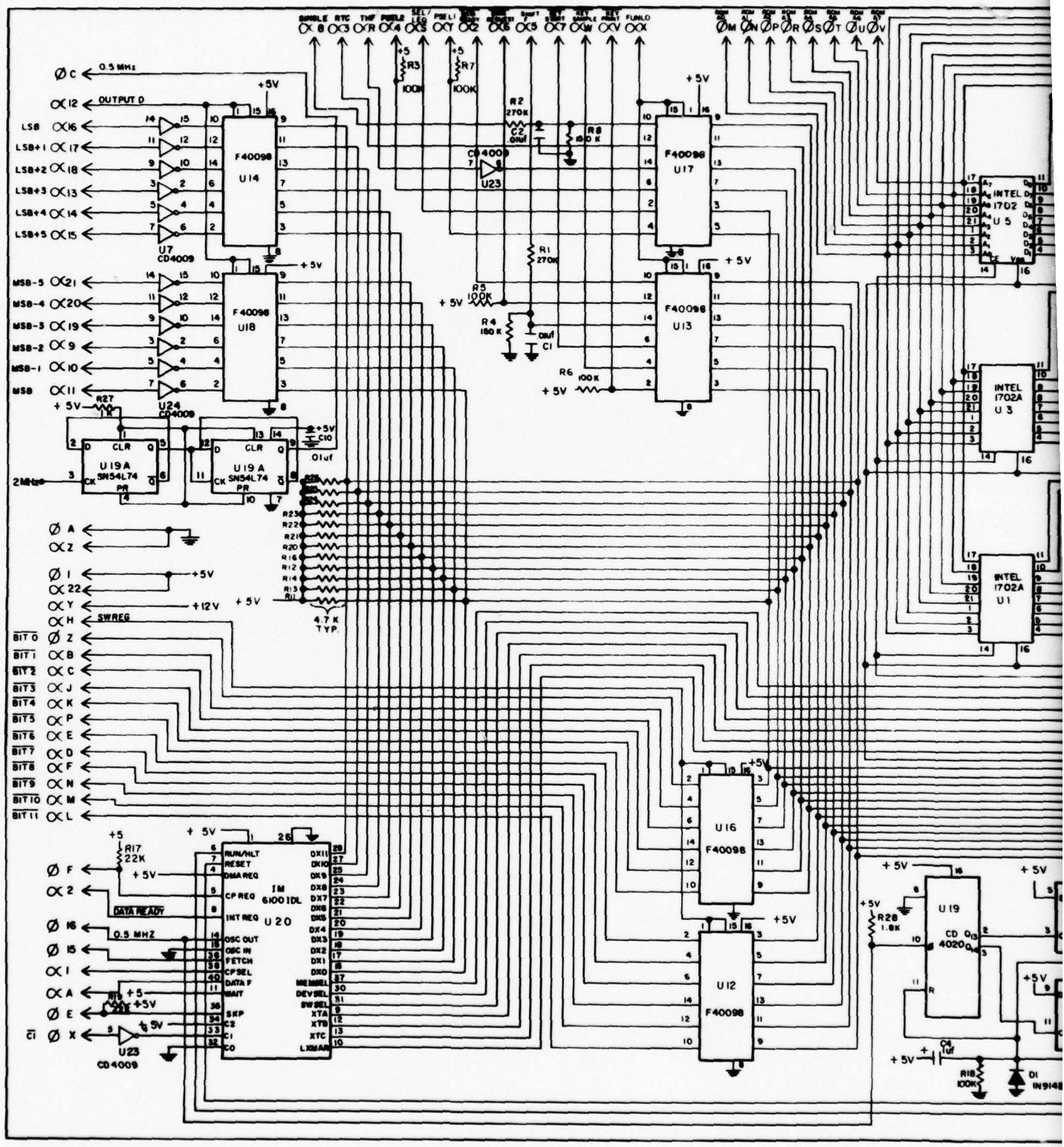
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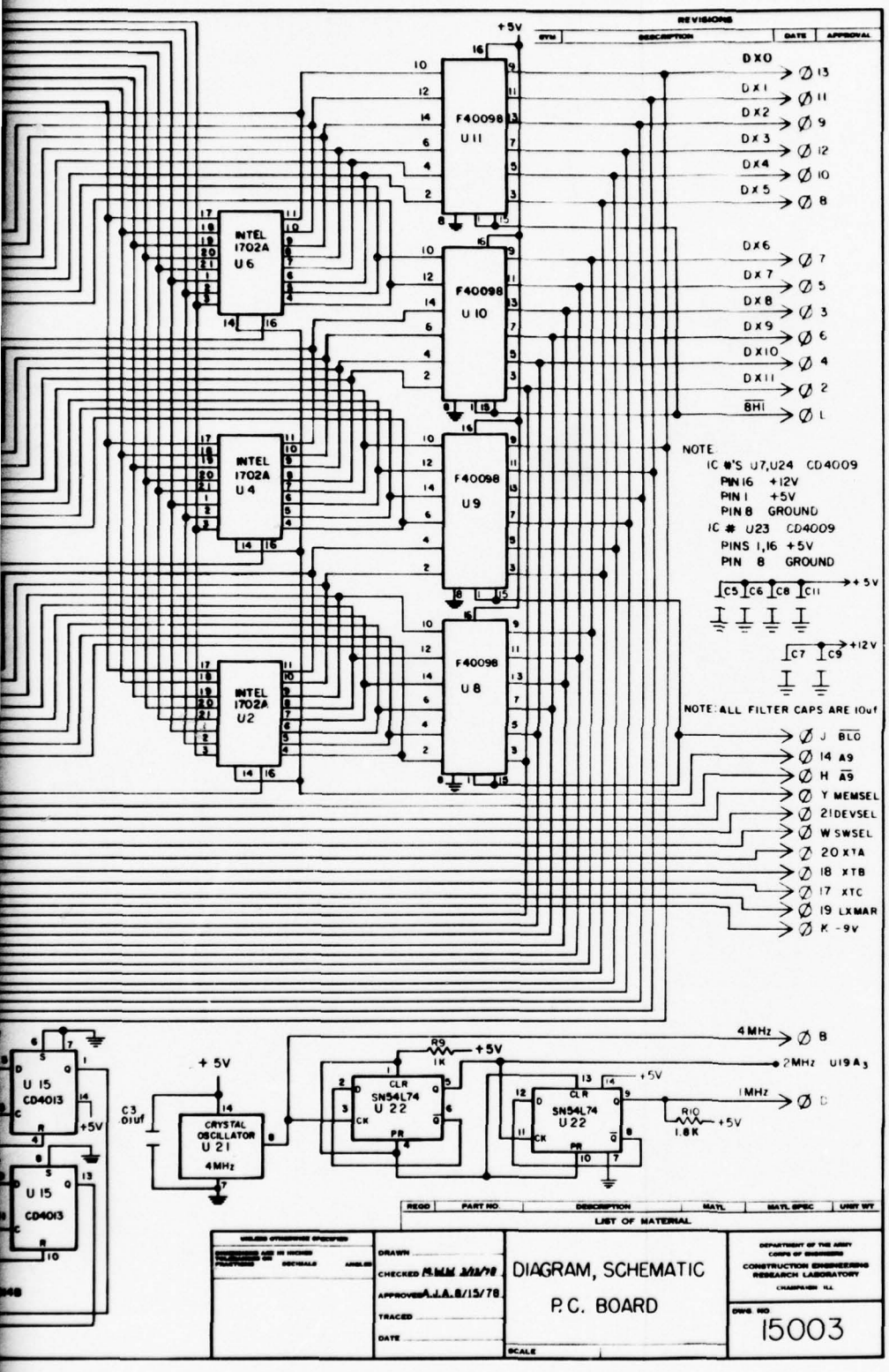
Board Number 15003 -- Parts List

Circuit Diagram Reference	Component Type				
R9, R27	Carbon	1/4W	5%	1	K Ω
R10, R15, R28	Carbon	1/4W	5%	1.8	K Ω
R11-R14, R20-R26, R16	Carbon	1/4W	5%	4.7	K Ω
R17, R19	Carbon	1/4W	5%	22	K Ω
R3, R5-R7, R18	Carbon	1/4W	5%	100	K Ω
R4, R8	Carbon	1/4W	5%	150	K Ω
R1, R2	Carbon	1/4W	5%	270	K Ω
C1-C3, C10	Ceramic	.01 uF		100	V
C4	Tantalum	1 uF		35	V
C5-C9	Tantalum	10 uF		35	V
D1-D25	Silicon Diode	1N914B			
U7, U23, U24	CD4009				
U12-U14, U16-U18	F40098				
U15	CD4013				
U19	CD4020				
U19A, U22	SN54L74				
U20	IM6100IDL				
U21	Crystal Oscillator MF5406 4MHZ				



NOTE: C5–C8 ARE BYPASS CAPACITORS. SPACES ARE PROVIDED ON BOARD FOR U1–U6 (I1702) AND U8–U11 (40098) BUT ARE NOT NORMALLY USED. DIODES D2–D25 ARE NEEDED ON INPUTS OF 40098 WHEN THEY ARE USED AND ADDED ON BOTTOM SIDE OF BOARD.


F40098 U14
F40098 U18
F40098 U17
F40098 U13
F40098 U16
F40098 U12
CD4009 U23
CD4009 U24
CD4009 U7
SN54L74 U19A
IM 6100 IDL U20
CD 4020 U19
INTEL 1702A U5
INTEL 1702A U3
INTEL 1702A U1
+5V
+12V
0.5 MHz
2MHz
DATA READY
SWREG
4.7K TYP.

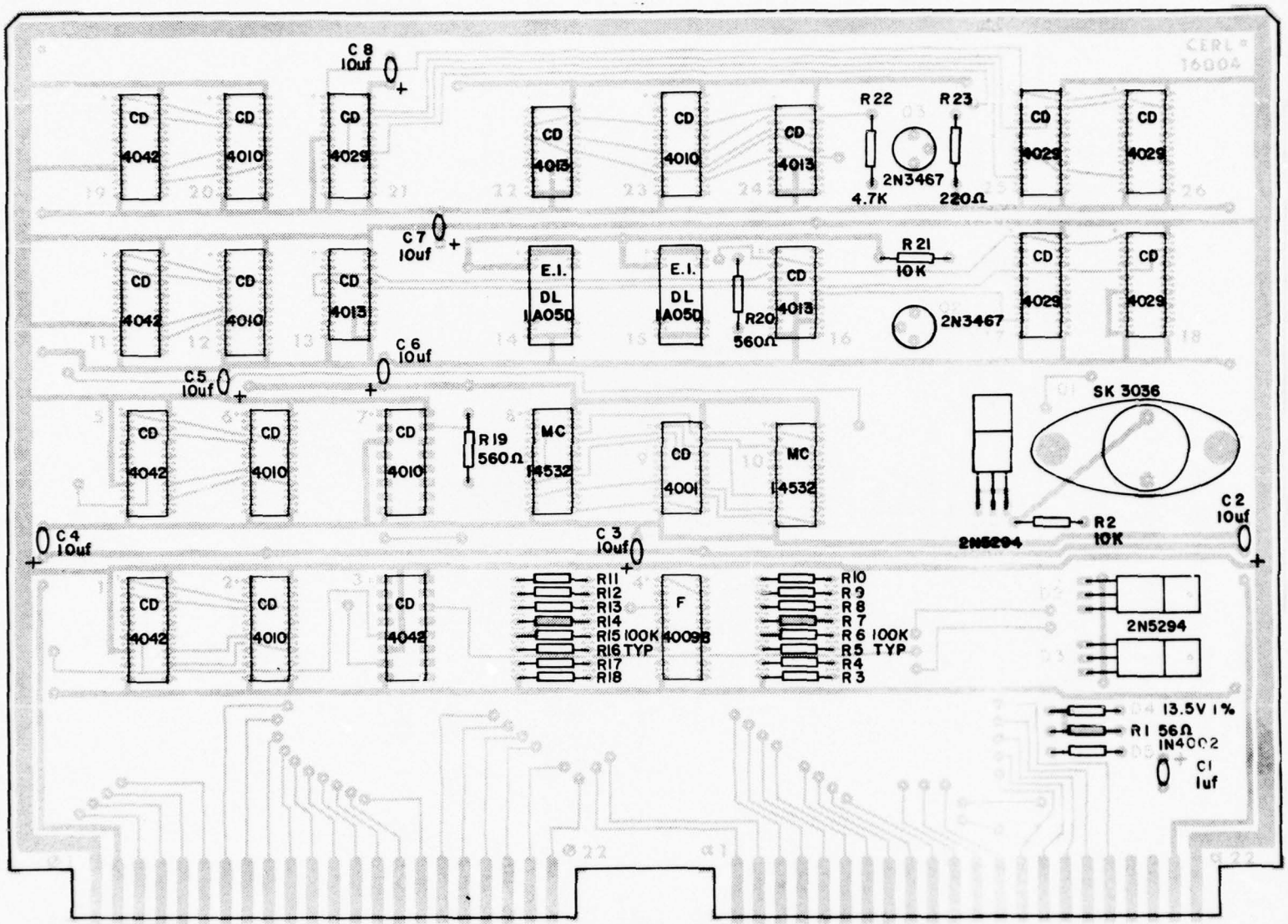

REVISIONS
ZON | DESCRIPTION | DATE | APPROVAL
+5V
F40098 U11
F40098 U10
F40098 U9
F40098 U8
INTEL 1702A U6
INTEL 1702A U4
INTEL 1702A U2
DX0 Ø 13
DX1 Ø 11
DX2 Ø 9
DX3 Ø 12
DX4 Ø 10
DX5 Ø 8
DX6 Ø 7
DX7 Ø 5
DX8 Ø 3
DX9 Ø 6
DX10 Ø 4
DX11 Ø 2
8HI Ø L
NOTE
IC #'S U7,U24 CD4009
PIN 16 +12V
PIN 1 +5V
PIN 8 GROUND
IC # U23 CD4009
PINS 1,16 +5V
PIN 8 GROUND
C5 C6 C8 C11 +5V
C7 C9 +12V
NOTE: ALL FILTER CAPS ARE 10uf
Ø J BLO
Ø 14 A9
Ø H A9
Ø Y MEMSEL
Ø 21 DEVSEL
Ø W SWSEL
Ø 20 XTA
Ø 18 XTB
Ø 17 XTC
Ø 19 LXMAR
Ø K -9V
U 15 CD4013
+5V
C3 .01uf
CRYSTAL OSCILLATOR U 21 4MHz
R9 1K
SN54L74 U 22
R10 1.8K
4MHz Ø B
2MHz U19 A3
1MHz Ø D
REQD | PART NO. | DESCRIPTION | MATL | MATL SPEC | UNIT WT
LIST OF MATERIAL
DRAWN
CHECKED
APPROVED A.J.A. 8/15/78
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN ILL.
DWG NO
15003

2

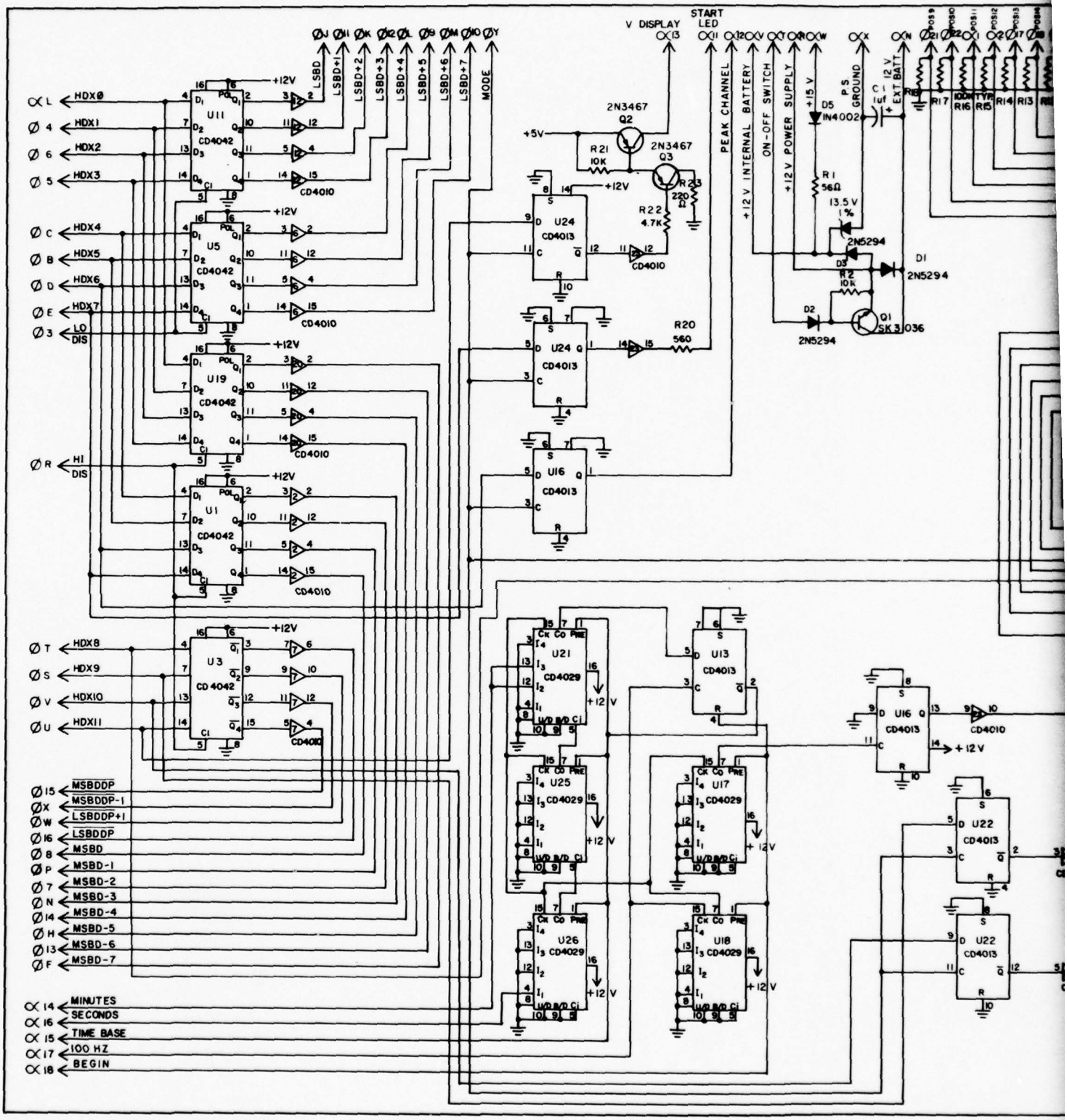
Table 14

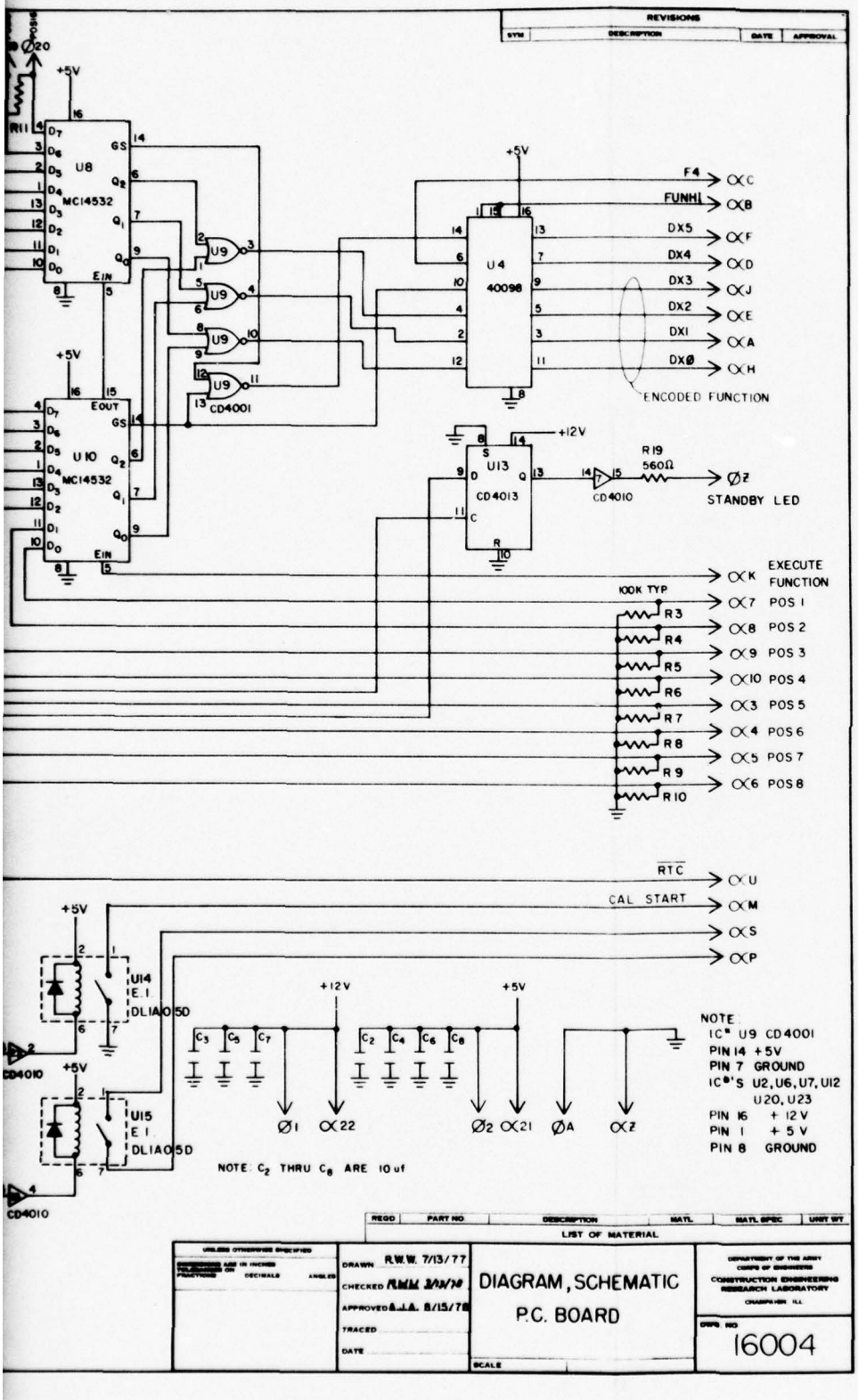
Board Number 16004 -- Parts List

Circuit Diagram Reference	Component Type				
R1	Carbon	1/4W	5%	56	Ω
R23	Carbon	1/4W	5%	220	Ω
R19, R20	Carbon	1/4W	5%	560	Ω
R22	Carbon	1/4W	5%	4.7	K Ω
R2, R21	Carbon	1/4W	5%	10	K Ω
R3-R18	Carbon	1/4W	5%	100	K Ω
C1	Tantalum	1 uF		35	V
C2-C8	Tantalum	10 uF		35	V
D1-D3	Silicon Power Trans	NPN	2N5294		
D4	Zener	1/2W	1%	13.5	V
D5	Silicon Diode	IN4002			
Q1	Silicon High Power	NPN	SK3036		
Q2, Q3	Silicon Trans	PNP	2N3467		
U1, U3, U5, U11, U19	CD4042				
U2, U6, U7, U12, U20, U23	CD4010				
U4	F40098				
U8, U10	MC14532				
U9	CD4001				
U13, U16, U22, U24	CD4013				
U14, U15	EI DL 1A05D				
U17, U18, U21, U25, U26	CD4029				



NOTE: C2–C8 ARE BYPASS CAPACITORS. D1–D3 ARE POWER TRANSISTORS WITH EMITTER AND BASE CONNECTED TOGETHER FOR HIGH POWER DIODE.


HDX0
HDX1
HDX2
HDX3
HDX4
HDX5
HDX6
HDX7
LO DIS
HI DIS
HDX8
HDX9
HDX10
HDX11
MSBDDP
MSBDDP-1
LSBDDP+1
LSBDDP
MSBD
MSBD-1
MSBD-2
MSBD-3
MSBD-4
MSBD-5
MSBD-6
MSBD-7
MINUTES
SECONDS
TIME BASE
100 HZ
BEGIN
LSBD
LSBD+1
LSBD+2
LSBD+3
LSBD+4
LSBD+5
LSBD+6
LSBD+7
MODE
START LED
V DISPLAY
PEAK CHANNEL
+12 V INTERNAL BATTERY
ON-OFF SWITCH
+12 V POWER SUPPLY
+15 V
PS GROUND
12 V EXT BATT
+5V
+12V
2N3467
2N5294
SK3036
CD4042
CD4010
CD4013
CD4029



REQD	PART NO	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED

DRAWN R.W.W. 7/13/77

CHECKED R.W.W. 7/13/77

APPROVED A.J.A. 8/15/78

TRACED

DATE

SCALE

DIAGRAM, SCHEMATIC
P.C. BOARD

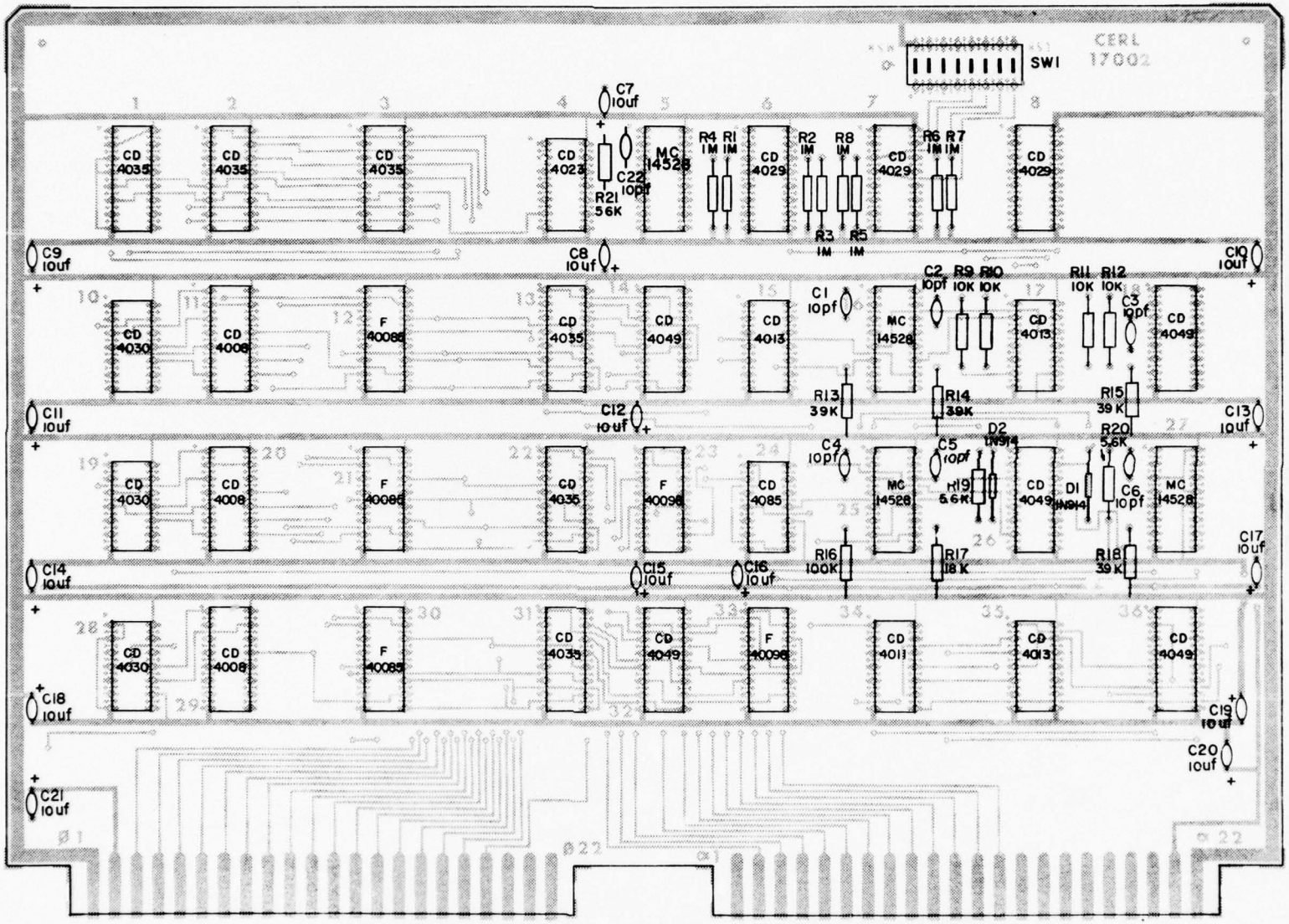
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN ILL.

DRG NO
16004

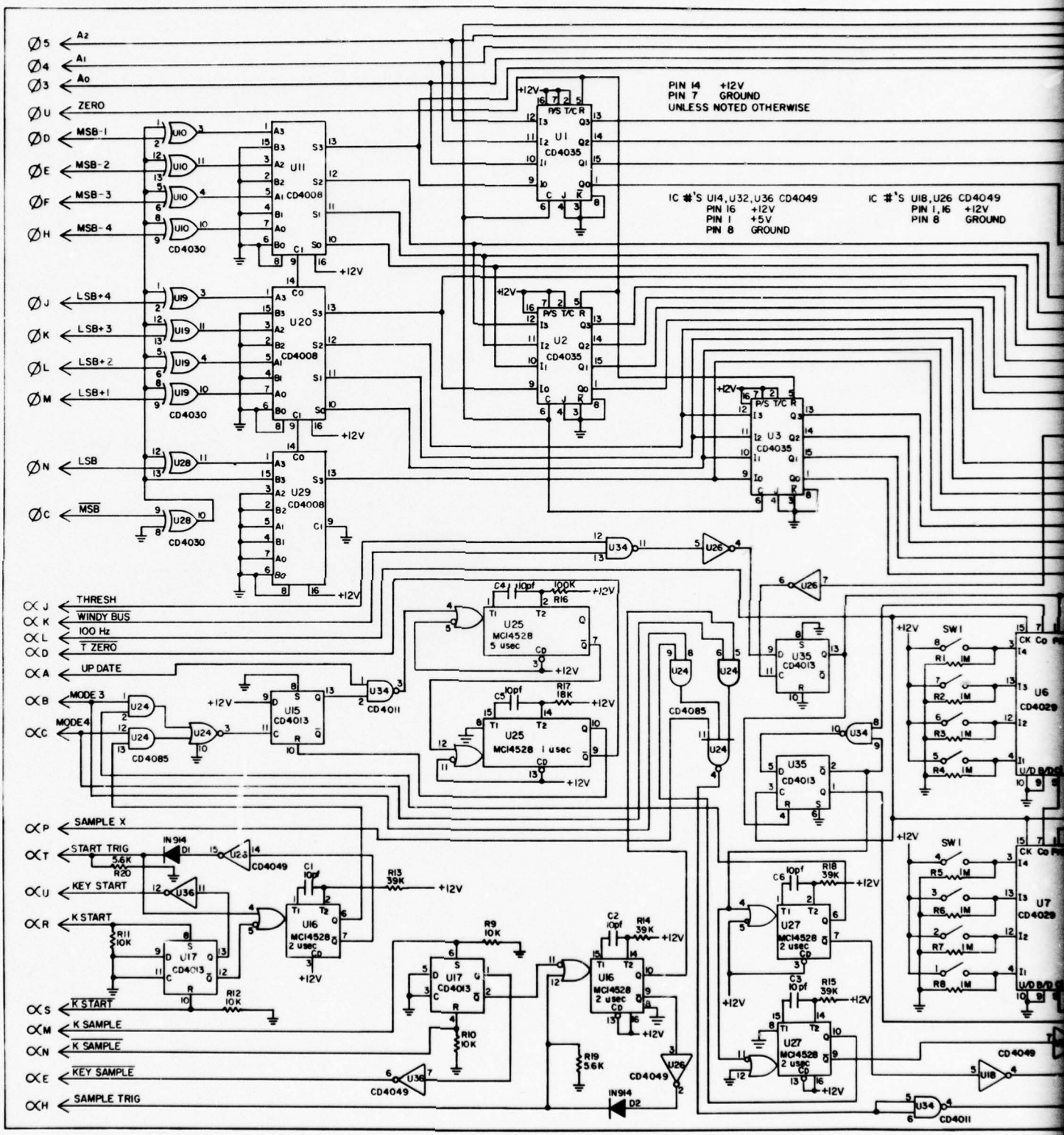
Table 15

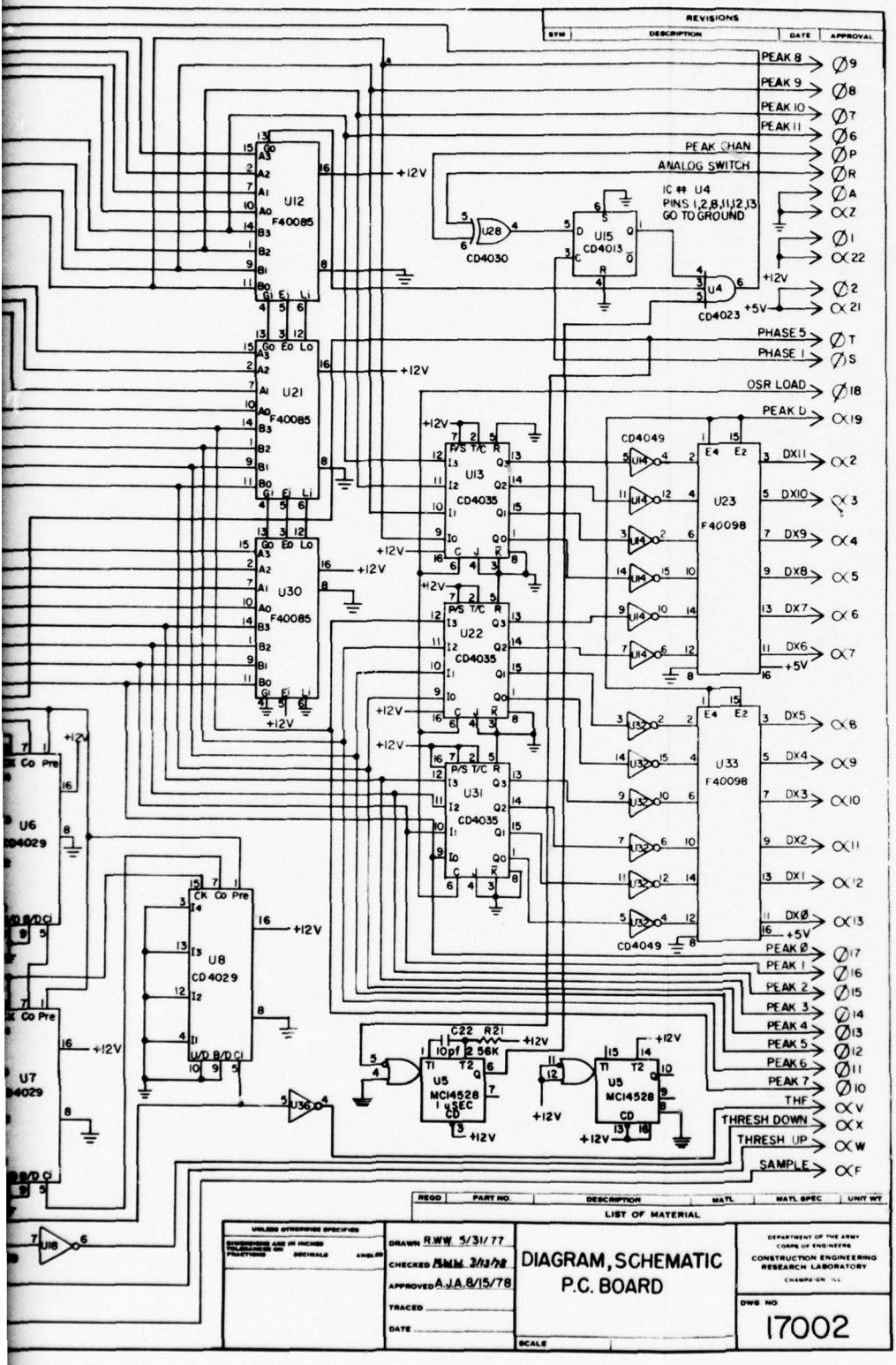
Board Number 17002 -- Parts List

Circuit Diagram Reference	Component Type			
R19, R20	Carbon	1/4W	5%	5.6 K Ω
R9-R12	Carbon	1/4W	5%	10 K Ω
R17	Carbon	1/4W	5%	18 K Ω
R13-R15, R18	Carbon	1/4W	5%	39 K Ω
R16	Carbon	1/4W	5%	100 K Ω
R1-R8	Carbon	1/4W	5%	1 M Ω
C1-C6	Mica	10 pF		500 V
C7-C21	Tantalum	10 uF		35 V
D1, D2	Silicon	IN914B		
U1-U3, U13, U22, U31	CD4035			
U4	CD4023			
U6-U8	CD4029			
U10, U19, U28	CD4030			
U11, U20, U29	CD4008			
U12, U21, U30	F40085			
U14, U18, U26, U32, U36	CD4049			
U15, U17, U35	CD4013			
U16, U25, U27	MC14528			
U23, U33	F40098			
U24	CD4085			
U34	CD4011			
U9 (SW1)	Dipswitch 8 Station		SPST	



NOTE: C7–C21 ARE BYPASS CAPACITORS. EACH CAPACITOR IS 10uf.


PIN 14 +12V
PIN 7 GROUND
UNLESS NOTED OTHERWISE
IC #'S U14, U32, U36 CD4049
PIN 16 +12V
PIN 1 +5V
PIN 8 GROUND
IC #'S U18, U26 CD4049
PIN 1, 16 +12V
PIN 8 GROUND
CD4030
CD4008
CD4035
CD4049
CD4011
CD4085
CD4029
MCI4528
CD4013
A2
A1
A0
ZERO
MSB-1
MSB-2
MSB-3
MSB-4
LSB+4
LSB+3
LSB+2
LSB+1
LSB
MSB
THRESH
WINDY BUS
100 Hz
T ZERO
UP DATE
MODE 3
MODE 4
SAMPLE X
START TRIG
KEY START
K START
K SAMPLE
K SAMPLE
KEY SAMPLE
SAMPLE TRIG
5 usec
1 usec
2 usec
SW1


REVISIONS
SYM | DESCRIPTION | DATE | APPROVAL
PEAK 8 → Ø9
PEAK 9 → Ø8
PEAK 10 → ØT
PEAK 11 → Ø6
PEAK CHAN → ØP
ANALOG SWITCH → ØR
ØA
∝Z
Ø1
∝22
Ø2
∝21
IC # U4
PINS 1,2,8,11,12,13
GO TO GROUND
U12 F40085
U21 F40085
U30 F40085
U28 CD4030
U15 CD4013
U4 CD4023
+12V
+5V
PHASE 5 → ØT
PHASE 1 → ØS
OSR LOAD → Ø18
PEAK D → ∝19
U13 CD4035
U22 CD4035
U31 CD4035
P/S T/C
CD4049
U23 F40098
U33 F40098
DX11 → ∝2
DX10 → ∝3
DX9 → ∝4
DX8 → ∝5
DX7 → ∝6
DX6 → ∝7
DX5 → ∝8
DX4 → ∝9
DX3 → ∝10
DX2 → ∝11
DX1 → ∝12
DXØ → ∝13
PEAK Ø → Ø17
PEAK 1 → Ø16
PEAK 2 → Ø15
PEAK 3 → Ø14
PEAK 4 → Ø13
PEAK 5 → Ø12
PEAK 6 → Ø11
PEAK 7 → Ø10
THF → ∝V
THRESH DOWN → ∝X
THRESH UP → ∝W
SAMPLE → ∝F
U8 CD4029
U6 CD4029
U7 CD4029
U36
U18
C22 10pf
R21 2.56K
U5 MC14528 CD
1 µSEC
REQD | PART NO. | DESCRIPTION | MATL | MATL SPEC | UNIT WT
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DRAWN R.W.W. 5/31/77
CHECKED A.W.W. 2/13/78
APPROVED A.J.A. 8/15/78
TRACED
DATE
DIAGRAM, SCHEMATIC
P.C. BOARD
SCALE
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING
RESEARCH LABORATORY
CHAMPAIGN, ILL.
DWG NO
17002

2

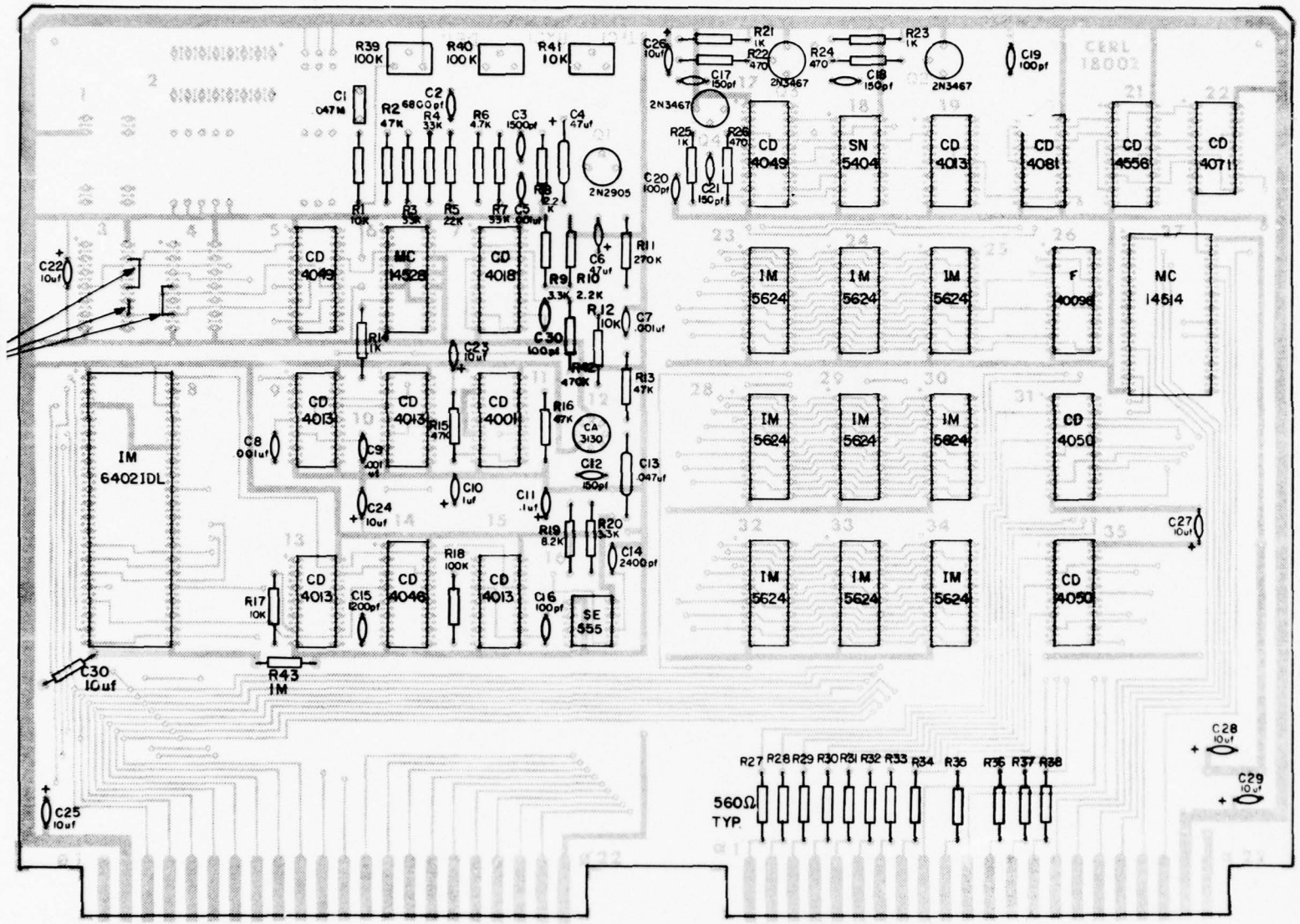
Table 16

Board Number 18002 -- Parts List

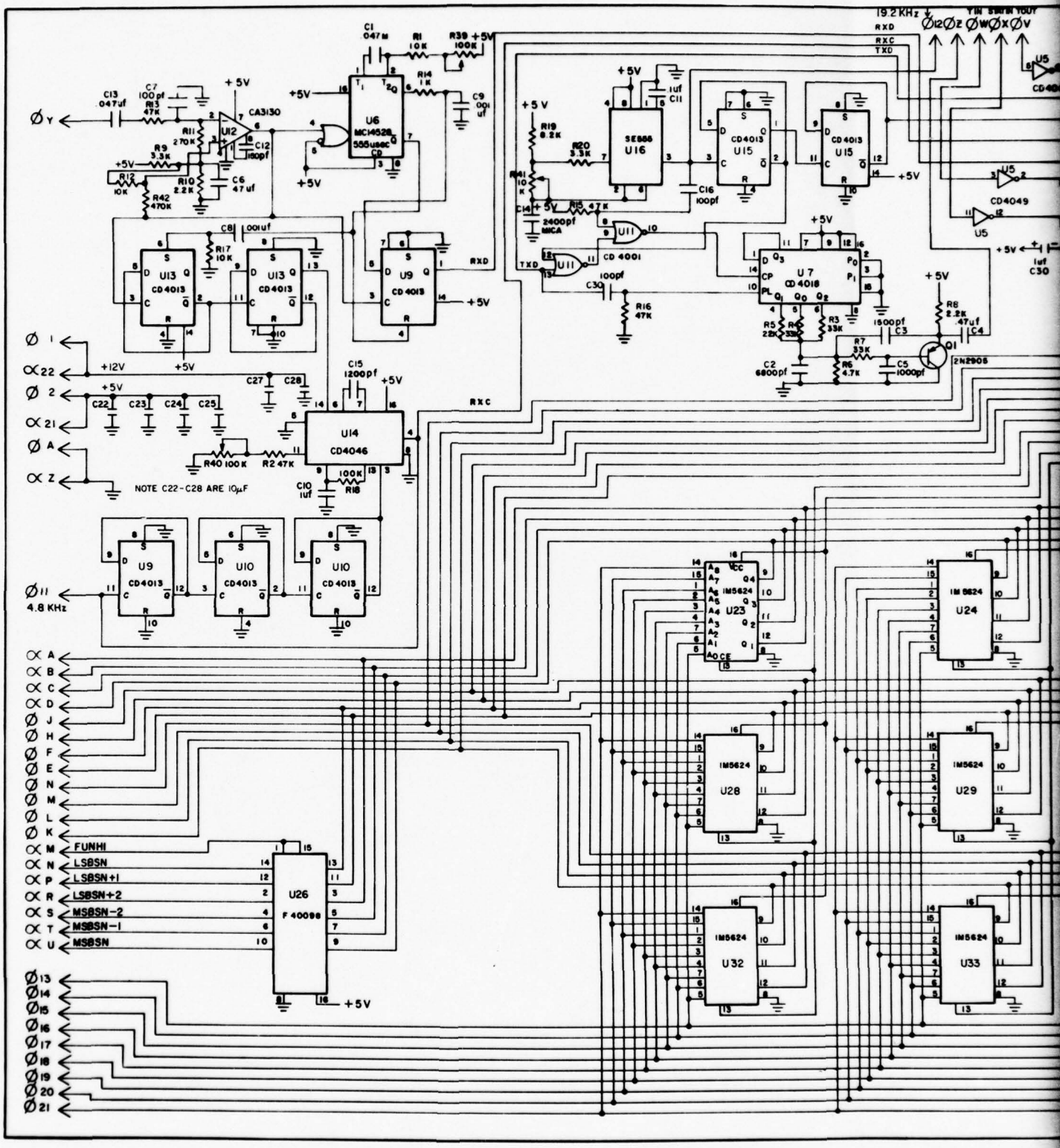
Circuit Diagram Reference	Component Type				
R22, R24, R26	Carbon	1/4W	5%	470	Ω
R27-R38	Carbon	1/4W	5%	560	Ω
R14, R21, R23, R25	Carbon	1/4W	5%	1	K Ω
R8, R10	Carbon	1/4W	5%	2.2	K Ω
R9, R20	Carbon	1/4W	5%	3.3	K Ω
R6	Carbon	1/4W	5%	4.7	K Ω
R19	Carbon	1/4W	5%	8.2	K Ω
R1, R12, R17	Carbon	1/4W	5%	10	K Ω
R5	Carbon	1/4W	5%	22	K Ω
R3, R4, R7	Carbon	1/4W	5%	33	K Ω
R2, R13, R15, R16	Carbon	1/4W	5%	47	K Ω
R18	Carbon	1/4W	5%	100	K Ω
R11	Carbon	1/4W	5%	270	K Ω
R42	Carbon	1/4W	5%	470	K Ω
R43	Carbon	1/4W	5%	1	M Ω
R41	Trimmer	Cermet		10	K Ω
R39, R40	Carbon	1/4W	5%	100	K Ω
C16, C19, C20, C30	Ceramic	100 pF		1	K V
C12, C17, C18, C21	Ceramic	150 pF		1	K V
C1	Mylar	.047 uF		100	V
C5, C7, C8, C9	Mylar	.001 uF		100	V
C15	Ceramic	1200 pF		1	K V
C3	Ceramic	1500 pF		1	K V
C14	Mica	2400 pF		500	V
C2	Ceramic	6800 pF		1	K V
C13	Ceramic	.047 uF		50	V
C11	Tantalum	.1 uF		35	V
C4	Tantalum	.47 uF		35	V
C10, C30	Tantalum	1 uF		35	V
C22-C29	Tantalum	10 uF		35	V
C6	Tantalum	47 uF		35	V
Q1	Silicon	PNP	2N2905		
Q2-Q4	Silicon	PNP	2N3467		
U5, U17	CD4009				
U6	MC14528				
U7	CD4018				
U8	IM6402IDL				
U9, U10, U13, U15, U19	CD4013				

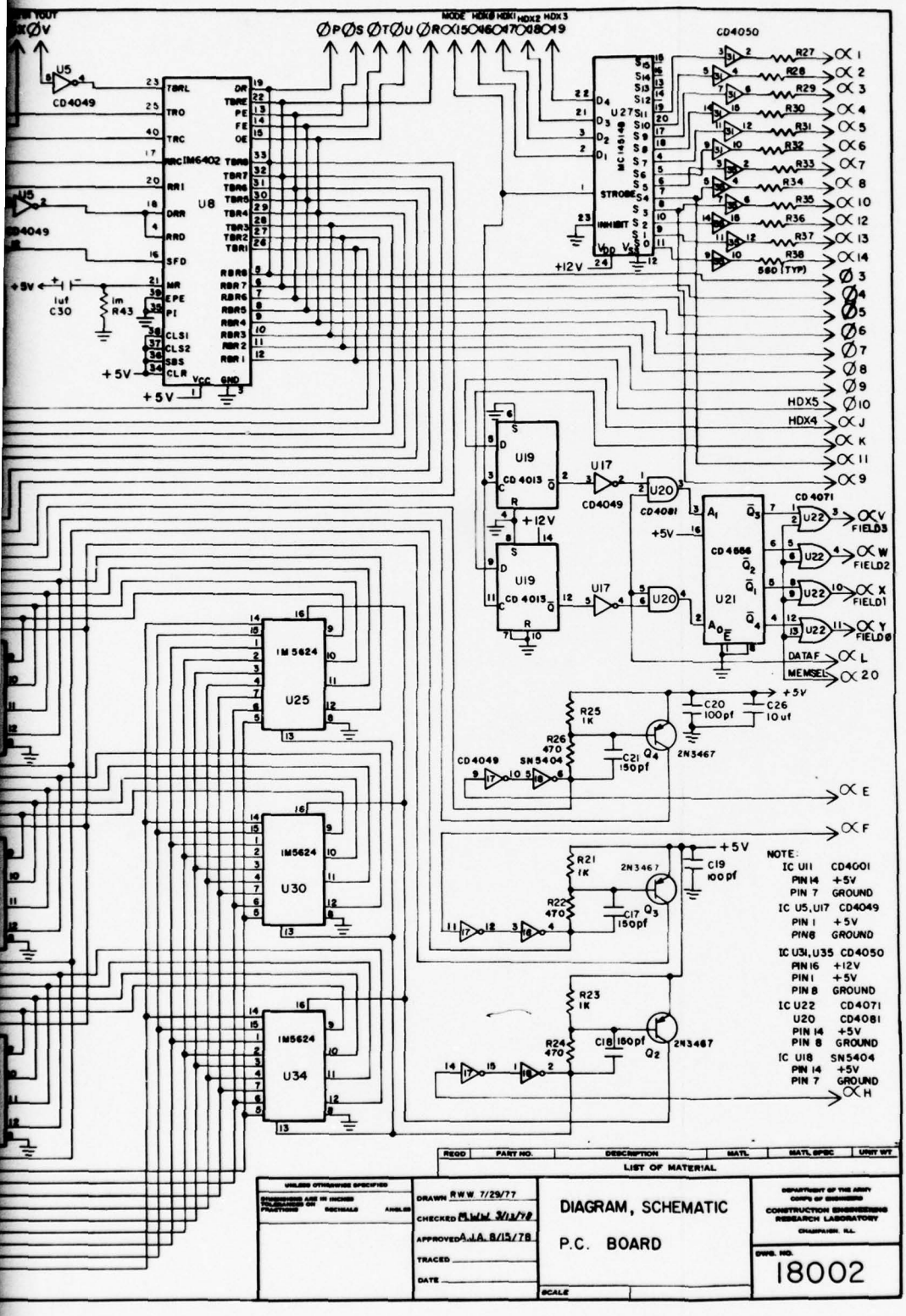
Table 16 (Cont'd)

Circuit Diagram Reference	Component Type
U11	CD4001
U12	CA3130AT
U14	CD4046
U16	SE555C Timer
U18	SN5404
U20	CD4081
U21	CD4556
U22	CD4071
U23-U25, U28-U30, U32-U34	IM5624
U26, U31, U35	F40098
U27	MC14514



NOTE: C22–C29 ARE BYPASS CAPACITORS.


NOTE C22-C28 ARE 10μF
4.8 KHz
19.2 KHz
RXD
RXC
TXD
FUNHI
LSBSN
LSBSN+1
LSBSN+2
MSBSN-2
MSBSN-1
MSBSN
+5V
+12V



REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

DRAWN	RWW 7/29/77
CHECKED	RWW 8/13/78
APPROVED	A.J.A. 8/15/78
TRACED	
DATE	

DIAGRAM, SCHEMATIC

P.C. BOARD

SCALE

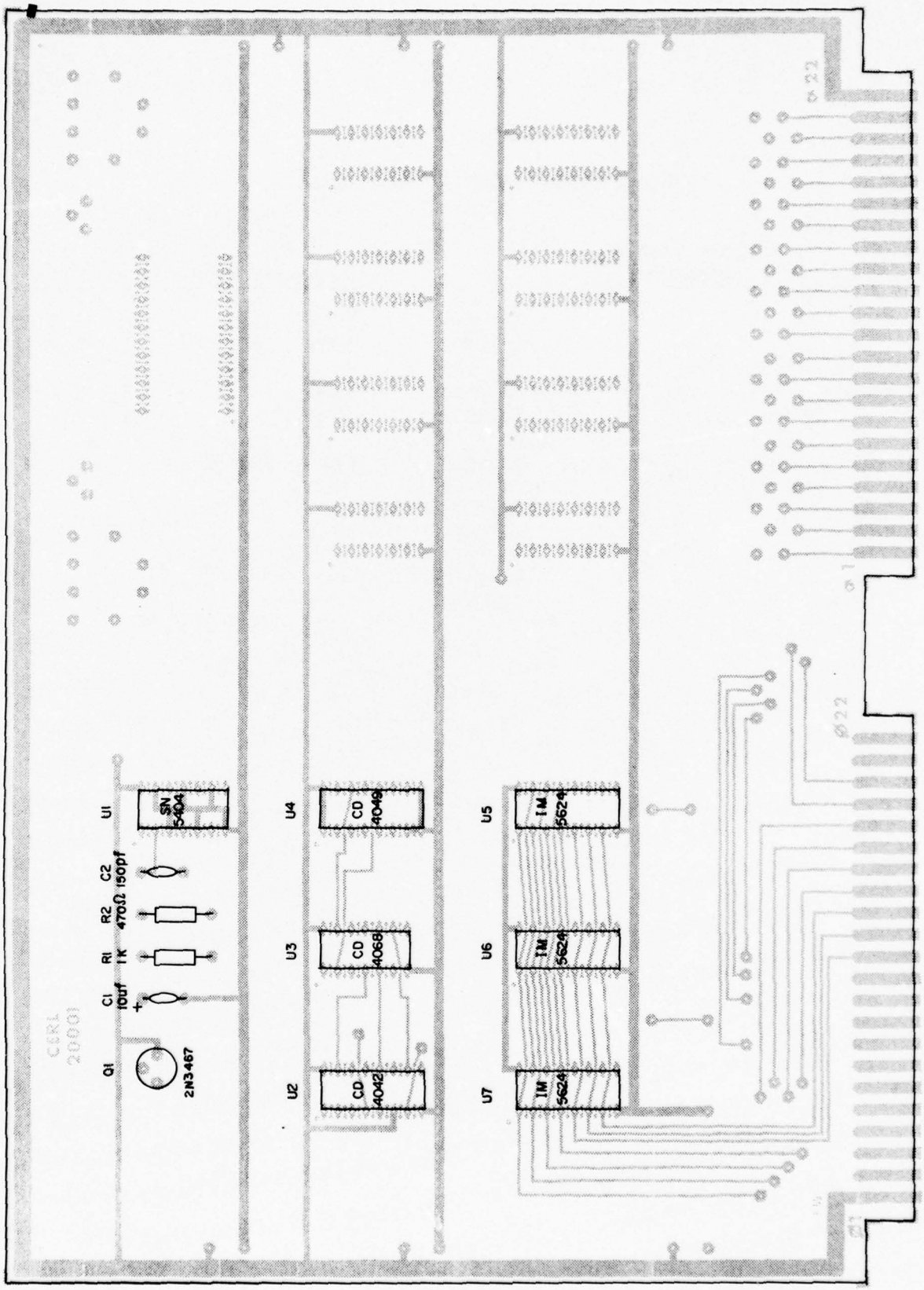
DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

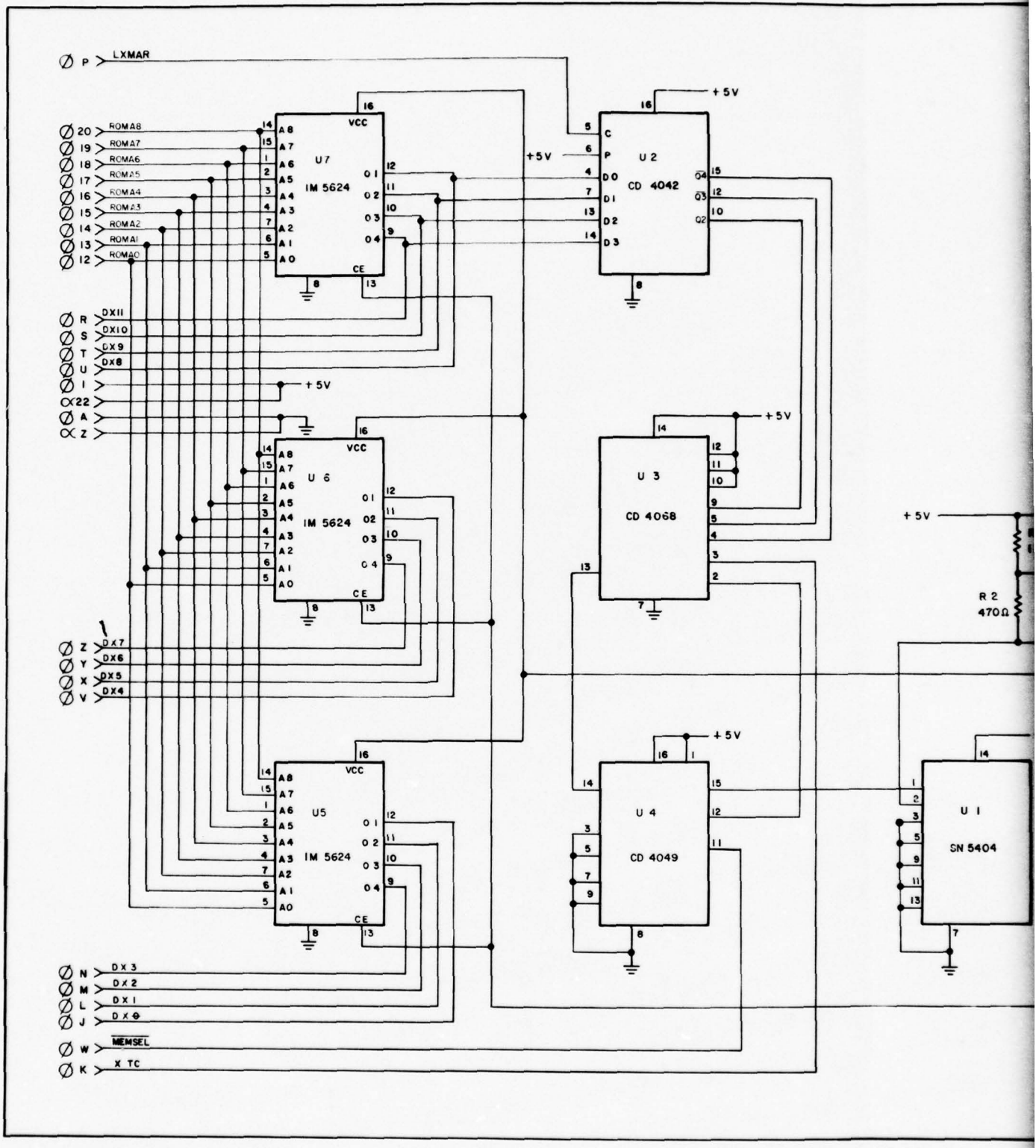
DWG. NO. 18002

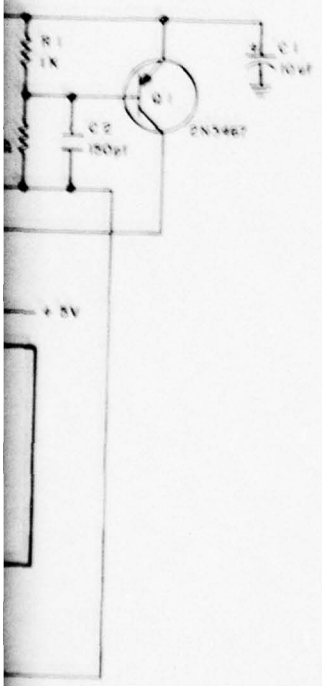
Table 17

Board Number 20001 -- Parts List

Circuit Diagram Reference	Component Type				
R2	Carbon	1/4W	5%	470	Ω
R1	Carbon	1/4W	5%	1	K Ω
C2	Ceramic	150 pF		1	K V
C1, C3-C5	Tantalum	10 uF		35	V
Q1	Silicon	PNP	2N3467		
U1	SN5404				
U2	CD4042				
U3	CD4068				
U4	CD4049				
U5-U7	IM5624				


CERL
2000
Q1
2N3467
C1
10uf
R1
1K
R2
470Ω
C2
150pf
U1
SN
5404
U2
CD
4042
U3
CD
4068
U4
CD
4049
U5
IM
5624
U6
IM
5624
U7
IM
5624
Ø22
Ø22


LXMAR
ROMA8
ROMA7
ROMA6
ROMA5
ROMA4
ROMA3
ROMA2
ROMA1
ROMA0
DX11
DX10
DX9
DX8
+5V
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
MEMSEL
X TC
U7
IM 5624
U6
IM 5624
U5
IM 5624
U2
CD 4042
U3
CD 4068
U4
CD 4049
U1
SN 5404
R 2
470Ω



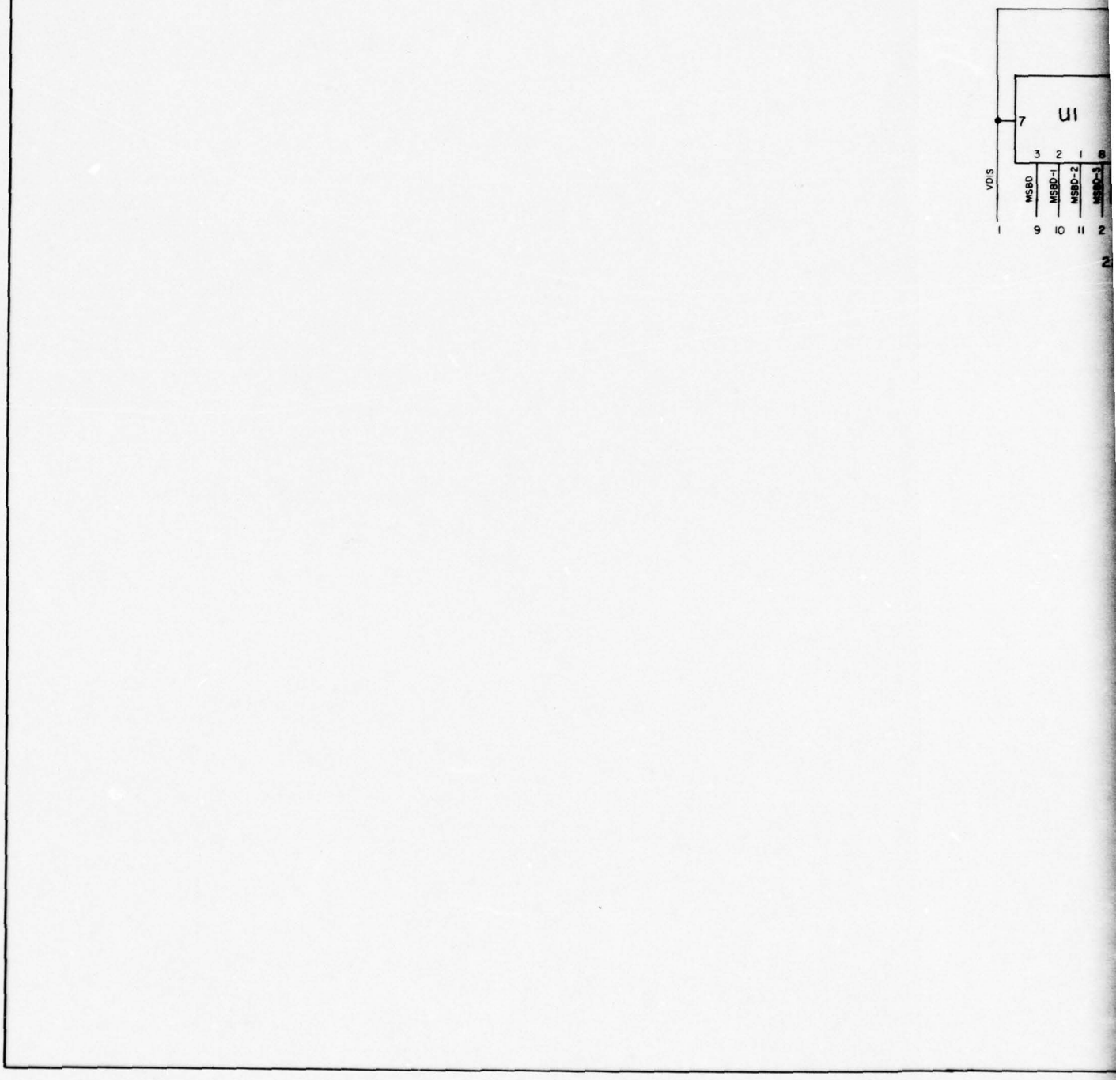
		SCHEMATIC, DIAGRAM P.C. BOARD	20001

2

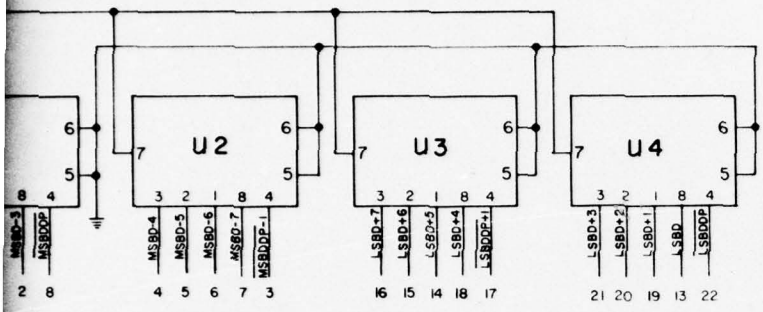
Table 18

Board Number 21001 -- Parts List

Circuit Diagram Reference	Component Type
U1-U4	HP5082-7300

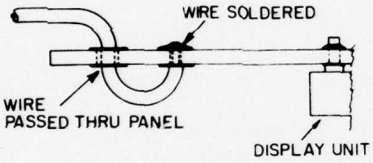

U1
7
3
2
1
VDIS
MSB0
MSB0-1
MSB0-2
MSB0-3
1
9
10
11
2

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

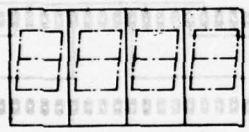


22 WIRES ATTACHED TO BOARD PER DETAIL-A

SCHEMATIC DIAGRAM



DETAIL A



HP5082-7300
NUMERIC INDICATOR (4)

PARTS LAYOUT

REQD	PART NO	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES ON FRACTIONS ___ DECIMALS ___ ANGLES ___	DRAWN J.H.O 9/23/78 CHECKED APPROVED A.J.A 9/23/78 TRACED DATE	DISPLAY BOARD SCALE	DEPARTMENT OF THE ARMY CORPS OF ENGINEERS CONSTRUCTION ENGINEERING RESEARCH LABORATORY CHAMPAIGN ILL. DWG NO. 21001

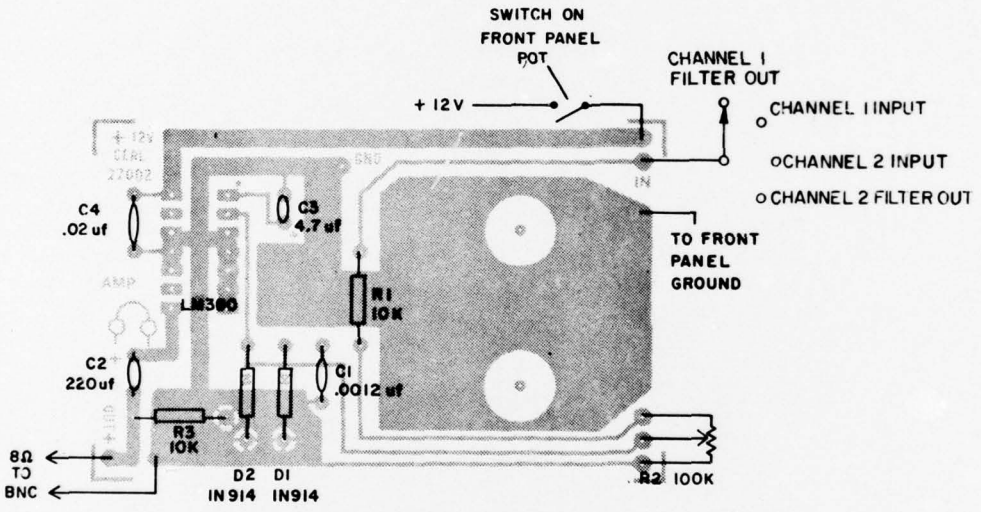
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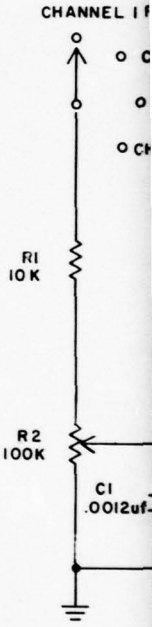
2

Table 19

Board Number 22002 -- Parts List

Circuit Diagram Reference	Component Type				
R1, R3	Carbon	1/4W	5%	10	K Ω
R2	Carbon Potentiometer with Switch		1W	100	K Ω
C1	Ceramic	1.2nf		100	V
C4	Ceramic	20 nf		100	V
C3	Tantalum	4.7μf		35	V
C2	Aluminum	220 μf		25	V
D1, D2	Silicon Diode		IN914B		
U1	LM380N				





REQD	PART NO.

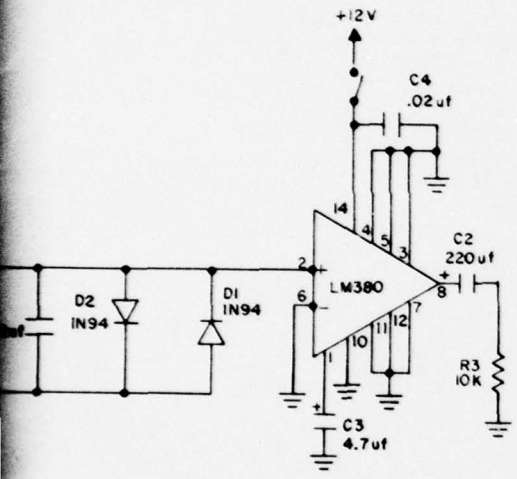
UNLESS OTHERWISE SPECIFIED	
DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN CHECKED APPROVED A.J.A. 8/15/78 TRACED DATE

I FILTER OUT

CHANNEL 1 INPUT

O CHANNEL 2 INPUT

CHANNEL 2 FILTER OUT



	DESCRIPTION	MATL	MATL SPEC	UNIT WT

LIST OF MATERIAL

HEADPHONE AMPLIFIER

DEPARTMENT OF THE ARMY
CORPS OF ENGINEERS
CONSTRUCTION ENGINEERING RESEARCH LABORATORY
CHAMPAIGN, ILL.

DWG. NO.
22002

SCALE

7 CABLES AND CONNECTORS WIRING LISTS

The following are lists of wiring between the chassis and all connectors on the chassis and the wiring from connectors on the chassis to the side connectors. If a specific device is to be connected to one of the side connectors (for example, the monitor is designed so that a data printer can be connected to the output side connector), then the wiring is also given from the side connector to the device.

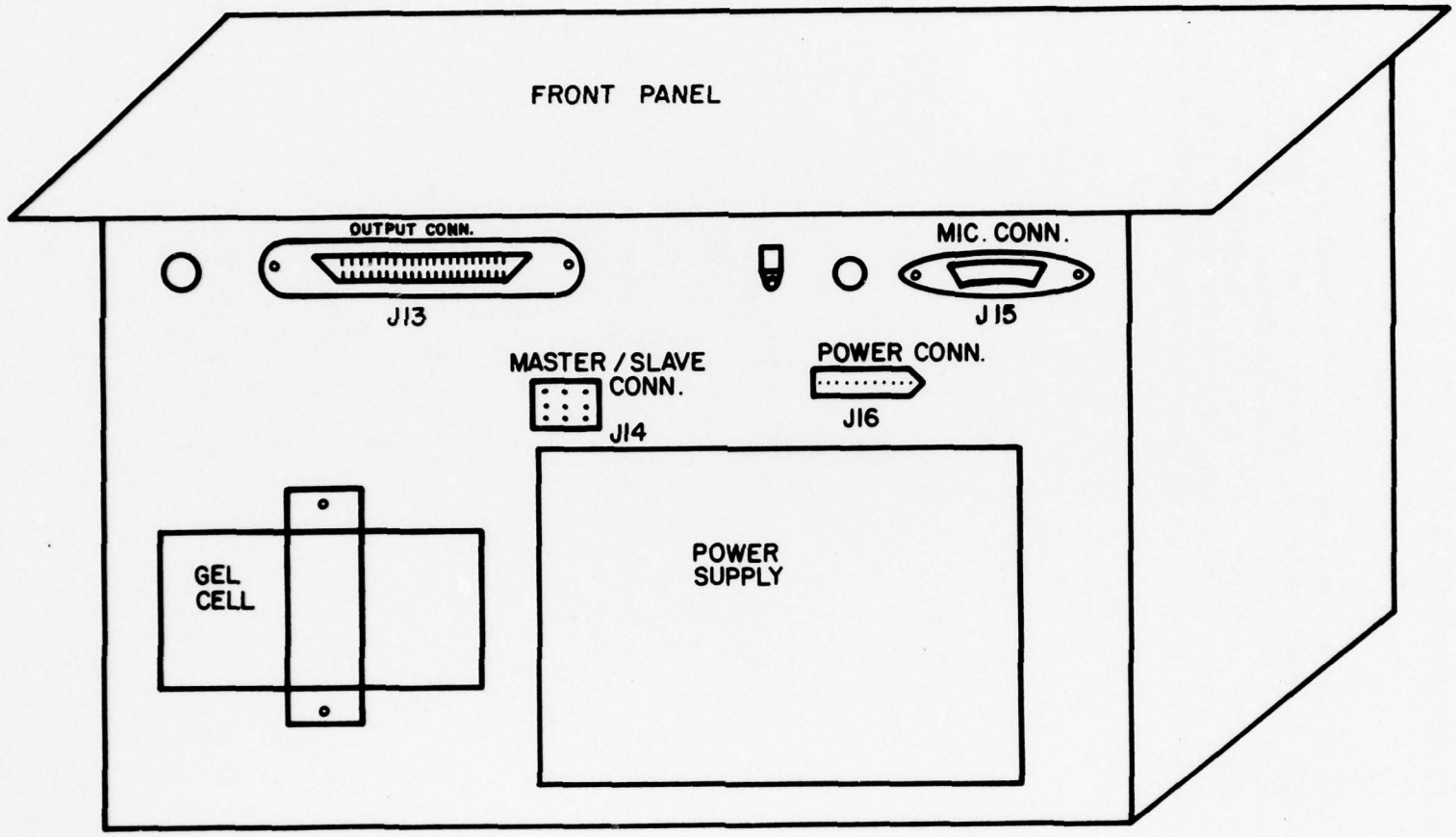


Figure 2. Layout of chassis connectors.

Table 20

Chassis to Side Connector Output

Monitor Signal Name	Chassis Connection	50 Pin Output Connector J13	Cable Color Code 52 Wire	48 Pin Side Conn. J17
PIO 36	12αE	31	WH/RED & ORG	A
PIO 35	12α6	33	ORG/WH & BLUE	B
PIO 34	12αF	6	BLUE/WH & ORG	C
PIO 33	12α5	44	GRN/WH & BLK	D
PIO 32	12αD	21	ORG/BLK & WH	E
PIO 31	12αK	10	WH/RED & BLUE	F
PIO 30	12α7	30	BLK/WH & GRN	G
PIO 29	12α2	16	BLUE/BLK	H
PIO 28	12α4	35	BLK/RED	J
PIO 27	12αJ	1	GRN	K
PIO 26	12α3	25	BLUE/WH & BLK	L
PIO 25	12αH	5	WH/BLK & GRN	M
PIO 24	12αM	49	RED/WH & BLUE	N
PIO 23	12α13	42	RED/BLK & GRN	P
PIO 22	12αN	40	GRN/BLK & ORG	Q
PIO 21	12α12	46	ORG/BLK	R
PIO 20	12αL	18	BLK	S
PIO 19	12αS	27	BLK/GRN & RED	T
PIO 18	12α14	22	RED/WH	U
PIO 17	12α9	7	GRN/WH & BLUE	V
PIO 16	12α11	20	WH/GRN & RED	W
PIO 15	12αR	2	WH/BLK & RED	X
PIO 14	12α10	4	RED/WH & BLK	Y
PIO 13	12αP	9	GRN/BLK	Z
PIO 12	12αU	43	RED	a
PIO 11	12α20	23	WH	b
PIO 10	12αV	12	ORG	c
PIO 9	12α19	14	GRN/WH	d
PIO 8	12αT	3	BLUE/RED & ORG	e
PIO 7	12αY	38	BLK/ORG & RED	f
PIO 6	12α21	11	ORG/GRN	g
PIO 5	12α16	39	BLK/WH & RED	h
PIO 4	12α18	24	RED/BLK	j
PIO 3	12αX	45	BLUE	k
PIO 2	12α17	13	BLUE/WH	l
PIO 1	12αW	34	RED/GRN	m
$\overline{\text{PRINT}}$	11αN	36	SHIELDED WIRE	z
$\overline{\text{DATA REQUEST}}$	15α6	15	ORG/BLUE & RED	t
LOGIC GND	P.S. DIG GND	41	GRN/RED & ORG	u

Table 20 (Cont'd)

Monitor Signal Name	Chassis Connection	50 Pin Output Connector J13	Cable Color Code 52 Wire	48 Pin Side Conn. J17
LOGIC GND	P.S. DIG GND	37	ORG/RED	v
LOGIC GND	P.S. DIG GND	17	BLK/WH & BLUE	w
+5 V	P.S. +5V	26	WH/BLK & BLUE	x
KEY PRINT	15αV	19	BLUE/RED	n
WINDY W	11α17	50	BLUE/RED & GRN	p
SHIELD	P.S. DIG GND	28	SHIELD	y
CHASSIS DIG GND	P.S. DIG GND	32	WH/RED	q
PSEL 2	15α 4	47	WH/BLK	r
PSEL 1	15α T	8	ORG/BLK & GRN	s
		48	ORG/GRN & RED	
		29	BLK/WH & ORG	

Table 21

Monitor Chassis to B&K 4921

Microphone 1

Monitor Signal Name	Monitor Connection	14 Pin Mic Conn. J15	Wire Type	Mic. 1 Monitor Side Conn. J19	Cable Color Code (Shielded)	B&K 4921 Connector	B&K 4921 Signal Name
CHASSIS	CHASSIS DIGITAL GROUND	10	BLK 24 GAUGE	J	WH/YEL	3	CASE GROUND
GROUND P.S.	P.S. DIGITAL GND	9	BLK 24 Gauge	A	WH/BLK	7	GROUND
ANALOG INPUT SEL. GND	1φ4	8	SHIELD	B	{SHIELD OF WH/BLK SHIELD OF WH/RED}	7	GROUND
ANALOG INPUT SEL.	1φD	1	SHIELDED WIRE	C	WH/RED	8	SIGNAL OUTPUT
+12 V	P.S. +12 V	3	RED 24 GAUGE	N	RED	{9 16}	+EXT. BATT. HEATER
GROUND P.S.	P.S. DIGITAL GND	9	BLK 24 GAUGE	M	BLK	10	-EXT. BATT.
MIC CAL RELAY	16 ∝ M	2	STRANDED GRN 24 GAUGE	D	WH/GRN	11	CAL. START
					FROM PIN 10 THRU 47 Ω	15	HEATER
WIND METER SW TO 18 K Ω	F.P. SW24	4	STRANDED YELLOW 24 GAUGE	H	WH	17	WIND DETECTOR
WIND METER SW TO 587 Ω	F.P. SW24	11	STRANDED	L	GRN	18	WIND DETECTOR

Table 21 (Cont'd)

MICROPHONE 2

Monitor Signal Name	Monitor Connection	14 Pin Mic Conn. J15	Wire Type	Mic. 2 Monitor Side Conn. J20	Cable Color Code (Shielded)	B&K 4921 Connector	B&K 4921 Signal Name
CHASSIS	CHASSIS DIGITAL GND	12	BLK 24 GAUGE	J	WH/YEL	3	CASE GROUND
GROUND P.S.	P.S. DIGITAL GROUND	13	BLK 24 GAUGE	A	WH/BLK	7	GROUND
ANALOG INPUT SEL. SND	1 α 4	14	SHIELD	B	{SHIELD OF WH/BLK, SHIELD OF WH/RED}	7	GROUND
ANALOG INPUT SEL.	1 α D	7	SHIELDED WIRE	C	WH/RED	8	SIGNAL OUTPUT
+12 V	P.S. +12 V	5	RED 24 GAUGE	N	RED	{9, 16}	+EXT. BATT. HEATER
GROUND P.S.	P.S. DIGITAL GROUND	13	BLK 24 GAUGE	M	BLK	10	-EXT. BATT.
MIC CAL RELAY	16 α M	6	STRANDED GRN 24 GAUGE	D	WH/GRN	11	CAL. START
WIND METER SW TO 18 K Ω	F.P. SW 24	J19 PIN H		H	WH	17	WIND DETECTOR
WIND METER SW TO 587 Ω	F.P. SW 24	J19 PIN L		L	GRN	18	WIND DETECTOR
					FROM PIN 10 THRU 47 Ω	15	HEATER

Table 22

Monitor to Master/Slave Connector

Monitor Connection	9 Pin Molex Connector J14	Cable Color Code	Monitor Side Connector J21	Monitor Signal Name Slave/Master
F.P. SW22 LEFT SIDE	7	WH	A	START/THRESH-UP
F.P. SW22 RIGHT SIDE	8	YEL	B	SAMPLE/THRESH-DOWN
	3	RED	C	
17 α K	2	ORG	D	$\overline{\text{WINDY BUS}}$
	1	BLUE	E	
	5	BROWN	F	
GROUND	4	BLK	H	GROUND
	6	GRN	J	

Table 23

Power Connectors: Chassis to Side Connector

Power Supply Connection (See Diagram)	5 Pin Chassis Power Connector J16	5 Pin Side Connector J18
+12 V	1	D
+12 V Ground	2	C
120 V AC Hot	3	E
120 V AC Cold	4	A
3RD Wire Ground	5	B

Table 24

Mini Sample Tape Control Connector

Pin	Signal	Wire to
1	Windy Bus	9 α 21
2	Ground	Digital Ground
3		
4	Tape Motor Hi	180C
5	Tape Motor Lo	180D
6		
7	+5	+5 volts

Schomer, Paul D
True-integrating environmental noise monitor and sound exposure level meter / by P. D. Schomer, A. J. Averbuch, M. W. Weisberg. -- Champaign, Ill. : Construction Engineering Research Laboratory ; Springfield, Va : available from National Technical Information Service , 1978 - 79.
2v. : ill. ; 27 cm. (Technical report - Construction Engineering Research Laboratory ; N-41)

1. Noise-measurement. I. Averbuch, Aaron J. II. Weisberg, M. W. III. Title. IV. Series: U.S. Construction Engineering Research Laboratory. Technical report ; N-41.

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