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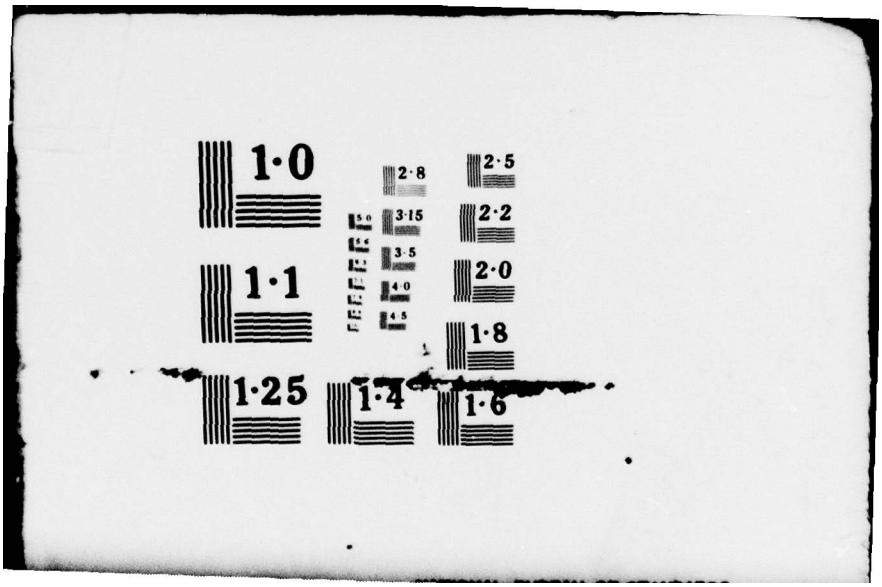
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EFFECT OF ANNEALING TEMPERATURES ON TCR AND RESISTANCE VALUES FOR DC SPUTTERED Cr-Si THIN FILM RESISTORS

(10) BY HAYDEN MORRIS
HENRY RHODES

UNDERWATER SYSTEMS DEPARTMENT

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Thin film high value resistors (>1000Ω/□) composed of a silicon-chromium mixture were sputter deposited under d.c. conditions in argon on to 99.6% as-fired alumina substrates. Reported are effects on TCR and resistor values which resulted from the variation of annealing temperatures. The resistors are for use in the fabrication of hybrid microcircuits intended for circuit applications which involve low power, low noise, digital and linear design requirements.

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SUMMARY

This report concerns thin film high value resistors (>1000 Ω/□) composed of a chromium-silicon mixture and sputter deposited under DC conditions in argon on 99.6% as-fired alumina substrates. Reported are effects on TCR and resistor values which resulted from the variation of annealing temperatures. The resistors are for use in the fabrication of hybrid microcircuits intended for circuit applications which involve low power, low noise, digital and linear design requirements.

Edward C. Whitman

E. C. WHITMAN
By direction

ACKNOWLEDGEMENTS

The CLIP-2 circuit used in this work is based on a circuit design developed by R. Quintero. The progress of the work was aided by the efforts of M. C. Marlow in carrying out various phases of the processing.

CONTENTS

ILLUSTRATIONS

INTRODUCTION

The design of low noise and low power hybrid microcircuits requires the use of high value thin film resistors with a temperature coefficient of resistance (TCR) value as close to zero as possible, such as ±10 parts per million per degree centigrade change in temperature (ppm/°C). Many techniques have been developed to form high value resistors on a substrate by the vacuum deposition of dielectric or semiconductor materials mixed in various ratios with metallic materials. It has been found that thin film resistors with specific resistivity and TCR values resulted from particular processes. The resistor characteristics were reported to be determined by process parameters such as the manner and rate of deposition, the substrate material, the substrate temperature, the resistive material, etc.

The development of chromium-silicon thin film resistor technology for monolithic silicon integrated circuit fabrication has been reported by Youmans[1] using vacuum deposition techniques, and later by Waits[2] using DC sputtering techniques. The results reported by Waits using various Cr-Si mixtures and DC sputter deposition techniques became of interest to the thin film hybrid microcircuit work because of the resistivity and TCR values which were obtained. A reference was made by Waits[3] to the deposition of Cr-Si resistor films on alumina ceramic substrates, as in the fabrication of hybrid microcircuits, but the results were not discussed in detail. The mixture ratios of chromium in silicon which Waits deposited ranged from 17.0 to 33.0 atomic percent chromium. As the ratio of chromium was increased, the resistivity was reported to decrease from 0.1 to 0.001 ohm-cm and the TCR changed from -1500 to +500 ppm/°C. In particular, it was found that for a mixture containing 27 atomic

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1. Youmans, Albert P., "Thin Film Resistor," U.S. Patent 3,381,255, patented 30 April 1968.

2. Waits, Robert K., "Sputtered Silicon-Chromium Resistive Films," Journal of Vacuum Science and Technology, Vol. 6, No. 2, 1968, p. 308.

3. Waits, Robert K., "Silicide Resistors for Integrated Circuits," Proceedings of the Institute of Electrical and Electronics Engineers, Inc., Vol. 59, No. 10, October 1971, p. 1425.

percent of chromium, the resistivity was about 7.4×10^{-3} ohm-cm and the average TCR was near zero. The post deposition annealing process to stabilize resistors was conducted in a nitrogen atmosphere at 550°C because that is the temperature necessary to alloy aluminum contacts to the silicon-integrated circuit. The results reported by Waits for Cr-Si mixtures are similar to those for mixtures of Cr-SiO reported by Glang et al,[4] Neugebauer,[5] and also Gasperic and Navinsek,[6] i.e., the TCR becomes more positive as the resistivity decreases, and the resistivity decreases as the metallic content increases.

Adapting a technology for another application can produce different characteristics for a thin film resistor material. This results from factors such as macroscopic changes in the films due to different deposition or processing parameters, and differences in substrate parameters such as thermal coefficients of expansion and surface roughness. The work reported here describes the differences in Cr-Si thin film resistor characteristics when hybrid microcircuit fabrication processing on alumina ceramic is used instead of silicon integrated circuit processing. In addition, other observations are presented and possible causes for the differences in film characteristics are discussed.

PROCEDURES AND RESULTS

Experimental Procedure

In the work reported here, 27 atomic percent chromium in silicon films were sputter deposited using argon gas under DC voltage conditions in an oil diffusion pumped vacuum chamber. The substrates on which the resistor films were deposited were as-fired 99.6% alumina with dimensions of .750 x .750 x .030 inches. The substrates were prepared for the deposition by one of two cleaning processes. One method employed was to scrub the substrates with detergent using a cotton swab and then placing them in a detergent ultrasonic bath for fifteen minutes. Next, they were rinsed several times with distilled water and agitated ultrasonically. After blow drying them in air, they were placed in boiling trichloroethylene for 15 minutes, followed by a 5-minute room temperature acetone bath, which was followed by 15 minutes in boiling H_2O_2. The next step was several ultrasonic rinses in distilled water followed by an ultrasonic bath in isopropyl alcohol after which they were blown dry and placed in an 85°C oven for one

4. Glang, R., Holmwood, R. A., and Herd, S. R., "Resistivity and Structure of Cr-SiO Cermet Films," Journal of Vacuum Science and Technology, Vol. 4, No. 4, P. 163.

5. Neugebauer, C. A., "Resistivity of Cermet Films Containing Oxides of Silicon," Thin Solid Films, Vol. 6, 1970, p. 443.

6. Gasperic, J., and Navinsek, B., "Some Electrical Properties of Thin Cermet Films," Thin Solid Films, Vol. 36, 1976, p. 353.

hour before being placed in the deposition chamber. The second and preferred cleaning method starts out the same with swabbing the substrate using detergent. This was followed by a detergent ultrasonic bath, then several rinses in distilled water with ultrasonic agitation followed by an ultrasonic rinse in isopropyl alcohol for 15 minutes. After this, they were blown dry and placed in an air oven at 1000°C for at least ten minutes. The substrates were placed on the substrate table in the deposition chamber after the oven temperature had been lowered to 100°C. The chamber was evacuated to a pressure of at least 5×10^{-7} Torr (6.67×10^{-5} Pa) and after the throttle valve was actuated, argon pressure was leaked in and set at 5.6×10^{-3} Torr (7.5×10^{-1} Pa) as measured on a thermocouple gauge in the deposition chamber. The Cr-Si sputtering target (13 cm in diameter) was sputtered for at least 25 minutes at 2.5 kV DC prior to deposition. After the presputtering, and since there was no mechanical shutter in the chamber, the discharge was turned off and the substrate table was rotated into position under the target with a separation distance of three centimeters. The discharge was then restarted at a target potential of 1250 or 1500 volts as desired. The deposition rates were 1.5 and 2.5 angstroms/second for the respective voltages and the films were deposited to a thickness of at least 400 angstroms. The thickness was measured using Tolansky interferometry methods on a glass slide which had been masked mechanically during the deposition. After deposition, the films were overcoated in a vacuum chamber with the contact metal film. At first, chromium and gold were used as the conductor/contact metal, however, it was found that the contact to the resistor films was not ohmic and this resulted in data which was inconsistent. For this reason the titanium, palladium, gold metallurgy was tried as the contact/conductor film and results were excellent. The metallization film thicknesses were 700Å, 2000Å, and 12000Å, respectively. The next steps in the processing were to delineate the conductor and resistor patterns using photolithography and chemical etching along with R.F. sputter etching. A resistor test pattern used in this work is shown in Figure 1, and a circuit pattern is shown in Figure 2. The resistor values were measured before and after various annealing temperatures to determine the effects on resistor and TCR values. The annealing cycles were carried out in a two-inch diameter single zone tube furnace having a heated zone 12 inches in length and with electronic feedback control of the heated zone. The temperature profile of the heated zone is shown in Figure 3. The substrates were placed within a four-inch length at the center of the heated zone, with argon or nitrogen flowing into one end of the tube at a rate of one standard cubic foot per hour (SCFH). The TCR value was determined by measuring the resistance at 50°C and then 150°C and calculating the TCR from the following equation where R_1 is measured at 50°C and R_2 is measured at 150°C.

$$\alpha \ (\text{ppm}/^{\circ}\text{C}) = 10^4 \left(\frac{R_2}{R_1} - 1 \right)$$

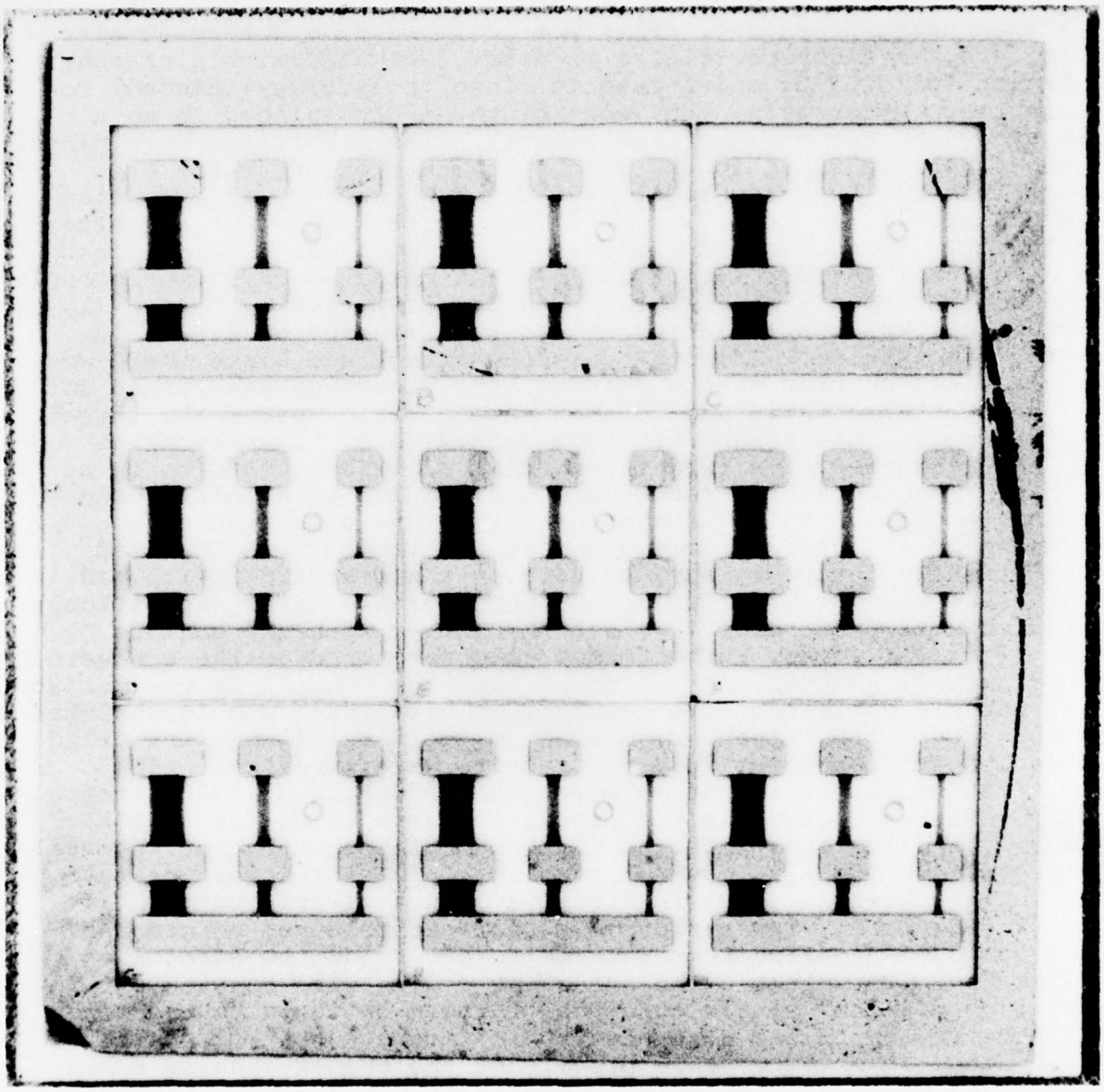

Figure 1

Resistor Test Pattern

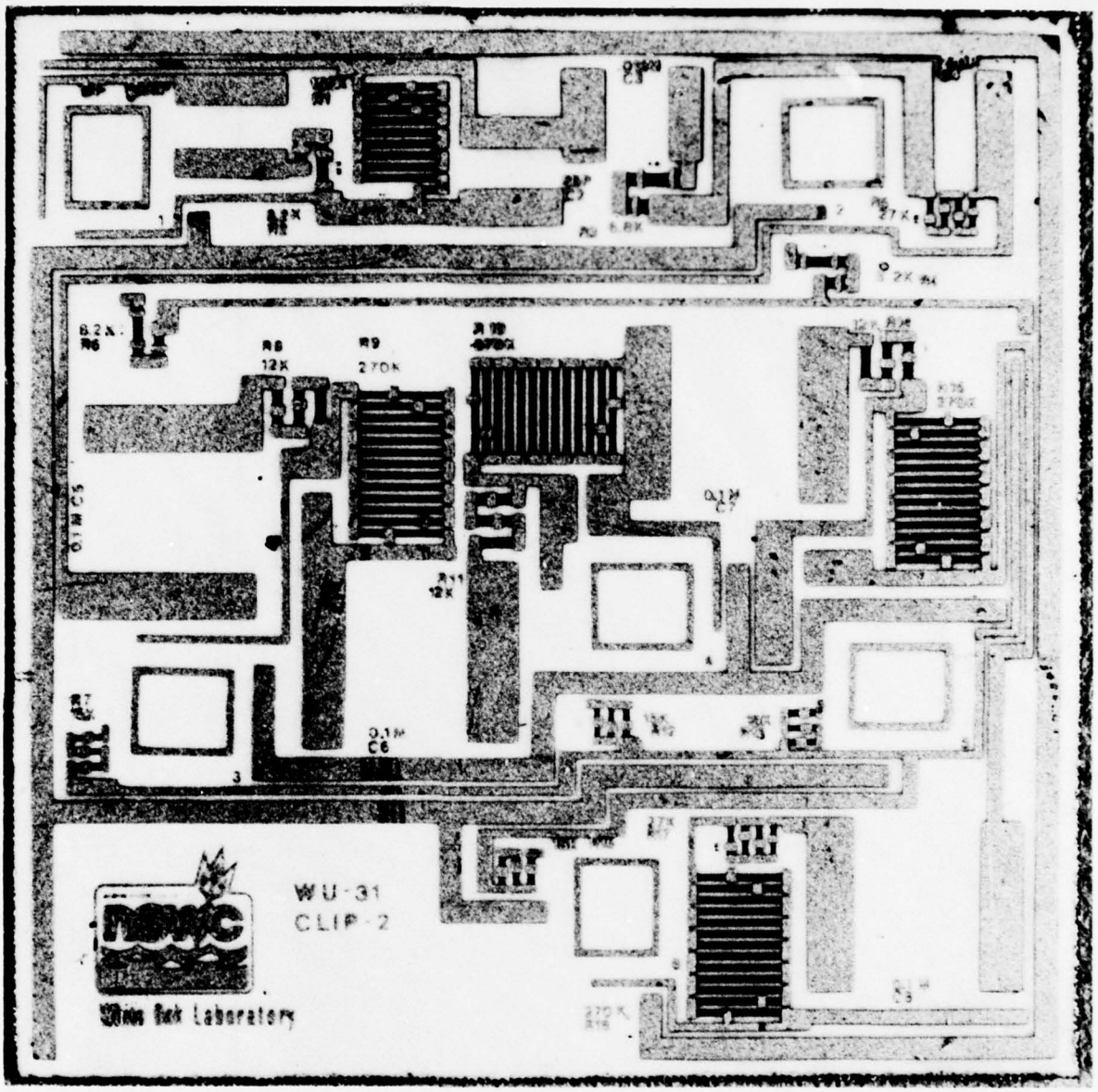

Figure 2

CLIP-2 Circuit Pattern

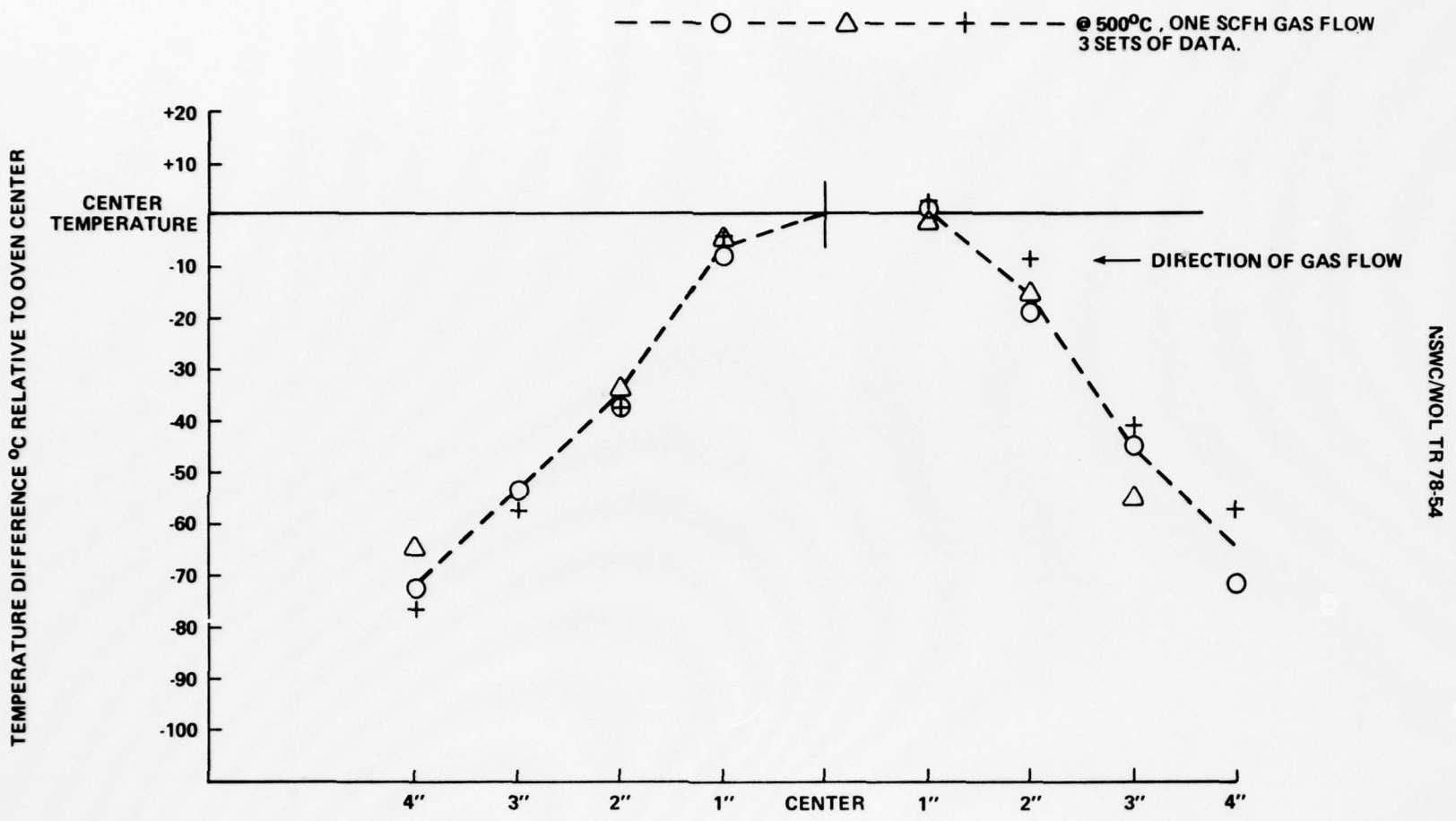

FIGURE 3. 2" SINGLE ZONE TUBE FURNACE TEMPERATURE PROFILE

No attempt was made to analyze the films to determine macroscopic and crystalline changes resulting from the various annealing temperatures.

Results

The effect of annealing temperatures on resistor values is shown for typical resistors in Figure 4, where the percent change in resistor values from the as-deposited value is plotted for specific annealing temperatures. The data plotted for the 470°C and 535°C annealing temperatures is presented to show the extremes of variation for four substrates from different deposition runs. At temperatures somewhere above 535°C, the metallization began to diffuse along the resistor causing resistor values to vary over a wide range for a run and therefore not to be reproducible with any accuracy. The variation of temperature as a function of time for a typical annealing cycle is shown in Figure 5.

The temperature coefficient of resistance was found to change also as a function of the annealing temperature, becoming more positive as the annealing cycle temperature was increased. At a temperature in the range of 485°C, the temperature coefficient of resistance was in the range of zero (±10). In Figure 6, data is plotted for typical resistors deposited at rates of 1.5 and 2.5 Å/sec showing the temperature coefficients of resistance resulting from various annealing temperatures. Some of the data shown is for resistors subjected to a single annealing temperature, while other data is for typical resistors subjected to several annealing cycles in sequence. It should be mentioned that several substrates were subjected to annealing in air atmosphere after being annealed in argon at the same temperature, with the result that resistivity was increased by from 9% to 13% and the TCR value changed typically by a factor greater than two, such as from +15 to +37 ppm/°C. At present, a set of data has not been obtained for air annealing at various temperatures.

In comparing results with those obtained by Waits for 27 atomic percent Cr films for monolithic integrated circuits, one finds that the resistivity values are in the same range, 4.74×10^{-2} to 1.1×10^{-2} ohm-cm, after consideration of surface roughness and differences in effects of annealing cycles.

However, the zero temperature coefficient of resistance was obtained at an annealing temperature lower than that for silicon monolithic integrated circuits, 485°C compared with 550°C. As to the reason why there are changes in TCR as a result of post deposition annealing conditions, one can only speculate since the films in this work were not analyzed to determine crystalline changes. The work by Waits reported that the diffraction patterns became sharper and lines indicating Cr were observed after the films were annealed at 550°C in N_2. The work reported tends to support that observation since as the annealing temperature increased, the TCR becomes more

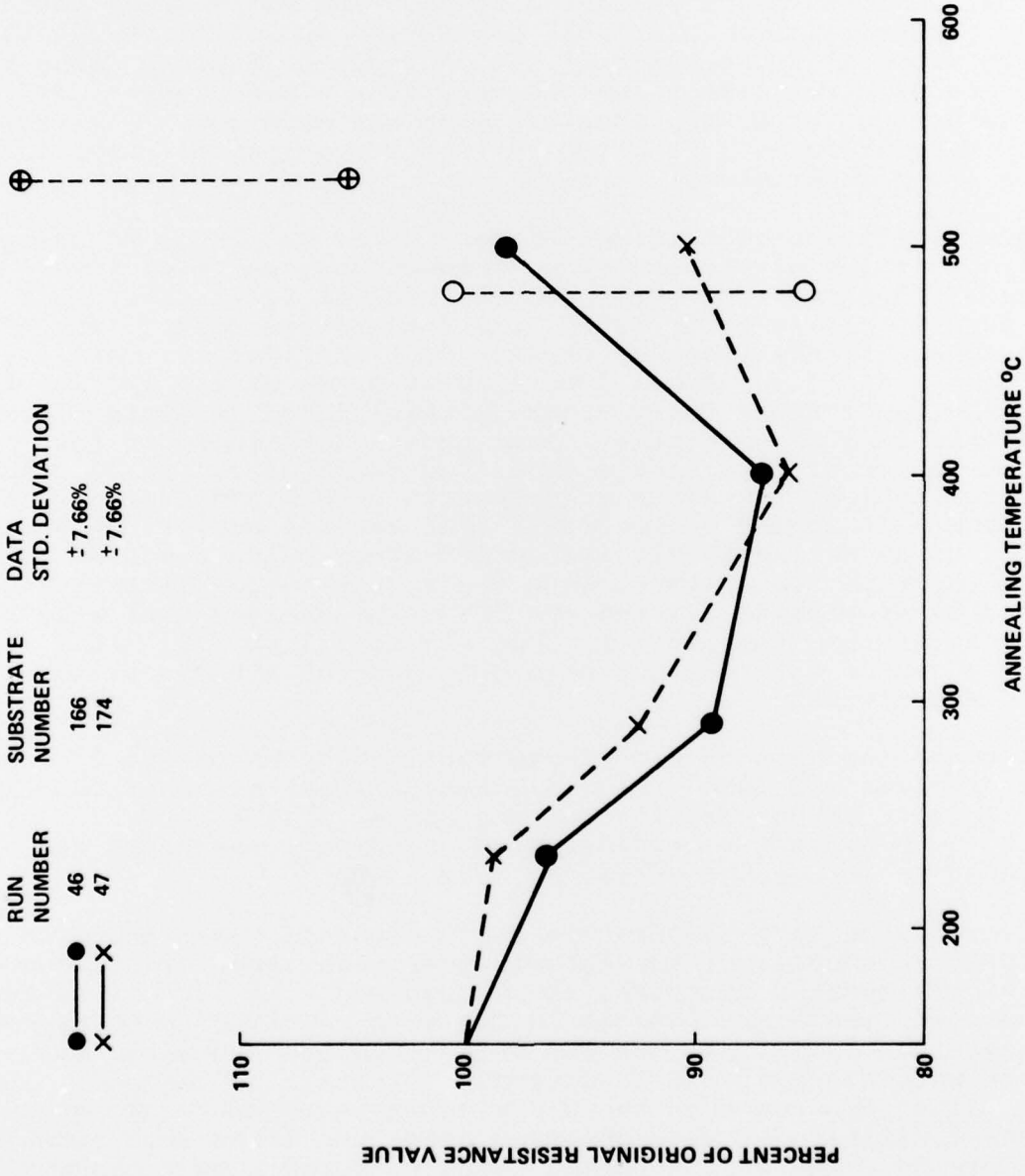

FIGURE 4. VARIATION IN RESISTIVITY VS. ANNEALING TEMPERATURE

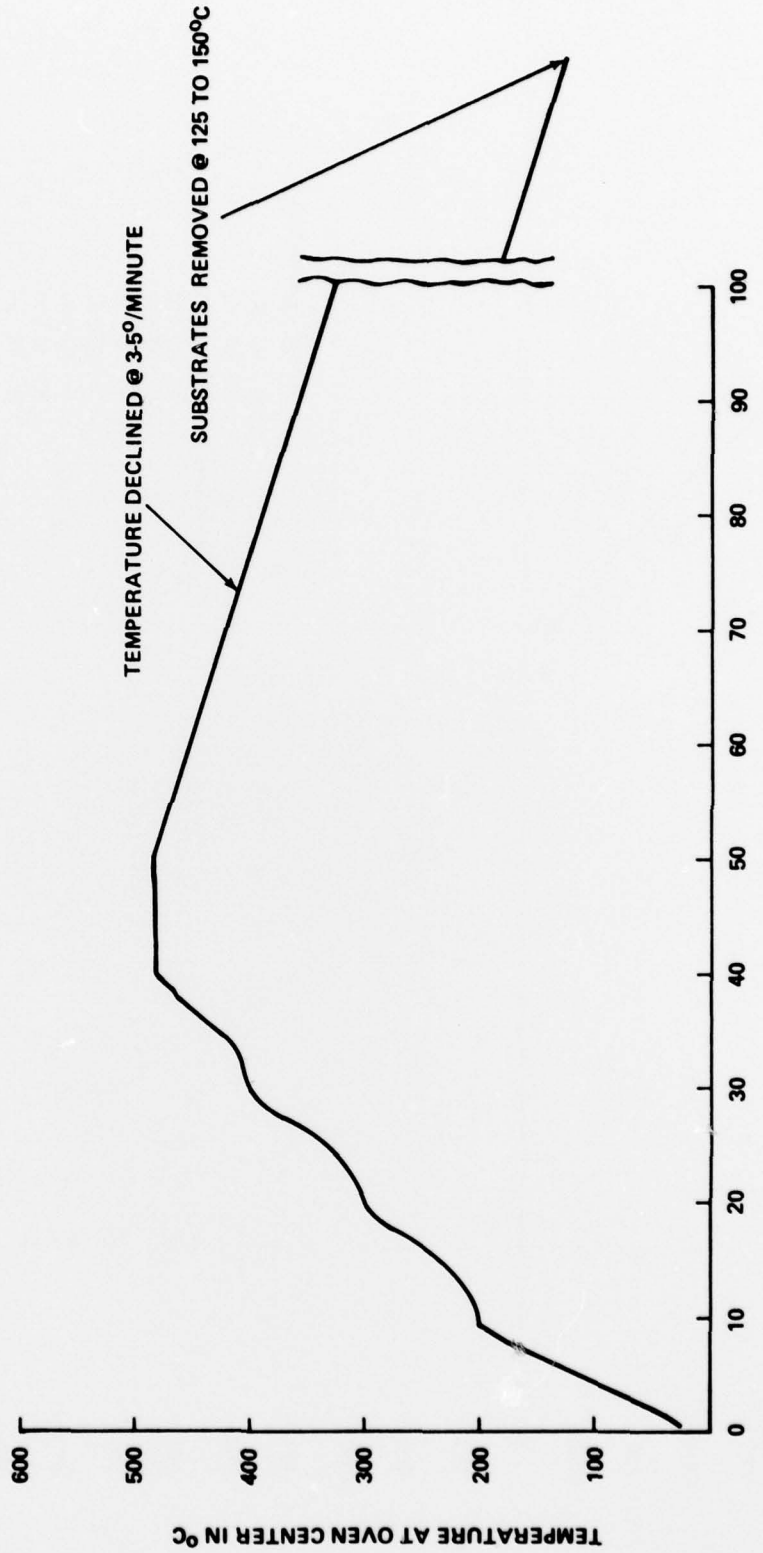

FIGURE 5. ANNEALING CYCLE TYPICAL TEMPERATURE VARIATION

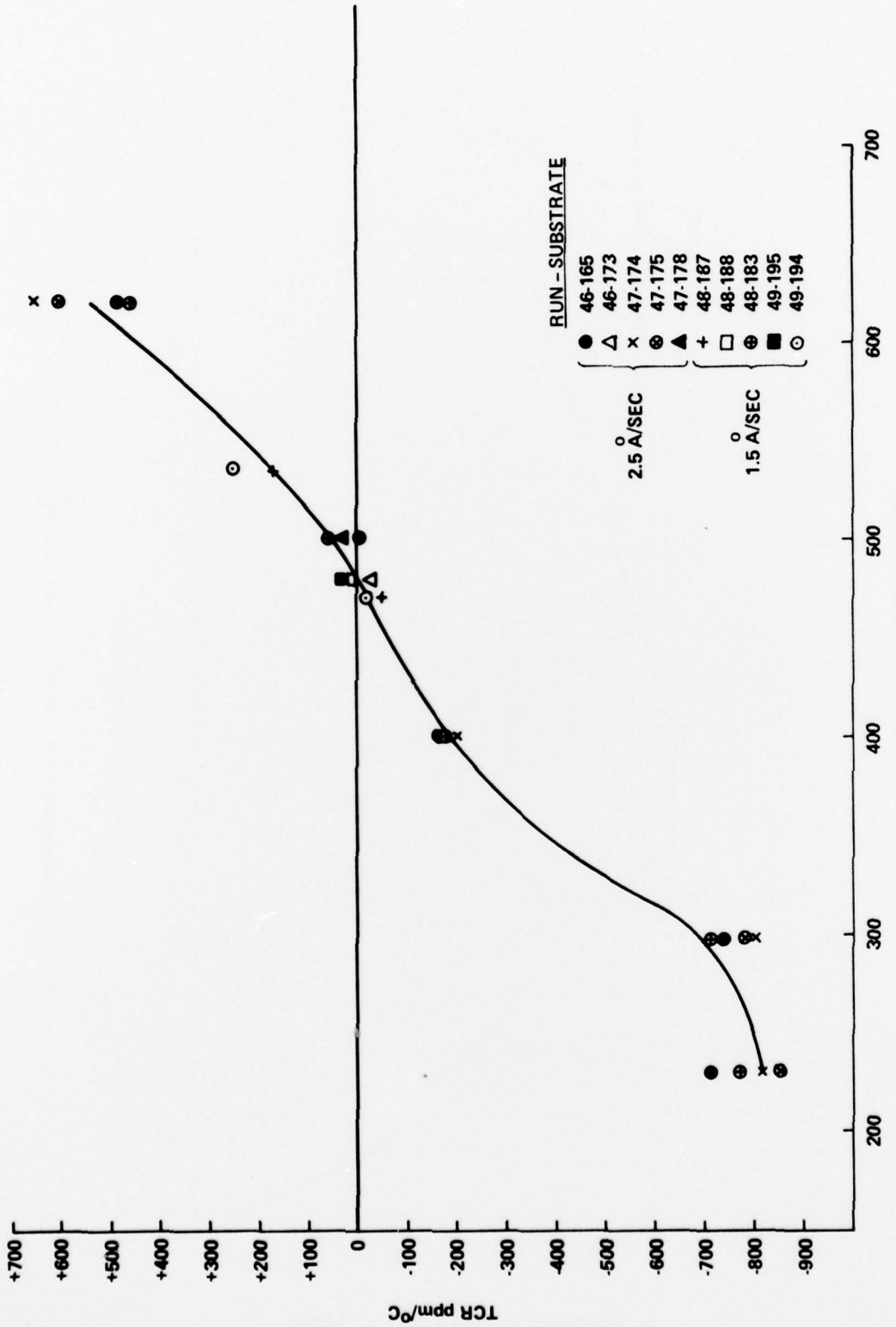

FIGURE 6. TCR VS. ANNEALING TEMPERATURE

positive indicating that chromium is influencing the characteristics of the film to a greater extent.

Other work reported in the literature by Hall[7] considers effects on TCR because of the mismatch of thermal coefficients of expansion for the film and the substrate material. Calculations for our films based on Hall's work indicates that the TCR value for the film on alumina should be less positive than for the same film on a silicon substrate. The work reported by Buczek[8] for reactively evaporated Ni-Cr films concludes that for a discontinuous or cermet film (when the substrate mismatch has a negligible effect) the TCR becomes more positive because of the increase in grain diameter and decrease in grain spacing. It is believed that our results tend to support Buczek's findings.

There have been some results reported where consideration was given to the influence of post deposition treatment on the TCR of the thin film resistor. Glang et al[4] reported results with a very low resistivity mixture of 83 atomic percent chromium in silicon showing that higher temperatures during the annealing cycle resulted in even more positive TCR values and demonstrated thereby that the oxide in Cr-SiO mixtures is the factor causing high resistivities and negative TCR's. Sato et al[9] and later Ostrander et al[10] in work with tantalum nitride resistors found that the temperature coefficient of resistance could be made to approach zero, as a result of annealing in vacuum at a particular temperature for several hours. In still other work on thick films, Isaak[11] has shown that for palladium-silver and resistor glaze inks, the annealing cycle determines the TCR.

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7. Hall, P. M., "The Effect of Expansion Mismatch on Temperature Coefficient of Resistance of Thin Films," Applied Physics Letters"

8. Buczek, D. M., "Thin Film Ni-Cr Resistor," 24th National Symposium of the American Vacuum Society, Boston, Massachusetts, November, 1977, Paper No. TF 5-8.

9. Sato, A., Oda, Y., and Hishinuma, Y., "Tantalum Nitride Resistors with Low TCR," in Proceedings of the 20th Electrical Components Conference, May 13-15, 1970, pp. 58-62.

10. Ostrander, W. J., Verhoef, J., and Bos, L. W., "Processing and Performance of Tantalum Nitride Thin Film Resistor Networks with +50 ppm/^{o}C TCR," The Institute of Electrical and Electronics Engineers Transactions on Parts, Hybrids and Packaging, Vol. PHP 9, No. 3, September 1973, p. 155.

11. Isaak, H. R., "Living With a Thick-Film Resistor Ink Series," In the Proceedings of the 19th Electronics Components Conference April 30, 1969, pp. 276-284.

CONCLUSIONS

The following conclusions can be drawn from this work:

(1) High value resistors in the range of 4.74×10^{-3} to 1.1×10^{-2} ohm-cm can be sputter deposited on as-fired 99.6% alumina substrates from a target consisting of a mixture of 27 atomic percent Cr in Si.

(2) The temperature coefficient resistance can be controlled as a function of the annealing temperature.

(3) The TCR value does not appear to be varied by differences in the deposition rate from 1.5 to 2.5 Å/second.

(4) There is difficulty in obtaining good ohmic contact to Cr-Si material using chromium and gold metallization.

(5) Good ohmic contacts can be made easily to Cr-Si material using the Ti-Pd-Au metallization.

(6) Cr-Si resistor films and the Ti-Pd-Au metallization can be delineated easily using chemical etching and R. F. sputter etching techniques.

It is also concluded that the investigation should be conducted further to determine such questions as the affect of air annealing and temperature variation on TCR; resistor stability under bias and storage conditions; the effects of factors such as gas flow rate, temperature control and annealing cycle duration on TCR and resistivity values; the effects of film thickness variations; the exact influence of coefficients of expansion mismatch between substrate and resistor film; also analysis of the films to determine changes in grain size and crystalline structure. In addition, it would be of major interest to our hybrid circuit work to determine the influence of the annealing cycle on the characteristics of other mixture ratios of chromium and silicon films and also on certain mixtures of Cr and SiO.

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