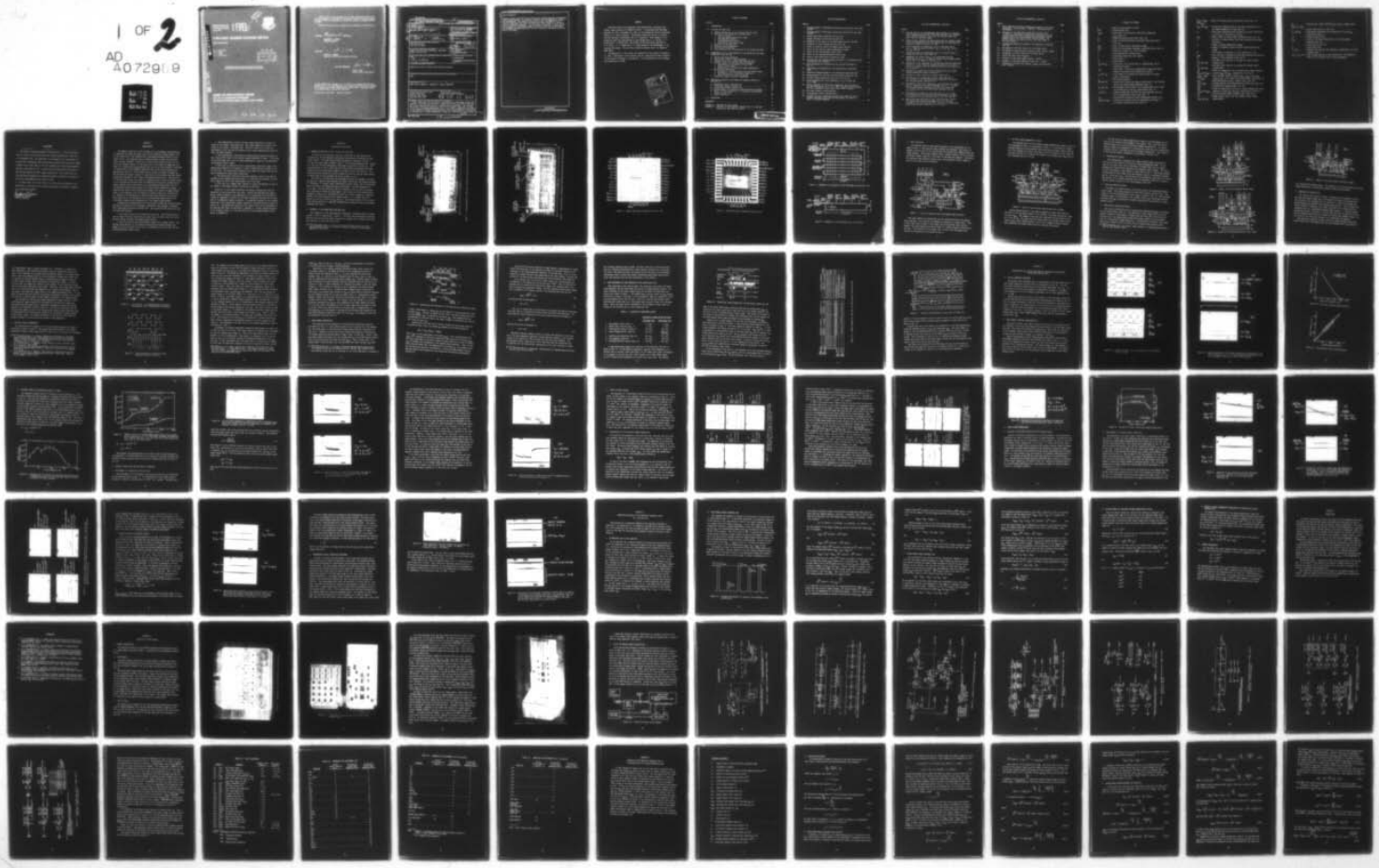
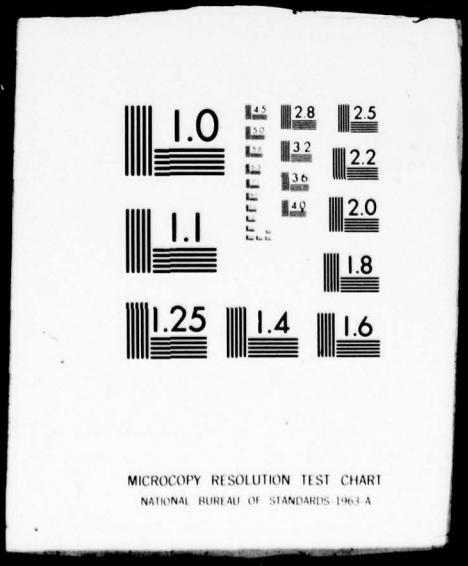
AD-A072 989 RCA LABS PRINCETON N J F/G 9/5
LOW-LOSS CHARGE-COUPLED DEVICE.(U)
JUN 79 W J KOSONOCKY, D J SAUER, C Y TAYAG F19628-77-C-0176
UNCLASSIFIED PRRL-78-CR-57 RADC-TR-79-144 NL

1 OF 2
AD A072989



1 OF 2
AD
A072989



AD A072989

RADC-TR-79-144
Final Technical Report
June 1979

LEVEL II

LOW-LOSS CHARGE-COUPLED DEVICE

RCA Laboratories

M. J. Kosonocky
D. J. Sauer
C. Y. Tayag
F. V. Shallcross

DDC
RECEIVED
AUG 17 1979
C

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

DDC FILE COPY

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

79 08 17 030

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-79-144 has been reviewed and is approved for publication.

APPROVED: Benjamin R. Capone

BENJAMIN R. CAPONE
Project Engineer

APPROVED: Robert M. Barrett

ROBERT M. BARRETT
Director, Solid State Sciences Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (ESE) Hanscom AFB MA 01731. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

90 1.

(19) **REPORT DOCUMENTATION PAGE**

READ INSTRUCTIONS BEFORE COMPLETING FORM

(18) 1. REPORT NUMBER: RADC-TR-79-144

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (and Subtitle): LOW-LOSS CHARGE-COUPLED DEVICE

(9) 5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report 15 May 77 - 15 Nov 78

(14) 6. PERFORMING ORG. REPORT NUMBER: PRRL-78-CR-57

(10) 7. AUTHOR(s): W. J. Kosonocky, C. Y. Tayag, D. J. Sauer, F. V. Shallcross

(15) 8. CONTRACT OR GRANT NUMBER(s): F19628-77-C-0176

9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA Laboratories, Princeton NJ 08540

(16) 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61102F 2305J124 (17) J1

(11) 11. CONTROLLING OFFICE NAME AND ADDRESS: Deputy for Electronic Technology (RADC/ESE), Hanscom AFB MA 01731

12. REPORT DATE: June 1979

13. NUMBER OF PAGES: 101

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same

(12) 101 p.

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Benjamin R. Capone (RADC/ESE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Charge-coupled devices, CCD
Low-loss CCD mode
Trailing bias charge
Long CCD delay line
Dark-current subtraction
Synchronous signal correlator

79 08 17 030

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Two closed-loop CCD structures, a 256-stage and a 1024-stage devices were designed, fabricated, and operated to demonstrate a low-loss mode of operation for a very long CCD delay line or a closed-loop CCD structure. The low-loss CCD concept consists of operating a CCD with each signal charge well followed by one or more trailing-bias-charge wells. Two orders of magnitude improvement in the effective transfer losses were demonstrated experimentally by periodically recombining at a signal-regeneration stage the (first-order) signal-charge → next page

(Cont'd)

DD FORM 1 JAN 73 1473

299 000

UNCLASSIFIED

Item 20 (Cont'd)

transfer losses collected by the trailing bias charger with the corresponding signal-charge packets. An effective transfer loss of 2.4×10^{-7} per transfer was demonstrated. The maximum time delay has also been improved by two orders of magnitude over that of conventional CCDs by means of a new dark-current subtraction technique. The 1024-stage closed-loop low-loss CCD was also operated as a synchronous signal correlator producing an improvement in the signal-to-noise ratio of 17.5 dB as a result of 100 signal recirculations in the loop.

PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-77-C-0176. It describes work performed from May 15, 1977 to November 15, 1978, in the Integrated Circuit Technology Center, J. H. Scott, Director. The Project Supervisor was D. E. O'Connor and the Principal Investigator was W. F. Kosonocky. Other Members of the Technical Staff who participated in this program were P. A. Levine, D. J. Sauer, and F. V. Shallcross. The coding of the chip layout was done by G. M. Meray. J. V. Groppe and C. Y. Tayag worked on the development of the low-loss CCD tester. The Air Force Technical Monitor was B. R. Capone of RADC (ESE).

The manuscript of this report was submitted by the authors on December 15, 1978. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for exchange and stimulation of ideas.

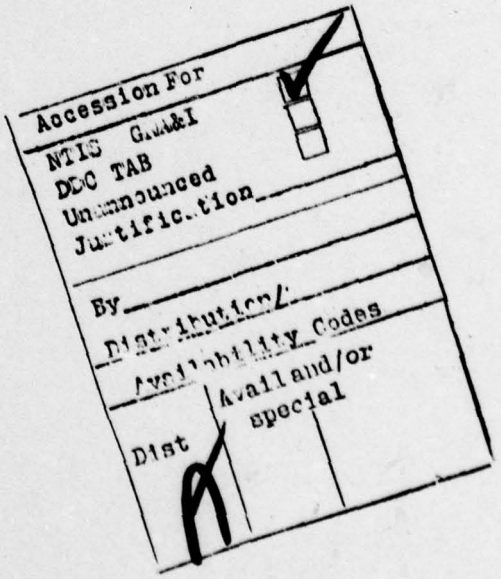


TABLE OF CONTENTS

PRECEDING PAGE BLANK

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

GLOSSARY OF SYMBOLS

A	= gain of recirculating CCD loop.
BCCD	= buried-channel CCD.
C_{DCS2}	= capacitance of dark-current subtraction stage gate G_{DCS2} (Fig. 11).
D_1	= floating-diffusion reset drain (Fig. 10).
D_2	= drain of floating-diffusion amplifier output MOS device (Fig. 10).
D_{DCS}	= drain of dark-current subtraction stage.
D_{OUT}	= drain of floating-gate amplifier output MOS device (Fig. 9).
e	= electronic charge (1.6×10^{-19} coulomb).
E	= bulk-trapping state energy level.
ε	= fractional charge loss per transfer.
ε_1	= first-order ε.
ε_2	= second-order ε.
ε_{1R} and ε_{2R}	= first-order ε and second order ε, respectively, due to regeneration stage.
ε_{BB}	= first-order ε occurring in regeneration stage when signal charge is separated from trailing bias charge.
ε_{LE} and ε_{TE}	= first-order ε on leading and trailing edge of a signal pulse, respectively.
f_c	= CCD clock frequency.
FG1 and FG2	= second-level polysilicon gates on both sides of the floating gate in the floating-gate amplifier (Fig. 9).
G_{1A} and G_{1B}	= input-signal barrier gates of the charge preset input stage for introducing Q_S and Q_{TB}, respectively (Fig. 7).
G_2 and G_3	= signal-storage gate (G_2) and the output-barrier gate (G_3) of the charge preset input stage (Fig. 7).
G_{1S}	= dark-current subtraction stage storage gate powered by ϕ_1.
G_{BCS} and G_{BCT}	= storage and transfer gates for separating Q_S and Q_{TB} in the signal-regeneration stage (Fig. 8).

G_{DCS1}, G_{DCS2}, and G_{DCS3} = gates of the dark-current subtraction stage (Fig. 11).

G_{RGS} and G_{RGT} = storage and transfer gates of the charge combining well in the signal-regeneration stage (Fig. 8).

G_S = first-level polysilicon gate extending the source diffusions S_{1A} and S_{1B} to the gates G_{1A} and G_{1B}.

I_{DCS} = drain current in dark-current subtraction stage (Fig. 11).

m = fraction of charge removed from loop by proportional charge subtractor.

M = number of signal-regeneration stages.

n = number of transfers between low-loss signal-regeneration stages.

N = total number of transfers in a CCD register (N = nM).

N_{rms} = rms noise due to N-charge carriers with Gaussian distribution.

N_t = density of bulk-trapping states [cm^{-3}].

ϕ_1 (ϕ_{1S} and ϕ_{1T}) = two-phase clock (applied to storage and transfer gates, respectively).

ϕ_2 (ϕ_{2S} and ϕ_{2T}) = two-phase clock (applied to storage and transfer gates, respectively).

ϕ_{BC} (ϕ_{BCS} and ϕ_{BCT}) = clock for regeneration of the trailing bias charge (applied to gates G_{BCS} and G_{BCT}, respectively, in Fig. 8).

ϕ_{DCS1}, ϕ_{DCS2}, and ϕ_{DCS3} = clock voltages applied to gates G_{DCS1}, G_{DCS2}, and G_{DCS3}, respectively, in the dark-current subtraction stage (Fig. 11).

ϕ_{FDT} = floating-diffusion output transfer pulse (Fig. 10).

ϕ_{OUT} (V_{OUT}) = voltage applied to floating-diffusion output gate (Fig. 10).

ϕ_{REC} = recirculation transfer pulse (Fig. 10).

ϕ_{RG} (ϕ_{RGS} and ϕ_{RGT}) = clock for combining Q_S with Q_{TB} in signal-regeneration stage (applied to gates G_{RGS} and G_{RGT}, respectively in Fig. 8).

Q_{DC} = subtracted dark-current charge at each clock cycle.

Q_S (Q_{S0} and Q_{S1}) = signal charge ('zero' and 'one' signal charge levels, respectively).

Q_{TB} (Q_{TB0} and Q_{TB1})	= trailing bias charge (following Q_{S0} and Q_{S1}, respectively).
S	= charge signal (Fig. 12, Fig. 16).
S_{1A} and S_{1B}	= input-source diffusions for introduction of Q_S and Q_{TB}, respectively (Fig. 7).
s/n	= signal-to-noise ratio.
S_{OUT}	= source of the output MOS device in the floating-gate amplifier (Fig. 9).
T	= trailing bias (Fig. 12).
τ_D	= total delay time.
τ_e and τ_t	= emission and trapping time constants, respectively, for bulk-trapping state.
V_{D1}, V_{G1A}, etc.	= bias voltages applied to the low-loss CCD. See Appendix A, Table A-1 for complete list of bias adjustments.

EVALUATION

1. This report is the Final Report on the contract. It covers research done on low-loss CCD devices during the contract period from 15 May 1977 to 15 November 1978. The objective of the research is to investigate the possibility of operating very long CCD delay lines with an effective charge transfer loss on the order of 10^{-7} per transfer and a time delay-bandwidth product on the order of 10^{6}. Closed loop CCD structures were operated in the low-loss mode by periodic signal regeneration. The closed-loop low-loss CCD can be operated as a synchronous signal correlator with signal to noise ratio improvements from -5.5db to 12db.

2. The above work is of value since it provides basic knowledge for the fabrication of new devices for accomplishing signal processing in Communication and Radar Systems.

Benjamin R. Capone

BENJAMIN R. CAPONE
Project Engineer

SECTION I

INTRODUCTION

The general objective of this program was to investigate the possibility of operating very long CCD delay lines with an effective charge transfer loss on the order of 10^{-7} per transfer and a time-delay-bandwidth product on the order of 10^{6}. To accomplish such an improved figure of merit for CCD delay lines, we have proposed a concept of a low-loss CCD by which we have (1) reduced the transfer losses in a CCD delay line by two orders of magnitude over those in a conventional buried-channel CCD, and (2) we have proposed a technique for subtraction of the thermally generated dark current which increased the maximum delay time in a CCD structure also by about two orders of magnitude. The low-loss CCD concept consists of operating a CCD structure with each signal-charge well followed by one or more trailing-bias-charge wells. The function of trailing bias charge is to keep the trapping states in the CCD channel filled. A very low effective transfer loss is achieved by periodically recombining the charge transfer losses collected by the trailing-bias-charge wells with the corresponding signal-charge packets at low-loss signal-regeneration stages. By adjusting the level of the trailing bias charge to be above the signal-charge level, we can guarantee that the effective transfer losses in a low-loss CCD are reduced to the second-order trapping losses encountered by the trailing bias charge due to the modulation of the trailing-bias-charge level by the first-order trapping losses experienced by the signal-charge packets.

To demonstrate experimentally the low-loss CCD concept and the dark-current subtraction technique we have designed, fabricated, and operated a 256-stage and a 1024-stage closed-loop low-loss CCD. The closed-loop CCD structures have the following features:

- Two parallel inputs are provided for each loop. One of the inputs is used to sample the input signal and the other input is used to form the trailing bias charge following the signal-charge packets.
- Each loop has one floating-diffusion output with a signal switch. The voltage pulses applied to the signal-switching gates determine whether the signal is to be circulated in the loop or transferred out of the loop via the floating-diffusion output stage.

- Two independently clocked, low-loss signal-regeneration stages are placed in the larger, 1024-stage loop. One signal-regeneration stage is included in the smaller, 256-stage loop. This will enable us to study the performance of the low-loss CCD operation with signal regenerations after 512, 1024, and 2048 transfers.
- Two floating-gate, nondestructive signal-sensing stages are placed in each loop on both sides of the low-loss signal-regeneration stage. In the case of the 1024-stage loop, only one signal-regeneration stage has the associated floating-gate output stages.
- Each loop is constructed with a dark-current subtraction stage. The dark-current subtractor is designed to remove a fixed amount of charge out of the CCD loop. The dark-current subtractor can remove the charge, but not the noise introduced by dark-current generation.
- The dark-current subtractor has been designed so that it can also be operated in the charge proportional mode. In this mode of operation, it will allow removal of 25% of the charge signal out of the loop.
- Each loop has a merged input junction to allow the addition of the input signal to the signal already circulating in the loop.

Section II of this report describes the design, construction, and the operation of the low-loss CCD test chips. Section III describes the experimental results obtained in the operation of the closed-loop low-loss CCDs including an experiment in which the 256-stage closed-loop low-loss CCD is operated as a synchronous signal correlator. A simplified analysis of the transfer losses due to the second-order charge trapping in the low-loss CCD is given in Section IV. The design and operation of the tester built for the operation of the low-loss CCD loops are described in Appendix A. A more rigorous analysis of the transfer losses in a low-loss CCD due to bulk-trapping states is presented in Appendix B.

SECTION II

LOW-LOSS CCD TEST CHIP

A. GENERAL DESCRIPTION OF THE LOW-LOSS CCD TEST CHIP

To study the characteristics and the performance of the low-loss CCD concepts [1], we have designed, fabricated, and operated a low-loss CCD test array, TC1230. This test array actually includes two separate 4.95 mm x 2.15 mm test chips shown in Figs. 1 and 2. The photomicrograph in Fig. 1 shows the test chip TC1230A containing a 1024-stage closed-loop low-loss CCD. The photomicrograph in Fig. 2 shows the test chip TC1230B containing a 256-stage closed-loop low-loss CCD and a number of process control test devices. The labeled photomicrographs of the two closed-loop low-loss CCD test chips bonded in 48-pin dual-in-line packages are shown in Figs. 3 and 4.

The low-loss CCD test chip was processed following our standard two-level polysilicon n-channel buried-channel CCD (BCCD) technology with non-self-aligned n^+ diffusions, p^+ channel stops, 1000-Å-thick channel oxide, and n^+ polysilicon gates processed with phosphorus-doped reflow glass. The BCCD channels are 25 μm wide. The gate structure has 10-μm polysilicon gates with 5-μm spaces, thus resulting in 30-μm-long CCD stages. The closed-loop CCD structures were designed to operate as a two-phase CCD with a dc offset voltage to be applied between the storage gates and the transfer gates, i.e., between the clock phases ϕ_{1S} and ϕ_{1T}, as well as ϕ_{2S} and ϕ_{2T}. The charge-corners of both closed loops were designed for a complete charge-transfer operation with the available two-phase CCD clocks.

B. FEATURES OF THE CLOSED-LOOP LOW-LOSS CCDs

The schematics of the 1024-stage and 256-stage, closed-loop CCDs are shown in Figs. 5 and 6, respectively. Except for the fact that the larger closed-loop structure has two low-loss signal-regeneration stages, both of these structures have the same features described below.

---

1. W. F. Kosonocky and D. J. Sauer, "CCD Long-Time Delay Line," Air Force Systems Command Contract No. F19628-77-C-0176, Scientific Interim Report, RADC-TR-78, July 1978.

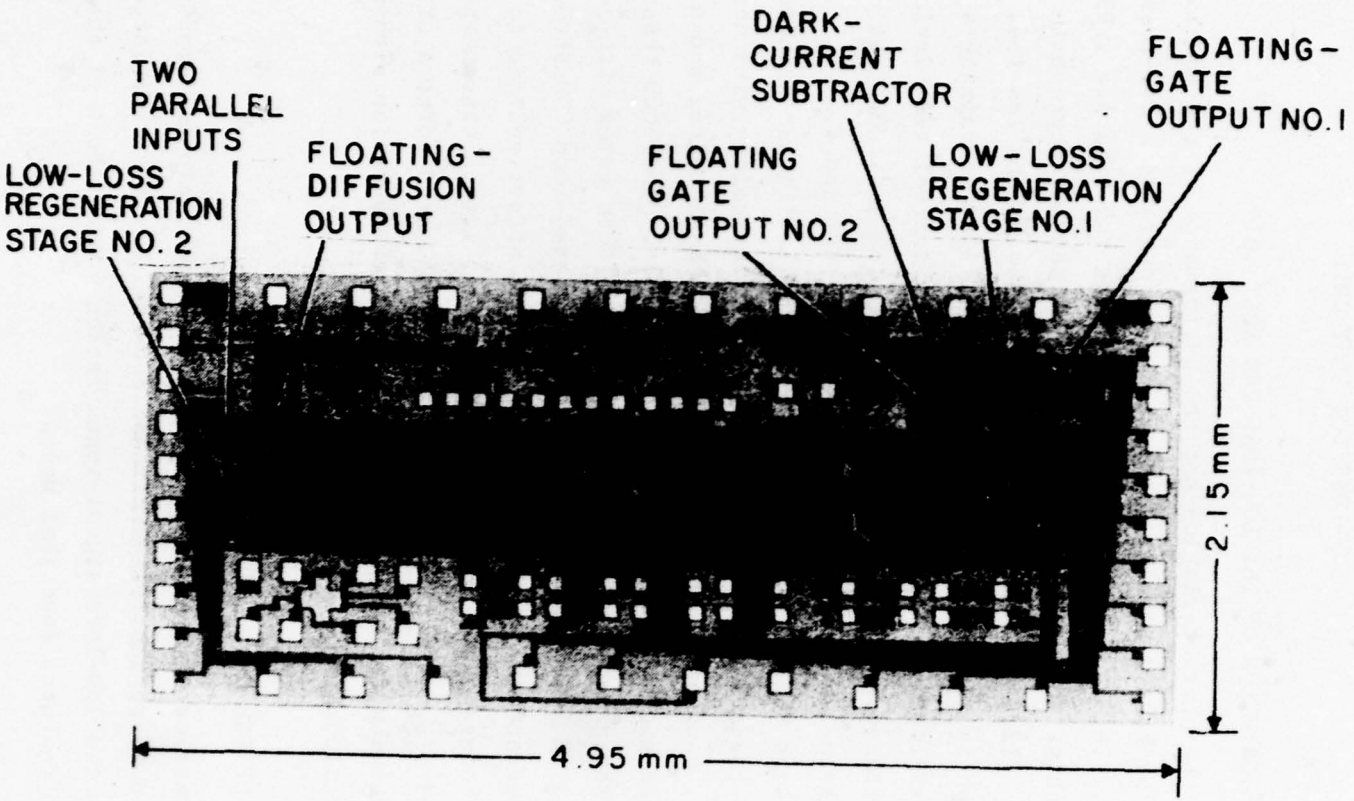


Figure 1. Photomicrograph of 1024-stage closed-loop low-loss CCD test chip TC1230A.

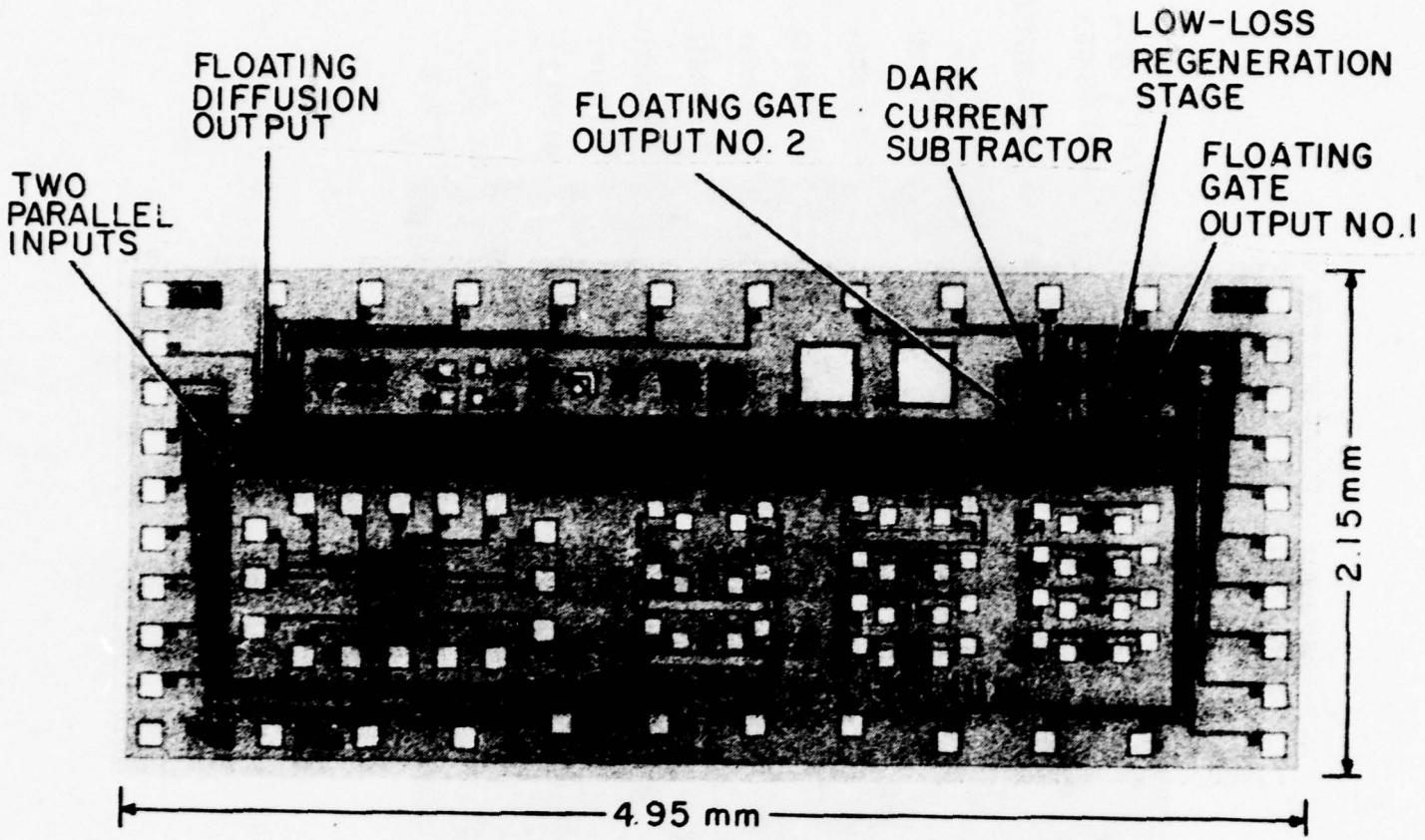


Figure 2. Photomicrograph of 256-stage closed-loop low-loss CCD test chip TC1230B.

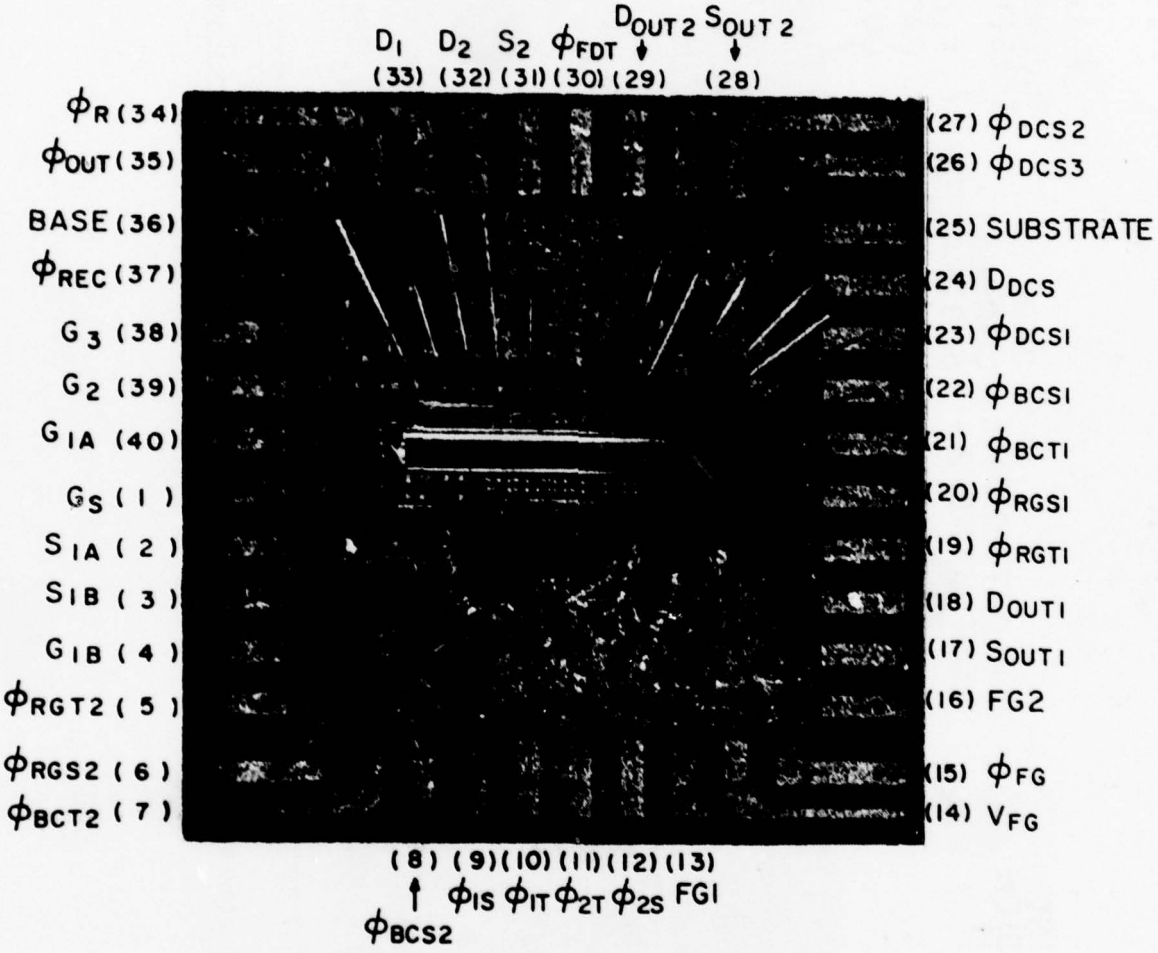


Figure 3. Bonded 1024-stage closed-loop low-loss CCD.

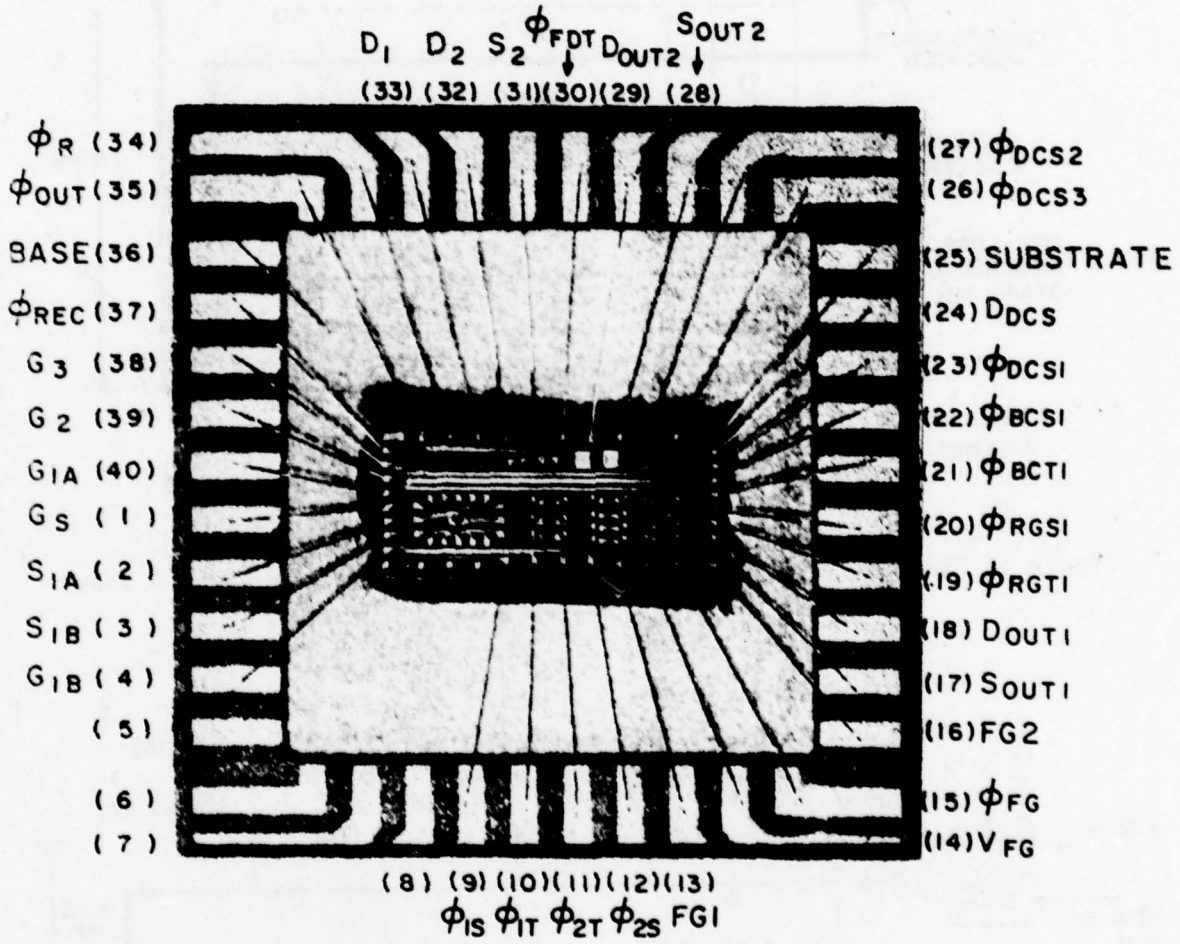


Figure 4. Bonded 256-stage closed-loop low-loss CCD.

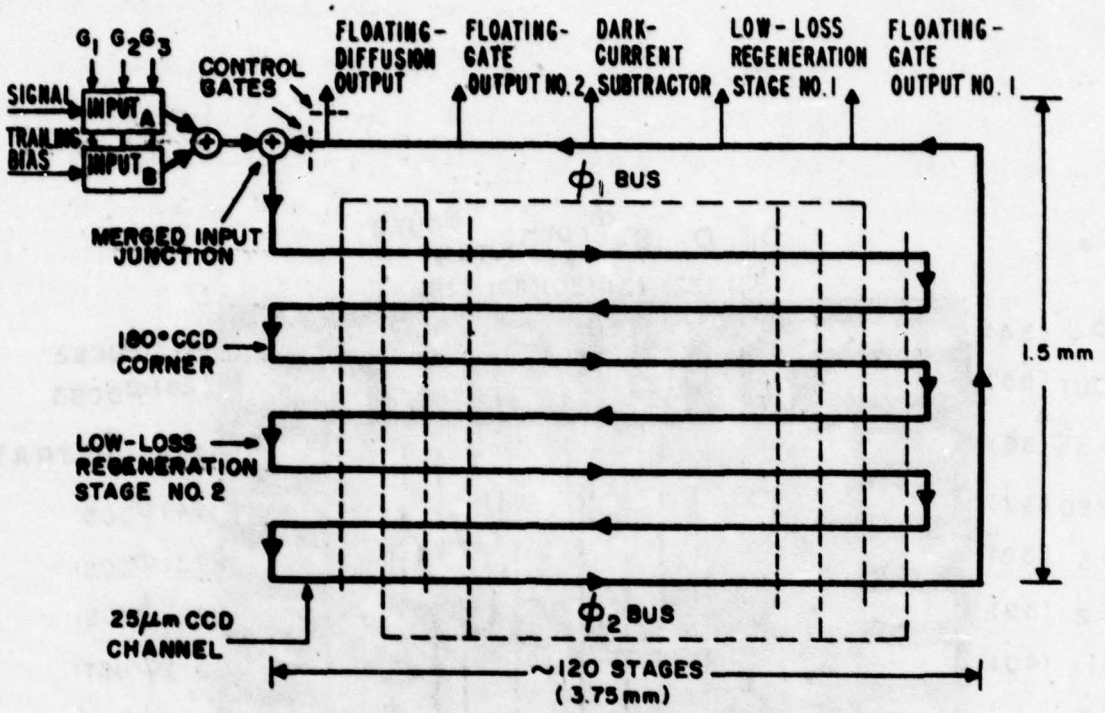


Figure 5. Schematic of the layout of the 1024-stage low-loss CCD loop.

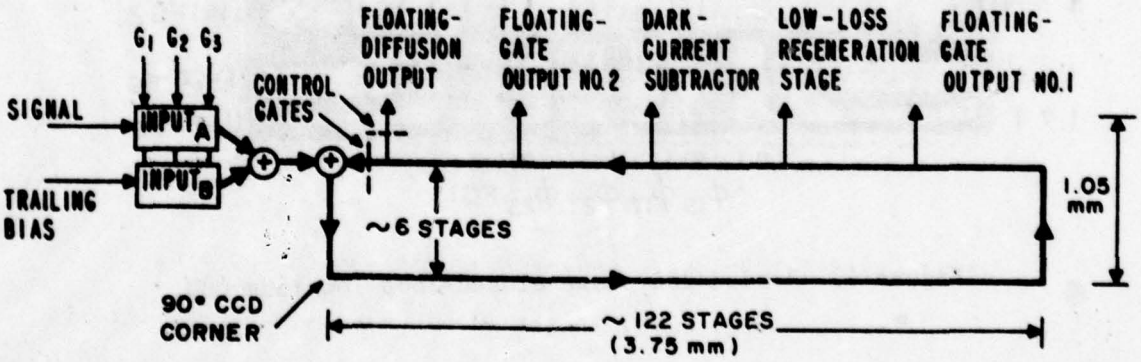


Figure 6. Schematic of the 256-stage low-loss CCD loop.

1. Input Structure

The detailed layout of the input structure of the closed-loop CCDs is shown in Fig. 7. Two parallel input channels are provided: one is for the signals, and the other is for introducing the trailing bias charge between the signal samples. These input channels have a channel width of 35 μm to provide sufficient dynamic range for a full well in the main CCD register. The inputs are operated using standard charge preset (fill-and-spill) with a negative pulse on the input-source diffusions.

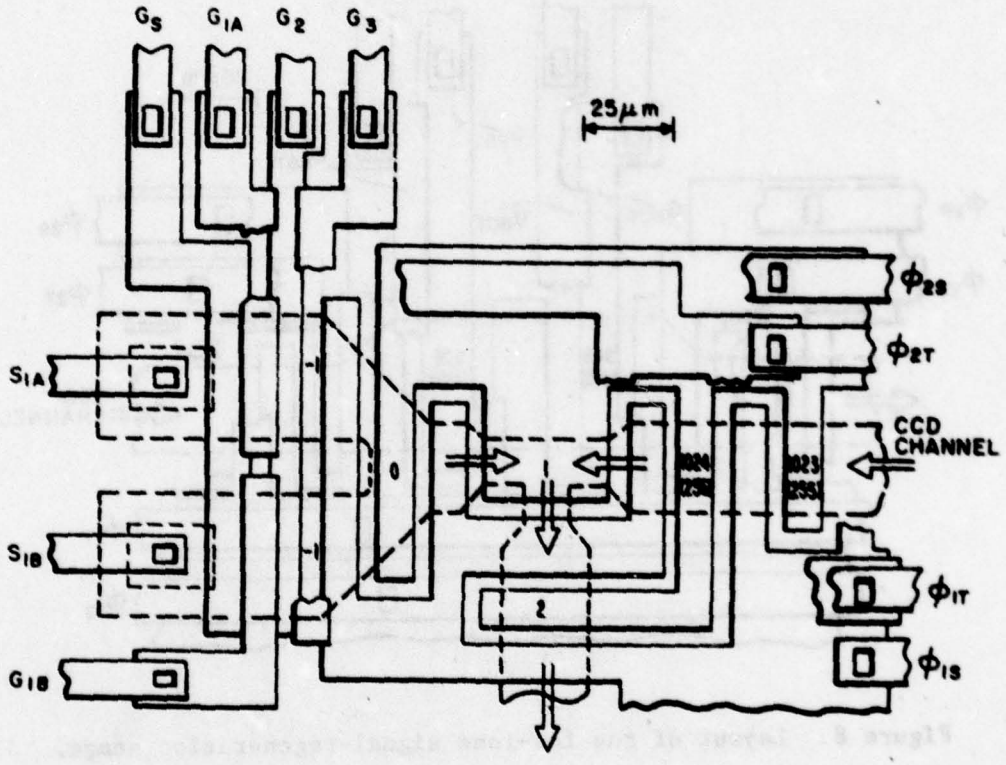


Figure 7. Layout of parallel inputs and merged input junction.

The input signals are introduced into the closed-loop CCD at the merged input junction. This junction is designed to operate as a signal adder. Thus, if the closed loop is empty, a new signal can be introduced into the loop. However, the input signal can also be added to a signal already circulating in the loop. The direction of the signal flow is built into the merged input junction as designated by the arrows in Fig. 7.

2. Low-Loss Signal-Regeneration Stage

The detailed layout of the low-loss signal-regeneration stage #1 shown in the photograph in Fig. 1 is illustrated in Fig. 8. To increase the charge-handling capacity of the potential wells carrying the signal charge combined with the trailing bias charge, the width of the CCD channel at this stage was increased from 25 to 37.5 μm and the length of the storage gates G_{RGS} and G_{1S} was increased from 10 to 15 μm.

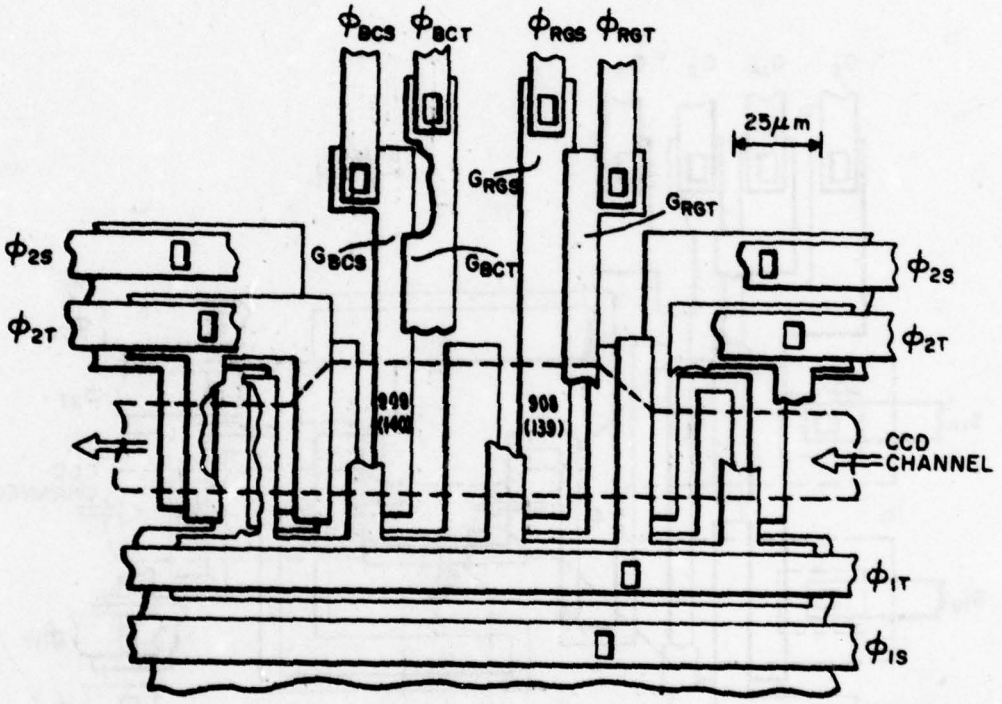


Figure 8. Layout of the low-loss signal-regeneration stage.

Another design feature of the signal-regeneration stage that should be mentioned is the increased length of the trailing bias-charge generating transfer gate, G_{BCT}. The length of this gate was increased from the typical value of 5 μm to 10 μm. The longer barrier formed under this transfer gate is provided to give lower charge-transfer loss at this incomplete charge transfer which separates the signal charge from the trailing bias charge.

The two low-loss signal-regeneration stages in the 1024-stage loop are laid out for operation with separate clock pulses. Thus, this loop can be operated either with one or two low-loss signal regenerations. Of course, there is always the possiblity of operating the closed loop as a conventional two-phase CCD not involving the low-loss signal regeneration. The operation of the low-loss signal regeneration is described in Section II.C.

3. Floating-Gate Outputs

Two floating-gate, nondestructive signal-sensing stages are placed in each loop on both sides of the low-loss signal-regeneration stage. In the case of the large loop, with a 1024-stage, two-phase CCD, only one signal-regeneration stage has the associated floating-gate output stages. The layout of the floating-gate output stage is illustrated in Fig. 9. The signal-sensing floating gate of this stage can be periodically reset to a reference potential V_{FG} by a clock pulse ϕ_{FG}. The function of two externally controllable dc levels, FG1 and FG2, is to provide isolation from the two-phase clocks and to assure a complete charge transfer at this floating-gate output [2].

4. Floating-Diffusion Output

The signal is removed from the closed-loop CCDs by the floating-diffusion output stage. This stage provides the destructive readout from the loop. The layout of the floating-diffusion output stage is shown in Fig. 10. The floating-diffusion output is controlled by the transfer pulses ϕ_{FDT} (floating-diffusion transfer) and ϕ_{REC} (recirculation transfer) operating in conjunction as complementary pulses.

5. Dark-Current Subtraction Stage

Each loop is constructed with a dark-current substraction stage illustrated by the layout shown in Fig. 11. The operation of this stage, which can be adjusted to remove a fixed amount of charge from the loop, will be described in Section II.E. This dark-current subtraction stage, however, can be operated also as a proportional charge subtractor. In this mode of operation, this stage will allow a removal of 25% of charge from the signal-charge packets and/or

2. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Rev. 36, 566-593 (1975).

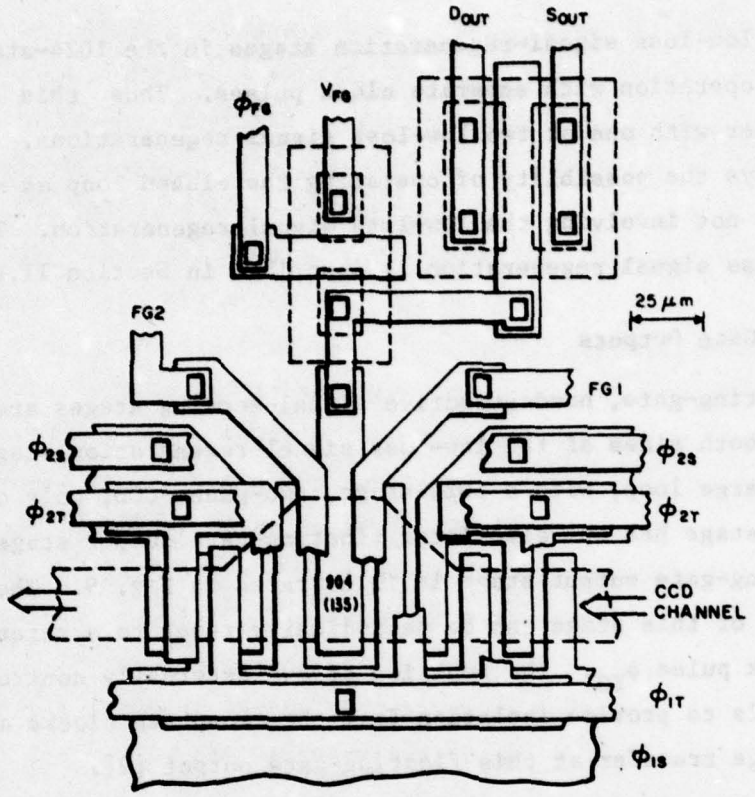


Figure 9. Layout of the floating-gate output stage.

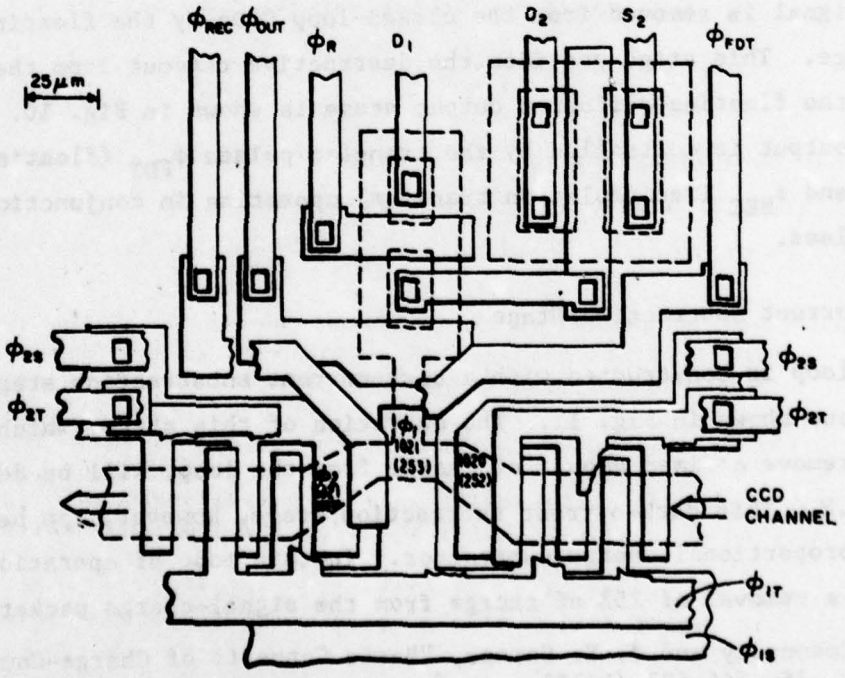


Figure 10. Layout of the floating-diffusion output stage.

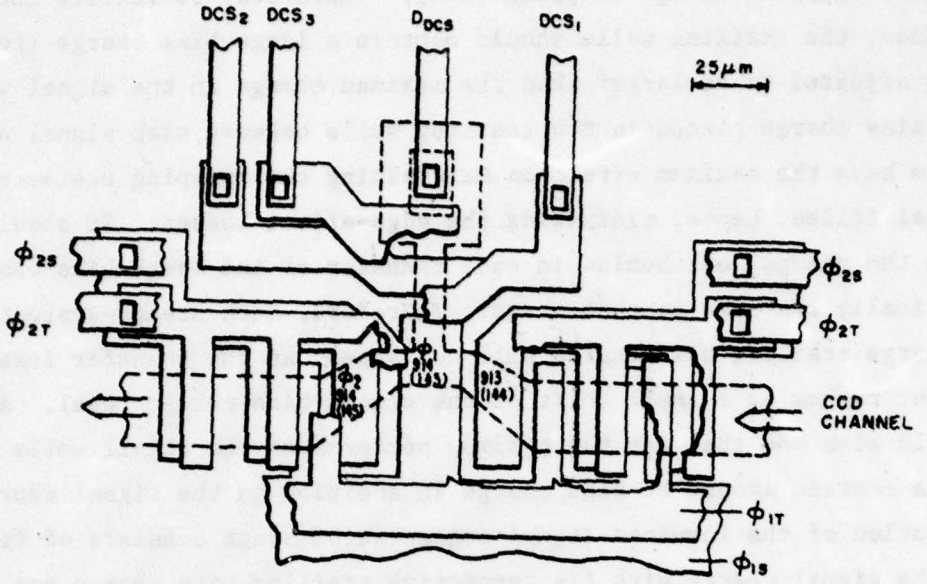


Figure 11. Layout of the dark-current subtraction stage.

the trailing bias-charge packets. The operation of the dark-current subtraction stage operating as a proportional subtractor has not been tested.

C. OPERATION OF LOW-LOSS CCD

The low-loss CCD concept is based on operating a CCD register in such a way that each signal-charge well is followed by at least one trailing well. The function of the trailing well (or wells) is to collect the charge left behind during each transfer of the signal-charge packet. Then, periodically, after a number of transfers, the charge collected by the trailing wells is recombined with the corresponding charge-signal packet at a low-loss signal-regeneration stage. Therefore, a low-loss CCD with one trailing well following each signal-charge well will recover the first-order transfer losses, i.e, the losses of the first loss trailer of a conventional CCD register.

The relatively constant transfer losses in surface-channel and buried-channel CCDs at the intermediate and low clock frequencies are attributed to

the "edge-effect" type of charge trapping [1-6]. Therefore, to achieve the best performance, the trailing wells should contain a large bias charge (fat zero) that is adjusted to be larger than the maximum charge in the signal wells. Such a large bias charge placed in the trailing wells between each signal well is expected to have the maximum effect on maintaining the trapping states of the CCD channel filled, hence, minimizing the edge-effect losses. It should be noted that the charge left behind in each transfer of the large bias charge will be practically the same at each stage. Therefore, such steady-state transfer loss of the large trailing bias charge will not appear as the transfer loss of the signal, but rather as a small shift of the signal-bias-charge level. At this point we should also add that for the optimum performance the signal wells should also contain a certain amount of bias charge in addition to the signal charge.

The operation of the low-loss signal-regeneration stage consists of first recombining the signal charge with its respective trailing bias charge and then separating the signal from a regenerated (reshaped) trailing bias charge. Therefore, the effective transfer losses of a low-loss CCD operating with one trailing bias charge are due to the second-order trapping losses resulting from the modulation of the trailing bias charge by the first-order trapping losses of the signal charge. For further discussion of the nature of the effective transfer losses of a low-loss CCD see Section IV and Appendix B.

D. LOW-LOSS SIGNAL REGENERATION

The construction and operation of a low-loss signal-regeneration stage is illustrated in Figs. 12 and 13. The charge-coupling structure of the signal-regeneration stage is shown schematically in Fig. 12(a) in the form of a two-phase

3. W. F. Kosonocky and J. E. Carnes, "Design and Performance of Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," Digest of Technical Papers, 1973 International Electron Device Meeting, Washington, D.C., 123-125, Dec. 3-5, 1973.
4. C. H. Sequin and M. F. Tompsett, *Charge Transfer Devices* (Academic Press, New York, 1975), pp. 70-108.
5. M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of Charge-Coupled Devices," IEEE Trans. Electron Devices ED-20, 45-55 (1973).
6. A. M. Mohsen and M. F. Tompsett, "The Effects of Bulk Traps on the Performance of Bulk Channel Charge-Coupled Devices," IEEE Trans. Electron Devices ED-21, 701-712 (1974).

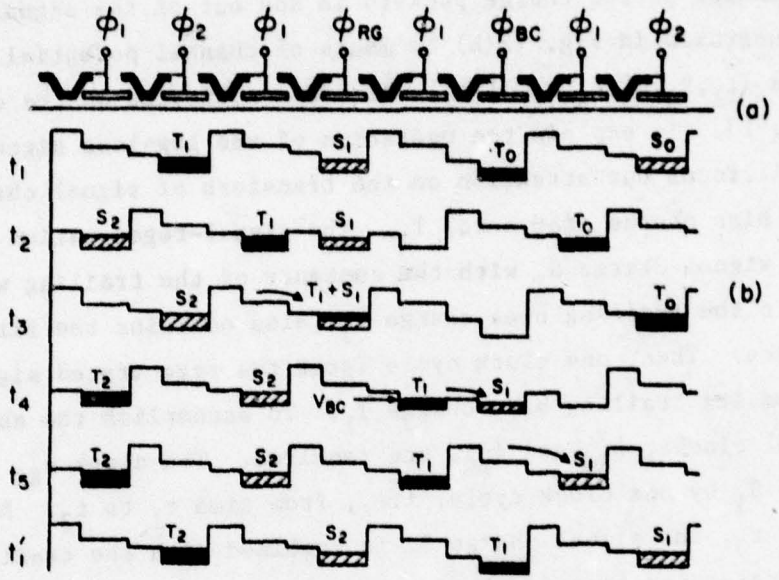


Figure 12. Low-loss CCD. (a) Charge-coupling structure. (b) Potential wells illustrating the operation.

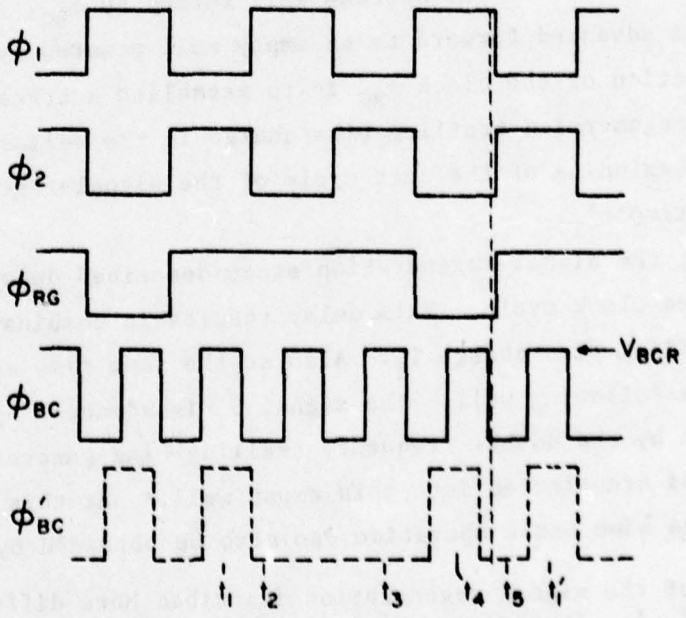


Figure 13. Clock waveforms for operation of the low-loss CCD shown in Fig. 12.

CCD. The transfer of the charge packets in and out of the signal-regeneration stage is illustrated in Fig. 12(b) by means of channel potential profiles at time instants (t_1,t_2,t_3,t_4,t_5, & t'_1) which are indicated on the clock waveforms shown in Fig. 13. To explain the operation of the low-loss signal-regeneration stage, we will focus our attention on the transfers of signal charge S_1 and its trailing bias charge (fat zero) T_1. The signal-regeneration stage first combines the signal charge S_1 with the contents of the trailing well, which in addition to the trailing bias charge T_1, also contains the first-order transfer losses. Then, one clock cycle later the regenerated signal S_1 is separated from its trailing bias charge T_1. To accomplish the above functions two additional clocks, ϕ_{RG} and ϕ_{BC}, are required. The clock ϕ_{RG} delays the signal charge S_1 by one clock cycle, i.e., from time t_1 to t_3. Because of this delay at time t_3, the signal charge S_1 is combined with the trailing bias charge T_1 and the first-order transfer losses contained in the trailing well. At time t_4, the combined charge ($S_1 + T_1$) is transferred to the adjacent potential well induced by clock ϕ_1. Note, however, that the adjacent CCD well is pulsed by a double-frequency bias-charge generating clock ϕ_{BC}. The result is that at time t_4 the signal charge, S_1, is skimmed by the potential barrier formed under the transfer gate and stored in the storage well formed by ϕ_{BC}. Then at time t_5 the signal S_1 is advanced forward to an empty well powered by the adjacent ϕ_1 clock. The function of the clock ϕ_{BC} is to establish a transfer barrier V_{BC} which leaves a regenerated trailing bias charge in the well induced by the clock ϕ_1. The beginning of the next cycle of the signal-regeneration stage is illustrated at time t'_1.

In general, the signal-regeneration stage described delays the signal, S_1, at time t_3 by one clock cycle. This delay results in combination of the signal S_1 with its trailing bias charge T_1. Also at the same time an empty well is generated at the following well. The signal S_1 is advanced by one cycle (at times t_4 and t_5) by the double frequency trailing-bias-generating clock ϕ_{BC} (see Fig. 13) and transferred into this empty well.* At this point it should be noted that the same basic operation can also be obtained by using a slower

*The operation of the signal regeneration described here differs from that reported in Ref. 1. In the case of Ref. 1 the signal regeneration result is a net delay of the signal by one clock cycle, while in the present case there is no such additional delay.

clock ϕ_{BC}' shown in Fig. 13. The ϕ_{BC}' clock may be preferable for operation of the low-loss CCD at higher clock frequencies.

Referring to the channel potential profiles in Fig. 12(b), we see that the signal charge, S_1, is always followed by the trailing bias charge T_1, except during the transfer at time t_4. At this transfer the first-order transfer loss, ε_1, results in a net transfer loss of $\varepsilon_1 Q_{S1}$, that, at time t'_1 will be combined with the following signal charge, Q_{S2}. Another charge transfer also involving first-order trapping loss that requires special attention is the transfer at time t'_1 which separates the trailing bias charge T_1 and the signal charge S_1. This transfer is referred to as an incomplete (or bucket-brigade type) charge transfer [2,7]. To assure higher charge-transfer efficiency at this point, the transfer gate powered by ϕ_{BCT} and generating the barrier potential V_{BC} was designed longer (10 μm long) as shown in Fig. 8. Experimental results, however, showed that even with the above modification we have about 0.7% charge transfer loss at this transfer. This transfer loss was reduced to 0.1% by an externally modified clock ϕ_{BC} so that skimming of the signal charge (as shown at t_4 in Fig. 12(b)) and dumping it into the next empty well (as shown at time t_5 in Fig. 12(b)) was repeated twice:* the first time, to transfer most of the charge Q_{S1}, and then again to measure-off the trailing bias charge with an approximately empty storage well under the clock ϕ_{BC}. The results of this test are described in Section III.D.3.

E. DARK-CURRENT SUBTRACTION

The construction and operation of a dark-current subtraction stage are illustrated in Fig. 14. The cross-sectional view of one gate of a CCD register, G_{1S}, and three gates of the dark-current subtraction stage are illustrated in Fig. 14(a). Operation of the dark-current subtraction stage is illustrated by the channel potential profiles shown in Figs. 14(b), (c) and (d). In Fig. 14(b), the charge signal introduced into the storage gate G_{1S} of the CCD register spills over into the potential well under the gate G_{DCS2}. Then, in Fig. 14(c), the charge signal is spilled back into the potential well under the gate G_{1S} while

7. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Rev. 34, 164-202 (1973).

*The modified double ϕ_{BC} is not included in the tester described in Appendix A.

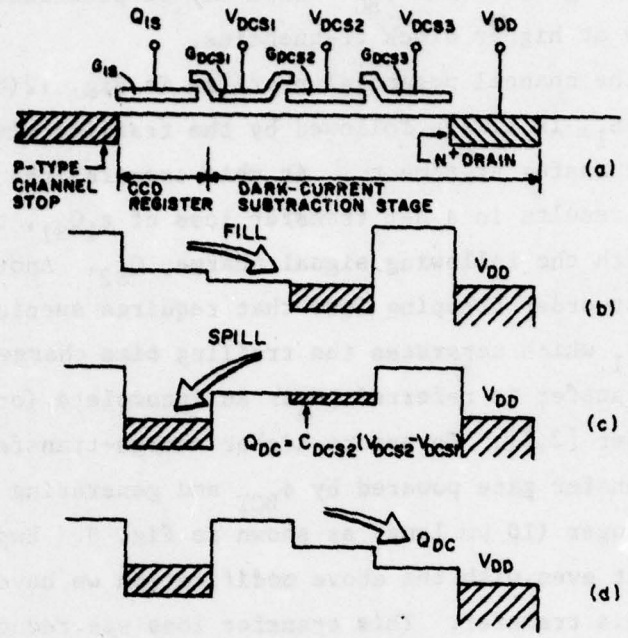


Figure 14. Construction and operation of the dark-current subtraction stage.

a small, fixed amount of charge Q_{DC} is left behind in the potential well under the gate G_{DCS2}. Finally, as shown in Fig. 14(d), the charge subtracted from the CCD channel, Q_{DC}, is spilled to the drain V_{DD}. This operation can be accomplished at the same time as the signal charge is transferred out from the well under the gate G_{1S}.

Assuming that the same type of surface channel is constructed under all the gates in Fig. 14(a), the charge Q_{DC} removed by the above process is

$$Q_{DC} = C_{DCS2}\left(V_{DCS2} - V_{DCS1}\right) \tag{1}$$

where C_{DCS2} is the capacitance of the gate G_{DCS2}. For a buried-channel CCD, C_{DCS2} will represent an effective capacitance associated with the gate G_{DCS2}. The only requirement of the above charge-scooping operation is that the charge Q_{DC} be constant and independent of the signal-charge magnitude. Also, for any given long CCD delay line, the magnitude of the charge Q_{DC} to be removed from the CCD structure should be controlled by a self-adjusting feedback circuit. This was done in the operation of the closed-loop CCD devices, described in Section III.

Since the dark-current subtraction stage removed a fixed amount of charge from a CCD structure, it can suppress the effect of the dark current on the reduction of the charge-handling capability of the CCD wells. But, it is not expected to remove the shot noise generated by the dark current. In fact, the process of the dark-current subtraction will also introduce a kTC noise [8].

Let us assume that the full-well signal charge in a buried-channel CCD corresponds to 10^6 charge carriers and has $s/n = 5\times10^3$. Now, if this CCD is operated with 10 dark-current subtraction stages, each removing 10% of full well of dark-current generated charge, the total generated dark-current charge will correspond to 10^6 charge carriers. The resulting rms noise will be

$$N_{rms} = \sqrt{10^6} = 10^3 . \tag{2}$$

and the s/n will be decreased to

$$s/n = 10^3 . \tag{3}$$

Now, let us assume that the time delay is increased 100 times by operating the above CCD as a closed-loop structure with 100 signal recirculations. The resulting shot noise introduced by the dark current should be increased to

$$N_{rms} = \sqrt{10^8} = 10^4 \tag{4}$$

and the s/n should be decreased to

$$s/n = 100 \tag{5}$$

The above analysis, however, does not include the reduction in the noise due to the time-dependent bandwidth limited operation because of the transfer losses in the operation of the low-loss CCD with very many transfers. Our experimental results (see Section III.D) show that when the closed-loop CCD is operated with the dark-current subtraction in the loop, adjusted to remove

8. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Rev. 33, 327-343 (1972).

the thermally generated dark current, the shot noise due to the dark current does not increase progressively but rather tends to saturate at a relatively low value. The result is that the closed-loop CCD structure can be operated continuously with a closed loop without developing appreciable dark-current noise (see Section III.D for more discussion of this effect).

F. CLOCK WAVEFORMS FOR THE OPERATION OF THE CLOSED-LOOP CCDs

When operating in the low-loss mode, the 256-stage loop stores 128 signal-charge packets, and the 1024-stage loop stores 512 signal-charge packets. The exact positions of the output stages along the CCD delay line described previously are listed in Table 1. The merged input junction (under the ϕ_{2S} storage electrode) is stage #1 (see Fig. 7), and subsequent stages are numbered in order counterclockwise around the CCD loop. Note that from the dual-channel input metering wells under gate G_2 to the merged input junction, there is a two-stage delay. Thus, the input may be considered to be at stage #-1 since these two stages are not actually part of the closed-loop CCD.

TABLE 1. LOCATIONS OF FUNCTIONAL STAGES

	Position of Stage Along CCD Loops	
	256-Stage Loop	1024-Stage Loop
1. Dual-Channel Input (Fig. 7)	-1 (ϕ_2)	-1 (ϕ_2)
2. Merged Input Junction (Fig. 7)	1 (ϕ_2)	1 (ϕ_2)
3. Floating-Gate Output #1 (Fig. 9)	135 (ϕ_2)	904 (ϕ_2)
4. Signal Regenerator(s) (Fig. 8)	139 (ϕ_2)	(506) (ϕ_2) 908 (ϕ_2)
5. Dark-Current Subtractor (Fig. 11)	145 (ϕ_1)	914 (ϕ_1)
6. Floating-Gate Output #2	151 (ϕ_2)	920 (ϕ_2)
7. Floating-Diffusion Output (Fig. 10)	253 (ϕ_1)	1021 (ϕ_1)

A simplified timing diagram for operation of the 256-stage CCD loop is shown in Fig. 15. As described in Appendix A, the CCD clock frequency f_c is divided down to provide a LOOP SIZE signal ($f_c/2^9$) whose pulse width corresponds to the length of the CCD loop (256 clock cycles), and a TOTAL DELAY signal ($f_c/2^{11}$) whose period determines the overall test cycle time. The leading

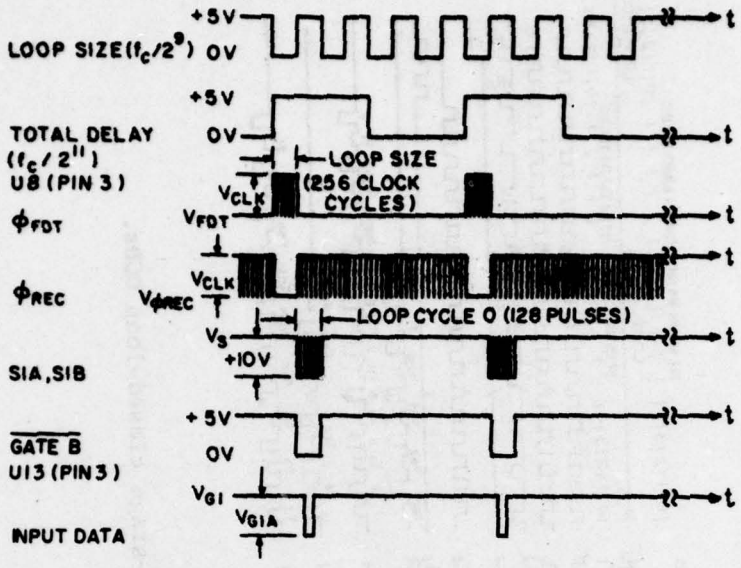


Figure 15. Simplified timing diagram for the 256-stage closed-loop CCD.

edge of the TOTAL DELAY signal initiates Loop Cycle N during which ϕ_{FDT} is pulsed for 256 clock cycles which reads out all of the charge stored in the CCD loop via the floating-diffusion output stage. This period is followed by Loop Cycle 0 during which new signals are introduced into the CCD register at the dual-channel input stage and charge is recirculated by pulsing ϕ_{REC}.

Figure 16 is a timing diagram for the 256- and 1024-stage, closed-loop CCDs operating in the low-loss mode. A more detailed timing diagram for Loop Cycle 0 is shown in Fig. 17. The input signal is applied to gate G_{1A}. In the timing diagrams a data input pattern of 0 1 1 0 is used. Note that a '1' level corresponds to a more negative level on the input gate G_{1A} and the negative S_{1A} strobe pulses occur when ϕ_1 is off. The S_{1A} pulses occur during even clock cycle times and S_{1B} pulses (for introducing trailing bias charge in the second input channel) occur at odd clock cycle times. A total of 128 S_{1A} and 128 S_{1B} pulses occur during Loop Cycle 0. At the beginning of Loop Cycle 1, the S_{1A}, S_{1B} pulses are inhibited and no further charge is introduced to the CCD via the dual-channel input stage.

At the beginning of Loop Cycle 0, the transfer out of the floating-diffusion stage ends by terminating the ϕ_{FDT} pulses, and the recirculation mode is started by initiating the ϕ_{REC} pulses. In the 256-stage loop, the first signal S_1

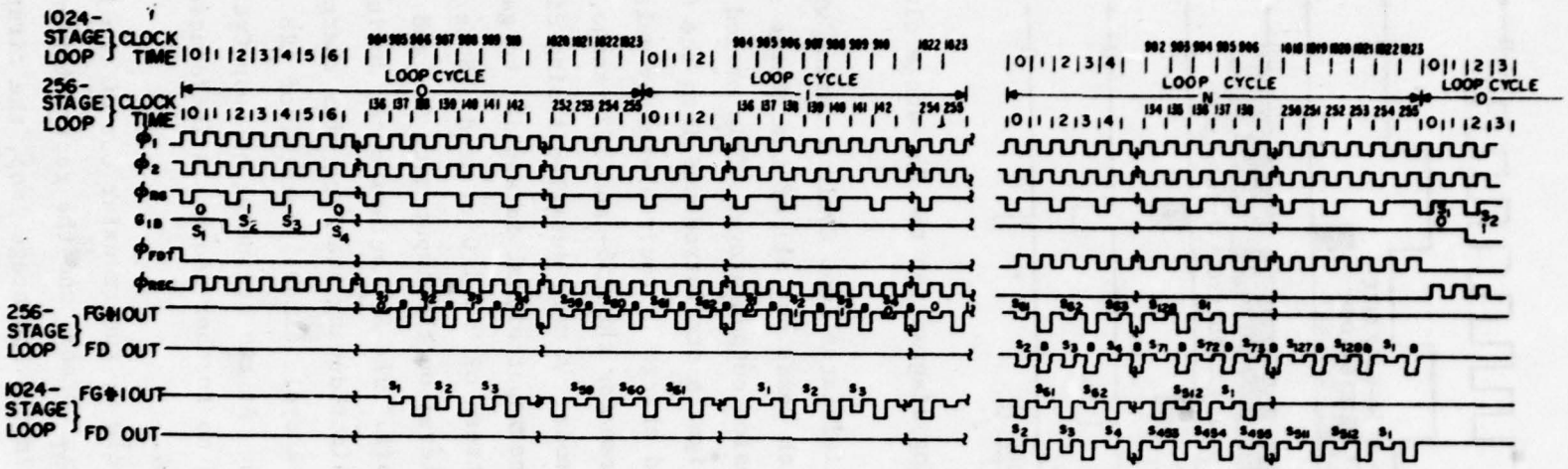


Figure 16. Timing diagram for the 256- and 1024-stage closed-loop CCDs.

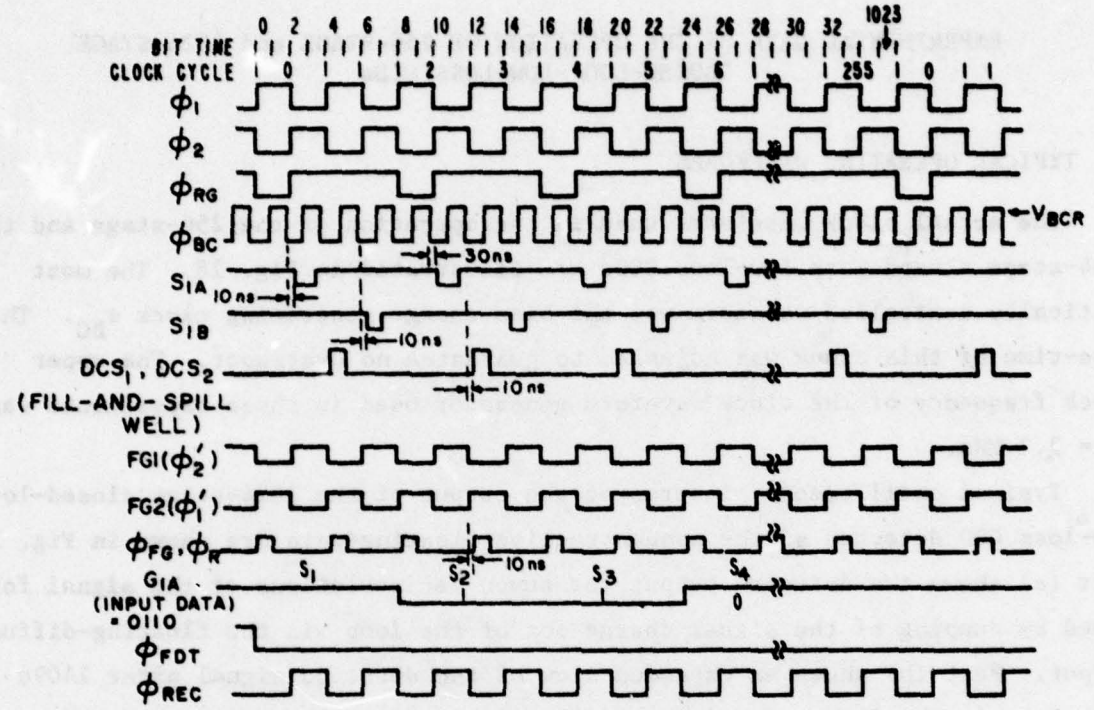


Figure 17. Detailed timing diagram of loop cycle 0 in Fig. 16.

appears at the floating-gate output #1 during clock time 136 in each loop cycle, and the bias charge trailing behind signal S_1 appears at clock time 137 as shown in Fig. 16.

During Loop Cycle N the signals are transferred to the floating-diffusion output by applying pulses to ϕ_{FDT} and inhibiting ϕ_{REC}. The first signal to appear at the floating-diffusion output (during clock time 0) is S_2. Signal S_1 appears during clock time 254 after signal S_{128} at the end of the data stream. This reordering of data is due to a two-stage differential delay between the input stage to the merged input junction and the floating-diffusion output stage to the merged input junction.

The timing for operation of the 1024-stage CCD loop is very similar to that for the 256-stage CCD loop and is also shown in Fig. 16. In this case, a total of 512 signals are stored in the low-loss mode of operation.

SECTION III

EXPERIMENTAL DATA ON THE OPERATION OF 256-STAGE and 1024-STAGE CLOSED-LOOP LOW-LOSS CCDs

A. TYPICAL OPERATING WAVEFORMS

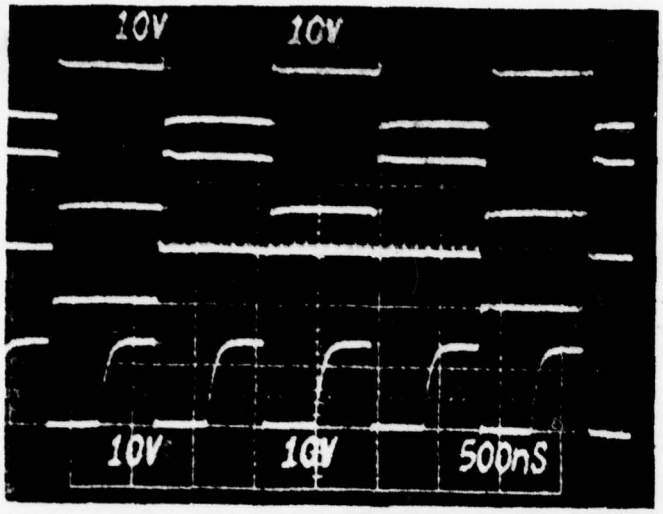
The actual clock waveforms used in the operation of the 256-stage and the 1024-stage closed-loop low-loss CCDs are illustrated in Fig. 18. The most critically controlled waveform was the bias-charge generating clock ϕ_{BC}. The rise-time of this clock was adjusted to guarantee no overshoot. The upper clock frequency of the clock waveform generator used in these experiments was f_c = 2.2 MHz.

Typical oscilloscope pictures of the output of the 1024-stage closed-loop low-loss CCD detected at the nondestructive floating-gate are shown in Fig. 19. Part (a) shows the detected output for seven recirculations of the signal followed by dumping of the signal charge out of the loop via the floating-diffusion output. Part (b) shows an expanded view of the detected signal after 14096 transfers in the loop. The detected signals in Fig. 19 consist of "one" signal-charge level, Q_{S1}, "zero" signal-charge level, Q_{SO}, and the trailing-bias-charge level, Q_{TB}.

B. INPUT/OUTPUT TRANSFER CHARACTERISTICS

The input transfer curve shown in Fig. 20 illustrates the calibration and the linearity of the dual input stage of the 1024-stage or the 256-stage closed-loop CCD. This curve was obtained by operating the input stage (one channel) in the standard charge preset (fill-and-spill) mode with a dc bias applied to the gate G_2 and the input voltage, V_{G1}, applied to gate G_{1A}.

Typical floating-gate output characteristics measured for two different 1024-stage closed-loop low-loss CCDs (TC1230A) are shown in Fig. 21. In this test we are comparing the signal charge, Q_s, with the observed oscilloscope waveform of the floating-gate output. The signal charge, Q_s, was measured in this test, as well as in the case in Fig. 20, by an electrometer. An inspection of Fig. 21 shows that the floating-gate output stage has a linear output transfer curve.



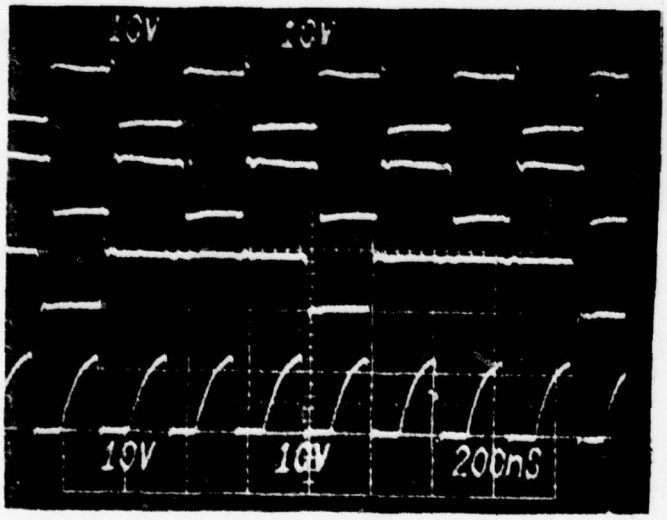


Figure 18. Pulser waveforms for clock frequency of (a) 0.55 MHz, and (b) 2.2 MHz.

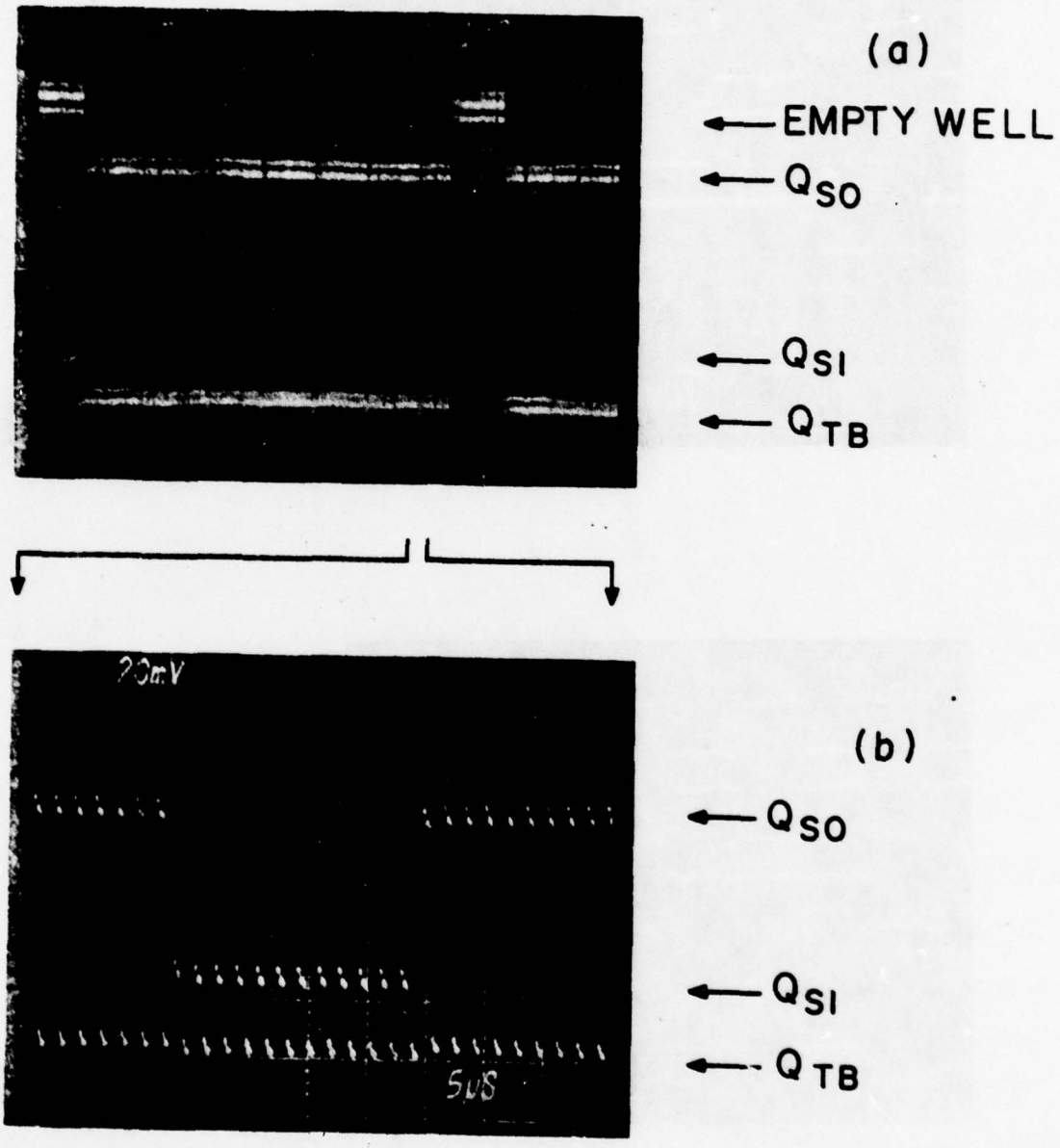


Figure 19. Output waveforms for 1024-stage closed-loop CCD operating in low-loss CCD mode at (a) f_c = 1.1 MHz with seven recirculations, and (b) an expanded output signal after 14096 transfers.

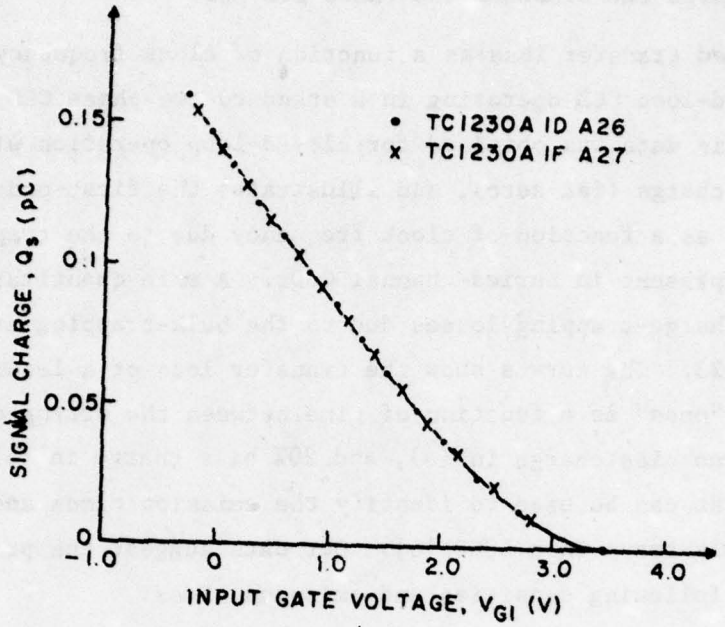


Figure 20. CCD input transfer characteristics.

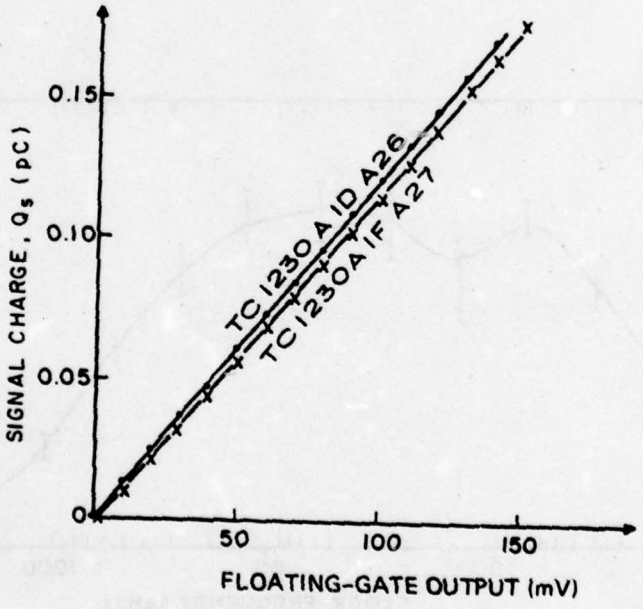


Figure 21. Floating-gate output characteristics.

C. TRANSFER LOSSES FOR STANDARD TWO-PHASE CCD MODE

The measured transfer loss as a function of clock frequency, f_c, of a 256-stage closed-loop CCD operating in a standard two-phase CCD mode is shown in Fig. 22. This data was obtained for closed-loop operation with 20% of full-well bias charge (fat zero), and illustrates the first-order (standard) transfer losses as a function of clock frequency due to the trapping of charge by bulk states present in buried-channel CCDs. A more quantitative characterization of the charge-trapping losses due to the bulk-trapping states is presented in Fig. 23. The curves show the transfer loss of a leading signal "one" in a string of "ones" as a function of time between the string of ones for operation with no bias charge in (a), and 20% bias charge in (b). This type of double-pulse test can be used to identify the emission times and calculate the densities of bulk traps in a BCCD [6]. Our data suggest the presence of two traps with the following densities and emission times:

(1) $N_{t1} = 3.6 \times 10^{11}\ cm^{-3}$

$\tau_{e1} = 5.6\ \mu s$

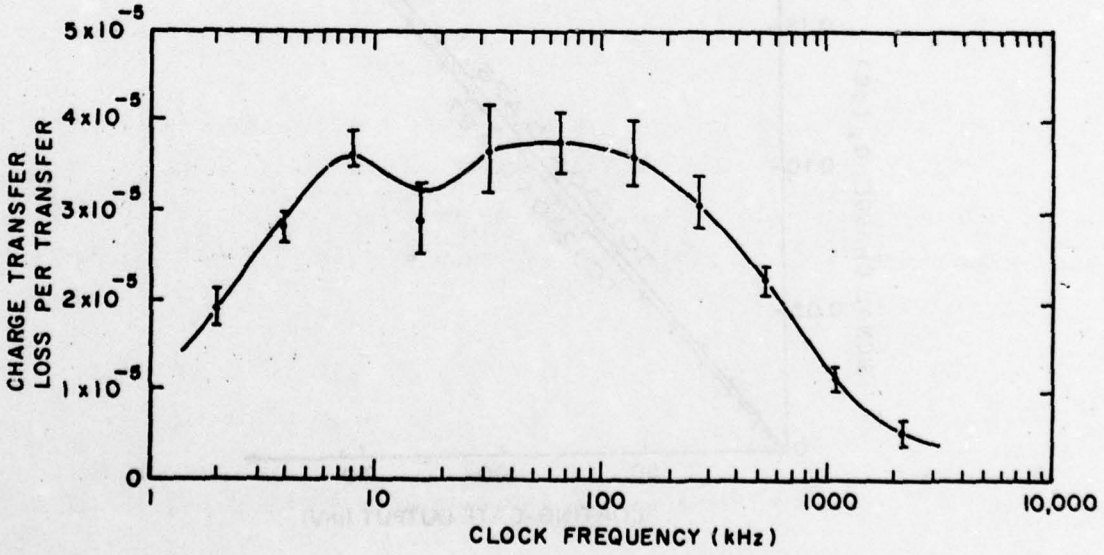


Figure 22. Transfer loss for closed-loop 256-stage CCD operating with a standard two-phase clock and 20% bias charge (fat zero) as function of clock frequency.

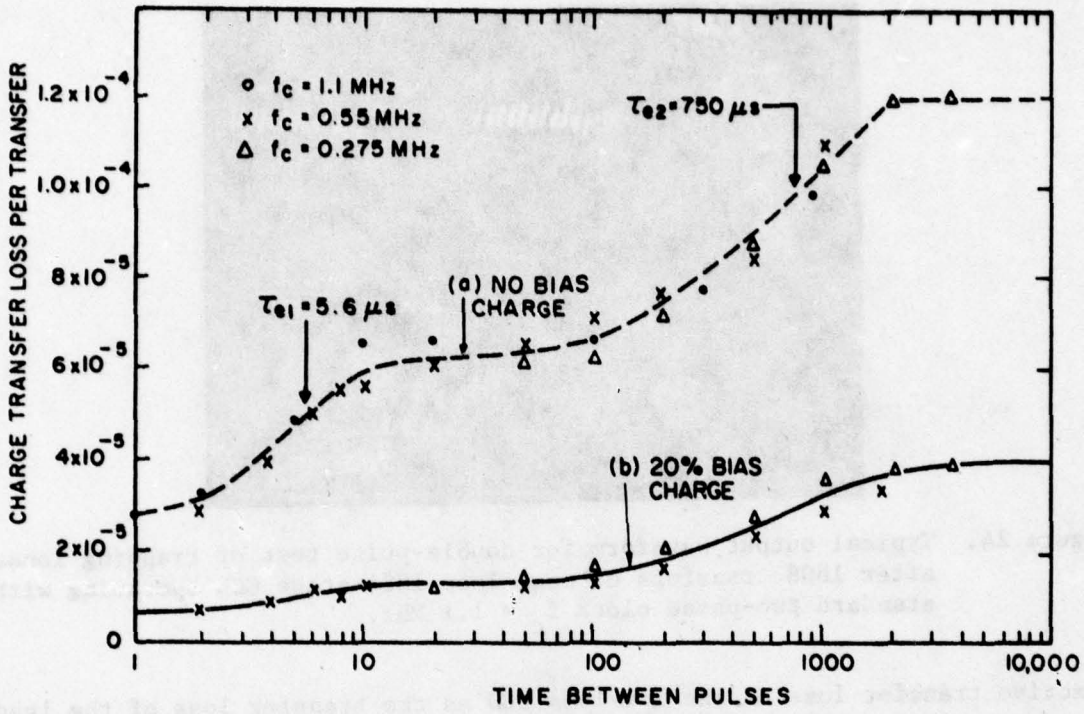


Figure 23. Transfer loss of the leading-edge signal charge in the double-pulse trapping-loss test for 1024-stage open-loop CCD operating with standard two-phase clock and, with (a) no bias charge (fat zero), and (b) 20% bias charge.

(2) $N_{t2} = 3.6 \times 10^{11}$ cm^{-3}

$\tau_{e2} = 750$ μs

The transfer loss measurements for the data in Fig. 23 were obtained by the operation of our 1024-stage device as an open-loop standard two-phase CCD. A typical output waveform observed during this double-pulse test is shown in Fig. 24.

D. TRANSFER LOSSES FOR LOW-LOSS MODE OF OPERATION

1. Performance of Closed-Loop Low-Loss CCDs

The performance of the 256-stage closed-loop low-loss CCD is illustrated by the waveforms shown in Fig. 25. As demonstrated by this figure we have achieved an effective transfer loss of 2.5×10^{-7} per transfer. We define the

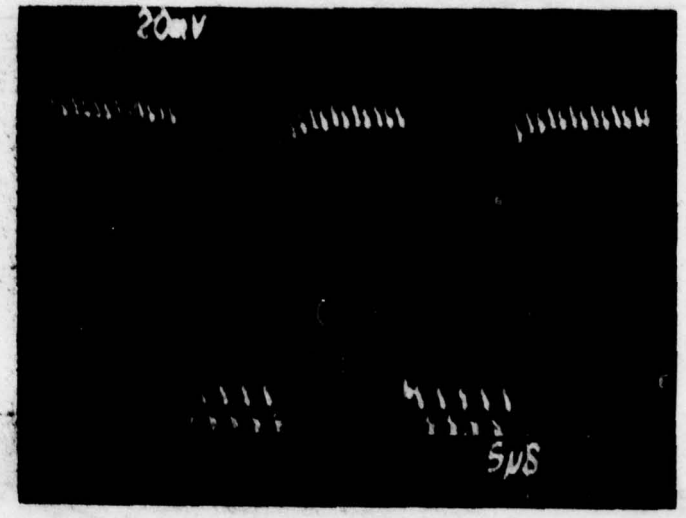


Figure 24. Typical output waveform for double-pulse test of trapping losses after 1808 transfers of open-loop 1024-stage CCD operating with standard two-phase clock f_c = 1.1 MHz.

effective transfer loss of the low-loss CCD as the transfer loss of the leading edge of an input pulse (the first "one" in a string of "ones"). The effective low-loss CCD transfer loss is

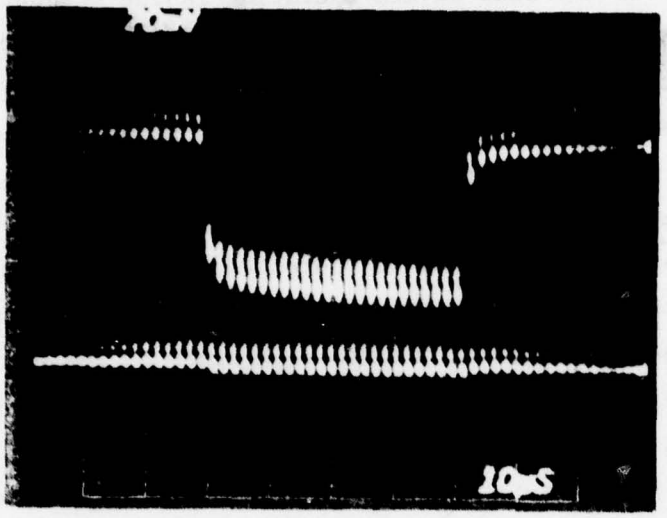
$$\varepsilon_{2T} = \frac{\Delta Q_{S1}(1)}{N(Q_{S1}-Q_{SO})} \tag{6}$$

where $\Delta Q_{S1}(1)$ is the difference between the initial value of the "one" at the input (i.e., as detected in the first recirculation) and the first "one" after N transfers, Q_{S1} is the amplitude of the signal charge "one," and Q_{SO} is the signal charge "zero." For the waveform in Fig. 25 we have used typical signal levels with

$$Q_{SO} = 0.2\ Q_{TB}$$

$$Q_{S1} = 0.8\ Q_{TB}$$

where Q_{TB} is the trailing bias charge adjusted just below the full well of the BCCD.

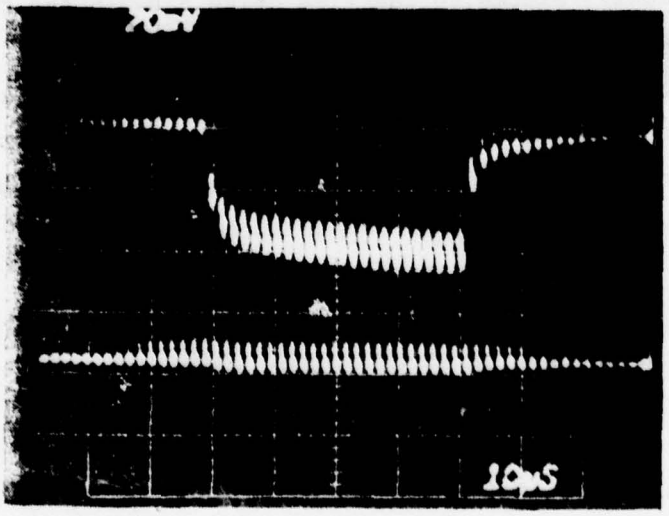


(a)

$\tau_D = 0.5\,s$

$N = 1.1 \times 10^6$

$\epsilon = 2.4 \times 10^{-7}$



(b)

$\tau_D = 1.0\,s$

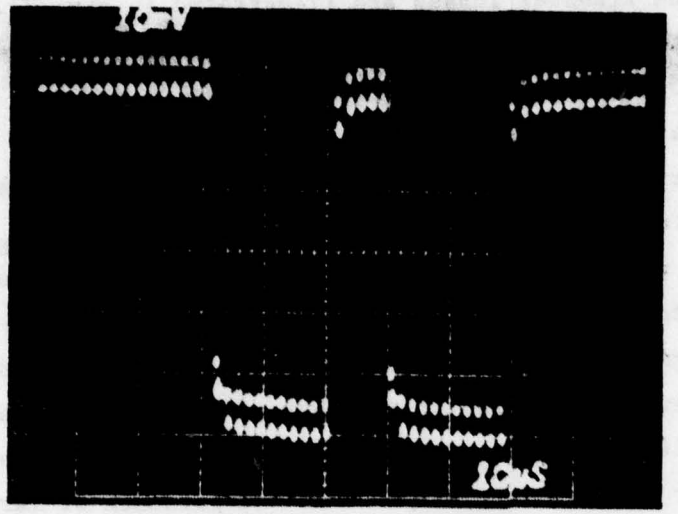
$N = 2.2 \times 10^6$

$\epsilon = 2.6 \times 10^{-7}$

Figure 25. Output waveforms of closed-loop low-loss 256-stage CCD at f_c = 1.0 MHz for initial values of Q_{SO} = 20 mV, Q_{S1} = 80 mV, and Q_{TB} = 100 mV.

The observation of the waveforms shown in Fig. 25 indicates that the transfer losses obtained in the low-loss CCD are about two orders of magnitude lower than the transfer losses of the same device operating in the standard two-phase CCD mode. Furthermore, the transfer losses of the low-loss CCD are qualitatively different from the standard CCD losses. First, the low-loss CCD losses appear to be symmetrical between the leading and the trailing edge of a signal pulse, i.e., about the same transfer loss is observed for the first "one" following a string of "zeros" as for the first "zero" following a string of "ones." Secondly, when a pulse input is used, the detected output after a large number of transfers (i.e., N on the order of 10^6) tends to have a long rise time that is some nonlinear function of the emission times of the bulk traps. A similar time constant is also present at the trailing edge of the pulse. The effect of the long time constant on the output waveforms is illustrated in Fig. 26. Here, we show two output waveforms of a 1024-stage closed-loop low-loss CCD in the double-pulse test at clock frequency of (a) 1.1 MHz, and (b) 140 kHz. As shown in (a) a short pulse with a total delay time, τ_D, of 0.2 s exhibits a transfer loss at the leading edge in combination with some attenuation. However, a long signal pulse after a time delay, τ_D, of 3 s exhibits a rise time that is directly related to the time delay between the two signal pulses. Note, the larger transfer loss at the leading edge of the first pulse is due to approximately one loop delay time between the second pulses and the first pulse. In connection with the long rise time obtained in the output of the low-loss CCD after a large number of transfers, we would like to point out that a short output pulse will appear at the output attenuated with an apparent transfer loss that is smaller than determined by Eq. (6).

It is also interesting to note that the signal charge used in this test is $Q_{S1} - Q_{SO} = 0.12$ pC, which corresponds to about 0.8×10^6 electrons. This means that while in the standard CCD mode the transfer loss of 1.6×10^{-5} per transfer corresponds to an average charge trapping of 13 electrons, in the low-loss CCD mode the transfer loss of 2.5×10^{-7} per transfer corresponds to an effective average charge trapping of 0.2 electrons per transfer.

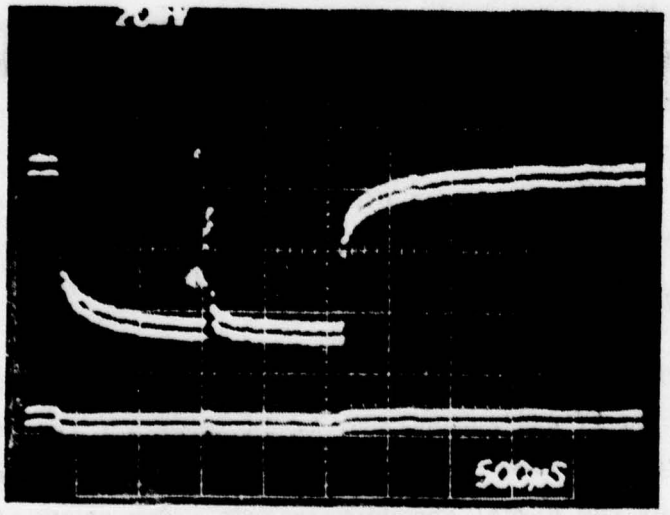


(a)

f_c = 1.1 MHz

τ_D = 0.2 s

N = 4.4×10^5



(b)

f_c = 140 kHz

τ_D = 3s

N = 8.4×10^5

Figure 26. Output waveforms for double-pulse test of trapping losses in closed-loop low-loss 1024-stage CCD.

2. Effect of Bias Charge

The operation of a 1024-stage closed-loop CCD in the low-loss mode and the effect of bias charge on the transfer losses are illustrated in Fig. 27. Parts (a) and (b) compare the detected signal for $Q_{SO}/Q_{TB} = 0.2$ after 1808 transfers with the detected signal after 4.4×10^5 transfers, from which a transfer loss of 5.7×10^{-7} per transfer is estimated. Comparison of (c) and (d) shows the improvement in the transfer loss from 2.8×10^{-7} to 2.4×10^{-7} as Q_{SO}/Q_{TB} is increased from 0.4 to 0.6. Then in (e) we show the operation with $Q_{SO}/Q_{TB} = 0.8$ in a negative input signal pulse or $Q_{S1}/Q_{TB} = 0.2$. In this case the transfer loss is 2.8×10^{-7} per transfer. Finally, the comparison of (c) with (f) shows the change in the pulse signal as the number of transfers, N, is increased from 4.4×10^5 to 2×10^6. The general conclusion of the above test is that signal bias charge $Q_{SO} = 0.4\ Q_{TB}$ is sufficient to achieve the minimum transfer losses. Also, the transfer loss for negative signal pulse in the presence of large Q_{SO} is lower but still comparable to the transfer loss for positive signal pulse.

3. Optimization of the Low-Loss Signal Regenerator

Our study of the operation of low-loss CCD loops indicates that the effective transfer losses are associated with a second-order trapping of charge by the bulk states from the trailing bias charge. The magnitude of the trailing bias charges is slowly modulated by the first-order trapping losses of the signal charge. The second-order trapping loss involves only the amount of trailing bias charge, Q_{TB1}, following the "one" signal charge, Q_{S1} that is larger than the preceding trailing bias charge, Q_{TB0}. In other words, the second-order trapping loss is due only to the charge signal difference,

$$\Delta Q_{TB} = Q_{TB1} - Q_{TB0}. \tag{7}$$

In view of the above transfer loss mechanism for the low-loss CCD, which is described further in Section IV and Appendix B, it is important that the trailing bias charge regenerated periodically at the low-loss signal regenerator be constant and independent of the signal charge magnitude. Our study of the operation of the regenerated trailing bias charge indicated that the incomplete charge transfer taking place when the signal charge is separated from the regenerated trailing bias charge (see Fig. 12(b) at t_4) produced a first-order

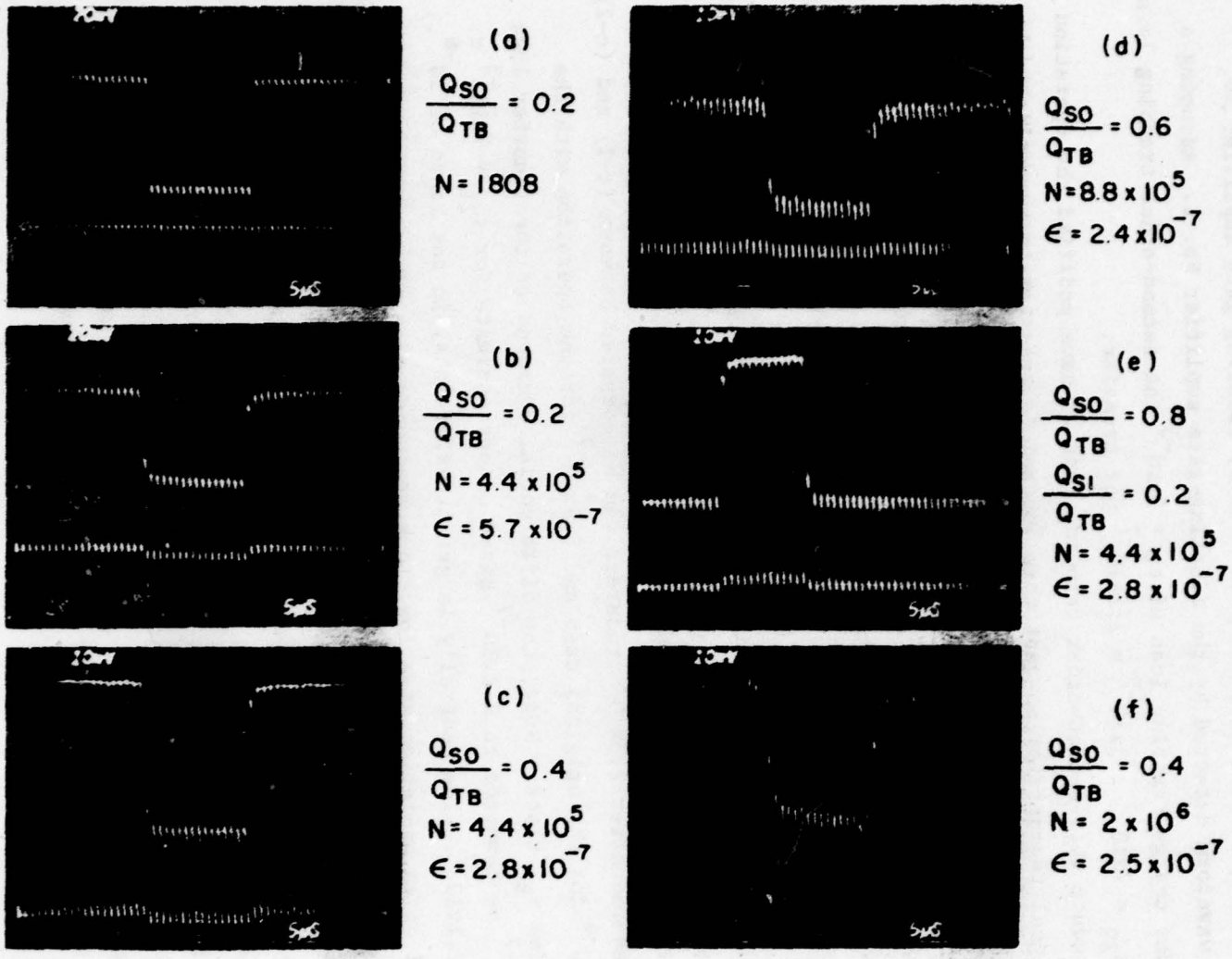


Figure 27. Comparison of transfer loss, ε, of closed-loop low-loss 1024-stage CCD at f_c = 2.2 MHz for various "zero" signal charge levels, Q_{SO}, and number of transfers, N.

transfer loss of about $7x10^{-3}$. We observed this effect initially by comparing the trailing-bias-charge waveform detected by floating-gate amplifier No. 1 with the waveform detected by the floating-gate amplifier No. 2. Assuming a first-order charge-trapping loss of $\varepsilon_1 = 3x10^{-5}$ the second-order trapping loss will be $\varepsilon_{2R} = 7x10^{-3} \times 3x10^{-5} = 2.1x10^{-7}$ per transfer.

To reduce this second-order trapping loss we have modified the operation of the signal regenerator so that this incomplete transfer is accomplished by a double ϕ_{BC} clock in two steps. First, the major part of the signal is transferred forward to the adjacent empty well and then the final level of the trailing bias is established with very small signal in the receiving well. The operation of a 1024-stage closed-loop low-loss CCD with the original and the double clock ϕ_{BC} is illustrated on the left and the right side of Fig. 28. The two types of bias-charge generating clocks are shown in part (a-1) and (a-2). Parts (b-1) and (b-2) show the step in the trailing bias charge, Q_{TB} due to the signal charge Q_{S1}. For the original ϕ_{BC} clock in (b-1) $\Delta Q_{TB}/Q_{S1}-Q_{SO} = 7x10^{-3}$. For the double ϕ_{BC} clock, $\Delta Q_{TB}/Q_{S1}-Q_{SO} = 10^{-3}$. The actual transfer losses measured after $2.8x10^5$ transfers can be compared between (c-1) and (c-2) as $1.07x10^{-6}$ for the original case and $8.9x10^{-7}$ for the operation with the double-pulse ϕ_{BC} clock. Note, the differential decrease of the transfer loss is $1.8x10^{-7}$ as compared to $2.1x10^{-7}$ based on our estimate for $\varepsilon_{2R} = 7x10^{-3} \times 3x10^{-5} = 2.1x10^{-7}$. The generally larger transfer loss, in the range of 10^{-6}, is typical of an operation at a low clock frequency of 4 kHz.

Since the effective transfer loss of the low-loss CCD is due to the second-order charge trapping of the trailing bias modulated by the signal charge, an experiment was performed whereby the signal detected at floating-gate amplifier No. 1, preceding the signal regenerator, was delayed by the proper amount to adjust the level of the trailing bias charge in an (adjustable) inverse direction to the signal charge. The result of this experiment with feed-forward-compensated signal regeneration is illustrated in Fig. 29, where an effective transfer loss of $4.5x10^{-8}$ per transfer was achieved.

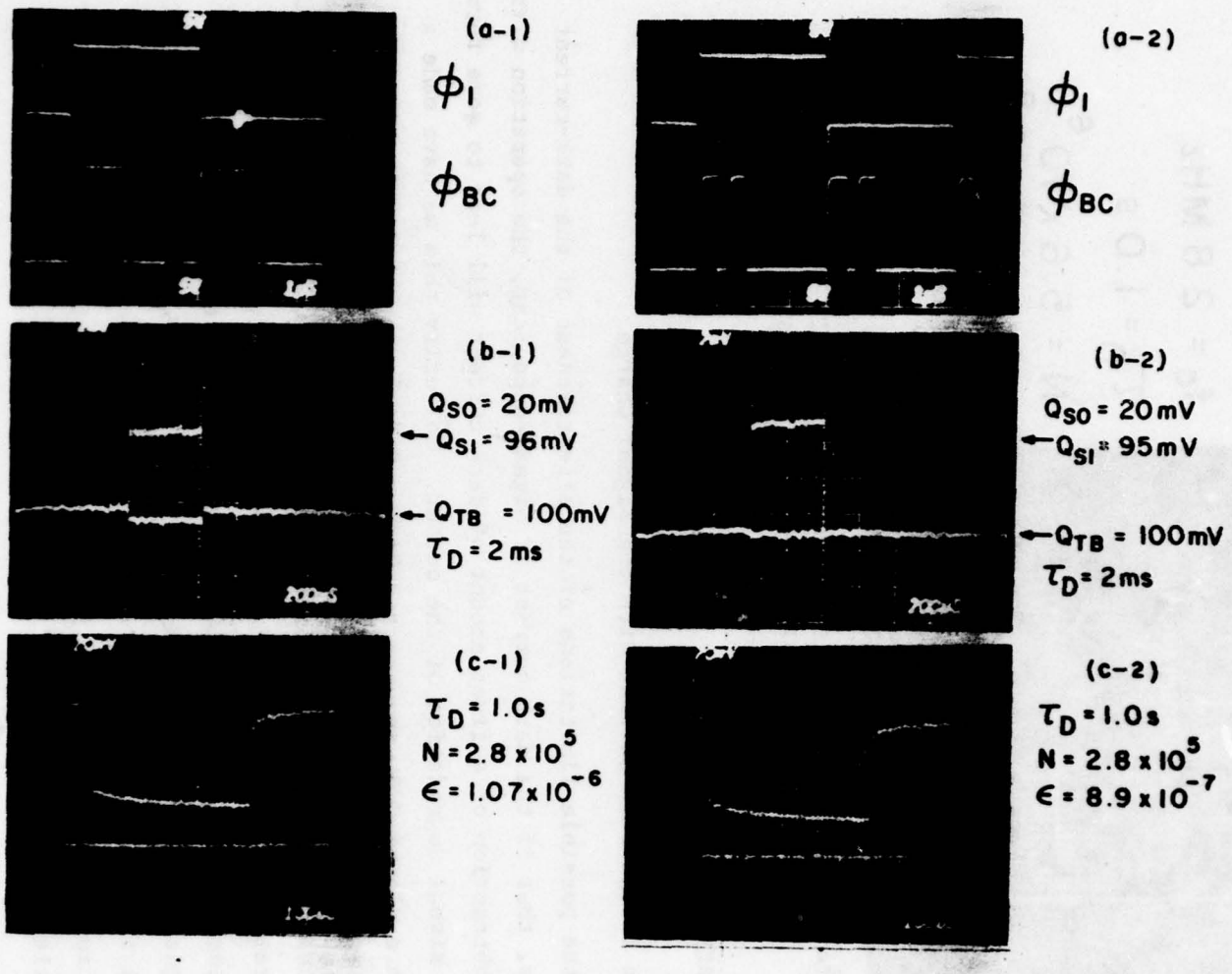


Figure 28. Comparison of the operation of a closed-loop low-loss 1024-stage CCD at f_c = 4 kHz using the original ϕ_{BC} clock (in the left side of the figure) and the double ϕ_{BC} clock (in the right side of the figure).

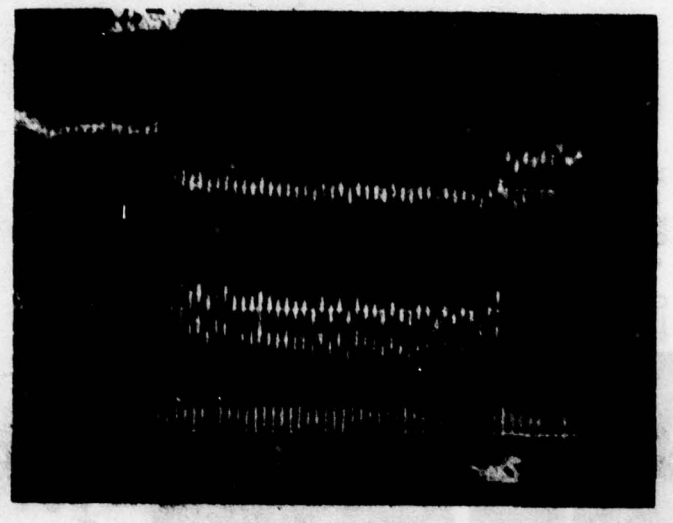


Figure 29. Operation of closed-loop low-loss 1024-stage CCD with feed-forward-compensated signal regeneration.

E. DARK-CURRENT SUBTRACTION

1. Variation of the Dark Current With the Signal Charge

One of the possible limitations of the effectiveness of the dark-current subtractor is, that if the dark current is signal-dependent, the operation with a periodic subtraction of a fixed amount of dark current will lead to some form of nonlinear signal degradation of the output. To verify this we have made a test in which a closed CCD was operated with certain constant levels of signal charge while the dark-current subtractor was adjusted to remove the excess signal. In this test, the subtracted charge, which was measured by an electrometer as a drain current, I_{DCS}, was equal to the thermally generated dark current. The measured curves for two 1024-stage devices of the drain-current, I_{DCS}, representing the average thermally generated dark current, as a function of the signal charge, Q_S, are shown in Fig. 30. These tests indicate that in our buried-channel CCDs there is a large range of signal for which the dark current is relatively constant.

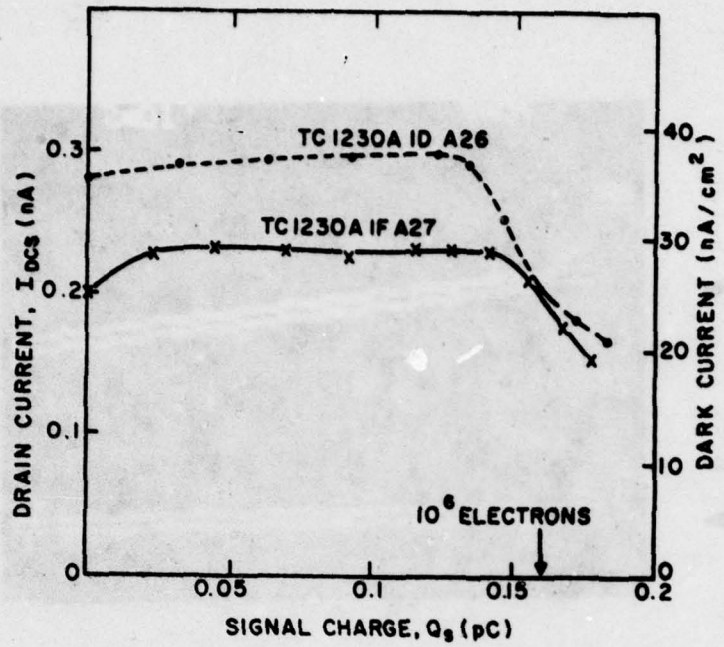


Figure 30. Variation of dark current with signal charge level.

2. Performance of the Dark-Current Subtractor

The operation of the dark-current subtractor is illustrated in Figs. 31, 32, and 33. In Fig. 31 we are comparing the operation of a 1024-stage closed-loop low-loss CCD without subtracting the dark current in (a) and with dark-current subtraction in (b). This comparison is made again in Fig. 32, but with only the signal bias charge, Q_{SO}, and the trailing bias charge, Q_{TB}, introduced in the loop. As we see in Fig. 32(a) the signal bias charge, Q_{SO}, increases to the level of the trailing bias charge, Q_{TB}, (which is periodically regenerated) in about 0.4 s. Then in about 0.7 s, Q_{SO} reaches a full well and starts spilling into the trailing bias charge. The operation of the closed-loop low-loss CCD is shown in Fig. 32(b) with the dark-current subtractor adjusted to remove the excess thermally generated current. Now, we observe no accumulation of dark current for a total delay time of the signal in the closed loop of 7.5 s.

The performance of the closed-loop CCD operating in the standard CCD mode in Fig. 33(a) with transfer loss of 5.4×10^{-5} per transfer and a delay time, τ_D, of 0.5 s is compared with the low-loss operation in Figs. 33(b), (c), and (d) with the delay time, during which the signal is being recirculated in the

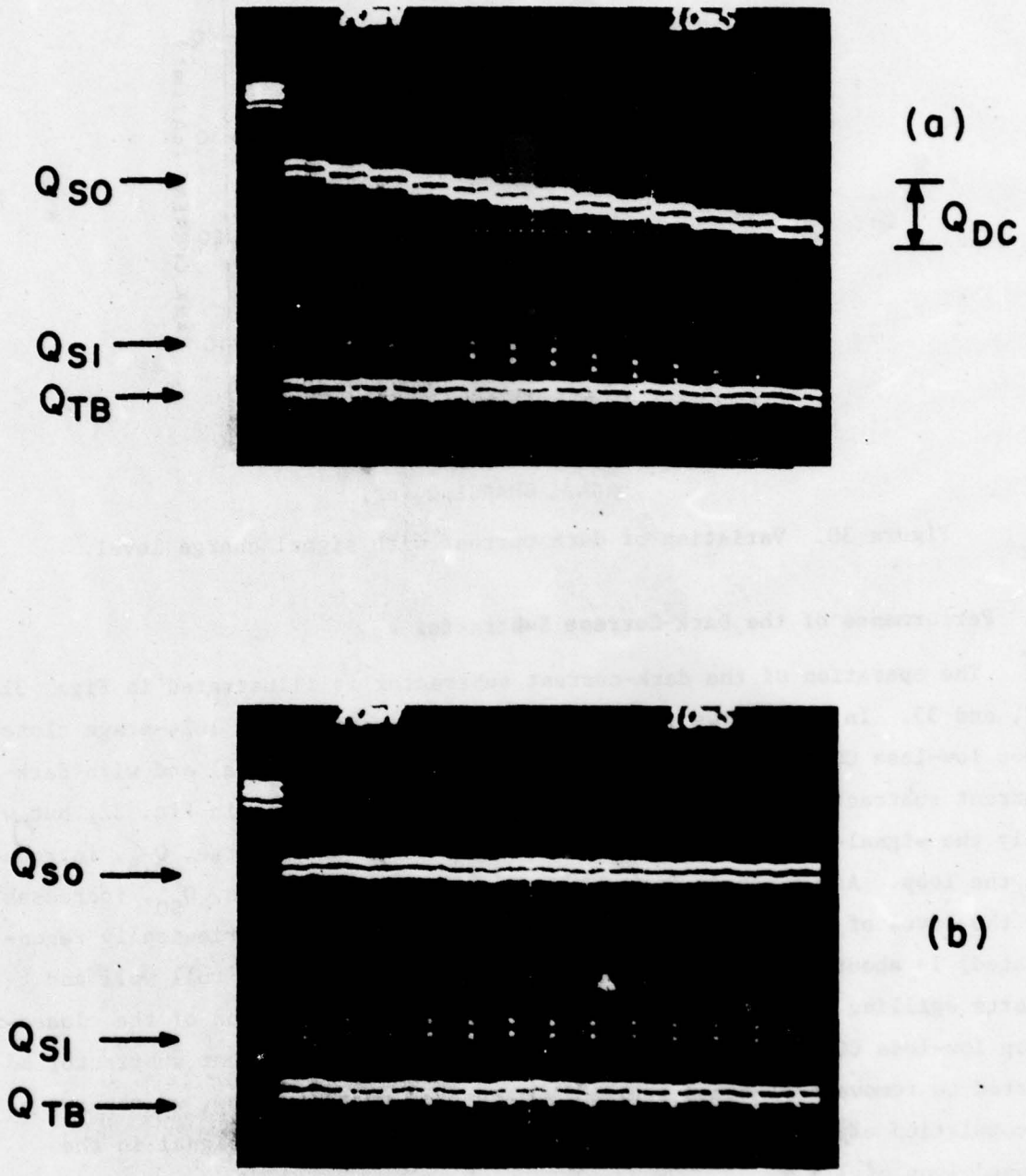


Figure 31. Operation of the closed-loop low-loss 1024-stage CCD at f_c = 140 kHz in (a) with dark-current subtractor OFF, and in (b) for dark-current subtractor ON.

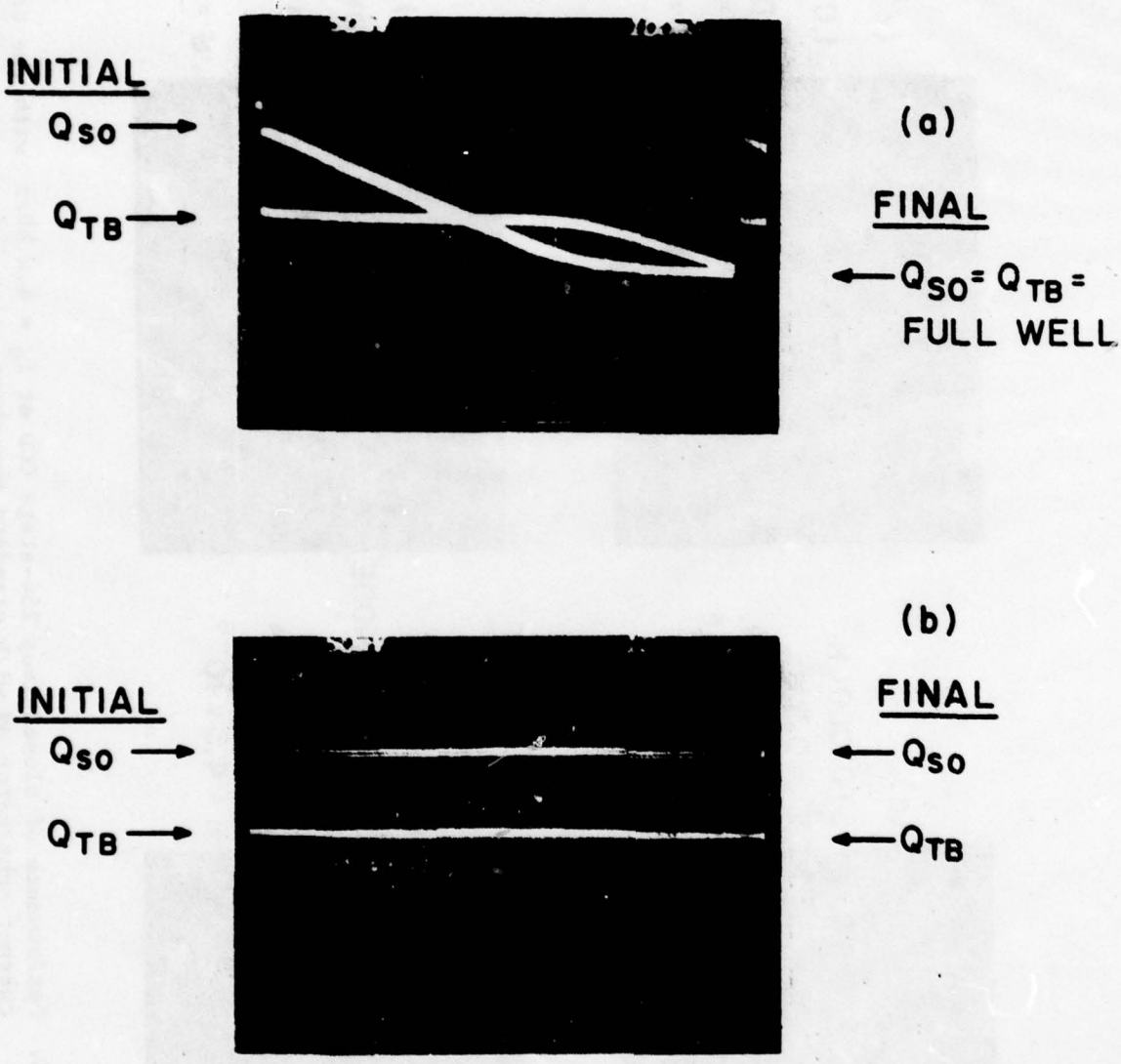


Figure 32. Waveforms of zero-level signal, Q_{SO}, and trailing bias charge, Q_{TB}, in closed-loop low-loss 1024-stage CCD at f_c = 140 kHz: (a) for dark-current subtractor OFF and total delay time τ_D = 0.925 s and (b) for dark-current subtractor ON and τ_D = 7.4 s.

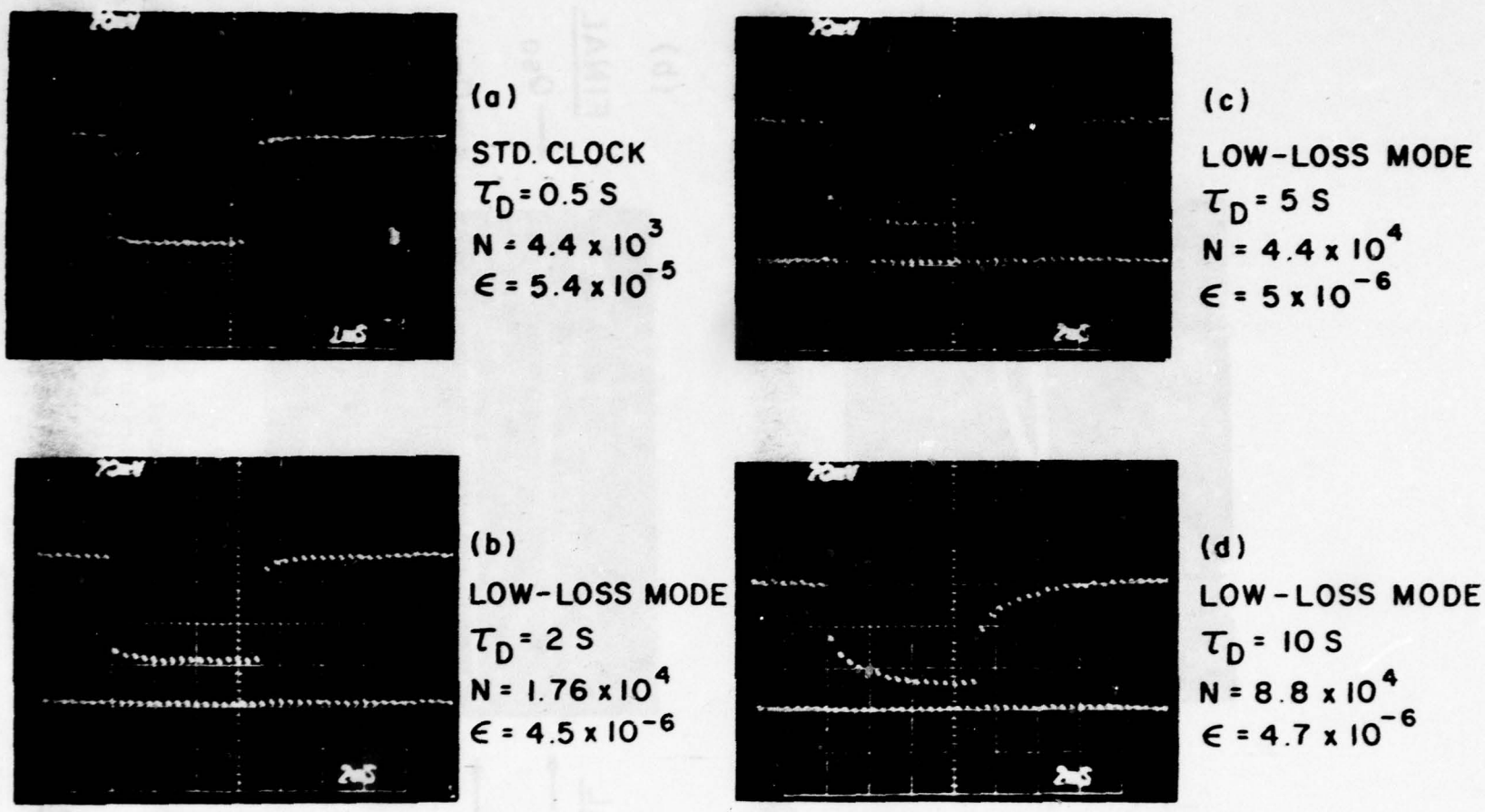


Figure 33. Performance of closed-loop 256-stage CCD at f_c = 4.4 kHz: with the dark-current subtractor ON with standard two-phase clock mode in (a), and low-loss mode in (b), (c), and (d).

loop, progressively increased from 2 s, to 5 s, and finally to 10 s. The waveform in Fig. 33 demonstrates that a signal can be recirculated for up to 10 s with the dark-current subtractor in the loop. In fact, the only limitation on how long the signal can be delayed or recirculated is not imposed by the dark current but by the transfer losses which tend to be larger at lower clock frequencies. As indicated in the next section, the shot noise introduced into the CCD by the dark current does not seem to accumulate appreciably.

3. Noise Introduced by the Dark Current

One of the more suprising results of our test of the closed-loop low-loss CCDs is that we have found that with the dark-current subtractor in the loop the dark-current shot noise does not seem to accumulate. This is demonstrated in Fig. 34. Here, the signal is in the form of a constant bias charge, Q_{SO}. The photograph in Fig. 34(a) shows the detected waveform during the first recirculation of the signal where we observe a peak-to-peak noise level of $V'_{(p-p)} = 0.8$ mV, or $V'_{rms} = 0.13$ mV. For $Q_{SO} = 95$ mV, we estimate the initial $s/n_{rms} = 57$ dB. Then in Fig. 34(b) after a recirculation delay time of 1.0 min, the value of $V''_{(p-p)} \approx 1.2$ mV, and the final $s/n_{rms} = 54$ dB. Since a full well of charge is generated in this device in about 0.5 s, in 1.0 min 120 full wells of dark-current charge are generated. A full well corresponds to 100 mV, 0.12 pC, or 7.5×10^5 electrons. Thus, the expected shot noise due to the full well of dark current is 9400 electrons. However, the rms noise in Fig. 34(a) of $V'_{N(rms)} = 0.13$ mV corresponds to $N'_{rms} = 975$ electrons. Then, after a delay time of 1.0 min with 120 full wells of dark current subtracted, the measured noise corresponds to $V''_{N(p-p)} = 1.2$ mV, $V''_{N(rms)} = 0.2$ mV, or $N''_{rms} = 1500$ electrons. Assuming that in Fig. 34(a) all the noise is due to the output amplifier, then in Fig. 34(b),

$$\sqrt{N^2_{\text{amplifier}} + N^2_{\text{dark current}}} = 1500$$

or

$N_{\text{dark current}} = 1133$ electrons, corresponding to the effective number of rms noise electrons due to the dark-current generation of 120 full wells of charge.

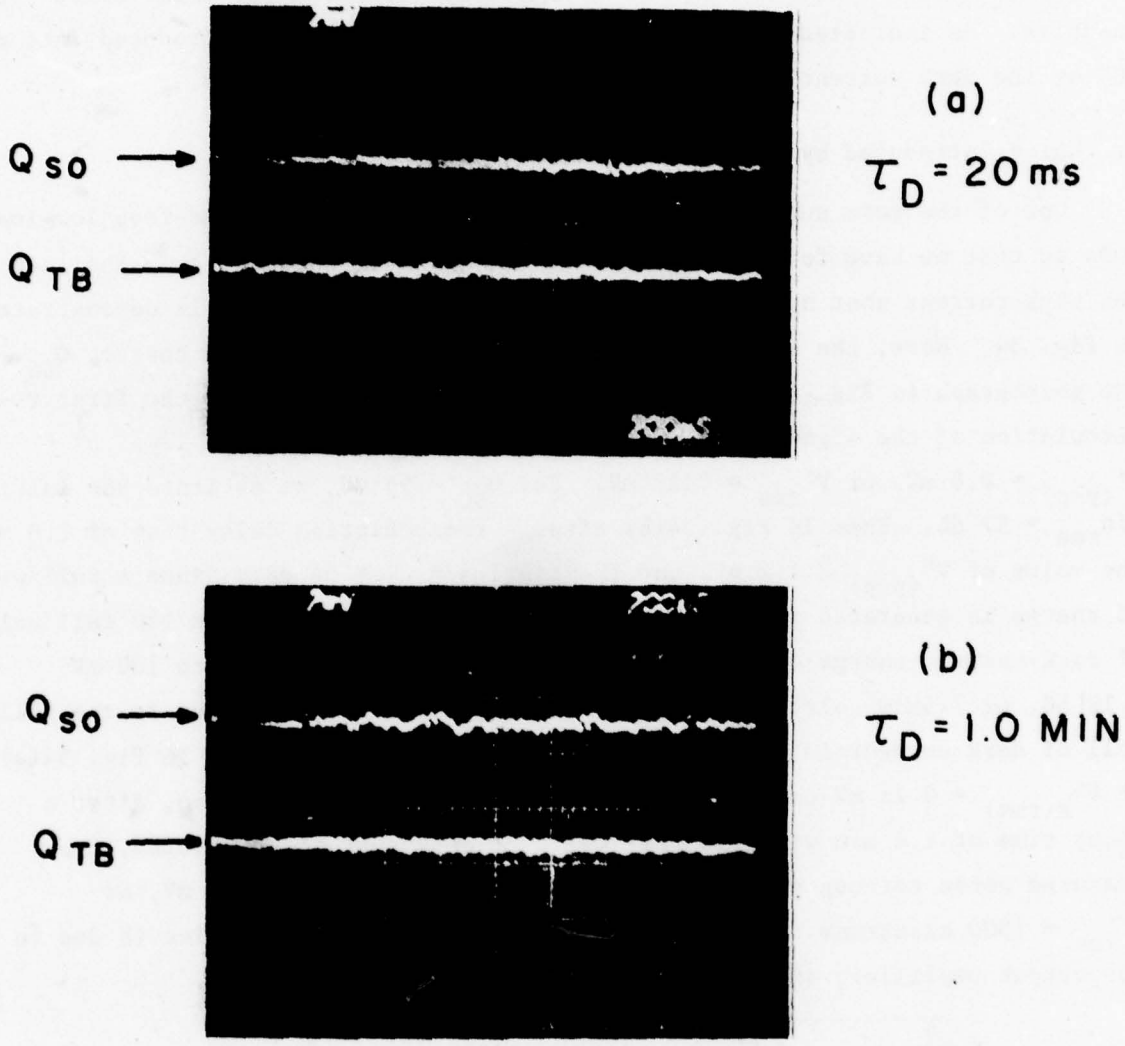


Figure 34. Amplified output waveforms of Q_{SO} = 95 mV and Q_{TB} = 100 mV for closed-loop low-loss 256-stage CCD at f_c = 140 kHz, showing (a) the initial noise level, and (b) the steady-state noise level (after a delay time τ_D = 1.0 min).

The above number should be compared to the calculated rms noise of 9400 electrons corresponding to 120 full wells of dark current. The above reduction of the dark-current noise may be attributed to the signal correlation between adjacent charge packets due to the charge transfer losses. This means that while the shot noise due to the dark current will saturate due to the signal averaging effect caused by the transfer losses, we cannot also maintain a signal in the loop indefinitely without dispersing it. There is, however, at least one application where we can use this effect. Namely, a continuously recirculating low-loss CCD loop with a proportional charge subtractor operating as a synchronous signal correlator. In this case the gain of the loop will be

$$A = \frac{1}{m} \tag{8}$$

where m is the fraction of charge removed from the loop by the proportional charge subtractor.

F. SYNCHRONOUS SIGNAL CORRELATOR EXPERIMENT

In order to evalute the performance of the closed-loop low-loss CCD in applications such as radar post-detection correlation, the TC1230B 256-stage delay line was operated as a synchronous recirculating correlator with a continuous input. The input signal consisted of a repetitive pulse occurring at each loop cycle period (256 clock cycles) mixed with random noise. The power spectrum of this random noise is shown in Fig. 35. Continuous S_{1A} strobe pulses were applied to the CCD input stage so that input signal charge was added continuously tc the signal charge already recirculating in the loop; however, the trailing bias charges were only introduced once (during Loop Cycle 0). The input-signal bias level was adjusted to be about 10% of a full well, and then the dark-current subtractor was adjusted to subtract out this 10% so that a steady-signal bias level of about 20% was maintained in the recirculating signal. (Note: This steady-signal bias level was determined by the signal-regeneration stage ϕ_{BC} skimming level.) The results of this experiment for 100 recirculations at a clock frequency of 1.1 MHz are shown in Fig. 36(a) for the case without random noise added to the input and in Fig. 36(b)

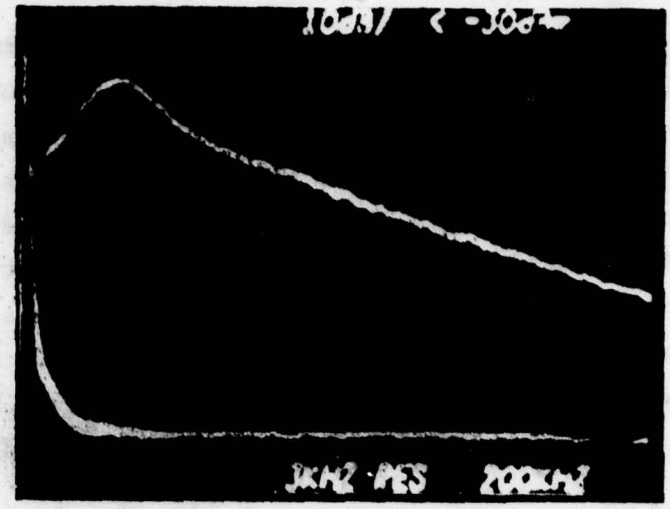


Figure 35. Power spectrum of external random-noise generator with 3-kHz resolution. Vertical scale: 10 dB/div. Horizontal scale: 200 kHz/div.

for the case with random noise. The top trace in each oscillograph shows the input signal applied to G_{1A} and the bottom trace shows the output signal after 100 times around the CCD loop (total delay τ_D = 23 ms).

In the case of Fig. 36(b) the measured input s/n = -5.5 dB and the measured output s/n = +12 dB. Thus, using the closed-loop low-loss CCD as a synchronous recirculating correlator, we have demonstrated an improvement in the signal-to-noise ratio of +17.5 dB for 100 summations of the signal which is comparable to the theoretical limit of $\sqrt{100}$ = 20 dB.

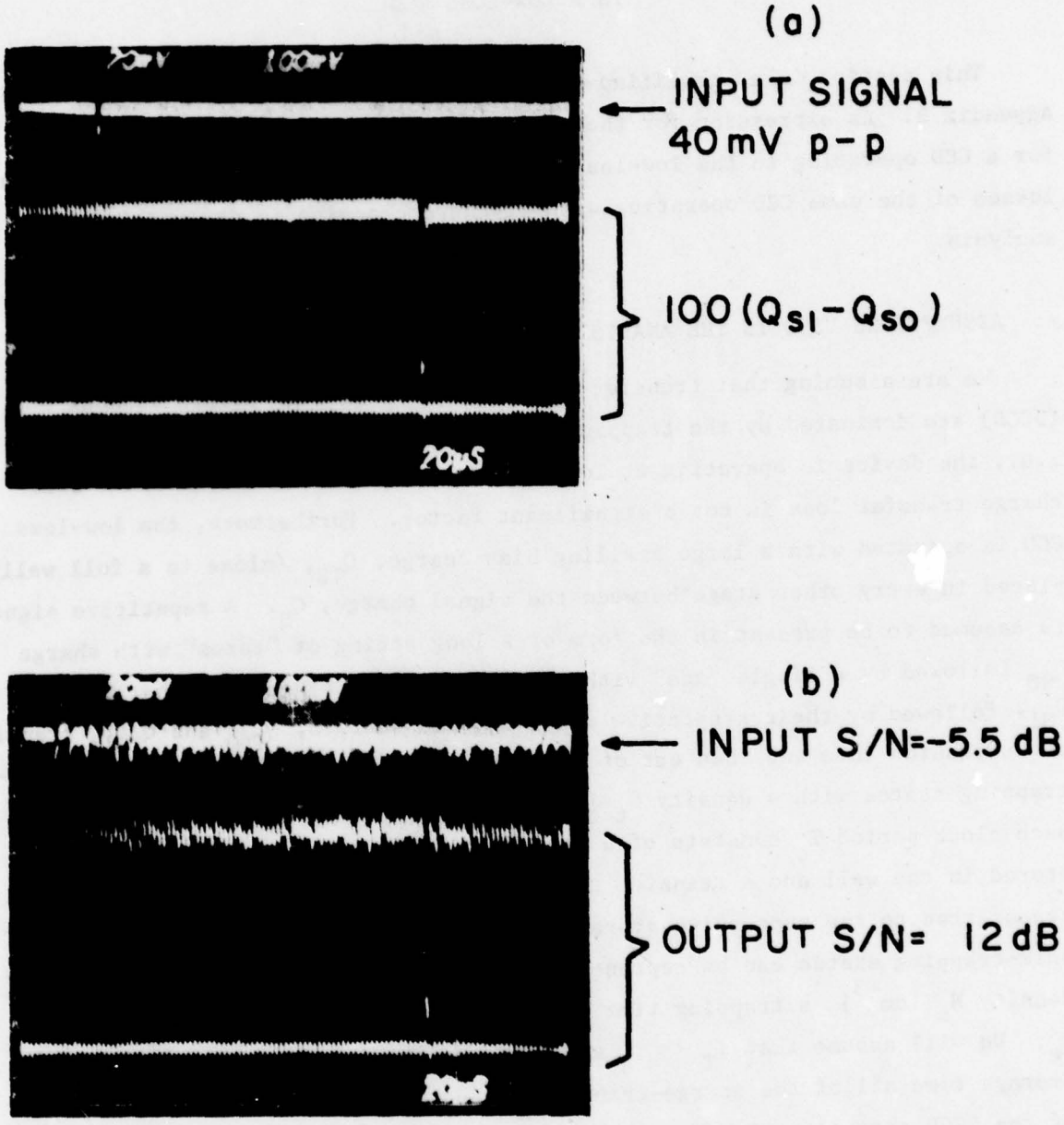


Figure 36. Operation of the 256-stage closed-loop low-loss CCD at 1.1 MHz as a synchronous recirculating correlator with continuous input (top trace) showing the floating-gate output summation after 100 recirculations (bottom trace): (a) without noise at the input, and (b) with noise added to the input signal.

SECTION IV

SIMPLIFIED ANALYSIS OF THE EFFECTIVE TRANSFER LOSSES IN A LOW-LOSS CCD

This section is a simplified version of the analysis presented in Appendix B. An expression for the effective (second-order) transfer losses for a CCD operating in the low-loss mode in terms of the first-order transfer losses of the same CCD operating with standard clocking is derived in this analysis.

A. ASSUMPTIONS USED IN THE ANALYSIS

We are assuming that transfer losses in the low-loss buried-channel CCD (BCCD) are dominated by the trapping of charge in the bulk-trapping states, i.e., the device is operating at low-to-medium clock frequencies where free-charge transfer loss is not a significant factor. Furthermore, the low-loss CCD is operated with a large trailing bias charge, Q_{TB}, (close to a full well) placed in every other stage between the signal charge, Q_S. A repetitive signal is assumed to be present in the form of a long string of "zeros" with charge Q_{SO} followed by a single "one" with charge Q_{S1}. The signal charges, Q_{SO} and Q_{S1}, followed by their respective trailing bias charges, Q_{TBO} and Q_{TB1}, transfer in succession into and then out of the same stage of the BCCD containing bulk-trapping states with a density N_t [cm^{-3}]. A two-phase BCCD is assumed where each clock period T_c consists of a storage time T_s during which the charge is stored in the well and a transfer time T_T during which the charge is being transferred to the successive storage well. Let us assume further that the bulk-trapping states can be represented with a single trapping state having a density N_t [cm^{-3}], a trapping time constant τ_t and an emission time constant τ_e. We will assume that $\tau_T << T_s$ and $\tau_t << \tau_e$. This means that during the storage time all of the charge-trapping states will be filled in the volume of the BCCD channel containing the signal charge, Q_{S1} or Q_{SO}, or the trailing bias charge, Q_{TB}.

B. FIRST-ORDER CHARGE TRANSFER LOSS

The trapping and emission of charge in the operation of the low-loss CCD is illustrated in Fig. 37. As mentioned previously, the repetitive signal is in the form of a very long string of "zeros" with signal charge Q_{S0} followed by a single "one" with signal charge Q_{S1}. At the input stage of the CCD (or immediately following a signal-regeneration stage) the signal-charge levels Q_{S0} and Q_{S1}, and trailing-bias-charge level Q_{TB} indicated by the dotted lines in Fig. 37 are present. The solid lines in Fig. 37 indicate the corresponding charge levels following a single transfer along the CCD register. Note that due to the first-order trapping losses the signal-charge levels increase, and the trailing-bias-charge levels decrease correspondingly. We will now show that to first order $\Delta Q_{S0} = -\Delta Q_{TB0}$ so that in a low-loss CCD mode the net first-order loss for the sum charge packet $Q_{SUM} = Q_{S0} + Q_{TB0}$ is zero.

Our analysis is based on conservation of the total charge (mobile and trapped) in the BCCD. The net change in the total charge contained within a given volume V of the BCCD is equal to the difference between the charge Q (initial) transferred into V and the charge Q (final) transferred out of V.

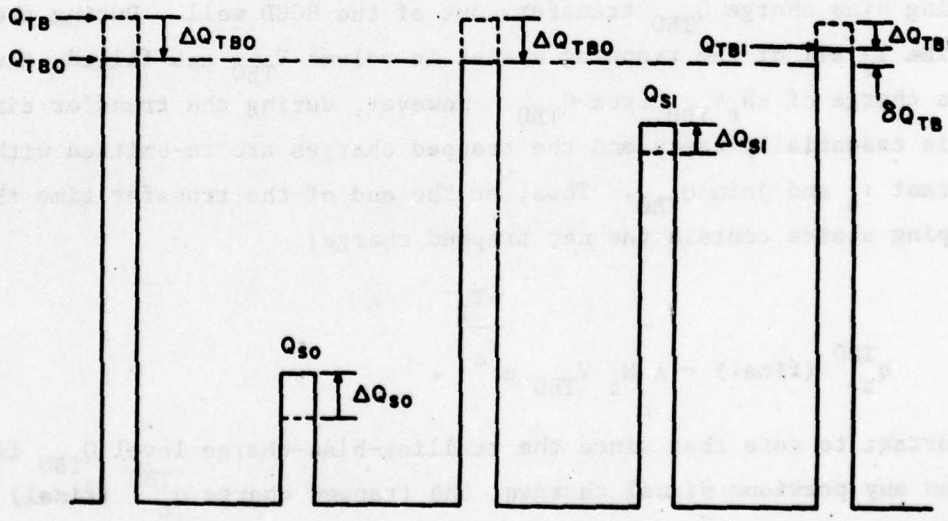


Figure 37. Trapping and emission of charge in the operation of the low-loss CCD.

Just before Q (initial) enters, the BCCD well is essentially empty and contains only the trapped charge q_t (initial). Similarly, after Q (final) transfers out of the well, only the trapped charge q_t (final) is present. Therefore, we have:

$$\Delta Q \equiv Q \text{ (final)} - Q \text{ (initial)} = q_t \text{ (initial)} - q_t \text{ (final)} . \quad (9)$$

For the transfer of the signal charge Q_{SO} and the trailing bias charge Q_{TBO}, Eq. (9) becomes:

$$\Delta Q_{SO} = q_t^{SO} \text{ (initial)} - q_t^{SO} \text{ (final)} \quad (10)$$

and

$$\Delta Q_{TBO} = q_t^{TBO} \text{ (initial)} - q_t^{TBO} \text{ (final)} . \quad (11)$$

Since the trapped charge q_t^{TBO} (initial) is the same as q_t^{SO} (final), the net change in the sum-charge packet $Q_{SUM} = Q_{SO} + Q_{TBO}$ is:

$$\Delta Q_{SUM} = \Delta Q_{SO} + \Delta Q_{TBO} = q_t^{SO} \text{ (initial)} - q_t^{TBO} \text{ (final)} . \quad (12)$$

Let us calculate how much charge q_t^{TBO} (final) is trapped in volume V_{TBO} after the trailing bias charge Q_{TBO} transfers out of the BCCD well. During the storage time T_S all of the trapping states in volume V_{TBO} are filled, thus trapping a charge of eN_tV_{TBO} from Q_{TBO}. However, during the transfer time T_T, the BCCD is essentially empty and the trapped charges are re-emitted with a time constant τ_e and join Q_{TBO}. Thus, at the end of the transfer time the bulk trapping states contain the net trapped charge:

$$q_t^{TBO} \text{ (final)} = e\, N_t\, V_{TBO}\, e^{\frac{-T_T}{\tau_e}} . \quad (13)$$

It is important to note that since the trailing-bias-charge level Q_{TBO} is larger than any previous signal charges, the trapped charge q_t^{TBO} (final) given by Eq. (13) is independent of the preceding signals. Since the signal charge Q_{SO} is immediately preceded by another trailing bias charge Q_{TBO}, the initial

trapped charge q_t^{S0} (initial) in Eq. (12) is also equal to q_t^{TBO} (final). Therefore, the net change in the sum charge packet due to first-order losses is zero:

$$\Delta Q_{SUM} = \Delta Q_{S0} + \Delta Q_{TBO} = 0 \ . \tag{14}$$

Referring again to Fig. 37, the first-order charge transfer losses ΔQ_{S0} and ΔQ_{S1} may be calculated from the trailing-edge fractional charge transfer loss ε_{TE} as follows:

$$\Delta Q_{S0} = - \Delta Q_{TBO} = \varepsilon_{TE} \ (Q_{TBO} - Q_{S0}) \tag{15}$$

and

$$\Delta Q_{S1} = - \Delta Q_{TB1} = \varepsilon_{TE} \ (Q_{TBO} - Q_{S1}) \ ; \tag{16}$$

ε_{TE} is measured from the increase in the first "zero" signal following a string of "ones" when the CCD is operated with standard clocks and the "zero" signal bias level is on the order of Q_{S0}.

C. SECOND-ORDER CHARGE TRANSFER LOSS

As we discussed in the previous section, during each transfer in a low-loss CCD, the signal charge increases by a small amount ΔQ_S and the trailing bias charge following the signal charge decreases by exactly the same amount. However, we see from Eqs. (15) and (16) that ΔQ_{S0} is larger than ΔQ_{S1} and therefore the trailing bias charge Q_{TBO} decreases more than the trailing bias charge Q_{TB1} during each transfer. This causes a step in the level of the trailing bias charge at each transfer which has the value:

$$\delta Q_{TB} \equiv \Delta Q_{TBO} - \Delta Q_{TB1} = \varepsilon_{TE} \ (Q_{S0} - Q_{S1}) \ . \tag{17}$$

We now assume that the first-order losses are sufficiently low so that δQ_{TB} is essentially constant and independent of the number of transfers i following a signal-regeneration stage. Therefore, at the i^{th} transfer, the difference in the level of the trailing bias charge Q_{TBO} and Q_{TB1} will be:

$$Q_{TBO} - Q_{TB1} = i \ \delta Q_{TB} = i \ \varepsilon_{TE} \ (Q_{S0} - Q_{S1}) \ . \tag{18}$$

By following an analysis similar to that used to derive Eq. (12), we find that the change in the sum charge packet $\Delta Q_{SUM} = \Delta Q_{S1} + Q_{TB1}$ for a single "one" following a string of "zeros" is:

$$\Delta Q_{SUM} = \Delta Q_{S1} + \Delta Q_{TB1} = q_t^{S1}\ (\text{initial}) - q_t^{TB1}\ (\text{final})\ . \tag{19}$$

Since the signal charge Q_{S1} is immediately preceded by a trailing bias charge Q_{TB0}, the trapped charge q_t^{S1} (initial) is the same as q_t^{TB0} (final). Thus, Eq. (19) may be written as:

$$\Delta Q_{SUM} = q_t^{TB0}\ (\text{final}) - q_t^{TB1}\ (\text{final})\ . \tag{20}$$

The charge loss ΔQ_{SUM} in Eq. (20) has the same form as in the case of a CCD with standard clocks having a string of Q_{TB0} bias charges followed by a single Q_{TB1} charge which is slightly larger. This allows us to write ΔQ_{SUM} in terms of the leading-edge loss ε_{LE} measured from the decrease in the first "one" signal following a string of "zeros" when the CCD is operated with standard clocks and the "zero" signal bias level is on the order of Q_{TB0}:

$$\Delta Q_{SUM} = \varepsilon_{LE}\ (Q_{TB0} - Q_{TB1})\ . \tag{21}$$

Substituting Eq. (18) into Eq. (21), we find the second-order loss for the sum-charge packet during the i^{th} transfer following a signal-regeneration stage is:

$$\Delta Q_{SUM}(i) = i\ \varepsilon_{LE}\varepsilon_{TE}\ (Q_{S0} - Q_{S1})\ . \tag{22}$$

Therefore, the average second-order fractional transfer loss for n transfers is:

$$\varepsilon_2 = \frac{\sum_{i=1}^{n} |\Delta Q_{SUM}(i)|}{n(Q_{S1}-Q_{S0})} \tag{23}$$

or

$$\varepsilon_2 = \frac{n+1}{2}\ \varepsilon_{LE}\varepsilon_{TE}\ . \tag{24}$$

D. OPTIMUM NUMBER OF TRANSFERS BETWEEN REGENERATION STAGES

Since the signal charge and trailing bias charge are combined at the signal-regeneration stage in the low-loss CCD, the combined charge sees a first-order loss due to bulk-trapping during two transfers at this point. For a device having n transfers between signal-regeneration stages, the average charge transfer loss due to the first-order losses at the signal-regeneration stage is:

$$\varepsilon_{1R} = 2\,\varepsilon_{LE}/n\ . \tag{25}$$

Adding Eqs. (24) and (25) we find that the total second-order charge transfer loss $\varepsilon_{TOT} = \varepsilon_{1R} + \varepsilon_2$ is a function of n:

$$\varepsilon_{TOT}(n) = \varepsilon_{LE}\left(\frac{2}{n} + \frac{n+1}{2}\,\varepsilon_{TE}\right)\ . \tag{26}$$

It is evident from Eq. (26) that there is an optimum value, n_{OPT}, for the number of transfers between regeneration stages which will minimize the total transfer loss. Setting the derivative $\frac{d\varepsilon_{TOT}}{dn}$ equal to zero, we find:

$$n_{OPT} = 2/\sqrt{\varepsilon_{TE}} \tag{27}$$

and

$$\varepsilon_{TOT}(\min) = \varepsilon_{LE}\ (\sqrt{\varepsilon_{TE}} + 1/\sqrt{\varepsilon_{TE}}) \tag{28}$$

for $n >> 1$. Typical values for n_{OPT} as a function of ε_{TE} are shown below:

ε_{TE}	n_{OPT}
1×10^{-4}	200
5×10^{-5}	282
2×10^{-5}	447
1×10^{-5}	632

E. EFFECT OF SIGNAL-REGENERATOR PERFORMANCE ON SECOND-ORDER CHARGE TRANSFER LOSS

Our study of the operation of the signal-regeneration stage (see Section III.D.E) indicates that the incomplete (bucket-brigade mode) charge transfer taking place when the signal charge is skimmed from the trailing bias charge produces a first-order loss $\varepsilon_{BB} \approx 7\text{x}10^{-3}$ when we use a normal ϕ_{BC} clock pulse. The resulting modulation of the trailing-bias-charge level by the signal charge causes an average second-order fractional charge transfer loss per transfer of:

$$\varepsilon_{2R} = \varepsilon_{LE}\,\varepsilon_{BB} \,. \tag{29}$$

Therefore, the total second-order charge transfer loss in this case is:

$$\varepsilon_{TOT} = \varepsilon_{LE}\left(\frac{2}{n} + \frac{n+1}{2}\,\varepsilon_{TE} + \varepsilon_{BB}\right). \tag{30}$$

F. SAMPLE CALCULATION

The following first-order charge transfer losses were measured on a TC1230 256-stage CCD operating with standard 2ϕ clocks at a frequency of 1.1 MHz:

$$\varepsilon_{LE} = 2.1\text{x}10^{-5}$$

$$\varepsilon_{TE} = 1.0\text{x}10^{-5}$$

$$\varepsilon_{BB} = 7\text{x}10^{-3} \,.$$

The leading-edge transfer loss ε_{LE} was measured in a double pulse test with 20% bias charge and a period of 250 µs between pulses corresponding to the recirculation period of the closed-loop CCD (cf. Fig. 23). Substituting the above values into Eq. (30) yields a calculated value for the effective second-order charge transfer loss of $\varepsilon_{TOT} = 2.9\text{x}10^{-7}$ which compares to a measured value of $\varepsilon = 2.4\text{x}10^{-7}$ for the same device operating in the low-loss mode.

SECTION V

CONCLUSIONS

To verify the proposed low-loss CCD concept we have designed, fabricated, and tested 256-stage and 1024-stage closed-loop CCD structures that can be operated in the low-loss CCD mode by periodic signal regeneration. With these two devices operating in the low-loss CCD mode we have demonstrated a reduction in the effective charge transfer losses by two orders of magnitude. While the typical transfer loss of our standard buried-channel CCD is about 2×10^{-5} per transfer, in the low-loss CCD mode we have achieved a transfer loss of 2.5×10^{-7} per transfer. In fact, in the case of the feed-forward-compensated signal regenerator we have observed a transfer loss as low as 4.5×10^{-8} per transfer.

We have demonstrated that by operating the closed-loop low-loss CCDs with a dark-current subtractor in the loop we can eliminate the effect of the dark current for very long delay times. We have stored a signal in the loop for up to 10 s during which an estimated 20 full wells of thermally generated charge were subtracted from the loop. The noise generated by the dark current tends to saturate at a low level maintaining a s/n_{rms} = 54 dB independent of the recirculation time.

We have developed a trapping-loss model for the operation of the low-loss CCD. On the basis of this model we have derived a simple formula for predicting the transfer loss of the low-loss CCD on the basis of transfer loss data for a standard buried-channel CCD.

The closed-loop low-loss CCD was operated as a synchronous signal correlator. With 100 signal recirculations we have demonstrated an improvement in the signal-to-noise ratio from -5.5 dB to 12 dB.

REFERENCES

1. W. F. Kosonocky and D. J. Sauer, "CCD Long-Time Delay Line," Air Force Systems Command Contract No. F19628-77-C-0176, Scientific Interim Report, RADC-TR-78, July 1978.

2. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Rev. 36, 566-593 (1975).

3. W. F. Kosonocky and J. E. Carnes, "Design and Performance of Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," Digest of Technical Papers, 1973 International Electron Device Meeting, Washington, D.C., 123-125, Dec. 3-5, 1973.

4. C. H. Sequin and M. F. Tompsett, *Charge Transfer Devices* (Academic Press, New York, 1975), pp. 70-108.

5. M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of Charge-Coupled Devices," IEEE Trans. Electron Devices ED-20, 45-55 (1973).

6. A. M. Mohsen and M. F. Tompsett, "The Effects of Bulk Traps on the Performance of Bulk Channel Charge-Coupled Devices," IEEE Trans. Electron Devices ED-21, 701-712 (1974).

7. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Rev. 34, 164-202 (1973).

8. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Rev. 33, 327-343 (1972).

APPENDIX A

LOW-LOSS CCD TEST SYSTEM

A. GENERAL DESCRIPTION

The electronic tester for the TC1230 closed-loop low-loss CCD consists of a power supply and control logic. A description of the hardware is given below:

1. Power Supply

The power supply provides the dc biases needed to operate the device. The clock waveform amplitude and dc bias, and dc potentials applied to the chip may be varied by means of the front panel controls which are shown in Fig A-1.

The front panel digital meter may be used to monitor any of the 14 adjustable voltages provided by the supply. Spares are provided for two additional voltage settings. The voltmeter selection is made by the combination of the 8-position rotary switch labeled "BIAS SELECTOR" and adjacent toggle switch labeled "UPR" and "LWR". The LED lights located above the voltage controls identify which column the voltmeter is monitoring. Either the upper or lower control of a particular column is measured depending on the position of the toggle switch. Below the front panel, adjacent to the fuse, is a set of panel BNCs for the MASTER CLOCK (external source pulse generator--TTL level), TRIG OUT, D'LY TRIGGER and a +5 V supply. The signals and dc biases are connected to the control logic by means of a 36-pin cable.

2. Control Logic

The control logic consists of two wire-assembled printed-circuit boards labeled "PULSE GENERATOR" (B1) and the "MOS CLOCK DRIVERS, CLAMPS and S/H" (B2) as shown in Fig. A-2. B1 supplies the logic waveforms (TTL level) which are then inverted and translated to variable amplitude clock waveforms on board B2.

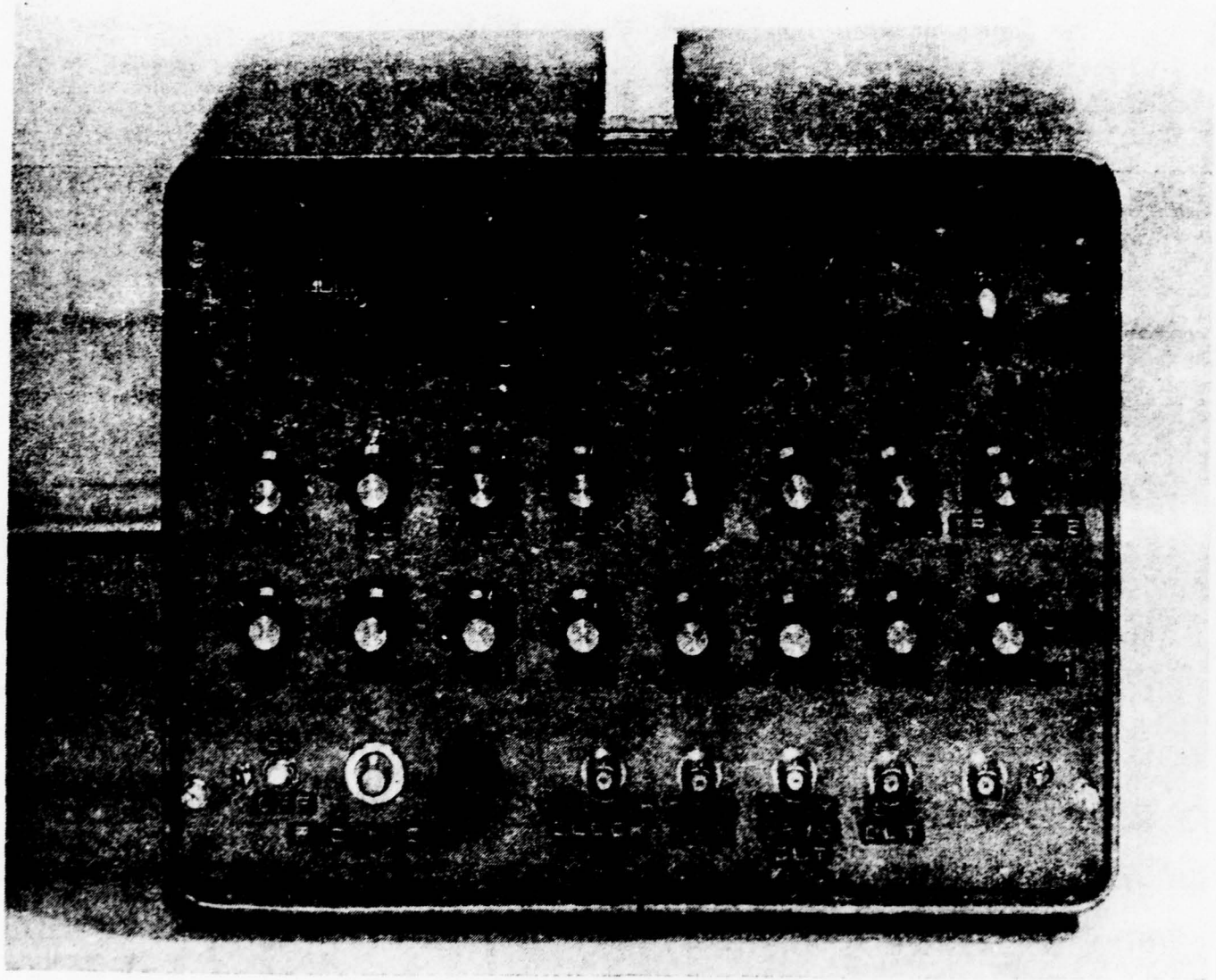


Figure A-1. Photograph of the power supply for the TC1230 tester.

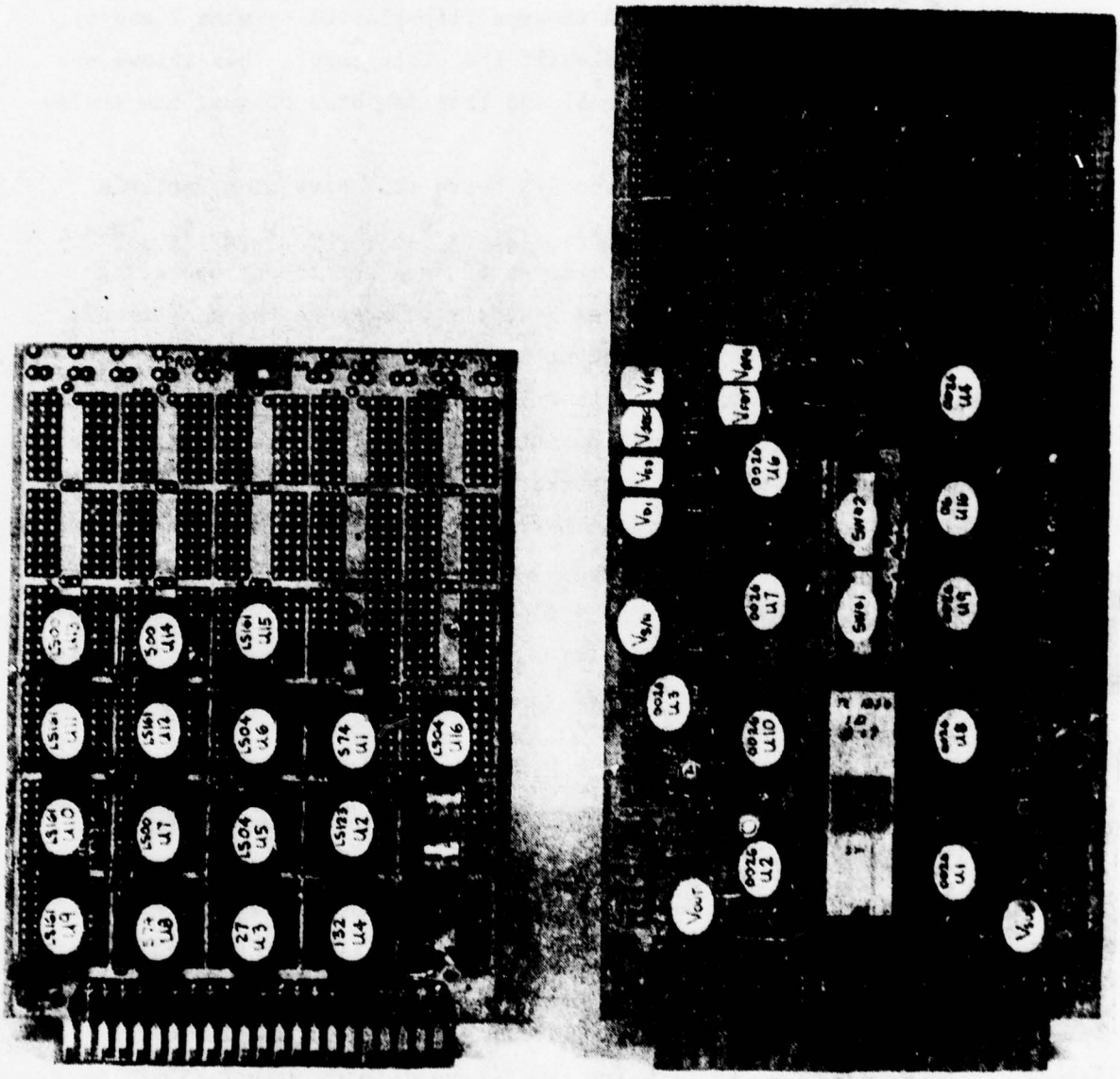


Figure A-2. Photograph of printed-circuit boards B1 (left) and B2 (right).

The pulse generator board has two trimmer pots which are used to adjust the pulse width of $\overline{S_{1A}}$,$\overline{S_{1B}}$ and $\overline{DCS1}$,$\overline{DCS2}$. Two modes of operation for the $\overline{DCS1}$,$\overline{DCS2}$ pulse may be selected using the miniature toggle slide switch. Sliding the switch to position +5 V, will generate $\overline{DCS1}$,$\overline{DCS2}$ pulses at the clock rate and sliding it to point A (D-type flip-flop U1 -- pins 2 and 6), will generate $\overline{DCS1}$,$\overline{DCS2}$ pulses at one-half the clock rate. This allows one to subtract charge from both the signal and trailing bias or just the trailing bias, respectively.

The MOS Clock Drivers, Clamps and S/H board (B2) have nine variable dc bias supplies labeled V_{OUT}, V_{DD}, V_{D1}, $V_{\phi REC}$, $V_{\phi R}$, V_{FDT}, $V_{\phi FG}$, V_{SUB} and $V_{S/H}$. These bias supplies are seldom adjusted once set to the operating level. Test points are provided on each supply to measure the bias level. A miniature toggle slide switch adjacent to the 40-pin test socket is provided to select signals for G_{1B}: either V_{BC} or G_{1A}. Test points for S_{OUT1}', S_{OUT2}' (which are the floating-gate outputs) and NOISE IN are also provided and labeled. Above the 40-pin test socket are two miniature switches (7020 series DIP-type by AMP) designated as SW#1 and SW#2. These switches control the signal-regeneration stages and select either standard two-phase or low-loss clocking. For standard two-phase clocking gates ϕ_{RGS}, ϕ_{RGT}, ϕ_{BCS}, and ϕ_{BCT} are driven by the ϕ_2 clock waveform. For low-loss mode operation gates ϕ_{RGS}, ϕ_{RGT} are driven by ϕ_{RG} and gates ϕ_{BCS}, ϕ_{BCT} are driven by ϕ_{BC} as shown in the timing diagram Fig. 17.

Adjacent to boards B1 and B2 are the "TOTAL DELAY", "LOOP SIZE", and "SOURCE STROBE A" switches which are chassis-mounted as shown in Fig. A-3. The "TOTAL DELAY" switch (labeled from 2^{11} to 2^{20}) selects the number of clock cycles during which the closed-loop CCD is recirculating (i.e., the total period between Loop Cycle 0 and Loop Cycle N). The "LOOP SIZE" toggle switch has two positions, either 256 (256-stage CCD -- TC1230B) or 1024 (1024-stage CCD -- TC1230A). Adjacent to the "LOOP SIZE" switch is a toggle switch labeled "SOURCE STROBE A" (S_{1A}) which has two positions, either "NORM" or "CONT". In normal operation "NORM", S_{1A} is gated with $\overline{GATE\ B}$ and will generate pulses only during the initial loading of the CCD loop during Loop Cycle 0. In continuous operation "CONT", S_{1A} will generate pulses continuously which allows one to add new signals to signals already recirculating in the loop.

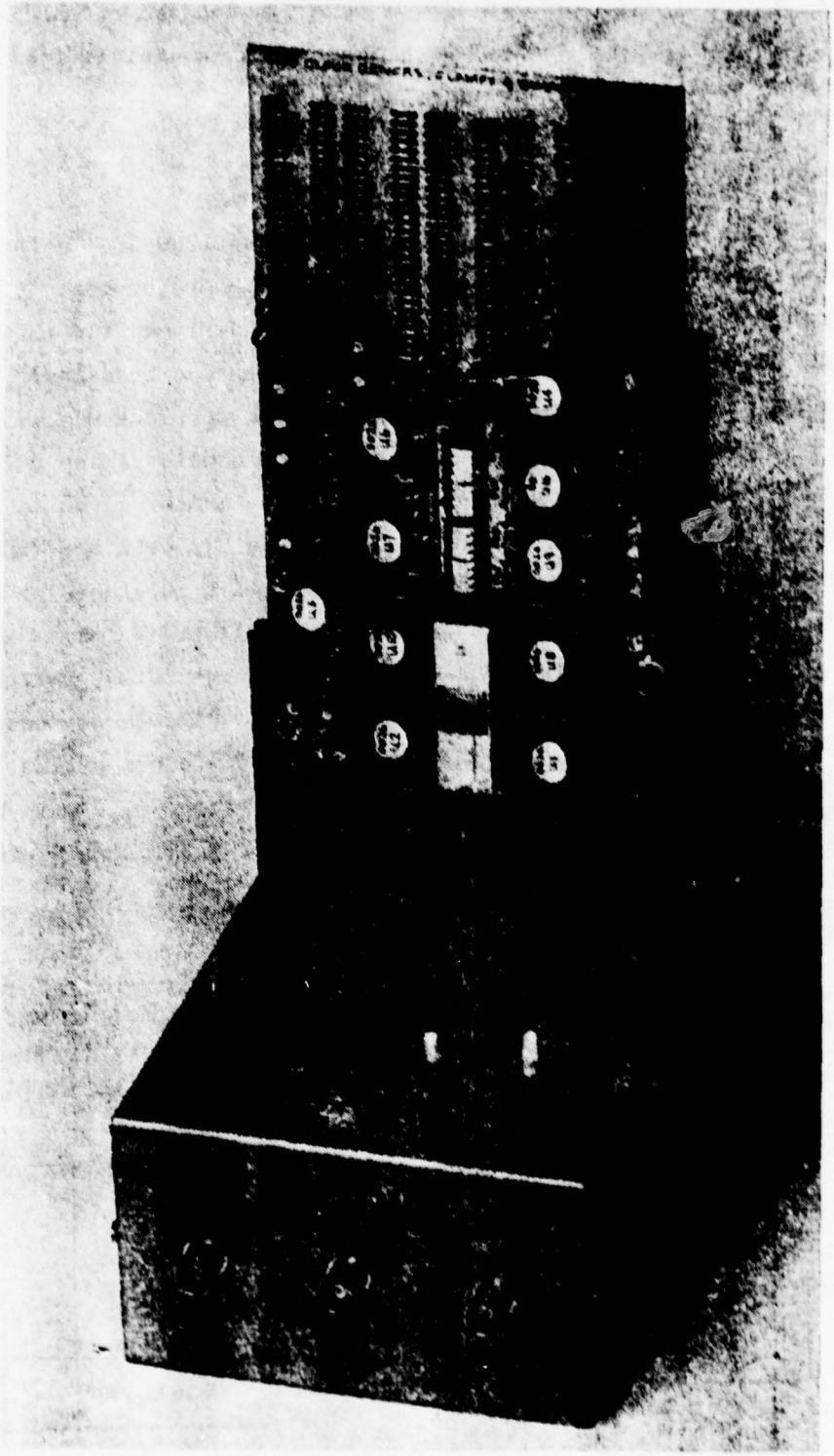


Figure A-3. Photograph of control logic for the TC1230 tester.

A panel BNC connector labeled "INPUT DATA" is located at the left front side of the control logic chassis, where input data is applied from a separate external pulse generator (TTL level).

B. TC1230 CCD TESTER CIRCUIT DESCRIPTION

Block and detailed schematic diagrams for the TC1230 CCD Tester are shown in Figs. A-4 - A-7. Referring to the Pulse Generator board B1 schematic shown in Fig. A-6, all of the timing waveforms are derived from the external master clock input (TTL level). The TTL levels are then translated to variable amplitude clock waveforms using MH0026 clock driver ICs located on board B2 (see Fig A-7). The duty cycle of the master clock should be approximately 50%. The clock ($\overline{CLK}$) which is divided down by 2 from the master clock is applied to the synchronous 20-stage binary counters U9-U12 and U15 (all are 74LS161) which control the timing for the CCD. (NOTE: Only the last 10 stages of the counters are utilized individually to count from 2^{11} to 2^{20} clock cycles). At the beginning of Loop Cycle N the TOTAL DELAY selected by the rotary switch is used to clock the D-type flip-flop U8 (pin 5) high which switches the output of the NAND gate U7 (pin 6) low until a period of 256 or 1024 clock cycles (determined by the LOOP SIZE switch) is completed. During this time, $\overline{\phi_{FDT}}$ will be pulsing which clocks signal charge out ot the CCD loop via the floating diffusion. At

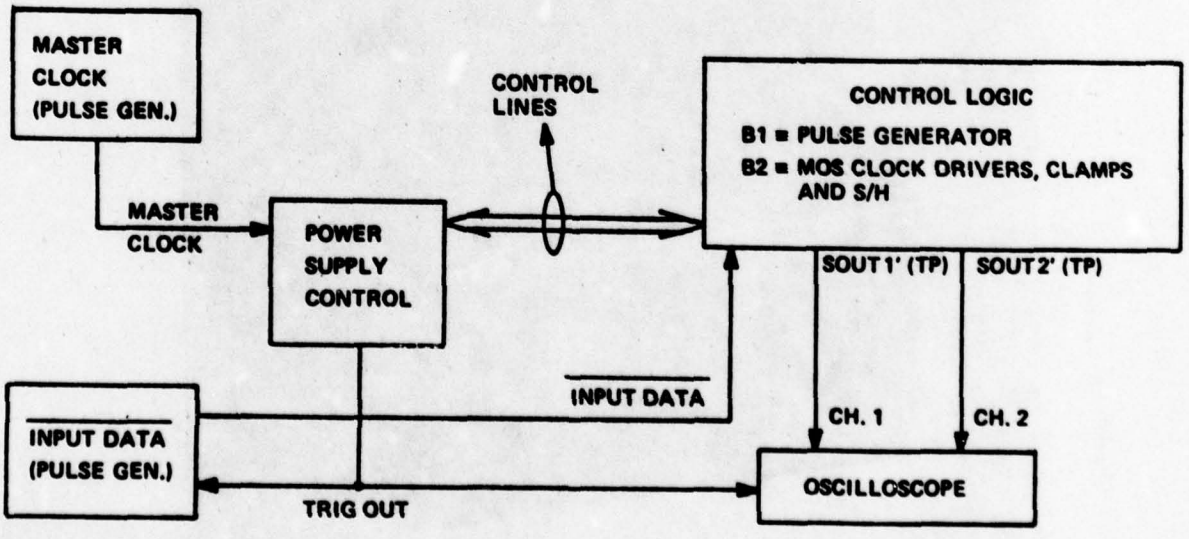


Figure A-4. TC1230 CCD tester block diagram

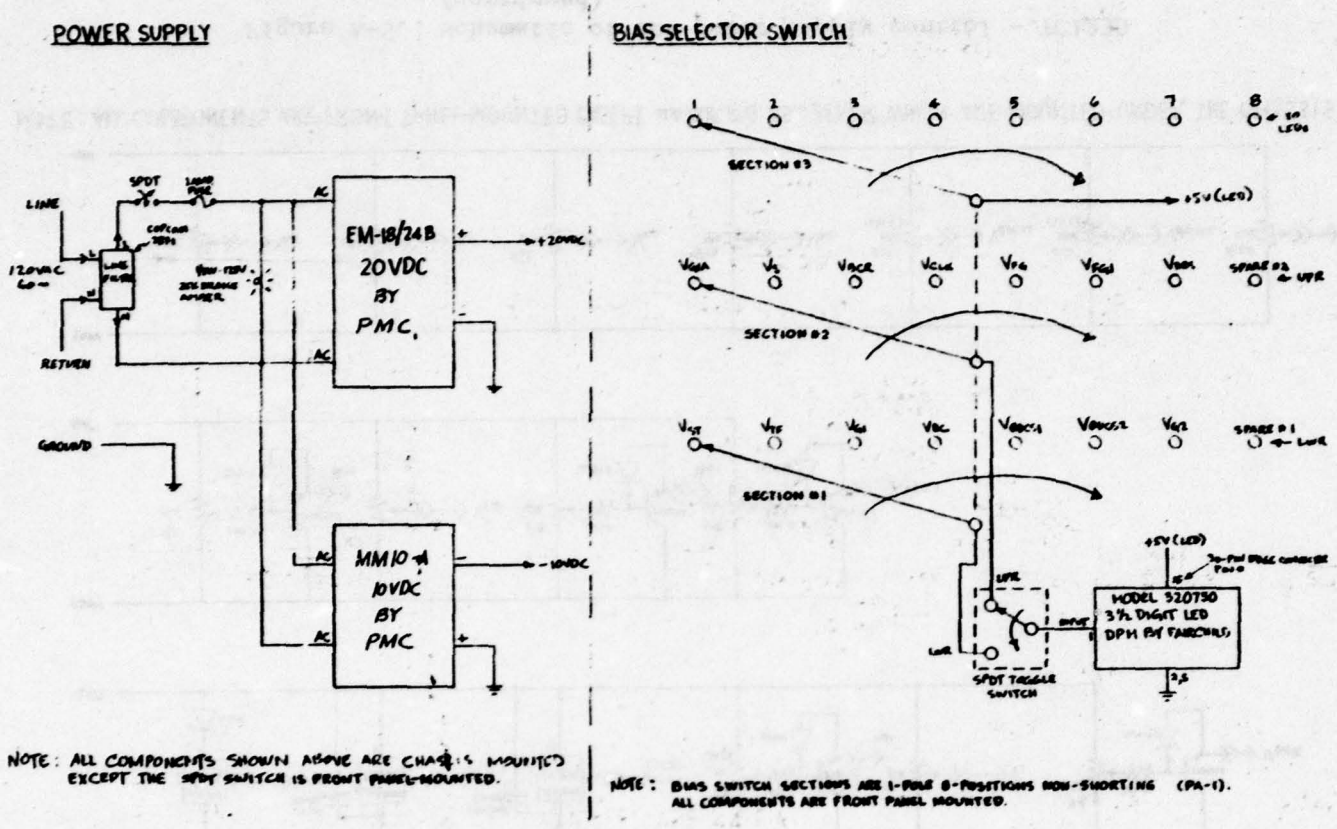
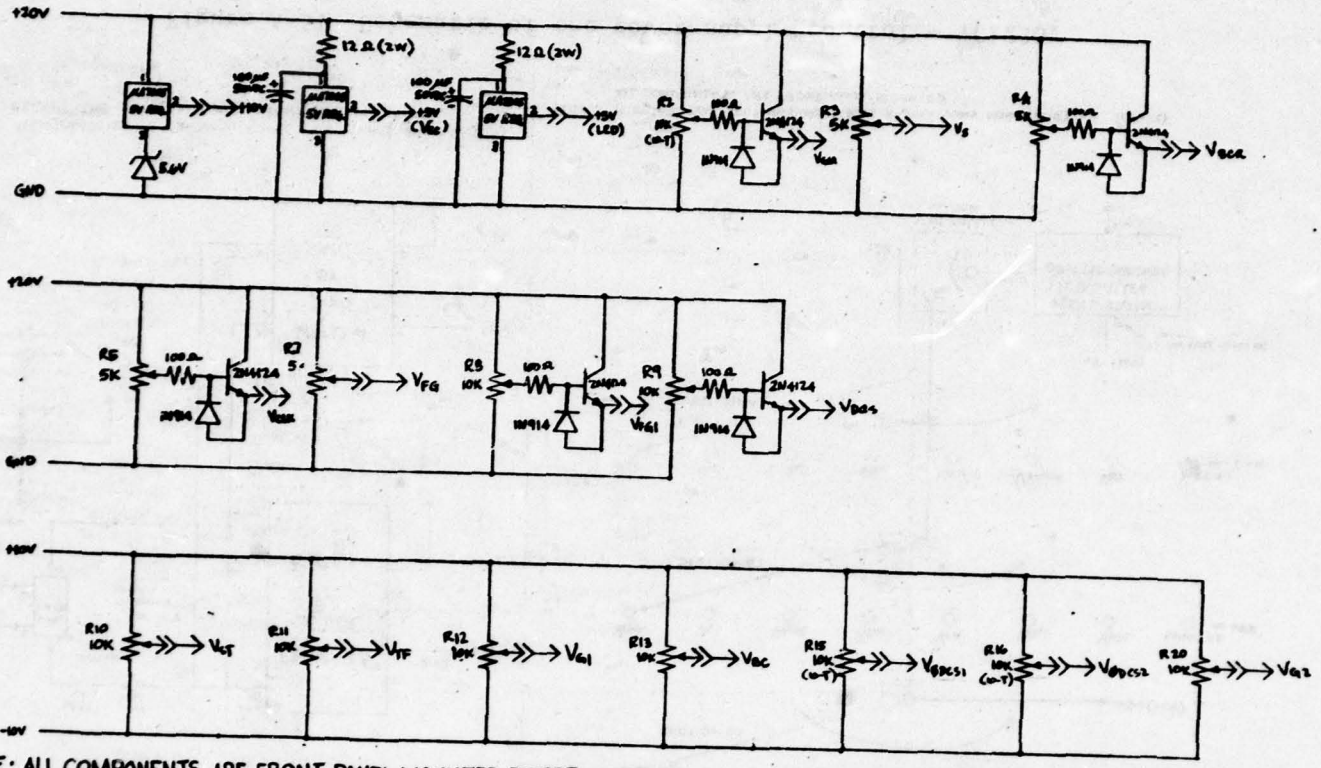
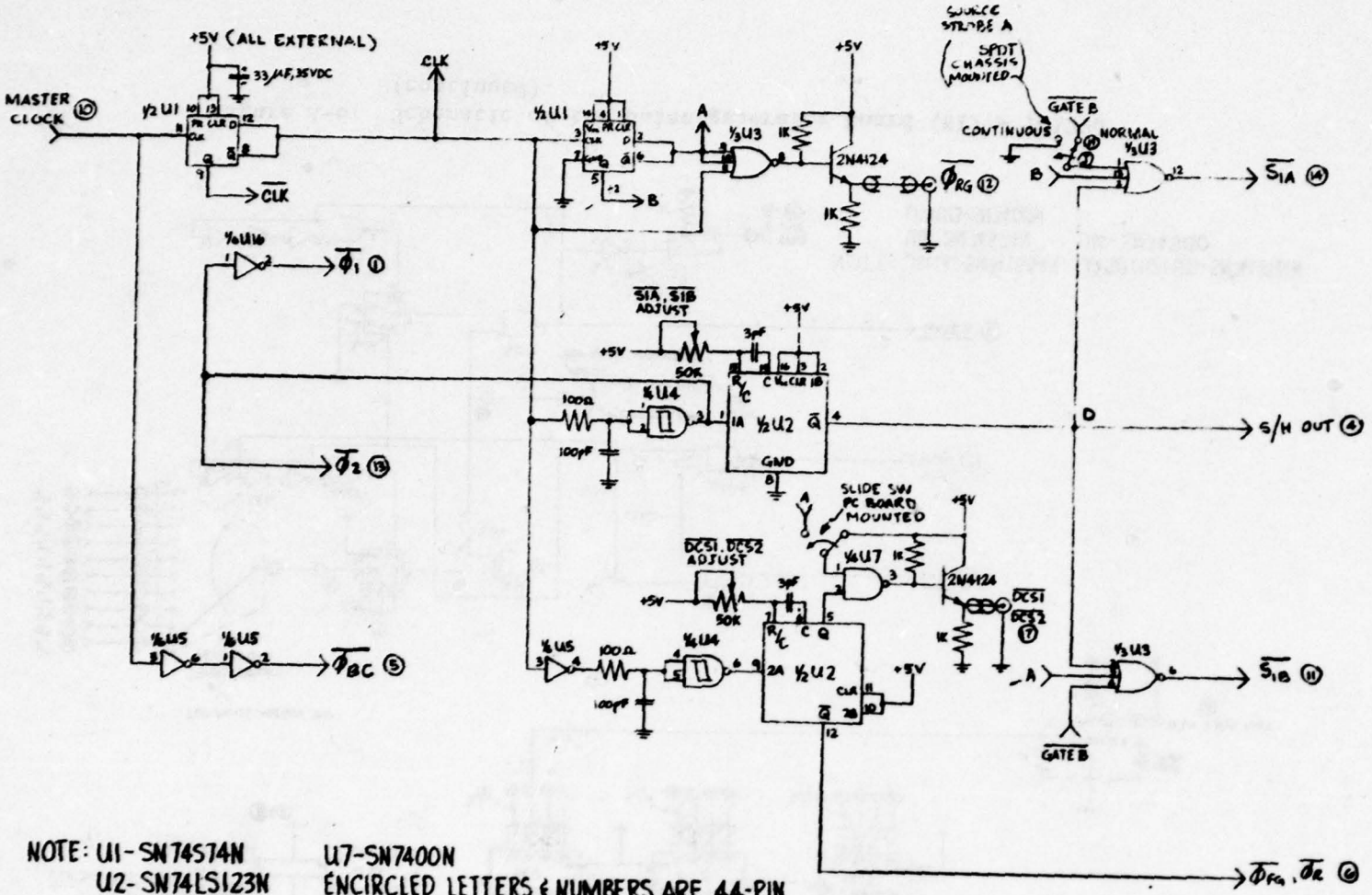


Figure A-5. Schematic of the power supply control - TC1230.



NOTE: ALL COMPONENTS ARE FRONT PANEL-MOUNTED EXCEPT μA7805 REG. & 5.6 ZENER WHICH ARE MOUNTED UNDER THE CHASSIS.

Figure A-5. Schematic of the power supply control - TC1230 (continued).



NOTE: U1 - SN74S74N
U2 - SN74LS123N
U3 - SN7427N
U4 - SN74132N
U5 & U16 - SN74LS04N
U7 - SN7400N
ENCIRCLED LETTERS & NUMBERS ARE 44-PIN EDGE CONNECTOR PIN #.
+5V - (22) (ALL EXTERNAL)
GND - (5) & (7)

Figure A-6. Schematic of the pulse generator board (B1) - TC1230.

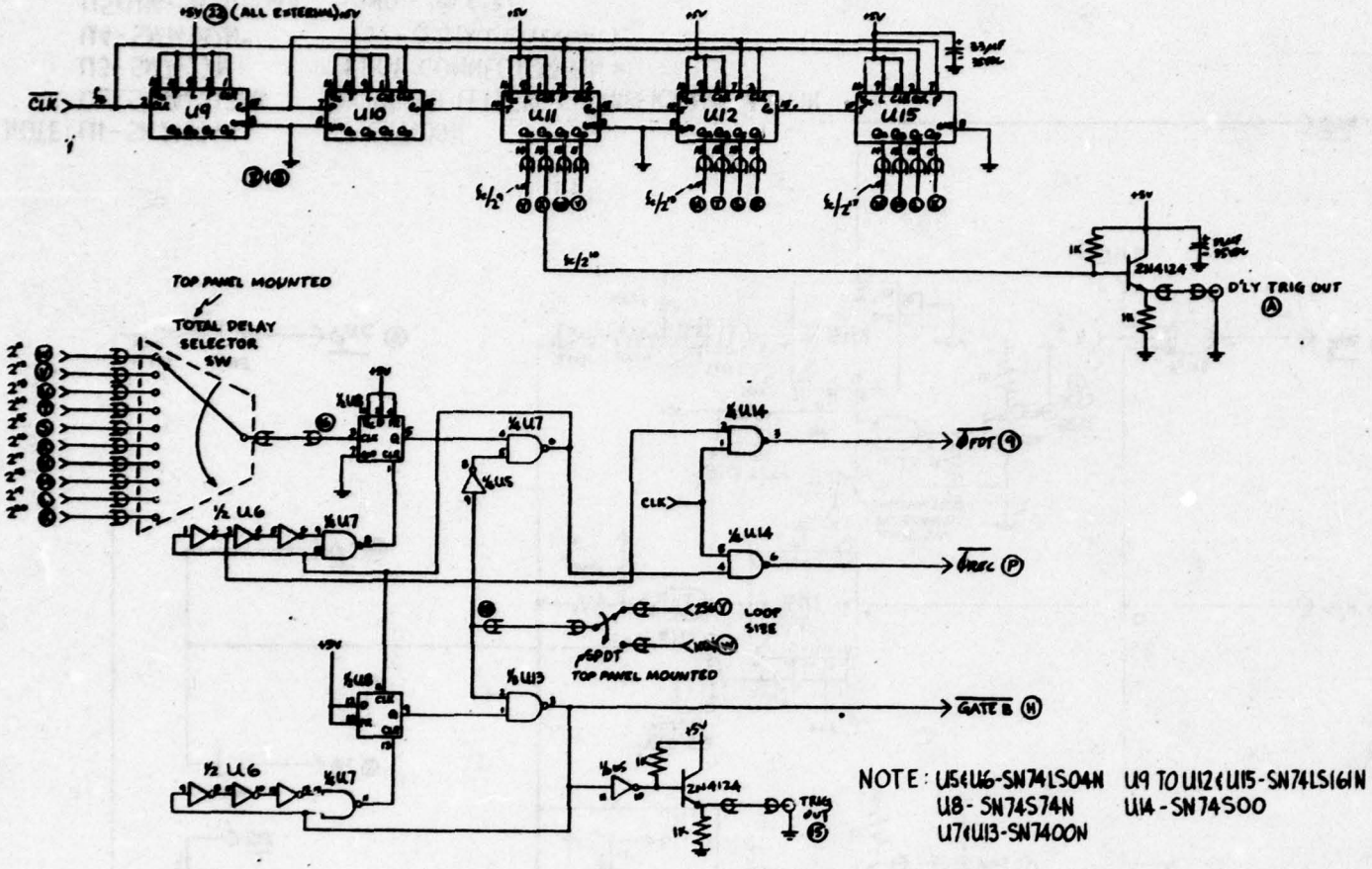
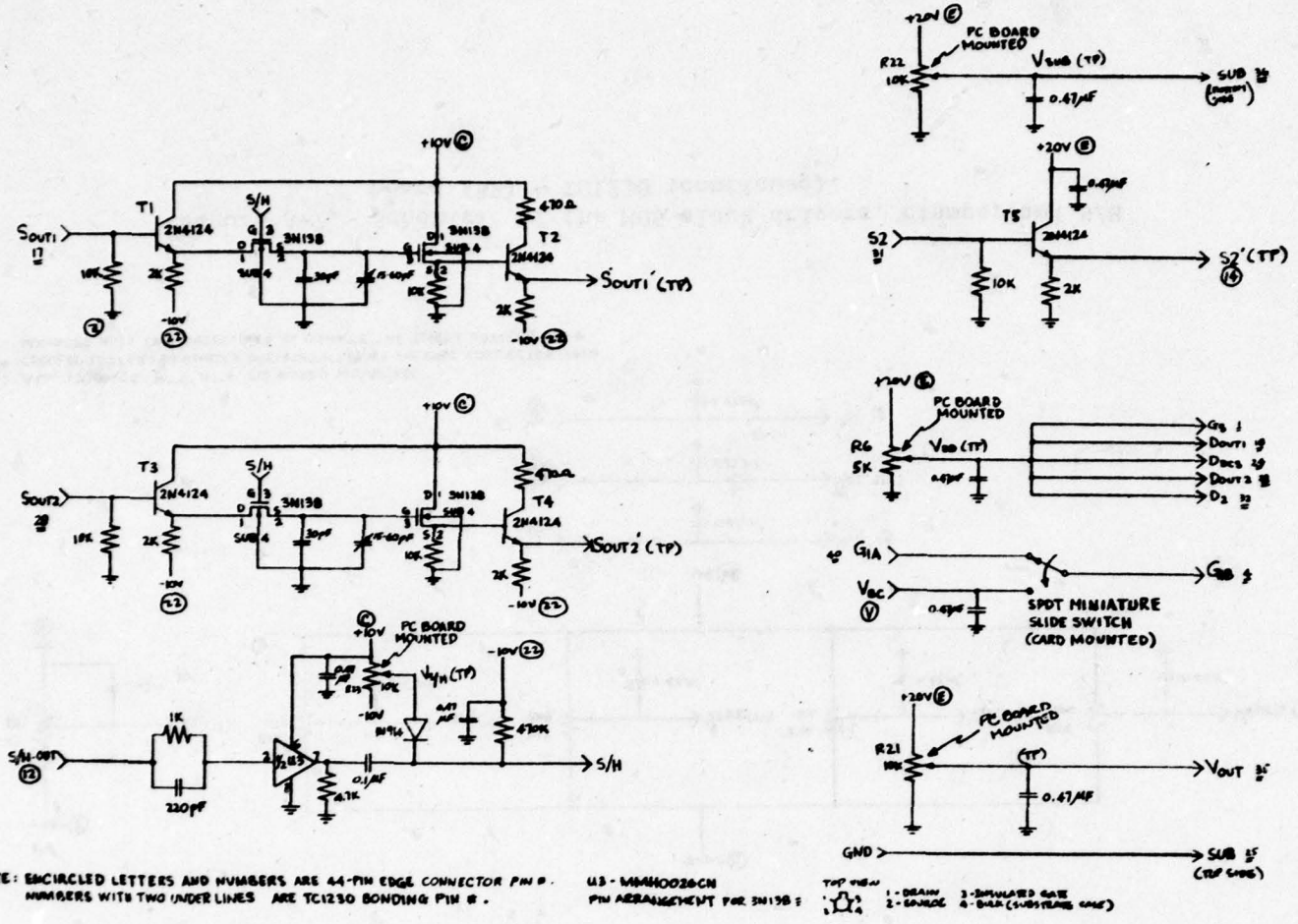


Figure A-6. Schematic of the pulse generator board (B1) - TC1230 (continued).



NOTE: ENCIRCLED LETTERS AND NUMBERS ARE 44-PIN EDGE CONNECTOR PIN #. NUMBERS WITH TWO UNDER LINES ARE TC1230 BONDING PIN #.

U3 - MMH0026CN
PIN ARRANGEMENT FOR 3N138:

TOP VIEW
1 - DRAIN 3 - SUPPLIED GATE
2 - SOURCE 4 - BULK (SUBSTRATE CASE)

Figure A-7. Schematic of the MOS clock drivers, clamps, and S/H. board (B2) - TC1230.

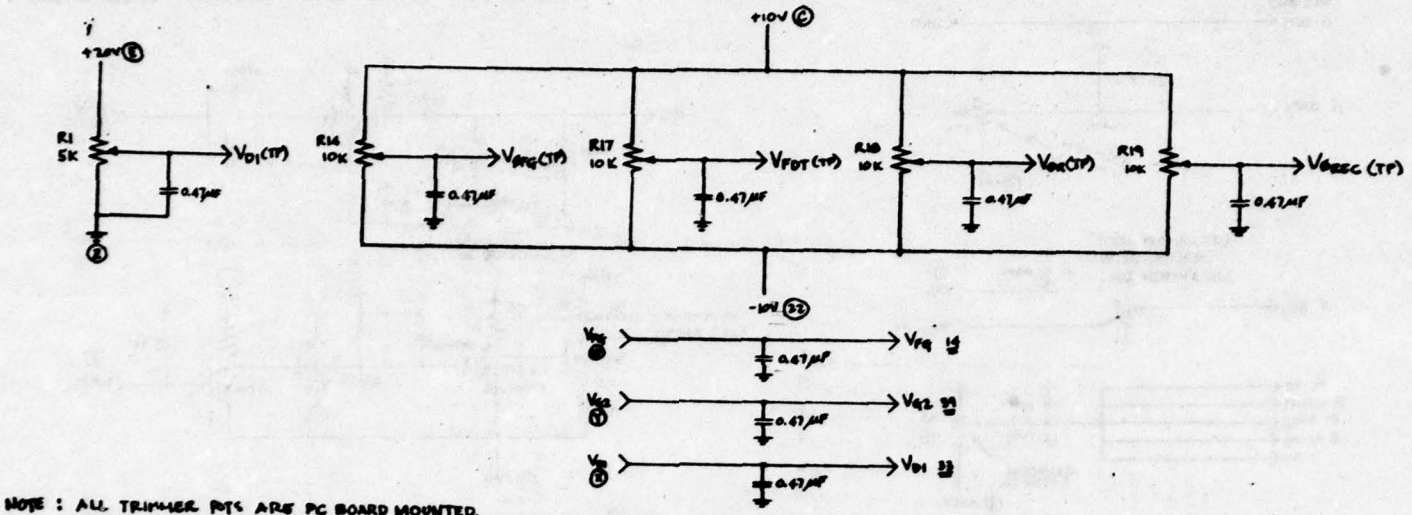


Figure A-7. Schematic of the MOS clock drivers, clamps, and S/H board (B2) - TC1230 (continued).

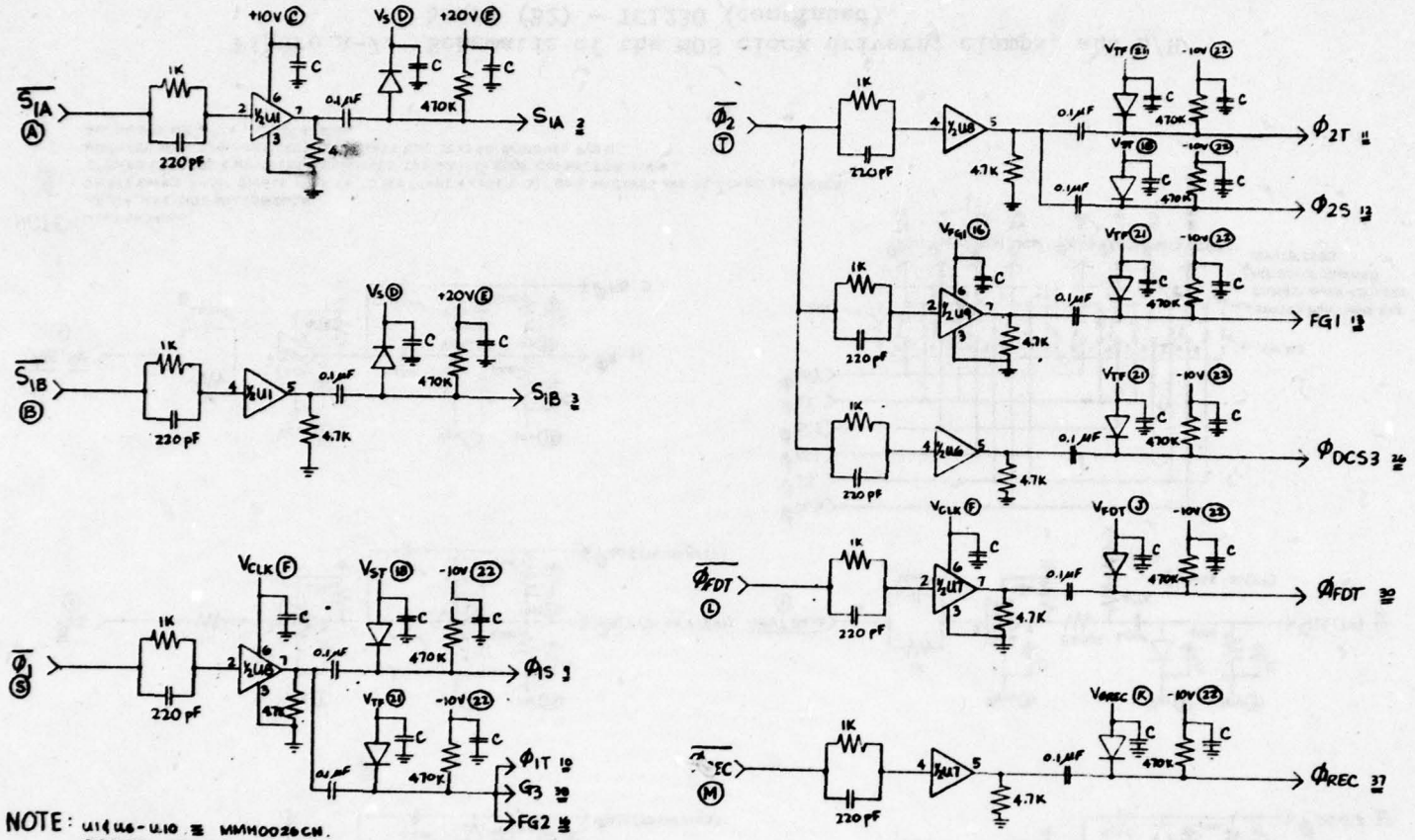


Figure A-7. Schematic of the MOS clock drivers, clamps, and S/H Board (B2) - TC1230 (continued).

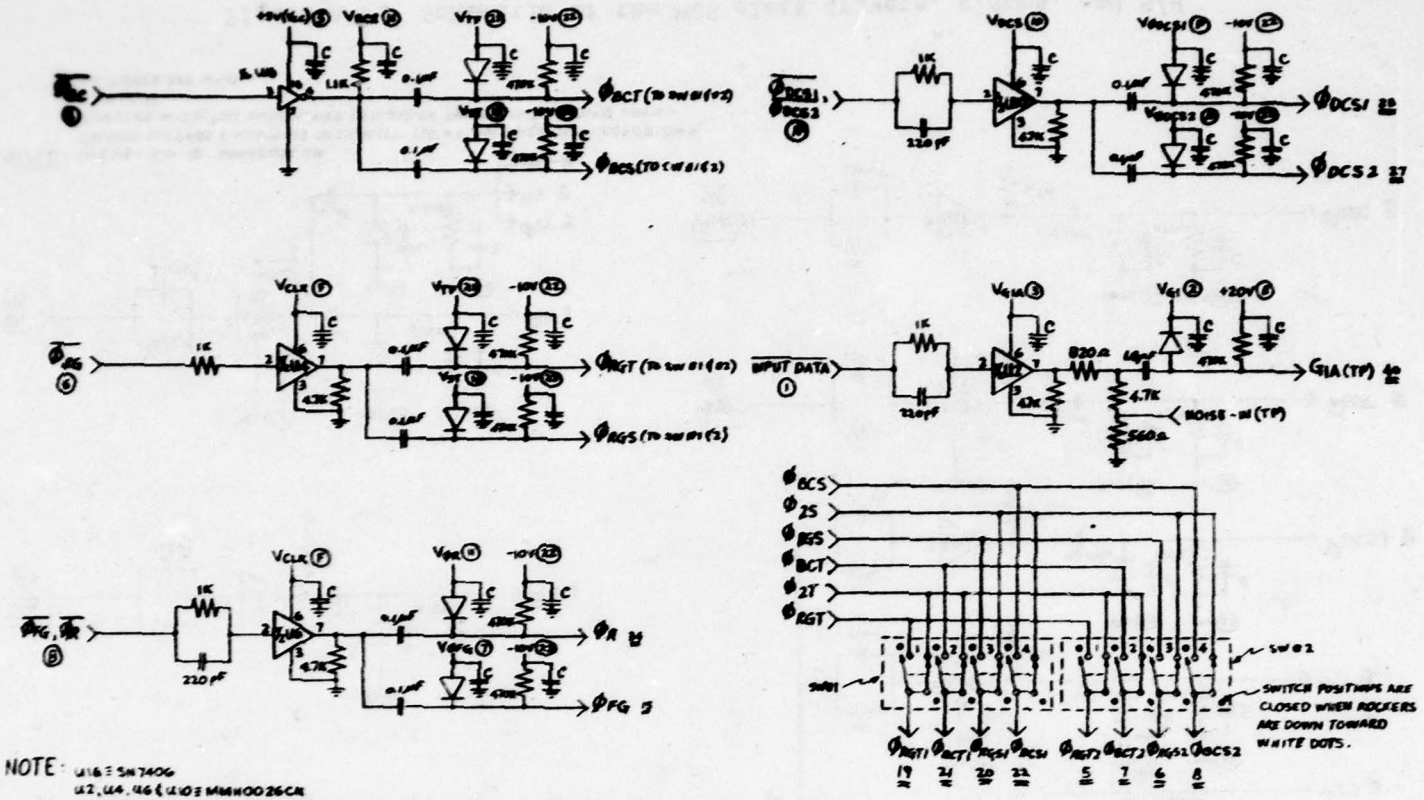


Figure A-7. Schematic of the MOS clock drivers, clamps, and S/H board (B2) - TC1230 (continued).

the end of Loop Cycle N, the output of NAND gate U7 (pin 8) will go low and reset the D-type flip-flop U8 (pin 1). Approximately 40 ns later, U8 (pin 11) is clocked and the output Q of U8 (pin 9) remains high, which forces $\overline{\text{GATE B}}$ low until the loop size period has elapsed. The rising edge of $\overline{\text{GATE B}}$ is then sensed by the NAND gate U7 (pin 12) and inverter U6 (pin 9), at which time the D-type flip-flop U8 (pin 13) will reset for approximately 30 ns. The reset pulse width applied to U8 is determined by the three cascaded inverters U6. Also, $\overline{\text{GATE B}}$ is inverted and buffered to provide the main trigger output starting at the beginning of Loop Cycle 0. $\overline{\phi_{REC}}$ is generated to recirculate signals in the loop when the output of NAND gate U7 (pin 6) is high, which is the case except during Loop Cycle N. $\overline{\phi_1}$ and its complement $\overline{\phi_2}$ are generated from the CLK pulse and are both delayed relative to $\overline{\phi_{BC}}$ (which is generated from the master clock) in order to prevent edge race conditions in the CCD regeneration stage. $\overline{\phi_{RG}}$ is generated by gating the CLK pulse with the output of D-type flip-flop U1 (pin 6), which has twice the CLK period. S/H_{OUT}, $\overline{DCS1}$,$\overline{DCS2}$, $\overline{\phi_{FG}}$,$\overline{\phi_R}$ and $\overline{S_{1A}}$,$\overline{S_{1B}}$ are all derived from the dual one-shot U2 -- 74LS123 which provides adjustable pulse width for these signals. $\overline{DCS1}$,$\overline{DCS2}$ can be generated either at one-half of the clock rate or at the clock rate f_c, depending on whether the input for NAND gate U7 (pin 1) is connected to A or +5 V, respectively.

The schematic for printed-circuit board B2 is shown in Fig. A-7. This board contains MOS clock drivers (MMH0026) and output clamps to obtain the required pulse amplitude and dc bias for the various waveforms which drive the TC1230 CCD. Sample and hold circuits for the floating gate output S_{OUT1} and S_{OUT2}, which use 3N138 MOSFET sampling transistors and source followers, are included on the board to reduce clock noise at these outputs.

Table A-1 lists the function of all the adjustable bias voltages supplied by the CCD tester. The adjustment range for each control, as well as nominal values for operating the TC1230 CCD in the low-loss mode are also listed.

The wiring connections between the power supply cable and the two printed-circuit boards are shown in Table A-2.

TABLE A-1. BIAS ADJUSTMENTS

Control		Function	Nominal Value (Volts)	Bias Range (Volts)
R1.	V_{D1}*	FD[a] Output Drain	+15	0 to +20
R2.	V_{G1A}	Input Data Amplitude	+ 2.3	0 to +20
R3.	V_S	Source Strobe Bias (S_{1A},S_{1B})	+16	+10
R4.	V_{BCR}	Bias Charge Pulse Amplitude (ϕ_{BC})	+12.6	0 to +20
R5.	V_{CLK}	Main Clock Amplitude (ϕ_1, ϕ_2, ϕ_R, ϕ_{RG}, ϕ_{FDT}, ϕ_{REC}, G_3, FG2)	+10.0	
R6.	V_{DD}*	Output Transistor Drain	+15	
R7.	V_{FG}	FG[b] Reset Source Bias	+ 3.0	
R8.	V_{FG1}	FG1 Transfer Gate Amplitude	+ 6.5	
R9.	V_{DCS}	DCS[c] Pulse Amplitude	+18.5	
R10.	V_{ST}	Storage Gate Bias (S)	0.0	-10 to +10
R11.	V_{TF}	Transfer Gate Bias (T)	- 4.2	
R12.	V_{G1}	Input Data Bias (G_{1A})	+ 3.0	
R13.	V_{BC}	Trailing Bias Level (G_{1B})	+ 1.5	
R14.	$V_{\phi FG}$	FG Reset Gate Bias	- 2.0	
R15.	$V_{\phi DCS1}$	DCS1 Gate Bias	- 2.3	
R16.	$V_{\phi DCS2}$	DCS2 Gate Bias	- 3.4	
R17.	V_{FDT}*	FD Transfer Gate Bias	- 3.0	
R18.	$V_{\phi R}$*	FD Reset Gate Bias	+ 5.0	
R19.	$V_{\phi REC}$*	Recirculate Gate Bias	- 3.0	
R20.	V_{G2}	Input Storage Well Bias	+ 3.2	
R21.	V_{OUT}	FD Output dc Gate Level	+20	0 to +20
R22.	V_{SUB}*	Base Substrate	+ 5	0 to +20
R23.	$V_{S/H}$*	Sample and Hold dc Bias	- 6.2	-10 to +10

NOTES: *Designates Trim-Pot mounted on board B2.

[a]FD: Floating Diffusion

[b]FG: Floating Gate

[c]DCS: Dark-Current Subtractor

TABLE A-2. CONNECTOR PIN ASSIGNMENT LIST

Function	36-Pin Cable Connector Pin #	PC Board B1 44-Pin Edge Connector Pin #	PC Board B2 44-Pin Edge Connector Pin #
+20V	1		E
+10V	2		C
+5 V (TTL)	3	22	5
-10 V	4		22
V_{G1A}	5		3
V_S	6		D
V_{BCR}	7		H
V_{CLK}	8		F
V_{FG}	9		W
V_{FG1}	10		16
V_{DCS}	35		10
V_{ST}	11		18
V_{TF}	12		21
V_{G1}	13		2
V_{BC}	14		V
$V_{\phi DCS1}$	15		P
$V_{\phi DCS2}$	16		R
V_{G2}	17		Y
GND	19	B & Z	Z
$V_{\phi FG}$			TP
V_{FDT}			TP
V_{ϕ}			TP
$V_{\phi REC}$			TP
V_{SH}			TP
V_{SUB}			TP
V_{D1}			TP
V_{DD}			TP
V_{OUT}			TP
S_{OUT1}'			TP
D_{OUT2}'			TP

TABLE A-2. CONNECTOR PIN ASSIGNMENT LIST (continued)

Function	36-Pin Cable Connector Pin #	PC Board B1 44-Pin Edge Connector Pin #	PC Board B2 44-Pin Edge Connector Pin #
S_2'			14
$\overline{S_{1A}}$		14□	A
$\overline{S_{1B}}$		11	B
$\overline{\phi_1}$		1	S
$\overline{\phi_2}$		13	T
$\overline{\phi_{BC}}$		5	4
$\overline{\phi_{RG}}$		12	6
$\overline{\phi_{FG}}$, $\overline{\phi_R}$		6	8
CH.#16($\overline{\phi_2}$)		13	9
$\overline{\phi_{FDT}}$		9	L
$\overline{\phi_{REC}}$		P	M
$\overline{\phi_{DCS1}}$, $\overline{\phi_{DCS2}}$		17	N
$\overline{\text{INPUT DATA}}$ (EXT.)*			1
S/H OUT		4	12
MASTER CLOCK (EXT.)*	21	10	
D'LY TRIG OUT*	25	A	
2^8*		Y	
2^{10}*		W	

NOTE: □ Normal or continuous selection (SPDT SW-Chassis Mounted) -- refer to final schematic for PIN OUT.

* 50 Ω coaxial cable connector.

TABLE A-2. CONNECTOR PIN ASSIGNMENT LIST (continued)

Function	36-Pin Cable Connector Pin #	PC Board B1 44-Pin Edge Connector Pin #	PC Board B2 44-Pin Edge Connector Pin #
2^{11}*		V	
2^{12}*		U	
2^{13}*		T	
2^{14}*		S	
2^{15}*		R	
2^{16}*		N	
2^{17}*		M	
2^{18}*		L	
2^{19}*		K	
TRIG OUT*	23	15	
TOTAL DELAY SELECTOR POLE TERMINAL*		16	
LOOP SIZE CENTER POLE* (SPDT SW)		18	
BIAS SPARE #1	36		19
BIAS SPARE #2	18		20

Note: *50 Ω coaxial cable connector.

APPENDIX B

ANALYSIS OF THE EFFECTIVE TRANSFER LOSS IN A LOW-LOSS BCCD DUE TO BULK-TRAPPING STATES

In this analysis we assume that the low-loss BCCD is operated with a trailing bias charge Q_{TB} which is larger than the signal charge Q_S in order to obtain minimum effective transfer losses. We also assume that the clock frequency f_c is below the point where free charge transfer is a limiting factor so that transfer losses are dominated by the interaction of Q_S and Q_{TB} with the bulk traps in the buried-channel region. Part A provides a brief review of the Schottky-Read-Hall rate equation describing bulk-trapping states. In Part B we derive equations for the first-order transfer loss of ΔQ_S and ΔQ_{TB} and show that although charge is redistributed between Q_S and Q_{TB} due to bulk-trapping, to first order there is no net transfer loss for the sum-charge packet $Q_{SUM} = Q_S + Q_{TB}$. The analysis of the effective transfer loss for Q_{SUM} due to second-order transfer losses is presented in Part C. In Part D we consider the effect of the interaction of multiple bulk traps having different energy levels. An expression for the second-order transfer loss with closed-loop operation is derived in Part E. In Part F the charge-transfer losses due to the signal-regeneration stage are discussed, and a sample calculation based on measured data is shown in Part G. The following analysis is based on the bulk trapping model for buried-channel CCDs described by Mohsen and Tompsett [6].

Glossary of Symbols

E	energy level of bulk trap below conduction band
k	Boltzmann's constant
N_c	effective density of states in the conduction band [cm^{-3}]
n_e	density of mobile electrons [C/cm^3]
N_t	density of bulk-trapping states [cm^{-3}]
n_t	charge density of filled traps [C/cm^3]
q_t	total trapped charge [C]
Q_S	signal charge level [C]
Q_{TB}	trailing bias charge level [C]
Q_{SO}	signal charge 'zero' level [C]
Q_{S1}	signal charge 'one' level [C]
Q_{TBO}	trailing bias charge level following Q_{SO} [C]
Q_{TB1}	trailing bias charge level following Q_{S1} [C]
Q_{SUM}	sum charge packet $Q_S + Q_{TB}$
T_S	storage time [s]
T_T	transfer time [s]
T_c	clock period [s]
t'	free-charge transfer time [s]
τ_e	bulk state emission time constant [s]
τ_t	bulk state trapping time constant [s]
V_S	volume occupied by signal charge Q_S [cm^3]
V_{TB}	volume occupied by trailing bias charge Q_{TB} [cm^3]
v_{th}	average thermal velocity of electrons [cm/s]
σ	bulk-trap capture cross section [cm^2]

A. BULK-TRAP OCCUPANCY

The interaction of minority carriers in the BCCD charge packet with bulk traps is described by the Schottky-Read-Hall rate equation:

$$\frac{dn_t}{dt} = \frac{(N_t - n_t)}{\tau_t} - \frac{n_t}{\tau_e} \quad . \tag{B-1}$$

where the trapping time constant τ_t is:

$$\tau_t = 1/\sigma \, v_{th} \, n_e \tag{B-2}$$

and the emission time constant τ_e is:

$$\tau_e = 1/\sigma \, v_{th} \, N_c \, e^{\frac{E}{kT}} \tag{B-3}$$

The equilibrium charge density of filled traps may be determined from Eq. (B-1) by setting $\frac{dn_t}{dt} = 0$. Solving for n_t we obtain:

$$n_t = \frac{eN_t}{1 + \frac{\tau_t}{\tau_e}} \tag{B-4}$$

The total trapped charge q_t in a volume V_S is given by:

$$q_t = \int_{V_S} n_t \, dV \quad . \tag{B-5}$$

For most traps of importance, $\tau_t << \tau_e$, and if we assume n_t is essentially constant over the volume V_S, Eq. (B-5) reduces to:

$$q_t = n_t \, V_S \approx e \, N_t \, V_S \quad . \tag{B-6}$$

B. FIRST-ORDER CHARGE TRANSFER LOSS ANALYSIS

In general, the change ΔQ_S in a signal charge Q_S due to interaction with bulk traps during a single transfer can be determined by comparing the initial state of the traps q_t (initial) in the CCD well before the signal charge enters

with the final state of the traps q_t (final) after the signal charge has transferred out of the region of the CCD. Since charge must be conserved, we have:

$$Q_S \text{ (initial)} + q_t \text{ (initial)} = Q_S \text{ (final)} + q_t \text{ (final)} \qquad \text{(B-7)}$$

or

$$\Delta Q_S = -\Delta q_t = q_t \text{ (initial)} - q_t \text{ (final)} . \qquad \text{(B-8)}$$

During the storage time T_S while the signal Q_S (which occupies volume V_S) is present in the CCD well, the bulk traps contained in that volume are filled to a level of $q_t = n_t V_S$. During the initial short transfer time t' (when most of the charge transfers out of the well) the traps remain filled. However, during the remaining transfer time $T_T' = T_T - t'$ the BCCD is essentially empty and the trapped charges which are emitted with a time constant τ_e can join the signal charge. At the end of the transfer time, the trapping states contain the net trapped charge:

$$q_t = n_t V_S e^{\frac{-T_T'}{\tau_e}} . \qquad \text{(B-9)}$$

We now consider the case of a low-loss CCD with an input data pattern containing a single 'one' signal charge Q_{S1} which is preceded by a string of 'zero' signal charges Q_{S0}. A trailing bias charge Q_{TB0} follows each signal charge Q_{S0}, and a trailing bias charge Q_{TB1} follows the signal charge Q_{S1}. (This analysis also applies to the leading 'one' signal charge of a string of 'ones'). We will now calculate the first-order transfer losses ΔQ_{S0} and ΔQ_{TB0} per transfer and show that their sum $\Delta Q_{SUM} = \Delta Q_{S0} + \Delta Q_{TB0}$ is identically equal to zero. (In Part C we calculate the first-order losses ΔQ_{S1} and ΔQ_{TB1} in which case the sum $\Delta Q_{SUM} = \Delta Q_{S1} + \Delta Q_{TB1}$ is not equal to zero and exhibits a net second-order transfer loss).

Calculation of ΔQ_{S0}:

$$\Delta Q_{S0} = q_t^{S0} \text{ (initial)} - q_t^{S0} \text{ (final)} ; \qquad \text{(B-10)}$$

$$q_t^{S0} \text{ (initial)} = n_t V_{TB0} e^{\frac{-T_T'}{\tau_e}} ; \qquad \text{(B-11)}$$

$$q_t^{SO}\ (\text{final}) = n_t\, V_{SO}\, e^{\frac{-T_T'}{\tau_e}} + n_t\, (V_{TBO}-V_{SO})\, e^{\frac{-T_T'}{\tau_e}}\, e^{\frac{-(T_S+T_T)}{\tau_e}} \qquad \text{(B-12)}$$

Note that Eq. (B-12) contains two terms. The first term is due to traps located in the center volume V_{SO} which remain filled during the storage time T_S and emit trapped charge only during the final transfer time $T_T' = T_T - t'$. The second term is due to the edge volume $V_{TBO}-V_{SO}$ which has an initial trap occupancy of $n_t(V_{TBO}-V_{SO})\, e^{\frac{-T_T'}{\tau_e}}$ and emits trapped charge during the entire period T_S+T_T. Substituting Eq. (B-11) and (B-12) into Eq. (B-10) we have:

$$\Delta Q_{SO} = n_t\, (V_{TBO}-V_{SO})\, e^{\frac{-T_T'}{\tau_e}} \left(1 - e^{\frac{-(T_T+T_S)}{\tau_e}}\right) \qquad \text{(B-13)}$$

In a similar fashion we calculate ΔQ_{TBO} as:

$$\Delta Q_{TBO} = q_t^{TBO}\ (\text{initial}) - q_t^{TBO}\ (\text{final}) \qquad \text{(B-14)}$$

where

$$q_t^{TBO}\ (\text{initial}) = q_t^{SO}\ (\text{final})\ (\text{See Eq. B-12}) \qquad \text{(B-15)}$$

and

$$q_t^{TBO}\ (\text{final}) = n_t\, V_{TBO}\, e^{\frac{-T_T'}{\tau_e}}\ . \qquad \text{(B-16)}$$

Thus

$$\Delta Q_{TBO} = -\, n_t\, (V_{TBO}-V_{SO})\, e^{\frac{-T_T'}{\tau_e}} \left(1 - e^{\frac{-(T_T+T_S)}{\tau_e}}\right) \qquad \text{(B-17)}$$

Comparing Eq. B-17 and Eq. B-13, we see that there is no net change in the sum charge packet Q_{SUM} during the transfer:

$$\Delta Q_{SUM} = \Delta Q_{SO} + \Delta Q_{TBO} = 0 \; . \tag{B-18}$$

Therefore, during the transfer operation in a low-loss CCD the signal charge increases by a small amount ΔQ_{SO} due to charge trapped from the preceding trailing bias charge near the edges which is re-emitted into the signal charge. The trailing bias charge Q_{TBO} which follows the signal charge decreases by exactly the same amount $(-\Delta Q_{SO})$ because it refills the edge traps that emitted charge into Q_{SO}.

C. SECOND-ORDER CHARGE-TRANSFER LOSS ANALYSIS

In this section we calculate the first-order losses ΔQ_{S1} and ΔQ_{TB1} which leads to a result that the sum-charge packet in this case $Q_{SUM} = Q_{S1} + Q_{TB1}$ does see a net second-order loss.

$$\Delta Q_{S1} = q_t^{S1}\,(\text{initial}) - q_t^{S1}\,(\text{final}) \; ; \tag{B-19}$$

$$q_t^{S1}(\text{initial}) = n_t \, V_{TBO} \, e^{\frac{-T_T'}{\tau_e}} \; ; \tag{B-20}$$

$$q_t^{S1}(\text{final}) = n_t V_{S1} \, e^{\frac{-T_T'}{\tau_e}} + n_t (V_{TBO} - V_{S1}) \, e^{\frac{-T_T'}{\tau_e}} \, e^{\frac{-(T_S+T_T)}{\tau_e}} \; ; \tag{B-21}$$

$$\Delta Q_{S1} = n_t (V_{TBO} - V_{S1}) \, e^{\frac{-T_T'}{\tau_e}} \left(1 - e^{\frac{-(T_T+T_S)}{\tau_e}} \right) \tag{B-22}$$

ΔQ_{TB1} is calculated following an analysis similar to the calculation for ΔQ_{TBO} as follows:

$$\Delta Q_{TB1} = q_t^{TB1}\,(\text{initial}) - q_t^{TB1}\,(\text{final}) \; ; \tag{B-23}$$

$$q_t^{TB1}(\text{initial}) = n_t V_{S1}\, e^{\frac{-T_T'}{\tau_e}} + n_t (V_{TB0}-V_{S1})\, e^{\frac{-T_T'}{\tau_e}}\, e^{\frac{-(T_S+T_T)}{\tau_e}}; \quad \text{(B-24)}$$

$$q_t^{TB1}(\text{final}) = n_t V_{TB1}\, e^{\frac{-T_T'}{\tau_e}}; \quad \text{(B-25)}$$

$$\Delta Q_{TB1} = n_t (V_{S1}-V_{TB1})\, e^{\frac{-T_T'}{\tau_e}} + n_t (V_{TB0}-V_{S1})\, e^{\frac{-T_T'}{\tau_e}}\, e^{\frac{-(T_S+T_T)}{\tau_e}}. \quad \text{(B-26)}$$

The change in the sum charge packet Q_{SUM} in this case is found by adding Eqs. (B-22) and (B-26):

$$\Delta Q_{SUM} = \Delta Q_{S1} + \Delta Q_{TB1} = n_t\, e^{\frac{-T_T'}{\tau_e}} (V_{TB0}-V_{TB1}). \quad \text{(B-27)}$$

The expression for ΔQ_{SUM} in Eq. (B-27) may also be derived in a simpler manner by noting that

$$\Delta Q_{SUM} = \left[q_t^{S1}\ (\text{initial}) - q_t^{S1}\ (\text{final})\right] + \left[q_t^{TB1}\ (\text{initial}) - q_t^{TB1}\ (\text{final})\right] \quad \text{(B-28)}$$

and since q_t^{S1} (final) = q_t^{TB1} (initial) this reduces to

$$\Delta Q_{SUM} = q_t^{S1}\ (\text{initial}) - q_t^{TB1}\ (\text{final}). \quad \text{(B-29)}$$

In other words, ΔQ_{SUM} depends only on the initial state of the bulk traps before Q_{S1} enters the CCD well and the final state of the bulk traps after Q_{TB1} transfers out of the CCD well.

Immediately following a signal-regeneration stage in the low-loss CCD, Q_{TB0} and Q_{TB1} are exactly equal so that the term $V_{TB0}-V_{TB1}$ in Eq. (B-27) is negligible. During each subsequent charge transfer down the CCD delay line

the volumes V_{TBO} and V_{TB1} both decrease due to the first-order charge-transfer losses ΔQ_{TBO} and ΔQ_{TB1}, respectively. However, since Q_{TBO} is decreasing faster than Q_{TB1}, a charge difference $Q_{TB1}-Q_{TBO}$ builds up on the trailing bias charge level which is proportional to the number of transfers i following the regeneration stage. It is this charge difference $Q_{TB1}-Q_{TBO}$ which causes the nonzero second-order transfer loss ΔQ_{SUM} in Eq. (B-27) since a corresponding volume difference $V_{TBO}-V_{TB1}$ is present in the buried channel well.

In order to evaluate the term $V_{TBO}-V_{TB1}$, we assume that the volume occupied by mobile charge carriers is linearly proportional to the size of the charge packet, which is a good approximation for relatively large signals in a BCCD [6]. Thus,

$$V_{TBO} - V_{TB1} = \frac{\partial V}{\partial Q} (Q_{TBO} - Q_{TB1}) \tag{B-30}$$

where $\frac{\partial V}{\partial Q}$ is the proportionality constant relating the volume to charge.

In general, during the i^{th} transfer following a signal-regeneration stage the magnitude of Q_{TBO} and Q_{TB1} is given by:

$$Q_{TBO}(i) = Q_{TBO}(0) + \sum_{j=1}^{i-1} \Delta Q_{TBO}(j) \tag{B-31}$$

$$Q_{TB1}(i) = Q_{TB1}(0) + \sum_{j=1}^{i-1} \Delta Q_{TB1}(j) \tag{B-32}$$

where $Q_{TBO}(0) = Q_{TB1}(0) = Q_{TB}$ is the initial value of the trailing bias charge established in the signal-regeneration stage. Combining Eqs. (B-31) and (B-32).

$$Q_{TBO}(i) - Q_{TB1}(i) = \sum_{j=1}^{i-1} \left[\Delta Q_{TBO}(j) - \Delta Q_{TB1}(j)\right] . \tag{B-33}$$

The term $\delta Q_{Tb} \equiv \Delta Q_{TBO} - \Delta Q_{TB1}$ can be evaluated by substituting from Eqs. (B-17) and (B-26) and rearranging terms to obtain:

$$\Delta Q_{TBO} - \Delta Q_{TB1} = n_t e^{\frac{-T_T'}{\tau_e}} \left[(V_{SO} - V_{S1} + V_{TB1} - V_{TBO}) + (V_{S1} - V_{SO})\, e^{\frac{-(T_T+T_S)}{\tau_e}} \right] . \tag{B-34}$$

AD-A072 989 RCA LABS PRINCETON N J F/G 9/5

LOW-LOSS CHARGE-COUPLED DEVICE.(U)

JUN 79 W J KOSONOCKY, D J SAUER, C Y TAYAG F19628-77-C-0176

UNCLASSIFIED PRRL-78-CR-57 RADC-TR-79-144 NL

2 OF 2

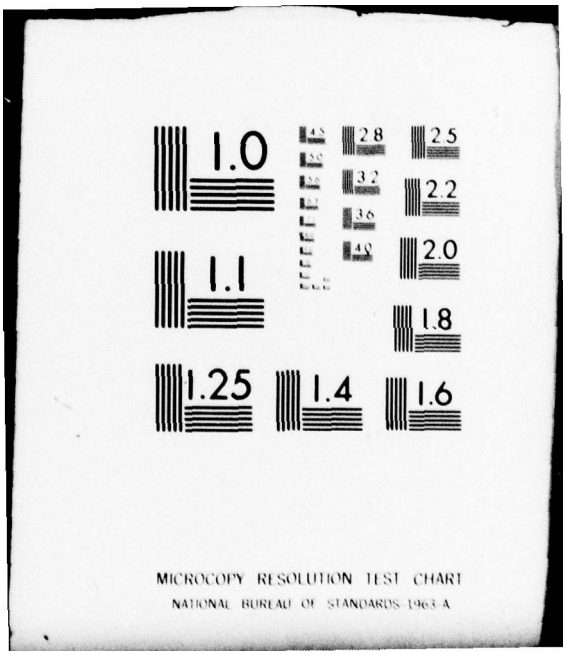
AD A072989

END

DATE FILMED

9-79

DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

We now make the assumption that the first-order losses are sufficiently low so that for the purpose of evaluating Eq. (B-34), $(V_{TB1}-V_{TB0}) << (V_{S0}-V_{S1})$ and $V_{S0}-V_{S1}$ is independent of the number of transfers i. With this assumption, Eq. (B-34) becomes:

$$\delta Q_{TB} \equiv \Delta Q_{TB0} - \Delta Q_{TB1} = n_t (V_{S0} - V_{S1}) e^{\frac{-T_T'}{\tau_e}} \left(1 - e^{\frac{-(T_T+T_S)}{\tau_e}}\right). \quad \text{(B-35)}$$

Combining Eqs. (B-27), (B-30), (B-33), and (B-35) we obtain an expression for the second-order trapping loss during the i^{th} transfer:

$$\Delta Q_{SUM}(i) = i\, n_t\, e^{\frac{-T_T'}{\tau_e}} \frac{\partial V}{\partial Q} \delta Q_{TB} . \quad \text{(B-36)}$$

For a low-loss CCD which has n transfers between regeneration stages, the total second-order trapping loss $\Delta Q_{SUM}(tot)$ following n transfers can be expressed as:

$$\Delta Q_{SUM}(tot) = \sum_{i=1}^{n} \Delta Q_{SUM}(i) = (1+2+\ldots+n)\, n_t e^{\frac{-T_T'}{\tau_e}} \frac{\partial V}{\partial Q} \delta Q_{TB} \quad \text{(B-37)}$$

or

$$\Delta Q_{SUM}(tot) = \frac{n(n+1)}{2}\, n_t\, e^{\frac{-T_T'}{\tau_e}} \frac{\partial V}{\partial Q} \delta Q_{TB} . \quad \text{(B-38)}$$

Finally, the average second-order fractional transfer loss $\varepsilon_2 = \Delta Q_{SUM}(tot)/n(Q_{S1}-Q_{S0})$ is given by:

$$\varepsilon_2 = \frac{n+1}{2(Q_{S1}-Q_{S0})}\, n_t\, e^{\frac{-T_T'}{\tau_e}} \frac{\partial V}{\partial Q} \delta Q_{TB} . \quad \text{(B-39)}$$

In view of the number of assumptions which were made to simplify the foregoing analysis, some of the factors which limit the accuracy of Eq. (B-39) should be

considered. We have implicitly assumed that the trap occupancy n_t given by Eq. (B-4) is constant throughout the volume occupied by the charge packet. Actually, the value of n_t near the edges is lower since the free charge density n_e is lower at these points, which increases the trapping time constant τ_t. In addition, in the transfer regions of the CCD as the free charge sweeps by, there is a filling probability F for the bulk traps which also reduces the value of n_t in these regions. As a result, the second-order transfer loss ε_2 given by Eq. (B-39) using a value $n_t = eN_t$ represents a 'worst case' value which we have found to be typically about 2 times higher than experimentally measured values.

D. INTERACTION OF MULTIPLE BULK-TRAPPING STATES

The analysis in Part C for the second-order trapping loss was based on a single bulk-trapping state model. In a buried-channel device with multiple bulk-trapping states, the interaction of these states must be considered to determine the second-order losses. For a device having m bulk-trapping states with energy levels E_1 to E_m, we can modify the expression for δQ_{TB} in Eq. (B-35) to:

$$\delta Q_{TB} = (V_{SO}-V_{S1}) \sum_{E=E_1}^{E_m} n_t(E)\, e^{\frac{-T_T'}{\tau_e(E)}} \left[1 - e^{\frac{-(T_T+T_S)}{\tau_e(E)}}\right]. \qquad \text{(B-40)}$$

The fractional transfer loss given by Eq. (B-39) is modified according to:

$$\varepsilon_2 = \frac{n+1}{2(Q_{S1}-Q_{SO})} \sum_{E=E_1}^{E_m} n_t(E)\, e^{\frac{-T_T'}{\tau_e(E)}} \frac{\partial V}{\partial Q}\, \delta Q_{TB}\,. \qquad \text{(B-41)}$$

E. SECOND-ORDER TRANSFER LOSS FOR CLOSED-LOOP OPERATION

When the low loss CCD is recirculating with a loop cycle time (i.e., total time around the closed loop) T_L which is comparable to a bulk-trap emission time constant τ_e, then the bulk traps in the edge volume $(V_{TB1}-V_{TBO})$ do not completely empty in the time T_L. As a result, less charge is trapped,

and Eq. (B-27) must be modified to:

$$\Delta Q_{SUM} = n_t \left[e^{\frac{-T_T'}{\tau_e}} - e^{\frac{-T_L}{\tau_e}} \right] (V_{TB0} - V_{TB1}) \quad . \tag{B-42}$$

Using this result in combination with multiple bulk-trapping states results in a second-order fractional transfer loss of:

$$\varepsilon_2 = \frac{n+1}{2(Q_{S1} - Q_{S0})} \sum_{E=E_1}^{E_m} n_t(E) \left[e^{\frac{-T_T'}{\tau_e}} - e^{\frac{-T_L}{\tau_e}} \right] \frac{\partial V}{\partial Q} \delta Q_{TB} \tag{B-43}$$

where δQ_{TB} is given by Eq. (B-40).

F. CHARGE-TRANSFER LOSSES DUE TO SIGNAL-REGENERATION STAGE

As discussed in Sections IV.D and IV.E, the signal-regeneration stage introduces the additional transfer losses ε_{1R} and ε_{2R} (see Eqs. 17 and 21 Section IV) which must be added to the second-order loss ε_{TOT}. The leading-edge transfer loss ε_{LE} used to calculate ε_{1R} and ε_{2R} may be expressed in terms of the bulk-trapping states as:

$$\varepsilon_{LE} = \sum_{E=E_1}^{E_m} n_t(E) \left[e^{-\frac{T_T'}{\tau_e(E)}} - e^{-\frac{T_L}{\tau_e(E)}} \right] \frac{\partial V}{\partial Q} \quad . \tag{B-44}$$

The trailing-edge transfer loss ε_{TE} may also be expressed as:

$$\varepsilon_{TE} = \frac{\delta Q_{TB}}{Q_{S1} - Q_{S0}} \tag{B-45}$$

where δQ_{TB} is given by Eq. (B-40). Therefore the total second-order charge transfer loss is given by (cf. Eq. 22 Section IV):

$$\varepsilon_{TOT} = \varepsilon_{LE} \left(\frac{2}{n} + \frac{n+1}{2} \varepsilon_{TE} + \varepsilon_{BB} \right) \tag{B-46}$$

where ε_{LE} is defined by Eq. (B-44), ε_{TE} is defined by Eq. (B-45), and ε_{BB} is measured as discussed in Section IV.E.

G. SAMPLE CALCULATION

Our data (see Section III.C) indicated the presence of two bulk-trapping states in the TC1230 BCCD with the following densities and emission times:

$$n_t(E_1) = 5.8 \times 10^{-8} \text{ C/cm}^3$$
$$\tau_e(E_1) = 5.6 \text{ μs}$$

$$n_t(E_2) = 5.8 \times 10^{-8} \text{ C/cm}^3$$
$$\tau_e(E_2) = 750 \text{ μs}$$

For the case of a TC1230 256-stage CCD operating at 1.1 MHz, the following parameters were measured:

$$Q_{SO} = 3.6 \times 10^{-14} \text{ C}$$
$$Q_{S1} = 9.6 \times 10^{-14} \text{ C}$$
$$T_T' = T_S = 0.45 \text{ μs}$$
$$\varepsilon_{BB} = 7 \times 10^{-3}$$

A value for $\frac{\partial V}{\partial Q}$ of $5\text{x}10^2 \text{cm}^3/\text{C}$ was estimated based on a buried-channel layer depth of 0.5 μm, and a storage area of 25 μm x 10 μm. Substituting these numbers into Eqs. (B-44), (B-45), and (B-46) we obtain the calculated values of $\varepsilon_{LE} = 3.45\text{x}10^{-5}$, $\varepsilon_{TE} = 0.4\text{x}10^{-5}$, and $\varepsilon_{TOT} = 4.1\text{x}10^{-7}$ The measured transfer loss for this device operating in the low-loss mode was $2.4\text{x}10^{-7}$.

MISSION
of
Rome Air Development Center

RADC plans and executes advanced development, test and selected acquisition programs in support of Command, Control, Communications and Intelligence (C³I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.