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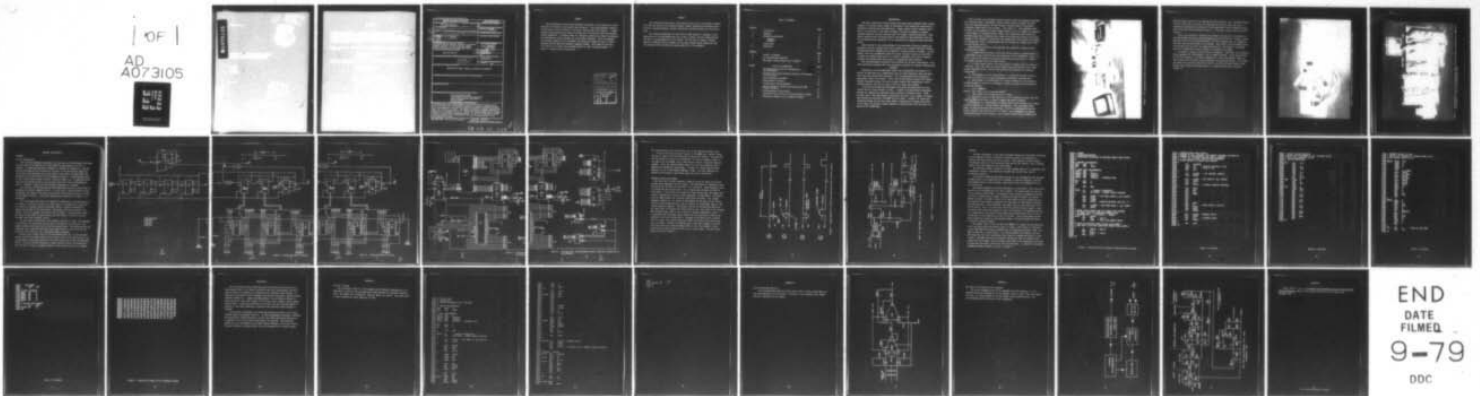
AEROSPACE MEDICAL RESEARCH LAB WRIGHT-PATTERSON AFB OH
DESIGN OF A MICROPROCESSOR BASED CARDIOTACHOMETER. (U)
APR 79 D RATINO, G POTOR, A MARKO, C SHARPER
AMRL-TR-79-21

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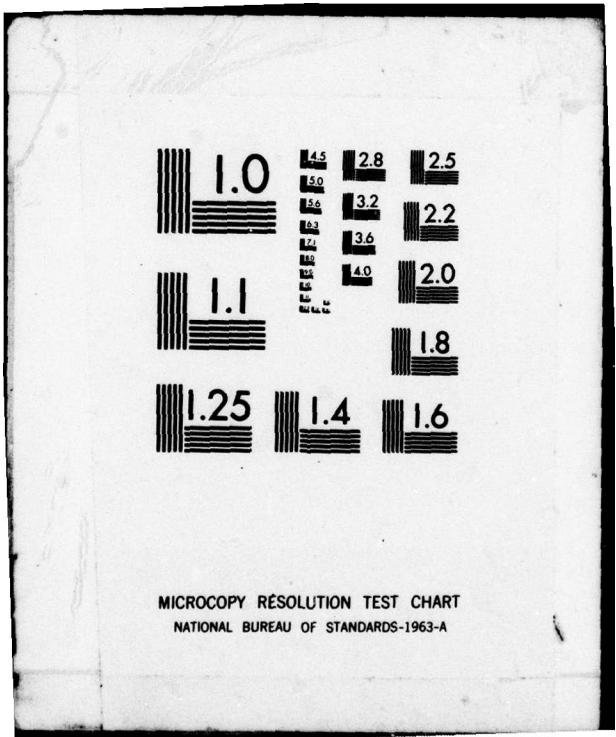
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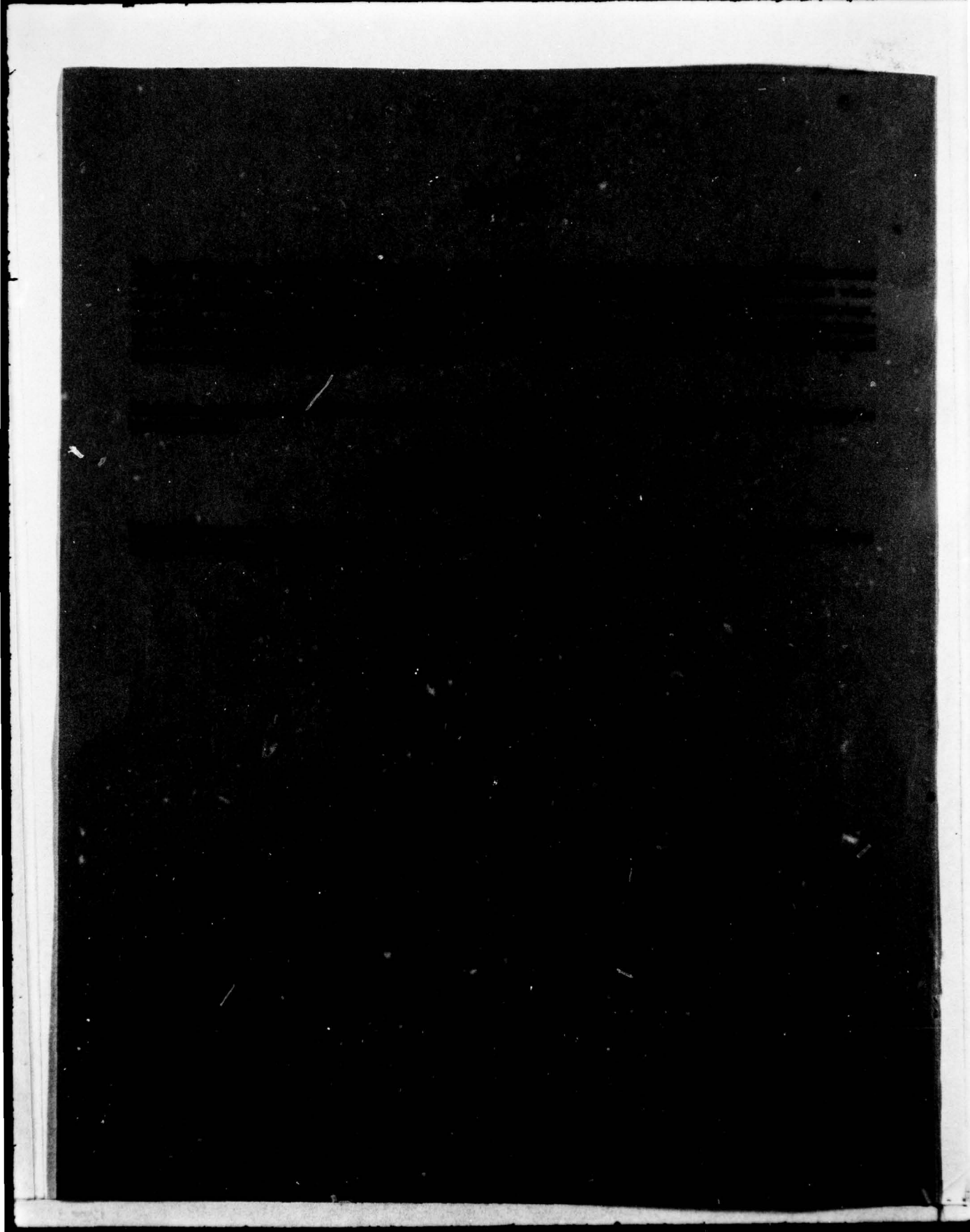


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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A microprocessor based cardiotaohometer has been designed and fabricated in-house using 8080 Intel microcomputer hardware and assembly language software. The cardiotaohometer accurately calculates and digitally displays beat-by-beat hear rate in beats per minute. The design incorporates standard semiconductor memory and I/O integrated circuits. Operational understanding does not require extensive microprocessor design background. In fact, the cardiotaoh's design provides excellent basic information in the use of microprocessor in the instrumentation field.			

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SUMMARY

The microprocessor based cardiometer described in this report was tested and found to function very reliably and accurately. The cardiometer requires no calibration and yet produces an errorless digital heart rate readout. A simple modular design approach was achieved through the utilization of 8080 Microcomputer system components. A minimum number of integrated circuits were used to accomplish the interfacing, timing, memory, and input/output functions. Both the hardware and software aspects of the instrument are explained through the use of circuit diagrams and the annotated assembly language program. The reason for writing this report is to convey the knowledge gained to other interested people who desire to design with microprocessors.

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PREFACE

The research and development described here was carried out between September 1977 and June 1978 in the Simulation Support Branch, Manned-Systems Effectiveness Division, Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

The authors acknowledge the assistance of TSgt Gregory D. Bathgate in the fabrication of the instrumentation, Mrs. Lynda A. Powell, and Mrs. Margy Horvath for help in the preparation of this report. We also wish to thank Mr. Donald McCollor, Raytheon Service Company, for his power supply design suggestions and the inclusion of his electro-cardiogram amplifier in the appendix.

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INTRODUCTION

The rapid evolution of microprocessor and large scale integrated (LSI) circuit elements is causing a major change of philosophy in the design and construction of electronic apparatus and instrumentation. Highly complex circuit modules, available at low cost and in very small packages, has made it possible to package complete computers in small portable units for single, dedicated functions. This report resulted from the efforts made by the authors to gain experience with the use of microprocessor components in the construction of special purpose instrumentation.

Since details of the inner-workings of microprocessor chips are complex and frequently obscure, designs using these elements must proceed "cook-book" fashion, using manufacturers suggestions and samples of working products as models. At the outset, there was considerable skepticism about the early success of this effort. A project was needed which would be as simple as possible, yet utilize computer concepts and components and also result in a needed and useful product.

The cardiometer described here fulfilled all of these requirements. Circuits incorporate designs taken from information supplied by component manufacturers.

APPROACH

Obtaining an electrocardiograph signal and electronically processing it to extract the QRS event as a standardized pulse of fixed amplitude, shape and duration, uses well established techniques. The following method was proposed for developing a heart rate display. Start with the QRS signal, measure the interval between successive pulses, from this interval compute the instantaneous rate in beats-per-minute, and use the result to drive a three digit display.

A facility for design and development work had to be established for this project and for future projects as well. A number of microprocessor development systems are commercially available using a variety of processor chips. These systems cover a very wide range of flexibility and cost. For a number of reasons, some necessarily arbitrary, the 8080 chip was chosen. Probably the single most compelling reason was the very large number of manufacturers making parts based on this chip, all within a single framework of compatibility which has come to be known as the "S-100 Buss".

Thus, we built our development system around an IMSAI microcomputer mainframe (with operator panel), 16K memory, Tarbell Format Cassette Storage, Processor Tech ALS-8 Operating System, CRT and Teletype terminals and an "Intelligent Breadboard" (Model BBC-5) also by IMSAI. (see Figure 1). The breadboard forms the heart of the system for circuit design purposes, as it is capable of accepting a large number of integrated circuit chips of all shapes and sizes along with necessary capacitors, resistors, etc.; while providing direct access to the inner workings of the computer. In this way, the computer not only controls the signals for testing new circuit configurations, but also becomes an integral part of the circuits as they evolve.

The architecture which was developed for the cardiotech consists of the following main elements:

1. An 8080 central processor chip (CPU) which executes a program stored in a 2708 EPROM, using a 6810 RAM chip for 128 bytes of 8-bit read/write memory. An 8228 is used as the system controller and bi-directional bus driver. A 8224 is the systems' crystal controlled master clock.

2. A 16-bit binary counter (two 8-bit chips in tandem) driven to count at a 1 KHz rate. The 1 KHz signal, derived by decade countdown from the CPU'S 2 MHz crystal controlled clock, serves as the precise time reference for counting milliseconds.

3. The program runs in a loop waiting for a pulse from the QRS circuits. This pulse is received via a 8255A programmable peripheral interface chip.

4. Upon receipt of the QRS pulse, the counter contents are transferred to the CPU whereupon a division is performed to obtain the heart rate according to the trivial formula:

$$H R = 60000/MS$$

Where -- HR = heart rate in beats per minute

MS = number of millisecond counts per beat.

5. The binary results of this division is then converted to three 4-bit BCD digits and fed via an 8255A to three 7-segment LED numeric displays.

The procedure for implementing this design started with setting up the components for the counters, display LED and interfacing on the intelligent breadboard, to allow development of the software. The first configuration used two 8255's - one for input and the other for output. After debugging the program sufficiently to get correct results, various modifications in both software and

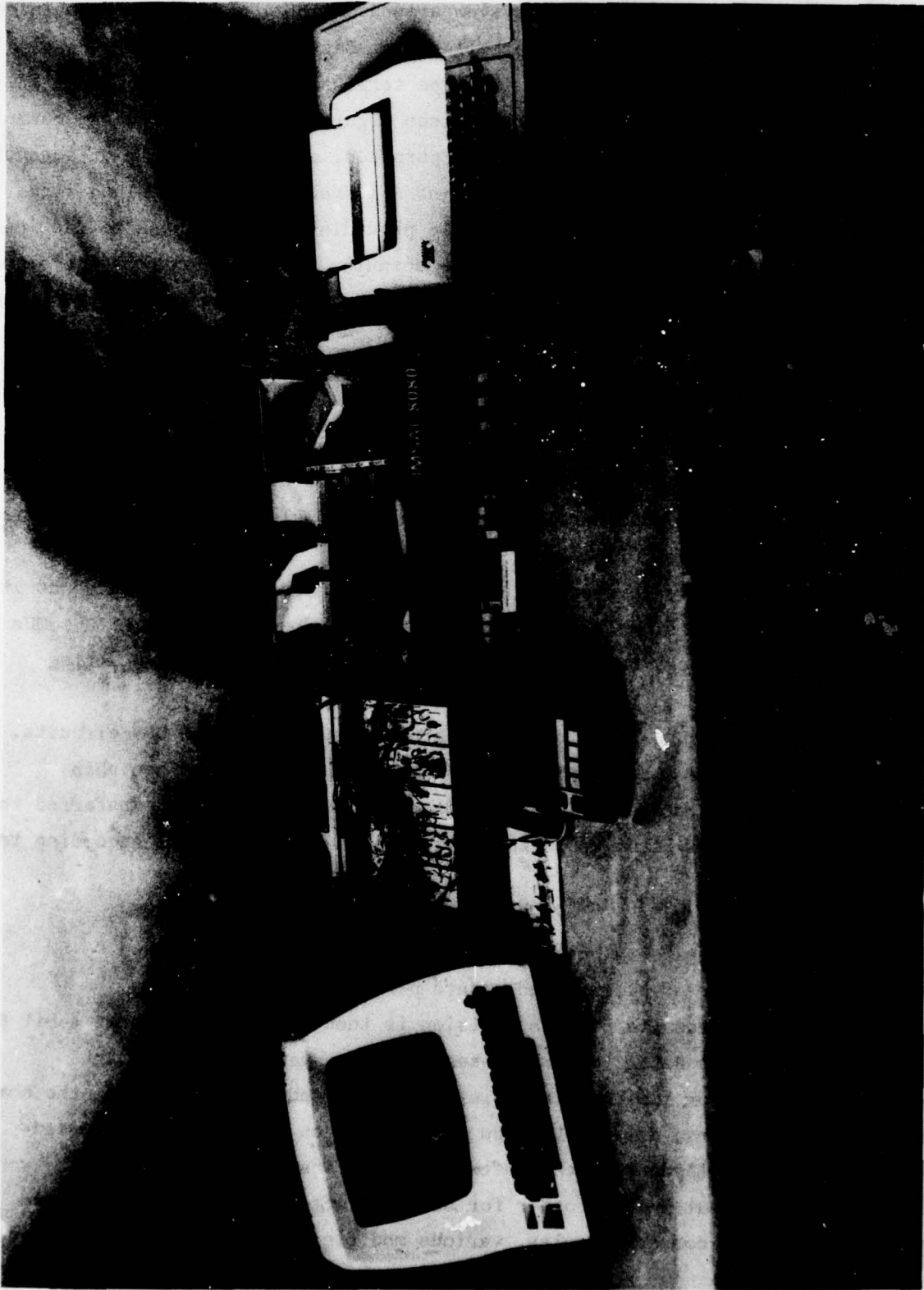


Figure 1. The experimental setup for designing the cardiometer.

hardware details were tried to simplify the entire system. This included eliminating one of the 8255's and using the remaining one for both input and output. A stand-alone experimental prototype of the microprocessor system hardware was then built using wire-wrap techniques (Figure 2). This was a crucial step for several reasons.

First, the interactive terminal and software aids would not be available in the wire-wrapped prototype, making debugging much more difficult. Second, a great majority of the circuit features needed in the full computer were not needed for this unit and were eliminated in this design. The results of these changes would not be known until the unit was completed and tried. And finally, the program would be on EROM and not easily subject to examination or change.

As expected, results of first tests were negative. Very short test procedures were programmed into 2708 EPROMS to aid in signal tracking. (The listing of one of the test programs is included in Appendix A). After considerable labor over what turned out to be minor circuit omissions, the prototype worked. It was used as a model for the construction of the final unit which included etched circuit boards, power supply and display panel in a complete stand-alone enclosure (Figure 3).

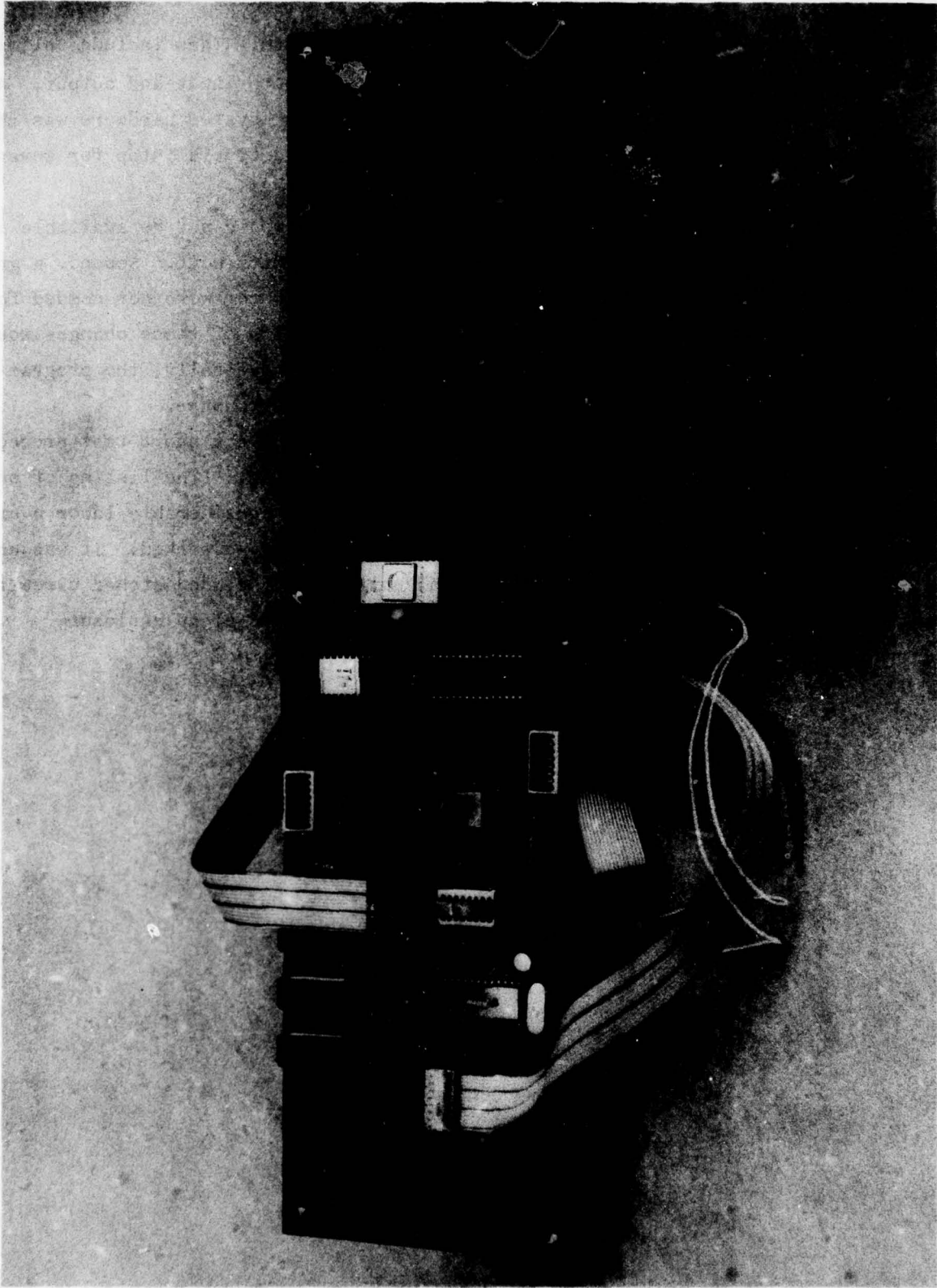


Figure 2. Microprocessor system hardware prototype wire-wrapped on vector board.

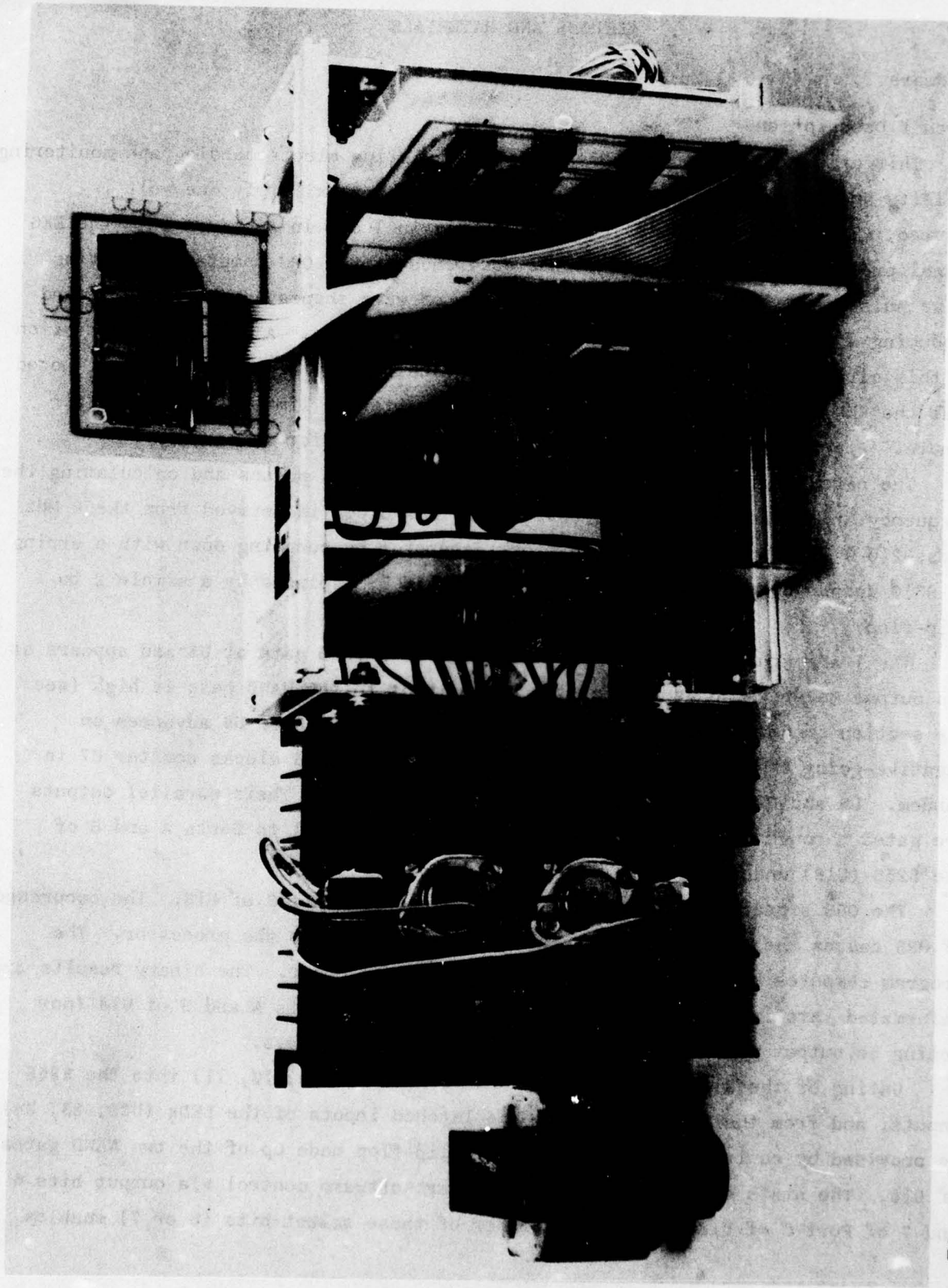


Figure 3. Cardiotachometer card rack showing power supply card, EKG signal processing card, 8080A CPU card, P8255A I/O card, and counter/buffer card.

METHODS AND MATERIALS

Hardware

Circuit Description

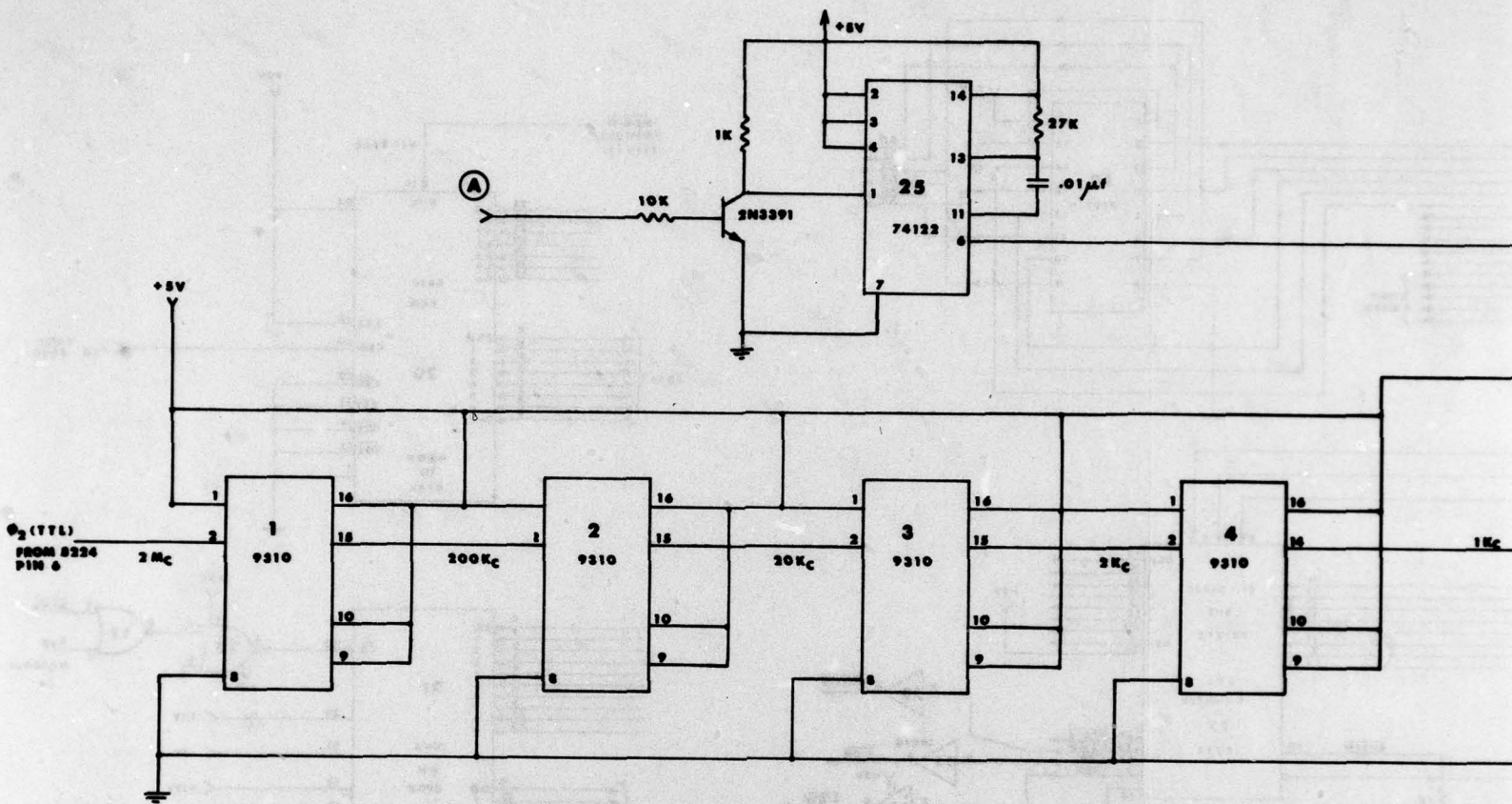
This unit was designed to operate in an existing electrocardiograph monitoring facility and the availability of an EKG signal of approximately one volt is assumed. (A simple EKG amplifier schematic is included in Appendix B.) The EKG signal processing section extracts the occurrence of the QRS complex, rejecting noise pulses and operating over a wide range of wave shapes and amplitudes, and producing a ± 2.5 volt pulse of 125 milliseconds duration. A detailed description of this circuit may be found in another technical report (1). It should be noted that the EKG processing section has an upper heart rate limit of 300 beats per minute. Appendix C shows block and schematic diagrams for reference.

The circuitry for determining the time between QRS pulses and calculating the frequency are shown in Figures 4 and 5. A 1 KHz clock is derived from the 2 MHz phase-2(\emptyset_2) TTL output of the 8224 clock generator by counting down with a string of 931 \emptyset decade counters. (The fourth 931 \emptyset could be replaced by a simple 2 to 1 flip-flop).

The 1 KHz square wave from U4 is applied to a NAND gate at U5 and appears at its output to drive U6 as long as the other input to the NAND gate is high (see the section of Sequence Control and Timing, below). Counter U6 advances on negative-going edge of the clock pulse. The output of U6 clocks counter U7 in tandem. U6 and U7 together thus form a 16-bit counter. Their parallel outputs are gated through 8T97 tri-state buffers U9, U10, and U11 to Ports A and B of the 8255 (U18) under software control.

The QRS signal is monitored by the software via Port C of U18. The occurrence of QRS causes the count since the last QRS to be input to the processor. The program computes beats per minute from the interval count. The binary results are reformatted into individual BCD digits and output via Ports A and B of U18 (now acting as output ports) to the latched LED numeric displays.

Gating of the signals from the counters buffers (U9, 1 \emptyset , 11) into the 8255 inputs, and from the 8255 outputs to the latched inputs of the LEDs (U22, 23, 24), is provided by control levels from the RS flip-flop made up of the two NAND gates of U15. The state of this flip-flop is under software control via output bits 6 and 7 of Port C of U18. A high to either of these select bits (6 or 7) enables



POWER REQUIREMENTS

- +8V @ 900MA
- 8V @ 25 MA
- +12V @ 125 MA
- 12V @ 25 MA

10:ENABLE
 ENABLE
 BUFFER
 COUNTER #1

1

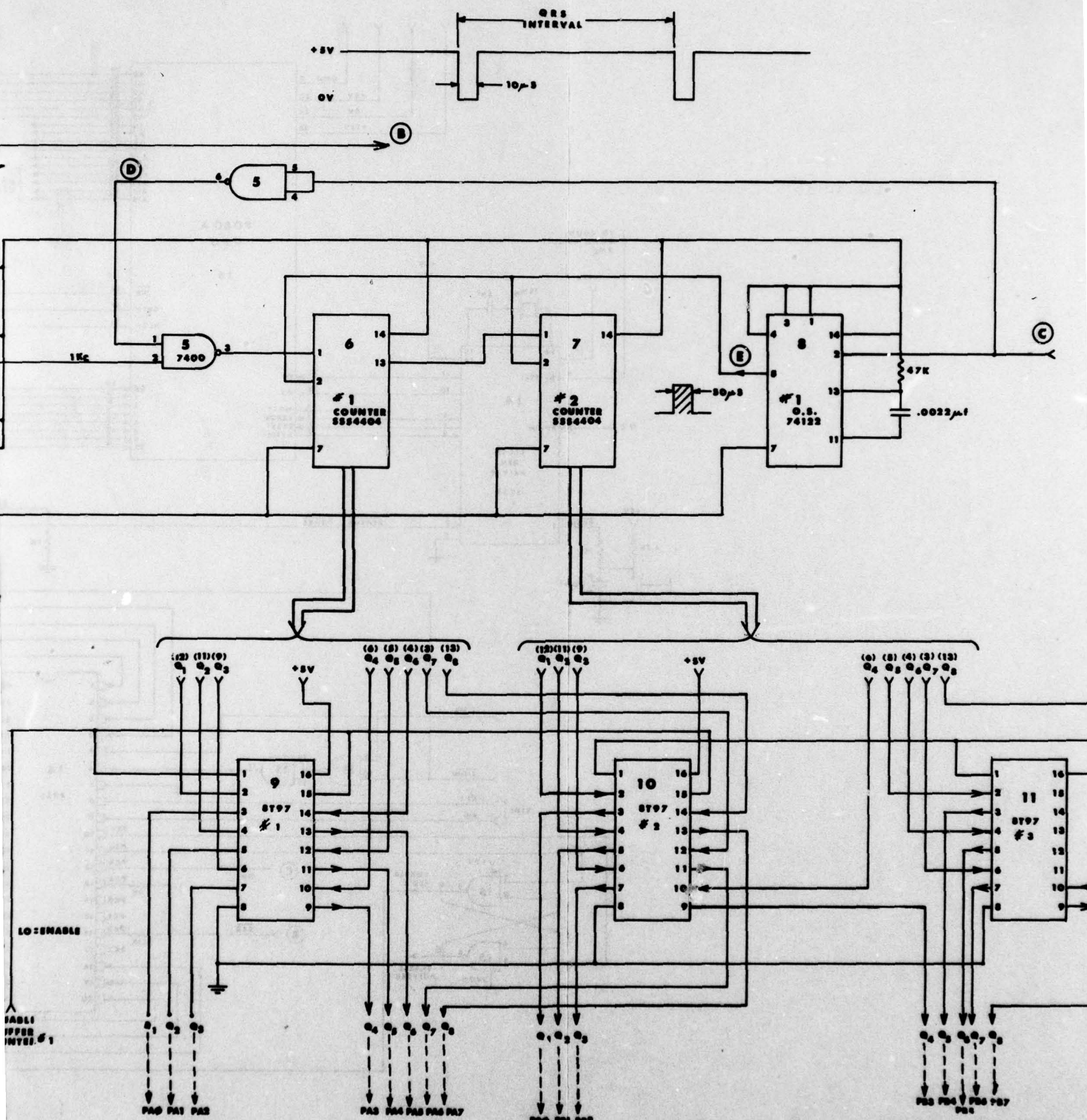


Figure 4. Timing and buffer circuitry.

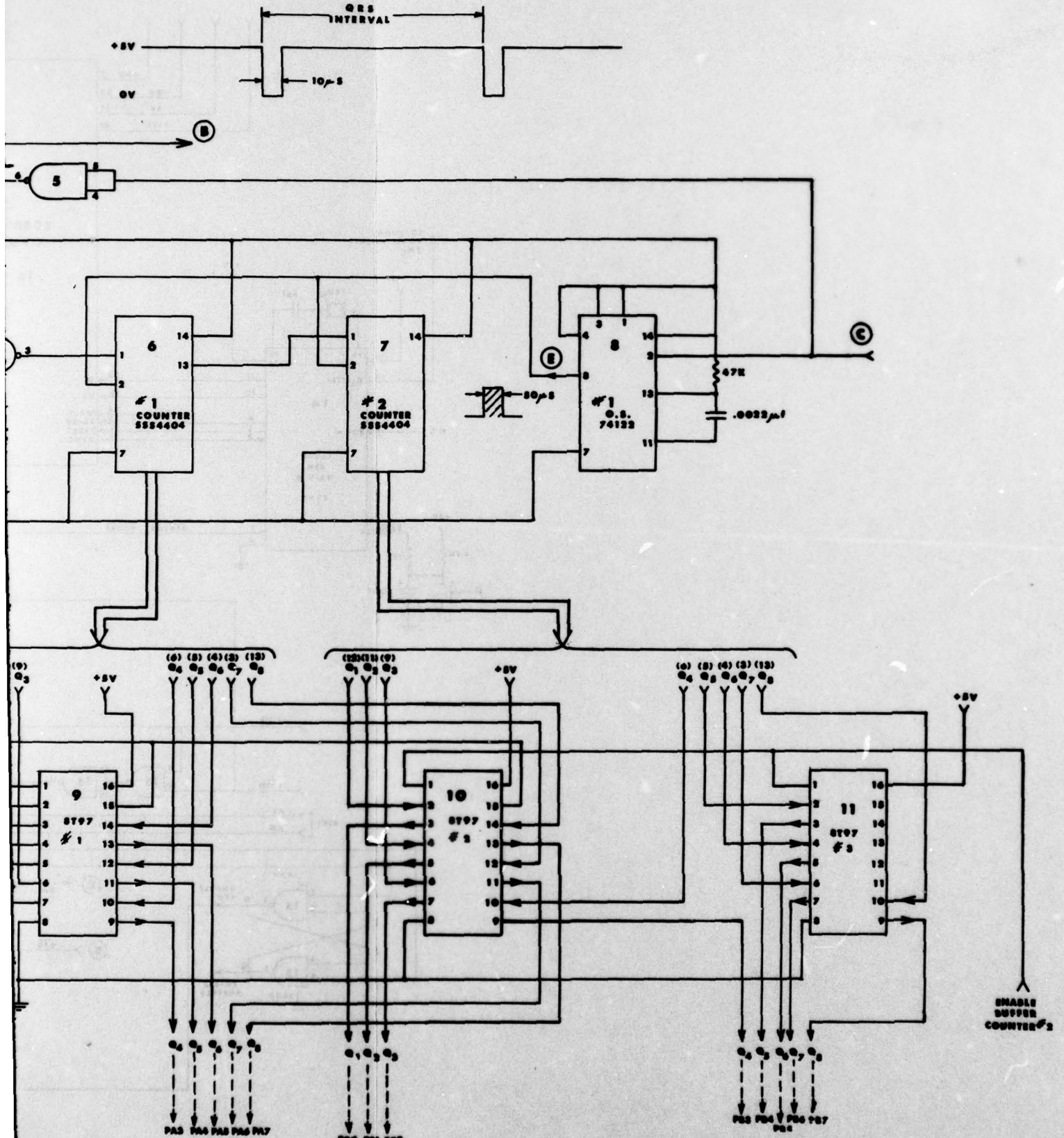


Figure 4. Timing and buffer circuitry.

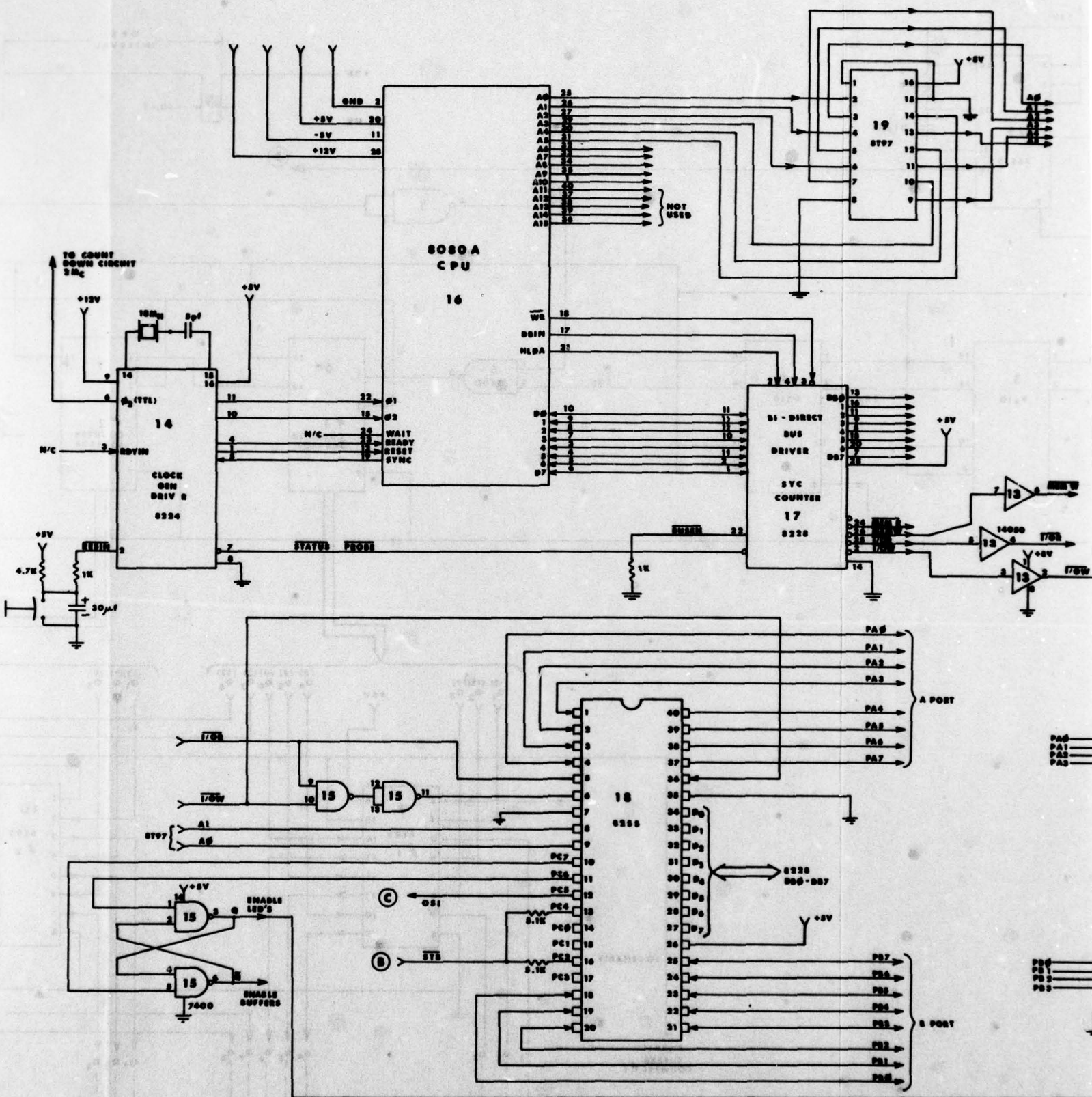


Figure 5. Microprocessor system schematic.

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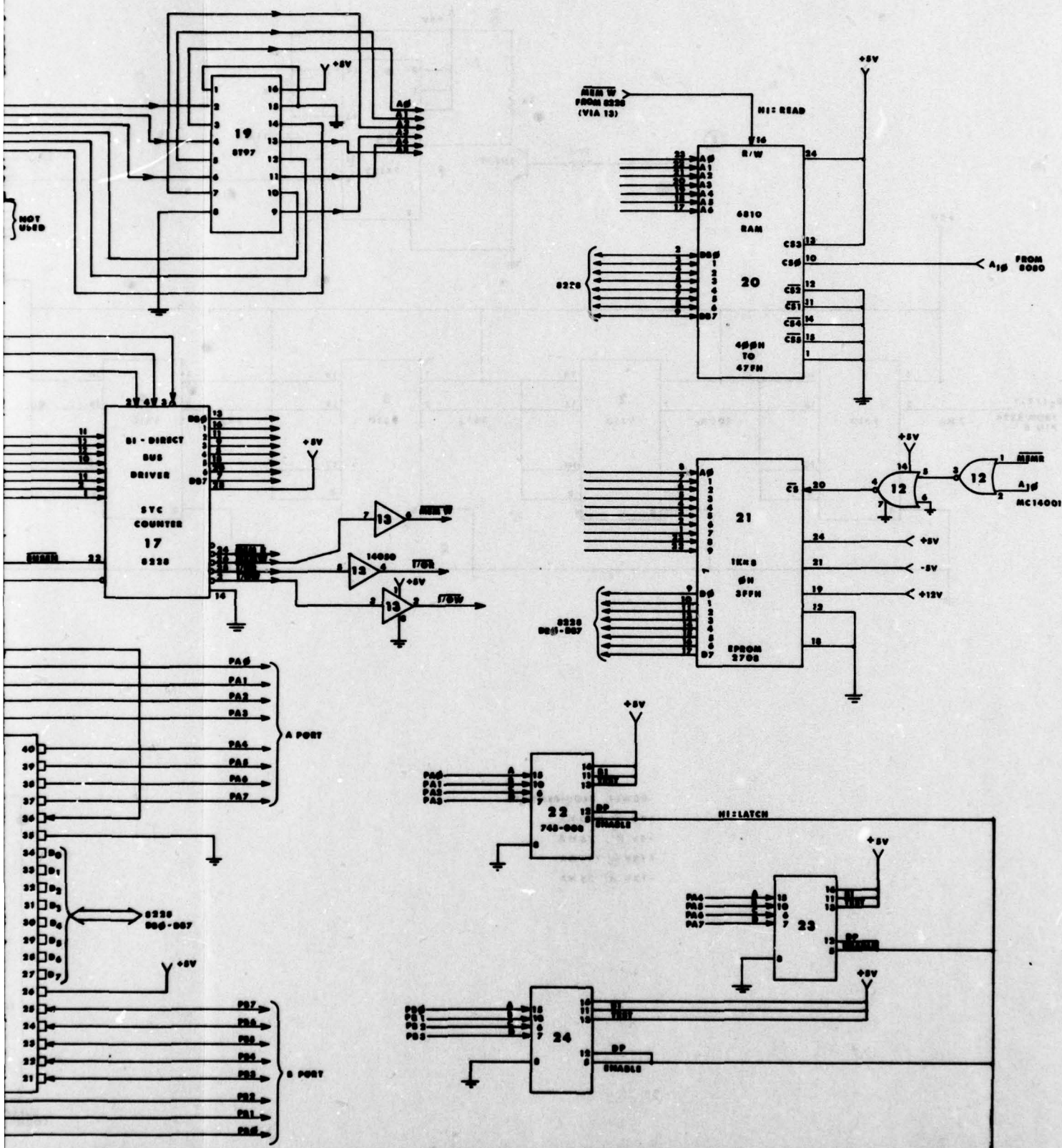


Figure 5. Microprocessor system hardware which essentially constitutes a microcomputer.

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the corresponding device by putting a low on the appropriate enable line.

The main processing elements consist of the 8080A and a typical configuration of support chips extracted from manufacturers manuals. The 8228 uses U13 for additional control line buffering. The control program resides in the 2708 1K by 8 UV-EPROM, with a 6810 128 by 8 RAM for stack and temporary storage. Since the required memory space is so limited, elaborate 16-bit address buss decoding is unnecessary. A single bit (A-10) selects ROM at address 0 if low or RAM address 400-HEX if high. The 8255 completes the system by providing all input/output data and control connections.

Sequence Control and Timing:

The 74122 (U25) one-shot produces a negative going TTL pulse of 10 microseconds which represents the QRS signal. This QRS signal is connected to pins PC4 and PC2 of the 8255 via individual 5.1 K resistors. These resistors serve to isolate PC2 and PC4 when Port C is in output mode and have no effect in input mode. A low on this line strobes or loads counter data into input Ports A and E, respectively. With the 8255 configured in Input Mode-1, the strobe sets the input buffer full flip-flop (IBF) within the 8255. (See timing diagram in Figure 6.) The output of IBF appears at PC5 where it can be monitored by the software and also used to serve as an acknowledge signal to the counter system as follows. The normally low PC5 is inverted and applied to the other input of the gate (U5) which controls the 1 KHz clock to the counters. When PC5 goes high, input to U6 is held low, thereby stopping the count. It is essential that the count remain stable until the data can be read by the software; first Port B, then Port A. Reading of the data on Port A causes IBF to be reset (this occurs within the 8255) which allows the clock pulses to U6 to resume. However, the falling edge of IBF also triggers a one-shot (U8) which delivers a 50 microsecond pulse to reset the counters to zero. Counting thus restarts after the fall of the reset signal. The units power supply is given in Figure 7.

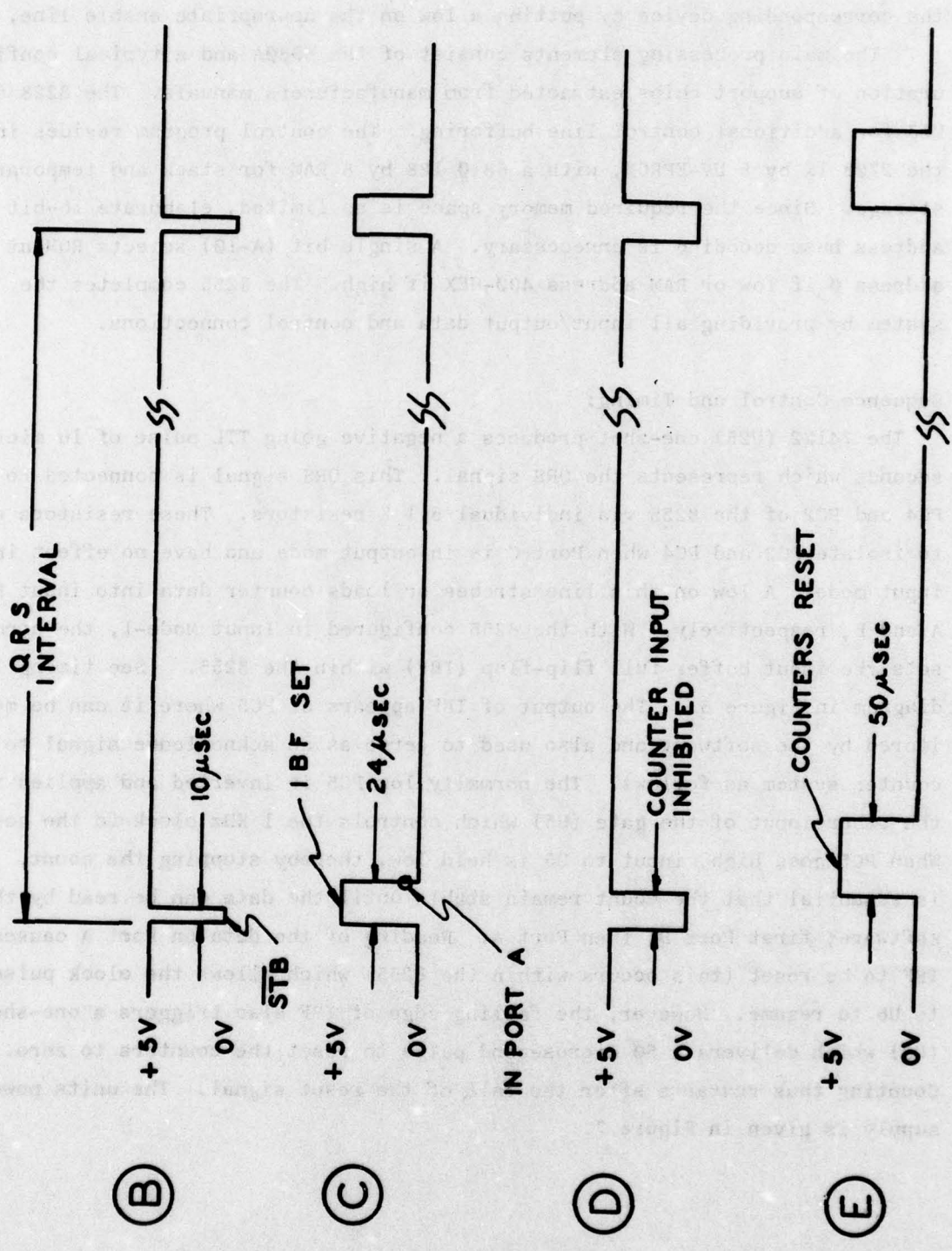
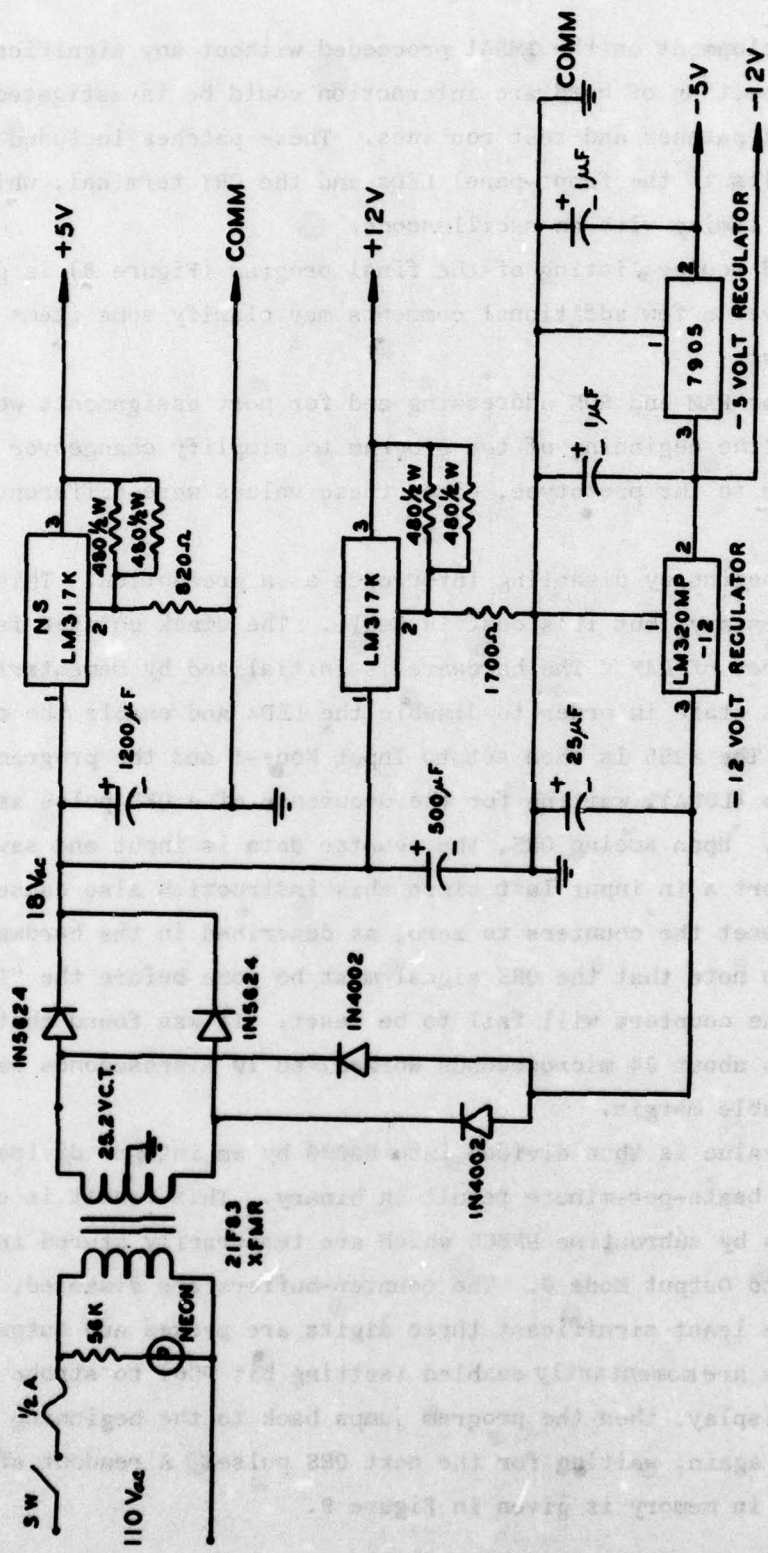


Figure 6. Timing diagram for reading and resetting the QRS interval counters.



NOTE: ALL REGULATORS ARE MOUNTED ON A SINK HEAT

Figure 7. Cardiometer power supply.

Software

Software development on the IMSAI proceeded without any significant difficulty as each separate section of hardware interaction could be investigated in isolation by small patches and test routines. These patches included sending intermediate results to the front-panel LEDs and the CRT terminal, while checking signal levels and timing with an oscilloscope.

The annotated source listing of the final program (Figure 8) is generally self-explanatory, however a few additional comments may clarify some items of particular interest:

The values for RAM and ROM addressing and for port assignments were assigned parametrically at the beginning of the program to simplify changeover from the development system to the prototype, since these values were different for the two situations.

The program begins by disabling interrupts as a precaution. This instruction should not be necessary, but its cost is small. The stack pointer is then set to an available area of RAM. The hardware is initialized by momentarily setting the 8255 to output state in order to disable the LEDs and enable the counter-buffer circuits. The 8255 is then set to Input Mode-1 and the program enters a test-and-wait loop (LOPA), waiting for the occurrence of a QRS pulse as detected by PC5 going high. Upon seeing QRS, the counter data is input and saved, first Port B then A. Port A is input last since this instruction also causes a chain of events which reset the counters to zero, as described in the hardware section. It is important to note that the QRS signal must be gone before the "In Port A" instruction, or the counters will fail to be reset. It was found that any QRS pulse length up to about 24 microseconds worked, so 10 microseconds was chosen to provide a reliable margin.

The counter value is then divided into 60000 by an integer divide subroutine (DIV), giving the beats-per-minute result in binary. This result is converted to five BCD digits by subroutine BNBCD which are temporarily stored in RAM. The 8255 is then set to Output Mode 0. The counter-buffers are disabled, and the BCD values for the least significant three digits are packed and output to Ports A and B. The LEDs are momentarily enabled (setting bit PC6) to strobe the new values into the display, then the program jumps back to the beginning of the loop to start all over again, waiting for the next QRS pulse. A readout of the EPROM's assembled program in memory is given in Figure 9.

```

0010 * CARDS
0020 * CARDIOTACHOMETER.
0030 * HEARTRATE DISPLAYED IN DECIMAL BEATS PER MINUTE.
0040 *
0050 *
0060 * MEMORY ASSIGNMENTS
0070 ROM EQU 0
0080 RAM EQU 400H
0090 *
0100 * 8255 PORT ASSIGNMENTS:
0110 PORTA EQU 0
0120 PORTB EQU PORTA+1
0130 PORTC EQU PORTA+2
0140 CNTRL EQU PORTA+3 ; CONTROL PORT
0150 *
0160 PSV EQU 6
0170 SP EQU 6
0180 *
0190 ORG ROM
0200 *
0210 LOOP: DI ; DISABLE INTERRUPTS
0220 LXI SP,STACK ; RESET STACK POINTER
0230 *
0240 MVI A,80H ; SET 8255 MODE 0, ALL OUTPUT
0250 OUT CNTRL
0260 MVI A,80H
0270 OUT PORTC ; ENABLE BUFFERS (SET BIT 7)
0280 *
0290 MVI A,8BFH ; SET 8255 MODE 1, ALL INPUT
0300 OUT CNTRL
0310 *
0320 * EVENT PULSE SHOULD BE NO LONGER THAN APPROX.
0330 * 20 USEC. MUST BE COMPLETED BEFORE THE
0340 * INSTRUCTION - < IN PORTA > , BELOW.
0350 LOPA: IN PORTC
0360 ANI 20H ; BIT 5
0370 JZ LOPA ; WAIT FOR EVENT PULSE
0380 *
0390 * READ MILLISECOND COUNT SINCE LAST EVENT
0400 * AND SAVE IN DE FOR COMPUTING EVENTS PER MINUTE.
0410 *
0420 IN PORTB ; MSB'S
0430 MOV D,A
0440 IN PORTA ; LSB'S
0450 MOV E,A
0460 *E

```

Figure 8. Annotated source listing of cardiometer program

```

0470 * COMPUTE BEATS PER MINUTE..
0480 * NUMBER OF MILLISECONDS PER MINUTE (60,000) DIVIDED BY
0490 * NUMBER OF MILLISECONDS PER EVENT INTERVAL
0500 * ( I.E. NO. OF MSEC. COUNTS PER INTERVAL)
0510 * GIVES NUMBER OF EVENTS PER MINUTE.
0520 *
0530     LXI     B,60000
0540     CALL    DIV      ; OBTAIN QUOTIENT IN BC
0550     MOV     D,B      ; MOVE TO DE
0560     MOV     E,C
0570 *
0580     LXI     H,NUM1   ; SET NUMERAL BUFFER
0590     CALL    BNBCD
0600 *
0610     MVI     A,80H   ; SET MODE 0, ALL OUTPUT
0620     OUT     CNTRL
0630     MVI     A,0
0640     OUT     PORTC   ; DISABLE COUNTER BUFFERS.
0650 *
0660     LDA     NUM3
0670     ANI     0FH
0680     MOV     B,A
0690     LDA     NUM4
0700     RLC
0710     RLC
0720     RLC
0730     RLC
0740     ANI     0F0H
0750     ORA     B      ; PACK FIRST 2 DIGITS
0760     OUT     PORTA
0770     LDA     NUM5
0780     OUT     PORTB
0790 *
0800     MVI     A,40H   ; ENABLE LED'S
0810     OUT     PORTC
0820     MVI     A,0     ; DISABLE LED'S
0830     OUT     PORTC
0840 *
0850     JMP     LOOP
0860 *E

```

Figure 8. Continued

```

0870 * 16-BIT DIVIDE ROUTINE
0880 * ENTER WITH DIVIDEND IN BC, DIVISOR IN DE
0890 * EXIT WITH QUOTIENT IN BC
0900 * IGNORE REMAINDER.
0910 *
0920 DIV    MOV    A,D
0930        CMA
0940        MOV    D,A
0950        MOV    A,E
0960        CMA
0970        MOV    E,A
0980        INX    D
0990        LXI    H,0
1000        MVI    A,17
1010 DV0    PUSH   H
1020        DAD    D
1030        JNC    DVI
1040        XTHL
1050 DVI    POP    H
1060        PUSH  PSW
1070        MOV    A,C
1080        RAL
1090        MOV    C,A
1100        MOV    A,B
1110        RAL
1120        MOV    B,A
1130        MOV    A,L
1140        RAL
1150        MOV    L,A
1160        MOV    A,H
1170        RAL
1180        MOV    H,A
1190        POP    PSW
1200        DCR    A
1210        JNZ    DV0
1220        RET
1230 *E

```

Figure 8. Continued

```

1240 * CONVERT BINARY TO BCD
1250 * ENTER WITH ADDRESS OF STORAGE AREA IN HL
1260 * AND BINARY VALUE IN DE
1270 *
1280 BNBCD  PUSH  PSW
1290        PUSH  B
1300        PUSH  D
1310        PUSH  H
1320        XCHG
1330        LXI   B,-10000
1340        CALL  DECNO
1350        LXI   B,-1000
1360        CALL  DECNO
1370        LXI   B,-100
1380        CALL  DECNO
1390        LXI   B,-10
1400        CALL  DECNO
1410        MOV   A,L
1420        STAX  D
1430        POP   H
1440        POP   D
1450        POP   B
1460        POP   PSW
1470        RET
1480 *
1490 DECNO  XRA   A
1500        PUSH  D
1510        MOV   E,L
1520        MOV   D,H
1530        INR   A
1540        DAD   B
1550        JC    DECNO+2
1560        DCR   A
1570        MOV   L,E
1580        MOV   H,D
1590        POP   D
1600        STAX  D
1610        INX   D
1620        RET
1630 *
1640 TIP    EQU   $      ; END OF ROM AREA
1650        COM   TIP
1660 *E

```

Figure 8. Continued


```

0000: F3 31 25 04 3E 80 D3 03 3E 80 D3 02 3E BF D3 03
0010: DB 02 E6 20 CA 10 00 DB 01 57 DB 00 5F 01 60 EA
0020: CD 55 00 50 59 21 00 04 CD 7B 00 3E 80 D3 03 3E
0030: 00 D3 02 3A 02 04 E6 0F 47 3A 03 04 07 07 07 07
0040: E6 F0 80 D3 00 3A 04 04 D3 01 3E 40 D3 02 3E 00
0050: D3 02 C3 00 00 7A 2F 57 7B 2F 5F 13 21 00 00 3E
0060: 11 E5 19 D2 67 00 E3 E1 F5 79 17 4F 78 17 47 7D
0070: 17 6F 7C 17 67 F1 3D C2 61 00 C9 F5 C5 D5 E5 EB
0080: 01 F0 D8 CD 9F 00 01 18 FC CD 9F 00 01 9C FF CD
0090: 9F 00 01 F6 FF CD 9F 00 7D 12 E1 D1 C1 F1 C9 AF
00A0: D5 5D 54 3C 09 DA A1 00 3D 6B 62 D1 12 13 C9

```

Figure 9. Hexadecimal readout of the assembled program

CONCLUSIONS

The microprocessor based cardiometer described here has proved to be very accurate (due to its crystal controlled time base) and extremely reliable, with no failures or tendency to instability after extensive bench testing. It requires no calibration, and in packaged form would be expected to operate without problems indefinitely. Changes and improvements, such as adding a digital to analog converter to provide a signal for driving a chart recorder, become immediately obvious. Using a microprocessor as the basis for any instrument makes it possible to add large complexity in behavior with relatively small changes in hardware.

As the project progressed, the nature and operation of each of the circuit elements became increasingly familiar. The 8255 programmable peripheral interface was particularly confusing however, and the Intel 8255A Application Note AP-15 in addition to the Intel Systems Users Manual was required. The experience gained with this instrument has provided a great confidence in the use of microprocessor elements as integral parts of any instrumentation of control system.

APPENDIX A

Cartest 2 Program

The following listing is a test program called CARTEST2 implemented on a UV PROM used to check out the microprocessor system hardware for improper operation. First, the number 124 is displayed. Then all digits are zeroed. Next, each digit in turn, displays the count from zero to nine.

```

0010 * 7JUL78 1300
0020 * CARIES12.A
0030 * CARDIOTACHOMETER TEST ROUTINE
0040 *
0050 * MEMORY ASSIGNMENTS
0060 ROM EQU 0
0070 RAM EQU 400H
0080 *
0090 * PORT ASSIGNMENTS
0100 PORTA EQU 0
0110 PORTE EQU PORTA+1
0120 PORTC EQU PORTA+2
0130 CNTRL EQU PORTA+3 ; CONTROL PORT
0140 *
0150 Psw EQU 6
0160 SP EQU 6
0170 *
0180 ORG ROM
0190 *
0200 LOOP: DI ; DISABLE INTERRUPTS
0210 LXI SP,STACK ; RESET STACK POINTER
0220 *
0230 MVI A,80H ; SET MODE 0, ALL OUTPUT
0240 OUT CNTRL
0250 *
0260 MVI A,21H
0270 OUT PORTA
0280 MVI A,4
0290 OUT PORTB
0300 *
0310 CALL STROB
0320 CALL DLY
0330 CALL DLY
0340 CALL DLY
0350 *
0360 MVI A,0
0370 OUT PORTA
0380 OUT PORTB
0390 CALL DLY
0400 *
0410 MVI B,10
0420 MVI C,0
0430 LOP1: CALL DLY
0440 MOV A,C
0450 OUT PORTA
0460 CALL STROB

```

```

0470      INR      C
0480      DCR      B
0490      JNZ      LOP1
0500 *E
0510      MVI      B,10
0520      MVI      C,0
0530 LOP2:  CALL    DLY
0540      MOV      A,C
0550      RLC
0560      RLC
0570      RLC
0580      RLC
0590      OUT      PORTA
0600      CALL    STROB
0610      INR      C
0620      DCR      B
0630      JNZ      LOP2
0640 *
0650      MVI      B,10
0660      MVI      C,0
0670 LOP3:  CALL    DLY
0680      MOV      A,C
0690      OUT      PORTB
0700      CALL    STROB
0710      INR      C
0720      DCR      B
0730      JNZ      LOP3
0740 *
0750      JMP      LOOP
0760 *
0770 *
0780 STROB: MVI      A,40H ; ENABLE LED'S
0790      OUT      PORTC
0800      MVI      A,80H
0810      OUT      PORTC ; DISABLE LED'S, ENABLE COUNT BUFFERS.
0820      RET
0830 *
0840 * DELAY 1 SECOND
0850 DLY:   LXI      H,1000
0860      PUSH    PSW
0870 DLY0:  DCR      H
0880      MVI      A,132
0890 DLY1:  DCR      A
0900      JNZ      DLY1
0910      MOV      A,H
0920      ORA      L
0930      JNZ      DLY0
0940      POP     PSW
0950      RET
0960 *
0970 TIP   EQU     3
0980      CUM     TIP
0990 *
1000 * RAM AREA
1010      ORG     RAM

```

1020 DS 20H
1030 STACK: LW 0
1040 *E
1050 *

ATTACH 3

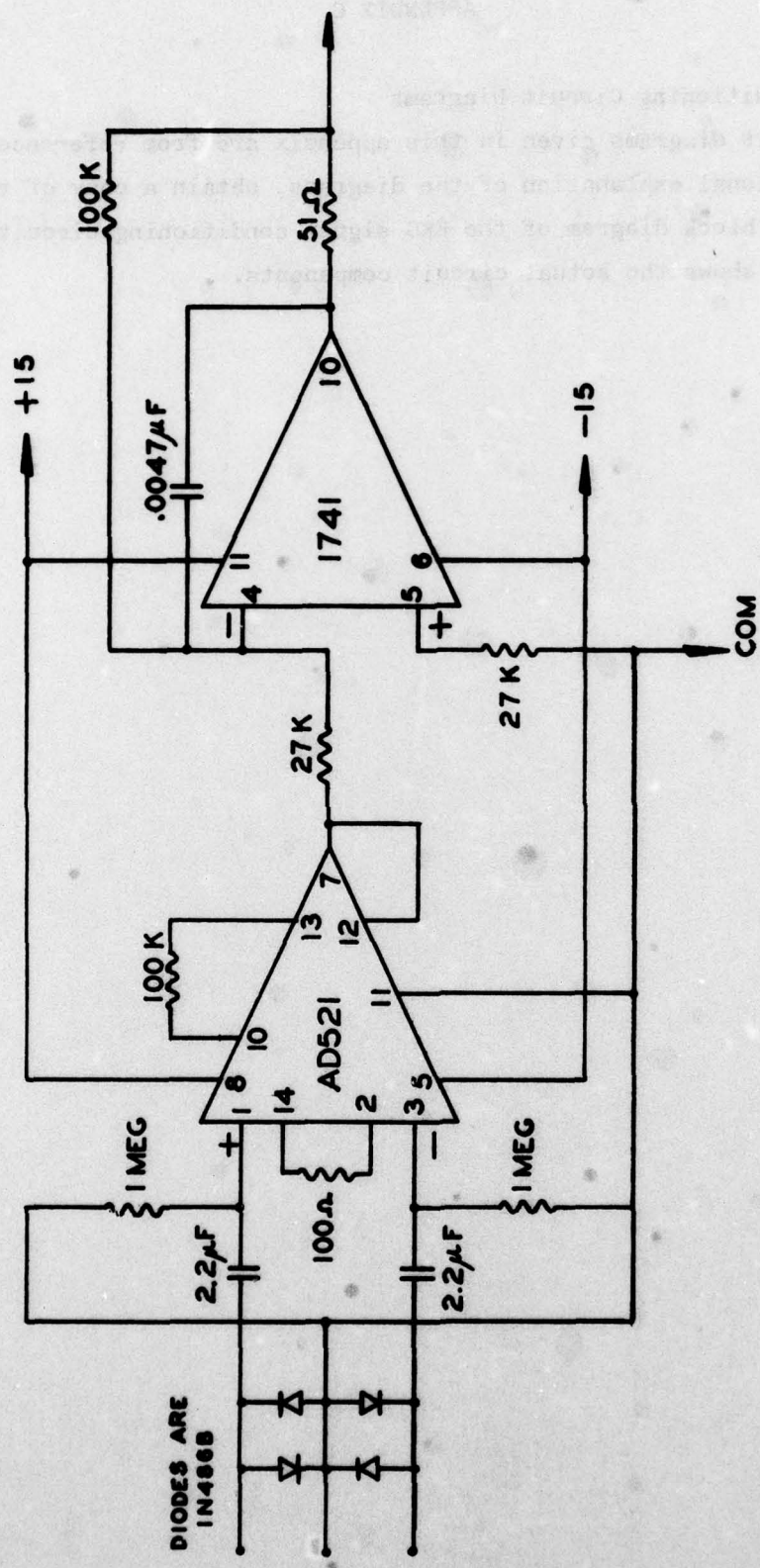
Electrostatic Amplifier

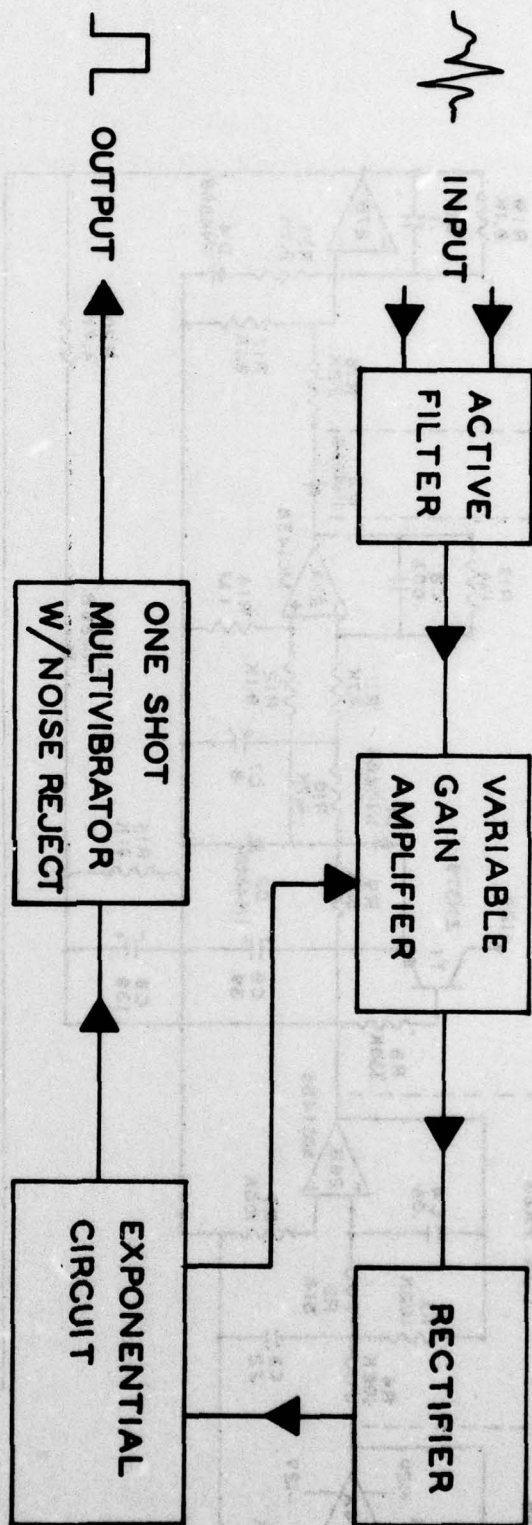
An electrostatic amplifier that can be used to obtain an output
the amplifier is given below. Circuitry is the courtesy of Mr. Dennis
McIntyre, Raytheon Service Company.

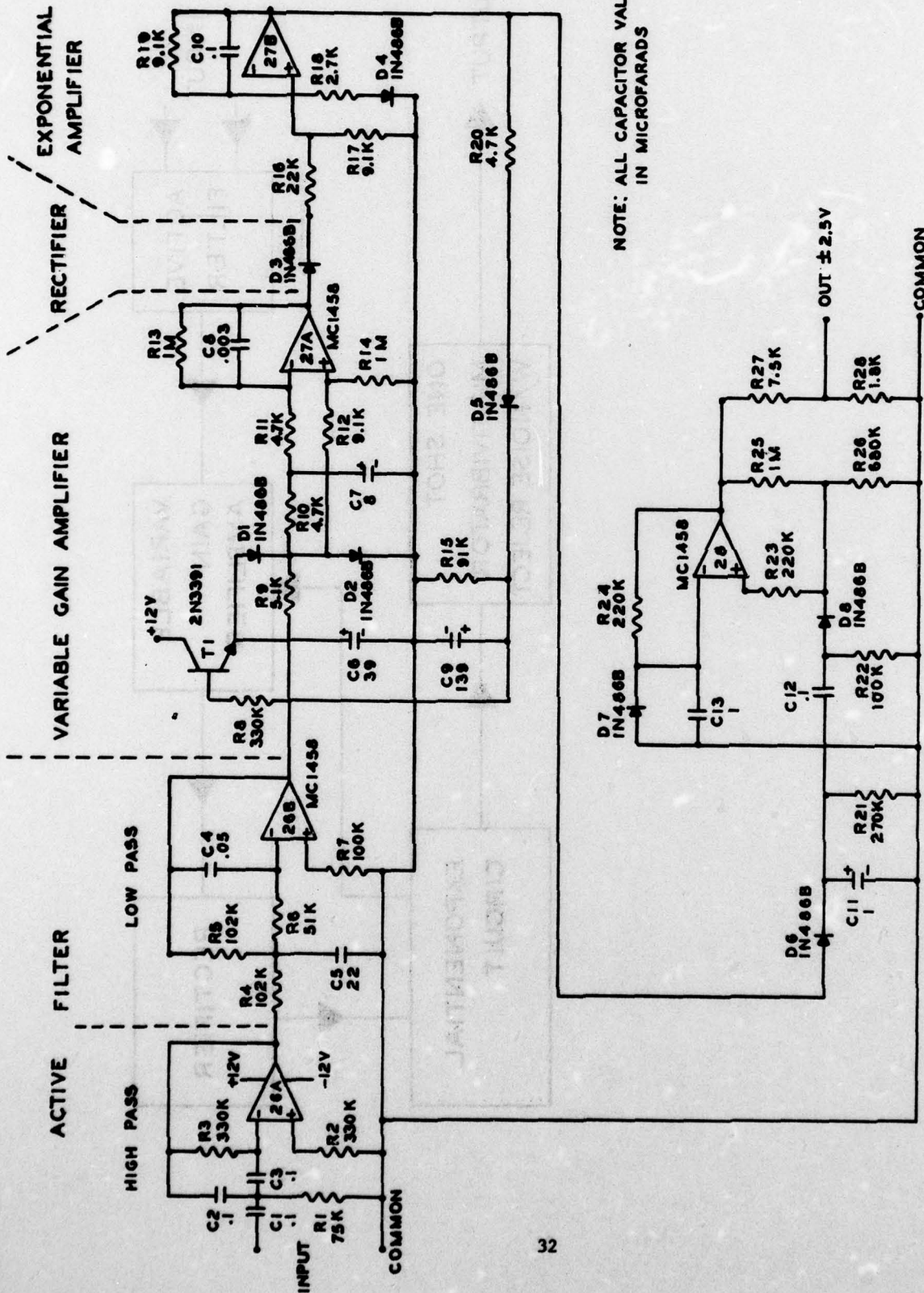
APPENDIX B

Electrocardiogram Amplifier

An electrocardiogram amplifier that can be used to obtain an EKG input for the cardiometer is given below. Circuitry is the courtesy of Mr. Donald McCollor, Raytheon Service Company.







NOTE: ALL CAPACITOR VALUES IN MICROFARADS

ONE SHOT MULTIVIBRATOR WITH NOISE REJECTION UNIT

REFERENCES

Marko, Adolf R., et al., An Improved Cardiometer Input Circuit for Heart Rate Determination, AMRL-TR-73-50, Wright Patterson Air Force Base, Ohio, September 1973.