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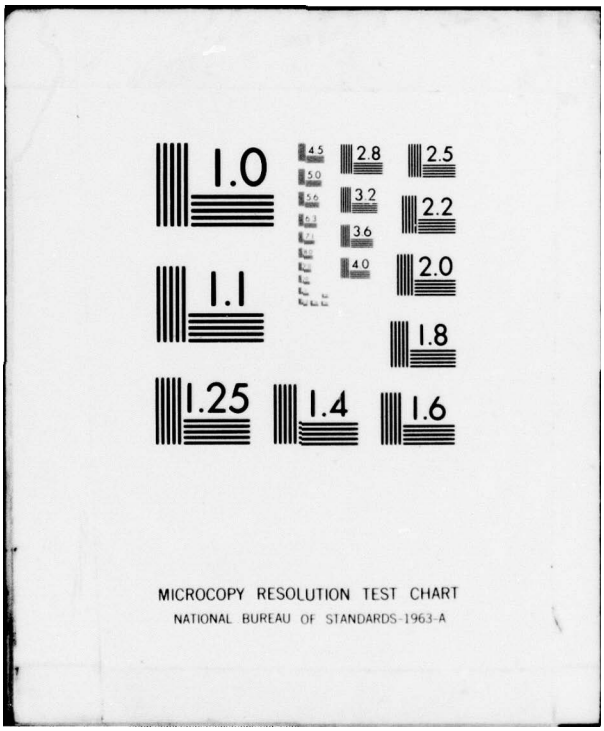
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by

(10) Clyde Musgrave

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The Satellite Signal Analyzer (S.S.A.) being designed and constructed by students in the Satellite Communications Laboratory of the Naval Postgraduate School will provide Real Time Spectrum Analysis of Communication Satellite UHF Signals. This thesis documents the digital control and test unit subsystems of this S.S.A. The digital control subsystem was designed and built to interface the PDP 11/34 MINICOMPUTER to all digitally controlled devices within the system. The control bus (CIB) provides 32 BITS

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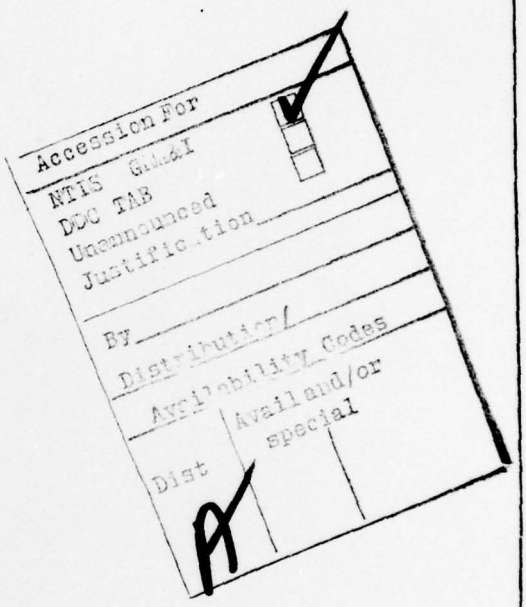

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DESIGN OF THE DIGITAL CONTROL AND TEST UNIT SUBSYSTEMS FOR A SATELLITE SIGNAL ANALYZER

by

Clyde Musgrave
Lieutenant, United States Navy
B.S.E.E., University of Nebraska, 1972

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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June 1979

Author C Musgrave

Approved by: John E Olson
Thesis Advisor

Milton L Wilcox
Second Reader

W E Kirk
Chairman, Department of Electrical Engineering

William M Tolles
Dean of Science and Engineering

ABSTRACT

The Satellite Signal Analyzer (S.S.A.) being designed and constructed by students in the Satellite Communications Laboratory of the Naval Postgraduate School will provide Real Time Spectrum Analysis of Communication Satellite UHF Signals. This thesis documents the digital control and test unit subsystems of this S.S.A. The digital control subsystem was designed and built to interface the PDP 11/34 MINICOMPUTER to all digitally controlled devices within the system. The control bus (CIB) provides 32 BITS of digital control on a single board. The TEST UNIT subsystem was designed and built to provide the capability to monitor various signals within the S.S.A. as well as conduct self-checks. The TEST UNIT is capable of measuring the Noise Figure/Temperature of the system receivers, monitoring the level and frequency of system signals, injecting signals into the receivers and transmitting signals to satellites.

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LIST OF ABBREVIATIONS

ADC	ANALOG-TO-DIGITAL CONVERSION
BIT	SINGLE DIGITAL INFORMATION
BPF	BANDPASS FILTER
BYTE	EIGHT BITS
CIB	CONTROL INTERFACE BOARD
CW	CONTINUOUS WAVE
dB	DECIBELS
dBm	DECIBELS REFERENCED TO 1 MILLIWATT
DIP	DUAL-IN-LINE PACKAGE
DMA	DIRECT MEMORY ACCESS
FFT	FAST FOURIER TRANSFORM
FLTSAT	FLEET SATELLITE
GAP	GAPFILLER SATELLITE
GND	GROUND
HP	HEWLETT PACKARD
HPA	HIGH POWER AMPLIFIER
IEEE	INSTITUTE OF ELECTRONIC AND ELECTRICAL ENGINEERS
IF	INTERMEDIATE FREQUENCY
I/O	INPUT/OUTPUT
LED	LIGHT EMITTING DIODE
LSB	LEAST SIGNIFICANT BIT
LSD	LEAST SIGNIFICANT DIGIT
MAX	MAXIMUM
MLS	MAXIMUM LENGTH SEQUENCE
MSB	MOST SIGNIFICANT BIT
MSD	MOST SIGNIFICANT DIGIT

NDR	NEW DATA READY
PRS	PSEUDO RANDOM SEQUENCE (MLS=PRS)
PSK	PHASE SHIFT KEYING
NAVELEX	NAVAL ELECTRONIC SYSTEMS COMMAND
NAVPGSCOL	NAVAL POSTGRADUATE SCHOOL
NC	NOT CONNECTED
PROM	PROGRAMMABLE READ-ONLY-MEMORY
R.F.	RADIO FREQUENCY
R.F.I.	RADIO FREQUENCY INTERFERENCE
SATCOM	SATELLITE COMMUNICATIONS
SIPO	SERIAL IN/PARALLEL OUT
SSA	SATELLITE SIGNAL ANALYZER
TTL	TRANSISTOR-TRANSISTOR LOGIC
XMT	TRANSMIT
XMTR	TRANSMITTER
XSITION	TRANSITION

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I. INTRODUCTION

A. BACKGROUND

The present Satellite Signal Analyzer project, funded by PME 106-1 of the Naval Electronic Systems Command (NAVELEX), is the prototype version of a similar system which was constructed from March 1977 until September 1978. The purpose of both was and is to provide "real-time" spectrum analysis of all the U.H.F. signals eminating from U. S. Navy satellite transponders.

B. S.S.A.

The S.S.A. will be an automatic spectrum analysis system capable of displaying, simultaneously, nine channels of FLTSAT on one video terminal, a wide band GAPFILLER channel, an enlarged version of a single FLTSAT channel, a "waterfall" time domain presentation display of one channel, or various other displays which the operator may select.

Figure 1.1 represents the block diagram of the S.S.A. presently being designed and constructed. Received satellite signals enter the S.S.A. at either QUAD OE-82A Antennas or the single OE-82A antenna and are coupled thru the identical RF UNITS 1, 2, & 3. The SIGNAL SELECTION UNIT is basically a routing network which provides the appropriate signals to the proper equipment. The received satellite signal proceeds, for processing, into the Spectrum Receivers (4 each) where it is down converted and exists in the S.S.A. as an analog signal

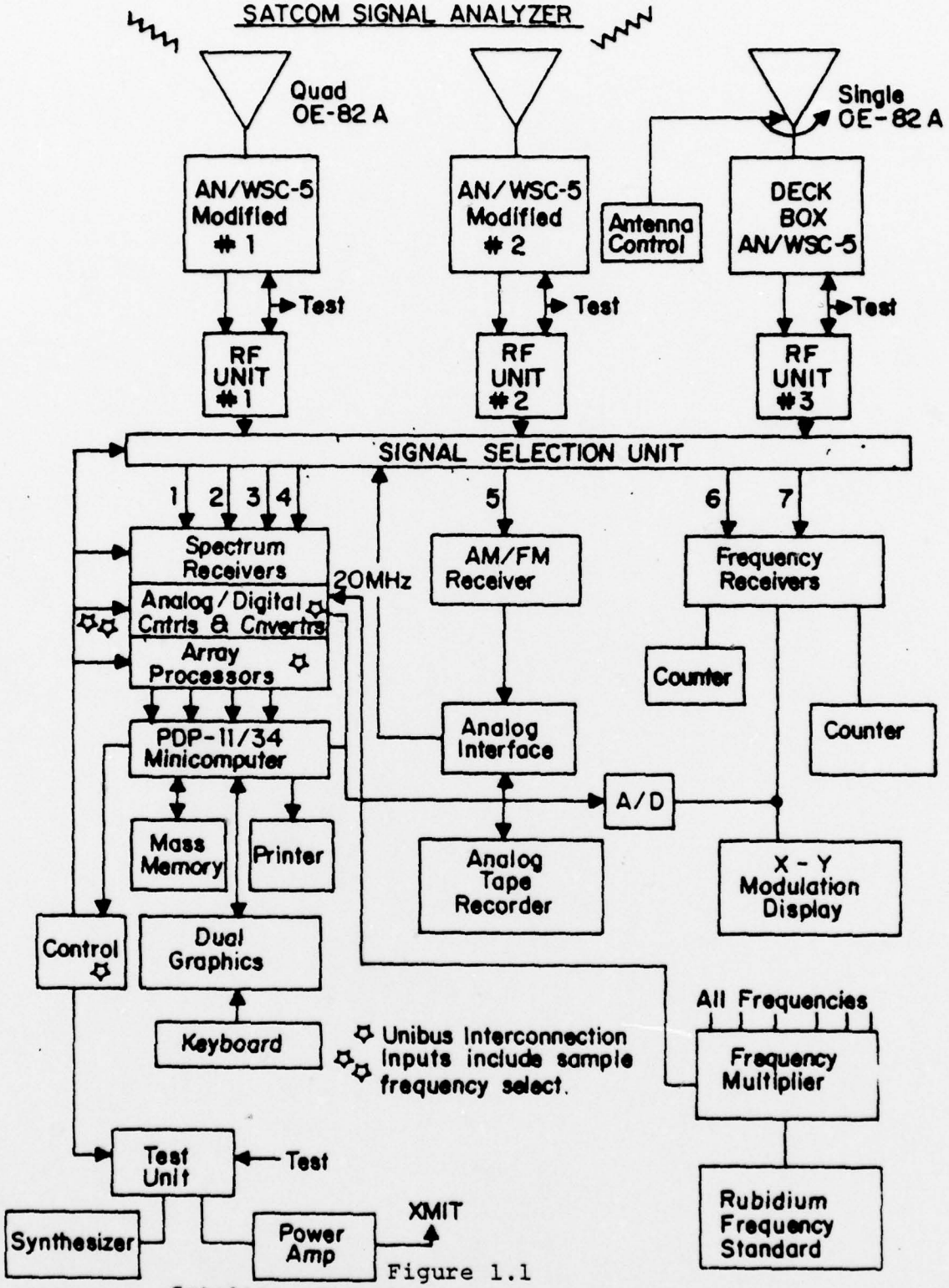

Figure 1.1
Satellite Signal Analyzer Block Diagram

for the final time. This analog signal is converted to a digital signal using the ADC boards designed and built in the Satellite Communications Lab [1].

This digital signal is sent to the SP400 ANALOGIC Array Processor in order to convert the digital time signal into a discrete frequency or spectral signal by taking the Fast Fourier Transform (FFT). The AP400 is capable of doint this without the intervention of the MINICOMPUTER PDP 11/34 manufactured by Digital Equipment Corporation. At the completion of the FFT, the AP400 does a DMA transfer into the memory of the PDP 11/34. The PDP 11/34, therefore, is free to accomplish multiple tasks such as control, display, system status monitoring and response, etc. until the AP400 is prepared to transfer information about the received satellite signal frequency components.

The remainder of the system is designed to support the previously discussed components or add additional capabilities not related to the basic function of spectrum analysis and will not be discussed here, with the exception of the Digital Control Subsystem and the Test Unit Subsystem.

C. DIGITAL CONTROL BUS

The PDP 11/34, a 16-BIT minicomputer, will be accomplishing such functions as digital control of various devices (e.g. ROCKLAND SYNTHESIZERS) when not involved in a D.M.A. of data from the AP400. The ROCKLAND synthesizers (5610A) are digitally (ACTIVE-LOW or NEGATIVE TRUE LOGIC) programmable, but require 32 BITS of data to specify the output frequency

(.1 - 159.999999 MHz) of ± 1Hz. An obvious need existed to interface the 16 BIT PDP 11/34 minicomputer to the right 32 BIT 5610A synthesizer. In addition, the Control Interface Board (CIB) must be capable of controlling all other devices which are digitally probrammable and it must be a single board, capable of being interchanged with other CIB's, regardless of the device to which it is connected.

The following, from Figure 1.1, are those devices which are digitally programmable and will be connected to the CIB:

1. TEST UNIT
2. RF UNITS 1, 2, and 3
3. SIGNAL SELECTION UNIT
4. SPECTRUM RECEIVERS
5. AN/FM RECEIVER
6. FREQUENCY RECEIVER
7. ANALOG/DIGITAL CONTROL AND CONVERTERS
8. FREQUENCY SYNTHESIZERS

D. TEST UNIT

The S.S.A. system will be capable of analyzing satellite signals with power levels in the range of -150 to -85 dBm. The test unit includes not only various manually selected self tests such as spectrum analysis of received signals and IF signals, but also a test transmitter for making roundtrip measurements on satellite signals and the capability to modulate this signal with a pseudo-random sequence.

II. DIGITAL CONTROL BUS

A. DESCRIPTION

In order for the PDP 11/34 (16 BIT minicomputer) to accurately and easily control the eight ROCKLAND 5610A synthesizers, as well as all the other devices necessary, the CONTROL INTERFACE BOARD was designed and constructed (ONE CIB for each device).

B. PDP 11/34 DR11C OUTPUT

The parallel INPUT/OUTPUT (I/O) board of the PDP 11/34 is the DR11C. It provides one 16 BIT INPUT AND OUTPUT port as well as one 16 BIT output only port. Since the PDP 11/34 has memory mapped I/O, it merely transfers information from one location in memory to the DR11C location o- vice versa when communicating with devices external (I/O) to the PDP 11/34. A strobe (or clock pulse), called NEW DATA READY (NDR), is also provided to indicate to external devices that new data is latched on the output lines. Each output line of the DR11C is capable of driving only 10 TTL loads. Table I shows some of the CIB specifications.

C. ROCKLAND SYNTHESIZER (5610A)

The ROCKLAND MODEL 5610A FREQUENCY SYNTHESIZER is a precision frequency generator capable of producing signals from 100 KHz to 159.999999 MHz with a +3 to +13 dBm leveled output into a 50Ω load.

TABLE I

CIB SPECIFICATIONS

DATA SOURCE	PDP 11/34 DR11C (Parallel I/O Board) 16 BITS
DATA LINES	POSITIVE TRUE LOGIC BYTE ORGANIZED
CONNECTED TO:	CIB DRIVER BOARD CONTROL INTERFACE BOARD D7 - D0 = DATA BITS S3 - S0 = DEVICE SELECT BITS A1, A0 = BYTE SELECT BITS NDR = NEW DATA READY
CONTROL BUS PACKAGE:	PRO LOG STANDARD BUS 7000 SERIES CR16 ONE HALF RACK
CIB	32 BITS OUT POSITIVE TRUE LOGIC BYTE ORGANIZED

	BCDWEIGHT			
	1	2	4	8
10MHz	15	16	40	41
1MHz	17	18	19	20
100KHz	1	2	26	27
10KHz	3	4	28	29
1KHz	5	6	30	31
100Hz	7	8	32	33
10Hz	9	10	34	35
1Hz	11	12	36	37

NUMBERS = REMOTE FREQUENCY CONNECTOR PINS

LOGICAL ONE = GROUND

LOGICAL ZERO = +5V

Figure 2.1

ROCKLAND SYNTHESIZER Remote Frequency Control

Remote frequency control is available by applying the appropriate "logical ones" and "logical zeros" to the correct pins of the remote frequency control connector. Figure 2.1 shows the correct pin connections for remotely programming a desired frequency, however the programming will be discussed later.

D. OPERATION OF THE CONTROL INTERFACE BOARD

In view of the fact that the PDP 11/34 DR11C output can drive only 10 TTL loads, a driver board was designed and constructed to provide (1) the capability to drive more than 10 devices and (2) the ability of the operator to visually inspect the DR11C information being sent to the CIB. Figure 2.2 shows the schematic of the DRIVER BOARD. Information from the DR11C enters the DRIVER BOARD at the PDP 11/34 out pins (at the right) and goes thru two inversions prior to reaching the CONTROL BUS. The 3.3KΩ resistors on the output of the 2nd inverter are pull-up resistors required for the 7416 inverters open collector output devices). The 3.3KΩ resistors on the input will be needed for the COMPUTER SIMULATOR TEST BOARD to be discussed later. The 7416 INVERTING HEX DRIVER is capable of sinking 40ma (i.e., a low state). Since each regular TTL input needs to sink 1.6ma [2], the 7416 is able to sink current for 25 TTL loads per line. The LED will draw approximately 10.5ma on each line and the pull-up resistor will draw approximately 1.5ma on each line for a low condition (i.e., 12ma total for a low condition). This means the 12ma is approximately 7.5 TTL loads leaving 17.5 TTL loads

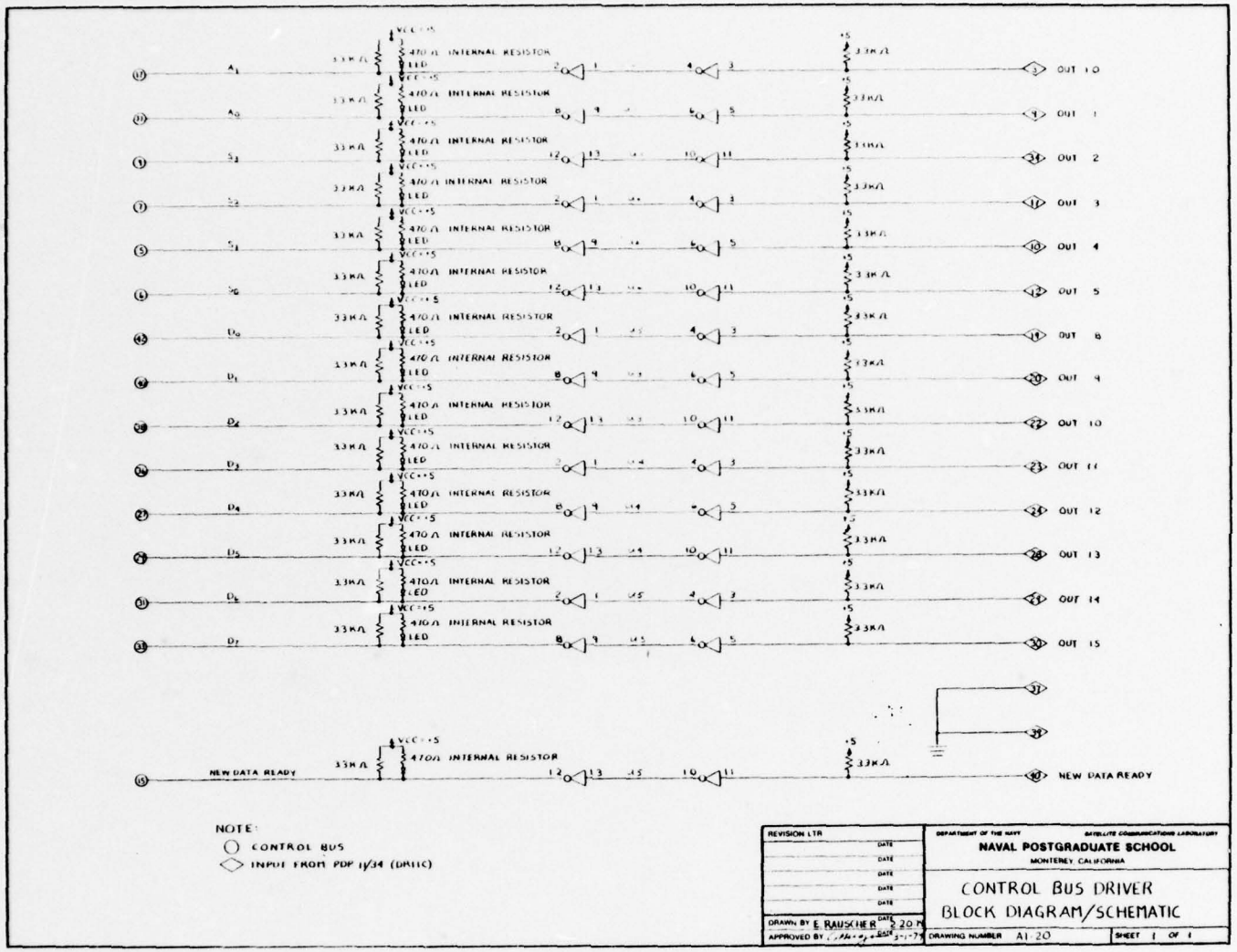

Figure 2.2
CIB Driver Board Schematic

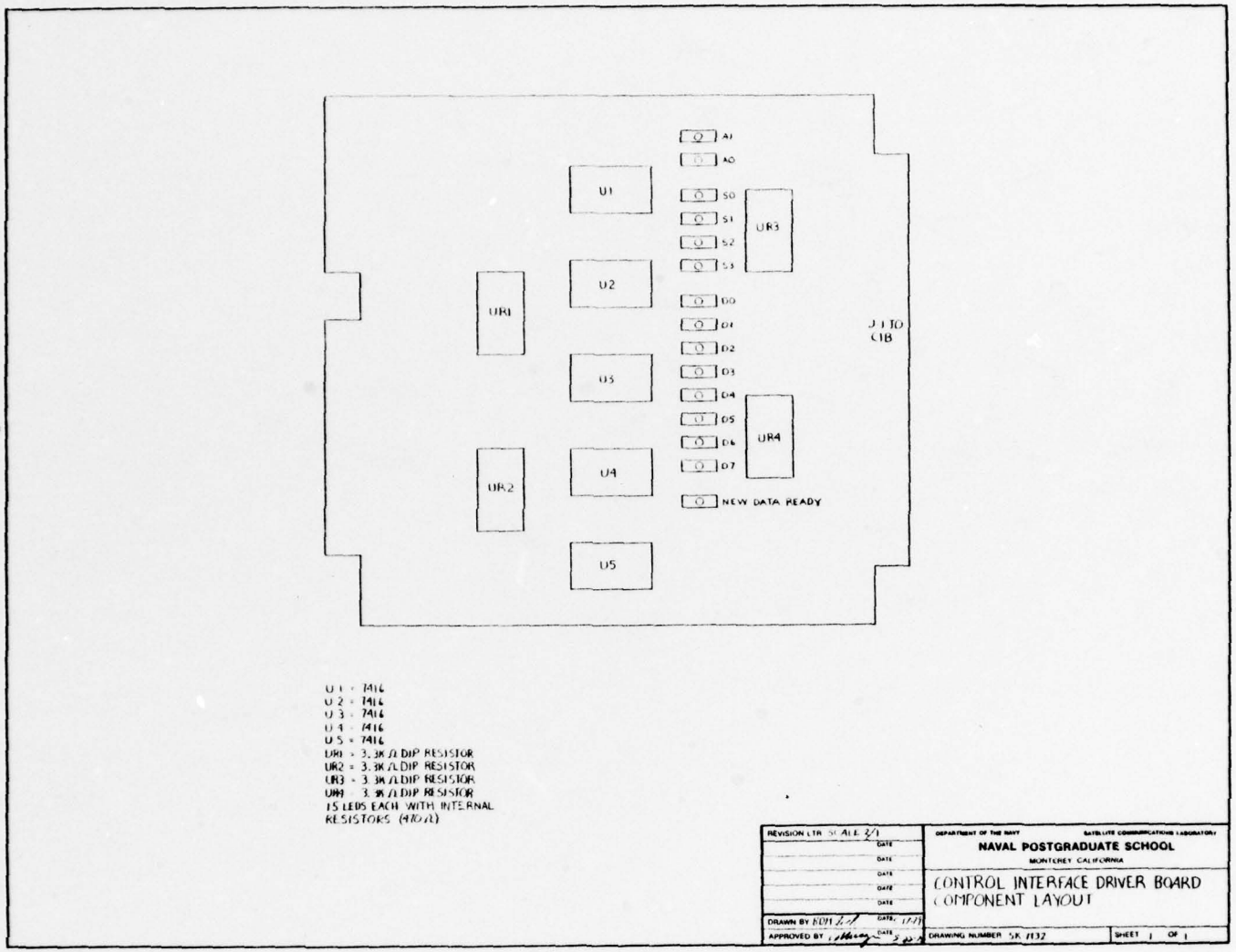

Figure 2.3
Control Interface Driver Board Component Layout

for which the second inverter can sink current. The CONTROL INTERFACE BOARDS, to be discussed shortly, are packaged in a STANDARD BUS 7000 SERIES CR 16 MOTHERBOARD ONE HALF RACK (manufactured by PRO-LOG CORP.). This rack has slots for only 16 boards total, with one slot taken by the DRIVER BOARD. Therefore, by confining the CONTROL BUS to one TTL load per line per board, the DRIVER BOARD is capable of providing the current requried. Figure 2.3 shows the physical layout of the parts on the CIB DRIVER BOARD.

The CONTROL INTERFACE BOARD now has 16 BITS plus the NEW DATA READY pulse from the PDP 11/34 DR11C and must convert them to 32 BITS for the ROCKLAND SYNTHESIZER and must hold or latch the 32 BITS to prevent the synthsizer from an undesired frequency change. The 16 BITS from the DR11C (only 14 of which are used (Figure 2.2) are organized in the following way, eight BITS for data to a device (DATA BYTE), four BITS for board selection (BOARD or DEVICE SELECT), and two BITS for selecting to which device pins the data is routed (BYTE SELECT). This bit organization will be discussed in greater detail later. The eight data BITS (D7=MSB THRU D0=LSB), Figure 2.4, are applied to U3 (74116 DUAL 4 BIT LATCH) thus ensuring only 15 TTL loads on each of these lines (one TTL local per line per board). This latch acts merely as a driver for U4, U5, and U7. Because the enables of U3 are tied to ground, the data on the input pins 22, 20, 18, 16, 10, 8, 6, and 4 goes immediately to the output pins of U3, 23, 21, 19, 17, 11, 9, 7, and 5 and is made available to the

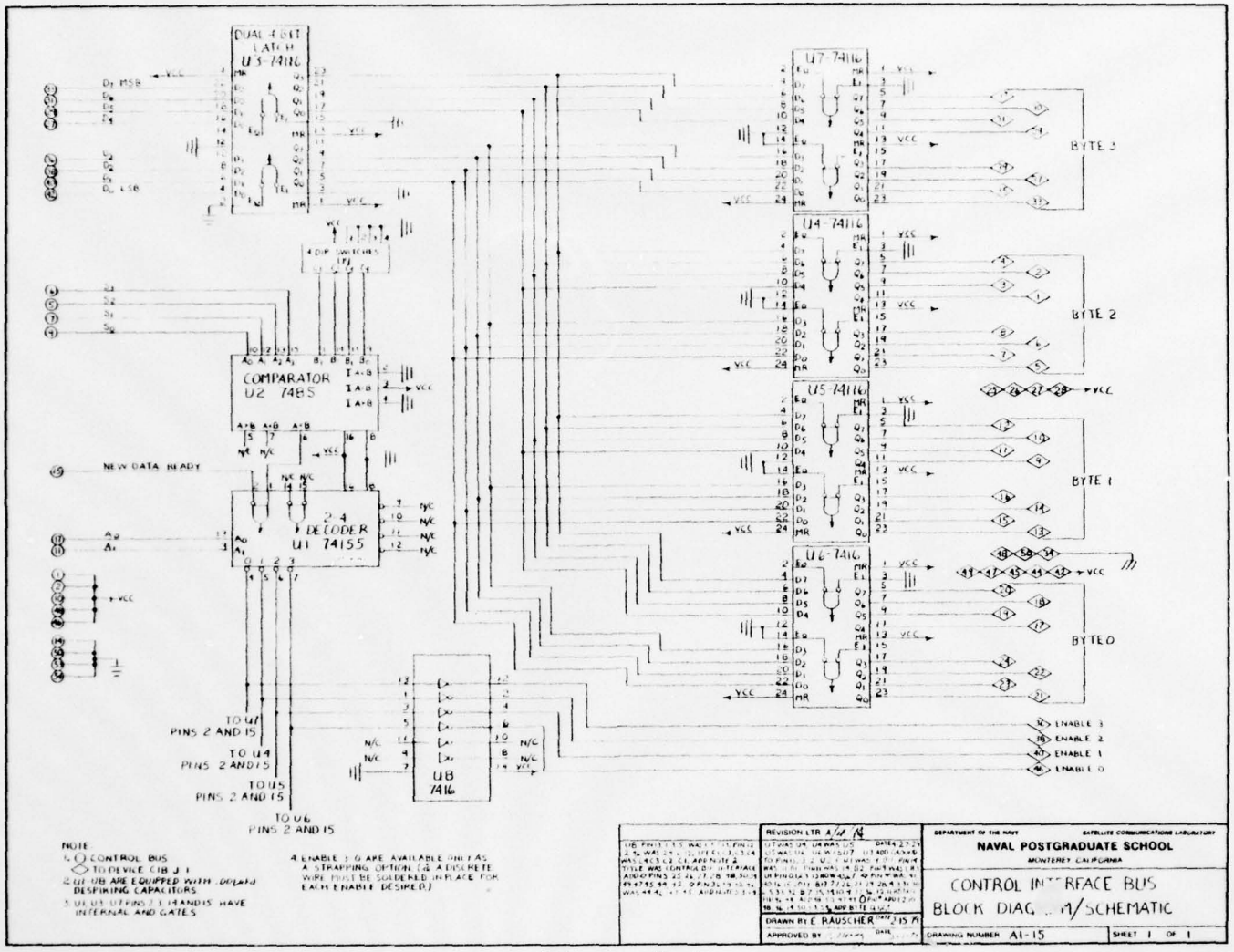

Figure 2.4
CONTROL INTERFACE BUS SCHEMATIC

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input pins of U4, U5, U6, and U7. The four BOARD SELECT BITS (S3, S2, S1, S0) determine the device to be controlled. One board equals one device unless more than 32 BITS of control are needed for a device (e.g., SIGNAL SELECTION UNIT). The four BOARD/DEVICE SELECT BITS (S3=MSB, S2, S1, S0=LSB) applied to pins 15, 13, 12, 10 of U2-7485 (comparator) are compared with the four bits on pins 1, 14, 11, 9 and if S_3, S_1, S_0 equal B_3, B_2, B_1, B_0 from the DIPSWITCH (DEVICE ADDRESS or BOARD ADDRESS) then the A=B output of U-2 goes from negative-to-positive. The 2 Bits (A_0=LSB, A_1=MSB) for selecting the device pins to which data is routed are applied to U1-74155 DECODER pins 13 and 3. NEW DATA READY is a positive-to-negative going pulse which strobes the decoder to produce a positive-to-negative strobe of U1 pins 4, 5, 6, or 7 depending upon the digital value on A_0 and A_1. Three factors must occur before the DECODER U1 puts a strobe out (1) the PDP 11/34 DR11C must have sent 14 BITS thru the DRIVER BOARD to the CONTROL BUS and (2) the COMPARATOR must have $S_3=B_3$, $S_2=B_2$, $S_1=B_1$, $S_0=B_0$ and as a result mush have made U1 pin 1 go positive and (3) the new data ready pulse must arrive. It should be noted, if the COMPATATOR does not recognize a match (i.e., $S_3\neq B_3$ or $S_2\neq B_2$ or $S_1\neq B_1$ or $S_0\neq B_0$ or all of these) then no strobe is applied to any of the latches U4, U5, U6, U7 and no data is latched into the devices, regardless of any other signals. The decoder U1 now makes either pin 4, 5, 6, or 7 go from positive-to-negative in one of the four following ways: (1) if A_1=1 and A_0=0, then U1 PIN 4 goes negative;

(2) if A_1=1 and A_0=0, then U1 PIN 5 goes negative; (3) if A_1=0 and A_0=1, the U1 PIN 6 goes negative; and (4) if A_1=0 and A_0=0, the U1 PIN 7 goes negative. By making one of those four pins go negative, one of the DUAL 4 BIT LATCH ENABLE lines are strobed. The strobing of U7 pins 2 and 15, for example, will cause the data on the input pins of U7 to be "LATCHED" into U7 and be applied to pins 32, 31, 30, 29, 39, 37, 35, and 33 of the connector to which the device is connected. In the case of a ROCKLAND SYNTHESIZER the 10MHz and 1MHz DIGITS would be changed. One will note the difference in pin numbers on Figure 2.1 for the ROCKLAND SYNTHESIZER and the pin numbers on the OUTPUT of EACH LATCH U4, U5, U6, and U7 (Figure 2.4). This was necessary due to the various numbering schemes on the connectors utilized. One strobe (enable 0,1,2,3) for each byte of control was provided for use if the device is not a ROCKLAND SYNTHESIZER but requires a strobe to indicate to a device to accept new data. The PINS 12, 2, 4 and 6 of U8 are not connected to PINS 36, 38, 40 and 46 of the output connector J1 but must have a discrete wire (jumper) to connect them together. In addition the pins 12, 2, 4 and 6 of U8 will require discrete pull-up resistors to +5V because U8-7416 has an open-collector output as previously mentioned in the C.I.B. DRIVER BOARD. Figure 2.5 shows the physical layout of all components on the CONTROL INTERFACE BOARD.

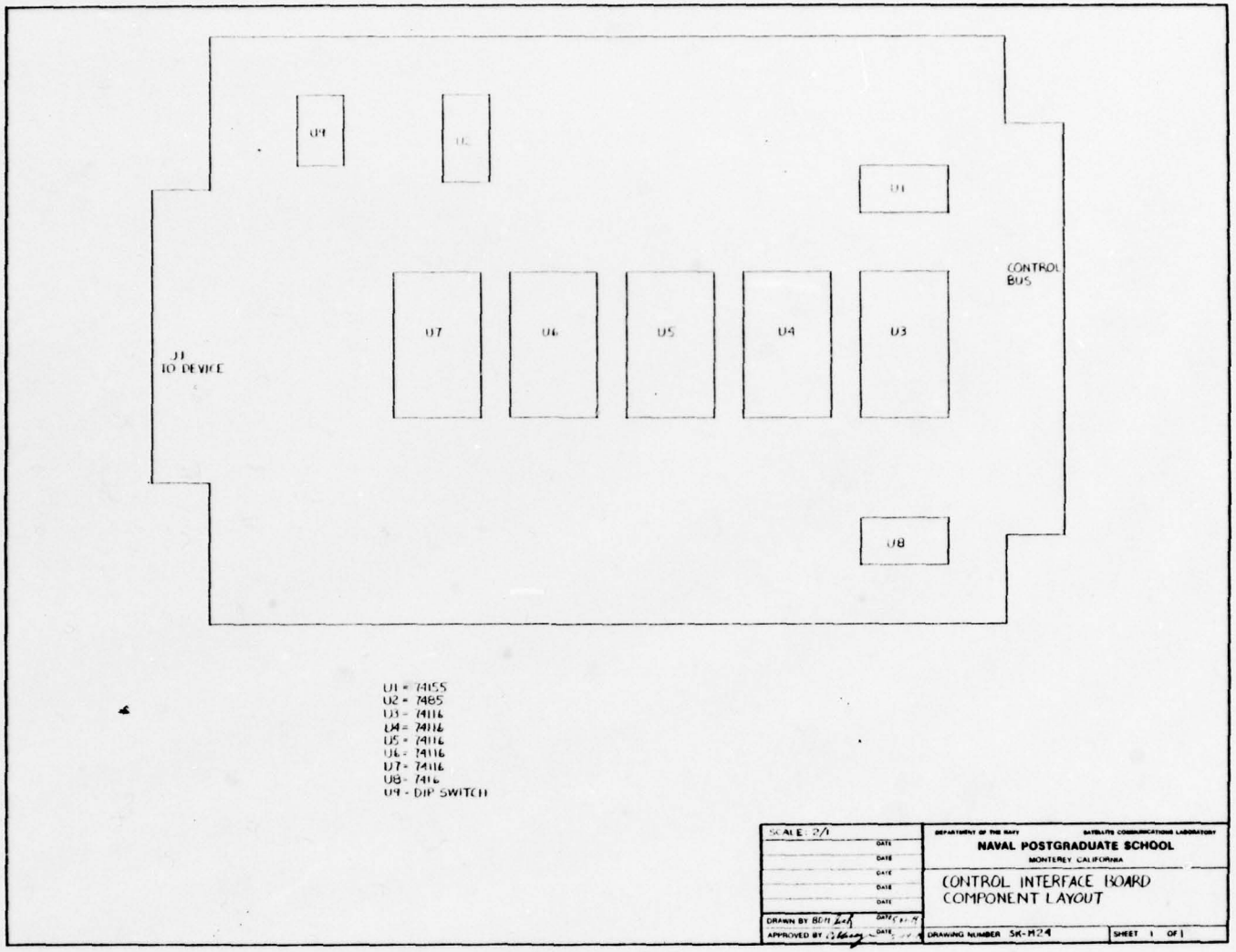


Figure 2.5
CONTROL INTERFACE BOARD COMPONENY LAYOUT

E. REMOTE CONTROL OF DEVICES USING PDP 11/34

Figure 2.6 is the data format required for the PDP 11/34 DR11C to communicate from the CIB and to a particular device with an example given. The digital word 065032 is allowing BYTE 2 (i.e., CIB output connector J1 PINS 4, 2, 3, 1, 8, 6, 7, 5) to be "LATCHED" on DEVICE 6 with data D7=0, D6=1, D5=1, D4=0, D3=1, D2=0, D1=1, D0=0. In the case of a ROCKLAND SYNTHESIZER, Figure 2.7 shows the programming method.

F. TEST BOARDS

. The following will be a description of the three test boards designed to trouble-shoot either the CIB or the ROCK-LAND SYNTHESIZERS or BOTH.

The COMPUTER SIMULATOR board takes the place of the PDP 11/34 DR11C and is a board consisting of a set of DIP Switches which either apply ground to the input lines of the CIB DRIVER BOARD or apply nothing. The 3.3kΩ resistors on the input lines to the 7416 HEX inverters of Figure 2.2 are pull-up resistors included so as to always pull the input lines high (+5V) unless pulled low by either the PDP 11/34 DR11C or by the COMPUTER SIMULATOR. A push button momentary switch is included on the COMPUTER SIMULATOR to simulate the positive-to-negative New Data Ready pulse. Figure 2.8 shows the schematic of the computer simulator and Figure 2.9 shows not only the component layout but also which DIP switches apply to data bits, board or device select Bits, and Byte select Bits. Appendices A and B discuss testing procedures using various combinations of the PDP 11/34, the COMPUTER SIMULATOR and the DEVICE SIMULATOR.

OCTAL WEIGHT	1	4	2	1	4	2	1	4	2	1	4	2	1	4	2	1
	D7	D6	D5	D4	D3	D2	D1	D0	X	X	S3	S2	S1	S0	A1	A0
	0	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0

D7 = MSB = DATA BIT
D6 = 2nd MSB = DATA BIT
D5 = 3rd MSB = DATA BIT
D4 = 4th MSB = DATA BIT
D3 = 5th MSB = DATA BIT
D2 = 6th MSB = DATA BIT
D1 = 7th MSB = DATA BIT
D0 = LSB = DATA BIT
X = Always Zero

S3 = MSB of Device Address
S2 = 2nd MSB of Device Address
S1 = 3rd MSB of Device Address
S0 = LSB of Device Address

A1 = MSB BYTE SELECT
A0 = LSB BYTE SELECT

Example: Digital Word Above = 065032

Figure 2.6

Communication From PDP 11/34 To The Control Interface Boards

NOTE: GROUND=LOGICAL ONE AND +5V = LOGICAL ZERO
EXAMPLE: 123.456789MHz

HEX WEIGHT

8421 PINS OF REMOTE FREQUENCY CONTROL ON ROCKLAND

10MHz X 12 → 1100 (i.e., PIN 41=GND, PIN 40=GND, PIN 16=+5, PIN 15=+5)

1MHz X 3 0011 (i.e., PIN 20=+5, PIN 19=+5, PIN 18=GND, PIN 17=GND)

100MHz X 4 0100 (i.e., PIN 27=+5, PIN 26=GND, PIN 2=+5, PIN 1=+5)

10KHz x 5 0101 (i.e., PIN 29=+5, PIN 28=GND, PIN 4=+5, PIN 3=GND)

1KHz X 6 0110 (i.e., PIN 31=+5, PIN 30=GND, PIN 6=GND, PIN 5=+5)

100Hz X 7 0111 (i.e., PIN 33=+5, PIN 32=GND, PIN 8=GND, PIN 7=GND)

10Hz X 8 1000 (i.e., PIN 35=GND, PIN 34=+5, PIN 10=+5, PIN 9=+5)

1Hz X 9 1001 (i.e., PIN 37=GND, PIN 36=+5, PIN 12=+5, PIN 11=GND)

The four sets of 16 data BITS from the PDP 11/34 DR11C to the CONTROL BUS would be as follows for the ROCKLAND SYNTHESIZER designated as DEVICE 14.

	D7	D6 D5 D4	D3 D3 D1	D0 X X	S3 S2 S1	S0 A1 A0	
10MHz&1MHz	1	1 0 0	0 0 1	1 0 0	1 1 1	0 1 1	BYTE 3
100KHz&10KHz	0	1 0 0	0 1 0	1 0 0	1 1 1	0 1 0	BYTE 2
1KHz&100Hz	0	1 1 0	0 1 1	1 0 0	1 1 1	0 0 1	BYTE 1
10Hz&1Hz	1	0 0 0	1 0 0	1 0 0	1 1 1	0 0 0	BYTE 0

The Four Digital Octal Coded Words Would Be

141473 = BYTE 3 = CHANGES MSD & 2nd MSD to 123.MHz on DEVICE 14

042472 = BYTE 2 = CHANGES 3rd & 4th MSD to .45MHz on DEVICE 14

063471 = BYTE 1 = CHANGES 5th & 6th MSD to 6.7KHz on DEVICE 14

104470 = BYTE 0 = CHANGES 7th & 8th MSD to 89Hz

Figure 2.7

Programming A ROCKLAND MODEL 5610A Synthesizer

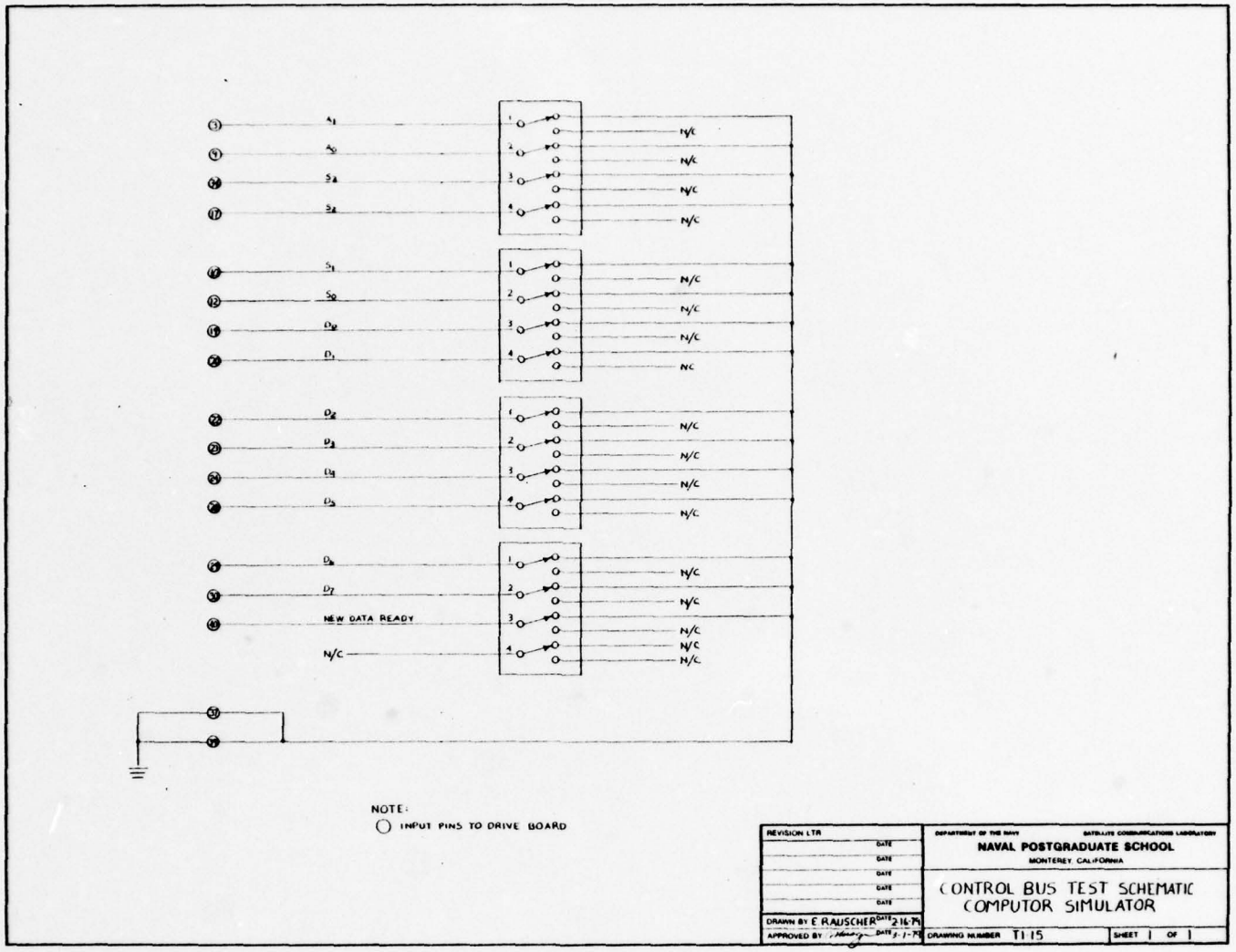


Figure 2.8
Control Bus Test Schematic Computer Simulator

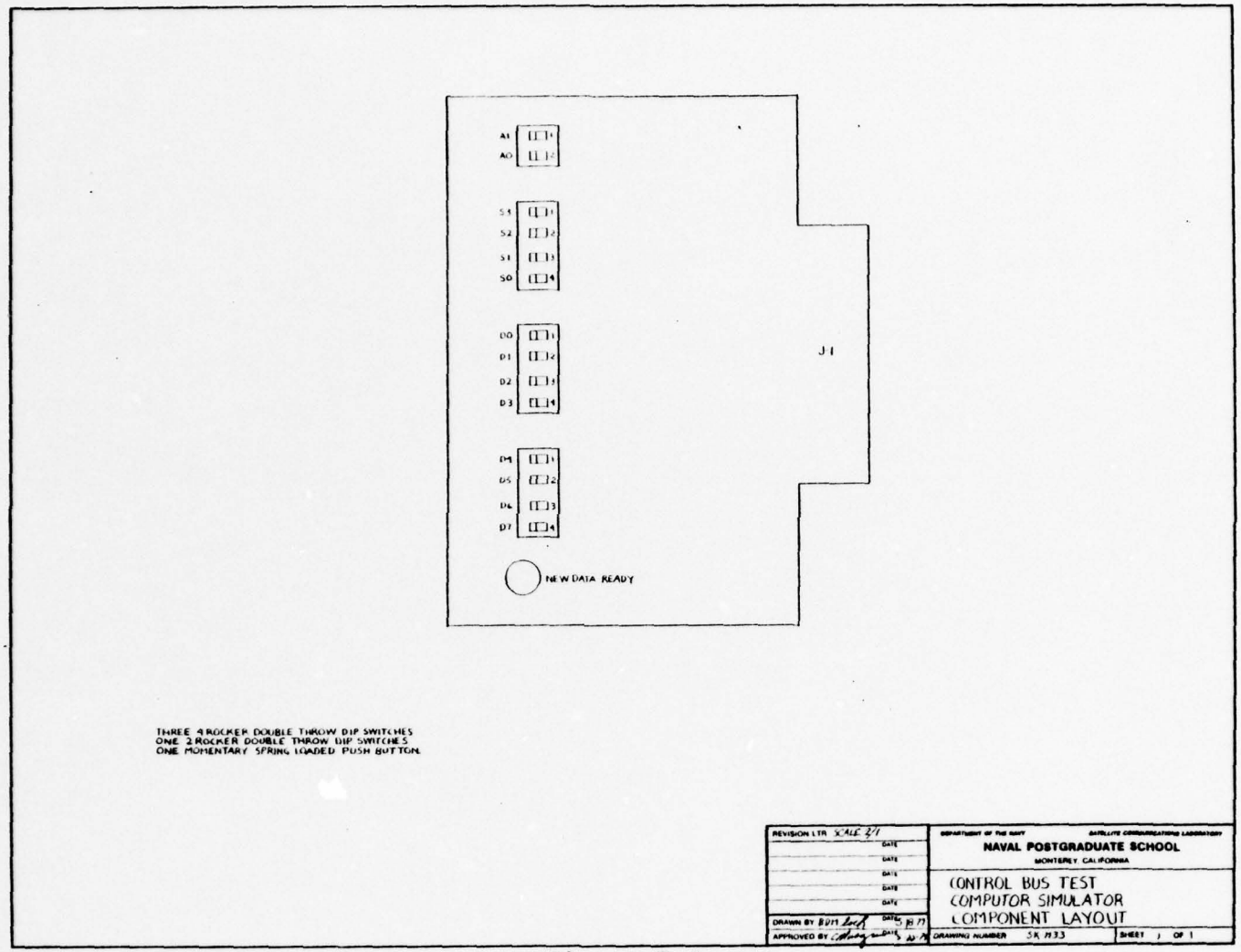


Figure 2.9
Control Bus Test Component Layout Computer Simulator

The DEVICE SIMULATOR is a board which substitutes for synthesizers or other devices under control of the PDP 11/34 DR11C or the COMPUTER SIMULATOR. The DEVICE SIMULATOR is merely a set of LEDs connected to the output of any one of the C.I.B.'s. As the PDP 11/34 DR11C or the COMPUTER SIMULATOR communicates thru the driver board and on thru the CIB (to which the DEVICE SIMULATOR is attached) the LEDs can be observed to change. Figure 2.10 shows the schematic and Figure 2.11 shows the component layout of the DEVICE SIMULATOR.

The ROCKLAND SYNTHESIZER TESTER has been designed and is under construction. Its purpose is to apply GROUND (LOGICAL ONE) or +5V (LOGICAL ZERO) to the same pins of the REMOTE FREQ. CONTROL CONNECTOR as the CIB (i.e., to SIMULATE the CIB). Figure 2.12 shows the schematic for the ROCKLAND SYNTHESIZER TESTER. This TESTER may be used to test any digitally programmable device driver by the CIB within the S.S.A.

G. CIB TERMINATOR

The purpose of the CIB TERMINATOR BOARD is to provide a termination impedance on each line of the CONTROL BUS. This termination impedance presents the electrical "appearance" of an almost infinitely long CONTROL BUS. In other words, signals which are on the CONTROL BUS, going from the driver board to a particular CIB, will propagate in one direction on the CONTROL BUS and finally be absorbed by the TERMINATOR. Without the TERMINATOR, this signal would propagate from the

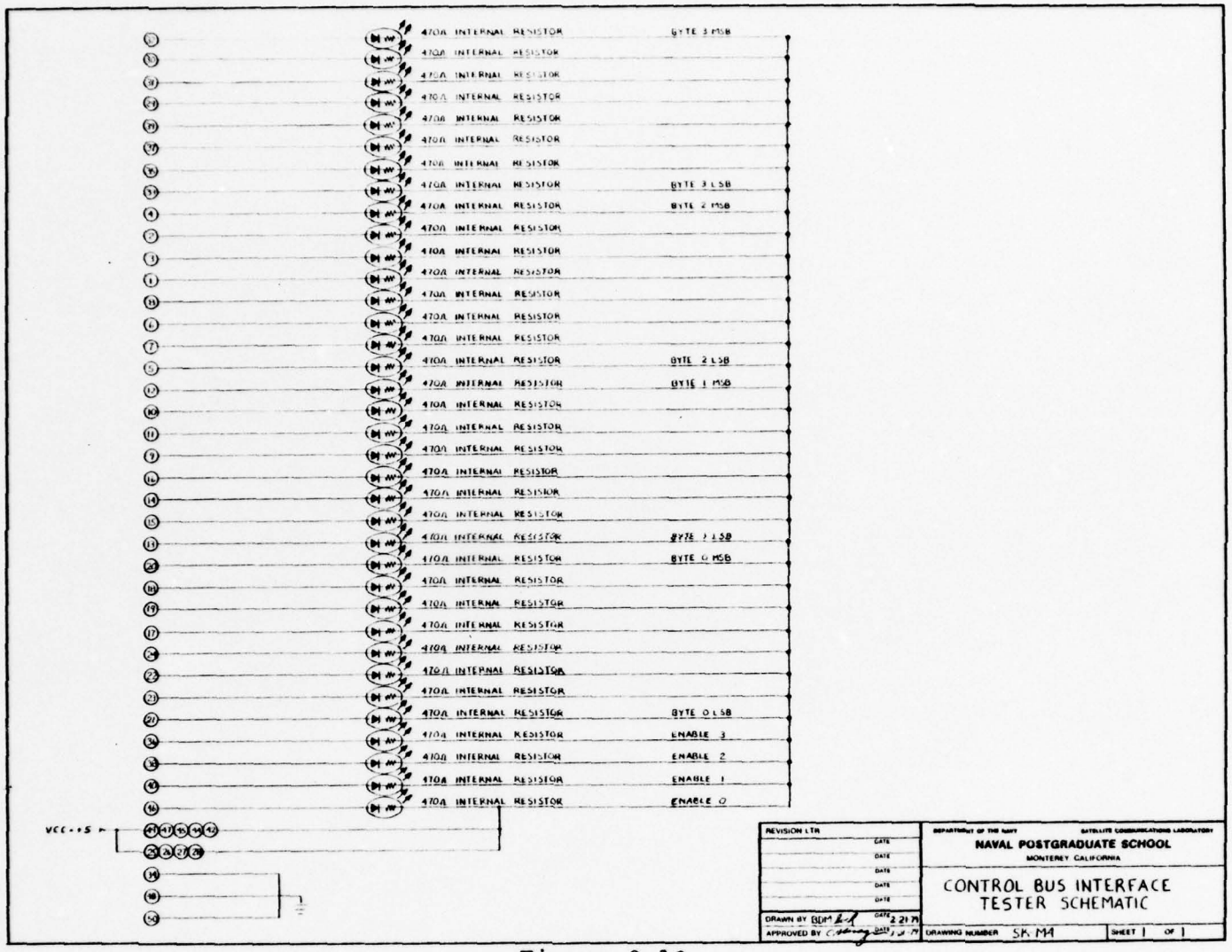


Figure 2.10
Control Bus Interface Tester Schematic

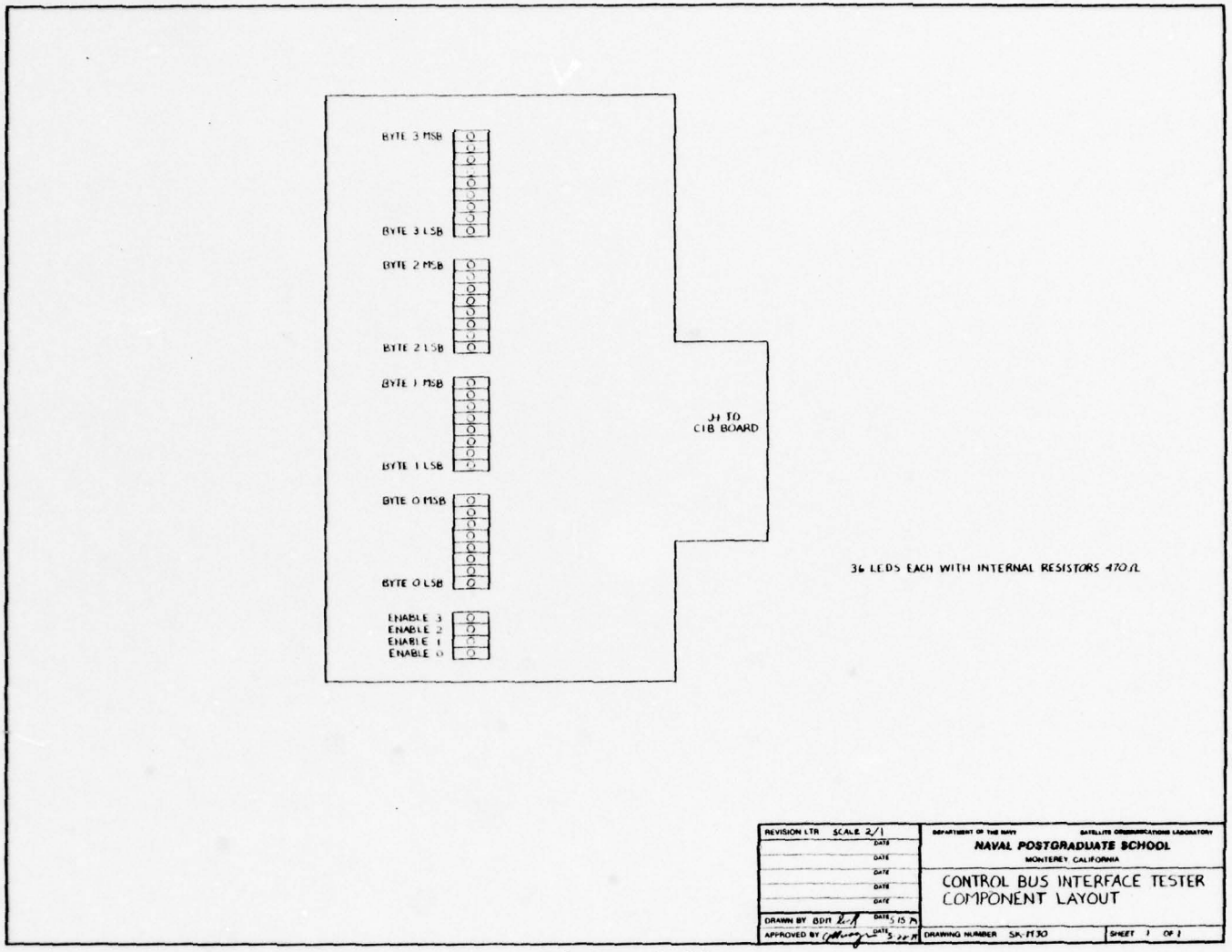


Figure 2.11
Control Bus Interface Tester Component Layout

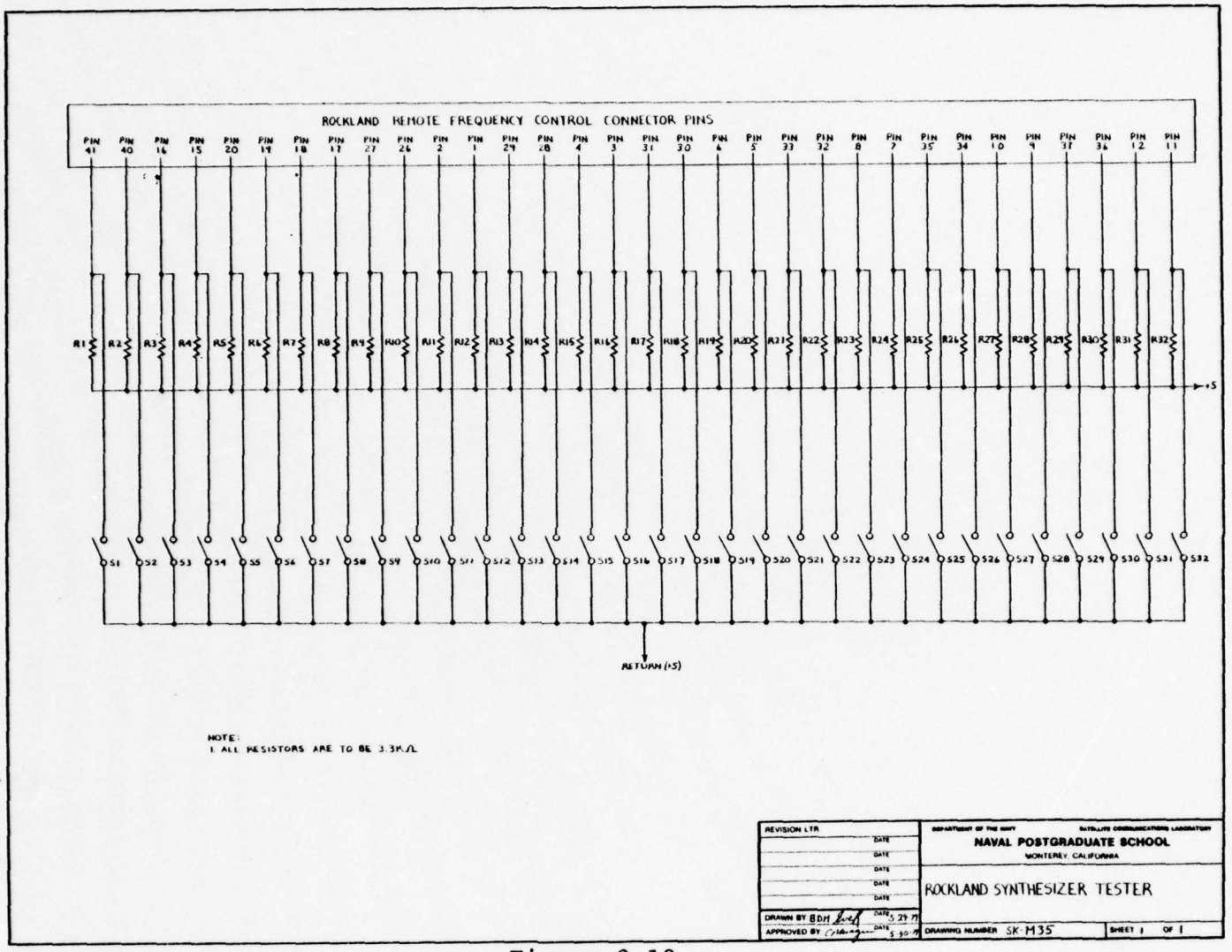


Figure 2.12
ROCKLAND SYNTHESIZER Tester

DRIVER BOARD, reach the electrical end of the CONTROL BUS. and then reflect back in the direction of the DRIVER BOARD. More simply said, the CIB TERMINATOR eliminates reflections and the resultant standing waves caused by reflections. Figure 2.13 shows the schematic and Figure 2.14 shows the COMPONENT LAYOUT of the CONTROL INTERFACE TERMINATOR BOARD. C16 (10μfd ELECTRO-LYTIC) is used to add some filtering to the +5(Vcc) supply for the CONTROL BUS.

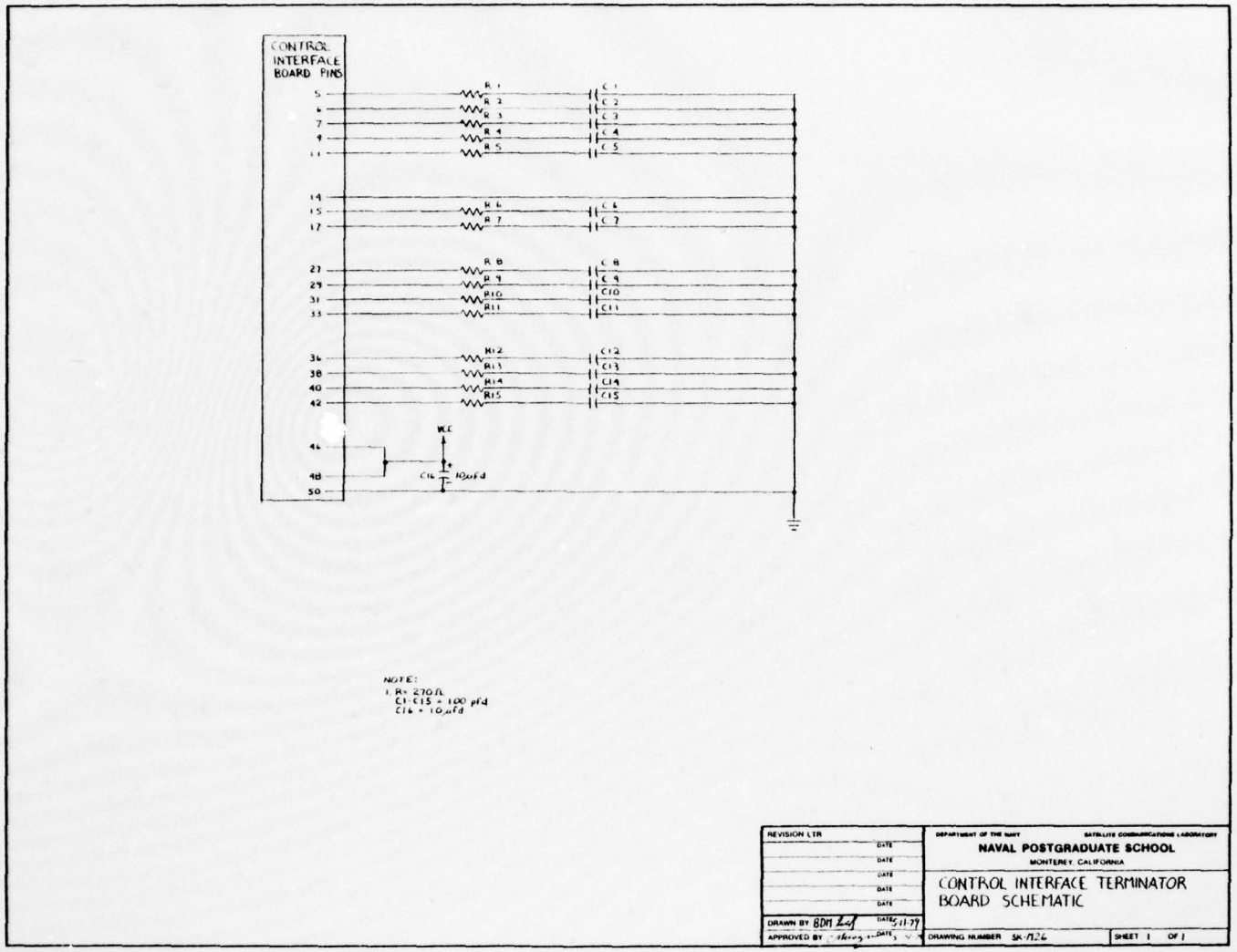


Figure 2.13
Control Interface Terminator Board Schematic

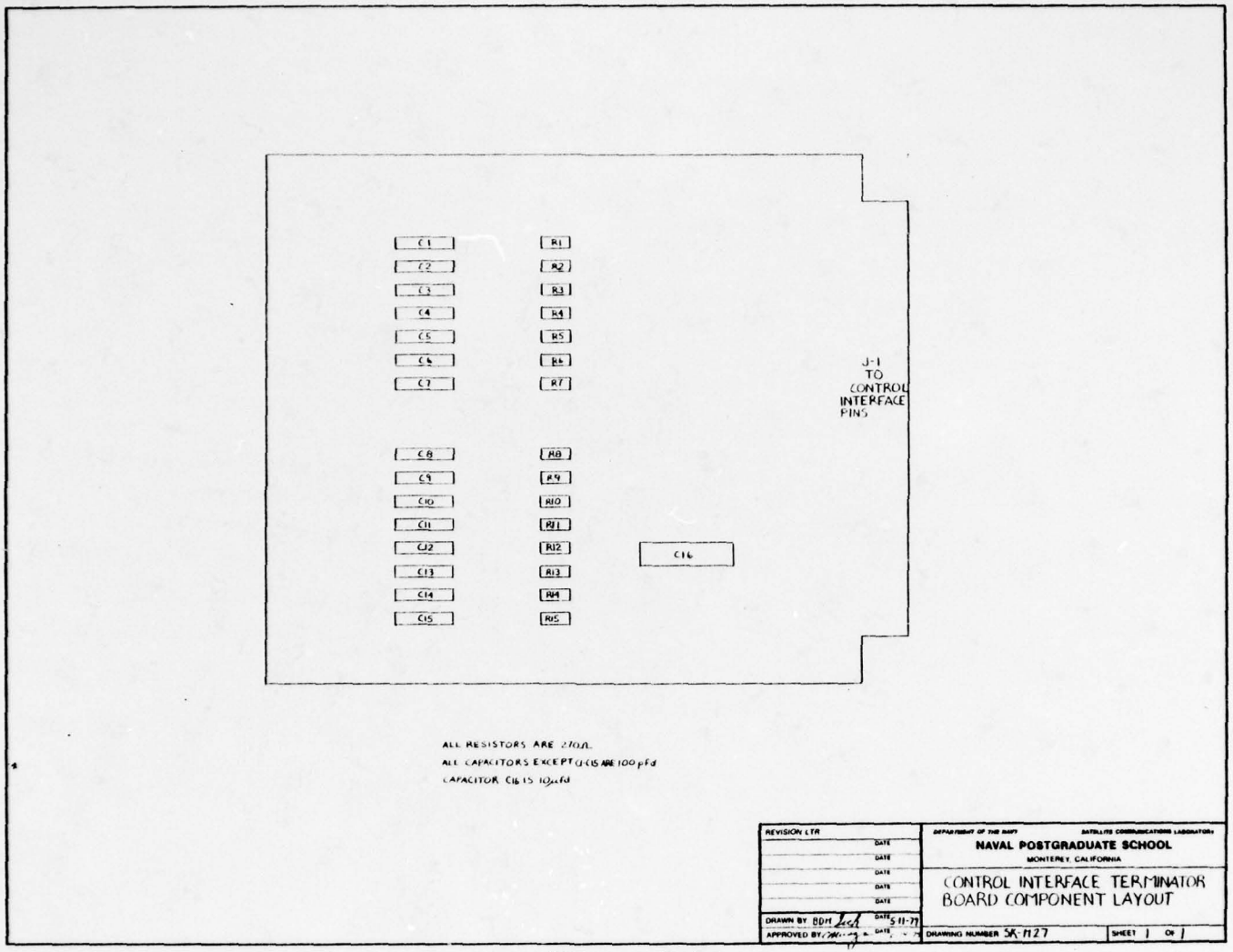


Figure 2.14
Control Interface Terminator Board Component Layout

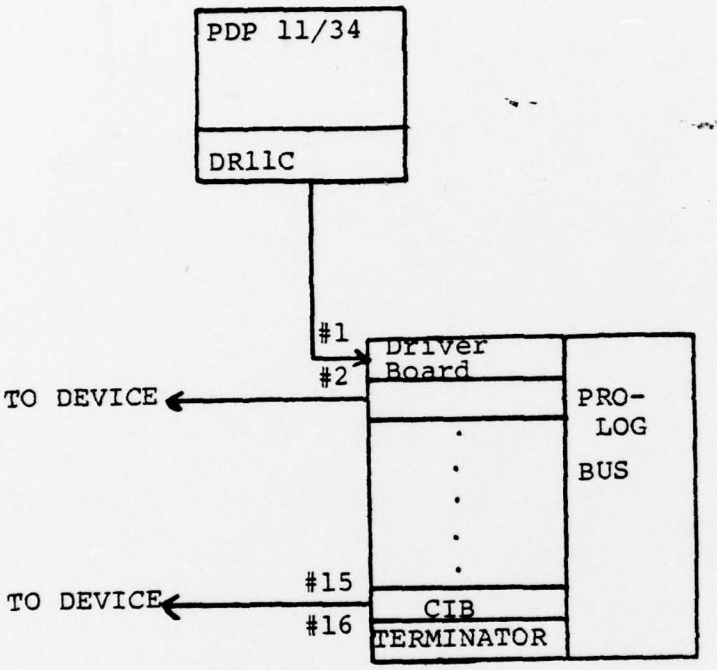


Figure 2.15

CIB System Configuration

III. TEST UNIT

A. INTRODUCTION

The ability to observe signals of any system while operating is a luxury which the operators and maintenance personnel would gladly have. The tolerances of the S.S.A. R. F. RECEIVER hardware makes this a necessity.

Figure 3.1 is a basic block diagram of the TEST UNIT (i.e., several pieces of hardware were omitted merely for simplicity of initial exposure). Table II shows some of the capabilities of the test unit. The NOISE FIGURE TEST applies a known voltage to a noise diode in the "front-end" (RF SECTION) of each receiving system. This known voltage will cause the noise diode to inject a known amount of noise into the RF PREAMP to test all S.S.A. and WSC5 receivers. The SPECTRUM ANALYSIS section provides the capability to monitor S.S.A. system signals: Two RF TRANSMIT (X1, X2) signals, three RF RCVR (RS1, RS2, RS3,) signals, and three I.F. RCVR (RC1. RC2, RC3) signals. In addition, the operator may select a "MARKER" frequency, displayed on a TEKTRONIX 7613/7L12 SPECTRUM ANALYZER in order to determine accurately the frequency being displayed. This PSECTRUM ANALYSIS section should not be considered a part of the S.S.A.'s ability to do spectrum analysis on satellite signals. The R.F. section of the TEST UNIT generates the proper frequency and power necessary to transmit a signal to the several satellites presently aloft. The LEVELER ensures

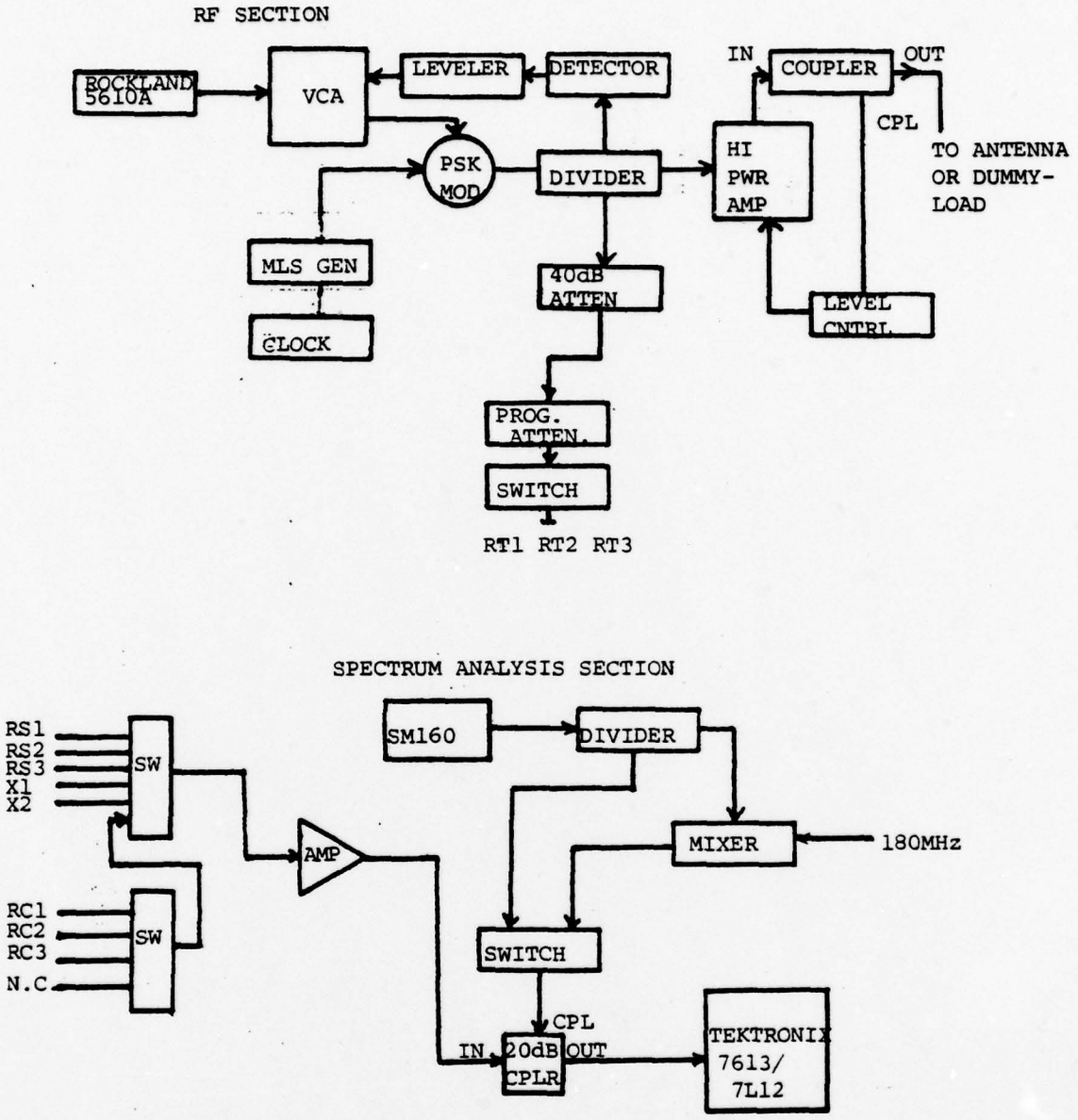


Figure 3.1
Test Unit Block Diagram (BASIC)

TABLE II

TEST UNIT CAPABILITIES

TEST XMITTER	290-320 MHz	
	100 WATTS(1dB power resolution)	
	TWO ANTENNAS	
	31dB POWER CONTROL RANGE	
RECEIVER TEST	240-270 MHz	
	-150 to -85 dBm	
	THREE FRONT-ENDS	
SPECTRUM ANALYSIS	RS1, RS2, RS3	240-270 MHz
	RC1, RC2, RC3	60-90 MHz
	X1, X2	290-320 MHz
PSEUDO-RANDOM SEQUENCE (P.R.S.)	LENGTH = 511 (2^9-1)	
CLOCK OF P.R.S.	75Hz, 300Hz, 600Hz, 1.2KHz, 2.4KHz, 4.8KHz, 9.6KHz, 19.2KHz	

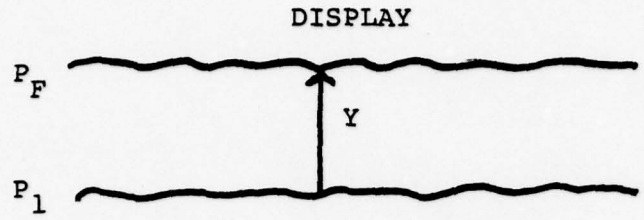
a constant power level is provided to the input of the Hi PWR AMP (H.P.A.). The H.P.A. has a 30dB GAIN. With an input power of 30 dBm, the H.P.A. is capable of transmitting 100W MAX to each antenna or the dummy load. A pseudo-random sequence generator is provided, with eight selectable clock-rates in order to transmit a PSK modulated signal. The RF section also provides an attenuated signal which can be used to inject a known frequency and power signal into the spectrum receivers (RT1, RT2, RT3).

B. NOISE FIGURE TEST SECTION

The NOISE FIGURE TEST has been designed and is under construction. The purpose, as previously stated, is to inject a known amount of noise and thereby measure the NOISE FIGURE of all the receivers. This is done as shown in Figure 3.2. Figure 3.3 shows the schematic of the NOISE FIGURE TEST. NT1 and NT2 are both provided to measure the NOISE FIGURE of the two RF UNITS immediately after the QUAD OE82 antennas (Figure 1.1).

C. SPECTRUM ANALYZER SECTION

This section, as previously mentioned, allows the operator the ability to display, on the TEKTRONIX SPECTRUM ANALYZER 7613/7L12, thos SSA signals of interest: RS1, RS2, RS3, X1, X2, RC1, RC2, RC3 and also provides the operator with a "MARKER" displayed so as to measure the frequencies of these signals.



k = BOLTZMAN'S CONSTANT

P_1 = PRESENT SYSTEM INPUT POWER

P_F = SYSTEM POWER (WITH NOISE DIODE ON)

T_A = TEMPERATURE OF ANTENNA

T_R = TEMPERATURE OF RECEIVER

T_D = TEMPERATURE OF NOISE DIODE

Top= TR+TA = SYSTEM OPERATING TEMPERATURE

Y = Y-FACTOR DUE TO NOISE DIODE

$$P_1 = k(T_A+T_R)BG$$

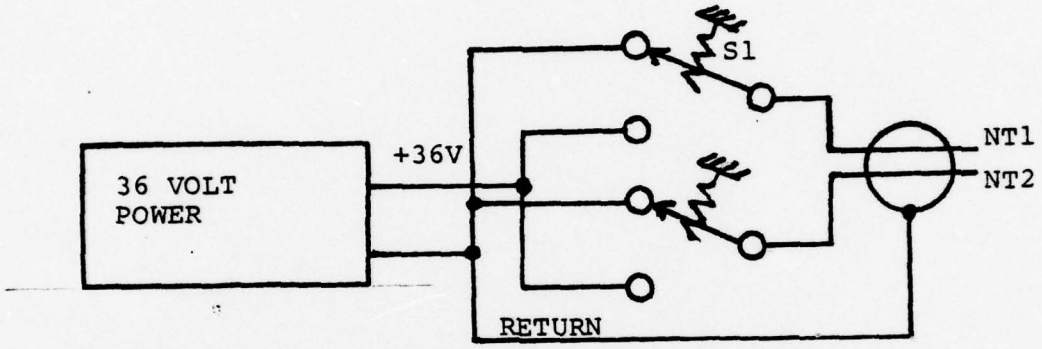
$$P_F = k(T_A+T_R+T_D)BG$$

$$Y = \frac{P_F}{P_1} = \frac{(T_A + T_R + T_D)}{T_A + T_R}$$

$$Y = \left(\frac{Top + T_D}{Top}\right)$$

solving for Top $$Top = \frac{T_D}{Y-1}$$

Figure 3.2
Noise Figure Test Calculations



S1 IS A DOUBLE-POLE, DOUBLE-THROW, CENTER REST, MOMENTARY SWITCH

NT1 = NOISE TEST #1

NT2 = NOISE TEST #2

Figure 3.3

Noise Figure Test Schematic

The selection of RS1, RS2, RS3 /240-270MHz/, or X1, X2 /290-320MHz/, or RC1, RC2, RC3 /60-90MHz/ for display on the TEKTRONIX 7613/7L12 SPECTRUM ANALYZER (called TEKTRONIX or 7613 or SPECTRUM ANALYZER hereafter) will be discussed in greater detail later, but for now assume RS1 has been selected with a push-button and the lamp beneath it has been illuminated. The signal RS1 (240-270 MHz) arrives at LORCH SWITCH S5 of Figure 3.4 from the RF "FRONT-END" of the SPECTRUM RECEIVERS. The operator selection (push-button action) of RS1 will route the signal thru S5 to the ANZAC AMPLIFIER, thru a coupler and into the 7613 for display and power level measurement. Assume now that the operator desires to measure the frequency of RS1 using the "MARKER". The thumbwheels which vary the frequency of the SM160 FREQUENCY SYNTHESIZER will be discussed later in more detail. But, presently, the operator selects the frequency at which he desires the MARKER to be (e.g., 243.000MHz). The SM160 is capable of generating frequencies from 20 to 260 MHz. The signal out of the SM160 will be 63 MHz so that when mixed with 180 MHz the resultant frequency will be 243.000MHz at the input "2" to SWITCH S4. Due to the fact that the operator has not only selected "MARKER ON", but also dialed a frequency which is valid for RS1, the control of S4 is such that the 243MHz passes thru S4 thru the 20dB coupler and is super-imposed on the screen of the 7613 with the RS1 signal. If RC1, RC2, or RC3 were selected, "MARKER ON" was selected, and a frequency from 60-90MHz was dialed on the THUMBWHEELS the operator would view one of either RC1, RC2, or RC3 and

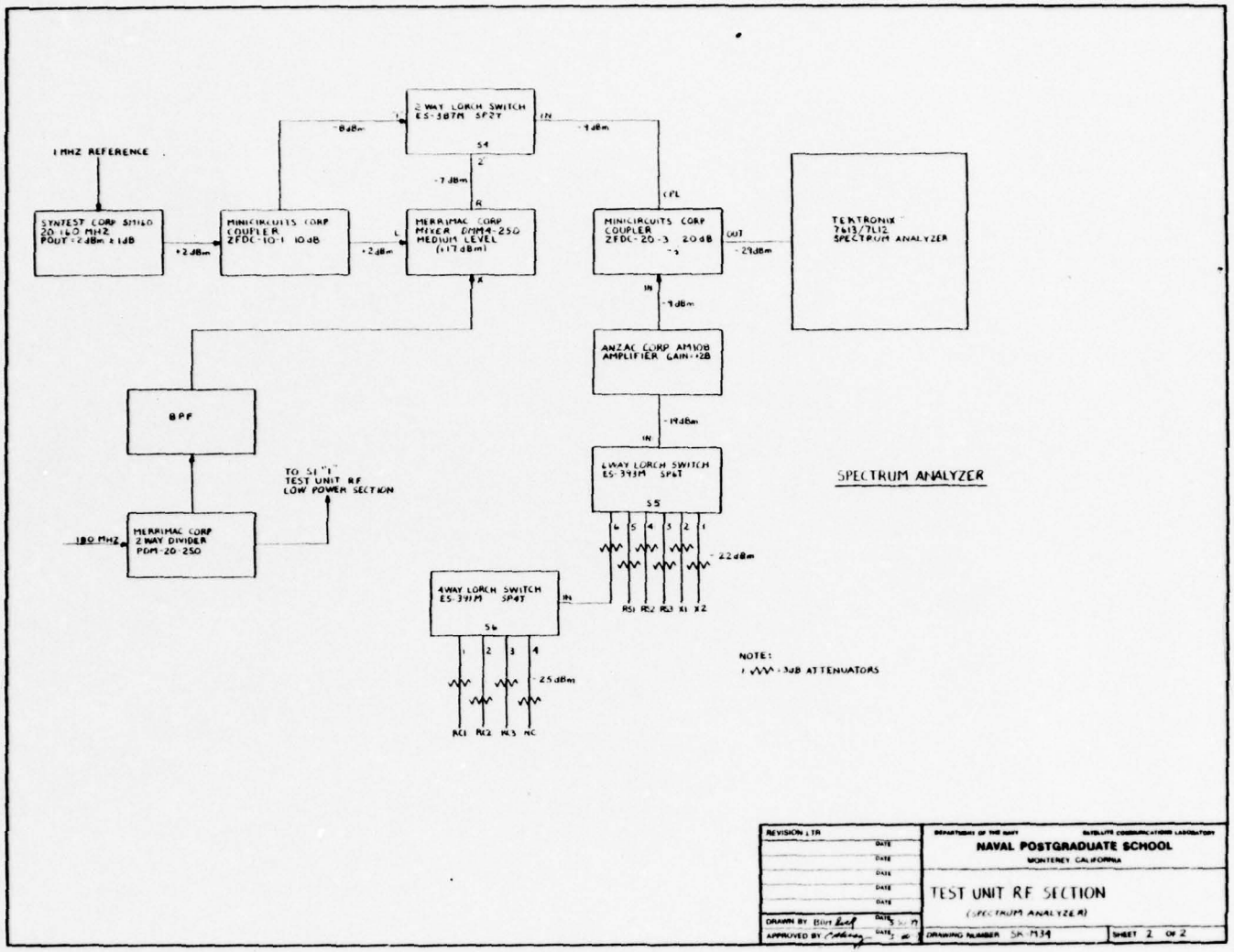


Figure 3.4

Test Unit Spectrum Analyzer Section

the MARKER both of which would be in the 60-90MHz range. An explanation of the SM160 FREQUENCY SYNTHESIZER and THUMBWHEELS is appropriate at this point. The SM160 frequency synthesizer is a digitally programmable, single board frequency generator with frequency resolution of 1KHz capable of generating frequencies from 20-160MHz. The RC1, RC2 and RC3 are the only signals in this range (60-90MHz). Each digital programming line for the SM160 comes directly from Figure 3.5 and Figure 3.6 and directly from the THUMBWHEELS with the exception of PINS 5, 4, 3, 2, and B.

These five programming lines are attached to a 74186-64 WORD X 8 BIT PROM (FUZEABLE LINK). This PROM has been programmed in order to ensure the SM160 produces the proper frequency based on the numbers dialed on the THUMBWHEELS. Appendix C covers the operation of these THUMBWHEELS. Figure 3.7 is a component layout of the pull-up resistors required to make the thumbwheels operate. Table I shows the selection of the THUMBWHEELS and the resultant frequency out of the SM160. Appendix D cover the programming of the 74186 PROM. This system produces the MARKER frequencies desired using only the SM160 and 74186 PROM. The logic for switch S4 (i.e., whether to select a frequency which is mixed with 180MHz or one which is not) will be covered later. The PROM also has one other unique feature programmed into it. That feature is an indicator to the operator that he has selected a frequency from 60-99.999MHz, 240-279.999MHz or 290-329.999MHz as shown in Table I. On Figure 3.5 pin 22 of J22 the 74186 PROM is

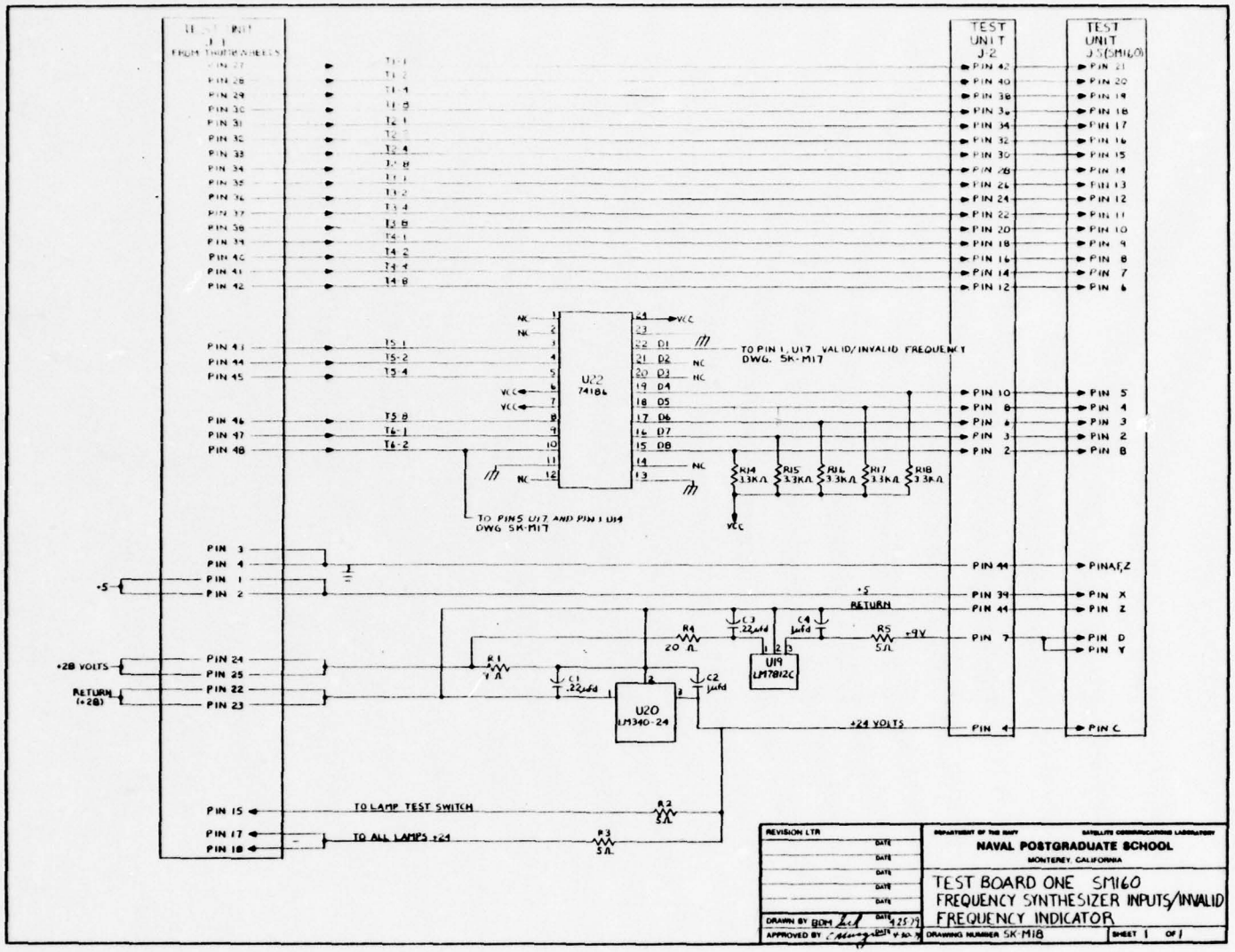


Figure 3.5

Test Board One SM160 Frequency Synthesizer Inputs/Invalid Freq Indicator

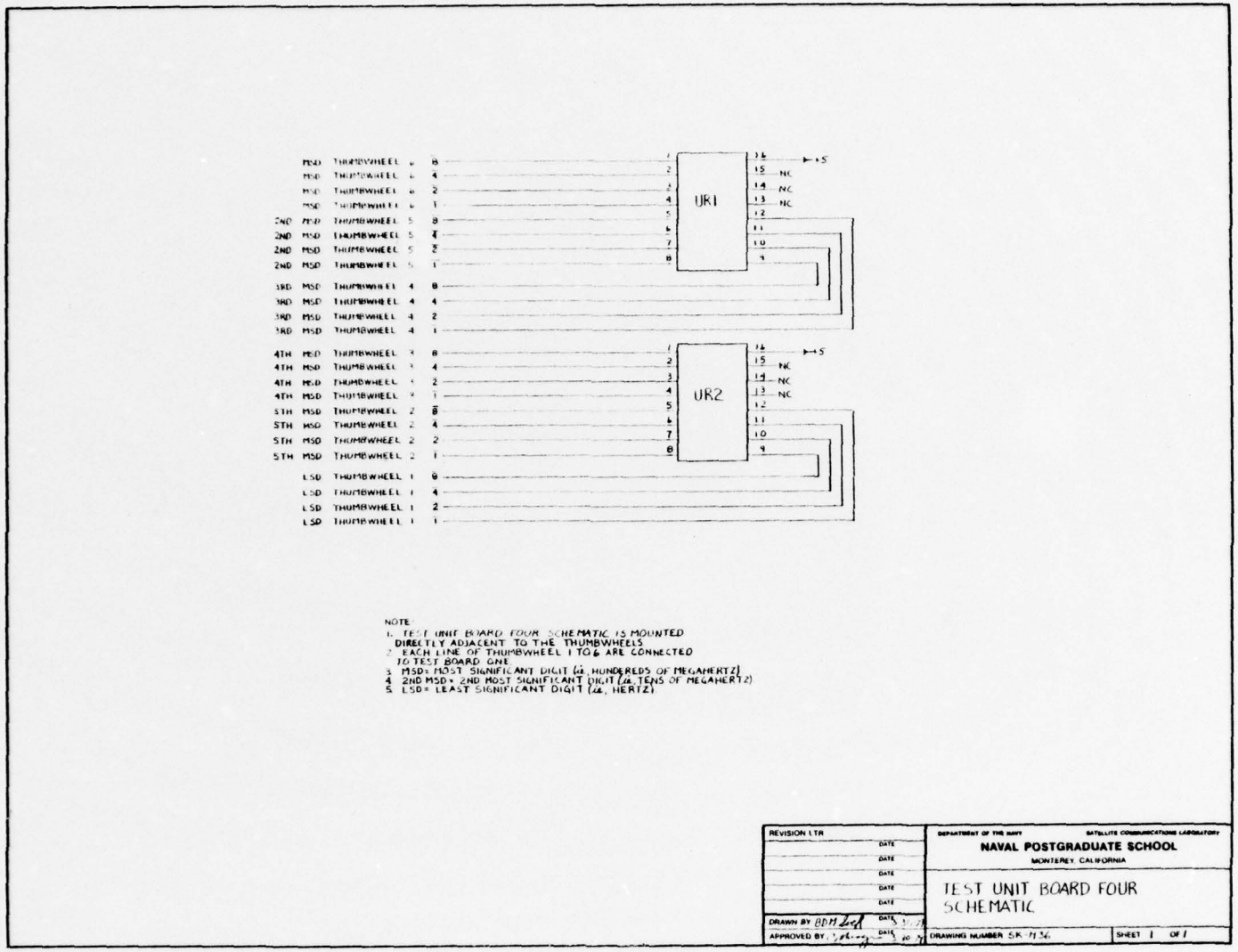


Figure 3.6

Test Board Four Schematic

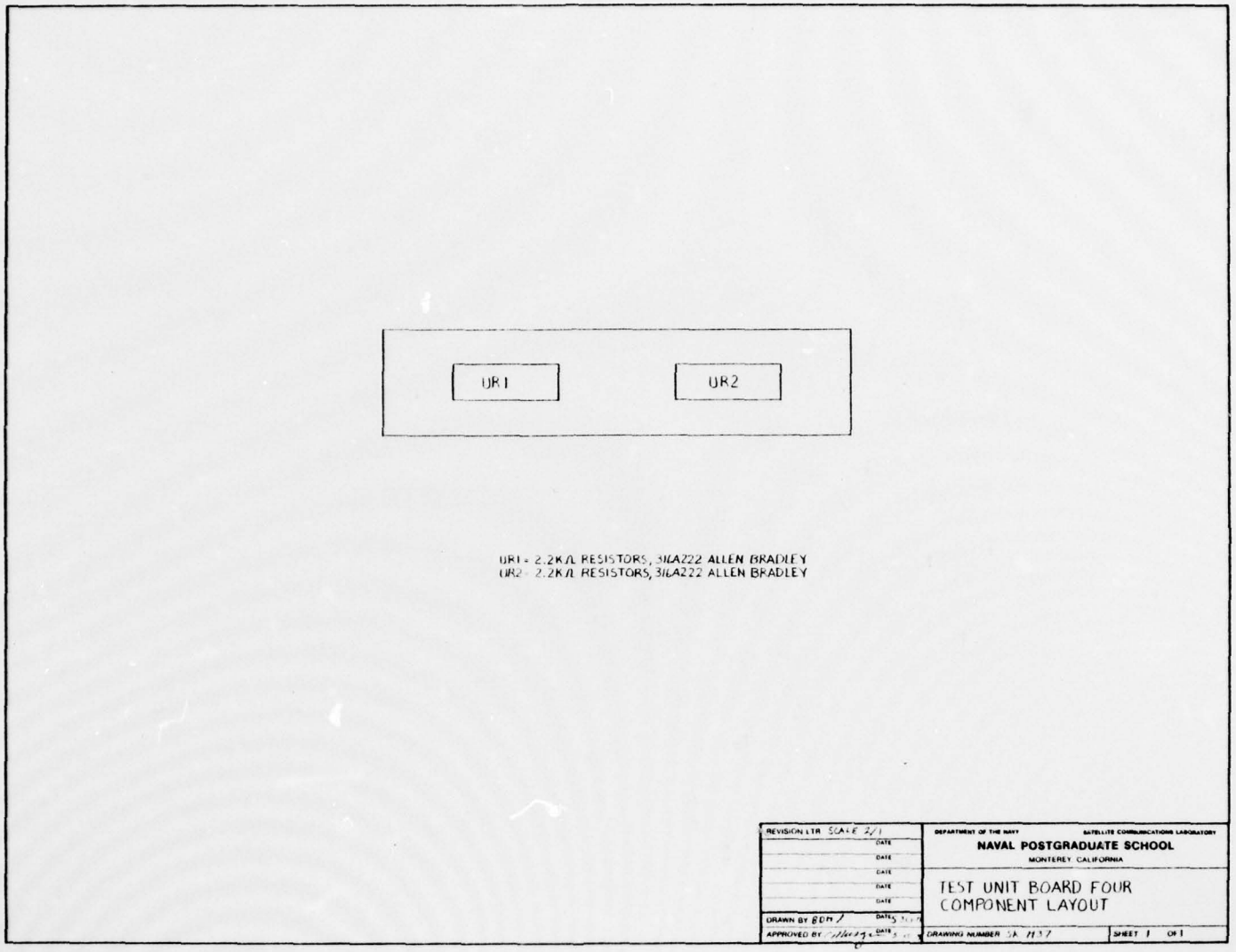


Figure 3.7

Test Board Four Component Layout

TABLE III

Thumbwheel Selection and SM160 Output

MST	2nd MST	SM160 OUTPUT	VALID FREQ
0	6	60 - 69.999MHz	YES
0	7	70 - 79.999MHz	YES
0	8	80 - 89.999MHz	YES
0	9	90 - 99.999MHz	YES
2	4	*60 - 69.999MHz	YES
2	5	*70 - 79.999MHz	YES
2	6	*80 - 89.999MHz	YES
2	7	*90 - 99.999MHz	YES
2	9	*110 - 119.999MHz	YES
3	0	*120 - 129.999MHz	YES
3	1	*130 - 139.999MHz	YES
3	2	*140 - 149.999MHz	YES

* These are mixed (up converted) with 180MHz to produce 240-270 or 290-320MHz

MST = Most significant thumbwheel (on operator's left)

All other frequencies are invalid.
As are all other MST & 2nd MST.

that line which provides an indication of a valid invalid frequency (Hi=ONE=Vcc=+5=VALID and LOW=ZERO=GND=INVALID). The remainder of Figure 3.5 is merely a set of 3-TERMINAL regulators used to provide the proper power supply voltages and currents to the SM160 and to produce +24 VOLTS which is used to illuminate the lamps and power the lamp drivers.

D. LOW POWER SECTION

The purpose of the LOW POWER SECTION, shown in the center of Figure 3.8, is to provide a signal of fixed power and in the frequency range 240-270MHz for the RECEIVER TEST or 290-320 MHz for the TEST XMTR. The ROCKLAND SYNTHESIZER generates frequencies of 100KHz-160MHz; determined by the CONTROL BUS. If the RVCR TEST has been selected the frequency out of the ROCKLAND will be 90-120MHz so as to mix with 150MHz from S1 and produce a signal at 240-270MHz. If the TEXT XMTR has been selected, the ROCKLAND will produce frequencies of 110-140MHz so as to mix with 180MHz from S1 and yield a signal at 290-320MHz. The control bits for the selection of 150 or 180MHz at SWITCH S1 are the same control bits which select the signal path thru SWITCH S2 and will be discussed in the SELECTION AND LAMP SECTION. After up-conversion (mixing in the MERRIMAC DMM4-250 MEDIUM LEVEL MIXER) the signal is sent thru a DOUBLE BALANCED MIXER, PSK MODULATOR, AMPLIFIER, an unspecified BAND-PASS FILTER, and a 2-WAY DIVIDER. One output of the 2-WAY DIVIDER is sent to SWITCH S2 for routing the signal to the RCVR TEST or TEST XMTR SECTIONS. The other output of the 2-WAY DIVIDER is connected to an R.F. crystal DETECTOR which

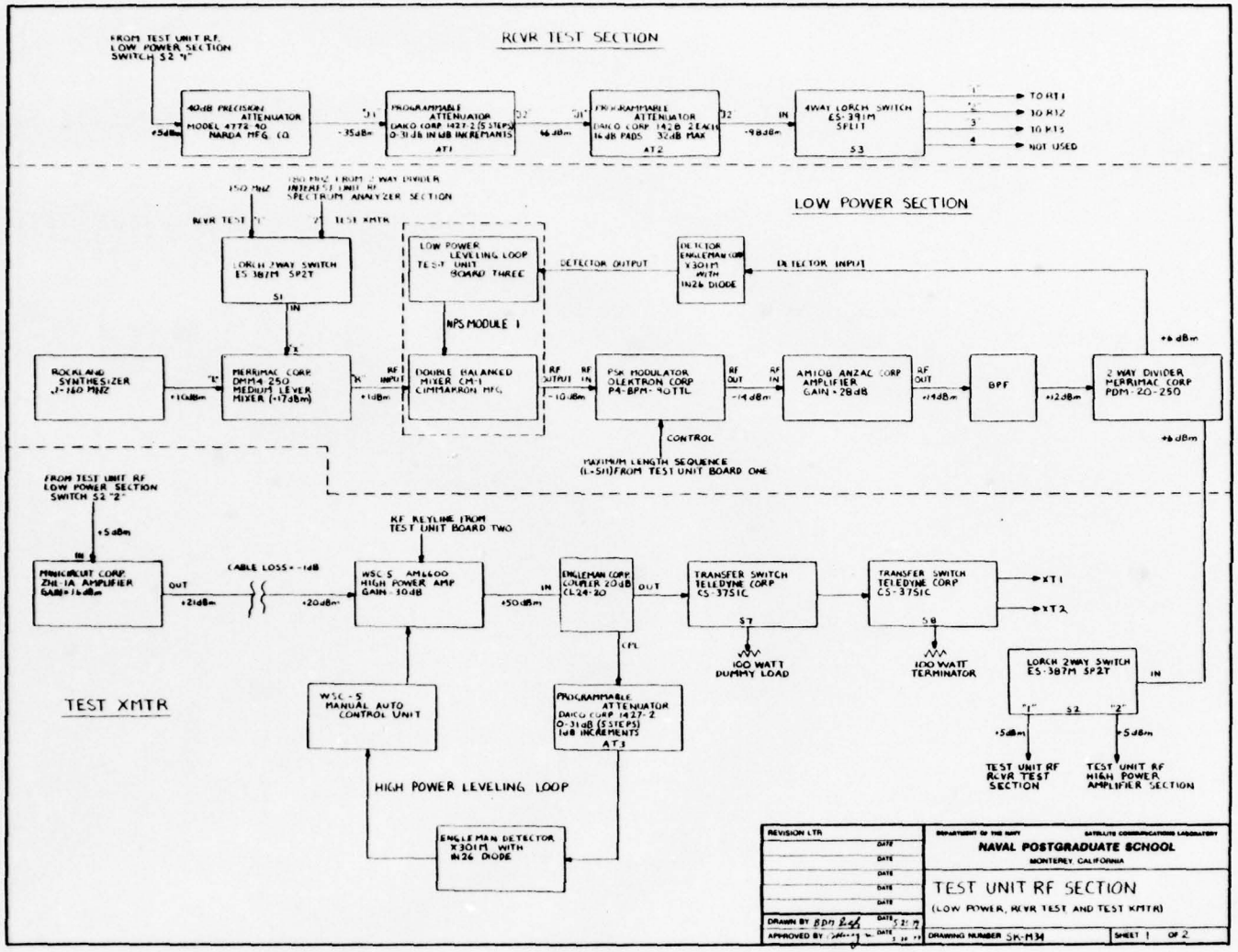


Figure 3.8

Test Unit RF Section - Low Power, RCVR Test and Test XMTR

converts the R.F. energy into a proportional positive D.C. voltage. The positive output of the detector is applied to the POSITIVE DETECTOR OUTPUT TERMINAL of the LOW POWER LEVELING LOOP Figure 3.9. Figure 3.10 is the component layout of the LOW POWER LEVELING LOOP. A brief explanation of the DOUBLE BALANCED MIXER will aid in the understanding of the LOS POWER LEVELING LOOP. The CM1 DOUBLE BALANCED MIXER manufactured by CIMARRON CORP. is being used as a current-controlled attenuator. The IF input port shown on Figure 3.11 can be driven with a D.C. control current to provide a variable attenuation from the RF input port to the RF output port also shown on Figure 3.11. The plot on Figure 3.11 was taken from the specification sheet from the CM1 [5]. The operational amplifier (OPAMP) 741 provides this D.C. control current to vary the amount of RF energy passed thru the DOUBLE BALANCED MIXER shown on Figure 3.8. On Figure 3.8, to summarize, the RF energy from the MERRIMAC MIXER is amplified by the AM108, split by the MERRIMAC 2-WAY DIVIDER, changed to a D.C. voltage by the ENGLEMAN detector and altered by the 741 to become a control current for the variable attenuation properties of the CIMARRON D.B.M. The two main questions which remain are (1) at what power level (i.e., attenuation value) is the loop set to operate and (2) how are instantaneous changes in RF power taken into account. A value of RF power into the detector which produces $1X10^{-1}$ VOLTS was chosen as the R.F. power calabration point. The R.F. power calibration point is the level of power above which the DOUBLE BALANCED MIXER commences to operate as a current

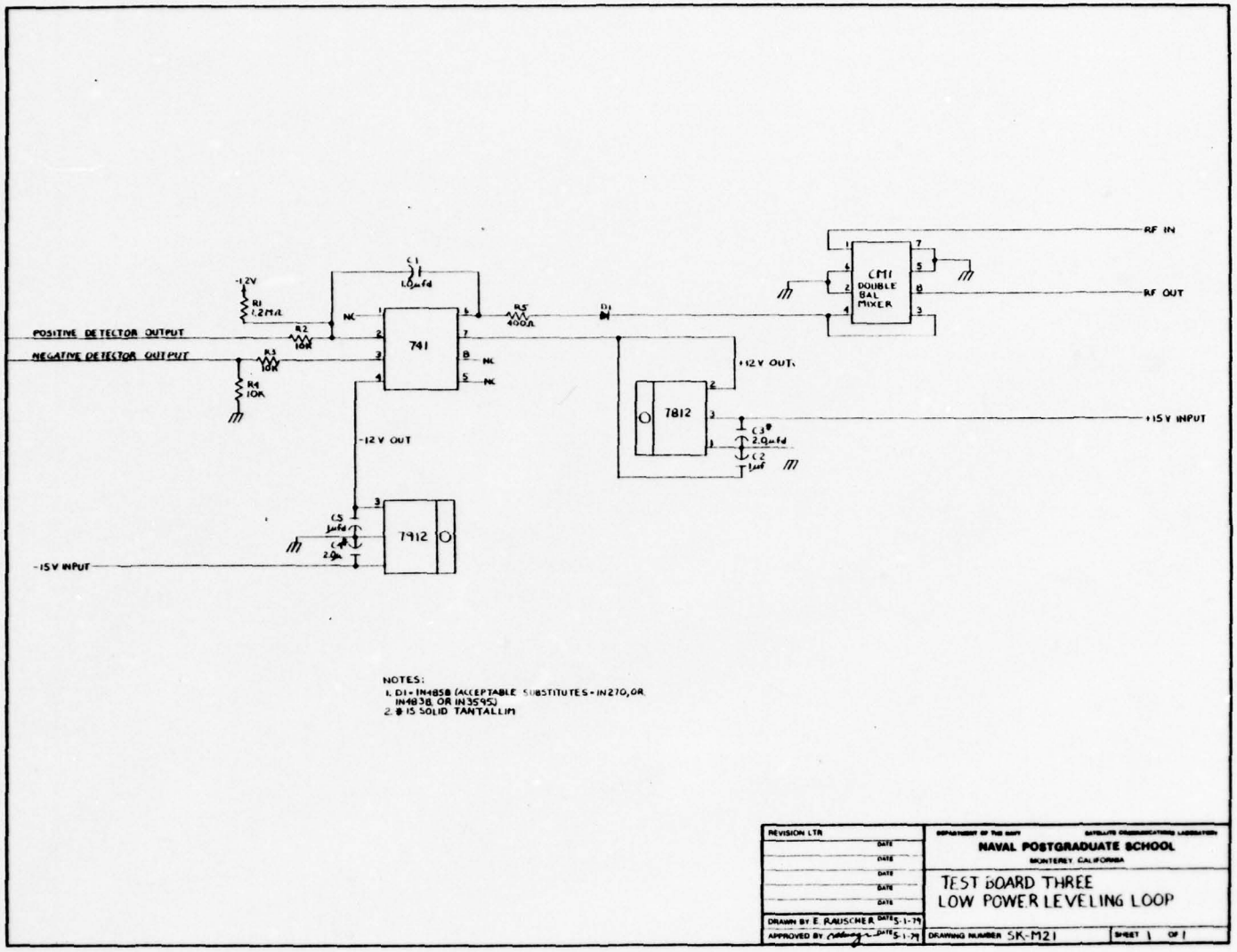


Figure 3.9

Test Board Three Low Power Leveling Loop

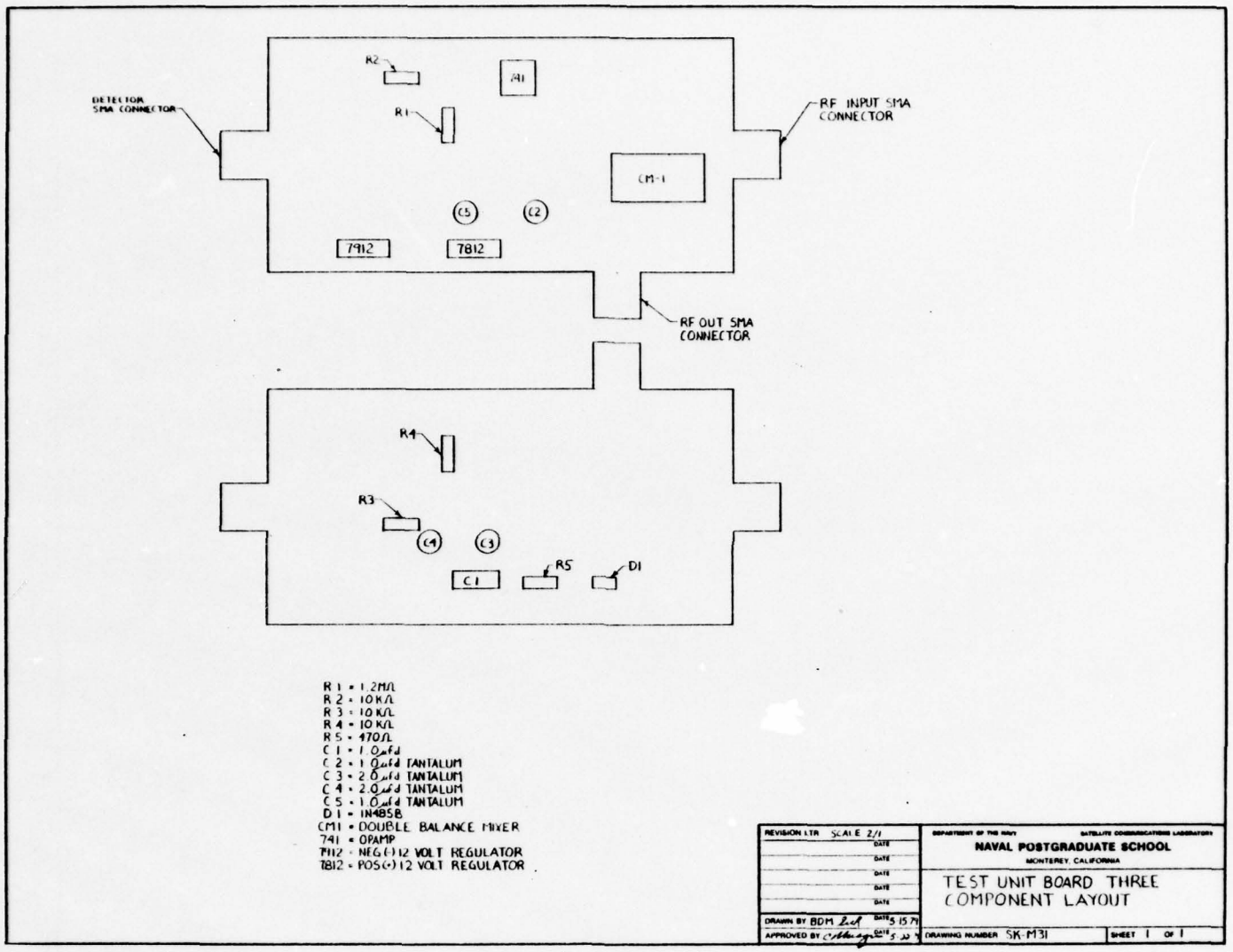
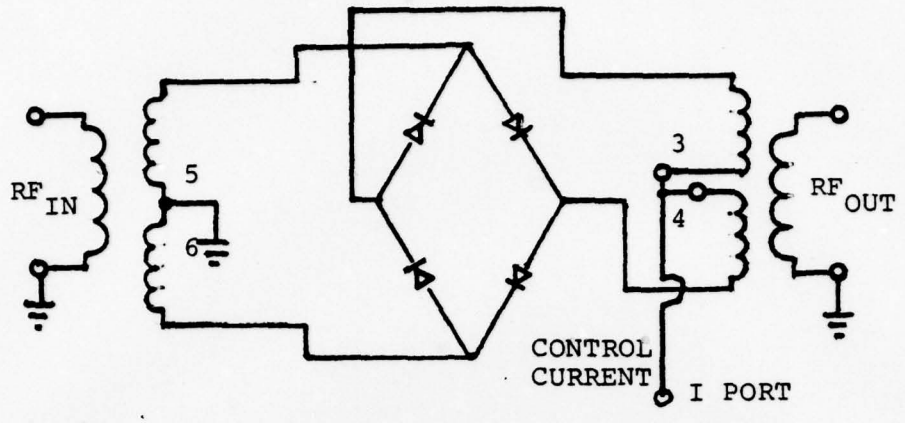
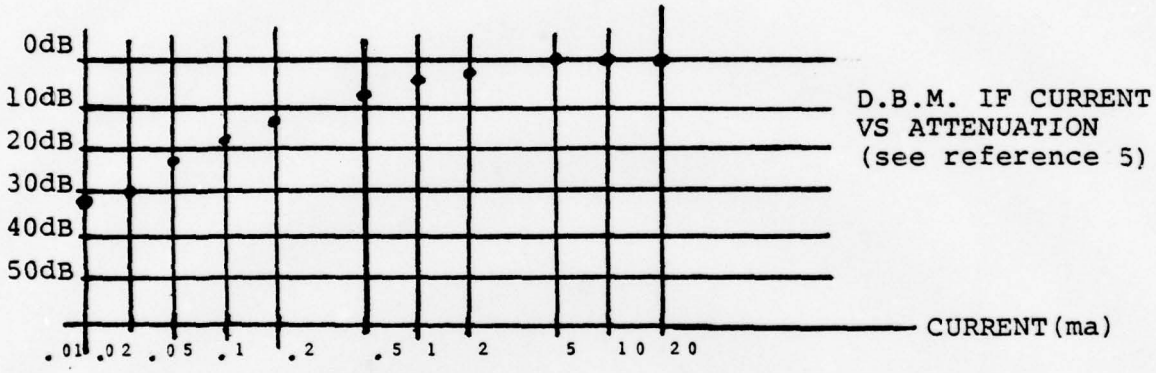


Figure 3.10

Test Board Three Component Layout





DBM ATTENUATION = RF_{OUT} - RF_{IN} in dB

This is the equivalent effect of a D.B.M. using current to change R and thereby changing the energy transfered from RF_{IN} to RF_{OUT}.

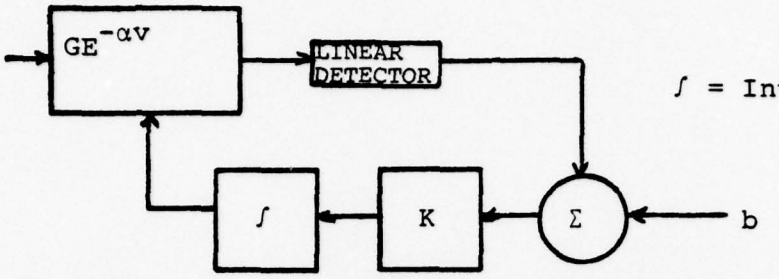
R = CURRENT CONTROLLED ATTENUATOR

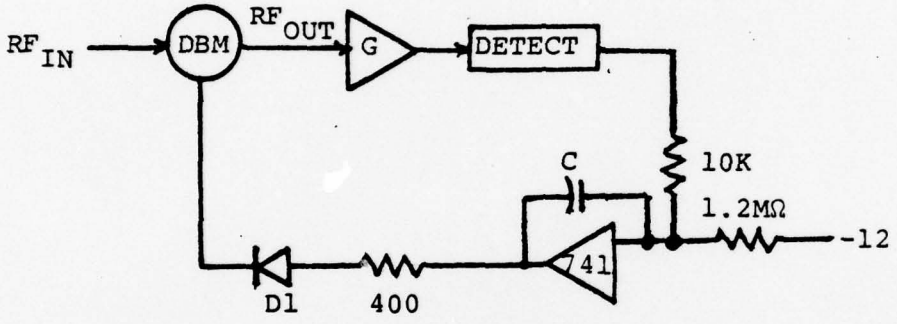
C = D.C. BLOCKING CAPACITORS

Figure 3.11
Double Balanced Mixer (DBM)

controlled attenuator. PIN 2 of the 741 on Figure 3.9 is a "VIRTUAL" ground so with .1VOLTS, from the detection thru 10KΩ, a current of 10μamps flows thru the 10KΩ resistor therefore, the 10μamps into the "virtual" ground must be nullified in order for the OPAMP to recognize a power increase and reduce the current into the DBM (so as to increase the attenuation) and correspondingly bring the power back down. The 1.2MΩ resistor, of Figure 3.9, tied between -12V and the virtual ground cause 10μamps to flow away from the "virtual" ground and thereby nullify the 10μamps into the "virtual" ground. Before proceeding to the question of how instantaneous changes in RF power are taken into account, one should observe the purpose of R5 and D1 in Figure 3.9. R5 is used only to limit the maximum current into the D.B.M. (12V÷400=25ma) and D1 is used to ensure the current does not flow out of the D.B.M. (i.e., limit the direction of current flow to one-way). The 7812 and 7912 of Figure 3.9 are THREE-TERMINAL REGULATORS which provide proper power supply voltages for the OPAMP. Now to consider the closed-loop response to instantaneous changes in power. Consider the system of Figure 3.12 with some gain (G), a response TIME (τ) to changes, an integrator and some reference voltage (b) [3].

The block diagram system and the one used in the LOW-POWER LEVELING LOOP are shown in Figure 3.12 and an abbreviated derivation of the closed loop response time is shown. Reference 3 has the detailed derivation for the block diagram system of Figure 3.12. One should notice that the gain K may





$\frac{K}{S} = (\frac{1}{CS10^4})(\frac{1}{400})$ b = .1 VOLTS

$K = \frac{1}{(C)(10^4)(400)} = \frac{2.5X10^{-7}}{C}$

α is determined by choosing the 1ma point on the graph in Figure 3.11. Now determine the slope at this point (8.7) dB/ma

$\alpha = \frac{10^4 dB/ma}{8.7 dB/ma} = 1149$ $\tau = \frac{1}{Kab} = (\frac{C}{2.5X10^{-7}})(\frac{1}{1149})(\frac{1}{.1})$

$\tau = 3.4 \times 10^4 C$ τ = CLOSED LOOP RESPONSE TIME CONSTANT

EXAMPLE: IF C = 1μfd τ = 34mSEC

Figure 3.12

Response Time Of Leveling Loop

be calculated, if desired, once the closed loop response time (i.e., the value of C) is determined. As a note, on Figure 3.9, C1 is 1.0μfd which makes the system response time = 34 mSEC as shown on Figure 3.12 and the gain (K) of the OPAMP i.e., K-.25.

E. PSEUDO-RANDOM SEQUENCE GENERATOR

A detailed explanation of the basic operation of pseudo-random sequence generation or of maximal-length sequences (MLS) will not be given here, but is contained in reference 4. However, the operation of TEST BOARD ONE MAXIMUM LENGTH SEQUENCE GENERATOR, Figure 3.13, will be covered. The component layout of TEST BOARD ONE is shown in Figure 3.14. The PSK modulate the RF power sent to the TEST SMTR section. This will allow the operator to observe the envelope of a PSK signal while doing system testing. The length of the MLS is $511(2^9-1)$ bits and the choice of sequence was made so it would be the same 511 bit sequence as the HEWLETT-PACKARD MODEL 1645A BIT ERROR RATE MEASUREMENT DEVICE. This is not a system component but is widely used for Navy bit error rate testing. Fibure 3.13 shows the schematic of the MLS generator. The clock for the 74164-U7 (SIPO) shift register and the 7474-U6 is derived from U1 a 19.2KHz CRYSTAL OSCILLATOR. U2, U3, U4 and U5 are 7474 flip-flops which are used to divide the 19.2 KHz into the CLOCK frequencies of 9.6KHz, 4.8KHz, 2.4KHz, 1.2KHz, 600Hz, 300Hz, and 75Hz. The selection of the clock is made by the CIB CLOBK SELECT BITS B0(LSB), B1, B2(MSB). The D (PIN 6) and H (PIN 13) outputs of its shift register

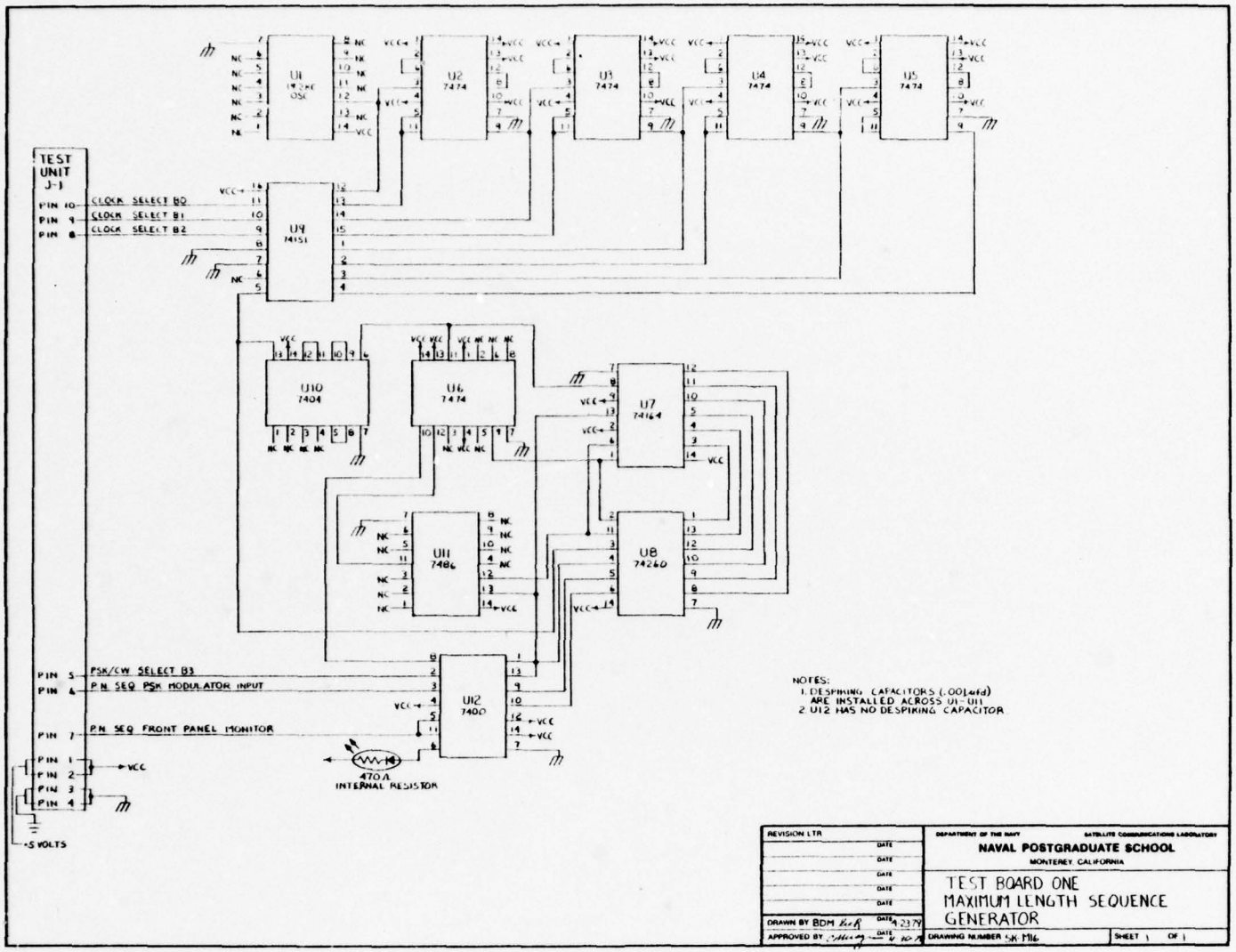


Figure 3.13

Test Board One Maximum Length Sequence Generator

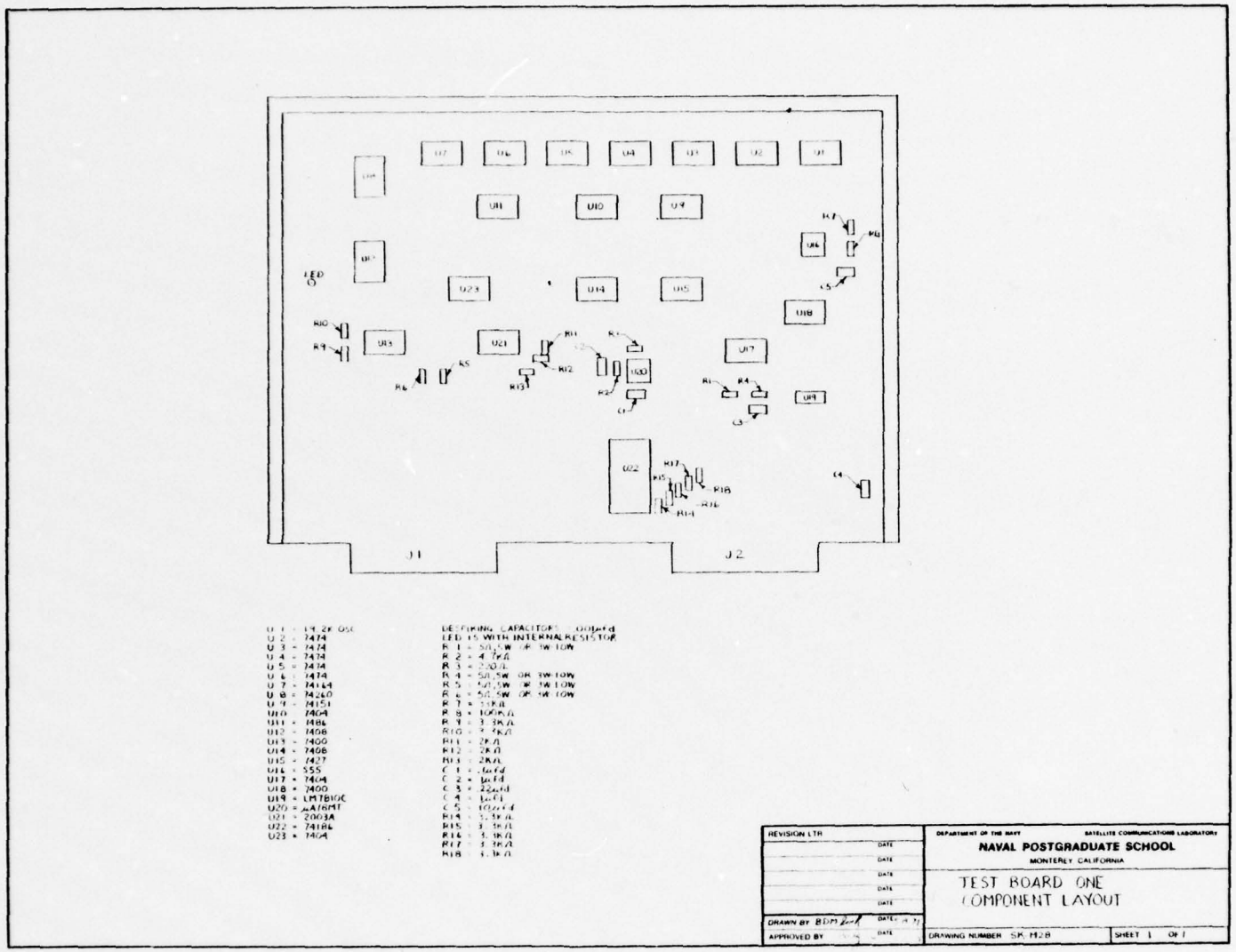


Figure 3.14

Test Board One Component Layout

U7-74164 are added together MODULO-TWO (EXOR) and the resultant output is used as the input PIN 12 of U6-7474 "D" TYPE FLIP-FLOP to produce the MAXIMUM LENGTH SEQUENCE. In order to prevent the MLS from sequencing into the all zeros state a comparison of each parallel output of the 74164-U7 and the output of U6-7474 PIN 9 is made. All of these are Nor'ed together in U8-74260 and the NAND'ed and tied to the set input of U6-7474 PIN 10. If the clock is low and the all zeros state is observed, the set line is brought low to change the output of U6 PIN 9 to a high value and restart the sequence. The CIB has the ability to select either the MLS to the MODULATOR (PSK) or no MLS to the MODULATOR (PSK) or no MLS to the MODULATOR (C.W.). The operator may observe the MLS at the BNC connector on the TEST UNIT FRONT PANEL or at the LED located on TEST BOARD ONE near U12.

F. RECEIVER TEST SECTION

The RCVR TEST SECTION at the TOP of Figure 3.8 receives the 240-270MHz, leveled, RF POWER signal from the LORCH SWITCH S2 "1", reduces the level 40dB with a fixed attenuator, reduces the level from 0 to 63dB with CIB programming and routes the signal from the LORCH SWITCH S3 to the locations necessary for injection of the RCVR TEST SIGNALS RT1, RT2, RT3. The large amount of attenuation is necessary so as to reduce the injected power to a level to which the receivers are capable of responding. It should be noted that the DAICO attenuators throughout the TEST UNIT require control voltages of 22V-30V. Therefore, C.I.B. control bits necessary

to change the attenuations are applied to the input of 2003 (+28V) DRIVERS on CMB1 (Appendix H) and then the output of the 2003 is applied to the attenuator. The control to select RCVR TEST (i.e., S2 "1") will be covered in the SELECTION AND LAMP SECTION.

G. TEST TRANSMITTER SECTION

The "2" output of LORCH SWITCH S2 on Figure 3.8 is amplified by the ZHL-1A to provide +20dBm input power of the WSC-5 AM6600 HIGH POWER AMP. With a gain of 30dB, the AM6600 is capable of sending 100W to the TRANSFER SWITCHES S7 and S8 and finally on to the antennas (i.e., signals XT1 or XT2) or to the DUMMY LOAD. A 100W TERMINATOR is attached to the portion of S8 to which power is not being routed to prevent signals from eminating to or from the unused line. The HIGH POWER LEVELING LOOP has the integrator and the D.B.M. contained in the AM6600. The coupler is used to sample the AM6600 output power and send a portion to the DAICO programmable attenuator. The ENGLEMAN DETECTOR converts the R.F. energy to a D.C. current which is sent directly to the AM 6600 in the AUTOMATIC MODE. In the MANUAL MODE the operator has control over the D.C. current sent to the AM6600. The HIGH POWER LOOP drives the H.P.A. so the detetor applies a fixed D.C. voltage level to the leveling part of the H.P.A. The maximum POWER OUT of the TEST XMTR occurs when the maximum attenuation has been placed in the loop; MAXIMUM CURRENT-MAXIMUM GAIN of AM6600. The minimum POWER OUT occurs when the minimum ATTENUATION has been inserted. the HIGH POWER LEVELING LOOP

remains to be calibrated (i.e., amount of power out for an inserted attenuation). The control to select the TEST XMTR will be covered in the next section as will the turning on and off of the AM6600 (RF KEYLINE). The wiring of switches S7 and S8 is covered in Appendix F.

H. SELECTION AND DISPLAY SECTION

The selection of the MARKER ON-OFF, the display of an INVALID FREQUENCY, and the control bits for SWITCH S4 (Figure 3.4) to select 60-90MHz MARKER, or 240-270 and 290-320MHz MARKER are contained on Figure 3.15. The MARKER ON and MARKER OFF switches are applied to U13-7400 which functions as a latch [2] to retain a signal corresponding to the closure of either switch. The "MARKER ON" is sent to U14 and NAND'ed with a low frequency clock (~1Hz) and sent to U21 for blinking the "MARKER ON" lamp. If the MARKER OFF SWITCH is pressed, the MARKER ON lamp is extinguished and the MARKER OFF signal from U13 goes directly to U21 to illuminate the MARKER OFF LAMP. If MARKER ON SWITCH has been pushed, the frequency selected by the THUMBWHEELS is valid, and a frequency of 60-90MHz is dialed on the THUMBWHEELS then SWITCH will be placed in the "2" position (i.e., PIN 14 of J1 is LOW). If a frequency of 240-270 or 290-320MHz is dialed on the THUMBWHEELS and all else is the same then S4 "1" (i.e., PIN 13 of J1) will be low. The LORCH SWITCHES are "ACTIVE-LOW" (NEGATIVE TRUE LOGIC). If either an INVALID FREQUENCY is dialed or the MARKER OFF button is pushed then both S4 control bits are HIGH shich eliminates the MARKER from the 7613. The FREQUENCY

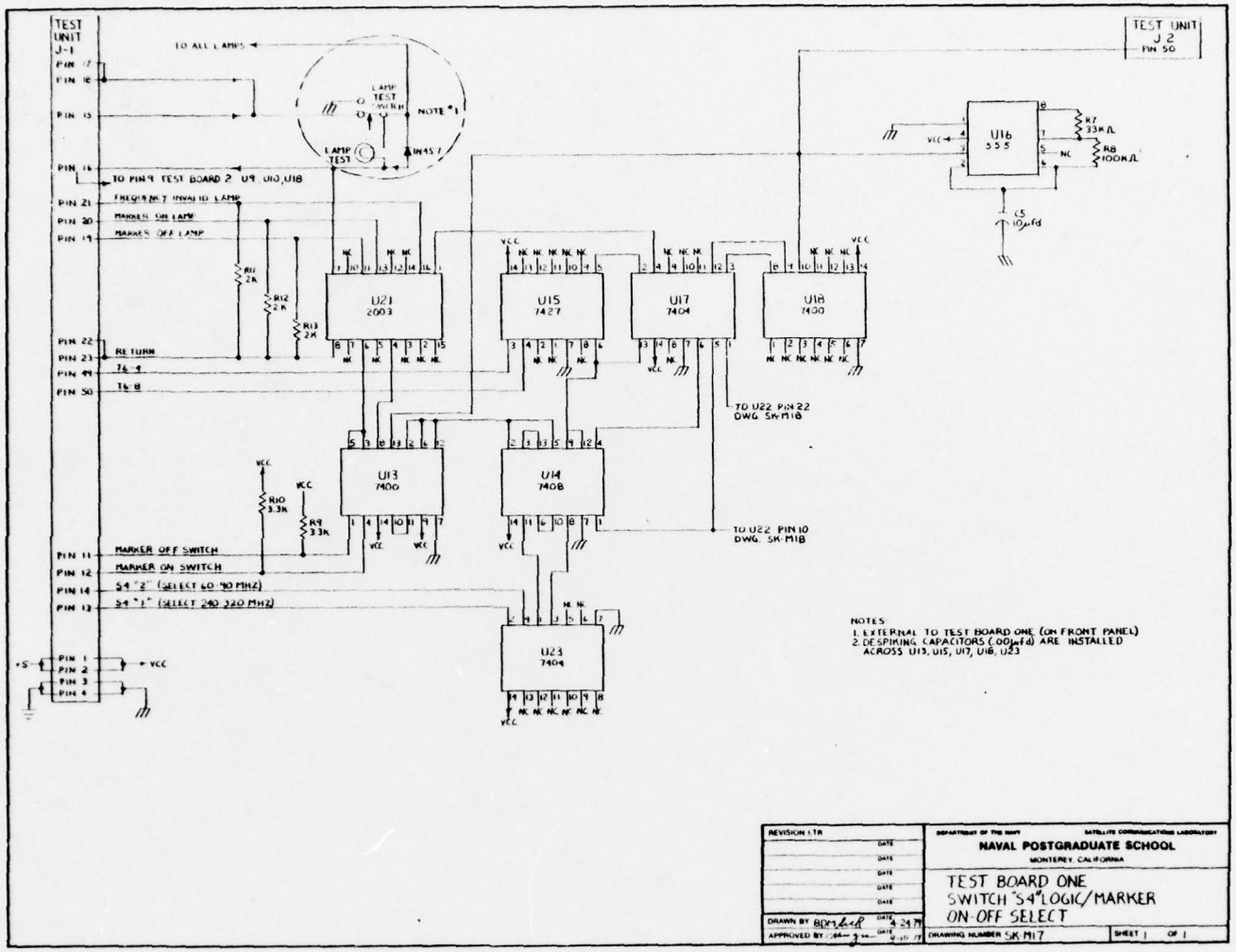


Figure 3.15

Test Board One Switch S4 Logic/Marker On-Off Select

INVALID is determined by observing the two most significant bits of the most significant THUMBWHEEL. If either of these is HIGH or if the signal on PIN 22 U22 (PROM) is LOW, then the frequency is not valid. The schematic for the lamp test switch is shown on Figure 3.15. Figure 3.16 is the component layout for TEST BOARD TWO.

The control of the signal which is displayed (RS1, RS2, RS3, X1, X2, RC1, RC2, RC3) on the 7613 is shown in Figure 3.17. The eight switches are connected to a priority encoder U1-74148 which puts out a 3 BIT address of the one of eight switches which has been pushed. U3-74175 latches the 3 bit address and sends the 3 bits to U6-74138 a 3 to 8 decoder. This decoder sends a LOW signal out on a line corresponding to the switch which had been pushed. This line remains LOW due to the latching of U3-74175. This low, through U7-7404 and U9-2003, illuminates the lamp under the pushed switch. The LOW signal is sent to LORCH SWITCHES S5 or S6 (ACTIVE LOW) to route the appropriate signal to the 7613. If one of RC1, RC2, or EC3 are selected, U5-7412 and U8-7404 cause the signal RC1, RC2, or RC3 to be routed through S5 thru S6 and into the 7613; Figure 3.4 shows this routing clearly. This selection of S5 or S6 is done by making the S6/S5 SWITCH TRANSITION LINE LOW.

The purposes of TEST BOARD TWO RCVR TEST AND TEST XMTR CONTROL, Figure 3.18, are to:

(1) provide control bits for the selection of RCVR TEST SIGNALS RT1, RT2, or RT3 (on SWITCH S3 Figure 3.8) and illuminate the RT1, RT2, or RT3 lamp.

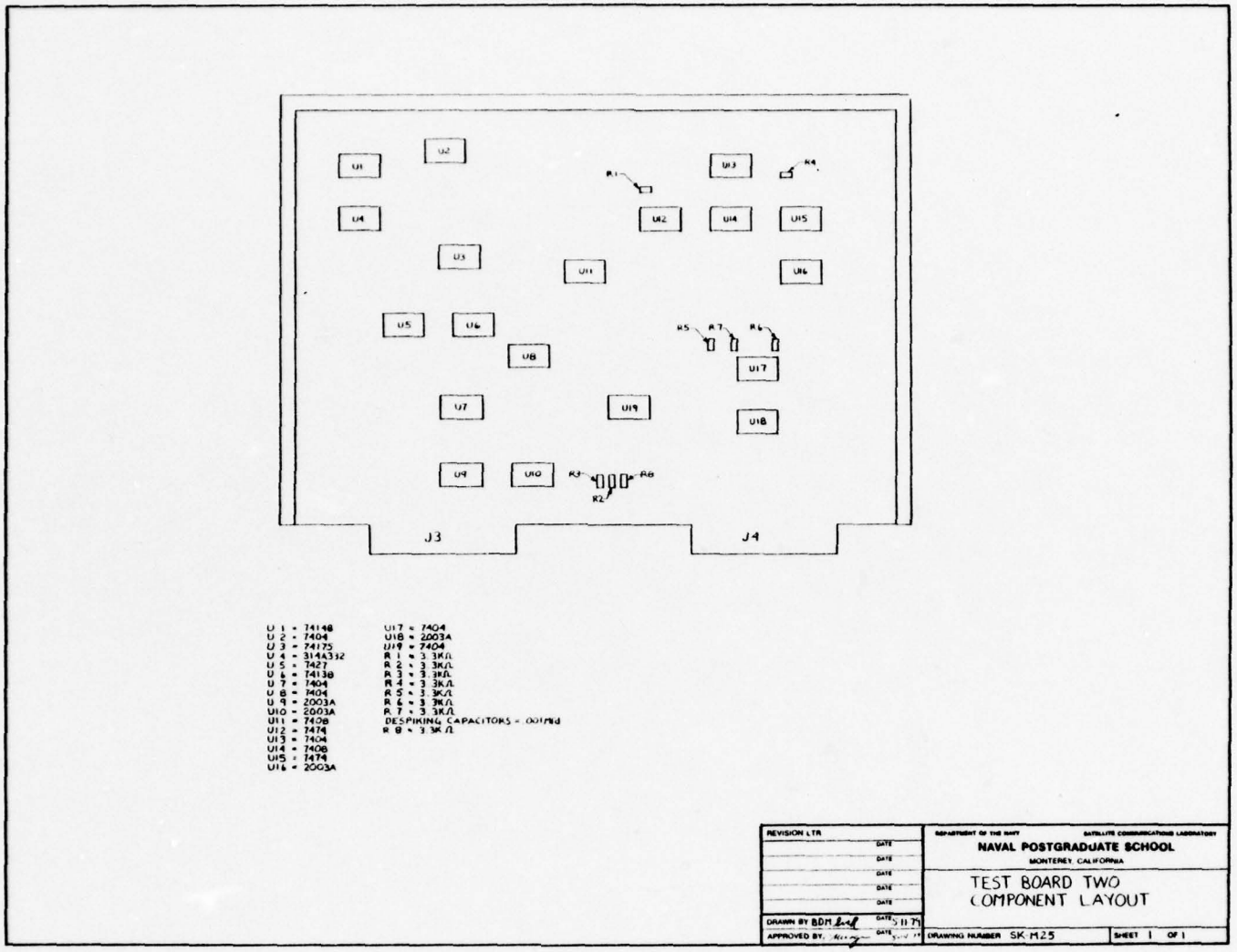


Figure 3.16

Test Board Two Component Layout

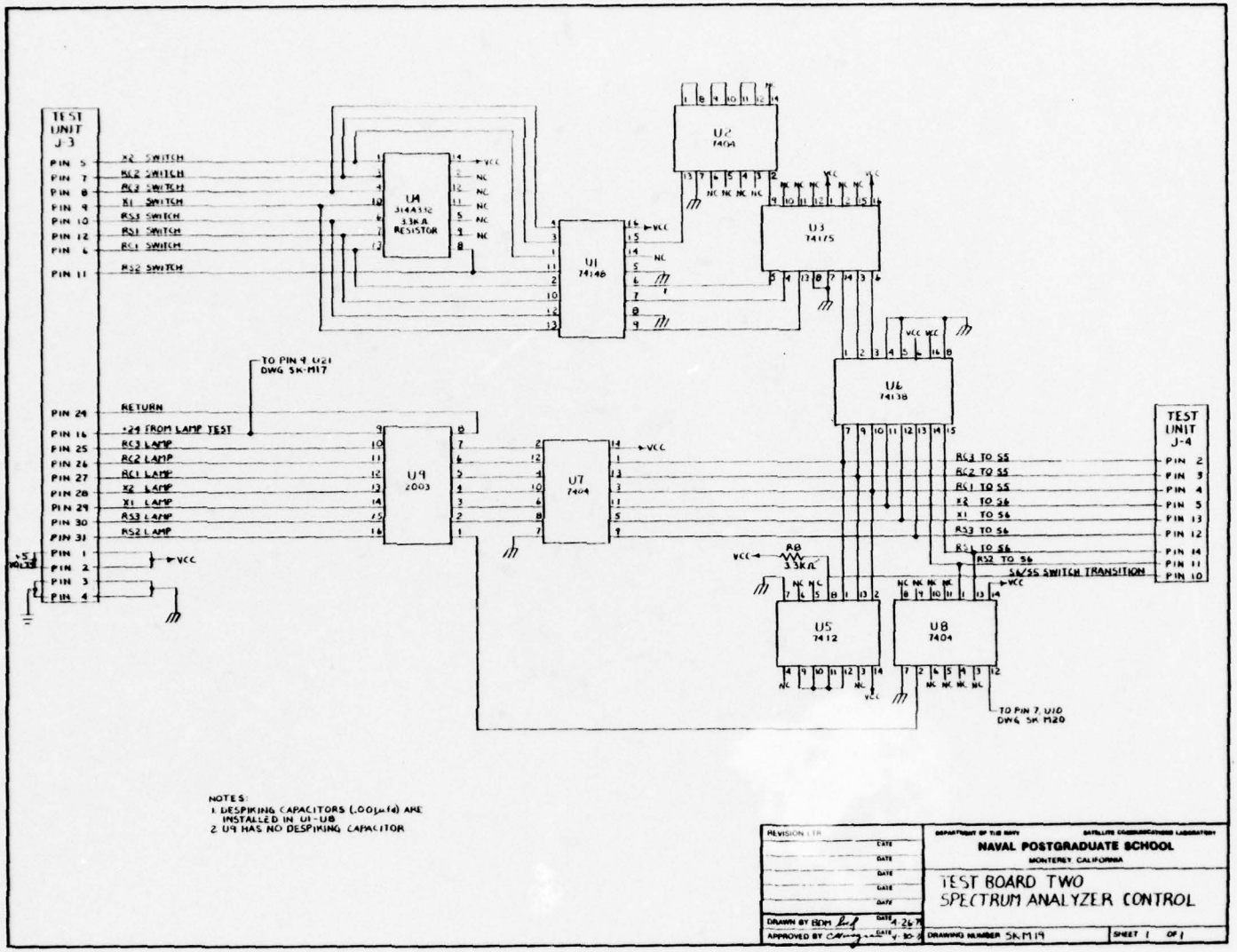


Figure 3.17

Test Board Two Spectrum Analyzer Control

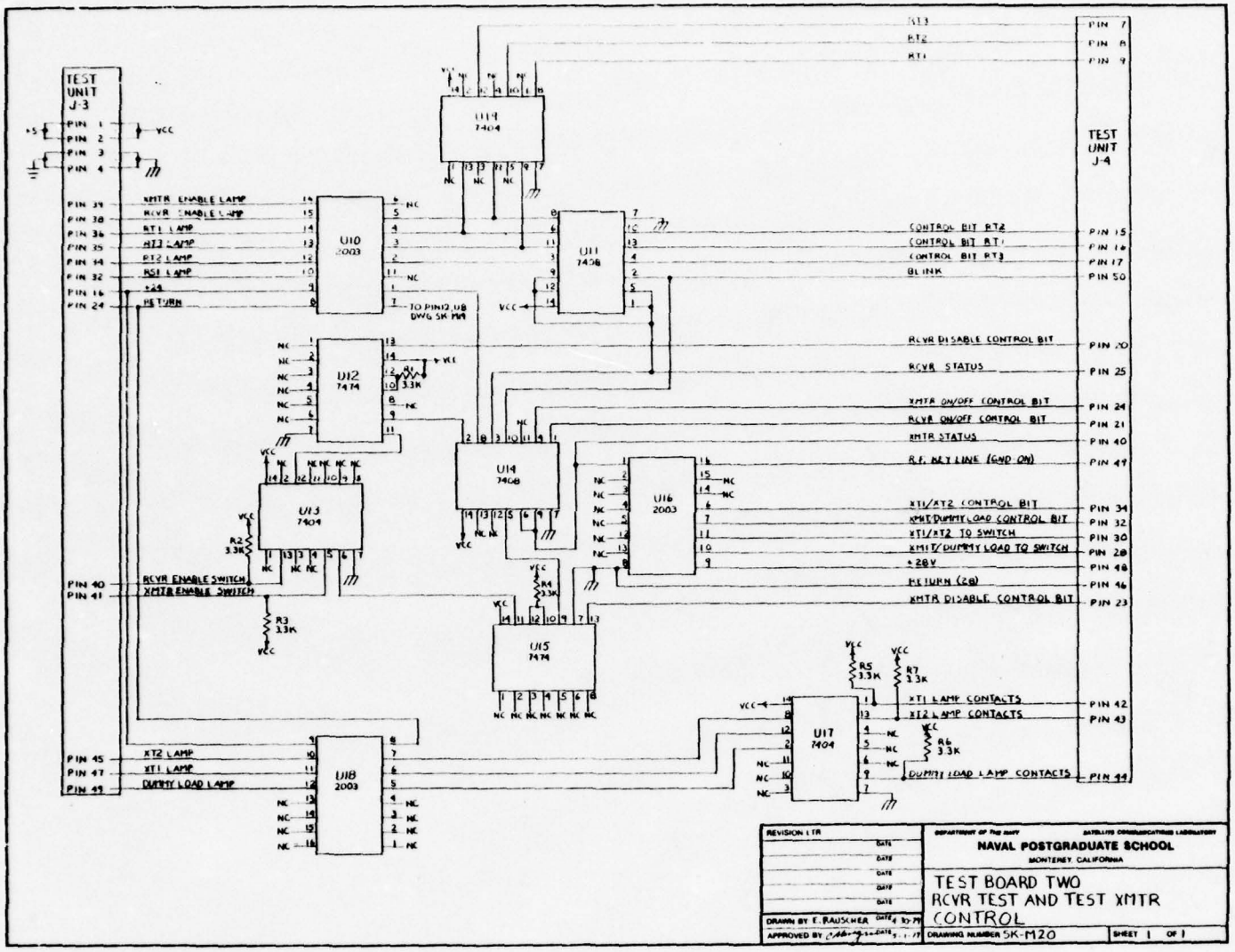


Figure 3.18

Test Board Two RCVR Test and Test XMTR Control

(2) provide control bits for the selection of RCVR TEST and blink the RCVR TEST ENABLE lamp.

(3) provide control bits for the selection of TEST XMTR and blink the TEST XMTR ENABLE lamp.

(4) provide control bits for the selection of XMIT or DUMMY LOAD and illuminate the DUMMY LOAD lamp if DUMMY LOAD selected or extinguish it if in XMIT.

(5) provide control bits for the selection of XT1 or XT2 and illuminate the XT1 or XT2 lamp.

(6) provide status for monitoring the RCVR TEST, TEST XMTR, XT1, XT2, XMIT, and DUMMY LOAD.

The CIB provides 3 bits to select RT1, RT2, or RT3 into U11-7408. U19-7404 is used to drive the appropriate line to SWITCH S3 low. The RT1, RT2, or RT3 lamp is illumianted by the appropriate line through U10-2003. The RCVR TEST must have three additional bits set HIGH before RT1, RT2, or RT3 control bits can activate any portion of S3. The RCVR ON/OFF CONTROL BIT and the RCVR DISABLE CONTROL BIT (both controlled by the CIB) both must be HIGH and, in addition, the operator must have selected the RCVR TEST by pressing the RCVR TEST ENABLE switch. If any one of these is not accomplished, then the RCVR TEST SIGNALS RT1, RT2, or RT3 will not be available. The TEST XMTR must have three bits set HIGH before the TEST XMTR RF KEYLINE is grounded which turns on the AM6600. The XMTR ON/OFF CONTROL BIT and the XMTR DISABLE CONTROL BIT (both controlled by the CIB) must be high and, in addition, the operator must have selected the TEST XMTR by

pressing the TEST XMTR ENABLE SWITCH. The XMIT/DUMMY LOAD select bit and the XT1/XT2 select bit comes from the CIB thru U16-2003 and back to S7 and S8 of Figure 3.8. The status of the RCVR TEST and the TEST XMTR (i.e., whether all three of the bits are HIGH) is routed to the input port of a DR11C in order that the computer may monitor both the RCVR TEST condition or the TEST XMTR condition. In addition a status line for XMIT, one for DUMMY LOAD and one for XT1/XT2 is also attached to the same DR11C to monitor the condition of switches S7 and S8.

I. KEY ENCODER AND LAMP MATRIX

The ability to have user defined push-buttons is a desireable feature and has been implemented as shown in Figures 3.19 and 3.20. The KEY ENCODER MM5740AAD on Figure 3.19 manufactured by National Semi Conductor Corp. is capable of producing an eight bit code for input to a DR11C, based on the closure of switch contacts connected to J3. The 7414-U19 is a Schmitt trigger which clocks the 5740 every 30 mSEC so the ENCODER scans X1-X9 and Y1-Y10 for a closure. Proper handshaking lines to and from the DR11C are also provided; DATA STROBE OUTPUT and DATA XMITTED. Based on which switch is closed, KEYBOARD PARSING SUBROUTINES will be written to react to any code (key closure) which is placed into the DR11C from the 5740. In order to light the lamp beneath the switch, which had been pressed, the DR11C provides an output to J1 on Figure 3.19. Each pin of J1 will receive 7 consecutive bits of information which are loaded serially into

the 74164 and provided to the 2003 in parallel which lights the appropriate lamp. The LAMP TEST SWITCH is provided. CONNECTOR AN1 is used to bus +28 VOLTS onto the key encoder and lamp matrix board.

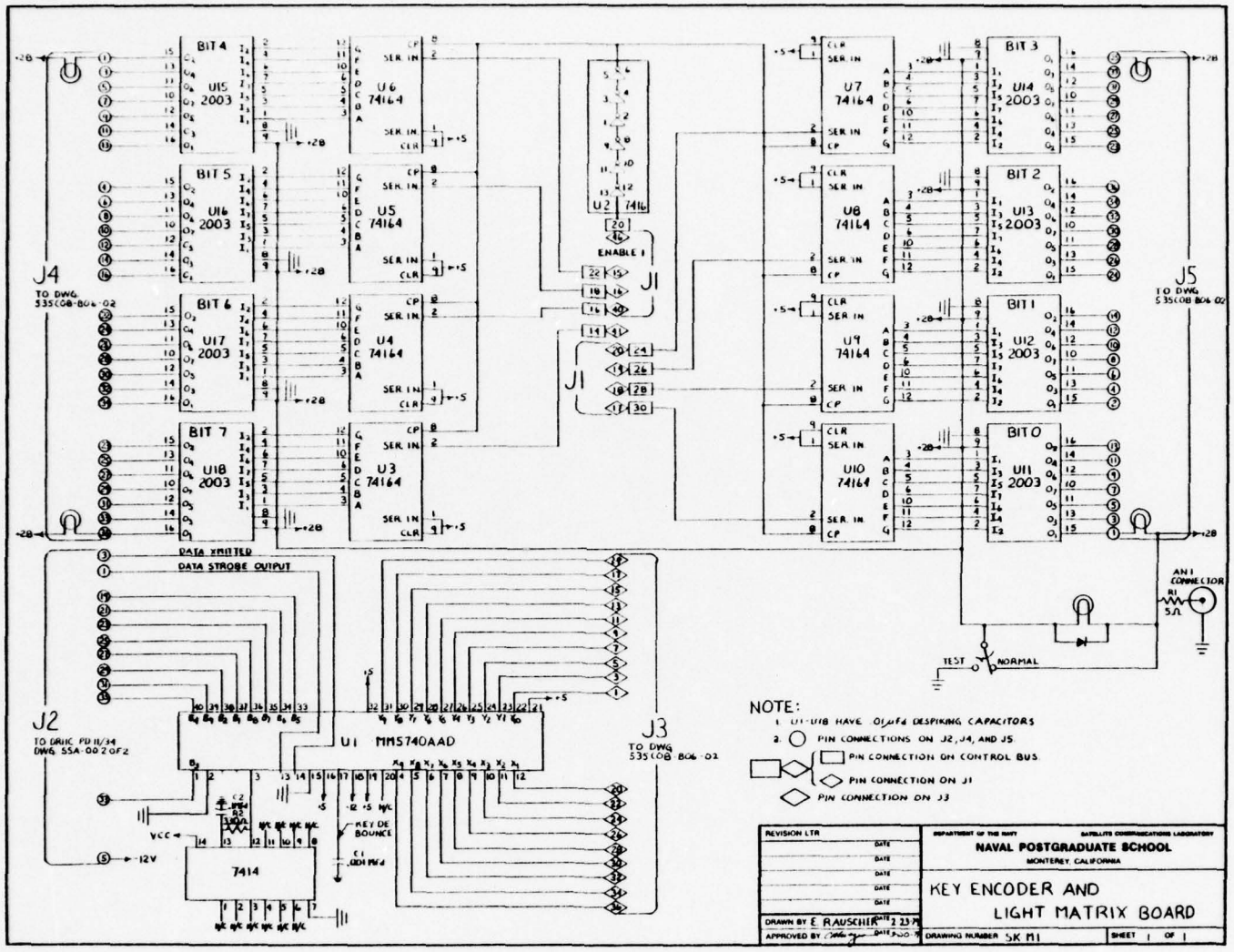


Table 3.19

Key Encoder and Light Matrix Board Schematic

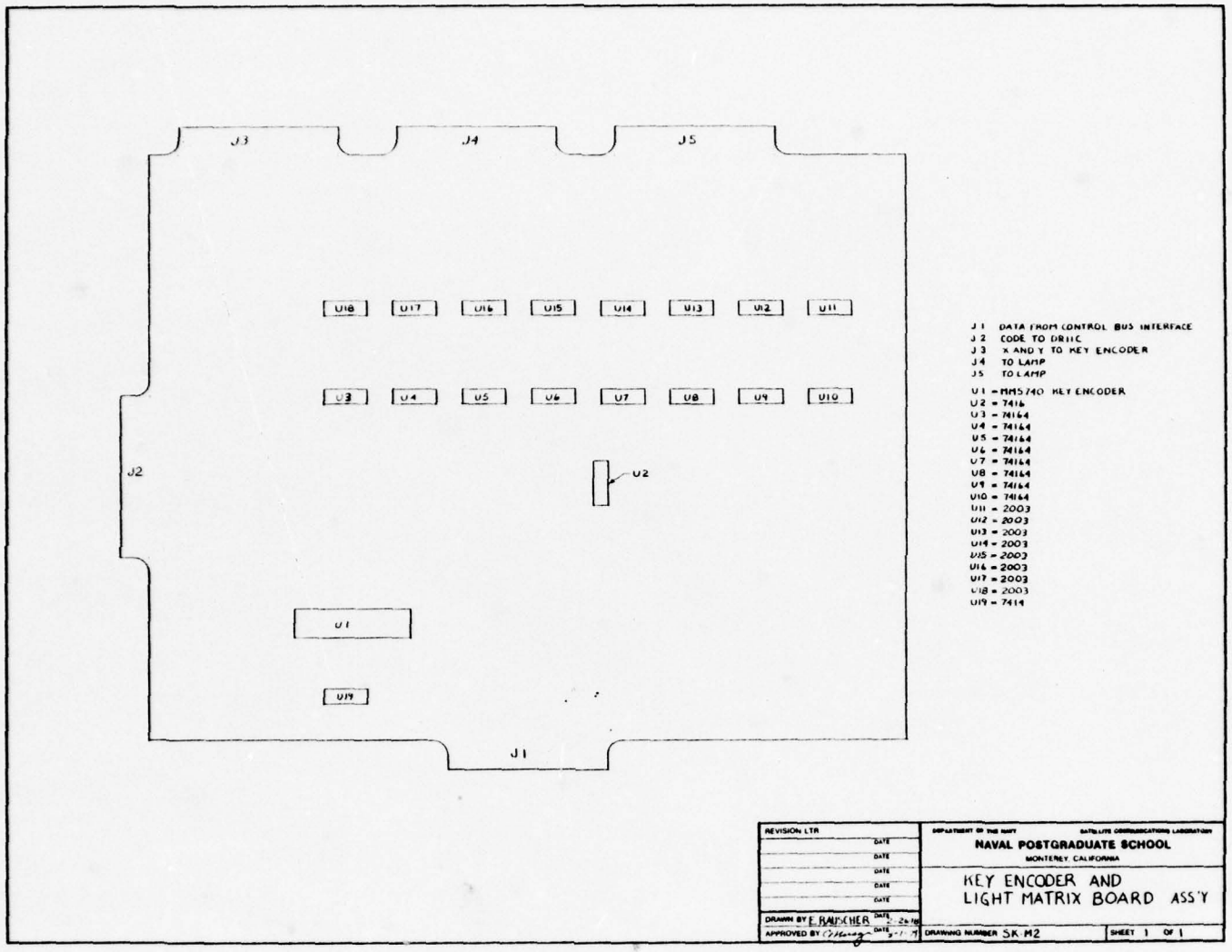
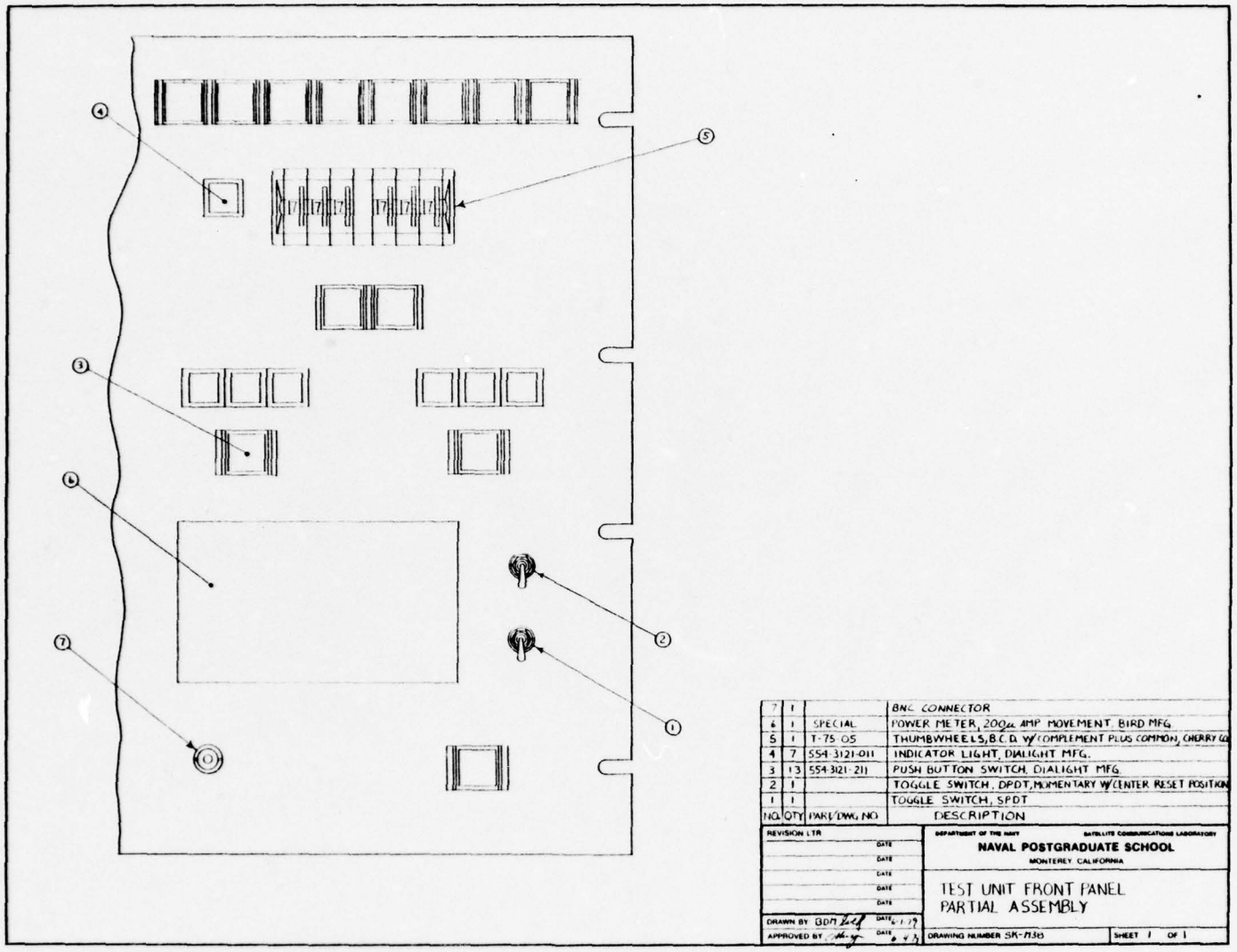


Figure 3.20

Key Encoder and Light Matrix Board Component Layout



NO.	QTY	PART/DWG. NO.	DESCRIPTION
7	1		BNC CONNECTOR
6	1	SPECIAL	POWER METER, 200μ AMP MOVEMENT, BIRD MFG.
5	1	T-75 05	THUMBWHEELS, B.C.D. W/COMPLEMENT PLUS COMMON, CHERRY CO.
4	7	554-3121-011	INDICATOR LIGHT, DIALIGHT MFG.
3	13	554-3121-211	PUSH BUTTON SWITCH, DIALIGHT MFG.
2	1		TOGGLE SWITCH, DPDT, MOMENTARY W/CENTER RESET POSITION
1	1		TOGGLE SWITCH, SPDT

REVISION LTR	DATE
DRAWN BY BDM	DATE 6/1/79
APPROVED BY	DATE 6/1/79

DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

TEST UNIT FRONT PANEL
PARTIAL ASSEMBLY

DRAWING NUMBER SK-1136 — SHEET 1 OF 1

Figure 3.21

Test Unit Front Panel Layout

IV. FUTURE CONSIDERATIONS

As previously discussed, the SPECTRUM ANALYZER section of the TEST UNIT is capable of monitoring eight signals: RS1, RS2, RS3, X1, X2, RC1, RC2, and RC3. The major factors limiting the number of signals monitored are U174148 (8 to 3 line PRIORITY ENCODER), U374175 (LATCH) and U674138 (3 to 8 line DECODER). If ONE 74147 (10 to 4 line PRIORITY ENCODER), the 74175 (LATCH) and a 7443 (4 to 10 line DECODER) were used, the SPECTRUM ANALYZER section would be capable of monitoring up to 10 signals by merely changing the size of S5 and S6 to 6 WAY SWITCHES (EACH). An additional lamp driver 2003 would be required as would additional switches on the front panel. One additional caution should be mentioned about the SM160 in the SPECTRUM ANALYZER section. The SM160 installed receives an external standard of 1 MHz for stability and does not use the internal 1MHz crystal oscillator. The caution - one should insure the jumper, normally installed by the factory and required for the internal 1MHz, is removed in order for the external 1MHz to operate the SM160. Another possible future change to the test unit, the TEST XMTR could be modified to transmit to all three antennas instead of the two presently used. An additional transfer SWITCH S9 (not shown on Figure 3.8) could be added (plus a 100W terminator) to allow power to be routed to XT3. SWITCH S7 would still be switching to XMIT or DUMMY LOAD while SWITCH S8 would be used to switch

between XT1 or XT2/XT3. SWITCH S9 would switch between XT2 or XT3. Sufficient control bits are available in BYTE 1 of BYTE 0 of Appendix F.

Appendices G thru T and EE are valuable in order to construct similar TEST UNITS.

Resistors R1 and R2 of TEST BOARD ONE (Figure 3.5) should be moved to a position external to TEST BOARD ONE to allow sufficient cooling of these resistors.

TEST BOARD FOUR (Figure 3.6) may be eliminated by placing pull-up resistors on TEST BOARD TWO (Figure 3.17 and 3.18).

V. CONCLUSIONS

The DIGITAL CONTROL and TEST UNIT subsystems for the Satellite Signal Analyzer System have been designed and constructed and are ready for use with the remainder of the system to be built. The digital control subsystems is capable of controlling all digitally programmable devices in the S.S.A. The fifteen CIB's with the 32 bits each allowed sufficient control for all applications (RF UNITS, SYNTHESIZERS, ETC.). The TEST UNIT is capable of monitoring RS1, RS2, RS3, RC1, RC2, RC3, X1, and X2, injecting RT1, RT2, RT3 into the "FRONT-END" of the receivers, making "round-trip" measurements thru the satellite and measuring the Noise Figure/ Temperature of the receivers.

APPENDIX A

TEST PROCEDURE FOR CONTROL INTERFACE BOARD

A. PDP 11/34 CONTROL

1. Attach Device Simulator (Light Board) to C.I.B. in question
2. Turn PDP 11/34 to On
3. Push Control & Halt/SS simultaneously (PDP 11/34) to stop CPU
4. Push Control & Boot simultaneously to obtain "Monitor" on screen
5. Type L_{Λ} 167772* (loads CIB address)
6. Type E_{Λ} → (Examine)
7. Type D_{Λ} $X_7X_6X_5X_4X_3X_2$ *

	4 2 1	4 2 1			
D7	D6 D5 D4	D3 D2 D1	D0 - -	S3 S2 S1	S0 A1 A0
Y_7	Y_6 Y_5 Y_4	Y_3 Y_2 Y_1	Y_0 0 0	Q_3 Q_2 Q_1	Q_0 R_1 R_0

$X_7 = Y_7$

$X_6 = Y_6(4) + Y_5(2) + Y_4(1)$

$X_5 = Y_3(4) + Y_2(2) + Y_1(1)$

$X_4 = Y_0(4) + 0 + 0$

$X_3 = Q_3(4) + Q_2(2) + Q_1(1)$

$X_2 = Q_0(4) + R_1(2) + R_0(1)$

See example on figure

8. Observe Device Stimulator
9. Repeat Steps 6, 7, and 8 as desired

Alternate E's and D's to ensure PDP 11/34 communicates with C.I.B. only. If E's and D's are not alternated, the address to which the PDP 11/34 is communicating will increment by one. In order to return to address 167772, one must start at Step (1).

NOTE: Λ = Space Bar

* = Carriage return

APPENDIX B

MANUAL CIB TEST PROCEDURES WITHOUT PDP 11/34

1. Attach Device Simulator (Light Board) to C.I.B. in question
2. Attach Computer Simulator to C.I.B. Driver Board
3. Set Dip Switches on Computer Simulator as desired
4. Press New Data Ready
5. Observe Device Simulator
6. Repeat Steps 3, 4, and 5 as desired

APPENDIX C

THUMBWHEEL OPERATION

CHERRY MFG, CORP.
THUMBWHEEL SERIES -T-75-05
WITH COMPLEMENT + COMMON

These thumbwheels provide a Binary-Coded-Decimal (BCD) code for each position 0-9. Four COMPLEMENT outputs are provided which either make a connection from one of the outputs to ground or makes no connection. The pull-up resistors attached to the thumbwheel outputs (Figures 3.6 and 3.7) will make the lines to the SM160 TEST BOARD ONE and the PROM be a HIGH value when the thumbwheel does not pull the line to ground, thereby defining a high when the output makes no connection and a low when the output makes a connection to ground.

APPENDIX D

PROM PROGRAMMING

74186 FUZEABLE LINK PROM
64 WORDS X 8 BITS

PROM ADDRESS (HEX)	PROM OUTPUT (HEX)
06	31
07	39
08	41
09	49
24	31
25	39
26	41
27	49
29	89
30	91
31	99
32	A1

ALL OTHER PROM ADDRESSES HAVE PROM OUTPUT = 00 (HEX)

74186 = TEXAS INSTRUMENT PROM

NOTE: ADF = MOST SIGNIFICANT BIT OF THE PROM ADDRESS
D08 = MOST SIGNIFICANT BIT OF THE PROM OUTPUT
PROM = POSITIVE TRUE LOGIC
HEX = HEXADECIMAL CODING

PROGRAMMING MAY BE ACCOMPLISHED WITH A PRO-LOG CORP PM-9055.

APPENDIX E

TEST UNIT CIB PROGRAMMING
(page 1 of 2)

BYTE 3	D7	1 = CW 0 = PSK
	D6	BIT 2 (MSB) CLOCK SELECT FOR MLS
	D5	BIT 1 CLOCK SELECT
	D4	BIT 0 (LSB) CLOCK SELECT
	D3	0 = AT1-16 1 = NO ATTENUATION
	D2	0 = AT1-8 1 = NO ATTENUATION
	D1	0 = AT1-4 1 = NO ATTENUATION
	D0	0 = AT1-2 1 = NO ATTENUATION
BYTE 2	D7	1 = RT2 SELECT 0 = NO SELECT
	D6	1 = RT1 SELECT 0 = NO SELECT
	D5	1 = RT3 SELECT 0 = NO SELECT
	D4	0 = AT1-1 1 = NO ATTENUATION
	D3	0 = AT2-16 1 = NO ATTENUATION
	D2	0 = AT2-16 1 = NO ATTENUATION
	D1	1 = RCVR TEST ON 0 = RCVR TEST OFF
	D0	1 = RCVR ENABLE 0 = RCVR TEST DISABLE
BYTE 1	D7	1 = TEST XMTR ON 0 = TEST XMTR OFF
	D6	1 = TEST XMTR ENABLE 0 = TEST SMTR DISABLE
	D5	1 = XMIT (S7) 0 = DUMMYLOAD (S7)
	D4	1 = XT1 (S8) 0 = XT2 (S8)
	D3	0 - NOT CONNECTED
	D2	0 - NOT CONNECTED
	D1	1 = S1"1" 0 = S2"1"
	D0	1 = S1"2" 0 = S2"2"

BYTE 0	D7	0 = AT3-16	1 = NO ATTENUATION
	D6	0 = AT3-8	1 = NO ATTENUATION
	D5	0 = AT3-4	1 = NO ATTENUATION
	D4	0 = AT3-2	1 = NO ATTENUATION
	D3	0 = AT3=1	1 = NO ATTENUATION
	D2	0 - NOT CONNECTED	
	D1	0 - NOT CONNECTED	
	D0	0 - NOT CONNECTED	

D7 = MSB

D0 = LSB

AT 1 AND AT2 ARE ATTENUATORS USED IN THE RCVR TEST OF FIGURE 3.8

AT 3 IS AN ATTENUATOR USED IN THE HIGH POWER LEVELING LOOP OF THE TEST XMITTER ON FIGURE 3.8

S1 AND S2 ARE SHOWN ON FIGURE 3.8

APPENDIX F

WIRING OF SWITCHES S7 AND S8

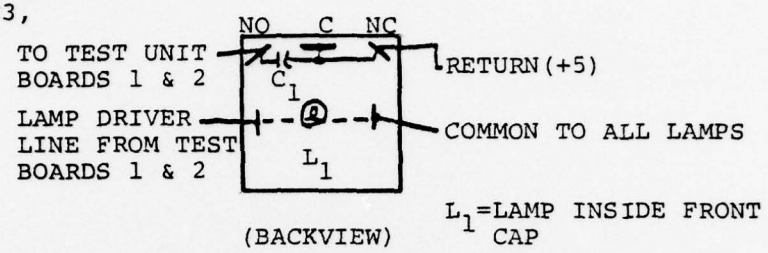
The transfer switches S7 and S8 manufactured by TELEDYNE MICROWAVE ARE SPDT switches with four ports designed to switch a common input between either of two outputs. The switch is activated by two control bits applied to the "1" and "2" terminals from the CIB thru a 2003 DRIVER. In the failsafe position (DUMMYLOAD for S7) port J1 is connected to J2 and J3 to J4. In the energized position (+28V on "1" with respect to "2") J1 is connected to J3 and J2 to J4.

Each switch contains indicator terminals labeled A, B, and C. The terminals were used to indicate the status of each switch to the PDP 11/34 and to illuminate the appropriate lamp on the front panel of the test unit. In the failsafe position (DUMMYLOAD for S7) terminal C is connected to terminal A. In the energized position (XMIT) terminal C is connected to B.

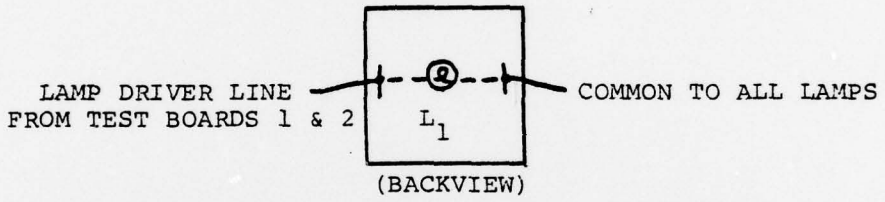
APPENDIX G

TEST UNIT FRONT PANEL
SWITCHES/INDICATORS WIRING DIAGRAM

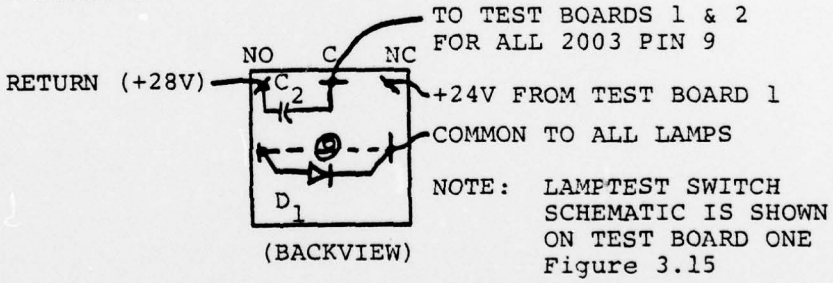
FOR ALL SWITCHES:
RC1, RC2, RC3,
X1, X2, RS1,
RS2, RS3,
TEST XMTR
ENABLE.



FOR ALL INDICATORS: RT1, RT2, RT3, XT1, XT2, DUMMYLOAD, FREQUENCY INVALID



FOR LAMP TEST SWITCH:



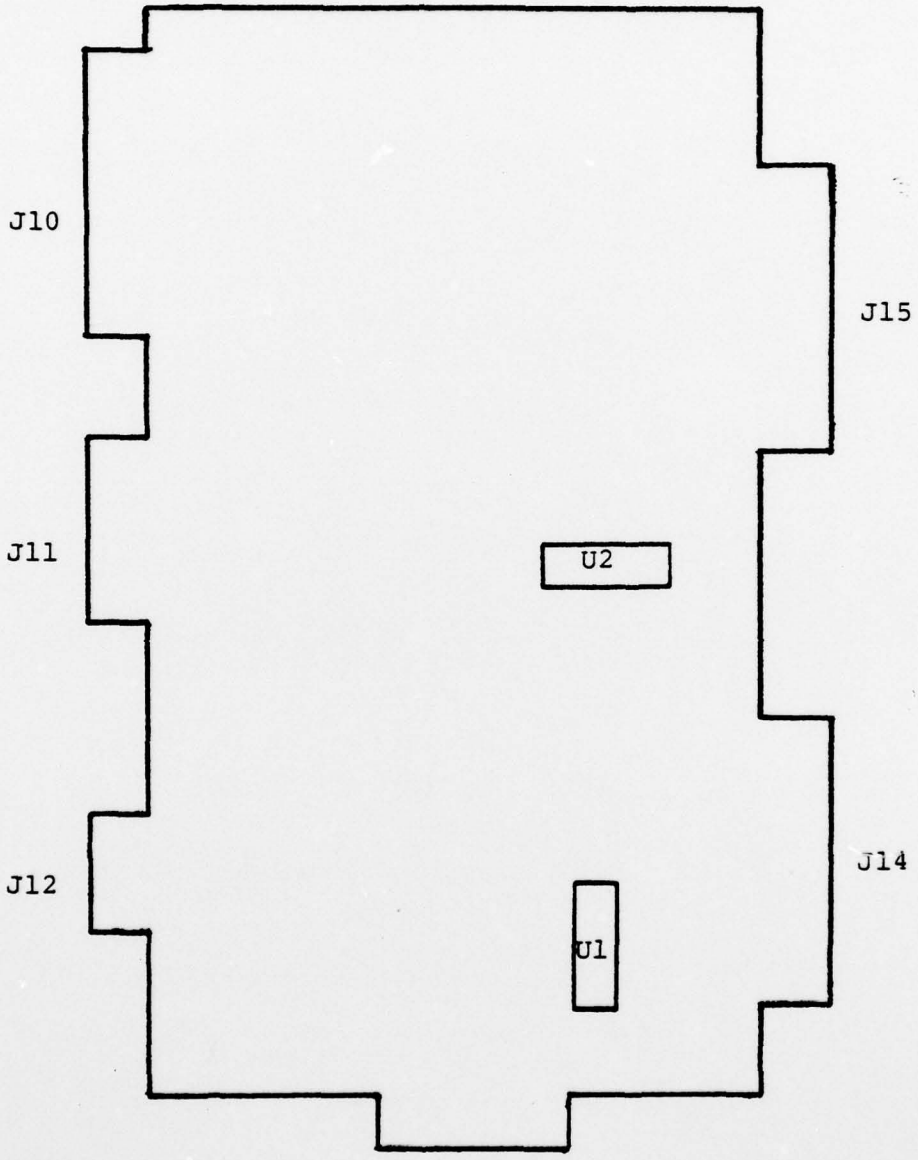
NO = NORMALLY OPEN TO C

NC = NORMALLY CLOSED TO C

$C_1=C_2=.001\mu fd$

APPENDIX H

TEST UNIT CMB1 LAYOUT DRAWING



APPENDIX I

TEST UNIT CONNECTORS

DESIGNATION	DESCRIPTION	MFG PART #
J1	50 PIN ANSLEY 1/10" CENTERS	609-5005M
J2	50 PIN ANSLEY 1/10" CENTERS	609-5005M
J3	50 PIN ANSLEY 1/10" CENTERS	609-5005M
J4	50 PIN ANSLEY 1/10" CENTERS	609-5005M
J5	44 PIN TRWCINCH .156" CENTERS	225-21821-401-117
J6	50 PIN AMPHENOL .156" CENTERS	57-40500
J7	50 PIN AMPHENOL .156" CENTERS	57-40500
J8	50 PIN AMPHENOL .156" CENTERS	57-40500
J9	NOT USED	
J10	50 PIN ANSLEY 1/10" CENTERS	609-5005M
J11	34 PIN ANSLEY 1/10" CENTERS	609-3415M
J12	16 PIN ANSLEY 1/10" CENTERS	609-1615M
J13	44 PIN AMPHENOL .156" CENTERS	225-21821-401-117
J14	50 PIN ANSLEY 1/10" CENTERS	609-5015M
J15	40 PIN ANSLEY 1/10" CENTERS	609-4015M

APPENDIX J

TEST UNIT WIRING-TABLE 1 (Page 1 of 4)

PINS OF TEST UNIT J1	PINS OF TEST UNIT J6	COLOR WIRE	PURPOSE OF J6 PINS
1	1	BROWN	+5 VOLTS to J8 PIN 1
2	26	WHITE-BLACK-VIOLET	+5 VOLTS to J8 PIN 26
3	2	RED	RETURN(+5) to J8 PIN 2
4	27	WHITE-BLACK-GRAY	RETURN(+5) to J8 PIN 27
5	3	ORANGE	B3(MLS) ON/OFF CONTROL to J8 PIN 8
6	28	WHITE-BROWN-RED	MLS to BNC CONNECTOR
7	4	YELLOW	MLS to PSK MOD
8	29	WHITE-BROWN-ORANGE	B2(MLS) CLOCK SELECT to J8 PIN 9
9	5	GREEN	B1(MLS) CLOCK SELECT to J8 PIN 3
10	30	WHITE-BROWN-YELLOW	B0(MLS) CLOCK SELECT to J8 PIN 4
11	6	BLUE	MARKER OFF SWITCH
12	31	WHITE-BROWN-GREEN	MARKER ON SWITCH
13	7	VIOLET	SWITCH S4 "1" to J8 PIN 6
14	32	WHITE-BROWN-BLUE	SWITCH S4 "2" to J8 PIN 7
15	8	GRAY	LAMPTEST SWITCH

TEST UNIT WIRING-TABLE 1 (Page 2 of 4)

PINS OF TEST UNIT J1	PINS OF TEST UNIT J6	COLOR WIRE	PURPOSE OF J6 PINS
16	33	WHITE-BROWN-VIOLET	TO PIN 9 2003's
17	9	WHITE	LAMPTEST SWITCH
18	34	WHITE-BROWN-GRAY	LAMPTEST SWITCH
19	10	BLACK	MARKER OFF LAMP
20	35	WHITE-RED-ORANGE	MARKER ON LAMP
21	11	WHITE-BROWN	FREQ INVALID LAMP
22	36	WHITE-RED-YELLOW	RETURN (+28V) to J8 PIN 36
23	12	WHITE-RED	RETURN (+28V) to J8 PIN 12
24	37	WHITE-RED-GREEN	+28 VOLTS to J8 PIN 11
25	13	WHITE-ORANGE	+28 VOLTS to J8 PIN 35
26	38	BROWN	*
27	14	WHITE-YELLOW	THUMBWHEEL T1 (LSD) $\overline{1}$
28	39	RED	THUMBWHEEL T1 (LSD) $\overline{2}$
29	15	WHITE-GREEN	THUMBWHEEL T1 (LSD) $\overline{4}$
30	40	ORANGE	THUMBWHEEL T1 (LSD) $\overline{8}$

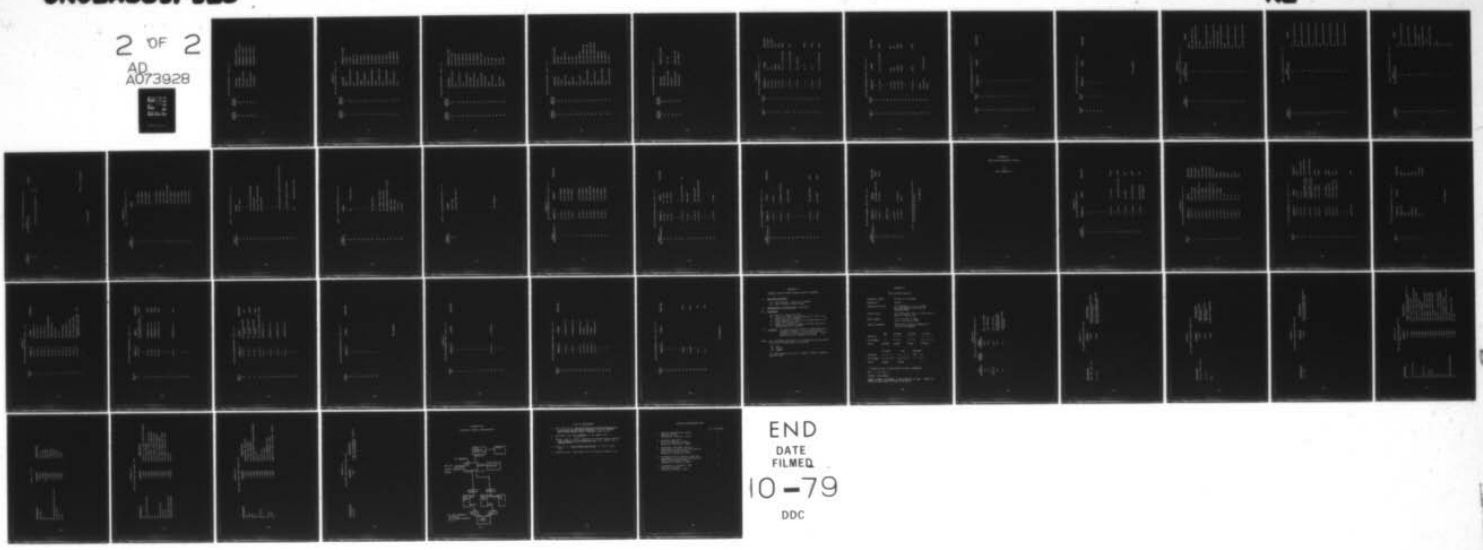
TEST UNIT WIRING-TABLE 1 (Page 3 of 4)

PINS OF TEST UNIT J1	PINS OF TEST UNIT J6	COLOR WIRE	PURPOSE OF J6 PINS
31	16	WHITE-BLUE	THUMBWHEEL T2 (2nd LSD) $\overline{1}$
32	41	YELLOW	THUMBWHEEL T2 (2nd LSD) $\overline{2}$
33	17	WHITE-VIOLET	THUMBWHEEL T2 (2nd LSD) $\overline{4}$
34	42	GREEN	THUMBWHEEL T2 (2nd LSD) $\overline{8}$
35	18	WHITE-GRAY	THUMBWHEEL T3 (3rd LSD) $\overline{1}$
36	43	BLUE	THUMBWHEEL T3 (3rd LSD) $\overline{2}$
37	19	WHITE-BLACK	THUMBWHEEL T3 (3rd LSD) $\overline{4}$
38	44	VIOLET	THUMBWHEEL T3 (3rd LSD) $\overline{8}$
39	20	WHITE-BLACK-BROWN	THUMBWHEEL T4 (4th LSD) $\overline{1}$
40	45	GRAY	THUMBWHEEL T4 (4th LSD) $\overline{2}$
41	21	WHITE-BLACK-RED	THUMBWHEEL T4 (4th LSD) $\overline{4}$
42	46	WHITE	THUMBWHEEL T4 (4th LSD) $\overline{8}$
43	22	WHITE-BLACK-ORANGE	THUMBWHEEL T5 (2nd MSD) $\overline{1}$
44	47	BLACK	THUMBWHEEL T5 (2nd MSD) $\overline{2}$
45	23	WHITE-BLACK-YELLOW	THUMBWHEEL T5 (2nd MSD) $\overline{4}$

AD-A073 928 NAVAL POSTGRADUATE SCHOOL MONTEREY CA F/G 9/5
DESIGN OF THE DIGITAL CONTROL AND TEST UNIT SUBSYSTEMS FOR A SA--ETC(U)
JUN 79 C MUSGRAVE

UNCLASSIFIED NL

2 OF 2
AD
A073928



END
DATE
FILMED
10-79
DDC

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TEST UNIT WIRING-TABLE 1 (Page 4 of 4)

PINS OF TEST UNIT J1	PINS OF TEST UNIT J6	COLOR WIRE	PURPOSE OF J6 PINS
46	48	WHITE-BROWN	THUMBWHEEL T5 (2nd MSD) $\overline{8}$
47	24	WHITE-BLACK-GREEN	THUMBWHEEL T6 (MSD) $\overline{1}$
48	49	WHITE-RED	THUMBWHEEL T6 (MSD) $\overline{2}$
49	25	WHITE-BLACK-BLUE	THUMBWHEEL T6 (MSD) $\overline{4}$
50	50	WHITE-ORANGE	THUMBWHEEL T6 (MSD) $\overline{8}$

APPENDIX K

TEST UNIT WIRING-TABLE 2 (Page 1 of 4)

PINS OF TEST UNIT J3	PINS OF TEST UNIT J7	COLOR WIRE	PURPOSE OF J7 PINS
1	1	BROWN	+5 VOLTS
2	26	WHITE-BLACK-VIOLET	+5 VOLTS
3	2	RED	RETURN (+5)
4	27	WHITE-BLACK-GRAY	RETURN (+5)
5	3	ORANGE	X2 SWITCH
6	28	WHITE-BROWN-RED	RC1 SWITCH
7	4	YELLOW	RC2 SWITCH
8	29	WHITE-BROWN-ORANGE	RC3 SWITCH
9	5	GREEN	X1 SWITCH
10	30	WHITE-BROWN-YELLOW	RS3 SWITCH
11	6	BLUE	RS2 SWITCH
12	31	WHITE-BROWN-GREEN	RS1 SWITCH
13	7	VIOLET	NOT CONNECTED
14	32	WHITE-BROWN-BLUE	NOT CONNECTED
15	8	GRAY	NOT CONNECTED

TEST UNIT WIRING-TABLE 2 (Page 2 of 4)

PINS OF TEST UNIT J3	PINS OF TEST UNIT J7	COLOR WIRE	PURPOSE OF J7 PINS
16	33	WHITE-BROWN-VIOLET	TO PIN 9 2003's
17	9	WHITE	NOT CONNECTED
18	34	WHITE-BROWN-GRAY	NOT CONNECTED
19	10	BLACK	NOT CONNECTED
20	35	WHITE-RED-ORANGE	NOT CONNECTED
21	11	WHITE-BROWN	NOT CONNECTED
22	36	WHITE-RED-YELLOW	NOT CONNECTED
23	12	WHITE-RED	NOT CONNECTED
24	37	WHITE-RED-GREEN	RETURN (+24V)
25	13	WHITE-ORANGE	RC3 LAMP
26	38	BROWN	RC2 LAMP
27	14	WHITE-YELLOW	RC1 LAMP
28	39	RED	X2 LAMP
29	15	WHITE-GREEN	X1 LAMP
30	40	ORANGE	RS3 LAMP

TEST UNIT WIRING-TABLE 2 (Page 3 of 4)

PINS OF TEST UNIT J3	PINS OF TEST UNIT J7	COLOR WIRE	PURPOSE OF J7 PINS
31	16	WHITE-BLUE	RS2 LAMP
32	41	YELLOW	RS1 LAMP
33	17	WHITE-VIOLET	NOT CONNECTED
34	42	GREEN	RT2 LAMP
35	18	WHITE-GRAY	RT3 LAMP
36	43	BLUE	RT1 LAMP
37	19	WHITE-BLACK	NOT CONNECTED
38	44	VIOLET	RCVR TEST ENABLE LAMP
39	20	WHITE-BLACK-BROWN	TEST XMTR ENABLE LAMP
40	45	GRAY	RCVR TEST ENABLE SWITCH
41	21	WHITE-BLACK-RED	TEST XMTR ENABLE SWITCH
42	46	WHITE	NOT CONNECTED
43	22	WHITE-BLACK-ORANGE	NOT CONNECTED
44	47	BLACK	NOT CONNECTED
45	23	WHITE-BLACK-YELLOW	XT2 LAMP

TEST UNIT WIRING-TABLE 2 (Page 4 of 4)

PINS OF TEST UNIT J3	PINS OF TEST UNIT J7	COLOR WIRE	PURPOSE OF J7 PINS
46	48	WHITE-BROWN	
47	24	WHITE-BLACK-GREEN	XT1 LAMP
48	49	WHITE-RED	
49	25	WHITE-BLACK-BLUE	DUMMY LOAD LAMP
50	50	WHITE-ORANGE	NOT CONNECTED

APPENDIX L

TEST UNIT MOTHERBOARD (CMB-1) {Page 1 of 4}

PINS OF J8	PINS OF J11	CONNECTS TO	PURPOSE	COLOR WIRE
1	1	J13 PIN U	+5V	PEA GREEN
26	2	J13 PIN V	+5V	PEA GREEN
2	3	J13 PIN S	RETURN	BLUE
27	4	J13 PIN T	RETURN	BLUE
3	5	J14 PIN 31	BIT 1 of CLOCK SELECT	WHITE
28	6	*		
4	7	J14 PIN 29	BIT 0 of CLOCK SELECT	RED
29	8	*		
5	9	J13 PIN 1	MLS to PSK MOD	
30	10	*		
6	11	J13 PIN 8	S4 "1"	BROWN
31	12	*		
7	13	J13 PIN 9	S4 "2"	BLACK
32	14	*		
8	15	J14 PIN 32	CW or PSK MOD SELECT	WHITE

TEST UNIT MOTHERBOARD (CMB-1) {Page 2 of 4}

PINS OF J8	PINS OF J11	CONNECTS TO	PURPOSE	COLOR WIRE
33	16	*		
9	17	J14 PIN 30	BIT 2 of CLOCK SELECT	PURPLE
34	18	*		
10	19	*		
35	20	J13 PIN P	+28V	RED
11	21	J13 PIN R	+28V	RED
36	22	J13 PIN M	RETURN	BLACK
12	23	J13 PIN N	RETURN	BLACK
37	24	*		
13	25	*		
38	26	J10 PIN 50	BLINK	WHITE
14	27	*		
39	28	GROUND		
15	29	SMA FITTING	1 MHz Ref SM160	
40	30	GROUND		

TEST UNIT MOTHERBOARD (CMB-1) {Page 3 of 4}

PIN OF J8	PIN OF J11	CONNECTS TO	PURPOSE	COLOR WIRE
16	31	*		
41	32	*		
17	33	*		
42	34	*		
18	*	*		
43	*	*		
19	*	*		
44	*	*		
20	*	*		
45	*	*		
21	*	*		
46	*	*		
22	*	*		
47	*	*		
23	*	*		

TEST UNIT MOTHERBOARD (CMB-1) {Page 4 of 4}

PINS OF J8	PINS OF J11	CONNECTS TO	PURPOSE	COLOR WIRE
48	*	*		
24	*	*		
49	*	*		
25	*	*		
50	*	*		

* NOT CONNECTED

APPENDIX M

TABLE 3 - TEST UNIT WIRING (Sheet 1 Of 4)

PINS OF TEST UNIT J2	PINS OF TEST UNIT J5 (SM160)	PURPOSE
1	1	GROUND
2	B	MOST SIGNIFICANT DIGIT
3	2	2nd MOST SIGNIFICANT DIGIT
4	C	+24 VOLTS
5	*	N/A
6	3	2nd MOST SIGNIFICANT DIGIT
7	D	8 VOLTS
8	4	2nd MOST SIGNIFICANT DIGIT
9	E	1MHz External Input
10	5	2nd MOST SIGNIFICANT DIGIT
11	F	GROUND
12	6	3rd MOST SIGNIFICANT DIGIT
13	*	N/A
14	7	3rd MOST SIGNIFICANT DIGIT
15	*	N/A
16	8	3rd MOST SIGNIFICANT DIGIT

TABLE 3 - TEST UNIT WIRING (Sheet 2 of 4)

PINS OF TEST UNIT J2	PINS OF TEST UNIT J5 (SM160)	PURPOSE
17	*	N/A
18	9	3rd MOST SIGNIFICANT DIGIT
19	*	N/A
20	10	4th MOST SIGNIFICANT DIGIT
21	*	N/A
22	11	4th MOST SIGNIFICANT DIGIT
23	*	N/A
24	12	4th MOST SIGNIFICANT DIGIT
25	*	N/A
26	13	4th MOST SIGNIFICANT DIGIT
27	*	N/A
28	14	5th MOST SIGNIFICANT DIGIT
29	*	N/A
30	15	5th MOST SIGNIFICANT DIGIT
31	*	N/A
32	16	5th MOST SIGNIFICANT DIGIT

TABLE 3 - TEST UNIT WIRING (Sheet 3 of 4)

PINS OF TEST UNIT J2	PINS OF TEST UNIT J5 (SM160)	PURPOSE
33	*	N/A
34	17	5th MOST SIGNIFICANT DIGIT
35	*	N/A
36	18	LEAST SIGNIFICANT DIGIT
37	*	N/A
38	19	LEAST SIGNIFICANT DIGIT
39	X	*NOT CONNECTED*
40	20	LEAST SIGNIFICANT DIGIT
41	Y	8 VOLTS
42	21	LEAST SIGNIFICANT DIGIT
43	*	N/A
44	Z	GROUND
45	*	N/A
46	*	N/A
47	*	N/A
48	*	N/A

TABLE 3 - TEST UNIT WIRING (Sheet 4 of 4)

PINS OF TEST UNIT J2	PINS OF TEST UNIT J5 (SM160)	PURPOSE
49	*	N/A
50	"BLINK" TO TEST UNIT BOARD TWO	N/A

PINK = 1 MHZ REFERENCE

* NOT CONNECTED

APPENDIX N

TABLE 4 - TEST UNIT WIRING (Sheet 1 of 4)

PINS OF TEST UNIT J4	PURPOSE
1	*
2	S6 RC3 CONTROL
3	S6 RC2 CONTROL
4	S6 RC1 CONTROL
5	S6 X2 CONTROL
6	*
7	S3 RT3 CONTROL
8	S3 RT2 CONTROL
9	S3 RT1 CONTROL
10	S6↔S4 XSITION CONTROL
11	S6 RS2 CONTROL
12	S6 RS3 CONTROL
13	S6 X1 CONTROL
14	S6 RS1 CONTROL
15	CIB RT3 SELECT
16	CIB RT2 SELECT

TABLE 4 - TEST UNIT WIRING (Sheet 2 of 4)

PINS OF TEST UNIT J4	PURPOSE
17	CIB RT1 SELECT
18	*
19	*
20	CIB RCVR TEST DISABLE/ENABLE
21	CIB RCVR ON/OFF
22	CIB TEST XMTR DISABLE/ENABLE
23	CIB XMTR ON/OFF
24	*
25	*
26	*
27	*
28	S7 XMIT/DUMMY LOAD CONTACTS (TO RELAY OF XFER SW)
29	*
30	S8 XT1/XT2 (TO RELAY OF XFER SW)
31	*
32	CIB XMIT/DUMMY LOAD SELECT

TABLE 4 - TEST UNIT WIRING (Sheet 3 Of 4)

PINS OF TEST UNIT J4	PURPOSE
33	*
34	CIB XT1/XT2 SELECT
35	*
36	*
37	*
38	*
39	*
40	TEST XMTR STATUS
41	*
42	XTZ CONTACTS FOR STATUS
43	XT1 CONTACTS FOR STATUS
44	XMIT/DUMMYLOAD CONTACTS FOR STATUS
45	RETURN (+28V)
46	RETURN (+28V)
47	+ 28Volts
48	+28 VOLTS

TABLE 4 - TEST UNIT WIRING (Sheet 4 of 4)

PINS OF TEST UNIT J4	PURPOSE
49	RF KEY LINE
50	BLINK FROM TEST UNIT J3

*NOT CONNECTED

APPENDIX O

TEST UNIT MOTHERBOARD (CMB-1) {Page 1 of 4}

PINS OF TEST UNIT J10(Note 1)	CONNECTS TO	PURPOSE	COLOR WIRE
1	*		
2	J13 PIN A	S6 RC3 CONTROL	
3	J13 PIN 2	S6 RC2 CONTROL	
4	J13 PIN B	S6 RC1 CONTROL	
5	J13 PIN 3	S6 X2 CONTROL	
6	*		
7	J13 PIN 4	S3 RT3 CONTROL	
8	J13 PIN D	S3 RT3 CONTROL	
9	J13 PIN 5	S3 RT1 CONTROL	
10	J13 PIN E	S6↔S4 TRANSITION	
11	J13 PIN 6	S6 RS2 CONTROL	
12	J13 PIN F	S6 RS3 CONTROL	
13	J13 PIN 7	S6 X1 CONTROL	
14	J13 PIN H	S6 RS1 CONTROL	

TEST UNIT MOTHERBAORD (CMB-1) {Page 2 of 4}

PINS OF TEST UNIT J10(Note 1)	CONNECTS TO	PURPOSE	COLOR WIRE
15	J14 PIN 4	RT 3 SELECT	
16	J14 PIN 2	RT 2 SELECT	
17	J14 PIN 3	RT 1 SELECT	
18	*		
19	*		
20	J12 PIN 16	RCVR ENABLE/DISABLE	RED
21	J14 PIN 7	RCVR ON/OFF	
22	*		
23	J14 PIN 10	TEST XMTR ON/OFF	
24	J14 PIN 12	TEST XMTR ENABLE/DISABLE	
25	*		
26	*		
27	*		
28	J15 PIN 23	S7 RELAY	

TEST UNIT MOTHERBOARD (CMB-1) {Page 3 of 4}

PINS OF TEST UNIT J10(Note 1)	CONNECTS TO	PURPOSE	COLOR WIRE
29	*		
30	J15 PIN 21	S8 RELAY	
31	*		
32	J14 PIN 11	XMT/DUMMY LOAD SELECT	
33	*		
34	J14 PIN 9	XT1/XT2 SELECT	
35	*		
36	*		
37	*		
38	*		
39	*		
40	J12 PIN 14	TEST XMTR STATUS	WHITE
41	*		
42	J12 PIN 12	XT2 STATUS	BLUE

TEST UNIT MOTHERBOARD (CMB-1) {Page 4 of 4}

PINS OF TEST UNIT J10(Note 1)	CONNECTS TO	PURPOSE	COLOR WIRE
43	J12 PIN 10	XMIT/DUMMY LOAD STATUS	YELLOW
44	J12 PIN 8	XT1 STATUS	PURPLE
45	*		
46	RETURN (+28)		
47	*		
48	+28 VOLTS		
49	J15 PIN 11	RF KEYLINE	
50	J11 PIN 26	BLINK	

Note 1: J10 is connected directly to Test Unit Board 2
(ie J9 not presently installed)

*NOT CONNECTED

APPENDIX P

TEST UNIT MOTHERBOARD (CMB-1)

J11

(SEE APPENDIX L)

APPENDIX Q

TEST UNIT MOTHERBOARD (CMB-1)

PINS OF TEST UNIT J12	CONNECTS TO	PURPOSE	COLOR WIRE
1	*		
2	*		
3	*		
4	*		
5	*		
6	*		
7	*		
8	J10 PIN 44	XTI STATUS	PURPLE
9	*		
10	J10 PIN 43	XMIT/DUMMY LOAD STATUS	YELLOW
11	*		
12	J10 PIN 42	XT2 STATUS	BLUE
13	*		
14	J10 PIN 40	TEST XMTR STATUS	WHITE
15	*		
16	J10 PIN 25	RCVR TEST STATUS	RED

* NOT CONNECTED

APPENDIX R

TEST UNIT MOTHERBOARD (CMB-1) {Page 1 of 3}

PINS OF J13	CONNECTS TO	PURPOSE	COLOR WIRE
1	J11 PIN 9	MLS to PSK MOD	WHITE-BLACK
2	J10 PIN 3	S5 RC2 CONTROL	WHITE-BROWN
3	J10 PIN 5	S6 X2 CONTROL PIN 6	WHITE-RED
4	J10 PIN 7	S3 RT3 CONTROL	WHITE-ORANGE
5	J10 PIN 9	S3 RT1 CONTROL	WHITE-YELLOW
6	J10 PIN 11	S6 RS2 CONTROL PIN 2	WHITE-GREEN
7	J10 PIN 13	S6 X1 CONTROL PIN 5	WHITE-BLUE
8	J11 PIN 11	S4 "1" CONTROL	BROWN
9	J11 PIN 13	S4 "2" CONTROL	ORANGE
10	U1 PIN 10	AT 1-16	YELLOW
11	U1 PIN 11	AT 1-8	GREEN
12	U1 PIN 12	AT 1-4	BLUE
13	U1 PIN 13	AT 1-2	VIOLET
14	U1 PIN 14	AT 1-1	GRAY

TEST UNIT MOTHERBOARD (CMB-1) {Page 2 of 3}

PINS OF J13	CONNECTS TO	PURPOSE	COLOR WIRE
15	U1 PIN 16	AT 2-16	WHITE
16	U1 PIN 15	AT 2-16	WHITE-RED-GREEN
17	J14 PIN 15	150 MHZ SELECT & RCVR SELECT(S1 "1" & S2 "1")	WHITE-BROWN-VIOLET
18	J14 PIN 13	180 MHZ SELECT & TEST SELECT(S1 "2" & S2 "2")	WHITE-BROWN-ORANGE
A	J10 PIN 2	S5 RC3 CONTROL	BROWN
B	J10 PIN 4	S5 RC1 CONTROL	ORANGE
C	*		
D	J10 PIN 8	S3 RT2 CONTROL	YELLOW
E	J10 PIN 10	S6→S5 TRANSITION	GREEN
F	J10 PIN 12	S6 RS3 CONTROL PIN 3	BLUE
H	J10 PIN 14	S6 RS CONTROL PIN 1	VIOLET
J	*		
K	*		
L	*		
M	RETURN (+28)		BLACK

TEST UNIT MOTHERBOARD (CMB-1) {Page 3 of 3}

PINS OF J13	CONNECTS TO	PURPOSE	COLOR WIRE
N	RETURN (+28)		BLACK
P	+28V		RED
R	+28V		RED
S	RETURN(+5)		BLUE
T	RETURN(+5)		BLUE
U	+5V		PEA GREEN
V	+5V		PEA GREEN

* NOT CONNECTED

APPENDIX S

TEST UNIT MOTHERBOARD (CMB-1) {Page 1 of 4}

PINS OF J14	CONNECTS TO	PURPOSE	COLOR WIRE
1	U1 PIN 5	ATTENUATOR AT1-1	
2	J10 PIN 16	RT2 SELECT S3	
3	J10 PIN 17	RT1 SELECT S3	
4	J10 PIN 15	RT3 SELECT S3	
5	J10 PIN 20	RCVR TEST ENABLE/DISABLE	
6	U1 PIN 7	ATTENUATOR AT2-16	
7	J10 PIN 21	RCVR ON/OFF	
8	U1 PIN 6	AT 2-16	
9	J10 PIN 34	XT1/XT2 SELECT	
10	J10 PIN 23	TEST XMTR ON/OFF	
11	J10 PIN 32	XMT/DUMMY LOAD SELECT	
12	J10 PIN 22	TEST XMTR ENABLE/DISABLE	
13	J13 PIN 18	180 MHZ SELECT & TEST XMTR SELECT(S1 "2" & S2 "2")	BLUE
14	*		

TEST UNIT MOTHERBOARD(CMB-1) {Page 2 of 4}

PINS OF J14	CONNECTS TO	PURPOSE	COLOR WIRE
15	J13 PIN 17	150 MHZ SELECT & RCVR TEST SELECT (S1 "1" & S2 " ")	YELLOW
16	*		
17	U2 PIN 4	ATTENUATOR AT 3-2	GREEN
18	U2 PIN 2	ATTENUATOR AT 3-8	BROWN
19	U2 PIN 3	ATTENUATOR AT 3-4	ORANGE
20	U2 PIN 1	ATTENUATOR AT 3-16	WHITE
21	*		
22	*		
23	*		
24	U2 PIN 5	ATTENUATOR AT 3-1	GRAY
25	*		
26	*		
27	*		
28	*		

TEST UNIT MOTHERBOARD(CMB-1) {Page 3 of 4}

PINS OF J14	CONNECTS TO	PURPOSE	COLOR WIRE
29	J11 PIN 7	BIT 0 of CLOCK SELECT FOR MLS	RED
30	J11 PIN 17	BIT 2 of CLOCK SELECT FOR MLS	PURPLE
31	J11 PIN 5	BIT 1 of CLOCK SELECT FOR MLS	WHITE
32	J11 PIN 15	CW or PSK MODULATION SELECT	WHITE
33	U1 PIN 4	ATTENUATOR AT 1-2	
34	*		
35	U1 PIN 3	ATTENUATOR AT 1-4	
36	*		
37	U1 PIN 2	ATTENUATOR AT 1-8	
38	*		
39	U1 PIN 1	ATTENUATOR AT 1-16	
40	*		
41	*		
42	*		

TEST UNIT MOTHERBOARD(CMB-1) {Page 4 of 4}

PINS OF J14	CONNECTS TO	PURPOSE	COLOR WIRE
43	*		
44	*		
45	*		
46	*		
47	*		
48	*		
49	*		
50	*		

*NOT CONNECTED

APPENDIX T

TEST UNIT MOTHERBOARD (CMB-1) {Page 1 of 3}

PINS OF J15	CONNECTS TO	PURPOSE	COLOR WIRE
1	*		
2	*		
3	*		
4	*		
5	*		
6	*		
7	*		
8	*		
9	*		
10	*		
11	J10 PIN 49	RF KEYLINE	
12	*		
13	*		
14	*		

TEST UNIT MOTHERBOARD (CMB-1) {Page 2 of 3}

PINS OF J15	CONNECTS TO	PURPOSE	COLOR WIRE
15	*		
16	U2 PIN 16	ATTENATOR AT1-16	
17	*		
18	U2 PIN 15	ATTENUATOR AT1-8	
19	*		
20	U2 PIN 14	ATTENUATOR AT1-4	
21	J10 PIN 30	S8 RELAY	
22	U2 PIN 13	ATTENUATOR AT1-2	
23	J10 PIN 28	S7 RELAY	
24	U2 PIN 12	ATTENUATOR AT1-1	
25	*		
26	*		
27	*		
28	*		

TEST UNIT MOTHERBOARD (CMB-1) {Page 3 of 3}

PINS OF J15	CONNECTS TO	PURPOSE	COLOR WIRE
29	*		
30	*		
31	*		
32	*		
33	*		
34	RETURN		BLACK
35	*		
36	RETURN		BLACK
37	*		
38	+28		RED
39	*		
40	+28		RED

*NOT CONNECTED

APPENDIX U

PRINTED CIRCUIT BOARD SOLDER DIPPING PROCEDURE

I. EQUIPMENT REQUIRED:

(a) 60/40 Solder - Quantity as Needed
(b) Flux - Kester's 1585 Liquid

II. TEMPERATURE OF SOLDER BATH = 485-500°F

III. PROCEDURE:

(a) Dip P.C. Board into Flux
(b) Place P.C. Board approximately 1/2" over a hot plate for 10-15 seconds
(c) Place heated P.C. board into solder bath at 15° angle from horizontal
(d) Allow P.C. board to remain in solder bath for approximately 2-3 seconds

IV. ICICLING: If icicling occurs the P.C. board has been allowed to remain in the liquid solder either too long or not long enough. Experimentation will eliminate icicling.

NOTE: This procedure applied to P.C. boards which are plated with the following types of plating:

(a) tin
(b) copper
(c) solder

If nickel plating is on P.C. board, another procedure must be used.

APPENDIX V

SM160 SPECIFICATIONS

FREQUENCY RANGE	20,000 to 159.999MHz
RESOLUTION	1000Hz
FREQUENCY SECTION	5½ DIGIT BCD (1, 2, 4, 8 BCD) ALL PROGRAMMING LINES ARE TTL POSITIVE TRUE
OUTPUT LEVEL	ECL LEVELS INTO 50Ω 0.7 VOLTS Peak-to-Peak or +2dBm ± 1dB
POWER REQMTS	+8 to +10 VDC at 800ma +22 to +30 VDC at 50ma
MATING CONNECTOR	TRW CINCH 50-44A-30 CONNECTOR IS 44 PIN .156 CENTERS

	MSD	2nd MSD	3rd MSD	4th MSD
FUNCTION	1	8 4 2 1	8 4 2 1	8 4 2 1
PIN NUMBER	B	2 3 4 5	6 7 8 9	10 11 12 13
DIGIT	X100MHz	X10MHz	X1MHz	X100KHz

	5th MSD				LSD				VOLTAGES	
FUNCTION	8	4	2	1	8	4	2	1	+24V	+10
PIN NUMBER	14	15	16	17	18	19	20	21	C	D,V
DIGIT	X10KHz				X1KHz					

+5 VOLTS ON PIN X IS AN OUTPUT TO SM160 CONNECTOR

GND: 1, 22, F-W, Z

OUTPUT: SMA FEMALE

REMOVE JUMPER IF EXTERNAL 1 MHz STANDARD IS USED. JUMPER IS SHOWN ON DATA SHEET PROVIDED WITH SM160.

APPENDIX W

PARTS LIST FOR CONTROL INTERFACE BOARD (CIB)

CIB DESIGNATION	QUANTITY REQUIRED	NUMBER DESIGNATION	
U1	1	74155	DUAL 4 BIT DECODER
U2	1	7485	4 BIT COMPACATOR
U3, U4 U5, U6, U7	1	74116	DUAL 4 BIT LATCH
U8	1	7416	HEX INVERTERS (OPEN COLLECTOR-DRIVER)
U9	1	———	4 ROCKER DOUBLE THROW DIP SWITCH

APPENDIX X

CIB DRIVER BOARD PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
UR1, UR2, UR3, UR4	1 EACH	314332=3.3KΩ DIP RESISTORS MFG=ALLEN BRADLEY
L1 - L15	1 EACH	LED's WITH INTERNAL RESISTORS MFG=DIALIGHT #555-3004

APPENDIX Y

CIB COMPUTER SIMULATOR PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
D7-D4, D3-D0, S3-S0	1 EACH	4 ROCKER DIP SWITCH MFG=CHERRY
$A_1 = A_0$	1 EACH	2 ROCKER DIP SWITCH MFG=CHERRY
NDR	1 EACH	PUSBUTTON (MOMENTARY)

APPENDIX Z

CIB DEVICE SIMULATOR PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
L1 - L36	1 EACH	LED's WITH INTERNAL RESISTORS MFG=DIALIGHT #555-3004

APPENDIX AA

TEST UNIT BOARD ONE PARTS LIST
(Page 1 of 2)

DESIGNATION	QUANTITY	DESCRIPTION
U1	1 EACH	19.2KHz DIP XTAL OSC. MODEL L13C MFG = CONNOR-WINFIELD
U2,U3,U4,U5,J6	1 EACH	7474 DUAL D FLIP FLOP
U7	1 EACH	74164 8 BIT SIPO SHIFT REGISTOR
U8	1 EACH	74260 DUAL 5 INPUT NOR GATE
U9	1 EACH	74151 1 of 8 SELECTOR
U10,U17,U23	1 EACH	7404 HEX INVERTERS
U11	1 EACH	7486 QUAD 2 INPUT EXOR GATE
U12,U14	1 EACH	7408 QUAD 2 INPUT AND GATE
U13,U18	1 EACH	7400 QUAD 2 INPUT NAND GATE
U15	1 EACH	7427 TRIPLE INPUT NOR GATE
U16	1 EACH	555 TIMER
U19	1 EACH	LM7810C + 10 VOLT REGULATOR
U20	1 EACH	LM340-24 + 24 VOLT REGULATOR
U21	1 EACH	2003 LAMPDRIVER (NAND)
U22	1 EACH	74186 FUZEABLE LINK PROM (64X8)
DESPIKING CAPACITORS	22 TOTAL	.001μfd
L1	1 EACH	LED DIALIGHT #555-3004
R1	1 EACH	9Ω 10W

DESIGNATION	QUANTITY	DESCRIPTION
R2,R3,R5	1 EACH	5Ω 5W
R4	1 EACH	20Ω 10W
R6	NOT USED	NOT USED
R7	1 EACH	33KΩ ¼W
R8	1 EACH	100KΩ ¼W
R9,R10,R14,R15,R16,R17, R18	1 EACH	3.3KΩ ¼W
R11,R12,R13	1 EACH	2KΩ ¼W
C1,C3	1 EACH	.22μfd
C2,C4	1 EACH	1μfd

APPENDIX BB

TEST UNIT BOARD TWO PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
U1	1 EACH	74148 8 to 3 LINE PRIORITY ENCODER
U2,U7,U8,U13,U17,U19	1 EACH	7404 HEX INVERTER
U3	1 EACH	74175 QUAD D TYPE FLIP FLOP
U4	1 EACH	314A332 DIP 3.3KΩ RESISTORS
U5	1 EACH	7427 TRIPLE INPUT NOR GATE
U6	1 EACH	74138 3 to 8 LINE DECODER
U9,U10,U16,U18	1 EACH	2003 LAMP DRIVER (NAND)
U11,U14	1 EACH	7408 QUAD 2 INPUT AND GATE
U12, U15	1 EACH	7474 DUAL D TYPE FLIP FLOP
R1,R2,R3,R4,R5,R6,R7	1 EACH	3.3KΩ ¼W
DESPIKING CAPACITORS	19 TOTAL	.001μfd

APPENDIX CC

TEST UNIT BOARD THREE PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
741	1 EACH	OPERATIONAL AMPLIFIER
7912	1 EACH	-12 VOLT REGULATOR
7812	1 EACH	+12 VOLT REGULATOR
CM1	1 EACH	DOUBLE BALANCED MIXER(MFG=C1MSTTON)
R1	1 EACH	1.2MΩ ¼W
R2,R3,R4	1 EACH	10KΩ ¼
R5	1 EACH	400-470Ω ¼W
C1	1 EACH	.10μfd (+30V)
C2,C5	1 EACH	1.0μfd TANTALUM (+30V)
C3,C4	1 EACH	2.0μfd TANTALUM (+30V)
D1	1 EACH	IN485B (or IN270, IN483B, IN3595)

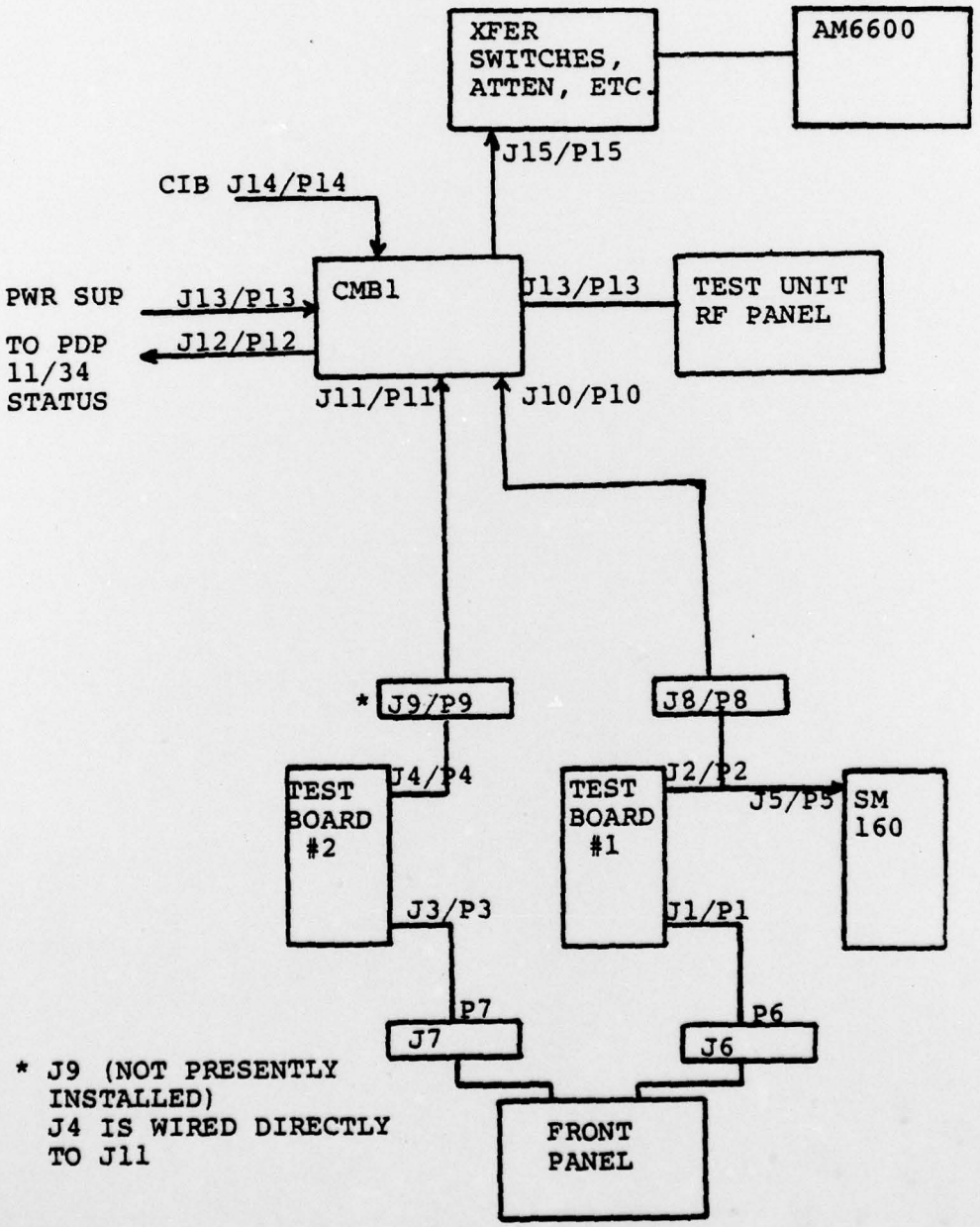
APPENDIX DD

TEST UNIT BOARD FOUR PARTS LIST

DESIGNATION	QUANTITY	DESCRIPTION
UR1,UR2	1 EACH	2.2KΩ DIP RESISTORS (314A222) MFG=ALLEN BRADLEY

APPENDIX EE

TEST UNIT CONTROL CONFIGURATION



* J9 (NOT PRESENTLY INSTALLED)
J4 IS WIRED DIRECTLY TO J11

LIST OF REFERENCES

1. Zell, William B., Analog-to-Digital Signal Processing In A Prototype SATCOM Signal Analyzer, M.S.E.E. Thesis, Naval Postgraduate School, Monterey, April 1979.

2. Lancaster, Don, TTL COOKBOOK, P. 31, SAMS, 1974.

3. Ohlson, John E., "Exact Dynamics of Automatic Gain Control", IEEE Transactions On Communications, Vol. COM-22, No. 1, January 1974.

4. Dixon, R. C., Spread Spectrum Systems, p. 54-56, Wiley, 1976.

5. Cimmaron Corp., Data Sheet CM-1, Division of VARI-L, Co.

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