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DEVELOPMENT OF CHARGE TRANSFER DEVICES FOR 1-2 MICRON IMAGING.(U)
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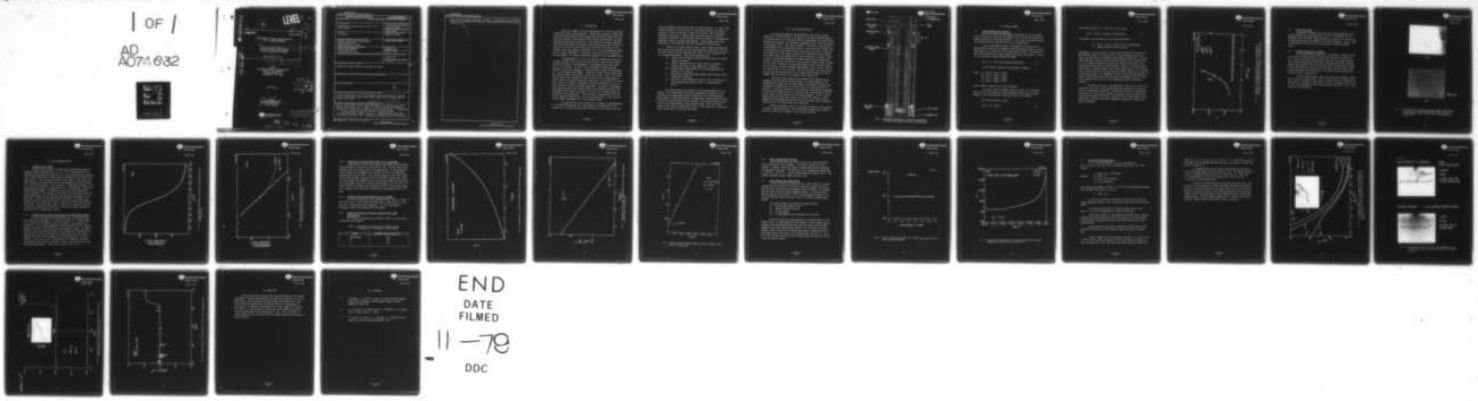

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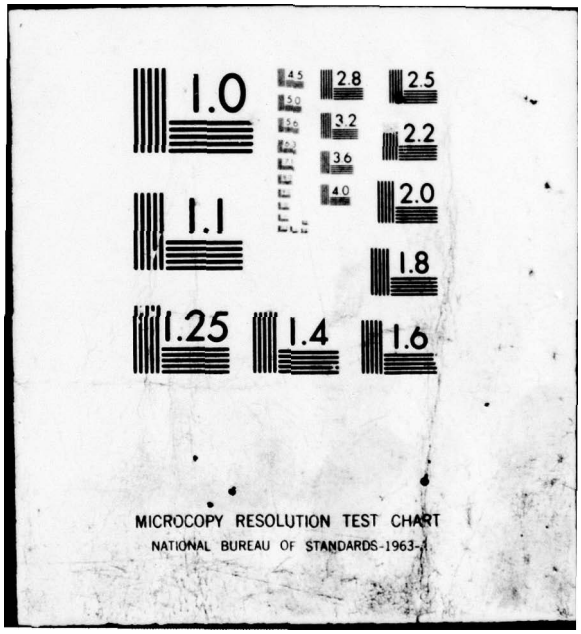
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DEVELOPMENT OF CHARGE TRANSFER DEVICES FOR 1-2 MICRON IMAGING

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

There is considerable interest in the development of an imaging system within the wavelength range of 1.0 - 1.8μm. The comcept of charge coupled devices emerges as one of the viable candidates for such an application. The advantages of a non-MIS, Schottky barrier, buried channel CCD are discussed.

A suitable material system for the 1.0 - 1.8μm CCD application is the n-GaAlSb/p+-GaSb hetero-system. Substantially improved surface morphology for this system is reported. This is achieved by the addition of As to the GaAlSb

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layer, thus forming the quaternary: GaAlAsSb. Characterization of Schottky barriers to this material are reported. The Schottky barrier height is found to be >0.7 eV.

1.0 INTRODUCTION

There are a number of military applications for a passive (available illumination) night vision capability. Technological advances in image intensifiers and high performance photocathodes have resulted in night vision systems which operate in the visible and near infrared spectrum under low level moonlight and starlight illumination. These systems are, however completely ineffective under moonless or overcast conditions because of the low level of light in the 0.5-0.9 μm region under such conditions. Since there is considerable night glow ambient illumination in the 1.0-1.8 μm wavelength region which is nearly independent of cloud-cover, one solution to this problem is the development of an imaging system which operates in this wavelength region.

The development of a 1.0-1.8 μm imaging system has been the goal of a number of research efforts over the past 10 years. Most of these efforts have been directed at the development of a photocathode which would work in the 1.0-1.8 μm region. In spite of the large number of device concepts examined, none has yet emerged as a viable candidate to meet the requirements for a 1.8 μm imaging photocathode. A potential alternative to a photocathode for infrared imaging is the charge coupled device (CCD). While Si CCD's have recently come to the forefront for both visible and 3-5 μm imaging applications, there are no suitable deep level impurities in this material for operation in the 1-2 μm region. Furthermore, Si devices designed for 3-5 μm, require cooling to ~40K for satisfactory operation. Such cooling requirements would make Army night vision devices prohibitively expensive and would place unacceptable restrictions on virtually all of the 1-2 μm imaging systems envisioned for Army applications. CCD's developed in new materials with high optical absorption coefficients in the 1-2 μm region offer a viable solution to the systems requirements for a 1-2 μm imaging system.

The approach that we are pursuing in this program is the development of a non-MIS heterojunction CCD. This approach is chosen because of the present lack of a viable MIS technology for materials other than silicon and

recent developments at the Science Center on non-MIS devices. In spite of the extensive studies of III-V MIS devices, significant problems still remain to be solved in order to fabricate a useful III-V MIS CCD. While significant progress has been made in reducing the surface state density on some MIS structures, the mobile ion and insulator stability problems in low temperature deposited or anodic insulators have remained. These problems prevent the realization of a MIS CCD with stable and reproducible characteristics.

There is now reason to believe that a buried channel heterojunction may not only avoid the above problems associated with insulators in a MIS CCD, but offer certain inherent advantages which render it more suitable for the 1.8 μm imaging application. Some of these advantages are:

(1) A built-in anti-blooming capability without the use of special channel stop regions.

(2) Superior radiation hardness to both particle (electrons, protons) and photon (x-rays, gamma rays) irradiation.

(3) Greater dynamic range because of low charge generation and absence of an insulator.

(4) High optical quantum efficiency achieved with intrinsic direct bandgap III-V materials.

(5) Lower dark current because the electric field is confined to a wide bandgap charge transport layer in a heterojunction device.

Thus heterojunction CCDs promise a very exciting approach to 1-2 μm imaging. While several material systems are potential candidates for this application, the GaAlSb-GaSb system is selected for the first development phase because it offers the potential to demonstrate a heterojunction CCD with a relatively simple Schottky barrier structure. We also have extensive experience in device applications of this material system. With this material system, at the expected average signal levels in this application, photon shot noise limited operation should be realizable.

2.0 DEVICE DESIGN CRITERIA

The proposed design for the heterojunction CCD (HJCCD) has been described in previous reports.[1] The physics of the device operation need not be discussed again, but a few points about key requirements for proper device operation are relevant. For reference a photograph of the initial test device is reproduced in Fig. 1 from previous reports. The device is fabricated on n-type GaAlAsSb with a p-type GaSb substrate. Device isolation (channel stop) is provided by a large Schottky barrier ring (guard ring) which is biased to fully deplete the n-type charge transport layer around the transfer channel. The transfer gates are Schottky barrier gates separated by 2 μm gaps. There is also a 2 μm separation between the transfer gates and the channel stop. Charge is injected into and removed from the device by means of ohmic contacts to the n-layer. Contact to the individual transfer gates is made by individual wire bonds. The device measures approximately 3 mm by 0.6 mm. Thus the p-n junction area is 1.8×10^{-2} cm^2. The key requirements for device operation are that all transfer gates be low leakage, that the guard ring be low leakage, and that the entire p-n junction area be defect free.

The reverse bias leakage current depends on the Schottky barrier leakage and the p-n junction reverse leakage. The former depends on the Schottky barrier height and the latter depends on the thermal leakage in the two materials composing the p-n junction as well as to the quality of this junction. In practice, the active layer thickness and doping must be adjusted so that when the Schottky barrier is reverse biased, punch-through of the depletion region to the p-substrate occurs before breakdown. This is crucial, especially for the guard ring. Failure to achieve this condition, causes leakage from the surrounding material to the active region, thus flooding the potential wells and rendering the device inoperative.

Another important criterion for successful operation of this device is material surface morphology. This surface must be sufficiently smooth to points are individually discussed in the following sections.

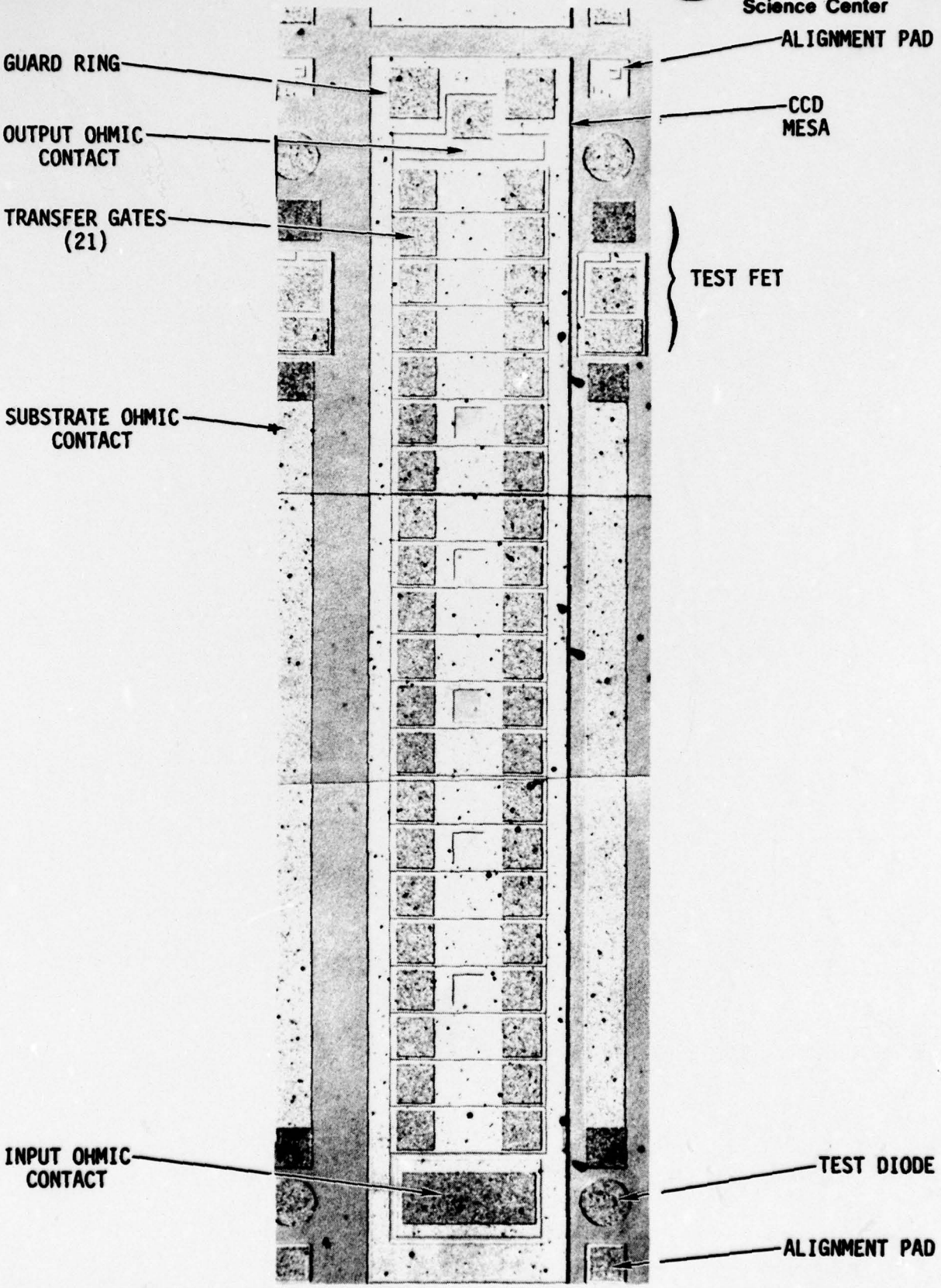

Fig. 1 Photograph showing the as processed GaAlSb/GaSb heterojunction Schottky gate CCD. (revised 7/78)

3.0 MATERIAL GROWTH

3.1 Lattice Matching by As Addition

One of the significant improvements made during the last six months in the LPE growth of GaAlSb was the addition of As to bring the lattice constant to match that of the GaSb substrate[2]. This is still an on-going task as the incorporation of As into the solid is not straightforward.

Part of the problem of the As incorporation is the difficulty in measuring the As content of the epitaxial layer accurately because of the very small amount of As required to lattice match GaAlSb to GaSb. Glissen et al.[3] (1978) have calculated the lattice constants of $Ga_xAl_{1-x}As_{1-y}Sb_y$ as a function of (x,y) assuming a linear interpolation scheme:

$$Q(x,y) = B_1 + (B_2-B_1)x+(B_4-B_3)y+(B_1-B_2+B_3-B_4)xy \qquad (1)$$

Q is the lattice constants of the quaternary compound

where $B_1 = Q(0,0) = A_{AlAs} = 5.611A$
$B_2 = Q(1,0) = A_{GaAs} = 5.6419A$
$B_3 = Q(1,1) = A_{GaSb} = 6.094A$
$B_4 = Q(0,1) = A_{AlSb} = 6.135A$

are the lattice constants of the binary compounds.

The present method of estimating the As content in the quaternary layer is by first measuring the lattice constants of the $Ga_xAl_{1-x}As_{1-y}Sb_y$ epitaxial layer and a reference $Ga_xAl_{1-x}Sb$ layer of the source x.

Then from equation (1) we get

$$Q(x,0) = B_1 + (B_2-B_1)X \qquad (2)$$

which gives the value of x. Then from (1)-(2) we get

$$Q(x,y) - Q(x,o) = (B_4-B_3)y + (B_1-B_2+B_3-B_4)xy \qquad (3)$$

This method is not accurate due to the following problems:

(i) $Q(x,y) - Q(x,0)$ is small and so is $(B_1-B_2+B_3-B_4)$
(ii) Bowing parameters are not included

Nevertheless, it served to give a trend of the As distribution coefficient in the GaAlAsSb system. One advantage of the present technique is that the actual lattice constants are measured rather than the composition. Since the lattice matching is more critical to good LPE growth as well as device quality, it is better to measure it directly and trade-off the accuracy in As distribution coefficient for lattice matching. Figure 2 is the distribution coefficient of a GaAlAsSb growth. One can see that at above 4×10^{-2} percent of As in the melt the As in the solid goes up steeply towards the As rich side of the phase diagram. This phenomena is similar to what has been obtained in GaSbAs as immiscibility gap except that the As concentration is still quite low for immiscibility to set in. Good homogeneous growth is therefore obtained.

One other difficulty in incorporating As in the solid is the low As solubility in the melt. By increasing the growth temperature, one will be able to increase the As solubility. Provided that the ratio of distribution coefficient of As to Sb stays constant (or goes up), this is one way to increase the As content in the solid. Already with the limited amount of work we were able to improve the surface morphology considerably by going from GaAlSb to GaAlAsSb.

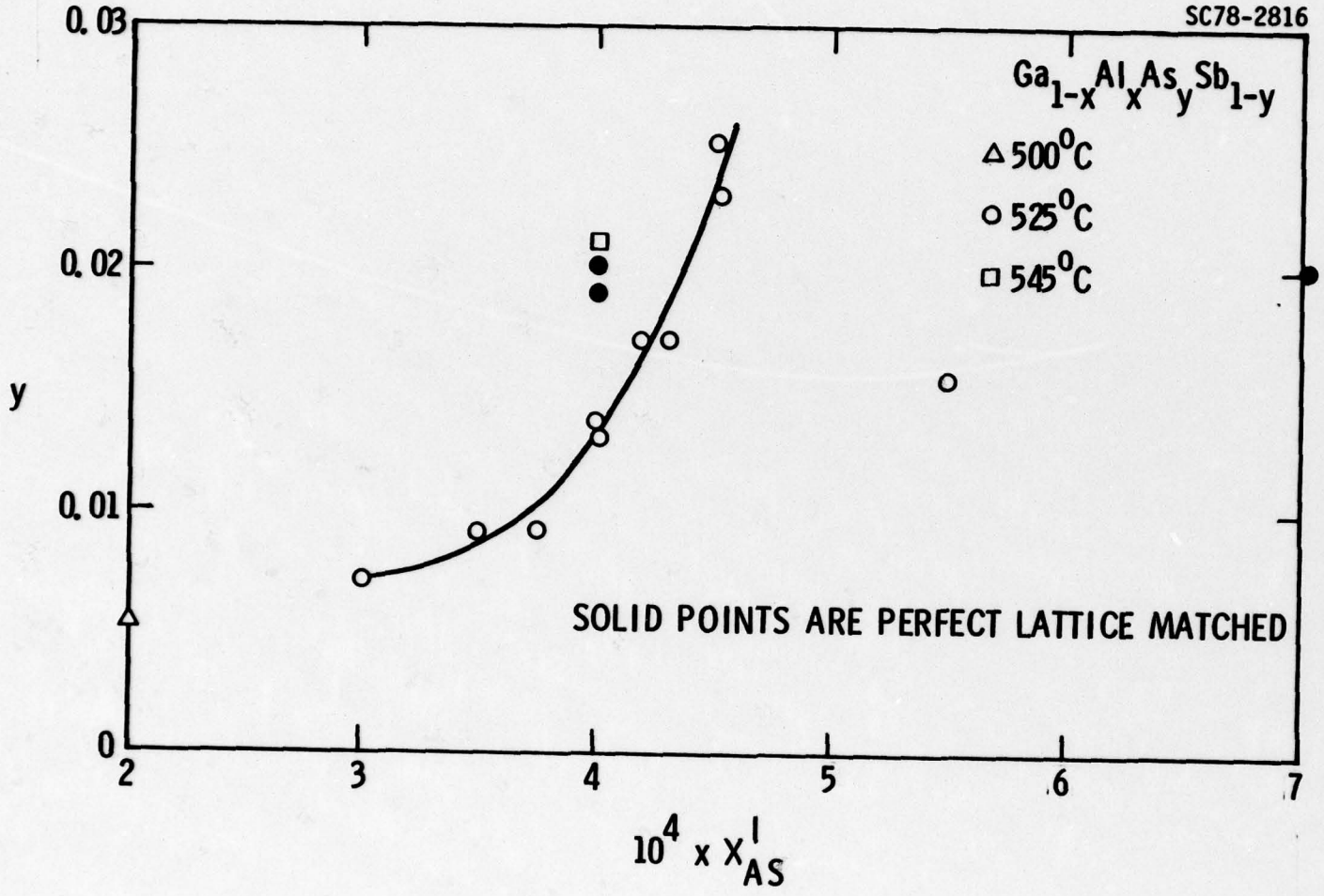

Fig. 2 Nonlinear distribution coefficient of A_S in the GaAlAsSb system. X is between 30 to 50 percent. (Two points to the right of the solid curve are results of two phase growth.)

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3.2 Surface Morphology

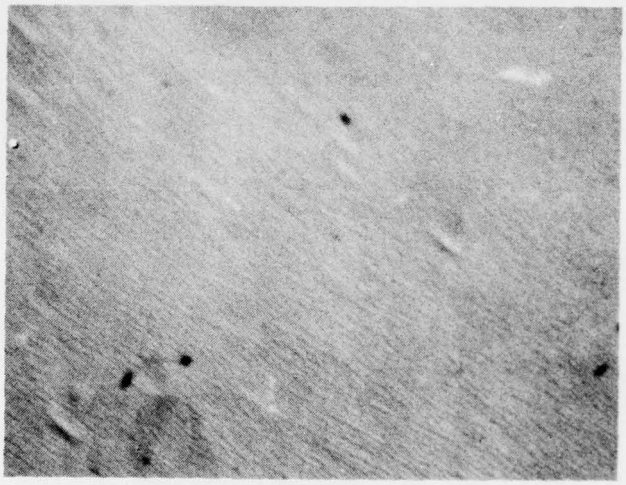
Considerable improvement was made in the surface morphology of LPE GaAlSb throughout the reporting period. Part of the improvement was undoubtedly due to the better lattice matching by As addition and part was due to experience and minor improvements in the growth technique. Figure 3 shows two photographs of an early and a later surfaces of GaAlAsSb epitaxial layers.

3.3 Aluminum concentration in GaAlSb

The desired aluminum concentration of the GaAlSb is ideally as high as possible for obvious reasons of large barrier height and low dark current. However, LPE growth considerations limits this to no more than 55%. During this reporting period, the surface morphology was steadily improved. However, when examined electrically by use of small Schottky barrier diodes, it was found that the p-n junction characteristics were quite leaky. Mesa etching through to the substrate also did not improve the leakage current indicating a bulk, leaky junction.

For 30% Al GaAlSb layer, however, mesa etching considerably reduced the p-n junction leakage current. Details of these results are reported in a later section. The cause for the higher p-n junction leakage current for 55% Al layer is not understood at this time and most of the work will be on 30% Al layers for CCD fabrication.

(a)



100 μm/cm

(b)

Fig. 3 (a) Surface of $Ga_{.45}Al_{.55}Sb$ on GaSb (sample k51) showing cross-hatch due to lattice mismatch and (b) surface of $Ga_{.45}Al_{.55}AsSb$ on GaSb (sample k50) showing absence of cross-hatch.

4.0 DEVICE CHARACTERIZATION

4.1 Schottky Barrier Height

Schottky barrier height to $Ga_{.45}Al_{.55}Sb$ was evaluated by three independent methods: photoresponse, C-V, I-V. In all the experiments to be described, the Schottky metal used was Cr-Au. The surface was lightly etched prior to metal deposition to remove native oxides which invariably form on the GaAlSb surface. The first metal deposited is Cr (~100A). This serves to enhance adhesion of the metalization to the semiconductor and blocks diffusion of Au into the semiconductor. This deposition is immediately followed (in the same evaporation system) by a deposition of Au. This deposition is typically between 1000A and 5000A. The thickness has no influence on the Schottky barrier parameters. This procedure is followed in all experiments except the photoresponse method in which case the total metalization thickness is less than 100A, in order to facilitate optical transmission. The metalization pattern consists of round dots (3 mil to 5 mil dia) uniformly distributed on the surface. The contact to the layer is achieved by a large dot, typically 20 times the diameter of the small dots. This dot has larger leakage and therefore acts as a pseudo-ohmic contact.

4.1.1 Schottky Barrier Height Determination by the Photoresponse Method

For this experiment thin Cr-Au Schottky dots, as described above, were evaporated on the sample. The sample was mounted in a suitable header and the dots were wire-bonded to pins on the header. The experiment was performed in a Cary-14 spectraphotometer especially modified with a feedback system to maintain a fixed intensity as the wavelength changes. The sample is inserted in the light beam and electrically connected to a current-mode preamplifier which in turn is connected to a lock-in-amplifier. The lock-in is synchronized to the chopping frequency of the light beam within the spectrometer. In this way, a plot of photocurrent vs. wavelength is obtained. The Schottky barrier height is determined directly by extrapolating the long wavelength photoresponse. Typical data is shown in Figs. 4, 5.

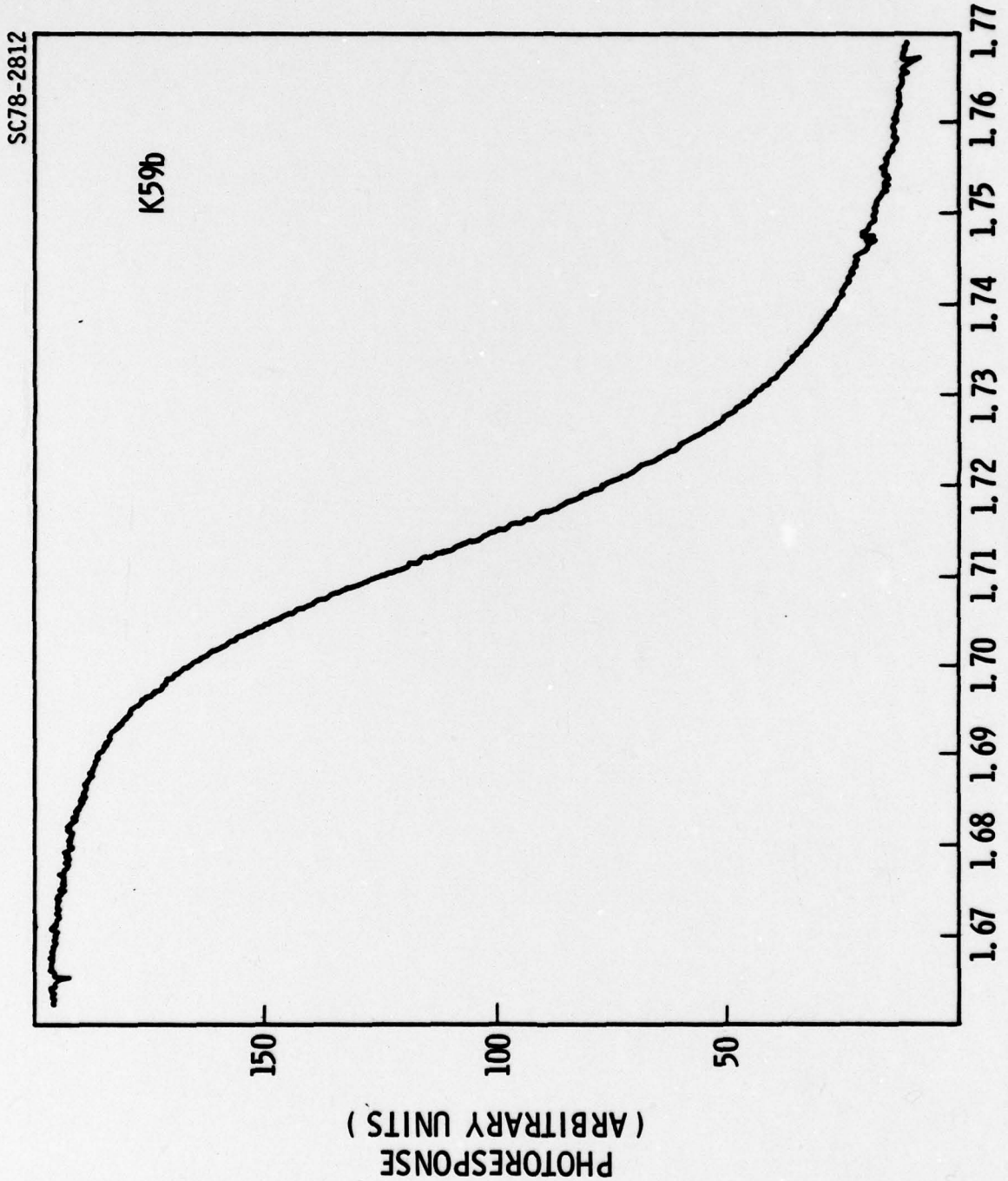


Fig. 4 Long wavelength photoresponse of 100Å Cr-Au Schottky barrier on $GaAl_{.45}Sb_{.55}$.

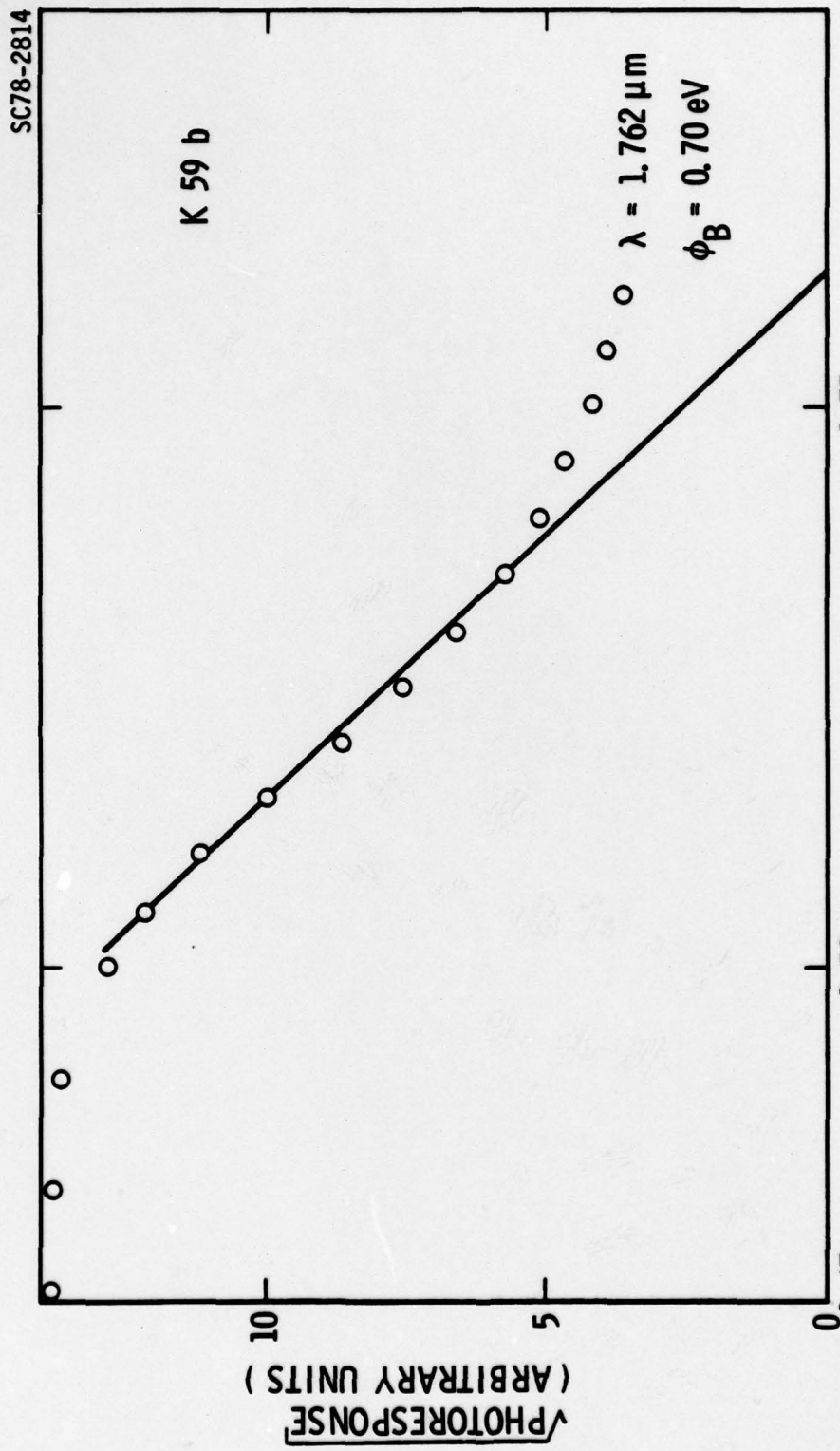


Fig. 5 Measured photoresponse and interpolated barrier height from Cr-Au Schottky barrier on $GaAl_{.45}Sb_{.55}$.

4.1.2 Schottky Barrier Height Determination by C-V Measurement

Capacitance vs. reverse bias voltage on the Schottky dots described above were taken at frequencies of 100 kHz and 1 MHz. The two contacts were between a small dot and the large dot described before. For the purposes of this experiment the arrangement can be thought of as the rf voltage being applied across two capacitors. Since the test capacitor (small dot) is much smaller than the other ($\simeq \frac{1}{20}$ dia.) most of the applied voltage drops across the smaller capacitor and the effect of the depletion region under the larger dot is negligible Once the C-V data has been obtained, a plot of $(1/C^2)$ vs. V reveals the barrier height by the intersection of this line with the voltage axis. Figures 6 and 7 show the C-V data and the corresponding $(1/C^2)$ vs. V data.

4.1.3 Schottky Barrier Height Determination by I-V Method

The barrier height can also be obtained from the forward I-V data. A plot of ℓn I vs. V in the forward diffusion region is made (see Fig. 8) and the line is extrapolated to the voltage axis. For this measurement, a Richardson constant of 100 amps/cm^2/°K^2 was assumed.

4.1.4 Comparison of Results of Various Schottky Barrier Height Determinations.

All the above experiments were conducted at 300°K. The following is a tabulation of the results:

Table I. Comparison of Schottky barrier height of Cr-Au to $Ga_{.45}Al_{.55}Sb$ as determined by three methods

Method	Schottky Barrier Height (eV)
Photoresponse	0.70
C-V	0.74
I-V	0.74

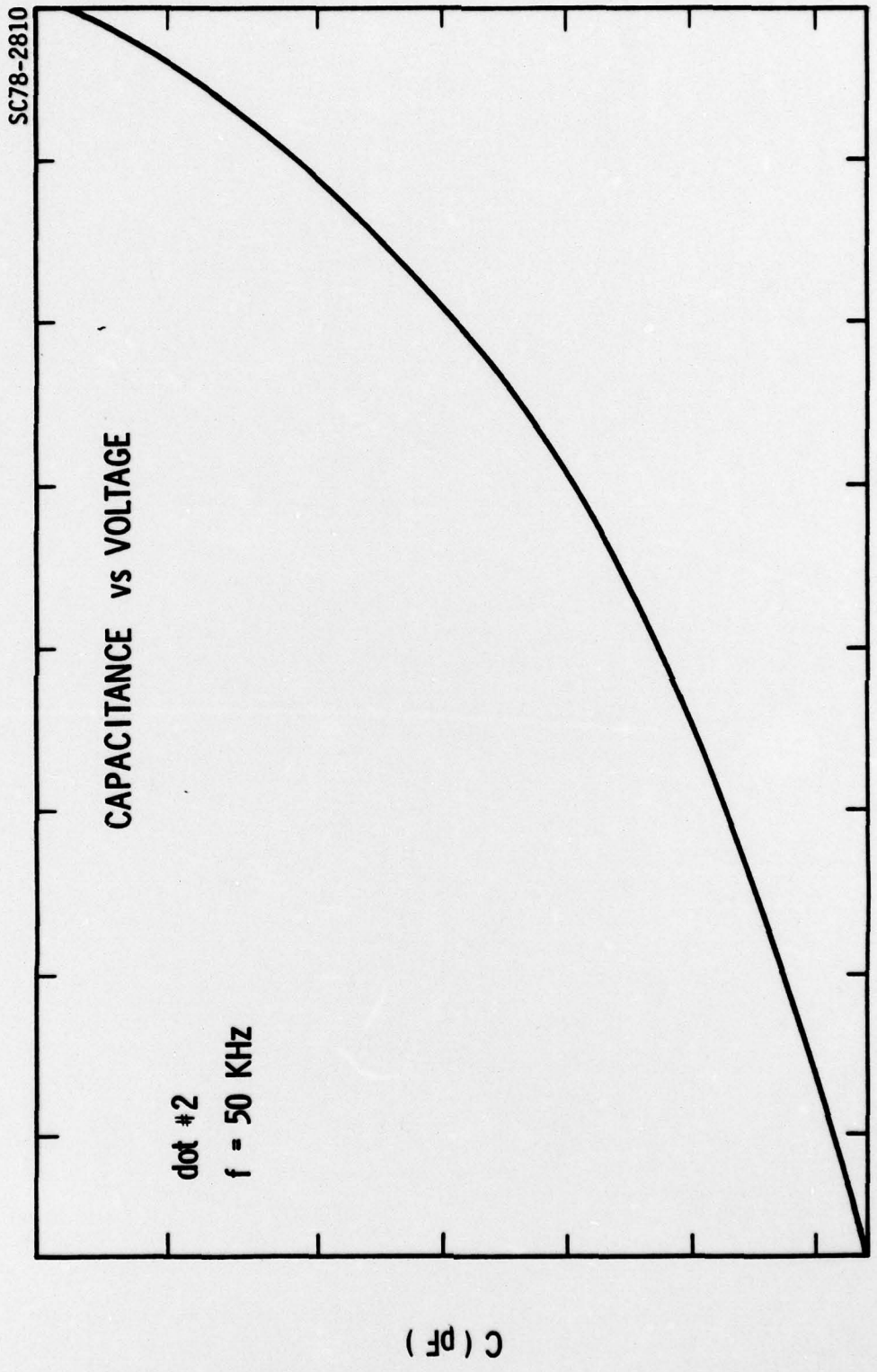


Fig. 6 Capacitance vs. voltage of Schottky barrier diode on $Ga_{.45}Al_{.55}Sb$.

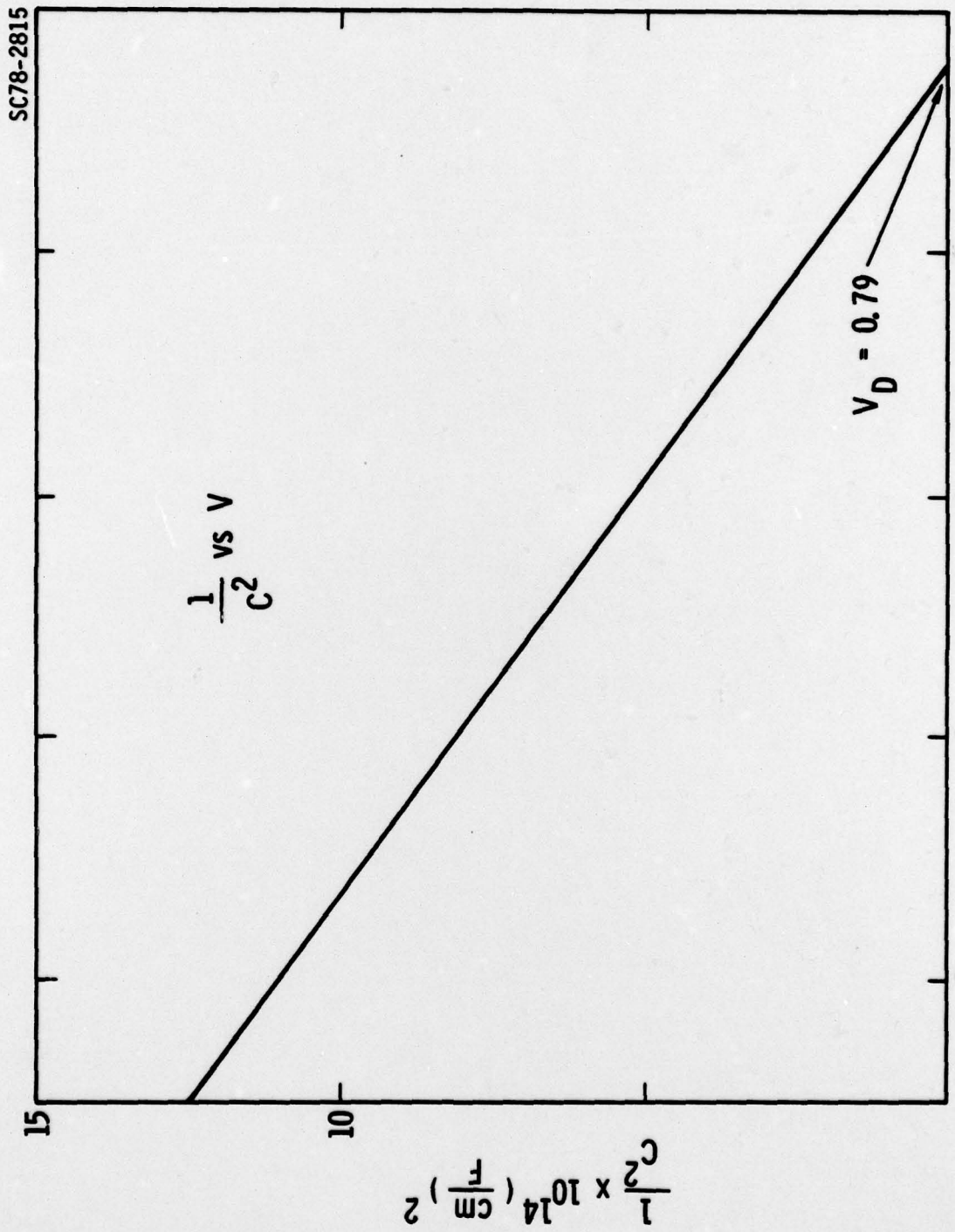


Fig. 7 Schottky barrier height determination from C-V data of Schottky barrier gate on $Ga_{.45}Al_{.55}Sb$.

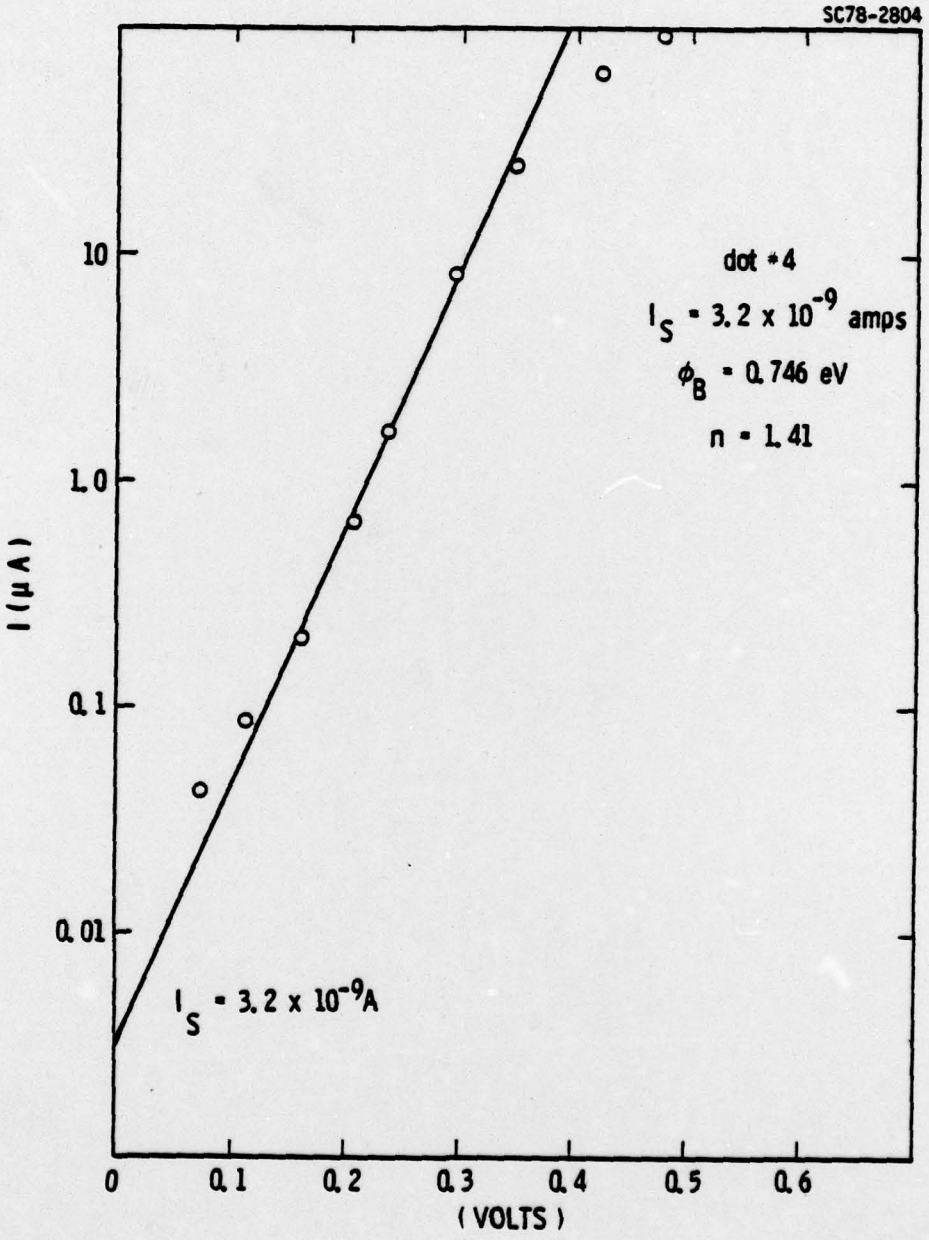


Fig. 8 Forward current-voltage characteristics of Schottky barrier gate on $Ga_{.45}Al_{.55}Sb$.

4.2 Carrier Concentration Profiles

Doping profiles were found using a PAR 41C C-V plotter interfaced with a Data General Eclipse computer. A dielectric constant of 15 was assumed. In general the results showed a uniform doping profile throughout the thickness of the layer. The resulting carrier concentration ranged from 8×10^{15} to 3×10^{16} cm^{-3}. A typical doping profile is shown in Fig. 9. The Schottky breakdown voltage ranged from 10-25 volts.

4.3 Layer Thickness and Punch-Through

In order to be able to operate the CCD, a total depletion (a punch-through) has to be achieved in the layer by applying a negative voltage to each gate and to the guard-ring surrounding the CCD structure. This voltage should be lower than the Schottky breakdown voltage. It was found experimentally that for layer doping of 10^{16} cm^{-3} and breakdown voltage of ~20 V, the layer thickness should be at most ~2.0 μm - in order to achieve punch-through.

The layer thickness was evaluated by several methods:

(1) Electron beam induced current
(2) Chemical selective-staining
(3) C-V measurements
(4) I-V measurements using a dot-guard-ring structure.

In order to verify if a punch-through can be reached under a single transfer gate, a C-V measurement was taken between a single transfer gate and the guard-ring surrounding the whole CCD structure (large Schottky contact compared to the single gate Schottky contact). An indication of punching-through is when a flat portion (constant capacitance) is observed in the C-V curve under reverse bias to the single transfer gate, (see Fig. 10). From this curve the layer thickness can be calculated given the gate area and the n-layer dielectric constant.

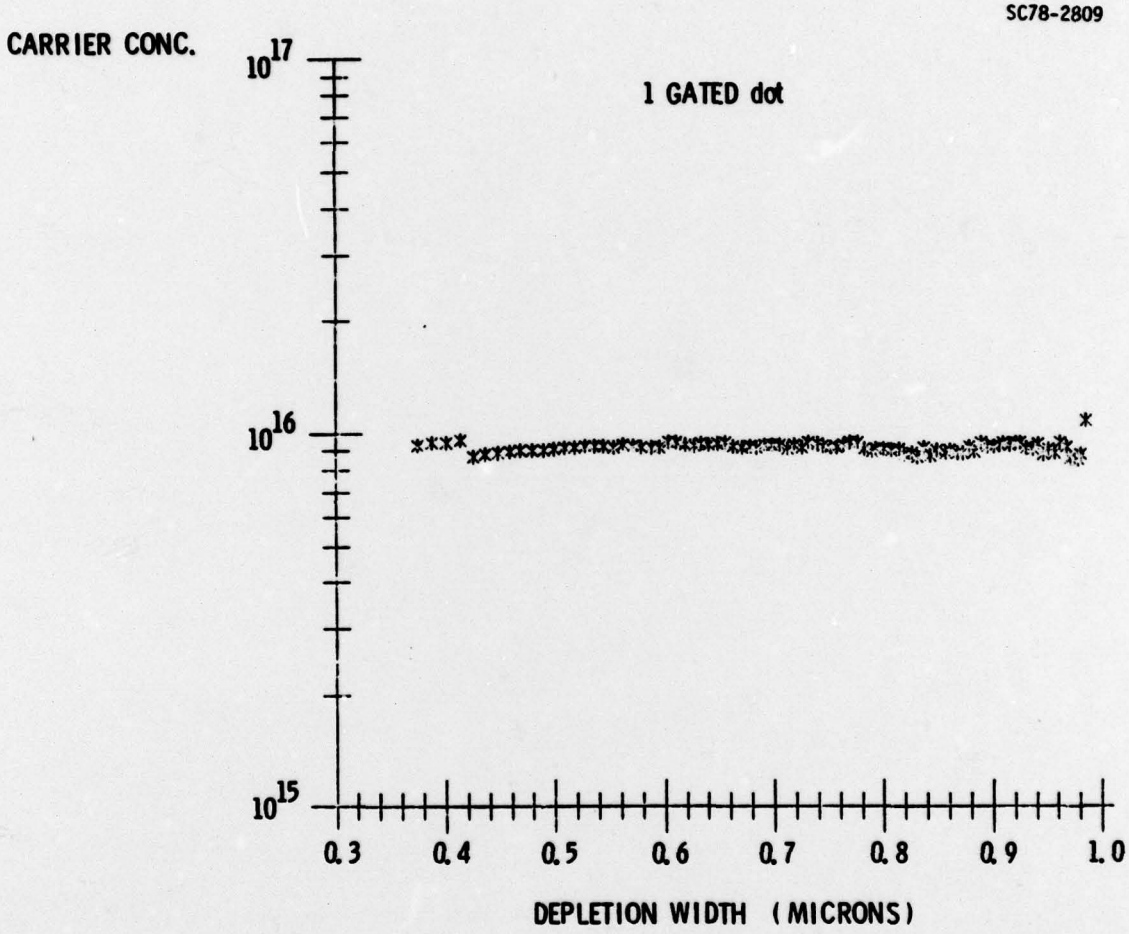


Fig. 9 Carrier concentration profile of n-type $Ga_{.45}Al_{.55}Sb$ epitaxial layer on p-GaSb substrate.

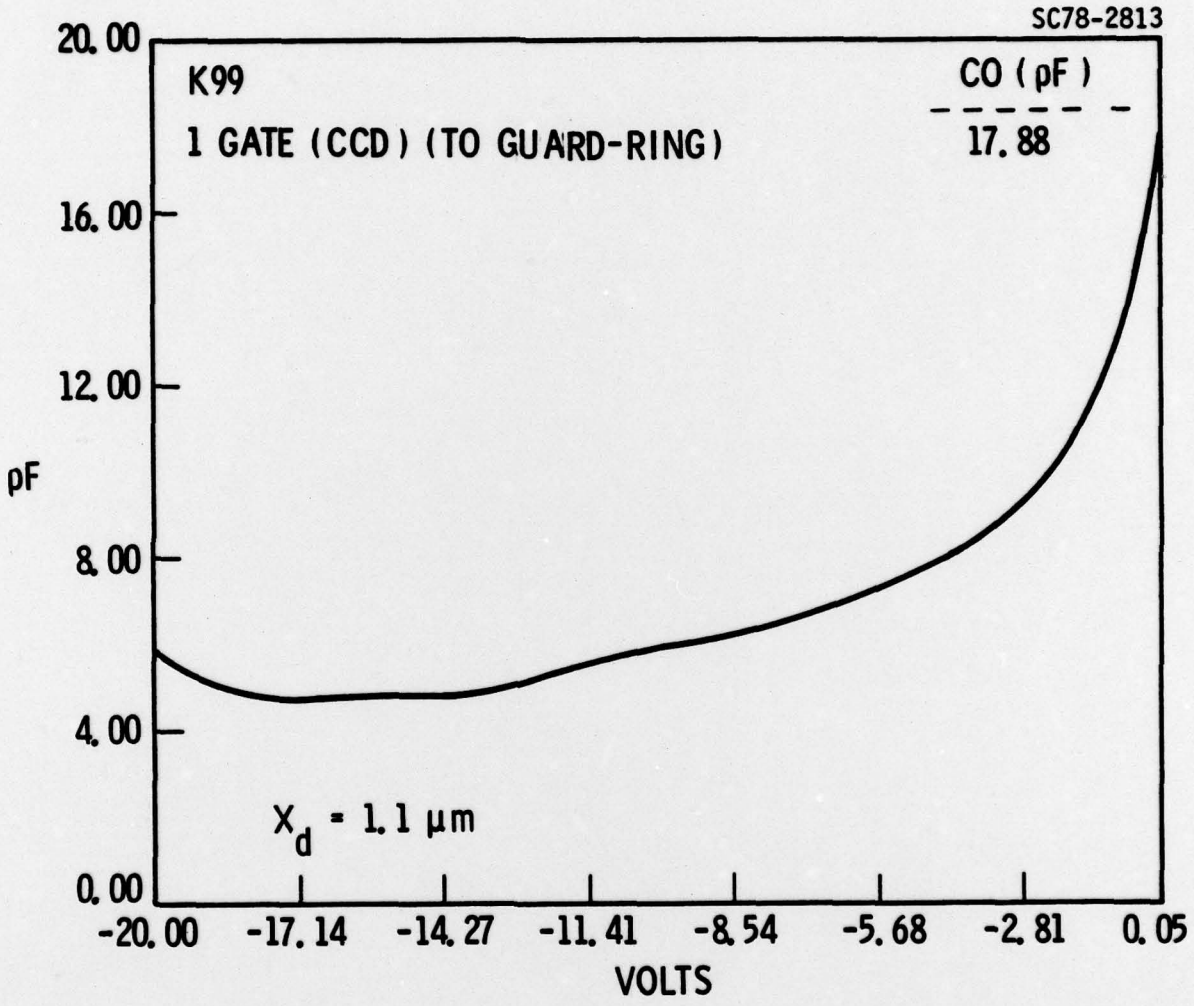


Fig. 10 Capacitance-voltage profile of $Ga_{.45}Al_{.55}Sb$/GaSb CCD measured between one transfer gate and guard ring.

4.3 P-N Junction Characterization

In our first mask design the area of a storage gate is 380 μm x 113 μm = 4.29×10^{-4} cm^{-2}. In thermal equilibrium a full "well" contains:

$$n = N_D Ad = 4.29 \times 10^8 \text{ electrons}$$

assuming: $N_D = 10^{16}$ cm^{-3}

$A = 4.29 \times 10^{-4}$ cm^2 (area)

$d = 1.0$ μm (thickness)

At an operation frequency of 100 kHz ($T = 10^{-5}$ sec) the corresponding current that can supply this charge per cycle is:

$$I = \frac{qn}{T} \quad F \ \mu A$$

In order to operate the CCD properly one has to be sure that the thermal generation current in the p-n junction is much smaller than the above number.

In order to evaluate the p-n junction leakage current a dot (area = 1.5×10^{-4} cm^2) surrounded by a guard-ring was used.

Using this structure, I-V measurement can be made and p-n junction characteristic can be evaluated by biasing the guard-ring to punch-through voltage and thus confining the dot area, eliminating the need for a mesa around the dot.

Using the guard-ring allows us to study the effectiveness of the guard-ring for later use of this concept in the real device as a channel stop.

Figure 11 shows the current through a dot (area = 1.5×10^{-4} cm^2) as a function of the voltage on the guard-ring for different dot voltages (p-n junction reverse bias) (this layer was quite lightly doped and thicker than

usual: BV = 36 V, d = 3.5 μm, N_D = 7 x 10^{15} cm^{-3}). It is seen that a dot area confinement, a punch-through underneath the guard-ring occurs at a guard-ring voltage of about -30 V.

I-V characteristics and the effect of the guard-ring are shown in Fig. 12 (room temperature) and Figs. 13 and 14 (77°K). The leakage current at 1 volt p-n junction reverse bias (77°K) is sufficiently low - (less than 1.0 nA corresponding to 6.25 x 10^4 electrons area = 4.29 x 10^{-4} cm^2, f = 100 kHz) to allow CCD operation.

In order to evaluate the surface leakage current when using a mesa structure, a mesa structure was etched around metal patterns with different areas and it was found that the p-n junction leakage current is proportional mainly to the gate area rather to its perimeter suggesting that the surface leakage current on the mesa edges is small compared to the p-n junction bulk leakage current. That the surface leakage current is small was verified by using EBIC response from the mesa edge near the p-n junction.

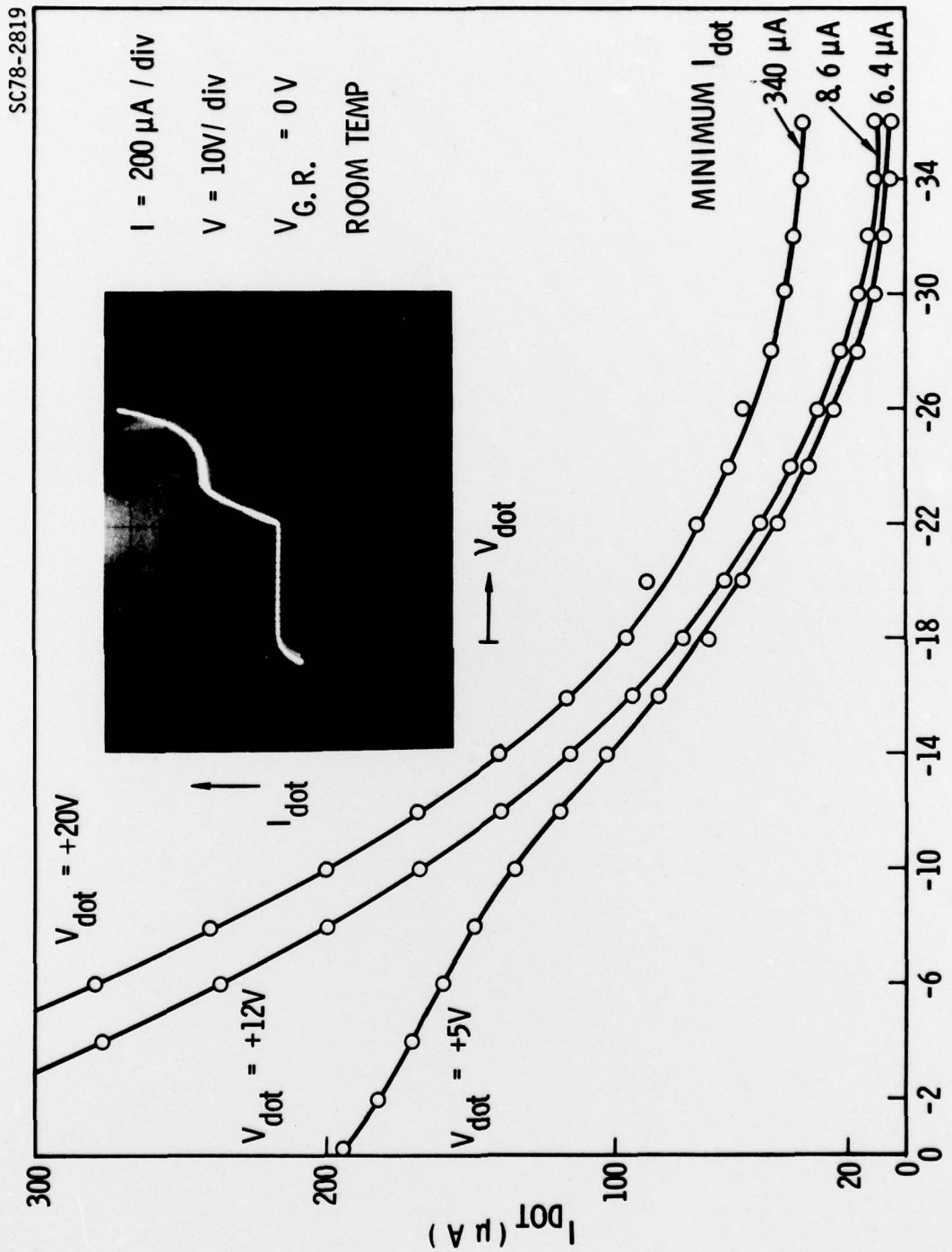


Fig. 11 p-n junction leakage of n-GaAlSb/p-GaSb heterojunction as a function of guard ring voltage. Inset shows p-n junction leakage (first quadrant) with zero guard ring voltage.

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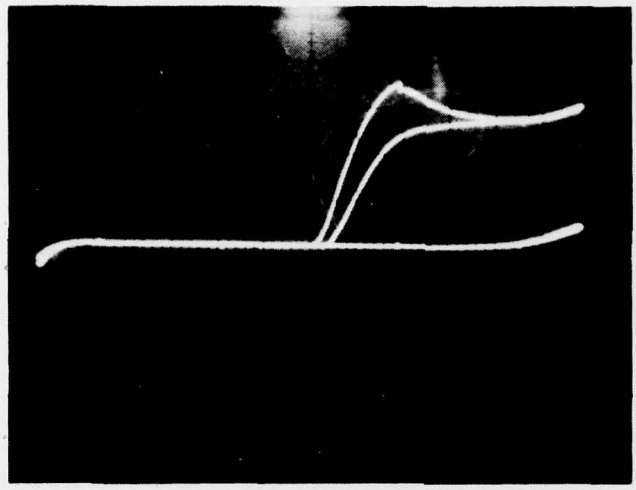
(GaSb SUBSTRATE IS GROUNDED)

KN55a
(WITH GUARD-RING)

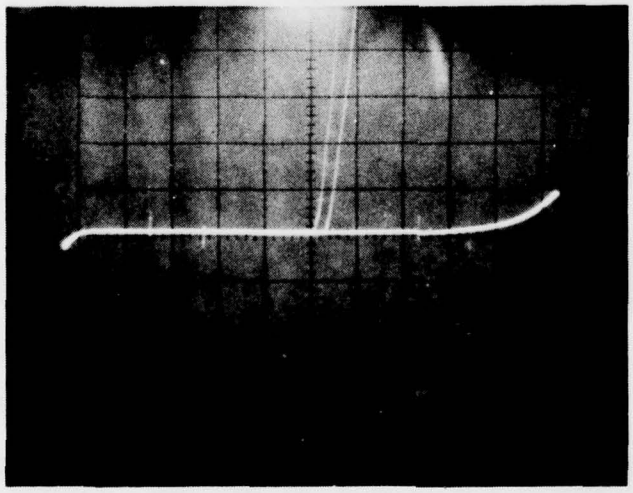


10 μa/div

2V/div

0 VOLTS AND -12V
TO THE GUARD-RING

SCHOTTKY REVERSE← →P-N JUNCTION REVERSE BIASED



2 μa/div

2 V/div

OV AND -12V TO
GUARD-RING

Fig. 12 Room temperature p-n junction I-V characteristics of n-GaAlSb/p-GaSb heterojunction showing effect of guard ring bias.

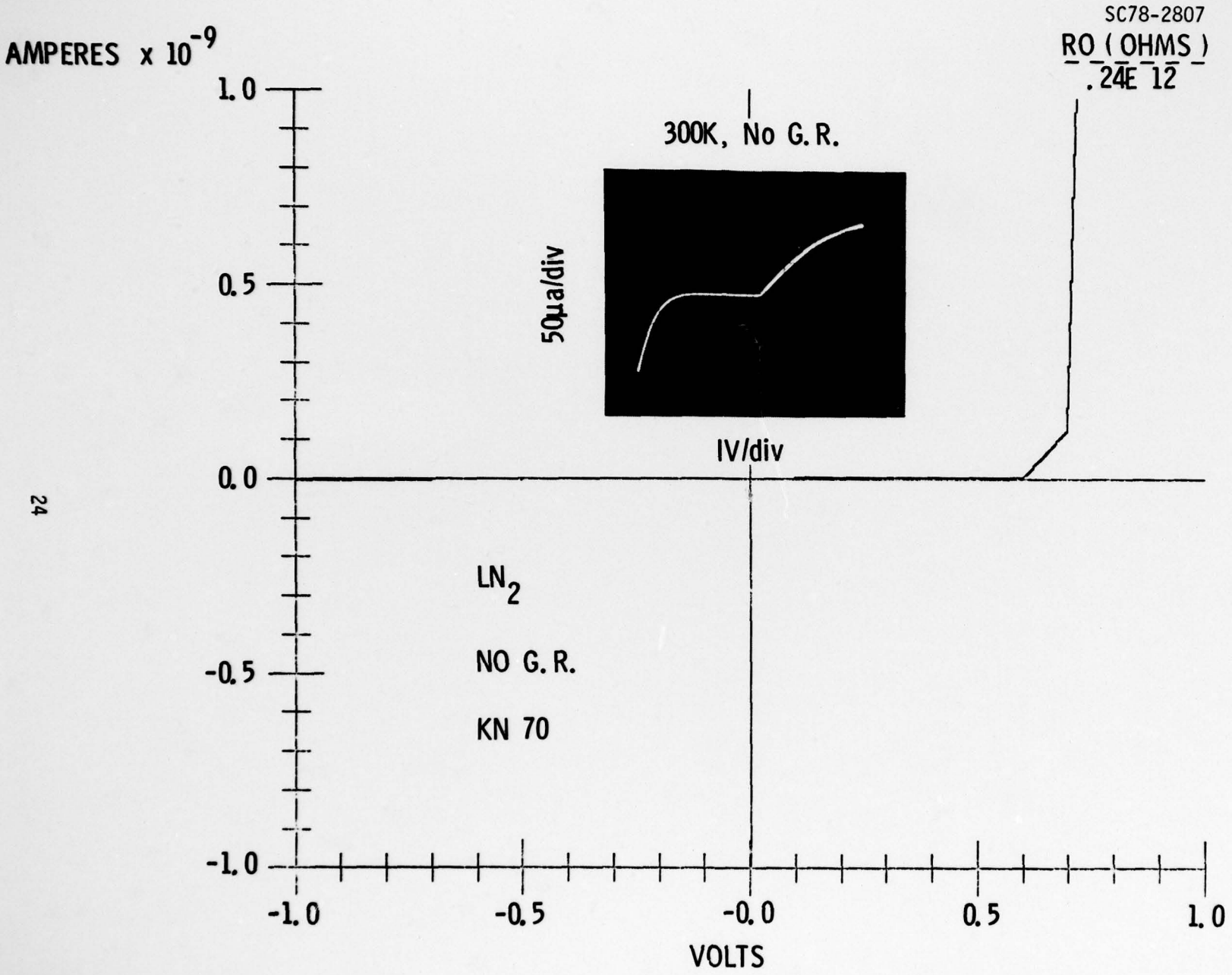


Fig. 13 Leakage current of Schottky barrier gate on n-$Ga_{.45}Al_{.55}Sb$ room temperature (inset photo) and at 77K.

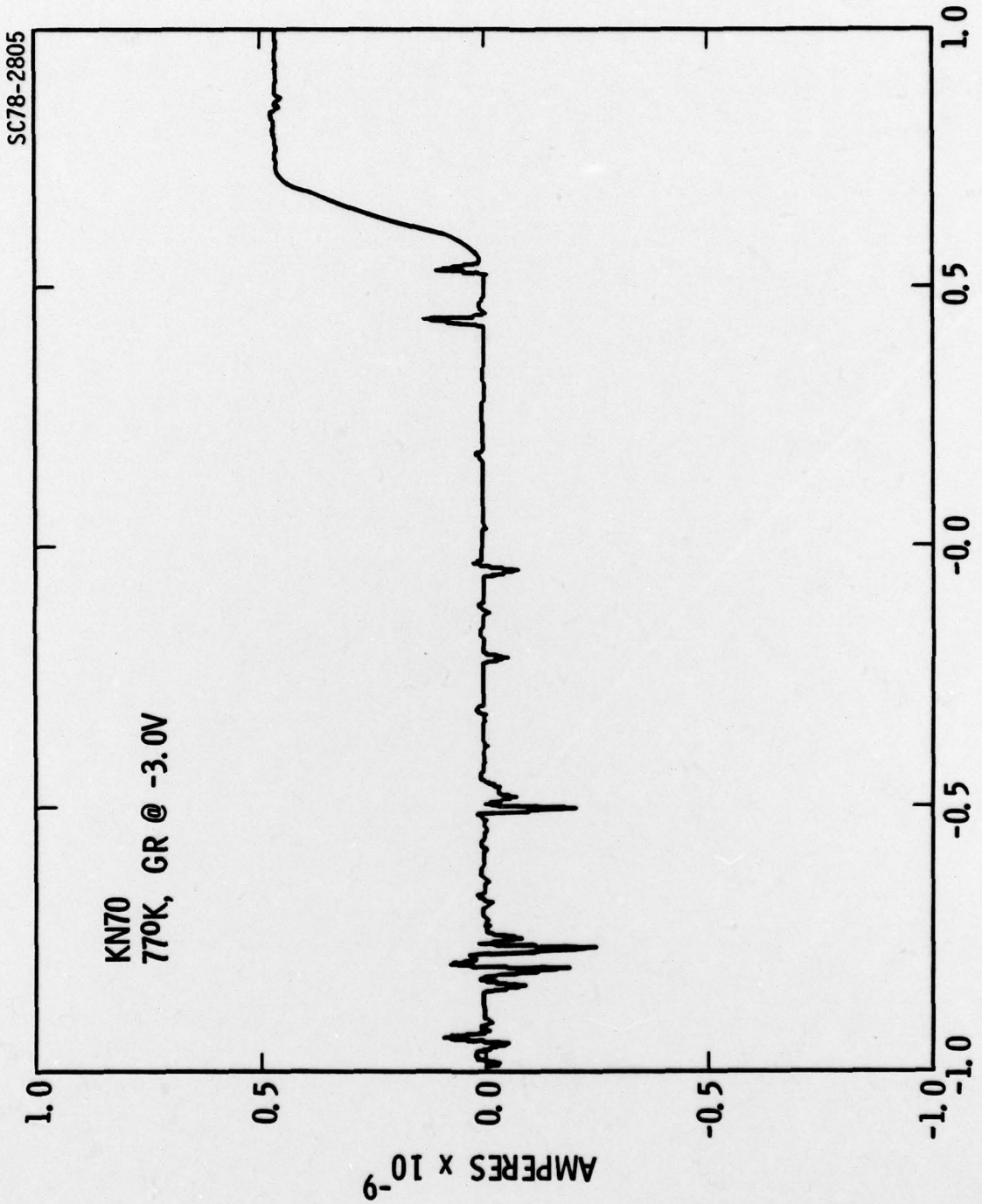


Fig. 14 Leakage current of Schottky barrier gate at 77K, expanded scale.

5.0 CONCLUSION

During this period, the most significant achievement was the dramatic improvement in surface morphology which was achieved by addition of As to the GaAlSb alloy. This new growth technique although incorporated late in the work period being reported here, has already resulted in substantially improved yield. An additional improvement which was not completed in time for this report is a revised mask set in which the device geometry has been reduced to approximately 2/3 the present device size. This will further increase the device yield to the point where a complete working device should be shortly obtained.

6.0 REFERENCES

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