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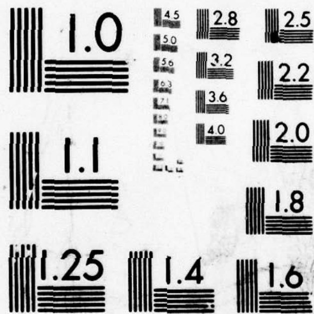

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DEVELOPMENT OF CHARGE TRANSFER DEVICES FOR 1-2 MICRON IMAGING

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I. Deyhimy, J. S. Harris, K. Wong

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by

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For

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There is considerable interest in the development of an imaging system within the wavelength range of 1.0 - 1.8μm. The concept of charge coupled devices emerges as one of the viable candidates for such an application. The advantages of a non-MIS, Schottky barrier, buried channel CCD, are discussed. Various configurations for backside illuminated devices are considered. The simplest representative configuration for evaluation of the concept consists of Schottky gates deposited on an active n-type channel supported by a p-type substrate.

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Analysis of the CCD shows that the optimum gap spacing is about 1 μm between gate electrodes to insure high charge transfer efficiency. Efforts in both materials growth and processing aimed at the development of this device are reported.

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1.0 INTRODUCTION

There are a number of military applications for a passive (available illumination) night vision capability. Technological advances in image intensifiers and high performance photocathodes have resulted in night vision systems which operate in the visible and near infrared spectrum under low level moonlight and starlight illumination. These systems are, however, completely ineffective under moonless or overcast conditions because of the low level of light in the 0.5-0.9μm region under such conditions. Since there is considerable night glow ambient illumination in the 1.0-1.8μm wavelength region which is nearly independent of cloud-cover, one solution to this problem is the development of an imaging system which operates in this wavelength region.

The development of a 1.0-1.8μm imaging system has been the goal of a number of research efforts over the past ten years. Most of these efforts have been directed at the development of a photocathode which would work in the 1.0-1.8μm region. In spite of the large number of device concepts examined, non has yet emerged as a viable candidate to meet the requirements for a 1.8μm imaging photocathode. A potential alternative to a photocathode for infrared imaging is the charge coupled device (CCD). While Si CCDs have recently come to the forefront for both visible and 3-5μm imaging applications, there are no suitable deep level impurities in this material for operation in the 1-2μm region. Furthermore, Si devices designed for 3-5μm, require cooling to ~40K for satisfactory operation. Such cooling requirements would make Army night vision devices prohibitively expensive and would place

unacceptable restrictions on virtually all of the 1-2μm imaging systems envisioned for Army applications. CCDs developed in new materials with high optical absorption coefficients in the 1-2μm region offer a viable solution to the systems requirements for a 1-2μm imaging system.

The approach that we are pursuing in this program is the development of a non-MIS heterojunction CCD in a narrow gap semiconductor. This approach is chosen because of the present lack of a viable MIS technology for materials other than silicon and recent developments at the Science Center on non-MIS devices. In spite of the extensive studies of III-V MIS devices, significant problems still remain to be solved in order to fabricate a useful III-V MIS CCD. While significant progress has been made in reducing the surface state density on some MIS structures, the mobile ion and insulator stability problems in low temperature deposited or anodic insulators have remained. These problems prevent the realization of an MIS CCD with stable and reproducible characteristics.

There is now reason to believe that a buried channel heterojunction may not only avoid the above problems associated with insulators in an MIS CCD but offer certain inherent advantages which render it more suitable for the 1.8μm imaging application. Some of these advantages are:

(1) A built-in antiblooming capability without the use of special channel stop regions

(2) Superior radiation hardness to both particle (electrons, protons) and photon (x-rays, gamma rays) irradiation

(3) Greater dynamic range because of low charge generation and absence of an insulator

(4) High optical quantum efficiency achieved with intrinsic direct bandgap III-V materials

(5) Lower dark current because the electric field is confined to a wide bandgap charge transport layer in a heterojunction device.

Thus, heterojunction CCDs promise a very exciting approach to 1-2μm imaging. While several material systems are potential candidates for this application, the GaAlSb-GaSb system is selected for the first development phase because it offers the potential to demonstrate a heterojunction CCD with a relatively simple Schottky barrier structure. We also have extensive experience in device applications of this material system. With this material system, at the expected average signal levels in this application, photon shot noise limited operation should be realizable.

During the first contract period several important milestones have been reached. The GaAlSb/GaSb system has been developed to the point where device structures of n-type $Ga_{.45}Al_{.55}Sb$ on p-type GaSb with the desired epitaxial layer uniformity and doping are routinely achieved. The remaining material problem is the surface morphology. This problem also appears to be near solution. All the fabrication steps required for producing the initial devices are developed and under control. In addition, the necessary electronics required for generating the clock pulses for the three-phase CCD are operational. Thus, at this point, we are on the threshold of producing the first GaAlSb/GaSb CCD.

2.0 DEVICE DESIGN

The ultimate goal of this program is a high resolution, large area, imaging CCD, sensitive to radiation in the 1.0-1.8μm region. The choice of materials is, therefore, dictated by the requirement for efficient photogeneration, i.e., the absorption of the IR radiation in a material with bandgap less than the photon energy of interest and creation of free electrons in the conduction band. Also, crucial to the successful operation of a low light level CCD is the ability to achieve low dark current at reasonable temperatures.

The best choice for the optical detector material is a III-V alloy whose bandgap has been adjusted for efficient optical absorption at the wavelength of interest, and the ideal device design is a heterojunction structure. Optical detectors fabricated from heterojunctions of III-V compounds have demonstrated near unity quantum efficiency. Thus, in the CCD case, the optical absorber layer composition and, therefore, bandgap is adjusted to have high optical absorption out to 1.8μm (0.69 eV), and a heterojunction is formed between this absorber and a wide bandgap alloy (the charge transport layer) which is transparent to the wavelength of interest. All of the light is absorbed very near the p-n junction and high quantum efficiency is obtained. Equally important, since the charge transport layer is a wide bandgap material, the dark current is orders of magnitude lower than if a homojunction device were used. Experimental verification of the feasibility of a Schottky gate CCD, such as proposed here, has been verified in this laboratory using GaAs.* This device is described in Appendix I.

*This work is supported under IR&D

2.1 Material Selection

High optical absorption in the 1-2μm region requires an energy gap, $E_g \leq 0.7$ eV. The possibilities include Ge, InGaAs, InAlAs, InAsP, GaSb, InPSb, InAlSb. Of these materials, InAlAs, InAlSb, InPSb can be eliminated because they have potential miscibility gaps in the solidus over certain composition ranges and there are no suitable substrates. Ge is a poor choice because a wide bandgap heterojunction channel layer is absolutely essential to meet the dark current requirements. Since all of the GaAs-Ge heterojunctions(1-3) produced to date exhibit very high tunneling currents, the lack of heterojunction potential eliminates Ge as the absorber. Of the remaining three materials (InGaAs, InAsP and GaSb), only InGaAs and GaSb have readily available lattice matching substrates and a suitable wide bandgap heterojunction potential. Thus, two candidate materials systems emerge from the above requirements: (1) GaSb absorber and $Al_{.55}Ga_{.45}Sb$ channel or (2) $In_{.53}Ga_{.47}As$ absorber and InP channel with GaSb or InP substrates, respectively.

Both of these materials systems have been studied extensively over the past four years, and operating device structures have been made with each system. We have grown both alloy systems by liquid phase epitaxy, and our choice of the GaSb-AlGaSb for this investigation is based upon this experience. The factors which favor the GaSb-AlGaSb system are the following:

(1) We have successfully grown n-$Al_{.55}Ga_{.45}Sb$ on p-GaSb and observed photoresponse between 0.9μm and 1.8μm in the photodiodes. This indicates that no heterojunction or

combination of a p-p heterojunction and wide bandgap p-n homojunction[4] electron barrier exists.

(2) The doping density of n-$Al_{.55}Ga_{.45}Sb$ can be controlled in the 10^{15} cm^{-3} range and complete carrier depletion has been achieved on a number of p-n-p structures with this alloy.

(3) Excellent Schottky barrier diodes with high reverse breakdown voltages have been fabricated on $Al_{.55}Ga_{.45}Sb$.

(4) The AlGaSb-GaSb system will operate out to ~1.73μm while the InP-InGaAs will only operate out to ~1.65μm. This very small difference in long wavelength cutoff creates an ~30% decrease in signal because of the night sky radiation distribution.[5] This is a serious loss to an already small signal. The GaSb alloy system offers a potential to increase the long wavelength response to 1.8μm at 200K by using $Ga_{.94}In_{.06}Sb$ as the absorber and capture an additional 15-20% signal over the GaSb or nearly double that of the InGaAs. This alloy may also be advantageous for maximum device performance because this alloy is a perfect lattice match to the $Al_{.55}Ga_{.45}Sb$ channel layer. An improved lattice match at this interface will reduce the number of interface states and may thus reduce the noise and dark current generated by these states.

Thus all of the required materials parameters have been already realized with this alloy system and the proposed CCD research effort can be devoted entirely to device design, fabrication and characterization.

In the InGaAs-InP system, neither long wavelength photoresponse nor the low doping with punch through has been demonstrated. Our experience with LPE growth of this system indicates that the lattice matched quaternary alloys of InGaAsP grow well on InP. However, as one approaches the InGaAs ternary alloy, there is a strong tendency for etchback into the InP and the junction quality is very poor. When sufficient P has been added to eliminate this problem, the long wavelength response has been reduced to $\sim 1.3 \mu m$. This type of etchback phenomena is commonly observed in composition (i.e., similar etchback has been observed in $Al_xGa_{(1-x)}Sb$ on GaSb with $x > 0.8$ and $Al_xGa_{(1-x)}As$ on GaAs with $x > 0.9$). The thermodynamic instability responsible for this etchback has been described in considerable detail in our prior work with AlGaSb on GaSb.[4,6] One final problem for the InP system is that the Schottky barrier height to n-InP is very low. This virtually precludes the early demonstration of charge transfer using the Schottky gate approach.

The AlGaSb-GaSb is clearly the more attractive material system because of the large amount of materials and processing research experience which has been amassed in this system.

2.2 CCD Configurations

The original focal plane device design utilizing a double heterojunction CCD concept (reference Fig. 2.1 in first quarterly report covering period May 11, 1977, through August 10, 1977)[7] has been abandoned. This is the result of mutual agreement with NVL. As a result of discussions with NVL, a somewhat simpler device structure (to be discussed

subsequently) has been substituted. This new device requires bonding the epitaxially grown structure to glass, saphire, or other suitable IR transmitting substrate and subsequent etching of the original semiconductor substrate. We believe that this scheme, while introducing two new unknowns, i.e., the bonding and etching operations, sufficiently simplifies the original proposed device structure as to make it attractive. Moreover, the currently ongoing work on the initial device structure previously described in the first quarterly technical report[7] and shown schematically in Fig. 2.1, is subsequently transferable to the ulitmate device. The implementation of this device is shown in Fig. 2.2. The desirability of the device of Fig. 2.2 as a "demonstration vehicle" stems from its simplicity. Thus, crsytal growth and processing requirements are simplified. At present, a total of three separate mask sets have been fabricated. The characteristics of the masks will be described subsequently in this report.

The material being investigated using the Schottky device as a vehicle is the GaSb-GaAlSb system. The device is illuminated through the Schottky gates. Light transmitted through the Schottky gates passes through the transport channel without attenuation and is absorbed within the first few thousand angstroms of the P-GaSb. Since the absorption length between 1 and 1.8μm in this material is much smaller than one diffusion length, most of the photogenerated hole-electron pairs contribute to stored charge in the channel. The absorber material is heavily doped ($N_a \simeq 10^{17}/cm^3$) so that the electric field will extend only a fraction of a micron into this material, thus limiting the g-r contribution to the dark current from the absorber. The total dark current in this device should be extremely low at the 200K

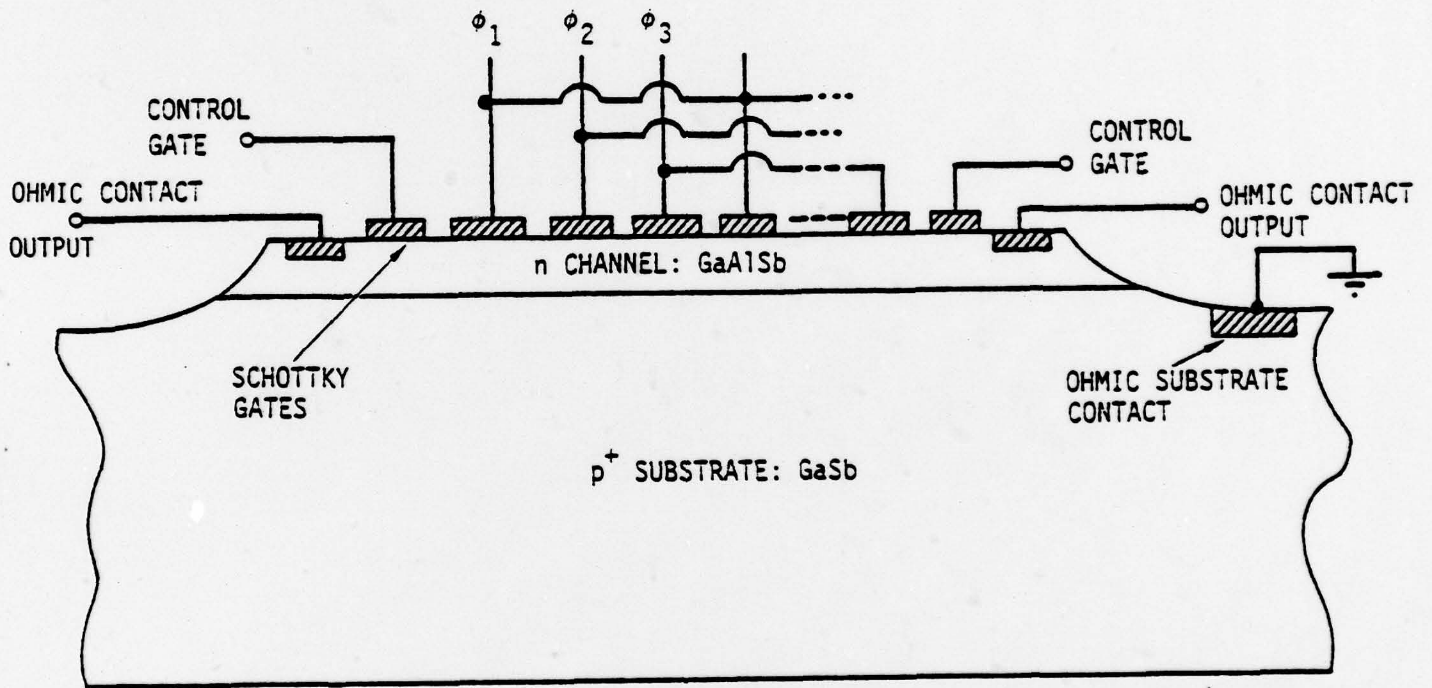


Fig. 2.1 Schottky Gate CCD Structure

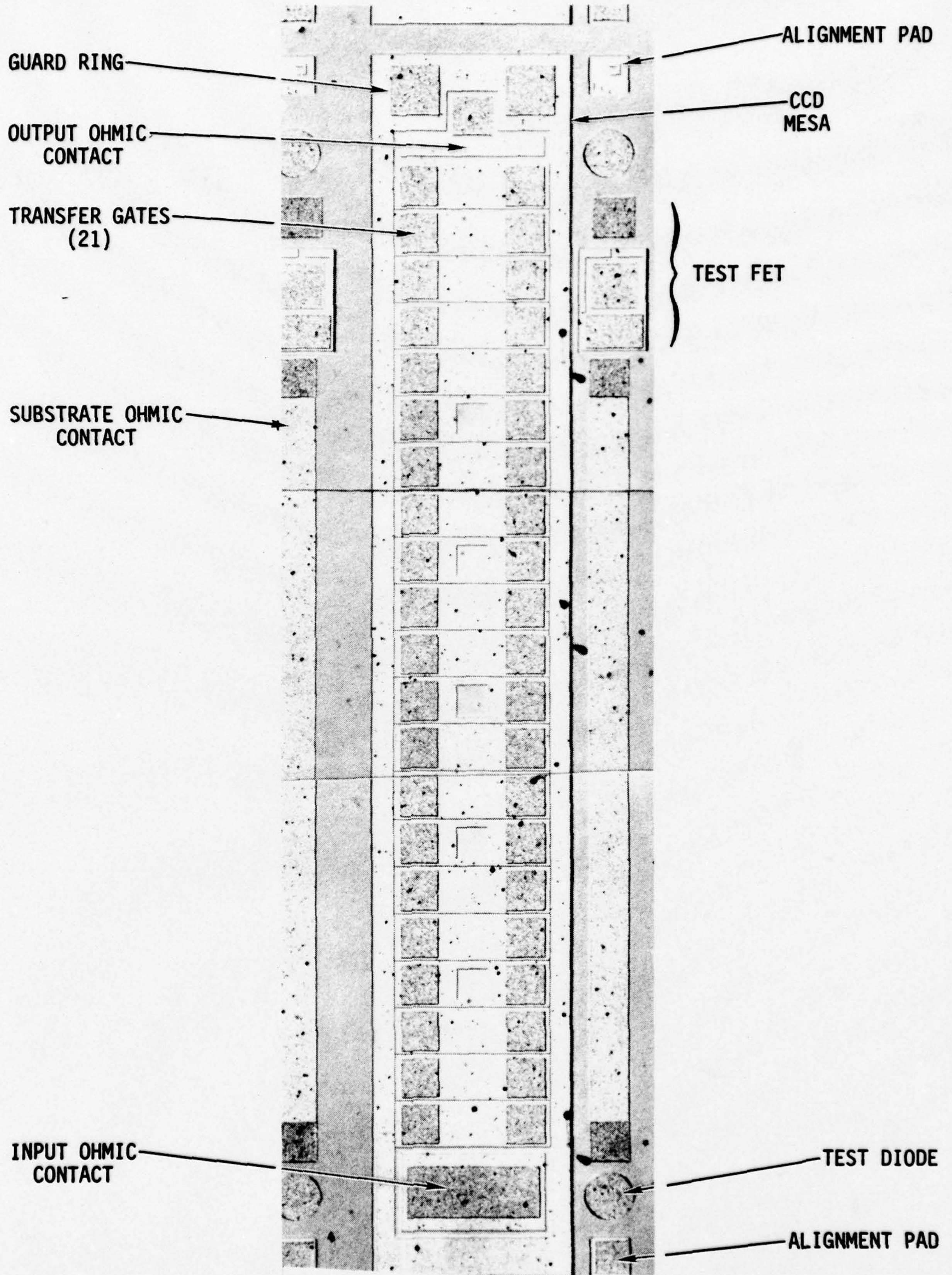


Fig. 2.2 Photograph showing the as processed GaAlSb/GaSb heterojunction Schottkv gate CCD. (revised 7/78)

operating temperature because of the wide bandgap channel layer and the substantial Schottky barrier height in GaAlSb. This initial device is not intended to demonstrate the ultimate in charge detection sensitivity since the substrate is highly doped, leading to relatively high output node capacitance. It will, however, serve as a tool for investigating charge transfer efficiency and on-chip FET performance. Both of these parameters are important. The first, obviously, the latter for determining the charge readout sensitivity.

2.3 Device Modeling

The model developed to calculate the potential profiles under an individual CCD gate(7) can be used to determine the potential depth in the channel under various gate voltage and stored charge conditions. The results of this calculation for the parameters pertaining to the GaAlSb/GaSb CCD are shown in Fig. 2.3. It can be seen that, as long as the gate voltage is below about 6 V, 1×10^{12} electrons/cm^2 can be stored under a gate. For a 25μm x 25μm pixel, assuming a three-phase CCD, this corresponds to about 2×10^6 electrons. Of course this calculation applies both to the demonstration device and the ultimate focal plane CCD.

The above one-dimensional calculation is valid for a region under an electrode far away from the edges of the gate. A region of primary interest for device design is the region between the gates because this governs charge transfer efficiency. In the gap region, the surface potential is no longer pinned by the metal gate and the potential in the semiconductor can be much more positive than under the gates. This means that there will be a tendency

Fig. 2.3 Calculated electron potential energy vs. distance under an individual HJCCD gate.

for electrons to be trapped in the regions between the gates if this gate spacing is too large. In order to design a device for high transfer efficiency, it is vital to be able to calculate the magnitude of this potential between the gates as a function of gate spacing.

A rigorous calculation on analytical basis of the two-dimensional potential distribution problem for the region of a gap between electrodes in the heterojunction CCD structure would be very difficult. Fortunately, the effect of the gap is a relatively small perturbation on the one-dimensional problem and it is possible to treat this two-dimensional problem, to a high degree of accuracy, by a perturbation approach. The details of the technique for doing this were discussed in the quarterly report.(7) The effect of the gap on the potential distribution is important; since if the gap is too large, charges can be trapped and transfer efficiency is reduced. Figure 2.4 shows the effect of a 1μm gap on the potential distribution between two adjacent gates which are held at different voltages. Thus, with a 1μm gap, no potential barriers or traps exist between the gates.

2.4 Device Design Goals

The initial device is a Schottky barrier gate linear array with an n-type $Ga_{.45}Al_{.55}Sb$ layer on a p^+-GaSb substrate. The layer is 2μm thick and the doping, $N_D \simeq 1 \times 10^{16}$ cm/^{3}, while the substrate is $N_A \simeq 1 \times 10^{17}$ cm/^{3}. The device is fabricated on a mesa. This CCD has a total of 21 gates as well as ohmic contacts for the input and the output. The gate spacing is between 1μm and 1.5μm. The main technologies required to fabricate the device are the heteroepitaxial growth of the GaAlSb/GaSb

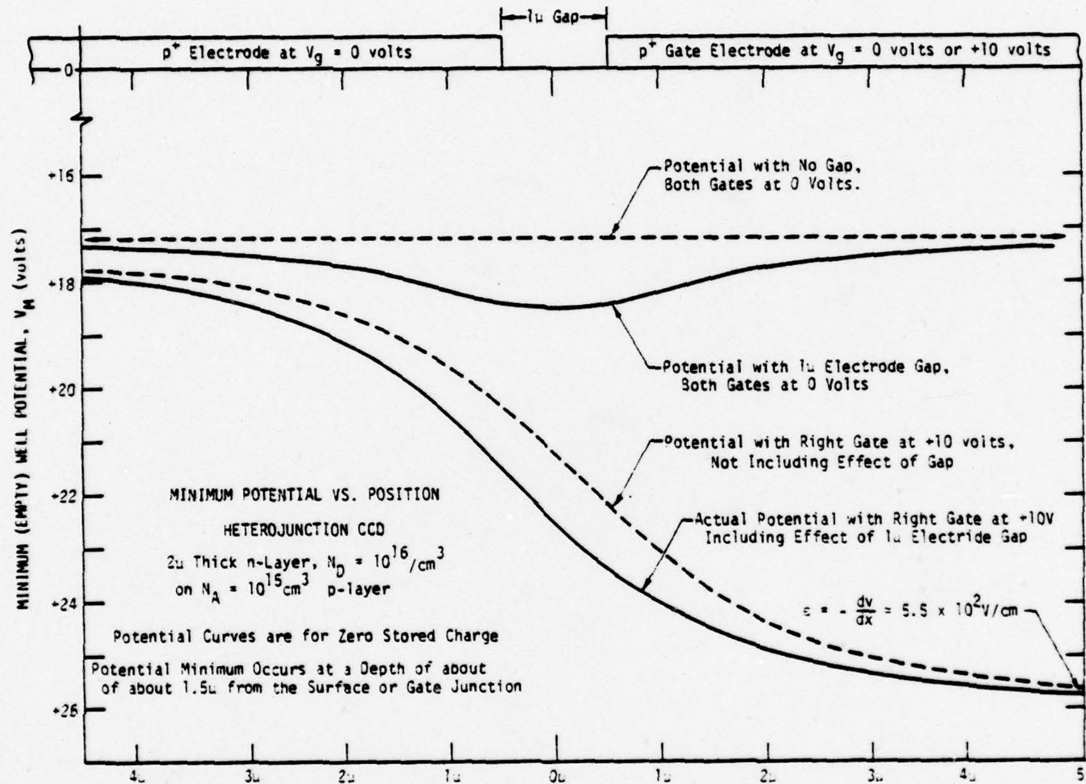


Fig. 2.4 Potential distribution between two adjacent gates for gate spacing of 1μm.

structures, ohmic contacts and the deposition of closely spaced Schottky barrier gate metalization patterns. This device will provide important data which will impact material and device design choices for subsequent phases of the program. The focus of the early measurements on the first devices will be to evaluate charge transfer efficiency and dark current vs temperature and to relate these to material and device design parameters. At this point we are close to demonstrating this device, the only major problem being availability of a sufficiently defect-free surface on the grown epilayer.

A brief examination of the requirement for a 400 x 400 element focal plane with 25μm resolution elements, reveals that a backside illuminated device design is essential. Since the GaSb substrate is opaque to 1-2μm radiation, the following configuration is proposed: n-GaAlSb is grown on p^+ GaSb just as in the initial device structure of Fig. 2.1. A p^+ ($N_A \simeq 10^{17}$ cm^{-3}) GaInSb absorber layer ($\simeq 2\mu$m thick) is then grown on top of the n-GaAlSb layer. This is followed by a relatively thick ($\simeq 5\mu$m) p^- GaAlSb layer. SiO_2 is sputtered or evaporated onto the top p^- GaAlSb layer. This structure is then fused to a suitable glass substrate, possibly Corning 7056. The p^+ GaSb substrate is then removed by a selective etch which etches p-GaSb much faster than n-GaAlSb. The CCD metalization pattern is then fabricated on the new surface of GaAlSb, similar to the device of Fig. 2.1.

This configuration has the advantage of utilizing all the technology developed for the initial device of Fig. 2.1. The significant problems to be addressed are selection of an IR transmitting glass with a low enough softening temperature so as not to degrade the semiconductor junctions and a

selective etch which etches p-GaSb much faster than n-GaAlSb. Figure 2.5 illustrates the steps in the fabrication of this device. The initial device of this configuration will be a one-axis CCD with optical input.

The existence of GaSb/GaAlSb heteroepitaxial technology at the Science Center coupled with the availability of glass-semiconductor fusing technology at NVL enhances the chances of realizing a 1-2μm focal plane in the near future.

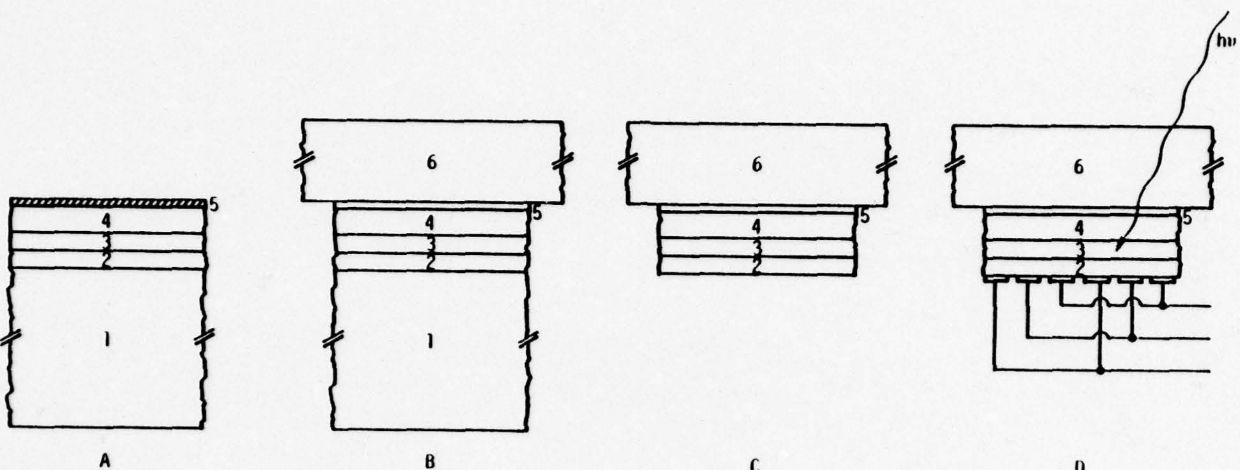


Fig. 2.5 Proposed scheme for fabricating backside illuminated CCD. a) As grown layers of n-GaAlSb channel (2), p-GaSb absorber (3), p-GaAlSb confinement and passivation layer, and sputtered SiO_2 (5) all on p^+-GaSb (1).
b) Glass is fused onto structure. c) p^+GaSb substrate is etched away.
d) Device is processed.

3.0 MATERIALS GROWTH AND CHARACTERIZATION

3.1 GaAlSb Growth

The major effort in the materials growth area during this reporting period has been the growth of n^{-} - $Ga_{0.45}Al_{0.55}Sb$ on p^{+} - GaSb by liquid phase epitaxy. Undoped <100>GaSb substrates were used. The as received substrates were grown p-type, having a reported carrier concentration of 1.7×10^{17}.

The substrates were prepared by mechanical lapping to the appropriate thickness, followed by chemical-mechanical polish in cabosil with H_2O_2 and water. The polished substrate had shiny surfaces free from any visible subsurface damage into the substrate. Experimentation with various etchants resulted in the discovery that bromine-methanol, mixed in the ratio 1:30 removes all surface damages while still maintaining a planar polished surface. The substrate preparation established thus far is shown below:

(1) Lapping in 3μm grit abrasive
(2) Polishing in cabosil + H_2O_2 + water
(3) Solvent cleaning
(4) Two minutes etch in HF to remove surface oxide
(5) Quench in methanol
(6) One minute etch in 1:30 bromine-methanol, with constant agitation
(7) Quench in methanol followed by rinsing in isopropyl alcohol.

In order to have good control of carrier concentration in the p-side of the junction, a buffer layer of undoped GaSb is grown on the substrate.

Both the GaAlSb layer and the buffer layer are grown at approximately 500°C. The composition of the melts was designed according to the 500°C liquidus (Fig. 3.1) and solidus (Fig. 3.2) GaAlSb ternary phase diagram calculated by Harris.[8] The composition of the GaAlSb melts was so designed that their saturation temperatures were about 2°C below that of the GaSb melt so that continuous growth of consecutive layers is possible. Unlike the GaAs system, there is another parameter in the LPE growth which is just as important as the saturation temperature. Namely, the temperature T_c at which spontaneous nucleation and growth of the solid phase occurs in the melt. T_c is extremely important in the GaSb system because the difference between the saturation temperature T_s and T_c is very small. Therefore, the initial growth temperature and the cooling rate have to be carefully controlled so that the temperature throughout the growth will not fall below T_c. Maintenance of this condition is essential because, if the temperature falls below T_c during the growth, crust formation will occur. In such a case, the Sb and Al in the melt will be depleted rapidly, causing etchback at the substrate.

During the initial stage of the LPE growth, surface wetting problems were encountered. The same problem with the growth of GaAlSb on GaSb had previously been reported both at the Science Center[9] and also by A. A. Vilisov et al. in Russia.[10] Harris[11] in an ESCA study discovered that the surface wetting problem was due to chloride contamination. However, in the present case, no high chloride reagents were used. Experiments with various solvents indicated that boiling in isopropyl alcohol, at the end of step 3 in the substrate preparation procedure, improved

.10
.01
.001

550
500
450
400

.02 .06 .10 .14 .18 .22

ATOM FRACTION Sb IN LIQUID, N_{Sb}

ATOM FRACTION Al IN LIQUID, N_{Al}

Fig. 3.1 AlGaSb liquidus isotherms
Experimental data points at 500°C and calculated fit using the values of Table 1.

Fig. 3.2 $Al_xGa_{(1-x)}Sb$ Solidus isotherms
Experimental data points at 500°C and computer fit using the values of Table 1.

the surface wetting. After incorporation of the above procedure, a number of good growths were achieved. However, boiling in isopropyl alcohol has not solved the problem in every case. Efforts in improvement of surface preparation techniques will be continued to reduce the surface wetting problem.

The surface condition of two of the layers is shown in Fig. 3.3(a) and (b). Figure 3.3(a) represents the surface morphology of an epitaxial layer grown at $4^{o}C$ supersaturation. Figure 3.3(b) represents the surface grown at $2^{o}C$ supersaturation. Comparison of the two cases shows that decrease of supersaturation results in tremendous improvement of the surface morphology. Further improvements will be pursued in order to make subsequent processing all right.

Jackson[9] has considered the problem of surface roughness of solids grown from a supersaturated melt and derived the following relationship.

$$\frac{\Delta G_s}{NkT_o} = \frac{\alpha N_A}{N^2}(N-N_A) - \ell n \left[\frac{N}{N-N_A}\right] - \frac{N_A}{N} \ell n \left[\frac{N-N_A}{N_A}\right]$$

where: G_s = free energy change per atom added to the surface

T_o = equilibrium temperature between the solid and the melt

N = total number of sites at the surface

N_A = total number of occupied sites

$\alpha \simeq (L/kT_o)f_k$

L = latent heat of the solidification process

f_k = fraction of all first neighbor lying in a plane parallel to the crystal face considered ($f_k = 1$ when the crystal face is the close-packed plane)

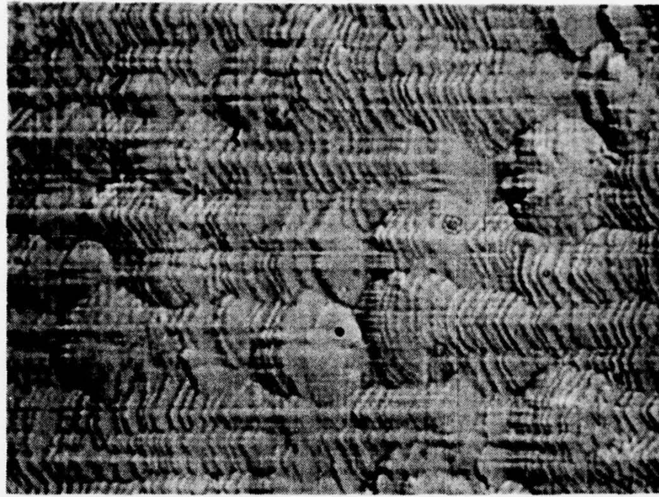


Fig. 3.3a Surface of the epitaxial layer of $Ga_{.45}Al_{.55}Sb$ grown at 4°C supersaturation.

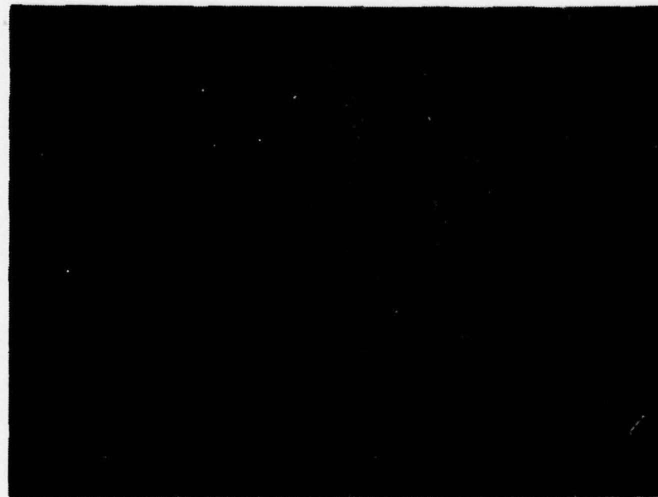


Fig. 3.3b Surface of the epitaxial layer of $Ga_{.45}Al_{.55}Sb$ grown at 2°C supersaturation.

The above functional relationship is shown in Fig. 3.4 for various values of α. The curves indicated that high α values result in a smoother surface. This is in qualitative agreement with our previous observation(4) that GaAlSb grew better on the <111> plane. This relationship also gives insight into techniques to improve the as grown surface morphology. Higher values of α give better surface finish, thus an increase in the L/T_0 ratio should improve the surface. The L/T_0 ratio can be altered by varying the growth temperature. Future efforts will be directed toward this line of thought for the improvement of surface morphology.

Information about the kinetics of the layer growth were also obtained from the successful growths. Figures 3.5(a) and (b) show the typical structure of the epitaxial layers grown at 4^oC supersaturation and 2^oC supersaturation, respectively. The topmost layer was $Ga_{0.45}Al_{0.55}Sb$ and the second layer was the GaSb buffer layer. Both 3.5(a) and 3.5(b) were obtained by growing at cooling rate of $1/2^oC/min$ for 2 minutes. The substantial difference in the resultant layer thickness suggests that the growth rate is strongly dependent on the amount of initial supersaturation. Also, the use of lower initial supersaturation gives better control over the layer thickness.

3.2 GaAlSb Characterization

3.2.1 Schottky Barrier Height

The Schottky barrier height, ϕ_0, to n-type III-V semiconductors generally lies in the vicinity of $2/3\ E_g$. Based on this prediction, the value of ϕ_0 for $Ga_{.45}Al_{.55}Sb$ would be ~0.75 eV. Contacts with both Al

Fig. 3.4 Surface roughness theory of Jackson[4], showing free energy change $\Delta G_s/NkT_o$ resulting from addition of N_A molecules to N possible sites vs N_A/N.

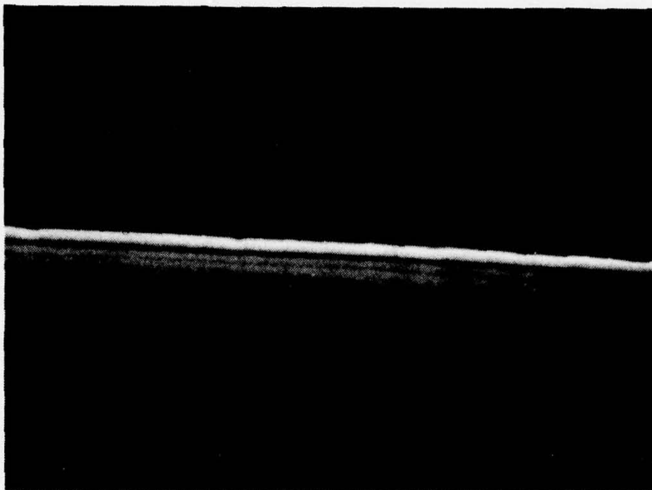


Fig. 3.5a Layer structure showing $Ga_{.45}Al_{.55}Sb$ (top layer) grown at 4°C supersaturation and the GaSb buffer layer.

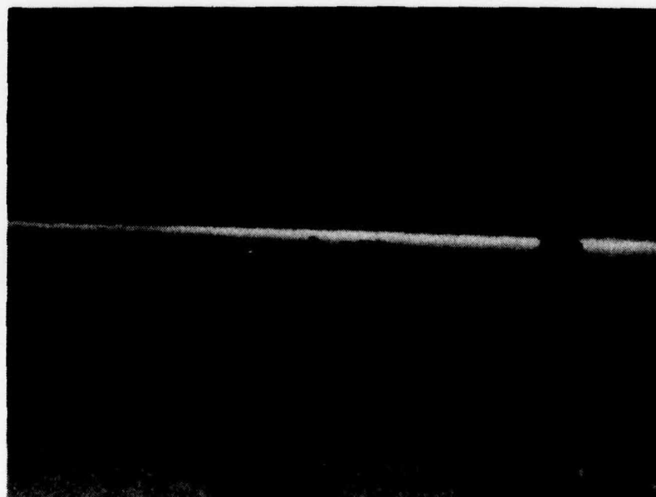


Fig. 3.5b Layer structure showing $Ga_{.45}Al_{.55}Sb$ (top layer) grown at 2°C supersaturation and the GaSb buffer layer.

and Au-Ge were made on the $Ga_{.45}Al_{.55}Sb$ layers to determine the height of the Schottky barrier. ϕ_0 values obtained by capacitance-voltage (C-V) measurements for the Au-Ge contacts gave a value of 0.7 eV which is in agreement with the prediction. However, Al barriers gave a ϕ_0 value of 2.2 eV. The data for the above two cases are shown in Figs. 3.6 and 3.7. The apparent discrepancy can be explained by the presence of Al_2O_3 at the metal semiconductor junction. The effects of such an oxide on the performance of the device have yet to be evaluated. However, the reverse I-V characteristics of the Al-GaAlSb barrier showed that it has a much lower leakage current than the AuGe contacts. This, in effect, could increase the signal to noise ratio giving a better CCD. This aspect of an interfacial barrier will be examined in the future.

3.2.2 Doping

Undoped GaAlSb layers grown at 500^oC were all p-type. The carrier concentration was approximately 10^{17} cm^{-3}. n^- -GaAlSb could be obtained by doping with appropriate amounts of Te. Since very small amounts of Te are needed, the Te is added in the form of Te doped GaSb with a doping level of 1.1×10^{18} cm^{-3}. The Te doped GaSb is added to the melts in amounts ranging from 200 to 2000μg. The carrier concentrations of the $Ga_{0.45}Al_{.55}Sb$ layers were then determined by C-V measurements. The carrier concentration profiles deduced from the data for three different doping levels are shown in Fig. 3.8.

In general, the results showed a uniform doping profile throughout the thickness of the layer. The resulting carrier concentrations ranged from

Fig. 3.6 C-V characteristics of AuGe Schottky barriers to $Ga_{.45}Al_{.55}Sb$.

Fig. 3.7 C-V characteristics of Al Schottky barriers to $Ga_{.45}Al_{.55}Sb$ for two samples of different doping density.

CALIBRATION POINT

10^{17} cm^{-3}

10^{16} cm^{-3}

10^{15} cm^{-3}

DOPING (CM^{-3}) ⟶

SAMPLE K05

SAMPLE K03

SAMPLE K08

0.1 0.2 0.3 0.4 0.5 0.6 1.0

DEPTH (MICRONS) ⟶

Fig. 3.8 Doping profile of three $Ga_{.45}Al_{.55}Sb$ layers grown by LPE.

10^{16} to 10^{17} cm^{-3}. A compilation of data from the present study and our previous study in Te-doping is shown in Fig. 3.9.

The curve is broken into two straight line regions. This suggests that there are two different incorporation mechanisms governing the doping of Te in GaAlSb. These two mechanisms can be understood if we examine why the undoped GaSb is always p-type. Reid et al[10] suggested that this was probably due to the substitution of Ga into Sb sites during the growth from a Ga rich melt. The initial process of Te doping could then be described as the competition between Ga atoms and Te atoms going onto an Sb site. However, the availability of this type of sites is limited ($\sim 10^{17}$ cm^{-3}). Therefore, this process would dominate at low Te concentration. On the other hand, when the concentration of Te is higher than the number of vacancies, Te atoms have to compete with the Sb atoms to go onto the Sb sites. These two processes dominate at different concentration ranges and thus give rise to the two different regions in the curve.

3.2.3 Photoresponse

The photoresponse of a p-GaSb-n/$Ga_{.45}Al_{.55}Sb$ junction is shown in Fig. 3.10. As expected, the photoresponse starts at 1.8μm where the GaAlSb is transparent, and the photons begin to have sufficient energy to excite electrons in the GaSb. As the energy of the photons is increased (i.e., decreased in wavelength), the photoresponse is relatively uniform until 0.8μm, where the photons begin to be absorbed in the $Ga_{.45}Al_{.55}Sb$ layer. At this point, most of the photons are absorbed at the surface of the n^- -GaAlSb layer and the carriers recombine at the surface, resulting in a cutoff

Fig. 3.9 Carrier concentration in the layer vs. atom fraction Te in the melt for $Al_{.55}Ga_{.45}Sb$ grown at 500°C.

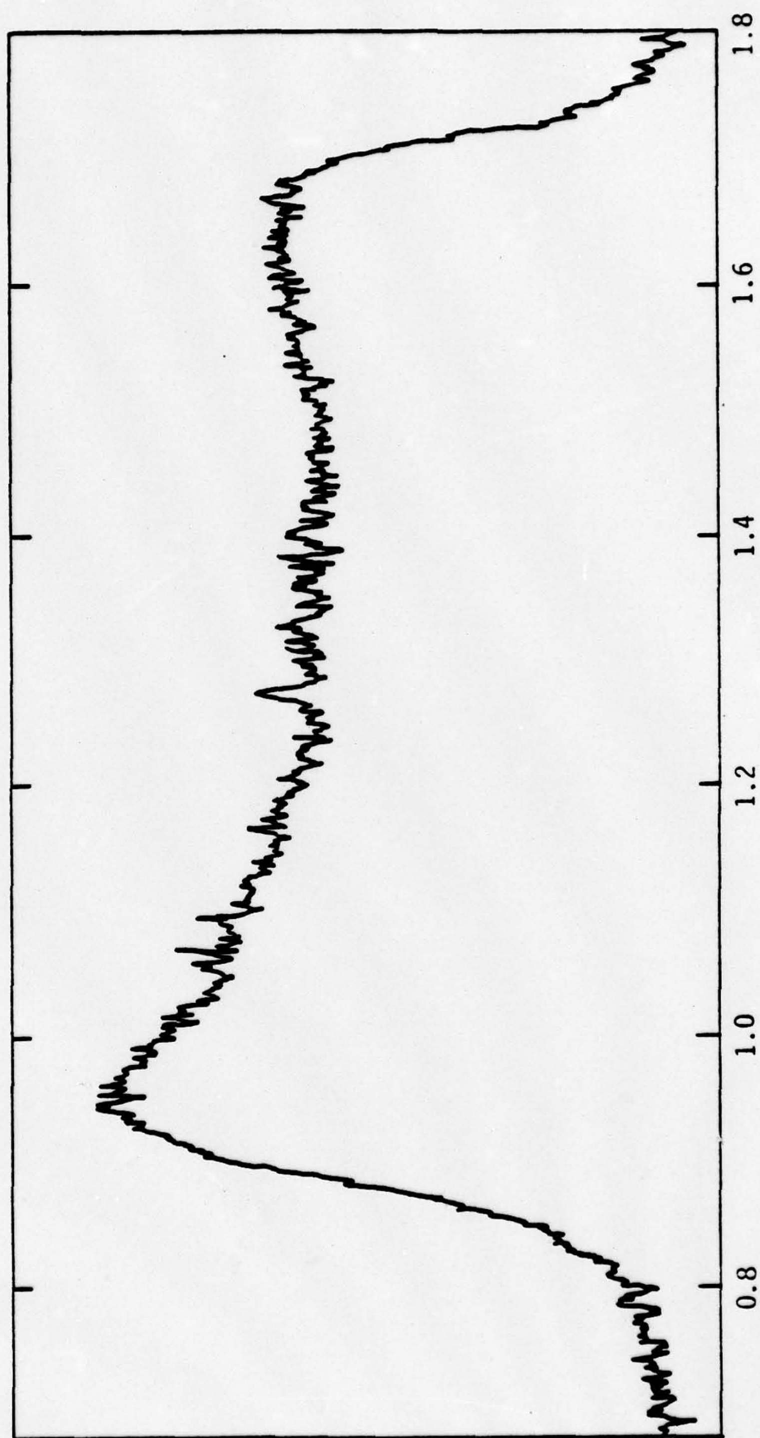


Fig. 3.10 Photoresponse of the n-$Ga_{.45}Al_{.55}Sb$-p-GaSb junction.

in the photoresponse wavelengths less than 0.8μm. This is precisely the type of photoresponse required for the heterojunction CCD and demonstrates that there are no heterojunction barriers or wide bandgap homojunction barriers created by etchback(4) which will limit device performance.

4.0 DEVICE FABRICATION AND TESTING

4.1 Device Processing

Most of the process development effort thus far has centered on developing a compatible technique for the definition of fine gaps (~1μm) between the CCD Schottky gates. The simplest processing technique which yields well defined edges is to apply photoresist on the prepared semiconductor surface, expose the gate mask, evaporate the gate metalization and remove the metal between the gates by dissolving the remaining photoresist. This is the so called "lifting" technique. One problem encountered in this process is that the metal being lifted tends to tear and leave ragged gate edges. The metal nominally used for the Schottky gates is Au. It has been found that by adding a small percentage of Ge to the Au before evaporation, a brittle metal alloy is formed which subsequently breaks cleanly in processing, thus leaving smooth edges on the gates. This Au-Ge Schottky exhibits low reverse leakage and this process seems to be well under control. We are now able to fabricate submicron gaps in complete CCD gate arrays repeatedly and reliably.

A second area being intensively pursued is the development of a two-level metalization technology. In a three-phase CCD, it is necessary to interconnect the third clocking phase since only two phases can be interconnected on the same level. Thus, an insulator is required to separate the two levels of metalization. It is desirable to use an insulator or combination of insulators which at once provide a pinhole free layer and provide passivation for the device. The difficulty is that this insulator

must be applied at relatively low temperatures to be compatible with processing steps which have preceeded it. This problem is not of fundamental importance to the device operation and, therefore, should not be allowed to form a bottleneck in the device development.

In order to speed up the development of this CCD, a new mask set has been designed and fabricated. With this mask set, only single-level metalization is required and a much faster feedback loop will be established in the process development cycle and CCDs ought to be much easier to fabricate. This mask set is now in use, and a device fabricated with is shown in Fig. 2.2.

4.2 Electronic Measurements

An important tool developed for the measurement of CCDs is a programmable CCD clock generator-driven system. Such a system has been developed via IR&D funding. The logic section in this system is programmable (by means of programmable read-only memories). This makes it easy to generate a new set of CCD transfer clock waveforms reasonably quick. It enables us to quickly modify the clock pulse sequences as required to test new device structures. Because the heterojunction and Schottky barrier CCDs are entirely new device types, it is important to have a versatile clock generator system which can be adjusted to optimize device performance.

Our clock generator is designed using high speed Schottky TTL and ECL logic and currently operates from DC to 20 MHz. The speed is limited by the access time of the PROMS. Figure 4.1 is a block diagram of the CCD clock generator system. The output consists of 16 parallel digital lines which feed

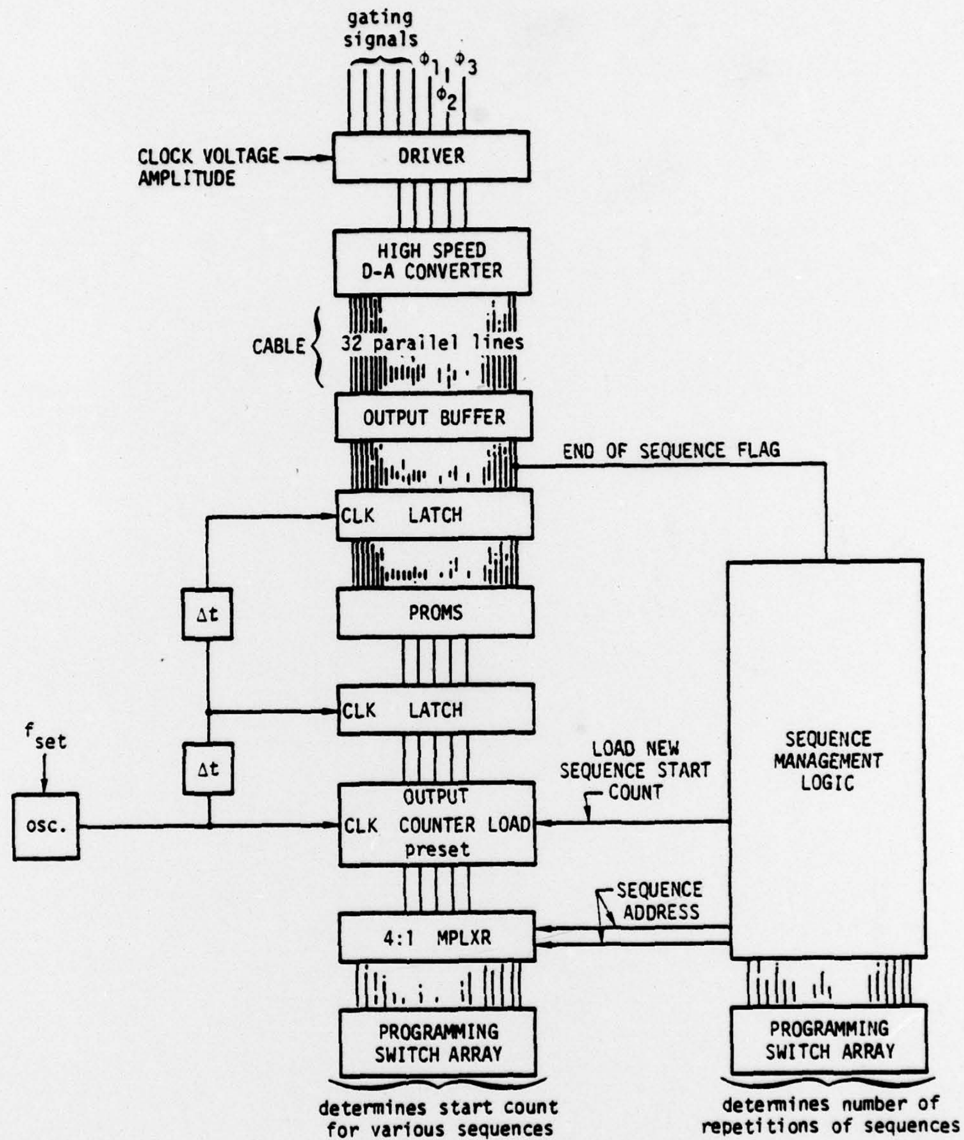


Fig. 4.1 Block diagram of programmable CCD clock generator.
(from Rockwell International Science Center IR&D Report 1978)

D/A converters connected through amplifiers to the CCD gates. Since 16 lines are available, some flexibility (at the expense of speed) is available in designing the shape of the clock waveforms.

A typical programming sequence to generate a desired waveform set would proceed as follows:

(1) Draw required clock phases, gating signals, etc., on paper

(2) Draw required digital inputs to the D to A converter needed to generate these signals

(3) Write down the binary or hexa-decimal code corresponding to the pattern at each time aperature

(4) Observe repetitions in the sequence and write a "1" in the end-of-sequence-flag slot for each repetition

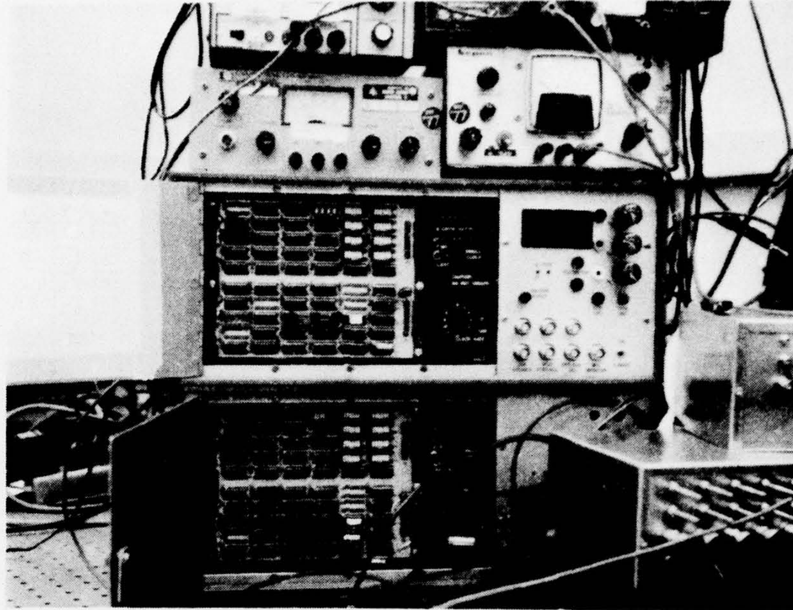
(5) Program switch array

(6) "Burn" PROM according to patterns in each sequence

(7) Insert PROM in system and single-step through code using indicator LEDs provided at outputs.

This software cycle can be completed in less than an hour by a practiced operator.

Since the master clock can be provided externally, several of these systems can be slaved to provide longer word lengths. Two such systems are at present being used to scan a two-dimensional CCD focal plane being developed at the Science Center. Figure 4.2 is a photo of this setup. So far, this system has proven quite versatile and is expected to be of continuing value in the CCD development program.



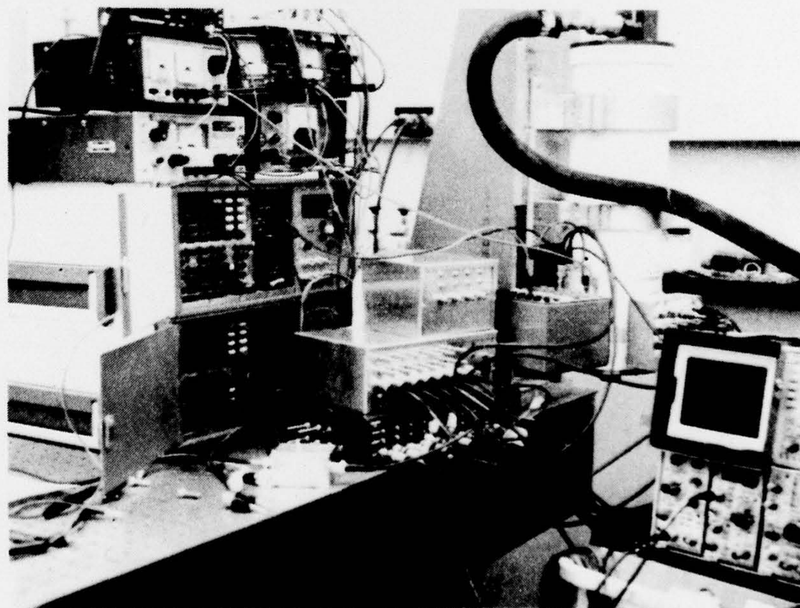


Fig. 4.2 Test set-up for the programmable CCD clock generator.

APPENDIX I

Schottky Barrier Gate GaAs CCD*

The Schottky barrier gate CCD concept has recently been demonstrated in this laboratory on GaAs. This device represents the first demonstration of charge transfer in a non-MIS (metal-insulator-semiconductor) CCD, as well as the first CCD in GaAs. The device is fabricated from a 2μm thick n-type ($N_D = 10^{16}$ cm^3) GaAs layer, grown by liquid phase epitaxy on a semi-insulating GaAs substrate. Figure A.1 is a photograph of the device and shows the array of closely spaced Schottky barrier gates delineated on a mesa (the large central rectangle extending along the length of the device). The gates are produced photolithographically and are separated by gaps of 1.4μm. Close examination on Fig. A.1 shows the extension of the gate "fingers" onto the substrate. This serves to block lateral flow of charge and the semi-insulating GaAs substrate thus forms a "natural" channel stop. The device is completed by ohmic contacts at the input and output ends.

Figure A.2 is a schematic of the experimental configuration used to verify charge transfer. In the initial experiment, the input and output ohmic contacts were biased to a large positive voltage (about + 20 V). the first and last gates were maintained at a dc voltage of about zero volts. The remaining gates were clocked with a three-phase clock operated between ±5 V. The output was connected to a transimpedance amplifier, so that changes in the output current could be detected. In order to inject signals into the device, the input ohmic contact potential is momentarily lowered to -5 V and returned. This input pulse is synchronized to occur when the first clocked

*This work is supported under IR&D

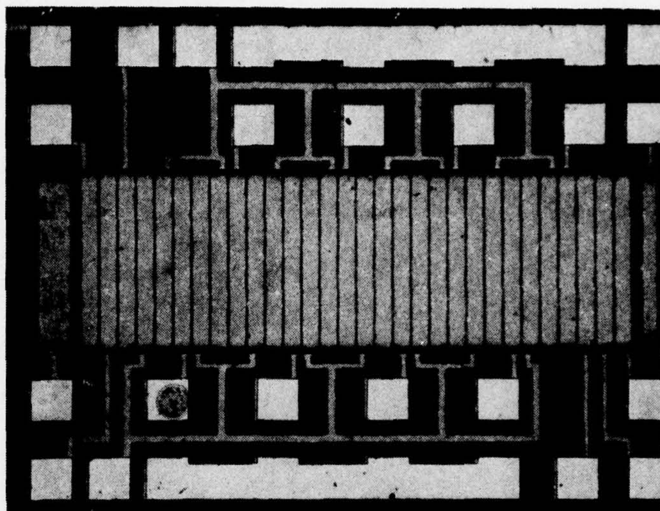


Fig. A.1 GaAs Schottky gate CCD.

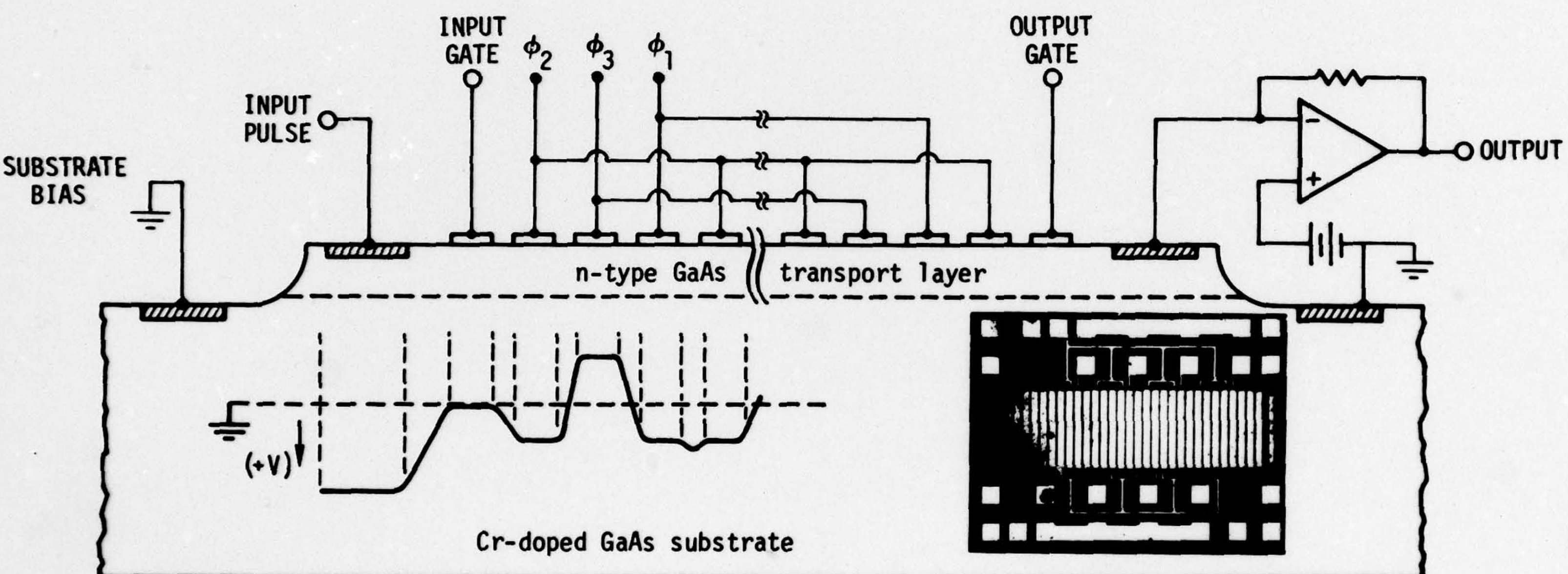


Fig. A.2 Schematic of scheme used to verify charge transfer in GaAs CCD (inset). The potential profile shown is at the instant before the input is pulsed.

gated ($\phi 2$ in this case) is positive and thus in a state ready to accept charge. The three-phase clock and the relative position of the input pulse are shown in Fig. A.3. Note that the input pulse occurs where $\phi 2$ is positive. Thus, every time $\phi 2$ is positive, there is an opportunity to inject a charge packet into the CCD. Once the charge packet is injected, it is confined to the region under one gate and is transferred along the device from gate to gate until it arrives at the final (zero volt biased) gate. When $\phi 2$ (the last clocked gate) makes a positive to negative transition, the charge packet is dumped into the output ohmic contact region and is detected as a current.

All connections to this device were made by means of a probe-card and the signal was detected in an external amplifier that was physically some distance from the device output node. Consequently, there was a large amount of feedthrough between the signal and drive lines which degrade the device performance. There was no attempt to optimize the clock slope or clock overlap. Initially, a single pulse was injected at the input and this produced a single output spike with the proper eight-stage delay. In this manner, multiple pulse bursts were injected with the proper number of output being observed in each case. Figure A.4 shows a burst of input pulses and the resulting delayed pulses at the output. A pulse code consisting of an arbitrarily selected combination of "1"s and "0"s was similarly tried. As a final qualitative experiment, a continuous input pulse stream was modulated with a sine wave of frequency much less than the clock frequency. The output sine wave was compared with the input and it was observed that as the input sine wave frequency was varied, there was always a fixed time delay between

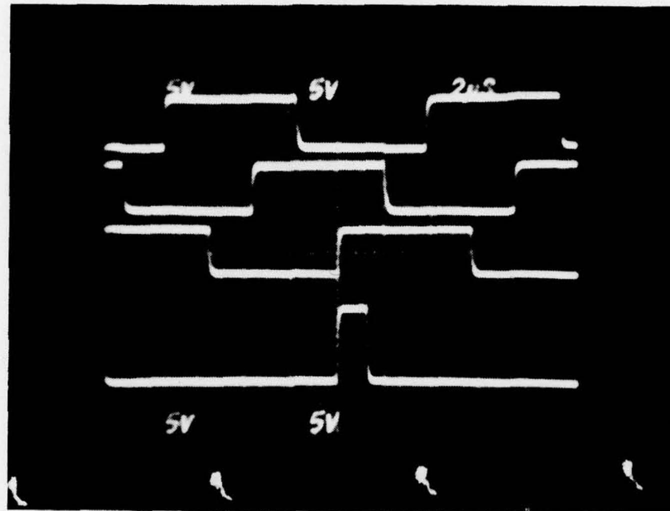


Fig. A.3 Three phase overlapping CCD clocks (top three waveforms) and input line (bottom).

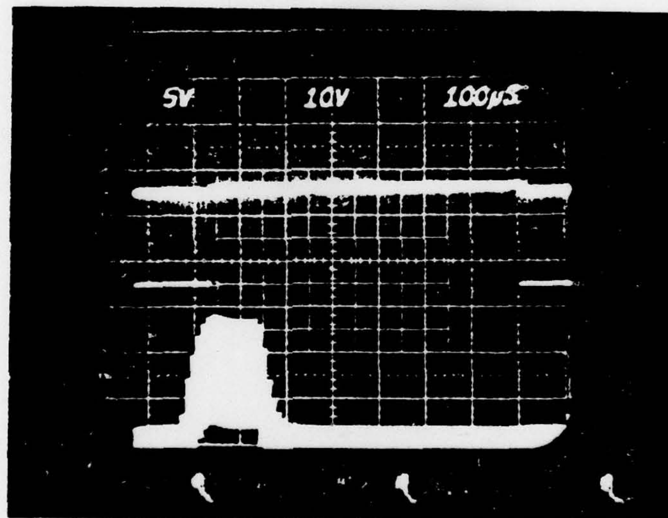


Fig. A.4 Photograph showing a burst of input pulses and the resulting delayed pulses at the output.

the input and output sine waves. A great deal of work remains to be done to fully evaluate this present device. As a first step, the devices must be mounted in a light tight header and hybrid integrated with a reset amplifier. In addition, the chip driver circuit must be improved to provide for controllable variation of clock pulse amplitude as well as rise and fall times. Finally, the input charge injection scheme must be modified to allow injection of a controlled amount of charge. These improvements in sensitivity must be made so that accurate charge transfer efficiency measurements can be made. Because of the long drive lines to the output amplifier clock drive feedthrough and noise degradation, it is impossible to make an accurate measure of charge transfer efficiency (CTE). It is, however, possible to establish a value of 0.97 as a lower limit CTE. Under similar experimental conditions, the first CTE estimate for a Si CCD was 0.94.

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