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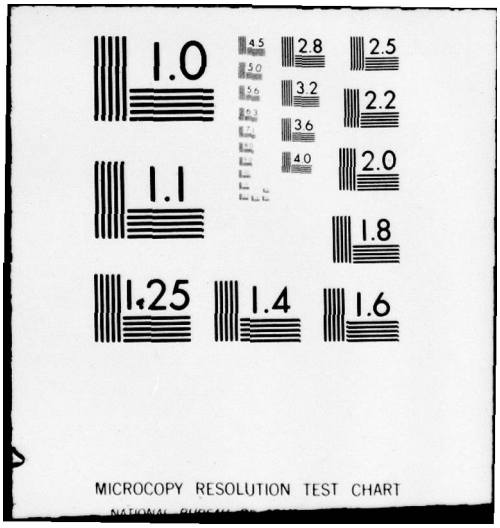
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DEVELOPMENT OF CHARGE TRANSFER DEVICES FOR 1-2 MICRON IMAGING

Final Report

By

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J. Appelbaum and J. S. Harris, Jr.

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By

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For

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

There is considerable interest in the development of an imaging system within the wavelength range of 1.0 - 1.8μm. The concept of charge coupled devices emerges as one of the viable candidates for such an application. The advantages of a non-MIS, Schottky barrier, buried channel CCD are discussed.

A suitable material system for the 1.0 - 1.8μm CCD application is the n-GaAlSb/p+-GaSb hetero-system. Substantially improved surface morphology for this system is reported. This is achieved by the addition of As to the AlGaSb

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layer, thus forming the quaternary: GaAlAsSb. Characterization of Schottky barriers to this material are reported. The Schottky barrier height is found to be >0.7eV.

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1.0 INTRODUCTION

There are a number of military applications for a passive (available illumination) night vision capability. Technological advances in image intensifiers and high performance photocathodes have resulted in night vision systems which operate in the visible and near infrared spectrum under low level moonlight and starlight illumination. These systems are, however completely ineffective under moonless or overcast conditions because of the low level of light in the 0.5-0.9 μm region under such conditions. Since there is considerable night glow ambient illumination in the 1.0-1.8 μm wavelength region which is nearly independent of cloud-cover, one solution to this problem is the development of an imaging system which operates in this wavelength region.

The development of a 1.0-1.8 μm imaging system has been the goal of a number of research efforts over the past 10 years. Most of these efforts have been directed at the development of a photocathode which would work in the 1.0-1.8 μm region. In spite of the large number of device concepts examined, none has yet emerged as a viable candidate to meet the requirements for a 1.8 μm imaging photocathode. A potential alternative to a photocathode for infrared imaging is the charge coupled device (CCD). While Si CCD's have recently come to the forefront for both visible and 3-5 μm imaging applications, there are no suitable deep level impurities in this material for operation in the 1-2 μm region. Furthermore, Si devices designed for 3-5 μm, require cooling to ~40K for satisfactory operation. Such cooling requirements would make Army night vision devices prohibitively expensive and would place unacceptable restrictions on virtually all of the 1-2 μm imaging systems envisioned for Army applications. CCD's developed in new materials with high optical absorption coefficients in the 1-2 μm region offer a viable solution to the systems requirements for a 1-2 μm imaging system.

The approach that we are pursuing in this program is the development of a non-MIS heterojunction CCD. This approach is chosen because of the present lack of a viable MIS technology for materials other than silicon and

recent developments at the Science Center on non-MIS devices. In spite of the extensive studies of III-V MIS devices, significant problems still remain to be solved in order to fabricate a useful III-V MIS CCD. While significant progress has been made in reducing the surface state density on some MIS structures, the mobile ion and insulator stability problems in low temperature deposited or anodic insulators have remained. These problems prevent the realization of a MIS CCD with stable and reproducible characteristics.

There are strong reasons to believe that a buried channel heterojunction CCD (HJCCD) may not only avoid the above problems associated with insulators in a MIS CCD, but that it may offer certain inherent advantages which render it more suitable for the 1-2 μm imaging application. Some of these advantages are:

(1) A built-in anti-blooming capability without the use of special channel stop regions.

(2) Superior radiation hardness to both particle (electrons, protons) and photon (x-rays, gamma rays) irradiation.

(3) Greater dynamic range because of low charge generation and absence of an insulator.

(4) High optical quantum efficiency achieved with intrinsic direct bandgap III-V materials.

(5) Lower dark current because the electric field is confined to a wide bandgap charge transport layer in a heterojunction device.

The key features of this device are summarized in Fig. 1.1.

Thus heterojunction CCDs promise a very exciting approach to 1-2 μm imaging. While several material systems are potential candidates for this application, the GaAlAsSb-GaSb system was selected for first development because it offers the potential to demonstrate a heterojunction CCD with a relatively simple Schottky barrier structure. In October 1978, the feasibility of this device design was experimentally verified, when the first heterojunction CCD was demonstrated as a part of the effort in this program. This

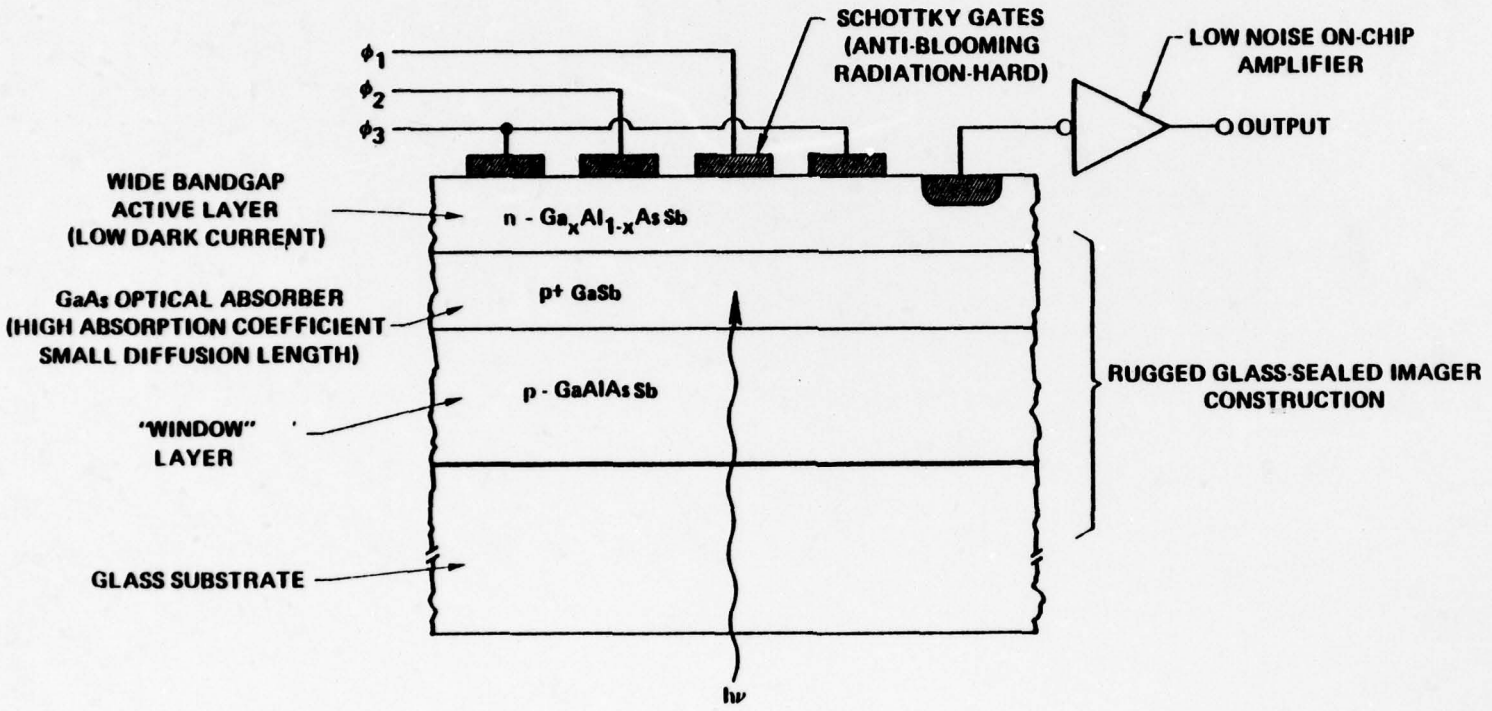

Fig. 1.1 Key features of heterojunction CCD imager design.

achievement was made possible because of drastically improved surface morphology and junction characteristics obtained in the n-GaAlAsSb/p-GaSb heterosystem.

Since the final imager design requires a glass-sealed structure (to be described in Section II), another significant development is the demonstration by Dr. John Pollard (NVL) that the GaAlAsSb material can be successfully fused to glass without strain-induced cracks.

2.0 TECHNICAL APPROACH

In this section the device design concept pursued toward the goal of an imaging CCD for the 1-2 μm region will be described. Also, results obtained in test structures designed to characterize and test various aspects of the device concept will be presented.

2.1 Schottky Barrier-Gate CCD

The Schottky barrier-gate CCD is quite similar to a conventional MIS (metal-insulator-semiconductor) buried channel CCD insofar as electrostatics are concerned. For similar substrate and channel doping and thickness, the potential profile under an electrode for a Schottky gate device differs in magnitude from an MIS device only by an amount which corresponds to the potential drop across the gate insulator in the latter structure.

The potential distribution under a gate can be calculated by the solution of the one dimensional Poisson's equation with the appropriate boundary conditions. This calculation is particularly simplified if an abrupt charge distribution (as indicated in Fig. 2.1) is assumed. A study of Fig. 2.1 is useful in understanding the electrostatics of the Schottky-gate buried channel CCD. Figure 2.1 shows the assumed charge density, ρ, the resulting electric field, E, and electron potential energy distribution, V, for a device with an ionized donor density, N_D, in the channel, ionized acceptor density, N_A, in the substrate, a stored charge in the channel, Q_S, and a channel layer thickness, T. The parameter of interest is the potential well depth, V_m as a function of gate bias voltage, V_g, and stored charge Q_S (= $-qN_D \Delta x$). The solution of Poisson's equation with the proper boundary conditions in this structure leads to an expression for the minimum electron potential, V_m:

$$V_m = \frac{qN_A}{2\varepsilon}\left(1 + \frac{N_A}{N_D}\right)(W - T)^2$$

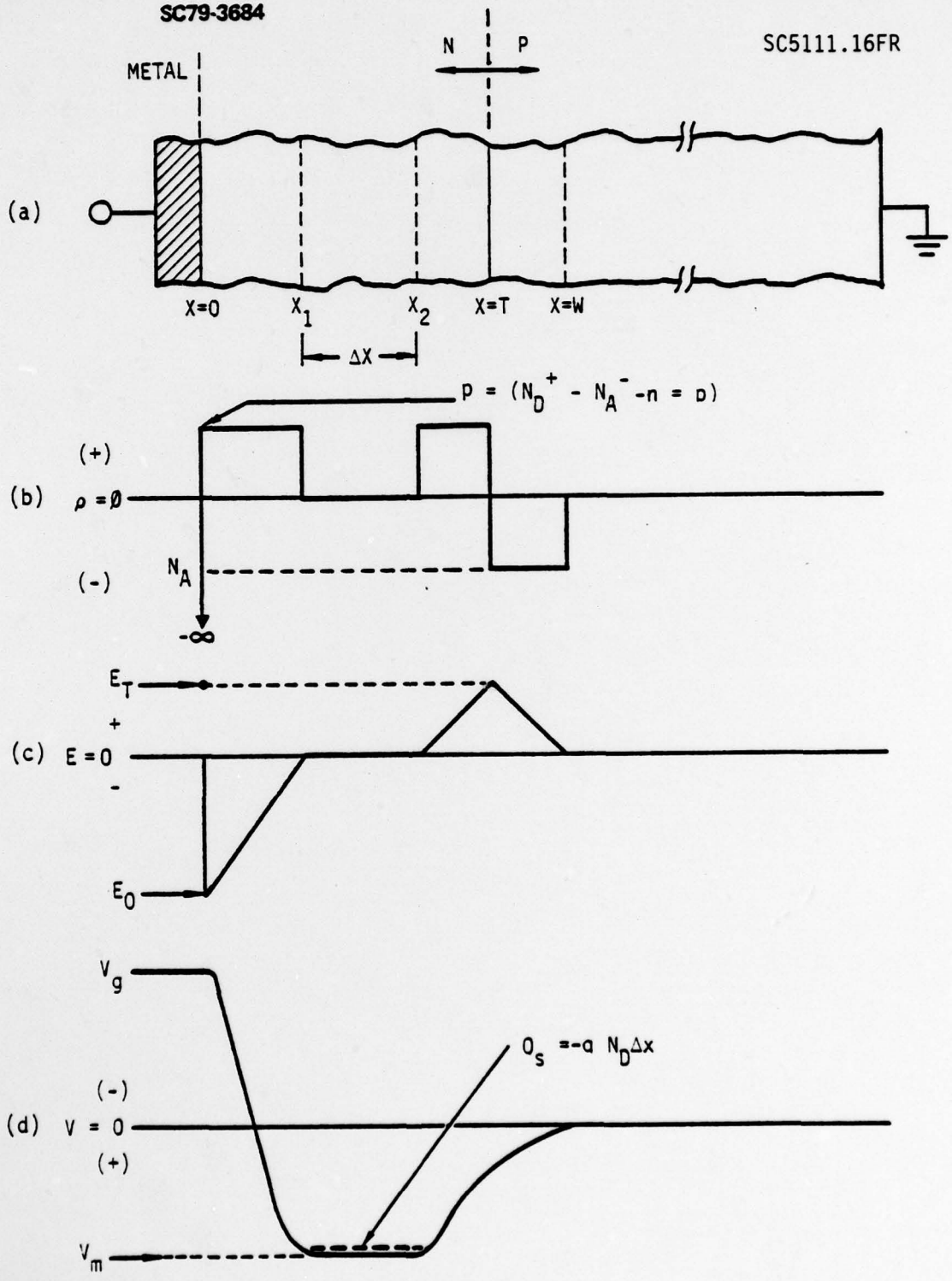

Fig. 2.1 Schottky barrier gate, buried channel CCD: (a) schematic cross-section under one gate, (b) assumed charge distribution, (c) electric field profile, (d) potential distribution.

where,

$$(W - T) = X_{DN}\left[\left(1 + \frac{N_D}{N_A} + \frac{2\varepsilon V_g}{qN_A X_{DN}}\right)^{1/2} - 1\right]$$

and,

$$X_{DN} = T - \frac{Q_S}{qN_D} \quad .$$

A reasonable set of parameters for the device are $N_D = 1 \times 10^{16}/cm^3$ and T = 2 μm for the channel, and $N_A = 1 \times 10^{17}/cm^3$ for the substrate. With these values fixed, we can compute the expected potential distribution under an individual gate for various values of stored charge and gate voltage. Figure 2.2 is the result of such a computation. The curves in Fig. 2.2 are for the ionized donor and acceptor densities and the layer thickness chosen above. These curves show that for a depleted channel with zero gate voltage, the potential minimum is V_m = +5.46 volts. With a stored charge of 1×10^{12} electrons/cm^2, the potential minimum is still V_m = 0.45 volts. Charge in excess of $1.25 \times 10^{12}/cm^2$ spills into the substrate, into adjacent wells, or into the gate depending on the potential minima in the adjacent wells. If the gate voltage is -5 volts, charge in excess of ~$5 \times 10^{11}/cm^2$ is injected into the substrate. If, on the other hand, the gate is biased beyond +5 volts, ($V_m - V_g$) continues to decrease until charge is finally injected into the gate. A plot of potential minimum V_m, as a function of gate voltage and stored charge is shown in Fig. 2.3. The dashed lines at the top and lower right side of the diagram are the points where the potential well depth is reduced to 0.4 volts. (A well depth of 0.4 eV is arbitrarily taken as the point where charge is injected over the barrier and into the gate or substrate.) These dashed lines define the operational boundaries of the device.

The information plotted in Fig. 2.3 demonstrates one of the unique features of the Schottky gate CCD; a natural anti-bloom feature for each cell without the necessity for special anti blooming channel stops. If the charge storage cell is operated with a 9 V gate bias, then the potential minimum V_m

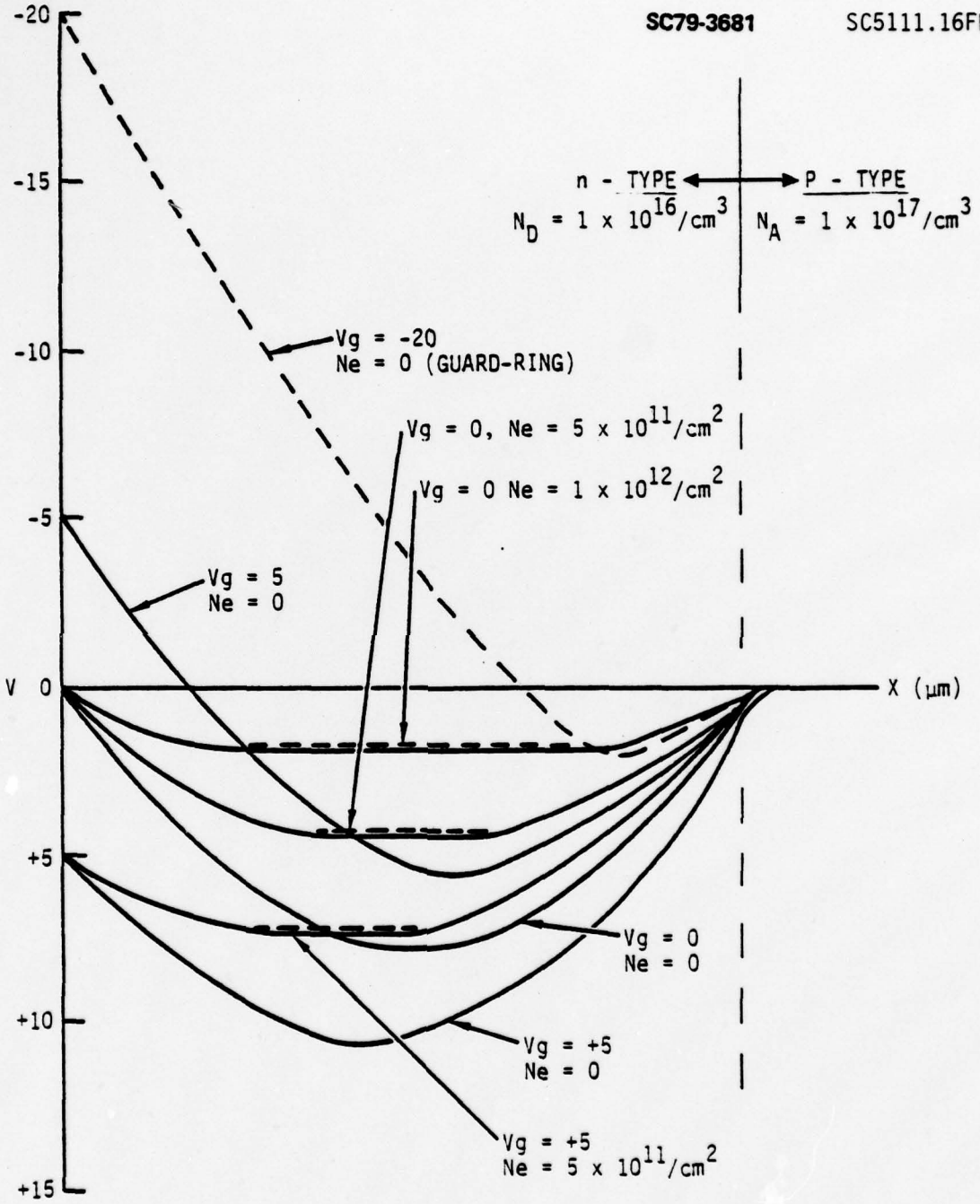

Fig. 2.2 Calculated electron potential energy vs. distance under a gate for various gate potentials and charge densities.

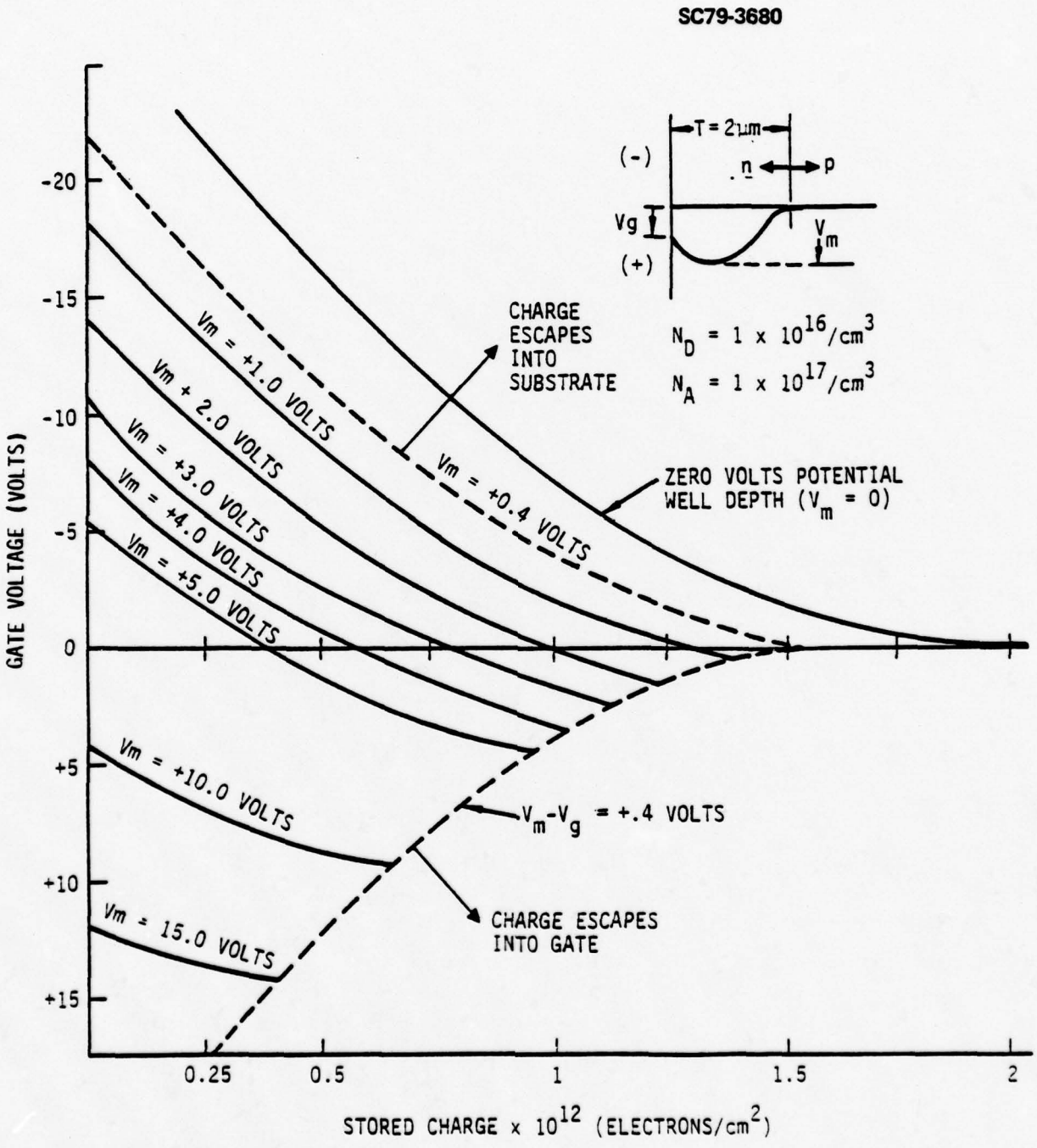

Fig. 2.3 Calculated values of potential minimum, V_m, as a function of gate voltage and stored charge density. The dashed lines represent the boundaries where charge will be injected into either the gate or substance.

is ~ +13 V with no charge. Moving horizontally to the right from V_g = +9 V to the intersection of the dotted line shows that V_m = +10 V with .7 x 10^{12} electrons/cm^2 and any number greater than this will be injected into the gate as long as the potential minima of all next nearest cells is V_m < +9 V. Figure 2.3 shows that as long as V_g < +4 V, this condition is satisfied, thus the gating cells on either side of the charge storage cell can be grounded (V_g = 0V) and still maintain charge localization under the desired cell. This anti-bloom feature is an important advantage of this CCD because Si buried channel CCD's cannot be protected against blooming and Si surface channel CCD's require special channel stop regions which increase processing complexity and reduce image resolution.

The above one-dimensional calculation is valid for a region under an electrode far away from the edges of the gate. A region of primary interest for device design is the region between the gates because this governs charge transfer speed and efficiency. In the gap region, the surface potential is no longer pinned by the metal gate and the potential in the semiconductor can be much more positive than under the gates. This means that there will be a tendency for electrons to be trapped in the regions between the gates if this gate spacing is too large. In order to design a device for high transfer efficiency, it is vital to be able to calculate the magnitude of this potential between the gates as a function of gate spacing.

A rigorous calculation on an analytical basis for the two-dimensional potential distribution problem for the region of the gap between electrodes in the Schottky gate CCD structure would be very difficult. Fortunately, the effect of the gap is a relatively small perturbation on the one-dimensional problem and it is possible to treat this two-dimensional problem to a high degree of accuracy by a perturbation approach. This basic approach is illustrated in Fig. 2.4. Figure 2.4(a) shows the one-dimensional problem consisting of a metal electrode, a depleted n-type layer with a positive charge density, N_D^+ and a depleted p-type region with a negative charge density N_A^-. The far side of the depletion region is bounded by undepleted p-type material

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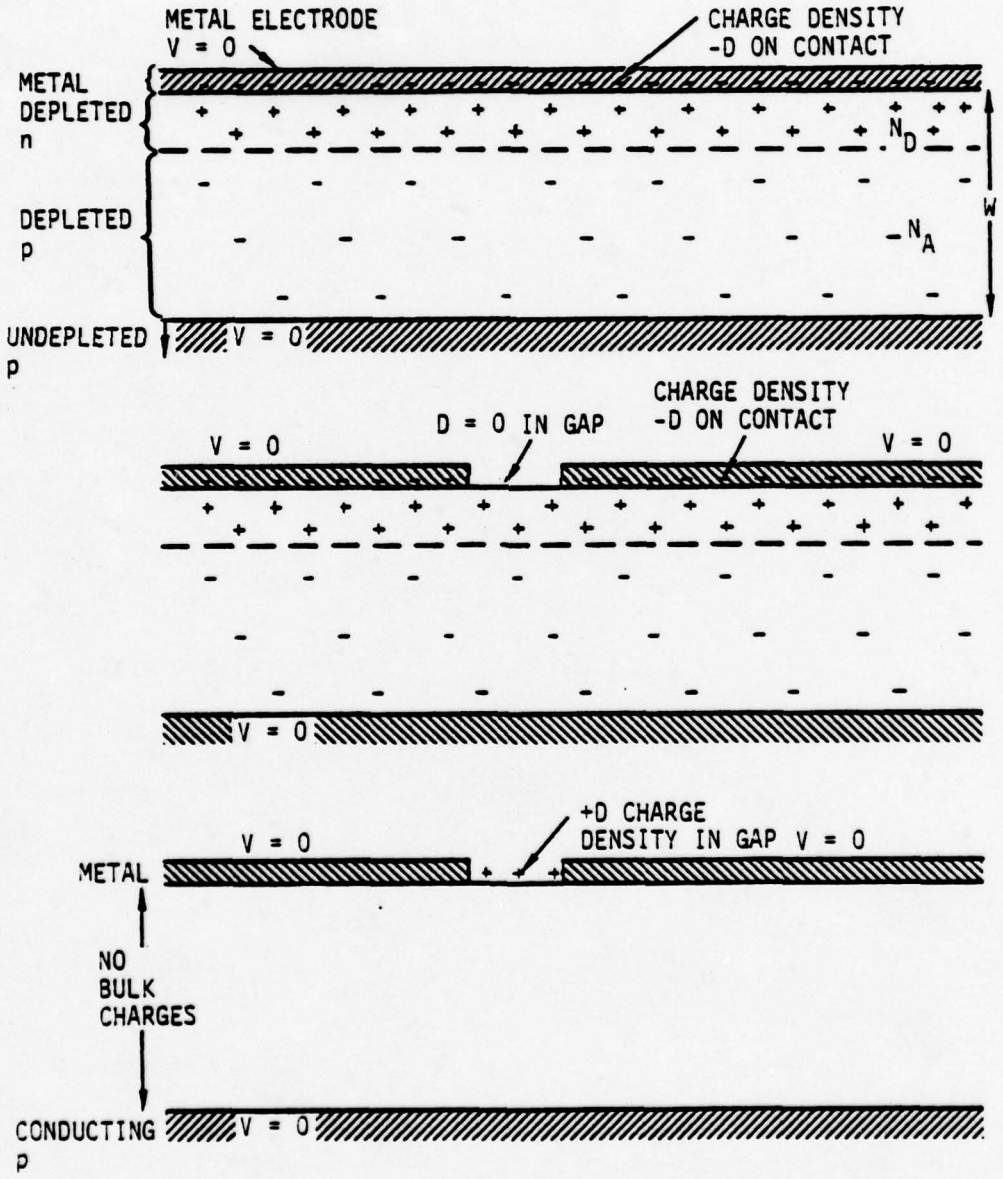

Fig. 2.4 Model for the perturbation calculation of the potential between gates. (a) The one-dimensional problem with zero gate spacing (i.e., a continuous gate). (b) The desired structure with two gates at the same or different potentials and zero charge density at the surface between gates. (c) The difference between (a) and (c) which removes all bulk charges and only leaves the two gates with a positive charge density at the surface between the gates.

which is treated as a conductor. An analytical solution for this one-dimensional problem has been shown in Figs. 2.2 and 2.3.

The problem of the electrode gap on the Schottky gate CCD structure is shown in Fig. 2.4(b). It consists of the electrode structure, a depleted n-type layer with positive charge density N_D^+ and a depleted p-type region with negative charge density N_A^-. The difference between Figs. 2.4(a) and (b) is that in the electrode gap, there is an absence of negative charge from the metal electrode. It is simply the influence of this missing charge density, D, in the gap which represents the perturbation of the gap. This perturbation is illustrated in Fig. 2.4(c) [i.e. the difference between parts (a) and (b)]. Thus, if we solve the perturbation problem of Fig. 2.4(c), we can superimpose this solution on the one-dimensional problem already solved and obtain a solution to the desired configuration in Fig. 2.4(b).

While in principle it would be possible to solve the problem in Fig. 2.4(c) analytically, it was decided that solution by electrical analog would be far easier. In the analog solution of this problem, a piece of carbon resistive paper with silver paint applied in the positions corresponding to the two electrodes and the conducting undepleted substrate was used. The dimensions of the analog were scaled up by a factor of 10^4. The driving function for the potential distribution problem in Fig. 2.4(c) is not a voltage applied to the electrodes, but rather a charge density D in the gap. The constant positive charge density implies a constant electric field at the semiconductor surface. A constant current density is thus required to produce a constant electric field at the surface in the analog problem. The potential distribution with this constant current density impressed on the gap and all of the electrodes at ground potential as indicated in Fig. 2.4(c) was measured on the carbon paper analog. The voltage distribution on the conductive paper analog is scaled to the actual semiconductor potential in the Schottky gate CCD device by scaling the surface electric field in the semiconductor to the analog electric field at the surface. Figure 2.5 shows the resultant sum of the one-dimensional potential distribution of Fig. 2.4(a) plus the perturba-

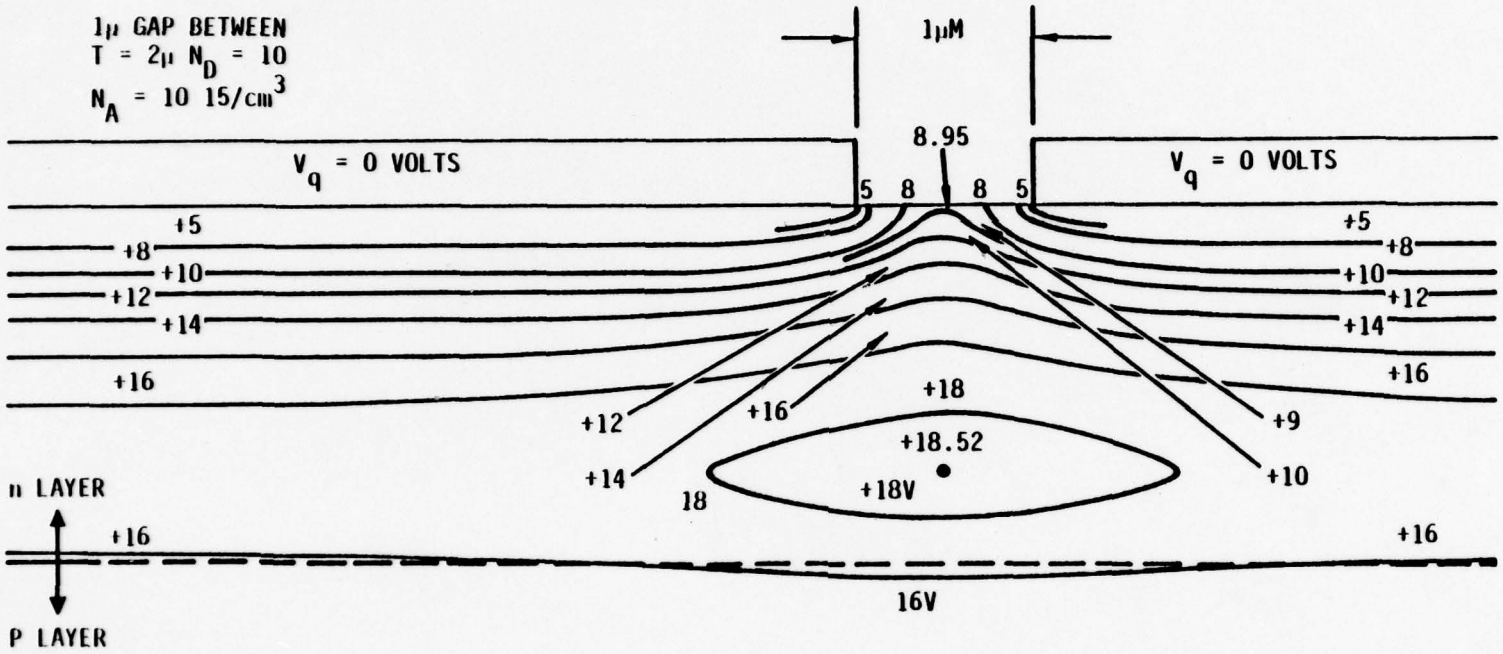

Fig. 2.5 Potential contours obtained from the carbon resistive paper analog solution of the perturbation problem. For a 1μm electrode gap, the potential minimum between gates is 18.52V compared to 17.2V under the gates.

tion potential of Fig. 2.4(c) derived from the analog solution for a 1 μm electrode gap. This computation was performed for a substrate doping of N_A = 1 x $10^{15}/cm^3$, but the results are qualitatively similar when N_A = 1 x $10^{17}/cm^3$. In the two-dimensional solution, the potential minimum between the electrodes is 18.5 V for a 1 μm gap. When the gap is increased to 2 μm, the potential between the electrodes increases to 22.5 V. The potential minimum as well as the surface potential between gates is strongly dependent upon the gate spacing as illustrated in Fig. 2.6. We see that the spatial location of the potential minimum also moves markedly towards the surface with increasing spacing. A gap of 2 μm or greater provides a sufficiently low potential so that it would be difficult to reliably extract charge from one gate to the next, thus leading to transfer inefficiency. For a 1 μm gap or smaller, the effect of this potential is minimal. Thus, mask design and fabrication techniques must be built around a 1 μm gate spacing.

Another topic of primary importance in the Schottky gate CCD design is the channel stop, or charge confinement in the plane of the CCD. In a conventional buried channel silicon CCD the channel stop region is a heavily doped p-region. Thus the signal charge packets are isolated by a p-type region on the bottom and sides and are isolated from each other by gate potentials. In the Schottky CCD, the channel stop is merely a gate (guard-ring) which totally surrounds the device on the sides and is DC biased to fully deplete the n-layer under it. Thus, the isolation of the channel from the rest of the chip is electrically equivalent to the isolation of the charge packets from each other along the channel. In order to guard against diffusion of carriers from the material outside of the guard ring, the region outside of the device active area is pinned to a voltage more positive than the guard-ring voltage by means of an ohmic contact. The separation of the charge packets from one another both in the direction of charge transfer, as well as the direction perpendicular to charge transfer are shown in Fig. 2.7.

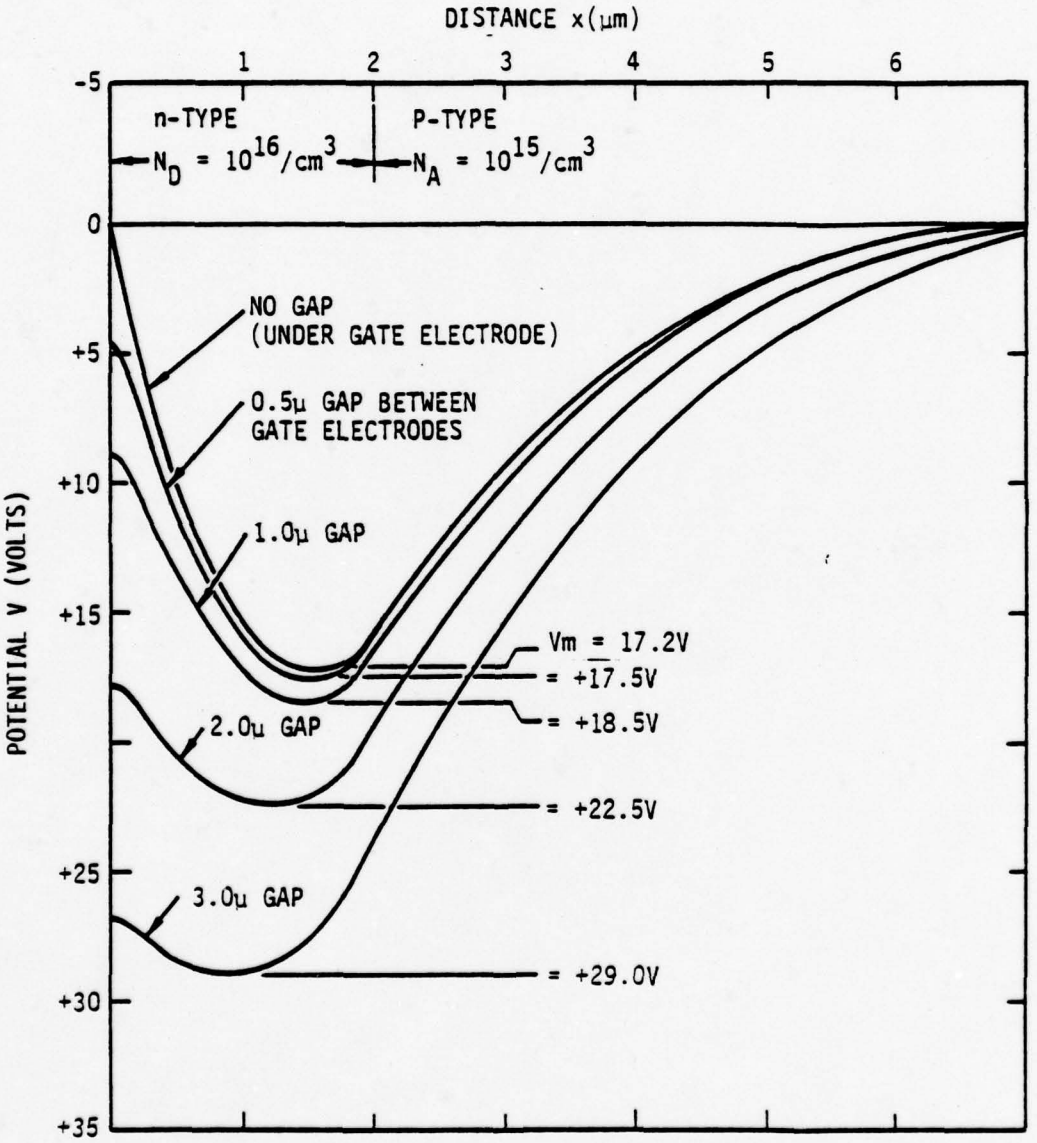

Fig. 2.6 Electron potential energy at the center of the electrode gap vs. distance with zero gate voltage and gate spacing as a parameter.

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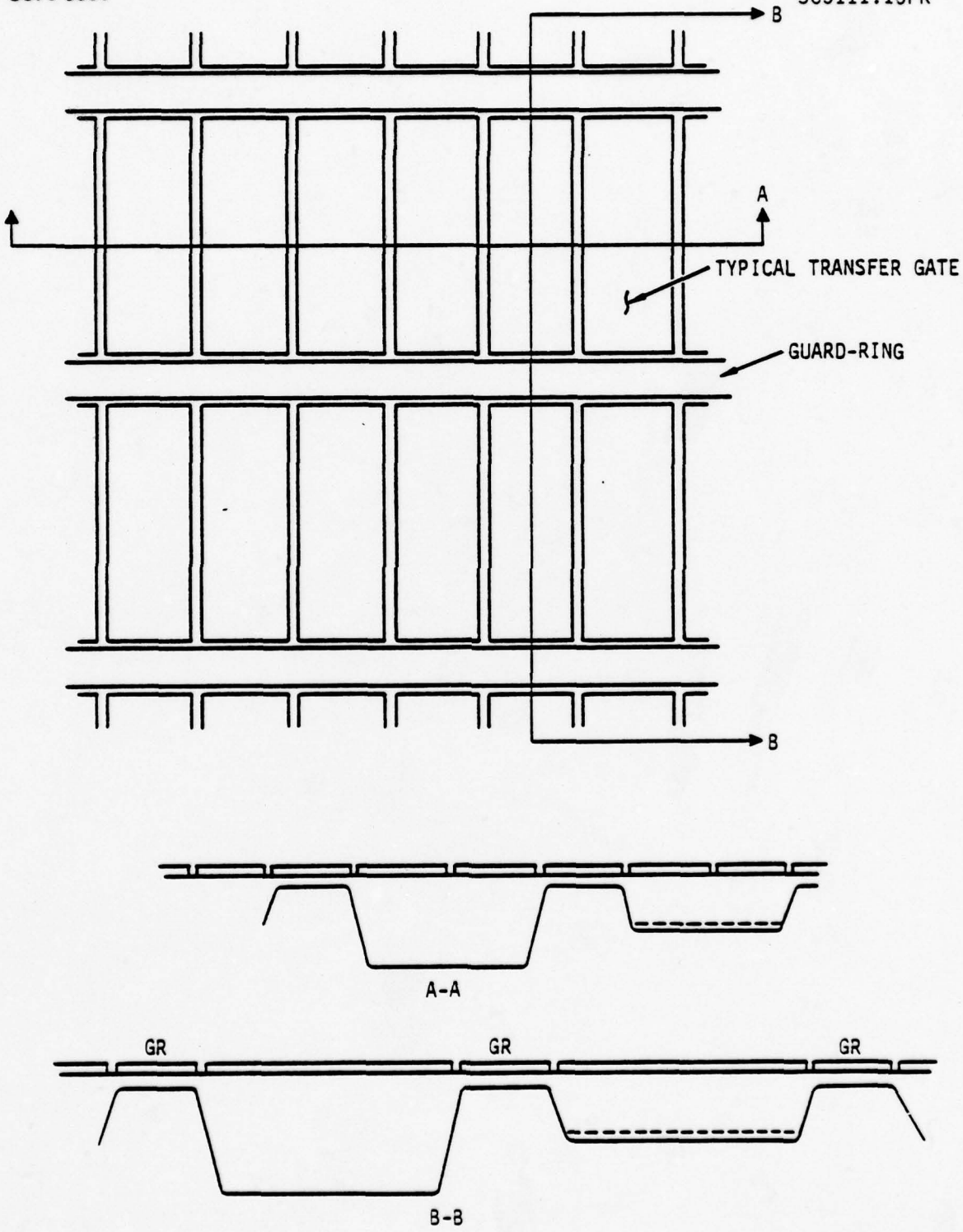

Fig. 2.7 Guard-ring channel stop in area array CCD.

2.2 Extension of Schottky Gate CCD Concept to an Area Imager

In addition to formation of potential wells and transfer of charge, a two-dimensional CCD imager must provide for efficient absorption of light, as well as multiplexing of the photogenerated signal from all the pixels onto a single video line. In Section 1, the backside-illuminated, heterojunction CCD concept for this application was described. This approach makes for high quantum efficiency and low dark current. One possible approach for the chip organization which makes possible the serialization of the pixel information is illustrated in Fig. 2.8.

In Fig. 2.8 the charge integration/transfer gates are arranged in rows, separated by the strips of the guard-ring. The area consumed by the guard-ring does not represent optical dead-space, since the photo-electrons generated in this region fall into potential wells in one or the other of the rows. The transfer gates are interconnected through a second level of metallization. A four phase transfer clock configuration is shown, although a three phase configuration is also possible. The charge integration/transfer gates in each row are separated from the multiplexer by a parallel-serial transfer gate. These gates (one per row) are connected together by second-level metalization. The guard-ring electrode "wraps around" the gates so that cross-talk between rows can be minimized. The multiplexer gates are electrically equivalent to the integration/transfer gates but are, of course, driven by their own clocks so that the parallel and serial transfers are synchronized. Ohmic contacts at the extreme ends of the multiplexer can be used for charge injection and for detection. The on-chip amplifier, which resides at one end of the multiplexer is not shown, but can be either a destructive readout (pre-charge amplifier) or a floating-gate device. The multiplexer array can be as long as needed to provide the required delay for formating purposes. Also, multiplexers can be provided at opposite ends of the imager to extend signal processing flexibility on the chip. An ohmic contact stripe completely surrounds the chip and is biased to provide an electron sink to reduce diffusion of electrons from the material outside of the active area.

Fig. 2.8 Imager chip organization. The imager array charge transfer is controlled by ϕ_1 to ϕ_4. The parallel/serial transfer gate controls transfer of charge between the imager and multiplexer sections. While ϕ_1 to ϕ_4 control the multiplexer charge transfer.

2.3 Device Processing and Fine-Line Lithography

Once the wafer has been sealed onto glass and the original substrate etched away, the device fabrication process consists of a relatively simple sequence. This process is illustrated in Fig. 2.9. The first mask step defines the ohmic contact regions discussed in connection with Fig. 2.8. The ohmic contact metalization is evaporated and subsequently alloyed with the semiconductor at a suitable temperature. At this point, the quality of the ohmic contacts is gauged by probing special patterns provided for this purpose. The second mask defines all the Schottky-barrier gates and guard-ring. Virtually all the close alignment tolerances such as the gaps between the gates are defined in this mask. This is particularly convenient, since the need for time consuming sub-micron alignments is eliminated. Currently the dimensional tolerance available in high resolution masks at the Rockwell Mask Facility (in Anaheim, California) is ± 0.1 μm. Figure 2.10 is a scanning electron micrograph of a photo-resist pattern defined on GaAs. The smaller features in this photo are of the order of 1 μm. Note that the photoresist has near vertical walls and is itself about 1 μm thick. Resolution of this quality is achieved daily in the CCD and integrated circuits programs at the Science Center. After the Schottky pattern has been defined, a plasma silicon nitride is deposited over the entire wafer. Holes or vias are opened in this insulator for the interconnection of the gates. The final metalization step, which interconnects the Schottky gates, is deposited and the device is ready for test.

One very important consideration in this process is the integrity of the insulator, i.e., the density of pin-holes must be sufficiently low to allow thousands of crossovers without a single short between the first and second levels of metalization. To verify the low pin-hole density and also to examine the reliability of the first to second level interconnects, a special process monitor mask set is routinely used (on a "dummy" wafer) with each wafer batch. This process monitor includes a test for shorts between 500 crossovers of 1st and 2nd level metalization, as well as a test for opens in

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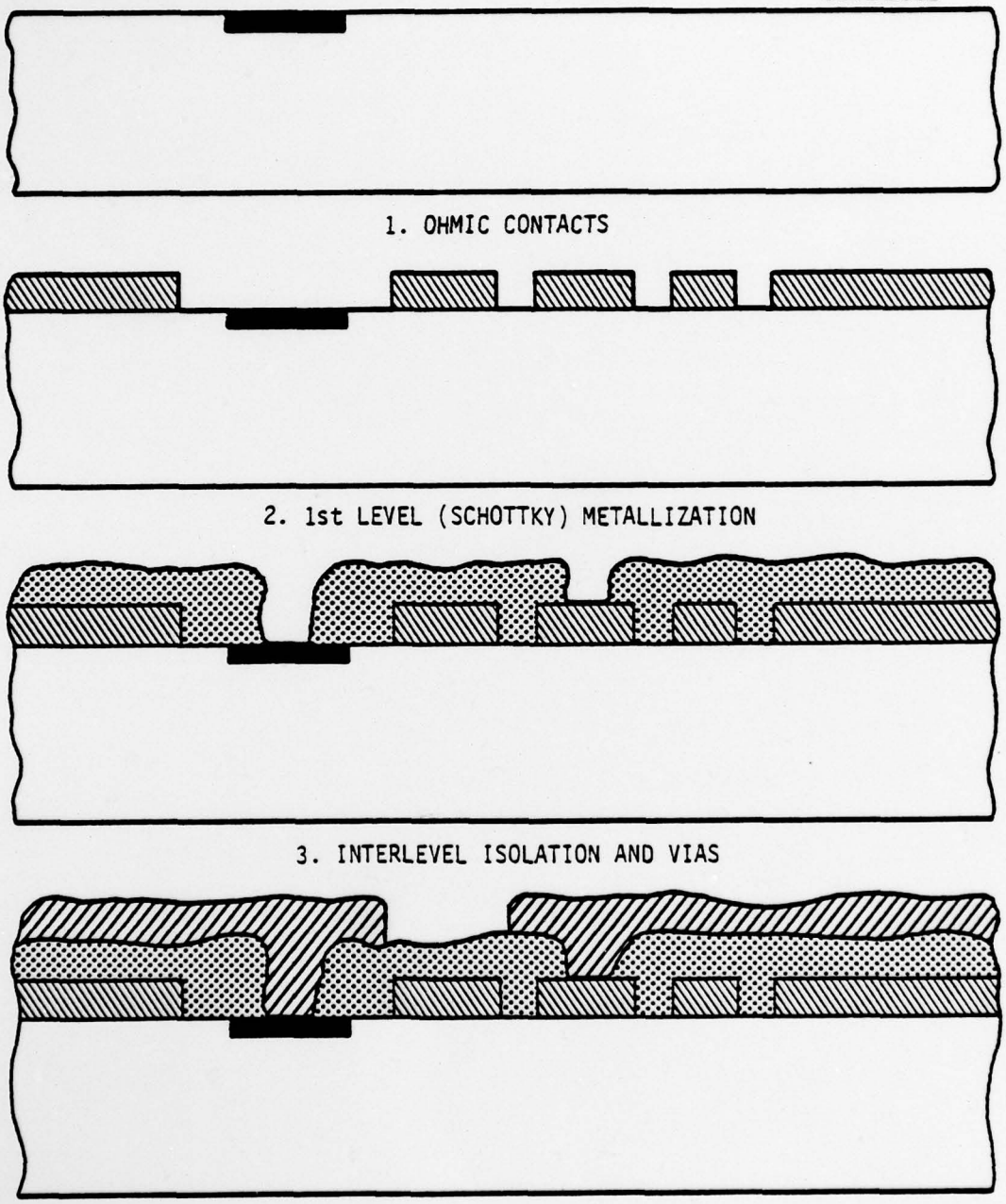

Fig. 2.9 Four masking step CCD fabrication sequence.

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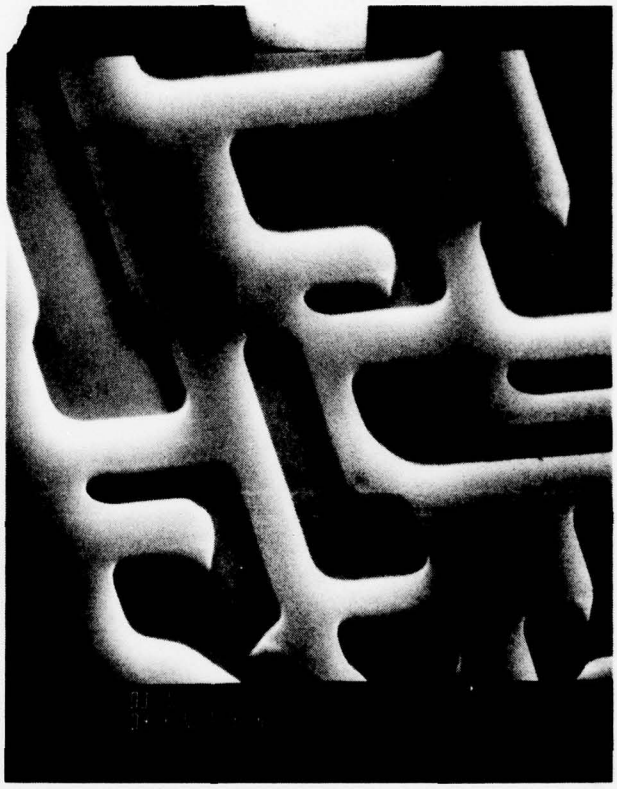

Fig. 2.10 Photoresist pattern showing typical micron-geometry resolution.

500 serially connected transfers between 1st and 2nd metals. Very high reliability has been observed using this test on the interlevel insulator.

2.4 Measurements and Characterization

A rather generalized approach has been taken at the Science Center in the design of the multi-channel waveform generators which provide all the clocks and sample/reset pulses required to drive a two-dimensional CCD array. A programmable waveform generator is the heart of the system. This instrument has 16 parallel channels which are updated from a random-access memory at a 20 MHz rate. Thus the output is updated every 50 nsec and the output of two channels can be delayed by a minimum of 50 nsec. The memory is written into by an on-line Data-General Eclipse computer under software control from a dedicated terminal. To change any of the waveforms, the necessary code is typed into the terminal. Permanent storage of the clock waveforms is on magnetic tape. The outputs of the waveform generator feed a set of amplifiers which can provide drive waveforms with $\leq \pm 25$ volt amplitude. The output waveforms as well as the rise and fall times are independently set by the computer. Thus, once a given set of test conditions have been decided upon, the information required to precisely reproduce them is available in digital form in the computer and can be recalled at will. A high speed A/D converter is also available so that CCD output waveforms can be digitized and stored in the computer for subsequent mathematical manipulation or comparison. Software routines have been written to continually vary a given test condition while simultaneously measuring CTE to optimize the latter. In this way, a printout of an optimized set of operating conditions can be produced for a given device.

2.5 Performance Evaluation

2.5.1 Well Capacity

Figures 2.2 and 2.3 can be used to determine the theoretically predicted charge in the well under a set of operating conditions and to determine

the well capacity. The measurement of this parameter is relatively straightforward if the CCD output ohmic contact is biased through a resistor, R. The signal charge, $\Delta Q = qN_e$ (N_e = number of signal electrons), causes a voltage change at the output which is directly measurable. Since this is an RC network, however, the amplitude of this output pulse cannot be directly interpreted in terms of number of electrons unless all the contributions to the node capacitance are accurately known. Since all the signal electrons must flow through the resistor, R, however, N_e can be determined by measuring the average current through R. This can be done with an accurate floating electrometer. Once i_{ave} is known, the value for N_e is a straightforward calculation:

$$i_{ave} = \frac{\Delta Q}{\Delta t} = \Delta Q f_{cl.} = qN_e f_{cl}$$

and

$$N_e = \frac{i_{ave}}{q f_{cl.}}$$

Alternatively, if the area under the output pulse can be determined, N_e can be evaluated as follows:

$$Q = qN_e = \frac{1}{R} \int V(t)\, dt$$

$$N_e = \frac{1}{qR} \int_0^\infty V(t)\, dt \quad .$$

Once ΔQ is known, then for a given set-up, the relationship $\Delta Q = C\Delta V$ can be used to determine the total node capacitance and subsequently ΔQ can be inferred directly by measuring ΔV. The required integral of V(t) can, of course, be evaluated by computer once V(t) is digitized as described earlier.

2.5.2 Transfer Efficiency

The transfer efficiency is readily evaluated using the method of Broderson et al.,[1] by measuring the normalized sum of deficits in either the leading edge or trailing edge of a sufficiently long pulse burst. This is permissible since conservation of charge requires that the total deficit in the leading and trailing edges be equivalent. Thus, using Broderson's notation, in the case of a destructive readout:

$$\varepsilon = \frac{L}{N - 1 + L} \quad ,$$

where N is the number of transfers and

$$L = \frac{1}{\Delta_T} \sum_i \Delta_i$$

where Δ_T is the difference between the saturated signal pulse amplitude and the background, and Δ_i is the relative loss of the i^{th} pulse. The effect of traps on the transfer efficiency can be evaluated by a double burst experiment in which the delay between bursts is varied to "sweep" through the effective time constants of the traps. These measurements can then be correlated to independent measurements of trap densities.

2.5.3 Dark Current

Dark current generation can occur at a number of regions within the Schottky barrier CCD. These include:

1. Thermal electron generation in the absorber within an electron diffusion length of the absorber-channel junction, (diffusion current).
2. Generation through traps or defects in the depletion region of the absorber, (g-r current).

3. Generation through traps of defects in the completely depleted channel layer (g-r current).
4. Schottky barrier leakage current.

The temperature dependent contribution from each of items 1, 2, 3, and 4 can be calculated. The thermal generation current for the absorber is just the reverse bias diffusion current for an ideal one-sided abrupt p^+-n junction diode.[2]

$$J_d^A = \frac{q D_n N_D}{L_n} = \frac{q D_n n_i^2}{L_n N_A} \tag{2.4}$$

where q is the electron charge, D_n is the electron diffusion coefficient, n_i is the intrinsic carrier concentration (dependent on temperature), N_A is the acceptor density and L_n is the electron diffusion length. For GaSb, the appropriate values are: D_n = 100 cm^2/sec, $N_A = 5 \times 10^{17}/cm^{-3}$, L_n = 3 μm, and $n_i = 2.8 \times 10^{12}$ at 300°K.

The generation current through traps in the depleted regions of the absorber and hole barrier layers is just the generation-recombination (g-r) current for the depletion region in a p-n junction. At first glance, one might think calculation of this term to be very straightforward, following the work of Sah, Noyce and Shockley:[3]

$$J_{g\text{-}r}^c = \frac{q n_i W}{2 \tau_n} \tag{2.5}$$

where W is the depletion width and τ_n is the electron lifetime. This equation is obtained only under the assumption that the material is very far away from thermal equilibrium (i.e., large reverse bias). While this is true for the channel layer, in the absorber there is almost no band bending and the small depleted region is still very near equilibrium. Thus, the above equation applies only to the channel layer. The appropriate values for the $Al_{.55}Ga_{.45}Sb$ channel layer are: W = 2.0 μm, $\tau_n = 5 \times 10^{-9}$ sec, and $n_i = 2.5 \times 10^8$ at 300°K.

In order to properly calculate the g-r current from a region near equilibrium, one must calculate the generation rate and integrate through the depletion region of the heavily doped material (the absorber in our case). This region is never of any importance for a homojunction device because n_i is the same for both sides of the junction and the large depletion width dominates. In the case of a heterojunction, n_i can be orders of magnitude different on the two sides of the junction. Thus, it is possible for the absorber region to dominate as the source of dark current.

The generation calculation for the absorber depletion region is extremely complex unless some simplifying assumptions are made. The generation rate is given by Eq. (4.4) of Schockley and Read.[4] Assuming that a single trap level at the center of the bandgap is responsible for the generation and that the electric field is constant in the depletion region, one can simplify the generation equation and integrate it to obtain the following expression,

$$J^{A}_{g-r} = \frac{q\, n_i\, W\, kT}{\tau_n \Delta} \left[\exp\ -(E_i - E_f - \Delta)/kT \ - \exp\ -(E_i - E_f)/kT\right] \qquad (2.6)$$

where k is Boltzmann's constant, T is temperature, E_i is the intrinsic Fermi level (i.e., $E_g/2$), E_f is the Fermi level in the heavily doped material and Δ is the potential change from equilibrium in the energy bands at the heterojunction interface with bias voltage applied. For the heterojunction device in Fig. 2.3 with an absorber doping of 5×10^{17} cm^{-3} and hole-barrier doping of 5×10^{15} cm^{-3} and 10 volts bias applied, Δ = 0.09 eV and W = 150Å.

The leakage current for a Schottky barrier is given by Sze:[5]

$$J_S^{sb} = A^{**}\, T^2 \exp\left(\frac{-q\, \phi_{bn}}{Kt}\right) \qquad (2.7)$$

where A^{**} is the effective Richardson constant, T is the temperature, ϕ_{bn} is the barrier height and k is Boltzman's constant. For a Schottky barrier to $Al_{.55}Ga_{.45}Sb$, $A^{**} \cong 100$ Amps/$cm^2/°K^2$ and ϕ_{bn} = 0.75 eV.

The temperature dependence for each of these contributions to the dark current as well as their sum have been calculated. The result is shown in Fig. 2.11. The two dominant terms are the generation through traps or defects in the completely depleted channel layer and the Schottky barrier reverse leakage. This dominance of the hole barrier g-r current necessitates the use of a wide bandgap channel layer, a heterojunction device. If a homojunction device were used with a depleted channel layer of the same bandgap as the absorber, this g-r source of dark current would be ~10^4 times larger and the device would have to be cooled to ~150°K to meet the minimum dark current requirements. The effect of dark current at the operating temperature of the device will be discussed in the following section.

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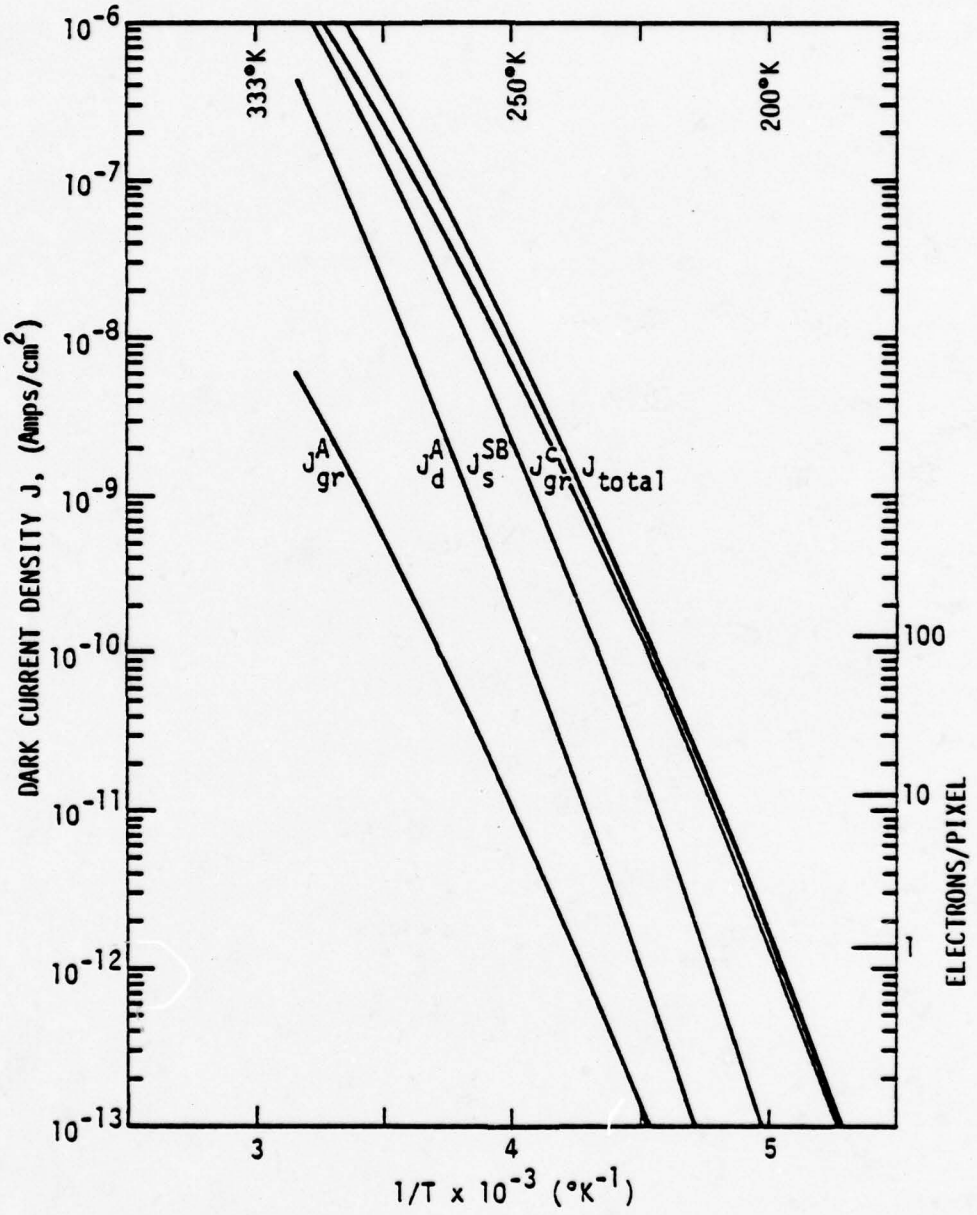

Fig. 2.11 Dark current and corresponding number of electrons/pixel as a function of device temperature of a Schottky barrier CCD with a 2u $Al_{.55}Ga_{.45}Sb$ channel layer. The contributions are:

J_d^A = generation in the absorber within a diffusion length of the channel-absorber junction

J_{gr}^A = generation within the depletion region of the absorber

J_{gr}^c = generation in the depleted channel layer

J_s^{sb} = reverse saturation current (leakage) of the Schottky barrier

3.0 MATERIAL GROWTH

3.1 Lattice Matching by As Addition

One of the significant achievements in this program in LPE growth of GaAlSb was the addition of As to bring the lattice constant to match that of the GaSb substrate.[6]

Part of the problem of the As incorporation is the difficulty in measuring the As content of the epitaxial layer accurately because of the very small amount of As required to lattice match GaAlSb to GaSb. Glissen et al. (1978)[7] have calculated the lattice constants of $Ga_xAl_{1-x}As_{1-y}Sb_y$ as a function of (x,y) assuming a linear interpolation scheme:

$$Q(x,y) = B_1 + (B_2-B_1)x+(B_4-B_3)y+(B_1-B_2+B_3-B_4)xy \qquad (3.1)$$

Q is the lattice constants of the quaternary compound

where $B_1 = Q(0,0) = A_{AlAs} = 5.611A$
$B_2 = Q(1,0) = A_{GaAs} = 5.6419A$
$B_3 = Q(1,1) = A_{GaSb} = 6.094A$
$B_4 = Q(0,1) = A_{AlSb} = 6.135A$

are the lattice constants of the binary compounds.

The present method of estimating the As content in the quaternary layer is by first measuring the lattice constants of the $Ga_xAl_{1-x}As_{1-y}Sb_y$ epitaxial layer and a reference $Ga_xAl_{1-x}Sb$ layer of the source x.

Then from equation (3.1) we get

$$Q(x,0) = B_1 + (B_2-B_1)X \qquad (3.2)$$

which gives the value of x. Then from (3.1)-(3.2) we get

$$Q(x,y) - Q(x,o) = (B_4-B_3)y + (B_1-B_2+B_3-B_4)xy \qquad (3.3)$$

This method is not accurate due to the following problems:

(i) $Q(x,y) - Q(x,0)$ is small and so is $(B_1-B_2+B_3-B_4)$
(ii) Bowing parameters are not included

Nevertheless, it served to give a trend of the As distribution coefficient in the GaAlAsSb system. One advantage of the present technique is that the actual lattice constants are measured rather than the composition. Since the lattice matching is more critical to good LPE growth as well as device quality, it is better to measure it directly and trade-off the accuracy in As distribution coefficient for lattice matching. Figure 2.12 is the distribution coefficient of a GaAlAsSb growth. One can see that at above 4×10^{-2} percent of As in the melt the As in the solid goes up steeply towards the As rich side of the phase diagram. This phenomena is similar to what has been obtained in GaSbAs as immiscibility gap except that the As concentration is still quite low for immiscibility to set in. Good homogeneous growth is therefore obtained.

One other difficulty in incorporating As in the solid is the low As solubility in the melt. By increasing the growth temperature, one will be able to increase the As solubility. Provided that the ratio of distribution coefficient of As to Sb stays constant (or goes up), this is one way to increase the As content in the solid. Already with the limited amount of work we were able to improve the surface morphology considerably by going from GaAlSb to GaAlAsSb.

3.2 Surface Morphology

Considerable improvement was made in the surface morphology of LPE GaAlSb in the latter part of the program. Part of the improvement was undoubtedly due to the better lattice matching by As addition and part was due to experience and minor improvements in the growth technique. Figure 2.13

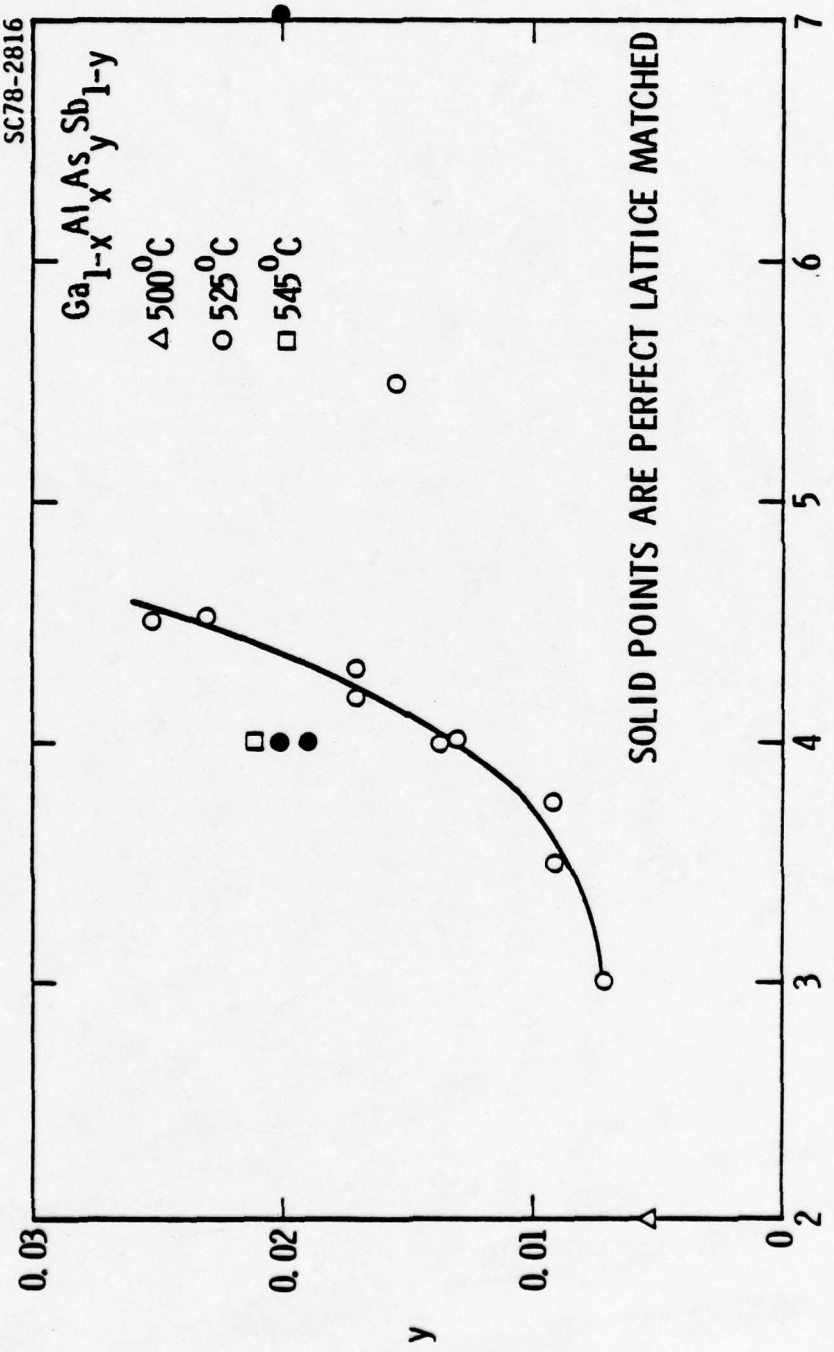

Fig. 2.12 Nonlinear distribution coefficient of As in the GaAlAsSb system. X is between 30 to 50 percent. (Two points to the right of the solid curve are results of two phase growth.)

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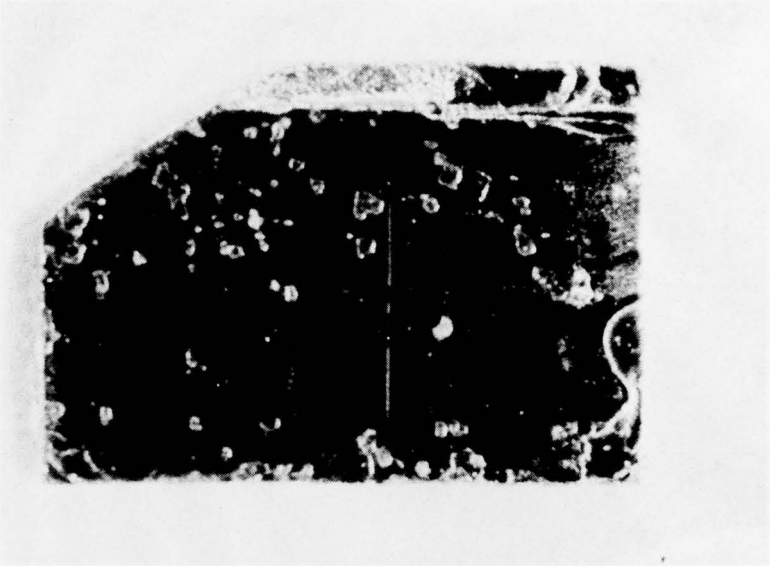
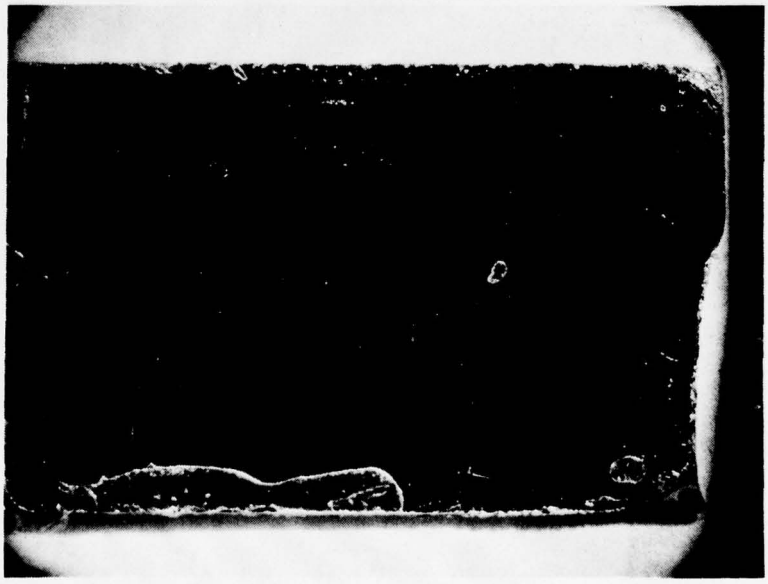


(a)



(b)

Fig. 2.13 Comparison of early GaAlSb epi-layer (a) with new GaAlAsSb layer (b). Wafer (b) is 1cm x 2cm.

shows two photographs of an early and a later surfaces of GaAlAsSb epitaxial layers.

3.3 Aluminum Concentration in GaAlSb

The desired aluminum concentration of the GaAlSb is ideally as high as possible for obvious reasons of large barrier height and low dark current. However, LPE growth considerations limits this to no more than 55%. During this reporting period, the surface morphology was steadily improved. However, when examined electrically by use of small Schottky barrier diodes, it was found that the p-n junction characteristics were quite leaky. Mesa etching through to the substrate also did not improve the leakage current indicating a bulk, leaky junction.

For 30% Al GaAlSb layer, however, mesa etching considerably reduced the p-n junction leakage current. Details of these results are reported in a later section.

4.0 DEVICE CHARACTERIZATION

4.1 Schottky Barrier Height

Schottky barrier height to $Ga_{.45}Al_{.55}Sb$ was evaluated by three independent methods: photoresponse, C-V, I-V. In all the experiments to be described, the Schottky metal used was Cr-Au. The surface was lightly etched prior to metal deposition to remove native oxides which invariably form on the GaAlSb surface. The first metal deposited is Cr (~100Å). This serves to enhance adhesion of the metalization to the semiconductor and blocks diffusion of Au into the semiconductor. This deposition is immediately followed (in the same evaporation system) by a deposition of Au. This deposition is typically between 1000Å and 5000Å. The thickness has no influence on the Schottky barrier parameters. This procedure is followed in all experiments except the photoresponse method in which case the total metalization thickness is less than 100Å, in order to facilitate optical transmission. The metalization pattern consists of round dots (3 mil to 5 mil dia) uniformly distributed on the surface. The contact to the layer is achieved by a large dot, typically 20 times the diameter of the small dots. This dot has larger leakage and therefore acts as a pseudo-ohmic contact.

4.1.1 Schottky Barrier Height Determination by the Photoresponse Method

For this experiment thin Cr-Au Schottky dots, as described above, were evaporated on the sample. The sample was mounted in a suitable header and the dots were wire-bonded to pins on the header. The experiment was performed in a Cary-14 spectraphotometer especially modified with a feedback system to maintain a fixed intensity as the wavelength changes. The sample is inserted in the light beam and electrically connected to a current-mode preamplifier which in turn is connected to a lock-in amplifier. The lock-in is synchronized to the chopping frequency of the light beam within the spectrometer. In this way, a plot of photocurrent vs. wavelength is obtained. The Schottky barrier height is determined directly by extrapolating the long wavelength photoresponse. Typical data is shown in Figs. 2.14, 2.15.

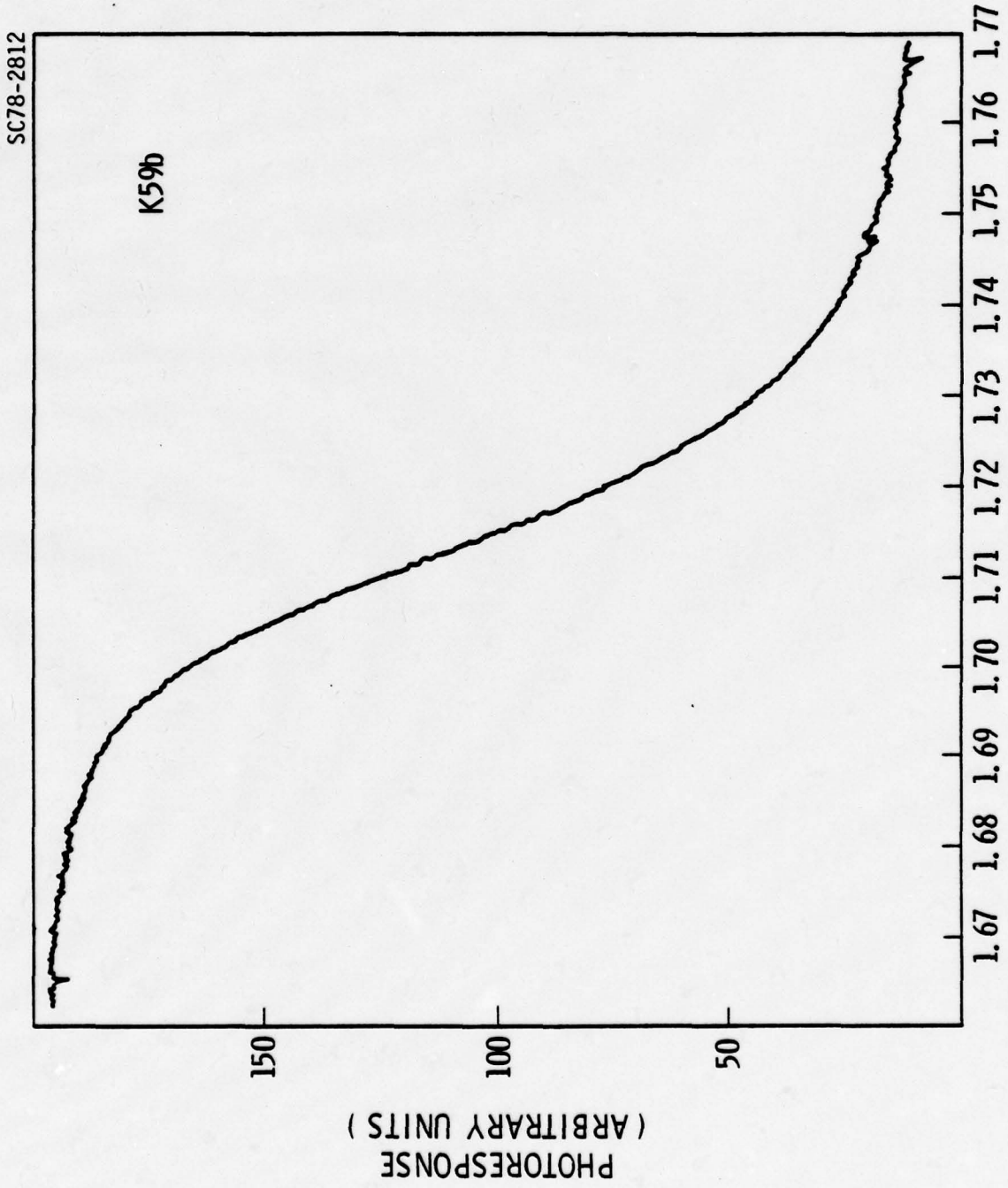


Fig. 2.14 Long wavelength photoresponse of 100Å Cr-Au Schottky barrier on $Ga_{.45}Al_{.55}Sb$.

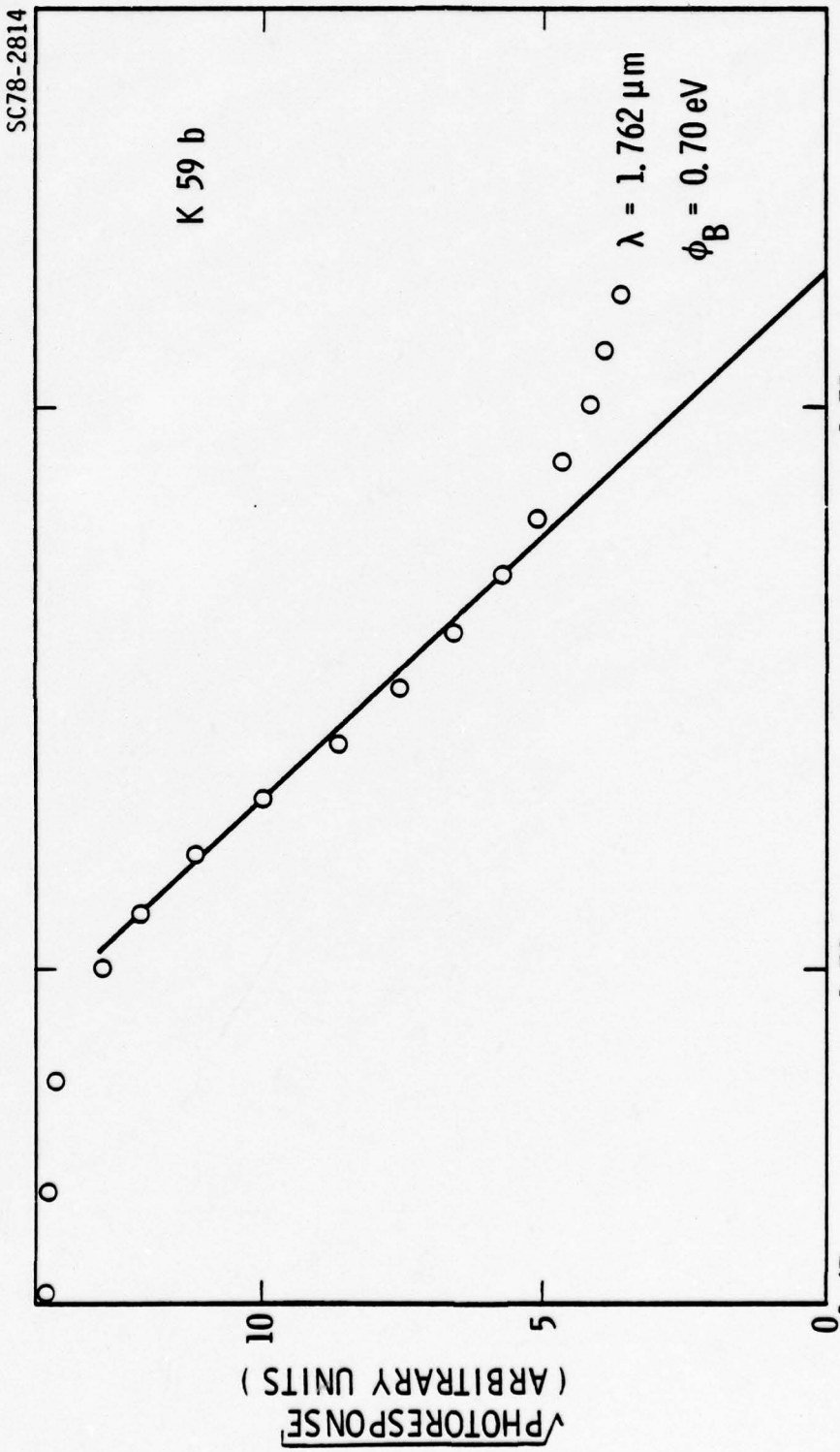


Fig. 2.15 Measured photoresponse and interpolated barrier height from Cr-Au Schottky barrier on $Ga_{.45}Al_{.55}Sb$.

4.1.2 Schottky Barrier Height Determination by C-V Measurement

Capacitance vs. reverse bias voltage on the Schottky dots described above were taken at frequencies of 50 kHz and 1 MHz. The two contacts were between a small dot and the large dot described before. For the purposes of this experiment the arrangement can be thought of as the rf voltage being applied across two capacitors. Since the test capacitor (small dot) is much smaller than the other ($\simeq \frac{1}{20}$ dia.) most of the applied voltage drops across the smaller capacitor and the effect of the depletion region under the larger dot is negligible. Once the C-V data has been obtained, a plot of $(1/C^2)$ vs. V reveals the barrier height by the intersection of this line with the voltage axis. Figures 2.16 and 2.17 show the C-V data and the corresponding $(1/C^2)$ vs. V data.

4.1.3 Schottky Barrier Height Determination by I-V Method

The barrier height can also be obtained from the forward I-V data. A plot of ℓn I vs. V in the forward diffusion region is made (see Fig. 2.18) and the line is extrapolated to the current axis. For this measurement, a Richardson constant of 100 amps/cm^2/°K^2 was assumed.

4.1.4 Comparison of Results of Various Schottky Barrier Height Determinations

All the above experiments were conducted at 300°K. The following is a tabulation of the results:

Table I. Comparison of Schottky barrier height of Cr-Au to $Ga_{.45}Al_{.55}Sb$ as determined by three methods

Method	Schottky Barrier Height (eV)
Photoresponse	0.70
C-V	0.74
I-V	0.74

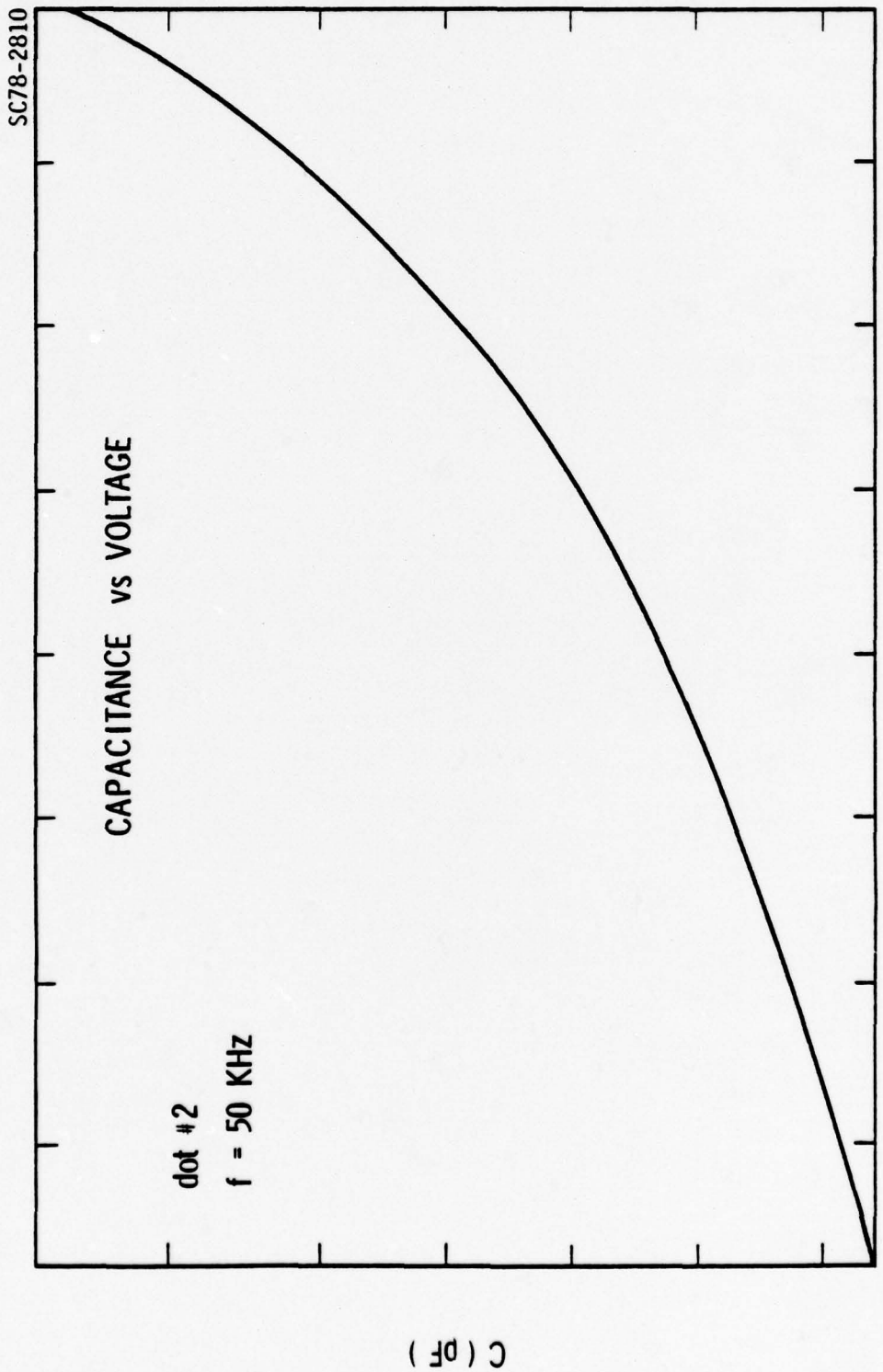


Fig. 2.16 Capacitance vs. voltage of Schottky barrier diode on $Ga_{.45}Al_{.55}Sb$.

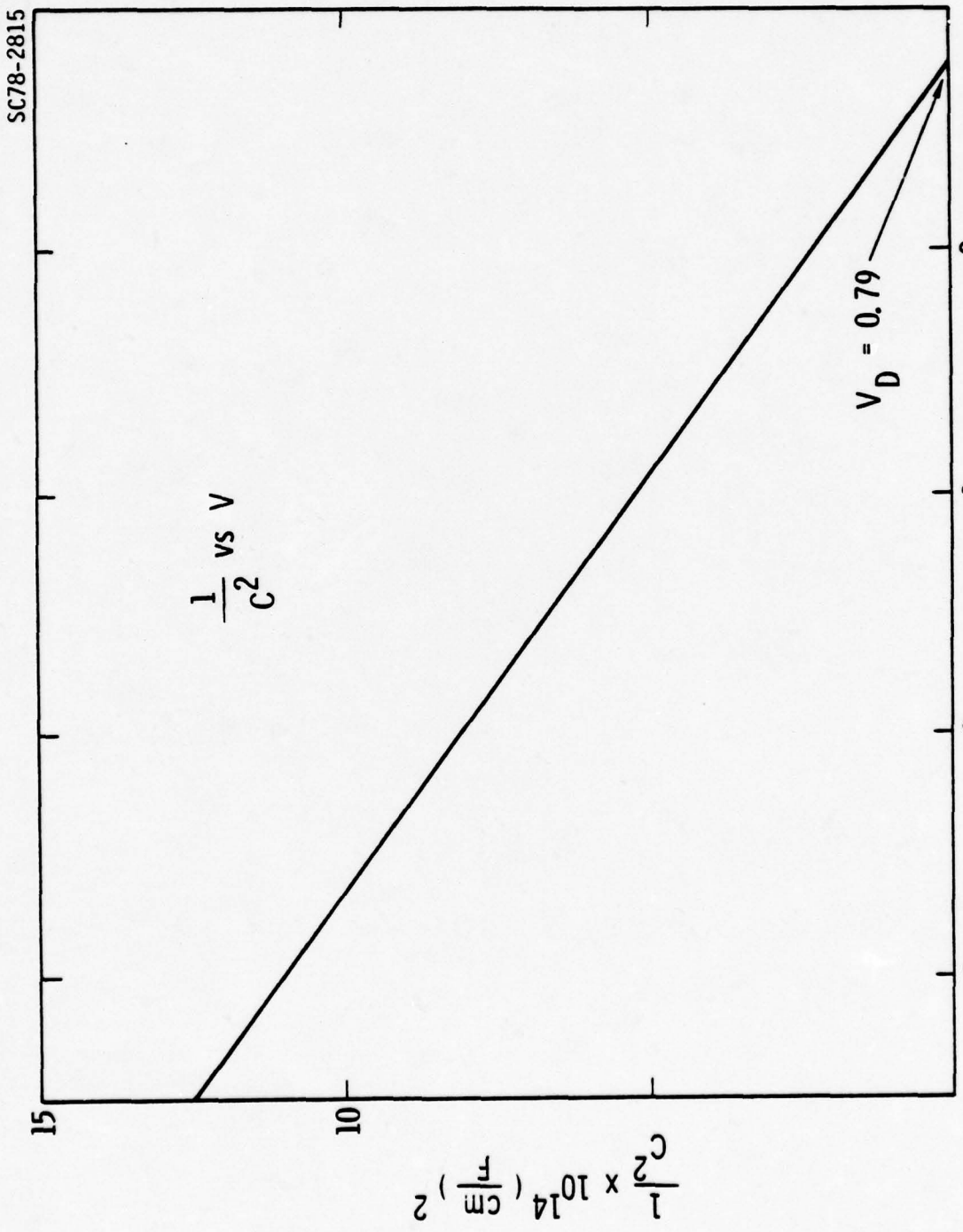


Fig. 2.17 Schottky barrier height determination from C-V data of Schottky barrier gate on $Ga_{.45}Al_{.55}Sb$.

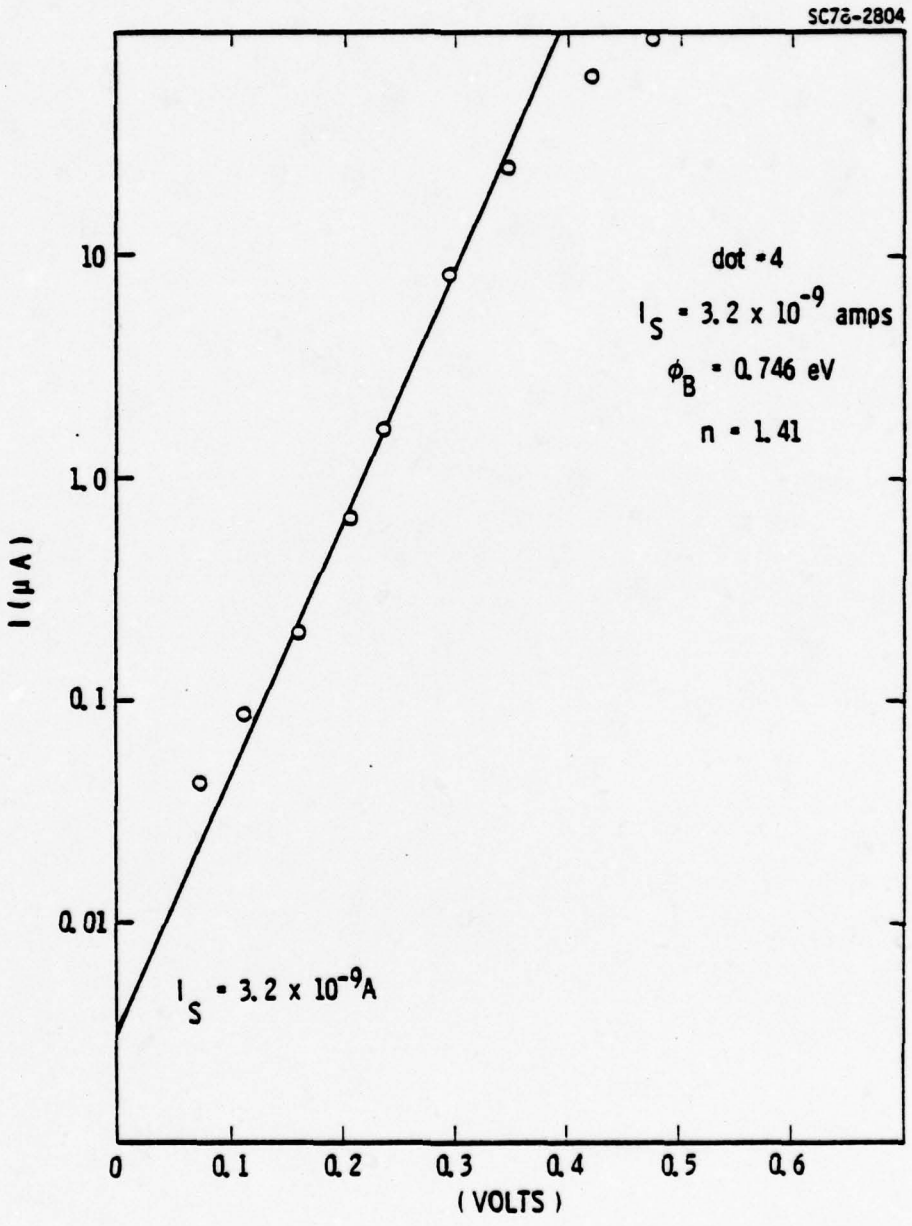


Fig. 2.13 Forward current-voltage characteristics of Schottky barrier gate on $Ga_{.45}Al_{.55}Sb$.

4.2 Carrier Concentration Profiles

Doping profiles were found using a PAR 410 C-V plotter interfaced with a Data General Eclipse computer. A dielectric constant of 15 was assumed. In general the results showed a uniform doping profile throughout the thickness of the layer. The resulting carrier concentration ranged from 8×10^{15} to 3×10^{16} cm^{-3}. A typical doping profile is shown in Fig. 2.19. The Schottky breakdown voltage ranged from 10-25 volts.

4.3 Layer Thickness and Punch-Through

In order to be able to operate the CCD, a total depletion (a punch-through) has to be achieved in the layer by applying a negative voltage to each gate and to the guard-ring surrounding the CCD structure. This voltage should be lower than the Schottky breakdown voltage. It was found experimentally that for layer doping of 10^{16} cm^{-3} and breakdown voltage of ~20 V, the layer thickness should be at most ~2.0 μm in order to achieve punch-through.

The layer thickness was evaluated by several methods:

(1) Electron beam induced current
(2) Chemical selective-staining
(3) C-V measurements
(4) I-V measurements using a dot-guard-ring structure.

In order to verify if a punch-through can be reached under a single transfer gate, a C-V measurement was taken between a single transfer gate and the guard-ring surrounding the whole CCD structure (large Schottky contact compared to the single gate Schottky contact). An indication of punching-through is when a flat portion (constant capacitance) is observed in the C-V curve under reverse bias to the single transfer gate, (see Fig. 2.20). From this curve the layer thickness can be calculated given the gate area and the n-layer dielectric constant.

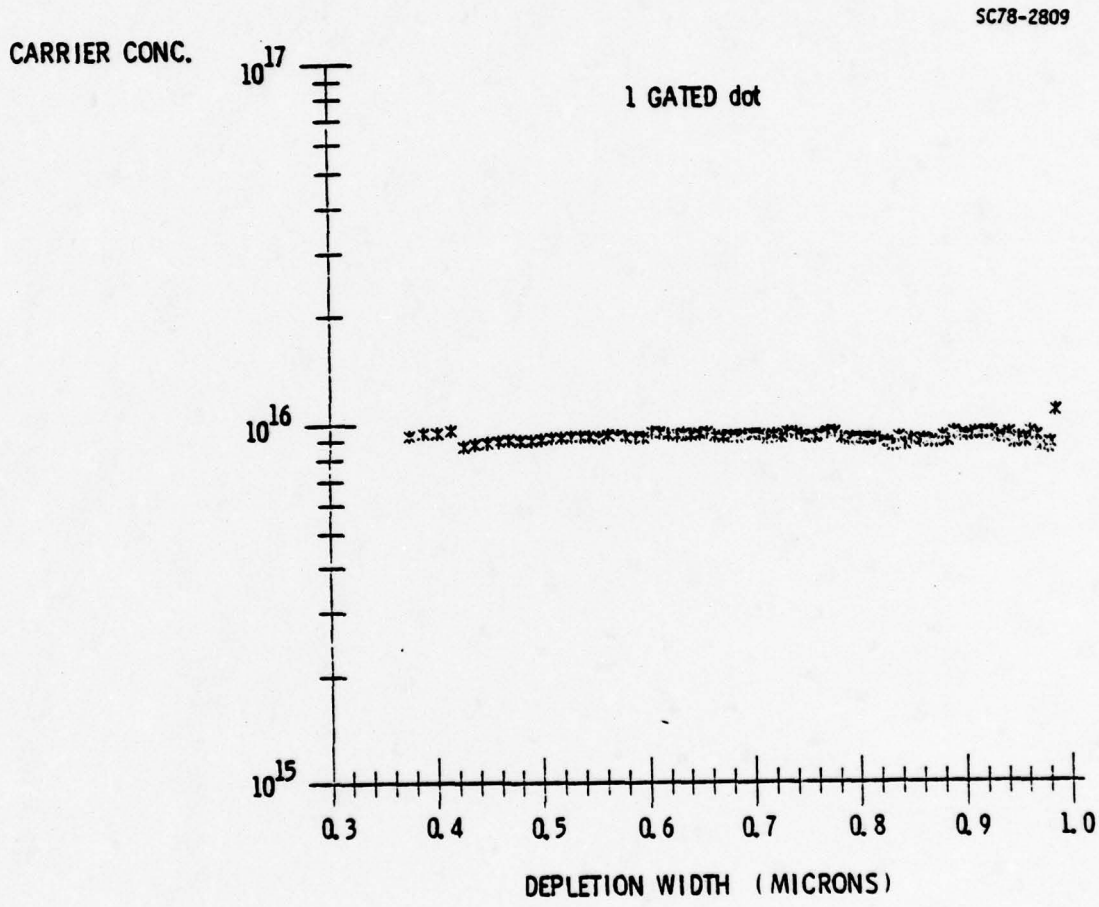


Fig. 2.19 Carrier concentration profile of n-type $Ga_{.45}Al_{.55}Sb$ epitaxial layer on p-GaSb substrate.

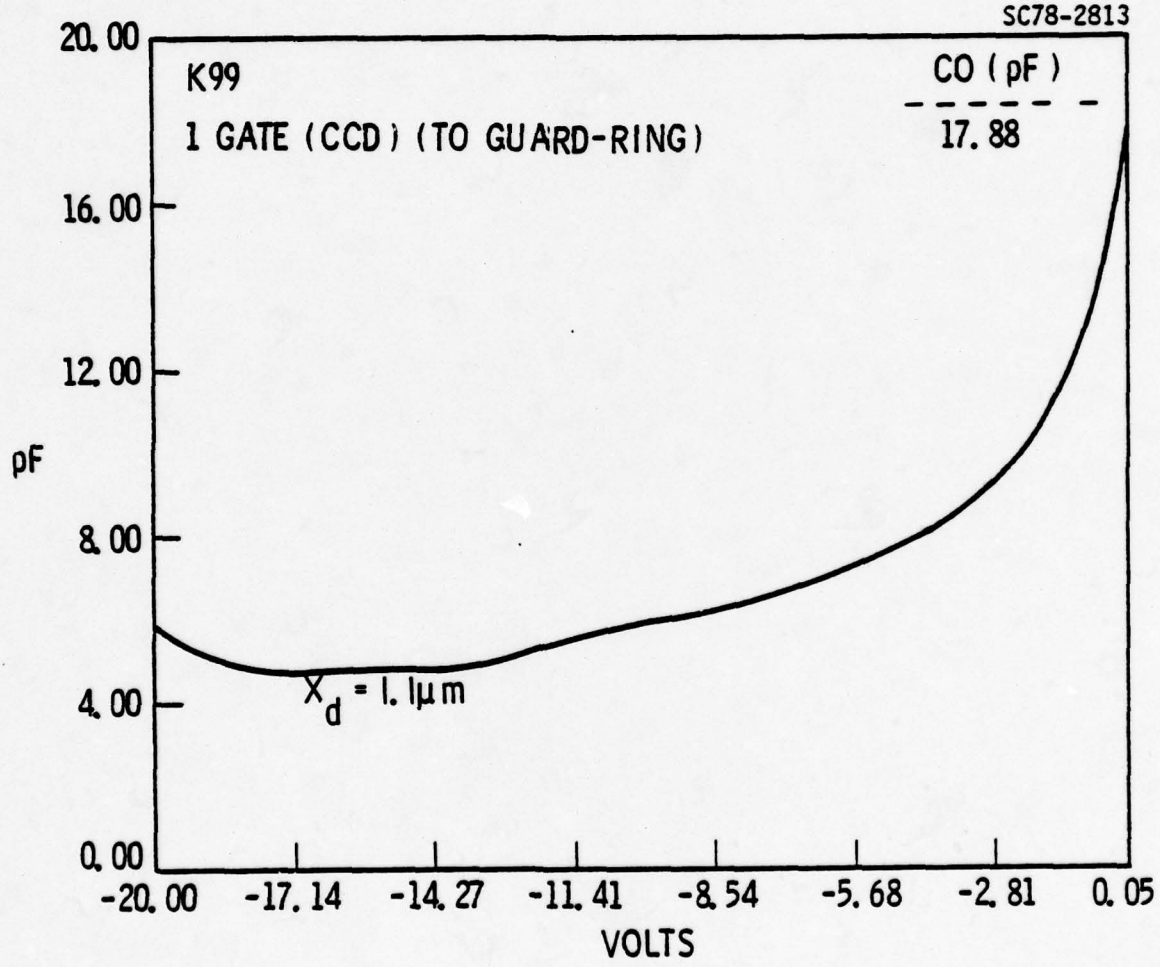


Fig. 2.20 Capacitance-voltage profile of $Ga_{.45}Al_{.55}Sb/GaSb$ CCD measured between one transfer gate and guard ring.

4.4 p-n Junction Characterization

In our first mask design the area of a storage gate is 380 μm x 113 μm = 4.29×10^{-4} cm^{-2}. In thermal equilibrium a full "well" contains:

$$n = N_D \, Ad = 4.29 \times 10^8 \text{ electrons}$$

assuming: $N_D = 10^{16}$ cm^{-3}

$A = 4.29 \times 10^{-4}$ cm^2 (area)

$d = 1.0$ μm (thickness)

At an operating frequency of 100 kHz ($T = 10^{-5}$ sec) the corresponding current that can supply this charge per cycle is:

$$I = \frac{qn}{T} \text{ (A)} .$$

In order to operate the CCD properly one has to be sure that the thermal generation current in the p-n junction is much smaller than the above number.

In order to evaluate the p-n junction leakage current a dot (area = 1.5×10^{-4} cm^2) surrounded by a guard-ring was used.

Using this structure, I-V measurement can be made and p-n junction characteristic can be evaluated by biasing the guard-ring to punch-through voltage and thus confining the dot area, eliminating the need for a mesa around the dot.

Using the guard-ring allows us to study the effectiveness of the guard-ring for later use of this concept in the real device as a channel stop.

Figure 2.21 shows the current through a dot (area = 1.5×10^{-4} cm^2) as a function of the voltage on the guard-ring for different dot voltages (p-n junction reverse bias) (this layer was quite lightly doped and thicker than usual: BV = 36 V, d = 3.5 μm, $N_D = 7 \times 10^{15}$ cm^{-3}). It is seen that a dot area

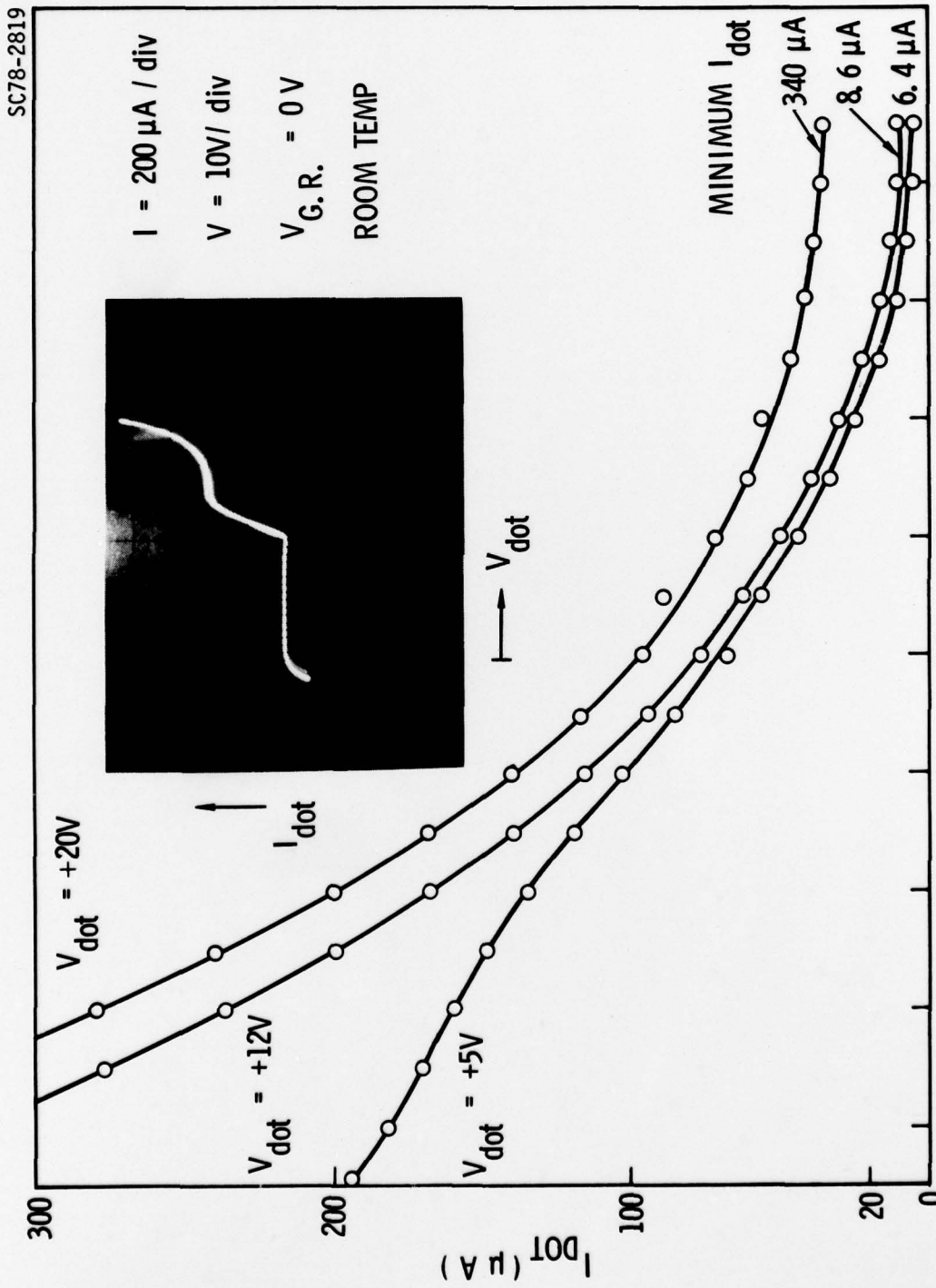


Fig. 2.21 p-n junction leakage of n-GaAlSb/p-GaSb heterojunction as a function of guard ring voltage. Inset shows p-n junction leakage (first quadrant) with zero guard ring voltage.

confinement, a punch-through underneath the guard-ring occurs at a guard-ring voltage of about -30 V.

I-V characteristics and the effect of the guard-ring are shown in Fig. 2.22 (room temperature) and Figs. 2.23 and 2.24 (77°K). The leakage current at 1 volt p-n junction reverse bias (77°K) is sufficiently low - less than 1.0 nA corresponding to 6.25×10^4 electrons, (area = 4.29×10^{-4} cm^2, f = 100 kHz) to allow CCD operation.

In order to evaluate the surface leakage current when using a mesa structure, a mesa structure was etched around metal patterns with different areas and it was found that the p-n junction leakage current is proportional mainly to the gate area rather to its perimeter suggesting that the surface leakage current on the mesa edges is small compared to the p-n junction bulk leakage current. That the surface leakage current is small was verified by using EBIC response from the mesa edge near the p-n junction.

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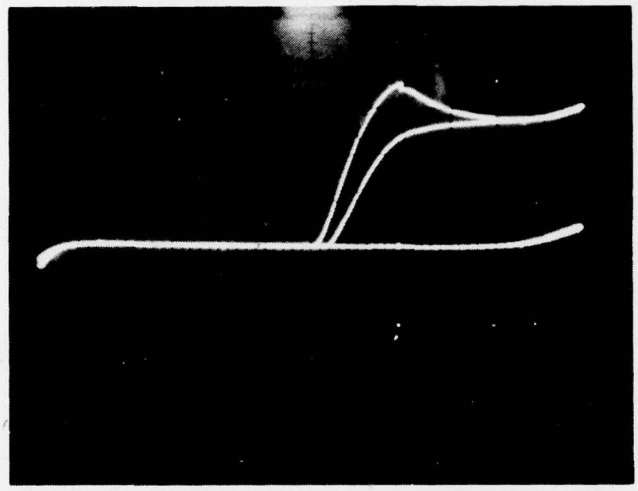
(GaSb SUBSTRATE IS GROUNDED)

KN55a
(WITH GUARD-RING)

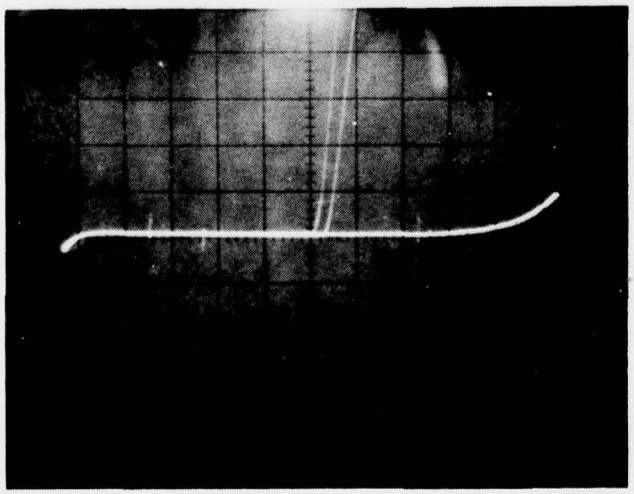


10 μa/div

2V/div

0 VOLTS AND -12V
TO THE GUARD-RING

SCHOTTKY REVERSE ← → P-N JUNCTION REVERSE BIASED



2 μa/div

2 V/div

OV AND -12V TO
GUARD-RING

Fig. 2.22 Room temperature p-n junction I-V characteristics of n-GaAlSb/p-GaSb heterojunction showing effect of guard ring bias.

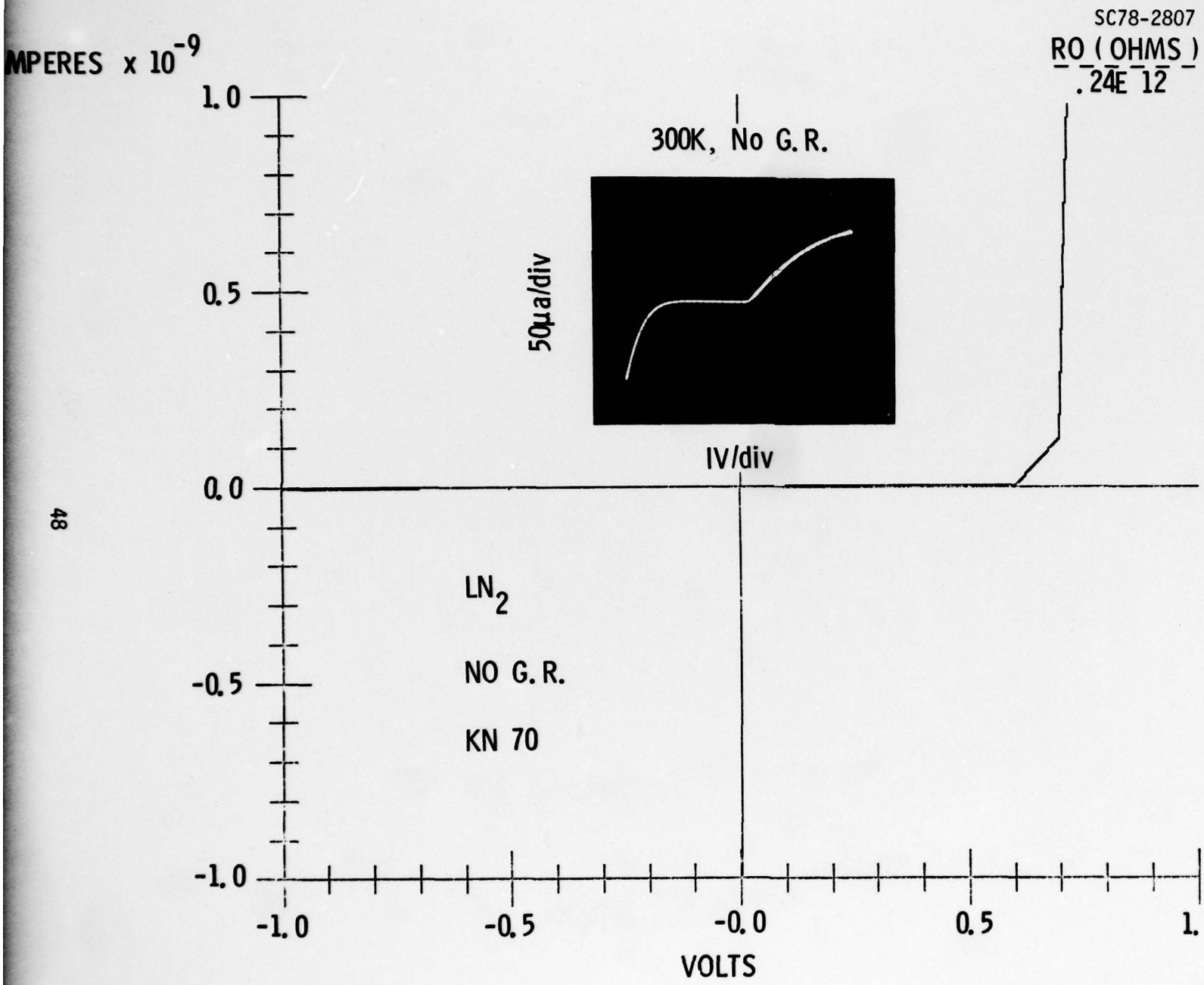


Fig. 2.23 Leakage current of Schottky barrier gate on n-$Ga_{.45}Al_{.55}Sb$ room temperature (inset photo) and at 77K.

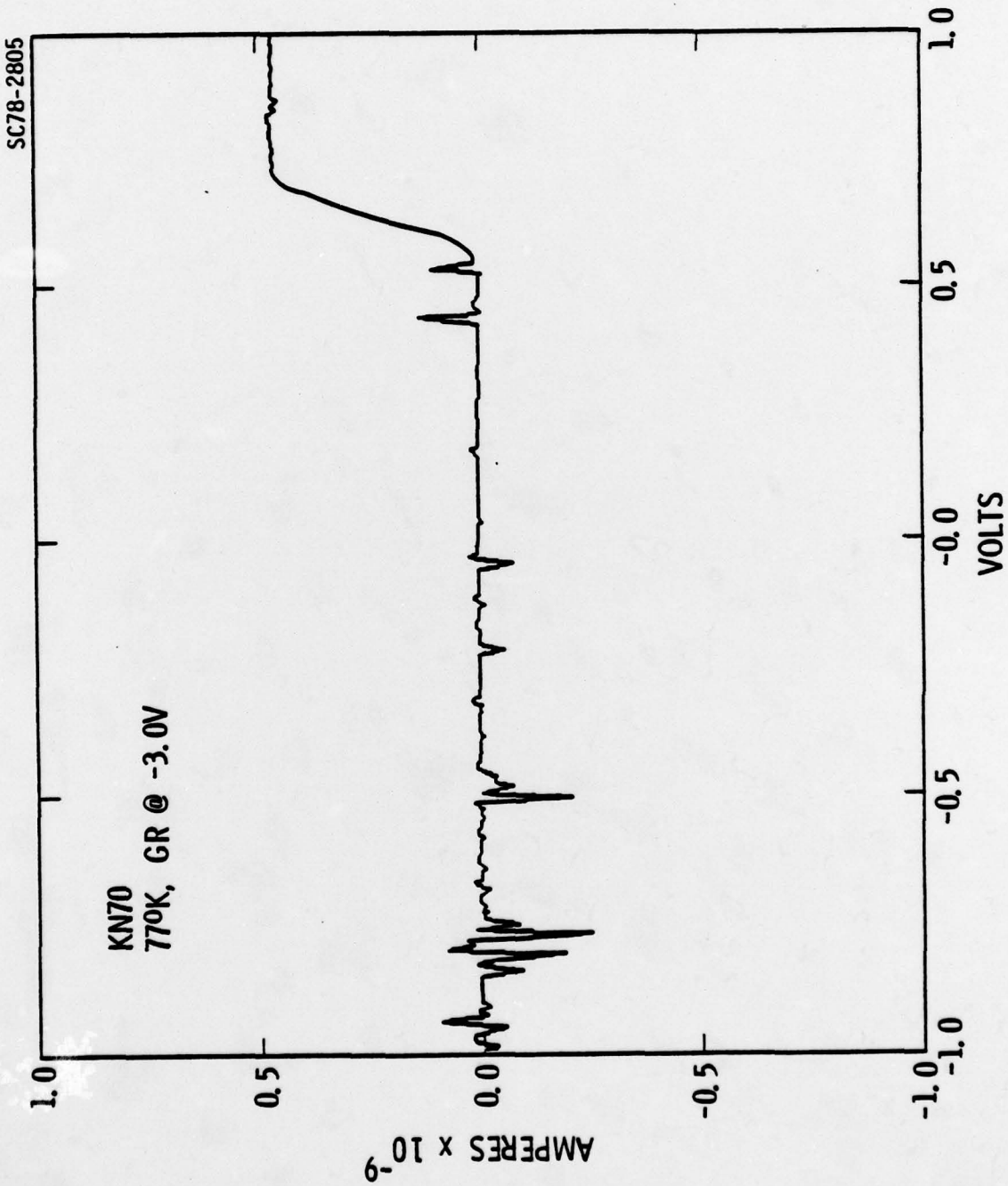


Fig. 2.24 Leakage current of Schottky barrier gate at 77K, expanded scale with G.R.

5.0 HETEROJUNCTION CCD DEMONSTRATION

One of the most significant results of this program is the operation of the first heterojunction CCD. This device consists of four gates, and is entirely planar. This demonstration was made possible because of the drastically improved epilayer surface morphology made possible by addition of As to the melt which results in a quaternary structure active layer, GaAlAsSb. One of the devices fabricated from the new quaternary wafers is shown in Fig. 2.35. The selection of devices suitable for bonding proceeds as follows. All the devices which do not have obvious lithographic flaws are probed one at a time. First, the device is tested for shorts between gates and shorts to the guard ring. Next the guard ring is tested for leakage. Finally, the ohmic contacts are tested by measuring the I-V characteristic between the input and output ohmic contacts. Unfortunately, this test is not conclusive at this stage, since the I-V characteristic does not distinguish between ohmic contacts that are properly formed and those which are shorted to the substrate. Measuring the I-V characteristic between an ohmic contact to the n-layer and the bottom substrate contact is also not conclusive. Normally, this test should result in a normal p-n diode characteristic, where the reverse bias condition corresponds to the reverse bias of the p-n junction. In this case, since the areas of the p-n junction is uncontrolled, a large leakage current is measured which is often indistinguishable from a shorted p-n junction. The solution to this problem is, of course, a guarded diode consisting of an ohmic contact dot surrounded by a Schottky guard ring which can be biased to isolate the p-n junction, in much the same way it is done in the CCD channel-stop.

Devices which exhibit no shorts and which have good ohmic contacts can be bonded up as CCDs. Even if ohmic contacts have not been formed, the device is useful for charge storage experiments. In fact, several devices like this have been bonded up and tested.

SC79-3528

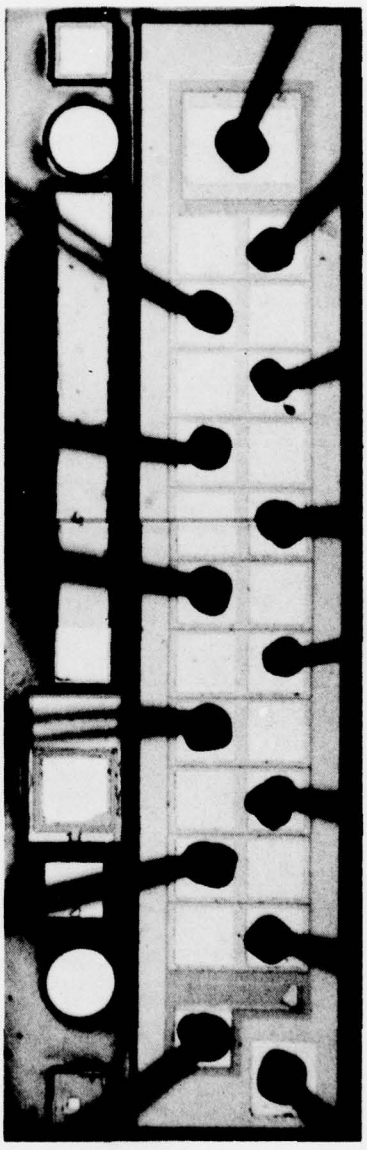


Fig. 2.25 GaAlAsSb/GaSb CCD structure.

The first experiment performed with one of these devices (K103) was to verify the charge storage effect in this planar structure. This experiment is important because it verifies the concept of using a biased guard ring for a channel stop. For this experiment, the guard ring is biased with a negative voltage sufficient to deplete the active layer and therefore isolate the device active area from the rest of the wafer. In this way, the isolation between a signal charge pocket and the rest of the wafer is the same as the isolation between transfer gates.

To perform this experiment, capacitance as a function of time is measured after the active region has been depleted of carriers. All the transfer gates are tied together and form one terminal of the test capacitor. The substrate is the other terminal. The guard ring is connected to an adjustable negative power supply. The measurement is initialized by pulsing the gates so that they are depleted. The capacitance is then measured as a function of time to determine how long it takes for equilibrium to be reestablished. This is the charge storage time. The best charge storage time measured was 800 sec at 77°K. This experiment is, of course, carried out in the dark. If the sample is illuminated during the experiment, the capacitance rapidly returns to the equilibrium value. The total gate area in this device was 4.3×10^{-3} cm^2. Much longer storage time should be attainable in the future. One problem with this initial experiment was that the potential outside of the guard ring was not controlled. This potential can float arbitrarily and can lead to dark current contributions from the rest of the wafer. In future experiments, this potential will be "pinned" to a value somewhat more positive than the guard ring potential to prevent electrons from the epilayer outside the device from contributing to dark current.

The most important test is to operate a device as a CCD and observe charge transfer. Such a test was successfully performed on Oct. 11, 1978. The major problem experienced in the attempt to perform this test was the lack of good ohmic contacts. In fact, in the first demonstration of charge transfer in the heterojunction CCD, the device selected had only one usable ohmic

contact. A defect had, however, caused the Schottky barrier of gate number 6 to be leaky. This gate was used as the output ohmic contact. From then on, the configuration was quite conventional.

Figure 2.26 shows the configuration of the first charge transfer demonstration. The input and output (Gate 6) ohmic contacts are biased to a positive voltage and are capacitatively coupled for signal input and output. The input pulse is synchronized to occur when ϕ_2 is positive. Therefore, the first clocked gate must be ϕ_2. The last gate is grounded so that it acts as a barrier for the charge pocket (see Fig. 2.26, T4 and T5). The remaining gates are tied to ϕ_3 and ϕ_1. The output pulse can be seen to occur when ϕ_1 makes a positive to negative transition. Figure 2.27 shows the results of this experiment. Figure 2.27a shows the input and the time delayed output pulse. Figure 2.27b shows the relation of these pulses to the clock phases. As can be seen from a study of Fig. 2.26 this experimental arrangement results in charge being injected into the first clocked gate (ϕ_2) every cycle.

This is the reason for the small difference between the output signal level and the background. Although this device consisted of only four gates, it is an encouraging first step and is a precursor to a larger device being operational, now that improved material technology has been achieved.

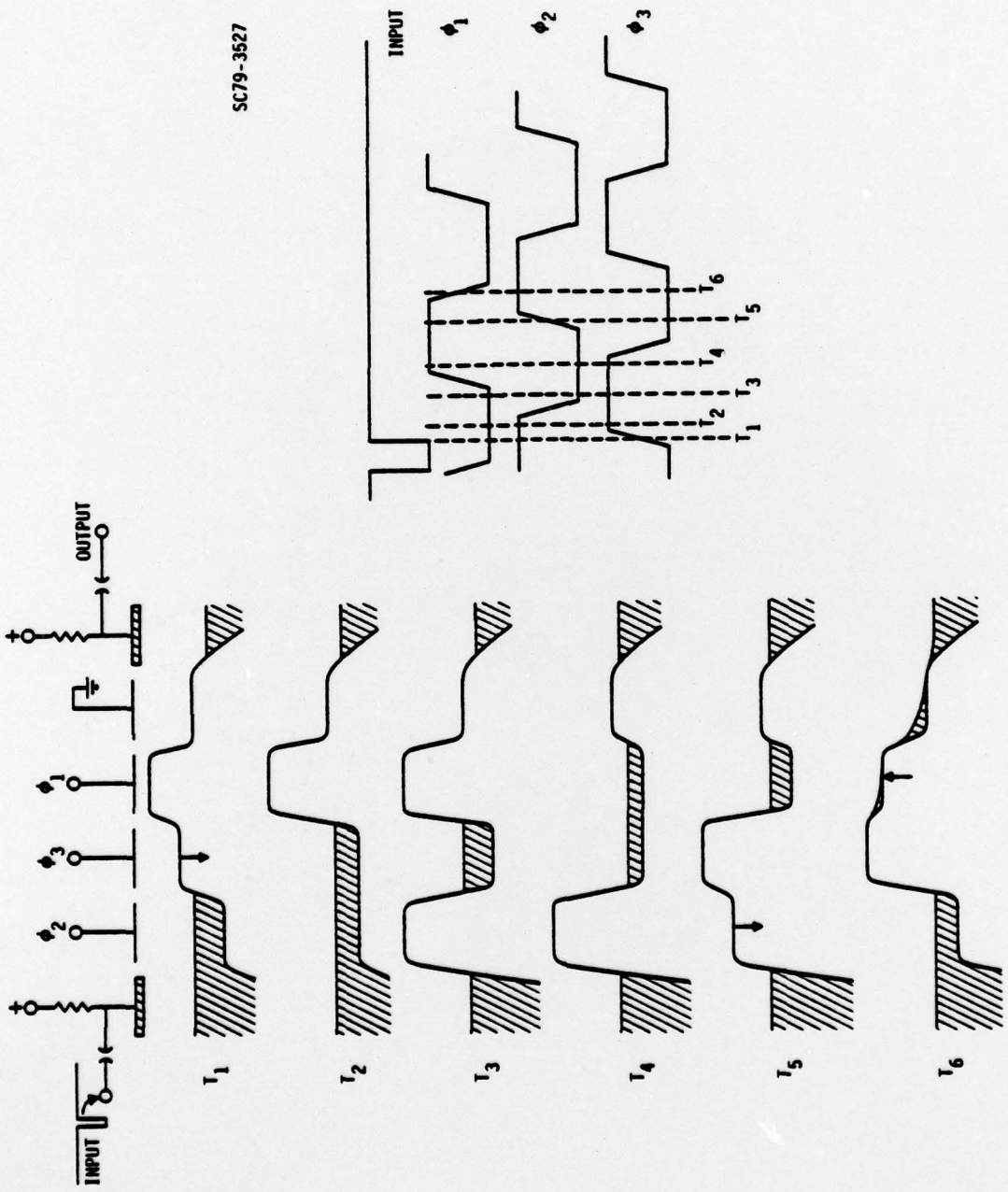


Fig. 2.26 Heterojunction CCD experimental set-up and timing diagram.

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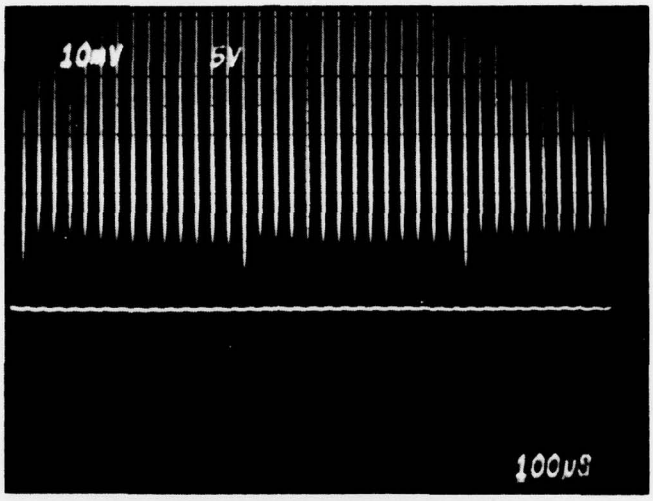
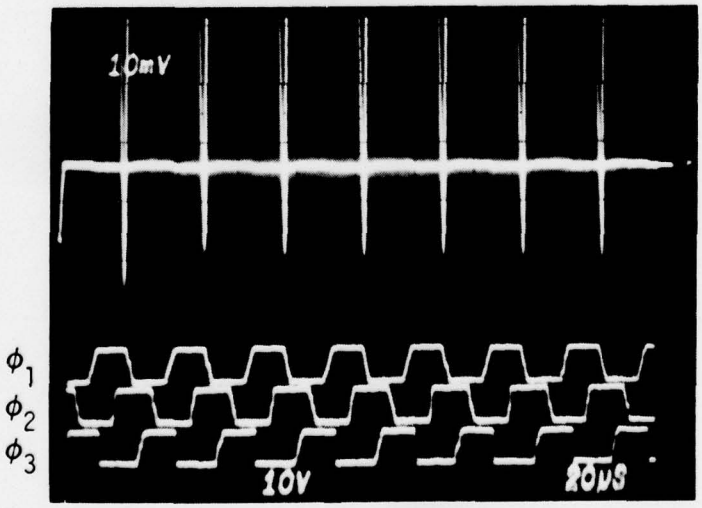


(a)



(b)

Fig. 2.27 (a) HJCCD output (top) and input pulse (bottom); (b) HJCCD input and output (top two waveforms) and 3 phase clocks, (bottom).

6.0 CONCLUSION AND RECOMMENDATIONS

This report marks the end of the current program to develop a charge coupled image sensor for the 1-2 μm spectral region. At this point, it is appropriate to summarize the results, discuss the difficulties, and project future progress toward the ultimate goal of a large area (400 x 400 pixels) image sensor.

The most important results are, as discussed in Section 2, the vastly improved GaAlAsSb material quality, in particular the improved surface quality. The material quality at present is such that 1 mm x 1 mm focal planes can be fabricated with usable yield. The second significant result is that it was demonstrated that the guard ring isolated device is feasible. Using a guard ring isolated device scheme, a focal plane can be designed which requires only 4 masking steps (including 2 level metalization), of which only 1 has critical tolerances and small (~1 μm) line widths. Finally, a prototype CCD in the GaAlAsSb/GaSb heterostructure was successfully operated. This is the first demonstration of CCD operation in a heterojunction structure. It is a significant first step since it opens the way for what is potentially a very high performance CCD imager technology.

Also significant, a wafer of GaAlSb/GaSb supplied by the Science Center was successfully fused to Corning 7056 glass by Dr. John Pollard at Night Vision Labs. This is a crucial part of the final imager design.

The only significant difficulty remaining is the formation of ohmic contacts to the n-GaAlAsSb epitaxial layer. Most of the difficulty arises from the native oxide which is invariably present on the epilayer surface. This problem can be alleviated most satisfactorily by growing a thin (~1000A) layer of n^+ GaSb on top of the n-GaAlAsSb. Subsequent etching of the n^+ GaSb from the surface everywhere except where ohmic contacts are desired, will substantially enhance formation of ohmic contacts. Alternatively, the GaAlAsSb surface can be covered with evaporated or sputtered oxide, then etched in a solvent which attacks the native oxide. Immediate evaporation of ohmic contact metalization will result in uniform subsequent alloying.

Yet a third method, which will be possible with the installation of a new piece of process equipment, is to sputter etch the surface where the ohmic contact is desired and perform an in situ metalization. The GaAlAsSb/GaSb technology is now at the stage where the next logical major step is the development of a device with considerably greater gate complexity than the existing initial device. For example, devices with approximately 100 gate complexity can be fabricated. Such a device would, if arranged as a linear array, permit the evaluation of transfer efficiency, characterization of bulk traps, and dark current. An imager can also be fabricated to allow evaluation of spectral response and sensitivity. From that point on, the development of larger area imagers will be paced, essentially by continued material development. This is partly due to the fact that Schottky gate integrated fabrication techniques are rapidly being developed at the Science Center in other programs and, therefore, problems such as multi-level metalization are not expected to hamper progress.

7.0 REFERENCES

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