LEVEL II

GaAs MONOLITHIC MICROWAVE SUBSYSTEM TECHNOLOGY BASE

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
Baltimore, Maryland 21203

Technical Report for period 15 March 1978 - 15 September 1978

Prepared for

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
Contract No. N00014-78-C-0268
DARPA Order No. 3543

Contract Authority: NR 251-028

Effective Date of Contract: March 15, 1978
Expiration Date of Contract: September 30, 1979

Principal Investigators

Dr. J. Oakes (Devices) (412) 256-7665
D.W. Maki (Circuits) (301) 765-7331

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23. ABSTRACT (Continued)

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Interdigital capacitors with values up to 2 pf have been fabricated for use as tuning capacitors.

A one bit phase shifter has been designed using lumped elements and Schottky barrier chip diodes. Testing was delayed however by a mask error which is being corrected.

ABSTRACT

In the materials area, effort on this program during the first six months has been devoted to process technology development and materials study and qualification. Equipment delays and malfunctions have limited progress, however, direct implants and implants into both VPE and LPE were investigated with encouraging results.

Investigation of self-aligned gate FET's have shown high gate resistance and feedback capacitance, and corresponding low gain, resulting in a decision to revert to realigned gate FET's.

Interdigital capacitors with values up to 2 pf have been fabricated for use as tuning capacitors.

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SUMMARY

The first six months of the program have primarily been devoted to process technology development, and materials study and qualification. The program has been delayed due to late deliveries of some equipment and subsequent revelations of equipment malfunction and improper assembly. These problems are being worked out, and in the meantime arrangements have been made and implemented to have ion implanting and capping done externally.

A major concern in the program is a reliable supply of qualified GaAs. Although a 3 inch crystal puller from Metals Research Corporation of Malvern England has been ordered, it will not be delivered and operating for some time. We have received and evaluated wafers from several vendors and have a large supply on order from Metals Research. These latter wafers are from a boule pulled on a machine identical to the one we are getting, and which should pass the Westinghouse qualification tests.

Although it is advantageous to implant directly into SI GaAs without the expense and extra processing involved in buffer layers, it is not yet established that consistent high quality implants can be achieved due to the high background dopants in unbuffered material. Direct implants, and implants into both VPE and LPE are currently being investigated. The data from direct implants made to date have geen encouraging but inconclusive. We must evaluate the test data from additional implantation runs and decide on a single technology to concentrate our efforts on. Specifically we must:

(1) determine if the lower mobilities resulting from direct implanation into SI GaAs observed at Westinghouse and other laboratories is an inherent deficiency,

(2) determine the expected magnitude of the difference in mobility,

(3) predict the performance degradation if any of the active devices (particularly the power FET's) due to the reduced mobility, and

(4) evaluate the relative value of the performance degradation if any versus the monolithic circuit processing simplification and projected yield and cost benefits due to eliminating the difficult buffer layer growth steps.

At the start of the program our main device effort was directed toward self-aligned gate techniques, and the first several runs of FET's made used them. Problems with high gate resistance and feedback capacitance resulting in low gain caused us to reconsider. The last run of FET's were made with realigned gates using our new Kasper mask aligner. Preliminary results have shown good gain, but disappointing power output and efficiency. The best results were obtained on wafers which were directly implanted.

In order to obtain high power output in a small area, an efficient means of heat sinking is required. The discrete devices fabricated to date use conventional heat sinking, i.e. the GaAs chip is thinned and mounted on a copper heat sink, with the drains wire bonded together on the top surface. A critical area in our program is the technique of etching through the back of the substrate and plating in a metallic structure to provide heat sinking and low inductance source interconnections. We have demonstrated the etching and plating process with good results, but we need to test many devices over a wide range of temperatures to check for any thermal stress problems and their impact on total process yield.

Interdigital capacitors have proven to be reliable, well controlled lumped elements for applications through X-band for capacitances up to 2 pf. Low yield was experienced on the early devices due to improper handling of the substrates and poor metallization. Later runs with a better surface finish have shown a greatly improved yield. Although the interdigital capacitor is satisfactory for all of the important tuning capacitor requirements, it cannot provide the much larger capacitance needed for bypass and feedthrough

applications, and it is incompatible with VPE buffer layers produced to date. The resistivity of the 10^{14} VPE material is only 13 Ωcm. This results in a shunt resistance term across the capacitor and yields an unsatisfactory low Q of 0.7. This is another strong point in favor of direct implants. Bypass and DC blocking applications require a higher capacitance than can be provided by interdigital capacitors. For these, overlay capacitors are necessary but a high Q is not required. Preliminary investigation of anodized aluminum capacitors has shown their fabrication process to be high yield and well controlled.

A one bit phase shifter has been designed and built using lumped elements and Schottky barrier chip diodes. There is a mask error which will prevent the device from working and a new mask is being generated. Circuits made with the defective mask will be RF tested to provide a limited amount of data.

The principal program thrusts during the next few months will be directed toward)1) identifying and correcting the causes of low power output of the realigned gate FET's, and (2) obtaining the information required to make a decision on direct implanation versus buffer layer growth and subsequent implantation.

1. NEW EQUIPMENT STATUS

1.1 WAFER ALIGNMENT SYSTEM (KASPER 2001-HRZ)

A Kasper 2001-HRZ high resolution mask aligner was received during the first six months of this program and has been used to make our realigned gate power FET's. We have recently installed an improved illuminator with better collimation to enhance the visibility of the micron-sized FET details during alignment. There is still a fault in the mainbody casting of the instrument which causes the optical microscope to defocus between alignment and exposure steps. This is an inconvenience, but does not interfere with the operation of the machine. A new casting is expected in October. The resolution of geometries at one micron has been achieved with no trouble.

1.2 LFE PLASMA NITRIDE DEPOSITION SYSTEM

The LFE low temperature nitride deposition system provides a plasma-enhanced reaction of silane and nitrogen to produce uniform films of Si_3N_4 at a low temperature. The system, as delivered, had many errors including defective logic for operating the value sequences and a 3-way gas valve that was installed backwards. These items have been corrected. A more serious problem is the presence of leaks in the piping of the system that allows oxygen to contaminate the nitride films. Many of these leaks have been located and cured, and a new baseplate for the vacuum jar is being machined to eliminate others. No suitable Si_3N_4 capping layers for GaAs have been produced by this machine as yet.

1.3 VARIAN/EXTRION 400 kV ION IMPLANTER

The Varian/Extrion 400 kV Ion Implanter provides sufficient energy for the deep implants required for power FET channels. The essential services (water, gas, electric) have been connected and the system is presently being

leak-checked. We expect an ion beam by the end of September and full operation in October.

1.4 $AsCl_3$ VAPOR PHASE EPITAXIAL REACTOR

A vapor phase epitaxial reactor for the growth of high purity GaAs buffer layers is nearing completion. The furnace tube, oven with sodium heat-pipe, mass-flow controllers, and piping are all completed. The system is now being leak tested and the control panel for the solenoid valves must be wired in. The first runs on this furnace should start in early October.

2. MATERIALS PROCESSING

2.1 GaAs SUBSTRATE MATERIAL

Polished semi-insulating GaAs (100) surface wafers for buffer layer epitaxy and ion implantation have been obtained from boat grown and (LEC) Czochralski grown ingots. Boat grown wafers were obtained from Crystal Specialities (65 in^2), Morgan Semiconductor (100 in^2) and Sumitomo Electric (70 in^2) (Japan). Czochralski grown wafers were obtained from Metals Research (70 in^2) (England). These wafers were purchased polished, the boat grown material polished using the Sodium hypochlorite technique while the LEC wafers were polished using bromine-methanol.

Substrate wafers having a minimum resistivity of 10^8 ohm-cm were qualified for epitaxy and for direct ion implantation by two techniques shown in figure 1. Wafers were considered qualified for epitaxy providing the resistivity did not degrade after heat treatment at 750°C for 2 hours in hydrogen. Wafers for ion implantation were qualified by heat treatment of a Si_3N_4 encapsulated wafer at 850°C for 15 minutes in H_2. The resistivity prior and after heat treatment has been measured using a 4-point probe and strong light on the sample as depicted in figure 1. More recently however, resistivities have been evaluated using the Van der Pauw Hall technique.

Figure 2 shows substrate supply and qualification results. Sample wafers from the front and tail ends of boat grown ingots from Crystal Specialities and Morgan Semiconductor were evaluated prior to ingot acceptance. Ingot CS-3828 was acceptable for epitaxy, but only the back half of the ingot was suitable for I^2. Of two MS ingots, a heavily chromim doped MS 9-5 was suitable for epitaxy, but only the front half for I^2. A second light chromim doped ingot MS 11-5 was unsuitable for either epitaxy or I^2. Wafers from

- Substrates as Received 10^4 ohm-cm
  Qualified if No Degradation in Resistivity After Heat Treatment

Epitaxy	Ion-Implant
750°C	850°C
H_2	Si_3N_4 Encapsulated
2 Hr	H_2 15 Min

- Evaluation Procedure

  4-Point Probe with Strong Light

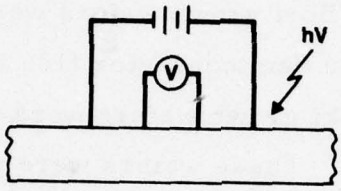

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Figure 1. Qualification Tests for VPE and Ion Implantation of GaAs

Sumitomo were prequalified type III, reported to show no thermal conversion after a 780°C heat treatment using the 4-point probe evaluation procedure. Wafers from MR were prequalified by heat treatment at 750°C under an arsine atmosphere. All MR wafers evaluated by Westinghouse were qualified for epitaxy and I^2. Wafer size varied from 9 cm^2 for boat grown material to 19 cm^2 LEC wafers. Forty-five square centimeter wafers are the target for large LEC grown material in the future.

Three hundred-square inches of LEC grown substrate material have been ordered from MR for future use. These wafers will be received unpolished, in order that Westinghouse can control the surface finish using a bromine-methanol etch. Additional ingots of boat grown material from CS and MS will be evaluated as ingots become available. Wafers of Laser Diode material, from Westinghouse in stock supplies, have been evaluated for epitaxy. About half of the ingots tested have qualified.

Suppliers	Ingot	Qualification		Cost $ Per In.^{2}
		EPI	Ion-Implant	
Boat Grown				
Laser Diode	Several	About Half		18
Crystal Specialties	3828	✓	Back Only	18
Morgan Semiconductor	9-5	✓	Front Only	18
	11-5	X	X	
Sumitomo Electric	Ex-78-029	✓		41
LEC Grown				
Metals Research	Test	✓	✓	27

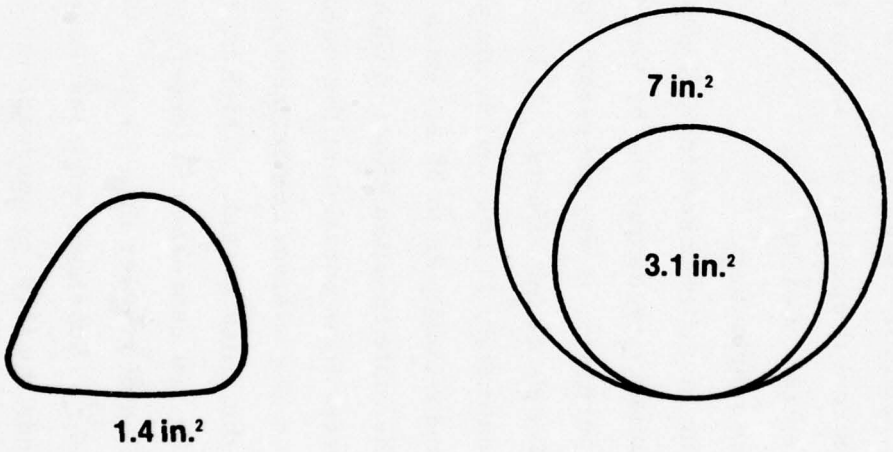

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Figure 2. Sources of GaAs Wafer Supply and Qualification Results

2.2 BUFFER GROWTH

Undoped epitaxial "buffer" layers for ion implantation have been grown on semi-insulating substrates by $AsCL_3$ vapor phase epitaxy at Westinghouse and by liquid phase epitaxy at Cornell.

2.2.1 VPE Material

Eightly VPE epitaxial layer runs have been made this period, with approximately 25 wafers used for ion implantation experiments. The other wafers were used for evaluation of growth parameters and electrical properties. The target properties are a 5 μm thick epitaxial layer, with a net carrier concentration of 10^{14} cm^{-3} or less, and a smooth surface morphology for device fabrication.

The impurity concentration was evaluated by the Schottky barrier capacitance technique and by Van der Pauw Hall measurements. For evaluation purposes, it was necessary to grow layers thicker than 5 μm to avoid surface depletion effects. At N = 1 x 10^{13} the Schottky depletion depth is approximately 11 μm, and 35 μm at 1 x 10^{12}, therefore, to evaluate concentrationand mobility 20 to 35 μm thick epitaxial layers were grown and evaluated.

The mole fraction effect in GaAs is well known[1], and is commonly used to suppress incorporation of the donor silicon into the epitaxial grown layer. Silicon is a system contaminant in VPE GaAs due to the reaction of gallium with the silica vessel. A high mole fraction of $AsCL_3$ increases the HCL content and represses Si incorporation. Buffer layers are grown with a mole fraction of greater than 5 x 10^{-3} to obtain carrier concentrations below 1 x 10^{15}. Substrate surfaces were misorientated 2 to 4 degrees off the (100) towards the (110) to decrease the occurance of hillock growth as a consequence of the high mole fraction.

The Hall mobility at 78°K, a commonly used measure of purity, ranged from 50,000 to 89,000 cm^2/volt-sec in the thickly grown n-type layers. The carrier freeze-out ratio's ranged from 0.99 to 1.16 and shows good control of the oxygen content in the epitaxial layers. Net carrier concentrations

ranged from 7×10^{12} to 9×10^{14} cm^{-3}, which is within the target range for ion implantation.

A problem which has occured is the growth of p-type undoped epitaxial layers. These layers are in general compensated and of high resistivity making measurements difficult. The source of the p-type impurity is unknown, although considerable effort has been undertaken to determine this.

a. One would suspect that the residual silicon would render the buffer layer n-type, and that changes in mole fraction would change the net carrier concentration. This, however, has not been shown to occur.

b. When the p-type growth was first observed, the epitaxial growth reactor was dismantled and throughly cleaned, and new sources of $AsCL_3$ and gallium used. This did not resolve the problem.

c. Substrate wafers from five different suppliers also did not change the p-type result.

d. A separate VPE reactor was used to grow buffer layer GaAs. The same p-type results were obtained, therefore, effectively eliminating local contamination as the source of high resistivity p-type epitaxy, and fixing the problem on the source batch of either $AsCL_3$ or gallium. Accordingly, a different lot of $AsCL_3$ was procured from Mining and Chemical Products Company, and a different lot of high grade special gallium obtained from Alusuisse. The new $AsCL_3$ was used in one reactor, the new gallium in the second reactor. While the results are still being evaluated at this point, a number of n-type high mobility layers were grown using the new batch of $AsCL_3$.

One of the p-type layers which was grown 34 μm in thickness was analyzed using a conventional Hall bar.[2] The net carrier concentration and mobility as a function of temperature are shown in figures 3 and 4. The net carrier concentration $N_A - N_D = 1.68 \times 10^{14}$ cm^{-3}, while $N_A = 2.03 \times 10^{14}$ cm^{-3} and $N_D = 3.46 \times 10^{13}$ cm^{-3} at 298°K. The linear region of figure 3 shows an activation energy of 0.34 eV. At this level, Fe and Ni are possible candidates as impurities.[3] Samples of the gallium lot, and of the gallium source used in growth of this layer were submitted for chemical analysis. At present Ni has

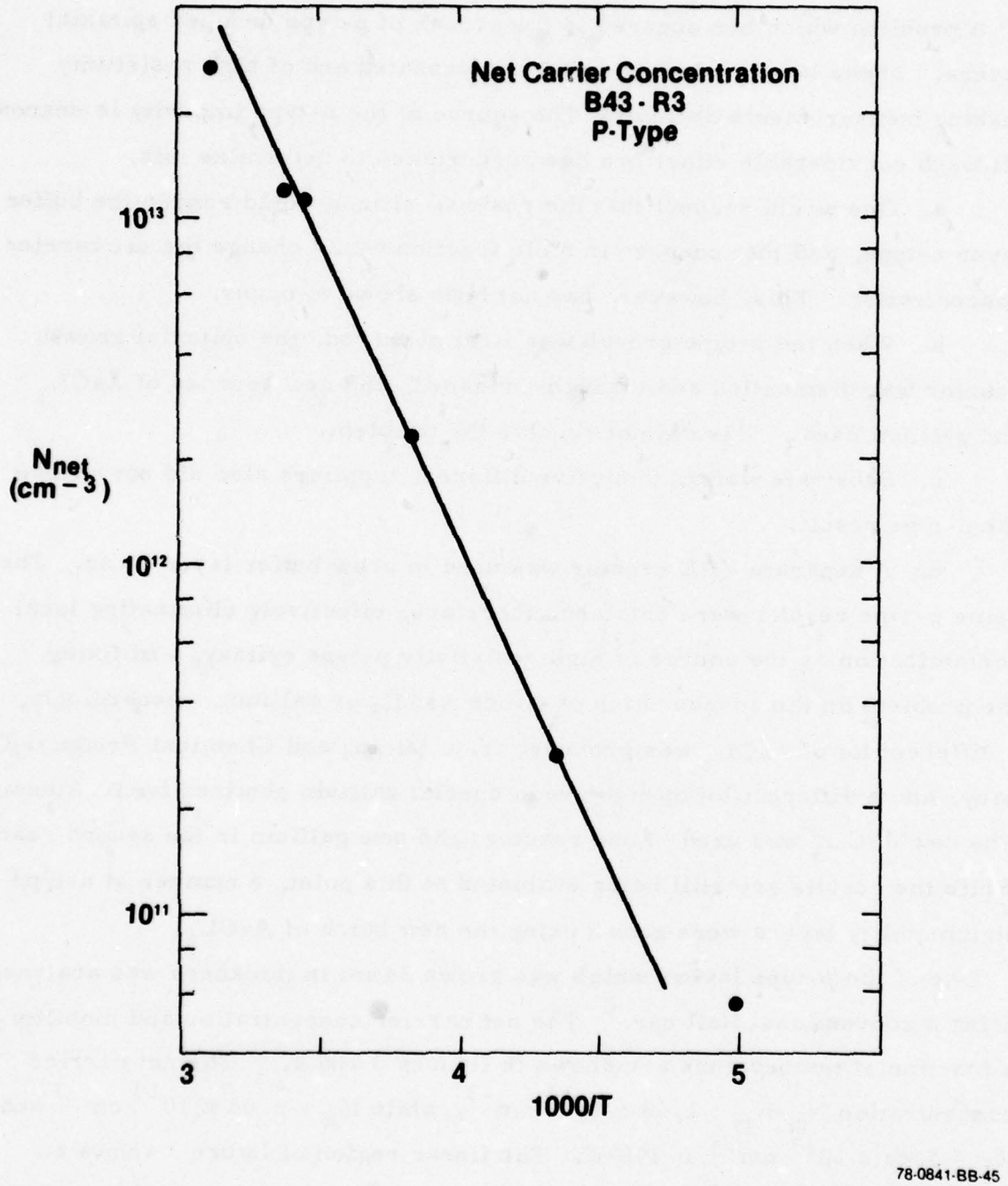


Figure 3. Net Carrier Concentration of P-Type GaAs Buffer versus Inverse Temperature

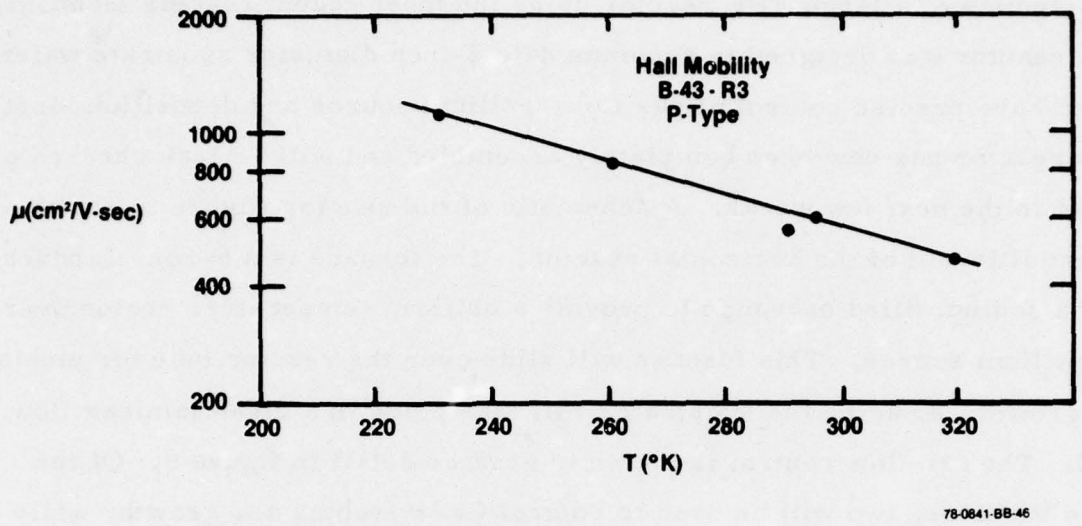


Figure 4. Hall Mobility of P-Type GaAs Buffer Layer versus Temperature

been seen at the 5 to 10 ppm level in both the pure gallium and source gallium, by emission and atomic absorption spectroscopy. This result has yet to be confirmed and quantified. No analysis of the $AsCL_3$ has yet been undertaken. Analysis to identify the source of the p-type growth will be continued.

It is of interest to note the relatively high mobility of this p-type sample shown as a function of temperature in figure 4, with a room temperature value of 580 cm^2/VT-sec.

The surface morphology, uniformity of the epitaxial layer, and repeatability of the layer thickness from run to run are important in device processing. Twelve consecutive runs were made with an average 5.0 μm thickness and deviation of 0.53 μm, where the run parameters were kept constant. Six runs were also made under identical conditions to grow thicker layers for evaluation, with the result a 21.7 μm average thickness and a 1.5 μm average deviation. Growth parameters have been adjusted to give smooth bright surface morphologies suitable for device fabrication.

2.2.2 New VPE Reactor Status

Prior to beginning of this project, Westinghouse undertook the design and construction of a large VPE reactor using the most recent reactor technology. This reactor was designed to accommodate 3-inch diameter substrate wafers and to have precise control of gas flow, gallium source and deposition kinetics. This reactor has now been completely assembled and will be leak checked and tested in the next few weeks. A schematic of the reactor (figure 5) shows the essential layout of the horizontal reactor. The furnace is a 6-zone Lindberg, with a sodium filled heat pipe to provide a uniform temperature region over the gallium source. This furnace will slide over the reactor tube for etching and growth. Loading the substrates will take place in a clean laminar flow hood. The gas flow control is shown in greater detail in figure 6. Of the three bubblers, two will be used to control GaAs etching and growth, while the 3rd is available for either $AsCL_3$ or a liquid dopant. The bubblers are thermostated to control T within less than 0.5°C. The gases, H_2, AsH_z and the doping gas H_2S are controlled with tylan mass flow controllers with a dilution scheme for the H_2S source. Sequence control is presently manual operation of teflon solenoid values, but computer control can be conveniently added. The H_2 source is pd purified and all gases filtered and pressure controlled. The reactor tube can be a double source, with a pure gallium and a doped gallium (or GaAs) source as desired. This reactor then will be capable of multilayer epitaxy, as well as the controlled growth of undoped or semi-insulating butter layers.

2.2.3 LPE Buffer Growth (Work Performed at Cornell Univerity)

Due to the uncertainty of the availability of high quality Semi-insulating GaAs substrates, it is necessary to have in hand several buffer layer options. The LPE technique offers a technology capable of producing Semi-insulating buffer layers suitable for ion implantation. The approach being taken is to reduce the residual or "background" impurity concentration as much as possible, and to investigate the growth and properties of the critical Cr-doped LPE buffer layers.

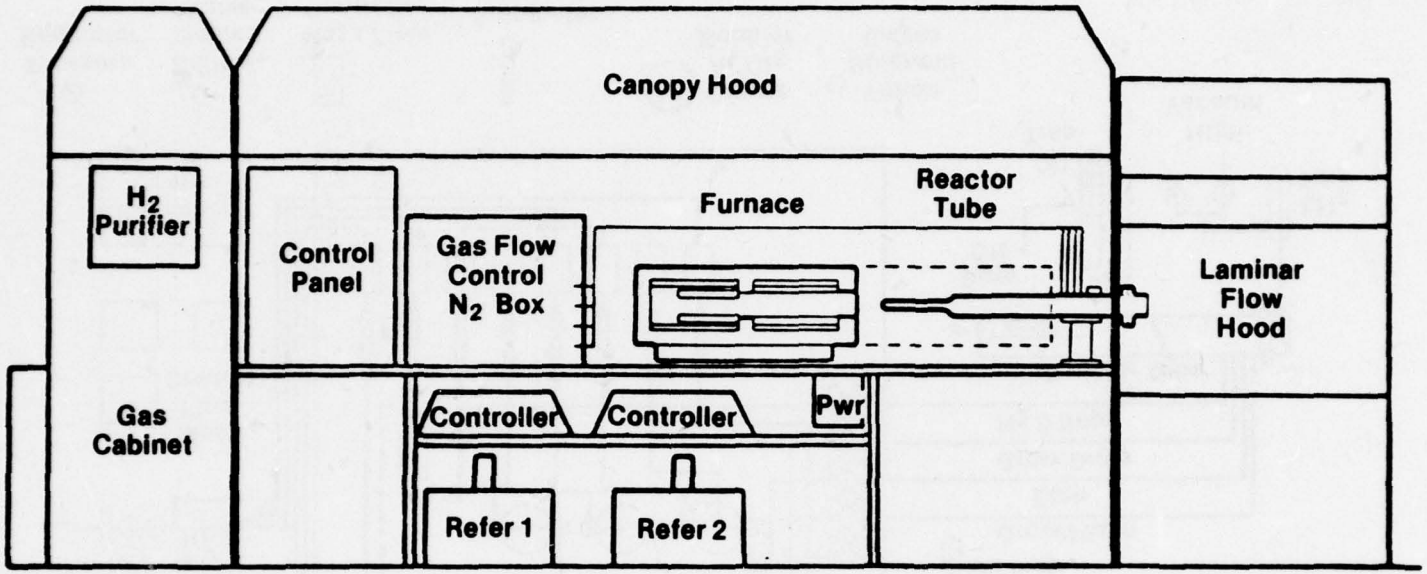


Figure 5. Physical Layout of A_SCL_3 GaAs VPE Reactor System

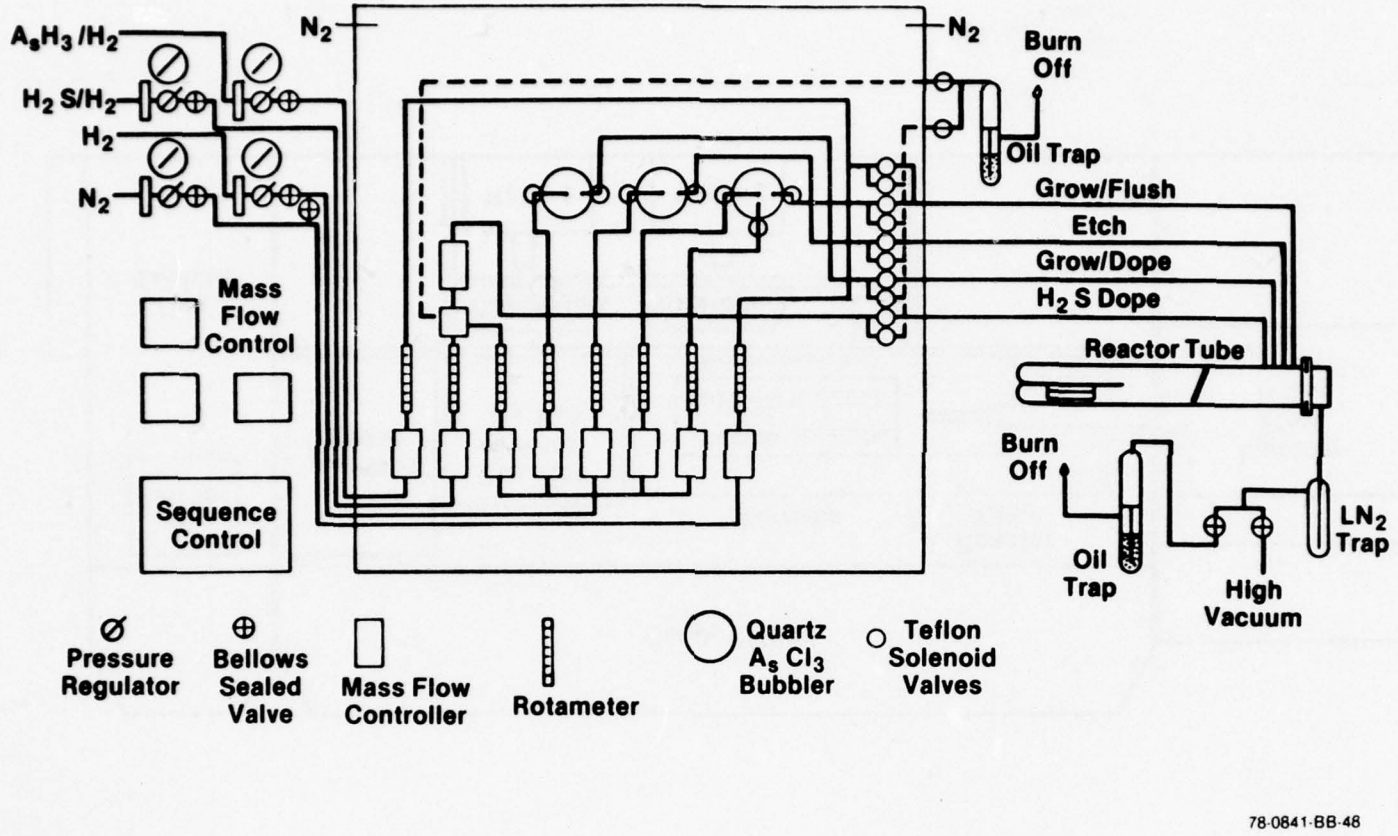


Figure 6. Gas Handling System for A_SCL_3 VPE Reactor

Wafers have been analyzed by both Hall measurements and deep level transient spectroscopy (DLTS), as well as conventional C-V profiling.

The reproducible background impurity concentration in LPE GaAs is now around 1×10^{14} net, and low-to-mid 10^{14} total ionized impurities per cm^3. Such background concentrations appear to result from the equilibrium dissociation reactions for SiO_2 in the presence of hydrogen, carbon, and gallium and therefore, represent an asymptotic chemical limit which will be approached by "clean" LPE systems, if baked sufficiently initially, and following exposure of the graphite crucible to air, as was described by Morkoc and Eastman[4] in 1976. A recent and significant advance resulting from the present effort has been the successful growth of high purity layers without the need for prolonged baking between runs. This was accomplished in a boat designed so that during the substrate reload operation, there is no need to disturb or break up the GaAs crust surrounding the melt. The intact crust prevents oxidation of the Ga in the melt resulting from exposure to air or to gases which desorb from the graphite crucible during furnace warmup. Also in progress are experiments to determine the effect of various surface treatments on the gas desorption from the graphite occurring during warmup after the crucible has been exposed to air for loading. Both pyrolytic graphite coating and a new surface impregnation process available from Ultra Carbon are being investigated. These treatments both appear to reduce the porosity of the graphite near the surface and may decrease the quantity of O_2 absorbed from the air, without sacrificing the basic purity or changing the elemental composition of the crucible material.

In the current experiments, layers were grown within one hour of the time the reactor reached growth temperature. Purity achieved was comparable to previous runs having 24-hour bake periods. Purity has not been found to be adversely affected by either of the coating treatments.

It is anticipated that reduced baking periods should not only improve the cycle time of the reactor but also reduce surface degradation of substrates.

Reduced outgassing of O_2 from the graphite should not only improve purity but also alleviate surface wetting problems. Further, it should be possible to do more definitive studies on the out-diffusion of deep acceptors from the substrate into layers grown by LPE since now purity can be maintained down to very short prebake times. Previously, most of the out-diffusing deep acceptors were either lost in the long purification prebake, or masked by high impurity concentrations following short bake out. Densification or coating of the graphite surfaces should also reduce the generation of graphite dust by the moving parts in sliding boats.

In the buffer layer Cr doping experiments, melt prebake requirements for both removal of Cr included impurities and subsequent re-equilibration of background silicon impurities have been established. Cr doping has been investigated at two growth temperatures. From Hall measurements the distribution coefficient of Cr and GaAs has been estimated to be about 5.8×10^{-7} at 700°C, and 1.8×10^{-6} at 780°C. Deep level transient spectroscopy has also been employed in an effort to corroborate the Hall measurements. At present, the agreement is within a factor of 2, with the DLTS showing lower Cr concentrations. The DLTS of Cr levels, however, presents some special difficulties which are currently under further investigation on a separate program, and it is hoped that a completely consistent picture will emerge. Semi-insulating layers have now been achieved at both 700°C and 780°C growth temperatures. At 780°C, a higher background can be compensated due to the higher distribution coefficient. Experiments are in progress to determine the stability of Cr doped epi layers against conversion during subsequent processing at elevated temperatures, especially in the case of annealing ion-implanted layers.

2.3 ION IMPLANTATION

2.3.1 Encapsulation

Westinghouse R&D is currently employing "pyrolytic" SiN for encapsulation of ion implanted GaAs. The "pyrolytic" system is similar to that described by J. P. Donnelly of Lincoln Laboratories. Samples are rapidly heated to 680°C

and 300 to 500 Å of SiN is deposited at rates of 200 to 300 Å/minute, 2000 Å of pyrolytic SiO_2 is then deposited on both the front and back surfaces. This encapsulant retains its cosmetic integrity to 950°C and 850°C for semi-insulating and VPE buffer substrates respectively; the lower limiting temperature in the buffer case is associated with failure at growth hillock. The largest sample that can be capped in this system is 1-1/8 by 5/8-inch as a result of both the temperature profile of the strip heater and the mixing profile of the reactant gases. Although 80 percent yield can be achieved with the system, the SiN layers are presumed not to be oxygen free and this results in Ga out diffusion and anomalous surface activity. This activity is confined to the first 500 to 1000 Å for deep Si implants.

The magnitude of this anomalous activity is examined in the third step of the current Westinghouse qualification procedure: (1) 750°C anneal (H_2) and 4-point probe, (2) 850°C anneal (encapsulated) and 4-point probe, and (3) $5 \times 10^{12}/cm^2$ 300 kV implant - 850°C anneal (encapsulated) and C-V profile. Although an early shipment of GaAs (cr) from Sumitomo Electric Industries (SEI) passed these tests, subsequent shipments have all failed part 3. Selected Morgan ingots and all Metals Research LEC ingots pass these tests and are currently being used for direct implants. All VPE buffer layers have passed these tests.

An LFE model PND-301/MQ plasma enhanced SiN deposition system has been installed at the R&D center. This system is capable of encapsulating 3 inch wafers and includes mass flow controllers and a capacitance manometer for reactant gas control. As delivered, the system also included several vacuum leaks, logic faults, and gas manifold assembly errors. The system is currently being rebuilt to meet the requirements of GaAs encapsulation. Initial results indicate that deposition at 340°C and 100W RF power using 3 cm^3/min (standard cubic cm per minute) N_2 and 36 cm^3/min of 1.5 percent SiH_4 in Ar yield the best encapsulant uniformity. Prof. Benjamin Streetman of the University of Illinois has been used as a consultant to assist in bringing

the plasma nitride system on line. He has demonstrated that Westinghouse wafers capped in a proven plasma system show little or no anomalous surface activity.

2.3.2 Sulfur Implantation

Figure 7 shows Miller capacitance n(x) vs x profiles taken from the test pattern on a processed, sulfur implanted wafer. The substrate was SEI material, implanted with 5×10^{12} S^{++} at 150 kV, and annealed at 860°C for 30 minutes. The n(x) profile shows characteristics of sulfur in and out diffusion. Somewhat better uniformity in depth and concentration is achieved by buffer implants, but these variations are, in general, typical. "Fat" FET mobility calculations yield values of only 3600 to 3650 $cm^2/V\text{-sec}$.

Differential Van der Pauw measurements are in progress in order to determine mobility profiles. Figure 8 shows the profile obtained from a SEI slice that failed qualification test[3]. The specimen was implanted with $3.5 \times 10^{12}/cm^2$ S^{++} at 150 kV and annealed for 60 minutes at 860°C. Stripping was performed by anodization in critric acid and ethylene glycol. Discrete data points were obtained by difference calculations and the solid curves by curve fitting to σ_s and $R_s \sigma_s^2$.

Sulfur implantation is not considered to be a viable technique for channel doping as a result of the out-diffusion profile, relatively poor profile control, and low mobility. It is retained as a reference standard, for qualification testing, and possibly for n^+ source and drain implantations. It is not expected that substitution of plasma SiN encapsulation will alter this judgement.

2.3.3 Silicon Implantation

Figure 9 shows Miller capacitance n(x) vs x profiles taken from the test pattern on a processed, silicon implanted VPE buffer layer. The sample was implanted to a dose of 5.5×10^{12} Si^{++} at 200 kV, annealed at 830°C for 15 minutes, and etched back 2000 Å to adjust the pinch off voltage. The curves exhibit good concentration and deep profile control. The deep standard deviation is 960 Å ±30 Å, and the shallow standard deviation measured before thinning is 1400 Å ±200 Å (R_m values for 300, 350, and 400 kV Si

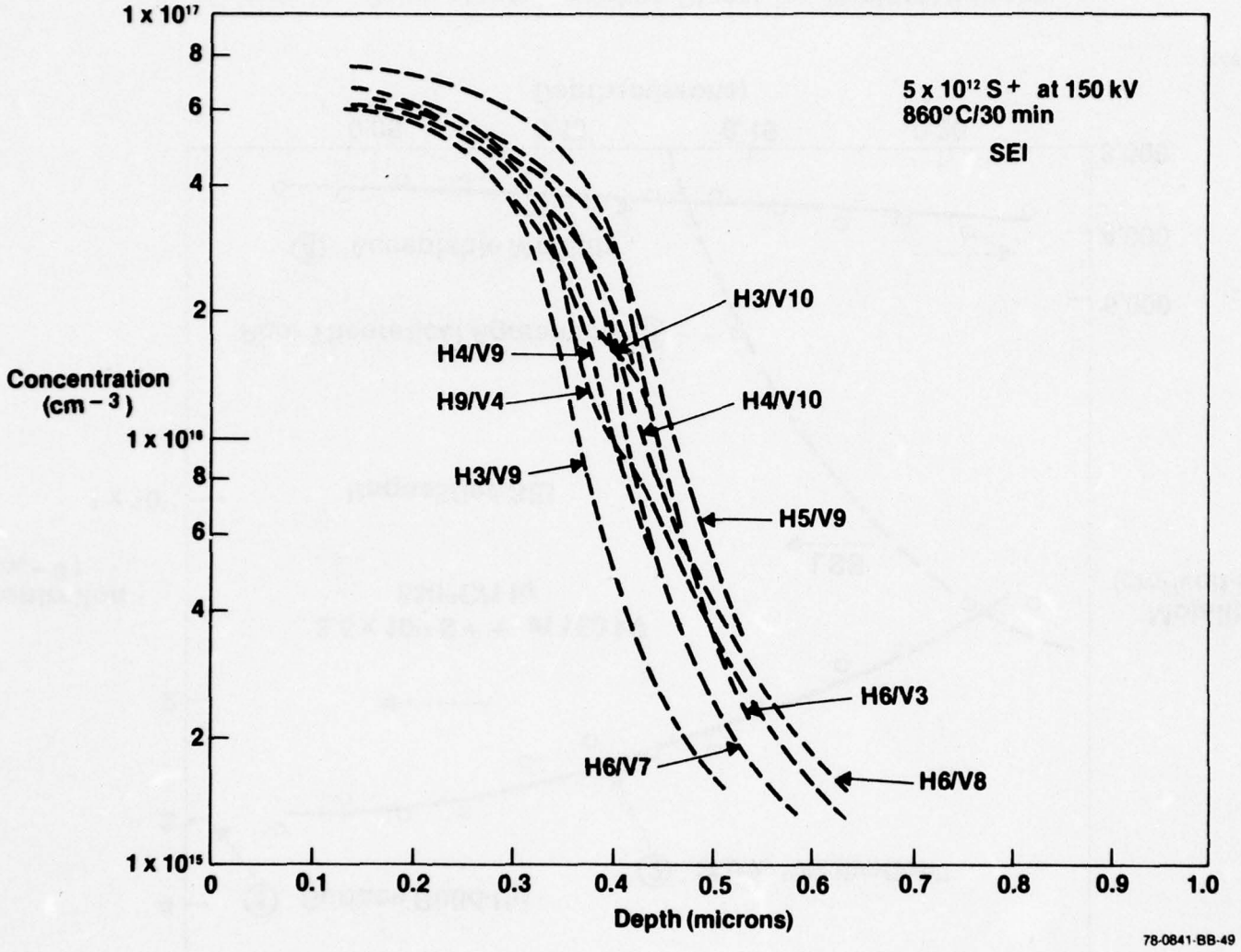


Figure 7. Direct Sulphur Implantation into Qualified SEI Substrate

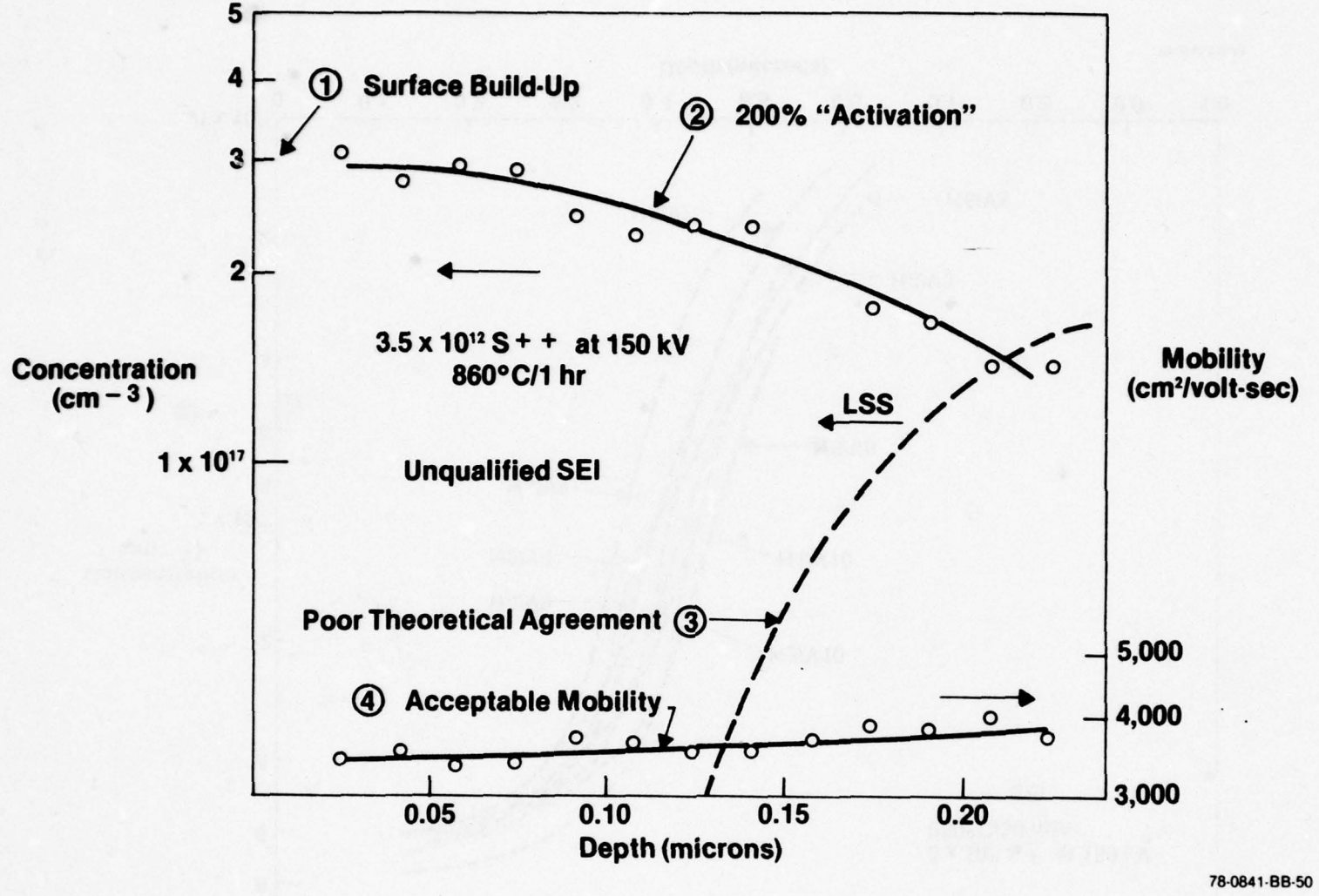


Figure 8. Prior Status: Sulphur Direct Ion Implantation into Unqualified Sumitomo Substrate

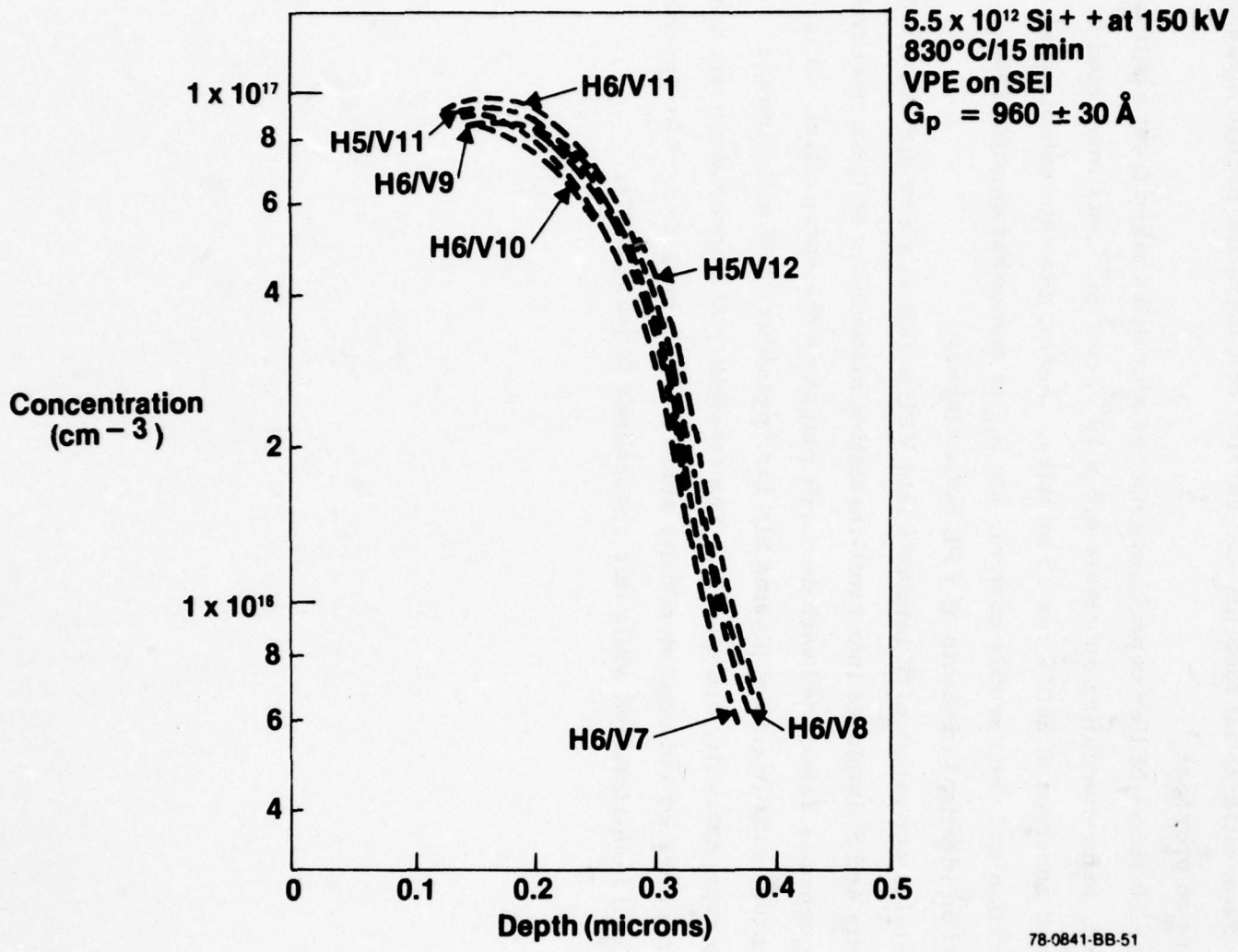


Figure 9. Channel Profile Si^{++} VPE Buffer - GaAs Showing Excellent Wafer Umformity in Dept of Peak and Rolloff - σ_p = 960 Å/±30A (7 Samples)

implants are 2900, 3100, and 3500 ±100 Å respectively). "Fat" FET drift mobility measurements made on these test chips yield 4400 cm^2/volt-sec. Van der Peuw differential mobility and carrier concentration profile measurements are in progress.

Figure 10 shows Miller capacitance n(x) vs x profiles taken from a silicon implanted, semi-insulating substrate 4.5 x $10^{12}/cm^2$ Si^{++} was implanted at 150 kV and annealed at 860°C for 15 minutes. Again, the data exhibit good concentration and deep profile control, but R_m is somewhat smaller than observed on identical implants of VPE buffer layers.

Controlled activation of Si implants into VPE buffer is more difficult than S implants and Si implants into semi-insulating material is still move difficult. This sequence is associated with demands placed on the encapsulant. It is expected that substitution of plasma SiN for "pyrolytic" SiN will improve both cap reproducibility and quality. The feasibility of improved quality has been demonstrated and reproducibility studies are in progress. The "pyrolytic" facility will be maintained while this changeover is being made.

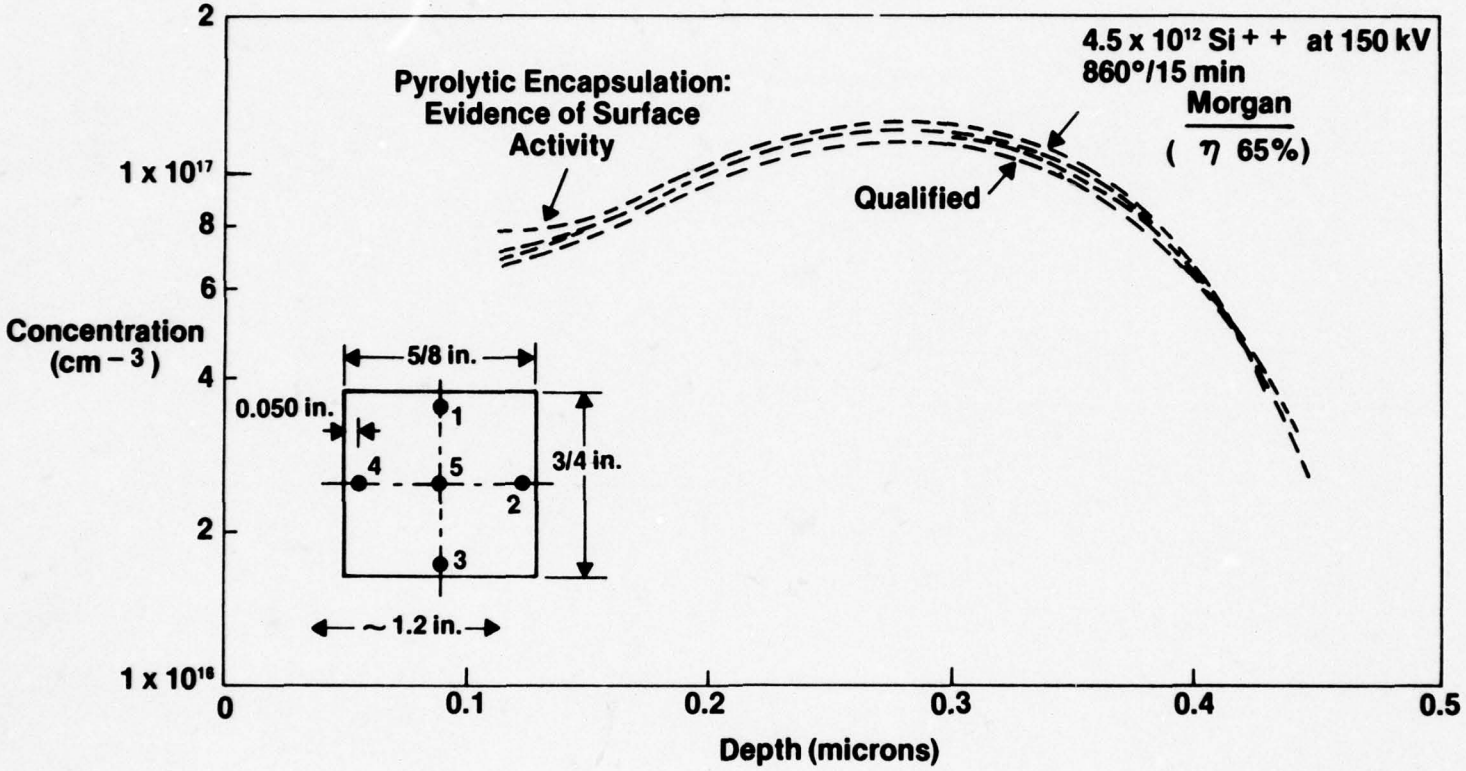


Figure 10. Comparison of Qualified vs Unqualified Substrates for Direct Implantation of Si^{++} into GaAs

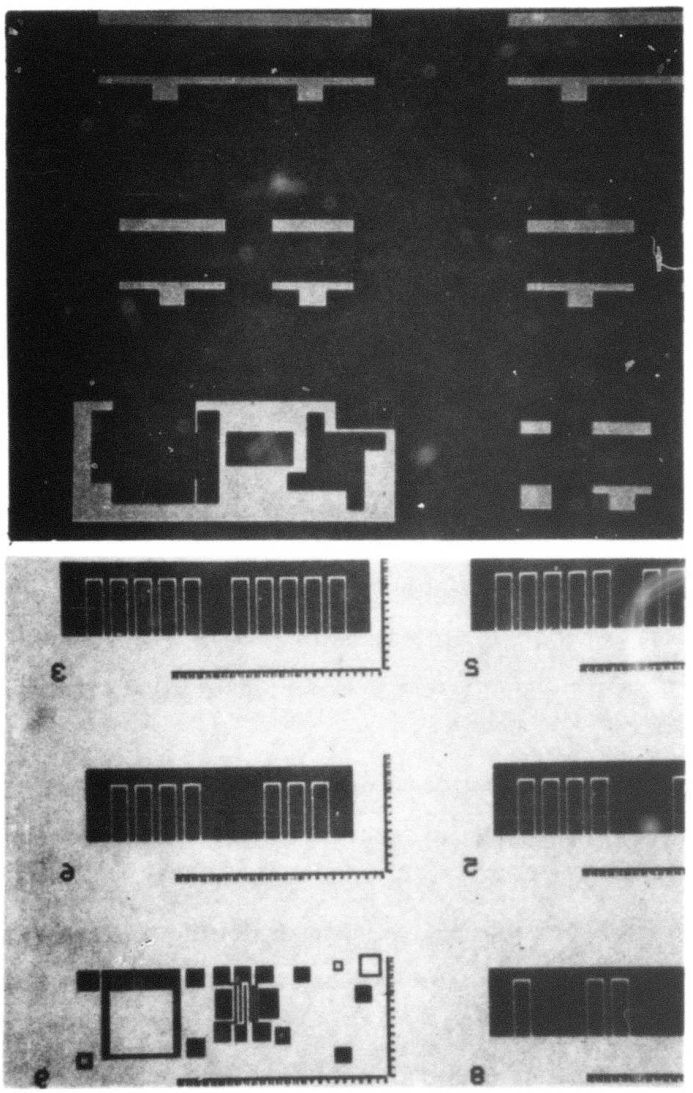
3. FET RESULTS

During the first six months of this contract Westinghouse has fabricated both self-aligned gate and re-aligned gate GaAs FET's on sulfur and silicon ion implanted wafers. The best RF results have been obtained from the re-aligned gate devices which show up to 9 dB small signal gain at 8 GHz from a 900 μm periphery transistor.

3.1 SELF-ALIGNED GATE DEVICES

Since the goal of this program is the integration of a 3-stage amplifier, the mask set to be used for both self-aligned and re-aligned includes devices with five different peripheries from 300 μm to 3000 μm. This will allow complete characterization of each device size likely to be used in the final amplifier. The basic design rules for the FET's include a 1 μm long gate with 150 μm wide individual gate fingers. The source-drain spacing is 4 μm. The 3,000 μm device is conservatively expected to give 2W output power.

The two masks needed for the self aligned device fabrication are shown in figure 11. The isolation mask is shown in figure 11a while figure 11b shows the drain-source oxide pattern. No separate gate mask is needed with the self-aligned approach. Not all devices are visible in these pictures, but the 900 μm and 1200 μm devices are completely visible as well as the test pattern. An overall pattern of three 3000 μm, three 1200 μm, five 900 μm, two 600 μm and two 300 μm devices plus the test pattern is stepped and repeated across the masks. The test pattern contains structure for measuring $N_D(X)$, contact resistance, Hall mobility, drift mobility, selective implant isolation and gate metallization resistance.



(a)
Isolation Mask

(b)
Oxide Mask

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Figure 11. Isolation and Oxide Masks for Self-Aligned Gate Power FET's

A closeup of one of the ohmic contact masks is shown in figure 12. This illustrates the chip identification by row and column used to permit mapping of device variations across a wafer after fabrication. The particular pattern shown is row 5, column 8.

Four slices of self-aligned gate FET's have been processed. One slice was merely to check out the new mask set. Three slices of working devices were successfully processed on ion implanted wafers.

1 slice - S^{++} implant - no buffer - Westinghouse No. 15A

2 slices - Si^{++} implant - VPE buffer - Westinghouse No. 18A, No. 18B

The Si^{++} profiles were similar to those shown in our prior Status Report and were taken from the same batch of implanted wafers. The S^{++} profile showed higher concentration at the surface and a less rapid drop into the semi-insulating substrate.

The I-V characteristics of typical 300 μm periphery devices from a Si^{++} slice and the S^{++} slice are shown in figure 13. In both cases, the knee voltage is 2V or less and the device exhibits complete pinch-off up to 9V

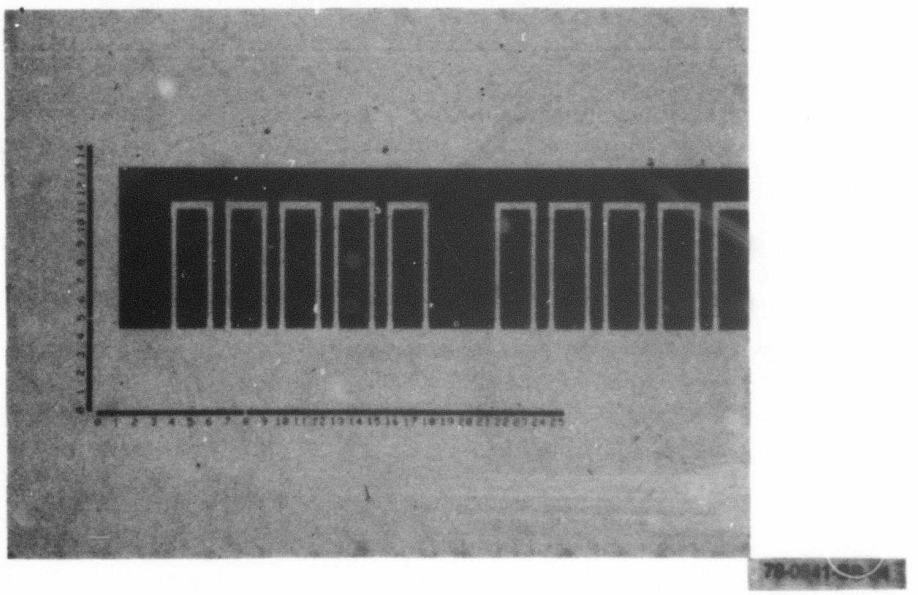
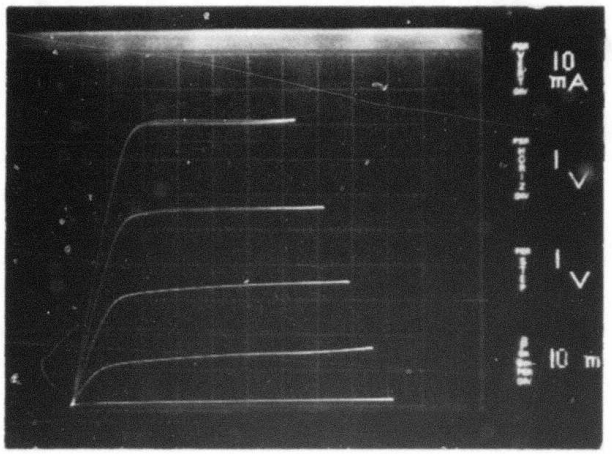
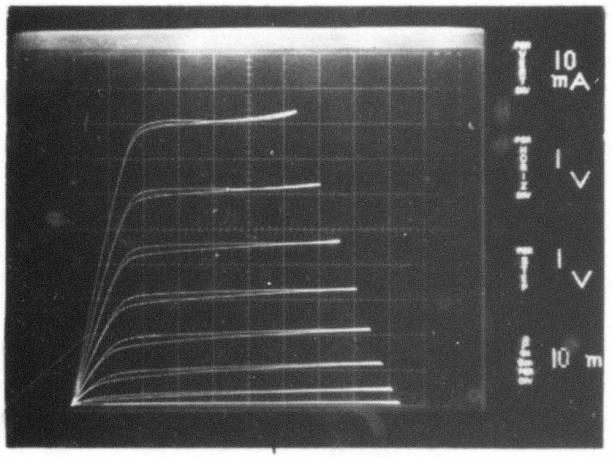


Figure 12. Closeup of Source-Drain Mask Showing Integral Row-Column Numbering (Device Shown in Row 5, Column 8)



(a) I-V Characteristics of Si^{++} Implanted FET



(b) I-V Characteristics of S^{++} Implanted FET

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Figure 13. I-V Characteristics of Si^{++} Implanted FET

drain voltage. The silicon implanted device shows superior gm (24 mmho vs 20 mmho) and less looping. FET's from the silicon wafers show drain-source breakdown voltages of 14 to 16V at low currents. In general, the silicon devices are superior and exhibit somewhat better gain.

The device uniformity in these wafers was degraded by nonuniform plating of the source-drain overhangs. This was caused by mask problems which have since been corrected. All devices have been thinned to 75 to 100 μm before mounting to provide adequate heatsinking. Although the self-aligned gate devices show good dc performance, the RF results have been disappointing. The small signal S-parameters of a three-drain Si implanted device (900 μm gate width) were measured from 6 to 10 GHz. The large signal performance was measured at 8 GHz. The small signal gain measured at 8 GHz was 2.8 dB, comparing favorably to the maximum available gain of 2.92 dB calculated from the S-parameter data. At an output power of +21.3 dBm the gain dropped to 1.7 dB, with a drain voltage of 6 volts and drain current at 80 mA. This shows a drain efficiency of 28 percent and a power added efficiency of only 9.1 percent. Small signal measurements of several 300 μm devices have shown maximum available gains ranging from 3.0 to 8.5 dB at 6 GHz.

There are several problem areas in the self-aligned gate devices. One difficult area involves access to the active region of the device, i.e., the source-gate-drain region, for either visual inspection or further processing after the device has been completed. Due to the Au-plated metal overhangs above the source-gate and gate-drain spaces, gate lengths variations or the origin of shorted electrodes are hidden from view. To passivate or at least protect this region from contaminants or dirt is very difficult. The only possibility may be a low-pressure CVD layer of SiO_2, but it is not clear that even this will penetrate underneath the Au overhangs.

Further problems include the lack of a thick (>0.4 μm) gate metal and elimination of stray feedback capacitance. When 0.4 μm or more of total

gate metal thickness is used, the yield of working devices drop dramatically due to shorted gates. This phenomenon is not predicted by an examination of the presumed electrode spacings during the gate evaporation. The thinner metal results in higher input resistance losses. Also, due to the device topology used for the self-aligned gate fabrication, the gate-drain feedback capacitance is high.

3.2 RE-ALIGNED GATE DEVICES

To overcome some of the problems with the self-aligned gate devices, four wafers of the GaAs FET's with realigned gate structures have been fabricated. The wafers are:

- 20A Si^{++} into buffer
- 20B Si^{++} into buffer
- 20C Si^{++} into SI substrate
- 15B S^{++} into SI substrate
  O^{+} for isolation

The doping profiles of 20B and 20C were shown in figure 8. The run 15B wafer used an oxygen implant for isolation rather than mesa etching. No RF results are available as yet except on 20C.

The re-aligned gate devices utilized Au-Ge/Ni ohmic contacts and Cr/Pd/Au Schottky barriers. The fabrication sequence was straight forward.

- Isolation Etch
- SiO_2 Deposition
- Ohmic Contact Deposition
- Photolithographic Definition thru SiO_2
- Alloy
- Gate Definition through SiO_2
- Gate Evaporator and Rejection
- Thinning Back and Back Metallization

A photograph of a typical device just prior to the gate metal evaporation is shown in figure 14. The gate openings in the photoresist are clearly visible with the gate interconnection bus to the right side of the photo. The gate

length of the finished devices was just under one micron with a source-drain spacing of 3.5 microns. While the final tabulation of yield for these wafers has not been completed, the surface finish of the alloyed ohmic contacts was the sprimary factor limiting the number of usable devices.

The small-signal S-parameter measurements of the 20C devices have shown a lower series input resistance, lower reverse feedthrough, S_{12}, and larger S_{21} than previous self-aligned gate FET's. A typical set of S-parameters for a 900 μm periphery device from 2 GHz to 10 GHz is shown in figure 15. The observed gain at 8 GHz for devices from wafer 20C ranged from 7 dB to 9 dB.

One of the 600 μm periphery power FET's from wafer No. 20C has been power tested at 8 GHz using coaxial slug tuners and Hewlett Packard 436A digital power meters. The output power reached 200 mW at 4.3 dB gain and -2 dB gain compression. The drain efficiency was 25 percent and the power-added efficiency was 15 percent. The low drain efficiency may be caused by high series output resistance at the drain contact.

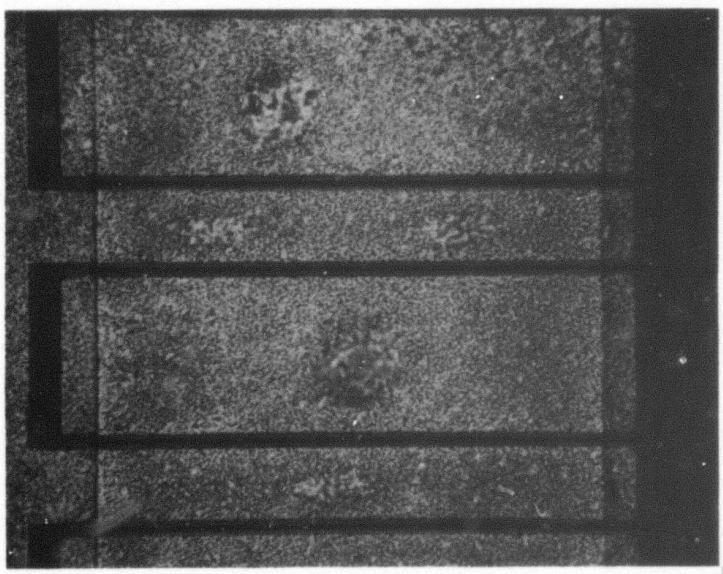


Figure 14. Micrograph of Realigned Gate FET Just Prior to Gate Metal Evaporation (Series 20 Device - Lg -1 μm, L_{SD} = 3.5 μm)

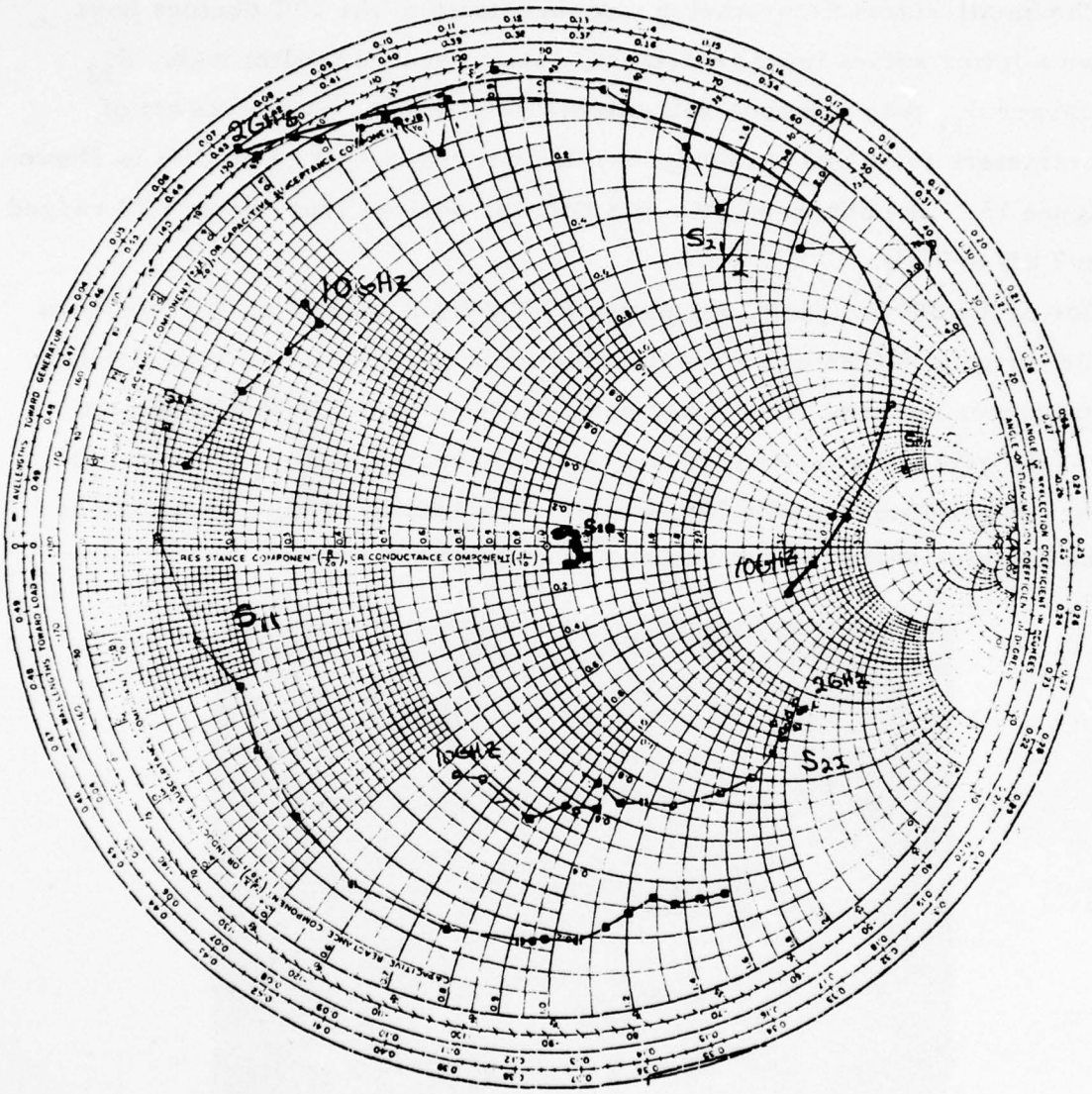


Figure 15. S-Parameters of 900 μm Periphery FET

3.3 HEAT SINKS FABRICATION

The problem of heat removal from the power FET's is a monolithic power IC can be solved by selective thinning of the GaAs under the active devices only. The Westinghouse approach is a 150 micron thick chip for rigidity which is thinned to 50 microns under the power FET's and plated with a 50 micron thick gold heat sink. In addition, by ion milling 50 micron deep holes from the top of this slice, the source metal of the FET can be grounded to the heat sink, providing a low inductance source interconnection.

The proposed procedure for fabricating these heat sinks and source interconnections is:

a. As the first processing step (before any FET's or circuit elements have been made) ion mill and etch 50 micron deep holes into the front surface (active layer side) of the GaAs wafer. These holes are positioned in the source pads of the power FET's of the finished chip.

b. During the metallization of the sources of the power FET's, the 50 micron deep holes will be coated with 5,000 to 10,000 Å of AuGe and Au.

c. After all the chip fabrication for the FET's and microwave circuitry has been finished on the active layer side of the slice, wax the slice active layer down to a quartz lapping block and bring the overall wafer thickness down to 150 microns.

d. Keeping the wafer waxed down, mask the back with photoresist, align a trough etching mask under the power FET's with an IR aligner, expose and develop. The troughs can then be etched 100 microns deep to catch the 50 micron deep metallized holes which were put in the sources of the power FET's in steps 1 and 2.

e. Evaporate Cr-Au and plate up 50 microns of Au in the thinned regions to carry the heat away from the FET's.

Most of these steps have now been carried out on bare GaAs test slices. The backs of test slices have been etched with the 100 micron deep troughs described in step (e) and plated with 50 microns of gold. No breakage or

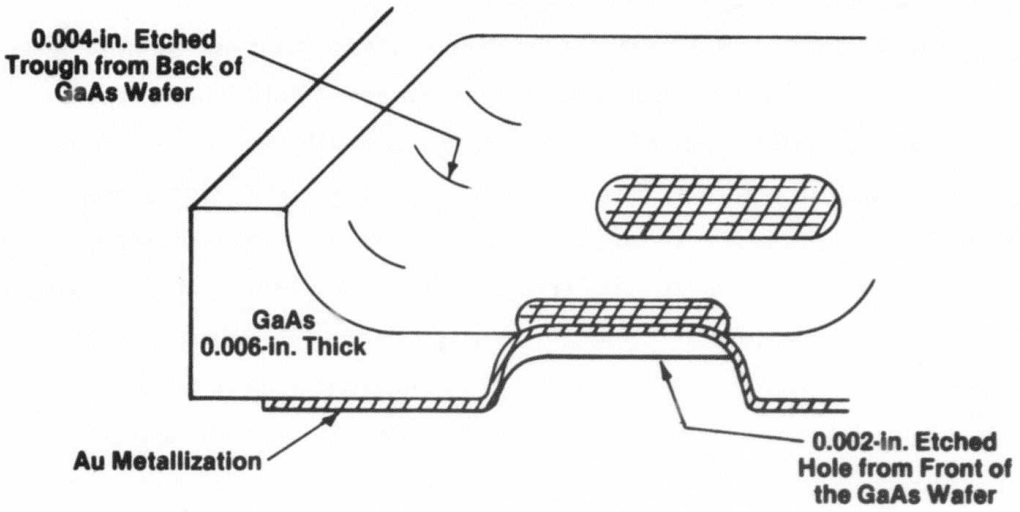
cracking has been observed in these pieces but thermal cycling will be used to further stress them.

The front source posts (steps (a) and (b)) have been fabricated on a bare slice, metallized and exposed in the bottom of the 100 micron deep trough etched from the back. A cross section of this is shown in figure 16. The 150 micron thick (0.006 in.) GaAs slice is upside down in the figure. The Au source metallization and etched source post appear on the bottom of the sketch while the etched trough comes down from the top and exposes the metal at the bottom of the source post. Also shown is a photograph of two source posts which have been exposed in the bottom of a 100 micron (0.004 in.) etched trough. This has been done on several pieces and there are no problems obtaining the required alignment of the masks on the bottom of the wafer using the IR aligner.

Several areas need further work to complete the selectively plated heat sink approach. First, the plated heat sinks must be thermally cycled and carefully examined for cracks due to stress or separation of the heat sink from the GaAs substrate. Then the process must be tried on a wafer of actual FET's to determine process compatibility and any effects on FET yield. Work on these steps is now underway.

3.4 DEVICE MODELLING

GaAs FET modules have been used by workers at Cornell University (Shur and Ku) to predict the expected drain breakdown voltage for power FET's and model the various small signal device parameters. The drain breakdown voltage for the power FET is assumed to be limited by the high field breakdown in the Gunn domain in the channel region between the gate and drain. This assumes that some means (either n^+ contacts or a recessed channel) has been used to eliminate breakdown due to current crowding at the drain contact. The model uses an analytic approach based on the accumulated charge in the Gunn domain remaining a small fraction of the total ionized charge density in the channel (~Nd). Using this approach, the predicted drain breakdown has been calculated for various doping densities. At 10^{17} cm^{-3} a



View of Au Posts in Bottom of
0.004-in. Deep Etched Trough in GaAs

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Figure 16. Hold Source Posts 0.002 in. Deep Exposed in 0.004 in. Deep Trough From Back of GaAs Slice

breakdown voltage of 80V should be possible. But the extent of the Gunn domain is also important and the gate-drain spacing must be able to accommodate it without the high fields reaching the drains contacts. At 10^{17} cm^{-3} this implies a gate-drain spacing of over 2 μm.

A small-signal FET model based on earlier devices has been used to predict the areas of the devices which need improvement. This has shown a higher C_{GD} and parasitic input resistance in the self-aligned gate devices which causes premature gain roll-off. In addition, the small signal model was used to predict the effect of doping variations on the s-parameters of an FET and the gain of a 5 to 10 GHz amplifier based on that device. Assuming that N_D was the only variant and that C_{GS} and gm were the primary device parameters affected by N_D. The 5 to 10 GHz amplifier showed ±1 dB maximum gain variation at the low frequencies when N_D was changed by ±20 percent from 10^{17} cm^{-3}. This work will be continued using the measured variation of s-parameters from wafers of fabricated devices.

4. LUMPED ELEMENTS

4.1 INTERDIGITAL CAPACITOR FABRICATION

At the start of this program it was planned to use overlay capacitors throughout the monolithic circuit. Dielectric thickness can be readily controlled and a wide range of capacitance values are obtainable. Their major drawback is that deposited SiO_2, which produces the highest Q's reported in the literature, needs to be densified at 700 to 1000° C in order to reduce RF losses. This densification step is not compatible with processed FET's and would have to be done simultaneously with the annealing step. This extra processing before annealing would complicate an already difficult step and has been rejected.

Interdigital capacitors were not considered because with gap widths of 25 μm a more, necessary for normal photolithographic processing with thick metallization, large areas would be required to obtain the desired capacitance values of 0.5 to 2.0 pf. Besides being wasteful of GaAs surface area, the capacitors would be electrically "large" at 10 GHz and would not behave as a truly lumped element. Two processing techniques have been developed which have produced 1 μm gaps in 2 μm thick gold, which gives high values of capacitance in a small area, and made interdigital capacitors useful in the monolithic circuit.

Interdigital capacitors were analyzed by Alley[5] who presented a simple lumped model that can be used when the physical size of the capacitor is small compared to a wavelength and a distributed model used when the size becomes significant fraction of a wavelength. At the frequencies of interest for this program, the capacitors used can be modeled accurately by the lumped equivalent circuit.

Three runs of interdigital capacitors were fabricated using ion milling. In this process, 2 μm of gold were deposited over a thin chromium film. A thick photoresist layer is spun on and the pattern is exposed using a well collimated light source. The photoresist covering what are to become the gaps is washed away and the substrate is exposed to the ion beam. Both the gold and the photoresist are eroded by the ions, with the photoresist eroding at a slower rate. When the gold is removed the chromium layer mills slowly and protects the underlying GaAs. Figure 17 shows 3 μm lines and 3 μm gaps ion milled through 2 μm of gold on a sapphire substrate. The trapezoidal shape is characteristic of ion milled structures. The yield on this batch of capacitors was low, due primarily to a poor surface finish on the metallized substrate caused by excessive handling. A second run of capacitors was made with 2 μm of gold on a polished GaAs wafer. This batch was ruined, however, by 2 to 5 μm "lumps" of gold which were carried over during sputtering. These modules kept the mask from making intimate contact with the photoresist and also tended to short out the finished capacitors after ion milling. A third run was made using a smooth carefully controlled 6000Å thick layer of gold on polished Si GaAs. A very high yield of 3 μm gap capacitors was obtained but with the expected reduced Q due to the high loss of the 6000Å thick gold.

Interdigital capacitors have also been made by plating through thick photoresist. This was done by, first, evaporating a thin layer of chrome and 1000Å of gold on the polished face of a gallium arsenide wafer. A 2 μm thick layer of photoresist was then applied over the gold and baked hard; the capacitor pattern was developed in the photoresist and was plated up. A commercial plating bath was used at its rated current density, but at a temperature of 20°C below that recommended by the manufacturer. This was done in an attempt to protect the photoresist and to prevent swelling of the photoresist lines which would, in turn reduce the size of the final gold lines. This was only partially successful as shown by the accompanying scanning electron microscope photos, figure 18.

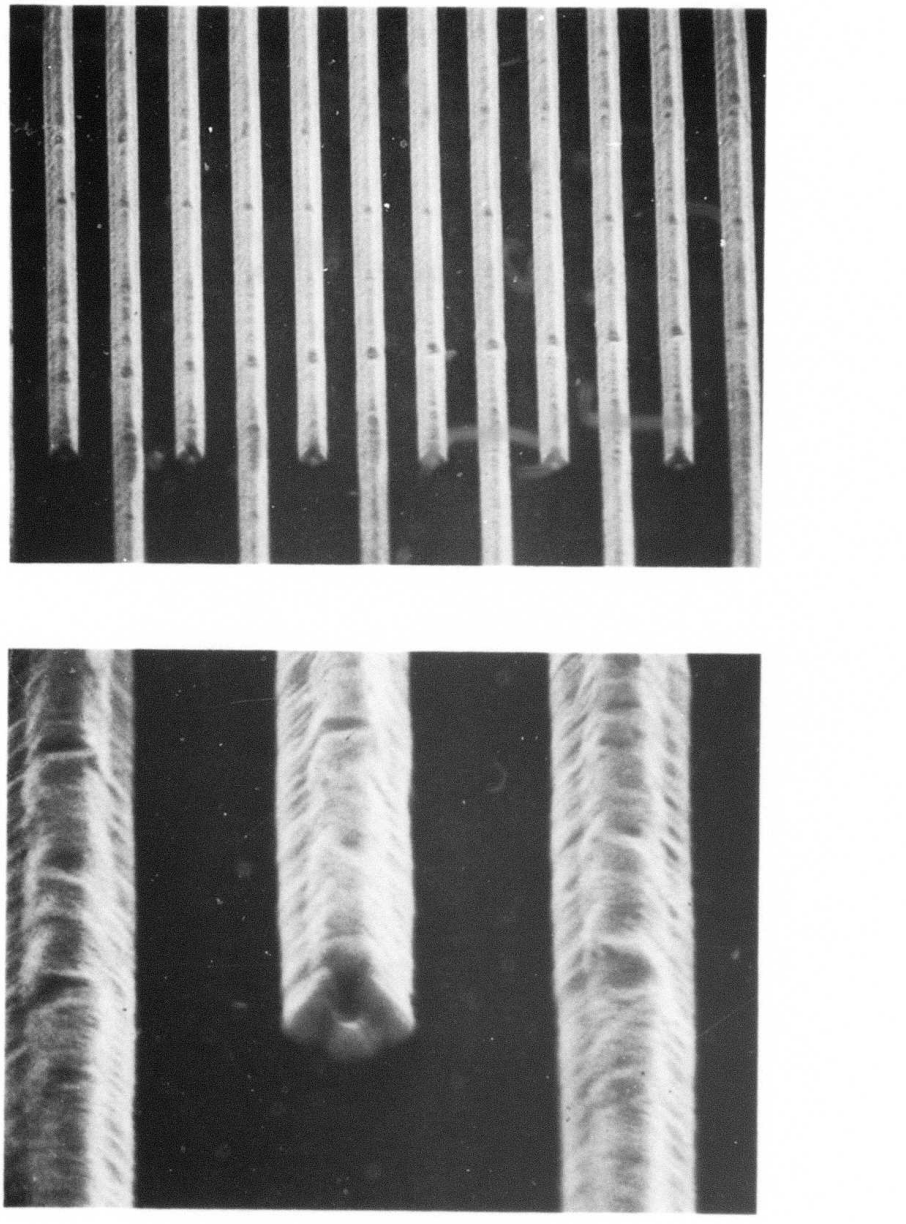

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Figure 17. SEM of Ion Milled 3 μm Interdigital Capacitor

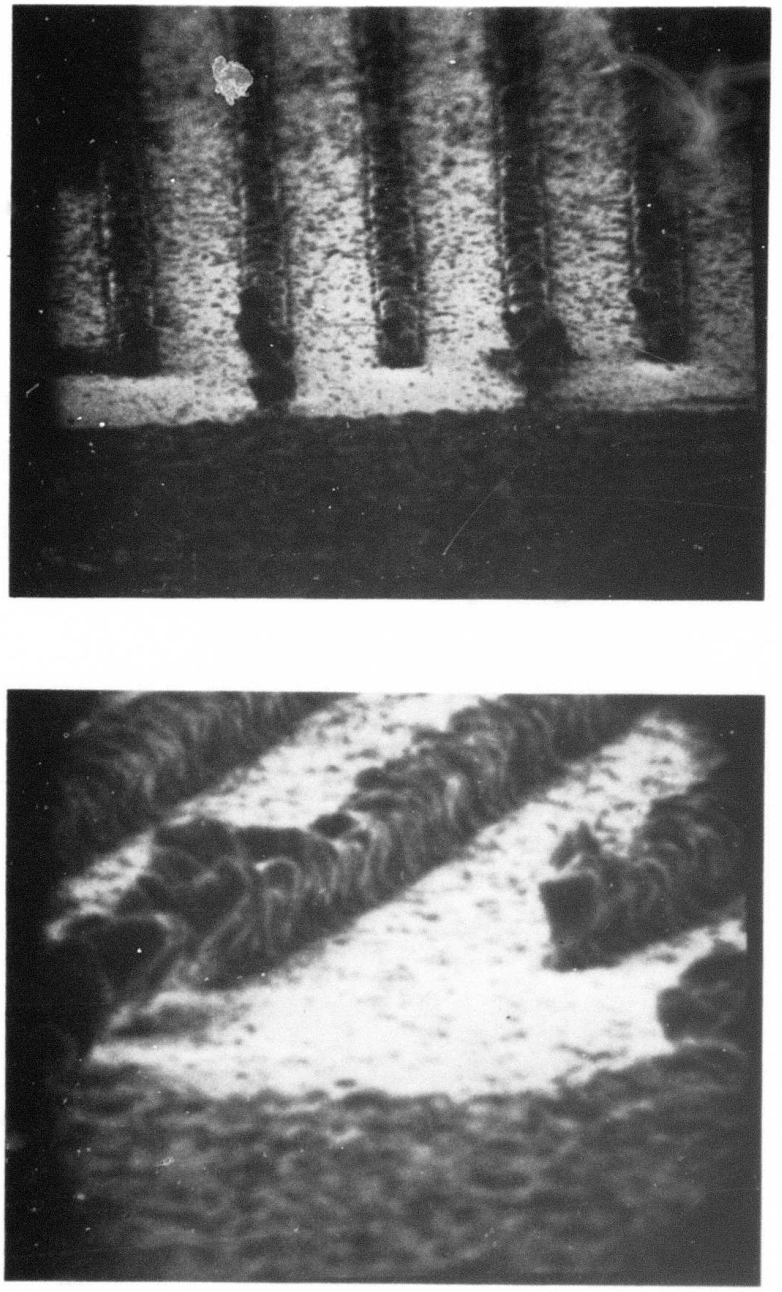

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Figure 18. SEM Photographs of Plated Interdigital Capacitors

The first plating attempt of 12 minutes produced well defined lines 1 μm thick; the second attempt of 30 minutes resulted in 4 μm lines that mushroomed at the top. The third try of 20 minutes plated out well defined lines 2 μm thick. However, the subsequent SEM photos showed a very course granular deposit, which when the thin chrome and gold between the lines was etched away, became even more rough.

The SEM photos also show what appears to be undercutting at the base of the lines. This was caused by the build up of photoresist around the edge of the wafer and thus prevented intimate contact of the photomask and the photoresist in the immediate area of the device pattern. This has been overcome by use of a two step photo process in which, first, all the photoresist except that in the device area is exposed and then developed away thus eliminating the thick edge buildup completely. Then the device pattern is exposed and developed in the remaining photoresist.

A fourth batch was fabricated using the two-step photo process and plating at a higher temperature and at a lower current density than before. Useable capacitors were produced, but the yield was not good and the plated gold was more porous than evaporated gold.

4.2 LUMPED ELEMENT MEASUREMENTS

Lumped elements used in monolithic circuits can be divided into two categories, those used in tuning applications and those used for RF bypass applications. The tuning elements need to be carefully controlled reactances with high Q's to minimize loss in the circuit. Bypass elements present a low impedance to the RF and a poor Q in them is tolerable in many instances. In the measurements of lumped elements to be used in a tuning application we need to determine their precise equivalent circuit. For bypass elements however, their impedance is so low, that it is difficult to get a good equivalent circuit, and we are normally satisfied to see that it is performing its intended function well.

Lumped elements could be tested, of course, by simply connecting them across a known transmission line and measuring the impedance. This is difficult to do, however, due to the parasitic reactances involved in connecting to the lumped element. A more accurate method is to build a resonant circuit and measure the resultant impedance versus frequency. Figure 19 shows a circuit used to measure interdigital capacitors and single turn inductors. Using this circuit, it is possible to measure the capacitor by itself and by bonding in two inductors and another capacitor to measure three resonant circuits. By analyzing the equivalent circuits shown in figure 20 and fitting to the measured data, it is possible to calculate the values of inductance and capacitance and their respective Q's.

The best results were obtained with interdigital capacitors with 3 μm fingers and gaps, and with 2 μm of gold. The theoretical capacitance was 0.856 pf and the calculated Q was 54 at 6 GHz. The measured capacitance was 0.75 pf and the range of Q was 40 to 55 at 6 GHz. The capacitors with 5 μm fingers and 1 μm gaps had a capacitance of 1.6 pf and a Q of 32 to 40 at 6 GHz. The inductors were 275 μm and 430 μm in diameter with a width of 50 μm and had inductance of 0.875 and 1.10 nH. The Q of the inductor has not been accurately determined due to the small number of circuits tested. The best estimate at this time is a Q of 60 at 6 GHz. The run of capacitors with 6000 Å of metal had a Q of approximately 10. Table I summarizes the RF results on lumped elements to date.

Although the yield of interdigital capacitors up to this point has not been good, it appears that with proper care in metallization and photoresist exposure, ion milling will produce useful high Q capacitors. There is, however, a difficulty which has not yet been resolved. All capacitors to date have been fabricated on either sapphire of semi-insulating GaAs. If the capacitor is made on a conductive substrate, we can express total Q as

$$\frac{1}{Q_T} = \frac{1}{Q_m} + \frac{1}{Q_D}$$

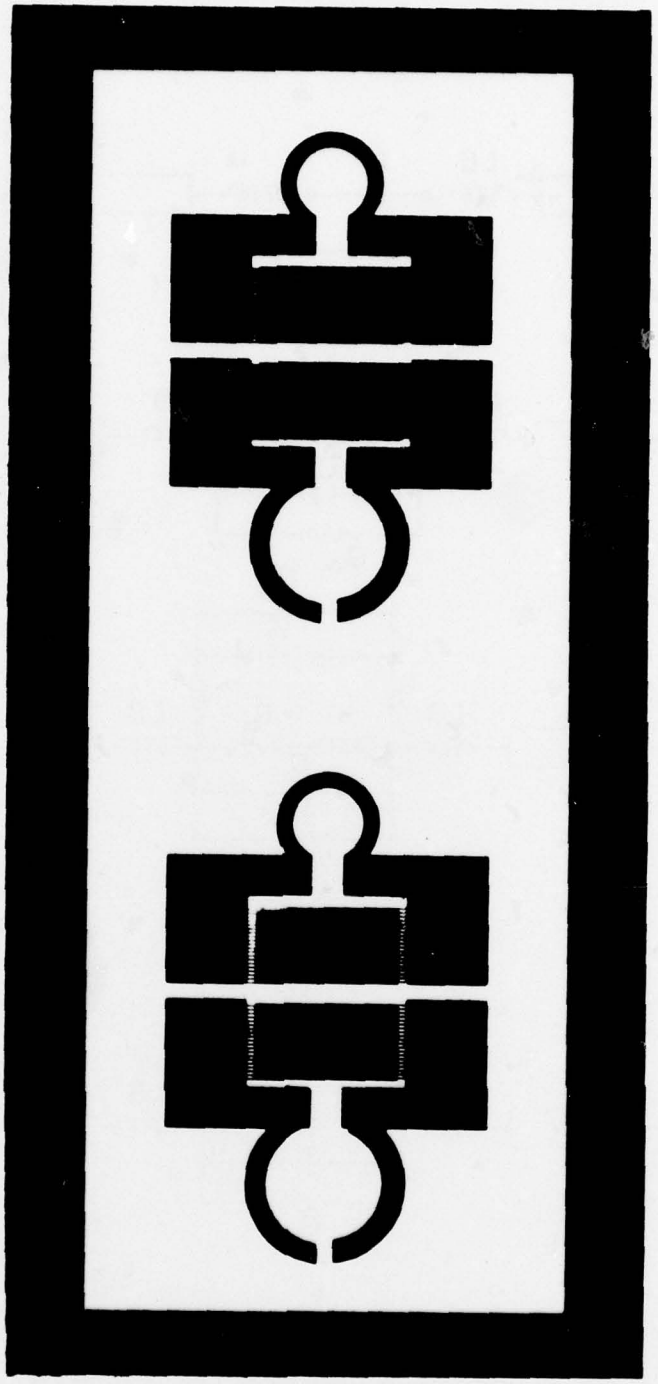

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Figure 19. Mask for Interdigital Capacitor Test

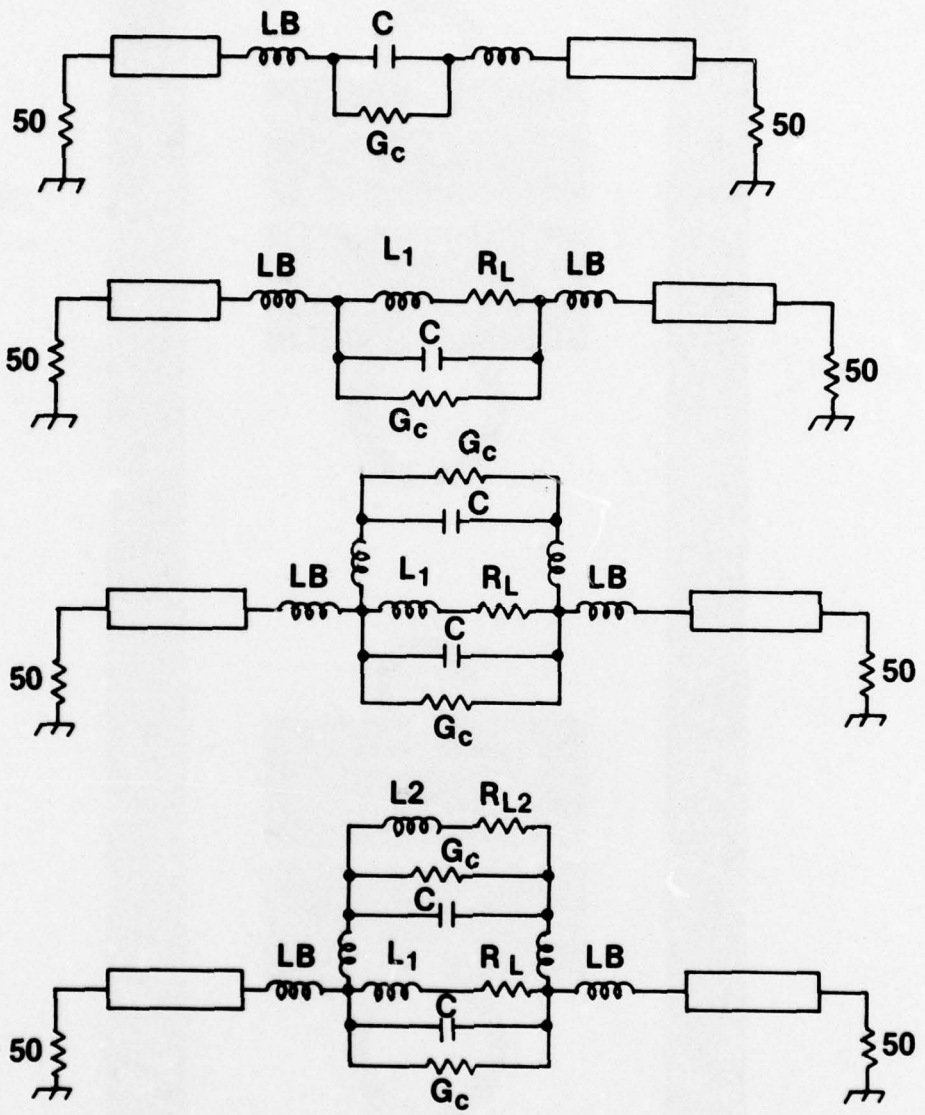

Figure 20. Equivalent Circuits of L-C Combinations

where Q_m is the Q due to metallization loss, Q_D is due to dielectric loss, and

$$Q_D = \frac{\omega C}{G} = \epsilon \omega \zeta$$

where

$$\zeta = \frac{1}{q \mu_n n}$$

If the devices are made directly onto semi-insulating GaAs there is no problem, but if a buffer layer is used it must be accounted for. The VPE buffer layers now being grown have a concentration, n, of about 1×10^{14}. From Sze[6], the resistivity is 12 ohm-cm yielding a Q_m at 7.5 GHz of 0.7. In order to be useful, either the buffer must be reduced in concentration to 10^{12} or below, or the buffer must be etched away beneath the capacitor.

4.3 ANODIZED CAPACITORS

Overlay capacitors were made by depositing aluminum on GaAs, anodizing the aluminum and evaporating a top conductor over the dielectric layer formed. Using this technique, a one hundred percent yield was achieved, and uniform dielectric thickness was maintained both across a single wafer and from wafer to wafer.

The capacitors fabricated had a capacitance of 25 pf, a breakdown voltage of 100 volts and a low frequency Q of 30. RF Q measurements on large capacitors (25 pf) are difficult to make because of the low impedances involved, but are relatively unimportant. These capacitors would be used only for RF bypass applications and Q's as low as 1 to 5 could be tolerated in many circuits. Using one of the 25 pf anodized capacitors as a short circuit at the end of a 50 ohm microstrip transmission line on a 0.6 mm thick alumina substrate yielded a reflection coefficient of less than 0.2 dB from 7 to 14 GHz. While this return loss is adequate for RF bypass applications, the use of these capacitors in a monolithic circuit requires further study to check compatability with other FET processing operations and also reliability studies to insure that the aluminum capacitor is adequately isolated from the gold metallization.

5. FET TEST FIXTURE

High gain microwave FET's are difficult to test in a standard 50 ohm system due to oscillation problems at low frequencies. A test fixture shown in figure 21 has been designed and constructed which is transparent in the band of interest and resistively loads the gate of the FET at low frequencies.

This test fixture will also be used to study lumped elements. Although we had originally envisioned an RF probe station to quickly measure lumped components, it is now felt that a simple test circuit with the lumped com-components bonded in place will give us greater accuracy and more confidence in the results. During later phases of the program, when large numbers of various lumped components and devices need to be evaluated quickly, a flexible microwave probe station will be reconsidered.

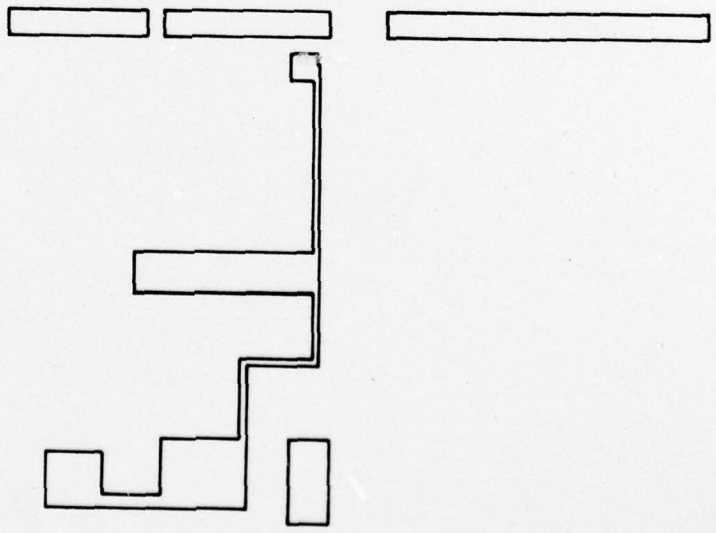

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Figure 21. Sketch of the FET Test Carrier
Substrate Size is 0.5 x 0.5 inch

6. PHASE SHIFTER

The basic phase shifter to be used in this program is the high-pass, low-pass shown schematically in figure 22. In this circuit when one set of diodes is forward biased, the other set is reverse biased. The RF energy then flows either through the filter formed by L_A, C_B, L_A or through C_A, L_B, C_A. The differential phase shift going through these filters is relatively flat over a wide frequency range. Table II lists the required element values to achieve phase shifts from 45 to 180 degrees at 7.5 GHz.

A 90 degree bit has been designed and a photograph of the mask is shown in figure 23. The mask has an error which is being corrected, but circuits will be built to test the fabrication procedure and limited RF testing will be performed while the new mask is in progress. The phase shifter will be built on GaAs and will use 5 μm interdigital capacitors and chip back to back Schottky barrier diodes. After the circuit is working properly with chip diodes, monolithic diodes will be grown in place.

The phase shifter is 80 x 86 mils and will be bonded to a 0.5 x 0.5 inch sapphire carrier substrate with coplanar transmission lines for RF in and out and bypassed bias lines.

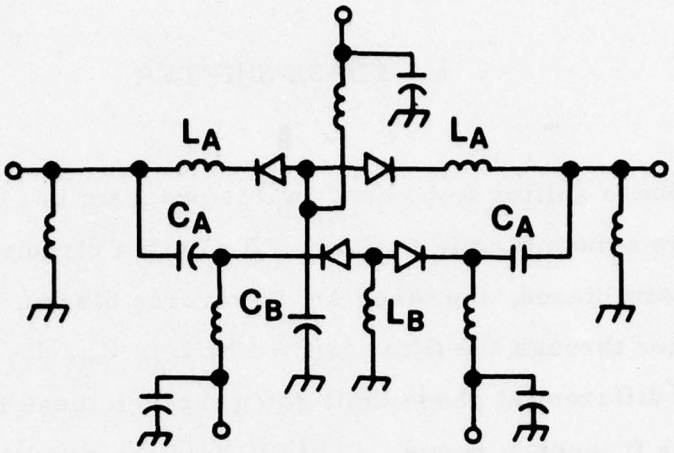

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Figure 22. Equivalent Circuit Model of One-Bit Phase Shifter Showing Bias Elements

TABLE 1
ELEMENT VALUES OF HIGH-PASS - LOW-PASS
PHASE SHIFTER FOR DIFFERENTIAL PHASE SHIFTS AT 7.5 GHz

$\Delta\phi$	L_A (nH)	L_B (nH)	C_A (pF)	C_B (pF)
180°	1.06	1.06	0.424	0.424
90°	0.439	1.50	1.024	0.300
45°	0.211	2.77	2.133	0.162

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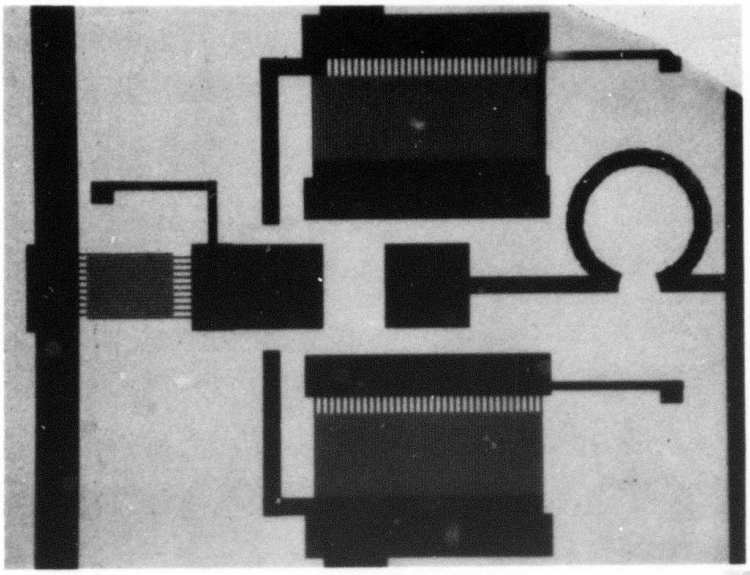

Figure 23. Photograph of 90 deg Bit Phase Shifter Mask

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