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FABRICATION AND ELECTRICAL PROPERTIES OF EPITAXIAL PBTE METAL-I--ETC(U)

AUG 79 P H ZIMMERMANN , M E MATHEWS

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Fabrication and Electrical Properties of Epitaxial PbTe Metal-Insulator-Semiconductor Structures

P. H. ZIMMERMANN, M. E. MATHEWS, and D. E. JOSLIN
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Interim Report

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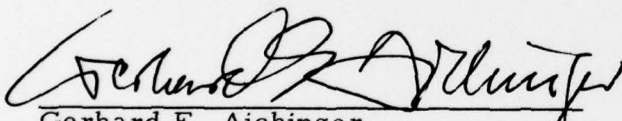
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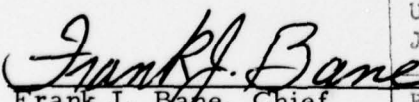
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This report has been reviewed by the Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.


Gerhard E. Aichinger
Project Officer

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Methods for the fabrication of metal insulator semiconductor structures with the use of epitaxial PbTe films are described. These methods obviate the need for treating the semiconductor surface. They involve epitaxial film growth in a vacuum environment by hot-wall epitaxy followed by (1) deposition of ZrO ₂ without breaking vacuum and (2) deposition of pyrolytic SiO ₂ . Capacitance-voltage characteristics in both cases closely correspond to theoretical values. Depletion layer generation is shown to be the dominant contribution to the inversion conductance.		

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PREFACE

It is a pleasure to acknowledge stimulating discussions with A. B. Chase, H. K. A. Kan, and D. A. Lilly.

The present business address of P. H. Zimmermann is Honeywell Electro-Optics Center, Lexington, Massachusetts, and of M. E. Mathews is Xerox Corporation, El Segundo, California.

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1. INTRODUCTION

Metal-insulator-semiconductor (MIS) structures fabricated from narrow bandgap semiconductors are becoming increasingly important in monolithic infrared imaging applications.^{1,2} Since both signal detection and processing can be accomplished on the same semiconductor chip with such structures, very high density focal plane arrays will be possible in the near future.

The suitability of PbTe for monolithic infrared application has been discussed by Tao et al.,³ and some experimental results on MIS structures fabricated from [100] PbTe bulk single crystals have been reported by Lilly et al.⁴ and Moulin et al.⁵ An alternative approach is the fabrication of MIS devices from epitaxial thin films. Epitaxial films grown in a vacuum environment have the advantage of not requiring surface lapping, etching, and cleaning, since the insulator can be deposited immediately after growth. For soft materials that require a foreign oxide such as PbTe, the lack of surface treatment is expected to result in a more ideal semiconductor-insulator interface. Moreover, this method has the potential of becoming a low-cost technology.

The fabrication method and MIS properties of structures fabricated with vacuum grown epitaxial thin films are discussed in this paper.

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2. DEVICE FABRICATION

A. EPITAXIAL THIN FILMS

Epitaxial thin films were grown in vacuum on cleaved BaF_2 substrates by means of the hot-wall-epitaxy (HWE) method.^{6,7} This method differs from other vacuum growth methods because a heated quartz tube is used to surround the space between the sources and the substrate. This tube is maintained at a higher temperature than other parts of the system, and, hence, the tube acts as a reflector for the effusing molecules. PbTe and Te are sublimated from two sources whose temperatures are controlled independently, which provides control of the stoichiometry of the resulting films (Fig. 1).

BaF_2 crystals obtained from the Harshaw Chemical Company were cleaved in the ambient to form 5 mm by 5 mm by 0.5 mm slab substrates and mounted in an oil-free vacuum growth chamber immediately after cleaving. The source materials used were double zone refined Te obtained from Cominco (Spokane, Washington) and PbTe obtained from Atomergic Chemetals Co. (Long Island, New York), both were 99.999% pure.

In initial growth trials, the BaF_2 slabs were attached directly to a substrate heater block with a thin layer of liquid Ga metal to provide a low-strain and highly thermal conductive mount. X-ray diffractometry verified that $[111]$ epitaxial thin films were grown routinely, but only rarely did the films have specularly reflecting surfaces. Most often, the surface consisted of submicron triangular pyramids. However, films with specularly reflecting surfaces could be grown routinely by severely restricting the thermal coupling between the BaF_2 substrate and the substrate heater block. The substrate was simply placed over a hole in a thin (0.4 mm) stainless steel fixture, which, in turn, was mounted just below the substrate heater block (Fig. 1). Typically, the substrate heater block was heated to the 370°C growth temperature while in an idling position, with the BaF_2 substrate "viewing" room temperature surfaces. While the substrate heater block was maintained at the growth temperature, the assembly was moved into the growth position over the hot-wall chamber (position B) by a rotating mechanism. Direct measurement of the substrate temperature with a small thermocouple indicated that the sample temperature was initially 260°C . When moved to the growth position, the sample temperature increased rapidly as a consequence of exposure to the hot wall and source radiation. The initial temperature rise rate was $50^\circ\text{C}/\text{min}$, and the sample was stabilized at about 460°C .

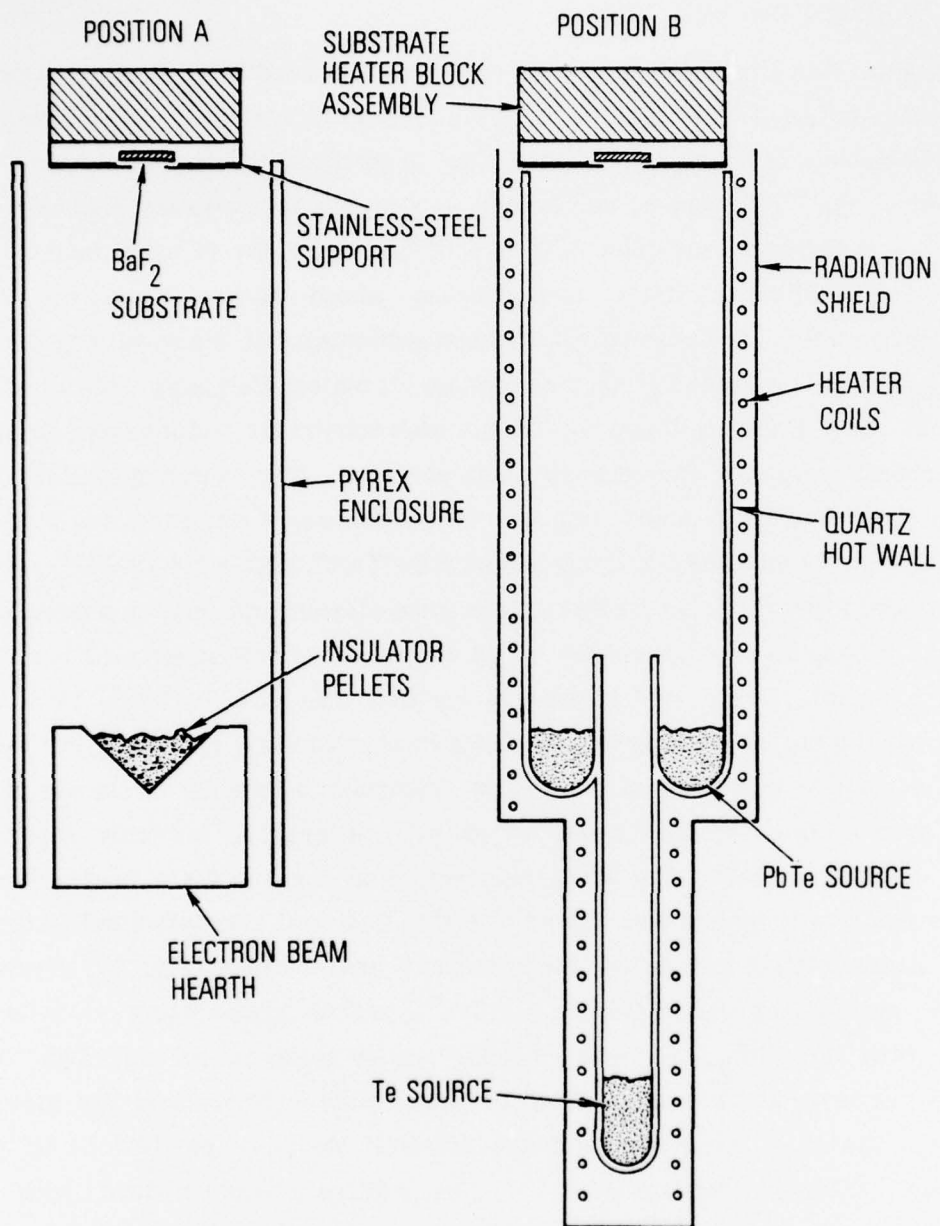


Fig. 1. Schematic diagram of PbTe HWE growth and in situ insulator vacuum deposition system.

It is suspected that this mounting scheme enhances the film growth by increasing the density of sites at which nucleation occurs because of the low substrate temperature at growth onset. In addition, island coalescence in the postnucleation growth stage is promoted by a rapid increase in substrate temperature, which, in turn, decreases the growth rate and increases the surface mobility.

Nominal growth temperatures were 530°C for the hot wall and the PbTe source, 370°C for the substrate heater block, and 290°C for the Te reservoir for films near the p-n turnover point. The growth rate was typically 1.6 $\mu\text{m/hr}$.

Electrical properties of the films are similar to the best reported in the literature.⁷ Carrier concentrations in the low 10^{16} cm^{-3} range at 77 K could be obtained routinely. Mobility values up to $3 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ and $1 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ were obtained at 77 K for n- and p-type films, respectively. Unpassivated n-type films exhibited changes in the Hall voltage with time over several days. In contrast, films passivated in situ with an insulator coating had stable Hall voltages that were different from those measured on the uncoated samples. These effects can be attributed to atmospheric exposure, which has been shown to affect the surface of PbTe and other lead chalcogenides driving the surfaces p-type.^{8,9}

B. INSULATOR DEPOSITION

Both ZrO_2 and SiO_2 were used as insulators in MIS structure fabrication. To prepare for the ZrO_2 deposition, the epitaxial PbTe film was moved away from the hot-wall growth position, into an idling position, thereby terminating the growth. After cooling for 30 min in a 10^{-6} Torr vacuum, the sample was moved into position A. ZrO_2 was then deposited at 5 A/sec to a nominal 1200-Å thickness by evaporating Merck pressed ZrO_2 pellets with an electron beam source. A background oxygen pressure of 1.5×10^{-5} Torr was maintained during the deposition by introducing UHP grade gas into the vacuum chamber at a low rate to ensure oxide stoichiometry. The sample temperature was estimated to rise to a minimum of 200°C during the deposition.

Low-temperature chemical vapor deposition (CVD) was the technique used to deposit SiO_2 . The PbTe films were removed from the growth chamber, mounted on a heater stage with Ga metal, and then transferred to a simple CVD chamber.¹⁰ Total atmospheric exposure of the PbTe film was limited to 15 min. After purging the CVD chamber with N_2 ($6300 \text{ cm}^3/\text{min}$), SiH_4 gas ($400 \text{ cm}^3/\text{min}$) was admitted, and the sample temperature was brought up to 275°C in 1 min. O_2 gas ($140 \text{ cm}^3/\text{min}$) was then admitted to initiate the SiO_2 film growth. The growth was terminated when the appropriate color was observed, giving films 800 to 900 Å thick.

MIS structures were completed by depositing a series of 250- μm -diameter Au metal gate electrodes in another vacuum chamber. After the metallization, selected samples were annealed under various conditions.

3. MIS PROPERTIES

Several requirements are essential for CCD or CID operation. Foremost among these are that the semiconductor surface potential can be manipulated by the gate voltage and that the minority carrier generation currents should be low. The equivalent circuit for the inverted semiconductor surface can be described by a conductance G_p in parallel with the depletion capacitance C_p . By the addition of the oxide capacitance in series, the equivalent circuit for the MIS structure in inversion is obtained. G_p , which is a measure of the minority carrier generation current, can be extracted from a plot of the measured MIS inversion conductance G_m or capacitance C_m as a function of frequency.^{5,11-13} Alternatively, G_p can be obtained from a measurement of the complex admittance at a single frequency. The parallel conductance and capacitance can be cast in terms of the measured admittance by a simplified version of expressions given by Nicollian and Goetzberger.¹²

$$\frac{G_p}{\omega} = \frac{C_{ox}^2 \frac{G_m}{\omega}}{(C_{ox} - C_m)^2 + \left(\frac{G_m}{\omega}\right)^2} \quad (1)$$

$$C_p = C_{ox} \frac{(C_{ox} - C_m) C_m - \left(\frac{G_m}{\omega}\right)^2}{(C_{ox} - C_m)^2 + \left(\frac{G_m}{\omega}\right)^2} \quad (2)$$

Conductance-voltage (G-V) and capacitance-voltage (C-V) the measurements were performed at various frequencies with the use of a PAR 184 current sensitive preamplifier and PAR 126 lock-in amplifier to characterize the MIS structures. Measurements were made with the sample immersed in a liquid nitrogen bath and shielded from the room-temperature background photon flux. A fine wire manipulated by a mechanical stage was used to make contact with the gate electrode.

Representative results for a p-type PbTe-ZrO₂ structure at 77 K are shown in Figs. 2 and 3, both before and after vacuum annealing. The annealing was accomplished at 10⁻⁷ Torr and at a sample temperature of 280°C for 2 hr. In both cases, C-V curves indicate that the semiconductor surface proceeds from accumulation through depletion into inversion as the gate voltage is increased. The slight voltage dependence at high-bias voltages is the result of voltage-dependent oxide dielectric properties. At 77 K, the structures could be biased to 60 V without breakdown, indicating that the dielectric strength is greater than 5 X 10⁶ V/cm. The G-V characteristics at 100 kHz were essentially flat, independent of voltage, with a notable absence of peaks at bias voltages corresponding to depletion and weak inversion. Such peaks would be expected to arise from fast surface states.^{12,13} It is estimated that the density of fast surface states is less than 3 X 10¹¹/eV/cm².

All characteristics exhibited some hysteresis. The direction of the hysteresis is consistent with hole or electron injection from the semiconductor. When annealed in vacuum, the hysteresis window narrowed, the semiconductor surface became less accumulated, and the surface carrier concentration increased.

The high-frequency characteristics of preannealed and postannealed structures could be fitted extremely well with numerical capacitance calculations. These calculations were performed by means of degenerate statistics¹⁴ with band parameters taken from a review article by Dalven.¹⁵ An example of the type of fit obtained with the flatband voltage and carrier concentration as adjustable parameters is shown in Fig. 2. The ratio of oxide dielectric constant to thickness was determined from the oxide capacitance.

The capacitance behavior observed at 400 Hz is still high frequency (Fig. 3). However, at this lower frequency, a contribution to the conductance in inversion is present. The parallel conductance calculated from these data is 1.6 X 10⁻⁴ mho/cm² for the unannealed sample and 1.1 X 10⁻⁴ mho/cm² for the annealed sample. The characteristic frequency of the structure (at which G_m/ω is a maximum) is given by¹¹ $f_o = G_p / 2\pi(C_{ox} + C_p)$ and can be calculated from these data to be 42 and 19 Hz, respectively. These frequencies correspond to a storage time of several milliseconds. (For some structures, G_p was extracted from a G_m/ω versus ω plot. These results are in agreement with the results obtained from the single-frequency admittance measurement).

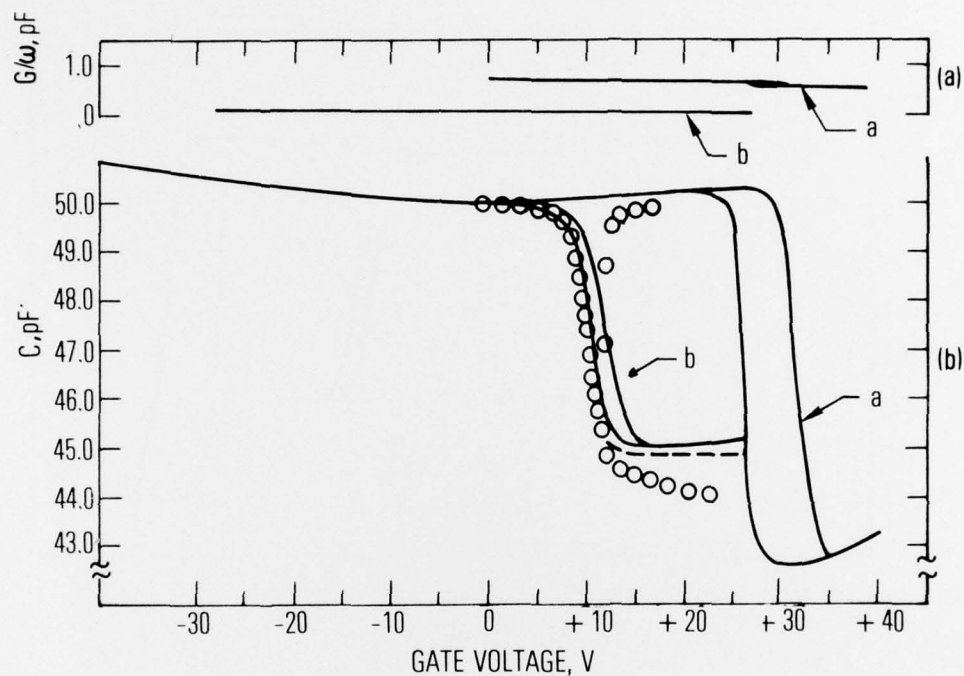


Fig. 2. 100-kHz experimental $C_m \omega^{-V}$ and $(G_m/\omega)-V$ characteristics of a p-Type PbTe-ZrO₂ structure. (a) Before vacuum anneal. (b) After vacuum anneal.

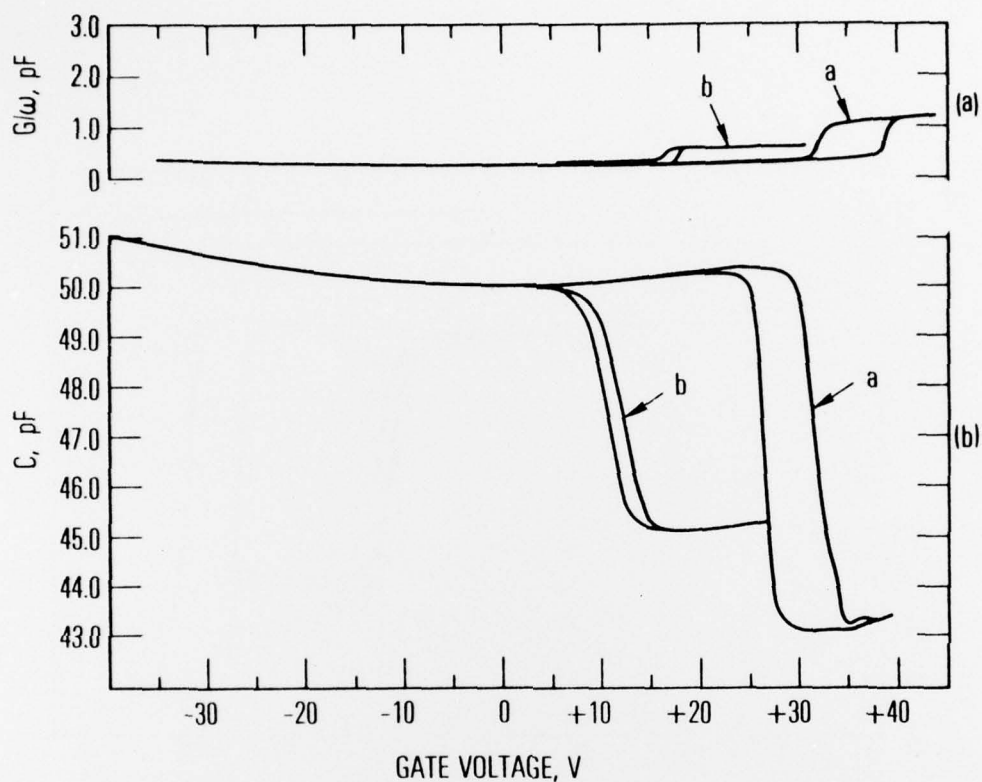


Fig. 3. 400-Hz experimental C_m -V and (G_m/ω) -V for the sample in Fig. 2. (a) Before vacuum anneal. (b) After vacuum anneal.

The admittance of the ZrO_2 MIS structures fabricated on different areas of the BaF_2 surface exhibited a high degree of uniformity, except in areas where a high density of cleavage steps was observed. In those areas, the oxide tended to be leaky and had abnormally high conductance values. Such difficulties may be circumvented by the substitution of carefully polished BaF_2 for the cleaved BaF_2 as the substrate for epitaxial growth.¹⁶

Several structures were also fabricated with SiO_2 . The characteristics of these structures exhibited a large amount of hysteresis (Fig. 4a), making accurate determination of G_p impossible. Annealing in an H_2 gas flow for 2 hr at 250°C dramatically narrowed the hysteresis window (Fig. 4b-4d). The C-V characteristics at 100 kHz corresponded closely to theoretical calculations. From admittance measurements at 1 kHz, G_p was determined as $6 \times 10^{-3} \text{ mho/cm}^2$. The uniformity of the admittance voltage characteristics was inferior to that of the ZrO_2 structures. This can be attributed to the less uniform pyrolytic SiO_2 deposition.

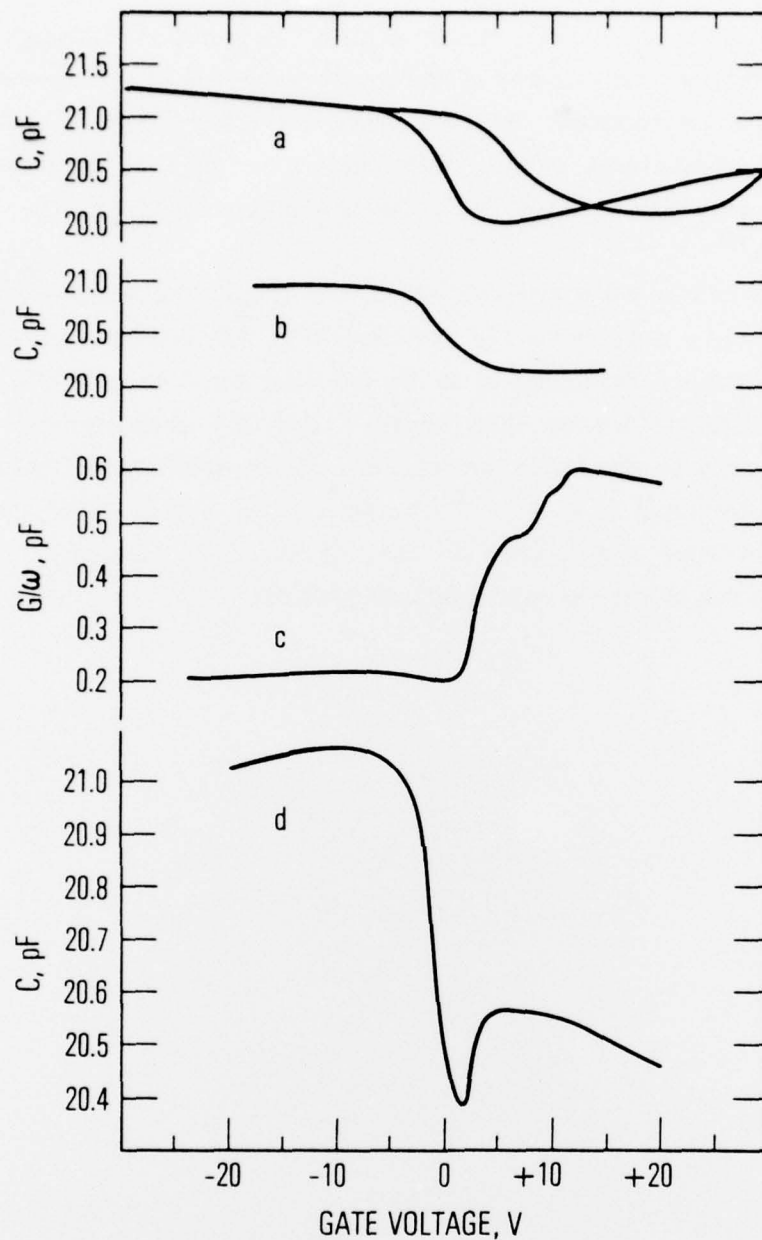


Fig. 4. Admittance-voltage characteristics of a p-type PbTe-pyrolitic SiO structure. Curves a and b are the C-V characteristics at 100 kHz before and after anneal, respectively; curves c and d are the conductance and capacitance of the annealed structure at 1kHz, respectively.

4. DISCUSSION

It has been demonstrated that PbTe MIS structures with high-frequency C-V characteristics very close to theoretical predictions can be fabricated by means of PbTe epitaxial thin films. In addition, by suitable annealing of the MIS structures, it appears possible to achieve a controlled degree of surface accumulation in p-type PbTe-ZrO₂ structures. Such accumulation is desirable for preventing a lateral conductance of minority carriers¹⁷ from contributing to the parallel conductance in inversion.

Three other terms that may contribute to G_p are bulk diffusion, surface generation, and depletion layer generation. These contributions can be summed, respectively, as^{11,20}

$$G_p = \frac{q \mu_n n_i^2}{L_n N_A} \alpha + \frac{q^2}{kT} N_A N_S \sigma_n v_n \exp\left(-\frac{q\psi_s}{kT}\right) + \frac{q n_i d}{\tau_g \psi_s} \quad (3)$$

where

q	=	electronic charge
μ_n	=	electronic mobility
n_i	=	intrinsic carrier concentration
L_n	=	electron diffusion length
N_A	=	acceptor concentration
N_S	=	surface state density per unit area
ψ_s	=	surface potential
σ_n	=	electron scattering cross section
v_n	=	electron thermal velocity
d	=	depletion layer width
τ_g	=	depletion generation lifetime

The parameter α is unity for thick films. For thin films of thickness t , its value may range from¹⁹ $\tanh(t/L_n)$ to $\coth(t/L_n)$, which corresponds to the limits of zero and infinite recombination velocity at the PbTe-BaF₂ interface, respectively.

The dominant contribution to the conductance can be determined by analyzing the temperature dependence of G_p . Experimentally, G_p is extracted from admittance data obtained at different temperatures. Such values are shown in Fig. 5. The temperature dependence of the conductance is activated and varies in the same manner as the intrinsic carrier concentration, indicating that the depletion-layer generation is dominant. The diffusion contribution is expected to have a stronger temperature dependence, determined mainly by n_i^2 according to Eq.(3). The surface generation term depends on temperature primarily through the exponential dependence on ψ_s/kT at a fixed gate voltage. Numerical calculations indicate that the surface potential varies considerably with temperature, causing a temperature dependence even stronger than that of n_i^2 .

Estimates of the size of the diffusion and surface generation contribution at 77 K indicate that these terms are much smaller than the observed conductance values. The bulk diffusion contribution is estimated with the diffusion lifetime of 2×10^{-7} sec determined for HWE PbTe films by the diode step recovery technique.¹⁸ The diffusion terms calculated is 5×10^{-7} mho/cm², with the use of material properties appropriate to these structures ($t = 6 \mu\text{m}$). The surface generation term, based on an estimate of $N_{SS} = 3 \times 10^{11}/\text{eV/cm}^2$ at midgap, is smaller than the observed conductance by orders of magnitude.

The depletion generation lifetime τ_g can be calculated from the expression for the depletion-layer conductance. A value of 2×10^{-9} sec is found for our better ZrO_2 structures. This value for the lifetime is surprisingly low in view of the diode recovery lifetime measurements. It is quite possible that the concentration of recombination centers is relatively large near the top surface of the epitaxial films. The surface region was formed during the last stage of growth, and thus is annealed to a lesser degree than the bulk of the film. It is suspected that in that case the recombination center concentration can be reduced by a subsequent annealing of the film at the growth temperature. It is also possible that the interfacial strain between the oxide coating and the PbTe may cause defects near the PbTe-oxide interface.

It was observed that the lifetime in the better ZrO_2 structures had decreased when rechecked after several weeks. It is speculated that such a decrease may be associated with a chemical reaction at the oxide-semiconductor interface and a defect or impurity

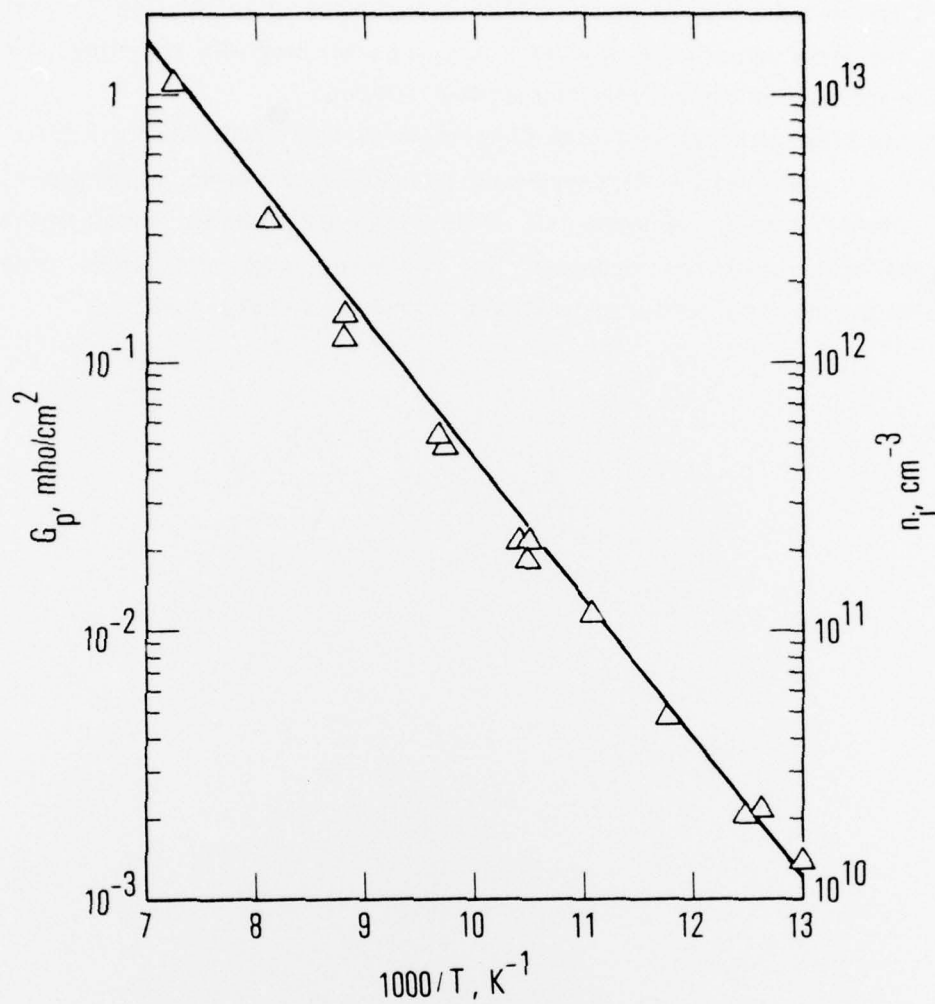


Fig. 5. Conductance values G_p per unit area for an annealed PbTe-ZrO₂ structure calculated from admittance measurements in inversion are shown as a function of inverse temperature (triangles). The PbTe intrinsic carrier concentration n_i (solid curve) was calculated from parameters given in Ref. 14.

diffusion into the film. Grain boundaries, which can be observed under Nomarski phase contrast microscopy, may be involved in such a process. Manipulating the grain size by varying the HWE growth parameters²¹ and then forming MIS structures could be an effective approach in the investigation of such effects.

It has been demonstrated that fabrication of MIS structures from PbTe epitaxial thin films is a viable method for fabricating monolithic structures, which are suitable for use as charge injection devices. It is expected that further development of such structures will drastically decrease the depletion layer generation process that dominates the minority carrier generation at the semiconductor surface.

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