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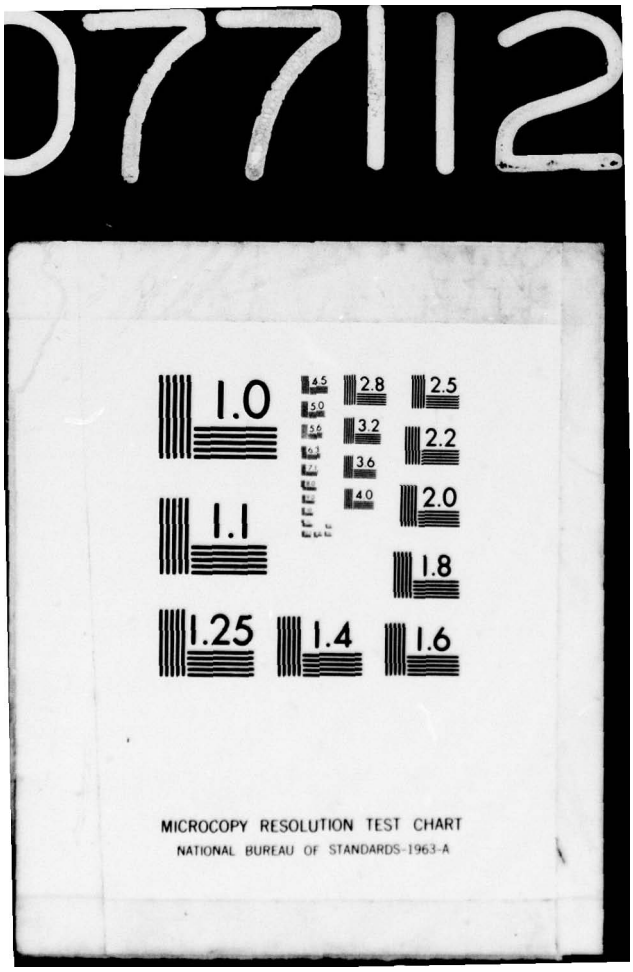
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TECHNICAL REPORT ARMID-TR-78002

THE APPLICATION OF DC-DC ENERGY CONVERSION IN A SOLAR ENERGY SYSTEM

JOHN P. TOBAK

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REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (14) Technical Report ARMID-TR-78062	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) (6) THE APPLICATION OF DC-DC ENERGY CONVERSION IN A SOLAR ENERGY SYSTEM	5. TYPE OF REPORT & PERIOD COVERED (9) Final rept.
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) (10) P. John Tobak	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS ARRADCOM, MISD Scientific & Eng App Div (DRDAR-MSA) Dover, NJ 07801	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS ARRADCOM, TSD STINFO (DRDAR-TSS) Dover, NJ 07801	(11) 12. REPORT DATE Sept [redacted]79 / 13. NUMBER OF PAGES 155
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (12) 155	15. SECURITY CLASS. (of this report) Unclassified / 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

(18) SBIE (19) AD-E400 363

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

DC-DC
Converter
Series switching
Regulator
Voltage multiplier
Flyback
Solar energy

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Expressions of voltage gain, current, and efficiency are developed for each of five different methods of DC-DC energy conversion. One of the five methods is selected as the design model for a prototype converter to be used in solar energy applications. Both the prototype's performance and the test methods employed are described. Efficiencies as high as 86% are measured along with a constant voltage line regulation of 0.04 volts per volt and a (over)

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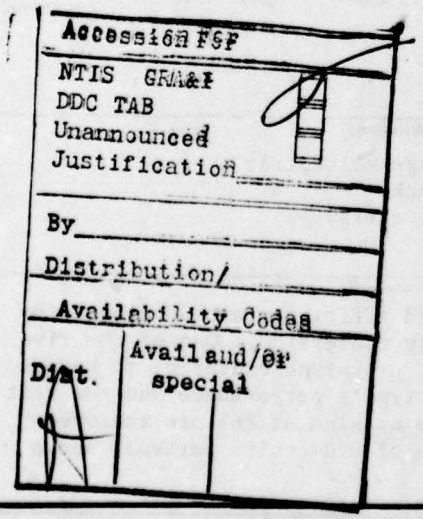
20. ABSTRACT (Continued)

constant voltage load regulation of 0.034 volts per ohm. The prototype acts as a constant 12-volt power supply capable of delivering up to 10-amp currents.



ACKNOWLEDGEMENTS

The author wishes to express his appreciation to the following ARRADCOM personnel for their comments, suggestions, and cooperation in the generation of this report: Mr. William A. Bussom, Mr. Bruce M. Nagel, Mr. Edward Lacher, Miss Carol Novak, Mrs. Sylvia Polanski, Mr. Robert Oravits and Mr. Victor Galgano.

FOREWORD

This report is an adaptation of a thesis submitted by the author to the Graduate School of Rutgers University in partial fulfillment of the requirements for the Degree of Master of Electrical Engineering, under a Picatinny Arsenal Technical Fellowship.

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INTRODUCTION

With supplies of oil and natural gas dwindling, solar energy must seriously be considered one of the future's major sources of thermal and electrical energy. The direct conversion of sunlight into electrical energy is known as photovoltaics. It is in this area of solar energy conversion that this report will concentrate.

Photovoltaic Technology

Solar cells are semiconductor photodiodes which have been optimized to efficiently convert sunlight into electrical power.[1] They consist primarily of a base material and a deposited region. The more popular base materials include silicon, cadmium sulfide, gallium arsenide, indium phosphide, amorphous silicon, and cadmium telluride. Silicon base structures are the most popular and consist of four different types. A conventional 12% efficient silicon type is the most popular. A silicon nonreflecting structure is the most efficient with a yield of 18%, but a low output voltage and poor response to short wavelengths limit its applications. The third type is a heterojunction structure which consists of a silicon base and a thin nonsilicon layer of semiconductor material. It offers efficiencies between

6% and 12%. The fourth type of silicon structure is the Schottky-barrier cell. It consists of a silicon base and a metallic deposit yielding efficiencies of 8%. Heterojunction and Schottky type structures are the most promising for future development. They are the most easily manufactured and require small amounts of rare materials. While offering efficiencies of only 6% to 8%, cadmium sulfide base structures offer low production costs and are therefore also being investigated. A 50% decrease in solar cell costs over the past two years, and the monetary encouragement of the Energy Research and Development Administration have done a great deal to increase the solar cell industry. The present cost of solar cells is approximately $15/peak watt. Although a projected goal of $.50/peak watt by 1986 seems distant, manufacturers feel confident in its realization.

Solar Cell Application

Areas of solar cell use can be divided into large scale and small scale applications.[2] Large scale photovoltaic applications are those which generate a large amount of electricity at one central location and then distribute it on demand. The basic problems with this type of system lie in the areas of peripheral equipment, energy storage, and backup from other sources

of energy. In large systems, sophisticated power conditioning equipment used for regulation, DC to AC conversion, and AC transmission increase cost and decrease overall efficiency. Methods of storing large amounts of generated power are also a problem. Areas of study include advanced electrical batteries, thermal storage in rocks and water, mechanical storage in large and fast moving flywheels, hydraulic storage in elevated water, and chemical storage in generated hydrogen for future burning. If none of the above methods of storage prove to be feasible, the problem of alternate backup utilities becomes paramount. Since solar conversion is only possible during daylight hours of high solar radiation intensity, alternate utilities must constantly maintain a high level of energy in reserve to meet any unexpected great demand. The result is a costly and inefficient energy system.

Unlike large scale systems, small scale applications face no transmission problems and adequately store reserve energy in common lead acid type batteries. While small systems of this type often find themselves in homes, office buildings, and small industries, they are primarily used in remote areas. Examples include desert water pumping stations, mountaintop radio and TV communication stations, microwave repeaters, offshore

drilling platforms, shipboard battery charges, buoy-mounted navigational aids, and space applications. It is in this area of small scale applications that this study is concentrated.

Solar devices produce a DC output which represents only 12% of the solar energy available. In addition, the voltage they generate is a variable function of sunlight and load. Storage batteries charged by solar panels lose their charge with use and produce varying terminal voltages. The result is the necessity for an interface between the supply and the load which offers both high efficiency and good regulation. Since this report only deals with loads requiring a DC supply, the desired interface is referred to as a DC-DC converter. Five of the most popular types of DC-DC converters are introduced. One is then chosen and designed to meet the specifications of a solar energy application.

Before a converter can be built, its input and output specifications must be defined. A survey of equipment requiring a DC supply indicates that a supply voltage of 12 V is the most in demand. The current requirements of a few 12 V items are listed in appendix A. The voltage characteristics of a typical rechargeable storage battery are also presented in appendix A. Since the voltage of a solar panel varies by as much as

15% of its nominal value, an input specification of ± 15% can be set to assure maximum panel and battery utilization. A list of all the design specifications appears in table 1.

A COMPUTER AIDED ANALYSIS OF SEVERAL APPROACHES TO DC-DC ENERGY CONVERSION

The capability to transfer energy efficiently is not only desirable but necessary in the light of present day energy problems. The DC-DC converter may provide such capability. In general, a DC-DC converter can be defined as a two-port network which extracts power from a constant voltage or current source and delivers it to a load at a different constant value of voltage or current. Its areas of application include photography, space systems, infrared device operations, solar energy systems, and energy transfer circuits used in the detonation of munitions.

Converters which attempt to maximize efficiency seek to satisfy the ideal input/output relationship of equation 1.

$$(V_{in}\ I_{in})_{AVG} = (V_{out}\ I_{out})_{AVG} \qquad (1)$$

In the converters discussed in this report, input and output voltages are constant. This allows equation 1 to be rewritten as

$$(V_{in})(I_{in_{AVG}}) = (V_{out})(I_{out_{AVG}}) \quad (2)$$

This implies that any decrease in voltage from input to output demands an increase in average current. In addition, any decrease in average current requires an increase in voltage. This results in the realization that in any conversion process of high efficiency, either a current or voltage boost must be experienced. Before such a boost can take place, the input DC signal must be transformed into an AC signal. This AC transition is necessary since voltage or current boosts can only be realized, from basic circuit theory, by equations 3 or 4.

$$v(t) = L \frac{di(t)}{dt} \quad (3)$$

$$i(t) = C \frac{dv(t)}{dt} \quad (4)$$

In the following examples, a transistor is used to generate the AC signals required in the conversion process. It performs as a switch operating between saturation and cutoff. Since the greatest amounts of power dissipation are experienced in the active region, a fast transition between the ON and OFF states is desirable. This results in the generation of an AC signal in the form of a square wave.

In the discussion of converters which follows, the development of steady state expressions describing voltage gain, current gain, and efficiency is emphasized.

Table 1. Converter specifications

Input voltage variation	±15% of Nominal
Output voltage	12 V ± .5 V
Output current	1 A - 15 A
Efficiency	70% +
Overshoot and undershoot for maximum charges in load	2 V
Recovery time (RT) for maximum changes in load	10 ms maximum for transient recovery to within 2% of final value

Self-Oscillating Transformer Coupled DC-DC Converter

The self-oscillating transformer coupled DC-DC converter (fig. 1) converts energy stored in its iron core to a voltage and current level determined by the turns-ratio of the transformer.[3,4] In order to transfer energy to the secondary, an AC signal is impressed across the primary winding of the transformer in the form of a square wave. Specifically, with transistor Q_2 off, Q_1 stays on until the core saturates. At that point, the base drive of Q_1, supplied by the voltage across N_2, decreases turning Q_1 off. As Q_1 turns off, the voltage across N_2 is reversed, and Q_2 turns on while Q_1 is driven off completely. The cycle is then repeated. In order to develop expressions for input and output waveforms, modifications must be made to the standard transformer model (fig. 2).[5,6] Equations 5 and 6 represent the loop equations which describe the circuit shown in figure 2.

$$V_1 = i_1 R_{ps} + L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{5}$$

$$V_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} + i_2 R_{ss} \tag{6}$$

where:

R_{ps} = Primary series resistance

R_{ss} = Secondary series resistance

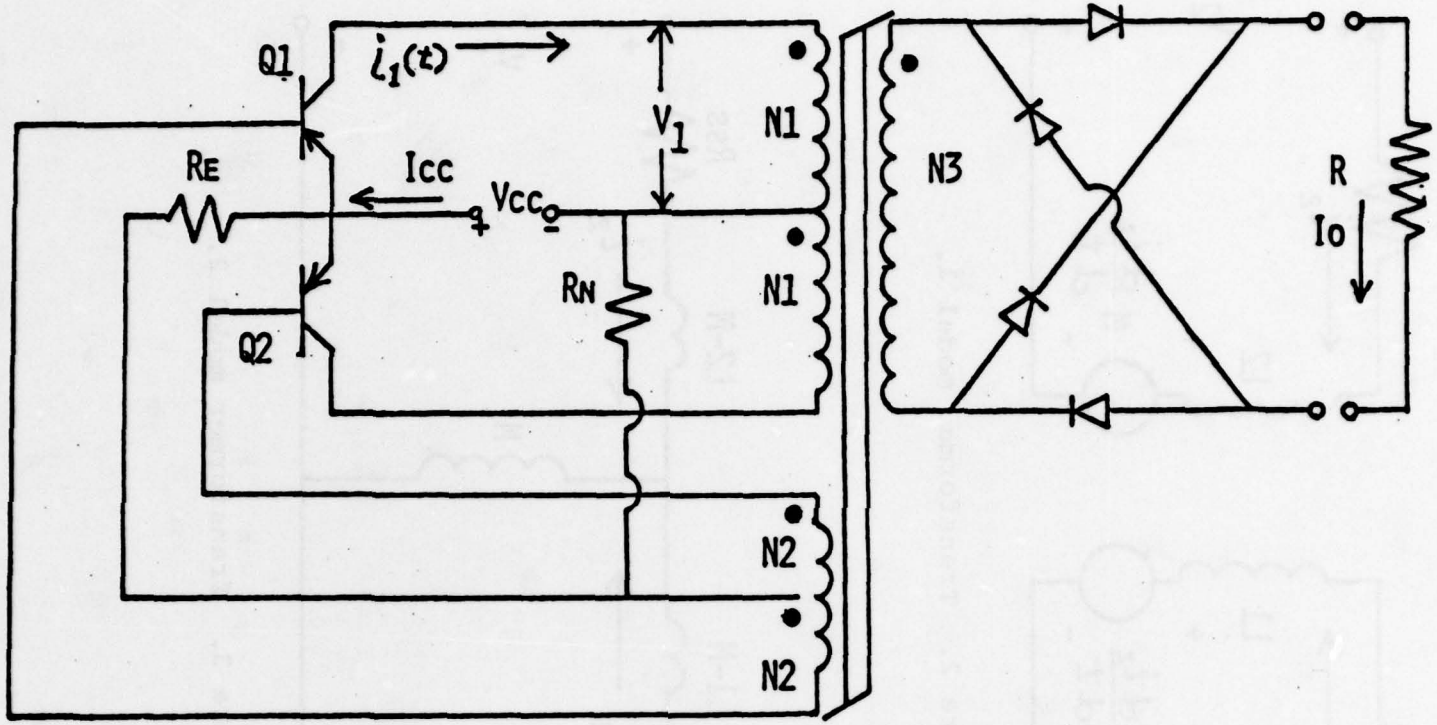

Figure 1. Self-oscillating transformer coupled DC-DC converter

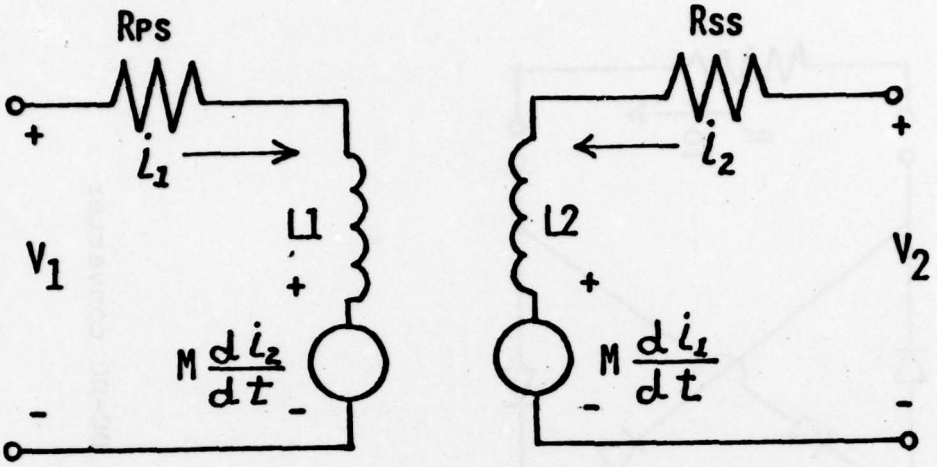

Figure 2. Transformer model 1.

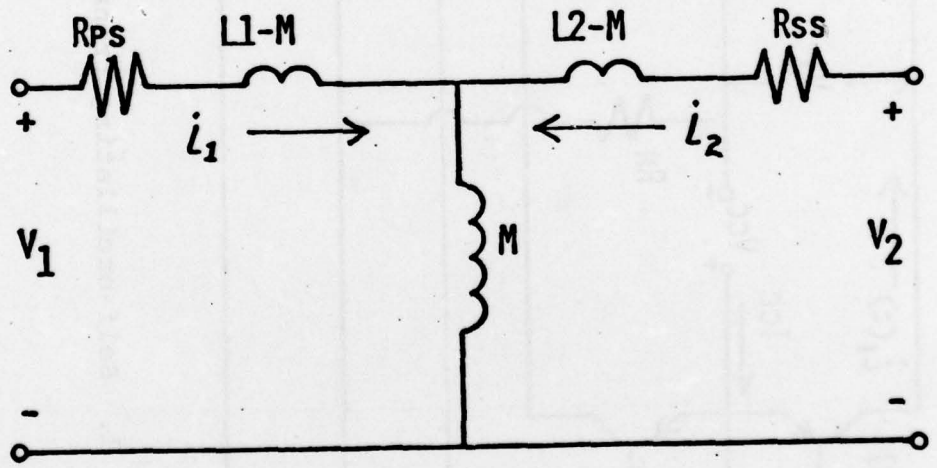

Figure 3. Transformer model 2.

L_1 = Primary inductance

L_2 = Secondary inductance

M = Mutual inductance

Equations 5 and 6 can also be obtained from the circuit shown in figure 3, making it mathematically equal to the circuit in figure 2. By introducing a variable, n, equations 5 and 6 can be rewritten as

$$V_1 = i_1 R_{ps} + L_1 \frac{di_1}{dt} + \frac{nM}{n} \frac{di_2}{dt} \qquad (7)$$

and

$$nV_2 = nM \frac{di_1}{dt} + \frac{n^2}{n} L_2 \frac{di_2}{dt} + \frac{n^2}{n} i_2 R_{ss} \quad . \qquad (8)$$

This results in the model in figure 4. If n is chosen as a value equal to the turns-ratio of the transformer,

$$n = N = \frac{N_1}{N_3} = (L_1/L_2)^{1/2} \quad . \qquad (9)$$

Figure 4 can now be redrawn as figure 5, where K is defined as the coupling coefficient and expressed as

$$K = \frac{M}{(L_1 L_2)^{1/2}} \leq 1 \quad . \qquad (10)$$

If a high value of K is assumed, figure 5 can be approximated by figure 6. With this as our model, expressions for voltage and current can now be developed.

The input voltage can be defined by figure 7. A description of the input current begins with the

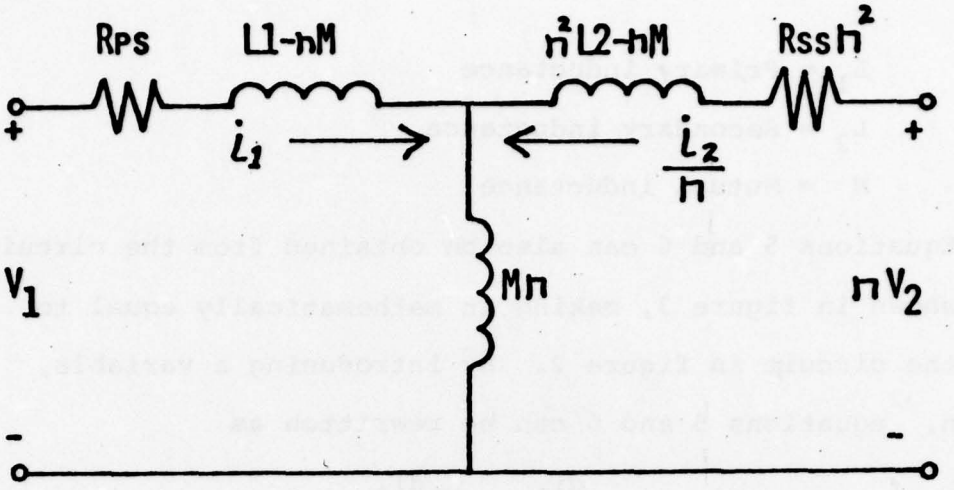

Figure 4. Transformer model (3).

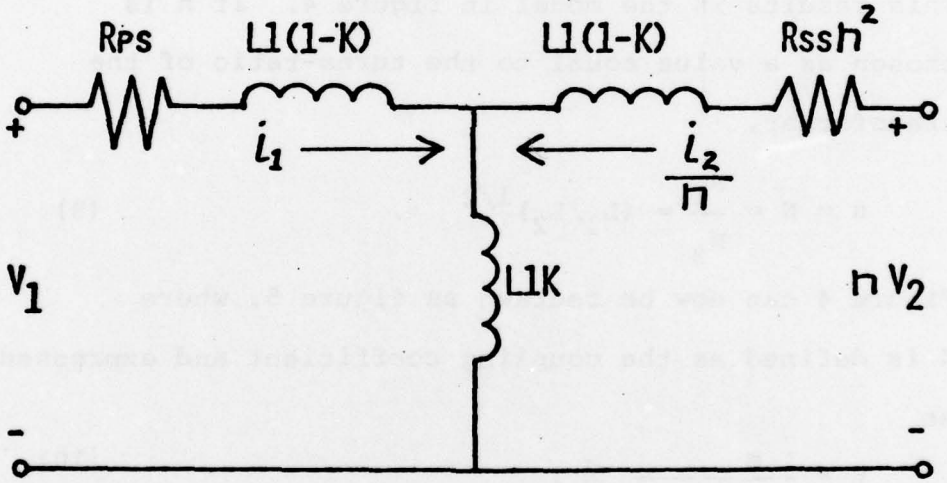

Figure 5. Transformer model (4).

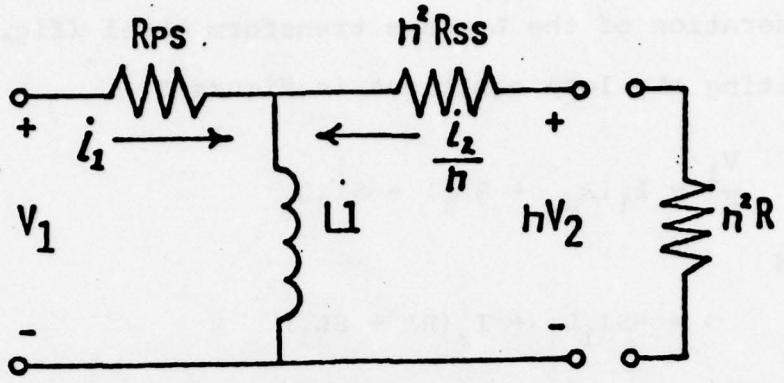

Figure 6. Approximated transformer model

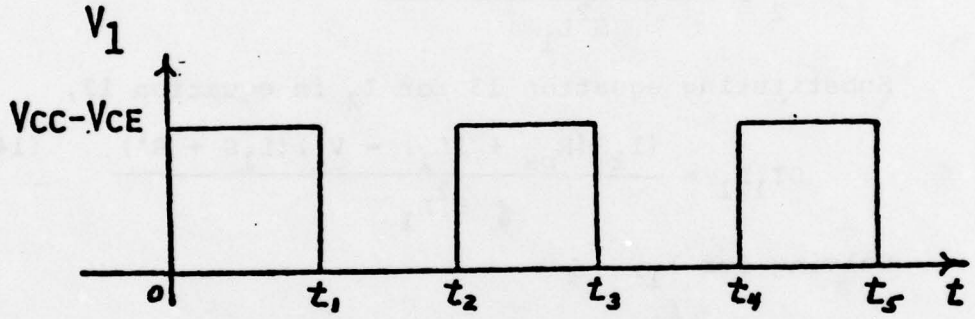

Figure 7. Input to figure 6.

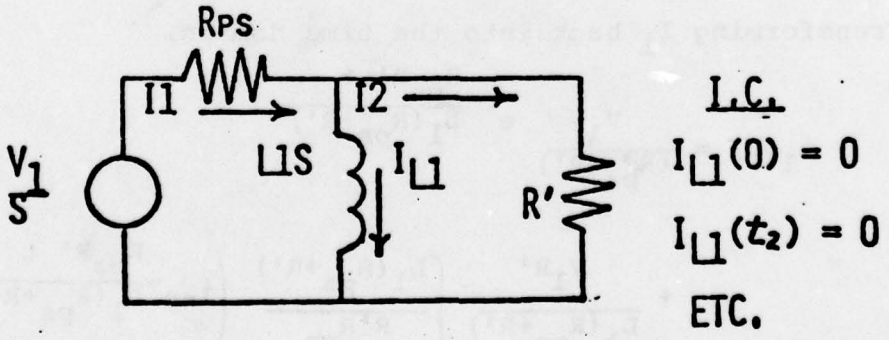

Figure 8. Laplace transform model of figure 6.

generation of the Laplace transform model (fig. 8).

Writing the loop equations in figure 8,

$$\frac{V_1}{S} = I_1(R_{ps} + SL_1) - SI_2L_1 \tag{11}$$

and

$$0 = -SI_1L_1 + I_2(R' + SL_1) \tag{12}$$

where $R' = N^2(R + R_{ss})$. We can now solve for I_2 in equation 11.

$$I_2 = \frac{I_1S(R_{ps} + SL_1) - V_1}{S^2L_1} \tag{13}$$

Substituting equation 13 for I_2 in equation 12,

$$SI_1L_1 = \frac{(I_1S(R_{ps} + SL_1) - V_1)(L_1S + R')}{S^2L_1} \tag{14}$$

Solving for I_1,

$$I_1 = \frac{V_1/(R_{ps} + R')}{S + \frac{R_{ps}R'}{L_1(R_{ps}+R')}} + \frac{V_1R'/L_1(R_{ps} + R')}{S\left(S + \frac{R_{ps}R'}{L_1(R_{ps}+R')}\right)} \tag{15}$$

Transforming I_1 back into the time domain,

$$i_1(t) = \frac{V_1}{(R_{ps}+R')} e^{-\frac{R_{ps}R' t}{L_1(R_{ps}+R')}} + \frac{V_1R'}{L_1(R_{ps}+R')}\left\{\frac{L_1(R_{ps}+R')}{R'R_{ps}}\left(1-e^{-\frac{R_{ps}R' t}{L_1(R_{ps}+R')}}\right)\right\} \tag{16}$$

yielding,

$$i_1(t) = \frac{V_1}{(R_{ps}+R')} \left\{ e^{-t/\tau} \left(1 - \frac{R_{ps}+R'}{R_{ps}} \right) + \frac{R_{ps}+R'}{R_{ps}} \right\} \tag{17}$$

where $\tau = \frac{L_1(R_{ps}+R')}{R_{ps}R'}$.

If we assume τ to be much greater than the switching period, $i_1(t)$ can be approximated by

$$i_1(t) = \frac{V_1}{R_{ps}+R'} \quad . \tag{18}$$

$i_1(t)$ is the magnitude of the current flowing through the saturated transistor in the direction indicated by figure 1. Since one transistor is on while the other is off, I_{cc} remains constant over the entire cycle and can be expressed as

$$I_{cc} = \frac{V_1}{R_{ps}+R'} \quad . \tag{19}$$

The current through the secondary is obtained by first substituting equation 15 for I_1 into equation 13 and solving for I_2:

$$I_2 = \frac{V_1}{R'+R_{ps}} \times \frac{1}{S + \frac{R_{ps}+R'}{L_1(R_{ps}+R')}} \tag{20}$$

Transforming I_2 back into the time domain,

$$i_2'(t) = \frac{V_1}{R_{ps}+R'} e^{-t/\tau} \quad . \tag{21}$$

If τ is again assumed to be much greater than the period, $i_2'(t)$ can be approximated by

$$i_2'(t) = \frac{V_1}{R_{ps}+R'} = i_2(t)/N \quad . \tag{22}$$

$i_2(t)$ is the magnitude of the current flowing through the secondary and changes direction with the switching of transistors Q_1 and Q_2. Since the output of the transformer is rectified (fig. 1), I_o can be assumed constant and equal to

$$I_o = \frac{V_1 N}{R_{ps}+R'} = \frac{N(V_{cc}-V_{cesat})}{R_{ps}+R'} \approx \frac{V_{cc}N}{R_{ps}+R'} \quad . \tag{23}$$

This allows the converter's efficiency to be expressed as

$$\text{Eff} = P_{out}/P_{in} = \frac{I_o^2 R}{V_{cc} I_{cc}} \quad . \tag{24}$$

Therefore,

$$\text{Eff} = \frac{V_{cc}^2 R N^2}{(R_{ps}+R')^2 \, V_{cc} \, (V_{cc}/(R_{ps}+R'))} \tag{25}$$

yielding

$$\text{Eff} = \frac{RN^2}{N^2(R+R_{ss}) + R_{ps}} \quad . \tag{26}$$

The voltage and current gains follow as

$$A_v = \frac{I_o R}{V_{cc}} = \frac{NV_{cc}R}{(R_{ps}+R')V_{cc}} = \frac{NR}{N^2(R+R_{ss}) + R_{ps}} \tag{27}$$

and

$$A_i = I_o/I_{cc} = \frac{NV_{cc}}{R_{ps}+R'} \times \frac{R_{ps}+R'}{V_{cc}} = N \quad . \qquad (28)$$

Eff and Av are plotted (figs. 9 and 10) with $R_{ps} = R_{ss} = 0.2$ ohms. The plots are made through the use of a Fortran program and Calcomp Plotter. Figures 9 and 10 demonstrate the dependence of voltage gain and efficiency on both load and turns-ratio. Investigation of the plots shows that highest efficiency results during periods of low voltage gain and high current gain.

The self oscillating transformer-coupled converter is therefore more efficiently used for voltage step down applications. Used in this role, it provides the designer good input/output isolation and high efficiency. Its disadvantages include the necessity of choosing a core with the proper flux vs. current characteristic, core loss, increased weight, and development of electromagnetic interference (EMI) due to fast transistor switching.

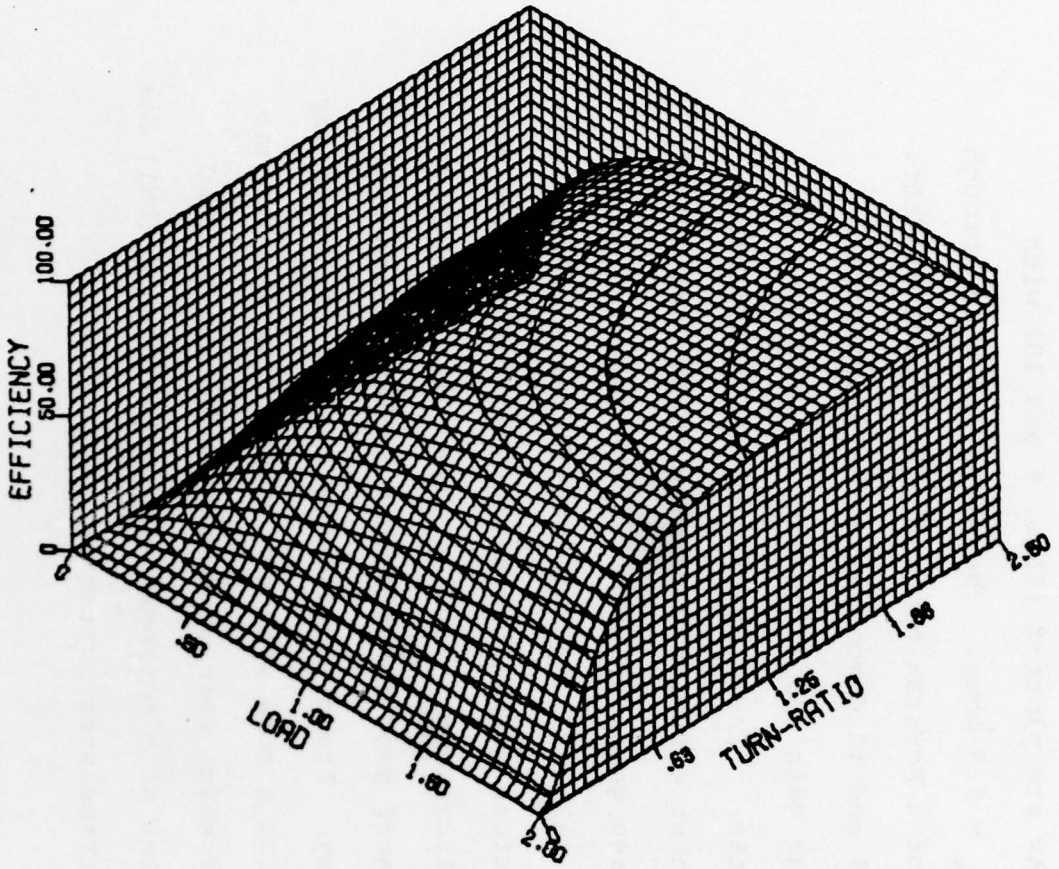

Figure 9. Transformer coupled efficiency

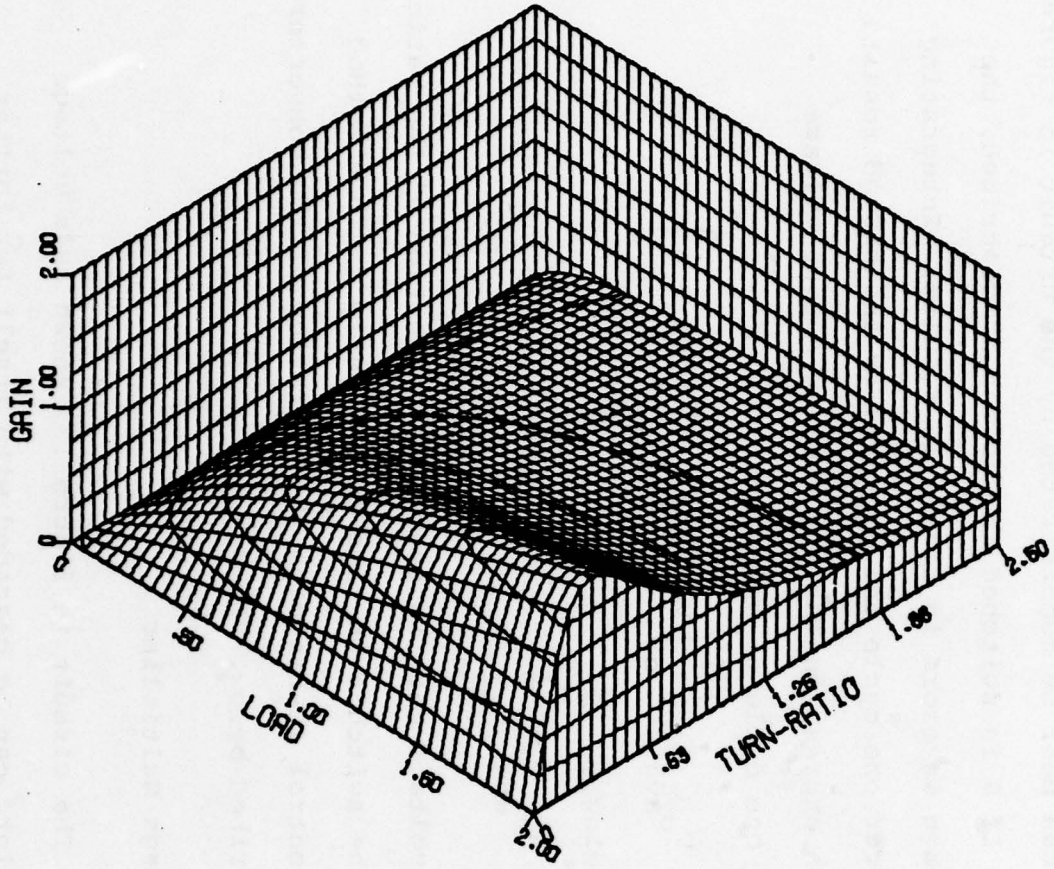

Figure 10. Transformer coupled voltage gain

Time Ratio Control

In the four converters remaining, a method of regulation known as time ratio control (TRC) determines the average voltage and current gains of the circuit.[7] TRC can best be demonstrated by the circuit in figure 11. If S is switched in the manner described, the voltage waveform in figure 12 results. Integrating V_o over one cycle and dividing by the period results in an expression for the average output voltage over one cycle of operation:

$$V_{o_{avg}} = \frac{1}{T}\int_o^T Vdt = \frac{1}{T}\left\{\int_o^{t_1} Vdt + o\right\} = \frac{Vt_1}{T}$$

Yielding,

$$A_{v_{avg}} = \frac{t_1}{T} \quad .$$

The voltage gain is therefore a function of the ratio of the switch's on-time to the period. This method of control is basic to the operation of the converters described below.

Voltage Multiplier

The circuit in figure 13, known as a voltage doubler, can be cascaded with itself for further voltage multiplication.[8] Such an n-Tupler is depicted in figure 14. With its input as shown,

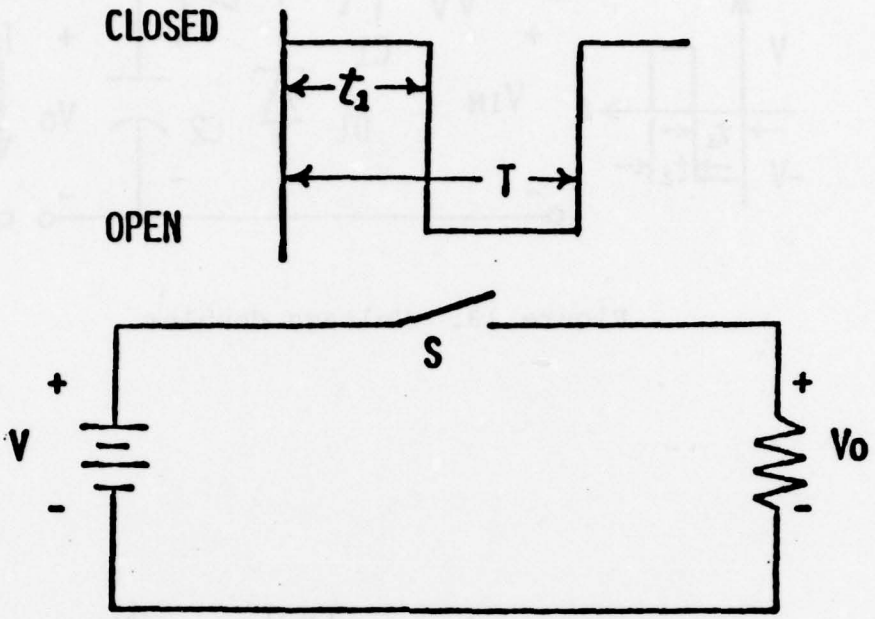

Figure 11. TRC controlled circuit

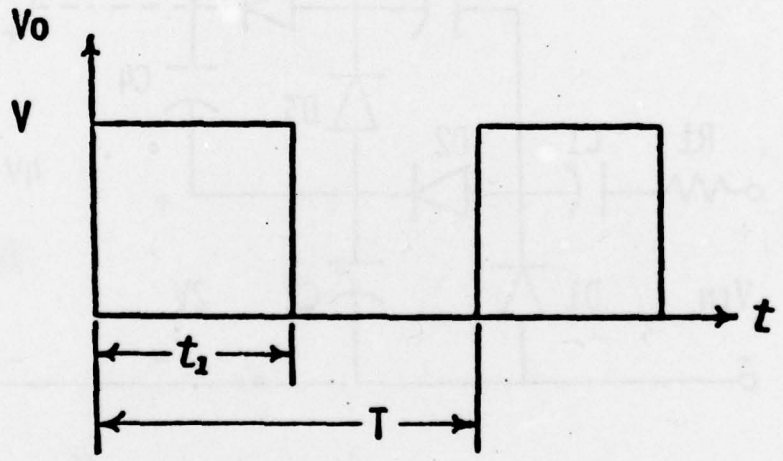

Figure 12. Output of figure 11.

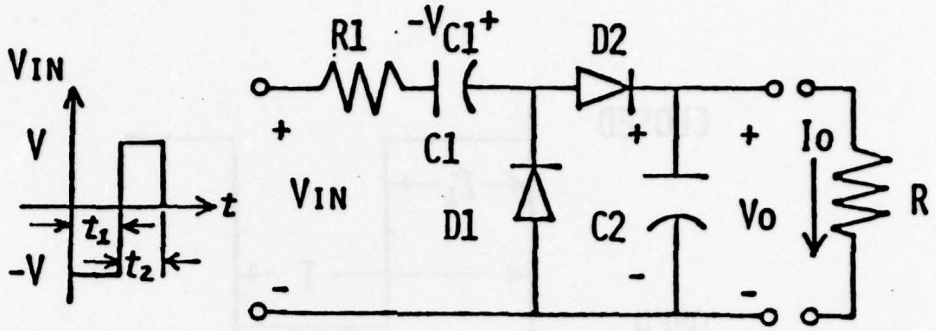

Figure 13. Voltage doubler

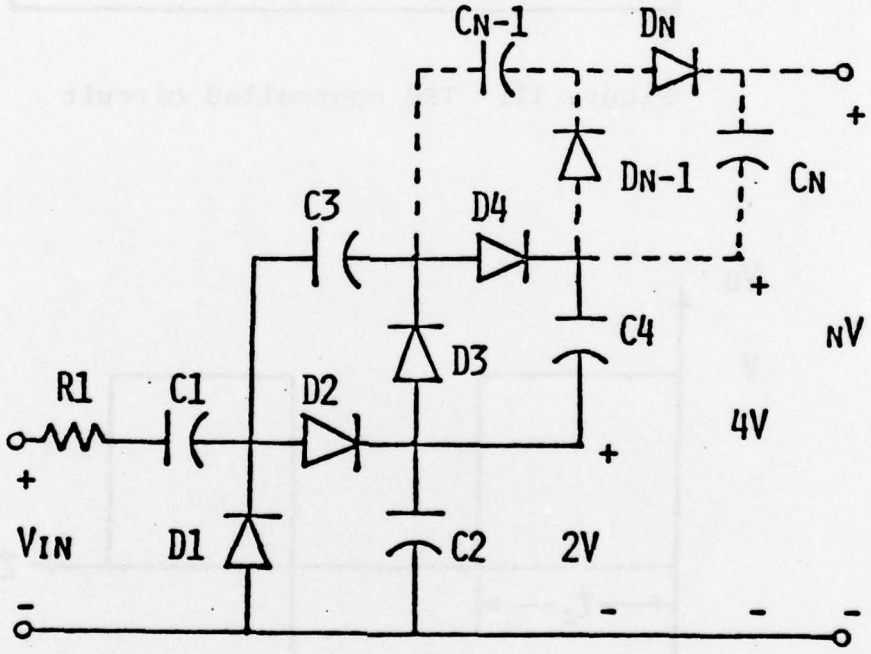

Figure 14. Voltage n-tupler

the doubler's operation is as follows: When V_{in} is negative, D_1 is forward biased and D_2 is open. C_1 charges to V with the polarity indicated and C_2 discharges slowly through the load. As V_{in} goes positive, D_1 becomes reverse biased and D_2 is turned on. At this point, C_2 charges to a value of $V+V_{C1}$. The cycle is then repeated, maintaining the voltage across C_2 at 2V.

In the steady state analysis of the circuit, it is assumed that the average voltage across the capacitors is constant, and the average current through them is zero. The period of switching is also assumed to be much less than the time constant of the output circuit, but much greater than the time constant which charges up C_1. With this in mind, the circuit's analysis can begin by saying that the average power supplied over one cycle is equal to the average power absorbed over that cycle. Therefore,

$$\begin{aligned} P_1(-V)(I_1)+P_2(V)(I_2) &= R_1(I_1)^2P_1+R_1(I_2)^2P_2 \\ &+ P_1(-V_{C1})I_1 + P_2(-V_{C1})I_2 \\ &+ P_1V_oI_{C2_1} + P_2V_oI_{C2_2} + P_{out} \end{aligned} \qquad (29)$$

where $P_1 = t_1/T$, $P_2 = t_2/T$, and $T = t_1+t_2$. I_1 and I_{C2_1} are currents which flow when V_{in} is negative, while I_2 and I_{C2_2} flow when V_{in} is positive. Since the average

current through C_1 and C_2 equals zero,

$$P_1I_1+P_2I_2 = 0 \text{ and } P_1I_{C2_1}+P_2I_{C2_2} = 0 \ . \tag{30}$$

By assuming V_{C1} to be essentially constant, equation 29 can be rewritten as

$$V(P_2I_2-P_1I_1) = R_1(P_1I_1^2+P_2I_2^2) + P_{out}. \tag{31}$$

Dividing by the left-hand side of the equation,

$$Eff_{avg} = 1 - \frac{R_1(P_1I_1^2+P_2I_2^2)}{V(P_2I_2-P_1I_1)} \ . \tag{32}$$

Since the average current through C_2 equals zero, $I_{o_{avg}} = P_2I_2$. With I_o assumed constant, $I_{o_{avg}} = I_o$ and,

$$Eff_{avg} = 1 - \frac{R_1I_2}{2VP_1} = 1 - \frac{R_1I_o}{2VP_1P_2} \tag{33}$$

Yielding

$$Eff_{avg} = 1 - \frac{R_1V_o}{2VRP_1P_2} \ . \tag{34}$$

When V_{in} is positive,

$$V = I_2R_1 - V_{C1} + V_o \ . \tag{35}$$

When V_{in} is negative,

$$-V = I_1R_1 - V_{C1} \ . \tag{36}$$

With V_{C1} constant over the entire cycle, equations 35 and 36 can be solved simultaneously for V yielding

$$V = \frac{R_1I_2}{2P_1} + \frac{V_o}{2} \ . \tag{37}$$

Substituting equation 37 into equation 34,

$$Eff_{avg} = 1 - \frac{R_1 V_o}{R P_1 P_2 \frac{(R_1 I_2 + V_o)}{P_1}} \tag{38}$$

Yielding

$$Eff_{avg} = \frac{R P_1 P_2}{R_1 + P_1 P_2 R} \quad . \tag{39}$$

The average voltage gain can be expressed by

$$A_{v_{avg}} = \frac{V_o}{V} = \frac{2V_o P_1}{R_1 I_2 + V_o P_1} = \frac{2V_o P_1}{\frac{R_1 V_o}{R P_2} + P_1 V_o}$$

Since $\frac{V_o}{R} = I_o = P_2 I_2$,

$$A_{v_{avg}} = \frac{2 P_1 P_2 R}{R_1 + P_1 P_2 R} \quad . \tag{41}$$

The average current gain follows as

$$A_{i_{avg}} = \frac{I_o}{P_1 I_1 + P_2 I_2} = \frac{P_2 I_2}{2 P_2 I_2} = \frac{1}{2} \quad . \tag{42}$$

Figures 15 through 18 represent the output of a computer simulation using the circuit analysis program SCEPTRE.[9] The program was run at different duty cycles with $V_{in} = \pm$ 10 V, $C_1 = C_2 = 10$ uf, $R_1 = 1$ ohm, $R = 100$ ohms, and a frequency of 100 KHZ. The program's output serves to confirm the results of equations 39 and 41. The equations themselves have been plotted in figures 19 and 20 with $R_1 = 0.2$ ohms. The contour plots of figures 19 and 20 demonstrate the dependency of voltage gain and efficiency

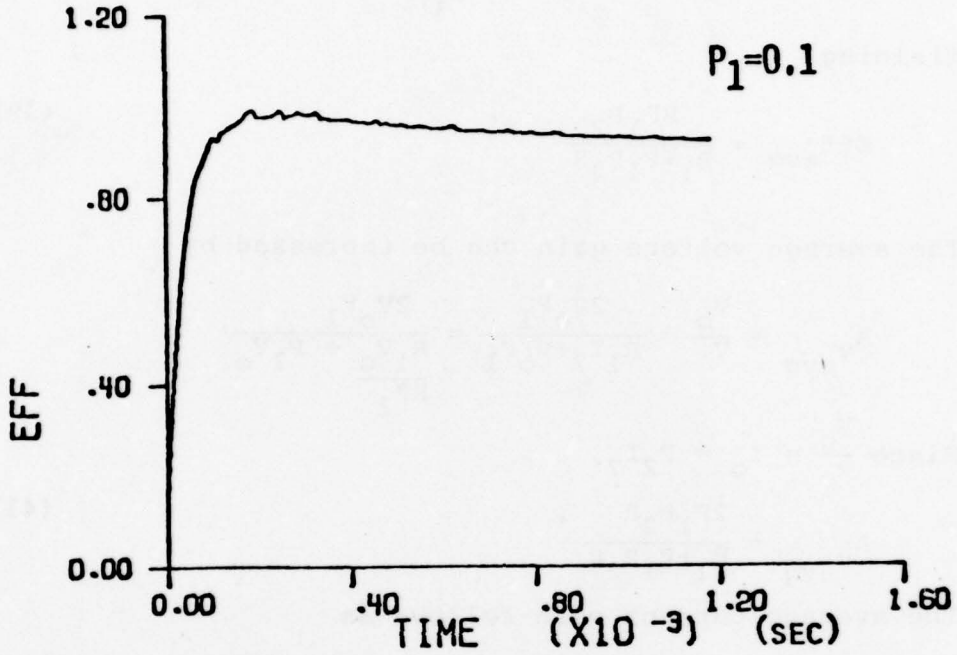

Figure 17. Doubler efficiency (P_1=0.1)

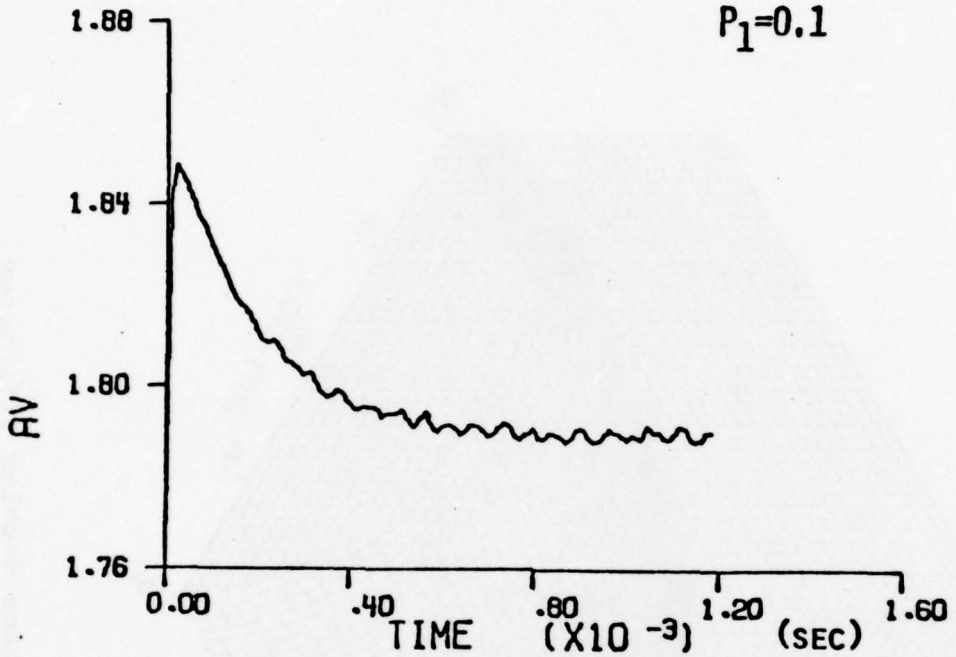

Figure 18. Doubler voltage gain (P_1=0.1)

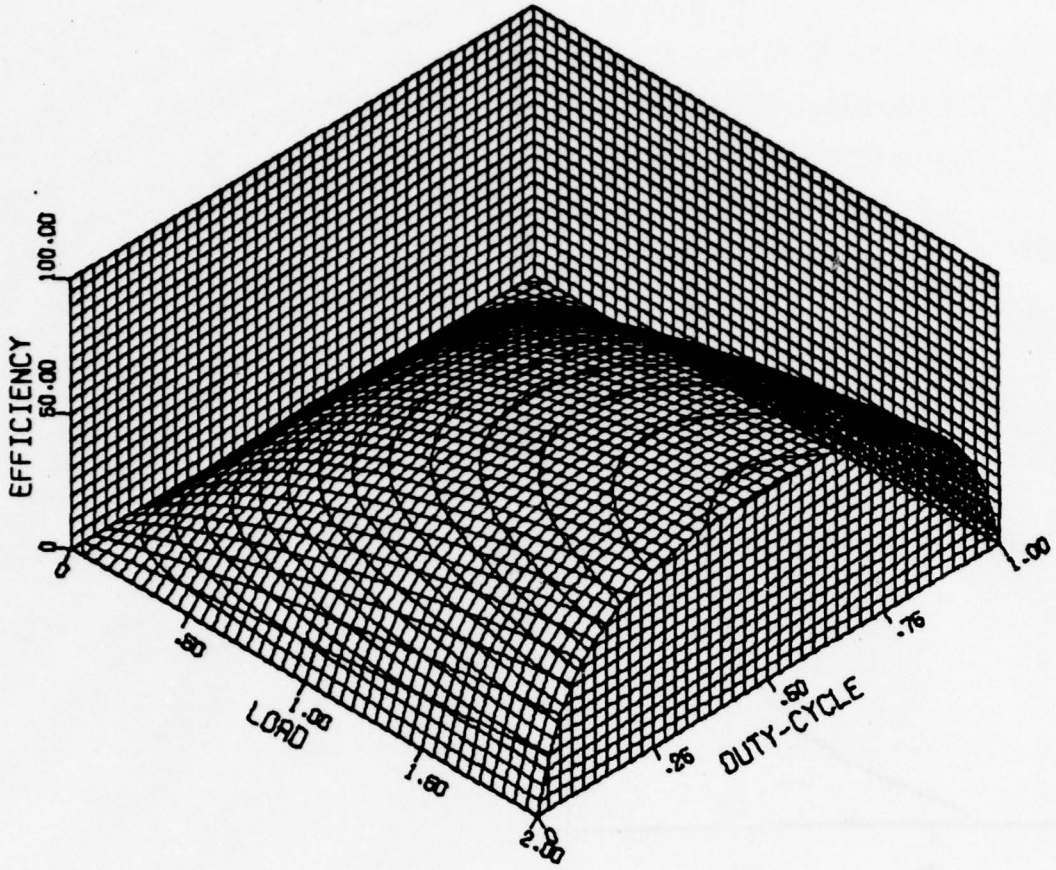

Figure 19. Voltage doubler efficiency

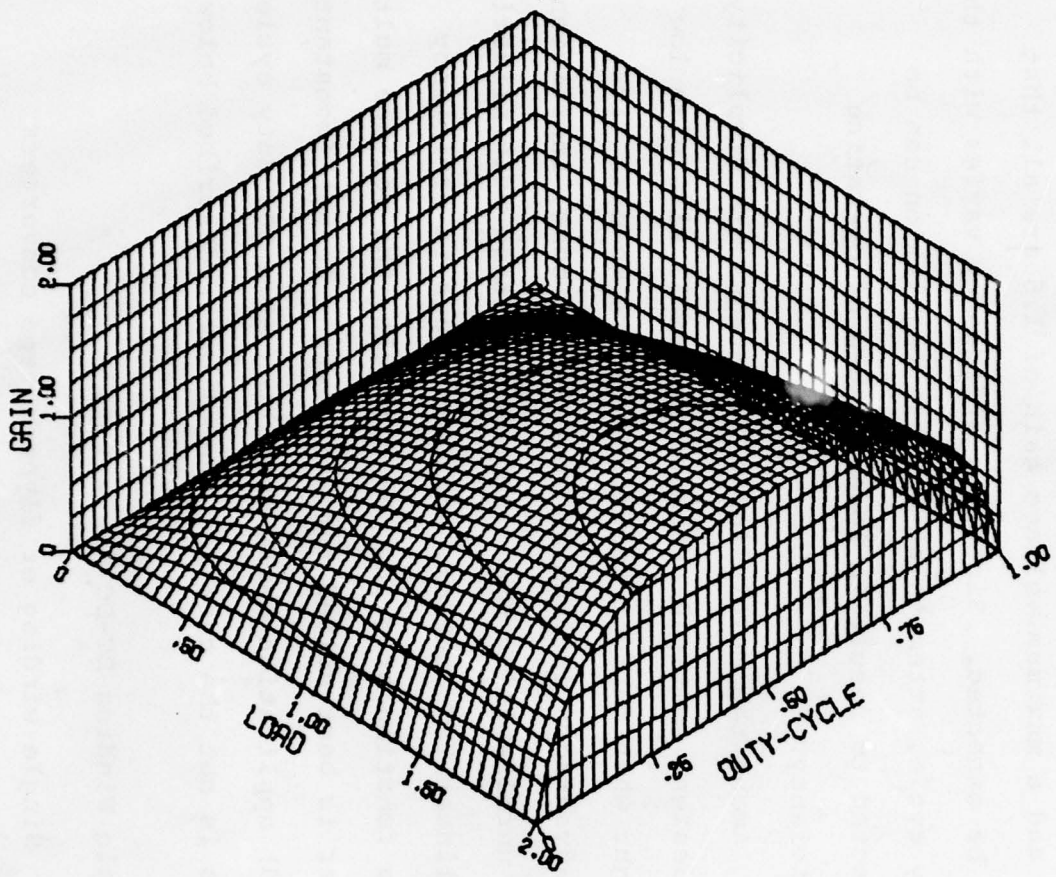

Figure 20. Voltage doubler voltage gain

on duty cycle and load. They also indicate the maximum values of efficiency and voltage gain which can be expected with a series resistance of 0.2 ohms. At a load resistance of 2 ohms, a maximum efficiency of 70% and a maximum voltage gain of 1.5 are all that can be expected. Since the efficiency varies with the duty cycle, attempts at voltage regulation can be expected to result in lower values of operating efficiency.

Among the multiplier's advantages are simplicity of design, multiple outputs, and small size with low weight when current requirements are modest. Its disadvantages include an increase in cost, inefficiency, and unreliability with increased voltage multiplication, nonlinear TRC control, and variations in efficiency as a function of gain. As a result, the voltage multiplier is best suited for a (constant input)/(constant load) application while operating at a 50% duty cycle. This is not the case for the circuits described below.

Single Winding DC-DC Converters

Single winding or flyback type converters (figs 21 through 23) all share a transistor, capacitor, inductor, and diode as basic circuit elements.[10] In the AC steady state analysis of these circuits, the

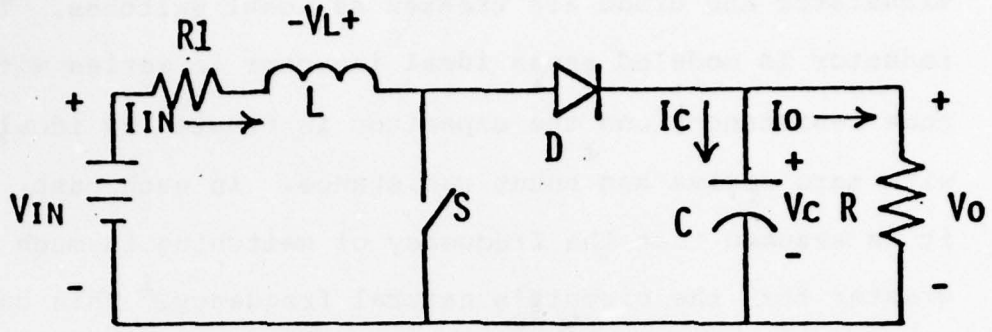

Figure 21. Voltage boost converter

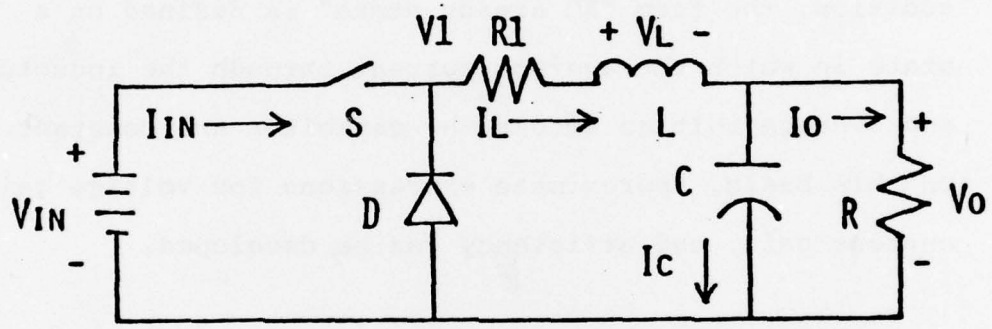

Figure 22. Current boost converter

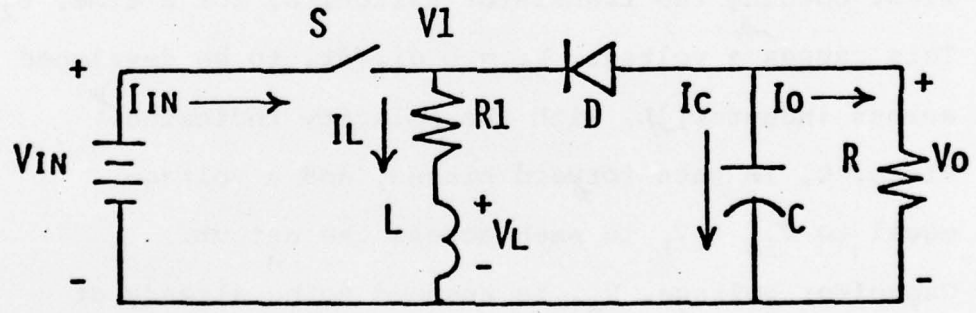

Figure 23. Voltage/current boost converter

transistor and diode are treated as ideal switches. The inductor is modeled as an ideal inductor in series with some resistance, and the capacitor is treated as ideal with zero series and shunt resistance. In each case, it is assumed that the frequency of switching is much greater than the circuit's natural frequency. This causes current ripple through the inductor and voltage ripple across the capacitor to be considered negligible. In addition, the term "AC steady state" is defined as a state in which the average current through the inductor and average voltage across the capacitor are constant. On this basis, approximate expressions for voltage gain, current gain, and efficiency can be developed.

Voltage Boost Converter

The voltage-boost converter (fig 21) operates by first opening the transistor switch, S, for a time, t_2. This causes a voltage, $V_L = L\ di_L/dt$, to be developed across inductor, L, with the polarity indicated. Diode, D, is then forward biased, and a voltage equal to $V_{in} + V_L$ is seen across the output. Capacitor voltage, V_c, is assumed to be already at that approximate value from the previous cycle. When S is closed for time t_1, diode D becomes open and V_L goes negative. During this time, the output voltage

and inductor current are assumed to remain constant with the exception of some negligible ripple. With $P_1=t_1/T$, $P_2=t_2/T$, and $T=t_1+t_2$, an expression for the average efficiency over one cycle can be developed. Since R_1 is the only source of loss,

$$Eff_{avg} = 1 - \frac{I_{in}^2 R_1}{V_{in} I_{in}} \tag{43}$$

or

$$Eff_{avg} = 1 - \frac{R_1}{(V_{in}/I_{in})} \quad . \tag{44}$$

The following equations are developed from the circuit in fig. 21 with V_{in}, I_{in}, V_o, and I_o assumed to be constant.

$$V_{in} = I_{in}R_1 + (V_L)_{avg} + P_2V_o \tag{45}$$

$$I_o = P_2I_{in} - (I_c)_{avg} \tag{46}$$

Since $(V_L)_{avg}$ and $(I_c)_{avg}$ are equal to zero,

$$V_{in} = I_{in}R_1 + P_2V_o, \tag{47}$$

and

$$I_o = P_2I_{in} \quad . \tag{48}$$

This results in

$$\frac{V_{in}}{I_{in}} = R_1 + \frac{P_2^2V_o}{I_o} \tag{49}$$

Since $V_o/I_o = R$,

$$\frac{V_{in}}{I_{in}} = R_{in} = R_1 + P_2^2R, \tag{50}$$

where R_{in} is the input resistance seen by the source.

Substituting into equation 44,

$$Eff_{avg} = \frac{R}{R+(R_1/P_2^2)} \quad . \tag{51}$$

The voltage gain can be expressed by

$$Av = (I_o R)/(R_{in} I_{in}) = P_2 I_{in} R / I_{in} R_{in} \tag{52}$$

Yielding

$$A_v = \frac{P_2 R}{R_{in}} = \frac{P_2 R}{R_1 + P_2^2 R} \quad . \tag{53}$$

Finally, the current gain results from equation 48 as

$$A_i = \frac{I_o}{I_{in}} = P_2 \quad . \tag{54}$$

Equations 51 and 53 are plotted in figures 24 and 25 with R_1 equal to 0.2 ohms. The plots indicate the dependence of both efficiency and gain on load and duty cycle. They also point out that areas of greater than 80% efficiency only exist for duty cycles between 65% and 100%. This range in duty cycle limits the regulator's ability to react to transient conditions while offering something less than the maximum gain of 1.25. High efficiency operation and maximum voltage regulation are therefore not concurrently available with the voltage boost DC-DC converter.

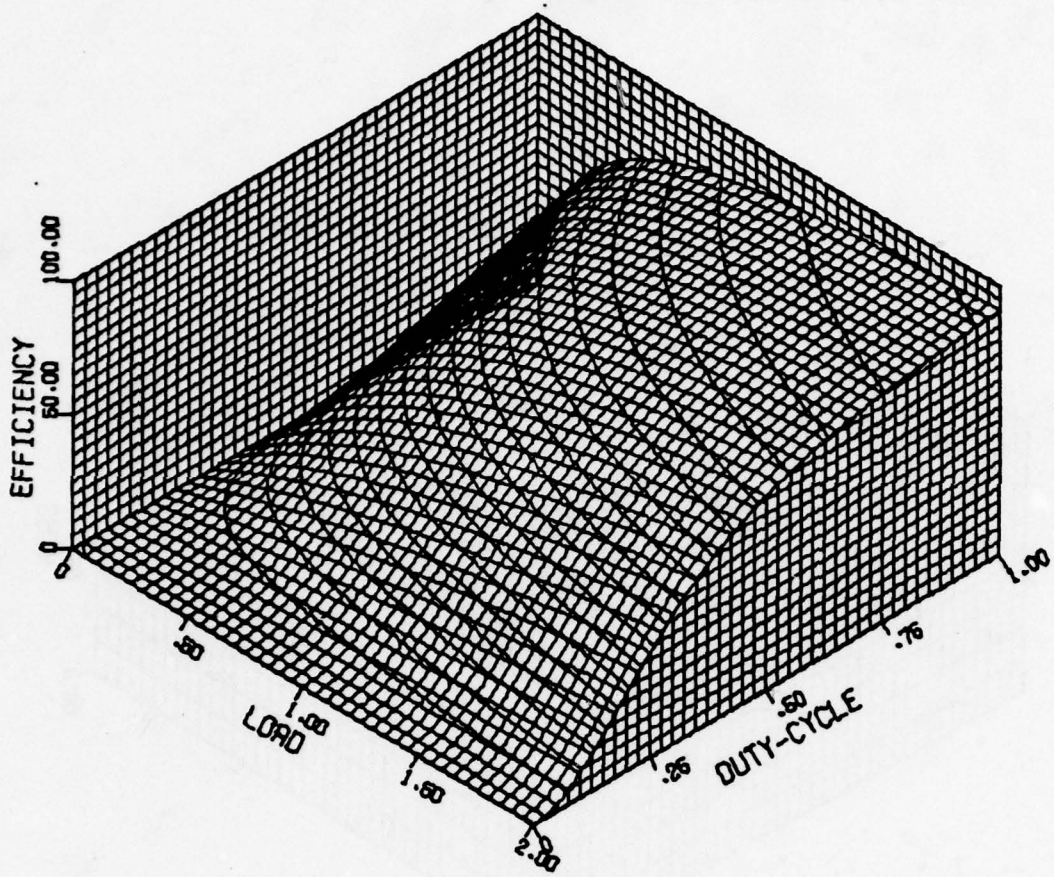

Figure 24. Voltage boost efficiency

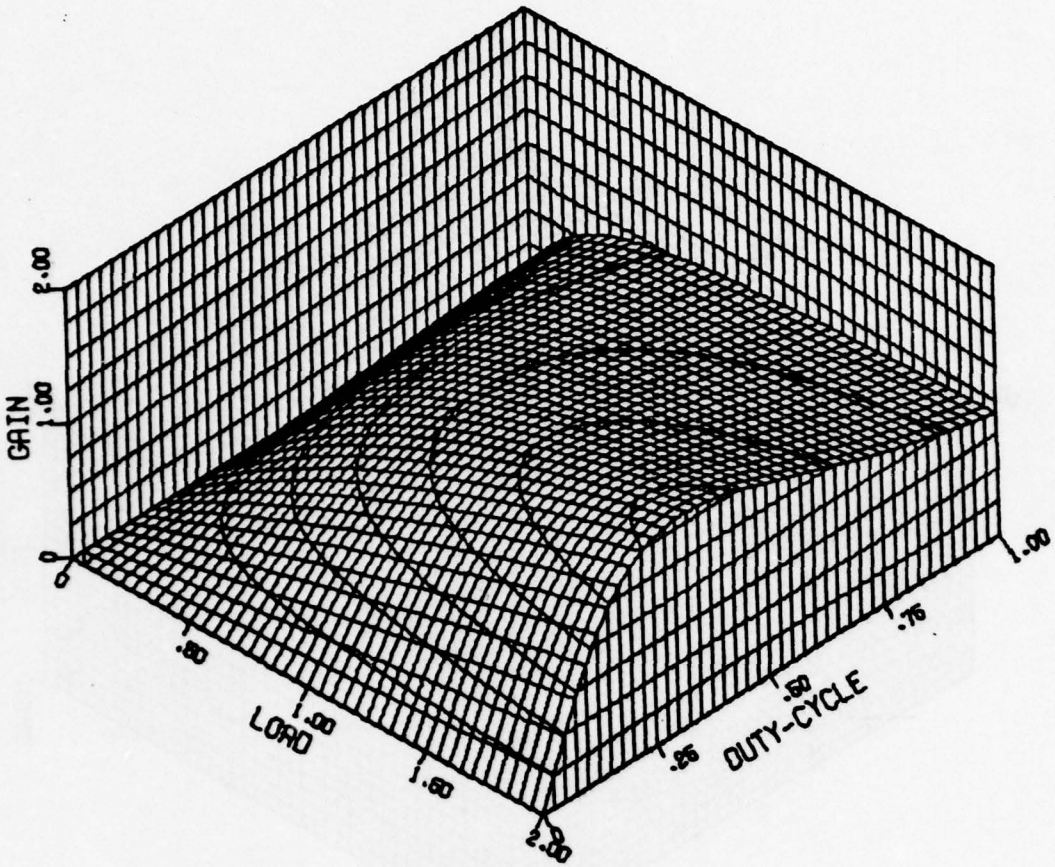

Figure 25. Voltage boost voltage gain

Current Boost Converter

The current boost converter (fig. 22) earns its name by being able to supply more average current than it absorbs. Its AC steady state operation can be explained as follows: With switch S, closed for time t_1, diode D becomes reverse biased, and current flows from the input through inductor L to the parallel combination of R and C. When S is open for time t_2, diode D conducts allowing the constant current of inductor, L, to flow to the R and C combination. Of course, the inductor current and capacitor voltage are really only approximately constant with some negligible ripple present. With $P_1=t_1/T$, $P_2=t_2/T$, and $T=t_1+t_2$, the following relations can be developed.

$$V_{l_{avg}} = P_1 V_{in}$$

$$V_{l_{avg}} = I_L R_1 + (V_L)_{avg} + I_o R$$

$$I_L = I_{c_{avg}} + I_o$$

$$I_{in_{avg}} = P_1 I_L .$$

Since $I_{c_{avg}}$ and $(V_L)_{avg}$ equal zero, the average current gain becomes

$$A_{i_{avg}} = \frac{I_o}{I_{in_{avg}}} = \frac{I_o}{P_1 I_L} = \frac{1}{P_1} \quad . \tag{55}$$

The voltage gain can be expressed by

$$Av = \frac{V_o}{V_{in}} = \frac{RI_o}{V_{l_{avg}}/P_1} = \frac{P_1 I_o R}{V_{l_{avg}}} \tag{56}$$

Yielding

$$A_v = \frac{P_1 R}{R+R_1} = \frac{R(1-P_2)}{R+R_1} \quad . \tag{57}$$

The average efficiency can now be expressed as

$$Eff_{avg} = A_v \, A_{i_{avg}} = \frac{R}{R+R_1} \quad . \tag{58}$$

Equations 57 and 58 are plotted (figs. 26 and 27) with R_1 = 0.2 ohms. Unlike the voltage boost converter, the plot in figure 26 indicates a linear regulating capability with a slope independent of duty cycle. In addition, the efficiency plot of figure 27 is independent of duty cycle and climbs to a value of 90% for high values of load resistance. The current boost converter therefore offers good regulation without sacrificing operating efficiency.

Voltage/Current Boost Converter

The converter of fig. 23 has a combination voltage and current boost capability. The circuit acts as one type of converter or the other depending on the duty cycle at which it is operating. When switch S is closed, diode D is reverse biased and the input current flows through inductor L for time t_1. The voltage across capacitor C is assumed to remain essentially constant during this part of the cycle. When S is opened for time t_2, diode D becomes forward biased allowing "constant

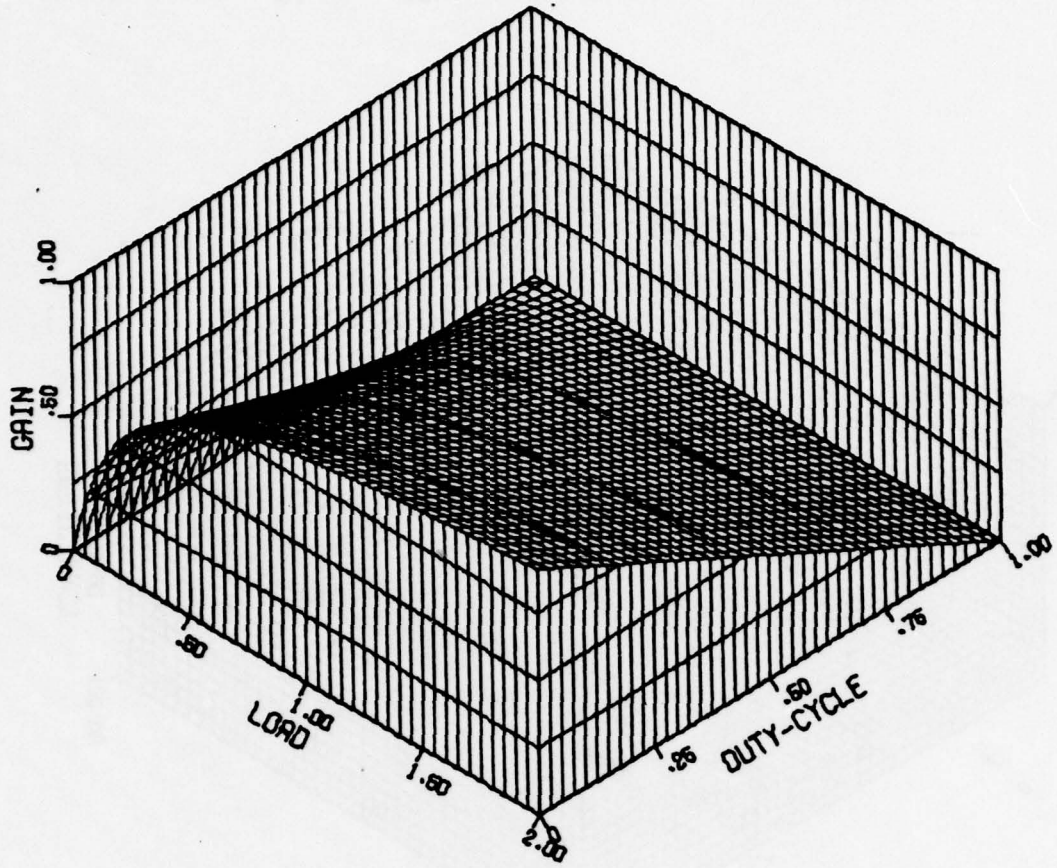

Figure 26. Current boost voltage gain

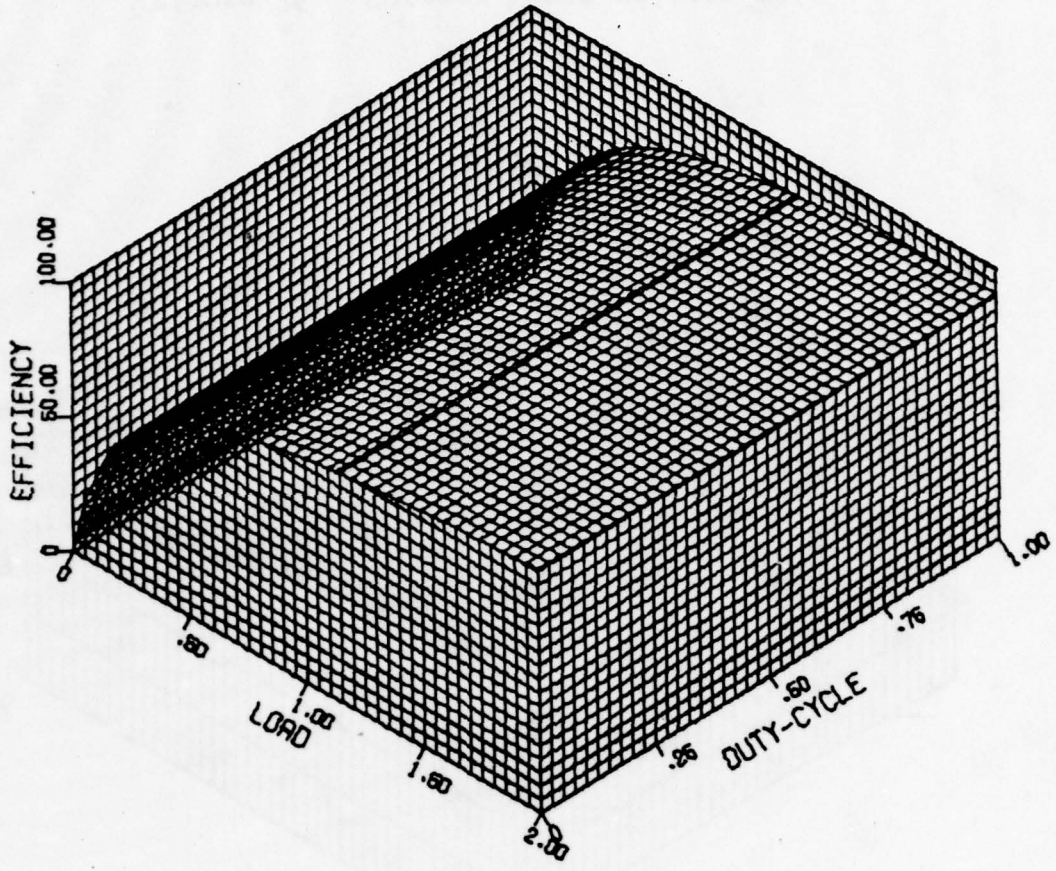

Figure 27. Current boost efficiency

current", I_L, to flow into the R and C combination. Again, $P_1=t_1/T$, $P_2=t_2/T$, and $T=t_1+t_2$. As a result the following expressions can be developed:

$$V_{l_{avg}} = P_1 V_{in} - P_2 V_o = I_L R_1 + (V_L)_{avg} \tag{59}$$

$$I_{in_{avg}} = P_1 I_L$$

and

$$I_o = -I_{c_{avg}} - P_2 I_L$$

Since $(V_L)_{avg}$ and $I_{c_{avg}}$ equal zero, $I_o = -P_2 I_L$ and $V_{l_{avg}} = I_L R_1$. Solving for V_{in} in equation 59,

$$V_{in} = \frac{I_L R_1 + P_2 V_o}{P_1} \quad . \tag{60}$$

An expression for the absolute voltage gain results as

$$|A_v| = \frac{|V_o|}{|V_{in}|} = \frac{|-I_o R\ P_1|}{|I_L R_1 + P_2 V_o|} \quad . \tag{61}$$

Since $I_L = \frac{-I_o}{P_2}$, and $V_o = -I_o R$,

$$|A_v| = \frac{P_1 P_2 R}{R_1 + P_2^2} = \frac{(1-P_2) P_2 R}{R_1 + P_2^2 R} \tag{62}$$

the average current gain is expressed as

$$|A_{i_{avg}}| = \frac{|-I_o|}{|I_{inavg}|} = \frac{P_2 I_L}{P_1 I_L} = \frac{P_2}{P_1} \quad . \tag{63}$$

The average efficiency can now be expressed as

$$Eff_{avg} = |A_v| \; |A_{i_{avg}}| = \frac{P_2^2 R}{R_1 + P_2^2 R} \qquad (64)$$

Equations 62 and 64 are plotted in figures 28 and 29 respectively with R_1 set equal to 0.2 ohms. The plots are very similar to those of the voltage boost converter exhibiting the same dependence of efficiency on duty cycle. This results in an undesirable linkage between efficiency, voltage gain, and voltage regulation. It is undesirable because high voltage gain and high efficiency do not occur concurrently. The converter is therefore most efficiently used as a current gain device which cannot offer as good a regulating capability as the current boost converter previously discussed.

The single winding type of DC-DC converter provides high reliability independent of load requirements, a good TRC regulation capability and, in the case of the current boost converter, high efficiency independent of duty cycle. In addition, it offers the option of using an air core instead of a lossy iron core in the inductor. Its disadvantages include the generation of electromagnetic interference and the existence of high frequency spikes on the output.

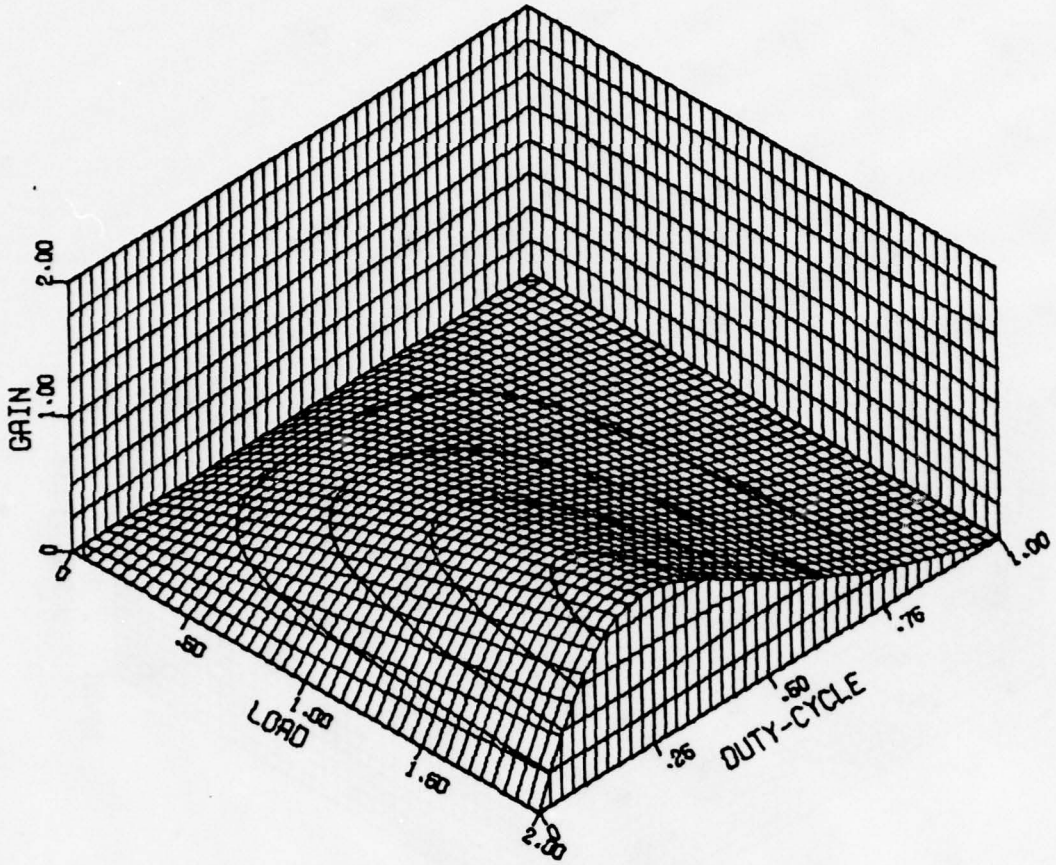

Figure 28. Voltage/current boost voltage gain

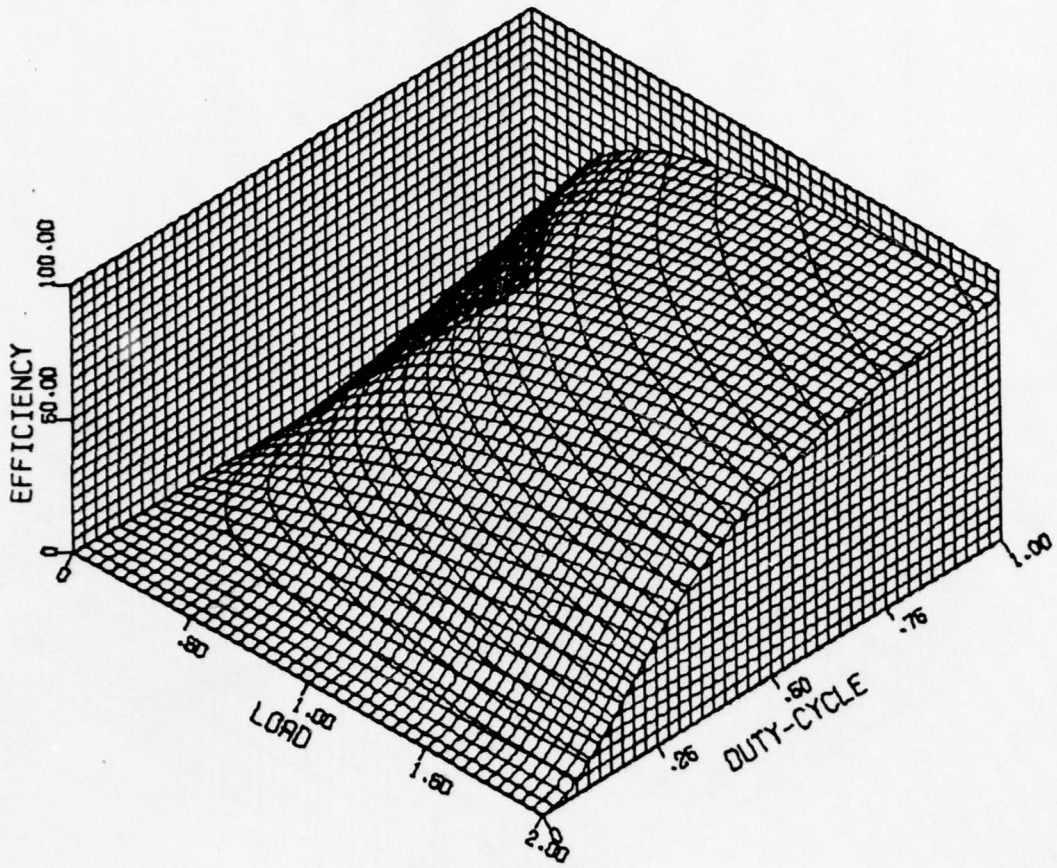

Figure 29. Voltage/current boost efficiency

This completes the discussion of some of the more popular types of DC-DC converters. With regard to efficiency and regulation, the current boost type of converter best satisfies the requirements of the solar energy application proposed. A more detailed discussion follows.

DESIGN & CONSTRUCTION OF A SERIES SWITCHING REGULATOR

Choosing a DC-DC Converter

Five DC-DC converters have been presented. The major considerations in determining which of these is best suited for a solar energy application are efficiency and regulation. Solar panels and lead acid storage batteries produce nominal voltages which vary by $\pm$ 15%. Since the turns-ratio of the transformer type of converter is constant,it reflects any percentage of change in input voltage directly to the output. If, for example, an output of 12 V is desired, a 15% change in the input results in a 1.8 V change in the output. This unacceptable change in output makes the transformer type of converter unable to meet the requirements of the proposed solar energy application.

The voltage multiplier, unlike the transformer type of converter, can be time ratio controlled, and can adjust its voltage gain to accommodate changes in

input voltage. Its efficiency, however, varies directly as a function of voltage gain. The result is that nominal operation must occur at an efficiency other than the maximum. This is best described by the plot in figure 20. For a load of 2 ohms, a $\pm$ 15% change in input can only be accommodated if a nominal voltage gain of approximately 1.25 or less is established. At this gain, a duty cycle of approximately 0.25 is needed. The plot in figure 19, shows that a duty cycle of 0.25 produces an operating efficiency of 65%. This value is unacceptable and eliminates the voltage multiplier as a candidate for the application proposed.

Of the three single winding circuits presented, only the current boost type allows the entire range of duty cycle to be used for regulation without experiencing a decrease in efficiency. Such a characteristic is desirable because it allows the accommodation of a greater variety of steady state input and output combinations. Nominal operation can also be centered in the 50% duty cycle area allowing maximum regulation to occur during transient conditions. On this basis, the current boost circuit is felt to be the best DC-DC converter available for the solar application proposed.

As seen from figure 26, if nominal operation is to occur at a duty cycle of 50%, a voltage gain of approximately 50% must first be established. Since storage batteries are most readily available at a value of 12 V, the realization of a 24 V supply is not difficult. With a supply of 24 V and a duty cycle of 50% representative of nominal operation, an analysis can be performed for the nominal case.

Steady State AC Response

The current boost circuit (fig. 22) is often referred to as a series switching regulator. Its main purpose is to filter the high frequency components of an AC signal generated by the switching of a transistor in series with a DC supply. The result is a DC output accompanied by some unfiltered AC which is referred to as RIPPLE. The magnitude of the ripple can be specified by choosing the proper values of inductance and capacitance. To accomplish this, voltage V_1 (fig 30) must first be approximated by the following Fourier series:

$$V_1(t)=12+\sum_{n=1}^{\infty} \frac{24}{n\pi}\left\{1-\cos(n\pi)\right\} \sin(2n\pi t/T) \quad n=1,3,5,\ldots \tag{65}$$

The generation of equation 65 is described in appendix B. Since V_1's fundamental frequency con-

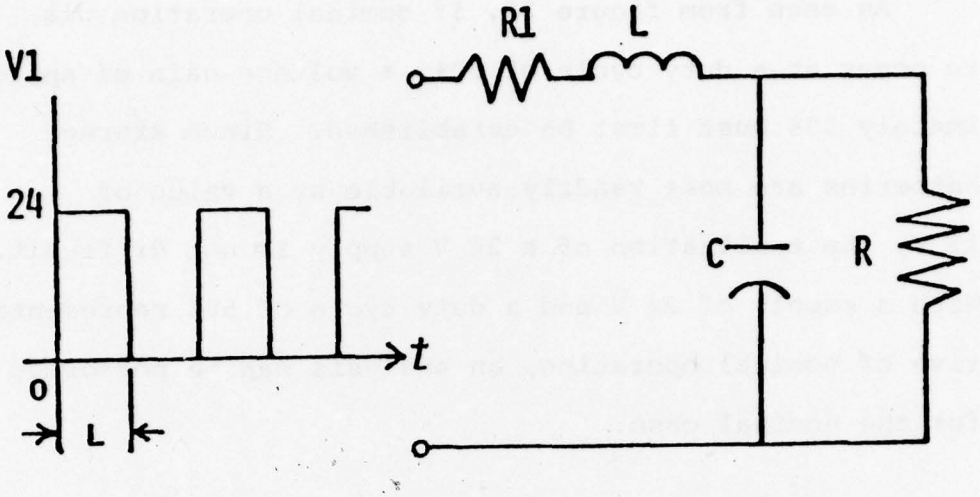

Figure 30. Regulator filter circuit

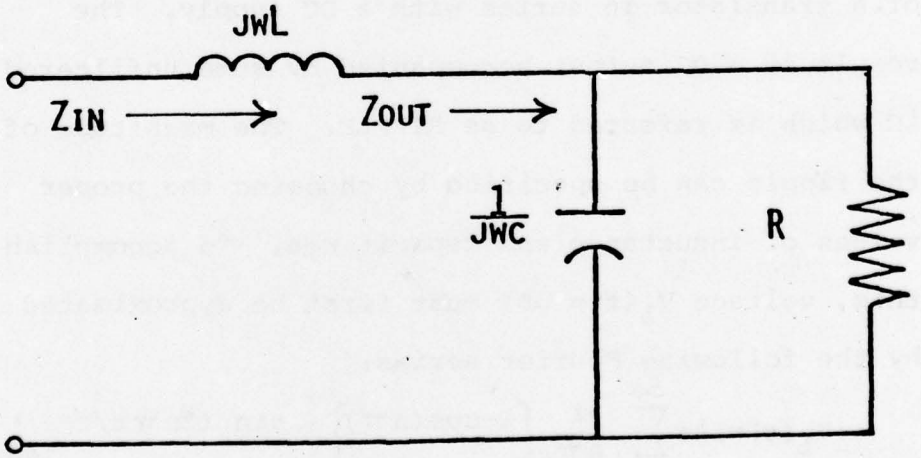

Figure 31. Steady state model of figure 30.

tributes to the majority of output ripple, equation 65 can further be approximated by equation 66:

$$V_1(t) = 12 + \frac{48}{\pi} \sin (2\pi t/T). \qquad (66)$$

The input impedance (fig 30) must also be derived. It can readily be obtained from the AC steady state model (fig 31) which assumes R_1 to be zero.

$$Zin(j\omega) = j\omega L + \frac{R}{jR\omega C+1} \quad . \qquad (67)$$

In order to obtain the value of Z_{in}, a value for ω must first be established. Normal operation of series switching regulators lies anywhere between 20 kHz and 50 kHz. [11] An operating frequency of greater than 20 kHz is desirable because it minimizes ripple and prevents operation in the audio range. Frequencies of over 50kHz introduce too many transitions through the transistor switch's active region. Increased transition through this lossy region results in decreased efficiency. In addition, duty cycles of 10% and 90% demand a switching speed of 1% of the switching period. High frequency operation would therefore make it difficult to obtain a power transistor with such a switching capability. As a result, a value of 30 kHz appears to be an attractive frequency at which to operate. Solving for ω ,

$$\omega = 2\pi f = 188.4 \times 10^3 \text{ RADIANS/SEC.}$$

Assuming $\omega = 188.4 \times 10^3$, R = 0.8 ohms, and C > 1000 uF, $R\omega C$ can be expressed as,

$$R\omega C > 150.72 >> 1 \quad . \tag{68}$$

Therefore equation 67 can be rewritten as

$$Zin(j\omega) = j\omega L + \frac{1}{j\omega C} \quad . \tag{69}$$

If $L > .1$ mH (70)

and $C > 1000$ uf, (71)

it can be said that

$$\omega L > 18.84 \text{ and } \frac{1}{\omega C} < 5.3X10^{-3}.$$

Therefore, $\omega L >> \frac{1}{\omega C}$ and $Z_{in}(j\omega)$ can further be approximated by

$$Z_{in}(j\omega) = j\omega L. \tag{72}$$

The zero to peak value of inductor ripple can now be obtained:

$$|I_L|_{RIPPLE} = \frac{|V_1|_{AC}}{|Z_{in}|} \tag{73}$$

$|V_1|_{AC}$ represents the magnitude of V_1's AC component. As a result,

$$|I_L|_{RIPPLE} = \frac{48}{\pi L} \quad . \tag{74}$$

An attempt will now be made to validate previous assumptions with regard to inductor current and capacitor voltage. It was earlier assumed that the

ripple content of these parameters was small. In keeping with this, a maximum zero to peak inductor ripple of 0.2 amps is permitted. A smaller maximum value could be set if it were not desirable to keep the value of L as small as possible. A small value of inductance results in a small series resistance and a physically smaller inductor. A value of 0.2 amps is chosen because it represents a 1.3% ripple at a 15 amp load and a 20% ripple at a load of 1 amp. Substituting values for $|I_L|_{RIPPLE}$ and ω into equation 74, yields the following solution for L:

$$L = 48/\pi \ (2\pi \times 30 \times 10^3 \times .2) = 0.405\text{mH} \ .$$

The value of C necessary to produce a desired output ripple can now be determined. From figure 31, the value of Z_{out} can be derived as

$$Z_{out} = \frac{R}{jR\omega C+1} \ . \qquad (75)$$

Assuming again that $R\omega C \gg 1$,

$$Z_{out} = \frac{1}{j\omega C} \ . \qquad (76)$$

The magnitude of the output voltage due to the AC component of V_1 can now be approximated by

$$|V_o|_{RIPPLE} = |I_L|_{RIPPLE} \times |Z_{out}| \ . \qquad (77)$$

Where $|V_o|_{RIPPLE}$ represents the zero-to-peak value of the

output ripple. Rewriting equation 71 to solve for C yields

$$C = 48/4\pi^3 f^2 L \left|V_o\right|_{RIPPLE} . \quad (78)$$

Specifying $\left|V_o\right|_{RIPPLE}$ at 1mV,

$$C = 1.06 \times 10^{-3} \text{farads.}$$

Since L and C both satisfy inequalities 70 and 71, a reevaluation of equations 67 and 75 is unnecessary.

Transient Response

The transient analysis begins with the generation of figure 30's Laplace transform representation. Figure 32 is such a representation and allows the development of equations 79 and 80:

$$V(s) + LI_o - \frac{V_{co}}{S} = I_1 (R_1+LS+(1/CS)) - I_2/CS \quad (79)$$

$$\frac{V_{co}}{S} = -I_1\frac{1}{CS} + I_2(R+\frac{1}{CS}) \quad (80)$$

The solution of these equations is described in appendix C and results in the following time domain expression for Vo(t):

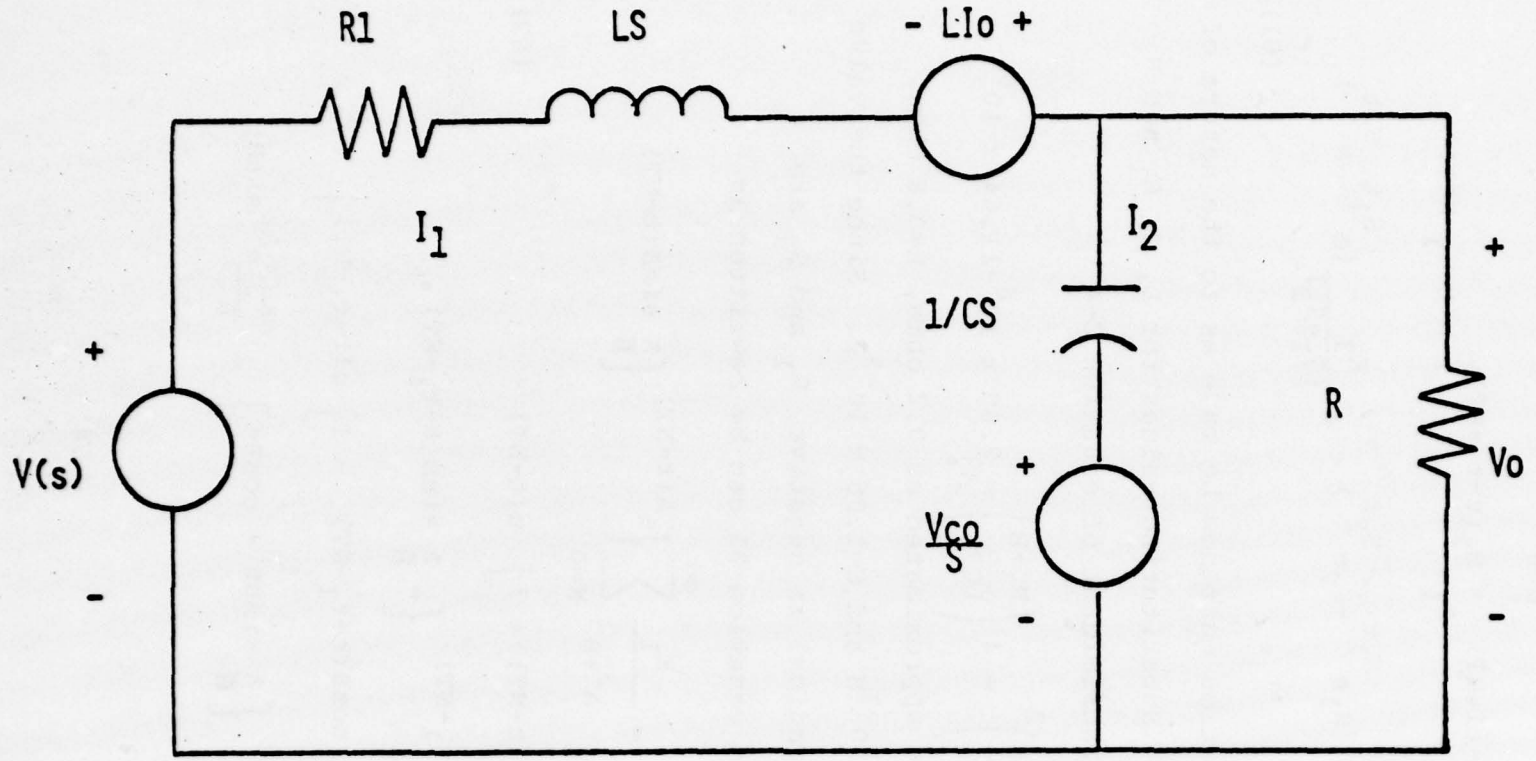

Figure 32. Laplace transform model of figure 30.

$$Vo(t) = \frac{K_1}{(S_1-S_2)S_1S_2} \sum_{N=0}^{\infty} ((S_2 e^{S_1(t-NT)} - S_1 e^{S_2(t-NT)} + S_1 - S_2)\, u(t-NT)$$

$$- (S_2 e^{S_1(t-t1-NT)} - S_1 e^{S_2(t-t_1-NT)})\, u(t-t_1-NT))$$

$$+ \frac{K_2}{(S_1-S_2)} (S_1 e^{S_1 t} - S_2 e^{S_2 t}) + \frac{K_3}{(S_1-S_2)} (e^{S_1 t} - e^{S_2 t}) \qquad (81)$$

A determination must now be made as to the nature of S_1 and S_2. Substituting values for L, C, R_1 and R into the discriminant of equation C-4 ,

$$\left(\frac{L+R_1RC}{LCR}\right)^2 - 4\left(\frac{R_1+R}{LCR}\right) = 2.80 \times 10^6 - 11.64 \times 10^6$$

where R_1 is approximated at 0.2 ohms, R=0.8 ohms, $L=0.405 \times 10^{-3}$H and $C=1.06 \times 10^{-3}$F. Since the value under the radical is negative, S_1 and S_2 are complex and equation 81 can be rewritten as

$$Vo(t) = \frac{K_1}{A^2+B^2} \sum_{N=0}^{\infty} \left\{ e^{A(t-NT)} \left\{ \frac{A}{B} \sin B(t-NT) \right.\right.$$

$$\left.\left. - \cos B(t-NT) + 1 \right\} u(t-NT) + \right. \qquad (82)$$

$$e^{(t-t_1-NT)} \left\{ - \frac{A}{B} \sin B(t-t_1-NT) + \right.$$

$$\left. \left. \cos B(t-t_1-NT) - 1 \right\} u(t-t_1-NT) \right\} +$$

$$K_2 e^{At} \left\{ \frac{A}{B} \sin Bt + \cos Bt \right\} + \frac{K_3}{B} e^{At} \sin Bt$$

where $A = -\left(\frac{L+R_1RC}{2LCR}\right)$ and

$$B = \sqrt{\left|\left(\frac{L+R_1RC}{2LCR}\right)^2 - \left(\frac{R_1+R}{LCR}\right)\right|} \quad .$$

Equation 82 describes the output voltage generated by the circuit in figure 22 with diode D out of the circuit. Diode D's effect on the circuit can be simulated by considering only the parallel combination of R and C whenever the current through inductor L is negative and switch S is open. By expressing these conditions as a Fortran program, values for overshoot and undershoot can be obtained for any set of initial conditions. The effect of time ratio control on the transient response can also be included by making t_1 a dynamic function of Vo(t). Figure D-1 describes the TRC relationship assumed for t_1/T as a function of $V_o(t)$. A list of the Fortran program appears in appendix D. Output from the program appears in figures 33 and 34. Figure 33 is a plot of the maximum overshoot and its recovery time (RT).[12] The overshoot was generated by switching the load from a value of 0.8 ohms to 12 ohms after a steady state output voltage of 12 V had been reached. The plot in figure 34 depicts a maximum undershoot developed by switching from a 12 ohm load to a 0.8 ohm load. Since the maximum overshoot is greater

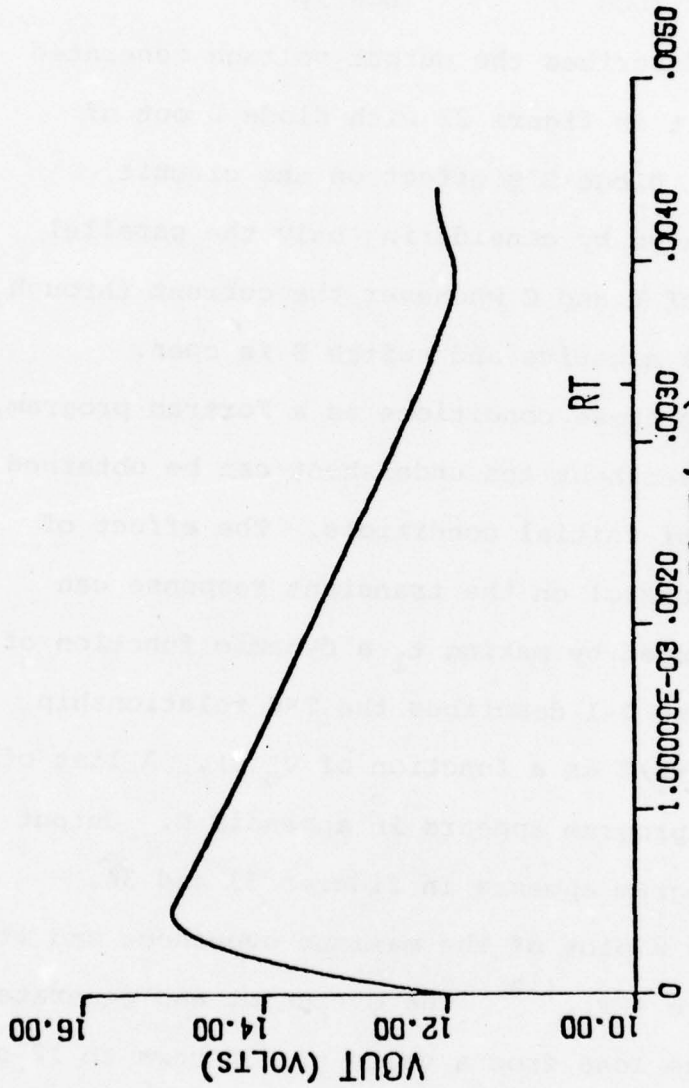

Figure 33. Maximum analytical overshoot (1)

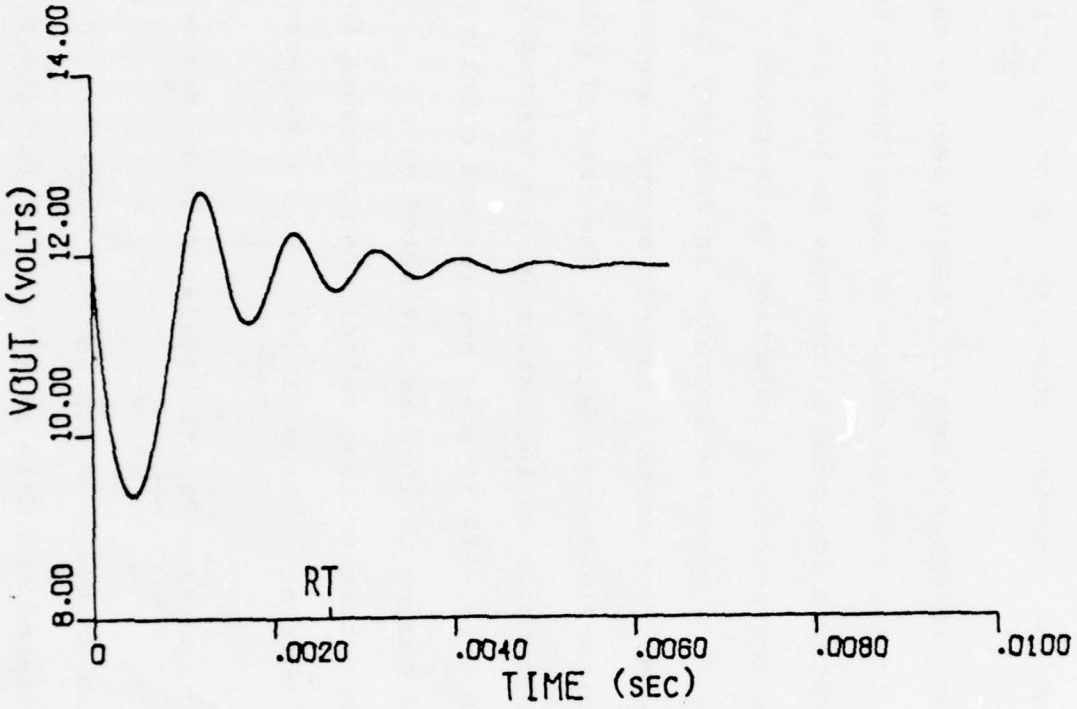

Figure 34. Maximum analytical undershoot (1)

than the specified value, adjustments in L and C have to be made. By looking at the derivatives of the capacitor voltage and inductor current, an insight can be developed as to the influence of L and C on the transient response. Since $\frac{dv_c(t)}{dt} = \frac{i_c}{C}$, an increase in capacitance is clearly seen to cause a decrease in the rate of change of capacitor voltage. The capacitor's response to changes in load is therefore decreased. A reduction in overshoot results with a possible increase in recovery time. The inductor represents a current source supplying the capacitor/load combination. The rate of change of its current is an indication of its response to a change in load. If it does not respond quickly enough, a change in load is reflected as a change in output voltage rather than a change in inductor current. Since $\frac{di_L(t)}{dt} = \frac{v_L}{L}$, a decrease in L serves to increase $\frac{di_L(t)}{dt}$ causing a short recovery time and a decrease in overshoot. With this in mind L is decreased and C is increased. Returning to equation 74, L is set to 0.3 mH causing the inductor ripple to increase to a value of 0.27 V. C is again calculated from equation 78 and becomes equal to

1.435×10^{-3}F. The introduction of these values into the program results in an overshoot of 1.85 V and a recovery time of 2.6 ms. An undershoot of 1.8 V also results with a recovery time of 2.5 ms. Figures 35 and 36 represent adjusted plots of overshoot and undershoot. Since the calculated values agree with the specifications, the regulator's filter design is complete.

Control Circuitry

The series switching regulator of figure 22 has been defined as a time ratio controlled device. The switch in series with the supply must therefore be opened and closed with a duty cycle determined by the output voltage. Figure 37 shows a circuit which accomplishes this through the use of a voltage controlled pulse width modulator (PWM), current amplifier (CA), and power switching device (PSD). When the pulse width modulator produces a square wave whose duty cycle and frequency are determined from the regulator's output ripple, the regulator is said to be self-oscillating.[13] If the modulator adjusts an externally created square wave, the regulator is identified as being externally driven. In the case of a self-oscillating switching regulator, advantage is taken of the

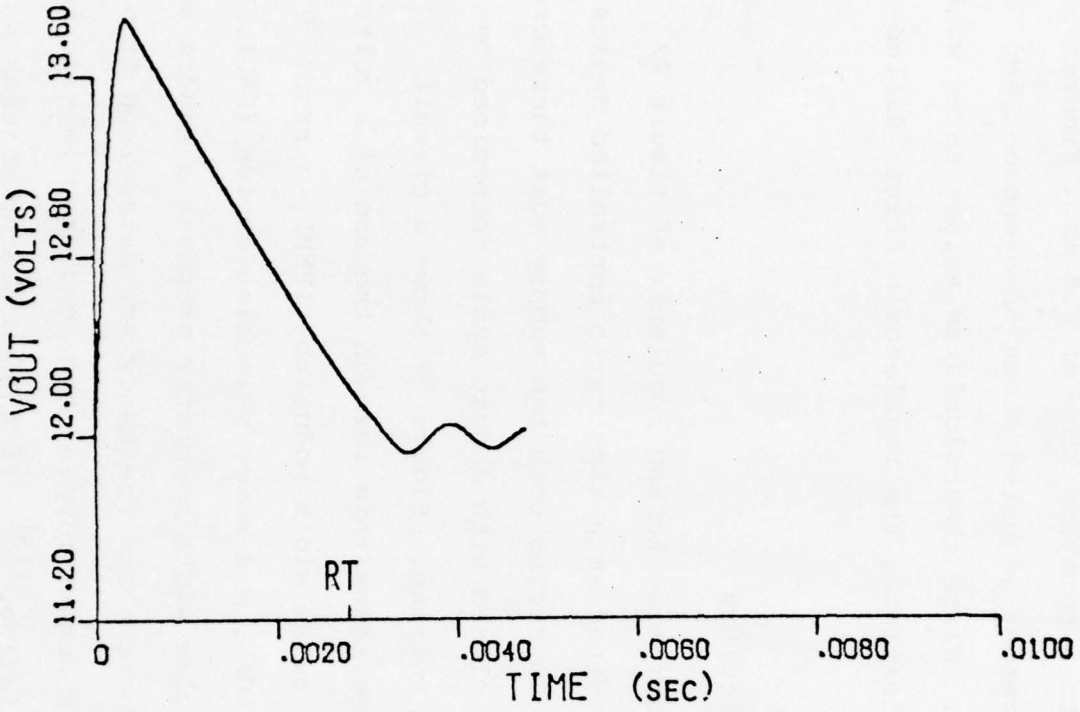

Figure 35. Maximum analytical overshoot (2)

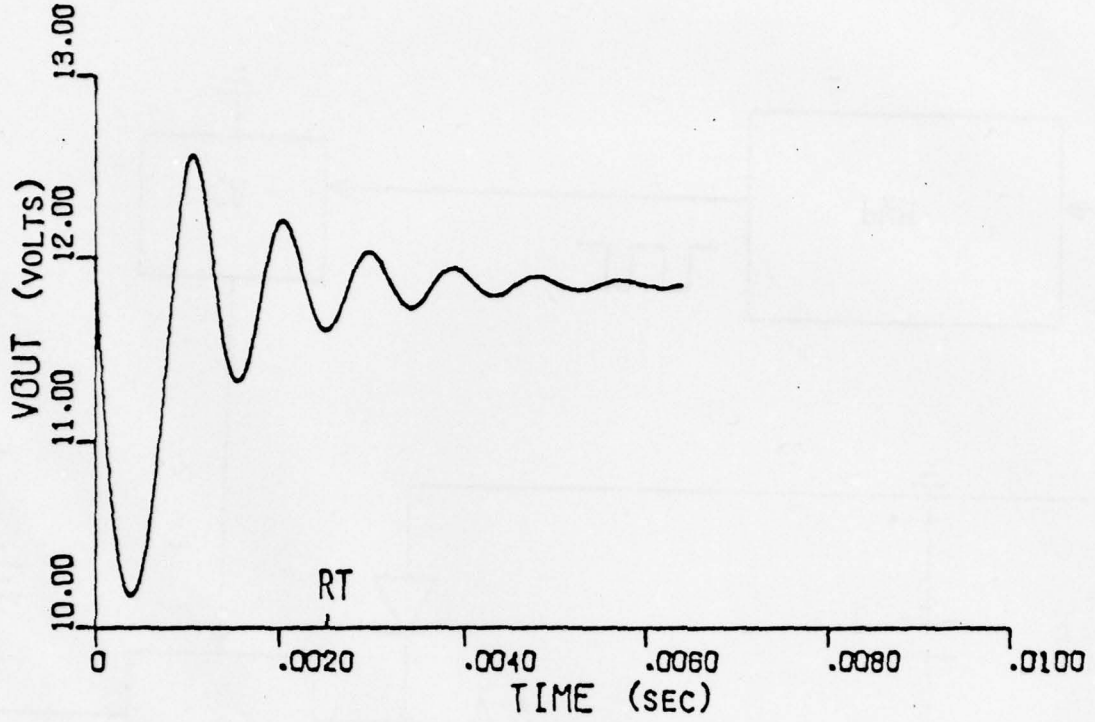

Figure 36. Maximum analytical undershoot (2)

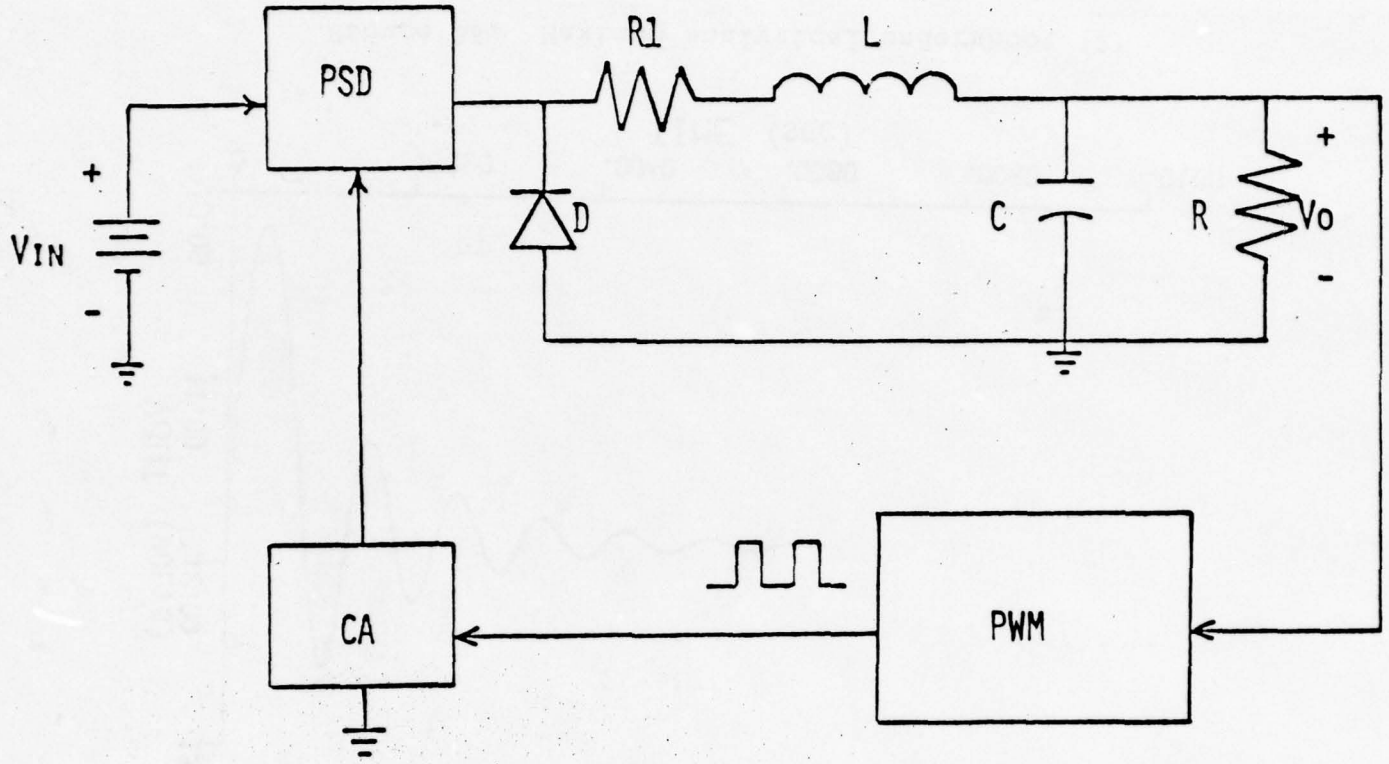

Figure 37. Series switching regulator

fact that the regulator's switching frequency is much greater than its natural frequency. Such a condition generates an output ripple in the form of a triangular wave. A linear relationship is therefore developed describing the output voltage as a function of time. Figure 38 indicates how such a linear relationship can be used to develop a change in pulse width. If the waveform of figure 38 turns a switch on and off by traversing some threshold T, a vertical movement in the triggering waveform generates a change in the triggering time, and a variation in pulse width.

The externally driven type of regulator varies the pulse width of a square wave obtained from some external source. An astable multivibrator is such a source and is used as the basis for the voltage controlled pulse-width modulator designed in this report. An astable multivibrator is discussed in appendix E and gives rise to a modified astable multivibrator whose operation is described by the following expressions for ON time and OFF time:

$$t_1 = KK_1 \ln\left\{\frac{(V_2-V_{be})}{KK_2}\right\} . \tag{83}$$

and

$$t_2 = KK_1 \ln\left\{\frac{(V_1-V_{be})}{KK_2}\right\} . \tag{84}$$

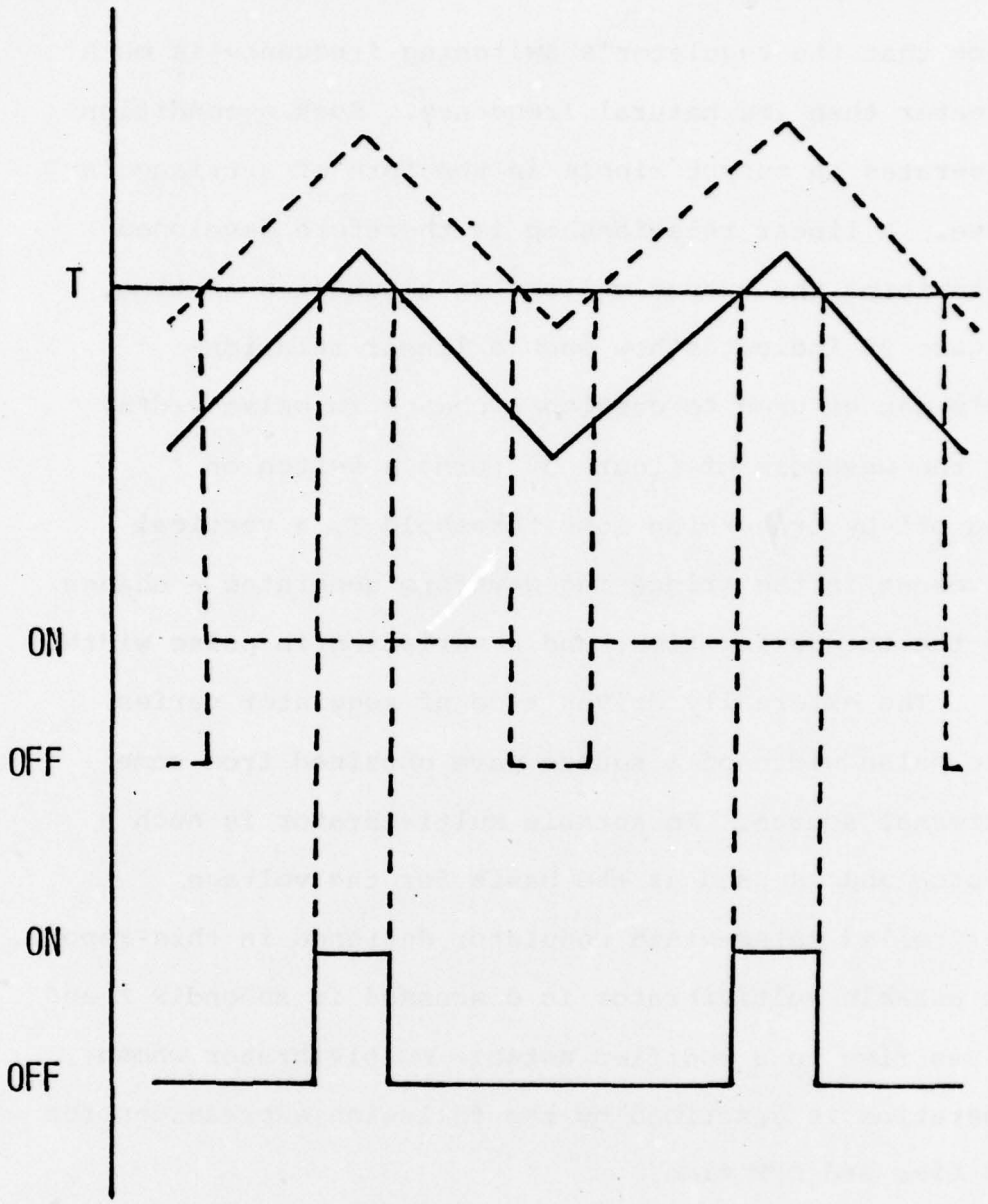

Figure 38. Self-oscillating method of control

The natural log curve[14] of figure 39 shows that an approximately linear range of operation exists between X = 1/4 and X = 3/4. If such a region of operation is realized, t_1 and t_2 can be described as linear functions of V_2 and V_1 when $V_2 \gg V_{be}$ and $V_1 \gg V_{be}$. By assuming the sum of V_1 and V_2 to remain constant, the sum of t_1 and t_2 can also be assumed approximately constant making the frequency of operation constant. As a result, the duty cycle becomes a variable function of V_1 or V_2 qualifying figure E-2 as a voltage controlled pulse width modulator. The realization of such a linear operating range begins by neglecting V_{be} in equations 83 and 84. Substituting the specified boundary conditions,

$$V_2 = \frac{1}{4} KK_2$$

and

$$V_1 = \frac{3}{4} KK_2$$

where $KK_2 = V_1 + V_2 - V_{be}$.

Solving for V_1,

$$V_1 = 3V_2.$$

Although approximate, the above relation can serve as a starting point from which to develop values

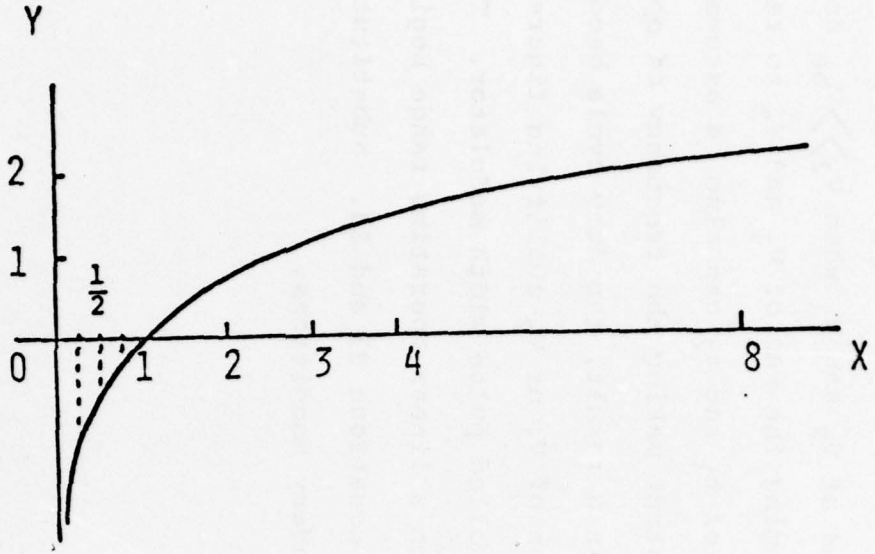

Figure 39. Natural log curve

for V_1 and V_2. By assuming a value of 4 V for V_2, V_1 becomes equal to 12 V, and expressions for duty cycle, period, and frequency can be defined. The duty cycle is defined by

$$P_1 = t_1/T = \frac{-R_2C_2}{T} \ln \left\{ \frac{V_2-V_{be}}{V_1+V_2-V_{be}} \right\} \qquad (85)$$

where the period, T, is defined as

$$T = t_1+t_2.$$

The frequency therefore becomes

$$F = 1/T.$$

The plot of equation 85 (fig 40) shows that an extension of the difference between V_1 and V_2 is required if the duty cycle is to range from 10% to 90%. By extending V_1 and V_2 to 3 V and 13 V, adjusted plots of duty cycle and frequency can be developed. These plots are shown in figures 42 and 43. Values for R_2C_2 in equation 85 were determined by specifying a frequency of 30kHz at a 50% duty cycle. This resulted in

$$R_2C_2 = R_1C_1 = (-T/2)/\ln \left\{ \frac{8-.7}{16-.7} \right\}$$

where

$$R_2C_2 = R_1C_1 = 22.5 \times 10^{-6} \text{sec.} \qquad (86)$$

Investigation of figures 42 and 43 reveals the duty cycle's range to be 10% to 90% while the change in fre-

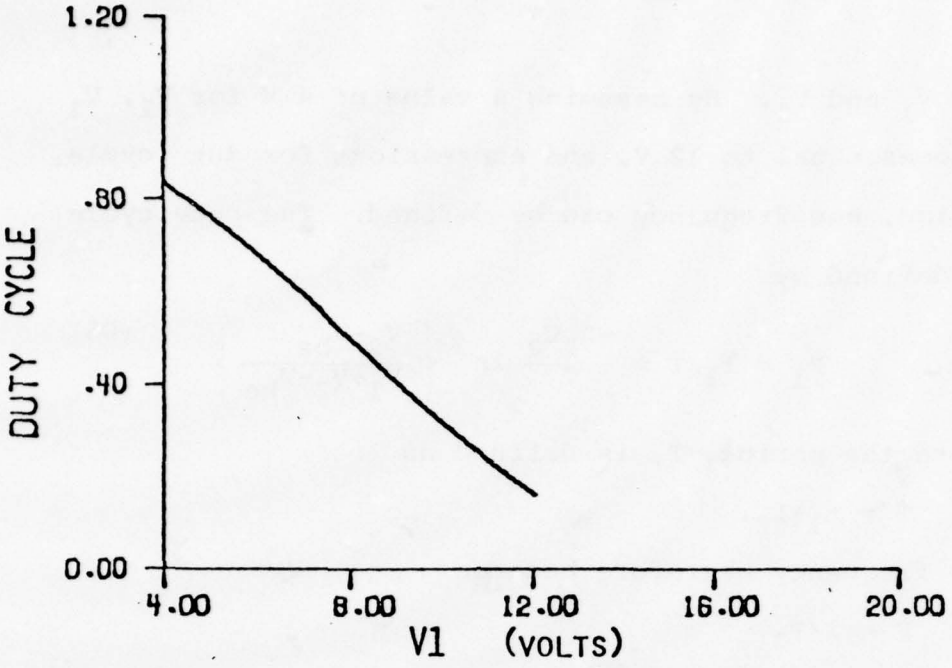

Figure 40. Duty cycle vs. output voltage (1)

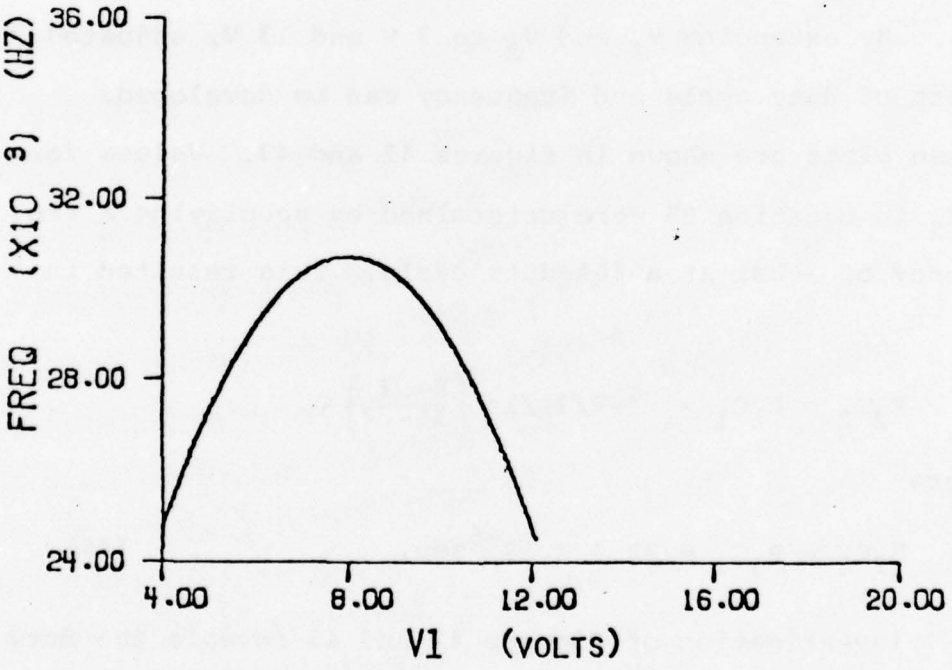

Figure 41. Frequency vs. output voltage (1)

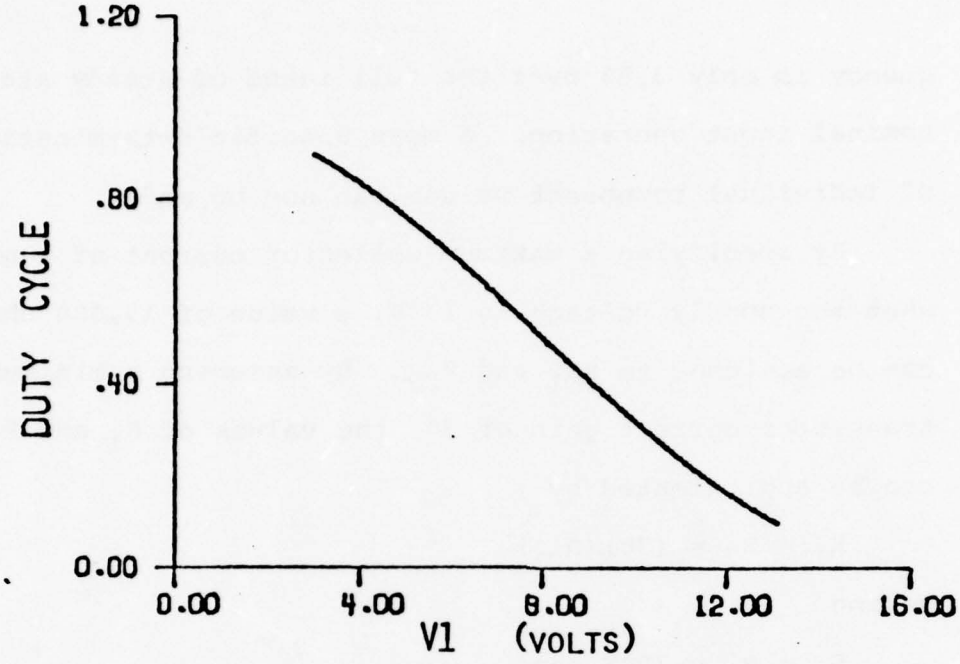

Figure 42. Duty cycle vs. output voltage (2)

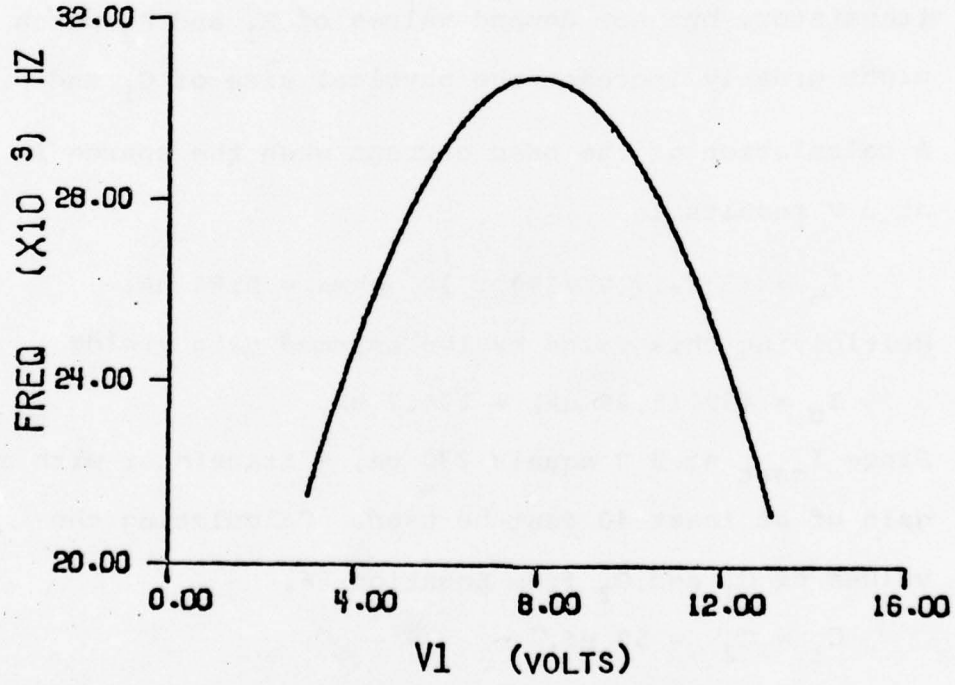

Figure 43. Frequency vs. output voltage (2)

quency is only 3.8% over the full range of steady state nominal input operation. A more specific determination of individual component values can now be made.

By specifying a maximum collector current of 1 ma when the supply voltage is 13 V, a value of 13,000 ohms can be assigned to R_{C1} and R_{C2}. By assuming a minimum transistor current gain of 30, the values of R_1 and R_2 can be approximated by

$$R_1 = R_2 = (30)(R_{C1})$$

making

$$R_1 = R_2 = 390K \text{ ohms.}$$

This results from the fact that the current flowing through R_1 and R_2 must be great enough to saturate the transistor, but not demand values of R_1 and R_2 which might greatly increase the physical size of C_1 and C_2. A calculation of the base current when the source is at 3 V results in

$$I_b = (3 \text{ V} - .7 \text{ V})/390 \times 10^3 \text{ ohms} = 5.89 \text{ uA.}$$

Multiplying this value by the assumed gain yields

$$I_c = (30)(5.89 \text{ uA}) = 176.7 \text{ uA.}$$

Since I_{csat} at 3 V equals 230 uA, a transistor with a gain of at least 40 must be used. Calculating the values of C_1 and C_2 from Equation 86,

$$C_1 = C_2 = 58 \text{ pf.}$$

This results in making $(R_{C1})(C_2) << (R_1)(C_1)$ and therefore causing the initial conditions of equations E-4, E-5, E-8, and E-9 to be valid. The choice of a 2N2222A as the switching transistor completes the specification of all but one of the circuit's components. The remaining element is a diode which must be inserted from the transistor's emitter to ground. Its insertion is shown by the dashed lines in figure E-2. The diode's purpose is to protect the transistor's base-to-emitter junction from high values of reverse voltage. A germanium diode, 1N486A, protects the junction while offering a very small forward bias voltage. Table E-1 represents the final component values of figure E-2.

With the help of the electronic circuit analysis program "SCEPTRE", the circuit in figure E-2 can be simulated using transistor and diode models for the 2N2222A and 1N486A semiconductors. The plots of figures 44 and 45 represent the base and collector voltages of transistors Q_1 and Q_2. They also confirm frequency calculations and expected circuit operation in general.

Upon attempting to obtain a 10% to 90% variation in duty cycle, laboratory results indicated that the modulator's transistors were unable to turn off with

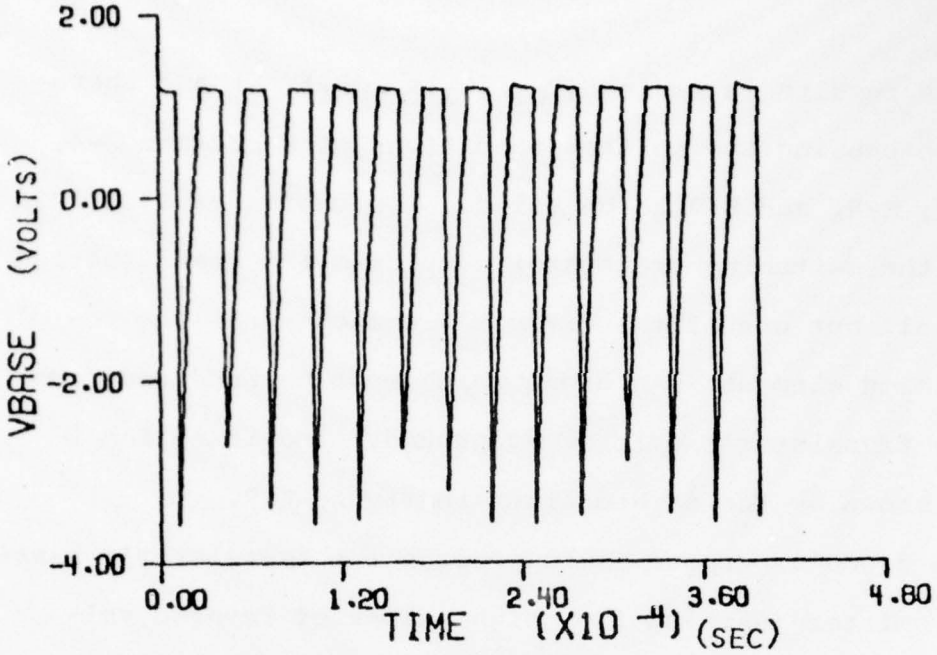

Figure 44. Base voltage of Q1

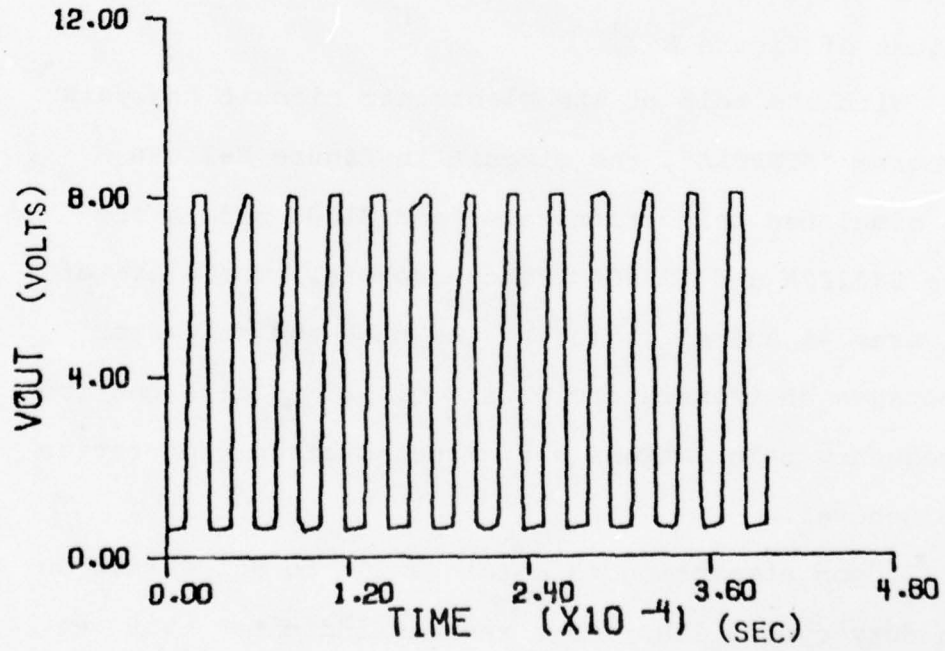

Figure 45. Collector voltage of Q1

enough speed to sustain oscillation. By allowing V_1 and V_2 to go between values of 5 V and 12 V, a 20% to 80% change in duty cycle was observed and proper multivibrator oscillation assured.

Pulse Width Modulator Control

The multivibrator described above has a pulse width which is controlled by the values of V_1 and V_2. V_1 and V_2 can also be linked to the regulators output making the modulator's pulse width a function of the regulator's output voltage. The circuit in figure 46 represents such a linkage. Its analysis begins by assuming a base-to-emitter drop of 0.7 V and a nominal current gain of 100 for each transistor. As the regulator's output increases from 11.7 V to 12.4 V diodes D_1 and D_2 act to maintain a 1.4 V rise between V_{regout} and the input of stage one. Stage one's primary function is to supply the regulator's feedback circuit with an input impedance of 100K ohms. With the help of Zener diode Z_1 stage one operates with a voltage gain of unity and goes from saturation to cut-off, while reflecting changes in V_{regout} at Q_2's base. Q_2's collector responds with a voltage gain of 10 and an excursion of 5 V to 12 V. This voltage

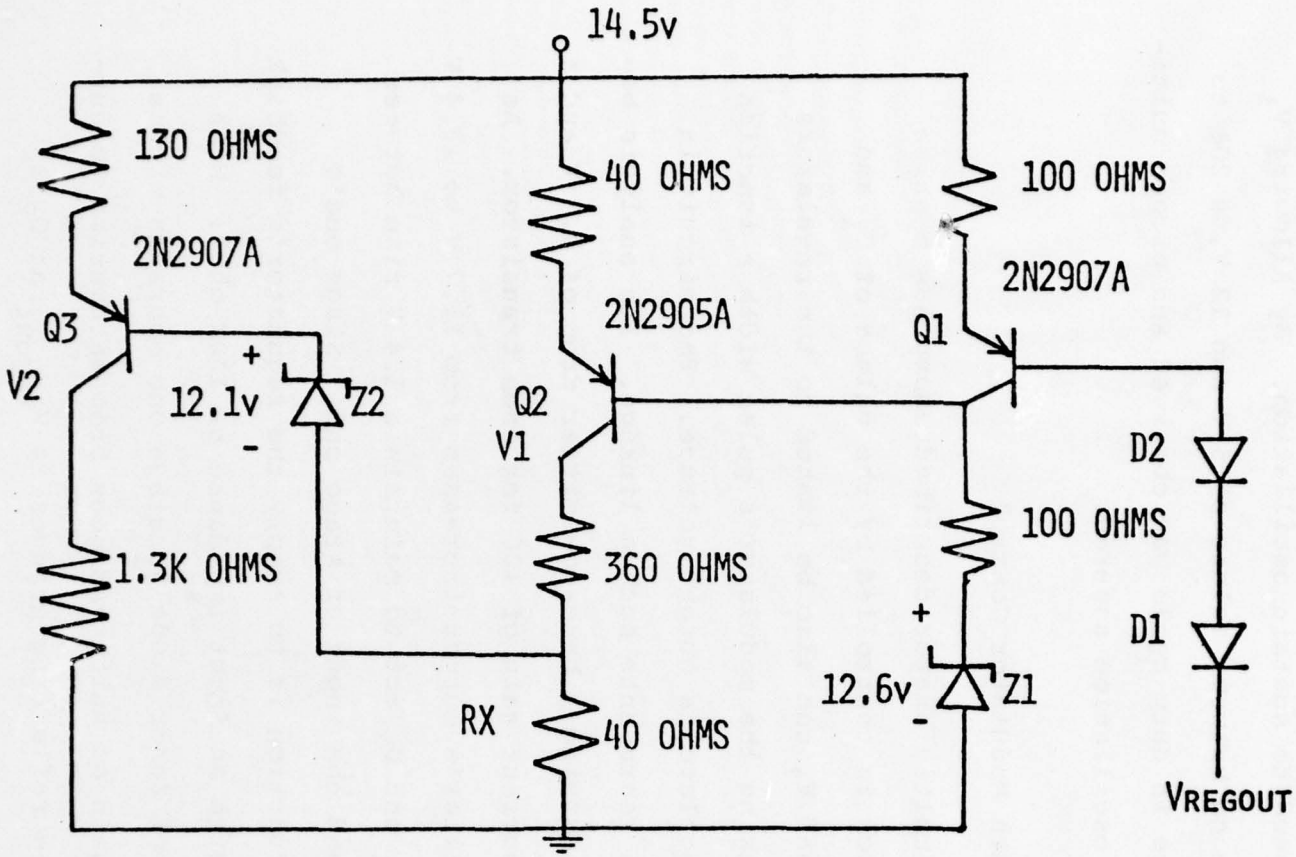

Figure 46. Pulse width modulator control circuit

acts to satisfy the requirements of V_1 without loading down Q_2's collector circuit. Resistor, R_X, functions to divide V_1 by a factor of 10. This value is then translated by Zener diode Z_2 to the base of Q_3. Q_3's collector reacts by decreasing from 12 V to 5 V. V_{CQ3} therefore qualifies as the source of voltage V_2. In operation the circuit in figure 47 replaces that in figure 46. The primary differences between the two circuits are the replacement of Z_2 by transistor Q_4 and its associated circuitry, and the introduction of resistors R_{Z1} and R_{B1}. Transistor Q_4's base circuit maintains its collector current at a constant of approximately 1 ma. A constant voltage is therefore seen across R_{CQ4}, and neither I_B nor I_{CQ4} act to undesirably affect the circuitry into which they flow. Resistor R_{Z1}'s effect is only seen when transistor Q_1 is cutoff. At that point I_1 is at a minimum and Z_1 operates on the knee of its characteristic. R_{Z1} can then act to slightly decrease V_{Z1} and more exactly determine the duty cycle desired. R_{B1}'s only function is to protect the base of Q_1 from excessive amounts of base current. When connected to the multivibrator (figure 2), values of 11.4 V and 12.4 V for V_{regout} produce duty cycles of 80% and 20%, respectively. The 14.5 V supply (figure 47) is made available through

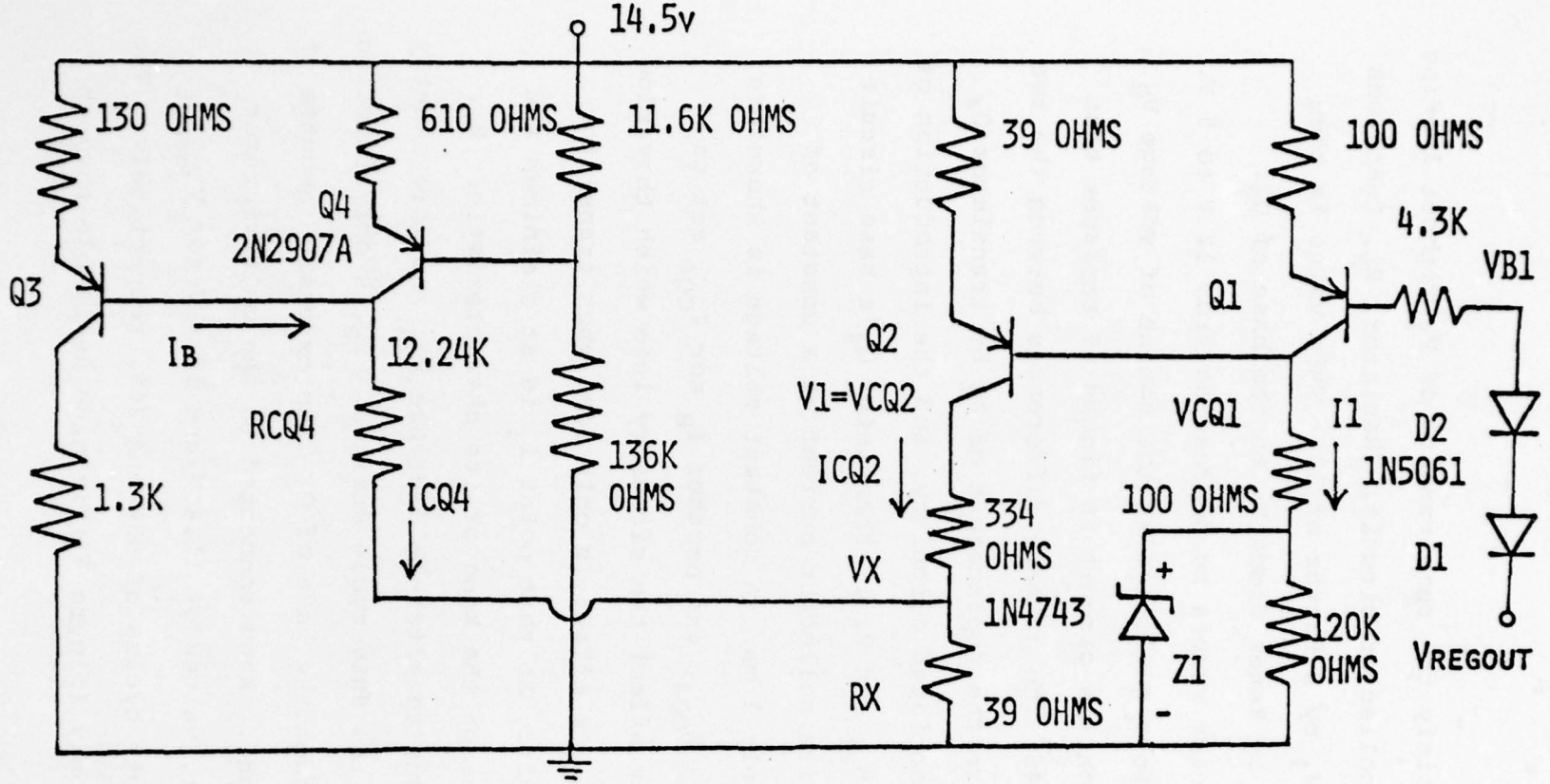

Figure 47. Modified pulse width modulator control circuit

the use of a Lambda Las-14U voltage regulator. [15] The regulator and its associated circuitry are shown in figure 48. It is capable of accepting input voltages between 6 V and 40 V, delivering an output current of 3 A, and dissipating as much as 30 watts at 25°c. Its output is a variable and can be adjusted by resistors R_1 and R_2 to deliver voltages between 2.65 V and 30 V. This completes the description of the voltage controlled pulse width modulator and allows attention to be focused on the current amplifier (CA) of figure 48.

Before the amplifier's maximum collector current can be determined, a power switching device (PSD) must be selected. Lambda's PMD-17K-100 is a Darlington pair made primarily for high power switching applications. [16] It offers an I_{cmax} of 20 A (continuous), a V_{ecmax} of 100 V, a Pd_{max} of 225 W at 25°c, and a minimum current gain of 1000. On this basis, it has been chosen to perform as the power switching device (PSD) (figure 48). The current amplifier's maximum collector current can now be specified at a value of at least 15 A/1000 or 15 mA. On this basis and that of criteria yet to be discussed, a maximum value of 50 mA will be assumed for I_{CQA}. With respect to the current amplifier's input, it is important that the base current

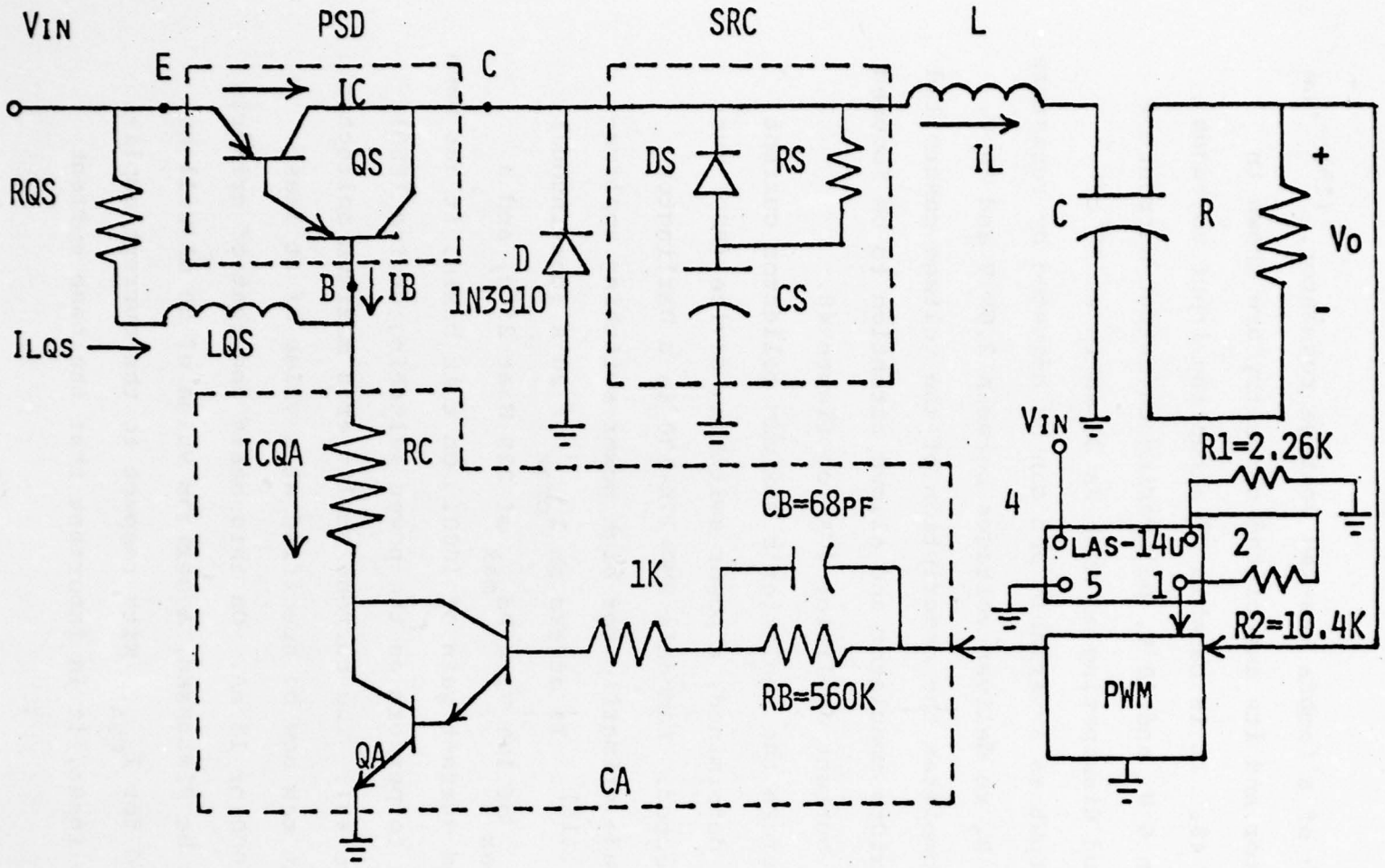

Figure 48. Modified series switching regulator

not be so great as to load down the output of the pulse width modulator. This can be accomplished by designing the current amplifier as a Darlington pair with a minimum current gain of 10,000. The result is a base current of only 5 uA. This amount of base current is small when compared to even 10% of the initial 380 uA needed to charge C_2 of figure E-2. By assuming a minimum modulator output of 5 V and a Darlington base-to-emitter voltage of 1.4 V, a maximum value of 720K ohm series resistance can be calculated which will produce a minimum base current of 5 uA. In practice an available value of 560K ohms is used. Figure 48 depicts this resistance in parallel with a capacitance of 68 pf. The capacitor's function is to assist in bringing the Darlington pair out of saturation and into cutoff when the modulator's output goes to zero. It accomplishes this by providing a negative voltage current sink which in turn acts more rapidly to remove charge carriers from the Darlington's base. The value of C_B is empirically obtained and is a function of the Darlington's extent of saturation. The only restriction on C_B is that it not increase too greatly the time constant which determines the charging rate of capacitor C_2 (fig. E-2). A 1K ohm resistor is placed in series with the Darlington's

base and protects it from excessive base currents.

In operation, the current amplifier cannot, by itself, drive the power Darlington from saturation to cutoff. Additional circuitry is needed. The resistor/inductor series combination in figure 48 represents such circuitry.[17] It was suggested by Ulf Andersson, ADDO AB, Malmo, Sweden and operates in the following manner: When the power Darlington is in saturation, the current through inductor L_{QS} increases as,

$$I_{LQS} = Imax(1-e^{-t/\tau}) \qquad (87)$$

where $\tau = L_{QS}/R_{QS} << $ switching period and $I_{max} = V_{eb}/R_{QS}$. As the power Darlington's base drive is removed, L_{QS} continues to conduct current back into the transistor's base, turning it off. When Q_S's base drive returns, L_{QS} fails to conduct immediately and Q_S saturates quickly. When calculating I_{max}, Andersson suggests that it be set equal to the value of I_B when Q_S is in saturation. I_B can be approximated by

$$I_B = ((V_{in}-V_{eb})/R_C) - I_{max}. \qquad (88)$$

Since h_{FE} is at its minimum of 1000 when I_c is equal to 15 A, a minimum base current of 15 mA will be designed for Q_S in saturation. In an attempt to satisfy Andersson's criterion, I_{max} will be chosen at a value of 15 mA when V_{in} is at a minimum of (24 V-15%(24 V)) or 20.4 V.

Solving for R_C from equation 88

$$R_C = (V_{in}-V_{eb})/(I_B+I_{max}) \qquad (89)$$

where

$$R_C = \frac{20.4\ V-2.8\ V}{30mA} \approx 586\ \text{ohms}$$

The value of I_B can be calculated from equation 88 when V_{in} is at a maximum of 27.6 V.

$$I_B = 27\ mA.$$

I_{max} is therefore equal to approximately one half the value of I_B. In an effort to decrease this difference, the value of I_{max} will be increased to 20 mA and the value of R_C recalculated when V_{in} equals 20.4 V. From equation 89,

$$R_C = 500\ \text{ohms}$$

Calculating, again, the value of I_B for V_{in} = 27.6 V,

$$I_B = 30\ mA.$$

The difference between I_{max} and I_B has decreased, but only at the expense of an increase in power dissipation. Andersson's criterion is not a strict condition on the value of I_{max}, but rather a rule of thumb used in its calculation. Treating it as such, an I_{max} of 20 mA is assumed acceptable, and any further increase in power dissipation is avoided. It was on this basis that a maximum value of 50 mA was earlier chosen for I_{CQA}. With the value of I_{max} defined, the

value of R_{QS} can be obtained by

$$R_{QS} = V_{eb}/I_{max} = 2.8v/20ma = 132 \text{ ohms.}$$

L_{QS} can now be determined. Its value must be large enough to turn Q_S off, but small enough to satisfy the condition $L_{QS}/R_{QS} << $ switching period. A value of 0.15 mH was found to satisfy the above condition while functioning satisfactorily to turn Q_S off. L_{QS} and R_{QS} assure Q_S's saturation and cutoff, but other switching related problems demand the introduction of even further circuitry.

When transistor Q_S turns on and off, it experiences, for a short time, simultaneous values of maximum voltage and current. Such a situation subjects the switching device to undesirable stresses and acts to decrease the regulator's operating efficiency. Figure 49 depicts this situation by displaying voltage V_{ec} and current I_C concurrently. While peak values of V_{ec} and I_C do not overlap when Q_S is turning on, they do when Q_S is turning off. Such an overlap can be rectified by the stress relief circuitry (SRC) which appears in parallel with diode D (figure 48) [18] When Q_S is in saturation, capacitor C_S charges up through resistor R_S to a value of $V_{in}-V_{ecsat}$. As Q_S begins to turn off, I_C decreases. Since inductor L does not tolerate an instantaneous change in current, capacitor C_S acts to

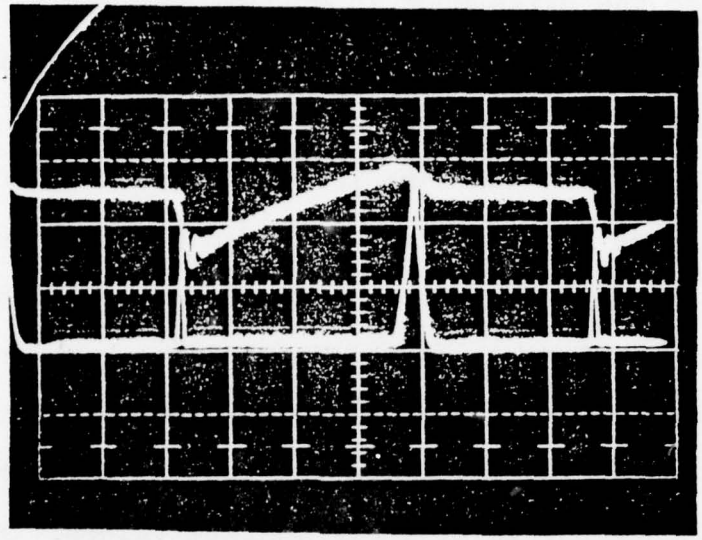

Figure 49. Switching waveforms without (SRC)

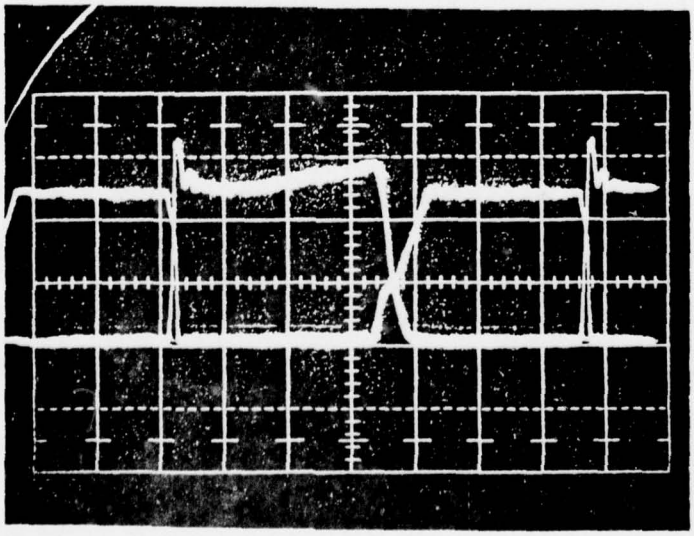

Figure 50. Switching waveforms with (SRC)

provide the difference in current between I_L and I_C. This continues until C_S discharges through diode D_S. If the current were not supplied by C_S, diode D would have had to be the immediate source of new current, and become forward biased as soon as it conducted even the slightest amount of current. It would therefore become forward biased before Q_S' collector current had a chance to decrease. This would cause the voltage across the transistor and the current through it to simultaneously be at their maximum values. Figure 50 represents V_{ec} and I_C after the introduction of the circuitry suggested. R_S and C_S are calculated by keeping their product less than one-sixth the switching period, and making C_S as large as possible without decreasing R_S to a value which might cause $(V_{in}-V_{ec})/R_S$ to be in excess of I_{cmax}. Values of 0.2 uF for C_S and 25 ohms for R_S were found to provide sufficient stress relief while satisfying the conditions specified above. It should be mentioned that the supression offered by figure 48 results only at the expense of energy lost during the charging of capacitor C_S. The amount of energy lost in charging C_S over one cycle can be expressed by

$$E_{lost} = \frac{1}{2} (C_S)(V_{cs})^2 \quad . \qquad (90)$$

The average power lost over one cycle becomes

$$P_{lost} = \frac{1}{2} (C_S)(V_{cs})^2/T \qquad (91)$$

where T is the period of operation.

Two components, inductor L and capacitor C, are basic to the regulator's operation and, to a large extent, determine its efficiency and the quality of its output. Inductor L was chosen to be wound on an air core with 12-gauge heavy armored polythermaleze transformer wire. The number of turns necessary to produce an inductance of 0.3 mH was determined by

$$N = (L/(Fxd))^{\frac{1}{2}} = \frac{300}{8X10^{-3}X2.25} = 129 \text{ turns} \quad .$$

L represents the desired inductance in microhenries, d represents the diameter of the coil in inches, and F defines a form factor obtained from the ratio of the coils diameter, d, to its length. The graph used to relate this ratio to F is available.[19] An air core was used because it offers a constant value of inductance and eliminates losses due to hysterisis and eddy currents. A wire gauge of twelve was used to minimize series resistance and reduce I^2R losses.

Capacitor C was chosen to be a Cornell-Dublier four terminal low-inductance capacitor.[20],[21] The graph

in appendix F is a typical comparison between a low inductance capacitor and a conventional capacitor. As the plot indicates, a low inductance capacitor has a much better high frequency characteristic, making it desirable for series switching applications. A capacitance of 1600 uF was chosen as the closest value available to that calculated earlier.

All of the semiconductors used were chosen on the basis of availability and satisfaction of certain circuit specifications. Transistors were expected to meet specifications on maximum power dissipation, maximum collector to emitter voltage, maximum collector current, and transistor current gain. Diodes were chosen on the basis of their maximum reverse voltage, maximum power dissipation, and forward voltage drop. Zener diode Z_1 was expected to meet the specified reference voltage and power dissipation. Diode D satisfied requirements on maximum reverse voltage, forward voltage drop, maximum forward current, and reverse recovery time. The reverse recovery time is important in this case because it determines the time for which Q_S experiences a high collector current while diode D is forward biased and V_{CEQS} is at a maximum.

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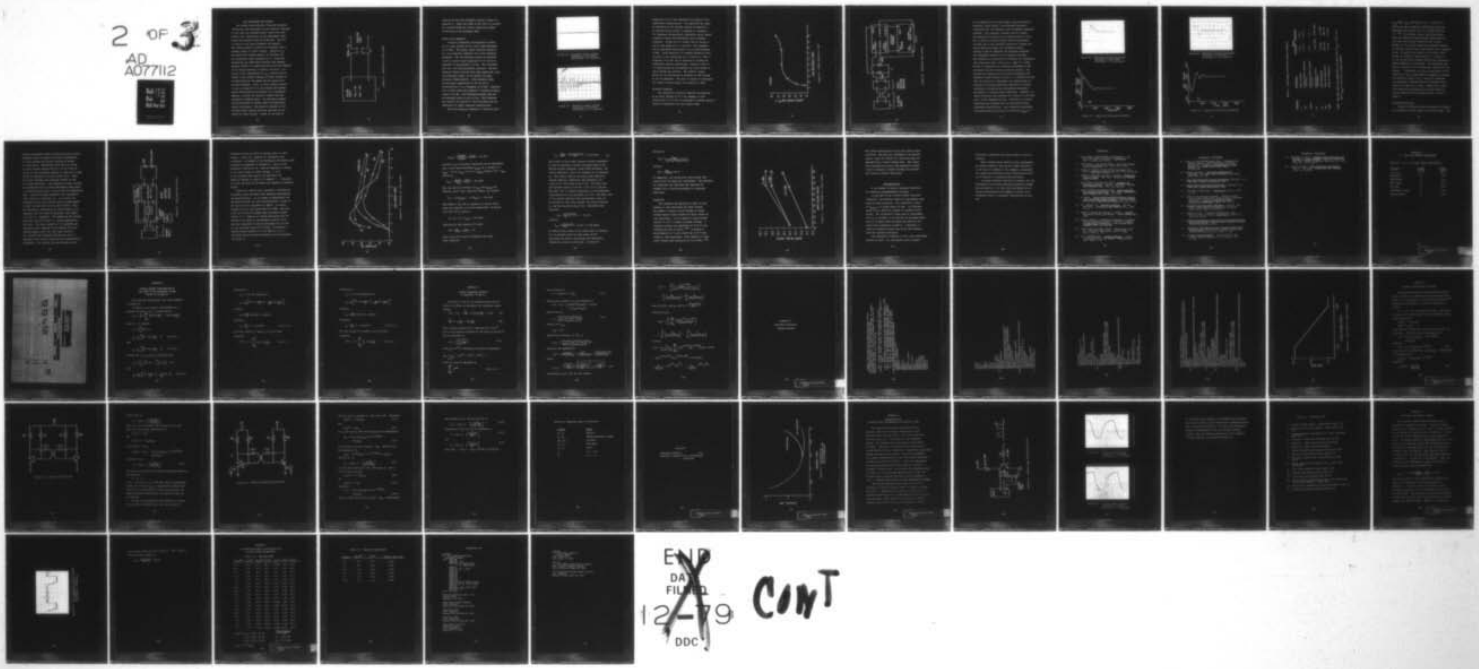

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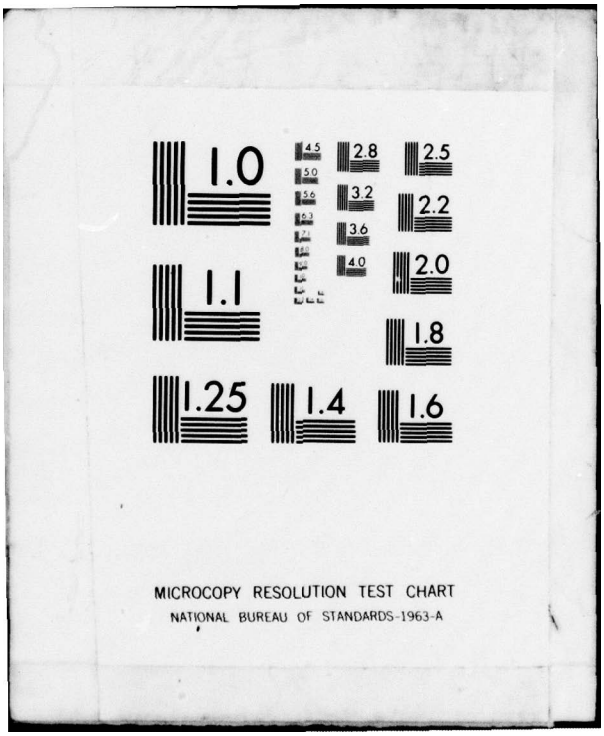
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TEST PROCEDURES AND RESULTS

The steady state response, transient response, efficiency, and regulation of the regulator designed in this work are discussed below, along with test results and a description of the measurement techniques and equipment used for each test. The cir- in figure 51 was used throughout the measurement taking proces to provide the regulator with a constant supply of input voltage. Capacitor C_{in} was mated with voltage supply E to minimize the high frequency ripple generated in E. Such high frequencies are undesirable because they generate magnetic fields of a magnitude which prove detrimental to the normal operation of nearby circuitry. As a result of the introduction of C_{in}, initial turn-on caused a more gradual increase in input voltage to be experienced by the Lambda Las-14u series pass voltage regulator. This, in turn, caused voltages V_1 and V_2 (figure E-2) to rise slowly and prevent proper multivibrator oscillation. As a corrective measure, a switch was placed in series with the regulator's feedback path. Its switching allowed the multivibrator to become reset and experience proper oscillation. The switch's presence is not necessary when storage batteries are used as the source of input voltage. Figure 51 was used in

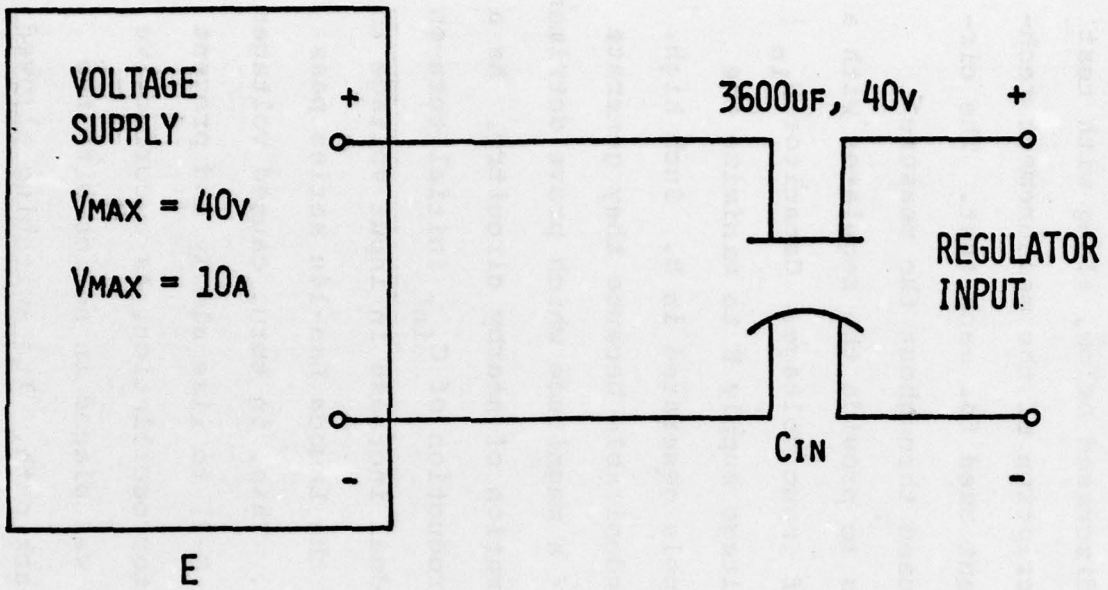

Figure 51. Regulator DC input supply

conjunction with the equipment listed in table G-1, appendix G. Among the items on the list is a secondary standard which was used to assure the proper calibration of the equipment used.

Steady State Response

Figure 52 represents the regulator's output for an input voltage of 24 V and a load resistance of 10 ohms. The output ripple consists primarily of a low frequency component and a high frequency component. The low frequency ripple was measured to have a zero-to-peak magnitude of 13.5 mV and a frequency of approximately 30 kHz. This disagrees with the 1 mV value previously required. The discrepency results from the fact that capacitors, even low inductance types, do not exhibit an ideal frequency characteristic. From capacitor data, an equivalent capacitance of 100 uF can be calculated for C at a frequency of 30 kHz. Substitution of this value into equation 77 yields an output ripple of 14 mV. The difference between this and the measured value is only 0.5 mV. This confirms the validity of equation 77 while pointing out the importance of proper component specification.

The high frequency component in figure 52 has a

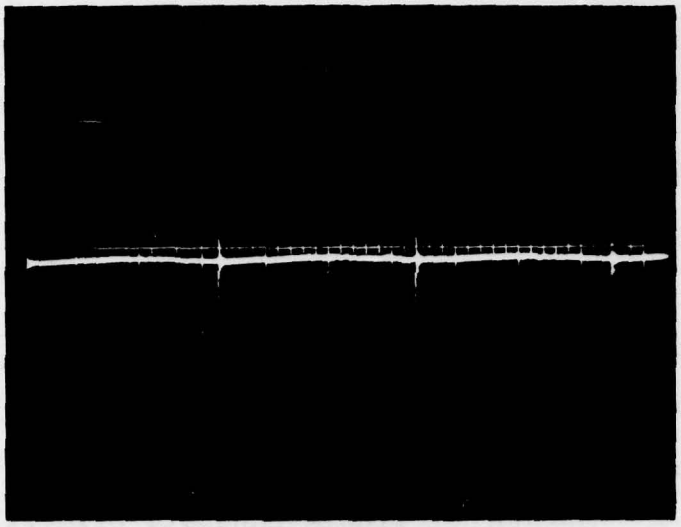

Figure 52. Regulator output voltage
((vertical = 0.5 V/Div)
(horizontal = 10 usec/Div)

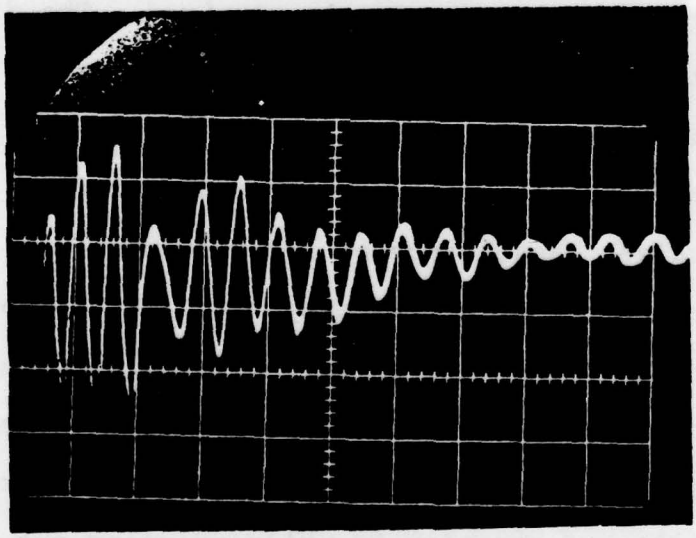

Figure 53. Regulator output voltage
(vertical = 0.2 V/Div)
(horizontal = 0.1 usec/Div)

magnitude of 0.8 V and represents the output's most undesirable characteristic. Its amplitude can again be explained by the nonideal nature of capacitor C. As implied by the curves in appendix F, capacitor C's impedance characteristic eventually curves upward increasing rather than decreasing with increased frequency. Figure 53 is a closer look at figure 52 with a time sweep of 0.1 u sec/div. The frequency can be calculated from figure 53 to be approximately 20 MHz. Since capacitor C's maximum impedance specification is only specified up to a value of 1 MHz, a frequency of 20 MHz can be expected to produce the undesirable results experienced. Values as high as 3 V peak-to-peak can be measured for large values of input voltage and current. The output's ripple factor can be calculated by dividing its RMS voltage by its DC component. The plot in figure 54 represents the output's ripple factor as a funtion of load.

Transient Response

The regulator's transient response was measured at an input voltage of 24 V for changes in load ranging from 1 A to the 10 A maximum of voltage supply E. Figure 55 represents the test circuit used.

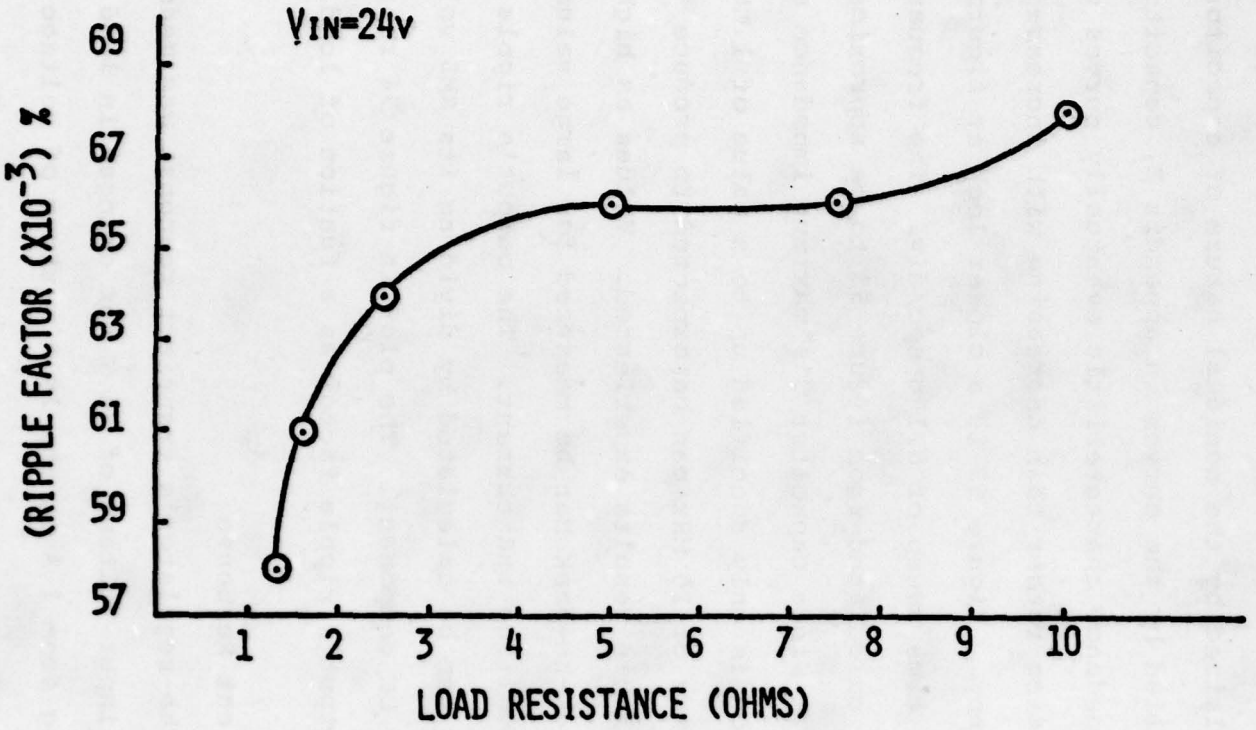

Figure 54. Ripple factor vs. load

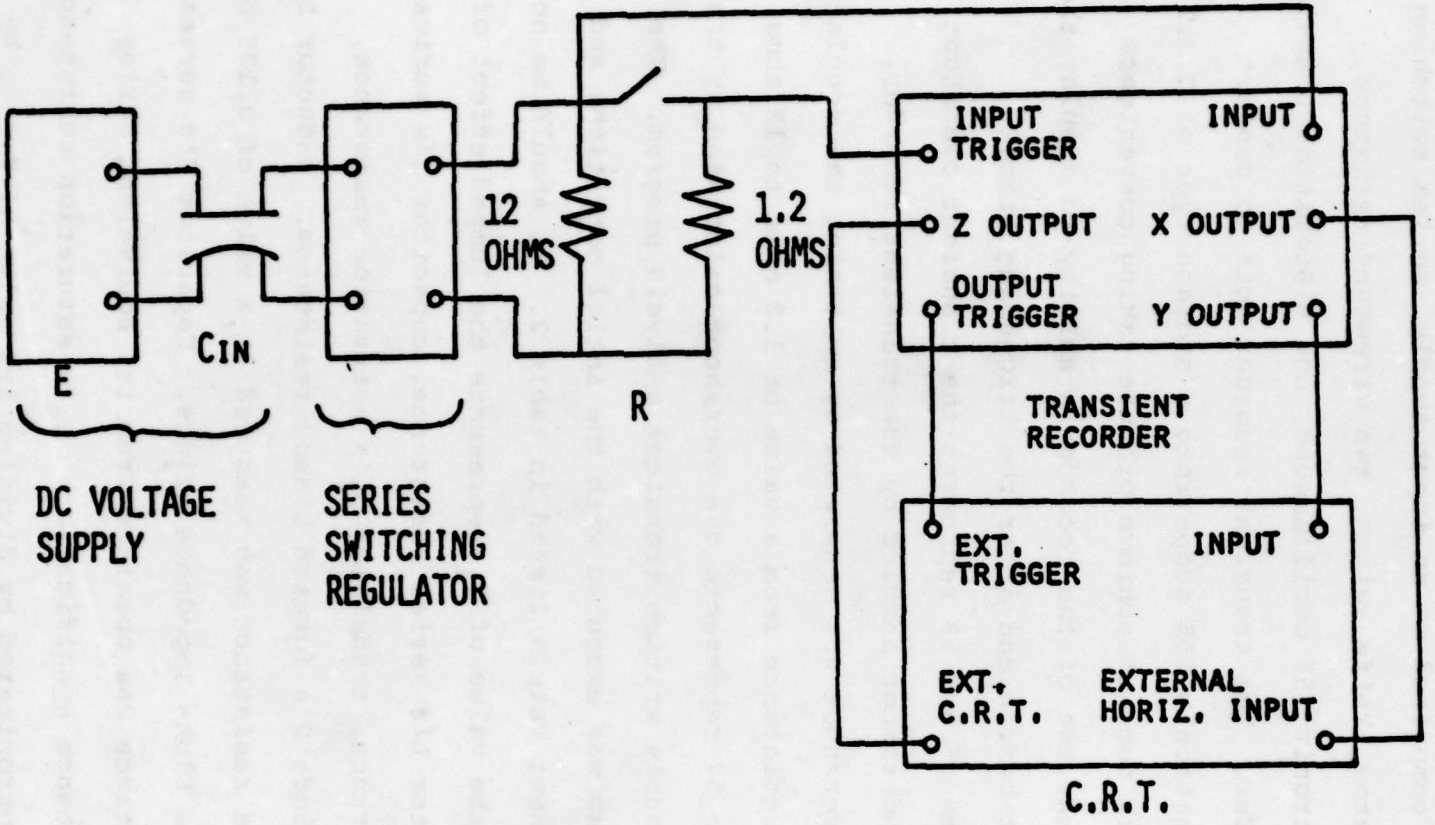

Figure 55. Transient test circuit

It is comprised of an input supply, series switching regulator, knife switch, two wirewound resistors, a Tektronix 555 oscilloscope, and a Biomation transient recorder. The transient recorder acts to convert the Tektronix 555 scope into a storage type of C.R.T. This is done to achieve picture taking convenience and make use of the recorder's ability to display the output before and after the triggering signal. Figures 56 and 58 represent the transient overshoot and undershoot sampled by the transient recorder. The overshoot was generated by switching the regulator's load resistance from a value of 1.2 ohms to 12 ohms. Figure 57 represents the overshoot calculated by the previously written transient analysis program. The program was executed with the intial conditions and component values listed in table 2. It should be noted that the value of R_1 represents the lumped effect of inductor L's series resistance, capacitor C's series resistance, transistor Q_S's saturation resistance, and diode D's forward biased resistance. Inductor L's series resistance was measured at a value of 0.135 ohms with a Fluke impedance bridge. Capacitor C's series resistance was obtained from its equivalent series resistance specification. Q_S's saturation resistance was approximated by dividing its value of V_{ecsat} by

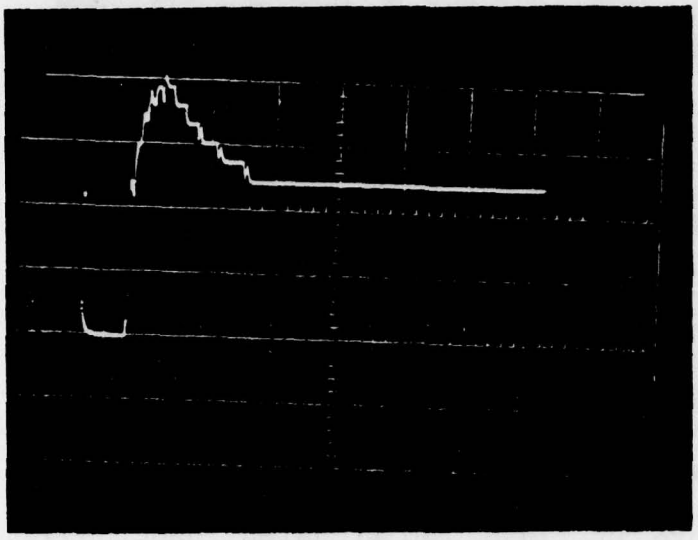

Figure 56. Measured transient overshoot
(vertical = 0.25 V/Div)
(horizontal = 731 usec/Div)

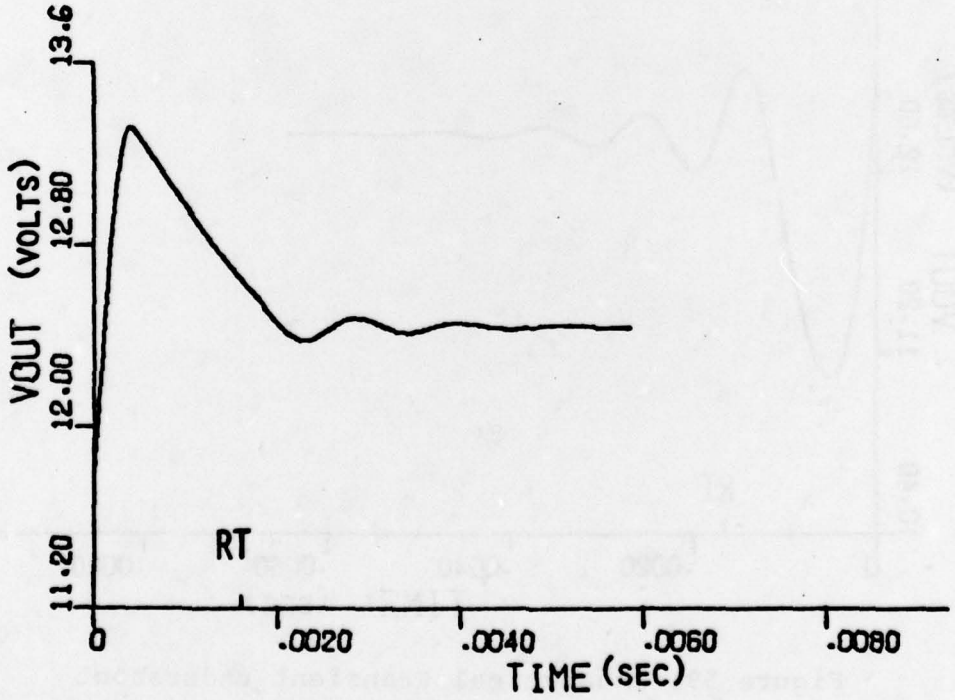

Figure 57. Analytical transient overshoot

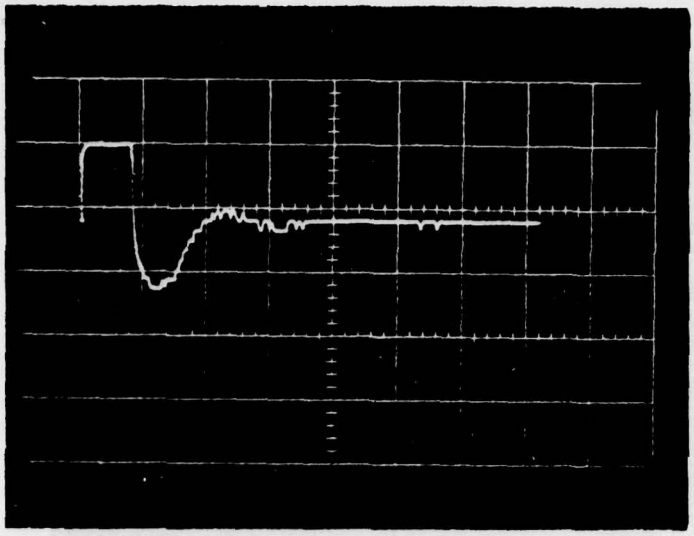

Figure 58. Measured transient undershoot
(vertical = 0.5 V/Div)
(horizontal = 731 usec/Div)

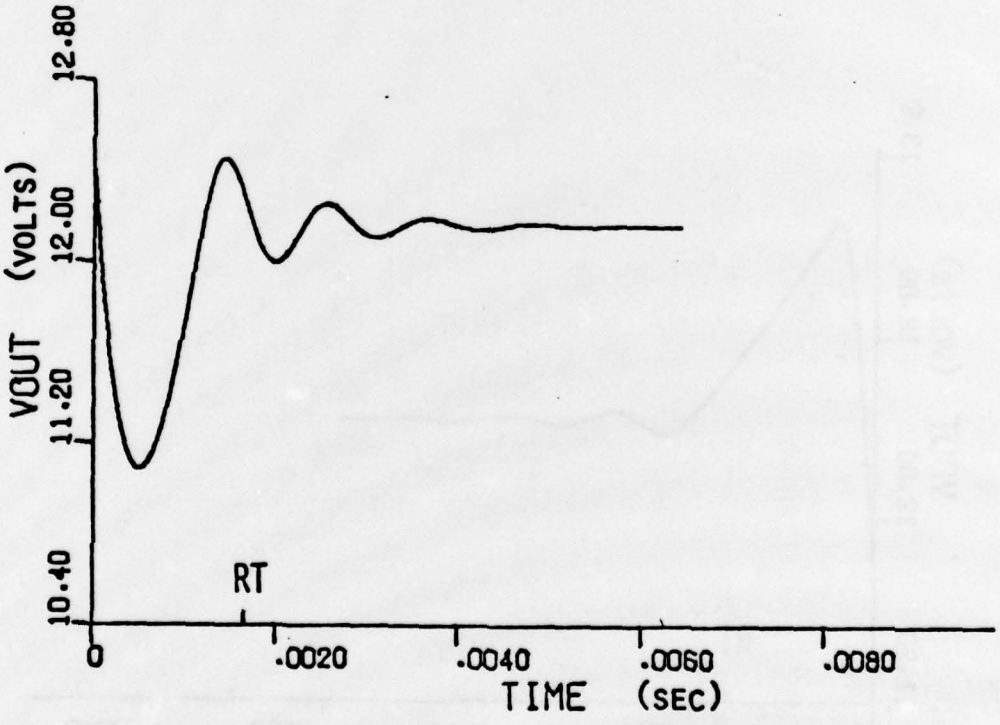

Figure 59. Analytical transient undershoot

Table 2. Definitions of fortran program variables

Variable	Definition	Value	
		Overshoot	Undershoot
V	Input voltage	24 V	24 V
VCO	Voltage across capacitor C at t=0	11.8 V	12.4 V
Duccur	Current through inductor L at t=0	10 A	1 A
R1	Equivalent series resistance	0.466 ohms	0.466 ohms
R2	Load resistance	12 ohms	1.2 ohms
CAP	Value of capacitor C	1600 uF	1600 uF
DUCT	Value of inductor L	0.3 mH	0.3 mH

NOTE: The duty cycle was specified to go from 20% @ V_{out} = 12.4 V to 80% @ V_{out} = 11.4 V in a linear fashion.

I_{csat} when I_{csat} was equal to 5 A. Diode D is a 1N3910 and has a resistive contribution which was determined by dividing its 1.4 V forward drop by 5 A. [22] The effects of Q_S's saturation resistance and diode D's forward biased resistance are only seen during their respective half cycles. Because of this, their values are averaged together to properly reflect their contribution over a complete cycle. By adding this result to the series resistances of inductor L and capacitor C, a value of R_1 can be used which closely reflects the regulator's series component of resistance. The photograph and plot in figures 56 and 57 agree very closely with one another. Differences can only be attributed to the inability of R_1's lumped model to completely simulate the nonlinear nature of R_1. Figure 58 represents the regulator's response when R is switched from a value of 12 ohms to 1.2 ohms. Figure 59 is figure 58's analytical counterpart and results from the initial conditions and component values listed in table 2.

Regulator Efficiency

Values of efficiency were calculated by dividing the regulator's output power by its input power. The

product of measured output voltage and output current produced values of output power while measurements of input voltage and current resulted in values of input power. Measurements were made for values of input voltage ranging from 18 V to 28 V and for values of load resistance between 1.2 ohms and 10 ohms Figure 60 represents the test circuit used. Input and output voltages were measured through the use of a Fluke multimeter. The regulator's output current was determined from a voltage measurement made across a 2.5 mohm current shunt in series with the regulator's load. Unlike the above parameters, the regulator's input current is primarily A.C. As a result, an averaging of the input current had to be made before it could be multiplied by the input voltage. This was achieved by integrating the input current's A.C. component over one cycle of operation, then adding it to the D.C. component. The Lambda Las-14U voltage regulator used all of the D.C. current supplied by the input. The input current's D.C. component was therefore easily measured by the Simpson 260 volt-ohm-milliameter (fig. 60). The input current's A.C. waveform was displayed through the use of a Tektronix P6016 current probe and then integrated by a planimeter. The integral was then divided by the

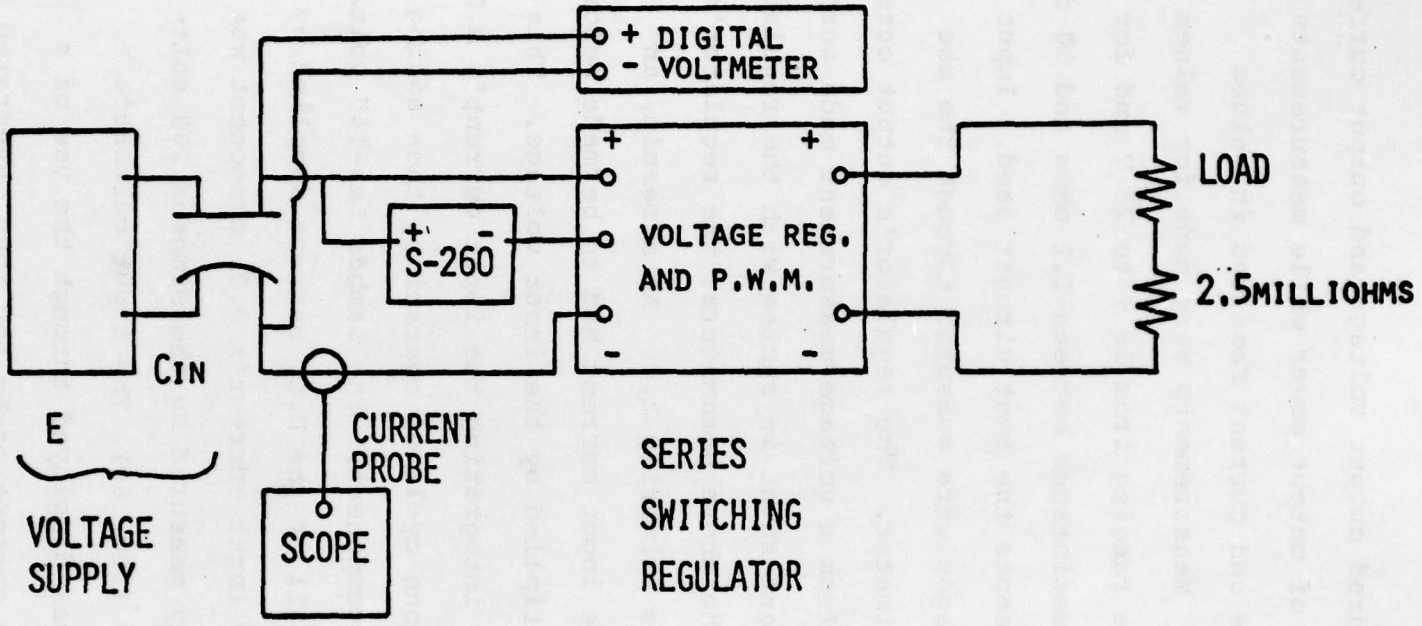

Figure 60. Efficiency test circuit

waveform's period to yield an average value of input current. Figure H-1, appendix H, represents such a waveform. An example of the efficiency calculation just discussed is presented in appendix H. Plots of the regulator's efficiency vs. load are presented in figure 61 for three values of input voltage. A list of the measured data used in the generation of figure 61 appears in table I-1, appendix I. A theoretical curve can also be calculated and compared to measured values.

Figure 61's dashed curve represents a theoretical efficiency curve generated from component measurements and specifications. In an attempt to demonstrate the mechanism by which the curve was generated, a point on the curve will be calculated in detail. An output voltage of 12 V, load resistance of 5 ohms, and duty cycle of 67% will be assumed when the input voltage equals 18 V. Inductor L's series resistance will be assumed to be equal to its measured value of 0.135 ohms and capacitor C's series resistance will be set to its specified value of 0.05 ohms. By assuming a forward biased surrent of 12 V/5 ohms or 2.4 A, a worst-case static forward resistance can be calculated for Diode, D:

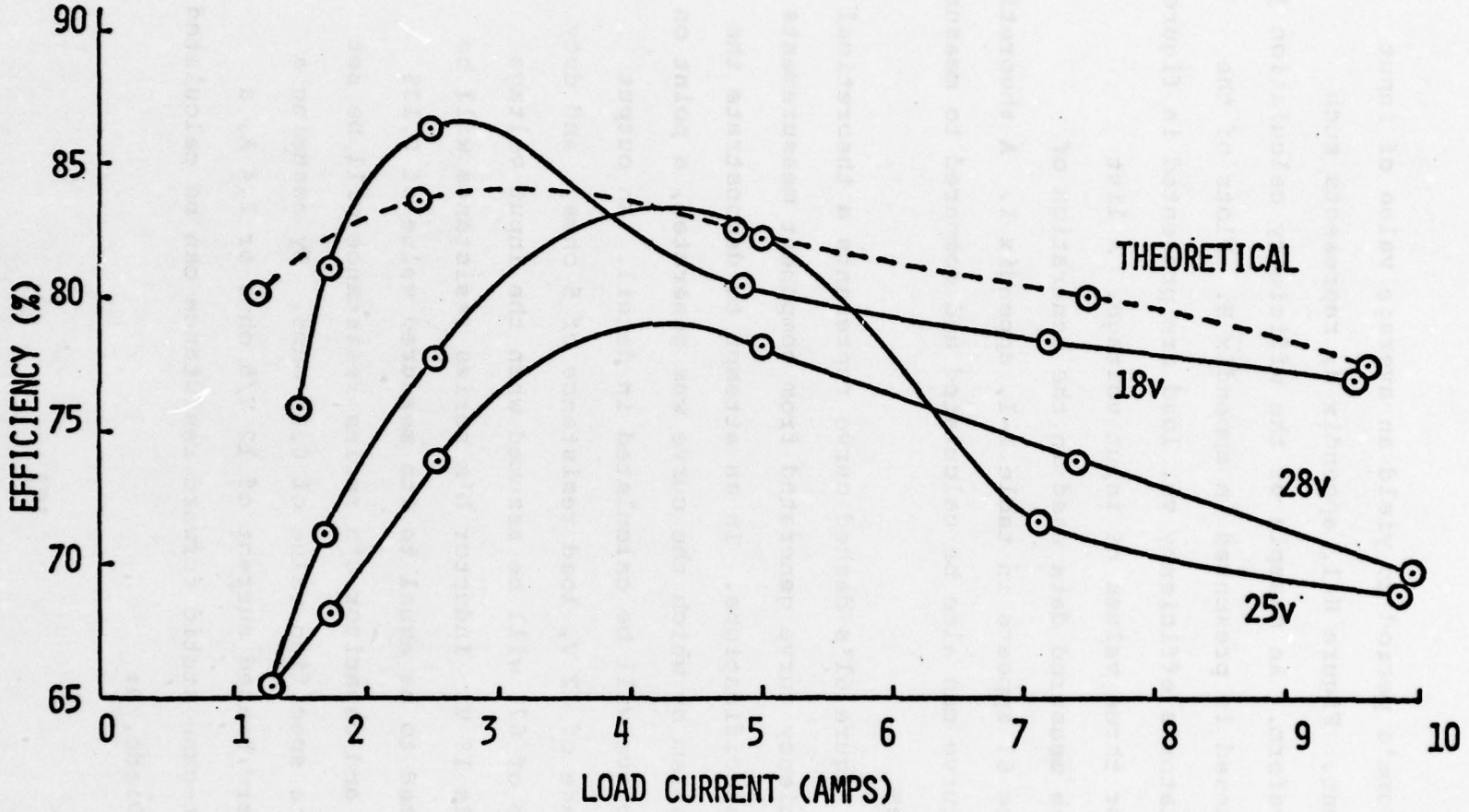

Figure 51. Efficiency vs. load current

$$R_{DIODE} = \frac{V_{FORWARD}}{I_{FORWARD}} = \frac{1.4\ V}{2.4\ A} = .58 \text{ ohms.}$$

Transistor Q_S's saturation resistance can be determined from a curve which specifies V_{ecsat} as a function of I_{csat}. For an I_{csat} of 2.4 A, V_{ecsat} equals 0.85 V R_{sat} results as

$$R_{sat} = \frac{V_{ecsat}}{I_{csat}} = \frac{.85\ V}{2.4\ A} = .354 \text{ ohms.}$$

When the resistive effects of R_{sat} and R_{DIODE} are combined, their total resistive effect, R_T, becomes

$$R_T = .33(R_{DIODE}) + .67(R_{sat}) = .428 \text{ ohms.}$$

When added to the sum of inductor L's series resistance and capacitor C's series resistance, an equivalent value of R_s results.

$$R_s = R_T + R_L + R_{cap} = .613 \text{ ohms.}$$

Substituting into equation 58 yields

$$Eff = \frac{R}{R+R_1} = \frac{5}{5.613} = .89 \quad .$$

This value can be used to determine the input power supplied,

$$P_{in} = \frac{P_{out}}{Eff} = \frac{(12\ V)(2.4\ A)}{.89} = 32.35\ \text{watts} \qquad (92)$$

This value of input power requires further adjustment. It must be refined to reflect the power used in the LAS-14u voltage regulator, pulse width modulator, and current amplifier, and in the charging up of capacitor C_S. The current used by the pulse width modulator/ voltage regulator combination was measured at an input of 18 V and found to be 42 mA. The power used was therefore equal to (42 mA) x (18 V) or 0.756 mW. The power lost in charging capacitor C_S was determined from equation 91, and was equal to 0.9 W. The power lost in the current amplifier was approximately equal to the product of the input voltage, the current through R_C, and the operating duty cycle. Expressed algebraically,

$$P_{ca} = \frac{V_{in}(V_{in}-V_{eb})}{R_C} \quad x \quad (0.67),$$

Yielding

$$P_{ca} = \frac{18(18-1.55)}{500} x \quad (0.67) = 0.398\ \text{Watts}$$

By adding these values to the input power of equation 92, an adjusted value of input power can be generated and used to recalculate the regulator's theoretical value of efficiency. Solving for

efficiency,

$$Eff = \frac{P_{out}}{P_{in}+P_{cap}+P_{mod/reg}+P_{ca}}$$

Yielding

$$Eff = \frac{288}{34.404} = 83.7\% \quad .$$

By comparison, the theoretical curve agrees very closely with its empirical counterpart. The theoretical algorithm just described can therefore be assumed to be a good approximation of regulator efficiency.

Regulation

The regulator was designed to react to both changes in load resistance and input voltage. The graphs in figure 62 show changes in output voltage against input voltage for three values of load resistance. A 10 V change in input voltage results in a 0.4 V change in output voltage. A constant voltage line regulation of 0.04 V/V can therefore be said to exist. [23] A change of approximately 0.3 V also occurs for an 8.75 ohm change in load resistance. This results in a constant voltage load regulation of 0.34 V/ohm. [23]

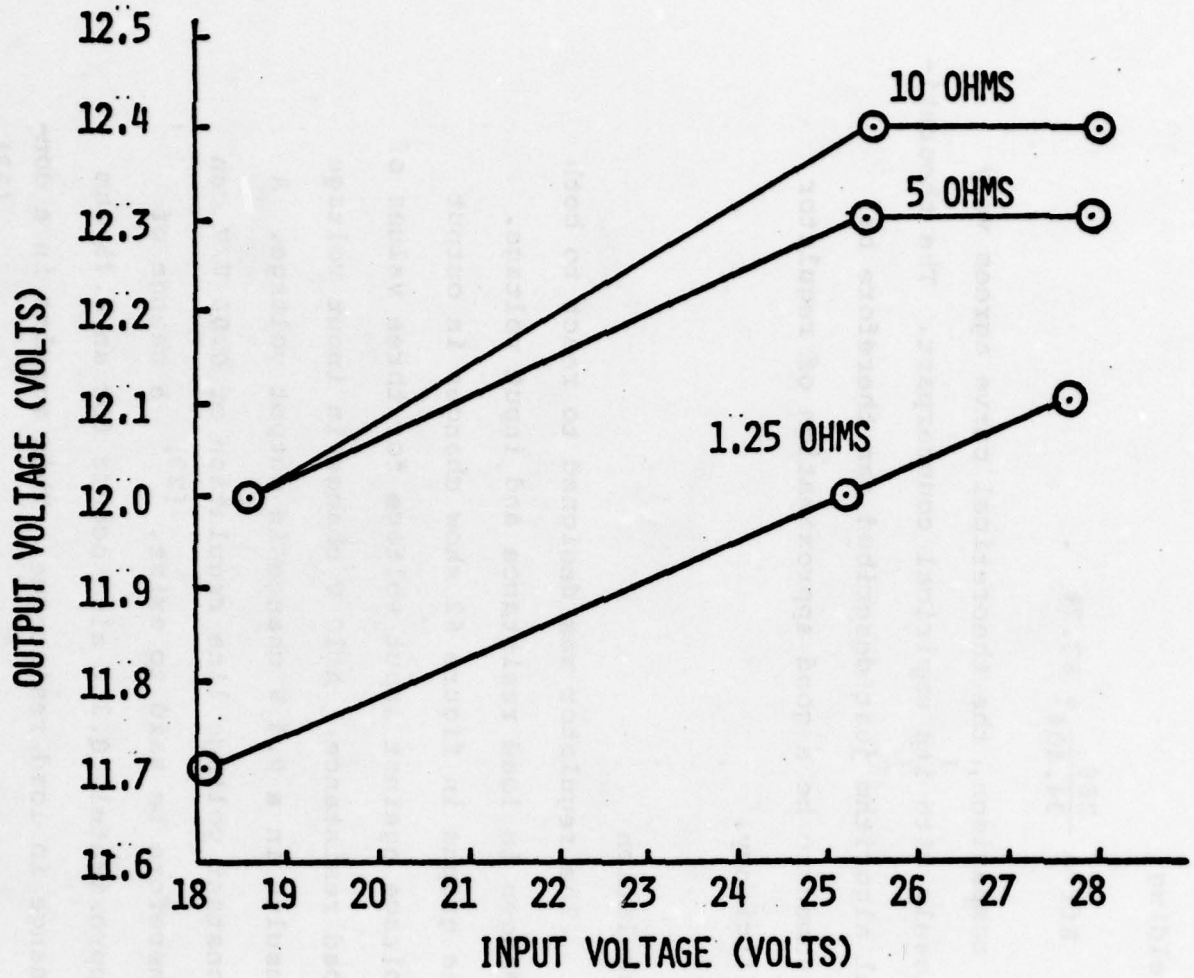

Figure 62. Output voltage vs. input voltage

The values displayed are within the voltage range specified. Had they not conformed to the specification, stage one (figure 47) could have been redesigned with a higher voltage gain. This would have increased the pulse width modulator's sensitivity to changes in output voltage and improved the circuit's overall regulation.

RECOMMENDATIONS

In an attempt to improve regulator operation, the following recommendations are made:

In the case of the circuit's power switching transistor, two possible avenues of improvement stem from its characteristics. The transistor's value of V_{ecsat} is a prime source of loss. Its decrease would yield a definite increase in regulator efficiency. The transistor's other area of improvement lies in an increase in its ability to dissipate power. Such an increase would eliminate the need for any lossy surge supression circuitry. A decrease in diode D's forward voltage drop would also decrease loss and increase efficiency.

The regulator's feedback circuitry also contributes greatly to loss. Its improvement would increase

efficiency, especially for large values of load resistance.

While changes which improve circuit performance are always possible, they are not always practical. In the case of inductor L, for example, a decreased wire gauge would decrease series resistance but only at the expense of increased cost and weight.

As energy problems continue to increase, and the efficiency of the series switching regulator becomes more attractive, it is felt that the demand for improved semiconductors and feedback circuitry will eventually result in regulator efficiencies of over 90%.

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APPENDIX A

12 - VOLT LOAD CURRENT REQUIREMENTS

Table A-1. 12 - volt load current requirements.

Equipment (-)	Voltage (volts)	Current (amps)
Television	12	1.33
Refrigerator	12	3.66
Water Pump	12	2.30
Air Pump	12	9.00
Fluorescent Lights	12	1.25
Vacuum Cleaner	12	10.00

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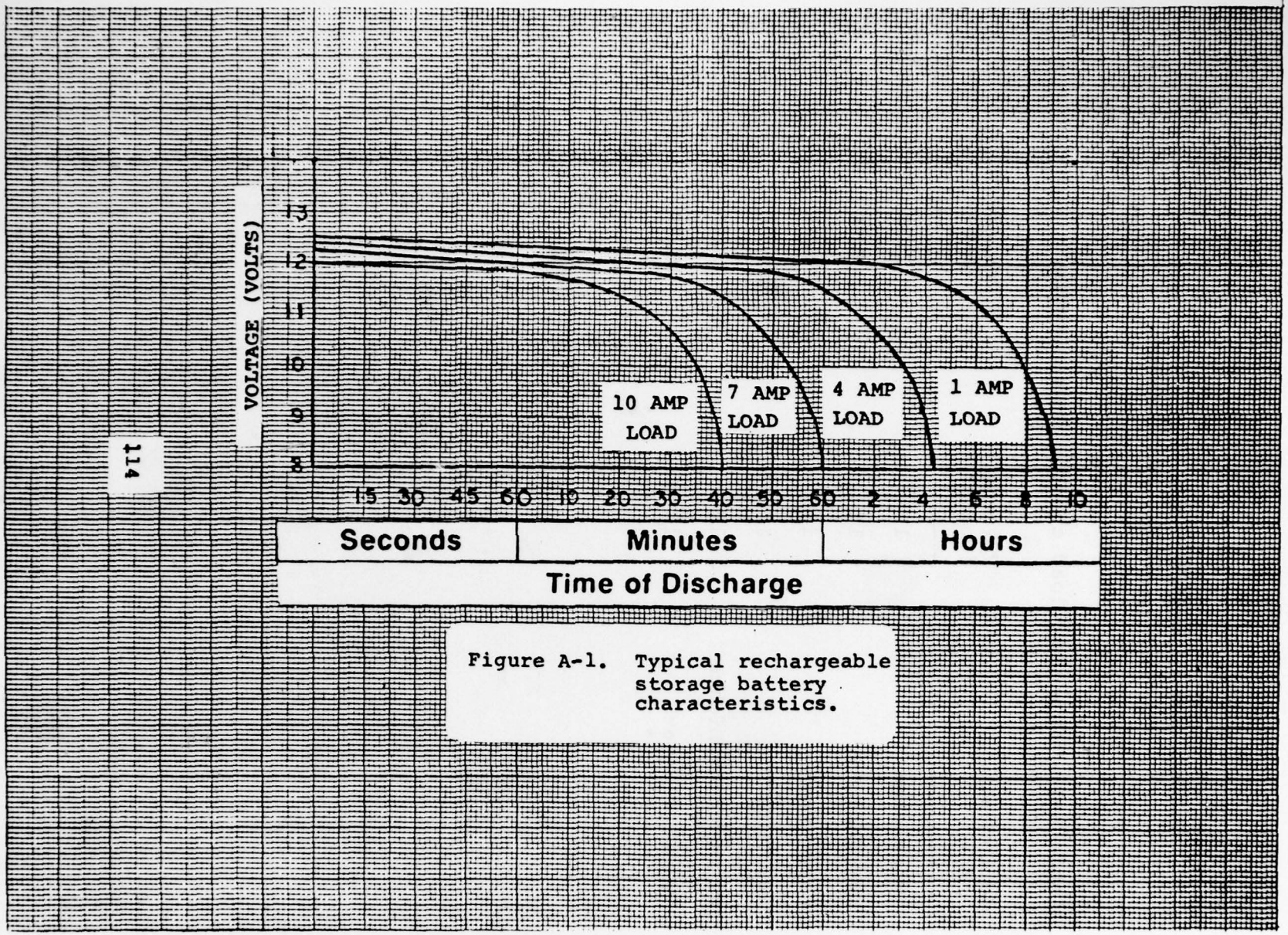

Figure A-1. Typical rechargeable storage battery characteristics.

APPENDIX B

FOURIER SERIES APPROXIMATION OF THE INPUT TO THE REGULATOR FILTER CIRCUIT OF FIGURE 30

This Appendix approximates the input waveform in figure 30.

In general, the Fourier approximation of a periodic function, F(t), is expressed as

$$F(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty} \left\{ a_n \cos \frac{n\pi t}{L} + b_n \sin \frac{n\pi t}{L} \right\}$$

where L = 1/2 period,

$$a_o = \frac{1}{L} \int_o^{2L} f(t)\, dt \quad ,$$

$$a_n = \frac{1}{L} \int_o^{2L} f(t) \cos \frac{n\pi t}{L}\, dt \qquad n=1,2,3...$$

and

$$b_n = \frac{1}{L} \int_o^{2L} f(t) \sin \frac{n\pi t}{L}\, dt \qquad n=1,2,3...$$

Solving for a_o, a_n, and b_n from figure 30,

$$a_o = \frac{1}{L} \left\{ \int_o^{L} 24\, dt + \int_L^{2L} o\, dt \right\} = 24$$

and

$$a_n = \frac{24}{L} \int_o^{L} \cos \frac{n\pi t}{L}\, dt = \frac{24}{n\pi} \sin n\pi, \qquad n=1,2,3...$$

Resulting in

$$a_n = 0 \text{ for all values of } n.$$

$$b_n = \frac{1}{L}\int_o^L 24 \sin \frac{n\pi t}{L}\, dt = \frac{-24}{n\pi} \cos \frac{n\pi t}{L} \Big|_o^L$$

Yielding

$$b_n = \frac{-24}{n\pi} (\cos(n\pi) - \cos(o)).$$

Therefore,

$$b_n = \frac{24}{n\pi} (1 - \cos(n\pi)) \qquad n=1,2,3,4...$$

All even values of n cause b_n to go to zero.

Therefore,

$$F(t) = 12 + \sum_{n=1}^{\infty} b_n \sin \frac{n\pi t}{L} , \qquad n=1,3,5...$$

Resulting in

$$a_n = 0 \text{ for all values of } n.$$

$$b_n = \frac{1}{L}\int_0^L 24 \sin \frac{n\pi t}{L}\, dt = \frac{-24}{n\pi} \cos \frac{n\pi t}{L} \Big|_0^L$$

Yielding

$$b_n = \frac{-24}{n\pi} (\cos(n\pi) - \cos(o)).$$

Therefore,

$$b_n = \frac{24}{n\pi} (1 - \cos(n\pi)) \qquad n=1,2,3,4...$$

All even values of n cause b_n to go to zero.

Therefore,

$$F(t) = 12 + \sum_{n=1}^{\infty} b_n \sin \frac{n\pi t}{L} , \qquad n=1,3,5...$$

APPENDIX C

LAPLACE TRANSFORM SOLUTION OF EQUATIONS 79 AND 80

Equations 79 and 80 are repeated below and are solved to produce an expression for regulator output voltage.

$$V(s) + LI_o - \frac{V_{co}}{S} = I_1(R_1+LS+\frac{1}{CS}) - I_2/CS \qquad (79)$$

$$\frac{V_{co}}{S} = -I_1(\frac{1}{CS}) + I_2(R+\frac{1}{CS}) \qquad (80)$$

Their solution begins with a definition of V(s).[24] V(s) is the Laplace transform of the input to figure 30 and is expressed as

$$V(S) = \frac{V(1-e^{-st_1})}{S(1-e^{-ST})}, \qquad (C-1)$$

where $\frac{V}{S}(1-e^{-St_1})$ represents one cycle of operation,

and $\frac{1}{1-e^{-ST}} = 1+e^{-ST} + e^{-2ST} + e^{-3ST} + \ldots.$

which can also be expressed as

$$\sum_{N=0}^{\infty} e^{-NTS}, \qquad N=0,1,2,3\ldots$$

From equation 80,

$$I_1 = I_2(RCS+1) - CV_{co}. \qquad (C-2)$$

Substituting equation C-2 into equation 79

$$V(S) + LI_o = I_2(LCRS^2+(L+R_1RC)S + (R_1+R)) + (-CV_{co}LS-CV_{co}R_1).$$

Solving for I_2,

$$I_2 = \frac{V(s)+LI_o+CV_{co}LS+CV_{co}R_1}{LCRS^2+(L+R_1RC)S+(R_1+R)} \quad . \qquad (C-3)$$

Solving for V_{out},

$$V_{out} = I_2R \quad .$$

Substituting equation C-3 for I_2,

$$Vo(s) = \frac{RV(s)+RCV_{co}LS+R(CV_{co}R_1+LI_o)}{LCRS^2+(L+R_1RC)S+(R_1+R)} \quad .$$

Factoring the denominator,

$$V_o(s) = \frac{V(s)/CL}{(S-S_1)(S-S_2)} + \frac{V_{co}S}{(S-S_1)(S-S_2)} + \frac{(CV_{co}R_1+LI_o)/CL}{(S-S_1)(S-S_2)}$$

where,

$$S_1,S_2 = \frac{-\left(\frac{L+R_1RC}{LCR}\right) \pm \sqrt{\left(\frac{L+R_1RC}{LCR}\right)^2 - 4\left(\frac{R_1+R}{LCR}\right)}}{2} \quad . \qquad (C-4)$$

Transforming $V_o(s)$ into the time domain,

$$V_o(t) = \mathcal{L}^{-1}\left\{\frac{K_1(1-e^{-St_1})}{S(1-e^{-ST})(S-S_1)(S-S_2)}\right\}$$

$$+ \mathcal{L}^{-1}\left\{\frac{SK_2}{(S-S_1)(S-S_2)}\right\} + \mathcal{L}^{-1}\left\{\frac{K_3}{(S-S_1)(S-S_2)}\right\}$$

where $K_1=V/CL$, $K_2=V_{co}$, and $K_3 = \frac{(CV_{co}R_1+LI_o)}{CL}$.

Rewriting $V_o(t)$,

$$V_o(t) = \mathcal{L}^{-1}\left\{\sum_{N=0}^{\infty} \frac{K_1(1-e^{-St_1})e^{-NTS}}{S(S-S_1)(S-S_2)}\right\}$$

$$+ \mathcal{L}^{-1}\left\{\frac{SK_2}{(S-S_1)(S-S_2)}\right\} + \mathcal{L}^{-1}\left\{\frac{K_3}{(S-S_1)(S-S_2)}\right\} .$$

Finally,

$$V_o(t)= \frac{K_1}{(S_1-S_2)S_1S_2}\sum_{N=0}^{\infty}((S_2e^{S_1(t-NT)} - S_1e^{S_2(t-NT)} + S_1-S_2)\ u(t-NT)$$

$$- (S_2e^{S_1(t-t_1-NT)} - S_1e^{S_2(t-t_1-NT)})\ u(t-t_1-NT))$$

$$+ \frac{K_2}{(S_1-S_2)}(S_1e^{S_1t} - S_2e^{S_2t}) + \frac{K_3}{(S_1-S_2)}(e^{S_1t} - e^{S_2t}) .$$

APPENDIX D

TRANSIENT SIMULATION

FORTRAN PROGRAM

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```
   PROGRAM TRANS(INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
**************************************************
THIS PROGRAM SIMULATES THE OUTPUT VOLTAGE RESPONSE OF A SERIES
SWITCHING REGULATOR.  A LIST OF THE VARIABLES WHICH MUST BE
DEFINED BY THE USER ARE LISTED BELOW.

    VCO = INITIAL VOLTAGE ON THE OUTPUT CAPACITOR IN VOLTS.
 DUCCUR = INITIAL CURRENT THROUGH THE REGULATORS SERIES INDUCTOR IN
          AMPS.
     R1 = RESISTANCE IN SERIES WITH THE REGULATORS INDUCTOR IN OHMS.
   DUCT = VALUE OF THE REGULATORS SERIES INDUCTANCE IN HENRIES.
    CAP = VALUE OF THE REGULATORS OUTPUT CAPACITOR IN FARADS.
     R2 = VALUE OF THE REGULATORS RESISTIVE LOAD IN OHMS.
      V = VALUE OF THE REGULATORS INPUT VOLTAGE IN VOLTS.
**************************************************
   DIMENSION Y(3300),X(3300)
   DIMENSION T1SAV(200)
   TKEEP=0.0
   JJ=0
   DUCCUR=15
   VCO=12
   DUTY=.5
   T1SAV(1)=.50*PER
   SUM=0
   PER=1./30000.
   IJK=0
   SUMSAV=12.
   TIMESAV=0.
   NPOINTS=3200
   XLABLE=4HTIME
   YLABLE=4HVOUT
   XLENGTH=5
   YLENGTH=3
```

```
      LOGX=0
      LOGY=0
      IST=0
      NX=4
      NY=4
      V=24.0
      KSAV=1
      ID=2
      K=6400
      R2=12
      R1=.2
      CAP=1.435E-3
      DUCT=.300E-3
  700 CONTINUE
      AK1=V/(CAP*DUCT)
      AK2=VCO
      AK3=(R1*CAP*VCO+DUCT*DUCCUR)/(CAP*DUCT)
      AL=-(DUCT+R1*R2*CAP)/(2*DUCT*CAP*R2)
      B=SQRT(-AL*AL+((R1+R2)/(DUCT*CAP*R2)))
      CONST=AK1/(AL*AL+B*B)
      DO 100 IT=1,K,ID
      SUBSUM=0.
      TIME=(IT*.000001)-.000001
      KK=(TIME/PER)+1
*****************************************************
      IF(JJ.NE.1) GO TO 80
      IF(CURIND.GT.0.0) GO TO 80
      TIME=TIME+TKEEP
      TSTART=TIME
      VSAVE=SUM
      TIME=TSTART-.000001
      KOLD=TIME/PER
   80 TIME=TIME+.000001
```

```
      KK=TIME/PER
      IF(KK.GT.KOLD) GO TO 110
      TNEW=TIME-TSTART
      SUM=VSAVE*EXP(-TNEW/(R2*CAP))
      IJK=IJK+1
      Y(IJK)=SUM
      X(IJK)=TIME
      WRITE(6,500) TIME,SUM
      IF(IJK.GE.3200) GO TO 210
      GO TO 90
  110 VCO=SUM
      JJ=0
      DUCCUR=0.0
      TKEEP=TIME
      T1SAV(1)=-SUM*.8*PER+10.1*PER
      IF(T1SAV(1).GT.(.9*PER))T1SAV(1)=.9*PER
      IF(T1SAV(1).LT.(.1*PER))T1SAV(1)=.1*PER
      DUTY=T1SAV(1)/PER
      SUMSAV=SUM
      TIMESAV=0.0
      IFLAG=0
      GO TO 700
C*****************************************************
   80 CONTINUE
      DO 200 IJ=1,KK
      N=IJ-1
      AN=N
      F=TIME-AN*PER
      II=1
      IF(F.LE.0.0)II=0
      G=TIME-T1SAV(IJ)-AN*PER
      JJ=1
      IF(G.LE.0.0)JJ=0
      CONST1=(AK1/(AL*AL+B*B))*II
```

```
      CONST2=-(AK1/(AL*AL+B*B))*JJ
      A=(AK1/(AL*AL+B*B))*EXP(AL*F)*((AL/B)*SIN(B*F)-COS(B*F))*II
      C=(AK1/(AL*AL+B*B))*EXP(AL*G)*((-AL/B)*SIN(B*G)+COS(B*G))*JJ
      SUBSUM=A+C+SUBSUM+CONST1+CONST2
      KSAV=KK
  200 CONTINUE
      KK=KSAV
      D=AK2*EXP(AL*TIME)*((AL/B)*SIN(B*TIME)+COS(B*TIME))+((AK3*EXP(AL
     1*TIME))/B)*SIN(B*TIME)
      SUM=D+SUBSUM
      IF(JJ.EQ.1) GO TO 50
      T1SAV(KK)=-SUM*.8*PER+10 .1*PER
      IF(T1SAV(KK).GT.(.9*PER))T1SAV(KK)=.9*PER
      IF(T1SAV(KK).LT.(.1*PER))T1SAV(KK)=.1*PER
   50 CONTINUE
      DUTY=T1SAV(KK)/PER
      TOUT=TIME+TKEEP
C     WRITE(6,500) TIME,SUM,DUTY
      WRITE(6,500)TOUT,SUM,DUTY
  500 FORMAT(5X,F20.15,5X,F10.5,F10.5)
      CALL DERIV(SUM,TIME,CAP,VCO,R2,CURIND,SUMSAV,TIMESAV,IFLAG,DUCCUR)
      IJK=IJK+1
      Y(IJK)=SUM
      X(IJK)=TOUT
C     X(IJK)=TIME
      IF(IJK.GE.3200) GO TO 210
      LL=KK+1
      T1SAV(LL)=-SUM*.8*PER+10 .1*PER
      IF(T1SAV(LL).GT.(.9*PER))T1SAV(LL)=.9*PER
      IF(T1SAV(LL).LT.(.1*PER))T1SAV(LL)=.1*PER
  100 CONTINUE
  210 CONTINUE
      CALL GRAPH(X,Y,NPOINTS,XLABLE,NX,YLABLE,NY,XLENGTH,YLENGTH,LOGX,LO
     1GY,IST)
      STOP
      END
```

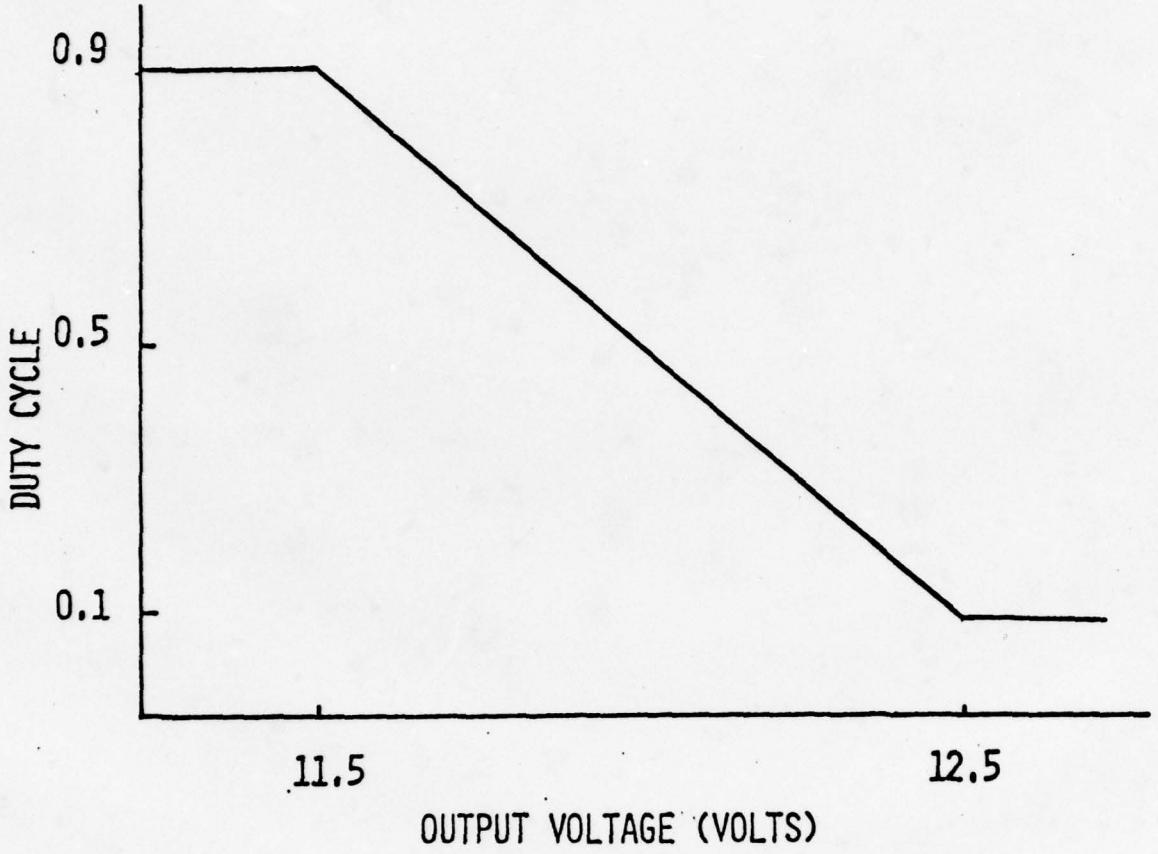

Figure D-1. Duty cycle vs. output voltage

APPENDIX E

ASTABLE MULTIVIBRATOR OPERATION

This Appendix discusses standard astable multivibrator operation and investigates modifications which result in its operation as a pulse width modulator.[25] An astable multivibrator (figure E-1) operates as follows:

If, at $t=0^-$, Q_1 is assumed to be off, just going on, and Q_2 is on just going off, the following initial conditions result:

$$V_{C2}(0^-) = -(V_{cc}-V_{be})$$

$$V_{C1}(0^-) = V_{be}.$$

As Q_1 goes on, Q_2 goes off, and Q_1 stays on until V_{C2} equals V_{be}. Monitoring the voltage across C2,

$$V_{C2} = (V_{cc}-(-(V_{cc}-V_{be}))) \ (1-e^{-t/R_2C_2}) - (V_{cc}-V_{be})$$

Therefore,

$$V_{C2} = V_{cc} -(2V_{cc}-V_{be}) \ e^{-t/R_2C_2} . \qquad \text{(E-1)}$$

If Q_2 turns on at time $t=t_1$, $V_{C2}(t_1)=V_{be}$. Substituting into equation E-1,

$$V_{be}-V_{cc} = -(2V_{cc}-V_{be}) \ e^{-t_1/R_2C_2}$$

Therefore,

$$e^{-t_1/R_2C_2} = \frac{V_{cc}-V_{be}}{2V_{cc}-V_{be}} . \qquad \text{(E-2)}$$

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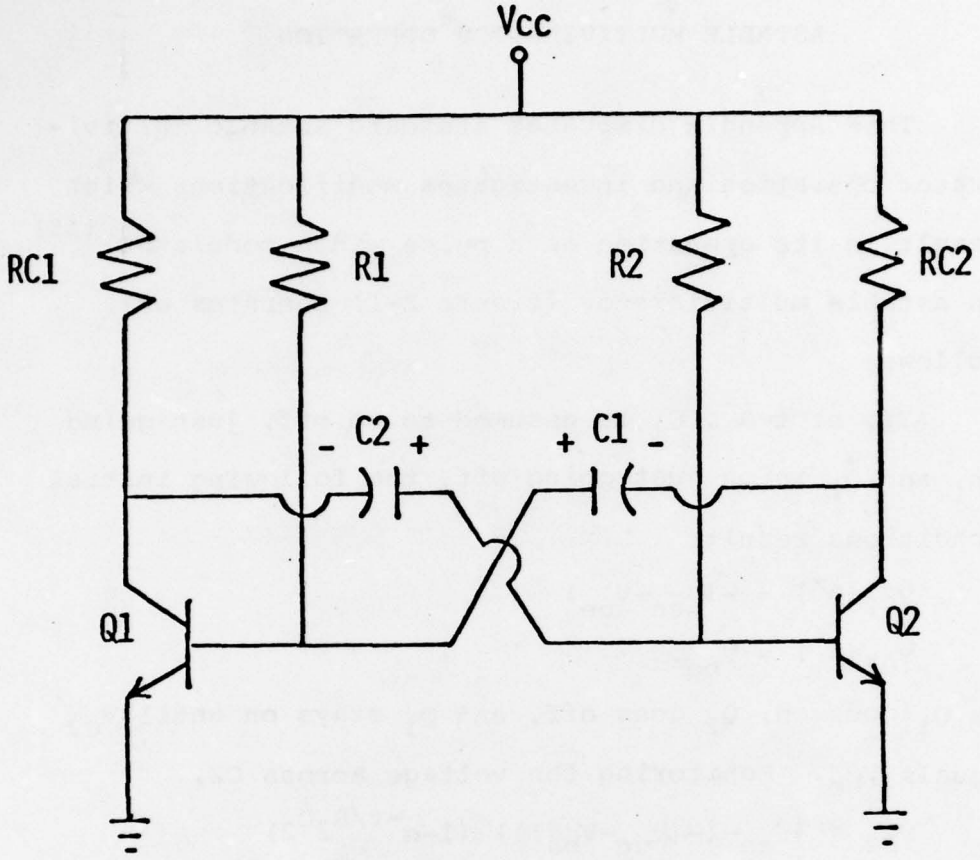

Figure E-1. Astable multivibrator

Solving for t_1,

$$t_1 = -R_2C_2 \ln \left\{ \frac{V_{cc}-V_{be}}{2V_{cc}-V_{be}} \right\}$$

When Q_1 is on, just going off, and Q_2 is off, just going on, the initial conditions are

$$V_{C2}(t_1^-) = V_{be}$$

and

$$V_{C1}(t_1^-) = -(V_{cc}-V_{be}).$$

Since $V_{C1}(t_2) = V_{be}$,

$$V_{C1}(t_2) = V_{be} = (V_{cc}+(V_{cc}-V_{be}))\ (1-e^{-t_1/R_2C_2}) - (V_{cc}-V_{be}) \quad .$$

Solving for t_2,

$$t_2 = -R_1C_1 \ln \left\{ \frac{V_{cc}-V_{be}}{2V_{cc}-V_{be}} \right\} \quad . \qquad \text{(E-3)}$$

One cycle of operation has just been described defining the period as

$$T = t_1 + t_2 \quad .$$

If $R_1 = R_2$ and $C_1 = C_2$, a 50% duty cycle is maintained unless the value of V_{cc}, in equation E-2 differs from that of V_{cc} in equation E-3. With this in mind, the modified astable multivibrator of figure E-2 can now be analyzed.

As with the conventional multivibrator of figure E-1, Q_1 will be assumed to be off, just going on,

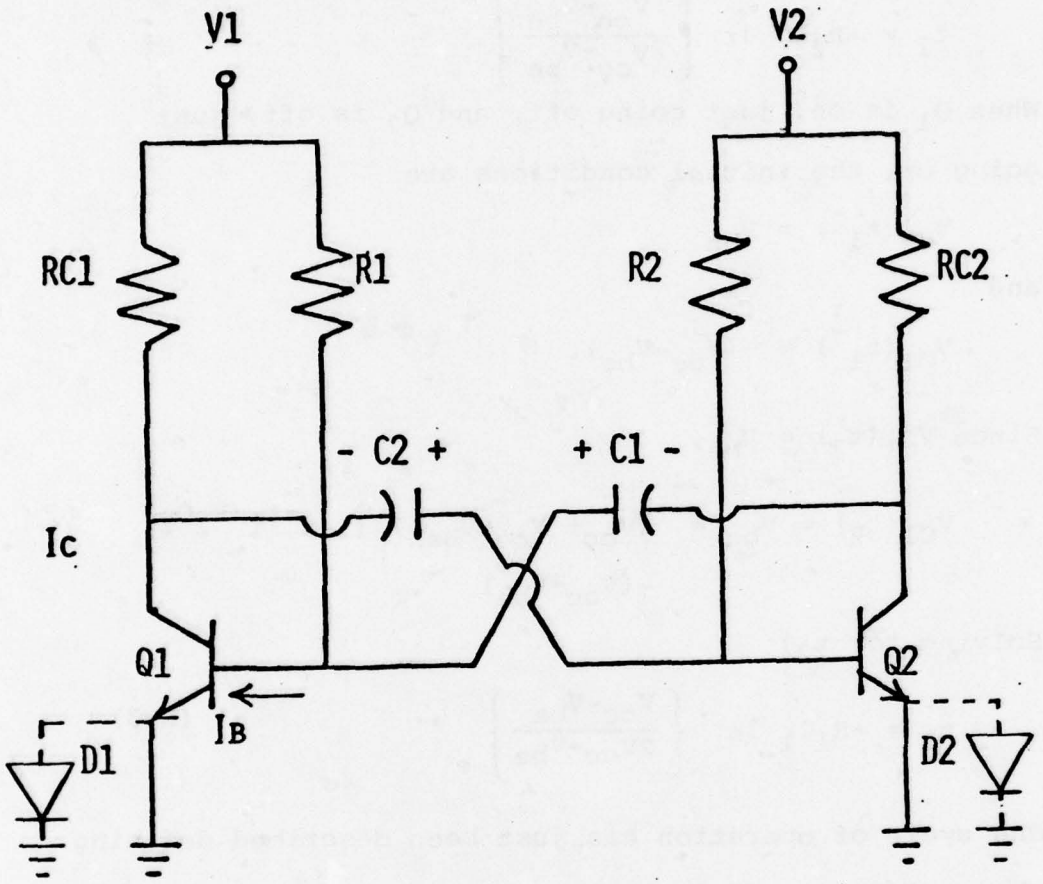

Figure E-2. Modified astable multivibrator

while Q_2 will be assumed on, just going off. Therefore,

$$V_{C2}(0^-) = -(V_1-V_{be}) \qquad \text{(E-4)}$$

and

$$V_{C1}(0^-) = V_{be}. \qquad \text{(E-5)}$$

As Q_1 goes on, Q_2 goes off and V_{C2} can be expressed as

$$V_{C2} = (V_2-(-(V_1-V_{be})))(1- e^{-t/R_2C_2}) - (V_1-V_{be}) \quad . \qquad \text{(E-6)}$$

If Q_2 turns on at $t=t_1$, $V_{C2}(t_1) = V_{be}$. Substituting into equation E-6,

$$V_{be} = (V_2+V_1-V_{be})\ (1- e^{-t_1/R_2C_2}) + V_{be}-V_1.$$

Solving for t_1,

$$t_1 = -R_2C_2\ \ln \left\{ \frac{V_2-V_{be}}{V_1+V_2-V_{be}} \right\} \quad . \qquad \text{(E-7)}$$

For the case where Q_2 is off, just going on, and Q_2 is on, just going off,

$$V_{C1}(t_1^-) = -(V_2-V_{be}) \qquad \text{(E-8)}$$

and

$$V_{C2}(t_1^-) = V_{be} \qquad \text{(E-9)}$$

Therefore,

$$V_{C1} = (V_1-(-(V_2-V_{be})))\ (1-e^{-t/R_1C_1}) -(V_2-V_{be}) \qquad \text{(E-10)}$$

Since Q_1 turns on at $t=t_2$, $V_{C1}(t_2) = V_{be}$. Substituting

into Equation E-10, and solving for t_2,

$$t_2 = -R_1C_1 \ln \left\{ \frac{V_1-V_{be}}{V_1+V_2-V_{be}} \right\} . \qquad \text{(E-11)}$$

Equations E-7 and E-11 can be rewritten as

$$t_1 = KK_1 \ln \left\{ \frac{(V_2-V_{be})}{KK_2} \right\} \qquad \text{(E-12)}$$

and

$$t_2 = KK_1 \ln \left\{ \frac{(V_1-V_{be})}{KK_2} \right\} \qquad \text{(E-13)}$$

where $KK_1 = -R_1C_1 = -R_2C_2$, and $KK_2 = V_1+V_2-V_{be}$.

Table E-1. Component value of figure E-2

Element	Value
Q_1, Q_2	2N2222A
D_1, D_2	1N486A equivalent (1N541)
R_{C1}, R_{C2}	13K ohms
R_1, R_2	390K ohms
C_1, C_2	58 pf
V_1	3 V 13 V
V_2	13 V 3 V

APPENDIX F

COMPARISON BETWEEN A LOW-INDUCTANCE CAPACITOR AND A CONVENTIONAL CAPACITOR.

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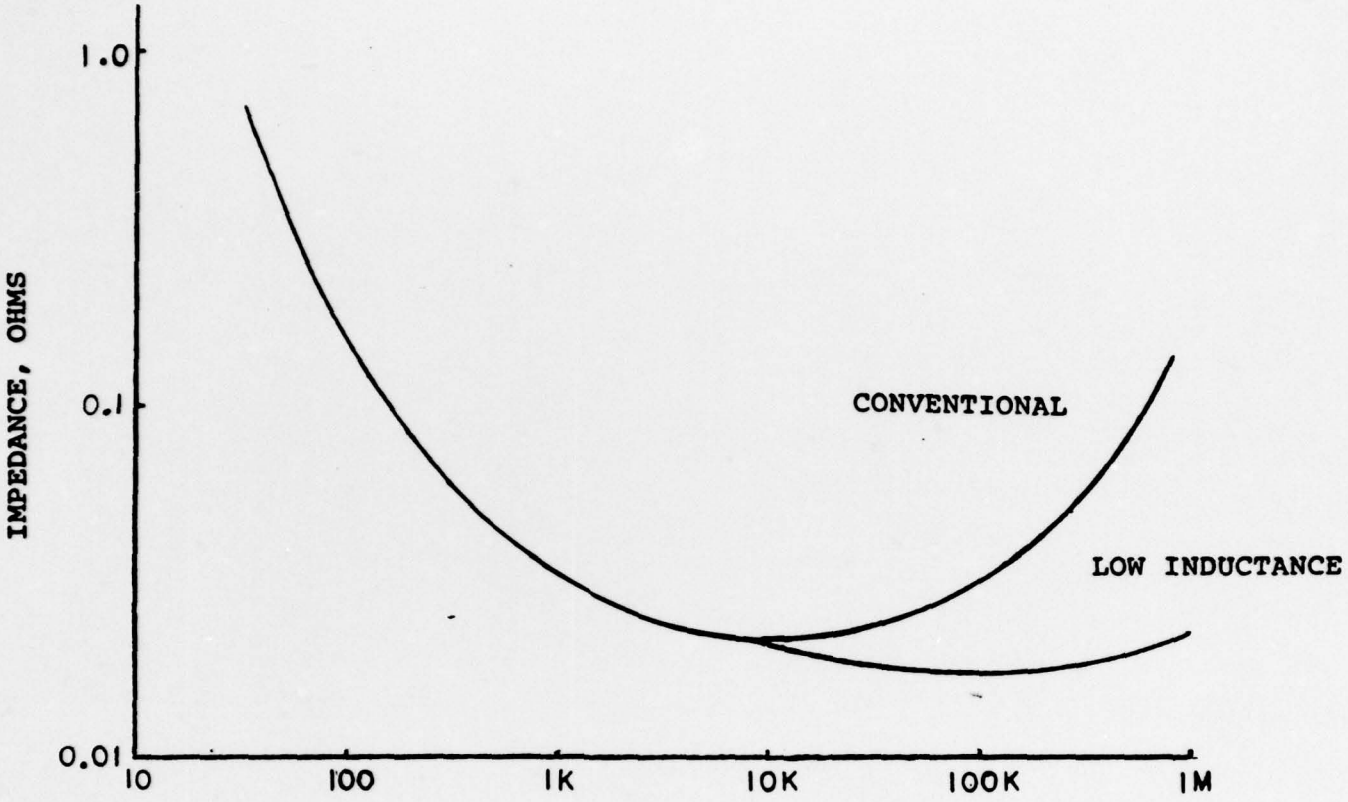

Figure F-1. Convential vs. low inductance capacitor comparison

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APPENDIX G

INSTRUMENTATION
(CURRENT PROBE CALIBRATION AND EQUIPMENT LIST)

This appendix deals with the method used to properly confirm the accurate calibration of the Tektronix P6016 current probe. The circuit used was that of figure G-1. It was used in the following manner: The current probe was placed in the circuit as shown. Trinsistor Q's base was then driven with a square wave of 30 kHz. Transistor Q reacted by oscillating between saturation and cutoff. Figure G-2 represents the current waveform seen by both the current probe and resistor R_4 during oscillation. Figure G-3 represents the voltage waveform seen across resistor R_4 with a standard voltage probe. By dividing the maximum voltage of figure G-3 by the bridge-measured value of R_4, the current values obtained from both figures disagree by 7.6%. A detailed description of this calculation follows

The voltage obtained from figure G-3 is 9.2 V. Divided by a value of R_4=4.75 ohms, it yields a current of 1.937 A. Comparing this result to a value of 1.8 A obtained from figure G-2, a difference of 0.137 A can be seen to exist. When compared to the current probe's reading, an error of 7.6% can be calculated. This is

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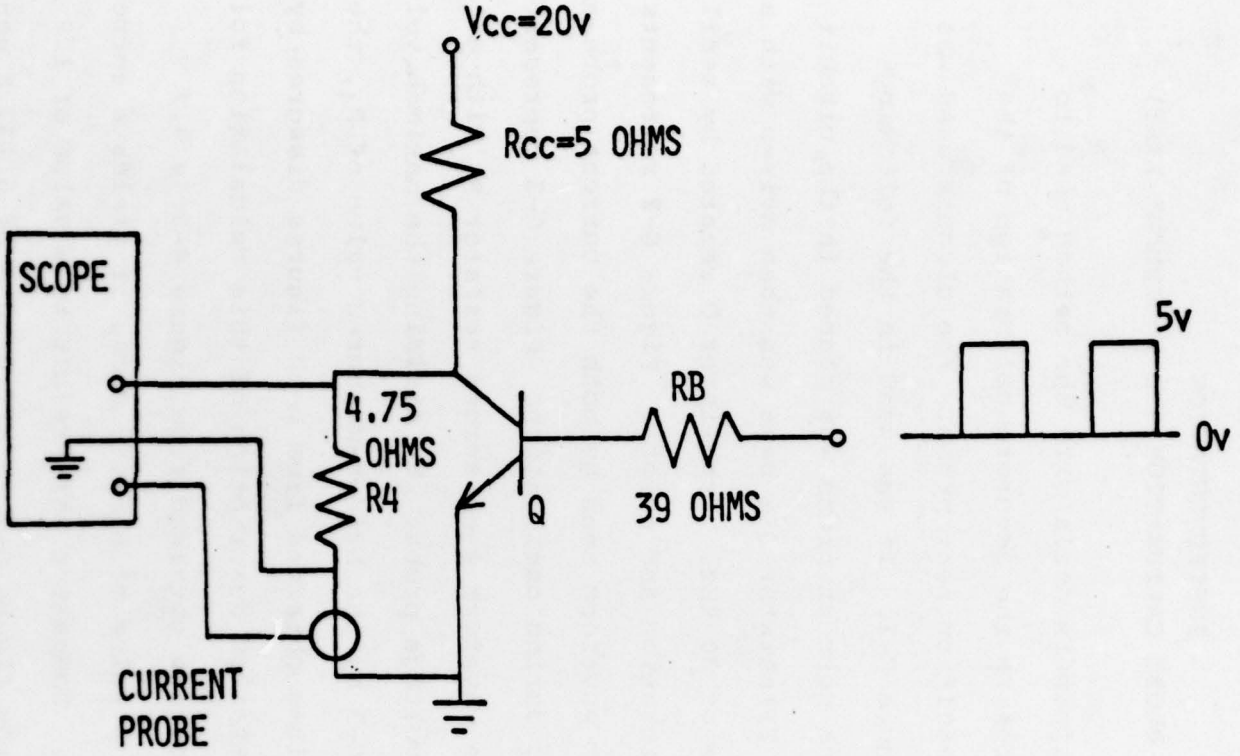

Figure G-1. Current probe calibration circuit

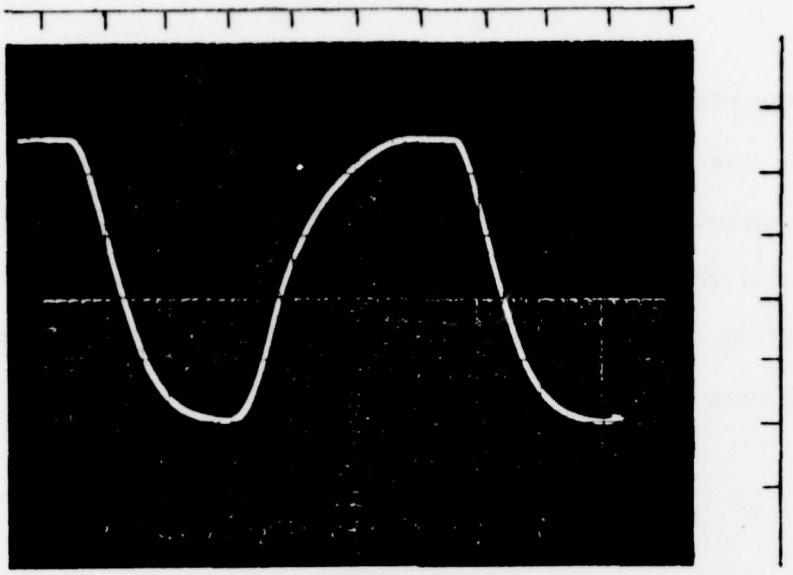

Figure G-2. Current probe waveform
(vertical = 0.4 A/Div)
(horizontal = 5 usec/Div)

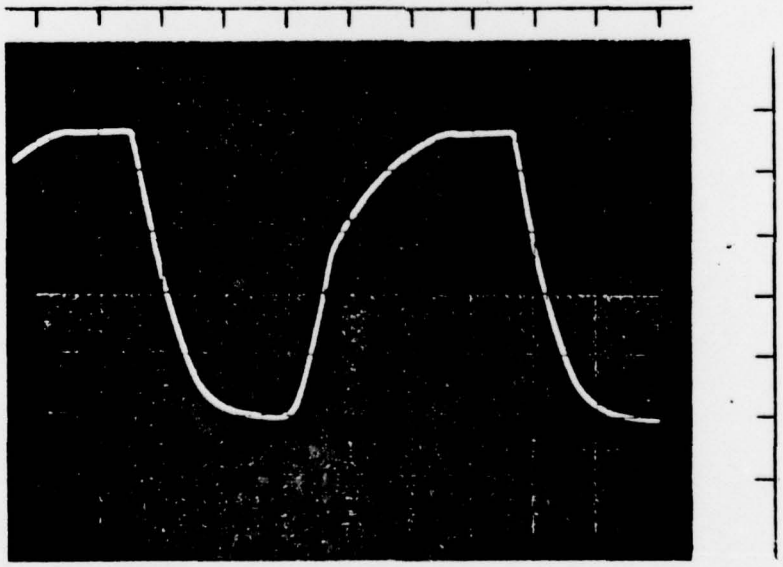

Figure G-3. Voltage probe waveform
(vertical = 2 V/Div)
(horizontal = 5 usec/Div)

an important result because it represents the adjustment which must be made to the average input currents measured when calculating efficiency. The only other difference between the waveforms is that the current waveform slightly lags the votage waveform due to the inductive influence present in wirewound resistor R_4.

Table G-1. Equipment list

1. Trygon DC Power Supply - Model RS40-10 40v, 10A
2. Deltron Inc. DC Power Supply - Model RP30-1 40v, 2.5A
3. Intercontinental Instruments Inc. Pulse Generator - Model PG-32
4. Tektronix - Model 555 Dual Beam Oscilloscope
5. Tektronix - Model 434 Storage Oscilloscope
6. Tektronix - Model 545B Oscilloscope
7. Hewlett Packard Oscilloscope Camera Model 196A
8. Tektronix Oscilloscope Camera Model C-30
9. Tektronix Current Probe and Termination Model P6016
10. Weston Electrical Instrument Corp. 20AMP Shunt, 50 mV drop
11. John Fluke Impedance Bridge Model 710A
12. Simpson Volt-Ohm-Millimater Model 260
13. Fluke Digital Multimeer Model 8000A
14. Radio Frequency Laboratories Inc. AC-DC Instrument Calibration Standard - Model 829D
15. Bruning OTT Compensating Polar Plainimeter - Type 16
16. Biomation Transient Recorder Model 610B

APPENDIX H

EFFICIENCY CALCULATION EXAMPLE

This appendix demonstrates the method used in determining regulator efficiency. Figure H-1 represents the A.C. component of the input's current waveform. By integrating the waveform with a planimeter, a value of 8.96 cm^2 can be obtained for the area under the curve. An average height in centimeters can then be obtained by dividing the area by the waveforms's period. The period is measured to be 5.91 cm, and produces an average height of 1.490 cm. This value is then increased by the 7.6% current probe adjustment described in appendix G. A value of 1.6 cm results. Since one division on the photograph is equal to 0.889 cm, an average current can be calculated as

$$I_{avg} = 1.6 \text{ cm} \times \frac{1 \text{ DIV}}{0.889 \text{cm}} \times \frac{1 \text{ A}}{1 \text{ DIV}} = 1.81 \text{ A.}$$

The input current is then calculated by adding this value to the measured DC current presented in appendix I. A sum of 1.852 is then multiplied by an input voltage of 18.6 V to generate an input power of 34.45 watts. The efficiency can then be calculated by dividing the input power into the product of output current and output voltage. Table I-1 of appendix I

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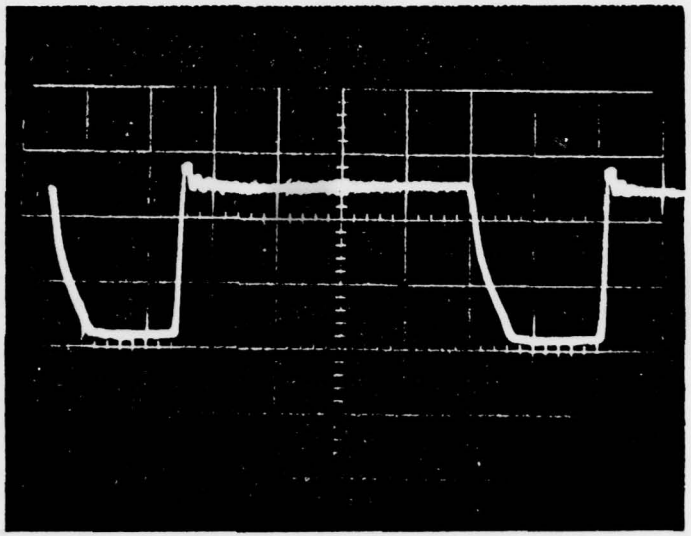

Figure H-1. A.C. component of input current
(vertical = 1 A/Div)
(horizontal = 5 usec/Div)

lists these values as 2.48 A and 12 V. This yields a peak efficiency result of,

$$EFF = \frac{(12)(2.48)}{34.45} = 86.4\% \ .$$

APPENDIX I

MEASURED DATA USED IN EFFICIENCY AND RIPPLE FACTOR CALCULATIONS

Table I-1. Measured data

V_{iout}(mV)	I_{out}(A)	V_{out}(V)	V_{in}(V)	I_{in}(A)	R(Ω)	Eff(%)
23.7	9.48	11.7	18.1	17.917	1.25	77.0
18.0	7.20	11.8	18.4	5.83	1.60	78.6
12.1	4.84	11.9	18.5	3.83	2.50	80.4
6.2	2.48	12.0	18.6	1.81	5.00	86.4
4.2	1.70	11.9	18.1	1.33	7.50	81.3
3.1	1.24	12.0	18.6	1.01	10.00	75.9
24.6	9.84	12.0	25.2	6.74	1.25	69.0
17.8	7.12	12.1	25.3	4.70	1.60	71.7
12.5	5.00	12.2	25.4	2.87	2.50	82.3
6.3	2.52	12.3	25.4	1.52	5.00	77.8
4.2	1.68	12.3	25.0	1.108	7.50	71.2
3.2	1.28	12.4	25.5	0.898	10.00	65.7
24.8	9.92	12.1	27.7	6.15	1.25	69.9
18.5	7.4	12.2	27.8	4.34	1.60	73.9
12.5	5.0	12.2	27.9	2.74	2.50	78.3
6.3	2.52	12.3	27.9	1.45	5.00	74.0
4.3	1.72	12.3	28.0	1.054	7.50	68.3
3.2	1.28	12.4	28.0	0.816	10.00	65.3

I_{in}(DC) @ V_{in} = 18v = 42 mA

@ V_{in} = 25v = 50 mA

@ V_{in} = 28v = 52 mA

$I_{out} = .4 \times V_{iout}$

Miscellaneous

L = .3 mH

R_1 = .135 ohms

R_4 = 4.75 ohms

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Table I-2. Measured output data

R(ohms)	V_{rms} (mV)	V_{dc} (V)	RIPPLE Factor (%)
1.0	8.4	12.3	0.068
7.5	8.1	12.2	0.066
5.0	8.1	12.2	0.066
2.5	7.7	12.1	0.064
1.6	7.3	12.0	0.061
1.25	7.0	12.0	0.058

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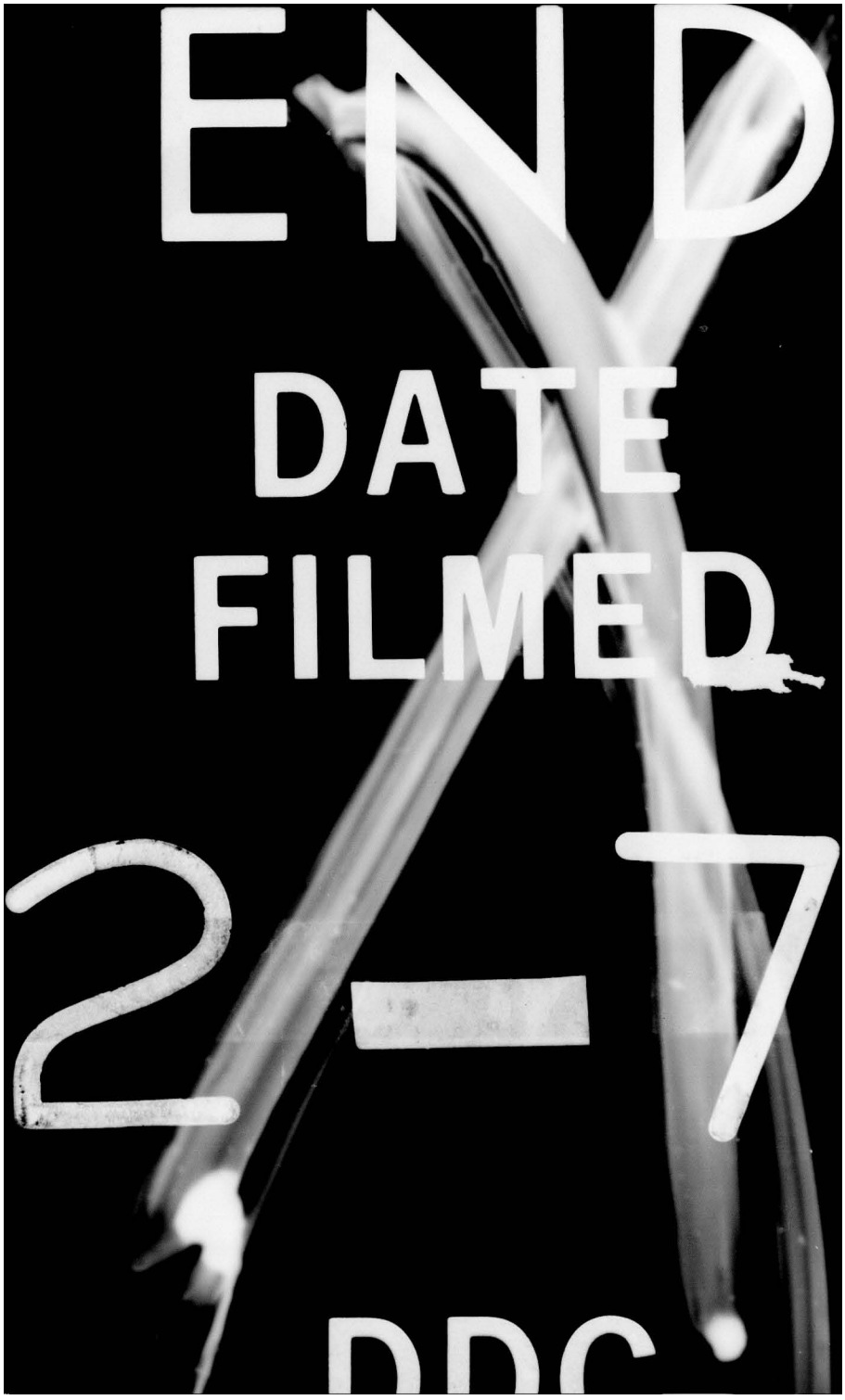
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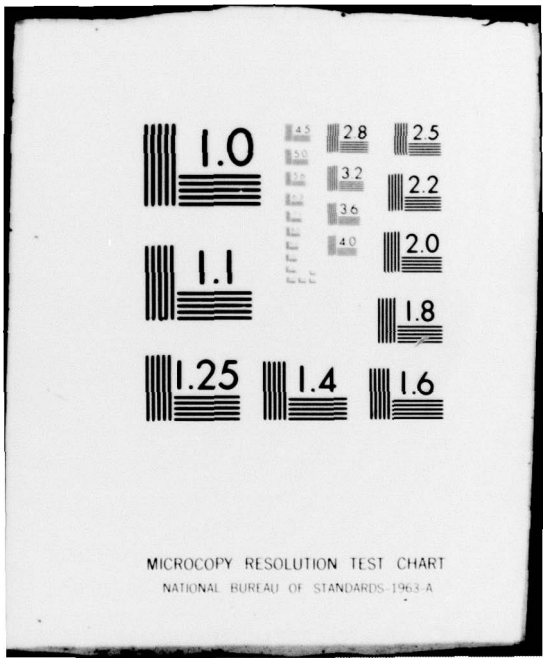
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THE APPLICATION OF DC-DC ENERGY CONVERSION IN A SOLAR ENERGY SYSTEM

John P. Tobak

September 1979

Make the following changes in Technical Report ARMID-TR-78002:

1. In the List of Figures, change page number for figures 15 and 16 to 25.1.

2. Add the attached page 25.1 following page 25.

3. Correct title of appendix F, page 137, to read: COMPARISON BETWEEN A LOW-INDUCTANCE CAPACITOR AND A CONVENTIONAL CAPACITOR.

14 July 1980

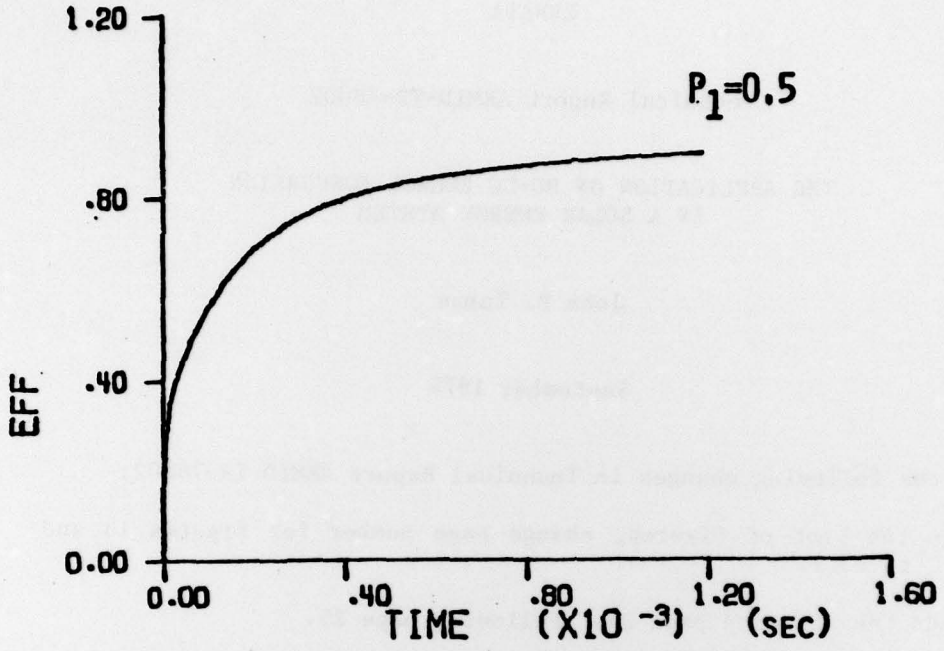

Figure 15. Doubler efficiency (P_1=0.5)

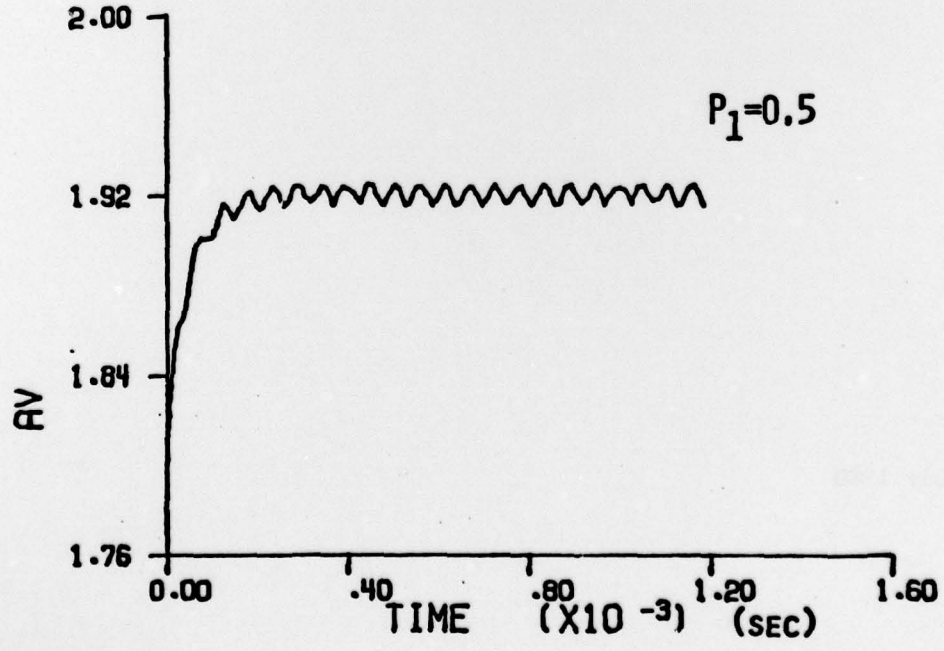

Figure 16. Doubler voltage gain (P_1=0.5)