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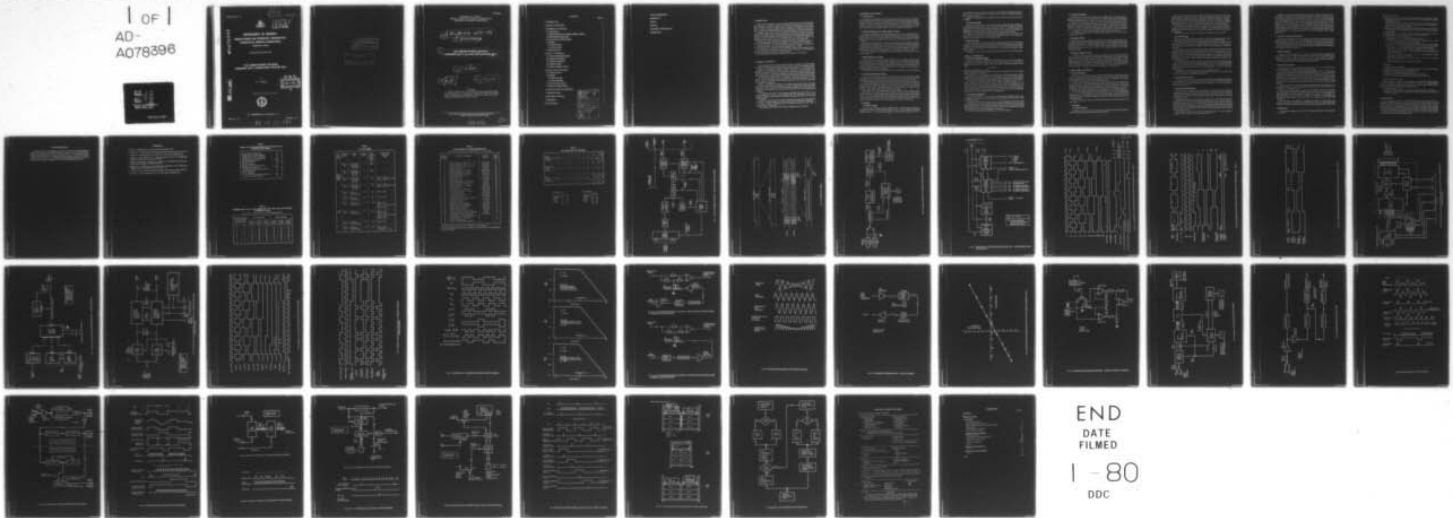
AERONAUTICAL RESEARCH LABS MELBOURNE (AUSTRALIA)  
THE AERODYNAMICS DIVISION AIRBORNE DATA ACQUISITION PACKAGE MK.--ETC(U)  
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MELBOURNE, VICTORIA

AERODYNAMICS NOTE 386

**THE AERODYNAMICS DIVISION**  
**AIRBORNE DATA ACQUISITION PACKAGE MK. I**

by  
A. J. FARRELL

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AIRBORNE DATA ACQUISITION PACKAGE MK.I

by  
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SUMMARY

A system is described which records 32 channels of analogue data in flight in digital form. Sampling rates of 15, 30 and 60 Hertz per channel are available, with an overall capacity of 1200 samples per second. The digital word size is 12 bits. Details of the circuits, including the in-flight quick-look facility are provided.

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## 1. INTRODUCTION

As part of the development of a control and stability mathematical model of the SEAKING Mk. 50 helicopter, a requirement existed for a data acquisition package for ground and flight trials to validate the model. The essential features required in the package were that it should record 32 channels of analogue signals at rates up to 60 Hertz per channel, for durations of up to 15 minutes. This memorandum describes the package designed to fulfil these requirements.

A magnetic tape recorder was chosen as the basic recording device. Because of reported difficulties with magnetic tape recorders in helicopters due to the severe vibration environment<sup>1</sup> a recorder with a proven capability in helicopters<sup>2</sup> was selected, the KUDELSKI NAGRA IV-SJ, which has two data tracks and one voice commentary track. To maximize the capacity of the recorder, data are recorded on each of the two data tracks using a self-clocking code.

Analogue multiplexing and analogue-to-digital conversion are accomplished using a commercially available module, and the control electronics were designed around this module.

A quick-look facility is provided which enables an operator to examine in analogue form what has been recorded for any input channel immediately after recording.

The package fulfils a requirement for an intermediate capacity system falling between the low-cost low data rate cassette-based systems (of the order of 200 bits/sec.) and the high-cost, high data rate equipment (of the order of 30,000 bits/sec.).

The following sections describe the operation and construction of the system.

## 2. GENERAL DESCRIPTION

The basic requirements of the system are listed in Table 1. The number of channels sampled at a given sampling rate may be altered within the bounds set by the total sampling capacity.

Figure 1 is a simplified block diagram of the recording electronics. The analogue signals are sampled by the multiplexer, digitised, converted to serial form, encoded and written into the tape. The operation of all parts of the system are synchronized by a master oscillator in the control and timing unit. The timing is arranged so that all the odd numbered analogue channels are recorded on track 1 (TR1), and all the even numbered channels are recorded on track 2 (TR2).

The recorded serial digital words, of 12-bits each, are grouped into frames of 12 words (Fig. 2) on each track, and the frames are grouped into blocks of 1024 frames each. The words and the frames are separated from each other by gaps. The first two words of each frame (FC and BC) are timing words.

Figure 3 is a simplified block diagram of the in-flight quick-look (QL) facility. The serial data from the selected track are decoded and converted to parallel form. The channel selected by the select switch is extracted from the data stream by the channel select latch, converted to analogue form and displayed on the oscilloscope. The QL facility may be used during recording or playback.

A ground-based QL facility which produces a post-flight hard copy output of any 6 recorded channels is described in another memorandum.<sup>3</sup> The arrangement is similar to the recording package QL, but both tracks are decoded simultaneously and there are six channel selection circuits.

In addition, a transcription unit to convert the recorded serial data into a form suitable for processing on a digital computer has been developed, and this is described in Reference 4.

A variety of signal conditioning circuits are employed because of the wide variety of transducer types providing inputs.

The following sections deal in detail with the component parts of the system.

### 3. RECORDING ELECTRONICS

#### 3.1 Control Section

Four printed circuit boards are involved in producing the control pulses and addresses. The interconnections and outputs of these boards are shown in the block diagram in Figure 4. The heart of the control section is the Timing and Control Unit, PART A and PART B boards (57/245 and 57/248). The timing of the entire recording system is synchronized by a 50 kHz ( $C_k$ ) master oscillator on the PART A board. All the control pulses and addresses are derived from this oscillator using combinational logic, as shown in Figure 5 (a), (b) and (c).

#### 3.2 Analogue Multiplexing and Analogue-to-Digital Conversion

The analogue multiplexer and analogue-to-digital conversion section (MUX/ADC) is a Data Translation DT1640 module with a DT16EX expander module, providing 32 single-ended analogue inputs, each with an input impedance of 100 k $\Omega$ , and 12-bit analogue-to-digital conversion. The maximum throughput rate is 25 kHz, and the module accuracy is  $\pm 0.03\%$  of full scale.

Later models of the flight data recorder will have the multiplex channel address supplied by a programmable read-only memory, but in the version being described, the channels are selected strictly in sequence. The MUX/ADC scans 20 inputs at a rate of 60 Hz each (Fig. 6). Three of the channels are sub-multiplexed by 2:1, to give six input channels at 30 Hz each, and three of the MUX/ADC channels are sub-multiplexed by 4:1 to give twelve channels at 15 Hz.

The control signals for the MUX/ADC and the sub-multiplexers come from the control section (Section 3.1).

#### 3.3 Digital Multiplexer and Timing

At the output of the digital multiplexer (DMUX), the data stream is grouped in the following sequence: firstly, two timing words, the frame count (FC) and the block count (BC), followed by a complete scan of the 20 analogue multiplexer inputs, each input being converted to a 12-bit digital data word. The DMUX, under the control of the control section (Section 3.1), switches the input data words so that the required format is achieved. The interconnections involving the DMUX are outlined in Figure 7.

The FC/BC counter, which is a 24-bit binary counter, is incremented by 1 count for each frame.

#### 3.4 Track Selection and Data Serializing

This part of the recording section (Fig. 8) selects and stores a word from the DMUX output data stream, performs a parallel-to-serial conversion and outputs a 12-bit serial data word, with appropriate interword and interframe gaps. These functions are duplicated for each track.

The DMUX address and track select signals are sequenced [Fig. 5 (a) and (b)] so that each track records the FC and the BC counts as the first two words of each frame. The following 20 words from the DMUX are alternately selected by the 12-bit latches such that all the odd numbered analogue MUX inputs appear on track 1 (TR1), while the even numbered inputs appear on track 2 (TR2), giving the recording format of Figure 2.

The timing of the 12-bit serial-to-parallel converter (SPC) is shown in Figure 9. The conversion operation is synchronized by the  $C_k/4$  clock derived from the master oscillator. Four-bit wide inter-word gaps (IWG) are inserted between the serial words by the SPC, while 12-bit (1 word) wide interframe gaps (IFG) are inserted between the frames by the SPC in conjunction with the IFG and reset circuit. Only one of the SPC boards (the TR2 side) is required to generate the mode control and shift register clock pulses for both tracks.

#### 3.5 Encoding

##### 3.5.1 BPAM Encoding

The binary pulse amplitude modulation (BPAM) code<sup>5</sup> is a single frequency self-clocking digital code in which a low pulse amplitude indicates a logic "0" while a high pulse amplitude indicates a logic "1". The principle disadvantage of this method of encoding is that it is a

non-saturating method and amplitude variations can cause detection ambiguities between a logic "0" and "1". The advantages are its simplicity and the fact that the recorder electronics do not require modification.

Figure 10 is a timing diagram for the BPAM encoders, which are on printed circuit board 57/236(R1).

### 3.5.2 Harvard Encoding

The Harvard or bi-phase mark code<sup>9</sup> is a self-clocking, saturating, frequency doubling code in which a logic transition occurs at the end of each bit period, with an additional transition in the middle of the bit period if the bit to be encoded is a logic "1". The method tends to be independent of recording amplitude changes, but requires more complex electronics than the BPAM method, and also requires the bypassing of the internal recorder electronics.

Figure 11 is a timing diagram of the bi-phase mark encoder which is on printed circuit board 57/264. The board is pin compatible with the BPAM encoder and the change-over requires no wiring modifications to the recording package.

### 3.6 Single Step Circuit

As part of the check and calibration procedure, the single step facility allows the recording electronics to be disabled, and each analogue input to be selected and examined at the analogue multiplexer output by operating the front panel switches. The circuit, which is on printed circuit board 57/249, also incorporates the driving circuit for the analogue multiplexer address indicator lights.

The sequence of operations to examine each analogue input in turn is described in Section 9.

## 4. SIGNAL CONDITIONING

### 4.1 Filters and Conditioning Amplifiers

The filters are DATEL FLT-LP6B50 six-pole Butterworth active filters, with one filter per printed circuit board (board number 57/265). The cut-off frequency ( $f_c$ ) of each filter is determined by a network of six identical resistors, the values of which are determined from the relation:

$$R = 100/f_c - 2$$

where  $R$  is in kilohms and  $f_c$  is in Hertz.

Plots of the amplitude/frequency response for the three cut-off frequencies of 3, 6 and 12 Hertz appear in Figure 12 (a), (b) and (c).

The differential conditioning amplifiers are based on the National Semiconductor LM725 integrated circuit operational amplifier, with four amplifiers per printed circuit card (number 57/259). The circuit arrangement follows the integrated circuit manufacturers recommendations.

The conditioning amplifier input and feedback resistors are selected to satisfy two criteria. Firstly, the gain is set to keep the amplifier output voltage swing within the range +5 to -5 volts, and secondly, where the aircraft instrument outputs are being conditioned, the input resistors are chosen so that the loading on the instrument is less than 1%, and preferably 0.1%, with a minimum value of 200 kilohms. Where aircraft instruments are not involved, the minimum resistor value is 10 kilohms. The loading effects will not affect the accuracy of the measurement since these errors will be calibrated out in the pre-flight checks.

### 4.2 Synchronous Demodulators

This circuit demodulates two types of input; amplitude modulated 400 Hz signals, e.g. the SEAKING rate gyroscope output, and phase-reversing amplitude modulated 400 Hz signals, e.g. LINVAR outputs.

Two versions of the synchronous demodulator are available. The Mk. II version [Fig. 13(a)] for large phase shifts, uses a 180° range active phase shifter. The Mk. III version with a simpler passive phase-shift network for situations requiring a smaller range of shift is the preferred card [Fig. 13(b)]. Figure 14 is a timing diagram common to the two versions. Reference 6 discusses the operation of the synchronous demodulator in more detail.

A total of eleven synchronous demodulators are used in the package.

### 4.3 Tachometer Demodulator

The SEAKING rotor tachometer produces a 21-volt peak-to-peak a.c. output with a frequency proportional to the rotor revolutions-per-minute (RPM). The tachometer demodulator converts the output frequency to a voltage, in the range  $\pm 5$  volts, proportional to the rotor RPM.

Consider the block diagram in Figure 15. The rotor tachometer output frequency ( $f_T$ ), after attenuation by the input amplifier, passes to the input of a phase locked loop (PLL). The PLL is arranged as a frequency modulation (FM) detector with the PLL local oscillator frequency ( $f_o$ ) set to the centre of the input frequency range. The PLL output is of the form  $f_T \pm f_o$ . A four-pole active filter removes the higher of the two frequencies, and the demodulated  $f_T - f_o$  component is conditioned by the output amplifier into the  $\pm 5$  volt range.

The nominal frequency range is 56 to 86 Hertz, which represents 83 to 127% of the normal rotor speed ( $N_r$ ) (Fig. 16).

### 4.4 Temperature Bridge

The temperature measuring bridge is an adaptation of an ARL strain gauge bridge circuit,<sup>7</sup> which has a triple operational amplifier configuration (Fig. 17). The temperature sensing element is a Matthey "Thermafilm" temperature detector, while the voltage regulator, which has a long-term stability of  $\leq 1\%$ , is a National Semiconductor LM317 integrated circuit. The gain of the bridge amplifier is set to give a +5 volt to -5 volt output swing for a  $-10^\circ\text{C}$  to  $40^\circ\text{C}$  temperature change.

### 4.5 Synchro-to-Analogue Converters

Two channels of three-wire synchro output are recorded. To convert each of these synchro signals to analogue form suitable for the MUX/ADC unit (Section 3.2), two modules are used. The first is the NATEL SD532A synchro-to-digital converter (SDC) which produces a 14-bit binary output and is mounted on printed circuit card 57/285. The second module is a 10-bit digital-to-analogue converter (DAC), an Analogue Devices DAC-107-1, on printed circuit card 57/253. The reduction in accuracy due to the conversion of only 10 of the 14 available bits, is from a possible  $\pm 4$  minutes of arc down to approximately  $\pm 21$  minutes of arc.

## 5. QUICK LOOK ELECTRONICS

### 5.1 General Description

From Figure 18 one of the two replay outputs from the recorder is selected. The decoder extracts from the replayed recorder data three signals—the data clock, the serial data and an inter-word gap (IWG) pulse. These signals combine in the serial-to-parallel converter to arrange the serial data into a succession of 12-bit parallel data words.

To select a channel from these data words a number is dialled on the "QL channel select" thumb wheel switch. Using the thumb wheel switch input, the data clock and the IWG pulses, the quick look (QL) channel select circuit generates a correctly timed pulse to the QL latch which picks out the required data word from each 12-word frame. The digital words stored in the QL latch are converted to analogue form and displayed on a monitoring oscilloscope.

For the sub-multiplexed channels the channel position (0 or 1 for 2:1 sub-multiplexed and 0, 1, 2 or 3 or 4:1 sub-multiplexed) is set on the "SUB-MUX select" switch. The SUB-MUX channel select circuit, using the switch input and the inter-frame gap (IFG) pulse from the QL channel select circuit, inhibits the QL latch control pulse so that it selects the required sub-multiplexed channel.

The following sections discuss in more detail the operation of the individual parts of the QL system.

### 5.2 Decoding

#### 5.2.1 bPAM Decoding

The function of the decoder is to extract from the recorder replay signal the signal data and clock, and an inter-word gap (IWG) pulse for each word.

From Figures 19 and 20, the recorder replay signal selected by the switch appears, after amplification, at the input of comparator 1. Outputs corresponding to the logic 1's in the data stream constitute the serial data input to the next stage of decoding. Comparator 2 triggers on every cycle of the inverted replay signal to produce the "raw clock". The raw clock triggers a delay monostable to provide the shift register clock (see Section 5.3). The negative-going edge of the shift register clock is timed to coincide with the position of the serial data logic 1's.

The IWG pulse is generated from the raw clock pulses. The "on" time of the monostable 1 is greater than the period between the new clock pulses, so the output remains at a logic "1" throughout a word. When a gap occurs, the output falls, triggering monostable 2, thus producing the IWG pulse.

The BPAM decoder is mounted on two printed circuit boards 57/273 and 57/274.

### 5.2.2 Harvard Decoder

The function of the Harvard (bi-phase) decoder is the same as the BPAM decoder, namely, to extract from the replayed signal the serial data, serial data clock and IWG pulses.

Considering Figures 21 and 22, the replayed signal from the recorder is amplified and fed to the inputs of two comparators, one of which detects positive signals and the other negative signals (with respect to ground). The combined outputs of these comparators constitutes the serial data.

The serial data clock and the IWG pulse are derived from the inverted serial data. The negative transition of the inverted serial data at the start of each bit period sets the "Q" of the clock timing flip-flop, which is connected as a latch, to a logic "1". This allows pulses from an oscillator to clock a counter. After eight pulses, the counter "D" line changes state, resetting the flip-flop "Q" to a logic "0" and stopping further counting. This sequence constitutes one serial data clock cycle. The oscillator frequency is arranged so that the time for eight pulses is 75% of the bit period.

The serial clock at this stage has 13 pulses per frame instead of 12. The clock pulse limiting circuit is employed to eliminate the unwanted last pulse. The " $\bar{Q}$ " of a latch-connected flip-flop within the clock limiting circuit is set by the IWG pulse to a logic "1". A counter in the limiter counts 12 incoming serial clock pulses, then resets the flip-flop " $\bar{Q}$ " to a logic "0", cutting off the last pulse.

The IWG pulse is derived in the same way as in the BPAM decoder.

The Harvard decoder is mounted on two printed circuit boards, 57/271 and 57/272, which are direct replacements for the BPAM decoder boards.

### 5.3 Serial to Parallel Converter

From Figure 23, the serial data from the decoder is clocked by the negative-going edges of the serial data clock into a 12-bit shift register. When the register is full, the IWG pulse transfers the 12-bit parallel word from the shift register to the output latch. The circuit is mounted on printed circuit board 57/235.

### 5.4 Quick Look Channel Selection

The function of the in-flight quick look (QL) facility is to extract the successive samples of a single channel from the recorded data stream and display it in analogue form on a monitoring oscilloscope. The operation of the QL system, which can be used during recording or on replay, is described in two parts, the first part being the basic QL facility, the second part being the sub-multiplexer section.

In the QL channel select circuit, Figure 24 (a), a number which is associated with a particular channel (Section 9) is dialled on the front panel channel select switch. A digital comparator compares the number with a count of the IWG pulses. When the number and the count are the same, the comparator output goes to a logic "1" [Fig. 24 (b)] and assuming that the SUB-MUX on/off switch is off, the next IWG pulse passes through the AND gate to store the serial to parallel converter output word in the QL latch. This word is converted to analogue form and displayed on an oscilloscope (Fig. 18).

The QL latch is the same as the 12-bit latch described in Section 3.4, while the digital to analogue converter is the same as that described in Section 4.5.

Dealing now with the sub-multiplexer channel select circuit, it can be seen from Table 2 that the sequence in which particular sub-multiplexed channels are recorded is related to the two least significant bits (LSB's) of the frame count (FC) word, i.e. the first word of each frame (Fig. 2). From Figures 25 and 26, the first IWG pulse selector circuit allows the first IWG pulse only of each frame through as the 2-bit latch control pulse. This pulse stores the two least significant bits of the FC word when a 4:1 sub-multiplexed channel is selected (B1 is set to a logic "0" when a 2:1 sub-multiplexed channel is selected). If the bits stored in the 2-bit latch match the binary code of the number selected on the thumb wheel switch, the comparator gives an output which allows the QL latch control pulse to be transmitted during that frame. As the switch number, N, is changed, the position in time of the comparator output changes appropriately.

## 6. ANCILLARY GROUND EQUIPMENT

Three pieces of equipment have been constructed which are used in conjunction with the flight data recorder. These are a test and calibration unit,<sup>8</sup> which simulates the input from aircraft instruments and other transducers to the 32 channels, and provides a calibration facility; a 6-channel ground-based quick-look unit,<sup>3</sup> which provides a post-flight hard copy readout of any six channels simultaneously; and a transcriber unit,<sup>4</sup> which converts the recorded serial data into standard computer-compatible form.

## 7. POWER SUPPLIES

The direct current power supplies (+5, +15 and -15 volts) to the electronic instrumentation are provided by ten power supply modules powered from the aircraft 115 volts, 400 Hertz single phase and +28 volts d.c. supplies. The aircraft a.c. and d.c. power supplies are connected through two circuit breaker protected input sockets on the main power supply box (see Section 8).

The relevant details of the power supplies are detailed in Table 3.

## 8. MECHANICAL DETAILS

The basic objective from the mechanical design point of view is a strong, accessible unit using existing flight proven designs and practices where possible.

The electronics are mounted on ARL standard M4 printed circuits in 10 ARL standard aluminium boxes manufactured to ARL drawing numbers 9348 to 9350. Up to 12 printed circuit cards can be accommodated in each box. The MUX/ADC modules are mounted in one of the standard boxes with special mounting attachments, and six of the ten power supply modules are mounted in a special lightweight box of the same dimensions as the standard boxes. The total of 12 boxes are mounted in a welded tubular steel frame fitted with integral carrying handles (Fig. 27). The frame has been successfully tested to 25 g loading without permanent distortion.

The tape recorder and control panel/oscilloscope assembly are each mounted on four anti-vibration mounts of a type suitable for helicopters. The main frame itself is intended to be bolted directly to the aircraft floor.

Each box is connected to the main wiring loom via CANNON DC 37P and DC 37S plugs and sockets retained by D 2019 and D 2020 anti-vibration catches. The wiring throughout is with RAYCHEM cross-linked polyalkene insulated size 22 copper wire manufactured to MIL-W-81044 (AS). Each solder joint is insulated and supported by RAYCHEM heat-shrinkable sleeving. Labelling of plugs and sockets is in accordance with the MIL-E-5400 specification.

The total weight of the package is 78 kilograms. If necessary, the total weight can be reduced to approximately 34 kilograms by replacing the filter boxes with a newer, lighter design which is now available, eliminating the quick-look system, and selecting different active filters.

## 9. OPERATION

The following is a suggested series of steps for operating the flight-data recording equipment on an aircraft:

### PRE-FLIGHT CHECKS

- (i) Replace recorder dry cells and check that oscilloscope batteries are charged. Connect aircraft power supplies and signal inputs and switch on. Check that the five MUX ADDRESS lights are on.  
*N.B.:* When switching from auxiliary power units to the internal aircraft supply, disconnect the two power supply and the five signal leads to avoid the possibility of spikes and surges damaging the equipment.
- (ii) Load the recorder with long-play tape (e.g. BASF DP26 double play, 360 m long tape on a 130 mm reel). This gives approximately 15 minutes of run time at 381 mm/second recording speed.
- (iii) Reset the system with the control panel reset switch and set the recorder to "record".
- (iv) Using the quick look system, check each channel in turn, as follows:—
  - (a) Select track 1 on control panel switch.
  - (b) Dial number  $0 \leq N \leq 11$  on the QL channel select switch.
  - (c) For  $N = 0$ , check oscilloscope for slow decrease in voltage from 0 to  $-10$  in 70 seconds, with no dropouts, i.e. breaks in the trace.
  - (d) For  $N = 1$ , oscilloscope should be steady somewhere in the 0 to  $-10$  volt range.
  - (e) For  $2 \leq N \leq 8$ , vary the input (e.g. move the cyclic control column) and check the response on the oscilloscope. Table 4 can be used to identify the input.
  - (f) For  $9 \leq N \leq 10$ , set the sub-multiplexer select switch to "on" and select "2:1" sub-multiplexing. Dial  $0 \leq M \leq 1$  on the SUB-MUX. Channel select switch and check the responses in (e).
  - (g) For  $N = 11$ , select "4:1", and dial  $0 \leq M \leq 3$  on the SUB-MUX. Channel select, checking each channel as before.
  - (h) Select track 2, and repeat (b) to (g) with  $2 \leq N \leq 7$  in (e),  $N = 8$  in (f) and  $10 \leq N \leq 11$  in (g).

A resumé of these steps appears in Figure 28 and Table 5.

### RECORDING

- (i) Install a fresh tape if required.
- (ii) Reset the system and check the recording level of each track on the monitor meter.
- (iii) Start the recording using the remote stop/start switch.
- (iv) Identify the recording with the one microphone.
- (v) Monitor the most important channel(s) on the QL oscilloscope.
- (vi) When the tape is almost finished, rewind and replace with a fresh tape.

### SINGLE STEP PROCEDURE

If during calibration or checking, it becomes desirable to examine each channel separately, the non-sub-multiplexed channels may be examined at the input to the analogue-to-digital converter by taking the oscilloscope input from the monitor point marked "MUX TEST" on the signal input strip and performing the following steps:

- (i) Set reset switch to "reset".
- (ii) Zero MUX channel address by depressing and releasing the MUX stroke switch.
- (iii) Depress MUX clear switch, and step MUX channels by depressing and releasing the MUX strobe switch.

### 10. CONCLUSION

This memorandum describes a 32-channel flight-data recording system based on a KUDELSKI NAGRA IV-SJ tape recorder and a DATAX MUX/ADC module. It features alternative (BPAM or Harvard) code recording formats and a built-in quick look system. It can record, with a commentary, data for up to 15 minutes on a single 130 mm tape reel. Test and ground replay equipment have also been constructed to support the system. The flight system has been ruggedly constructed for the severe vibration environment of the helicopter.

Even though it has been designed for a specific project, the system is versatile enough to be useful in a wide variety of data acquisition tasks.

#### ACKNOWLEDGEMENTS

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## REFERENCES

1. Farrell, P., (Structures Division, ARL), private communication, 1976.
2. Gould, D. G., NAE (Canada) Data Recording System, private communication, Nov. 1975.
3. Creed, S. H., Six-Channel Quick Look System. Aero. Tech. Memo. (proposed) 1978.
4. Farrell, A. J., and Hourigan, D. F., A Data Transcriber for the Aero. Div. Flight Data Acquisition System. Aero. Tech. Memo. 310, 1978.
5. Patterns, Communication and Media—an Introduction to PCM. Bell and Howell Instruments Division, Pasadena, California 91109, USA.
6. Macken, W. J., Synchronous and Non-synchronous Rectification with an Operational Amplifier. Electronic Engineering, March 1973, pp. 17-18.
7. Ludowyk, C., Strain Gauge Instrumentation Amplifier. ARL Drawing Number 51544, 1975.
8. Ferrarotto, P., Test and Calibration Unit. Aero. Tech. Memo. (proposed) 1977.

**TABLE 1**

**Summary of Data Recording Requirements for SEAKING Mk. 50  
Mathematical Model Validation**

Total number of analogue inputs	32
Analogue inputs at 60 Hz sample rate	14
Analogue inputs at 30 Hz sample rate	6
Analogue inputs at 15 Hz sample rate	12
Total sampling capacity/sec	1200
Overall accuracy (%)	0.2
Data word size (bits)	12
Maximum continuous run time (mins)	15
Differential input impedance (in kilohms, as seen by analogue inputs)	≥ 100
Mass of package (kg)	78
Power consumption:	
from 115 V, 400 Hz, single phase (in watts)	200
from 28 V d.c. supply (in watts)	27

**TABLE 2**

**Relationship between the Two Least Significant Bits of the Frame Count and the Recorded  
Sub-multiplexed Channels**

(Two cycles of 4:1 and four cycles of 2:1 sub-multiplexing shown)

Two Least Significant Bits of the Frame Count Word (FC)		Track 1 Channels			Track 2 Channels		
		Frame Position 10 (2:1)	Frame Position 11 (2:1)	Frame Position 12 (4:1)	Frame Position 10 (2:1)	Frame Position 11 (4:1)	Frame Position 12 (4:1)
B1	B0						
0	0	15	19	25	17	21	29
0	1	16	20	26	18	22	30
1	0	15	19	27	17	23	31
1	1	16	20	28	18	24	32
0	0	15	19	25	17	21	29
0	1	16	20	26	18	22	30
1	0	15	19	27	17	23	31
1	1	16	20	28	18	24	32

**TABLE 3**  
**D.C. Power Supplies**

Air-craft Supply	Module Position	Module Type	Output (volts)	Total Available Output Current (mA)	Output Current Allocation (mA)
115 V, 400 Hz Single Phase	Box 10 (A)	KLAASING-REUVERS Type 546	+5	2000	
	Box 10 (B)	KLAASING-REUVERS Type 546	+5	2000	
	Box 10 (C)	KLAASING-REUVERS Type 566	$\pm 15$	$\pm 300$	Box 5 ( $\pm 150$ ) Box 6 ( $\pm 150$ ) } total $\pm 300$
	Box 10 (D)	KLAASING-REUVERS Type 566	$\pm 15$	$\pm 300$	Box 8 ( $\pm 150$ ) Box 9 ( $\pm 110$ ) } total $\pm 260$
+28 V d.c.	Box 10 (E)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 7 ( $\pm 160$ )
	Box 10 (F)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 4 ( $\pm 155$ )
	Box 12 (8)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 1 ( $\pm 4$ ) Box 4 ( $\pm 33$ ) Box 5 ( $\pm 35$ ) Box 12 ( $\pm 86$ ) } total $\pm 158$
	Box 12 (9)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 2 ( $\pm 17$ ) Box 6 ( $\pm 38$ ) Box 7 ( $\pm 33$ ) Box 8 ( $\pm 35$ ) Box 9 ( $\pm 37$ ) } total $\pm 160$
	Box 12 (10)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 11 ( $\pm 53$ )
	Box 12 (11)	SCI Type 50C28-15D165	$\pm 15$	$\pm 165$	Box 3 ( $\pm 80$ ) Transducers ( $\approx \pm 70$ )

**TABLE 4**

**SEAKING Flight Tests—Channel Identification Table**

All signals are conditioned to be within the range  $\pm 5$  V for recording

Channel Number	Quantity to be Measured	Instrument Sensitivity	Sample Rate (Hz)
1	Cyclic stick position—Pitch ( $+18^\circ$ , $-15^\circ$ )	266 mV/deg.	60
2	Cyclic stick position—Roll ( $\pm 15^\circ$ )	322 mV/deg.	60
3	Collective stick position ( $+27^\circ$ to $+49^\circ$ )	99.6 mV/deg.	60
4	Pitch vane (0-360°)	13 mV/0	60
5	Fore/Aft push/pull rod ( $\pm 25$ mm)	198.9 mV/mm	60
6	Lateral push/pull rod ( $\pm 25$ mm)	200 mV/mm	60
7	Collective push/pull rod ( $\pm 32$ mm)	156 mV/mm	60
8	Yaw push-pull rod ( $\pm 25$ mm)	200 mV/mm	60
9	Side slip vane (0-360°)	13 mV/0	60
10	Roll attitude ( $\pm 24^\circ$ )	66.87 mV/deg.	60
11	Vertical acceleration ( $\pm 15$ g max.)	325 mV/g	60
12	Longitudinal acceleration ( $\pm 10$ g max.)	500 mV/g	60
13	Lateral acceleration ( $\pm 10$ g max.)	500 mV/g	60
14	Vertical acceleration ( $\pm 10$ g max.)	500 mV/g	60
15	Pitch attitude ( $\pm 15^\circ$ )	99.28 mV/deg.	30
16	Yaw pedal position ( $\pm 28.6$ mm)	200 mV/mm	30
17	Yaw angular acceleration ( $\pm 30^\circ$ /sec.)	162 mV/mm	30
18*	Yaw attitude (0-360°)	27.78 mV/deg.	30
19	Longitudinal cable angle ( $\pm 12^\circ$ )	405 mV/deg.	30
20	Lateral cable angle ( $\pm 12^\circ$ )	369 mV/deg.	30
21	Longitudinal velocity ( $+140$ , $-30$ knots)	35.5 mV/kt	15
22	Lateral velocity ( $\pm 30$ knots)	156 mV/kt	15
23	Airspeed (0-0.2 kPa)	25 mV/kt	15
24	Radar altitude (raw) (0-400 ft)	24.92 mV/ft	15
25	Radar altitude (smooth) (0-400 ft)	24.92 mV/ft	15
26	Pressure altitude (85-110 kPa)	200 mV/kt	15
27	Altitude change ( $\pm 300$ ft)	15.12 mV/ft	15
28	Temperature (0-40°C) (20°C = 0 V)	250 mV/°C	15
29	Torque (3-w synchro, 11, 6 V rms, 400 Hz)	0-100%	15
30	Rotor RPM (21 V ptp, 70 Hz max.)	See Figure 16	15
31	Cable depth pot. { Indirect measurement	—	15
32	Cable height pot. { (computed)		
33	Time (continuous clock)	—	60
34	Event/voice (commentary microphone)	—	—

For Quick Look select procedure for any channel (1 to 33) see Figure 28.

\* A switch-selectable alternative input to channel 18 is engine torque 2, with characteristics similar to channel 29.

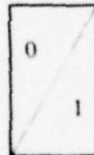
TABLE 5

Data Frame/Quick Look Relationships

Track 1 Channel Allocation	FC	BC	1	3	5	7	9	11	13	15 16	19 20	25 26 28
QL Channel Select Number	0	1	2	3	4	5	6	7	8	9	10	11
Track 2 Channel Allocation	FC	BC	2	4	6	27	10	12	14	17 18	21 22 23 24	29 30 31 32

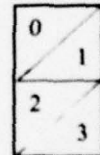
2:1 SUB-MUX

SUB-MUX  
Channel  
select  
number



4:1 SUB-MUX

SUB-MUX  
Channel  
select  
number



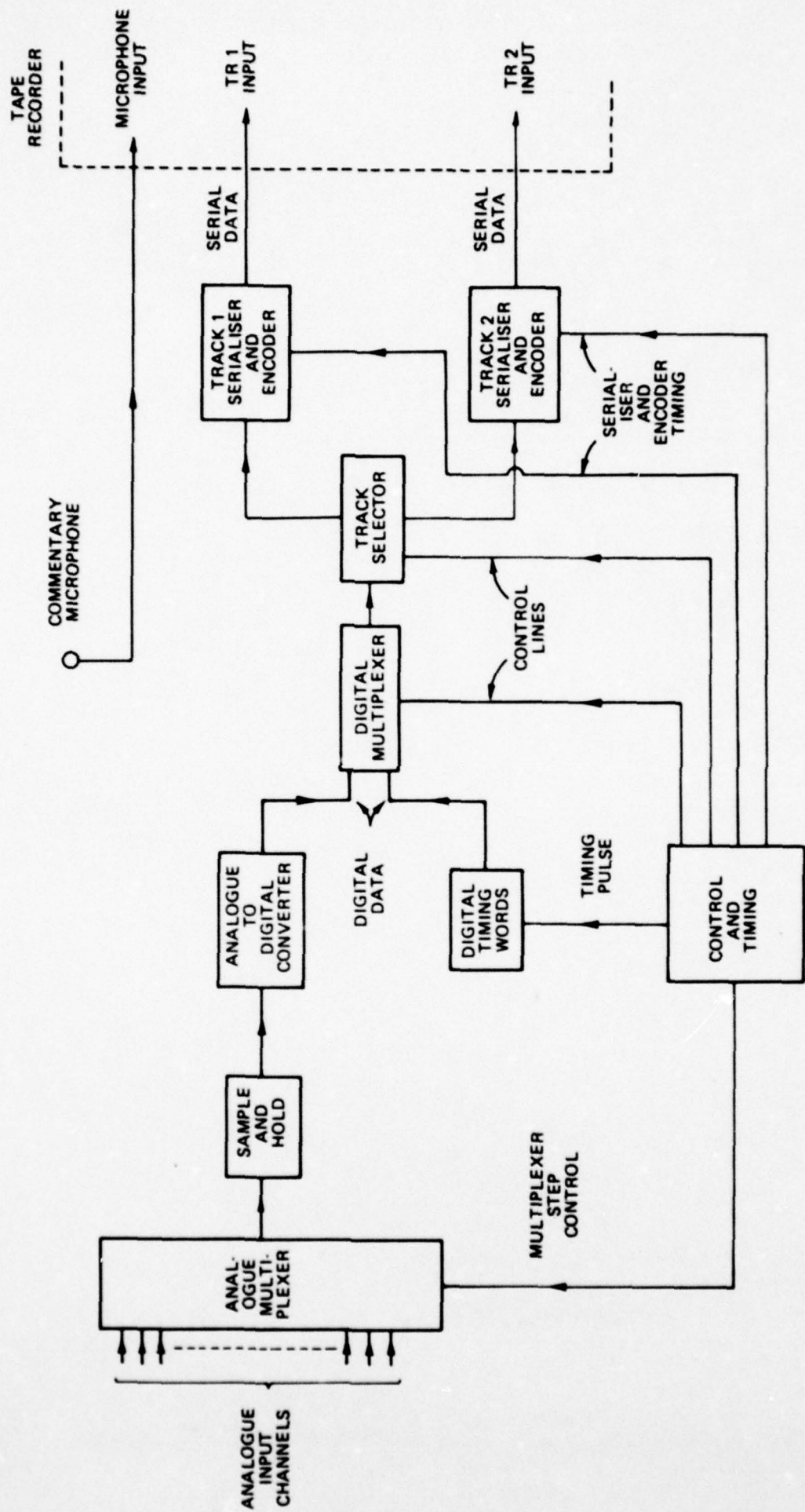


FIG. 1 DATA RECORDING SYSTEM - SIMPLIFIED BLOCK DIAGRAM

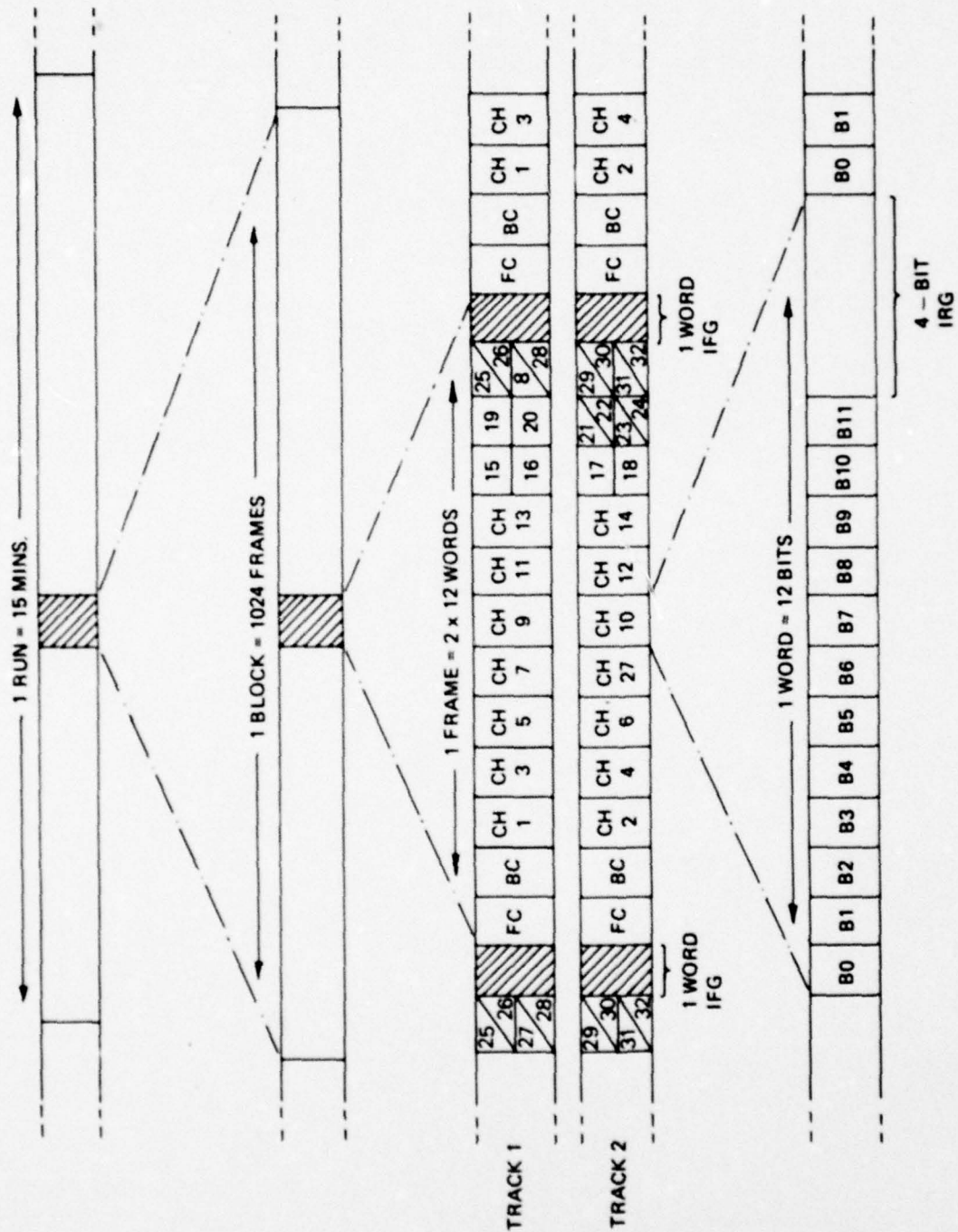


FIG. 2 RECORDING FORMAT

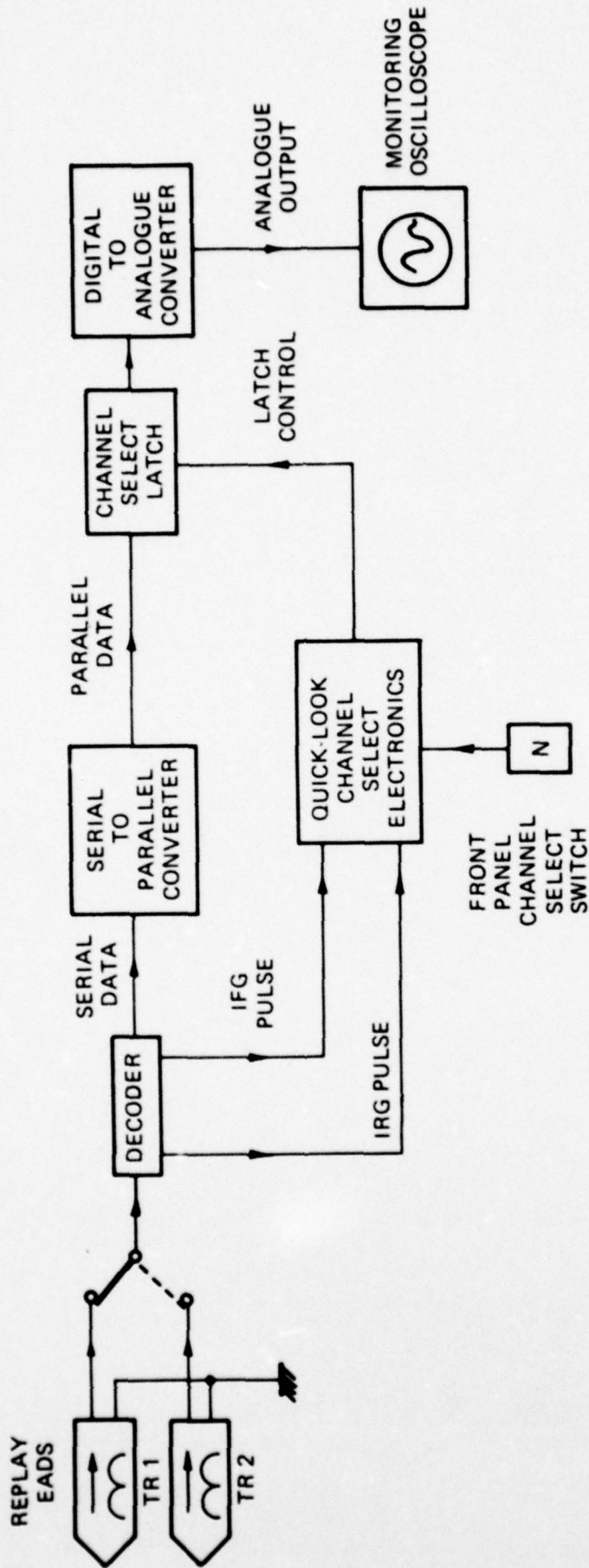


FIG. 3 QUICK-LOOK FACILITY SIMPLIFIED BLOCK DIAGRAM

TO ENCODERS (57/236 )

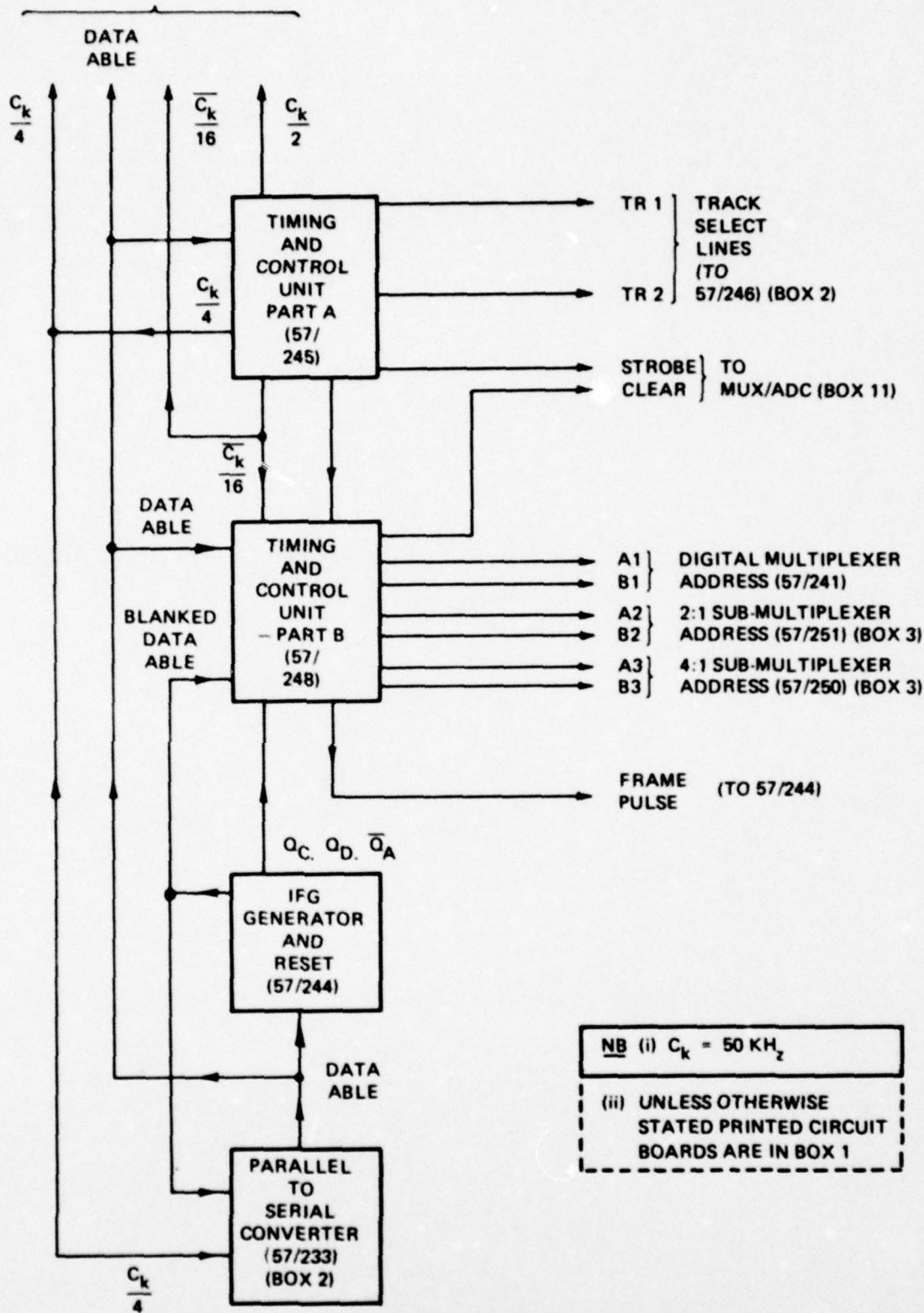


FIG. 4 RECORDING ELECTRONICS CONTROL SECTION - INTERCONNECTIONS AND OUTPUTS.



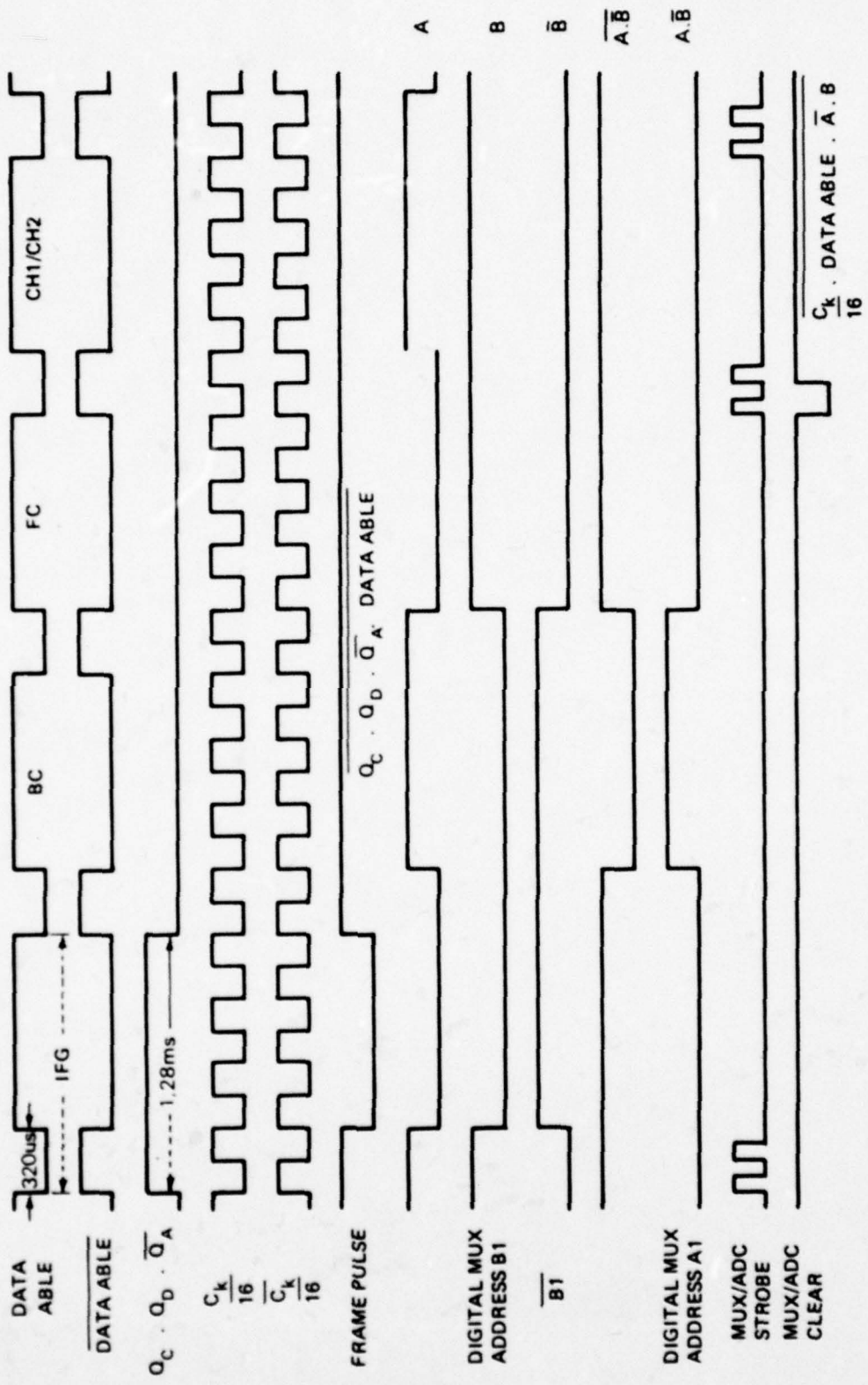


FIG 5. (b) RECORDING ELECTRONICS CONTROL SECTION TIMING DIAGRAM - PART 2

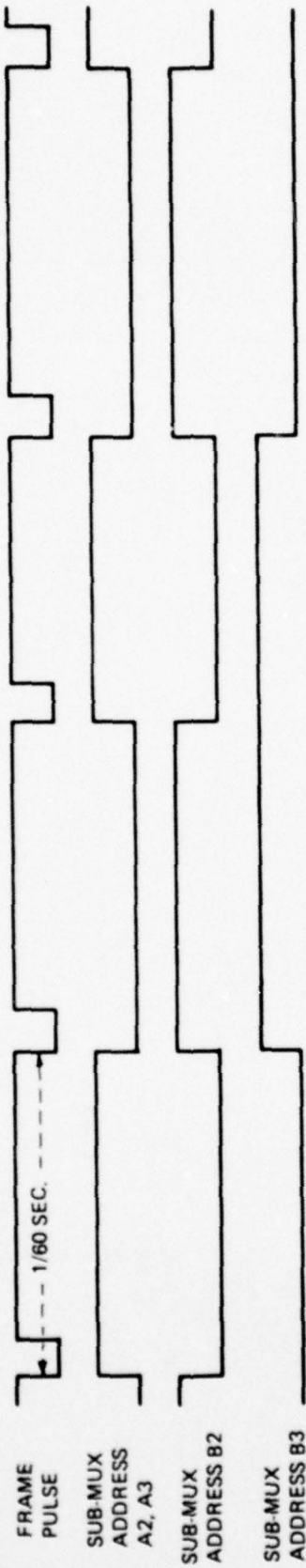


FIG. 5(c). RECORDING ELECTRONICS CONTROL SECTION TIMING DIAGRAM - PART 3

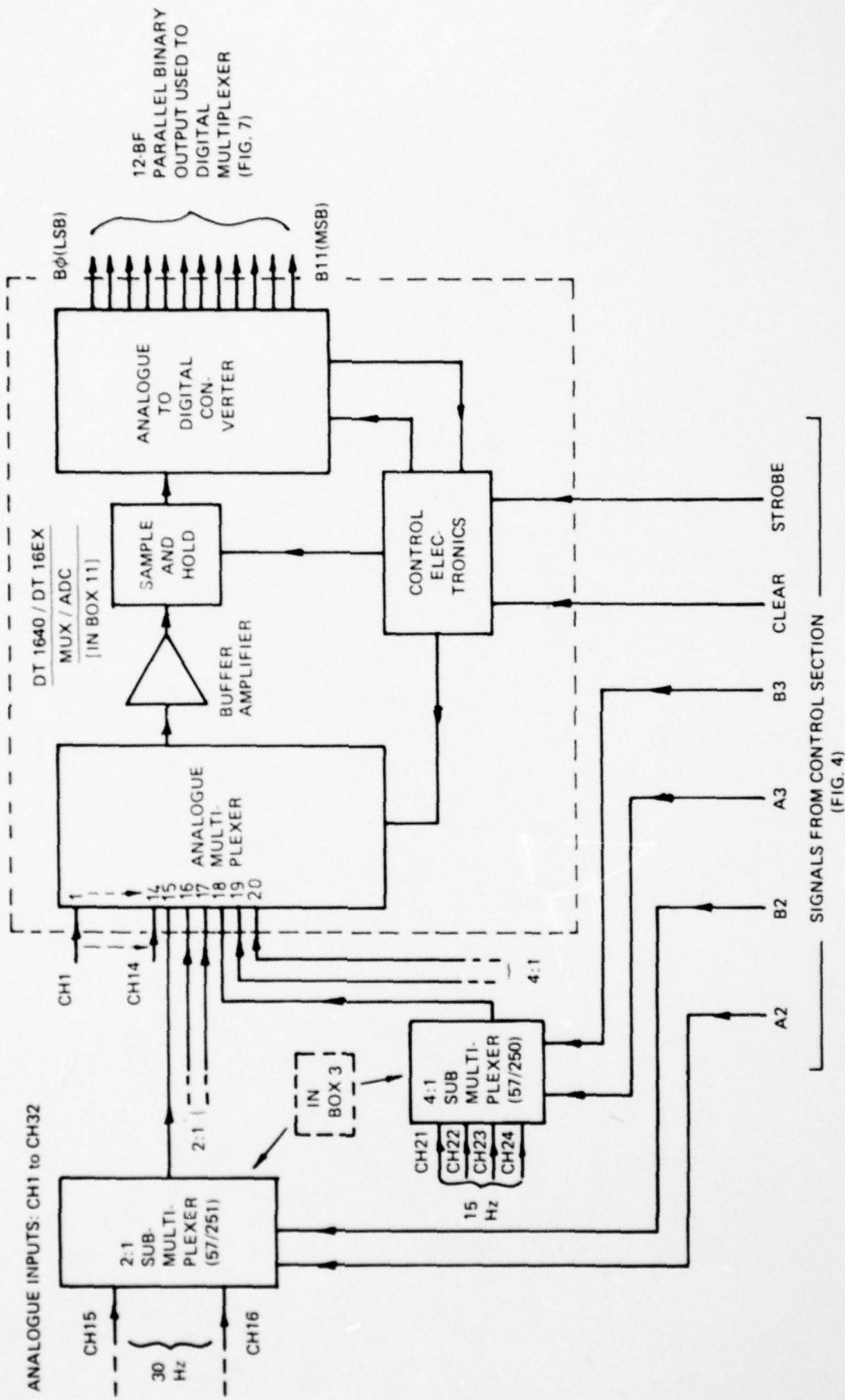
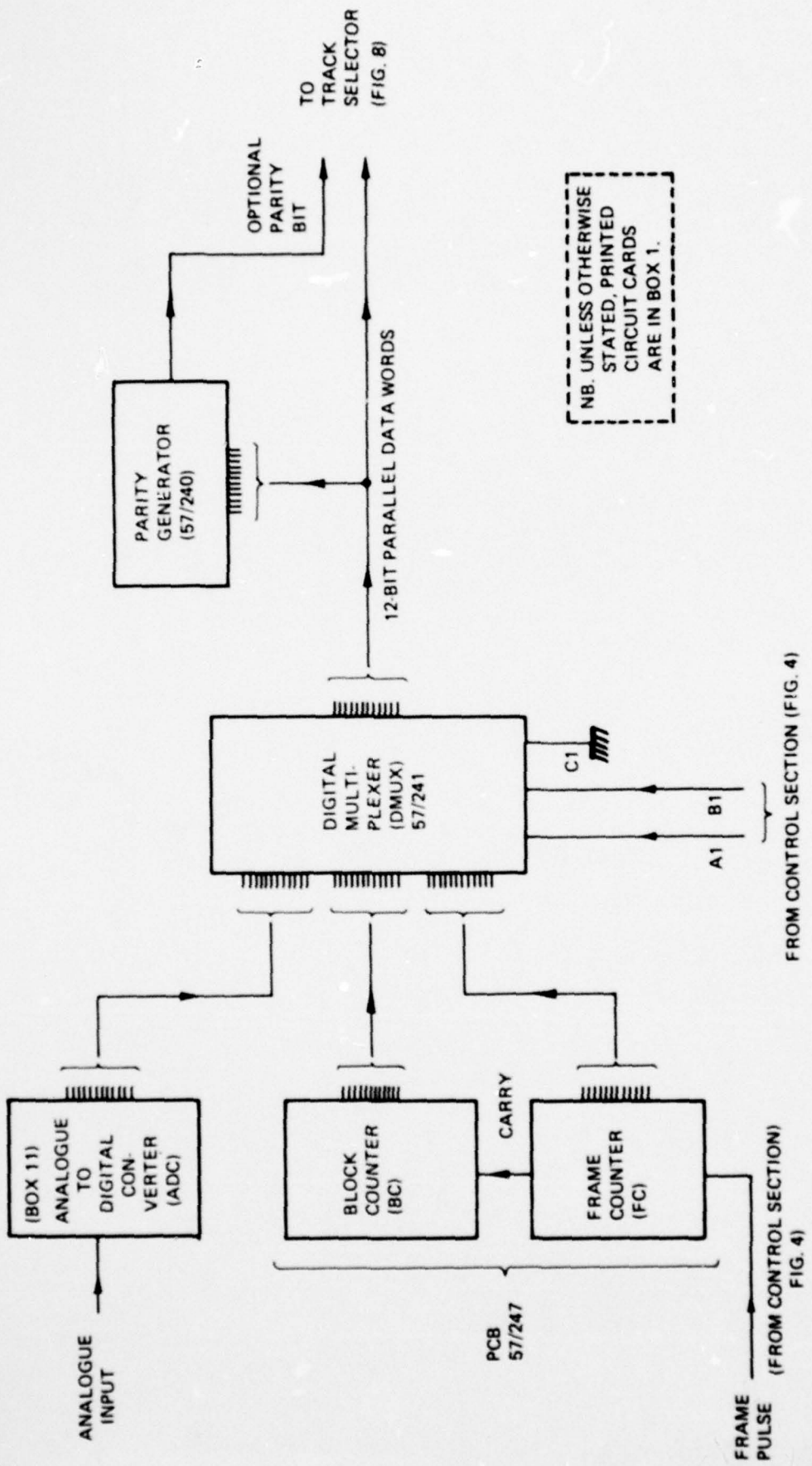


FIG. 6. ANALOGUE MULTIPLEXING, SUB-MULTIPLEXING AND DIGITAL CONVERSION  
- BLOCK DIAGRAM

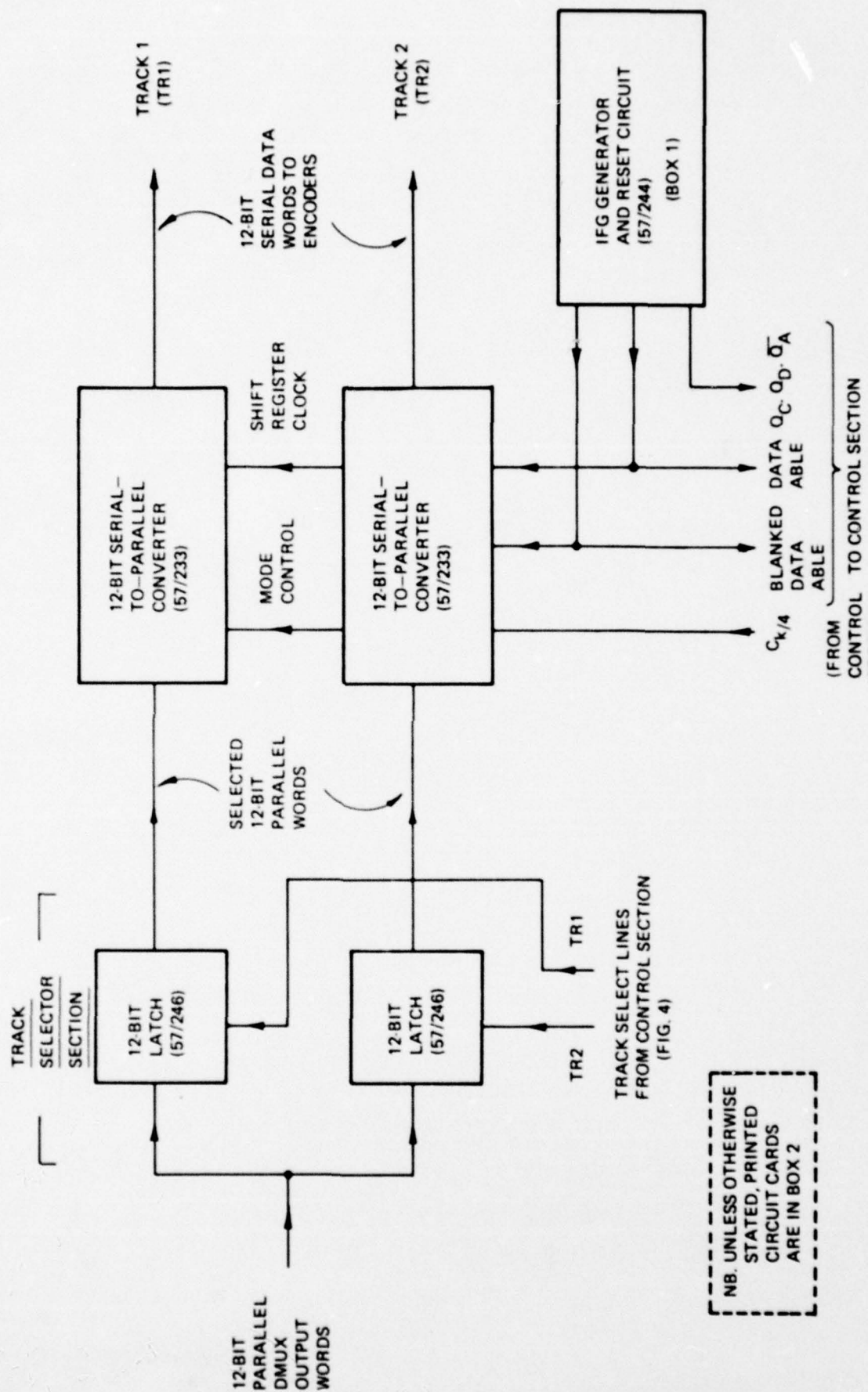


NB. UNLESS OTHERWISE STATED, PRINTED CIRCUIT CARDS ARE IN BOX 1.

FROM CONTROL SECTION (FIG. 4)

FRAME PULSE (FROM CONTROL SECTION) FIG. 4)

FIG. 7. DIGITAL MULTIPLEXER INTERCONNECTIONS - BLOCK DIAGRAM



NB. UNLESS OTHERWISE STATED, PRINTED CIRCUIT CARDS ARE IN BOX 2

FIG. 8. TRACK SELECTION AND SERIAL-TO-PARALLEL CONVERTER SECTION BLOCK DIAGRAM

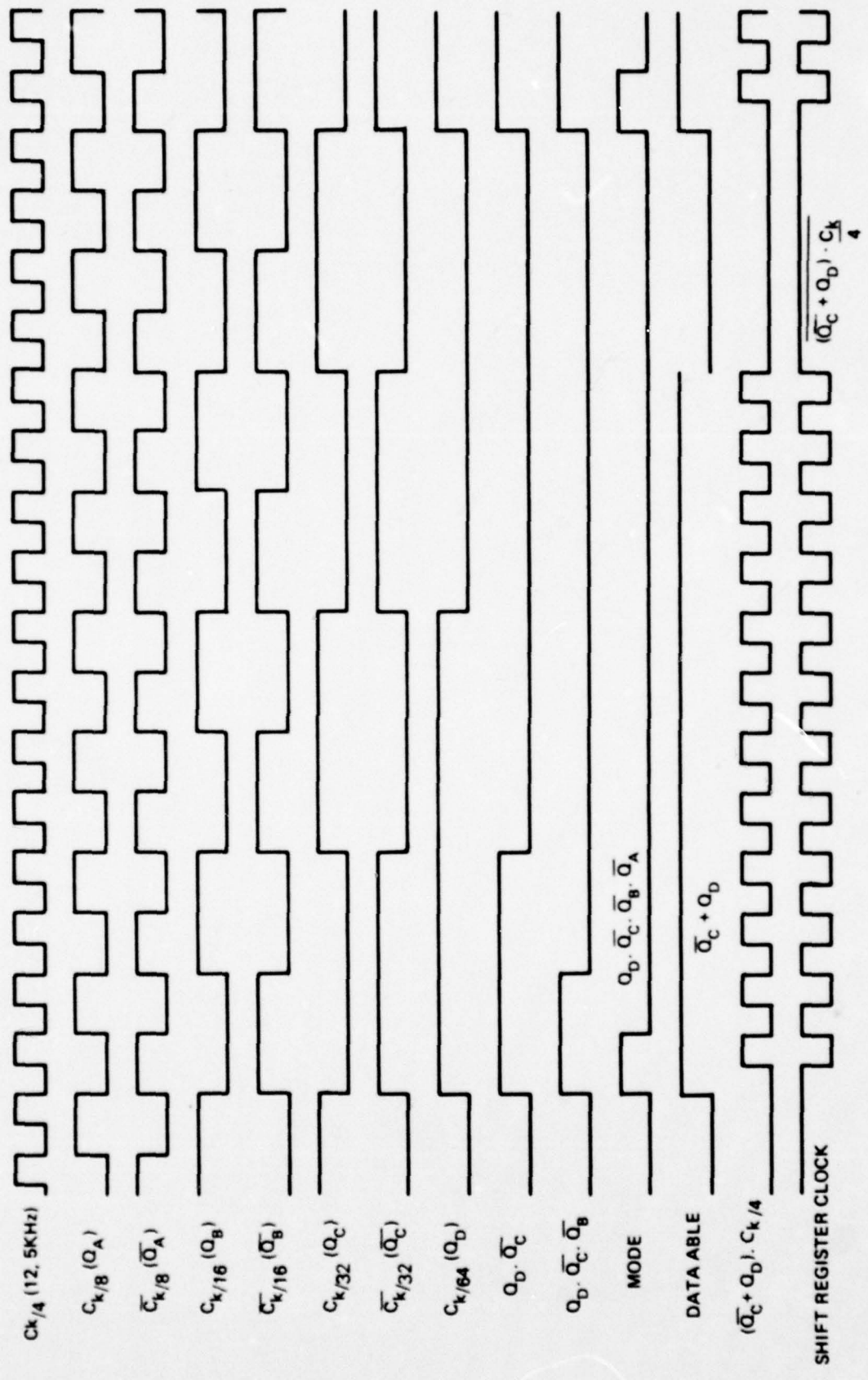


FIG. 9. SERIAL-TO-PARALLEL CONVERTER TIMING DIAGRAM.

$$\frac{(\overline{O_C} + O_D) \cdot Ck}{4}$$

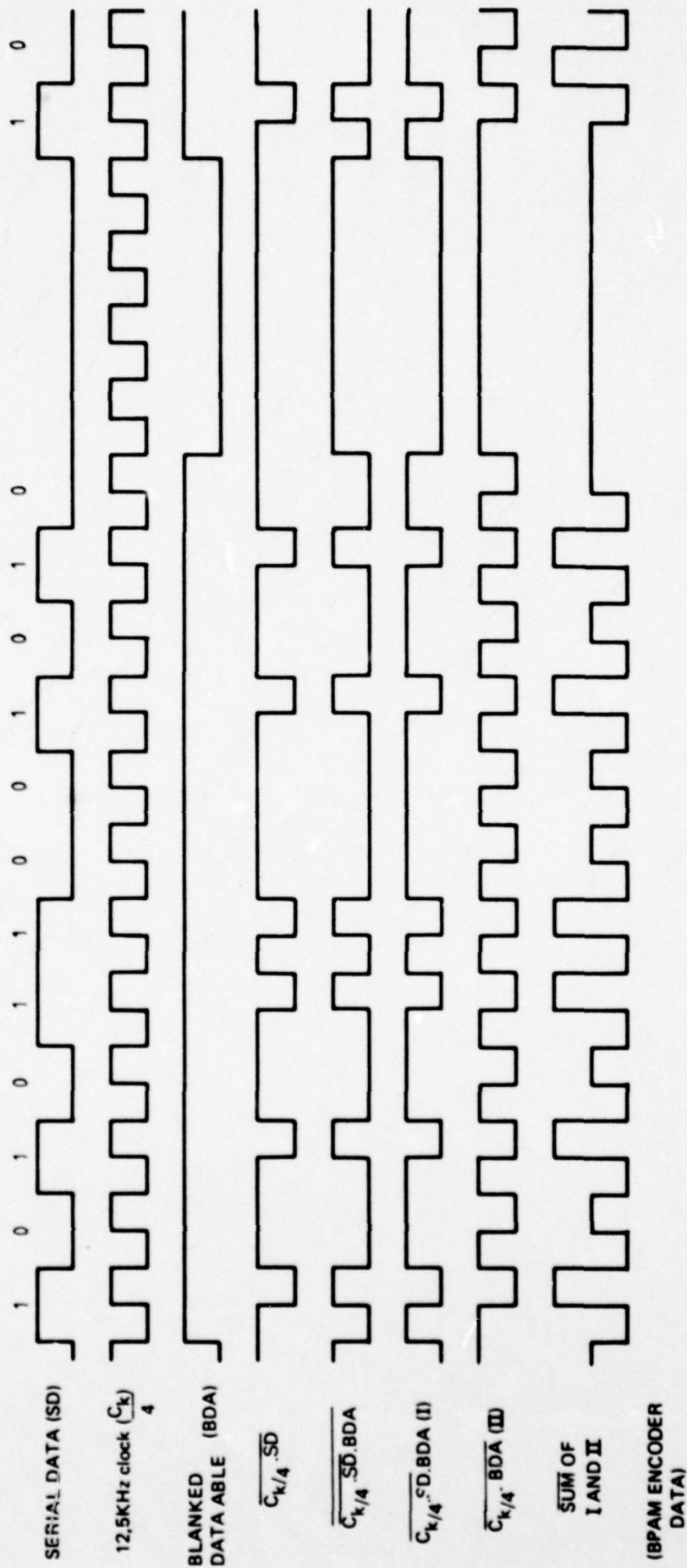


FIG. 10. BINARY PULSE AMPLITUDE MODULATION (BPAM) ENCODER TIMING DIAGRAM

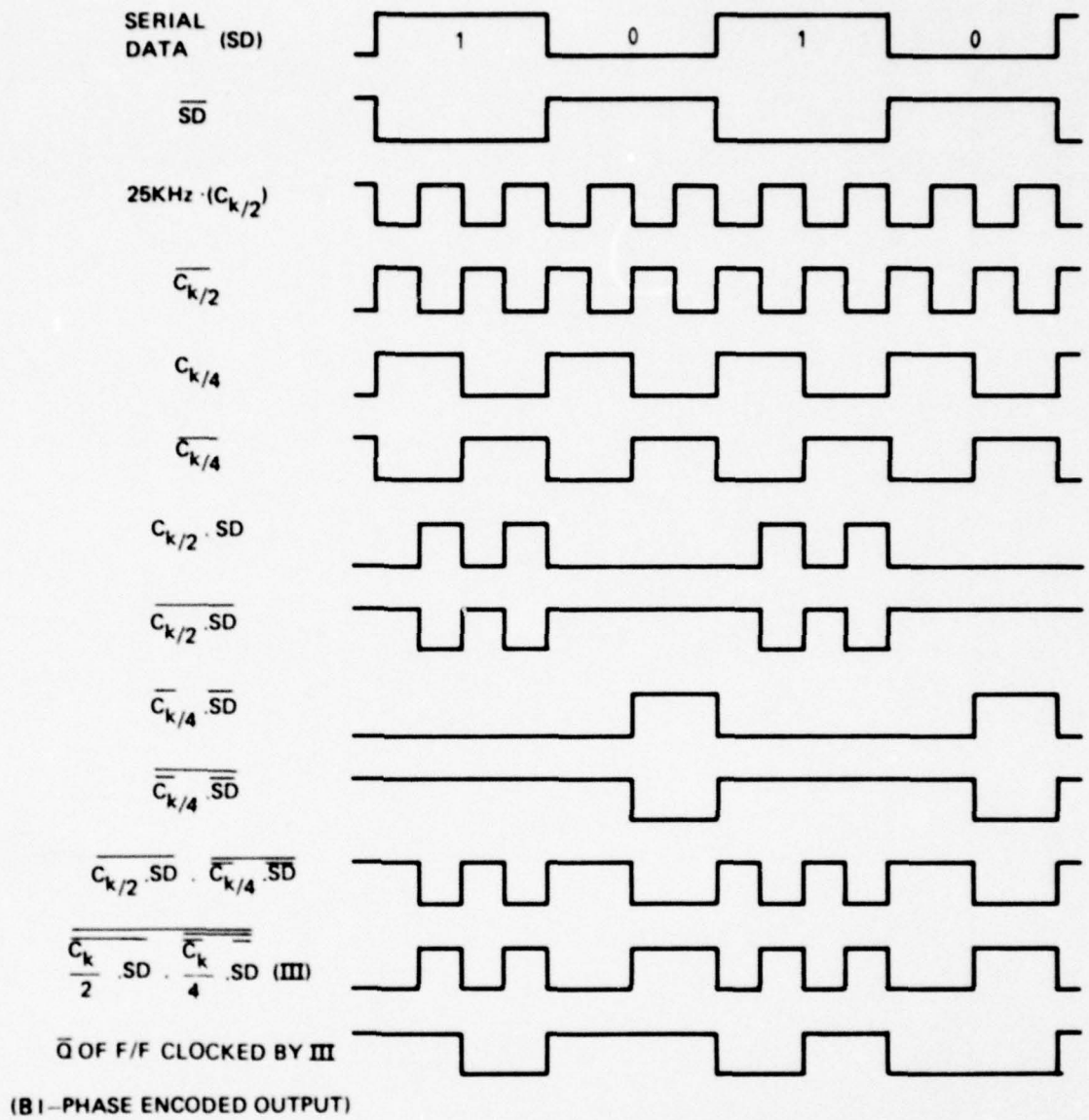


FIG. 11. HARVARD (BI-PHASE MARK) ENCODER TIMING DIAGRAM

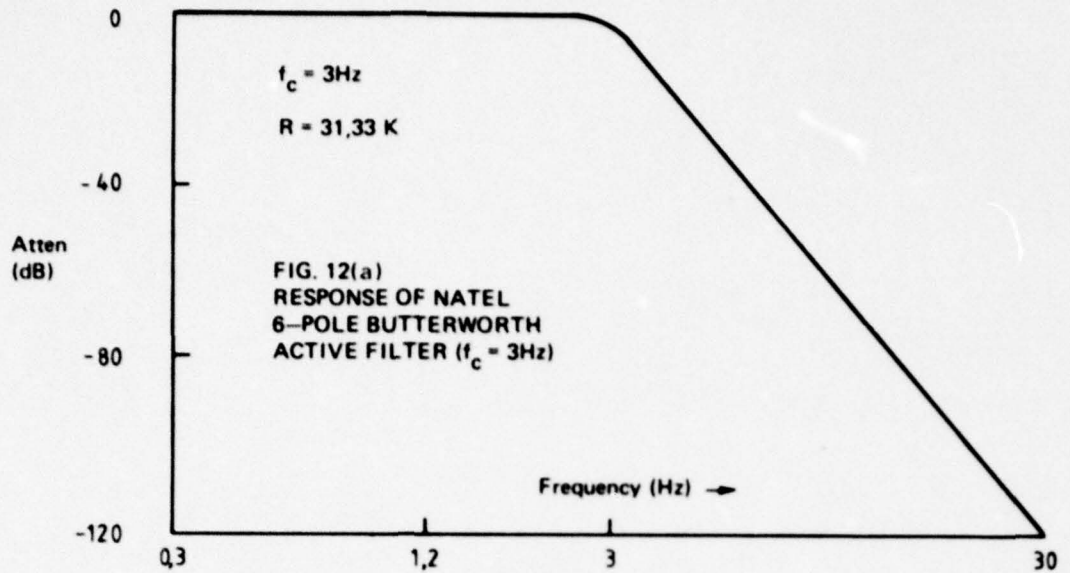


FIG. 12(a)

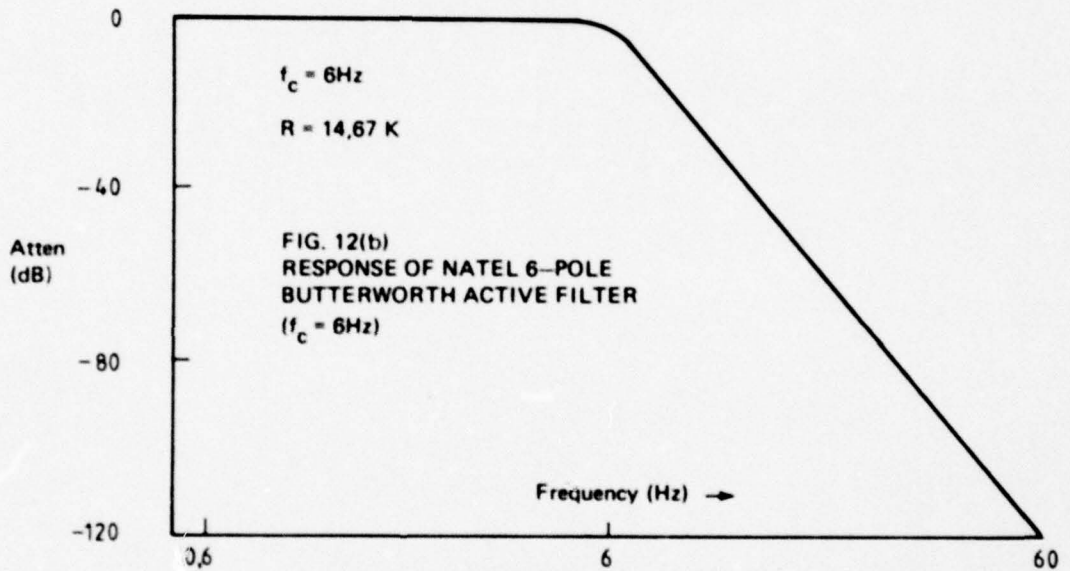


FIG. 12(b)



FIG. 12(c)

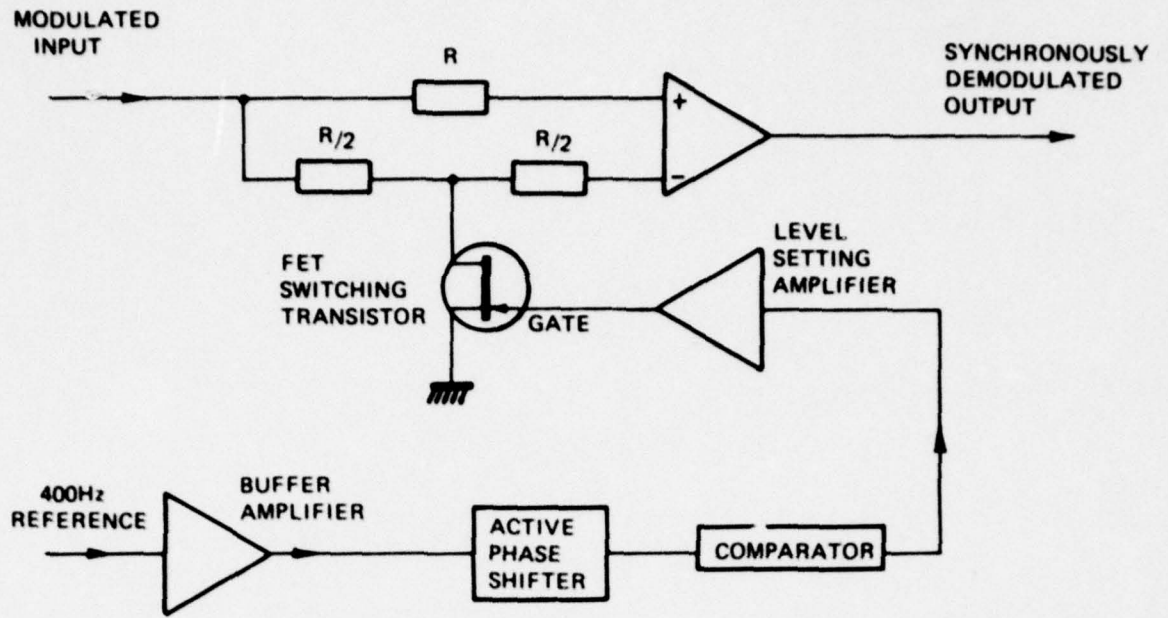


FIG. 13(a). SYNCHRONOUS DEMODULATOR MK II. (PRINTED CIRCUIT BOARD 57/302)  
- 2 DEMODULATORS PER BOARD

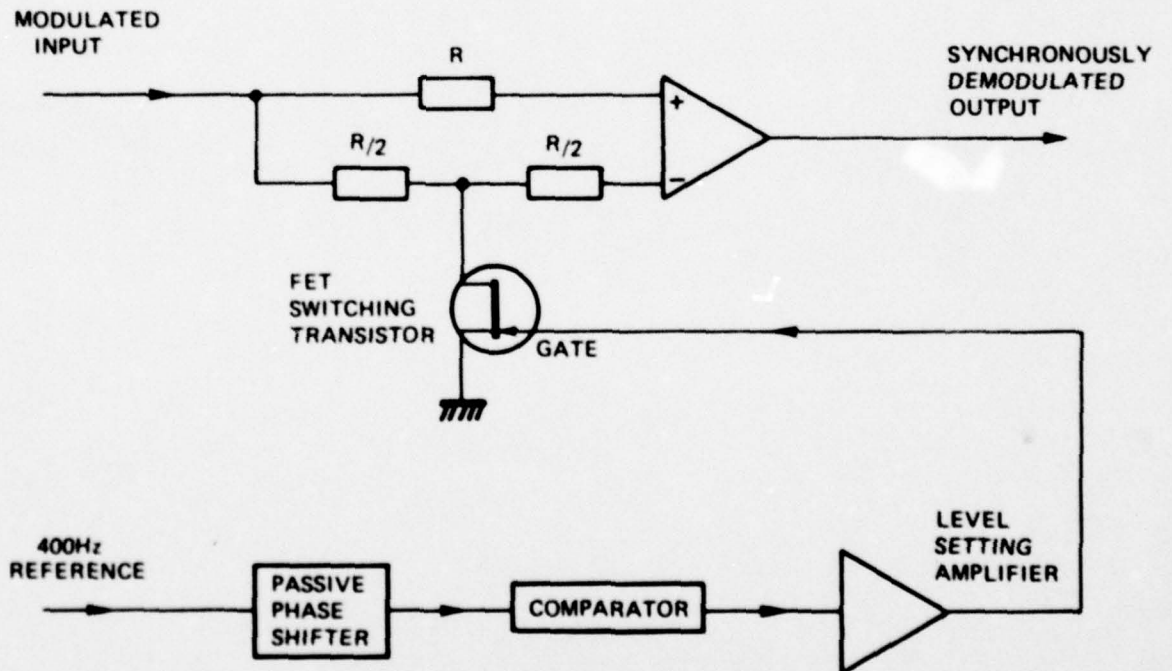


FIG. 13(b). SYNCHRONOUS DEMODULATOR MK III (PRINTED CIRCUIT BOARD 57/306)  
- 2 DEMODULATORS PER BOARD

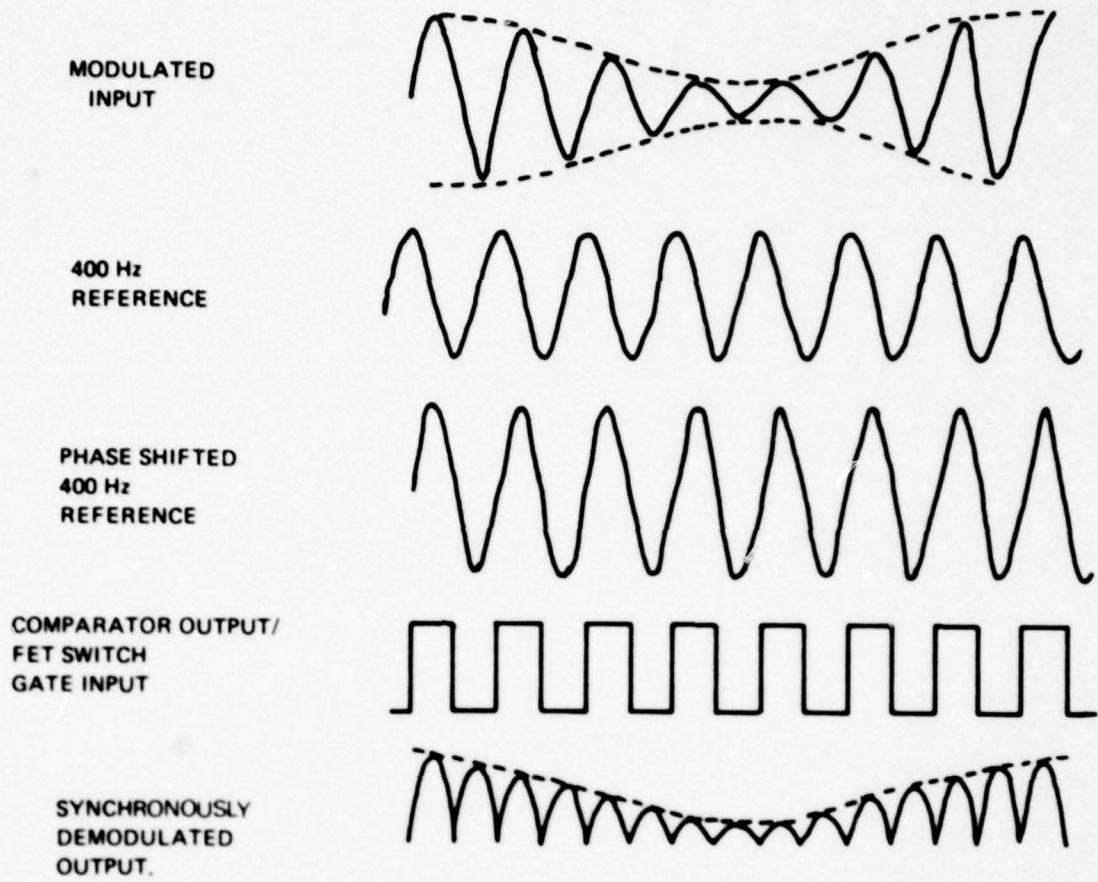
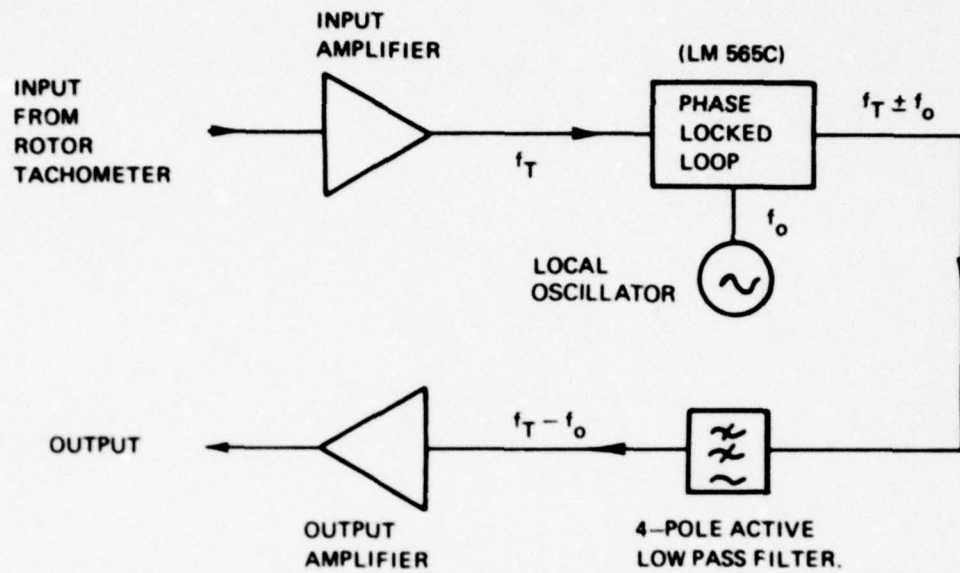


FIG. 14. SYNCHRONOUS DEMODULATOR TIMING DIAGRAM.



PRINTED CIRCUIT BOARD 57/315

FIG. 15. TACHOMETER DEMODULATOR - BLOCK DIAGRAM

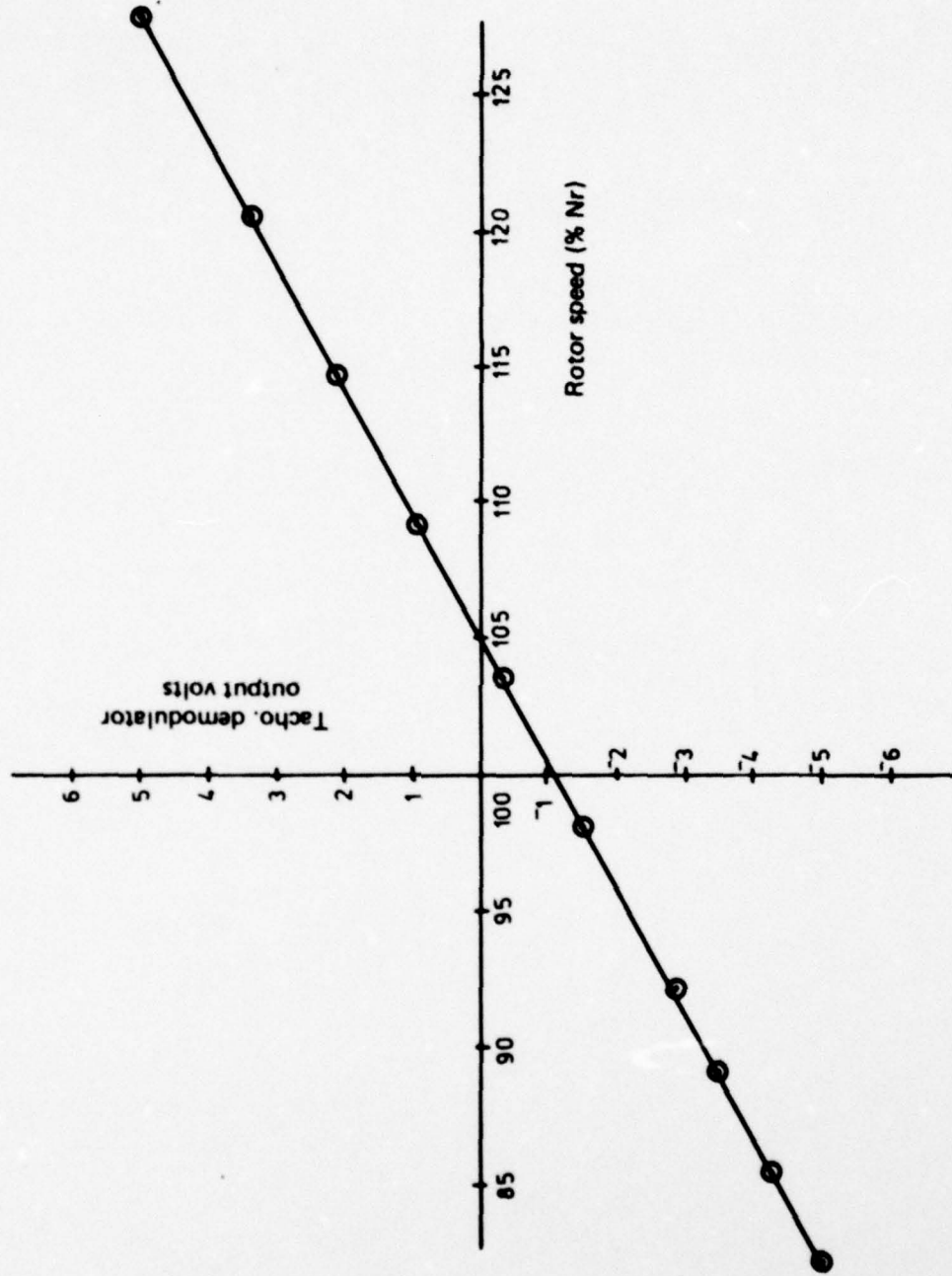


FIG. 16. INPUT/OUTPUT CHARACTERISTICS OF THE TACHOMETER DEMODULATOR

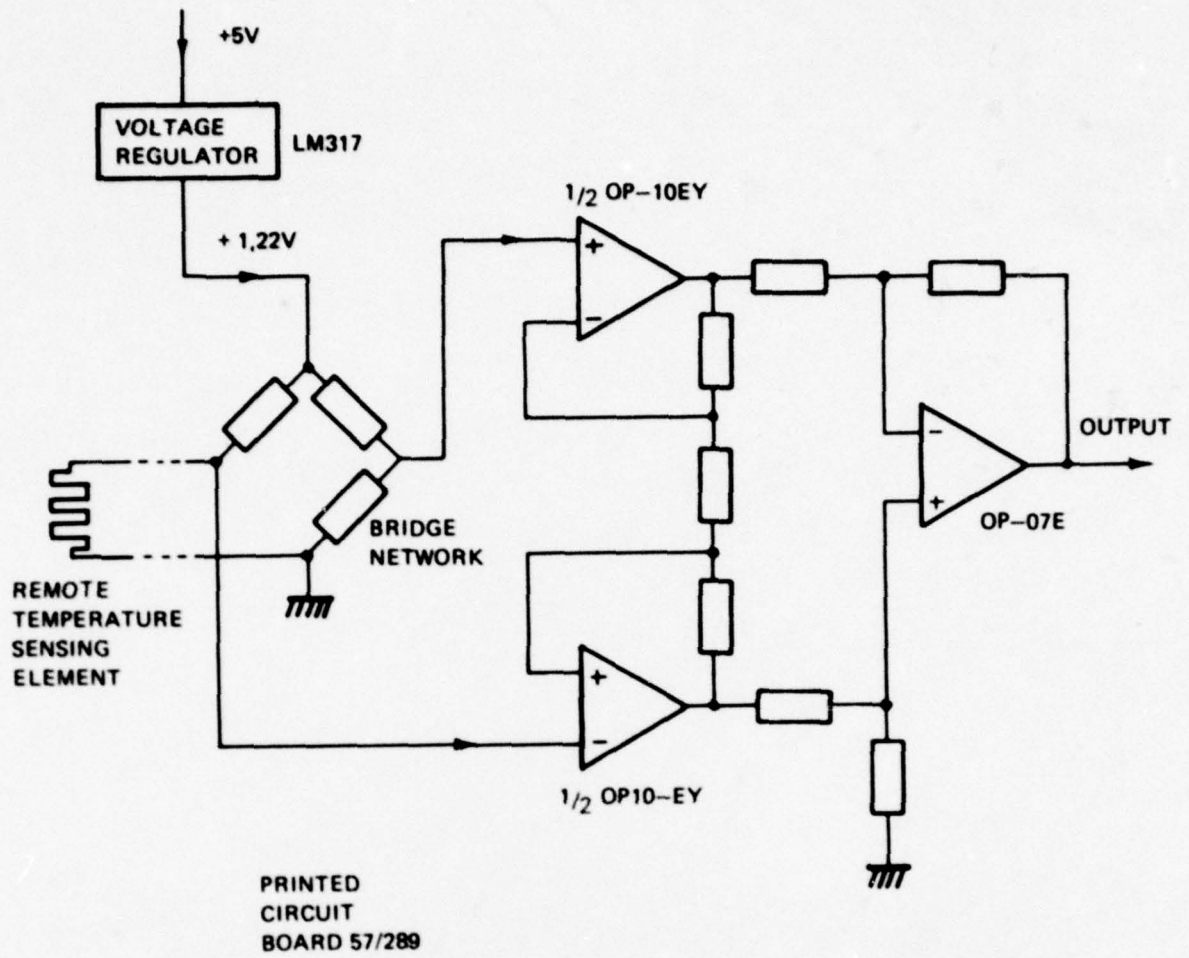


FIG. 17. TEMPERATURE MEASURING BRIDGE - SIMPLIFIED CIRCUIT DIAGRAM

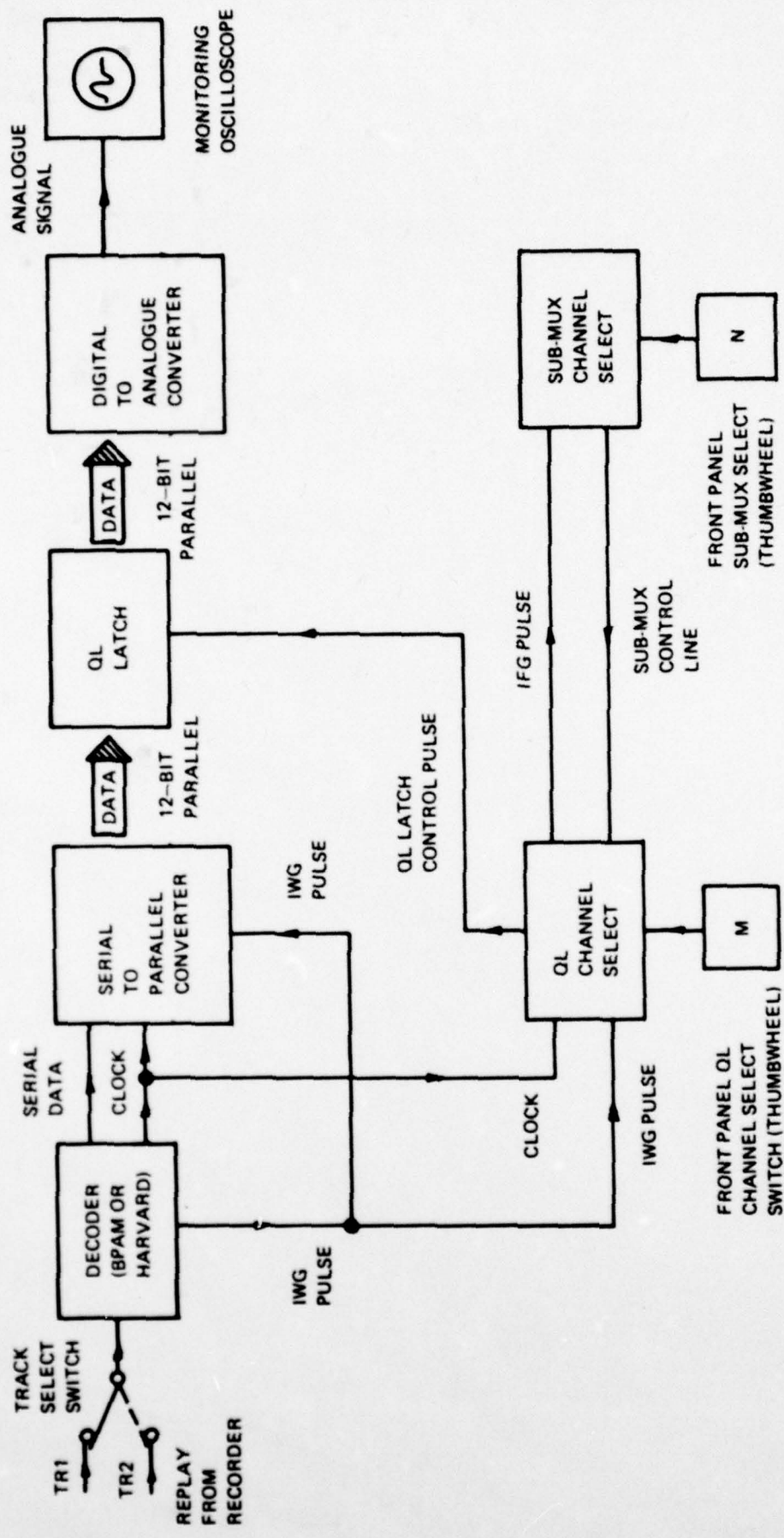


FIG. 18. QUICK-LOOK SECTION BLOCK DIAGRAM

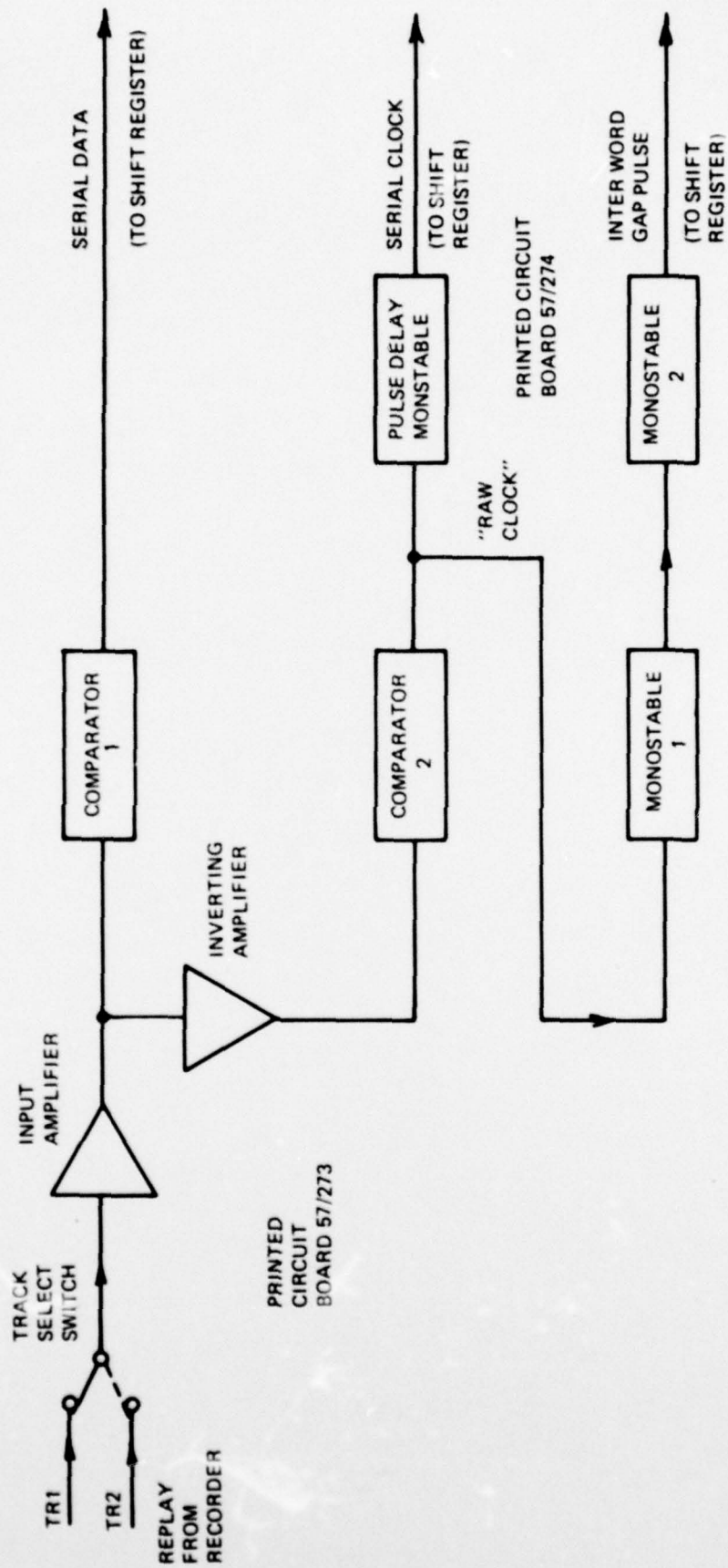


FIG. 19. BPAM DECODER BLOCK DIAGRAM

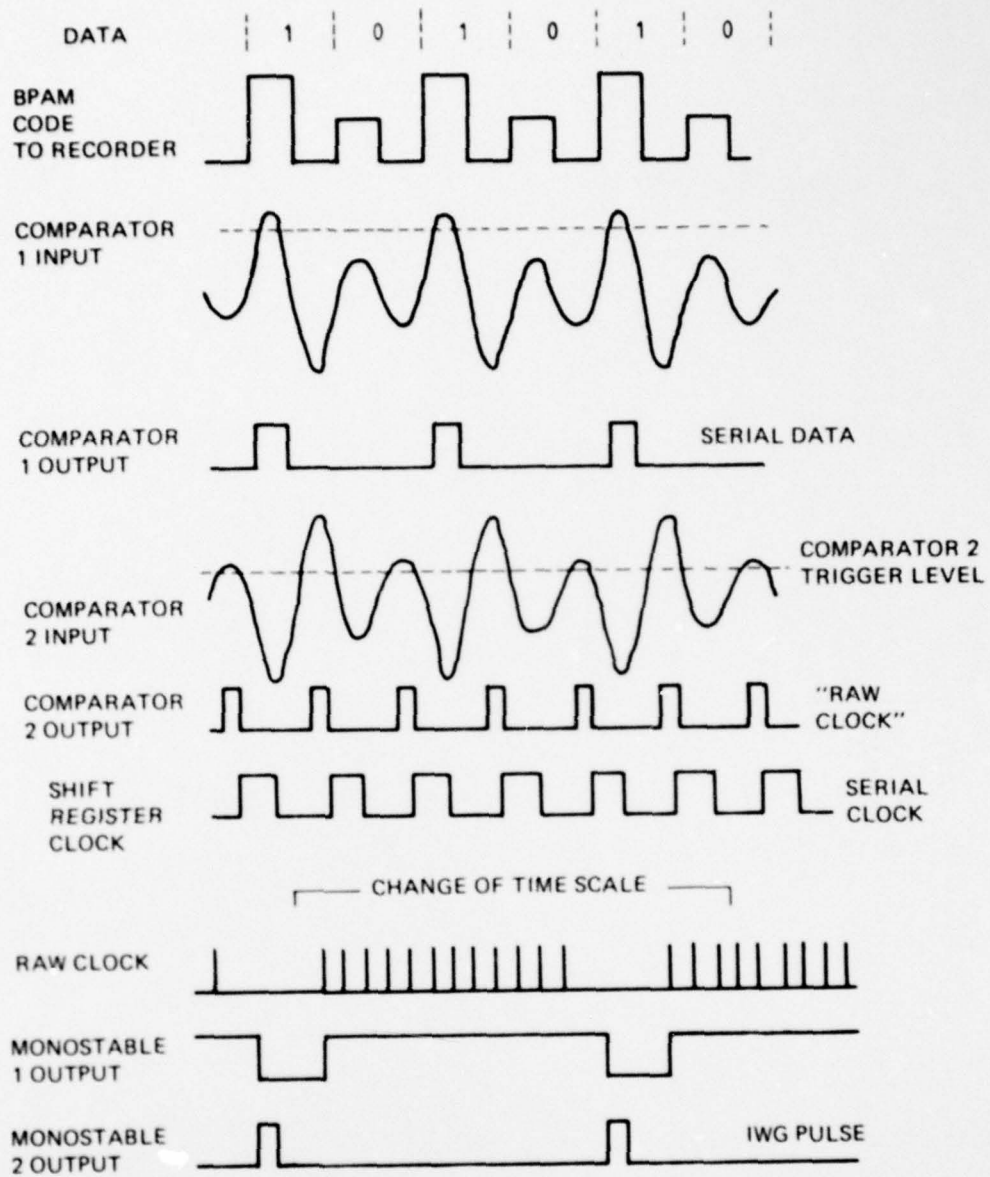


FIG. 20. BPAM DECODER TIMING DIAGRAM

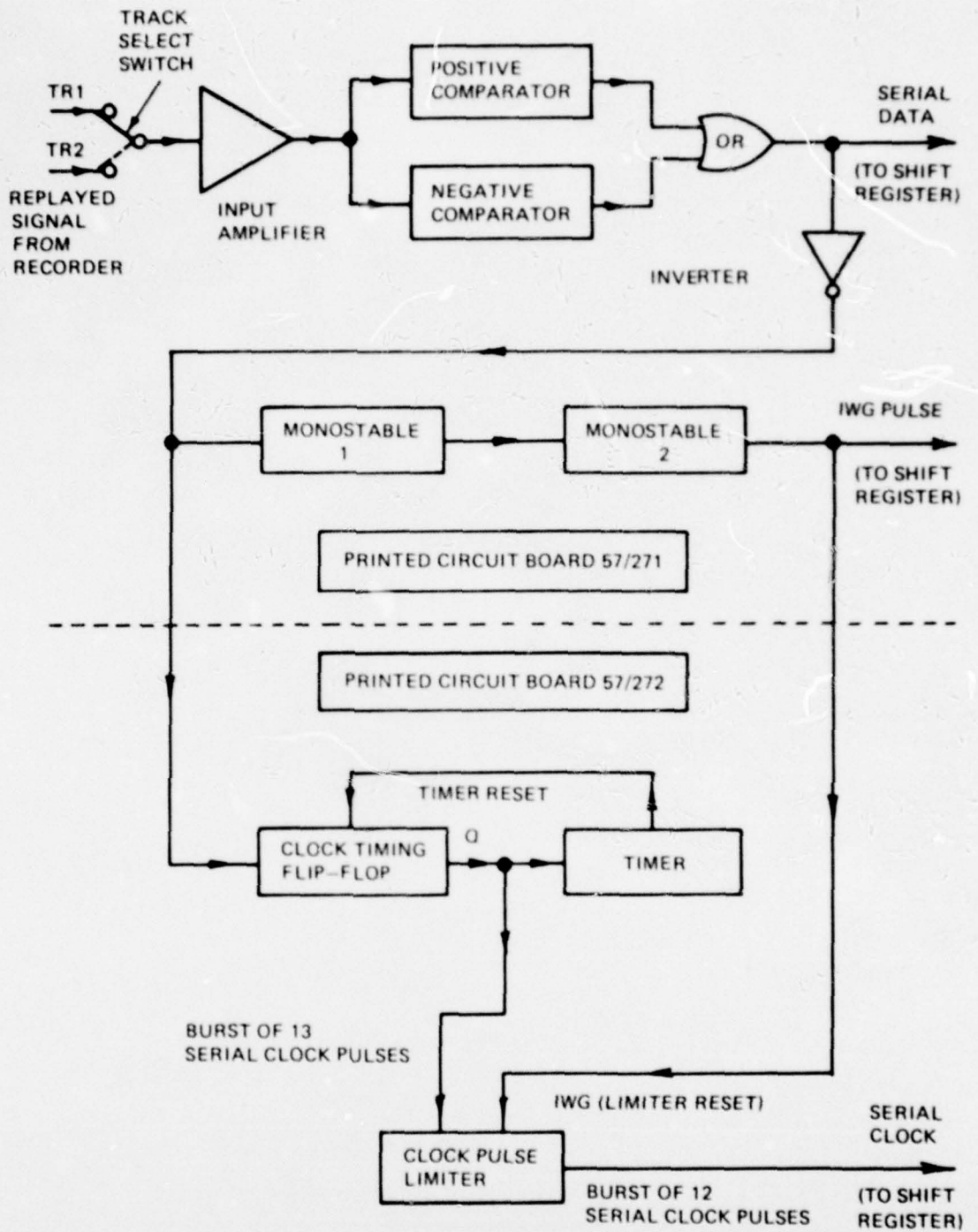


FIG. 21. HARVARD (BI-PHASE) DECODER TIMING DIAGRAM.

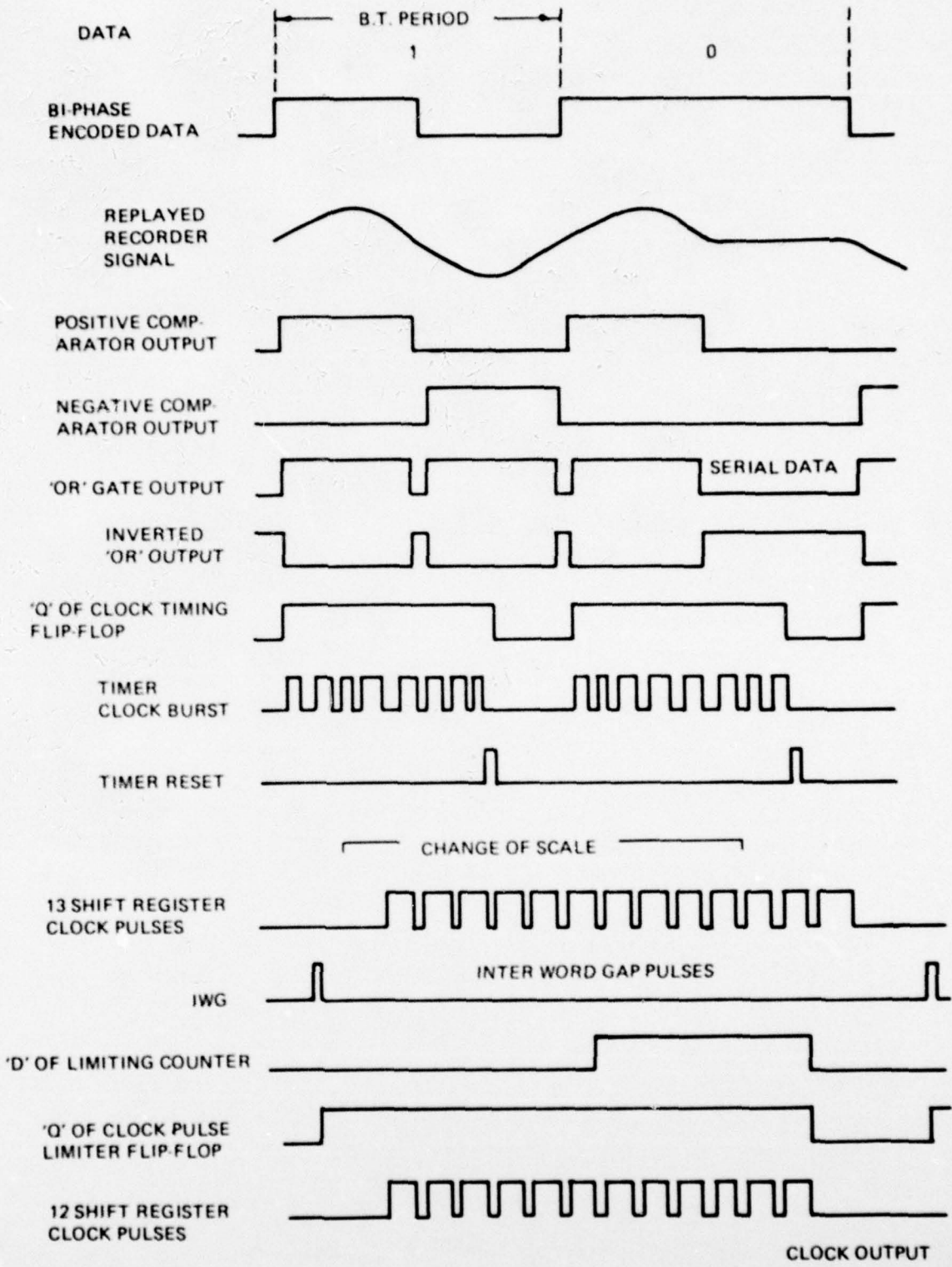


FIG. 22 HARVARD (BI-PHASE) DECODER TIMING DIAGRAM

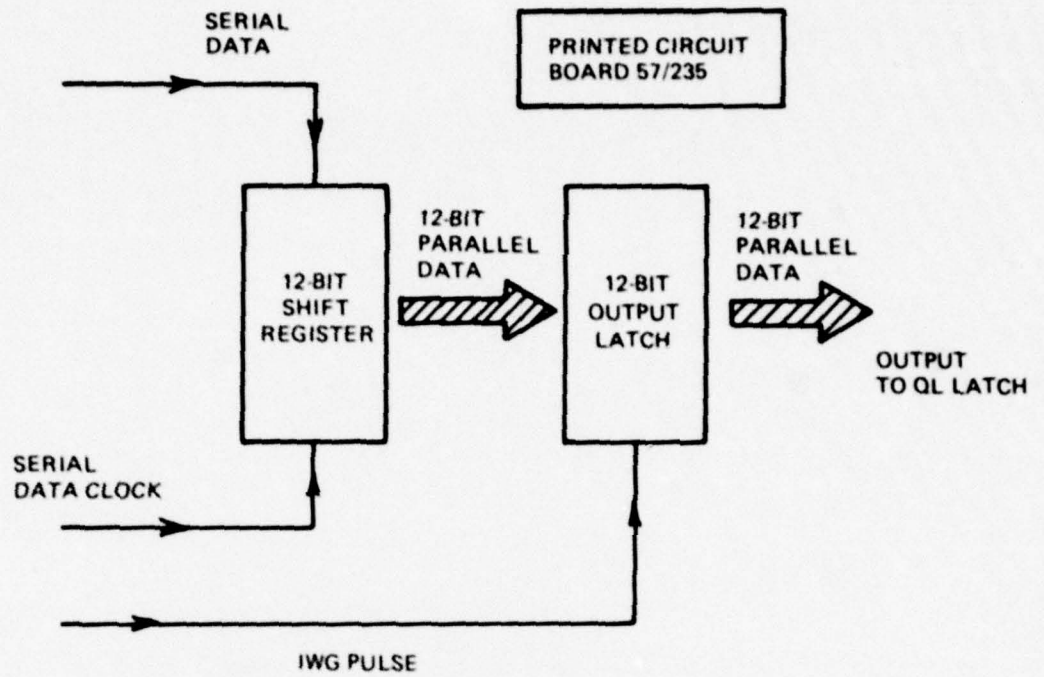


FIG. 23 (a) SERIAL TO PARALLEL CONVERTER BLOCK DIAGRAM

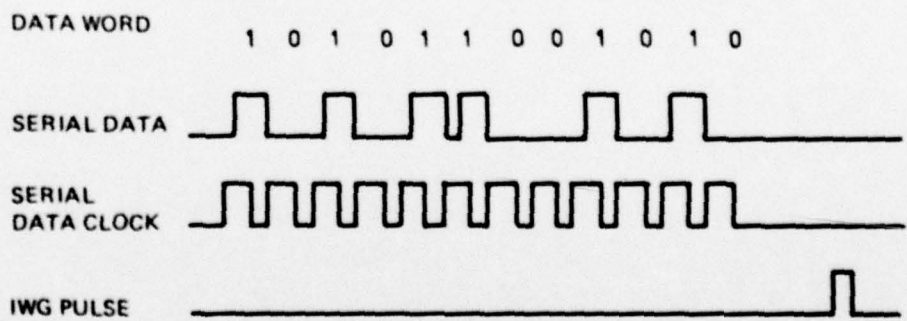


FIG. 23 (b) SERIAL TO PARALLEL CONVERTER TIMING DIAGRAM

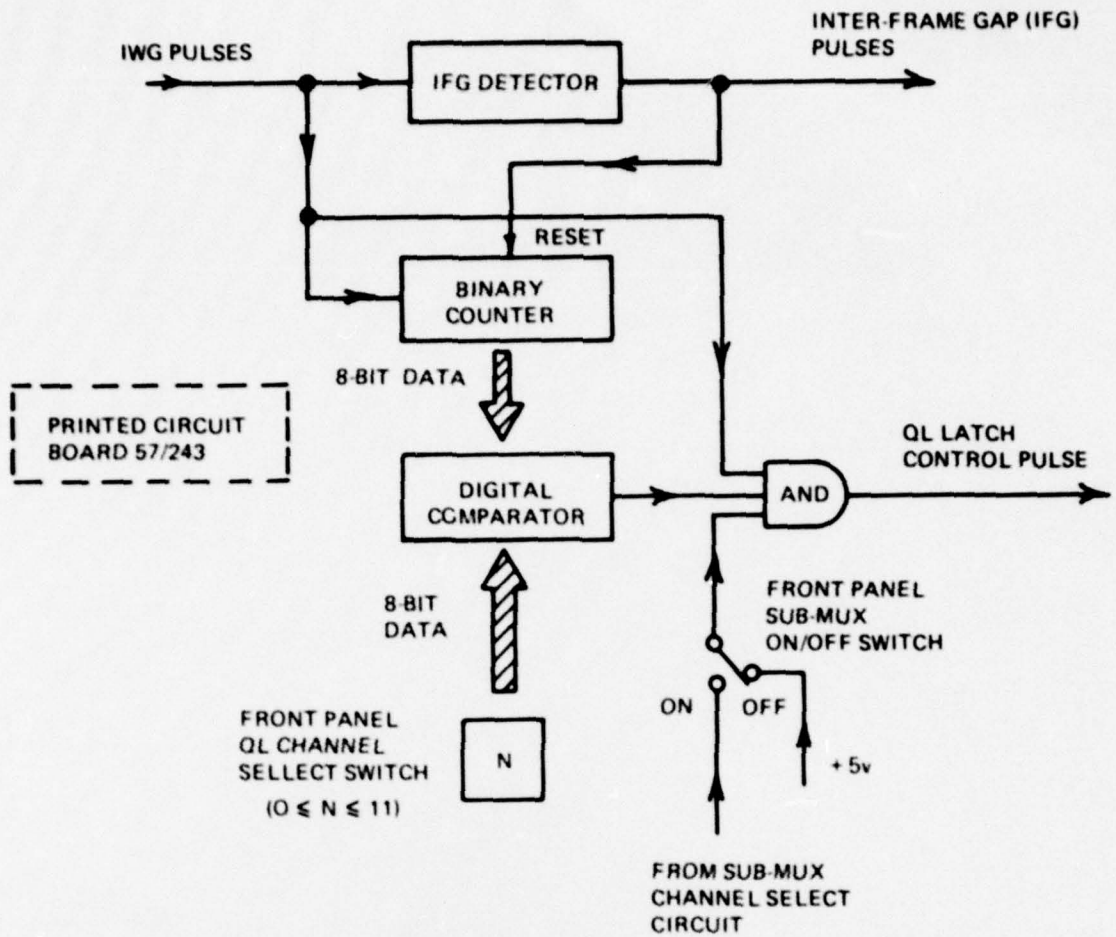


FIG. 24 (a) QL CHANNEL SELECT CIRCUIT BLOCK DIAGRAM

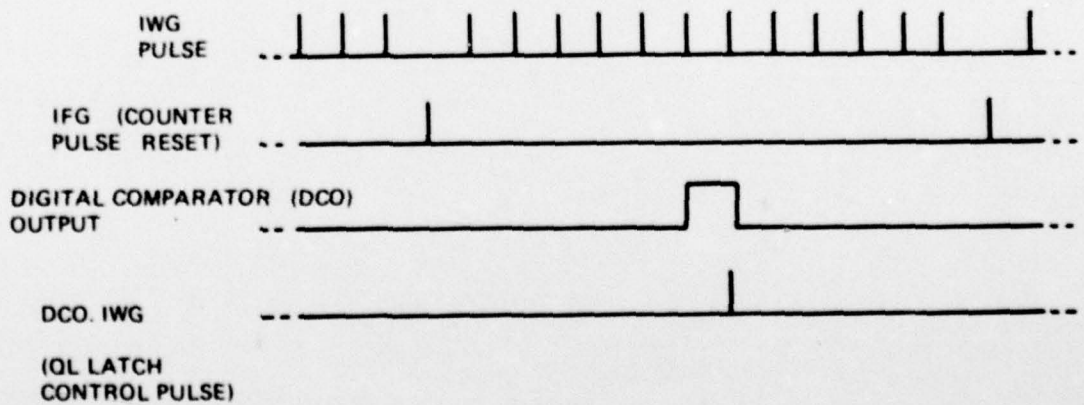


FIG. 24 (b) QL CHANNEL SELECT CIRCUIT TIMING DIAGRAM.

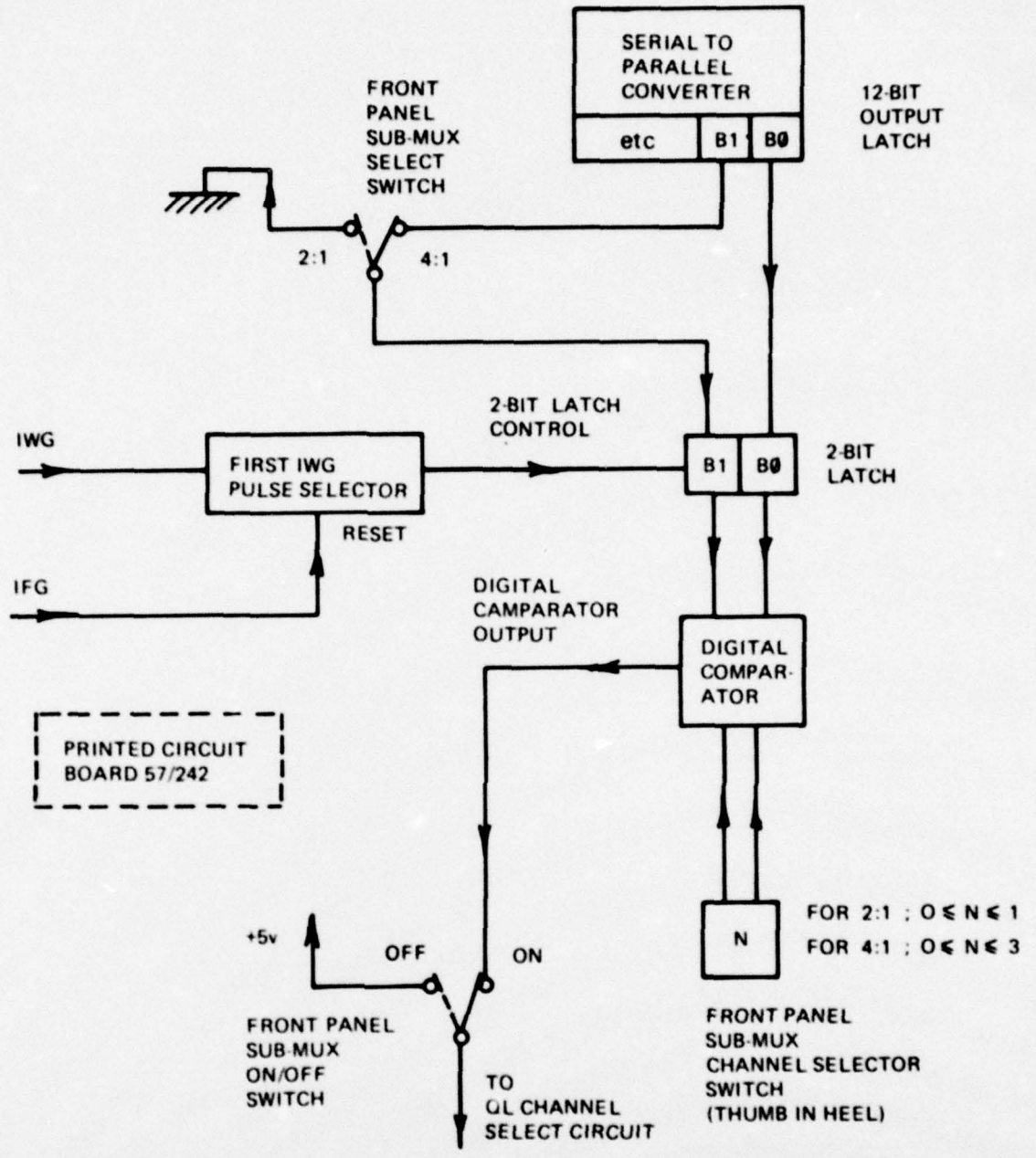


FIG 25. SUB-MULTIPLEXER CHANNEL SELECT CIRCUIT BLOCK DIAGRAM

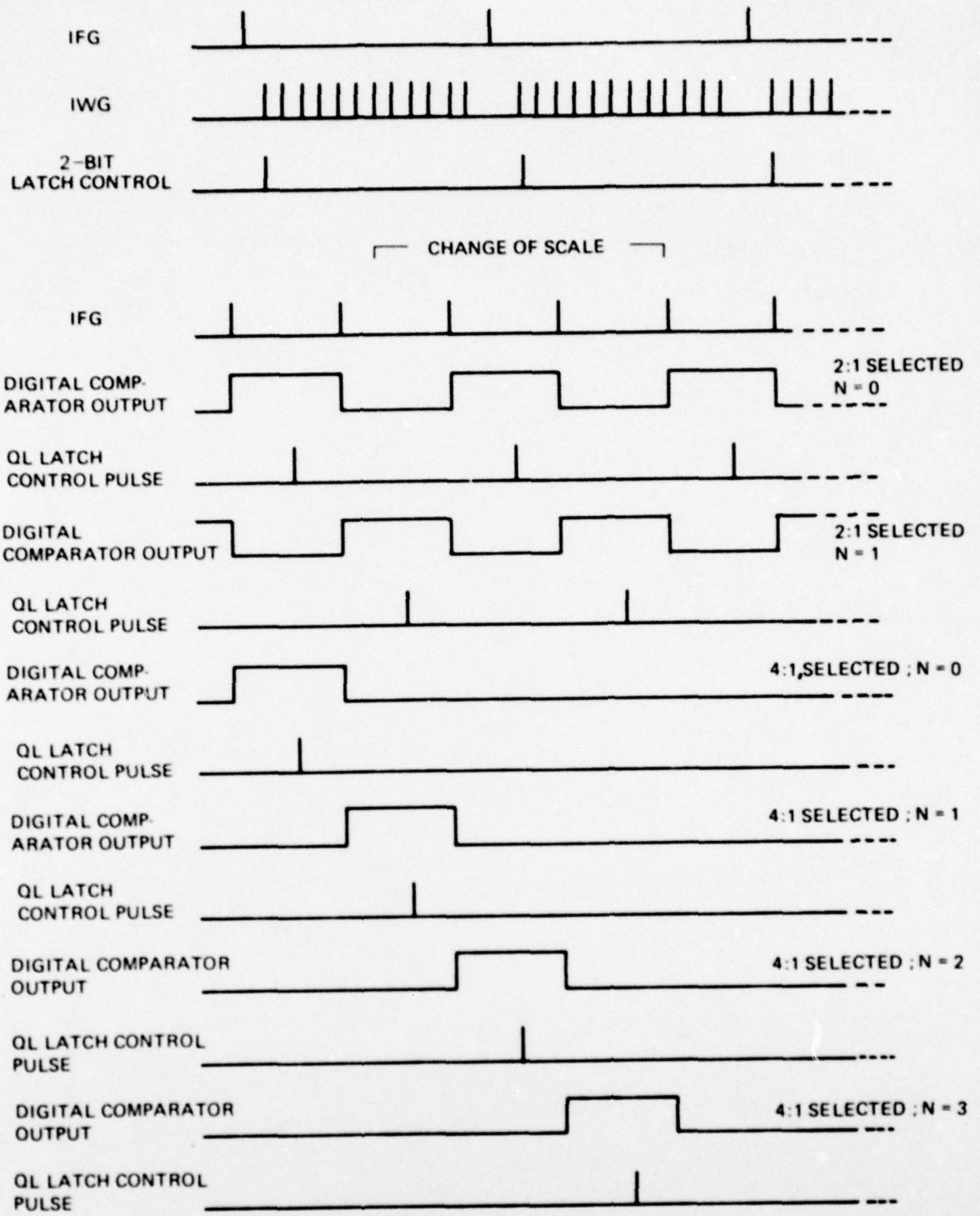
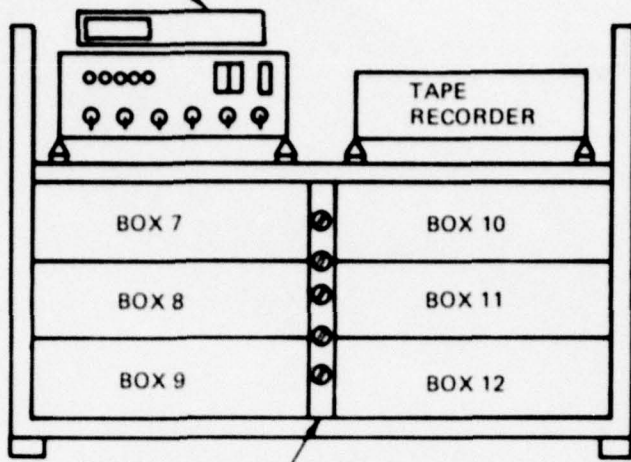


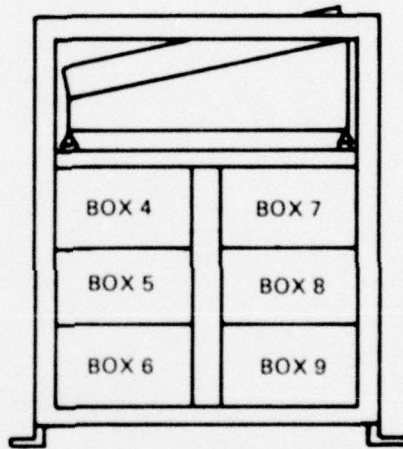
FIG. 26 SUB-MULTIPLEXER CHANNEL SELECT CIRCUIT TIMING DIAGRAM

MONITORING OSCILLOSCOPE

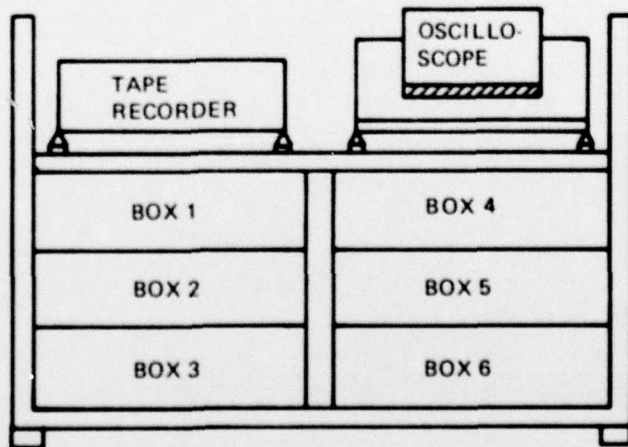


FRONT VIEW

DIGITAL INPUT CONNECTORS STRIP



SIDE VIEW



REAR VIEW

FIG. 27 DATA ACQUISITION SYSTEM GENERAL CONFIGURATION

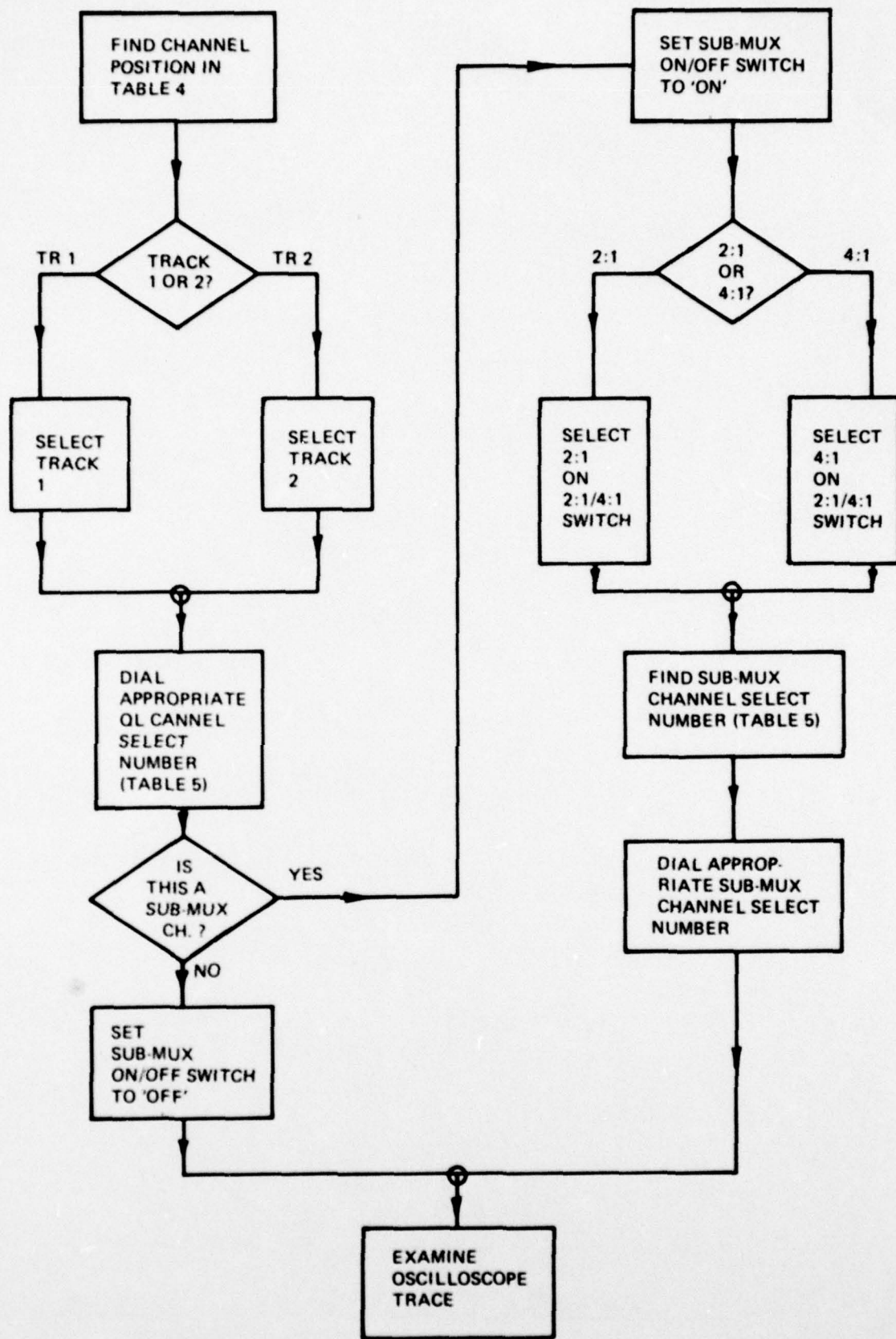


FIG. 28 QUICK LOOK CHANNEL SELECT PROCEDURE

**DOCUMENT CONTROL DATA SHEET**

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16. **ABSTRACT**

*A system is described which records 32 channels of analogue data in flight in digital form. Sampling rates of 15, 30 and 60 Hertz per channel are available, with an overall capacity of 1200 samples per second. The digital word size is 12 bits. Details of the circuits, including the in-flight quick-look facility are provided.*

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