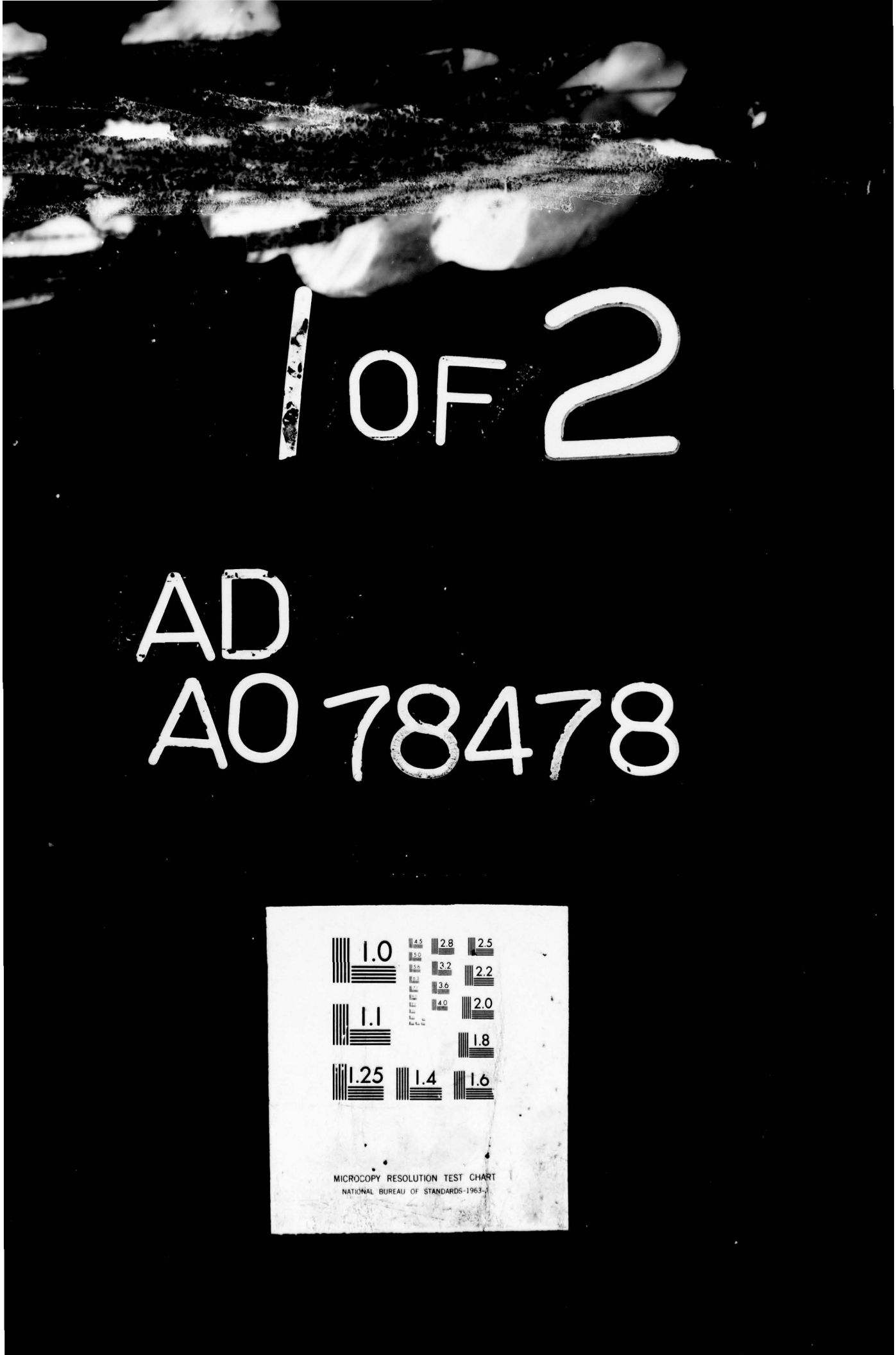
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RADC-TR-79-243
Final Technical Report
October 1979

SIGNAL PROCESSING FOR UNATTENDED RADAR

ITT-Gilfillan

John M. Milan
Robert H. Fletcher, Jr.
Charles D. Lucas, Jr.
Jack W. Goodwin

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SIGNAL PROCESSING FOR UNATTENDED RADAR

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RADC-TR-79-243 has been reviewed and is approved for publication.

APPROVED: Eugene J. Tippie

EUGENE J. TIPPIE
Project Engineer

APPROVED: Frank Rehm

FRANK J. REHM
Acting Technical Director
Surveillance Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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SPUR - Signal Processor for Unattended Radar
UAR - Unattended Radar
Optimum Filters
FFT - Fast Fourier Transfer
Clutter Processing
Signal Processing Architecture

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This final report documents the results of a six-month study conducted during Phase I of a contract to examine Signal Processing for Unattended Radars. Based on a general set of system and processor requirements for a representative unattended radar, various signal processing operations, architectures, and technologies are evaluated. A recommended signal processor is identified, and the selection rationale is presented. The principle selection criteria are those of reliability, performance, cost, maintainability, risk and power consumption. The major risk areas in the selected processor have been (Cont'd)

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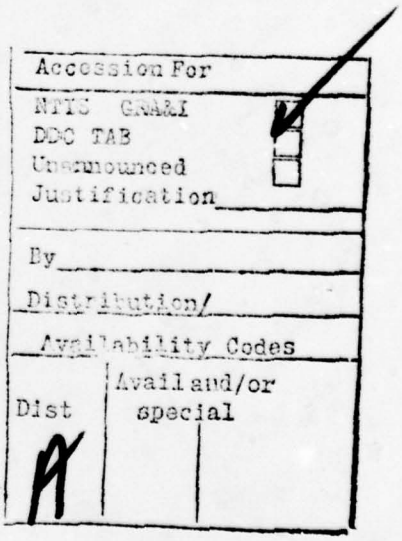
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identified and a validation plan proposed for Phase II of the SPUR effort. This plan consists of recommended approaches, including a formal test plan, for reducing these risks.

PREFACE

This Final Report Summary provides a brief description of the activities conducted during the six-month Phase I effort of the Signal Processor for Unattended Radar (SPUR), Contract No. F30602-78-C-0288. The basic requirements of the SPUR are identified, and the optimum processor resulting from the numerous tradeoffs of the study is described. A brief discussion of the Phase II Validation Plan is also provided.

A detailed description of the total Phase I effort is given in the Signal Processor for Unattended Radar (SPUR), Phase I, Final Report, dated 28 March 1979.



SIGNAL PROCESSOR FOR UNATTENDED RADAR (SPUR)

Final Report

SUMMARY

A major factor in the rapidly escalating costs of present day radar systems is that associated with operational and support personnel. As a consequence, there is considerable interest in reducing personnel requirements through the development of minimally attended and unattended radars. Several studies have been conducted which indicate that the radar signal processor, with its potential reliability problems, may be the most critical element in the system. The Signal Processor for Unattended Radar (SPUR) program was initiated to determine the optimum processor architecture and appropriate technology to support the development of an unattended radar.

The program, as defined by the Air Force, consists of two phases. Phase I called for an investigation of all potentially promising components, technologies, and architectures in order to identify the optimum processor configuration. In addition, sufficient analysis and design detail was required to demonstrate that the performance and functional requirements of the processor can be met. A further requirement of the Phase I effort was identification of the major processor risk areas and development of a Validation Plan for Phase II. These activities have been completed and are documented in the SPUR final report.

Phase II, which is optional to the Government, involves detail design, fabrication, and testing of the critical processor elements, both hardware and software. The plan for this activity, including a Phase II test plan, is also presented in the final report.

SPUR REQUIREMENTS AND PARAMETERS

Many of the basic signal processor requirements and parameters were postulated at the beginning of the study in order to bound the areas of investigation to a reasonable set of processor configurations. The major performance, functional, and environmental parameters for the processor are listed in Table 1-I. These parameters were established as guidelines only, and one of the requirements of the study was to identify any parameter which seriously impacts the processor design and to recommend alternative approaches.

OPTIMIZATION CRITERIA

The SPUR parameters and requirements established the basic constraints for determining the optimum processor configuration. The prime objective of the study was to develop a signal processor design which will satisfy these requirements and, at the same time, can be efficiently implemented. Thus, while reliability and performance are considered to be the major factors in optimizing the processor, there are other characteristics to be considered as well. These include, for example:

a) Automatic calibration and repair capabilities,
b) Modularity concepts and ease of maintenance,

TABLE 1-I. REQUIREMENTS AND PARAMETERS ESTABLISHED TO BOUND THE SPUR STUDY EFFORT

Performance:	
Range	5-60 nmi
Range Resolution	0.1 nmi
Land Clutter Improvement Factor	>50 dB
MTBF	20K to 100K hrs
Functions:	
Pulse Compression	32:1
Spectral Filtering	8-Pulse
CFAR	32 Cell Averaging
Clutter Map	Zero Velocity Superclutter/ Intraclutter Detection Processing
MTI	In Conjunction w/Spectral Filtering
Postdetection Integration	4 Pulses
Environmental:	
Operating Temperature Range = 0°F to +120°F	
Storage Temperature Range = -70°F to +100°F	

9524a-1

c) Risks and risk abatement approaches,
d) Cost,
e) Power consumption.

In order to account for these various characteristics in evaluating alternative implementations, weighting factors were assigned in accordance with Table 1-II. The weights are to some extent arbitrary; however, they do indicate the relative importance of the different characteristics assumed during the numerous tradeoffs conducted in the study.

OPTIMUM PROCESSOR

Using the optimization criteria discussed above, the optimum processor for the SPUR was determined. Figure 1 provides the basic block diagram of the processor. Its principle characteristics are listed in Table 1-III.

TABLE 1-II. WEIGHTING FACTORS ESTABLISHED FOR EVALUATING ALTERNATIVE PROCESSOR CONFIGURATIONS

	Weighting	Comments
Reliability *	10	Fault-Tolerant Design*
Performance	10	Meet Requirements
Cost	7	60 Systems
Maintainability*	6	Remove and Replace Concept
Risk	6	Near Term Requirement Reduces Risk
Power	5	Minimize

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*Fault-tolerant design improves maintainability.

The selected architecture employs two A/D converters for separate I & Q channels with a single additional converter utilized as a hot spare in standby redundancy. It has its own automatic calibration loop and dedicated test logic.

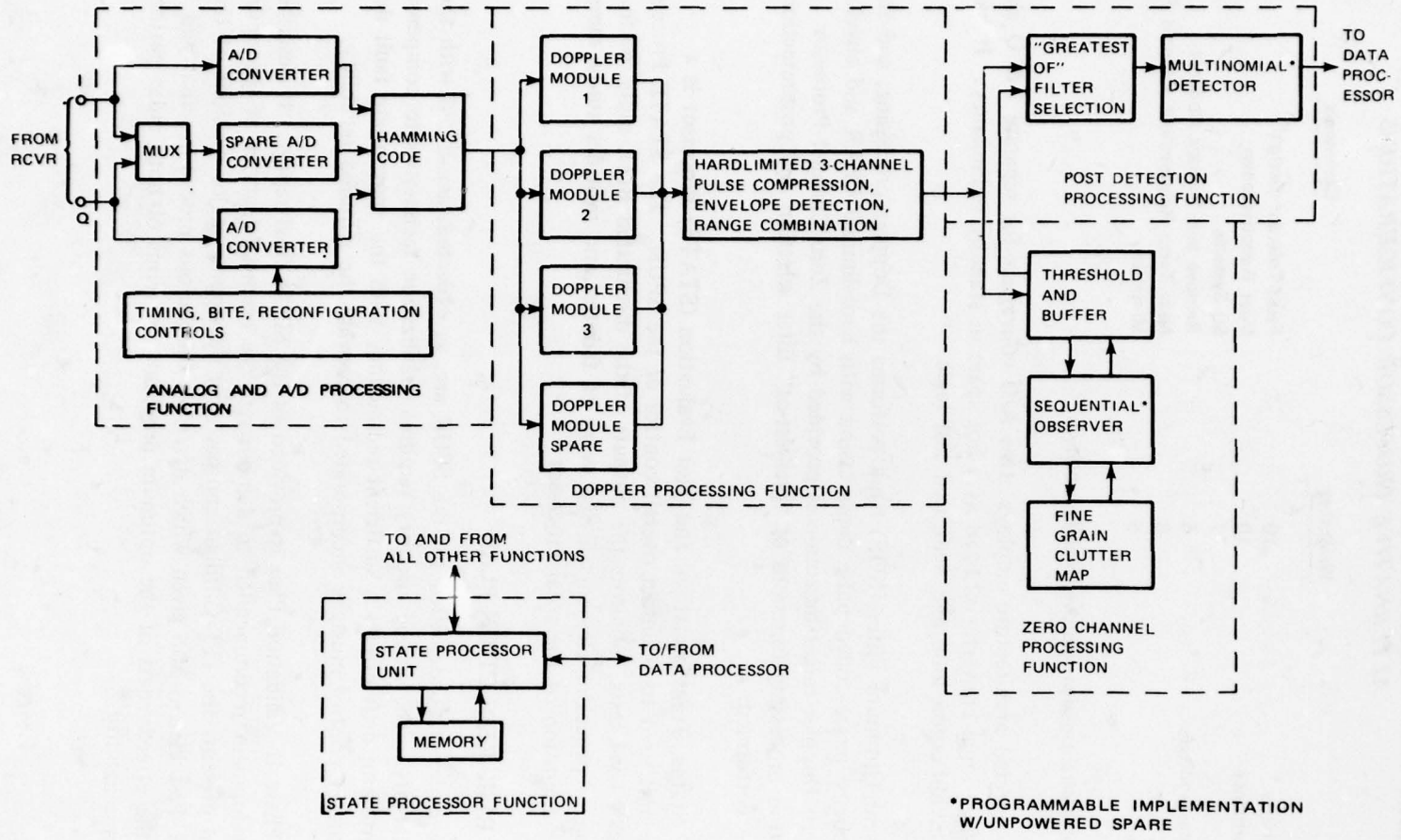
A Near Optimum Filter (NOF) bank performs the Doppler processing, and this is followed by binary phase-coded pulse compression with hard-limited CFAR and envelope detection. Zero Doppler target detection is provided by the Zero Channel Processor. Finally the postdetection processing functions of "greatest-of" filter selection and postdetection integration are performed.

The Status, Transformation, and Test Evaluation (STATE) Processor is a programmable unit used to maintain overall control of the SPUR. The STATE Processor directs processor level tests, monitors the outputs of the distributed BITE units, performs the reconfiguration of processor elements in the event of failures, and provides status messages describing the condition of the total processor.

RISKS AND RISK REDUCTION PLAN

The major risks identified for the SPUR are, as expected, associated with the processor reliability. The analog circuitry requires stabilization techniques to compensate for long-and short-term drift effects. Sufficient redundancy with the appropriate fault detection logic and recovery control must be incorporated to provide the required reliability.

A Phase II Validation Plan is provided in the SPUR final report. It describes the hardware development recommended to demonstrate the essential features of the optimum processor and presents the ITT Gilfillan approach for developing major portions of this hardware. A Test Plan is also given which describes the various procedures that will be used in verifying the effectiveness of the optimum processor, in terms of both radar performance and processor reliability.



S-4

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Figure 1. Overall Block Diagram of the SPUR *which defines the five selected processing functions and operations performed in each*

TABLE 1-III. CHARACTERISTICS OF THE SPUR

A/D Converter

11 bits
Double Sampling in Range (1.6 MHz rate)
dc Correction Loop for stability

Doppler Filtering

Narrowband Filterbank of 6 Near Optimum Filters (including zero filter) generated from a 9-pulse coherent group (including 1 fill pulse).

50.9 dB Land Clutter Improvement Factor

Pulse Compression and CFAR

Hard limited 31-bit binary phase-coded pulse compressor with offset channels for high velocity targets.

Zero Channel Processing

Fine grain clutter map and censor process for intraclutter visibility of crossing targets.

Postdetection Processing

Sequential greatest of filter selection followed by multinomial detection on four hits.

Distributed BITE with STATE Processor for Monitor and Control

MTBF:	22,331 hours
Power:	219 watts
Processing Gain:	0.15 dB worst case

PREFACE

This Final Report documents the activities conducted during the six-month Phase I effort of the Signal Processor for Unattended Radar (SPUR), Contract No. F30602-78-C-0288. Included in this report is an examination of the basic processor requirements and evaluation of the most promising architectures for satisfying these requirements. Assessments of the applicable technologies, both analog and digital, are also provided. The result of these activities is a recommended signal processor architecture – called the optimum processor – along with its specific performance and reliability requirements.

In support of the Air Force optional Phase II effort, the major processor risk areas are identified. Plans for reducing the risks associated with these areas and for validating the recommended processor configuration are also provided. A major element of these plans is the Phase II Test Plan included in this report. During the detail design activities of Phase II, minor modifications to the plan are anticipated in order to more closely relate to the final processor configuration. These changes will be documented in the Test Plan update called for during Phase II.

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EVALUATION

With the continuing inflationary trends, the cost of manpower for operating and maintaining radar surveillance sites has become an excessive burden for the Air Force. Initial investigation of the problems associated with unmanned or minimally manned sites had highlighted the signal processing as one of the major technical challenges. The Signal Processing for Unattended Radar (SPUR) Study provides a base for estimating performance, reliability, power consumption, and cost for radar signal processing for future RADC efforts as they apply to TPO R1C. The study specifically addresses the problems and parameter as reflected by the need for an unattended radar for the DEW line. The study demonstrates the feasibility of utilizing existing and/or near term technology to perform the signal processing in an unattended environment while meeting the reliability, power and cost restraints of the DEW line.

Eugene J. Tjimie

EUGENE J. TIMMIE
Project Engineer

Section 1

INTRODUCTION

Rapid advances in technology in recent years have led to a considerable expansion in the capabilities and sophistication of modern radars. More exacting mission requirements are being established which call for improved performance and expanded capabilities. Simultaneously, budgetary limitations provide increasing pressure for minimizing the Life Cycle Costs (LCC) of systems. A major factor in the LCC equation is the cost associated with qualified support and operator personnel. As a result, efforts to capitalize on the advances of technology while reducing the ever increasing manpower costs are receiving considerable emphasis within the U.S. Air Force and other armed services as well.

These considerations are apparent, for example, in the requirements for the 3D Minimally Attended Radar (MAR) of the Air Force SEEK IGLOO program and, to an even greater extent, by the Unattended Radar (UAR) planned for the SEEK FROST program. For both of these systems, the reduction or elimination of on-site and support personnel will significantly reduce operating and maintenance (O&M) costs of the systems relative to more conventional radars.

In 1976 the Air Force funded three Unattended/Minimally Attended Radar Design Studies – by ITT Gilfillan, General Electric, and Raytheon – to examine various approaches for replacing the current DEW Line radars with unattended radars. One of the major conclusions resulting from these studies is that, in many respects, the radar signal processor may be the most critical element of the system. This is particularly true in terms of reliability and minimum prime power requirements. As a result, the Air Force awarded to ITT Gilfillan, through a competitive procurement, the Signal Processor for Unattended Radar (SPUR) contract with the objective of obtaining an optimum processor design.

The program, as defined by the Air Force, consists of two phases. Phase I called for the investigation of all potentially promising components, technologies, and architectures in order to identify the optimum processor configuration. In addition, sufficient analysis and design detail was required to demonstrate that the performance and functional requirements of the processor can be met. A further requirement of the Phase I effort was an identification of the major processor risk areas and the development of a Validation Plan for Phase II. This report documents the activities and principle results of the Phase I effort.

Phase II, which is optional to the Government, involves the detail design, fabrication, and testing of the critical processor elements, both hardware and software. The plan for this activity is discussed in Section 7 of this report. A major element of the Validation Plan is the Phase II Test Plan given in Appendix A.

1.1 SPUR REQUIREMENTS AND PARAMETERS

A number of the basic signal processor requirements and parameters were postulated at the beginning of the study in order to bound the areas of investigation to a reasonable set of processor configurations. The major performance, functional, and environmental parameters for the processor are listed in Table 1-I. These parameters were established as guidelines only, and one of the requirements of the study was to identify any of the parameters which seriously impact the processor design and to recommend alternative approaches.

As a further bound on the areas of investigation, the processor was defined to be those functions normally occurring between the video detectors and the declaration of a target following postdetection integration. One principle exception was the possible inclusion of IF pulse compression which normally precedes the quadrature detectors. Thus the SPUR study is concentrated on the processing functions frequently termed ***signal*** processing and does not address the so-called ***data*** processing operations. In the past, these areas often corresponded to the division between special purpose and general purpose hardware. However, this distinction is becoming increasingly blurred with the advances in speed and power of programmable devices.

The object in limiting the processor to the areas discussed above was to develop an optimized design that was as independent of the other parameters of the radar as possible. Thus, the results of this study should have broad applicability to a variety of different radar implementations. In conducting some of the performance tradeoffs and analyses, however, it was necessary to make some additional assumptions about the other radar characteristics. The major assumptions of this nature are provided in Table 1-II. These parameters were used in clutter calculations, in loss calculations for high velocity targets, and in establishing signal-to-noise (s/n) levels through the different parts of the processor. In general, these parameters affect characteristics such as dynamic range, memory sizing, etc., and do not strongly impact the basic architecture of the signal processor.

In addition to the processing parameters and requirements discussed above, the clutter environment for the unattended radar was also specified. This is given in Table 1-III. It was assumed that in general, more than one type of clutter, for example, ground and weather clutter, may be present at the same time in a particular range bin.

1.2 OPTIMIZATION CRITERIA

The SPUR parameters and requirements discussed in the previous section, established the basic constraints for determining the optimum processor configuration. The prime objective of the study was to develop a signal processor design that will satisfy these requirements and, at the same time, can be efficiently implemented. Thus, while reliability and performance are considered to be the major factors in optimizing the processor, there are other characteristics to be considered as well. These include, for example:

a) Automatic calibration and repair capabilities,
b) Modularity concepts and ease of maintenance.

TABLE 1-I. REQUIREMENTS AND PARAMETERS ESTABLISHED TO BOUND THE SPUR STUDY EFFORT

Performance:	
Range	5-60 nmi
Range Resolution	0.1 nmi
Land Clutter Improvement Factor	>50 dB
MTBF	20K to 100K hrs
Functions:	
Pulse Compression	32:1
Spectral Filtering	8-Pulse
CFAR	32 Cell Averaging
Clutter Map	Zero Velocity Superclutter/ Intraclutter Detection Processing
MTi	In Conjunction w/Spectral Filtering
Postdetection Integration	4 Pulses
Environmental:	
Operating Temperature Range = 0°F to +120°F	
Storage Temperature Range = -70°F to +100°F	

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TABLE 1-II. ADDITIONAL RADAR PARAMETERS ASSUMED IN CONDUCTING PERFORMANCE TRADEOFFS AND ANALYSES

Baseline Radar Parameters:	
Antenna Beamwidths	
Azimuth	3°
Elevation	30°
Antenna Rotation Rate	15 rpm
Target Velocity	±2400 Knots
Probability of Detection	90% (after PDI)
Probability of False Alarm	2×10^{-5} (after PDI)

9524-68

TABLE 1-III. A CLUTTER MODEL THAT CHARACTERIZES THE SPUR RADAR ENVIRONMENT

Land Clutter		
Amplitude Distribution	Log – Normal	
Reflectivity		
Median	-34 dB m^2/m^2	
84th Percentile	-24 dB m^2/m^2	
Spectrum (Gaussian)		
Standard Deviation (30 knot wind)	0.2 m/sec	
Sea Clutter (Sea State 4)		
Amplitude Distribution	Rayleigh	
Reflectivity/Grazing Angle/ Polarization	H	V
1.0 degree	-52	-45 dB m^2/m^2
3	-48	-38
10	-45	-31
Spectrum (Gaussian)		
Mean Velocity	2.5	1.3 m/sec
Standard Deviation	0.9	0.9 m/sec
Weather Clutter (15 mm/hr Rain)		
Cell Diameter	5 nmi	
Ceiling	30K ft	
Radial Velocity	0 to 80 knots	
Shear	0 to 80 knots from 0 to 50K feet with any arbitrary shear distribution over this altitude range	
Amplitude Distribution	Rayleigh	
Reflectivity	-88 dB m^2/m^3	

9524-69

c) Risks and risk abatement approaches,
d) Cost,
e) Power consumption.

In order to account for these various characteristics in evaluating alternative implementations, weighting factors were assigned in accordance with Table 1-IV. The weights are, to some extent, arbitrary; however, they do indicate the relative importance of the different characteristics assumed during the numerous tradeoffs conducted in the study.

1.3 OPTIMUM PROCESSOR

The optimum processor for the SPUR has been determined using the optimization criteria discussed above. We now give a brief summary description of the optimum processor and its principle characteristics that resulted from the study. Subsequent sections of this report describe the detailed analyses and tradeoffs conducted in arriving at this approach. More detail regarding the optimum processor and the tradeoffs leading to its selection is provided in Section 6, Description of Optimum Processor.

Figure 1-1 is a block diagram of the optimum processor. Some of the most important features incorporated in the processor design are listed in Table 1-V. Table 1-VI summarizes the major parameters. In developing this approach five functional areas were identified. These are Analog and A/D; Doppler; Zero Channel; Post Detection; and Status Transformation, and Test Evaluation (STATE) Processor Functions.

1.3.1 Analog and A/D Processing Function

The A/D converter is the principal element in this functional area. The selected architecture employs two A/D converters for separate I and Q channels with a single additional converter utilized as a hot spare in standby redundancy. The hot spare is used to avoid having to switch the five voltage levels required for the A/D. Dedicated test logic is provided to continually test all three converters, to isolate a faulty channel, and provide status to the STATE processor. An automatic calibration loop is also provided to compensate for drift in analog components. The A/D converter is designed to test and reconfigure itself; thus the STATE processor is just a monitor for this unit.

1.3.2 Doppler Processing Function

This functional area contains the Near Optimum Filter (NOF) Bank, binary phase-coded pulse compression with hard limited CFAR, and the envelope detection circuitry. The NOF Bank is built around the LSI multiplier-accumulator chips. The pulse compression and envelope detection operations are hard-wired parts of the processor. Moreover the pulse compression operation is implemented in three parallel channels, each matched to different velocity targets. This is done to compensate for s/n losses that normally accompany high velocity targets when a binary phase-coded waveform is used.

TABLE 1-IV. WEIGHTING FACTORS ESTABLISHED FOR EVALUATING ALTERNATIVE PROCESSOR CONFIGURATIONS

	Weighting	Comments
Reliability *	10	Fault-Tolerant Design*
Performance	10	Meet Requirements
Cost	7	60 Systems
Maintainability*	6	Remove and Replace Concept
Risk	6	Near Term Requirement Reduces Risk
Power	5	Minimize

9524-70

*Fault-tolerant design improves maintainability.

TABLE 1-V. SOME PRIME FEATURES INCORPORATED IN THE OPTIMUM PROCESSOR DESIGN

Double Sampling in Range

11 Bits A/D Conversion

Near Optimum Filter Doppler Processing (9 pulses – 6 filters)

31-Bit Binary Phased-Coded Pulse Compression with offset channels for high velocity targets

Hard-Limited CFAR

Zero Doppler Processing for Intraclutter Visibility of Crossing Targets

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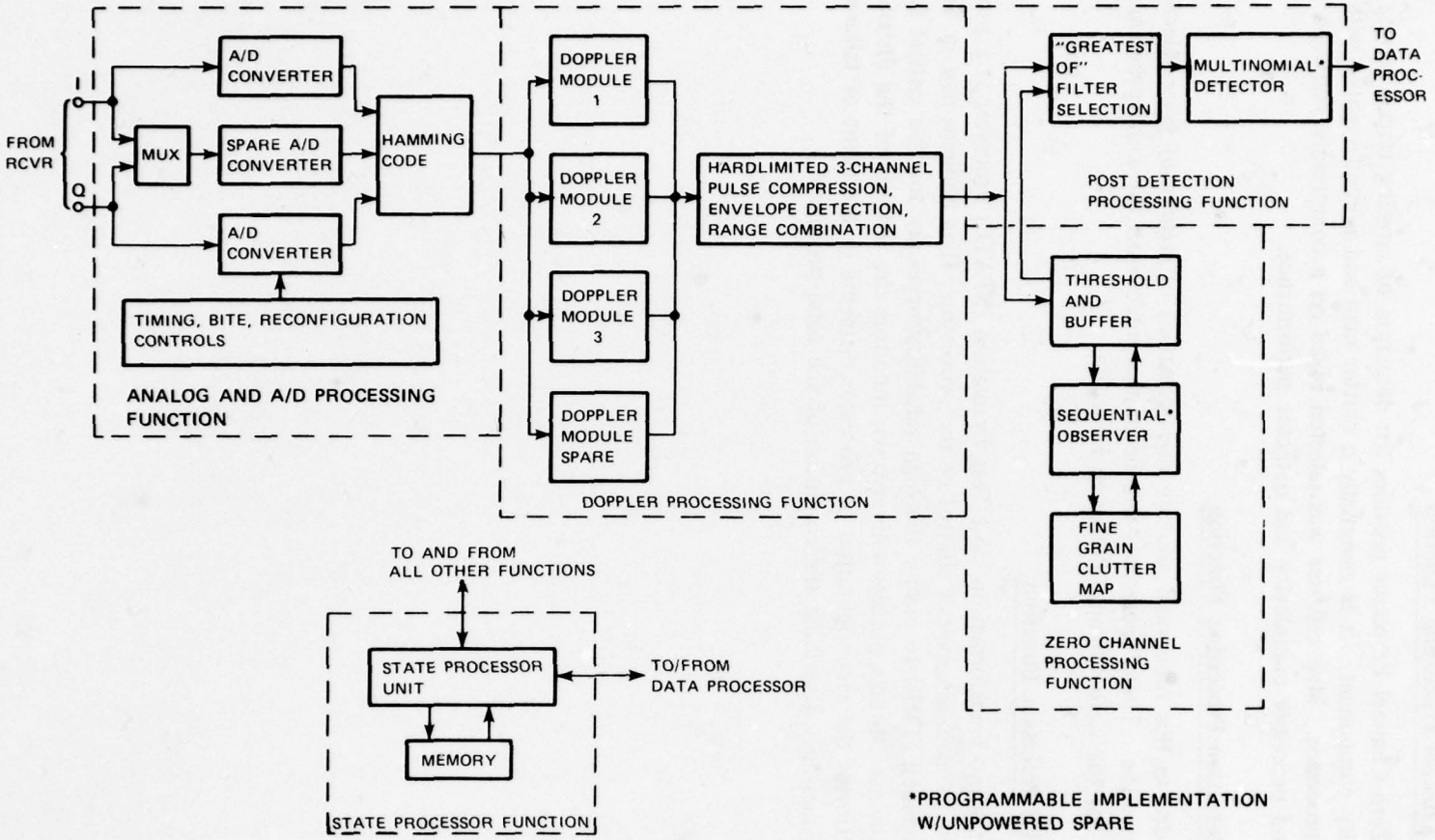
Multinomial Postdetection Integration (4 pulses)

Distributed BITE with STATE Monitor and Controller

TABLE 1-VI. A SUMMARY LIST OF THE MAJOR PARAMETERS OF THE OPTIMUM PROCESSOR

Range Coverage	5–60 nmi
Range Resolution	0.1 nmi
Input Data Rate	1.62 MHz (Each I&Q)
Land Clutter Improvement Factor	50.9 dB
Reliability	44.78 f/10^6 hours → 22,331 MTBF
Power Consumption	226 watts
Processing Losses (Excluding 9.0 dB Integration Gain)	8.85 dB
Number of Boards	10

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Figure 1-1. Overall Block Diagram of the SPUR *which defines the five selected processing functions and operations performed in each*

1.3.3 Zero Channel Processing Function

The Zero Channel Processor provides for detection of crossing targets having little or no radial velocity component. It is essentially a clutter map and is implemented with a programmable processor. Map cell size was selected based on a compromise between memory requirements and processor complexity and detector performance.

1.3.4 Postdetection Processing Function

Included in this functional area are the operations of ***greatest-of*** filter selection and multinomial detection. These operations will be implemented with the same programmable processor used for the Zero Channel Processor Function.

1.3.5 STATE Processor Function

The Status, Transformation, and Test Evaluation (STATE) Processor is a programmable unit used to maintain overall control of the processor. It is implemented in Triple Modular Redundancy (TMR) to ensure the high reliability necessary for this critical function. The STATE Processor directs processor level tests, monitors the outputs of the distributed BITE units, performs the reconfiguration of processor elements in the event of failures, and provides status messages describing the condition of the total processor.

Section 2

PROCESSOR FUNCTIONAL REQUIREMENTS

The specified SPUR parameters, discussed in Section 1.1 of this report, provide the top-level requirements for the SPUR processor. To facilitate the tradeoffs and analysis required in determining the optimum design, the processor was divided into five functional areas. These are identified in the block diagram of Figure 2-1.

The functional breakout is sufficiently general to permit optimization of the individual functions and, at the same time, is specific enough to support identification and design of the processor units within each function. Moreover, this functional breakout simplifies establishment of interface requirements and memory allocations.

In this section we discuss the impact of the various SPUR requirements on the processor functions identified above. First, we provide a summary of the major performance requirements and specific effects of each on the different functions. Then, we give a brief discussion of the implications of the very high reliability requirement and our reliability enhancement design for meeting this requirement.

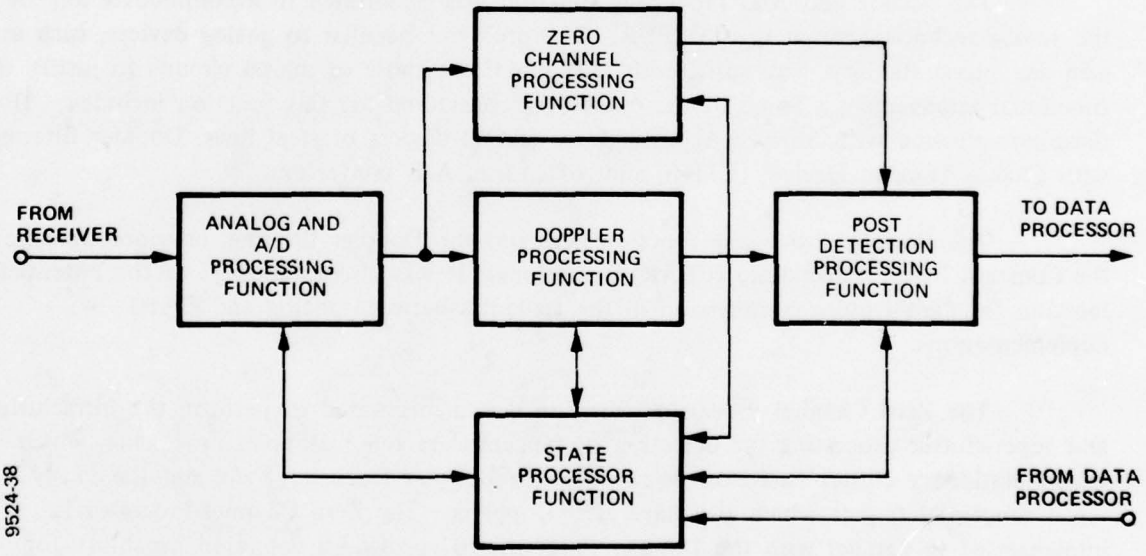


Figure 2-1. The SPUR is Organized into Five Generic Processor Functions

2.1 PERFORMANCE REQUIREMENTS

As shown in the block diagram of Figure 2-1, five functional areas were established for the SPUR. These are the Analog and A/D Processing Function; Doppler Processing Function; Zero Channel Processing Function; Postdetection Processing Function; and the Status, Transformation, and Test Evaluation (STATE) Processor Function.

The STATE Processor is the basic SPUR controller and monitoring unit. It continuously polls the distributed BITE associated with the various units. It also generates and detects higher level BITE signals to test for failures between units which may not be covered by the local BITE. In the event of a failure, the STATE Processor is responsible for directing the recovery of the SPUR through reconfiguration of redundant units.

The STATE Processor is an important element in the SPUR and is essential in obtaining the reliability needed to support unattended operation. Section 6.3 of this report describes the STATE Processor in some detail. In evaluating the impact of the SPUR requirements on the STATE Processor, however, it was determined that the specific values of the different parameters had little effect on the STATE Processor design. (This does not apply to the reliability requirement, of course, which is the main reason the STATE Processor is used.) As a result, our discussion in this section of the specific requirements and their effects on the SPUR will center on the remaining four functional areas.

The Analog and A/D Processing function was established to accommodate any of the analog technology used in the SPUR. The problems peculiar to analog devices, such as gain and phase stability, are sufficiently different from those of digital circuits to justify this functional arrangement. Some of the operations considered for this function included: IF pulse compression with Surface Acoustic Wave (SAW) devices or steel lines, Doppler filtering with Charge Transfer Devices (CTDs), and, of course, A/D conversion.

The Doppler Processing function performs the Doppler filtering, envelope detection, the Constant False Alarm Rate (CFAR) operations. It was also established as the potential location for digital pulse compression in the tradeoffs between analog and digital implementations.

The Zero Channel Processing function was incorporated to perform the intraclutter and super-clutter processing for detection of tangential targets. Doppler processing, which rejects stationary clutter based on its zero or low Doppler frequency, will simultaneously reject tangential targets which also have zero Dopplers. The Zero Channel Processor is implemented in parallel with the Doppler Processor to provide a detection capability for these targets. Essentially it is a clutter map that detects scan-to-scan variations in the signal levels in each radar cell.

The Postdetection Processing function performs the ***greatest-of*** filter selection and postdetection integration. The greatest-of operation selects the Doppler channel for each range bin having the largest absolute value. Several approaches were identified for implementing the postdetection integration ranging from binary to full dynamic range integration.

Table 2-I summarizes major effects of the various SPUR requirements on each of these four functional areas. In some of the areas these effects are only qualitatively defined. During the many tradeoffs leading to selection of the optimum processor, quantitative values were developed for the particular implementation evaluated. These are discussed in subsequent sections of this report, especially in Section 6, Description of the Optimum Processor.

2.2 RELIABILITY ENHANCEMENT REQUIREMENTS

A key requirement for modern radar systems is high operational availability; i.e., combination of an acceptable reliability, specified in terms of mean-time-between-failure (MTBF); and good maintainability, specified in terms of mean-time-to-repair (MTTR). In particular, operational availability, A_0, is defined as

$$A_0 = \frac{MTBF}{MTBF + MTTR} = \frac{1}{1 + MTTR/MTBF}$$

where MTTR includes preventive maintenance downtime. The availability is, therefore, high when the failure rate is low (which implies a high MTBF) and the repair time is short.

In an unattended radar, however, the high availability requirement translates directly into a high reliability requirement because maintenance technicians are not at the site to quickly return a system to normal operation. This does not imply, however, that the SPUR maintainability requirements in terms of MTTR are reduced. Due to the great distances involved and the potential for rapid weather changes in the Arctic, it is essential that maintenance technicians be able to repair the radar as quickly as possible.

For the SPUR, the high reliability requirement is specified as an MTBF of 20,000 to 100,000 hours (or, equivalently, the acceptable failure rate range is 10 – 50 failures per million hours). This is an order of magnitude increase over typical modern signal processor MTBF requirements. To achieve this increase in reliability requires consideration of the reliability requirement throughout the development of the processor.

Given the complexity of the processing task, the SPUR reliability requirements cannot be met with a totally serial design (i.e., no redundancies employed). This conclusion is arrived at using initial parts count estimates and calculating the failure rates of typical parts considered for the SPUR. Calculations of the failure rates are based on standard MIL-HDBK-217B procedures using the formula and parameter values shown in Table 2-II for semiconductor devices. Quality factors for three classes of devices are indicated. Class S devices (the highest reliability class designated) are not available, and the quantity requirements

TABLE 2-I. EFFECTS OF THE SPUR REQUIREMENTS ON VARIOUS PROCESSOR FUNCTIONS

Requirement	General	Effects: Analog and A/D Processor	Effects: Doppler Processor	Effects: Zero Channel Processor	Effects: Postdetection Processor
Range 5–60 nmi	800 μsec Min PRI (w/40 μsec Transmitter Pulse)	800 μsec Min Delay for PRTs 1100 I, 1100 Q Samples/Sweep	550 Range Bins/Sweep, 2200 Storage Cells/Sweep	550 Clutter Cells/Coherent Batch Max	550 Postdetection Processes/ Coherent Batch
Range Resolution 0.1 nmi	1.23 μsec Range Bin	810 kHz Video Bandwidth Double Sampling Requires 1.6 MHz Rate			
Pulse Compression Ratio 32:1	Transmitter Pulse ≅ 40 μsec Selection of Type	Potential Position for Pulse Compression Sample Twice per Compressed Pulsewidth	Potential Position for Pulse Compression	Increased Dynamic Range on Point Clutter	–
Land Clutter Improvement Factor >50 dB	Other Clutter Also Considered	Dynamic Range >50 dB No. of Bits ⩾10	Selection of Process. Dynamic Range. Operation Against Model	Wide Dynamic Range Clutter	–
FFT 8-Pulse	Coherent Baseband Process	–	Coherent Batch of 8 Pulses Min Allows ~10 μsec Processing Time/Range Bin	Processing Time per Batch is 6.4 msec Min for all Cells	Processing Time per Batch is 25.6 msec Min for all Cells
MTI	Only in Conjunction w/Coherent Process Increases No. of Pulses per Coherent Batch	Possible Location	Possible Location	Increases Batch Time Available for Processing	Increases Batch Time Available for Processing

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TABLE 2-I. EFFECTS OF THE SPUR REQUIREMENTS ON VARIOUS PROCESSOR FUNCTIONS (Continued)

Requirement	General	Effects: Analog and A/D Processor	Effects: Doppler Processor	Effects: Zero Channel Processor	Effects: Postdetection Processor
CFAR 32-Cell	Selection of Type	–	Location of CFAR	–	"Greatest Of" Selects Largest
Clutter Map – Zero Velocity Super Clutter/ Intraclutter Detection Processing	–	–	–	Size of Cell, Memory Size. Algorithm. Location of Pulse Compression	Matching to Greatest of Process
Post Detection Integration = 4 Pulses	32 Hits/Beamwidth Min	–	Four Coherent Batches per Beamwidth	Minimum Azimuth Cell is BW/4	Selection of Type Memory/ Dynamic Range
Prf's 2 Available	Affects Velocity Response	–	–	–	Destagger Required
Environmental	MIL-SPEC Components	Calibration Loops Ovens	–	–	–

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TABLE 2-II. CALCULATION OF FAILURE RATES FOR DIGITAL DEVICES *were based on the standard formula with the parameters specified for this SPUR application.*

FORMULA: $\lambda_P = \pi_L \pi_Q (C_1\pi_T + C_2\pi_E) \pi_P$

π_L = Learning Factor: Mature Devices = 1.0

π_Q = Quality Factor: Class S = 1.0, Class B = 2.0, Class B-1 = 5.0 (See text)

C_1, C_2 = Circuit complexity factors (function of no. of gates)

π_T = Temperature factor based on T_a = 49°C + 11°C (rise) = 60°C

π_E = Environment Factor: Fixed ground = 1.0

π_P = Pin Factor: (for SSI/MSI devices)

No. of Pins	π_P
<24	1.0
24 to 40	1.1
42 to 64	1.2
>64	1.3

of the SPUR are not likely to generate sufficient interest within industry for qualification of these devices. Thus, for SPUR, only level B qualified devices and manufacturer tested devices to level B, class B-1, are considered. As can be seen in the table, these devices have a reliability factor difference of 2.5, while the cost varies from 1.5:1 to 4:1. For the SPUR, class B parts are recommended.

The failure rates of typical devices are shown in Table 2-III. The serial reliability model assumes that failure rates are constant and failures occur independently. Under these assumptions the reliability is given by the exponential probability distribution

$$R = e^{-\lambda t}$$

where λ is the device failure rate (or 1/MTBF) normally expressed in failures/10^6, and t is time. The constant failure rate assumption is reasonable when the system has eliminated early failures (through screening or burn-in) and does not have components approaching wearout. Operation is then in the flat central position of the classic reliability curve.

Reliability of the series connection of N components is given by the product of the reliability of the components, viz.

$$R_T = \prod_{i=1}^{N} R_i$$

TABLE 2-III. FAILURE RATES FOR TYPICAL DEVICES USED IN THE SPUR were calculated based on standard techniques.

Device	λ (f/10^6)
Multiplier – Accumulator (12 x 12)	2.87
8-bit A/D Converter (LSI)	15.84
6-bit A/D Converter (LSI)	0.61
AM 2901A	0.27
4K MOS RAM	1.348
16K MOS RAM	3.468
Typical bipolar SSI/MSI (39 gates)	0.058
Typical CMOS SSI/MSI (39 gates)	0.165

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This implies that the failure rate of the series connection is simply the sum of the individual failure rates,

$$\lambda_T = \sum_{i=1}^{N} \lambda_i$$

Thus, from Table 2-II, we see, for example, that the use of more than 13 Class B (or 5 Class B-1) 16K memory chips will result in a total failure rate greater than the maximum allowed value of 50 f/10^6 hours. Since the Zero Channel Processor alone exceeds these memory requirements, it is obvious that a totally serial architecture will not suffice for the SPUR.

With the incorporation of redundancy, the calculation of system MTBF (or equivalently λ_T) becomes more involved, and it must be treated as a time dependent quantity. For the purposes of the SPUR, the MTBFs are calculated on the basis of 1-month and 3-month maintenance intervals, at which time the system is completely restored, including all failed redundancies. Thus when the system is configured to meet 20,000 hours MTBF based on a 3-month interval, it has a probability of 89.6 percent of operating for three months without a system-relevant failure, while it has a probability of 97.3 percent of operating for one month. The corresponding probability of success versus other MTBFs is shown in Table 2-IV.

The key to obtaining high system reliability is to design it into the system from the beginning. At the module level, this type of design should use the minimum number of parts at the proper stress levels and, in general, should favor the use of LSI and other more highly integrated devices over many simple functions. At the system level, the key method for designed-in reliability is the proper partitioning of the system into blocks based on failure rate, function, and potential for protection by redundancy. This partitioning is accomplished as the system architecture is developed. After the system is partitioned, selective redundancies are added, based on benefit-versus-cost calculations, until the processor meets or exceeds the reliability requirements.

TABLE 2-IV. RELIABILITY FOR THE SYSTEM tabulated versus MTBF and operating time

MTBF	3-Month Reliability	1-Month Reliability
20,000	89.6%	96.4%
40,000	94.7%	98.2%
60,000	96.4%	98.8%
80,000	97.3%	99.1%
100,000	97.8%	99.3%

To facilitate optimization of the processor reliability, the processor is partitioned into a serial connection of independent blocks. This arrangement and the assumption of independence, which is reasonable for a properly partitioned system, permits use of the equations above in computing the total system reliability and corresponding failure rate. In this case, however, redundancy is employed in each of the blocks to reduce its failure rate. As a result, the individual λ_i's and the corresponding total failure rate are functions of the maintenance interval.

Reliability calculation for each of the blocks depends upon the type of redundancy implemented within the block. A general equation has been formulated for calculation of the reliability of the blocks considering imperfect switches, warm standbys, and all types of redundancy [1]. However, for the preliminary SPUR reliability estimates, cold standbys (when appropriate) and m/n hot processors have been assumed. The resulting equations are given in Figure 2-2. Thus these reliability estimation calculations assume that coverage is perfect (i.e., if a fault occurs, it is detected, isolated, and cleared when redundant units are available). This is a strong assumption and its validity depends heavily on the design of the BITE and STATE processor. However, for the sizing study it is a reasonable starting condition. During the Phase II Validation Program, these factors will strongly affect the design activities, and reliability calculations will be modified as the design matures.

[1] Mathur, F.P. and deSousa, P.T., "Reliability Modeling and Analysis of General Modular Redundant Systems," IEEE Transactions on Reliability, Vol R-24, 5, Dec 1975.

COLD STANDBYS:

$$R(N, N, L) = R_0^N \sum_{i=0}^{L} \frac{(N\lambda T)^i}{i!}$$

M/N PROCESSOR (HOT STANDBYS OR PARALLEL PROCESSES):

$$R(M, N, O) = \sum_{j=M}^{N} (-1)^j \binom{N}{j} \left[\sum_{i=M}^{j} (-1)^i \binom{j}{i} \right] R_0^j$$

$$= \sum_{j=m}^{N} \binom{N}{j} R_0^j (1-R_0)^{N-j}$$

WHERE

$R(M, N, L)$ = RELIABILITY OF MODULAR BLOCK
M = NO. OF UNITS REQUIRED
N = NO. OF UNITS ONLINE
L = NO. OF COLD STANDBYS.

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Figure 2-2. Simplified Reliability Equations, Based on a General Modularly Redundant Reliability Equation, were used for the SPUR Reliability Estimates.

Section 3

SYSTEM AND CLUTTER ANALYSIS

For the SPUR study, appropriate analyses were performed to ensure that the optimum processor would meet the performance requirements. Specific areas covered by this analysis, discussed in the following sections, begin with definition of the clutter models and conclude with several special interest topics.

3.1 CLUTTER PROCESSING ENVIRONMENT

The radar operates in a severe arctic clutter environment. The assumed clutter model is shown in Table 3-I. The clutter specifications affect both the processor functional design and performance evaluation.

A log-normal distribution of land clutter reflectivity is assumed. This is consistent with the 2-valued (mean and 84th percentile) data showr.. The log-normal statistics together with the high reflectivity characteristic of ground clutter result in a requirement for large dynamic range signal processing.

Sea clutter has lower intensity and is normally significant only at shorter ranges. Sea clutter intensity diminishes rapidly at ranges approaching the radar horizon. This is due to the sharp fall-off in reflectivity which occurs as the grazing angle goes to zero at the horizon. Of the data provided, the worst case corresponds to a grazing angle of 1 degree. For a radar sited 3500 feet above mean sea level, this occurs at a range of 28.1 nmi. Rayleigh amplitude statistics are assumed. This statistical model applies when the size of the radar range resolution cell is large compared to the water wavelength. For SPUR, the wavelength criterion is fully satisfied.

Weather clutter has a broad spectrum with substantial values of mean velocity. With a 30K-ft rain ceiling and a wind shear of 80 knots in 50K feet, a spectral width of as much as 24m/sec is obtainable. This is reduced somewhat when the effects of radar siting, earth curvature, and antenna pattern are included. Performance is calculated for various offsets of weather clutter including the worst case.

The simultaneous presence of ground clutter with weather or sea clutter produces a bimodal spectrum. The achievement of high performance in such spectra is a design goal of the optimum SPUR.

Regulation of false alarms is of vital importance in the UAR. Radar target reporting is fully automated and high performance CFAR is necessary to prevent loss of radar function due to overload of the data processor and/or narrowband data link. The CFAR must also have high efficiency since losses in the signal processing contribute directly to overall radar power demand. The definition of clutter statistics provides a basis for optimization of the CFAR function.

TABLE 3-I. QUANTIFIED DETAILS OF LAND, SEA, AND WEATHER CLUTTER FOR THE SPUR

Land Clutter		
Amplitude Distribution	Log – Normal	
Reflectivity		
Median	-34 dB m^2/m^2	
84th Percentile	-24 dB m^2/m^2	
Spectrum (Gaussian)		
Standard Deviation (30-knot wind)	0.2 m/sec	
Sea Clutter (Sea State 4)		
Amplitude Distribution	Rayleigh	
Reflectivity vs Grazing Angle and Polarization		
Grazing Angle	H	V
1.0 degree	-52	-45 dB m^2/m^2
3	-48	-38
10	-45	-31
Spectrum (Gaussian)		
Mean Velocity	2.5	1.3 m/sec
Standard Deviation	0.9	0.9 m/sec
Weather Clutter (15 mm/hr Rain)		
Cell Diameter	5 nmi	
Ceiling	30K ft	
Radial Velocity	0 to 80 knots	
Shear	See Note	
Amplitude Distribution	Rayleigh	
Reflectivity	-88 dB m^2/m^3	

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Note: The wind shear is 0 to 80 knots from 0 to 50K feet with any arbitrary shear distribution over this altitude range.

3.2 DEVELOPMENT OF CLUTTER SPECTRAL MODELS

In order to evaluate the performance of candidate filter banks against clutter, spectral models for the three types of clutter were developed. The c/n ratios are based on the clutter model shown in Table 3-I (for estimating clutter cross sections) and an estimate of radar system front-end noise. The spectral spread and offsets were determined as described in Section 3.1. The resulting spectra for ground, rain, and sea clutter are shown in Figures 3-1, 3-2, and 3-3 respectively. In all cases, the prf is the reciprocal of the average of two slightly different pulse intervals that are alternated from group to group for improved velocity response. Also, in all cases, the system noise is white and has a relative spectral density of zero dB.

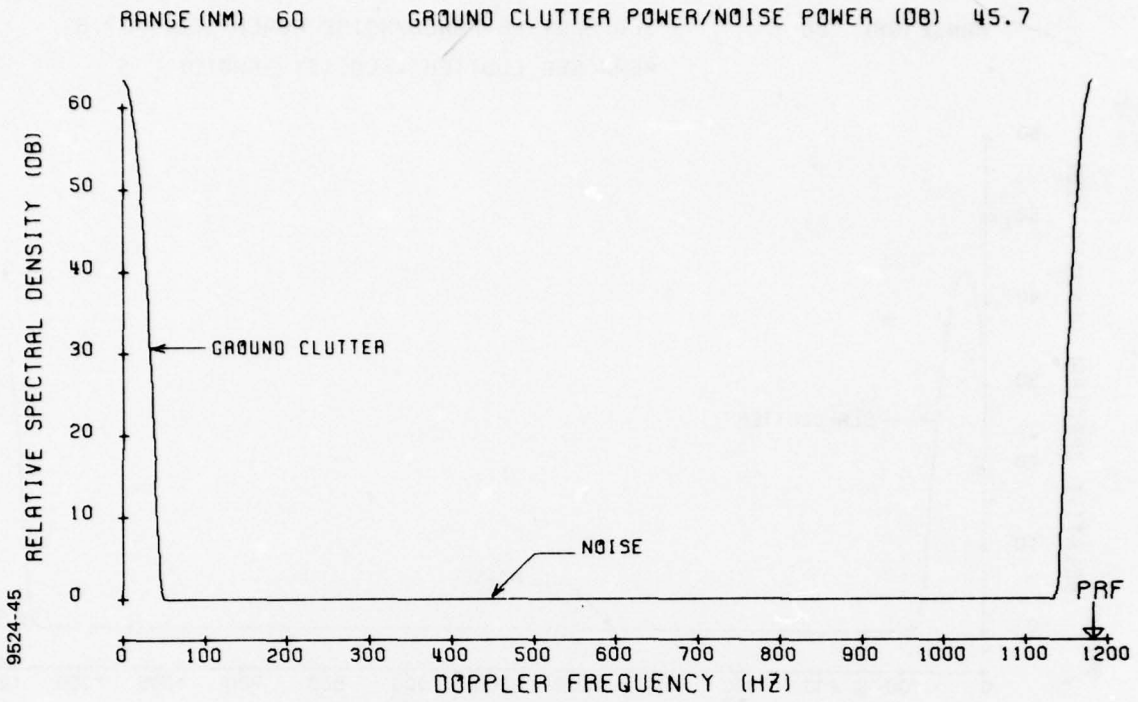


Figure 3-1. The Spectra of Ground Clutter from 60 nmi and System Noise are shown at the filter bank input

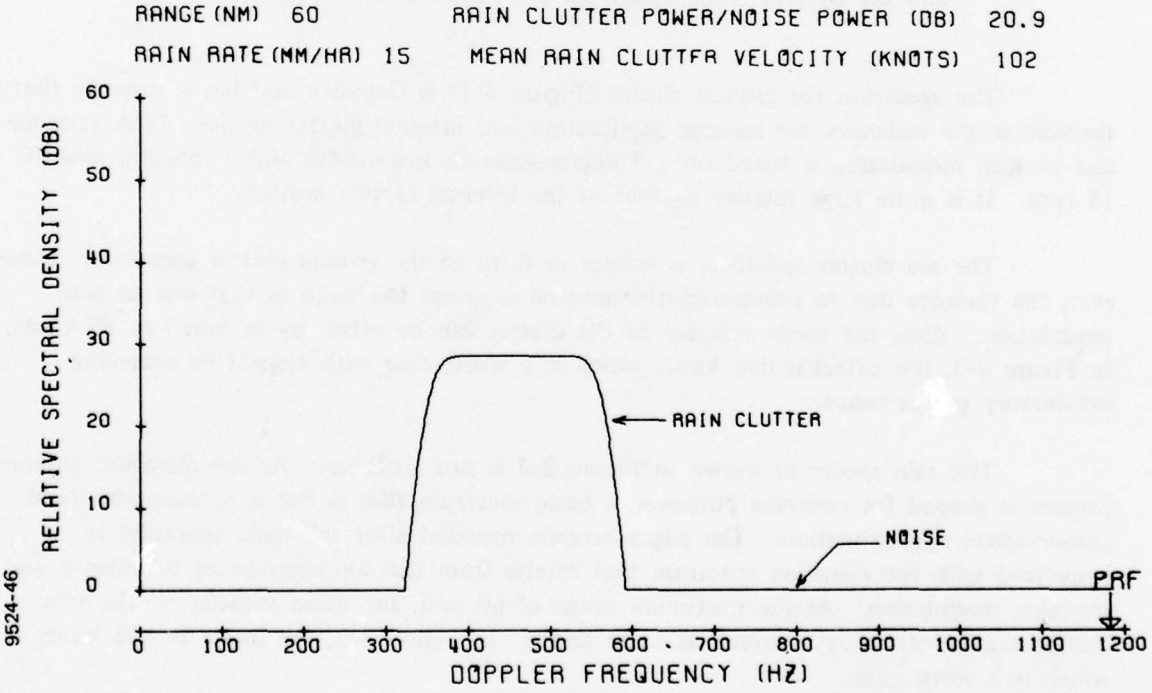


Figure 3-2. The Spectrum of Rain Clutter from 60 nmi having the Maximum Mean Velocity and the System Noise Spectrum are shown at the filter bank input

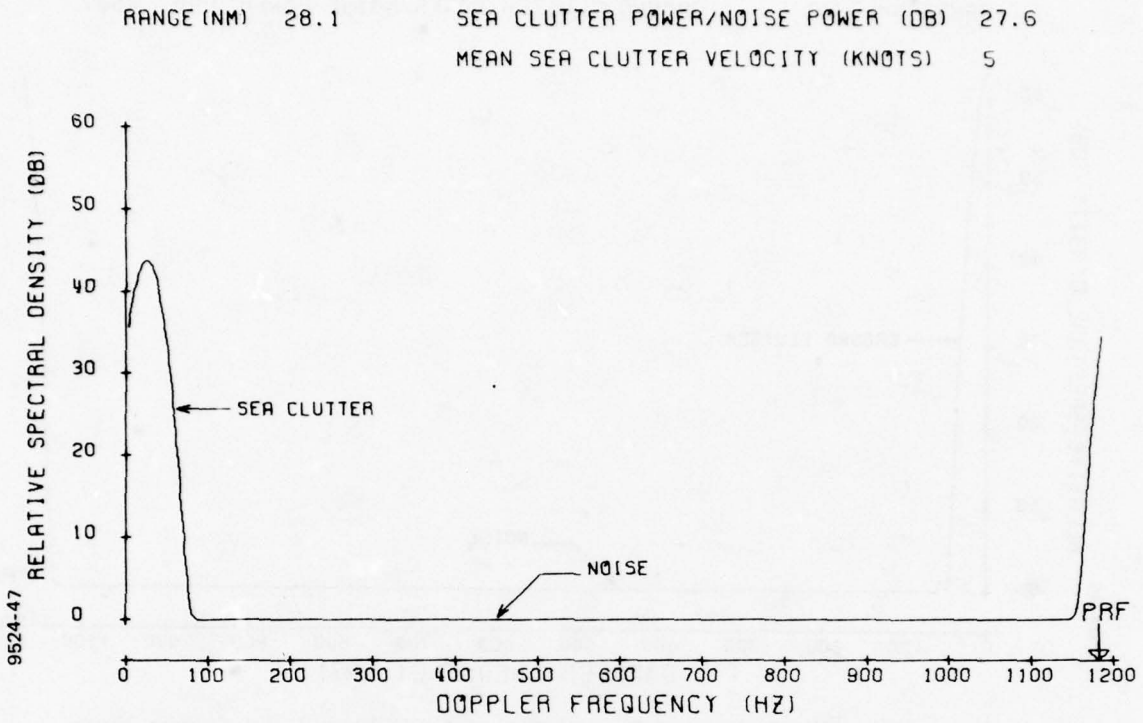


***Figure 3-3. The Spectrum of Sea Clutter from 28.1 nmi having the Maximum Mean Velocity and the System Noise Spectrum** are shown at the filter bank input*

The spectrum for ground clutter (Figure 3-1) is Gaussian and has a variance that is the sum of the variances due to scan modulation and internal clutter motion. The variance due to scan modulation is based on a 3 degree-azimuth beamwidth and a rotation rate of 15 rpm. It is quite large relative to that of the internal clutter motion.

The sea clutter spectrum is similar in form to the ground clutter spectrum. However, the variance due to internal clutter motion is about the same as that due to scan modulation. Also, the mean velocity of the clutter can be offset by as much as ±5 knots. In Figure 3-3, the offset is five knots which is a worst case with respect to achieving satisfactory performance.

The rain spectrum shown in Figure 3-2 is not Gaussian. As the elevation antenna pattern is shaped for coverage purposes, a basic spectrum that is flat is a reasonable (and conservative) approximation. The edges become rounded after the basic spectrum is convolved with the Gaussian spectrum that results from the combination of turbulence and scanning modulation. At the maximum range of 60 nmi, the mean velocity of the rain clutter can be offset by as much as ±102 knots. In Figure 3-2, the offset is 102 knots which is a worst case.

3.3 SELECTION OF CLUTTER FILTERS FOR SPUR

The SPUR is required to have an improvement factor against ground clutter that exceeds 50 dB. In addition, good performance should be attained in a ground clutter plus rain clutter environment where the mean Doppler shift of the rain clutter can be a significant fraction of the prf. The general clutter filter configuration most suitable for these requirements is based on a bank of narrowband filters. The individual filters are operated on a coherent batch basis and may be classified as being all-zero, FIR (finite impulse response), nonrecursive, or transversal. The number of samples (pulses) in the batch is a major factor in determining how well the filters can discriminate signals from a background spectrum of clutter and noise. It has been determined that an eight-pulse batch is suitable for SPUR. (An additional fill pulse is transmitted to accommodate second-time-around echoes as discussed in Section 3.7.)

For a single channel clutter filter such as a canceler, the improvement, due to clutter filtering at a particular signal frequency, can be defined as the ratio of the output signal-to-clutter-plus-noise ratio to the input signal-to-clutter-plus-noise ratio. The improvement factor is given by averaging the improvement over all signal frequencies. This definition of improvement factor can be extended to multiple channel clutter filters such as the narrowband filter banks being studied here. As any particular signal frequency is applied to all filters, the improvement due to each filter can be separately determined. When the filter outputs are properly normalized with respect to their residues of clutter-plus-noise and combined on a ***greatest-of*** basis, the average detection statistics are determined by the filter giving the greatest improvement at that particular signal frequency. The AGI (Average Greatest Improvement) is obtained by averaging the greatest improvement over all signal frequencies. For example, the AGIs of the SPUR filter bank in ground and sea clutter environments are shown in Figures 3-4 and 3-5. AGI is equivalent to the improvement factor of a single channel clutter filter.

The specific filter bank configurations that have been evaluated are:

a) Optimum filter bank,
b) Near-Optimum Filter (NOF) bank,
c) 8-Point FFT with optimum weights,
d) 2-Pulse Canceler followed by 8-Point FFT with optimum weights.

The optimum filter bank provides the best possible clutter filtering performance under conditions that are completely known. Although this requirement is too restrictive for the SPUR, the optimum filter bank provides a performance reference that is useful in evaluating other filter banks. Also optimum filter banks provide a basis for deriving near-optimum filter banks which are practical candidates for the SPUR.

For a given set of conditions, the weights of a transversal clutter filter can be optimized such that the improvement in the output signal-to-clutter-plus-noise ratio relative to the input signal-to-clutter-plus-noise ratio is maximized. ITTG has developed computer programs that automatically derive such optimum filters. The input data required include: the batch size (number of pulses), time between pulses (or prf), spectrum of the input

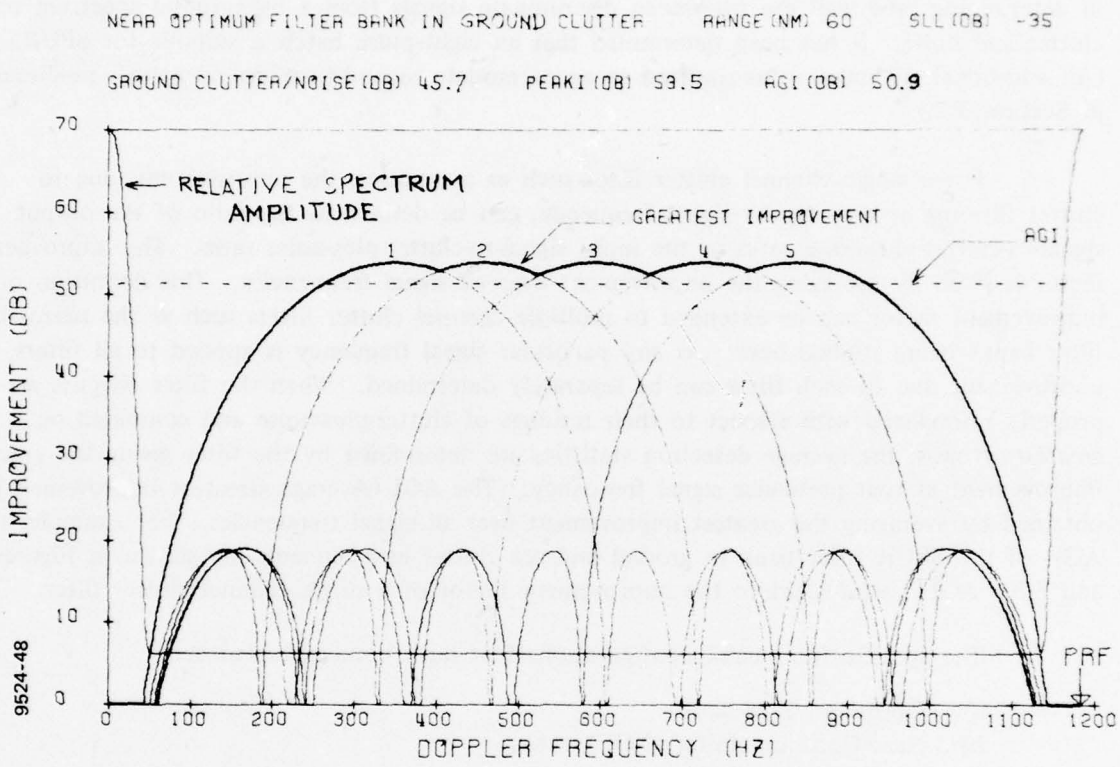


Figure 3-4. The Envelope of Improvements due to Each Filter in the Bank *used to calculate the AGI in ground clutter*

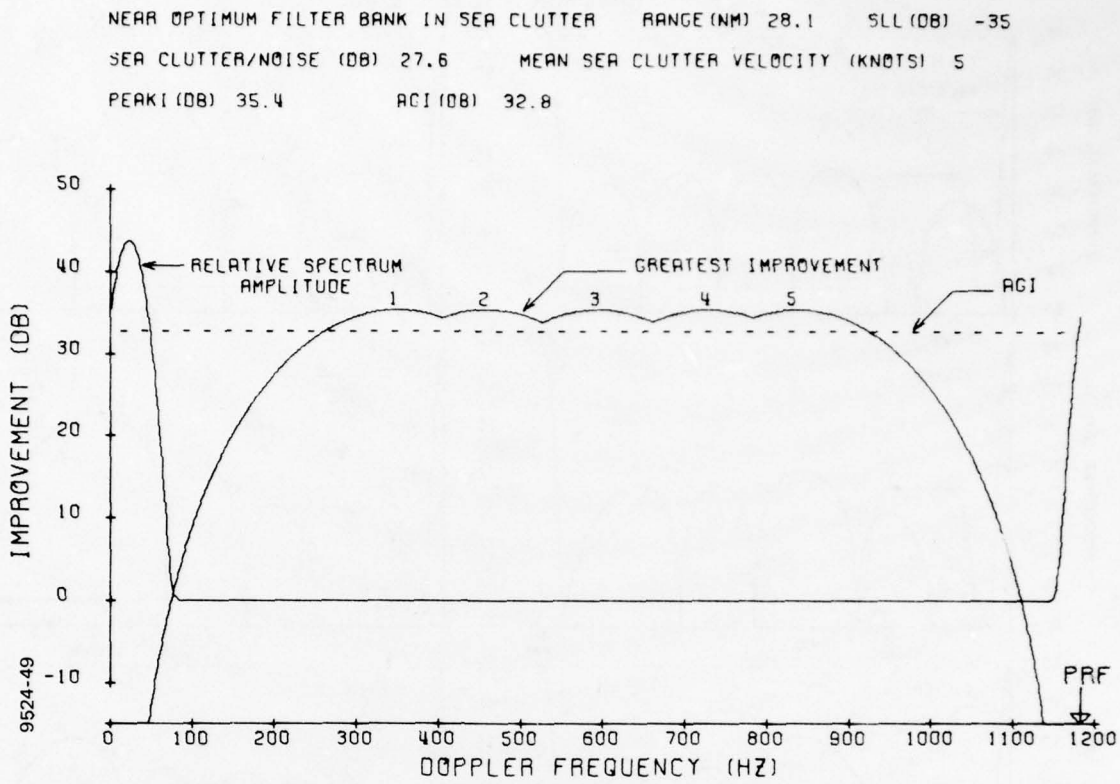


Figure 3-5. The Envelopes of Improvements due to each Filter in the Bank used to calculate the AGI in sea clutter having maximum mean velocity

clutter-plus-noise, and the signal frequency. The optimization approach used is sometimes described as a hill-climbing technique. The transmission zeros of the filter are always of unit magnitude and initially have equally spaced angles. The angles are first sequentially increased or decreased by a fixed amount until the improvement is maximized under those conditions. The size of the step is then halved and the process repeated until the improvement is further maximized. This entire process is repeated until the step size has been reduced to 0.5 degree. It has been determined that step sizes smaller than 0.5 degree result in negligible improvement gains. A representative input spectrum includes a combination of ground clutter, rain clutter, and noise. The ground clutter power exceeds the rain clutter power and both exceed the noise power. The rain clutter spectrum has a mean frequency that can occur within a range that is quite large relative to the prf. For a particular input spectrum, optimum filters can be derived for every signal frequency and the corresponding maximum improvement can be determined. The average of such improvements over all signal frequencies is the AGI of a filter bank having as many optimum filters as there are signal frequencies. In practice, it is found that filters optimized at signal frequencies that are multiples of prf/8, form a filter bank that provides a suitable basis for comparison with 8-point FFT filter banks and other similar configurations. An example is shown in Figure 3-6. The input clutter spectrum is

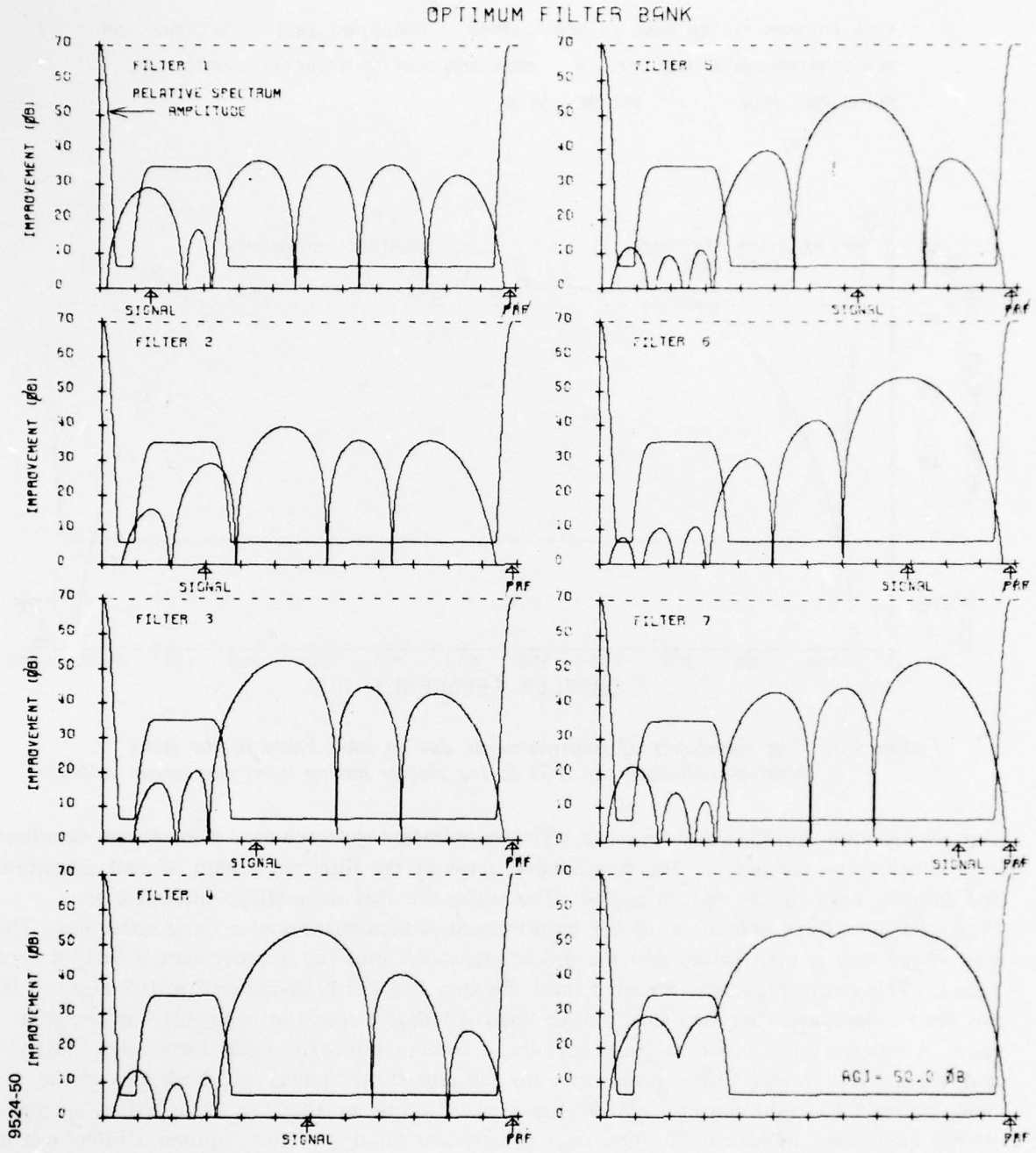


Figure 3-6. Individual and Composite Improvements for Filters Optimized at Signals separated by prf/8. The clutter spectrum is bimodal.

bimodal. The rain clutter spectrum has a positive mean frequency that is substantial. Seven filters have been derived that are optimum at signal frequencies which are multiples of prf/8. For each filter, the improvement obtainable at all signal frequencies is shown. This includes the signal frequencies at which the particular filters were optimized. Filters 1 and 2 are good examples of filters that provide maximum improvement at the signal frequencies used as a basis for optimization while providing greater improvements at certain other signal frequencies. However, these greater improvements do not appear in the envelope of greatest improvements because even greater improvements are provided by filters 3 through 7. It is estimated that the AGI of 50 dB is within two dB of the maximum AGI that would be provided by any number of optimum filters.

The near-optimum filter (NOF) bank is derived from a set of optimum filter banks generated in those clutter environments that require the highest performance. For the SPUR, this corresponds to operating in both ground and rain clutter at 60 nmi. Optimum filter banks were developed that cover the full range of variations in the mean frequency of the rain clutter spectrum. They were then used to determine the fixed number and fixed locations of those transmission zeros that represent the best compromise for the suppression contiguous subbands between zero frequency and the prf. These zeros were also placed such that the sidelobes of each filter are down by the same fixed amount. The frequency responses of the sidelobes of each filter are down by the same fixed amount. The frequency responses of the individual filters in a typical NOF bank are shown in Figure 3-7. Although not shown, an additional filter is centered around zero Doppler which is switched in when there is no ground clutter. Performance of this NOF bank was also determined under the same conditions used in deriving the optimum filter bank shown in Figure 3-6. The results are shown in Figure 3-8. Although the individual filters provide improvement functions that appear dissimilar, the improvement envelopes are quite similar with AGIs that differ by only 1.2 dB. This particular NOF bank was selected as the candidate for the SPUR. In making the selection, the performances of various NOF banks and optimum filter banks were compared under the same conditions. The results are shown in Table 3-II. Comparisons were weighted in favor of the lesser number of filters and also took into account that a mean rain velocity of zero knots is more likely than 102 knots. With a six-filter bank, a sidelobe level of -35 dB is a good choice. With five filters, sidelobe levels of -35 dB and -40 dB are both good choices. Between five and six filters, the comparison weightings favor five filters. The final selection is a five-filter bank with a sidelobe level of -35 dB.

The other configurations that have been evaluated are the 8-Point FFT with optimum weights and a two-pulse canceler followed by an 8-Point FFT with optimum weights. The results (along with those for the near-optimum filter) are summarized in Table 3-III. Amplitude weights are applied to the FFT according to Dolph-Chebyshev. This minimizes the width of the mainlobe response for a specified constant sidelobe level. The sidelobe level is the main trade parameter that determines performance. As it is decreased, the mainlobe broadens and additional filters respond to ground clutter in the mainlobe. When ground clutter is present, these filters are normally excised. For sidelobe levels as low as -45 dB, five filters remain in the bank. For sidelobe levels lower than -45 dB, only

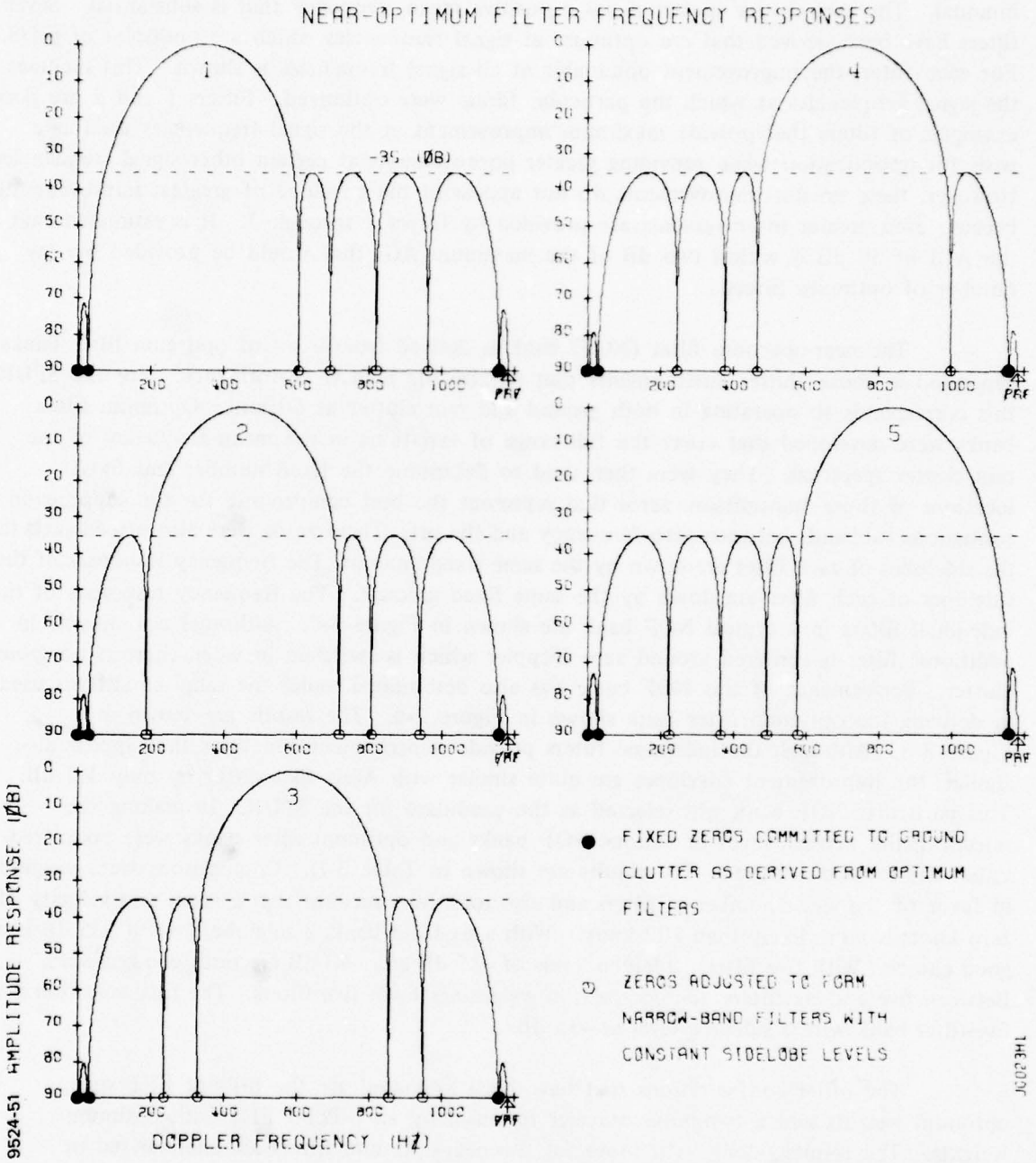


Figure 3-7. Frequency Responses of all Filters in a Typical NOF Bank

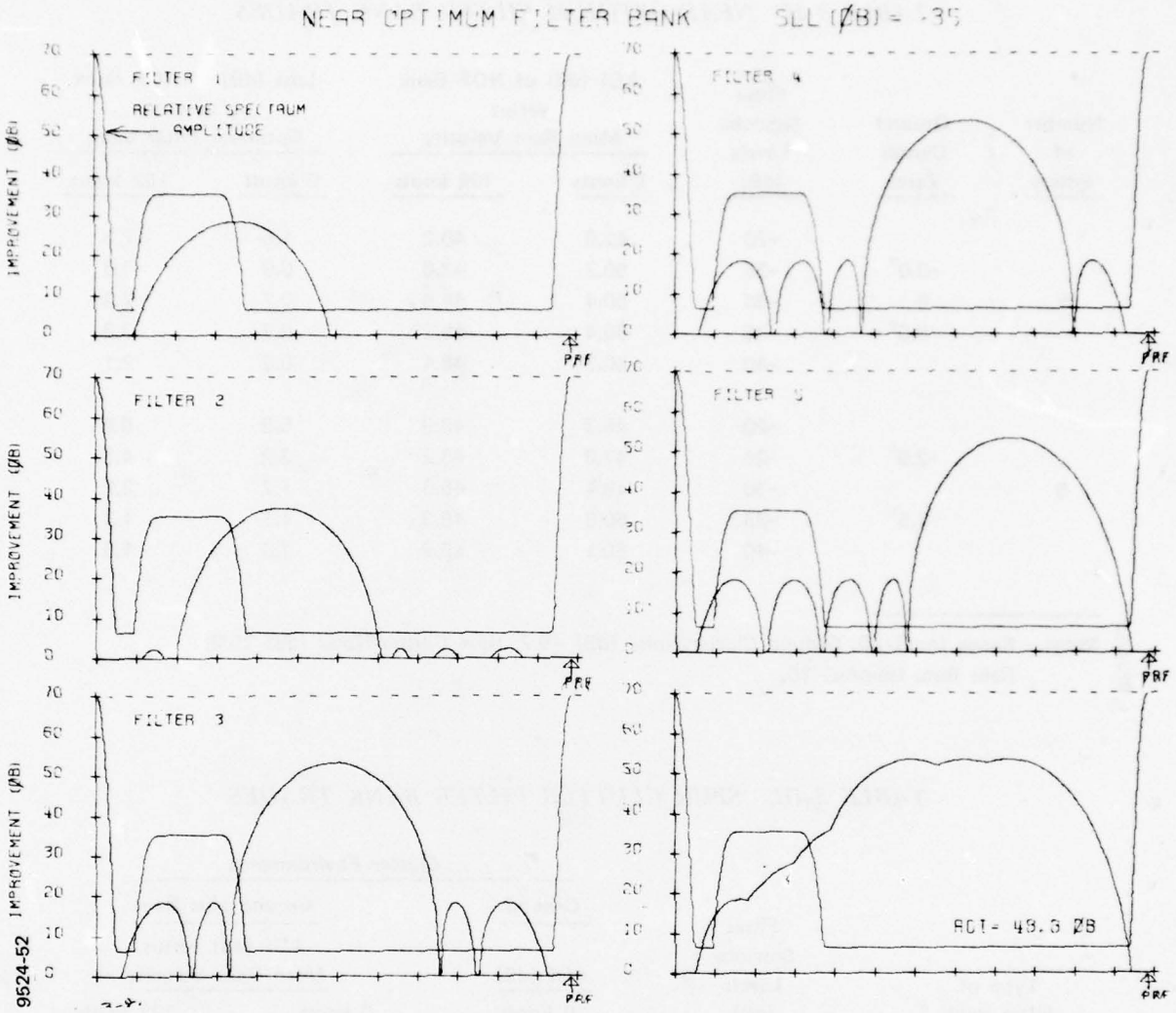


Figure 3-8. Individual and Composite Improvements in Bimodal Clutter for Near-Optimum Filter Bank

TABLE 3-II. NEAR-OPTIMUM FILTER BANK TRADES

Number of Filters	Ground Clutter Zeros	Filter Sidelobe Levels (dB)	AGI (dB) of NOF Bank versus Mean Rain Velocity		Loss (dB) of NOF Bank relative to Optimum Filter Bank	
			0 knots	102 knots	0 knots	102 knots
5	-8.0°	-20	49.6	40.2	1.5	7.3
		-25	50.2	43.6	0.9	3.9
	0	-30	50.4	44.6	0.7	2.9
	8.0°	-35	50.4	45.2	0.7	2.3
		-40	50.3	45.4	0.8	2.1
6	-2.5°	-20	45.3	40.9	5.8	6.6
		-25	47.9	43.2	3.2	4.3
		-30	49.4	45.3	1.7	2.2
	2.5°	-35	50.0	46.3	1.1	1.2
		-40	50.1	45.9	1.0	1.6

9524-53

Notes: Range (nmi) 60; Ground Clutter/Noise (dB) 45.7; Rain Clutter/Noise (dB) 20.9; Rain Rate (mm/hr) 15.

TABLE 3-III. SPUR CLUTTER FILTER BANK TRADES

Type of Filter Bank	Filter Sidelobe Levels (dB)	Clutter Environments		
		Ground	Ground plus Rain	
		AGI (dB)	AGI (dB) versus Mean Rain Velocity	
		0 knots	0 knots	102 knots
Near-Optimum 8-Point FFT	-35	50.9	50.4	45.2
	-40	44.3	43.5	40.8
	-45	46.9	46.2	40.3
	-50	46.9	46.4	35.0
	-55	47.9	47.9	34.0
2-Pulse Canceler plus 8-Point FFT	-20	46.5	46.0	36.9
	-30	47.5	47.0	41.4
	-40	47.2	46.7	42.7
	-45	46.9	46.4	42.8

9524-54

Notes: Range (nmi) 60; Ground Clutter/Noise (dB) 45.7; Rain Clutter Noise (dB) 20.9; Rain Rate (mm/hr) 15.

three filters remain. Under bimodal conditions and with large mean rain velocities, the limited velocity coverage of a three-filter bank is not adequate to maintain good performance. This is shown in Table 3-III for the 8-Point FFT at -50 and -55 sidelobe levels. The sidelobe level selected as best for this configuration is -45 dB. In the final candidate configuration, the FFT is preceded by a two-pulse canceler which suppresses most of the ground clutter. The main function of the FFT is to suppress the rain clutter. In general, higher sidelobe levels are acceptable which allow more filters in the bank. According to the results, a sidelobe level of -30 dB is best and performs somewhat better than the FFT alone. Of the three configurations, the near-optimum filter bank is the only candidate which meets the 50 dB Improvement Factor requirement. It is the recommended Doppler Filtering process for the SPUR.

3.4 PROCESSOR GAINS AND LOSSES

An important part of the design and optimization of a radar signal processor is consideration of the gains and losses attributed to the selected processor functions and the specific algorithms used for implementation. It makes little sense to optimize a processor for low power and high reliability without consideration of the effects on other parts of the system. Without this consideration, the selected system could cause large increases in the requirements of other parts of the system to be able to meet the radar system requirements such as detection range. For example, from the range equation, an additional 3 dB of processor losses could require a doubling of the transmitter power or, at least, a combination of increases in transmitter power and antenna gain and a decrease in receiver noise which totals 3 dB. The calculation and consideration of processor gains and losses for the functions ensures that the SPUR optimization will inherently consider the other parts of an unattended radar system without specifically defining them, thereby achieving a ***real-world*** design.

During system analysis of the SPUR, gains and losses have been calculated for the potential algorithms of the processing functions. Gain is provided in the Doppler filtering because the narrowband filter bank is implemented as a coherent process. Losses are inherent in all other processes. These gains and losses (Table 3-IV) are tabulated for several design alternatives for each function.

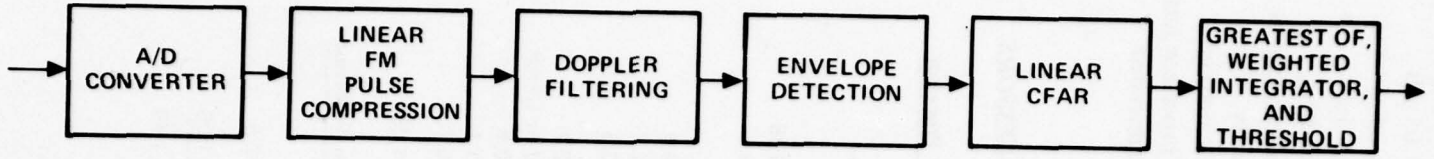
Initial loss considerations led to the definition of two example processor configurations at opposite ends of the implementation spectrum for determination of overall net processor gain. These examples are a fully linear processor (a, Figure 3-9), and a nonlinear processor (b, Figure 3-9). Each processor contains the same functions but employs different implementations:

a) A/D conversion,
b) Pulse compression,
c) Doppler filtering,
d) Envelope detection,
e) Constant False Alarm Rate (CFAR) process,
f) Filter collapsing (greatest-of selection),
g) Postdetection integration,
h) Thresholding.

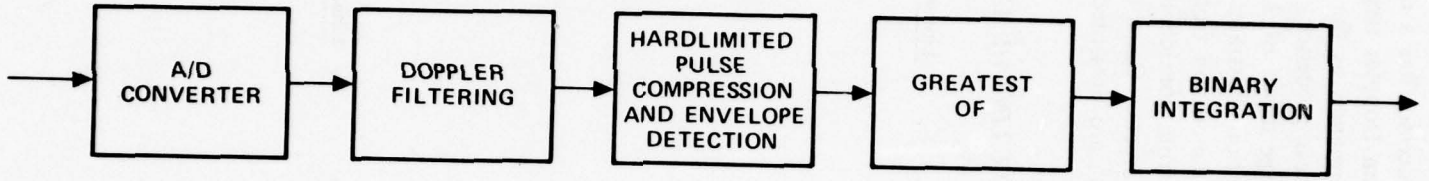
TABLE 3-IV. GAINS AND LOSSES FOR PROCESSING FUNCTIONS

Function	Loss (dB)			Comments
		Mismatch		
Pulse Compression		No Doppler	Maximum Doppler	Max Doppler = 2400 knots
Linear FM (32:1)		1.3	1.4	Hamming Wtg
Nonlinear FM (32:1)		0	1.0	Taylor Wtg
Binary Phase Code (31:1)		0	2.5	
A/D Conversion		Quantization	Range Straddle	
		0.35		rms Noise at LSB
			0.8	Double Sampling
			1.8	Single Sampling
Doppler Filtering	Coherent Gain	Wtg	Filter Straddle	
FFT	(9.0)	1.35	0.7	45 dB Sidelobe
Canceller + FFT	(9.5)	2.5	0.9	Average
Near Optimum Filters	(9.0)	1.2	0.6	35 dB Sidelobes
CFAR		Threshold Estimate		
Linear (32 Cell)		1.3		
Hardlimited Pulse Compression		2.7		Includes Envelope Detection
Envelope Detection		Approximation		
Max [|I|, |Q|] + α min [|I|, |Q|]		0.2		α = ¼
		0.1		α = ½
Filter Collapsing		Greatest Of		
Preintegration		0.5		Six Filters
Post Integration		0.3		Six Filters
Postdetection Integration		Detection		
Binary		1.1		Sliding Window
Multinomial		0.4		Four Levels (2 Bits)
Weighted Integrator		0.35		Full Dynamic Range
Sweep Integrator		2.7		Full Dynamic Range
Threshold Quantization		0.7		

9524-55



a. LINEAR PROCESSOR



b. NONLINEAR PROCESSOR

9524-56

Figure 3-9. Linear and Nonlinear Processor Configurations

The linear processor has a net processing gain of 1.8 dB against a zero Doppler target (a, Table 3-V), while the nonlinear processor has a net processing gain of 1.05 dB under the same conditions. When a maximum Doppler target (at ±2400 knots) is considered, the linear processor retains most of its performance, as the net gain decreases only slightly to 1.7 dB (b, Table 3-V). However, the nonlinear processor, with a single channel of hard limited pulse compression, has a relatively large drop of 2.5 dB. The net processing gain is -1.45 dB (a loss). This performance degradation illustrates the well-known sensitivity of biphase codes to Doppler offset. The key conclusion from these examples is that neither processor should be immediately eliminated from consideration, but the nonlinear processor has marginal performance against high Doppler targets. Gains and losses for the recommended optimum processor, derived from Table 3-IV, are presented in Section 3.5.

TABLE 3-V. GAINS AND LOSSES FOR LINEAR AND NONLINEAR PROCESSORS

a. Zero Doppler Target	Linear Processor	Nonlinear Processor
Pulse Compression Mismatch	-1.3	-0-
A/D Conversion		
Quantization	-0.35	-0.35
Range Straddle	-0.8	-0.8
Doppler Filtering		
Coherent Gain	+9.0	+9.0
Weighting	-1.2	-1.2
Filter Straddle	-0.6	-0.6
CFAR	-1.3	-2.7
Envelope Detection	-0.1	Included in CFAR
Filter Collapsing	-0.5	-0.5
Postdetection Integration	-0.35	-1.1
Threshold Quantization	-0.7	-0.7
Total	+1.8	+1.05

b. Maximum Doppler Target (±2400 knots)	Linear Processor	Nonlinear Processor
Pulse Compression Mismatch	-1.4	-2.5
All Other Gains and Losses	+3.1	+1.05
Total	+1.7	-1.45

9524-57

3.5 OPTIMUM SPUR PERFORMANCE SUMMARY

Performance of the optimum SPUR in the most important single mode clutter environments is shown in Table 3-VI. The ground clutter case can be regarded as a baseline and will be described. The ground clutter cross section at 60 nmi is based on the 84th percentile of the given clutter model, the size of the resolution cell, and an allowance of 0.8 dB for range sidelobe clutter due to pulse compression. The system noise is consistent with achieving a clutter processing improvement in s/(c+n) that exceeds 50 dB and a final s/(c+n) prior to detection (13.7 dB) that includes a 4 dB margin. This margin provides for such things as the detection of fluctuating targets and for some degree of system deterioration. The input ratios shown are all affected differently by the A/D conversion losses. The s/n is reduced by both the quantization noise (0.3 dB) and range straddle (0.8 dB). The c/n is reduced by quantization noise (0.3 dB) alone. The corresponding s/(c+n) is reduced to -48.0 dB. The c/n of 45.7 dB applied to the near-optimum filter bank improves the s/(c+n) by 50.9 dB for a result of 2.9 dB. The pulse compression loss of 3.3 dB combines the 2.7 dB loss due to hardlimited CFAR (which includes the envelope detection loss) and a maximum loss of 0.6 dB due to Doppler mismatch.

The various ratios for the case with rain clutter alone are determined in a similar way. The mean velocity of the rain is maximum which is worst case. The net loss in performance of 5.4 dB is due to the adaptive CFAR suppression of those Doppler filter channels that are responsive to the rain clutter spectrum.

In the clear, the zero Doppler channel is added and the entire filter bank operates against noise alone. The resulting AGI of 6.5 dB includes the coherent gain of the filters and all losses except greatest-of. The net increase in performance of 1.3 dB relative to the ground clutter case is mainly due to the addition of the zero Doppler channel.

The model for sea clutter does not apply reasonably at a range of 60 nmi. However, for an assumed radar height of 3500 feet, the lowest grazing angle for which the model provides data occurs at a range of 28.1 nmi. This range was used to calculate the performance. With a mean velocity of the sea clutter that is maximum (worst case), the performance achieved is significantly better than that required.

In the ground clutter case, the residue after near-optimum filtering is almost entirely due to the system noise. That is, the clutter is almost completely suppressed. The addition of ground clutter to the rain case thus reduces the performance by only about 0.3 dB.

TABLE 3-VI. OPTIMAL SPUR PERFORMANCE SUMMARY FOR VARIOUS CLUTTER ENVIRONMENTS

	Loss	Gain	Note Key	Clutter Environments: Ground $\frac{s}{n}$	Ground $\frac{c}{n}$	Ground $\frac{s}{c+n}$	Rain $\frac{s}{n}$	Rain $\frac{c}{n}$	Rain $\frac{s}{c+n}$	Sea $\frac{s}{n}$	Sea $\frac{c}{n}$	Sea $\frac{s}{c+n}$	Clear $\frac{s}{n}$
			1										
			2	-1.2	46.0	-47.2	-1.2	21.1	-22.4	12.0	27.9	-15.9	-1.2
A/D Conversion	0.3		3										
	0.8		4										
Near-Optimum Filter Bank	(AGI)		5	-2.3	45.7 (50.9)	-48.0	-2.3	20.9 (20.7)	-23.2	10.9	27.6 (32.8)	-16.7	-2.3 (6.5)
Three-Channel Pulse Compressor	3.3	14.9	6			2.9			-2.5			16.1	4.2
						14.5			9.1			27.7	15.8
"Greatest Of" Across Pulse Compressors	0.3					14.2			8.8			27.4	15.5
"Greatest Of" Across Doppler Filters	0.5		7			13.7			8.3			26.9	15.0
Multinomial PDI Over Four Hits													

$P_D = 0.90$ $P_{FA} = 2 \times 10^{-5}$

NOTES:

1. All quantities are in dB
2. Inputs based on range of 60 nmi except for sea clutter which are for 28.1 nmi
3. Quantization Noise
4. Range Straddle (two samples per range bin)
5. AGI includes coherent filter gain, losses, and clutter attenuation when applicable
6. Loss is for the worst case Doppler mismatch. Gain is for 31-bit code
7. s/n = 9.7 required for nonfluctuating target. Includes loss due to approximation of thresholds.

9524-58

3.6 DYNAMIC RANGE REQUIREMENTS

The number of bits used in the analog-to-digital conversion process impacts both performance and implementation. Performance aspects include the maximum input c/n ratio (dynamic range) at which target detection can occur and the losses due to quantization noise and range straddle (sampling). Implementation aspects include the word size required for subsequent processing and the number of cells required in the residue map (in the data processing).

For an input signal amplitude range of ±1, the quanta in an n-bit digitization is given by $q = 2/(2^n - 1)$ and the quantization noise variance is $\sigma_q^2 = q^2/12 = 1/3(2^n - 1)^2$. The variance of the system noise is σ_s^2 in the I-channel and the same in the Q-channel. It is made large compared to quantization noise by setting $\sigma_s = q$ in both I- and Q-channels. Thus, $\sigma_s^2 = q^2$ and $\sigma_s^2 = 12\ \sigma_q^2$. The total noise in each channel has been increased by $(\sigma_s^2 + \sigma_q^2)/\sigma_s^2 = 13/12$ or 0.35 dB.

A summary of residue map cells and dynamic range vs number of bits is shown in Table 3-VII. The analysis is based on the log-normal ground clutter distribution model, which at the 84th percentile, corresponds to a ground clutter to noise ratio of 46.0 dB at the input to the A/D converter. If the SPUR were to saturate at this level, it would prevent detection in 16 percent of those cells that contain clutter. A cell containing saturating ground clutter is censored by the residue map. Of the 264,000 single batch detection cells in the processor, an average of 29 percent of them or 77,000 cells were estimated to contain ground clutter for this analysis. Thus for a c/n ratio of 46.0 dB, the residue map must provide for 16 percent of 77,000 or 12,300 cells which may saturate. These results are shown in the first row of Table 3-VII and correspond roughly to 9-bit digitization. Results are also shown for increased numbers of bits. The full-scale input c/n ratios are arrived at as follows: The amplitude of the phasor prior to I- and Q-detection must not exceed a value that corresponds to full-scale digitization (+1 or −1) in either the I- or Q-channel. Otherwise, saturation will occur in either the I- or Q-channel. Variance of the system noise prior to detection is the sum of the independent noise variances in the I- and Q-channels. Thus $\sigma_s^2 = 2q^2$ and the full-scale c/n ratio is given by $(2^n - 1)^2/8$.

As the number of bits increases, there is a significant reduction in the size of the residue map. However, the increasing clutter residue after filtering (due to larger clutter than the MTI can handle) would have an increasingly deleterious effect on performance, becoming quite significant at 12 bits. Also, system instabilities may limit the higher input c/n ratios.

3.7 PERFORMANCE DEGRADATION DUE TO SECOND-TIME ECHOES

A radar operating at a fixed prf has range ambiguities at invervals of T/12.36 nmi, where T is the time between pulses in μsec. That is, the echo from a range resolution cell at range R, which is within the normal range coverage, may be accompanied by echoes from

TABLE 3-VII. ANALOG-TO-DIGITAL CONVERSION TRADES

Number of Bits	Full-Scale Input c/n Ratio (dB)	Full-Scale Backscatter Coefficient, σ°_{FS} (dB) (Note 2)	Probability that σ°_{FS} is Exceeded (Note 2)	Number of Cells which may Saturate (Note 3)
Note 1	46.0	-24.0	0.16	12,300
10	51.2	-18.8	0.07	5,390
11	57.2	-12.8	0.015	1,160
12	63.2	-6.8	0.003	231

NOTES:

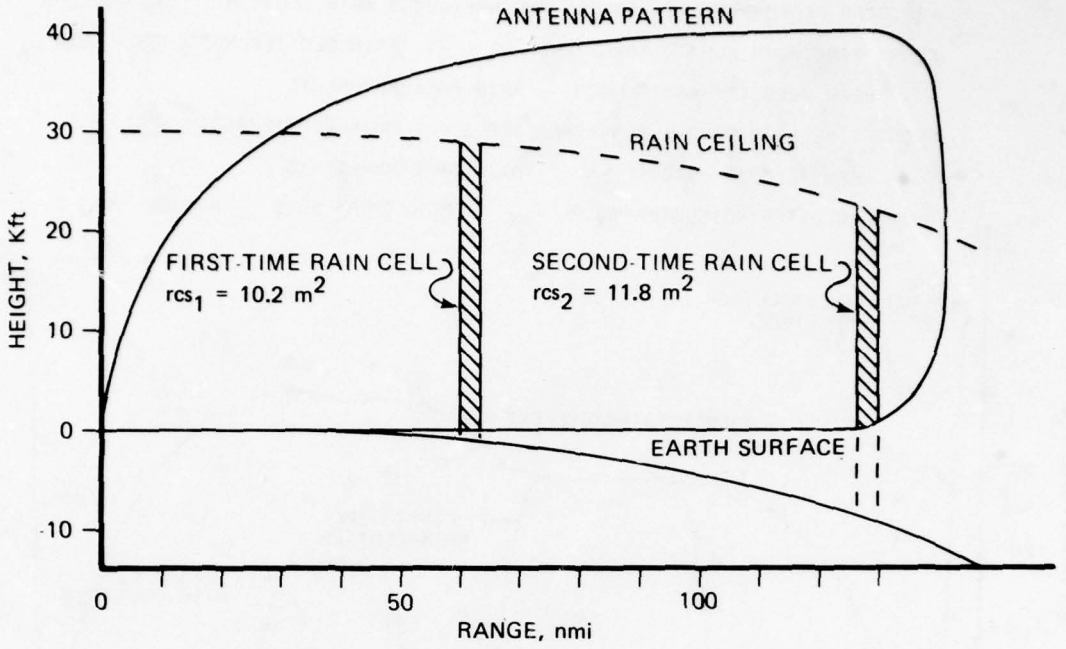
1. c/n = 46.0 dB corresponds to reflectivity at the 84th percentile such as used in the performance summary (Table 3-VI)
2. Based on log-normal distribution of land clutter
3. Based on an estimated 77K cells containing clutter. This is 29 percent of 264K cells total.

9524-59

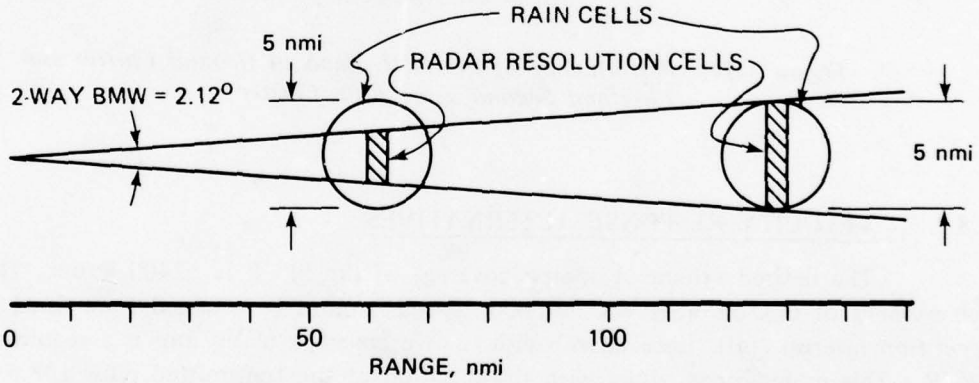
cells at R + TM/12.36 nmi that have been illuminated by the Mth preceding transmission. Such ambiguous echoes can increase the total clutter intake. In addition, performance of the clutter filters against echo clutter may be significantly degraded.

Performance of the SPUR has been evaluated with multiple-time echoes from both rain and ground clutter. The geometry used in calculating the effects of second-time rain clutter is shown in Figure 3-10. Rain returns beyond second-time around are reduced sufficiently such that conventional STC, applied in the receiver from 5 to 30 nmi, effectively eliminates the returns during the first half of the range. From 30–40 nmi, a small degradation of performance (<1 dB) is expected whenever rain occurs simultaneously in the first-, second-, and third-time around range cells. However, this small degradation and low probability of occurrence do not warrant additional processing. Third-time around returns appearing beyond 40 nmi are insignificant because of the antenna pattern, rain ceiling of 30,000 feet and the increased range. NOF bank performance results are shown in Figure 3-11. The conditions assumed are very close to worst case. Also, the combination of heavy rain in both the first-time and second-time resolution cells with almost directly opposite mean velocities is unlikely. Under these conditions, the AGI is reduced to 32.6 dB from 45.2 dB as was shown in Table 3-II. These results are based on processing the returns from a transmitted batch of eight pulses. After the first return from the first-time resolution cell is received by itself, the next seven returns are accompanied by the returns from the second-time resolution cell.

Frequency responses of the NOF bank to the seven second-time returns are shown in Figure 3-12. Comparing these responses with those of Figure 3-7, the loss of the first second-time return results in a severe reduction in the filter attenuation around zero Doppler (i.e., at ground clutter frequencies). With second-time ground clutter, the AGI falls to 37.7 dB from the baseline performance of 50.9 dB against ground clutter. This causes a commensurate reduction in the final s/n ratio. However, by transmitting an additional ***fill pulse*** and ignoring the first return, the responses to second-time returns are restored to those of Figure 3-7. With this fill pulse, the effect of second-time ground clutter on the final s/n ratio is negligible. Although returns from point clutter at even greater ranges may be possible, they will be sparse and will be properly censured out by the clutter residue map. It is recommended that a single fill pulse be used.



a. RANGE-ELEVATION GEOMETRY



b. RANGE-AZIMUTH GEOMETRY

NOTES:

1. RAIN RATE = 15 mm/hr, BOTH CELLS
2. WHEN REFERRED TO FIRST-TIME RAIN CELL, rcs_2 = 0.56 m^2 AND rcs_1/rcs_2 = -12.6 dB.
3. FIRST-TIME AZIMUTH BEAM FILLING FACTOR = 0.992.
4. SECOND-TIME AZIMUTH BEAM FILLING FACTOR = 0.785.

9524-60

Figure 3-10. Possible Geometry of Significant Second-Time Echoes from Rain

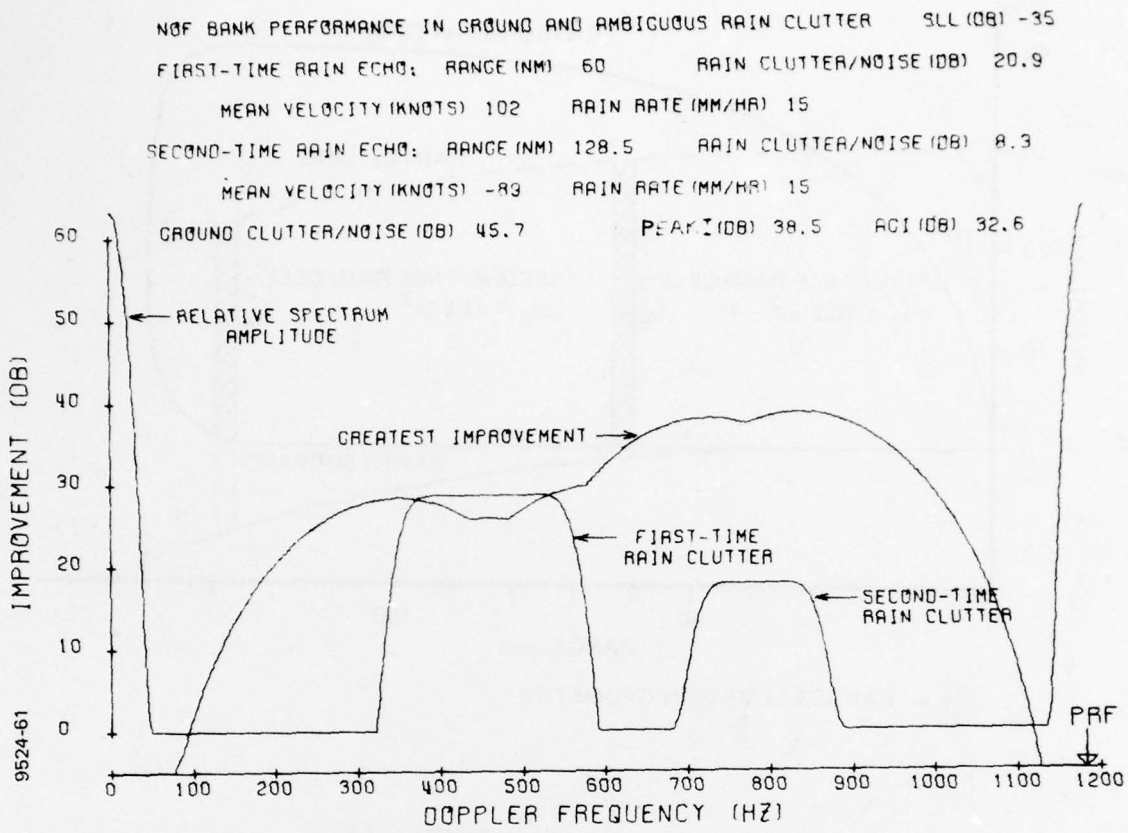


Figure 3-11. Performance of the NOF Bank in Ground Clutter and First and Second Time Rain Clutter

3.8 VELOCITY RESPONSE ALTERNATIVES

The desired velocity response coverage of the SPUR is ±2400 knots. However, achievement of this coverage without blind speeds cannot be attained by a fixed pulse repetition interval (pri), since unambiguous range coverage of 60 nmi is a requirement of the SPUR. This requirement, along with the duration of the transmitted pulse (38.5 μsec) and minimal deadtime, results in the selection of 801 μsec (i.e., blind speeds at multiples of 279.4 knots), as the minimum acceptable pri for the SPUR. Thus, 16 blind speeds occur in the desired Doppler velocity coverage when the pri is fixed.

The natural solution to eliminate blind speeds is to vary the pri. In the SPUR, this variation must be on a group-to-group basis, since the SPUR is a coherent processor using a 9-pulse group (see Section 3.7 for discussion of this recommended group). Thus, the classic staggered pri solution becomes the so-called multiple pri solution in the coherent processor case.

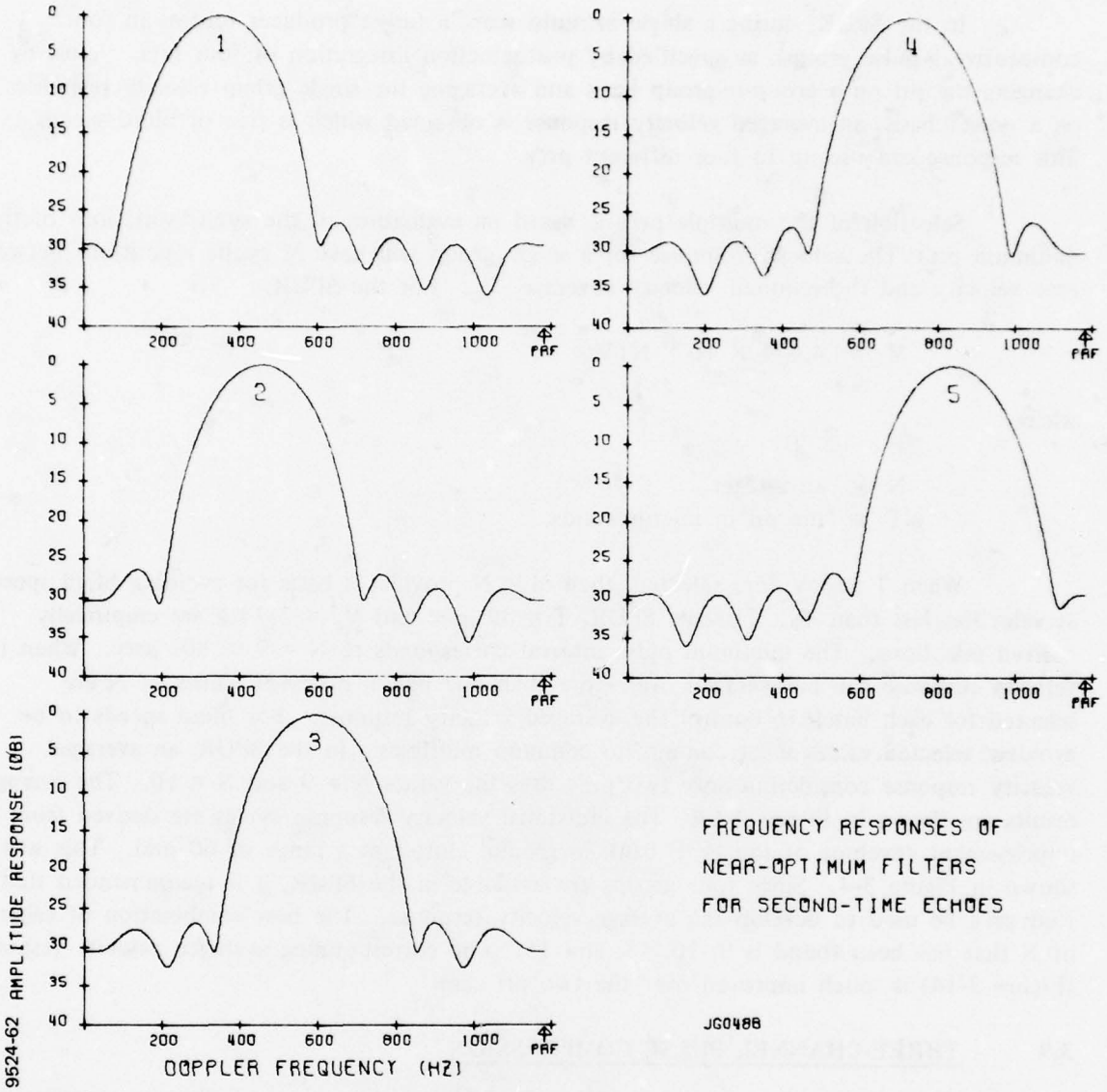


Figure 3-12. Clutter Filter Responses to Second-Time Echoes show Degraded Sidelobes, *because first return is missing*

In the SPUR, during a single azimuth scan, a target produces returns in four consecutive 9-pulse groups, as specified by postdetection integration of four hits. Thus, by changing the pri on a group-to-group basis and averaging the single group velocity responses on a power basis, an averaged velocity response is obtained which is free of blind speeds. This response can use up to four different pri's.

Selection of the multiple pri's is based on evaluation of the cyclic variations of the minimum pri. The velocity response for a single group will have M cyclic repetitions between zero velocity and the required velocity coverage, V_c. For the SPUR,

$$M = 4.474 \times 10^{-6} NTV_c$$

where

N = an integer
NT = the pri in microseconds.

When T and V_c are selected, then M = N provides a basis for avoiding blind speeds at velocities less than V_c. For the SPUR, T = 89 μsec and V_c = 2511.4 are empirically derived selections. The minimum pulse interval corresponds to N = 9 or 801 μsec. When the velocity response can be averaged over more than one batch, different values of N are selected for each batch to control the averaged velocity response. For blind speeds to be avoided, selected values must contain no common multiples. In the SPUR, an averaged velocity response considering only two pri's uses the values N = 9 and N = 10. The averaged results are shown in Figure 3-13. The individual velocity response cycles are derived from the improvement envelope of the NOF bank in ground clutter at a range of 60 nmi. This was shown in Figure 3-4. Since four groups are available in the SPUR, it is recommended that four pri's be used to develop the average velocity response. The best combination of values of N that has been found is 9, 10, 13, and 15. The corresponding averaged velocity response (Figure 3-14) is much improved over the two pri case.

3.9 THREE-CHANNEL PULSE COMPRESSION

Since binary phase coding is highly Doppler sensitive, a modified pulse compressor consisting of three channels was evaluated for the SPUR. In this concept (Figure 3-15), Doppler losses are reduced by effectively sharing the required Doppler coverage among three pulse compressor channels which are matched or approximately matched at three different frequencies.

The three-channel pulse compression approach was analyzed using a simulation that includes:

a) The use of typical 31-bit binary phase coded waveforms;
b) An IF filter that has a 3 dB bandwidth that is either one, two, or four times the 3 dB bandwidth of the waveform;

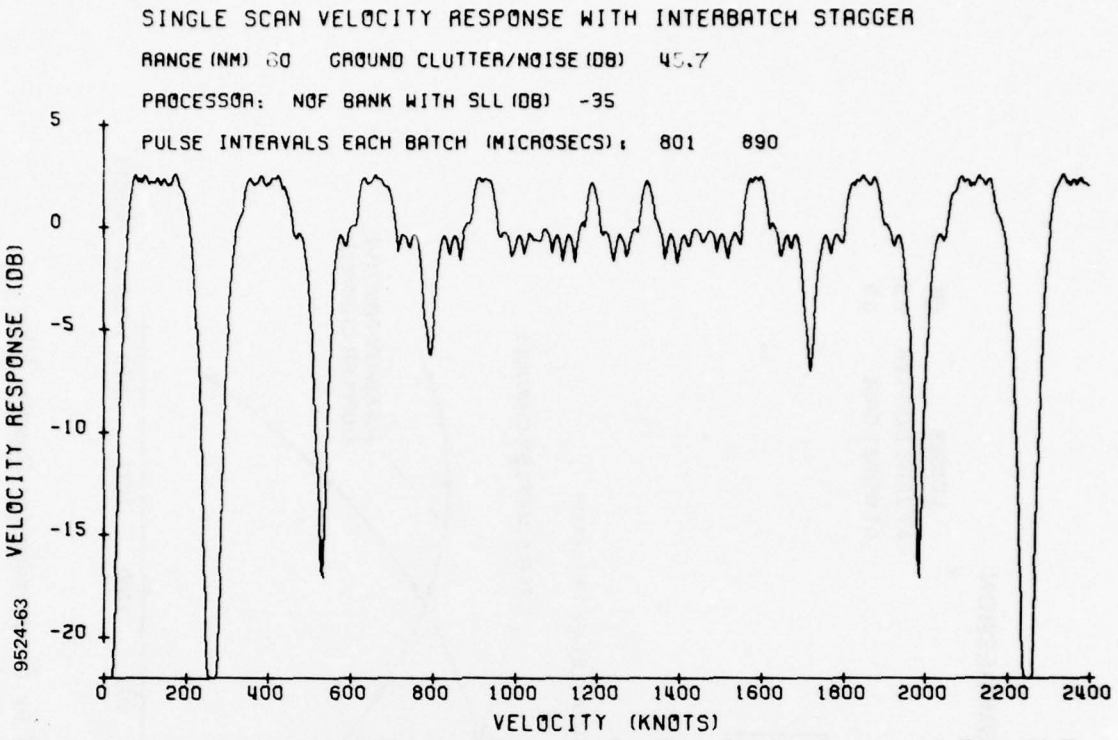


Figure 3-13. The Averaged Velocity Response for Two Batches has several Deep Nulls within the Required Velocity Coverage

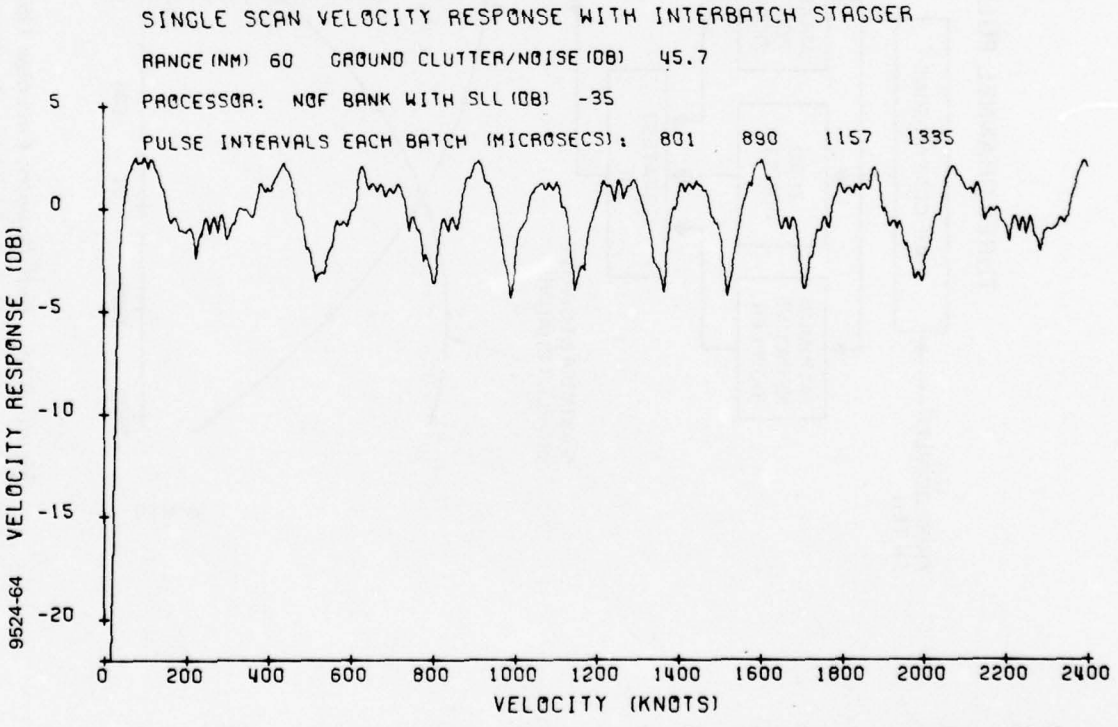


Figure 3-14. The Averaged Velocity Response for Four Batches has no Deep Nulls within the Required Velocity Coverage

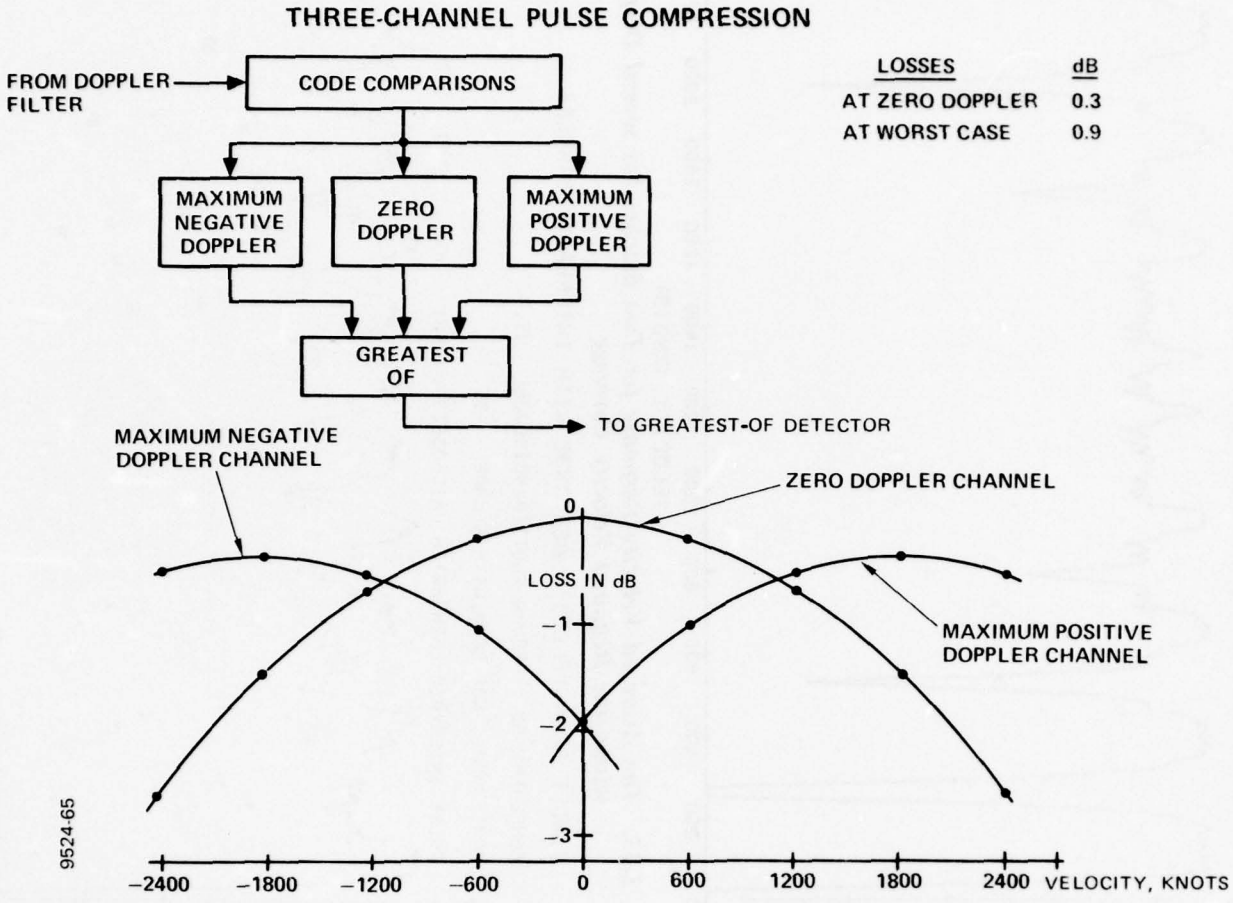


Figure 3-15. Full Doppler Coverage Obtained by Compressing the Doppler Filter Output in Three Overlapping Channels

c) Double range sampling that can be advanced or delayed relative to the filtered waveform;

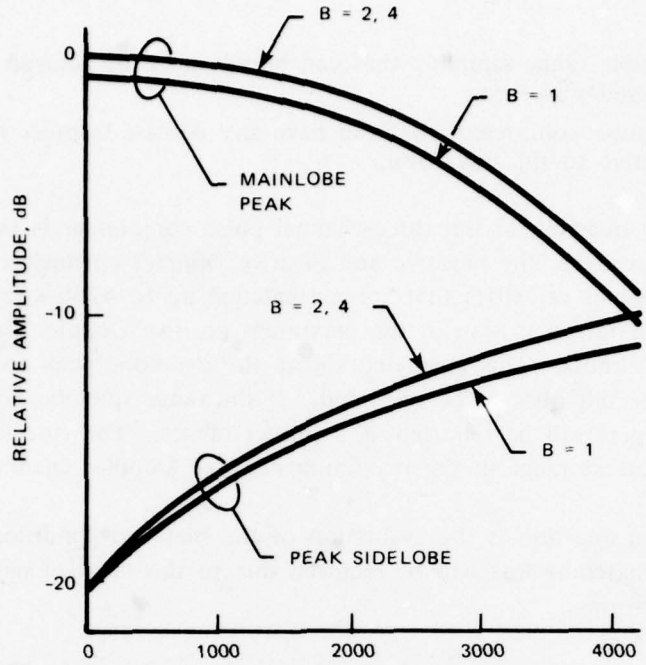
d) A pulse compressor that can have any desired Doppler frequency mismatch relative to the waveform.

One key question in the three-channel pulse compressor is the sidelobe performance. As shown in Figure 3-15, the negative and positive Doppler channels can have targets in them having relative Doppler velocities that are mismatched up to 4200 knots. For example, consider a -2400 knot target as seen in the maximum positive Doppler channel which is nominally matched at +1800 knots. This mismatch causes the mainlobe peak to be reduced and the peak time or range sidelobes to be increased. If the range sidelobes are high enough to be detected, false targets will be reported at incorrect ranges. The true target would also be reported at the correct range in the maximum negative Doppler channel.

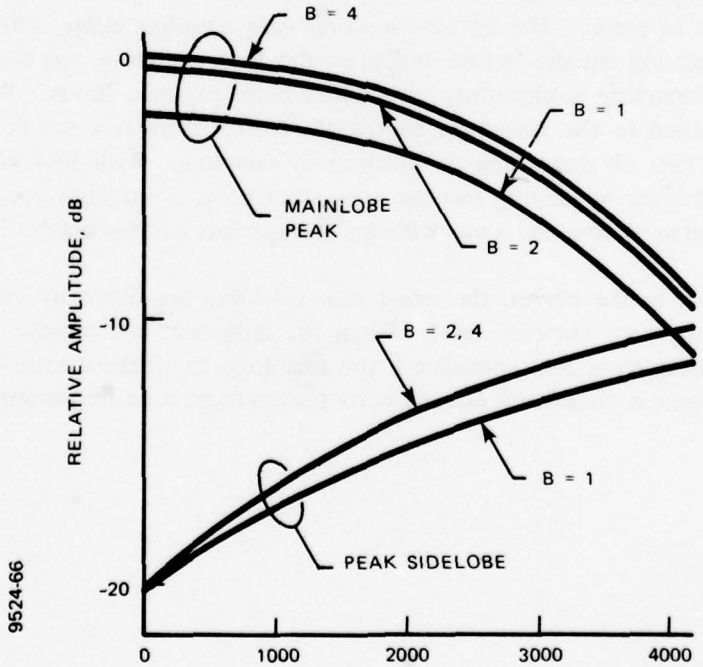
A second question is the evaluation of the matched condition. If the IF bandwidth is too narrow, a matching loss will be incurred due to the sampled nature of the process and the rounded waveforms.

A simulation was performed to evaluate these questions. The results are summarized in Figure 3-16. The relative amplitude of the mainlobe and peak sidelobes are plotted for three IF bandwidths and two sampling positions on the waveform. The curves for ***best case sampling delay*** correspond to one of the range samples occurring at the exact peak of the mainlobe response in range. The curves for ***worst case sampling delay*** correspond to the range samples occurring equally before and after the peak mainlobe response (in range). In operation, actual sampling is uniformly distributed between these limits. When the IF filter bandwidth is matched to the waveform bandwidth (B=1), there is a mainlobe loss that varies between one and two dB depending on position of sampling. With B=4, this loss is essentially zero. However, the accompanying increase in system noise is intolerable. A good compromise selects B to be between one and two, with an average loss of less than 0.5 dB.

As shown in the curves, the worst case sidelobes are down by 10.5 dB (compared with 20.3 dB in the zero Doppler case). When the reduction in mainlobe response, due to the offset and mismatch is also considered, the mainlobe to sidelobe ratio is 9.5 dB. Although this margin is considered adequate, its preservation is an important design consideration.



a. BEST CASE SAMPLING DELAY (SEE TEXT)



b. WORST CASE SAMPLING DELAY (SEE TEXT)

NOTE: B = RATIO OF IF BANDWIDTH TO WAVEFORM BANDWIDTH

Figure 3-16. Pulse Compressor Response Amplitudes For Combinations of Doppler, IF Bandwidths, and Sampling Delay

Section 4

TECHNOLOGY EVALUATIONS

Current and emerging technologies were evaluated to assess their applicability to implementing functions of the Signal Processor for Unattended Radar. Since any technology evaluation is necessarily a snapshot in time and the electronics industry (semiconductors, in particular) is moving at a rapid development pace, the current state-of-the-art was evaluated relatively early in the study and limited projections (through about 1980) were made to assess the development activity. Promising technologies, both analog and digital, were evaluated based on speed, power, and applicability to the maintenance concepts of an unattended radar, such as stability, automatic calibration, and automatic adjustment. The breadth of the considerations is illustrated in Table 4-I.

Several technologies were eliminated early in the study because of mismatches to SPUR requirements. As shown in Table 4-I, these rejections included such digital technologies as Emitter Coupled Logic (ECL) (due to high power consumption) and P-Channel Metal Oxide Semiconductor (PMOS) (due to slow speed). The remaining technologies were evaluated in more depth and are discussed in following paragraphs. This section discusses the attributes and deficiencies among the various considered technologies relative to the SPUR requirements. However, in development of the optimum processor, tradeoffs among potential alternatives, each of which can meet the SPUR requirements, were made to achieve the best processor. These final tradeoffs are discussed and illustrated in Section 6, Description of the Optimum Processor, under the appropriate functional heading.

4.1 ANALOG TECHNOLOGIES

Analog technology evaluations were broken into two categories: a) those technologies applicable to several functions, and b) those technologies directed to a specific function. In the former category were Charge Transfer Devices, including Bucket Brigade Devices (BBDs) and Charge Coupled Devices (CCDs). The latter category included Surface Acoustic Wave (SAW) devices and steel lines. While SAWs can be used for Doppler processing via transversal filtering based on the Chirp-Z Transform, this processing was not considered in depth for the SPUR. The relatively high sample rate, wide dynamic range, and relatively long storage times make the required analog corner-turner memory design very difficult and risky. Consequently, SAW devices and steel lines were considered for pulse compression only.

Charge Transfer Devices are highly attractive because of low power consumption and compactness. They have applications in MTI (cancellers), pulse compression, Doppler processing, and CFAR. MTI requires simple delay lines, while the other processes require tapped delay lines to generate transversal filters. Currently available devices were evaluated for three factors: speed, dynamic range, and unattended operation features. A typical example of a simple delay line is the Fairchild CCD321A, while the Reticon TAD32A (which is a bucket-brigade device) is an example of a tapped delay line. Some pertinent characteristics of these devices are listed in Table 4-II.

TABLE 4-I. FIVE AREAS WERE INVESTIGATED FOR TECHNOLOGY APPLICABLE TO SPUR REQUIREMENTS

ANALOG-TO-DIGITAL CONVERTER TECHNOLOGIES

ANALOG TECHNOLOGIES

Charge Transfer Devices
Surface Acoustic Wave Devices
Steel Dispersive Delay Lines

DIGITAL TECHNOLOGIES

Emitter Coupled Logic (ECL) – Rejected due to high power demand
Low Power Schottky Transistor-Transistor Logic (LS TTL)
Integrated Injection Logic (I^2L)
Complementary Metal Oxide Semiconductor (CMOS)
N-Channel Metal Oxide Semiconductor (NMOS)
P-Channel Metal Oxide Semiconductor (PMOS) – Rejected due to slow speed
Large Scale Integration (LSI) in above technologies
Uncommitted Arrays in above technologies.

PROGRAMMABLE TECHNOLOGIES

Bit Slice Based Microprocessors
Dedicated 16-Bit Microprocessors

MEMORY TECHNOLOGIES

NMOS
CMOS
Charge Coupled Devices (CCD)
Bipolar (Read Only Memories)
Bubble Memories
Metal Nitride Oxide Semiconductor (MNOS)

9524-1

TABLE 4-II. PERTINENT CHARACTERISTICS FOR TWO CHARGE TRANSFER DEVICES illustrate current performance of delay lines and tapped delay lines.

	CCD321	TAD32
Clock Speed	20 MHz	5 MHz
Bandwidth (max)	5 MHz	2.5 MHz
Dynamic Range	49 dB	43 dB
Storage Cells	910	—
Taps	—	32

9524-2

CTDs exhibit adequate speed for the SPUR. However, as shown in Table 4-II, the dynamic range (peak signal-to-rms noise) at maximum temperature is specified and measured at 49 dB for the delay lines and calculated at 43 dB for the tapped delay lines. This dynamic range is not adequate to meet the SPUR requirements for front-end processor functions such as MTI or pulse compression. Excessive limiting of the large dynamic range clutter will occur. As is well known, limiting reduces the achievable improvement factor of the signal processor and can saturate automatic target detection systems and subsequent residue maps. On the other hand, these devices can meet the requirement of post clutter filtering processing. However, once the conversion to the digital domain is forced, it is not generally attractive to return to analog processing because the major expense of analog-to-digital conversion has been paid.

Unattended operation features of currently available devices were also evaluated. The delay lines require several adjustment potentiometers for optimum device operation. While this alone does not preclude unattended operation, variations with temperature and clock rate have been noted. An example of this variation (Figure 4-1) illustrates the increase in harmonic distortion in a CCD321A when the temperature was varied over 55°C. In general, this increase in harmonics decreases the usable dynamic range of the device.

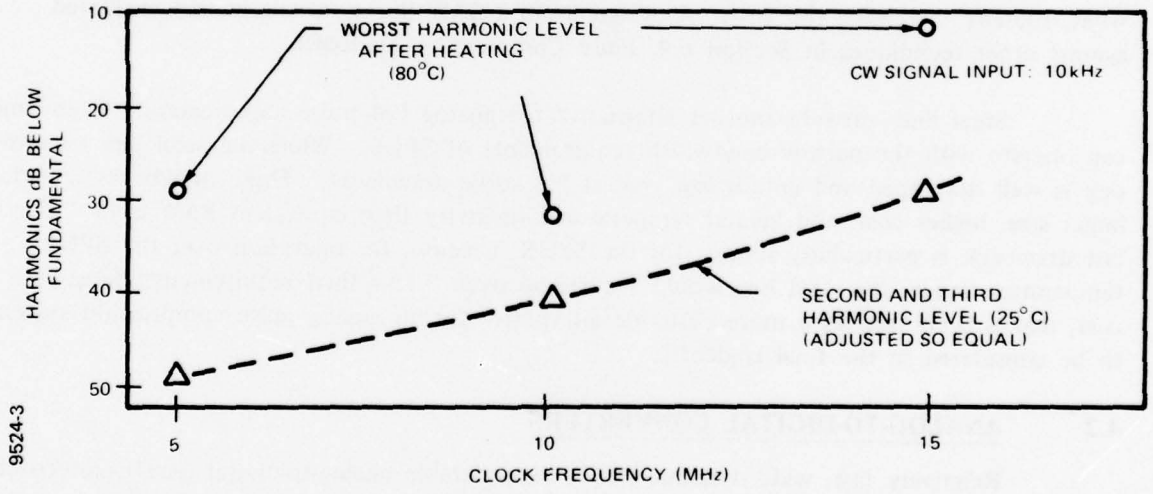


***Figure 4-1. Harmonic Levels at the Output of a CCD 321A** show large temperature and clock rate sensitivities*

Since currently available devices do not have adequate performance, the state and direction of device development were investigated. While laboratory devices can perform to significantly higher levels than the above devices, the trends for production indicate that suitable devices will not be available in the required time frame or even in the mid-1980s. In general, the developments in CTDs seem to be aimed at areas with dynamic ranges on the order of 40 - 45 dB, specialized filter functions, and image processing. There they provide a real alternative to digital signal processing.

With the rejection of CTDs for use in the SPUR, investigation of additional analog devices which would have supported the CTD system was discontinued. However, for analog processors of reduced dynamic range, a plethora of exciting new devices is becoming available including low power, high performance operational amplifiers, multipliers and other multi-function units based on similar techniques, and multiplying digital-to-analog converters.

SAW devices are potentially attractive for pulse compression when this function is implemented ahead of Doppler processing. The SAW device is passive, compact, and can meet the SPUR requirements over the temperature range without use of an oven (when fabricated on ST-cut quartz). The use of ST-cut quartz does result in a relatively large insertion loss, i.e., up to 30 dB, which must be recovered by a following amplifier; however, the line driver and following gain amplifiers are the only power consuming parts of the circuit. The relatively narrow bandwidth (i.e., 800 kHz) of the SPUR complicates the design somewhat, thereby increasing the cost. A design using a SAW line is discussed and evaluated against other techniques in Section 6.4, Pulse Compression Tradeoffs.

Steel lines provide another alternative for analog FM pulse compression. These units can operate with the narrow bandwidth requirements of SPUR. While the steel line technology is well developed and entails low risk, it has some drawbacks. These drawbacks include larger size, higher cost, and greater temperature sensitivity than equivalent SAW units. This last drawback is particularly serious for the SPUR, because, for operation over the SPUR temperature range, the steel line would require an oven. This final requirement, along with cost, makes SAW devices a more desirable alternative for an analog pulse compression system to be considered in the final tradeoffs.

4.2 ANALOG-TO-DIGITAL CONVERTERS

Relatively fast, wide dynamic range, highly stable analog-to-digital (A/D) conversion is a key requirement of the SPUR. The combination of a conversion time of 618 nsec (two samples per 0.1 nmi range bin) and a resolution of 11 - 12 bits is not currently available in modular successive approximation converters or monolithic flash converters, the two circuit techniques used for fast, wide dynamic range converters.

Successive approximation devices (Figure 4-2) perform A/D conversion by evaluating one bit at a time through a comparison of the unknown input signal with sums of accurately known binary fractions of full scale. The bit-by-bit result becomes the digital word. The comparisons are timed by a fast (usually internal) clock operating from a system encode

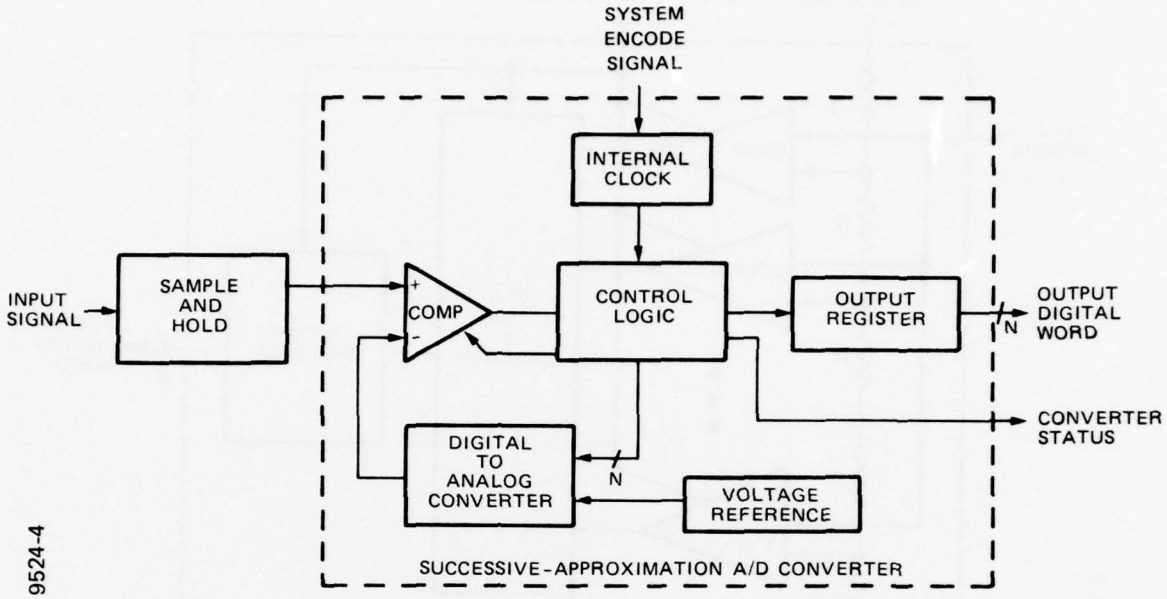


Figure 4-2. The Successive Approximation A/D Converter *uses a comparator to generate one bit at a time.*

signal. Since the conversion is made over many internal clock periods (i.e., 12 for a 12-bit A/D converter), a sample-and-hold circuit is usually required prior to the A/D converter to keep the signal constant during the conversion time. These converters meet the SPUR resolution requirement of 11 - 12 bits, but their conversion times are too long. The conversion times for high resolution, successive-approximation units are not expected to drop significantly over the next year or two because major demands for converters are being met with current devices. Developments are now aimed at converters and microprocessors on a single chip and other microprocessor-compatible configurations. However, a potentially attractive A/D converter can be developed from these units using a bank of parallel modules in staggered operation. An architecture using a representative device (Datel ADC-EH12B3, 12-bits at 2.0 μsec) is discussed in Section 6.5, Analog-to-Digital Converter Tradeoffs.

Flash converters, usually as monolithic devices (Figure 4-3), perform A/D conversion by using a parallel bank of 2^n-1 comparators to convert an unknown input signal to an n-bit digital word. The thresholds of the comparators are set one least-significant-bit (LSB) apart, so as to cover the full input range, by a precision resistor string. The states of the outputs from the 2^n-1 comparators are reduced to the n-bit word by an on-chip digital network. Thus, in a flash converter, all bits are developed at once by the comparators and a sample-and-hold circuit is not required. Current flash converters far surpass the speed requirements of SPUR, but their resolution is inadequate. State-of-the-art TRW units have a resolution

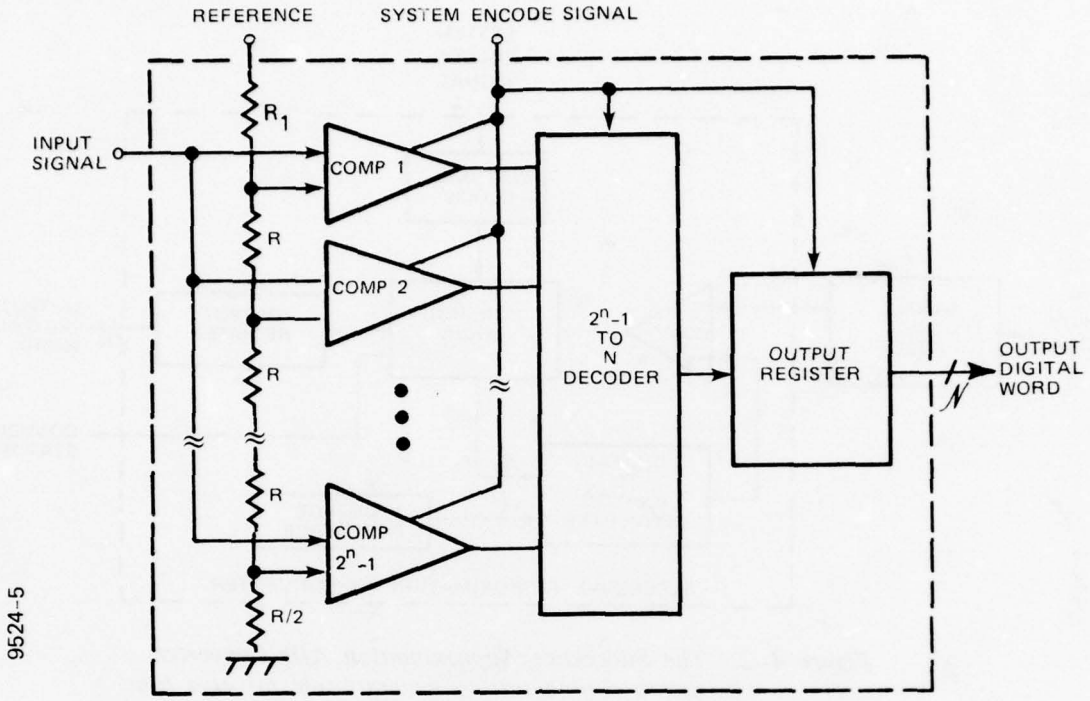


Figure 4-3. The Flash Converter Uses a Bank of Computers *to generate all bits at the same time.*

of 8-bits at 33 nsec conversion time. Since an 8-bit unit requires 255 comparators plus the digital reduction network on a single chip, this resolution will not be improved in the next few years. Current work is progressing on monolithic 8-bit D/A converters with similar speeds.

An A/D converter meeting SPUR requirements can be developed from the flash converter by doing the conversion in two steps, essentially a coarse and fine conversion (Figure 4-4). The first 8-bit unit is used as the coarse conversion with the eight bits sent to the digital correction circuitry (discussed following) and the digital-to-analog circuit. The resulting analog signal from this device is subtracted from the input signal and the resulting difference or subrange signal is converted by the second A/D converter, a 6-bit unit. These six bits are sent to the digital correction circuitry for final correction to the required number of output bits. The digital correction circuitry is designed based on the specified accuracies of the first A/D converter and the D/A converter. When the D/A converter is specified to have accuracy to the 11 - 12 bits required of the final converter, then the digital correction circuitry will be used to correct the final bits based on the accuracy of the initial A/D converter only. This accuracy can be controlled such that the correction applied at the output will consist of 0 ±1 LSB of the first converter. The two-step flash converter requires a sample-and-hold circuit to keep the signal constant during the first conversion and subsequent difference operation. Use of a two-stage flash converter is further described in Section 6.5.

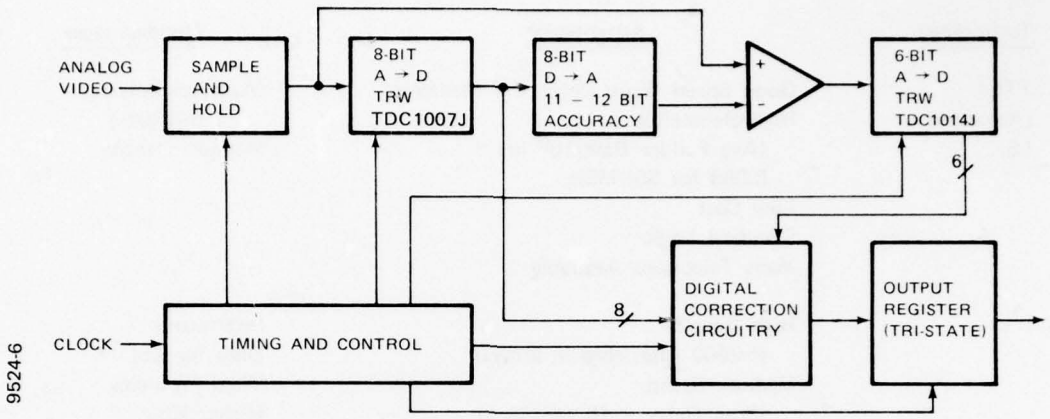


Figure 4-4. ***The Two-Step Flash Converter*** *achieves the required resolution by performing coarse and fine conversions*

4.3 DIGITAL TECHNOLOGIES

Four major digital technologies (two bipolar and two metal oxide semiconductor (MOS)) were evaluated for applicability to implementing the functions of SPUR. An overview of technology characteristics (Table 4-III) illustrates the relative advantages and disadvantages of each. From this table, it is clear that each technology has significant advantages which make it attractive for portions of the processor. However, each also has drawbacks which preclude its exclusive use. The selection of technologies for specific functions of the SPUR was accomplished by evaluating estimated designs of each function in a particular technology.

4.3.1 Bipolar Technologies

Transistor Transistor Logic (TTL), particularly Low-Power Schottky (LSTTL), is a well-developed logic form which has excellent speed capability at a modest power level. The many advantages of TTL for systems which are not severely power-limited have led to its acceptance as a digital standard. The characteristics shown in Table 4-III are for the third generation Low Power Schottky devices currently being introduced by semiconductor manufacturers such as Texas Instruments and Fairchild. The power dissipation of this generation of Low Power Schottky has been cut in half from that of its predecessor, while the speed

TABLE 4-III. AN OVERVIEW OF THE ADVANTAGES AND DISADVANTAGES OF FOUR MAJOR DIGITAL TECHNOLOGIES SHOW NO IDEAL TECHNOLOGY FOR SPUR

Technology	Advantages	Disadvantages
TTL (Advanced LS)	Good Speed (Prop Delay = 4 nsec/gate) High Reliability (Avg Failure Rate/10^6 hrs = 0.058 for SSI/MSI) Low Cost Standard Logic Many Functions Available	Moderate Power (1 mW/gate) Medium Density
I^2L	High Density (~2000 gates/chip in arrays) Medium Speed (Prop Delay = 10 nsec/gate) Medium Power (0.2 mW/gate)	Interfacing Only for LSI Yield Problems Higher Risk
CMOS	Low Quiescent Power (0.07 mW/gate) Many Functions Available Easy Interfacing	Power Dissipation a Function of Clock Rate Relatively Slow Speed (Prop Delay = 20 nsec/gate) Medium Reliability (Avg Failure Rate/10^6 hrs = 0.165 for SSI/MSI) Medium Cost Handling Care Required
NMOS	High Density (16 bit CPU on a chip) Medium Power (0.3 mW/gate) Medium Speed (Prop Delay = 15 nsec/gate) Low Cost Acceptable Interfacing	No Functions Available Only for LSI Handling Care Required

9524-7

has been doubled. Since this technology is just being introduced, it carries about a 25 percent cost differential above standard LSTTL, but this will disappear by 1981. This generation of devices will have the best performance available in LS into the early 1980s. For the SPUR, basic LSTTL costs have been used as the normalizer for cost comparisons of fixed logic designs.

Since TTL has become a standard for digital logic design, most other logic families provide "TTL compatibility" through interface chips or on-chip TTL input/output drivers. This compatibility allows changing among technologies when such a change has significant advantages. One obvious example of this technology interchange is the use of MOS memories in basically TTL system designs. MOS memories have greater density and lower power and cost than TTL memories.

Integrated Injection Logic (I^2L) is attractive as a low-power, medium speed technology. It is particularly appropriate for LSI implementations because of its simple gate structures which allow high density circuits to be fabricated. While the design of I^2L circuitry is relatively straightforward, the processing requirements to achieve superior performance are somewhat extensive. This exotic processing has led to yield problems both in microprocessor developments and uncommitted arrays, causing unexpected delays in shipping hardware. Also no standard process which can be second-sourced has developed. While these problems are currently being worked, a wait-and-see attitude has developed among some major development houses. Thus I^2L remains a technology of the future. For the SPUR these factors cause us to weigh other technologies as lower risk since we do not have absolute requirements for I^2L such as radiation hardness and very low voltage operation, like the 1.5 volts used for watch circuits.

4.3.2 MOS Technologies

The MOS technologies feature high chip densities along with relatively low power. These chip densities are the result of small cell sizes of the building blocks and very low power dissipation per cell. Two major technology related pushes are evident in MOS:
a) development of LSI devices in NMOS (N-channel metal oxide semiconductor), and
b) development of a CMOS (complementary metal oxide semiconductor) logic family with which extremely low power dissipation can be obtained under the appropriate application conditions.

NMOS technology has recently seen major development activity in memories and microprocessors. The trends for the technology are not only higher density chips (e.g., 64K random access memory chips and 16-bit microprocessor CPUs on a chip), but also higher speeds (memory access times better than 100 μsec and microprocessor clocks on the order of 8-10 MHz). These higher densities are generally the result of three developments: increase in economical chip or die size, decrease in basic cell size, and modifications to the basic NMOS technology (e.g., going to specialized designs such as Vertical Metal Oxide Semiconductor (VMOS) and High Performance MOS (HMOS)). While the technology will continue

to advance, the major breakthroughs applicable to the early 1980s probably have been announced. Much of the work between now and about 1981 will be devoted to getting high density memories and 16-bit microprocessors into full production. This will allow the semiconductor economic laws to lower the prices and create widespread demand for the parts. Additional development in this time frame can be expected in the support chips necessary for configuring microcomputer systems. For the SPUR, NMOS memories and 16-bit microprocessors have been evaluated (see Section 6, Description of the Optimum Processor).

Low power dissipation is the chief feature of the CMOS (Complementary Metal Oxide Semiconductor) technology. Because the designs use both PMOS and NMOS devices as switches in a cell (Figure 4-5), the dc power dissipation is only a function of the leakage currents of the two switches. This power dissipation, consequently, is very small (on the order of nanowatts). However, because power is dissipated when the devices are switching, the total power usage of the devices is dependent on the system clock rate. This dependence is shown in the typical power dissipation versus switching rate curve for CMOS (Figure 4-6). As shown in the curve, this dissipation is also dependent on power supply voltage. CMOS devices are usually characterized at 5, 10, and 15 volts. Since the power supply voltage level also affects the speed of the devices (with a doubling of speed when the level is increased from five to ten volts), tradeoffs between speed, power, and power supply voltage can be made in designing with CMOS devices.

The SPUR requirements indicate a processing rate or clock speed on the order of 1.6 MHz. For functions such as the post Doppler Filter Processing, this speed translates to operation of CMOS devices at 10V minimum for single channel operation. While the power is not minimized at this clock rate and voltage level, slower speeds at the minimum voltage (5 volts) require more processing channels, increased complexity, and increased cost. On the other hand, this increased complexity can be implemented in a more natural fault-tolerant structure such as parallel channels with standby redundancy. However, with the cost of CMOS projected at about two times equivalent TTL functions (currently it runs about 2.35), and the factor of 2.8 greater failure rate in CMOS over TTL, the cost of an acceptable system in parallel channel CMOS is doubled over a single channel CMOS implementation.

In addition to standard CMOS devices, much development work is occurring in more advanced CMOS technology such as Silicon on Sapphire (CMOS/SOS) and oxide-isolated CMOS. CMOS/SOS promises higher speeds than conventional CMOS, but at the present time it is considerably more expensive, restricted to a few vendors (RCA, Hughes, Rockwell), and aimed at specialized applications. This specialization is expected to remain the trend over the time frame of interest. Oxide-isolated CMOS, on the other hand, is a more widespread technology development which will increase the speed of CMOS with little power penalty. Preliminary reports show a goal of 10 MHz operation at 5V compared to the current performance of 1 MHz at 5V. This performance improvement should be available in uncommitted array form in late 1979 and appears feasible for semicustom LSI of higher complexity than currently available.

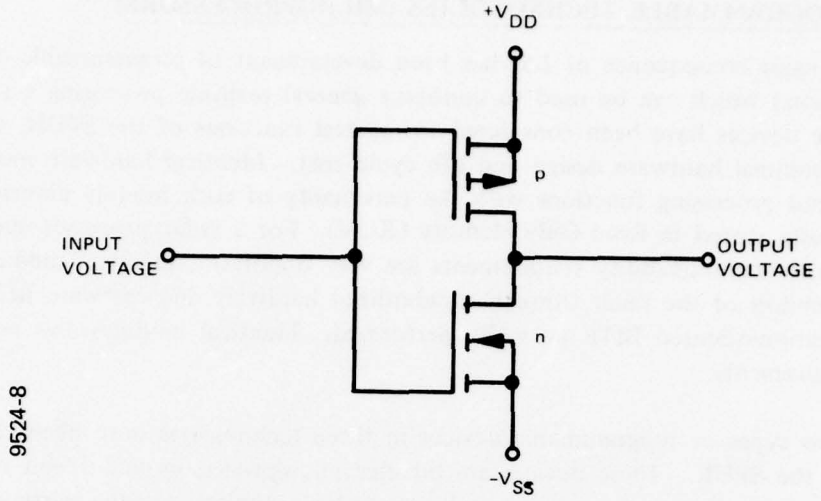


Figure 4-5. ***The Basic CMOS Cell consists of PMOS and NMOS Devices*** *such that in the quiescent state only leakage currents cause power dissipation.*

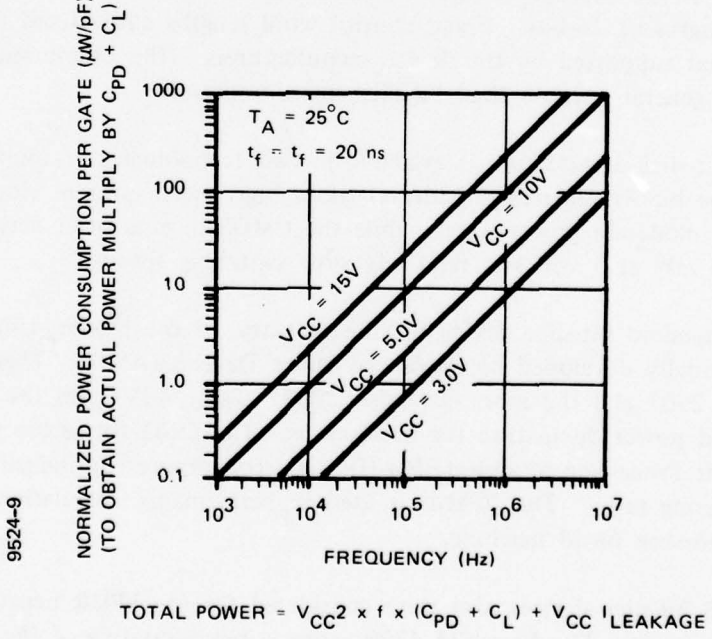


Figure 4-6. ***Normalized Power Dissipation Curves for CMOS Devices*** *illustrate heavy dependence on switching speed and power supply voltage level.*

4.4 PROGRAMMABLE TECHNOLOGIES (MICROPROCESSORS)

A major consequence of LSI has been development of programmable devices (microprocessors) which can be used to configure general realtime processing systems. These programmable devices have been considered for several functions of the SPUR, where they can lead to minimal hardware design and life cycle cost. Identical hardware modules can be used for several processing functions with the personality of each module determined by firmware usually stored in Read Only Memory (ROM). For a radar processor such as the SPUR, in which maintainability requirements are very important, identical modules improve the maintainability of the radar through standardized hardware and software BITE in addition to the application-oriented BITE normally performed. Identical modules also reduce spares stocking requirements.

Two types of programmable devices in three technologies have been considered for functions of the SPUR. These devices are bit-slice microprocessors and 16-bit microprocessors. Bit-slice devices allow the microprocessor design to be optimized for the particular class of processing tasks expected, because the architecture of the processor is largely determined by the designer. In addition, data word length is selectable, usually in increments of four-bits (hence the name bit-slice) and the instruction set and microcode are completely determined by the designer. These microprocessors tend to have wide control words allowing considerable parallel operation of the processor in bit-oriented tasks common to radar signal processing (i.e., tasks other than arithmetic functions unless additional Arithmetic Logic Units (ALUs) are provided). The 16-bit microprocessors, on the other hand, are characterized by data and control word lengths of 16-bits. Fixed control word lengths allow fixed instruction sets which are developed and supported by the device manufacturers. The 16-bit microprocessors are, therefore, more general purpose than bit-slice microprocessors.

The bit-slice architecture is available in two technologies of interest: Schottky TTL and CMOS. The bipolar devices provide relatively high speed (system clocks on the order of 200 nsec) at moderate power levels, while the CMOS devices offer very low power (on the order of 70 mW at 5 volts) at relatively slow switching speeds.

The standard bit-slice device for the industry, at the present time, is the bipolar 2900 series originally developed by Advanced Micro Devices (AMD). This series has two CPU chips, the 2901 and the more advanced 2903. Table 4-IV gives the current and projected speed and power dissipation for these chips. The 2903 forms the basis of the second-generation Radar Processing Module (RPM-II), a microcomputer optimized by ITT Gilfillan for radar processing tasks. The RPM-II is used in performance calculations (Section 6) as a representative bit-slice based machine.

CMOS bit-slice devices also were considered for the SPUR because of their potentially low-power usage. The Fairchild 4700 series is representative of the current state of the art. A comparison of these devices with bipolar devices (Table 4-V) shows the advantages of each technology. The low power usage of CMOS is attractive; however, when its speed

TABLE 4-IV. INCREASED SPEED IS PROJECTED FOR THE BIPOLAR BIT-SLICE MICROPROCESSOR FAMILY

2900 Series – Low Power Schottky

Device	Speed	Power	Availability
2901A	180 nsec	5V/160 mA (each 4-bits)	Now
2901B	155 nsec		Now
2901C	140 nsec		1980
2903	200 nsec	5V/220 mA (each 4-bits)	Now
2903A	180 nsec		1980

9524-10

TABLE 4-V. BIPOLAR DEVICES FEATURE HIGH SPEED, WHILE CMOS DEVICES FEATURE LOW POWER IN BIT-SLICE MICROPROCESSORS

	2900 Series	4700 Series
Technology	LS TTL	CMOS
System Clock Speed	5 MHz	1 MHz (5 volts)
Word Size (Bit Slice)	4	4
ALU Instructions	16	64
ALU Registers	16	8
Power (watts)	1.1	70 mW
Failure Rate ($f/10^6$ hr)*	0.277	0.496

9524-11

* MIL-HDBK-217C

is compared to the 2900 series and evaluated against the processing requirements of the SPUR, the CMOS implementation requires almost three times as much hardware as the bipolar implementation. As described in Section 6, Description of the Optimum Processor, a bipolar-based microcomputer on one board can perform all of the processing recommended for implementation in programmable hardware. The equivalent CMOS implementation would require three microcomputers plus redundancy. This design is considerably more complicated due to the partitioning requirements and more costly due to the increase in hardware required and the price differential between bipolar and CMOS devices. For these reasons, in the time frame of interest, the CMOS implementation, even though it can attain some power savings, is not competitive with the bipolar bit-slice processor for the SPUR. It was, therefore, not considered beyond the preliminary technology speed and sizing study.

The 16-bit microprocessor is the second type of device considered for SPUR programmable processing. In these devices, the CPU is fabricated on a single chip using NMOS or related technology (such as HMOS). Second generation units are now becoming available which provide an order of magnitude improvement in performance over previous devices. Units from several manufacturers were considered (Table 4-VI) early in the study. The Motorola 68000 was selected for further evaluation in SPUR processing tasks because it has an advanced architecture which is amenable to multiprocessing and a powerful instruction set tailored to higher order language software development. Motorola will support PASCAL on the MC68000. A representative MC68000-based microcomputer was configured and is evaluated versus the bit-slice based RPM-II in Section 6.

An overall comparison of the processing capabilities and special features of the MC68000 and the RPM-II are shown in three tables. A basic performance characteristics comparison of the two processors is shown in Table 4-VII. Note that data and program storage is separate in the RPM-II and combined in the MC68000. The speed comparisons show that even though the basic clock rate for the MC68000 is higher, instruction times for the MC68000 are longer than for the RPM-II. The RPM-II performs all simple instructions except a conditional branch command in a single clock cycle of 200 nsec, while the MC68000 uses multiple clock cycles to perform every instruction with the number of clock cycles used dependent on the instruction. In both processors multiplies and divides are handled by repeated shifts and adds or subtracts through well-known algorithms since neither processor as configured has a fast hardware multiply capability.

The special features of the MC68000 microprocessor (Table 4-VIII) include instructions to speed up data transfers (such as LOAD MULTIPLE REGISTERS), an advanced interrupt structure, and multiprocessor oriented features (shared bus and shared memory environment). The special features of the RPM-II (Table 4-IX) include a dynamic environment for enabling and masking interrupts, separation of data and instructions, and a versatile I/O structure with multiple ports.

TABLE 4-VI. THREE 16-BIT MICROPROCESSOR REPRESENT SECOND GENERATION PERFORMANCE UNITS

Device	Speed*	Power	Features
8086	400 nsec	5V/275 mA	Multiprocessor-Oriented
68000	500 nsec	5V/300 mA	Higher Order Languages
Z8000	750 nsec	5V/300 mA	Multiprocessor-Oriented

9524-12

*Shortest Instruction Times

TABLE 4-VII. COMPARISON OF BASIC PERFORMANCE CHARACTERISTICS OF THE MC68000 16-BIT MICROPROCESSOR AND THE RPM-II BIT-SLICE-BASED MICROPROCESSOR

	MC68000	RPM-II
Data Word Size	16-Bits (32-Bits Internal)	16-Bits
Data Storage	Data and Program	64K Words
Program Storage	Storage Combined — 8M Words	4K Words
Number of Instructions Available in Instruction Set	61	User Defined
Program Instruction Word	16-Bits Wide	56-Bits Wide
Clock Rate	8 MHz	5 MHz
Instruction Times		
Shift	1.25 μs (1 bit) 4.75 μs (15 bits)	200 nsec (1 to 4 bits) 800 nsec (16 bits)
Add, Subtract	1 μsec	200 nsec
Multiply	8.75 μsec	3.2 μsec
Divide	17.75 μsec	3.2 μsec

9524-13

TABLE 4-VIII. MC68000 PERFORMANCE CHARACTERISTICS CONTAIN SPECIAL FEATURES, which aid in usage of the microprocessor

9524-15

- Multiply and Divide
- Decrement and Branch Nonzero
- Load Multiple Registers
- Store Multiple Registers
- Multilevel Interrupt and Trap Structure
- Memory Bus Arbitration
- Shared Bus
- Shared Memory Environment
- Arithmetic and Logical Shifts

TABLE 4-IX. THE RPM-II FEATURES A VERSATILE DATA MANAGEMENT AND I/O STRUCTURE

9524-15

- Multiply and Divide
- Single and Double Length Normalization
- Conversion between Sign Magnitude and Two's Complement
- Increment by One or Two
- Left or Right Shift of Data after ALU
- Arithmetic and Logic Shifts
- Dynamic Interrupt Structuring
- Interrupt Service Routine Nesting
- Programmed I/O and DMA I/O Modes of Data Transfer
- Multiple I/O Ports and FIFO Port
- Separate Instruction and Data Buses

Trends in programmable processing were also investigated early in the study to identify developments which would affect the SPUR. Developments in three areas are described: 16-bit microprocessors, dedicated BITE, and peripheral chips. Sixteen-bit microprocessor architectures are maturing toward high performance computers and away from the more limited architectures of the early 8-bit microprocessors. The MC68000 is a good example in this area, because it is not just an extension of the 8-bit MC6800 microprocessor but a major change and upgrade of the microprocessor concept. Along with more mature architectures of the 16-bit microprocessors, more 16-bit single chip microcomputers will be available. These devices add program memory (ROM) and random access memory onto the chip along with the CPU. Currently, and for the SPUR time frame, these devices are relatively slow. However, they will be important in the future. A key development area for this type of device will be to structure them for multiprocessor operation instead of stand-alone units.

Dedicated BITE is a development of considerable interest. Special programs for test of the microprocessor are provided on the chip such that the microprocessor operation can be checked independent of the application program. The Z8 8-bit single chip microcomputer provides this advanced feature with a special 64-word test ROM located on the chip. This development will lead to better fault isolation in the future, but its true value will be beyond the time frame considered for the SPUR.

Peripheral chips will see continued development in support of microprocessors. These support chips, such as memory management modules, are currently announced or are in development for all of the 16-bit second generation microprocessors. These LSI devices obviously aid the hardware development of a microcomputer.

4.5 MEMORY TECHNOLOGIES

Memory is a key area in the optimization of the SPUR because relatively large amounts of data are manipulated and stored in the processor. Memory technologies were investigated in four categories:

a) Random Access Memories (RAMs);
b) Charge Coupled Devices (CCDs);
c) Read Only Memories (ROMs);
d) Nonvolatile Memories.

The current and projected characteristics of each memory type are illustrated in Table 4-X. Most developments over the SPUR time frame are of an evolutionary nature. Increases in memory density per chip are expected in all areas except dynamic RAMs.

Random Access Memories – RAMs are generally required for the bulk of data storage. Some examples of this storage are collection of A/D data before Doppler filtering,

TABLE 4-X. CURRENT AND PROJECTED MEMORY SIZES SHOW INCREASING DENSITY FOR ALL TYPES EXCEPT DYNAMIC RAMs

	1978			1980	Candidate
	Size	Example	Mfr	Size	Usage
Random Access Memories (RAMs)					
Dynamic NMOS	64K	TMS4164	TI	64K	Doppler Processor
Static NMOS	8K	MK4118	Mostek	16K	Unit Memory
CMOS	4K	6504	Harris	16K	Clutter Map Memory
					Buffer Memory
Charge Coupled Devices (CCDs)					
	64K	TMS3064	TI	256K	Clutter Map Memory
Read Only Memories (ROMs)					
ROM	64K	S4264	AMI	128K	
PROM	16K	S82S190	Signetics	32K	Processor
UVEROM	32K	TMS2532	TI	64K	Program Memory
EAROM	8K	ER2805	GI	16K	
Nonvolatile Memories					
Bubble Memories	256K	RBM256	Rockwell	1M	Nonvolatile copy of Processor Program Memory
MNOS Semiconductor Memories	1K	NC7054	Nitron	4K	Nonvolatile copy of Processor Program Memory

9524-16

one candidate for the clutter map in the zero channel processor, and buffer storage throughout the processor. Since the memory requirements are somewhat different in each area, the optimum SPUR is developed by performing architecture, technology, and sizing tradeoffs separately in each area (see Section 6).

Three major trends, which are of particular interest to SPUR, are developing in RAMs:

a) Emphasis on production of currently introduced dynamic RAMs as opposed to announcements of higher density devices;

b) Emphasis on density increases in NMOS and CMOS static RAMs with power-saving features and faster speeds;

c) Chip organization changes from the current K words by 1-bit to more chips with L words by N bits.

Dynamic RAM densities of up to 64K-bits have already been announced. During the time period (between now and 1980), emphasis is shifting from the announcements of higher densities (256K-bit devices are not expected until 1981-2) to the production and delivery of 16K and 64K devices. This emphasis on production will drive the cost of these devices down the classic semiconductor production cost curve such that dynamic RAM systems will be the lower cost system when compared to static RAMs for memory sizes of 12K words and above. (Currently, economics show dynamic RAMs more cost-effective above 16K words and statics preferred below 8K, with the middle ground requiring a detailed analysis.) Of course, the optimal system considers more than cost, but the above guidelines aid in the selection process.

In static RAMs, the emphasis will continue to be on higher density, with an increase from the currently available 4K devices up to 16K devices. These devices also will start down the production cost curve in the time frame of interest, but progress is not expected to be as rapid as with the dynamic RAMs. An important additional feature being designed into new static devices is the power-down feature. When the chip is deselected, this feature tends to reduce the required power between 70 and 85 percent for NMOS devices and to make the standby power requirements for CMOS devices almost negligible. This feature is particularly important for memory systems which require only selected parts to be operational, such as a clutter map. In general, with a careful system design, the use of power-down causes minimal loss of access time. The actual time for power-up for a particular chip is on the order of the access time of the device, so the design key is to power-up slightly ahead of usage time. While power-down devices have a small cost penalty currently associated with them, this cost penalty is not entirely due to the power-down capability because the performance parameters (such as access time) of the chips are also superior to older designs. No future cost penalty is expected for these devices because the trend of the entire industry is to produce new devices with this capability.

With the increasing emphasis on power reduction and savings, CMOS memory technology will see heavy development. This work will be aimed not only at increased density to stay abreast of NMOS static density but also at increased speed (i.e., faster access times) for the devices. Current devices are about three times slower than NMOS devices, but this gap is expected to be narrowed during the 1979-1980 time frame.

The third major area of RAM development is of an architectural nature. With the proliferation of microprocessors, new memory chips will have organizations of L words by N bits, in addition to the standard K words by 1-bit. While this new organization is attractive, because it will reduce chip count in some systems as the chip density increases, it will create a potential problem relative to reliability of a system. In general, memories in

a highly reliable, fault-tolerant processor must be protected by some form of redundancy. In place of duplicating the entire memory, error correction codes are attractive because they require less hardware than memory replication. However, in memory chips organized as L words by N bits, memory error correction, using Hamming codes, is not straightforward because address decoding is located on the chip. If an address error occurs, the entire word can be in error in an unknown pattern; whereas, with 1-bit per word per chip, only a single bit can be in error. The single bit will be corrected by the memory error correction circuitry. With multiple bits per chip, error correction can be split up as shown in Figure 4-7, but this partitioning and correction may be more costly than desired. The key design task is to match the architecture of the memory system to the requirements.

Charge Coupled Devices – CCD memories are classed as semirandom access memories because their storage architecture onchip is in blocks or loops of data such that the sequential access times within a loop are quite good (~200 nsec) while access times between loops are slow. Therefore, for the SPUR, CCD memories have been considered for areas where data requirements are sequential in nature. The clutter map is the main area because data storage and retrieval can be set up as a very orderly process on a sector basis. This usage of CCDs is considered in Section 6. As shown there, CCDs require a RAM buffer to match the clutter map data rate to the CCD memory clock rate of 5 MHz. CCD memories of 256K bits per chip should be available in 1980, up from the current 64K. They provide a very high density storage medium for areas which require storage of large amounts of data.

CCD memories have unclear trends, at the present time, because of cost problems within the industry. These memories naturally fit between RAM memories on the high-speed side and mass storage devices on the slow-speed side. However, they must show definite cost advantages to make inroads into either market. An appropriate cost advantage would be at a bit cost of approximately one-fourth the bit cost of dynamic RAMs. This figure is suggested because CCD memories have a natural 4-to-1 density advantage over dynamic RAMs in the chip design. The development of a CCD memory chip is based on the design of the dynamic RAM and usually arrives about one year later. For example, 64K dynamic RAMs are now available in samples, and 256K CCDs can be expected in mid-to-late 1979. Up to the present time, the requirement for approximately one-fourth the cost has not been met by manufacturers, because the rapid development of dynamic RAMs has not allowed sales of enough CCD memories. However, this situation may change at the 256K level for CCDs, because of the increased development time required for the next level of dynamic RAMs. Thus, the 256K level will be the real testing area for the viability of CCD memory.

Read only memories (ROMs) provide one storage mechanization for programs driving programmable parts of the processor. The areas considered include Doppler processing, zero channel or clutter map processing, postdetection processing, and the STATE processor. While for large system quantities, mask-programmed ROMs provide the least costly approach, the quantities of the SPUR indicate that PROMs would be more cost-effective in the final

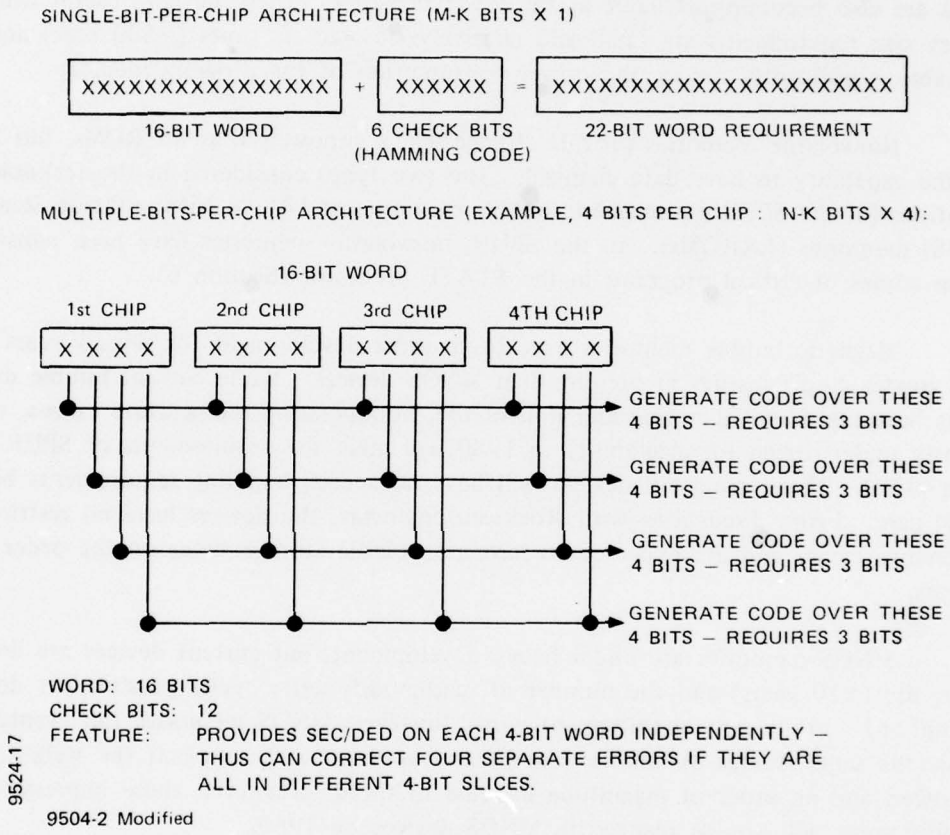


Figure 4-7. Memory Chips Organized N-K Bits × L Require More Protection Bits than Chips Organized M-K Bits × 1.

systems. During development, UVEROMs or ROM simulators (i.e., RAM storage loaded by a paper tape) would be used. The access time of Electrically Alterable ROMs (EAROMs), (also discussed below under nonvolatile memories) are presently too slow for the SPUR requirements.

The trends in ROMs are toward larger size and lower power consumption. NMOS devices are challenging bipolar devices, particularly at the higher densities, but their access times remain above those of bipolar devices which can be as low as 35 nsec. Some CMOS devices are also becoming available at the lower densities. These devices, useful where memory size requirements are small and relatively slow access times (~500 nsec) are acceptable, significantly reduce the power consumption of the program memory.

Nonvolatile memories provide storage when unpowered, as do ROMs, but they also have the capability to have data changed. The two types considered in the technology evaluations for the SPUR are magnetic bubble memories and Metal Nitride Oxide Semiconductor (MNOS) memories (EAROMs). In the SPUR, nonvolatile memories have been considered for backup copies of critical programs in the STATE processor (Section 6).

Magnetic bubble memories have been under development for several years and have much greater chip densities at present than MNOS devices. While current bubble memory devices have restricted operating and nonvolatile, nonoperating temperature ranges, the units currently under design for availability in 1980 will meet the requirements of SPUR (Table 4-XI). These projected devices will have no special handling requirements beyond normal care. From discussions with Rockwell engineers, the devices have no restrictions on data change cycles and are expected to have nonvolatile storage times on the order of 50 years.

MNOS memories are under heavy development, but current devices are limited by storage life (~10 years) and the number of read-modify-write cycles possible per device (~1 million). From early development work, however, MNOS memories can eventually provide the same storage as bubble memories at approximately one-half the weight, one-fourth the power, and an order of magnitude increase in speed. However, these impressive performance gains will not be realized in MNOS devices by 1980.

The trend for nonvolatile memories between now and 1980 shows these two technologies beginning to compete. However, in this near-term look, bubble memories are expected to see increasing usage, while MNOS devices will remain in heavy development. Beyond 1980, MNOS memories will make significant inroads into nonvolatile memory slots and, if the historical pattern of semiconductor technology displacing magnetic technology holds, bubble memories will be relegated to very specialized applications where extremely long hold times and many write/rewrite cycles are required.

TABLE 4-XI. TEMPERATURE LIMIT IMPROVEMENTS ARE PROJECTED FOR BUBBLE MEMORY DEVICES BY 1980

Device	Temperature Range	
Device	Operating	Nonvolatile, Nonoperating
Current 256K-Bit Units	-10°C to +70°C	-50°C to +100°C
Projected 1M-Bit Units	-40°C to +100°C	-55°C to +125°C

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Section 5

SIGNAL PROCESSOR ARCHITECTURE

5.1 INTRODUCTORY CONCEPTS

Computer architecture as a phrase enjoys wide usage within the computing community. However, different segments of the community, such as the system programmer segment, will tend to emphasize those aspects of an architecture most immediate to their own work and to deemphasize less immediate ones. Also, certain features of an architecture are sometimes intentionally made transparent to an entire class of users. This emphasizes the importance of defining the term signal processor ***architecture*** as it is used within the SPUR final report.

A machine architecture is defined as a conceptual framework in which a mapping is produced between a set of requirements representative of a problem to be solved, or of a capability to be provided, and a set of machine constructs capable of meeting those requirements. The flow of control and information within and between the elements of the set of machine constructs produces the solution to the problem or provides the required capability. This flow takes place according to a set of rules specified by the machine architect.

Implicit within this conceptual framework is the concept of levels. It is useful to distinguish four levels within an architecture at this time:

a) System level
b) Function or unit level,
c) Device level,
d) User level.

System, function or unit, and device levels provide increasingly detailed viewpoints of a particular architecture. This form of perspective allows two different systems to share a common architecture at, say, the system level, and to still have significantly different architecture at the function or device levels.

The user level is intended to encompass a wide variety of actual users such as a programmer or operator and of more abstract users such as cost constraints for which the system may be thought to provide services. Accordingly, a user may be thought of as another system or unit, a programmer, an operator, or even a maintenance operation.

Within the context of SPUR, the system level applies directly to the signal processor. Identifiable functions and/or units within functions in the signal processor correspond to the function/unit level. Several abstract users were explicitly recognized during the study, namely: the radar system, data processor system, and, through the tradeoff matrix, reliability, performance, cost, maintainability, risk and power functions.

5.2 REQUIREMENTS OF SIGNAL PROCESSOR ARCHITECTURES

Signal processor architectures can be distinguished from the class of general purpose digital computer architectures by the unique set of problems which signal processors are required to solve. Although the problem set is restricted, the associated signal processing rates expressed as input/output data rates, memory access rates, and arithmetic processing rates are usually so high that most general purpose computer architectures are not, in fact, suitable for handling a signal processing problem of even modest proportions. A set of typical qualitative processing requirements for a signal processor is provided in Table 5-I.

Requirements of the type identified in Table 5-I can be met by a number of alternative architectures. However, some form of concurrent processing will be necessary to meet the heavy arithmetic processing requirements. Further, since the signal processing algorithms are both restricted and well defined (for a given application), some form of functional, sequential partitioning along a pipeline can prove to be efficient. This is why, traditionally, high performance signal processors have been designed as functionally distributed pipeline processors. The more closely the pipeline is tailored to the specific requirements of a given signal processing requirement, the more efficient it becomes in that application and the less applicable it becomes for other signal processing tasks.

TABLE 5-I. COMMON REQUIREMENTS OF SIGNAL PROCESSORS
which distinguish their architectures from general purpose digital computers

Moderate to High Precision/High Bandwidth Analog-to-Digital Converters
High to Very High Real Time Input Data Rates
High to Very High Memory Access Requirements
Moderate to Very Large Memory Requirements
Well-Defined Processing Algorithms with Heavy Arithmetic Processing requiring only Limited Precision

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5.3 IMPACT OF A FAULT TOLERANT REQUIREMENT ON SIGNAL PROCESSOR ARCHITECTURES

In addition to the conventional processing requirements for a Signal Processor, the SPUR must also provide a high degree of fault tolerance to satisfy the user level requirement of an MTBF in the 20,000- to 100,000-hour range. The impact of a fault tolerant requirement on the architecture of a pipeline signal processor is summarized in Table 5-II.

Fault tolerance rules out a single thread pipeline architecture in favor of the use of parallel, redundant structures within a pipeline architecture. In a fault-tolerant design, the pipeline is optimally partitioned into blocks of approximately equal failure rate such that selective redundancy can be provided in each block so as to maximize the MTBF for a given cost/power level. Thus, the type of redundancy is optimized for each application area.

TABLE 5-II. A FAULT TOLERANCE REQUIREMENT IMPACTS THE ARCHITECTURE OF PIPELINED SIGNAL PROCESSORS

Fault Tolerance:

- Rules Out Single Thread Pipeline Architectures
- Favors the Use of Parallel, Redundant Processing Structures within a Pipeline Architecture
- Favors Paritioning into blocks of Equal Failure Rate with Selective Partial Redundancy Added
- Favors Distributed BITE with Centralized Control of Fault Tolerant Features

9524-31

The effectiveness of selective redundancy is directly limited by the coverage provided in the fault detection system. Accordingly, a truly fault tolerant system requires a very high level of fault detection, fault-isolation, and fault correction coverage. The SPUR architecture provides for this coverage through the combination of distributed BITE (built-in-test equipment) with centralized switching and monitoring of the selectively redundant fault tolerant units.

Distributed BITE has several advantages not provided by centralized BITE. These advantages include:

a) Better fault isolation;
b) Simpler testing of the BITE circuits themselves;
c) Use of low level, distributed testing which results in simpler tests.

In the SPUR, the distributed BITE is monitored and controlled by a centralized STATE (Status, Transformation, and Test Evaluation) processor, which is a highly reliable unit that is tasked with validating the status of the signal processor system. The STATE processor performs this validation by monitoring the results of the distributed BITE, initiating special tests when required, switching in redundant units as required in the event of a failure in one of the partitioned blocks of the system, and retaining the status of the processor blocks (see Section 6).

5.4 ALTERNATIVES IN SIGNAL PROCESSOR ARCHITECTURES

Representative alternative structures for signal processor architectures at the system and function/unit levels are summarized in Table 5-III for processor, storage, control, input/output, and communication functions.

During the SPUR study, tradeoffs of alternative machine structures were made for both the system level and unit level. Results of these tradeoffs are presented in Section 6, which reports on the proposed optimum processor for the SPUR.

TABLE 5-III. AN ARCHITECTURAL FRAMEWORK SELECTS BETWEEN ALTERNATIVE MACHINE STRUCTURES

Processor Structure Alternatives

Centralized vs Distributed

Functional (dedicated) units

Pipeline

Parallel (Multiple Instruction Stream/Multiple Data Stream (MIMD))

Array (Single Instruction Stream/Multiple Data Stream (SIMD))

Storage Structure Alternatives

Serial Access vs Random Access

Hierarchies (scratch pad, cache, bulk)

Stacks (Last In First Out – Push Down)

Buffers (First In First Out)

Control Structure Alternatives

Fixed logic (sequential state machines)

Microprogrammable

Programmable

I/O Structure Alternatives

Signal Conditioning

Discrete Programmed vs Buffered/Direct Memory Access

Communication Structure Alternatives

Buses

Cross Bar Switches

Interrupts

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General conclusions on the applicability to Signal Processors of alternative machine structures are summarized here on a major category basis:

a) Processor Structures – Pipeline structures are most applicable. Parallel/array structures within the pipeline provide for the required degree of fault tolerance.

b) Storage Structures – The high failure rate of memory encourages optimal use of the memory function. General purpose bulk memory organizations are too inefficient to provide the required access rates for signal processing applications. Distributed memory organizations with dedicated memory for major processing functions are required.

c) Control Structures – Control structures tend to be device driven. Microprocessor-based units use programmable control structures. Dedicated special purpose units use sequential state control structures.

d) I/O Structures – I/O structures are closely related to storage structures. General purpose structures are not required in signal processing applications. Special purpose I/O structures are more efficient in providing the high input data rates required in signal processing applications.

e) Communication Structures – Bus structures provide required fault tolerant data paths for connecting parallel redundant units.

5.5 CANDIDATE SIGNAL PROCESSOR ARCHITECTURES

Selection and development of the SPUR architecture is one key to successful optimization of the processor. Three system level architectures were considered:

1) A pipeline of specialized functional processor units with fixed logic control structures (Figure 5-1).

2) A pipeline using two or more types of processor units in which each processor unit type is configured using bit slice microprocessors, and in which a microprogrammable control structure is used in each processor unit type (Figure 5-2).

3) A pipeline using a single processor unit type in which the processor unit is configured using a common 16-bit microprogrammable processor (Figure 5-3).

5.5.1 First Architecture Candidate

The first architecture is characterized by fixed specialized designs which, in general, are hardwired. This architecture is attractive in a minimized design because each function and every interface can be optimized. However, flexibility in the processor is essentially lost because changes require redesign of the hardware and interfaces to the new configuration. These changes can be difficult and costly in a previously minimized system design.

5.5.2 Second Architecture Candidate

The second architecture, using two or more programmable bit-slice based processors, optimizes the processor modules for the type of task being performed. In the SPUR, in this type of architecture, there is a natural break by area into two processor types: a) a high speed, relatively unsophisticated processor for performing the fast Doppler filtering at the front end of the processor, and b) a medium speed, more general-purpose processor for performing the more varied processing following the Doppler filtering. In this second area the data rate has been reduced by a factor of 8 by the coherent processing of the front end.

In the front end, speed is attained by operating the processors in parallel, all performing the same task. These processors would all be controlled by the same instruction stream. An example of this type of processor is the ITT Gilfillan developed Array Processing Module (APM). Three processors per board operate in parallel to achieve high throughput. In

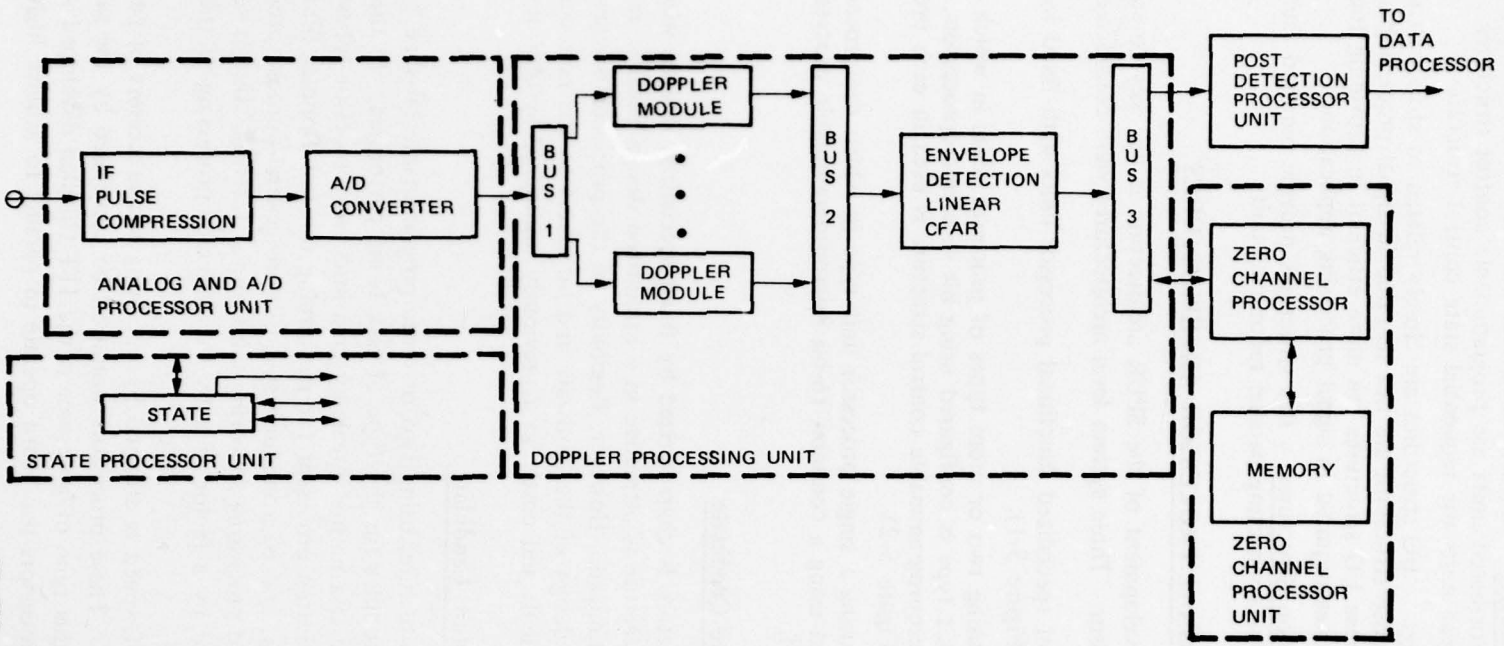


***Figure 5-1. The First Architecture Candidate for the SPUR** uses fixed logic to implement the functional blocks*

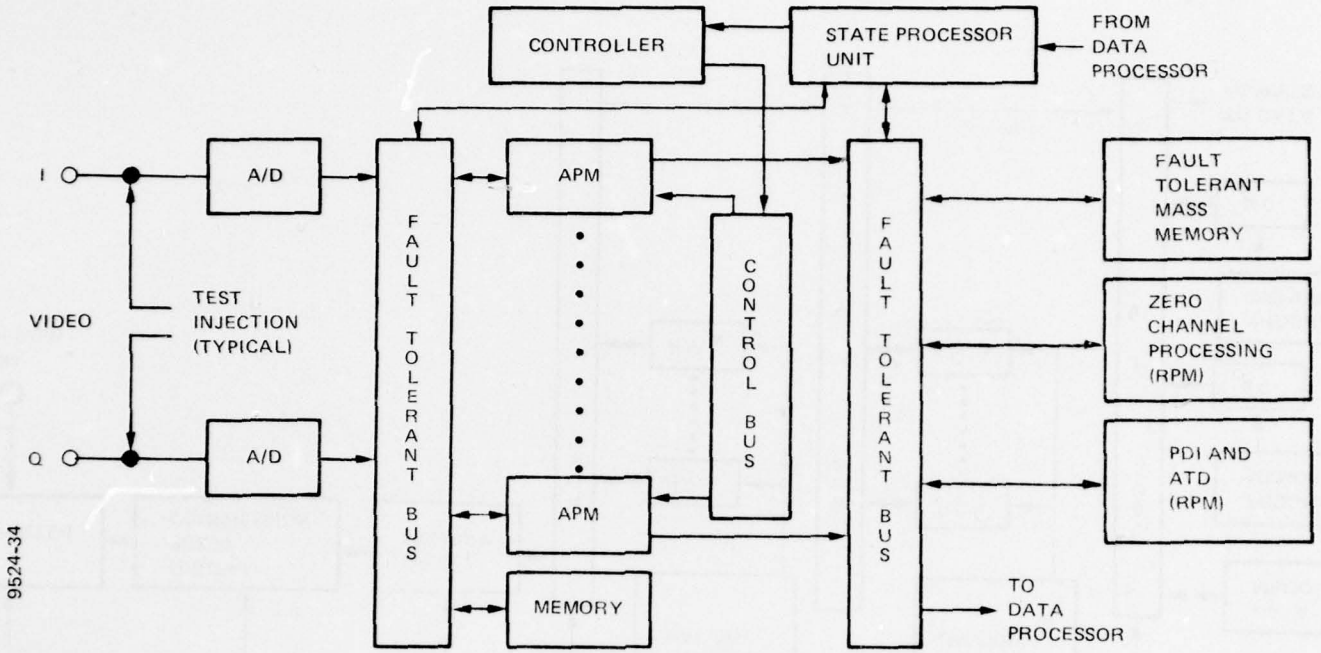


Figure 5-2. Two Separately Optimized Programmable Modules (APM and RPM, see text) *are used in the second candidate architecture for the SPUR*

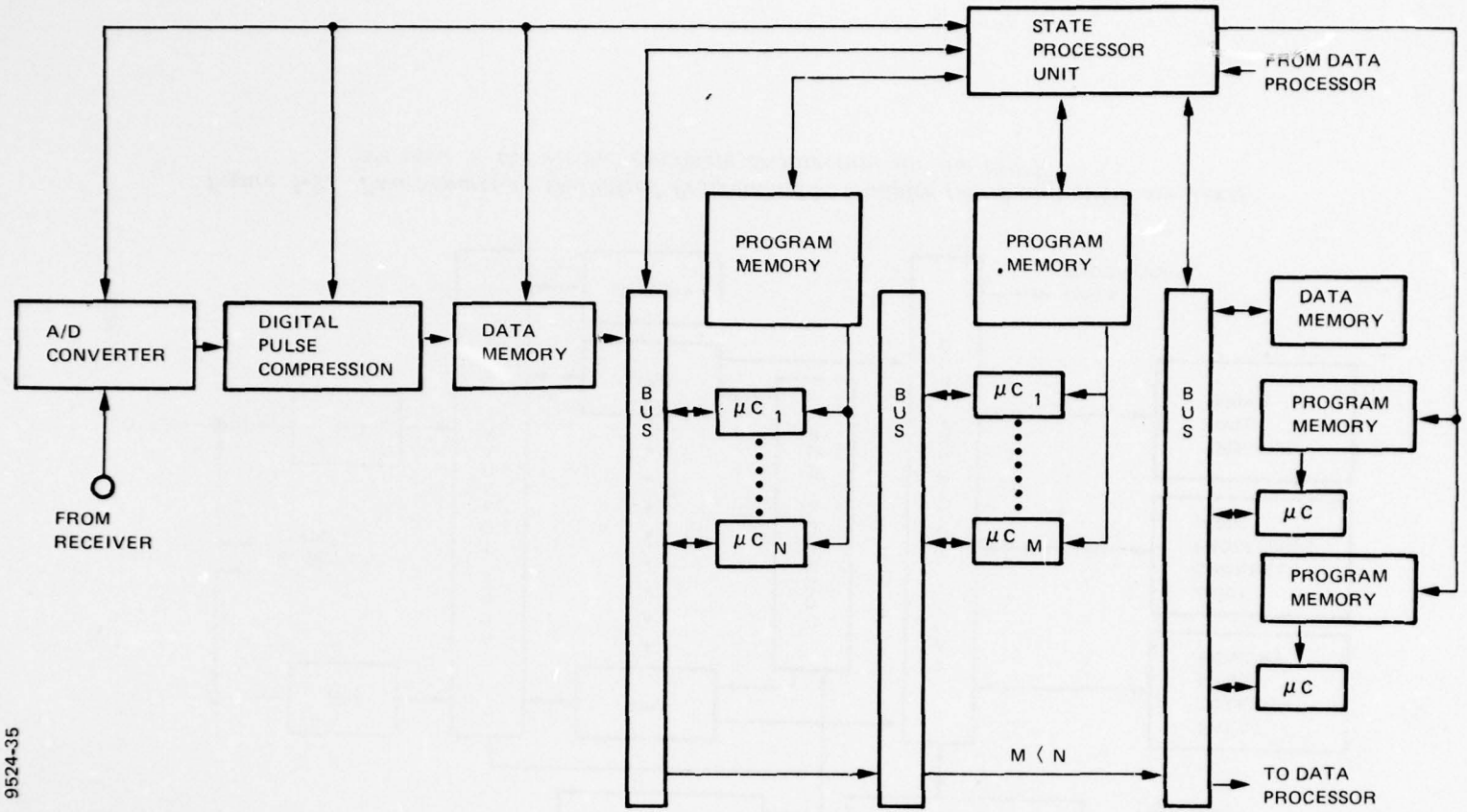


Figure 5-3. A Single Type of Programmable Module Forms the Hardware Basis *of the third candidate architecture for the SPUR*

FFT implementations, the APMs can be cascaded to increase the order of the processor. An example of this type of processor which was considered for the Doppler modules is discussed in Section 6.

Post-Doppler filtering processing is characterized by medium-throughput, bit and word-oriented processing. A slower speed, more general purpose processor is applicable to this area. The ITT Gilfillan developed second generation Radar Processing Module (RPM-II) was evaluated in this area. This unit, through its wide control word, has the capability for several parallel operations on a single clock. With several input-output ports, this processor is very versatile in post-Doppler filtering processing.

5.5.3 Third Architecture Candidate

The third architecture, using a dedicated 16-bit microprocessor throughout the system, is attractive because the hardware is standardized. The microprocessors are programmed within a block to perform the same tasks. Thus within blocks, the architecture becomes highly distributed since all data does not pass through all microprocessors. The distinction among groupings of processors is the number of processors required to accomplish the tasks. As an example of a processor which may be used in this architecture, the MC68000 has been evaluated. It is representative of second-generation, 16-bit units available within the time frame of interest. During this evaluation, it became clear that the speed of the MC68000 is not adequate for front-end processing (i.e., the number of MC68000's required becomes excessive). Thus the consideration of this architecture then became comparison of this device with the RPM-II for post-Doppler filtering processing.

As has been discussed, at the system level each architecture is configured as a pipeline processor, but each system architecture differs in the number, type, and interconnection of units required. All architectures utilize: 1) a fast analog-to-digital converter unit for digitizing the input data at a rate of two samples per range bin, and b) the STATE processor unit for centralized operation of the fault-tolerance features of the system. During the study these architectures were developed and compared from the system, function, device and user viewpoints. The optimum processor architecture, described in detail in Section 6, is a combination of these architectures.

Section 6

DESCRIPTION OF OPTIMUM PROCESSOR

6.1 OPTIMUM PROCESSOR SPECIFICATIONS AND CHARACTERISTICS

The recommended optimum SPUR is a unified solution providing the required signal processing for a modern, 2D gap-filler type of unattended radar operating in severe clutter in a harsh environment. The specifications for the SPUR illustrate that the goals for the unattended radar processing parameters have been met or exceeded in most cases by the recommended design (see Table 6-I).

For development of the SPUR, five functional areas were defined (Figure 6-1). The detailed optimizations of each function are described in subsequent topics in this section. This optimization for each functional area was based on the SPUR weighting matrix (Table 6-II). In order to obtain values from this matrix, data in each category was normalized to the more desirable alternative and multiplied by the weighting factor before final summation. Thus, the ***lowest*** score in the comparisons points to the recommended alternative.

The recommended SPUR is shown in the block diagram of Figure 6-2. This functional block diagram locates each unit of the processor within its designated function. The characteristics of each function (see Table 6-III) give a detailed look at the functional aspects of the recommended SPUR. The next section discusses the fault-tolerant features of the recommended SPUR.

The Analog-to-Digital Converter System, providing 11-bit resolution and accuracy, has several special features. It operates at a 1.62 MHz sample rate, thereby providing two samples per range bin. Each A/D converter has a dc stabilization loop around it to correct for long term drift of the zero level. The I and Q words are Hamming encoded for single error correction/double error detection before being sent to the Doppler Processing Function. Since the A/D converter system is packaged on a single board, it performs its own BITE and reconfiguration in conjunction with requests from the STATE Processor. A function generator is located on the board for test purposes and this generator can be commanded by the STATE Processor for test target generation for the entire processor.

The selected Doppler Processing Function consists of two units: 1) the Doppler Modules and 2) Postfiltering Processor. The Doppler Modules implement the recommended Near Optimum Filter Bank consisting of six filters including the zero filter. These six filters are generated from nine pulses in the coherent group. Each Doppler Module, (three are active at one time), generates the six filters for 1/3 of the range bins. A double-buffered memory for the process receives the encoded I and Q data from the A/D converter function.

TABLE 6-I. OVERALL SPECIFICATIONS FOR THE SPUR define an advanced, highly reliable signal processor

Specification	Goal	SPUR
Range	5–60 nmi	5–60 nmi
Range Resolution	0.1 nmi	0.1 nmi
Land Clutter Improvement Factor	>50 dB	50.9
Pulse Compression Ratio	32:1	31:1
FFT	8-Pulse Optimum Weights	Narrowband Near-Optimum
MTI	3 Pulses	Filter Bank operating on 9 Pulses
Range Average CFAR	32 Sample	31-bit hard limited pulse compression
Clutter Map	Zero Velocity Superclutter/ Intraclutter Detection Processing	Zero Velocity Intraclutter Detection Processing
Postdetection Integration	4 Samples	4 Samples
prf's	2 Available	4 Recommended
MTBF	20,000 to 100,000 hours	22,331 hours
Power	Minimize	226W
Processing Gain	–	0.15 dB Worst Case
Maintainability	For unattended operation in remote, harsh environments	Remove and replace concepts

9524-74

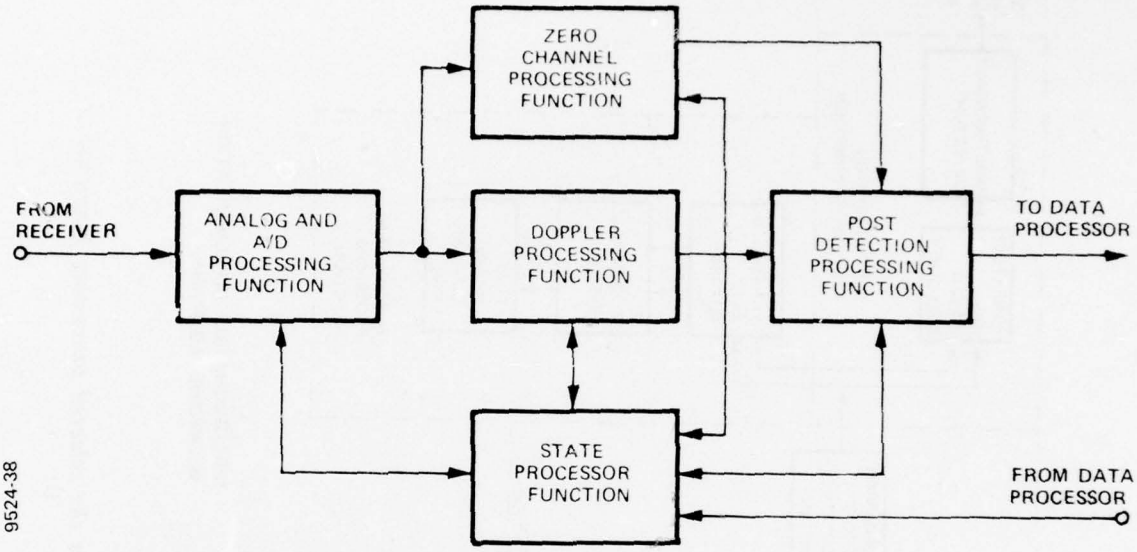


Figure 6-1. The SPUR Consists of Five Generic Functions

TABLE 6-II. THE SPUR WEIGHTING MATRIX WAS USED IN OPTIMIZING EACH FUNCTION

	Weighting	Comments
Reliability	10	Fault-Tolerant Design*
Performance	10	Meet Requirements
Cost	7	60 Systems
Maintainability*	6	Remove and Replace Concept
Risk	6	Near Term Requirement Reduces Risk
Power	5	Minimize

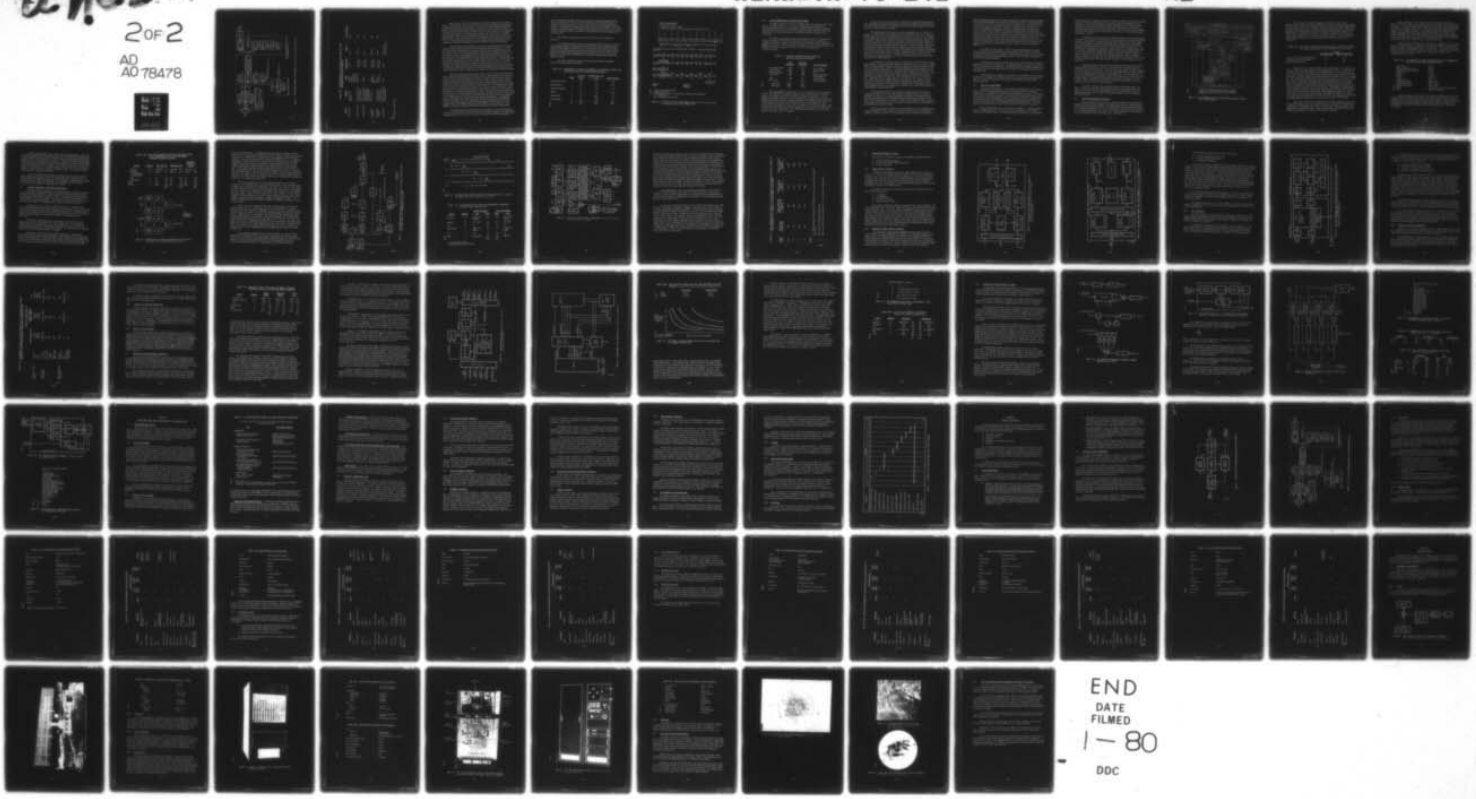
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*Fault-tolerant design improves maintainability.

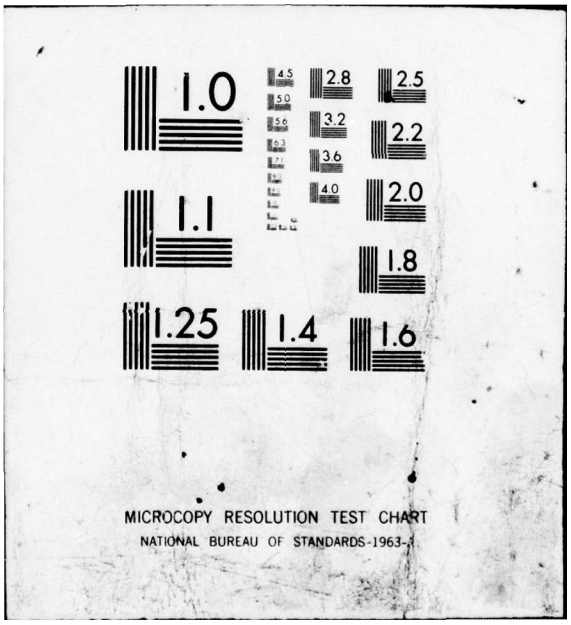
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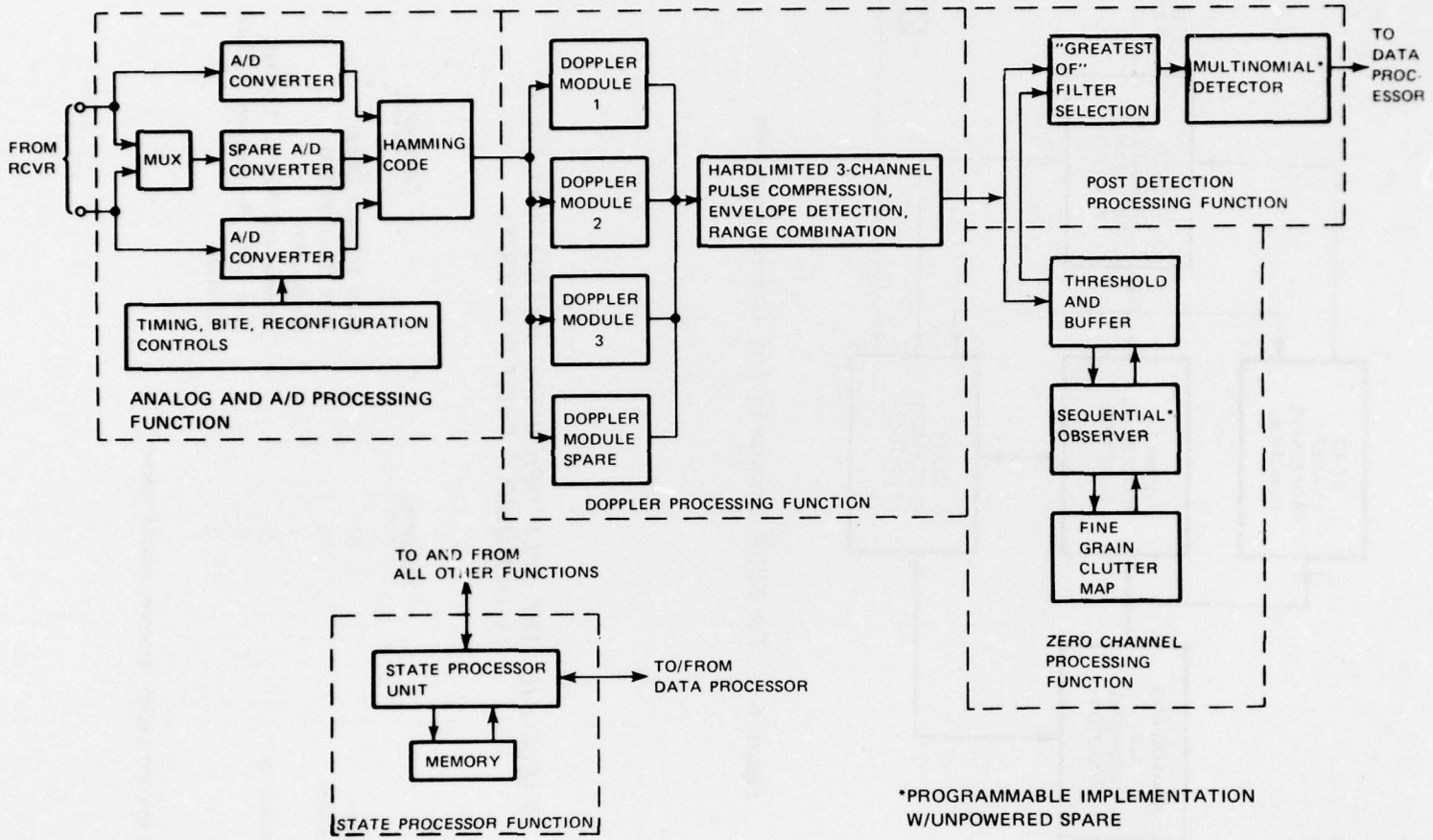
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9524-71

*Figure 6-2. **Overall Block Diagram of the SPUR** defines the selected processing functions*

TABLE 6-III. CHARACTERISTICS AND SPECIAL FEATURES OF THE RECOMMENDED SPUR FUNCTIONS

Function	Algorithm	Speed	Dynamic Range	Memory	No. of Instructions
A/D Converter	Two-step Flash Converters	1.62 MHz I and Q (Two Samples per Range Bin)	11-bits	None	None
Doppler Processing	Near Optimum Filters (9 pulse coherent group – 6 filters)	4.85 MHz rate	11-bits input, 1-bit output	917K bits	None
Doppler Processing	Hard limited 3-channel Pulse Compression, Envelope Detection Range Combination	1.82 MHz	1-bit input 6 bits output	None	None
Zero Channel Processing	Censor Process	3.6 μsec/ Clutter Map Cell	6-bits input Clutter Map	819K bits	280
Postdetection Processing	Sequential greatest of across filters multinomial detector	4.6 μsec/ resolution cell	6-bits input 1-bit output	4K bits	155
State Processor	Status, Transformation and Test Evaluation	5 MHz	16-bits	2K words data 16K words program	*

*Depends on detailed design.

9524-75

Since the data is stored in this RAM with the position determined by the number of clocks from transmit time, this memory effectively performs the destagger function required on a group-to-group basis for as many staggers as are active in the system. Before the filters are generated, the Hamming encoding is removed, with any error sent to the STATE Processor. The filters are generated by eight complex multiplies and seven sums performed in two multiplier/accumulators per module. The resulting data is available to the STATE Processor for BITE operation and the MSBs are sent to the Postfiltering Processor. Fault tolerance features of the Doppler Modules are discussed in Section 6.2. Each Doppler Module is packaged on a single 14 in. x 15 in. board and, therefore, four boards are required for the SPUR. Because of this packaging, all reconfiguration and BITE requests are performed by the STATE Processor.

The Postfiltering Processor (PFP) unit receives the hard-limited data from the Doppler Modules in range bin order and performs 31-bit hard limited pulse compression on it. This pulse compression is performed in the equivalent of three channels by splitting the code into two sections, 15 and 16 bits, performing antiphase rotations and recombining the sections. The three outputs are sent to a greatest-of circuit for selection of the maximum response in the pulse compressor. After pulse compression, which also provides CFAR, the I and Q channels are combined in an approximation to an envelope detector, max [|I|, |Q|] + ½ min[|I|, |Q|], and then the two samples in range are added to obtain a single sample per range bin. Six bits of resolution are provided at this point. The PFP is located on one 14 in. x 15 in. board. It is monitored by the STATE Processor but contains no reconfigurable functions since its failure rate is relatively low. BITE signals are provided to the PFP such that the pulse compression can be checked independent of the test target generator. Results are evaluated by the STATE Processor.

When the zero filter is processed by the PFP, it is sent to the Zero Channel Processor. This processor performs control on the zero filter such that, when ground clutter is present, its output is censored from the Postdetection Processor. The Zero Channel Processor consists of a Censor Process and a fine grain clutter map. The Censor Process, using a sequential observer technique, determines when ground clutter is present in a particular clutter map cell. The fine grain map is provided to store the results of this determination for cells throughout the coverage area of the radar. The clutter map cell size is 3/4° x 0.4 nmi (i.e., one coherent group by four range bins) and 2^{16} map locations are provided. When clutter is present in a cell, the output of the zero filter to the Postdetection Processor is censored. The zero filter output is gated by the condition of the cell in the map based on previous scans. However, the current zero filter output is also thresholded and used to update the sequential observer censor process for the following scan. The Zero Channel Processor has the Censor Process implemented in a programmable processor, the RPM-II. The clutter map, program memory and interfacing to the RPM-II are located on an interface board. The STATE Processor controls the BITE operations of the interface board, extended BITE requirements for the RPM-II, and test evaluation. A spare RPM-II is provided for redundancy and the STATE processor controls this reconfiguration.

The Postdetection Processor (PDP) receives six-bit data from the PFP from all filters except the zero filter (which comes via the Zero Channel Processor Function). The PDP performs the greatest-of function across the five or six filters and performs multinomial integration over

one azimuth beamwidth (4-hits). The greatest of function is performed sequentially for the filters. The greatest of function and the first thresholds of the multinomial detector are performed on hardware located on the same interface board as the Zero Channel Processor hardware. The remainder of the multinomial process is performed in the RPM-II. The output results (i.e., threshold crossings) are stored in a shift register on the interface board. The data processor accesses them there. The STATE Processor handles BITE and reconfiguration for this unit as well.

The STATE Processor, located on one 14 in. x 15 in. board, is discussed in Section 6.3.

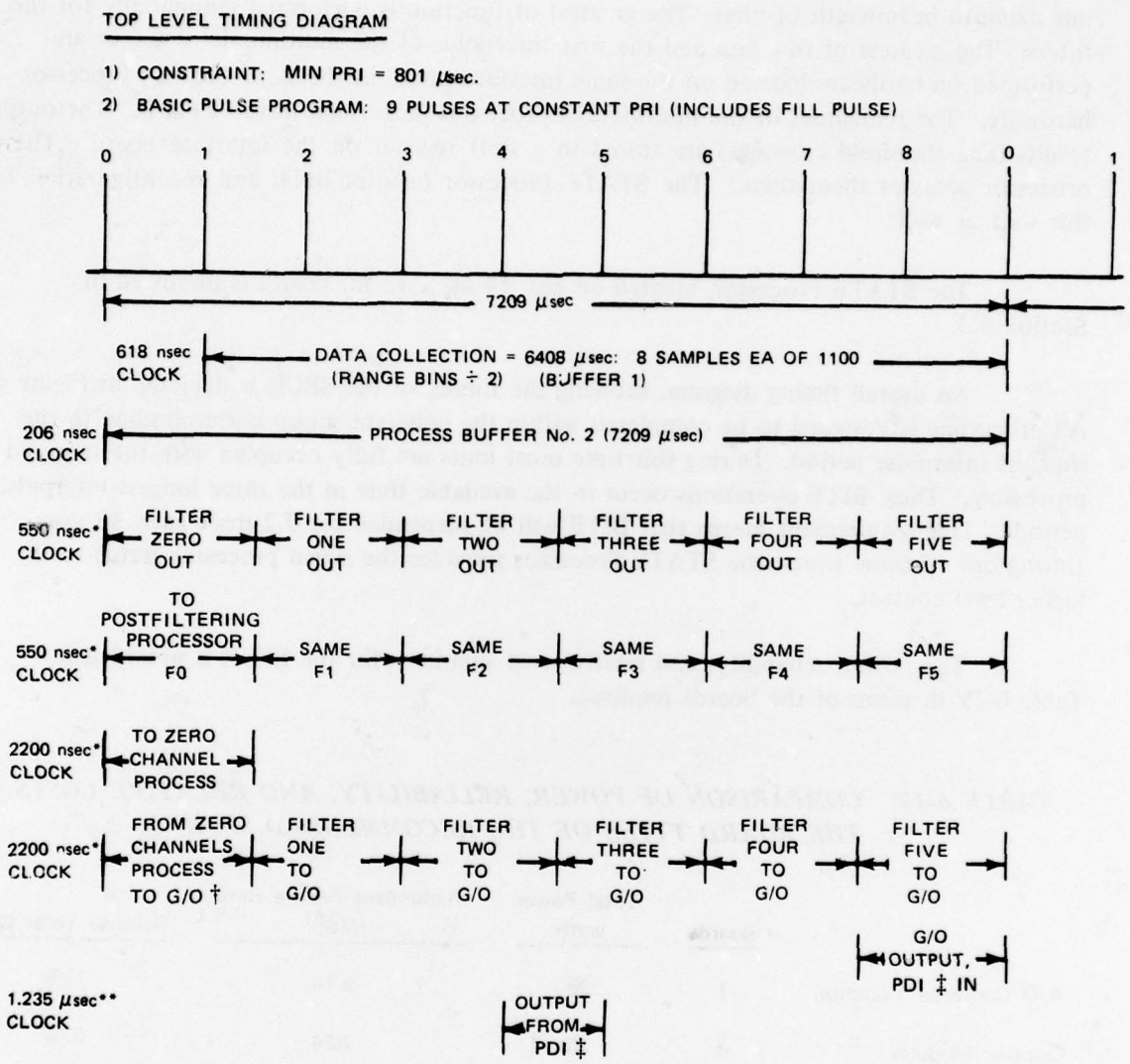
An overall timing diagram, showing the timing of the SPUR is depicted in Figure 6-3. All processing is designed to be completed within the coherent group corresponding to the shortest interpulse period. During this time most units are fully occupied with the required processing. Thus, BITE operations occur in the available time in the three longest interpulse periods. This requirement means that BITE will be suspended for 7.2 msec each 38 msec. During one of these times, the STATE Processor provides the signal processor status to the higher level control.

The power, reliability, and relative cost summary for the SPUR is provided in Table 6–IV in terms of the boards required.

TABLE 6-IV. COMPARISON OF POWER, RELIABILITY, AND RELATIVE COSTS FOR THE BOARD TYPES OF THE RECOMMENDED SPUR

	Boards	Total Power watts	Redundant Failure Rate $f/10^6$	Relative Total Cost
A/D Converter Function	1	38	9.14	13%
Doppler Modules	4	75	7.24	37%
Post Filtering Processor	1	16	7.39	4%
RPM-II	2	40	1.21	22%
Interface Board	1	35	15.80	13%
STATE Processor	1	22	4.00	11%
	10	226	44.78	100%

9524-77



9524-76

* NOTE: SMALL SKEW NOT SHOWN

** CORRECTION FOR SKEW

*** TIME AVAILABLE FOR BITE = 1602 μsec, 4005 μsec, 4806 μsec WITH PROPOSED PRTs.

† G/O = GREATEST OF

‡ PDI = POSTDETECTION INTEGRATION

Figure 6-3. ***An Overall Top Level Timing Diagram*** *illustrates the processing occurring in each processor unit for the minimum PRI*

6.2 FAULT TOLERANCE FEATURES OF THE SPUR

The SPUR is optimized to meet the reliability goals of an unattended radar. These goals are met through the use of: a) processor partitioning into modular units, b) selective redundancy within the modular units, c) distributed BITE to discover and isolate faults within the processor, and d) a STATE Processor to perform centralized control and monitoring of the status of the processor. The STATE processor is discussed in the next section.

The SPUR is partitioned into blocks along functional lines with consideration for potential redundancies for reduction of failure rate. Six basic areas are defined in the reliability block diagram. Table 6-V lists these areas and the chosen type of redundancy, if applicable, in each area. All time dependent calculations are based on 3-month intervals. The MTBF of the SPUR is increased by a factor of 6.9 over a non-fault-tolerant equivalent processor.

TABLE 6-V. SELECTIVE REDUNDANCIES APPLIED TO ACHIEVE REQUIRED RELIABILITY

	Serial Failure Rate	Redundancy Failure Rate	Type of Redundancy
A/D Converter System	41.81	9.14	2/3 Hot Standby
Doppler Modules	146.86	7.24	3/4 Cold Standby
Postfiltering Processor	7.39	7.39	None
Interface Board	96.05	15.80	Clutter Map SEC/DED and Spare Bank
RPM	16.06	1.21	1/2 Cold Standby
State Processor	—	4.0	TMR, Dual Memories
$\lambda(f/10^6$ hours)	308.17	44.78	
MTBF (hours)	3245	22,331	

9524-90

The Analog-to-Digital Converter uses a 2 out of 3 architecture with all units always powered. This redundancy was selected because the A/D converters require five different voltages for operation, and the risk in switching all of them to apply power to a cold standby was considered excessive. Since all A/D converters are located on one board, reconfiguration among the three units is internally controlled. The STATE Processor monitors the status of the units and requests test target generation and extended BITE tests. One extended BITE test generates a sequence which is registered as a failure by the BITE. This test checks the BITE circuitry and causes reconfiguration to occur which allows operation and checkout of the spare A/D converter. The STATE processor initiates a reset of the A/D converter system after the test is complete.

After the A/D conversion is made, the I and Q data is encoded using a Hamming code. This Single Error Correction, Double Error Detection (SEC/DED) code, added to protect the Doppler Module Memories, is implemented at this point to provide single error correction across the bus interface between functions.

The Doppler Modules, in addition to having the SEC/DED code on memory, are arranged in a cold standby configuration of three active modules and one spare. Since each module occupies one full board, the STATE Processor monitors the status of active modules and the BITE results, requests extended BITE, and controls the reconfiguration upon discovery and isolation of faults. Power switching is controlled by the STATE Processor through a set of relays arranged to provide redundancy against the most likely failure modes. Relays are thought of as unreliable components but their failure rate is a strong function of the number of operations and since this will be small (two operations per day for checkout yield only 180 operations in 90 days, and this is reduced if the redundant unit is required operationally), they are the recommended switching mechanism. Independent relays will apply power to one module and remove it from another. A backup method for deleting a module from the processor chain without removing power exists since the module outputs are tristate devices controlled by the STATE Processor.

Any module may be placed in any set of ranges since the STATE Processor assigns logical addresses to the modules, which controls the timing. Thus, even after failure of more than one module, degraded operation is possible by placing the remaining modules or module at the most important range position. The Doppler Modules sample the incoming data from the A/D converter in range blocks; i.e., contiguous range samples until the memory is full. This sequence is used to preserve pulse compression even in degraded operation modes. If the sampling were interleaved, relatively large sidelobe responses would appear after pulse compression when one module has failed (i.e., every third range bin stuck at zero or stuck at one). BITE signals for the Doppler Module are injected into the multiplexers located just prior to the complex multiplier functions. This injection allows checkout of the filter function independent of the Hamming encoded input data. In addition, a uniform weights program and other test programs can be requested by the STATE Processor from the weight PROM for extended BITE tests.

The Postfiltering Processor has a relatively low serial failure rate and hence no redundancy was added to this unit. BITE signals are injected at the input to the pulse compressor such that it can be tested independent of the processor test target generator. Since the pulse compressor is three-channel, degraded operation is possible when a failure occurs in the separated parts of the channel. In this case, the STATE Processor can use the tristate registers to allow only one or two channels to remain operational. The probability of this degraded mode occurring is small.

The interface board contains the I/O to the RPM-II for the Zero Channel Processor and the Postdetection Processor. Most of this logic is in small amounts not amenable to redundancy techniques. However, the fine grain clutter map is located on this board and it

requires redundancy protection. This protection is provided by a Single Error Correction/Double Error Detection (SEC/DED) code and a spare partial memory bank. The STATE Processor controls the use of the spare partial memory bank on notification of a double fault by the error detection code. The spare bank remains in a nonselected mode when not in use (i.e., it is not completely unpowered). This choice is possible because the clutter map memory is CMOS and the standby power drain is exceptionally small. In addition, each active bank of the memory is power programmed by its chip select line such that only one memory bank of four is powered at any time except for short changeover times. The STATE Processor requests BITE tests on the logic of the Postdetection Processor and the Zero Channel Processor plus test cases of the entire processors. A continual memory test is also performed by reading and writing a known value sequentially into all of the memory cells. This test is performed over a long period of time, i.e., several seconds as a background BITE test.

The RPM-II, a microcomputer, contains a resident diagnostic program memory (2K words) which performs standardized data manipulation and I/O checks. The STATE Processor monitors these checks and requests extended BITE when required. It also performs reconfiguration when the operational RPM-II has failed. Power switching is performed as described for the Doppler Modules.

Degraded mode operation is possible when the Zero Channel Processor has failed by disabling the output of the zero filter (i.e., not allowing transfer to the greatest of circuitry when the clutter map is not operational). The STATE Processor controls this degraded mode. It should be noted that this degraded mode can be used in sectors should some part of the map malfunction.

Dual redundant power supplies for the SPUR are recommended to attain reasonable reliability. These supplies must be isolated so that a failure in one will not bring down the others. The current requirements are not excessive for the SPUR by modern digital processing standards.

6.3 THE STATE PROCESSOR

The Status, Transformation, and Test Evaluation (STATE) Processor is the unique feature of the recommended Signal Processor for the Unattended Radar. It provides a centralized focus on reliability for overall processor configuration and control. This selection assures cohesive operation and reporting for the SPUR because the STATE Processor conveys the total status of the signal processor to the data processor and beyond. It performs the monitoring of all units of the SPUR and the reconfiguration control on all but the A/D converter system which has its own built-in BITE for reconfiguration control. The STATE Processor's interaction with the rest of the Signal Processor was described in Section 6.2.

Since the STATE Processor is at the heart of the SPUR, it is extremely important that it be a highly-reliable unit. To this end, the specified failure rate for the STATE Processor is 4.0 failures/10^6 hours. The detailed design of the SPUR must use a programmable

unit because it must be amenable to change as experience is gained in its interaction with the units of the SPUR. The recommended basic processor for the STATE Processor is the MC68000 in a Triple Modular Redundant (TMR) configuration, such that three processors perform the same task and the results are voted upon. The program memory must be duplicated with a hardware switch-over capability and a hardware power-on startup capability. The STATE Processor having these features fits on one 14 in. x 15 in. board and consumes approximately 22 watts.

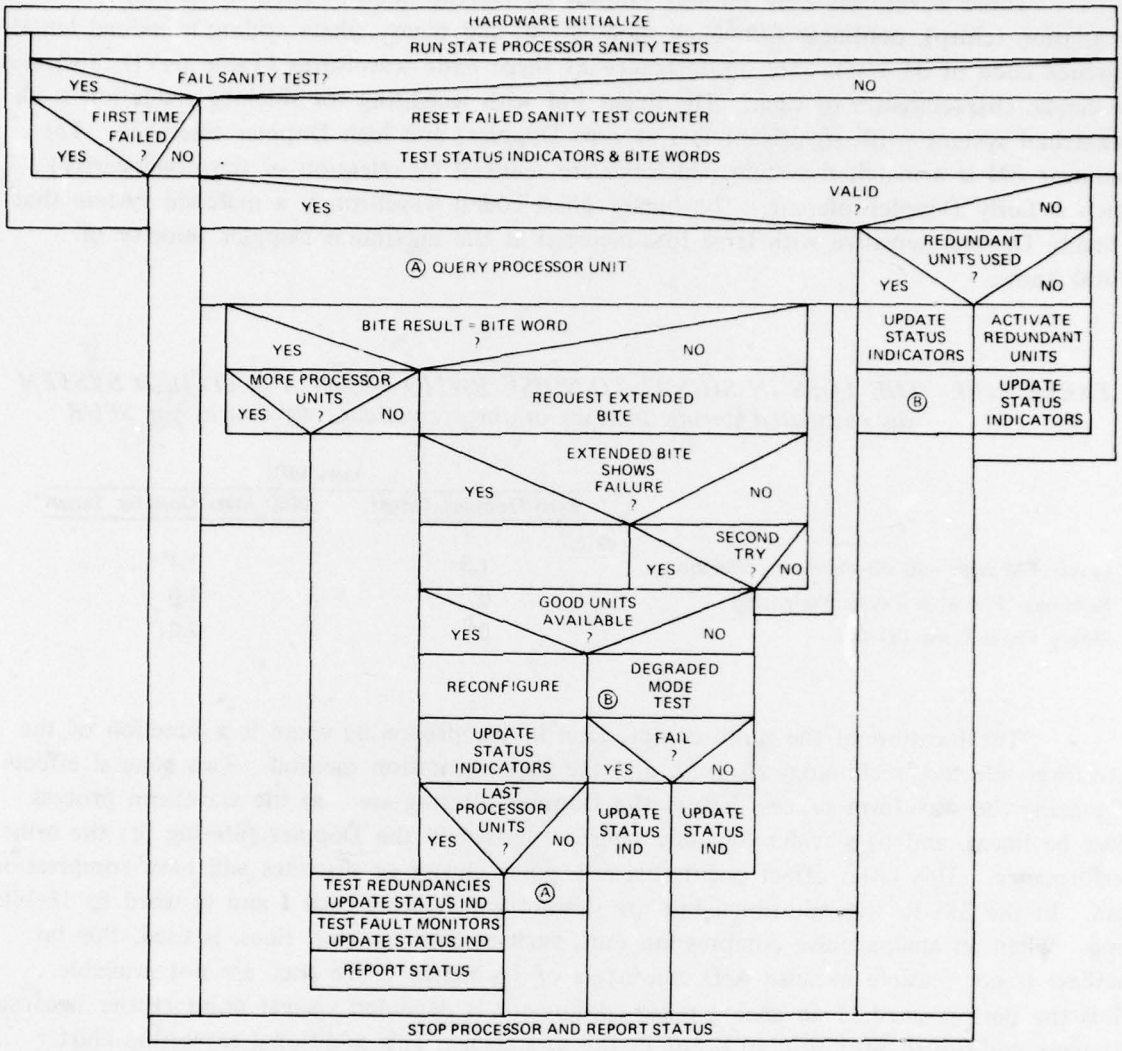
A flowgraph for the operations of the STATE Processor (Figure 6-4) illustrates the interactions of the functions of the processor. Its basic operation is to monitor the processor operation by comparison of the BITE results with stored expected results for the specific tests. When these tests are failed, extended BITE tests are performed for fault isolation leading to reconfiguration of the processor to replace failed modules with spare ones. In addition to the continual BITE operations, the STATE Processor occasionally injects a fault into a function through the extended BITE routines to test the fault monitoring logic. If a fault is not recorded, the monitors may be stuck at good and be unable to detect any faults. Additionally, the STATE Processor occasionally activates a spare or redundant module to ensure that it is still good. The preferred method for doing this exercise is to use the fault injecting extended BITE routine, allow switch-over, test the redundant unit, and switch back.

The STATE Processor performs several key functions on power-on for the SPUR. Through a hardware initialize, it is driven to a test program for the STATE Processor itself, which tests for processor sanity. This initial test is very important because a failure in the STATE Processor can create havoc in the rest of the SPUR with such things as repeated or cyclic reconfigurations and overloading extended BITE tests. After the sanity tests are passed, the STATE Processor ascertains the status of the remainder of the SPUR and normal operation begins. All through this initial phase any problems are reported to the data processor. If the data processor does not receive processor status messages, it can cause a hardware initialize to restart the STATE Processor.

The STATE Processor design is highly specialized to the detailed design of the SPUR. In sizing the unit, 16K of program memory and 2K of data storage have been allocated for the unit. With the recommendation of use of the MC68000, higher level language programming may be desirable. This potential requirement was not considered for the initial sizing.

6.4 PULSE COMPRESSION TRADEOFFS

Pulse compression selection requires a multifaceted evaluation involving waveform selection, performance analysis, location of the pulse compression in the processing chain, technology selection, and implementation. The SPUR pulse compression function parameters are a compressed pulselength of 1.23 μsec (corresponding to a range resolution of 0.1 nmi) and a time-bandwidth product on the order of 32. The specifications and characteristics of the recommended pulse compression unit are given in Section 6.1.



9524-91

NOTE:
SYSTEM TIMER INSURES THAT REPORT IS RECEIVED IN GIVEN TIME FRAME; OTHERWISE, THE STATE PROCESSOR IS ASSUMED INCAPABLE OF TRANSMISSION. THIS ASSUMPTION CAUSES EXTERNAL HARDWARE INITIALIZE AND WAIT FOR RESPONSE. IF NO RESPONSE IS RECEIVED IN GIVEN TIME FRAME, THE SYSTEM IS SHUT DOWN.

Figure 6-4. The Flowgraph shows the Logical Interaction of the Functions of the STATE Processor

Three waveforms were initially considered for the SPUR: linear frequency modulation (chirp), nonlinear frequency modulation, and binary phase coding (maximal length sequence code of 31 bits). The performance of these basic waveforms (Table 6-VI) illustrates the classic characteristics of each. The linear FM with weighting for sidelobe reduction is an unmatched system (with significant loss at zero Doppler) and high Doppler tolerance. The nonlinear FM is a matched system (sidelobes are reduced by selection of the nonlinearity) which is fairly Doppler-tolerant. The binary phase-coded waveform is a matched system that is highly Doppler sensitive with large loss incurred at the maximum Doppler velocity of ±2400 knots.

TABLE 6-VI. THE LOSS IN SIGNAL-TO-NOISE RATIO FROM A MATCHED SYSTEM *was calculated during analyses of three candidate waveforms for SPUR*

	Loss (dB)	
	Zero Doppler Target	2400 knot Doppler Target
Linear FM with -40 dB Hamming Weighting	1.3	1.4
Nonlinear FM with Taylor Weighting	0	1.0
Binary Phase Code (31-bit)	0	2.5

9524-92

The location of the pulse compression in the processing chain is a function of the waveform selected, technology utilized, and the implementation method. Two general effects of placing the waveform process before the Doppler filtering are: a) the waveform process must be linear, and b) a wider dynamic range is desired in the Doppler filtering for the same performance. This latter effect occurs because point clutter or discretes will have compression gain. In the SPUR, five additional bits are desired which bring each I and Q word to 16-bits long. When an analog pulse compression unit, such as SAW or steel lines, is used, this bit increase is not feasible because A/D converters of 16-bits at 0.618 μsec are not available. Thus the performance of an analog pulse compressor is degraded against point clutter because it causes additional saturation to occur in the processor. This additional saturating clutter must be removed by a residue map (considered part of the data processor, not the SPUR) to keep the false alarm rate at the required level. When digital pulse compression is used, it occurs after the A/D converter so that extended word lengths are feasible. The extended word lengths force the Doppler filters to use the 16-bit x 16-bit multiplier/accumulator which have longer processing times (200 nsec vs 170 nsec for the 12-bit x 12-bit device).

When pulse compression is accomplished after the Doppler filtering, it need not be linear and the dynamic ranges of the functions are reduced. Two types of nonlinearities are soft-limiting (i.e., using sign + n bits, where n is less than the 13-bits at the output of the Doppler filters), and hard-limiting (i.e., using the sign bit only). Hard-limited binary phase coded pulse compression is an example of this nonlinear processing.

After consideration of the candidate waveforms, applicable technology, and placement within the processor, three implementations were selected for the final tradeoffs. These were: a) linear FM implemented by SAW line, b) linear FM implemented digitally and preceding the Doppler filtering, and c) hard-limited binary phase-coding implemented digitally after the Doppler processing. The comparison among these alternatives also considers implementation of the required Constant False Alarm Rate (CFAR) function. CFAR is evaluated at this time because hard-limited binary phase-coded pulse compression provides the CFAR, while the two linear FM implementations require a separate CFAR function implemented after Doppler filtering and envelope detection.

Linear FM pulse compression using a SAW line is accomplished in the IF domain ahead of the phase detectors. In addition to the SAW lines, amplifiers are required for driving the input and amplifying the output of the SAW line. The specifications for the SAW line considered for the SPUR are given in Table 6-VII. As noted in the technology evaluations, Section 4.1, SAW implementation is considered preferable to an IF implementation using steel lines.

TABLE 6-VII. A CANDIDATE SAW LINE FOR LINEAR FM PULSE COMPRESSOR FOR THE SPUR HAS THESE SPECIFICATIONS

Center Frequency	30 MHz
Compressed Pulsewidth (-3 dB)	1.25 μsec
Bandwidth (40 dB Taylor Weighting)	1 MHz
Dispersion Time	40 μsec
Sidelobes	$<$ -27 dB
Doppler	±2400 knots
Insertion Loss	30 dB
Temperature Coefficient	0.03 ppm/°C^2
Operating Temperature	-20°C to +70°C
Nonoperating Temperature	-65°C to +50°C
Package	Unheated device in machined aluminum case
Size	10.0 x 2.0 x 0.5 inches

9524-93

Digital implementation of the linear FM waveform was evaluated for a fixed pulse compressor based on the Butler phase matrix. This implementation for a fixed code was preferable to the use of fast convolution through an FFT, multiply, and IFFT. Programmable implementations were briefly considered, but the cost and complexity associated with programmable versions would completely dominate the processor and, as a consequence, were rejected.

Binary phase-coded (BPC) pulse compression, implemented digitally, is placed after the Doppler filtering such that hard-limiting can be used. Hard-limiting, as previously mentioned, provides the CFAR required by the SPUR. However, binary phase-coding is highly Doppler sensitive and would increase the losses by 2.5 dB against 2400-knot Doppler targets. Since this loss is quite high, BPC pulse compression would have been rejected on this basis if this loss could not be reduced. However, from previous research, the loss in BPC can be reduced by implementation of a multichannel pulse compressor, with the channels offset in frequency to cover the expected range of the Doppler velocities. This system is the BPC pulse compressor considered for the SPUR.

The three candidate pulse compressors including CFAR were evaluated using the SPUR weighting matrix (Table 6-VIII). The SAW and BPC pulse compressors have no redundancy, but the digital pulse compressor is fully redundant (1/2 cold standby) to achieve the given failure rate. Based on these results, the three channel, hard-limited binary phase-coded pulse compressor is recommended for the SPUR.

6.5 ANALOG-TO-DIGITAL CONVERTER TRADEOFFS

Evaluation of analog technology in the SPUR application (as discussed in Section 4.1, Analog Technologies, and Section 6.4, Pulse Compression Tradeoffs) has shown that early conversion to the digital domain is desirable. Hence, in the recommended configuration, the analog-to-digital (A/D) converter is placed at the input to the SPUR (equivalently, at the output of the I- and Q-phase detectors). The Analog and A/D Converter Function in the functional block diagram of the SPUR therefore consists of the A/D converter only.

Tradeoffs for the A/D converter consisted of two parts: 1) selection of the recommended implementation method for the converter, and 2) selection of the recommended number of bits for the converter. These evaluations were performed in conjunction with the system analysis described in Section 3.6, Dynamic Range Requirements, and with the selected method of Doppler filtering, as recommended in Section 6.1 and discussed in the next section.

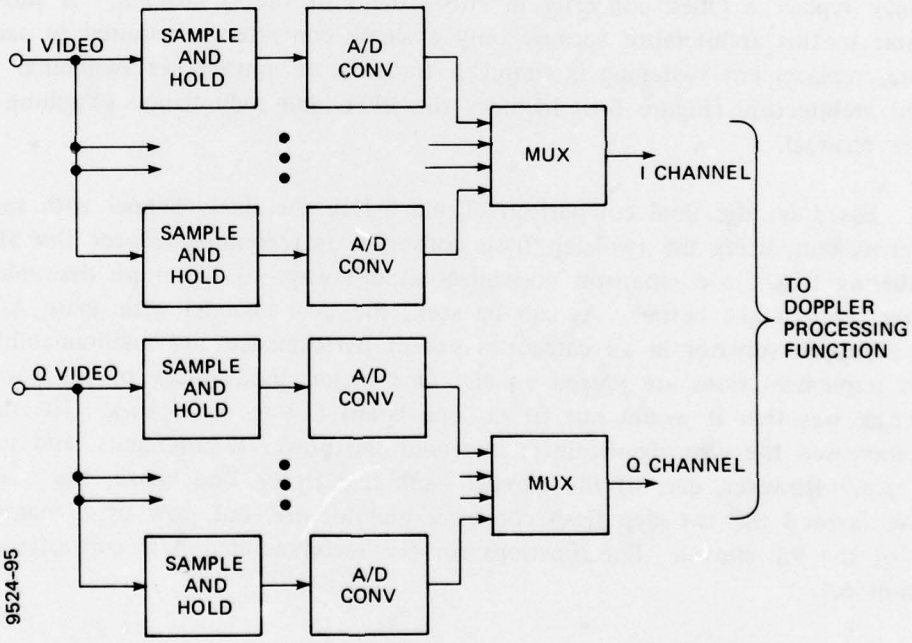
Two methods of implementing the A/D converter were compared in the final evaluation leading to the recommended unit. These methods were: 1) two channels of parallel banks of A/D converters using successive approximation devices, and 2) two A/D converter channels, each based on two-step flash converters. The basic devices were described in Section 4.2, Analog-to-Digital Conversion Technologies.

Parallel banks of A/D converters are inherently attractive in a highly reliable processor because they contain natural fault-tolerance. Their parallelism (m devices operating) leads to an m/n architecture by extending the basic design to include spare units (Figure 6-5). At the present state-of-the-art in modular converters (12 bits at 2.0 μsec conversion time), four units are required in each channel (I and Q) to achieve the speed required by the SPUR

TABLE 6-VIII. THE SPUR WEIGHTING MATRIX IS DEVELOPED FOR PULSE COMPRESSION AND CFAR FOR THREE CANDIDATE IMPLEMENTATIONS

Criterion	Weighting	SAW Linear FM		Digital Linear FM		Hard-limited Binary Phase Coding	
Reliability	10	8.24 f/10^6	11.2	8.08 f/10^6	10.9	7.39 f/10^6	10
Performance Pulse Compression plus CFAR Loss	10	-2.8 dB	10	-2.8 dB	10	-3.6 dB	22.9
Cost	7	2.5	17.5	3.5	24.5	1.0	7.0
Maintainability	6	1.1	6.6	1.2	7.2	1.0	6.0
Risk	6	1.25	7.5	1.2	7.2	1.0	6.0
Power	5	22.4W	7.0	56.8	17.75	16.0W	5.0
			59.8		77.55		56.9

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***Figure 6-5. Parallel banks of successive approximation A/D converters** are one candidate for the SPUR A/D converter system*

(618 nsec conversion time). An additional unit in each channel is added to provide fault-tolerance. (A single spare module, protecting both channels is rejected due to potential introduction of crosstalk between channels and to more complicated control and BITE circuitry.) Two major considerations in this architecture (Figure 6-6) are: 1) a sample-and-hold device is required ahead of each converter, and 2) the control circuitry and output multiplexing circuitry are relatively complicated. Sample-and-hold units ahead of each modular converter hold the input constant for the conversion time of 2 μsec, required since the A/D converters (being successive approximation devices) convert one bit at a time. This additional unit per A/D module adds significant cost and power to this A/D converter implementation. More control circuitry is required because the input sample-and-hold units must sample the input in sequence (Figure 6-7) to allow enough time for each conversion to be made, and the output digital words must be multiplexed back together to interface with the Doppler Processing units.

The second architecture in the final evaluations consisted of two channels (I and Q) of A/D converters based on two-step flash converters. Flash converters exceed the SPUR speed requirements. By performing a coarse and a fine conversion (two steps), the flash converters can be used to meet the dynamic range requirements. A fault-tolerant structure is attained in this architecture by providing a spare two-step flash A/D converter which may replace a failed converter in either the I or the Q channel. A single spare is permissible in this architecture because only a single converter is required in each channel. Therefore, replacement switching is simply a function of multiplexer switching. The evaluated architecture (Figure 6-8) includes the BITE and redundancy switching to utilize the spare channel.

Based on the final comparison (Table 6-IX), the dual channel with spare A/D converter system, using the two-step flash converter, is recommended for the SPUR. Remembering that the comparison normalization is always to the more desirable alternative, the lower score is the better. As can be seen, the dual channel with spare A/D converter system is judged superior in all categories except performance and maintainability where the two implementations are judged equal. One major disadvantage of the parallel bank architecture was that it would not fit on one board (14 in. x 15 in.). The use of two boards increased the cost significantly, increased the power requirements, and increased the failure rate. However, even if the parallel bank had fit on one board, the tradeoff would still have favored the two-step flash converter architecture, but now by a margin of 4.5 instead of the 9.0 shown. Specifications for the recommended A/D converter are listed in Section 6.1.

The recommended dynamic range of the A/D converter (i.e., number of bits provided by the converter) is based on performance requirements, risk, and cost. While a 10-bit (sign + nine bits) unit can provide adequate performance against the specified clutter models in terms of dynamic range limitations due to the quantization noise of the converter, the SPUR must operate in a heterogeneous ground clutter environment

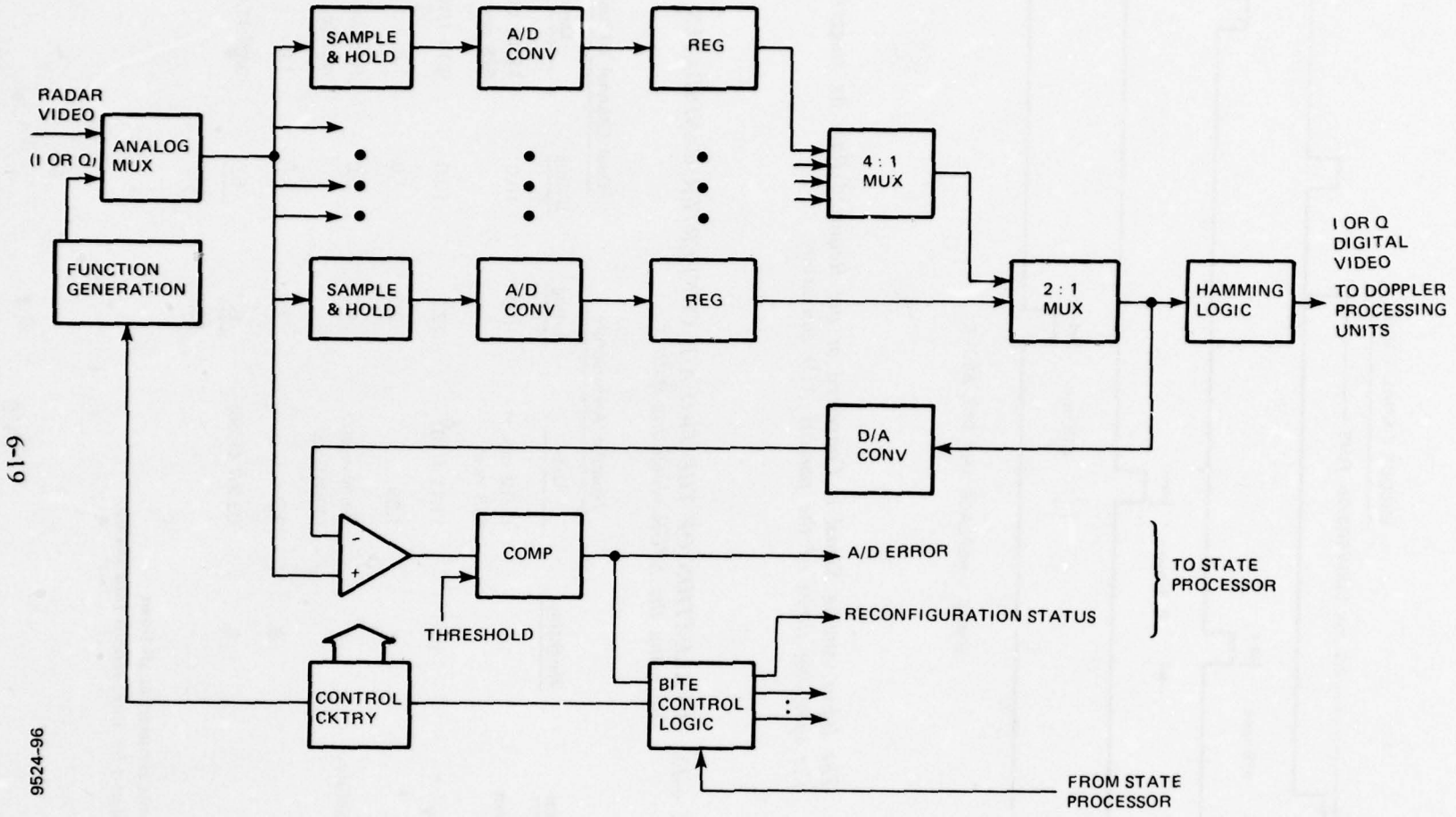


Figure 6-6. The Parallel Bank A/D Converter uses Two Channels of the Above Architecture with Independent BITE and Reconfiguration per Channel

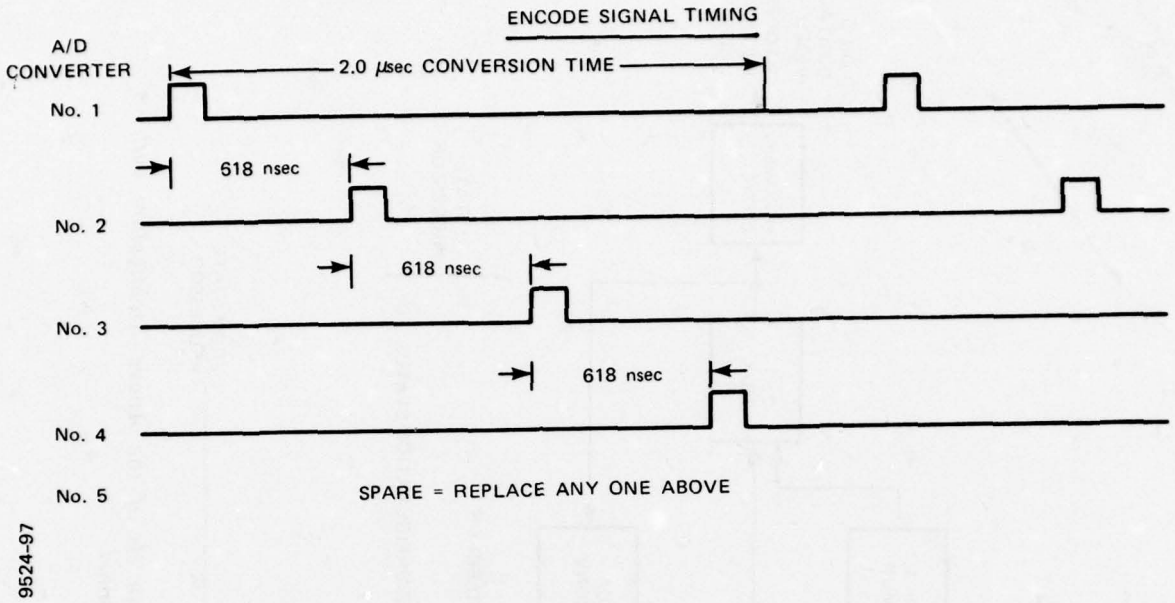


Figure 6-7. The Input Analog Signal is Converted at the Required Rate *by staggering the sampling times of the parallel A/D converters.*

TABLE 6-IX. EVALUATION OF THE TWO A/D CONVERTER CANDIDATES by using the SPUR weighting matrix

		Modular Architecture		Dual Channel W/Spare	
Criterion	**Weighting**	**Data**	**Rating**	**Rating**	**Data**
Performance	10	11/12 bits at 618 nsec	10.0	10.0	11/12 bits at 618 nsec
Reliability **	10	11.11 $f/10^6$	12.2	10.0	9.14 $f/10^6$
Cost	7	1.33	9.3	7.0	1.0
Maintainability	6	Remove and replace	6.0	6.0	Remove and replace
Risk	6	1.2	7.2	6.0	1.0
Power *	5	63.2W (1.66)	8.3	5.0	38W (1.0)
			53.0	44.0	

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* All units powered at all times

** Calculated for three-month time period.

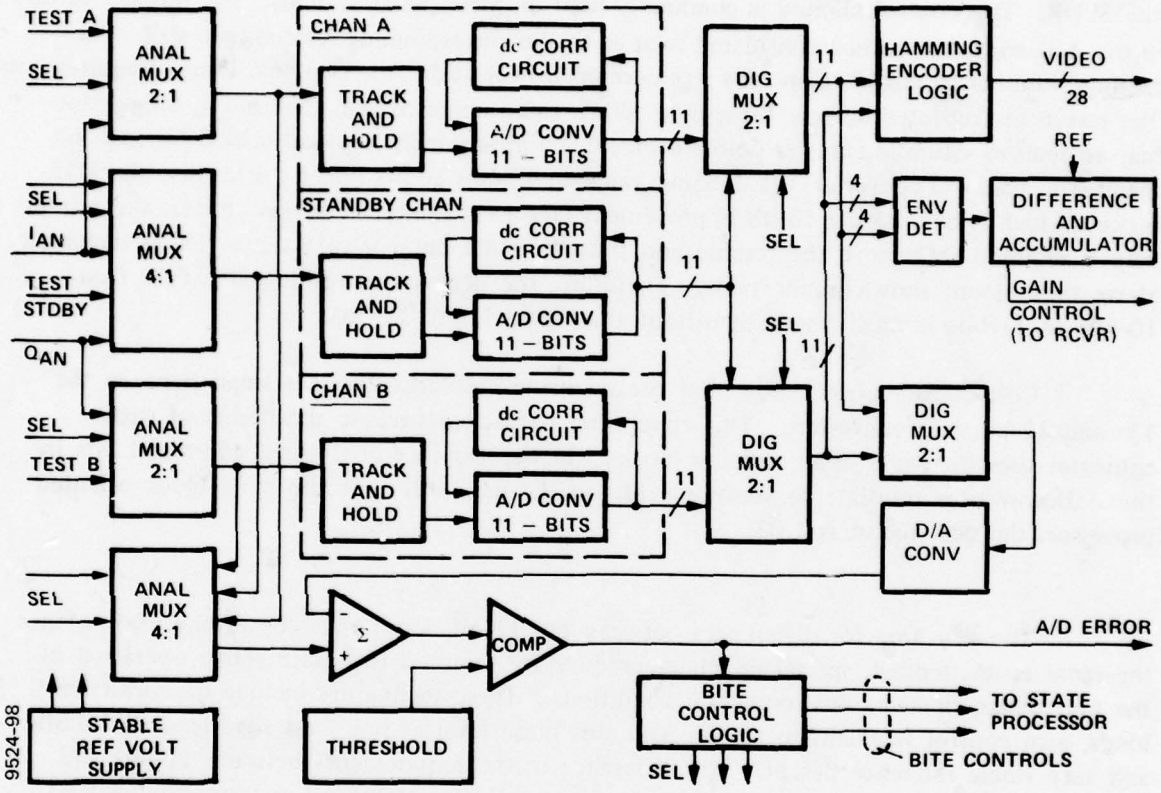


Figure 6–8. ***The Two-Step Flash Converter Architecture*** *uses one spare converter to protect the two in operation*

characterized by many discrete points of clutter. In order to minimize the loss of performance due to these points saturating and being detected as targets, added dynamic range was considered for the SPUR A/D converter. Thus, 11- and 12-bit units were evaluated. In the predicted clutter environment, some saturation is inevitable. The proposed method for controlling these discretes is the use of a residue map after the postdetection integration (second threshold). The residue map is not part of the SPUR itself but is located in the data processor which follows the SPUR. This control method is commonly used on many radar systems. The number of bits in the A/D converter is then considered relative to the corresponding residue map size. The required number of residue map cells was developed in Section 3.6, Dynamic Range Requirements. The results are repeated here as Table 6-X. While the number of cells required in the residue map to remove saturating clutter points decreases by approximately a factor of 5 for each bit increase in the A/D converter, the dynamic range at 12-bits allows linear clutter into the MTI process which is beyond the 50 dB improvement factor capability. For this clutter, the residue map is required to remove the residue and thus the total number of residue cells is increased above the amount shown in the table. Therefore, the decrease in residue map cells from 10-bits to 11-bits is much more significant than from 11- to 12-bits.

Cost considerations show that the recurring cost differential is small between the 11- and 12-bit A/D converters. This conclusion is reached because the design of each converter uses the same basic building blocks. In the Doppler processing, additional bits in the A/D converter translate to additional bits in the memory. For the range-block oriented processor, the cost factor is 1.03.

The key area for differences between the 11-bit and 12-bit converter is risk. Since the radar is unattended, special design techniques are required to ensure stable operation of the unit under changing environmental conditions. These techniques include dc correction loops, gain control to maintain the receiver rms noise level at one least significant bit (LSB), and very stable reference design. The difference in the requirements between 11-bits and 12-bits is a factor of two. This translates, when specifying stabilities in terms of the least significant bit, to requirements of 0.49 for 11-bits (1 volt peak) and 0.24 for 12-bits. The attainment of the 12-bit number is significantly harder than the 11-bit number, which is already difficult. After consideration of these design requirements and the risk involved, the advantage of a wider input dynamic range was judged to be outweighed by the risks involved in stabilizing and maintaining the 12-bit A/D converter system for unattended operation at 12-bit performance. Thus the 11-bit A/D converter is recommended as a compromise between the 10-bit and 12-bit units.

TABLE 6-X. THE NUMBER OF BITS USED IN A/D CONVERSION ARE TRADED WITH THE NUMBER OF CELLS REQUIRED IN A RESIDUE MAP FOLLOWING DETECTION

Number of Bits	Full-Scale Input c/n Ratio (dB)	Full-Scale Backscatter Coefficient, σ°_{FS} (dB) (Note 2)	Probability that σ°_{FS} is Exceeded (Note 2)	Number of Cells Which May Saturate (Note 3)
Note 1	46.0	-24.0	0.16	12,300
10	51.2	-18.8	0.07	5,390
11	57.2	-12.8	0.015	1,160
12	63.2	-6.8	0.003	231

NOTES:

1. c/n = 46.0 dB corresponds to reflectivity at the 84th percentile such as used in the performance summary (Table 3-VI)
2. Based on log-normal distribution of land clutter.
3. Based on an estimated 77K cells containing clutter. This is 29 percent of 264K cells total.

6.6 DOPPLER PROCESSING TRADES

Trade studies were performed to evaluate three Doppler processing architectures:

a) A Doppler Module architecture,
b) A Range Block Doppler Module architecture,
c) An FFT architecture.

6.6.1 Doppler Module Architecture

A simplified block diagram of the doppler module (DM) architecture is given in Figure 6-9. A total of eight Doppler modules is provided, of which six are powered up in an online mode and two are powered down in an offline mode. Each of the six Doppler modules is used to implement one of six near-optimum FIR filters which collectively form the Doppler filter bank. All eight modules are identical and each module is capable of implementing any one of the six filters. The individual modules online/offline state and filter designation is assigned by the STATE processor.

Each Doppler module has four major elements which are duplicated for the real and imaginary part processing:

a) A multiplier,
b) An accumulator,
c) A main store memory,
d) An output buffer memory.

Range ordered complex data samples are presented to the complex multiplier at the system data sample rate of $(618\ \text{nsec})^{-1}$ during each of the eight listening periods within the 9-pulse transmission group. A range bin sample is multiplied by the complex weight specified for that sample in the filter and accumulated with the previous weighted samples for that range bin. The partial sum is stored in the main store memory and recirculated until all eight samples have been weighted and accumulated. The final sum is hard limited (sign-bit only) and stored in the output buffer memory. Data from the output buffer memory for a Doppler module is sent to the pulse compression unit under control of the STATE processor. The output buffer memory for a given module will contain the hard-limited range ordered response of the filter to which that module is assigned.

6.6.2 Range Block Doppler Module Architecture

In the Range Block Doppler Module (RBDM) architecture (Figure 6-10), each module performs the required calculations to implement six near-optimum FIR filters for a block of ranges. The filters implemented are identical to the near-optimum FIR filters implemented using the Doppler Module architecture previously discussed. Four range block Doppler modules are provided, of which three are powered up in an online mode and one is powered down in an offline mode. All four modules are identical. The individual modules online/offline state and range block designation is assigned by the STATE processor.

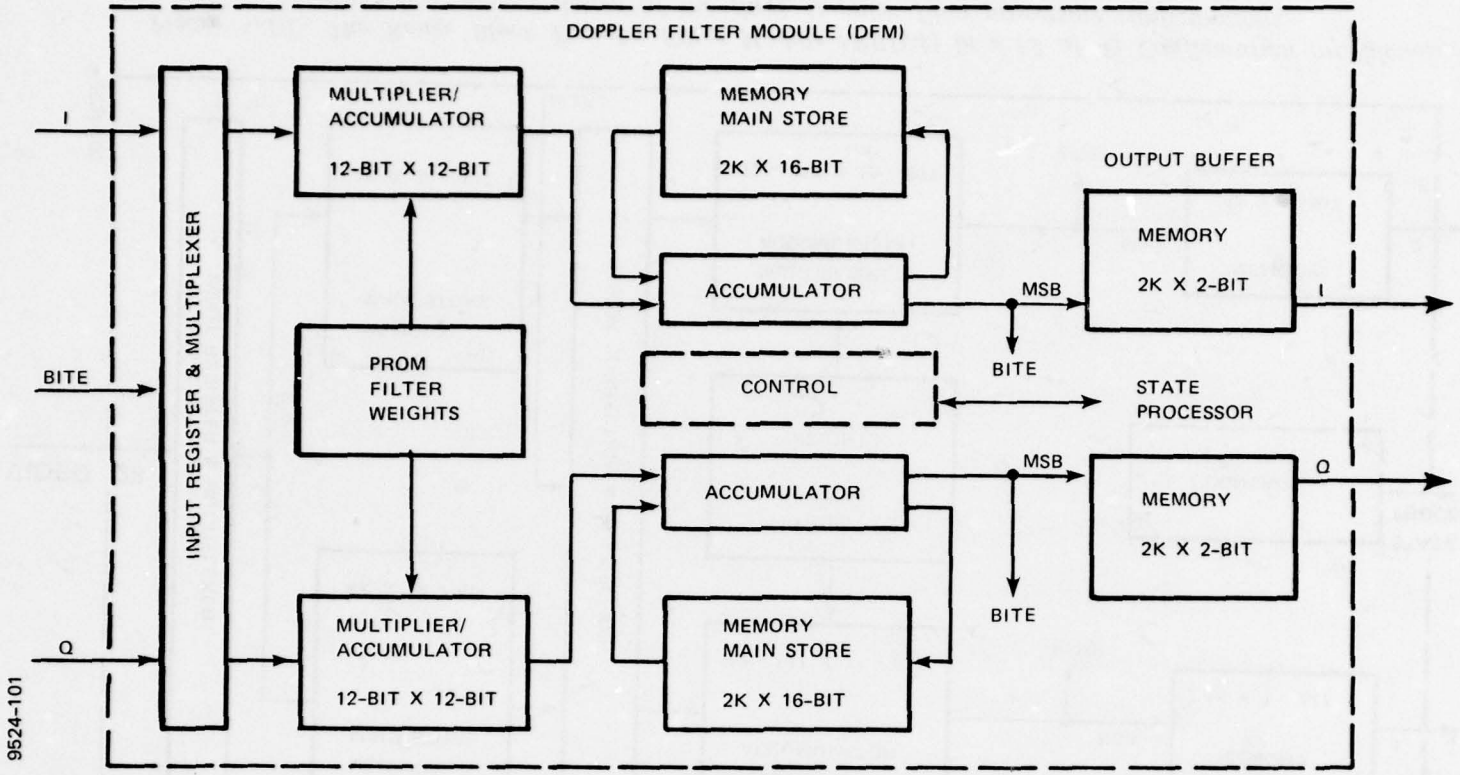


Figure 6–9. ***The Doppler Filter Module (DFM) in a (6 of 8) Configuration*** *provides the most reliable design of the three doppler processing configurations.*

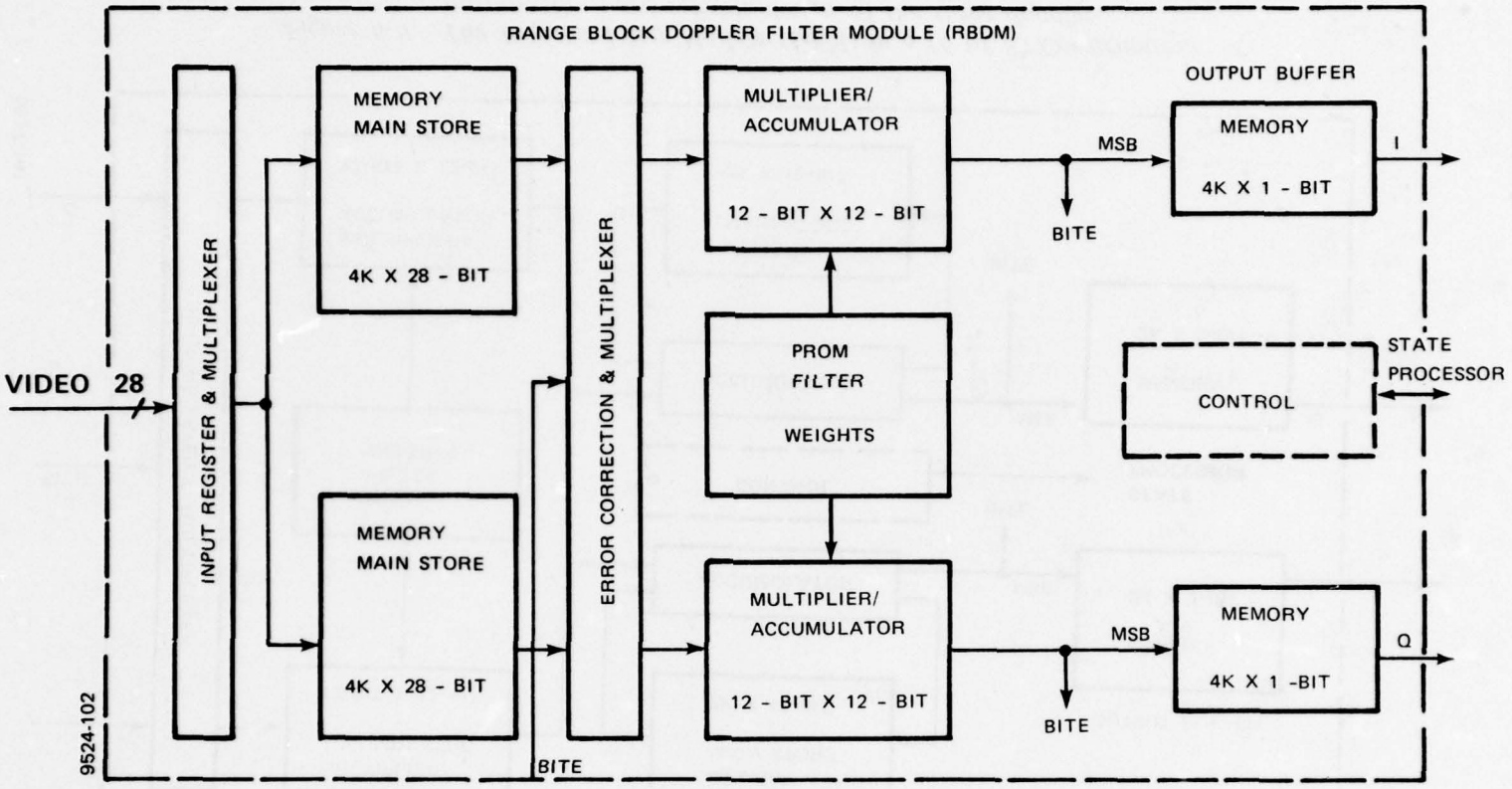


Figure 6–10. The Range Block Doppler Filter Module (RBDM) in a (3 of 4) Configuration *provides the lowest power design of the three Doppler filter processing configurations*

Each Range Block Doppler Module has three major elements:

a) A double buffered main store memory,
b) A complex multiplier/accumulator,
c) An output buffer memory.

The main store memory is configured using two independent random access memory modules. The two memory modules alternate as input buffer memory and as processor buffer memory. The input buffer memory receives and stores complex data samples either at the system data sample rate of $(618 \text{ nsec})^{-1}$ for one-third the range bins, or at one-third the system data sample rate of $(1854 \text{ nsec})^{-1}$. The processor buffer memory provides complex data samples to the complex multiplier/accumulator. The samples are ordered by pulse and then by range such that all eight samples for a given range bin are read out from the processor buffer memory to be followed by all eight samples for the next consecutive range bin. The entire processor buffer memory is read out to the complex multiplier/accumulator in the sequence stated above a total of six times – one time for each of the six FIR filters which are calculated. Readout from the processor buffer memory occurs at a rate of $(412 \text{ nsec})^{-1}$ per complex sample.

In the multiplier/accumulator, the eight samples for a range bin are weighted using the eight complex weights for the filter being calculated and the sum of the eight complex products are accumulated. The final sum is hard-limited (sign-bit only) and stored in the output buffer memory.

The output buffer memory is itself double buffered. Data from the output buffer memory is multiplexed onto an output data bus for the designated range block under control of the STATE processor.

6.6.3 FFT Architecture

The FFT architecture is used to implement a Doppler filter bank which consists of eight identically shaped FIR filters equally spaced across the Doppler frequency band. Time domain weighting with Chebyschev weights is used to suppress sidelobes to a uniform level suitable for ground clutter suppression.

A simplified block diagram of the FFT architecture is given in Figure 6-11. The FFT processor consists of a single Memory/IO module and two Processor modules, one of which is powered up in an online mode and one of which is powered down in an offline mode. The Processor modules online/offline state is controlled by the STATE processor.

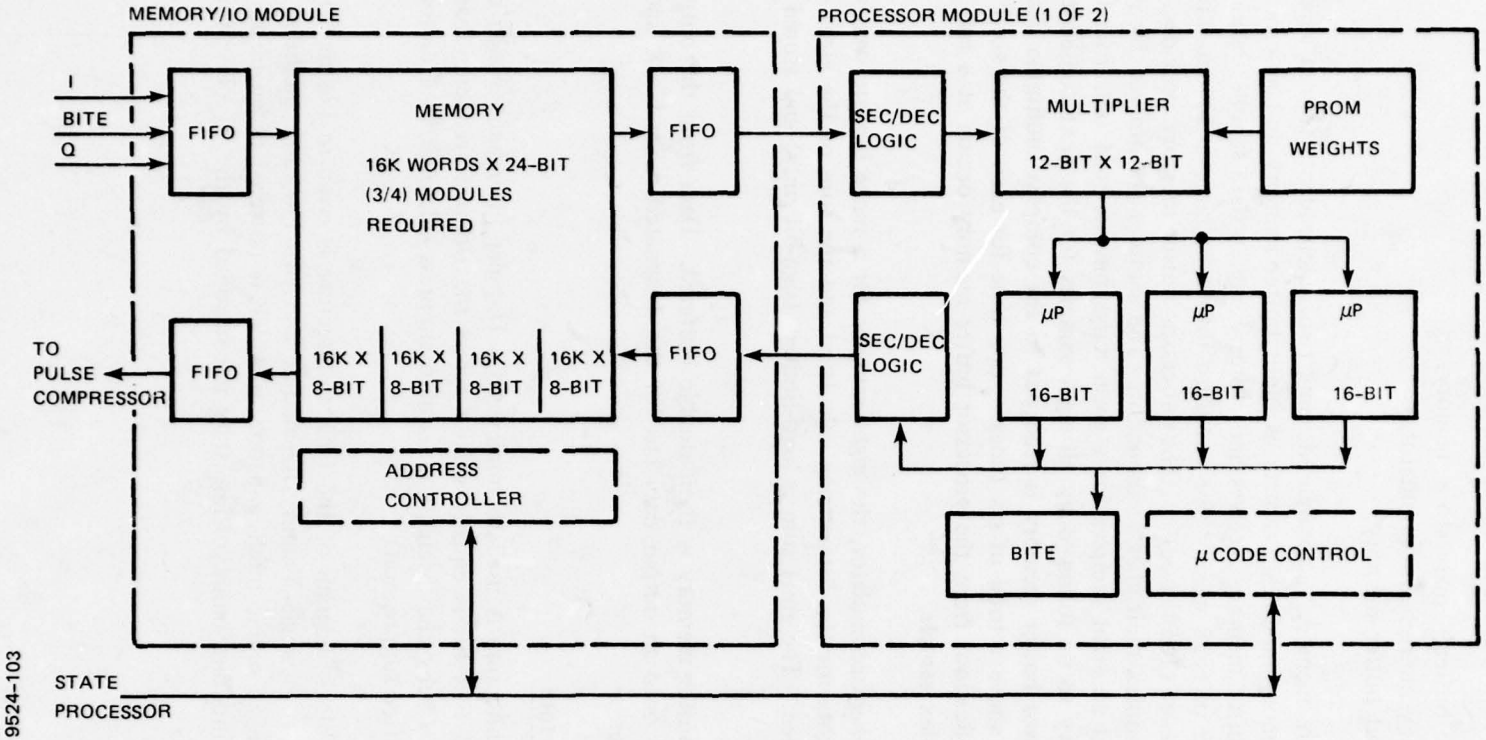


Figure 6–11. The FFT Architecture with One Memory/IO Module and Two Processor Modules in a (1 of 2) Configuration *provides the lowest cost design of the three Doppler processing configurations*

The Memory/IO module accepts range ordered complex input data samples from an input bus at the system data sample rate of $(618 \text{ nsec})^{-1}$. Input data samples are stored in a memory for the eight listening periods within the 9-pulse transmission group. Access to the memory is shared between four functions:

a) Storage of complex input data samples,
b) Retrieval of complex input data samples,
c) Storage of hard-limited processed filter data,
d) Retrieval of hard-limited processed filter data.

Memory is organized into 16K-words by 24-bits. Access is page-oriented with each page containing 128 words of 24-bits each. Memory access is shared between the functions using a dedicated round-robin time-slice arrangement. Each time-slice contains nine clock periods of 208 nanoseconds. The first clock in the time-slice period is reserved for page access and the remaining eight clocks are available for eight read cycles or write cycles, or a mixture of read and write cycles. FIFO buffer memories are used by each of the four functions to match their data rates to the effective data rate provided by their dedicated access times. Nine of the 18 time-slices are dedicated to the storage of complex input data samples. Eight of 18 time-slices are dedicated to the retrieval of complex input data samples. One of 18 time-slices is dedicated to the storage and retrieval of hard-limited processed filter data.

The Memory/IO module retrieves complex input data samples from the Processor module memory in the required sequence; receives hard-limited processed filter data from the processor and stores this data in the memory; and retrieves the hard-limited processed filter data from the memory and sends it to the Pulse Compression Unit in the required sequence.

The Processor module contains a single 12-bit by 12-bit multiplier, and three 16-bit microprocessors. The processor is pipelined in two stages. The first stage performs all required multiplications for each of three range bins of data during a period of 81 clocks (one clock equals 208 nanoseconds). The second stage performs all required 8-point FFT operations for each of three range bins of data during the next 81 clocks (each of the three microprocessors processes data for one of the three range bins).

6.6.4 Comparison of Memory Requirements

Memory is a cost, power and reliability driver in the SPUR Doppler processor. The three Doppler processor architectures resulted in significantly different memory designs. Major features of these three memory designs are summarized in Table 6-XI.

The FFT architecture was based around the use of a 16K, dynamic, MOS memory chip. This organization requires a high memory access rate $(208 \text{ nsec})^{-1}$, but provides for low cost per bit, low failure rate per bit and reasonably low power per bit. Note that a single, centralized memory organization was provided in order to make use of the 16K word by 1-bit memory chip form factor.

TABLE 6-XI. RELIABILITY, POWER, AND COST IMPACTS EVALUATED FOR THE MEMORY DESIGNS OF THE THREE DOPPLER PROCESSING ARCHITECTURES

		Doppler Processing Architectures		
		Doppler Module (DM)	Range Block Doppler Module (RBDM)	FFT
Memory Requirement in Bits	Per Module	73,728	229,376	524,288
	Online	442,368	688,128	524,288
	Total	589,824	917,504	524,288
Memory Chip Characteristics	Chip Size	4K, Static, MOS	4K, Static, CMOS	16K, Dynamic, MOS
	No. of Chips	144	224	32
	Cost Per Bit	1.0	1.0	0.5
	λ Per Bit (10^{-10})	3.29	3.29	2.11
	Power Per Bit mW X 10^{-3}	90.3	12.7	29.2
Memory Architecture Characteristics	Min Cycle Time (nsecs)	309	412	208
	Error Correction	No	SEC/DED (26/27)	SEC/DED (15/16)
	Active Modules/ Total Modules	6/8	3/4	3/4

The range block Doppler module with a memory access rate of $(412 \text{ nsec})^{-1}$ was designed to use the very low power 4K by 1-bit CMOS memory chip. However, to provide for this low memory access rate, a double buffered memory organization was required which resulted in a relatively high total memory requirement.

The Doppler module was designed to use a 1K word by 4-bit static MOS, memory chip. The memory organization and addressing requirements for the Doppler module are the simplest of the three memory designs.

6.6.5 Comparison of Reliability Requirements

Selective redundancy was added to each of the three architectures to provide an acceptable level of reliability. The Doppler Module (DM) was designed to operate in a 6 out of 8 configuration. No additional redundancy was added to the basic Doppler Module itself. The Range Block Doppler Module (RBDM) was designed to operate in a 3 out of 4 configuration. In addition, a single bit error correction/double error detection code (26 of 27) was provided for the main store memory. The FFT was designed with the Processor module operating in a 1 out of 2 configuration. The single Memory/IO module was provided with both a single bit error correction/double error detection code (15 of 16) and a 3 out of 4 memory module redundancy capability.

6.6.6 Results of the Trade Studies

Results of the trade studies for the Doppler processing function are presented in Table 6-XII. It is noted that the FFT does not meet the minimum performance requirement of 50 dB Improvement Factor against ground clutter and is therefore not recommended. Relative performance of both the Doppler Module (DM) and the Range Block Doppler Module (RBDM) is very close with neither one having a clear advantage over the other. The Range Block Doppler Module (RBDM) was selected for the Doppler filtering because (a) the RBDM provides higher reliability for the combined functions of A/D conversion and Doppler processing which were considered separately in the preceding tradeoffs, and (b) the RBDM is easier to test in an experimental radar than the DM since a single RBDM unit develops all the Doppler filters for a block of range bins.

6.7 ZERO CHANNEL PROCESSOR TRADEOFFS

The Zero Channel Processor (ZCP) is an important part of the false alarm control of the SPUR against the severe ground clutter environment of the arctic. In the SPUR the ZCP operates on the data from the zero Doppler filter after it has been pulse compressed, envelope detected, and combined into one sample per range bin (from the original two). The output from the ZCP is sent to the Post Detection Processor (PDP) as one input to the ***greatest-of*** filter selector (the remaining five filters from the Doppler Processing Modules form the other inputs).

The key feature of the ZCP is a fine grain clutter map which stores a dynamic history of the clutter environment in which the radar is located. The clutter map is a dedicated unit, i.e., unlike a push-down memory stack, it provides fixed storage locations for each cell over the full area of coverage. The dynamic history of the clutter map is used as

TABLE 6-XII. TRADEOFF TABLE EVALUATION OF THREE CANDIDATE IMPLEMENTATIONS OF THE SPUR DOPPLER FILTERING

Criterion	Weighting	Doppler Modules		Range Block Modules		8-Point FFT	
Performance	10	50.9 dB	10	50.9 dB	10	46.9	20.9
Reliability (f/10^6 hrs)	10	5.411	10	7.241	13.4	11.822	21.8
Cost	7	1.87	13.1	1.95	13.7	1.0	7.0
Maintainability	6	1.0	6.0	1.0	6.0	1.2	7.2
Risk	6	1.0	6.0	1.1	6.6	1.2	7.2
Power (Watts)	5	145.8	9.7	75.3	5.0	107.6	7.2
			54.8		54.7		71.3

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a control function on the zero filter data presented for postdetection processing. When clutter is present, the clutter map removes the output of the zero Doppler filter from the PDP. Since it is a fine grain map, it provides the capability for intraclutter visibility because it allows use of the zero filter in any relatively clear areas located among patches of heavy clutter. Thus, the use of MTI is improved from an area function to a cell function determined by the size of the map cells.

Three major tradeoffs were performed for the Zero Channel Processor. These tradeoffs were an evaluation of the algorithm to be used, the implementation and technology of the processor and the memory, and the cell size of the fine grain clutter map (hence the amount of memory required). In addition to evaluating these candidates independent of the rest of the processor, this area provided the opportunity for an important tradeoff in overall implementation of those features beyond the envelope detection. This tradeoff, as discussed below, allowed integrated implementation of this unit with the Postdetection Processor discussed in Section 6.8.

Two algorithms were considered for the SPUR: threshold process and censor process. The threshold process develops an estimate of the clutter intensity in a particular cell through averaging over several scans and sets a threshold for each cell as a function of that intensity. Returns in the cell which exceed the threshold are passed to the Postdetection Processor for inclusion in the greatest-of filter selection. Thus, this process provides superclutter visibility in addition to the intraclutter visibility previously described, i.e., when the target is greater than clutter in the same cell by a selected amount it can still be detected. The censor process, on the other hand, detects clutter in a cell and censors that cell from the output as long as the ***clutter present*** conditions are met. A sequential observer, which maintains a count on the number of hits per cell, is used to implement the censor process. The censor process does not provide superclutter visibility for tangential targets; it does, however, provide intraclutter visibility for these targets.

The ZCP is a natural area for evaluation of microprocessor implementations because the data rate is reduced by a factor of 16 from the front-end processing and the task is a relatively straight-forward repetitive algorithm. Hence, two microprocessor implementations were evaluated: the 16-bit Radar Processing Module-II, based on bit-slice bipolar technology; and the second generation 16-bit MC68000 based on MOS technology. Each implementation was evaluated for both the threshold process and censor process.

The RPM-II (Figure 6-12) is a 16-bit microcomputer designed around the AM2903 bit-slice microprocessor chip. It is configured on one 14 in. × 15 in. board containing all of the hardware except the program memory which is stored in offboard PROMs. The instruction or control word is fully microprogrammed and is 56-bits wide. Special features of the RPM-II, also discussed in Section 4.4, center around its versatile I/O structure and capability for parallel operations.

The MC68000 is representative of second generation 16-bit microprocessors in terms of speed and architecture. A block diagram for the MC68000 (Figure 6-13) shows the relative simplicity of a basic design. Two MC68000 systems of the complexity required for the SPUR processing can reside on one 14 in. × 15 in. board. The control word and data word are each 16-bits in the MC68000 and they enter through the multiplexed input port. Special features of the MC68000 include a very powerful instruction set which is oriented to higher level languages (particularly PASCAL) and a versatile memory management structure.

Evaluation of the RPM-II and MC68000 for the two candidate processes of the Zero Channel Processor show that the speed of the RPM-II is about twice that of the MC68000 and the threshold process requires greater than 4 times as much processing time per cell as the censor process (Table 6-XIII). The two processors also require approximately the same number of instructions for each algorithm, although they are quite different instructions.

The cell size for the fine grain clutter map is an important tradeoff because it affects processor performance and memory size. The number of cells versus the granularity in range and azimuth of the cell is shown in Figure 6-14. Since the purpose of the Zero Channel Processor is to aid in detection of tangential targets, the azimuth granularity is therefore selected to be as small as possible; namely, 3/4 degree or one coherent pulse group. The granularity in range is then determined by a compromise between map performance and map memory requirements. The recommended range granularity is 0.4 nmi as this limits the map size to 64K (2^{16}) cells. Fixed map cells are obtained when a 13-bit azimuth encoder is used and the cells are set up with 17 counts per cell except for those cells located at n × 11.25° which use counts of 18. Thus, 448 sectors use 17 counts and 32 sectors use 18 counts. This definition keeps the cell locations constant, which is important in fine grain clutter maps.

The above comparisons for the Zero Channel Process (ZCP) do not force an algorithm selection. However, an external consideration has a heavy bearing on the final decision: the use of hard-limited binary phase-coded pulse compression limits the dynamic range at the output of the range combination function to 6-bits or a signal-to-noise ratio of

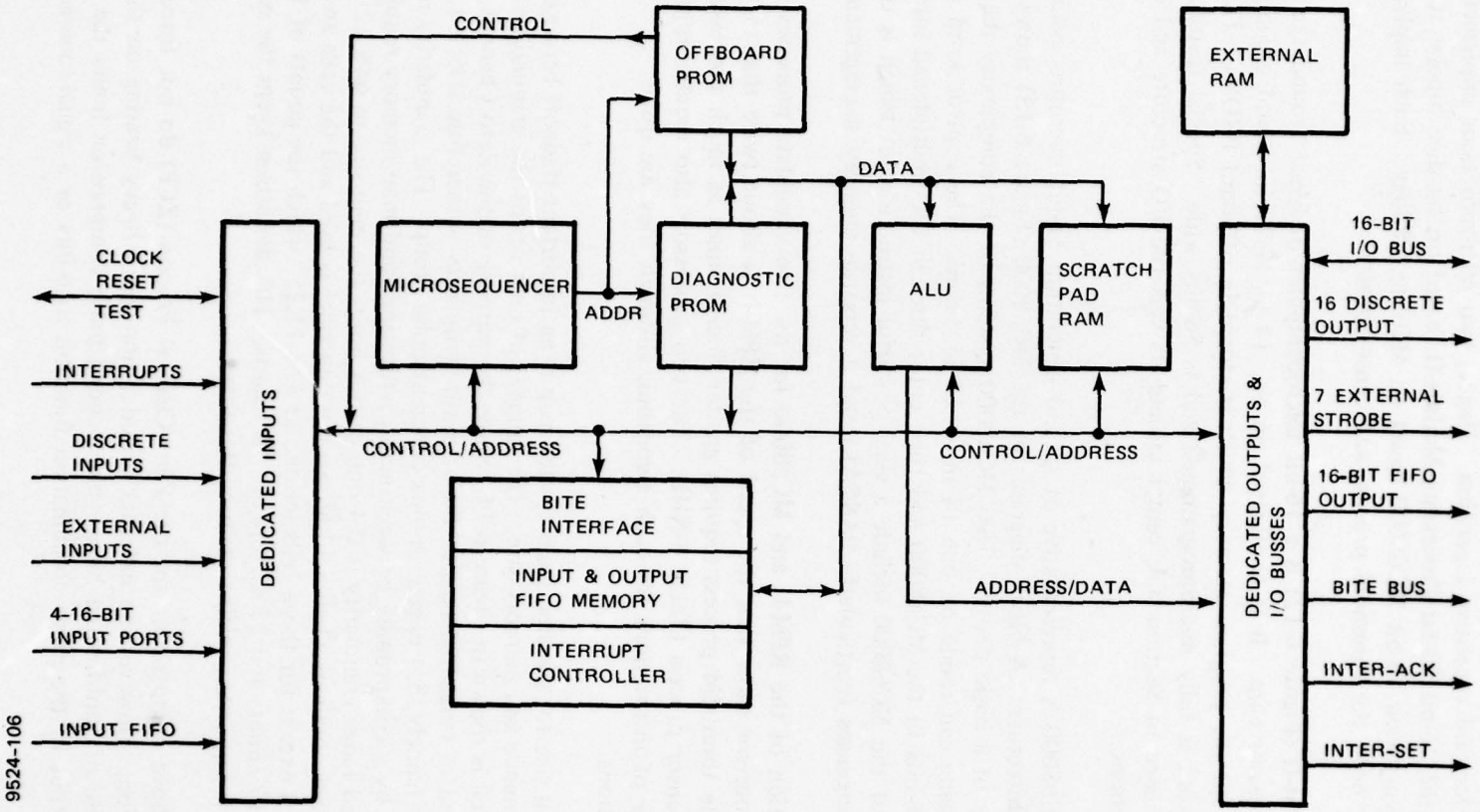


Figure 6–12. The RPM-II block diagram *illustrates the versatile I/O structure of the processor.*

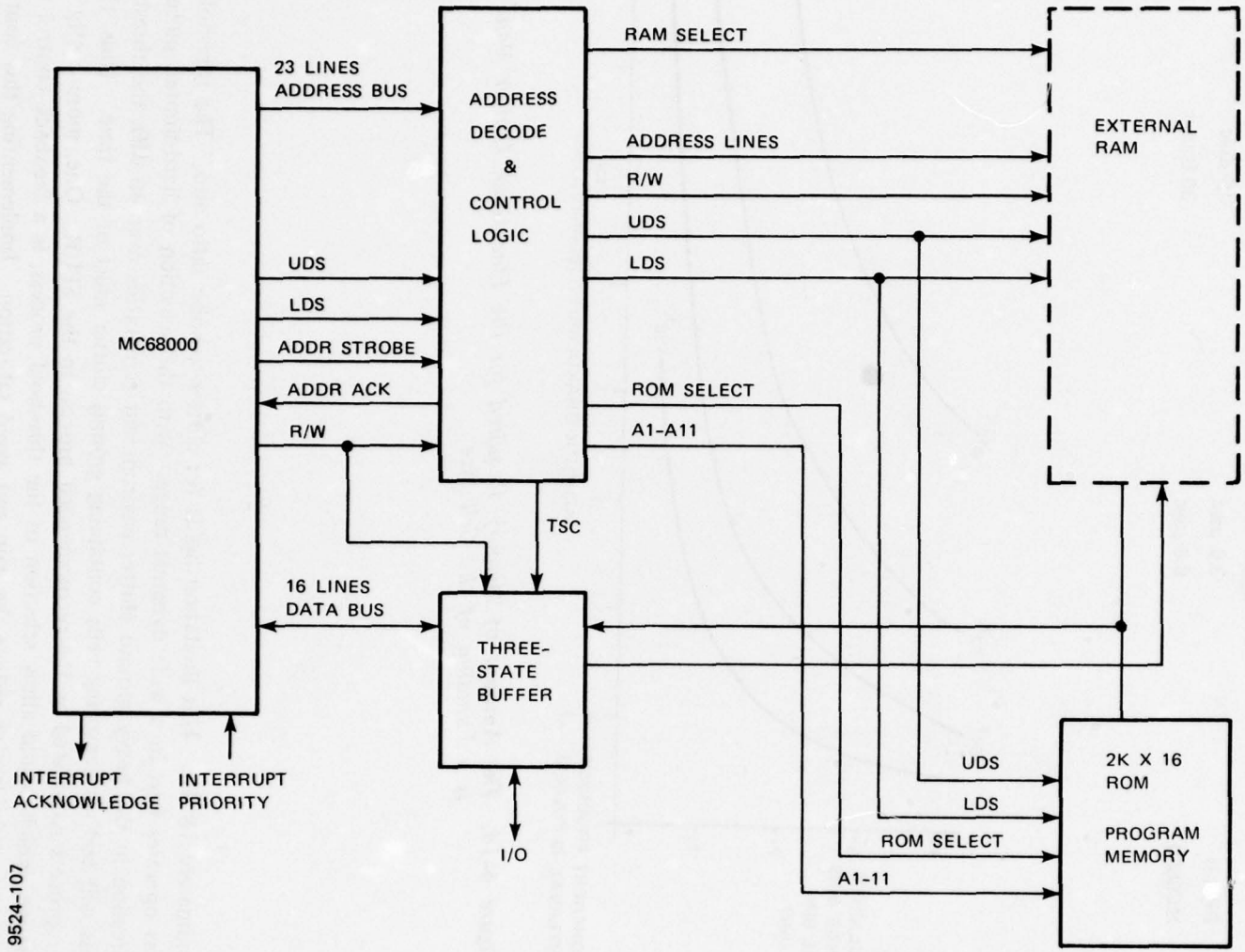
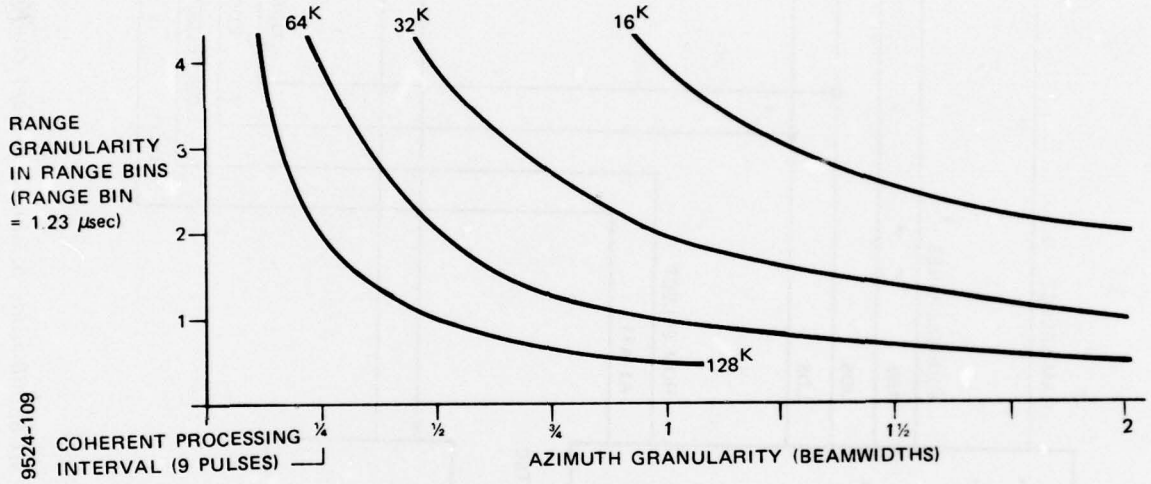


Figure 6-13. ***Block Diagram of the MC68000*** *leads to simple system configurations*

TABLE 6-XIII. THE EXECUTION TIMES PER CELL FOR THE RPM-II AND THE MC68000 are shown for the censor process and the threshold process

	Censor Process	Threshold Process
RPM-II	3.6 μsec	15 μsec
MC6800	6.6 μsec	30.8 μsec

9524-108



9524-109

Figure 6-14. The Amount of Memory Required for the Fine Grain Clutter Map is a Function of the Cell Size

approximately 18 dB. This limitation holds for clutter-to-noise ratio also. The threshold process operates best in a wide dynamic range. With the selection of hard-limited pulse compression in the heavy ground clutter environment (c/n ratios over 46 dB), the threshold process will end up censoring cells containing ground clutter most of the time. Thus, the censor process is selected as the recommended process in the SPUR. One, more costly alternative, which would allow selection of the threshold process, is a feedback control to the zero channel filter to reduce the gain and avoid saturation. Implementing this control requires a unique zero Doppler filter, thereby adversely affecting reliability and maintainability. Hence it was not considered further.

With the selection of the algorithm, the clutter map memory can be specified. A sequential observer algorithm is proposed for the censor process. As shown in Figure 6-15 this algorithm increments by 8 upon a hit in the cell and decrements by 1 upon a miss. The effective threshold, which defines the presence of ground clutter, is selected such that a crossing target will not trigger the cell. In this clutter map, six bits provide sufficient dynamic range for the sequential observer. Had a threshold process been selected, the dynamic range of the clutter map would have been much higher.

The SPUR clutter map, because of its large size, is a critical design. Two architectures using two technologies are compared: a CCD design using 64K devices and a CMOS memory design using 16K × 1 devices, which are projected to be available in mid-1980 (within the SPUR timeframe). Because of its high level of integration, the CCD design requires only 12 memory chips to provide the required storage and full redundancy in the map. The redundant map is powered down. In addition, a dual buffer is required to match the CCD clock rate of 1–5 MHz with the usage rate of the radar, which is controlled by the microprocessor. This small memory (256 × 8) requires two chips. The CMOS design requires 50 memory chips to accomplish the storage and provide the desired reliability. Its fault tolerance is improved by using a single error correction, double error detection code and a spare memory bank (16K × 6) which can replace any one of the four banks in use. The CMOS bank takes maximum advantage of the power down option by only having one bank of devices powered at any one time. The tradeoff matrix between the candidates (Table 6-XIV) shows an edge for the CMOS design, and thus it is selected as the SPUR memory choice.

Final selection in the implementation is between the RPM-II and the MC68000. Since programmable processing was considered for the Zero Channel Processor and the Postdetection Processor units, a combined implementation was investigated. This evaluation, based on the speeds of the units and the desirability of having one unit perform both tasks led to the recommendation of the RPM-II for the postdetection programmable processing. The MC68000, being a factor of two slower than the RPM-II, was marginal in performing both tasks, while the RPM-II was well within a conservative estimate.

SEQUENTIAL OBSERVER ALGORITHM

$$S_n = S_{n-1} + \delta$$

S_n = CLUTTER COUNT AT n^{th} SCAN

S_{n-1} = CLUTTER COUNT AT n-1 SCAN

$$\delta = \begin{cases} +8, \text{ FOR HIT ON } n^{th} \text{ SCAN} \\ -1, \text{ FOR MISS ON } n^{th} \text{ SCAN} \end{cases}$$

9524-110

Figure 6-15. The Sequential Observer keeps a Count Relative to Hits in each Cell in the Clutter Map

TABLE 6-XIV. CLUTTER MAP MEMORY CANDIDATES
evaluated in the SPUR optimization matrix

Criterion	Weighting	CCD Memory		CMOS Memory	
Reliability	10	4.56 f/10^6 hrs	11.3	10.0	4.05 f/10^6 hrs
Performance	10	Same	10.0	10.0	Same
Cost	7	1.0	7.0	10.8	1.54
Maintainability	6	On single board	6.0	6.0	On single board
Risk	6	1.0	6.0	7.2	1.2
Power	5	5.83W	10.8	5.0	2.6W
			51.1	49.0	

9524-111

6.8 POSTDETECTION PROCESSING TRADES

The Postdetection Processing Function performs a sequential greatest-of operation across the Doppler filters followed by postdetection integration over about one radar beamwidth (four hits). The integrated output is examined by detection logic which makes the decisions regarding target presence/absence for output to the data processor.

Four design alternatives were configured for the SPUR postdetection integrator (Figure 6-16), but after consideration of detection losses relative to linear integration, the choices were reduced to the binary and multinomial detections for detailed evaluation.

The binary detector considered is the common moving window detector which makes use of the double-threshold or binary method of integration. The radar video is thresholded by a primary comparator and the resulting binary data (0/1) is integrated over one radar beamwidth by moving-average logic (m-out-of-n process). For the SPUR, since four hits are available, n = 4. In calculating performance of the binary integrator, m was set to 2 since it has been shown that values of m approximately equal to n/2 are optimum for this type of integrator.

Since, as discussed in Section 6.7, the RPM-II has been selected as the programmable module for performing the Zero Channel Process and the Postdetection Process, the block diagram of the m/n detector is as shown in Figure 6-17. The interface board consists of the greatest-of logic, the first level comparator, and buffer memory before the RPM. A shift register memory stores the outputs of the comparator for an entire sweep (550 range bins) before transferring this data to the 4-bit wide FIFO stack. This stack is used such that the RPM-II can operate on 4-bit wide data to perform the 2/4 sliding window process. The FIFO stack and rotation logic are shown in Figure 6-18. After performing the m/n process, the RPM-II strobes the results into an output shift register which is interrogated by the data processor for subsequent processing.

The RPM program designed to perform the 2/4 binary process is shown in Figure 6-19. The maximum time required for this subroutine is 1.65 msec per 550 range bins. However, the algorithm execution time is data dependent. The minimum execution time for 550 range bins is on the order of 0.8 msec. In general, the average execution time would be closer to the lower value because most m/n comparisons will not result in a threshold crossing.

The second method of postdetection integration considered is the multinomial detector. This digital detector is so named because, while it is still a double threshold process, the output of the first-threshold process is quantized to more than 1-bit. As tabulated in Section 3.4, the loss due to postdetection integration drops from the 1.1 dB of the binary detector to 0.4 dB when two bits are used in the first-threshold. Thus for the SPUR, a multinomial detector using two bits at the output of the first-threshold was evaluated.

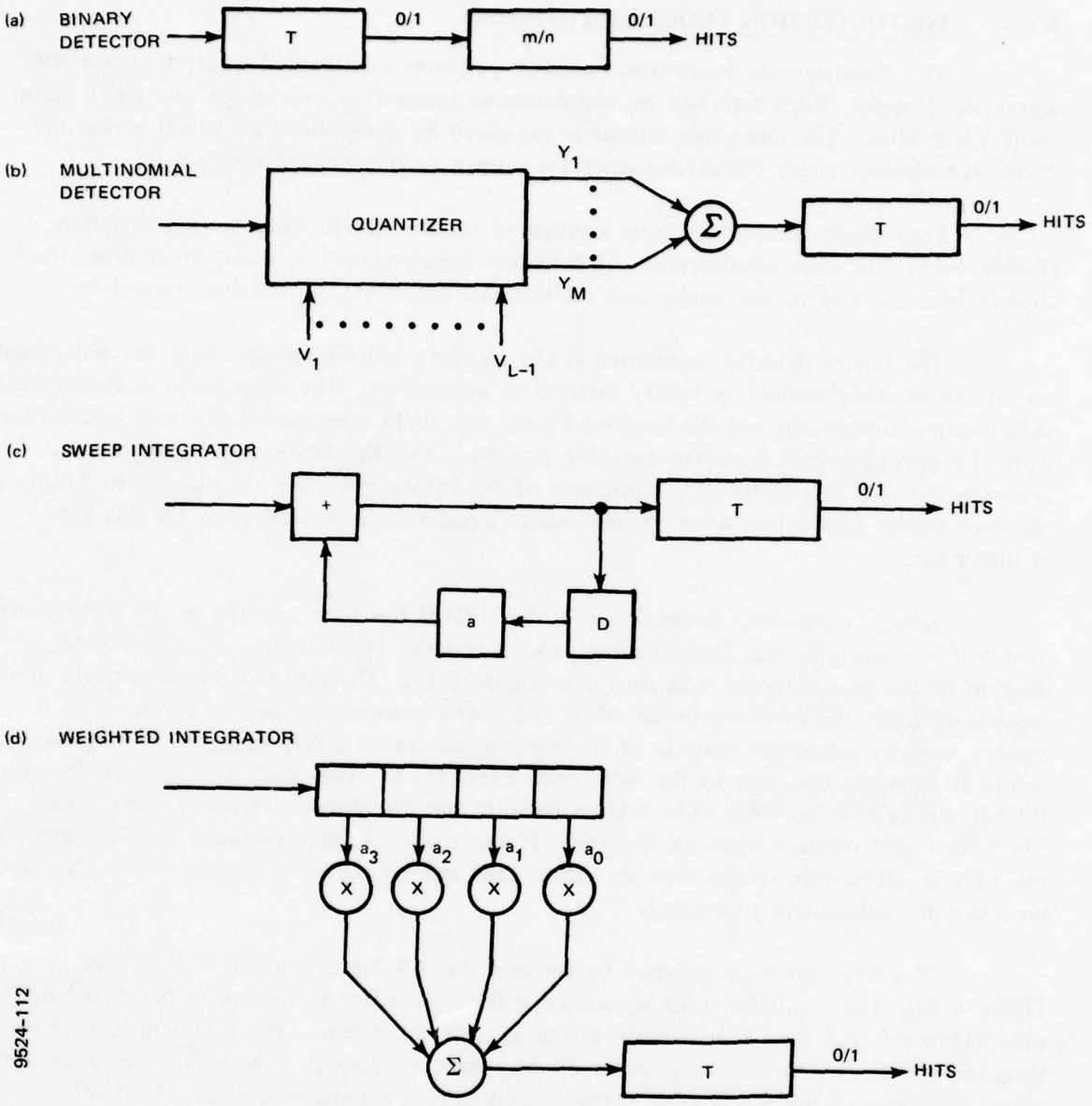


Figure 6-16. Four Methods of Postdetection Integration Originally Considered for the SPUR

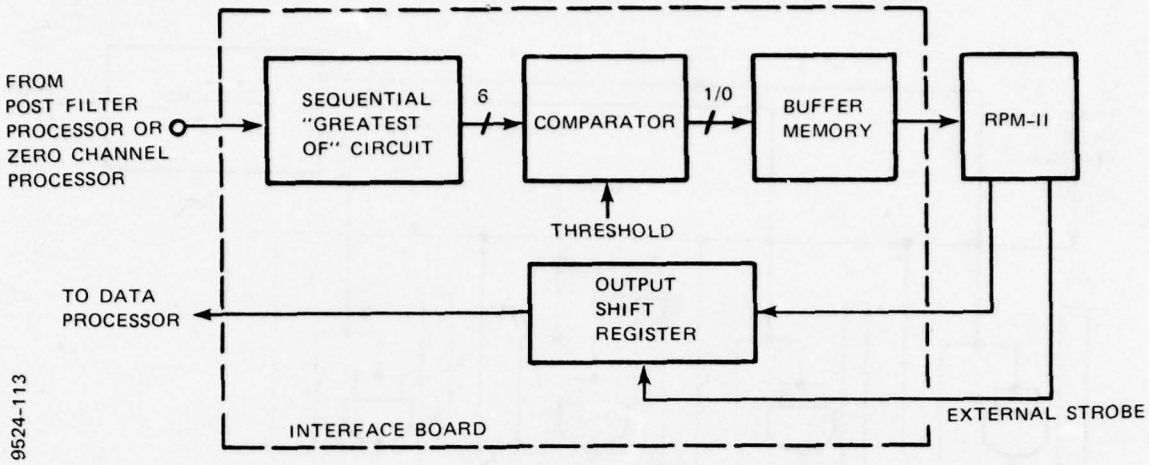


Figure 6-17. The m/n Binary Detector, as on Candidate for the Postdetection Processor, is configured on an interface board and the RPM-II.

The multinomial detector quantizes the input digital video into one of four levels (represented by 2-bits), by comparison with three thresholds (see Figure 6-16b). The integrator sums the quantized outputs to obtain the detection statistic

$$Z = \sum_{i=1}^{4} Y_i$$

which is compared to the second threshold. The performance for the SPUR was evaluated for threshold settings as shown in Table 6-XV.

The block diagram for the multinomial detector (Figure 6-20) is configured (similar to the binary detector) as an interface board and the RPM-II. Similar functions to the binary detector are also performed but now they generate and operate on 2-bit data instead of binary data. The outputs are similarly provided to a shift register which is interrogated by the data processor for further processing.

The RPM-II program for performing the multinomial detection is shown in Figure 6-21. The time required for this program to operate on 550 range bins is constant at 1.95 msec because it is not data dependent.

The comparison between the binary and multinomial detection processes is contained in Table 6-XVI. The costs, power and reliability are calculated only for the interface board in this table because the RPM is common to both processes. The multinomial detector is recommended because of its performance advantages over the binary detector.

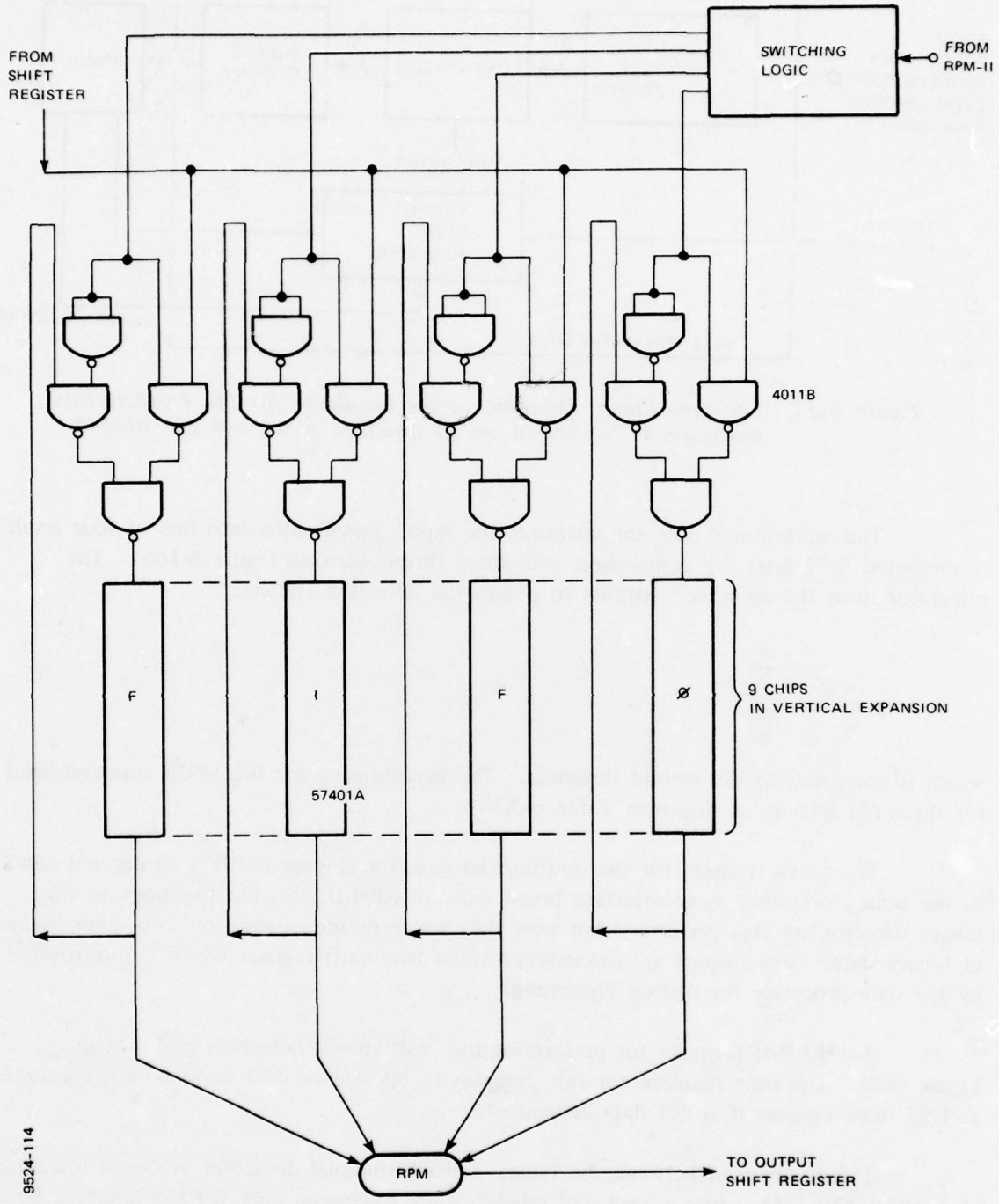


***Figure 6-18. Data for 2/4 Detection** is buffered by a FIFO stack and rotation logic*

```
                    RPM – POST DETECTION INTEGRATION
                    CALL PDI

                    SUBROUTINE (PDI)
                    B REGA TOREGA
                    REGA OR V(18000) TOREGB
                    A P1 TOREGA
                    REGA XOR V(10000)
                    GOTO (PDI1) IF ALUZ
                    REGA XOR V(10001)
                    GOTO (PDI1) IF ALUZ
                    REGA XOR V(10002)
                    GOTO (PDI1) IF ALUZ
                    REGA XOR V(10004)
                    GOTO (PDI1) IF ALUZ
                    REGA XOR V(10008)
                    GOTO (PDI1) IF ALUZ
                    B V(10001) ES(1)
                    GOTO (PDI2)
PDI1                B V(1000) ES(1)
PDI2                RETURN
```

9524-115

Figure 6-19. The Subroutine for Performing a Sliding 2/4 Detector in the RPM-II is Optimized for Fast Processing

TABLE 6-XV. PERFORMANCE OF THE MULTINOMIAL SELECTOR
evaluated for a specific set of thresholds

Conditions		First Thresholds			Second Threshold
M	P_f	V_1	V_2	V_3	W
4	10^{-6}	2.105	3.147	3.921	7

9524-116

TABLE 6-XVI. THE MULTINOMIAL DETECTOR IS SELECTED
based on its superior performance

		Multinomial		Binary	
		Data	Rating	Rating	Data
Reliability	10	5.60 f/10^6	20.4	10.0	2.74 f/10^6
Performance	10	-0.4 dB	10	37.5	-1.1 dB
Cost	7	1.89	13.2	7.0	1.0
Maintainability	6	Same	6.0	6.0	Same
Risk	6	1.1	6.6	6.0	1.0
Power	5	21.6W	9.0	5.0	12W
			65.2	71.5	

9524-119

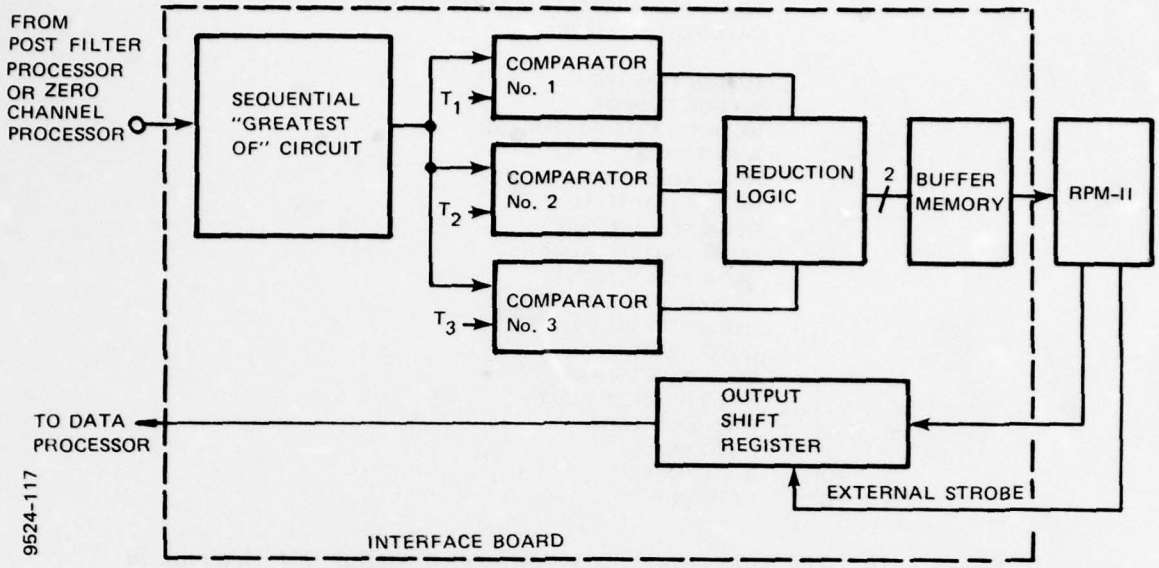


Figure 6-20. ***The Multinomial Detector Candidate*** *is configured similarly to the binary detector.*

```
                (RPM) – POST DETECTION INTEGRATION
                CALL PDI

                SUBROUTINE (PDI)
                B REGA TOREGA
                REGA OR V(10000) TOREGB
                B V(7) TOR(7)
                A P1 TOREGA
                REGA AND V(10003) TOR (0)
                REGA AND V(100012) DSR TOR(1)
                REGA AND V(100150) DSR TOREGA
                A REGA DSR TOREGA
                REGA AND V(10003) TOR(2)
                REGA AND V(100012) DSR TOR(3)
                AR(0) ADD BR(1) TOR(0)
                AR(0) ADD BR(2) TOR(0)
                AR(0) ADD BR(3) TOR(0)
                AR(7) SUB BR(0)
                GOTO (PDI1) IF ALUPOS
                B V(10001) ES(1)
                ES(2)
                GOTO (PDI2)
PDI1            B V(10000) ES(1)
                ES(2)
PDI2            RETURN
```

9524-118

Figure 6-21. ***The Subroutine for Multinomial Detection operates on 550 range bins in 1.95 msec.***

Section 7

PROCESSOR RISK AREAS AND PHASE II VALIDATION PLAN

7.1 PROCESSOR RISK AREAS

The major processor risk areas have been identified and are discussed below. These risks are broken into two groups – overall processor level risks, and specific risks associated with individual functions and units. The Phase II Validation Plan, which includes the Test Plan of Appendix A, is designed to reduce these identified risks by analysis and appropriate testing at the function, processor, and system levels. Table 7-I summarizes the major identified risks and proposed techniques for their reduction.

7.1.1 Processor Level Risks

At the processor level two major risk areas are of special importance. These are: a) automatic testing and calibration of the processor analog circuitry, and b) fault isolation and reconfiguration for the various functions. Automatic testing and calibration are accomplished by using feedback loops with relatively long time constants to monitor and control analog elements of the processor. These loops correct for drift and temperature variation of the circuitry relative to stabilized references. A second method of minimizing risk in this area is the early conversion into the digital domain which is essentially independent of aging and temperature drift effects.

The fault isolation and reconfiguration risks in the processor have been addressed by utilizing a distributed BITE approach with a centralized focus for control and monitoring of the processor status. The distributed BITE will isolate faults within a function and, in some cases, direct the reconfiguration of that function. In addition, a message is sent to the STATE processor which can also invoke reconfiguration in some functions. The STATE processor provides the centralized focus for the reliability and status of the processor. As such, it must be much more reliable than any of the other constituent parts. It must also be programmable to allow for improvements and additions as the processor is developed.

These overall risks have been carefully considered during the Phase I activity and will receive special attention during the detail design of Phase II. Verification of our recommended approaches for reducing the risks will be carried out during the testing of Phase II.

7.1.2 Function or Unit Level Risks

In addition to the overall processor risks mentioned above, several risk areas associated with specific processor functions have also been identified. While not explicitly called out in all of the functions below, it is obvious that the reliability, fault detection, and reconfiguration capabilities of each of the units are important characteristics. Risks associated with these characteristics have been addressed and the units are designed with these factors

TABLE 7-I. MAJOR PROCESSOR RISKS AND RISK REDUCTION APPROACHES

The major processor risks have been determined and plans developed for reducing these risks

Risks	Risk Reduction Approach
Processor Level	
Automatic Testing and Calibration of Processor Analog Circuitry	Calibration Feedback Loops Early Conversion to Digital Domain Hardware Demonstration and Test
Fault Isolation and Reconfiguration of Processor Functions	Distributed BITE STATE Processor Hardware Demonstration and Test
Function or Unit Level *	
Analog and A/D Processing Function Implementation and Cost	Detailed Design and Analysis
Doppler Processing Function Achievable Improvement Factor Filter Losses	Analysis and Hardware Demonstration
Post Filtering Processing Function Pulse Compression and CFAR Losses	Analysis and Hardware Demonstration
Zero Channel Processing Function and Post Detection Processing Function Algorithm Selection Clutter Map Cell Sizing	Analysis and Hardware Demonstration
STATE Processor	
Monitor and Control other Processor Functions	Detailed Design and Hardware Demonstration

9524-36

* Reliability and Intraunit Reconfigurations are potential risks to all units and will be addressed during Phase II through Analysis and Hardware Demonstration

receiving special attention. During Phase II, reliability will be verified through analysis of the detailed circuit designs with MIL-HDBK-217B as the principle guide. Fault detection and reconfiguration within the units, where appropriate, will be demonstrated using the developed hardware and software.

Analog and A/D Processing Function – The testing and calibration problems inherent to analog circuitry are discussed in the overall processor risks above. In addition, there are potential implementation and cost risks associated with the selection of 11 bits of dynamic range. Our basic design approach with the two-stage A/D converter is intended to minimize these problems. A detailed design will be developed during Phase II to further reduce these risk factors.

Doppler Processing Function – The major risk associated with this function is achievement of the required MTI Improvement Factor, particularly against bimodal clutter and second-time-around clutter. This risk is minimized by selection of the Near Optimum Filter Bank and application of CFAR individually to each filter in the bank. Processing losses are an additional area of potential risk. Analysis has been used to calculate the achievable Improvement Factor and processor losses, and several tests are proposed to measure these characteristics during Phase II.

Postfiltering Processing Function – This function performs the biphase coded pulse compression and envelope detection. The principle risks in this area are related to the s/n loss for high velocity targets and for the hard limiting CFAR. These risks will be minimized through analysis and demonstrations in the test bed system.

Zero Channel Processing Function and Postdetection Processing Function – The principle risks associated with these functions relate to the processor noise loading, selection of algorithms, and the cell-sizing in the clutter map. Noise loading impacts the speed and complexity of the processing functions and will vary somewhat for different radar designs. Our baseline radar design, given in Section 1-2, assumes reasonable noise levels and false alarm requirements. Substantial changes may require faster and more complex processing. Risks associated with algorithm selection and cell-sizing will be reduced during the design phase and verified with hardware tests. The prf stagger must also be properly chosen to ensure high probability of detection as a function of target Doppler.

STATE Processor – The primary risks of the STATE Processor relate to its internal reliability and its ability to monitor and control the other processor functional areas. Once again, these risks will be reduced by analysis and detailed design during Phase II, and its performance will be verified through testing and hardware demonstrations.

7.2 PHASE II VALIDATION PLAN

The prime objective of the Phase II effort is to verify the characteristics of the processor design selected during Phase I. The principle verification procedure is outlined in the Phase II Test Plan of Appendix A. In order to maximize the expected benefits of the effort subject to the fixed cost constraints of the contract, we will use existing or modifiable equipment to the maximum extent possible. Also, emphasis will be placed on fundamental principles rather than on particular components and specific detailed designs. For example, reliability demonstrations will concentrate on processor architecture and fault-tolerant designs rather than on the reliability of individual components. This approach is adopted in order to avoid lengthy and expensive component reliability test programs, the results of which have applicability only to the components themselves and thus may be rendered obsolete by new devices or technology.

7.2.1 Functional Performance Verification

In accordance with the Statement of Work, verification of the functional performance of the SPUR is one of the major objectives of the Phase II program. Our approach is to combine analysis and hardware demonstration in accomplishing this objective. Analysis is used first in establishing the basic performance requirements for the functional areas of the SPUR. Furthermore, during various stages of the hardware tests, analysis will be applied to ensure that the synthesized system satisfies the program requirements. This will be especially important in analyzing the results obtained in our L-band Test Bed facility where the SPUR will be integrated into a working 2D radar. In particular, operation of the SPUR in severe clutter will be demonstrated using the test bed system, and sufficient analysis will be conducted to assure adequate clutter suppression.

All of the hardware developed for the SPUR will be tested to verify the functional performance. For example, each unit will be operated at speeds sufficient to meet the processing time requirements. Dynamic range and memory tests will be conducted to ensure compatibility with clutter models. CFAR and pulse compression algorithms and circuits will be verified.

Performance tests will generally be conducted at three levels. The first is at the unit level where the specific characteristics of that unit, independent of the other processor elements, are verified. The second level involves testing of the units as an integrated processor. The top level of performance testing will be in the test bed where actual operation in a radar will be demonstrated.

7.2.2 Power Consumption Verification

Units developed for the SPUR will be tested for power consumption. This characteristic was one of the major design considerations of the Phase I effort, and sufficient elements of the processor will be developed to permit a very good estimate for the power consumption of the total SPUR. Dual-redundant, split power supplies will be required in the final SPUR; however, laboratory supplies will be used in conducting the hardware tests. Power supply efficiency will be considered in determining total SPUR power requirements.

7.2.3 Reliability Verification

Verification of the SPUR reliability is a top priority objective of the Validation Plan. As discussed above, we will concentrate on verifying the basic processor architecture rather than the reliability of specific components. In addition to maximizing the potential benefits of the development and test effort, an additional reason for this approach is that even very high reliability components will still require some degree of redundancy and fault tolerance in order to meet the total SPUR MTBF goals. When redundancy is used, the processor reliability becomes less sensitive to the reliability characteristics of the constituent elements. Moreover, once the fault detection logic and switching implementations are determined, it becomes relatively simple to add additional redundant units. While there are

obvious cost tradeoffs to be considered here, emphasis on processor architecture provides a great deal of flexibility in compensating for the reliability characteristics of the particular components used in a unit.

MIL-HDBK-217B and 217C will be used in predicting the worst-case reliability of the various components of the SPUR. In addition, a general reliability computer program, ARIES (Automated Reliability Interactive Estimation System), developed at UCLA, will be used in optimizing the total reliability of the processor.

A major consideration in developing and testing a high reliability processor, such as SPUR, is that of coverage. This characteristic determines the capability of the processor to recover from a fault through use of redundancy and fault-tolerant elements. For example, achieving 100 percent coverage in a function provides complete protection for any fault within that function. As an illustration, the entire processor could be replicated in standby redundancy. With appropriate detection and switching circuitry, this provides 100 percent coverage; however, it is not a very cost-effective approach. In development of the SPUR, coverage is considered for each of the processor units.

Testing coverage characteristics of the SPUR will be conducted during Phase II. This testing will be carried out at both the unit and processor level tests. These tests will include exercising the fault detection and isolation logic, verifying the reconfiguration operation, demonstrating the proper operation of fault-tolerant circuits, generating fault reports and status messages, evaluating degraded mode operation, etc. All of these factors will be included in the final reliability analysis of the SPUR.

7.2.4 Performance Monitoring/Fault Isolation Verification

Closely related to the reliability demonstrations are the performance monitoring and fault isolation verification tests. These characteristics will be used for reconfiguring redundant units and tested as part of the reliability tests. Monitoring and fault isolation will also be implemented and tested for units which do not incorporate redundancy. In these cases, a processor failure or degraded operation results, and status messages are required to facilitate repair activities.

7.2.5 Stability Verification

Short-term circuit stability and automatic adjustment and alignment will be demonstrated during the Phase II effort. Direct verification of long-term stability will not be possible during the time frame of the demonstration effort. However, fault monitoring and automatic adjustment features will be demonstrated to verify their effectiveness against such long-term effects. Moreover, sufficient component analysis will be conducted to determine the inherent stability characteristics of the components, both with aging and as a function of temperature. Where analysis so indicates, temperature stabilization techniques will be implemented and limited temperature cycling tests conducted on these devices.

7.2.6 Design Integrity Verification

Throughout the Phase II effort we will continuously review the progress relative to the Phase I projections – with special emphasis on the parameters of reliability, performance, and power consumption.

The Phase II effort will begin with generation of Unit Design Requirements (UDRs) based on the in-depth design of the recommended approach of Phase I. The UDR is developed by the designer and defines the required parameters of the circuits to be developed and the designer's method of development. As soon as draft versions of the UDRs are prepared, a Conceptual Design Review (CDR) will be held. This review is intended to ensure that the designer fully understands the requirements of his equipment – including functional performance, reliability, reconfiguration capability, interfaces, etc. After the Conceptual Design Review, the UDRs will be finalized and detailed circuit design begins.

Approximately one month after the CDR, an Analytic Design Review will be conducted. This review will focus on the initial parameters of designed-in reliability and maintainability, power consumption, and the balance of these parameters with performance. At this review, the designer will present his reliability estimates and maintainability features, power consumption estimates, any specialized circuitry required, for example, to maintain equipment stability, and the supporting analysis documenting his design decisions.

The Final Design Review (FDR) is scheduled to occur three months after the start of Phase II. At this time, the paper design will be complete, and the review will be held to ensure that the design meets all the requirements, all interfaces have been incorporated, the testing procedure is fully established, and that the unit is ready for fabrication. At this time, the tentative Test Plan developed in Phase I will be updated to conform with the specific requirements of the selected processor architecture. This updated Test Plan will be used during the testing operations of Phase II.

Following the FDR, hardware fabrication will begin. Testing of the hardware will be performed as an integral part of the fabrication process. Results of these tests shall be continuously reviewed to ensure that the results are compatible with both the designer's predictions and the requirements allocated to that unit. Upon completion of the design, the unit will enter the Unit Level Test Phase described in the Test Plan.

7.2.7 Test Equipment and Instrumentation

To facilitate verification of critical SPUR areas, we will make maximum use of existing test equipment and other associated in-house radar hardware. This will include standard laboratory test equipment in addition to the ITT Gilfillan L-band test bed facility.

The L-band test bed facility is a high-performance 2D radar installed in our main plant in Van Nuys, California. Our location in the middle of the San Fernando Valley is ideal for demonstrating some of the basic performance characteristics required of the SPUR.

The valley is surrounded by mountains and provides severe ground clutter environment. Seasonal storms also provide opportunities for evaluating processor performance in the presence of strong rain clutter. Moreover, our location between the Van Nuys and Burbank-Pasadena-Glendale Airports provides a large number of aircraft targets-of-opportunity. Additional information describing our test bed facility is provided in Appendix B of this report.

During the system level tests of Phase II, PPI photographs will be used in evaluating SPUR effectiveness in suppressing clutter and providing high probabilities of target detection. Simulation will also be used, where appropriate, to support the analysis and demonstration effort. We will use our existing in-house computer facility for this purpose.

7.2.8 Schedule

A schedule for the Phase II program is provided in Figure 7-1. Milestones have been established for completion of the various reviews and tests. During the early part of the Phase II effort, a detailed schedule for each unit will be developed. As a result, some modifications of the schedule are expected; however, these should be minor and will not delay completion of the test program.

7.2.9 Data Collection and Analysis

The tests and demonstrations to be conducted do not require the use of extensive data collection equipment. In general, data will be collected manually, using standard laboratory and radar test equipment. Analyses of results will be carried out in the most appropriate manner, depending on the particular results. While we will not specifically test component level reliability; component failures will be analyzed in sufficient detail to determine that the failures did not result from improper operation or overstressing of the components.

In cases of less than predicted performance, sufficient analysis will be conducted to determine the reason(s) for the discrepancy. Minor problems will be corrected and the equipment retested. Problems which result in substantial equipment redesign or complex test procedures will be identified, and the analysis will be repeated based upon the modifications. In these cases, however, equipment modifications will not be implemented.

Upon conclusion of the tests, all pertinent test results will be incorporated into a final analysis of a total SPUR. Extrapolations will be performed, where required, to account for the limited time and complexity of the tests. A detailed processor configuration with its expected operating parameters and performance characteristics will result.

7.2.10 Test Report

Test results will be documented and presented to the Air Force in a Test Report of ITT Gilfillan format. This report will be included in the Phase II Technical Report scheduled for delivery 13 months after exercise of the Phase II option.

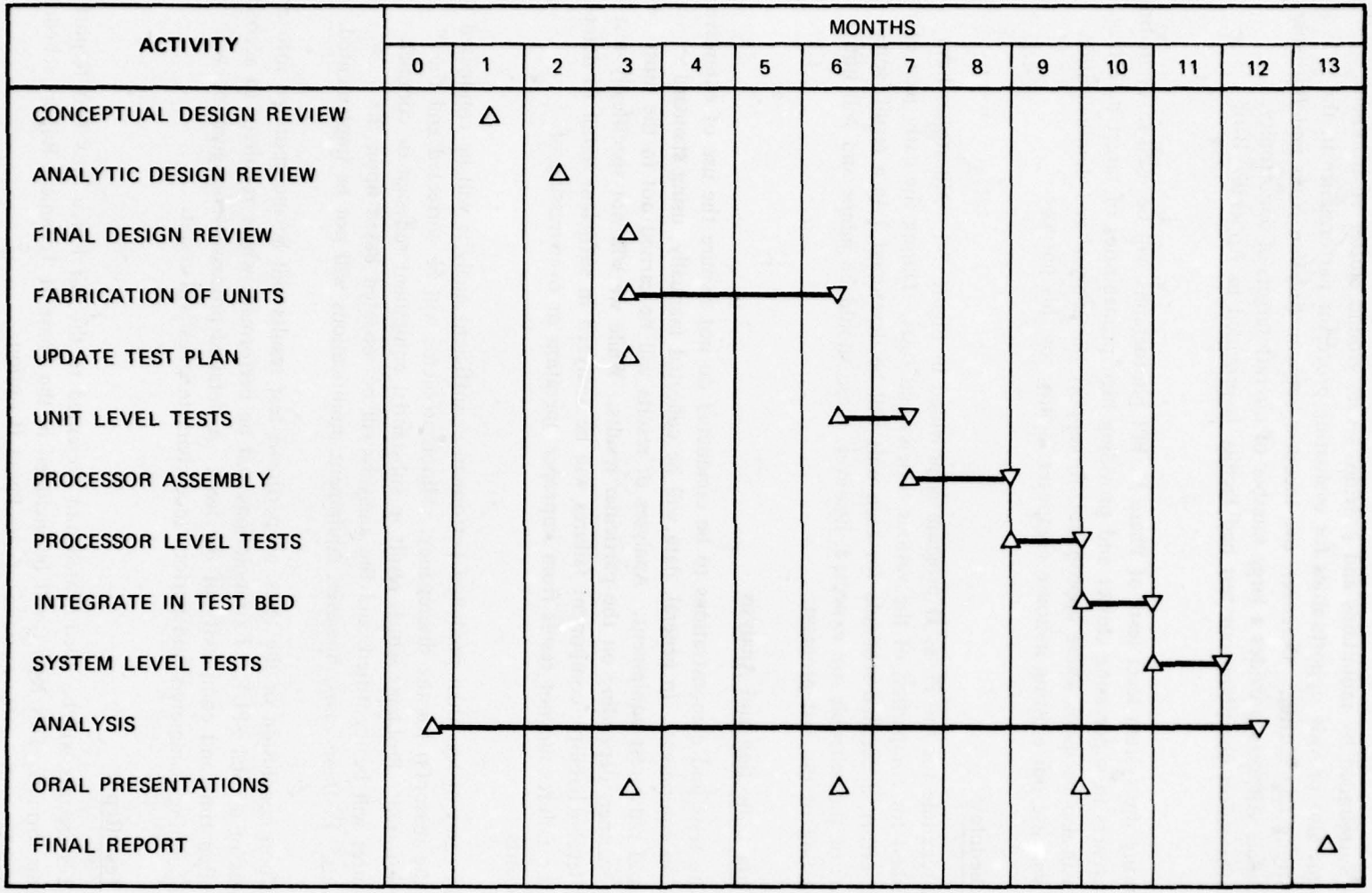


Figure 7-1. A Schedule for the Various Activities of the Phase II Program

Appendix A

PHASE II TEST PLAN

This Appendix describes the test plan that has been developed for implementation during Phase II of the SPUR contract. Objectives of this plan are to verify the essential characteristics of the unattended radar signal processor identified during Phase I of the SPUR effort. These characteristics include the following:

a) Functional performance,
b) Power consumption,
c) Reliability,
d) Performance monitoring/fault isolation,
e) Stability.

The test program described herein has been structured to demonstrate the above characteristics in a cost-effective manner. In particular, maximum use is made of available equipment and components. Moreover, emphasis has been placed on verifying the basic principles of high-performance and high-reliability designs, with less attention given to the specific devices themselves. In particular, there are no plans for reliability testing at the component level.

As specified in the contract Statement of Work, this plan will be revised and updated during the Phase II effort. Revisions are expected to be minor, consisting primarily of refinements developed during the detailed design process.

A.1 TEST PROCEDURES

The procedures to be followed in verifying the critical SPUR areas are discussed below. Selection of the specific procedure for testing a particular unit is determined by trading off the cost of the test including unit fabrication versus the potential benefits in reducing the risks.

a) **Analysis** – Analysis, including simulation will be conducted during Phase II with two principle objectives – to verify the design requirements established for the processor units and to insure that the units and processor as a whole will satisfy the requirements of the SOW. Much of the analysis has been completed in Phase I; however, some analysis will be carried out in more detail in Phase II, and it will incorporate any changes that result during this phase.

   In the reliability area especially, there will be a great deal of reliance on analysis both for reliability predictions and for Failure Modes and Effects Analysis. While redundancy switching and self-healing operations will be demonstrated as part of the test plan, overall processor reliability will be determined by analysis.

b) **Unit Level Tests** – Testing at the unit level (viz., Doppler Module, A/D Converter, etc.), shall be used in verifying the characteristics peculiar to each unit. Included in this category of tests are parameters such as speed, power, intraunit fault detection, etc. Internal reconfiguration or automatic calibration will also be demonstrated for units designed with these capabilities.

c) **Processor Level Tests** – These tests will be conducted on the integrated processor hardware. The interfaces between processor units will be verified at this level as part of the processor integration. In addition, tests shall be run to verify the fault detection properties of the processor and to demonstrate the interunit reconfiguration operations. Furthermore, status monitoring and message reporting will be verified.

d) **System Level Tests** – Tests at the system level will be conducted using the L-band test bed facility at ITT Gilfillan. These tests shall be used to determine the basic functional performance of the processor in an actual severe clutter environment. In addition, these tests shall be used to verify the functional requirements developed by analysis for the various units within the processor.

A.2 DETAILED TEST DESCRIPTION

The generic block diagram of Figure A-1 illustrates the five basic functions which comprise the SPUR. This functional breakout is sufficiently general to permit optimization of the individual functions, and, at the same time, is specific enough to support the identification and design of the processor units within each function.

The principle activity of Phase I was to determine the optimum configuration of the processor. In terms of the generic block diagram of Figure A-1, this required identifying the specific operations associated with each function and, simultaneously, the most effective implementation approach for each operation. Figure A-2 illustrates, at the unit level, the processor recommended as a result of the Phase I effort.

The major units of the processor are described below, along with the validation procedures for each. General specifications for the units have been developed, and these are included in the unit descriptions. Verification worksheets are also provided for each unit. The major characteristics of each unit are listed on these sheets, and, associated with each applicable characteristic, is the requirement for that unit. These requirements are generally derived from the higher level processor requirements and in many cases are more appropriately classified as design goals.

During the detailed design process of Phase II, all requirements will be continuously addressed and reallocations will be established as necessary. Any changes that result will be incorporated in the updated test plan to be submitted in Phase II.

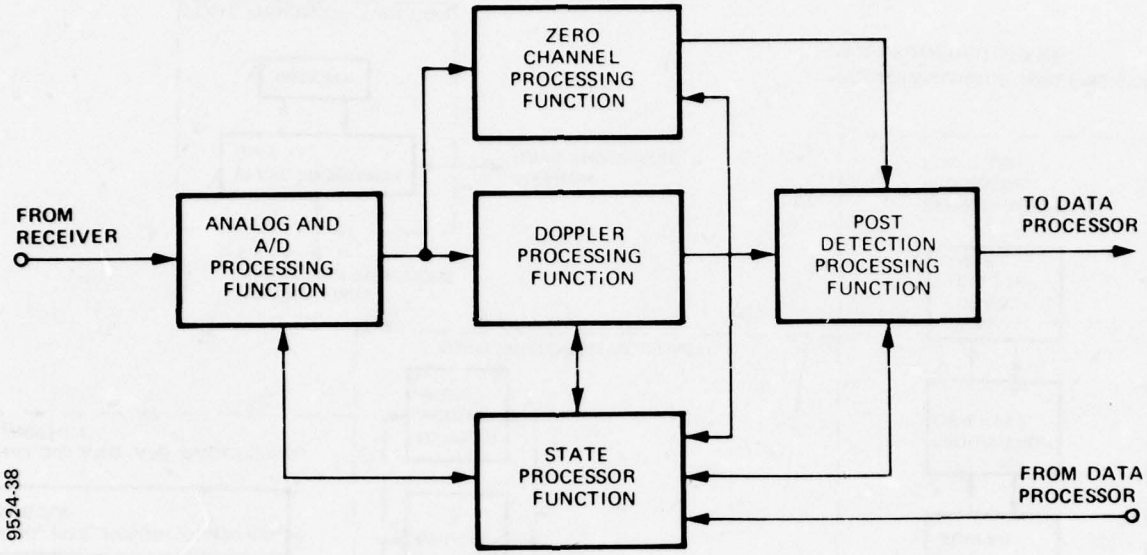


Figure A-1. SPUR Generic Block Diagram depicting Processing Functions

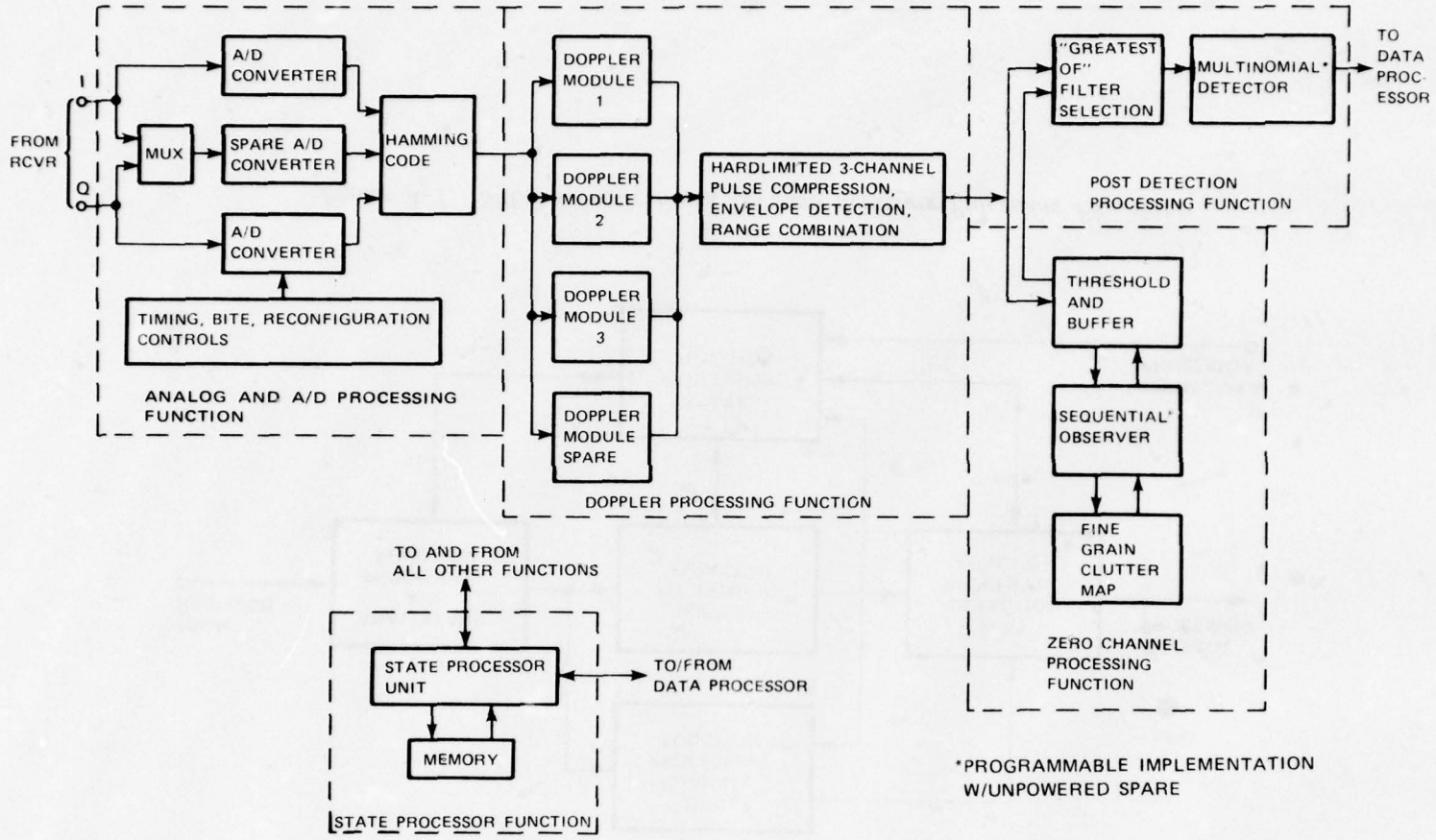


Figure A-2. Unit Level SPUR Block Diagram for Recommended Processor

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A.2.1 A/D Converter

For the processor under consideration, the A/D converter is considered a critical item. The dynamic range, sampling stability, and speed must be sufficient to satisfy the overall system requirements of clutter rejection, range bin size, and processing losses. Furthermore, the presence of analog signals and circuitry imposes the requirement for automatic calibration techniques to account for long- and short-term drift problems. Also, the converter reliability, fault detection and reconfiguration capabilities are important considerations and should be verified.

Table A-I is a set of preliminary specifications for the A/D converter. These have been developed based on the total system requirements and are considered reasonable for use in an unattended radar. (Note: The gain and absolute linearity requirements are less critical than the differential linearity, feedthrough, and crosstalk requirements since the application requires relative and not absolute values.)

Unfortunately development of an A/D converter with all of these capabilities is expensive and would seriously limit the resources available for the rest of the verification plan. Consequently, we propose to verify the A/D converter through the following procedure:

a) Design and develop automatic calibration circuitry;

b) Test calibration circuitry with commercial A/D;

c) Develop fault detection circuitry and multiplexer switch;

d) Test fault monitor and switch with commercial A/Ds;

e) Implement system level tests with high-speed commercial, or in-house developed, A/D;

f) Conduct preliminary design of two-step flash A/D converter unit;

g) Develop power, reliability, cost, environmental factors, and special handling characteristics from the preliminary design and developed hardware.

The verification worksheet for the A/D converter is given in Table A-II.

A.2.2 Doppler Module

The Doppler module is also considered to be a critical item in the SPUR concept. We propose to design, develop, and test two of these modules during Phase II.

Table A-III provides a list of major performance specifications for the Doppler module, and the verification worksheet of Table A-IV identifies the validation procedures to be followed for the various parameters.

TABLE A-I. ANALOG/DIGITAL CONVERTER SPECIFICATIONS

Speed	0.618 μsec maximum conversion time (Both I& Q)
Dynamic Range (Resolution)	11 bits
Power Consumption	38 watts
Losses	0.35 dB Quantization 0.8 dB Range Straddle (double sampling)
Calibration	dc Offset Control Loop
Reliability	9.14 f/10^6 hours
Reconfiguration	2 converters with 1 hot standby
Modularity	1 board for complete unit
Environmental	0° – 120°F Operating; -70° – 100°F Storage
Interfaces	Receiver/Doppler Modules/STATE
Linearity	±1%
Differential Linearity*	±1 LSB
Gain	±1%
Feedthrough	±½ LSB
Crosstalk	±½ LSB

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*Monotonic over required temperature range. No missing codes.

TABLE A-II. VERIFICATION WORKSHEET FOR A/D CONVERTER

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	0.618 μsec Conversion Time (Both I & O)	X			X	Commercial or In-House A/D
Dynamic Range	11-Bits	X	X		X	Commercial or In-House A/D
Memory Size						
Power	38 Watts	X	X			
Losses	0.35 dB Quantization 0.8 dB Range Straddle	X			X	Commercial or In-House A/D
Program Instructions	N/A					
BITE/Calibration	dc Offset Control Loop	X	X			
Reliability	9.14 f/10^6 hr	X				MIL-HDBK-217B,C
Reconfiguration	2 of 3 Required		X	X		Demo switching
Modularity	1 board					
Environmental	0°–120° F Operating -70°–100° F Storage	X	X			
Special Handling	None	X				
Interfaces	Receiver/DM/STATE			X		
Other (Linearity, Gain, Feedthrough, Crosstalk)	A/D Specifications		X			

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TABLE A-III. DOPPLER MODULE SPECIFICATIONS

Speed	1.6 MHz Input Data Rate (I & Q)
Dynamic Range	11-bits Input/1-Bit Hard-limited Output
Memory Size	229K bits
Power Consumption	25 watts
Losses	1.8 dB
Program Instructions	Filter Weight Selection
BITE	Test Case
Reliability	7.24 f/10^6 hours
Reconfiguration	3 out of 4 cold standby redundancy
Modularity	1 DM/board
Environmental	0°–120°F Operating; -70°–100°F Storage
Special Handling	Grounded Pins Carrier for CMOS Memory
Interfaces	A/D/Postfiltering Processor/STATE Processor

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For the complete SPUR, three parallel modules will be required to cover the Doppler spectrum, with a fourth channel added to provide redundancy. Since the modules are all identical except for the filter weights, we consider two channels sufficient to demonstrate all of the principle features, including fault detection and reconfiguration switching.

A.2.3 Postfiltering Processor

The Postfiltering Processor will consist of the biphase coded pulse compression unit and the envelope detector. Specifications for these functions are provided in Table A-V. During Phase II the following activities relating to the Postfiltering Processor will be conducted:

a) Test a three-channel biphase coded pulse compression unit that is being developed in-house. Three channels are used to provide velocity offsets to reduce losses associated with high-velocity targets.

b) Design, develop and test the envelope detection circuit.

The verification worksheet identifying the level of testing for the Postfiltering Processor is provided in Table A-VI.

TABLE A-IV. VERIFICATION WORKSHEET FOR DOPPLER MODULE (DM)

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	1.6 MHz		X			Input Data Rate
Dynamic Range	11 Bits Input/Hard limited Output		X			Compatible with A/D
Memory Size	229 K bits	X			X	Words/Batch
Power	25 Watts		X			
Losses	1.8 dB	X			X	Near Optimum Filter
Program Instructions	Selection of Weights			X		
BITE/Calibration	Test Case			X		
Reliability	7.24 f/10^6 hr	X				MIL-HDBK-217B,C
Reconfiguration	3 of 4			X		Demo 1 of 2 Switching
Modularity	2 Units/Board		X			
Environmental	0°–120°F Operating -70°–100°F Storage	X				
Special Handling	Grounded Pins Carrier	X				
Interfaces	A/D/PFP/State			X		

TABLE A-V. POSTFILTERING PROCESSOR SPECIFICATIONS

Speed	1.82 MHz
Dynamic Range	1-bit Hard-limited Input; 6-bits Output
Power Consumption	16 watts
Losses	3.6 dB (including CFAR)
BITE	Test Case
Reliability	7.39 f/10^6 hours
Modularity	1 Board
Environmental	0°–120°F Operating; -70°–100°F Storage
Interfaces	Doppler Modules/Post Detection Processor/Zero Channel Processor/ STATE Processor

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TABLE A-VI. VERIFICATION WORKSHEET FOR POSTFILTERING PROCESSOR (PFP)

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	1.82 MHz		X			In-House Equipment
Dynamic Range	Hard Limited Input 6-Bits Output		X			In-House Equipment
Memory Size	None					
Power	16 Watts		X			
Losses	3.6 dB	X		X	X	Including CFAR
Program Instructions	None					
BITE/Calibration	Test Case					
Reliability	7.39 f/10^6 hr	X				MIL-HDBK-217B,C
Reconfiguration	None					
Modularity	1 Board		X			
Environmental	0°–120°F Operating -70°–100°F Storage	X				
Special Handling	None	X				
Interfaces	DM/PDP/ZCP/STATE			X		

A.2.4 Zero Channel Processor

The Zero Channel Processor and its associated memory are used to provide for detection of crossing, or zero-Doppler, targets. Preliminary specifications are given in Table A-VII. During Phase II the Zero Channel Processor will be designed, developed and tested. In order to minimize cost of memory, the zero channel capability will be provided for only a segment of the radar volume. The verification worksheet of Table A-VIII describes the validation procedures to be used for the Zero Channel Processor.

A.2.5 Postdetection Processor

The Postdetection Processor performs the ***greatest of*** channel selection and post detection integration operations. Specification for these units are provided in Table A-IX. During Phase II, we will design, develop and test the Postdetection Processor with validation procedures conducted as indicated on the verification worksheet of Table A-X.

A.2.6 STATE Processor Unit

The STATE Processor Unit is the controller for the SPUR. It monitors the BITE signals of the other processor units, directs interunit tests, reconfigures the processor when faults are indicated, and continually evaluates and reports the processor status. The STATE Processor Unit is a critical item in the SPUR, especially in terms of processor reliability and maintainability. We will design, develop, and test the STATE Processor Unit during the Phase II program.

Specifications for the STATE Processor Unit are listed in Table A-XI and the verification worksheet is given in Table A-XII.

TABLE A-VII. ZERO CHANNEL PROCESSOR SPECIFICATION

Speed	3.6 μsec/cell
Dynamic Range	6-bits in map
Clutter Map Memory Size	64K words/16K spare bank
Power Consumption	40 watts for RPM-II
Program Instructions	280
BITE	Test Cases
Reliability	9.11 f/10^6 hours (½ interface board + RPM-II)
Reconfiguration	4/5 Memory Modules required 1/2 RPM-II's required
Modularity	1 Interface board, 2 RPMs
Environmental	0°–120°F Operating; -70°–100°F Storage
Interfaces	Post Filtering Processor/Post Detection Processor/ STATE Processor

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TABLE A-VIII. VERIFICATION WORKSHEET FOR ZERO CHANNEL PROCESSOR (ZCP)

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	3.6 μsec/cell		X			
Dynamic Range	6 Bits	X				
Memory Size	64K words	X			X	
Power	RPM–II 40W		X			
Losses	–	X			X	
Program Instructions	280 Instructions			X		
Stability/Calibration	Test Case			X		
Reliability	9.11 f/10^6 hr (RPM-II + ½ Interface Bd)	X				
Reconfiguration	4/5 Memory Modules ½ RPM-II			X		
Modularity	1 interface board 2 RPM–IIs		X			
Environmental	0°–120°F Operating -70°–100°F Storage	X				
Special Handling		X				
Interfaces	PFP/STATE/PDP			X		

TABLE A-IX. POSTDETECTION PROCESSOR SPECIFICATIONS

Speed	550 words/1.95 msec
Dynamic Range	6-bits Input/1-bit Output
Memory Size	4K bits
Power	35 Watts (Interface Board Only)
Losses	1.4 dB
Program Instructions	155 Instructions
BITE	Test Case
Reliability	7.9 f/10^6 hours (½ Interface Board Only)
Reconfiguration	1 of 2 RPMs
Modularity	1 Interface board/2 RPM boards
Environmental	0°–120°F Operating; -70°–100°F Storage
Interfaces	Postfiltering Processor/Zero Channel Processor/STATE Processor

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TABLE A-X. VERIFICATION WORKSHEET FOR POSTDETECTION PROCESSOR (PDP)

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	550 words/1.95 msec		X			Input Data Rate
Dynamic Range	6-Bits Input 1-Bit Output		X X			Multinomial Integrator
Memory Size	4K Bits	X			X	
Power	35 Watts Interface Board		X			
Losses	1.4 dB	X			X	
Program Instructions	155 Instructions			X		
BITE/Calibration	Test Case					
Reliability	7.9 f/10^6 hr ½ Interface Board	X				
Reconfiguration	1 of 2 RPMs			X		
Modularity	1 Interface Board/2 RPM Boards		X			
Environmental	0°–120°F Operating -70°–100°F Storage	X				
Special Handling	None	X				
Interfaces	PFP/STATE/ZCP			X		

TABLE A-XI. STATE PROCESSOR UNIT SPECIFICATIONS

Speed	5 MHz
Word Size	16 bits
Memory Size	16K Words Program Memory 2K Words Data Memory
Power	22 watts
Program Instructions	(TBD) Instructions
BITE	Internal Test Cases Processor Test Cases
Reliability	4.0 f/10^6 hours
Reconfiguration	Triple Modular Redundancy
Modularity	1 Board
Environmental	0°–120°F Operating; -70°–100°F Storage
Interfaces	A/D Converter/Doppler Modules/Postfiltering Processor/ Zero Channel Processor/Post Detection Processor

9524-89

TABLE A-XII. VERIFICATION WORKSHEET FOR STATE PROCESSOR

Characteristic	Requirement	Verification Approach: Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	Remarks
Speed	5 MHz	X	X			
Dynamic Range	Word Size 16 Bits		X			
Memory Size	16K Words Program Mem/ 2K Data Mem			X		
Power	22 Watts		X			
Losses	N/A					
Program Instructions	(TBD) Instructions			X		
BITE/Calibration	Test Cases					Internal Checks Processor Check
Reliability	4.0 f/10^6 hr	X				
Reconfiguration	Internal Redundancy		X	X	X	TMR
Modularity	1 Board		X			
Environmental	0°–120°F Operating -70°–100°F Storage	X				
Special Handling	None	X				
Interfaces	A/D/DM/PFP/ZCP/PDP			X		

9524-89

Appendix B

TEST BED RADAR

During the Phase II validation effort the SPUR hardware will be incorporated into the solid-state L-band test bed radar installed in our plant at Van Nuys, California. In this appendix we describe the radar equipment, operating environment and the modifications that will be made to accommodate the SPUR hardware.

B.1 EQUIPMENT DESCRIPTION

Figure B-1 is a block diagram of the current test bed system. It is configured with an instrumented range of 200 nmi and provides 360-degree azimuth coverage with a frame time of 12 seconds. While frequency restrictions limit our operation at the Van Nuys plant to the single frequency of 1275 MHz, the radar has been designed for operation over the entire L-band region – from 1215 to 1400 MHz.

B.1.1 Antenna

The antenna is an edge slotted waveguide planar array as shown in Figure B-2. It consists of 12 horizontal linear arrays stacked vertically and end-fed from a dispersive line feed. Major performance characteristics of the antenna are listed in Table B-I.

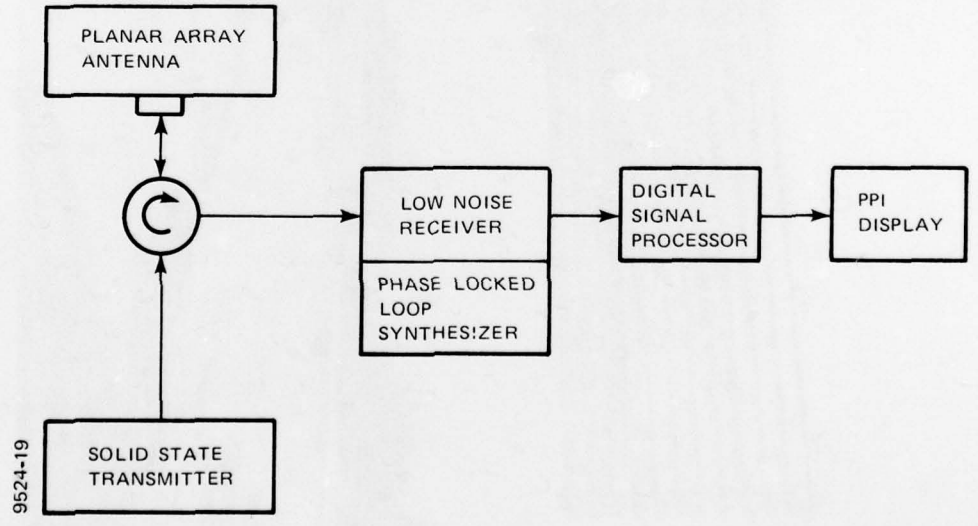


Figure B-1. Block Diagram of the Solid State L-Band Test Bed Radar *which is available at ITTG for system test of the SPUR hardware*

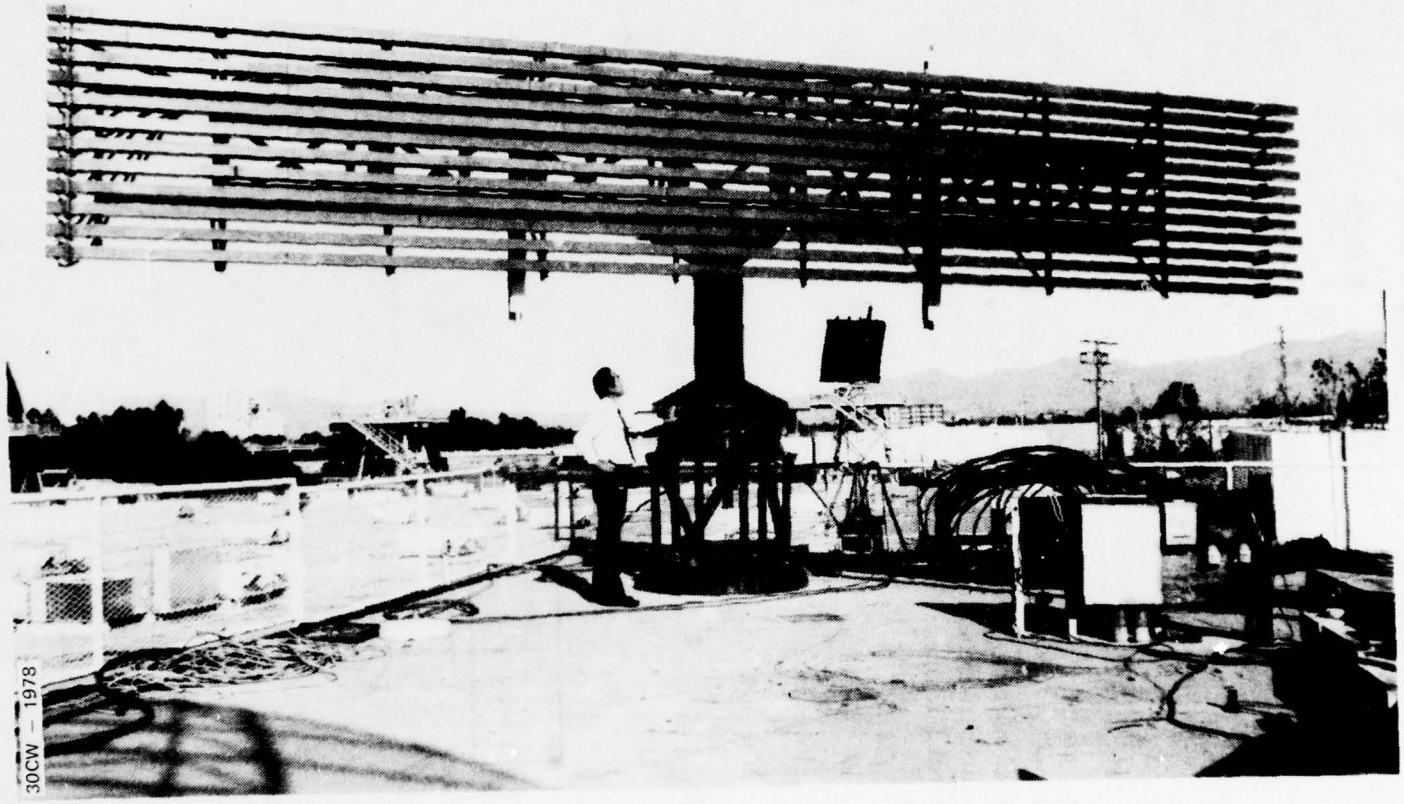


Figure B-2. The Test Bed Radar Uses an Edge Slotted Waveguide Planar Array Antenna

TABLE B-I. PRINCIPLE ANTENNA CHARACTERISTICS (at 1275 MHz)

Gain	27.45 dBI
Beamwidth	
Azimuth	1.8°
Elevation	9° at -3 dB
	21° at -10 dB
Sidelobes	
Azimuth	-39 dB peak
Elevation	-13.4 dB peak
Aperture	
Horizontal	401.8 in.
Vertical	75 in.

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B.1.2 Transmitter

The test bed transmitter is a centralized solid state master oscillator power amplifier. Figure B-3 is a photograph of the transmitter. It consists of a preamp driver and three stages of amplification with a final output power of 16.6 kW peak power. It also provides frequency and waveform agility and has excellent stability characteristics for MTI processing. The transmitter exhibits a very high degree of fault tolerance and permits on-line repair via module replacement. Table B-II lists some of the principle characteristics of the transmitter.

B.1.3 Receiver/Synthesizer

The test bed receiver consists of a wideband low-noise GaAs FET front-end in a double conversion superheterodyne configuration. The synthesizer employs a crystal controlled, phased locked loop for generating the first LO, second LO, COHO, system clock, and binary phase code modulated transmitter RF drive. The dynamic range and stability characteristics of the receiver/synthesizer are compatible with high MTI performance requirements. A photograph of the receiver/synthesizer is provided in Figure B-4, and Table B-III lists some of the major characteristics.

B.1.4 Signal Processor

The digital signal processor (Figure B-5), performs the video processing, display interface and program control. The video processor consists of In-Phase (I) and Quadrature (Q) channels with 10-bit analog-to-digital conversion, 4/8-point FFT clutter filtering, pre-compression limiting CFAR, 31-bit pulse compression and I- and Q-channel combination. The FFT computer program is stored in controller boards and executed in Array Processing Module boards using Random Access Memory boards for working data storage. The display interface provides video for PPI display. The program control uses the system clock signal from the receiver to control scan program and system timing functions. Table B-IV provides some of the major characteristics of the digital signal processor.

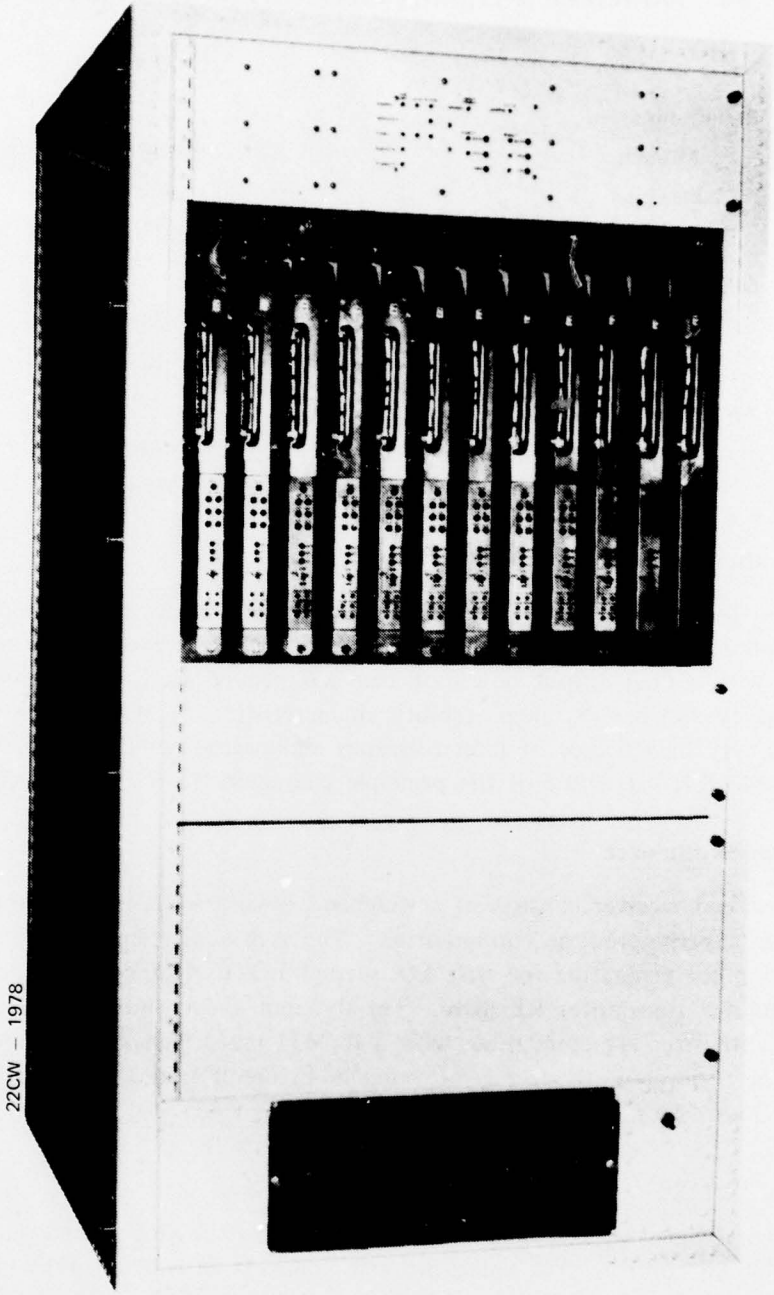


Figure B-3. RF Power is Obtained with a Centralized Fault Tolerant Solid-State Transmitter

TABLE B-II. TEST BED TRANSMITTER CHARACTERISTICS

Architecture	Centralized, Fault Tolerant with Solid State Modules
Configuration	
Preamp Driver	Commercial
Preamplifier	1/3 Module
Driver	2 Modules
Final	20 Modules
Power	
Peak	16.6 kW
Average	1 kW at 6% duty
Cooling	Air
BITE	Fault Detections/Isolation to Module
Maintainability	On-line Module Replacement

9524-23

TABLE B-III. RECEIVER/SYNTHESIZER CHARACTERISTICS

Type	
Receiver	Dual Conversion Superheterodyne
Synthesizer	Crystal Controlled Phase Locked Loop
GaAs FET Amp Noise Figure	1.3 dB
T/R Limiter STC	36. dB
Second IF Bandwidth	1.8 MHz
Image Rejection	60 dB
Dynamic Range	80 dB linear
Video Channels	I&Q
Transmitter Drive Power	0.1W peak

9524-25

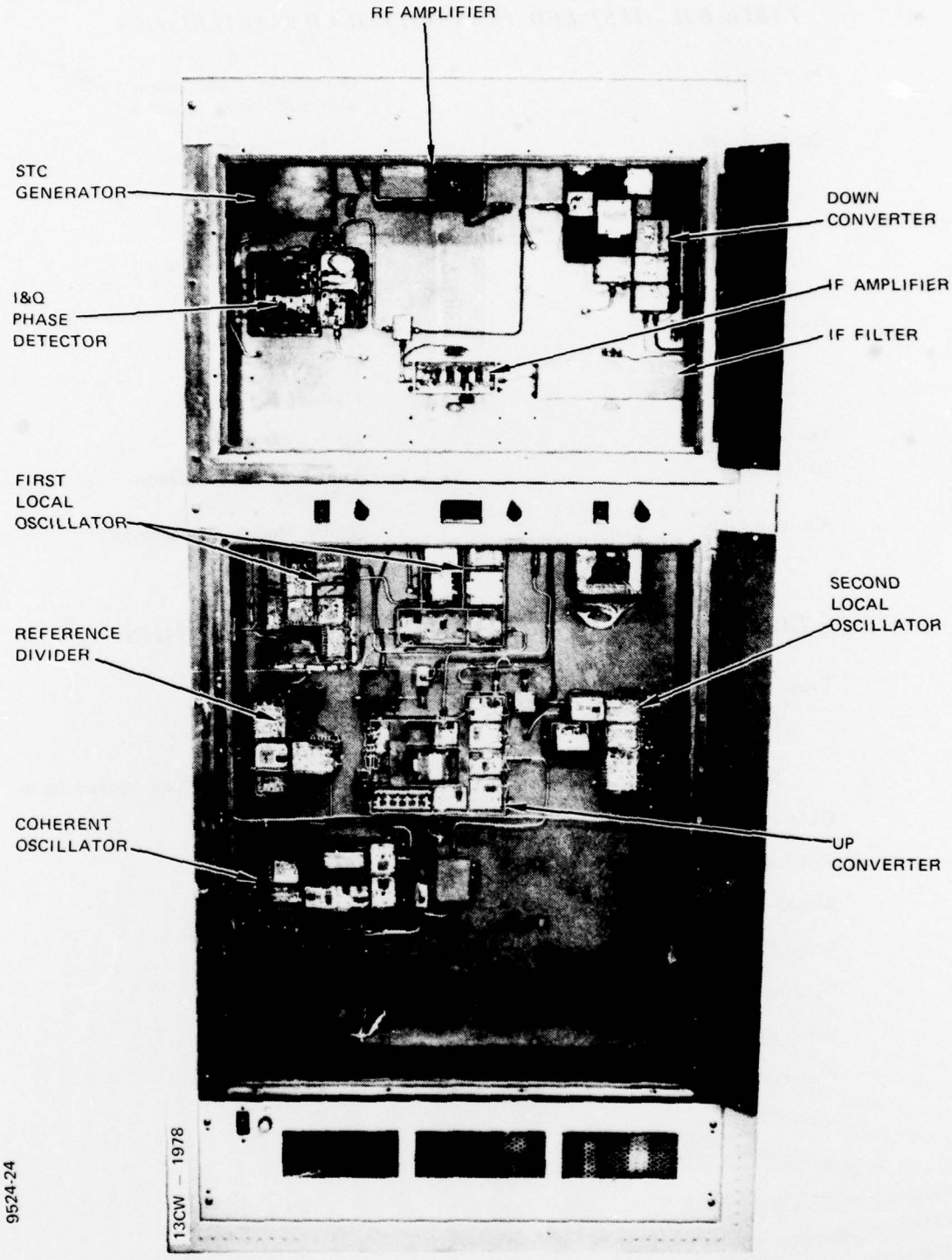


Figure B-4. The Test Bed incorporates a Fully Coherent Dual Conversion Superheterodyne Receiver and Phase Locked Loop Synthesizer

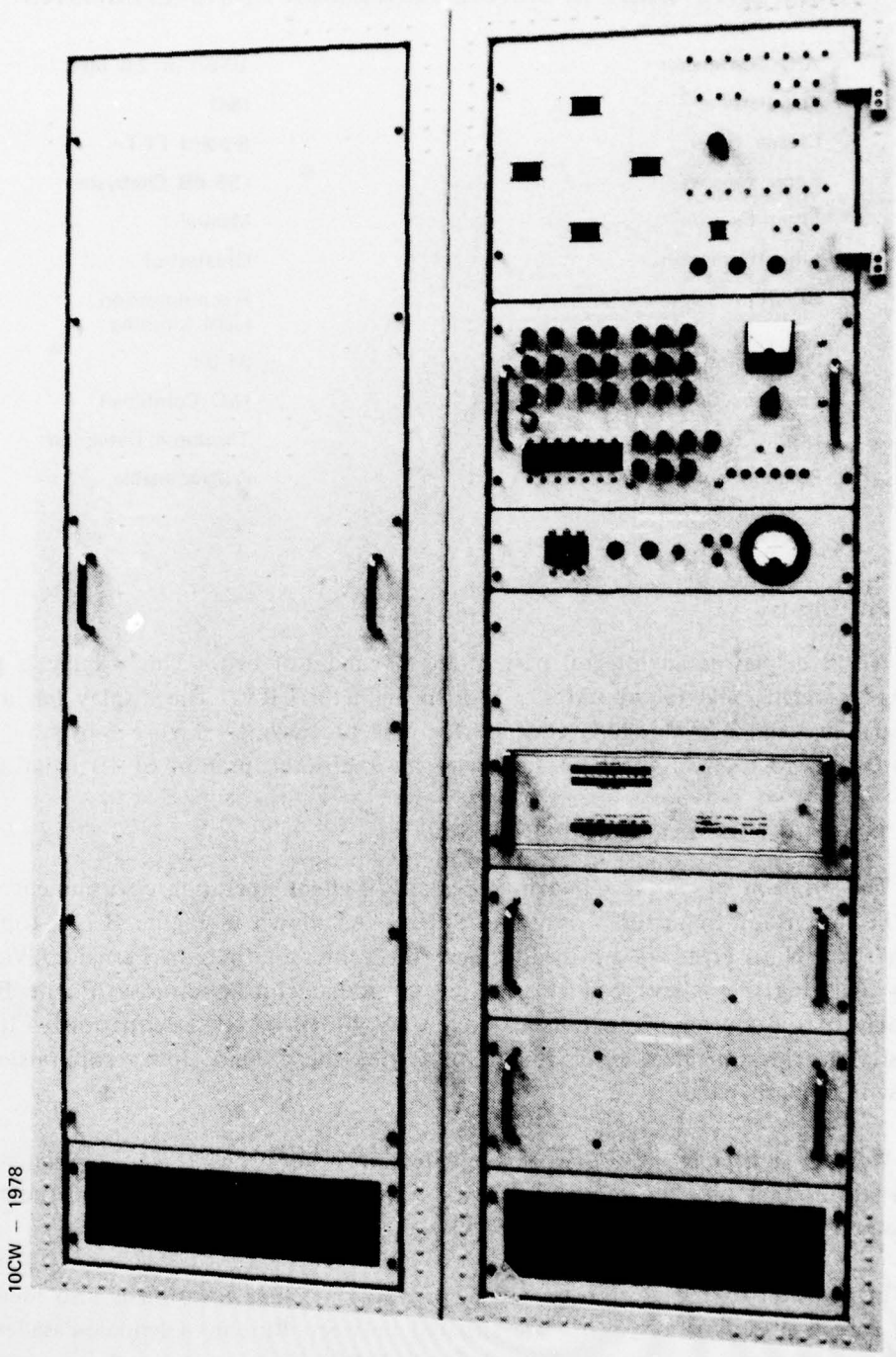


Figure B-5. Test Bed Digital Signal Processor *performs clutter processing and pulse compression*

TABLE B-IV. DIGITAL SIGNAL PROCESSOR CHARACTERISTICS

A/D Conversion	10-Bit at 2.6 MHz
Channels	I&Q
Clutter Filter	8-point FFT
Filter Weights	-55 dB Chebyshev
Filter Excision	Manual
Filter Detection	Greatest-of
CFAR	Precompression Hard Limiting
Pulse Compression	31-Bit
Envelope Detection	I&Q Combined
Display Video	Threshold Detection
Program Control	Programmable

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B.1.5 PPI Display

A PPI display is an integral part of the L-band test bed. This display is produced by Sanders Associates and incorporates a 24-inch diameter CRT. The display has a full graphic capability and provides high contrast for ease of viewing. Figure B-6 is a representative photograph of the CRT face with an exposure duration of 10 radar scans.

B.2 TEST BED RADAR ENVIRONMENT

The location of our test bed provides an excellent operating environment for testing some of the important characteristics of the SPUR. As shown in Figure B-7, a topographical map of the Van Nuys area, we are located near the center of the San Fernando Valley. The mountains that ring the valley produce very severe ground clutter returns. Figure B-8 presents a PPI display of the clutter of an L-band radar with 40 dB of RF attenuation. Clutter of this intensity provides an ideal environment for testing the ground clutter suppression techniques of modern radars.

Weather clutter is, of course, less predictable. During winter and spring we have occasional storms that provide significant weather clutter returns. If the opportunity arises, we will demonstrate the SPUR performance in the presence of such clutter.

In addition to the clutter environment, our Van Nuys location is also ideal in terms of aircraft targets-of-opportunity. We are situated between Burbank-Glendale-Pasadena Airport and Van Nuys Airport – one of the busiest General Aviation airports in the country. Moreover, we are less than 20 miles from Los Angeles International Airport. As a result we have a great deal of aircraft traffic with a wide assortment of flight trajectories.

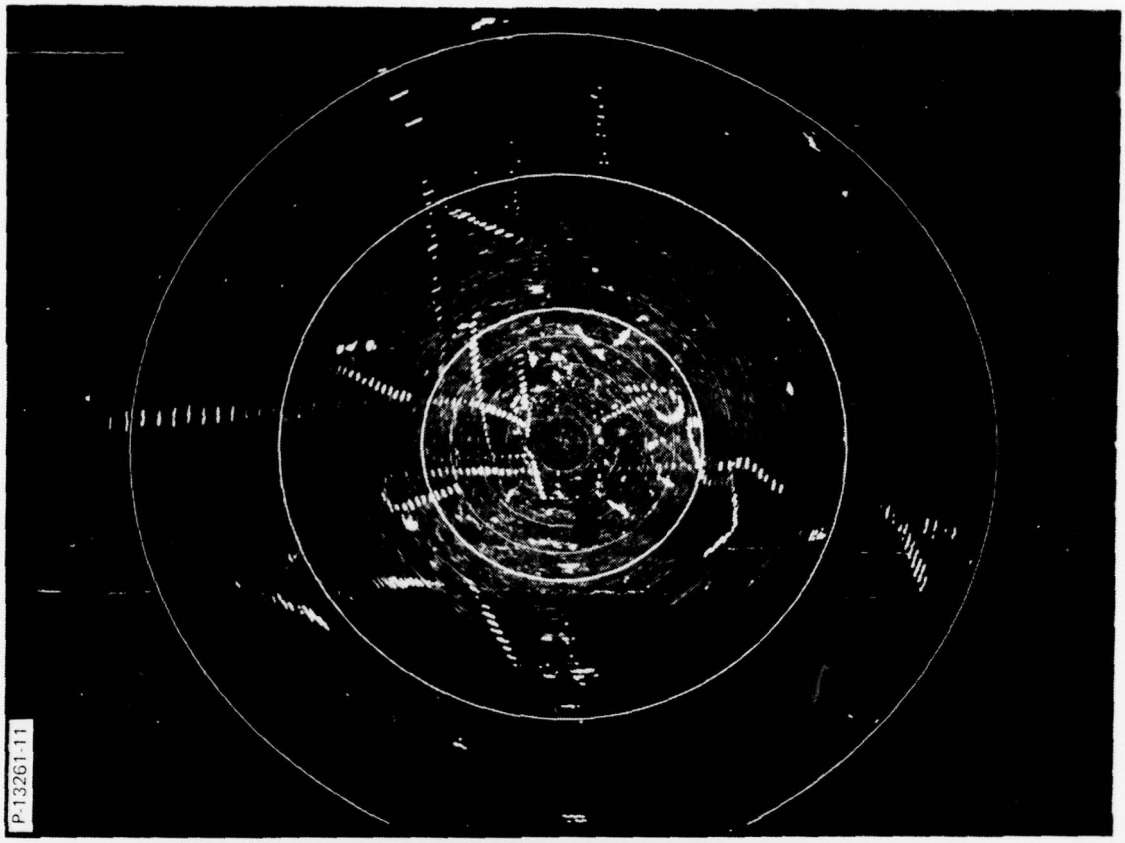


Figure B-6. ***Representative Photograph of PPI Display*** *demonstrates the quality of the PPI presentation*

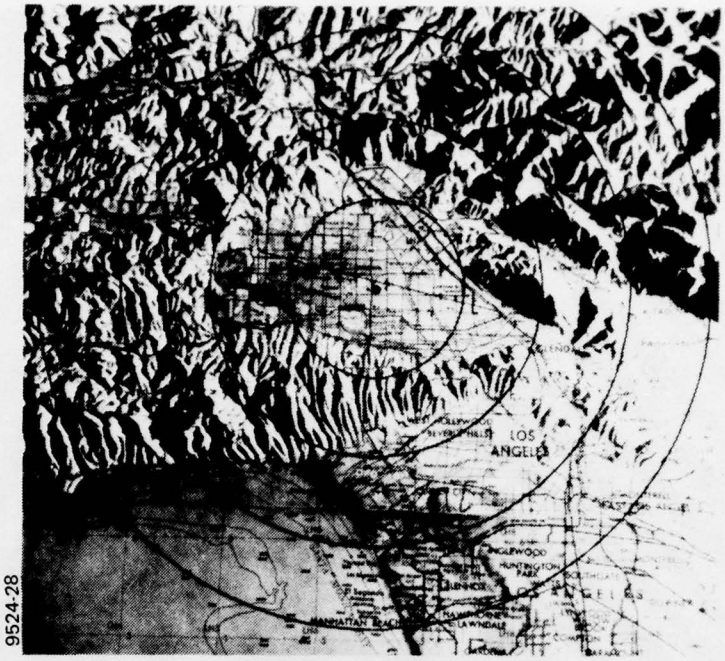


Figure B-7. Topographical Map of the Van Nuys Area *shows ITTG location in the middle of the San Fernando valley*

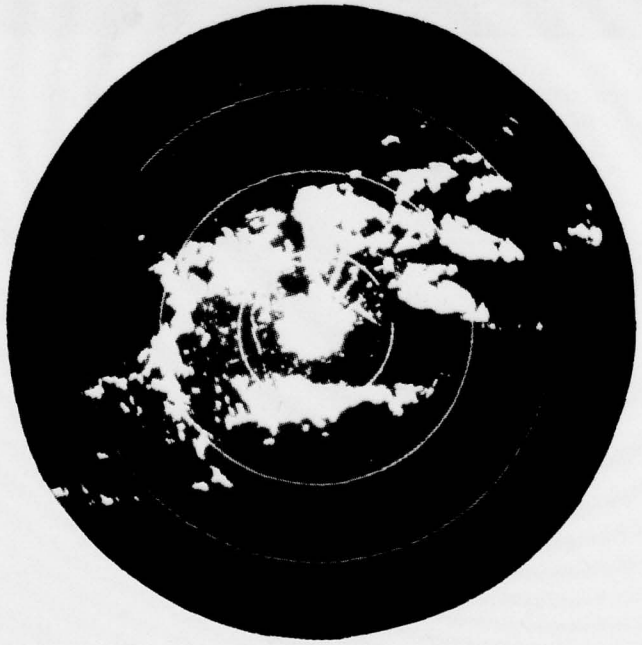


Figure B-8. L-Band Radar Returns Measured with 40 dB RF Attenuation *demonstrates severe clutter environment*

B.3 TEST BED MODIFICATIONS REQUIRED FOR SPUR VALIDATION

The major modification required for incorporating SPUR hardware into the radar test bed involves replacing the existing signal processor with the SPUR. We currently plan to operate the SPUR in parallel with the test bed processor so that some of the existing processor equipment, such as the display driver, can be used with minimum changes.

The test bed antenna beamwidth and rotation rate are essentially fixed and cannot be substantially modified for the SPUR activity. Thus, the resulting azimuth resolution and scan modulation will not necessarily be the same as that of the, as yet undefined, UAR. However, analysis will be used to account for the differences in performance that can be expected from variations in these parameters. Pulse repetition frequencies will be selected that provide the proper number of pulses per beamwidth needed for coherent and noncoherent processing of the SPUR.

The transmitter pulsewidth will be increased from the present 24.4 μsec to approximately 40 μsec. A slight reduction in peak power may also be incorporated; however this will be determined at a later date.

Modifications to the existing receiver will be minimal. Reduction of the final IF bandwidth from 1.8 MHz to about 0.6 MHz is the only anticipated change.

Modification of the system timing and triggers will be implemented in the synthesizer. If possible, we plan to use the existing basic system clock as well as the current COHO and LOs.

The test bed radar has been tested and documented in considerable detail. Moreover, the modifications described here, with the exception of the SPUR itself, are considered relatively minor. Thus, we are confident that the system level tests will be useful in validating performance characteristics of the SPUR itself, without being overly concerned with potential anomalies due to the other radar equipment.