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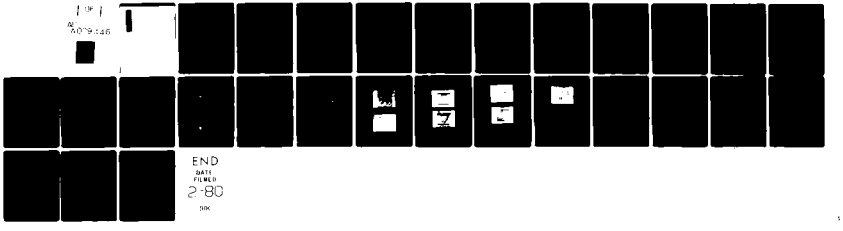

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The objectives of this research program are: (i) to develop planar GaAs transferred-electron logic devices (TELDs), and (ii) to fabricate and evaluate a monolithic full ADDER.

The TELD-FET combination device provides substantial improvements in operating characteristics over TELD with resistive loads. It has better trigger-sensitivity and stability. The power dissipation

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can also be reduced to 0.16 to 0.2 of that for TELDs with resistive load. The capacitive output of TELD-FET makes direct interconnections possible without level shifting. Majority logic can be implemented with TELDs which reduces the component count substantially. The full ADDER circuit is a good example of this.

In the previous phase of this program a design of a full ADDER with GaAs TELD-FET devices was discussed. Uniformly doped material and 1.0-μm gate length devices have been used in the above design. The design is now extended to (i) FET and TELD sections with selective doping, and (ii) 0.5-μm gate length devices. Both the selective doping as well as smaller gate length substantially improve the device performance. The process schedule developed in the previous phase of the program for a 1.0-μm-long device has been debugged and several monolithic ADDER circuits were fabricated. Discrete test FET and TELD dc characteristics were evaluated on the curve tracer. FET characteristics were in close agreement with the design goals, but TELDs did not show any substantial current drop. A maximum current drop measured was 10 to 15%, and the design goals are 25 to 35%.

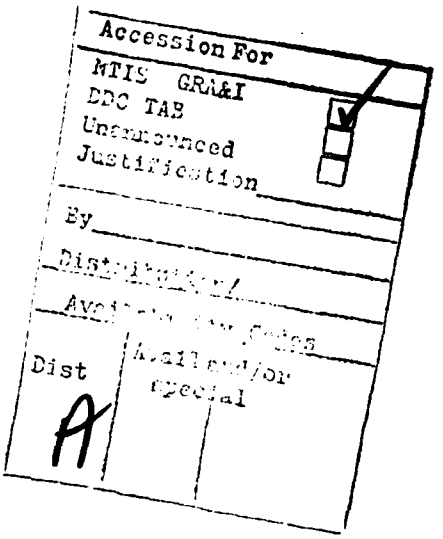
Technology was developed for the fabrication of small-scale GaAs integrated circuits. Further improvements are required in the growth of GaAs epitaxial layers which will result in improved device characteristics. The 25 to 30% current drop devices are required for the successful operation of TELD integrated digital circuits.

PREFACE

This Final Report describes the work done in the Microwave Technology Center of RCA Laboratories, Princeton, NJ, under Contract No. N00014-75-C-0100 during the period of 10 October 1974 to 14 May 1979. F. Sterzer is the Center's Director, S. Y. Narayan is the Project Supervisor, and L. C. Upadhyayula the Project Scientist. Others who participated in the program are R. E. Smith, S. T. Jolly, J. P. Paczkowski, D. R. Capewell, E. E. Beck, and J. E. Brown. The draft of this report was submitted in May, 1979.

The research done during 10 July 1974 to 14 March 1978 was reported earlier through Annual Reports.

This research was sponsored by the Office of Naval Research, and M. N. Yoder was the Contract Monitor.



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SECTION I

INTRODUCTION

The objectives of this research program are: (i) to develop planar GaAs transferred-electron logic devices (TELDs), and (ii) to fabricate and evaluate a monolithic full ADDER.

In the previous phase of this program a design of a full ADDER with GaAs TELD-FET devices was discussed. Uniformly doped material and 1.0-μm gate length devices have been used in the above design. The design is now extended to (i) FET and TELD sections with selective doping, and (ii) 0.5-μm gate length devices. Both the selective doping as well as smaller gate length substantially improve the device performance. The process schedule developed in the previous phase of the program for a 1.0-μm-long device has been debugged and several monolithic ADDER circuits were fabricated. Discrete test FET and TELD dc characteristics were evaluated on the curve tracer. FET characteristics were in close agreement with the design goals, but TELDs did not show any substantial current drop. A maximum current drop measured was 10 to 15%, and the design goals are 25 to 35%.

The effort in the design, fabrication, and evaluation of the ADDER circuit is described in the following sections.

SECTION II

DEVICE DESIGN

A. INTRODUCTION

The advantages of integral TELD-FET devices for logic applications were pointed out in our previous Annual Report [1]. Design of the 1.0-μm gate length devices with uniformly doped materials was also discussed. The improvement of the device characteristics by (i) reducing the gate length, and (ii) selective doping TELD and FET sections is discussed in this section. The improved devices can be incorporated in the fabricaton of the monolithic ADDER for further improving its performance.

B. TELD OUTPUT SECTION

A detailed discussion on TELD design was given in the Annual Report [1]. In the TELD-FET combination, the TELD section is used to provide the output. A capacitive pickoff is used to eliminate the dc level shifting and stability problems. The output of a TELD with capacitive electrode is given by

$$\Delta V_o = \alpha K V_{th} \tag{1}$$

where α = coupling coefficient,

K = percentage current drop,

and V_{th} = TELD threshold voltage.

It is obvious from Eq. (1) that ΔV_o is large when α, K and V_{th} are large.

As discussed in our annual report, $V_{th} = \ell \cdot E_{th}$ and can not be made large indefinitely. The TELD length ℓ is clearly fixed by the maximum frequency of operation and also by power dissipation considerations. We have chosen the device transit length ℓ to be 20 μm. V_{th} is therefore about 8 V. The only parameters which can be used to increase ΔV_o are thus α and K.

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1. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Transferred-Electron Logic Device (TELD) Development," ONR Contract No. N00014-75-C-0100, Annual Report, September 1978.

1. Effect of Doping On Current Drop

The fractional current drop K depends on the electron peak-and-valley velocity in the material. For GaAs, the electron velocity can be calculated as a function of the electric field using the relation

$$\upsilon(E) = \frac{\mu E + v_s \left|\frac{E}{E_c}\right|^4}{1 + \left|\frac{E}{E_c}\right|^4} \qquad (2)$$

Here μ is the low field mobility, E_c is the critical field ($\sim$ 3.9 kV/cm for GaAs) and v_s is the saturation velocity ($\sim$ 0.96×10^7 cm/s). Figure 1 shows the v-E curves for GaAs using μ as a parameter. Note that the peak velocity (v_p) depends strongly on μ and is higher for material with higher μ. It is well known that high μ occurs with lower doping. Also note that for electric fields greater than 7 to 8 kV/cm, the valley velocity does not show a strong dependence on μ. For the values of typical domain fields, the valley velocity approaches v_s, the saturated velocity. The fractional current drop K is therefore higher for lower doped material.

2. Effect of Doping on the Coupling Constant

The coupling constant α is defined as

$$\alpha = \frac{C_d}{C_d + ZC_g} \qquad (3)$$

where C_d = domain capacitance,
C_g = input gate capacitance of the following device,
and Z = fanout factor.

The domain capacitance C_d is given by

$$C_d = \sqrt{\frac{6\varepsilon e/\mu'/en}{v_p \ell}}\ Wd \qquad (4)$$

where μ' = negative differential mobility
ℓ = transit length,
W = device width,
d = channel thickness,
v_p = peak velocity of electrons,
ε = dielectric constant,
and e = electronic charge.

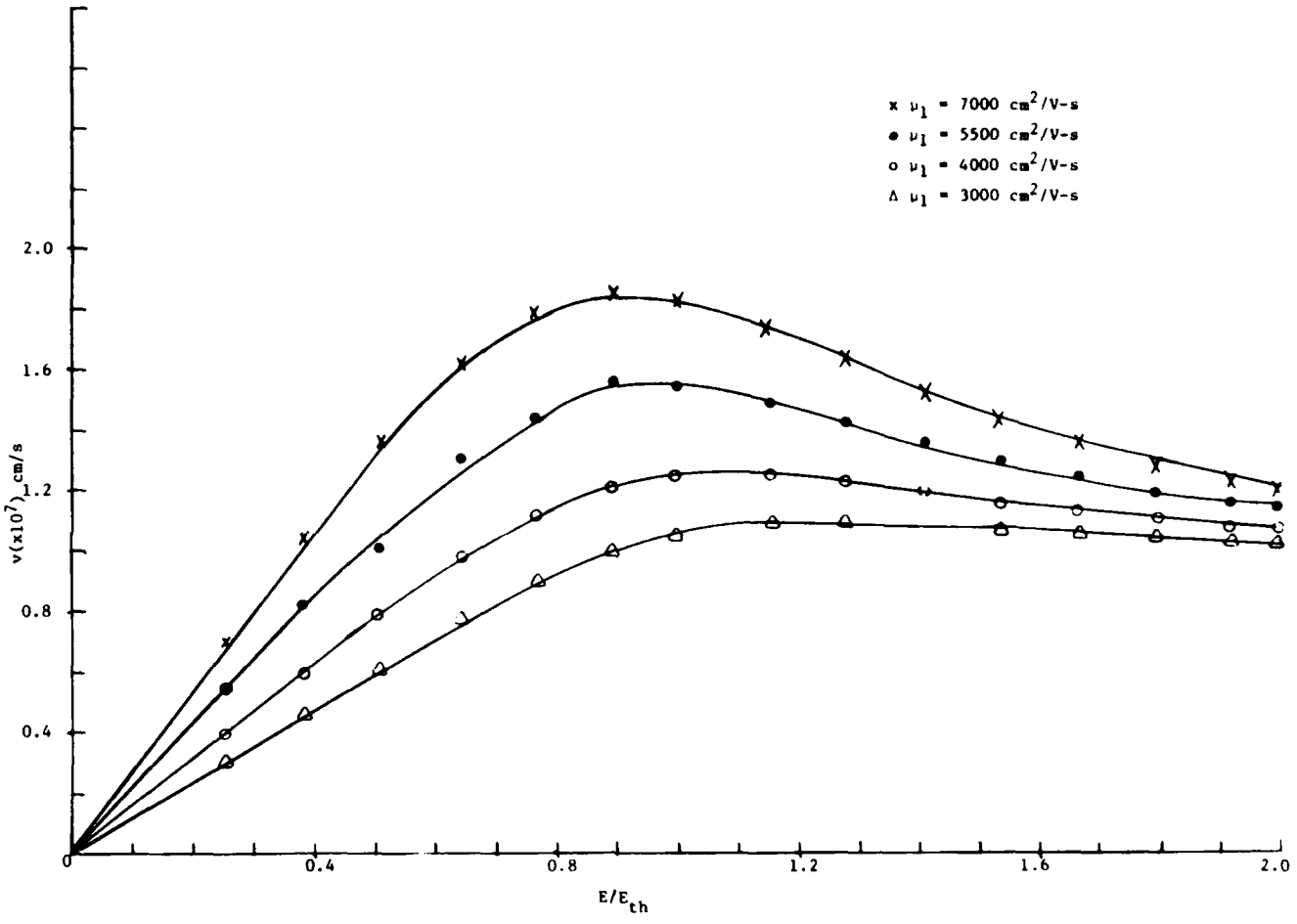

Figure 1. Velocity-field characteristics for GaAs with low field mobility as a parameter.

When the nd product is maintained constant, the domain capacitance varies as $\sqrt{d}$. For lower doped material the channel thickness d is higher (for nd = constant) and so is the domain capacitance. Also, for the same TELD threshold current ($I_{th} = ne\ v_p\ Wd$), W is larger for lower doped material, which results in an increase in the domain capacitance. Therefore, a lower doped material is preferable for the transferred-electron logic device section. For nd = $2x10^{12}$ cm^{-2}, TELD parameters have been calculated for two different doping densities and summarized in Table 1. A device width of 15 μm and device length for 20 μm were assumed.

TABLE 1. TELD PARAMETERS CALCULATED AS A FUNCTION OF DOPING

n (cm^{-3})	d (μm)	V_p cm/s	K	C_d (fF)
$2x10^{16}$	1.0	$1.6x10^7$	0.35	5.18
$8x10^{15}$	2.5	$1.85x10^7$	0.46	7.62

from this table it is clear that K and C_d are higher for the device with lower doping.

C. FET SECTION DESIGN

From Figs. 4 and 6 of R. B. Fair [2] one can conclude that the drain saturation current (I_{DSS}) and transconductance (g_m) increase with doping density for any given pinchoff voltage. Therefore, a heavily doped channel ($n \sim 10^{17}$ cm^{-3}) is preferable for the FET section.

When the material parameters (n, V_p) are fixed by I_{DS} and g_m considerations, the only parameter available for minimizing the gate capacitance is ℓ_g. When ℓ_g is reduced, C_g decreases in the same proportion. Optical photolithography limits ℓ_g to 1.5 to 2.0 μm, self-aligned gate technology limits it to 0.7 to 1.0 μm and side etching techniques limit it to 0.5 to 0.6 μm.

The pertinent parameters of the FET input section calculated from Ref. [2] for channel dopings of $1x10^{16}cm^{-3}$ and $8x10^{16}cm^{-3}$ are shown in Table 2. In both cases the pinchoff voltage has been chosen to be 5 V, the gate width is 90 μm, and the drain current required is about 4 to 7 mA.

2. R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETs," IEEE Trans. Electron Devices ED-21(6), 357 (1974).

TABLE 2. FET PARAMETERS CALCULATED AS A FUNCTION OF DOPING

Doping Density (cm^{-3})	Pinchoff Voltage (V)	Gate Bias (V)	Drain Current (mA)	Trans-conductance (mS)	Gate Capa-citance (fF)
$1x10^{16}$	5	-1.5	4.6	1.9	18
$8x10^{16}$	5	-2.65	7.0	2.88	40

D. TELD-FET INTEGRAL DEVICE

We will now consider the TELD-FET combination device and its performance. Uniformly doped, as well as selectively doped channels for the two devices will be considered.

The parameters of interest are the output voltage ΔV_o and the corresponding current change $\Delta I = g_m \Delta V_o$. For our full ADDER implementation we require a fanout capability of at least 2-2/3. We will therefore assume this value for Z and calculate ΔV_o and ΔI for the TELD-FET with gate lengths of 1.0 μm and 0.5 μm for the compromise doping of $1\text{-}2x10^{16} cm^{-3}$ and the selective doping (FET section $8x10^{16} cm^{-3}$; TELD section $8x10^{15} cm^{-3}$) cases. The results are summarized in Tables 3 and 4.

Note that the use of selective doping increases ΔV_o by about 12%, and ΔI by about 60%. The second conclusion is that the use of 0.5-μm gate length results in a significant improvement in performance. Based on this theory, our ultimate technology development goals are to (i) use selective doping for the FET and TELD regions, and (ii) reduce gate length to submicrometer values.

E. MSI TEST VEHICLE

A full ADDER has been chosen as a test vehicle for TELD MSI technology development. In a full ADDER, the sum (S_n) and carry (C_n) for the n^{th} bit are generated from the data inputs X_n and Y_n and the carry from the previous bit C_{n-1}. The expressions used in generating S_n and C_n are:

$$S_n = (X_n \oplus Y_n) \oplus C_{n-1} \tag{5}$$

$$C_n = X_n Y_n + X_n C_{n-1} + Y_n C_{n-1} \tag{6}$$

A full ADDER using TELD-FET devices is shown in Fig. 2. The sum output is generated in a two-stage, two-input exclusive-OR circuit and the carry

TABLE 3. TELD-FET DEVICE (UNIFORMLY DOPED MATERIAL)

FET								TELD				
Doping Density (cm^{-3})	V_p (V)	I_g (μm)	V_G (V)	I_{DS} (mA)	g_m mS	C_g (fF)	ΔI (mA)	d (μm)	K	Cd (fF)	α	V_o (V)
$2x10^{16}$	5	1.0	-2	7	2	23	0.8	1.0	0.35	5.18	0.145	0.4
$2x10^{16}$	5	0.5	-2	7	2	11.4	1.42	1.0	0.35	5.18	0.254	0.71
$1x10^{16}$	5	1.0	1.5	4.6	1.92	18	1.21	1.5	0.40	5.9	0.197	0.63
$1x10^{16}$	5	0.5	1.5	4.6	1.92	9	2.1	1.5	0.40	5.9	0.328	1.1

TABLE 4. TELD-FET DEVICE (SELECTIVE DOPING)

FET								TELD					
Doping (cm^{-3})	V_p (V)	Ig (μm)	V_g (V)	I_{DS} (mA)	g_m (mS)	Cg (fF)	ΔI (mA)	Doping (cm^{-3})	d (μm)	K	Cd (fF)	α	V_o (V)
$8x10^{16}$	5	1.0	-2.65	7	2.88	40	1.29	$8x10^{15}$	2.5	0.46	7.62	0.122	0.45
$8x10^{16}$	5	0.5	-2.65	7	2.88	20	2.3	$8x10^{15}$	2.5	0.46	7.62	0.218	0.80

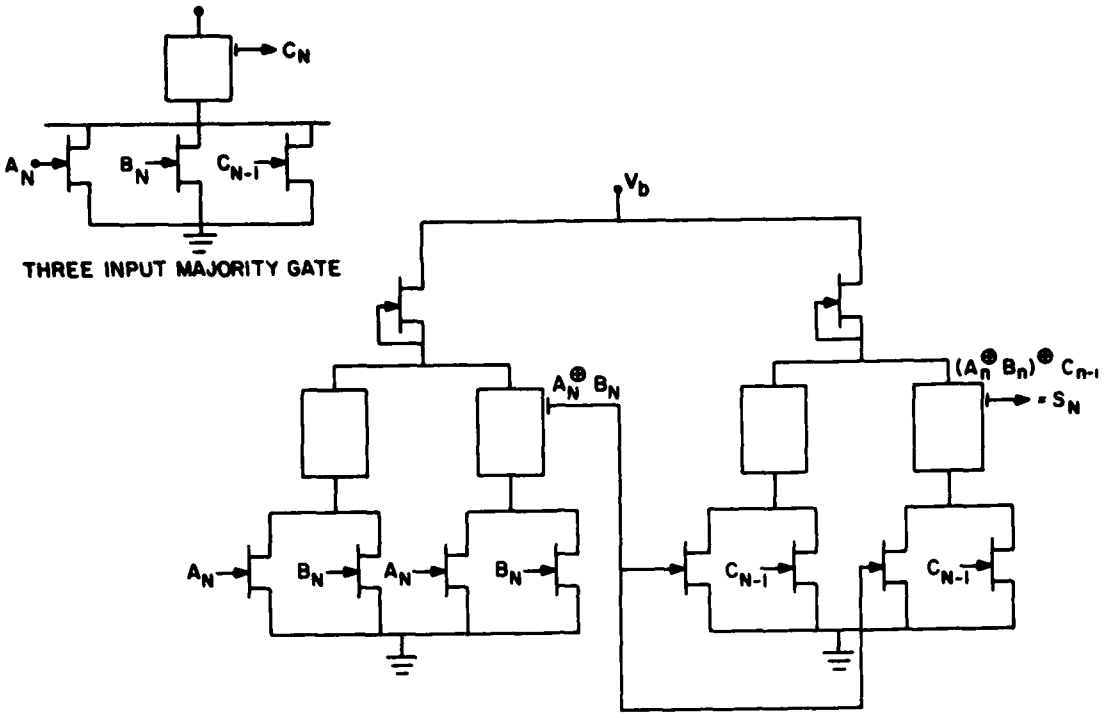

Figure 2. Schematic of the TELD-FET full ADDER.

output is generated in a two-out-of-three MAJORITY gate. Figure 3 shows the layout of the monolithic ADDER. The transit time for TELDs is about 200 ps, and therefore the circuit is expected to work at 2 to 3-gigabit rates.

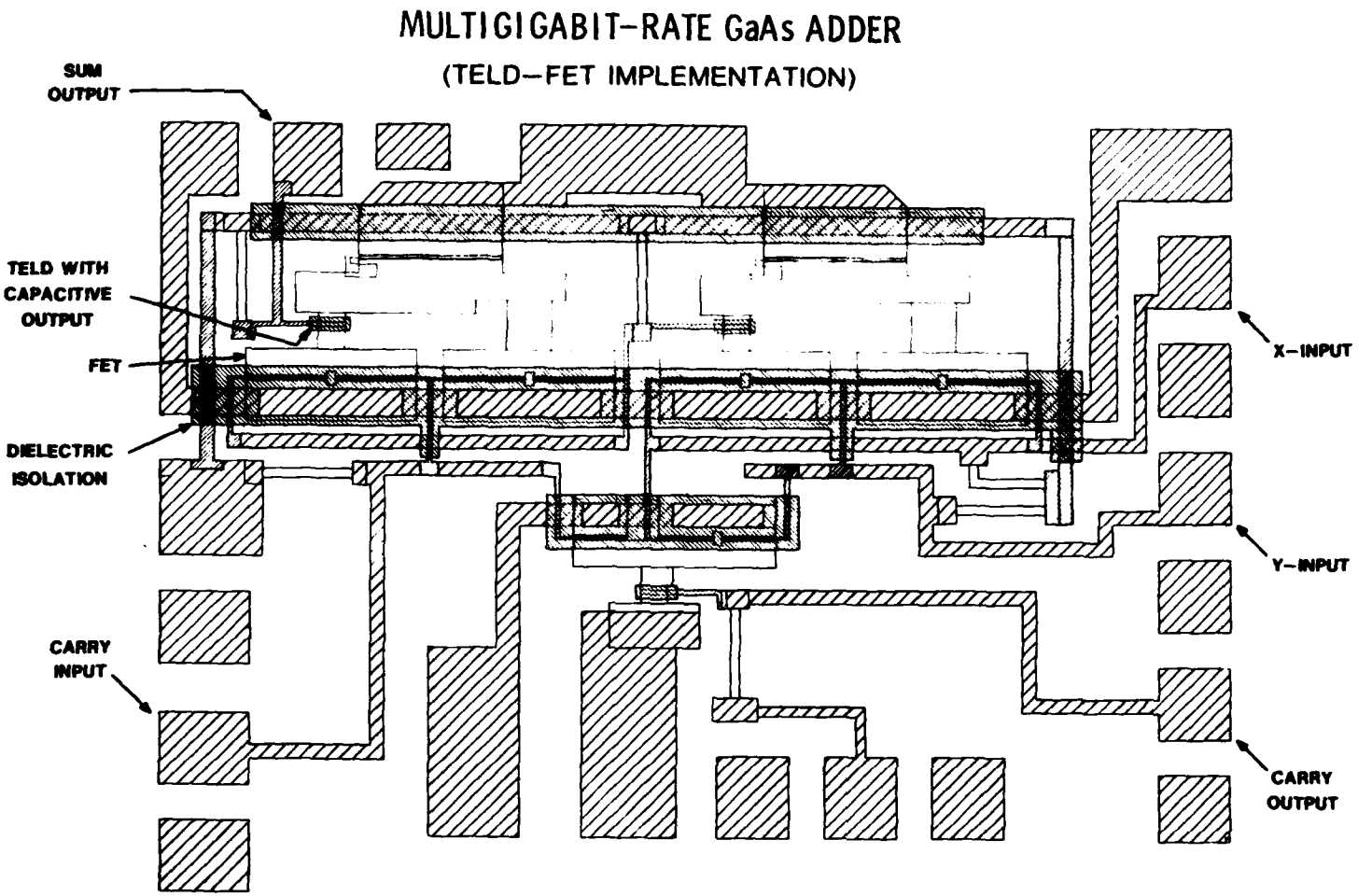

Figure 3. Layout of a multigigabit-rate GaAs ADDER (TELD-FET implementation).

SECTION III

TECHNOLOGY DEVELOPMENT

A. INTRODUCTION

The technology development started in the final quarter of last-year's program was continued. The process schedule was debugged. Several wafers were processed and the ADDER IC was completed. The dc characteristics were measured on discrete test FETs and TELDs. In most of the wafers TELDs did not show any current drop. In a few wafers TELDs showed 5 to 15% current drop which is not adequate for the successful operation of the IC.

B. PROCESS DEVELOPMENT

A process schedule has been developed for fabricating GaAs integrated circuits. Self-aligned gate technology was used for realizing micrometer-size gates and dry etching was used instead of wet chemical etching wherever possible for better geometry control. The starting wafers for our processing are n^+-n-SI GaAs epitaxial wafers grown in our laboratory by either vapor hydride or trichloride synthesis. The fabrication steps are schematically shown in Fig. 4, and summarized below.

1. Ohmic contact metallization was deposited over the n^+ face.
2. Device active regions were delineated by mesa etching. The etching was done partly with ion-beam milling for better geometry definition and partly with a preferential chemical etch for gradual sloping mesa edges for gates.
3. FET channels were opened with ion-beam etching (IBE). A chemical touch-up etch was used to undercut the source-drain regions and provide overhangs for self-registration of gates.
4. Ti/Pd/Au metallization was deposited to form FET gates and some of the interconnections.
5. TELD active regions are opened using IBE and the channel thickness is adjusted so that the TELD and FET currents are compatible.
6. SiO_2 and/or Si_3N_4 dielectric layers were deposited either by CVD or by plasma deposition.
7. Capacitive-pickoff and interconnect regions were defined.
8. Ti/Pd/Au second-level interconnections and bonding pads were formed.

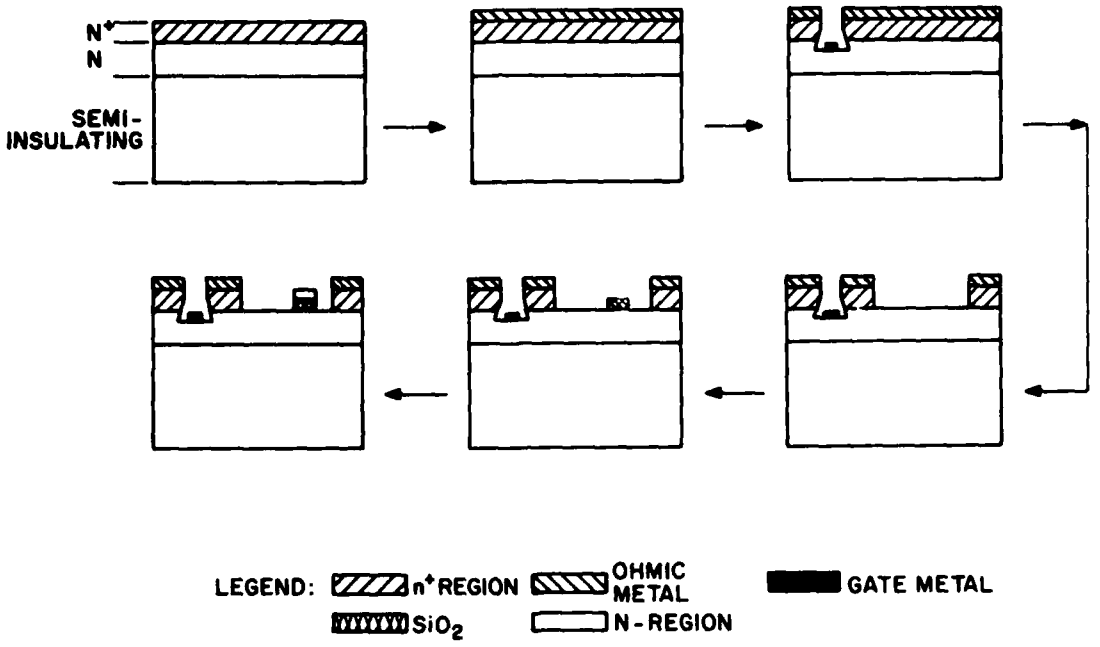

Figure 4. Process schedule for the fabrication of self-aligned gate TELD-FET devices.

C. INTEGRATED CIRCUITS

The integrated circuit consisted of test and ADDER chips. The device geometries on the test chip are identical to those on the ADDER chip. The contact pads on the test chip are made much bigger (50 μm x 50 μm instead of 10 μm x 10 μm) to facilitate testing during the process.

Figure 5 shows a photomicrograph of a test chip. Three different types of I-V characteristics observed on discrete TELDs are shown in Fig. 6. In Fig. 6(a) the device does not exhibit any current drop. As far as we can determine, the nd and nl products are greater than the critical values required. In Fig. 6(b) the device shows asymmetry in the characteristic. When the anode is biased positive, the device exhibits current saturation, and when biased in the opposite polarity it exhibits current thresholding. The TELD has a rectangular active channel, and we do not understand the origin of the asymmetry. In Fig. 6(c) the device exhibits 15% current drop. The threshold current and voltage are close to the design values. However, a current drop of 25 to 30% is required for the successful operation of the ADDER circuit.

The dc transfer characteristics of a typical FET are shown in Fig.7. The drain saturation current (I_{DSS}) is 8 to 10 mA, and the transconductance (g_m) is 2.0 to 4.0 mS. These values are in good agreement with the design goals.

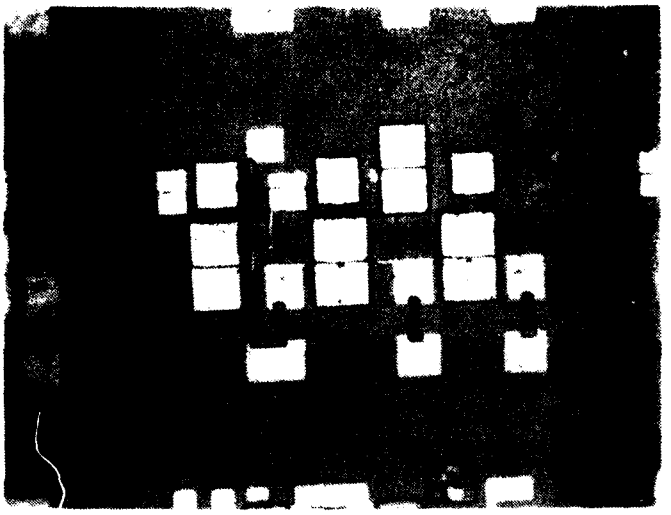

Figure 5. Photomicrograph of a test chip.

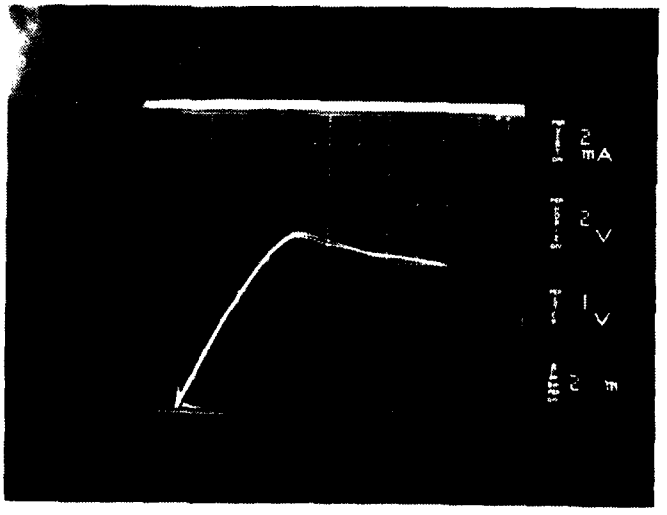

Figure 6(a). TELD characteristic showing current saturation.

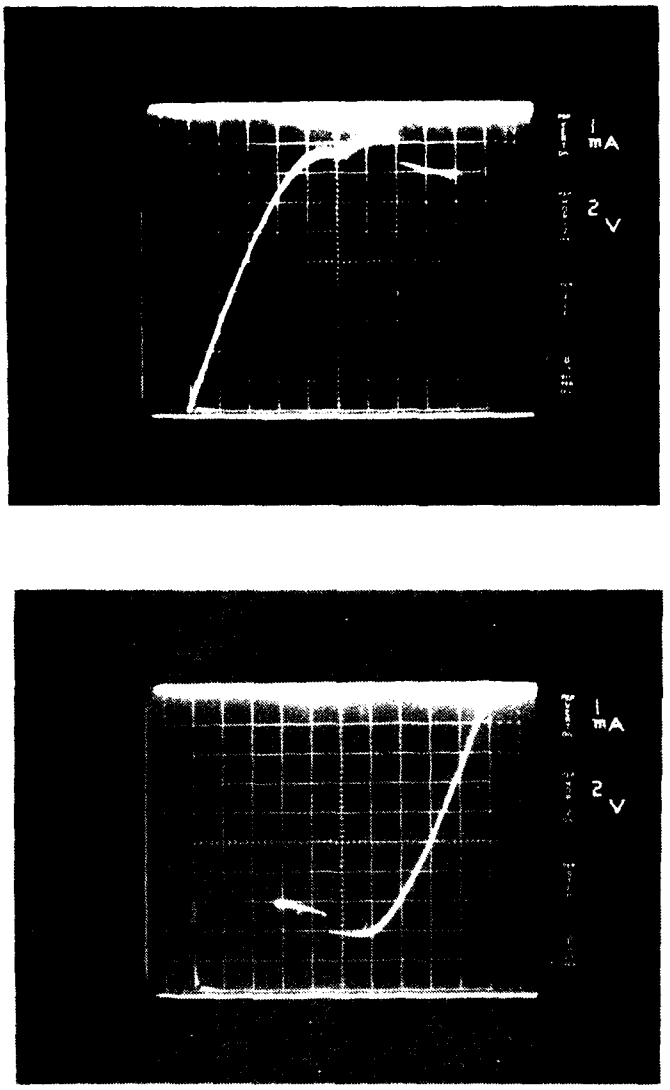

Figure 6(b). TELD characteristic showing polarity dependence:
(1) normal polarity (current saturates), and
(2) reverse polarity (current dropback observed).

Figure 6(c). TELD characteristic showing current drop.

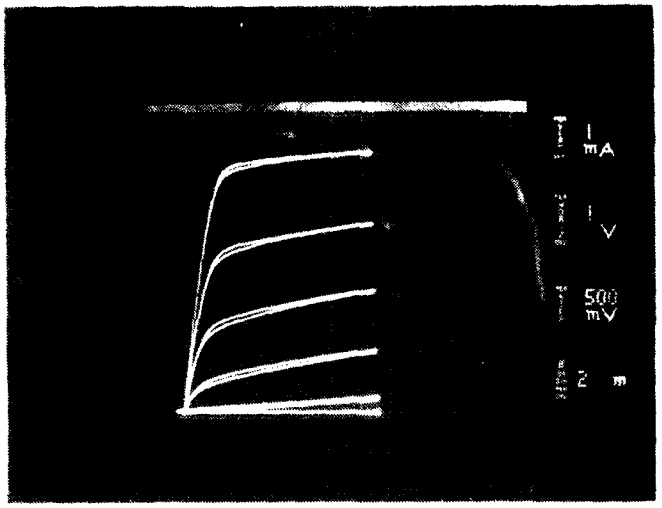

Figure 7. FET transfer characteristics.

The material parameters used and device characteristics observed on most of the wafers processed during the reporting period are summarized in Table 4. It can be seen that we had difficulty in getting FETs and TELDs working together satisfactorily.

A photomicrograph of a fabricated ADDER chip is shown in Fig. 8. We were able to successfully go through all the processing steps and complete the ADDER circuit. We could not evaluate the ADDER operation as the current drop in TELDs was too small.

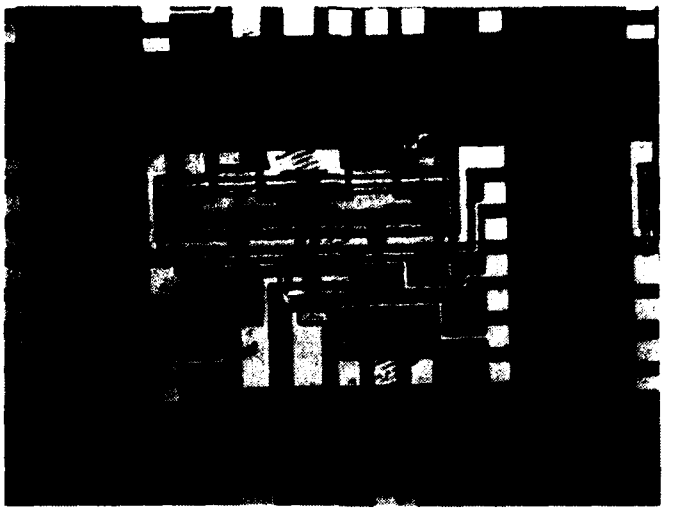

Figure 8. Photomicrograph of a fabricated GaAs full ADDER chip.

TABLE 5. MATERIAL PROPERTIES AND DEVICE CHARACTERISTICS ON THE WAFERS PROCESSED DURING THIS PHASE OF THE PROGRAM.

	Material Parameters				FET Characteristics		TELD Characteristics		
	Active Channel		n^+ Capping Layer						
Wafer #	Doping ($x10^{16} cm^{-3}$)	Thickness (μm)	Doping ($x10^{18} cm^{-3}$)	Thickness (μm)	I_{DSS} (mA)	gm (mS)	Threshold Current (mA)	Percentage Current Drop	Comments
C-285	2.0	1.0	3.0	0.4					
C-314	2.0	1.0	3.0	0.4					
C-315	2.0	1.0	3.0	0.4	14.0	8.0	16.0	15.0	IC being completed.
C-316	2.0	1.0	3.0	0.4	-	-	9.0	-	TELDs saturating.
C-332	2.0	1.0	3.0	0.4	-	-	14.0	<5	Very light-sensitive
C-333	2.0	1.0	3.0	0.4	-	-	13.0	-	Current saturates
C-348	2.0	1.0	3.0	0.4	-	-	20.0	-	Current saturates
C-349	2.0	1.0	3.0	0.4	-	-	12.0	-	Current saturates
C-350	2.0	1.0	3.0	0.4	-	-	15.0	-	Current saturates
C-351	2.0	1.0	3.0	0.4	18-20	2.0	40.0	<3	
C-413	2.0	1.4	-	-	-	-	-	-	Contacts nonohmic; metal bubbling
C-416	2.0	1.4	-	-	-	-	-	-	Metal bubbled; hard to open FETs
C-417	2.0	1.4	-	-	<0.5	-	-	-	FET current very low
C-448	2.0	1.0	0.2	0.4	-	-	18.0	<2	Has 1.0-μm undoped buffer
C-471	2.0	1.4	-	-	14.0	4-5	3.0	-	FET unstable; TELDs saturate
C-490	2.0	1.0	0.2	0.4	-	-	-	-	Has undoped buffer; after etching 3.1-μ-deep for mesas, no isolation; low V_β
C-491	2.0	1.0	0.2	0.4	16.0	-	20.0	10	TELDs completed first. Difficulty in completing FETs
C-642	2.0	3.5	-	-	-	-	6.0	-	Electrolytically etched; no current drop; electron trapping effects observed.
C-643	2.0	1.4	0.2	0.2	-	-	25.0	-	TELD saturates.
C-644	2.0	1.4	0.2	0.2	16.0	1.0	8.0	12	No current drop in normal polarity; current drop seen in the opposite polarity. IC completed.

TABLE 5. (Continued)

Wafer #	Material Parameters: Active Channel Doping ($x10^{16} cm^{-3}$)	Active Channel Thickness (μm)	n^+ Capping Layer Doping ($x10^{18} cm^{-3}$)	n^+ Capping Layer Thickness (μm)	FET Characteristics: I_{DSS} (mA)	FET Characteristics: gm (mS)	TELD Characteristics: Threshold Current (mA)	TELD Characteristics: Percentage Current Drop	Comments
D-92	2.0	1.0	3.0	0.4	-	-	-	-	Has 5-μm buffer. After milling 2.4 μ, no intermesa isolation.
D-93	2.0	1.0	-	-	-	-	-	-	No intermesa isolation.
D-94	2.0	1.0	-	-	-	-	6.0	-	TELDs saturating.
D-97	2.0	1.0	3.0	0.4	-	-			Has 5-μm buffer; TELDs saturating
D-122	2.0	1.4	-	-	-	-	12-14	20-25	TELDs saturate in the normal polarity and thresholds in the opposite polarity. Has 5-μm undoped buffer.
D-123	2.0	1.4	-	-	-	-	-	-	Contacts nonohmic; has 5-μm undoped buffer.
D-132	2.0	1.0	3.0	0.4	-	-	-	-	Has 5-μm undoped buffer; no mesa isolation after milling deep into buffer layer.
D-149	2.0	1.4	-	-	-	-	-	-	Contacts nonohmic.
D-150	2.0	1.4	-	-	8.0	4.0	4.0	-	TELD saturate; IC completed.
D-168	2.0	1.4	-	-	-	-	1.0	-	TELDs saturate.
D-172	2.0	1.4	-	-	-	-	-	-	Contacts nonohmic.
D-183	2.0	1.2	-	-	-	-	2.5-3.0	10-15	Has 6-μm buffer; TELDs low current; FETs not completed.
D-195	2.0	1.4	-	-	16.0	7.0	1.0	-	Has 5-μm buffer; FETs unstable; TELDs saturate.
D-200	2.0	1.4	-	-	-	-	90.0	-	TELDs saturate; have to mill 5 μm for isolation.
D-258	2.0	1.4	-	-	-	-	4.0	-	Has 5-μm buffer; TELDs saturate.
D-297	2.0	1.4	-	-	-	-	40.0	-	TELDs saturate.
D-385	2.0	1.2	0.2	0.3	7.0	4.0	-	-	FETs unstable; burning out during measurements on the curve tracer.
D-386	2.0	1.2	0.2	0.3	16.0	4.0	6.0	-	TELDs saturate.
D-390	2.0	1.4	0.2	0.2	8.0	4.0	5.0	-	FETs have positive slope in saturation; TELDs saturate.
D-391	2.0	1.4	0.2	0.2	10.0	4.0	5.0	<5	IC completed.
D-415	2.0	1.4	0.2	0.2	-	-	7.0	-	No current drop in TELDs; current jumps above threshold voltage.
D-423	1.0	3.5	-	-	-	-	7.5	-	Current jumps above threshold voltage.
D-493	2.0	1.0	0.1	0.4	-	-	2.0	-	Electron trapping effects observed.
B-1053	1-1.5	1.0	3.0	0.3	-	-	-	-	Contacts nonohmic.
B-69+	2.0	1.5	-	-	-	-	25.0	-	No thresholding; has 1.5-μ undoped buffer.
B-138+	1.0	1.6	1.0	0.4	-	-	6.0	-	TELD saturates; trapping effects observed.

+Wafers grown after the semi-automated control system was installed.

SECTION IV

CONCLUSIONS

The TELD-FET combination device provides substantial improvements in operating characteristics over TELD with resistive loads. It has better trigger-sensitivity and stability. The power dissipation can also be reduced to 0.16 to 0.2 of that for TELDs with resistive load. The capacitive output of TELD-FET makes direct interconnections possible without level shifting. Majority logic can be implemented with TELDs which reduces the component count substantially. The full ADDER circuit is a good example of this. Technology was developed for the fabrication of small-scale GaAs integrated circuits. Further improvements are required in the growth of GaAs epitaxial layers which will result in improved device characteristics. The 25 to 30% current drop devices are required for the successful operation of TELD integrated digital circuits.

REFERENCES

1. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Transferred-Electron Logic Device (TELD) Development," ONR Contract No. N00014-75-C-0100, Annual Repeat, September 1978.
2. R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETs," IEEE Trans. Electron Devices ED-21(6), 357 (1974).

BIBLIOGRAPHY

TECHNICAL REPORTS

1. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Microwave Shift Register," ONR Contract No. N00014-75-C-0100, Annual Report, February, 1976.
2. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Transferred-Electron Logic Device (TELD) Development," ONR Contract No. N00014-75-C-0100, April, 1977.
3. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Transferred-Electron Logic Devices (TELD) Development," ONR Contract No. N00014-75-C-0100, September, 1978.

PUBLICATIONS AND PRESENTATIONS

The following articles were published in technical journals, or presented at technical conferences.

1. L. C. Upadhyayula et al., "Transferred-Electron Logic Devices (TELDs) for Gigabit Rate Signal Processing," Digest of Technical Papers, 1976 IEEE-MTTS International Microwave Symposium, p. 164.
2. L. C. Upadhyayula, "Trigger Sensitivity of Transferred-Electron Logic Devices," IEEE Trans. Electron Devices ED-23, 1049-1052 (Sept. 1976).
3. L. C. Upadhyayula et al., "Transferred-Electron Logic Devices (TELDs) for Gigabit Rate Signal Processing," IEEE Trans. Microwave Theory and Techniques MTT-2 (12), 920 (Dec. 1976).
4. L. C. Upadhyayula, "Monolithic Logic Circuits with Transferred-Electron Logic Devices (TELDs)," Digest of Technical Papers, First Specialty Conference on Gigabit Logic for Microwave Systems, May 1979, Orlando, Florida, p. 136.

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