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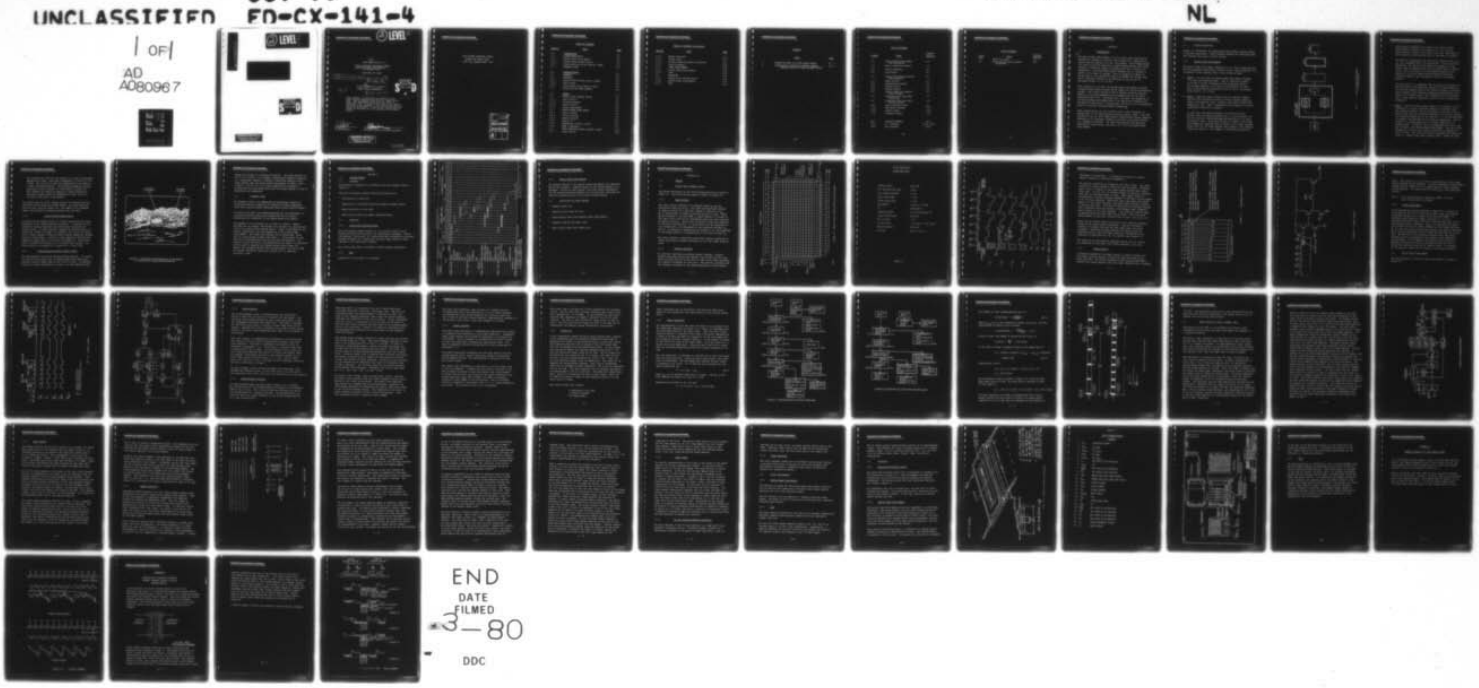

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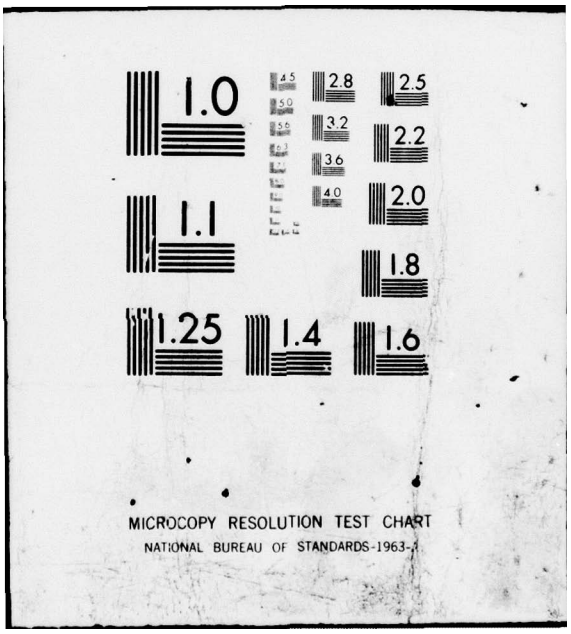
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(2) LEVEL II

**FAIRCHILD IMAGING SYSTEMS**
A Division of Fairchild Camera and Instrument Corporation

(14) Report FED-CX-141-4

# Fourth Quarterly Technical Report
# (6) Analog Frame Store Memory,
# 15 October 1979

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(12) 58

(11) 15 Oct 79





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Director, Electro-Optical Equipment

**FAIRCHILD IMAGING SYSTEMS**
A Division of Fairchild Camera and Instrument Corporation

THIS FOURTH QUARTERLY REPORT
COVERS THE PERIOD FROM
JULY 1979 THROUGH SEPT. 1979

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# SECTION I

## 1.0 INTRODUCTION

The Analog Frame Store Memory is an all solid state high density storage unit capable of storing a full frame of TV information in analog form for periods up to ten (10) seconds. The storage element is a state-of-the-art monolithic charge coupled device (CCD) which contains a sufficient number of storage sites for a field of TV information. The Frame Store Memory combines two (2) devices to obtain a full frame of storage. Data is inputted to memory in analog form at the standard TV rate of 30 Frames Per Second (FPS) and is outputted through an A/D converter at one of six (6) selectable rates; 0.1 to 7.5 FPS.

When installed in the RPV, the Analog Frame Store Memory provides a frame storage buffer between the TV camera and the data compression encoder. Full frame storage of the TV imagery minimizes the complexity of the data compressor when transmitting over the RPV's narrow band data link. The small size, low power and ruggedness of the Analog Frame Store Memory make it an attractive candidate for the Army RPV application, in particular, and to act as an intermediate buffer for general TV based imaging systems.

Image reconstruction of the received signal, after decoding, is accomplished in the Image Analyzer Digital Display (IADD). The IADD consists of two (2) full frame dynamic random-access digital memories operating in a "ping-pong" fashion to provide a continuous display on a standard TV monitor. The IADD also provides the operating instructions (Mode Select, Data Rate, etc.) for the Analog Frame Store Memory.

## 1.1 SYSTEM DESCRIPTION

Figure 1-1 illustrates the Analog Frame Store Memory System concept in the RPV application. Those elements designed and developed under this contract are shown in heavy outline.

### 1.1.1 Analog Frame Store Memory

The Analog Frame Store Memory combines two (2) field storage devices with the necessary electronics (drivers, logic, video processor, etc.) to operate on the incoming video in the following modes:

A. Mode 1 - In this mode the Analog Frame Store Memory operates in a scan rate reduction mode. Data is inputted to memory at 30 FPS in either interlaced or non-interlaced format. The storage capacity is 512 lines at 640 samples per line. Data is digitized and outputted at one of six (6) selectable rates from 0.1 to 7.5 FPS.

B. Mode 2 - Sampling theory dictates that at least two samples per pixel are required in order to resolve imagery unambiguously at the Nyquist limit. However, this would require 1280 samples per line. Mode 2 requires only 640 samples to achieve unambiguous resolution at Nyquist.

   In this mode, multiplexed sampling is used at twice the Nyquist limit for each horizontal line. In this fashion, two TV lines contain interleaved sampling data which is at twice the Nyquist limit. Twice Nyquist data is stored in the frame store memory by inputting data to device 2 with input transfer clocks that are 1/2 pixel delayed with respect to the transfer clocks for device 1. For example, a black-white pattern at

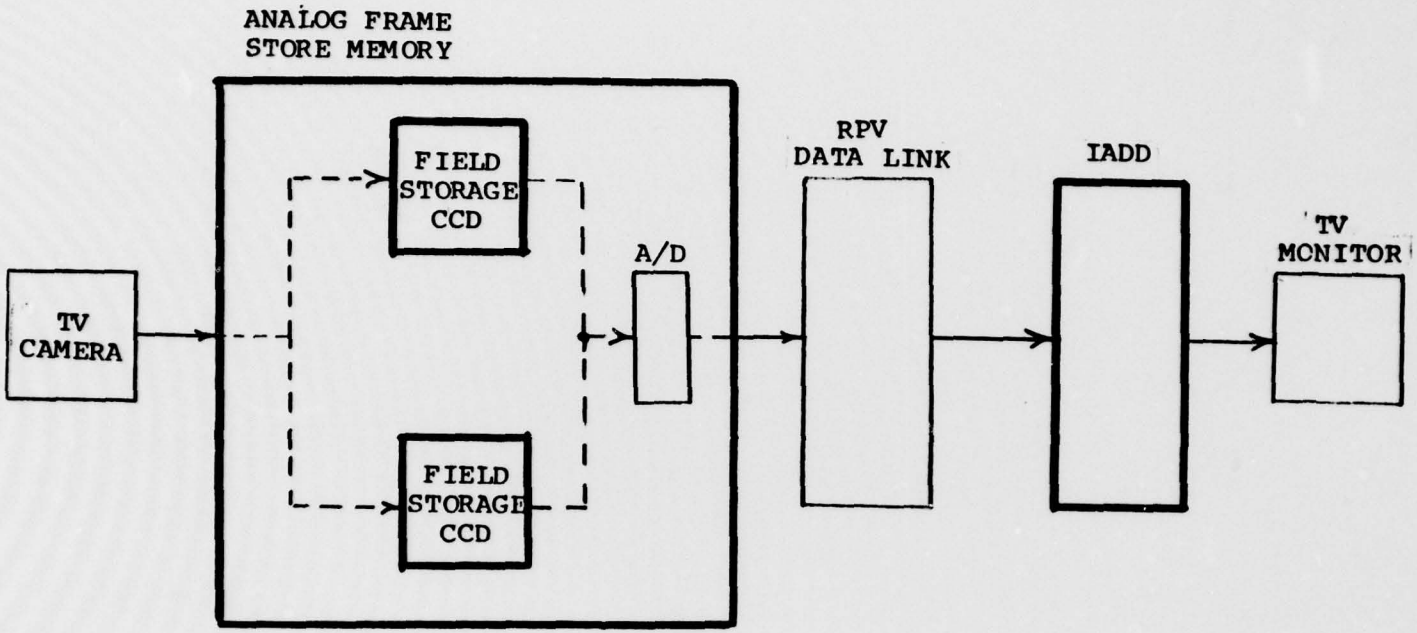



FIG. 1 - 1 ANALOG FRAME STORE MEMORY
RPV APPLICATION

twice Nyquist frequency will result in all white levels being stored in device 1 for lines 1,3,5, etc. and all black levels in device 2 for lines 2,4,5, etc. This data is scan converted, digitized and sent to the IADD as in Mode 1.

The IADD will reconstruct the picture by reading lines 2,4,6, etc. out of memory with a 1/2 pixel shift. Prior to the D/A conversion, the odd and even fields are chopped at twice Nyquist with in phase and 180° out of phase signals, respectively. This will result in a dot pattern display on the monitor of a full TV frame having increased horizontal resolution greater than the Nyquist limit of the storage devices.

From the above, it is apparent that as long as the display is reconstructed in the same mode, and with the same timing, as the original sampled video a "dot matrix" display is obtained which contains video frequency components proportioned to the width of the sample pulse. This technique will be evaluated from a human factors standpoint as well as from a resolution standpoint.

C. Mode 3 - There are applications where it is necessary to view a portion of a scene, containing targets of interest, with more frequent updates than are available in the scan rate reduction mode and still maintain compatibility with the information handling capability of the data link. It is also desirable to preserve the remainder of the scene as background. This is typical of a system operating in a target acquisition or tracking mode. In Mode 3, this is accomplished by storing two sets of data in the Analog Frame Store Memory. One set of data represents a field of the incoming video and is updated at a rate of 1 FPS. The other set of data represents the center 112 lines of a frame of the same incoming video. These 112 lines

are truncated so that only the center 112 of the 640 available samples are stored. This data is updated at a rate of 7.5 or 15 FPS. The two sets of data are transmitted to the IADD in a time interleaved fashion. The resulting composite picture displayed on the TV monitor is illustrated in Figure 1-2. This concept can readily be adapted to target tracking by providing variable position information to move the 112 x 112 area to any point in the raster.

The outputs from the field storage devices are combined and A/D converted into an eight bit serial format. The code idents for start of line, start of frame, etc., are added to the combined output and formatted to operate directly into the IADD.

### 1.1.2 Analog Field Storage Device

The Analog Field Storage Device is a solid state monolithic array operating on the "charge coupled" principle. It consists of 640 columns of storage registers with each column containing 256 storage sites. An input register, capable of clocking data in at rates from 40KHz to 12.0MHz, is located at the top of the array, with an ouput register having the same clocking capability located along the bottom edge. A device is thus capable of storing 164K samples of analog data or one field of standard TV. Data can be held in storage for periods up to 10 seconds with cooling. The entire device is contained on a single 199 x 740 mil chip.

### 1.1.3 Image Analyzer Digital Display (IADD)

The IADD performs the picture reconstruction function. It accepts the digital data stream from the Analog Frame Store Memory and creates a digital image frame of 488 x 640 x 8 bits. It performs digital to analog conversions to create a 30 FPS composite video

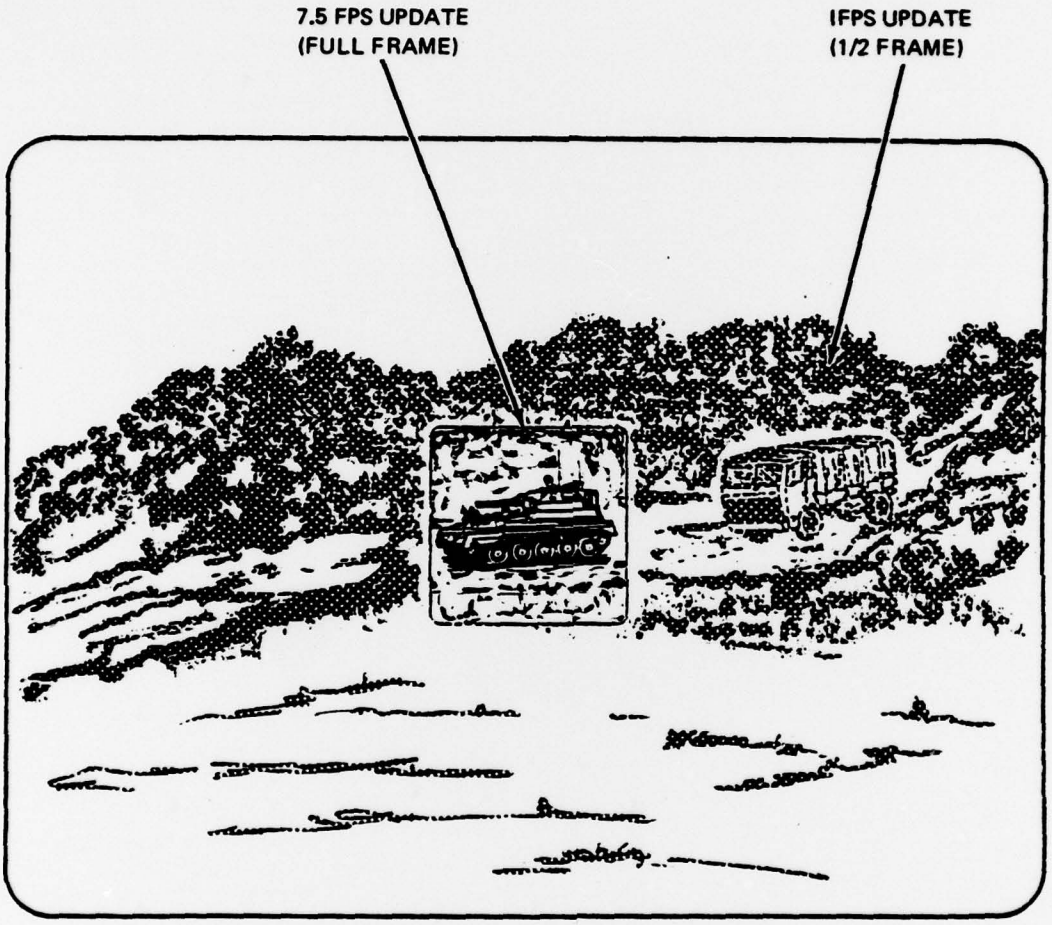



FIGURE 1-2. ILLUSTRATED TV MONITOR DISPLAY OF THE IMAGERY AT THE IADD OUTPUT DURING MODE 3 OPERATION

signal for display on a standard TV monitor. The IADD consists of two (2) 512 x 1024 x 8 bit dynamic random-access memories operating in a "ping-pong" fashion to provide a continuous display of the video signals from the Analog Frame Store Memory in modes 1 and 2. In Mode 3, two (2) 112 x 112 static memories are operated to re-construct the high speed data while the dynamic memory is used to reconstruct the background.

## 1.2 PROGRAM'S GOAL

The program's goal is to demonstrate an operational capability to provide scan rate reduction of standard TV signals employing solid state analog storage techniques using charge coupled devices.

To achieve this goal, the program provides for the development of a state-of-the-art analog field storage CCD and the design, fabrication and evaluation of the Analog Frame Store Memory.

The program is to be carried out in three (3) phases. Phase I provides for the design, fabrication (six devices) and characterization of the analog field storage device. Phase II provides for the design, fabrication, test and evaluation of one Analog Frame Store Memory. The frame store memory will be fabricated, using two (2) field storage devices from Phase I. During Phase II, the IADD will be designed and built for use during evaluation. The results of both the Phase I characterization and Phase II evaluation will be used to optimize the storage device during Phase III. Twelve (12) optimized devices will be fabricated, two will be used to retrofit the Analog Frame Store Memory and the remainder delivered to NVL.

SECTION II

## 2.0 PROGRAM STATUS

### 2.1 SCHEDULE

The program is proceeding in accordance with the schedule shown in Figure 2-1.

The major milestones achieved during this quarter are:

- Continuation of wafer fab.
- Completion of the Analog Frame Store Memory hardware design.
- Began fabrication of the IADD
- Began Analog Frame Store Memory software design.

### 2.2 TECHNICAL

#### 2.2.1 Anlaog Field Storage Device

The seven masking steps referred to in an earlier report can be further divided into forty-four (44) fabrication processes. During this quarter, thirty-nine (39) wafers have been successfully processed through seventeen (17) operations, bringing these wafers to step nineteen in the fabrication process.

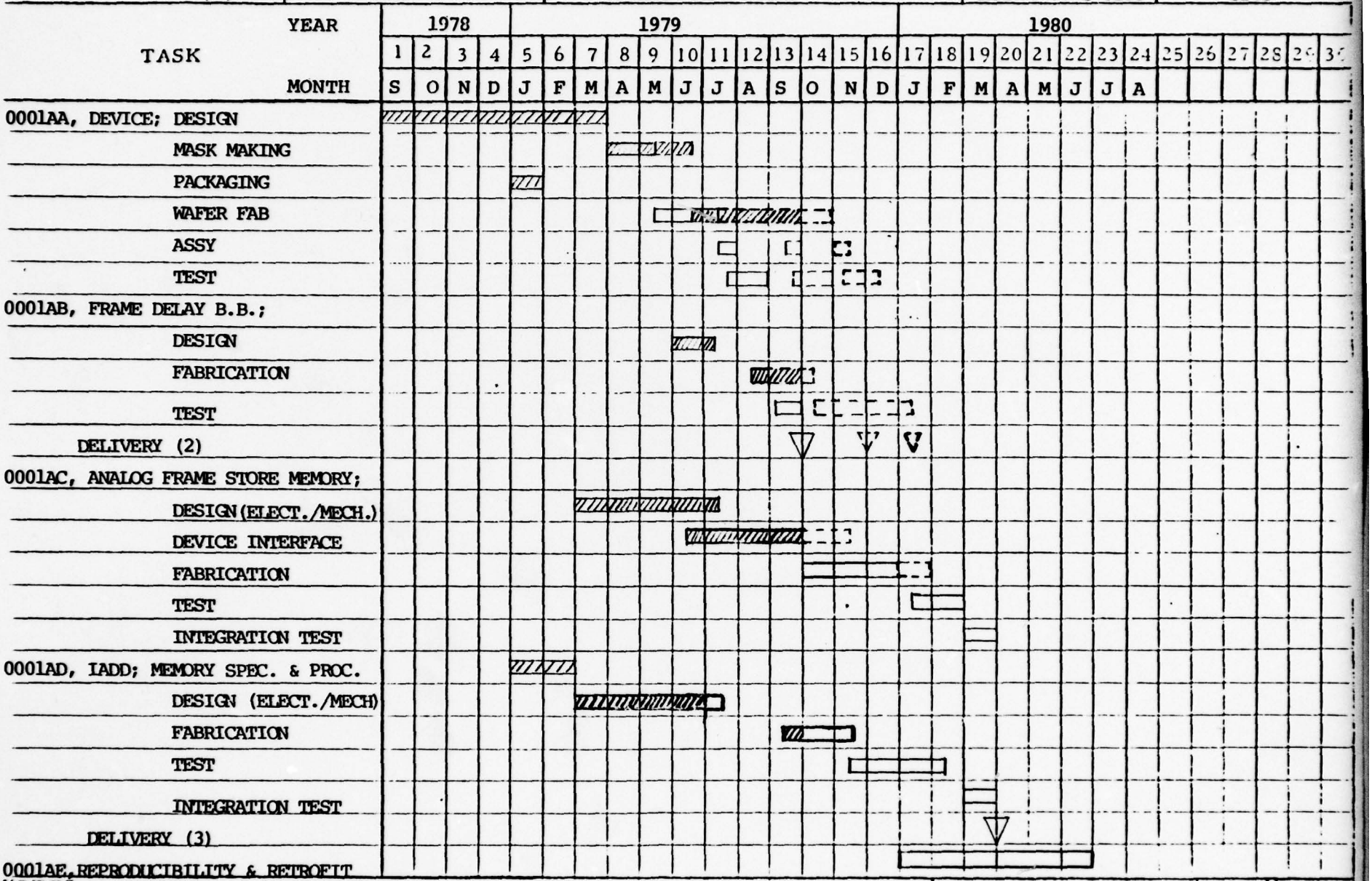
The initial poly mask is included in these nineteen operations.

#### 2.2.2 IADD

Fabrication of the IADD is in progress.

# PROJECT SCHEDULE

| Proj. Engr. | Date (1) | Customer | Project Title | Contract | Job No. |
|---|---|---|---|---|---|
| A. Roberts | 4/5/79 | NVL | ANALOG FRAME STORE | DAAK70-78-C-0165 | 6248 |




NOTES (1) Schedule revised as of 13TH Monthly Report
(2) Delivery of 0001AA and 0001AB
(3) Delivery of 0001AC and 0001AD

KEY: Complete - Planned - Slip - Delivery

### 2.2.3 Analog Frame Store Memory

The hardware design of the Analog Frame Store Memory was completed during this quarter. Software design for the microprocessor is in progress. During the next quarter, the total power requirements for the Analog Frame Store Memory will be finalized, including the power for optimum cooling of the field storage devices.

## 2.3 ACTIVITIES FOR NEXT QUARTER

- Complete wafer fab.
- Complete device assy and test.
- Define Analog Frame Store Memory power requirements.
- Complete IADD fab and begin test.
- Begin Analog Frame Store Memory fab.

SECTION III

# 3.0 DESIGN

## 3.1 ANALOG FIELD STORAGE DEVICE

The design objectives for the field storage device are listed in Table 3-1. The device block diagram is shown in Figure 3-1.

### 3.1.1 Input Circuit

The input circuit consists of a diffused diode $V_{IN}$ and two polysilicon gates $\phi_3$ and $V_R$. The input structure and clocking is shown in Figure 3-2. The input voltage is applied to $V_{IN}$. $\phi_S$ is clocked high to sample $V_{IN}$ during the $\phi_1$ low time. After $\phi_S$ has returned to the low state, a charge packet Q is stored in the input circuit and can be transferred along the input register by clocks $\phi_1$ and $\phi_2$. These input horizontal clocks are generated by off-chip clock drivers. It can be seen that the magnitude of Q is determined by the difference of the potentials between $V_{IN}$ and $V_R$. By applying an appropriate dc voltage to $V_R$, the magnitude of the charge packet Q is proportional to the input voltage $V_{IN}$.

The input register is designed using buried channel technology to insure good charge transfer efficiency at the high speed clocking rates.

### 3.1.2 Parallel Register

The parallel registers are surface channel devices. Surface channel technology allows more charge to be stored per unit area. Since the major portion of the chip is taken up by these registers, this greatly influences the chip size. The parallel registers are low frequency registers so the speed advantage of buried channel

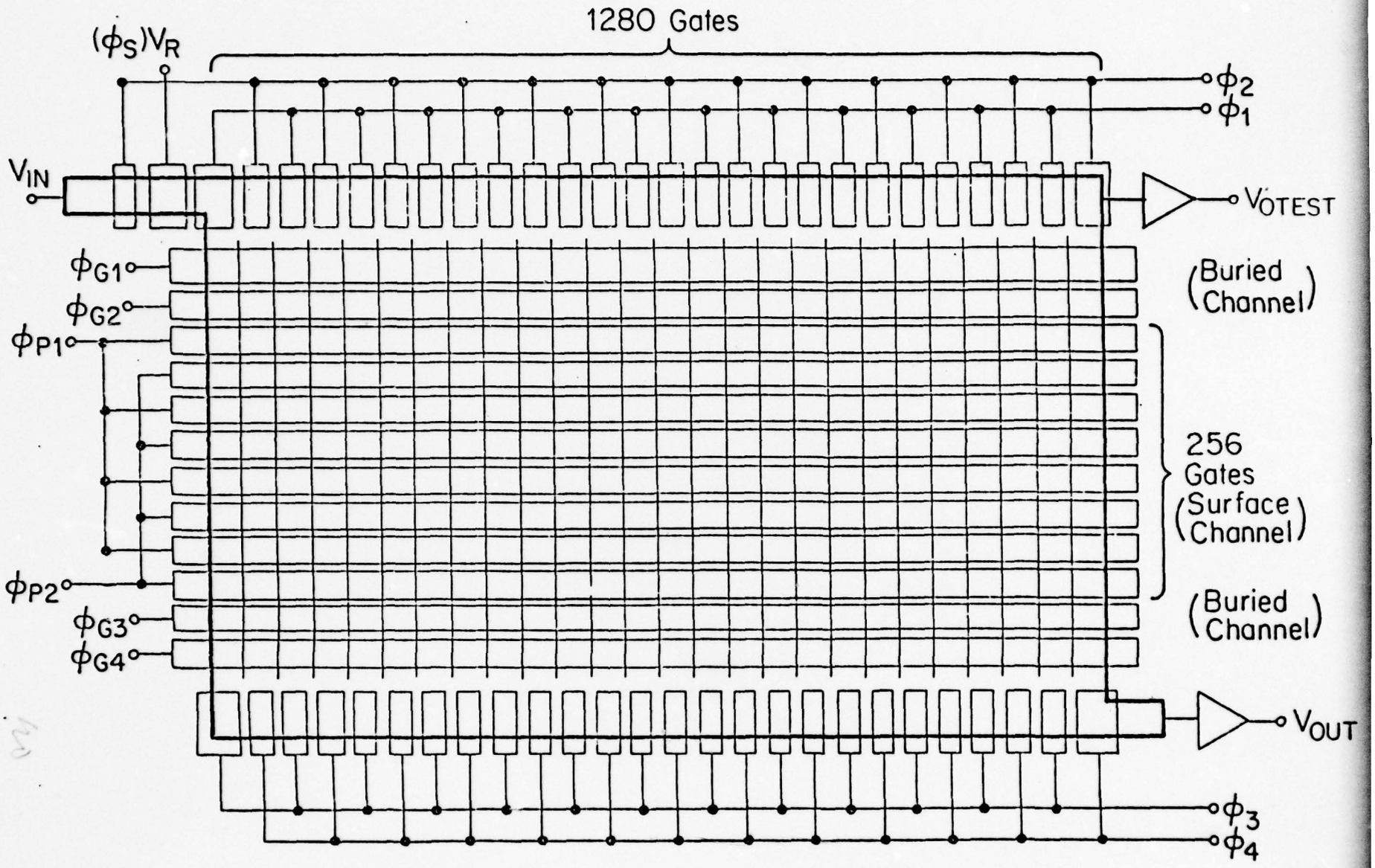



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FIGURE 3-1 ANALOG FIELD STORAGE DEVICE BLOCK DIAGRAM

## FIELD STORE DEVICE

## DESIGN OBJECTIVES

| | |
|---|---|
| STORAGE CAPACITY | 640 X 256 |
| MAX. HORIZONTAL DATA RATE | 12 MHz |
| MAX. VERTICAL DATA RATE | 16 KHz |
| INPUT SIGNAL SWING | 1 V TYP. |
| OUTPUT SIGNAL SWING | 1 V TYP. |
| NONLINEARITY | $\pm$ 3% TYP., $\pm$ 5% MAX. |
| CTE | 0.99995 MIN. |
| SATURATION CHARGE | $0.9 \times 10^6$ ELECTRONS TYP. |
| SIGNAL-TO-NOISE RATIO | 50 dB MIN. |
| MAX. DC SUPPLY | + 15 V |
| AC CLOCK INPUT | 4 TTL CLOCKS + 2 MOS CLOCKS |
| POWER DISSIPATION | 300 mW MAX. |
| CHIP AREA | 199 mil X 740 mil |

**TABLE 3-1**

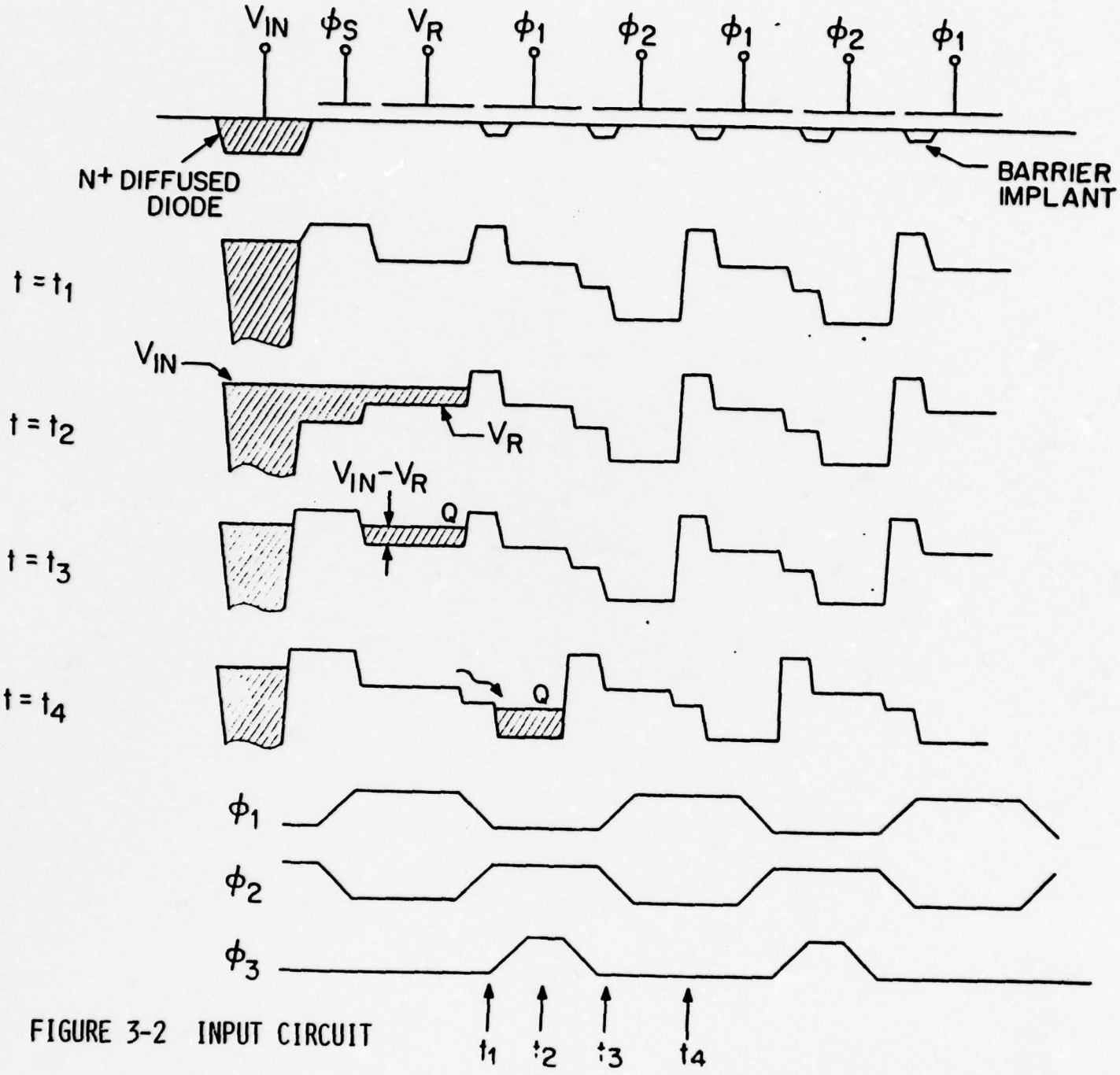



FIGURE 3-2 INPUT CIRCUIT

technology is unnecessary. A discussion of buried to surface channel transfer is contained in Appendix 2.

The parallel registers are clocked by two phase clocks. The input register and output register clocks are also two phase. Therefore, when a line is clocked in, the signal charge resides under every other gate. As this line is clocked through the parallel registers, only half the available space is used. Each signal charge is clocked down a vertical register adjacent to the gate it was stopped at in the input register. Since only every other gate had charge under it in the input register, only every other vertical register is used by each line. So as not to waste half the vertical register area, alternate lines are clocked in and stopped under different sets of gates in the input register. Odd lines are stopped under the $\phi_2$ gates and even lines under the $\phi_1$ gates. With this interlacing scheme all parallel register area is used, (see figure 3-3).

There are two special gates at each end of the parallel registers. Charge is not stored under these gates. They are included to isolate the storage area from the high speed input and output registers. Capacitive coupling between the parallel and I/O registers during input and output clocking is minimized by the insertion of these gates G1, G2, G3, and G4, (see Figure 3-1).

All clocks to run the parallel registers and G1, G2, G3, and G4 are generated on chip from 2 TTL clocks supplied to the chip.

### 3.1.3 Output Circuit

A schematic diagram of the output circuit is shown in Figure 3-4. The output register employs the same two phase structure as the input register. The on-chip generated clocks $\phi_3$ and $\phi_4$ (SEE NOTE 1) transfer the charge packets along the output register into a diffused

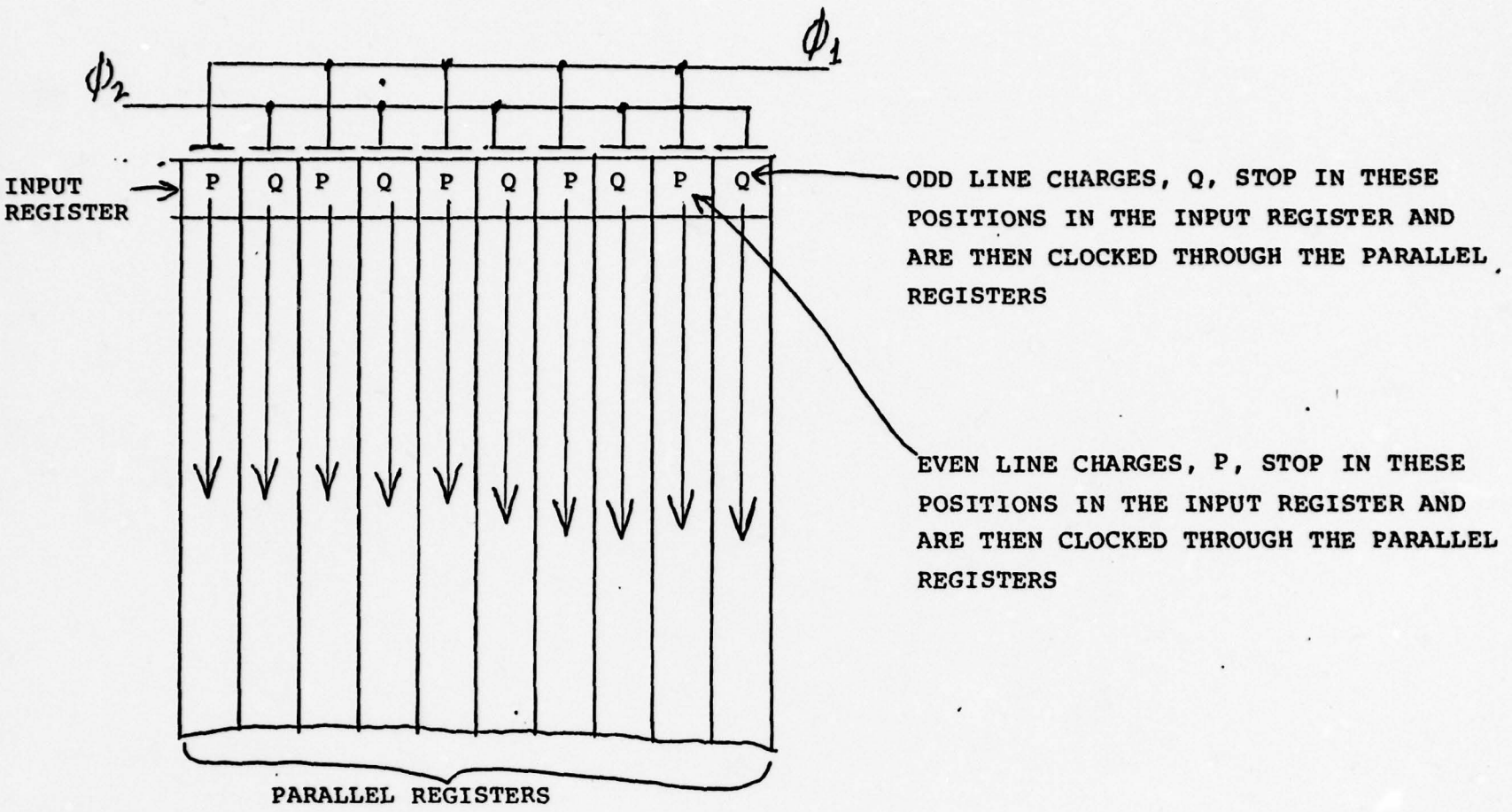



FIGURE 3-3 INTERLEAVED CLOCKING

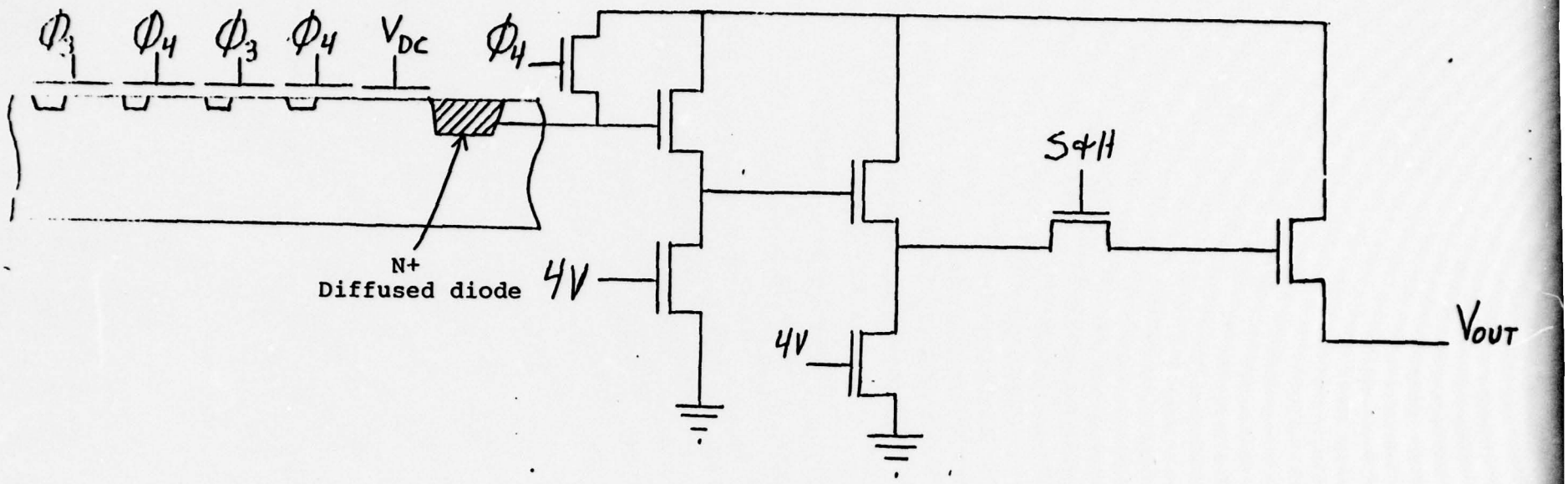



FIGURE 3- 4 OUTPUT CIRCUIT

diode. The potential of this diode is monitored by a three stage source-follower output amplifier. A gating transistor is positioned between the two stages so that a sample-and-hold output waveform can be obtained. The sample and hold clock $\phi_{SH}$ is also generated on-chip.

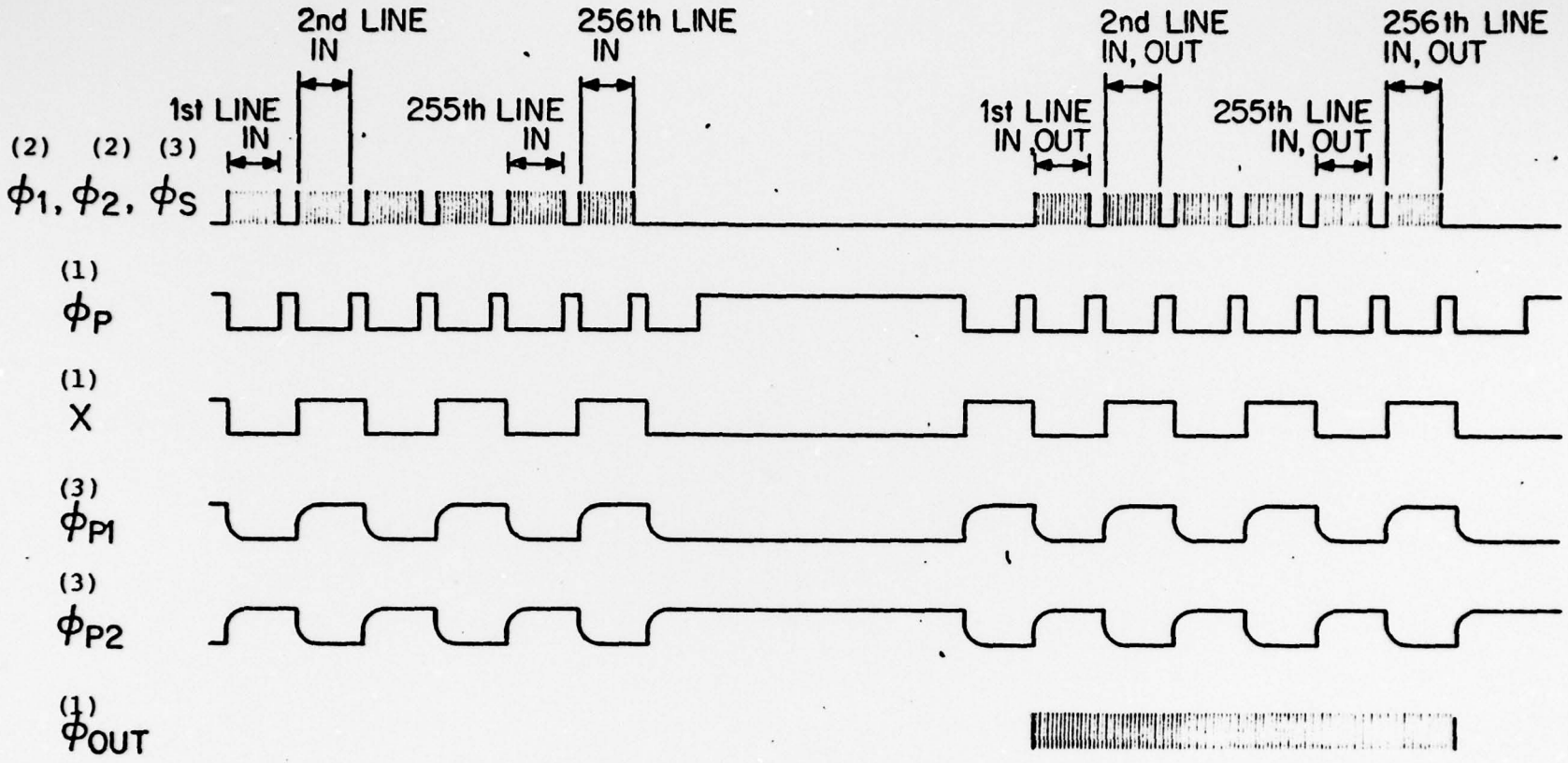
Note 1: For clocking speeds in excess of 400KHz, off-chip clock drivers must be provided.

### 3.1.4 Timing Requirement

As illustrated by the block diagram of Figure 3-1, a maximum of three external TTL level clocks and two MOS clocks are required to operate the device, at output rates less than 400KHz. A detailed timing diagram is shown in Figure 3-5. $\phi_I$ is a continuous MOS level input clock which controls the input circuit and the input serial registers. $\phi_{OUT}$ is a continuous TTL level clock which controls the output register and the output amplifier. $\phi_P$ is a TTL level input clock which controls the parallel registers. $\phi_P$ is typically operated at the 15.7KHz line rate with 10 µs high time. During this 10 µs horizontal blanking time, the serial register clocks are stopped and the parallel clock generators are activated. In this manner, the internal logic circuits to generate the parallel clocks are disabled during the 53.5 µs active line time when read-in and read-out occur. No coupling of the parallel clocks will be visible in the output waveform.

## 3.2 ANALOG FRAME STORE MEMORY

The block diagram of the Analog Frame Store Memory is shown in Figure 3-6.




(1) External TTL Clocks
(2) External MOS Clocks
(3) Internally Generated Clocks

FIG. 3-5 TIMING DIAGRAM

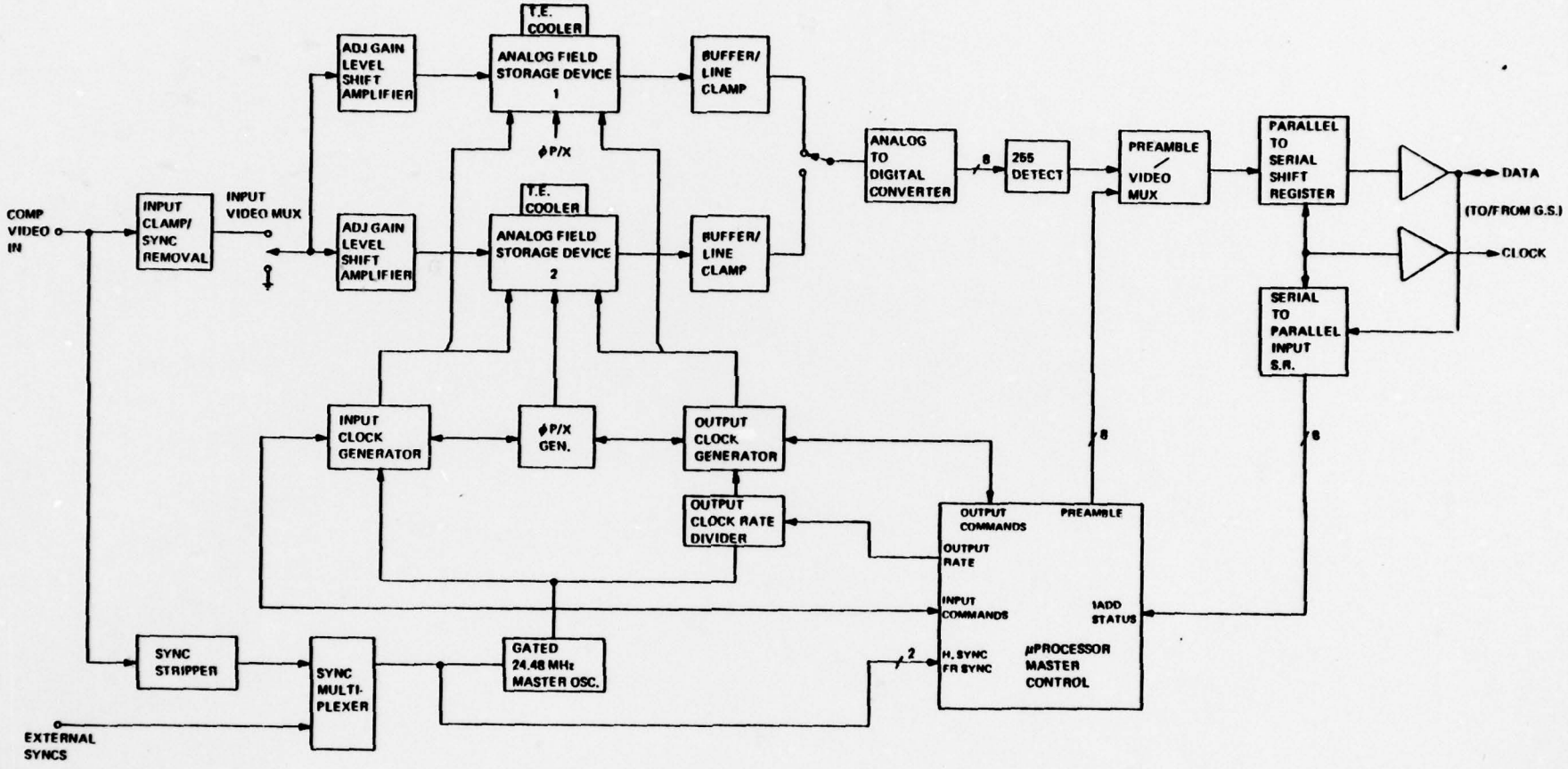



**FIGURE 3-6. ANALOG FRAME STORE MEMORY BLOCK DIAGRAM**

### 3.2.1 Input Circuits

The 30 FPS composite video is clamped during the "back porch" period of each line and the sync is removed from the signal. The resulting video passes through the input video multiplexer to the two independent adjustable gain amplifiers. The input is grounded for the first right pixels to provide a black clamp level for the outputs. Although the video is present at the input of each device, gating of the input clocks determines when video is to be stored in the devices.

Each video channel is independently adjustable to the desired gain and offset for the particular storage device through a wide band video amplifier. This data is inputted to the device via $\emptyset_I$ as described in paragraph 3.1.1. During Mode 2, alternate line video is inputted 180° out of phase. In this fashion, two TV lines contain interleaved sampling data which is at twice the Nyquist limit. For example a black-white pattern at twice Nyquist results in all white levels being stored for lines 1, 3, 5 etc., and all black levels for lines 2,4, 6 etc. This data is scan converted, digitized and sent to the IADD as in Mode 1.

The sync stripper circuit derives Horizontal and Frame Sync from standard EIA composite video. If the video input is in the form of non-interlaced serial data, Horizontal and Frame Syncs must be supplied.

### 3.2.2 Timing/Control Circuits

An 8085A microprocessor provides overall control for the system. The instructions for the microprocessor are stored in a UV Eraseable PROM of 2K x 8 bits. 256 x 8 bits of RAM are available for use by the microprocessor for temporary storage. The microprocessor controls the input and output functions of the field storage memories on a line oriented basis.

Real-time control is attained by the use of three hard-wired interrupts-line sync, frame sync, and output sync. The first two interrupts permit the microprocessor to maintain an input line count of the incoming composite video, while the latter interrupt indicates the completion of one line of output. Status information from the I.A.D.D. is converted to an 8 bit word in the serial to parallel input shift register, and then input to the microprocessor via an 8 bit input port. Control I.D. words are generated by the microprocessor and inserted into the data path via the preamble/ video multiplexer.

The maximum clock frequency required to output the slow scan digital data is 24.48 MHz at 7.5 FPS. The clock frequency required to input data to the storage device at 30 FPS is 12.24 MHz. In order to maintain a synchronous system, a master 24.48 MHz oscillator will be used with all clocks derived from this source. The input clock must be gated to provide precise synchronization with the incoming video. Since the input clock is derived from the master oscillator, the master oscillator must be capable of being gated at the start of each line during the input operation. Start-up of the oscillator will be delayed for an additional half cycle for alternate lines in Mode 2 operation. All clocking rates will be binary multiples of the master clock frequency. Therefore, the actual frame rates are .117, .469, .938, 1.88, 3.75 and 7.5 FPS.

The output clock divider, under microprocessor control, provides the output clock generator with the proper frequency clocks corresponding to the frame rate selected. The output clock generator, upon receipt of a command from the microprocessor, generates the clock pulses necessary for outputting one line of video from either of the two field storage devices. Upon completion of one line, an output complete interrupt is sent to the microprocessor. Each line outputted requires a separate output command.

30

The input clock generator, upon reciept of a command from the microprocessor and at the beginning of a line of video generates the appropriate clock pulses necessary for inputting video into one or both of the field storage devices. Inputting will continue for the multiple lines until a stop input command is received.

### 3.2.3 Output Circuits

The output from each device is independently amplified and filtered to eliminate clock modulation in the output amplifier. Independent black clamp circuits are provided to establish a dc reference for each device. The dc reference is derived from the first 8 pixels of each line which were referenced to black during input. The data is outputted from the storage device via $\emptyset_0$ as described in paragarph 3.1.3

The output multiplexer recombines the slow scan outputs from the storage devices into a serial output data format by "ping-pong" action between devices. The multiplexing is controlled via the Mux control signal.

The analog video information is converted to an 8 bit binary word by the A/D converter. A sample and hold circuit (internal to the A/D) provides the means to store the analog video level present at strobe time and hold this level for the entire conversion time. Strobe repetition rates from 47.8KHz to 3.06MHz are possible, yielding an equal number of A/D conversions. The A/D converter selected is capable of conversions from d.c. to 11 mega-conversions per second. The conversion time is 150 nanoseconds.

Each pixel time is divided into 8 bits representing 256 intensity levels. The bit time clock is eight times the pixel clock, yielding a maximum rate of 24.48MHz. At the beginning of each pixel time the next character is loaded in parallel to an 8 bit shift register. The data is then shifted out under control of the bit clock. The bit clock and S/R output are sent to the IADD for reconstruction and display through differential line drivers.

### 3.2.4 Control ID

In any transmission system involving serial digital data, synchronizing information must be inserted to identify the data and to establish the "frame" of the serialized byte (in this case, pixel). This synchronizing data must be unique in that the actual data must not be confused with the synchronizing data. In this system, the Frame Store Memory A/D converter generates data from 0 - 255 with 255 having the binary value of all ones. The A/D output will be tested for this condition and if it occurs, the least significant bit will be inverted changing the value to 254. Thus, the all ones condition cannot occur in normal data. This code will be reserved for synchronizing purposes. Each line of transmitted video will be preceded by three characters. The first two characters will be all ones. The third character will be uniquely defined by its relationship to the all ones data. This byte will always begin with a zero bit to establish the byte or pixel frame. Each line of video will contain a start of line character unless it is the first line of a frame.

Each line of video will contain:

2 characters of all ones
1 control character
640 image pixels

These characters will be inserted to read from the Frame Store Memory at the appropriate time under control of the central timing logic.

### 3.2.5 Mode 3 Operation

The implementation if the dual data rate mode is in accordance with the algorithms described in Figure 3-7 or Figure 3-8 depending upon the interlaced nature of the input video. The first set of data, stored in device 2, consists of 256 lines x 640 pixels representing a field of TV data and shall be referred to as the slow speed data. The second set of data, stored in device 1, is the center 112 pixels of the center 112 lines of the input video. This data shall be referred to as high speed data. Using an actual count of 112 rather than 100 maintains compatibility with the counting sequence of the IADD.

The slow speed data is outputted at .938 FPS and is time interleaved with the high speed data. After each high speed output, slow speed data is transmitted. The slow speed data requires several cycles to complete a full field. At 7.5 FPS the time allocated for slow speed transmission is:

$$T = (4 \times T_{st}) - T_{hs} \qquad \text{(EQ 1)}$$

Where $T_{st}$ is the standard frame time 33.33 msec., and $T_{hs}$ is the time required to output 112 lines at 7.5 FPS.

Substituting the above in EQ 1 we have

$$T = (4 \times 33.33) - 9.0 = 124.32 \text{ msec.}$$

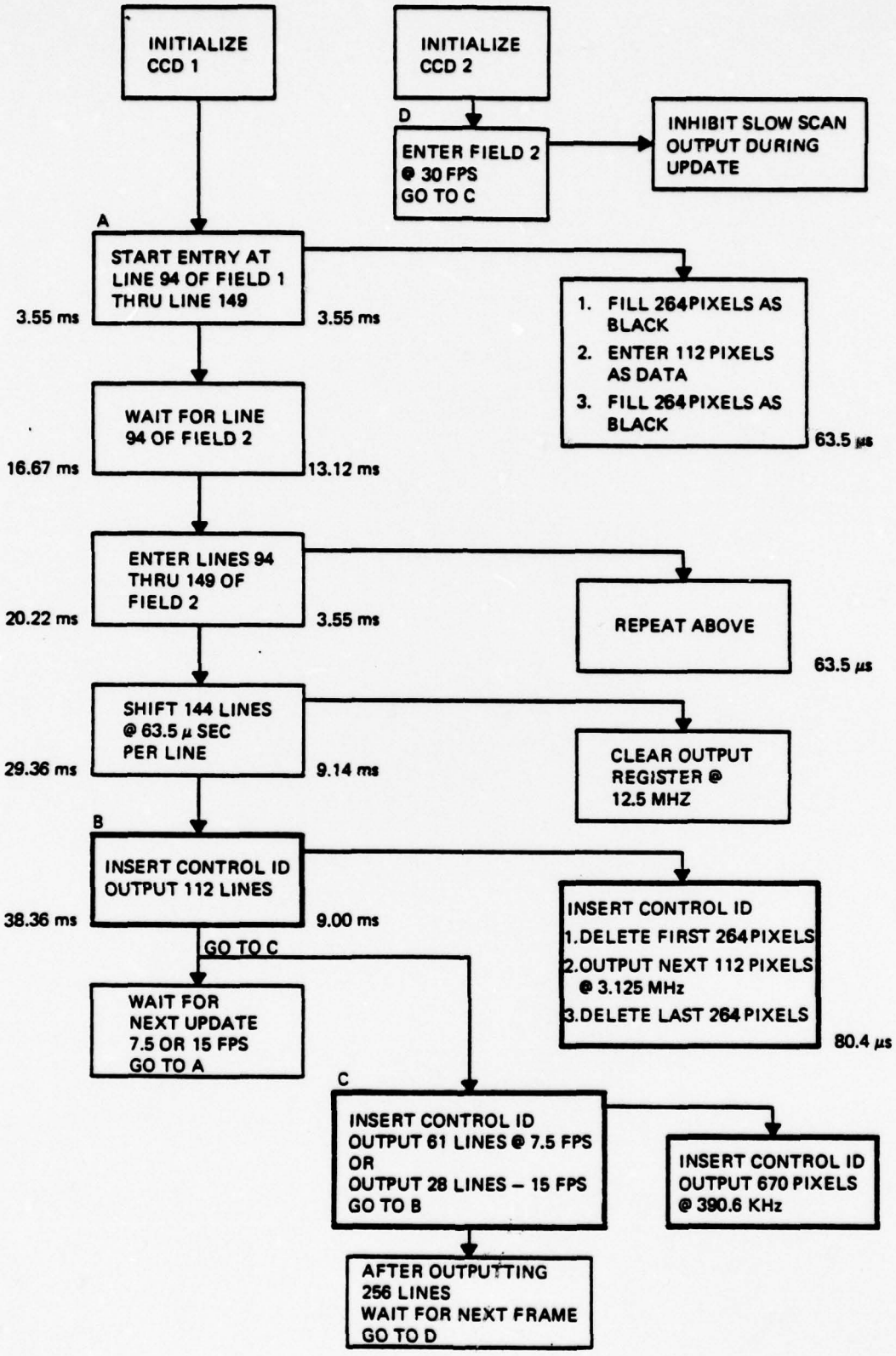



FIGURE 3-7. ALGORITHM; DUAL DATA RATE, INTERLACED

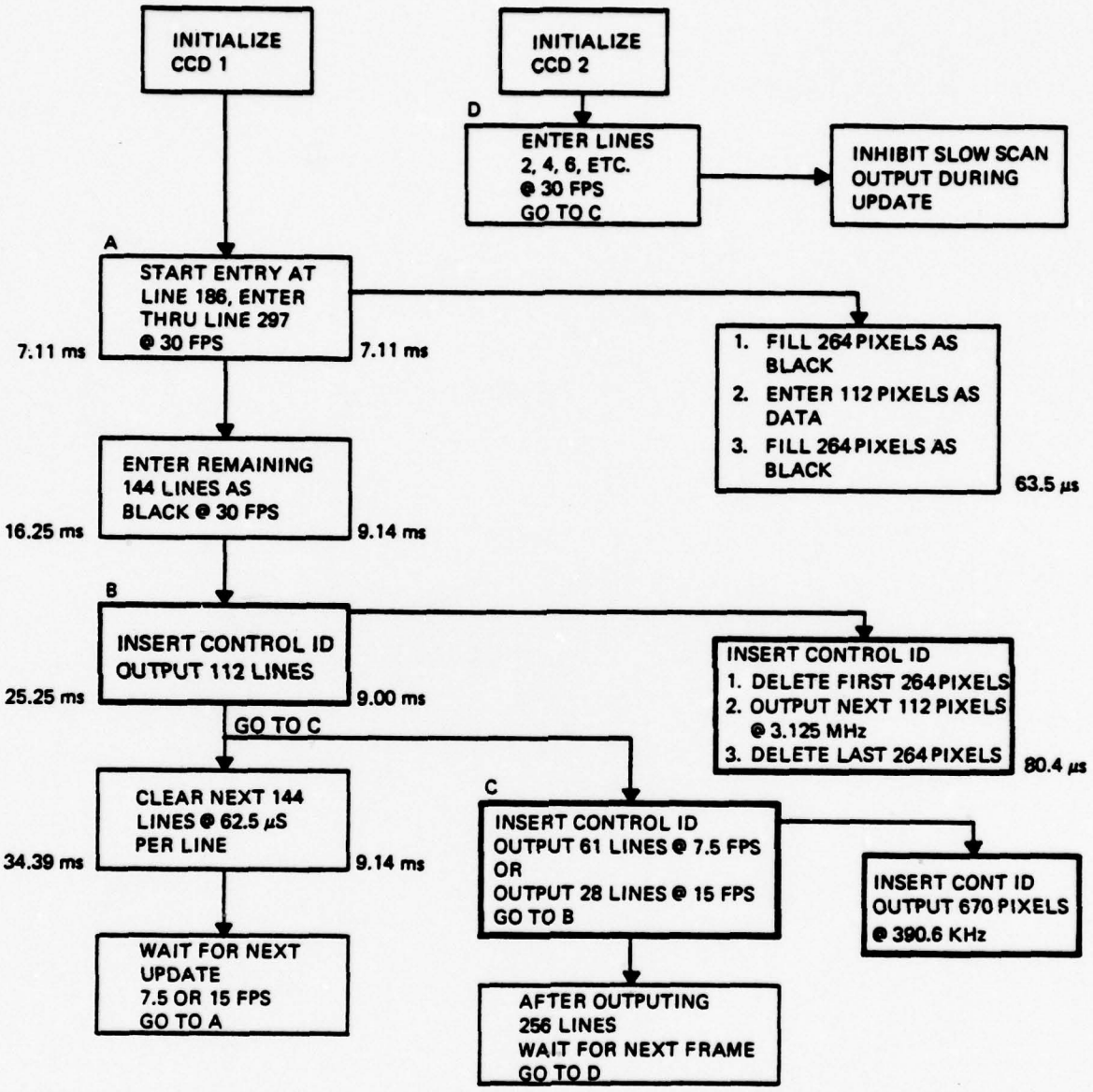



FIGURE 3-8. ALGORITHM; DUAL DATA RATE, NON-INTERLACED

The number of lines transmitted per cycle is

$$\#\text{Lines/Cycle} = \frac{\text{T Cycle}}{\text{T Line}} \qquad \text{(EQ 2)}$$

Where $T_{line}$ is the time required to output one line at .938 FPS. Substituting the above in EQ 2 we have

$$\#\text{ Lines/Cycles} = \frac{124.32}{2.022} = 61.47$$

Using 61 lines, the number of cycles for 256 lines is:

$$\#\text{ Cycles} = \frac{256}{61} = 4.19 \text{ Cycles}$$

or the time to output a complete field of slow speed data is:

$$T_s = (\#\text{Lines} \times \#\text{Cycles} \times T_{line}) + (T_{line} \times \text{Overflow}) + \text{Update time} \qquad \text{(EQ 3)}$$

Substituting in EQ 3:

$$T_s = (61 \times 4 \times 2.022) + (2.022 \times 12) + 45$$

$$T_s = 562.63 \text{ msec}$$

The interleaved output is shown in Figure 3-9. With the high speed data rate at 15 FPS, the total time to complete a field at slow speed is:

$$T_s = (28 \times 9 \times 2.022) + (4 \times 2.022) + 90 = 607.5 \text{ msec.}$$

The data received by the IADD is reconstructed into a split screen display with the center 112 lines x 112 pixels being updated at 7.5 or 15 FPS, and the remainder of the display at

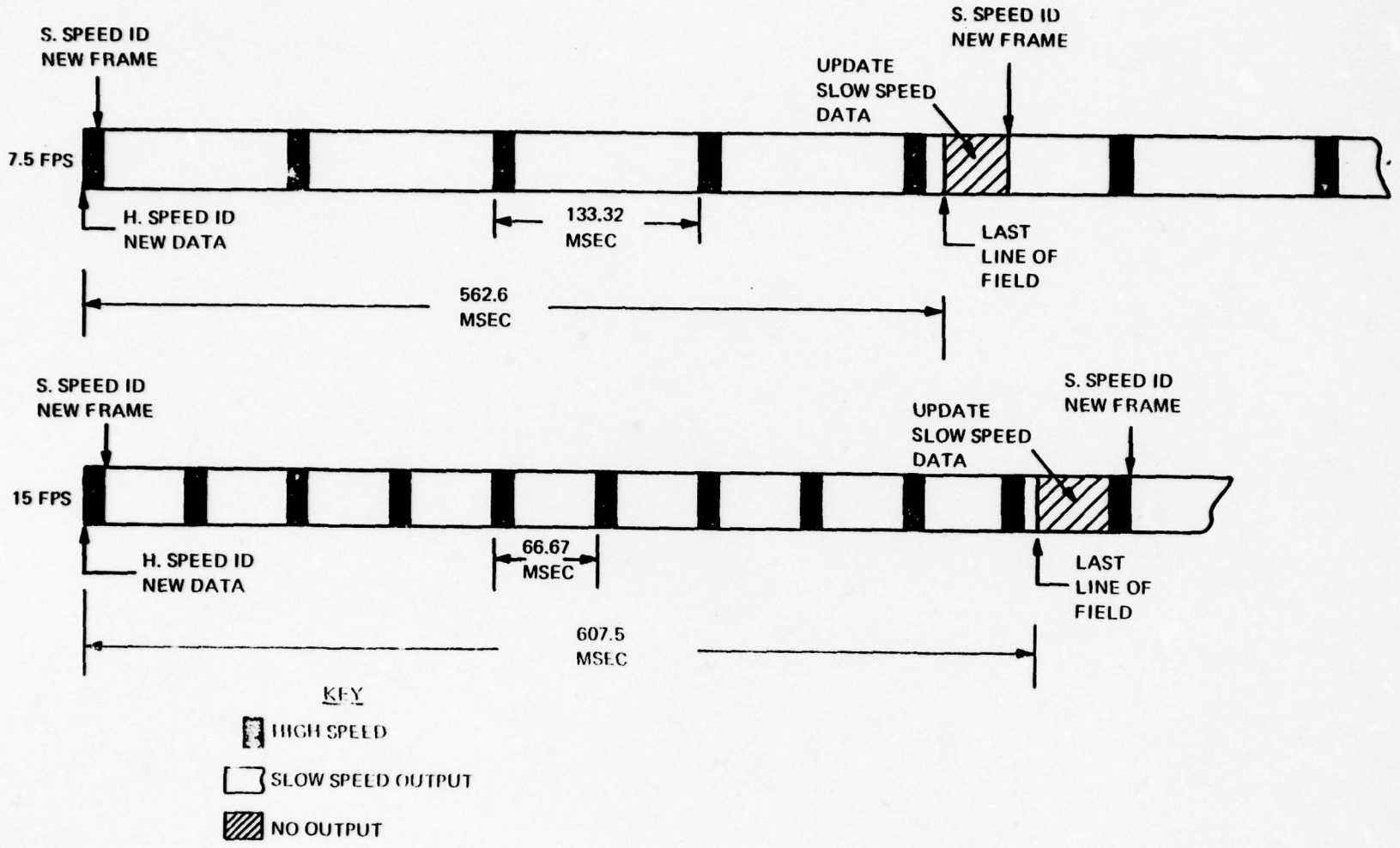



FIGURE 3-9. DUAL DATA RATE OUTPUT

.938 FPS. The horizontal resolution of both sections will be the same while the vertical resolution of the center portion will be greater than that of the outer portion.

## 3.3 IMAGE ANALYZER DIGITAL DISPLAY (IADD)

The function of the IADD is to reconstruct the digital video information received from the Frame Store Memory for display on a standard TV monitor.

The digital video information is received via a simulated transmission data link from the Frame Store Memory at data rates from 0.1 to 7.5 frames per second. All IADD operations (mode, update rate, and interlace format) are controlled by front panel switches. This status information is provided to the Frame Store Memory over the same data link, when the Frame Store is being reloaded.

The IADD memory is required to store 488 lines, 640 pixels per line, with 8 intensity bits per pixel. A memory configuration of 512 x 1024 x 8 will store one frame of data. To provide an uninterrupted display while the memory is being updated requires two full frame memories of storage. While one frame is updated with the latest low speed video information, the other frame is providing the display with 30 frames per second video. Following completion of the low speed update and at the beginning of the next display frame, the memories' roles are reversed providing continuous display. Two additonal partial frame memories are provided for use during mode 3 operation when the center 112 pixels of the center 112 lines are updated at a higher rate than the remaining background data. The two partial frame memories, each consisting of 128 x 128 x 8 bits of storage, provide the same "ping-pong" updating operation as the full frame memories for uninterrupted display of the center area in mode 3 operation.

Refer to Figure 3-10 for the overall block diagram of the IADD. The input data is clocked into the Input Shift Register by the input clock to provide a single 8 bit pixel. The Control Decode detects the control identification codes being transferred (such as start frame, start line, etc.) and also provides synchronization information with respect to the 8 bit pixels. The Pixel Group assembly shift register assembles eight, 8 bit pixels into a single 64 bit word for writing into one of the four frame memories. The memory addressing circuitry sequentially counts through the 80 pixel groups (of 8 pixels each) per line and 488 lines per frame, converting each screen position to a memory address for write-in into one of the four frame memories. The Master Control logic, evaluating the mode/data rate status switches and the control identification decode, selects one of the frame memories. Display readout utilizes equivalent pixel group and line counters to address one of the four frame memories selected for the display mode. The Sync Generator/Output Video Control circuitry generates the timing signals necessary to sequentially read the memory in synchronization with composite sync applied to the video processor. The memory outputs, 64 bits wide each, are tri-state outputs enabling one of the four memories to be presented to the Video Bit Assembly Shift Register as eight pixels. The video shift register sequentially clocks one pixel at a time (8 intensity bits per pixel) to the Digital to Analog Converter for conversion to one of 255 levels of video. The Video Processor mixes this video signal with composite sync and composite blanking to provide the composite video necessary for display on a standard TV monitor. The Video Chop Circuit is enabled in mode 2 only to present the D/A converter with two digital codes per pixel time consisting of the pixel's actual bit weight and then all zeroes; this provides resolution enhancement when coupled with the video acquisition performed by the Frame Store Memory in mode 2.

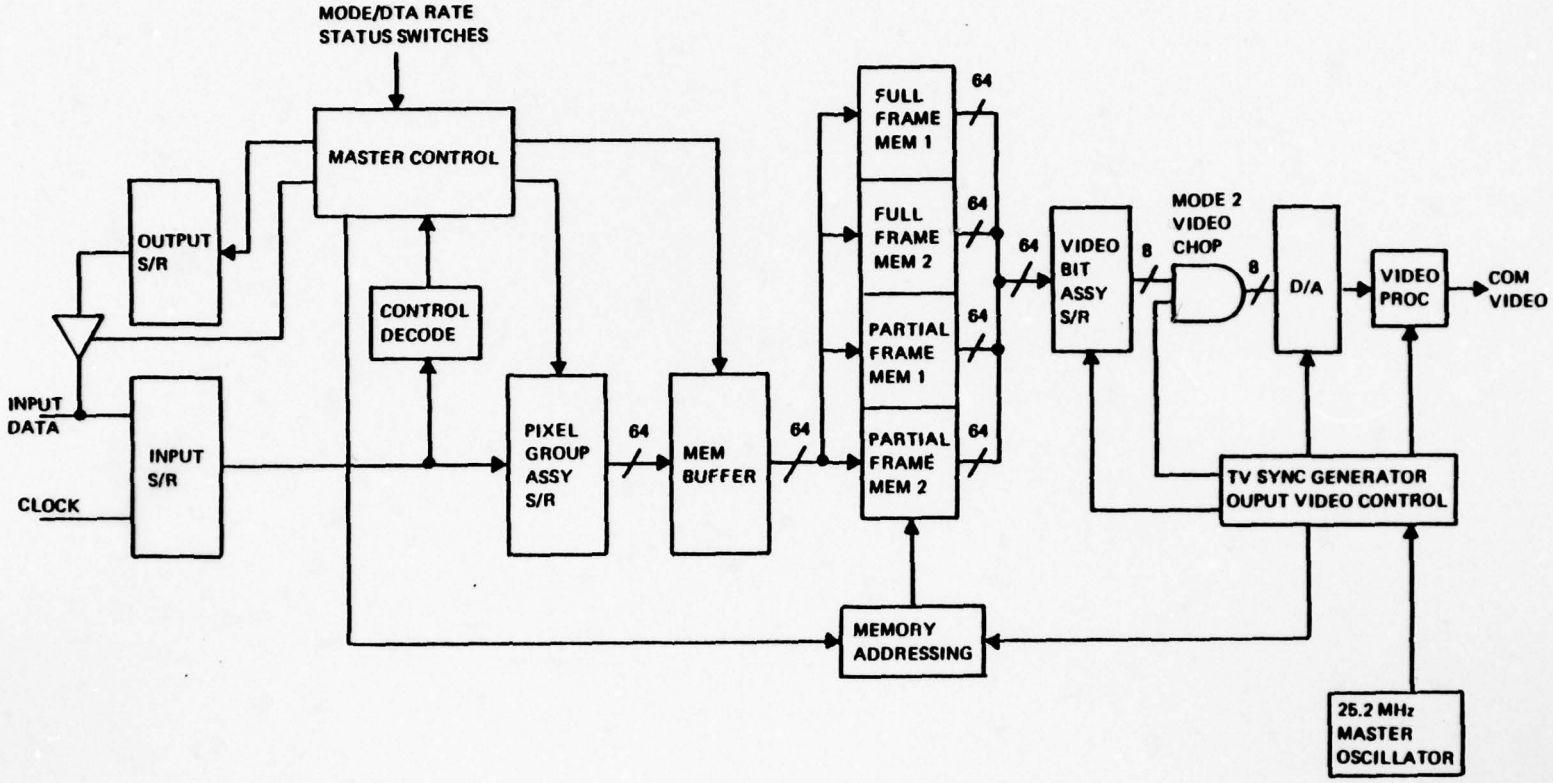



FIGURE 3-10. IADD BLOCK DIAGRAM

### 3.3.1 Input Section

The primary function of the input circuitry is to convert the serial data stream into a 64 bit parallel word for memory write-in. As discussed previously, the speed of the input data ranges from 0.1 to 7.5 frames per second. This corresponds to pixel rate from 47.8KHz to 3.06MHz. However, since there are 8 intensity bits per pixel, the actual data rates range from 382.5KHz to 24.48MHz. Therefore, Shottky TTL devices have been selected for the input shift register and control decode areas to handle the 25MHz data rates.

As an 8 bit pixel appears at the output of the input shift register, each bit is transferred to the input of one of the eight shift registers composing the Pixel Group Assembly Shift Register. This transfer occurs once for every eight input clock cycles enabling the use of low power Shottky technology in this and succeeding stages. Following the filling of all 64 bits of the Pixel Assembly shift register, the Memory Buffer is strobed. Clocked once per 64 input clocks, the clock rate ranges from 6.1KHz to 382.5KHz. This implies a memory cycle time of less than 2.56 microseconds - well within the 500 nanosecond cycle time of the memories selected.

The control decode sequence involves two steps. First a preamble of sixteen "ones" followed by two "zeroes" must be detected. The first zero following the sixteen ones if the first bit of the eight bit control identification word. As all input data is received in eight bit multiples, this detection provides synchronization for all succeeding pixels until another control code is detected. The control identification will be Start Frame, Start Line, Start Hi Frequency, Start Lo Frequency, or Status Request. The absence of a valid code detection will enable a front panel

fault light to indicate transmission unlock. The combination of this code and the front panel switch information provides all the data required for the Master Control Logic to enter the eight pixels in the correct address of the correct memory.

Decoding the "Status Request" code indicates to the IADD that the Frame Store Memory is about to go "OFF LINE" on the data line while still providing a clock signal. The Master Control will then enable its own tri-state data driver and shift out the mode/data rate status of the front panel switches to the Frame Store Memory. The clock frequency during this transfer will be 1.56MHz (slow enough to prevent errors due to clock/data skew arising from unequal delays). This sequence will occur only during normally "dead" time for the link, i.e., when the Frame Store Memory is reloading. Figure 3-11 illustrates the control identification codes to be used.

### 3.3.2 Memory Subsystem

The Memory System consists of two full frame dynamic random access memories and two partial frame static random access memories. Each of the four memories is completely independent with separate read/write controls and addressing logic. Two full frames of storage are required to provide an uninterrupted display while asynchronously receiving a new frame of data. In addition, during mode 3 operation only, the center, 112 pixels of the center 112 lines are stored in the two partial frame memories with one frame serving as the display memory while the other partial frame serves as the update memory.

The 30 frame per second display refreshing imposes a 12.6MHz video update rate upon the memories. This would correspond to a memory read cycle time of 80 nanoseconds. By reading 8 pixels of video simultaneously, the cycle time can be increased to 640 nanoseconds - a realistic time for commercially available memory systems. 8 pixels

| INPUTS | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| START FRAME |
|---|
| START LINE |
| START HI FREQ. |
| START LO FREQ. |
| STATUS REQUEST |

| OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|
| O | $M_1$ | $M_0$ | $D_2$ | $D_1$ | $D_0$ | I | H |

SWITCH STATUS
(Explained below)

| MODE | $M_1$ | $M_0$ | DATA RATE | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | .117 FPS | 0 | 0 | 0 |
| 2 | 1 | 0 | .469 FPS | 0 | 0 | 1 |
| 3 | 1 | 1 | .938 FPS | 0 | 1 | 0 |
| | | | 1.88 FPS | 0 | 1 | 1 |
| INTERLACE | | I | 3.75 FPS | 1 | 0 | 0 |
| NON-INTERLACED | | 0 | 7.5 FPS | 1 | 0 | 1 |
| INTERLACED | | 1 | | | | |

| HI-SPD DTA RATE | H |
|---|---|
| 7.5 FPS | 0 |
| 15 FPS | 1 |

FIGURE 3-11 CONTROL CODES

of video, with 8 intensity bits per pixel requires 64 bits of data to be read simultaneously from the memory-defining the memory architecture as 64 bits wide. Each TV line containing 640 pixels is organized as 80 pixel-groups (of 8 pixels each). The 8 pixels are loaded into shift registers following each memory read cycle and shifted out at the proper 12.6MHz rate while the memory is operating at 1.56MHz. 488 lines of 80 pixel groups each requires the storage of 39,040 64 bit words per frame. A commercially available memory system of 65,536 words by 64 bits has been selected to fulfill these requirements for each frame of dynamic memory.

Four printed circuit boards of 65K by 16 each will provide the desired one frame storage. Each board is composed of sixty-four 16,384 bit dynamic RAM devices. Four additional boards of buffering and control are required to complete one frame of storage. Two full frames of 8 boards each are required.

The partial frame memories require considerably less storage. 112 lines of 14 pixel groups each yields 1,568 64 bit words. Thirty-two static RAM devices (1,024 x 4) will be configured to provide a partial frame memory of 2,048 by 64. Two partial frame memories, as described above, are required.

The two dynamic full frame memories impose an additonal constraint on operation, a need for period refreshing of the stored data to prevent data loss. 128 memory cycles performed on certain addresses are required within a 2 millisecond period to prevent data loss. The memory controller P.C. board associated with each frame memory contains circuitry to automatically provide one of these memory cycles every 16 microseconds. This function is not possible during display readout as every memory cycle during the active line period (53 microseconds) is utilized. However, normal display readout cycles will also refresh the memory as long as all of the 128 addresses

of all of the memory devices are utilized within a two millisecond period. By proper direction of the address lines to the memory, this mode of refresh would be possible. Another factor to be considered is the time period during vertical retrace (approximately 13 milliseconds) and in mode 3 during the center 112 lines when the memory is not being accessed. Switching to the automatic refresh mode during these time periods is not practical because the refresh address counter of the memory controller would not be synchronized with the display readout address. This condition could leave a gap of greater than 2 milliseconds between refreshes during the transition periods to and from automatic refresh.

A solution compatible with all modes of operation which has been selected involves no dependence upon normal read or write cycles to provide refreshing. Instead the TV Sync-Generator circuitry will provide refresh requests during the horizontal retrace time (a 10 microsecond period where no memory cycles are required). This refresh will continue through vertical retrace. The memory controller will provide the refresh address for this mode. Then when the frame memory is switched from display readout to frame update mode, the refresh mode can switch to automatic (using the same refresh address counter) without any refresh gaps. The automatic mode is allowed during frame update because successive memory cycles are not necessary (one write cycle every 2.56 microseconds is the fastest update rate).

The three modes of operation present various requirements to the memories' operation. Mode 1 and 2 are indistinguishable to the memories, the video of mode 2 is "chopped" following memory readout. The input data of modes 1 and 2 consists of 488 lines of pixel groups (640 pixels) per line in either interlaced or non-interlaced format. One write-in counter ( composed of a modulo 80 pixel group counter, modulo 244 field line counter, and field flip/flop) is used for both full frame memories; the frame memory being updated has the write-in counters multiplexed onto its

address lines. Non-interlaced input involves interchanging the field flip/flop with the l.s.b. of the field line counter. One read out counter (with an identical configuration as the write-in counter) is utilized by all four frame memories. In mode 1 or 2, the frame memory not updated is addressed by the readout counter for readout synchronized with the TV Sync Generator.

Mode 3 operation involves the storage of one field of data (background) in one of the full frame memories, and a partial field of data (center 112 pixels of center 112 lines) received in either interlaced or non-interlaced form stored in one of the partial frame memories. The two data types are received at different update rates with the low speed (1 frame per second) background data being interrupted several times during the field transfer by the high speed (7.5 or 15 frames per second) center area data. This fact necessitates an additional set of write-in counters for the high speed data so that the line number at which the low speed data was interrupted can be maintained for use when that data transfer is resumed. At the start of a display frame, the most recently updated full frame and partial frame memories are selected for readout; if either frame's alternate memory completes a new update following this time, the memories are not switched until the start of the next display frame. The single readout counter (interlaced readout only) will initially be addressed to one of the full frame memories at the start of a field and begin readout or pseudo-readout (in the odd field there is no available data and consequentially all "zeroes" are substituted for memory data) until the center 112 area is decoded. At this time the readout address is directed to the partial frame memory selected at the start of the frame and readout then continues with this memory. Display readouts will continue alternating between these two memories as the center area is traversed. Following the center 112 lines, control and addressing will revert back to the full frame memory for the

remainder of the field. The partial frame memory will not actually see the same address as the full frame memory, but will instead pass through a subtraction circuit (pixel group minus 33, and field line minus 94) which compensates for the different memory sizes of the full frame and partial frame memories.

### 3.3.3 Output Logic

The digital representation of the video at the output of the memory consists of 64 bits representing 8 pixels. At the end of each memory cycle all 64 bits are loaded into eight parallel to serial shift registers. During the time the next memory cycle is in process, each of the 8 pixels is individually presented to the Digital to Analog Converter. In modes 1 and 3, the D/A converter is clocked once for each 8 bit pixel (12.6Mhz) with the resulting analog voltage appearing at its output. Mode 2 provides a slight complication to this scheme. In this mode the D/A converter is clocked twice per each pixel output from the shift register. The video chopper sequentially presents the 8 bit pixel and then all "zeroes" (or vice versa) to the D/A converter once per pixel output. The resulting analog video output appears as normal video for one-half the normal pixel time of 80 nanoseconds and is zero for the other half of the normal pixel time. The phasing of the chopped video is reversed on alternate fields to provide enhanced resolution. The Digital to Analog converter selected must be capable of updating at either 12.5 or 25 MHz, providing a relatively "glitchless" output. A commercally available 30MHz D/A converter with an add-on deglitcher has been selected to perform this function.

### 3.3.4 TV Sync Generator/Master Oscillator

The main component of the TV Sync Generator is a CMOS LSI TV sync generator integrated circuit. Clocked by 504KHz (obtained by a synchronous countdown of the Master 25.2MHz oscillator), this I.C.

provides all TV line, field, and frame related signals used in the IADD. Combining these signals with 25.2MHz and its derivatives yields the video, chop, and D/A clocks used in the output area.

### 3.3.5 Video Processor

The video processor passes the D/A converter analog output through a low pass filter prior to mixing the video with composite sync and blanking to produce a composite video output suitable for display on a standard TV monitor.

## 3.4 POWER REQUIREMENTS

### 3.4.1 Analog Frame Store Memory

The operating voltages for the analog frame store memory circuitry will be derived from commercially available power supply modules operating off 115V, 60Hz laboratory power.

The A/D converter will be powered by a separate dedicated power module. The power to the TE coolers will be derived from a separate dedicated power module.

### 3.4.2 IADD

The power supplies selected for the IADD will be standard commercially available computer grade supplies operating off the laboratory 115VAC, 60Hz line.

The two full frame dynamic memories require +12V, +5V, and -5V at currents under 13, 33 and 1 Amp, respectively. Additionally, a power-on sequence and failure control will not enable the +12V and +5V supplies without the presence of the -5V (VBB) supply.

The two static partial frame memories require +5V at approximately 6 Amps. The remaining TTL logic circuitry requires +5V at approximately 8 Amps. The D/A converter requires +15V, -15V, +5V, and -5.2V at currents under 150ma., 250ma., 30ma., and 100 ma., respectively.

## 3.5 PACKAGING

### 3.5.1 Analog Field Storage Device

The Analog Field Storage Device will be packaged in a hermetic DIP as illustrated in Figure 3-12. This arrangement provides the flexibility for both cooling and ease of handling in uncooled breadboards. The device pinouts and their associated functions are listed in Table 3-2.

For breadboard use, the top brazed pins are bent over to form a standard dip package. For cooled applications, these pins are cut back and wire bonds attached. In this way, there is no cooling losses through the pins.

### 3.5.2 Analog Frame Store Memory

The Analog Frame Store Memory electronic components, A/D converter, connectors, associated harness, and the field storage devices are contained in the electronics enclosure detailed in Figure 3-13. The circuitry is mounted on five plug-in circuit cards. The logic cards are standard wire wrapped boards and the processing circuit card are vector boards with the same outline dimensions. The A/D converter is hard mounted to the chassis.

Each analog field storage device is contained in a sealed plug-in assembly containing a thermoelectric cooler. The storage device is mounted to the TE cooler. The module will plug into a receptacle

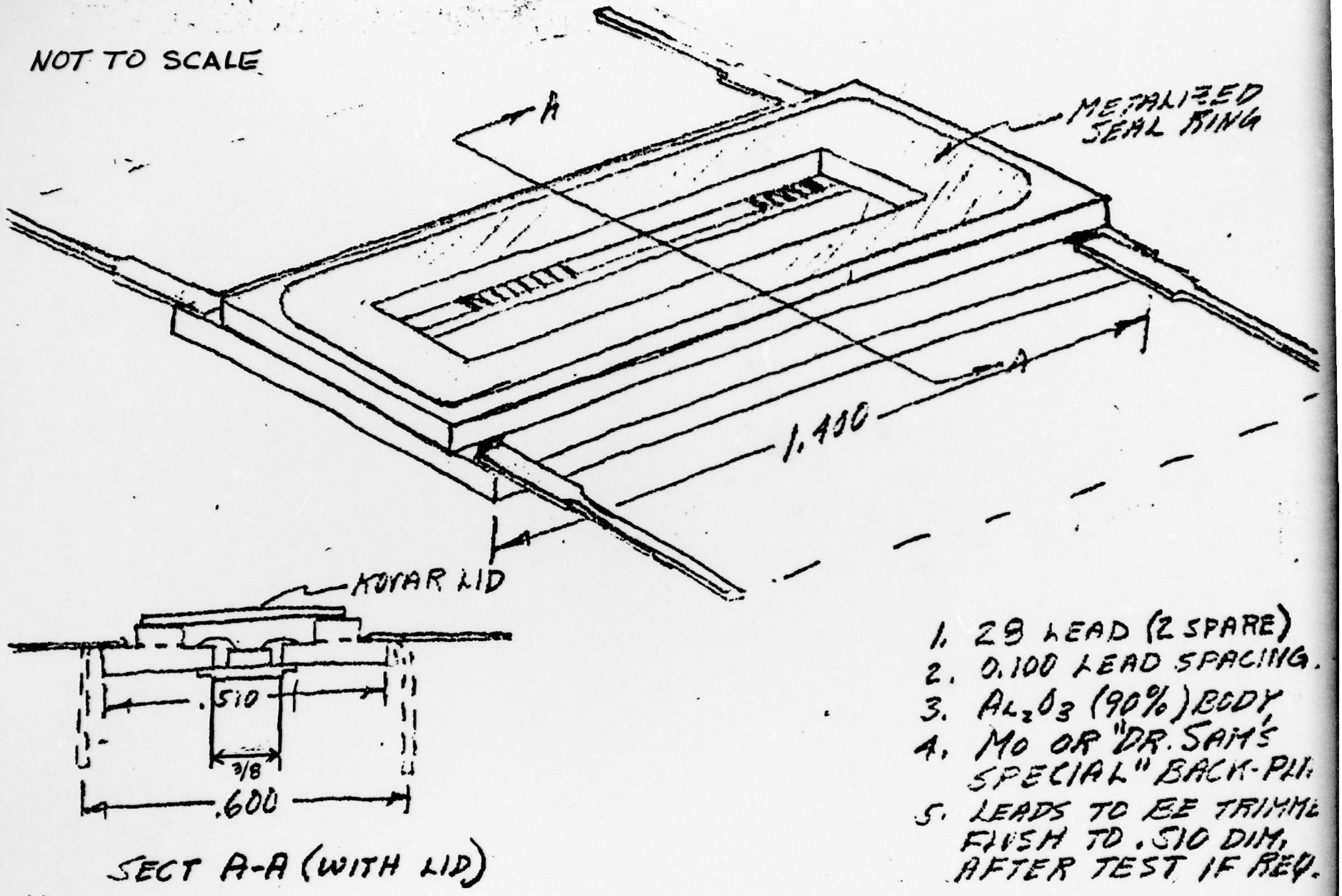



FIG. 3-12 PROPOSED PACKAGE (CONCEPTUAL)

TABLE 3-2

## FIELD STORAGE DEVICE

## PINOUTS

| | | |
|---|---|---|
| 1. | $V_{SS}$ | SUBSTRATE GROUND |
| 2. | $\phi_{3IN}$ | $\phi_3$ GATE |
| 3. | $\phi_{3OUT}$ | $\phi_3$ CLOCK |
| 4. | $\phi_{4IN}$ | $\phi_4$ GATE |
| 5. | $\phi_{4OUT}$ | $\phi_4$ CLOCK |
| 6. | $\overline{X}$ | TTL CLOCK TO BE SUPPLIED |
| 7. | $V_{CD2}$ | 12V |
| 8. | $\overline{\phi_{OUT}}$ | TTL CLOCK TO BE SUPPLIED |
| 9. | $\overline{\phi_P}$ | TTL CLOCK TO BE SUPPLIED |
| 10. | SHG | SAMPLE AND HOLD CLOCK GROUND |
| 11. | $\phi_{SH}$ | SAMPLE AND HOLD CLOCK TEST POINT |
| 12. | $V_{OUT}$ | OUTPUT SIGNAL |
| 13. | $V_{CG}$ | CLOCK GROUND |
| 14. | $V_{SG}$ | SIGNAL GROUND |
| 15. | $V_{OTEST}$ | TEST OUTPUT |
| 16. | $V_{DD}$ | 14V |
| 17. | OG | OUTPUT GATE BIAS |
| 18. | $V_{CD1}$ | 5V |
| 19. | $\overline{\phi_{IN}}$ | TTL CLOCK TO BE SUPPLIED |
| 20. | $\overline{\phi_P}$ | TTL CLOCK TO BE SUPPLIED |
| 21. | $\phi_2$ | MOS CLOCK TO BE SUPPLIED |
| 22. | $\phi_1$ | MOS CLOCK TO BE SUPPLIED |
| 23. | $V_R$ | INPUT REFERENCE VOTLAGE |
| 24. | $V_1$ | INPUT SIGNAL |

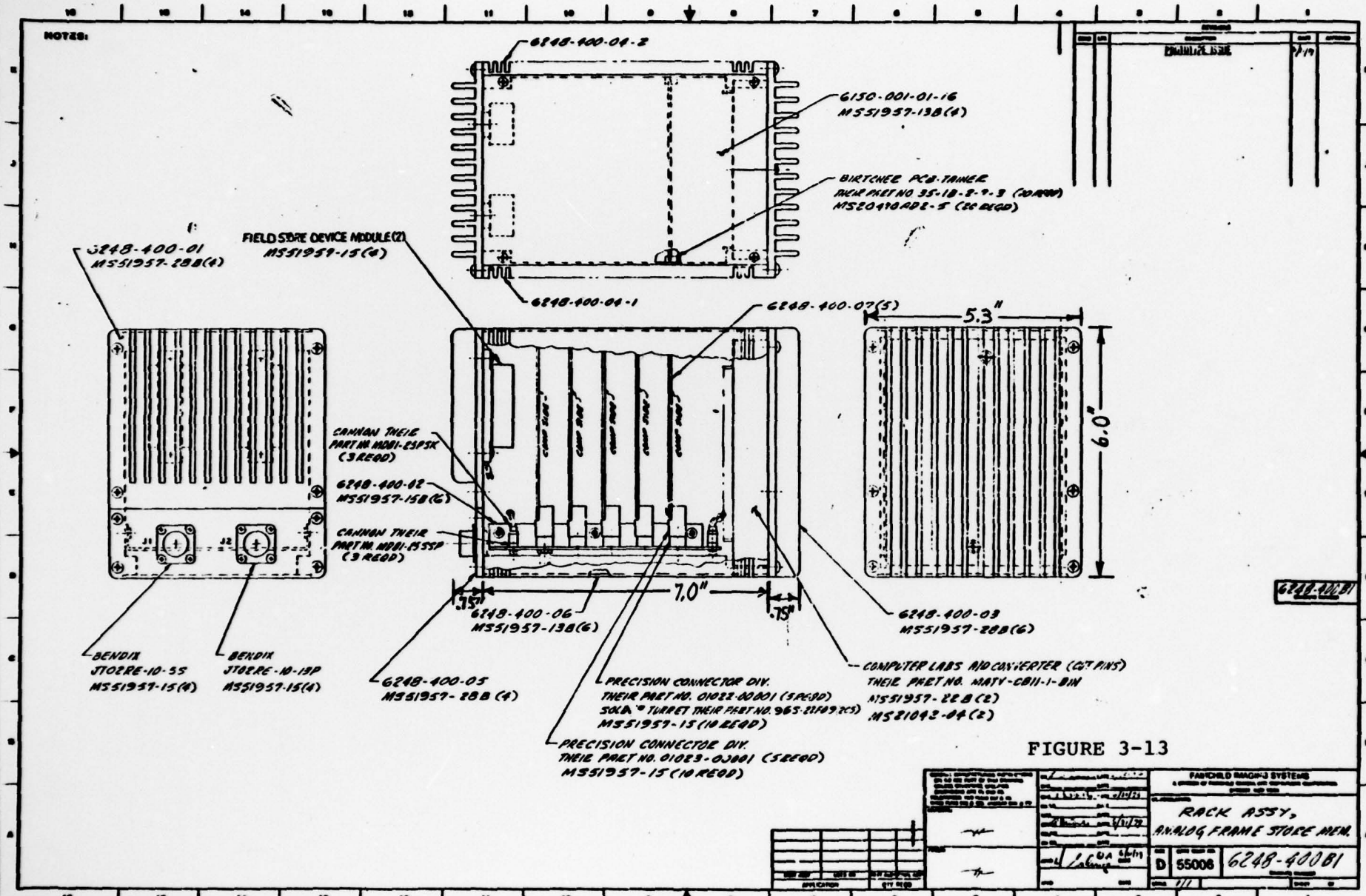

NOTES:
6248-400-04-2
6130-001-01-16
MS51957-138(4)
BIRTCHER PCB-TAINER
THEIR PART NO 35-18-2-9-3 (20 REQD)
MS20410AD2-5 (20 REQD)
FIELD STORE DEVICE MODULE (7)
MS51959-15(4)
6248-400-01
MS51957-28B(4)
6248-400-04-1
6248-400-07(5)
5.3"
6.0"
CANNON THEIR
PART NO MDBI-E9PSK
(3 REQD)
6248-400-02
MS51957-158(6)
CANNON THEIR
PART NO MDBI-F9SP
(3 REQD)
7.0"
.75"
.75"
6248-400-06
MS51957-138(6)
6248-400-03
MS51957-28B(6)
BENDIX
JTO2RE-10-5S
MS51957-15(4)
BENDIX
JTO2RE-10-19P
MS51957-15(4)
6248-400-05
MS51957-28B (4)
PRECISION CONNECTOR DIV.
THEIR PART NO. 01022-00001 (3 REQD)
SOLDA "O" TURRET THEIR PART NO. 965-22F09.2C5)
MS51957-15 (10 REQD)
COMPUTER LABS A/D CONVERTER (64 PINS)
THEIR PART NO. MATY-CB11-1-BIN
MS51957-22B(2)
MS81042-04(2)
PRECISION CONNECTOR DIV.
THEIR PART NO. 01023-03001 (5 REQD)
MS51957-15 (10 REQD)
FAIRCHILD WEAPON SYSTEMS
RACK ASSY,
A.V. ANALOG FRAME STORE MEM.
D
55006
6248-400B1

FIGURE 3-13

at the rear of the enclosure bringing it into contact with an externally mounted heat sink. To minimize the heat rise in the unit, power supplies for the Analog Frame Store Memory will be contained in a separate enclosure.

### 3.5.3 IADD

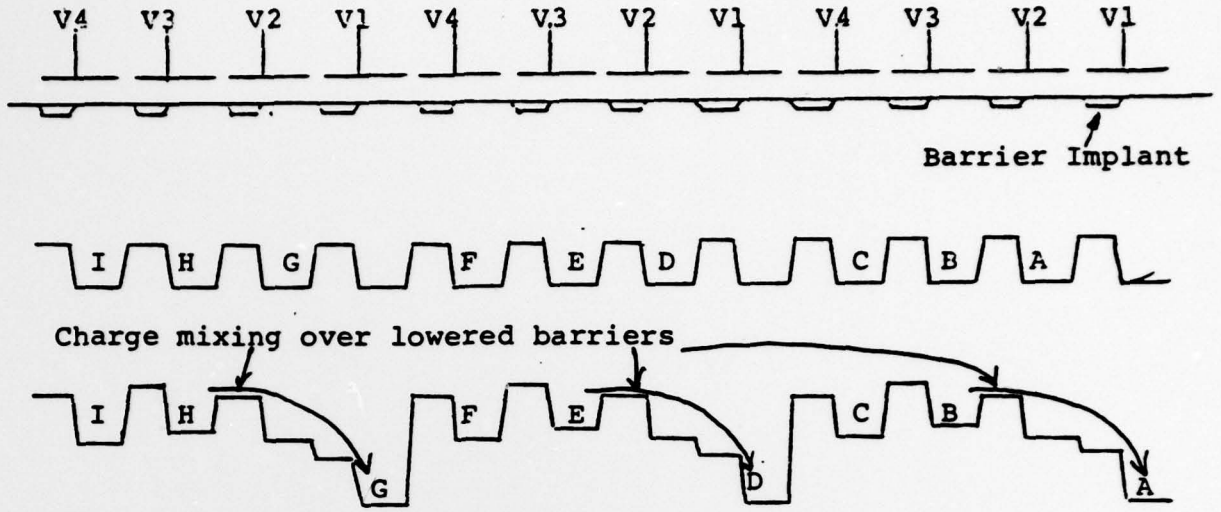
The IADD electronics is contained in a 42 x 19 inch equipment rack. The main power supplies are positioned at the bottom of the rack and are provided with fan cooling. The control panel is situated in the rack at average "eye ball" level. It contains the master ON/OFF controls, several status lamps, the mode select switch and frame rate select switch. A 33 position card assembly positioned in the equipment rack contains all of the IADD circuitry. The dynamic full frame memory system occupies 16 positions, the static partial frame memories occupy 2 positions, and the remaining circuitry occupies 4 positions. The dynamic memory system is composed of printed circuit boards while all other functions are implemented with wire-wrap or vector board conforming to the dimensions of the card assembly.

# APPENDIX 1

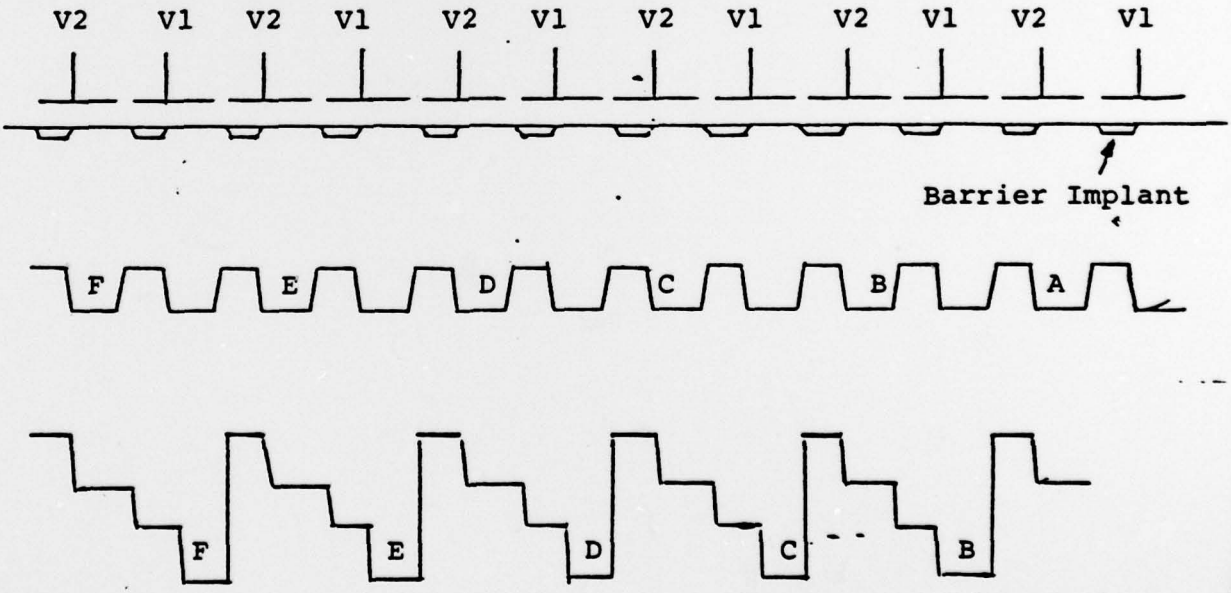
## CHARGE SPILLAGE IN A FOUR PHASE SYSTEM

In a four phase clocking scheme, charge is stored under adjacent gates. Any coupling between a gate, whose voltage is high, and the adjacent gates, whose voltages are low, could cause signal charges to mix, as illustrated in Figure A-1.

When $V_1$ goes high, the wells under $V_1$ drop, collecting charges D and G as they should. However, the wells under $V_2$ drop slightly due to the coupling effect. This causes some of charge E to mix with D, and H to mix with G. In the two phase scheme charge is stored under alternate gates so this problem does not arise.




4 PHASE RIPPLE CLOCKS




2 PHASE CLOCKS

FIGURE A1-1 CLOCKING SCHEMES

## APPENDIX 2

## DESCRIPTION OF BURIED-TO-SURFACE CHANNEL TRANSFER REGION IN FIELD STORAGE DEVICE

In the design of the field storage device, a strip of n+ diffusion (see Figure 1) is positioned between the buried channel and surface channel areas. This n+ area acts as a conductor between the buried and surface channel regions. Both the buried and surface channel implants overlap the n+ strip to allow for alignment tolerances. This overlap assures us that there will be no small potential wells at the interface where signal charge may be trapped.

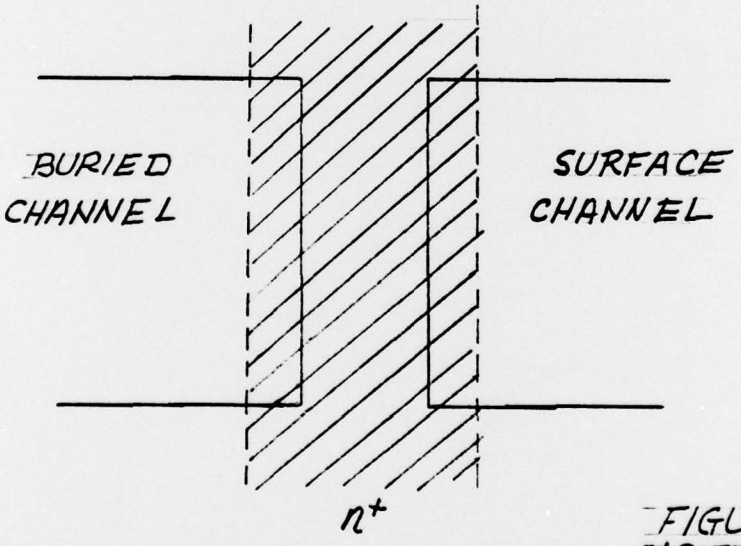
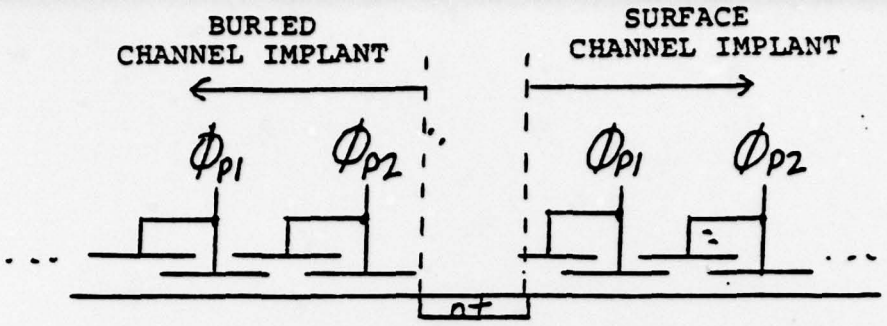



FIGURE A2-1
n+ DIFFUSION DIAGRAM

Signal charge transfer across the n+ strip is shown by the potential well diagrams of Figure 2. The shaded areas show the level to which the wells are filled. Originally the charge is distributed as shown in Figure 2A. All voltages then go low as shown in Figure 2B. The Ø P2 clocks then go high. The charge Q stored in the n+ area, between the barrier level in the surface channel and the well level in the buried channel, mixes with signal

chargeB, spreading over the n+ area and the well of the last P2 gate before the n+ area (Figure 2C). All clocks then go low, dumping the mixed charge into the n+ area. The n+ area is now filled above the barrier level in the surface channel by an amount corresponding to the signal charge B. All charge in the n+ area above the barrier level of the surface channel is signal charge B, (Figure 2D); therefore, when Ø P1 goes high, signal charge B and only B moves into the first P1 gate past the n+ region (Figure 2E). Signal charge B has been transferred past the n+ strip, without gain or loss of charge, and we have the situation we started with in Figure 2A.

A similar scheme is used at the surface to buried channel interface.



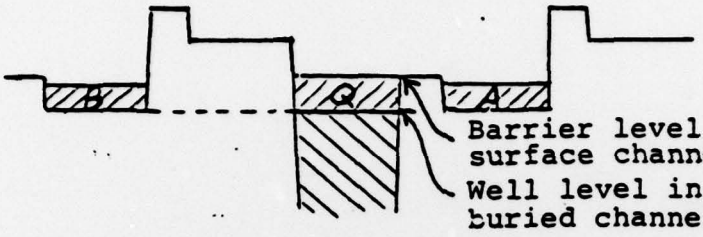




FIGURE 2A

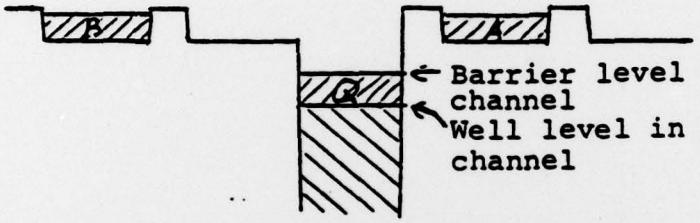



FIGURE 2B

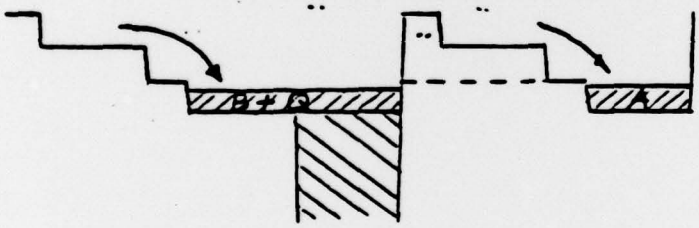



FIGURE 2C

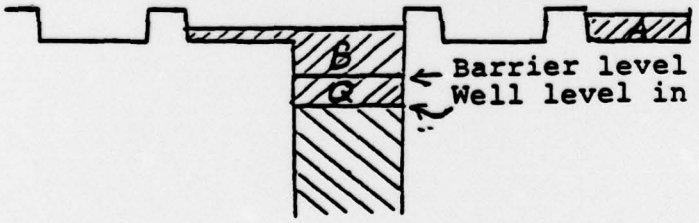



FIGURE 2D

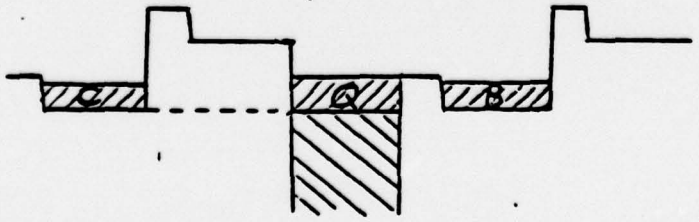



FIGURE 2E

F I G U R E A2-2 WELL DIAGRAM