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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL OXIDE SEMICONDUCTOR DEVICES

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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

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The current papers describe the use of a graded insulator to facilitate characterization in charge storage devices, the annealing of radiation induced positive charge, a comprehensive treatment of electron trapping and detrapping in As implanted SiO_2, characterization of the electron traps in SiO_2 as influenced by processing procedures, and a study of hole trapping in the bulk of ion implanted SiO_2.

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INTRODUCTION

Trapping of charge in SiO_2 can lead to changes in the characteristics of Si devices that limit the useful life expectancy of the device; however, traps in the SiO_2 can also be used beneficially to provide new device structures. We are continuing to investigate both of these aspects. The work done on this contract has provided a background of information that enables us to vary the trapping probability of an electron flowing through the SiO_2 from 10^{-6} to 1 at will. We are also addressing the equally important problem that is concerned with various mechanisms for releasing the trapped electrons (discussed in the paper by DeKeersmaecker and DiMaria). The papers included in this report cover all these points. We are also investigating new device structures that include a graded insulator at the SiO_2–gate interface. The grading of the insulator at this interface enables us to inject charge (either holes or electrons) at a reduced electric field from the gate. This charge can be used to charge and discharge "floating gate structures" which results in an improved device for electrically-alterable read-only store applications. Preliminary work on these structures has yielded promising results and a paper by DiMaria is included, describing this work.

Radiation damage effects associated with the radiations used for the construction of modern-high density circuits are of increasing concern. One aspect of this is a recent observation that annealing is more difficult with a poly silicon gate structure than with aluminum gate structures. This is discussed in the paper by Aitken.

Presentations made during this period are as follows:

11/30/78-12/2/78	D.J. DiMaria, D.R. Young, R.F. DeKeersmaecker, and D.W. Ormond, "Novel Uses of Charge Trapping Layers in MOS Structures" at the Semiconductor Interface Specialists Conference, Miami, Florida.
1/ 5/79	D.R. Young, "Electron Trapping in SiO_2" at Lehigh University.
1/11/79	D.R. Young, "Electron Trapping in SiO_2" at Hanscomb Air Force Base.
3/ 6/79	D.R. Young, "Electron Trapping in SiO_2" at Yale University.

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Papers published:

1. Light Activated Storage Device (LASD), D.J. DiMaria, R.F. DeKeersmaecker, D.R. Young, *J. Appl. Phys.* **49**, 4655 (1978).

2. Centroid Location of Implanted Ions in the SiO_2 Layer of MOS Structures using the Photo I-V Technique, D.J. DiMaria, D.R. Young, R.F. DeKeersmaecker, W.R. Hunter and C.M. Serrano, *J. Appl. Phys.* **49**, 5441 (1978).

3. Charge Trapping in Thermal Silicon Dioxide, D.J. DiMaria, *Jap. J. Appl. Phys.* **18**, 3 (1978).

GRADED OR STEPPED ENERGY BAND GAP INSULATOR MIS STRUCTURES (GI-MIS OR SI-MIS)*

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ABSTRACT: A new concept in non-volatile semiconductor memory using graded or stepped energy band gap insulators under the gate electrode of a metal-insulator-semiconductor (MIS) type structure is described. With the graded or stepped insulator, electrons or holes can be injected from the gate electrode at low to moderate applied fields. These carriers then flow under the applied voltage bias into a wide energy band gap insulator (such as SiO_2) with a purposely introduced charge trapping layer (such as ion implanted As, deposited W, or deposited polycrystalline Si). This trapping layer captures and stores electrons ("write" operation) or holes ("erase" operation) with as close to 100% efficiency as possible. Because of the larger energy barriers at the semiconductor (such as Si) interface with the wide energy band gap insulator (such as SiO_2), few carriers of the opposite sign are injected. Therefore, the substrate Si-SiO_2 interface for instance, can be used strictly for charge sensing ("read" operation) such as in a field effect transistor. Several experimental examples are mentioned. A detailed description of stepped insulator structures using thin Si_3N_4 ($\approx$ 5.2 eV band gap) layers on SiO_2 ($\approx$ 9 eV band gap) with an ion implanted As region is given. Some advantages of these structures over other non-volatile semiconductor memory devices are discussed.

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In this communication, a novel type of semiconductor device useful for electrically-alterable read-only memory (EAROM) is described. This device is formed by stepping or grading the energy band gap near the metal gate electrode of a metal-insulator-semiconductor (MIS) structure as shown in Fig. 1. With this type of structure, electrons or holes can be injected from the gate electrode more easily into the insulating layer with less applied voltage. This can be seen in Fig. 2 for negative gate voltage bias (electron injection from the gate) where the average electric field in the bulk of the wide band gap insulator is the same for Figs. 2a, 2b, and 2c. The band bending in the stepped or graded region in Figs. 2 and 3 is indicative of a material with a dielectric constant greater than that of SiO_2. Electron or hole injection from the semiconductor substrate will not simultaneously occur due to the larger energy band gap (see Fig. 1) which those carriers "see" for the same average electric fields that produce injection (via tunneling) from the top gate contact. Using the graded or stepped energy band gap insulator - MIS system (which will be referred to as GI-MIS or SI-MIS from hereon), a non-volatile semiconductor structure can be fabricated which uses the substrate Si-insulator interface strictly for sensing storaged charge ("read" operation) in a purposely introduced charge trapping layer in the wide energy band gap insulator (as shown in Fig. 3). Ion implanted As and P [1-3], deposited W less than a monolayer thick [4-8], and deposited polycrystalline silicon [9-12] can be used for this trapping layer which will capture either injected electrons or holes. The "write" ("erase") operation is achieved by election (hole) injection at low to moderate average electic fields from the gate electrode for negative (positive) voltage bias and the subsequent capture of preferably all injected electrons (holes) in the trapping region. This separation of the interface used for the sensing and the charging operations makes this structure unique compared to other types of non-volatile memory structures, or their variations, such as floating-gate avalanche-injection metal-silicon dioxide-semiconductor (FAMOS) [9] or metal-silicon nitride-silicon dioxide-semiconductor (MNOS) [12] structures. GI-MIS and SI-MIS devices also potentially have other advantages over these EAROM structures. Some of these are the following:

1) Applied voltages are low. Local electric fields at the substrate Si-insulator interface are low and interface state generation should be minimized; therefore, this interface should not deteriorate. MNOS structures are believed to deteriorate with cycling due to high electric fields at the thin, tunnel SiO_2 interface with the Si substrate. Power requirements are low for GI-MIS or SI-MIS structures since large Si currents are not required as for FAMOS operation where avalanche injection from the Si substrate is used to charge traps.

2) Interface state generation or trapped charge build-up at the Si-SiO_2 interface (particularly holes) due to "hot" carrier injection from the Si substrate will not occur. FAMOS structures or their variations have these problems which limit the number of cycles they can be put through.

3) GI-MIS or SI-MIS structures can be electrically "erased" in place in short times with the same type of charge retention as FAMOS devices. Many FAMOS-like structures are difficult to erase and require ultra-violet light and long times (minutes to hours) to photodetrap electrons on the floating gate embedded in the SiO_2 layer [9-12].

One type of experimental structure fabricated to demonstrate GI-MIS or SI-MIS type operation is a variation of an MNOS device. However, unlike the MNOS structures which have a thick Si_3N_4 trapping layer to store charge and a thin tunnel SiO_2 layer of $\approx$ 25 - 30 Å thickness grown on the Si substrate, the SI-MIS devices have thick oxide and thin nitride layers. The thin Si_3N_4 layer (5.2 eV band gap with a low-frequency dielectric constant of 7.5) is used as the electron or hole injecting layer and not as a charge storage layer as in a standard MNOS structure. The energy band diagram for this type of SI-MIS structure is similar to that shown in Figs. 1b and 2b. The "dry" SiO_2 layers (9 eV band gap with a low-frequency dielectric constant of 3.9) in these SI-MIS structures were grown on <100> 2 Ωcm p-type Si substrates at 1000°C in O_2 to thicknesses between 400-1300 Å. The Si_3N_4 layers were chemically vapor deposited (CVD) to thicknesses between 25-600 Å at 810°C with a

NH_3/SiH_4 ratio in the gas phase of 150/1 on top of the SiO_2 layer at a deposition rate of 200 Å/min.

The charge trapping region was formed in the thick SiO_2 layer by ion implanting As prior to the Si_3N_4 deposition. After implantation, a 1000°C anneal in N_2 for 30 min was performed to remove radiation damage [1-3] followed by a 500°C anneal in forming gas (90% nitrogen and 10% hydrogen) for 30 min to reduce surface states at the Si-SiO_2 interface. Finally,the SiO_2 surface was cleaned of metals and hydrocarbons using procedures previously described [1-3,13] followed by Al gate metallization (circular area of .005 cm^2).

Fig. 4 shows the "write" and "erase" operation of one of these SI-MIS structures. This structure consists of a 1350 Å SiO_2 layer and a 300 Å Si_3N_4 layer. An As implant with a fluence of 1×10^{16} ions/cm^2 at an energy of 60 keV was used to form the trapping region for electrons and holes. This heavy fluence was used to insure 100% trapping of injected carriers. Lighter fluences, which were also studied, were not as effective. Gate voltages producing a moderate average field in the SiO_2 of 6 MV/cm for negative polarity (5 MV/cm for positive polarity), neglecting trapped space charge effects in the thin Si_3N_4 layers, were used to inject electrons (holes) which were trapped on As-related sites [1-3]. This moved the high frequency (1 MHz) capacitance-voltage curves to more positive (negative) voltages due to the change in the internal electric fields as sensed by the Si substrate [14,15]. Without the trapping region, no significant charge storage effects were seen under the conditions listed in Fig. 4. The Si_3N_4 layer was kept as thin as possible relative to the oxide layer to minimize trapped space charge effects in this layer which would limit injection efficiencies [16,17].

Scaled-down structures similar to that in Fig. 4 with an oxide thickness of 550 Å and a nitride thickness of 50 Å were also fabricated. The trapping layer for those was formed using a 10 keV implant. This low implantation energy was used to prevent n-type doping with As of the p-type Si substrate. Thinner oxide layers were not possible due to this doping effect, and lower energy implants at fluences of 1×10^{16} ions/cm^2 were also difficult due to the implanta-

tion times involved. Other structures with oxide and nitride thicknesses in the range between the thinnest and thickest were also fabricated. All structures behaved in a fashion similar to those in Fig. 4 for comparable conditions with applied voltage requirements decreasing with insulator thickness.

Some structures without the Si_3N_4 layer but with the 1×10^{16} As ions/cm^2 charge trapping layer were also fabricated. These structures also showed some switching action similar to that in Fig. 4. This was probably due to some grading of the energy band gap as shown in Figs. 1c, 2c, and 3 and/or the introduction of defect or impurity energy levels caused by the implantation into which charge carriers could tunnel from the metal gate electrode before possibly thermalizing or tunneling to the appropriate conduction or valence band. Introduction of defect or impurity energy levels or bands near the gate electrode is another means of getting carriers to tunnel into the insulator at low or moderate applied electric fields and could be used in addition to or instead of grading the band gap.

The SI-MIS structures reported here using ion implanted oxide layers and an injecting layer of smaller energy band gap Si_3N_4 could be cycled fairly reproducibly between the "written" and "erased" states with some small amount of "walk out" of the C-V curves to more positive gate voltages with cycling. Once written, "read perturb" effects at room temperature were fairly low with only a small percentage of trapped electrons being lost or compensated at the low average fields required for actual read operations in a field effect transistor (FET) structure. The thinnest structures could be "written" at a gate voltage of -48 V and "erased" at +38 V in 100 msec.

As seen in Fig. 2, a CI-MIS structure should be a more efficient carrier injector than a SI-MIS structure. A graded band gap can be pictured as a stepped band gap with an infinite number of steps. A more efficient injector using a CVD deposited SiO_2 layer with increasing Si content and therefore decreasing resistivity [18] and probably decreasing energy band gap has recently been fabricated. These structures appear to be very efficient electron injectors

but poor hole injectors. In these structures, $\geq 10^6$ times the electron current and $\simeq 10^2$ times the hole current were observed for the same average electric fields in the thermal SiO_2 layer as compared to structures with the injecting layer absent. They could be "written" in msec at gate voltages of $\leq$ -25 V depending on the thickness of the structure and "erased" in minutes at $\leq$ 25 V. These will be described in detail in future publications.

Possibly the best GI-MIS structure can be achieved using an SiO_2 film graded to Si. This structure should provide extremely efficient electron and hole injection, particularly with a polycrystalline Si gate electrode. With this type of GI-MIS structure, there should be no barrier for either electrons or holes at the polycrystalline Si-graded insulator interface at low to moderate applied fields. The CVD graded films discussed previously can only have a maximum of $\approx$ 10% additional Si content over stoichiometric SiO_2 [18] and therefore are not expected to be graded completely to Si. However, complete grading to Si with CVD systems might be attained at lower temperatures [18] possibly with the assistance of a rf plasma (plasma-enhanced CVD [19,20]).

Other materials to grade the SiO_2 layer to a metal or a poly-Si gate electrode contact with low-frequency dielectric constants equal to or less than that of thermal SiO_2 are desirable. However, the materials discussed here have larger dielectric constants as do most, if not all materials with a decreasing band gap. The graded or stepped insulator could also be put above the Si substrate instead of under the gate electrode; however, the advantages of using separate interfaces for charge sensing and charge injection would be lost. Future research in these areas could possibly yield devices which hold trapped charge in a very stable manner like FAMOS structures but which have very fast switching times in the μsec range due to the nature of the injecting region.

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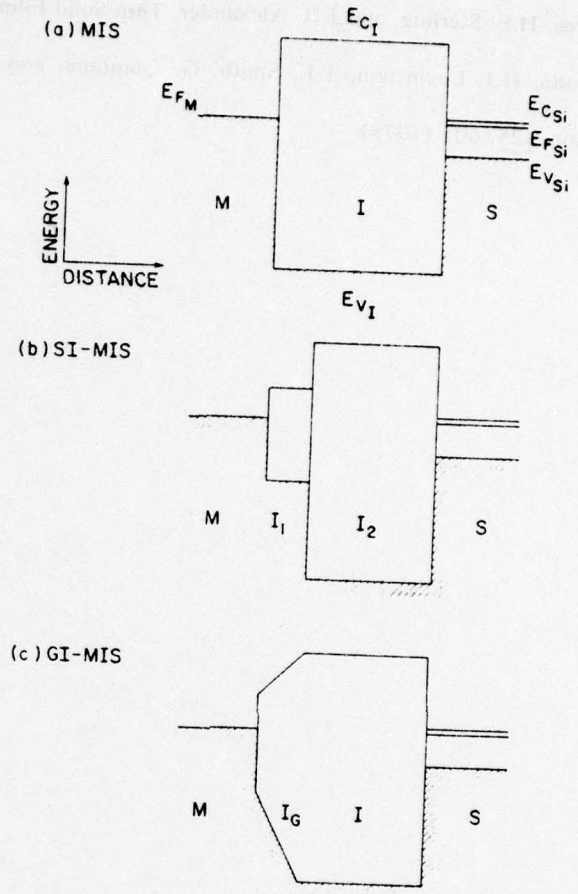


Fig. 1: Zero-field energy band diagram for (a)-MIS, (b)-stepped insulator (SI-MIS), and (c)-graded insulator (GI-MIS) structures.

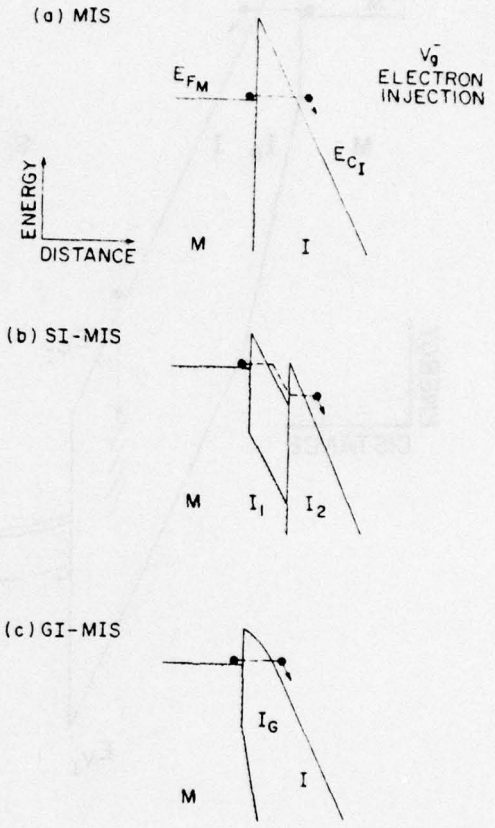


Fig. 2: **Energy band diagram for negative gate bias (electron injection from the gate electrode) for (a)-MIS, (b)-stepped insulator (SI-MIS), and (c)-graded insulator (GI-MIS) structures.**

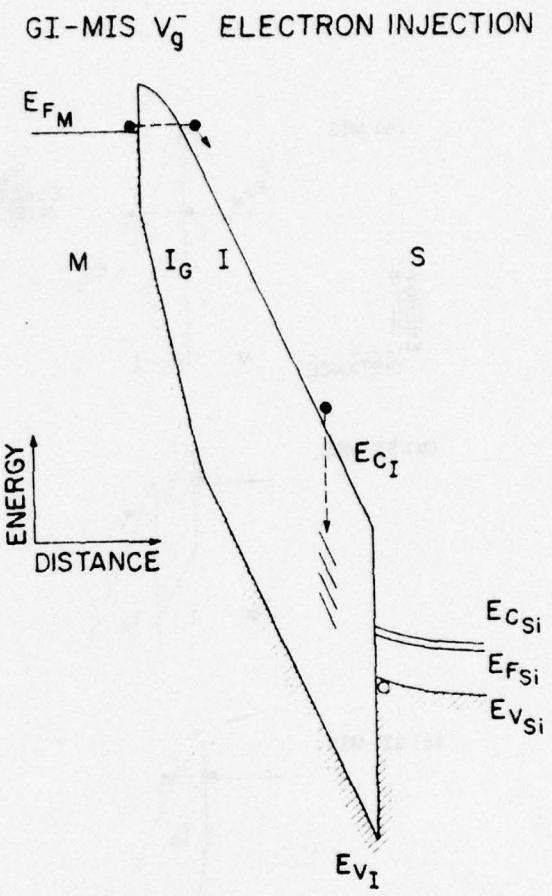


Fig. 3: Energy band diagram for negative gate bias for graded insulator (GI-MIS) structure showing electron injection from the gate electrode and subsequent capture in a purposely introduced charge trapping layer in the bulk of the wide band gap insulator layer near the interface of this layer and the Si substrate.

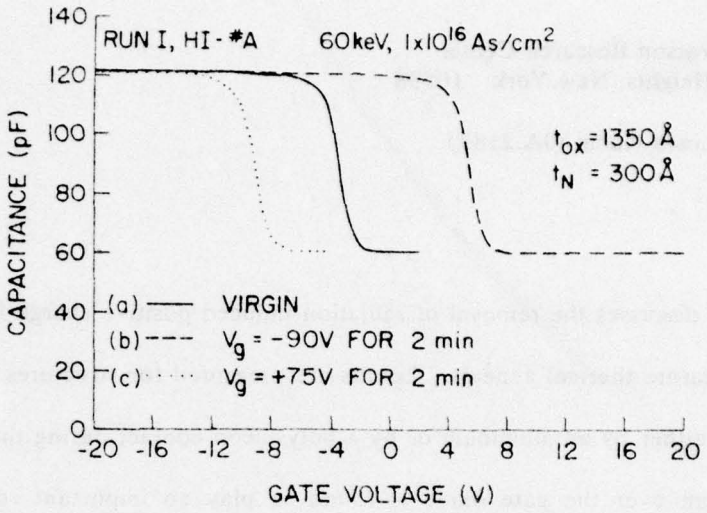


Fig. 4: High frequency (1 MHz) capacitance as a function of gate voltage for a SI-MIS structure with a 1350 Å thermal SiO_2 layer, a 300 Å Si_3N_4 layer, and a 60 keV 1×10^{16} ions/cm^2 implanted As region in the thick SiO_2 layer. (a)-as fabricated virgin SI-MIS, (b)-after stressing for 2 min at a gate voltage of -90 V (electron injection and trapping), and (c)-after stressing for 2 min at a gate voltage of +75 V (hole injection and trapping).

ANNEALING OF RADIATION-INDUCED POSITIVE CHARGE IN MOS DEVICES WITH ALUMINUM AND POLYSILICON GATE CONTACTS

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Abstract

This paper discusses the removal of radiation-induced positive charge from MOS structures by low temperature thermal anneals. Results are presented for structures in which the gate oxide is covered either by an aluminum or by a polysilicon contact during the anneal. The presence of aluminum over the gate oxide is found to play an important role in the annealing of radiation-induced positive charge in these structures . While a 400°C anneal is sufficient to remove this charge from capacitior structures with aluminum gates, it leaves a small amount of residual charge (about $6x10^{10}cm^{-2}$) in structures with polysilicon gates. Anneals at temperatures in excess of 550°C are required to remove this charge completely from the polysilicon-gated MOS devices. However when a thin layer of aluminum is present over the polysilicon contact during the anneal the charge can be removed easily at 400°C. The results in capacitor structures are consistent with those found in polysilicon gate MOSFET's with similar coverage over the gate oxide.

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Introduction

Semiconductor processing environments in which ionizing radiation plays a direct role or appears as a by-product are being used to fabricate the next generation of MOSFET devices. Electron-beam lithography and reactive ion etching, for example, allow the fabrication of dense arrays of small MOSFET's.[1] Ionizing radiation is known to cause a buildup of positive charge and surface states in the oxide layer of MOS devices.[2] Past studies have concentrated on the rate at which these changes occur in optically fabricated devices operating in radiation environments such as outer space[3]. These changes can be removed by subsequent thermal anneals. Because annealing is impractical in such cases , little effort has been made to study it. In processing environments, however, thermal annealing is a practical step and is used routinely to remove the "damage" introduced into the oxide by the ionizing radiation encountered in a particular processing step. Earlier annealing studies have restricted themselves to MOS devices with aluminum gates. In these devices, anneals at 400°C are sufficient to remove both positive charge and surface states[2]. Newer FET technologies make extensive use of polysilicon contacts over the gate oxides. No published data exists for annealing of radiation damage in these structures.

In this paper the annealing of positive charge introduced by ionizing radiation into the gate oxides of MOS devices is studied. Results are presented for MOS devices with both aluminum and polysilicon contacts over the gate oxide. Recently other studies have also identified a neutral electron trap as another constituent of ionization damage[4], the annealing of this center appears independent of contact metallurgy and is not discussed here. Detailed studies of these neutral traps are published elsewhere.[4,5,6]

The motivation for this work was to determine the extent to which positive charge introduced into MOS structures by process-related ionizing radiation is removed by low temperature anneals. Even though polysilicon gate technology is widely practiced in the semiconductor industry and may be used in conjunction with ionizing radiation to fabricate

high density circuits, little information is available on the annealing of radiation-induced positive charge in this technology. Residual positive charge in MOSFET's has two practical consequences which are important to operation of the device. It lowers the threshold voltage of such devices and directly affects the operating conditions. Unannealed charge can also act as an efficient trap for hot-electrons injected into the oxide from the substrate during operation of the device.[5,6] This process aggravates potential instabilities in the operating characteristics of MOSFET's with small channel dimensions[7].

Experimental Details

Both capacitor and FET structures were used in these experiments. Oxide films 35 and 50 nm thick were grown in dry O_2 at 1000°C on p-type substrates. The resistivity of the wafers was 0.1 to 0.2 Ω-cm for the capacitors and 0.5 Ω-cm for the FET's. Such highly-doped material is necessary for the uniform injection of minority carriers at low applied fields.[8,9] Two types of capacitors were formed by covering the oxide with a film of aluminum (MOS) or by a layer of phosphorous-doped polysilicon covered by aluminum (MPOS). After deposition of the aluminum in a resistance-heated evaporation system and definition of the capacitor gate area ($5 \times 10^{-4} cm^2$), the capacitors were annealed for 20 minutes at 400°C in forming gas to reduce the surface state density in the oxide. The capacitors were then exposed to a flux of 25 KV electrons as described later.

Subsequent to irradiation a third type of capacitor was formed from sections of the MPOS wafer by stripping off the aluminum overlying the polysilicon gate contact. This procedure left POS (polysilicon-oxide-silicon) capacitors with the same gate oxide as the MPOS capacitors. The FET's consisted of large area ($5 \times 10^{-4} cm^2$) enclosed devices designed for trapping studies in oxides.[10] The gate oxide was covered by a single polysilicon layer (POS) and was contacted by an aluminum pad in the thick oxide region away from the gate area. In all cases the polysilicon was degenerately doped and was 350 nm thick.

A 25 KV electron beam was used to irradiate the samples. At this energy the beam penetrates the overlying layers of aluminum and polysilicon into the oxide[11]. Because the densities and atomic numbers of aluminum and silicon are so similar, the amount of energy deposited into the oxide film depends to first order only on the total thickness of the aluminum or aluminum/polysilicon contact. For this reason the total thickness of the contact on the MOS or MPOS capacitors was kept constant at 750 nm. A dosage of 20 $\mu C/cm^2$ was used to simulate typical electron beam resist exposures. Since the POS capacitors were formed from the MPOS capacitors after the irradiation step, the oxides themselves and the radiation damage in the oxides is identical in both of these capacitors.

After exposure to the electron beam the samples were annealed. The annealing conditions were identical for the samples with different contact metallurgy. At each annealing step the MOS, MPOS, and POS samples were annealed simultaneously in the same furnace. When forming gas was used in the anneal, it consisted of 90% N_2 and 10% H_2.

The densities of positively charged traps in the oxides were determined at various points in the experiments, i.e., before irradiation, after irradiation, and after anneals designed to reduce the radiation damage. Two methods of measuring the positive charge densities were employed. One was to measure the absolute flat-band voltage or threshold voltage and compare it with that prior to irradiation. The difference between these voltages is proportional to the charge density in the oxide caused by the radiation. However, after annealing the amount of charge present in the oxide is small and difficult to measure by this method. Therefore the densities of positively charged traps were also determined in an independent measurement. In this measurement, hot electrons were injected uniformly from the substrate into the oxide where a small fraction of them are captured by the radiation-induced traps. This measurement is differential by nature and flat-band voltage changes in the range of millivolts can be detected. The resultant shift of flat-band or threshold voltage which occurs is proportional to the total density of positive and neutral traps in the oxide. The rate at which

this shift occurs is related to the cross-section of the trap[6]. The measured cross-section is used to identify that portion of the shift due to positive charge in the oxide. The positive charge density determined from the injection experiments provides a valuable check on the density determined by comparison of absolute flat-band or threshold voltages at the various stages of the experiment. The electron currents through the oxide were generated by avalanche injection techniques in the capacitors[8,9] and by optically-induced hot-electron injection in the FET's.[10] Small currents (2×10^{-8} A-cm^{-2}) were used to fill the traps with large cross-sections and as these saturated the current was gradually raised to populate the remaining traps at an acceptable rate.

Results and Discussion

The annealing of radition induced positive charge in MOS, MPOS, and POS structures is contrasted in Fig. 1. The effective density of positive charge in the oxide is plotted against the time of anneal in forming gas at 400°C. The positive charge density was determined by subtracting the absolute flat-band voltages measured prior to irradiation from those measured after irradiation and anneal. This voltage was converted to a trap density by assuming that this charge resides at the single crystal silicon/SiO_2 interface. Oxide thickness for these samples was 35 nm. The higher density of charge present in the polysilicon gate capacitor before anneal is due to increased sensitivity of the gate oxide to ionizing radiation caused by the additional heat-treatment used to dope the polysilicon gate.[12] The results show that while the radiation-induced positive charge can indeed be removed from MOS or MPOS structures at 400°C, a small amount ($\sim 6\times10^{10}$ cm^{-2}) remains in the POS structures. Note also that the anneal proceeds slower in the MPOS capacitor than in the MOS capacitor but that after 30 minutes the positive charge is removed in both. Similar results are obtained when the samples are annealed in pure hydrogen as illustrated in Fig. 2. Note that while the charge densities reach the same end points after 30 minutes in either forming gas or hydrogen, the approach to the end point is somewhat more rapid when hydrogen is used during the anneal. The key

ingredient to the effectiveness of the anneal appears to be the presence of aluminum over the gate during the anneal. Note however, that the aluminum is still effective in aiding the anneal when separated by 350 nm of polysilicon from the oxide. Aluminum sintering at low temperatures has been long established as a process which reduces surface state densities in aluminum gate devices[13]. The special properties of this metal may be associated with its reactivity or its work function but are not understood. Surface reactions which produce some species effective in annealing could explain the similarity in annealing between the MOS and MPOS case. Aluminum does however penetrate easily through polysilicon films at this temperature[14] so that aluminum reactions at the polysilicon/SiO_2 interface are still possible in the MPOS capacitors.

The data presented in Fig.1 shows the amount of positive charge present in the oxide as a consequence of being irradiated. The charge density present in the oxide before irradiation is too small to determine accurately by subtracting the absolute flat-band voltages. As mentioned earlier, electron injection techniques can measure small amounts of positive charge accurately. Using this technique, the charge density measured in the unirradiated controls is below 1.2×10^{10} cm^{-2}.

Another capacitor structure with 350 nm of CVD oxide between the aluminum and polysilcon (MOPOS) was also examined. Radiation damage in these structures does not readily anneal at 400°C. Apparently, the CVD oxide prevents the diffusion of the active species to the single crystal silicon/gate oxide interface.

The same trends in the effects of aluminum on the annealing process are observed when the residual positive charge present in polysilicon gate capacitors is measured by using electron injection . The capacitors used in this experiment were similar to the MPOS and POS capacitors described earlier. They differed in that their gate oxides were 50 nm thick. In Fig. 3, the results of avalanche injection experiments on three sample from the same wafer are displayed. Two of these samples were exposed in the electron beam and then annealed for 30

minutes in forming gas. Of these two, one had aluminum present over the polysilicon gate during the anneal, the other did not. The third sample was a control not exposed to electron beam.

In Fig. 3, the shift in flat-band voltage which occurs as electrons injected into the oxide become trapped is plotted against the number of electrons passed through the oxide per square centimeter of gate area. The electron capture cross-section and field-dependence of positive charge in SiO_2 is well-established and predicts that at the oxide field present across these samples during injection (1.5 MV/cm), the positive traps will be filled after approximately 1×10^{14} electrons/cm^2 have been injected.[15] After this number of electrons has been injected into the oxide the positive charge is completely annihilated and the capacitor is restored to its zero charge state. As seen in Fig. 3 there is an additional shift in flat-band voltage which occurs as more electrons are injected into the oxide. This shift is due to remnant radiation-induced neutral centers trapping electrons in the oxide. Comparisons of the voltage shifts at $1x10^{14}$ electrons/cm^2 show that the sample annealed without aluminum over the polysilicon gate contains more positive charge than that annealed with aluminum over the polysilicon gate. A small amount of positive charge (about 20 mv) is also present in the unirradiated control. As in Figures 1 and 2, the radiation-induced charge in the sample with aluminum over the polysilicon gate has been significantly reduced by the anneal. The initial flat-band voltages observed in these samples were consistent with the flat-band voltage shifts measured after $1x10^{14}$ electrons/cm^2 had been injected into the oxide. The shifts observed in irradiated samples which were not annealed are at

least an order of magnitude larger than those in Fig. 3 and are consistent with the densities shown in Fig. 1 and 2 for the unannealed oxides.

So far the annealing of radiation-induced positive charge in capacitor structures has been discussed. Polysilicon gate MOSFET's also show residual radiation-induced charge after low temperature anneals. Positive charge generated in the oxide of polysilicon gate MOSFET's by

x-rays generated during evaporation of aluminum in an e-gun system has been studied by Ning[5]. Anneals at temperatures above 550°C are reported to remove this charge completely. Quantitatively similar results on polysilicon gate MOSFET's exposed to electron beam radiation directly are presented here. These devices were fabricated with resistance-heated aluminum and optical lithography, exposed to the electron beam directly and then annealed. The beam energy was 25 KV and the dosage was 20 $\mu C/cm^2$. The effective density of positive charge introduced into the oxide by this treatment was about $7x10^{11}$ cm^{-2}. Table I shows the positive charge density present in the gate oxide following a 30 minute anneal at each of the temperatures indicated in the first column. In these devices also, temperatures above 550°C are required for complete removal of the charge. The difficulty in removing the charge from these MOSFET's arises because of the absence of aluminum directly on the polysilicon gate. Typically the polysilicon gate is covered by 350 nm of CVD oxide and the aluminum contact to the polysilicon is made away from the active gate region.

Summary and Conclusion

In summary, the effectiveness of low temperature anneals in removing radiation-related positive charge from oxides in MOS structures with aluminum and polysilicon contacts has been examined. Earlier conclusions about the removal of radiation damage by thermal anneals have been shown incomplete. Studies of polysilicon and aluminum gate structures show the important but still unexplained role played by aluminum in annealing of positive charge. Thermal anneals at temperatures in excess of 550°C are required to remove radiation-related positive charge completely from oxides underlying polysilicon gates.

The technological implications of these results are not obvious and require a few comments. As mentioned earlier, threshold control and stability in polysilicon gate MOSFET's are related to residual charge and are an important concern in device design. The most ideal situation is one in which all positive charge introduced by ionizing radiation in the course of processing is removed completely by thermal anneals prior to operation of the device. The

evidence presented so far shows that temperatures in excess of 550°C are required to do this. Such anneals are feasible at all processing steps prior to deposition of the final aluminum contact metallurgy. After aluminum is deposited into the contact holes , however, anneal temperatures are limited by the penetration of aluminum into the silicon junctions.[16] The upper limit for this temperature runs from 400°C for pure aluminum to 500°C for aluminum saturated with silicon. Since anneal temperatures are limited after metallization, process sequences which subject the MOSFET to ionizing radiation after deposition of aluminum contact metallurgy are the most critical.

The residual damage present in the device after such an anneal does not preclude the use of processes such as electron-beam lithography for manufacturing high speed circuitry. Two recent papers deal with radiation damage and hot-electron instabilities in 1μ channel length MOSFET's fabricated with electron-beam lithography[17,18]. While some residual charge is shown to be present in these devices after low temperature post-metal anneals, the impact of this damage on device thresholds and stability is within acceptable limits. However some constraints on the possible operating voltages are required to guarantee the long-term stability of the device.

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Table I

ANNEALING OF RADIATION INDUCED[a]
POSITIVE CHARGE IN POLYSILICON GATE MOSFET'S

ANNEAL[b] TEMPERATURES (°C)	REMNANT POSITIVE[b] CHARGE DENSITY (CM^{-2})
400	1.8×10^{11}
400,450	1.1×10^{11}
400, 450, 500	0.7×10^{11}
400, 450, 500, 550	0.4×10^{11}

[a] Dosage $20\mu C/cm^2$ at 25 KV.

[b] Forming gas

[c] Oxide Thickness 35 nm.

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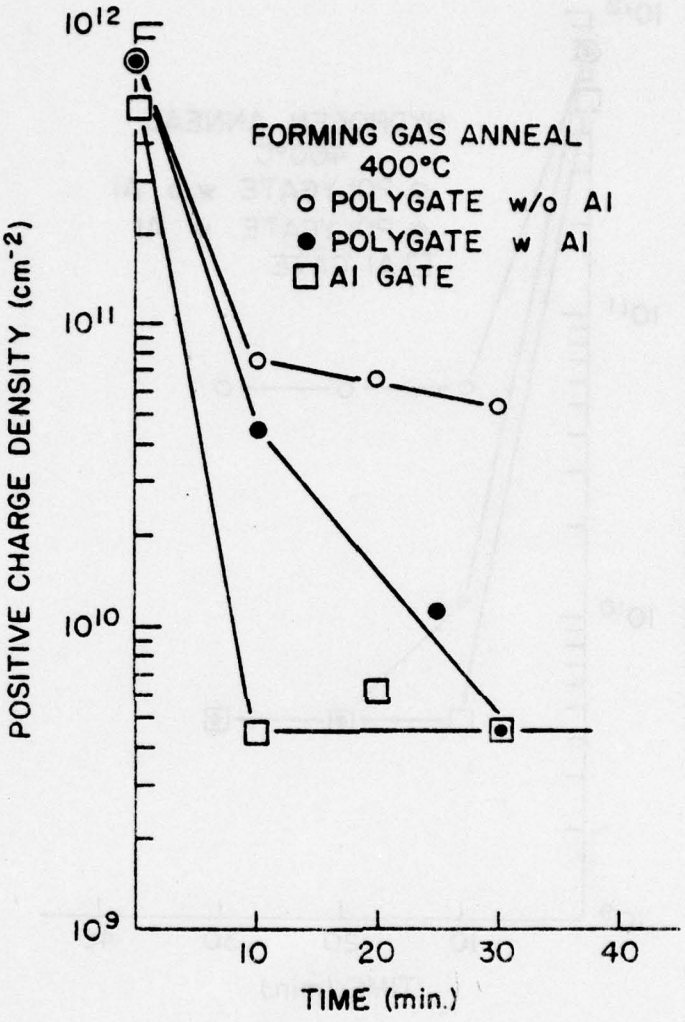


Fig. 1 **Removal of radiation-induced positive charge from capacitor structures with the indicated contact metallurgies in place over the gate during the anneal. The total effective density of positive charge remaining after an anneal step at 400°C in forming gas is plotted against the anneal time. The oxides were 35.0 nm thick.**

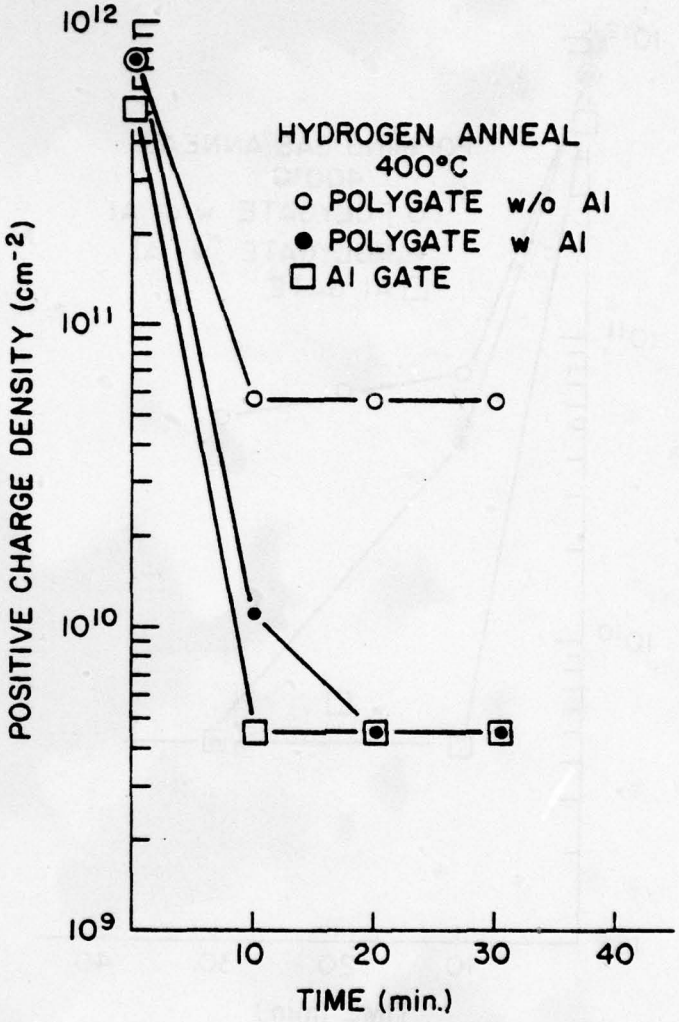


Fig. 2. Removal of radiation induced positive charge from capacitor structures with the indicated contact metallurgies in place over the gate during the anneal. The total effective density of positive charge remaining after an anneal step at 400°C in pure hydrogen is plotted against the anneal time. The oxides were 35.0 nm thick.

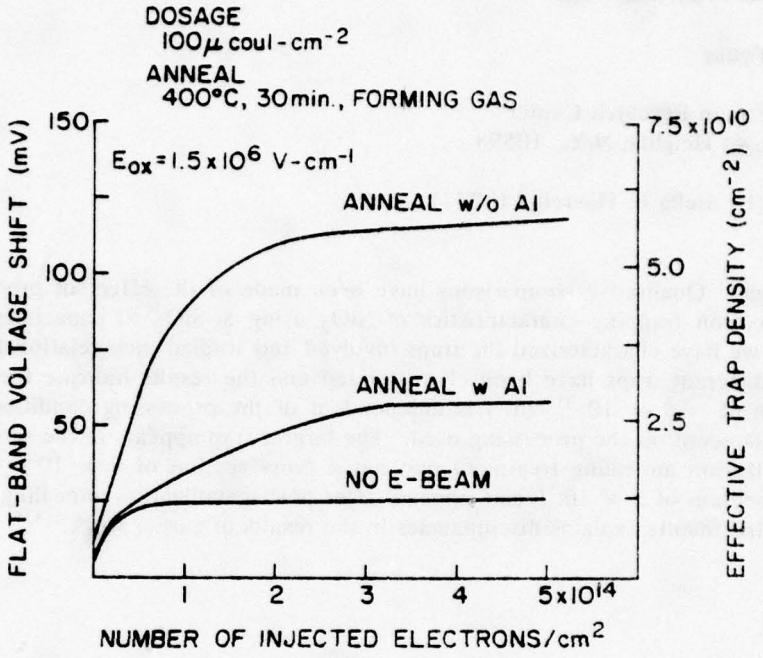


Fig. 3 Capture of injected electrons by unannealed positive charge in the oxides of polysilicon gate capacitors. The two uppermost curves were from capacitors exposed to an electron beam and then annealed as indicated. The bottom curve is from an unirradiated control on the same wafer. The flat-band voltage shift (left-hand axis) or effective trap density (right-hand axis) is plotted against the number of electrons injected per unit area into the oxides of the capacitors.

CHARACTERIZATION OF ELECTRON TRAPS IN SiO_2 AS INFLUENCED BY PROCESSING PARAMETERS*

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Abstract: Qualitative comparisons have been made of the effect of processing conditions on the electron trapping characteristics of SiO_2 using Si-SiO_2-Al capacitors.[2,4] In the present work, we have characterized the traps involved and studied their relationship to the processing. Four different traps have been characterized and the results indicate the smallest trap (cross section of $\sim 9 \times 10^{-20}$ cm^{-2}) is independent of the processing conditions. The larger traps are dependent on the processing used. The largest trap appears in the sample without the post metallization annealing treatment and has a cross section of 8×10^{-18} cm^2. The trap with cross section of 2×10^{-18} cm^2 appears after post metallization annealing. The importance of these treatments explains discrepancies in the results of earlier work.[1,3,4]

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I. Introduction

The electron trap densities and cross sections of SiO_2 have been measured as a function of the annealing treatments used. The samples consist of .1 to .2 Ωcm p-type Si, thermally grown SiO_2 with a nominal thickness of 500Å, and evaporated Al electrodes. The effects of heat treatment at the oxidation temperature (1000°C) and treatment after the Al is applied (400°C) are compared. Earlier work[1,2,3,4] has shown the importance of these treatments. The high temperature treatment (1000°C), referred to as POA, reduces the trapping if ambients of N_2 or Ar are used, which does not occur to the same extent if forming gas (90% N_2 + 10% H_2), called F.G., is used. The post metallization treatment which is usually done at 400°C in F.G., referred to as PMA, has the surprising effect of reducing the cross section of the dominant trap. Previous workers have studied the effect of this treatment on the Si-SiO_2 interface properties[5,6]; however, this work shows an effect on the bulk properties of the SiO_2 as verified by photo I-V measurements[4,7].

II. Experimental Procedures

A. Sample Preparation

The Si wafers used were p-type with a resistivity of .1 to .2 Ωcm. The wafers were <100> oriented. The cleaning and oxidation procedures used have been described previously.[8] The POA treatment was done in the oxidation furnace at the same temperature as the oxidation (1000°C). The samples were removed from the oxidation furnace and placed in the evaporator as soon as possible. Previous experience had indicated that an extensive exposure to the laboratory ambient had a significant impact on the results obtained. It is hoped that the Al electrodes protect the SiO_2 from further contamination. The oxide thickness used was nominally 500 Å and the Al electrode diameter was 8.13×10^{-2} cm.

B. Measurement Procedure

The avalanche injection technique[9] is used to induce electron current in the SiO_2. Unless specified otherwise the average avalanche current density used for these experiments was 5.9×10^{-5} Å/cm^2. The measurement, automatic data acquisition, and analysis techniques have been described before[4]. The wave form used in the present work is a 50 kHz saw tooth wave form instead of the square waves used before. This change does not effect the electron trapping results; however, the saw tooth wave form enables us to use the same apparatus for hole trapping studies[10]. Recent work[4] has shown the desirability of making the measurements

at 120°C to avoid complications due to the build up of positive charge at the Si-SiO_2 interface that occurs if the measurement is made at room temperature. Unless indicated otherwise, all the measurements reported in this work were made at 120°C.

The photo I-V technique has been used to study the centroid of the trapped charge and these results indicate a centroid close to the center of the SiO_2[4]; however, there is a small displacement from the center toward the Al-SiO_2 interface. As a result, we conclude that the traps we are studying under these conditions are bulk SiO_2 traps and are not associated with the Al-SiO_2 or Si-SiO_2 interface.[4,7]

III. Comparisons of Various Processing Conditions

A. The effect of POA

The effect of the POA treatment is shown in Fig. 1 where we compare the change in flat-band voltage (ΔV_{FB}) as a function of time for the sample without POA and the sample with a POA treatment of 60 min. in N_2. The flat-band voltage shifts for the former case are about 3 times larger than for the latter case. This reduction does not occur to the same extent if the ambient gas used is forming gas instead of N_2. These results clearly indicate a deleterious effect due to the H_2. It is also interesting to note the relatively large trapping rate with 30 min. N_2 followed by 30 min. F.G. as compared with the reverse order. The "H_2 effect" is reversable at this temperature. These relative comparisons are correct; however, the detailed shape of these curves is effected by the positive charge effect[4,7] since these measurements were made at 20°C. The results for 30 min. N_2 and 30 min. F.G. + 30 min. N_2 are comparable. The results for annealing in Ar are identical to N_2 as shown by Fig. 2 measured at 120°C. In Fig. 3 the importance of POA is shown with the measurements also made at 120°C. These curves become parallel at longer times which indicates that the smaller cross section traps are independent of these treatments.

B. The effect of PMA

Fig. 4 shows the effect of PMA is to reduce the time constant of the exponential curve associated with the charge build up process. This indicates a larger trap cross section for the dominant trap without PMA as compared to the dominant trap with PMA. The total trap density is also reduced by PMA as can be seen by the reduction of the flat-band voltage shift taken at the longer times. The long time shift depends on the total trap density.

In Fig. 5 the temperature used for PMA is varied and it is seen that temperatures above 350°C are required. At 350°C, comparisons were made between N_2 and F.G. ambients with identical results which is probably due to the effect of the Al electrodes in sealing the SiO_2 from ambient effects at this temperature.

IV. Quantitative Results

A. Methods used for characterization

Trap characterization requires that we fit exponentials to the data. The magnitude of the exponentials is related to the trap density and the time constant is related to the trap cross section. This procedure is difficult since a particular run can be controlled by 2 to 3 traps; however, the large number of measurements made by our automatic apparatus (500 to 1000 for a particular run) makes it possible to do this. We fit the data for the longer times first, after the larger traps are saturated. This enables us to characterize the smallest cross section trap. The magnitude of this trap must be corrected for the trap filling that has occurred up to the time of the first measurement used for this trap. The corrected exponential is subtracted from the original data and the resultant used to characterize the next larger trap. In a similar way the third trap can be evaluated.

The accuracy of the overall characterization is evaluated by calculating the standard deviation of the difference between the original data points and the sum of the exponentials. If the fit is satisfactory the standard deviation is .020 to .050 volts as compared to a total shift of 2 to 10 volts. Another procedure used is to plot the result as the exponentials for the individual traps are subtracted from the original data. The magnitude of the final results indicates the validity of the characterization.

For samples with a relatively large cross section trap (such as the samples without PMA), it is impossible to obtain accurate results using a single value of the avalanche current. A larger current is required for the small cross section traps and a smaller current for the large trap. This is accomplished by increasing the current at about 1504 sec. (for this particular run) from 9.8×10^{-6} A/cm^2 to 5.88×10^{-5} A/cm^2. The computer programs can be used by increasing the effective time scale by a factor of 6 over the real time after the current is increased ($5.88 \times 10^{-5} \div 9.8 \times 10^{-6} \simeq 6$). In this case the actual run of 50,000 sec. had an effective duration of 300,000 sec.. An example of this run with the time corrected is shown in Fig. 6. This sample had a POA treatment in F.G. for 30 min. and the standard PMA treat-

ment. The effect of successively subtracting the exponentials corresponding to the various traps is also shown.

The results of the characterizations are shown in Table 1. To simplify the discussion that follows, the following abbreviations will be used. F.G. 30 min. NOPMA will indicate the sample was heated in forming gas at 1000°C for 30 minutes but did not receive a post metallization annealing treatment. The other abbreviations are obvious. The smallest traps measured had a cross section of $\sim 9 \times 10^{-20}$ cm^2 referred to as (A). The (A) trap for F.G. 30 min. PMA is indicated as having a smaller cross section and a larger density. This is most likely an inaccuracy in characterization since the time constants are long for this trap compared with the measurement time. The difference does not appear to be significant. It was not possible to measure these traps for the F.G. 30 min. NOPMA sample due to the large flat-band voltage shifts associated with the larger traps which exceeded the range of the apparatus. The A traps are independent of the processing conditions. This observation is consistent with the parallel nature of the curves shown in Fig. 3 for the longer times. The (B) traps (cross section $\sim 4 \times 10^{-19}$ cm^2) are also present for all the runs; however, their density seems larger for the runs with forming gas. The larger cross section of the (B) trap for F.G. 60 min. (NOPMA) was probably due to the (A) trap which was not characterized for this run and its effect could not be subtracted from the data. The (C) traps (cross section $\sim 2 \times 10^{-18}$ cm^2) are present in the samples with PMA but not in the samples with NOPMA. The density of the (C) traps is larger for the samples with forming gas treatment. The (D) traps (cross section $\sim 8 \times 10^{-18}$ cm^2) are only present in the runs with NOPMA. Their density is also larger for the samples with a forming gas treatment. It is possible that the PMA treatment converts the (D) traps to the (C) traps although the density of the (C) traps is less than the (D) traps.

V. Conclusions

The electron trapping characteristics of SiO_2 are sensitive to the processing conditions; the heat treatment and gaseous ambient at 1000°C, and the heat treatment after the aluminum electrodes are applied. The processing conditions do not effect the smallest traps with cross sections of $\sim 9 \times 10^{-20}$ cm^2. Traps with cross sections of $\sim 4 \times 10^{-19}$ cm^2 had a larger density, if the heat treatment at 1000°C used forming gas as an ambient instead of N_2 or Ar. The post metallization heat treatment (400°C) did not effect these traps. Larger traps with cross section of $\sim 2 \times 10^{-18}$ cm^2 were observed with post metallization heat treatment and traps with cross section of $\sim 8 \times 10^{-18}$ cm^2 were observed without this heat treatment.

The large cross section observed by Nicollian and Berglund of 1.5×10^{-17} cm^2 as compared with more recent work by[3,4] indicating a cross section of $\sim 2 \times 10^{-18}$ cm^2 can be explained as being due to the post metallization annealing treatment used in the recent work. The discrepancy of our result of 8×10^{-18} cm^2 as compared to Nicollian and Berglund's value of 1.5×10^{-17} cm^2 may be a result of the corrections we have applied for the smaller traps. The present work indicates a significant effect on the bulk properties of the SiO_2 as a result of the post metallization annealing treatment. Previous workers had observed effects due to this treatment related to the Si-SiO_2 interface. The measurements have been made at 120°C to avoid errors due to the positive charge effect.

Di Maria, Aitken, and Young[11] measured the electron trapping in SiO_2 at 77°K. This also avoids the positive charge effect since the donor states responsible for this effect are not generated at this temperature. Their work did not use the analysis procedure used in more recent work and therefore the results are not as accurate (particularly with respect to the trap densities). They observed traps with cross sections of 1×10^{-17} cm^2, 5×10^{-20} cm^2 and 6×10^{-21} cm^2. The two largest traps are similar in cross section to the results of this work. The smallest trap was not evaluated at 120°C.

The difference in results for treatments in forming gas as compared to N_2, which must be due to the H_2 present, for the larger traps is probably consistent with the earlier conclusions that these traps are related to OH groups in the SiO_2.

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TABLE I

Trap Characterization

	F.G. 30 min. PMA				F.G. 60 min. NOPMA		
	σ	N_{eff}	N_v		σ	N_{eff}	N_v
(C)	2.93×10^{-18}	1.47×10^{12}	5.9×10^{17}	(D)	8.8×10^{-18}	1.9×10^{12}	7.6×10^{17}
(B)	5.02×10^{-19}	4.12×10^{11}	1.6×10^{17}	(C)	3.9×10^{-18}	3.7×10^{11}	1.5×10^{17}
(A)	4.69×10^{-20}	1.08×10^{12}	4.3×10^{17}	(B)	8.8×10^{-19}	4.6×10^{11}	1.8×10^{17}

N_2 (PMA)

	30 min.				60 min.		
	σ	N_{eff}	N_v		σ	N_{eff}	N_v
(C)	2.9×10^{-18}	6.7×10^{11}	2.7×10^{17}	(C)	1.9×10^{-18}	5.0×10^{11}	2.0×10^{17}
(B)	4.4×10^{-19}	2.2×10^{11}	8.8×10^{16}	(B)	4.9×10^{-19}	1.2×10^{11}	4.8×10^{16}
(A)	9.9×10^{-20}	6.5×10^{11}	2.6×10^{17}	(A)	8.7×10^{-20}	6.3×10^{11}	2.5×10^{17}

N_2 30 min. NOPMA

	σ	N_{eff}	N_v
(D)	7.2×10^{-18}	1.1×10^{12}	4.4×10^{17}
(B)	5.3×10^{-19}	1.8×10^{11}	7.2×10^{16}
(A)	8.6×10^{-20}	5.8×10^{11}	2.3×10^{17}

The trap cross sections (σ) are in cm^2, N_{eff} is the effective areal density in cm^{-2}, N_V is the volume density in cm^{-3} calculated from N_{eff} using a centroid correction of 2 (assuming the traps are uniformly distributed throughout the SiO_2) and dividing by the thickness. The time in minutes refers to the time for heat treatment at 1000°C. The traps with the same letters are thought to be identical.

FIGURE CAPTIONS

Figure 1. Effect of post oxidation annealing (POA) on electron trapping (as measured by the flat band voltage shift) as a function of time. These samples all had the standard PMA treatment. The measurements for this series were made at 20°C.

Figure 2. Comparison of 1000°C annealing in N_2 and Ar showing identical results. These samples had the standard PMA treatment.

Figure 3. The effect of POA on the charge build up process. These samples had the standard PMA treatment.

Figure 4. Reduction in cross section of dominant trap as a result of PMA.

Figure 5. Dependence on the temperature used for PMA. In each case the time was 20 min.. The standard POA treatment was used.

Figure 6. Effect of subtracting exponentials for 3 traps successively from the original data. This sample at a treatment of F.G. 30 min. PMA. The traps had cross sections of 4.7×10^{-20}, 5.02×10^{-19}, and 2.9×10^{-18} cm^2, respectively. The corresponding effective areal densities were 1.08×10^{12}, 4.12×10^{11}, and 1.47×10^{12} cm^{-2}.

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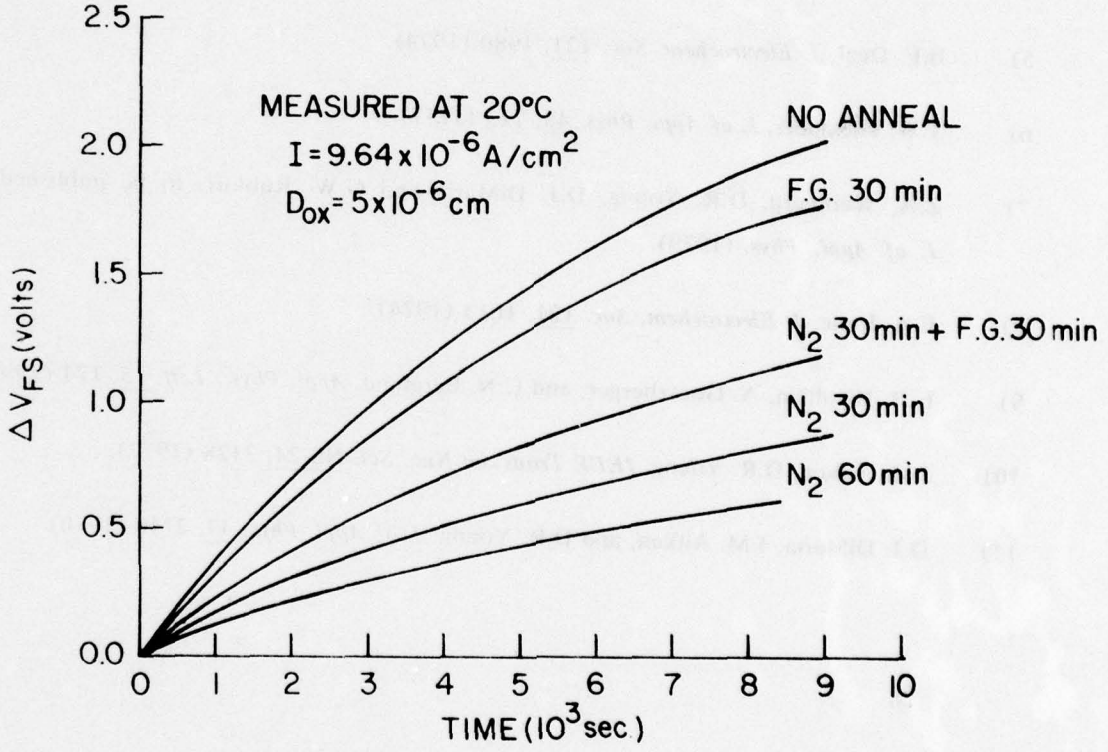

2.5
2.0
1.5
1.0
0.5
0.0
ΔV_{FS} (volts)
MEASURED AT 20°C
$I = 9.64 \times 10^{-6} A/cm^2$
$D_{ox} = 5 \times 10^{-6} cm$
NO ANNEAL
F.G. 30 min
N_2 30min + F.G. 30 min
N_2 30min
N_2 60min
0 1 2 3 4 5 6 7 8 9 10
TIME (10^3 sec)

FIGURE 1

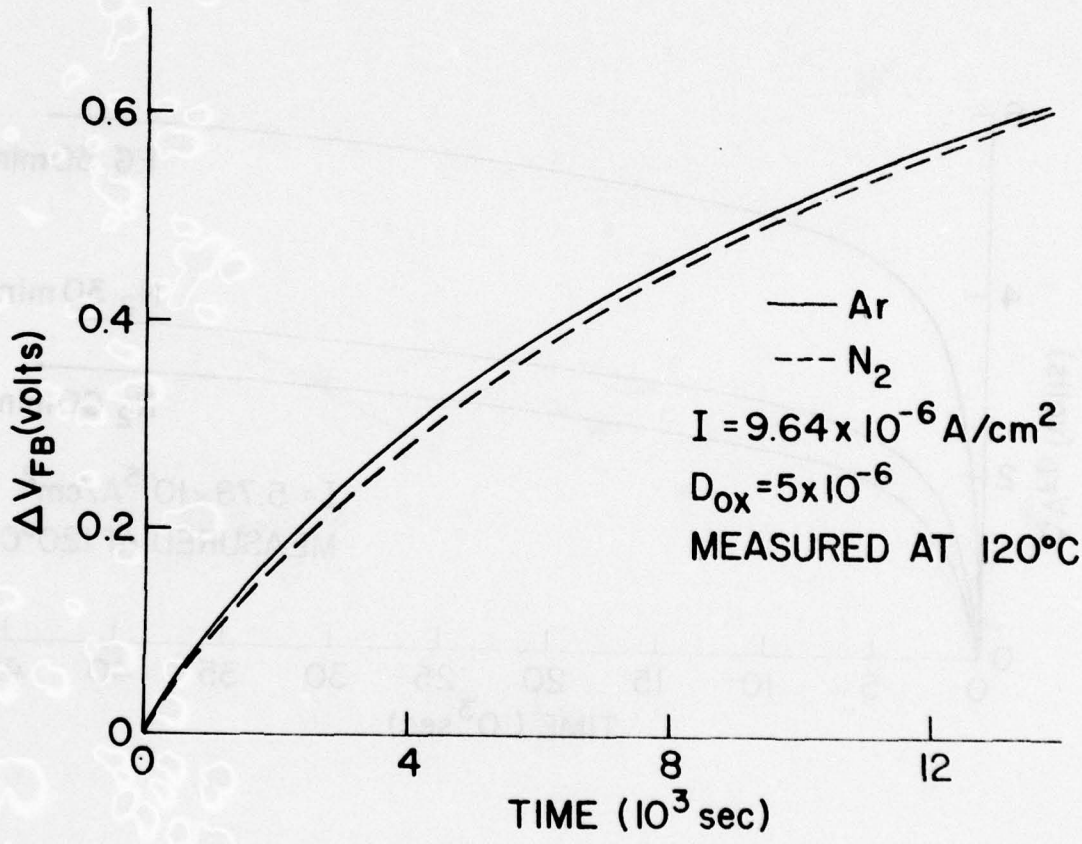

0.6
0.4
0.2
0
ΔV_{FB}(volts)
0
4
8
12
TIME (10^3 sec)
Ar
N_2
$I = 9.64 \times 10^{-6}$ A/cm^2
$D_{ox} = 5 \times 10^{-6}$
MEASURED AT 120°C

FIGURE 2

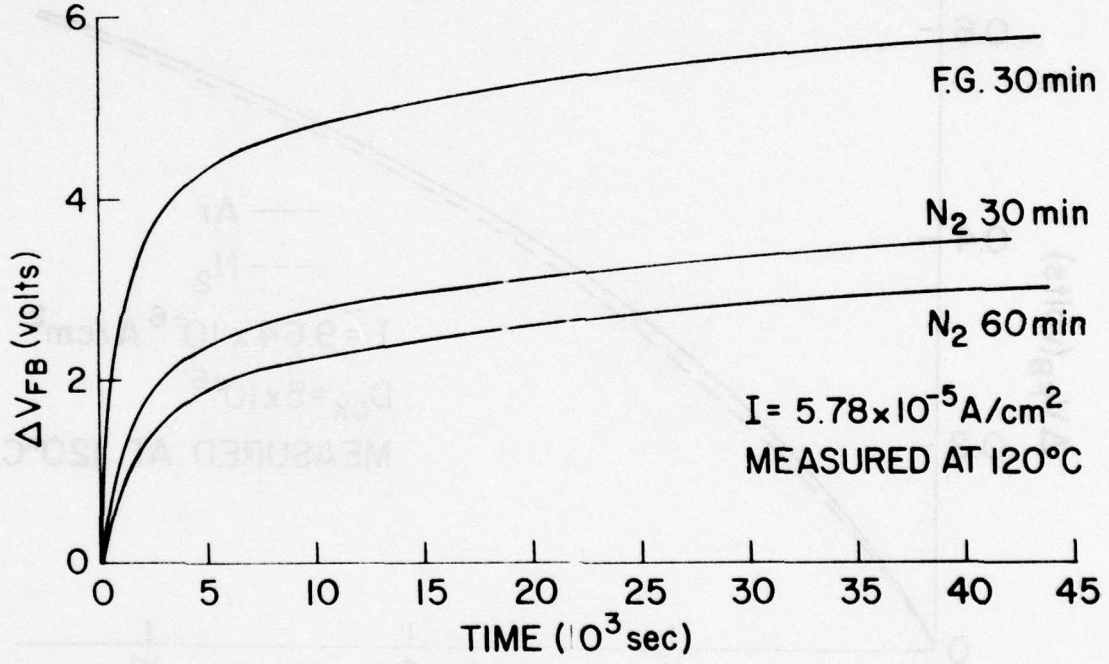

6
4
2
0
ΔV_{FB} (volts)
F.G. 30min
N_2 30 min
N_2 60min
I= 5.78×10^{-5} A/cm^2
MEASURED AT 120°C
0
5
10
15
20
25
30
35
40
45
TIME (10^3 sec)

FIGURE 3

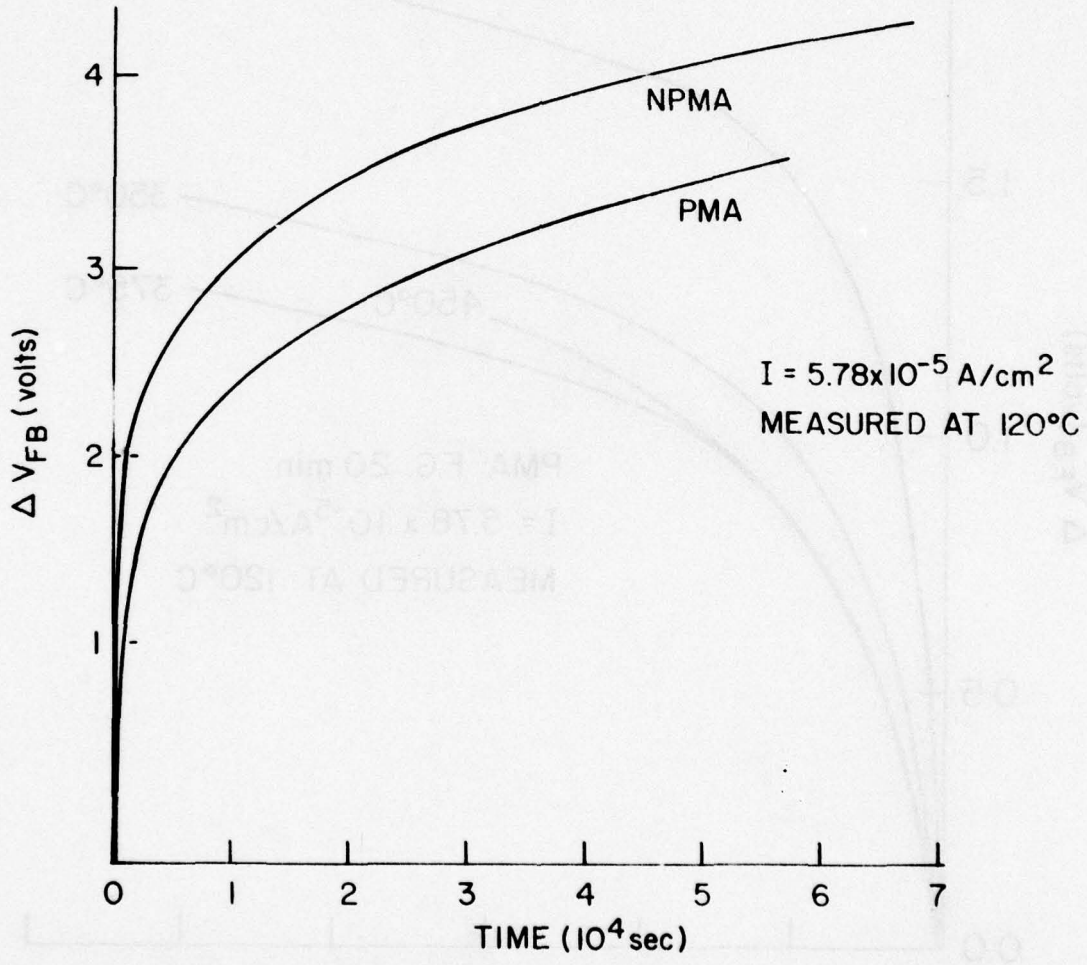

NPMA
PMA
I = 5.78x10⁻⁵ A/cm²
MEASURED AT 120°C
Δ V_FB (volts)
TIME (10⁴ sec)
0
1
2
3
4
5
6
7

FIGURE 4

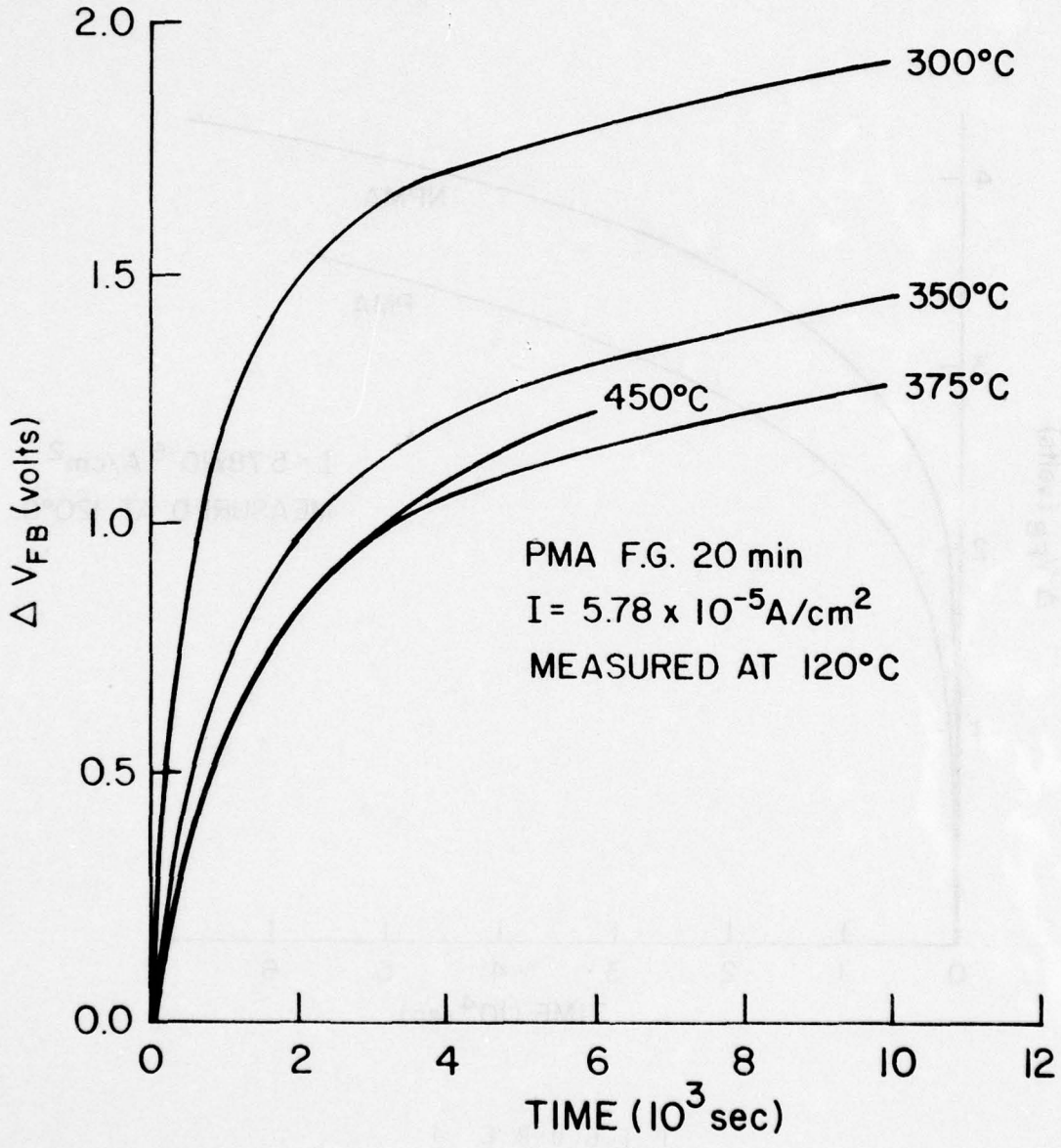

2.0
1.5
1.0
0.5
0.0
Δ V_{FB} (volts)
300°C
350°C
450°C
375°C
PMA F.G. 20 min
I = 5.78 x 10^{-5} A/cm^2
MEASURED AT 120°C
0
2
4
6
8
10
12
TIME (10^3 sec)

FIGURE 5

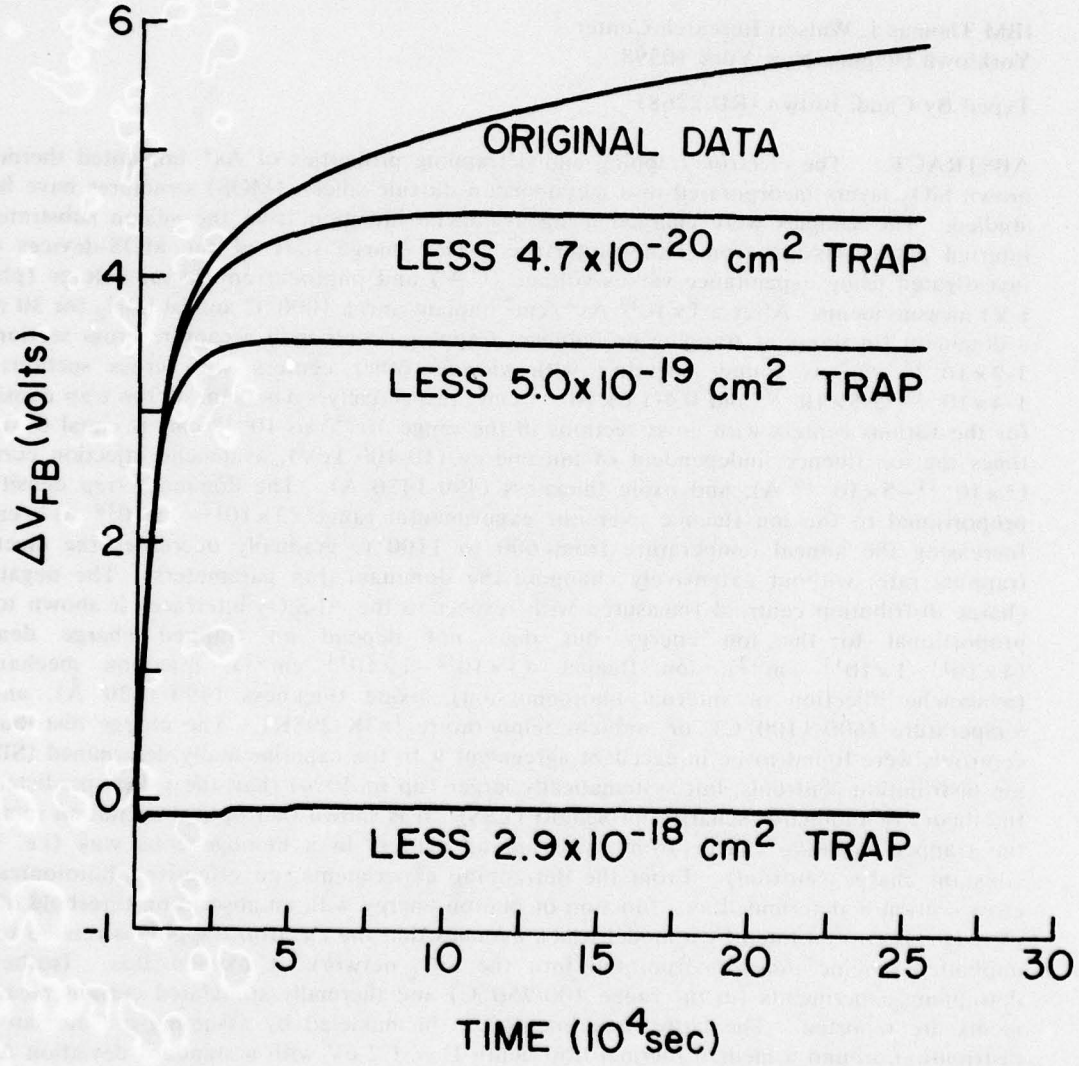

6
4
2
0
-1
ΔVFB (volts)
ORIGINAL DATA
LESS 4.7x10-20 cm2 TRAP
LESS 5.0x10-19 cm2 TRAP
LESS 2.9x10-18 cm2 TRAP
5
10
15
20
25
30
TIME (10⁴sec)

FIGURE 6

ELECTRON TRAPPING AND DETRAPPING CHARACTERISTICS OF ARSENIC IMPLANTED SiO_2 LAYERS*

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ABSTRACT: The electron trapping and detrapping properties of As^+ implanted thermally grown SiO_2 layers incorporated into metal-silicon dioxide-silicon (MOS) structures have been studied. The samples were charged using avalanche injection from the silicon substrate or internal photoemission from either interface. The charge state of the MOS-devices was investigated using capacitance-versus-voltage (C-V) and photocurrent-versus-voltage (photo I-V) measurements. After a 1×10^{13} As^+/cm^2 implant and a 1000°C anneal in N_2 for 30 min, a dominant (in terms of trapping probability) trapping center with a capture cross section of $1\text{-}2\times10^{-15}$ cm^2 is found, together with various other centers with cross sections of $1\text{-}4\times10^{-17}$, $2\text{-}5\times10^{-16}$ and $0.4\text{-}1.6\times10^{-14}$ cm^2, respectively. The sum of the trap densities for the various centers with cross sections in the range 10^{-15} to 10^{-16} cm^2 is equal to 0.7-1 times the ion fluence, independent of ion energy (10-100 keV), avalanche injection current (5×10^{-11}–5×10^{-10} A), and oxide thickness (490-1430 Å). The dominant trap density is proportional to the ion fluence over our experimental range (3×10^{12}–1×10^{14} As^+/cm^2). Increasing the anneal temperature from 600 to 1100°C gradually decreases the electron trapping rate, without extensively changing the dominant-trap parameters. The negative-charge distribution centroid (measured with respect to the Al-SiO_2 interface) is shown to be proportional to the ion energy but does not depend on trapped charge density (4×10^{11}–1×10^{13} cm^{-2}), ion fluence (3×10^{12}–1×10^{14} cm^{-2}), injection mechanism (avalanche injection or internal photoemission), oxide thickness (490-1430 Å), anneal temperature (600-1100°C), or ambient temperature (83K-295K). The charge distribution centroids were found to be in excellent agreement with the experimentally determined (SIMS) ion distribution centroids, but systematically larger (up to 40%) than the values predicted by the theory of Lindhard, Scharff and Schiott (LSS). It is shown that optical excitation removes the trapped negative charge from the trapping centers in a homogeneous way (i.e. with constant charge centroid). From the detrapping experiments, an effective photoionization cross section is determined as a function of photon energy with an absorption threshold of 3.3 eV. This is corroborated by a model which assumes that the electron trapping is related to the implanted arsenic ions, incorporated into the SiO_2-network at oxygen-sites. Isothermal detrapping experiments (in the range 100-250°C) and thermally stimulated current meausrements are reported. The latter experiments can be modeled by assuming a Gaussian trap distribution around a median thermal trap depth E = 1.2 eV with a standard deviation ΔE = 0.2 eV.

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I. INTRODUCTION

Ion implantation has recently become available as a standard doping technique in semiconductor processing, where its high degree of control of profiles for the common silicon dopants such as boron, phosphorus, and arsenic has been appreciated [1].

Unwanted side-effects, however, may occur when implanting these ions through a thermally grown SiO_2-layer in order to dope the substrate underneath. It has been shown, for example, that surface states are generated at the Si-SiO_2 interface [2,3] and that defects are created in the substrate due to recoiling oxygen atoms from the oxide layer [4]. Recently, several experiments have demonstrated that ion implantation also affects the oxide layer by introducing electron trapping centers [5-8]. It has even been proposed to use the electron trapping phenomenon to harden metal-silicon dioxide-silicon (MOS) structures which have to operate in an ionizing radiation environment [9,10]. Such effects have generated little concern among device designers, perhaps due to the belief that the electron trapping is correlated with structural damage in the SiO_2-layer and should therefore have disappeared after the annealing treatment necessary to restore the crystallinity of the implanted substrate lattice.

In recent publications from this laboratory [11-13] it was reported that ion implantation into the oxide layer of device-grade MOS-structures can cause considerably enhanced electron trapping, persisting after a high temperature anneal (typically at 1000°C). In this paper, the electron trapping characteristics of arsenic-implanted SiO_2-layers are investigated in detail, using mainly avalanche injection as a charging tool, and subsequent photoemission measurements to probe the amount of charge and its location in the oxide. The possibility of removing the charge both by optical and thermal excitation from the trapping sites is demonstrated and the detrapping properties are studied.

It was expected that annealing at high temperatures would reduce trapping effects related to damage and that there would be an increasing correlation between any remnant trapping

and the nature of the implanted ions. We have indeed found strong indications for such a correlation, although the exact nature of the trapping sites is uncertain at present. Yet, it is believed that techniques such as those applied here will prove useful to investigate the poorly understood electrical and structural effects of impurities in SiO_2, not only from dopants deliberately introduced in large concentrations during the processing, but also from inadvertently incorporated trace impurities.

II. EXPERIMENTAL

A. Sample Fabrication

The samples used were 0.1 - 0.2 Ωcm p-type <100> silicon wafers. After thermal oxidation in a nominally dry oxygen ambient at 1000°C to thicknesses ranging from 490 to 1440 Å (determined by ellipsometry), the wafers were given the As^+ implantation at room temperature with fluences ranging from 3×10^{12} to 1×10^{14} cm^{-2} and ion energies from 10 to 100 keV. Then all wafers were cleaned using alkaline-peroxide and acid-peroxide solutions [14] and annealed in nitrogen at 1000°C for 30 min unless otherwise specified. Using a shadow mask, thin (120-150 Å) circular aluminum electrodes with an area of 5.2×10^{-3} cm^2 were deposited from an rf-heated crucible at a pressure of 10^{-6} torr to form MOS capacitors. The semi-transparent metal electrodes were used to permit generation of photocurrents from both the silicon and the aluminum contacts. The exact aluminum thickness was determined from a white-light transmission measurement through aluminum deposited on quartz plates concurrently with the wafers. Finally, all MOS devices were given a post-metallization annealing treatment at 400°C in forming gas (N_2/H_2 mixture) for 20 min to reduce the density of surface states.

B. Measurement of Trapping Properties

Avalanche injection [15,16] from the silicon substrate driven into deep depletion was used to inject electrons into the SiO_2 layer. Using an automated feedback circuit, the amplitude of a 50-kHz ramp wave was continuously adjusted in order to keep the average dc injection current constant at a preset level in the range from 10^{-11} to 10^{-8} A. The current was periodically interrupted to sense the flat-band voltage which increased as some of the injected electrons were captured in the oxide. These flat-band voltage readings with the corresponding total injection-time readings were stored in a minicomputer with an active workspace of 64 kbytes (IBM model 5100). The flat-band voltage shifts are defined as the shifts of the 1-MHz capacitance-versus-voltage (C-V) curves, measured after charging, with respect to the initial C-V curve.

In the absence of detrapping, we can use first-order kinetics as treated by Ning and Yu [17] to derive the trapping parameters from the observed evolution of the flat-band voltage shift ΔV_{FB} in time at a constant avalanche injection current density j [18]:

$$\Delta V_{FB}(t) = eN_{eff}(L/\epsilon)[1 - exp(-\sigma_c j\, t/e)] \tag{1}$$

where e is the electron charge, L is the oxide thickness, ϵ is the low frequency permittivity of SiO_2, σ_c is the capture cross section of the oxide traps and N_{eff} is their effective density defined by:

$$N_{eff} = (\bar{x}/L)N_T, \tag{2}$$

where $\bar{x}$ is the centroid of the trapped charge distribution as measured from the Al-SiO_2 interface, and N_T is the total density of available trapping sites $N_t(x)$ integrated over the oxide thickness:

$$N_T = \int_0^L N_t(x)dx. \tag{3}$$

If more than one trapping center is present, the actual shift $\Delta V_{FB}(t)$ will be the summation of the individual contributions of each center, characterized by its own capture cross section $\sigma_{c,i}$ and density $N_{T,i}$ [19].

C. Measurement of Trapped Charge and its Centroid

It has been reported [20] that photocurrent-versus-voltage (photo I-V) characteristics for MOS structures are sensitive to the amount of trapped charge and its centroid in the insulator. This technique has been routinely applied during our study to determine both parameters. To generate the photocurrents in our MOS structures, a 900-W xenon arc lamp was used in combination with a 500-mm grating monochromator (Bausch and Lomb). The photon flux at the output was in the range $10^{12}-10^{13}$ photons/cm^2-sec. At positive (negative) gate bias a photon energy of 5(4.5) eV was used in order to excite electrons over the SiO_2-Si(Al) barrier. Current measurements were done at room temperature in air with the remote head of a fast picoammeter (Keithley model 417) directly connected to the sample chamber fitted with a quartz window. Front contact to the semitransparent gate of the MOS samples was made using 5 mil electrochemically polished tungsten probes. The gate voltage was increased using a voltage step generator, usually in steps of 1 V, and both voltage and current readings were directly stored into an IBM VM168 computer via an interface unit (IBM Research device coupler).

After homogeneous bulk charge trapping, the photo I-V curves are expected to shift in a parallel manner along the voltage axis, at all but possibly the lowest gate voltages. The shifts were shown to depend on the charge location for a given charge density [20]. The following relations are obtained for the gate voltage shifts at a fixed photocurrent level:

$$\Delta V_g^- = V_{g_b}^- - V_{g_a}^- = (L - \bar{x})Q/\epsilon \qquad (4a)$$

of the charge distribution. Reproducibility checks on photo I-V data were also performed to ascertain that the charge distribution was only minimally perturbed.

The measurement times were kept as short as possible (usually 24 s illumination time) but long enough to allow phototransients to decay and the light intensities were occasionally reduced using wire-mesh screens to yield the lowest possible photocurrents still compatible with the noise levels (useful current range: 10^{-13} – 10^{-11} A). In this way, perturbation of the trapped oxide charge by additional trapping or by photodetrapping was avoided during the photocurrent measurements. Under positive bias, the sample was illuminated with an ordinary incandescent lamp, besides the monochromatic beam, to assist the build-up of the inversion layer. Dark currents, although usually very small, have been subtracted from measured photocurrents before the data were stored.

It is a particular feature of our monochromator set-up, that the sample can be charged in situ using avalanche injection. This avoids moving the sample and eliminates possible variations in the photoemission currents after repositioning of the wafer, due to a spatially inhomogeneous light intensity.

D. Photodetrapping Measurements

After charging the traps in the oxide by avalanche injection from the Si or by internal photoemission from the Si or Al [23], the photodetrapping was studied at successively increasing photon energies using the same monochromator as described above. An electric shutter was used to control the time of illumination which was usually 5 min. The flat-band voltage shift resulting from this illumination was monitored using an automated set-up. For measurements below room temperature, a liquid-nitrogen transfer system (Air Products Heli-Tran) was used in connection with an optical cryostat.

In order to characterize the detrapping phenomenon, the photon flux at the sample position had to be measured. For this purpose, the MOS sample was replaced by a thermopile

$$\Delta V_g^+ = V_{g_b}^+ - V_{g_a}^+ = -\bar{x}Q/\varepsilon \tag{4b}$$

where the superscripts (+ or −) refer to the metal gate polarity, the subscripts a and b refer to the sample before and after charging, respectively, and Q is the integral of the trapped charge density over the oxide thickness.

It has been shown previously that the flat-band voltage shift ΔV_{FB} and ΔV_g^+ are equal in magnitude if there is only bulk trapped charge present in the oxide [20,21]. This can be understood as follows. While ΔV_{FB} tracks the field in the silicon, and is, therefore, sensitive to both bulk oxide charge and charge at the Si-SiO_2 interface, ΔV_g^+ is only determined by the field in the oxide, which is not sensitive to charges at the Si-SiO_2 interface. A one-to-one correlation between ΔV_{FB} and ΔV_g^+ is, therefore, only possible if there is no interface charge.

By combining Eqs. 4a and 4b, the following expressions are obtained for the trapped charge density Q and the centroid $\bar{x}$ of its distribution:

$$Q = (\varepsilon/L)(\Delta V_g^- - \Delta V_g^+) \tag{5}$$

$$\bar{x} = L[1-(\Delta V_g^-/\Delta V_g^+)]^{-1}. \tag{6}$$

When photocurrents are generated by chopped-light techniques, degenerate Si-substrates have to be used in order to reduce the displacement current induced by a varying surface potential. One of the features of the photo I-V technique as developed by DiMaria [20] is that it uses continuous light, so that sufficient time can be allowed for a large transient photoelectric effect in the substrate to decay. The use of degenerate Si is then no longer mandatory and it becomes possible to do complementary high-frequency (1 MHz) C-V measurements [22] on the same sample before and after a photocurrent-versus-voltage run to monitor perturbations

with a CaF_2 window. The monochromatic beam was chopped using a 13-Hz electric chopper (Bulova), and the output voltage of the thermopile was measured with a lock-in amplifier (PAR 124) via a transformer for impedance matching (PAR 190).

E. Thermal Detrapping

To study the isothermal emptying of the trapping sites the samples were put on a covered hot stage in a nitrogen flow. The temperature of the stage can be raised to 250°C and kept constant within 2°C using a thermistor-controlled power supply.

Thermally-stimulated current measurements were performed in a modified thermoluminescence dosimeter (Harshaw model 2000) as described previously [24]. A background current, measured during a second heating cycle, was subtracted from the initially measured discharging current.

III. ANALYSIS OF AVALANCHE INJECTION DATA.

A. Ion Energy Dependence

Figure 1 shows the flat-band voltage shifts as a function of injection time for samples implanted with arsenic at varying ion energies. The faster charging at higher ion energies is understood in terms of the increasing ion penetration depth, which is expected to yield an increasing charge-distribution centroid (measured with respect to the gate), provided the charge build-up is closely correlated with either the implanted ions themselves or their effects in the oxide. As seen in Fig. 2, the average flat-band voltage shift, calculated over a constant charging time interval (approx. 5000 s) varies linearly with ion energy. Since to a first-order approximation, the ion distribution centroid is varying linearly with ion energy, it is concluded that the integrated oxide charge and, therefore, the integrated number of traps created in the oxide is essentially independent of ion energy. The variation of the charge centroid $\bar{x}$ with ion energy as determined using the photo I-V technique will be addressed directly in Sec. V-B.

The analysis described in Sec. II-B was applied to reduce the ΔV_{FB}-versus-time data using a computer program. The program is able to fit 2 exponentials of the form of Eq. 1 to a given set of data points. By carrying out the measurements over extended periods of time and carefully selecting the time interval over which the analysis is performed, we were able to extract up to 5 trapping centers from the data. This procedure relies upon the fact that, when a time equal to approximately 5 time constants has elapsed, the contribution of a particular trap to the trapping rate has vanished. A fit was generally considered satisfactory when the standard deviation between the measurement and the calculated sum of exponentials was less than 5 mV. Capture cross sections and trap densities resulting from typical runs are summarized in Table I. It is important to notice, that the Table lists values for the trap density integrated over the oxide, N_T, and not for the effective trap density N_{eff}. To obtain N_T from N_{eff}, data for the centroid $\bar{x}$ (as determined in Sec. V) had to be used. It was also assumed here that the different trapping centers result in charge distributions with identical centroids. This assumption is supported by experimental evidence, as will be discussed further.

From Eq. 1, it is seen that the charging time constant for a single trap level is given by $\tau = e/(\sigma_c j)$. To perform a meaningful fit, this time constant has to be much larger than the time interval between V_{FB}-readings, yet, smaller than the total measurement duration (50,000 s, corresponding to 1000 measurement points, is a practical limit in our experiments). Depending on the order-of-magnitude of the cross section for which one wants to accumulate data, the current density can be chosen to meet these requirements. The current density was varied from 10^{-5} to 10^{-8} A/cm^2. This range gave us access to traps with cross sections varying roughly from 10^{-14} to 10^{-18} cm^2, but there are limitations on both extremities of this range.

First we consider the limitations for small capture cross sections. When the avalanche injection is performed with high current densities in order to study small capture cross sections, it has been observed that positive charge builds up at the Si-SiO_2 interface [25], counteracting the effect of the negative charge accumulation in the bulk of the SiO_2 and distorting the

ΔV_{FB}-data. The origin of this phenomenon is at present not understood. Although the centers at the Si-SiO_2 interface are still created, it has been observed that they will not become charged when the measurement is performed at temperatures slightly above room temperature (100-120°C). Using this procedure, 2 centers with low capture cross section were measured in a control sample, as shown in Table II. Since this electron trapping, associated with water in the oxide layer, is a homogeneous bulk phenomenon at room temperature [25], the charge centroid was taken to be half the oxide thickness. A trapping center with a cross section of $1\text{-}4\times10^{-17}$ cm^2 is also found in some of the implanted samples, as seen in Table I, but its density has been considerably increased by the implantation. Moreover, this center was not reproduced in subsequent control samples (unlike the 10^{-18}-cm^2 center), but always appeared after the arsenic implantation. It thus appears to be related to the ion implantation process and its corresponding charge centroid is, therefore, assumed to be equal to the value obtained from photo I-V data. In order to determine the 10^{-17}-cm^2 trap density with sufficient resolution, the injected electron density has to be of the order 2×10^{17} cm^{-2}. This requires a low saturated ΔV_{FB}-value from the larger capture cross sections and thus a low implant energy or fluence. For the measurement on wafer AS7B at 120°C, no results on a 10^{-15}-cm^2 trap are reported, in view of a partial thermal detrapping effect (see Sec. VII). The presence of the 10^{-18}-cm^2 trap in the implanted samples has not been investigated.

On the high side of the cross-section-scale, a trap with a σ_c from $\sim4\times10^{-15}$ to 10^{-14} cm^2 has been consistently observed in the implanted samples. This may correspond to a Coulomb-attractive (positively charged) center, whose capture cross section has been lowered by the electric field in the oxide during avalanche injection (3-4 MV/cm). The resolution for this center was poor due to the low charging time constant and the small density; therefore the results are reported in parentheses in Table I. Photoinjection experiments at low fields ($\sim$ 0.5 MV/cm) which yield more information on these centers are discussed below (Sec. IV (i)).

It is also seen from Table I that there is a spectrum of centers with cross sections varying from approximately 1×10^{-15} to 1×10^{-16} cm^2. No systematic partition of centers among these various cross sections is observed, but the sum of the trap densities is seen to be of the same order-of-magnitude as the ion fluence, and fairly independent of ion energy contrary to what has been observed for Al-implanted samples [12]. In any charging experiment, the 10^{-15}-cm^2 cross section will be dominant due to the large initial capture probability, given by the product of the capture cross section and the effective trap density [17].

B. Ion Fluence Dependence

Increasing the implanted ion fluence is expected to increase the density of available trapping sites in the oxide. This was investigated by implanting a set of 3 wafers at an energy of 80 keV at increasing fluences of respectively 3×10^{12}, 10^{13} and 10^{14} As^+/cm^2. The results of the avalanche injection analysis are given in Table III.

It is seen that, if one considers the dominant trapping center with $\sigma_c \approx 1\text{-}2\times10^{-15}$ cm^2, the trap density N_T is proportional to the ion fluence.

In Fig. 3, the ratio of the flat-band voltage shift has been plotted versus charging time for a fluence of 10^{14} cm^{-2} relative to 10^{13} cm^{-2} (curve A) and for a fluence of 10^{13} cm^{-2} relative to 3×10^{12} cm^{-2} (curve B), charged respectively with an avalanche injection current of 3×10^{-11} A and 9×10^{-11} A. It is seen that in both cases the ratio approaches the fluence ratio of 10 and 3.3, respectively.

C. Annealing Dependence

In order to determine a practical anneal temperature for our further studies, 3 wafers were implanted with 1×10^{13} As^+/cm^2 at 80 keV, and annealed in nitrogen for 30 min at 600, 800, and 1000°C, respectively. The flat-band voltage shifts during avalanche injection as a function of time are shown in Fig. 4. It is seen that higher anneal temperatures reduce the

electron trapping rate. The results obtained from the avalanche injection analysis are given in Table IV. The capture cross-section of the center with $\sigma_c \approx 10^{-15}$ cm^2 is seen to decrease slightly with anneal temperature from 600 to 1000°C, whereas after a 1000°C-anneal the trap density for this center is higher than for the 80 keV implant from batch AS7 (for which results are given in Table I). However, these numbers have to be treated with caution. The measurement time after which the maximum ΔV_{FB} in our set-up is reached, is only of the order of one time-constant of the charging process for the lower anneal temperatures (600 and 800°C), so an accurate fit of the data cannot be performed.

The completion of the high-temperature anneal was investigated by annealing wafer AS7E at 1000°C for 2 h and AS7F at 1100°C for 30 min, both in nitrogen. In Fig. 5, the ΔV_{FB}-vs-time data obtained during avalanche injection are compared with data for a sample from the same batch annealed at 1000°C for 30 min. It is seen that the longer anneal at 1000°C does not further decrease the trapping rate. From this observation, it was concluded that a 30 min anneal at 1000°C is sufficient to terminate the removal of gross structural damage.

As seen in Fig. 5, the 1100°C treatment further reduced the trapping rate in batch AS7. During a duplicate of this experiment (only with a lower implant fluence of $5 \times 10^{12} As^+/cm^2$), this observation was not reproduced, as the 1000 and 1100°C anneals for 30 min resulted in an almost identical trapping rate. We have occasionally also observed reverse annealing phenomena, yielding lower trapping rates after an 800°C anneal compared to a 1000°C anneal. These observations led us to conclude that the details of the ion implantation (e.g. dose rate) and the annealing treatment (e.g. heating or cooling rate) might have an impact upon the location of the implanted ions and their trapping efficiency in the oxide and thus ultimately be responsible for variations in the electron trapping rate from run to run, all other processing variables being constant. Although masked by same irreproducibilities from run to run, the general trend in our experiments was for the longer or higher -temperature anneals to

reduce the trapping rate, i.e. remove traps from the high cross section range (order 10^{-15}–10^{-16} cm^2).

The trapping parameters for wafers AS7E and AS7F are included in Table IV. The longer anneal at 1000°C resulted in a higher density of trapping sites with $\sigma_c \approx 10^{-15}$ cm^2 when compared with the results for wafer AS7D (Table I), but since a considerable amount of traps with $\sigma_c \approx 5 \times 10^{-16}$ cm^2 was found in wafer AS7D, the trapping rates in both wafers are nearly equal. Here, the 1100°C anneal is seen to reduce the concentration of all centers in the 10^{-15}- to 10^{-16}-cm^2 range of capture cross sections, and therefore reduces the trapping rate approximately by a factor of 2 compared to a 1000°C anneal.

D. Oxide Thickness Dependence

Wafer AS7M with a 490-Å thick SiO_2 layer was implanted with 1×10^{13} As^+/cm^2 at 20 keV. The trapping parameters summarized in Table V, are similar to those reported for MOS structures with 1400-Å thick SiO_2 layers, indicating that no ions are penetrating into the silicon through the 490-Å oxide film and that the ion distribution is not considerably broadened as is the case for Al-implants [12].

IV. DISCUSSION OF TRAPPING PARAMETER RESULTS

(i) The major capture cross section values which are detected in our experiments are indicative of electrically neutral trapping centers [26]. This is compatible with the approximately net neutral state of the virgin samples after implantation and annealing as indicated by C-V measurements.

In most of the implanted samples, centers with a capture cross section larger than 10^{-15} cm^2, although poorly resolved from the avalanche injection data, contribute a few hundred mV to the flat-band voltage shift after avalanche injection. As mentioned above, these centers might be due to a small amount of remnant positive charge,

originating from the ion implantation. The presence of these centers was further investigated by photoinjection at $\hbar\omega = 4.5$ eV from the Al-electrode using low electric fields ($\sim$ 0.5 MV/cm). After injecting electron densities of the order 10^{13} cm^{-2}, the photo I-V shifts were indicative of negative charge build-up in the oxide, but the resulting ΔV_{FB} was larger than could be accounted for by trapping from centers with cross sections $\lesssim 10^{-15}$ cm^2. It was concluded that part of this charge must be captured by coulombic-type centers, in view of the small injected-electron densities for which the charging occurs. The negative charge distribution and thus the corresponding trap distribution was shown to have a centroid close to the value found after charging the major trapping centers (as reported in Sec. V).

The only center detected in the ion implanted samples which was also present in the control sample was the 10^{-17}-cm^2 trap. Its density being considerably enhanced by the implantation, it is concluded that all centers reported here are related to the ion implantation treatment.

(ii) The fact that the total trap density for the major centers is not dependent upon implantation energy, is an indication that the primary damage caused by the implantation in the SiO_2 layer has been annealed out during the 1000°C treatment and that the trapping phenomena are closely related to the implanted ion species, rather than with residual damage.

(iii) An implantation with 1×10^{13} Al$^+$/cm^2 at 30 keV into 730 Å thick SiO_2 layers followed by a 1050°C anneal was previously reported to result in electron trapping [11]. The dominant cross sections in that experiment were at least an order of magnitude lower (1.26×10^{-16} cm^2 and 1.40×10^{-17} cm^2) which also indicates that the nature of the implanted ion strongly influences the trapping behavior. Moreover, in the case of the implanted Al$^+$ it was observed that the trap density was proportional to the implant energy and was not independent of the energy as was observed for As$^+$.

(iv) The sum of trap densities with cross sections in the range $10^{-15}-10^{-16}$ cm^2 is of the order $(0.7-1)\times$ the ion fluence. When the traps with cross section $1\text{-}4\times10^{-17}$ cm^2 are included, it follows that the total density of available traps can be larger than the fluence of implanted ions, indicating that every incoming ion is possibly able to generate more than one trapping site. However, this observation is critically dependent upon the value for the charge centroid $\bar{x}$ used to calculate N_T from the quantity N_{eff} resulting from the data reduction (Eq. 2). In our calculations we used a constant value for $\bar{x}$ for all centers determined at a particular implantation energy, which implicitly assumes that every trapping center has the same spatial distribution at a given ion energy. This assumption was experimentally verified as discussed in Sec. V-C-1.

(v) The initial trapping probability for injected electrons crossing the oxide is given by the product [17]

$$\eta(0) = \sigma_c N_T. \tag{8}$$

Since N_T is proportional to the ion fluence ϕ, it is useful to define a trapping probability per implanted ion $\eta(0)/\phi$ which yields the number of initially trapped electrons per injected electron and per ion present in the oxide. This ratio $\eta(0)/\phi$ for the dominant As^+ implantation related center is the highest encountered so far in an ion implanted oxide which received a high temperature anneal, suggesting concern for device applications involving As^+ implanted oxide layers, if charge trapping is not desired.

(vi) Field-ionization of trapped charge was investigated on sample AS4X with a 1274-Å thick SiO_2 layer implanted at 60 keV with 1×10^{13} As^+/cm^2. After avalanche injection up to $\Delta V_{FB} \approx 8$ V, the sample was stressed with $V_g = +40$ V, which is approximately equal to the maximum oxide voltage drop during avalanche injection. After a stressing period equa to 3 times the total avalanche-injection time only 7% of the charge was lost (as verified by photo I-V measurements before and after stressing),

which means that only a minor portion of the electrons is stripped off from the trapping sites during the avalanche charging process.

(vii) An avalanche charging experiment was carried out at 77K with a current of 9×10^{-11} A for wafer AS4Y, implanted with 1×10^{13} As^+/cm^2 at 60 keV. The density for the 1×10^{-15}-cm^2 trap was not noticeably higher than at room temperature, but the Coulombic-type trap density ($\sigma_c \gtrsim 10^{-15}$ cm^2) was slightly increased.

V. ANALYSIS OF PHOTO I-V DATA

A. General Results

Figures 6 and 7 show photocurrent measurements as a function of gate voltage for a typical sample with a positive and negative gate bias, respectively. Since the effect of avalanche injection charging is to introduce a parallel shift in the photo I-V characteristics over a large voltage range, it is concluded that the major portion of the charge is located in the bulk of the oxide, i.e. beyond the range of the potential maximum in the oxide at the injecting interface [20,21]. From the shifts of the photo I-V characteristics, the centroid $\bar{x}$ and the areal density Q of the trapped charge can be calculated using Eqs. 5 and 6. Flat-band voltage shifts after charging were nearly equal to the positive photo I-V voltage shift ΔV_g^+ for positive bias, as expected for bulk oxide charging [20,21].

B. Charge Distribution Centroid as a Function of Ion Energy

Figure 8 shows the centroid $\bar{x}$ of the negative-charge distribution after avalanche injection as a function of ion implantation energy [13]. Each point represents an average taken over several measurements. In the same figure, the solid line represents the theoretical values for the ion distribution centroids. These were computed from the tables of Gibbons, Johnson, and Mylroie [27], based on the theory of Lindhard, Scharff, and Schiøtt (LSS). The theoretical centroid values used in Fig. 8 differ from the tabulated values for the projected

range R_p since the density of thermal amorphous SiO_2 as used in our study is smaller than the density of single-crystal SiO_2 (as used in Ref. 27) by a factor of 0.84.

We included in Fig. 8 the centroid values calculated from experimentally determined As-distributions. For this purpose, As^+-ions were implanted with a fluence of 1×10^{14} cm^{-2} over the same energy range into 1400-Å thick thermal SiO_2 layers. The samples were analysed using a Cameca secondary-ion mass spectrometer (SIMS). An O_2^+ primary ion beam was used to sputter the surface while alternately monitoring the secondary $^{90}Si_2O_2^+$ and $^{91}AsO^+$ signals. The sputter-time scale was converted into depth in the SiO_2 by measuring the sputtered crater depth with a Talystep instrument (Taylor-Hobson) and calculating the sputtering rate in the SiO_2. Both the centroids determined from photo I-V measurements and those determined from the SIMS data are up to 40% larger than the theoretical values.

Figure 8 also includes the results of independent determinations of the ion distribution centroid using SIMS from Ref. 28 and He^+ backscattering (RBS) from Ref. 29. As seen in the figure, good agreement is found between all experimental results for the ion-distribution centroid and the photo I-V data for the trapped-charge distribution centroid.

It is concluded from the good agreement between the centroids obtained from photo I-V data and from experimentally determined (SIMS) profiles, that the charge distribution is closely tracking the implanted ion distribution. This conclusion was also drawn in previous studies for trapping related to implanted Al^+ and P^+ in SiO_2 after a 1000-1050°C anneal in N_2 for 30 min [13]. We believe that the high anneal temperatures used in our study allowed us to reduce the implantation related damage to a level where the nature of the implanted ion and its spatial distribution become the dominant features in the electron trapping phenomenon. Previous studies using a 1×10^{14} Al^+/cm^2 implantation at 20 keV without annealing [7] indicated that the trapped-charge centroid differed from the ion-distribution centroid, probably because the trapping occurred mainly at displacement damage sites.

The arsenic distribution profile was determined on two samples implanted with 80 keV As^+-ions, one without post -implantation anneal and one with a 1000°C anneal in nitrogen for 30 min. The impurity distributions were essentially identical, indicating that no detectable diffusion of the implanted arsenic in the SiO_2 layer occurs during our standard 1000°C anneal treatment. Figure 9 compares the profile calculated from LSS theory with the experimentally determined profile for an 80-keV As^+ implant into SiO_2. It is seen that the experimental profile, besides having a larger range, is slightly wider than the theoretical one.

C. Further Centroid Studies

1. Dependence on trapped charge density.

During reproducibility measurements of the charge centroid, samples implanted at various energies were charged up to varying flat-band voltage shifts. Within the small experimental error no dependence of the centroid on the charge level present in the oxide (in the range $4\times10^{11}-1\times10^{13}$ cm^{-2}) was found. Since during avalanche injection the centers with the largest capture cross section will be the first ones to fill to completion followed by those with smaller cross sections, the latter observation means that the respective negative charge distributions associated with their corresponding trapping centers have very similar centroids. This result has previously been alluded to in Sec. IV (iv).

2. Photodetrapping experiments.

The photo I-V techn que has also been used to ascertain that optical excitation removes trapped negative charge from the bulk of the oxide. This becomes clear from Figs. 10 and 11, where the photo I-V characteristics measured after successive detrapping steps are shown, for positive and negative gate bias, respectively. The photo I-V shift for positive gate bias ΔV_g^+ is seen to track closely the decreasing ΔV_{FB}-value during photodetrapping, which eliminate:

the generation of compensating positive charge at the Si-SiO_2 interface as a possible explanation for the back-shift of the C-V characteristics during a detrapping experiment.

The detrapping experiments are performed with zero gate bias, in order to avoid electron photo-injection from the contacts at photon energies greater than the SiO_2-Si(Al) energy barrier [30]. The internal fields in the SiO_2 layer due to the trapped negative charge build an additional potential barrier against electron injection. But the same internal fields favor hole injection, especially from the Si valence band. Tunneling injection of holes into the SiO_2 and recombination with the trapped negative charge could then be viewed as an explanation for the 'detrapping' experiments. At first sight, this model would not be in conflict with the observed one-to-one correspondence between ΔV_g^+ and ΔV_{FB}. However, the Si-SiO_2 interface with its high trapping probability for holes [31] is very likely to trap some of these injected holes, which would ultimately make ΔV_g^+ and ΔV_{FB} different. We then conclude that our detrapping experiments really involve the release of negative charge.

It was also investigated whether the negative charge which is removed during photodetrapping is the same charge which was trapped previously during avalanche injection. It could be conceived that in the uncharged sample compensating positive and negative charges are initially present and that, as the positive charge is being neutralized by injected electrons, an increasing amount of negative oxide charge emerges. In this case, the negative charge being removed during photodetrapping might <u>not</u> be the charge previously captured by the positive centers. The following experiment weakens this idea. An uncharged as-fabricated MOS capacitor on wafer AS4X was illuminated at 3.9 eV for $\approx$ 12 3/4 h at V_g = +21 V without showing an appreciable detrapping of supposedly compensated negative charge. It had been ascertained first that stressing at V_g = +21 V in the dark for $\approx$ 4 3/4 h had no effect on the V_{FB} of the MOS structure.

The observation that repetitive charging operations following optical discharging occur at the same rate [30], is also evidence against mutual screening of charged centers on a

macroscopic scale. An oxide with compensating positive and negative centers would be expected to show Coulomb-attractive electron trapping on the positive site for the first charging (with possibly some screening from the negatively charged sites), and neutral charging behavior thereafter, once the negative center was optically emptied.

Calculations of the charge centroid $\bar{x}$ after successive detrapping experiments show that the trapped negative charge is being removed in a homogeneous way, i.e. the centroid $\bar{x}$ is constant within the small experimental error, provided small portions of the charge are removed. When large portions of the charge are removed, optical interference effects become important and determine the charge centroid, particularly in the structures with thick oxides [30]. Short illuminations removing small charge portions would result in a varying charge centroid $\bar{x}$ if centers with different σ_p - values had different spatial distributions, since photodetrapping is favoring the depopulation of centers with the highest photoionization cross sections. The fact that $\bar{x}$ is essentially constant during photodepopulation is more support for our assumption that all trapping centers have approximately the same centroid.

3. Ion fluence dependence.

Table VI summarizes the charge centroid values for three samples implanted with As^+ fluences of 3×10^{12}, 1×10^{13}, and 1×10^{14} cm^{-2}, respectively, all charged by avalanche injection at a current of 5×10^{-10} A. There is no correlation seen between the ion fluence and the charge centroid. Although the initial trapping probability given by Eq. 8 is close to 10% for the major center in wafer AS7J implanted with 1×10^{14} As^+/cm^2, the centroid is not moving towards the Si-SiO_2 interface in that wafer.

4. Injection mechanism dependence.

Since, as discussed above, the initial trapping probability is large for sample AS7J implanted with 1×10^{14} As^+/cm^2, a check was made to determine whether the charge centroid

would be dependent on the injecting interface; i.e. whether the injected electrons would be trapped closer to the interface from which they originate. As an injection mechanism from the Al electrode, we used internal photoemission under negative gate bias. This experiment was also important in the light of our study reported elsewhere [30], in which photoinjection and photodetrapping of an As^+ implanted SiO_2 layer is the basis for an MOS type non-volatile memory device. The result of our centroid measurements after photoinjection from the Al gate is included in Table VI. After charging wafer AS7J at $V_g = -15$ V up to $\Delta V_{FB} \approx 7$ V and at $V_g = -30$ V up to $\Delta V_{FB} \approx 16$ V, the charge centroids $\bar{x}$ as measured from the Al-SiO_2 interface were found to be 540 Å, which is very close to the value found after avalanche injection.

5. Oxide thickness dependence.

Sample AS7M with a 490-Å thick SiO_2 layer was implanted with 1×10^{13} As^+/cm^2 at 20 keV. Within experimental error, the charge centroid was equal to the one found in sample AS7B with a 1414-Å thick SiO_2 layer implanted under the same conditions.

The observation that the centroid $\bar{x}$ is not smaller for the 490-Å thick SiO_2 layer than for the 1414-Å thick layer is more evidence for the fact that even with the thin oxide layer little if any implanted As is penetrating into the Si-substrate. The charge centroid in sample AS7M was also verified to be very stable during photodetrapping experiments.

6. Annealing dependence.

The charge centroid was measured after avalanche injection on wafers from 2 batches implanted at 40 and 80 keV, respectively, and annealed at 600, 800, and 1000°C. Within experimental error (at most 20-30 Å) the centroids for a particular energy coincide, indicating that any defect distribution, which were to move the trapped charge centroid towards the outer

oxide interface in an incompletely annealed sample, has been essentially removed by the 600°C anneal.

The experimental charge centroids for wafers AS7E (annealed at 1000°C for 2 h) and AS7F (annealed at 1100°C for 30 min) were respectively 455 and 463 Å. These values are very close to the 468 Å found after a 1000°C anneal for 30 min, which indicates that only minimal diffusion, if any, of the implanted As occurs during these extended anneal treatments.

Although the avalanche injection analysis of Sec. III-C showed that for a 1000°C anneal the distribution of trapping centers among the various capture cross sections depends on the anneal time, the trapping rate was found to saturate after a 30 min anneal in batch AS7. Moreover the charge centroid location was shown to saturate at anneal temperatures as low as 600°C. For all practical purposes we, therefore, adopted a 30 min anneal at 1000°C as a standard treatment.

7. Temperature dependence.

For a 60-keV implant, the charge centroid after avalanche charging at 83K was found to be identical to the room-temperature value.

VI. PHOTODETRAPPING RESULTS

As was described in Sec. V-C-2, the electrons trapped in As^+ related sites can be depopulated under illumination. It has been previously demonstrated that, by monitoring the flat-band voltage shift during optical detrapping, we can deduce information on two important parameters, the photoionization cross section σ_p and the optical trap depth $\Delta E_t = E_g - E_t$ [32]. The energy levels corresponding with the trap, E_t, and with the bottom of the conduction band, E_g, are measured with respect to the top of the valence band of the SiO_2. The structure in the wavelength dependence of the photoionization cross section is critically

dependent on oxide thickness for thicknesses above 500 Å due to the optical interference phenomenon [32]. Consequently, the experiments were repeated with thinner oxides (approx. 400 Å) which have a decreased oxide thickness sensitivity as shown by computer simulations. The main features of the analysis will be repeated here for clarity.

Assuming first-order kinetics and neglecting charge retrapping (which is reasonable in view of the small capture probability $\lesssim 10^{-3}$), the local depopulation of occupied traps under illumination is governed by the following equation:

$$\delta n_t(x,E,t)/\delta t = - F_p(x,\hbar\omega)\sigma_p(x,E,\hbar\omega)n_t(x,E,t) \tag{9}$$

where n_t is the trapped electron concentration per unit energy, F_p is the local photon flux in the SiO_2 layer, and σ_p is the trap photoionization cross section. The photon flux F_p is a function of both the photon energy $\hbar\omega$ and the position x in the SiO_2 layer (measured from the Al-SiO_2 interface) due to the optical interference phenomenon [33]:

$$F_p(x,\hbar\omega) = F_{p0}(\hbar\omega)F_{p1}(x,\hbar\omega) \tag{10}$$

where $F_{p0}(\hbar\omega)$ is the intensity spectrum for the xenon arc lamp and $F_{p1}(x,\hbar\omega)$ is the standing wave pattern in the oxide layer at photon energy $\hbar\omega$.

The photoionization cross section σ_p is a function of the trap energy level E in the SiO_2 band gap and of the photon energy $\hbar\omega$, since it includes the transition probability to a final state $E+\hbar\omega$, and may be position dependent i) through a position-dependent electric field due to the presence of charge in the SiO_2 layer, and ii) through spatially separated traps with different σ_p-versus-energy dependence. The field dependence of σ_p was experimentally shown to be negligible. The constant charge centroid for widely varying charge levels suggests similar spatial distributions for different traps.

Integrating Eq. 9 over the oxide thickness and over the energy gap of the SiO_2 then yields:

$$d/dt[\int_o^L \int_o^{E_g} n_t(x,E,t)dEdx] =$$

$$-\int_o^L \int_o^{E_g} F_p(x,\hbar\omega)\sigma_p(E,\hbar\omega)n_t(x,E,t)dEdx. \tag{11}$$

It is easily shown that Eq. 11 finally yields

$$d[\Delta V_{FB}(t)]/dt =$$

$$-\Delta V_{FB}(t)\int_o^L F_p(x,\hbar\omega)n_{t2}(x)dx\int_{E_g-\hbar\omega}^{E_g} \sigma_p(E,\hbar\omega)n_{t1}(E)dE \tag{12}$$

where the trapped electron concentration was written as

$$n_t = n_{t0}(t)n_{t1}(E)n_{t2}(x). \tag{13}$$

The separation of variables as performed in Eq. 13 is supported by the centroid determinations during a photodepopulation sequence as discussed in Sec. V-C-2. From those experiments, it followed that the centroid $\bar{x}$ of the charge distribution is constant in time, and that all trapping sites related to the ion implantation have the same spatial distribution. After very long discharging times, the centroid of any remaining trapped charge will shift towards a minimum in the standing wave pattern of the light [30]. Since the illumination interval is small compared to the discharging time constant as shown below, the interference effect can be disregarded and the depopulation is occurring homogeneously.

For the normalized spatial trap distribution $n_{t2}(x)$, a Gaussian profile was assumed with mean depth $\bar{x}$ as determined from photo I-V data and straggling as determined by the SIMS profiling measurements. Equation 12 is abbreviated as

$$d[\Delta V_{FB}(t)]/dt = -\Delta V_{FB}(t)\chi(\hbar\omega)\Sigma(\hbar\omega), \tag{14}$$

where $\chi(\hbar\omega)$ is the convolution of the photon flux with the spatial distribution of the trapping centers and $\Sigma(\hbar\omega)$ is the convolution of the photoionization cross section with the optically accessible trap distribution over energy. The latter quantity will be viewed as an effective photoionization cross section.

The solution to Eq. 14 is

$$\Delta V_{FB}(t) = \Delta V_{FB}(0)exp[-\chi(\hbar\omega)\Sigma(\hbar\omega)t]. \tag{15}$$

From Fig. 12, it follows that initially ΔV_{FB} is varying exponentially with time. It is also concluded that the typical discharging time of 5 min used in our experiment, is small compared to the discharging time constant. Therefore, Eq. 14 can be approximated by:

$$[\Delta V_{FB}(0)-\Delta V_{FB}(t)]/\Delta V_{FB}(0) = \chi(\hbar\omega)\Sigma(\hbar\omega)t. \tag{16}$$

This equation was used to determine the effective photoionization cross section $\Sigma(\hbar\omega)$. The quantity $\chi(\hbar\omega)$ can be calculated, knowing the sample geometry (layer thicknesses and ion range parameters) and the photon energy; $\Delta V_{FB}(0)-\Delta V_{FB}(t)$ is the measured reduction in flat-band voltage shift during the discharging interval t.

Figure 13 displays the effective photoionization cross section $\Sigma(\hbar\omega)$ measured at room temperature as a function of photon energy for a wafer implanted with 1×10^{13} As^+/cm^2 at 10 keV. In the calculation of $\chi(\hbar\omega)$ the spatial distribution $n_{12}(x)$ of the trapped charge has to be known. We assumed a Gaussian distribution with a centroid of 109 Å, as calculated from photo I-V data, and a theoretical standard deviation of 31 Å. These parameters do not have a major influence on the structure of the $\Sigma(\hbar\omega)$-spectrum since, as mentioned previously, it was verified from computer simulations that the optical interference is minimized in the oxide layer

with a thickness of approximately 400 Å. Note that the photoionization spectrum displays a broad maximum at approximately 5.2 eV.

The optical constants for the respective layers of the MOS structure used in the calculation of the standing wave pattern were tested as follows. The reflectivity for an MOS device with similar dimensions, only with a blanket aluminum evaporation over a large area, was measured over the entire photon energy range and was found to be in good agreement with the calculated reflectivity, using the optical constants for the respective layers. Finally, we also included the influence of the monochromator slit width upon the wavelength bandpass. This was shown to represent a minor effect for our experimental settings (full width at half maximum = 50 Å), only smoothing out the local oscillations in the calculated $\Sigma(h\omega)$-spectrum [34].

The accuracy with which the effective photoionization cross section can be obtained is ultimately determined by the incident photon flux measurement. Although extreme care was taken in assessing every factor involved, the absolute values can probably not be guaranteed to within better than a factor of two.

The effective photoionization cross section spectrum in the 3 to 5.5-eV range for a 1270-Å thick oxide film measured at 79K was also found to be very similar to the room temperature spectrum.

It has been suggested that one of the electron traps observed in As-implanted SiO_2 corresponds to the unaffected As 4p-level, found midway in the SiO_2 band gap for arsenic atoms at oxygen sites in the SiO_2 network [32]. This result is obtained from a tight-binding model for substitutional impurities in SiO_2. The photoionization threshold of 3.3 eV calculated from a least-squares fit to the linear portion of the spectrum in Fig. 13 is in excellent agreement with the theoretical photoionization threshold of 3.2 eV [35], which lends credibility to the model assuming substitutional arsenic on oxygen sites.

VII. THERMAL DETRAPPING

It has been demonstrated in the previous section that the trapped electron distribution is optically erasable with photons of energy above 4 eV. We also investigated whether an equivalent thermal activation can remove electrons from arsenic-related trapping sites in the oxide.

Assuming first order kinetics, thermal detrapping for a single-level trap obeys the following equation:

$$d(\Delta V_{FB})/dt = - p\Delta V_{FB}. \tag{17}$$

The detrapping probability p is expressed as:

$$p = s \exp (- E_a/kT) \tag{18}$$

where s is the frequency factor in the case where retrapping is negligible, E_a the thermal activation energy (or thermal trap depth), k Boltzmann's constant, and T the absolute temperature. Under those assumptions, the flat-band voltage shift $\Delta V_{FB}(t)$ during thermal detrapping then obeys the relationship:

$$ln[\Delta V_{FB}(0)/\Delta V_{FB}(t)] = st \exp (- E_a/kT). \tag{19}$$

The experiments pertaining to thermal detrapping are now reported and discussed.

(i) Several capacitors from wafer AS4Y, implanted with 1×10^{13} As^+/cm^2 at 60 keV, were charged up to $\Delta V_{FB} \approx 5.8$ V. For every temperature a freshly charged capacitor was used. The flat-band voltages were successively measured at room temperature after isothermal detrapping with zero gate bias. The evolution of ΔV_{FB} at successive

temperatures is shown in Fig. 14, where the abscissa indicates the cumulative time at high temperature. In Fig. 15 these data are replotted to check whether the discharging can be described by Eq. 19. If the thermal discharging kinetics were of the first order and there were only one activation energy over the whole measurement interval, all data points of Fig. 15 would follow straight lines. It is seen that this only holds for very short times (<5 min).

Assuming that a first-order process with a single activation energy holds for short times, an average activation energy E_a = 0.38 eV was calculated, with a standard deviation of 0.09 eV. In order to observe such a low activation energy over a temperature range from 100 to 250°C, a very low frequency factor s has to be invoked. We indeed found values for s ranging from 10^2 to 10^3 s^{-1}; these values differ widely from the atomic vibration frequency (10^{12}–10^{13} s^{-1}) and are hard to account for. At this point, a multi-step discharging process could possibly be speculated upon to explain both the small activation energy and the small frequency factor.

(ii) Photo I-V data confirmed that removal of negative charge in a homogeneous fashion (i.e. with constant charge centroid) is involved in thermal detrapping. Avalanche injection charging provided additional information. After an avalanche injection run on a sample from wafer AS4Y (60 keV, 1×10^{13} As^+/cm^2) mainly filling the 10^{-15}-cm^2 trap up to ΔV_{FB} = 8.7 V, this shift was thermally reduced (at 200°C for 1 min with V_g = 0 V) to $\Delta V_{FB} \approx 5$ V. A second avalanche injection run then initially proceeded at the expected charging rate for a 10^{-15}-cm^2 trap and yielded the same saturated ΔV_{FB}-value (calculated from N_{eff}) as the first run, indicating that the thermal treatment does not annihilate trapping sites, but merely empties them.

(iii) The effect of the electric field in the oxide on the isothermal detrapping phenomenon was also considered. It was verified that neither an increase in the internal oxide fields (by increasing the charge level in the sample from 1 to 2×10^{12} cm^{-2}, which increases

the band bending in the oxide), nor a moderate increase in the external field (from 0 to 2.4 MV/cm) enhanced the detrapping rate.

(iv) The isothermal detrapping characteristics appear to be dependent on the nature of the implanted ion. Electrons trapped on both ion implanted tungsten (1×10^{13} cm^{-2} implant at 60 keV; anneal at 1050°C in N_2 for 30 min) and evaporated tungsten (sandwiched between thin thermal SiO_2 and CVD SiO_2 [36]) require temperatures up to 200°C to initiate any detectable detrapping. In Ref. 36 an activation energy of 0.9 eV was calculated; assuming a monoenergetic trap, a frequency factor $s \approx 10^5$ s^{-1} follows.

The observation that the detrapping process depends on the nature of the impurity indicates that the release of trapped electrons is involved and <u>not</u> the thermal activation of holes and subsequent annihilation of the trapped electrons by recombination. It seems that such a process would be independent of the impurity species.

(v) Thermally stimulated current (TSC) measurements were performed on similar As^+-implanted samples from room temperature to 400°C using a hyperbolic heating rate,

$$1/T = 1/T_0 - at, \tag{20}$$

where T is the absolute temperature, T_0 is the initial temperature, a is a proportionality constant, and t is time [24]. The current related to the discharging phenomenon showed a threshold at about 60°C and a broad maximum around 220°C.

Attempts to fit the data to a model assuming higher-order kinetics were unsuccessful. Using a first-order model and a monoenergetic trap, the same low values for E_a and s resulted, as found above from the isothermal detrapping measurements.

However, as seen in Fig. 16, the broad discharging-current–versus–temperature curve could be accounted for by assuming a Gaussian distribution of traps with a median energy E_m = 1.2(3) eV and a standard energy deviation ΔE = 0.2 eV. At present, it is not clear whether the increasing current beyond 290°C is due to an additional deeper trap distribution or to enhanced conduction in the sample.

A frequency factor $s = 10^{12}\ s^{-1}$ was chosen arbitrarily, but the obtained fit was only weakly affected by varying s over the range $10^{11}-10^{13}\ s^{-1}$. Note that the value used for s is of the same order as the atomic vibration frequencies. It is, therefore, believed that the description in terms of detrapping from centers with a spread in activation energies is realistic. A similar conclusion was reached in Ref. 37 which studied the kinetics associated with the release of mobile ions from traps in MOS-structures.

The median thermal trap energy of 1.2 eV is also in line with the expectations from the optical absorption spectrum with a threshold of 3.3 eV and a broad maximum around 5.2 eV [38].

VIII. DISCUSSION

Reports of the electrical effects of ions implanted into SiO_2 as studied in this work, are scarce in the literature. But the nature of the structural damage in SiO_2 upon implantation and its annealing behavior have been explored using a variety of techniques: interferometric and photoelastic methods [39], ellipsometry combined with IR-absorption [40,41], optical absorption in the visible and UV range of the spectrum [42], ESR [43,44], and the cantilever beam technique [45]. Although details may be different, the general conclusion appears to be that atomic displacement effects disappear in a temperature range from 600°C to the oxide growth temperature. Moreover, the lowest anneal temperature is observed when the displacement damage in the oxide has reached a saturation value. The volume density of deposited displace-

ment energy necessary to achieve saturation was found in Ref. 45 to be approximately 10^{20} keV/cm^3. Since the energy deposition for a 10^{13}-As$^+$/cm^2 implant is of this order-of-magnitude [46], it is believed that the major portion of the structural damage is removed from our oxides after an anneal at temperatures as low as 600°C. This might explain the constant charge distribution centroid found for all higher anneal temperatures. Whether the decreasing trapping rate for increasing anneal temperatures above 600°C is due to the removal of remnant secondary damage or to a gradual relocation of the As-atoms in the SiO_2-network from active to inactive sites is not known, since the structural damage and/or the local atomic environment were not directly investigated.

The observation that the trap density after arsenic implantation is independent of ion energy, as opposed to aluminum implantation [11], is possibly also related to the energy deposited into atomic collisions. It follows from the observations of Ref. 45 that the displacement damage per unit volume in the SiO_2 increases linearly with the volume density of deposited energy in atomic collisions up to a threshold volume density. Also, to a first-order approximation the volume density of deposited energy is a function only of the implanted ion and the ion fluence. Since for equal ion fluences the volume density of deposited energy in atomic collisions is smaller for aluminum than for arsenic ions, the displacement damage will be smaller for Al than for As. As discussed earlier, we assume that displacement of oxygen atoms is necessary to allow implanted ions to occupy their most effective trapping sites. It is suggested that for low-energy Al-implants, the volume ion density is too high compared to the damage density in order to incorporate all ions into their most effective trapping sites. With increasing energy the volume ion density decreases and a larger fraction of the total ion fluence will be accomodated into the SiO_2-network, yielding a trap density depending on energy. For implanted arsenic, it is suggested that the displacement damage density is high enough to incorporate a fixed fraction of the 10^{13}-cm^{-2} ion fluence into the more effective trapping sites, regardless of ion energy.

The amount of active electron trapping sites was found to be proportional and (at least for fluences up to 10^{13} cm^{-2}) nearly equal to the implanted arsenic fluence. Moreover, the location of the charge distribution centroid after charging the electron traps was found to be proportional to the implanted-ion energy and in excellent agreement with the experimentally determined ion distribution centroid. These observations lend credibility to our assumption that the electron trapping phenomenon is directly related to the implanted ions.

The results of other experiments performed in this laboratory, which will be reported in forthcoming publications, shed more light on the present work. Although the atomic masses of aluminum and phosphorus are nearly identical, it has been observed that these ions exhibit considerably different electron trapping behavior after high-temperature annealing. It is thus concluded that the nature of the implanted ions is of prime importance in determining the electron trapping characteristics, regardless of the exact physical origin of the trapping sites.

The negative charge trapped in the oxide on As-related sites was shown to be removable both optically and thermally. From the photodetrapping experiments, an effective photoionization cross section has been determined as a function of photon energy, with a threshold of 3.3 eV. It has been argued that this is corroborated by a simple model assuming that the implanted As-ions are incorporated into the SiO_2-network at oxygen sites. There is evidence for the creation of oxygen-vacancies in SiO_2 during ion implantation from optical absorption [42], ESR [43], and from the detection of recoiled oxygen atoms near the Si-SiO_2 interface [47].

At this point, it would be of value to apply some of the analytical techniques mentioned earlier (ESR, IR-absorption, ...) to investigate the local atomic environment of the implanted ions after successive annealing steps. Nevertheless, neither the experimental procedure nor the analysis involved seem to be straightforward for such a dilute doping in an amorphous matrix.

IX. CONCLUSIONS

The electron trapping properties in well-annealed (usually at 1000°C in N_2 for 30 min) As^+ implanted SiO_2 layers in MOS structures have been studied using mainly avalanche injection and photocurrent-versus-voltage measurements.

After a 1×10^{13}-As^+/cm^2 implant, trapping centers with various capture cross sections were found. A small density of coulombic-type traps ($0.5-7\times10^{11}$ cm^{-2}) with a capture cross section in the range $0.4-1.6\times10^{-14}$ cm^2 was found from the avalance injection analysis in most samples (at electric fields of 3-4 MV/cm). The sum of the dominant trap densities with cross sections in the range $10^{-15}-10^{-16}$ cm^2 is equal to 0.7–1 times the ion fluence, independent of ion energy, avalanche injection current density, and oxide thickness over the ranges used in our study. The dominant trap densities were found to scale with ion fluence. Annealing at increasing temperatures from 600 to 1100°C gradually reduces the electron trapping rate with some irreproducibility from run to run at the highest anneal temperatures. Centers with cross sections in the range $1-4\times10^{-17}$ cm^2 were also present in some of the control samples, but their density was considerably enhanced in the implanted samples.

The centroid of the negative charge distribution as measured from the Al-SiO_2 interface was found to be proportional to the implantation energy. The trapped charge density, ion fluence, injection mechanism, oxide thickness, anneal temperature, and ambient temperature did not influence the charge centroid over the ranges used in our study. Excellent agreement was found between the charge distribution centroids and the ion distribution centroids as determined by SIMS, but both were found to be larger than predicted by LSS-theory (up to 40%).

Photodetrapping was shown to proceed in a homogeneous way, i.e. leaving the charge centroid unchanged, provided optical interference effects are considered. From flat-band voltage shift measurements during photodetrapping at successively increasing photon energies,

an effective photoionization cross section was determined, which is the convolution of the photoionization cross section with the optically accessible trap density in the energy gap of the SiO_2. The experimental optical absorption threshold of 3.3 eV is in agreement with the threshold calculated from a model which assumes that the electron trapping is related with the implanted As-atoms incorporated substitutionally into the SiO_2-network at O-sites.

Isothermal detrapping experiments have been reported showing that the electrons trapped at As-related sites can be thermally released. The thermally stimulated current measurements could be described assuming a frequency factor of the order $10^{11}-10^{13}$ s^{-1} and a spread in activation energy $\Delta E = 0.2$ eV around a median energy $E = 1.2$ eV. This value is in accord with the expectations from the reported photoionization spectrum.

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TABLE I

Trapping parameters as a function of implant energy.

All samples were implanted with 1×10^{13} As^+/cm^2 and annealed in nitrogen at 1000°C for 30 min.

The resolution for the data in parentheses is poor.

Sample	E	L	$\bar{x}$	σ_{c1}	N_{T1}	σ_{c2}	N_{T2}	σ_{c3}	N_{T3}	σ_{c4}	N_{T4}
	(keV)	(Å)	(Å)	(cm^2)	(cm^{-2})	(cm^2)	(cm^{-2})	(cm^2)	(cm^{-2})	(cm^2)	(cm^{-2})
AS7A	10	1371	123	$(4.3\times10^{-15}$	$7.4\times10^{11})$	1.6×10^{-15}	2.0×10^{12}	1.5×10^{-16} 5.4×10^{-16}	2.5×10^{12} 3.6×10^{12}	3.7×10^{-17}	6.9×10^{12}
AS7B	20	1414	204	---[a]	---[a]	$0.9\text{-}1.3\times10^{-15}$	2.7×10^{12}[b]	2.0×10^{-16}	4.8×10^{12}	2.4×10^{-17}	4.8×10^{12}
AS7B[c]				---[d]	---[d]	---[d]	---[d]	2.9×10^{-16}	3.8×10^{12}	$0.9\text{-}3\times10^{-17}$[e]	5.5×10^{12}
AS7C[f]	40	1416	315	$(1.2\times10^{-14}$	$1.6\times10^{11})$	1.2×10^{-15}	4.6×10^{12}	1.8×10^{-16}	4.9×10^{12}	---	---
AS7D[f]	60	1433	468	$(5.8\times10^{-15}$	$3.0\times10^{11})$	1.8×10^{-15}	1.8×10^{12}	4.6×10^{-16}	5.7×10^{12}	---	---
AS4X[f]	60	1274	465	$(4.8\times10^{-15}$	$2.0\times10^{11})$	1.4×10^{-15}	3.8×10^{12}	3.7×10^{-16}	2.9×10^{12}	---	---
AS7G[f]	80	1415	571	$(1.4\times10^{-14}$	$5.6\times10^{10})$	1.7×10^{-15}	4.6×10^{12}	---	---	---	---
AS7H[f]	100	1415	630	$(1.6\times10^{-14}$	$8.9\times10^{10})$	1.8×10^{-15}	5.6×10^{12}	---	---	---	---

a) No evidence for a coulombic-type center was obtained.

b) The majority of the trapping centers appear with $\sigma_c = 0.9\times10^{-15}$ cm^2.

c) Separate measurement at 120°C with avalanche current density $j = 10^{-6}$ A/cm^2.

d) Data for these centers have been omitted since the resolution was poor due to the large current density.

e) Two centers were resolved, with σ_c of 0.9 and 3×10^{-17} cm^2, respectively. N_{T4} is the sum for both centers.

f) The centers for which entries are missing could not be detected due to V_{FB} exceeding the limits of the measuring equipment before a sufficient injected-electron density was obtained.

TABLE II

Trap parameters for a control sample that received all the processing steps, except for the ion implantation.

The avalanche injection was performed at 120°C with $j = 10^{-5} A/cm^2$.

L (Å)	σ_{c1} (cm^2)	N_{T1} (cm^{-2})	σ_{c2} (cm^2)	N_{T2} (cm^{-2})
491	$(1.5-2.6)\times10^{-17}$	6.2×10^{11}	3.0×10^{-18}	3.8×10^{12}

TABLE III

Trapping parameters as a function of As^+ ion fluence at a fixed energy of 80 keV.

The data for the coulombic-type center are not reported.

The centers for which entries are missing could not be detected (see footnote f in Table I).

Sample	L (Å)	$\bar{x}$ (Å)	Ion Fluence (cm^{-2})	σ_{c1} (cm^2)	N_{T1} (cm^{-2})	σ_{c2} (cm^2)	N_{T2} (cm^{-2})	σ_{c3} (cm^2)	N_{T3} (cm^{-2})
			Avalanche injection current $I = 5\times10^{-10}$ A						
AS7I	1423	535	3×10^{12}	9.2×10^{-16}	1.3×10^{12}	2.9×10^{-16}	1.1×10^{12}	3.7×10^{-17}	2.3×10^{12}
AS7G	1415	571	1×10^{13}	1.3×10^{-15}	5.7×10^{12}	---	---	---	---
			Avalanche injection current $I = 3\times10^{-11}$ A						
AS7J	1405	525	1×10^{14}	2.3×10^{-15}	4.3×10^{13}	---	---	---	---

TABLE IV

Trapping parameters as a function of annealing treatment after a 1×10^{13} As^+/cm^2 implant.

The data for the coulombic-type center are not reported.

The centers for which entries are missing could not be detected (see footnote f in Table I).

Wafer	Ion Energy (keV)	Anneal	σ_{c1} (cm^2)	N_{T1} (cm^{-2})	σ_{c2} (cm^2)	N_{T2} (cm^{-2})	σ_{c3} (cm^2)	N_{T3} (cm^{-2})
AS2D	80	600°C-30 min.	2.2×10^{-15}	8.7×10^{12}	---	---	---	---
AS2E	80	800°C-30 min.	1.5×10^{-15}	7.9×10^{12}	---	---	---	---
AS2F	80	1000°C-30 min.	9.3×10^{-16}	7.7×10^{12}	---	---	---	---
AS7E	60	1000°C-2 hrs.	1.2×10^{-15}	7.5×10^{12}	---	---	---	---
AS7F	60	1100°C-30 min.	1.1×10^{-15} 5.5×10^{-16}	1.3×10^{12} 2.0×10^{12}	1.8×10^{-16}	5.9×10^{11}	5.1×10^{-17}	2.7×10^{12}

TABLE V

Trapping parameters for a wafer with L = 490 Å implanted with 1×10^{13} As^+/cm^2 at 20 keV.

Data for the coulombic-type trap have been omitted.

$\bar{x}$ (Å)	σ_{c1} (cm^2)	N_{T1} (cm^{-2})	σ_{c2} (cm^2)	N_{T2} (cm^{-2})	σ_{c3} (cm^2)	N_{T3} (cm^{-2})
190	9.8×10^{-16}	4.4×10^{12}	2.4×10^{-16}	1.0×10^{12}	7.1×10^{-17}	4.8×10^{12}

TABLE VI

Charge distribution centroid as a function of ion fluence.

All samples were implanted at 80 keV.

Sample	L (Å)	As^+ fluence (cm^{-2})	Injection mechanism	$\bar{x}$ (Å)
AS7I	1423	3×10^{12}	A[a]	535
AS7G	1415	1×10^{13}	A	570
AS7J	1405	1×10^{14}	A	510
			P[b]	540

[a] A = avalanche injection from the Si substrate at $I = 5\times10^{-10}$ A.

[b] P = photoinjection from the Al gate at 4.5 eV photon energy with $I = 1\text{-}2\times10^{-11}$ A.

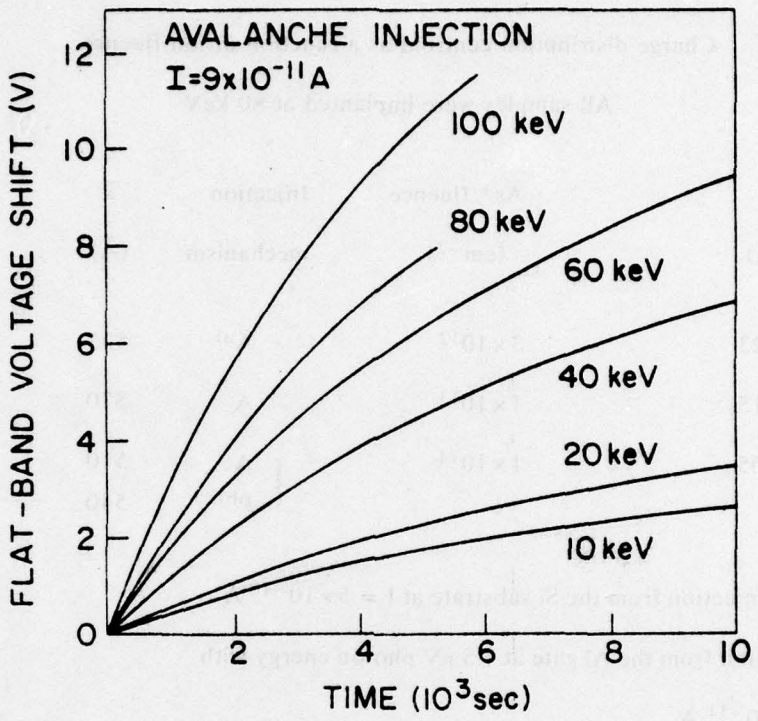


Fig. 1 Flat-band voltage shift as a function of time during avalanche injection at a current $I = 9\times10^{-11}$ A for various implantation energies. All samples (from batch AS7) were implanted with 1×10^{13} As^+/cm^2, have an average oxide thickness of 1410 Å and were annealed in N_2 for 30 min at 1000°C.

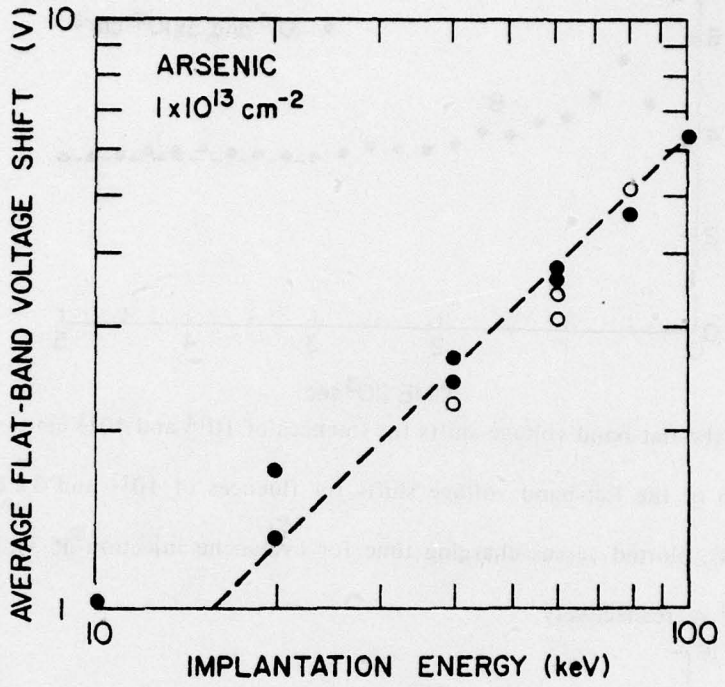


Fig. 2 Log-log plot of the average flat-band voltage shift, taken to 5264 s, as a function of implantation energy. All samples were charged at 9×10^{-11} A. The average ΔV_{FB} is calculated as the sum of all shifts (measured after equally spaced time intervals) divided by the number of measurements. The solid circles represent data from batch AS7. The open circles are data collected from various other batches.

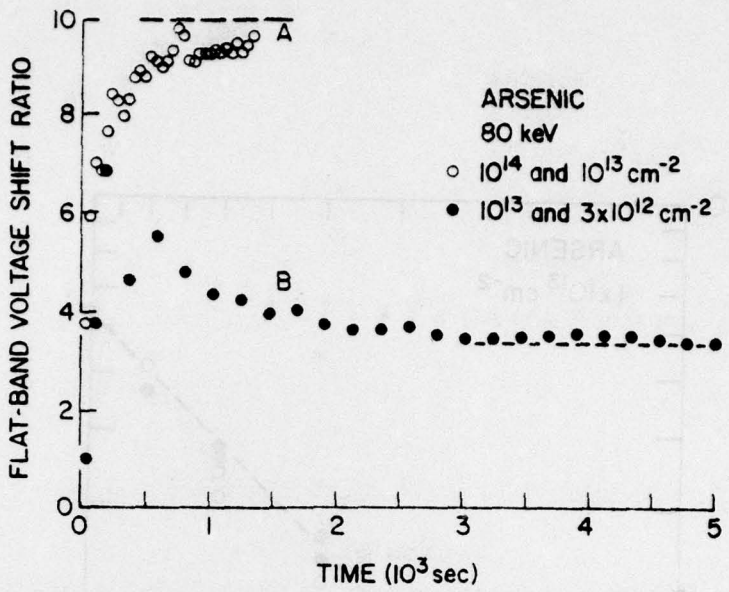


Fig. 3 Ratio of the flat-band voltage shifts for fluences of 10^{14} and 10^{13} cm^{-2} (curve A) and ratio of the flat-band voltage shifts for fluences of 10^{13} and 3×10^{12} cm^{-2} (curve B), plotted versus charging time for avalanche injection at 3×10^{-11} and 9×10^{-11} A, respectively.

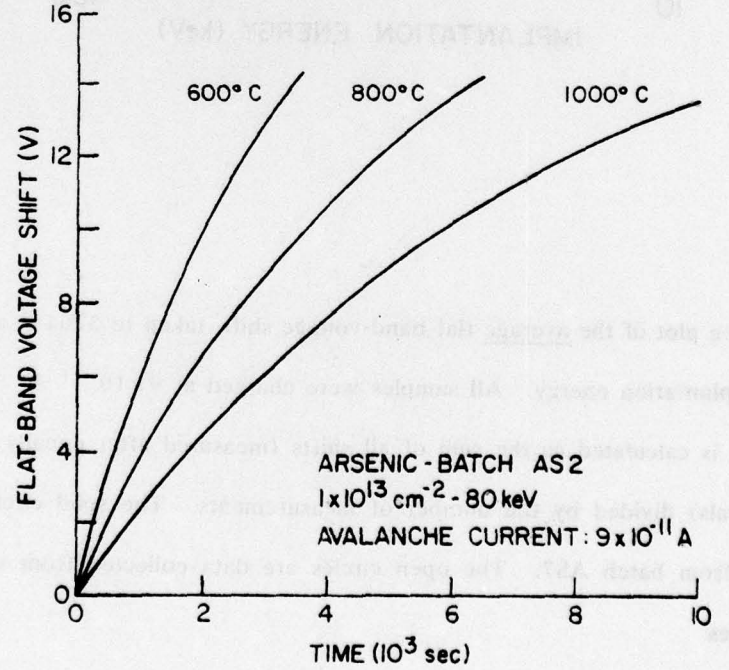


Fig. 4 Flat-band voltage shift versus time during avalanche injection at $I = 9\times10^{-11}$ A. The samples have an oxide thickness of approx. 1360 Å, were implanted with 1×10^{13} As$^+$/cm^2 at 80 keV and annealed in N_2 for 30 min at the respective temperatures.

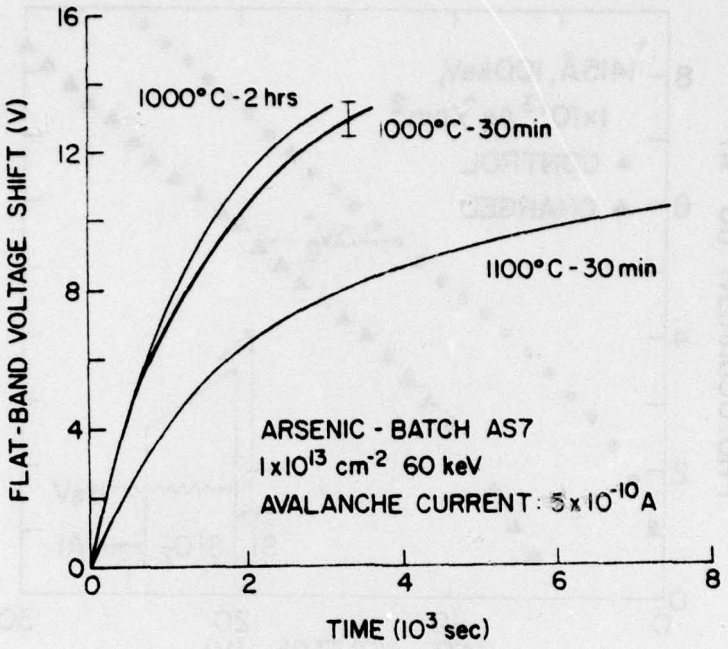


Fig. 5 Flat-band voltage shift versus time during avalanche injection at $I = 5 \times 10^{-10}$ A. The samples have an oxide thickness of approx. 143 Å, were implanted with 1×10^{13} As^+/cm^2 at 60 keV and annealed as shown. The error bar indicates the measured spread in ΔV_{FB} across the sample.

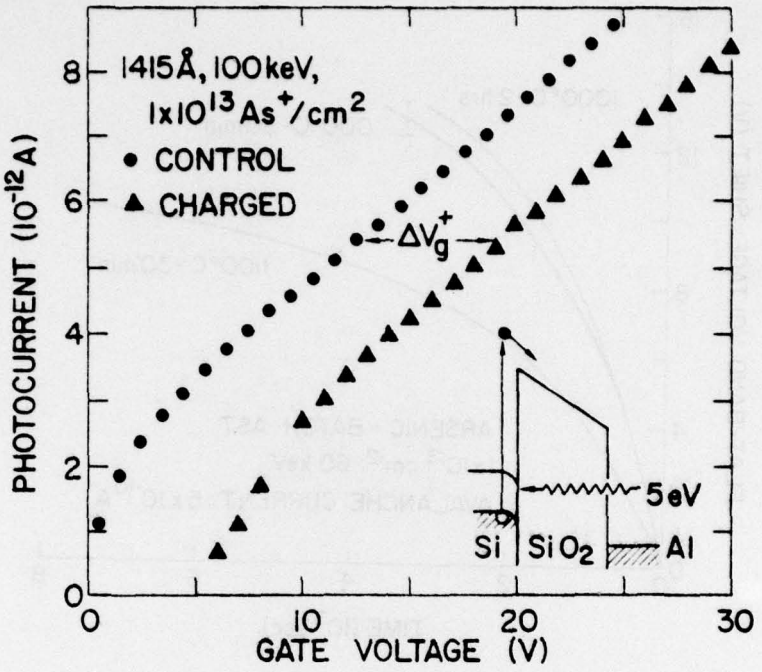


Fig. 6 Photocurrent as a function of applied gate voltage for positive bias before (solid circles) and after (solid triangles) partial charging of the As-related traps by in situ avalanche injection. The sample was annealed in N_2 for 30 min at 1000°C after implantation. The insert shows the energy band diagram for the uncharged MOS structure. Photon energy for the photo I-V measurements is 5 eV and the Si is the injecting electrode. $\Delta V_g^+ = 6.78 \pm 0.12$ V; $\Delta V_{FB} = 6.3 \pm 0.3$ V.

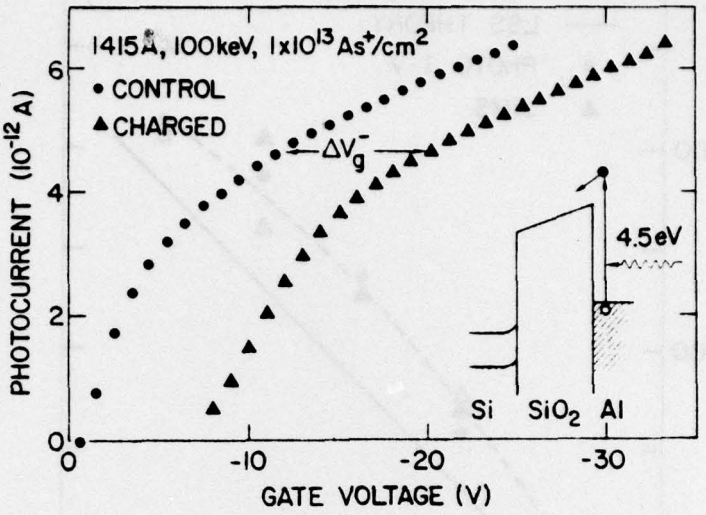


Fig. 7 Photocurrent as a function of applied gate voltage for negative bias before (solid circles) and after (solid triangles) partial charging of the As-related traps by <u>in situ</u> avalanche injection for the same sample as in Fig. 6. Photon energy for the photo I-V measurements is 4.5 eV and the Al is the injecting electrode. $\Delta V_g^- = -8.05 \pm 0.11$ V; from ΔV_g^+ (Fig. 6) and ΔV_g^- values, $\bar{x} = 647$ Å and $Q/e = -2.2 \times 10^{12}$ cm^{-2} are calculated (Eqs. 5 and 6).

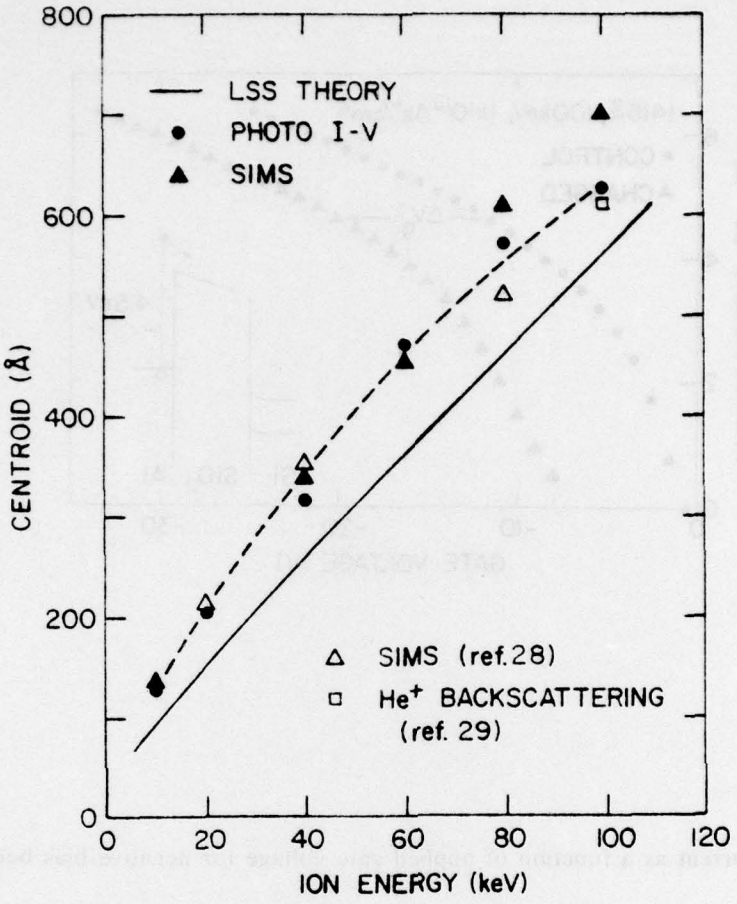


Fig. 8 Experimental charge distribution centroid (from photo I-V data), experimental ion distribution centroid (from SIMS and RBS), and theoretical ion distribution centroid (from LSS theory) as a function of ion energy. The wafers in our experiments have an average oxide thickness of 1410 Å, were implanted with 1×10^{13} As^+/cm^2 (for photo I-V) or 1×10^{14} As^+/cm^2 (for SIMS) and annealed in N_2 for 30 min at 1000°C. The SIMS results from Ref. 28 are for 5×10^{14}-As^+/cm^2 implants. The He^+ backscattering result is for a 1×10^{16} As^+/cm^2 implant at 100 keV (Ref. 29).

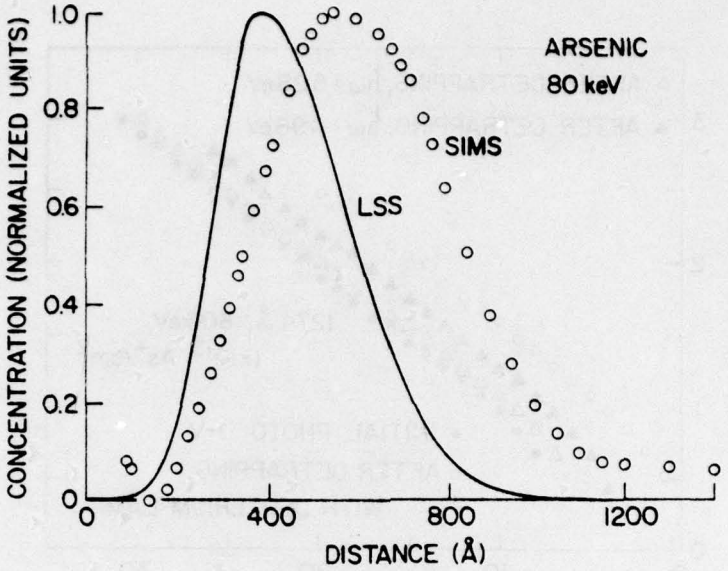


Fig. 9 Experimental (SIMS) and theoretical (LSS) profiles in normalized units for an 80-keV As^+ implant in SiO_2. The wafer used for SIMS was implanted with a fluence of 1×10^{14} ions/cm^2 and annealed in N_2 at 1000°C for 30 min. Standard deviation ΔR_p (LSS) = 148 Å; ΔR_p (SIMS) = 233 Å.

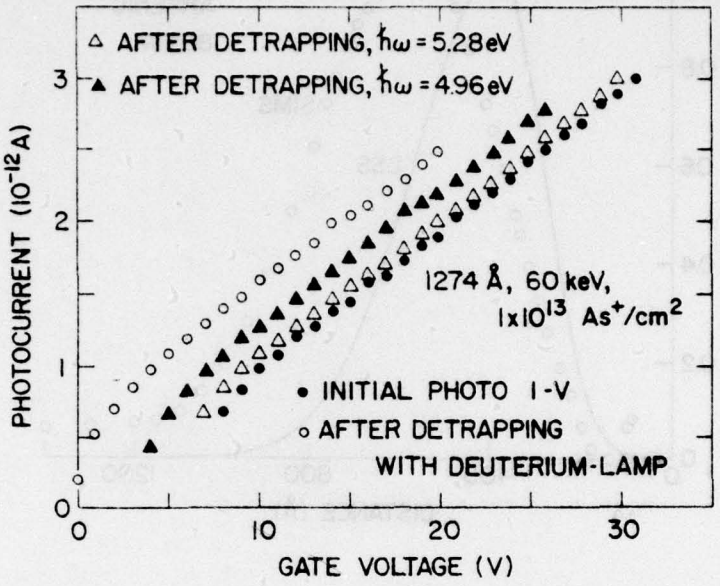


Fig. 10 Photocurrent for 5-eV light as a function of applied gate voltage for positive bias for a sample initially charged by avalanche injection to ΔV_{FB} = +8.5 V, reduced to ΔV_{FB} = 7.8 V after a photoionization cross section measurement (see Section VI), at successive stages of a detrapping sequence:

A. (solid circles) initial photo I-V.

B. (open triangles) after partial photodetrapping with V_g = 0 V at a photon energy of 5.28 eV for 298.5 min.; ΔV_{FB} = 6.7 V.

C. (solid triangles) after further photodetrapping with V_g = 0 V at a photon energy of 4.96 eV for 908.5 min; ΔV_{FB} = 4.9 V.

D. (open circles) after further photodetrapping at V_g = −1 V with the whole spectrum of a deuterium-lamp (cut off with a filter at ~ 5.5 eV) for 90 min; ΔV_{FB} = 1.1 V.

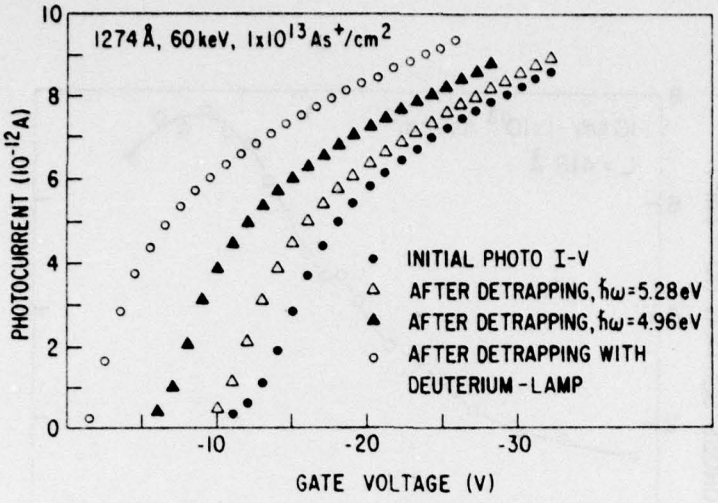


Fig. 11 Photocurrent for 4.5-eV light as a function of applied gate voltage for negative bias for the same sample as in Fig. 10. The symbols have the same meaning as in Fig. 10.

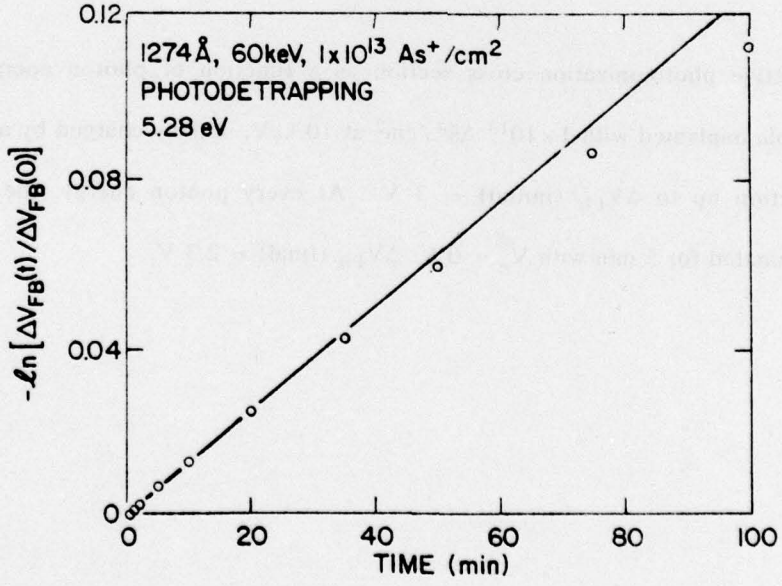


Fig. 12 Negative natural logarithm of the ratio $\Delta V_{FB}(t)/\Delta V_{FB}(0)$ as a function of time during photodetrapping at $\hbar\omega$ = 5.28 eV from an initial flat-band voltage shift ΔV_{FB} = 7.5 V. The linear fit through the initial portion of the data is characteristic for exponential discharging with a time constant of 800 min.

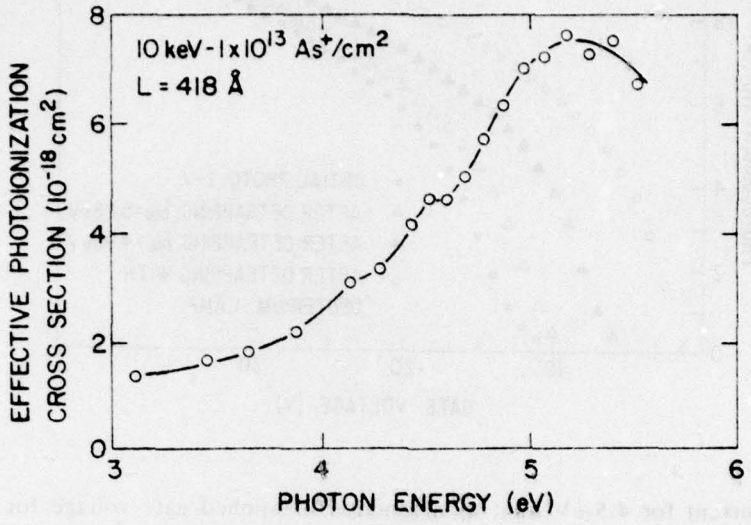


Fig. 13 Effective photoionization cross section as a function of photon energy for a sample implanted with 1×10^{13} As^+/cm^2 at 10 keV, initially charged by avalanche injection up to ΔV_{FB} (initial) = 3 V. At every photon energy, the MOS is illuminated for 5 min with V_g = 0 V; ΔV_{FB} (final) = 2.3 V.

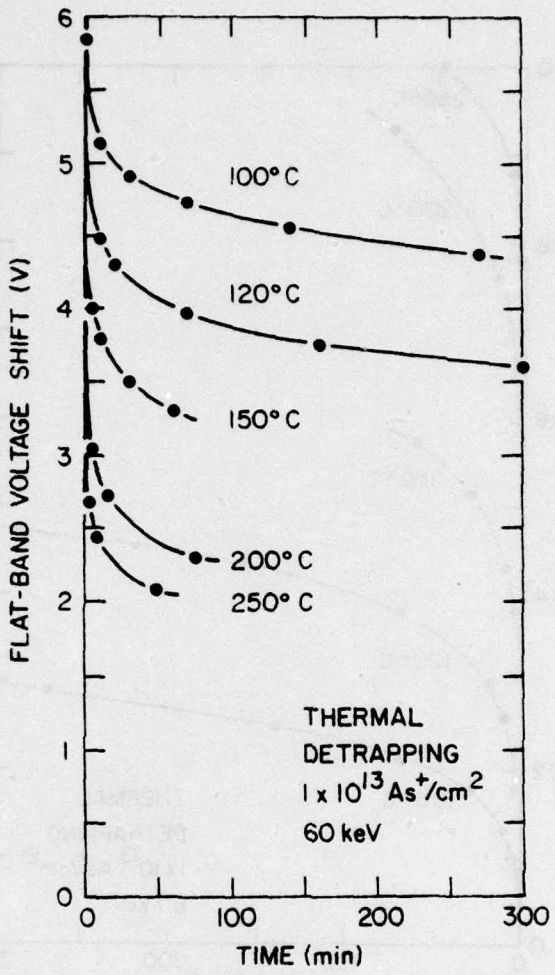


Fig. 14 Flat-band voltage shift versus time during isothermal detrapping for samples from wafer AS4Y implanted at 60 keV with 1×10^{13} As^+/cm^2. All samples were charged with $I = 2\times10^{-10}$ A up to ΔV_{FB} (initial) $\approx$ 5.8 V. The abscissa shows cumulative times spent at the indicated temperatures with zero gate bias after a 1 to 3 min warm-up. The samples are cooled to room temperature to perform the V_{FB}-measurements.

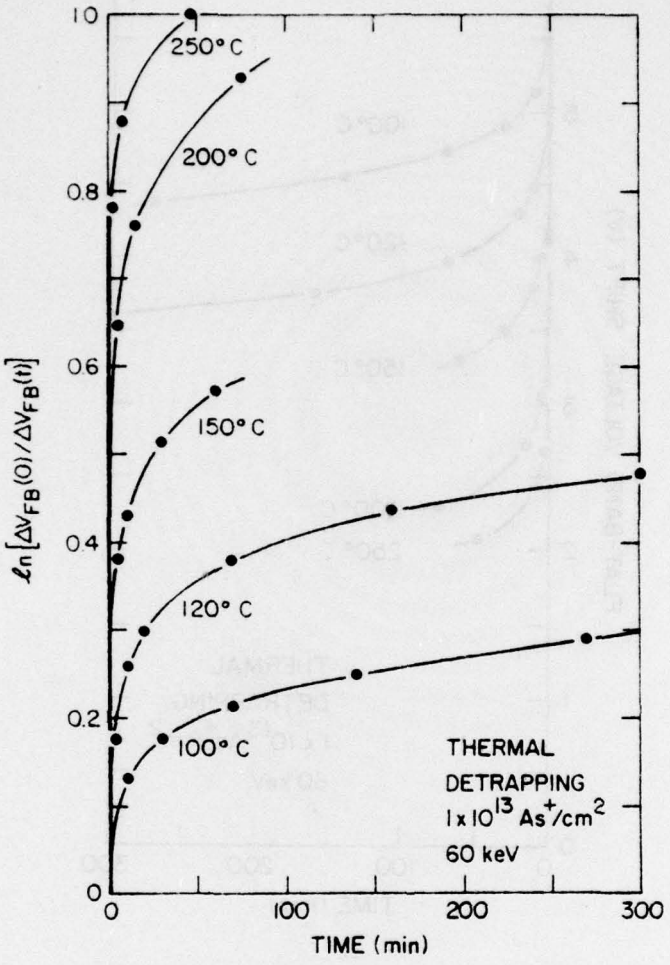


Fig. 15 Natural logarithm of the ratio $\Delta V_{FB}(0)/\Delta V_{FB}(t)$ versus cumulative time during isothermal detrapping, obtained by converting the data of Fig. 14.

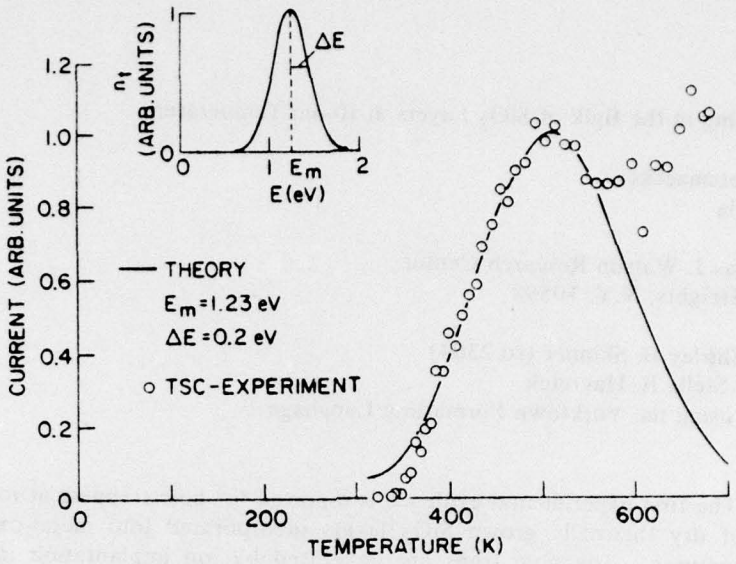


Fig. 16 Current (in arbitrary units) measured in the external cricuit during a TSC-experiment as a function of absolute temperature with $V_g = -9.07$ V(open dots). The background current measured during a second heating has been subtracted from the data. The sample was from wafer AS4Y (same as in Fig. 14 and 15) and was initially charged with an avalanche current $I = 9\times10^{-10}$ A for 1500 sec to $\Delta V_{FB} \simeq 11$ V, which was reduced to $\Delta V_{FB} \simeq 1$V after the TSC-experiment. The solid line is a fit of the first current peak with the sum of individual current contributions from a Gaussian distribution of traps with spread $\Delta E = 0.2$ eV in activation energy around $E_m = 1.23$ eV (as shown in the inset). The frequency factor used in the fit is 10^{12} s^{-1}.

Hole Trapping in the Bulk of SiO_2 Layers at Room Temperature

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Abstract: The first experimental evidence is reported for hole trapping at room temperature in the bulk of dry thermally grown SiO_2 layers incorporated into metal-oxide-semiconductor (MOS) structures. The hole traps are generated by ion implantation into the SiO_2 layer followed by a high temperature anneal. Hole avalanche injection from the n-type Si-substrate is used to introduce holes into the SiO_2. Electron internal photoemission (photo I-V) measurements are used to locate the trapped positive charge. The magnitude of the cross-over voltage, defined as the gate voltage necessary to suppress electron current injection originating from the metal, is shown to be closely related to the charge location in the oxide. From current measurements in the high-field regime, the hole distribution centroid is calculated, and is found to be coincident with earlier determinations of the electron distribution centroid in the oxide of p-type samples which received a similar implantation and annealing. At low applied voltages, it is shown that an oxide with trapped positive bulk charge (holes) will appear as a "giant, macroscopic potential well" to injected electrons where all carriers get trapped by the holes.

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ABSTRACT

The first experimental evidence is reported for hole trapping at room temperature in the bulk of dry thermally grown SiO_2 layers incorporated into metal-oxide-semiconductor (MOS) structures. The hole traps are generated by ion implantation into the SiO_2 layer followed by a high temperature anneal. Hole avalanche injection from the n-type Si-substrate is used to introduce holes into the SiO_2. Electron internal photoemission (photo I-V) measurements are used to locate the trapped positive charge. The magnitude of the cross-over voltage, defined as the gate voltage necessary to suppress electron current injection originating from the metal, is shown to be closely related to the charge location in the oxide. From current measurements in the high-field regime, the hole distribution centroid is calculated, and is found to be coincident with earlier determinations of the electron distribution centroid in the oxide of p-type samples which received a similar implantation and annealing. At low applied voltages, it is shown that an oxide with trapped positive bulk charge (holes) will appear as a "giant, macroscopic potential well" to injected electrons where all carriers get trapped by the holes.

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I. INTRODUCTION

Several groups have firmly established that holes, generated in the thermal SiO_2 layer of metal-oxide-semiconductor (MOS) devices at liquid nitrogen temperatures, are immobilized in the bulk of the insulator [1-3]. Recently bulk positive charging has also been invoked to explain high field conduction and breakdown in MOS devices *at room temperature* [4,5]. However, experiments performed in this laboratory aimed at locating positive charge created in clean dry-grown SiO_2 layers under various conditions at room temperature have always shown that the holes responsible for the positive charging are located near either the Al-SiO_2 or the Si-SiO_2 interface [6]. Therefore, it was concluded that the experimental results mentioned above [4,5] could not be interpreted as being due to permanent bulk positive charge.

In this paper, we report what we believe to be the first indisputable evidence for trapping of holes in the bulk of SiO_2 layers at room temperature. The phenomenon was observed in thermal SiO_2 layers grown using the fabrication standards for modern integrated circuits, but having received either a P^+-or an As^+-implantation, followed by a high temperature anneal. Avalanche injection from the silicon substrate was used in our experiments to introduce holes into the SiO_2. Some of the holes were consequently immobilized in deep traps. The effect of this positive trapped oxide charge upon electron currents induced by internal photoemission from the contacts was then studied in order to determine the spatial location and the density of the trapped holes. Other techniques such as capacitance-versus-voltage (C-V) measurements as a function of oxide thickness during oxide etch-back experiments [7] can in principle also be applied to locate oxide charge. However, their implementation is tedious and destructive, as opposed to the method used in this paper.

II. EXPERIMENTAL

The starting material consisted of n-type (100) silicon wafers with a resistivity of approximately 0.1 Ωcm. The samples were oxidized in nominally dry O_2 at 1000°C to thicknesses ranging from 50 to 120 nm. The ion implantation was then performed with energies and fluences as reported in Table I. Every batch of samples included a control sample which was not implanted. All samples, including the controls, received a post-implant cleaning treatment using alkaline-peroxide and acid-peroxide solutions, and a high-temperature anneal in nitrogen in order to remove the implantation-induced oxide damage. Then, a matrix of semitransparent aluminum dots (area $5.2 \times 10^{-3} cm^2$, ~ 12 nm thick) was evaporated to form MOS capacitors, and finally the structures received a post-metallization anneal in forming gas (85% N_2; 15% H_2) at 400°C for 20 min.

We used the avalanche injection technique [8] in order to inject holes into the SiO_2 layer of the MOS devices. This technique relies upon the acceleration towards the Si-SiO_2 interface of holes as minority carriers in the depletion layer of the silicon substrate, their avalanche multiplication under breakdown conditions, and the injection of the hottest part of their distribution over the energy barrier into the SiO_2 valence band. The detailed wave shape of the depleting pulse has been shown to be important for hole injection [9,10]. In our experiments a 50-kHz sawtooth wave was used.

After injection into the SiO_2 layer, a fraction of the holes are trapped and hence contribute to the oxide charge, which was monitored by high-frequency (1 MHz) C-V measurements. Part if not all of this oxide charge is due to holes immobilized in the innate hole trapping centers at the Si-SiO_2 interface [10]. The oxide-charge effect upon the photoemission current-versus-voltage (photo I-V) curves was then studied. A monochromatic-light beam derived from a xenon arc lamp using a 500-mm grating monochromator (Bausch and Lomb), excites the electron population in both electrodes. It is a unique feature that the samples can be charged using avalanche injection *in situ* in our photoelectric set-up. This allows the samples to be left in position between photo I-V measurements, and thus eliminates current variation due to repositioning in the beam.

III. THEORY

The combined action of the image-force effect and the applied electric field creates a potential barrier in the oxide near the injecting interface of the MOS structure. The influence of oxide charge and its location upon photo I-V characteristics can generally be understood by determining the position of this potential maximum with respect to the oxide charge distribution, and by calculating the effect this charge has upon the electric field (*without* the image force contribution) at the potential maximum [11,12].

When investigating positive oxide charge by means of photostimulated electron currents, partial annihilation of the oxide charge will take place, leading to displacement currents [6]. The various components of the current in the external circuit from the MOS structure are analyzed. Particular attention is paid to the situation where electron injection from both interfaces occurs.

A. Potential maximum and electric fields.

The potential barrier at a location x_0 near the injecting interface can be surmounted by an increasing number of electrons as it is lowered by an increasing applied voltage [13]. The field

at the potential maximum at time t, *without* the image force contribution, determined from Poisson's equation is given by [12]:

$$E\,(x_o^+,t) = \frac{V_g^+ - \phi_{ms} - \psi_s^+}{L} + \frac{1}{\epsilon}\frac{\bar{x}}{L}\,Q - \frac{1}{\epsilon}\int_{x_o^+}^{L}\rho(x,t)dx \qquad (1a)$$

for positive gate voltage, and by

$$E(x_o^-,t) = \frac{V_g^- - \phi_{ms} - \psi_s^-}{L} - \frac{1}{\epsilon}(1-\frac{\bar{x}}{L})Q + \frac{1}{\epsilon}\int_{o}^{x_o^-}\rho(x,t)dx \qquad (1b)$$

for negative gate voltage. The Al-SiO_2 interface is the origin of the x-coordinates taken positive towards the Si-SiO_2 interface, V_g is the applied gate voltage, ϕ_{ms} is the work function difference between the aluminum gate and the silicon substrate, ψ_s is the silicon surface potential, ϵ is the oxide low frequency permittivity, $\bar{x}$ is the centroid of the trapped charge distribution, Q is the integral of the oxide charge $\rho(x,t)$ over the oxide thickness L, and the superscripts (+ and -) refer to the voltage polarity of the metal gate electrode.

The effect of *negative* charge accumulated mainly in the bulk of the SiO_2 layer on the photo I-V curves has been amply documented recently [12,14,15]. In this case, the photo I-V curves obtained after charging for internal electron photoemission from either interface (generated by 4 to 5-eV photons) are shifted in a parallel fashion along the voltage axis to larger applied voltages. For electric fields $\gtrsim$ 0.5 MV/cm^2, the potential maximum is located within 20 Å of the injecting interface, which makes the third term in Eqs. (1a) and (1b) negligible for charge located mainly in the bulk. In order to have the same photocurrent before and after charging, the electric field at x_o has to be constant, which requires a change in applied gate voltage $\Delta V_g = V_g^{charged} - V_g^{uncharged}$ given by[12]

$$\Delta V_g^+ = -\frac{1}{\epsilon}\,\bar{x}Q \qquad (2a)$$

for Si injection, and

$$\Delta V_g^- = \frac{1}{\epsilon}(L - \bar{x})\,Q \qquad (2b)$$

for Al injection, provided the surface potential ψ_s can be considered constant for each polarity over the gate voltage range of interest.

At low electric fields, photoinjection of electrons from either contact is blocked due to the internal fields built up by the negative oxide charge. This internal field must be overcome by

the applied field before the photocurrent can flow. This introduces a distinct discontinuity in the photo I-V curves.

It has been recently verified experimentally that *positive* charge trapped near either interface of the SiO_2 layer causes the photo I-V curve for injection from the same interface to deviate gradually from the curve for the uncharged sample at increasing gate voltages [6]. This deviation is in the direction of increasing photocurrent for the charged sample (as compared to the uncharged condition) at constant gate voltages. At very low applied fields, the potential maximum location x_o is far enough removed from the injecting interface, so that the second and third term in either Eq. 1a or 1b cancel and the gate voltage needed to attain a given field $E(x_o,t)$ at the potential maximum is the same for the charged sample as for the uncharged condition. Towards higher fields, a gradual deviation of the photo I-V curves will occur, and ultimately the curves will become nearly parallel (see Fig. 1) when the potential maximum has moved close enough towards the injecting interface for the majority of the charge to reside beyond the maximum and, therefore, to appear as bulk oxide charge [6]. Obviously, the same argument holds for *negative* charge distributed near the injecting interface, but the deviation towards higher voltages will now have the opposite sign.

It is important to notice that with charge near only one interface, the photoemission curve from the opposite electrode will undergo only a minute shift. For example, if charge is present near the Si-SiO_2 interface ($\bar{x} \approx L$) the second term in Eq. 1b for $E(x_o^-,t)$ will be very small, and the photo I-V curve for Al injection will be hardly affected.

For the case of trapped charge of the same sign near both the Si-SiO_2 and the Al-SiO_2 interface, the photoemission curves will exhibit a characteristic "splitting" away from photoemission curves for the uncharged case with increasing electric field for both gate voltage polarities. If the complete photo I-V characteristic is not obtained for this case, an erroneous conclusion for the actual charge location might be obtained. For instance, if values for ΔV_g^+ and ΔV_g^- are extracted from photo I-V shifts from only the high field portion of the characteristic and a value for the charge distribution centroid $\bar{x}$ is calculated using the photo I-V relationship [11]

$$\bar{x} / L = [1 - (\Delta V_g^- / \Delta V_g^+)]^{-1}, \qquad (3)$$

one would obtain a value of $\bar{x} = L/2$ for equivalent magnitudes of ΔV_g^+ and ΔV_g^- (ΔV_g^- and Δ_g^+ have opposite signs). From this, one might conclude that a homogeneous uniform charge distribution is present in the oxide bulk when actually equal amounts of charge are distributed in similar fashion near both interfaces.

The average electric field in the oxide

$$E_{av} = [\int_{o}^{L} E(x)dx]/L,$$

can be calculated from an expression for E(x), obtained by substituting x for x_o^+ (or x_o^-) in Eq. 1a (or 1b). It follows that

$$E_{av} = (V_g - \phi_{ms} - \psi_s)/L. \tag{4}$$

It is thus seen that the field at the potential maximum, $E(x_o, t)$, as given by Eqs. 1a or 1b is calculated by adding the charge-related quantity $(Q\bar{x}/L)/\epsilon$ or $-[(1-\bar{x}/L)Q]/\epsilon$ to the average oxide field E_{av}, assuming no charge is present between x_o and the injecting interface (i.e. the third term in Eqs. 1a and 1b can be neglected). As discussed above, the field $E(x_o, t)$ at the potential maximum is kept constant in order to maintain a constant photocurrent level, which means that it is the average oxide field which has to be changed by either one of the aforementioned charge-related quantities, depending upon the gate voltage polarity. It follows, therefore, that the average oxide field (or the oxide voltage drop $V_{ox} = E_{av}\ L$) is a logical variable for plotting photocurrents, as performed in Fig. 1, if one wants to obtain the charge-related quantities from Eqs. 2a and 2b.

In the case of *negative* bulk oxide charge and a p-type substrate, ψ_s is nearly constant (for V_g negative) or changes only before the strong onset of photocurrents, and is constant thereafter (for V_g positive). It is thus possible to use the applied gate voltage instead of the oxide voltage drop as a variable. For *positive* oxide charge and an n-type substrate as in this paper, the variation of ψ_s *with* V_g *near flat-band after charging* (for V_g negative) has to be considered. Therefore, the oxide voltage drop is used as a variable when plotting subsequent photo I-V data.

B. Current densities.

Let us now investigate the influence of positive charge in the oxide upon the various current components.

The current density, measured in the external circuit of the MOS-structure, derived from the current continuity equation and Poisson's equation, is:

$$J_{ext}^{+} = J(x_o^+, t) - \frac{\epsilon}{L}\frac{d\psi_s^+}{dt} + \frac{1}{L}\frac{d}{dt}(\bar{x}Q) - \int_{x_o^+}^{L}\frac{\partial\rho(x,t)}{\partial t}dx \tag{5a}$$

for injection from the Si-SiO_2 interface, and

$$J^-_{ext} = J(x^-_o,t) - \frac{\epsilon}{L}\frac{d\psi^-_s}{dt} - \frac{d}{dt}\left[(1-\frac{\bar{x}}{L})Q\right] + \int_o^{x^-_o}\frac{\partial\rho(x,t)}{\partial t}dx \qquad (5b)$$

for injection from the Al-SiO_2 interface, where $J(x_o, t)$ corresponds to the electron current density at the potential maximum x_o. The superscripts again refer to the voltage polarity of the gate electrode. Note that the vector corresponding to an electron current density conventionally represents the flow of positive carriers in the opposite direction. Its magnitude is, therefore, positive for an electron flow in the negative x-direction.

a. *Si injection*

$J^+_{inj} = J(x^+_o,t) - \int_{x^+_o}^{L} [\partial\rho(x,t)/\partial t]dx$ is the current density in the oxide at the injecting Si interface. The external current density can be written as

$$J^+_{ext} = J^+_{inj} + J^+_d. \qquad (6a)$$

The displacement current density J^+_d lumps together the component $(1/L)d(\bar{x}Q)/dt$, which is the direct effect of positive charge annihilation, (time derivative of the image charge in the Si electrode, induced by the decreasing oxide charge) and the component $-(\epsilon/L)\, d\psi^+_s/dt$, which is the indirect effect (time-derivative of the Si electrode charge which corresponds to the changing oxide voltage drop). For an n-type substrate, trapped positive charge, and positive gate bias voltages, the Si substrate is always accumulated and $d\psi^+_s/dt$ resulting from any positive oxide charge annihilation is negligible.

The displacement current density $(1/L)\, d(\bar{x}Q)/dt$ is larger for charges close to the Si-SiO_2 interface ($\bar{x} \approx L$).

b. *Al injection*

$J^-_{inj} = J(x^-_o,t) + \int_o^{x^-_o} [\partial\rho(x,t)/\partial t]dx$ is the current density in the oxide at the injecting Al-interface. Similarly as for the Si injection, the external current density can be written as

$$J^-_{ext} = J^-_{inj} + J^-_d, \qquad (6b)$$

where the displacement current density J^-_d again represents a direct and an indirect component.

The term $(\epsilon/L)(d\psi^-_s/dt)$ in J^-_d is noticeable only in the depletion and weak-inversion region. The quantity $d\psi_s/dt$ can be written as $(d\psi_s/dQ_s) \times (dQ_s/dt)$, where Q_s is the silicon space-charge density; dQ_s/dt is proportional to dQ/dt. Since, for the low-resistivity substrates used in our experiments, the silicon space-charge capacitance $C_D = dQ_s/d\psi_s$ is large and

changes over a wide gate-voltage region (compared to a high-resistivity substrate), $d\psi_s^-/dt$ will be small and vary gradually.

The third term in Eq. 5b corresponding to the annihilation of positive charges at the Si-SiO_2 interface can now be neglected ($\bar{x} \approx L$), but the same term corresponding to the annihilation of bulk positive charge has to be considered.

Reducing the intensity of the monochromatic light source will reduce the injected electron current density, and therefore the hole annihilation rate and the corresponding displacement current J_d. As a consequence, the ratio J_d/J_{ext}, which determines the relative importance of the displacement current, will remain unaltered. But since the time constant for the annihilation process is proportional to J_{inj}^{-1}, it is advantageous to do the measurement at the lowest possible light intensities, which yield very reproducible, although distorted by J_d, photo I-V plots.

The electron capture by Coulomb-attractive centers in the oxide has been shown to have a *strongly field-dependent cross section* [6,16,17]. For average oxide fields ranging from 5×10^5 to 3×10^6 V/cm an E_{av}^{-3} -dependence was found for the capture cross section, which was reduced from approximately 5×10^{-13} to 4×10^{-15} cm^2 [6,16,17]. Holes trapped on sites normally present near the Si-SiO_2 interface [6] and holes trapped on sites related to implanted As or P in the bulk of the SiO_2 layer were observed to behave in a similar fashion with respect to electron capture; that is, they both are coulombic-attractive sites with a field dependent capture cross section [6]. Therefore, less positive charge annihilation by injected electrons will occur during the photo I-V measurements at higher fields.

C. Double Injection

Substituting $x = 0$ for x_o^+ in Eq. 1a yields the expression for the electric field E_{Al}^+ at the Al-SiO_2 interface under *positive* gate bias:

$$E_{Al}^+ = \frac{V_g^+ - \phi_{ms} - \psi_s^+}{L} - \frac{1}{\epsilon}\left(1-\frac{\bar{x}}{L}\right)Q. \qquad (7a)$$

Similarly substituting $x = L$ for x_o^- into Eq. 1b, we find the field at the Si-SiO_2 interface under *negative* gate bias,

$$E_{Si}^- = \frac{V_g^- - \phi_{ms} - \psi_s^-}{L} + \frac{\bar{x}}{L}Q. \qquad (7b)$$

It is noted that, due to the positive oxide charge Q, the electric field at the Al-SiO_2 interface will still be negative for small positive gate voltages. Likewise, the field at the Si-SiO_2 interface will still be positive for small negative gate voltages. Photon energies which excite electrons over both energy barriers (i.e. $\hbar\omega \gtrsim 4.2$ eV), will then induce electron injection from both electrodes simultaneously in a certain gate voltage range. These electron currents will subtract. Once the externally applied voltage is high enough to make the oxide field at either one of the interfaces prevent electron injection, double injection ceases.

Which current dominates when double injection occurs at a given gate voltage is determined by several factors:

i) the aluminum and oxide thicknesses, which determine the absorptance in both electrodes. Oxide thickness is important in determining optical interference effects which in turn affect the absorptance in both electrodes. This absorptance, together with the energy difference $\hbar\omega - \phi_B$, determines the source of electrons excited over the energy barrier ϕ_B at the interface;

ii) the magnitude *and the location* of the positive charge, which determines (1) the electric field strength at both interfaces and, therefore, the injected current densities, and (2) the displacement currents.

As shown above, the displacement current component due to annihilation of positive charge close to the Si-SiO_2 interface ($\bar{x} \approx L$) will be small for aluminum injection. The same charge distribution will cause a large displacement current for silicon injection which will subtract from the injected current density, and to a large extent reduce the external current corresponding to Si injection. Assuming equal injection currents from both interfaces, the external current component corresponding to Al injection will, therefore, dominate when positive charge is trapped near the Si-SiO_2 interface. In our MOS structures, there is more light absorbed in the Al electrode than transmitted into the Si, which further enhances Al injection. This condition is somewhat offset by the larger electric field at the Si-SiO_2 interface. Yet, since the photo I-V relation is sublinear for electric fields $\gtrsim 0.3$ MV/cm [11], this larger field probably does not compensate for the stronger Al absorption.

Therefore, when positive charge is distributed near the Si-SiO_2 interface, the net external current will be dominated by Al photoemission at very low gate bias and for photon energies allowing injection from both interfaces.

It is interesting to notice that, under those conditions for which the electric fields favor electron injection at both interfaces, every injected electron will end up trapped in the oxide by a positively charged center. The oxide appears as a "giant potential well" to electrons, although the microscopic trapping probability, given by the product of the electron capture cross section and the density of available electron traps integrated over the oxide thickness [18], can be considerably less than one.

D. Exclusive Al injection

It can be shown that for injection from the Al-SiO_2 interface and under those conditions where no injected electron leaves the oxide, the external current density is given by

$$J_{ext} \approx d\,[(\bar{x}Q)/L]/dt \tag{8}$$

if the silicon surface potential variation is disregarded. When $\bar{x} \approx L$, J_{ext} approaches dQ/dt, which is also equal to the injected current density J_{inj} (since every injected electron is assumed to become trapped). It follows then that annihilation of positive charges very close to the Si-SiO_2 interface does not induce a displacement current component for Al injection or, in other words, when only injection from the Al interface is allowed to occur, any displacement current (visible as a distortion in the photo I-V curve) must originate from the annihilation of positive charges *removed from the Si-SiO_2 interface*.

For the case where positive charges are only present near the Al-SiO_2 interface ($\bar{x} \approx 0$), J_{ext} becomes very small for Al injection and for complete trapping of the injected electrons (see Eq. 8).

A bimodal distribution of positive charges, nearly equally distributed near the Si-SiO_2 and Al-SiO_2 interfaces is possible. In that case, and for exclusive Al injection ($\hbar\omega \lesssim 4.2$ eV) at $V_g = 0$ V, one might expect a contribution to the external current from electrons which escape recombination with positive charges near the Al-SiO_2 interface and drift towards the Si-SiO_2 interface. The field in the oxide bulk which causes this current will be very small for comparable charge densities near both interfaces, and thus easily reversed by a slightly positive gate voltage bias. From that point on, we are left with the previously discussed case of positive charge near the Al-SiO_2 interface (the charge near the other interface does not affect the current). It was concluded that the external current will then be very small due to a large compensating displacement current.

E. Cross-Over Voltage

As discussed above, the external current is dominated by Al injection when positive charge is present near the Si-SiO_2 interface. We are able to calculate the gate voltage required to suppress this Al dominated injection and to start Si dominated injection beyond that voltage, which is defined as the *cross-over voltage*. This is essentially equal to the gate voltage necessary to achieve the flat-band (i.e. zero field) condition at the Al-SiO_2 interface. Note that, although the photoemission currents have been plotted as a function of the voltage drop across the oxide, the cross-over voltage will be referred to as the applied *gate* voltage.

In Ref. 6, the cross-over voltage was calculated to be approximately +0.5 V for 2.5×10^{12} positive charges/cm^2 distributed mostly within 50 Å of the Si-SiO_2 interface for a 935 Å thick oxide layer. Figure 2 shows the oxide band bending V (in normalized units) for various charge distributions as a function of the charge distribution centroid. The oxide band bending was calculated for zero applied gate bias; the silicon surface potential ψ_s and the work-function difference ϕ_{ms} have been neglected. As can be deduced from Fig. 2, the same amount of positive charge placed in a sheet in the middle of a 1000 Å thick oxide layer depresses the oxide conduction band by ~ 3 eV. In this case, it requires a gate voltage bias of + 6 or − 6 V to flatten the energy bands at the Al or Si electrode, respectively. Thus, if one allows injection from the Al interface only (i.e. for photon energies between 3.1 and 4 eV [19]), the cross-over voltage will be + 6 V. Note that for $0 < V_g < 6$ V, the external current is originating from the Al (and is therefore denoted by J^-_{ext}), although the gate voltage polarity is positive. For higher positive gate voltages the external current will be zero, since the low photon energy does not allow Si injection.

In the low-field region (-6 V $< V_g < 6$ V) and for photon energies *above* 4.2 eV, electrons will not only be injected from the Al, as discussed above, but also from the Si valence band and cause a current flow in the opposing direction. The further the positive charge centroid is removed from the Si interface, the more important becomes the contribution of Si injection to the external current. Which current component dominates is again determined by the location and the magnitude of the oxide charge, and by the absorptivity of both electrodes. In general the Al component dominates, but the net current will have a lower cross-over voltage than in the case of current injection from the Al electrode only (photon energies $\lesssim$ 4.2 eV).

F. Summary

We have systematically studied the low-field region of the photoemission curves, eliminating double injection by using photon energies which allow only Al injection. As demonstrated above, the magnitude of the current and the shape of the photo I-V curve for low gate voltages, in addition to the cross-over voltage determined in this way, are important criteria in order to distinguish between a bulk positive charge distribution and positive charge accumulation near either one or both interfaces.

IV. RESULTS

Figure 3 depicts the C-V curves for an As^+-implanted MOS structure before (a) and after (b) avalanche injection of holes, and after subsequent recording of the photo I-V curve for negative (c) and positive (d) gate voltage polarity. Figure 4 shows the electron photoemission current versus oxide voltage drop for the same sample for injection from the aluminum at a photon energy of 4 eV, measured before and after hole injection and trapping, respectively. The important features of the photoemission curve after hole injection in Fig. 4 are:

i) The cross-over voltage of $\approx +10$ V;

ii) The distortion with respect to the photoemission curve for the uncharged situation (for $10\ V \leq V_{ox} \leq -15\ V$), which is due to the subtraction from the injected current density of a displacement current (caused by the positive charge annihilation by injected electrons);

iii) The nearly parallel shift in the direction of less negative voltages with respect to the photo I-V curve for the uncharged sample, for $V_{ox} \lesssim -20$ V, which is indicative of positive charging.

As seen in Fig. 5, the cross-over voltage for the photo I-V curve under positive bias after hole trapping is only ≈ 6.5 V. This is caused by the higher photon energy of 5 eV, necessary to initiate electron photoinjection from the silicon, which simultaneously allows compensating injection from the aluminum in the low-field region near the cross-over voltage (see Sec.III-E).

At higher V_{ox} values, the photoemission curves after hole trapping tend to become parallel with respect to the uncharged state, when the influence of displacement currents is reduced due to a reduced capture rate for electrons by the positive charge. This is caused by the field dependence of the capture cross section for electrons.

For injection from the silicon, bending of the energy bands in the silicon could pose a problem, since it causes a different barrier for electrons originating from various depths in the substrate. However, in our experiments the silicon substrate is always accumulated for positive gate bias, and the silicon surface potential is nearly fixed. Also, since the photo I-V technique relies upon the comparison of current measurements before and after charging, the results will not be affected.

Figures 6 and 7 show the photoemission curves before and after charging of an unimplanted control sample for negative and positive gate voltages, respectively. The photocurrent-versus-voltage characteristics after charging are different from those for the implanted case (Figs. 4 and 5). For both polarities, the curves gradually deviate towards higher gate voltages, indicative of positive charging very close to both interfaces. The cross-over voltage of only a few hundred mV is consistent with that conclusion. The initial charge state $\Delta V_{FB} \approx -6.75$ V) in the control sample was obtained after injection of 2.2×10^{14} holes/cm^2 into the oxide. In comparison, $\Delta V_{FB} = -10.6$ V was reached for the implanted sample after injecting only $\sim 1.3 \times 10^{13}$ holes/cm^2 into the oxide. The latter injection level failed to show any effect on the photoemission curves for the control sample.

The control sample of Figs. 6 and 7 which received an 800°C anneal in N_2 for 30 min after oxidation showed less interface hole trapping than a corresponding sample which received a 1000°C treatment (see Fig. 1). Other work performed at this laboratory [20] has confirmed that there is indeed an optimum anneal temperature around 800°C which minimizes hole trapping near the Si-SiO_2 interface. Therefore, the ion implanted samples were also given an 800°C anneal in order to minimize the interface trapping contribution but still anneal out the gross implant damage.

Since it has been established that there is a bulk distribution of positive charges present in the ion implanted samples after hole injection, it is now possible to determine a centroid value from Eq. 3 using ΔV_{ox}^{+} and ΔV_{ox}^{-} obtained from the highest oxide voltage region of the photo I-V curves. The results are included in Table I. The photo I-V measurements for the implanted sample of batch C were performed *only in the high oxide voltage region* in order to further reduce the positive-charge annihilation during the photoemission measurements. As discussed in Sec.III-B-b, the electron capture by Coulomb-attractive centers is greatly reduced for large applied electric fields. At low applied fields when the trapped positive bulk oxide charge (holes) makes the oxide layer look like a "giant potential well" for electrons, all injected carriers from either interface are observed (from C-V or photo I-V measurements) to be trapped by the holes and annihilate them.

In order to separate the bulk hole trapping from the hole distribution near the Si-SiO_2 interface (which is still present despite the optimized anneal at 800°C), the measurements for the charged samples of batches A and C were performed after a partial annihilation with the samples biased at the Si flat-band condition, which leads to preferential annihilation of the interface charge in view of the field-dependent electron capture cross section. The local field in the oxide at flat-band near the Si-SiO_2 interface is very low which leads to a large capture cross section ($\approx 10^{-12}$ - 10^{-13} cm^2) for electrons on trapped holes near this interface. However, the local fields in the region of the bulk trapped holes on sites related to implanted ions is much higher with a respectively lower electron capture cross section ($< 10^{-13}$ cm^2) which leads to less trapped hole annihilation by injected electrons for the same applied voltage bias required for the flat-band voltage condition.

The hole distribution centroids are found to be in good agreement with the *electron* distribution centroids found after avalanche-injection from p-type samples which received similar processing and an identical ion implantation into the SiO_2 layer. This electron distribution centroid was 25 nm for the 15-keV P-implant and 46 nm for the 60-keV As-implant [15,21]. The electron distribution centroid has previously been shown to be in excellent agreement with the ion distribution centroid obtained from a depth-profile determined by secondary ion mass spectrometry [20]. It is believed that the deep hole trapping sites introduced by the ion implantation are related to the ions themselves and not to gross structural damage in the oxide, in view of the annealing treatment at high temperature after the implant.

V. CONCLUSION

We have presented the first experimental evidence for hole trapping in the bulk of dry thermally grown SiO_2 layers at room temperature. The deep traps causing the permanent trapping were created by ion implantation followed by a high temperature anneal, and the holes were injected into the SiO_2 by avalanching the underlying substrate.

In view of the dominant trapping probability for holes compared to the trapping probability for electron observed in similarly processed p-type samples, this study generates concern about the use of ion implantation in the fabrication of devices intended for operation in an ionizing radiation environment creating electron-hole pairs. However, the possibility of storing both electrons and holes in an SiO_2 layer may prove useful in a novel type of electrically alterable memory device.

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Table I

Experimental parameters and hole - distribution centroids for the various samples.

Batch	Oxide thickness (nm)	Ion	Dose (cm^{-2})	Energy (keV)	Anneal	Hole-distribution centroid (nm)
A	51	P	$5x10^{14}$	15	1000°C-30min.	24.1 (±1.7)
B	106	As	$1x10^{13}$	60	1000°C-30min.	42.2 (±2.6)
C	124	As	$5x10^{12}$	60	800°C-30min.	49.7 (±2.5)

FIGURE CAPTIONS

Fig. 1 Current measured in the external circuit of the MOS capacitor as a function of the oxide voltage drop (photo I-V curves) for positive gate bias on a control sample (L = 126 nm), which received a 1000°C anneal in nitrogen for 30 min after oxidation, measured before (closed dots) and after avalanche injection (open dots), respectively. The photon energy used to generate the internal photoemission currents was 5 eV. The total injected hole density was approximately 6×10^{13} cm^{-2}, which resulted in an initial flat-band voltage shift $\Delta V_{FB} = -10$ V. The injected hole density has been calculated from the injected current density, which was obtained from the external current density by correcting for the displacement currents due to changing image charge (hole trapping) and changing electrode charge (increasing avalanche voltage). After recording the corresponding photo I-V curve for negative gate bias, this flat-band voltage shift was reduced to approx. - 8.5 V, due to charge annihilation.

Fig. 2 Normalized oxide band bending V (divide by $(qLN)/\varepsilon$ where N is the total density of positive charges/cm^2, as a function of normalized charge centroid $\bar{x}$ (divided by L) for a homogeneous distribution, a δ-function shaped distribution, and a Gaussian distribution (with standard deviation $\sigma \approx \bar{x}/3$, which corresponds to the As^+-implantation; for $\bar{x}/L \gtrsim 0.5$ penetration of the distribution into the Si sets in). The inset illustrates the conduction band bending in the oxide for a δ-function distribution with $N = 2.5 \times 10^{12} cm^{-2}$. Also shown are the corresponding absolute value of the flat-band voltage shift ($|\Delta V_{FB}|$) and the gate voltage V_M necessary to flatten the bands at the Al-SiO_2 interface (the cross-over voltage for $\hbar\omega \lesssim 4.2$ eV). $|\Delta V_{FB}|$ and V_M (also normalized to $(qLN)/\varepsilon$) do not depend on the *shape* of the charge distribution.

Fig. 3 Capacitance - versus - voltage (C-V) curves for an ion implanted sample from batch C (L=124nm) measured in conjunction with the photo I-V curves of Figs. 4 and 5:

a. - Initial plot for virgin sample and after the first two photo I-V runs (V_g - and + , resp.) before charging.

b. - After avalanche-injection of 1.3×10^{13} holes/cm^2; $\Delta V_{FB} = -10.5$ V.

c. - After photo I-V run with V_g negative; $\Delta V_{FB} = -8.5$ V.

d. - After photo I-V run with V_g positive; $\Delta V_{FB} = -6.5$ V.

There is an appreciable amount of charge annihilation during the recording of the second set of photo I-V curves.

Fig. 4 Current (absolute value) measured in the external circuit of the MOS capacitor as a function of the oxide voltage drop (photo I-V curves) for negative gate bias for the same sample as in Fig. 3, measured before (closed dots) and after avalanche injection (open dots), respectively. The photon energy is 4 eV. The inset illustrates the various current density components.

Fig. 5 Photo I-V curves for positive gate bias for the same sample as in Figs. 3 and 4. The photon energy is 5 eV. The symbols have the same meaning as in Fig. 4.

Fig. 6 Photo I-V curves (absolute values of the current) for negative gate bias (at 4 eV) for a control sample from batch C (L=129 nm) which went through the same processing steps as the sample of Figs. 3,4 and 5, except for the implantation, measured before charging (closed dots), after injection of 1.3×10^{13} holes/cm^2 (open dots), and after injection of 2.2×10^{14} holes/cm^2 (open triangles), respectively. The first injection did not result in any flat-band voltage shift. The second injection initially yielded ΔV_{FB} = - 6.75 V, which was reduced to - 6.3 V after 40 min relaxation. The final photo I-V measurements sequentially reduced this shift to - 5.2 and - 4.2 V after the run for negative and positive gate bias, respectively.

Fig. 7 Photo I-V curves for positive gate bias (at 5 eV) for the same sample as in Fig. 6. The symbols have the same meaning as in Fig. 6.

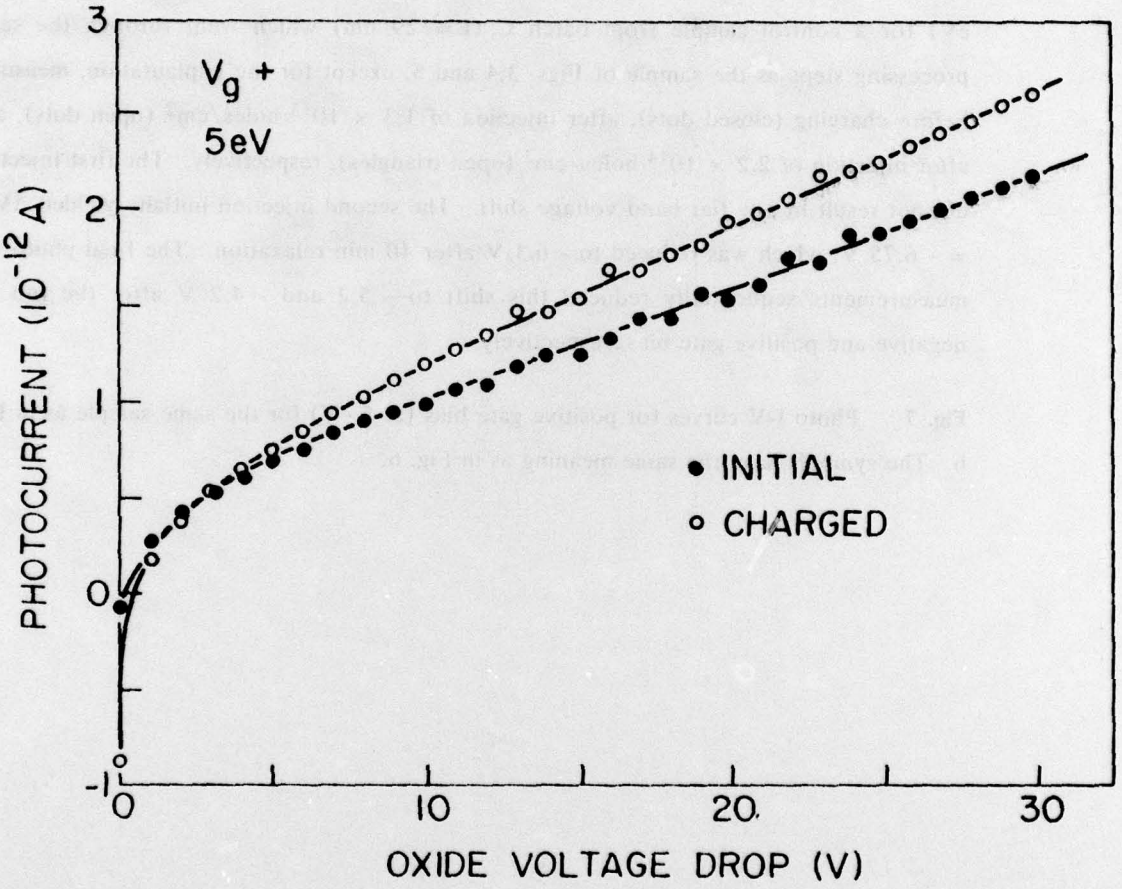

V_g +
5eV
PHOTOCURRENT (10^{-12} A)
3
2
1
0
-1
0
10
20
30
OXIDE VOLTAGE DROP (V)
INITIAL
CHARGED

FIGURE 1

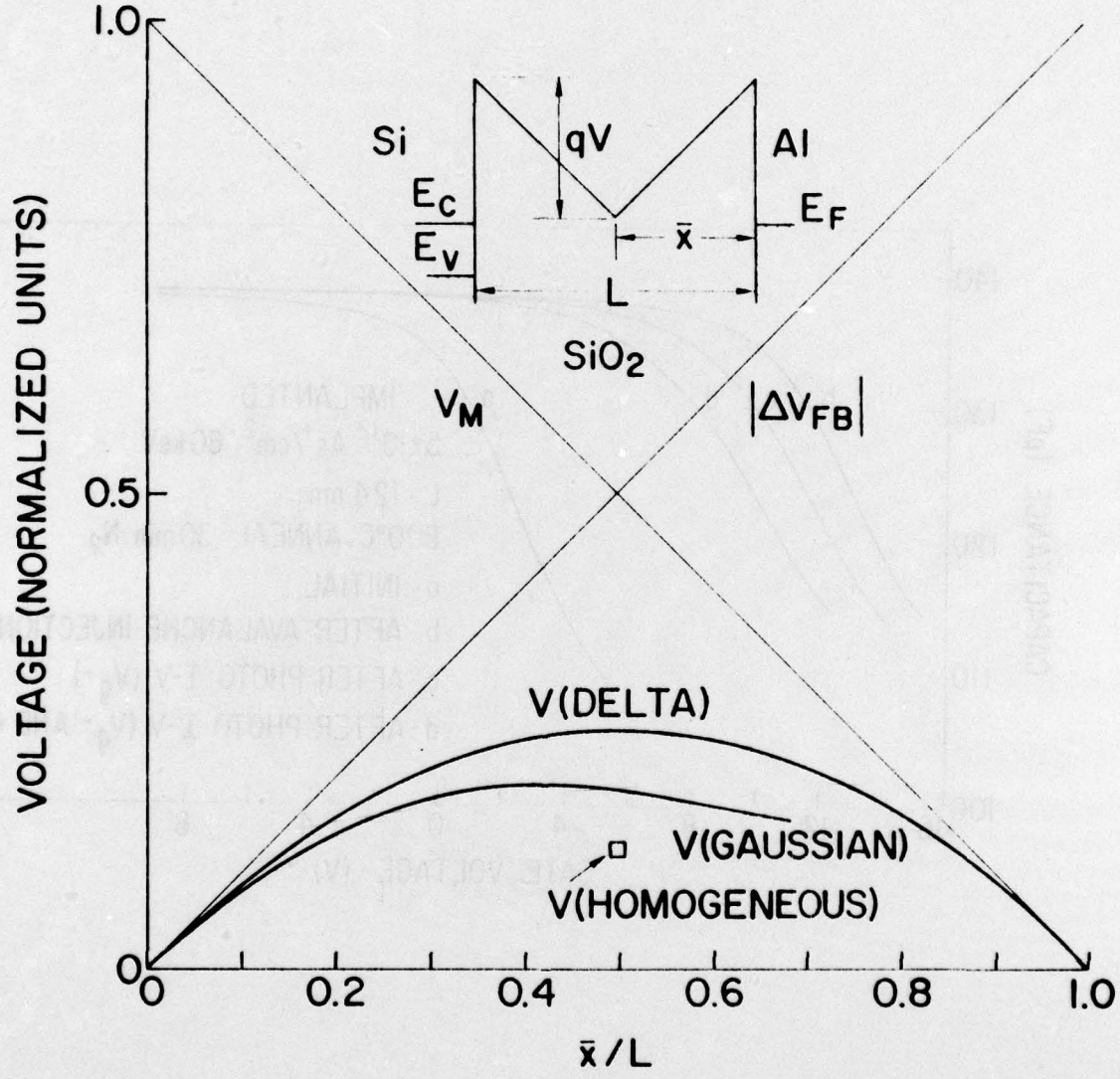

1.0
0.5
0
VOLTAGE (NORMALIZED UNITS)
Si
qV
Al
E_C
E_V
E_F
$\bar{x}$
L
SiO_2
V_M
$|\Delta V_{FB}|$
V(DELTA)
V(GAUSSIAN)
V(HOMOGENEOUS)
0
0.2
0.4
0.6
0.8
1.0
$\bar{x}/L$

FIGURE 2

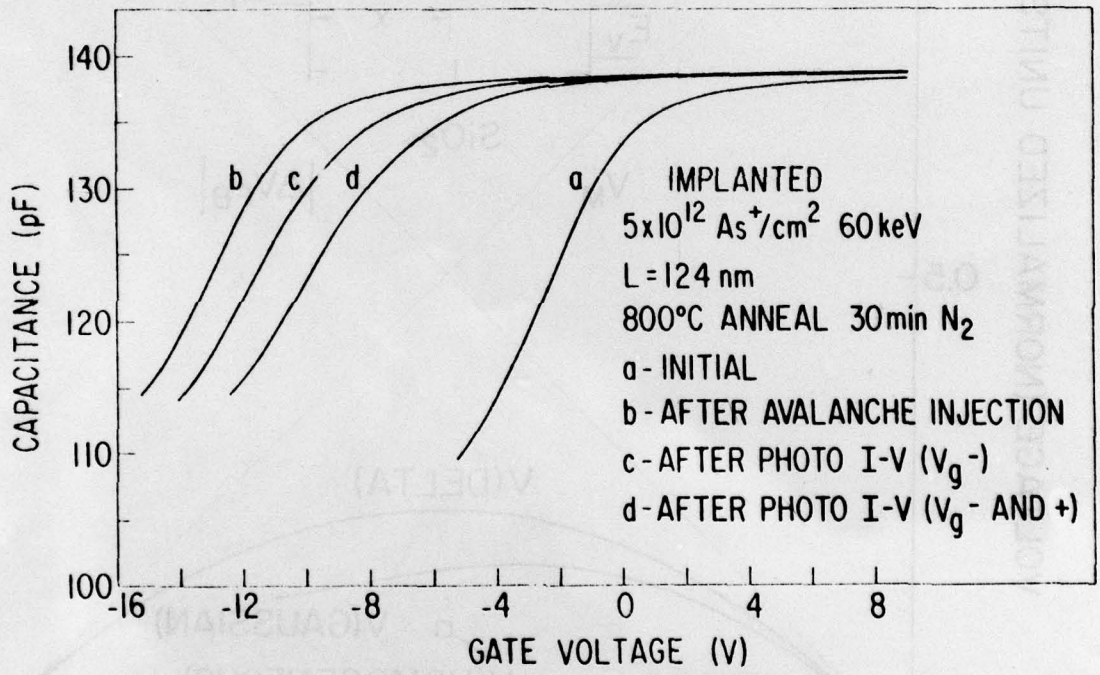

140
130
120
110
100
CAPACITANCE (pF)
-16
-12
-8
-4
0
4
8
GATE VOLTAGE (V)
a
b
c
d
IMPLANTED
5x10^12 As+/cm2 60keV
L = 124 nm
800°C ANNEAL 30min N2
a - INITIAL
b - AFTER AVALANCHE INJECTION
c - AFTER PHOTO I-V (Vg -)
d - AFTER PHOTO I-V (Vg - AND +)

FIGURE 3

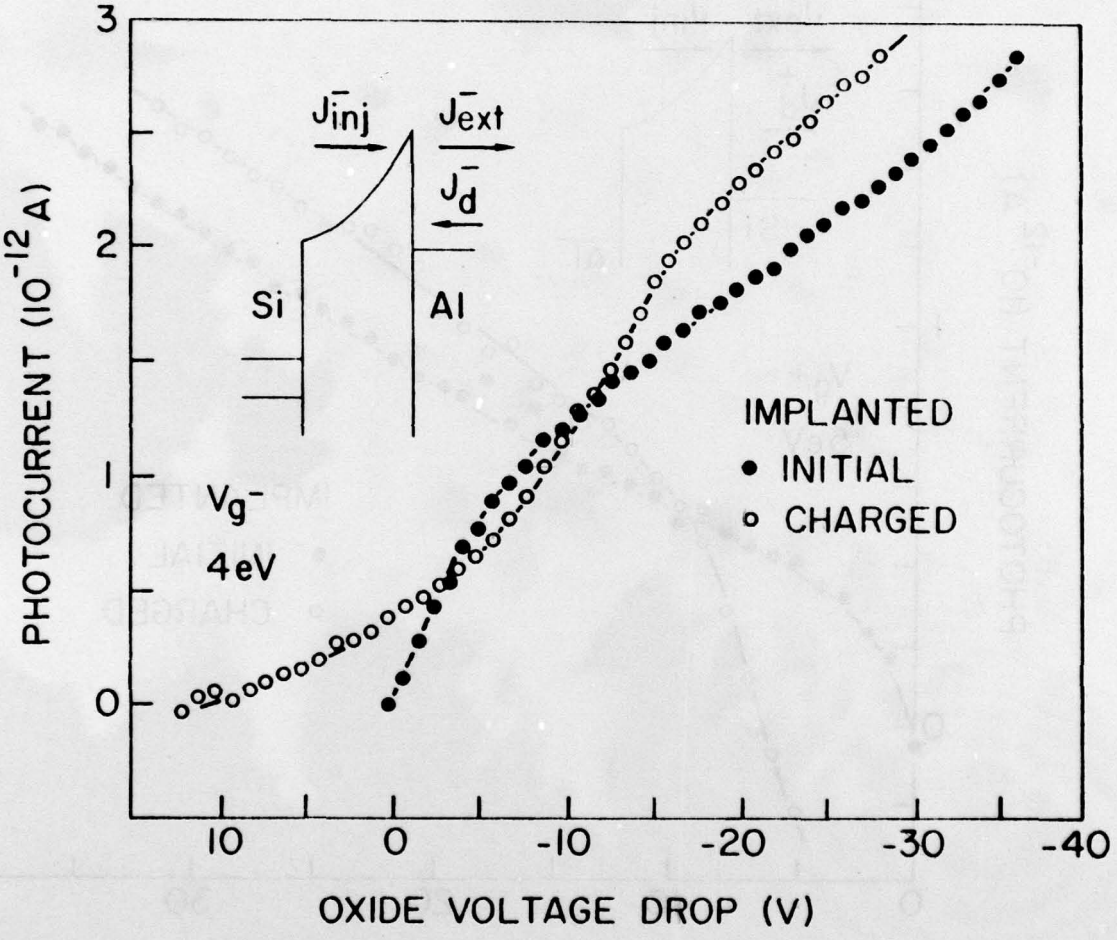

PHOTOCURRENT (10^{-12} A)
3
2
1
0
10
0
-10
-20
-30
-40
OXIDE VOLTAGE DROP (V)
J_{inj}^-
J_{ext}^-
J_d^-
Si
Al
V_g^-
4eV
IMPLANTED
• INITIAL
o CHARGED

FIGURE 4

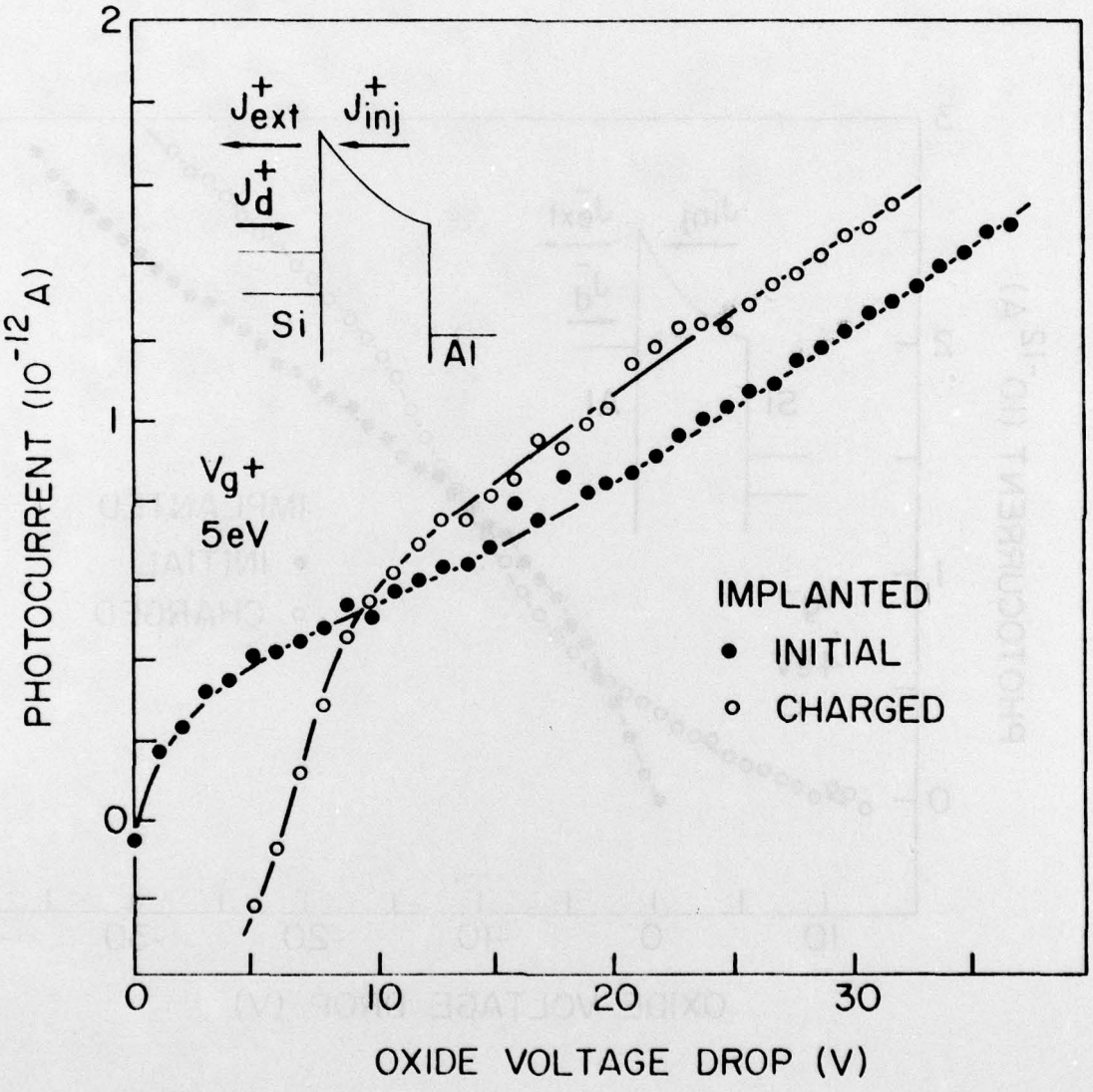

2
1
0
PHOTOCURRENT (10^{-12} A)
J^+_{ext}
J^+_{inj}
J^+_d
Si
Al
V_g+
5eV
IMPLANTED
INITIAL
CHARGED
0
10
20
30
OXIDE VOLTAGE DROP (V)

FIGURE 5

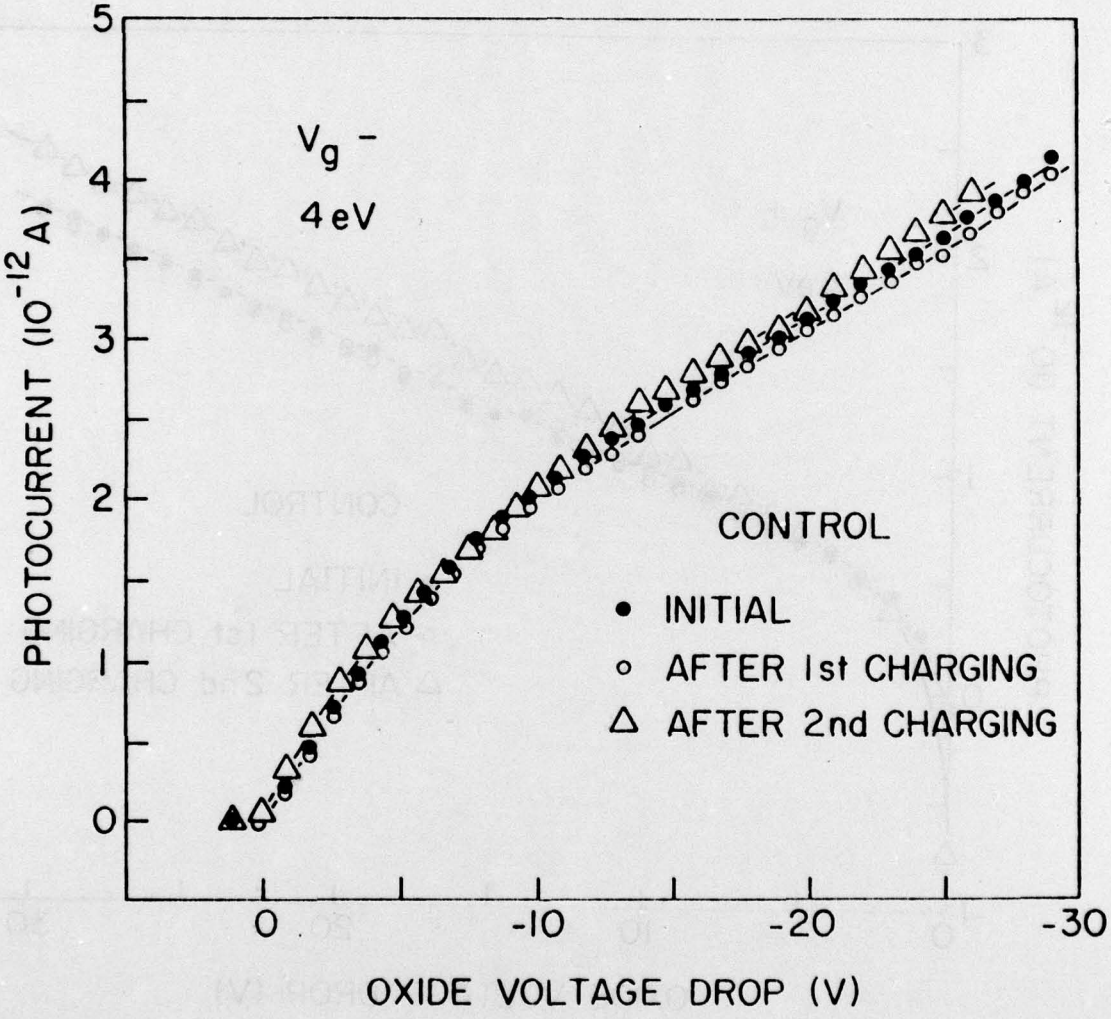

5
4
3
2
1
0
PHOTOCURRENT (10^{-12} A)
V_g -
4 eV
CONTROL
INITIAL
AFTER 1st CHARGING
AFTER 2nd CHARGING
0
-10
-20
-30
OXIDE VOLTAGE DROP (V)

FIGURE 6

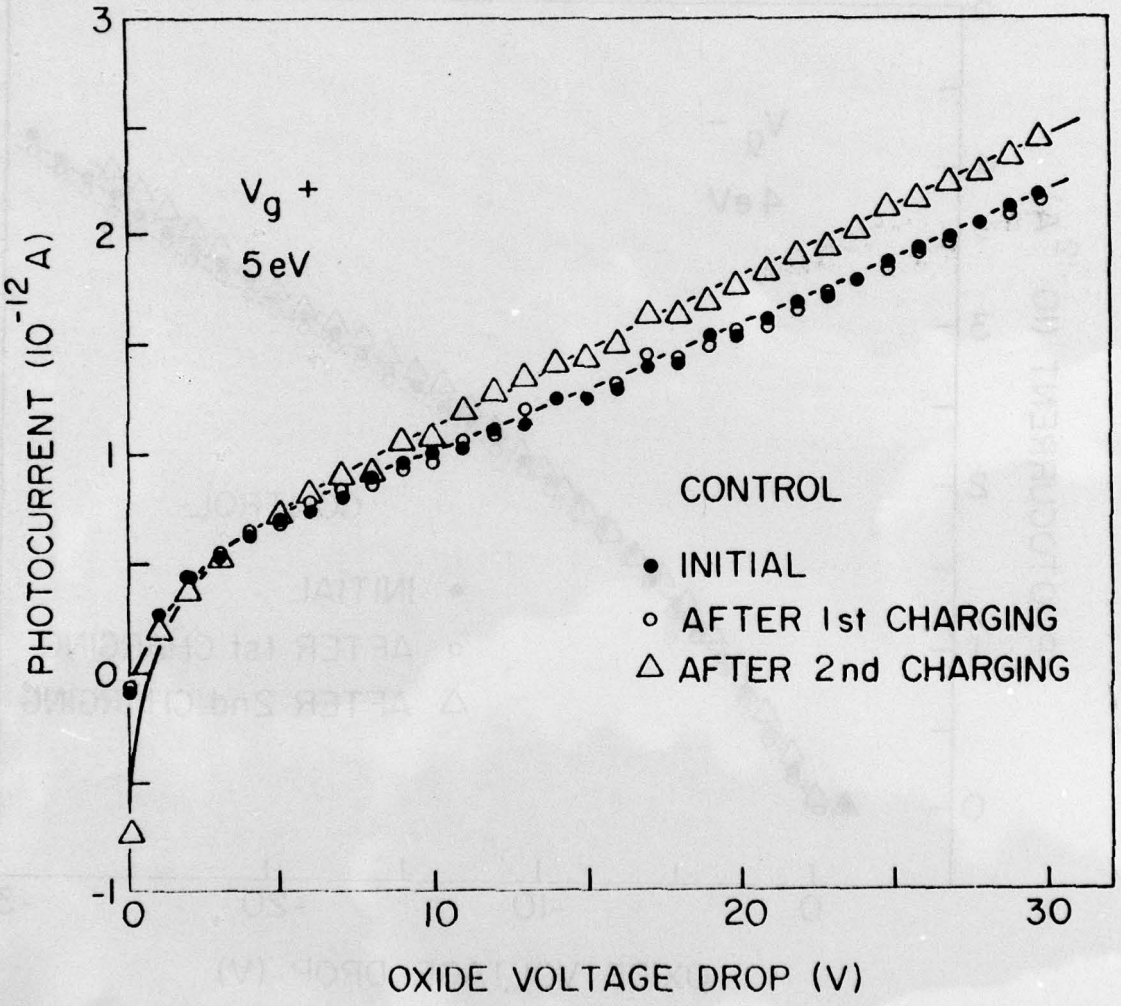

3
2
1
0
-1
0
10
20
30
PHOTOCURRENT (10^{-12} A)
OXIDE VOLTAGE DROP (V)
V_g +
5eV
CONTROL
• INITIAL
o AFTER 1st CHARGING
△ AFTER 2nd CHARGING

FIGURE 7

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