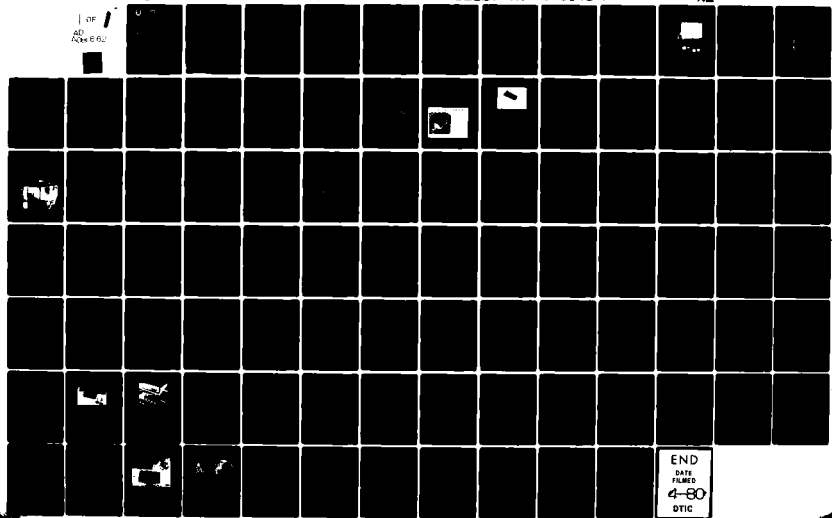


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**MNOS BORAM MANUFACTURING METHODS AND
TECHNOLOGY PROJECT**

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WESTINGHOUSE ELECTRIC CORPORATION
Systems Development Division
Baltimore, Maryland 21203

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TABLE OF CONTENTS

	Page
1. INTRODUCTION	1-1
2. BACKGROUND	2-1
2.1 Military Storage	2-1
2.1.1 Secondary Storage	2-1
2.1.2 Airborne Recorders	2-4
2.1.3 Program Storage	2-4
2.2 MNOS BORAM Hybrid Circuits	2-6
2.2.1 MNOS BORAM Technology	2-6
2.2.2 Hybrid Circuit Packaging	2-6
2.3 MM&T Project	2-7
2.3.1 Project Goals	2-7
2.3.2 Project Tasks	2-7
3. MNOS BORAM CHIP FABRICATION	3-1
3.1 Device Considerations	3-1
3.1.1 Transistor Structure	3-1
3.1.2 BORAM Integrated Circuits	3-3
3.2 Manufacturing Oriented Chip Design Features	3-4
3.2.1 Bit Density Growth Plans	3-4
3.2.2 Die Size Reduction	3-4
3.2.3 Surface Contour Simplification	3-4
3.2.4 Tape Carrier Compatibility	3-6
3.3 Chip Processing	3-7
3.3.1 Manufacturing Sequence and Processes	3-7
3.3.2 Progress in Nitride Deposition	3-10
3.3.3 Progress in Photoimaging	3-13
4. ELECTRICAL TESTS AND SCREENS	4-1
4.1 Transistor Characteristics	4-1
4.1.1 Threshold Decay Characteristics	4-1
4.1.2 Pulse Response Characteristics	4-2
4.2 Memory Cell Endurance-Retention	4-3
4.2.1 Objective and Plan	4-3
4.2.2 The MNOS Test Vehicle	4-3
4.2.3 The Test Method	4-4
4.2.4 The Test Results	4-6
4.3 Wafer Probe Test	4-23
4.3.1 Overview	4-23
4.3.2 Test Categories	4-25
4.4 Hybrid Circuit Test	4-39
4.4.1 Statement of the Development Problem	4-39
4.4.2 Functional Test Station Description	4-40
4.4.3 Functional Test Station Performance	4-45

TABLE OF CONTENTS (Continued)

	Page
5. HYBRID CIRCUIT FABRICATION	5-1
5.1 Hybrid Circuit Description	5-1
5.1.1 Component Parts	5-1
5.1.2 Electrical Configuration	5-1
5.1.3 Thermal Configuration	5-1
5.2 Hybrid Substrate	5-2
5.2.1 Substrate Structure	5-4
5.2.2 Multiple Substrate Screening	5-4
5.2.3 Multiple Bonding Options	5-5
5.2.4 Automatic Probe Test	5-5
5.3 Hybrid Package	5-5
5.3.1 Standardization Approach	5-5
5.3.2 Package Options	5-5
5.3.3 Oil Canning Problem	5-5
5.4 Hybrid Processing	5-6
5.4.1 Chip Lead Bonding	5-6
5.4.2 Package Sealing	5-6
6. DISTRIBUTION LIST	6-1

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LIST OF ILLUSTRATIONS

Figure		Page
2-1	Computer System Memory Hierarchy	2-2
2-2	MNOS BORAM Advanced Development Model	2-3
2-3	Elements of AIRS	2-5
3-1	Comparison Between Protected and Unprotected Transistor Structures	3-2
3-2	MNOS BORAM Chip Growth Plan	3-5
3-3	Close-Up View of Tape Carrier Bonded 6002 Chip	3-6
3-4	Tape Carrier Bonded BORAM Hybrid	3-7
3-5	Cyclic Wafer Processing Flow Pattern	3-8
3-6	BORAM 6002 Fabrication Sequence	3-9
3-7	Sequential Cross Section of BORAM 6002	3-11
3-8	Direct-Step Wafer Aligner	3-13
3-9	Comparison of Photoimaging Approaches	3-14
4-1	Typical Initial Threshold Decay Characteristic	4-1
4-2	Typical Pulse Response Characteristic	4-2
4-3	6020 Cell Window Measurement Circuitry	4-4
4-4	Window Decay Rate as a Function of Endurance Stress	4-22
4-5	Window Voltages at 1 Hour as a Function of Endurance Stress	4-22
4-6	Endurance Retention Characteristic	4-23
4-7	BORAM 6002 Functional Block Diagram	4-24
4-8	Signal Assignment for Category No. 2 Tests	4-27
4-9	Operating Sequence for Shift Register Tests	4-28
4-10	Detailed Timing for Clocks and Data	4-29
4-11	Operating Sequences for Memory Tests	4-30
4-12	Transistor Test Structure Circuit Diagram	4-34
4-13	Operating Sequence of Group Erase	4-38
4-14	Test System Functional Block Diagram	4-41
4-15	Elements of the BORAM Functional Test Station	4-42
4-16	BORAM Hybrid Circuits in Functional Test Fixture	4-43
4-17	BORAM Functional Test Unit	4-43
4-18	Software Development Considerations	4-45
4-19	Sample of Macrocode for the Hybrid Test Program	4-46
4-20	Sample Microcode Listing	4-48
4-21	Operating Sequences for Functional Tests	4-50
4-22	Detailed Timing for Clocks and Data	4-51
4-23	Sample Production Oriented Test Report	4-53
4-24	Sample Engineering Oriented Test Report	4-54
4-25	Sequence of Operations for the BORAM Functional Test	4-55
5-1	Initial Configuration of Westinghouse Part 647R527G01	5-2
5-2	Component Parts of the Initial Configuration of Part 647R527G01	5-3
5-3	MNOS BORAM Hybrid Circuit Simplified Thermal Model	5-4

1. INTRODUCTION

Manufacturing methods and technology project number 2769758 has been successful in establishing a production capability for metal-nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random-access memory (BORAM). This final technical report for the project provides a summary of the technology, and an account of specific accomplishments of the project.

The subject is approached in Section 2 by an initial discussion of the reasons for the project and a description of goals and tasks. Section 3 examines MNOS chip fabrication. Some tutorial background and discussion of future trends is included in addition to presentation of contract achievements. Section 4 is devoted to several aspects of electrical tests and screens. Finally, the fabrication of the hybrid circuit is reviewed in Section 5.

The MNOS BORAM MM&T project has been a significant factor in the growth of the technology for military application. At present the BORAM hybrids have been selected for use by a few military programs, and several other programs are conducting tradeoff and breadboard studies. MNOS BORAM shows promise of filling serious needs for wide temperature range high density nonvolatile solid-state storage.

2. BACKGROUND

Military needs for storage of digital data in several application areas can be cost effectively met by using MNOS BORAM devices packaged in hybrid circuits. This MM&T project was the last step in the development of this technology before the engineering development of specific memory systems.

2.1 MILITARY STORAGE

The cost, reliability, power dissipation, environmental limitations, and physical bulk of digital data storage constitutes a major consideration in the implementation of a modern electronic system. This is particularly true in military applications that may involve high stress environments, or may place emphasis on achievement of some specific attribute such as small size or low power. In at least three classes of applications, MNOS BORAM shows promise of providing significant advantages over available alternative technologies.

2.1.1 Secondary Storage

The traditional approach to implementation of secondary storage is to employ a magnetic drum or disc. For many military applications this is simply not a viable alternative, because drums and discs cannot stand-up in the required environments. In fact, it was the lack of suitable secondary storage alternatives that led to definition of the BORAM concept.

The idea of a Block-Oriented Random-Access Memory and the acronym BORAM was originated by Mr. David Hadden, in June of 1963 at what was then ECOM. A BORAM was defined as an all-electronic memory with certain performance goals. No implementation technology was specified.

In most computer systems, memory is organized in a hierarchical fashion in order to achieve required capacity and performance at a tolerable cost. Figure 2-1 illustrates the general concept. Primary memory is randomly word addressable. It provides fast data access and is relatively expensive. Secondary and higher order memory may be addressable in a different fashion. Higher levels have progressively larger capacity, slower access and lower cost. Hierarchy design involves tradeoffs at each level of such parameters as access time, storage capacity and cost. The design is usually conceived to achieve some desired global objective like maximum computer throughput per dollar.

Hierarchical concepts have worked quite well in commercial computing applications, but have had little impact on many military systems. For example, it is quite common for military real time programs to be stored in main memory because the access delays associated with electromechanical storage cannot be tolerated. In some cases, the use of drums or discs is prevented by environmental considerations such as temperature or mechanical stress.

The technical feasibility of using MNOS to build a BORAM unit suitable for military use was demonstrated by the design, fabrication and evaluation of a computer secondary storage unit. This advanced development was carried out by the Westinghouse Electric Corporation under U.S. Army contract DAAB07-72-C-0236. The work was sponsored jointly by the U.S. Army Electronics Command and the Naval Air Systems Command. Module evaluations were conducted at the Naval Air Test Center and at Fort Monmouth. The final technical report was given the number ECOM-0236-5.

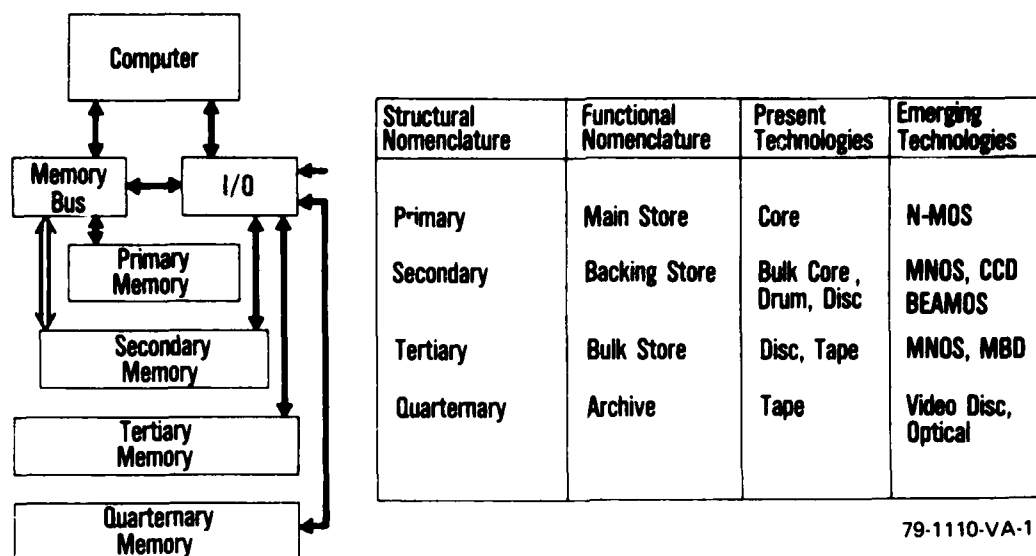


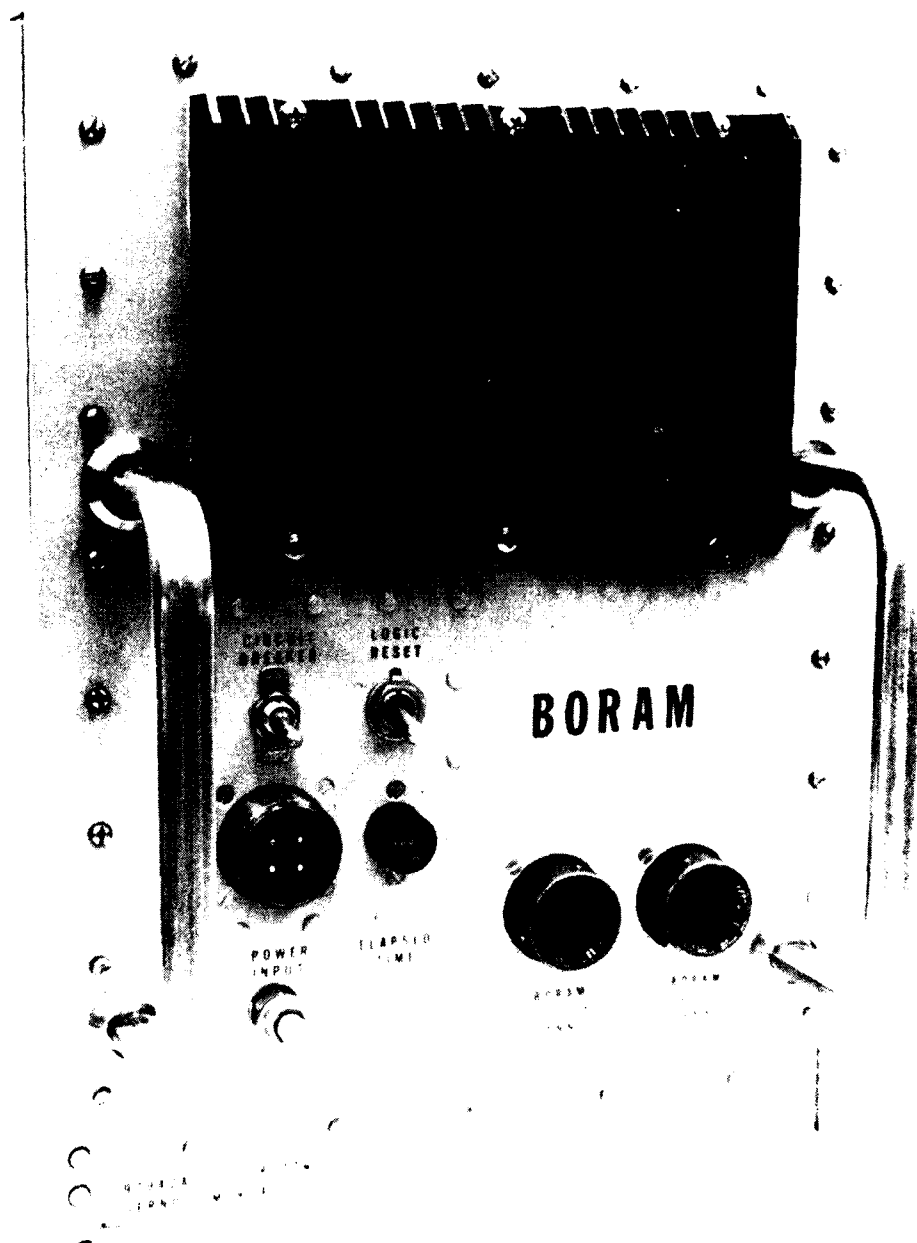
Figure 2-1. Computer System Memory Hierarchy

Figure 2-2 shows the 16.8-megabit advanced development model (ADM) that was delivered in October of 1975 with a 1/64th population. This early design confirmed that an all-electronic self-contained general purpose secondary storage unit could be built. No external controllers or power supplies were required for operation. The design avoided problems common to electromechanical storage originating from moving parts, vacuum systems, moisture and dust particles. The unit's data access delay of less than 30 microseconds was more than 100 times better than the fastest drum. No rotation latency time existed. The flow rates were designed to match the maximums allowed by the computer interface specifications. The highly modular design demonstrated volume and weight advantages over comparable fixed-head magnetic systems.

Government evaluators confirmed the performance and physical characteristics of the ADM by direct measurement. The unit was interfaced to several host computer systems and was observed to perform well. By actual demonstration, the ADM was shown to be compatible with standard military hardware and software. The flexibility of the design was shown to allow easy interfacing, and to promote built-in diagnostic capabilities.

Studies conducted on MNOS BORAM designs patterned after the ADM have tended to be positive. The Naval Air Development Center investigated the life-cycle cost of MNOS BORAM. Reliability potential was shown by models to support MTBF's on the order of 10,000 hours. Initial procurement costs were projected to be competitive with disc and drums using an 8,192-bit MNOS chip. The cost was projected to become more favorable as the bit density per chip increased. Modularity and reparability were shown to be definite assets.

Overall, the evidence indicates that MNOS BORAM can be a superior alternative to fixed-head electromechanical storage. However, it should be noted that secondary storage is only one of many potential application areas.



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Figure 2-2. MNOS BORAM Advanced Development Model

2.1.2 Airborne Recorders

The Accident Information Retrieval System (AIRS) being developed by Hamilton Standard for AVRADCOM is an example of a class of application which can benefit from the unique characteristics of MNOS BORAM. Figure 2-3 shows the elements of AIRS. Sensors monitor important variables on the aircraft, and this data is constantly examined by a microprocessor system. A history of the flight is maintained in a solid-state nonvolatile memory formed by one MNOS BORAM hybrid circuit.

The memory is a critical element of the AIRS. The mission of the system is to provide a record that will allow investigation into the cause of an accident. The data must survive in the environment of a crash, and the memory must be capable of providing reliable operation in the most hostile flight environments.

To ensure survivability, Hamilton Standard has developed a "crash protected" module to enclose the BORAM hybrid circuit. The module provides mechanical and thermal protection.

Recently, the efficiency of the protected memory was demonstrated by the successful completion of qualification tests per Federal Aviation Regulation Part 37.150, Aircraft Flight Recorders TSO-C51a. At the beginning of the test series a data pattern was written into the BORAM hybrid circuit. At the end of the stress tests the hybrid circuit was read, and the data pattern was checked. All bits were found to have been correctly retained.

The initial stress was a 1000g, 5 millisecond, 1/2 sine shock test in 6 directions. A penetration test was performed that involved dropping a sharp pointed (0.05 in³) member attached to a 500-pound weight from a height of 10 feet onto each side of the protected module. The module was also subjected to crush forces of 5,000 pounds for 5 minutes in each of the three main orthogonal axes. A flame test exposed the module to temperatures of 1100°C for a half hour over more than 50 percent of the module surface. Finally, the module was submerged in salt water for 36 hours.

The fire associated with a crash is probably the most demanding aspect of the requirements placed on the memory. Water is enclosed in the protected module around the BORAM hybrid to limit the temperature rise. Test results at Hamilton Standard show that the hybrid should not be exposed to more than 160°C. Tests by Hamilton Standard on MNOS BORAM devices have confirmed data retention after exposure to 160°C for 2 hours.

The wide temperature range of the MNOS BORAM chips is a definite asset in the AIRS. The operating temperature range is -55 to +125°C. This feature, plus nonvolatility and high density packaging make MNOS BORAM the best available technology for this type of airborne recorder.

2.1.3 Program Storage

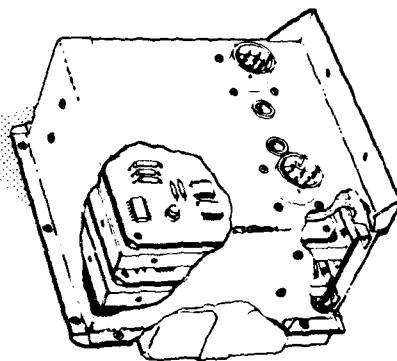
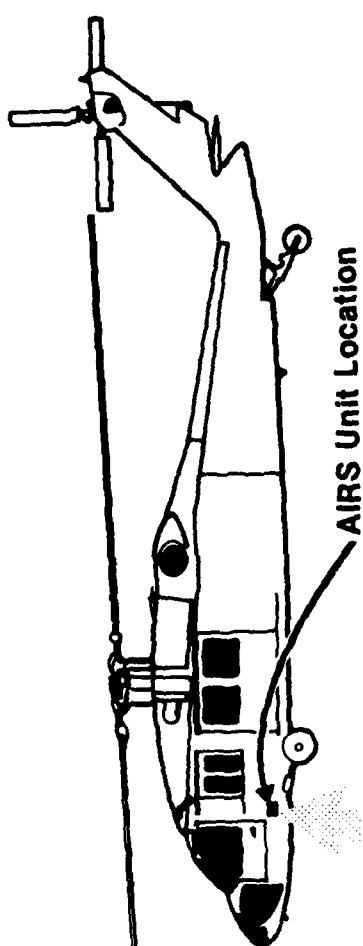
The storage of computer programs is a requirement common to almost all military electronic systems, and a variety of memory technologies have been used for this purpose. For many systems, MNOS BORAM hybrid circuits can provide a very attractive means of program storage.

MNOS BORAM is particularly suitable where electrical reprogrammability is a desirable feature. It also offers wide temperature range operation, high packaging density, low power dissipation, and high performance in a paging mode.

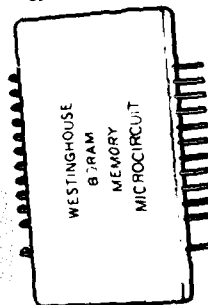
Westinghouse is currently developing a program storage card for use in radar systems. This particular design uses eight BORAM hybrids that contain 16 of the 8,192-bit BORAM chips. A single 6.4 × 8.3-inch card stores 65,536 words where each word contains 16 bits.

AIRS

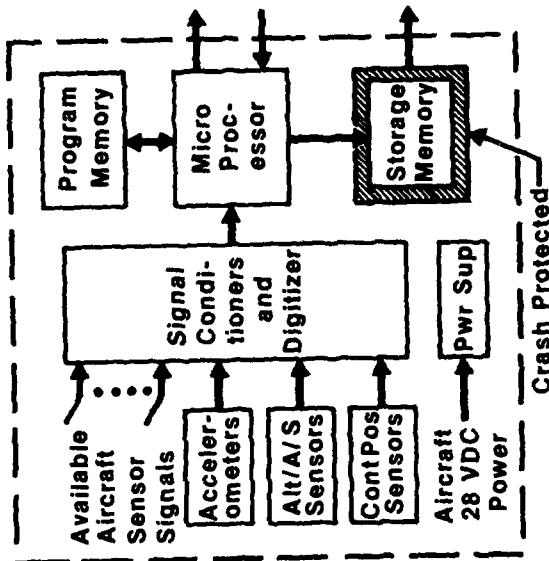
Accident Information Retrieval System



Size: 6.35" L X 5.0" H X 6.0" W



MNOS BORAM
32,768-Bit Hybrid Circuit



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Figure 2-3. Elements of AIRS

2.2 MNOS BORAM HYBRID CIRCUITS

MNOS BORAM devices packaged in hybrid circuits offer the military user several important features. While the significance of these items can only be weighed in the context of a specific application, it is well to at least tabulate them for general consideration.

2.2.1 MNOS BORAM Technology

The choice of MNOS BORAM technology over present day memory alternatives usually keys on one or more of the following features:

- Silicon IC Fabrication Technology
- Full -55 to $+125^{\circ}\text{C}$ Operation
- Nonvolatile Data Storage
- Data Access in Terms of Microseconds
- Bit Density Growth Potential
- Normal IC Voltage Interfaces
- Low-Power Operation.

The cumulative investment in silicon integrated circuit technology is an enormous magnitude. Manufacture of MNOS BORAM uses these proven materials, processes and equipment. As the art improves because of VHSIC and VLSI advances, MNOS BORAM will improve.

Because of the push of IC technology to finer geometrics, it is certain that MNOS BORAM will achieve higher bit densities per chip. Advanced circuit design studies indicate that 256K to 1M-bit chips will emerge.

Of the available nonvolatile memory technologies, MNOS BORAM is most often compared with magnetic bubbles. Bubble data-access times are many milliseconds versus tens of microseconds for MNOS. Bubble output signals are millivolts compared to volts for MNOS. The -55 to $+125^{\circ}\text{C}$ operating temperature range (with data retention nonoperating up to 160°C) for MNOS BORAM cannot be approached by even the most optimistic projections for bubble devices.

2.2.2 Hybrid Circuit Packaging

MNOS BORAM is conducive to very simple high density packaging. A BORAM hybrid need contain only the memory chips. The permanent magnets and field coils associated with bubble devices are not required.

Obviously, MNOS BORAM chips can be placed in a wide variety of single or multiple chip packages. Westinghouse has used dual in-line packages, flat packages, leadless carriers and multichip hybrid packages (MHP). For the broadest range of military applications, the hybrid package offers the best density and lowest cost.

Hybrid circuit density advantages are obvious to most observers, but the economics of the hybrid approach may not be. The cost of one hybrid containing 16 chips should be compared to the cost of 16 discrete packages. For military use, a significant portion of the device cost is associated with testing and screening. The cost to test and screen one hybrid (including yield loss) is only slightly more than the cost to test and screen one discrete package. This cost on a per chip basis strongly favors the hybrid approach.

2.3 MM&T PROJECT

During the early 70's the potential of MNOS BORAM was well recognized within the Army. Technical feasibility had been proven, but questions concerning producibility still existed. It remained for a manufacturing methods and technology project to face the practical issues of achieving an economically viable production capability.

2.3.1 Project Goals

The purpose of MM&T project number 2769758 was to establish a production capability for metal-nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random-access memory (BORAM).

At the conclusion of the effort, the Government was to have a source of supply for MNOS BORAM hybrid circuits. A pilot production line with a demonstrated throughput capacity of 1875 hybrids per month on a 5-day week, one-shift basis was to be established.

2.3.2 Project Tasks

The MM&T effort encompassed all of the activities necessary to develop, specify, operate and debug the required production capability. In the immature phases, two sets of engineering samples were produced as a learning vehicle, and as means by which progress could be measured. After acceptable tests and test programs were established, a group of confirmatory samples were produced to prove that the product was ready for production. Extensive testing and documentation was required with the confirmatory samples. Finally, a pilot production run was performed. During the pilot run, yield and throughput information was gathered to demonstrate that the required capacity of 1875 hybrids per month had been achieved.

During the course of the MM&T project, the Westinghouse Electric Corporation acted independently to supply capital equipment and process development that enhanced the MNOS BORAM production capability. Westinghouse investment in MNOS BORAM is now approaching four million dollars.

The combined affect of the MM&T and Westinghouse efforts have produced significant progress in BORAM chip fabrication, electrical tests and screens, and in hybrid circuit fabrication. The remaining sections of this report describe those activities, and outlines individual achievements of interest.

3. MNOS BORAM CHIP FABRICATION

The MNOS BORAM 6002 chip was the primary development vehicle for the MM&T project. This discussion will treat the device structure, explain manufacturing oriented design features, and finally present the details of chip processing.

3.1 DEVICE CONSIDERATIONS

MNOS BORAM is currently fabricated using P-channel metal gate technology. The nitride-oxide dual-dielectric insulator enhances reliability and makes possible the realization of nonmemory and memory transistors within a single integrated circuit.

3.1.1 Transistor Structure

An MNOS nonmemory transistor performs the same type of functions as a conventional MOS transistor. The physical form of the MNOS device is similar to the MOS device, except that the insulator region is composed of two dielectric layers. The MNOS BORAM nonmemory transistor has 800 angstroms of oxide (SiO_2) adjacent to the silicon, and 450 angstroms of nitride (Si_3N_4) over the oxide.

Two types of memory transistors have been used in previous MNOS work at Westinghouse. Figure 3-1 compares the so-called unprotected and protected transistor structures. The major physical difference is that the thin 15 to 25 Å tunneling oxide does not overlap the P+ diffusions in the drain source protected (DSP) device.

Unprotected transistors exhibit severe degradation with use. After about 10^6 erase-write cycles the V_{HC} and V_{LC} states cannot be distinguished. This class of transistor is also difficult to employ in integrated circuit arrays because of depletion mode operation while in the high conduction state.

The DSP transistor has been shown to provide reliable memory operation beyond 10^{11} erase-write cycles. The central device design concept was to protect the thin oxide from stresses associated with material imperfections and/or electric fields. The thick nonmemory oxide employed close to the source and drain determines the gate breakdown potential. Junction fields do not affect the stability of the tunneling oxide.

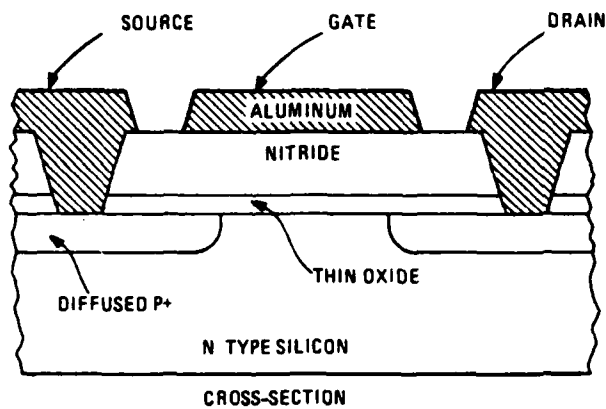
The DSP device can be thought of as a memory transistor in series with two nonmemory transistors as shown in the equivalent circuit of figure 3-1(B). The P-channel enhancement mode nonmemory transistors determine the high conductance state of the DSP structure, and therefore, the DSP device is confined to enhancement mode operation. In large integrated arrays this is an important feature. Interconnection schemes for erase, write, read and standby can be achieved without contending with difficult parasitic current problems.

Some of the advantages of the DSP transistors can be summarized as follows:

- a. Reliable memory operation for $> 10^{11}$ high field erase write cycles can be achieved
- b. Enhancement mode operation allows the parallel connection of transistors in large arrays in a manner compatible with read circuitry
- c. Drain and source breakdown voltages are increased to that of conventional nonmemory transistors

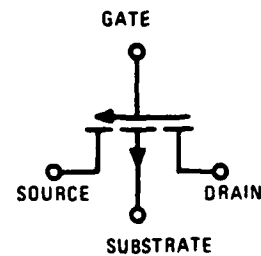
d. DSP transistor gate capacitance is reduced to about 25 percent of unprotected transistor gate capacitance. This allows four times as many DSP devices to be driven in parallel in an array with equivalent response times

e. DSP transistor gate to source capacitance is much smaller than that of unprotected transistors. Address voltage feedthrough to memory detection circuitry is reduced.

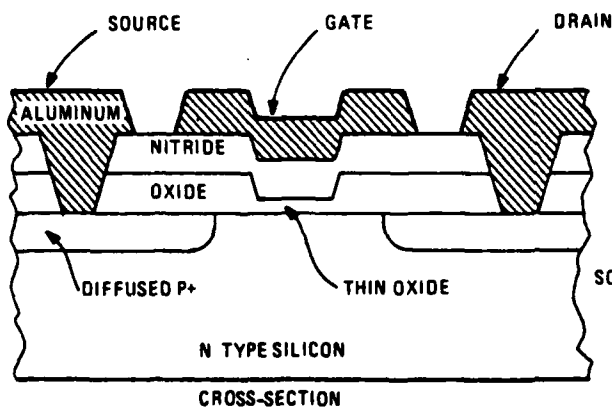


CROSS-SECTION

(A) UNPROTECTED TRANSISTOR

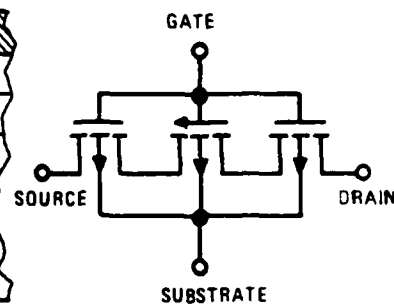


EQUIVALENT CIRCUIT



CROSS-SECTION

(B) DRAIN SOURCE PROTECTED (DSP) TRANSISTOR



EQUIVALENT CIRCUIT

79-1110-VA-3

Figure 3-1. Comparison Between Protected and Unprotected Transistor Structures

3.1.2 BORAM Integrated Circuits

At Westinghouse, BORAM integrated circuit development has been concurrent with memory system development. As a result the best characteristics of the MNOS technology have been intelligently applied to achieve computer secondary storage requirements.

To achieve cost effective performance, a solid-state computer secondary storage unit must provide fast write and read capability. RAM organized MNOS electrically alterable memory chips are incompatible with this application because millisecond write times are required. To overcome this limitation, MNOS BORAM chips are designed for 10 to 100 microsecond write times, and operate in parallel on blocks of data to provide adequate data rates.

A BORAM chip contains a fully decoded random-access memory, and a shift register for data I/O. A single read or write involves the transfer of many bits in parallel into the shift register. The contents of the shift register may be shifted at megahertz rates. This arrangement allows the MNOS RAM to operate at modest speeds compatible with high-yield production, while the shift register maintains the high-bit transfer rate required by the application.

Experience with volatile semiconductor RAM production has shown that yield to dynamic response criteria such as access time is a major impact item. MNOS BORAM devices should suffer very little production loss to dynamic criteria. The chip circuitry when operating in a secondary storage unit will never be required to operate near the performance limits of the device.

MNOS BORAM chip development has been a process of continuous simplification and refinement over several years. Initial designs required two-level metalization and single transistor cells to achieve producible die sizes. Attempts to manufacture these devices led to identification of critical circuit and process problems. Successive designs eliminated and/or avoided these difficulties (see table 3-1).

The most successful design prior to this project was the BORAM 6000C. It employs a single-level metal interconnect and a two-transistor cell. The two-transistor cell has proven to be a major factor in high-yield production in the presence of variability of transistor characteristics. It has also improved the opportunities for thorough test of the memory array, and provides longer effective data retention times than single transistor cells.

Table 3-1. Chip Evolution - Process and Topology Simplification

DEVICE NUMBER	FIELD THRESHOLD SUPPRESSION APPROACH	DIE SIZE mils	MASKING OPERATIONS	METAL LAYERS	TRANSISTORS PER CELL
6000	Nitride field shield	154 x 175	11	2	1
6000A	Nitride field shield	154 x 170	12	2	1
6000A	Ion implant	154 x 170	12	2	1
6000B	Channel stoppers	151 x 169	8	1	1
6000C	Channel stoppers	163 x 169	8	1	2
6002	Ion Implant	99 x 128	9	1	2

79-1110-TA-4

3.2 MANUFACTURING ORIENTED CHIP DESIGN FEATURES

The cost effectiveness of MNOS BORAM will be affected by many factors which come into play at different levels of product use and manufacture. In particular the long term growth and application of the product should be considered. Of immediate concern is the need for the design to be compatible with the natural variability of current materials and processes.

3.2.1 Bit Density Growth Plans

Because of the strong development trends in the semiconductor industry, and because of detailed circuit design projections, it is known that the number of bits per BORAM chip will increase sharply in the near future. Westinghouse is concerned that the investment in production capability and in circuit and system development not be made obsolete by the thrust to higher bit density.

To accomplish this purpose, Westinghouse established a plan for controlled growth of bit capacity per chip. As shown in figure 3-2, a series of chips called the 6002, 6008, 6016, and 6065 were planned. Therefore, the bits per chip grows from 2K to 8K to 16K, and then to 65K.

All of the chips in the series are pin for pin compatible. A larger device can be used in place of any smaller device. This controlled growth scheme allows conversion of memory systems based on the smaller chips to the larger chips with minimum cost impact.

Each chip is of course an evolutionary improvement over the preceding device, and necessarily incorporates new features which enhance utility and yield. For example, the 6008 device has lower dissipation and more relaxed waveform timing requirements than the 6002 chip.

3.2.2 Die Size Reduction

A first principle of silicon IC design is to make the die as small as possible consistent with available process limitations. Small die area improves yield and increases the number of dice per Wafer. An early objective of the MM&T was to simplify and shrink the BORAM chip.

The point of reference at the beginning of the effort was the 6000C chip that measured 163×169 mils. The reduced die, the 6002 chip, measured 99×128 mils. This is 46 percent of the 6000C area.

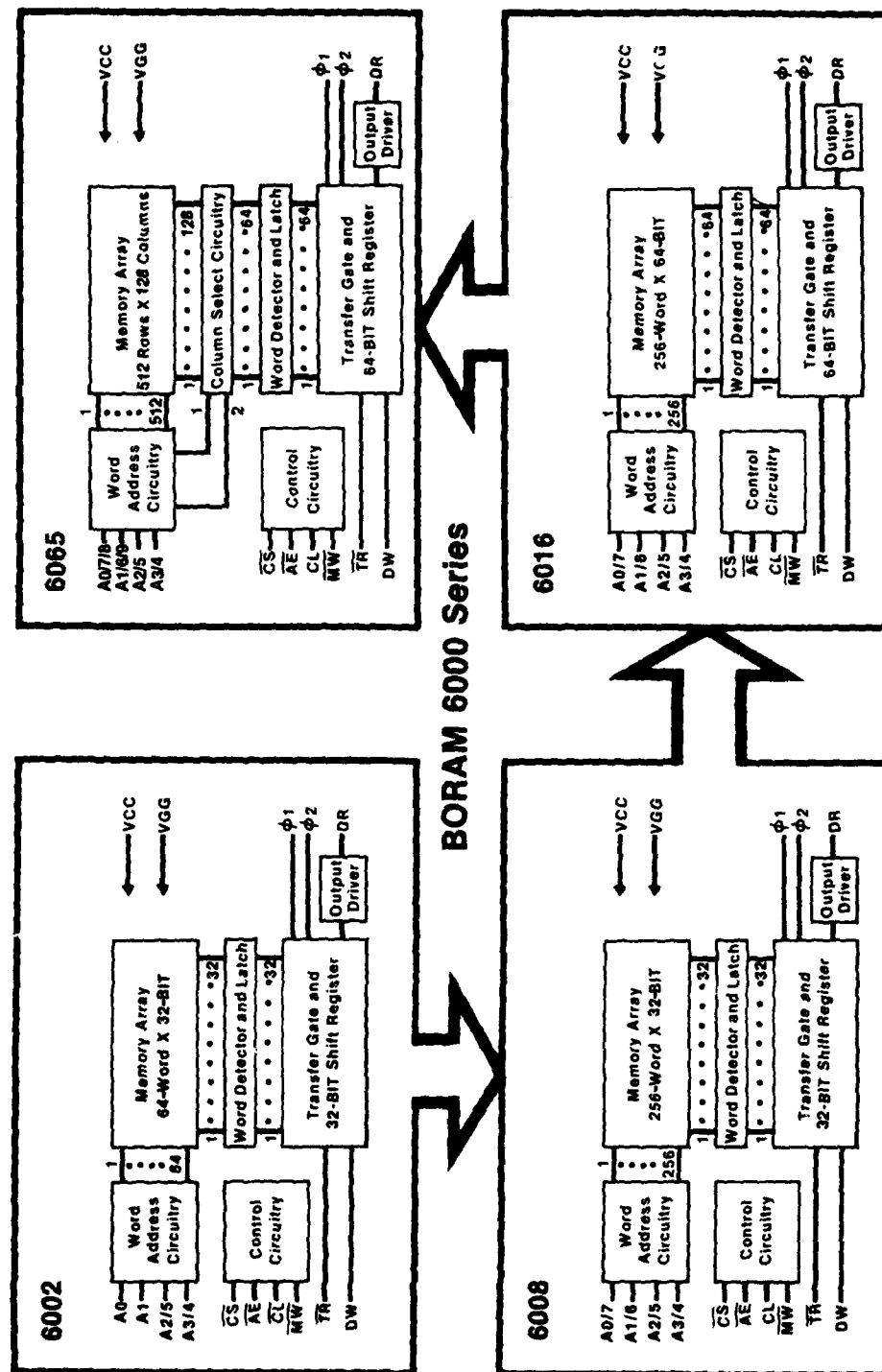
Area compression was achieved in the memory array portion of the chip by using two row address decoders. The decoder pitch on either side of the array was approximately the same as that for earlier designs, but because the left and right row selection circuits were interleaved the cell density was almost doubled.

3.2.3 Surface Contour Simplification

An important consideration in integrated circuit manufacture is to ensure that the interconnect metal will maintain adequate thickness over the surface contours of the die. If the chip design contains abrupt steps of dimensions which approach the thickness of the metal, significant yield and reliability problems can be expected.

The design of the 6000C incorporated an approach which held the largest step to a reasonable magnitude, and caused that step to be "beveled" or sloped. It was desired to maintain that same advantage for the 6002 chip.

The largest step in insulator thickness occurs where the metal enters or leaves a field region. The 6000C controlled field parasitics by using channel stoppers. The 6002 employs an ion implant to raise the field inversion threshold. This approach requires less chip area and maintains the same simplified surface characteristics.



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Figure 3-2. MNOS BORAM Chip Growth Plan

The field silox consists of 7000A undoped oxide and 3000A of doped oxide. During the gate and contact etch, the high etch rate of the doped oxide causes a sloping of the oxide steps. Cleaning before metal deposition then removes all of the doped oxide.

3.2.4 Tape Carrier Compatibility

During the MM&T project and for near-term production, gold ultrasonic wire bonding will be used. In 1980 and 1981 the process will be converted to tape chip carrier. One design consideration for the 6002 was to maintain compatibility with tape carrier technology.

To ensure that the future conversion would not encounter unusual problems, Westinghouse initiated tape carrier development in parallel with the MM&T activities. Figure 3-3 shows a closeup of a 6002 device with tape carrier leads. Figure 3-4 shows a hybrid circuit populated with tape bonded 6002 chips.

Westinghouse has fabricated and tested tape bonded BORAM hybrids using several different types of tape and processes. These experimental devices are being used as development vehicles to prove the processes and tooling, and to confirm the reliability of the end product.

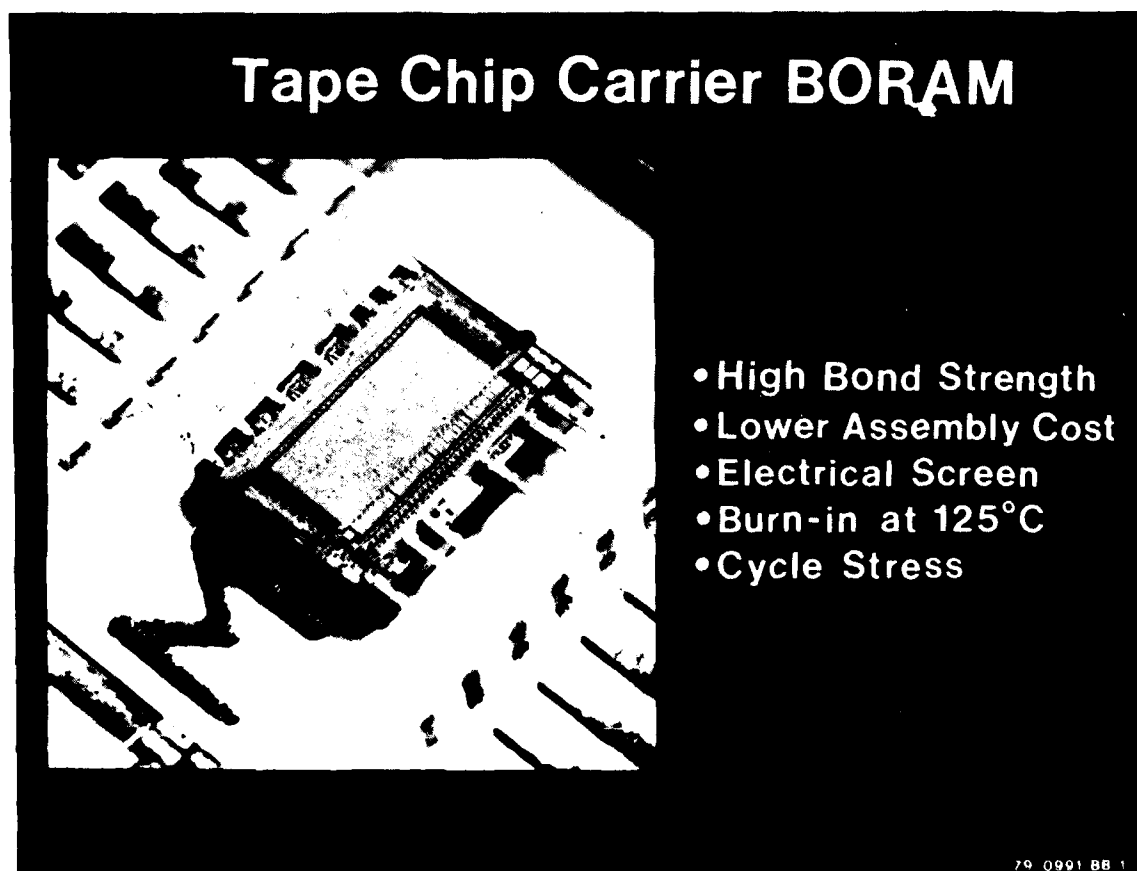


Figure 3-3. Close-Up View of Tape Carrier Bonded 6002 Chip

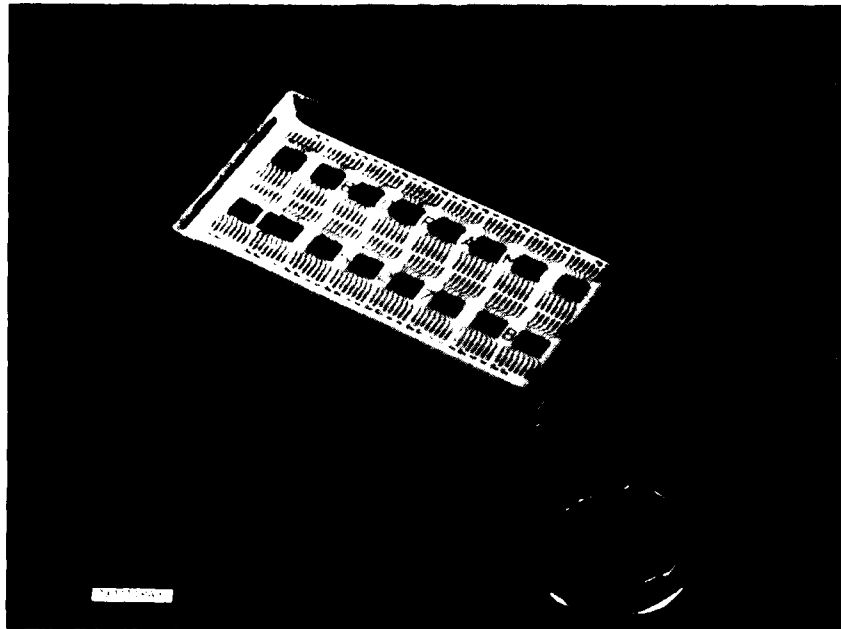


Figure 3-4. Tape Carrier Bonded BORAM Hybrid

3.3 CHIP PROCESSING

The Westinghouse MNOS BORAM chip processing sequence involving nine masks was established at the beginning of the MM&T project. During the course of the effort significant improvements were made in nitride deposition and in photoimaging.

3.3.1 Manufacturing Sequence and Processes

Two objectives were kept in mind during the development of the MNOS BORAM wafer processing sequence. The first was simplicity — reduce the sequence to the minimum number of maskings and avoid yield impacting topological features. The second objective was to use only well known and characterized individual process steps. By doing this, the risks in manufacturing would be minimal.

Figure 3-5 provides a simple concept of how material flows during MNOS BORAM fabrication. The characteristic cyclic nature of semiconductor manufacture is evident. A wafer is first prepared by some photo and/or chemical process step, and then it is given some treatment which modifies the surface structure of the wafer.

The modification operations are oxide growth, diffusions, and depositions. These stations see the wafer only one time during fabrication. The photolithographic, etching and cleaning processes see the wafer many times. Photo processing experiences the highest work load volume.

MNOS BORAM starting material is a $\langle 100 \rangle$ silicon epitaxial wafer. The substrate is 20 to 40 ohm cm. An N type 10^{15} cm^{-3} epitaxial layer $14 \mu\text{m}$ thick exists on the processing surface. Figure 3-6 shows the process sequence. Cleaning processes are described in table 3-2. Figure 3-7 illustrates how the wafer cross section is modified after various steps. Table 3-3 summarizes the various insulator thicknesses.

Cycles (1) to (4) form the P-, N+ and P+ diffused layers. Conventional deposition and drive sequences are employed. Table 3-4 summarizes the diffusion conditions. Cycle (5) forms the nonmemory transistor gate oxide. This heat treatment also continues the P+ drive.

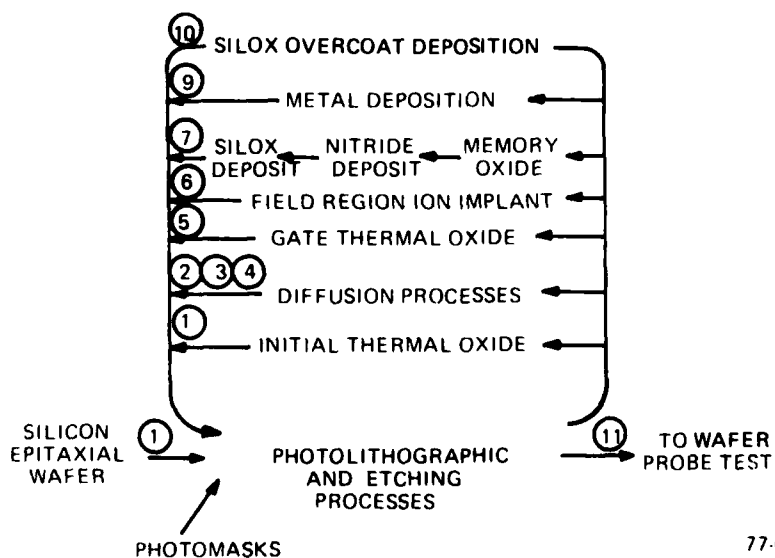
Cycle (6) is an ion implantation step which is used to reduce the resistivity of the N epi in the field regions, and thus to increase the field parasitic threshold voltage.

Cycle (7) is the heart of the MNOS process. The memory oxide and nitride layers are formed. Control of the tunneling oxide and the nitride are critical to achievement of proper memory characteristics.

Cycle (8) opens contact windows to silicon by a 2-step etching process. The contact photomask is used to etch through the silox layer. Photoresist is then removed, and the silox layer serves as a mask for the nitride etch. This leaves the gate oxide still in contact windows.

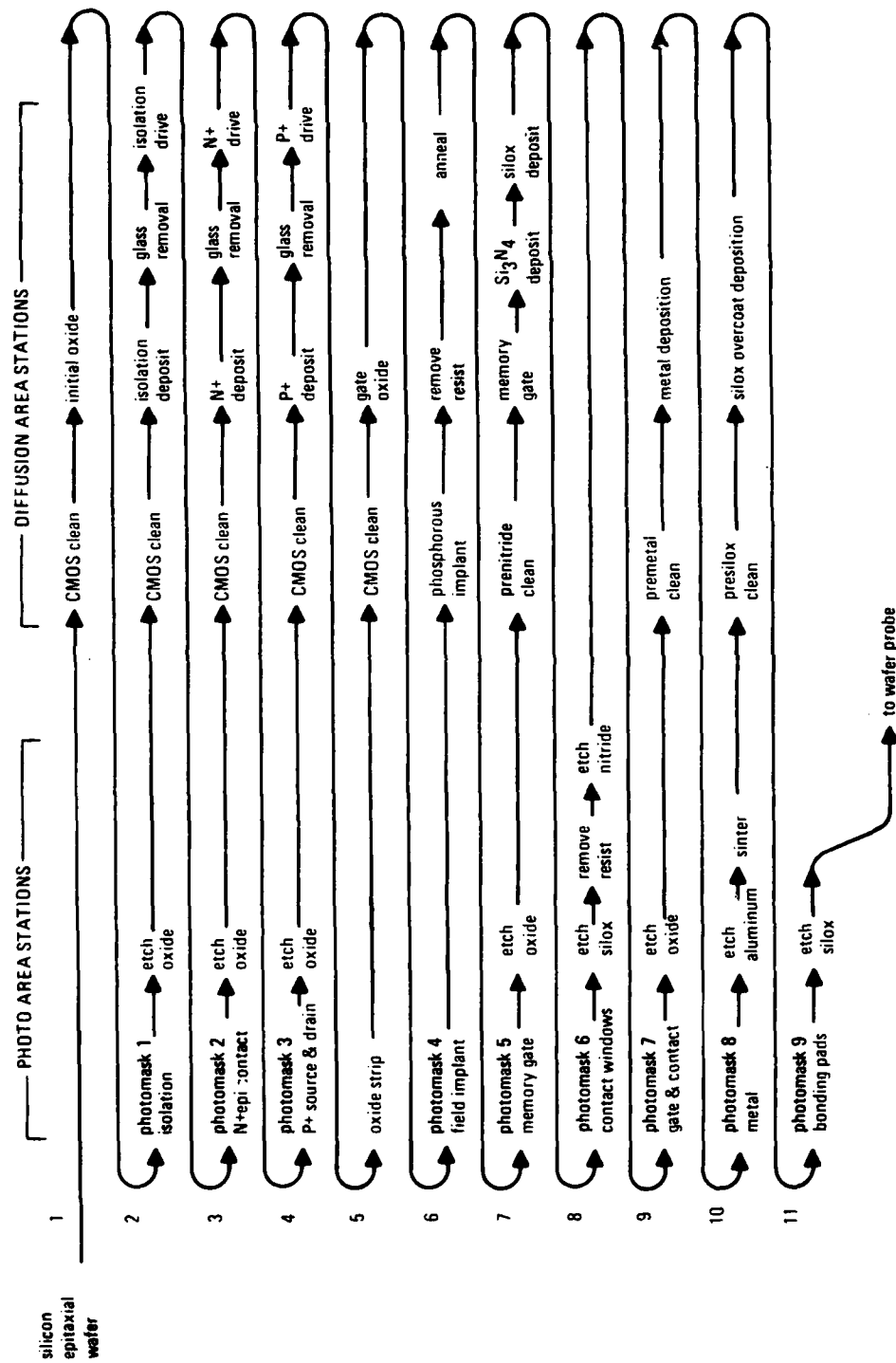
Cycle (9) applies photoresist everywhere except in the gate and contact windows. The contact windows on mask 7 are purposely defined as smaller than the contact windows on mask 6. This forms a stair step structure for metal cross-overs going down to the silicon. An oxide etch is performed which removes the silox over gates and removes the thermal oxide over contacts. Then an aluminum-silicon layer is deposited over the wafer.

Cycle (10) defines the aluminum interconnect pattern, sinters the contacts to silicon, and overcoats the wafer with silox. Finally cycle (11) concludes the sequence by removing the silox overcoat from the bonding pads.



77-0520-VA-3

Figure 3-5. Cyclic Wafer Processing Flow Pattern



77-0520 VA-6

Figure 3-6. BORAM 6002 Fabrication Sequence

Table 3-2. MNOS BORAM Cleaning Processes

Process	Sequence of Operations										
CMOS Clean	H ₂ SO ₄ 175°C 10 min	 DI Rinse 25°C	 HNO ₃ 80°C 15 min	 DI Rinse 25°C	 HF 10:1 15 sec	 DI Rinse 25°C	 DI Rinse 100°C	 Dist H ₂ O Rinse 25°C			
Pre Nitride Clean	H ₂ SO ₄ 175°C 10 min	 DI Rinse 25°C	 HNO ₃ 80°C 15 min	 DI Rinse 25°C	 HF 100:1 60 sec	 DI Rinse 25°C					
Pre Metal Clean	H ₂ SO ₄ 175°C 10 min	 DI Rinse 25°C	 HNO ₃ 80°C 15 min	 DI Rinse 25°C	 HF 10:1 15 sec	 DI Rinse 25°C					

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3.3.2 Progress in Nitride Deposition

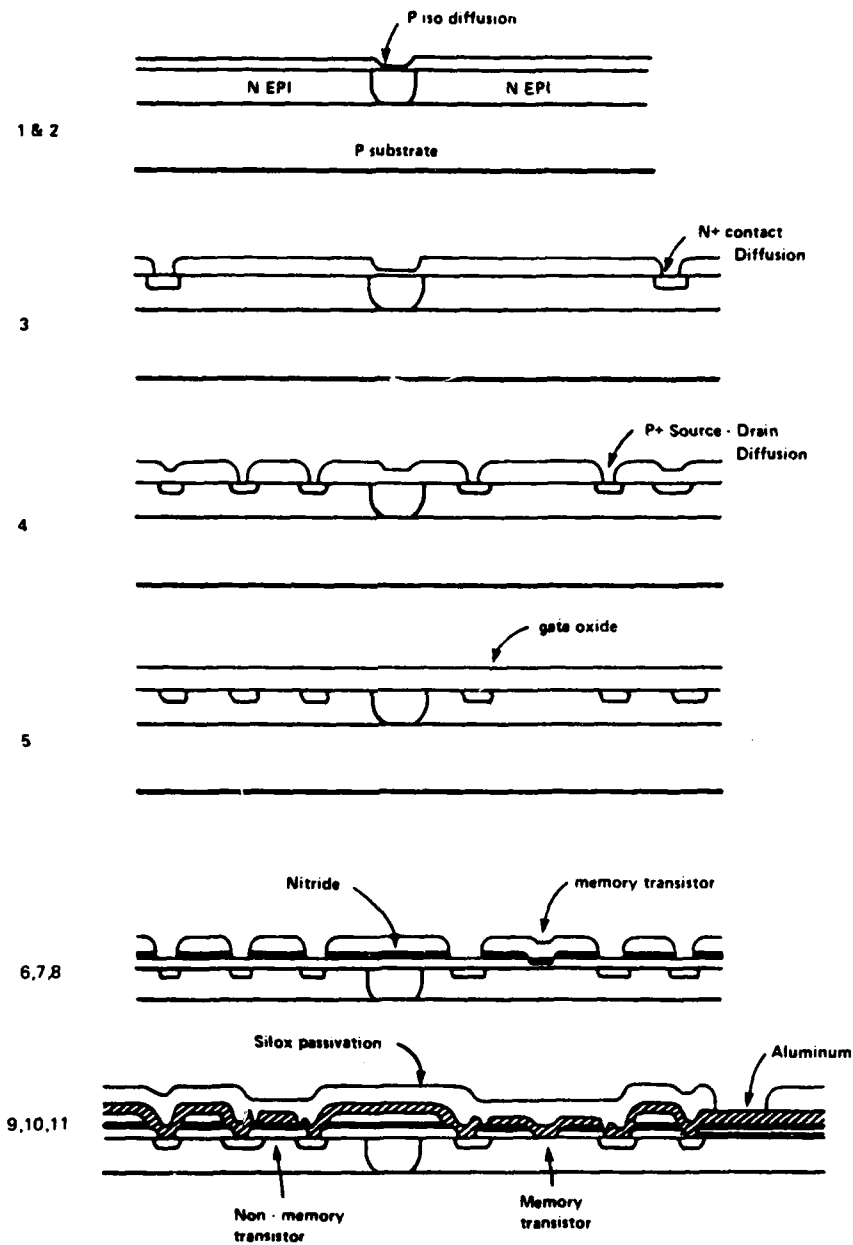
At the beginning of the MM&T project a matter of some concern was control of the nitride. In particular, it was known that electric field stresses on the tunnel layer were very sensitive to the nitride thickness. Thin nitride could lead to excessive stress and rapid degradation of retention characteristics.

The baseline nitride process was an atmospheric pressure chemical vapor deposition (APCVD). Control of nitride thickness was investigated by ellipsometer measurements. Observations of thickness in the center of the wafer showed a coefficient of variation of ± 8.5 percent within a run, and ± 23.5 percent run-to-run. Observations of thickness across individual wafers showed coefficients of variation from ± 1.9 to ± 3.8 percent depending on wafer position in the susceptor.

Nitride thickness control was improved considerably by a change from APCVD to low pressure chemical vapor deposition (LPVCD). Within run variability has improved to ± 2.0 percent, and run-to-run variability is ± 3.2 percent. Uniformity across a wafer is ± 0.9 percent.

Before converting to LPCVD, investigations were carried out to determine the properties of MNOS transistors made using various LPCVD process parameter settings. Pulse response, charge decay slopes and endurance were examined. The final LPCVD process was shown to provide performance acceptable for BORAM applications. Moreover, the range of variability of transistor characteristics was observed to reduce sharply.

The introduction of LPCVD was a major contribution toward achievement of reliable low-cost production. It should be noted that this advance came about because MNOS is a silicon IC technology, and it will make use of the improvements made in that technology. LPCVD equipment was developed and is being marketed to the semiconductor industry for a variety of applications.



79-1110-VA-7

Figure 3-7. Sequential Cross Section of BORAM 6002

Table 3-3. MNOS BORAM 6002 Structure

Topological Region of Chip	Material	Nominal Thickness (angstroms)
Field Region	• Silox • Metal • Silox • Nitride • Oxide	10,000 10,000 7,000 465 800
Nonmemory Gate Region	• Silox • Metal • Nitride • Oxide	10,000 10,000 465 800
Memory Gate Region	• Silox • Metal • Nitride • Tunneling Oxide	10,000 10,000 465 ~020

79-1110-TA-8

Table 3-4. Summary of Diffusion Steps for MNOS BORAM

Diffusion	Dopant	Deposition				Drive		
		Temp (°C)	Preheat (minutes)	Dep (minutes)	Flush (minutes)	Temp (°C)	Wet (minutes)	Dry (minutes)
Isolation	Boron	1150	5	30	1	1200	10	510
N+	Phosphorus	950	5	14	1	1000	90	5
P+	Boron	1100	5	15	1	900	20	0

79-1110-TA-9

3.3.3 Progress in Photoimaging

One advancement in BORAM manufacture came about too late to be included in the MM&T activity, but it is of such significance that it deserves mention. This is the use of a direct-step wafer (DSW) aligner shown in figure 3-8.

In order to understand the significance of the DSW it should be compared with the processes used during the MM&T. Figure 3-9 provides a summary of the two approaches.

The MM&T made use of an automated plate production system. Chip design and layout was accomplished using a CALMA design system that features multi-terminal input stations, powerful software, and large storage capability. A computer controlled David Mann Pattern Generator and Photo-Repeater provided positional accuracies and line width tolerances to one-quarter of a micrometer. Working photomasks are derived from a series of contact printing operations that originate from one master print and a set of submaster prints. Photoimaging on the wafer is accomplished by aligning a working photomask with a given wafer, bringing the mask into contact with the wafer, and then exposing the photoresist.

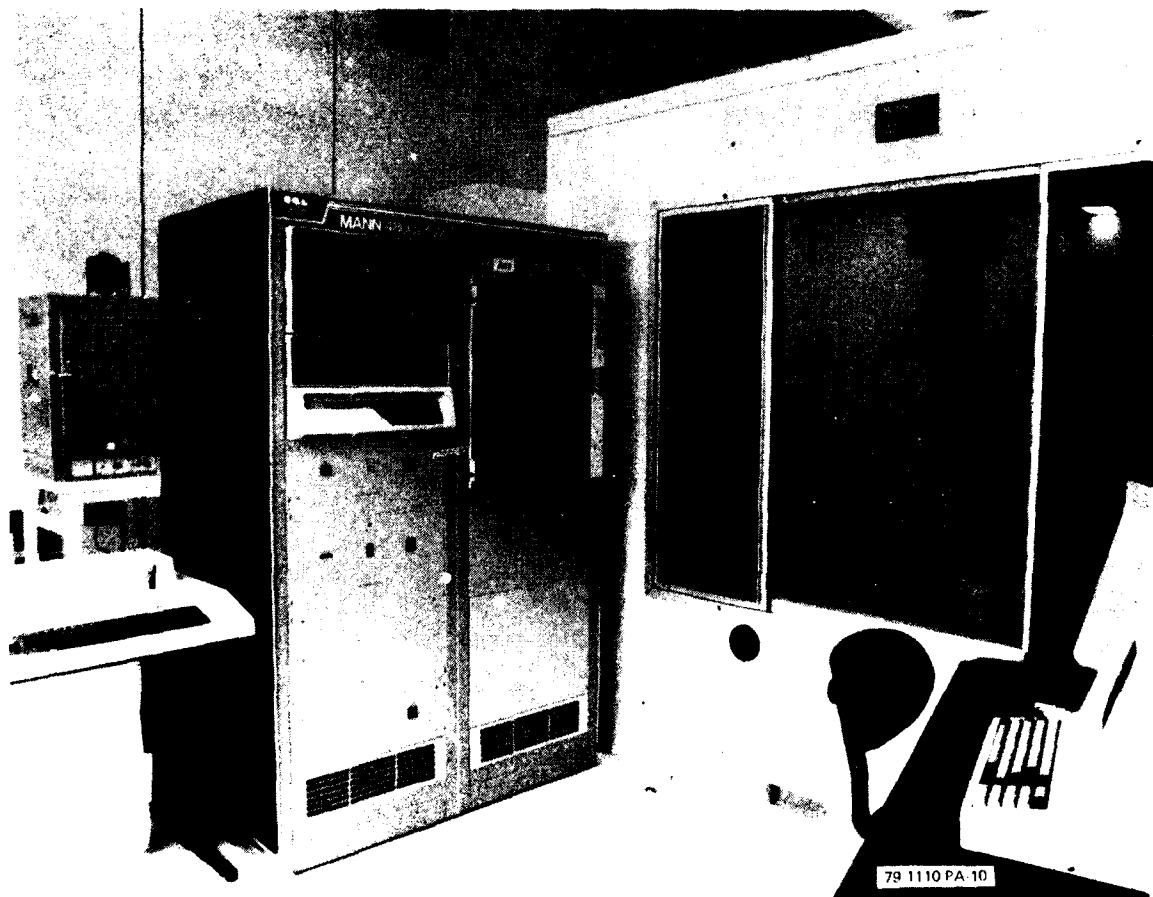


Figure 3-8. Direct-Step Wafer Aligner

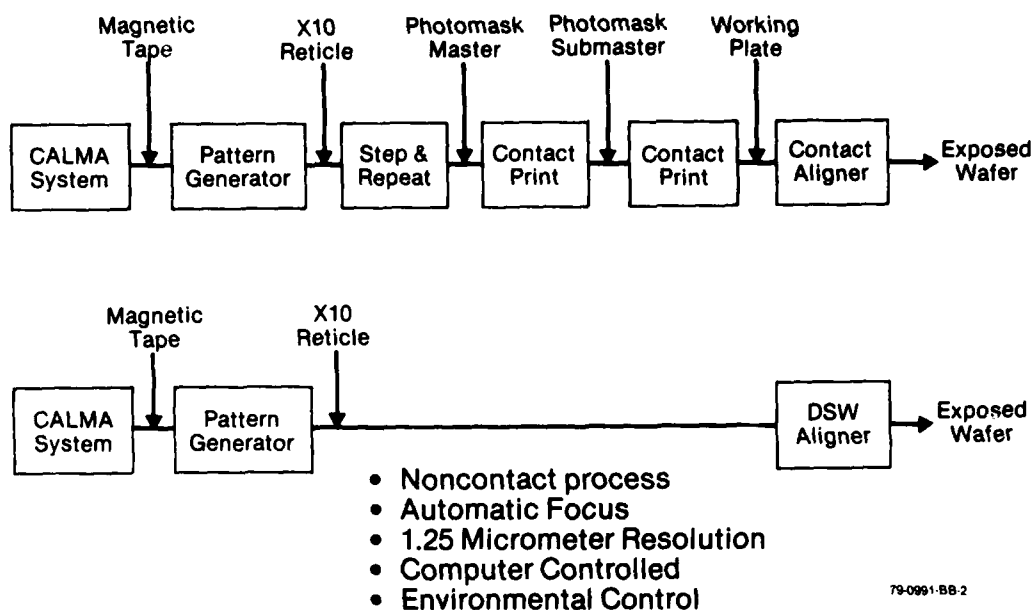


Figure 3-9. Comparison of Photoimaging Approaches

In the DSW approach, an X10 reticle is used to optically project the image of a single die directly onto the wafer. The wafer is mounted on a movable stage, and the wafer is automatically repositioned to allow exposure of each die site. The DSW approach eliminates the manufacture and control of one-to-one photomasks.

The DSW approach provides several advantages over previous methods. First it is noncontact printing. Because the mask and wafer do not touch, no damage is introduced to either the mask or the photoresist coating. Second, the DSW mask is much less critical for small imperfections. The DSW reticle is X10, and a defect would have to be on the order of 10 micrometers in size in order to be resolved on the wafer. Third, the DSW provides better than a factor of two improvement in registration and alignment over one-to-one projection systems. The unit is capable of $\pm 0.35 \mu\text{m}$ (three sigma) registration with $\pm 0.1 \mu\text{m}$ alignment error.

The DSW features laser metering of the stage placement, light integration for constant exposure energy, computer control of the system, and automatic focus maintained by photoelectric detection of the surface within each image area. The DSW is capable of routinely producing 1.5 to 1.75 micrometer lines in positive resist.

Experience with the DSW has resulted in sharply increased yields on BORAM 8K-bit chips. Because of the ability to process finer lines and spaces, it has opened the door to immediate reductions in die size. Also progress toward higher bit capacities per chip has been accelerated.

4. ELECTRICAL TESTS AND SCREENS

One of the primary tasks for the MM&T project was to completely define the BOREM product test procedures. In working toward that objective several intermediate investigations had to be carried out. Four different levels of test were treated: transistors, cells, wafer probe and hybrids.

4.1 TRANSISTOR CHARACTERISTICS

The threshold decay and pulse response characteristics of memory transistors were investigated using a special test unit called the "VT tester." Test samples were obtained from the test patterns included on each BOREM 6002 die.

4.1.1 Threshold Decay Characteristics

Figure 4-1 shows the typical form of the threshold decay characteristic. The upper curve presents the decay of the high conduction threshold or cleared state. The lower curve presents the decay of the low conduction threshold or written state. Threshold voltages are measured at 10 microamps. The abscissa is the read delay time in hours. Hours are used instead of the device physicist's usual practice of seconds, because BOREM retention is specified in hours. The test conditions and the data presentation format were chosen to approximate practical BOREM application conditions.

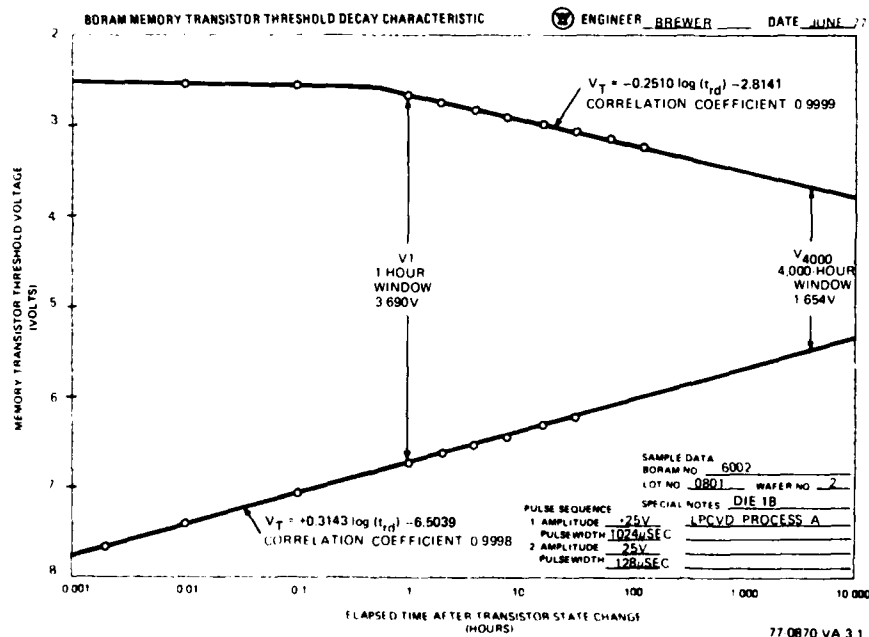


Figure 4-1. Typical Initial Threshold Decay Characteristic

The written state was established by applying a VGS pulse sequence of +25 volts for 3.6 seconds and -25 volts for 128 microseconds, repeated 16 times. Therefore, the transistor should be a saturated clear state prior to the write pulse. The write is generally not sufficient to establish a saturated low conduction threshold.

Observations of the threshold voltage began at 0.001 hours (3.6 seconds) after termination of the write pulse. Additional measurements were taken at 0.01, 0.1, 1, 2, 4, 8, 16, 32, 64, and 128 hours.

The decay characteristic from the cleared state is slightly more complicated. The cleared state was established by a VGS pulse sequence of -25 volts for 3.6 seconds and +25 volts for 1024 microseconds, repeated 16 times. Therefore, the transistor should be a saturated write state prior to application of the final clear pulse. After termination of the final clear pulse, the threshold voltage was observed at 0.001, 0.01, 0.1, 1, 2, 4, 8, 16, 32, 64, and 128 hours.

4.1.2 Pulse Response Characteristics

The pulse response from a saturated state was also explored. Figure 4-2 shows the write and clear response characteristic curves for six different pulse amplitudes overlaid on one graph. The form of these curves was typical of the population.

The so-called pulse response curve is a plot of threshold voltage against the pulsewidth of the applied gate voltage. Normally, the pulsewidth scale is logarithmic. This means of displaying the dependence of threshold shift on pulse duration has come to be common practice. Quantitative values for a given curve depend on rules for the measurements, and these details must always be clearly stated.

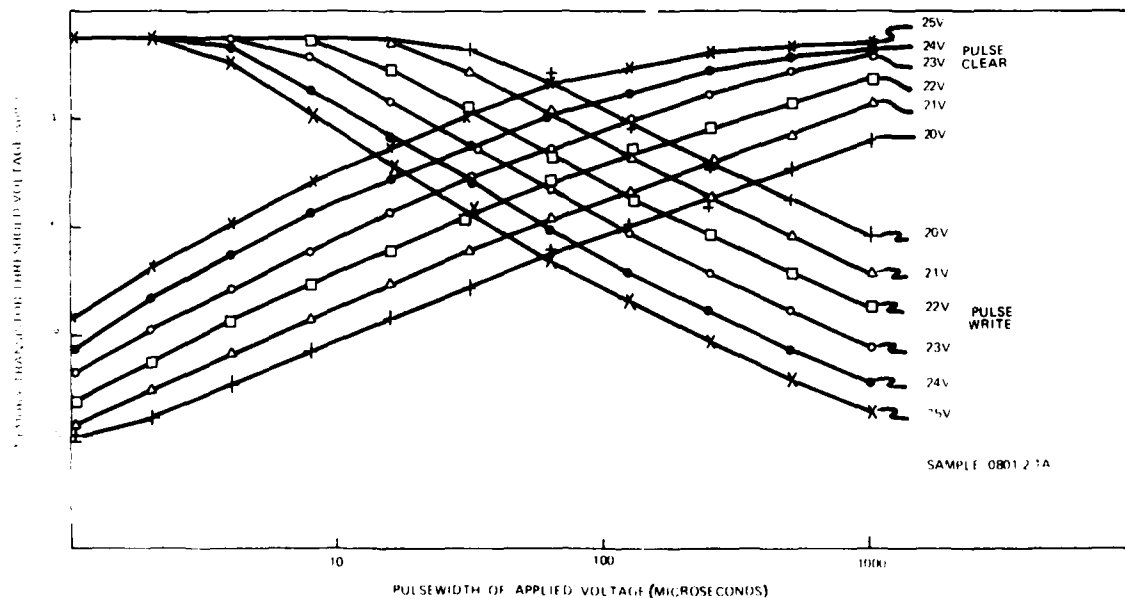


Figure 4-2. Typical Pulse Response Characteristic

One point on a write pulse response curve is obtained by initially shifting the threshold to a saturated clear level, pulsing the gate with a fixed amplitude and duration write pulse, and then measuring the threshold after a specified time delay. The procedure is repeated with a new pulsewidth to obtain additional data points. A clear response curve is similar, except that the clearing and writing pulses are interchanged.

The Westinghouse VT tester gathers this automatically and stores it in a memory for recall. The read delay time is 3.6 seconds. Pulsewidths follow the sequence 1,2,4...512, 1024 microseconds. Thresholds are measured at a drain current of 10 microamperes.

Pulse response is very important to proper operation of memory transistors in an integrated circuit array. In fact, the previously presented decay characteristic data actually contains a great amount of information related to pulse response. There the question was, does the memory transistor exhibit a combination of pulse response (window) and decay slope compatible with retention objectives.

For the pulse response characteristic curves more subtle considerations are involved. It is possible to use this data (in combination with some additional measurements) to quantify many of the parameters in device switching models.

4.2 MEMORY CELL ENDURANCE-RETENTION

A significant experiment on retention time after endurance stress was conducted on Westinghouse BORAM MNOS memory cells. Measurements of retention were collected on 512 BORAM memory cells for over 8,600 hours. Analysis of the data provided a useful guide to application of this MNOS nonvolatile memory product.

4.2.1 Objective and Plan

The objective of the experiment was to establish the endurance-retention capability of the BORAM MNOS process and memory cell design by collecting retention data on a sufficient number of cells which had been subjected to various endurance stresses. Those memory cells were to be in operating LSI memory arrays, in contrast to previous experiments on isolated single cell or single transistor test structures.

The plan for the experiment was to subject certain memory cells in the memory array of many functional memory devices to various levels of endurance stress and to determine the retention time for those cells. The experiment consisted of three steps. First, 16 cells of the memory array in 16 MNOS parts were subjected to a range of endurance stresses. The 16 cells were in one row in the memory array. Second, a pattern was written into each array. Third, the difference between the two-memory transistor threshold voltages were measured for each cell in the stressed row and for an unstressed row, at intervals of time after write which extended from 2 hours to over 8,600 hours.

4.2.2 The MNOS Test Vehicle

The Westinghouse BORAM MNOS process is used for several electrically alterable nonvolatile memory parts. One of these parts is a 1024-bit alterable ROM, called the 1K AROM, mask set number 6020. It was chosen as the test vehicle for this endurance-retention evaluation of the BORAM process because: (1) it has a memory transistor threshold test feature, (2) the memory transistor cell is processed in the same manner as for BORAM memory parts, and (3) the memory cell design is the same as that used in BORAM arrays. The test circuitry incorporated in this part permits making analog measurement of the threshold voltage for each of the two memory transistors per cell in each one of 1024 memory cells in the array.

Figure 4-3 shows the memory threshold test circuitry as a simplified schematic of the 6020 device. In normal operation, the test enable terminal (T) is LOW, connecting the memory transistor source lines to the detection latch and decoupling the test points (+ and -) from those source lines. When the test enable terminal (T) is HIGH, to enable this memory transistor threshold voltage test feature, the source lines are connected to the test points and decoupled from the detection latch.

4.2.3 The Test Method

The methods and procedures used in this experiment are described in three parts. First is the method of subjecting the parts to endurance stress with some comments on selection of parts. Second is the method of writing each part with the "zero time" retention pattern. Third is the method of measuring the thresholds of the memory transistor.

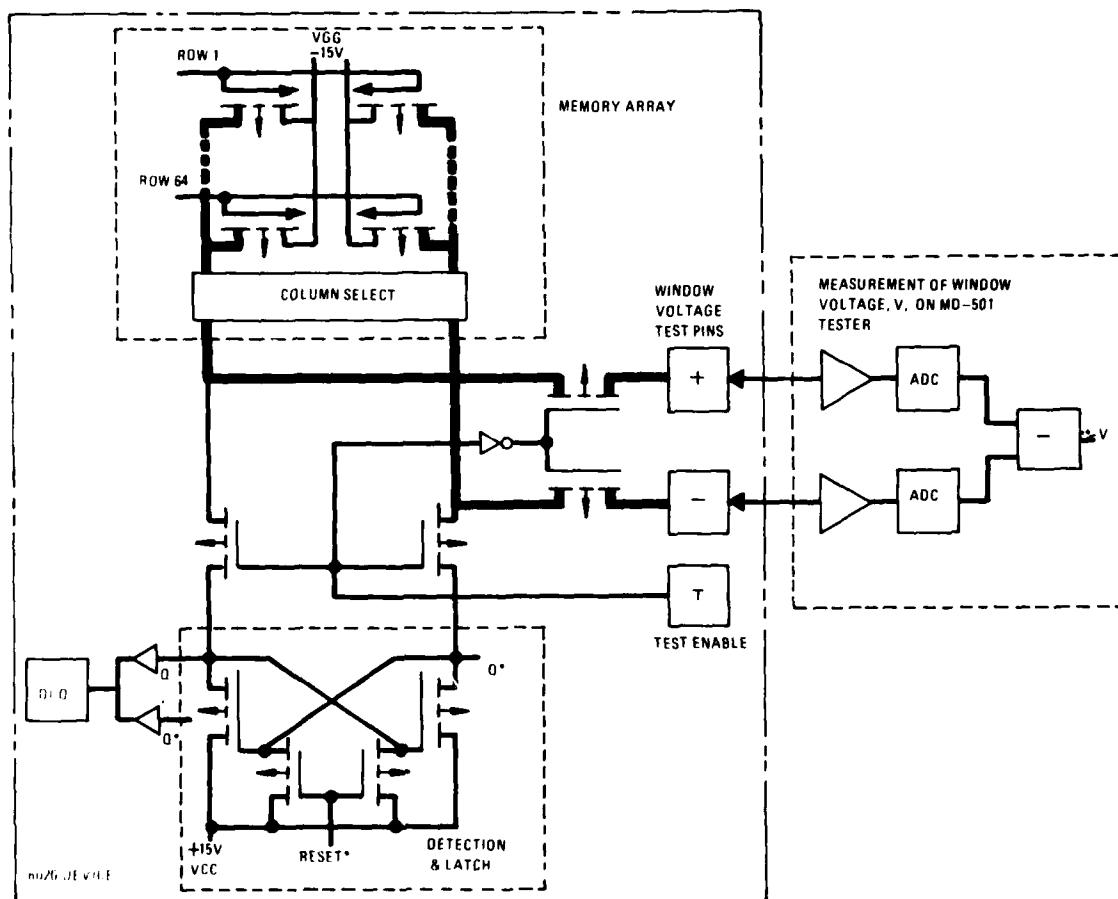


Figure 4-3. 6020 Cell Window Measurement Circuitry

4.2.3.1 Endurance Stress

Endurance stress testing for the MNOS parts involved erasing a set of memory cells, writing each cell to a certain state; then erasing the set of cells again and writing each cell to the complementary state. By repetition of these two erase-write cycles, the desired endurance stress is accumulated. These two erase-write cycles have caused each transistor in each of the memory cells to have had one reversal of threshold level, and each transistor can be said to have accumulated one endurance stress cycle.

The 6020 has row erase capability, so that one row of 16 memory cells can be cycle-stressed with the remaining 63 rows remaining unstressed. The first row was chosen for cycle stress and the second row was used as an unstressed control row. Parts were stressed using the standard BORAM voltages and erase and write times of 1,000 μ sec erase and 200 μ sec write pulsewidth. That row was first erased, then each cell in turn was written, requiring somewhat over 4.2 msec per erase-write (16 cells) cycles. For 10^4 cycles, only 42 seconds are required; for 10^6 cycles, 1 hour 10 minutes is necessary; and for 10^8 cycles nearly 5 days elapse.

Sixteen AROM 6020 parts from two process lots were made available for this experiment. The parts were not screened nor especially selected. The endurance stress on the first row of these parts was as follows:

Quantity of Parts:	2	2	2	4	3	3
Endurance cycles:	zero	10^4	10^6	10^8	10^7	10^8

A laboratory test set was used to apply repetitive erase-write cycles using a checkerboard pattern, alternating with the complement (CKBD and CKBD*). This test set was used for endurance stress at 10^4 , 10^6 and 10^8 (by running 10^6 ten times). Because internal circuitry was designed for CRT display, there is considerable "dead time" between stress cycles, so that 10^6 cycles took 1 hour 23 minutes.

For endurance stresses of 10^7 and 10^8 , a microprocessor-controlled burn-in system was used. Programming the KIM-1 microprocessor permitted application of the same BORAM standard timing. The stress pattern written into the first row was 1001100...(9999 in hexadecimal) and the complement (6666 in hex), on alternate cycles. This system had the advantage of stressing several parts in parallel.

4.2.3.2 Retention Pattern Write

After the parts were endurance stressed each was erased and written, and the time of writing was noted. This is the zero reference time for the retention measurements. Two patterns were used for the retention test. Most parts were written with all ONEs. Several parts were written with a checkerboard (CKBD) pattern. The CKBD pattern was generated by the AND of the least significant row address bit and the least significant column address bit (A0-A4).

4.2.3.3 Transistor Threshold Measurement

An electrical test program written for the Macrodata MD-501 automatic tester was used for all threshold measurements. A sample and hold voltmeter with 100 megohm input impedance was used to measure the voltage at each of the two test points (+ and -). It sampled with an aperture of about 30 nsec, and then held the voltage for the analog to digital conversion. Each test point has a 20 megohm pullup to VCC (+15V) to optimize response and minimize loading. The test program turns power ON, sets up each address in sequence, pulses chip select, waits 50 μ sec for the high impedance measurement to stabilize, then takes the sample at the (+) terminal and converts. Then the program pulses chip select, waits 50 μ sec and takes the sample at the (-) terminal. This sequence

continues through all 1024 addresses. The two measurements at each address are subtracted and the absolute value of the difference is printed. Test procedure includes incorporating the serial number of the parts, and the date and time of reading with the test printout.

The parts were separated into three groups according to when endurance stress was complete. The write and first several reads were on 3, 8 and 11 May 1978. Readings were taken at one-third to one decade intervals of time. The readings spanned a year on 16 parts with 16 stressed memory cells and 16 unstressed cells for a total of 4.49 million memory cell-hours of retention data.

4.2.4 The Test Results

In the following paragraphs the method of processing the data is described, the results of data evaluation for each part are presented, and then the analysis of data for all parts collectively is shown.

4.2.4.1 Initial Data Processing

The printout from the Macrodata MD-501 automatic tester is a set of 16 voltages per row for each 6020 part for each time of measurement. The values are differences between the threshold voltages of the two memory transistors in a cell, indicative of the memory window. Printout was obtained for the first row which was endurance stressed, and for the second row which was unstressed. Some parts were measured at 11 different times, ranging from 30 seconds after write to 8,904 hours (371 days) after write. Other parts were measured eight or ten times covering the same span of time.

Because there is generally a change of decay rate in the vicinity of an hour, the measurements made earlier than 2 hours were not included in the data analysis. From the five to seven sets of printouts for times between 2 and 8,904 hours, five sets were chosen for each part, eliminating some data where the tester or printer was clearly malfunctioning.

The data from the Macrodata MD-501 automatic tester printout and the accompanying accumulated hours since the part was written were entered into an HP9825A computer for tabulation, evaluation, analysis and summary. For each part at each time of measurement, a set of 16 values represented the cells of the stressed row, and a second set of 16 values represented the cells of an unstressed row. This data taken at five different times was assembled by the computer into two 16 by 5 matrices of values. The computer was programmed to compute a least squares fit to a linear equation of the difference voltages as a function of log time for the five data values per cell. Results of this calculation include the slope (decay rate in mV per decade of time), the intercept (window voltage in mV at 1 hour, i.e., zero on the log time axis) and the correlation coefficient of fit to the line. In addition, an estimate of retention time was made using 100 mV as the minimum voltage difference which can be reliably read by the detection circuit in BORAM memory parts. This estimate is simply a calculation of the time at which the straight line fit reaches 100 mV.

The computer stored all this data and results of calculations on magnetic tape for reference. It printed a working data sheet for each part, showing all measurement values in a matrix format and listing the results of the least squares fit. Also calculated were the mean and standard deviation (sigma) for each row of 16 cells for each time of measurement. Finally, a least squares fit to these average values was computed and printed.

4.2.4.2 Study of Data on Individual Parts

The 16 samples used for this experiment were chosen randomly from a previously unscreened population. Availability of the computer data summary provided the first opportunity to examine the detail characteristics of each sample, and to view the consistency of the data.

Three parts were dropped from the sample because of grossly atypical characteristics which would have caused rejection during normal device screening. The irregularities were small initial windows which differed significantly from that for neighboring cells. The BORAM margin test conducted at reduced write voltage eliminates devices of this nature.

Another observation based upon study of individual cell performance on all parts was that the last two cells in the first row had generally larger voltage differences than all other cells. Specifically, the 16th cell ranked first for 10 of 14 parts. In those parts, the value for the 16th cell was about 3 sigmas above the mean for the row. The value for the 15th cell ranked first for 7 of 14 parts by about 2 sigmas. As a result, the estimates of retention time for these cells are significantly longer, by 2 to 5 decades.

There are layout considerations which indicate that the end memory cells, especially in the first row of the array, could have superior retention performance. Another significant finding gained from measurement of voltage differences on the AROM lab test set was that the Macrodata MD-501 had omitted printout of the reading for cell 0, the first memory cell of the array. Thus the first 15 readings printed by the MD are for memory cell numbers 1 through 15 of the first row, and for the first cell of the second row. Because the second row was not stressed, this finding accounts for the 16th reading having a significantly larger value. Clearly, the 16th printout value should be excluded from analysis of stressed cells. Also, for the reasons earlier noted, the 15th printout value which is the last cell in the first row, should be excluded from further analysis directed toward determining an endurance-retention limit for system applications. Accordingly, the analysis which follows was based upon memory cells 1 through 14 of the stressed row on each part, omitting cells 0 and 15.

The data for 13 parts is shown in tables 4-1 through 4-13. The title for each table includes the serial number of the 6020 part and the date when the part was written, hence when the retention test started. Also given is the number of endurance cycles. For the one part that was not endurance stressed, 100 endurance cycles were assumed. The 100 clear-write cycles are shown in the title as 1E2. Each table shows the differential cell voltages measured on the Macrodata MD-501 automatic tester, in millivolts, for each cell at each of the five times measured. The results of the least squares fit for a linear equation in voltage difference as a function of log time are given for each cell. The measure of fit is shown by the "corr.coef," entry, the majority of which are 0.999 or 1.000. The slope of the line is decay rate, given by "mV/decade." The intercept of the line is the window voltage at 1 hour (where $\log t = 0$), shown by the "mV at 1 hour" entry. The estimate of retention time is denoted "hours to 0.1V" because 100 mV sensitivity is the appropriate limit of detection. These estimates are presented in exponential powers of ten notation, e.g., 4,000 hours is printed 4.00E03. A few values for 1 through 10 years are given here for reference and ease of interpretation:

1 year	2 years	5 years	10 years
8.77E03	1.75E04	4.38E04	8.77E04

Data for the 14 unstressed cells of each part was studied but not plotted. The same calculations of fit to a linear voltage vs log time relationship were made with good success. Virtually all the coefficients of correlation were 1.00. The mean of window voltage decay rate, r_v , was between 341 and 407 mV per decade, with exception of one at 158. The overall mean for all parts was 354 mV per

decade. Standard deviation of r_V for each part was between 3 and 18 mV per decade. The means of window voltage at one hour, V_1 , ranged from 3848 to 4451 mV, with an exception at 2145 mV. The standard deviations were between 14 and 217 mV. Estimates of retention time for these unstressed (under 100 cycles) parts ranged from $1.05E10$ to $1.05E13$ hours, the shortest of which is over one million years. In all, the unstressed parts performance was fairly consistent.

4.2.4.3 Analysis of Data on All Parts

A working summary of the computations for each part was developed by an additional computer program. The parts were ranked in order of increasing endurance stress and listed with the key parameters for study, plotting and evaluation. This effort was directed toward presentation of the endurance-retention data in a manner which is both informative and useful for applications guidance. The first two parameters of interest were those of the linear fit of window voltage to log time for each part. These parameters, window voltage decay rate (r_V) and window voltage at 1 hour (V_1) were plotted vs the endurance stress in erase-write cycles (N), and are shown in figures 4-4 and 4-5. The mean values are plotted as small circles with one standard deviation shown by a range bar. The data is reasonably consistent in that the standard deviations are less than 7 percent of the respective means, generally around 4 percent. In figure 4-4, two parts stressed at 10^6 cycles and two at 10^7 are seen to have smaller decay rates (r_V) than other parts of the same stress. In figure 4-5, the same four parts have larger windows at one hour (V_1) than other parts of the same stress, although the separation is less apparent here than in figure 4-4. Because the purpose of the analysis is to develop a guide to system applications, these four parts with superior decay characteristics are set aside. Using the data for the remaining nine parts, least squares fit were computed for r_V and V_1 vs $\log N$. These are shown in the same figures. They provide a good indication of the decay rate and window size to be expected from the BORAM process.

The summary of data for all parts included the estimates of retention time (t_R). The standard deviation of t_R over the 14 cells of each part was computed. A factor of 1.96 times the standard deviation was plotted to include 95 percent of the population. Actually, because parts with t_R on the high side of the mean are of no concern, attention should be focused on the low side. About 97.5 percent of the population should lie above the lower limit. In figure 4-6, these estimates and 95 percent range bars are plotted vs the number of erase-write cycles (N). Again, the four parts stressed at N of 10^6 and 10^7 are seen to have superior performance. A least squares fit of a line to $\log t_R$ vs $\log N$ was computed with these four parts excluded, as before. This estimate of t_R is very sensitive to the data for each cell of each part. Nevertheless the line is seen to fit rather well, passing quite near most of the mean values.

Of interest in evaluating endurance-retention performance is the product of $N \cdot t_R$ which has been used as a figure of merit. A value of 10^{12} has been discussed in some previous writings on the Westinghouse BORAM memory products and a dashed line in figure 4-6 shows this value. The $N \cdot t_R$ product for the calculated fit is 12.7 at 10^6 erase-write cycles and 12.8 at 10^7 cycles. A significant observation is that only a portion of the distribution for only two parts out of the 13 plotted parts lie below the dashed " 10^{12} figure of merit" line.

An observation of some interest and worthy of further study is that the decay rate seems to lessen at longer times. Such can be seen in figure 4-1. The calculated decay rate for all five measurements in time is 0.67 volts per decade, but the decay rate between 4,875 hours and 8,713 hours is 0.39 V per decade. This is seen on other parts, to a greater or lesser degree, and has been observed on different MNOS memory device designs. A calculated estimate based upon the last three measurements rather than all five would certainly indicate longer retention time.

Table 4-1. Retention Characteristic for 14 Cells From Part 6020 Serial 131
(Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3280	2930	3045	3200	3270	2965	3095
212.50	2830	2520	2615	2690	2805	2520	2685
428.50	2680	2390	2510	2535	2665	2360	2560
4947.00	2205	1970	2105	2025	2175	1945	2150
8781.00	2155	1900	2040	1970	2115	1870	2080
corr. const.	0.999	0.999	0.999	0.999	0.999	0.999	1.000
mV/decode	-434	-409	-381	-473	-444	-416	-387
mV of 1 hour	3837	3490	3522	3798	3841	3489	3589
hours to .1V	4.03E08	1.91E08	9.51E08	6.65E07	2.64E08	1.39E08	1.05E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
19.92	3205	3305	2960	3090	3200	3285	2935
212.50	2695	2835	2500	2680	2680	2815	2490
428.50	2535	2690	2365	2545	2520	2670	2330
4947.00	2025	2195	1935	2140	2010	2180	1915
8781.00	1940	2110	1870	2060	1910	2090	1840
corr. const.	1.000	1.000	0.999	1.000	1.000	1.000	0.999
mV/decode	-482	-456	-415	-391	-489	-455	-416
mV of 1 hour	3821	3896	3479	3590	3824	3874	3459
hours to .1V	5.17E07	1.07E08	1.40E08	8.37E08	4.07E07	1.93E08	1.18E08

Table 4-2. Retention Characteristic for 14 Cells From Part 6020 Serial 134
(Retention Test Started 11 May 1978 After 7E5 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
24.40	2770	2750	2745	2745	2750	2715	2795
144.50	2345	2300	2300	2315	2340	2305	2350
360.80	2130	2100	2105	2090	2125	2090	2145
4875.00	1570	1550	1540	1540	1555	1520	1570
8713.00	1475	1470	1450	1460	1460	1445	1485
corr. coef.	0.999	0.998	0.999	0.998	1.000	0.999	0.999
mV/decode	-508	-500	-506	-505	-508	-503	-514
mV at 1 hour	3453	3408	3419	3417	3442	3396	3481
hours to .1V	4.00E06	4.09E06	3.58E06	3.70E06	3.77E06	3.59E06	3.78E06

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
24.40	2740	2765	2770	2770	2735	2765	2750
144.50	2310	2345	2345	2340	2310	2340	2654
360.80	2090	2120	2120	2120	2095	2120	2100
4875.00	1535	1555	1560	1545	1535	1550	1540
8713.00	1435	1460	1475	1460	1450	1455	1455
corr. coef.	0.999	0.999	0.999	0.999	0.999	0.999	0.974
mV/decode	-511	-513	-510	-516	-505	-515	-552
mV at 1 hour	3424	3458	3454	3464	3413	3460	3616
hours to .1V	3.25E06	3.51E06	3.81E06	3.31E06	3.60E06	3.37E06	2.34E06

Table 4-3. Retention Characteristic for 14 Cells From Part 6020 Serial 148
(Retention Test Started 3 May 1978 After 1E2 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3540	3375	3505	3495	3570	3520	3580
75.00	3200	3030	3165	3150	3220	3170	3235
551.60	2865	2705	2835	2810	2885	2835	2905
5057.00	2870	2370	2505	2475	2545	2490	2565
8904.00	2480	2305	2440	2405	2475	2425	2495
corr. coef.	0.949	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-296	-353	-352	-360	-361	-362	-358
mV at 1 hour	3771	3686	3815	3813	3889	3840	3897
hours to .1V	2.41E12	1.44E10	3.66E10	2.10E10	3.13E10	2.17E10	4.12E10

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
7.66	3525	3570	3535	3615	3590	3620	3580
75.00	3180	3215	3175	3265	3250	3270	3230
551.60	2840	2880	2840	2935	2910	2935	2895
5057.00	2495	2540	2500	2590	2565	2595	2550
8904.00	2430	2470	2425	2525	2495	2530	2485
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-362	-362	-365	-360	-362	-360	-362
mV at 1 hour	3847	3888	3854	3933	3914	3937	3900
hours to .1V	2.19E10	2.86E10	1.98E10	4.47E10	3.44E10	4.57E10	3.18E10

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Table 4-4. Retention Characteristic for 14 Cells From Part 6020 Serial 151
(Retention Test Started 8 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3445	3285	3280	3465	3480	3335	3330
212.50	3060	2895	2895	3075	3085	2946	2935
428.50	2940	2780	2775	2950	2960	2825	2815
4947.00	2535	2380	2375	2545	2540	2430	2415
8781.00	2445	2300	2290	2455	2450	2350	2335
corr. coef.	1.300	1.000	1.000	1.000	1.000	1.000	1.000
mV/decode	-379	-374	-376	-383	-391	-374	-378
mV at 1 hour	3939	3768	3768	3963	3991	3817	3816
hours to .1V	1.32E10	6.37E09	5.73E09	1.21E10	8.71E09	8.64E09	6.86E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
19.92	3475	3475	3340	3355	3505	3460	3370
212.50	3085	3080	2950	2965	3115	3070	2971
428.50	2955	2960	2835	2840	2975	2945	2845
4947.00	2545	2540	2430	2450	2555	2525	2445
8781.00	2455	2450	2345	2365	2465	2440	2360
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decode	-387	-389	-378	-375	-396	-389	-383
mV at 1 hour	3980	3983	3825	3837	4024	3968	3862
hours to .1V	1.03E10	9.41E09	7.53E09	9.23E09	8.05E09	9.00E09	6.71E09

Table 4-5. Retention Characteristic for 14 Cells From Part 6020 Serial 152
(Retention Test Started 8 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3425	3340	3375	3415	3430	3345	3385
212.50	3030	2955	2990	3010	3035	2961	3000
428.50	2905	2850	2870	2890	2910	2840	2880
4947.00	2500	2455	2490	2465	2490	2450	2480
8781.00	2410	2395	2405	2390	2410	2380	2400
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-385	-360	-367	-391	-389	-368	-375
mV at 1 hour	3923	3803	3845	3921	3936	3817	3870
hours to .1V	8.68E09	1.94E10	1.62E10	5.91E09	7.30E09	1.29E10	1.16E10

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
19.92	3420	3420	3350	3370	3440	3420	3385
212.50	3015	3020	2970	3000	3030	3015	3000
428.50	2885	2895	2850	2875	2905	2885	2880
4947.00	2470	2470	2460	2495	2475	2460	2485
8781.00	2390	2390	2380	2410	2390	2380	2415
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-392	-393	-368	-364	-399	-396	-370
mV at 1 hour	3925	3931	3826	3842	3958	3934	3861
hours to .1V	5.75E09	5.66E09	1.30E10	1.89E10	4.55E09	4.68E09	1.48E10

Table 4-6. Retention Characteristic for 14 Cells From Part 6020 Serial 153
(Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3500	3100	3205	3400	3500	3120	3230
212.50	3060	2430	2565	2915	3050	2667	2790
428.50	2915	2495	2630	2765	2910	2510	2660
4947.00	2445	2060	2200	2280	2435	2080	2230
8781.00	2335	1975	2105	2190	2330	1995	2145
corr. coef.	1.000	0.976	0.979	1.000	1.000	0.999	1.000
mV/decode	-442	-406	-396	-460	-444	-427	-411
mV at 1 hour	4079	3539	3642	3989	4079	3661	3754
hours to .1V	1.01E09	3.02E08	8.70E08	2.83E08	9.16E08	2.20E08	7.68E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
19.92	3420	3525	3105	3215	3425	3510	3120
212.50	2930	3070	2645	2755	2940	3060	2666
428.50	2780	2925	2510	2640	2790	2925	2510
4947.00	2300	2445	2070	2210	2305	2450	2075
8781.00	2210	2345	1995	2120	2215	2350	1990
corr. coef.	1.000	1.000	0.999	0.999	1.000	1.000	0.999
mV/decode	-459	-449	-422	-413	-460	-441	-429
mV at 1 hour	4005	4109	3637	3735	4014	4084	3664
hours to .1V	3.15E08	8.61E08	2.44E08	6.44E08	3.21E08	1.10E09	2.04E08

Table 4-7. Retention Characteristic for 14 Cells From Part 6020 Serial 156
(Retention Test Started 3 May 1978 After 1E4 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3705	3370	3710	3380	3730	3390	3765
75.00	3360	2965	3365	2980	3380	2980	3410
551.60	2985	2555	2990	2565	3000	2565	3030
5057.00	2560	2120	2570	2125	2575	2130	2605
8904.00	2485	2025	2480	2035	2490	2040	2520
corr. coef.	0.999	1.000	0.999	1.000	0.999	1.000	0.999
mV/decade	-407	-444	-408	-446	-412	-447	-414
mV at 1 hour	4090	3776	4097	3790	4120	3796	4155
hours to .1V	6.32E09	1.88E08	6.16E09	1.90E08	5.59E09	1.89E08	6.30E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
7.66	3385	3765	3385	3760	3420	3745	3400
75.00	2980	3415	2980	3410	3010	3385	2985
551.60	2570	3020	2570	3020	2595	3000	2570
5057.00	2125	2600	2145	2595	2155	2580	2135
8904.00	2030	2510	2050	2510	2060	2495	2050
corr. coef.	1.000	0.999	1.000	0.999	1.000	0.999	1.000
mV/decade	-448	-417	-441	-416	-449	-415	-447
mV at 1 hour	3797	4160	3785	4154	3830	4133	3804
hours to .1V	1.78E08	5.35E09	2.31E08	5.49E09	2.00E08	5.18E09	1.94E08

Table 4-8. Retention Characteristic for 14 Cells From Part 6020 Serial 267
(Retention Test Started 11 May 1978 After 1E8 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
2.00	2585	2640	2560	2535	2625	2630	2550
144.50	1315	1405	1290	1065	1405	1410	1085
360.80	1065	1165	1065	1040	1165	1165	1060
4875.00	560	655	590	570	660	660	575
8713.00	400	625	540	570	640	645	515
corr. coef.	0.995	0.991	0.989	0.969	0.991	0.991	0.975
mV/decode	-593	-561	-558	-539	-553	-554	-552
mV at 1 hour	2685	2716	2620	2520	2699	2703	2554
hours to .1V	2.28E04	4.64E04	3.29E04	3.07E04	4.97E04	5.00E04	2.77E04

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
2.00	2535	2565	2590	2580	2590	2600	2970
144.50	1060	1135	1165	1115	1120	1170	1530
360.80	1035	1105	1130	1080	1095	1135	1485
4875.00	540	625	655	605	620	650	950
8713.00	465	590	625	540	595	610	915
corr. coef.	0.977	0.975	0.975	0.975	0.972	0.976	0.980
mV/decode	-561	-539	-537	-553	-545	-543	-563
mV at 1 hour	2545	2567	2591	2583	2582	2606	2994
hours to .1V	2.30E04	3.78E04	4.36E04	3.08E04	3.59E04	4.13E04	1.38E05

Table 4-9. Retention Characteristic for 14 Cells From Part 6020 Serial 269
(Retention Test Started 3 May 1978 After 1E4 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3680	3390	3645	3330	3585	3305	3580
75.00	3305	2985	3250	2925	3200	2900	3190
551.60	2905	2585	2865	2530	2800	2510	2780
5057.00	2485	2175	2440	2135	2365	2120	2345
8904.00	2395	2095	2350	2050	2280	2035	2260
corr. coef.	0.999	1.000	1.000	1.000	0.999	1.000	0.999
mV/decode	-426	-428	-427	-422	-433	-418	-438
mV at 1 hour	4075	3773	4034	3704	3985	3674	3984
hours to .1V	2.14E09	3.76E08	1.61E09	3.49E08	9.35E08	3.53E08	7.28E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
7.66	3310	3570	3310	3575	3355	3615	3400
75.00	2890	3180	2890	3180	2935	3230	2990
551.60	2495	2775	2490	2780	2540	2820	2590
5057.00	2085	2340	2080	2345	2130	2385	2180
8904.00	2000	2240	2000	2255	2050	2300	2100
corr. coef.	1.000	1.000	1.000	1.000	1.000	0.999	1.000
mV/decode	-431	-439	-432	-437	-430	-437	-430
mV at 1 hour	3691	3977	3691	3976	3734	4020	3782
hours to .1V	2.11E08	6.66E08	2.03E08	7.48E08	2.78E08	9.34E08	3.72E08

Table 4-10. Retention Characteristic for 14 Cells From Part 6020 Serial 270
(Retention Test Started 3 May 1978 After 1E5 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3475	3120	3475	3110	3445	3100	3465
75.00	3070	2645	3075	2655	3045	2630	3050
551.60	2645	2235	2640	2220	2615	2215	2630
5057.00	2180	1805	2180	1770	2140	1770	2155
8904.00	2095	1715	2085	1685	2050	1690	2075
corr. coef.	0.999	1.000	0.999	1.000	0.999	1.000	1.000
mV/decode	-459	-460	-462	-471	-464	-465	-461
mV at 1 hour	3901	3515	3906	3527	3881	3504	3889
hours to .1V	1.90E08	2.63E07	1.75E08	1.90E07	1.39E08	2.12E07	1.67E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
7.66	3105	3440	3145	3485	3165	3500	3155
75.00	2655	2986	2690	3070	2700	3085	2685
551.60	2220	2600	2255	2640	2270	2660	2265
5057.00	1780	2120	1810	2170	1820	2180	1815
8904.00	1700	2035	1730	2080	1745	2085	1735
corr. coef.	1.000	1.000	1.000	0.999	1.000	0.999	1.000
mV/decode	-465	-463	-468	-466	-470	-469	-468
mV at 1 hour	3515	3853	3557	3916	3575	3937	3562
hours to .1V	2.22E07	1.29E08	2.44E07	1.52E08	2.52E07	1.50E08	2.50E07

**Table 4-11. Retention Characteristic for 14 Cells From Part 6020 Serial 271
(Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)**

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	2900	2855	2970	2830	2970	2830	2950
212.50	2268	2280	2410	2170	2310	2268	2385
428.50	2050	2105	2240	1970	2125	2075	2215
4947.00	1440	1580	1710	1360	1520	1535	1680
8781.00	1335	1480	1600	1260	1410	1430	1570
corr. coef. mV/decade mV at 1 hour hours to .1V	0.999 -596 3655 9.22E05	0.999 -520 3505 3.53E06	1.000 -518 3626 6.41E06	0.999 -596 3575 6.74E05	0.999 -590 3707 1.29E06	0.999 -531 3505 2.55E06	1.000 -522 3610 5.33E06
READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
19.92	2850	2905	2880	2975	2770	2915	2765
212.50	2185	2250	2300	2415	2110	2245	2211
428.50	1975	2045	2125	2235	1910	2065	2015
4947.00	1355	1435	1590	1685	1290	1460	1495
8781.00	1265	1330	1490	1580	1195	1355	1395
corr. coef. mV/decade mV at 1 hour hours to .1V	0.999 -604 3605 6.35E05	0.999 -598 3655 8.81E05	0.999 -526 3539 3.44E06	1.000 -530 3651 5.02E06	0.999 -599 3521 5.09E05	0.999 -590 3648 1.03E06	0.999 -520 3421 2.44E06

Table 4-12. Retention Characteristic for 14 Cells From Part 6020 Serial 275
(Retention Test Started 3 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	2805	2820	2855	2830	2875	2865	2880
75.00	2250	2095	2315	2305	2330	2325	2335
551.60	1750	1810	1790	1820	1805	1840	1810
5057.00	1230	1325	1270	1335	1285	1355	1285
8904.00	1140	1245	1185	1255	1200	1270	1195
corr. coef.	1.000	0.991	0.999	0.999	0.999	0.999	0.999
mV/decode	-549	-497	-554	-521	-555	-526	-558
mV at 1 hour	3280	3167	3340	3278	3359	3314	3369
hours to .1V	6.17E05	1.47E06	7.10E05	1.28E06	7.45E05	1.30E06	7.23E05

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
7.66	2715	2865	2840	2860	2835	2855	2735
75.00	2165	2320	2310	2310	2305	2310	2175
551.60	1660	1790	1815	1785	1810	1780	1675
5057.00	1160	1260	1310	1260	1320	1255	1175
8904.00	1065	1175	1215	1175	1240	1180	1080
corr. coef.	0.999	0.999	1.000	0.999	0.999	0.999	0.999
mV/decode	-543	-561	-536	-558	-528	-557	-544
mV at 1 hour	3183	3357	3308	3347	3290	3341	3200
hours to .1V	4.71E05	6.45E05	9.66E05	6.55E05	1.11E06	6.62E05	4.97E05

Table 4-13. Retention Characteristic for 14 Cells From Part 6020 Serial 278
(Retention Test Started 11 May 1978 After 1E8 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
2.00	3505	3480	3375	3345	3530	3475	3395
24.40	2635	2600	2435	2405	2655	2590	2460
360.80	1810	1775	1595	1565	1830	1750	1620
4875.00	1280	1155	1000	980	1215	1130	1025
8713.00	1005	1030	910	880	1150	1055	975
corr. coef.	0.996	0.997	0.994	0.994	0.995	0.995	0.993
mV/decade	-663	-668	-672	-671	-655	-665	-664
mV at 1 hour	3621	3593	3459	3428	3632	3580	3473
hours to .1V	2.05E05	1.71E05	9.95E04	9.15E04	2.46E05	1.70E05	1.19E05

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14
2.00	3350	3485	3445	3410	3415	3505	3445
24.40	2410	2590	2540	2475	2470	2600	2545
360.80	1570	1760	1710	1650	1635	1770	1715
4875.00	995	1150	1100	1060	1050	1165	1100
8713.00	805	1080	1025	970	1000	1085	1045
corr. coef.	0.995	0.995	0.995	0.994	0.992	0.995	0.994
mV/decade	-683	-660	-663	-665	-662	-663	-660
mV at 1 hour	3447	3581	3539	3491	3486	3599	3538
hours to .1V	8.01E04	1.87E05	1.53E05	1.27E05	1.30E05	1.90E05	1.61E05

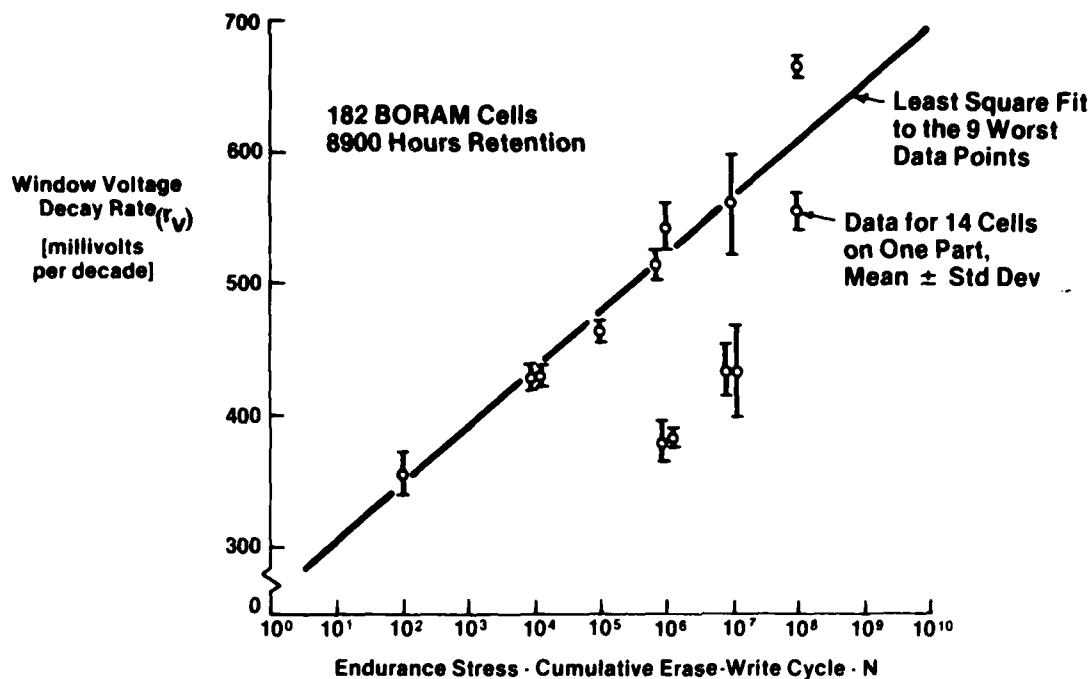


Figure 4-4. Window Decay Rate as a Function of Endurance Stress

79 0467 BR 1

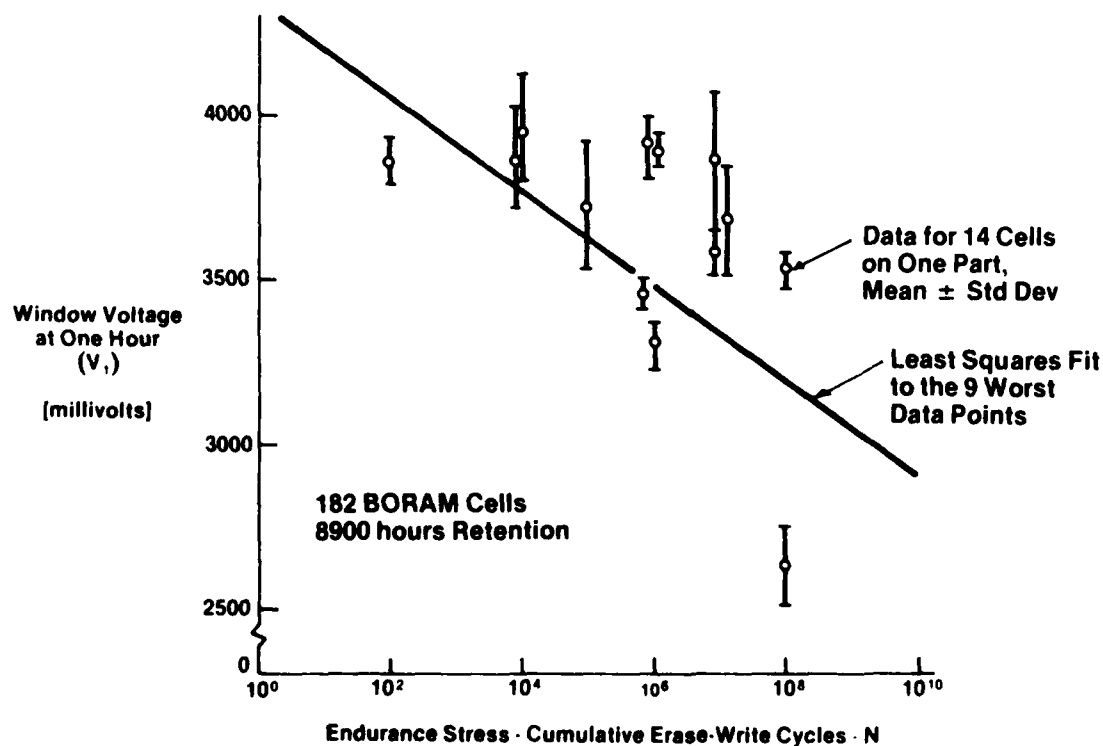
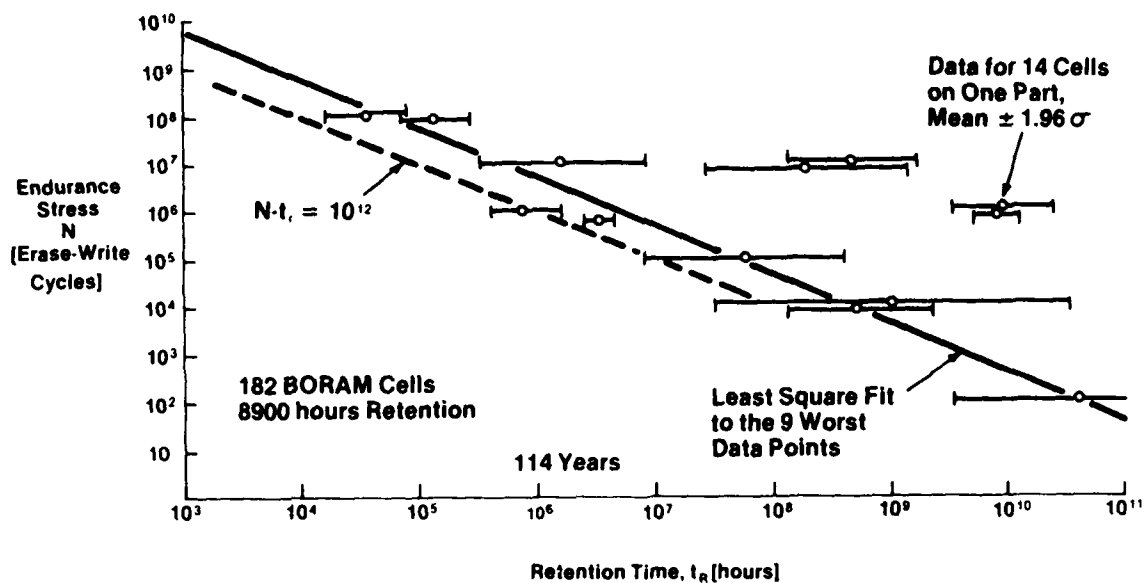


Figure 4-5. Window Voltage at 1 Hour as a Function of Endurance Stress

79 0467 BR 2



79 0467 BB

Figure 4-6. Endurance Retention Characteristic

4.3 WAFER PROBE TEST

This discussion outlines the technical approach to wafer probe test of the MNOS BORAM 6002 integrated circuit. The probe test was implemented on the Macrodata 501 automatic test system. The test program for the Macrodata system has been designated program "C1".

4.3.1 Overview

The wafer probe test consists of a sequence of 55 tests which have been divided into six categories. The categories are:

1. Substrate diode tests
2. Functional screen
3. Static parameter tests
4. Retention screen
5. Test structure measurements
6. Pulse response screen

Category No. 5 tests do not reject material, but merely record data for information purposes. All other tests involve accept-reject decisions. When the status of a given die has been determined it is assigned to a "BIN" by the test equipment. BIN number assignments are as follows.

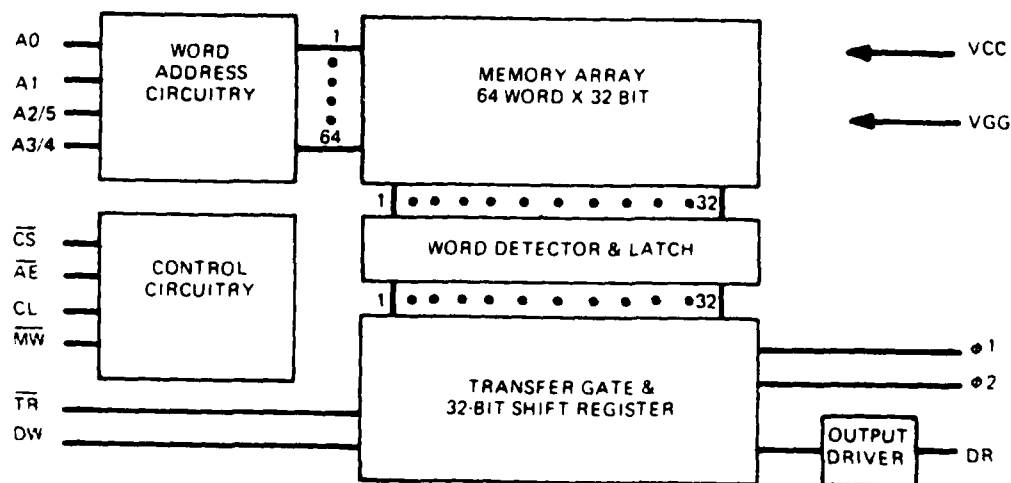
Test Number(s)	Criteria	BIN
1-1 to 1-16	Fail	10
2-1 to 2-3	Fail	9

2-4 to 2-6	Fail	8
3-1 to 3-12	Fail	7
3-13 to 3-14	Fail	6
3-15 to 3-20	Fail	5
4-1	Fail	4
6-1 to 6-4	Fail	3
6-5 to 6-6	Fail	2
6-7	Fail	1
All tests	Pass	0

Tests are performed in order by category and number within category. Testing is terminated at the first failure. For a part to qualify for use it must pass all tests and be classified as a "BIN 0" part.

The text below documents the circuit conditions for each test. Individual test categories are treated separately.

As shown in figure 4-7, the BORAM 6002 contains a fully decoded 64-word by 32-bit RAM and a 32-bit dynamic two-phase shift register. All I/O are accomplished serially through the shift register. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32-bit latch. The RAM and shift register can operate independently. Data stored in the latch may be written into the RAM while new data is shifted into the register.



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Figure 4-7. BORAM 6002 Functional Block Diagram

4.3.2 Test Categories

4.3.2.1 Test Category No. 1: Substrate Diode Tests

Every input terminal to the BORAM chip has an associated substrate diode. Under normal operating conditions where VCC is maintained as the most positive chip voltage, this diode is reverse biased. A similar situation exists for the on-chip test structures except the reference node is SUB rather than VCC, and the GT terminal is isolated (i.e., does not have an associated substrate diode).

The forward voltage drop of the substrate diodes is tested primarily to provide positive evidence of good probe contact to the wafer. In rare cases, however, this test can be an indication of process problems such as inadequate etching, poor ohmic contact, or improper diffusions.

Table 4-14 and associated footnotes define the 16 substrate diode tests.

4.3.2.2 Test Category No. 2: Functional Screen

The purpose of test category No. 2 is to eliminate nonfunctional die from further consideration before significant test time has been invested. A sequence of six functional tests are performed at nominal device operating speeds. The shift register is exercised first, then the memory is checked. The first memory test writes unique data into every row address. If this data can be read back correctly, the possibility of a fault in the chip address circuitry has been eliminated. Checkerboard and checkerboard bar tests then verify that every cell can store both ones and zeros.

Table 4-15 provides a summary outline of the category No. 2 tests. Test details are provided by the figures and tables referenced in table 4-15.

Table 4-14. Substrate Diode Tests

Test Number	Device Terminal Conditions ³																		
	VCC	TR	VGG	CS	A2 5	A3 4	A0	A1	AE	MW	CL	DR	DW	2	1	SUB	MD	FD	GT ²
1 1	GND	1																	
1 2	GND						1												
1 3	GND																		
1 4	GND											1							
1 5	GND								1										
1 6	GND			1															
1 7	GND														1				
1 8	GND													1					
1 9	GND																		
1 10	GND					1													
1 11	GND								1										
1 12	GND									1									
1 13	GND															1			
1 14	GND												1						
1 15																GND	1		
1 16																GND		1	

Notes

1. This is the node under test. Force 0.2 milliamperes into the node and measure the resulting voltage from the node to ground. Accept voltage readings from +0.3 volts up to 1.0 volts.
2. The GT terminal does not have an associated substrate diode.
3. Terminals not labeled are open circuited.

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Table 4-15. Summary and Description of Test Category No. 2: Functional Screen

Test Number	General Description of Test	Referenced Figures	Referenced Tables
2-1	SHIFT REGISTER TEST 1 MHz data rate zero data pattern	4-8, 4-9, 4-10	4-16
2-2	SHIFT REGISTER TEST 1 MHz data rate one data pattern	4-8, 4-9, 4-10	4-16
2-3	SHIFT REGISTER TEST 1 MHz data rate zero-one data pattern	4-8, 4-9, 4-10	4-16
2-4	ADDRESS & MEMORY TEST 1000 μ sec erase, 200 μ sec write diagonal data pattern	4-8, 4-10, 4-11	4-16, 4-17
2-5	MEMORY TEST 1000 μ sec erase, 200 μ sec write checkerboard data pattern	4-8, 4-10, 4-11	4-16, 4-18 4-19
2-6	MEMORY TEST 1000 μ sec erase, 200 μ sec write complementary checkerboard data pattern	4-8, 4-10, 4-11	4-16, 4-18, 4-19

7d 02b8 1A 0-2

4.3.2.3 Test Category No. 3: Static Parameter Tests

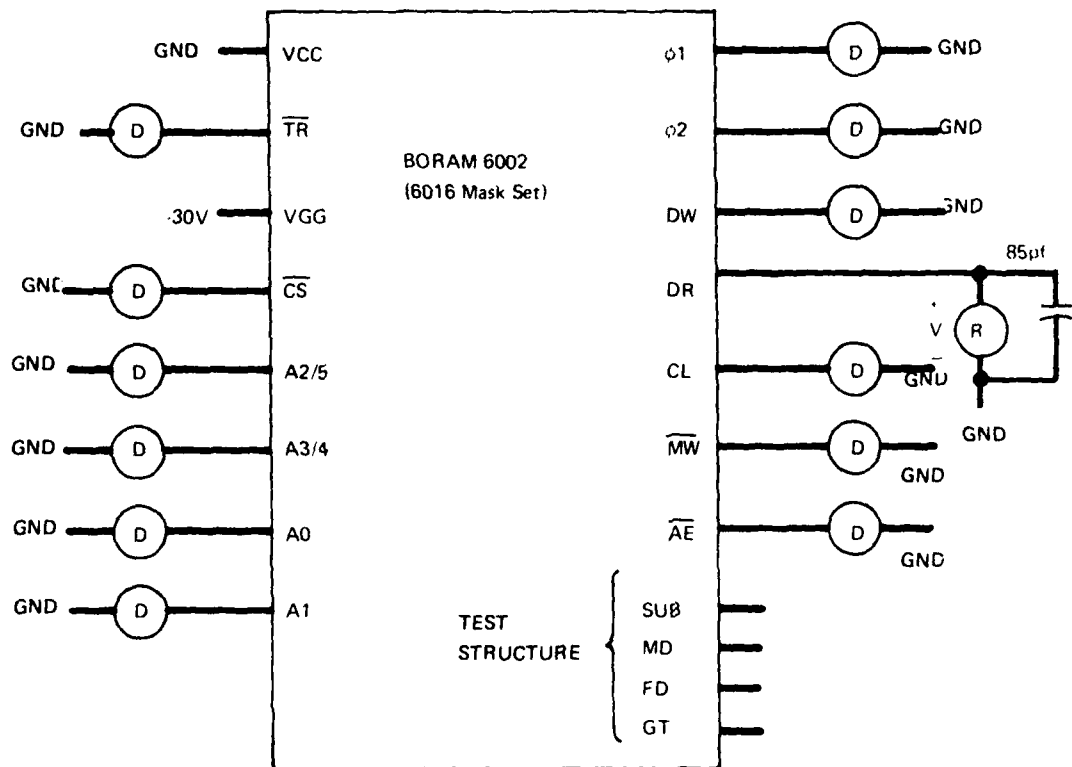
The category No. 3 test exhaustively examines the device under test for leakage current levels, signal threshold values, output drive capability, and supply current demand. Table 4-20 defines the test conditions.

Tests 3-13 and 3-14 are somewhat unusual in that several conventional device parameters are verified simultaneously.

In test 3-13, the input data line DW is held at the maximum low voltage level of -10.25 volts while both shift register clock phases are held at maximum low voltage values of -14.0 volts. Under this condition the input zero should propagate through the shift register and appear at the data output line DR. While the output stage is being driven by this worst case zero, a current of 5 milliamperes is forced into DR and the resulting voltage from DR to ground is measured. Therefore, test 3-13 verifies the parameters VIL, VOL and the output current sink capability.

Similar comments apply for test 3-14. Here the parameters verified are VIH (DW signal), VIL ($\phi 1$ and $\phi 2$), VOH and the output current source capability.

Tests 3-15 to 3-20 measure the supply current drain under static conditions. It should be noted that operating power dissipation in a memory system depends on the control waveform timing. Power calculations must consider the duty cycles involved.



- Notes:
1. "D" indicates driver. A driver is a programmed pulse generator.
 2. "R" indicates receiver. For category 2 tests the receiver measures the output voltage.
 3. The test socket is to present a total capacitive load to the device under test of 85pf.

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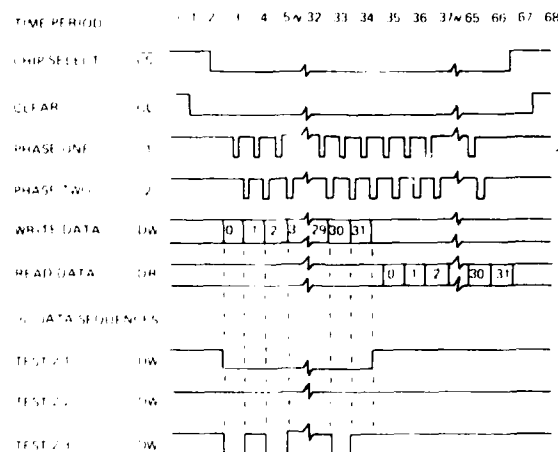
Figure 4-8. Signal Assignment for Category No. 2 Tests

Table 4-16. Driver Amplitudes for Category No. 2 Tests

Signal Symbol	Most Positive Amplitude Volts	Most Negative Amplitude Volts
$\overline{TR}$	VCC - 2.0	VCC - 10.5
$\overline{CS}$	VCC - 2.0	VCC - 34.65
A2/5	VCC - 2.0	VCC - 10.5
A3/4	VCC - 2.0	VCC - 10.5
A0	VCC - 2.0	VCC - 10.5
A1	VCC - 2.0	VCC - 10.5
ϕ_1	VCC - 2.0	VCC - 14.25
ϕ_2	VCC - 2.0	VCC - 14.25
DW	VCC - 2.0	VCC - 10.5
CL	VCC - 2.0	VCC - 14.25
$\overline{MW}$	VCC - 2.0	VCC - 10.5
$\overline{AE}$	VCC - 2.0	VCC - 10.5

78 0286 T 4

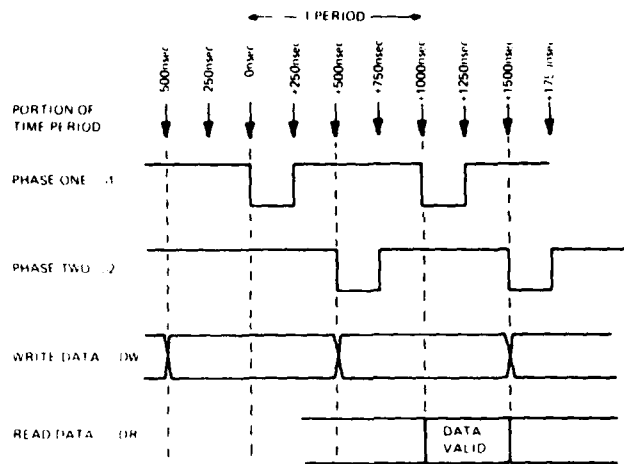
WAVEFORM SEQUENCE



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78 0286 V A 5

Figure 4-9. Operating Sequence for Shift Register Tests



- Notes:
1. Pulse amplitudes per table 2
 2. Rise and fall times (10% to 90%) ≤ 50 nsec
 3. DW may change at times other than shown above provided it is valid during phase one

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Figure 4-10. Detailed Timing for Clocks and Data

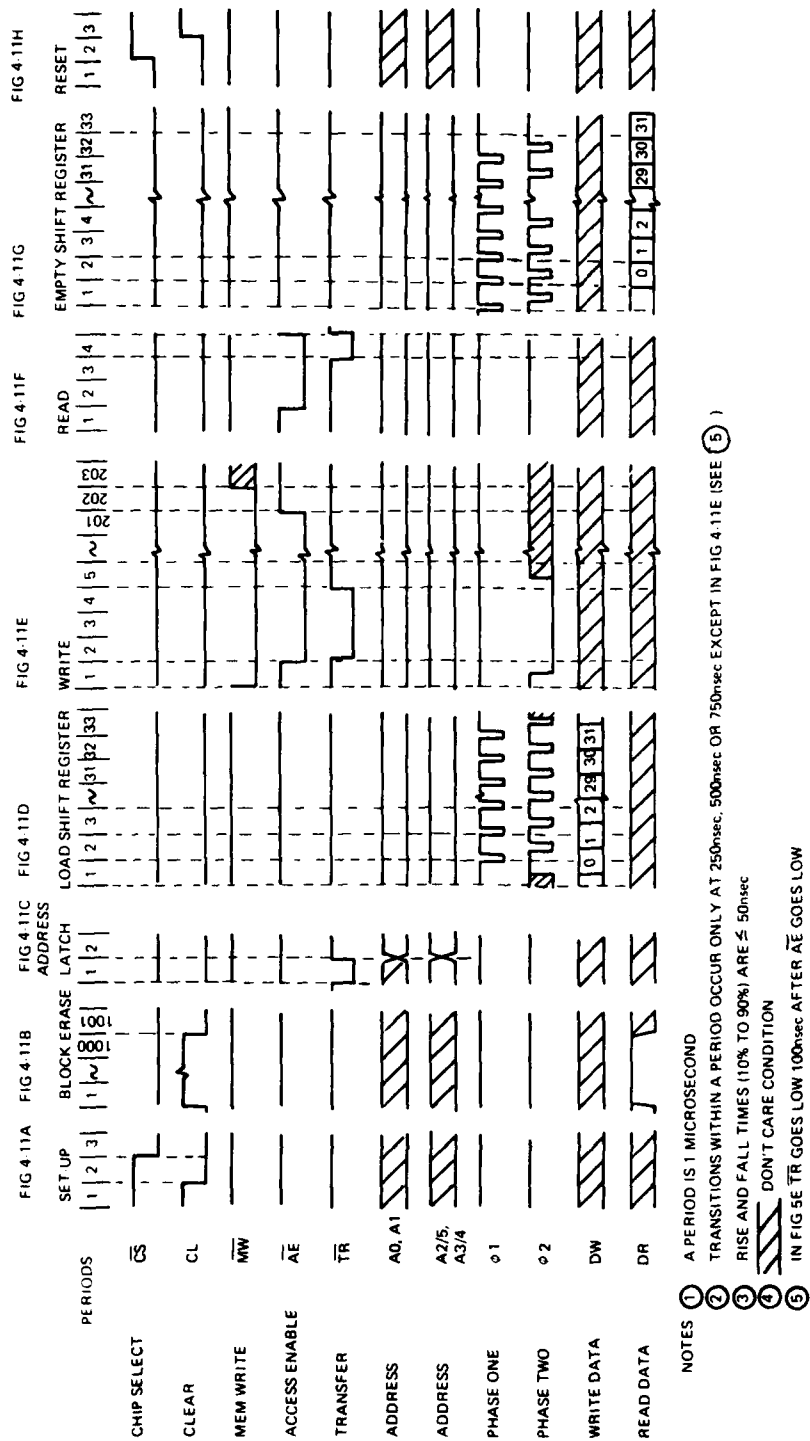
Table 4-17. Address and Memory Test Logical Flow Sequence

Step	Logical Operation
1	Setup CL and CS per Fig. 4-11 a
2	Block Erase per Fig. 4-11b
3	Address = 0
4	Setup Address Lines per Fig. 4-11c
5	Data = Function (Address) per Note Below
6	Load Shift Register per Fig. 4-11d
7	Write Data per Fig. 4-11e
8	Address = Address + 1
9	If (Address $\leq$ 64) then 4
10	Address = 0
11	Setup Address Lines per Fig. 4-11c
12	Read Data to Latch per Fig. 4-11f
13	Empty Shift Register per Fig. 4-11g
14	If (Data $\neq$ Function (Address)) then BIN and 18
15	Address = Address + 1
16	If (Address $\leq$ 64) then 11
17	Reset CS and CL per Fig. 4-11h
18	End Routine

Note: Diagonal Data Pattern per Figure below

Rows	Columns					
	0	1	...	30	31	
0	0	0	0	0	0	1
1	0	0	0	0	1	0
...	0	0	0	1	0	0
30	0	0	1	0	0	0
31	1	0	0	0	0	0
32	1	1	1	1	1	0
33	1	1	1	1	0	1
...	1	1	1	0	1	1
62	1	0	1	1	1	1
63	0	1	1	1	1	1

78-0286 TA 7 1



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Figure 4-11. Operating Sequences for Memory Tests

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Table 4-18. Memory Test Logical Flow Sequence

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 4-11a
2	Block Erase per Fig.4-11b
3	Address = 0
4	Setup Address Lines per Fig. 4-11c
5	Data = (per Table 4-19)
6	Load Shift Register per Fig. 4-11d
7	Write Data per Fig. 4-11e
8	Address = Address + 1
9	If (Address < 64) then 4
10	Address = 0
11	Setup Address Lines per Fig. 4-11c
12	Read Data to Latch per Fig. 4-11f
13	Empty Shift Register per Fig.4-11g
14	If (Data $\neq$ (per Table 4-19)) then BIN and 18
15	Address = Address + 1
16	If (Address < 64) then 11
17	Reset $\overline{CS}$ and CL per Fig. 4-11h
18	End Routine

78-0286-TA-9 -1

Table 4-19. Memory Test Data Patterns

Test Number	Row Address	Data Pattern Required In Shift Register																																	
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
2-5	Even	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
2-5	Odd	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2-6	Even	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2-6	Odd	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

78-0286 TA 10

Table 4-20. Static Parameter Tests

Test Name	Test Description	Device Terminal Conditions 6														Terminal Under Test	25°C Test Limits		
		VCC	TR	VGG	CS	A2 5	A3 4	A0	A1	AE	MW	CL	DR	DW	2		Min	Max	Units
3-1	Input Leakage	1			-37.5V											CS		20	μA
3-2	Input Leakage	+20V	2	10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		+20V	+20V	TR		10	μA
3-3	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	2	+20V	+20V	+20V	+5V		+20V	+20V	A0		10	μA
3-4	Input Leakage	+20V	+20V	10V	+20V	+20V	2	+20V	+20V	+20V	+20V	+5V		+20V	+20V	A3 4		10	μA
3-5	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	2	+20V	+20V	+20V	+5V		+20V	+20V	A1		10	μA
3-6	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		+20V	2	A2		10	μA
3-7	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		2	+20V	DW		10	μA
3-8	Input Leakage	+20V	+20V	10V	+20V	2	+20V	+20V	+20V	+20V	+20V	+5V		+20V	+20V	A2 5		10	μA
3-9	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	2	+20V	+20V	+5V		+20V	+20V	AE		10	μA
3-10	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	+20V	2	+5V			+20V	+20V	MW		10	μA
3-11	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	+20V	+20V	+5V			+20V	2	CL		10	μA
3-12	Input Leakage	+20V	+20V	10V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		2	+20V	+20V	DR		10	μA
3-13	Input & Output Low Voltage Test	GND	GND	30V	35V	GND	GND	GND	GND	GND	GND	15V	3	10.25V	14V	14V	DR	10.5	Volts
3-14	Input & Output High Voltage Test	GND	GND	30V	35V	GND	GND	GND	GND	GND	GND	15V	4	1.75V-14V	14V	14V	DR	45	Volts
3-15	Supply Current Disconnected Standby	5	GND	30V	GND	GND	GND	GND	GND	GND	GND	15V		GND	GND	GND	VCC	100.0	μA
3-16	Supply Current Selected Standby	5	GND	33V	33V	GND	GND	GND	GND	GND	GND	15V		GND	GND	GND	VCC	7.0	15.0 mA
3-17	Supply Current Read	5	GND	33V	33V	GND	GND	GND	GND	GND	GND	15V		GND	GND	GND	VCC	11.0	37.0 mA
3-18	Supply Current Write	5	GND	33V	33V	GND	GND	GND	GND	GND	15V	15V		GND	GND	GND	VCC	10.0	32.0 mA
3-19	Supply Current Chip Clear	5	GND	33V	33V	GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	VCC	7.0	15.0 mA
3-20	Supply Current Group Clear	5	GND	33V	33V	GND	GND	GND	GND	GND	15V	15V	GND		GND	GND	VCC	8.0	18.0 mA

1. Measure the current flow from GND into VCC.
2. Measure the current flow out of this node to GND.
3. Measure the voltage from DR and measure the voltage from DR to GND.
4. Measure the voltage from DR and measure the voltage from DR to GND.
5. Measure the current flow from GND into VCC.
6. Measure the current flow from GND into VCC.

78-0281-1A 11-1

4.3.2.4 Test Category No. 4: Retention Screen

Test category No. 4 was established to isolate chips which are likely to have poor nonvolatile data retention characteristics. The test simulates end-of-retention conditions by writing the memory cells using a reduced voltage (table 4-21).

Note that erase and read are performed at nominal supply voltages and nominal control signal timing. This avoids confusion of circuit operating limitations with possible retention defects.

4.3.2.5 Test Category No. 5: Test Structure Measurements

The BORAM 6002 die contains some device structures which are not part of the functional memory configuration defined in figure 4-7. These structures were provided to allow measurement of fundamental process characteristics, and include several capacitors and transistors.

Probe test is a convenient point to gather statistically significant amounts of data without incurring excessive cost. These test structures are not normally available for measurements after device packaging.

Table 4-23 and figure 4-12 document the category No. 5 tests. Nonmemory threshold and memory transistor thresholds are monitored. The magnitude of voltage present on the N type epitaxial memory substrate for two circuit operating conditions is also measured.

Table 4-21. Summary and Description of Test Category No. 4: Retention Screen

Test Number	General Description of Test	Referenced Figures	Referenced Tables
4-1	RETENTION SCREEN 1000μsec erase, 200μsec write zero and one data patterns 1. VGG = -30V erase chip 2. VGG = -27V write zero 3. VGG = -30V read zero 4. VGG = -30V erase chip 5. VGG = -27V write one 6. VGG = -30V read one Both the zero and one patterns must be verified to pass the test.	4-8, 4-10, 4-11	4-16, 4-22

78-0286-TA-12.1

Table 4-22. Retention Screen Logical Flow Sequence

Step	Logical Operation
1	K=0
2	Set up CL and $\overline{CS}$ per Fig. 4-11a
3	Set VGG = -30 Volts
4	Block Erase per Fig. 4-11b
5	Data = K
6	Set VGG = -27 Volts
7	Address = 0
8	Set up Address Lines per Fig. 4-11c
9	Load Shift Register per Fig. 4-11d
10	Write Data per Fig. 4-11e
11	Address = Address + 1
12	If (Address $\leq$ 64) then 8
13	Set VGG = -30 Volts
14	Address = 0
15	Set up Address Lines per Fig. 4-11d
16	Read Data to Latch per Fig. 4-11f
17	Empty Shift Register per Fig. 4-11g
18	If (Data $\neq$ K) then BIN and 24
19	Address = Address + 1
20	If (Address $\leq$ 64) then 15
21	K = $\overline{K}$
22	If (K = 1) then 4
23	Reset $\overline{CS}$ and CL per Fig. 4-11h
24	End Routine

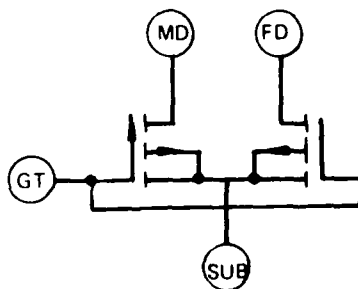
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Table 4-23. Test Structure Measurements

Test Item	Description	Phase of Test	Device Terminal Conditions																
			VCC	TR	VGG	CS	A2	A3	A4	A0	A1	AE	MW	CL	DR	DW	22	GT	SUB
1	Memory threshold voltage	measurement																	GND
2	Memory high conduction threshold voltage	set up																	GND
3	Memory low conduction threshold voltage	measurement																	GND
4	Memory low conduction threshold voltage	set up																	GND
5	Substrate voltage high	measurement	GND	GND	30V	35V	GND	GND	GND	GND	15V	GND	15V	GND	GND	GND	GND	GND	GND
6	Substrate voltage low	measurement	GND	GND	30V	35V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

1. Tie the feedback (FD) and gate (GT) terminals together. Force 10 megohms out of the node and measure the voltage from the node to ground (GND).
2. Force GT to +25 volts for 1 millisecond.
3. Tie the memory diode (MD) and gate (GT) terminals together. Force 10 megohms out of the node and measure the voltage from the node to ground (GND).
4. Force GT to 25 volts for 200 microseconds.
5. Measure the voltage from SUB to (GND).

78-0286-VA-14



78-0286-VA-15

Figure 4-12. Transistor Test Structure Circuit Diagram

4.3.2.6 Test Category No. 6: Pulse Response Screen

Category No. 6 tests are a continuation of the functional screen begun in category No. 2. A device which has survived up to category No. 6 has been proven to have in-specification static parameters, to be functional under nominal operating conditions, and to have a reasonable retention window. The purpose of the pulse response screen is to exhaustively examine the part to ensure that it can perform in all operating modes without a detracting dependence on past data history (table 4-24).

Table 4-24. Summary and Description of Test Category No. 6: Pulse Response Screen

Test Number	General Description of Test	Referenced Figures	Referenced Tables
6.1	ERASE RECOVERY TEST 1000 μ sec erase, 200 μ sec write zero data pattern erase-write 100 times one data pattern erase-write 1 time, read	4-8, 4-10, 4-11	4-16, 4-25
6.2	ERASE RECOVERY TEST 1000 μ sec erase, 200 μ sec write one data pattern erase-write 100 times zero data pattern erase-write 1 time, read	4-8, 4-10, 4-11	4-16, 4-25
6.3	ERASE RECOVERY TEST 1000 μ sec erase, 200 μ sec write checkerboard pattern erase-write 100 times complement checkerboard pattern erase-write 1 time, read	4-8, 4-10, 4-11	4-16, 4-25
6.4	ERASE RECOVERY TEST 1000 μ sec erase, 200 μ sec write complement checkerboard pattern erase-write 100 times checkerboard pattern erase-write 1 time, read	4-8, 4-10, 4-11	4-16, 4-25
6.5	GROUP OPERATION TEST 1000 μ sec erase, 200 μ sec write complement checkerboard pattern begin at address 63 and count down group erase-write entire chip read entire chip	4-8, 4-10, 4-11, 4-13	4-16, 4-26
6.6	GROUP OPERATION TEST 1000 μ sec erase, 200 μ sec write checkerboard pattern begin at address 0 and count up group erase-write entire chip read entire chip	4-8, 4-10, 4-11, 4-13	4-16, 4-26
6.7	READ DISTURB TEST use data written during test 6.6 read data to latch 1000 times read entire chip	4-8, 4-10, 4-11	4-16, 4-27

P 0268 TA-16-2

Table 4-25. Erase Recovery Test Logical Flow Sequence

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 4-11a
2	J = 1
3	Block Erase per Fig. 4-11b
4	Address = 0
5	Setup Address Lines per Fig. 4-11c
6	Data = (per Note at Bottom of Page)
7	Load Shift Register per Fig. 4-11d
8	Write Data per Fig. 4-11e
9	Address = Address + 1
10	If (Address < 64) then 5
11	J = J + 1
12	If (J < 101) then 3
13	Block Erase per Fig. 4-11b
14	Address = 0
15	Setup Address Lines per Fig. 4-11c
16	Data = (Complement of Data used in Step 6)
17	Load Shift Register per Fig. 4-11d
18	Write Data per Fig. 4-11e
19	Address = Address + 1
20	If (Address < 64) then 15
21	Address = 0
22	Setup Address Lines per Fig. 4-11c
23	Read Data to Latch per Fig. 4-11f
24	Empty Shift Register per Fig. 4-11g
25	If (Data $\neq$ (Complement of Data used in Step 6)) then BIN and 29
26	Address = Address + 1
27	If (Address < 64) then 22
28	Reset $\overline{CS}$ and CL per Fig. 4-11h
29	End Routine

Note:

Test Number	Data Pattern to be Used in Step 6
6-1	All Zero
6-2	All One
6-3	Checkerboard (Defined in Table 4-19 for Test Number 2-5)
6-4	Complement Checkerboard

78-0286 TA 1 / 2

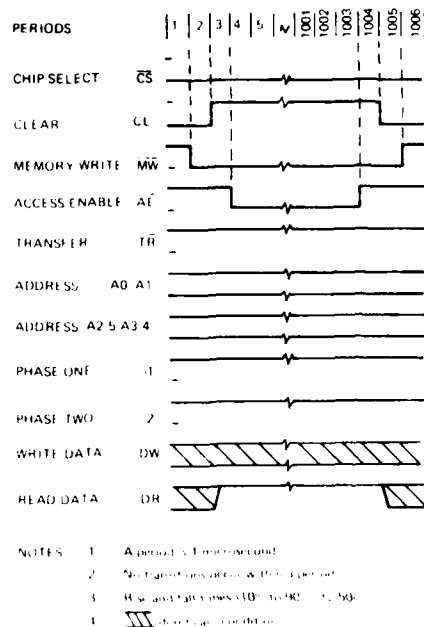
Table 4-26. Group Operations Test Logical Flow Diagram

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 4-11a
2	Address = (63 for Test 6-5) (0 for Test 6-6)
3	Setup Address Lines per Fig. 4-11c
4	Group Erase per Fig. 4-13
5	Data (per Note at Bottom of Page)
6	Load Shift Register per Fig. 4-11d
7	Write Data per Fig. 4-11e
8	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
9	Load Shift Register per Fig. 4-11d
10	Write Data per Fig. 4-11e
11	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
12	Load Shift Register per Fig. 4-11d
13	Write Data per Fig. 4-11e
14	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
15	Load Shift Register per Fig. 4-11d
16	Write Data per Fig. 4-11e
17	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
18	(If Address $\neq$ -1 then 3 for Test 6-5) (If Address $\neq$ 64 then 3 for Test 6-6)
19	Address = 0
20	Setup Address Lines per Fig. 4-11c
21	Read Data to Latch per Fig. 4-11f
22	Empty Shift Register per Fig. 4-11g
23	If Data $\neq$ (per Note at Bottom of Page) then BIN and 26
24	Address = Address + 1
25	If Address $\neq$ 64 then 20
26	Reset $\overline{CS}$ and CL per Fig. 4-11h
27	End Routine

Note

Test Number	Data Pattern
6-5	Complement Checkerboard
6-6	Checkerboard (Defined in Table 4-19 for Test Number 2-5)

78-0286-TA-18-2



78-0286-VA-19

Figure 4-13. Operating Sequence of Group Erase

Table 4-27. Read Disturb Test Logical Flow Sequence

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 4-11a
2	J = 1
3	Address = 0
4	Setup Address Lines per Fig. 4-11c
5	Read Data to Latch per Fig. 4-11f
6	Address = Address + 1
7	If (Address < 64) then 4
8	J = J + 1
9	If (J < 1001) then 3
10	Address = 0
11	Setup Address Lines per Fig. 4-11c
12	Read Data to Latch per Fig. 4-11f
13	Empty Shift Register per Fig. 4-11g
14	If (Data $\neq$ Checkerboard) then 15 and 18
15	Address = Address + 1
16	If (Address < 64) then 11
17	Reset $\overline{CS}$ and CL per Fig. 4-11h
18	End Routine

Note

Checkerboard Pattern Defined in Table 4-19 for Test Number 2-5

78-0286-TA-20-2

4.4 HYBRID CIRCUIT TEST

A functional test station was established to process the BORAM memory microcircuit. This test system provides both manufacturing and engineering oriented reports, and is capable of volume throughput in excess of the MM&T production rate requirement.

This discussion explains the requirements and objectives of the test station development effort, describes the hardware and software which has been developed, gives the functional test specification, and presents data to show that development objectives were achieved.

4.4.1 Statement of the Development Program

The functional test station must provide specific data in a timely manner in a convenient format. It must with a high confidence level isolate defective chips. In addition, it must comply with the MM&T contract throughput requirement. This discussion will present those detailed requirements.

a. Functional Test Station Purpose

The first electrical test of the BORAM hybrid after assembly occurs at work station A10. Station A10 is the "Hybrid Circuit Functional Test Station." It is located in the MNOS Test Laboratory at the Westinghouse Advanced Technology Laboratories facility.

At station A10 the hybrid circuits are unlidded, and chip replacement or wire bond replacement actions are feasible. This test station must handle the highest volume of hybrids for any given production quantity because all rework units return to this point.

The purpose of the functional test station is to certify that a given hybrid circuit is fully operational and is suitable for further processing, or in the event of a detected failure the purpose of the test station is to provide information to guide rework decisions.

b. Test Requirement

The functional test is a test of unfinished product performed for manufacturing decision making purposes. The test criteria are thus a function of the manufacturer's judgment as to how to determine that the product is functioning properly with a minimum expenditure of test time.

c. Report Requirements

The nature of the manufacturing decisions at station A10 dictates the report requirements. The needs of the technician who must perform a rework action must be met. The needs of an engineer or technician who must diagnose the probable cause of a detected failure must be met.

The rework action is best served by a simple hard copy report which clearly identifies the chip or chips which must be visually examined and possibly replaced. Preferably, this document should be small enough to travel with the normal hybrid circuit routing ticket documentation package. It would be helpful if the chips were identified in a manner consistent with the actual physical locations of the die on the ceramic substrate. This feature would tend to reduce human errors in device location.

Before a given hybrid is routed for rework action the test technician must define the nature of the problem involved. To support this effort a second more detailed test report is required. This document should show which tests passed or failed for each chip in the hybrid. The data summary should allow identification of the most probable cause of failure.

d. Throughput Requirement

The throughput requirement for station A10 is derived from the MM&T contract requirement for pilot line capacity. If the line is operated 5 days a week on a one-shift basis, the total volume capacity is required to be at least 1875 hybrids per month.

To examine individual station throughput requirements, it is convenient to express the rate specification in hybrids per hour. A nominal month by the above operating criteria contains 160 hours. Therefore, the line rate requirement is 11.7 hybrids per hour.

The functional test station must process every hybrid circuit at least two times. Each device is tested before and after cycle stress. In addition to these two tests per hybrid, any rework action implies two additional tests per hybrid.

An exact computation of the volume which must move through station A10 depends on the amount of rework, and is a complex calculation. A simplified worst case calculation can be made to set upper bounds on the necessary capacity. Arbitrarily assume a very poor rework experience. Say that every hybrid must be reworked one time, that 40 percent must be reworked twice, that 20 percent must be reworked three times, and that 5 percent must be reworked four times. The implied number of functional tests per delivered finished hybrid are:

2 tests (1 initial + 1 rework + 0.4 rework + 0.2 rework + 0.05 rework)

2 tests (2.65)

5.30 tests

Since the required rate of finished hybrids is 11.7 per hour, the upper bound capacity of station A10 to meet contract requirements is:

5.30×11.7 hybrids/hour

62 hybrids/hour

e. Additional Objectives

The primary concern is the rapid screening of the BORAM hybrid at operation 10 in the hybrid assembly and test flow. There are, however, test considerations of importance to BORAM production which are beyond the scope of operation 10, and yet should influence the design of the test system.

The production of BORAM systems involves memory testing at four levels of product complexity:

- a. Memory Chips
- b. Multichip Hybrids
- c. Memory Cards or Modules
- d. Memory Systems

These tests are very similar. It would be a major advantage if the test system designed for hybrid test could also conveniently perform the other three levels of test.

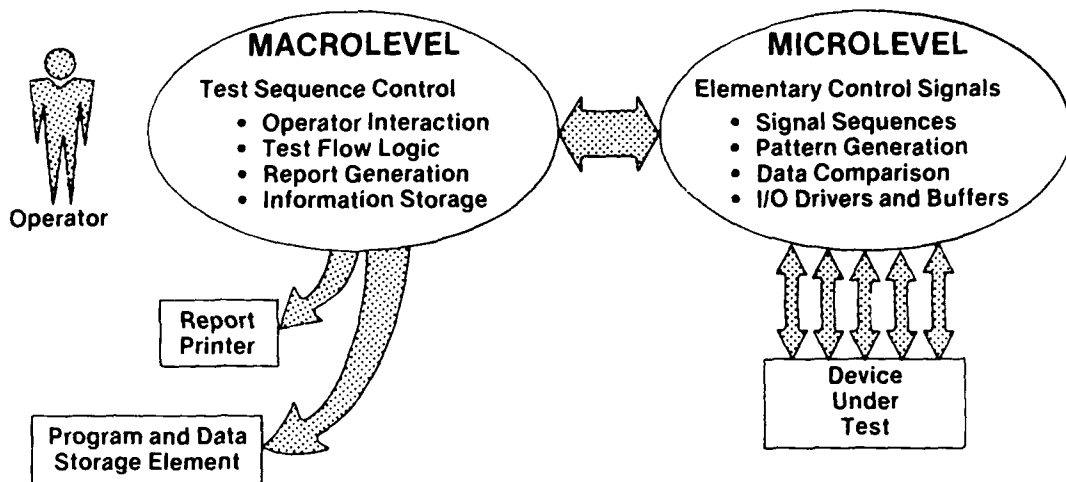
Finally the test system design must consider the practical aspects common to all equipment developments. Hardware cost and reliability must be reasonable. Software development and documentation must be easily accomplished without major labor expenditures.

4.4.2 Functional Test Station Description

The BORAM Functional Test Station is based on an architectural concept which contributes greatly to economy and ease of use. The system is suitable for application to all four levels of BORAM testing. This discussion explains the design concept, describes the hardware, reviews the hardware operation, examines the software functions, and briefly describes the microcode assembler used to support software development.

a. Macrolevel and Microlevel Partitioning

The fundamental architectural concept on which the design of the Functional Test Station is based is to partition the test problem into two parts: a "macrolevel" and a "microlevel." Figure 4-14 illustrates the points of concern for each level.



78 0220-VG-7

Figure 4-14. Test System Functional Block Diagram

The macrolevel is concerned with overall test objectives and the human oriented requirements. Macrolevel software acts as the executive controller for the test. Macrolevel hardware interacts directly with the user.

The microlevel is concerned with the execution of the detailed control sequences for accomplishing device operation. Microlevel software responds to macrolevel commands to accomplish a required function. Given the command "WRITE," the microcode might proceed to write a complex data pattern into an assembly of memory chips. Microlevel hardware interfaces to the macrolevel hardware and to the device under test. The microlevel hardware must provide the proper voltage levels, waveshapes and timing.

The advantage of this partitioning is that each set of problems becomes easier to treat. The flexibility of both the hardware and the software is greatly increased.

b. Elements of the Test Station

Figure 4-15 shows the hardware elements used to implement the Functional Test Station. The primary macrolevel component is an HP9825A calculator. This device is an inexpensive, yet very powerful general purpose computer.

HP9825A programs are written in a high level language with many of the features of BASIC. The calculator mainframe incorporates an alphanumeric keyboard, a magnetic tape cassette drive, a 32-character I.E.D display, and a paper tape printer. Extensive program editing and debugging features are built into the unit. The particular HP9825A used in the Functional Test Station is equipped with 23,228 bytes of main memory.

The I/O capability of the calculator is further supplemented by an HP9866B, Thermal Line Printer. This unit is used to prepare the test reports.



Figure 4-15. Elements of the BORAM Functional Test Station

Program and data storage are accomplished using the tape cartridge feature of the HP9825A mainframe. The tape capacity is more than adequate to store both macrolevel and microlevel programs as well as many utility routines.

The microlevel component in the system is the BORAM Functional Test Unit (FTU) shown in the foreground of figure 4-15. This device communicates with the HP9825A via a 16-bit channel. This is the cable at the left side of the unit. Two channels are provided to communicate with devices under test. In figure 4-15, the two cables at the right of the unit are shown connected to PC boards which can accommodate 30 integrated circuits for test. Figure 4-16 shows the BORAM hybrid circuit test fixtures. The availability of two channels allows the operator to be loading and processing the paper work for one group of eight hybrids while the other group is being tested. This provision eliminates time losses due to handling.

c. Hardware Operation

To conduct a test the operator inserts a tape cartridge containing the test program into the HP9825A. When the calculator is turned on the machine automatically loads the program into main memory and begins to run the program. The LED display informs the operator as to what processes are taking place, and gives prompts when operator action is required.

The operator is asked to enter such data as date of test, which test channel is to be used, the number of hybrids to be tested, and the serial numbers of each hybrid. The test program prepares the Functional Test Unit to conduct the microfunctions by communicating over the 16-bit channel.

The block diagram shown in figure 4-17 describes the internal structure of the BORAM Functional Test Unit. A microcontroller based on the Am2911 microsequencer chip forms the heart of the test unit.

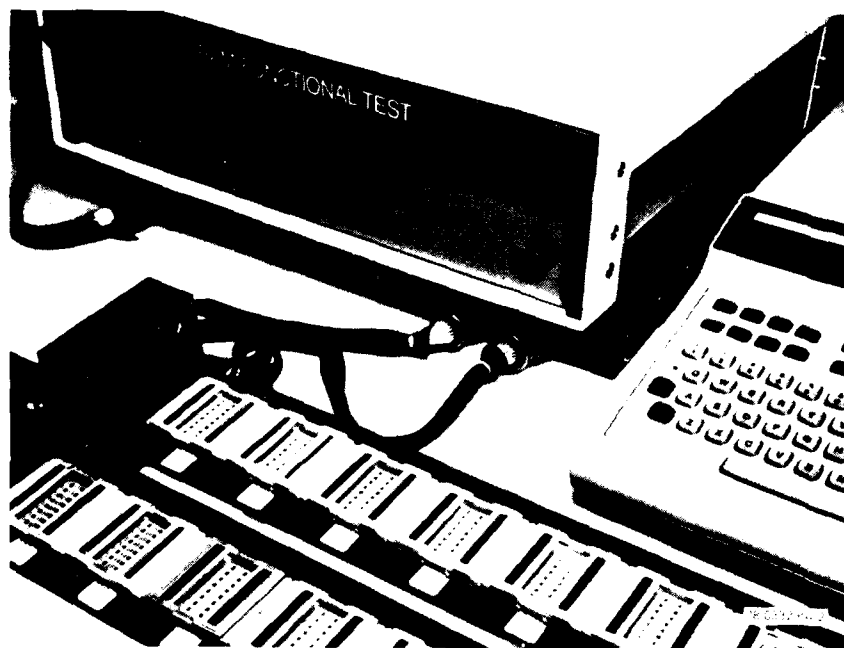
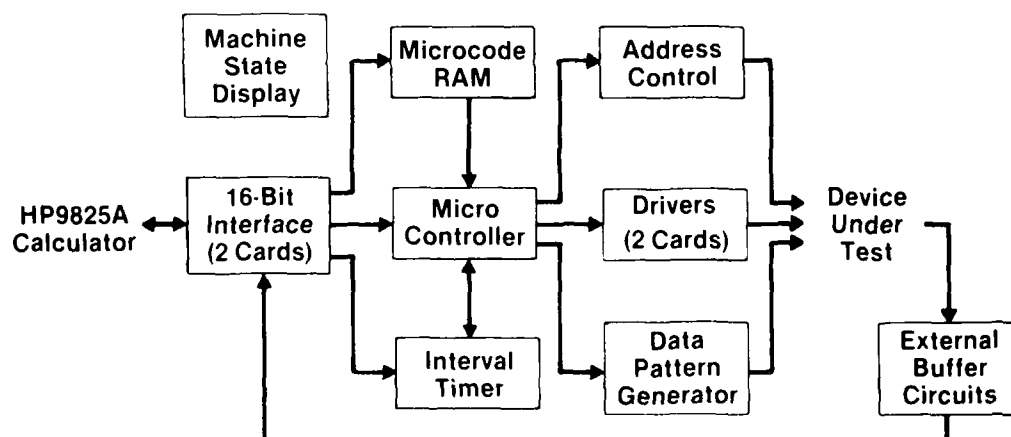


Figure 4-16. BORAM Hybrid Circuits in Functional Test Fixture



78 0220 V.6 6

Figure 4-17. BORAM Functional Test Unit

During the initialization phase of the test, the HP9825A reads the microcode program from the tape cartridge and sends it via the 16-bit bus to the Functional Test Unit. The microcode is stored in a RAM. This feature makes the unit particularly easy to use and to reconfigure. The option of microcode storage in ROM's or PROM's was also allowed for in the hardware design.

The interface to the device under test necessarily involves specific waveshapes and voltage levels. The output circuits on the driver cards, the address card and data pattern card accomplish this function.

Pulse timing and duration are set by the microcode routines or by command from the HP9825A. For example, the erase and write times for BORAM chips are set by calculator software.

Data patterns and data checking are selected by HP9825A software. The data pattern generator card in the Functional Test Unit provides the selected patterns.

One feature of some importance is not shown clearly in figure 4-17. The buffered data coming from the device under test is actually routed back to the data pattern generator card. On that card the 16 signals can be exclusive ORed with the source data pattern. Thus, the HP9825A can command that the Functional Test Unit return either the data pattern read from the device under test, or the error pattern resulting from the exclusive OR operation.

After initialization is complete the HP9825A LED display will indicate "READY FOR TEST." When the operator pushes the "CONTINUE" button, the test sequence for up to eight hybrid circuits will be automatically conducted. At the conclusion of the test, production oriented reports will be printed for each hybrid circuit. Then an engineering oriented report will be printed for all of the hybrids under test.

d. Software Considerations

For operation the Functional Test Station requires two sets of software programs. Figure 4-18 gives an overview of the programming task. The macrolevel program runs on the HP9825A. The microlevel program runs on the microcontroller in the Functional Test Unit.

The software development begins with a clear statement of test objectives. What is it that must be achieved? The macro planning activity extends these requirements into specific definitions of the test sequence and output reports. Then the desired tests are detailed in terms of tape file storage, main memory variable assignments, and operator interaction requirements. Finally the actual coding can be performed.

Figure 4-19 is a sample of the HP9825A coding used in the BORAM Hybrid Test Program. The HP9825A has a wide range of instruction types. For example, it provides string operations, matrix operations, binary operations, and all the usual features of BASIC. In addition, it offers a rich assortment of instructions to control and to interact with I/O devices.

The microcode development task begins with a careful definition of the interface to the device under test. What are the required signals, and how do they relate in time sequence to accomplish specific functions? What are the functions that the macrocode will request? How should the addressing sequence be arranged?

The microcoding task cannot really be separated from hardware design. The criteria for proper program operation is the actual observation of the waveforms at the terminals of the device under test.

Microcode development depends heavily on the use of the HP9825A. An assembler and various utility routines allow the engineer to interactively observe the effects at the device under test and modify this program until the desired results are achieved.

e. Microcode Assembler

The primary tool used for microcode development is an assembly program. The assembly language instruction set is presented in table 4-28. The mnemonics were established by Advanced Micro Devices, Inc. which manufactures the Am2911 microsequencer chip.

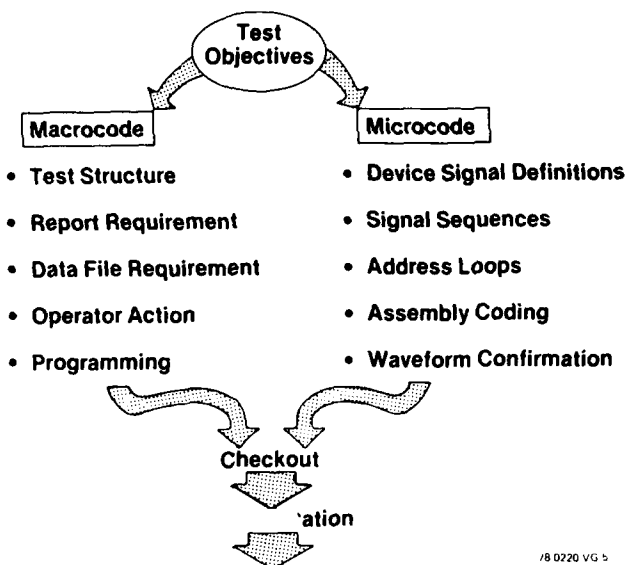


Figure 4-18. Software Development Considerations

The assembler allows the engineer to key in lines of code at the HP9825A keyboard. The code and any arguments are examined for consistency with validated symbols and instruction formats. If an error is detected, the assembler asks for re-entry of the line. When the code is accepted as valid it is written into a microcode memory map file on the tape cartridge.

At any time the engineer may examine lines of code on the LED display or he may request a hard copy memory map listing. Figure 4-20 is an example of such a listing. The address space ranges from 000 to 255. The map shows the assembly language instructions and arguments, and then gives the equivalent data as it will appear in the LED display (machine state display per figure 4-17) incorporated in the Functional Test Unit. These seven hexadecimal characters are convenient for confirming that the hardware has actually received the desired code.

4.4.3 Functional Test Station Performance

This discussion reviews the observed characteristics of the test station in such a manner that judgments can be made as to whether development objectives have been achieved.

a. Test Sequence

The microcircuit has two data inputs (DWA and DWB) and two data outputs (DRA and DRB). The "A" data lines are associated with the eight odd numbered chips. The "B" data lines are associated with the eight even numbered chips. Each chip select line controls one odd and one even numbered device. Data outputs are tristate. A deselected chip is powered down, and its DR output line is in a high impedance state. In the hybrid circuit only one odd and one even chip may be selected at any given time. The selected chip controls the output bus, and has both active source and sink capability.

```

201: "TEST SUBROUTINES":
202: "SP":eir 8,162:wtb 8,21:ret
203: "TS1":eir 8,162:wtb 8,21:ret
204: "TS2":wtb 8,0:wait 1
205: if rds(8)mod2=0:jmp 0
206: "TS4":wtb 8,0-8:eir 8,130
207: for I=0 to 7:-1-Y:if r 8,"XX",2040
208: if rds("XX")=-1:jmp 0
209: for J=1 to 2048:bandrdb("XX"),Y-Y:next J
210: band(Y-XCM,11,XCM,11)-XCM,11:next J
211: wrt 16,7,"TEST ",W:ret
212: "TS3":for I=0 to 7:wrt 16,9,I+1,XCM,11:ret I:next I
213: "#####":
214: prt "BORHM HYBRID","TEST PROGRAM":prt 8,"PAIR ",f1,0,"x",f8,0
215: "D1":prt "Test Channel A or B":A#
216: if pos(A#," ")=1:A#(2)-A#(3):jmp 0
217: 0-C:if "A"=A#(1,1):18-C
218: if "B"=A#(1,1):16-C
219: if C=0:prt "INVALID INPUT":eto "D1"
220: if rds(8)>299:dsr "TURN ON TEST SYSTEM":jmp 1
221: wait 10:dsr "NOW LOADING MICROCODE":eto 1:cc
222: for I=0 to 255:num(C#(I+1,1)-48+K:if I>154:K=-K+
223: wtc 8,1:wtb 8,161+K:0-L
224: for J=2 to 5:num(C#(I+1,J)-48+K:if I>154:K=-K+
225: 16L+K-L:next J:if L>32767:L-65536+L
226: wtc 8,3:wtb 8,L:next J
227: dsr "LOADING DATA RAM":but "XX"
228: for J=1 to 4:for I=1 to 128:wtb "XX",I:next I:next J:dsr "SP"
229: wtb 8,1024:wtb 8,4:if r "XX",8:wait 1
230: if rds("XX")=-1:jmp 0
231: sir 8,0:wait 10:eir 8,162:fat 8,+2,f1,0,f1,0,x,f8,0
232: "CLEAR TIME":1000+T:wtb 8,0:wtb 8,int(T-1):2
233: "WRITE TIME":200+U:wtb 8,13:wtb 8,int(U-1):2
234: "TEST":prt "HOW MANY MICROCIRCUITS?":0
235: dsr prt "ENTER HYBRID":prt "SERIAL NUMBER":f1,f1,f1,f1
236: for I=1 to 9:prt 8,I:next I
237: dsr "READY FOR TEST":eto
238: for I=1 to 7:for J=0 to 7:-1-X(I,J):next J:next I
239: fat 8,f2,0,x,f8,0,x,f8,0:fat 9,"PAIR ",f1,0,"x",f8,0
240: ret 7:c5,f1,0:rd 0
241: "#1":dsr "PERFORMING TEST #1":but "XX":1:dsr "TS1"
242: wtb 8,3072:esb "TS2"
243: prt "COUNTER":esb "TS3"
244: "#2":dsr "PERFORMING TEST #2":2+X:but "XX":1:dsr "TS1"
245: wtb 8,392
246: for I=1 to 10:wtb 8,C:wait 1
247: if rds(8)mod2=0: jmp 0
248: next I:esb "TS1"
249: wtb 8,3696:esb "TS2"
250: wrt "ERASE RECOVERY":prt "CHECK FOR B":fat "XX"
+10404

```

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Figure 4-19. Sample of Macrocode for the Hybrid Test Program

Table 4-28. Microcode Assembly Language Instruction Set

Mnemonic	I ₃	I ₂	I ₁	I ₀	Instruction
JZ	L	L	L	L	Jump to Address Zero
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register
JMAP	L	L	H	L	Jump to Address at Mapping PROM Output
CJP	L	L	H	H	Conditional Jump to Address in Pipeline Register
PUSH	L	H	L	L	Push Stack and Conditionally Load Counter
JSRP	L	H	L	H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register
CJV	L	H	H	L	Conditional Jump to Vector Address
JRP	L	H	H	H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register
RFCT	H	L	L	L	Repeat Loop if Counter is not Equal to Zero
RPCT	H	L	L	H	Repeat Pipeline Address if Counter is not Equal to Zero
CRTN	H	L	H	L	Conditional Return-from-Subroutine
CJPP	H	L	H	H	Conditional Jump to Pipeline Address and Pop Stack
LDCT	H	H	L	L	Load Counter and Continue
LOOP	H	H	L	H	Test End of Loop
CONT	H	H	H	L	Continue to Next Address
JP	H	H	H	H	Jump to Pipeline Register Address

78-0220-VG-3

Table 4-29 summarizes the six tests performed at the Functional Test Station. The referenced figures and tables document the details of each test (figures 4-21, 4-22 and tables 4-30, 4-31). The counter pattern test places unique data in every addressable row of the memory chips. This test verifies proper operation of the on-chip addressing circuitry. The series of erase-recovery tests (see paragraph 4.3.2 below) eliminate parts with marginal pulse response at the MNOS transistor cell. The zero pattern and one pattern tests are included for completeness to ensure against marginal escapes from the first three tests. The philosophy is that only a comprehensive test sequence can be trusted to certify that a part is suitable for use.

A final test called "read disturb" was included for experimental purposes, and to conform to a minimum read requirement of 10 cycles stated in the ECOM device specification SCS503 (table 4-32). It happens that the BORAM 6002 circuit was designed to enhance stored data every time the part is read. Thus reading should actually increase the data retention time. The read disturb test is expected to verify this characteristic.

b. Production Report

A sample copy of the production oriented test report for two hybrid circuits is shown in figure 4-23. The reports indicate the pass or fail status of each of the 16 chips in the hybrid.

This is an action document. It is intended that the reports for each hybrid will be cut apart, and will travel with the normal routing ticket documentation. The technician in charge of rework will locate a chip to be repaired using this report.

Test results are printed on the report in a manner which matches the physical location of the die on the hybrid substrate. This similarity in orientation was established to reduce the possibilities for human error in locating a specific die.

MICROCODE ASSEMBLY LANGUAGE MEMORY MAP

RAM ADDRESS	INST CODE	FIELD ONE	FIELD TWO	FIELD THREE	FIELD FOUR	HEX DISPLAY IN HEXADIGIT
128	LDCT	4065				80 C 0FE1
129	CONT	-P39	-TM1	-P12	PH1	81 E 0001
130	CONT	-P39	-TM1	-P12	PH2	82 E 0002
131	CONT	-P39	-TM1	-P12	PH4	83 E 0000
132	CJS	252	-GND			84 F F000
133	CJS	247	-GND			85 F F000
134	RPCT	129	CTR			86 A 811F
135	CRTN		-GND			87 A 0000
136	CONT	-P39	-AMR	-P12	P04	88 E 0000
137	CONT	-P39	-AMR	-P12	P04	89 E 0000
138	CRTN		-GND			8A A 0000
139	CONT	-P39	-TM1	-P12	P04	8B E 0000
140	CONT	-P39	-TM1	-P12	GCP	8C E 0007
141	CRTN		-GND			8D F 0000
142	LDCT	4095				8E C 0F7F
143	RPCT	143	CTR			8F A 8F1F
144	CRTN		-GND			90 A 0000
145	JZ					91 0 0000
146	CONT	-ST0	-BPE	-P12	P04	92 E 0400
147	CONT	-P39	-TM1	CLL	P04	93 E 0000
148	CONT	-P39	-TM1	-CSR	P04	94 E 0070
149	CONT	-FLG	-TM1	-CSR	P04	95 E 7060
150	CRTN		-GND			96 A 0000
151	JZ					97 0 0000
152	CONT	-P39	-CEP	-P12	P04	98 E 0500
153	CONT	-P39	-BCE	-P12	P04	99 E 0F00
154	CONT	-P39	-TM1	-P12	ACP	9A E 0004
155	CONT	-P39	-BCE	-P12	P04	9B E 0700
156	CONT	-P39	-CEP	-P12	P04	9C E 0000
157	CRTN		-GND			9D A 0000
158	JZ					9E 0 0000
159	JZ					9F 0 0000

REQ#700000

78-0332-VA-4

Figure 4-20. Sample Microcode Listing

Table 4-29. Summary and Description of Tests

Test Number	General Description	32-Bit Shift Register Data Pattern	References	
			Figures	Table
1	COUNTER PATTERN for addressing verification	row address = a MS 16 bits = $2a + 2$ in binary LS 16 bits = $2a + 1$ in binary	4-21 4-22	4-30
2	ERASE RECOVERY CHKBD Write CHKBD BAR 10 times Write CHKBD 1 time & read	CHECKER BOARD a even 1010 ~ 1010 a odd 0101 ~ 0101	4-21 4-22	4-31
3	ERASE RECOVERY CHKBD BAR Write CHKBD 9 times Write CHKBD BAR 1 time & read	CHECKERBOARD BAR a even 0101 ~ 0101 a odd 1010 ~ 1010	4-21 4-22	4-31
4	ZERO Write ZERO 1 time & read	0000 ~ 0000	4-21 4-22	4-30
5	ONE Write ONE 1 time & read	1111 ~ 1111	4-21 4-22	4-30
6	READ DISTURB ONE Read device 9 times	1111 ~ 1111	4-21 4-22	4-32

*Nominal supply conditions for all tests are VCC = +15V and VGG = -15V.

78-0219-TA 3 2

c. Engineering Report

A sample engineering oriented test report for two hybrid circuits appears in figure 4-24. This report presents the test results for each of six tests performed on each chip.

The engineering report is intended to allow a diagnosis of possible circuit problems to guide rework action. To use this tool the engineer or technician must be familiar with the nature of the individual tests.

As an example consider the results for chip 06 in hybrid 00015. This chip passed the counter pattern, erase recovery-checkerboard bar, zero pattern, one pattern, and read disturb tests. This implies that the chip functions properly. All wires must be in place, and all on-chip circuitry must operate. The chip failed the erase recovery-checkerboard test. This implies that some memory transistor(s) are slow in recovery from multiple clearing. Thus in this case the rework action required is to replace the chip.

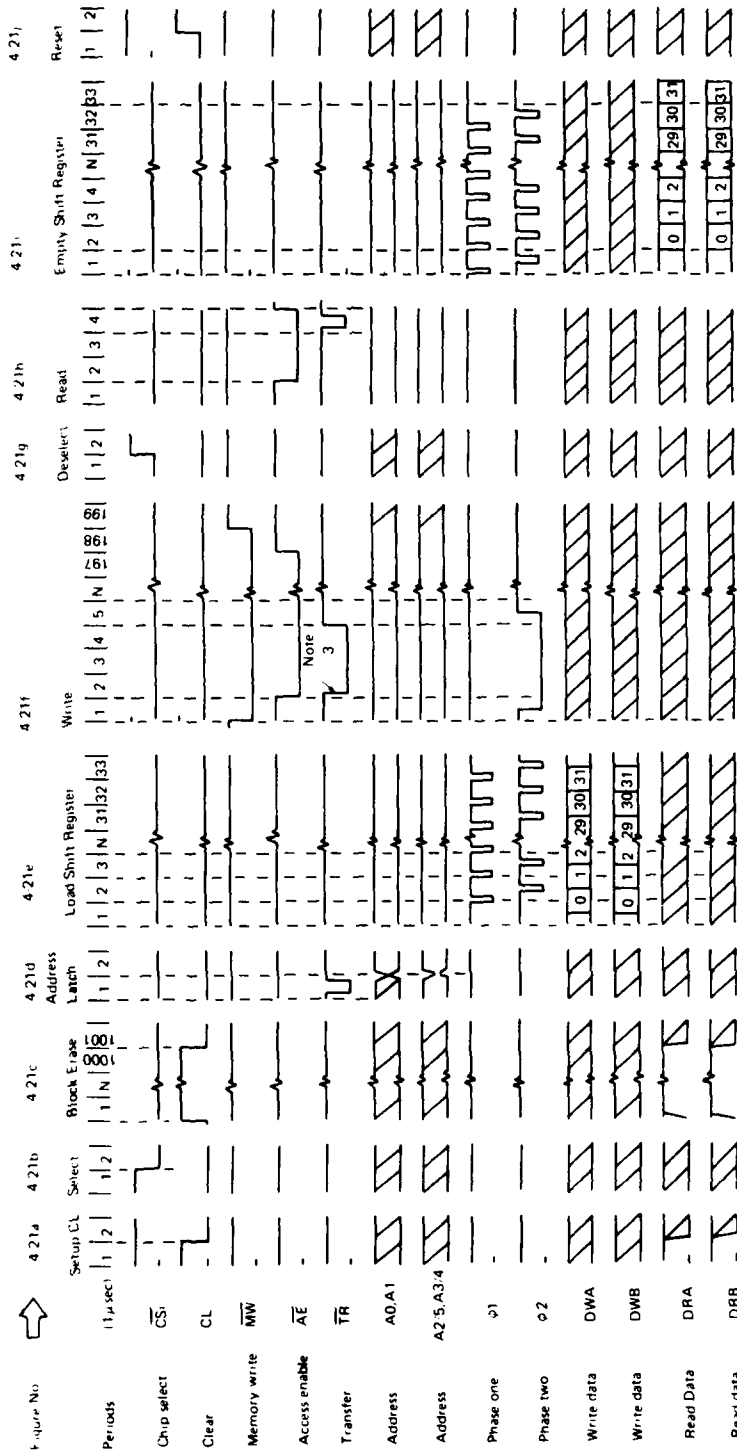
In other cases the combination of test results may indicate a wire bond problem, and detailed visual inspection would be called for.

d. Throughput Observations

The throughput capacity of the BORAM functional test station has been examined by formulating the sequence of actions an operator must perform, and by timing each individual action.

In this experiment, the actions were performed by engineers who had no significant previous experience with the detailed motions involved. Because the engineers lack the dexterity which would be acquired by a test operator, the observed times are believed to be pessimistic.

The scenario for a test operator involves two phases. A "start-up activity" sequence prepares the test system and the first group of eight hybrids for test. An "operating activity" maintains a continuous flow of hybrids through the test system by repeating a sequence of operations. It is assumed that the operator is continuously being given a supply of hybrids to be tested, and that hybrids which have been tested are removed together with the test reports by other personnel.



- NOTES
- ① A period is 1 microsecond in duration
 - ② Transitions within a period occur at 250 nsec, 500 nsec or 750 nsec except per ③
 - ③ In figure 4-21f TR goes low 100 nsec after AE goes low
 - ④ don't care condition
 - ⑤ Rise and fall times (10% to 90%) are ≤ 50 nsec
 - ⑥ DRA and DRB logic zero < VCC - 10.5 volts, logic one ≥ VCC - 4.5 volts

78-0332-VA 5.1

Figure 4-21. Operating Sequences for Functional Tests

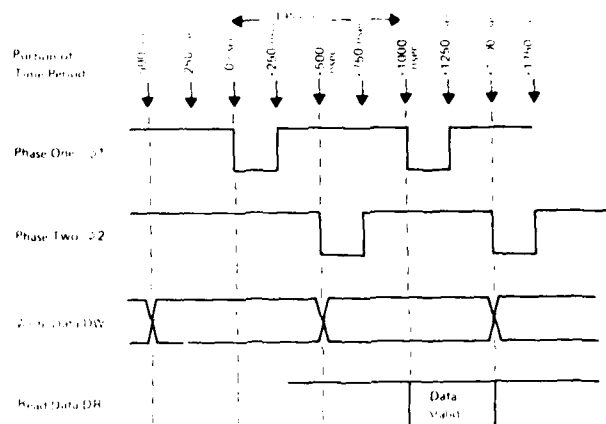


Figure 4-22. Detailed Timing for Clocks and Data
 1. Q1 and Q2 are outputs of 10, 100, or 500 ns.
 2. DQ only change at times other than those already provided. 1.5 ns is minimum phase time.

78-0332 TA-6-1

Figure 4-22. Detailed Timing for Clocks and Data

Table 4-30. Memory Tests Logical Flow Sequence

Step	Logical Operation
1	Setup CL per fig. 4-21a
2	Initialize chip select counter ($i=0$ and $\overline{CS_i} = \overline{CS_0}$)
3	Setup $\overline{CS_i}$ per fig. 4-21b
4	Erase selected chips per fig. 4-21c
5	Initialize address counter (address = 0)
6	Setup address lines per fig. 4-21d
7	Set data pattern per table 4-29
8	Load DWA and DWB shift registers per fig. 4-21e
9	Write data per fig. 4-21f
10	Increment address counter (address = address + 1)
11	If (address < 64) then 6
12	Reset $\overline{CS_i}$ per fig. 4-21g
13	Increment chip select counter ($i=i+1$ and $\overline{CS_i} = \overline{CS_{i+1}}$)
14	If ($i < 8$) then 3
15	Initialize chip select counter ($i = 0$ and $\overline{CS_i} = \overline{CS_0}$)
16	Setup $\overline{CS_i}$ per fig. 4-21b
17	Initialize address counter (address = 0)
18	Setup address lines per fig. 4-21d
19	Read data to latch per fig. 4-21h
20	Empty DRA and DRB shift registers per fig. 4-21i
21	If (data $\neq$ (per table 4-29)), then record FAIL
22	Increment address counter (address = address + 1)
23	If (address < 64) then 18
24	Reset $\overline{CS_i}$ per fig. 4-21g
25	Increment chip select counter ($i = i+1$ and $\overline{CS_i} = \overline{CS_{i+1}}$)
26	If ($i < 8$) then 16
27	Reset CL per fig. 4-21j
28	End Routine

78-0332 TA-6-1

Table 4-31. Erase Recovery Tests Logical Flow Sequence

Step	Logical Operation
1	Setup CL per fig. 4-21a
2	Initialize write counter ($j=0$)
3	Initialize chip select counter ($i=0$ and $\overline{CS_i} = \overline{CS_0}$)
4	Select $\overline{CS_i}$ per fig. 4-21b
5	Erase selected chips per fig. 4-21c
6	Initialize address counter (address = 0)
7	Setup address lines per fig. 4-21d
8	Set data pattern per table 4-29
9	Load DWA and DWB shift registers per fig. 4-21e
10	Write data per fig. 4-21f
11	Increment address counter (Address = Address + 1)
12	If (address < 64) then 7
13	Reset $\overline{CS_i}$ per fig. 4-21g
14	Increment chip select counter ($i = i+1$ and $\overline{CS_i} = \overline{CS_{i+1}}$)
15	If ($i < 8$) then 4
16	Increment write counter ($j = j+1$)
17	If ($j < 11$) then 3
18	Initialize chip select counter ($i = 0$ and $\overline{CS_i} = \overline{CS_0}$)
19	Select $\overline{CS_i}$ per fig. 4-21b
20	Erase selected chips per fig. 4-21c
21	Initialize address counter (address = 0)
22	Setup address lines per fig. 4-21d
23	Setup data pattern (complement of step 8 data)
24	Load DWA and DWB shift registers per fig. 4-21e
25	Write data per fig. 4-21f
26	Increment address counter (address = address + 1)
27	If (address < 64) then 22
28	Reset $\overline{CS_i}$ per fig. 4-21g
29	Increment chip select counter ($i=i+1$ and $\overline{CS_i} = \overline{CS_{i+1}}$)
30	If ($i < 8$) then 19
31	Initialize chip select counter ($i = 0$ and $\overline{CS_i} = \overline{CS_0}$)
32	Select $\overline{CS_i}$ per fig. 4-21b
33	Initialize address counter (address = 0)
34	Setup address lines per fig. 4-21d
35	Read data to latch per fig. 4-21h
36	Empty DRA and DRB shift registers per fig. 4-21i
37	If (data $\neq$ per table 4-29) then record FAIL
38	Increment address counter (address = address + 1)
39	If (address < 64) then 34
40	Reset $\overline{CS_i}$ per fig. 4-21g
41	Increment chip select counter ($i = i+1$ and $\overline{CS_i} = \overline{CS_{i+1}}$)
42	If ($i < 8$) then 32
43	Reset CL per fig. 4-21j
44	End Routine

78-0332-TA-7 1

Table 4-32. Read Disturb Test Logical Flow Sequence

Step	Logical Operation
1	Setup CL per fig. 4-21a
2	Initialize read loop counter (J=0)
3	Initialize chip select counter (i=0 and $\overline{CS_i} = \overline{CS_0}$)
4	Setup $\overline{CS_i}$ per fig. 4-21b
5	Initialize address counter (address = 0)
6	Setup address lines per fig. 4-21d
7	Read data to latch per fig. 4-21h
8	Empty DRA and DRB shift registers per fig. 4-21i
9	If (data $\neq$ one) then record FAIL
10	Increment address counter (address = address + 1)
11	If (address < 64) then 6
12	Reset $\overline{CS_i}$ per fig. 4-21g
13	Increment chip select counter (i=i+1 and $\overline{CS_i} = \overline{CS_{i+1}}$)
14	If (i < 8) then 4
15	Increment read loop counter (J = J+1)
16	If (J < 9) then 3
17	Reset CL per fig. 4-21j
18	End Routine

78-U332-TA-8 -1

ROUTINE 1: CIRCUIT FUNCTIONAL TEST

TEST # 1000 10-199-1

CHIP 1 PASS	CHIP 2 PASS
CHIP 3 PASS	CHIP 4 PASS
CHIP 5 PASS	CHIP 6 PASS
CHIP 7 PASS	CHIP 8 PASS
CHIP 9 PASS	CHIP 10 PASS
CHIP 11 PASS	CHIP 12 PASS
CHIP 13 PASS	CHIP 14 PASS
CHIP 15 PASS	CHIP 16 PASS

ROUTINE 2: CIRCUIT FUNCTIONAL TEST

TEST # 1000 10-199-1

CHIP 1 PASS	CHIP 2 PASS
CHIP 3 PASS	CHIP 4 PASS
CHIP 5 PASS	CHIP 6 PASS
CHIP 7 PASS	CHIP 8 PASS
CHIP 9 PASS	CHIP 10 PASS
CHIP 11 PASS	CHIP 12 PASS
CHIP 13 PASS	CHIP 14 PASS
CHIP 15 PASS	CHIP 16 PASS

78-U332-VA-8

Figure 4-23. Sample Production Oriented Test Report

BOPRM HYBRID MICROCIRCUIT FUNCTIONAL TEST 10 JAN 70
 Clear 1000 microseconds Write 100 microseconds

SERIAL NUMBER	CHIP NUMBER	TEST #1	TEST #2	TEST #3	TEST #4	TEST #5	TEST #6	ALL TESTS
00014	01	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	02	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	03	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	04	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	05	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	06	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	07	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	08	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	09	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	10	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	11	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	12	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	13	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	14	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	15	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00014	16	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	01	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	02	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	03	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	04	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	05	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	06	PASS	---	PASS	PASS	PASS	PASS	---
00015	07	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	08	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	09	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	10	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	11	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	12	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	13	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	14	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	15	PASS	PASS	PASS	PASS	PASS	PASS	PASS
00015	16	PASS	PASS	PASS	PASS	PASS	PASS	PASS

78-0332-VA-10

Figure 4-24. Sample Engineering Oriented Test Report

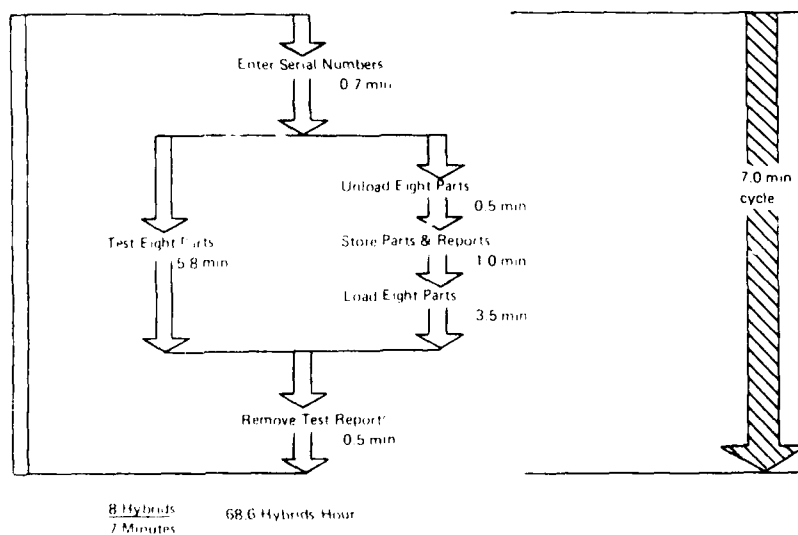
A working assumption is that hybrids are brought to the test station in a container in groups of eight. The container also accommodates the routing ticket and other traveling manufacturing documentation. Each hybrid is labeled by a control number or serial number easily seen by the operator.

The operator's responsibility is to see that each hybrid is tested, and that the hybrids are returned to the proper container with the test reports. The serial numbers on the reports uniquely relate the data to the part.

To maintain a steady flow of product the operator must use both test channels. While channel A is engaged in testing eight hybrids, the operator must unload and reload channel B. Figure 4-25 shows this operating sequence and gives the times observed for each element. An operator should be able to cycle eight parts every 7 minutes.

For the set of assumptions given this should be a comfortable working rate. In terms of hybrids per hour it amounts to 68.6. In paragraph 4.4.1.1d it was shown that an upper bound on the throughput requirement was 62 hybrids per hour.

The setup activity was also examined. To prepare the test system, about 0.5 minutes are required to insert the tape cartridge and load the test program. To run the initialization portion of the program takes 0.6 minutes. The initial loading of eight hybrids into test sockets takes about 3.5 minutes. The sum of these times is 4.6 minutes.



78 0332 VA 11

Figure 4-25. Sequence of Operations for the BORAM Functional Test

5. HYBRID CIRCUIT FABRICATION

The MNOS BORAM hybrid circuit packaging approach was conceived to provide low cost, high density and growth potential simultaneously. A baseline fabrication approach was established which made use of previously defined materials, processes and tooling. At the same time each element of hybrid was defined to easily allow the introduction of new materials, processes and tooling. During the course of the MM&T project several improvements were introduced, and several others have been defined and are being developed.

5.1 HYBRID CIRCUIT DESCRIPTION

The MNOS BORAM hybrid is approximately one by two inches, and it contains 16 BORAM monolithic integrated circuits. Both the physical and electrical configuration of the hybrid are important in achievement of low cost manufacture.

5.1.1 Component Parts

The initial configuration of the 647R527G01 hybrid circuit is shown in figure 5-1. The component parts are illustrated in figure 5-2. A 24-pin metal case houses an epoxy bonded alumina substrate. The multilayer substrate provides the interconnection pattern for 16 epoxy bonded 6002 chips. A hermetic seal is achieved by using a solder preform to attach a lid to the metal case.

The configuration of the 647R527G01 hybrid was modified during the MM&T to incorporate the use of a welded lid, and to change some dimensional details of the metal case.

5.1.2 Electrical Configuration

A significant advantage of the BORAM hybrid electrical configuration is that it does not impose any serious constraints on the hybrid circuit fabrication approach. Close control of impedance levels, propagation delays and crosstalk is not necessary for proper circuit operation.

The details of the electrical circuit were described in Section 4 on electrical testing. The input terminals of 6002 chips are high impedance lines, and thus series input resistance is not critical. Input capacitance is not critical either, but it should be held to low levels to avoid placing excessive demands on external driver circuitry. Table 5-1 presents the capacitance values used for circuit design purposes. These numbers are slightly higher than values actually measured on hybrid circuits.

5.1.3 Thermal Configuration

Circuit reliability is dependent on the thermal characteristics of the packaging approach. Early in the MM&T program approximate thermal models were developed to ensure that proper consideration was given to this important factor.

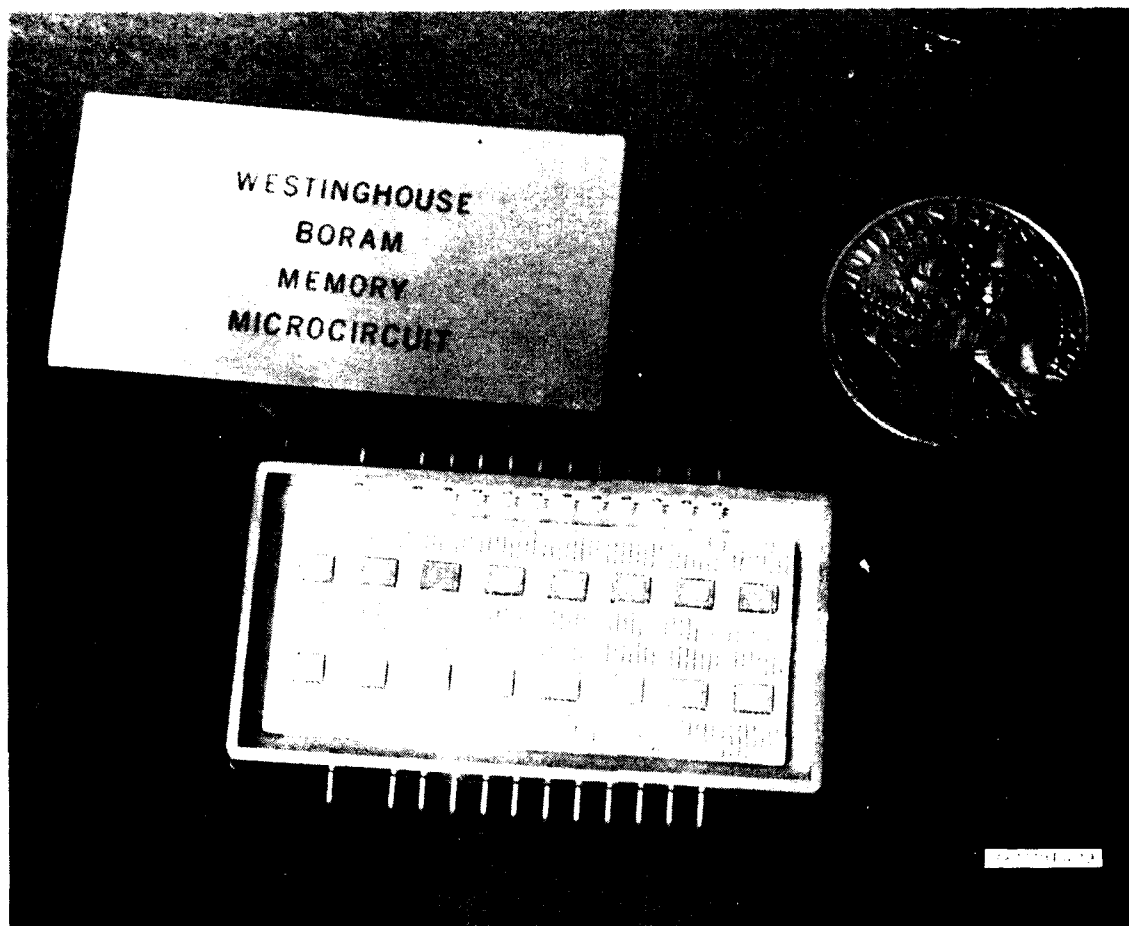


Figure 5-1. Initial Configuration of Westinghouse Part 647R527G01

Figure 5-3 shows the thermal situation for one chip within the hybrid. The chips are positioned sufficiently far apart, and have such a low-duty cycle that thermal interaction should be negligible. Table 5-2 quantifies the individual elements of the approximate model.

The model predicts $10.59^{\circ}\text{C}/\text{watt}$ for a single die. Since two chips are active at any given time, the hybrid circuit thermal resistance is $5.3^{\circ}\text{C}/\text{watt}$. Because of a change in alumina substrate thickness, a more recent version of the hybrid circuit has a thermal resistance less than $5^{\circ}\text{C}/\text{watt}$.

5.2 HYBRID SUBSTRATE

The hybrid circuit substrate provides for the electrical interconnection and mechanical support of the BORAM monolithic chips.

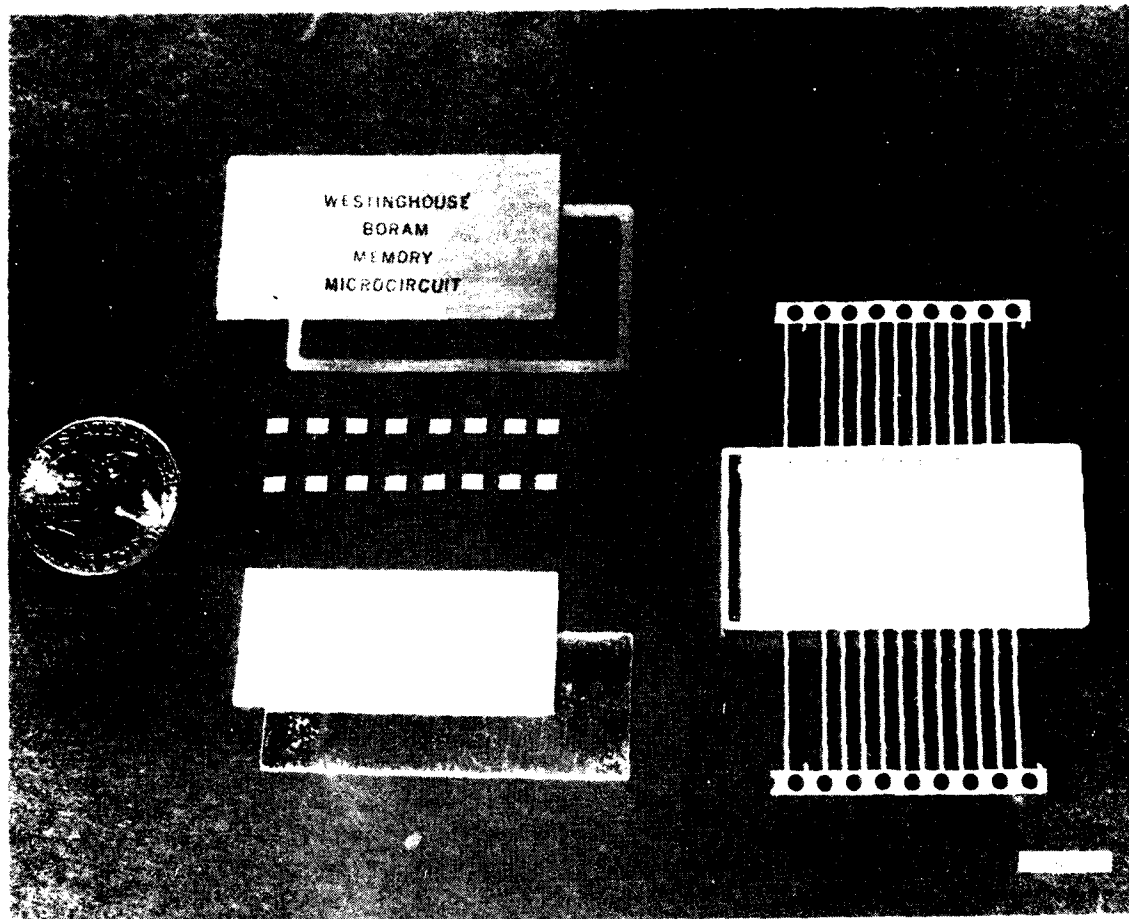
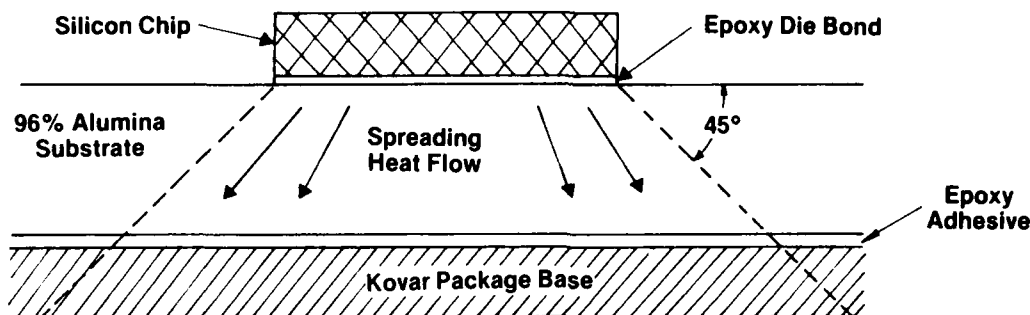


Figure 5-2. Component Parts of the Initial Configuration of Part 647R527G01

Table 5-1. Part 647R527G01 Input Capacitance

Signal Description	Symbols	Capacitance (pf)
Clock Inputs	$\phi 1, \phi 2$	135
Chip Select Inputs	$\overline{CS0}$ to $\overline{CS7}$	35
Control Inputs	$\overline{AE}, \overline{MW}, \overline{TR}$	80
Clear Input	CL	160
Address Inputs	A0 to A3	90
Write Data Inputs	DWA, DWB	40
Read Data Outputs	DRA, DRB	60

79 1110 1A 13



$$\theta_{JC} = \theta_{\text{silicon}} + \theta_{\text{epoxy 1}} + \theta_{\text{alumina}} + \theta_{\text{epoxy 2}} + \theta_{\text{kovar}}$$

77-0663-BB-11

Figure 5-3. MNOS BORAM Hybrid Circuit Simplified Thermal Model

5.2.1 Substrate Structure

Many fabrication options exist for the substrate. The particular implementation chosen was compatible with existing Westinghouse processes and tooling.

The substrate dimensions are 1.700 by 0.780 inches. Interconnection is accomplished by four metal layers. The layers are separated by and supported by a dielectric material. Layer-to-layer interconnections are made by 0.015 by 0.015 inch vias. The top metal layer is exposed, and provides pads for wire bonding.

The base material is alumina. For MM&T production the alumina was 0.040-inch thick. More recently it has become possible to reduce the alumina thickness to 0.020 inch.

5.2.2 Multiple Substrate Screening

To reduce the labor content of substrate manufacture, six hybrid circuit substrates were silkscreened on a single piece of alumina. After completion of all screening and firing operations the individual substrates were separated by sawing.

Table 5-2. MNOS BORAM Hybrid Circuit Thermal Resistance Components

Material	Thermal Conductivity K watts/inch °C	Material Thickness t inches	Effective Cross-Section (L) (W) inches ²	Thermal Resistance θ °C/watt
Silicon	3.60	0.016	(0.099) (0.128)	0.35
Epoxy	0.025	0.001	(0.099) (0.128)	3.16
Alumina	0.670	0.046	(0.145) (0.174)	2.72
Epoxy	0.020	0.003	(0.194) (0.223)	3.47
Kovar	0.420	0.020	(0.217) (0.246)	0.89

$$\theta = t/K L W$$

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5.2.3 Multiple Bonding Options

Layout of the top layer of the substrate allowed the use of conventional wire bonding or tape bonding. The pads were defined to accept tape carrier versions of the 2K-bit, 8K-bit and larger chips in the 6000 series.

5.2.4 Automatic Probe Test

Each substrate is tested for interconnect pattern continuity. Both opens and shorts are screened. The equipment employed for MM&T production is called a Flying-Head Probe. This equipment employs two probes that are moved from point-to-point under computer control. Probing paths are optimized by software during programming. The final control program is stored on a magnetic tape cartridge.

5.3 HYBRID PACKAGE

A metal case was chosen for the BORAM hybrid circuit primarily because of its cost potential. The package external dimensions were selected to maintain compatibility with tooling for previously developed ceramic packages.

5.3.1 Standardization Approach

Economy and reliability can be achieved when packages are manufactured in volume for multiple users. To promote this situation, Westinghouse strives to reduce the variability in package use by establishing standard options for designers.

The basic specification for the BORAM hybrid metal case establishes the materials, processing and quality assurance provisions for a family of packages.

5.3.2 Package Options

Flexibility in package definition and room for growth is maintained by allowing various package options to be specified without altering the basic specification. One such feature under current study is the option of using nickel coated cases instead of gold coating. Elimination of gold can mean a significant cost saving. Procurement options are specified by suffix digits on the package part number.

5.3.3 Oil Canning Problem

During the course of the MM&T, it was discovered that the 0.015-inch thickness of the bottom of the package was not adequate to meet mechanical stress requirements. During centrifuge tests at 10,000g the base of the case would bow inward. The resulting stress on the alumina substrate would either cause cracking of the alumina or separation of the substrate from the case at the epoxy bond.

After extensive tests, it was established that the use of an 0.020-inch base would allow survival of 10,000g stresses. The mass of the substrate was also reduced by the use of 0.020-inch thick alumina instead of 0.040 inch.

5.4 HYBRID PROCESSING

For the most part the hybrid assembly procedure made use of well established processing and tooling. In the areas of bonding to the chips and sealing the case changes were introduced which deserve special comment.

5.4.1 Chip Lead Bonding

The initial approach employed for connecting the BORAM chip pads to the appropriate pads on the substrate was a manual technique. An operator would use 0.001-inch gold wire in an ultrasonic bonder to connect each chip. The use of ultrasonics avoided high temperatures during processing.

Later, the throughput and reliability of bonding was improved by the introduction of a computer controlled wire bonder. The automatic wire bonder consists of an ultrasonic bonder, a master console, a disk memory, an operators control pendant and a power supply.

Computer controlled bonding was used with good results during the pilot production run. The machine achieves bonding speeds at least six times faster than that of a manual station.

In the future tape bonding will be employed for BORAM hybrids. During the time period of the MM&T, but under separate funding, Westinghouse has fabricated and tested tape carrier BORAM hybrids.

Several aspects of the tape carrier technology have motivated its development for BORAM. This approach should lower assembly costs by direct automation and by reduction of rework. It also holds promise for an increase in reliability because of greatly increased bond strength. Gold 0.001-inch wire bonds have a typical bond strength of less than 6 grams. Tape bonds typically show bond strength greater than 50 grams.

The availability of tape mounted chips makes it possible to test and burn-in every chip before it is inserted into a hybrid package. This capability is expected to sharply reduce the need for removal of chips from the hybrid after initial assembly, and to reduce the failure rate through hybrid package burn-in.

5.4.2 Package Sealing

As described earlier the initial sealing approach was to solder the lid to the case. A preform was employed to standardize the amount of solder and the distribution of the solder.

For several reasons the soldering approach was less than ideal. The solder preform was expensive because of the mechanical dimensions and the particular alloys required. Solder flow was not well controlled, and solder splashes down the side of the package were common. Although no data was gathered to confirm the phenomena, it was feared that solder particles could end up inside a sealed package and become a reliability hazard. In addition, there was a small but significant yield loss through the sealing operation after hermeticity tests.

To avoid these problems a welded lid was introduced. The new process was successfully used for the MM&T pilot production. Yield through hermeticity tests approached 100 percent. The individual hybrid circuit appearance was improved because of the elimination of solder splashes. More important the package reliability was improved.

The lid used for soldering was simply a flat rectangular piece of metal. The lid used for welding is stepped down in thickness around the periphery where the weld is to be made. Westinghouse has developed techniques for the removal of a welded lid, and for the successful resealing of the package. This ability to delid, rework and reliably reseal a hybrid opens new opportunities for improved economics.

6. DISTRIBUTION LIST

Addressee	Qty	Addressee	Qty
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