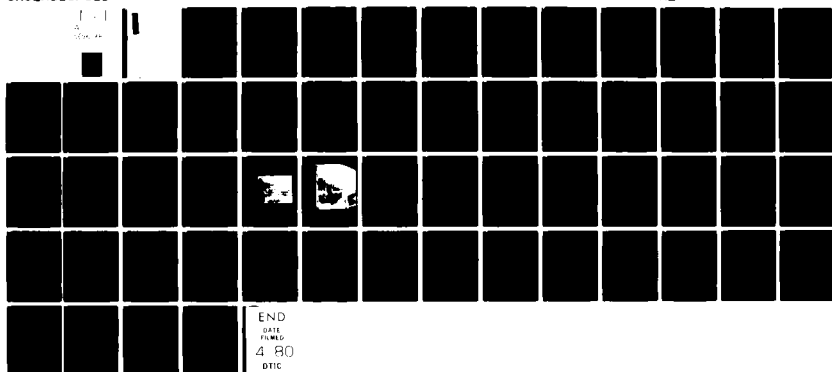


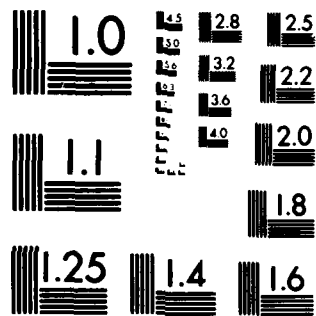
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ABSTRACT

A microprocessor based electron beam lithography system has been developed for production of Schottky barrier diodes with submicron geometric features.

The electron beam lithography system is described along with details of the fabrication procedure. Complete logic diagrams and listings of the microprocessor operating software are included.

1.0 Introduction.

In a number of areas of semiconductor device technology there is an increasing need for fabrication techniques useful in producing devices with geometric features smaller than one micrometer. Typical applications include Large Scale Integrated circuits, Microwave Transistors (and gigabit rate logic) and improved performance Schottky-barrier diodes for use at millimeter and sub-millimeter wavelengths. Reasons for utilizing sub-micron geometries are both economic (improved yield through reduced chip size) in the case of LSI circuitry, and enhanced performance in the case of the microwave devices. The system described below has been developed primarily for the fabrication of Schottky barrier diodes with complex submicron features. These diodes will then be compared with theoretical models to investigate techniques for reduction of equivalent series resistance by control of device geometry.

Fabrication of semiconductor devices with submicron features requires a fundamental departure from conventional photolithographic techniques. Ultimate resolution in photolithographic processes is almost wholly limited by the wavelength of the light source utilized to expose the resist-coated semiconductor. The resolution limitation occurs when features in the mask begin to approach the wavelength of the exposing illumination source. As the feature size approaches the illumination wavelength, diffraction mechanisms cause the "shadows" of the mask on the substrate to lose their sharp edges hence reducing the contrast of images formed on the semiconductor. The reduced contrast, upon development of the photoresist, increases the size of the resulting image, hence increasing the size of the minimum producible feature. The electron beam lithographic system described here overcomes this problem by eliminating the wavelength-of-light dependence, instead resolution is limited by resist chemistry and this limit is at least one order of magnitude and perhaps two orders of magnitude smaller than the limit imposed by conventional photolithography. Conventional device fabrication processes using UV light sources have a resolution limit of approximately 1.0 micrometer. Electron beam systems typically achieve 0.1 micrometer resolution and with careful control of resist chemistry and processing, resolution of ~ 0.01 micrometer (100 Å) has been reported.

The system developed for electron beam lithography is shown in block diagram form in Figure 1. The U.C.C. owned JEOL JSM-35 Scanning Electron Microscope with a JEOL model BBD-35 beam blanking device installed is used as an electron beam source. The beam is switched on and off to form the image in the resist in synchronism with both scanning and pattern data signals by a microprocessor based controller called

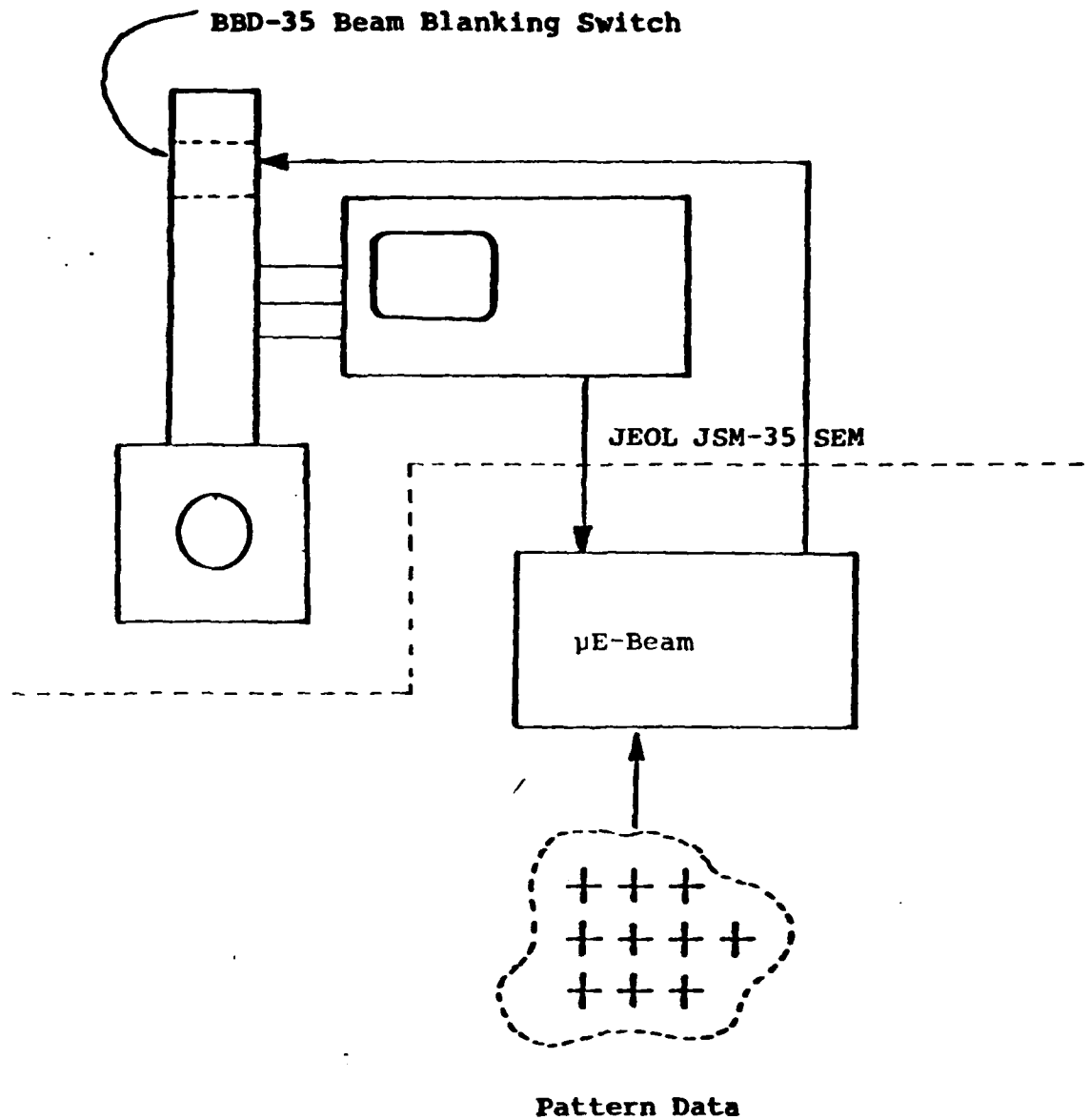


Figure 1. Block Diagram Electron Beam Lithography System.

the μ E-beam. The μ E-beam controller and its operation are described in greater detail in the following sections.

2.0 The μ E-Beam System.

2.1 Design Criteria.

The design of the microprocessor based electron beam exposure system developed for this program is based on the following criteria:

- (1) The system must be invisible to the normal operation of the electron microscope. This requirement is forced both by the shared usage of the SEM with other departments in the College, as well as the necessity of using the microscope in its usual mode for examination of devices produced by E-beam lithography. In addition, the standard observational mode provides a convenient method for focussing and initial alignment of the electron beam prior to exposure.
- (2) Raster graphic techniques must be employed in pattern formation. Although powerful arguments exist for vector graphic exposure systems, the benefits of the raster graphic approach are more applicable in this instance. First, interface to the SEM is simpler since all scan signals to form the raster are already generated by the SEM. One need only switch the electron beam on and off in synchronism with the pattern and scan signals to form an image. Second, for the relatively simple patterns required by Schottky diodes which are repeated many times over the exposure area, pattern specification is simpler than with a vector graphic system. In cases where more complicated patterns might be required (as for example, a microwave FET) powerful pattern compaction algorithms are available which will minimize the storage requirements for pattern data. Raster graphics also allow slightly simpler utilization of serial access data storage media such as magnetic tape.
- (3) The system must be versatile and upward expandable for future growth to more complex applications. For initial use the versatility of the system must allow for rapid change of exposure patterns. For later applications, the ability to handle pattern data in magnetic tape form as well as performing registration for multiple exposures must be possible within the confines of the original design.

The system which satisfies these criteria is described in some detail in the following sections.

2.2 Beam Blanking Switch.

The switching of the electron beam is performed by a JEOL model BBD-35 beam blanking device. This device, purchased from and fitted by JEOL (the SEM manufacturers) is located in the electron column between the electron gun and the entrance to the first electron lens. Beam switching is accomplished as shown in Figure 2. When the blanking coil is not energized, the electron beam passes normally through the aperture plate. When the blanking coil is energized the beam is deflected to the side and out of the open aperture, thus effectively shutting off the electron beam to the sample. The switching time for the blanking device is specified by JEOL to be less than 1.0 micro-second. Associated with the beam blanking device is a pulse amplifier to take a low level input and produce sufficient current to drive the blanking coil.

2.3 Principles of operation.

The μ E-Beam system is based on the Motorola 6800 micro-processor and its associated family of components. As in most microprocessor based systems it is convenient to separately discuss the hardware and software aspects of the system, this is done in sections 2.4 and 2.5. However, an overview of the basic operational principles will simplify understanding of both hardware and software; this is given here.

As described above the pattern image is formed via a raster graphic approach. The raster generated by the SEM consists of 2500 horizontal lines per frame. The scan rate used is approximately 40 milliseconds per line, thus giving approximately 100 seconds per frame. Due to the rectangular format of the raster, there are approximately 3200 resolution cells per horizontal line, giving a total resolution of 3200 x 2500 equal area cells. The μ E-beam senses the beginning and end of each horizontal scan line by the horizontal blanking signal from the scan generator in the SEM. Each horizontal scan line is subdivided into 3200 addressable time slots by the μ E-beam. By sensing when the frame starts (from the PHOTOSTART signal from the SEM scan generator) and then counting horizontal lines and turning the beam on or off at selected time slots within each horizontal line, the image is formed in a manner analogous to a monochrome television receiver. The μ E-beam does not use the entire 3200 x 2500 array of possible cells, but a subset 2048 x 2048 near the center. The scan geometry is shown in Figure 3. The reasons for this are several: First, non-linearities in deflection

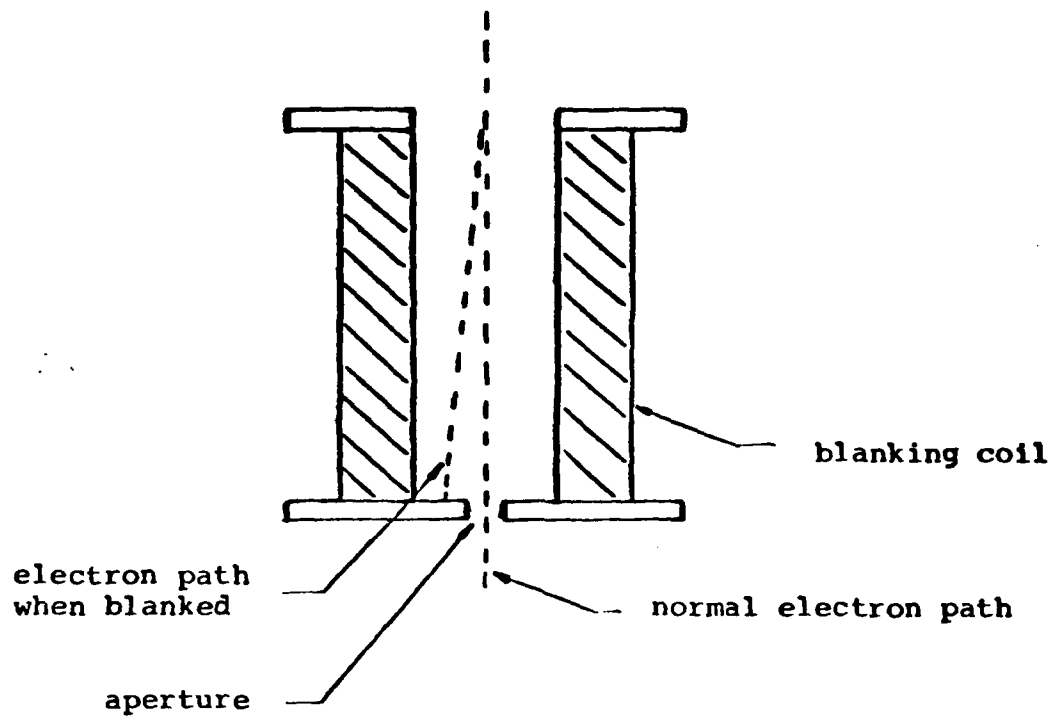


Figure 2. Beam Blanking Switch.

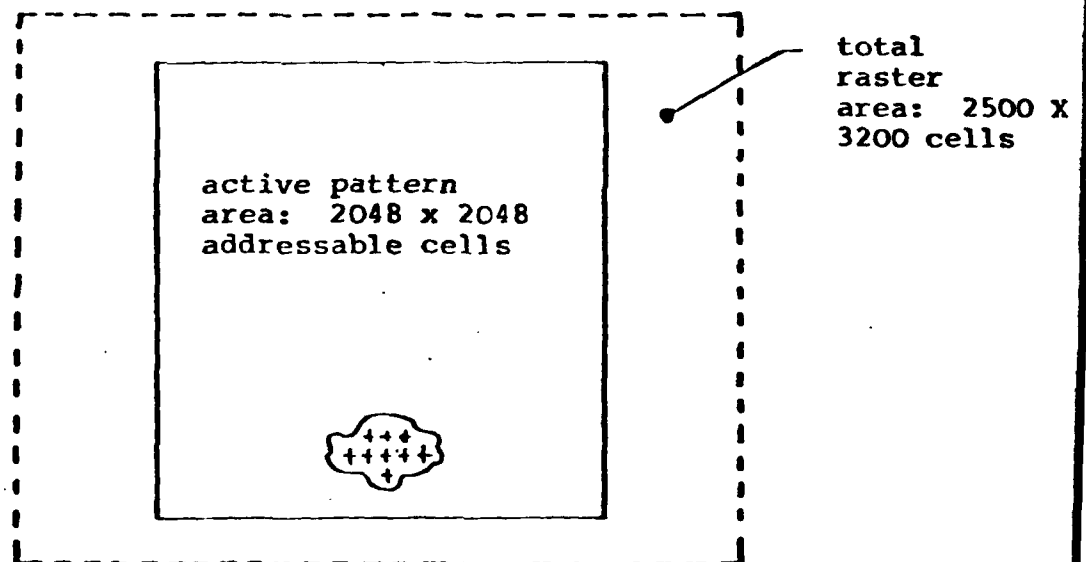


Figure 3. Scan geometry.

are more apt to be serious near the edges of the scan; second, a margin at the top allows time for synchronisation with the scan signals for each exposure; third, 2048 x 2048 is a more convenient dimension from the point of view of the microprocessor system.

Up to this point the scan dimensions have been described in unit-less terms. This is because the physical dimension of the scanned area is solely a function of the magnification setting of the microscope which is adjusted so that the 2048 x 2048 image area, covers a physical region approximately 205 x 205 micrometers. This gives a minimum resolution cell of 0.1 x 0.1 micrometers (1000 Å x 1000 Å). This forms a lower limit for pattern features well suited to most millimeter devices as well as to the achievable resolution of the resist. In addition the 205 x 205 micron size means the process steps developed for handling the 250 micron square diode chips produced by photolithographic techniques within the Solid State Electronics Laboratory are easily applicable to the E-beam lithography devices.

2.4 µE-Beam Hardware.

The µE-Beam is comprised of two basic functional units: the microprocessor board and the interface board. The microprocessor board is from the Motorola Micro Module Family, a 68MM01A single board computer, while the interface board was custom designed for this application. These two circuit boards along with power supplies, cooling fan and a small circuit board containing lamp and switch drivers and a level shifter for the Beam Blanking Device are housed in a Motorola 68MMSC5 card cage. A block diagram is shown in Figure 4.

2.4.1 Microprocessor.

The 68MM01A is a complete microcomputer on a single PC board. Included are a system clock, MPU, 1 kilobyte of RAM, 32 lines parallel I/O and an asynchronous serial communication port. The necessary bus interface circuitry is also included to allow the 68MM01A to function in a bus oriented environment. A total of 4kbytes of ROM is decoded on the board. In this application, the highest 1 kbyte is used for a modified version of Motorola's MICROBUG debug/monitor program, approximately 1 kbyte is devoted to the system software leaving approximately 2 kbytes of onboard address space for pattern storage. As will be discussed below the operating system is readily expandable to more complicated tasks, such as handling a tape drive for complex pattern, registration etc.

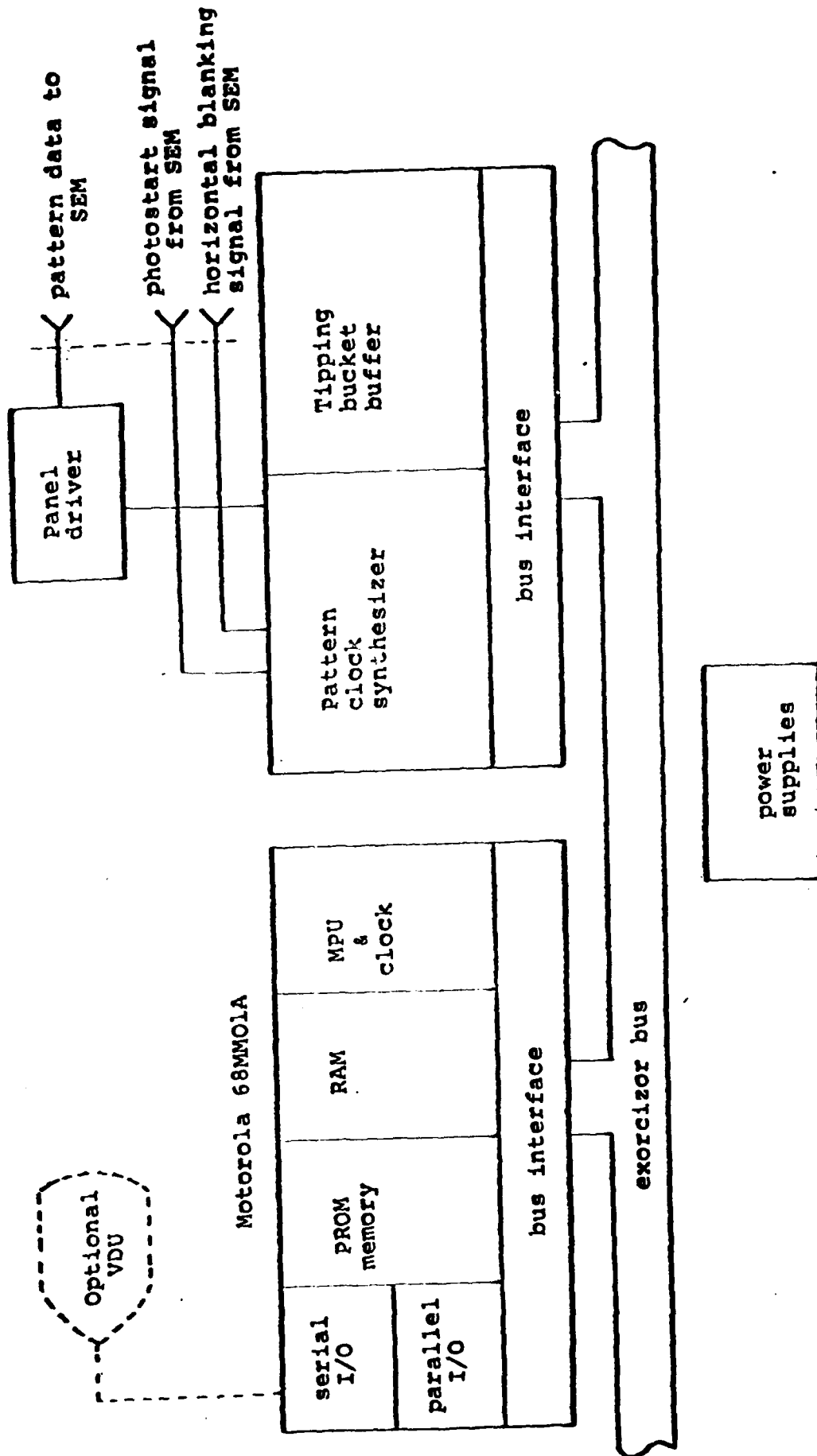


Figure 4. Block diagram uE-Beam System.

2.4.2 Interface Board.

The interface board consists of three functional units: bus interface and address decoders, timing synthesizer, and a tipping bucket buffer. Bus interface and address decoding is accomplished via standard low power schottky TTL integrated circuits, and standard TTL bus transceivers. Address, data and control signals are accepted from the bus and processed to provide the signals required by the other sections of the interface. A schematic of the bus interface is shown in Appendix A. A block diagram of the Interface Board is shown in Figure 5.

The timing synthesizer is built around a Motorola MC6840 programmable timer. The three sections of the timer are dedicated to: (1) synchronization with SEM horizontal blanking signals; (2) generation of enabling signals to the tipping bucket buffer; (3) counting horizontal blanking pulses to define image areas. Synchronization is accomplished in conjunction with a frequency synthesizer composed of a 19.6608 MHz crystal oscillator and a 12 bit programmable divider. The 12 bit divider consists of a 4 bit pre-scaler, set by jumpers and an 8 bit divider under microprocessor control through the A-section of a MC6821 PIA. In operation the programmable divider is used to provide a clock signal running at approximately 3200 times the SEM horizontal line frequency. The synchronization process is controlled by the microprocessor via information supplied by one section of the 6840 programmable timer. The details of synchronization process are described in the software section.

Once synchronized with the SEM the 3200X clock, (called the pattern clock) is gated with a delay output from the second section of the programmable timer to generate the clock signal used to write the pattern data out to the beam blanking switch. The third section of the 6840 is used to count horizontal scan lines by counting the horizontal blanking pulses. The output from this section is used to define top and bottom margin regions as well as to provide a linecount in the active pattern region for use in pattern generation.

The tipping bucket buffer is comprised of two 256 byte (2048 bit) buffers, switching circuits to switch data and address sources, and address generation and control circuitry. The two identical buffers are implemented with Motorola MC6810 128 byte RAMS. At any instant, the address and data lines of one buffer are connected to the microprocessor address and data bus, and the other buffer is connected to the address generation circuits on the Interface Board. The buffer connected to the address generator on the interface then is supplying pattern data for the current line being exposed.

The address generator consists of an 11 bit counter driven

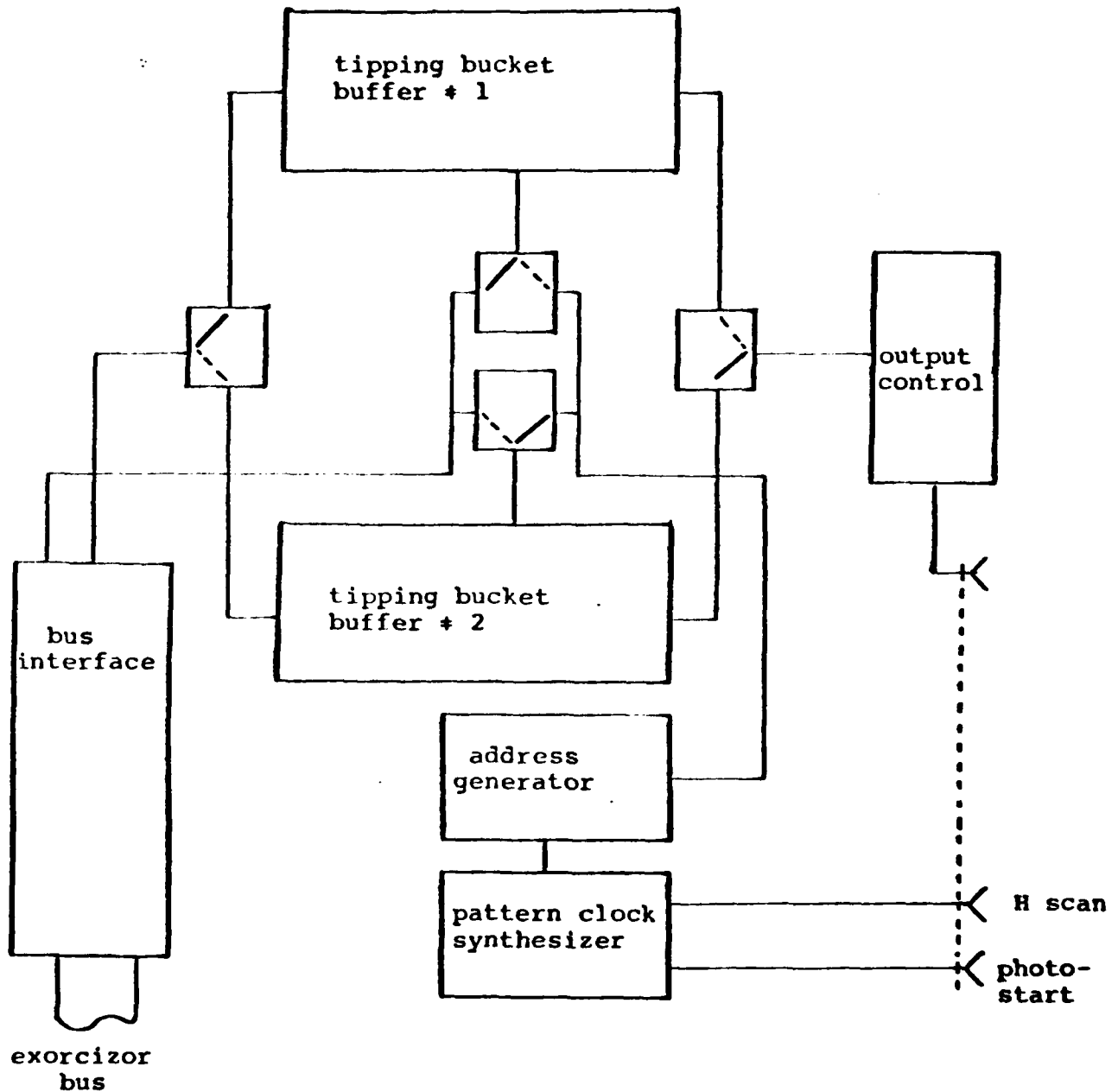


Figure 5. Interface board block diagram.

by the pattern clock signal from the timing synthesizer. The pattern clock is added with the output of timer two of the 6840 which forms the left hand margin of the image space. The first three bits of the address generator select each of the eight bits of each byte of the buffer, while the last eight bits of the address generator select the byte address of sequential bytes in the buffer. Thus the output of the buffer connected to the address generator consists of a serial stream starting with bit 0 of byte 0 continuing through to bit 7 of byte 255. This serial output is then fed to a level shifter on the panel driver board which provides the signal to the beam blanking device. At the end of the current scan line, the buffer previously connected to the processor bus, is then switched to the address generator to provide the new line of pattern data, while the buffer previously connected to the address generator is switched to the processor bus to be filled with the next line of pattern data. Figure 6, is a timing diagram showing the signals during each horizontal scan line. The chief virtue of the tipping bucket structure is that the processor is freed from the overhead of actually clocking data out to the SEM at the relatively slow pattern rate. In each horizontal scan period of approximately 40 milliseconds, the processor overhead is only about 5 milliseconds, which is time required to fill the buffer with the next line of pattern data. Thus in applications which require more elaborate pattern handling than the simple patterns necessary in Schottky diodes, considerable processor time is available.

A panel driver board is located on the front panel of the μ E-Beam. This board, driven by the B-section of the 6821 PIA on the interface board, contains the lamp drivers, and switch drivers for the two panel switches and three LED on the panel. All operator interaction with the μ E-Beam is through these switches and indicators. In addition the panel driver board contains the level shifter from the data output to the beam blanking device. Complete logic diagrams for the interface board are given in Appendix A.

2.5 μ E-Beam Software.

2.5.1 Overview and Design Philosophy.

The μ E-Beam operating software is a compact group of programs (less than one thousand bytes exclusive of pattern data) developed with the following design philosophy: First the system should be as flexible as possible especially in allowing for future performance growth; second, patterns should be readily changable. This is accomplished in the present version by separating the operating software from the pattern software into two separate PROMS. Third, operator interaction must be minimized to permit rapid automatic

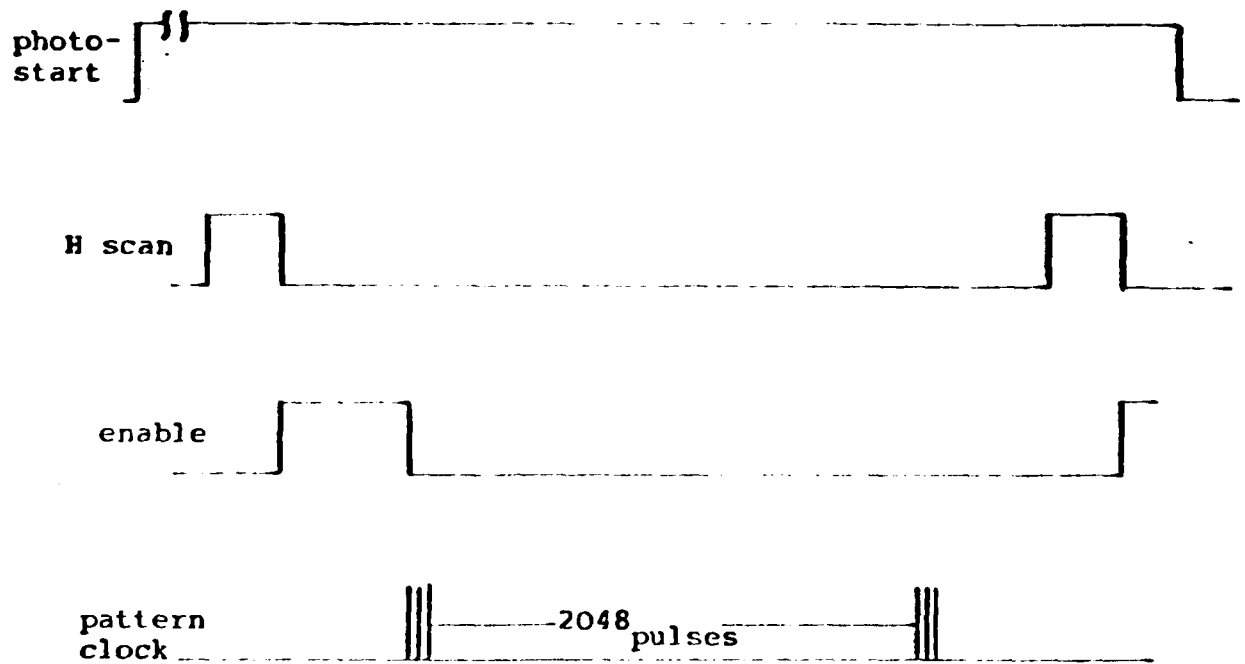


Figure 6. Timing Diagram Exposure Cycle.

operation of the electron beam exposure process. And finally the entire system should be interrupt driven to handle interaction with a variety of randomly occurring real time input and output requirements. For convenience during development and debug stages, the μ E-Beam software works in conjunction with a slightly modified version of Motorola's MICROBUG monotor program. The modification is a change to the power up/reset vector to allow a test of the serial communication port on the 68MM01A processor board. If a VDU is connected as indicated by CTS input being logically true, then program control is passed to MICROBUG for testing and debugging. If no VDU is sensed, then program control passes to the μ E-Beam software.

A simplified flow chart of the μ E-Beam system is shown in Figure 7. On power-up the various programmable peripherals are initialized and the program then waits for an interrupt to occur. On interrupt, devices are polled, the interrupting device serviced and on return the pattern program is checked to see if a new line of pattern data is to be loaded into the tipping bucket buffer. The program then waits for the next interrupt. For purposes of compatibility with MICROBUG, all interrupt vectors and stack pointers are set as expected by MICROBUG. Figure 8 shows a system memory map.

In the following sections the various modules of the software are discussed separately. All software was developed on a Motorola Exorcizer system and extensive use was made of the Relocatable Macro Assembler and Linking Loader utilities in the course of this program. A complete listing of the μ E-Beam software is given in Appendix B.

2.5.2. Initialization Module.

The initialization module is entered on powerup and immediately sets the interrupt mask to prevent any interrupts during initialization. The stack pointer and interrupt vectors are set, several counters used in later stages are initialized and the PIA (Programmable Interface Adapter, MC6821) and PTM (Programmable Timer Module MC6840) are configured as follows:

PIA: Port A, all lines set to output
CA1, input positive edge sensed
CA2, output set to zero

Port B, lines 0-2 inputs
lines 3-7 outputs
CB1, input, negative edge sensed
CB2, input, negative edge sensed

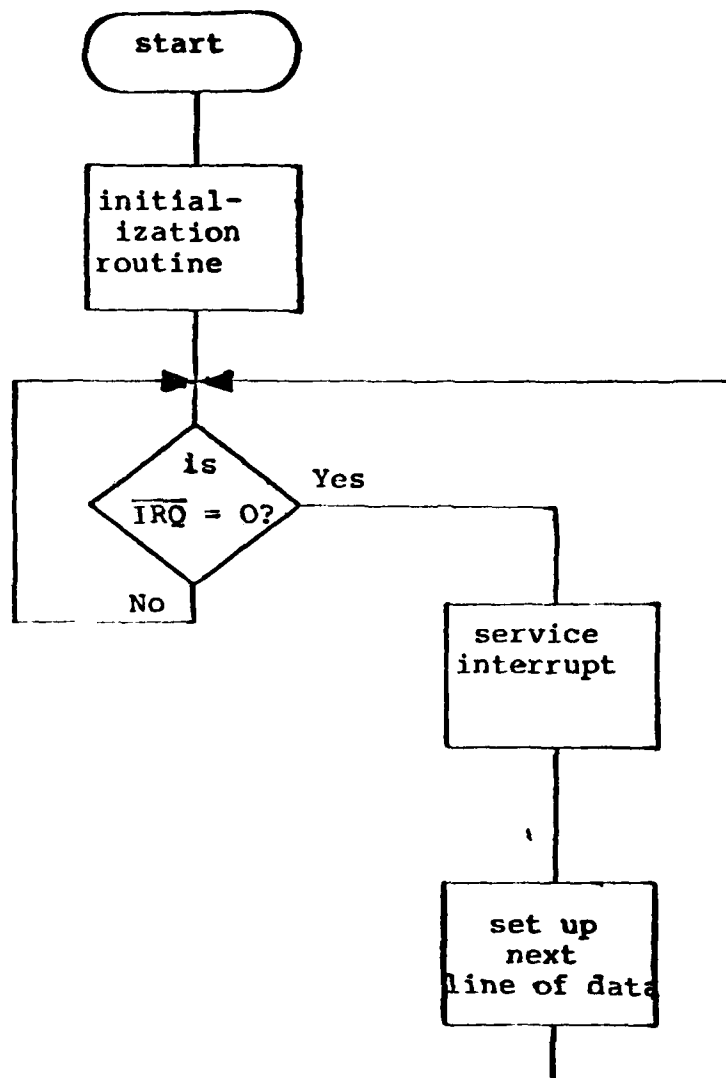


Figure 7. Overall flow chart.

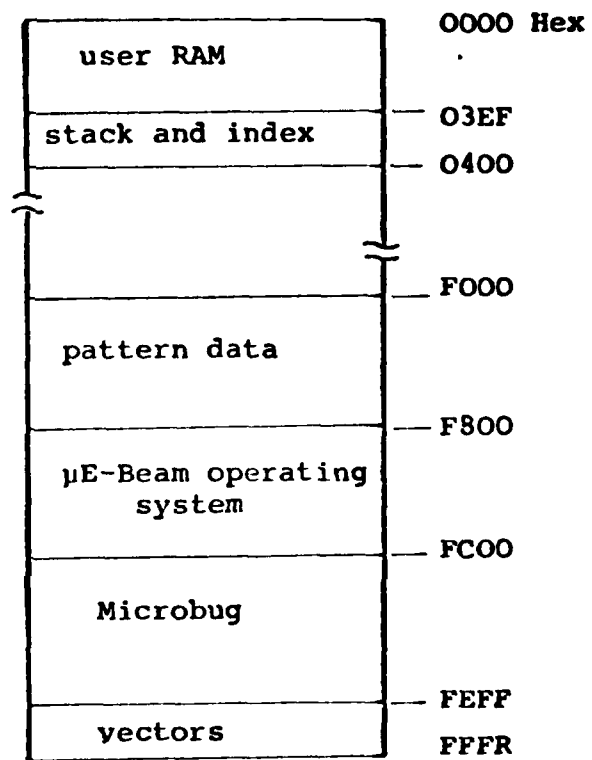


Figure 8. Memory Map.

PTM: Timer 1: external clock, pulse width comparison mode, interrupt generated if gate senses positive edge before timeout. Sixteen bit counting mode is selected. Initial value in data register is 6400 decimal.

Timer 2: external clock, oneshot, sixteen bit counting modes are selected, no data is entered; interrupts are disabled.

Timer 3: external clock and continuous counting modes are selected. Interrupts are disabled. Data is set to 225 decimal.

On completion of the initialization program, control is passed to the Background routine.

2.5.3. Background Module.

In the idle period after initialization and when not servicing interrupts, the program returns to the background program. On entering from initialization, the interrupt mask is cleared and a wait state is entered awaiting interrupts. On completion of interrupt service, the pattern program is checked to see if a new line of pattern data is to be loaded into the tipping bucket buffer. After the pattern routine has been checked, the processor again reverts to its waiting state until the next interrupt occurs.

2.5.4. Interrupt Handling Routines.

Interrupts to the μ E-Beam software arise from three sources: The panel switches, signals from the electron microscope indicating horizontal scan lines or start of exposure sequence, and from the programmable timer. These are handled

by two interrupt service modules. The first module contains the polling and service routines for all interrupt conditions except the synchronisation process at the start of each exposure cycle. The synchronisation is handled by a separate module.

A flow chart of the interrupt handling process is shown in Figure 9. On entering the interrupt service routine the front panel "stop" switch is checked, if this switch is closed, the entire execution is aborted and the program reverts to its wait state. Next the front panel "start" switch is checked, if this switch is pushed the NOT READY light is lit and further closures of this switch are ignored. When the NOT READY light is set on, the control register of Timer 1 is set to enable interrupts from Timer 1 and the synchronisation process begins. After the synchronisation process is started Timer 3 which counts horizontal scan lines is checked. If an interrupt occurs from Timer 3 indicating the end of the top margin region has been reached and synchronisation is not indicated by the READY light being lit, then execution is abandoned. In this manner synchronisation is assured before any pattern data is output to the SEM.

The synchronisation process is carried out by adjusting the programmable divider so that 3200 pattern clock pulses occur between the falling edge of one horizontal blanking pulse and the rising edge of the next horizontal blanking pulse. This is accomplished by presetting Timer 1 to 6400 and operating it in the pulse width comparison mode using the output of the synthesizer as the clock for Timer 1. An interrupt is generated on the next rising edge of a horizontal blanking pulse; at that time the residue in the timer is read by the processor. If the residue is equal to 3200, then the pattern clock is set to the right frequency. If the residue is less than 3200 the pattern clock is too fast and vice versa. From this process the divider ratio to the programmable divider is adjusted up or down to bring the residue to 3200. In practise, this process takes several horizontal scan lines, as successive corrections are made to the divider ratio. As the residue nears 3200, the residue is averaged over 4 horizontal scan periods to increase sensitivity and smaller corrections are made.

Once synchronisation is achieved, Timer 2 which functions in a monostable mode is loaded with a value of 576 which is one half the difference between the horizontal scan line width of 3200 and the active pattern line width of 2048. Timer 2 is gated by the falling edge of the horizontal blanking signal and thus its output forms a delay signal to make the left hand margin of the pattern space. On exiting the synchronisation routine the NOT READY light is turned off and the READY light is turned on, enabling transition to the portion of operation cycle in which pattern data is output to the SEM.

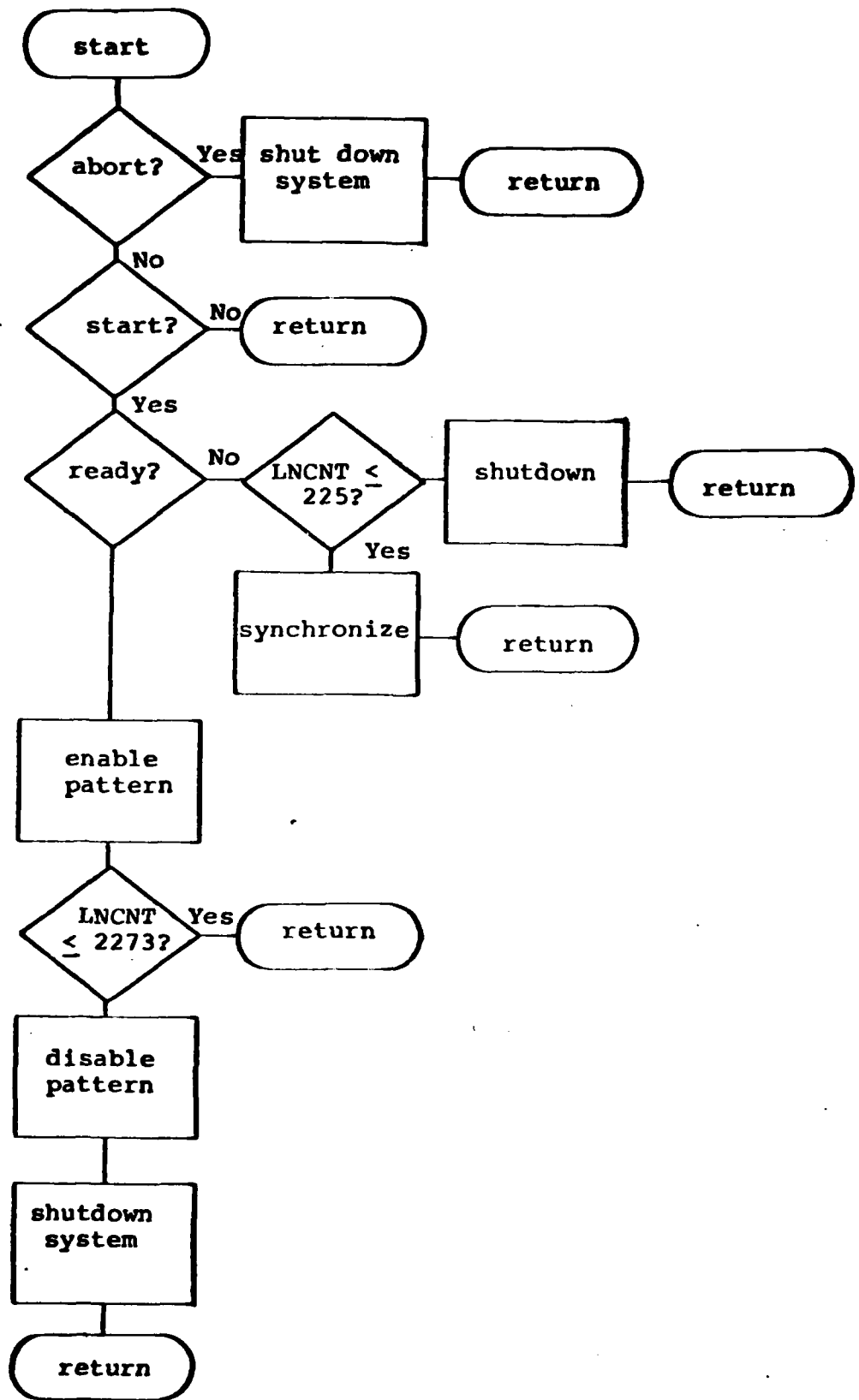


Figure 9. Flow chart for Interrupt service.

Following synchronisation Timer 1 is disabled and further interrupts from the horizontal blanking signal are ignored until an interrupt from Timer 3 is received indicating the end of the top margin space. At this time Timer 2 is enabled, and Timer 3 is loaded with 2048 (800 hex), the PATTERN light on the panel is lit, and the first line of pattern data is loaded into the tipping bucket buffer. Subsequent horizontal blanking signals initiate the following sequence of events: Timer 2 (operating in the one-shot mode) is triggered to form the left side margin; when Timer 2 times out, the pattern clock is enabled and serial pattern data is sent to the Beam Blanking Device. Once the data transfer is initiated, the program causes the next line of data to be loaded into the tipping bucket buffer. Timer 3 is decremented by one count and program control is passed out of the interrupt service modules to the Pattern program which is discussed separately below.

The above sequence of events is repeated 2048 times until Timer 3 reaches zero. At this time an interrupt is generated by Timer 3 indicating the end of the pattern region. When the pattern is complete, further data output is halted and the remaining 225 horizontal lines are counted, until the frame is complete. Upon completion of the frame, all execution is halted and the program returns to Background to await the next closure of the START switch to initiate the next exposure.

2.5.5 Pattern Module.

The program which controls the selection of pattern data loaded into the tipping bucket buffer is located in a separate PROM from the rest of the μ E-beam operating system. This allows simple change of pattern without changing the operating system PROM.

Although exact operation of the PATTERN program varies from pattern to pattern, the general process is basically the same. On return from interrupt servicing a variable named LNCNT is checked. LNCNT is compared with a list of values used to define horizontal boundaries in the exposed image. Depending on the value, a pointer to the appropriate line of pattern data is set into a location named SRCPNT; once SRCPNT is set to the value for next data line, program control returns to Background and waits for the next interrupt. SRCPNT is used as a pointer to the top of the data line and at the next horizontal blanking interrupt the 256 byte block pointed to by SRCPNT is loaded into the Tipping Bucket Buffer.

Utilizing only the decoded ROM address space on the 68MM01A board approximately 2048 (decimal) bytes are available for pattern data while using MICROBUG. If MICROBUG is not used an additional 1024 (decimal) bytes of address space are available. In a practical sense this limits pattern complexity

to those capable of being described in less than 7 lines of pattern with MICROBUG resident and less than 10 to 11 lines without MICROBUG. More complex patterns require either additional ROM space on another board or a tape based system, both of which are within the capabilities of the present hardware.

3.0 Diode Fabrication.

Schottky barrier diodes are currently being fabricated utilizing the μ E-Beam lithography system described above. In the following sections the diode fabrication process employed as well as details of the resist are described.

3.1 Electron Beam Resist.

The basis of any lithographic technique for semiconductor production, either photolithography or electron beam lithography, is that of applying a thin layer of a material sensitive to the exposing wavelength over the semiconductor surface. This material is not attacked by later processing steps such as etching, and thus protects the semiconductor. This sensitive material, known as resist, by its photo or electron beam sensitivity allows a pattern to be formed in it. The exposing process alters the solubility of the resist, thus allowing "development" of the exposed image by washing the exposed resist in the appropriate solvent. Electron beam resists (as photoresists) are classed as negative if the exposure decreases solubility of the resist in its developer and positive if the exposing process increases solubility in the developer. Although in general the radiation chemistry of resists is quite complex, negative resists function by forming cross links in the polymer exposed to radiation, while positive resists function as a result of radiation induced chain scission of the relatively weak bonds making up the polymer. Both positive and negative electron resists are available and for this application a positive resist was chosen. For the diode fabrication process only a relatively small portion of the resist surface area is actually to be removed to allow the semiconductor surface to be etched, thus a positive resist (one in which the resist to be removed is exposed to the electron beam) has the important advantage of allowing a much smaller total electron dose to be used, minimizing the possibility of semiconductor damage by the electron beam. In addition positive resists, by their polymeric structure allow somewhat finer resolution than negative resists.

The above explanation of resist operation is adequate for understanding the gross effects of electron beam - resist interaction, however several important second order effects need to be mentioned to more fully grasp the functional

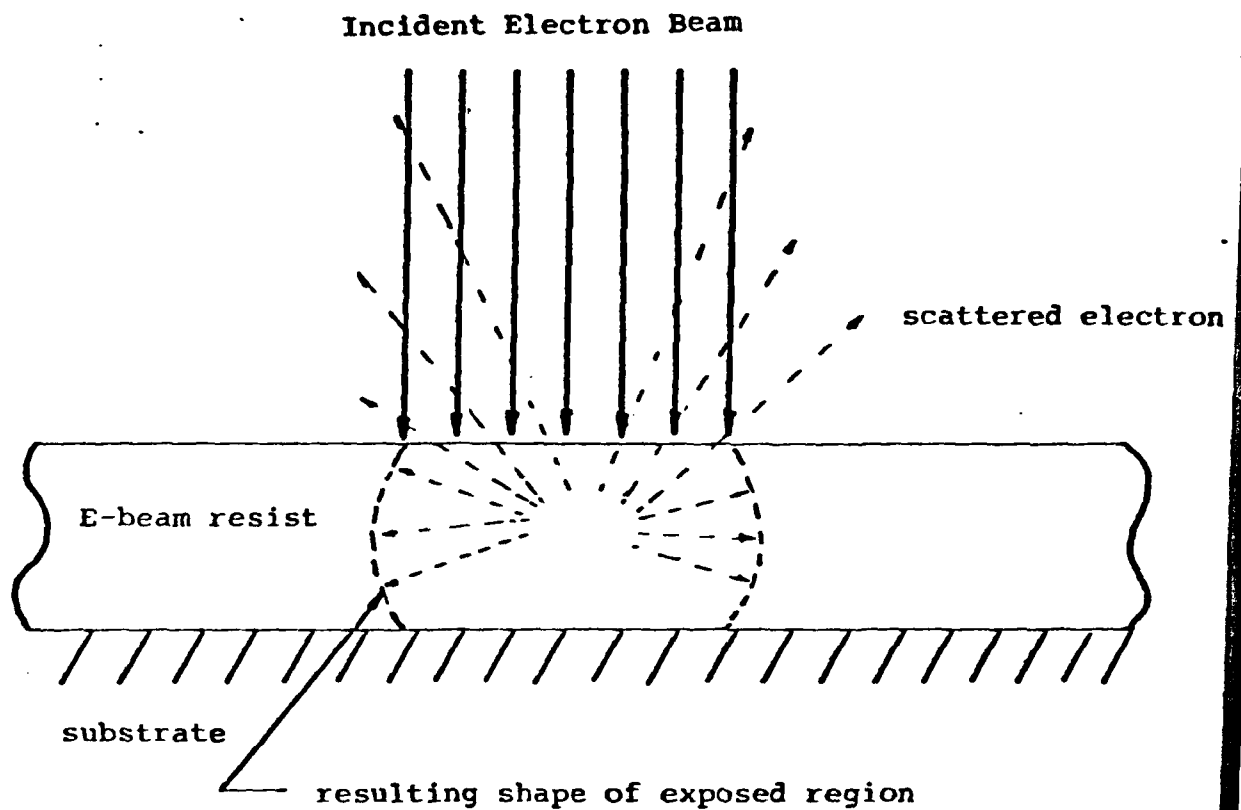


Figure 10. Effect of scattering by resist.

limitations in electron beam lithography. The exposure of the resist is dependent upon the total electron dosage received per unit area. The dosage has units of charge/area as is defined by:

$$D = \frac{It}{A} \quad \dots (1)$$

in which

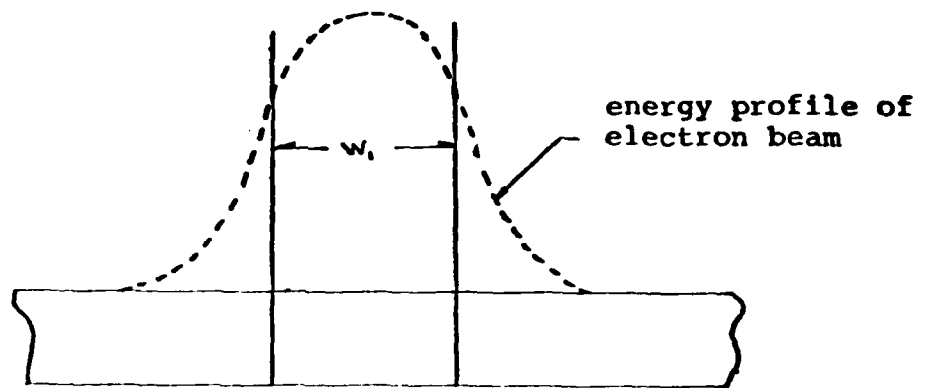
D = dosage in coulombs/cm²

I = current in amperes of the electron beam

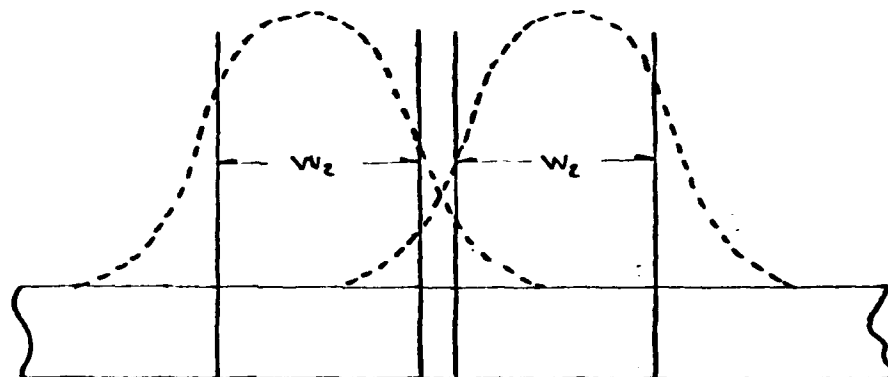
t = dwell time in seconds for each
resolution cell

A = area in cm² of electron beam

The dosage necessary to completely expose an area of resist is a function of the resist chemistry and is known as the sensitivity of the resist. For an electron beam lithography system to be useful the total exposure time should be minimized. From equation (1) above this would imply an increase in beam current as t is reduced to maintain a constant dosage. Beam current can only be increased by either increasing the beam area (allowing more total electrons to hit the resist) which would increase the minimum feature size producible, or by increasing the energy in each incident electron, that is by increasing the accelerating potential in the electron column. As electron energy is increased the first of the secondary effects become noticable. Energy in the incident electrons is absorbed by inducing scission of the polymer bonds, but also due to the non-zero scattering cross-section some of the electrons are scattered in the resist. If the energy in the incident beam is sufficient, some of the scattered electrons will have sufficient energy to also cause scission of resist bonds. The effects of this are the exposure of a larger area than expected due simply to beam sizes and the undercutting of pattern features as shown in Figure 10. For a given resist and minimum feature size (beam diameter) an optimum beam energy exists for minimum exposure time. Several analytic studies have treated this problem^{2,3} however for a particular fabrication process it's more easily determined empirically. The next second order effect which alters the exposure process is the result of the approximately gaussian shape of the incident electron beam. This effect known as the proximity effect is illustrated in Figure 11 (a). As is shown, the concept of a resolution cell is based on a rectangular approximation of the beam shape. As long as areas exposed to the beam are relatively widely spaced, the proximity



a) Exposure of isolated region



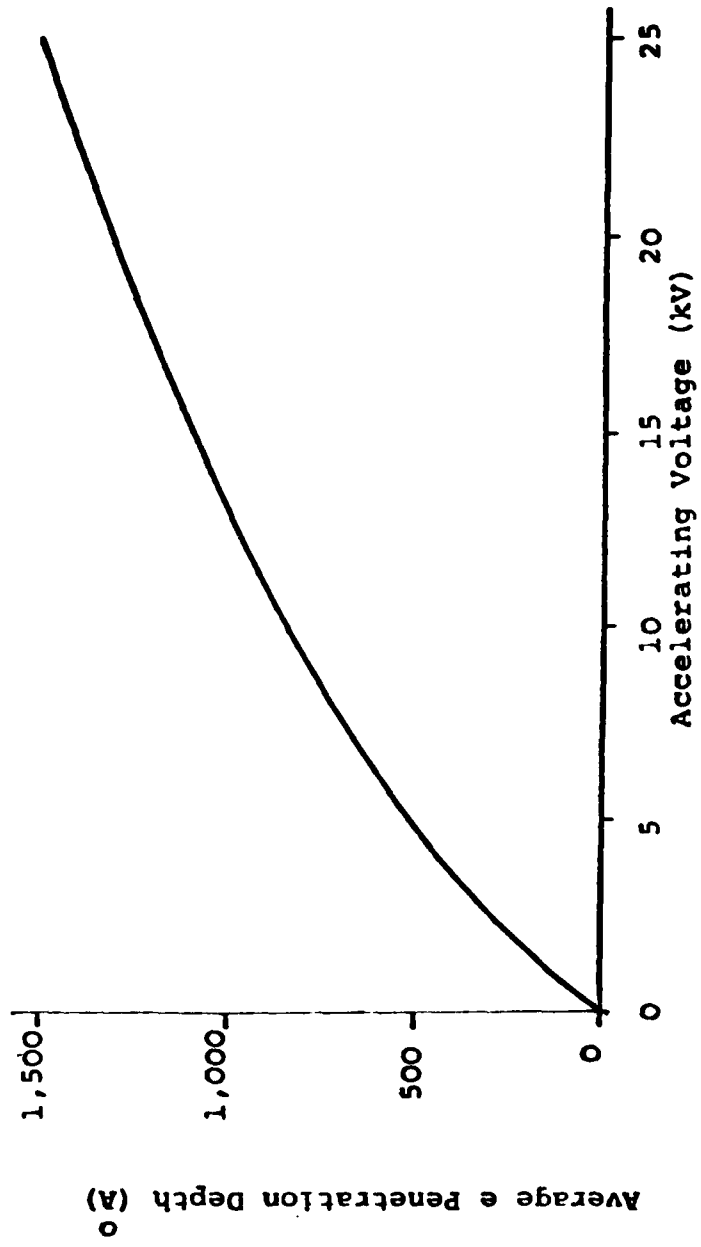
b) Proximity effect: $w_2 > w_1$

Figure 11. Proximity effect.

effect is not noticeable since the spill over due to non-rectangular beam shape is not significant. However as features become more closely spaced, as in Figure 11 (b) the area between the two exposed regions receives an appreciable electron dosage from the skirts of the gaussian beam in the two areas actually exposed. This effect causes a widening of the exposed areas and a resultant narrowing of the unexposed area. The process is also interrelated with the scattering process described above since electrons scattered from the resist surface effectively broadened the skirts of the incident beam. A Monte Carlo method analysis of this effect was reported by Phang et al⁴ and showed a fairly sharp boundary of the effect for spacings less than approximately 1.0 micrometers for nominal beam diameters in the vicinity of 0.1 to 0.2 micrometers. In usual practise, a proximity correction algorithm is applied once the final device geometry is specified. This is normally an empirical reduction in width of an exposed area based on its distance from the closest exposed region. For the work on diode shapes, proximity correction is not significant since the features are generally widely spaced.

A third second order effect is the effect of surface charging. If the electron beam is incident on a dielectric with sufficiently low conductivity, no currents will flow and the incident electrons will remain bound where incident on the surface. This charge accumulation causes an electric field which repels further electrons thus limiting the total dosage available to cause exposure. Since the usual electron microscopy technique of coating the surface with a thin (100Å) film of a conductor such as gold would prohibit exposure of the resist, the only alternative is to select a resist with sufficiently good conductivity to eliminate surface charging. This, happily, is the case with many resists. The fourth effect which must be considered in deciding upon electron beam exposure parameters is the effect of the incident beam on the substrate (semiconductor). Schottky barrier mixer diodes are formed by opening windows in a SiO₂ layer over epitaxial Gallium Arsenide. The results of a study by Hale and Brown⁵ of the penetration of SiO₂ by electrons of varying energy is shown in Figure 12. Thus by limiting electron accelerating potential in relation to SiO₂ thickness, damage to the epitaxial Gallium Arsenide layer can be eliminated.

The resist used in this program has been Shipley AZ-2400 or Shipley AZ-2415. These two resists which differ only in solids content are typical of Diazo type positive working resists. Chemically, they consist of a low molecular weight Novolak resin plus substituted naphthoquinone diazides as the electron active species. The solvent system is a mixture of cellosolve acetate, xylene and n-butyl acetate. Exposure results from decomposition of the diazide components, followed by a rearrangement and hydrolysis⁶. The developer is a simple monobasic aqueous alkine solution. Initially diazo resists were felt to be unsuitable as electron resists although they



Electron Penetration in SiO₂ vs Acceleration Voltage by K.F. Hale and M.H. Brown

Figure 12.

are quite widely used as photoresists in semiconductor manufacture. In 1978 Shaw and Hatzakis re-evaluated the performance of diazo resists for E-beam use and noted excellent performance of the AZ-2400 family. Nearly vertical walls in the exposed resist film and minimum loss of unexposed film thickness during development were measured in their work. Additionally, diazo resists were among the only electron beam resists sufficiently stable to allow plasma etching after image development. An example of the excellent performance of the AZ-2415 resist is shown in Figure 13. This SEM photograph is taken at a magnification of 36000X and shows the developed image of a cross diode anode shape. The width of each limb is approximately 0.5 micron and the length of each limb is 1.4 microns. To heighten contrast for purposes of SEM examination the resist is covered with a evaporated gold layer of approximately 250Å, which produces a slight rounding on resist edges.

3.2 Semiconductor preparation.

The semiconductor samples used in this work have been epitaxial gallium arsenide. Semiconductor preparation follows standard processes developed in the Solid State Electronics Laboratory for production of high performance millimeter and submillimeter Schottky barrier mixer diodes using conventional photolithography and are briefly described here for completeness. The gallium arsenide samples are received from several vendors with the epilayer already formed. The slice is cleaned by successively scrubbing and boiling in trichloroethylene, isopropanol, acetone and xylene. Following a bake at 200°C, a 3000 to 4000 Å layer of SiO₂ is sputtered onto the slice. The slice is scribed and broken into 5 millimeter squares and the chips are then lapped to a thickness of approximately 0.1 millimeter. The back contact is formed by evaporating approximately 250Å of gold followed by electroplating with tin-nickel. The ohmic contact is then alloyed at 350°C for four minutes in an argon atmosphere. The SiO₂ layer is then etched in buffered HF to a thickness of approximately 2000Å. The chip is next cleaned and baked as above prior to resist application.

The resist layer is spun onto the cleaned chip at 3000 RPM for one minute. The resist being applied prior to spinning with a syringe equipped with a 0.2 micron final filter. The resist film is then soft baked at 90°C for 30 minutes. When the baking is complete, the chip is mounted in the exposure fixture shown in Figure 14. This exposure fixture is machined to mount into the goniometer stage of the electron microscope. Following exposure as described below the chip is developed in Shipley AZ-2401 developer diluted 1:3.5 with deionized water using mild agitation by a magnetic stirrer until microscopic examination shows development is complete. The chip is again baked to stabilize the film, etched to open the windows in

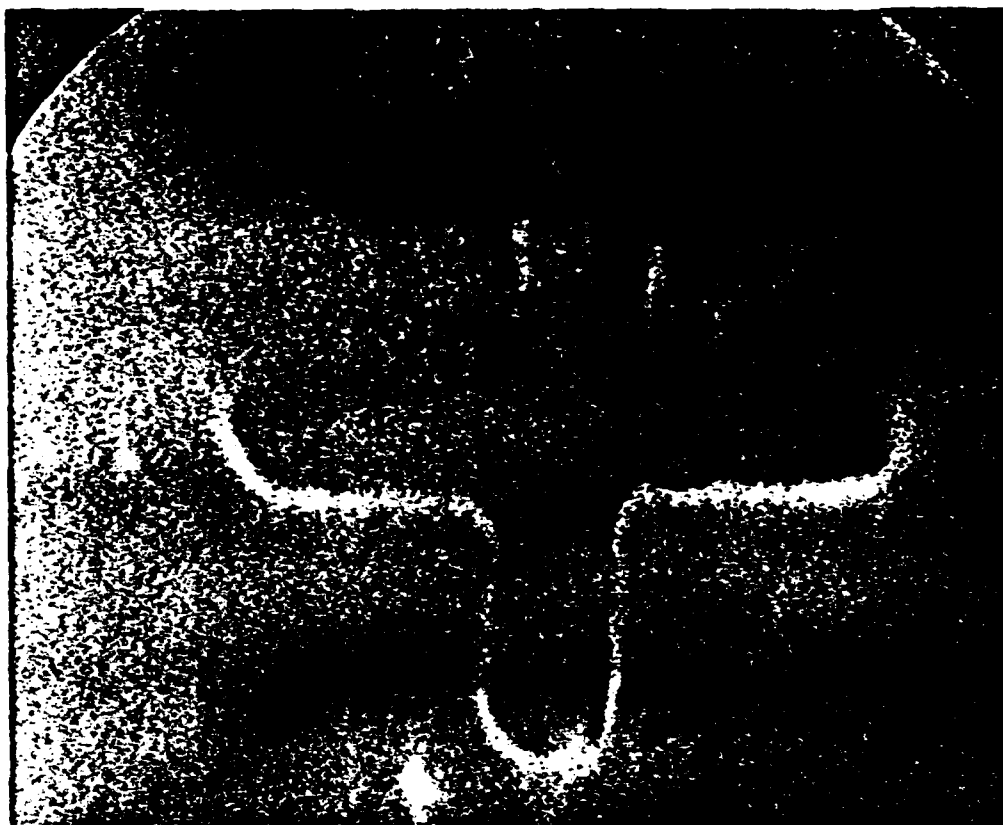


Figure 13.

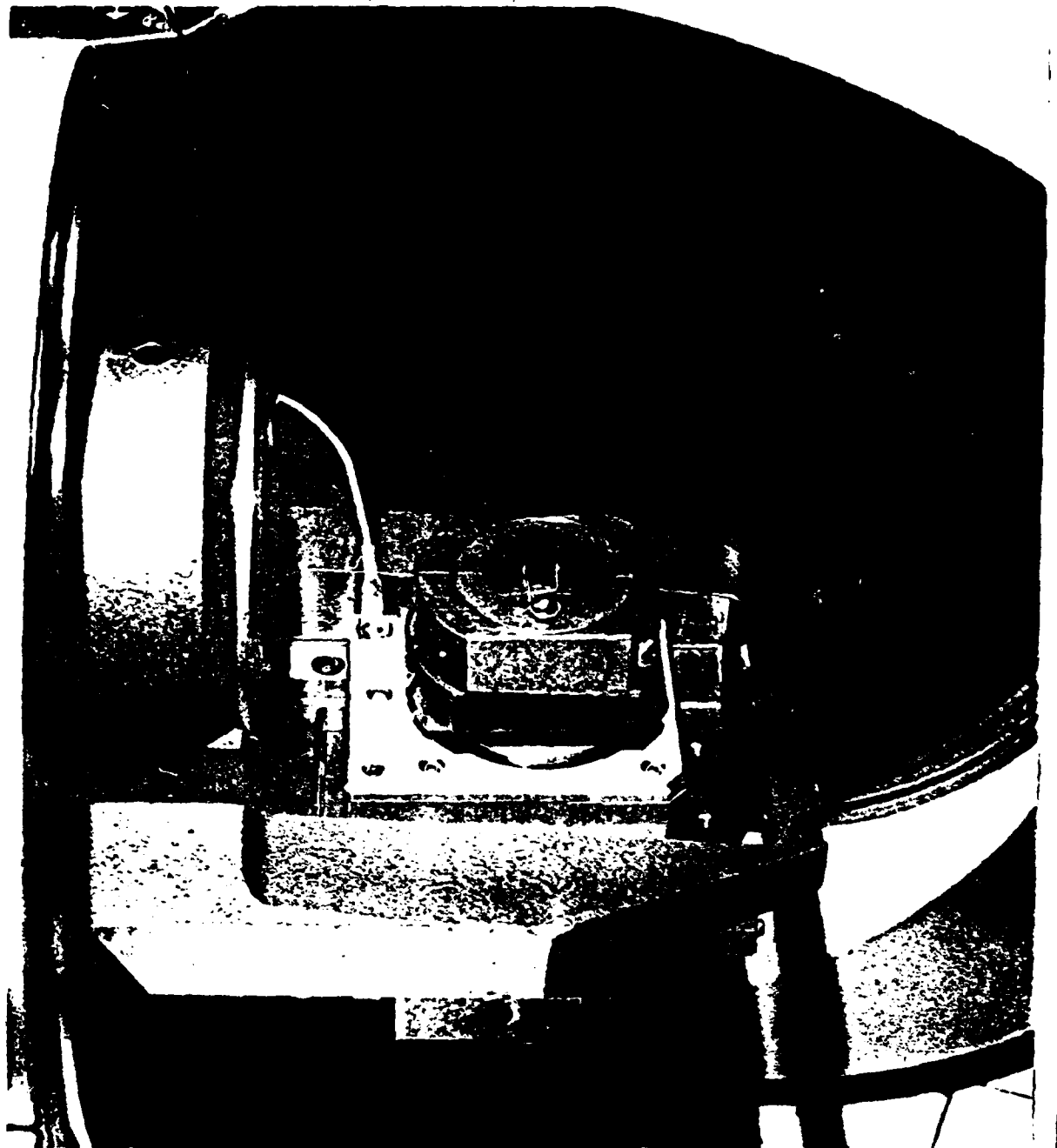


Figure 14.

the SiO₂ and the Schottky barriers are then formed by pulse plating² with platinum. The chip is then finally scribed and broken into 0.250 millimeter squares for testing.

3.3 Exposure.

The chip is mounted in the goniometer stage of the SEM and the beam voltage is set to the selected value. The SEM is then focussed at a magnification of 4300X on the edge of the chip. After focussing, the magnification is reduced to 430X which yields an exposed area of ~ 205 microns square. The beam current, which is monitored using an electrometer, is then adjusted to the required value for the resist being used. Beam currents usually being in the range of $0.5 - 2.0 \times 10^{-10}$ amperes.

When focus and beam current are adjusted the beam blanking device is set to the external mode which blanks the electron beam until pattern information from the μ E-beam is received. The chip is next positioned using the X-Y adjustment on the SEM stage to the coordinates for the first exposure. The exposure is made and the chip is then adjusted to the next coordinate where the next exposure is made. This step and repeat process is continued until the desired number of patterns is put down. At intervals during the step and repeat process, full raster scans are put in place of pattern scans. These are used during development and etching for easier monitoring of these processes and also is used to monitor beam current during exposure.

In the entire diode production process a dummy chip of low grade gallium arsenide is processed along with the sample chip from the resist coating stages through E-beam exposure and development. This chip is used to establish development times for the sample chip and as a general monitor of all processing steps.

4.0 Work planned for next period.

In the next year efforts will be made to refine the diode production process. In particular problems associated with sensitivity of the unexposed resist film to plasma processing will be treated. Several diode geometries will be fabricated and their results compared with both DC and RF tests. A comparison between circular and complex diode shapes fabricated on the same material will be performed. A pattern which will include both circular and complex Schottky barrier geometries on a single 200 micron square chip is easily within the capabilities of the current μ E-beam system configuration. This pattern will facilitate accurate RF measurements since the

chip will not need to be changed, to evaluate each shape. The change can be effected by simply contacting either a complex (cross shaped) diode or a circular diode. In addition, this process should minimize the possibility of variation in material properties clouding results.

5.0 Papers presented:

- (1) A paper entitled "Electron Beam Lithography using a Scanning Electron Microscope" was presented at the Irish Society of Electron Microscopy Annual Meeting, Limerick, Ireland on 26 April 1979.
- (2) A paper entitled "Electron Beam Fabrication of Submillimeter Schottky Barrier Diodes" has been accepted for presentation at the IEEE Submillimeter Meeting, Miami, Florida, 10-15 December 1979.
- (3) A paper entitled "Finite Element Analysis of Schottky Barrier Diodes" has been accepted for presentation also at the IEEE Submillimeter Meeting.

6.0 Acknowledgements.

The continued support and assistance of Dr. W. Reville and Ms. Miriam Cotter of the Electron Microscope Unit, University College, Cork is gratefully acknowledged. Likewise the assistance of and discussions with Mr. R.A. Erridge and Dr. W.M. Kelly of the Solid State Electronics Laboratory, U.C.C. is also gratefully acknowledged.

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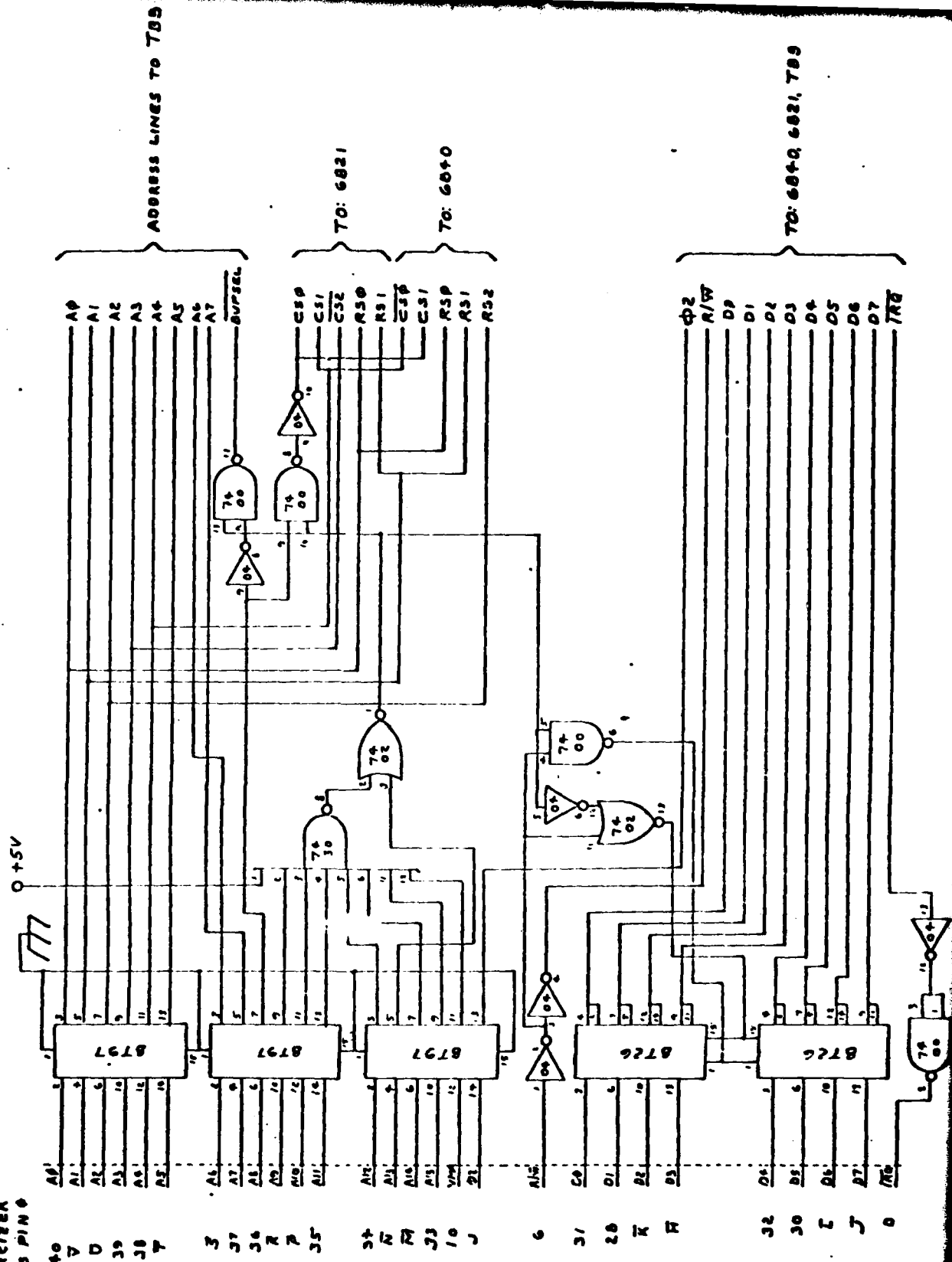
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3. Hawryluk et al, J.Appl.Phys. 46(6):2528, 1969.
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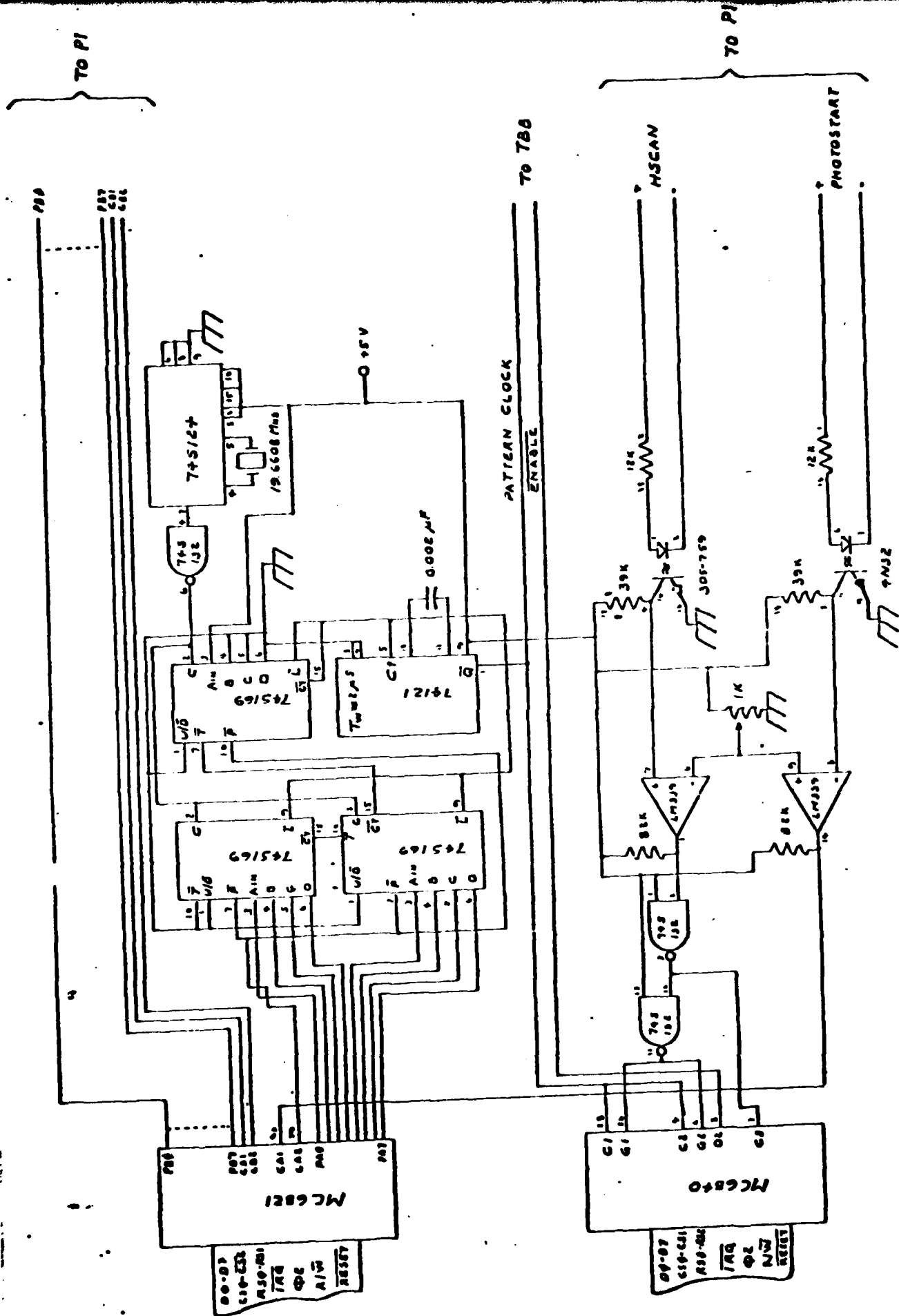
A1

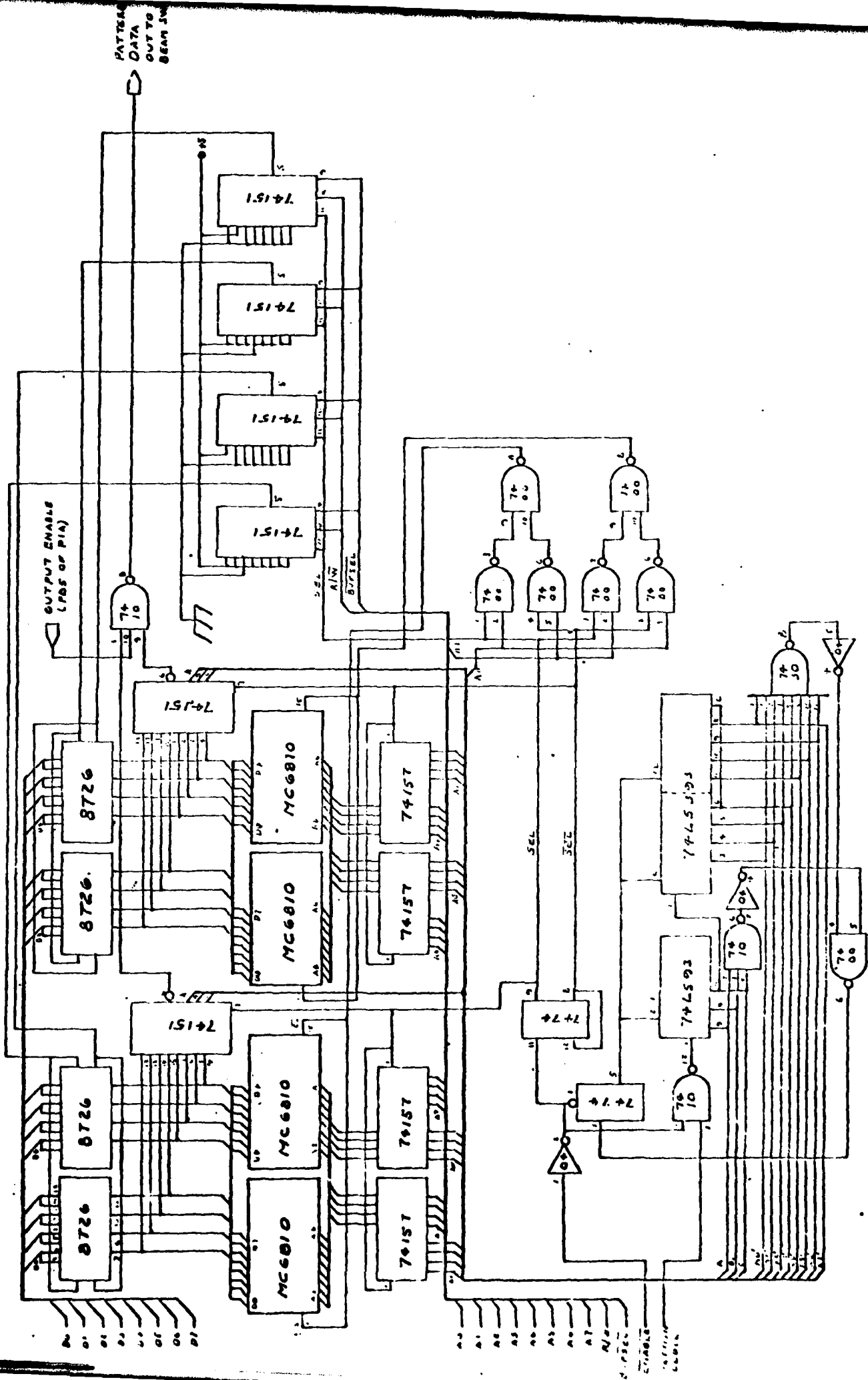
APPENDIX A

Logic diagrams

EXERCIZER
BUS PIN 0







B1

APPENDIX B

Software listing.

```

00002          TTL      INITIALIZATION MODULE
00003          OPT      REL
00004          IDNT     INI V1.04
00005          NAM      INI104
00006          * DATE: 9 MARCH 1979
00007          *
00008          *!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
00009          *
00010          * REV 1.04 CHANGES THE SYSTEM TO COMPENSATE
00011          * FOR RECTANGULAR SEM SCAN RASTER GEOMETRY. A
00012          * WIDTH TO HEIGHT RATIO OF 1.28:1 IS ASSUMED
00013          *
00014          *!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
00015          *-----
00016          *
00017          *THIS MODULE INITIALIZES THE PTM AND PIA. THE PTM
00018          *IS SETUP INITIALLY AS FOLLOWS:
00019          * TIMER1:  EXT CLOCK, PW COMPARISON, INTERRUPT
00020          *             IF GATE GOES POSITIVE BEFORE TIMEOUT.
00021          *             OUTPUT IS ENABLED, BUT NOT USED.
00022          *             SIXTEEN BIT COUNTING MODE.
00023          *             INITIAL DATA VALUE IS SET TO $1388
00024          *             ($5000) INTERRUPT IS ENABLED, DUMMY
00025          *             REGISTER FOR TCR1 IS TIM1. BIT0 OF
00026          *             TCR1 IS SET TO ZERO TO HOLD ALL TIMER
00027          *             PRESET.
00028          *
00029          *
00030          * TIMER2:  EXT CLOCK, ONESHOT MODE, NO INTERRUPTS,
00031          *             16 BIT COUNTING MODE, OUTPUT IS EN-
00032          *             ABLED; NO DATA IS ENTERED,
00033          *
00034          * TIMER3:  EXT CLOCK, CONTINUOUS COUNTING, INTER-
00035          *             RUPT IS DISABLED, NO OUTPUT
00036          *
00037          *
00038          * PIA SET UP IS AS FOLLOWS:
00039          * PIA A PORT: ALL OUTPUTS, DATA=DIVRAT
00040          * PIA A CR:  CA1 INPUT, CA2 OUTPUT, SET TO ZERO
00041          *             INTERRUPT ON POSITIVE EDGE OF CA1,
00042          *             IS ENABLED.
00043          * PIA B PORT: 0-2 INPUTS
00044          *             3-7 OUTPUTS
00045          *             CB1 INPUT INTRPT ON NEG EDGE, ENABLE
00046          *             CB2 INPUT INTRPT ON NEG EDGE ENABLE
00047          *
00048          *
00049          * THIS MODULE ALSO CONTAINS:
00050          * THE PATCH TO MICROBUG TO TEST IF AN EXTERNAL
00051          * DEVICE (VDU) IS CONNECTED TO THE ACIA PORT. IF A
00052          * EXTERNAL DEVICE IS PRESENT EXECUTION OF MICRO-
00053          * BUG STARTS WHEN POWERUP/RESET IS ACTIVATED, OTH
00054          * WISE THE APPLICATION PROGRAM WHICH BEGINS AT
00055          * $F800 IS EXECUTED.
00056          *
00057          *-----
00058          XREF      TIM1, TIM2, TIM3, BCKGND, INTRPT, SUM, CN
00059          XREF      SRCPNT, PATDAT

```



```

00118P 0035 CE 0423 A      LDX    #$0423
00119P 0038 FF DF94 A      STX     TREG4    TIMER2 DATA
00120P 003B CE 00E2 A      LDX     #$00E2
00121P 003E FF DF96 A      STX     TREG6    TIMER3 DATA
00122
00123      *PIA SET UP
00124      *
00125P 0041 86 00 A      LDAA    #$00
00126P 0043 B7 DF89 A      STAA    PREG1
00127P 0046 86 FF A      LDAA    #$FF
00128P 0048 B7 DF88 A      STAA    PREG0
00129P 004B 86 3F A      LDAA    #$3F
00130P 004D B7 DF89 A      STAA    PREG1
00131P 0050 86 0000 P      LDAA    DIVRAT
00132P 0053 B7 DF88 A      STAA    PREG0    DIVIDER DATA
00133P 0056 86 00 A      LDAA    #$00
00134P 0058 B7 DF88 A      STAA    PREG3
00135P 005B 86 F8 A      LDAA    #$F8
00136P 005D B7 DF8A A      STAA    PREG2
00137P 0060 86 0C A      LDAA    #$0C
00138P 0062 B7 DF8B A      STAA    PREG3
00139
00140P 0065 7F 0000 A      CLR     SUM      ZERO SUM REGISTER
00141P 0068 86 03 A      LDAA    #$03
00142P 006A B7 0000 A      STAA    CNTR1    INITIALIZE CNTR1
00143
00144P 006D CE 00FF A      LDX     #PATDAT+$FF
00145P 0070 FF 0000 A      STX     SRCPNT    SETUP DATA POINTER
00146
00147P 0073 CE 0000 A      LDX     #INTRPT
00148P 0076 FF 0380 A      STX     $0380    SETUP INTERRUPT VECTOR
00149
00150P 0079 7E 0000 A      JMP     BCKGND
00151
END
TOTAL ERRORS 00000

```

```

R      BCKGND 00058*00150
R      CNTR1  00058*00142
DP 0000 DIVRAT 00062 00064*00131
P 000F INI0   00094 00101*
DP 0001 INIT  00061 00088*
R      INTRPT 00058*00147
R      PATDAT 00059*00144
D DF88 PREG0  00060 00067*00128 00132
D DF89 PREG1  00060 00068*00126 00130
D DF8A PREG2  00060 00069*00136
D DF8B PREG3  00060 00070*00134 00138
R      SRCPNT 00059*00145
R      SUM    00058*00140
R      TIM1   00058*00105
R      TIM2   00058*00103 00108
R      TIM3   00058*00111
D DF90 TREG0  00060 00073*00106 00112
D DF91 TREG1  00060 00074*00102 00109
D DF92 TREG2  00060 00075*00117
D DF93 TREG3  00061 00076*

```

D DF94 TREG4 00061 00077*00119
D DF95 TREG5 00061 00078*
D DF96 TREG6 00061 00079*00121
D DF97 TREG7 00061 00080*

```

00002          TTL      BACKGROUND PROGRAM MODULE
00003          OPT      REL
00004          IDNT     BCK V1.0
00005          *
00006          *
00007          *-----*
00008          *BACKGROUND PROGRAM CONTAINS THE ROUTINES WHICH
00009          *AWAIT THE INTERRUPT REQUEST AND THEN GO SET
00010          *THE VECTOR NAMED SRCPNT WHICH BLKMOV USES TO
00011          *LOAD THE TIPPING BUCKET BUFFER. THE SUBRTN WHICH
00012          *CONTAINS THE DATA FOR THE IMAGE IS CALLED
00013          *PATTRN
00014          *-----*
00015          *
00016          XREF      SRCPNT, TREG6, TREG7, LNCNT, PATTRN
00017          XDEF      BCKGND
00018          *
00019          *
00020P 0000          PSCT
00021          *
00022P 0000 0E      BCKGND CLI          ENABLE INTRUPTS
00023P 0001 3E      WAI              WAIT HERE FOR INT TO OCCUR
00024P 0002 0F      SEI              DISABLE INTRPT TO LOAD BUF
00025P 0003 FE 0000 A    LDX          TREG6      GET TIMER3 DATA
00026P 0006 FF 0000 A    STX          LNCNT
00027P 0009 BD 0000 A    JSR          PATTRN
00028P 000C 20 F2 0000   BRA          BCKGND
00029          END
TOTAL ERRORS 00000

```

```

DP 0000 BCKGND 00017 00022*00028
R      LNCNT 00016*00026
R      PATTRN 00016*00027
R      SRCPNT 00016*
R      TREG6 00016*00025
R      TREG7 00016*

```

```

00001          TTL      INTERRUPT SERVICE MODULE 2.02
00002          OPT      REL
00003          IDNT     INT 2.02
00004          NAM      INT201
00005          *
00006          * DATE: 9 MARCH 1979
00007          *
00008          XREF     PREG0, PREG1, PREG2, PREG3, TREG0, TREG1
00009          XREF     TREG2, TREG3, TREG4
00010          XREF     TREG5, TREG6, TREG7, SRV3
00011          XREF     DIVRAT
00012          *
00013          *
00014          XDEF     INTRPT, SRV0, SRV2, SRV4, SRV5
00015          XDEF     BLKMOV, BASE1, SUM, PREVAL
00016          XDEF     SRCPNT, TIM1, TIM2, TIM3, LNCNT, STCK
00017          XDEF     CNTR, CNTR1, PWBUF, BUTTON
00018          *
00019P 0000          PSCT
00020          *
00021P 0000          40      A MSK0      FCB      $40
00022P 0001          80      A MSK1      FCB      $80
00023P 0002          80      A MSK2      FCB      $80
00024P 0003          01      A MSK3      FCB      $01
00025P 0004          02      A MSK4      FCB      $02
00026P 0005          04      A MSK5      FCB      $04
00027          *
00028D 0000          DSCT
00029          *
00030D 0000          0001    A TIM1      RMB      1      *DUMMY FOR TIMER1 C/R
00031D 0001          0001    A TIM2      RMB      1
00032D 0002          0001    A TIM3      RMB      1
00033D 0003          0002    A PWBUF     RMB      2
00034D 0005          0002    A SRCPNT    RMB      2
00035D 0007          0002    A LNCNT     RMB      2
00036D 0009          0002    A STCK      RMB      2
00037D 000B          0001    A CNTR      RMB      1
00038D 000C          0002    A SUM       RMB      2
00039D 000E          0002    A PREVAL    RMB      2
00040D 0010          0001    A CNTR1     RMB      1
00041D 0011          0001    A BUTTON    RMB      1
00042          *
00043A 0000          ASCT
00044          DEFF     A BASE1    EQU      $DEFF
00045          *
00046P 0006          PSCT
00047          *
00048P 0006 B6 0000    A INTRPT    LDAA     PREG3      CHECK IF BUTTON PSHED
00049P 0009 16          TAB          SAVE A IN B
00050P 000A B6 0000    A          LDAA     PREG2      GET PIA B DATA
00051P 000D B7 0011    D          STAA     BUTTON
00052P 0010 17          TBA
00053P 0011 B4 0000    P          ANDA     MSK0      IS BUTTON PUSHED?
00054P 0014 27 06 001C BEQ          INT1      NO, GO ON
00055P 0016 BD 005F    P          JSR          SRV0      YES GO SERVICE IT
00056P 0019 24 01 001C BCC          INT1      MUST NOT BE AN ABORT
00057P 001B 3B          RTI
00058P 001C 01          INT1     NOP          HAS HSCAN PULSE COME

```

00059P	001D	B6	0000	A	INT2	LDAA	PREG1	CHECK FOR VSCAN
00060P	0020	B4	0002	P		ANDA	MSK2	IS IT VSCAN?
00061P	0023	27	03	0020		BEQ	INT3	NO, CONTINUE ON YOUR MERRY
00062P	0025	8D	00EF	P		JSR	SRV2	YES GO SERVICE IT
00063P	0028	B6	0000	A	INT3	LDAA	TREG1	NOW CHECK TIMER INTRPTS
00064P	002B	16				TAB		SAVE A IN B
00065P	002C	F5	0002	P		BITB	MSK2	
00066P	002F	27	2D	005E		BEQ	INT6	
00067P	0031	B6	0000	D		LDAA	TIM1	GET TIMER1 STATUS REG
00068P	0034	85	40	A		BITA	#40	TEST TO SEE IF T2 INT ENAB
00069P	0036	27	08	0040		BEQ	INT4	INT ISN'T ENABLED
00070P	0038	F5	0003	P	INT30	BITB	MSK3	IS IT TIMER1?
00071P	003B	27	03	0040		BEQ	INT4	MUST NOT BE
00072P	003D	8D	0000	A		JSR	SRV3	IT IS
00073P	0040	B6	0001	D	INT4	LDAA	TIM2	
00074P	0043	85	40	A		BITA	#40	TEST IF INT IS ENABLED
00075P	0045	27	08	004F		BEQ	INT5	
00076P	0047	F5	0004	P		BITB	MSK4	IS IT TIMER2?
00077P	004A	27	03	004F		BEQ	INT5	NOPE
00078P	004C	8D	0121	P		JSR	SRV4	YES IT IS
00079P	004F	B6	0002	D	INT5	LDAA	TIM3	GET TIMER3 STATUS
00080P	0052	85	40	A		BITA	#40	TEST IF INT IS ENABLED
00081P	0054	27	08	005E		BEQ	INT6	MUST NOT BE
00082P	0056	F5	0005	P		BITB	MSK5	IS TIMER3 INTERRUPTED
00083P	0059	27	03	005E		BEQ	INT6	NOT TIMER3
00084P	005B	8D	0130	P		JSR	SRV5	YES
00085P	005E	3B			INT6	RTI		

```

00087 *-----
00088 *
00089 * SUBROUTINE TO SERVICE THE B SECTION OF THE PIA.
00090 * ROUTINE CHECKS TO SEE WHICH SWITCH IS CLOSED.
00091 * IF THE ABORT SWITCH IS ACTIVATED THE SUBRTN
00092 * RETURNS WITH THE CARRY SET CAUSING A RETURN
00093 * FROM INTERRUPT AND ALL OPERATION REVERTS TO THE
00094 * BACKGROUND MODE AWAITING THE CLOSURE OF THE
00095 * START SWITCH.
00096 *-----
00097 *
00098 *
00099 *
00100 *
00101 *
00102P 005F 37      SRV0   PSHB           SAVE B
00103P 0060 B6 0011 D    LDAA   BUTTON   GET PIA-B DATA
00104P 0063 85 01      A    BITA   #$01   IS IT ABORT TIME?
00105P 0065 27 1B 0082  BEQ     SRV01   NOPE
00106      *ABORT PATH THRU SRV02
00107P 0067 B6 0000 A SRV02 LDAA   PREG1   YES, LETS GET OUT OF HERE
00108P 006A 8A 08      A    ORAA   #$08   TURN ON CA2(STOP PTRN CLK)
00109P 006C B7 0000 A    STAA   PREG1
00110P 006F 86 17      A    LDAA   #$17   TRN OFF PB3, PB6, PB7(RDY/NO
00111P 0071 B7 0000 A    STAA   PREG2
00112P 0074 B6 0001 D    LDAA   TIM2    GET TIMER2 CONDX
00113P 0077 84 7F      A    ANDA   #$7F   TURN OFF BIT7(O/P ENABLE)
00114P 0079 B7 0000 A    STAA   TREG1   PUT IN TIMER2 C/R
00115P 007C B7 0001 D    STAA   TIM2    RETURN TO DUMMY
00116P 007F 7E 00D4 P    JMP     SRV04   EXIT PATH
00117P 0082 B6 0011 D SRV01 LDAA   BUTTON   GET PIA-B WORD
00118P 0085 85 40      A    BITA   #$40   IS IT NOT READY?
00119P 0087 26 48 00D1  BNE     SRV03   YES GO ON
00120P 0089 85 80      A    BITA   #$80   IS IT READY
00121P 008B 26 44 00D1  BNE     SRV03   CONTINUE ON IF READY
00122P 008D 85 02      A    BITA   #$02   NO, IS START PUSHED
00123P 008F 27 43 00D4  BEQ     SRV04   NOT THISTIME, EXIT
00124P 0091 86 01      A    LDAA   #$01   YES
00125P 0093 BA 0001 D    ORAA   TIM2    ACCESS TO TIMER1 C-REG
00126P 0096 B7 0000 A    STAA   TREG1
00127P 0099 B7 0001 D    STAA   TIM2
00128P 009C C6 D9      A    LDAB   #$D9   TIMER1, PW MODE, INT BEFORE
00129P 009E F7 0000 D    STAB   TIM1
00130P 00A1 F7 0000 A    STAB   TREG0   SET UP TIMER1
00131P 00A4 84 FE      A    ANDA   #$FE
00132P 00A6 B7 0001 D    STAA   TIM2
00133P 00A9 B7 0000 A    STAA   TREG1   ACCESS TO TIMER3
00134P 00AC 86 40      A    LDAA   #$40   TIMER3, COUNT, 16 BIT, INT EN
00135P 00AE B7 0000 A    STAA   TREG0
00136P 00B1 B7 0002 D    STAA   TIM3
00137P 00B4 CE 1900 A    LDX     #$1900
00138P 00B7 FF 0000 A    STX     TREG2   TIMER1 DATA
00139P 00BA CE 00E1 A    LDX     #$00E1
00140P 00BD FF 0000 A    STX     TREG6   TIMER3 DATA
00141P 00C0 FF 000E D    STX     PREVAL
00142P 00C3 B6 0000 A    LDAA   DIVRAT   SETUP DIVIDER RATIO
00143P 00C6 B7 0000 A    STAA   PREG0   PUT IN PIA-A
00144P 00C9 B6 0000 A    LDAA   PREG2   GET PIA-B DATA

```

00145P	00CC	86	47	A	LDAA	#\$47	TURN ON NOT READY
00146P	00CE	B7	0000	A	STAA	PREG2	
00147P	00D1	0C			SRV03	CLC	EXIT PATH WITH CARRY CLEAR
00148P	00D2	20	03	00D7	BRA	SRV05	
00149P	00D4	0D			SRV04	SEC	
00150P	00D5	20	00	00D7	BRA	SRV05	EXIT PATH WITH CARRY SET
00151P	00D7	33			SRV05	PULB	
00152P	00D8	39				RTS	
00153					*		
00154					*		

```

00156
00157
00158
00159
00160
00161
00162P 00D9 BF 0009 D BLKMOV STS STCK SAVE STACK PNTR
00163P 00DC 8E DEFF A BLK0 LDS #BASE1 GET DESTN PNTR
00164P 00DF FE 0005 D LDX SRCPNT
00165P 00E2 C6 00 A LDAB #00 SET BYTE CNTR
00166P 00E4 A6 00 A BLK1 LDAA 0,X GET BYTE
00167P 00E6 36 PSHA PUT BYTE IN BUFFER
00168P 00E7 09 DEX DECR SRCPOINTER
00169P 00E8 5C INCB INCR BYTE CNTR
00170P 00E9 26 F9 00E4 BNE BLK1 GO ROUND AGAIN IF NOT DONE
00171P 00EB BE 0009 D LDS STCK RESTORE STACK POINTER
00172P 00EE 39 RTS
00173
00174
00175
00176
00177
00178
00179
00180
00181
00182P 00EF 37 SRV2 PSHB SAVE B IN STACK
00183P 00F0 B6 0000 A LDAA PREG0 DUMMY READ TO CLR IRQ
00184P 00F3 B6 0000 A LDAA PREG2 B WORD OF PIA
00185P 00F6 85 80 A BITA #00 IS READY SET?
00186P 00F8 26 22 011C BNE SRV21 LETS GET OUTTAHERE
00187P 00FA 85 40 A BITA #40 IS NOT READY SET?
00188P 00FC 27 20 011E BEQ SRV22 EXIT TO ABORT
00189P 00FE B6 0001 D LDAA TIM2
00190P 0101 8A 01 A ORAA #01
00191P 0103 B7 0001 D STAA TIM2
00192P 0106 B7 0000 A STAA TREG1 ACCESS TIMER1
00193P 0109 B6 0000 D LDAA TIM1
00194P 010C 84 FE A ANDA #$FE CLEAR BIT0
00195P 010E B7 0000 D STAA TIM1
00196P 0111 B7 0000 A STAA TREG0 ENABLE ALL TIMERS
00197P 0114 B6 0000 A LDAA PREG1
00198P 0117 84 F7 A ANDA #$F7 CLR BIT3 CR-A
00199P 0119 B7 0000 A STAA PREG1
00200P 011C 33 SRV21 PULB RESTORE B
00201P 011D 39 RTS
00202P 011E 7E 0067 P SRV22 JMP SRV02 ABORT, ABORT, ABORT!!!!
00203

```

```

00205
00206
00207
00208
00209
00210
00211
00212
00213
00214
00215P 0121 37
00216P 0122 B6 0000 A
00217P 0125 B6 0000 A
00218P 0128 B6 0000 A
00219P 0128 B0 00D9 P
00220P 012E 33
00221P 012F 39
00222
00223
00224
00225
00226
00227
00228
00229
00230
00231
00232P 0130 37
00233P 0131 B6 0000 A
00234P 0134 85 80 A
00235P 0136 27 70 01A8
00236P 0138 B6 000E D
00237P 013B F6 000F D
00238P 013E 40
00239P 013F 26 20 0161
00240P 0141 C1 E1 A
00241P 0143 26 1C 0161
00242P 0145 86 E1 A
00243P 0147 B7 0000 A
00244P 014A B7 0001 D
00245P 014D B6 0000 A
00246P 0150 8A 28 A
00247P 0152 B7 0000 A
00248P 0155 CE 0800 A
00249P 0158 FF 0000 A
00250P 015B FF 000E D
00251P 015E 7E 01A6 P
00252P 0161 81 08 A
00253P 0163 26 2A 018F
00254P 0165 5D
00255P 0166 26 27 018F
00256P 0168 B6 0000 A
00257P 016B 8A 08 A
00258P 016D B7 0000 A
00259P 0170 B6 0001 D
00260P 0173 84 7F A
00261P 0175 B7 0001 D
00262P 0178 B7 0000 A

*-----*
*SRV4: SRV4 IS THE SUBROUTINE SERVICING INTERRUPT
* ARISING FROM TIMER2. THE INTERRUPT FROM TIMER2
* TO CAUSE THE TIPPING BUCKET BUFFER TO BE FILLED
* FROM MEMORY (PATTRN SUBROUTINE), THE ACTUAL TRA
* DATA IS DONE BY THE SUBROUTINE NAMED BLKMOV
* WHICH LIVES IN SRV1.
*-----*
*
*
*
SRV4  PSHB          SAVE B IN STACK
      LDAA  TREG1
      LDAA  TREG3    TIMER2 MSB
      LDAA  TREG4    TIMER2 LSB
      JSR   BLKMOV   GO LOAD BUFFER
      PULB          RESTORE B
      RTS
*
*
*-----*
*SRV5, SUBROUTINE TO SERVICE INTERRUPTS FROM
* TIMER #3. TIMER3 COUNTS HSCAN PULSES AND IS USE
* TO SET THE TOP AND BOTTOM MARGINS OF THE IMAGE
*-----*
*
*
SRV5  PSHB          SAVE B
      LDAA  PREG2    GET PIA-B
      BITA  #$80     IS READY LITE LIT?
      BEQ   SRV53    NO, THEN ABORT, ABORT, ABORT!
      LDAA  PREVAL   MSPART OF PREVAL
      LDAB  PREVAL+1 LS PART
      TSTA          IS MSPART=0?
      BNE   SRV50    NO, IT IS NOT
      CMPB  #$E1     WELL, THEN IS LSPART=225D?
      BNE   SRV50    NO IT IS NOT
      LDAA  #$E1     DATA TO TURN ON TIMER2 0/P
      STAA  TREG1    PUT IN C/R TIMER2
      STAA  TIM2     SAVE IN DUMMY REG
      LDAA  PREG2    GET PIA B AGAIN
      ORAA  #$28     TURN ON PATTERN LITE/DATA
      STAA  PREG2    RETURN TO PIA
      LDX   #$800
      STX   TREG6    NEW DATA TO TIMER3
      STX   PREVAL   STORE IN PREVAL AS WELL
      JMP   SRV52    EXIT PATH
      CMPA  #$08     IS MSPART=08H?
      BNE   SRV51    NOT AT ALL
      TSTB          IS LSPART=00?
      BNE   SRV51    NOT THIS TIME
      LDAA  PREG1    GET CONT REG A
      ORAA  #$08     STOP SYNTHZR CLOCK
      STAA  PREG1    RETURN TO CONT REG
      LDAA  TIM2     GET TIMER CONTRL DATA
      ANDA  #$7F     TURN OFF BIT7(O/P ENABLE)
      STAA  TIM2     RETURN TO DUMMY
      STAA  TREG1    ENTER IN TIM2 C/R

```

00263P	017B	CE	00E2	A	LDX	##00E2	BOTTOM MARGIN VALUE
00264P	017E	FF	000E	D	STX	PREVAL	STORE FOR NEXT TIME
00265P	0181	FF	0000	A	STX	TREG6	DATA FOR BOTTOM MARGIN
00266P	0184	B6	0000	A	LDAA	PREG2	GET PIAB DATA
00267P	0187	84	D7	A	ANDA	##D7	TURN OFF PATTERN LITE/DATA
00268P	0189	B7	0000	A	STAA	PREG2	RETURN TO PIAB
00269P	018C	7E	01A6	P	JMP	SRV52	EXIT PATH
00270P	018F	4D			TSTA		IS MSPART=0?
00271P	0190	26	14	01A6	BNE	SRV52	NO, THIS IS A LOT OF DUNG
00272P	0192	C1	E2	A	CMPB	##E2	IS LSPART=226D?
00273P	0194	26	10	01A6	BNE	SRV52	SEE ABOVE
00274P	0196	B6	0000	A	LDAA	PREG2	GET PIAB REG
00275P	0199	86	10	A	LDAA	##10	TURN ON FINISHED LITE
00276P	019B	B7	0000	A	STAA	PREG2	
00277P	019E	7E	01A6	P	JMP	SRV52	
00278P	01A1	01			NOP		
00279P	01A2	01			NOP		
00280P	01A3	01			NOP		
00281P	01A4	01			NOP		SPARES
00282P	01A5	01			NOP		
00283P	01A6	33			PULB		REJOIN INTRPT
00284P	01A7	39			RTS		
00285P	01A8	7E	0067	P	JMP	SRV02	EXIT PATH TO ABORT
00286					END		
TOTAL ERRORS 00000							

D	DEFF	BASE1	00015	00044*00163
P	00DC	BLK0	00163*	
P	00E4	BLK1	00166*00170	
DP	00D9	BLKMOV	00015	00162*00219
DD	0011	BUTTON	00017	00041*00051 00103 00117
DD	000B	CNTR	00017	00037*
DD	0010	CNTR1	00017	00040*
R		DIVRAT	00011*00142	
P	001C	INT1	00054	00056 00058*
P	001D	INT2	00059*	
P	0028	INT3	00061	00063*
P	0038	INT30	00070*	
P	0040	INT4	00069	00071 00073*
P	004F	INT5	00075	00077 00079*
P	005E	INT6	00066	00081 00083 00085*
DP	0006	INTRPT	00014	00048*
DD	0007	LNCNT	00016	00035*
P	0000	MSK0	00021*00053	
P	0001	MSK1	00022*	
P	0002	MSK2	00023*00060	00065
P	0003	MSK3	00024*00070	
P	0004	MSK4	00025*00076	
P	0005	MSK5	00026*00082	
R		PREG0	00008*00143	00183
R		PREG1	00008*00059	00107 00109 00197 00199 00256 00258
R		PREG2	00008*00050	00111 00144 00146 00184 00233 00245 00247
			00266 00268 00274 00276	
R		PREG3	00008*00048	
DD	000E	PREVAL	00015	00039*00141 00236 00237 00250 00264
DD	0003	PWBUF	00017	00033*

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DD 0005 SRCPNT 00016 00034*00164
DP 005F SRV0 00014 00055 00102*
P 0082 SRV01 00105 00117*
P 0067 SRV02 00107*00202 00285
P 0001 SRV03 00119 00121 00147*
P 0004 SRV04 00116 00123 00149*
P 0007 SRV05 00148 00150 00151*
DP 00EF SRV2 00014 00062 00182*
P 011C SRV21 00186 00200*
P 011E SRV22 00188 00202*
R SRV3 00010*00072
DP 0121 SRV4 00014 00078 00215*
DP 0130 SRV5 00014 00084 00232*
P 0161 SRV50 00239 00241 00252*
P 018F SRV51 00253 00255 00270*
P 01A6 SRV52 00251 00269 00271 00273 00277 00283*
P 01A8 SRV53 00235 00285*
DD 0009 STCK 00016 00036*00162 00171
DD 000C SUM 00015 00038*
DD 0000 TIM1 00016 00030*00067 00129 00193 00195
DD 0001 TIM2 00016 00031*00073 00112 00115 00125 00127 00132 00189
00191 00244 00259 00261
DD 0002 TIM3 00016 00032*00079 00136
R TREG0 00008*00130 00135 00196
R TREG1 00008*00063 00114 00126 00133 00192 00216 00243 00262
R TREG2 00009*00138
R TREG3 00009*00217
R TREG4 00009*00218
R TREG5 00010*
R TREG6 00010*00140 00249 00265
R TREG7 00010*

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00001          TTL      SRV: MODULE TO SERVICE INTERRUPTS F
00002          OPT      REL
00003          IDNT     SRV V1.03
00004          NAM      SRV103
00005          *
00006          *DATE: 9 MARCH 1979
00007          *
00008          *
00009          XREF     PREG0, PREG1, PREG2, PREG3, TREG0, TREG1
00010          XREF     TREG2, TREG3, TREG4, TREG5, TREG6, TREG7
00011          XREF     SRCPNT, TIM1, TIM2, TIM3, LNCNT, STCK
00012          XREF     BASE1, PREVAL, SUM
00013          XREF     CNTR, CNTR1, PWBUF
00014          *
00015          XDEF      SRV3
00016          *
00017          *-----
00018          *SRV3 SUBROUTINE USED TO SYNCHRONISE THE CLOCK IN
00019          *THE MICRO E-BEAM WITH THE SWEEP SIGNALS OF THE
00020          * SCANNING ELECTRON MICROSCOPE.
00021          *
00022          *  TIMER CONTROL REGISTER NOTES:
00023          *      BIT4=0  FREQ COMPARE MODE
00024          *      BIT4=1  PW COMPARE MODE
00025          *      BIT5=0  INTRPT IF GATE BEFORE TIMEOUT
00026          *      BIT5=1  INTRPT IF TIMEOUT BEFORE GATE
00027          *
00028          *
00029          *
00030          *-----
00031P 0000          PSCT
00032          *
00033P 0000 37      SRV3  PSHB          SAVE B IN STACK
00034P 0001 7A 0000 A      DEC      CNTR1
00035P 0004 B6 0000 A      LDAA     TREG2
00036P 0007 F6 0000 A      LDAB     TREG3      NEEDED TO CLR IRQ
00037P 000A B6 0000 A      LDAA     CNTR1
00038P 000D 2C 34 0043      BGE      SRV310
00039P 000F B6 0000 A      LDAA     TIM1      GET STATUS OF T1 FROM DUMM
00040P 0012 84 10      A      ANDA     #$10      TEST BIT 4
00041P 0014 27 30 0046      BEQ      SRV311      BIT4 IS SET
00042P 0016 F6 0000 A      SRV30  LDAB     TREG3      GET LS PART OF T1 DATA
00043P 0019 B6 0000 A      LDAA     TREG2      GET MS PART OF T1 DATA
00044P 001C B7 0000 A      STAA     PWBUF
00045P 001F F7 0001 A      STAB     PWBUF+1      SAVE PW DATA IN BUFFER
00046P 0022 C0 80      A      SUBB     #$80
00047P 0024 82 0C      A      SBCA     #$0C      SUBTRACT 32000 FROM RESIDU
00048P 0026 2B 34 005C      BMI      SRV33
00049P 0028 4D      TSTA          IS MSPART=0?
00050P 0029 26 21 004C      BNE      SRV32      NO
00051P 002B C1 40      A      CMPB     #$40      IS LSPART=40?
00052P 002D 22 1A 0049      BHI      SRV321      MUST BE BIGGER THAN DELTA
00053P 002F FB 0001 A      SRV31  ADDB     SUM+1      ADD RESIDUE TO SUM REG
00054P 0032 B9 0000 A      ADCA     SUM
00055P 0035 B7 0000 A      STAA     SUM
00056P 0038 F7 0001 A      STAB     SUM+1      STORE IN SUM REGISTER
00057P 003B 7A 0000 A      DEC      CNTR
00058P 003E B6 0000 A      LDAA     CNTR

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00059P	0041	2D 34 0077		BLT	SRV35	GO TRIM UP DIV. RATIO
00060P	0043	7E 00FC	P	SRV310 JMP	SRV39	EXIT PATH
00061P	0046	7E 00DC	P	SRV311 JMP	SRV38	
00062P	0049	7A 0000	A	SRV321 DEC	PREG0	DEC DIVIDER RATIO
00063P	004C	86 03	A	SRV32 LDAA	#\$03	
00064P	004E	B7 0000	A	STAA	CNTR1	
00065P	0051	86 04	A	LDAA	#\$04	
00066P	0053	B7 0000	A	STAA	CNTR	RESET CNTR
00067P	0056	7A 0000	A	DEC	PREG0	INCR DIV. RATIO
00068P	0059	7E 00FC	P	JMP	SRV39	JUMP TO EXIT PATH
00069P	005C	81 FF	A	SRV33 CMPA	#\$FF	IS MSPART=\$FF?
00070P	005E	26 07 0067		BNE	SRV34	NO
00071P	0060	C1 C0	A	CMPB	#\$C0	IS B LT DELTA?
00072P	0062	24 CB 002F		BCC	SRV31	
00073P	0064	7C 0000	A	INC	PREG0	INC DIVIDER RATIO
00074P	0067	86 03	A	SRV34 LDAA	#\$03	
00075P	0069	B7 0000	A	STAA	CNTR1	
00076P	006C	86 04	A	LDAA	#\$04	
00077P	006E	B7 0000	A	STAA	CNTR	
00078P	0071	7C 0000	A	INC	PREG0	INCR DIVIDER RATIO
00079P	0074	7E 00FC	P	JMP	SRV39	
00080P	0077	F6 0001	A	SRV35 LDAB	SUM+1	GET CONTENTS OF SUM REG
00081P	007A	B6 0000	A	LDAA	SUM	
00082P	007D	2D 13 0092		BLT	SRV351	
00083P	007F	44		LSRA		
00084P	0080	56		RORB		
00085P	0081	44		LSRA		
00086P	0082	56		RORB		DIVIDE SUM BY \$04
00087P	0083	7F 0000	A	CLR	SUM	ZERO SUM REG FOR NEXT USE
00088P	0086	7F 0001	A	CLR	SUM+1	
00089P	0089	4D		TSTA		
00090P	008A	26 C0 004C		BNE	SRV32	IF A NE 0 GO FIX DIV RATIO
00091P	008C	C1 19	A	CMPB	#\$19	
00092P	008E	22 BC 004C		BHI	SRV32	
00093P	0090	2F 17 00A9		BLE	SRV37	
00094P	0092	43		SRV351 COMA		COMPLMNT A
00095P	0093	53		COMB		COMPLMNT B
00096P	0094	CB 01	A	ADDB	#\$01	FORM2'S COMP OF A
00097P	0096	89 00	A	ADCA	#\$00	
00098P	0098	44		LSRA		
00099P	0099	56		RORB		
00100P	009A	44		LSRA		
00101P	009B	56		RORB		DIVIDE SUM BY 4
00102P	009C	7F 0000	A	CLR	SUM	ZERO SUM REG
00103P	009F	7F 0001	A	CLR	SUM+1	
00104P	00A2	4D		TSTA		
00105P	00A3	26 C2 0067		BNE	SRV34	IF A NE 0 GO FIX DIV DATA
00106P	00A5	C1 19	A	CMPB	#\$19	
00107P	00A7	22 BE 0067		BHI	SRV34	
00108P	00A9	B6 0000	A	SRV37 LDAA	TIM1	GET TIMER1 CR
00109P	00AC	84 10	A	ANDA	#\$10	IS BIT4=0?
00110P	00AE	27 2C 00DC		BEQ	SRV38	YES
00111P	00B0	B6 0000	A	LDAA	TIM1	
00112P	00B3	84 DF	A	ANDA	#\$DF	TURN OFF BIT5
00113P	00B5	84 EF	A	ANDA	#\$EF	TURN OFF BIT4
00114P	00B7	B7 0000	A	STAA	TIM1	
00115P	00BA	F6 0000	A	LDAB	TIM2	
00116P	00BD	CA 01	A	ORAB	#\$01	ACCESS CR1

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00117P 00BF F7 0000 A STAB TIM2
00118P 00C2 F7 0000 A STAB TREG1
00119P 00C5 B7 0000 A STAA TREG0
00120P 00C8 86 19 A LDAA #$19
00121P 00CA C6 00 A LDAB #$00 PUT 6400D IN A&B
00122P 00CC F0 0001 A SUBB PWBUF+1
00123P 00CF B2 0000 A SBCA PWBUF CALCULATE PW
00124P 00D2 80 08 A SUBA #$08 SUBTRACT 2048D
00125P 00D4 44 LSR A
00126P 00D5 56 ROR B DIV RESULT BY 2
00127 * ADD A #$08 ADD 2048D TO MARGIN
00128P 00D6 B7 0000 A STAA PWBUF MSPART TO BUFFER
00129P 00D9 F7 0001 A STAB PWBUF+1 LSPART TO NEXT BUFFER
00130 * LDX #5000 ($1388)
00131 * STX TREG2 PUT 5000 INTO T1 DATA
00132 * LDA A #$06
00133 * STA A CNTR1
00134 * BRA SRV39 EXIT PATH
00135P 00DC 01 SRV38 NOP * LDA A #$13
00136 * LDA B #$88
00137 * SUB B TREG3
00138 * SBC A TREG2
00139 * STA A TREG2
00140 * STA B TREG3 A&B REGS NOW HAVE PW
00141 * SUB B PWBUF+1
00142 * SBC A PWBUF
00143P 00DD B7 0000 A STAA TREG4
00144P 00E0 F7 0000 A STAB TREG5 SETUP DELAY FOR T2
00145P 00E3 B6 0000 A LDAA TIM1 GET TIMER1 STATUS
00146P 00E6 84 BF A ANDA #$BF
00147P 00E8 B7 0000 A STAA TREG0 DISABLE T1 INTRPT
00148P 00EB B7 0000 A STAA TIM1
00149P 00EE B6 0000 A LDAA PREG2
00150P 00F1 8A 80 A ORAA #$80 TURN ON READY LITE
00151P 00F3 84 BF A ANDA #$BF TURN OFF NOTREADY LITE
00152P 00F5 B7 0000 A STAA PREG2
00153P 00F8 FE 0000 A LDX TREG6
00154P 00FB 01 NOP
00155P 00FC 01 SRV39 NOP
00156P 00FD 01 NOP
00157P 00FE 01 NOP SPARES
00158P 00FF 01 NOP
00159P 0100 01 NOP
00160P 0101 33 PULB RESTORE B
00161P 0102 39 RTS
00162 END
TOTAL ERRORS 00000

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```

R BASE1 00012*
R CNTR 00013*00057 00058 00066 00077
R CNTR1 00013*00034 00037 00064 00075
R LNCNT 00011*
R PREG0 00009*00062 00067 00073 00078
R PREG1 00009*
R PREG2 00009*00149 00152
R PREG3 00009*

```

```

R      PREVAL 00012*
R      PWBUF  00013*00044 00045 00122 00123 00128 00129
R      SRCPNT 00011*
DP 0000 SRV3  00015 00033*
P 0016 SRV30  00042*
P 002F SRV31  00053*00072
P 0043 SRV310 00038 00060*
P 0046 SRV311 00041 00061*
P 004C SRV32  00050 00063*00090 00092
P 0049 SRV321 00052 00062*
P 005C SRV33  00048 00069*
P 0067 SRV34  00070 00074*00105 00107
P 0077 SRV35  00059 00080*
P 0092 SRV351 00082 00094*
P 00A9 SRV37  00093 00108*
P 00DC SRV38  00061 00110 00135*
P 00FC SRV39  00060 00068 00079 00155*
R      STCK   00011*
R      SUM    00012*00053 00054 00055 00056 00080 00081 00087 00088
              00102 00103
R      TIM1   00011*00039 00108 00111 00114 00145 00148
R      TIM2   00011*00115 00117
R      TIM3   00011*
R      TREG0  00009*00119 00147
R      TREG1  00009*00118
R      TREG2  00010*00035 00043
R      TREG3  00010*00036 00042
R      TREG4  00010*00143
R      TREG5  00010*00144
R      TREG6  00010*00153
R      TREG7  00010*

```

PAGE 001 MAP .SA:0

NO UNDEFINED SYMBOLS

MEMORY MAP

S SIZE STR END COMN
A 022C F000 F22B
B 0000 0020 0020 0000
C 0000 0020 0020 0000
D 03E1 0020 0400 0000
P 0338 F800 FB37 0000

MODULE NAME BSCT DSCT PSCT
PATRN 0020 0020 F800
INI104 0020 0020 F800
0020 0020 F87C
INT201 0020 0020 F88A
SRV103 0020 0032 FA35

DEFINED SYMBOLS

MODULE NAME: PATRN
PATDAT A F02C PATRN A F000

MODULE NAME: INI104
DIVRAT P F800 INIT P F801 PREG0 A DF88 PREG1 A DF89
PREG2 A DF8A PREG3 A DF8B TREG0 A DF90 TREG1 A DF91
TREG2 A DF92 TREG3 A DF93 TREG4 A DF94 TREG5 A DF95
TREG6 A DF96 TREG7 A DF97

MODULE NAME:
BCKGND P F87C

MODULE NAME: INT201
BASE1 A DEFF BLKMOV P F963 BUTTON D 0031 CNTR D 002B
CNTR1 D 0030 INTRPT P F890 LNCNT D 0027 PREVAL D 002E
PWBUF D 0023 SRCPNT D 0025 SRV0 P F8E9 SRV2 P F979
SRV4 P F98B SRV5 P F98A STCK D 0029 SUM D 002C
TIM1 D 0020 TIM2 D 0021 TIM3 D 0022

MODULE NAME: SRV103
SRV3 P FA35