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MANUFACTURING METHODS AND TECHNOLOGY MEASURE FOR FABRICATION OF--ETC(U)
OCT 79 B B ADAMS, M F DEVITO, W L KROWN DAAK70-78-C-0120

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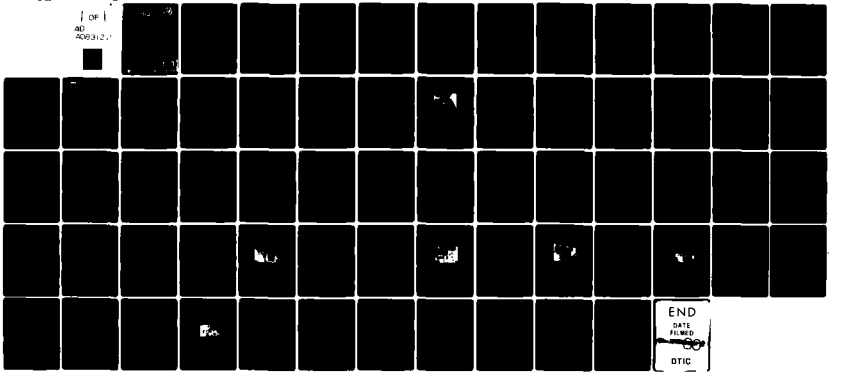

Manufacturing Methods and Technology Measure for Fabrication of Silicon Transcalent Rectifier Interim Technical Report

Period Covered:

17 December, 1978 through 22 October, 1979

Contract No. DAAK70-78-C-0120

Prepared by:

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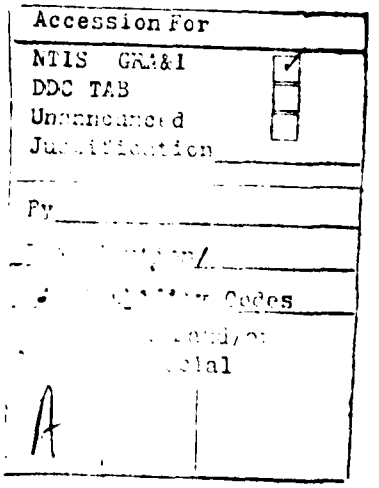
SUMMARY

This report describes in detail the more important steps in the fabrication and testing of the confirmatory samples of the MM&T Silicon Transcalent Rectifier program. Factors used in the selection of the prototype design are presented. The data from all ten confirmatory samples including description of test circuits and test results are contained herein as well as some decision making data taken on additional devices.

The ten confirmatory sample devices successfully passed all of the inspections required by the contract. All devices were then shipped to MERADCOM on September 18, 1979. Government acceptance of the shipment is awaited.



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18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Environmental testing	Statistical analysis	Heat-Pipe
Ion implanted	Transcalent Rectifier	Power Diode
Webless wick	"Go", "No-Go" gauge	Isothermal
Convoluted and nonconvoluted	Thermal resistance	

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

RCA has successfully completed the fabrication and testing of the ten confirmatory samples. This report thoroughly describes the test results as well as the basis for selecting the prototype design. It also includes a picture or block diagram of each test circuit utilized. All devices passed all inspections with a yield of 100%.

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I. INTRODUCTION

This report is the Interim Technical Report describing the work performed by RCA, Lancaster, PA during the confirmatory phase of the contract covering the period of 17 December 1978-22 October 1979. Work was performed in accordance with the DRDME-EA Purchase Description, dated 16 November, 1977 to the MERADCOM Semiconductor Device, Silicon Transcalent Rectifier Specification, dated 6 June 1978, as attached to the contract. The scope of the contract covers the MM&T tasks for fabricating a semiconductor device, silicon Transcalent rectifier, RCA type J15401 and the subsequent pilot production of the device.

Although this report covers the confirmatory phase of the program, the 24 months duration program will establish the production engineering techniques and verify a pilot production capability for the J15401 silicon Transcalent rectifier conforming to Fig. 1 of this report. Electrical, thermal and environmental inspections are a part of this report per DD 1423 of the contract.

II. DEVICE

A. Description of the Structure

The Transcalent rectifier type J15401 is thoroughly described in the report entitled, "Manufacturing Methods and Technology Measure for Fabrication of Silicon Transcalent Rectifier, Interim Technical Report, dated January 1979. The above report includes a Flow Diagram for the J15401 rectifier wafer metallizing, contouring and testing and a Flow Diagram for the assembly and processing of the J15401 rectifier. Included also are many step by step procedures utilized in the processes described. The report stipulated will serve as an aid to the understanding of this report, however, the cross section drawing of the Transcalent rectifier will conform to Fig. 1 of this report.

III. PROCESS AND FABRICATION IMPROVEMENTS INVESTIGATED

All ten confirmatory sample rectifier devices were fabricated utilizing as much as possible the recommendations given in RCA proposal DP-8135 and the descriptions given in this report.

Four product design variations were tested in the confirmatory sample phase. However, the differences were slight as the outline or interface surfaces of the device remained the same and the performance characteristics were identical. Each variation was included as a possible production improvement consisting of the following items.

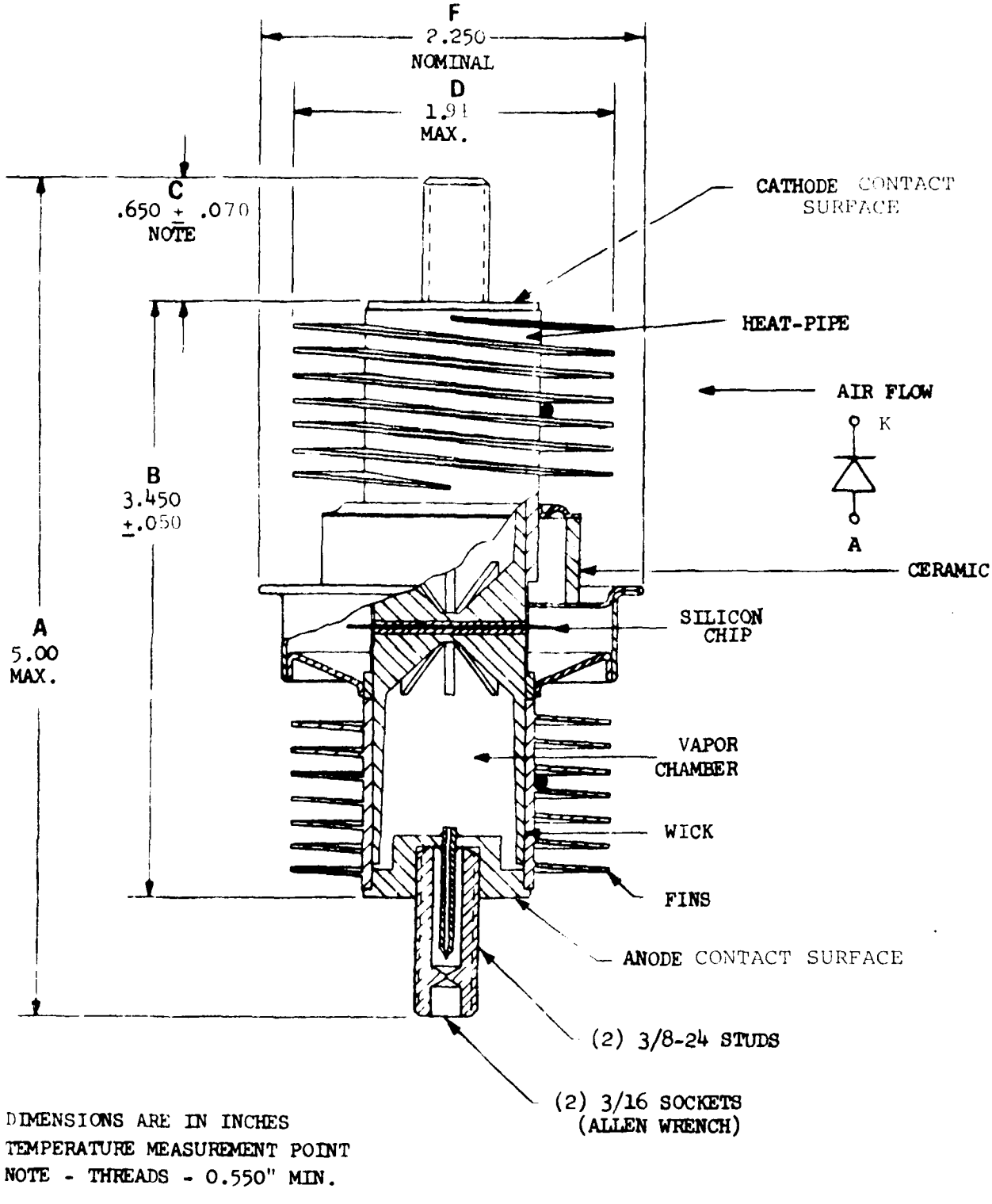


Figure 1 Transcalent Rectifier Type J15401 Cross Section Drawing

A. Ion Implantation

Two units were successfully tested which were ion implanted with a boron $N_{dose} = 6 \times 10^{15}$ at 200 KeV on one side and a phosphorus $N_{dose} = 6.5 \times 10^{15}$ at 180 Kev on the other side. There was no detectable difference in electrical performance of the ion implanted vs. the standard process rectifiers. Ion implantation eliminated five of the nine process steps and substituted the two implants.

The ion implantation was investigated as a future production method. Unfortunately, the time for implanting with our equipment was 20 minutes per wafer for the boron side alone. One side of a wafer could be boron doped in 3.5 minutes with our standard procedures, and this time could easily be cut in half by doubling the wafer boat size. A hot source implanter could implant economically, but the contractor does not intend to buy one at the present time. Consequently, standard doped wafers will be used in the pilot run.

B. Webless Wicked

This concept is shown in Fig. 2. The anode portion of the cross section shows a webless wick. Conversely the cathode portion (ceramic side) displays a webbed wicked assembly. Eliminating the wick is a definite process improvement which helps to make the device more manufacturable. Consequently, this approach will be used in the pilot run.

C. Tungsten Button-Convoluted

The convoluted design was incorporated into the cathode heat-pipe to reduce low temperature stresses. Fig. 3 displays the convoluted concept. Test results indicate that the rectifier does not need the convolution at low temperatures which simplifies the construction of the part in question. Confidence was gained when two non-convoluted designs were tested down to $-55^{o}C$ which is much more severe than the $-25^{o}C$ test stipulated by the contract.

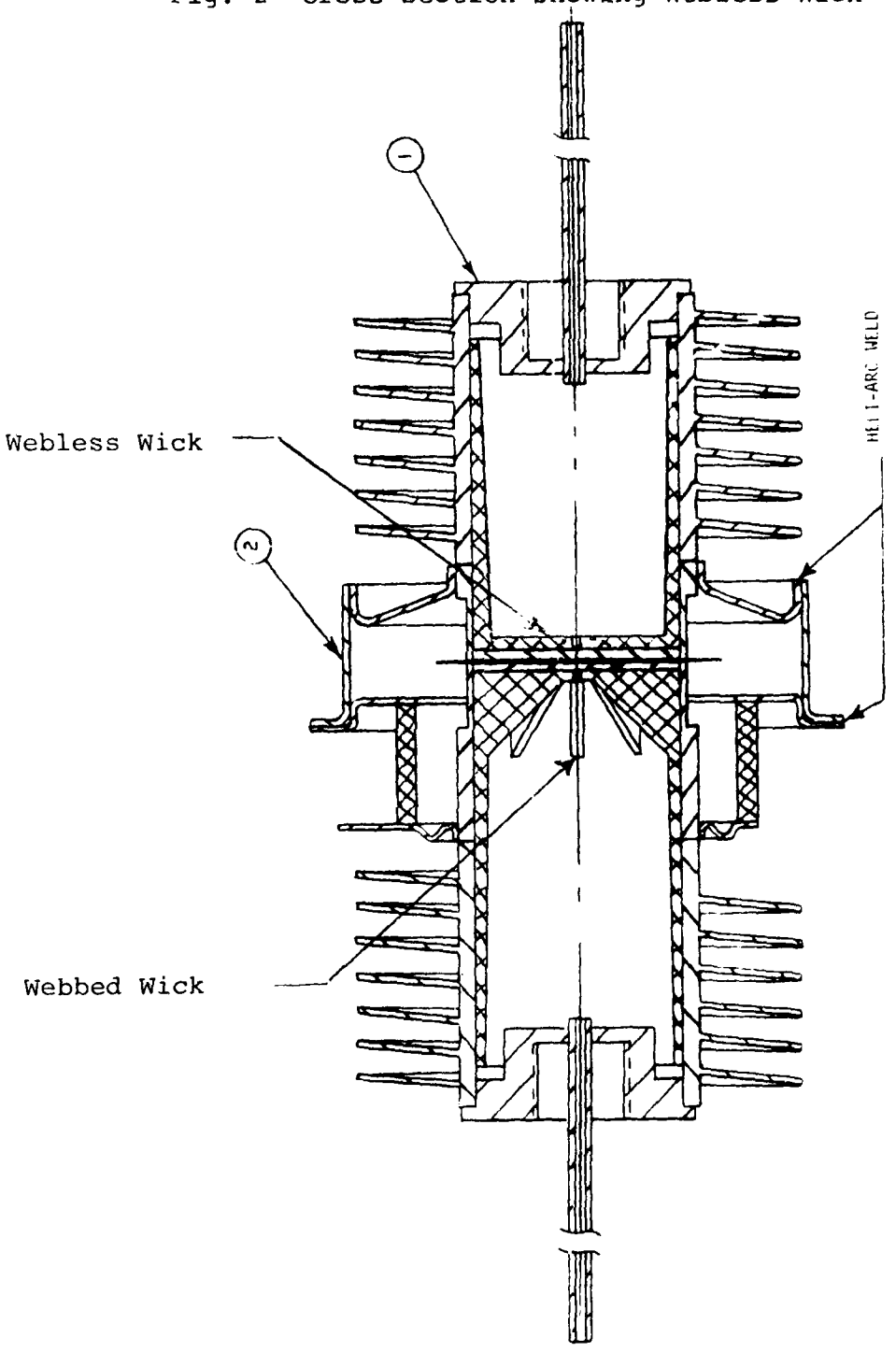
D. Tungsten Button - Nonconvoluted

This approach which can be seen in Fig. 2 has been adopted as the pilot run design for reasons discussed under C.

E. Conclusion

The design of the pilot run devices includes the outline of Fig. 1, standard doped wafers, webless wicks, and non-convoluted cathode strain sleeves. This combination of

Fig. 2 Cross Section Showing Webless Wick



SCALE

DIMENSIONS IN

CAUTION Use only the lubricants specified in E.S. 33-33-805

UNLESS OTHERWISE SHOWN DIMENSIONS SHOWN WITHOUT TOLERANCES ARE DESIGN CENTERS

9E 1-78 110 DLY/AU

TL 359 10-78

* CHANGE
** ADDITION
*** DELETION

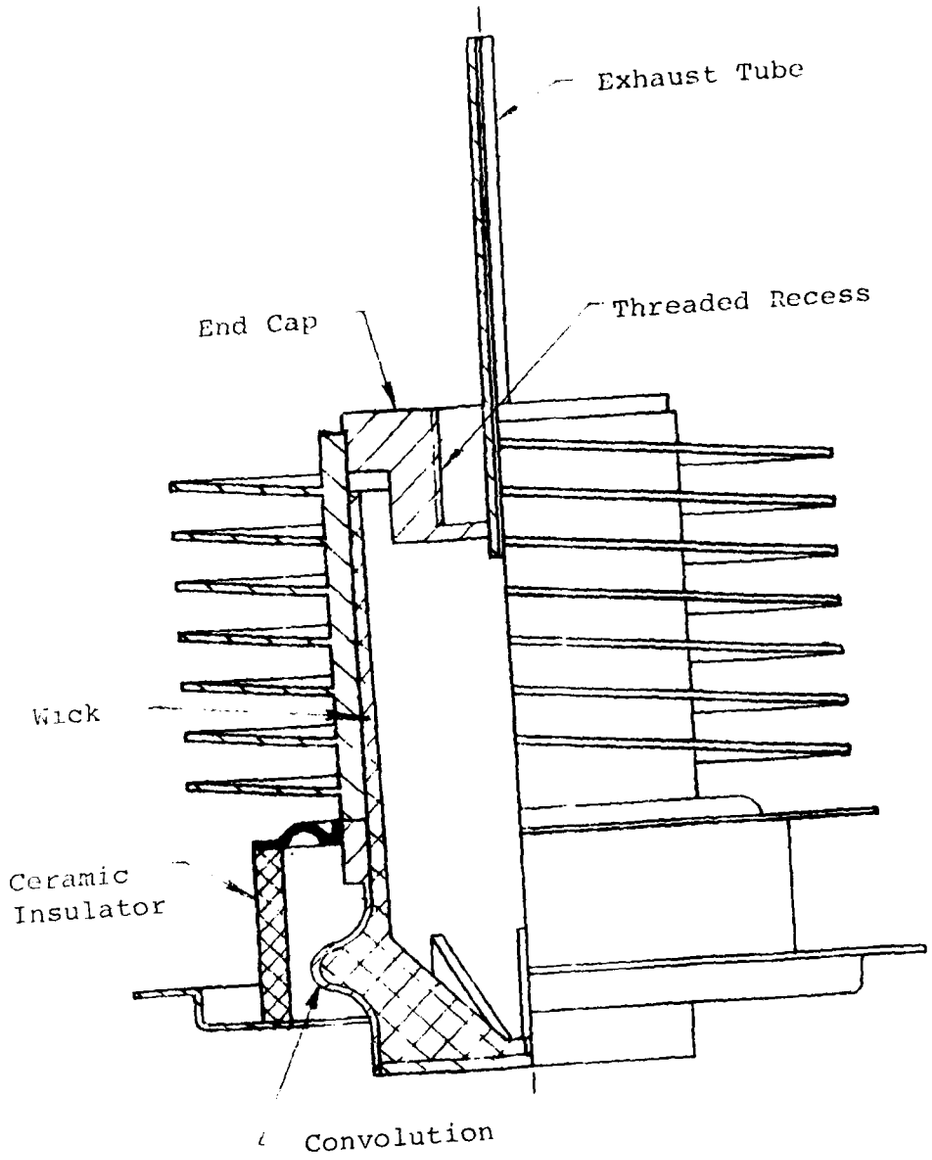


Figure 3 Pre-Fabricated Cathode (Emitter) Heat-Pipe

features has been proven acceptable via the confirmatory tests and they will remain in force as part of the identity of the J15401 Transcalent silicon rectifier.

IV. ELECTRICAL, MECHANICAL, THERMAL AND ENVIRONMENTAL INSPECTION CONFIRMATORY TEST PROGRAM

Ten silicon rectifiers were tested during the Confirmatory Sample phase of this program. The total sample consisted of four variations. The serial numbers and corresponding construction variations were as follows:

Ser. No.	Variation
II-2 II-3	Ion Implanted
J149 J150 J151	Webless Wicked
J157 J160 J162	Tungsten Button: Convoluted
J156 J163	Tungsten Button: Nonconvoluted

Due to the variations in construction, the number of units subjected to each environmental test was equal to or greater than the sample size listed in the confirmatory test plan previously issued. Table 1 lists the plan's sample size and the actual number of devices tested. In addition, it lists the permitted percentage of failures.

A. Group A Inspection

1. Subgroup 1

All of the Transcalent rectifiers were visually and mechanically inspected in conformance to method 2071 and Fig. 1 of the specification as modified by the Interim Engineering Report dated January 1979 using the specified method 2066. The actual measurements of the ten confirmatory J15401C rectifiers are listed in Table 2. Table 3 shows the results of a statistical analysis of these data which indicate that all of the devices met the specified dimensions with margin.

In addition to taking actual measurements all the devices were checked using the "go-no-go" gauge shown in Fig. 4.

TABLE 1

Sample Size

Subgroup No.	Title	% of Units To Be Tested	Actual % of Units Tested	% Allowed To Fail	Actual % Failed
1	Barometric Pressure Reduced	50	100	0	0
2	Blocking Voltage L.T.	30	100	0	0
3	Thermal Shock	20	100	0	0
	Moisture Resistance	20	20	0	0
	Salt Atmosphere	20	20	0	0
4	Thermal Fatigue	100	100	10	0
5	Shock	20	50	0	0
	Vibration, Variable Freq.	20	50	0	0

Table 2

Physical Dimensions of Confirmatory Samples

Device #	A	B	C	D	F
II2	4.761	3.456	0.640	1.808	2.100
II3	4.761	3.464	0.650	1.834	2.100
J149	4.737	3.447	0.635	1.800	2.104
J150	4.751	3.463	0.647	1.806	2.101
J151	4.744	3.455	0.641	1.805	2.100
J156	4.748	3.476	0.624	1.800	2.100
J157	4.723	3.465	0.632	1.790	2.102
J160	4.749	3.472	0.631	1.792	2.106
J162	4.748	3.472	0.628	1.804	2.102
J163	4.718	3.463	0.635	1.803	2.100

Table 3

Statistical Analysis of the Dimensional Data
of the Confirmatory Samples

Character	Avg.	Sigma	Max.	Min.	Chi-Sq.	N
Dim. A	4.744	0.014	4.761	4.718	8.38	10
Dim. B	3.463	0.009	3.476	3.447	2.95	10
Dim. C	0.636	0.008	0.650	0.624	3.82	10
Dim. D	1.804	0.012	1.834	1.790	12.40	10
Dim. F	2.102	0.002	2.106	2.100	15.21	10

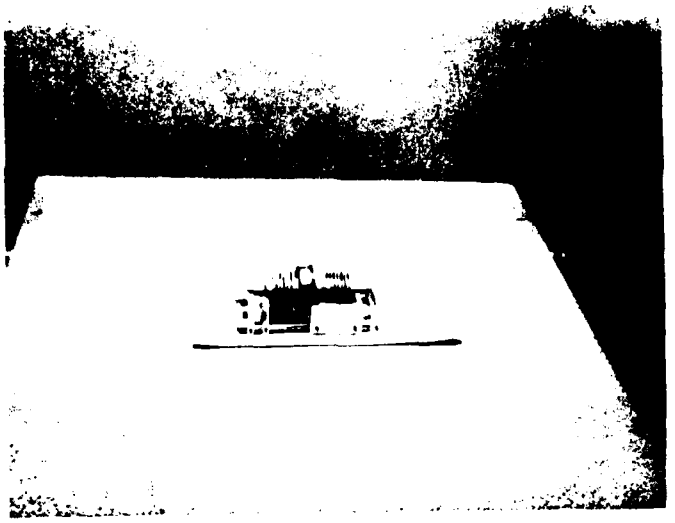


Fig. 4 J1540l "Go-No-Go" Gauge

2. Subgroup 2 - Test Temperature $T_A = 25 \pm 3^oC$

All confirmatory samples were tested for reverse current, i_r, and reverse voltage, V_r, under the conditions specified for method 4016.2. Fig. 5 is a histogram of the reverse current measured under the conditions in the specification. Table 4 lists the detail data.

From the statistical data we can expect all of the measurements to be less than 1.2 mA or 8% of the specified 15 mA maximum.

Prior to submitting the devices to electrical test they all were tested out to 1000 volts of reverse voltage to insure that a sufficient safety margin existed.

3. Subgroup 3 - Thermal Resistance

The thermal resistance of the Transcalent rectifiers was measured using the specified method described in paragraph 4.6.1 of the specification. Each rectifier was calibrated for a temperature dependent parameter by recording the forward voltage drop at 4 amperes at several temperatures. The thermal resistance ($R_{\theta JC}$) was tested at 250 amperes of heating current, interrupted by a short period of time (less than 1 msec.) when the current was reduced to the metering value of 4 amperes. The forward voltage drop across the device was measured and used to determine the junction temperature from the calibration data. Simultaneously, the external temperature of the heat-pipes was measured and recorded. The difference in temperatures divided by the input heating power is the thermal impedance (transient) or resistance (steady state) of the device. The values of thermal resistance calculated from the data measured on the ten confirmatory samples are shown in Table 4. Fig. 6 is a histogram of these data. Thermal resistance calculated on the same devices after the environmental tests are listed in Table 5 with the initial values for comparison.

```
HISTOGRAM DATA[;1]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.5 .02 25
VERT SCALE:1
CHAR:IR+25  C
   CHARACTERISTIC-IR+25  C
    AVERAGE- 0.822
    SIGMA--- 0.1250599856
    MAXIMUM- 0.92
    MINIMUM- 0.61
    SAMPLE-- 10
```

No. of Devices

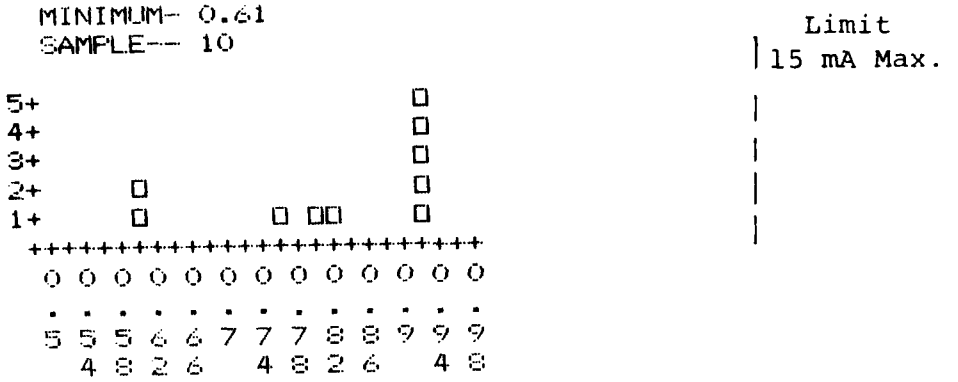


Fig. 5 Reverse Current at +25°C, (mA)

```
Histogram Data (3)

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.03 .02 25
VERT SCALE:1
CHAR:RΘJC
     CHARACTERISTIC-RΘJC
   AVERAGE- 0.114
   SIGMA--- 0.04718756898
   MAXIMUM- 0.2
   MINIMUM- 0.07
   SAMPLE-- 10
```

No. of Devices

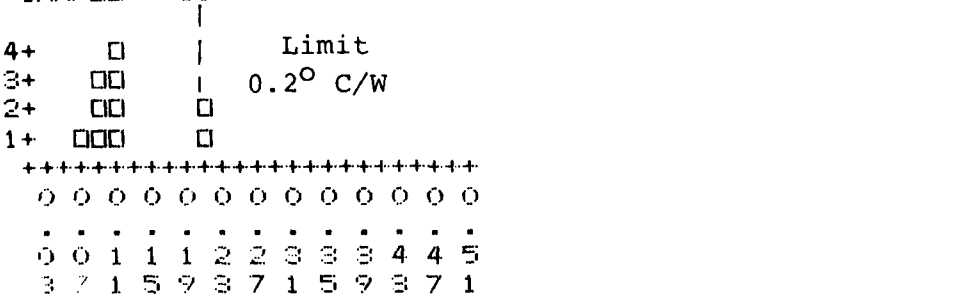


Fig. 6 Thermal Resistance, $R_{\Theta JC}$ (°C/W)

TABLE 4

Date 9/5/79

Confirmatory Samples

Tester P. Bransby

Electrical Data

	Visual	Dimensions	+25°C Rev. Cur. and Rev. Voltage	Thermal Resistance for Rect. Diode	+125°C Rev. Current and Rev. Voltage	Forward Voltage	Post Surge Current Test	Reverse Recovery Time	Post Barometric Pressure
Method Symbol	2071	2066	4016.2 i_r	Para. 4.6.1 $R_{\theta JC}$	4016.2 i_r	4011.3 V_f	4066.2 i_r	4031 t_{rr}	1001.1 i_r
Units			mA	°C/W	mA	Volts	mA	usec.	mA
Ser. No.									
J149	✓	✓	0.81	0.10	1.75	1.0	0.72	2.8	0.72
J150	✓	✓	0.61	0.11	1.80	1.0	0.51	2.6	0.72
J151	✓	✓	0.77	0.11	4.12	1.0	0.61	2.8	0.72
J156	✓	✓	0.92	0.07	6.18	0.92	0.72	2.4	0.68
J157	✓	✓	0.92	0.09	5.36	0.98	0.82	2.9	0.72
J160	✓	✓	0.92	0.08	2.06	0.98	0.82	3.0	0.72
J162	✓	✓	0.82	0.08	2.57	1.0	0.82	3.2	0.72
J163	✓	✓	0.92	0.20	1.85	1.0	0.82	2.9	0.69
II-2	✓	✓	0.61	0.10	1.44	1.0	0.61	2.4	0.33
II-3	✓	✓	0.92	0.20	1.44	1.0	0.67	2.0	0.29
Spec.			15 Max.	0.2 Max.	60 Max.	2.0 Max.	15 Max.	15.0 Max.	15 Max.

Table 5

Initial and Final Thermal Resistance

$^{o}C/W$

$T_A = 25 \pm 3^{o}C$

Ser. No.	J149	J150	J151	J156	J157	J160	J162	J163	II2	II3	Max. Spec. $^{o}C/W$
Initial	0.1	0.11	0.11	0.07	0.09	0.08	0.08	0.2	0.1	0.2	0.2
Final	0.13	0.10	0.16	0.14	0.10	0.1	0.09	0.15	0.2	0.19	0.2

Two of the devices, I13 (ion implanted) and J163 (nonconvoluted), had initial Thermal Impedance measurements at the upper limit of the specification, $0.2^{o}C/W$. Since similarly constructed devices in the confirmatory sample, I1-2 and J156, had initial normal measurements of $0.1^{o}C/W$ and $0.07^{o}C/W$ respectively, it is not believed that the high measurements are construction orientated, but rather a normal variation.

4. Subgroup 4 - Test Temperature of Case: $125 \pm 6^{o}C$
   Reverse Current, i_r, and Reverse Voltage, V_r

   The devices were tested under the specified conditions by method 4016.2. The specificaiton limit for maximum peak current is 60 mA. The detail data measured is listed in Table 4. Fig. 7 is a histogram of the distribution of the i_r measured at a reverse voltage of 800 V. These data indicate that all the devices were well within the maximum limits specified.

B. Group B Inspection

1. Subgroup 1 - Forward Voltage, V_f: Test at Room Ambient Temperature of $25 \pm 3^{o}C$

   The peak forward voltage drop was measured across all of the devices using method 4011.3. The devices were conducting an average current of 250 amperes when the measurements were made. Since the current conducted by the device is nearly 180^{o} of conduction angle, the peak current is approximately 800 amperes and the RMS current is about 400 amperes.

   During the tests, the Transcalent rectifiers were allowed to reach thermal equilibrium and the heat-pipe was confirmed to be isothermal. Room ambient air was blown across the fins to limit the temperature of the heat-pipes to $100^{o}C$.

   The individual data are listed in Table 4 and the distribution is shown in Fig. 8. All devices passed.

Histogram Data (2)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.0 .22 25
VERT SCALE:1
CHAR:IR+125
     CHARACTERISTIC-IR+125
     AVERAGE- 2.857
     SIGMA--- 1.731813757
     MAXIMUM- 6.18
     MINIMUM- 1.44
     SAMPLE-- 10

  2+  □ □
  1+  □□□□ □       □       □    □
   ++++++++++++++++++++++++++++++
    1 1 1 2 2 3 3 4 4 4 5 5 6
      . . . . . . . . . . . .
      4 8 3 7 2 6 0 5 9 4 8 2
      4 8 2 6   4 8 2 6   4 8
```

No. of Devices

Limit
60 mA Max.

Fig. 7 Reverse Current at 125°C Case Temp., (mA)

Histogram Data (4)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.8 .01 25
VERT SCALE:1
CHAR:VFM
       CHARACTERISTIC-VFM
    AVERAGE- 0.988
    SIGMA--- 0.02529822128
    MAXIMUM- 1
    MINIMUM- 0.92
    SAMPLE-- 10

  7+                        □
  6+                        □
  5+                        □
  4+                        □
  3+                        □
  2+                     □  □
  1+              □      □  □
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 1 1 1
    . . . . . . . . . .   . .
    9 8 8 8 8 9 9 9 9 9   0 0
      2 4 6 8   2 4 6 8   2 4
```

No. of Devices

Limit
2 V Max.

Fig. 8 Forward Voltage Drop, V_F (volts)

2. Subgroup 2 - Surge Current, i_f
Test Temperature, $T_A = 25 \pm 3^{o}C$

All confirmatory samples were tested under the conditions listed in the specification using method 4066.2. The surge current test was performed in the RCA owned test circuit that was developed for the J15371 Transcalent thyristor under Contract No. DAAB07-76-C-8120 and modified to test the rectifiers. The pulses of surge current were repeated at a rate of one pulse per minute for ten total surges. The 800 volts of reverse voltage, V_r, was reapplied following each surge. After the surge test, the reverse current was remeasured to confirm that the 4000 amperes peak surge currents did not damage the devices.

The values of reverse current measured after this surge test are listed in Table 4 and the distribution is plotted in Fig. 9. Comparing these data with those measured initially (reverse current - $25^{o}C$) indicated the confirmatory samples were not affected by the surge test.

3. Subgroup 3 - Reverse Recovery Time, T_{rr}
Test Temperature $T_A = 25 \pm 3^{o}C$

All devices were tested for reverse recovery time per the procedures of method 4031 of MIL-Std-750B. A modified circuit as outlined in the JEDEC Publication No. RS282 was used. This circuit utilizes the circuit parameters specified, however, the I_{FM} is standardized at 125 instead of 50 peak amperes.

The data measured on the engineering samples are listed in Table 4 and the distribution shown in Fig. 10. Again, the devices passed with margin.

C. Group C Inspection

1. Subgroup 1 - Barometric Pressure Reduced

All of the confirmatory devices were successfully tested under the conditions listed using the specified method 1001.1. A device which arcs over or exhibits harmful coronas that deteriorate the device is considered a failure. After exposure to the low pressure test the devices were tested for reverse current per Subgroup 2 of Table 1. The detail data is listed in Table 4 and the distribution plotted in Fig. 11.

Histogram Data (6)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:POST SURGE IR
 CHARACTERISTIC-POST SURGE IR
    AVERAGE- 0.712
    SIGMA--- 0.1106845885
    MAXIMUM- 0.82
    MINIMUM- 0.51
    SAMPLE-- 10

  4+         □
  3+         □
  2+    □ □ □
  1+ □ □□□ □
   ++++++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Limit
15 mA Max.

Fig. 9 Post Surge Reverse Current, I_r , (mA)

HISTOGRAM DATA[;5]

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.9 .06 25
VERT SCALE:1
CHAR:TRR
      CHARACTERISTIC-TRR
    AVERAGE  2.7
    SIGMA--  0.3527668415
    MAXIMUM- 3.2
    MINIMUM- 2
    SAMPLE-- 10

  2+           □      □ □
  1+  □        □  □   □ □ □  □
   ++++++++++++++++++++++++++++
    1 2 2 2 2 2 2 2 2 2 3 3 3
    . . . . . . . . . . . . .
    9 0 1 2 3 5 6 7 8 9 1 2 3
      2 4 6 8   2 4 6 8   2 4
```

No. of Devices

Limit
15 µsec. Max.

Fig. 10 Reverse Recovery Time, T_{rr} (µsec)

```
HISTOGRAM DATA[;7]
 LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.20 .05 25
 VERT SCALE:1
 CHAR:POST BARO IR
  CHARACTERISTIC-POST BARO IR
     AVERAGE- 0.631
     SIGMA--- 0.1700620802
     MAXIMUM- 0.72
     MINIMUM- 0.29
     SAMPLE-- 10

  6+            □
  5+            □
  4+            □
  3+            □
  2+           □□
  1+ □□        □□
   +++++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 1 1 1 1 1
    . . . . . . . .   . . . .
    2 3 4 5 6 7 8 9   1 2 3 4
```

No. of Devices

Limit
15 mA Max.

Fig. 11 Post Barometric Pressure Reverse Current, I_r (mA)

```
 HISTOGRAM DATA[;8]
 LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.04 .05 25
 VERT SCALE:1
 CHAR:POST BVLT IR
  CHARACTERISTIC-POST BVLT IR
     AVERAGE- 0.654
     SIGMA--- 0.1024369725
     MAXIMUM- 0.72
     MINIMUM- 0.46
     SAMPLE-- 10

  8+                 □
  7+                 □
  6+                 □
  5+                 □
  4+                 □
  3+                 □
  2+           □     □
  1+           □     □
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```

No. of Devices

Limit
15 mA Max.

Fig. 12 Post Blocking Voltage Reverse Current, I_r (mA)

2. Subgroup 2 - Blocking Voltage Life Test Temperature: $T_C = 125 \pm 6^{\circ}C$

All of the confirmatory devices were tested for 200 hours, each under the conditions specified, using the method of para. 4.6.2. After exposure to the blocking voltage life test, the reverse current was measured and recorded. The detail data measured is listed in Table 6 and the distribution of the data plotted in Fig. 12. All devices passed with margin.

The test plan required that only three devices be tested for this parameter. Since four different types of devices made up the samples (see Sec. IV) it was decided that all ten devices should be tested for this parameter for a complete evaluation.

3. Subgroup 3 - Thermal Shock, Moisture Resistance and Salt Atmosphere Tests

All the confirmatory devices were tested for Thermal Shock using test method 1051.1 and the conditions stated in the specification. After five cycles, the rectifiers were removed from the environmental chamber and two were submitted to the Moisture Resistance test, method 1021.1.

Reverse current measurements per Subgroup 2 of Table 1 of the specifications were taken as a check at this point to determine if the devices had survived the Thermal Shock and Moisture Resistance tests. All the units passed. Detail data is listed in Table 6 and the distributions plotted in Figs. 13 and 14.

The two devices (II2, II3) which had been subjected to the Moisture Test were subjected to the Salt Atmosphere test method 1041.1 for 24 hours. After the test, the salt was washed off of the devices which were then examined. The markings were legible and there was no evidence of flaking, pitting of the finish, or corrosion that would interfere with the application of the devices.

Reverse current tests per Subgroup 2 of Table 1 of the specification were performed, the detail data are listed in Table 6 and the distribution is plotted in Fig. 15. All devices passed with margin.

TABLE 6

Date 8/29/79

Post Environmental Data

Tester P. Bransby

	Post Blocking Voltage L.T.	Post Thermal Shock Test	Post Thermal Shock and Moisture Test	Post Salt Spray Test	Post Shock and Vibration Test	Post Thermal Fatigue L.T.	Post Thermal Fatigue Thermal Resistance Test	Final Envir. Thermal Resistance Test
Method	Par. 4.6.2	1051.1	1021.1 1051.1	1041.1	2016.2, 2056	Par. 4.6.3	Par. 4.6.1	Par. 4.6.1
Symbol	i_r	i_r	i_r	i_r	i_r	i_r	$R_{\theta jc}$	$R_{\theta jc}$
Units	mA	mA	mA	mA	mA	mA	°C/W	°C/W
Ser. No.								
J149	0.70	0.69	--	--	--	0.70	0.13	--
J150	0.70	0.69	--	--	--	0.70	0.10	--
J151	0.70	0.61	--	--	0.72	0.70	0.12	0.16
J156	0.70	0.60	--	--	0.67	0.57	0.14	0.14
J157	0.72	0.50	--	--	0.74	0.70	0.098	0.10
J160	0.70	0.50	--	--	--	0.70	0.10	--
J162	0.70	0.60	--	--	--	0.78	0.09	--
J163	0.70	0.50	--	--	--	0.72	0.15	--
II2	0.46	--	0.41	0.41	0.46	0.56	0.2	--
II3	0.46	--	0.41	0.41	0.46	0.56	0.19	--
Spec.	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	0.2 (Max.)	0.2 (Max.)

Histogram Data (9)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.40 .02 25
VERT SCALE:1
CHAR:POST THER SH
 CHARACTERISTIC-POST THER SH
   AVERAGE- 0.58625
   SIGMA--- 0.07998888851
   MAXIMUM- 0.69
   MINIMUM- 0.5
   SAMPLE-- 8

 3+      □     □
 2+      □     □   □
 1+      □     □   □
  ++++++++++++++++++++++++++
   0 0 0 0 0 0 0 0 0 0 0 0 0
   . . . . . . . . . . . . .
   4 4 4 5 5 6 6 6 7 7 8 8 8
     4 8 2 6   4 8 2 6   4 8
```

No. of Devices

Limit
15 mA Max.

Fig. 13 Post Thermal Shock Reverse Current, I_r (mA)

Histogram Data (10)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.35 .02 25
VERT SCALE:1
CHAR:TH SH MO
 CHARACTERISTIC-TH SH MO
       AVERAGE- 0.41
       SIGMA--- 0
       MAXIMUM- 0.41
       MINIMUM- 0.41
       SAMPLE-- 2

 2+   □
 1+   □
  ++++++++++++++++++++++++++
   0 0 0 0 0 0 0 0 0 0 0 0 0
   . . . . . . . . . . . . .
   3 3 4 4 5 5 5 6 6 7 7 7 8
   5 9 3 7 1 5 9 3 7 1 5 9 3
```

No. of Devices

Limit
15 mA Max.

Fig. 14 Post Thermal Shock and Moisture Reverse Current, I_r (mA)

Histogram Data (11)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.35 .01 25
VERT SCALE:1
CHAR:POST SALT SP
 CHARACTERISTIC-POST SALT SP
        AVERAGE- 0.41
        SIGMA--- 0
        MAXIMUM- 0.41
        MINIMUM- 0.41
        SAMPLE-- 2

  2+       □
  1+       □
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    3 3 3 4 4 4 4 4 5 5 5 5 5
    5 7 9 1 3 5 7 9 1 3 5 7 9
```

No. of Devices

Limit
15 mA Max.

Fig. 15 Post Salt Spray Reverse Current, I_r, (mA)

```
HISTOGRAM DATA[;13]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:POST TH FRT
  CHARACTERISTIC-POST TH FRT
    AVERAGE- 0.669
    SIGMA--- 0.0769487564
    MAXIMUM- 0.78
    MINIMUM- 0.56
    SAMPLE-- 10

  6+       □
  5+       □
  4+       □
  3+   □   □
  2+   □   □
  1+   □   □□
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Limit
15 mA Max.

Fig. 16 Post Thermal Fatigue Reverse Current, I_r (mA)

4. Subgroup 4 - Thermal Fatigue Test

All of the confirmatory samples were tested for reliability under the specified Thermal Fatigue Test Conditions and Spec. paragraph 4.6.3. The "on" and "off" times were two minutes each. The air flow across the devices was adjusted so that when the devices were conducting, the case or heat-pipe temperature was 90 + 10°C max. and 30 + 10°C min. The devices were subjected to a minimum of 200 "on-off" cycles. Ten measurements per Subgroup 2 of Table 1 were made. Detail data are listed in Table 6 and distribution is plotted in Fig. 16.

Since the sample consisted of four different constructions, an additional post thermal fatigue parameter was measured, Thermal Impedance. These data are listed in Table 6 and the distribution is plotted in Fig. 17.

All devices passed. The ion-implanted devices came closest to the specification limit of 0.2°C/W. Because of this high thermal impedance and other considerations, ion-implanted devices will not be used in the pilot run of this MM&T contract.

5. Subgroup 5 - Shock & Vibration Tests

Five of the confirmatory samples were shock tested in RCA's Environmental Laboratory, Lancaster, PA using the specified conditions and test method 2016.2.

Following the shock tests, all devices were subjected to a vibration test of variable frequency described in the Specification and Test Method 2056. After the shock and vibration tests, the reverse current measurements at 800 volts and the thermal resistance measurements of Subgroups 2 and 3 of Table 1 were repeated successfully to verify the integrity of the devices. Detail data are listed in Table 6 and the distributions are plotted in Figs. 18 and 19.

The Acceptance Test Procedure required that only two devices be subjected to the Shock and Vibration Tests. Since four different constructions were represented in the sample, RCA subjected a sample of each to the environmental test as follows:

```
HISTOGRAM DATA[;14]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.07 .03 25
VERT SCALE:1
CHAR:POST ENVR REJC
CHARACTERISTIC-POST ENVR REJC
   AVERAGE- 0.1318
   SIGMA--- 0.03871778231
   MAXIMUM- 0.2
   MINIMUM- 0.09
   SAMPLE-- 10
```

No. of Devices

```
  4+ □
  3+ □□
  2+ □□ □
  1+ □□□□
   +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    0 1 1 2 3 3 4 4 5 6 6 7 7
    7 3 9 5 1 7 3 9 5 1 7 3 9
```

Limit
0.2° C/W Max.

Fig. 17 Post Thermal Fatique Thermal Impedance (°C/W)

Histogram Data (12)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.40 .05 25
VERT SCALE:1
CHAR:SH VIR
    CHARACTERISTIC-SH VIR
    AVERAGE- 0.61
    SIGMA--- 0.1392838828
    MAXIMUM- 0.74
    MINIMUM- 0.46
    SAMPLE-- 5
```

No. of Devices

```
  2+ □     □
  1+ □    □□
   +++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . .   . . . . . .
    4 5 6 7 8 9   1 2 3 4 5 6
```

Limit
15 mA Max.

Fig. 18 Post Shock and Vibration Reverse Current, I_r (mA)

Histogram Data (15)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.08 .02 25
VERT SCALE:1
CHAR:FIN ENVR RΘJC
 CHARACTERISTIC-FIN ENVR RΘJC
   AVERAGE- 0.1388888889
   SIGMA--- 0.0805550463
   MAXIMUM- 0.16
   MINIMUM- 0.1
   SAMPLE-- 3
                                  Limit
                                  0.2°C/W Max.
  1+ □ □□
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    0 1 1 2 2 2 3 3 4 4 4 5 5
    8 2 6   4 8 2 6   4 8 2 6
```

No. of Devices

Fig. 19 Post Shock and Vibration Thermal Resistance, $R_{\Theta JC}$ (°C/W

```
      HISTOGRAM DATA[;16]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :3.5 .5 25
VERT SCALE:1
CHAR:DIM A
     CHARACTERISTIC-DIM A
   AVERAGE- 4.744
   SIGMA--- 0.01433720878
   MAXIMUM- 4.761
   MINIMUM- 4.718
   SAMPLE-- 10

 10+  □
  9+  □
  8+  □
  7+  □
  6+  □
  5+  □
  4+  □
  3+  □
  2+  □
  1+  □
   ++++++++++++++++++++++++++
    3 4 5 6 7 8 9 1 1 1 1 1 1
    . . . . . . . 0 1 2 3 4 5
    5 5 5 5 5 5 5 . . . . . .
                  5 5 5 5 5 5
```

No. of Devices

Fig. 20 Statistical Distribution of Dimension A

No. of Devices	Construction
1	Webless Wicked
1	Convoluted Tungsten Button
1	Nonconvoluted Tungsten Button
2	Ion-Implanted

Again all devices passed. The Thermal Resistance data listed for II2 and II3 were measured after the Shock and Vibration Tests.

D. General Data

Table 7 lists a statistical analysis of all the data measured during this confirmatory test. Table 8 lists the key for identifying the individual characteristics. Figs. 20, 21, 22, 23 and 24 show the distribution of the dimensions of the samples.

In addition to the tests discussed, two nonconvoluted devices with tungsten buttons were subjected to two complete thermal shock tests using method 1051.1 and a low temperature of -55°C instead of the specified -25°C. This action results in doubling the number of nonconvoluted tested doubling the number of cycles to 10 instead of 5, and doubling the stress to -55°C instead of -25°C. Both devices passed with flying colors.

S/N	Reverse Current (I_r) mA	Thermal Resistance ($R_{\theta JC}$) °C/W	
J155	0.82	0.1	initial data
	0.1	0.15	after test
J158	0.87	0.09	initial data
	0.1	0.12	after test

V. TEST EQUIPMENT

Refer to the First through Sixth Monthly Reports for this contract for additional information concerning test apparatus. The electrical and environmental test equipment survey listed in the Interim Report for the Engineering Samples repeated and updated here for reference in Table 9.

Table 7

Statistical Analysis of Confirmatory Data

PRODUCT-----CONFIMATORY SILICON TRANSCALENT RECTIFIER DATA						
CHARACTERISTIC	AVG	SIGMA	MAX	MIN	CHI-SQ	N
1	.822	.125	.920	.610	21.20	10
2	2.857	1.732	6.180	1.440	12.85	10
3	.114	.047	.200	.070	18.89	10
4	.988	.025	1.000	.920	19.69	10
5	2.700	.358	3.200	2.000	4.71	10
6	.712	.111	.820	.510	8.26	10
7	.631	.170	.720	.290	23.41	10
8	.654	.102	.720	.460	26.26	10
9	.586	.080	.690	.500	16.37	8
10	.410		.410	.410	2.00	2
11	.410		.410	.410	2.00	2
12	.610	.139	.740	.460	9.71	5
13	.669	.077	.780	.560	14.74	10
14	.132	.089	.200	.090	11.12	10
15	.138	.031	.160	.100	4.30	8
16	4.744	.014	4.761	4.718	8.38	10
17	3.463	.009	3.476	3.447	2.95	10
18	.636	.008	.650	.624	3.82	10
19	1.804	.012	1.834	1.790	12.40	10
20	2.102	.002	2.106	2.100	15.21	10

TUESDAY, OCTOBER 9,1979

Table 8

Key to Statistical Analysis of Table 7

Characteristic #	Definition
1	Reverse Current (I_r) at +25°C
2	Reverse Current (I_r) at +125°C
3	Thermal Impedance $R_{\theta JC}$
4	Forward Voltage (V_{FM})
5	Reverse Recovery Time (T_{rr})
6	Post Surge Test, Reverse Current (I_r)
7	Post Barometric Test, Reverse Current (I_r)
8	Post Blocking Voltage Life Test, Reverse Current (I_r)
9	Post Thermal Shock Test, Reverse Current (I_r)
10	Post Thermal Shock & Moisture Test, Reverse Current (I_r)
11	Post Salt Spray Test. Reverse Current (I_r)
12	Post Shock & Vibration Test, Reverse Current (I_r)
13	Post Thermal Fatigue Test, Reverse Current (I_r)
14	Post Environmental Test, Thermal Resistance ($R_{\theta JC}$)
15	Final Environmental Test, Thermal Resistance ($R_{\theta JC}$)
16	Dimension A
17	Dimension B
18	Dimension C
19	Dimension D
20	Dimension F

TABLE 9

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility
2066	Physical Dimensions	Precision Vernier Calipers and "go-no-go" gauge available.
4016.2	Reverse Current	Facilities available for A.C. Method. Temperature Controlled Oven available.
Par. 4.6.1	Thermal Resistance	Engineering Test Facility available.
4011.3	Forward Voltage	Power Supply and Monitoring available.
4066.2	Surge Current	Surge Fwd. Current and Rev. Voltage Supplies are available.
4031	Reverse Recovery Time	JEDEC Test Circuit developed and test results correlate with RCA, Somerville, NJ, test data. Test equipment is operational.
1001.1	Barometric Pressure (reduced)	Vacuum Chamber and V_r Supply available. Supply modified for half-wave operation.
Par. 4.6.2	Blocking-Voltage Life Test	Oven and Supply are available. Supply modified for half-wave operation.
1051.1	Thermal Shock (Temperature Cycling)	Test facility available at RCA, Lancaster, Environmental Test Laboratory.
1021.1	Moisture Resistance	Ditto
2016.2	Shock	Ditto
2056	Vibration, Variable Frequencies	Ditto

TABLE 9 (Cont.)

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility
1041.1	Salt Atmosphere (corrosion)	Test facility available at RCA, Lancaster, Environmental Test Laboratory.
Par. 4.6.3	Thermal Fatigue Test	Power Supply and Controller are available.

DRT 9/22/78
MFD 1/10/79
MFD 9/25/79

```
      HISTOGRAM DATA[;17]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.9 .5 25
VERT SCALE:1
CHAR:DIM B
     CHARACTERISTIC-DIM B
   AVERAGE- 3.4633
   SIGMA--- 0.00884496090l
   MAXIMUM- 3.476
   MINIMUM- 3.447
   SAMPLE-- 10

 10+    □
  9+    □
  8+    □
  7+    □
  6+    □
  5+    □
  4+    □
  3+    □
  2+    □
  1+    □
   +++++++++++++++++++++++++++
    1 2 3 4 5 6 7 8 9 1 1 1 1
                  . 0 1 2 3
    . . . . . . . . . . . . .
    5 5 5 5 5 5 5 5 5 5 5 5 5
                      5 5 5 5
```

No. of Devices

Fig. 21 Statistical Distribution of Dimension B

```
   HISTOGRAM DATA[;18]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:DIM C
     CHARACTERISTIC-DIM C
   AVERAGE- 0.6363
   SIGMA--- 0.008219894565
   MAXIMUM- 0.65
   MINIMUM- 0.624
   SAMPLE-- 10

  9+    □
  8+    □
  7+    □
  6+    □
  5+    □
  4+    □
  3+    □
  2+    □
  1+    □□
   +++++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Fig. 22 Statistical Distribution of Dimension C

```
      HISTOGRAM DATA[;19]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.5 .3 25
VERT SCALE:1
CHAR:DIM D
     CHARACTERISTIC-DIM D
   AVERAGE- 1.8042
   SIGMA--- 0.011988888874
   MAXIMUM- 1.834
   MINIMUM- 1.79
   SAMPLE-- 10

No. of Devices
  8+      □
  7+      □
  6+      □
  5+      □
  4+      □
  3+      □
  2+     □□
  1+     □□
   ++++++++++++++++++++++++++++
    0 1 1 2 2 3 4 4 5 5 6 7 7
    . . . . . . . . . . . . .
    5 1 7 3 9 5 1 7 3 9 5 1 7
```

Fig. 23 Statistical Distribution of Dimension D

```
      HISTOGRAM DATA[;20]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.5 .1 25
VERT SCALE:1
CHAR:DIM F
     CHARACTERISTIC-DIM F
   AVERAGE- 2.1015
   SIGMA--- 0.002068278941
   MAXIMUM- 2.106
   MINIMUM- 2.1
   SAMPLE-- 10

No. of Devices
 10+       □
  9+       □
  8+       □
  7+       □
  6+       □
  5+       □
  4+       □
  3+       □
  2+       □
  1+       □
   ++++++++++++++++++++++++++++
    1 1 1 2 2 2 2 2 3 3 3 3 3
    . . . . . . . . . . . . .
    5 7 9 1 3 5 7 9 1 3 5 7 9
```

Fig. 24 Statistical Distribution of Dimension F

A. Surge Current Test Set

The surge current test is a survival test which demonstrates that a rectifier is capable of conducting unusually large amounts of current without being destroyed. In the surge test, there are four distinct, sequential circuit functions:

Application of 250 amperes average (400 amperes RMS) of "on" state heating current to bring the rectifier junction to its normal operating temperature,

Application of one 60 Hz, positive, 1/2 cycle high current surge to the DUT,

Application of one 60 Hz, negative, 1/2 cycle reverse high voltage pulse to the DUT.

The above test sequence of operations is repeated at one minute intervals for 10 total surges.

The repetitive surge current test is shown in Fig. 25. The circuit block diagram is illustrated in Fig. 26. Three power supplies are also involved in this test of DUT's ability to withstand overloads. Sequencing on the exact half or full 60 Hz cycle is designed into the equipment. High voltage interlocks are used for safety of the operating personnel.

An a.c. heating current supply heats the DUT to its normal operating temperature before a second supply applies a single, half cycle forward current surge to the DUT. On the subsequent half cycle, an 800 volt peak reverse a.c. voltage is applied to test whether the device has retained its blocking capability following the surge. This surge sequence is repeated ten times at one minute intervals. All parameters are recorded temporarily on a storage oscilloscope for approximately 10 ms.

Other test conditions, such as higher peak surges, lower reverse voltages and different time intervals can be set up, if desired. Forced air cooling is utilized.

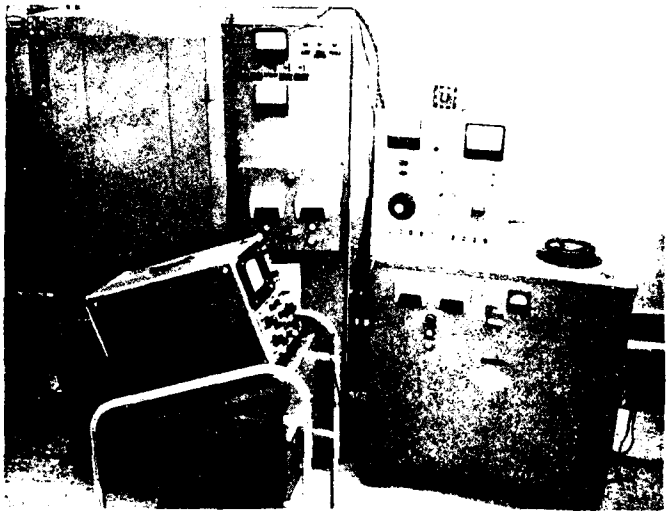


Figure 25 Repetitive Surge Current Test Set. The DUT was mounted inside the interlocked door on the left in the photograph.

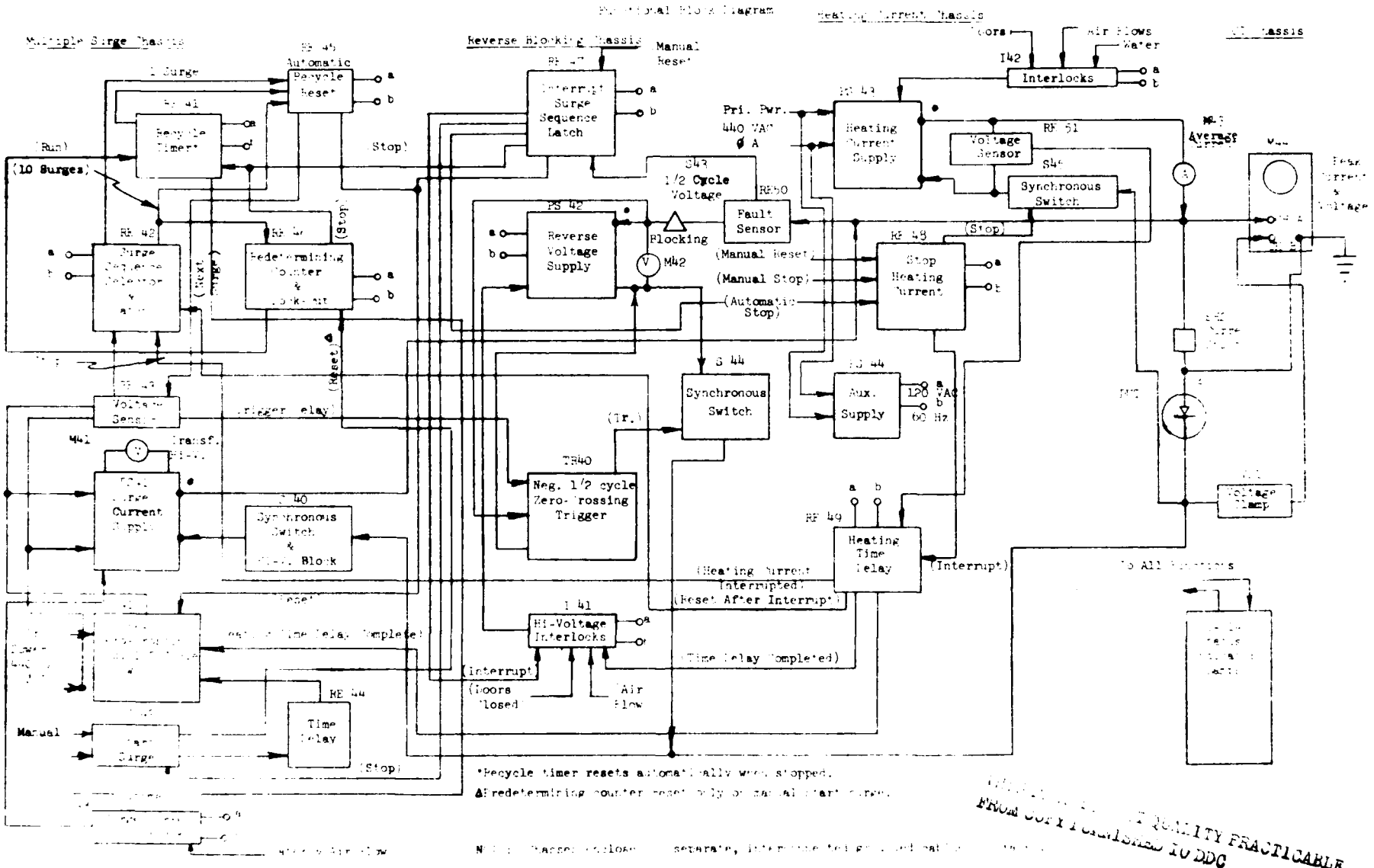


Figure 26

B. Forward On-State Voltage Test Set

In the forward on-state voltage test the peak forward voltage drop is measured while the rectifier is conducting its rated current. At the same time the operation of the heat-pipes is confirmed.

The test set shown in Fig. 27 applies the full rated average a.c. current to the DUT. The cooling air flow is adjusted to achieve the required 100°C on the case of the heat-pipe of the DUT before the peak forward voltage is read on the oscilloscope. A functional block diagram of the circuit is shown in Fig. 28.

During this test the temperature is measured at several points along the heat-pipes. In this way, the heat-pipes' thermal balance and isothermal characteristics can be verified. A poorly functioning heat-pipe is not isothermal. Properly functioning heat-pipes are important not only for the reliability of the DUT, but also because the on-state voltage is a function of the junction temperature.

C. Thermal Fatigue Test Set

Rectifiers are temperature cycled by operating them in a circuit in which the devices are heated by conducting their full rated current of 250 A average and cooled by blowing room temperature air across the fins on the device. The test is conducted for a minimum of 200 cycles. The test set is shown in Fig. 29 along with the functional block diagram of the circuit in Fig. 30. The air flow is adjustable to assure that the specified minimum and maximum (min. $T_C = 30 \pm 10^{\circ}C$, max. $T_C = 90 \pm 10^{\circ}C$) temperatures are achieved on every cycle. A recorder connected to a thermocouple attached to the rectifier is used to verify not only the temperature range, but also the number of cycles.

D. Blocking Current Test Set

The blocking current test set is used to measure the leakage currents of the reverse blocking junction. The test set along with the functional block diagram of the circuit are shown in Figs. 31 and 32, respectively. The reverse blocking (leakage) currents are measured at the full rated a.c. voltage of 800 volts peak. These currents are measured at both room temperature (25°C) and at the maximum rated temperature (125°C) of the Device Under Test (DUT).

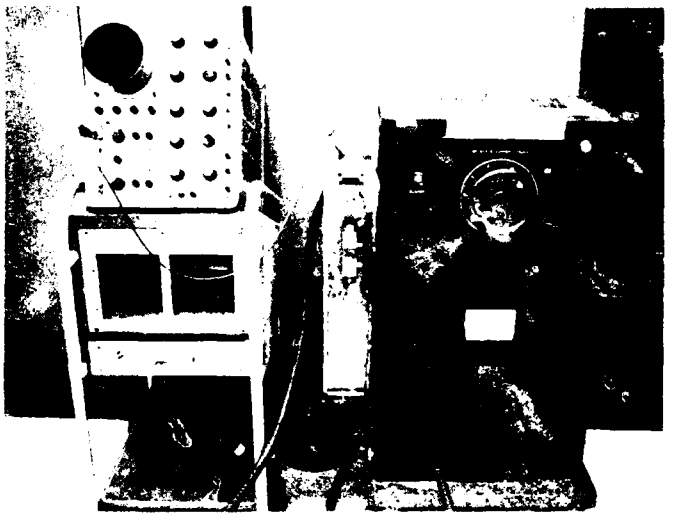


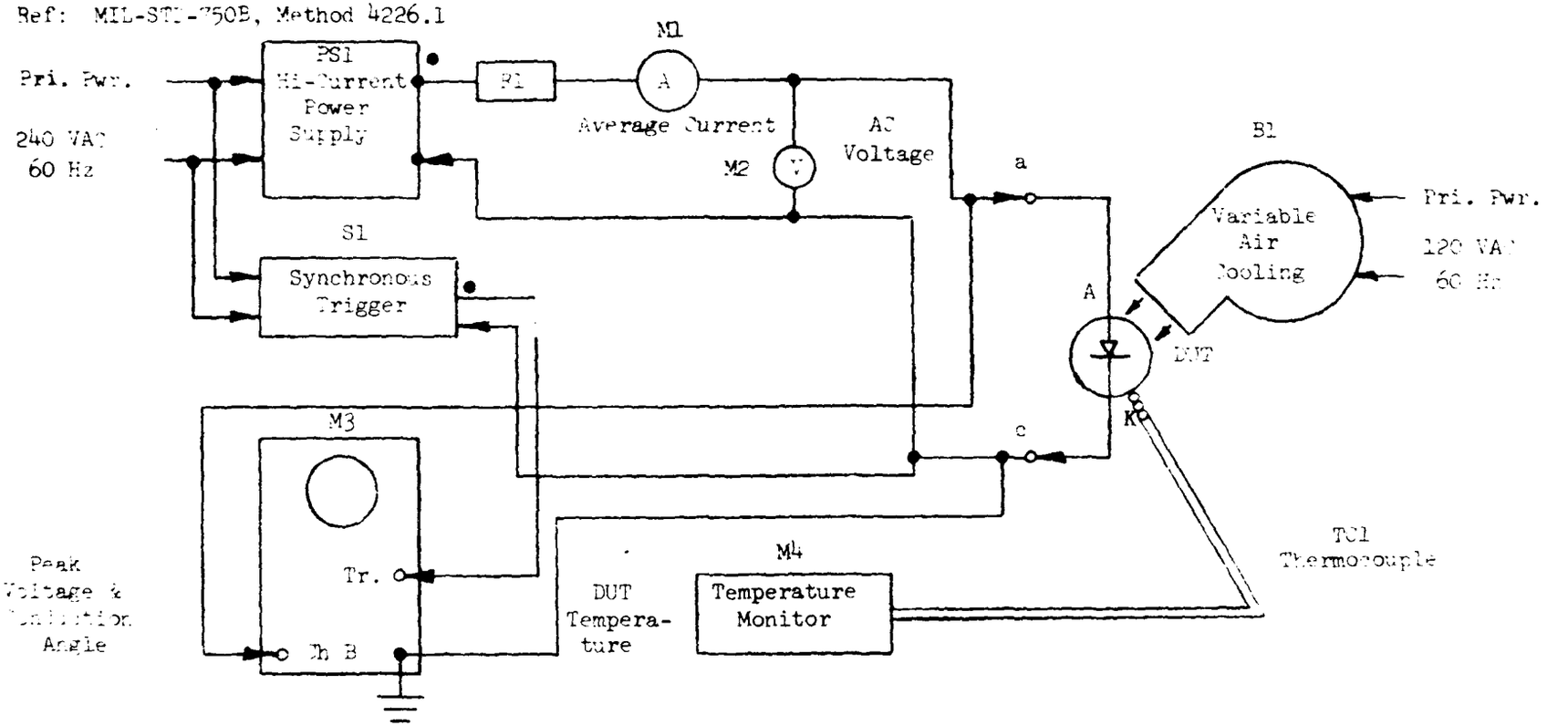
Figure 27 Forward On-State Voltage Test Set. The DUT was mounted at the top of the cooling air duct in the center of the photograph.

Figure 28 Forward "ON" Voltage Test Set - Portable

1/12/77 RER
1/10/79 MFD

Block Diagram

Ref: MIL-STD-750B, Method 4226.1



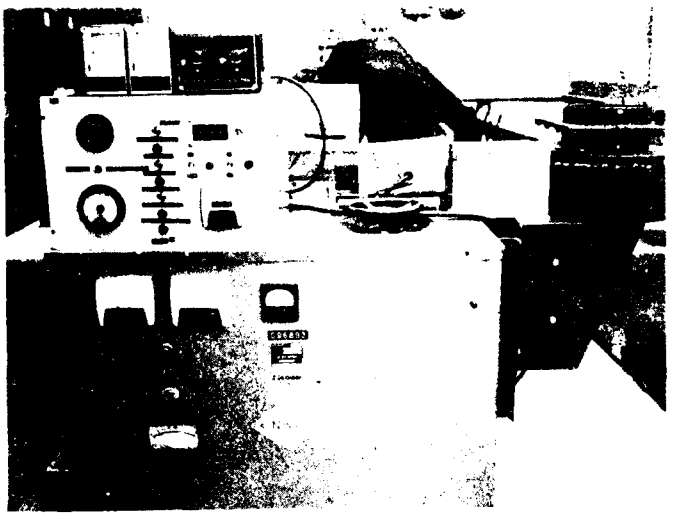


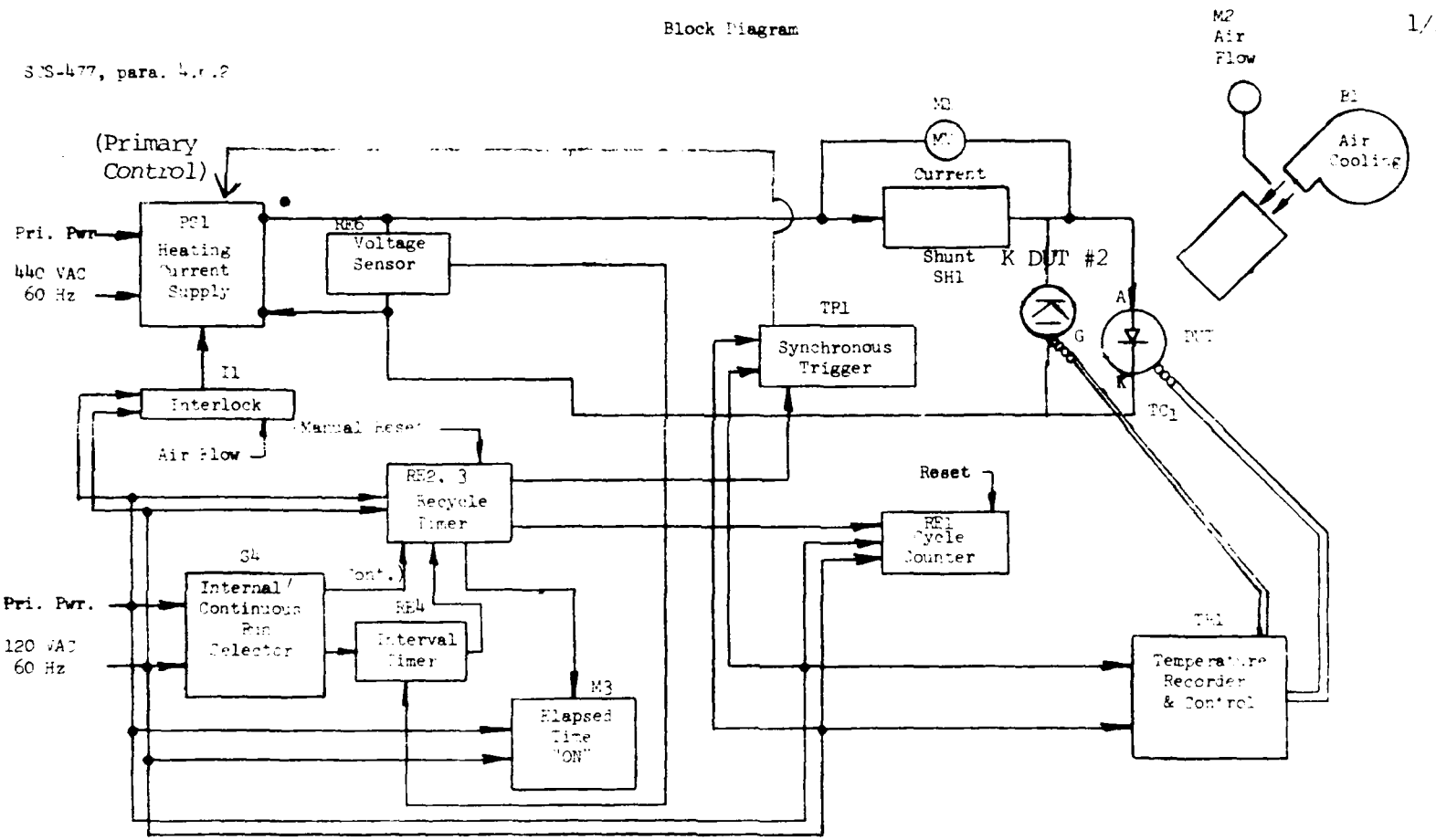
Fig. 29 Thermal Fatigue Test S
The DUT's
of view i
Gold
back of the

Figure 30 Thermal Fatigue Test Set

Block Diagram

1/10/79 MHD

Ref S/S-477, para. 4.r.2



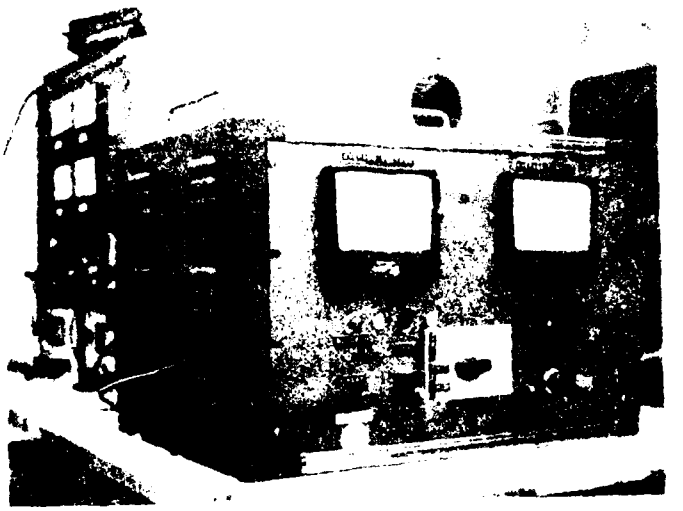
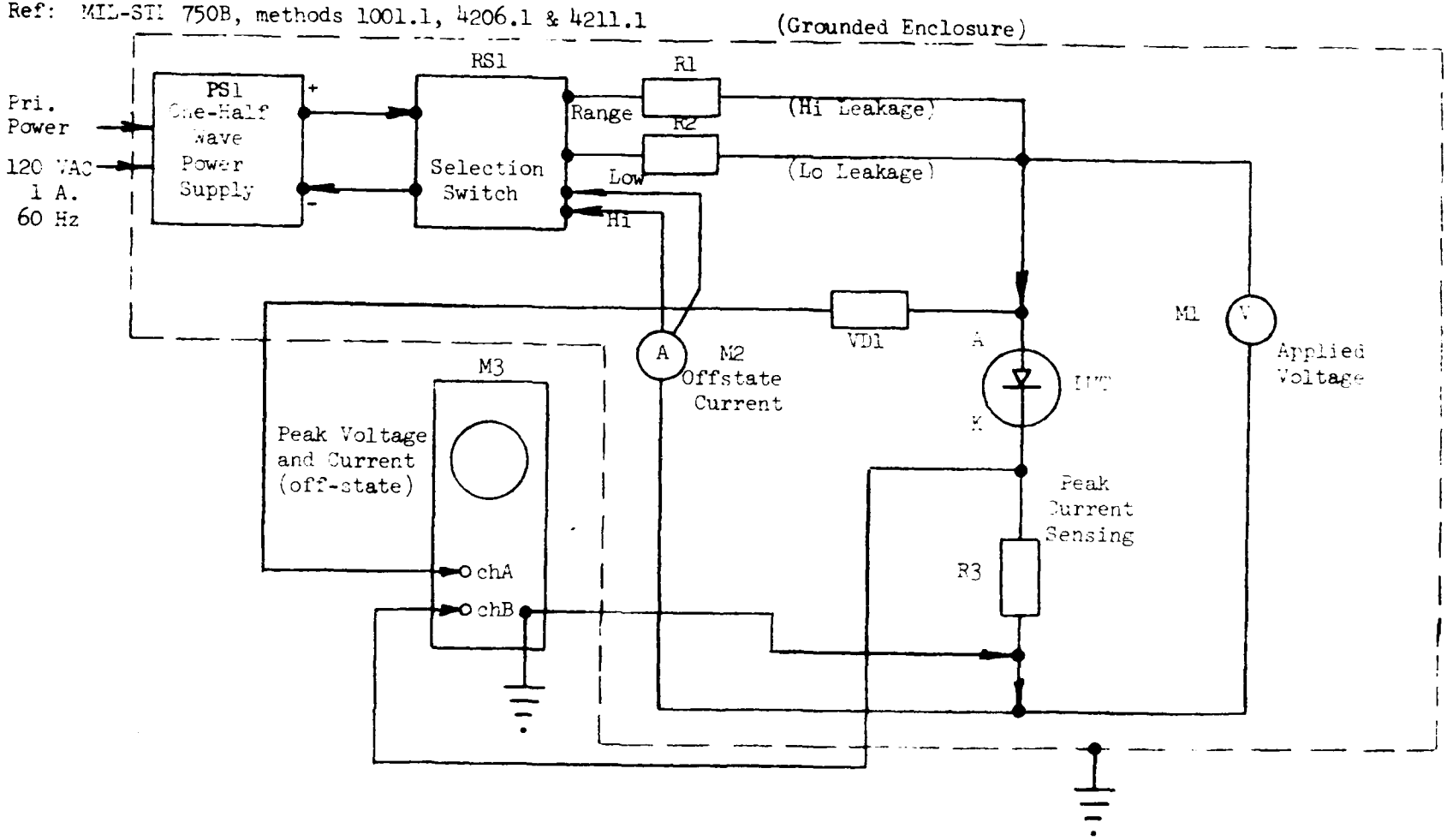


Fig. 3 i Blocking Current [illegible]
This set was used [illegible]
temperature as well as [illegible]
comparable with [illegible]
or a vacuum system [illegible]
shown) for the high temperature and radiation [illegible]
metric pressure [illegible]
Reverse blocking [illegible]
and measured with [illegible]
equipment.

Figure 32 Reverse Blocking Current Test Set - A. C. Method 1/7/77
RER

Block Diagram

Ref: MIL-STD 750B, methods 1001.1, 4206.1 & 4211.1



The measurement is performed by monitoring the voltage drop across a calibrated resistor in series with the DUT. This enables an oscilloscope to be used to measure the peak current since the oscilloscope is a voltage rather than a current measuring device. Ohm's law converts the reading to the current.

E. Blocking Voltage Life Test

Rectifiers are life tested for 200 hours by subjecting them to reverse blocking voltages of 800 volts while at a temperature of 125°C. A 60 Hz 1/2 wave AC power supply is used for voltage power. The test set is shown in Fig. 33 and the functional block diagram is shown in Fig. 34.

Metering within the test set provides the temperature of the DUT, elapsed time, voltage and current. A jack is provided for the measurement of the peak voltage with an oscilloscope. Indicator lamps and high voltage fuses are included in the power supply to indicate whether a DUT has failed to block the high voltage during the tests. The test set is designed to test six devices simultaneously.

The power supply is connected through a voltage regulator to the primary power lines of the high temperature oven. In this way, the power and timing are removed from the DUT in the event of a power interruption that would reduce the oven temperature below the test value. An interlocked oven door also removes the high voltage from the DUT when the oven door is opened, thus, protecting the personnel.

This power supply is also used for the Reduced Barometric Pressure test for half wave voltage application to the DUT in the vacuum chamber.

F. Thermal Resistance Test Set

The thermal resistance test set is used to determine the thermal resistance between the junction and the base of the fins on the heat-pipe.

Prior to testing the rectifier, each device is calibrated by recording the forward voltage (V_F) drop at 4.0 A as a function of temperature. At each selected temperature, sufficient time is taken to insure that the junction, the heat-pipes and the oven are all in thermal equilibrium. At 4.0 A, V_F versus temperature is interpreted from measurements of the V_F at temperatures between the selected temperatures.

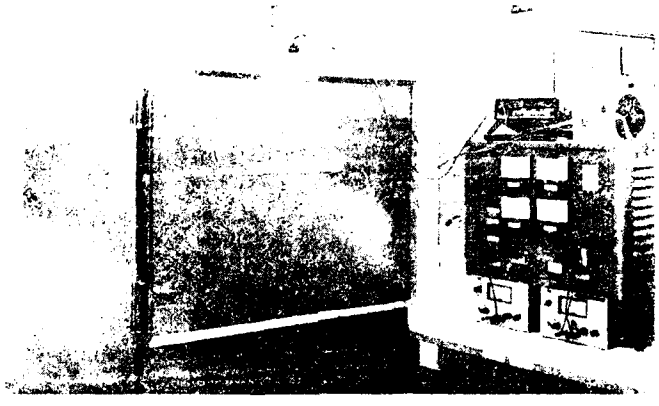


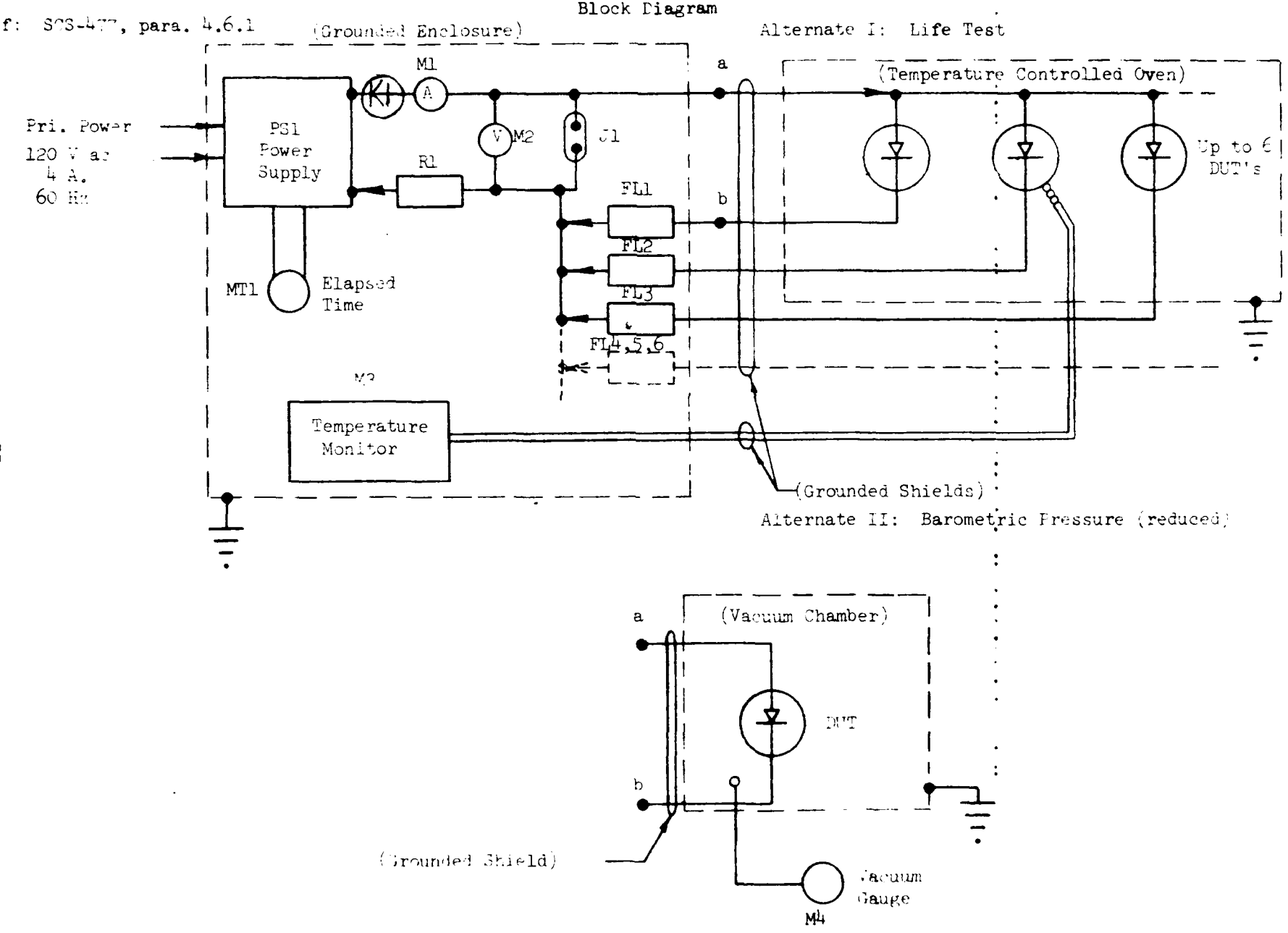
Fig. 33 Blocking Voltage Life Test Set including the temperature controlled oven. This oven is also used for the other high temperature tests.

1/7/77 RER
1/10/79 MFD

Figure 34 Blocking Voltage Life Test/Barometric Pressure Test Set

Block Diagram

Ref: SCS-477, para. 4.6.1



It is this characteristic of V_F versus temperature at 4.0 A which is employed to determine the junction temperature during the thermal resistance test. The difference between the junction temperature and the case temperature, which is measured with a thermocouple attached to the outside wall of the heat-pipe, divided by heating power is the thermal resistance.

When a rectifier is tested it is heated by passing rated current through the device. This heating current is interrupted every 50.0 ms for about 0.5 ms. During the interruption, the V_F is measured at the calibration current of 4.0 A.

The test set is shown in Fig. 35. Fig. 36 is a functional block diagram of the circuit.

The thermal resistance of the Transcalent rectifier is a function of dissipation power and ambient temperature.

VI. CONCLUSION AND RECOMMENDATIONS

The confirmatory sample phase of the program has been successfully completed on schedule as stipulated by the program evaluation chart (PERT). See Int. Tech. Rept. Jan. 1979.

No particular difficulties were involved in this phase of the program, and we are ready to proceed with the pilot run program when permission is obtained. It is suggested that this approval be given as early as possible so that this work can proceed on schedule.

We shall proceed with the preliminary pilot run report as quickly as possible since we recommended that a pilot run demonstration be given early in the pilot production run. This approach has the advantage of many parts and subassemblies being available to demonstrate sequential operations in a short amount of time.

All drawings and procedures will be updated to reflect the final design for the pilot run, namely, standard doped, webless wick and nonconvoluted cathode strain isolation rings. The reasons for the final design have already been discussed and verified in the body of this report.

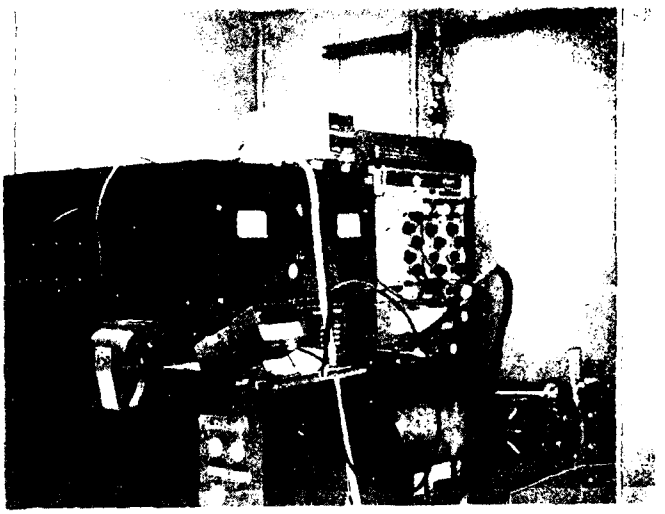


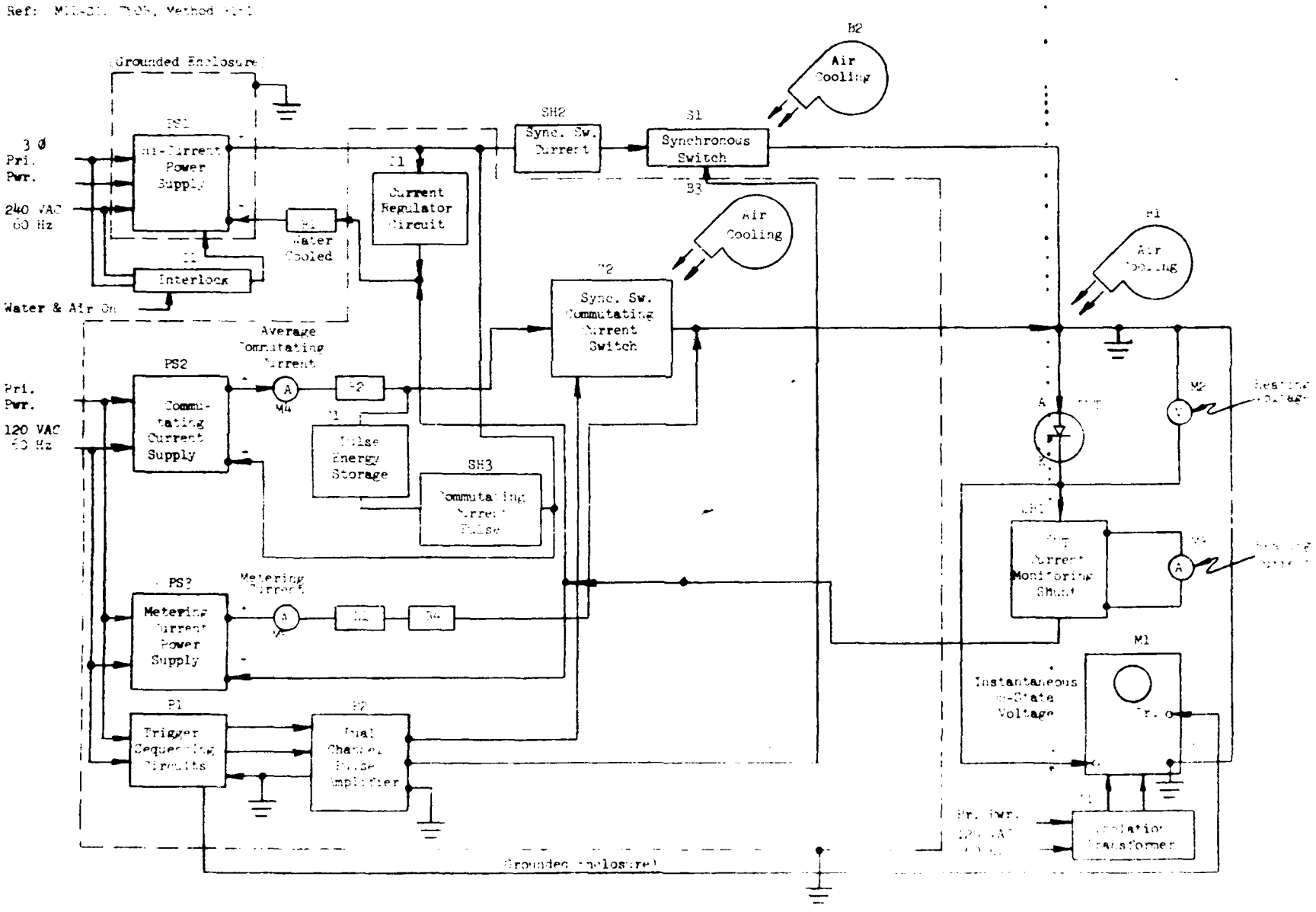
Fig. 35 Thermal Resistance Test Set. The DUT is mounted in the end of the cooling air duct shown in the foreground.

Figure 36 Thermal Resistance Test Set

Block Diagram

1/10/79 MFD

Ref: MIL-STD-750, Method 3101



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