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A SIGNAL DELAY UNIT FOR TOA DIRECTION-FINDING EVALUATION.(U)
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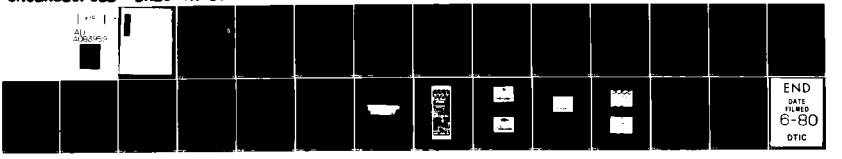

RESEARCH AND DEVELOPMENT BRANCH

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DEPARTMENT OF NATIONAL DEFENCE
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DEFENCE RESEARCH ESTABLISHMENT OTTAWA

TECHNICAL NOTE NO. 80-5

A SIGNAL DELAY UNIT FOR TOA DIRECTION-FINDING EVALUATION

by

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COM EW Section
Defence Electronics Division

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ABSTRACT

A Signal Delay Unit (SDU) was developed to provide differentially delayed baseband signals for laboratory evaluation of an experimental Time of Arrival (TOA) direction-finding system.

The SDU is a completely self-contained unit employing a tapped Bucket Brigade Device (BBD) delay line to realize up to four independent differential signal delays of from one to 256 microsecconds.

RÉSUMÉ

Une unité à délais du signal a été developpée pour fournir des sorties différentielles de bande latéralle retardées pour évaluer en laboratoire un systéme de radiogoniométrie basé sur le temps d'arriver du signal.

L'unité à délais est complétement autonome et utilise des lignes à délais dans une configuration "Bucket Brigade Device" pour réaliser jusqu'à quatre signaux différentiels indépendants, retardées de une à 256 microsecondes.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

1.0 INTRODUCTION

A Signal Delay Unit (SDU) was designed at DREO to meet the requirements for testing an experimental Time of Arrival (TOA) emitter location system. In the land tactical environment, using a DREO type of TOA system, one can expect the time difference of arrival of signal between two antennae to be as large as one hundred microseconds. Unfortunately, a large number of factors may influence the measured time delay in a practical situation. Therefore, before field trials one should perform repeatable laboratory simulations to evaluate the system hardware limitations.

Traditional approaches to the implementation of a delay line suffer serious shortcomings in this type of application. Generally, the delays achievable with acoustic or transmission line techniques are very short and difficult to control.

Linear phase delay active filters may be used, but these are sensitive to component variations, and lack flexibility. A/D conversion with digital storage and subsequent D/A conversion remains an effective solution, but incurs a substantial hardware overhead.

Recent developments in Charge Transfer Device (CTD) technology, in particular, the availability of practical Bucket Brigade Devices (BBDs) and Charge-coupled Devices (CCDs) offer many advantages. These advantages include the following:

Flexibility - A wide range of delays can be accommodated by using appropriate signal taps and selecting a suitable clock frequency.

High Stability- The delay in a CTD is an integral multiple of the clock period which can be made extremely stable by using a crystal or other precision oscillator

Low Cost - The CTD approach can be implemented with commercially available CTDs requiring only minimal support circuitry.

2.0 CONCEPTUAL APPROACH

Figure 1 gives the basic conceptual approach to the implementation of a delay line. The design is based on the sample and hold operation which is fundamental to the theory of CTDs. Referring to Figure 1, switch S_1,

under the control of clock signal ϕ_1, periodically closes; capacitor C_1 acquires the potential of the input signal on each switch closure, thereby implementing a sample and hold operation. Between switch closures which are initiating by ϕ_1, S_2 closes under the control of ϕ_2 and capacitor C_2 acquires the potential on C_1.

After one complete clock cycle the input signal potential that existed at the beginning of the cycle has been transferred to capacitor C_2. Consequently, it has been delayed by the duration of one clock cycle.

The pair of sample and hold circuits constructed from capacitors C_1 and C_2, switches S_1 and S_2, and the two associated buffer amplifiers therefore constitute one stage of the analog shift register or clocked delay line.

It is possible to cascade additional delay stages to obtain much longer delays. By inspection, the total delay of such a shift register is the product of the clock period and the number of delay stages.

There are then two ways of varying the delay, that is, to vary the clock frequency and/or vary the tap location used in the shift register to recover signal samples. The ability to obtain several different delays simultaneously from one delay line, by using different taps, is a valuable technique.

It should be noted that since the clocked analog shift register is a sampled data system; it shares their inherent limitations. These include the nyquist limit for input signal bandwidth, the $(\sin \chi)/\chi$ high frequency roll off and the need for low-pass filtering of the output to recover the baseband output signal. Also, without ideal circuit elements, there is a finite limit to the useable storage time in each sample and hold stage, thereby placing restrictions on the lower clock frequency limit. In practical CTDs, there is a dispersion effect resulting from the incomplete transfer of signal samples between delay stages. It has been shown [1] that this interaction between samples leads to an additional phase shift of

$$\Delta\phi = (n\epsilon \ \ \text{Sin}\ 2\Pi\ f/f_c) \qquad (1)$$

and a low-pass filter amplitude response of

$$|H(f)| = \exp\ [\ -n\epsilon\ (1 - \text{Cos}\ 2\Pi\ f/f_c)] \qquad (2)$$

where, ϵ is the transfer inefficiency, which refers to the fraction of signal left behind on each transfer operation, f_c is the clock frequency and n is the number of delay stages.

These effects can be minimized by using a high clock frequency and/or minimizing the number of transfers, where this is feasible.

3.0 IMPLEMENTATION OF A DELAY LINE

The delay line implementation using sample and hold circuits, although realizable with discrete components, is very unsatisfactory from the viewpoint of integrated circuit technology. This is because it requires a precision unity gain buffer amplifier in each stage.

This requirement is avoided in the CTD technology by making use of clock-induced electric fields to transfer nearly all of the charge stored in an integrated storage capacitor to the storage capacitor of the next stage.

Charge transfer devices may be implemented as Charge-Coupled Devices (CCDs), Bucket Brigade Devices (BBDs), and Single Transfer Devices (STDs). For analog signal processing applications, BBDs are currently most popular; they represent a straightforward realization of a delay line using conventional MOSFET* technology. In BBD technology, Figure 2, MOSFET transistors are used as voltage controlled switches, a role for which they have nearly ideal characteristics, limited only by a rather appreciable "ON" state resistance. The storage capacitors are realized by the source/drain capacitances inherent in the MOSFET structure.

The virtually complete transfer of charge is accomplished by using a capacitive coupling between the clocks and the drain/source diffusion on the side of the MOSFET corresponding to the direction of charge flow. When the MOSFET is switched "ON" by the clock going high (positive for n-channel technology), the capacitive coupling forces this floating source/drain diffusion positive, thereby inducing the majority carriers to flow from the previous stage. This capacitance is obtained by overlapping the gate and the appropriate source/drain diffusion.

The CTD used in the DREO Delay Unit is the Reticon TAD-32A, a 32 stage BBD fabricated in n-channel silicon technology. Signal samples at each stage are sensed by source follower amplifiers for external availability. This is useful in applications where several different delays are simultaneously required, with the restriction that they will be integral multiples of the clock period up to 32.

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*Bipolar transistors and JFETs have been used but have significant disadvantages.

The TAD-32A can use clock frequencies from 1 KHz to 5 MHz. This provides greater than a three decade range of delays by varying the clock frequency, in addition to the 1:32 range obtainable by tap selection.

4.0 DELAY UNIT ORGANIZATION

The TAD-32A BBD requires analog and digital support circuitry for operation. This support circuitry may be broken down into the following functional blocks:

1) Clock Generator (composed of crystal oscillator, frequency pre-scaler and phase splitter).

2) Input Buffer Amplifier.

3) Output Buffer Amplifier(s).

4) Power Supply

Their organization in the DREO Delay Unit is illustrated in Figure 3.

Delays are varied by two methods: clock frequency pre-scaling by 2^{-n} where, n is 1, 2, 3 or 4 and by tap selection from the 32 stages of the TAD-32A. The frequency pre-scaling yields a choice of clock frequencies including 1 MHz, 500 KHz, 250 KHz and 125 KHz corresponding to delays of 1 μs, 2 μs, 4 μs and 8 μs per tap. This allows a range of delays from 1 μs to 256 μs in increments ranging from 1 to 8 μs.

Up to four signal delays are simultaneously available through the use of the four output buffer amplifiers which can be connected to any of the TAD-32A output taps via a patch board.

5.0 DELAY UNIT SUPPORT CIRCUITRY

The design and analysis of the Delay Unit support circuitry is now presented.

5.1 Clock Generator

With clocked delay lines, such as the TAD-32A, the performance of the clock generator circuitry is very important. Since the signal delay will be essentially an integral multiple of the clock period, a stable delay requires a correspondingly stable clock oscillator. If additional control over the delay interval is desired, a programmable clock frequency is necessary. The clock waveform itself must have suitable amplitudes, rise and fall times, and in the case of the TAD-32A and many other CTDs, should be a symmetrical, overlapping, two phase square wave.

The clock generator of Figure 4 fulfills these requirements using the TAD-32A. It consists of four distinct blocks; a crystal oscillator, a frequency pre-scaler, a phase splitter and a clock driver.

The logic is implemented with TTL except for the clock driver which must provide a 15 volt clock swing.

A 74S124 oscillator IC is used with a 4 MHz crystal to generate the master clock. A π network of 27 pf capacitors was required with the crystal to ensure stable oscillator operation. Due to the frequency division by two in the phase splitter and the frequency pre-scaler ($\div$ 2 setting) the maximum clock frequency for the TAD-32A is 1 MHz. This results in a minimum delay of 1 μs per tap.

The frequency pre-scaler consists of a conventional TTL four bit synchronous binary counter, the 74163.

The phase splitter is a Shottky TTL D-type flip-flop connected as a $\div$ 2 counter. The Q and $\bar{Q}$ outputs provide the two clock phases required for TAD-32A operation, the flip-flop design assuring a sufficient degree of symmetry.

The clock driver uses the MH 0026 dual clock driver which can be driven by TTL levels when (capacitively coupled) and is designed for an output swing that approaches within one diode drop of the 15 volt supply voltage.

The 47 Ω resistors in series with each output suppress ringing. The inductance of the clock lines and the load capacitance comprise a series LC resonant circuit that can be damped by series resistance. Potentiometer P_1 allows the clock output high levels to be balanced for optimum TAD-32A operation.

5.2 Input Buffer Amplifier

The primary purpose of the input buffer amplifier is to provide isolation between the signal source and the TAD-32A BBD.

The TAD-32A has a high input impedance since a relatively small signal current can quickly change the integrated storage capacitor of the first delay stage to a significant voltage. However, the existence of a

small feed through capacitance between the gate and source/drain input of the input MOSFET transistor switch means that a low driving impedance is essential if clock induced noise is to be minimized on the signal source. An area of recurrent difficulty in the design of analog CTD circuits is the isolation of the clock circuits from the signal path. In general, this implies that low impedance analog I/O circuitry should be used in combination with layout precautions that will maximize the separation between clock and analog circuitry.

Since the TAD-32A is specified for an input signal level of ~ 3V P-P, for maximum signal-to-noise performance consistent with reasonable linearity, it was felt that an input buffer amplifier of unity gain would be compatible with operational requirements. Consequently a 2N3819 junction field effect transistor was selected in a source-follower configuration to resolve the input buffer requirements (Figure 5).

A source follower stage has wide bandwidth, low phase shift, and a low output impedance. It is therefore almost ideal for the input buffer amplifier.

Potentiometer P_1 provides a master gain control for the delay unit and largely determines the input impedance, which is about 10 K ohms. The output from the source follower is capacitively coupled to the analog input of the TAD-32A. Potentiometer P_2 is used to set the bias level to a nominal value of 5 volts DC.

5.3 TAD-32A Output Buffer Amplifier

The TAD-32A output taps should be loaded by a very low impedance to minimize coupling interactions between taps, and to maintain the phase and frequency integrity of the output signal. Consequently, a suitable output buffer amplifier is required to permit the interface of the TAD-32A in signal processing systems. An appropriate buffer amplifier must have an excellent frequency and phase response, low input and output impedances, voltage gain, and provide a reasonable DC operating point for the source follower tap outputs of the TAD-32A.

In addition, the output buffer amplifier should be relatively economical to implement since one is required for each desired signal delay. In the Signal Delay Unit up to four delays were required. These requirements are satisfied by the two stage amplifier illustrated in Figure 5, which utilizes a common base amplifier for a low input impedance and high voltage gain, directly coupled to a common collector (emitter follower) output stage to realize a low output impedance. Both the common base and common collector amplifier configurations are characterized by a wide bandwidth and good stability when implemented with modern silicon planar transistors. This is an important consideration in view of the fast rise and fall times needed for a time-sampled signal.

Transistor Q_1, connected as a PNP common base amplifier has a very low input impedance ($<< 1$ KΩ) and provides a DC path for the quiescent operating current of the source follower, tap outputs, of the TAD-32A. The

operating point of Q_1 is determined by variable resistors P_3 and P_4. P_4 sets the base bias voltage (and consequently the quiescent emitter voltage) of Q_1 while P_3 defines the load line slope and thus determines the operating point and voltage gain of Q_1 in conjunction with P_4. P_4, in setting the quiescent emitter voltage of Q_1, sets the quiescent gate-source and source-drain voltages on the corresponding TAD-32A tap output source follower. To ensure linear operation of the tap output source follower, it is desirable to set P_4 for a quiescent emitter voltage on Q_1 of 5V DC. The gain of the output buffer amplifier is normally adjusted for an overall system gain of $\frac{1}{2}$.

The diode-connected transistor, Q_2, provides temperature compensation for Q_1. Q_3 is a conventional PNP emitter follower stage with near unity voltage gain and a low output impedance. The use of a PNP transistor avoids the possibility of Q_3 being cut off by large signal swings approaching ground at the collector of Q_1. 2N4403 PNP transistors were selected because of their high current, gain-bandwidth product, linearity and low cost.

As the Delay Unit does not include a low-pass filter on the output, it is necessary to use an external low-pass filter to recover the baseband signal from the time-sampled output. This was not included since mis-matches between low-pass filters would introduce differential delays between the outputs that would be difficult to compensate.

5.4 Power Supply

Two different supply voltages are required in the delay unit, namely, + 15V DC. for the TAD-32A BBD and the associated 0026 TTL to MOS level translator, and + 5V DC. for the clock generator (TTL) logic.

These requirements are readily satisfied by the circuit of Figure 6 which consists of a full wave bridge rectifier and the appropriate IC voltage regulators. The use of the transformer centertap to provide half of the unregulated output voltage to the 5 volt regulator IC reduces the power dissipation of this IC, thereby relaxing its heat sink requirements.

The IC regulators used have thermal overload protection and current limiting as well as high performance. The analog input bias voltage and V_{bb} for the TAD-32A are obtained by using resistor divider networks on the 15 volt power supply.

5.5 Delay Unit Construction Details

The DREO Delay Unit was designed to occupy a 5¼" height in a standard 19" rack. All controls are located on the front panel while I/O connections are made on the back via BNC connectors, as shown in Figure 7. The Delay Unit electronics is fabricated on a printed circuit board which is mounted on the front panel. A half size PC board layout is presented in Figure 8. The rear cover of the Unit is mounted by four screws and is easily removed for servicing since only the I/O cables constitute the physical connection.

6.0 PERFORMANCE OF THE DELAY UNIT

Measured performance gave a frequency response of 19 Hz - 25 KHz, within 0.5 dB, for the minimum clock frequency of 125 Khz and an input level of 1V peak. Higher clock frequency settings will extend the high frequency response.

Figures 9-11 illustrate the harmonic distortion performance as a function of input level. For inputs up to 2V P-P, all harmonics are over 40 dB below the fundamental, and the noise floor is over 60 dB below the 2V P-P input level.

The output waveforms from the SDU for 2 KHz sinewave and triangle wave inputs are illustrated in Figures 12 and 13 respectively. Output waveforms (a) and (b) are the unfiltered signals obtained from the buffered output taps 1 and 25 respectively of the TAD-32A BBD. Since the clock frequency was set to 125 KHz, the differential delay per tap is 8 μS for a total differential delay of 192 μS. The high frequency components in waveforms (a) and (b) are filtered out by 6 pole Bessel lowpass filters (f_c = 5 KHz) to yield waveforms (c) and (d).

The only critical aspect of the Delay Unit is the necessity of using a low-pass filter, with excellent transient response, to recover the base-band signal from the time-sampled output wave forms.

7.0 REFERENCES

1. Seguin and Tompsett, Charge Transfer Devices, 1975. p.p. 76.

2. Ibid, p.p. 76.

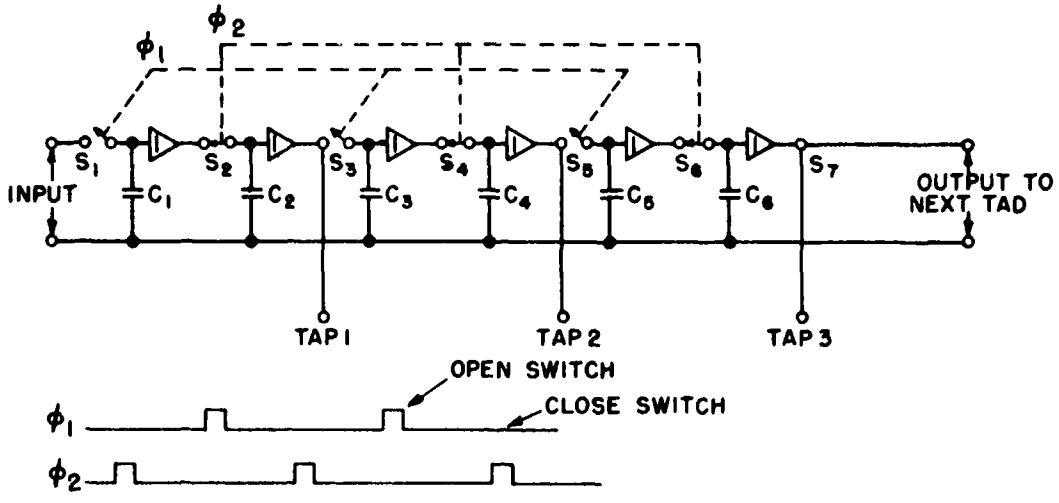


FIGURE 1 - A TAPPED ANALOG DELAY LINE MADE WITH SAMPLE AND HOLDS

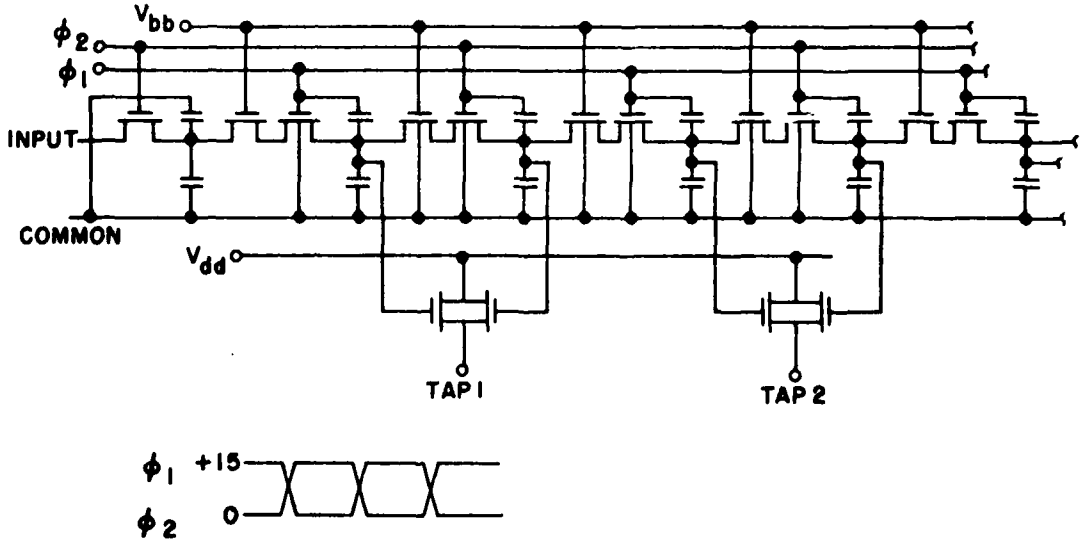


FIGURE 2 - A TAPPED ANALOG DELAY LINE MADE USING METAL-OXIDE-SILICON INTEGRATED CIRCUIT TECHNOLOGY

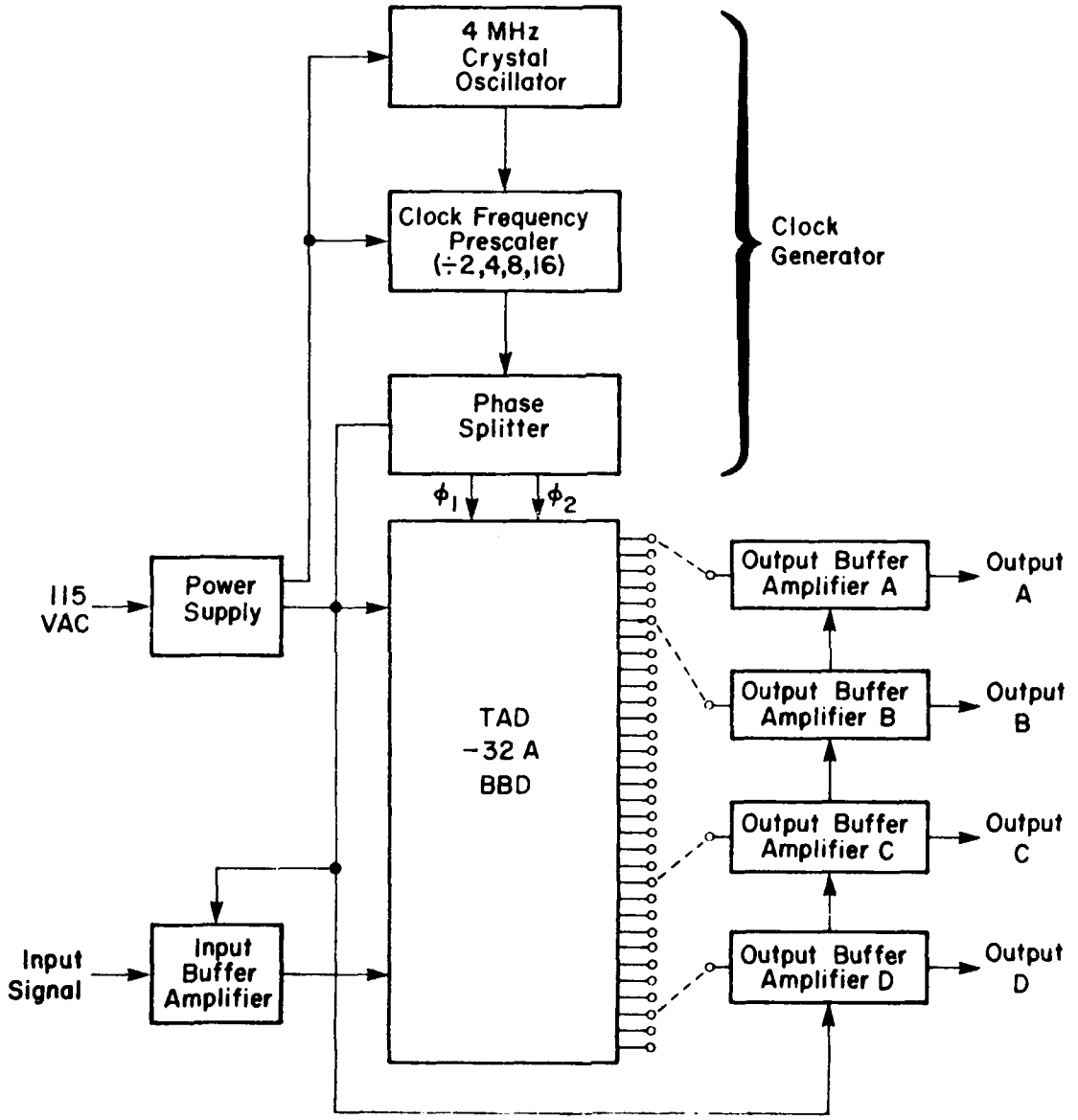
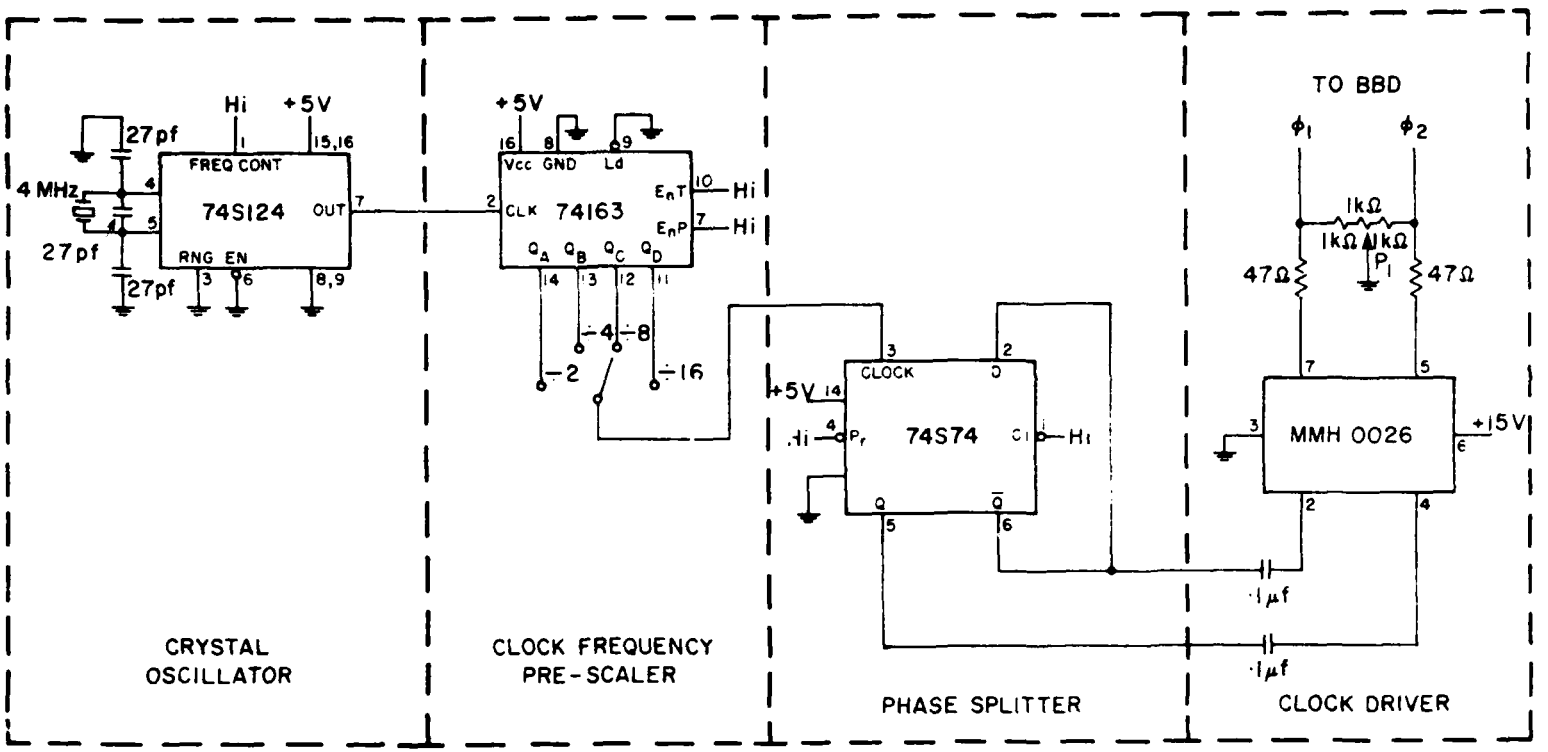


FIGURE 3 - SIGNAL DELAY UNIT ORGANIZATION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+5V
27pf
FREQ CONT
74S124
OUT
4 MHz
RNG EN
27pf
27pf
+5V
Vcc GND Ld
CLK 74163
Hi
Hi
÷2
÷4
÷8
÷16
+5V
Hi
CLOCK
74S74
Hi
TO BBD
ϕ1
ϕ2
1kΩ
1kΩ
1kΩ
P1
47Ω
47Ω
MMH 0026
+15V
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CRYSTAL OSCILLATOR
CLOCK FREQUENCY PRE-SCALER
PHASE SPLITTER
CLOCK DRIVER

FIGURE 4

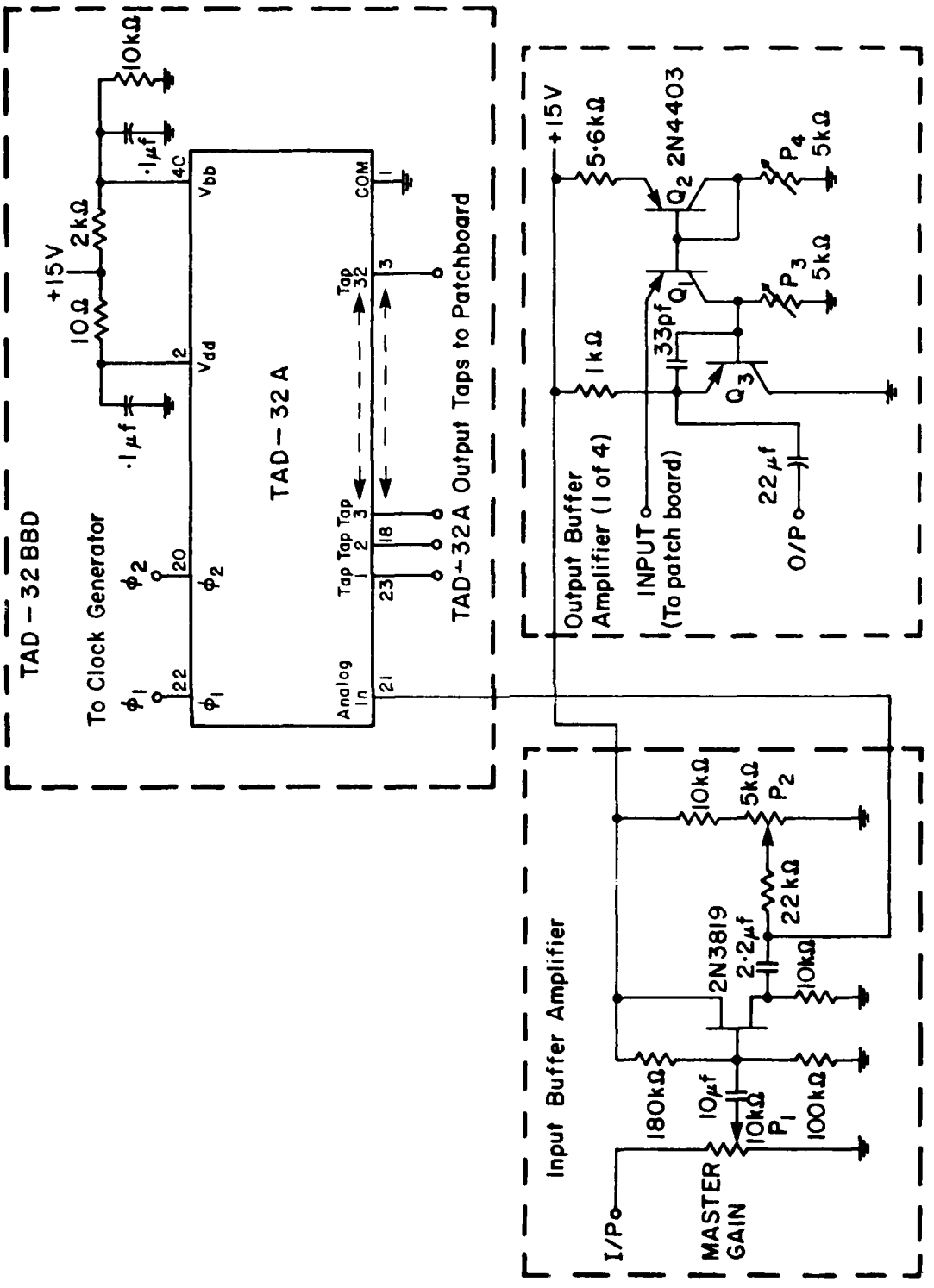


FIGURE 5 - TAD-32 BUCKET BRIGADE DEVICE AND ANALOG SUPPORT CIRCUITS

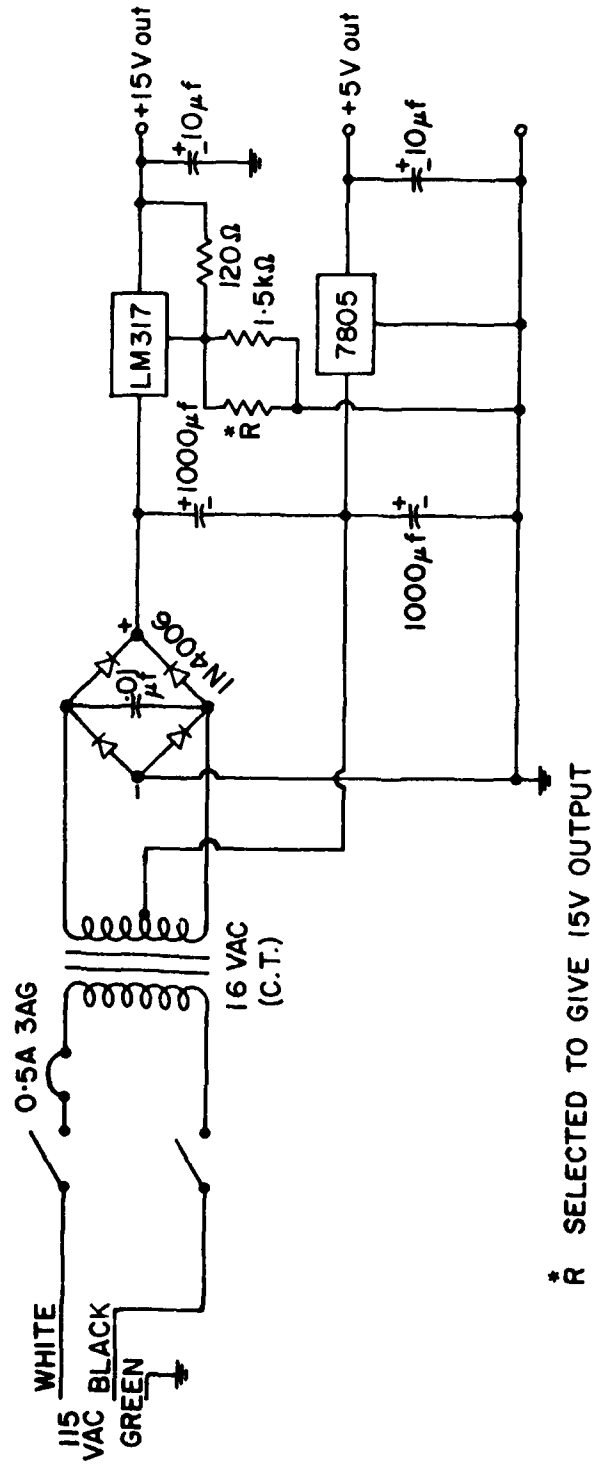


FIGURE 6 - SIGNAL DELAY UNIT POWER SUPPLY

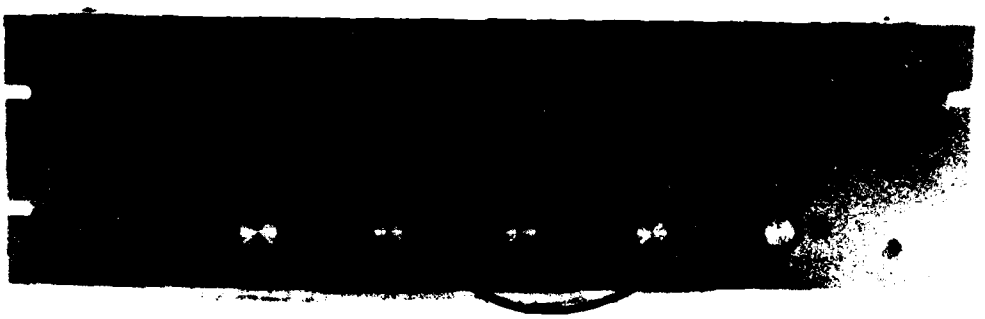


FIGURE 7 - SIGNAL DELAY UNIT

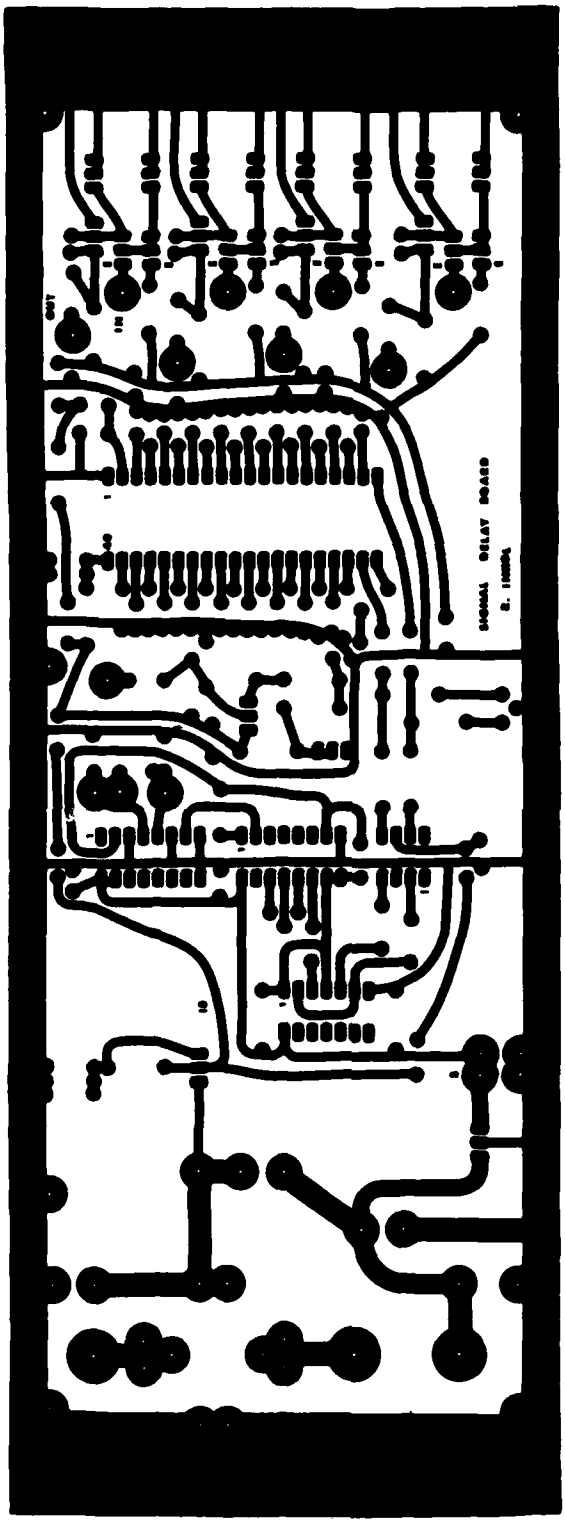


FIGURE 8 - PC BOARD LAYOUT

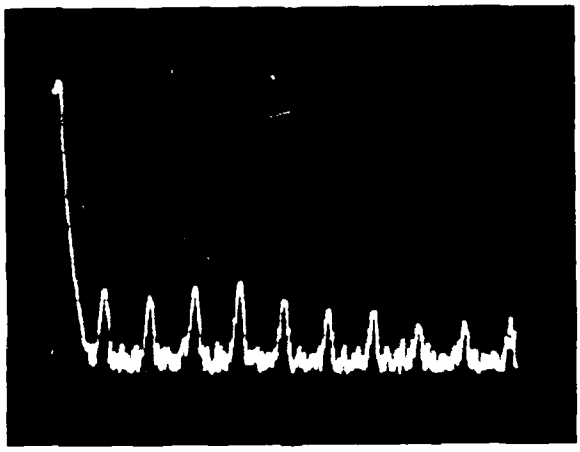


FIGURE 9 - HARMONIC CONTENT OF SDU OUTPUT FOR .5V P-P 1 KHz SINUSOID INPUT AND MINIMUM INPUT ATTENUATION, VERTICAL: 10 dB/ DIVISION, HORIZONTAL: 1 KHz/DIVISION

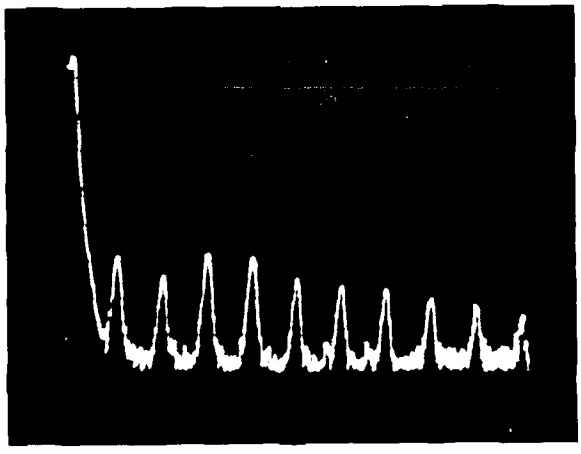


FIGURE 10 - HARMONIC CONTENT OF SDU OUTPUT FOR 1V P-P 1 KHz SINUSOID INPUT AND MINIMUM ATTENUATION, VERTICAL: 10 dB/DIVISION HORIZONTAL: 1 KHz/DIVISION

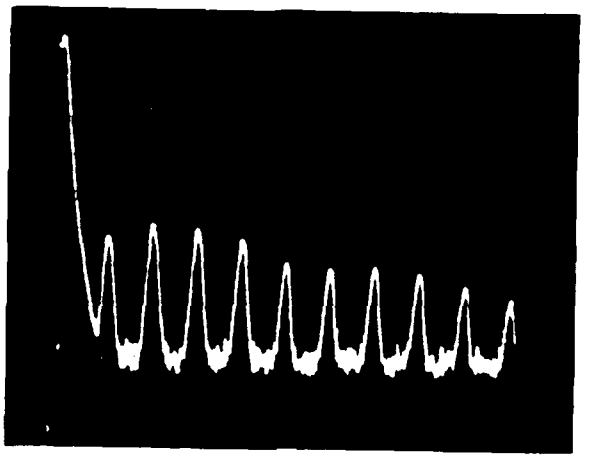
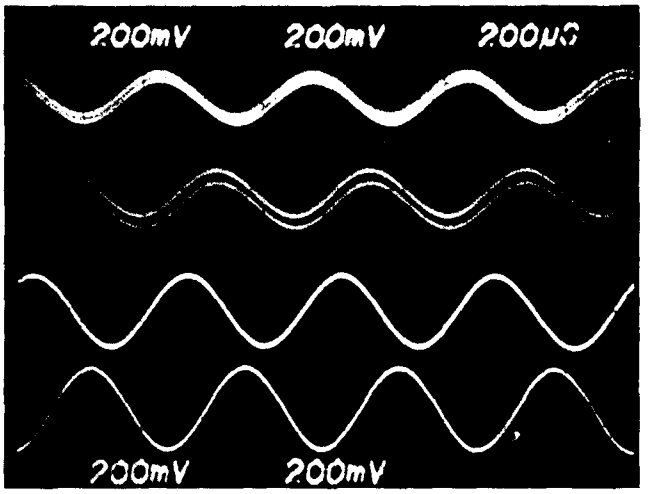


FIGURE 11 - HARMONIC CONTENT OF SDU OUTPUT FOR 2V P-P 1 KHz SINUSOID INPUT AND MINIMUM INPUT ATTENUATION, VERTICAL: 10 dB/DIVISION, HORIZONTAL: 1 KHz/DIVISION



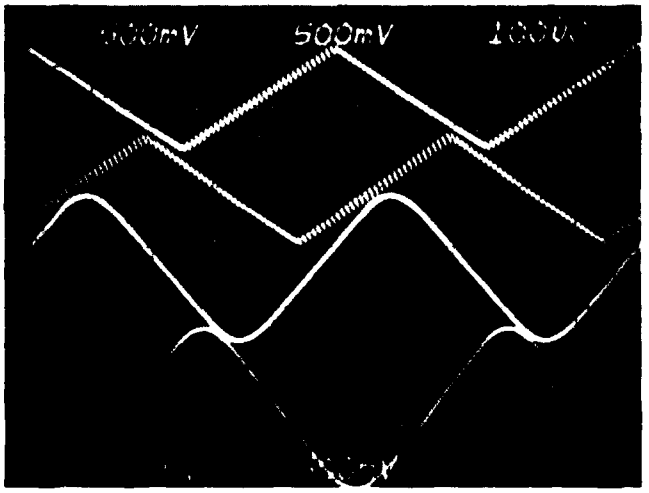
(a)

(b)

(c)

(d)

FIGURE 12 - OPERATION OF SDU FOR SINEWAVE INPUT



(a)

(b)

(c)

(d)

FIGURE 13 - OPERATION OF SDU FOR TRIANGE-WAVE INPUT

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The SDU is a completely self-contained unit employing a tapped Bucket Brigade Device (BBD) delay line to realize up to four independent differential signal delays of from one to 256 microseconds (U).

DSIS

KEY WORDS

Delay Line
Charge Transfer Device
Bucket Brigade Device

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