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THESIS

INTEGRATED CIRCUIT DESIGN OF A VIDEO
RECONSTRUCTOR FOR A RANGE-GATED
MOVING TARGET INDICATOR.

by

George Achilleus/Papadopoulos
December 1979

Thesis Advsior: John M. Bouldry

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20. (continued)

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Integrated Circuit Design of a Video
Reconstructor for a Range-Gated
Moving Target Indicator

by

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

The video reconstructor circuit (VRC) of the channelized or range gated moving target indicator (RGF/MTI) is designed for integrating on a single dual in-line integrated circuit package (DIP). The developed chip model is tested and its performance evaluated for a wide range of operating conditions. The tests indicate that the model offers superior performance over the RGF using discrete components. An extension of this technique offers opportunities in reducing the majority of the remaining channel elements to chip size. For many MTI applications this will yield still additional benefits.

Full TTL compatibility of the design makes the device easily controllable with digital logic. The threshold voltage setting, the output gate control and the integration time constant can be set by software or firmware.

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TABLE OF SYMBOLS AND ABBREVIATIONS

RGF/MTI   range gated moving target indicator (f denotes that the range gate or else channel contains filter)

VR/RGF   video reconstructor of the range gate

RF   radio frequency

IF   intermediate frequency

VF   intermediate frequency

F_c carrier

F_o operating

PW, Z   pulse width

PRT, PRP, T   pulse repetition period

PRF = 1/T   pulse repetition frequency

n, k   number of hits

σ targets radar cross section

F_N Nyquist holding frequency

F   sampling frequency

T   sampling period

RPM   rotations per minute

SL^o angular velocity in degrees

SL_r angular velocity in radions

θ_B azimout angle of radars beam @ 3dB

ϕ_B elevation angle of radars beam @ 3dB

R   range, distance

ΔR	range resolution
ΔF	frequency resolution
I	improvement factor
RCVR/XMTR	
$\bar{S}_r$	RF signal power density
$\bar{S}_{rr}$	power density of the signal
VRC	discrete videa reconstructor circuit
VRIC	integrated video reconstructor circuit

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I. INTRODUCTION

The intent of this thesis is to improve the performance
of the range gated moving target indicator (RGF/MTI) and to
design the video reconstructor circuit (VRC) of the range
gated channel on a single dual in-line IC package (DIP)
chip.

The discrete circuit in Figure 1 was constructed in
1973 by N. Koral [1] and was improved by Charles J. Boyle
[2] in 1975. Twenty channels and a timing system have been
integrated in a demonstration unit which operates in con-
junction with the AN/UPS-1 surveillance radar. From the
circuit of the channel the sample and hold and the gate
filter can be implemented using IC's readily available in
the market. The design of the last part, the VRC, is
presented in this thesis.

In Part II radar operating fundamentals and the RGF/MTI
problems, are introduced. The signal processing in a radar
system is first examined and it is then specialized in MTI
theory for both the real time domain process (MTI with
delay line cancelers) and frequency domain process (the
RFG/MTI). In conjunction with the existing models of the
RGF/MTI channels useful observations of its performance,
advantages and disadvantages are made. In addition the
specifications of the channels are examined to facilitate

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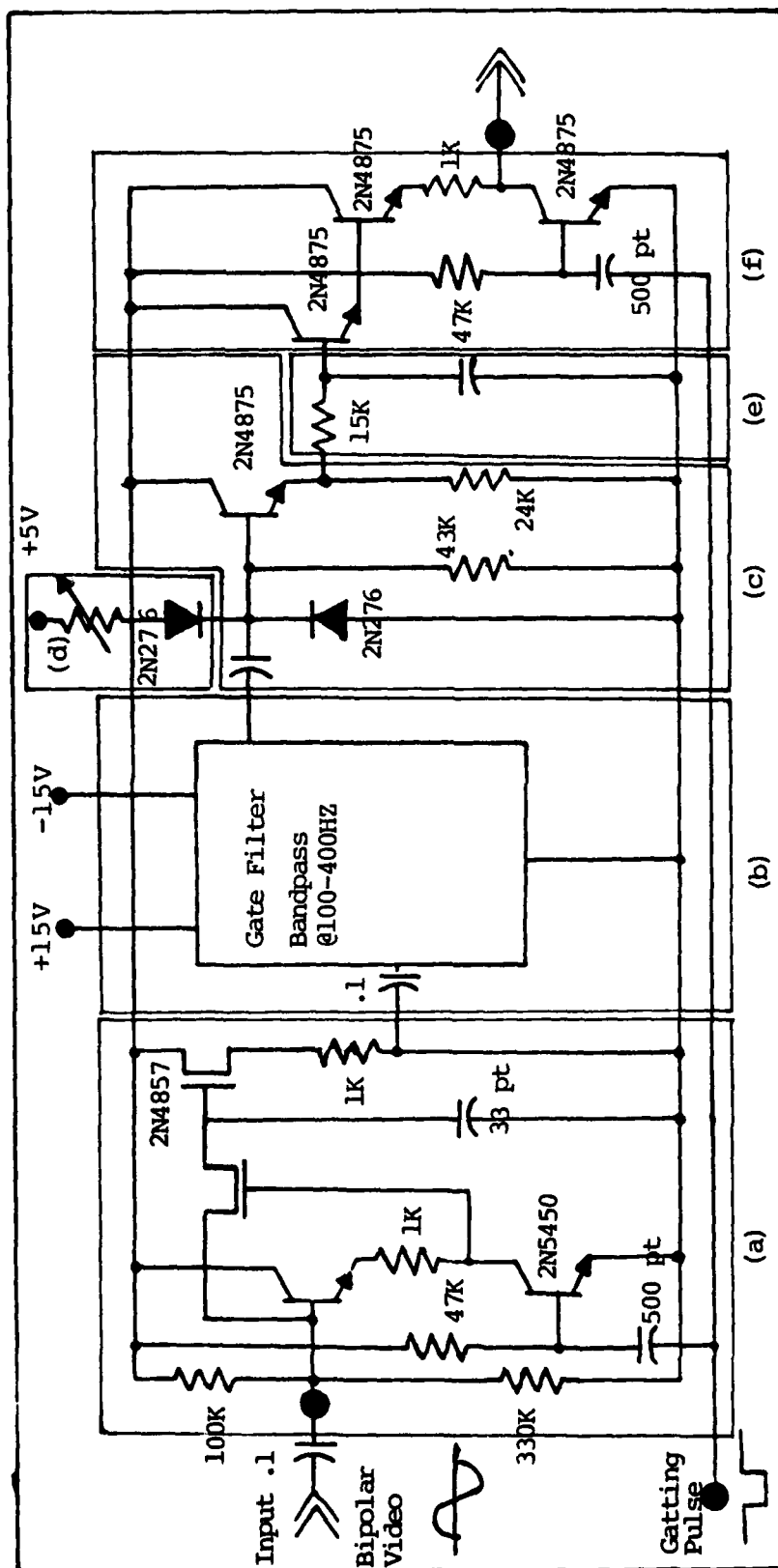
Figure 1. Original channel of the RGF/MTI ([1], [2]); (a) Sample and hold circuit or boa con generator, (b) gate bandpass filter, (c) half-way rectifier, (d) threshold setting, (e) integrator, and (f) output gate.

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the definition of the requirements of the updated and improved circuit model, which is to be integrated on a chip.

The reason for this long introduction to the problem is the author's belief that despite numerous disadvantages, the RGF/MTI has potential for excellent performance.

Part III, the Design of the Video Reconstructor Circuit (VRC) of the RGF/MTI on DC Single Duel in Line IC Package (DIP) starts with an overview of a typical IC development procedure, and the responsibilities of the designer. A flow chart of the design process is developed and followed closely until the completion of the design with the layout.

In Part IV, Experimental Procedure, the circuit model, tests and performance evaluation are presented.

The conclusions drawn from this IC development are contained in Part V, Conclusions.

In Appendix A the author presents a pseudorandom (Jitter) PRF generator, a sample and hold circuit and a first order recursive sampled analog gate filter (expandable to higher order). These circuits use readily available IC devices and may be parts of an updated version of the RGF/MTI channel.

In Appendix B, the characteristic curves, the component specifications and the layout schematics [3] used during this design are shown for convenience.

In Appendix C the mathematical analysis of the rectangular pulse and the rectangular pulse train is shown.

Finally, Appendix D contains the cost effective analysis for the new device.

II. RADAR OPERATION FUNDAMENTALS AND THE RGF/MTI PROBLEMS

A. SIGNAL ANALYSIS

This section presents a brief discussion of the theory and operation of a typical MTI radar system (Figure 2). The signal waveforms involved in the entire radar process from the beginning to the end of the transmit/receive cycle are shown in Figure 3.

The radar cycle begins at the oscillator in the frequency generating subsystem, where the baseband sinusoid A is generated.

$$A = G \sin (2nft)$$

This waveform is then frequency translated to the radar operating frequency (RF). Because of device limitations, frequency translation is made in several mixer stages and can be expressed analytically by the identity:

$$SmA \cdot SinA' \equiv \tfrac{1}{2} [\sin (A+B) + \sin (A-B)]$$

A high pass filter for frequency-up translation in the transmitter (a low pass filter for frequency-down translation in the receiver) is used to reject the low frequency component (high frequency component in the receiver).

It should be noted that for the remainder of the analysis all amplitude terms will be omitted, since their only significance is to represent the gain of the stages.

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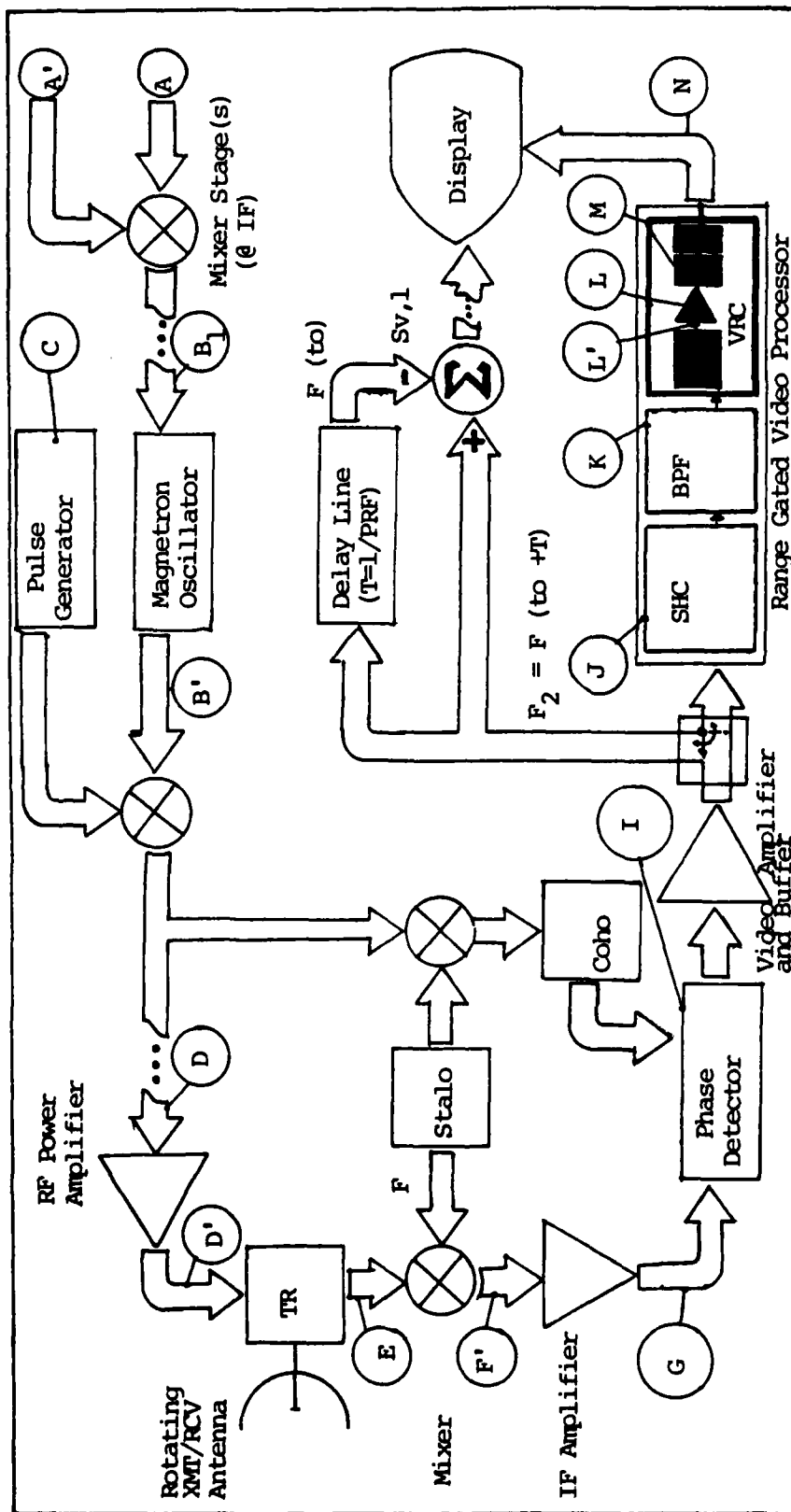
Figure 2. Block diagram of a typical MTI radar. The radar uses the same antennas for transmission, reception. Direct energy leakage from the high energy side (XMTR) to the low energy side (RCVR) is prevented by the TR isolator. The video reconstructor circuit, port of the video processor is shown in heavy dark ink.

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$$A = \sin(2\pi\, f_1 t)$$

$$B' = \sin(2\pi\, f_{IF} t)$$

$$B = \sin(2\pi\, f_{RF} t)$$

$$C = P(t)$$

$$D = \sin[(2\pi f_{RF})\, t]; \quad KT < t < KT + \tau, \quad k = 1, 2, 3\ldots$$

$$E = \sin[2\pi (f_{RR} \pm f_m) t - \frac{4\pi f_{RF} R}{C}]$$

$$F = \sin(2\pi\, f_{IF} t)$$

$$G = \sin[\pm 2\pi\, f_{dt} - \phi] = \sin(\pm \frac{4\pi v_r t}{\lambda} - \phi)$$

I = phase detector output

J = sample and hold output

K = filter output

L = full wave rectified video

M = integrated (dc) video

N' = Gating pulse

N = VRIC output
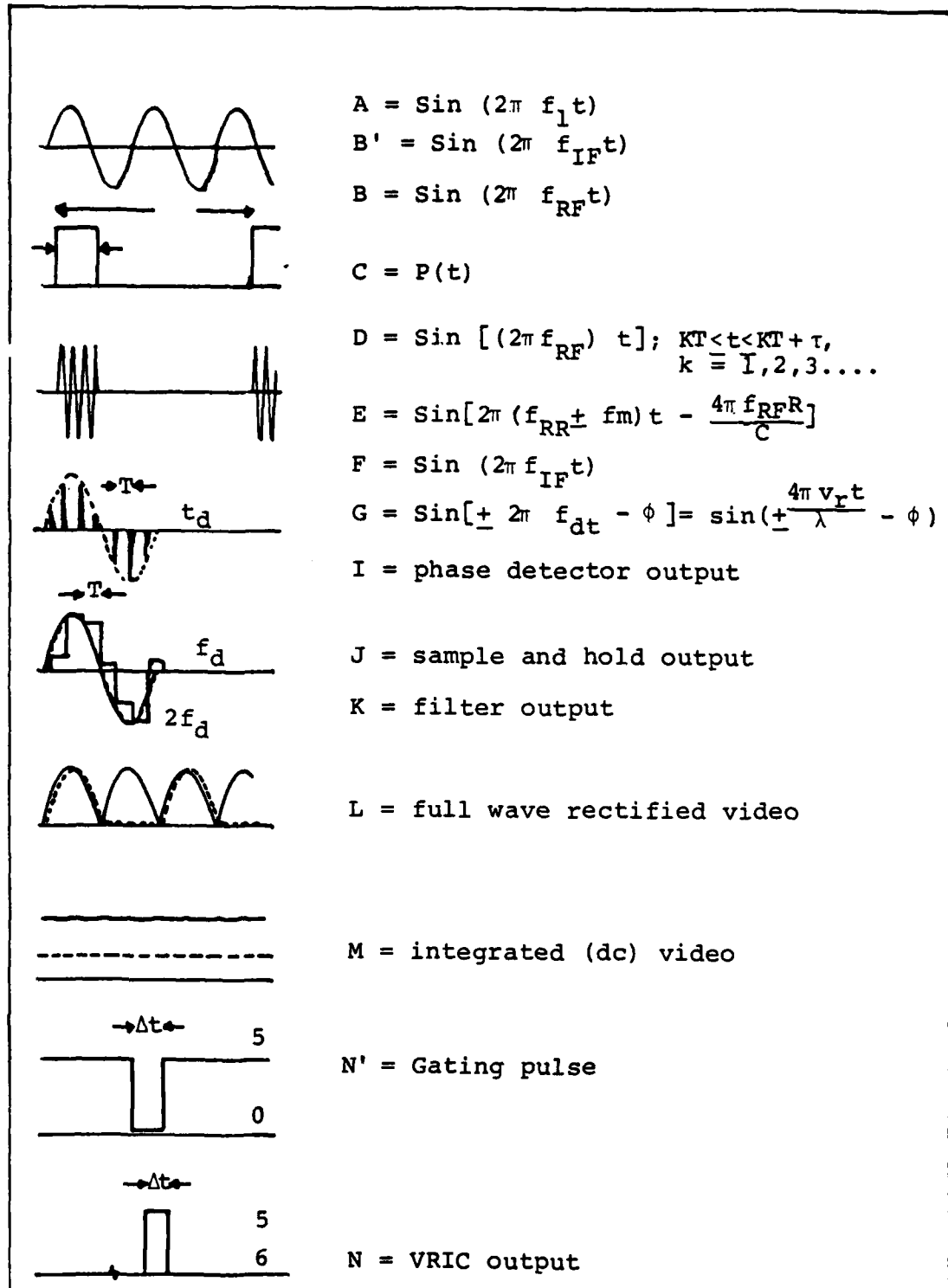
Figure 3.   Radar waveforms.

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For transmitter operation the sum frequency output from the last mixer stage is amplitude modulated by a train of rectangular pulses[1] (C) in the modulator. The modulated carrier (D) is:

$$D_t = \text{Sin } (2\pi f_{RF})t \cdot p(t)$$

$$= \begin{array}{l} \text{Sin } (2\pi f_{RF})t \; ; \; KT \leq t \leq KT+\tau, \; k = 1, 2, \ldots \\ 0 \qquad\qquad\qquad \text{elsewhere.} \end{array}$$

T is the pulse repetition period (PRP)

τ is the pulse width (PW)

In the frequency domain the pulse train is described as:

$$C_f = \frac{A\tau}{T} \sum_{-\infty}^{\infty} \frac{\text{Sin } (n\pi t/T)}{n\pi \tau/T} \; \exp \, [j2\pi nt/T]$$

and the sinusoid as:

$$B_f = \delta(f_{RF}) + \delta(-f_{RF})$$

thus, the expression for the pulse modulated RF signal becomes:

$$D_f = B_f \star C_f$$

$$= \frac{A\tau}{2\pi} \{ \text{Sa}[(f + f_{RF})\frac{\tau}{2}] + \text{Sa}[(f - f_{RF})\frac{\tau}{2}] \}$$

The graphical representation of the waveform in both time and frequency domain is given in Figure 4.

---

[1]The rectangular pulse and the rectangular pulse train are not realistic waveforms but approximations to an ideal waveform generated from the addition of several harmonic terms of a sinusoidal waveform (See Appendix C for details.).

Time Domain	Frequency Domain

$p(t) = \text{rect } (t/\tau)$

$= \{ ^1_0 \quad ; \quad KT \leq t \leq KT+\tau$

$\quad K\ 0,1,2,\ldots$
$\quad \text{elsewhere}$

$p(f) = \frac{A\tau}{T} \sum\limits_{-\infty}^{\infty} \frac{\text{Sin}(n\pi\tau/T)}{n\pi\tau/T} e^{\frac{J2\pi nt}{T}}$

$B(t) = \text{Sin } (2\pi f)t$

$B(f) = \delta(-f) + \delta(f)$

$B(t) \cdot C(t) = \text{Sin } [(2\pi f)t] \cdot p(t)$

$B(f) * C(f) = \frac{1}{2} \frac{A\tau}{2\pi} [\text{ Sa } (f+f_o)\frac{\tau}{2}$

$\quad + \text{Sa } (f-f_o)\frac{\tau}{2}]$
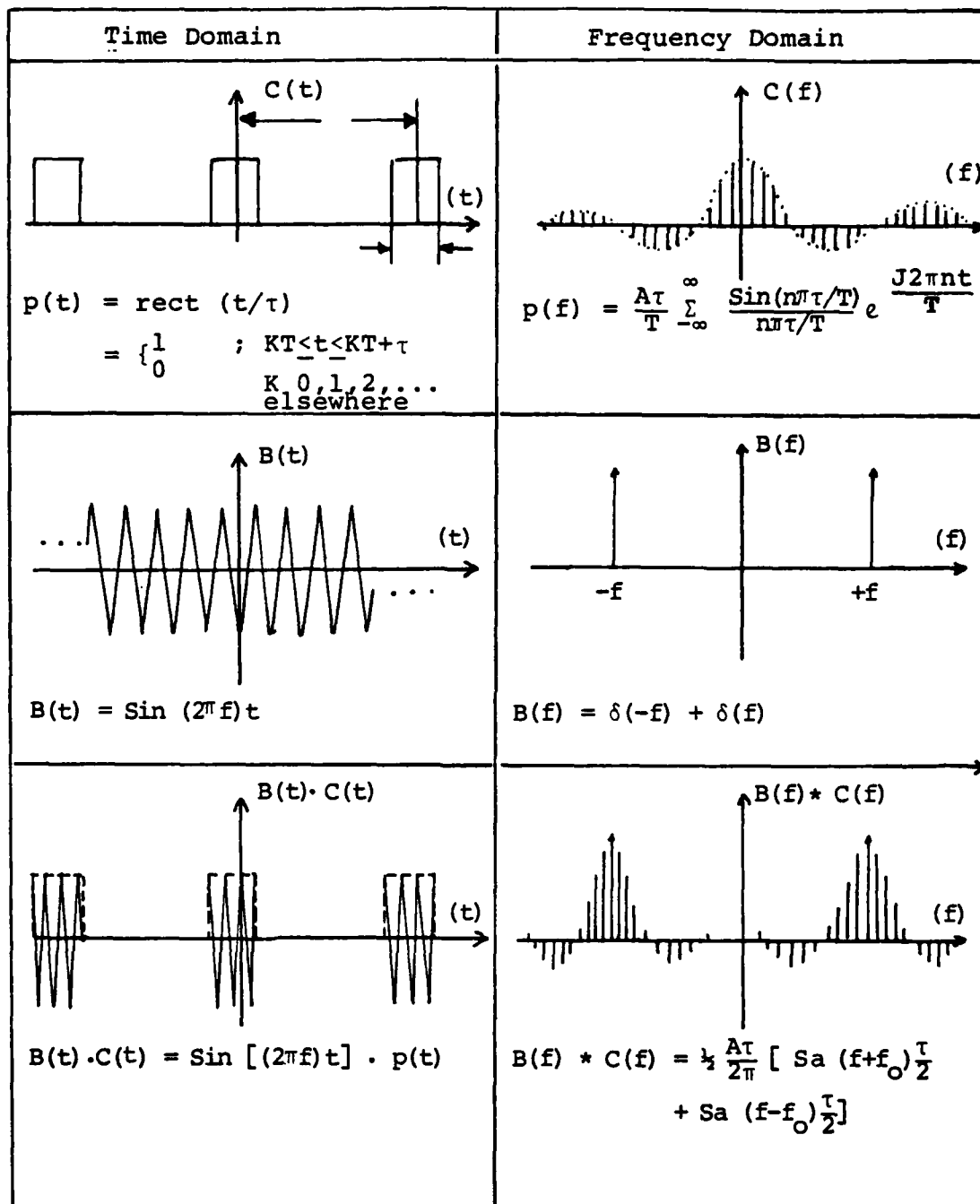
Figure 4. Carrier pulse modulation and its graphical presentation in time and frequency domains.

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The pulse modulated RF signal, properly amplified, is then transmitted to free space. Typically, the transmit operation corresponds to the pulse width. The radiation pattern is determined from antenna characteristics (i.e., A_e, g_d, D). Generally it has a narrow beamwidth and low jidlobes.

After the transmit cycle is completed, the duplexer (TR) isolated the XMTR from the RIVR which now is turned on. The radiated energy is propagated with a velocity close to the speed of light ($C = 3 \times 10^8$ m/sec). The power density at distance R from the XMT antenna is given by:

$$\bar{S}_r = \frac{g_d \; P_t}{4 \pi R^2}$$

Any objects in the surrounding space are illuminated. Depending on their physical and electrical characteristics, they absorb a portion of the incident energy (Sa) and reflect/reradiate the remainder (Srr). Most objects that are "targets" have a ratio of absorbed to reradiated energy less than unity. Objects having ratios greater than unity are classified as "clutter." These defining terms are not true in all cases. Targets on clutter have also been defined by the differences in their frequency spectra. In most cases manmade objects are constructed from conductive materials which reradiate most of the incident energy. Thus, the "target" to "clutter" ratio limitation is correct.

$$: \frac{\bar{S}a}{\bar{S}rr} \leq 1 \quad \text{"Targets"}$$

$$\frac{\bar{S}a}{\bar{S}rr} > 1 \quad \text{clutter}$$

"Targets," in general, have poor directional characteristics and the reradiation of a fraction of incident energy is omnidirectional or nearly so. It is customary to assume omnidirectional characteristics. Thus:

$$\bar{S}rr = \frac{\bar{S}r \cdot \sigma}{4\pi R^2}$$

$$= \frac{g_d \, P_t \cdot \sigma}{(4\pi R^2)^2}$$

The term, σ, radar cross section, has been added to generalize the expression. Note that Srr now represents the power density in the vicinity of the radar antenna. If the effective area of the antenna is:

$$Ae = \frac{\lambda^2 \, g_d}{4\pi}$$

where $\lambda (=c/f)$ is the wavelength of the transmitted signal.

The signal power at the receiver front end will be:

$$\bar{S} = \frac{g_d \cdot P_t \cdot \sigma \cdot \lambda^2 \cdot g_d}{4\pi R^2 \quad 4\pi}$$

$$= \frac{\lambda^2 \cdot g_d 2 \cdot P_t \cdot \sigma}{(4\pi)^3 \, R^4}$$

The pulse modulated carrier signal has been amplitude (AM) and angle (FM, PM) modulated from the rotating antenna as well as from the target. Undesirable signals (noise) are also received from the antenna. Therefore, the total power available in the front end of the receiver (P) is:

$$\bar{P} = \bar{S} + \bar{N}$$

The carrier waveform (S_R) is:

$$S_R = G \, \text{Sin} \left[2\pi (f_{RF} \pm f_m) \, t - \frac{4\pi f_{RF} R}{C} \right]$$

where:

$\Delta f = f_{RF} \pm f_m$ is the FM term

$\phi = (4\pi \cdot f_{RF} \cdot R)/C$ is the phase shift due to the
reflection on the target at the distance R.

During the time the receiver is "ON" more than one signal return may arrive within the unambiguous range of the radar. These signals will be processed by the receiver.

The process of signal detection differs from radar to radar. Because it is the purpose of this thesis to investigate a new technology to improve signal processing in an MTI radar, only that type of detection process will be further considered here.

B. THE DOPPLER FREQUENCY SHIFT AS THE FUNDAMENTAL MTI THEORY

The Doppler theorem states that the difference in frequency between the incident waveform and its reflection from

an object moving with velocity Vr relative to the observation point is:

$$|f_d| = \frac{2Vr \; f_{RF}}{C}$$

$$= \frac{2Vr}{\lambda}$$

The sign of the frequency is taken as positive if the moving object approaches the observation point; otherwise, it is negative.

This frequency shift introduces angle modulation of the pulse modulated carrier (D) which now becomes:

$$S_R = G \; Sin \; [2\pi(f_{RF} \pm f_d) \; t + K\phi]$$

The spectrum of the Doppler frequency shift is extended from zero to several KHZ (corresponding to the maximum possible velocity of manmade objects). The lower region of this spectrum corresponds to "stationary" or "near stationary targets" and is called clutter. Some examples of clutter are; clouds, sea-waves, weather, mountains, etc.

It is obvious that the upper and lower limits of the Doppler spectrum are not easily definable but they depend on the application and the operating conditions.

C. MTI RADARS AND SIGNAL PROCESSING

The MTI radar receiver serves to detect a Doppler frequency shift that corresponds to targets of interest within the radar's useful range and uses this frequency to generate a signal that the operator will recognize.

For the detection of the Doppler frequency and because RF discriminators do not have enough frequency resolution, the received signal or echo return, is down frequency translated (to the video region) using several mixer stages (with low pass filters). Analytically:

$$G'' = E \cdot G =$$

$$= \{Sin[2\pi(f_{RF} \pm f_d) t - K\phi] + Noise\} \cdot Sin[(2\pi f_{ST}) t]$$

$$= Sin[2\pi(f_{RF} + f_{ST} \pm f_d) t - K\phi]$$

$$+ Sin[2\pi(f_{RF} - f_{ST} \pm f_d) t - \phi] + Noise$$

f_{ST} is the STALO or the IF. After the low pass filter remains only:

$$G' = Sin[2\pi(f_{RF} - f_{ST} \pm f_d) t - \phi]$$

Assuming that $f_{ST} = f_{IF,1} + f_{IF,2} + \dots \simeq f_{RF}$ or $f_{RF} - f_{ST}$

$$= f_{COHO}, \text{ then:}$$

$$G = Sin[\pm 2\pi f_{dt} - \phi]$$

$$= Sin[\pm \frac{4\pi V_{rt}}{\lambda} - \phi]$$

The Doppler frequency is extracted by one of the following procedures.

1. MTI Employing Delay Line Connectors (t-domain)

The signal G is delayed in time by passing through a delay line[2] with delay time (t_d) EXACTLY equal to the PRP(T). Then it is subtracted from the present (at the time $T_o + T$) input $G_1 = G(t_o + T)$ to give the video signal:

$$Sv = G(t_o + T) - G(t_o)$$

$$= Sin[\pm \frac{4\pi V_r}{\lambda} (t_o + T) - \phi] - Sin[\pm \frac{4\pi V_r}{\lambda} t_o - \phi]$$

$$= Sin(2\pi f_d T) \cos [2\pi f_d (t_o + T/2) - \phi]$$

Note that:

a. If $f_d \neq 0$ then the video signal is also a non-zero signal $(Sr \neq 0)$ provided that:

$$2\pi f_d (t+T/2) - \phi \neq \pi/2$$

b. If $f_d = \frac{K}{T}$; $K = 0,1,2,\ldots.$ Then:

$$sin(2\pi f_d T) = Sin(\frac{2\pi K}{T} T) \equiv 0$$

The speeds for which $f_d = K/T$ are called blind speeds and are given by the equation:

$$V(K) = k \cdot \frac{C}{2f_{RF} T}$$

Blind speeds are eliminated with "staggered" or "jittered" PRF systems (such as the one shown in Appendix A). Unfortunately jittered PRF cannot be employed very easily on

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[2]Traditionally, delay lines are formed using mercury or quartz crystals.

MTI radars using delay lines because as may be recalled, the delay line must have a delay time constant exactly equal to the VRF. Therefore, only a staggered PRF system can be used. For this system two delay lines (one for each PRF value) are required.

Other disadvantages accompanying this type of MTI signal processing are:

(1)   High power loss in the delay line and the associated transducer.

(2)   Large and bulky processors.

(3)   Crystals used require high degrees of geometrical accuracy and high temperature stability; thus, difficult and expensive construction.

(4)   Crystals are extremely sensitive to shipboard shocks and vibrations.

2.   MTI Employing Range Gates and Filters RGF/MTI

In the frequency domain Doppler frequency detection is accomplished by banks of narrow band filters. This process offers both range resolution, if range gates are used, and Doppler resolution if narrow band Doppler filters are employed.

In the past narrow band filters were difficult to design and occupied considerable space. Today Doppler frequency banks can be readily designed with good frequency characteristics.

The RGF/MTI method is more effective than the original MTI with the delay line connector and is more commonly used particularly in its digital form.

However, once PRF are employed the wide frequency spectrum required to give range resolution is lost. Detection of a moving target can be made but time or range information is missing.

To overcome this problem range gates are employed. Subsequent portions of the time domain signals are assigned to a series of channels by a gating sequence. This gating scheme permits the appropriate target signal to enter into the appropriate channel. All input gates conduct for exactly the same time Δt related to $\tau = PW$. Pulses from the output gates are time multiplexed in such a way that a pulse occurs only at the points of the range scale where a moving target was detected. The process through the gates can be viewed as a sampling process, with PW of the sampling pulse equal to the conducting time of the input gate. Thus Δt, the gate time, determines the useful bandwidth.

Each channel (Figure 6) except the input gate contains; (a) a sample and hold circuit (or box car generator) which converts the bipolar video pulse train at the output from the phase detector (I) to a staircase bipolar video (J), (b) a gate filter which permits only the Doppler frequency to be processed (still bipolar), (c) a video reconstructor circuit (VRC) which contains a rectifier, integrator, threshold

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setting network and an output gate, converts the bipolar

video to a unipolar (dc) voltage, compared with a reference

signal (threshold) and when a gating pulse is present,

outputs a pulse.

The disadvantages of the RGF/MTI process are basic-

ally due to the hardware. To implement the functional

block of Figure 5 a large number of components is required.

The components of the existing circuit [1,3] are all discrete

except for the gate filter (hybrid). Discrete components

consume a considerable amount of power, require multiple

voltage supply, have low performance capability, require

considerable support and documentation and are difficult

to service.

This thesis reduces these problems to the minimum.
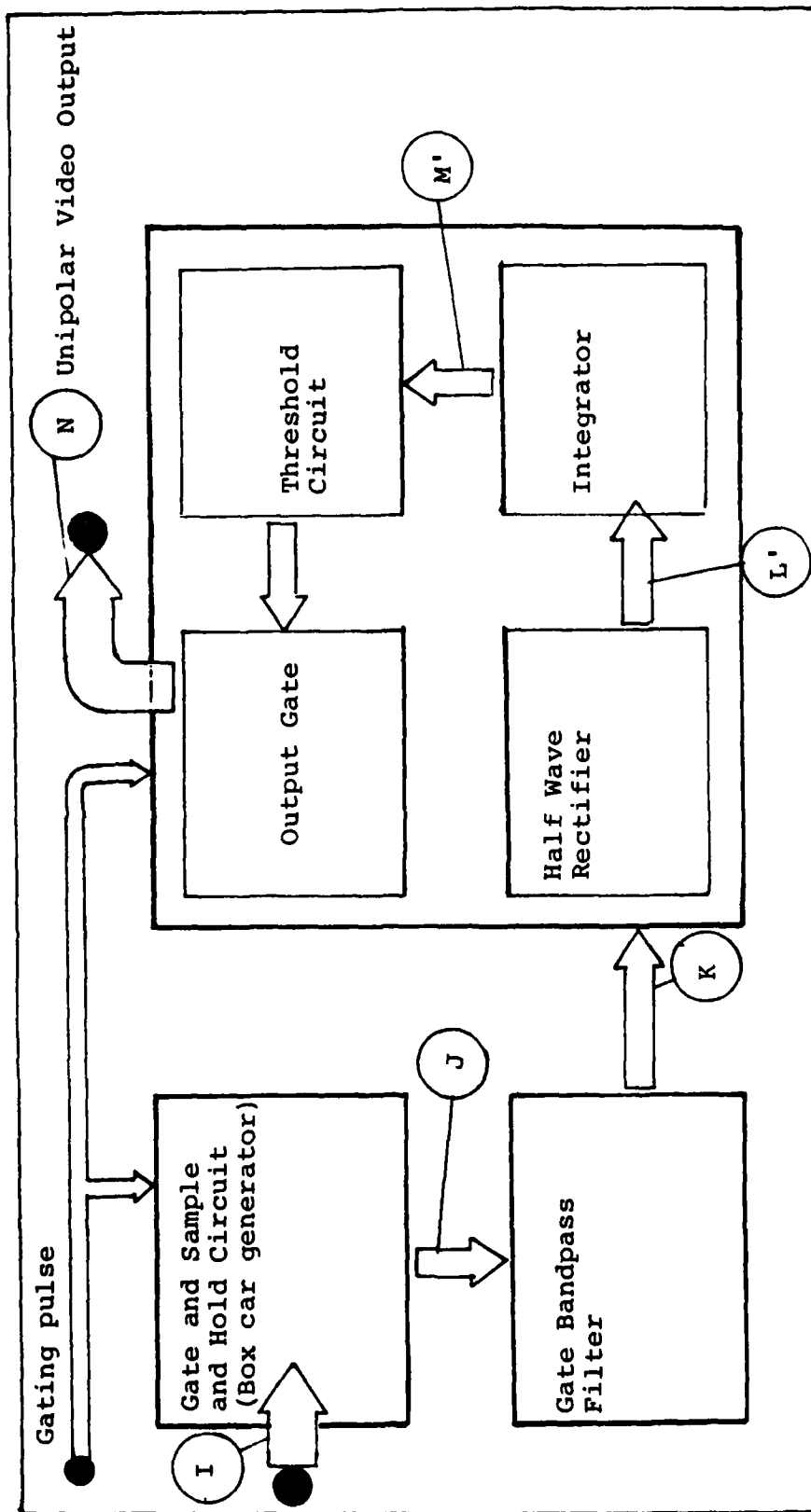
Figure 5. Functional block diagram of the existing RGF/MTI channel.

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III. THE DESIGN OF THE VIDEO RECONSTRUCTOR CIRCUIT (VRC)
      OF THE RGF/MTI ON A SINGLE DUAL IN-LINE IC PACKAGE (DIP)

A. GENERAL

The design of the VRC on a DIP (chip) is based on "Semicuston IC design" procedures and the "monochip" concept.

Several semiconductor industries have developed a series of standardized chips which contain a large number of integrated components in fixed locations. The surface of the chip is designed in such a way that many different paths, to interconnect the components, can be made. Components having identical characteristics with those on the chips are available in kit form to facilitate the following steps of the design.

In the first stage of the developmental procedure, production is customized. The design develops the metalization mask for the interconnection of the components of the circuit. To ensure safe production, kit parts may be used to build the prototype of the circuit. Then a series of tests and measurements may be obtained to make sure that none of the components reach limiting conditions. The final circuit configuration is used for the development of the rough layout schematic. Figure 6 is the flowchart of a typical IC development procedure, derived by the author. Step 12 calls for the layout of the chip. This is a fundamental step in the design and is the step that the designer himself must provide.
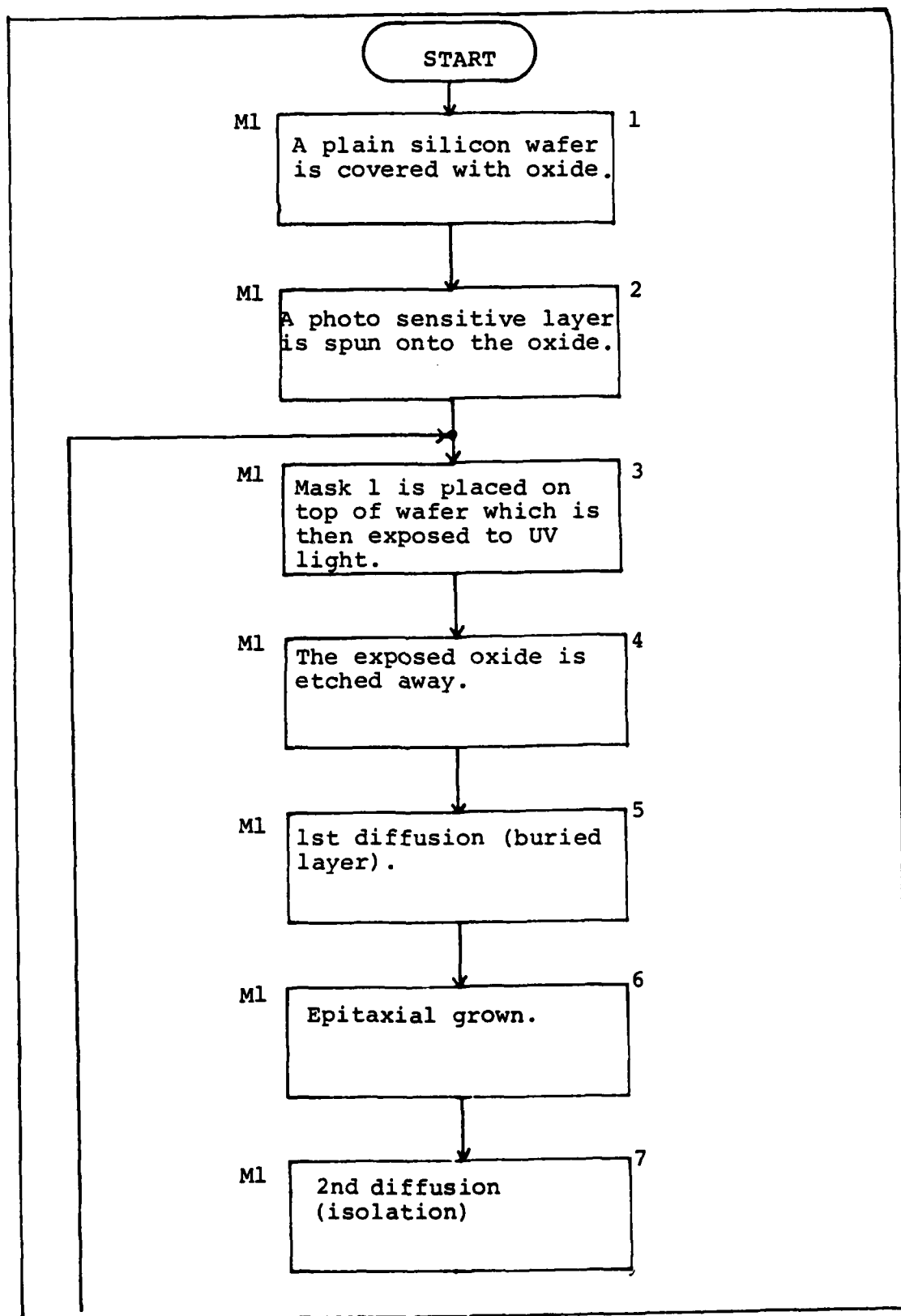
Figure 6. Flowchart of a typical IC development procedure;
M - manufacturer, D = semicustom designer (here
the author.

Figure 6.   (continued)

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```
                              14
M2    ┌──────────────────────┐
      │ The layout is "taped."│
      │  (Mylar taping)       │
      └──────────────────────┘
                 │
                 ▼              15
M2    ┌──────────────────────┐
      │ The layout is photo   │
      │ reduced.              │
      └──────────────────────┘
                 │
                 ▼              16
M2    ┌──────────────────────┐
      │ The custom metalliza- │
      │ tion mask is placed   │
      │ on wafer and then it  │
      │ is exposed in UC.     │
      └──────────────────────┘
                 │
                 ▼              17
M2    ┌──────────────────────┐
      │ The pattern and the   │
      │ parameters of the dice│
      │ (on the wafer) are    │
      │ evaluated.            │
      └──────────────────────┘
                 │
                 ▼              18
M2    ┌──────────────────────┐
      │ Computer controlled   │
      │ tip tests chips.      │
      └──────────────────────┘
                 │
                 ▼              19
M2    ┌──────────────────────┐
      │ The wafers fractured  │
      │ in dice and the defec-│
      │ tive are removed.     │
      └──────────────────────┘
                 │
                 ▼              20
M2    ┌──────────────────────┐
      │ Dice are sealed on the│
      │ open packages.        │
      └──────────────────────┘
                 │
                 ▼              21
M2    ┌──────────────────────┐        ⟋‾‾‾⟍
      │ Pins are connected to │──────▶│ END │
      │ pads and the package is│       ⟍___⟋
      │ sealed hermetically.  │
      └──────────────────────┘
```

Figure 6. (continued)

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Here, this step represents the initial effort of the thesis in seeking a desirable VRIC and it is shown in detail in Figure 7. Section B contains the complete design process based on this step.

After the completion of the layout, the responsibility for production is returned to the manufacturer (steps 13 through 23 in Figure 6).
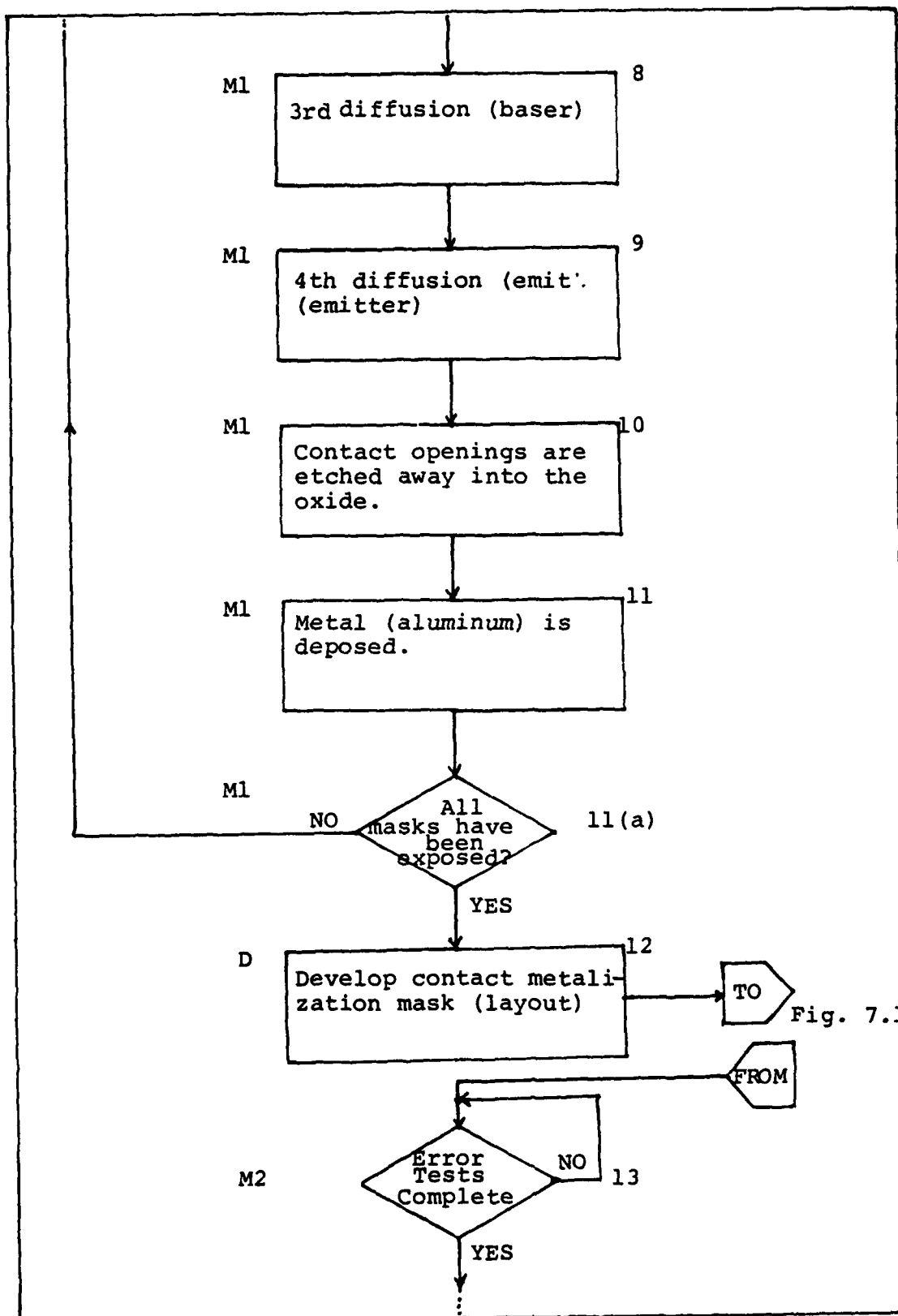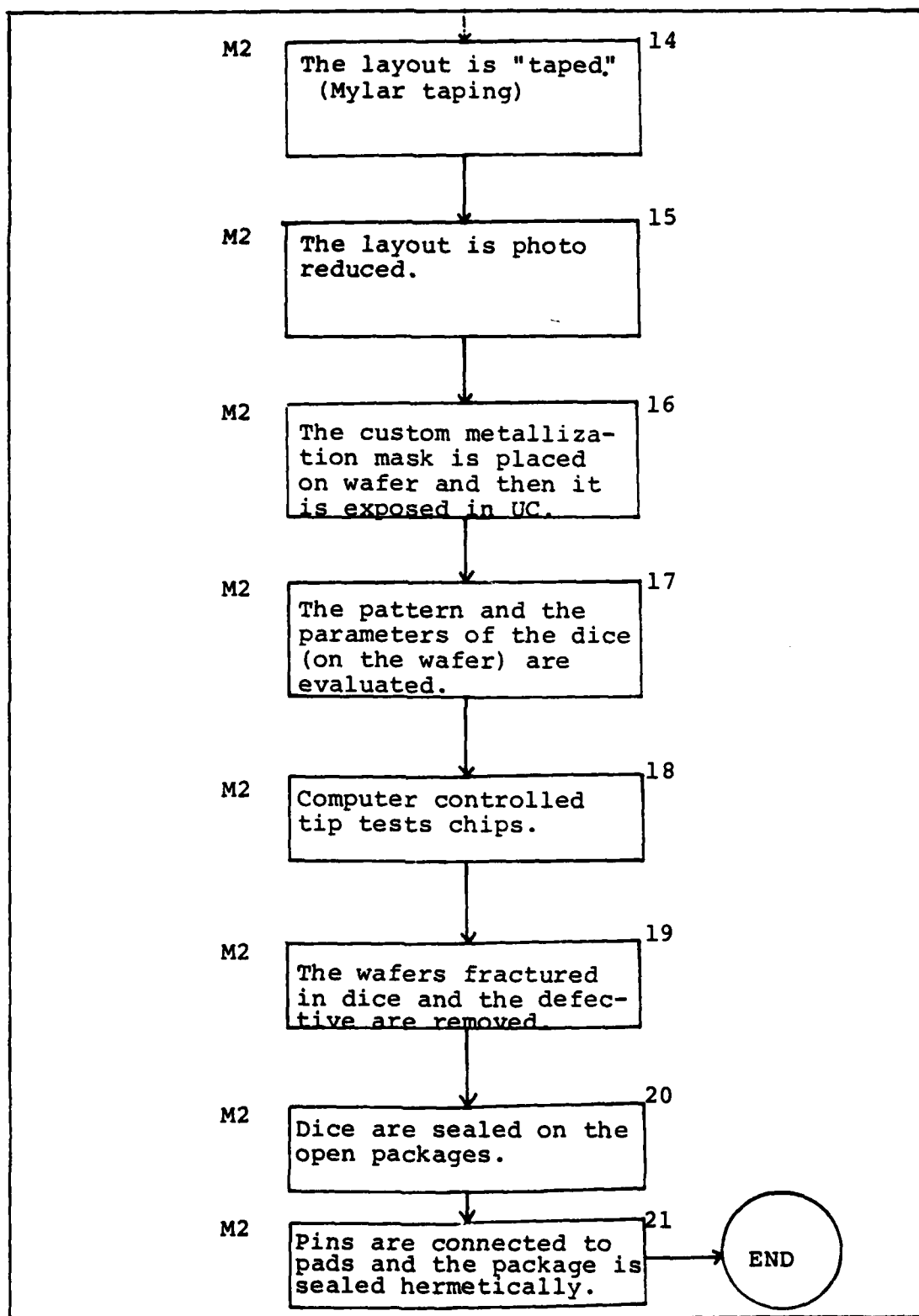
B. VRIC DESIGN PROCESS

To facilitate the design procedure, the flowchart developed in Figure 7 was followed closely. Each step of the design procedure is explained below.

1. General Specifications

Since the VRIC was desired to be comparable with the existing range gates [1,2] the specifications of the basic circuit (Figure 1) were reconsidered. These specifications are:

a. Input ports:

(1) Bipolar video input signal (from the gate filter) 6 V_{pp}, 100-400 HZ.

(2) Unipolar video (from the output from the integrator to the threshold and gating network.

(3) Threshold (reference) signal, 0.1 to 5V.

(4) Gating pulse, negative, TTL compatable, PW = 0.625 μ sec.

b. Output ports:

(1) Half wave rectifier output (input to the integrator) at the half of the input voltage level.
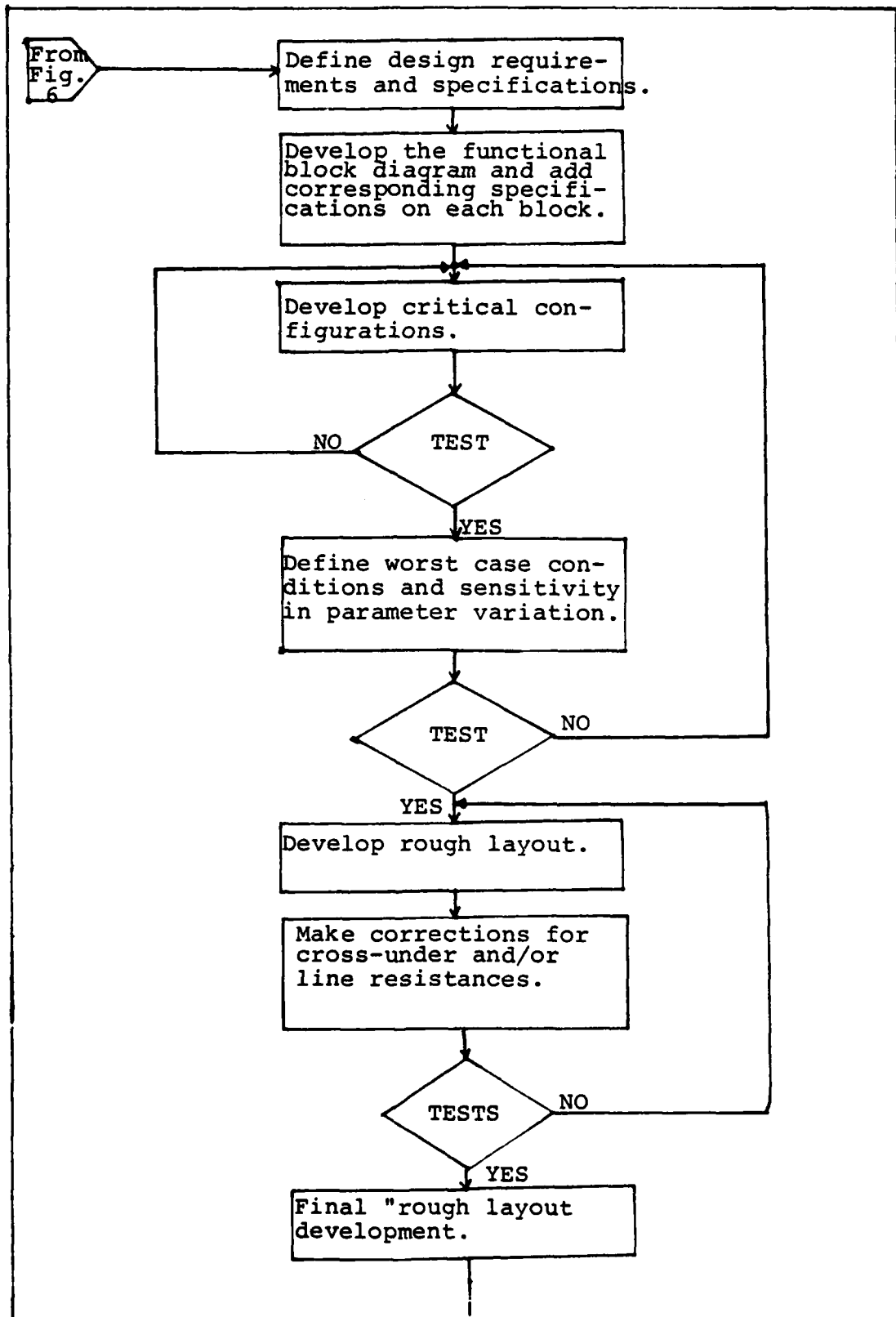
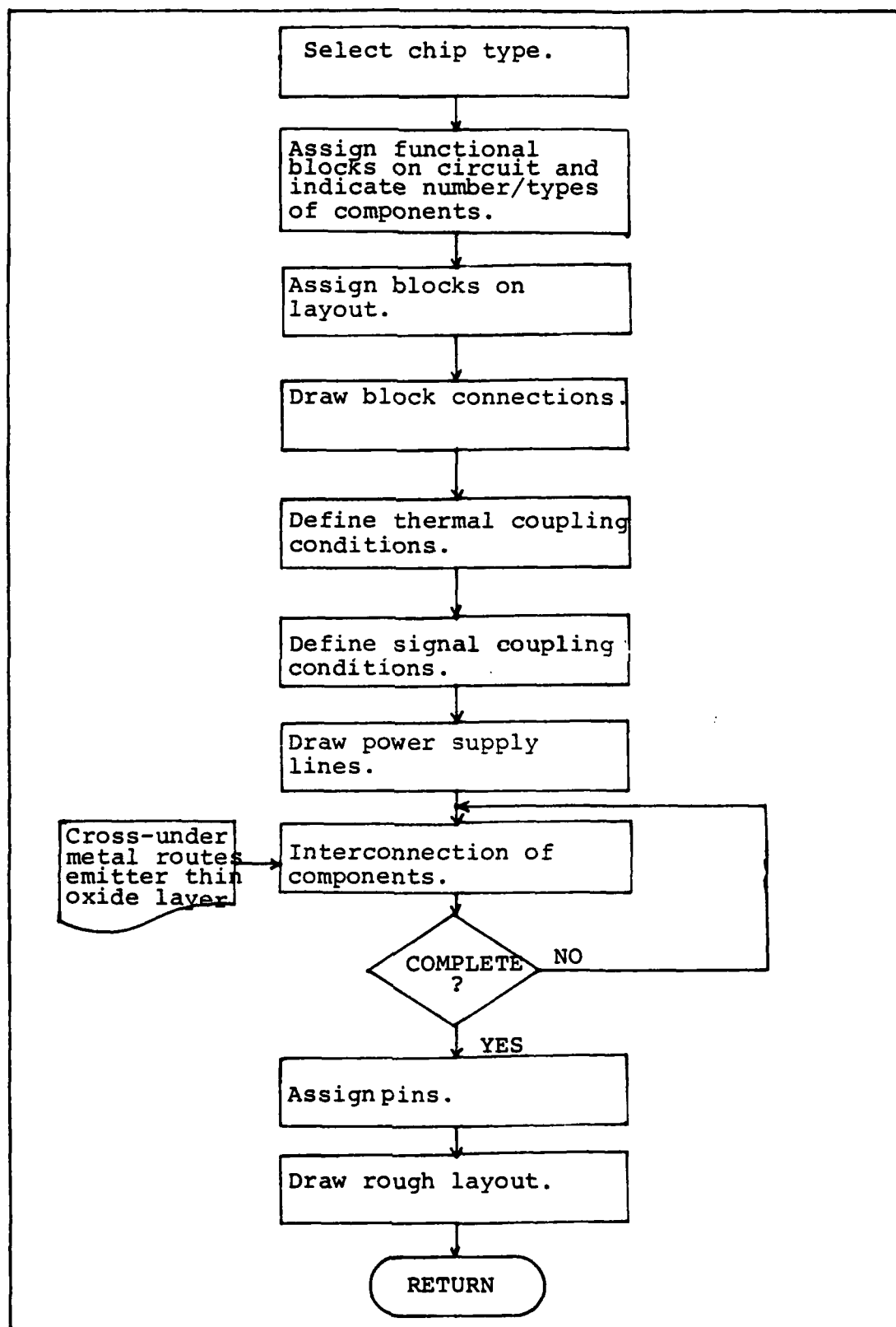Figure 7. Layout development details.

37

Figure 7. (continued)

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NOTE: In the new design it has been replaced by a full wave rectifier.

(2) Output gate, unipolar video TTL compatible, positive, pulse.

c. Power supplies/ground terminals (+24V, +15V, -15V, GND).

These specifications of the older discrete video reconstructor (VRC) were modified to satisfy not only the AN/UPS-1 surveillance radar[3] but to make them more general. The new specifications are listed in the VRIC specification sheet (Figure 14).

2. Block Diagram

After modification of the VRC specifications and the replacement of the HWR with a FWR, the block diagram of Figure 8 was developed. At each input/output port, the characteristic letters (corresponding to waveforms of Figure 2 are also shown). NOTE: The title "VRC" (video reconstructor circuit) as it appears in the block diagram of Figure 6 (discrete circuit) has been replaced by "VRIC" (video reconstructor intergrated circuit). Also, the "integrator" block has been removed from the IC main block. The reasons for this is that capacitance value equivalent to those required for the integrator cannot be obtained in IC's.

_____

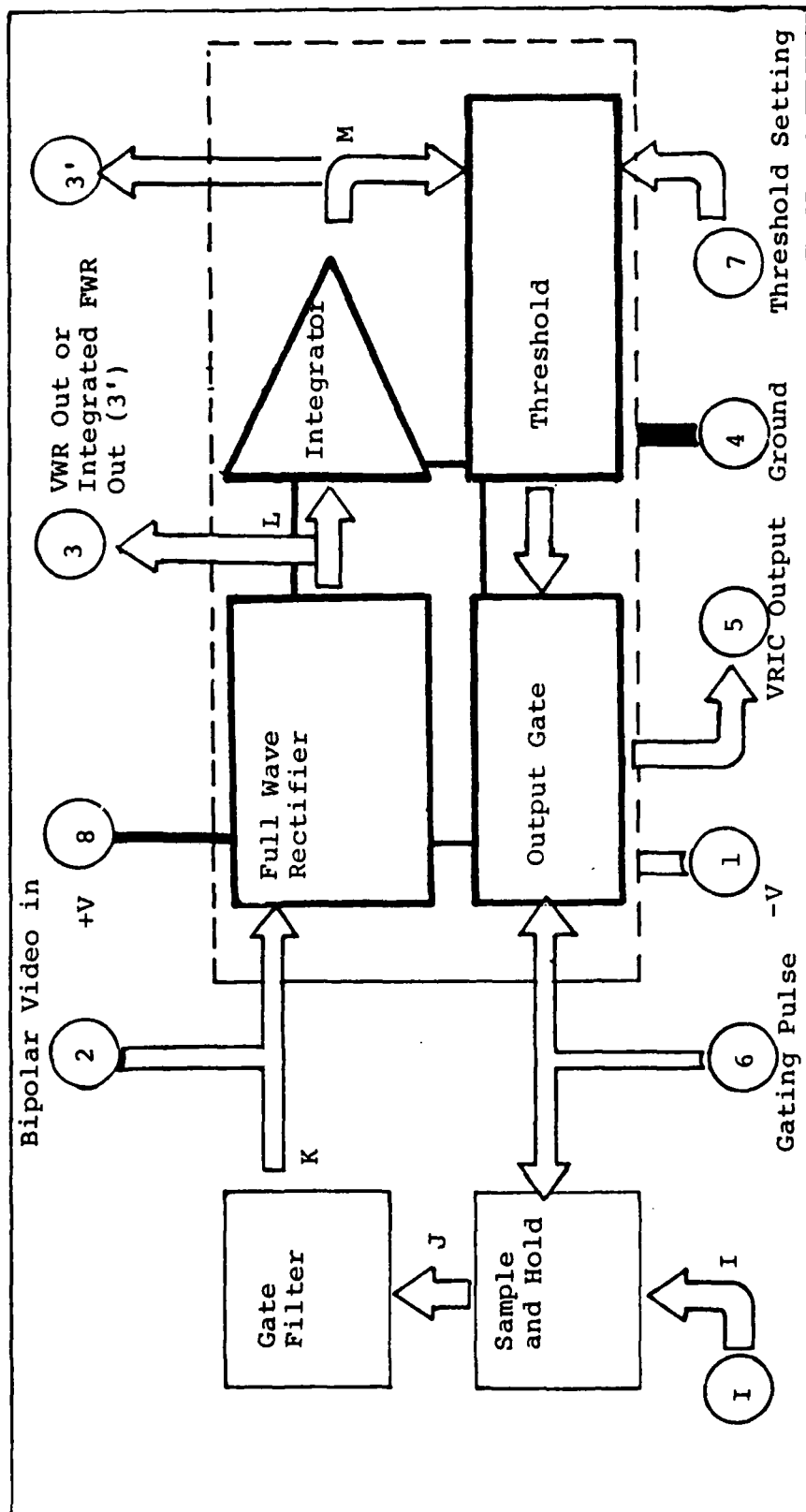[3]The original model [1,2] was designed to operate in conjunction with the AN/UPS-1 radar.

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Figure 8. Block diagram of the improved RGF/MTI channel. In the VRIC part the rectifier is referred to as full wave rectifier and the "integrator" has been removed out of the block VRIC.

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3. Generation of Circuit Configurations

From the several circuits for this stage, the circuit shown in Figure 9 was shown experimentally (Part IV) to be the best. The functional blocks a, b, c, and d are analyzed as follows:

a. Full wave rectifier

The input, bipolar video voltage, is applied to the base of Q1. This voltage is converted from Q3, Q4 and Q101, Q103 to bipolar current at the collector of Q2. During positive half cycles this current flows through the composite PNP (from Q5, QLO6) to the load (10KΩ). During the negative half cycles this current is "mirrored" to the load from the Q104, Q105. The waveform at the output of the FWR is a unipolar video which is then taken to the integrator.

b. Integrator

The integrator is implemented only by the external capacitor (C) connected from the output of the FWR to ground. The time constant is adjusted to the dwell time of the antenna. This time is different from system to system and for the same system may be different from gate to gate. The integrator time constant together with the PRP has a major effect on the power spectrum of the echo return [9]. The output from the integrator is a dc voltage at a level equal to the average of the input voltage.

c. Threshold circuit

The dc voltage from the integrator output is applied to the base of Q107 and is compared with the
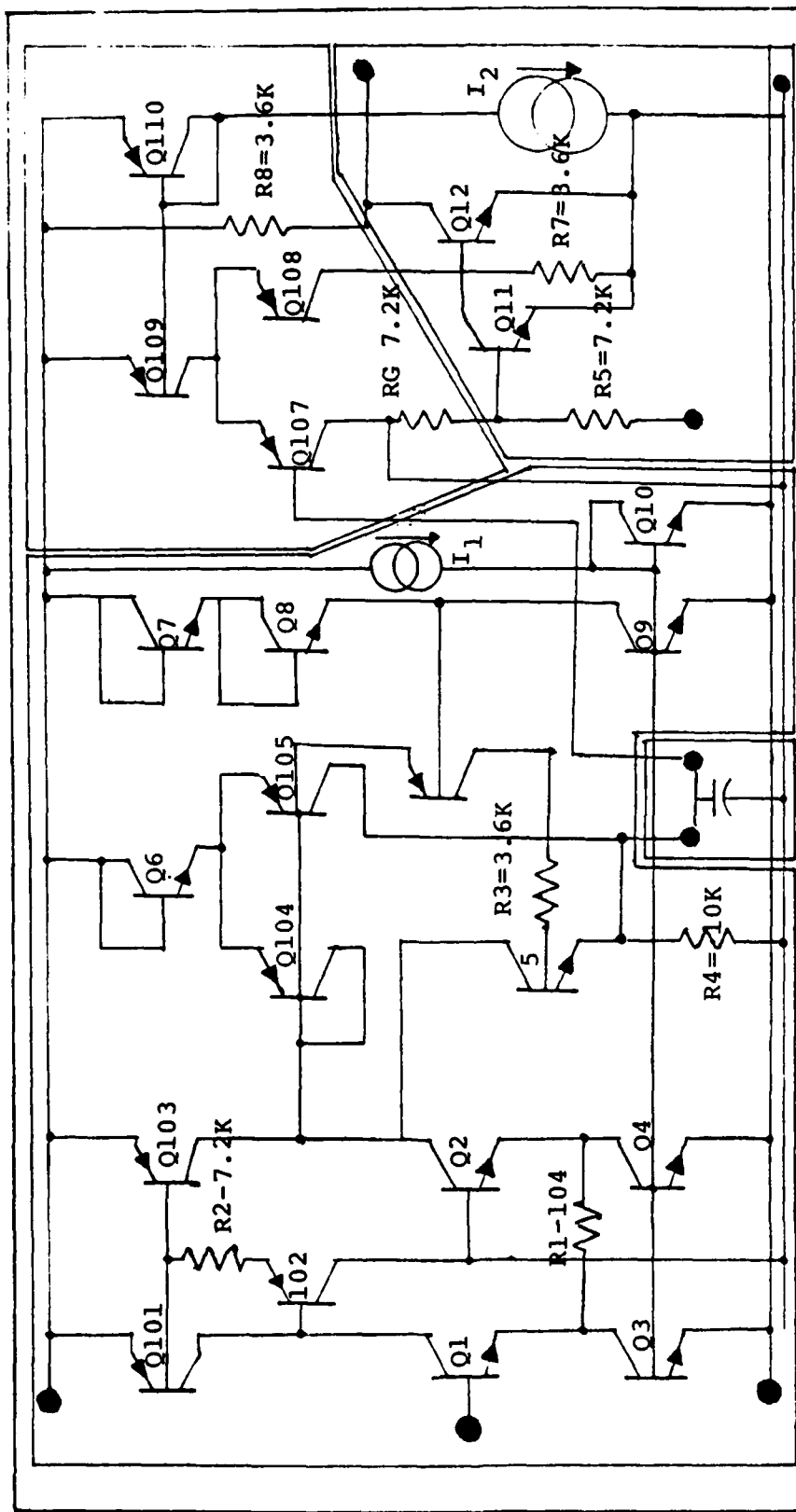
Figure 9. The VRIC detailed schematic diagram; (a) the FWR, (b) the integrator (external), (c) the threshold setting network, (d) the output gate. The terminals 1-8 are assigned as the pins of the IC. NOTE: All NPN transistors are numbered with number 1-99 and the PNP transitors 101-109.

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threshold or reference voltage applied to the base of Q108.
When $Vin \geq V_{th}$ a nonzero output is produced. In this case
it is applied to the collector of Q11 of the output gate
circuit.

d.   Output Gate Circuit

The output gate functions as an "AND" gate.
The inputs to the "AND" gate are the gate control signal
(same with the one controlling the input gate) and the
output from c. When both the inputs are not zero, the
gate produces a TTL compatible pulse with: $PW \propto \Delta \tau$ where
$\Delta \tau$ is the duration of the control signal.

4. Circuit Tests and Performance Evaluation

This part of the design, concerning circuit implemen-
tation (model) and various tests performed to ensure proper
operation, is described in Part IV Experimental Procedure.

5. Development of the VRIC Layout

The development of the layout is the last major
part of the semicustom design (Step 12 shown in Fig. 6
expanded in Fig. 7) and it is described as follows:

a.   Chip selection - From the "monochips A,B,C,D,E,
F,I,J,K (Appendix B) type D was selected because of the
component match with the requirements of the VRIC.

b.   Functional block assignment - The VRIC in Figure 9
was divided into functional blocks:

(1)   Current source -1

(2)   FWR input stage

(3)   Composite PNP and mirror

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(4)   Comparator

(5)   "AND: gate

(6)   Current source -2

and the circuit components were listed separately for each block.

c.   Block allocation - Using the number and type of the components required for each block, the allocation of the layout area was made (Figure 10).   An important factor that was considered at the same time was the requirement to eliminate the need for crossover connections. These connections are based on the cross-under resistance of selected transistors (not used).   The subject is greated in n-1 of this section.   The components in each block were numbered (1-99 for NPN transistors, 101-139 for PNP transistor).   Resistors were not numbered.   The allocation was completed locating the components away (as much as it was possible) from the border lines.

d.   Block interconnections - It was found practical to draw the interconnection lines between blocks in the early stage.   The lines should not be long because of the aluminum metal conduct resistance which is introduced $(t0 \times 10^{-3} \text{ m}\Omega$ per square inch).

e.   Thermal coupling - The heat sources of the VRIC were located over the widest possible area and uniformly displaced.   Components requiring matching were located symmetrically across hypothetical isothermal lines for equal heating.   Such component pairs are Q1-Q2, Q3-Q4, Q101-Q103, Q107-Q108.
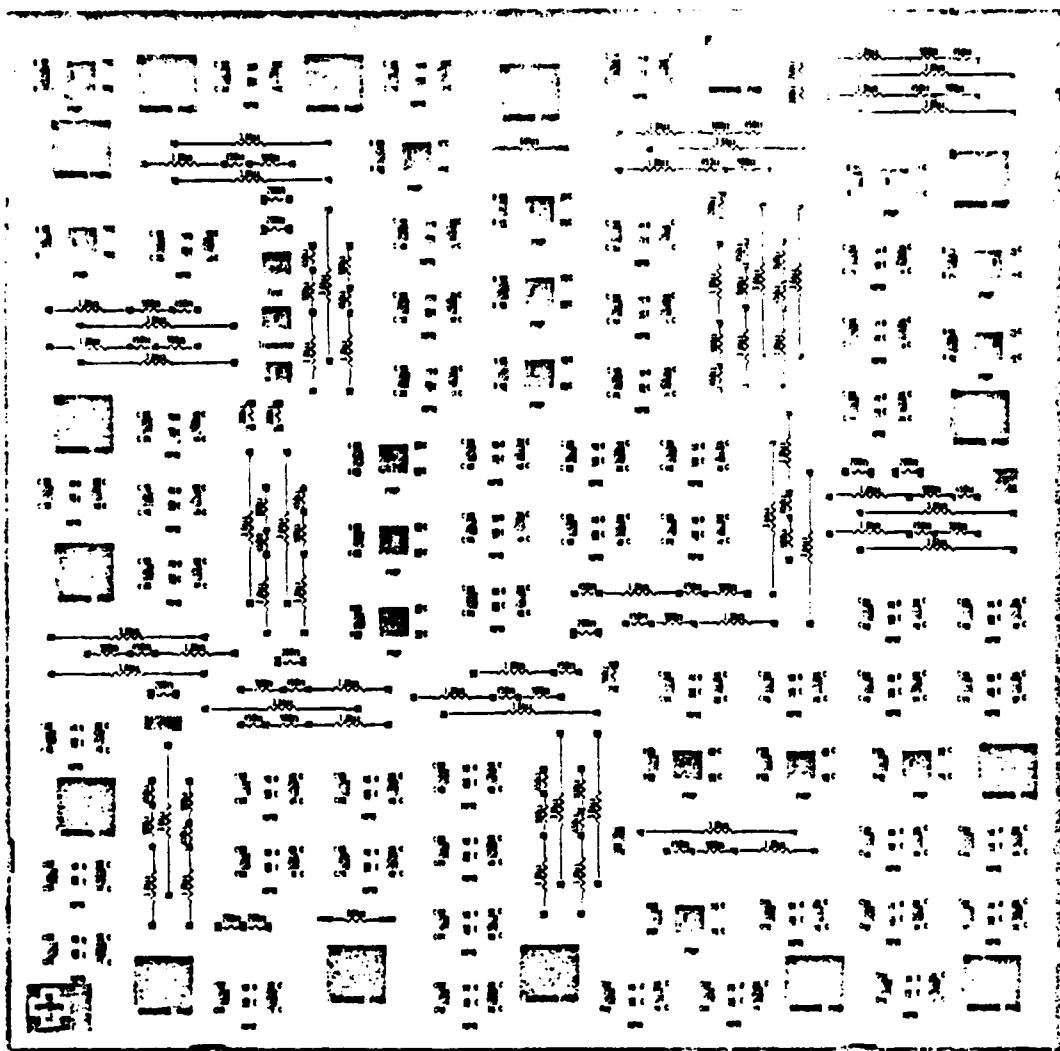
Figure 10.   The layout sheet of the "D" type chip [3].

f. Signal coupling - Since the inductive and capacitive coupling between the bonding wires and the package pins are critical at high frequencies and can lead to oscillations, lines with widely differing frequencies were physically separated as much as possible.

g. Power lines - The most negative voltage was connected to the substrate and the most positive to the N-layer. At least one connection had to be made from the -V to the peripheral pad (negative) and one from the +V to one internal +r auxiliary pad.

h. Component interconnections - For the component interconnection the factors 1,2 and 3 were carefully considered.

(1) Cross-unders. The cross-under resistance between the conducts of the multiple collectors of the transistor was used when it was necessary to cross two lines (Figure 11.2). Conceptually, the cross-under resistance is similar to the pinch resistance (Figures 11.b, c). Since the cross-under resistance is considerable (values can be obtained for the pinch resistors) it may affect the operation of the circuit. For this reason, cross-under resistances were calculated (from Figure 19) and added to the model to test its performance. After this, reevaluation was necessary.

(2) Metal routes - The maximum number of metal routes that can be drawn on each area of the layout is indicated from the number of dotted lines. The metal runs are 10 micron wide and they must be 10 micron apart from the
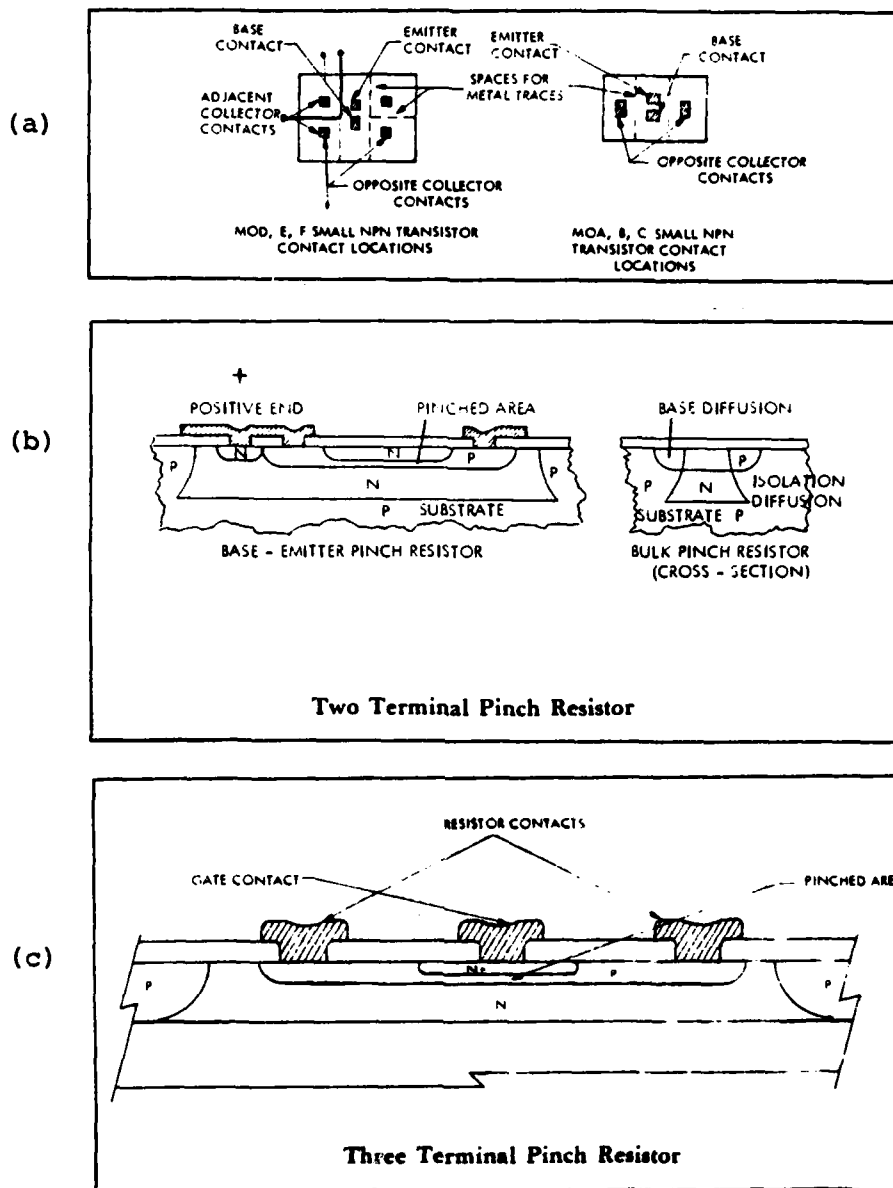
46

(a)

(b)

(c)

Figure 11. Cross-under and pinch resistances;
(a) demonstration of crossover connection
using cross-under resistance, (b) a two
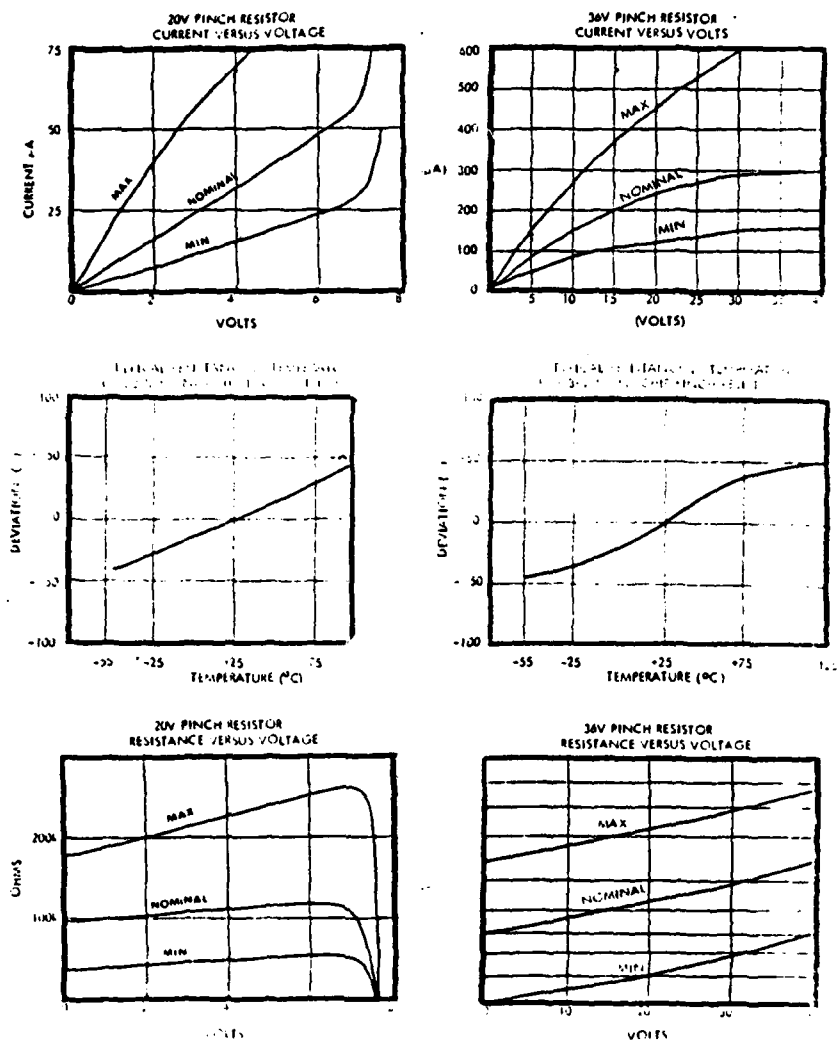terminal and (c) a three terminal pinch
resistor [3].

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Figure 12. Resistor characteristics. The characteristics
shown are the pinch resistor characteristics
used also for cross-under resistor value
evaluation [3].

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nearest other metal run or component. Their thickness is
1 micron and their specific resistance 50 mΩ/square micron.
For considerably long paths the line resistance was calculated
and was added to the corresponding line of the model. Also,
the current density of several critical circuit lines had to
be considered and the width of these lines were predetermined.

(3) Emitter thin-oxide layer - Lines directly
connected to pads may cause permanent damage to the very thin
emitter oxide layer. For this reason, such lines were drawn
away from the emitter thin oxide layers (shaded regions on
the layout in Figure 10).

i. Pin Assignment

Pin assignment was made using a simple rule:
bonding pads and package pins should be connected with
straight lines and without crossings.

j. Layout Sketch

The rough layout sketch of the VRIC was drawn
according to the above procedure and is shown in Figure 13.
This figure shows the metallization mask of the VRIC. This
mask (a manufacturer's responsibility) is done for demon-
stration purposes only and should not be used for the real
mask development. (Due to the need of accurate measurement
instrument for the width of the connection lines or distance
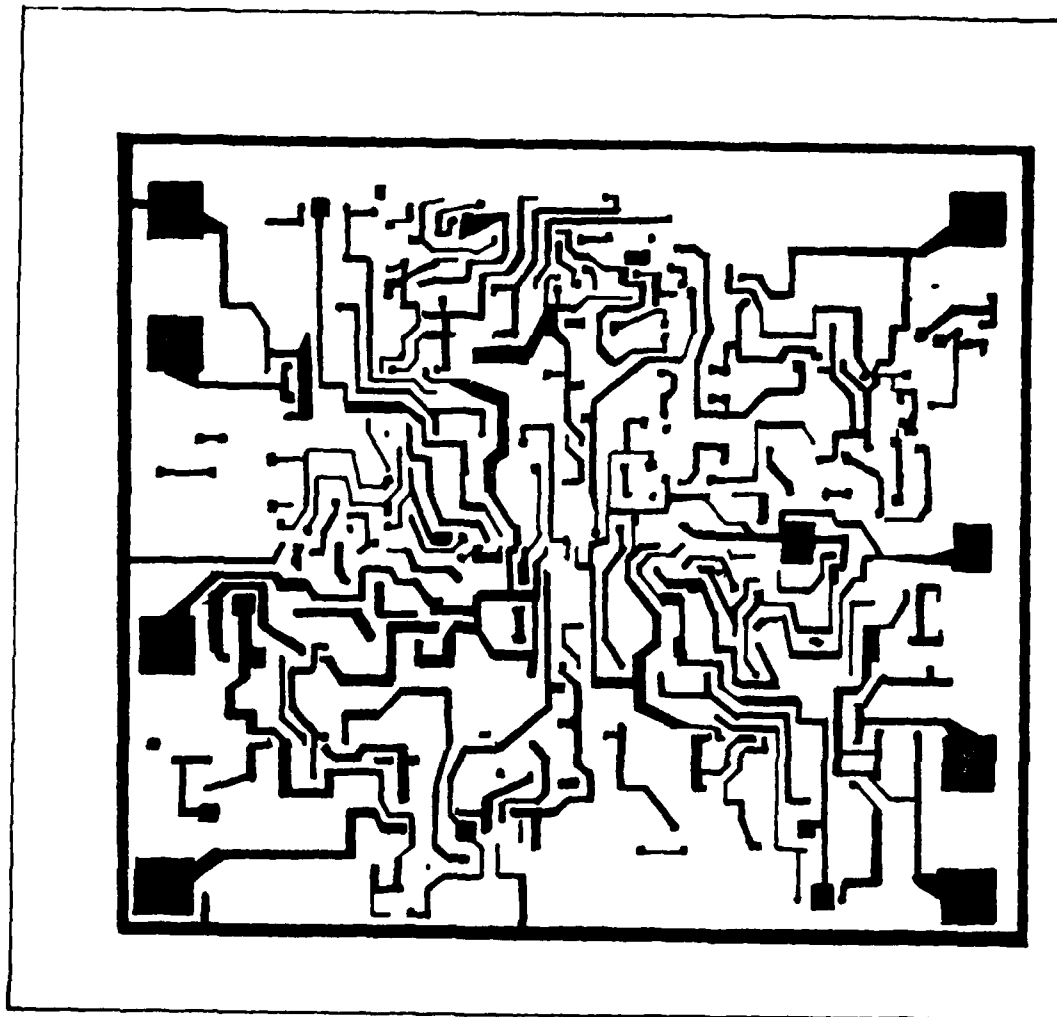between two lines, the indicated dimensions are not in scale.)

Figure 13.   Rough layout of the VRIC.

C. VRIC SPECIFICATIONS

The developed layout of the VRIC is the final step of the design procedure. With the layout completed, a production order for this device (the VRIC) may be placed at any time. The first devices could be available in four weeks. The total cost of the production is about one-fourth of a full custom design of the same circuit. Cost effectiveness over the discrete equivalent circuit cannot be exactly defined since it depends on the per year production.

In addition to the design effort, packaging information, connection diagram, absolute maximum ratings and typical applications for the VRIC are included below.

1. Packaging Information

In order to satisfy the mechanical and electrical requirements of MIL-STD-883, the VRIC must be packaged in the slightly more expensive ceramic packages (CERDIP).

2. Connection and Functional Block Diagram

The connection diagram is shown in Figure 14 together with the functional block diagram of the VRIC.

3. Absolute Maximum Ratings

	Charac-teristics	Values		
		min.	nominal	max.
Supply voltage -1	+V	+3	+5	+15
Supply voltage -2	-V	-3	-5	-15
Power dissipation	P_d		mW	
Input short circuit duration	I_c		N/A	
Operating temp. range	T_o°		N/A	
Storage temp. range	T_s°		N/A	
Lead (soldering) temp.	T		300°C	
Threshold voltage level	V_{TH}		0-5V dc	
Gating pulse	TTL		positive	
Input voltage	V_{in}	100mV	3Vpp	6Vpp
Output voltage	Vo	TTL positive		

Table I. Absolute maximum ratings of the VRIC.

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			Volt.
1.	-V	Negative power supply input (connected to substrate)	-5
2.	ANALOG INPUT	Typically a video signal. Power level programmable from 10mV to 8Volt. The use of input balance circuit is recommended.	
3.	FWR OUT		
4.	GND		
5.	VIDEO OUT	Digital TTL compatible pulse output 0-5V.	
6.	V_{TH}	Acceptable 0-5 volts.	
7.	GATE CTRL	Gating pulse, active low	
8.	+V		+5

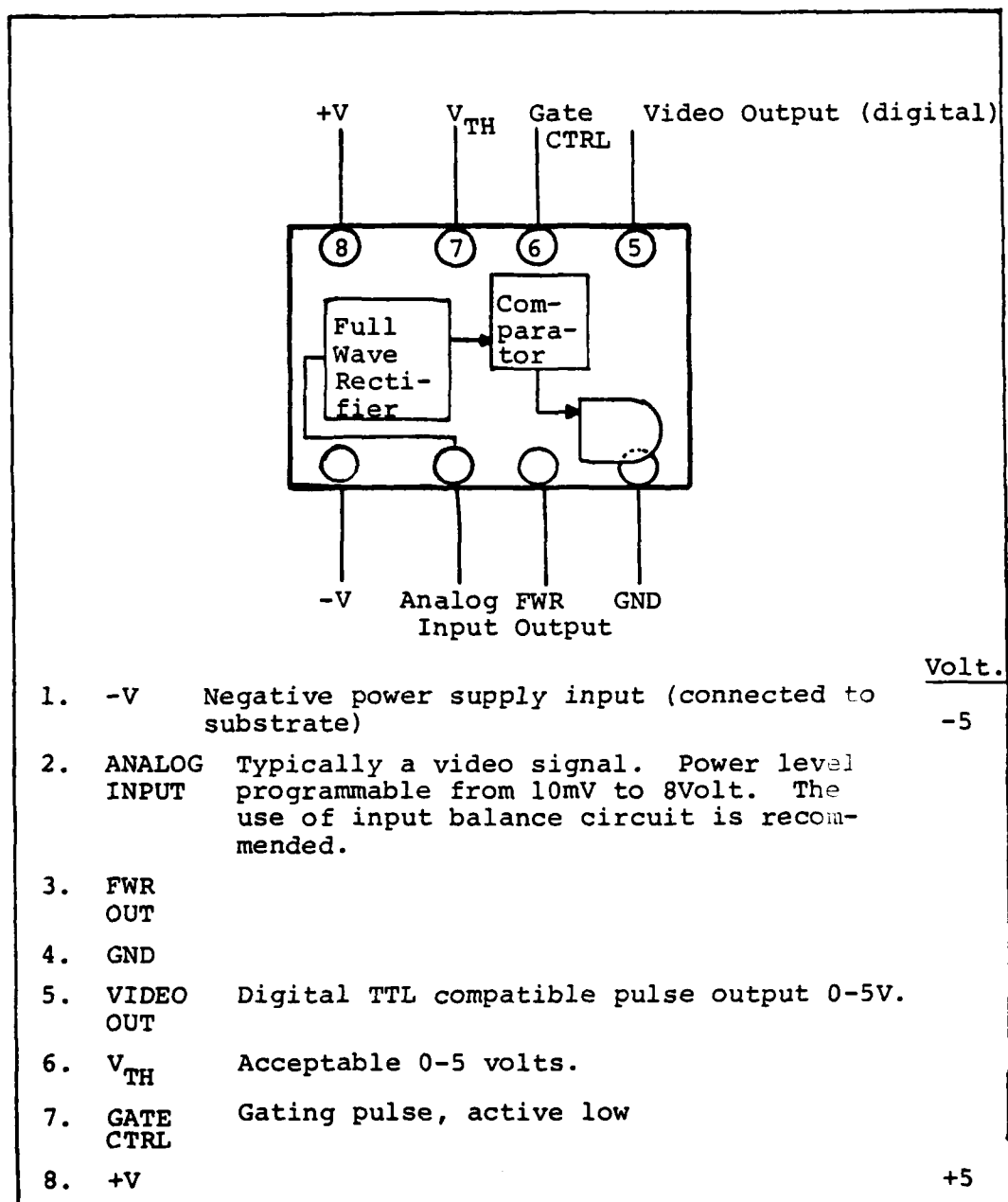Figure 14. Specification sheet of the VRIC; (a) packaging information, (b) functional and connections diagrams, (c) pin assignments.

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4. Typical Applications

Figure 15 shows the connection diagrams as: (a) FWR and (b) VRC in a RGF/MTI channel. Other applications may be (c) threshold circuit, (d) "AND" gate.
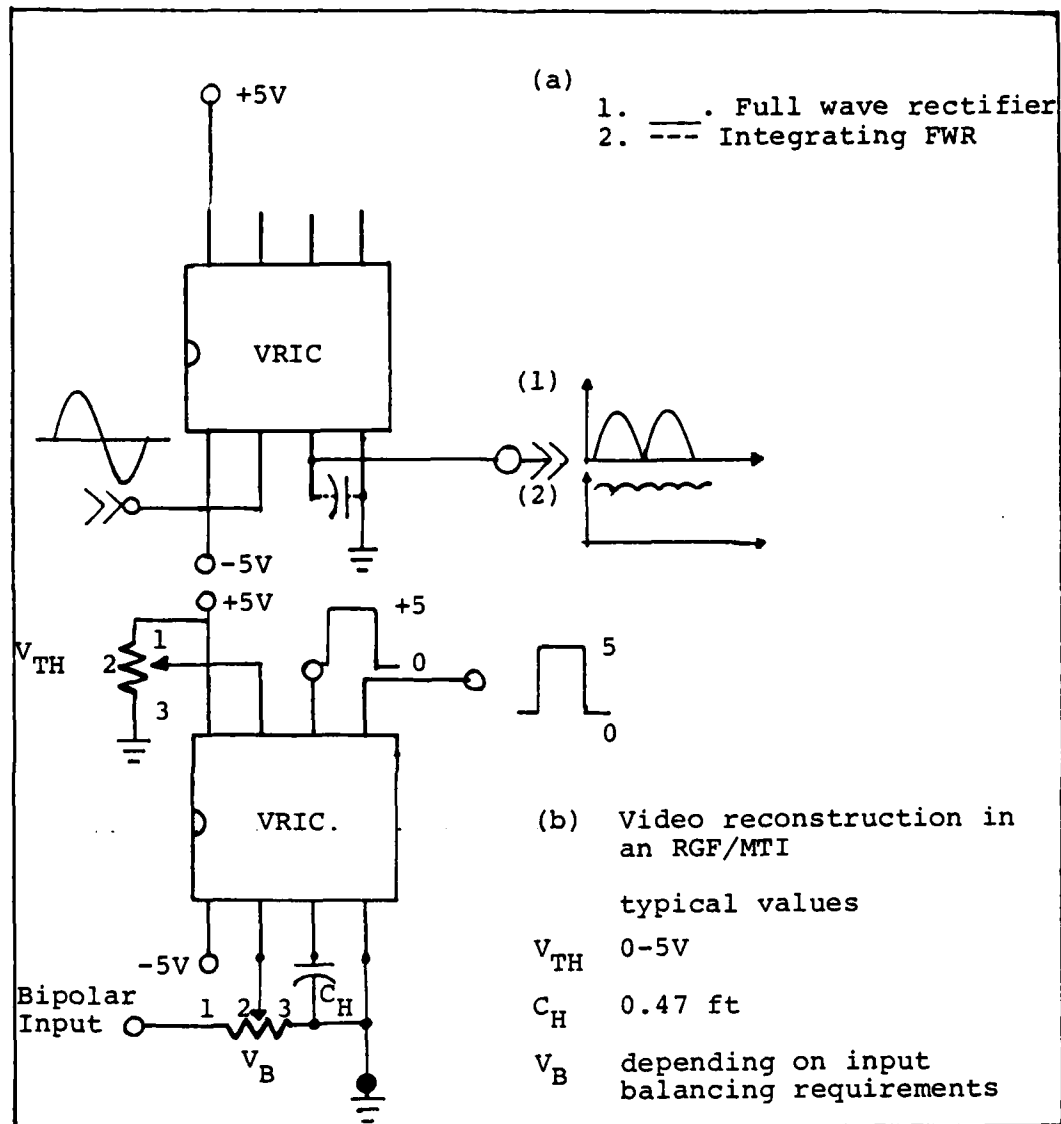
Figure 15.   Typical application configurations of the VRIC chip (developed from this thesis).

IV. EXPERIMENTAL PROCEDURE, PERFORMANCE EVALUATION, TESTS

A. BREADBOARDING

The schematic diagram of the VRIC (Figure 9) was imple-
mented using KH ports provided especially for semicustom
IC design. Electrical characteristics and connection dia-
grams for these parts can be found in Appendix B [3]. The
parts UO-001 and MO-003 were selected for the VRIC.

The connection diagram of the VRIC model (breadboard)
is shown in Figure 16. It should be noted that even though
the resistors have nominal values, they are shown as varia-
ble resistors. The reasons for this are:

1. It was found that almost all resistors of the
successful circuit configuration had to be corrected for
cross-under and line resistances on the layout (the circuit
was then retested).

2. For the "worst case" design, each resistor required
a wide range of values (this case is studied in Section B.1).

The VRIC configuration with the nominal resistor values
was first examined for proper operation. A sinusoidal wave-
form of about 1 KHZ was selected as an input "test" signal.
This is a very close approximation to the bipolar video used
in the real system. The input voltage level was selected
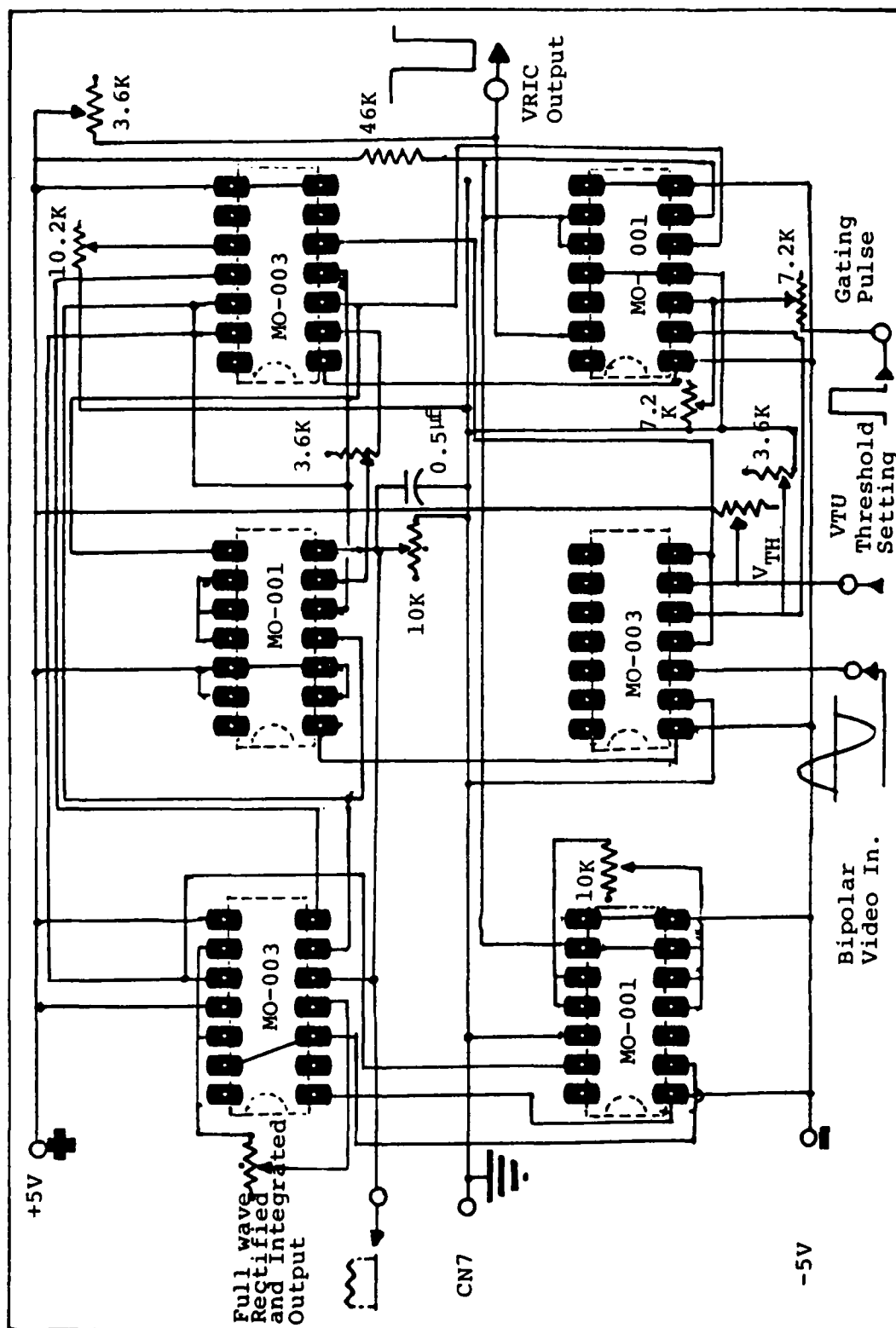to be 3 Vpp with the option to be variable from 100 mV to
20V for testing.

Figure 16. The VRIC model connections diagram.

Starting with an input signal variation of 100mV p-p the beginning of the full wave rectification was observed. As the input level was increased, the level of the rectified negative half cycle also increased from 0.5 to 7.0 Vpp at the input full wave rectification was "perfect." Beyond this "saturation" was observed until about 20 Vpp. Table II contains the values for the input and rectified voltages. Figure 17 is the plot of the output Vo versus the input Vi. This curve is the experimental characteristic curve of the device. Figures 18 and 19 contain the pictures of input/ output waveforms of all the stages from the oscilloscope. NOTE: The operating point of the device can be externally adjusted by an input balancing circuit which was added during the thesis testings.

B. TESTS

1. Worst Case Resistor Values

The components (transistors, resistors) fabricated on chips have Gaussian distribution of their parameters. Testings for "worst case" resistor values started by varying the nominal resistor values R1 through R10 within the limits of the region (a) 68% shown in Figure 20. The same was done in regions (b) 95% and (c) 99.8%.

For all the resistor variations except for R5 and R9, the effect on the output was observed to be small. The variations of R5 and R9, which are the current sources I1 and I2, had a large effect on I1 and I2 as it can be seen from the relations:

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TABLE II. VRIC Input/Output Voltage Measurements

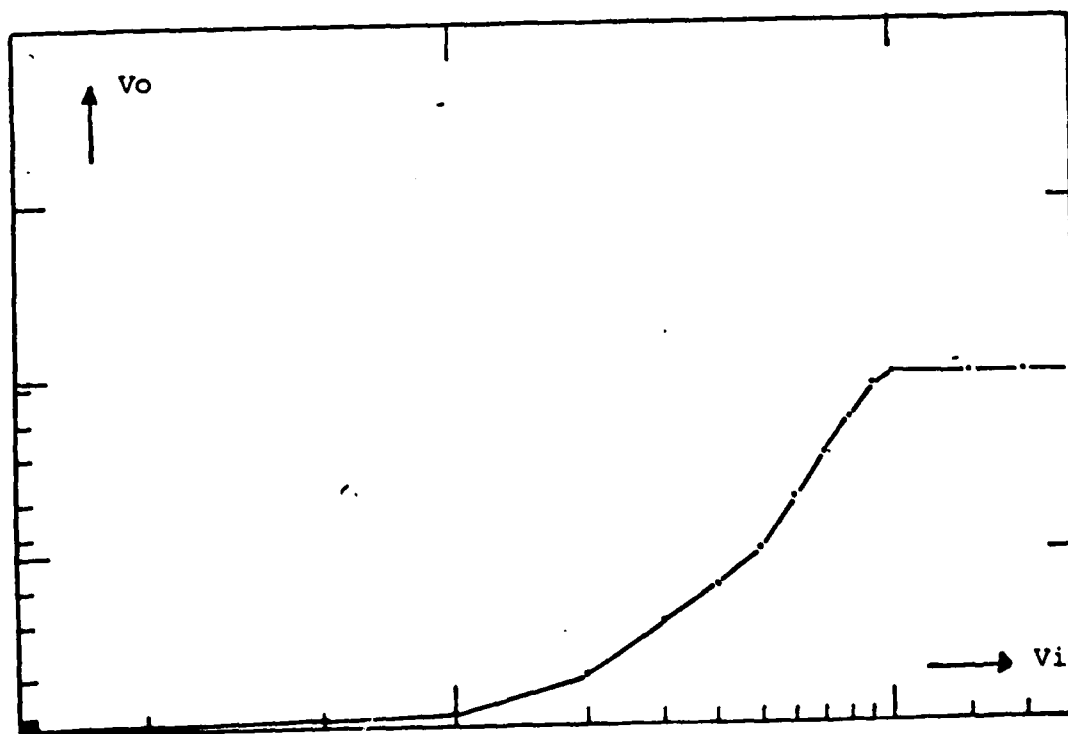|	Input (Vo)	Output (Vi)		Input	Output
1	<100mV	$\emptyset$	9	$5V_{pp}$	2.6
2	100mV	10mV	10	$6V_{pp}$	3.1
3	200mV	60mV	11	$7V_{pp}$	3.5
4	500mV	250mV	12	$8V_{pp}$	3.9
5	$1V_{pp}$	0.6V	13	$9V_{pp}$	4.0
6	$2V_{pp}$	1.2	14	$10V_{pp}$	4.0
7	$3V_{pp}$	1.6	15	$15V_{pp}$	4.0
8	$4V_{pp}$	2.2	16	$20V_{pp}$	4.0

Figure 17. VRIC characteristic curve (experimental). The curve is obtained from the plot of the values in Table II above.
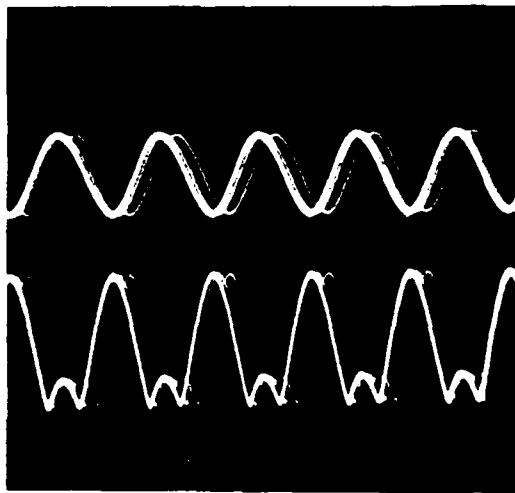
a. Scale: 100mV/division
800Hz

Vin = 100mV pp
Vo = 10mV dc

Rectification (FWR)
just begins.
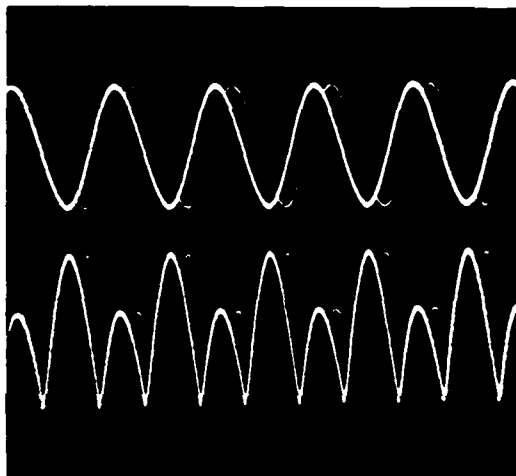
b. Scale: 100mV/division
800Hz

Vin = 200mV pp
Vo = 60mV dc
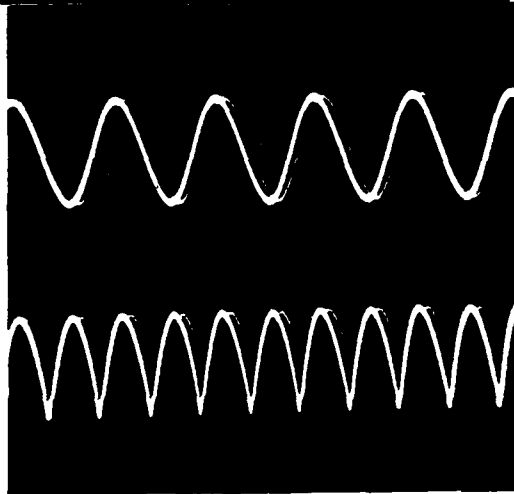
c. Scale: 500mV/division
800Hz

Vin = 1V pp
Vo = 0.6V dc

Symmetrical "perfect"
rectification.

Figure 18. Pictures of the input and FWR output waveforms
from the oscilloscope.
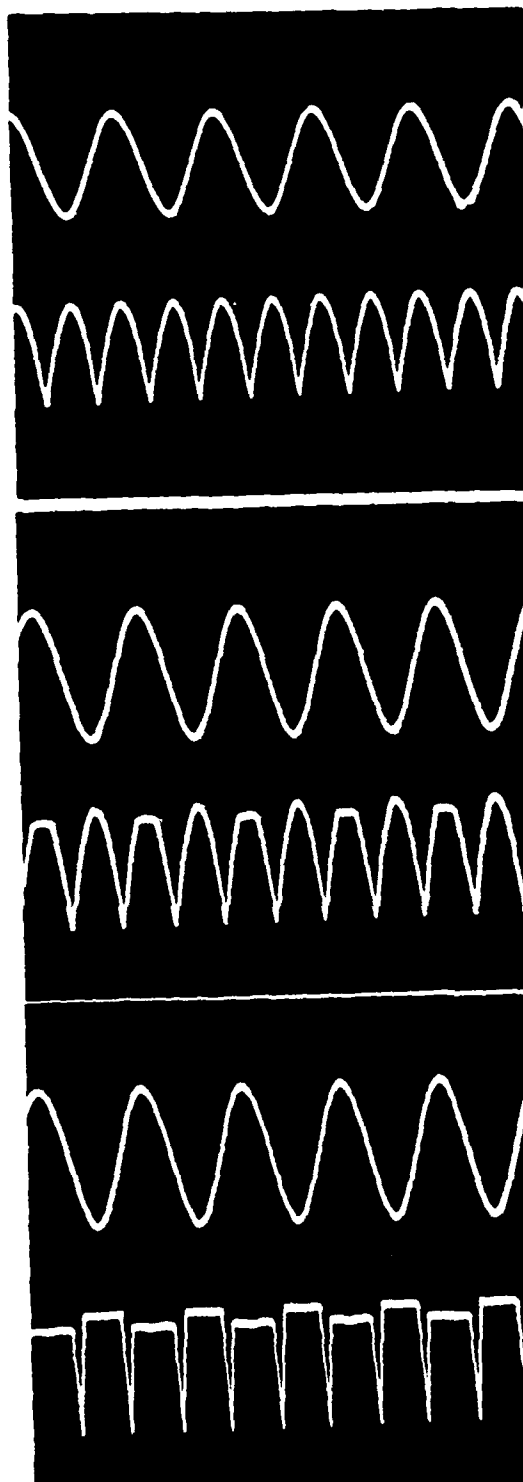
d. Scale: 2V/division
    800Hz

    Vin = 4 Vpp
    Vo = 2.2 V_{dc}

    Rectification is
    still "perfect."

e. Scale: 5V/division
    800Hz

    Vin = 10 Vpp
    Vo = 4 V_{dc}

    "Saturation" begins.

f. Scale: 10V/division
    800Hz

    Vin = 20 Vpp
    Vo = 4 V_{dc}

    Still in "saturation."

Figure 18. (continued)
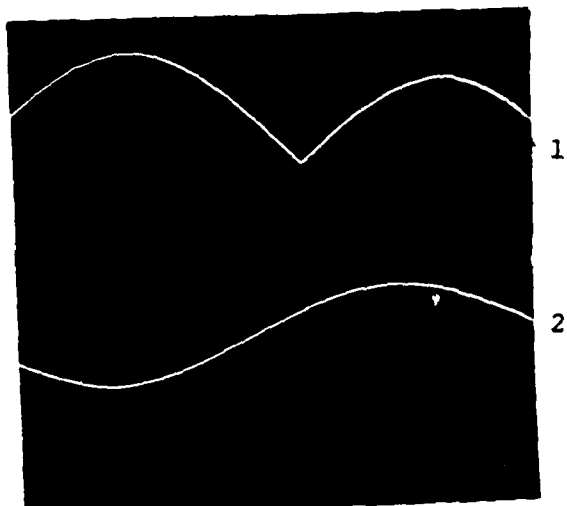
1

2

g. The full wave recti-
fier output (1) when
the input (2) is not
balanced. Note: The
second half cycle is
not at the same voltage
level as the first half
cycle.
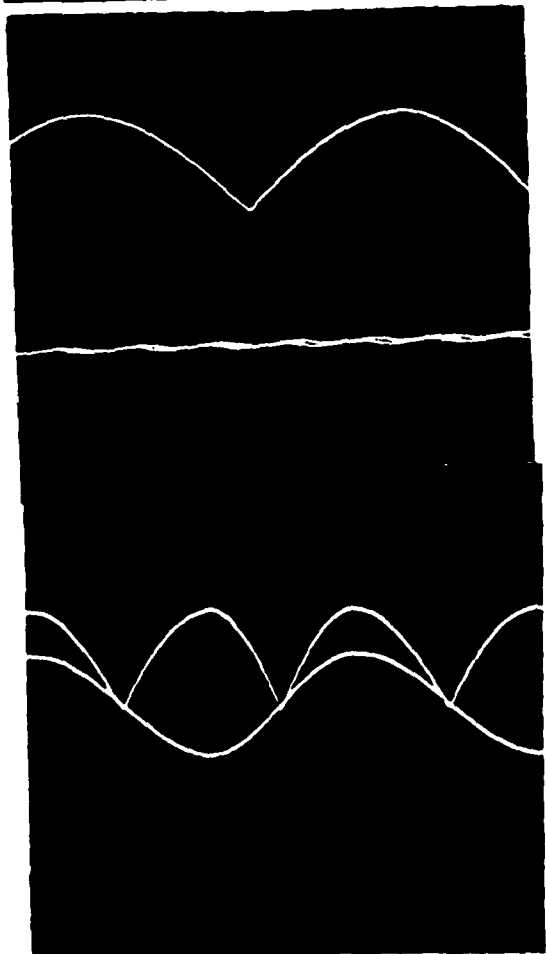
1

2

h.
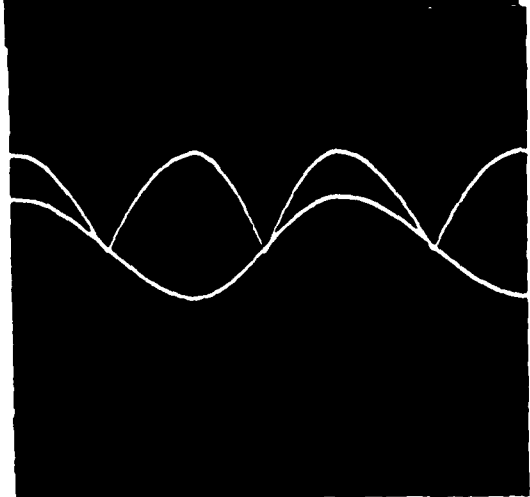
1

2

i. Superimposed input
and FWR output to
demonstrate the
rectification.

Figure 18. (continued)
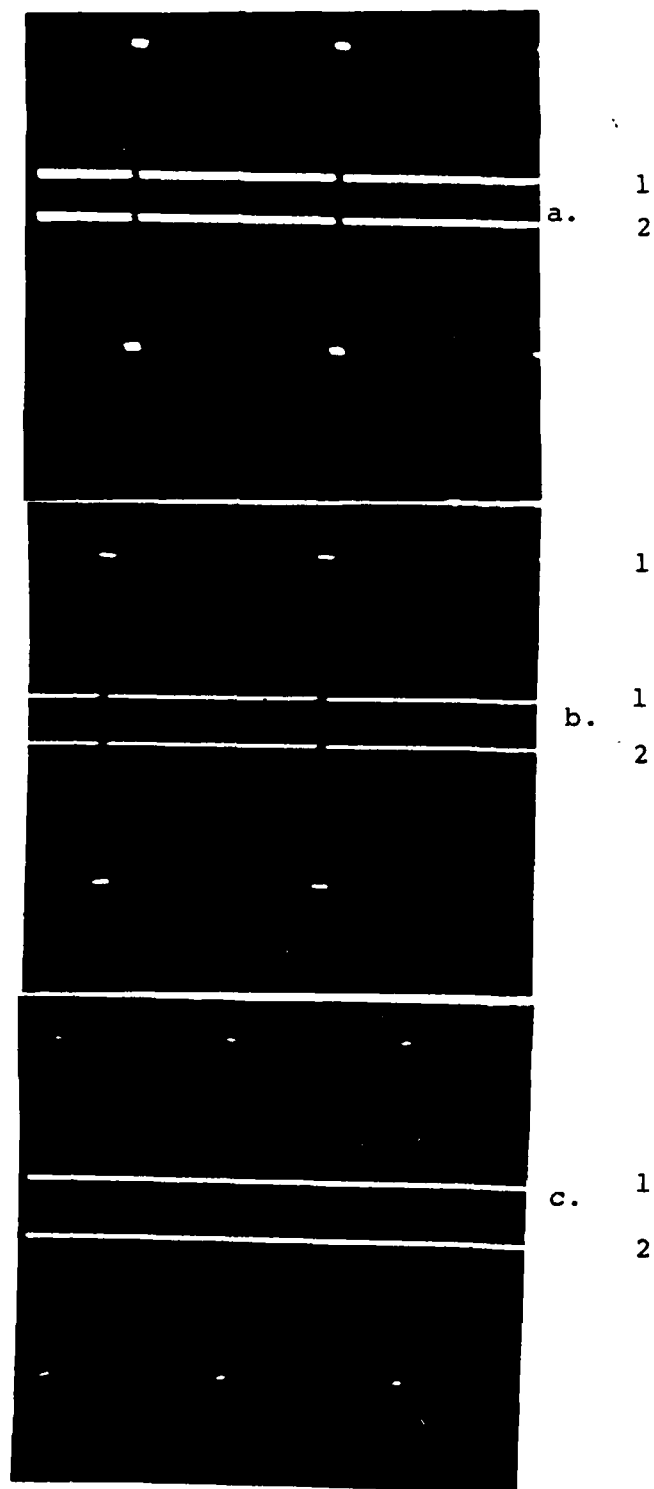
Figure 19. Gating pulse (1) and VRIC output (2). It can be seen that the duration of the negative output, follows the PW of the gating pulse.
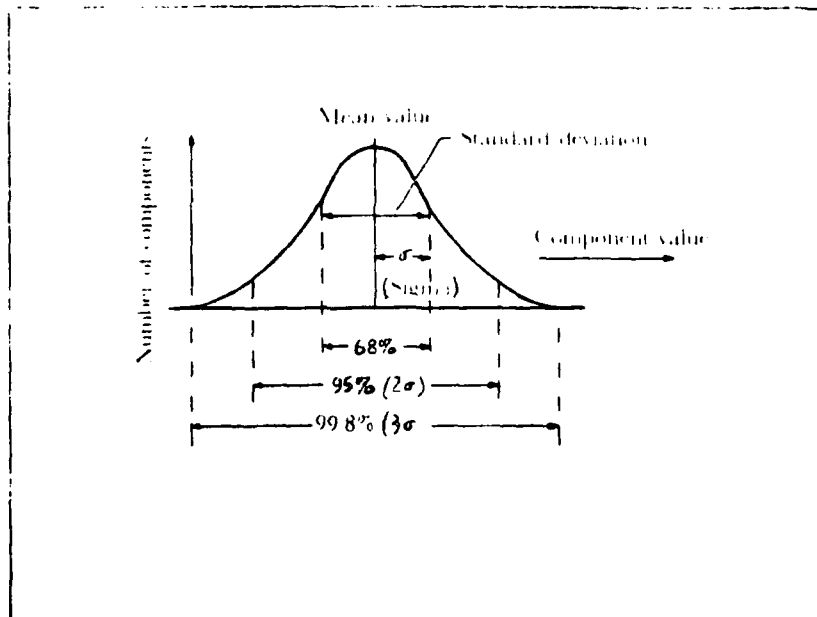
Figure 20.   Normal or Gaussian distribution with standard
deviation.
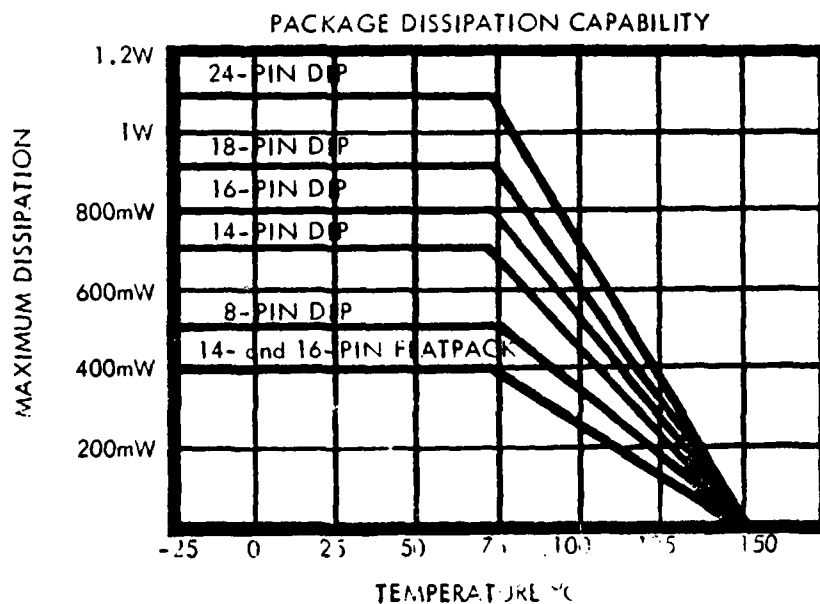
Figure 21.   Device maximum power dissipation.

$$I_1 = \frac{+V - V_{be} - (-V)}{R5}$$

$$I_2 = \frac{+V - V_{be}}{R9}$$

The optimum output response from the rectifier and the gate, the currents I1 and I2 were found (experimentally) to be 200xA and 400xA, respectively. Solving for R5 and R9 in the above equation:

$$R5 = 46K, \quad R9 = 10.2K$$

To overcome the sensitivity of the circuit with respect to resistor variation, the resistors R5 and R9 were implemented by using the maximum number of small value resistors in series and parallel combinations. This way the mean value of the combination was very close to the value of R5 and R9 (nominal).

2. Tests for Transistor Parameter Variation

The distribution of transistor parameter values such as h_{fe}, V_{be}, etc, is also Gaussian. To determine the effect on circuit operation the kit parts were interchanged/replaced many times. Some effect was observed on the shape of the output from the FWR but there was no effect on the integrated (dc) output. The cause of the FWR output shape variation was due to shifting of the operating point of some transistors to the beginning of the nonlinear portion of the characteristics. This effect was not considered to be significant and thus the operation was called "safe."

3. Substrate Current Measurements and Power Dissipation

Connecting all the substrate contacts to the most negative supply (-v) through a 10Ω resistor, the total current through the VRIC "device" was measured to be about 1.2mA. The maximum permissible current for the devices is 2mA [3]. Therefore the device was found to operate within its limits. The power dissipation (calculated) was 380mw (at room temperature, 25°C) which is a very satisfactory value for an 8 pin chip (Figure 21).

V. CONCLUSIONS

Several conclusions concerning the performance, the effectiveness, and the features of this device can be drawn from the design procedure and the performance evaluation of the VRIC on the 8 pin dual in-line IC package (DIP) developed in this thesis.

The original model of the circuit, on which this IC design is based, is the discrete circuit of the RGF/MTI channel integrated in the 20 channel MTI simulator that exists in the radar laboratory at the Naval Postgraduate School (NPS). This original circuit was constructed by N. Koral [1] in 1972 and was improved by C. J. Boyle [2] in 1975 and the laboratory personnel. The advantages, disadvantages, and performance of this circuit were dircussed in Part I. Results of the comparison between VRIC and the original circuit are listed in Table III and are explained below.

A. PERFORMANCE

The video reconstructor integrated circuit has 50% (3dB) improved performance over the video reconstructor circuit. The reason is that the half wave rectifier of the video reconstructor circuit utilizes only half the energy of the bipolar video signal (Doppler). The designed video reconstructor integrated circuit utilizes all the available energy.

B. SIZE

The video reconstructor circuit has fourteen components within a volume of 1¼" x 1¼" x 1" (1.5625 cubic inches) and the video reconstructor integrated circuit has thirty-two components in 3/8" x 1/4" x 1/8" (0.0117 cubic inches). Thus the video reconstructor integrated circuit occupies 75% less space. This difference is even greater if the total required space (for integration and cooling) will be considered.

The total size reduction that may result in a system from the use of the video reconstructor integrated circuit amounts to 150-200%.

C. POWER DISSIPATION

The maximum power dissipation for the video reconstructor integrated circuit is about 350mw and 1200-1500mw from the VRC. Thus the VRIC consumes 75% less power than the VRC.

D. SYSTEM DEVELOPMENT, MAINTENANCE AND SERVICE COST

For the integration of the video reconstructor integrated circuit in a system 13, only connections per channel are required for the video reconstructor circuit. Therefore, the cost of system development and service/maintenance is reduced by about 60%.

E. DEVICE SUPPORT AND DOCUMENTATION COST (DSCS)

The video reconstructor integrated circuit as a single chip required single unit support and documentation instead of the unit support/documentation required for the video

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reconstructor circuit. Therefore the device support and documentation cost is reduced by 80%.

F. PRODUCTION COST

From the cost analysis presented in Appendix D, it can be seen that the video reconstructor integrated circuit is more cost effective than the video reconstructor circuit for quantities greater than 5K/year. For RGF/MTI applications, a large number of gates (and thus video reconstructor integrated circuits) is required for each system. Therefore, even for a small number of radars, a large quantity of video reconstructor integrated circuits will be required and thus the production cost per device will be greatly reduced.

G. OTHER FEATURES OF THE VIDEO RECONSTRUCTOR INTEGRATED CIRCUIT

Some additional features of the video reconstructor integrated circuit, which are not available from the video reconstructor circuit, are listed below.

The importance of these features may not be readily apparent but it is the author's opinion that they may change in the feature many of the MTI design approaches in favor of the RGF/MTI. These features are:

1. Full TTL compatibility (and thus full programmability).

2. Integration (time constant, threshold/reference voltage output control signal) may be independently programmed to perform complicated operations required from a sophisticated radar system.

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TABLE III. Quantitive Figures from the Comparison of the
Discrete Video Reconstructor Circuit and the
Integrated Video Reconstructor Integrated Circuit

No.	Description	VRC	VRIC	
1	Performance	---	50% (3d)	better
2	Size	---	150%	smaller
3	Power consumption	---	75%	less
4	System development, maintenance and service cost	---	60%	less
5	Device support and documentation cost	---	80%	less
6	Production cost for production rate			
	(a) less than 5K/year	lower	---	
	(b) more than 5K/year	---		lower
			(percentage depends on real quantity)	

APPENDIX A

UPDATED RGF IC BUILDING BLOCKS

In this appendix the author presents three circuits
that may be used with the developed IC to implement a
complete and updated channel of the RGF/MTI and a "jittered"
PRF which can be used to serve the system.

1. Pseudorandom (Jittered) PRF System

A pseudorandom PRF system is a very desirable PRF in
MTI radars because it offers blind speed elimination and is
an excellent ECCM. Probably technical reasons keep this
system from general usage (difficult, complex implementation).
Most designers use staggered PRF with poorer results.

The design presented here (Figure 22) offers small
size, low power consumption and all the other advantages of
the compact IC designs.

The basic idea of this design was to use the digital
output of a pseudorandom sequence generator to generate a
voltage with approximately Gaussian distribution and to use
this voltage as a control voltage in a one shot multi-
vibrator (74123) to produce a pulse of period approximately
Gaussian. The requirements which necessitated the 74123's
use were:

a. The need of adjustment of the mean value (PRF)
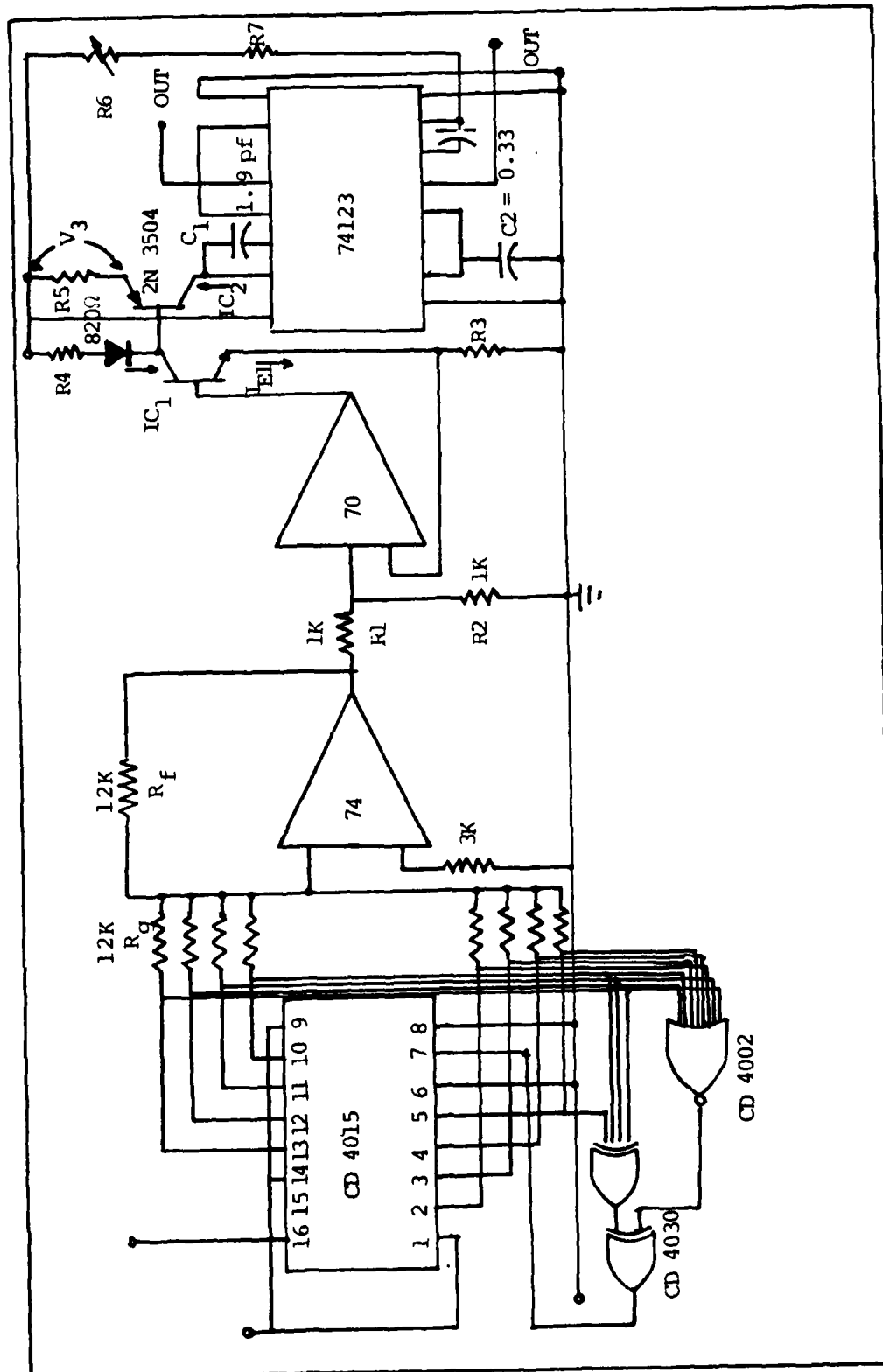close (but not on) to the nominal PRF value of the radar
system.

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Figure 22. A pseudorandom (jittered) PRF generator.

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b. The need to adjust the pulse width (pw=2) of the produced pulses to the radar's requirements.

The pseudorandom sequence generator (Figure 22) is implemented with a 4 or 8 bit shift register (CD 4015) which initially supresses the all zero condition with a 4/8 "NAND" gate. The NAND gate output and the main feedback output are EX-OR-ed to insure that the simultaneous effect on the DATA line will not occur. The main feedback is EX-OR-ing several outputs from the SR to cause RESET on the DATA in line. The feedback conditions are specified from the designer. It was found though that 03 and 04 of the 4 bit SR and 04,05,06,08 of the 8 bit SR give better results. Explaining the 4 bit SR in the feedback loop, Table IV is obtained as a result.

TABLE IV. Pseudorandom Sequence Generator True Table

Q1	Q2	Q3	Q4	Q3+Q4	EQ	V
1	1	1	1	0	4	20
0	1	1	1	0	3	15
0	0	1	1	0	2	10
0	0	0	1	1	1	5
1	0	0	1	0	1	5
0	1	0	0	0	1	5
0	0	0	0	1	1	5
1	0	1	0	1	2	10
1	1	0	0	0	2	10
0	1	0	0	1	2	10
1	0	1	0	0	3	15
0	1	0	1	1	2	10
1	0	0	0	1	2	10
1	1	0	0	1	3	15
1	1	0	0	1	3	15
1	1	1	1	0	4	20

From this table it can be seen that the 20V output occurs once, the 15V four times, the 10 volts six times, the 5V four times and this sequence (1, 4, 6, 4, 1) is repeated again.

The sequence 1, 4, 6, 4, 1 is recognized to be the binomial sequence. Since the binomial is a very good approximation to the Gaussian, it is called "pseudorandom" and the sequence pseudorandom sequence. Figure 23 shows the distribution of the summed voltage throughout one period. For convenience these voltages are scaled down in the summer using feedback resistance equal to the half of the R2.

The next step (refer to Figure 23) is a simple buffer stage, added forthe circuit protection.

The dual refrigerable os multivibrator performs pulse generation. A current (I_1) is proportional to the control voltage is generated from the voltage to current converter (Q1, Q2, D1) is charging the capacitor C_1 affecting in this way the output frequency. The voltage V_1 determined by the voltage divider R1/R2 is equal to V_2 and is:

$$V_1 = V_2 = (\frac{R2}{R1+R2}) \text{ Vin}$$

and since $I_{C_1} \cong I_{E_1}$

$$I_{C_1} = \frac{V_2}{R3}$$

$$= \frac{R2}{(R1+R2)R3} \cdot \text{Vin}$$

To keep $I_{B1,2}$ small, transistors with h_{fe} about 250 must be used.

The pulse width is given by:

$$PW = R6 \times R7 \times C3$$

and thus can be adjusted R6 or R7.
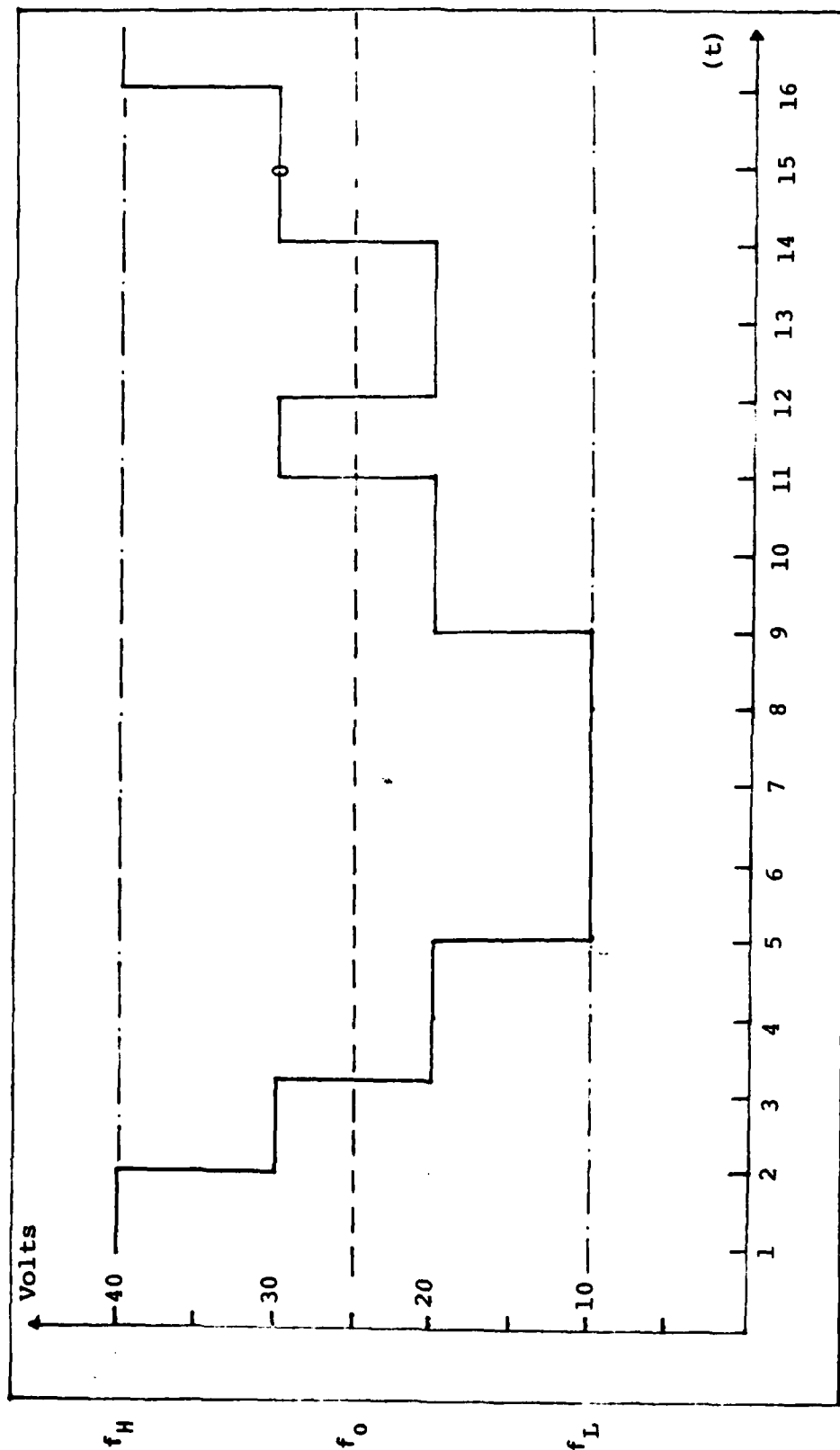
Figure 23. The distribution of the sum voltage from the pseudorandom sequence generator over one period.

The output frequency is given by:

$$f_o = \frac{1}{T + 60 \times 10^{-9} \text{ sec}}$$

where

T is the on time of the os which depends on the IC_1 (proportional to the control voltage).

2. Sample and Hold Circuit

The circuit in Figure 24 was built using a readily available, low cost IC and has very good performance. It is suggested, therefore, for the RGF implementation.

3. Gate Filter

For the gate filter an eighth order recursive sample analog comb filter may be used. The circuits for the delay lines that were used (SAD 512) were provided from the semiconductor Laboratory at NPS. Only one stage was built and tested (Figure 25). The input/output relationship is shown in Figure 26 together with the frequency response of the filter.
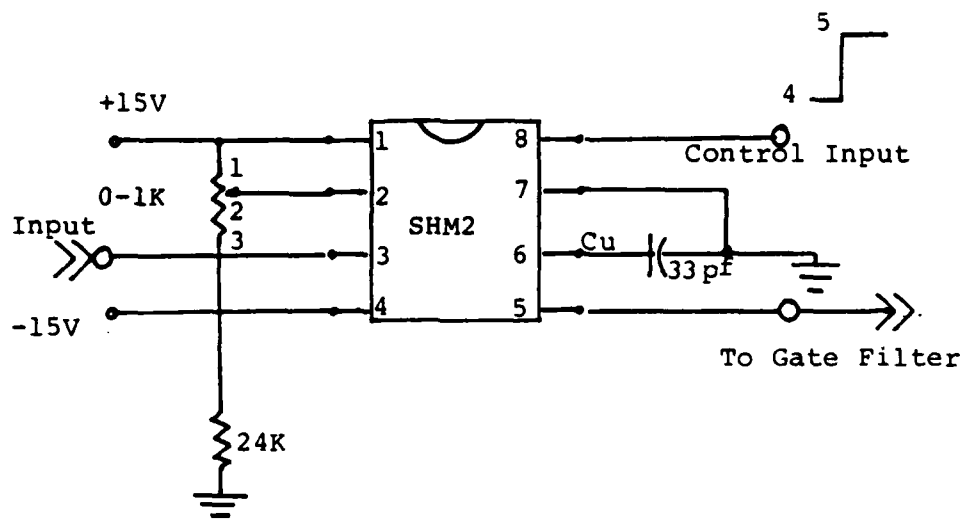
Figure 24. A sample and hold circuit (using a low cost IC) suitable for integration in the RGF/MTI channel.

$$H(z) = \frac{a_o + a_1 z^{-1}}{b_1 z^{-1}}$$
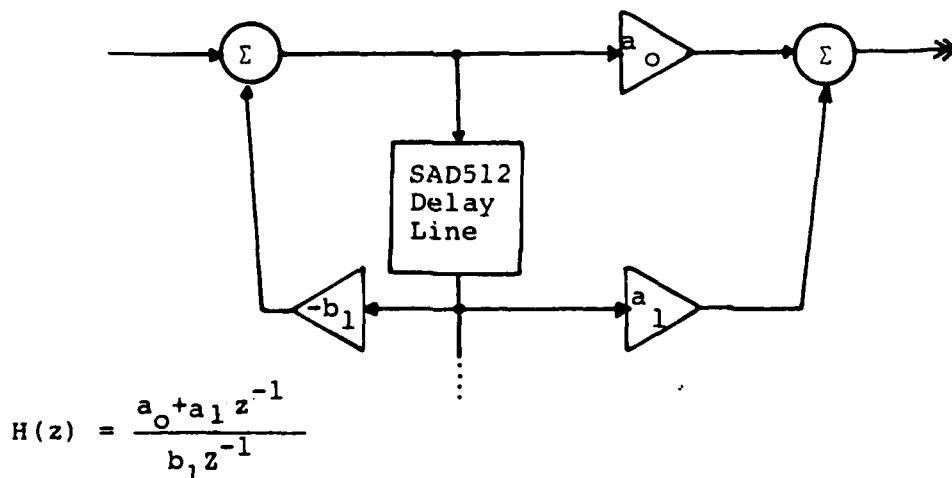
Figure 25. Block diagram of the first order recursive comb filter (can be expanded to any higher order. For transformation of the transfer functions, refer to [9].
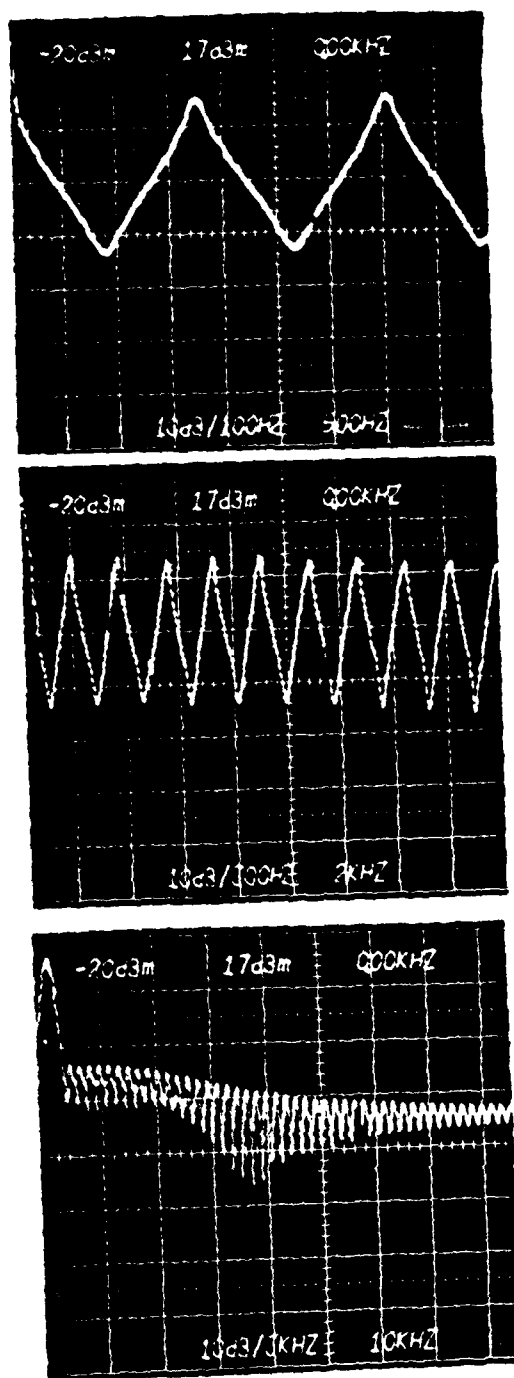
Figure 26. Pictures from the spectrum analyzer showing the frequency characteristics of the tested first order recursive comb filter.

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APPENDIX B

LAYOUT SHEETS FOR THE SEMICUSTOM DESIGN KIT PARTS

The layout sheets on the following pages are taken from
[3].

Linear bipolar   [illegible] NPN transistors   [illegible] 1.8 k ohms
260 components   [illegible] PNP transistors   [illegible] 3.6 k ohms
71 × 81 mils   15 Schottky diodes   [illegible] 30 k ohms (pinch)
16 pins max   16 resistors 200 ohms   [illegible] 100 k ohms (pinch)
20 volts max   43 resistors 450 ohms   [illegible] base resistance
[illegible]   43 resistors 900 ohms

Figure 27.   Monochip A.

Linear, bipolar
300 components
81 × 81 mils
24 pins max
20 volts max
69 small signal transistors
12 PNP transistors
16 Schottky diodes

_____ ohms
_____ ohms
_____ k ohms
_____ k ohms
_____ 40 k ohms (pinch)
_____ 100 k ohms (pinch)
_____ k ohms base resistance

Figure 28.   Monochip B.

80

Linear, bipolar
110 components
51 × 56 mils.
14 pins max.
20 volts max
22 small NPN transistors
8 PNP transistors
6 Schottky diodes
8 resistors 200 ohms
18 resistors 450 ohms
20 resistors 900 ohms
13 resistors 1 8 k ohms
10 resistors 3 6 k ohms
2 resistors 30 k ohms
(pinch)
all ohms base
resistance

Figure 29.   Monochip C.

81

Linear, bipolar
209 components
80 × 80 mils
16 pins max.
36 volts max.
50 small NPN transistors
16 dual PNP transistors
15 resistors 200 ohms
30 resistors 450 ohms
14 resistors 900 ohms
9 resistors 1.8 k ohms
4 resistors 3.6 k ohms
resistors 60 k ohms

metal-gate resistance

Figure 30.   Monochip D.

Linear, bipolar
200 components
70 × 70 mils
18 pins max
20 volts max
48 small NPN transistors
15 dual PNP transistors
8 resistors 200 ohms
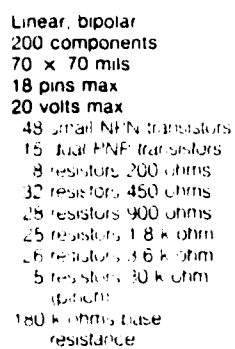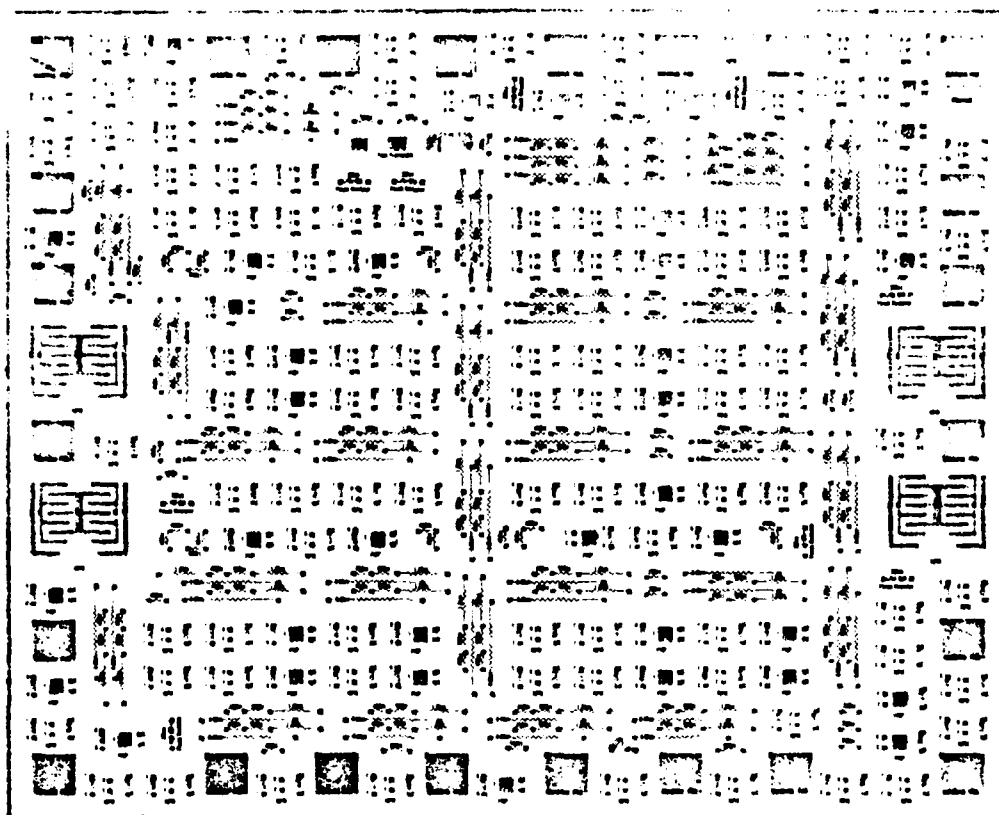32 resistors 450 ohms
28 resistors 900 ohms
25 resistors 1.8 k ohm
26 resistors 3.6 k ohm
5 resistors 30 k ohm
(pinch)
180 k ohms base
resistance

Figure 31.   Monochip E.

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Linear, bipolar
460 components
91 × 110 mils.
24 pins max.
20 volts max.
  92 small NPN transistors
   4 large NPN transistors
 36 dual PNP transistors

18 resistors 200 ohms
88 resistors 450 ohms
68 resistors 900 ohms
61 resistors 1.8 k ohm
61 resistors 3.6 k ohm
  9 resistors 30 k ohm (pinch)
433 k ohms base resistance

Figure 32. Monochip F.

84

Linear, bipolar
310 components
75 × 78 mils.
18 pins max.
20 volts max.
58 small NPN transistors
2 large NPN transistors
18 dual PNP transistors

19 resistors 200 ohms
68 resistors 450 ohms
65 resistors 900 ohms
44 resistors 1.8 k ohms
27 resistors 3.6 k ohms
8 resistors 60 k ohm (pinch)
269 k ohms base resistance

Figure 33.   Monochip G.

85
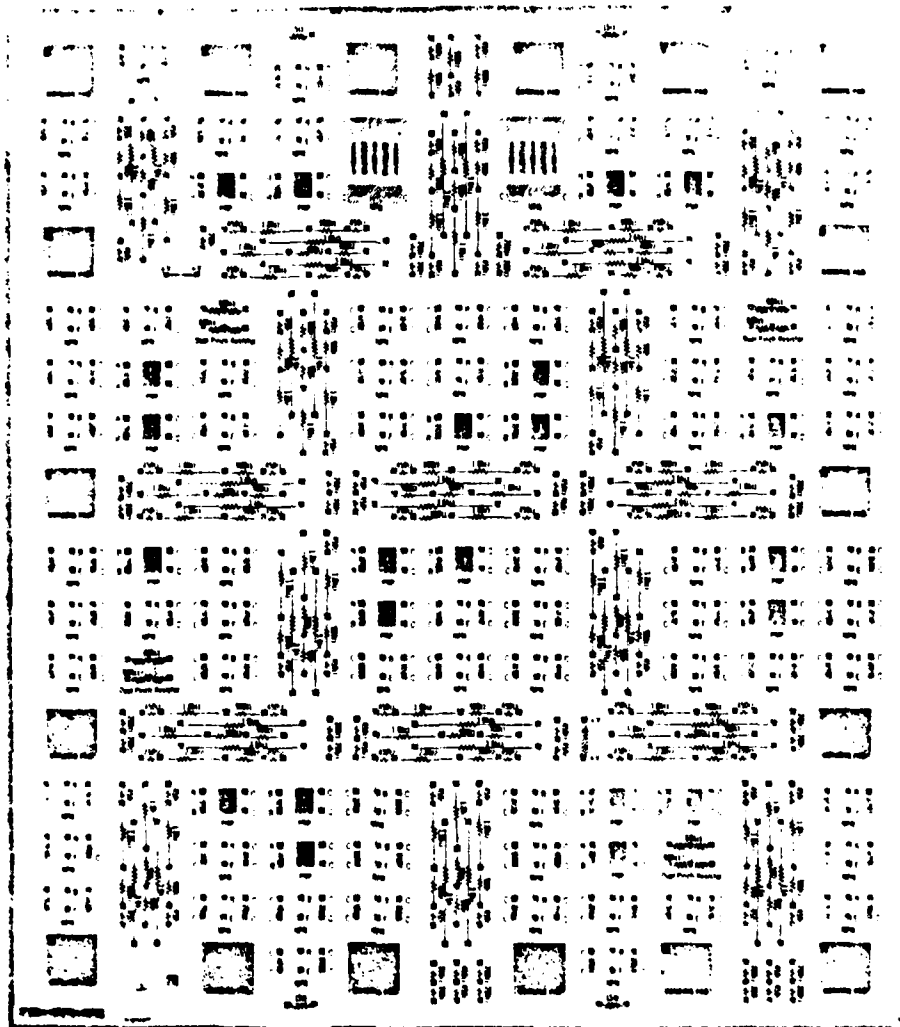
Linear, bipolar
202 components
77 × 88 mils.
18 pins max.
20 volts max.
70 small NPN transistors
2 medium transistors
22 dual PNP transistors
29 resistors 200 ohms
82 resistors 400 ohms
75 resistors 900 ohms
54 resistors 1.8 k ohms
36 resistors 3.6 k ohms
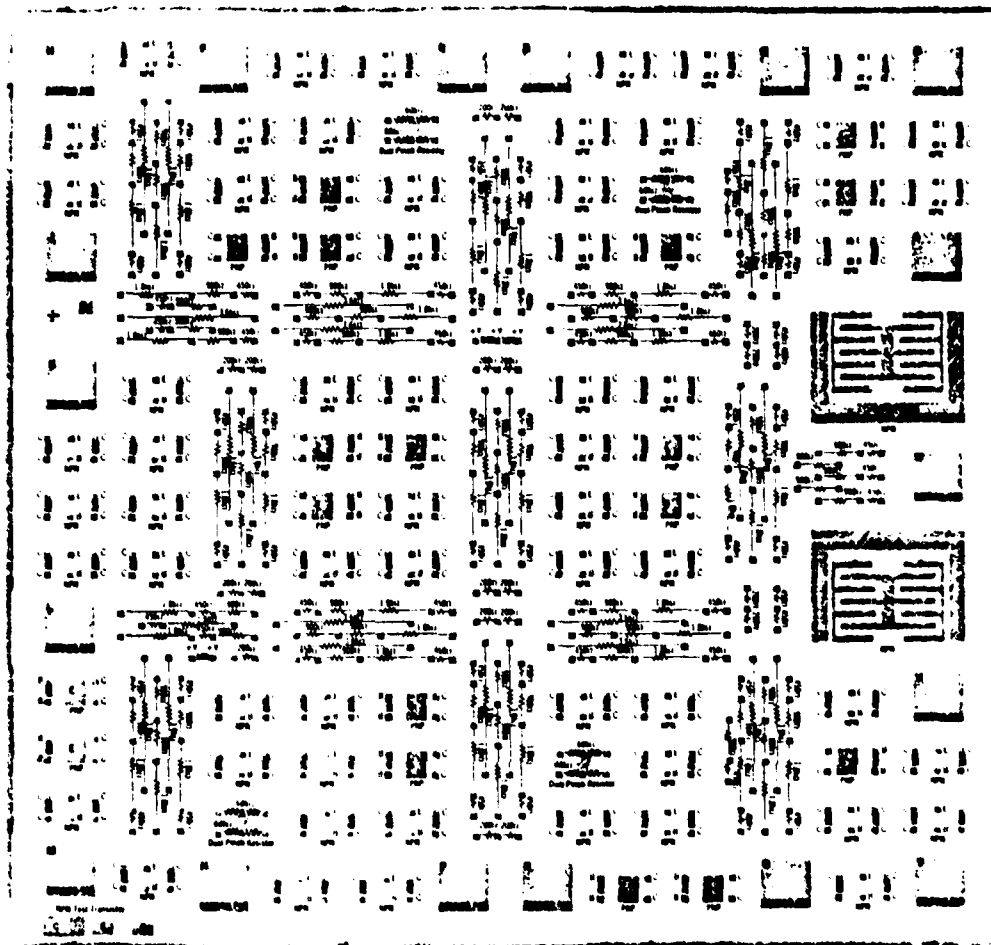8 resistors 60 k ohms
(pinch)

Figure 34.   Monochip H.

Linear, bipolar
251 components
81 × 100 mils.
24 pins, max.
20 volts max
76 small NPN transistors
2 medium NPN transistors
2 large NPN transistors
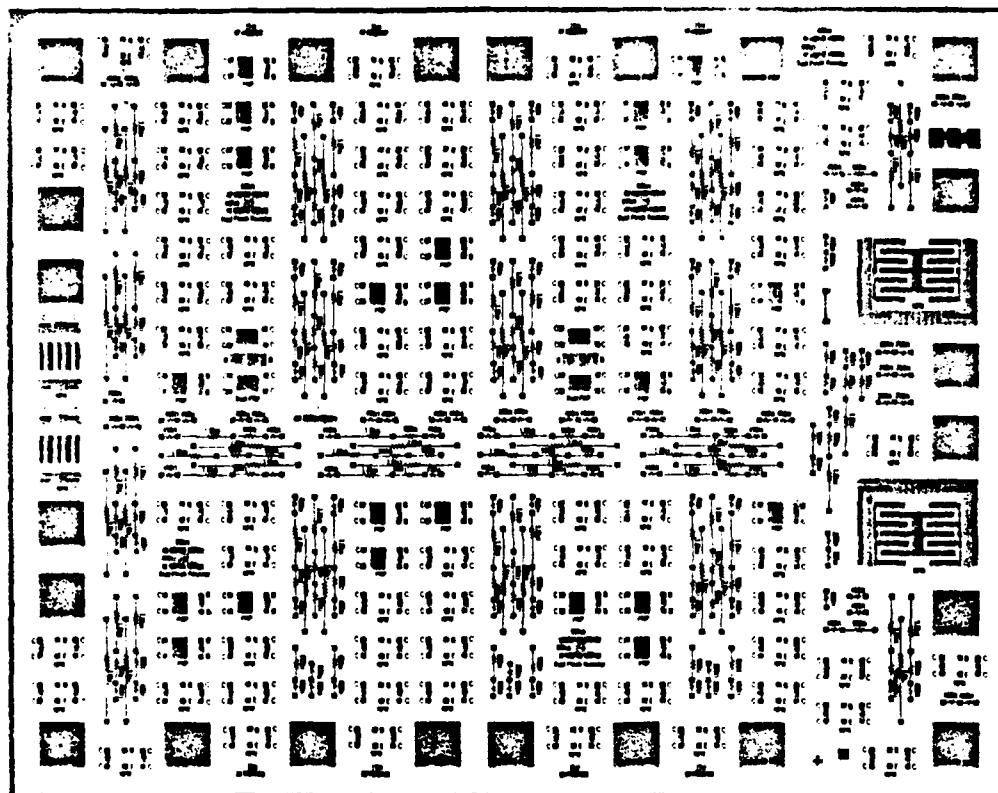
22 dual PNP transistors
4 quad PNP transistors
23 resistors 200 ohms
103 resistors 450 ohms
77 resistors 900 ohms
53 resistors 1 8 k ohms
36 resistors 3 6 k ohms
10 resistors 60 k ohms
(pinch)

Figure 35.   Monochip I.

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Linear, bipolar
168 components
61 × 65 mils.
18 pins max.
20 volts max.
36 small NPN transistors
2 medium NPN transistors
12 dual PNP transistors
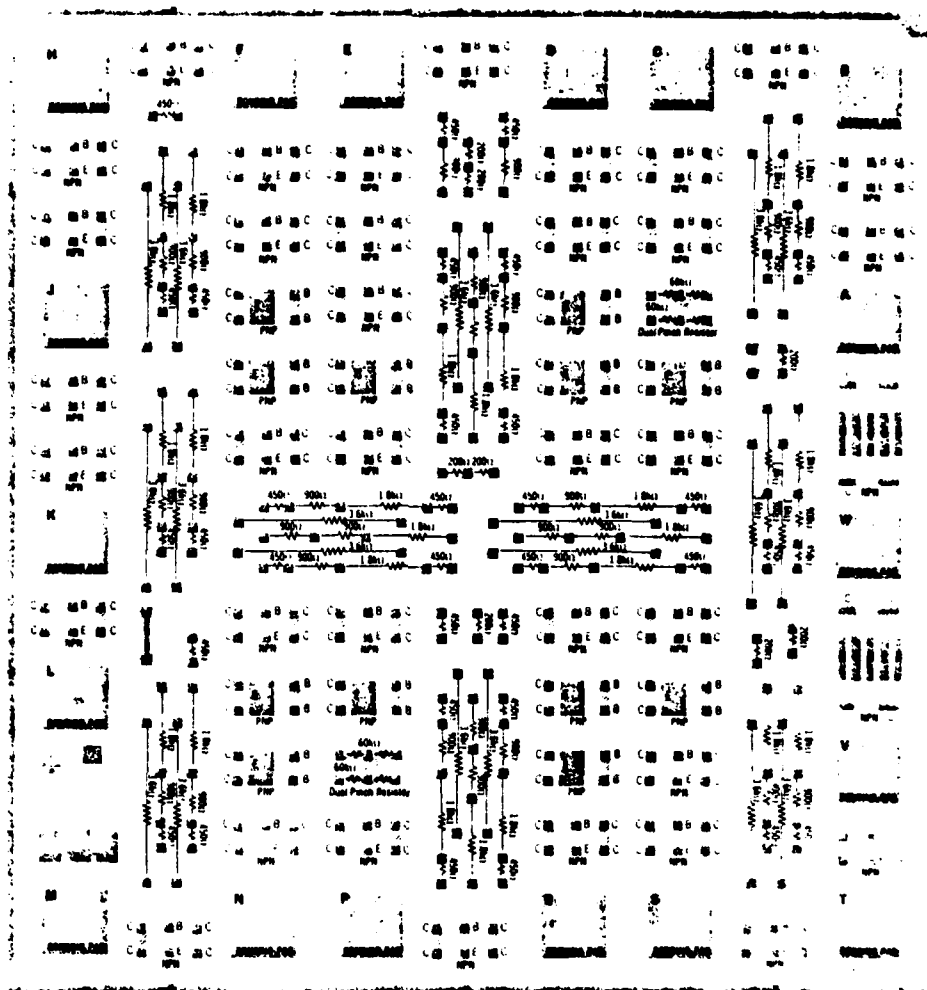8 resistors 20 ohms
34 resistors 450 ohms
30 resistors 900 ohms
24 resistors 1 8 k ohms
20 resistors 3 6 k ohms
4 resistors 60 k ohms
(pinch)

Figure 36. Monochip J.

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APPENDIX C

ANALYSIS OF THE RECTANGULAR PULSE AND RECTANGULAR PULSE TRAIN

1. Generation of the Rectangular Pulse

A continuous in time domain signal can be specified by a set of parameters (independent of the papercut choice of the time origin).

$$f(t) = \sum_n f(n)\phi_n(t)$$

$$\cong \sum_{n=1}^{N} f(n)\phi_n(t)$$

where:

$\phi n(t)$ is a linearly independent set of functions defining the internal structure of $f(t)$.

$f(n)$ is a set of numbers.

The internal square error, due to the approximation in the second equation, is:

$$\int_{t_1}^{t_2} |\varepsilon_n(t)|^2 dt = \int_{t_1}^{t_2} |f(t) - \sum_{n-1}^{N} fn\phi_n(t)|^2 dt$$

and is minimized by proper choice of the set $f(n)$. Defining

$$K_n = \int_{t_1}^{t_2} |\phi_n(t)|^2 dt$$

then

$$\int_{t_1}^{t_2} |\varepsilon_N(t)|^2 dt = \int_{t_1}^{t_2} |f(t)|^2 dt - \sum_{n-1}^{N} |fn|^2 Kn$$

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and

$$K_n = 1 \text{ for all } n \text{ in the set.}$$

NOTE: The first number of the equation for the square error is the energy contained in $f(t)$ which is assumed to be finite.

$\phi_n(t)$ must be such that:

$$\lim_{n=\infty} \int_{t_1}^{t_2} |\epsilon_N(t)|^2 dt = 0$$

Thus, for the complete orthogonal set it is:

$$f(t) = \sum_{n=1}^{\infty} f(n) \phi_n(t)$$

$$\int_{t_1}^{t_2} |f(t)|^2 dt = \sum_{n=1}^{\infty} |fins|^2 Kn$$

$$f(n) = \frac{1}{Kn} \int_{t_1}^{t_2} f(t) \phi_n^*(t) dt =$$

$$= \frac{\int_{t_1}^{t_2} f(t) \phi n^*(t) dt}{\int_{t_1}^{t_2} |\phi_n(t)|^2 dt}$$

The last equation is recognized to be Parserval's theorem. The expression of a set of functions such as $f(t)$ by an infinite set of mutually orthogonal functions is called "Generized Fourier Series Representation of $f(t)$.

The rectangular function:

$$f(t) = \begin{cases} 1 & ; \ 0<t<1 \\ -1 & ; \ 1<t<2 \end{cases}$$

has finite energy and can be expressed by a set of functions as it was described above. Assume that it is chosen:

$$\phi_n(t) = Sin(n\pi t); \quad n>0$$

Since Sin(nnt) and Sin(mnt) are orthogonal then:

$$\int_{t_1=0}^{t_2=2} Sin(n\pi t)\ Sin(m\pi t)\,dt = \begin{cases} 1 & ; \ n=m \\ 0 & ; \ n\neq m \end{cases}$$

and therefore it can be written:

$$f(t) = \sum_{n=1}^{\infty} f(n)\ Sin(n\pi t)$$

$$= \frac{\displaystyle\int_0^2 f(t)\ Sin(n\pi t)\,dt}{\displaystyle\int_0^2 Sin^2(n\pi t)\,dt}$$

$$= \int_0^2 f(t)\ Sin(n\pi t)\,dt =$$

$$= \int_0^1 Sin(n\pi t)\,dt - \int_1^2 Sin(n\pi t)\,dt =$$

$$= \left.\frac{cos(n\pi t)}{n\pi}\right|_0^1 + \left.\frac{cos\ n\pi t}{n\pi}\right|_1^2 =$$

$$= \frac{1}{n\pi}\,[1-(-1)-((-1)-1)]$$

Thus

$$f(n) = \begin{cases} \dfrac{4}{n\pi} & :n \text{ odd } (n=2K+1) \\ 0 & :n \text{ even } (n=2K) \end{cases}$$

$$K = 0,\ 1,\ 2,\ 3\ldots.$$

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and

$$\phi_n = \text{Sin}(n\pi t); \quad n > 0$$

So

$$f(t) = \frac{4}{n} \left(\text{Sin}(\pi t) + \frac{1}{3} \sin(3\pi t) - \frac{1}{5} \sin(5\pi t) + \dots \right)$$

The error due to the introduced approximation is shown in C.1.(b) and it is analyzed as follows:

$$\int_{t_1}^{t_2} |\epsilon_n(f)|^2 dt = \int_{t_1}^{t_2} |f(t)|^2 dt - \sum_{n-1}^{N} |f(n)|^2 k$$

$$\int_0^2 |\epsilon_1(t)|^2 = 2 - \left(\frac{4}{\pi}\right)^2 \qquad\qquad =0.379; \quad N=1$$

$$= 2 - \left(\frac{4}{\pi}\right)^2 - \left(\frac{4}{3\pi}\right)^2 \qquad\qquad =0.1999; \quad N=3$$

$$= 2 - \left(\frac{4}{\pi}\right)^2 - \left(\frac{4}{3\pi}\right)^2 - \left(\frac{4}{5\pi}\right)^2 \qquad =0.134; \quad N=5$$

$$= 2 - \left(\frac{4}{\pi}\right)^2 - \left(\frac{4}{5\pi}\right)^2 - \left(\frac{4}{7\pi}\right)^2 \qquad =0.101; \quad N=7$$

From a plot of these, it can be seen that 95% of the energy is contained in the first 4 terms since the higher order term (i.e., N-9) becomes insignificant. Therefore, the function generator, as a physical device, does not generate the ideal waveform

$$f(t) = \begin{cases} 1 & 0 < t < 1 \\ -1 & 1 < t < 2 \end{cases}$$

but generates the waveform

$$f(t) = \frac{4}{\pi} \left(\cos\ (\omega_o t) - \frac{1}{3} \cos\ (3\omega_o t) + \right.$$

$$\left. +\frac{1}{5} \cos(5\omega_o t - \frac{1}{7} \cos\ (7\omega_o t) + \dots \right.$$

2. The Use of the Gate Function as Sampling Function

Applying the transformation formula, the frequency domain presentation of a rectangular pulse train is obtained as follows:

$$F(n) = \frac{1}{T} \int_{T/2}^{T/2} f(t) e^{-jn\omega_o t}\, dt$$

$$= \frac{1}{T} \cdot \int_{T/2}^{T/2} A e^{-jn\omega_o t}\, dt = -\frac{A}{jn\omega_o t}\ e^{-jn\omega_o t/2}\ {}_{-e}{}^{jn\omega_o t}$$

$$= \frac{2A}{n\omega_o t}\ \frac{e^{jn\omega_o t/2} - e^{-jn\omega_o t/2}}{2j} = \frac{2A}{n\omega_o t}\ \mathrm{Sin}\,(n\omega_o t/2)$$

$$= \frac{A}{n\omega_o T/2} \cdot \frac{2}{\tau} \cdot \mathrm{Sin}\,(n\omega_o \tau/2) = \frac{A\tau}{T}\ \frac{\mathrm{Sin}\,(n\omega_o t/1)}{n\omega_o t/2}$$

where

τ = PW, pulse width

T = PRT, pulse repetition period

$F(o) = \frac{A\tau}{T}$, the magnitude factor

$\frac{\mathrm{Sin}\,(n\omega_o \tau/2)}{n\omega_o \tau/2}$ = envelope or sampling function

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APPENDIX D

COST ANALYSIS FOR THE IC DESIGN

Items a through g are considered as "fixed" costs [7], items h through l are considered as "variable" or "unit" costs. This procedure is related to the production cost of either a circuit implemented with discrete components or with an integrated circuit semicustom designed. These are analyzed below:

a. Circuit Design and Breadboard

The semicustom design is more expensive since it is a new development and incorporates new technology. However, the difference in cost is not large. After all with the monochip concept, the engineering time spent on the design was not more than the time required for the design of the original discrete circuit.

b. IC Layout

The layout of the metalization mask which provides the interconnection between the component of the IC design, required additional time. There is no equivalent procedure for the discrete circuit design for comparison. Table III shows the estimated work time requirements. The monochip type D used for 80-90% utilization of the area requires 35 to 60 working hours.

3. IC Tooling Fee

The charges for the integration procedure covering tooling, test equipment, material and engineering development

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TABLE III. Estimated Working Time for the Layout Development
(time in manhours)

Chip Utilization %	Chip Type				
	A	B	C	D	E
60	15	10	5	10	10
70	25	20	10	20	20
80	60	45	20	35	35
90	100	80	80	60	60

cost for the first 50 units of the production, at the present time, amounts to $2800. The cost per unit, after the base production quantity, depends on the production per year requirements (up to 100,000/year) and may be anywhere between 5 to 7 dollars each.

c. DC Board Layout

A DC board layout with a custom IC requires considerably less time than the discrete circuit layout because of the reduced number of interconnections. The size of the IC layout compared with discrete computations may be as low as 1:50.

d. Reliability Testing

The cost for standard reliable tests of the semicustom IC is about the same but the quality level of the IC is always superior due to the reduced number of components.

e. Special Package Development

The effectiveness of the package development can be seen in c and d above.

f. Documentation

A semicustom or custom IC reduces the documentation cost related to component count. Items requiring documentation are:

(1) assembly procedure

(2) testing procedure

(3) PC board debugging procedure

(4) components and vendor listing

(5) inventory control procedures.

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g. Overhead

The overage development overhead cost is 100% on top of item (a) through (f). This covers supervisory personnel, facilities cost, indirect supplies, power, etc.

h. Components

The component portion depends on the chip size, the package type and the production quantity.

i. Supplier

The cost of supplies associated with the production is about the same for an IC or discrete design.

j. DC Board

The current cost of the DC boards in quantities of 1000 is:

(1) set up charge--$100-$200

(2) single-sided boards--$0.037-0.005 psi

(3) double-sided boards--$0.065-0.075 psi

(4) cost per drilled hole--$0.025-0.0035

The DC board size requirement for an IC design is significantly lower and thus the cost is less (about 50%).

k. Direct labor

(The costs compared concern)

(1) assembly

(2) tests

(3) reworked tests

l. Overhead

The cost of the production overhead consists of:

(1) Supervision

        (a)   On line supervision per hourly employees;
                44% of the direct labor, total.

        (b)   One section leader per three line supervisors;
                25%, 95% of the direct labor, total.

        (c)   One general manager per four section leaders;
                8% of the direct labor, total.

        (d)   One corporate officer per three general
                managers; 3% of the total direct labor costs.

(The Supervisor's salary rate for (a) 175 percent, (b) 300 percent
(c) 400 percent, (d) 500 percent.

      (2) Purchasing and Stocking

      (3) Inventory

      (4) Quality Assurance

      (5) Field Service

  m. Conclusions on the IC Cost Reduction

      (1) Smaller, simpler PC board

      (2) Less incoming inspection

      (3) Reduced component insertion time

      (4) Less rework

      (5) Smaller supervisory overhead

      (6) Smaller purchasing, stocking, inventory cost

      (7) Reduced quality assurance cost

      (8) Less frequent field service

Because the production cost is a function of the per year
quantity, the semicustom IC design is cost effective for
quantities of 5,000 units per year.

    Conclusions and application of the entire IC design are
given in Section IV.

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