LEVEL II

12

RAYTHEON

DGM

FAMILY OF
DIGITAL GROUP
MULTIPLEXERS

FINAL

9 FINAL TYPE

TECHNICAL REPORT,

ON

6 DIGITAL GROUP MULTIPLEXERS (DGM)

FAMILY OF EQUIPMENTS.

DGM PROGRAM

CONTRACT NO. DAAB07-75-C-0036

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CDRL SEQ. NO. G037

11 JANUARY 1980

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PREPARED FOR:
UNITED STATES ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY

PREPARED BY:
RAYTHEON COMPANY
EQUIPMENT DIVISION
COMMUNICATIONS SYSTEM LABORATORY
SUDBURY, MASSACHUSETTS 01776

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APPENDIX

A	IC Cross Index	

PREFACE

List of
Acronyms vs. Nomenclature
of the DGM Equipments

Nomenclature	Acronym	Description
C-10716( )/TRC	OCU-1	Orderwire Control Unit - 1
C-10717( )/TRC	OCU-2	Orderwire Control Unit - 2
MD-1023( )/G	LSCDM	Low Speed Cable Driver Modem
MD-1024( )/G	HSCDM	High Speed Cable Driver Modem
MD-1025( )/G	RLGM/CD	RLGM Cable Driver
MD-1026( )(P)/G	GM	Group Modem
MD-1065( )(P)/G	103 MOD	AN/GRC-103 Radio Modem
TD-1218( )/G	LSPR	Low Speed Pulse Restorer
TD-1219( )/G	HSPR	High Speed Pulse Restorer
TD-1233( )/TTC	RLGM	Remote Loop Group Multiplexer
TD-1234( )/TTC	RMC	Remote Multiplexer Combiner
TD-1235( )/TTC	LGM	Loop Group Multiplexer
TD-1236( )/G	TGM	Trunk Group Multiplexer
TD-1237( )/G	MGM	Master Group Multiplexer
TS-3647( )/G	COU	Cable Orderwire Unit

NOTICE

The Final Type Technical Report (CDRL G037) on the DGM equipment is an update of the Design Plan Document (CDRL B019). All future tense sentences which were used in the Design Plan should have been changed to present or past tense. There is a chance, however, that not all of the tense changes were caught during review. In actual fact the equipment design is complete and this notice is incorporated to alert the reader to possible incorrect tense usage.

SECTION 1

SUMMARY

This report describes the work done on the Digital Group Multiplex family of equipments. This family of equipments is a component of the TRI-TAC system and works with the TRI-TAC switch, AN/TTC-39; the Communications Nodal Control Element, AN/TSQ-111; and a number of inventory ATACS equipments.

The equipment is designed in accordance with the specification TT-B1-2202-0013A and subsidiary specifications referenced therein. One of those specifications is unique to the DGM family: EL-CP0163-0001, the TEMPEST requirement.

In this report, the system design, electrical design, and mechanical design is discussed. EMI design is included in both electrical and mechanical sections. Reference is made to other data items that cover maintainability, reliability, and nuclear designs.

SECTION 2

SYSTEM DESIGN

The most far reaching system problem is the orderwire. In this section calculations are presented which justify the choice of orderwire concepts. The unit design sections following then carry these concepts into the affected equipments. Some aspects of interunit timing are also discussed in the system section. The final telemetry concept is discussed. Framing coordination is common to all units and is also presented here.

2.1 DIPHASE GROUP MODEM ORDERWIRE DESIGN

The diphase group modem is required to carry traffic on CX-11230 cable at 14 different rates plus a secure voice orderwire plus 2 kb/s telemetry at rates of 256 kb/s and above. This section addresses the means by which these signals are to share the same cables. An analog orderwire can replace the secure voice orderwire and telemetry.

2.1.1 DESIGN GOALS AND REQUIREMENTS

The GM handles traffic at rates from 72 to 4608 kb/s. The distance over which it must transmit depends on the rate as follows:

Rate (kb/s)	Maximum Distance (miles)
Up to 576	2
1024 to 2304	1
4096 and 4608	1/2

The secure orderwire was either the VINSON at 16 kb/s or the PARKHILL with a 300 to 2700 cps band. The same channel can also handle an unsecure analog maintenance orderwire. It is desirable that the maintenance orderwire use only passive circuitry in the GM. This can be done if the maintenance orderwire is put on the cable without modulation.

2.1.2 DESIGN APPROACH

The original specification requirements for a line rate equal to the traffic rate implied the use of Frequency Division Multiplex (FDM) techniques to add the orderwire and telemetry signals to the traffic signal. The FDM approach was analyzed at great length using computer techniques and found to be inadequate. It was not possible to provide secure orderwire and telemetry below a traffic rate of 512 kb/s. Even at that rate, a considerable technical risk in the performance of actual modem circuitry remained. The results of this analysis are presented in paragraph 2.1.3 below.

In an effort to eliminate the traffic rate restriction, three other alternatives were considered:

a. Time Divisior Multiplexing (TDM) - This would put the 16 and 2 kb/s signals in the traffic bit stream. The line rate would then be higher than the traffic rate. The lowest line rate would be 640 kb/s, thus providing sufficient frequency space for the analog orderwire to be added at baseband using FDM techniques. The analog orderwire could be either a secure PARKHILL system orderwire or an unsecure maintenance orderwire. To be precise, this is a hybrid TDM/FDM system, but will be referred to subsequently as a TDM system for simplicity.

The TDM approach can be adapted to use with equipments not having a system orderwire or telemetry. To do this, each traffic rate has two line rates. The higher rate provides system orderwire and telemetry using TDM. The lower rate is equal to the traffic rate, and provides only a maintenance orderwire. All traffic rates from 72 to 4608 kb/s will be handled this way.

b. Space Division Multiplexing - If the orderwires were put on WF-16 field wire laid along side the CX-11230, there would be no interference problems. Laying the field wire at the same time as the cable would seem to be no great problem, but this scheme has not generated much enthusiasm.

c. Multi-Sampling - The low rates could be built up to some fixed high rate, say 2048 mb/s, and the higher rates sent unmodified. This limits the distance to one mile from 72 to 2304 mb/s, and also suffers from an unacceptable increase in line rate similar to the TDM approach.

d. Change of Requirements - The FDM approach can be made to work if the requirements are changed. The new FDM approach is based on the present requirements:

For rates at and above 256 kb/s - 16 kb/s secure voice plus 2 kb/s telemetry or analog maintenance order wire.

For rates from 72 to 288 kb/s - Analog maintenance order wire only.

2.1.3 DETAILED DESIGN DESCRIPTION

2.1.3.1 FDM Calculations, Original Requirements

In this section, we will determine the signal to interference requirements, the telemetry carrier frequency, filter performance, minimum traffic rate, and guidelines for setting the relative levels of the three signals. Since all quantities interact, we must approach the problem by assuming one or more quantities, calculating the others and seeing if the system will work with the original assumptions. If not, the original assumptions are changed and the calculations repeated. The calculations given here are the result of several iterations of this process.

Figure 2-1 shows a block diagram of the signal paths in the GM. The orderwire signal passes through two low pass filters, assumed identical. High pass filtering in this path is assumed to have negligible effect. The telemetry signal is modulated on the carrier and then put through two band pass filters. Again there will be negligible high pass filtering. The traffic is put through two high pass filters. Furthermore, the cable plus cable equalizer acts as a low pass filter to the traffic.

Let us assume the bandwidths of the low pass filtering, and get from that the eye degradation of the orderwire and telemetry. The orderwire low pass filter is assumed to have a 3 dB point at $\sqrt{2}$ times its bit rate, or

22.63 kHz. The telemetry band pass filter is assumed to have 3 dB points at $2\sqrt{2}$ times its bit rate, or 5.66 kHz. This gives similar eye patterns. The size of the eye pattern after two identical low pass filters is given in Figure 2-2. At the bandwidths chosen, the degradation with respect to the peak signal is about 1 dB for either three or four pole filters.

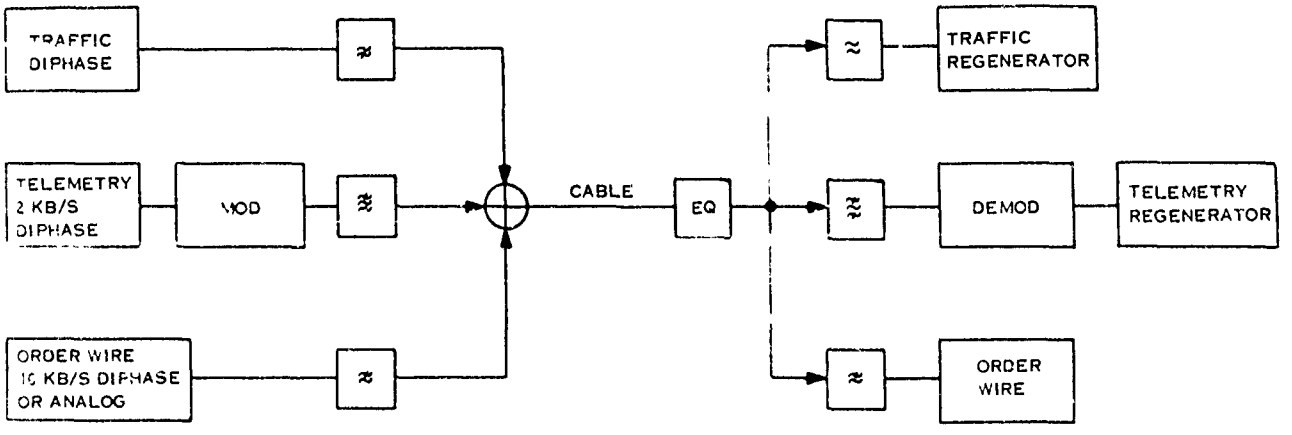


Figure 2-1. Signal Paths in GM, FDM Approach, Original Requirements

Let us calculate the minimum value of signal to interference ratio that the filtering must provide. We assume that the total peak interference must be at least 3 dB below the eye opening. This means that the total peak interference must be at least 4 dB below the peak signal of both the orderwire and the telemetry. Each of the three signals on the line receives interference from the other two. We assume that the allowance should be divided equally, so any one should be 6 dB below the total (peak addition). Therefore, any one interference should be at least 10 dB below the peak signal.

There is no assurance that this allowance is enough to work with actual modems until well along in the breadboard phase. Therefore, the system designer will plan to give better performance wherever possible. A more desirable figure would be 20 dB.

Let us now set the telemetry carrier frequency and the number of poles in the orderwire and telemetry filters. From previous iterations it is known that the choice of telemetry carrier frequency is not the limiting factor in

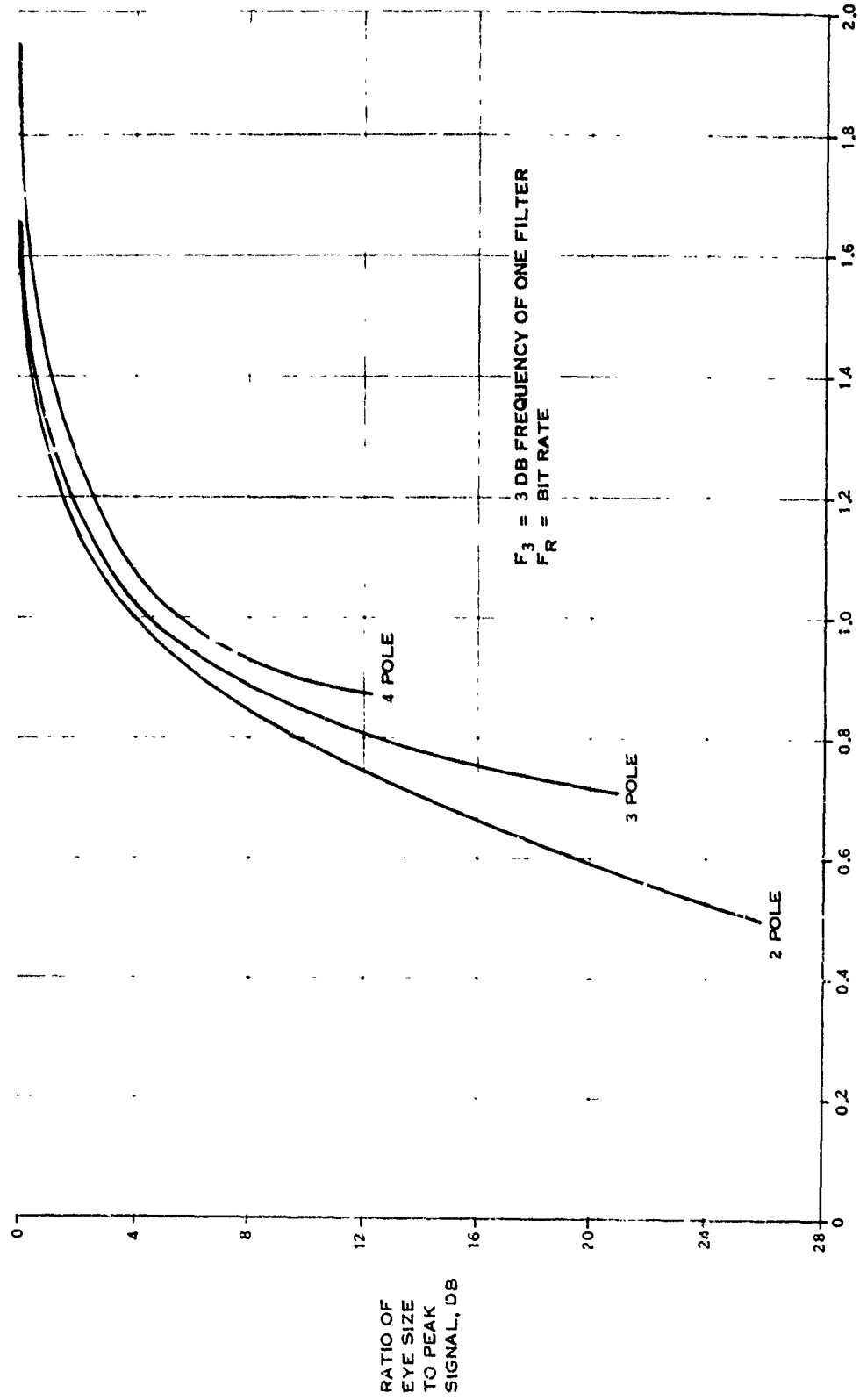


Figure 2-2. Eye Degradation By Two Low-Pass Filters

the overall modem performance, therefore we can allow ourselves to set the frequency on the basis of 20 dB signal-to-noise ratio.

The carrier frequency is set by examining the interference between orderwire and telemetry. Figure 2-3 shows the interference from the orderwire to the telemetry as a function of the carrier frequency. The number of poles in the carrier filter is a parameter. All frequencies are normalized to the bit rate of the orderwire. We obtain the following results:

f_o (kHz)	Atten (dB) 3 Pole	Atten (dB) 4 Pole
24	15	15
28	27	35
32	37	40
36	37	39
40	32	33

Note that over most of this range, there is very little advantage in using a four pole filter. Therefore, we choose a three pole band pass filter.

Figure 2-4 shows the interference from the telemetry to the orderwire as a function of carrier frequency. The number of poles in the low pass filter is a parameter. All frequencies are normalized to the bit rate of the telemetry. We obtain the following results:

f_o (kHz)	Atten (dB) 3 Pole	Atten (dB) 4 Pole
24	5	3
28	6	8
32	8	16
36	11	25
40	14	31

Note that above 28 kHz, there is considerable advantage in using a four pole filter. Therefore, we choose a four pole low pass filter.

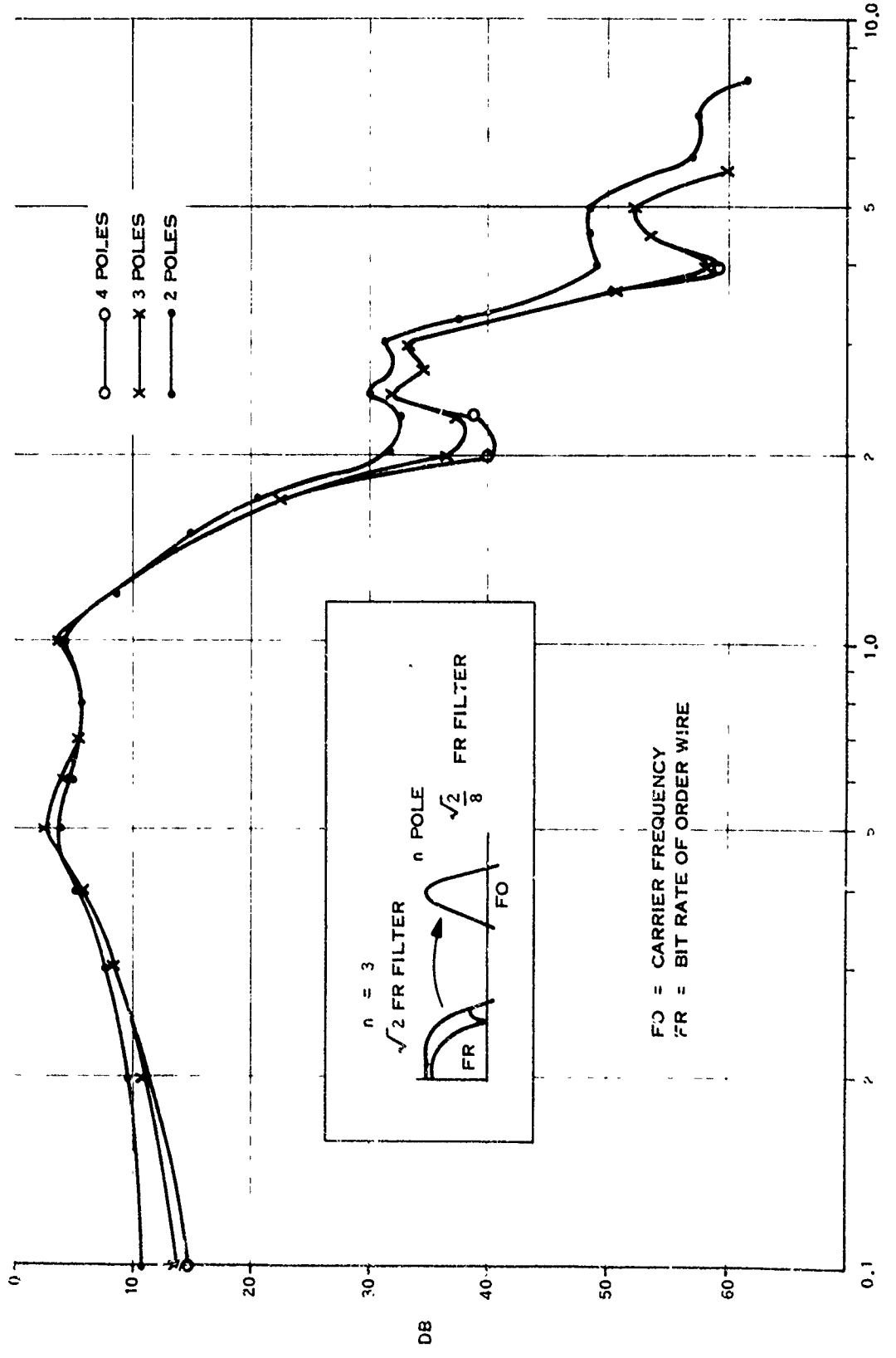


Figure 2-3. Interference Attenuation from Orderwire to Telemetry

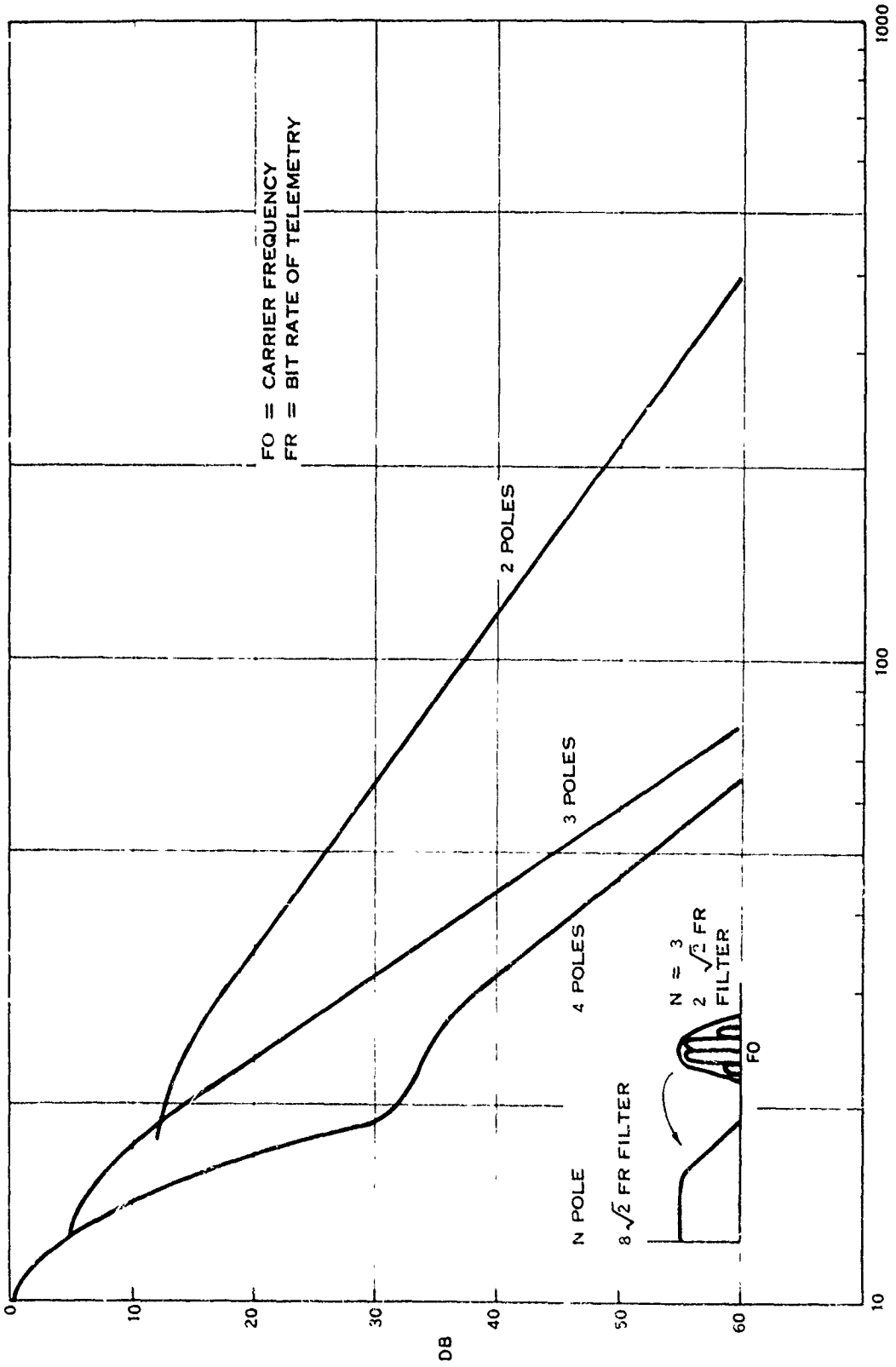


Figure 2-4. Interference Attenuation from Telemetry to Orderwire

One of the parameters we have at our command is the relative level of the signals. Therefore, the easiest way to determine the carrier frequency is to set a limit on the sum of the attenuations from the telemetry to the orderwire and from the orderwire to the telemetry. Afterwards, the levels can be adjusted to equalize performance. The minimum value for this sum is 20 dB, but the desired value is 40 dB. The sum is:

f_o (kHz)	Sum of Attenuations (dB)
24	18
28	35
32	53
36	62
40	68

If we are to be precise, we should, at this point, correct the sum of the attenuations to allow for the effect of varying cable lengths, which changes the relative received levels given fixed transmit levels. However, from previous iterations, it is known that this correction is about 1 dB, and the variable length effect must be controlled by the interferences between the orderwire and the traffic signals. Therefore, we can neglect it here. We now choose the carrier frequency as 32 kHz because it gives us a sum above the desired 40 dB. We remember, however, that if there is trouble later with the telemetry interfering with the traffic, we can cut the carrier down to 28 kHz and still have a fairly conservative design.

Let us now get the interaction of these two signals with the traffic. This will set the minimum traffic rate. We must now assume a very important parameter: the 3 dB frequency of the high pass filter. We know from past iterations that if this frequency is not set rather high, there will not be a clean enough low frequency slot for any telemetry or orderwire. Setting this frequency high causes a very serious degradation of the traffic eye. Figure 2-5 shows the degradation of the eye pattern for dual high pass filters and a single low pass filter. The low pass filter, which represents the cable plus equalizer, is assumed to have a 3 dB frequency of twice the bit rate. If this is changed to $\sqrt{2}$ times the bit rate, it makes very little difference.

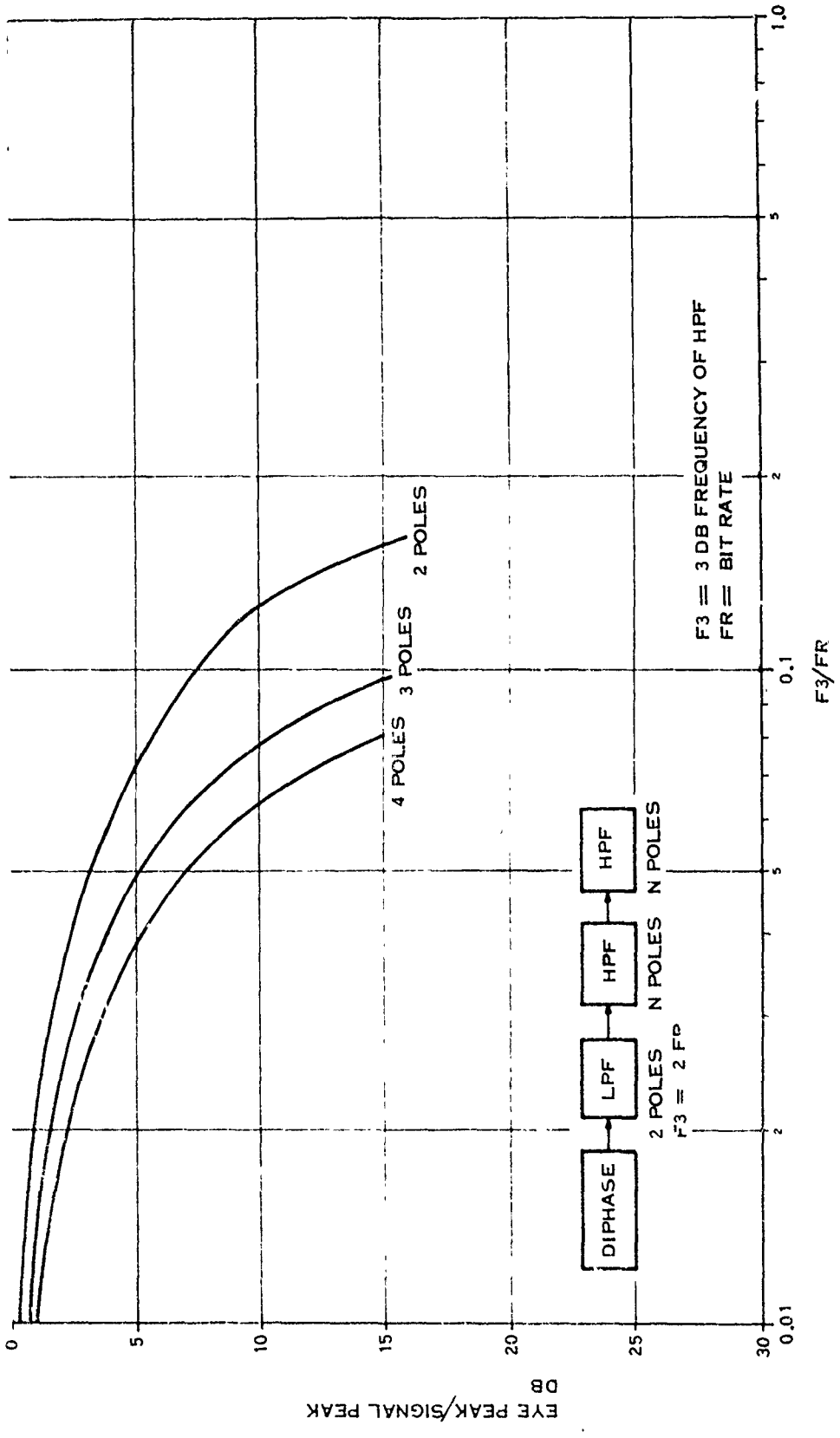


Figure 2-5. Eye Degradation for the High Pass Filters

A three pole high pass filter is chosen, and three bandwidths are carried through the following calculations. The reason for this is the degradation is so serious that the ability of the regenerator to handle it is crucial. This ability will be known later. Let us carry three filter values: 5 percent, 7-1/2 percent, and 10 percent of the bit rate. This gives us degradations of 5, 9-1/2, and 15-1/2 dB, respectively. Translated into the signal-to-noise allowance for one interfering source, this means that the traffic requires the following signal-to-noise ratios:

3 dB Frequency (% of Bit Rate)	S/N in Traffic	Sum of Atten (dB)
5	14	24
7-1/2	18-1/2	28-1/2
10	24-1/2	34-1/2

10 dB is added to get the sum of attenuations. This is the minimum allowed in either the orderwire or telemetry. We would like to add in another 10 dB, but this is the crucial case, and we may not have it to spare.

From previous iterations, it is known that the interference between the traffic and the telemetry is not the limiting case. Therefore, we will merely give the results here.

Traffic (kb/s)	Sum of Attenuations, Tlm. to Traff. + Traff. to Tlm.		
	5% Filter	7-1/2% Filter	10% Filter
256	35	35	39
288	37	38	43.5
512	51	60	72
576	55.5	62.5	80.5
1024	84	106.5	120
1152	93	114.5	128

This shows that the telemetry will permit operation down to 256 kb/s, even if the telemetry carrier is at 32 kHz.

Now let us look at the orderwire to traffic interactions. Figure 2-6 shows the interference from the telemetry into the traffic. The frequencies are normalized to the orderwire bit rate. We have already chosen a three pole filter. We obtain the following results:

Traffic (kb/s)	Attenuation (5% Filter)	Attenuation (7-1/2% Filter)	Attenuation (10% Filter)
256	-1	4	7
288	0	5	9
512	7	13.5	18.5
576	9	15.5	20.5
1024	18.5	27	33.5
1152	20.5	29.5	36.5

Figure 2-7 shows the interference from the traffic to the orderwire. Three pole high pass filters are shown at 5 percent, 7-1/2 percent, and ten percent of the bit rate. All frequencies are normalized to the bit rate. The frequency variable on the abscissa is the 3 dB point of the low pass filter, which appears to vary because of this normalization. We obtain the following results:

Traffic (kb/s)	Attenuation (5% Filter)	Attenuation (7-1/2% Filter)	Attenuation (10% Filter)
256	7.5	16.5	25.5
288	10.5	19.5	28.5
512	24.5	33.5	42.5
576	27.5	36.5	45.5
1024	42	51	60
1152	45	54	63

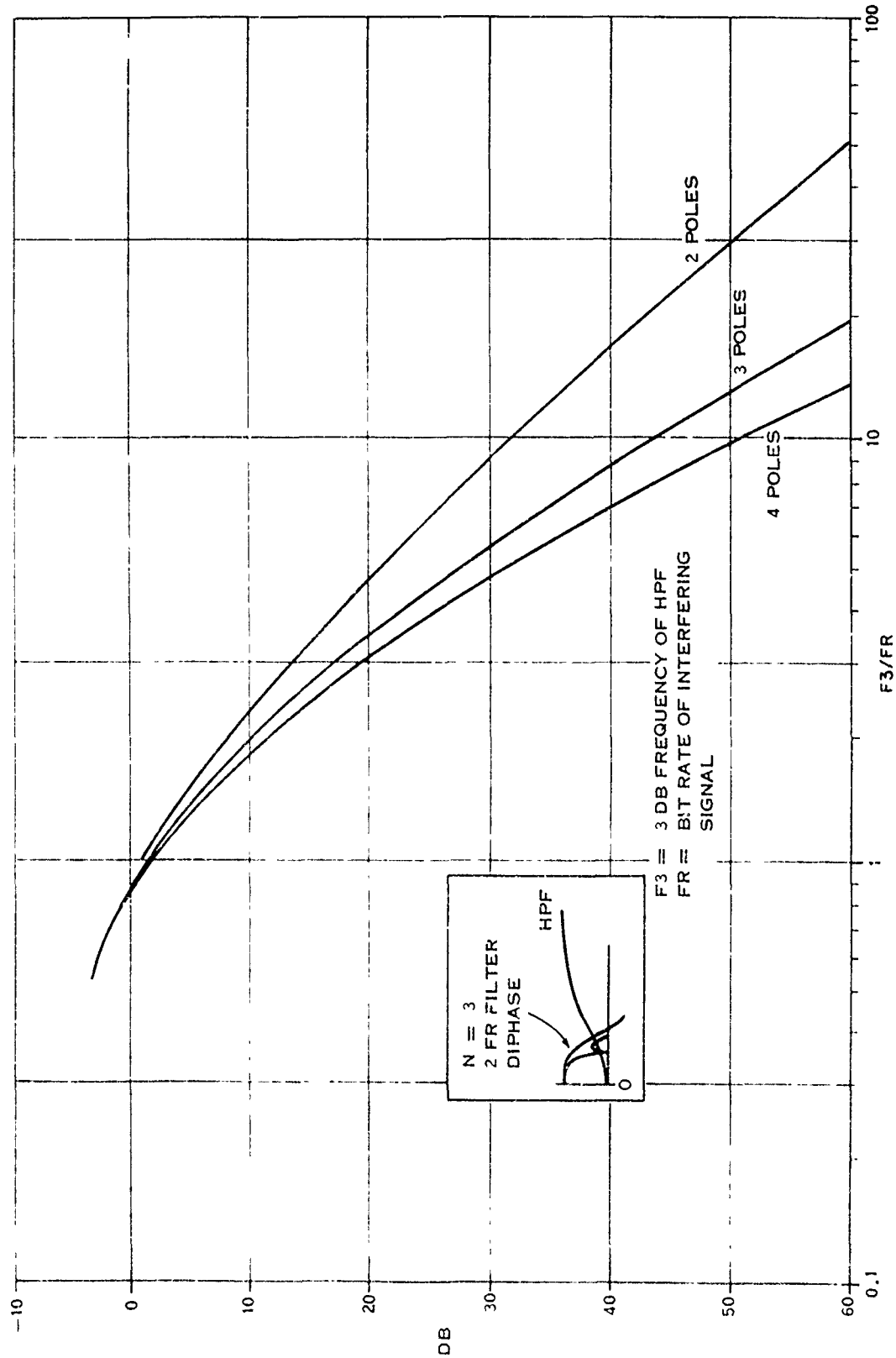


Figure 2-6. Interference Attenuation Through High-Pass Filter

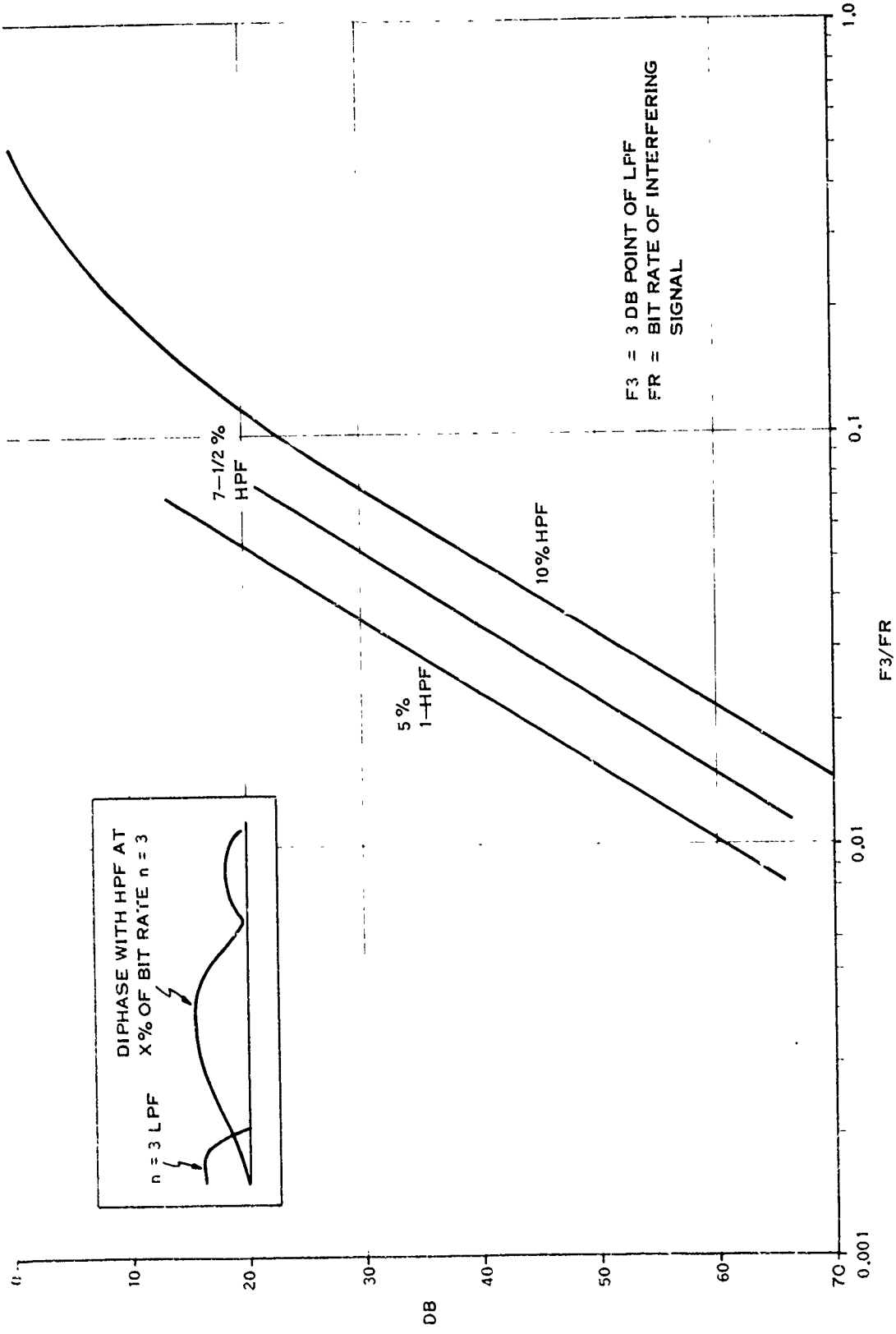


Figure 2-7. Interference Attenuation Through Low-Pass Filter

Now we can get our sums of attenuation:

Traffic (kb/s)	Sum (5% Filter)	Sum (7-1/2% Filter)	Sum (10% Filter)
256	6.5	20.5	32.5
288	10.5	24.5	37.5
512	31.5	47	61
576	36.5	52	66
1024	60.5	78	93.5
1152	65.5	83.5	99.5
Min required	24	28.5	34.5
Min traffic rate	512	512	288

A minimum traffic rate of 512 kb/s seems achievable. Operation at 288 kb/s looks possible on paper, but the regenerator that will work with the ten percent filter has yet to be demonstrated. Even 7-1/2 percent is a risky design.

2.1.3.2 TDM Calculations

In the TDM approach, two modes of operation are provided. In the first, Mode A, the line rate is increased to accommodate the VINSON and 2 kb/s telemetry. The lower rates are built up to provide a well cleaned up band at the bottom for the PARKHILL or maintenance orderwires. In the second, Mode B, the line rate is equal to the traffic rate. This is shown in the following table:

	Line Rate (kb/s)	
Traffic Rate (kb/s)	Mode A	Mode B
72	640	72
128	576	128
144	640	144
256	576	256
288	640	288
512	576	511
576	640	576
1024	2304	1024
1152	2560	1152
1536	2304	1536
2048	2304	2048
2304	2560	2304
4096	4608	4096
4608	5120	4608

All the traffic rates from 72 to 576 kb/s in Mode A use either 576 or 640 kb/s on the line. These line rates are chosen to provide two mile operation while providing the maximum baseband for the analog orderwire. For use with RLGM and RMC, a maintenance orderwire can be provided in Mode B all the way down to 72 kb/s (see paragraph 2.6).

The interference calculation for the TDM scheme is based on the most difficult case: 72 kb/s in Mode B. At the option of the designer, all Mode B cases can use the same levels and filters. The performance of the traffic will be better at higher rates because the intersymbol interference will be reduced. The performance of the orderwire will be better at higher rates because the spectral density of the higher rate signals is less.

In Mode A, the same filters and levels can also be used for maintenance orderwire.

Let us now calculate the interference for the 72 kb/s Mode B case. Preliminary breadboarding has determined that the maximum high pass filtering that the regenerator can accept is a 5 percent filter; i.e., the 3 dB point is at 3600 cps.

The orderwire is an analog speech signal. It can be treated as having a Gaussian amplitude distribution on a long-term average, with an unknown risk of short-term deviations. Curves are available which give the long-term spectral distribution, but it is risky to rely on them here. Sibilants or whistling can violate this spectrum for many milliseconds. If we assume a flat spectrum, that should cover sibilants, but the system cannot be guaranteed safe from whistling.

To get the interference from the orderwire into the traffic, we integrate a flat spectrum passed through the 5 percent high pass filter up to 2800 cps. If the orderwire low pass filter reaches its specified attenuation at 2800 cps, the integrated value should not be exceeded by speech or sibilants. The integrated result is that the power in the traffic channel will be 14.8 dB below the total speech power. As a matter of interest, if a whistle is no higher than the test tone level and no higher than 2000 cps, the limit will not be exceeded.

The 2800 cps figure was selected to give an adequate filter transition. It has a very sharp band edge. The maintenance orderwire would probably originate from a fairly wideband orderwire console, and would have to be band limited in the GM. An elliptic filter having a rather steep band edge will be used for band limiting. This defines the maintenance orderwire bandwidth, as will be seen.

To get the interference from the traffic into the orderwire, we integrate the diphase spectrum components passing through the 5 percent high pass filter to 2800 cps. This gives an interference power 51.8 dB below the diphase rms value (or peak value, they are about equal).

It is intended that the modems operate at fixed transmit levels and have no adjustment of receive levels or equalization. We will see if the breadboard performance permits this kind of operation. The R units will then equalize two miles of cable to 144 kc, using a simple one pole, one zero equalizer. The GM will have to equalize two miles of cable to 640 kc because it must transmit up to this rate for two miles. The calculations have been done for both equalizations and the results are the same within 1/2 dB. Therefore, the only difference made by the wide equalization is the higher gain amplifier required.

The R units have the option of equalizing to 144 kc or 640 kc. If an R unit at 144 kc feeds a GM equalized for 640 kc, it will still work. We now need to get the loss variation with distance of the signals (see Figure 2-8). The orderwire loss is 5 1/2 dB per mile. The diphase loss is less straightforward. The loss of importance is the loss measured at the sampling point of the equalized eye. This loss is approximately equal to the loss of the variable cable and the fixed equalizer at the lower 3 dB point of the equalizer, 16 kc. The loss of the cable is 6 dB per mile, and the loss of the equalizer is 29 dB.

Refer to Figure 2-9. The traffic passes through a total loss of:

$$6M + 29 \text{ dB}$$

with M in miles. The orderwire encounters the following loss in getting into the traffic channel:

$$5.5M + 14.8 + 32 \text{ dB}$$

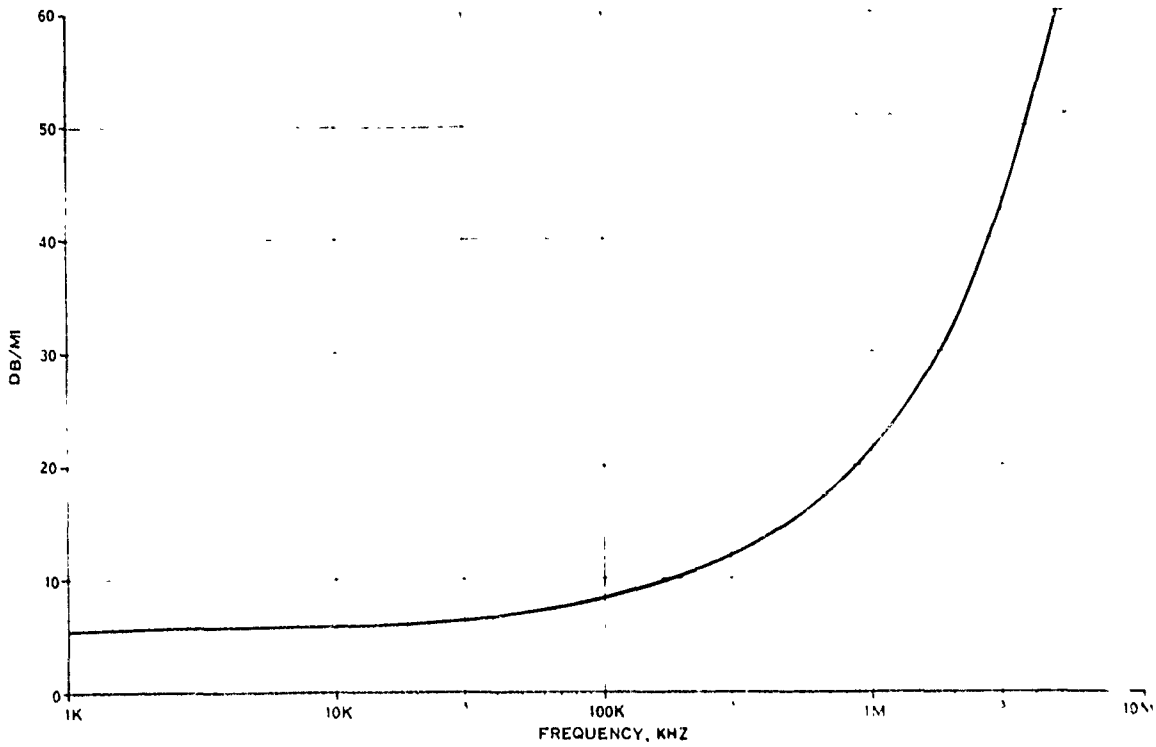


Figure 2-8. Attenuation of CX-11230 Cable Between 62Ω Impedances

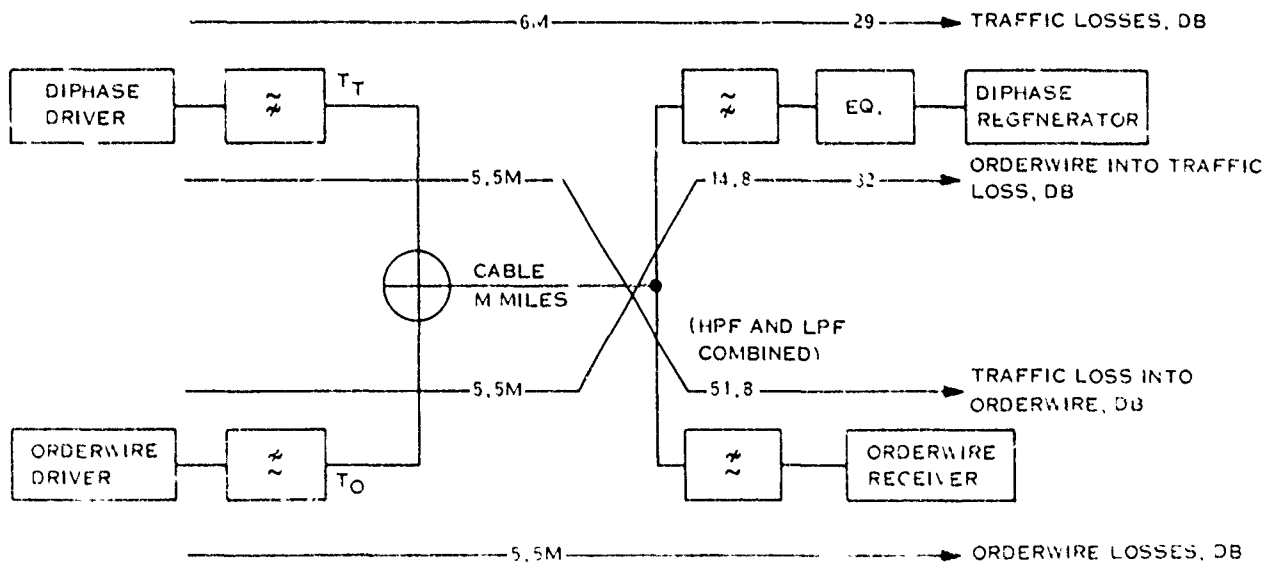


Figure 2-9. Signal and Interference Paths FDM Approach

Designating the traffic transmit level in dBm as T_t and the orderwire transmit level in dBm as T_o, the signal to noise ratio in the traffic channel peak to rms is:

$$T_t - T_o + 17.8 - 0.5M$$

Setting this to 25.5 dB, we obtain the maximum allowable orderwire level:

$$T_t - T_o = 7.7 + 0.5M$$

The highest orderwire level is set by the two mile case and is 8.7 dB below the traffic.

The loss experienced by the orderwire is in its own channel is just:

$$5.5M$$

When the traffic signal enters the orderwire channel, the only components that count are those at the orderwire frequencies. The loss at these frequencies is:

$$5.5M + 51.8 \text{ dB}$$

The signal to noise in the orderwire is then: (rms to rms basis)

$$T_o - T_t + 51.8 \text{ dB}$$

Let us set the minimum orderwire signal to noise ratio at 20 dB. This gives a definitely audible interference signal, but a useful orderwire will result. The minimum orderwire signal level (test tone) is then 31.8 dB below the traffic.

The transmit traffic level is set equal to the signal out of the existing TTC-39 modems: 3V p-p into 62 ohms. This is 36.3 mW or + 15.6 dBm. The maximum orderwire level is then +6.9 dBm. Due to the unpredictable short term behavior of speech, we must make sure that this level is not exceeded. The minimum orderwire level for 20 dB S/N is -16.2 dBm.

It is desirable to make the maintenance orderwire in the GM passive. If the COU were the only unit interfacing with the RLGMCD and the GM, we would have freedom to set the orderwire level anywhere in the range -16.2 to +6.9 dBm. However, the CNCE must also interface here, and we might be stuck with a -4 dBm transmit level. For the moment, let us assume the losses in the GM filter and transformer to be 2 dB from input to line (and

from line to output). With a -4 dBm interface level, our assumption will give a -6 dBm line signal, and a 30.2 S/N. With two miles of cable, the received line signal will be -17 dBm and the received signal will be -19 dBm at the interface. This is low but useable in the CNCE. It is quite adequate for the COU which can work on a circuit loss of 30+ dB. The only problem is the signaling tone. The CNCE puts out a -14 $\pm$1 dBm signaling tone at a -4 dBm test tone level. Since this allows signaling to be as low as 11 dB below test tone, the minimum signaling received level is -30 dBm. The CNCE signaling sensitivity is specified down to -29 dBm. If the losses were to be 4 dB each instead of 2, the received test tone would be -23 dBm, and the signaling level -34 dBm.

To get around this either:

a. The CNCE must provide increased sensitivity, or

b. A CNCE to CNCE connection must be prohibited and the COU must make up the difference by having higher transmit levels at its end of the system, or

c. The GM and RLGMCD must have amplifiers or

d. The CNCE must provide higher transmit levels

Let us now choose a filter design for planning purposes. The traffic high-pass filter is already chosen as being a 3-pole Butterworth filter having 3 dB frequency of 3600 cps. Figure 2-10 shows a constant input impedance filter in the transmit side. This would be a good idea for the driver, which may be non-linear. A non-linear driver working into a reactive impedance can give bad distortion, particularly unequal rise and fall times. Figure 2-11 shows the receive side. The relative positions of the filter and transformer are at the designer's option.

In order to get the best possible bandwidth, at moderate cost, choose a 4-pole elliptic filter for the orderwire. This provides a handy output inductor adjusted to reduce loading of the traffic. This inductor may have to be adjusted to reduce interaction between the filters. Since this filter need only provide 15 dB total attenuation in conjunction with the high pass filter, a stop band attenuation of only 25 dB is chosen. The frequency where it reaches this value

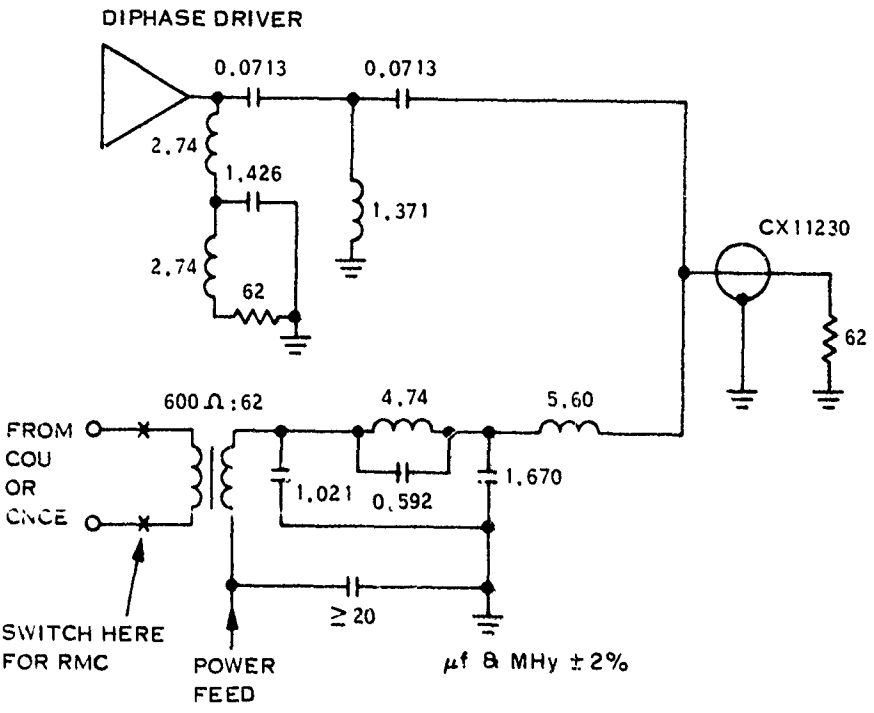


Figure 2-10. Transmit Circuits

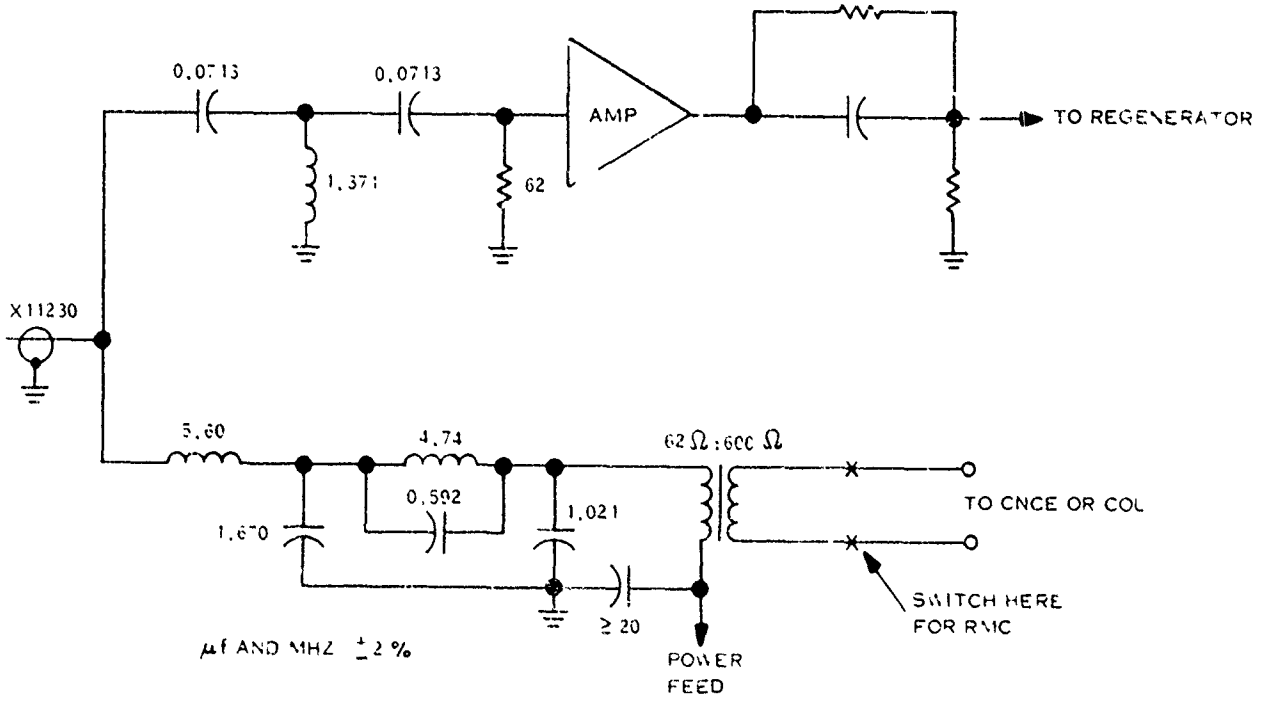


Figure 2-11. Receive Circuits

is set at 2800 cps. To get the maximum pass band, we will choose a filter with about 1/3 dB ripple. This means allowing a considerable reflection coefficient. It takes no more circuitry than a filter with less ripple, and a mismatch on the orderwire interface appears to be a low price for a wider pass band. Choosing a filter with a 25 percent reflection coefficient provides 0.25 dB ripple and a band edge of 2000 cps. The 25 percent reflection coefficient means that the impedance can vary from 0.6 to 1.667 times the nominal impedance. Figures 2-10 and 2-11 show this filter with a transformer on the interface side. The position of the transformer is a designer's option.

2.1.3.3 FDM Calculations With Revised Requirements

In order to make the FDM approach practical, the requirements have been revised, as mentioned in paragraph 2.1.2.d. This revision reduces the number of signals on the cable at one time to be reduced from 3 to 2. This improves the required interference levels by 6 dB as each signal encounters one interferer instead of 2. The 6 dB advantage permits operation down to 256 kb/s, whereas with 3 signals, operation could be provided only down to 512 kb/s.

To achieve the two-signal goal, the two digital signals, 16 kb/s VINSON and 2 kb/s telemetry are Time Division Multiplexed together. The resulting bit stream is 32 db/s, thus allowing for plenty of overhead for demultiplexing. When used, the maintenance orderwire occupies the same part of the spectrum previously occupied by the 32 kb/s signal.

Figure 2-12 shows a block diagram of a GM with this scheme. Note that there is no high pass filter in the traffic transmit circuit. In this case, the transmit high pass filter does not pull its weight. It causes degradation in the eye pattern in an amount more than the reduction in interference into the orderwire than it provides. Therefore, it can be eliminated. The optimum orderwire level rises as a consequence.

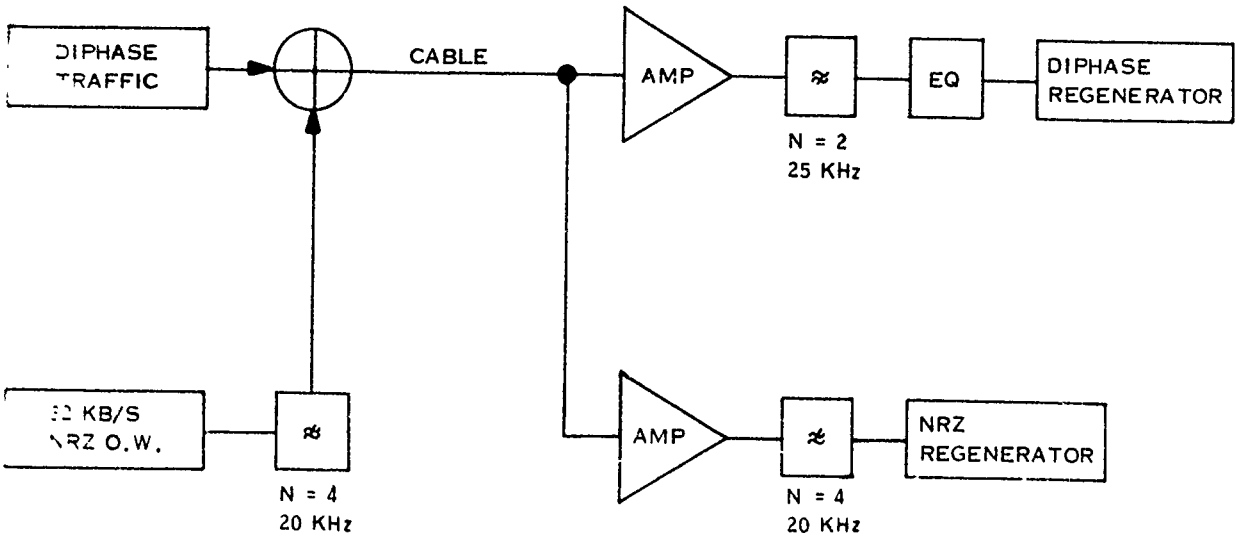


Figure 2-12. Group Modem with Revised Requirements

Figure 2-13 shows the computer calculated interference of the traffic into the orderwire. The only filter reducing this interference is the orderwire receive filter. The filter chosen is a 4-pole filter with a 3 dB point at 20 kHz. Thus $f_o/f_r = 20/256 = 0.078$, and the interference peak from Figure 2-13 is 24.7 dB below the traffic signal level.

Figure 2-14 shows the computer calculated interference of the orderwire into the traffic. The filters reducing this interference are the orderwire transmit low pass filter and the traffic receive high pass filter. The orderwire signal is a 32 kb/s NRZ signal to minimize the required bandwidth. The transmit low pass filter is the same as the receive low pass filter, i.e., a 4-pole filter at 20 kHz. The receive high pass filter is a 2-pole filter with a 3 dB point at 25 kHz. This is approximately a 10% filter, but the resultant eye pattern is good because there is only one such filter in the traffic signal path. Normalizing with respect to the orderwire rate of 32 kb/s: the high pass filter $f_3/f_r = 25/32 = 0.78$, and the low pass filter $f_3/f_r = 20/32 = 0.625$. The interference peak from Figure 2-14 is 7 dB below the orderwire signal level.

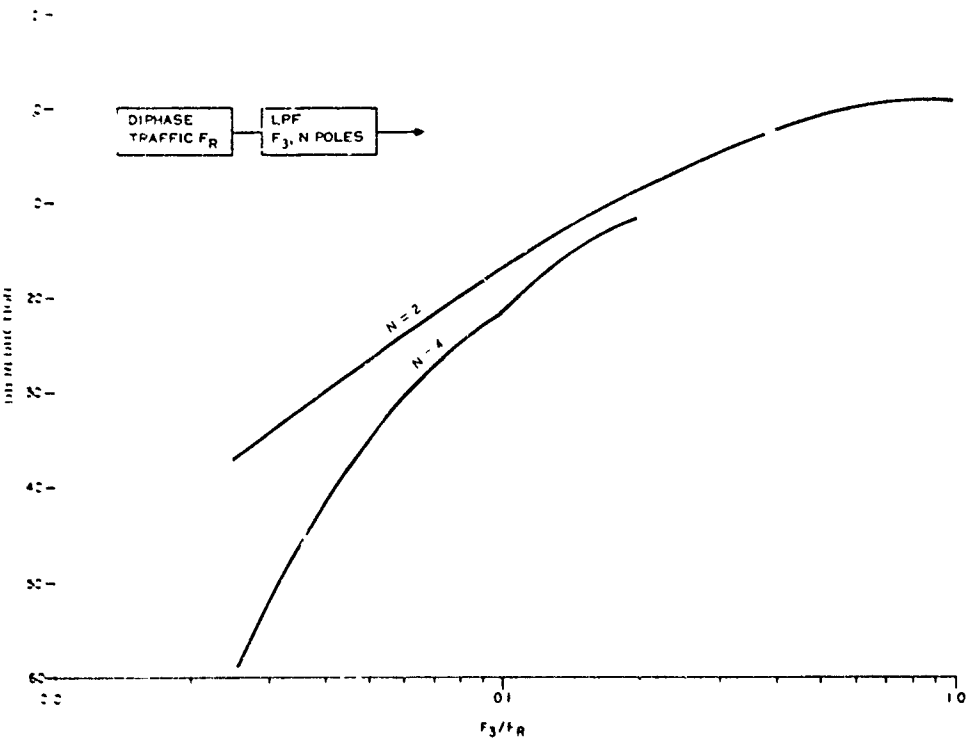


Figure 2-13. Interference Reduction through Low Pass Filter

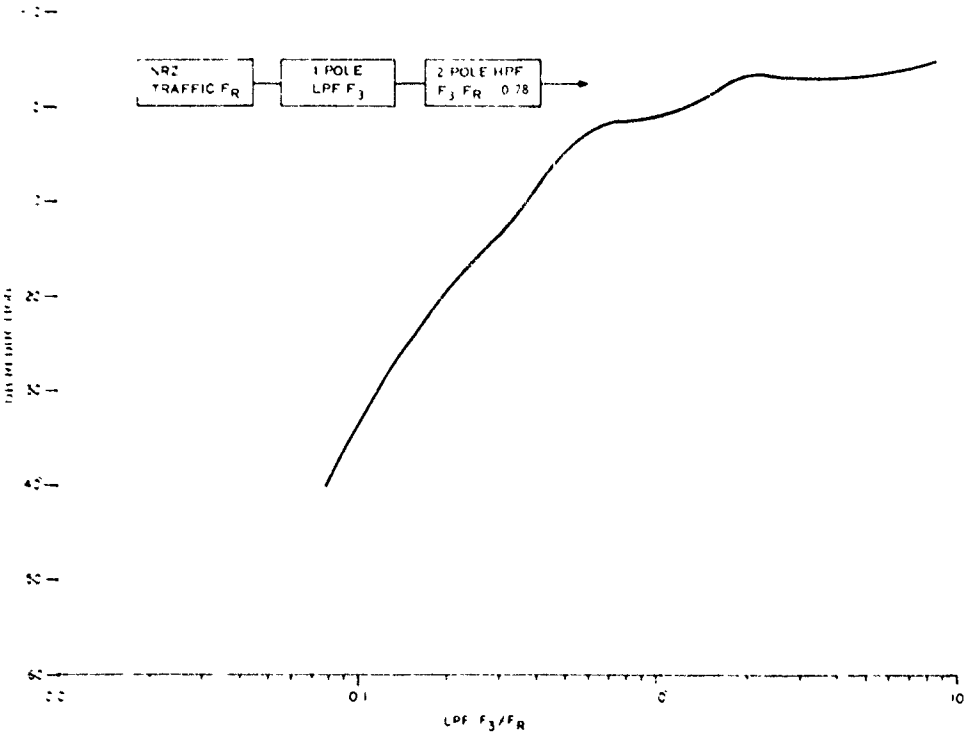


Figure 2-14. Interference Reduction through High and Low Pass Filters

Now let us calculate the required signal to noise ratios. Figure 2-15 shows the eye degradation caused by a single high pass filter. For the traffic, f_3/f_r = 25/256 = 0.098, and degradation is 3 dB. If we set the peak interference 3 dB below the eye peak, the required signal to noise ratio is 3 + 3 = 6 dB. To get the eye degradation of the orderwire signal we can use Figure 2-2. That was calculated for a diphase signal, but as far as the high pass filter effect is concerned, an NRZ signal at 32 kb/s is equivalent to a diphase signal at 16 kb/s. Therefore, we enter Figure 2-2 at an equivalent f_3/f_r = 20/16 = 1.25. The degradation for 4-pole filters is 2 dB. The required signal to noise ratio is then 3 + 2 = 5 dB.

If we have the freedom to set levels, we compare the sum of the attenuations required with the sum of the attenuations available. The sum of the attenuations required is 6 + 5 = 11 dB. The sum of the attenuations available is 24.7 + 7 = 31.7 dB. Therefore, this scheme is practical and there is almost 20 dB leeway in setting levels.

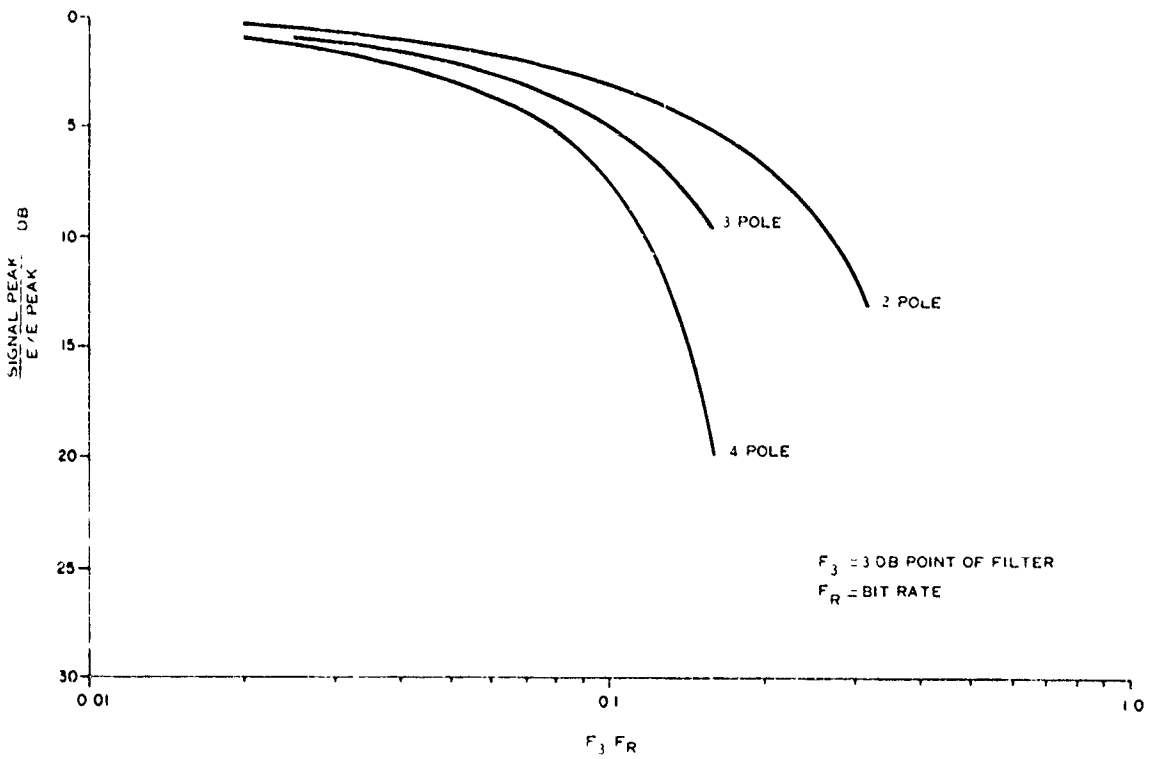


Figure 2-15. Degradation of Eye Size through One High Pass Filter, Diphase Signal

We now need the interference between the maintenance orderwire and the traffic. The maintenance orderwire must be provided down to 72 kb/s, and that is the limiting case. Again, we will assume no transmit high pass filter in the traffic. There will be a 10% receive high pass filter, i.e., at 7200 Hz. Calculations of the interference from the orderwire to the traffic were made assuming both a 2-pole and a 3-pole filter. The integration was carried up to 2800 Hz as was done in paragraph 2.1.3.2. The result is that for the 2-pole filter, the interference is 23 dB below the orderwire level, and for the 3-pole filter the interference is 32.7 dB below the orderwire level.

Calculations were made of the interference from the traffic to the orderwire. There is no high pass filter helping here. Again the integration was carried up to 2800 Hz. The result is that the interference is 40.1 dB below the traffic level.

For the speech signals, the S/N in the traffic is set to be 20 dB below the eye peak: 20 + 3 = 23 dB. The minimum S/N in the orderwire is set at 20 dB. Therefore the required sum of the attenuations provided is 63.1 dB for the 2-pole filter and 73.8 dB for the 3-pole filter. Therefore, either will work. The three pole filter will provide a better signal to noise ratio in the orderwire, but only if enough orderwire input is available to raise the orderwire level on the cable. If the GM is to have a passive orderwire which is limited by the CNCE level to -4 dBm, there is no particular advantage in the 3-pole filter. The levels were discussed in paragraph 2.1.3.2, and the same limitations apply here.

The low pass filter used in the maintenance orderwire must be a sharp one, as discussed in paragraph 2.1.3.2, because it must work with traffic down to 72 kb/s. However, there is another interesting case that should be explored: if there are two versions of the diphase GM, each one would be much simpler. This is a possibility for improved design that will be explored. In that case, there is another interference case that should be calculated: what if there were no sharp low pass filter for rates of 256 kb/s and above? It would save a lot of space on the modem. The design of the modem would then break into two versions, 72 to 144 kb/s with maintenance orderwire only, and 256 to 4608 kb/s with secure plus telemetry or maintenance orderwire.

To explore this possibility, we derive approximate integrals for the interference. For the orderwire into the traffic we have:

$$\frac{P_{tot}}{E^2} = \frac{1}{B}\int_0^B \frac{\left(\frac{f}{f_3}\right)^{2N}}{1+\left(\frac{f}{f_3}\right)^{2N}}\ df$$

Where P_{tot} is the interference power, E^2 is the orderwire power, B is the top frequency of the orderwire, f_3 is the 3 dB frequency of the high pass filter, and N is the number of poles in the high pass filter. If $B \ll f_3$, we have the approximation:

$$\frac{P_{tot}}{E^2} \approx \frac{1}{2N+1}\left(\frac{B}{f_3}\right)^{2N}$$

If we assume B = 4 kHz and f_3 = 25 kHz, the orderwire interference into the traffic is 38.8 dB below the orderwire level.

For the traffic into the orderwire we have:

$$\frac{P_{tot}}{E^2} = \int_0^B \frac{2}{f_r}\left(\frac{\sin^2\theta}{\theta}\right)^2 df \qquad \theta = \frac{\pi f}{2f_r}$$

Now E^2 is the traffic power, P_{tot} is again the interference power, B again the top frequency of the orderwire, and f_r is the information bit rate. If $B \ll f_r$, we have:

$$\frac{P_{tot}}{E^2} \approx \frac{\pi^2}{6}\left(\frac{B}{f_r}\right)^3$$

With B = 4 kHz and f_r = 256 kb/s, the traffic interference into the orderwire is 52 dB below the traffic level. The sum of the attenuations is a handsome 90.8 dB. Therefore, the two version concept of the diphase modem has much to recommend it on theoretical grounds. The actual merits of this scheme depend on the physical configuration and cost.

With the addition of a maintenance orderwire to the remote units, these considerations have been obsoleted. The diphase GM must be compatible with the remote unit maintenance orderwire, and this design is described in paragraph 2.6.

2.2 CDM ORDERWIRE

There are two versions of the CDM: High Speed and Low Speed. The two versions have the same orderwire requirements: a maintenance orderwire, a secure voice orderwire, and a 2 kb/s telemetry channel. These units act as cable terminals for repeatered cable systems. To simplify the repeaters, the line rates of the CDM's are independent of the traffic carried. The spacing between repeaters is fixed, although the distance between a terminal and the first repeater is variable. The system length is varied by varying the number of repeaters.

2.2.1 DESIGN GOALS AND REQUIREMENTS

The Low Speed CDM handles traffic at rates from 72 to 2048 kb/s. The High Speed CDM handles traffic at rates from 4096 to 18,720 kb/s. Other significant quantities are:

Version	Line Rate (kb/s)	Repeater Spacing (mi.)	Maximum System Length (mi.)
High Speed	18,720	1/4	5
Low Speed	2,048	1	40

The maintenance orderwire is an analog voice channel having a bandwidth of at least 1700 cps. It should work with faulty repeaters in the system and be independent of cable power and any other signal on the cable. Access to this orderwire is available at the CDM and each repeater.

The secure orderwire is the VINSON at 16 kb/s.

2.2.2 DESIGN APPROACH

The Low Speed CDM required more design effort because the orderwire requirements are the same for both systems while the lower traffic rate gives the more difficult problems in combining and decombining, and the system is the longer, thus giving more loss and tandeming problems. After the Low Speed system was determined, then the High Speed system was made similar for the purposes of commonality.

The specification called for the line rate to be equal to the highest traffic rate handled. This implied that Frequency Division Multiplexing be used to get all the signals on the same cable. Therefore, the first approach was to design an FDM system.

In an FDM system, the combined line signal must be split at each repeater. This is because:

a. The traffic must be regenerated at each repeater.

b. The maintenance orderwire must go through each repeater on a passive basis.

c. The loss in the long cable system is so great that the secure orderwire and telemetry must be amplified in each repeater, while the maintenance orderwire must use loading coils.

This presents a serious problem: the filtering effects on the orderwire and telemetry signals are compounded 80 times in a 40 mile system. This is the effect that limits the system length. In an effort to eliminate the length limitation, two alternatives are considered:

a. Time Division Multiplexing - This would put the 16 kb/s VINSON and the 2 kb/s telemetry in with the traffic bit stream. This raises the line rate slightly. The line rate is then not as specified, but this affects the Pulse Repeater and the CDM only. The traffic and orderwire signals would enter and leave the cable terminals in exactly the same manner as the FDM system, so no compatibility problems with other equipments are created. This alternative was pursued in the equipment design Sections 11 and 12.

b. Space Division Multiplexing - Putting the orderwire signals on another cable or field wire is not so easy here. The 40 mile length would require orderwire repeaters at intervals. This alternative was not pursued.

2.2.3 DETAILED DESIGN DESCRIPTION

In this section, we will determine the characteristics of an FDM system designed to go 40 miles. Since the computer calculations show this to be impossible, a second iteration of the system is given. Then the characteristics of the alternative TDM system are discussed.

2.2.3.1 FDM Calculations

Again, the system design is an iterative process. We assume some parameters, calculate the others, and see if the original assumptions give a workable system. If not, the original assumptions are changed, and the calculations repeated. The calculations given here have already been through several iterations.

Figure 2-16 shows a block diagram of the signal paths in the CDM and the PR. The maintenance orderwire passes through low pass filters and loading coils. The traffic passes through two high pass filters before regeneration. The telemetry and secure orderwire signals are put on carriers and passed through individual bandpass filters in the CDM. At each PR, the two carriers pass through the same bandpass filter, with one filter at the input and another at the output. The cable plus equalizer acts as a low pass filter for the traffic.

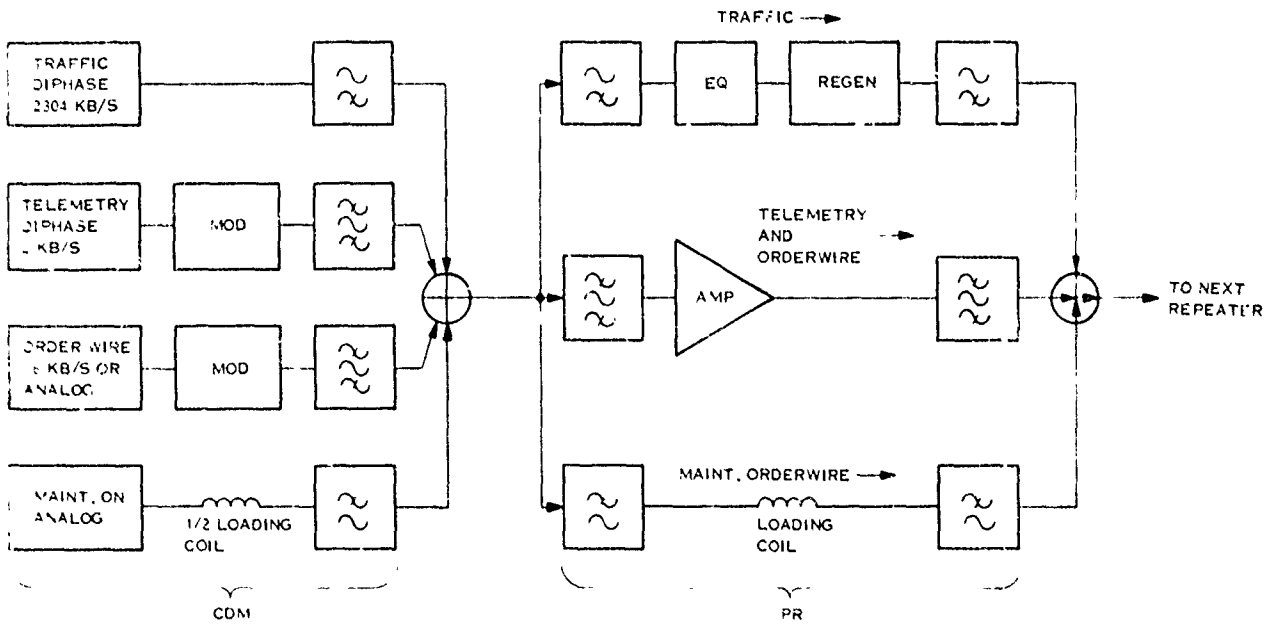


Figure 2-16. Signal Paths in the CDM and PR FDM Approach

Let us assume the bandwidths of the individual bandpass filters, and get from that the eye degradation of the digital secure orderw and the telemetry. These filters are assumed to have 3 dB points at $2\sqrt{2}$ times the bit rates, or 45.25 and 5.65 kHz, respectively. Figure 2-2 shows the size of the eye pattern for low pass filters, and this can be used for the equivalent bandpass filters. At the bandwidths chosen, the degradation with respect to the peak signal is about 1 dB for either three or four pole filters.

The minimum value of signal to interference ratio for these signals is 10 dB, just like the case of the GM in paragraph 2.1.3. Again, a more desirable figure would be 20 dB.

Let us now set the spacing between the telemetry and orderwire carriers and the number of poles in their bandpass filters. From previous iterations, it is known that this is determined primarily by their mutual interference and is almost independent of their interferences with the traffic and maintenance signals.

Figure 2-3 shows the interference from the orderwire to the telemetry. The computer program used to provide the data for this curve treats a base-band signal as if it were a carrier signal. Therefore, the figure can be used for two carrier signals at any frequency including dc. The only thing that matters is the separation between carriers. All frequencies are normalized to the bit rate of the orderwire. We obtain the following results:

Separation (kHz)	Attenuation (dB) 3 Pole	4 Pole
24	15	15
28	27	32
32	37	40
40	32	32
48	33	33

The four pole filter is not much better than the three pole, so we choose the three pole. 32 kHz spacing puts the telemetry in the spectral null of the 16 kb/s orderwire signal, so it is better than higher or lower frequencies.

Figure 2-4 can be used for the interference from the telemetry to the orderwire for the same reasons used for Figure 2-3. All frequencies are normalized to the bit rate of the telemetry. We obtain the following results:

Separation (kHz)	Attenuation (dB) 3 Pole	4 Pole
24	5	3
28	5.5	8
32	8	15
40	14	31.5
48	20	34

The four pole filter is noticeably better, and is therefore chosen. Again, since we have the option of setting the relative levels, we add the attenuation from the orderwire to the telemetry to the attenuation from the telemetry to the orderwire:

Separation (kHz)	Sum of Attenuations (dB)
24	18
28	35
32	52
40	63.5
48	67

The sum should be at least 20 dB, and 40 dB is desirable. 32 kHz spacing meets 40 dB and 24 kHz meets neither level. The spectral null is what makes 32 kHz so good. 28 kHz meets the minimum but not the desirable level. For this iteration we choose 32 kHz, although if it becomes crucial further on, 28 kHz can be used.

It is now necessary to consider the interactions of the carrier signals and bandpass filters with the maintenance orderwire at the low end and the traffic at the high end. After a number of iterations it was found that there were two major limitations on the system length: the degradation of the carrier eye patterns caused by the tandem bandpass filters and the increase in

maintenance orderwire loss caused by the loading effects of the tandem bandpass filters. The orderwire loss at 1600 cps was 6 dB per mile if the bandpass filter was designed at 62 ohms, but dropped to 1.8 dB per mile if the filter was designed at 250 ohms. Increasing this impedance further causes the high pass filter to distort the bandpass filter to the point that the orderwire eye pattern closed. A 72 dB loss orderwire may be designed, but it is a risky thing to put in the field.

At the high end a filter set was designed to minimize the carrier eye pattern degradation at the expense of degrading the traffic eye pattern. The purpose was to determine the upper bounds on system length. The upper 3 dB point of the bandpass filter was set at 100 kHz, and the 3 dB point of the high pass filter was set at 200 kHz. The high pass filter then becomes a ten percent filter, and, as stated in Section 2.1.3, a ten percent filter is probably beyond the capabilities of a practical regenerator. Even with this filter the computer run of the tandem filter eye patterns showed that phase distortion on the carriers closed the eye after only one filter.

The computer was then instructed to ignore the phase function. This is the equivalent of perfect phase equalization. The resultant eye patterns are given here first in terms of the number of filters (two per mile), and as a function of VINSON carrier frequency at 16 filters (eight miles). The VINSON suffers the most. Figure 2-17 shows the eye degradation as a function of number of repeaters. A 70 percent degradation should be set as the limit, because perfect equalization cannot be achieved in finite circuitry. It is estimated that practical equalization would cut the eye size to 25 percent, a rather poor figure. It is important to note that there is not enough room in the repeaters for phase equalizers. It must be done in the CDM, and therefore must be varied for system length. Figure 2-13 assumes a 48 kHz carrier for the VINSON. Is the situation better if this is lowered? Consider Figure 2-18. Practically no benefit is gained. This is because phase distortion due to band edge amplitude distortion extends quite far toward the band center. Another degradation is shown in Figure 2-19. Here it is shown that 100 percent modulation causes additional degradation of the eye pattern. Figure 2-12 can be applied to the VINSON at 12 miles or the telemetry at 32 miles. The reason

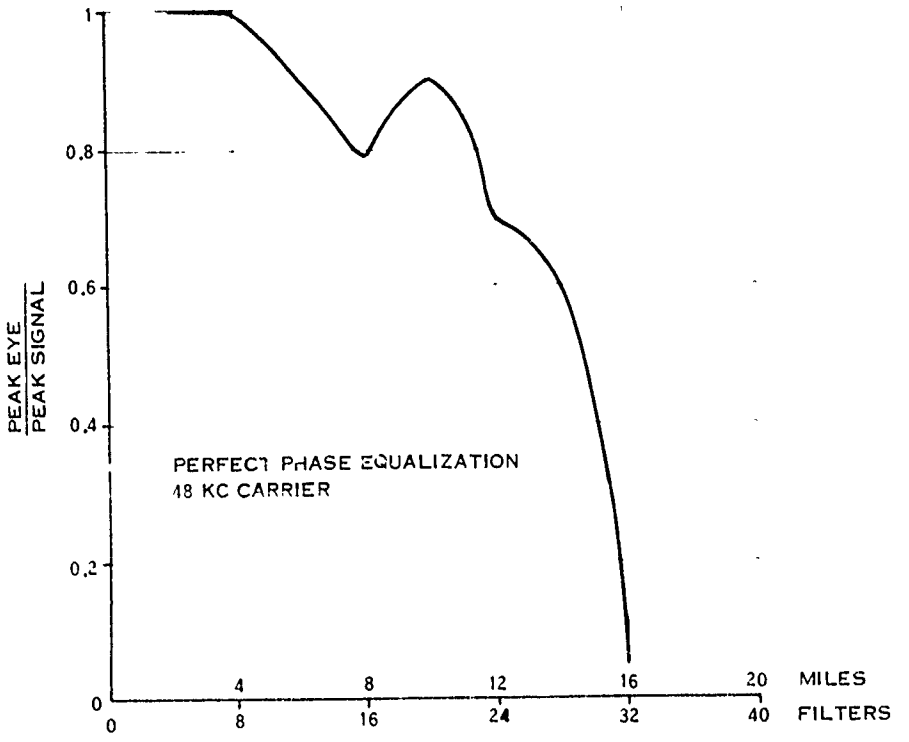


Figure 2-17. Eye Degradation of 16 kb/s Diphase vs System Length

for this degradation is that the amplitude characteristic of the compounded filters suppresses the information sideband nearest the band edge while enhancing that nearest the band center. This gives the effect similar to that of a vestigial sideband system. Vestigial sideband systems have the characteristics that the frequency response is a function of modulation depth.

The result of this iteration is that an FDM system cannot go the full distance. It would appear from the computer runs that a 12 mile system would work, but when actual equipment is built it is more likely that the length would be no more than five miles. What can the next iteration consider? Two possibilities are:

a. A system designed to go five to eight miles using FDM.

b. A TDM system designed to go 40 miles.

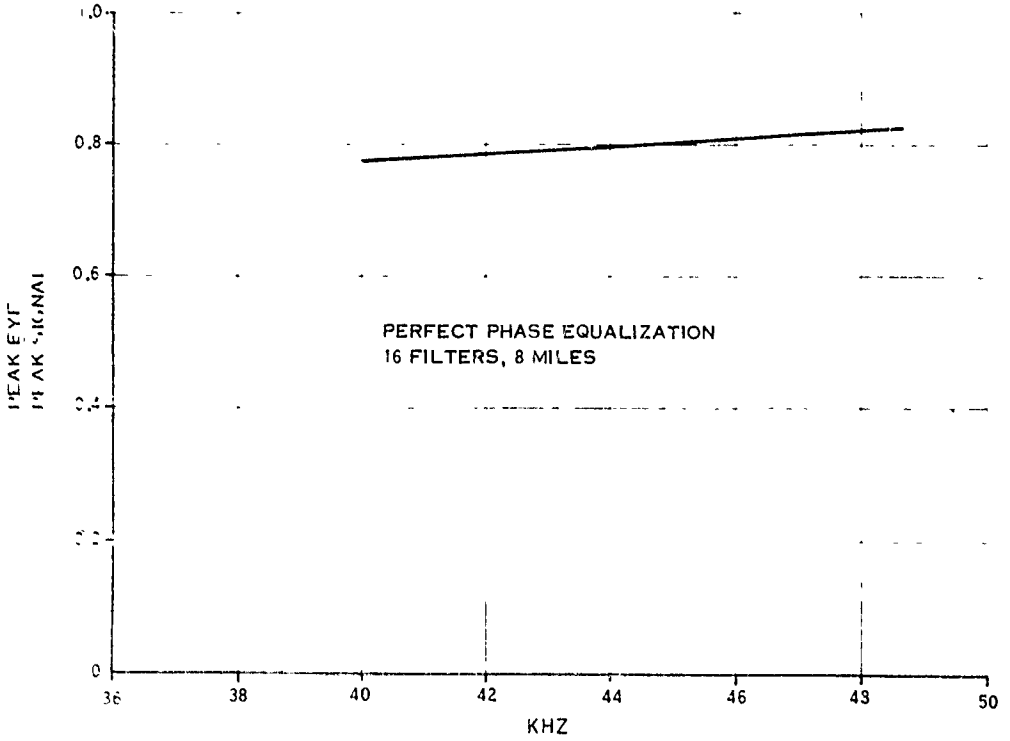


Figure 2-18. Eye Degradation of 16 kb/s Diphase vs Carrier Frequency

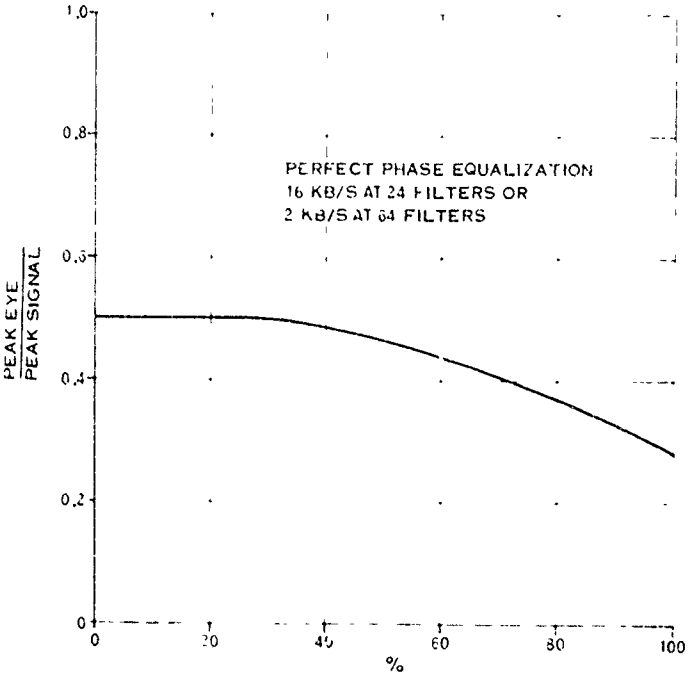


Figure 2-19. Eye Degradation vs Percent Modulation

2.2.3.2 TDM System

The TDM system was the one with the least risk. The worst problem was to get a simple regenerator to extract stable timing in the presence of high pass filtering.

In choosing the TDM system, we raised the line rate. The line rate for the low speed system became 2304 mb/s, to choose a rate in the TRI-TAC spec. This affects only the CDM, PR, and COU, all of which are units in this contract. The other elements in the TRI-TAC family are presented with separated traffic (at the traffic rate), secure orderwire, maintenance orderwire, and telemetry in the identical manner to that of an FDM system.

In a TDM system, the VINSON and telemetry are multiplexed into the traffic. The VINSON uses an external buffer to accommodate its asynchronous clock.

Let us calculate the interferences between the two signals on the cable: the digital signal and the maintenance orderwire. From previous iterations of this calculation, it is known that the interferences are very low, simple approximations are capable of giving useful results, and a great amount of freedom is available to the designer to change the various levels and filters without noticeable effect on system performance.

First we choose the traffic high pass filter. It is assumed as a 3-pole Butterworth filter at 30 kHz. For the low speed line rate of 2304 kb/s, this is a 1.3 percent filter. The eye degradation is about 1 dB. There is only one interfering signal on the line, and it is an analog signal. We will, therefore, require a 20 dB eye peak to interference rms ratio, or 21 dB signal peak to rms interference ratio.

The orderwire signal will receive a contribution of traffic interference from each repeater. They will almost be in phase, so let us assume that they are completely in phase. Therefore, if we want a 20 dB s/n (rms to rms) in the orderwire at the end of 40 repeaters, we need 20 + 32 = 52 dB per repeater.

To calculate the interference from the orderwire to the traffic, we assume that the orderwire can be represented by a sinewave at full test tone level at 1700 cps. This is conservative. With the assumed high pass filter, the attenuation is 74.8 dB.

To calculate the interference from the traffic to the orderwire, we will approximate the spectrum and integrate.

$$\frac{P}{E^2} = \int_0^{f_H} \frac{2}{f_r} \left(\frac{\sin^2 \theta}{\theta} \right)^2 A(f)df \qquad \theta = \frac{\pi f}{2f_r}$$

P = Interference Power

E = Peak Diphase Voltage

f_r = Bit Rate

f_H = Top Orderwire Frequency

$A(f)$ = Power Attenuation of HPF $\approx \left(\frac{f}{f_o} \right)^{2N}$

f_o = 3 dB point of HPF

N = Number of poles in HPF

For a 3-pole filter, the approximate value of the integral is:

$$\frac{P}{E^2} \approx \frac{\pi^2}{18} \frac{f_H^9}{f_r^3 f_o^6}$$

Putting in 1.8 kHz for the top orderwire frequency, 2304 kb/s for the bit rate, and 30 kHz for the filter corner frequency we get an interference power 169.1 dB below the diphase power.

With attenuations such as these, the levels of the diphase and the orderwire can be set to optimize the repeater power, CCU design, etc. As a matter of interest, the maximum allowable orderwire power works out to be 3 kW.

2.2.3.3 Digitization of the PARKHILL

An investigation of digitization of the PARKHILL was made. The alternative of providing a PARKHILL on a separate carrier similar to that of the FDM approach was considered. However, the complex separation filters and AGC amplifiers would still be required in the repeaters for this signal alone. It was estimated that the PR would weigh 11 pounds using this approach. If the PARKHILL is digitized, the amplifiers and filters would be eliminated. This saves so much circuit board space, and as a consequence, so much case size, that the resultant repeater would save at least 2 pounds.

Of course, the digitization circuitry would have to be provided in the CDM. However, the CDM is estimated to meet its weight spec with enough to spare for an additional circuit board. Furthermore, the volume and power is also available. Therefore, digitization of the PARKHILL offers a very attractive weight radeoff.

It introduces one risk, which will be dealt with. The PARKHILL specification mentions no limit for quantization distortion. Quantization distortion sounds like noise, but it is not noise, because it depends on signal level. It is a form of non-harmonic distortion. The safest way to determine the effect of this distortion on the PARKHILL is by experiment. Since the PARKHILL is not at present available for experimentation, a temporary solution is adopted. This is to plan for an A/D converter well in excess of what might be required. There is enough bit rate in the format for an allocation of 96 kb/s for the PARKHILL. This can provide an 8 kc sampling rate and 12 bit encoding. 12 bit A/D encoders are available in military versions, and there is plenty of room on a circuit board for a coder, decoder, smoothing filter, and all necessary audio circuitry.

A 12 bit A/D conversion provides a step size 1/4096 times the peak to peak signal. The rms quantization noise is then lower than 69.2 dB below rms signal. This is far more than could possibly be needed. The breadboard

system will be built with a 12-bit coder, and when the PARKHILL becomes available, a test will be made to see how many of these bits can be cut off. It would appear likely that an 8-bit coder would be more than adequate, and an 8-bit coder is considerably cheaper than a 12.

After this investigation was completed, the PARKHILL requirement was eliminated.

2.3 RLGM AND RMC ORDERWIRE

These units now have a requirement for a maintenance orderwire. Since they interconnect with the RLCMCD and diphase GM in the shelter, the latter units must also have a compatible orderwire. The maintenance orderwire must be passive within these units and not depend on traffic or unit operation to work. Furthermore, the bandwidth of this maintenance orderwire is specified to be that of the MIL-STD-188-100 voice channel, which is flat to within 4 dB up to 3000 Hz. An additional 4 dB attenuation is allowed up to 3400 Hz.

The calculations in paragraph 2.1.3.3 assumed that filtering could be provided which eliminates interference between the traffic and the orderwire. However, this required wider band makes it impossible to provide the necessary isolation. To provide the wider band, it is necessary to permit some degradation of both the traffic and the orderwire. A workable design is possible if the following degradations are permitted:

a. The minimum signal-to-noise objective of 20 dB in the orderwire need be provided only down to 144 kb/s. Given the triangular shape of the low frequency end of the diphase spectrum, this will give 11 dB S/N at 72 kb/s.

b. Speech on the maintenance orderwire will give occasional burst errors which may cause reframing of the multiplexers. Since this is a maintenance orderwire, the system normally operates without speech on the orderwire.

To provide this bandwidth, all filtering in the orderwire is removed. The interference from the orderwire into the traffic is then controlled by the spectral density of speech along with a 7200 Hz high pass filter in the traffic receiver.

This kind of control permits occasional speech bursts to affect the traffic, but it will not occur too often to prevent maintenance personnel from servicing the units. The interference from the traffic into the orderwire is then limited only by the frequency response of the orderwire phone and the human ear. This is represented by a C-message weighted meter.

If we use the approximations from paragraph 2.1.3.3, the interference from the orderwire to the traffic is:

$$\frac{P_{TOT}}{E^2} = \frac{1}{2x2+1}\left(\frac{3300}{7200}\right)^4 \longrightarrow 20.5 \text{ dB Down}$$

The interference from the traffic to the orderwire at 144 kb/s is:

$$\frac{P_{TOT}}{E^2} = \frac{\pi^2}{6}\left(\frac{3300}{14400}\right)^3 \longrightarrow 47 \text{ dB Down}$$

The orderwire levels are rms and the traffic levels are peak. The bandwidth of 3300 Hz is that of the C-message weighting filter. To get a minimum S/N of 20 dB in the orderwire with a traffic level of 3 volts (15.6 dBm), the minimum orderwire level is -11.4 dBm. Assuming the orderwire to have Gaussian amplitude distribution, the traffic S/N should be set to 23 dB for essentially error-free performance. Given these equalizers, filters, and cable losses, the maximum orderwire level is +15.1 dBm. We choose +5 dBm as the optimum. This gives 10 dB margin in each direction, at least on paper.

The next problem is how to mix the orderwire and traffic signal. Amplification of the orderwire is not permitted. The overlap of the bandwidths is too much for combining in a high pass/low pass filter set. The only option left is a resistive pad. Since the orderwire level chosen is higher than the standard -4 dBm, we would have to call upon the COU anyway. It has enough output capability to make up the resistive pad losses. Using bridging resistors of 600 ohms at both transmit and receive cable interfaces, the level into the unit from the COU calculates to be +21.3 dBm, and the output level into the COU calculates to be -21.9 dBm. Since the amplifiers in the COU are already capable of driving two directions of a 40 mi mile cable system simultaneously, this requirement is within the COU's capability. A 4-wire, full duplex interface at 600 ohms impedance level is added for this application.

The RLGM has one maintenance orderwire, and was designed to accept a cable from the COU directly. The RMC has two maintenance orderwires, one on the high group and one on the low group. They operate independently and either will accept a COU. The GM has the possibility of six maintenance orderwires and not enough connector space on the back for separate connectors. Furthermore, the back of the unit is not easily accessible. Therefore, a common connector must be cabled to an orderwire facility such as an orderwire control unit. The RLGMCD has enough room for two separate connectors, but the connectors are also on the back, so orderwire access must still be through the orderwire control unit.

Figure 2-20 shows the interface between the COU and any unit having this maintenance orderwire.

2.4 INTERUNIT TIMING

There are a number of general rules which cover timing signals between DGM units and other units in the system. There are also quite a few exceptions and special cases not covered by these rules. We will first state the general rules and then investigate the significant individual cases.

2.4.1 GROUP, SUPERGROUP, AND MASTERGROUP SIGNALS

These are all full duplex signals carrying data and related timing in both directions. The data is balanced NRZ and the timing is a balanced square wave having a frequency equal to the bit rate. They go in the same direction between units, as shown in Figure 4.3-13 of MIL-STD-188-100. The positive to negative timing transition is centered on the data bits.

2.4.2 DIPHASE SIGNALS

These are full duplex signals with data and timing contained in the same waveform. Conditioned diphase is used on the channel, group, supergroup, and mastergroup lines. The channel signals are carried balanced on WF-16 field wire, which may be extended inside shelters using RG-108. The group, supergroup, and mastergroup signals are carried unbalanced on CX-11230 cable.

2.4.3 STATION CLOCK SIGNALS

These are signals resembling the related timing signals in paragraph 2.4.1 above. However, they are not related to a data signal. Some units accept a station clock as an option and use it to time the transmit output data. When used, the arrangement is as shown in Figure 4.3-10 of MIL-STD-188-100, although

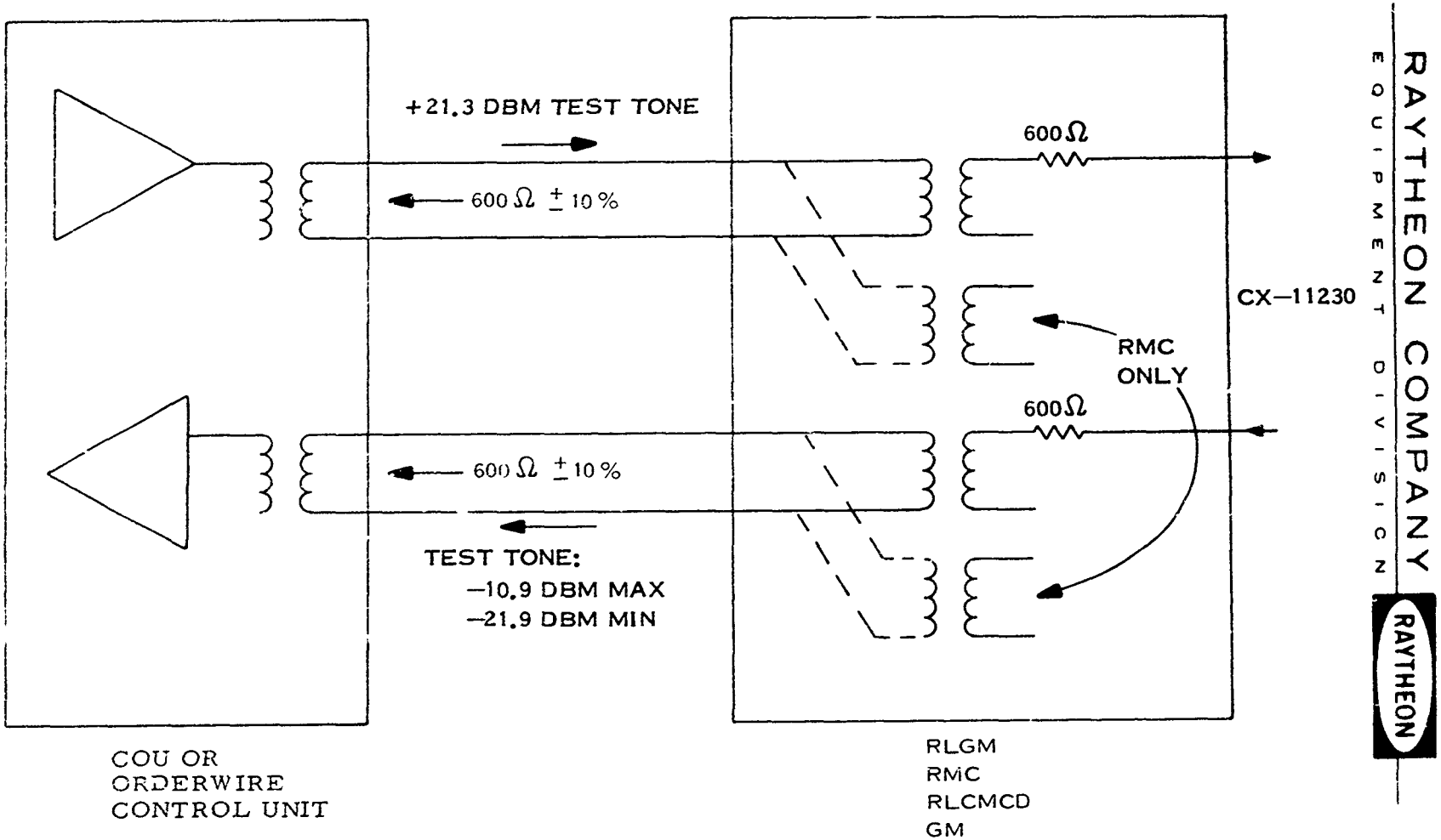


Figure 2 '0. Interface Drawing

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the station clock is not supplied to the sink. The sink must use either the related timing or a diphase data signal. In the DGM units, data comes into the source to be retimed. Paragraph 4.3.1.6.3 of MIL-STD-188-100 permits the phase relationship of this data to vary by $\pm$1-1/2 bits due to delays in the wiring. These variations are essentially static, and can be handled by autophase circuits. The station clock negative to positive transitions command data transitions. These data transitions are allowed to occur later by up to 12-1/2 percent of a bit.

2.4.4 TELEMETRY CHANNEL SIGNALS

These signals are 2 kb/s in most DGM units. The MGM is the exception, having 16 and 32 kb/s rates. All telemetry signals supplied to the DGM units are synchronous to the system clock, but there is no guaranteed phase relationship. The phase delays depend on wiring, and are static, so autophase circuits can solve this problem. Autophase circuits can be designed to work without a related timing input. This solves the problem of receiving telemetry from the KY-82 as mentioned in paragraph 3.2.1.3.3 of the TCCF spec. Therefore, no timing input to the telemetry channel will be provided. A related timing output will, however, be provided with the telemetry channel data output.

2.4.5 MODEM TIMING

The principle timing mode of the GM, RLGMCD, and the CDM is to use related timing for the transmit traffic. This timing is the only one guaranteed to be present at all locations. Related timing is a square wave at the traffic rate as mentioned in paragraph 2.4.1. The Diphase GM and CDM also have the capability of using timing recovered from the received cable signal.

This loop-back timing capability does not seem to be needed by the system. If the modems are at a node, the loop-back cannot be used because the incoming and outgoing timing are slightly different. If the modems are at a through traffic point, such as a radio to cable system interface, the loop-back timing again cannot be used because the radio system will cause the jitter in one direction to be different from that in the other direction.

Loop-back can only be used at the end of an extension facility, or at certain TGM locations, where sufficient buffering is available to take up the radio jitter. At these facilities, the loop-back must be in the multiplexer in order for the multiplexer to operate. If there is a TED present, the multiplexer loops back the RED clock. A loop-back of the BLACK station clock must also be made, and this is provided by the TED, using the BLACK station clock output of the modem. Thus, the internal timing loop-back in the modem is never needed.

The bipolar modem cannot use station clock, because the TD-976 has a free-running clock, and cannot be synchronized to a station clock. The dipulse modem might use a station clock, but it is better off using related clock.

The system orderwire on the diphase GM requires a station clock. The system orderwire receives signals from the VINSON buffer at 16 kb/s and the telemetry source at 2 kb/s. The telemetry source might be an LKG, which supplies no timing. Although the VINSON buffer in the CNCE supplies timing, the system orderwire must operate with either the 2 kb/s or the 16 kb/s alone as well as together. Therefore, a timing input cannot be counted on. Deriving the timing from the traffic, which varies from 72 to 4608 kb/s, requires too much circuitry for the GM. Therefore, a station clock, one per modem case, is required for the diphase GM system orderwire. The station clock is at the transmit combined orderwire rate of 32 kb/s.

2.4.6 MGM TIMING

The MGM is required to use station clock at the mastergroup rate, loop-back timing, or a free running internal oscillator. Again there is a problem with the TCCF. If it cannot provide the 9.36 or 18.72 MHz station clock, an alternate frequency is necessary. A 32 kHz station clock has been suggested. In the final version, the MGM is able to accept either a 16 or 32 kHz clock.

2.4.7 TGM TIMING

The TGM is required to use external station clock, loop-back timing, or one of the group inputs. The external station clock is to be supplied at the supergroup and group rates. However, it only needs station clock at the supergroup rate. Group rate station clocks will not be accepted. Related timing at the supergroup and group inputs will be available and are required. The group input to be used for the supergroup output will be group one, since it always has the highest group rate.

2.5 TELEMETRY

As a result of a recommendation by the TCCF contractor, the 150 b/s local telemetry has been removed from the DGM. Its function is replaced by a number of alarms and the use of the 2 kb/s telemetry channel in the RLGM, RMC, LGM and TGM. The new philosophy is as follows:

a. No 150 b/s telemetry.

b. The RLGM and RMC have a permanent internal loop-back of the 2 kb/s telemetry. The subchannel looped back is the one that the present specification designates for local telemetry. When the unit is in SA alarm, the telemetry subchannel is forced to "0".

c. The LGM/LM and TGM have an optional, switch-controlled, loop-back. In the "internal" switch position, the alarm state forces the looped subchannel to "0". In the "external" switch position, the alarm state forces the 2 kb data signal coming out of the demultiplexer at the connector to "0". In "external", the transmit subchannel transmits whatever is put into its input connector. A pull-up at this input will force the transmit subchannel to "1" if someone forgets to connect anything. The subchannel on which all this occurs is the one that the present specification designates for local telemetry. The shifting of other subchannels in the TGM goes on as before. The alarm that controls the subchannel is SA, not S.

d. The MGM, GM, RLGMCD and CDM do not have loop-back.

e. Some units have more than one alarm. The definitions of the alarms are:

"S" - This is the alarm originally called for in the specification. It is sometimes referred to as the BITE summary alarm. It goes into the alarm state if anything is wrong, e.g., loss of frame, loss of a channel, loss of power supply, loss of interunit signals and failures of the internal circuitry. (Note that includes input signals. Telemetry and VINSON inputs are excepted. Channel signals are monitored only when activity is expected.)

"LS" - This is an alarm that indicates a loss of incoming signal on the CX-11230 cable. Its meaning is that the fault is outside the shelter. It

assumes the normal state if power fails. It should be as little affected by failures within the unit as possible.

"SA" - This is an alarm that includes all the faults of S except out of frame. Furthermore, it is inhibited by LS on those units which have an LS alarm. It assumes the alarm state on loss of power, just like S. Note that it includes loss of input signals on the equipment side interface, just like S, but since SA is inhibited by LS, SA does not include input signals on the cable (CX-11230) side, if there is a cable side.

"FS" - This is an alarm that indicates that the MGM is out of frame. The assumption is that most causes of out of frame are outside of the shelter, mainly in the transmission. The assumption is at least partially true.

f. The RLGM and RMC generate S and SA alarms with external connections for both. See paragraph 2.4h for definition of S and SA.

g. The GM, RLGMCD and CDM have S, SA, and LS. The definitions above are straightforward for the CDM, but the other two units need some further qualifications. The GM and RLGMCD carry more than one group. The unit case has only one each S, LS, and SA. However, the inhibition of SA by LS should be done on an individual group basis. That is, if the letters without subscript refer to the unit alarms that come out of the box, and the letters with subcripts refer to the alarms sensed for an individual group:

$$LS = LS_1 + LS_2 + \ldots.$$

$$SA = SA_1 + SA_2 + \ldots.$$

$$SA_n = (\text{internal faults} + \text{equipment side input faults} + \text{power loss})\overline{LS}_n$$

$$S = S_1 + S_2 + \ldots.$$

In setting the input sensor point, there is another important issue. The orderwire signal may interact. The maintenance orderwire is not a problem. If there is a loss of traffic from the far end, and the sensor is right at the cable input, LS will be in the alarm state most of the time. Occasionally it will drop into the normal state when someone is talking, but most of the time the right answer will be presented. This assumes that no orderwire signaling scheme uses

tone-on-while-idle signaling. However, the system orderwire on the GM is on all the time. If we put this LS sensor right at the input, it will not respond to loss of traffic alone. If we put the LS sensor after orderwire separation, it will respond to an internal fault in the circuitry from the cable input to the separation point. The circuitry involved includes an amplifier. It has been decided to put the sensor at the input.

All three, S, SA, and LS provide external connection.

h. The LGM and TGM have S and SA. One difference between S and SA in these units is that loss of frame puts S in alarm and not SA. Further, the channel BITE on the LGM, RLGM and RMC should not produce an SA alarm. The problem here is that the channel BITE is only effective when the channel is active. Therefore, a fault in a channel will produce an intermittent alarm, and it is in the normal state most of the time. The channel BITE should produce an S alarm. S does not leave the shelter, and if an operator notices repeated alarms on S, he can call for the switch to make a loop test, keeping the test pattern on each loop long enough for him to locate the faulty channel. However, SA goes into a remote computer. It may cause considerable confusion here to have an alarm entered into the computer which alarm goes away before any action can be taken. Both S and SA provide external connection.

i. The MGM has S, SA and FS. The intentions are straightforward. The only confusion is the interaction between FS and the other alarms. Certainly a loss of mastergroup input would cause an out of frame. However, the MGM is designed so that loss of Supergroup input will suppress the FS Alarm. Some circuitry failures in the framing cards would cause an out of frame. All three, S, SA and FS provide external connection.

2.6 FRAMING COORDINATION

The framing procedure for the DGM matches that of the TTC-39. It is a cooperative procedure, and the handshaking must be the same for all units that interoperate. The individual units can have some latitude in implementation, and indeed there are many details that differ between processor controlled and hardwired equipments. However, they must all use the procedure of Figure 2-21.

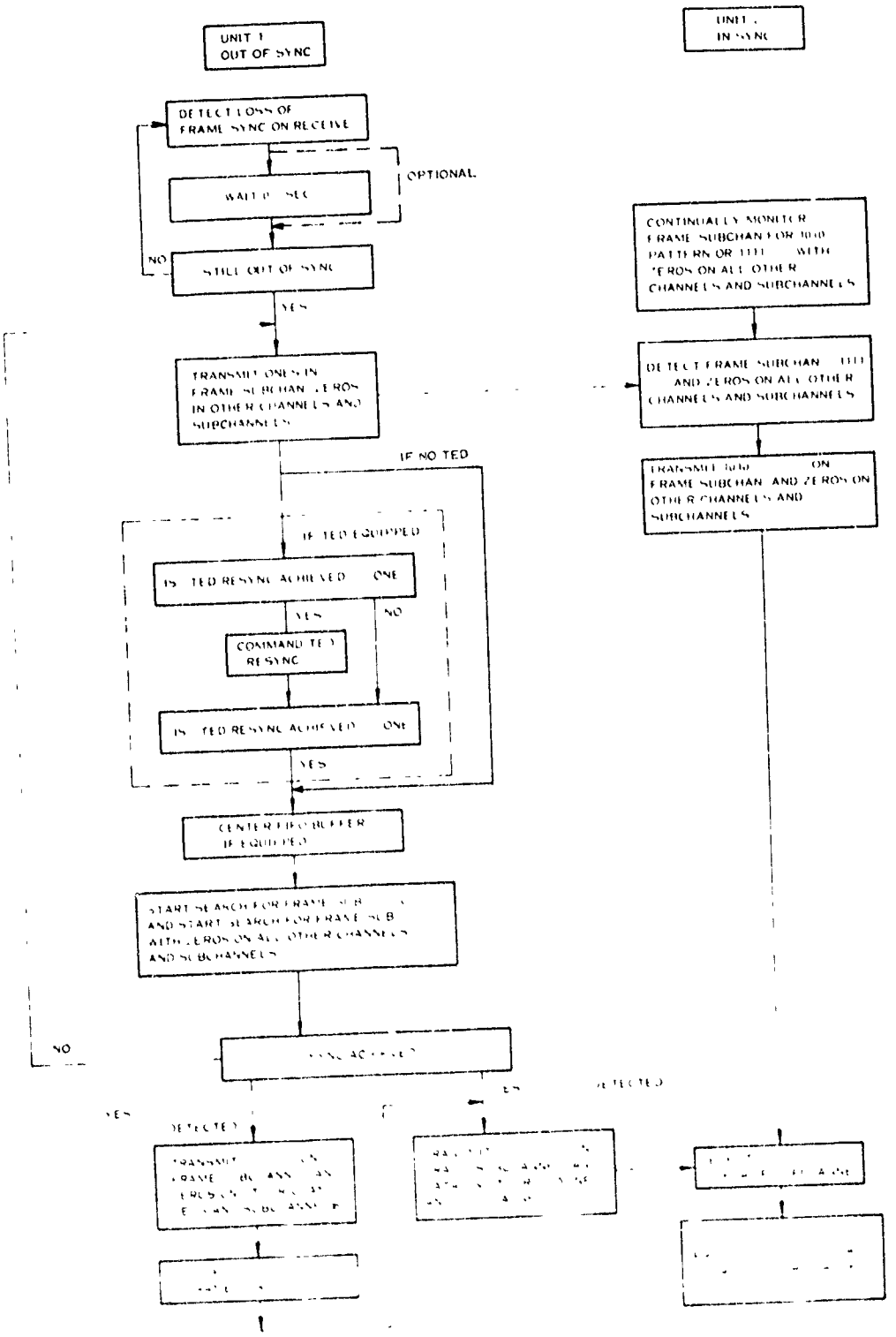


Figure 2-21. Synchronization Flow Diagram

In Figure 2-21, two units interoperate. In some cases, one unit would be the 39 switch and the other a member of the DGM family. In others, both could be members of the DGM family. One example of this is where an LGM connects to the group side of the TGM. The LGM and the group circuit of the TGM interoperate in this fashion. The supergroup of the TGM interoperates with the switch or TCCF independently of the group framing.

In the DGM family, only the LGM and the Group and Supergroup sides of the TGM use the TED option.

2.7 EQUIPMENT SIDE INTERFACES

After a number of interchanges between the various contractors and government agencies involved, an equipment side interface has been agreed upon. The termination is dictated by the TED driver.

In order to be compatible with the TED, the termination of the balanced signal interface must be 100 ohms center tapped to ground. Other signals may have a grounded or ungrounded center tap.

The revised balanced signal interface characteristics are:

a. Driver Output. Line-to-line voltage minimum as measured into 100 ohms shall be +100 mV for a digital "1", -100 mV for a digital "0". Polarity shall be measured on the pin with the later letter in the alphabet. The pin with the earlier letter in the alphabet shall be used as the reference. The differential voltage levels in this paragraph shall be valid for operation of the driver into a load whose center-tap is either grounded or ungrounded. The maximum voltage measured from either line to ground shall not exceed ± 3 volts.

b. Line-to-line voltage maximum measured directly into a 100 ohms termination shall be +4 volts.

c. Rise and Fall Times. For rise and fall times measured in a 100 ohm resistive dummy load at the driver output terminals, see Figure 2-22 and Table 2-1.

d. Clock/Data Phasing. When data and clock are related, this is referred to as STD INT in the connector tables. See Figure 2-22. Another type of phasing, referred to as STD EXT in the connector tables, relates station clock into the data output of the unit. In this case, the negative to positive transition of the clock shall be followed by the data transition within ±25% of the data unit interval. Polarity shall be as described in a.

e. Driver Offset. The magnitude of the generator offset voltage, measured between the center point of the test load and generator circuit ground shall not be greater than 3 volts.

f. Signal Balance. When the binary state changes, the polarity of V_t (see Figure 2-22) shall be reversed ($\overline{V}_t$). The magnitude of the difference in the magnitudes of V_t and $\overline{V}_t$ shall be less than 10% of V_t.

g. Ringing. When 100 ft of RG-108 A/U cable terminated in a 78 ohm dummy load is connected to the driver output, the waveform at the line output shall not overshoot its final value by more than 15%. Undershoot shall not reduce the signal to less than 87 mV.

h. Slew Rate. When 100 feet of RG-108 A/U cable terminated in a 78 ohm dummy load is connected to the driver output, the transition between ±40 mV (either direction) shall take no more than 10 ns for group data and timing signals and station clocks, and 100 ns for digital orderwire data and timing signals at 2, 16, and 32 kb/s.

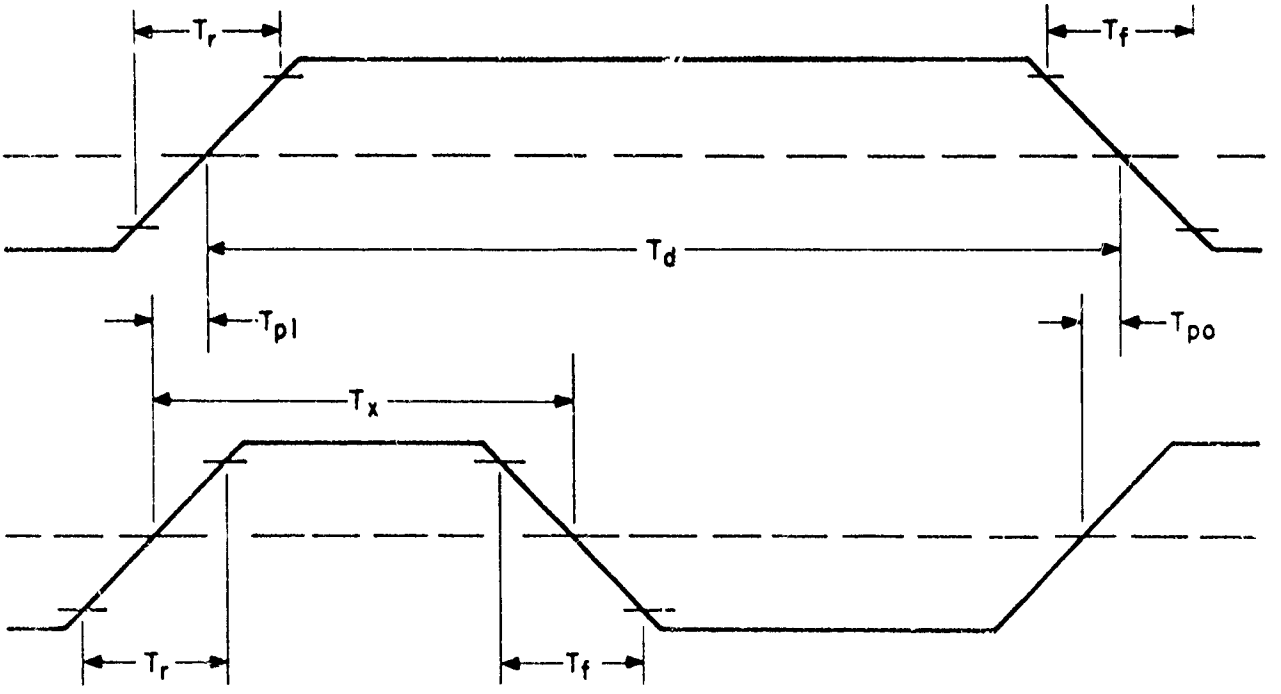
i. Receiver Sensitivity. The receiver shall deliver the proper digital output when a line-to-line voltage of +50 mV for a digital "1" or -50 mV for a digital "0" is applied at the receiver input terminals.

j. Input Load Impedance. 100 ohms ±10% line-to-line. Group rate data, clock, and timing inputs shall be center tapped to ground; all others may float.

TABLE 2-1

SIGNAL CHARACTERISTICS

Maximum Bit Rate	Delays Ns, Maximum	Rise or Fall Times, Ns Maximum	Clock Width Tolerance Ns Maximum
32 kb/s	±1500	3000	±1500
576 kb/s	± 240	300	± 120
5.0 Mb/s	± 29	30	± 15
18.72 Mb/s	± 8	8	± 4



T_d = Nominal Data Bit Time = 1/Bit Rate

T_x = Clock Pulse Width = $T_d/2$, nominal. Tolerance per Table 2-1

T_{pl} = Logic 1 Delay = Per Table 2-1

T_{po} = Logic 0 Delay = Per Table 2-1

T_r = Rise Time 10 - 90% = Per Table 2-1

T_f = Fall Time 10 - 90% = Per Table 2-1

Figure 2-22. Balanced Signal Waveshapes

k. Protection. The driver and receiver shall withstand without damage either:

Short, any line to ground

Short, line to line

Misconnection, to another line carrying a signal covered by paragraph a.

2.7.1 SLEW TIME

The TED interface document, TT-A3-9008-0024 requires that the slew time be limited to prevent the balanced line receivers from oscillating. The requirement is that the signal should get through the region from -40 mV to +40 mV (either direction) in less than 10 ns. Some of the DGM equipments did not meet this requirement because of filter pins put on the units to meet TEMPEST and EMI requirements. One unit, the LGM, did not meet in because of the line driver used (AMD 2616) which has a controlled slew rate.

Experiments with the TED were made to find out if the spec requirement was really necessary. At the maximum LGM rate of 576 kb/s, the tolerance of the TED was reached with a 280 ns slew time. This long a slew time means that a single data 1 or 0 barely crosses the triggering point of the line receiver, so that actually the TED only malfunctioned when the amplitude was inadequate. At the TGM maximum rate of 4608, the maximum slew time was 20 ns. Again, the amplitude is affected by such a long slew time.

It would appear that the 10 ns requirement is unrealistic. That there is a slew time problem somewhere can be demonstrated by the fact that the TED line receivers oscillate under both open circuit and short circuit conditions. NSA later confirmed that the 10 ns requirement can be relaxed.

However, Raytheon and the government have not relaxed this requirement. This is because the slew time affects diphase asymmetry as discussed in par 2.8. The slew specification remains at 10 ns for all signals that could drive the GM traffic port, where the asymmetry problem originates.

The 55107 line receivers used in the DGM program also have a slew time problem. Experiments have shown that the slew tolerance varies from about 150 ns to 400 ns depending on how much extraneous noise is present on the line. Therefore, the Raytheon ICD, 910669, calls for the digital signals at rates of 32 kb/s and below to have slew times of less than 100 ns.

2.8 103 MODEM

The 103 Modem is the functional equivalent of the present Group Modem, but it is designed to pass group traffic over the AN/GRC-103 radio instead of CX-11230 cable. In addition to the group traffic, the 103 Modem provides a Digital Voice Orderwire (DVOW), a Data Orderwire (DOW), and, in cooperation with the radio, an Analog Voice Orderwire (AVOW). All orderwires and the group traffic are usable simultaneously.

The 103 Modem is a baseband modem only. The rf modulation and demodulation are performed by the radio. The 103 Modem sends NRZ data at two rates to the radio and receives from the radio a video signal. The video signal is a filtered version of the NRZ data with added noise and AVOW. In the case of the higher rate, 1280 kb/s, the video signal is a biternary wave. In the case of the lower rate, the video signal is a binary wave.

The modem regenerates the digital portion of the video signal, separates the AVOW, and sends the recovered AVOW signal back to the radio.

2.8.1 REQUIREMENT DOCUMENTS

The requirements for the 103 Modem are set down in TT-B1-2202-0013A W/SCN 11 as modified by ECP PM-007C1.

2.8.2 CONFIGURATIONS

The configurations of the 103 Modem and the shelters in which it is used are primarily determined by the requirement for encrypted frame. The 103 Modem can be used without encrypted frame, and this simpler configuration is derived from the encrypted one by putting bypass cables in place of the TED connections. At the equipment side, group data and related timing are exchanged with the adjacent unit, no matter what unit that is. No other timing signals are used.

2.8.2.1 Shelter Configurations

The 103 Modem can be used in multiplex shelters such as the AN/TRC-173, and radio repeater shelters such as the AN/TRC-174. The multiplex shelter is the end of the line at least for the group to be considered. Entry to the mux shelter on this group side can be either on cable, thus becoming a cable terminal, or on radio, thus becoming a radio terminal. The repeater shelter can operate as a radio-to-radio repeater or a cable-to-radio repeater. It might be used as a cable-to-cable repeater, but none of the timing or crypto aspects of the 103 Modem are influenced by this case.

Figure 2-23 shows the significant cases. Both radio and cable terminals are shown because the cable terminal crypto arrangement must be considered in the 103 Modem system design, even though the 103 Modem is not used there. The radio-to-cable repeater is shown both forward and backward, because it is asymmetric.

The top line of 2-23 shows the CNCE and a cable-to-radio repeater where the cable side faces the node. If there is a SRWBR link present at the node, this has no effect on the timing or crypto arrangements (at least on the group). The group leaves the first line on radio and could jump to any of the other three lines.

The second line is the radio-to-radio repeater. This is designed to be completely symmetrical (at least for the group). The radio path out of the second line could jump to either of the next two lines.

The third line shows a radio terminal. The group considered stops here. If there is an application for encrypted subgroups beyond this point, that is a story for another day.

The fourth line shows a radio-to-cable repeater and a cable terminal. This kind of repeater is asymmetric, but the timing and crypto arrangements will be designed so that the repeater is reversable without any internal change to the group signals and timing. It can be seen that the cable-to-radio repeater on the first line is the mirror image of the radio-to-cable repeater on the fourth line.

The arrangements of Figure 2-23 were made to provide not only the required encrypted frame, but also these important features:

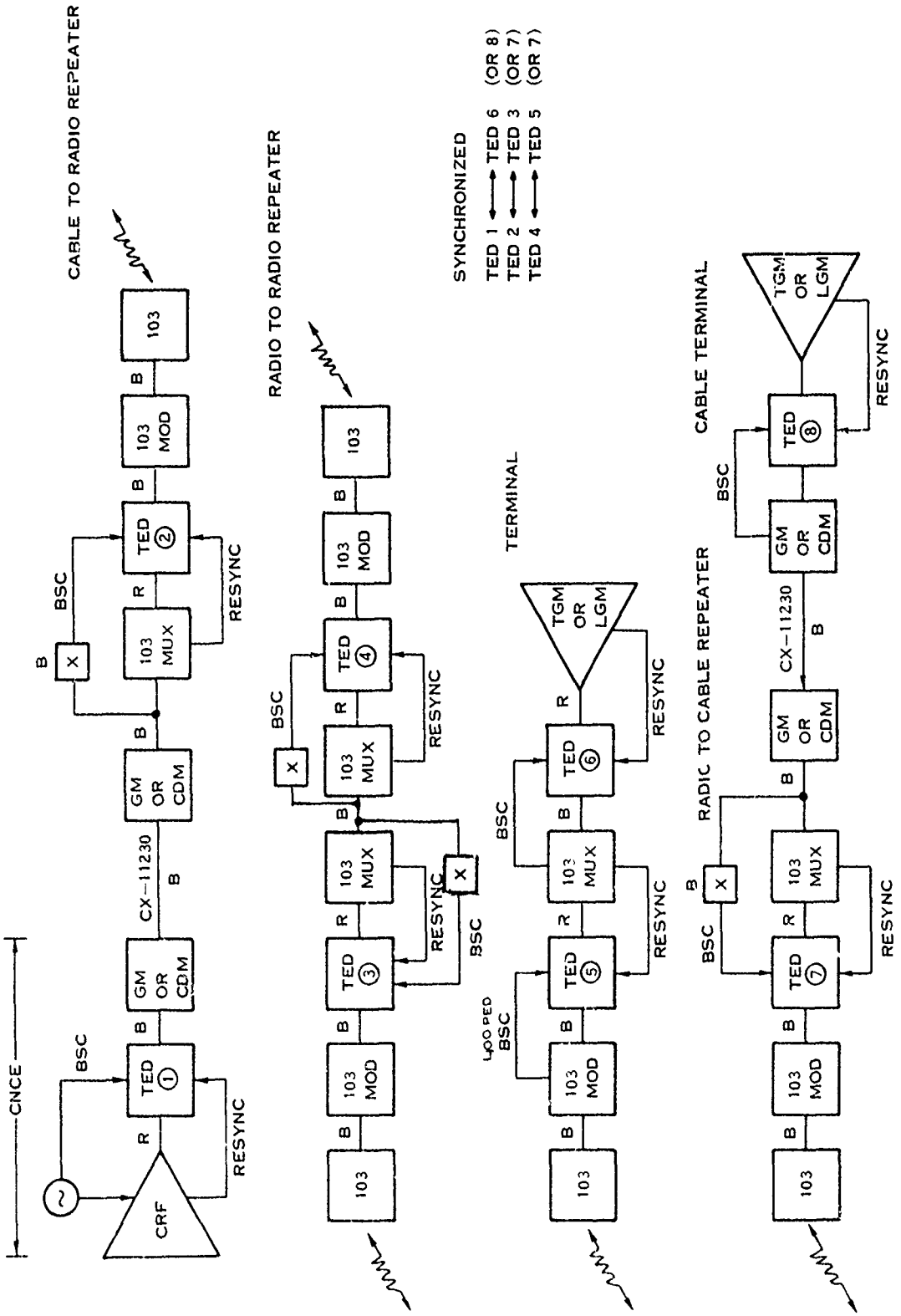


Figure 2-23 103 Modem Applications

a. The group equipment side interface of the 103 Modem is BLACK. As a result, no plain text appears on any CX-11230 cable.

b. Maximum isolation between BLACK Station Clocks (BSC) and RED signals is provided.

The principle consequence of all this is that the group is doubly encrypted on the radio and singly encrypted on the cable. We have tried to eliminate the double encryption, but that required a special unit between the 103 Modem and the cable modem to resynchronize the TED required at that point. A TGM in the single group mode might be used for this special unit. The addition of the TGM was rejected in favor of the double encryption.

2.8.2.2 BSC Arrangements

To understand the BSC and crypto arrangements, the multiplex and modem proper, both parts of the 103 Modem, are shown separately. In the top line, the repeater faces the node on the cable side (see Figure 2-23). Timing comes in through the GM at the group rate. In order to provide maximum timing purity, the BSC for the TED must be derived from this in a timing multiplier in the BLACK part of the 103 mux section. The multiplier must take the various timing rates (128 to 1152 kHz) and multiply them up to 640 or 1280 kHz, because this TED works at the radio rate.

On the second line of Figure 2-23, the radio-to-radio repeater is shown. Here the BSC for the TED's is also derived by the multipler. A separate BSC for radio repeaters was found to be unnecessary.

At the radio terminal on line three of Figure 2-23. there are two crypto units. The left hand one protects the 103 Modem frame. It gets its BSC from the modem section. This results in a timing loop-back on the BLACK side of this crypto. The other crypto protects the TGM or LGM frame. It gets BSC from the BLACK part of the 103 mux section. This BSC is at the group rate.

The repeater arrangement on line four of Figure 2-23 is the mirror image of the arrangement on line one. The cable terminal arrangement is the same as that already used for the GM.

2.8.2.3 Crypto Sync Arrangements

The first level of encryption involves the cryptos at the CNCE and at the terminal. Thus TED 1 works with TED 6 or TED 8. TED 6 or TED 8 receives resynch commands from either the TGM or the LGM, as applicable.

The second level of encryption is on a radio link by radio link basis. Thus TED 2 works with TED 3 or TED 7, etc. These cryptos receive resync commands from the mux section of the 103 Modem.

2.8.2.4 DVOW and DOW

The DVOW is a 16 kb/s channel synchronous to the group data. It uses the VINSON as an end instrument, a self-synchronous device. A buffer is provided in another unit, the OCU, which provides synchronization. The 103 Modem provides 16 kb/s receive data to the OCU with related 16 kHz timing. The OCU needs this timing signal to operate its signaling detectors. The VINSON does not accept a timing input. The 103 Modem accepts 16 kb/s transmit data without timing. It has an autophase circuit at its input because there is no known phase relationship between the VINSON buffer output and the group data. The VINSON buffer needs timing synchronized to the group data in order to do its synchronizing, so the transmit part of the 103 Modem provides a 16 kHz timing to the OCU for this purpose. Summing up, the 103 Modem puts out and accepts 16 kb data. It puts out two 16 kHz timing signals, one related to the received 16 kb data, and one synchronized to the transmit group data.

The DVOW signal into the 103 Modem goes through the TED, thereby becoming doubly encrypted on the radio links.

The DOW is a 2 kb/s channel synchronous to the group data. The OCU is the source of this signal. The 103 Modem provides 2 kb/s receive data to the OCU with related 2 kHz timing. The 103 Modem accepts 2 kb/s transmit data without timing. The 103 Modem also provides 2 kHz transmit timing. This is necessary because the 103 Modem might work without encrypted framing. If the framing is not encrypted, the DOW must be encrypted with a DLED. The DLED needs transmit timing from the 103 Modem. If the DLED transmit timing comes from the transmit section of the modem, potential problems due to the difference between transmit and receive frequencies are eliminated. In this case, DLED's

will be present on the DOW. The DLED timing arrangement requires that timing come from its BLACK side. This could be either transmit or receive timing from the 103 Modem, but using transmit timing gives the DOW system better immunity from other equipment failures. Summing up, the DOW interface is electrically the same as the DVOW interface, transmit data in, receive data out, and both transmit and receive timing outputs.

When the DOW goes through the TED, DELD's need not be used.

2.8.3 ASSIGNMENT OF SIGNALS TO CONNECTORS

The radio side interfaces are simple. The digital signal is carried in coax in both directions. It is planned to use separate BNC connectors. The AVOW interface consists of one pair for recovered orderwire and one pair for control in each module. All four pairs will be in one multi-pin connector.

Figure 2-24 shows a block diagram of the 103 Modem with these signal lines identified as well as the equipment side signals.

In particular, Table 2-23 shows the allocation of signals to connectors.

2.8.4 ELECTRICAL INTERFACES

The Group data, timing, and BSC; DOW and DVOW data and timing; and all signals going to the TED are balanced signals with 100 ohm terminations. They conform to ICD 910669, paragraph 1.1.

Figure 2-25 shows a simplified diagram of the GRC-103 radio interfaces. The video input impedance is 91 ohms. The 103 Modem delivers a fixed level of 2V p-p to the radio. The radio is specified to give the required deviation with any input from 1 to 4V p-p. The radio has two outputs, either one of which could be used. We have used the video one, which will give 1V p-p into 91 ohms for a deviation of $\pm$300 kHz. The modem operates over a range from 1/2 to 2V p-p. This range can be accommodated without a pot.

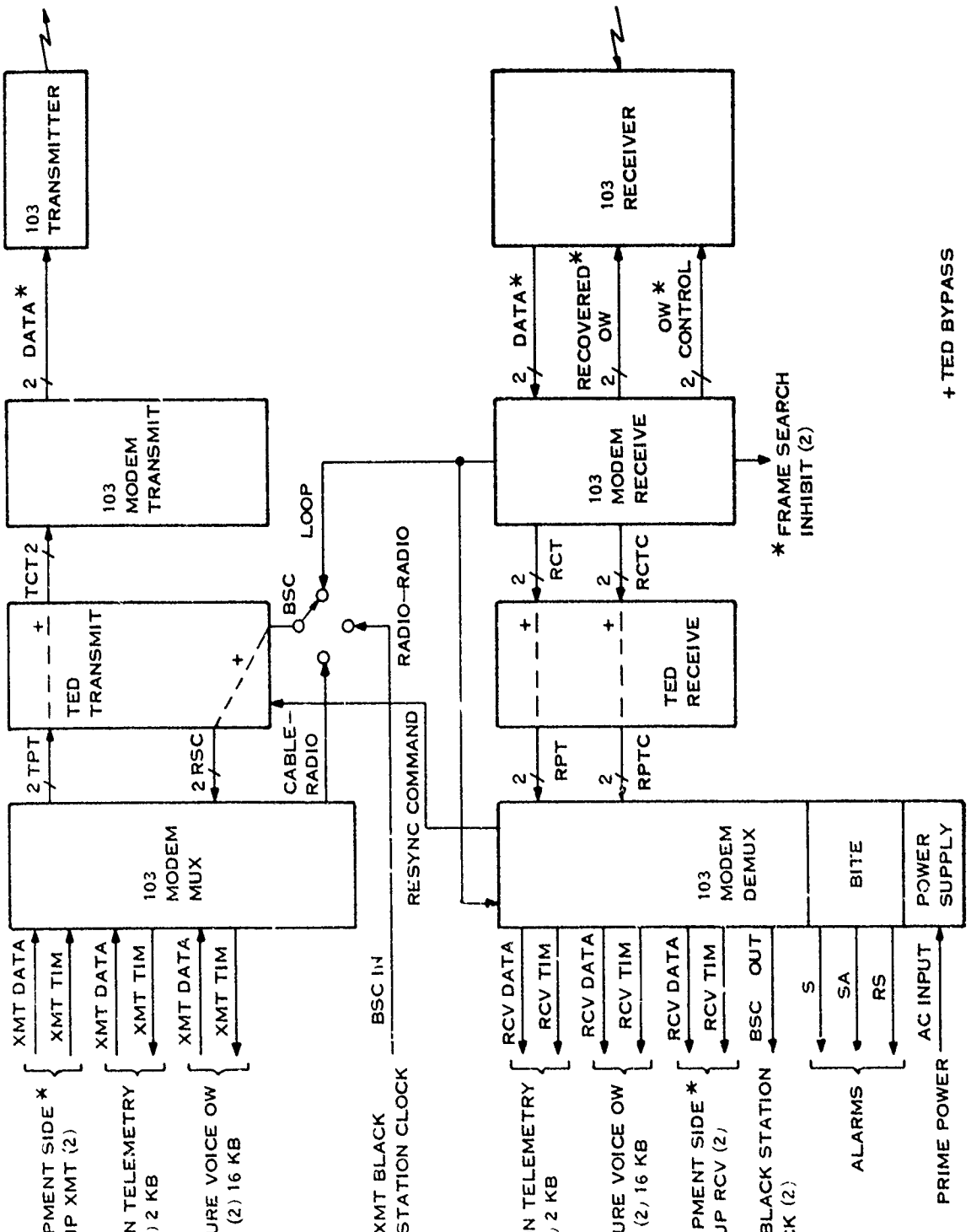


Figure 2-24 103 Modem Block Diagram

The radio orderwire input from the modem expects a nominal -4 dBm into 600 ohms. The radio termination is unbalanced. We feel that an unbalanced line is risky, a balanced interface is presented which can be grounded at the radio end. Therefore, at least some noise rejection is achieved. We thus have a fixed gain in the modem.

Alarm interfaces are contact closures, with closure representing the alarm state.

The frame squelch is in accordance with ICD 910669, paragraph 1.9.

The TED control is the Resync Command line per TT-A3-9008-0024, using the balanced option. Resync achieved is not required.

Table 2.8-1. 103 Modem Connectors

J1. Equipment Side Group 1

Signals:	Recommended Cable:	Minimum Number of Pins:
Xmt Data Xmt Tim Rcv Data Rcv Tim BSC	5 Shielded Twisted Pair	15

J2. Equipment Side Group 2

Identical to J1

J3. DVOW 1 and 2

Signals (2 each):	Recommended Cable:	Minimum Number of Pins:
Xmt Data Xmt Tim Rcv Data Rcv Tim	8 Pairs, Overall Shield	17

J4. DOW 1 and 2

Identical to J3

J5. TED RED 1 and 2

Signals (2 each):	Recommended Cable:	Minimum Number of Pins:
TPT RSC RPT RPTC	8 Shielded Twisted Pair	24

Table 2.8-1. 103 Modem Connectors (Continued)

J6 TED BLACK 1 and 2

Signals (2 each):	Recommended Cable:	Minimum Number of Pins:
TCT BSC RCT RCTC Resync Command	10 Shielded Twisted Pair	30

J7. AVOW 1 and 2

Signals (2 each):	Recommended Cable:	Minimum Number of Pins:
Recovered OW OW Control	4 Pairs, Overall Shield	9

J8. Alarms and Squelch

Signals:	Recommenced Cable:	Minimum Number of Pins:
S SA RS Squelch 1 Squelch 2	5 Pairs, Overall Shield	11

J9. To Radio 1
J10. To Radio 2
J11. From Radio 1
J12. From Radio 2

All BNC's with 91 ohm cable

J13. Power

J14. To Radio 1 EUROCOM
J15. To Radio 2 EUROCOM

BNC's with 91 ohm cable

J16. Timing Group 1

BSC 1 BSC In	2 Shielded Twisted Pair	6

J17. Timing Group 2

Identical to J16

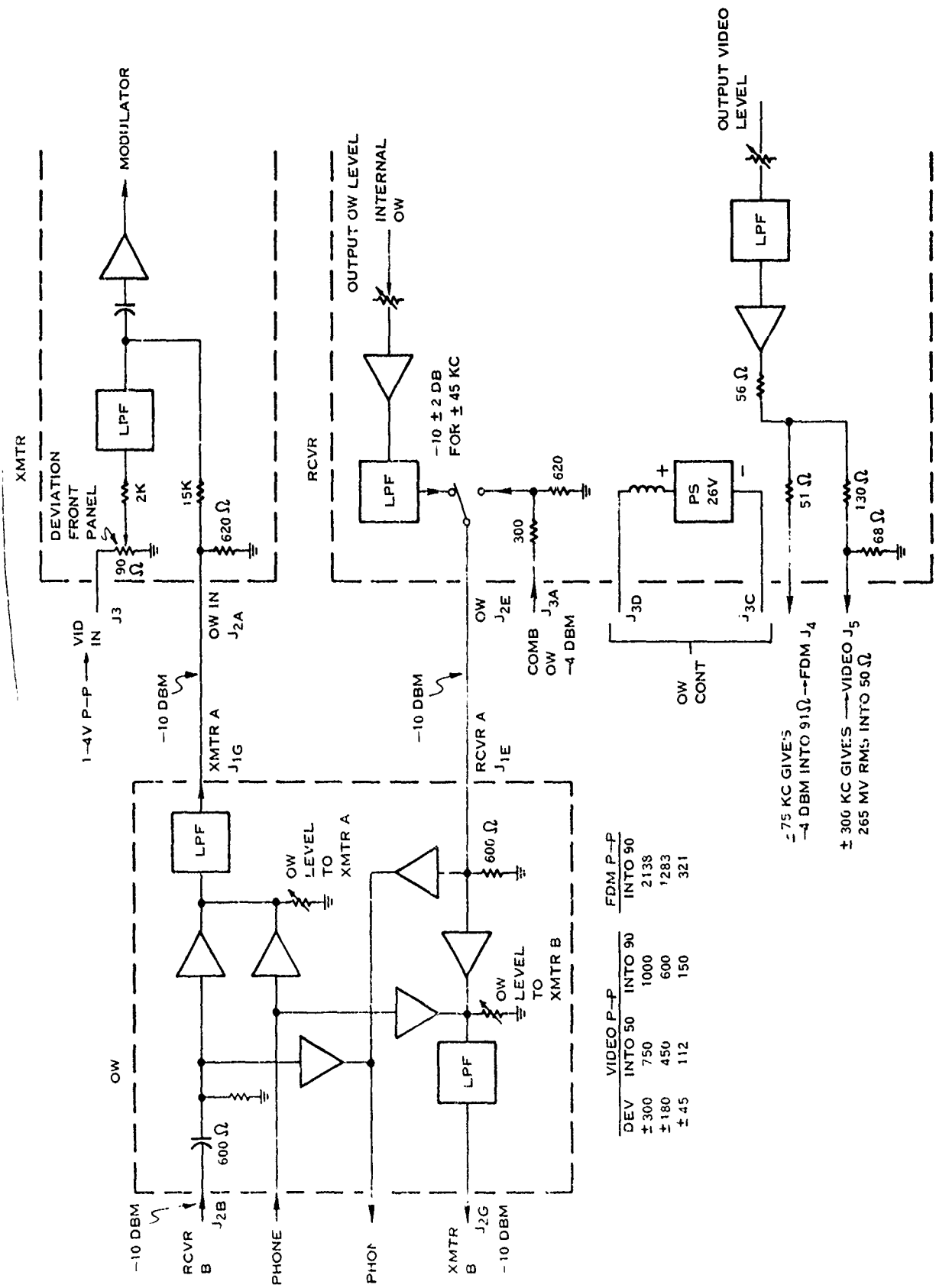


Figure 2-25 GRC-103 Radio Interfaces

2.8.5 VIDEO SIGNAL CHARACTERISTICS

The GRC-103 radio was designed to handle 1152 kb/s on a biternary basis and 576 kb/s on a binary basis. In order to get the DVOW and DOW over the radio, we are going to use TDM. This increases the bit rates to 1280 and 640, respectively.

Therefore, we may widen the baseband by 11 percent. This can be done either in the modem transmit section (pre-equalization) or the modem receive (post-equalization) section. Pre-equalization will give the best radio range, but it spreads the spectrum slightly. Post-equalization will reduce the radio range. Since this is an FM radio, its output noise spectrum is triangular. Therefore, if we change the receiver baseband width only, the variation of noise power with bandwidth is 30 dB per decade. An 11 percent increase in bandwidth translates into a 1.4 dB increase in noise.

Figure 2-26 shows the measured error rate performance of the old TD-202, taken under laboratory conditions. This eliminates temperature and radio output level variations. It is proposed to put the 103 Modem specification points as indicated in Figure 2-26. This will allow for post-equalization, temperature variations, and permit elimination of a modem input pot.

2.8.6 BEHAVIOUR DURING DEGRADED CONDITIONS

2.8.6.1 Fades

For fades of 30 msec or less, the modem receive timing and demux frame will maintain BCI. The 30 msec time is interpreted to mean a time during which the modem receiver is without any input information whatever. This means that in a true fading condition, BCI will be maintained over much longer fades. This is because there is usually a large signal range between the median received signal level and the signal level at which the timing recovery loses lock. The true outage time tolerance depends on the fade rate.

As the signal fades, the modem may take several actions, depending on length of fade:

a. It generates a frame squelch. This is useful only if the multiplexer is in the same shelter, i.e., at a radio terminal.

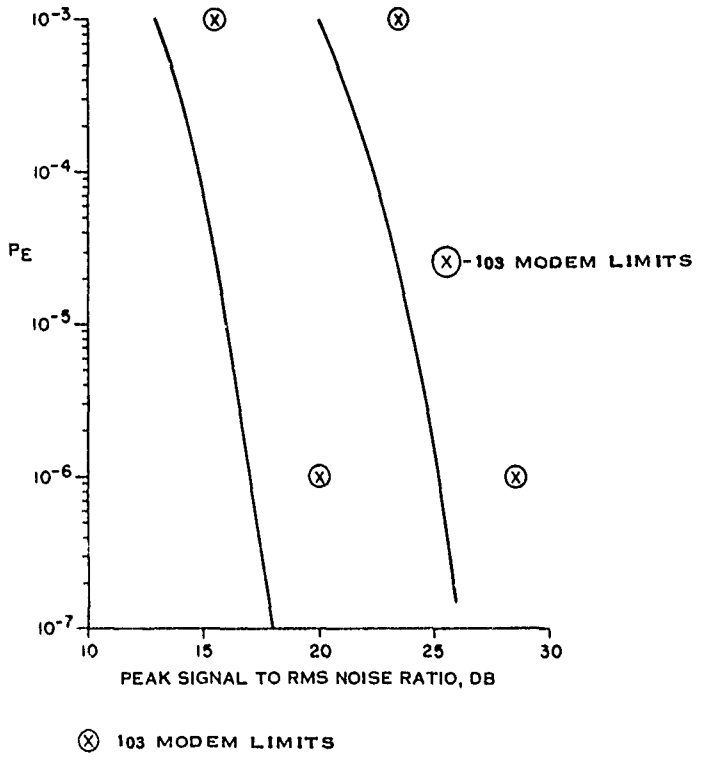


Figure 2-26 TD-202 Measured BER Performance

b. It operates the RS alarm sensor. The alarm itself will wait about one second.

c. It initiates the receive orderwire circuit to the radio. The modem orderwire separator makes the S/N in the orderwire worse instead of better if the error rate is very high. The actual transfer is displayed 30 ms.

If the fade is long enough so that the modem mux loses frame, further action will take place:

d. The group, DVOW, and DOW data outputs go to all 1's. It is necessary to do this for the DVOW because the OCU and CNCE have digital bridges which are siezed by activity. If a faded DVOW channel were connected to the bridge, it would sieze the bridge and lock out any good channels. Treating the group and DOW data signals is not necessary, but we will plan to put the feature in just in case. The related timing signals will be left running. The 2 kHz DOW timing is not usable during search. The 16 kHz DVOW timing is usable, as it may be used by other units such as the OCU.

e. For very long fades, the received timing signals will reach their free-running stability. This should be no more than 15 ppm off nominal. This will permit degraded DVOW and DOW operation from an OCU utilizing the 16 KHz timing signal.

2.8.6.2 Equipment Failure

If the equipment that fails is the remote radio, the failure will appear to the modem as a long fade. BCI will of course be lost, and actions a. through e. will be taken. There will be plenty of time for the RS alarm to operate. If the remote radio loses its modulation for any reason, the reaction of the modem is the same. The modem looks for the digital signal in the radio output. A radio receiver with no carrier puts out a large noise signal, but the modem rejects this just like it would a quiet circuit.

When there is no digital signal into the modem from the radio receiver, a number of BITE sensors inside the modem will indicate failure. The RS alarm will then go on. SA alarm on the same modem module however, will be suppressed. However, if RS is generated by one modem module while there is a real internal failure in the other modem module, the SA alarm will be generated.

There is a frame sensor on the modem demux. The question is: What alarms should be generated if there is a digital signal incoming (no RS alarm) but the demux is out of frame? Other DGM multiplexers will not give SA alarm on the grounds that most out of frame conditions are due to transmission failures. Given that there is no RS alarm, most transmission failures are discounted. An out of frame condition could be due either to a demux fault or the remote modem's mux fault. Since the demux frame circuit is more complex, the probability is higher that the demux is at fault, but not a great deal higher. We will include out of frame in the SA alarm.

If the equipment that fails is in the path driving the modem's equipment side group input, the modem takes actions which depend on whether the timing signal fails along with the data. The timing signal that matters is the one that runs the transmitter, and this is different in different configurations. It could be the related timing or loop timing. (Failure in loop timing is a failure internal to the modem.)

If the modem is using loop timing, and it does not fail, the modem will accept any signal still present. That is, failures in the digital orderwires and the group traffic are independent. The orderwires only need data in, while the group needs data and timing.

If the modem is using related timing, the failures are independent among the digital orderwires and group traffic only if the related timing does not fail.

No matter which of the two timing sources is used, if the timing fails, there is a failure or degradation of more than one signal. In addition, if the BSC's have no termination or cable connected, the operation of the modem shall not be adversely affected. There is a PLO in the transmitter which will take over operation of the modem. Its stability is about ±15 ppm, not enough to carry group traffic, but enough for the digital orderwires with some degradation. The DOW may loose BCI every 33 seconds depending on the OCU configuration. This is enough to get the telemetry data through, as that repeats every 1.3 seconds. The DVOW will loose BCI every 4.2 seconds. This will give very poor transmission. However, if the OCU uses the 16 kHz timing from the modem transmit section, BCI will be maintained as far as the rest of the system tracks this degraded timing. This would usually be as far as the top of the hill at the node, and will always be at least as far as the next shelter.

2.8.6.3 Outage Sensing

If the actions of paragraph 2.8.6 are to be taken, sensors must decide when the signal is poor enough to take action. An activity detector on the video input is useless, because a faded FM receiver gives a large noise output. Characteristics of the video signal itself must be sensed, and there are two candidates: timing and framing.

Timing is sensed by a narrow filter at the output of the zero crossing detector. The amplitude of the output is nearly constant for all useful S/N ratios, but fails below a S/N of 12 dB. This kind of sensor is not very precise, because there is amplitude modulation of the filter output due to data activity. However, it gives sensing at the earliest reliable point in the modem receiver.

The demux frame circuit is simpler in that most of the circuitry is required anyway. Its drawback is that it senses well back in the modem receiver, even behind the TED. However, it is a good sensor for the frame inhibit signal and the DVOW and DOW squelch. Certainly, if the modem demux is out of frame,

the group and digital orderwires are useless. Furthermore, the demux will sense the outage faster than the LGM or TGM, so the inhibit will catch them. The inhibit signal will not wait 30 ms like the frame search does.

If there are no failures within the modem or the TED, the demux frame is the best place to tie the RS alarm and the orderwire control because the indication if more reliable. However, these failures are important, and we will use the timing sensor for the alarm and control. This means that on slow fades we will be uncertain about the operating point of the alarms and will get a bounce condition.

The bounce condition causes no system trouble. What happens is that the sensor output will flicker on and off. It cannot be reported to the OCU unless the flickering persists for at least 1 second, and if it does persist, it is proper to report the alarm. The 1 second delay is provided by the BITE card.

2.8.7 FRAME

Figure 2-27 shows the frame formats. They have been chosen to give the simplest relationships between blocks and frames and between different rates and minimum buffers size. For the biternary signals, the frame code is three adjacent bits, alternating between 111 and 000. The frame rate is 16,000 per second, giving 80 bits per frame. The DVOW bit, marked V, follows the data block after the 111, and the DOW bit, marked T, follows the data block after the 000. The group data is carried in 18 bit blocks. With 1024 Kb traffic, two bits of these blocks are filled with dummy bits, 01 after the 111 frame and 10 after the 000 frame.

The binary cases use a single bit frame code altering between 1 and 0. The traffic is carried in 9 bit blocks which, in the 512 Kb case is filled with a dummy bit, 0 in every block. The frame rate is again 16,000 per second with 40 bits per frame. Modulation of the group data within the blocks is used so that the performance of the radio and the regenerator will be just as good with unencrypted groups as the encrypted ones. Table 2-24 shows this modulation as well as the multiple sampling pattern used for 288 Kb and less. The 288 Kb case takes two blocks to repeat because there are nine bits in a block.

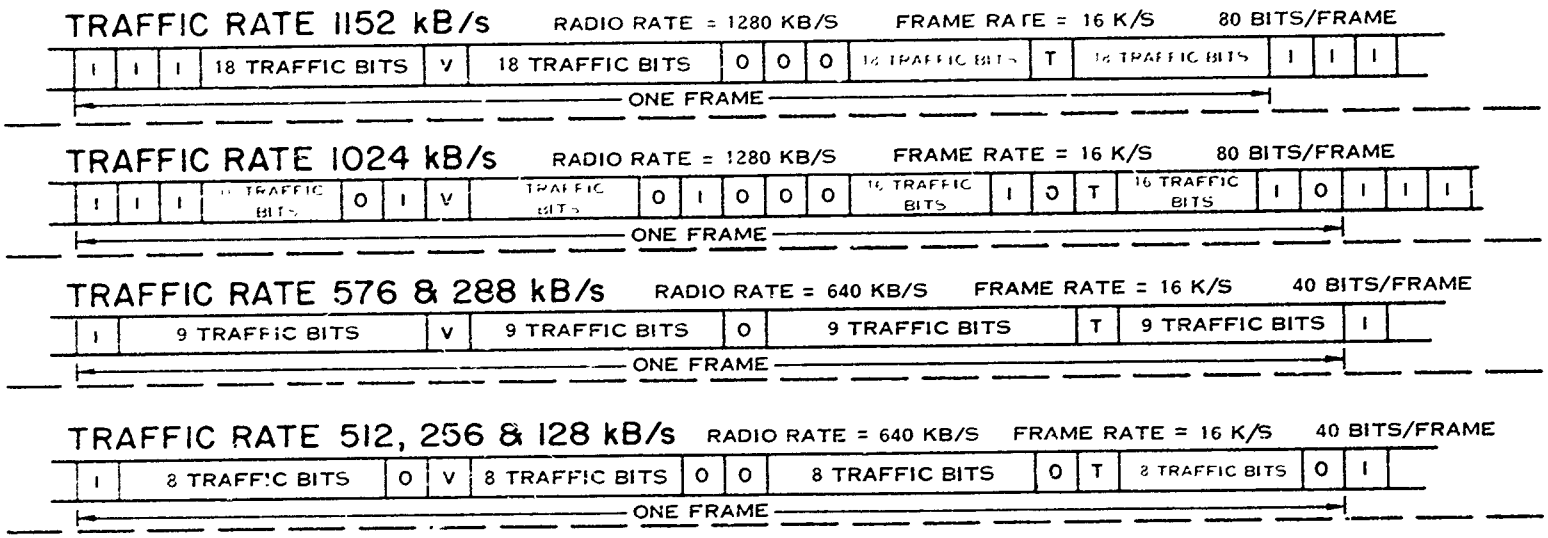


Figure 2-27 AN/GRC-103 Modem Frame

Table 2.8-2. Group Data Modulation

Bit Rate, kb/s	Group Bits in Block	Modulation
1152	18	$D_1\ \overline{D_2}\ D_3\ \overline{D_4} \ldots D_{17}\ \overline{D_{18}}$
1024	16	$D_1\ \overline{D_2}\ D_3\ \overline{D_4} \ldots D_{15}\ \overline{D_{16}}$
576	9	$D_1\ \overline{D_2}\ D_3\ \overline{D_4} \ldots \overline{D_8}\ D_9$
512	8	$D_1\ \overline{D_2}\ D_3\ \overline{D_4} \ldots D_7\ \overline{D_8}$
288	9	$D_1\ \overline{D_1}\ D_2\ \overline{D_2} \ldots \overline{D_4}\ D_5$ (OH) $D_5\ \overline{D_6}\ D_6\ \overline{D_7} \ldots \overline{D_9}\ D_9$
256	8	$D_1\ \overline{D_1}\ D_2\ \overline{D_2} \ldots D_4\ \overline{D_4}$
128	8	$D_1\ \overline{D_1}\ D_1\ \overline{D_1}\ D_2\ \overline{D_2}\ D_2\ \overline{D_2}$

The DOW bit is also modulated. The modulation is the same as used in the GM: The data is EXCLUSIVE OR'd with a 16 kHz square wave which is set low at the DOW bit transition time.

These frame formats are immune to false loc. if the group is all 1's or all 0's and the digital orderwire channels are idle or active. Furthermore, the frame format is immune to unencrypted traffic. No known multiplexers or end instruments put out a 1010 pattern on a permanent basis.

2.8.7.1 Framing Lock-In Calculations

First we must determine the number frame bit verification tests that will keep the false lock probability well below 10 percent of the trials. The 1 bit frame code used in binary is the worst case. There are 20 bits between frame bits. If we count the first time we look at a bit in the number of tests, the probability of false lock per bit is:

$$2^{-(M-1)}$$

because the alternating pattern forces us to accept either a 1 or a 0 on the first look. The advantage of doing this is that we only have to search a half-frame. The probability per half-frame is then:

$$20 \times 2^{-(M-1)}$$

Setting this equal to 2 percent, we get M = 10.96, so we take M = 11.

To estimate the frame-in time, we assume that the frame search starts at the worst bit and calculate the average search time to the next frame bit. This simplified procedure gives a number accurate enough to guarantee that a series of measurements will better the number at least 90 percent of the time.

Each of the false bits must be rejected. The rejection alone takes one half-frame. Testing takes more time. The probability of a bit passing the test the first time is 1.0, because we accept it, whatever it is. The probability of a random bit passing any subsequent test is 1/2. The probability of passing K or more tests is $2^{-(K-1)}$. The probability of passing K tests and then failing is:

$$P(K) - P(K+1) = 2^{-(K-1)} - 2^{-K} = 2^{-K}$$

In order to get the average number of half-frames taken per bit we sum the probability of taking K tests multiplied by the time necessary to do K tests over the values of K. The time necessary to do K tests and then fail is K half-frames, because we bet to take one test each half frame.
The average number of half-frames taken per bit is:

$$\sum_{1}^{M} \frac{K}{2^K} \approx \sum_{1}^{\infty} \frac{K}{2^K} = 2$$

This figure will now be used to calculate the lock-in time, where it appears in the "testing data bits" term.

The lock in time, in half-frames, for a distance between frame bits of N bits is then:

1 (rejecting) + 2N (testing data bits) + (M - 1) (testing the frame bit) = M + 2N

With N = 20 and M = 11, lock-in takes 51 half-frames. There are 32,000 half-frames per second, so this is 1.6 ms. We have increased the number of tests to M = 17, giving 1.79 ms.

For the biternary case (Figure 2-28), the 3 bit frame code speeds things up. If we calculate again the number of tests to keep false lock below 2 percent, we get M = 4.

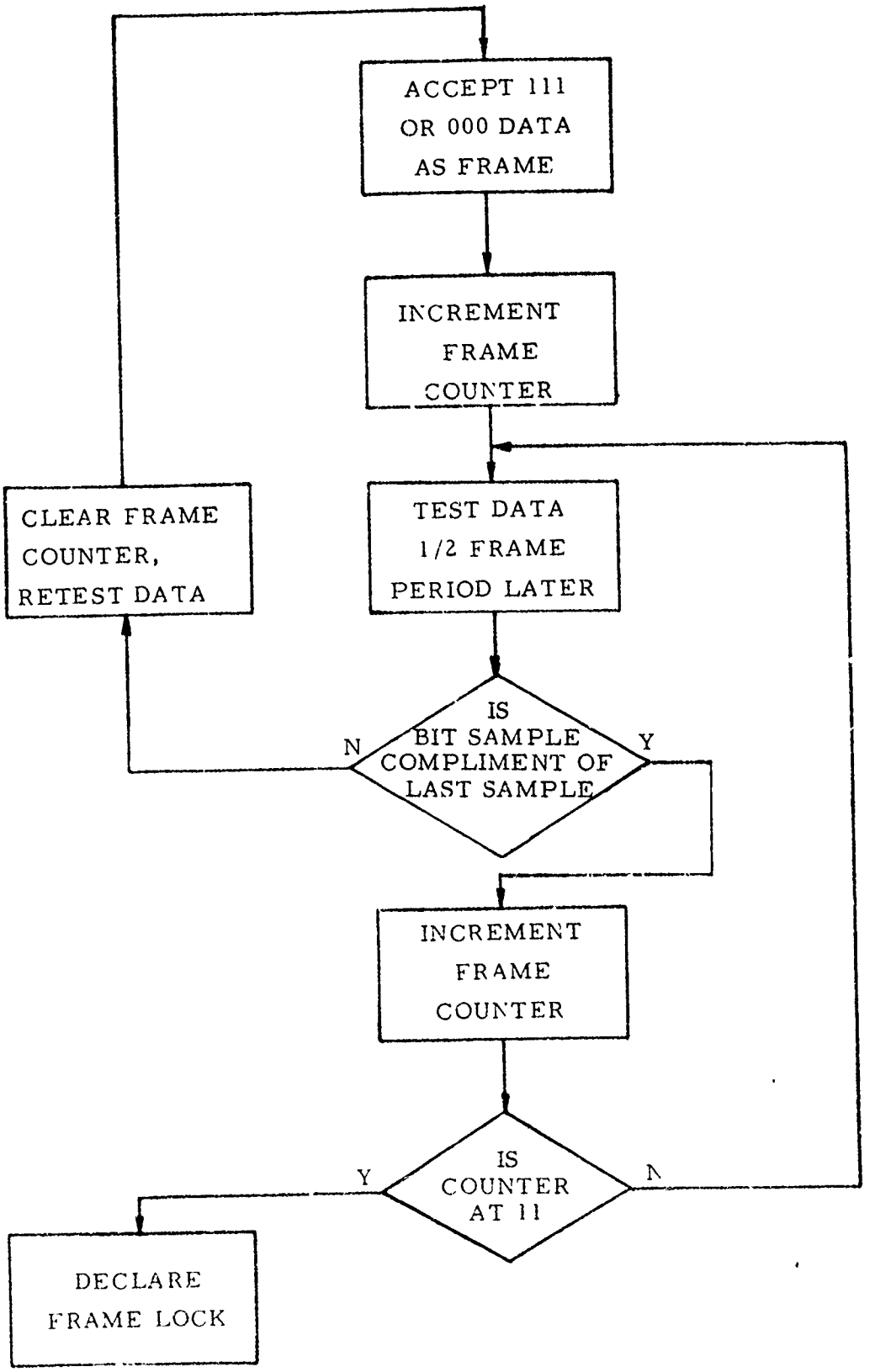


Figure 2-28 . AN/GRC-103 Modem Framing Flow Chart, Biternary.

Again, rejecting bits takes a half-frame, 40 bits here. We examine the data three bits at a time, but search one bit at a time. The probability of any random bit simulating either 111 or 000 on the first test is then $2/(2)^3$, as we must accept either. On subsequent tests, the probability of passing is $1/(2)^3$. The probability of passing K or more tests is $2/(2)^{3K}$. The probability of passing K tests and then failing is:

$$\frac{2}{2^{3K}} - \frac{2}{2^{3K+1}} = \frac{7}{4 \times 2^{3K}}$$

The average number of half-frames per bit is:

$$\sum_{1}^{M} \frac{7}{4} \frac{K}{8^K} \approx \frac{7}{4} \sum_{1}^{\infty} \frac{K}{8^K} = \frac{2}{7}$$

The lock in time, in half-frames, is then:

$$1 + 2N/7 + (M - 1)$$

With N = 40 and M = 11, this is 22.4 half-frames or 0.7 ms. We have increased the number of tests to M = 17, thus getting 0.82 ms.

2.8.7.2 Framing Maintenance Calculations

The exact calculation of frame maintenance performance is a very difficult random-walk problem. However, it is so easy to give very good performance, a gross approximation will serve. Let us set the drop-out criterion to M frame bits in error in some short time, say 2M or 3M half-frames. This time has little effect in this approximation. Then the drop-out probability for binary per half-frame is $(P_e)^M$. We calculate the mean time to drop-out in hours, H:

$$H = \frac{1}{3600 \times 32,000 \, (P_e)^M}$$

For M = 11 and $P_e = 10^{-3}$, we get 8.68×10^{24} hours. Frame drop-out will occur with 5 wrong bits out of 16.

For biternary (Figure 2-29), we assume that any one of the three bits in error counts as a defective code. Then the estimated mean time between drop-outs is:

$$H = \frac{1}{(3P_e)^M \times 3600 \times 32,000}$$

which gives 4.9×10^{19} hours for M = 11 and $P_e = 10^{-3}$. Frame drop-out will occur with 6 wrong codes out of 16.

2.8.7.3 Bit Acquisition Calculations

In meeting the bit and frame acquisition time specifications, the bit acquisition is expected to take longer than frame-in. The PLO that acquires bit timing is subject to several conflicting requirements: It must maintain timing over a 30 ms outage. It must have a free running stability of 15 ppm, and accept the MGM jitter which can swing $\pm$47 ppm.

Let us estimate the maximum bit acquisition time by setting the loop as narrow as we can. The pull in range should be at least 15 ppm plus 47 ppm, or 62 ppm. At 640 kHz, this is:

$$\omega_p = 62 \times 10^{-6} \times 2\pi \times 640 \times 10^3 = 249 \text{ rad/sec, minimum}$$

The natural frequency of the loop is:

$$\omega_n = \frac{2\omega_p}{\pi} = 159 \text{ rad/sec}$$

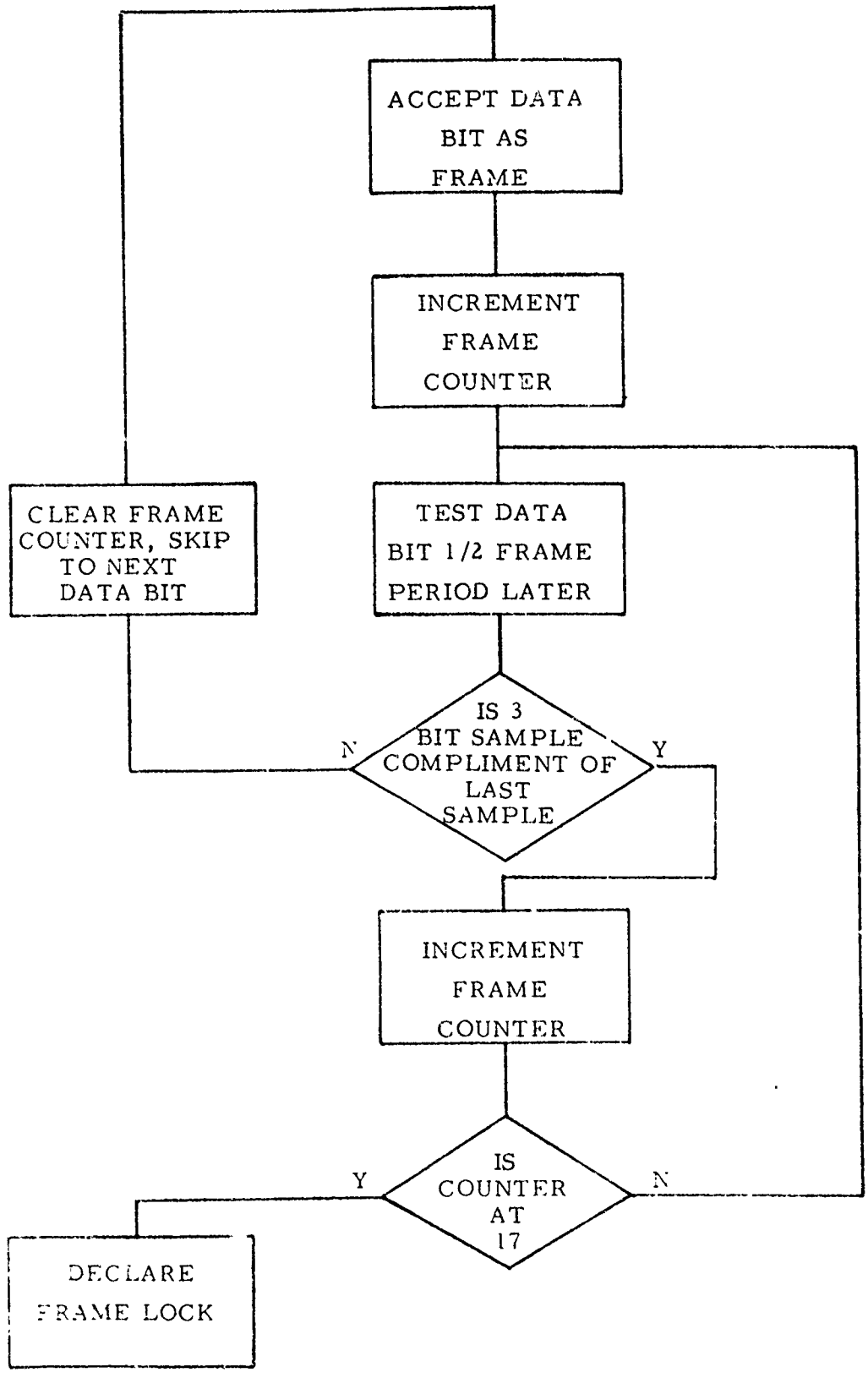


Figure 2-29 AN/GRC-103 Modem Framing Flow Chart, Binary

The acquisition time is approximately:

$$T \approx \frac{(\Delta\omega)^2}{2\delta\,\omega_n^3}$$

where

$\Delta\omega$ is the frequency error before acquisition and is equal to the minimum lock-in range. δ is the damping factor. If the designed lock-in range is equal to the minimum:

$$T = \frac{1}{2\delta\,\omega_n}$$

Using

$\delta = 1$, we get

$T = 3.12$ ms.

If these assumptions hold up, the bit and frame acquisition time would be about 4.7 ms in the binary case. Biternary is faster.

2.8.7.4 Framing Loss Detection and Reacquisition Calculation

If BCI has been lost, but timing maintained, the dropout time and BCI maintenance time must be added to the framing time. The dropout time in 50 percent errors is again a random-walk problem, but let us assume that an extreme value is twice the length of time over which errors are accumulated. This was assumed in the framing maintenance calculation at no more than 64 half frames. This is 2.1 ms. The maintenance time is at most 35 ms, thus dropout and reframe are estimated at 38.7 ms. The spec has been changed to 39 ms.

Dropout time in biternary is the same, because we count any error in the 3 bit code as a defective code. Dropout plus frame-in is faster, about 37.8 ms.

2.8.7.5 BCI Maintenance

The 103 Modem is required to maintain BCI for signal losses up to 30 ms. The multiplexer in the modem must be prevented from dropping out and coming back. A delay of 31 to 35 ms will be provided.

2.8.8 FRAME SQUELCH

The 103 Modem will provide a frame search inhibit signal in accordance with the specification. However, in a TRI-TAC system, this feature is useless.

First consider a single hop system. One radio hop connects a radio terminal to the node. If a fade affects the signal toward the node, the group mux in either the CNCE or the switch will go out of frame because this mux has no access to the frame squelch signal. The framing handshake routing will cause traffic in both directions to be interrupted. The frame squelch has accomplished nothing.

In many cases, a fade will affect both directions, either simultaneously or within a very short time. Again the frame squelch accomplishes nothing.

The only time it works is when the fade affects the signal away from the node only. The mux in the radio terminal is prevented from starting a resynch and reframe cycle.

If there is more than one radio hop in the system, the frame squelch hardly ever helps. Any fades that affect the repeater station will cause the resync and reframe cycle.

2.8.9 TED CONTROL

The modem mux must request the TED to resynchronize at the proper times. When the mux is in frame and drops out, it must request a resync right away, within a few bits at most. In most cases, the system will be back on the air after the first request. If there is an equipment failure somewhere, it will

be a long time before the system is back up. During this time repeated requests must be originated.

To ensure that the second and subsequent requests do not put the system into a continuous turmoil, these requests must be spaced by a minimum period. We will take this to be the TED resync time plus the specified modem mux drop-out and reframe time (this is longer than the calculated time). The TED at 640 kb/s and a 40 mile hop will take at most 13.2 ms. The specified modem mux time is 25 ms. The minimum spacing between resync requests is then 38.2 ms. The maximum is a fairly open figure. Restoral after equipment failure is a matter of many minutes, so any spacing from 100 ms to 5 seconds or so will not influence system performance.

2.3 ASYMMETRY

Informal interface tests were made between the DGM family and the 3ª switch. The interface point between the two is where a digital group signal is exchanged on CX-11230 cable in conditioned diphase form. The Raytheon Conditioned Diphase GM faces the Sylvania Conditioned Diphase GM.

It was found that the 39 GM was extremely intolerant of asymmetry in the diphase waveform. Asymmetry is the misplacement of the zero crossing in the center of digital 0's with respect to the ideal center. The tolerance is worst at the highest rate, being only 4 percent of the NRZ bit interval at 4ºº mb/s. This figure becomes about 8 percent in the 2 mb/s range, and 10 to 20 percent from 1 mb/s down.

Most of this intolerance was discovered to be in a fault sensor which was intended to alarm on excessive jitter. This sensor detects asymmetry as jitter. Another series of tests were run to determine how much asymmetry could be tolerated without this sensor. In the 39 Supergroup Modem the 4 mb/s tolerance went up to 10 percent, and the 2 mb/s to greater than 12 percent. The group modem was more tolerant than this, except at 1/4 mile distance. There, the fact that the slicer does not slice the signal at zero volts causes further problems with asymmetry. One reading of 6 percent was encountered.

Experiments were made with the GM in the CNCE. The Martin GM was more tolerant, being generally no worse than 9 or 10 percent, and often better.

The Martin and Raytheon GM's generate asymmetry because they use the related timing directly to form the diphase wave. This is the simplest way, and uses the least PCB area, but means that the symmetry of the diphase wave can be no better, and is generally worse, than the related clock.

The asymmetry generated in the DGM GM was analyzed and was found to come from three sources. The first is the distortion of the signals caused by delays and rise times in the logic circuits within the modem. The second is the asymmetry allowed on the related timing coming into the modem. The third is the slew time, which is converted into asymmetry in the ratio of 3:4. The worst case figures are:

Modem	13.0 ns
Input timing asymmetry	15.0 ns
3/4 of the slew time	7.5 ns
Total	35.5 ns

This is 16.4 percent of a bit at 4608 kb/s and 8.2 percent of a bit at 2304 kb/s. Actual modems run between 1/2 and 3/4 of the maximum.

A look at the three sources will show that any appreciable improvement in the asymmetry would involve making the diphase asymmetry independent of the related timing waveshape. This would require a great deal of PCB area. The 39 GM solves this problem by providing 8X group rate clock to each modem. This solution would not fit in the GM case.

A solution which will fit is being developed on a separate contract. Preliminary results indicate that the asymmetry can be kept to less than 5% of a bit over the range of equipment side clock distortion permitted by ICD 002.

2.10 MGM JITTER INVESTIGATION

2.10.1 FREQUENCY JITTER VS PHASE JITTER

In general, both the phase jitter and the frequency jitter are of interest. Some equipments are more sensitive to the phase peaks and others to the frequency peaks. The equipments sensitive to the phase peaks are those with very narrow timing bandwidths. These equipments do not track the frequency peaks. Therefore, their phase stays at a nearly constant position while the input data varies in phase about that position. Examples of this are the TRC-170 and the CDM. They dejitterize the incoming signal.

The equipments sensitive to the frequency peaks are those with wider timing bandwidths. These equipments try to track the incoming frequency peaks. An example of this is the GM. It passes the incoming jitter through to its output. It is very probable that the TRC-143 and TRC-144 are more sensitive to the frequency peaks.

There appears to be some equipments that are part way between and are affected by both. The group modem in the RMC is an example of this. It is sensitive to frequency peaks, but the sensitivity is worse at the time when a phase peak occurs.

2.10.2 MULTIHOP VS SINGLE HOP JITTER

In an actual system, jitter is eliminated by passing through the CRF in a CNCE or the time division matrix in a switch. Therefore, any group coming out of a node normally has one hop of bit stuffing jitter when it reaches the top

of the hill. Therefore, most of the TRI-TAC system will experience the jitter of one hop of bit stuffing.

This jitter is quite different from subsequent hops because the master-group clock and the group clocks come from the same source.

When a group which comes from one node (with one hop of jitter) arrives locally at the top of the hill, a second hop of jitter is introduced in getting down the hill. Therefore, at the bottom of the hill, the CNCE (or switch, if there is no local CNCE) can normally expect to see two hops of jitter on incoming groups. If there is a local CNCE and a switch together, the switch will not see any bit stuffing jitter.

Normally, this group, with the two hops of jitter, enters the CRF in the CNCE. When it emerges, there is no jitter left. However, it is possible to patch the incoming group from the MGM right back out the MGM. This group arrives back at the top of the hill with three hops of bit stuffing jitter. The frequency and phase jitter components vary differently as the number of hops increases.

2.10.3 FREQUENCY JITTER

The maximum frequency deviation is measured from the nominal group bit rate, not the average of the actual group put in. The maximum peak frequency deviation is $\pm$ 47 ppm from nominal. The rate of change of frequency is such that the rise time, measured at the 10 percent and 90 percent points, of a change from one peak to the other is 30 usec. The maximum rate of change of frequency is 3.5 ppm per microsecond. This peak is achieved in the first hop and does not increase in later hops.

2.10.4 PHASE JITTER

The p-p phase jitter is measureable on a scope. Because the maximum jitter occurs rather infrequently, a storage scope was used. Using a single MGM, measurements can be made of the jitter from one or two hops. To get the one hop jitter, the mastergroup clock is synchronized to the group clock. To get two hop jitter, the mastergroup is free-running. The one hop jitter is present, along with the second hop contribution, when the master-group clock is free-running.

Quantatively the jitter consists of at least three components:

a. A slowly occurring component with peak-to-peak value up to 2 bits for 2 hop jitter and up to 4 bits for 3 hop jitter.

b. A more rapidly occurring component which is roughly one-half the total peak-to-peak value. For example, at the 4915.2 kbps rate this component was estimated at 0.9 bits by taking a 10 second time exposure photo which visually resolved these two components.

c. A very rapidly occurring component with a peak-to-peak amplitude of one quarter bit or less. This is the synchronous jitter component due to the predominent occurrence of alternate stuffs and spills. It is isolated by slaving the multiplexer clock to the group rate clock.

The phase deviation given in Table 2-2 are those for the worst case; which is the low mastergroup for group rates up to 2304 kb/s. The 4096, 4608, and 4915.2 kb/s rates can only use the high mastergroup, and that is the figure given for those rates.

TABLE 2-2. PEAK-TO-PEAK JITTER, IN BITS

Group Rate, kb/s	1 Hop	2 Hops	3 Hops
72	Less	1.0	2.5
128	than	1.0	2.5
144	0.06	1.0	2.5
256	↓	1.0	2.5
288		1.1	2.5
512	0.06	1.3	2.6
576	0.07	1.4	2.7
1024	0.11	1.5	3.0
1152	0.12	1.6	3.1
1536	0.16	1.9	3.4
2048	0.20	2.2	3.7
2304	0.24	2.3	4.0
4096	0.20	2.2	3.8
4608	0.24	2.3	4.0
4915.2	0.26	2.4	4.2

2.10.5 JITTER WAVEFORM

Figure 2-30 shows a jitter waveform, both frequency and phase. In the case shown, the actual input group rate is close to the nominal rate. Most of the time, the frequency moves rapidly between the two limits. The resultant phase change is then a small triangular wave. Occasionally, the frequency stays at one peak for a longer time, thus giving a bigger phase change. In a one hop system all groups are synchronized to the mastergroup. In this case, the small phase changes happen all the time, and the bigger changes do not occur.

2.10.6 JITTER REDUCTION

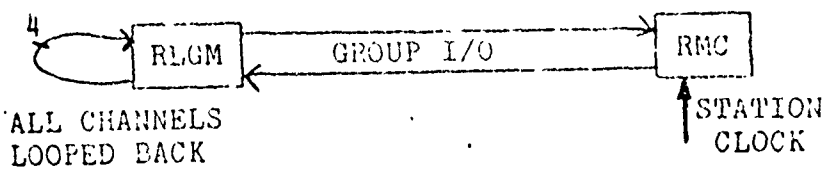
Work is underway on another contract to develop a Group Logic PCB which will have much less jitter. Preliminary results indicated that the frequency jitter can be kept below ± 1.25 ppm.

2.11 FALSE FRAME LOCK

The hand-shaking frame routine used in TRI-TAC was not designed for loop-back applications, but looping back a group is a handy technique for testing, troubleshooting and demonstrations. However a false lock condition is possible in some cases. Two cases of this problem are analyzed below.

2.11.1 LOOPING AT CHANNEL INTERFACE

A stable state of false synchronization exists for a pair of DGM multiplexers when one of the multiplexers has all of its channels looped back on themselves. The following is a demonstration of the problem:



Assume that both the RLGM and RMC are connected as shown. The RLGM recovers timing from the Conditioned Diphase group signal from the RMC. Power is applied to both units and the group signal is connected. Initially both units attempt to frame while the phase-locked loop on the RLGM Timing Generator is still locking to the recovered clock. At a time before lock in the phase locked loop is achieved, both units declare themselves "In-Frame". Lock to the recovered clock is then achieved. The resulting change in the RLGM transmit frequency may then cause the RMC to lose frame. The RMC is "Out-of-Frame" and transmits DATA 0, a 1111 frame pattern, and 0's

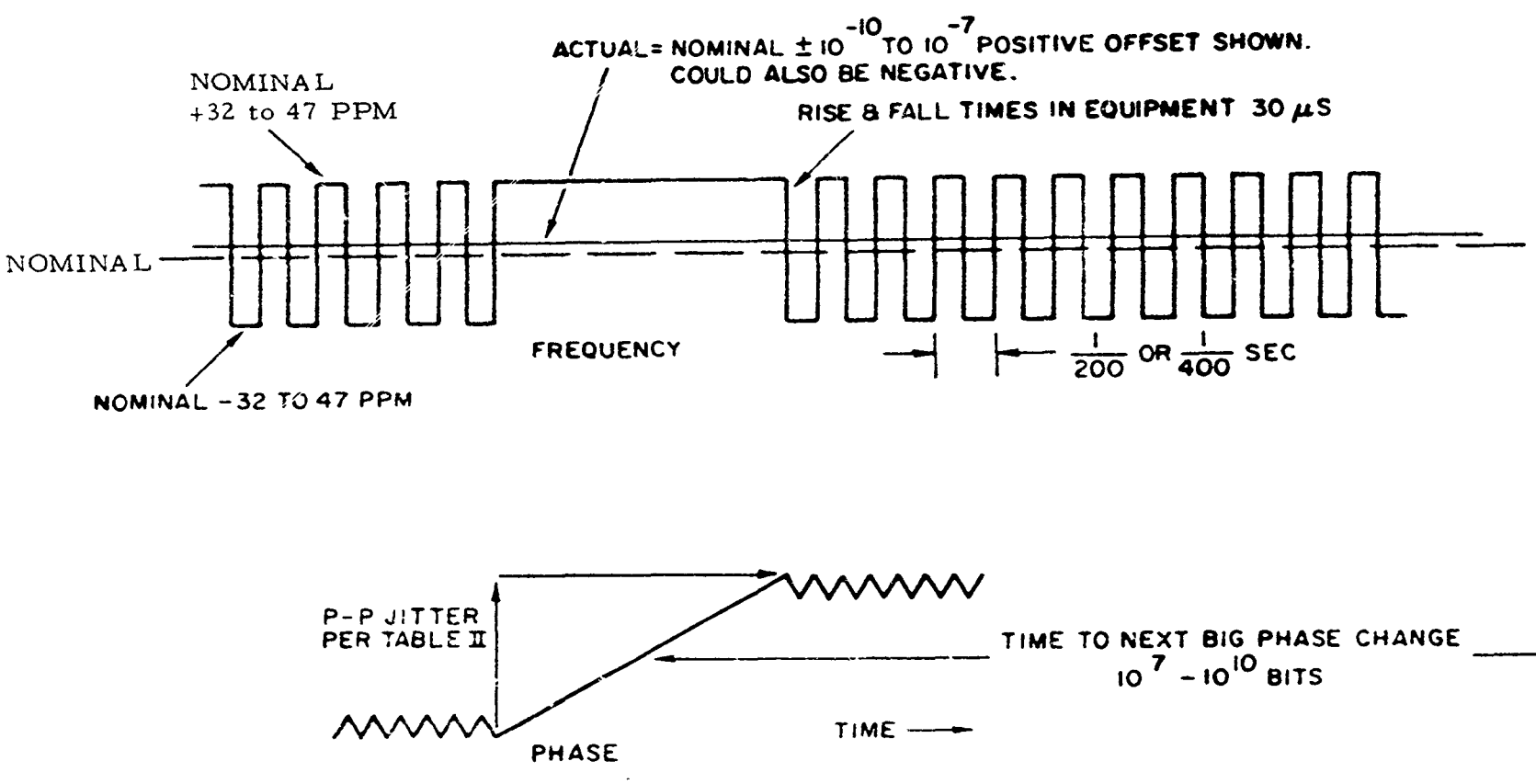


Figure 2-30. MGM Jitter

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EQUIPMENT DIVISION
RAYTHEON

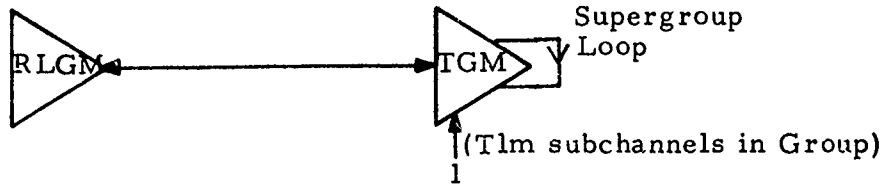


in all other subchannels of the overhead channel. The RLGM at this point has not yet detected the 1111 pattern transmitted by the RMC, so the RLGM transmits the "In-Frame" pattern (1010), all DATA = 0 (due to the loop-back of all data channels which have just been set to all 0's by the RMC) and some unused (i.e., all 1's) overhead subchannels. The RMC, having declared itself "Out-of Frame", initiates frame search. Frame search sometimes acquires lock on the unused overhead subchannel (a 1111 pattern). Frame acquisition can occur in as few as 32 correct frame bits. During the time that the RMC acquires frame, the RLGM has been in the process of detecting the "Out-of-Frame" again. The RLGM turns the data back on after 32 bits because it has received "In-Frame" from the RMC. Now the RMC is locked to the false pattern and does not transmit data to the RLGM (the 1111 pattern indicates to the RMC that it shall not transmit data). Because the RMC transmits no data 1's, the looped-back RLGM transmits no data 1's and the RMC stays locked to the other subchannels. The state is stable with no indication (BITE or Alarm lights) that anything is wrong. The link does not pass data.

The following observations are made. The state is entered only when all channels are looped-back, causing false lock in the unit which is not looped back. When the loop-back is opened, the condition corrects itself (in the above example the RMC would detect the 1111 pattern with DATA $\neq$ 0's and resume frame search when the loop-back was opened). The false state exists as a result of the specification for idle or unused channels (all 1's), the definition of frame coordination and search procedures and the specification of detection and acquisition times. The condition is not unique to DGM equipment; any multiplexer using the same techniques has the same problem.

The problem is not tied to the characteristics of the Timing Generator phase-locked loop per se. Any disturbance to the link which, in the example, would cause the RMC to declare "Out-of-Frame" while maintaining the RLGM "In-Frame" has a potential of causing the false sync problem.

2.11.2 LOOPING AT GROUP INTERFACE



1. Both muxes in frame. Channels idle, all 1. Subchannels from TGM to RLGM also 1. At least 2 subchannels from RLGM to TGM also 1.
2. Disturbance in link between muxes occurs so that RLGM loses frame.
3. RLGM puts out 11111 frame + channels and subchannels = 0.
4. RLGM gets this returned immediately, except that subchannels = 1, because TGM group has not yet detected any change.
5. RLGM can frame-in in 32 frames. (This is about the same for other muxes.) It frames on the subchannel, finding 1111 in the telemetry subchannel.
6. RLGM puts out 1010 frame + channels and subchannels = 0 because it has found 1111 and the data = 0 test is satisfied. Important: data = 0 is its own data returned.
7. Finally TGM detects the RLGM's change to 1111 (Step 3). This takes 32 to 35 frames. The TGM will now shut off the channels and subchannels, setting all to 0. However, it is too late, the RLGM has declared in-frame and is designed to withstand a drop-out.
8. Since the TGM is just now receiving 1010, the TGM will have the channels and subchannels set to 0 for only 32 frames. The RLGM easily withstands this interruption, as it is only 8 ms. The TGM goes back to turning the data on, which unfortunately includes the subchannel 1's as well as the looped channel 0's.

2.12 ANALOG ORDERWIRE LEVELS

Measurements were made on fully-equipped, full length cable systems of the loss in the analog orderwires. These showed less loss than previous

measurements. This is because in the fully equipped system, both coax shields and the overall shield are connected together at each equipment. (This improves the EMP and lightning protection considerably) At orderwire frequencies, not all the return current flows in the same coax as the outgoing current, so the effect of the other shields is to lower the total loss as compared to measurements taken with a single coax shield.

2.12.1 REPEATERED CABLE SYSTEM

The insertion loss of 40 miles of cable and repeaters was measured by first connecting the CDM's directly together and then through the cable system. Measurements were taken before the receiver AGC. The loss at 1000 cps was 38.2 dB. The loss at 1600 cps was 36.2 dB. Subsequent analysis has shown that the rise in frequency response is due to the addition of lumped capacitance at the repeaters. These measurements were taken at room temperature.

The CDM will provide a level out of the equipment side which is the result of the receive AGC amplifier. When the signal originates from another CDM, it will be in the AGC range, and the output will be a nominal -4 dBm. When the signal originates from a COU, it can be below the AGC range. Let us calculate this.

First we take the measured 0.98 dB per mile loss and increase it to 1.17 dB to provide for high temperature cable. The COU can be at most 39 miles away, giving 45.6 dB loss. The COU can apparently put out + 7 1/2 dBm with 6-volt batteries, giving an input to the CDM of -38.1 dBm. The gain of the CDM below the AGC range is 24 dB, so the CDM will put out -14.1 dBm on the equipment side.

Another result of the current flow in the other shields is near end crosstalk (NEXT) at orderwire frequencies. A test was made of this, and it was discovered that with the nominal signal coming out of the CDM, a return signal of -19.7 dBm was measured. This is within the AGC range of the CDM. This means that we have a 0 dB NEXT ratio. If it were not for the AGC amplifier, the incoming signal to NEXT ratio would be negative (in dB).

2.12.2 UNREPEATERED CABLE SYSTEM

Measurements were also made of the orderwire loss in this system. Here the cable does not behave like an attenuator, but more like a resistor. Therefore, the plot of dB loss vs. miles is not linear. See Fig. 2-31. The loss at 2 miles with correction for temperature is 9 1/2 dB.

When we include the losses in the resistive pads in the GM (31.75 dB), the total maximum loss is 41.25 dB. The nominal transmit signal (equipment side) of + 21.3 dBm will produce -19.95 dBm out of the receiver. Measurements of NEXT in this system show a return signal of -25.5 dBm, giving a NEXT ratio of 5.55 dB.

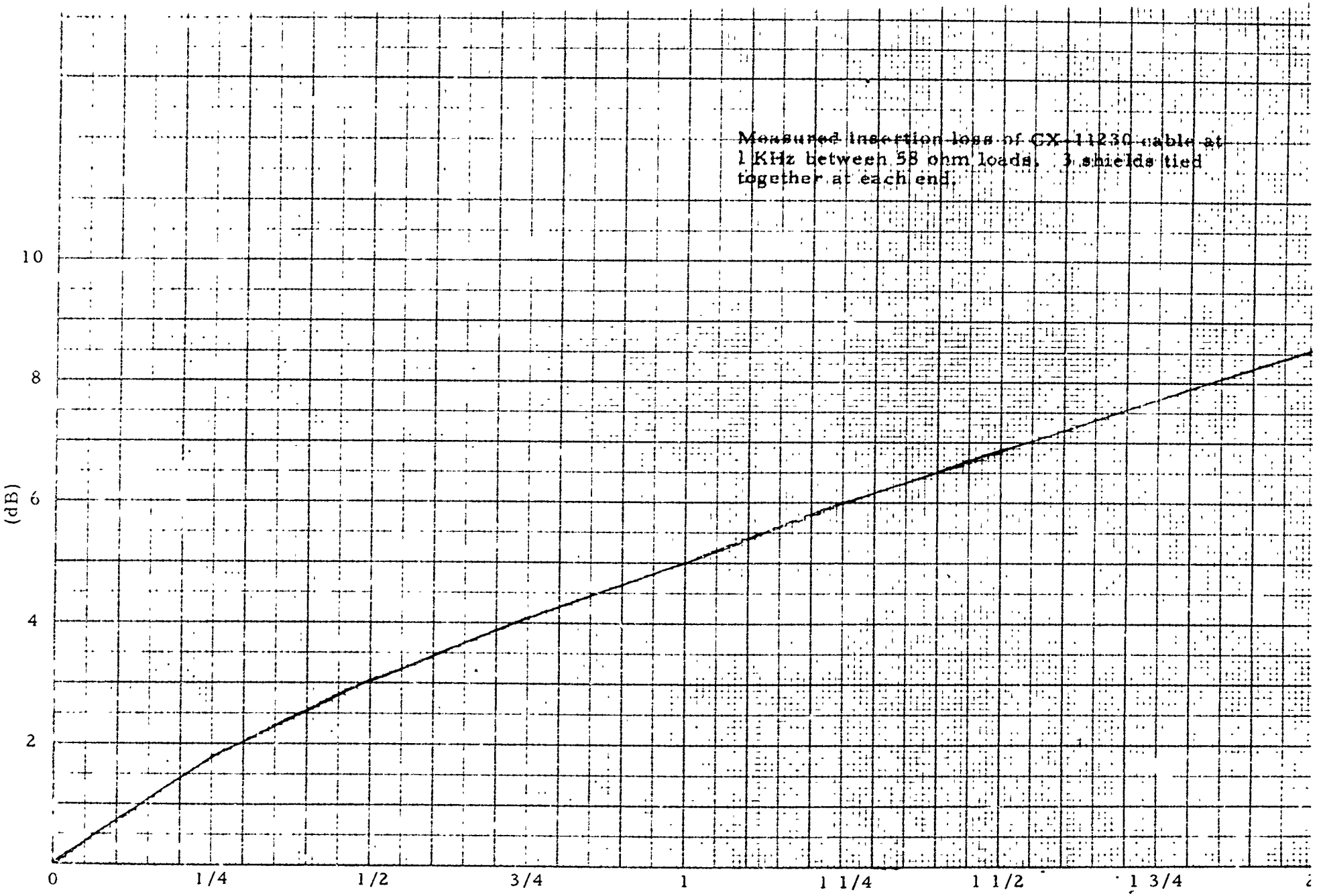


Figure 2-31 Measured Insertion Loss



SECTION 3

LGM

(See Sylvania writeup - Volume II).

SECTION 4
AN/GRC-103 MODEM

4.1 DESIGN GOALS AND REQUIREMENTS

The AN/GRC-103 Modem design approach outlined in Paragraph 4.2 and 4.3 meets the system goals of the Prime Item Development Specification 11400. This approach utilizes previous DGM and PCM design techniques to meet the unit functional requirements. Careful attention has been given, in the design and partitioning, to meet the encrypted frame operating requirements. Table 4.3-1 lists specific functional requirements.

On the equipment side, the AN/GRC-103 Modem can interface directly with the Multiplexer TD-1235( )/TCC, Multiplexer TD-1236( )/G, Multiplexer TD-1237( )/G, Diphase Digital Data Modem MD-1026( )(P)/G, Cable Driver Modem MD-1023( )/G and the Trunk Encryption Device (TED) KG-81. The digital orderwire interface is with the OCU. The analog orderwire and radio interface is with the AN/GRC-103 radio. Prime power is supplied from 115 $\pm$10% V, 47.5 to 420 Hz ac source.

4.2 AN/GRC-103 MODEM DESIGN APPROACH

The modem block diagrams and formats are presented in Figures 2.8-2 and 2.8-5. Two identical modem modules: with five printed circuit cards each, one BITE printed circuit card and a plug in power supply comprise a fully loaded AN/GRC-103 modem. Partitioning is provided to physically and electrically isolate the "RED" circuitry.

The modem power supply is identical to the MD-1026( )(P)/G supply and provides the $\pm$12 and $\pm$15 Vdc voltage required for internal operation.

4.3 DETAILED DESIGN DESCRIPTION

4.3.1 TRANSMIT TIMING CIRCUITS

Figure 4.3-1 illustrates the circuit design approach of the Transmit Timing circuits. This design provides basic timing and control signals required for both the RED and BLACK transmit portions of the AN/GRC-103 Modem.

Table 4.3-1. Modem Functional Requirements

Group Rates	128, 256, 288, 512, 576, 1024 and 1152 kb/s
Equipment Side Interface	Balanced NRZ and Timing
Radio Side Interface	Transmit-Unbalanced NRZ, ±10%, 2 Vp-p into 91 ohms, 640 or 1280 kb/s Receive Unbalanced NRZ 0.5 to 2 Vp-p into 91 ohms, 640 or 1280 kb/s
TED Interface	640 or 1280 kb/s Balanced NRZ and Timing
Frame Squelch	TTL
Digital Orderwire	16 kb/s and 2 kb/s Balanced NRZ and Timing
Analog Orderwire	Analog, Balanced 300 to 1700 Hz, Contact Closure
BLACK Station Clock	640 or 1280 kHz Balanced
Timing Options	From Internal Receiver. From Related Clock Timing Maintenance for 30 Milliseconds
BITE	Locates Equipment Faults to Single Replaceable Subassembly
Alarms	S, SA, RS Contact Closure
MTBF	4000 Hours
Power	115 Vac ±10%, 50 to 400 Hz, 85 Watts Maximum
Size	8-1/2H X 12D X 19-Inch W, Rack Mount
Weight	15 KG Maximum

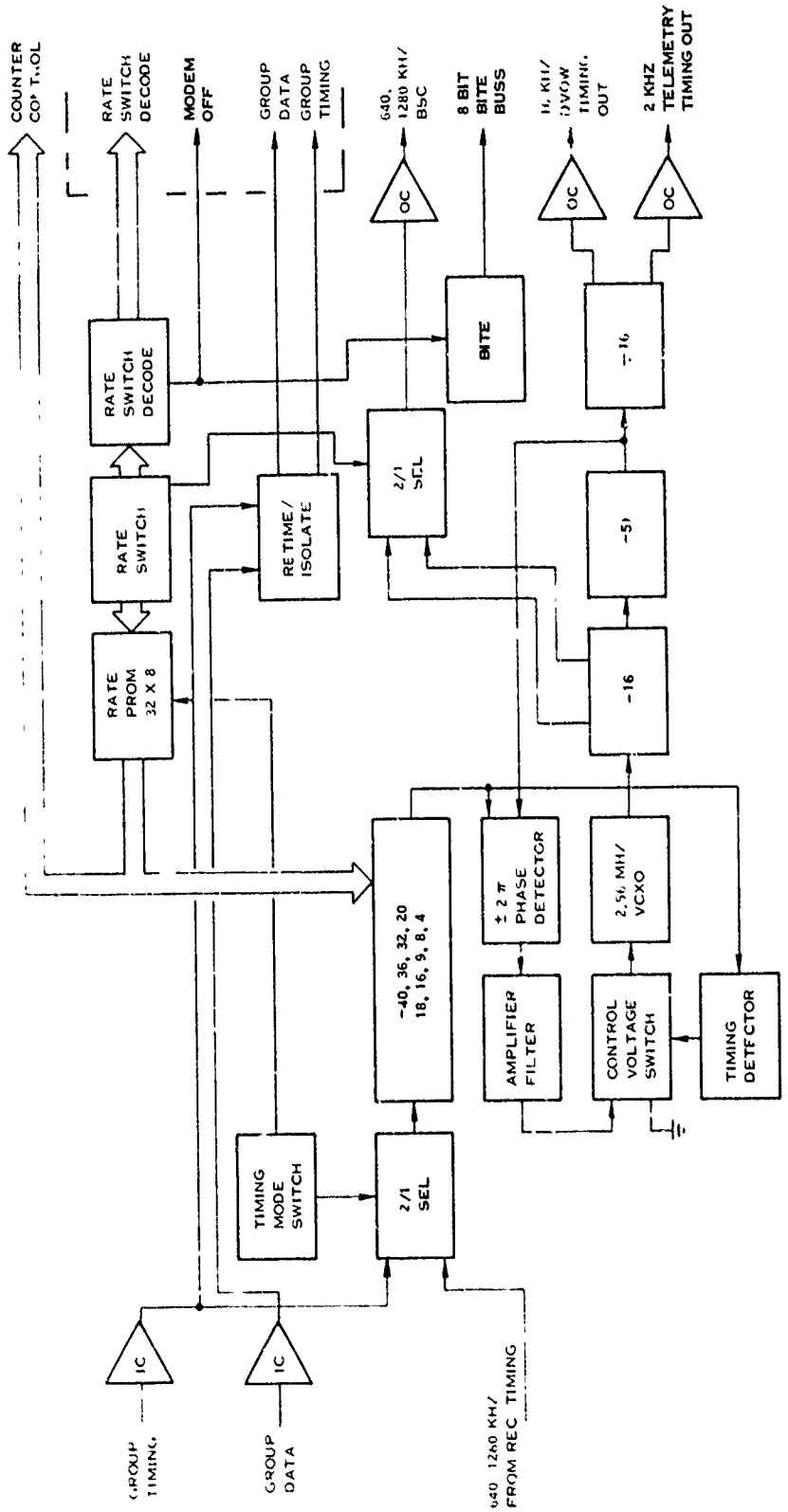


Figure 4.3-1. Transmit Timing Circuits

The 640 or 1280 KHz BSC signal may be derived from two (2) sources: the related group timing or the 640, 1280 KHz looped timing from the modem receive circuits. Two timing mode switches, located on the printed circuit board, select the desired operating mode. All modes provide maximum protection against contamination by the "RED" frame and format signals.

The received 640/1280 KHz signal is derived from the received radio signal. As this signal has encrypted frame, the regenerated timing is "clean". The related group timing signal is BLACK but is also inputted to the RED circuits. A buffer isolates the group timing signal used for generation of the BSC. Note that in the group timing mode, the design approach does not use any signals from the MUX buffer for locking the PLL. Therefore, the buffer occupancy does not "center" automatically and reset circuitry is required. As reset circuitry is required for the other timing modes, there is no circuitry penalty.

Under control of the thumbwheel rate switch, located on the PCB, the selected timing source is divided down to a 32 kHz rate. This is the maximum frequency common to all source rates and is the reference for the 2.56 MHz PLL. The desired characteristics for the PLL are: high dc gain, a $\pm$15 PPM stability VCXO, sufficient capture range for a $\pm$47 PPM MGM offset plus the $\pm$15 PPM VCXO stability, and narrow bandwidth to reduce the MGM jitter.

A high dc gain is required to minimize the timing phase shifts at the "RED" group data buffer. Since the PLL reference is at 32 kHz, a small phase shift at the phase detector is multiplied (percentage wise) by the group rate divided by 32 kHz. For the worst case 1152 kHz group rate the factor is 36. Therefore, for example, if the PLL requires a phase change of $\pm 30^{\circ}$ to satisfy all lock-in conditions, the phase shift at the RED buffer would be $\pm 1080^{\circ}$ or $\pm$3 bits. This could cause unnecessary resets of the buffer (especially if the buffer size is limited) with the MGM and with temperature variations. Unfortunately, a large dc gain gives large PLL bandwidth. However, the bandwidth can be reduced with a filter. With some phase detectors, the $\pm\pi/2$ or $\pm$ types, the filter also reduces the capture range of the PLL.

The phase detector chosen for this design is the $\pm 2\pi$ (or phase frequency) type. With this type, the PLL can be designed to maintain an adequate capture range with large dc gains and filtering to provide the desired PLL bandwidth. Therefore, the PLL bandwidth will be minimized, as consistent with the overall system response times. The VCXO is specified to provide ± 15 PPM stability as well as a ± 62 PPM minimum pull in range. A 2.56 MHz frequency was chosen in order to generate accurate complimentary squarewaves at the 1280 kHz rate. These are necessary for internal circuitry only. VCXO's meeting the above specifications have been procured and are working properly.

The programmable counters are under control of the 32 x 8 PROM which decodes the PCB RATE switch, and the Timing Mode switches. This provides for division of the selected timing signal by 4, 8, 9, 16, 18, 20, 32, 36, or 40 as required, to generate the 32 kHz reference. The rate switch is identical to other DGM equipments and settings will be according to DGM standards as listed below.

Rate (kHz)	Rate Switch Setting
1152	9
1024	8
576	7
512	6
288	5
256	4
128	2

Also, rate switch position 0 shuts that modem off. The modem off signal then inhibits bite indications on all five modem CCAs. The 2.56 MHz PLL provides the 640/1280 kHz BSC and the 16 kHz DVOW signal at standard DGM output levels. Signals to the "RED" circuits are the group data (isolated by retiming) and the counter control signals. As the latter signals are static dc levels, no additional buffering is required.

4.3.2 MUX CIRCUITS

These circuits provide the formatting of the group data, auto-phasing of the DVOW and Telemetry data, and multiplexing of these signals with the fill and frame pattern. To minimize RED signal modulation of critical outputs, these circuits are physically and electrically isolated from the Transmit Timing circuits. Figure 4.3-2 shows the MUX circuits.

The clocks required to implement the formats shown in Figure 2.8-5 are generated from the 640 or 1280 kHz RSC input. A programmable ÷20 or ÷40 counter provides the addressing for the format PROM. Both the counter and PROM are under control of the Transmit Timing circuits RATE switch. The format PROM provides addressing for the multiplexer as well as controlling the format clock generator. The output of the format clock generator is derived from the RSC input and contains gaps corresponding to the DVOW, Telemetry, fill and frame time slots. Additionally, for the 288, 256 and 128 kb/s rates, clock-pulses are regularly deleted (every second or fourth). This provides a formatted clock input, at the exact group rate, to read out the 64 x 1 FIFO buffer. The input to the FIFO buffer is the continuous group data and timing signals from the Transmit Timing circuits. The occupancy of the FIFO is monitored and a reset is generated whenever an underflow, or overflow condition occurs. This effectively sets the FIFO half full. With the reset approach, a 64 x 1 FIFO allows an approximate maximum of 32 bits occupancy variations within the buffer. This greatly exceeds the maximum 5-bit format gap plus the maximum 4-bit MGM jitter. The formatted data and its compliment are applied to the multiplexer.

The Telemetry data signal is synchronous with the modem timing. However the phasing of this data is arbitrary and an automatic phase circuit is required. Basically, this circuit resamples the data with an internal clock at the data rate. If the data transitions are too close to the internal clock, another phase of the internal clock is selected. Either clock phase gives correctly resampled data properly phased for the multiplexer circuits. Before the Telemetry data is multiplexed, it is exclusive-or modulated with an 8 kHz clock signal. This clock signal is phased so that it is set low at the transitions of the resampled Telemetry data.

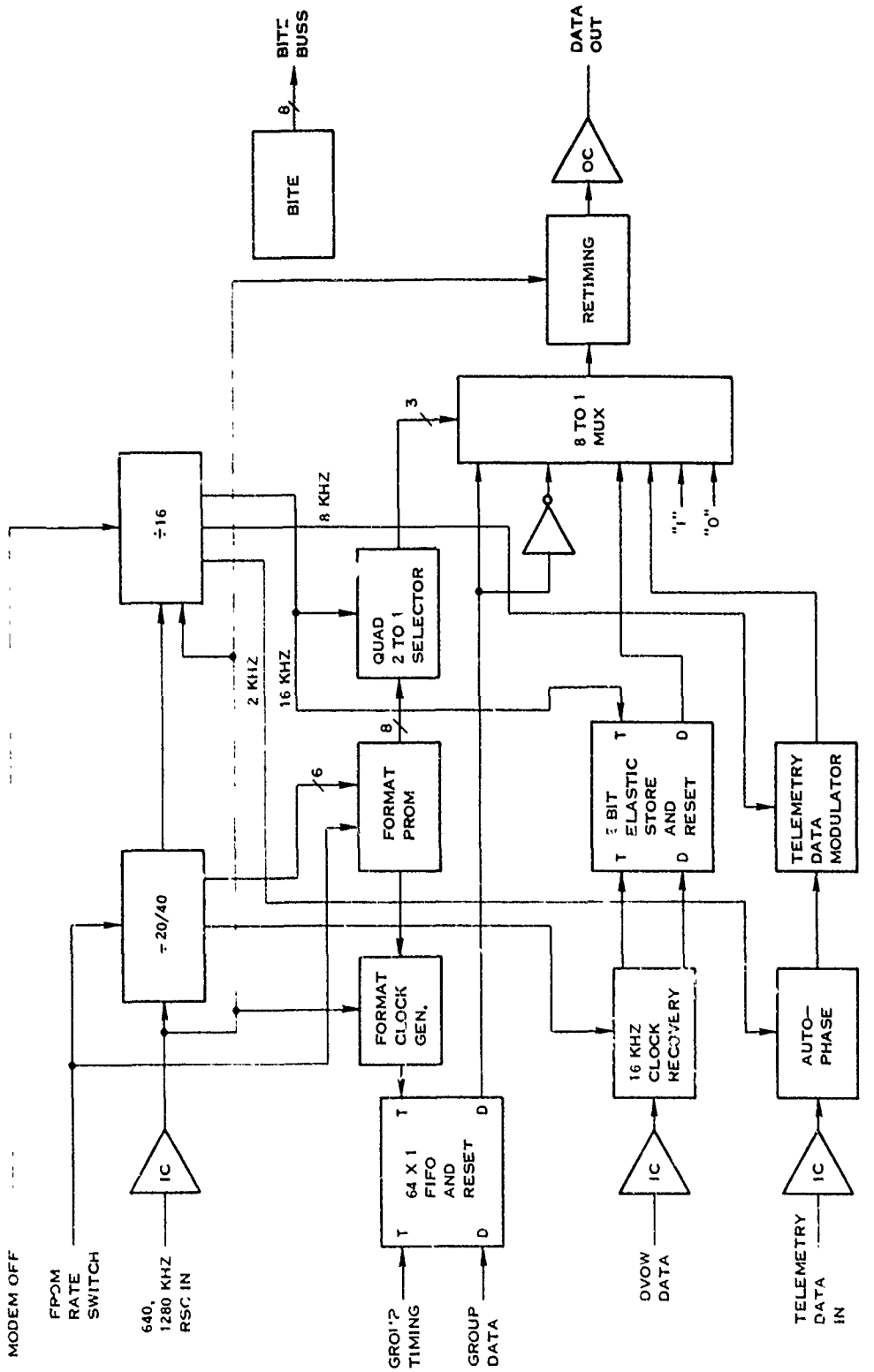


Figure 4.3-2. MUX Circuits

The DVOW data signal is also synchronous, however, it may contain jitter that exceeds the range of an autophase circuit. This jitter would cause continuous switching of the internal clock phase, and resultant data errors. To avoid this problem, a 2-bit elastic store buffers the DVOW data. As this requires a clock to read in the DVOW data, a 16 kHz clock is derived from the input data. The elastic store has reset circuitry which monitors the store occupancy. Whenever a limit condition exists, the store occupancy is reset. This circuit will accommodate the expected $\pm 1/2$ bit maximum jitter. The retimed DVOW data is also applied to the multiplexer circuits.

The multiplexer is under control of a three line address generated by the format PROM and Quad 2 to 1 selector. This allows the formatted data, its compliment, resampled DVOW data, resampled and modulated Telemetry data, or a 1 or 0 to be selected according to the required format. The multiplexed data is retimed and outputted as 640 or 1280 kb/s RED data.

4.3.3 TRANSMIT BUFFER CIRCUITS

The transmit buffer circuits (Figure 4.3-3) simply receives the encrypted (from the TED) or unencrypted (from the RED data output) 640 or 1280 kb/s data and converts it to interface levels compatible with the radio. The To Radio signal is NRZ binary data, two volts peak-to-peak (into 91 ohms) with rise and fall times of 160 to 280 ns. These circuits are mounted in a separate compartment with integral transmit coaxial connectors. The BITE detector outputs are applied to these respective Radio Regenerator circuits where a separate LED provides the fault indication.

4.3.4 RADIO REGENERATOR CIRCUITS

These circuits accept the 640 kb/s binary or 1280 kb/s biternary baseband radio signal (plus analog orderwire), recovers the timing and regenerates the original binary data signal. Additionally the analog orderwire is separated from the data and applied to the radio. For poor S/N radio signals, an RS alarm is generated, and an Orderwire Control signal enables orderwire recovery at the Radio. When the modem is out of frame, a Frame Search Inhibit signal is generated. Figure 4.3-4 is a detailed block diagram of the radio regenerator circuits.

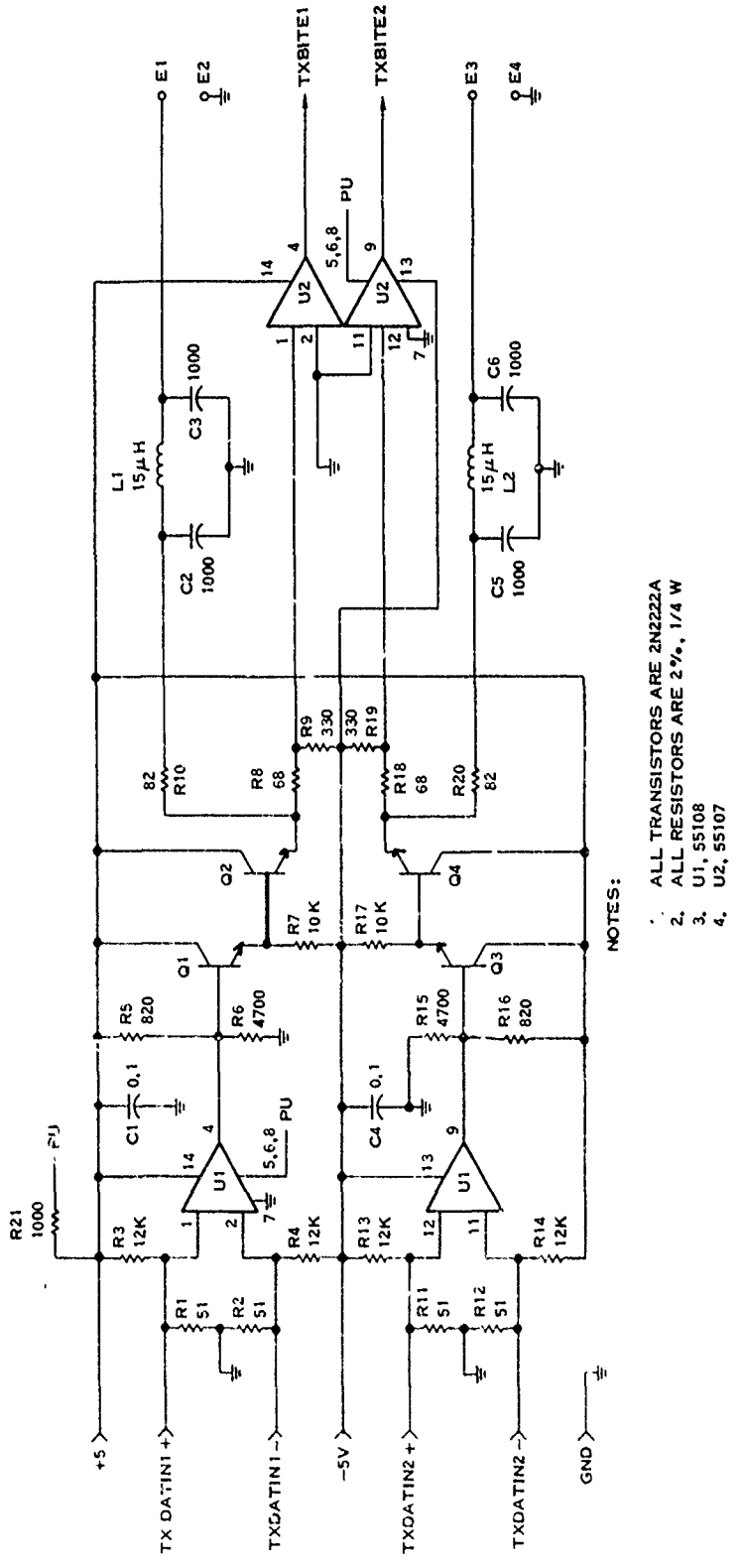


Figure 4.3-2. Transmit Buffer Circuits

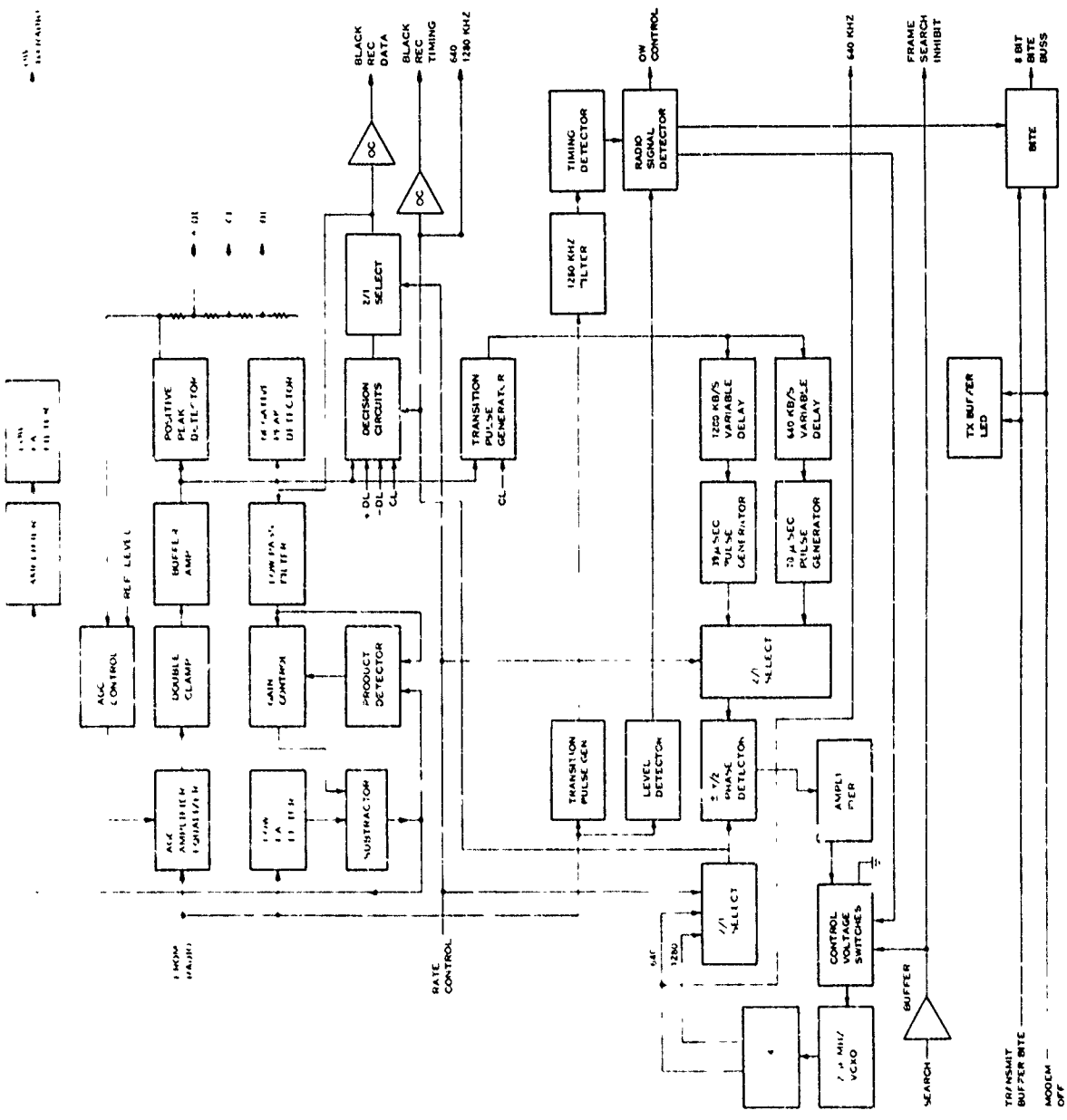


Figure 4.3-4. Radio Regenerator Circuits

The 0.5 to 2.0 volt from radio signal is first amplified to approximately three volts peak-to-peak. Therefore, the AGC controls the voltage gain of this stage from 1.5 to 6. Also the amplifier provides additional high frequency "boost" to properly equalize the data signal. This is required as the normal Gaussian radio response is optimized for the 576 and 1152 kb/s rates. A single pole network is sufficient to approximate an overall Gaussian response for the 640 and 1280 kb/s rates. A wideband op amp with feedback controlled gain and a FET AGC provides the AGC amplifier function. A LF-157 type op amp has both the necessary bandwidth and slew rate for this application. The AGC control maintains the output of the positive peak detector at the reference level of +1.5 volts.

Before the equalized radio signal is applied to the regenerator circuits, the analog orderwire signal is removed by the double clamp. This type of circuit has been proven effective in the TD-202 Combiner A, for removing analog orderwire up to 30 percent of the digital signal. While the clamp is effective, some residual orderwire is present and previous experience indicates the biternary S/N performance is reduced by approximately 1.5 dB. The buffered output of the clamp is applied to the positive and negative peak detector circuits, the decision circuit and the transition pulse generator circuits. The peak detector circuits provide positive and negative dc voltages equal to the peaks of the signals. Resistor dividers then derive the biternary plus and minus decision levels and the center level. Note that the AGC control maintains the positive peak equal to the reference voltage. Therefore, with noise on the signal, the AGC tends to maintain the noise peaks at the reference level. To obtain optimum S/N performance in biternary operation the decision levels must be predistorted to compensate for this effect. Note that predistorted decision levels are not unique to an AGC approach, but is inherent with the peak detectors themselves. As the levels are experimentally optimized with noise, there is no real performance degradation. Past biternary designs have given decision levels that were very close to the predicted predistorted values of one-third the peak voltages.

Before the data can be regenerated, the 640 or 1280 kb/s timing must be extracted from the data transitions. Pulses are generated from the data crossings and applied to two precision variable delay circuits. These circuits adjust the phase of the sampling timing, with respect to the clamped radio signal, to the optimum position. A 54LS221 precision dual one shot provides these delays with excellent stability. The trailing edge of the delay circuits is then used to generate half-width pulses; 39 and 78 μs for the 1280 and 640 kb/s rates, respectively. Therefore, these circuits have converted the data transitions into half-width pulses. The rate switch selects the appropriate half-width pulses and clock output applied to the PLL phase detector.

The receive regenerator PLL utilizes the same VCXO as the Transmit Timing circuits. However, the desired loop characteristics are different. A high dc gain is desirable to minimize the phase shift of the recovered timing, but it is not possible, or desirable to appreciably narrow the loop bandwidth. Due to the randomness of the data, half-width pulses are generated randomly at integral multiples of the data period. Only the $\pm\pi/2$ type phase detector, using a filter to reduce loop bandwidth does reduce the capture range. Fortunately, a wider bandwidth is desirable as this allows the sampling clock to "track" jitter on the radio signal. With the high gain, this maintains the sampling point at the optimum position for any lower frequency jitter on the radio signal. Therefore, no loop filtering is used.

To determine the quality of the received radio signal, transition pulses are generated directly from the radio input. With a good signal, these pulses, when bandpass filtered, give a 1280 KHz sinewave signal with little AM. This is detected and controls the RS detector. The RS signal detector will alarm when the bit error rate (binary and biternary) exceeds approximately 10^{-2}. Additionally, the level of the radio signal is monitored. Therefore, when the radio signal S/N is poor, or if the radio signal fails, an RS alarm condition is declared. This activates the OW control relay contacts and the BITE card RS alarm contacts. The RS signal detector will alarm when the bit error rate (binary and biternary) exceeds approximately 10^{-2}. Additionally the last VCXO control voltage is maintained for at least 30 ms. As the PLL is still in lock at the threshold S/N (the PLL lock is quite rugged), this provides receive clocks at $\pm$15 PPM stability as long as the poor S/N or no signal condition persists.

In normal operation, the locked 640 or 1280 kHz timing is applied to the decision circuits. For binary signals (640 kb/s) the data is sampled at approximately the center of the binary "eye". If the signal is above the center level it is a logic 1, below a logic zero. For the biternary case (1280 kb/s) the data is sampled at approximately the transition times. The decision logic is slightly more complicated, but is easily implemented with a JK type flip-flop. If the signal is above the +DL, it is a logic 1, below the -DL it is a logic 0. However, if the signal is between levels, the last decision is complimented. The Rate Control switch selects the appropriate decision circuit output, and this regenerated data is outputted, with the sample clock as Receive Data and Receive Timing. Additionally, the 640 or 1280 kHz timing signal is used by the Receive Timing circuits and outputted as BSC 1. A 640 kHz Timing signal is also applied to the Receive Timing circuits.

As shown, the orderwire recovery circuits are relatively complicated, however other techniques give poor audio quality. With simple low-pass filtering, the low frequency content of the data signal is audible. Likewise, the limitations of the double clamp, while acceptable for data recovery, does not give good quality audio by simple subtraction of the clamp output from the input. The approach shown is conceptually identical to the TD-202 Combiner A. Essentially the recovered data is subtracted from the input radio signal giving the resultant orderwire signal. As only the low frequency energy of the data signal is a problem, both signals are first low pass filtered. Additionally, the regenerated data is passed through a gain controlled amplifier. In this manner, the input to the subtractor can be adjusted to reduce the residual low frequency data on the orderwire to virtually zero. An analog multiplier multiplies the subtractor output with the regenerated data. As noise and the orderwire signal do not correlate with the data, their net product is zero. The product detector output adjusts the level of the regenerated data to minimize the residual data on the orderwire signal. This technique gives better than the required 20 dB "clean up" of the orderwire signal. The orderwire signal is amplified and filtered before being outputted to the radio at a -4 dBm level.



However, with poor data S/N ratios, data errors introduce noise in this type of recovery circuit. Therefore, when this condition is sensed, orderwire recovery is automatically transferred back to the radio.

The Frame Search Inhibit is just the buffered search signal from the MUX circuits. This inhibits frame search of other equipments whenever the AN/GRC-103 Modem is out of frame.

4.3.5 RECEIVE TIMING

The Receive Timing circuits are shown in Figure 4.3-5. Again, the main feature of the design is generation of the appropriate group DVOW and Telemetry timings from only black signals. All necessary timing signals are derived from an 8192/9216 kHz PLL. The 64 kHz reference for this loop is derived by dividing by 10, the 640 kHz timing recovered from the BLACK frame radio signal. The 64 kHz controlled clock is either (depending on the group rate) the 8192 or 9216 kHz VCXO output divided by 128 or 144, respectively. Desirable characteristics for this PLL are large dc gain and narrow bandwidth. Stability is not critical, as during an outage the ± 15 PPM requirement is maintained by the regenerator VCXO supplying the reference. A $\pm 2\pi$ type phase detector with a loop filter gives a PLL with the desired characteristics. However, Paragraph 3.2.1.5 of the specification 11400 limits the bandwidth of the PLL. This spec includes the lock time of the loop as well as the frame in time of the modem. This should limit the loop bandwidth to approximately 25 Hz.

A $\div 16$ counter, four to one selector controlled by the rate switch, and a $\div 4$ counter provide the appropriate group rate clock. This signal is used to re-time the group data from the DEMUX circuits; and is outputted as the BSC and Group Timing signals. It is also applied, through a buffer to provide isolation, to the DEMUX circuits. A buffered 16 kHz signal is also applied to the DEMUX circuits. The Resync pulse circuits generate 20 μs pulses from the resync trigger signal supplied by the DEMUX circuits. When the modem is out of frame, resync pulses are generated every 62 ms.

Figure 4.3-6 is a block diagram of the DEMUX Timing circuits. These circuits find the frame pattern, demultiplex the data, demodulate the Group and Telemetry signals and provide the three data signals. Only the Telemetry and clock output directly to the equipment side.

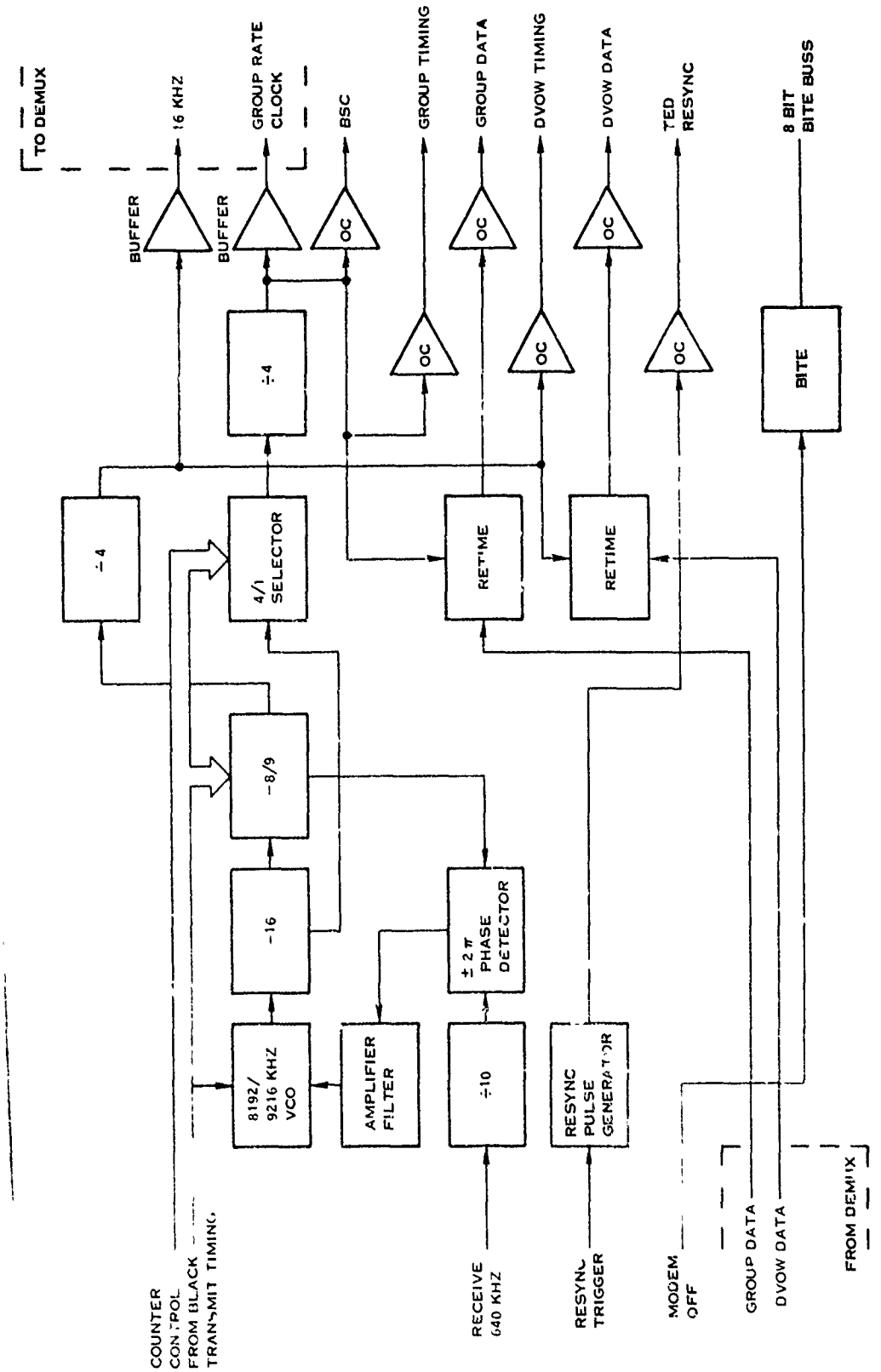


Figure 4.3-5. Receive Timing Circuits

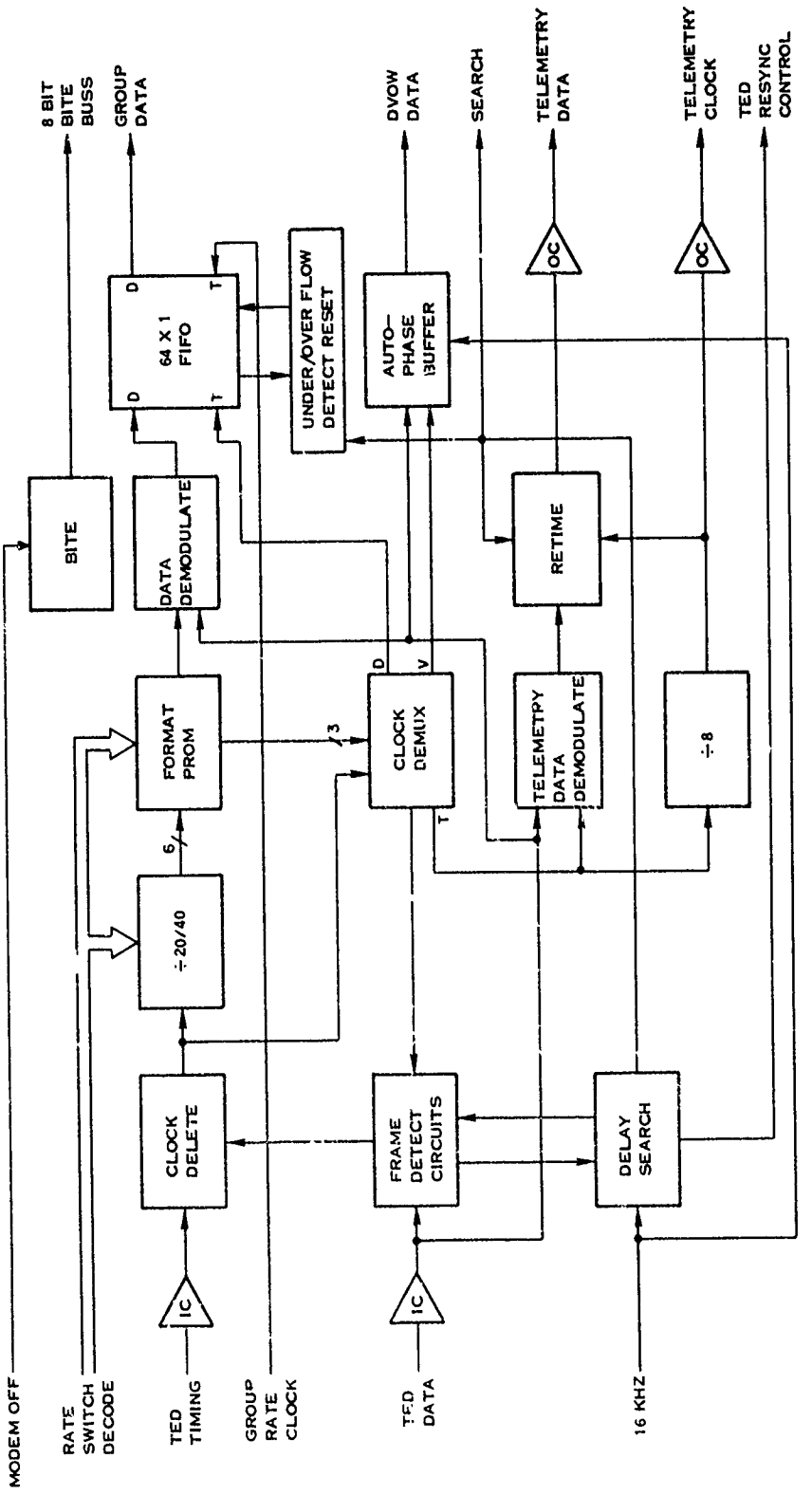


Figure 4.3-6. DEMUX Circuits

Data and Timing is applied from either the TED (encyrpted frame) or the data regenerator (unencrypted frame). In either case, the 640 or 1280 kHz timing is applied to a clock delete circuit, which during frame search, deleted one pulse at a time. The clock output is applied to a ÷20/40 counter and the clock demux. This counter, controlled by the XMT TIM rate switch, divides the input clock by 20 or 40 depending on the format. The outputs of the counter, plus static rate control signals, address the format PROM. This PROM provides signals to the clock demux circuits which with the clock signal, generates the group, DVOW, Telemetry and frame clock pulses according to the unique format for each rate. The assumed frame clock is applied to the frame detect circuits which examine the input data, according to the rate, for the 1, 0 or 111,000 frame. When lock is achieved, the four clocks from the clock demux align with the corresponding data bits in the format.

When lock is lost, the delay search circuits provide a 30 ms delay before returning to the search mode. This allows BCI to be maintained for the required 30 ms. If lock is not reachieved during this interval, frame search is enabled. Additionally, the TED resync control signal then enables TED resync pulses (from the receive timing circuits) to be sent every 62 ms.

The group data is first demodulated to remove the alternate data polarity inversion and applied to a 64 x 1 FIFO. This data is entered into the FIFO with the group clock signal from the clock demux. Data is read out of the FIFO with the group rate clock generated in the receive timing circuits. As in the MUX the FIFO must have reset circuitry to avoid overflow or underflow. The FIFO is initialized to one-half full by the lock signal. Normally, this should prevent overflow or underflow of the FIFO. However, to further insure this protection, the occupancy of the FIFO is also monitored continuously. If a limit condition exists, the FIFO is then again set to one-half occupancy. The group data output is then sent to the receive timing circuits.

The Telemetry data is demultiplexed and demodulated from the 640/1280 kb/s data with a 16 kHz clock from the clock demux circuits. This clock is also applied to a ÷8 counter. The 2 kb/s demodulated data is then retimed with the ÷8 counter 2 kHz squarewave output. The retimed Telemetry data and clock are outputted at standard DGM levels, when out of lock, the data is set to all "ones".

4.3.7 BITE

The AN/GRC-103 Modem used the identical BITE approach and printed circuit board developed during the DGM programs. However, to meet the specific unit BITE functions, a new PROM coding was necessary. Provision is made to suppress false BITE indications when only one modem module is in operation, or if only one modem module is in the unit. The BITE approach and design is discussed in detail in Paragraph 20.

4.3.8 HFE

The 103 Modem design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are incorporated onto the accessible edge of the PCB's. These controls are protected by the front panel cover. No controls are located on the RED PCB's. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connectors are located on the rear of the case and are positioned to ensure maximum accessibility. The unit case is shown in Figure 15.1.8-1. The rear panel layout is shown in Figure 15.1.8-2.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472.

4.3.9 RELIABILITY DESIGN

The AN/GRC-103 Modem has a specified MTBF of 4000 hours. This is equivalent to 250 failures in 10^6 hours. The reliability prediction and the demonstrated results are summarized in Table 4.3-2.

Table 4.3-2

AN/GRC-103 Modem
RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
4000	7974	4391

SECTION 5

RLGM

(See Sylvania writeup - Volume II).

SECTION 6
RLGM/CD

The Remote Loop Group Multiplexer Cable Driver (RLGM/CD) is required to carry traffic at either 72 kbp/s or 144 kbp/s. The cable modulation is conditioned diphase, and is transmitted down CX-11230 cable at lengths up to 3.2 km. The RLGM/CD provides power via the cable to operate an RLGM and its associated DSVT's. Maintenance orderwire is provided along with the line side signals and it terminates in the COU.

6.1 DESIGN GOALS AND REQUIREMENTS

RLGM/CD function requirements are summarized in Table 6-1. The RLGM/CD handles traffic at 72 kbp/s or 144 kbp/s. Balanced NRZ and timing signals are accepted at the equipment side, and are converted to unbalanced conditioned diphase for transmission over up to 3.2 km of CX-11230 cable. Power for the RLGM is also applied to the cable as 180 Vdc at 0.300 amperes. Maintenance orderwire is also accepted balanced at the equipment side.

6.2 DESIGN APPROACH

The original concept of the RLGM/CD was to have a five inch high case containing one power supply and one cable driver modem card. The approach taken is a dual RLGM/CD (see Figure 6-1) in a full size case. This approach allows the use of a standard size DGM case and standard size DGM panels. Each cable driver and the cable interface will occupy a standard size panel and a fourth card, the BITE panel, will be the same common panel used in other units.

The RLGM/CD uses the same power feed circuit as the RMC so that both will present the same interface to the RLGM.

TABLE 6-1

DUAL RLGM CABLE DRIVER FUNCTIONAL REQUIREMENTS

Function	Requirement	Specification
Size	19-inch-rack mounting 12 inches deep, maximum 8.5 inches high, maximum	SCL-1280(3.3.3) (3.2.2.4)
Weight	Not to exceed 15 kilograms	(3.2.2.4.2)
Prime Power	ac or dc input Not to exceed 200 watts	(3.2.1.4.4)
Power Feed	Power for all functions of RLGM including DSVT power feed	(3.2.1.4.4.1)
Maintenance Orderwire	Passive 300 - 3400 Hz analog voice	(3.1.2.8.2)
Reliability	MTBF - 4000 hours	(3.2.3.1)
Environment	Temperature (-25°F to +145°F) humidity, altitude, dust, salt fog, fungus, vibration and shock	(3.2.5.1)
EMC	Tests for modems of MIL-STD-461	(3.3.2.2)
Nuclear	Section 30 of TT-B1-3001-0011 except 30.2.4.1.1 and 30.2.4.1.2	(3.3.8.2)

6.3 DETAILED DESIGN DESCRIPTION

6.3.1 RLGM/CD TRANSMIT SIDE

Equipment side inputs to the RLGM/CD are balanced NRZ data and related timing. Balanced inputs are terminated in 100 ohms. Figure 6-2 shows a block diagram of the RLGM/CD. Interface circuits are described in Section 2.7 for equipment side signals.

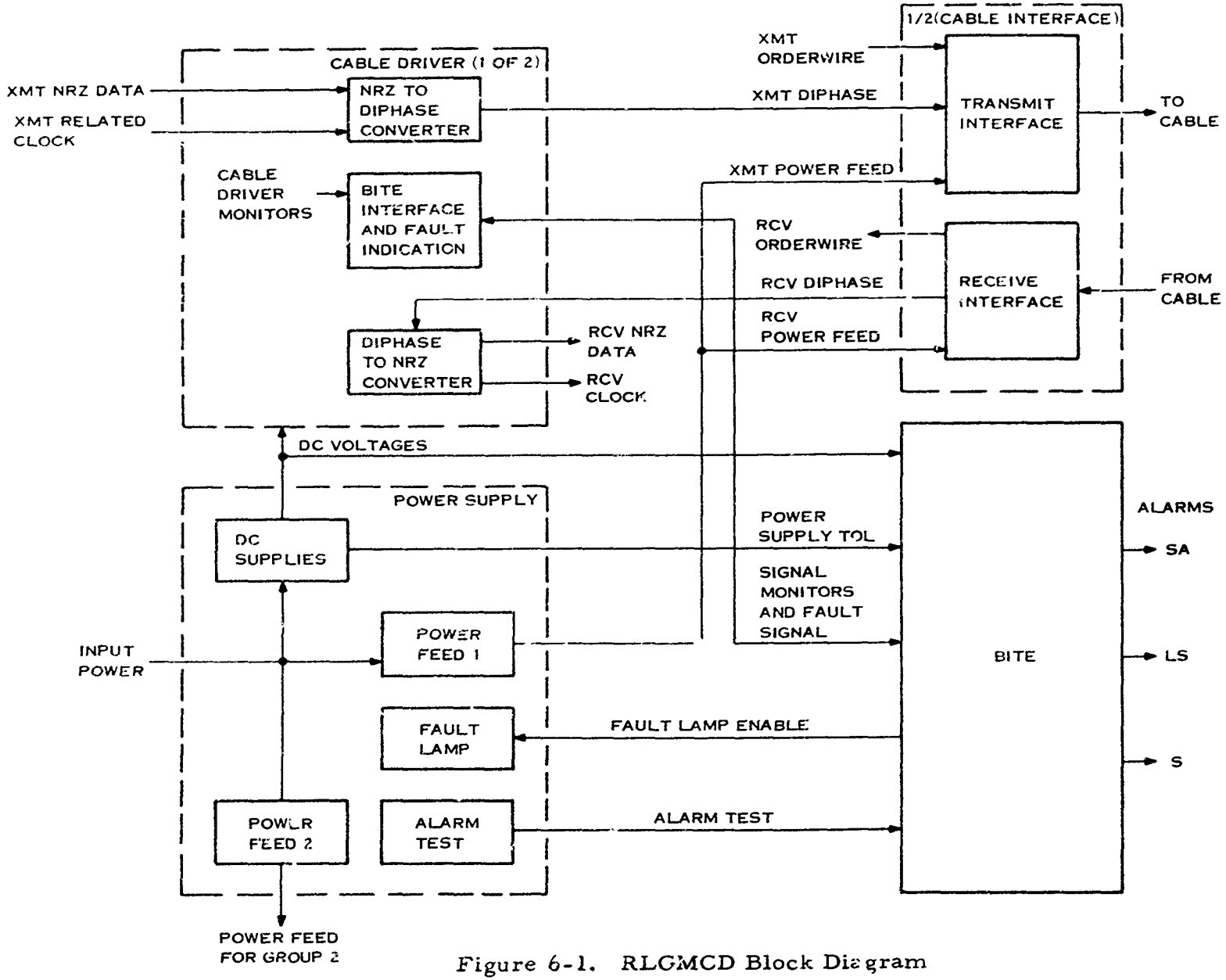


Figure 6-1. RLGMCD Block Diagram

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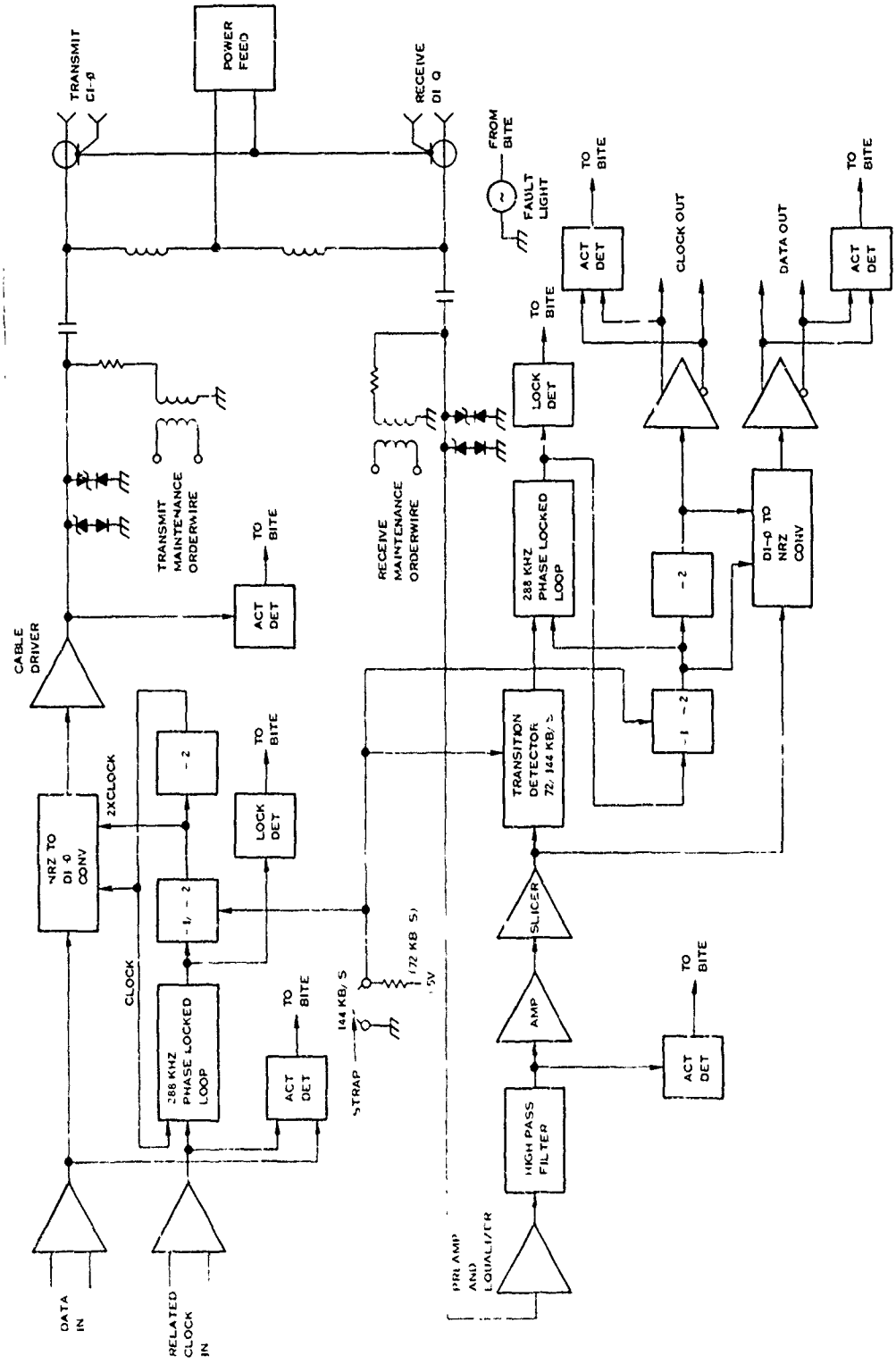
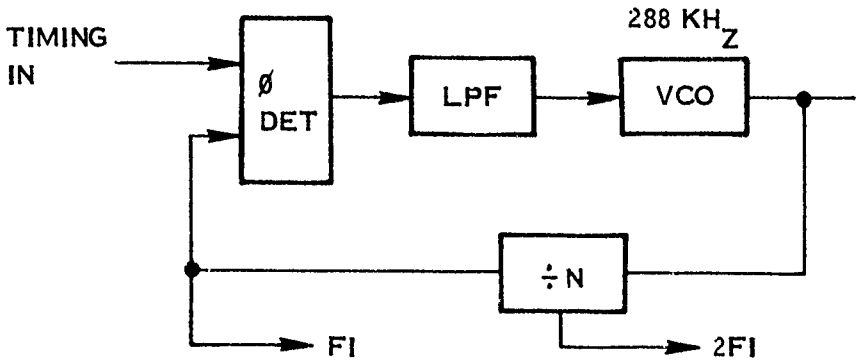


Figure 6-2. RLGM/CD Detailed Block Diagram

The clock is fed into an X2 multiplier employing a phase-locked loop (see Figure 6-3), since a clock at twice the data rate is required to convert binary to conditioned diphase. A strap controlled gate selects the correct phase-locked loop frequency divider for generating the binary-to-diphase conversion clocks for each data gate. The data, the clock, and the 2X clock are then fed into a binary to diphase converter (see Figure 6-4). The conditioned diphase out of the converter is applied to a cable driver. The driver consists of active components and presents a constant output impedance to data as well as to audio frequencies. The driver is isolated from the power feed by a blocking capacitor.



FIN	N
72	4
144	2

Figure 6-3. X2 Multiplier

6.3.2 RLGM/CD RECEIVE SIDE

The CX-11230 cable attenuation between 72 kHz and 144 kHz is fairly flat. The attenuation for 3.2 km at 144 kHz is approximately 18 dB and is about 17 dB at 72 kHz. The cable receiver will restore the signal to approximately 2 V p-p for use in timing recovery and data detection.

The cable will be equalized for maximum length. At shorter lengths, the resulting overshoot will be clipped off and the signal will be sliced around the center.

Figure 6-2 shows the block diagram of the receive side. The signal from the cable is ac coupled to the preamplifier and equalizer through a blocking capacitor. The equalized signal is filtered in a high pass filter to remove the analog

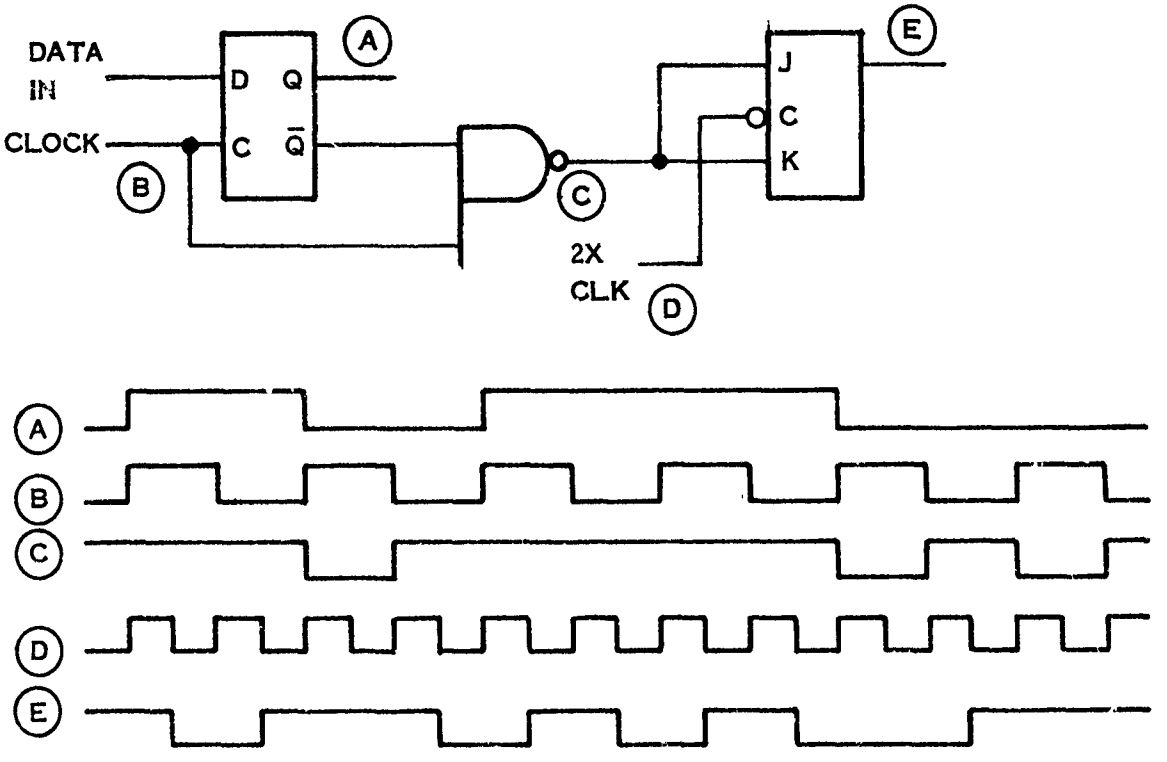


Figure 6-4. Binary to Diphase Converter

orderwire. The signal is then amplified, sliced, and sent to the timing recovery circuit.

The timing recovery circuit is a phase-locked loop consisting of a voltage controlled oscillator (VCO) locked to the received data transitions at a 90-degree phase angle at center frequency. The transitions are made in the transition detector which consists of one-shots generating pulses for each positive and negative transition of the diphase data. The pulses sent to the phase-locked loop are equal in width to approximately one-half of the diphase data pulse. Since both data rates require different width transition pulses, each data rate employs separate one-shots. The proper pulsewidth output is selected through a selector gate controlled by an external strap. An exclusive OR phase detector in the phase-locked loop

compares the data transitions to the VCO timing transitions. At center frequency, the data and VCO timing transitions are at a 90-degree phase angle and the phase detector output pulses are one-half the width of the input pulses. Any positive or negative offset from the center frequency proportionately increases or decreases the width of the phase detector output pulses. The output pulses are filtered to give the control voltage to the VCO. The VCO output is either left alone or divided by two, depending upon the data rate (see Figure 6-5). The 72 or 144 Kb data rate will be a strap option depending on a 16 or 32 Kb DSUT rate.

The diphase data from the preamplifier is sampled twice per bit by the 2X clock produced in the timing recovery circuit. Interference from noise or crosstalk on the shielded cable has been estimated to be at least 20 dB below the diphase signal level.

The signal out of the amplifier is sliced by a comparator referenced to 0 volt. The resultant logic level is strobed into a diphase to binary converter by the rising edge of the 2X clock (see Figure 6-6). The converter consists of a

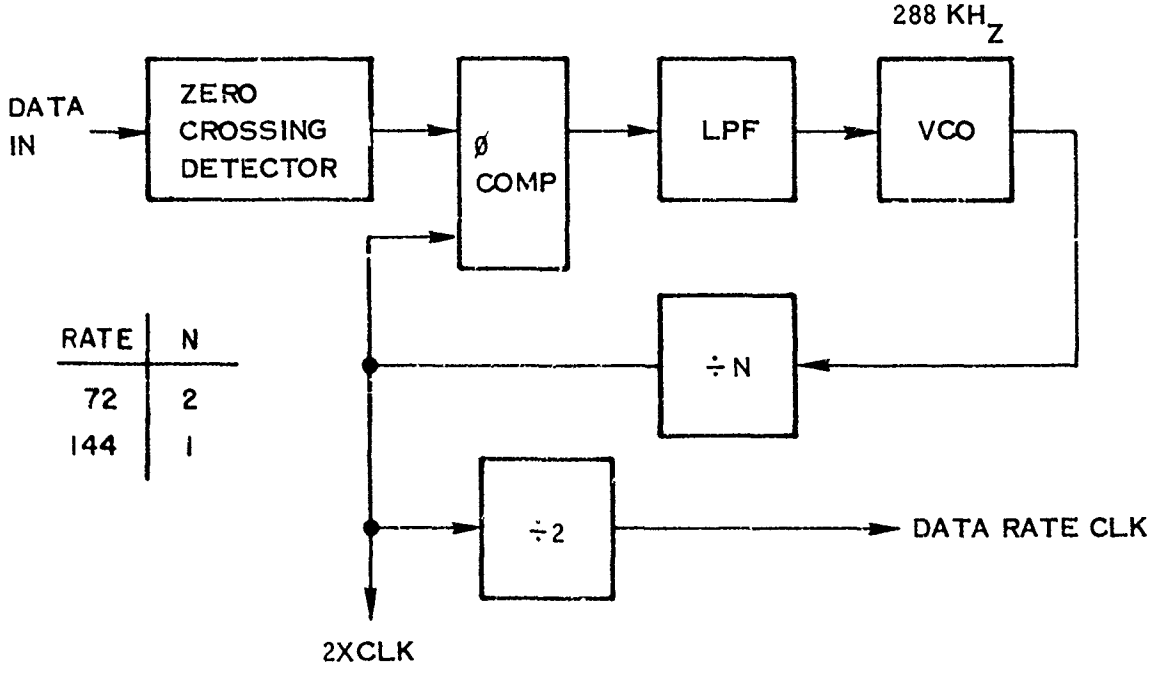


Figure 6-5. Clock Recovery Loop

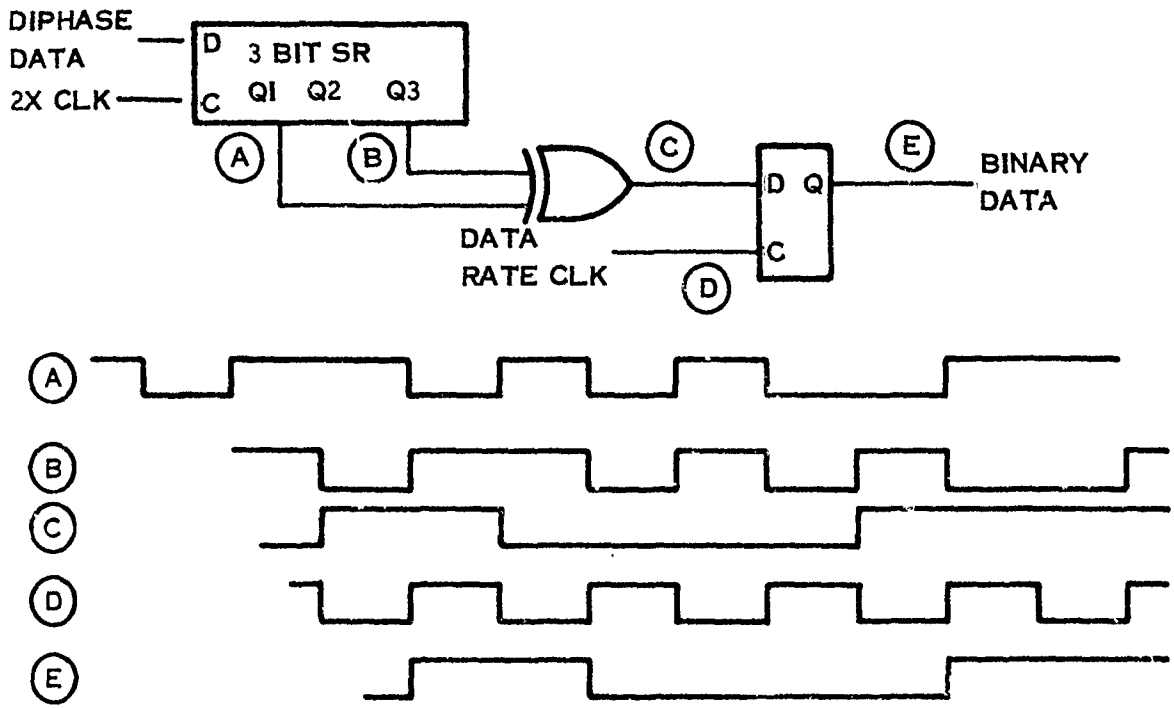


Figure 6-6. Diphase to Binary Converter

three bit shift register with the first and third outputs applied to an exclusive OR circuit. The output of the exclusive OR circuit is then resampled at the data rate.

The recovered data and timing are then applied to balanced NRZ drivers.

6.3.3 RLGM/CD POWER FEED

The power supply for the RLGM/CD (described in Section 14) provides 180 Vdc at 300 mA. This voltage is fed down the cable as means of powering the RLGM. The current is split up by applying the 180 volts to both transmit and receive lines. Therefore, the diphase data in and out and the transmit and receive orderwire are superimposed on the dc voltage. AC isolation is provided by blocking coils in both power feeds.

6.3.4 MAINTENANCE ORDERWIRE

An analog voice orderwire is provided with each cable driver. The orderwire is completely passive in the RLGMCD and will operate with or without unit power or with a faulty RLGMCD in the system. Audio transformers interface the orderwire with the cable.

6.3.5 BITE (BUILT-IN TEST EQUIPMENT) AND ALARMS

Various points within the RLGM/CD are monitored for proper operation, such as activity detection of signal inputs and outputs and phase-locked loop-in-lock detection. These status points will enable fault isolation to a single printed circuit board. An LED indication is provided on each driver card for ease in fault isolation.

Any detected fault within the unit will activate a summary fault light and will also provide a dc closure at pins of an external connector. This is called an S alarm (see Figure 6-1). Two other alarms, SA and LS, will provide dc closures at pins of the external connector. SA alarm will indicate a fault within the unit and loss of input cable signal will inhibit the SA alarm. LS alarm will indicate loss of incoming signal on either CX-11230 cable.

6.3.6 CABLE INTERFACE

A card called the Cable Interface is common to both drivers and contains the orderwire circuitry and the blocking capacitors. The power feed ac blocking coils are placed in the power supply. Two smaller inductance coils, one in the transmit power feed and one in the receive power feed, are located on the interface board to block any noise from the cable getting into the power supply. The line EMP protection diodes are also located on this panel on the cable driver side of the blocking capacitors.

The +180 volt power feed are isolated to this card and are not present on the two cable driver cards.

6.3.7 EMI

The equipment side signal lines into and out of this device are balanced. The balanced lines carry the traffic at rates of 72 or 144 kB/s. This balance is the primary suppression means. Shielded twisted pairs such as RG-108 are connected here to maintain good EMI suppression. There is a floating alarm which appears as a balanced line. All equipment side signals in this unit are digital, having a basic $(\sin x/x)^2$ spectral response. The clock line is chosen to be balanced for TEMPEST reasons. The diphase line signal has an $(\sin^2 X/X)^2$ spectral shape. waveshaping required for EMI suppression will be less serious than the cable.

The power line has a single EMI filter specified for dc, 60 Hz and 400 Hz. This makes it larger than a conventional filter, but smaller than two filters. The power line filter has an integral power line connector which gives far better performance and saves additional space.

6.3.8 HFE

The RLGM Cable Driver design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

The unit BITE control and alarm is positioned for rapid recognition and ease of identification.

Connections are located on the rear of the case and are positioned to ensure maximum accessibility. Front and rear panel layouts are shown in Figures 6-7 and 6-8.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472.

6.3.9 RELIABILITY

The reliability requirement for a single RLGM Cable Driver as contained in Specification TT-B1-2202-0013, Rev. 1, is an MTBF of 4000 hours (250 failures per million hours). The reliability prediction and the demonstrated results are summarized in Table 6-2.

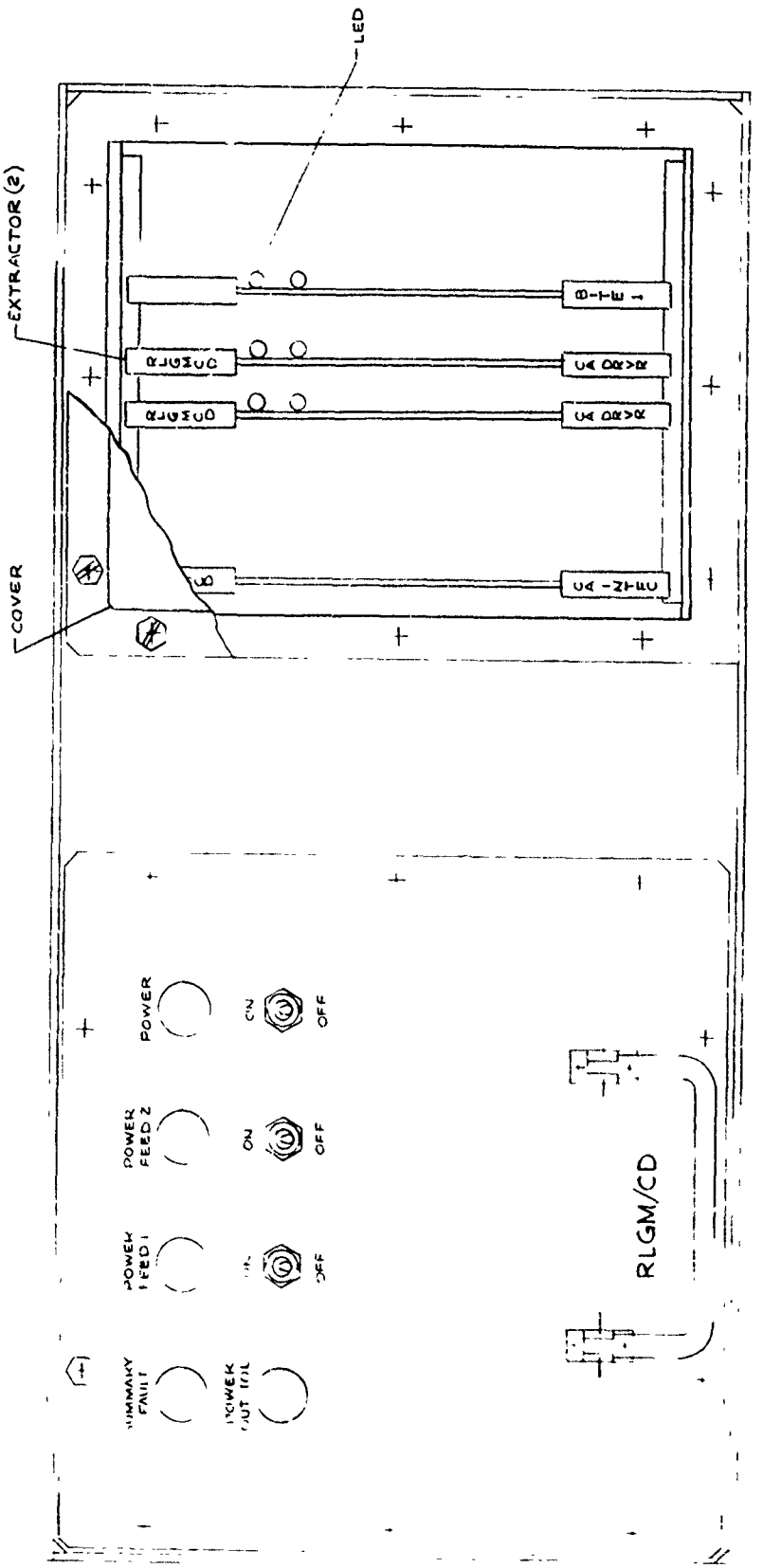


Figure 6-7. RLGM Cable Driver Front Panel

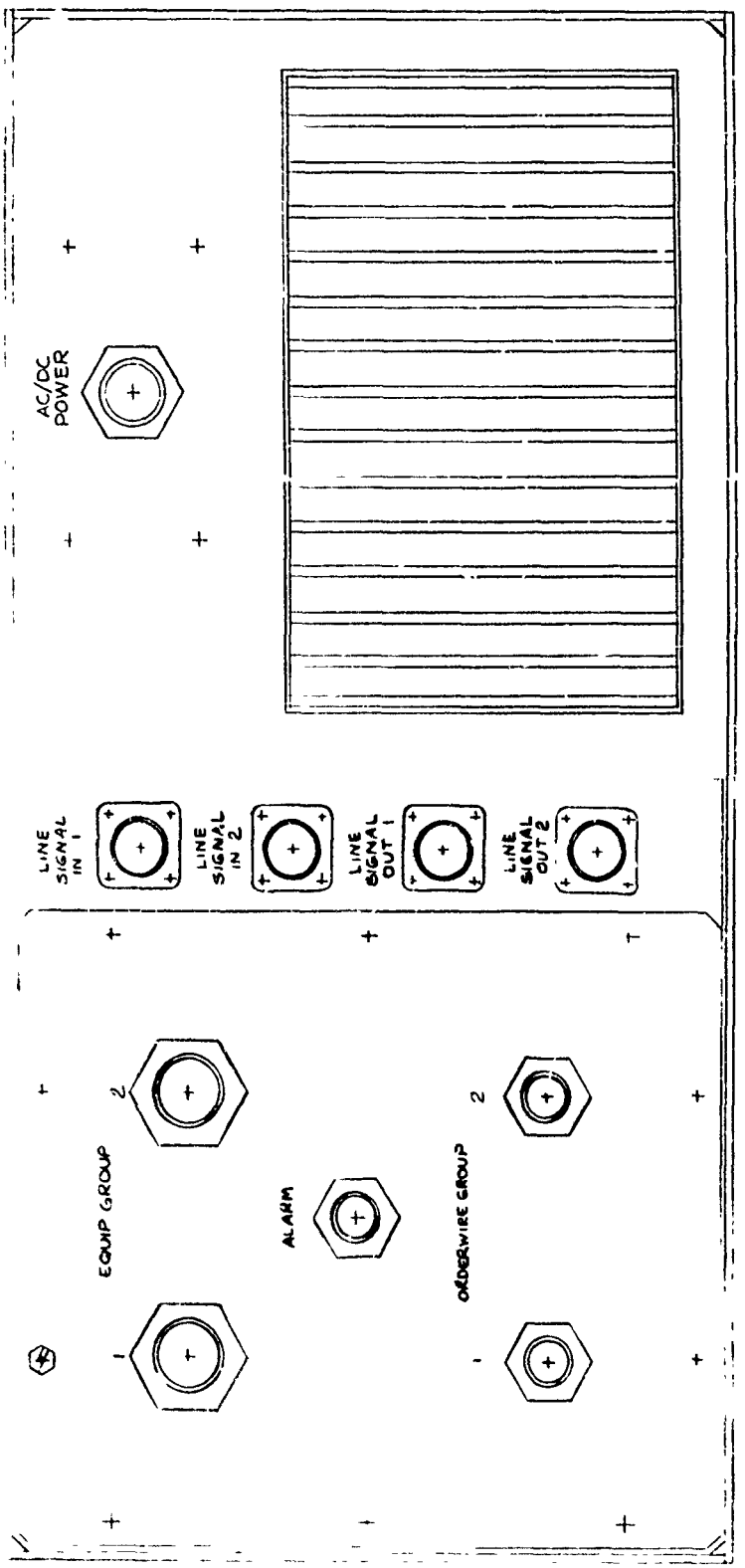


Figure 6-8. RLGM Cable Driver Rear Panel

TABLE 6-2

REMOTE LOOP GROUP MULTIPLEXER/
CABLE DRIVER RELIABILITY

	Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
Single	4000	18,457	13,600 (Note)
Dual	N/A	16,889	6,800 (Note)

NOTE: There were no failures during the demonstration test. The hours listed indicate the minimum demonstrated MTBF, by assuming a failure just after the test.

SECTION 7

RMC

(See Sylvania writeup - Volume II).

SECTION 8

TGM

8.1 DESIGN GOALS AND REQUIREMENTS

The performance goals are as enumerated in the specification with the exception of the frame storage capability. The present design is capable of sufficient storage for a maximum group size of 144 channels.

When the TGM is used in a system where the channels have a 16 kb/s rate and the frame has a 2 kb/s rate, it will not deliver a 4608 or 4096 kb/s supergroup. This would contain 288 channels and could not be accepted by any other TRI-TAC elements. Providing the added capability would increase the complexity and power dissipation of the equipment.

Table 8-1 contains a summary of the TGM functional requirements primarily as stated in the specification with the exception of the power dissipation and weight. The TGM Group rate structure is shown in Tables 8-2, 8-3, and 8-4 for the various classes of input rates.

With respect to the output, the TGM formats two types of supergroup outputs:

a. Normal - The supergroup output of the TGM is formed by aligning the frames (except for single channel operation), and then bit interleaving the group inputs; where no frame (and no overhead bits) appear in groups inputs 2, 3, or 4, the same format is adopted, but with no frame alignment of such groups and with overhead bit positions replaced by traffic bits. The appropriate format for each combination of group inputs identified in Table 8-1 is listed below: O = an overhead bit from the group input to Port N and N = a traffic bit from the group input to Port N.

TABLE 8-1

TGM FUNCTIONAL REQUIREMENTS

Number of Groups:	Up to Four
Group Rate:	72 kb/s to 2304 kb/s
Type of Multiplexing:	Synchronous
Group Interface:	Balanced NRZ and Timing
Super Group Rate:	128 kb/s to 4608 kb/s
Super Group Interface:	Balanced NRZ and Timing
BITE:	Locates equipment faults to replaceable subassembly
Telemetry Output:	150 b/s giving: Frame status for groups and super group; loss of receive group or super group; super group frame error count.
Telemetry Transmission:	2 kb/s telemetry subchannel, balanced NRZ and timing.
Timing:	Transmit timing from: Station clock; receive supergroup; group 1 on low speed side.
Framing:	Within 50 ms for 4 kb/s frame rate with minimum probability 0.9 in 0.1 percent BER random errors; and within 100 ms with minimum probability 0.9 in 20 percent Burst BER at 1 to 20 Hz rate with five percent duty cycle.
MTBF:	5000 hours
Power:	115 Vac ±10%, 50 to 400 Hz or 24 dc battery, 60 watts maximum input.
Size:	8-1/2" H x 12" D x 19" rack mount.
Weight:	10 kg

TABLE 8-2

TGM GROUP RATES

Input Bit Rates (kb/s)				Output Bit Rate (kb/s)	Frame Format[1]
Input No. 1	2	3	4		
2048[5]	2048	0	0	4096[5]	A1
2048	1024	1024	0	4096	B
2048	128-1024[2]	0, 128-512	0, 128-512	4096	C
1024	1024	128-1024	0, 128-1024	4096	A3
1024	512	512	128-512	4096	A3
1024	1024	0	0	2048	A1
1024	512	512	0	2048	B
1024	128-512	0, 128, 256	0, 128, 256	2048	C
512	512	128-512	0, 128-256	2048	A3
512	256	256	128, 256	2048	A3
512	512	512	0	1536[3]	A2
512	512	0	0	1024	A1
512	256	256	0	1024	B
512	128, 256	0, 128	0, 128	1024	C
256	256	128, 256	0, 128, 256	1024	A3
256	128	128	128	1024	A3
512	0	0	0	512	*
256	256	0	0	512	A1
256	128	0, 128	0	512	B
128[4]	128	128	0, 128	512	A3
256	0	0	0	256	*
128[4]	128	0	0	256	A1
128	0	0	0	128	*

*The overhead and traffic bit relationship is identical to the input overhead and traffic bit relationship.

Notes:

1/ X-Y means X or Y or any standard intermediate bit rate, e.g., 128-1024 means 128 or 256 or 512 or 1024.

2/ For the 512, 512, 512, 0 kb/s input bit rate combination, both 2048 and 1536 kb/s output rates are applicable, and the required output rate is switch selectable.

3/ For the 512, 512, 512, 0 kb/s input bit rate combination, both 2048 and 1536 kb/s output rates are applicable, and the required output rate is switch selectable.

4/ 128 kb/s input group rate will only be utilized with a 16 kb/s channel rate.

5/ With 16 kb/s channels, the maximum output bit rate is 2048 kb/s (128 channels), the maximum input bit rate is 1024 kb/s (64 channels).

TABLE 8-3

TGM GROUP RATES

Input Bit Rates (kb/s)				Output Bit Rate (kb/s)	Frame Format[1]
Input #1	Input #2	Input #3	Input #4		
2304[4]	2304	0	0	4608[4]	A1
2304	1152	1152	0	4608	B
2304	144-1152[2]	0, 144-576	0, 144-576	4608	C
1152	1152	144-1152	0, 144-1152	4608	A3
1152	576	576	144-576	4608	A3
1152	1152	0	0	2304	A1
1152	576	576	0	2304	B
1152	144-576	0, 144, 288	0, 144, 288	2304	C
576	576	144-576	0, 144-576	2304	A3
576	288	288	144, 288	2304	A3
576	576	0	0	1152	A1
576	288	288	0	1152	B
576	144-288	0, 144	0, 144	1152	C
288	288	144, 288	0, 144, 288	1152	A3
288	144	144	144	1152	A3
576	0	0	0	576	*
288	288	0	0	576	A1
288	144	0, 144	0	576	B
144[3]	144	144	0, 144	576	A3
288	0	0	0	288	*
144[3]	144	0	0	288	A1
144	0	0	0	144	*

*The output overhead and traffic bit relationship is identical to the input overhead and traffic bit relationship

Notes:

1/ X-Y means X or Y or any standard intermediate bit rate; e.g., 144-1152 means 144 or 288 or 576 or 1152.

2/ 144 kb/s input group rate is only utilized with a 16 Kb/s channel rate.

3/ 144 kb/s input group rate is only utilized with a 16 Kb/s channel rate.

4/ With 16 kb/s channels, the maximum output bit rate is 2304 kb/s (144 channels), the maximum input bit rate is 1152 kb/s (72 channels)

TABLE 8-4

TGM GROUP RATES
(RLGM OPERATION)

Input Bit Rate (kb/s)				Output Bit Rate (kb/s)
Input #1	Input #2	Input #3	Input #4	
144	--	--	--	288 (9 ch)
144	144	--	--	288 (9 ch)
144	144	144	--	576 (18 ch)
144	144	144	144	576 (18 ch)

Notes:

1. Bit rates reduced by a factor of two when loop rate is reduced to 16 kb/s.

Where appropriate, the bits of low rate group inputs will be multiple sampled to provide the correct interleaving patterns.

For single channel operation, the supergroup overhead and traffic bit relationship is idertical to the overhead and traffic bit relationship on group number one.

Format A1. $0_1, 0_2, 1, 2, 1, 2, --------$
Format A2. $0_1, 0_2, 0_3, 1, 2, 3, , 2, 3, --------$
Format A3. $0_1, 0_2, 0_3, 0_4, 1, 2, 3, 4, 1, 2, 3, 4, --------$
Format B. $0_1, 0_2, 1, 0_3, 1, 2, 1, 3, 1, 2, 1, 3, --------$
Format C. $0_1, 0_2, 1, 0_3, 1, 2, 1, 0_4, 1, 2, 1, 3, 1, 2, 1, 4, --------$

b. RLGM - The TGM accepts one to four RLGM group inputs and produce a supergroup frame output for a nine and 18 channel configuration as listed in Table 8-4. The nine channel supergroup output is a serial bit stream consisting of an overhead channel bit followed by eight traffic bits. These traffic bits will be assigned in the following order: Channel 1 from group 1, channel 1 from group 2, channel 2 from group 1, channel 2 from group 2, --, channel 4 from group 2. For the 18 channel configuration,

the group output is serial bit stream consisting of an overhead channel bit followed by a spare bit which is set to one, followed by 16 traffic bits derived from RLGM group inputs. These traffic bits will be assigned in the following order: Channel 1 from group 1, channel 1 from group 2, channel 1 from group 3, channel 1 from group 4, channel 2 from group 1, channel 2 from group 2, channel 2 from group 3, channel 2 from group 4, ... , channel 4 from group 4.

8.2 DESIGN APPROACH

Figure 8-1 shows a block diagram of the Trunk Group Multiplexer. The unit consists basically of four Group Multiplexer/Demultiplexer modules, which reclock and delay the group input and output signals so as to be able to line them up in an overall supergroup reference. In each Group Mux/Demux module are the associated input and output buffering circuits and sufficient delay storage to line the individual groups up with the supergroup frame. Frame sensing logic is also incorporated in each of these modules so as to sample the frame bit as required. While the frame sensing logic is done on a per channel basis, the actual framing procedure algorithm and control of the framing for the supergroup and all four groups is done in the microcontroller module.

The individual groups are combined into a supergroup on the Supergroup B Module. Here, the supergroup is combined and reclocked, and telemetry and framing patterns are introduced. The supergroup is demultiplexed on the Supergroup Timing module and feeds the individual group modules for outputting the demultiplexed group signals. This module also generates the associated group clocks and timing reference for delaying the input supergroup frame. The Supergroup B module contains the necessary circuitry for buffering and aligning the incoming data to the internal supergroup frame reference. The frame sensing logic for the supergroup reception is done on this module, however, controlling the frame synchronization is done on the Microcontroller module. The microcontroller utilizes the same framing algorithm and procedure for each group input as well as the supergroup input. As a result, the same hardware can be utilized for all five framing programs, and be time-shared among them.

Figure 8-2 shows a flow chart of the framing procedure required. Basically, all data is input on the I/O bus and the algorithm and procedural control implemented within the microcontroller. Results or actions to be taken is outputted

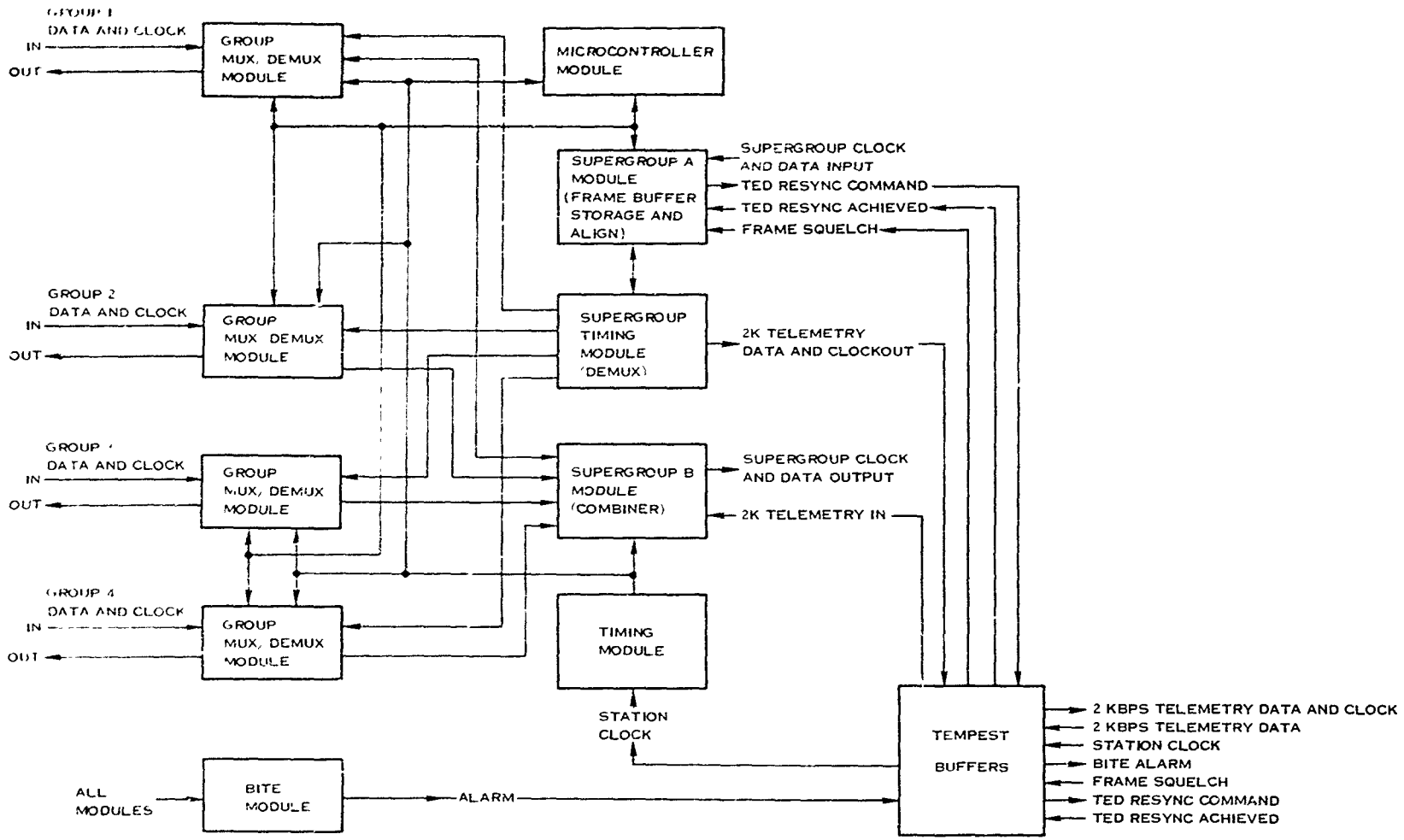


Figure 8-1. TGM Block Diagram

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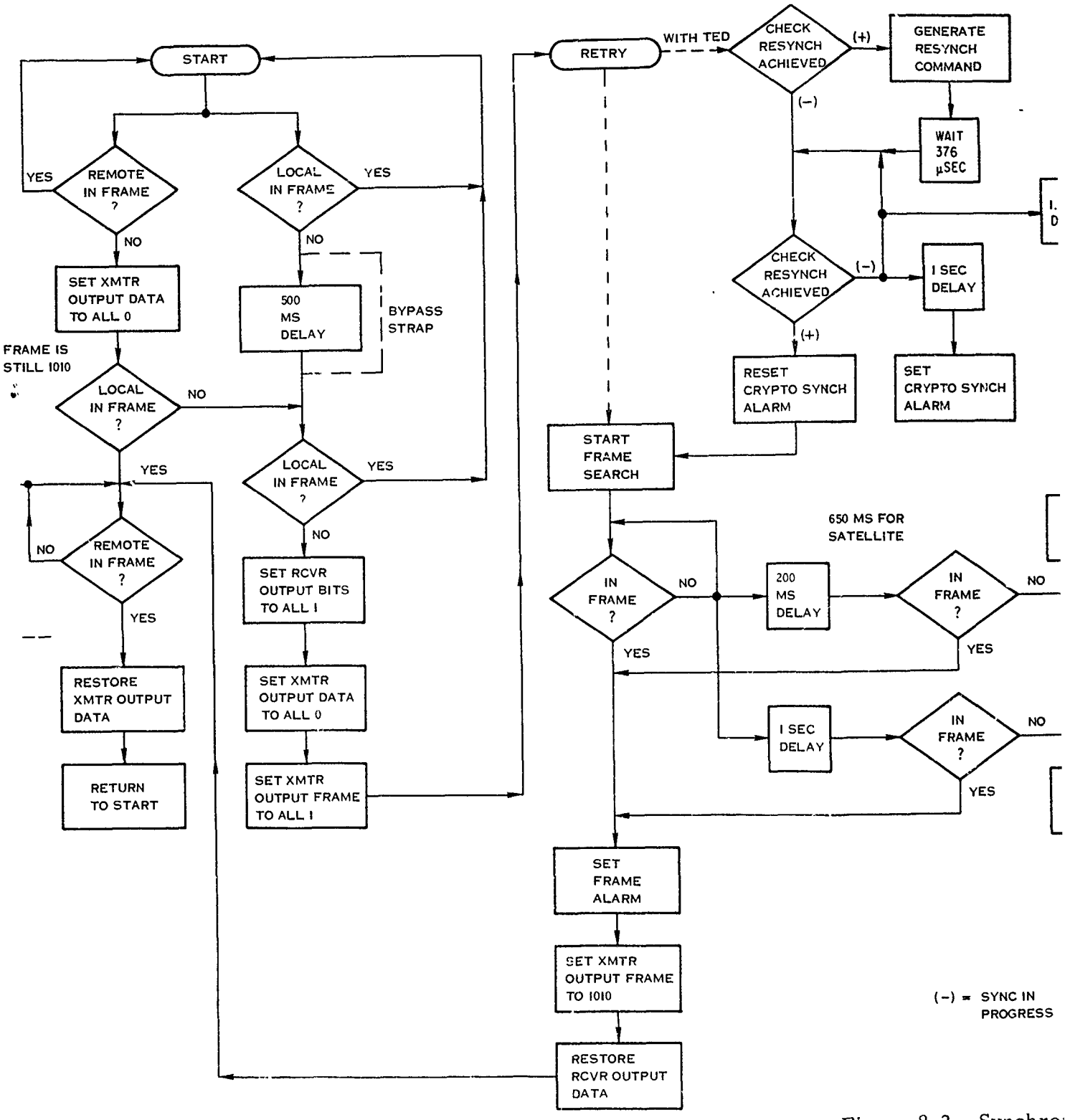


Figure 8-2. Synchro

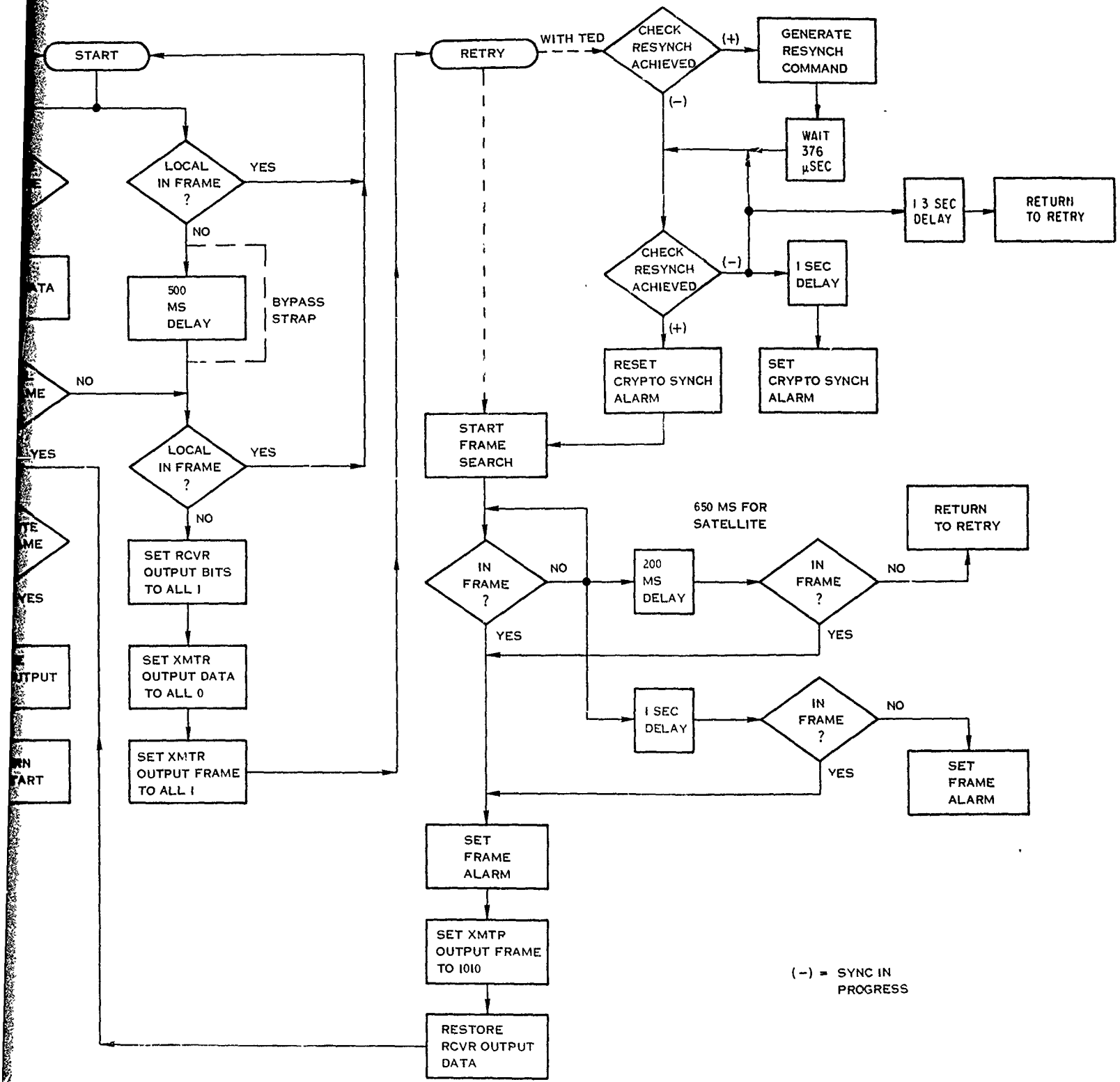


Figure 8-2. Synchronizer Flow Chart

on the I/O bus to individual modules as required. Timeouts required is implemented using a 500 Hz interrupt counted within the microprocessor. Strapping options and other manual control inputs are implemented using status registers connected to the I/O bus.

The procedure is basically identical to that of the TCC-39 switch. Since it is a handshaking procedure, it is essential that the DGM use exactly the same procedure to provide interoperability. The algorithm utilizes the TCC-39 switch analysis and resulting parameters to meet both the specification framing and TCC-39 switch interoperability requirements.

The synchronization time starts when Unit 1 detects that it is out of frame sync. Unit 1 sends 1111 -- frame and ZEROs on the data channel to indicate that it is out of frame sync. Unit 2 uses a 30 out of 32 criterion to detect 1111 -- frame and a 176 out of 512 criterion to detect all ZEROs on the data channels. Unit 2 detects that Unit 1 is out of frame when both of these detection criteria are met. Unit 2 detects that Unit 1 is out of frame within 10.5 ms for a 4 kb/s frame signal and 21 ms for a 2 kb/s frame signal. An additional average detection delay of 25 ms is expected in burst noise environment. When Unit 2 detects that Unit 1 is out of frame, it removes all data and transmits only 1010 -- frame. Unit 1 searches for and acquires 1010 -- frame synchronization within 10.7 ms for a 4 kb/s frame signal and within 21.5 ms for a 2 kb/s frame signal. Upon acquiring frame sync, Unit 1 changes its transmit frame signal from 1111 -- frame to 1010 -- frame and connects data to the data channels. Unit 2 detects the 1010 -- frame and data in the same manner that it detected 1111 frame and ZEROs on the data channels above. When Unit 2 detects that Unit 1 is in frame, it connects data to the data channels and communication is restored.

Since Unit 2 can switch from the all ONEs pattern to an alternate zero-one patterns while Unit 1 is still looking for the all ONEs pattern, separate all ONEs, zero-one and one-zero searches will be made. These will be made concurrently on frame bits. All three cumulative counts will be tested for the 30 out of 32 criterion. If any one passes this test, the frame pattern has been detected and the program continued looking for 176 out of 512 ZEROs on the data channels. As a result of using a microcontroller for the synchronizer, the additional counters required manifest themselves as additional locations in RAM. There are sufficient storage locations in RAM so no increase in hardware results.

A microcontroller was selected here as the best approach for the sync algorithm for a number of reasons. First, the same algorithm must be utilized for five different inputs. This could be accomplished using five different logic circuits, however, they would be running only a very small fraction of the overall time. As a result, the overall duty cycle of the circuits would be quite low. One, therefore, would like to time-share synchronizer circuits. With respect to the synchronizer algorithm itself, a maximum amount of flexibility is desirable so that the algorithm may be changed at future dates to improve the system with a minimum amount of changes to the hardware. Both of these requirements lend themselves to the use of a microcontroller where random logic may be most easily implemented and changed merely by changing the firmware, that is, programmable read-only memories in the microcontroller.

With respect to the storage requirements of the multiplexer, a number of approaches were considered. A centralized RAM storage for all groups was first considered, however, it was discounted because the speed requirements would have been too great for present day technology utilizing a single RAM. If the RAM were segmented into words, it was felt that the same storage requirements would be the same as for the segmentation of a RAM on a group basis. Segmenting the RAM on a group basis also allows for identical group modules to be utilized rather than one larger special module. In selecting the individual integrated circuits to use for storage, a RAM was used because of the speed requirements and the ability to change the total number of bits used within the device. In determining the specific device to be used for storage, a 1024 by 1 and a 256 by 1 RAM were considered. The dissipation for the larger RAM was found to be approximately the same as that of three of the smaller RAMS which would give adequate storage capabilities. As a result, the larger RAM was used.

An attempt was made to incorporate the input FIFO into the group RAM storage, but was discontinued when a single integrated circuit FIFO was found to be available. With this circuit, the complexity of the design was greatly reduced. The FIFO to be used contains 64 bits and, as a result, does not contain the buffering capabilities stated in the proposal (256 bits). However,

use of this single integrated circuit considerably reduces the power requirements over the 256 bit FIFO which must be designed with many separate MSI functions.

The specification does not identify any requirements for the FIFO. The requirement of inputs from extension facilities, where no master clock exists, due to radio or cable jitter of ±2 μsec is 19 bits. If inputs came from different nodes having different master clocks, 163 bits would be required. Since this requirement apparently does not exist, the 64 bit FIFO is more than adequate, and is used.

A separate module is utilized for generating the telemetry signals required for the TGM. In addition, a timing module is incorporated so as to generate all clock circuits required for the other modules from the group input clock, station clock, or supergroup input clock utilizing a phase lock to obtain a basic clock frequency of 4.608 MHz or 4.096 MHz. TEMPEST buffers are provided on all BLACK inputs and outputs, i.e., all non-group and supergroup data and clock inputs and outputs.

8.3 DETAILED DESIGN DESCRIPTION

8.3.1 GROUP MUX/DEMUX MODULE

Figure 8-3 shows a detailed block diagram of the Group Mux/Demux module. This module basically contains all the delay storage, frame sensing logic and reclocking required for each of the group input/output signals. The group input data signals and clock are clocked into a 64 bit FIFO. This unit has totally asynchronous input and output clocks and, therefore, accomplishes the clock buffering between input groups and the TGM. In addition, it supplies the capability of ±32 bits of delay variation on the input signal. 19 bits is adequate for radio or cable extensions. As a result, more than adequate storage requirements have been implemented. This serial output bit stream from the FIFO drives the frame sample logic.

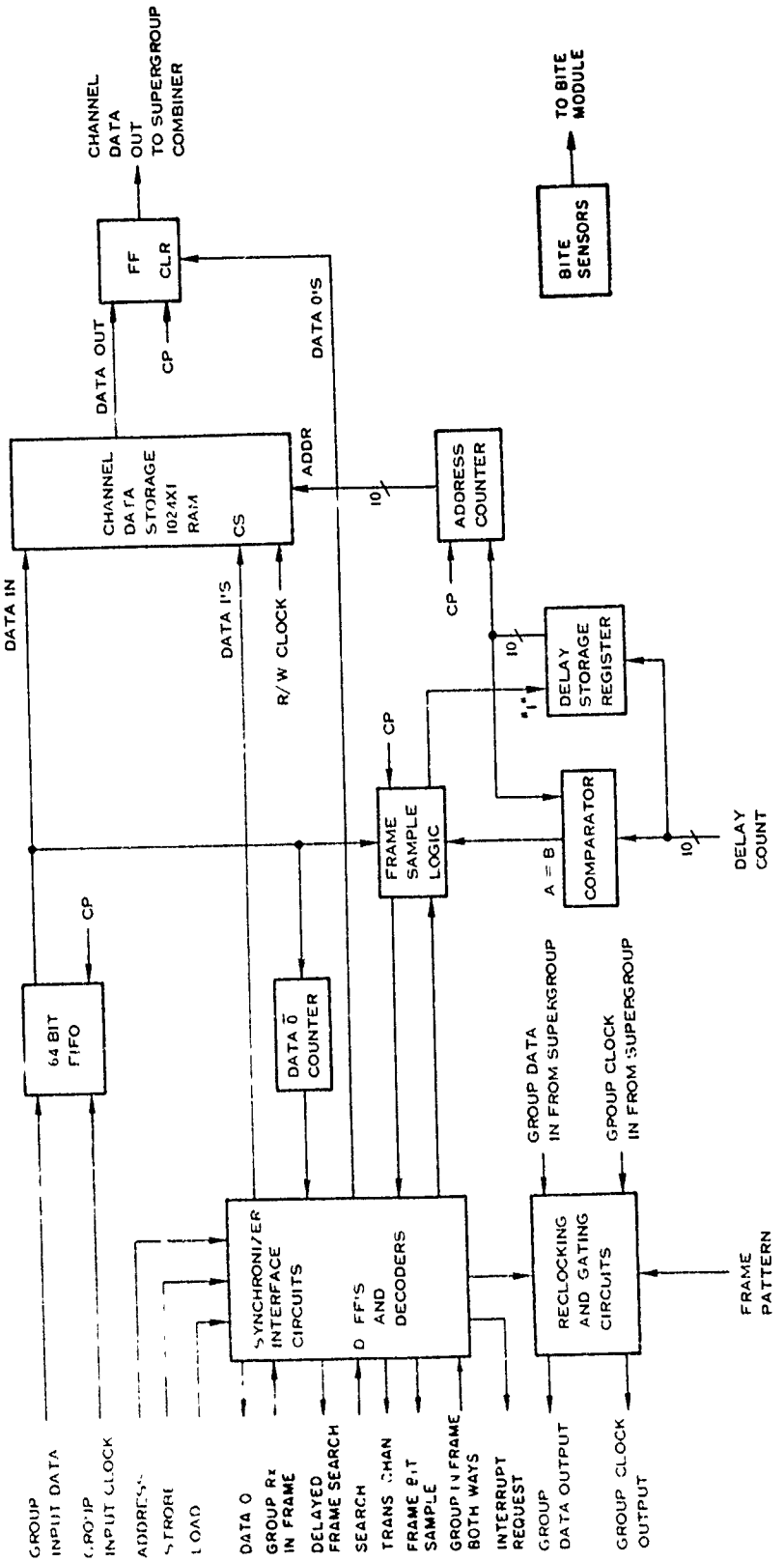


Figure 8-3. Group Mux/Demux

The frame sample logic searches for the framing bit and sample bit. The logic, under a command from the microcontroller initiates search for the frame bit at the bit rate. When a one is detected in the frame sample logic, the count in the frame bit counter located on the timing circuits will be stored in a delay storage register located on this module. The frame bit counter supplies a delay count for each of the modules. Therefore, the relative position of the sample framing bit is stored locally on this module. As a result, the relative group frame bit, positions itself to a common reference (the frame bit counter). After the detection of the frame bit, the microcontroller interface circuits, which are primarily a set of D flip-flops and decoders, will raise an interrupt request for the microcontroller to allow it to process the sampled bit. The microcontroller services the interrupt and performs a step in the algorithm before the next trial frame bit occurs (250 microseconds later).

The frame bit counter having counted the total number of bits per frame will, one frame later, present the same number as stored in the delay register. The comparator compares these two and presents a sample pulse to the frame sample logic to sample the next frame bit. Once again, an interrupt occurs for the sync algorithm and the algorithm continues to process the bits. When the frame pattern is finally detected and the non-zero data bits must be counted, they are counted in a counter located on this module and again the results transmitted to the microcontroller for evaluation in the algorithm.

When finally synchronized, the delay storage register contains the required delay from a fixed reference point (frame bit counter) for the individual group bit stream. This number is used as the modulus is on an address counter for a 1024 by one RAM which stores the data for that particular channel. For each bit, the address counter is incremented, the data being read out prior to writing in of new data. A delay equal to that of the modulus is thus obtained. The output data is gated to either all one's or all zero's as required by the framing algorithm through microcontroller interface circuits, and the reclocking flip-flop on the output of the RAM. This output feeds the supergroup combiner where it is combined with the other channels.

Figure 8-4 shows the microcontroller Interface Circuits block diagram used on the Group or Supergroup A modules.

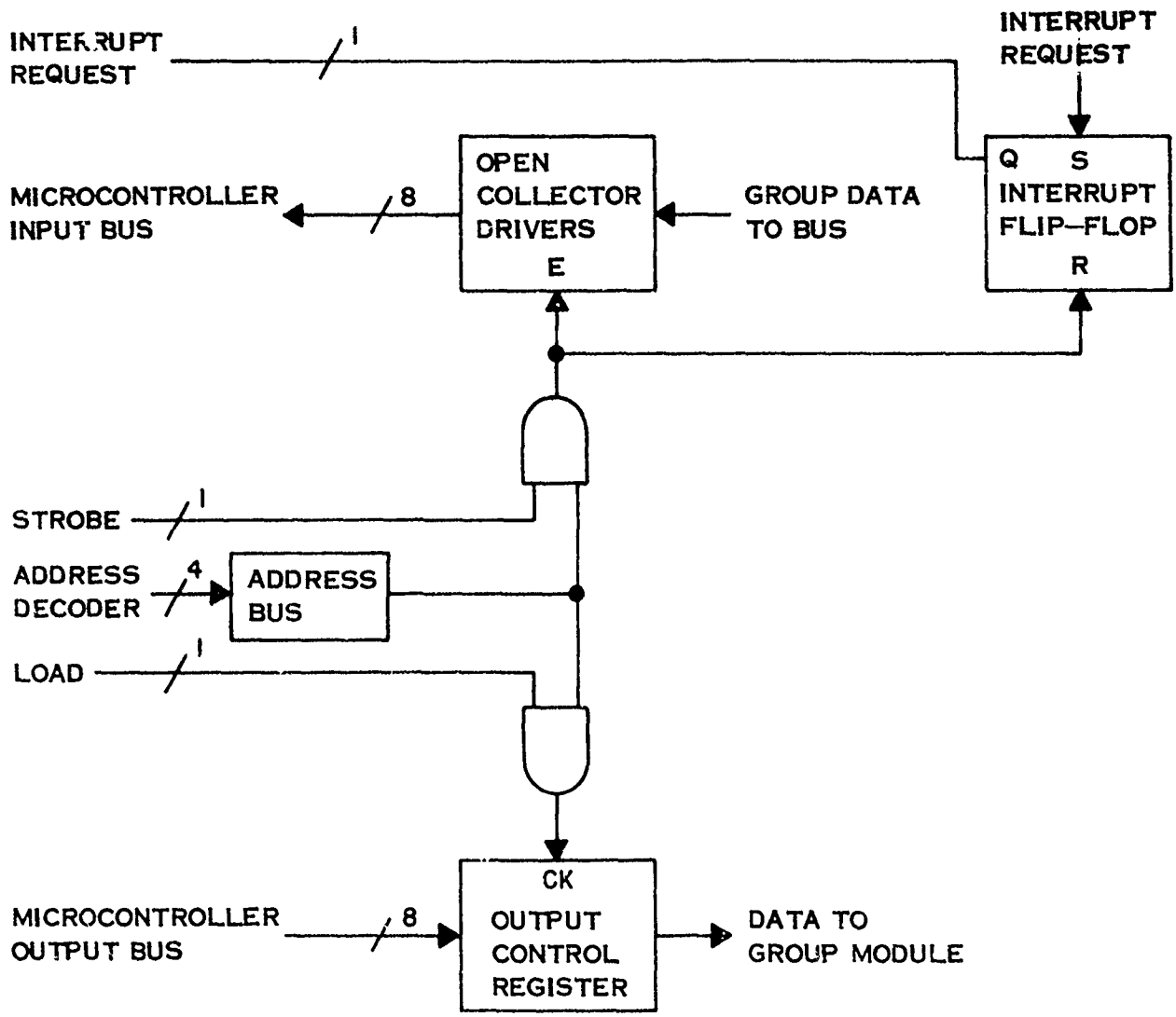


Figure 8-4. Microcontroller Interface Circuits on Group or Supergroup Modules

If the module requests servicing, it sets the interrupt flip-flop. Upon recognizing the interrupt, the microcontroller addresses the module on the four bit address bus. The microcontroller subsequently enables the module data onto the input bus with the strobe pulse for its duration while resetting the interrupt flip-flop. Since only one module is addressed at a time, this is the only data to appear on the bus at that time. Furthermore, since the drivers are open collector, they only drive the line when enabled and, as a result, do not load the bus when disabled.

If data is to be loaded into the module from the microcontroller, the module is addressed using the address bus and the data is placed on the output data bus. The microcontroller then enables the load pulse and the data is read into the output control register on the group module.

This module also contains the reclocking and gating circuits required for the output of the supergroup demultiplexer. The local group telemetry and frame pattern are added in these circuits as required. The reclocking and gating circuit outputs drive the group clock and data outputs. The information for the framing and associated control signals required as a result of group level in-frame/out-of-frame status is obtained once again from the microtroller through the interface circuits on the module.

Bite test points monitored on the Group Mux/Demux module are as follows:

Demux Group Data In (from Supergroup)
Frame Pulse In (from Supergroup Timing)
Terminal Count of RAM Address Counter
Group Data Clock Out (to external interface)
Demux Group Data Out (to external interface)
FIFO Reset
Terminal Count of Data 512 Counter
Group Rate Zero
Tx Data Clock In (from Supergroup Timing)
Rx Internal Group Clock In (from Timing Module)
Group Tx Data Out (to Supergroup)
Interrupt Flip-Flop
Rx Group Data In (from External Interface)
Rx In Sync
Rx Group Clock In (from External Interface)

8.3.2 SUPERGROUP A MODULE

The Supergroup A Module, Figure 8-5, contains the interface circuits delay storage and frame sensing logic required for the supergroup data input. These circuits are conceptually the same as those used on the Group Mux/Demux module with a few exceptions.

Since a supergroup input clock is available, the input data need only be re-clocked and no elastic store is required.

With respect to the microcontroller interface circuits, the transparent channel bit has been omitted. In addition, the TED Resync command, TED Resync Achieved and Frame Inhibit signals have been added. These allow the additional controlling the TED sync and supergroup framing from the microcontroller.

The RAM storage for the supergroup is twice that required for the supergroup modules. As a result, two 1024X1 RAM's are used in a 1024X2 bit word. This configuration was used so that the RAM's may run at half the speed (a more conservative design). The RAM output is recombined into a single serial bit stream at its output. The RAM delay addressing circuitry is similar to that of the group module with the exception that eleven bits are required to address the complete delay range. The delay count input is derived from the Supergroup Timing Module frame counter.

The following points on the Supergroup A Module will be monitored for BITE:

Interrupt
RAM Address counter output
Data Not Zero output
RAM Write Enable pulse
Delayed Data In
Data Out
Supergroup Clock/2

8.3.3 SUPERGROUP TIMING MODULE

Figure 8-6 shows a block diagram of the Supergroup Timing module.

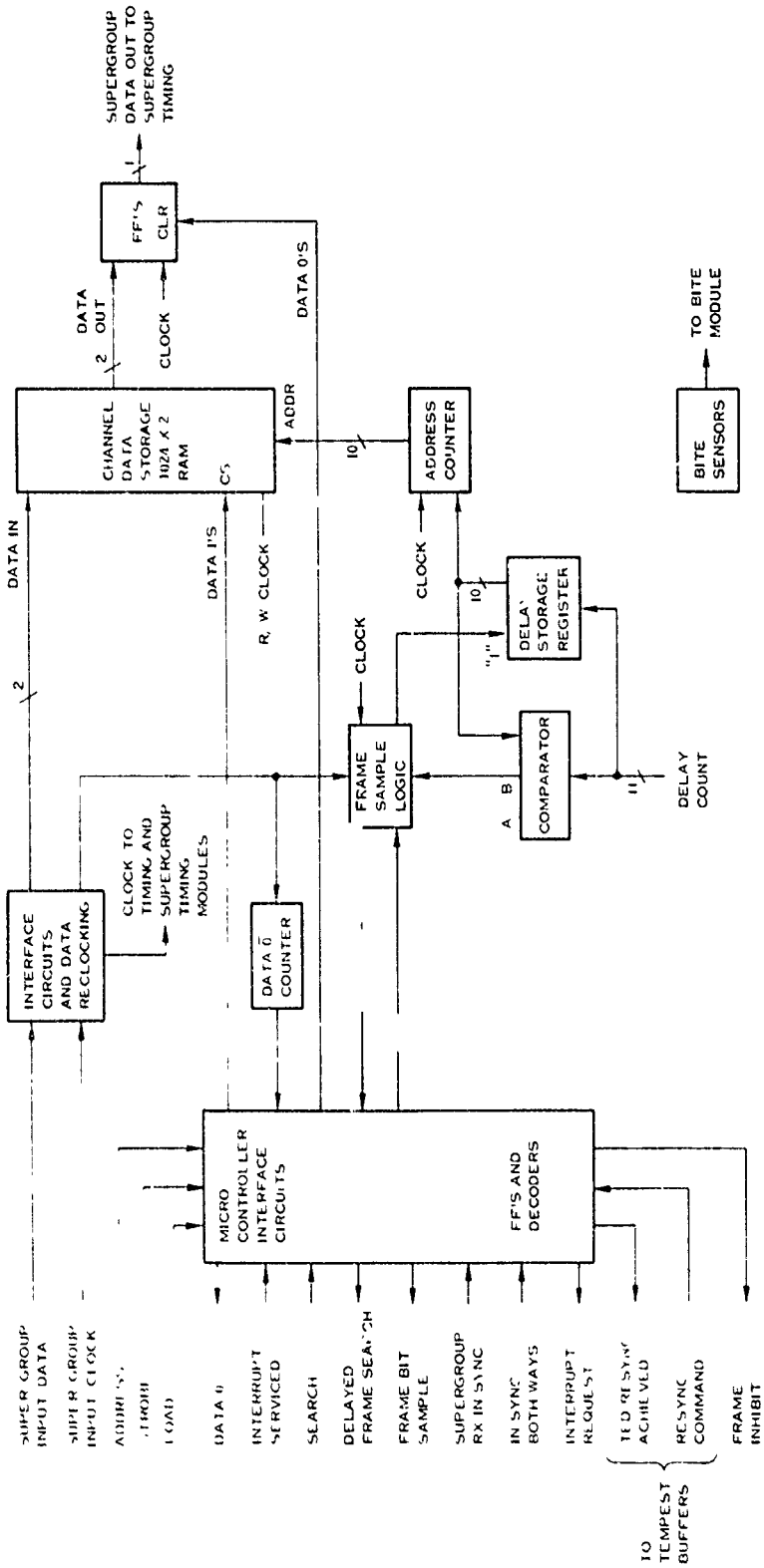


Figure 8-5. Supergroup A Module

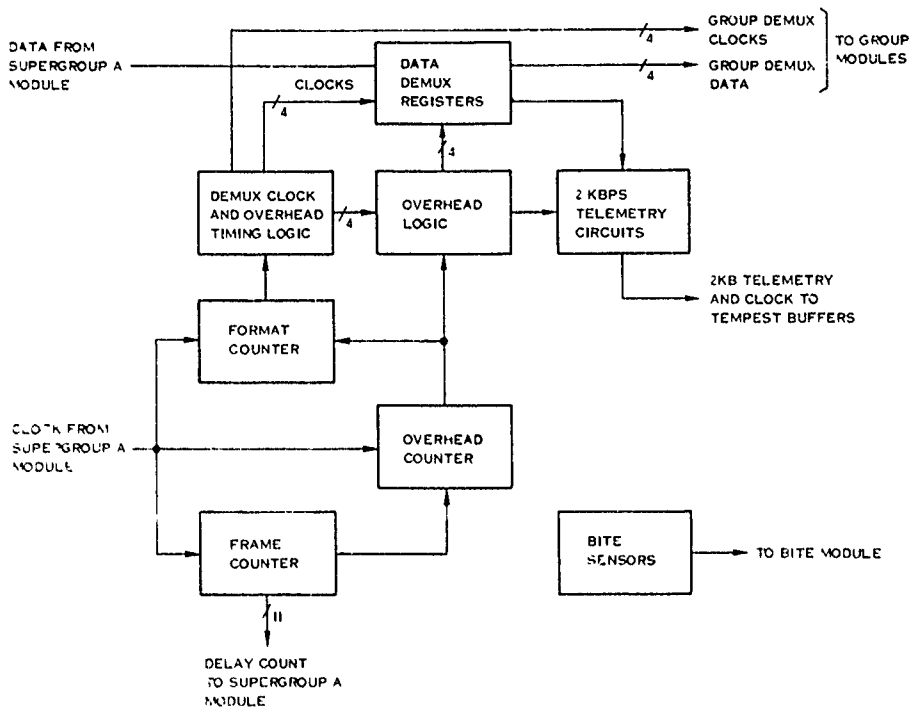


Figure 8-6. Supergroup Timing

The frame search counter divides the Supergroup input clock by the number of bits per frame for the chosen rate. The count (delay count) is continually sent to the Supergroup A Module which determines at what count the frame pulse occurs and delays the input data so that the frame pulse arrives at the Supergroup Timing Module coincident with the frame search counter's lowest or loaded count.

The overhead rate counter divides the Supergroup input clock by a number that achieves the overhead rate. In the normal mode an overhead gate is generated at its loaded count. In the RLGM mode the overgate is terminated by the first load pulse not coincident with load pulse of the frame format counter. The load pulse of the overhead rate counter is synchronized with the load pulse of the frame search counter.

The rate PROM-controlled or addressed by a manual rate switch-determines the counting intervals for the overhead counter and the frame search counter since its interval is always eight times that of the overhead counter's. The overhead PROM generates the group clock pulse and then overhead bits positions. Spurs are eliminated by using reclock flip-flops.

The 2K telemetry circuits store and forward the supergroup overhead bits when required. In the normal the fifth overhead bit is transposed to the sixth overhead position of Group 1 with a logical "1" dummied into its location. The sixth supergroup overhead bit is transposed to the Group 1 seventh overhead position and the seventh overhead bit is produced locally for the two kbps local telemetry channel. For RLGM the overhead bits are not forwarded but set to a logical "1" for all groups.

The following points are monitored on the Supergroup Timing Module:

Overhead Counter
Frame Counter
Frame Format Counter
2K Telemetry Clock Out

8.3.4 SUPERGROUP B MODULE

The Supergroup B Module is used to combine the aligned group data from the group modules into one supergroup bit stream. Figure 8-7 is a block diagram of the logic. As can be seen, the circuitry has three major input interfaces: data from the Group Modules; clocking and control signals from the Timing Modules; and the local telemetry data. A one-of-fourteen multiplexer serves as the heart of the combiner structure. The associated control signals simply select the source which is to be switched into the supergroup data stream; the source may be either data or overhead information.

The bank of delay flip-flops is used to delay the group data streams with the resolution of the supergroup clock. The various delays are necessary to cover all the supergroup formats specified in the DGM Design Plan.

The Group 1 telemetry register logic is used to strip off the overhead bits in the Group 1 data stream (overhead channels 6 and 7) and to provide the storage for these bits so that they may be forwarded in the supergroup data stream (overhead channels 5 and 6) during the following frame. Note that as per the DGM Performance Spec, this is done only for the non-RLGM formats.

The local telemetry logic is used to reliably sample and store the 2 kHz local telemetry signals so that it may be presented to the multiplexer for insertion into the supergroup data stream. This circuitry employs an autophasing circuit

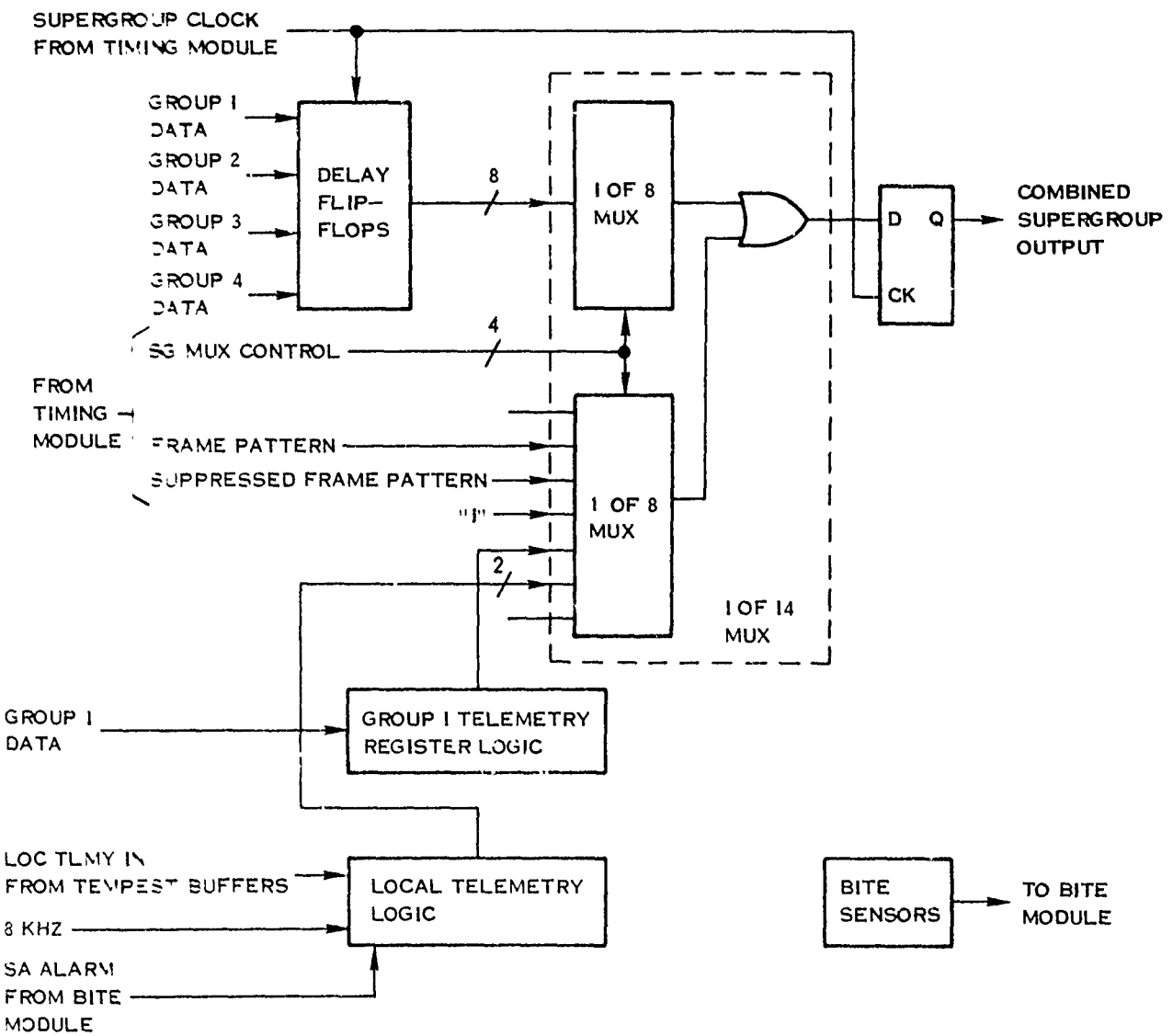


Figure 8-7. Supergroup B Module

which essentially locates the active edge of the sampling clock away from the data transition times. A telemetry loop-back switch has also been incorporated into this logic per DGM POD No. 22A.

The following points are tested for BITE on the Supergroup B Module:

Combined Supergroup Data Out
Supergroup Half-rate Clock
8 kHz Local Telemetry Clock

8.3.5 MICROCONTROLLER MODULE

The Microcontroller Module, which performs the framing algorithm, is basically an eight bit machine. A microcontroller was selected primarily because of its ability to perform random logic most efficiently, particularly where a number of circuits require the same random logic to be performed. As a result, the microcontroller can perform this logic for all inputs on the time-shared basis, and thus utilize the basic speed capabilities of the present day TTL devices to minimize the hardware required.

A number of other considerations were traded off in determing the approach to design. An individual synchronizer circuit for each group input would have increased the hardware considerably, along with dissipation, since it would not be time-shared. If one time-shares any sort of logic and desires some degree of flexibility in order to implement changes in algorithms one basically must come to using the microcontrol approach, primarily because of its great flexibility and availability of devices to perform the task in this manner. The microprocessor described is a bipolar device. Some slower speed, higher density, lower dissipation, MOS devices were considered. However, they have slow instruction times (microseconds), and an order of magnitude more time is required to perform the same operations. As a result, there would be insufficient time to service all interrupts and the circuitry would be inadequate to perform the task at hand.

Figure 8-8 shows a block diagram of the microcontroller module. The microcontroller is an eight bit machine operating at a 400 nanosecond minimum cycle time. In considering the requirements of this microcontroller, one must first consider the task at hand. The maximum frame rate is 4 kb/s. A frame

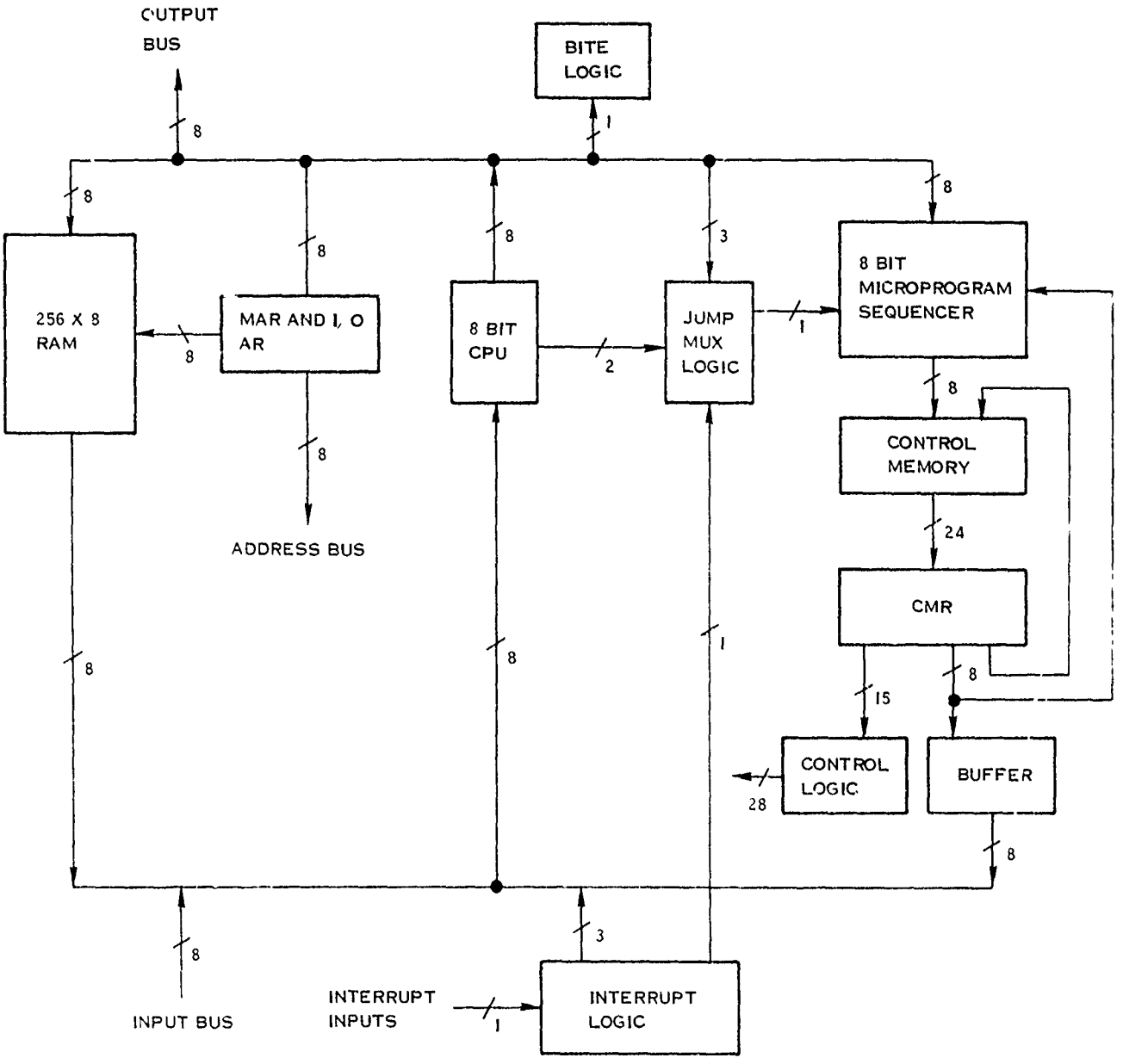


Figure 8-8. Microcontroller Block Diagram

sample bit may occur every 250 microseconds. During this 250 microseconds, the synchronization algorithm must be run for each of the group inputs and for the supergroup input, or a total of five synchronization programs. This allows approximately 50 microseconds for each program. With a cycle time of approximately 400 to 500 nanoseconds, some 100 instructions may be done within this period of time. The number of instructions required for each test of the frame bit is estimated at about 75 to 80 instructions maximum. As a result, with the 400 ns cycle time, there is sufficient time to do all five programs within the 250 microseconds.

The total program length for the framing algorithm is presently estimated at approximately 300 words. As a result, a control memory with 512 words is more than adequate for the task at hand. In addition, a total of about 95 words of storage in RAM are required to store the present program variables and addresses.

Another input to the priority interrupt circuits will be that of a 500 Hz pulse from the timing module which will allow for real time time-out functions. Shown on the diagram is an eight bit MAR and I/O address register. Through this register, the microcontroller will address individual modules on a four bit address bus. An eight bit output data bus and an eight bit input bus will interface with the modules to send instructions and receive data, respectively, from an individual module. The outputs include: in sync indicators, search commands, interrupt serviced, TED resync command and reset command. The microcontroller also outputs a load pulse to load the individual addressed module at the other end with the instruction. In addition, it has the capability of outputting a strobe pulse which turns the individual module on for transmission of signals to the microcontroller on the input bus. These include: the frame sample bit, data zero, TED resync achieved, frame inhibit and delayed frame search.

BITE is accomplished by use of a flip-flop addressed by the MSB of the address bus and cleared by data on the output bus via the firmware after having been asynchronously set.

8.3.6 TIMING MODULE

The timing circuits module generates all timing and clock pulses required in common for all the other modules. Figure 8-9 shows a

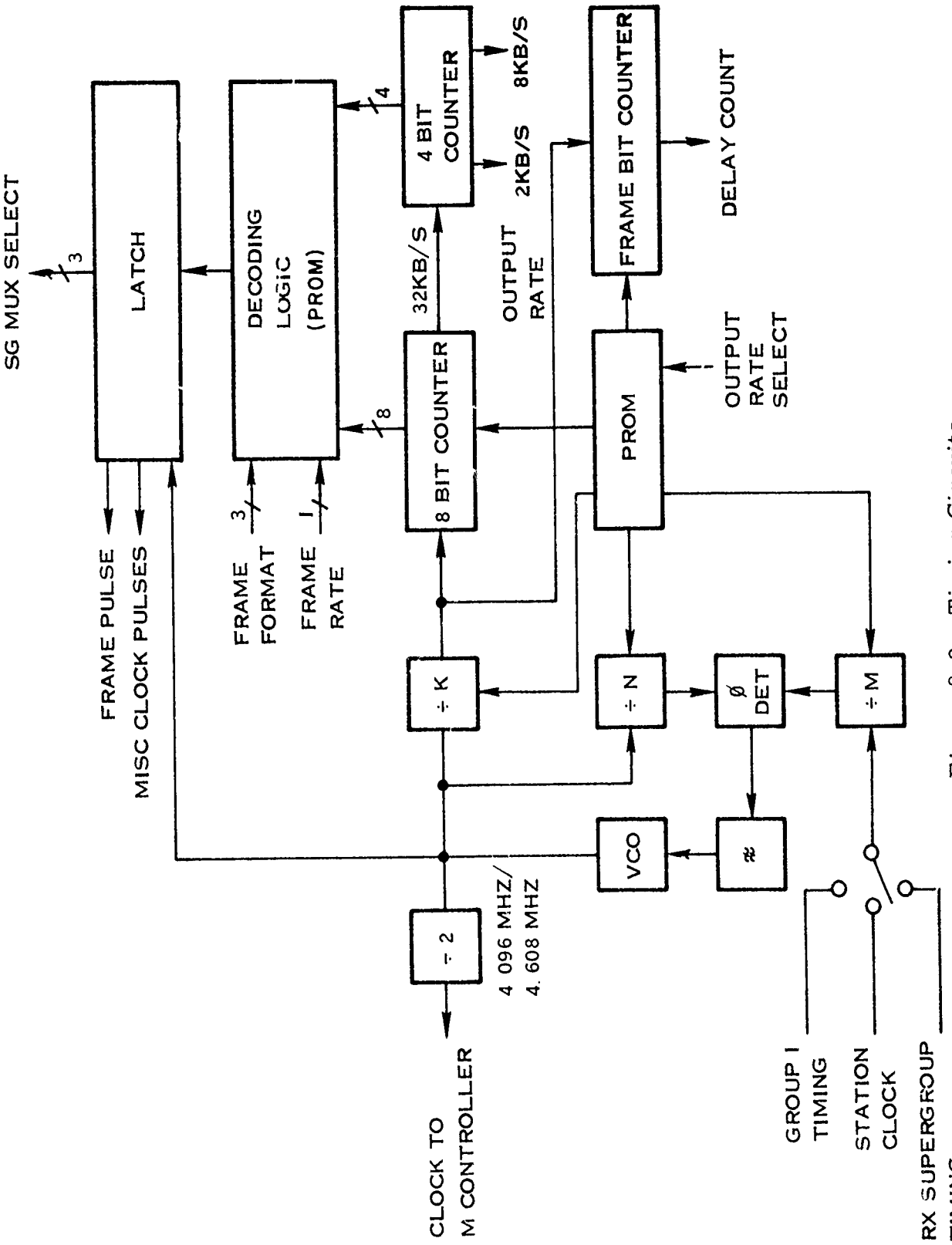


Figure 8-9. Timing Circuits

block diagram of the timing circuits. The basic clock generation is derived from a phase locked loop which obtained its input from one of three sources. The sources are either group one timing, station clock or the receive supergroup timing. The phase locked loop is a standard design where the input reference clock is divided down and compared with the divided down VCO output in a phase detector and used to control the VCO. The VCO output will be either 4.096 MHz or 4.608 MHz as determined by the respective class of input rates. In the case where the station clock or receive supergroup timing is at 4 MHz, the divide by M and N will be adjusted accordingly so as to produce the same 4 MHz output. In addition, 4 MHz output is desired so as to obtain a 2 MHz clock for the microporcessor regardless of the group or supergroup rate. The values of M and N are controlled by a PROM whose input is determined by the output rate required.

The output of the VCO is then divided by a constnat which is also a function of the output rate so as to obtain the appropriate output rate timing to drive all the coding logic required. This output rate drives the frame bit counter which provides the prime reference to which each of the individual group modules must delay the input of the group so as to line up the frame. In addition, the output rate will be counted down to 2 kHz which is the minimum framing rate required for the system. Outputs of this 12 bit counter will drive the decoding logic, which in conjunction with frame format and frame rate inputs, will derive all the miscellaneous clock and framing pulses required for the system. In addition, the decoding logic also supplies the supergroup multiplexer select address which again is a function of the frame format.

a. The 500 Hz signal is monitored to check the frame counter chain down through the module 4 counter which is used to generate the suppressed frame pattern.

b. An output of the register which clocks the SG data MUX control lines is monitored, thus providing some indication that the format counter and SG Timing ROM are operational.

c. A single output of the Overhead Control ROM provides a check on This ROM as well as the timing circuitry which addresses it.

8.3.7 BITE Module

The TGM utilizes the standard DGM BITE module programmed to do fault diagnostics on the above mentioned modules. A description of this module appears in Section 20. The points monitored on each module are described in the module discussions.

8.3.8 EMI

The group and supergroup side signal lines into and out of this device are balanced per paragraph 2.7. This interface relies on balance as its primary means of EMI suppression. The external cables connected here are shielded twisted pair, such as RG-108, so a high degree of suppression can be maintained. There is a wide range of bit rates on these lines, from 72 to 4308 kb/s, and waveshaping suitable for the highest rate would be ineffective at the lowest. There are auxiliary signals for orderwire and telemetry that are balanced per paragraph 2.7. These use waveshaping and are carried externally in multipair cable. The full duplex telemetry channel has a rate of 2 kb/s. There is a station clock line which will be balanced for TEMPEST reasons and a floating alarm line which appears as a balanced line. All the above equipment side signals are digital and have the basic $(\sin x/x)^2$ spectral shape.

The power line has a single EMI filter specified for dc, 50 Hz, 60 Hz, and 400 Hz making it larger than a conventional filter, but smaller than two filters. The power line filter has an integral power line connector which gives far better filter performance as installed on the unit and saves additional space.

8.3.9 HFE

The TGM design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are incorporated onto the accessible edge of the PCB's. These controls are protected by the front panel cover. The setup controls located on the front panel are screwdriver adjustable. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connectors are located on the rear of the case and will be positioned to ensure maximum accessibility.

Figures 8-10 and 8-11 show layouts for the front and rear of the TGM.

8.3.10 RELIABILITY DESIGN

The TGM has a specified MTBF of 5000 hours. This is equivalent to 200 failures in 10^6 hours. The reliability prediction and the demonstrated results are summarized in Table 8-5.

TABLE 8-5

TGM RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
5000	6627	15,500

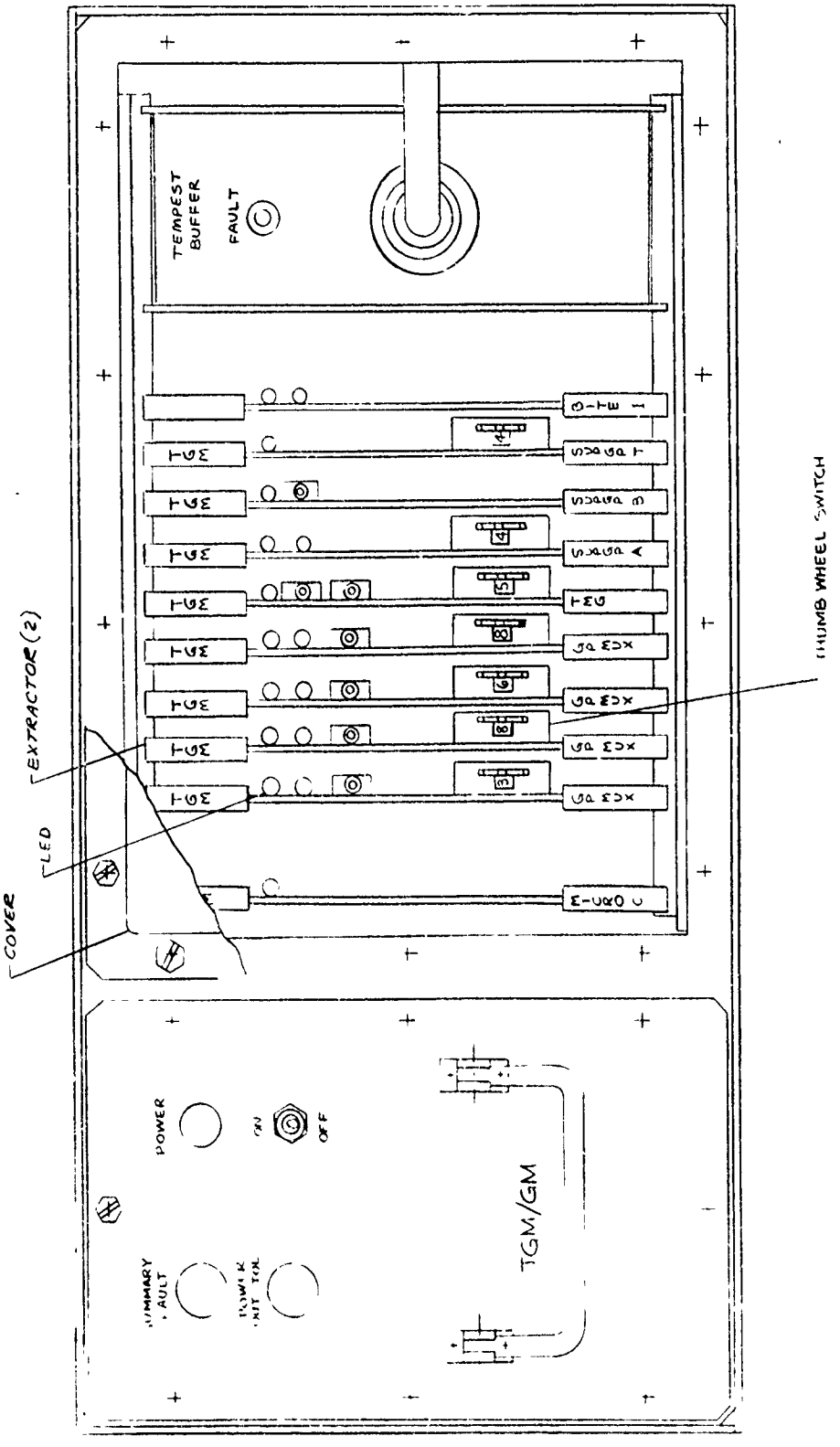


Figure 8-10. TGM Front View

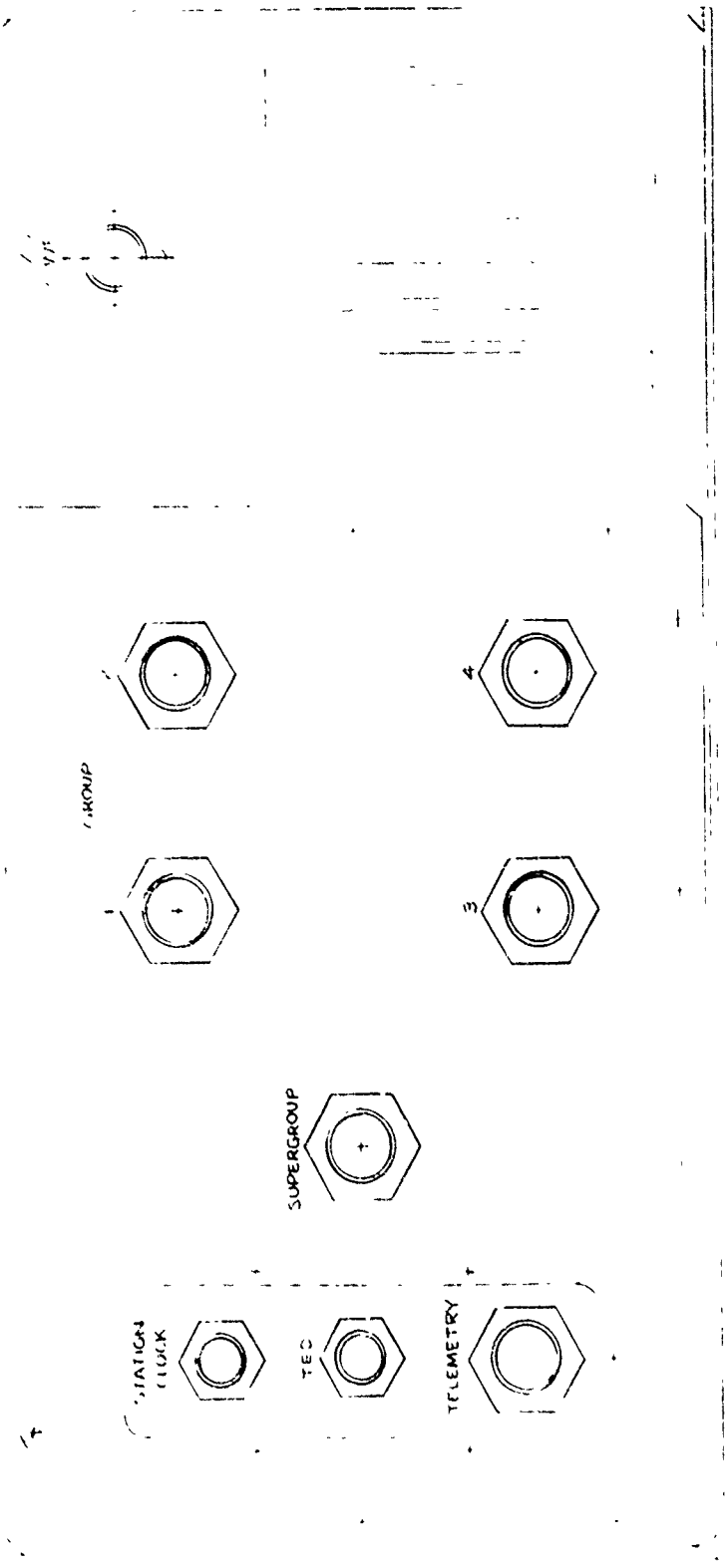


Figure 8-11. TGM Rear View

SECTION 9

MASTER GROUP MULTIPLEXER

9.1 DESIGN GOALS AND REQUIREMENTS

The Master Group Multiplexer (MGM) provides versatile digital transmission capability by asynchronous combining of up to 12 group or supergroup inputs into a mastergroup output, and decombining of a mastergroup input into its constituent groups and supergroups. The MGM operates asynchronously in that it is capable of accepting inputs which have not been slaved to a single timing source. Group and supergroup inputs (data and timing) range from 0.072 to 4.9152 Mb/s with a maximum aggregate input rate of 18.432 Mb/s when the output mastergroup rate is 18.720 Mb/s, or a maximum aggregate input rate of 9.216 Mb/s when the output mastergroup rate is 9.360 Mb/s.

The MGM will allow inputs in any combination subject to the aggregate traffic limit. In addition the MGM will accept most permutations of any possible input rate combination.

Two digital orderwire channels are provided in the MGM. Both channels are bit synchronous to the multiplexer clock and each may operate at 16 or 32 kb/s, switch selectable.

Transmit multiplex timing for the MGM is obtained from:

a. External station clock at 32 kHz or 16 kHz

b. Receive mastergroup timing

c. Internal clock with stability of not less than 5 ppm

The MGM is capable of accepting a control signal which when set inhibits frame search on the receive mastergroup.

An input/output diagram of the MGM is shown in Figure 9-1.

A summary of electrical design requirements is given in Table 9-1. Table 9-1a lists the nominal group rates. Table 9-1b lists the characteristics of the balanced digital interface for the group, mastergroup, and orderwire signals.

TABLE 9 1

MGM REQUIREMENTS

Mastergroup Rate	18.720 Mb/s or 9.360 Mb/s; operator selectable
Mastergroup Interface	Balanced NRZ and timing
Number of Groups	Up to 12 separate groups, not slaved to single timing source
Group Rate	72 kb/s to 4915.2 kb/s as shown in Table 9-1A
Group Interface	Balanced NRZ and Timing
Group Throughput	Total aggregate bit rate of all groups not to exceed 18.432 Mb/s (9.216 Mb/s) at 18.720 Mb/s (9.360 Mb/s) mastergroup rate.
Bit Stuffing	Maintain bit count integrity for not less than 24 hours for input bit streams having a stability of 3×10^{-5} in a 0.1% BER random error environment.
Timing	Transmit timing from station clock at 16/32 kHz, receive mastergroup, or internal clock at 5 ppm stability.
Framing	Acquire within 20 milliseconds with 0.9 probability in 0.1% BER random errors. Maintain for not less than 24 hours with minimum probability of 0.9 in 0.1% BER random errors. Detect frame loss within 100 milliseconds with minimum probability of 0.9. Inhibit frame search upon external command.
Telemetry Orderwire	16/32 kb/s synchronous balanced NRZ and timing
Voice Orderwire	16/32 kb/s synchronous balanced NRZ
BITE	Locates equipment faults to a replaceable subassembly.
MTBF	4000 hours
Power	120 Vac, 50 to 400 Hz, or 28 Vdc Battery, 100 watts input
Size	14" H x 12" D x 19" Rack Mount
Weight	20 Kg

TABLE 9-1a

MGM NOMINAL GROUP RATE INPUTS (KHZ)

72	1024.0
128	1152.0
144	1536.0
256	2048.0
238	2304.0
512	4096.0*
576	4608.0*
	4915.2*

*The MGM does not operate with these group rate inputs for low rate mastergroup (9.36 Mb/s) operation.

TABLE 9-1b

BALANCED DIGITAL INTERFACE SIGNAL CHARACTERISTICS

Driver Characteristics	
Minimum Line-to-Line Voltage	+87 mV for digital "1", -87 mV for digital "0" measured at end of 100 feet of RG-108 cable, terminated in 100 ohms. Voltages balanced to ±10%.
Maximum Output Voltage	±3 volts either line-to-ground. ±4 volts line-to-line into 100 ohms.
Rise and Fall Times	Mastergroup: 8 ns maximum Group: 30 ns maximum Orderwire: 270 ns maximum
Clock	Half bit interval with following tolerance: Mastergroup: ±4 ns Group: ±15 ns Orderwire: ±120 ns
Clock/Data Phasing	Negative to positive clock transition is followed by data transition. Allowable delays are: Mastergroup: ±8 ns Group: ±29 ns Orderwire: ±240 ns
Receiver Characteristics	
Sensitivity	50 mV.
Impedance	100 ohms ±10% line-to-line.

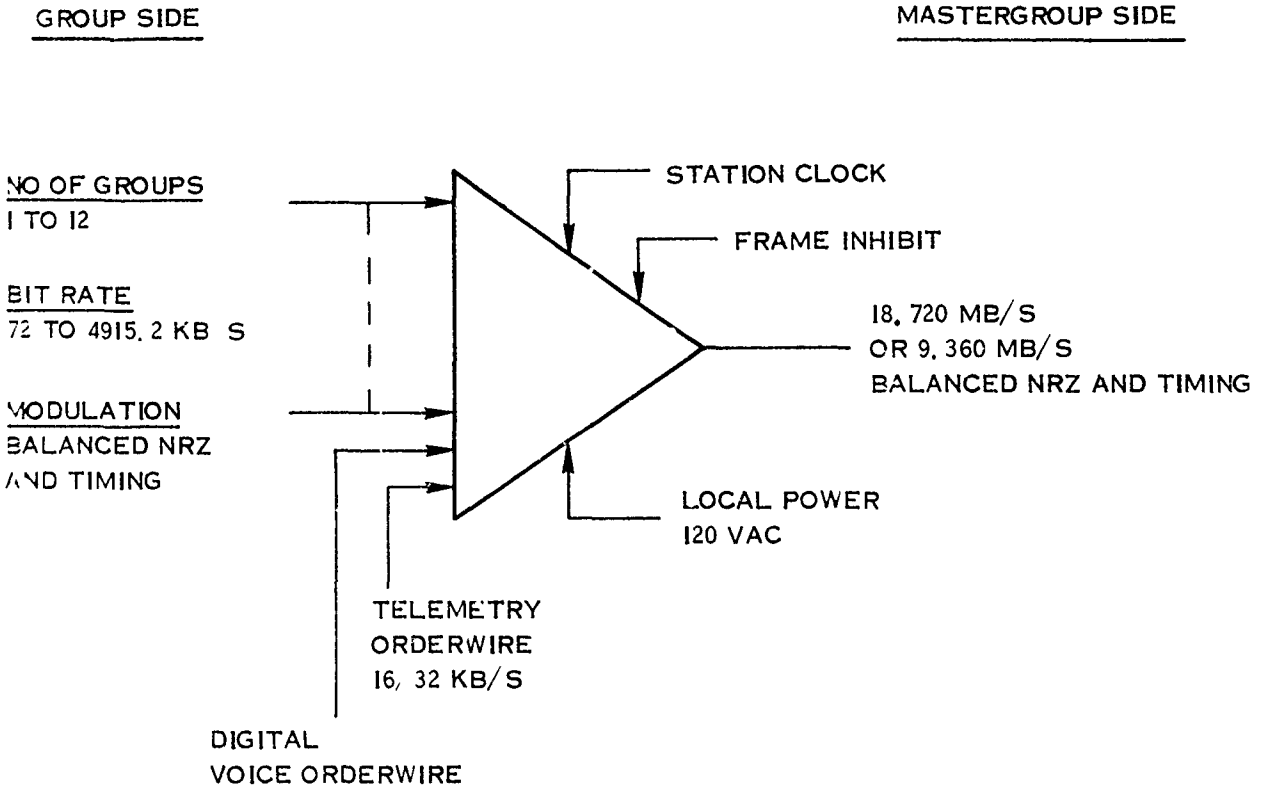


Figure 9-1. MGM Input/Output Diagram

9.2 DESIGN APPROACH

9.2.1 ASYNCHRONOUS COMBINING

The MGM processes group or supergroup inputs which are not slaved to a single timing source. Hence, data to be multiplexed must first be justified with respect to the multiplexer clock by the addition or deletion of bits before being synchronously interleaved. Positive justification or pulse-stuffing synchronization results when input data is brought into synchronization by the addition of bits. Negative justification or pulse spilling results when the input data is brought into synchronization by the deletion of bits. A combination of positive and negative justification can be employed to synchronize an incoming data stream at a rate equal to its nominal value.

The locations of the stuff bits and/or the locations and values of the spilled bits must be signalled to the demultiplexer via an overhead channel in order to properly reconstitute the demultiplexed channel. Special care must be

exercised in signalling a stuff or spill because an error in decoding this information will violate the bit count integrity of the associated channel. Hence, this information is redundantly coded to provide a known level of protection over a specified time interval in a specified error environment. The identity of the channel being justified is determined by the location of the signalling message with respect to a framing signal.

The elastic store is the hardware mechanism by which an incoming bit stream is rate justified. It serves as a buffer between the incoming bit stream and the transmission rate allotted by the multiplexer. If the incoming rate is higher, then elastic store occupancy increases by a bit or more until a bit can be spilled into and conveyed by the overhead channel. A spill message must first be signalled to the demultiplexer so that it can route the spill bit into the outgoing channel bit stream at its correct location.

Conversely, if the incoming rate is low relative to the transmission rate allotted by the multiplexer set, then elastic store occupancy decreases by a bit or more until the equipment allows a pre-arranged multiplex time slot to pass wit out using a bit from the elastic store. The resulting bit thus transmitted in the traffic channel has no information value and is denoted a stuff bit. The demultiplexer must be signalled in advance via the overhead channel to reject the stuff bit.

An elastic store is also required on the outgoing equipment group interface to smooth out the rate discontinuities at which data is read into the store. Data is read into the store from both the traffic channel and from the overhead channel. Stuff bits conveyed via the traffic channel are not read into the buffer whereas spill bits conveyed via the overhead channel are read in. Hence the read-in rate tends to be somewhat irregular even though strict bit count integrity is maintained. The function of the outgoing side store is to provide nearly uniform and continuous readout of the group data by using the occupancy of the buffer to control a VCXO in a phase locked loop arrangement.

On the order of three bits must be allotted to the elastic stores for variations in occupany inherent in the technique of spilling and stuffing. Additional factors are dependent on the overhead channel format, the multiplex frame length, tandem operation, and the regularity of assigned time slots to a particular channel. For the chosen approach a store size of 8 bits appears adequate.

9.2.2 MULTIPLEX FRAME

A most basic electrical characteristic of the MGM is its frame format. This determines its traffic handling capability, both in total throughput rate and flexibility of rate assignment, synchronization time, resistance to loss of bit integrity, and the circuit complexity.

The first consideration regards rate multiplicity The frame length must be such that each possible rate may be allotted an integer number of time slots in the frame, to satisfy the requirement that the MGM accept inputs in any combination subject to the aggregate traffic limit. The number 11700 is the smallest frame length (at the high mastergroup rate) for which each of the possible input rates can be allotted an integral number of bits in the frame. Table 9-2 lists the number of times the number of required time slot assignments per frame for each of the specified input rates.

TABLE 9-2

REQUIRED BITS/FRAME FOR EACH INPUT RATE

Rate Mb/s	Required Bits/Frame @ 11700 Frame Length	
	18.72 Mb/s	9.36 Mb/s
0.072	45	90
0.128	80	160
0.144	90	180
0.256	160	320
0.288	180	360
0.512	320	640
0.576	360	720
1.024	640	1280
1.152	720	1440
1.536	960	1920
2.048	1280	2560
2.304	1440	2880
4.096	2560	
4.608	2880	
4.9152	3072	

Of the 11700 bits in a multiplex frame, 11520 are allotted to traffic channels (corresponding to an aggregate traffic rate of 18.432 Mb/s for a mastergroup rate of 18.720 Mb/s) and 180 are allotted to overhead. The overhead must include voice orderwire and telemetry orderwire (each of which require an allotment of 40 bits to provide 32 kb/s at the low mastergroup rate), stuff/spill indicator words and spill bit location for one or more channels, and framing bits.

The stuff/spill or justification messages employ signalling in which the position of the signalling code relative to a frame code provides an indication of the channel being justified. Since there are up to 12 channels to be multiplexed, 12 separate locations must be periodically identified. In the selected format six justification messages are located in every multiplex frame. The term "major frame" or "control channel frame" is used to designate two multiplex frames. Thus, the signalling format repeats once, and the traffic format twice every major frame.

It is also convenient to divide the 11700 bit multiplex frame into nine equal length blocks. Each 1300 bit block allots 1280 bits to traffic channels and 20 bits to overhead. Regardless of the mix of input rates, the data formats will repeat every nine blocks, or one multiplex frame.

9.2.3 OVERHEAD FORMAT

The rationale for the selection of the overhead format is discussed in this section. The traffic channel interleaving arrangement is presented in the next section.

Details of the arrangement of the 1300-bit blocks which comprise the 11700 bit multiplex frame are shown in Figure 9-2. The nine blocks in each multiplex frame are transmitted in the order 1, 2, 3, ..., 9, 1, 2, ... Transmission of two multiplex frames, odd and even, comprises a major frame.

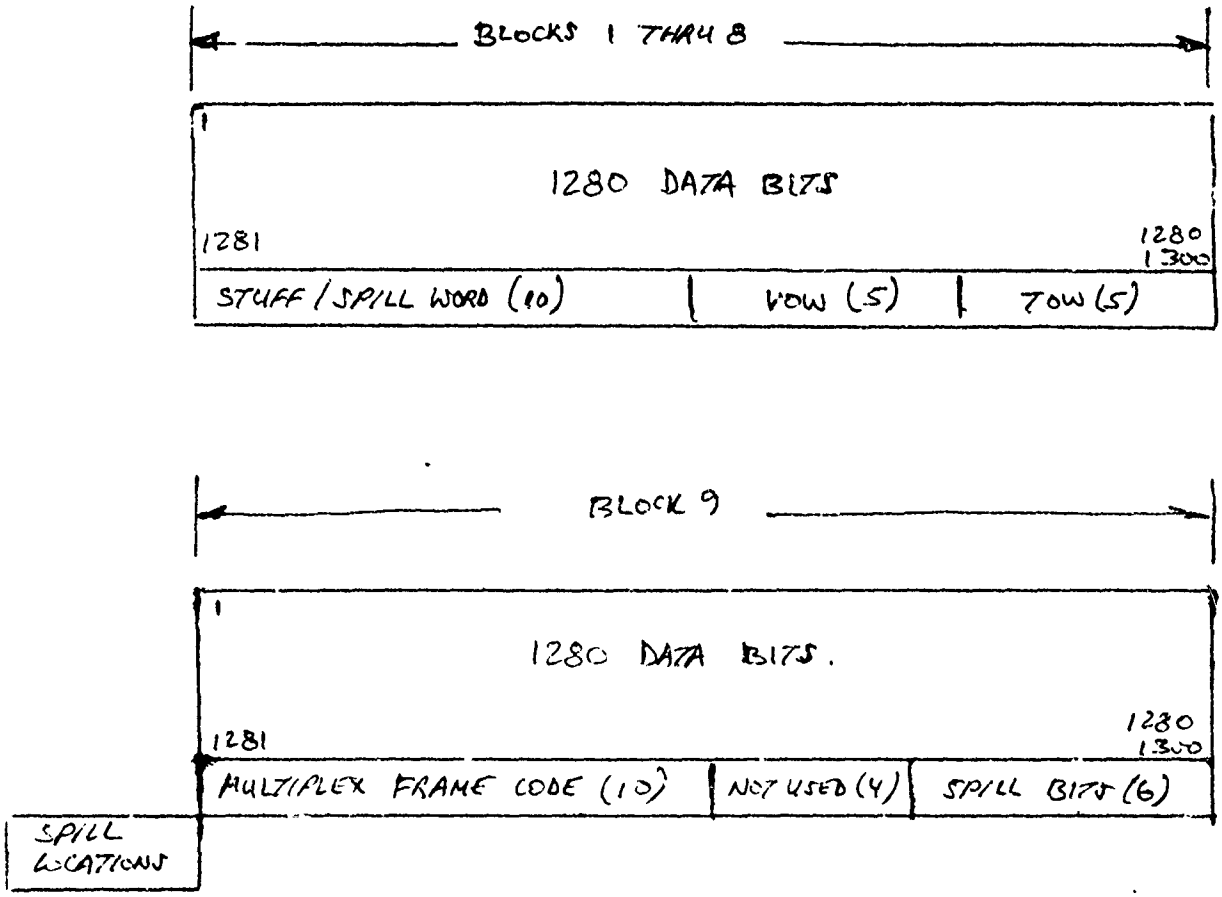
The 20 overhead bits of blocks 1 through 8 contain a 10 bit stuff/spill indicator word, a five bit digital voice orderwire word (VOW), and a five bit telemetry orderwire word (TOW). The stuff/spill words serve two functions. During

equipment frame-in the ten bit code or its complement is used to acquire block synchronization. Thereafter, seven bits of the stuff/spill word are majority decoded to indicate whether a stuff or spill has been signalled. With regard to spill bits, note that only the spill indicator message, i.e., information that a spill will occur in the future, is signalled in these blocks. The actual spill bits, if any, are signalled in block nine. Stuff/spill indicator words for six channels are signalled in each multiplex frame. The indicator words for channel one are signalled sequentially in blocks one through six for odd multiplex frames. The indicator words for channels 7 through 12 are signalled in blocks one through six for even multiplex frames.

The VOW and TOW bit allotment provides a 16/32 kb/s capability for both channels at the high or low mastergroup rate. Thus, at the high mastergroup rate only alternate even numbered blocks 2, 4, 6, 8 will contain valid VOW or TOW data words when the corresponding orderwire channel operates at 32 kb/s. An orderwire channel at 16 kb/s will utilize blocks four and eight. At the low mastergroup rate a 32 kb/s orderwire channel will utilize all its allotted time slots in blocks one through eight, and a 16 kb/s channel will utilize alternate even numbered blocks 2, 4, 6, 8.

The overhead segment of block nine differs in format from the other blocks. It begins with a ten bit multiplex frame code which is complemented in alternate multiplex frames. Bits 11 through 14 are not used. Bits 15 through 20 are spill bit slots. Bit 15 is the spill bit slot for channel one in odd multiplex frames, and is the spill bit slot for channel seven in even multiplex frames, etc. Figure 9-2 also indicates the logical location of bits deleted by the multiplexer (spill bits) which are to be reinserted by the demultiplexer. All spills for a given multiplex frame are executed simultaneously at the end of block nine at a time when no readout occurs at any channel buffer. This event occurs once per multiplex frame and is used to define the end of block nine. This procedure is used because it limits the maximum required operating speed of any channel elastic store to approximately 10 Mb/s. Any stuff bits signalled in blocks one through six are also located in block nine. The stuff bit is the first occurrence of that channel in the following block.

BLOCK : 1280 DATA BITS + 20 OVERHEAD BITS
MULTIPLEX FRAME : 9 BLOCKS (11700 BITS)
MAJOR FRAME : 2 MULTIPLEX FRAMES.



NOTES :
VOW : 5-BIT ALLOCATION FOR DIGITAL VOICE ORDERWIRE
TOW : 5-BIT ALLOCATION FOR TELEMETRY ORDERWIRE
MULTIPLEX FRAME CODE IN OVERHEAD SEGMENT OF BLOCK 9 TOGGLES ON ALTERNATE MULTIPLEX FRAMES.

Figure 9-2. Multiplex Format

Stuff, spill, and multiplex frame patterns are based on a ten bit Williard code as shown below. In each case the right-most bit is transmitted first.

STF:	0 0 0 0 1 1 1 0 1 1
SPL:	1 1 1 1 0 0 0 1 0 0
MFC:	1 1 0 1 1 1 0 0 0 0
$\overline{\text{MFC}}$:	0 0 1 0 0 0 1 1 1 1

9.2.3.1 Permissible Rate Variations

Per specification, input rates may differ from nominal by $\pm$30 parts per million (ppm). In addition, the internal clock of the MGM has a stability of $\pm$5 ppm.

The permissible rate variation between the multiplexer timing and that of the channel inputs is determined by the number of justification (stuff/spill) opportunities available to each channel per unit of time. The overhead channel described above provides one justification opportunity per channel in each major frame (two multiplex frames).

The multiplex frame rate at the low mastergroup rate is 800 frames/sec. thus the minimum signalling rate per input channel is 400 Hz. This is 81 ppm of the highest input rate (4915.2 kb/s) and hence is fully adequate to meet stuff/spill demands, i.e., $\pm$81 ppm capacity versus $\pm$30 ppm maximum input deviation from nominal for the input data and $\pm$5 ppm permissible mastergroup clock offset.

9.2.3.2 Bit Count Integrity

Per specification, bit count integrity (BCI) is to be maintained for not less than 24 hours in an error environment of 0.1 percent BER random errors.

Maintenance of BCI depends on correctly decoding the stuff/spill indicator words in the overhead channel. Seven bits of the 10 bit stuff/spill indicator words are decoded to determine if a stuff or spill is being signaled. If an indicator word is incorrectly decoded then BCI for the associated channel will be lost. At a 10^{-3} error rate the probability of incorrect decoding (four or more errors in the seven bit word) is 3.5×10^{-11}. The signalling rate per input channel at the high intergroup rate is 800 per second.

Hence, the mean time to loss of BCI per input is on the order of:

$$\frac{1}{3.5 \times 10^{-11}} \frac{\text{trials}}{\text{failure}} \times \frac{1}{800 \text{ trials/sec.}} = 3.5714 \times 10^{7} \text{ sec./failure}$$

The probability distribution of this event can reasonably be assumed to be Poisson. Hence it is of the form $1\text{-}e^{-x/m}$ where X is the desired observation time (24 hours or 8.64×10^{4} sec.) and $m = 3.5714 \times 10^{7}$. The probability of losing BCI over a 24-hour interval is then:

$$\frac{X}{M} = \frac{8.64 \times 10^{4}}{3.5714 \times 10^{7}} = 0.0024$$

Hence the probability of maintaining BCI over a 24-hour interval is 0.9975.

9.2.3.3 Framing

The framing specification for the MGM requires that frame be acquired within 20 milliseconds, with a minimum probability of 0.9, and be maintained for not less than 24 hours with a minimum probability of 0.9, in an error environment of 0.1 percent BER random errors. Loss of frame is to be detected within 100 milliseconds with a minimum probability of 0.9.

The choice of codes should be such that it tends to minimize the probability of false sync indication when part of the code is in the frame sync detector. Williard codes are optimum synchronization codes in this sense and are used for stuff, spill, and multiplex frame codes (MFC).

The framing process utilizes the stuff/spill words in blocks 1-8 and the multiplex frame code or its complement in block 9. To establish frame, a detector attempts to define a frame in the incoming mastergroup data stream by taking samples from the stream and comparing the samples with an acceptable frame pattern. The frame detector during acquisition accepts as a valid frame pattern the stuff or spill code, or the multiplex frame code or its complement. The probability of a random data sample matching an acceptable frame pattern on any such trial is then $4 \times (\frac{1}{2})^{10}$.

When such a ten bit pattern matches an acceptable frame code, then a block frame counter is released and the candidate frame is tested again one block later. If ten consecutive samples match, the detector locks. In addition, when the MFC or $\overline{\text{MFC}}$ is detected, then a multiplex frame counter is appropriately set. This will decrease the overall frame-in time because as block frame is established, multiplex frame is tested at least once.

A flow chart of the framing process is shown in Figure 9-3.

We may now define the following parameters:

N = number of bits between framing patterns = 1300

m = number of tests required to achieve lock = 10

Pf = probability of a random data sample matching an acceptable frame code = $\left(\frac{1}{2}\right)^8$ = 0.003906

Qf = 1 - Pf = 0.9960937

P_e = Probability of error in the frame code bit = 10^{-3}

P_E = probability of error in the frame code word sample = 1 - $(0.999)^{10}$ = 0.009955

a = delay to next test after an acceptable sample = 1300 bits

b = delay to next test after an unacceptable sample = 1 bit

Lock-in time depends on how many bits, K, one starts from the frame location. A minimum of b-K bits is required to shift through the frame; the mth test will be passed a(m-1) bits later. Thus a minimum of a(m-1) + b x K bits is required to achieve lock. A practical upper bound on the time to lock is obtained by setting K to its maximum ($K_{max.}$ n - 1 1299) and evaluating the minimum delay plus the mean plus three times the deviation. This conservatively establishes the frame-in time with probability of 0.95. The mean and deviation are evaluated from a flow graph analysis of the framing process.

Maximum Delay MDLY a(m - 1) + bK bits

MEAN Ka P_F + λ_1 bits

λ_1 m P_F [nb + a($\frac{m-1}{2}$ + (n-K-1) $\frac{P_F}{Q_F}$] bits

DEV [a K $\frac{P_F}{Q_F}$ + λ_1^2 + 2 λ_1 Ka $\frac{P_F}{Q_F}$] bits

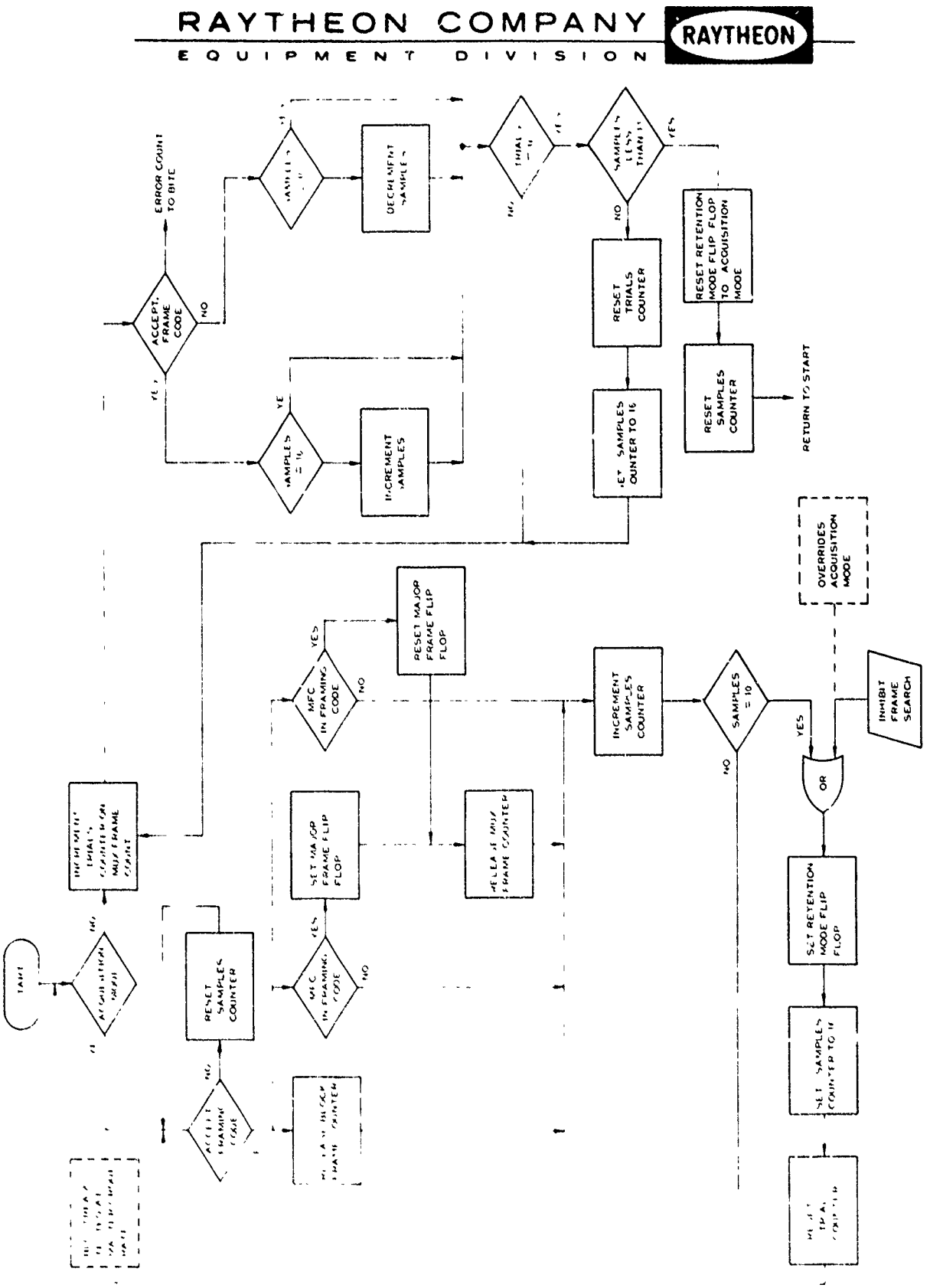


Figure 9-3. MGM Framing Flow Chart

FRAME-IN = MDLY + MEAN + 3DEV evaluated at K = n-1.

Substituting in numerical values:

$$MDLY = 12990_1\ \lambda_1 = 71.5,\ MEAN = 6622 \text{ and } DEV = 3097$$

The Frame-in then equals 2.8912×10^4 bits which at the low mastergroup rate of 9.36 mb/s requires 3.09 milliseconds. This is the time to establish block frame. During that time there is at least one sample of the multiplex frame code (MFC or $\overline{MFC}$). If we require an additional seven samples to verify the MFC, then at the low mastergroup rate an additional $7 \times 1.25 = 8.75$ milliseconds are required. The total frame-in time is then 11.84 milliseconds.

Once frame has been acquired, the multiplex frame code is monitored to detect loss of frame. A straightforward scheme is to count the number of times that the frame code is received in error in some sample of N occurrences of the frame code. If this number equals or exceeds a threshold, then loss of frame is declared. A convenient sample size is N=16. The probability that in 16 trials, we will not receive 11 or more successful frame code indications in a bit error environment of 10^{-3} is less than 10^{-9}.

The mean time for an error indication at the high mastergroup rate is then:

$$m = \frac{1}{10^{-9}} \frac{\text{trials}}{\text{failures}} \times 11700 \frac{\text{bits}}{\text{frame}} \times \frac{1}{18.72} \times 10^6 \frac{\text{sec.}}{\text{bit}}$$

$$\times\ 16 \frac{\text{frames}}{\text{trial}}$$

$$m = 10^7 \text{ sec./failure}$$

The probability of losing frame over a 24-hour interval (8.64×10^4 sec.) is then $8.64 \times 10^4 / 10^7 = 0.00864$.

Hence, the probability of maintaining frame sync over a 24-hour interval at 10^{-3} bit error rate is 0.991.

On the other hand, when frame is truly lost, the probability that the "frame code" is in error is 7/8 so that simulating the frame code in 11 or more of 16 trials has a low probability. Loss of frame can then be detected within 8 milliseconds, i.e., frame loss happens during one 4 millisecond test interval and is detected during the next test interval.

9.2.4 INTERLEAVING ARRANGEMENT

The MGM in its combining function must interleave bits from up to 12 input channels. Each channel may have any one of 15 pre-designated rates (12 at the low mastergroup rate) subject to the restriction that the sum of the input rates may not exceed 18.432 Mb/s for the 18.72 Mb/s output rate or 9.216 Mb/s for the 9.36 Mb/s output rate.

The number of appearances required by each rate in each multiplex frame of 11700 bits is determined by the frame rate of 1600 per second at the 18.72 Mb/s output rate and 800 per second at the 9.36 Mb/s output rate. These numbers are shown in Table 9-2. We might also note that the number of appearances per block of 1300 bits is not necessarily an integer number. For example, at the high mastergroup rate an input at 4.096 Mb/s requires 2560 bits in the frame or an average of 284 4/9 bits/block. Some blocks will have 284 bits and others will have 285 in the ratio 5/9 and 4/9, respectively.

Requirements for the interleaving scheme are:

a. The interleaving scheme must result in a channel assignment for every time slot in the multiplex frame. The "channel" may, in fact, be the overhead channel, or the null channel. The latter are filler bits which represents no channel and exist because the aggregate traffic rate may exceed the sum of the input rates that have been assigned to each channel. Filler bits simply make up for the excess bit capacity of the output when it is not fully utilized by the assigned rates.

b. Interleaving should result in a repetetive data pattern in each multiplex frame.

c. Interleaving should result in as uniform a distribution of bits from each channel within a block as is possible. This simplifies timing recovery and minimizes the size of the channel elastic store.

d. Interleaving should be simple to implement and require little power.

One approach to multiplex time slot assignment is to compute the interleaving format for a desired rate assignment and store it in random access memory (RAM) for subsequent use during multiplexing and demultiplexing. Several schemes were developed which allow easy computation of the required time slots to be assigned each channel and provide a reasonably uniform distribution of the time slots assigned to any channel.

The problems with this approach are the required RAM size, its operating speed, and its power consumption. A straightforward allocation requires a 11700 x 4 bit RAM for both the multiplexer and the demultiplexer. That is, each of the 11700 time slots in the multiplex frame be allotted a four bit channel address. If data assembly is serial bit-by-bit, then this memory must be accessible at a 18.72 Mb/s rate. Only ECL RAM's such as the 256 x 1 bit SN10144 have access times commensurate with the high mastergroup rate. Each format memory would require 184 of these devices and dissipate 96 watts.

The required RAM access rate could be reduced by accessing the channel address for a number of time slots simultaneously. If we were to access four channel addresses in parallel, the memory organization would be $\frac{11700}{4}$ x (4 x 4). The access rate would then be under 5 MHz so that 1024 x 1 bit RAM devices could be used. Each format memory would then require 48 storage devices and dissipate on the order of 28 watts.

Considering the required power, the above approach is only feasible if the frame can be made shorter, and data assembled in multi-bit packets. The frame can only be made shorter if some channel rates are synchronously rate converted to a rate such that the required number of bits/frame for the entire amended rate family is divisible by a common integer.

For example, with reference to Table 9-2, one may note that with three exceptions, at the high mastergroup rate, the required number of bits/frame are each divisible by eight. The three exceptions are the rates 0.288, 0.144, and 0.072 Mb/s. Suppose the multiplex frame length were reduced by a factor of four to 2925 bits and data assembled in four bit packets. Two 1024 x 4 bit format RAM's would then be required. Each need be accessible at just under 5 MHz and would require about 2.5 watts. From the standpoint of format memory power consumption, this is a desirable approach. There are, however, some disadvantages and penalties.

a. With respect to the rate exceptions the 0.288 Mb/s rate can be treated as though it were 0.384 Mb/s by reading in a three bit word into the channel elastic store and reading out a four bit word at a rate commensurate with 0.384 Mb/s. Every four bit output word will then have one filler bit in a fixed location due to the synchronous rate conversion. The 0.144 Mb/s rate can be processed in an identical manner by treating it as though it were 0.192 Mb/s. There is no similar easy way to handle the 0.72 Mb/s rate for the high rate mastergroup case; hence, it would be an allowable input only for the low rate mastergroup. Hence, these rate exceptions restrict flexibility of rate assignment in the MGM. At the high mastergroup rate 0.072 Mb/s would not be an allowable input, each occurrence of 0.288 Mb/s would reduce the allowable aggregate traffic rate by 0.096 Mb/s, and each occurrence of 0.144 Mb/s would reduce the allowable aggregate rate by 0.048 Mb/s.

b. The channel elastic stores increase in complexity in order to format a four bit data packet. The extent of this increase may be a doubling for that portion of the channel circuit which directly concerns the elastic stores. In addition, if data is assembled in four bit packets, it may also be necessary to perform stuffs and spills in four bit packets. This, in turn, makes timing smoothing on the receive side more difficult.

The above mentioned disadvantages associated with a feasible size format memory led to consideration of dynamic allocation of multiplex time slots to the various channels. In this approach, we synthesize the precise nominal required

readout rate, synchronous to the mastergroup clock, as shown in Figure 9-4. A scanner clock equal to the aggregate traffic rate is generated by deleting four consecutive mastergroup clock pulses in every group of 260. The scanner clock is then divided down as shown to generate a full complement of possible read-out rates. In some cases the divider modulus is varied repetitively to obtain a non-integer divider. For example the 18.432 MHZ scanner clock is divided by 3 for one cycle followed by three cycles of divide by 4 to obtain the 4.9152 MHZ rate. The selected readout rate for each channel is routed to a priority scanner circuit which operates at the maximum allowable aggregate input rate (18.432 or 9.216 Mb/s).

In the priority scanner circuit a particular channel is serviced when its generated nominal readout (multiplex side) or read-in (demultiplex side) clock makes a transition during a scanning interval. Only one channel is serviced during each scan interval. If two or more channels simultaneously demand service, then the request at the lowest port number is given priority and other requests remain pending. If no channel demands service during the scan interval, then by default the null channel is "serviced" by the creation of a filter bit. This is not a stuff bit and is automatically deleted by the demultiplexer as a consequence of its inverse logic.

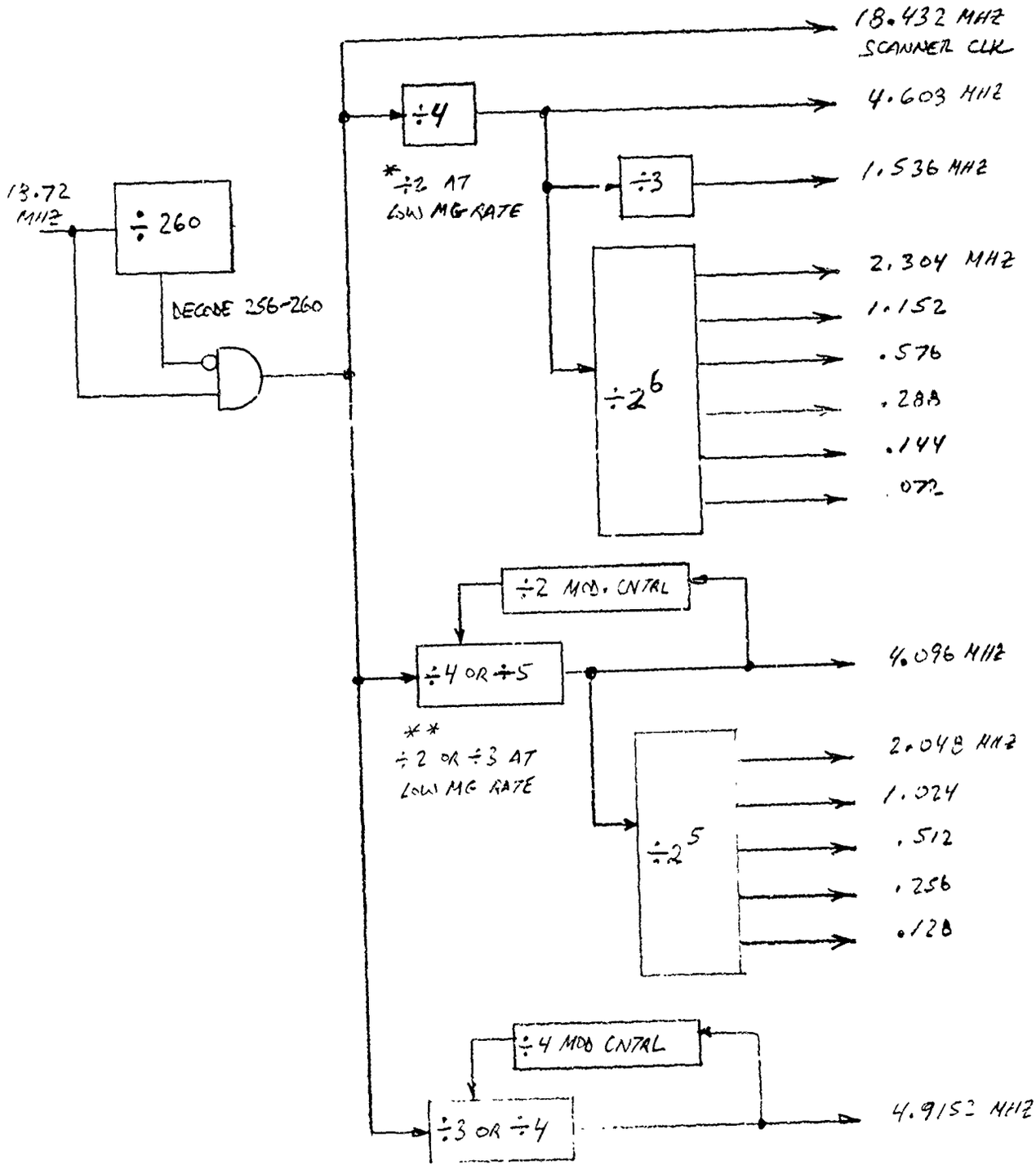


Figure 9-4. Readout Rate Synthesis

Dynamic allocation of the multiplex time slots as described above is the chosen approach because:

a. No frame format memory is required to store a channel address for every time slot in the frame.

b. Time slots allocated to each channel on the basis of its rate requirements are nearly uniformly distributed, within the constraints of higher rate channels competing for a given time slot. However, the non-uniformity in the readout clock spacing will not exceed one clock interval of the nominal readout rate.

c. The channel elastic stores do not see the block asymmetry in the multiplex frame format because the priority scanner operates at the aggregate traffic rate, not the mastergroup rate. This factor, coupled with the nearly uniform distribution of store read-out or read-in clocks, allows the channel elastic stores to be of minimum size compared with other schemes.

One disadvantage of this approach is the required operating speed, 18.432 Mb/s, of the scanner circuit. Multiple scanner circuits, each operating at a submultiple of the 18.432 Mb/s rate could be used if the resultant decrease in flexibility of rate assignment were acceptable.

9.2.5 RECEIVE CHANNEL TIMING SMOOTHING

Receive channel timing smoothing follows the method presented in the proposal wherein a detailed comparison of various timing recovery schemes was presented. Figure 9-5 indicates the chosen approach. The timing synthesizer uses a 4.096 MHz $\pm$47 ppm voltage controlled crystal oscillator (VCXO) as a local oscillator. The control voltage to the VCXO is a TTL logic level so that the resultant output frequency is essentially at either of two frequencies:

4.096 MHz + 47 ppm or 4.096 MHz - 47 ppm.

The 4.096 MHz output of the VCXO may be used directly for one of the required rate families. For the 4.9152 MHz rate the VCXO output is mixed with the 9.0112 MHz i-f and the difference frequency recovered in a crystal filter. The 4.608 MHz rate family uses the 8.704 MHz i-f mixed with the 4.096 MHz VCXO output and a second crystal filter. The VCXO or filter output is applied to a timing

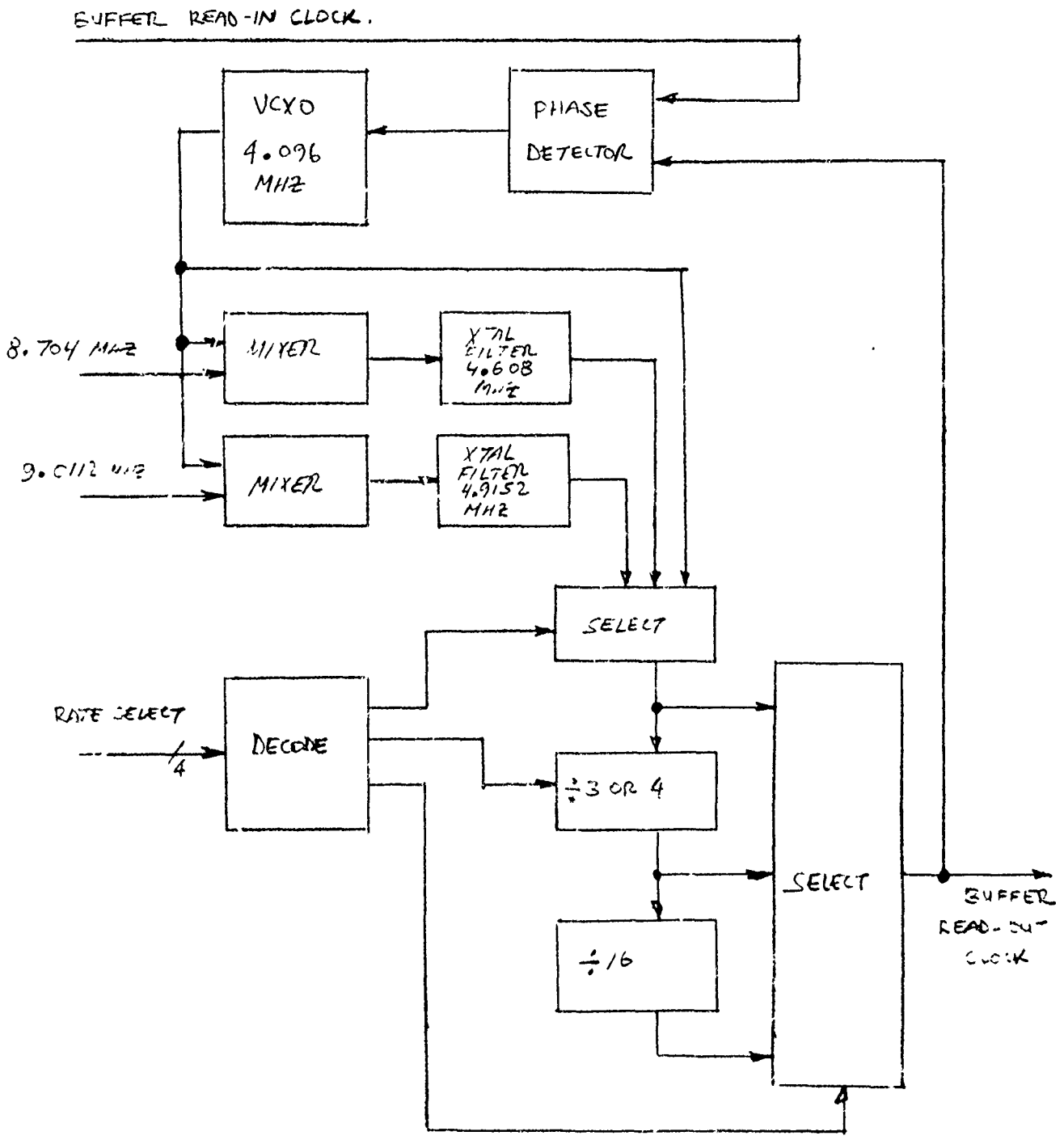


Figure 9-5. Receive Channel Timing Smoothing

countdown chain and the appropriate output is used as the read out clock for the channel buffer store. The occupancy of the buffer store is monitored in a phase detector whose digital output drives the VCXO. Heterodyning allows operation at multiple rates while also allowing the control oscillator to operate at essentially one frequency. The frequency swing of the VCXO is wide enough to accommodate the frequency tolerance of the group inputs and the mux clock and narrow enough (because there is no overshoot) to feed crystal filter repeaters. Energy storage in the oscillator tank prevents phase discontinuities; hence, the output phase is a smooth function of time.

Elastic store occupancy changes of ± 3 bits might be expected due to stuffing and spilling bits plus queueing of requests at the scanner logic. The time jitter of the output data and clock will occur at a rate of approximately one bit per 10^4 bit times with a peak-to-peak amplitude nearly equal to the peak-to-peak occupancy swings in the elastic store. Therefore, Group Modems or CDM's connecting to MGM channels must be operated with the MGM channel output clock not station clock. The TGM can accept an MGM channel signal using the elastic store on its inputs to absorb any jitter relative to station clock.

9.2.6 UNIT ORGANIZATION

Figures 9-6 and 9-7 illustrate the transmit and receive functional organization of the MGM. Figure 9-8 indicates the unit organization in terms of its module complement. The unit consists of channel circuits, common circuits (transmit and receive), orderwire logic, BITE, and power supply.

Each channel card contains circuits for both the transmit and receive functions. These include interface circuits, transmit and receive rate buffers, receive timing smoothing, and rate selection. Input data and timing, interfaced to TTL logic levels, from each channel card are routed to the BITE circuits which monitor activity. As a typical BITE activity, the BITE circuits compares, for each channel, the readout timing (transmit) with the incoming timing, and the read-in timing (receive) with the outgoing timing to check for agreement over a test time interval.

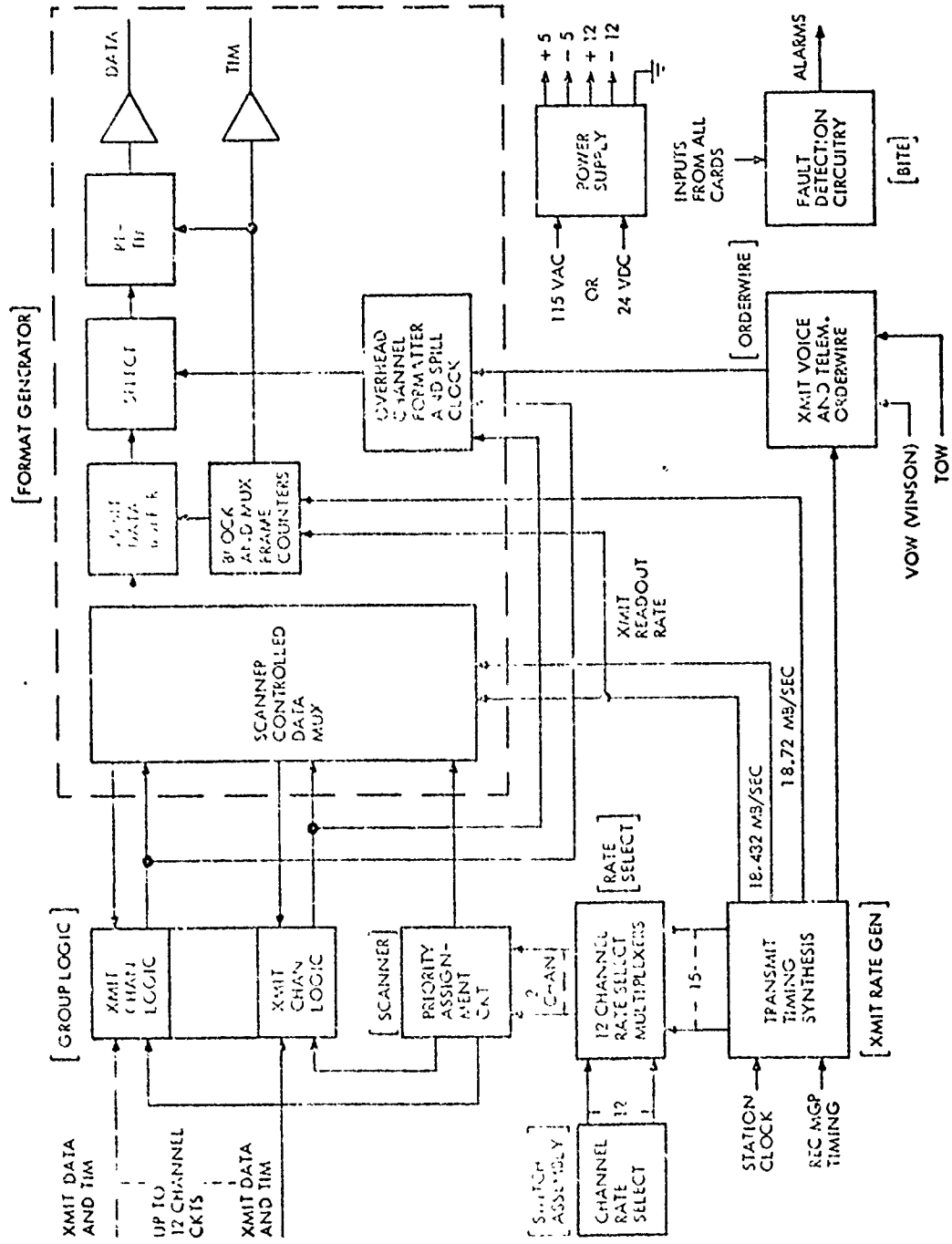


Figure 9-6. MGM Multiplex Block Diagram

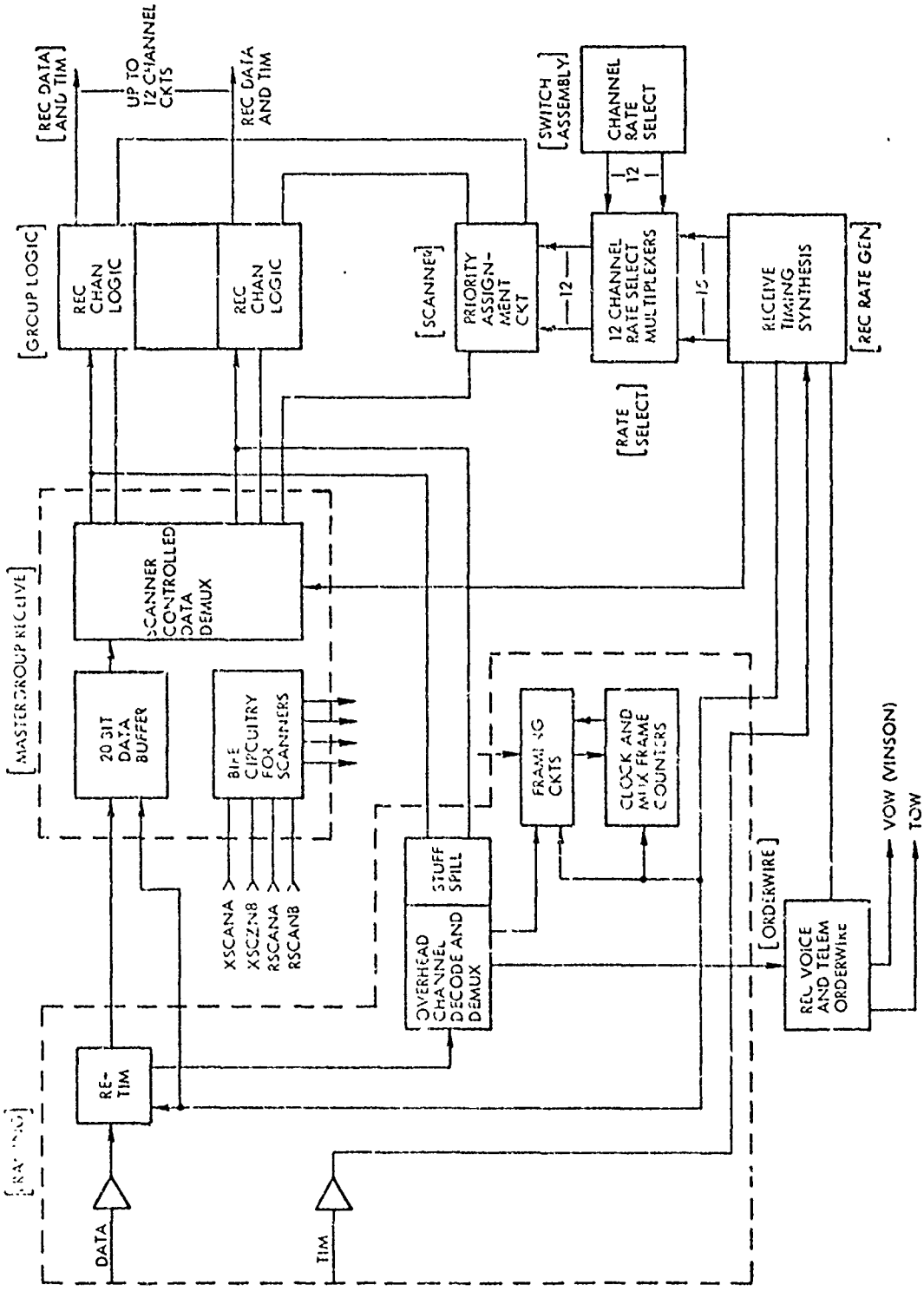


Figure 9-7. MGM Demultiplex Block Diagram

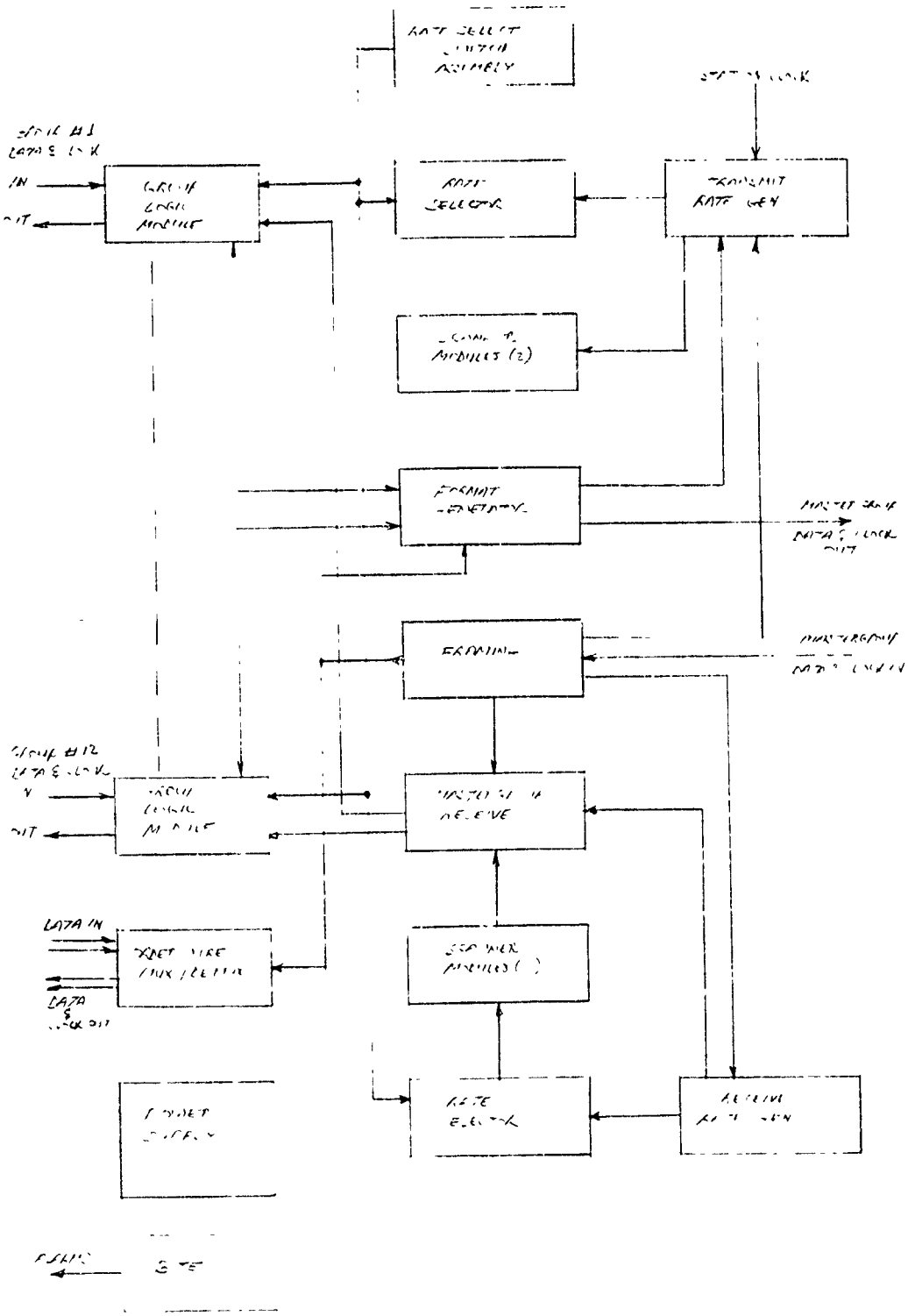


Figure 9-8. MGM Functional Block Diagram By Module

Transmit common circuits consist of a timing synthesizer, scanner controlled data multiplex, overhead channel message composer, a 20 bit high speed buffer, counter timing chains to define the 1300 bit block frame and nine block multiplex frame, and driver interface circuits. The timing synthesizer generates all of the possible nominal readout rates which the channel circuits may use. The scanner generates a repetitive sequence of addresses over a frame interval based on the desired mix of traffic rates to control a data multiplexer.

The data multiplexer is operated at the aggregate traffic rate, 18.432 Mb/s when the mastergroup rate is 18.72 Mb/s, and feeds a 20 bit data buffer. This buffer is in turn read-out at the mastergroup rate for 1280/1300 of each block frame. Each time that the block frame counter reaches a count of 1280, the contents of the data buffer is depleted and a 20 bit overhead word is read into the output bit stream from the overhead channel formatter. Meanwhile data continues to enter the data buffer and when the block frame counter reaches its terminal count of 1300, data is again read out of the buffer. The overhead channel formatter controls the insertion of frame coder, stuff/spill indicator words, spill bits, and voice and telemetry orderwire information.

Inverse functions are performed by the demultiplex circuits after a frame reference location has been determined by the framing circuits.

The channel readout rates generated on the transmit side are synchronous to the mastergroup clock. Transmit mastergroup timing may originate from an external station clock at 16/32 kHz, receive mastergroup timing or an internal clock. The readout clocks have a common transition precisely once per multiplex frame and this event is used to reference the beginning of the 20 Bit overhead segment of Block nine. Spills for any channels, as required, are performed, simultaneously at that time. To insure that the receive scanner logic performs the precise inverse logic of the transmit scanner, the receive block and multiplex timing chains are used to reset the receive timing generator. All receive nominal read-in rates will then also have a common transition at the end of Block nine. Consequently, all receive spill bits will be loaded into the receive channel buffer simultaneously at this time.

Generally the BITE card receives inputs from all other cards in order to evaluate operating status of the unit and aid in locating possible faults to a single replaceable assembly.

Rate related channel assignment programming for the transmit and receive scanners is accomplished by the priority channel assignment logic.

Table 9-3 lists the controls and indicators for the MGM and Table 9-3A lists the module format.

9.2.7 MGM PACKAGING DESIGN PROBLEMS

Based on the original requirements and the proposed circuit (unit design), it is impractical to package a 12 channel MGM into the standard 8.5" size case. In addition, the power dissipated by the 12 channel unit would have resulted in excessive air and junction temperatures in a standard case configuration and size. These packaging and thermal problems and eventual solutions are discussed in the paragraphs below.

The MGM was estimated to dissipate 92 watts typically on its printed circuit board (PCB) modules (see Table 9-4). The required input power is then 182 watts when operated from 28 Vdc at an estimated power supply efficiency of 50 percent, when operated from 115 Vac at a power supply efficiency of 60 percent. If the above estimate were instead based on the average of typical and maximum integrated circuit power dissipations, then the indicated values would be increased by approximately 28 percent to 118 watts dissipation by the PCB's, 197 watts input for AC operation. An additional 5 watts is required to operate the forced air fan. A thermal analysis contained in Section 15 illustrates that this amount of heat cannot be handled in this case size in an ambient environment of 145°F without forced air cooling.

9.2.7.1 Solutions

The current design of the MGM has been configured in a 14" high by 12" deep by 14-1/4" wide case. The case has been divided into three major compartments, i.e., power supply, switch and fan chassis and PCB compartment (see Figures 9-9 and 9-10).

TABLE 9-3

MGM CONTROLS AND INDICATORS

Power Supply	
On/Off	Applies prime power to supply
LED (Green)	ON if Power ON
Power out TOL	ON if dc outputs out of tolerance. Push to test.
BITE	
Summary Fault Lamp	Front panel lamp ON for any fault except power supply failure. Push-to-test.
Alarm Relays	Rear connector contacts held open in normal operation. S: Summary Fault SA: Summary Fault, except Frame FS: Frame Alarm
LED (Red)	One on each PCB Module. LED is on for fault condition.
Switch Assembly	
Rate Select	Selects one of 15 group rates, or place in OFF position if group module is not used.
Inhibit	Set ON to inhibit group module BITE, and disable outgoing group traffic.
Timing Control	
MGM Rate	Selects high or low mastergroup rate
EXT/INT	Selects external timing or internal oscillator
STA CLOCK	Selects external station clock. Clock rate is strap option.
Orderwire	
TOW Rate	Selects 16 or 32 kb/s Telemetry orderwire rate
VOW Rate	Selects 16 or 32 kb/s Voice orderwire rate

TABLE 9-3A
MGM MODULE FORMAT

MODULE	POS.	FUNCTION
FORMAT GEN	A1	Multiplexes Group and Overhead Data to format the Master Group Data stream.
TRANS RATE GEN	A2	Generates a scan clock and a full complement of Group Rate Timing signals.
RATE SELECTOR	A3,A20	Selects the transmit and receive channel rate timing signals.
SCANNER LOGIC	A4,A5 A18,A19	Provides for the assignment of multiplexed time slots for each active traffic channel.
GROUP LOGIC	A6 thru A17	Provides full duplex rate buffering for asynchronous group signals.
REC. RATE GEN	A21	Generates the receive scan clock and a full complement of group rate timing signals synchronous to the master group clock.
FRAMING	A22	Synchronizes the incoming master group bit stream to the local multiplex block and frame counters.
MASTER GROUP REC.	A23	Demultiplexes the received master group data stream into constituent data channels.
ORDERWIRE MUX / DEMUX	A24	Provides two full duplex digital orderwire channels operating at 16 or 32 KB/S.
BITE		Monitors signals in and out of the MGM and internal circuits.

TABLE 9-4

MGM POWER DISSIPATION

Printed Circuit Boards PCB	Quantity	Dissipation/PCB	Totals (Watts)
Chan. Logic	12	2.37	28.44
Format Generator	1	6.64	6.64
Scanner	4	5.68	22.72
Framing	1	6.75	6.75
Rate Select	2	2.03	4.06
Transmitter Rate Generator	1	5.80	5.80
Receiver Rate Generator	1	5.63	5.63
Master Group Receive	1	5.82	5.82
Orderwire	1	2.48	2.48
BITE	1	3.70	3.70
Total PCB			92.04 Watts
Input Power DC @ 50% Efficiency			184.1 Watts
Input Power AC @ 60% Efficiency			153.4 Watts
Additional Power for Fan			5.2 Watts

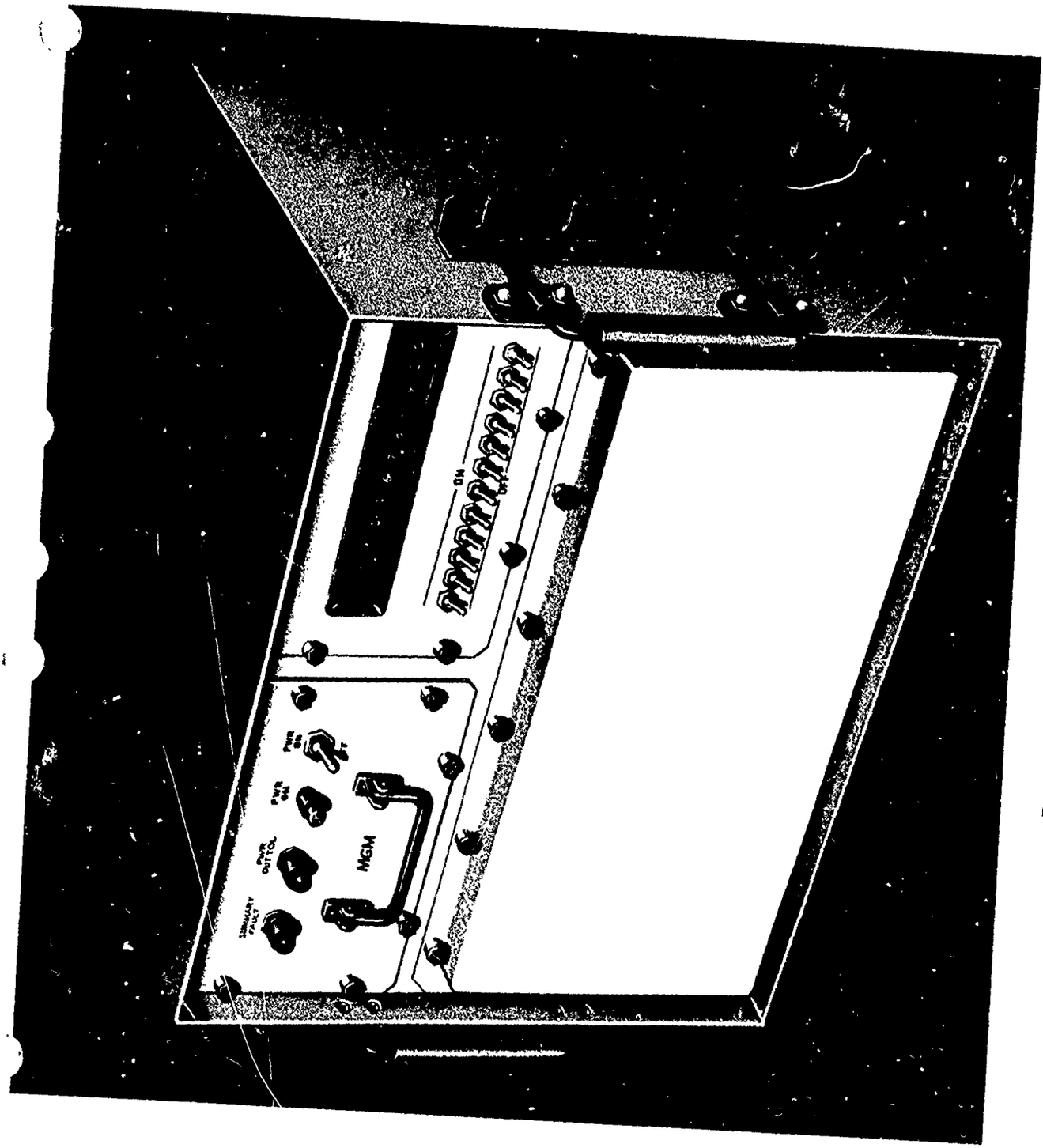


Figure 9-9. MGM Unit Configuration

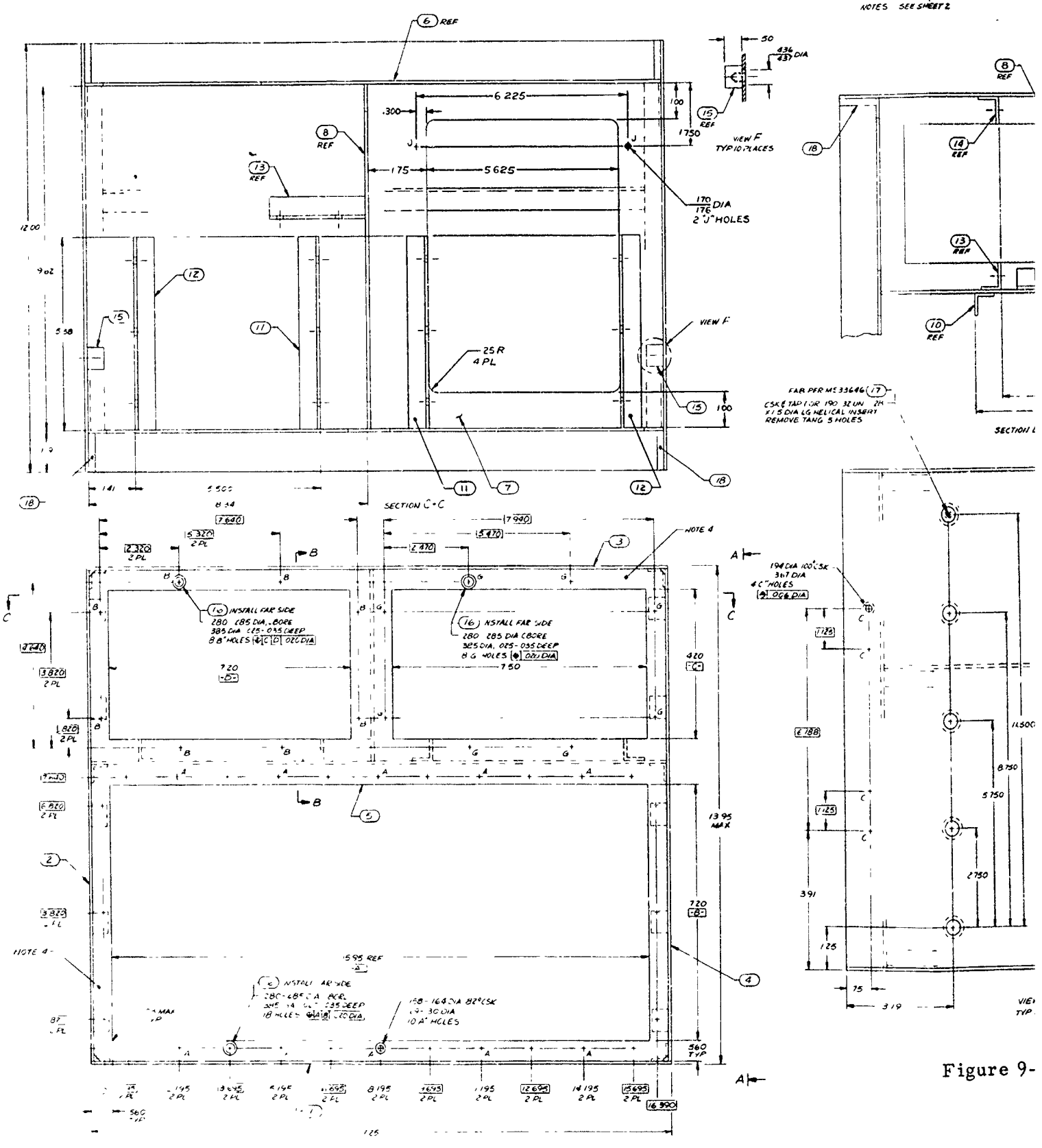

NOTES SEE SHEET 2
6 REF
8 REF
13 REF
12
15
11
18
7
VIEW F
TYP 10 PLACES
VIEW F
SECTION C-C
6 225
5625
175
300
1750
100
170/176 DIA 2 "J" HOLES
25 R 4 PL
436/437 DIA
50
14 REF
10 REF
FAR PER MS 33646 (17)
CSK & TAP 1 OR 190 32 UN 2A X 1.5 DIA LG HELICAL INSERT REMOVE TANG 5 HOLES
SECTION L
NOTE 4
(10) INSTALL FAR SIDE 280 285 DIA C BORE 385 DIA .025-.035 DEEP 88 HOLES
(16) INSTALL FAR SIDE 280 285 DIA C BORE 325 DIA, 025-035 DEEP 8 G HOLES
(1) INSTALL AR SIDE
158-164 DIA 82° CSK
10 A HOLES
1595 REF
1395 MAX
720
560 TYP
750
420
194 DIA 100° CSK 3x7 DIA 4 C HOLES
066 DIA
1125
1188
875
575
275
391
125
75
319
11500
16900

Figure 9-

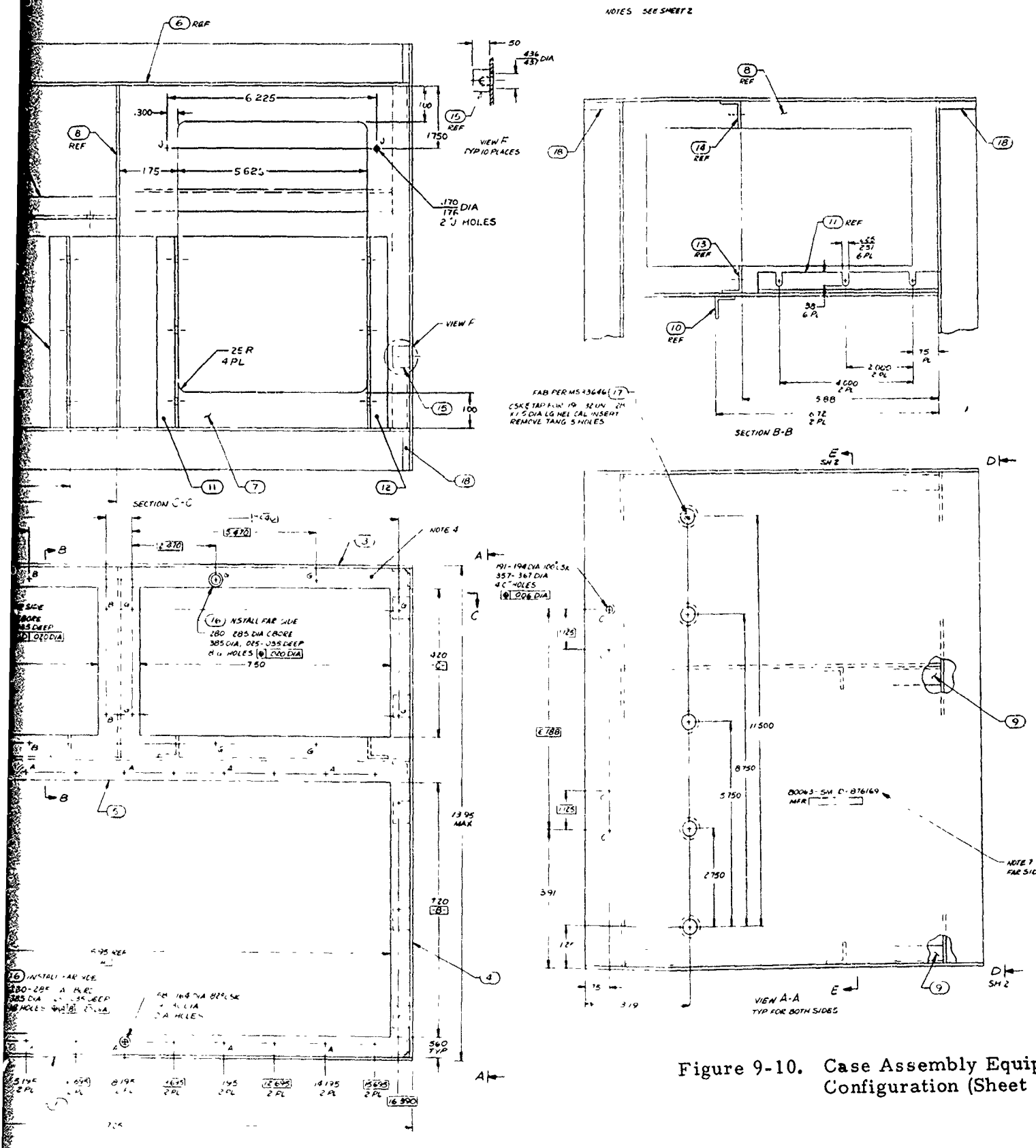
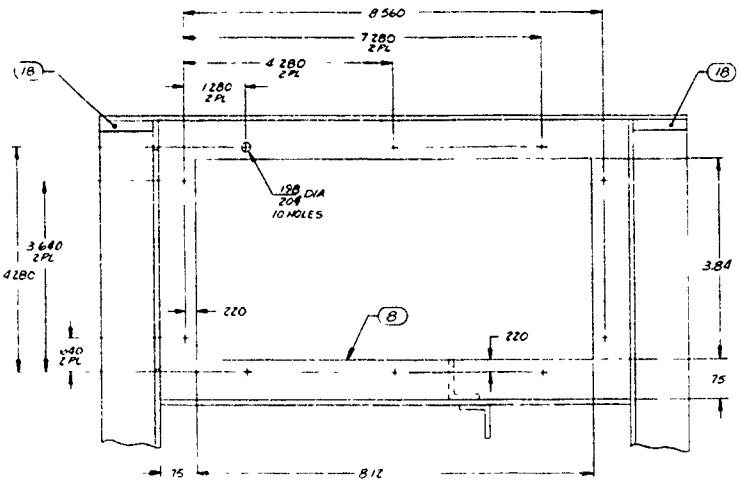


Figure 9-10. Case Assembly Equipment Configuration (Sheet 1 of 2

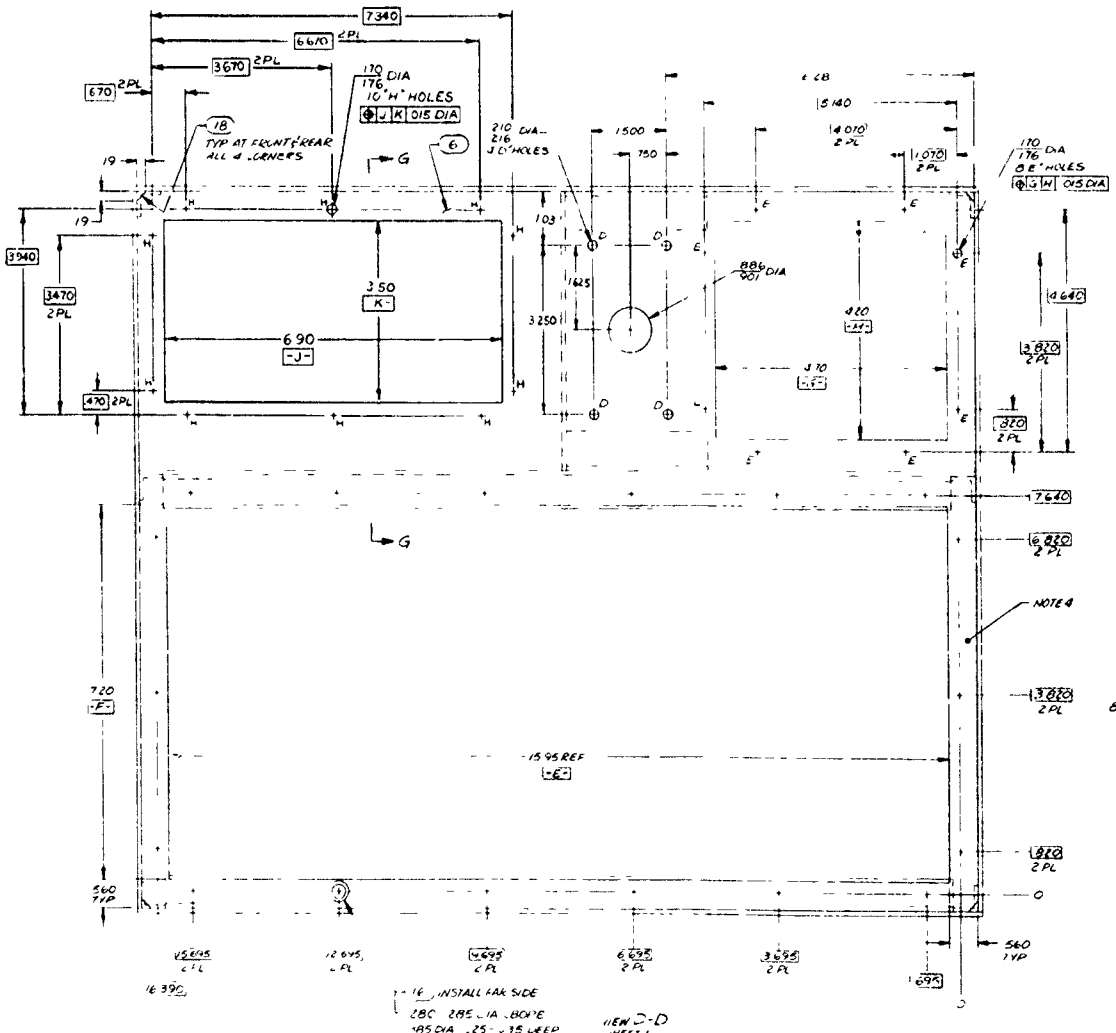
RAYTHEON COMP

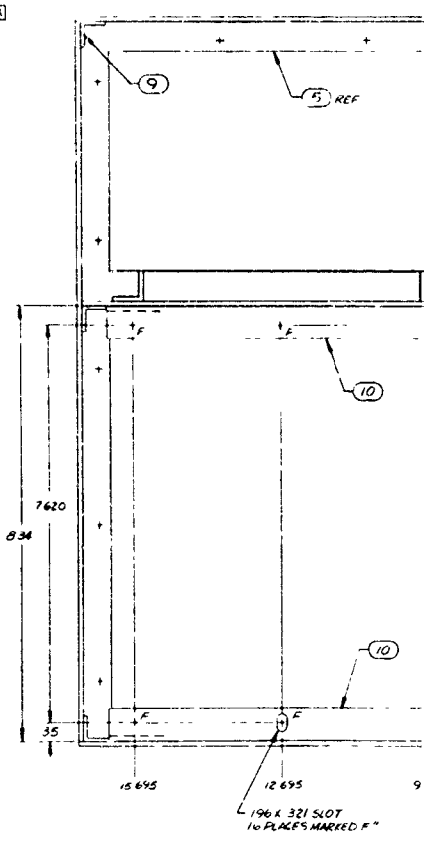
EQUIPMENT DIVIS



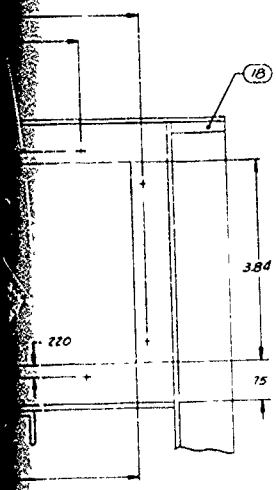
SECTION G-G

FIND NO	MATERIAL
1,2,3,4,5, 6,7,8	.090 THK ALUMINUM 6061-T6 QQ A 250/11
9	500 X 500 X .062 THK ALUMINUM, EXTRUDED ANGLE, 6063 TS QQ A-200/9
0	625 X 625 X .090 THK ALUMINUM, EXTRUDED ANGLE 6063 TS QQ A 200/9
1, 12	580 X 625 X .090 THK ALUMINUM EXTRUDED ANGLE 6063 TS QQ A 200/9
13, 14	625 X 750 X .090 THK ALUMINUM, EXTRUDED ANGLE 6063-TS QQ A-200/9
15	625 DIA ALUMINIUM, 6061 T6 QQ-A 200/8
18	ALUMINUM 6061 T6 QQ A 250/11



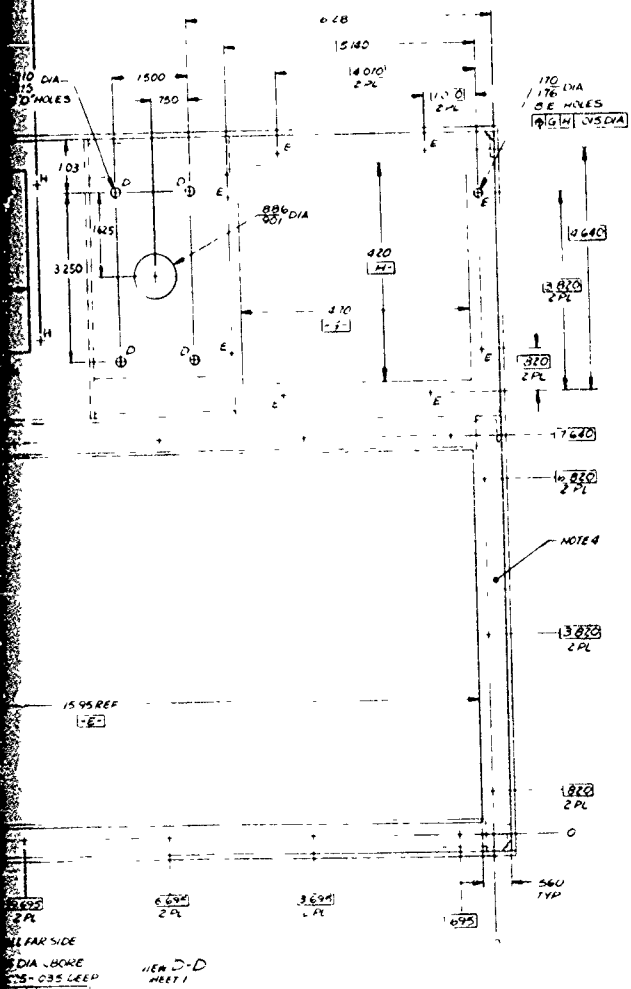


Figur



FIND NO	MATERIAL
1,2,3,4,5, 6,7,8	.090 THK ALUMINUM 6061-T6 QQ A 250/11
9	500 X 500 X .062 THK ALUMINUM EXTRUDED ANGLE, 6063 T5 QQ-A-200/9
10	625 X 625 X .090 THK ALUMINUM, EXTRUDED ANGLE 6063-T5 QQ A 200/9
11, 12	560 X 625 X .090 THK ALUMINUM EXTRUDED ANGLE 6063 T5 QQ A 200/9
13, 14	625 X 750 X .090 THK ALUMINUM, EXTRUDED ANGLE 6063-T5 QQ A-200/9
15	625 DIA ALUMINUM, 6061 T6 QQ A 200/8
16	ALUMINUM 6061 T6 QQ A 250/11

NOTES
1. DIP BRAZE PER MIL B-7883 TYPE II
2. FINISH E513 PER SPEC MIL F-14072 TO BE ELECTRICALLY CONDUCTIVE
3. HEAT TREATMENT AIR COOL AFTER BRAZING AND OVEN AGE AT 350 DEGREES FAHRENHEIT FOR 6 TO 12 HOURS
3.1 MECHANICAL PROPERTIES PER SPEC QQ A 250/11 FOR 6061-T6 ALUMINUM
4. MASK ALL HOLES AND .50 ALL AROUND EA EXTERIOR OPENING
5. EXTERIOR SURFACES, FINISH P513C LIGHT GRAY COLOR NO 26250 PER TT-E-529 & FED-STD 595
6. DIAGONAL MEASUREMENTS TO BE EQUAL WITHIN .040 FRONT AND REAR OPENINGS
7. MARK 12 HIGH BLACK CHARACTERS, GROUP II, PER MIL-M 13231 LOCATE APPROX WHERE SHOWN



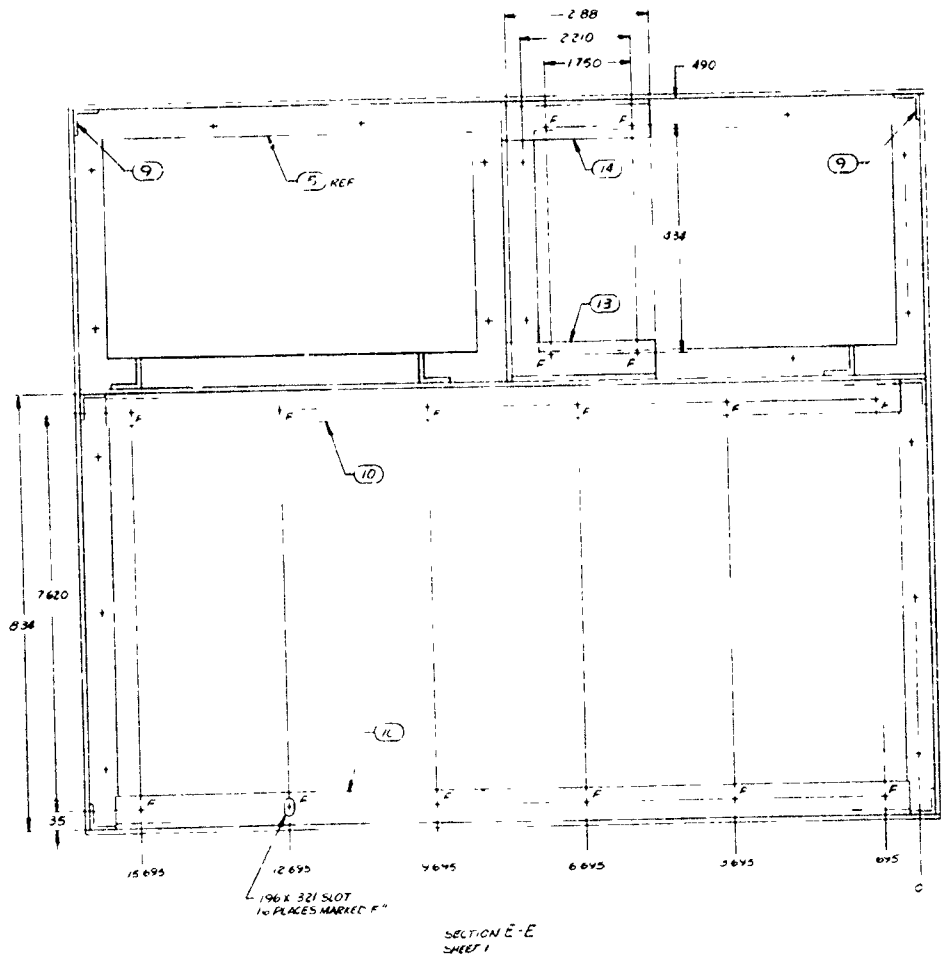


Figure 9-10. Case Assembly Equipment Configuration (Sheet 2 of 2

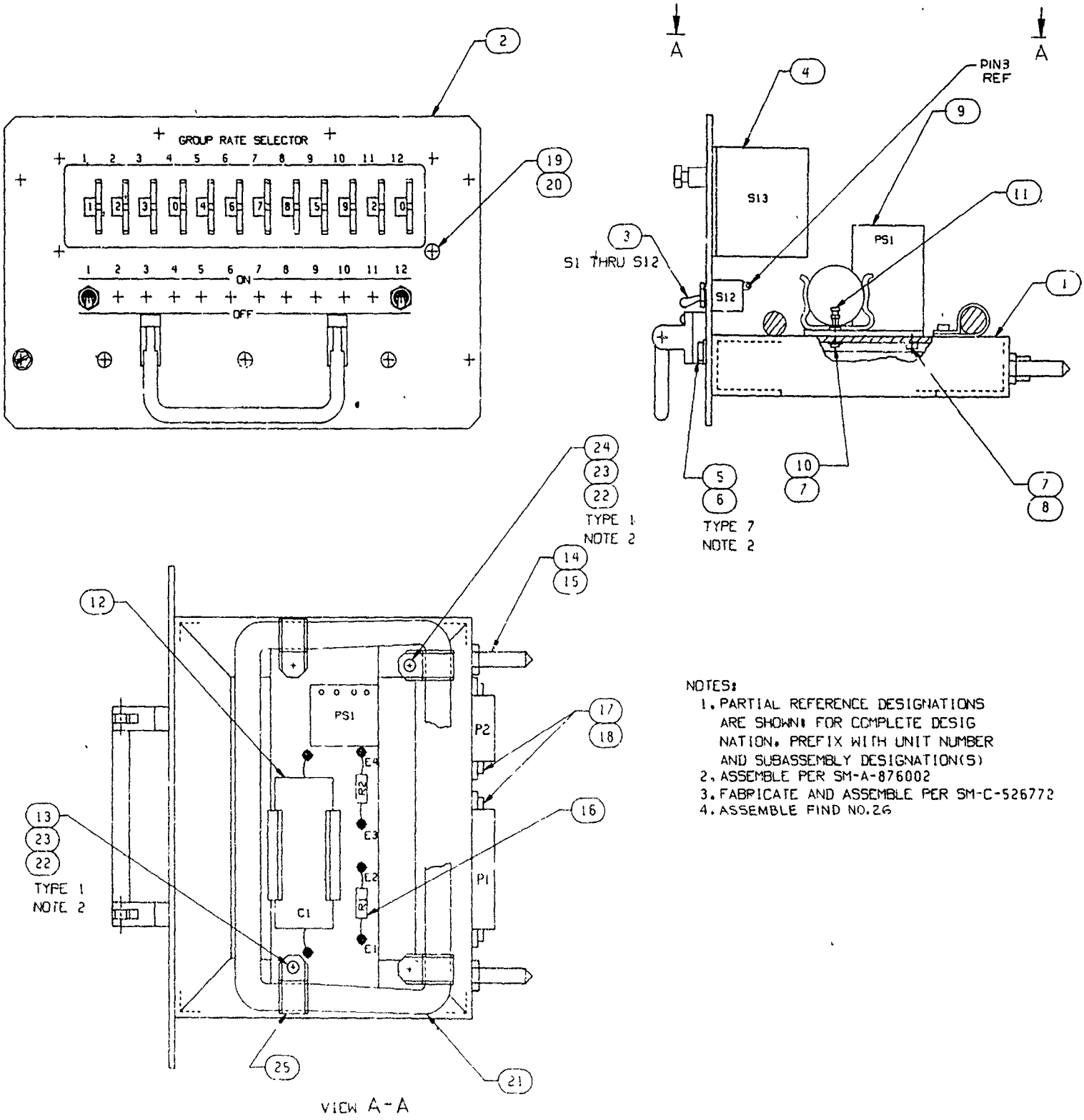
The power supply compartment is located above the PCB compartment. Wiring to and from the PS is via feed through capacitors located in a vertical wall which separates the PS and the switch/fan compartment. This wall has an opening to allow air flow.

The fan/switch compartment (see Figure 9-11) is RFI/EMI isolated from the external ambient via gasketed interfaces but is open to the PCB compartment to allow unimpeded air circulation. The MGM with its front panel in place, as is normal operation, has an air opening across the PCB compartment with an air filter cover. External air is drawn in thru this opening, circulated thru the case and exhausted at the rear of the switch assembly.

The switch/fan chassis is designed as a separable subassembly containing the Rate Selector switch assembly, its associated toggle switches, cable harness, blower (Aximax 2H by Rotron) and its associated dc/ac power pack mounted to a heat sink which protrudes through the back of the equipment case. Interconnections from the assembly to the w/w plate is via rack and panel connector and harness.

9.2.8 EMI

The MGM has signal interfaces with other shelter mounted units. All the traffic signals, groups, supergroups, and the mastergroups are balanced. This interface relies on the balance as its primary means of EMI suppression. The external cables connected here are shielded twisted pair, such as RE-108, so a high degree of suppression can be maintained. There is a wide range of bit rates on these lines, groups, and supergroups from 72 to 4951.2 kb/s and mastergroup 9.36 or 18.72 Mb/s, and waveshaping suitable for the highest rate would be ineffective at the lowest. Some waveshaping occurs as a result of limitations of the logic used, especially in the mastergroup. There are auxiliary signals for orderwire and telemetry that are also balanced. These use waveshaping and are carried externally in multi-pair cable. The full duplex telemetry channel and the orderwire channel have rates of 16 or 32 Kb/s. There is a floating alarm line which appears as a balanced line. All signals are digital and have the basic $(\sin x/x)^2$ spectral shape.



NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIG NATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. ASSEMBLE PER SM-A-876002
3. FABRICATE AND ASSEMBLE PER SM-C-526772
4. ASSEMBLE FIND NO. 26

Figure 9-11. Fan/Switch Layout

The power line has a single EMI filter specified for dc, 50 Hz, and 400 Hz. This makes it larger than a conventional filter, but smaller than two filters. The power line filter has an integral power line connector which gives far better filter performance as installed on the unit and saves additional space. A grounding terminal is provided on the back of the unit.

The logic families used here are low power Shottky TTL for the most part to save power, and regular Schottky for the high-speed portions.

9.2.9 RELIABILITY DESIGN

The MGM has a specified MTBF of 4000 hours. This is equivalent to 250 failures in 10^6 hours. The reliability prediction and the demonstrated results are summarized in Table 9-5.

TABLE 9-5

MGM RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
4000	4857	6800

9.3 DETAILED DESIGN DESCRIPTIONS

9.3.1 GROUP LOGIC MODULE

A block diagram of the Group Logic Module is shown in Figure 9-12. This module provides full duplex rate buffering for asynchronous group signals applied to the multiplexer.

Input data and timing pass through interface circuits to enter an eight bit buffer store. Rate equalization of incoming data is implemented by means of bit stuffing and spilling technique. Data is read out of the buffer under common circuit control so as to maintain the store occupancy near half full. The store occupancy is monitored by applying the read-in and read-out timing to a phase detector. The state of the occupancy monitor is sampled and stored once per major frame by the XSTROBE signal. The stored occupancy signal then controls whether a stuff or spill indicator word will be signalled in that major frame, and whether a spill or stuff will be executed in response to the SPILL clock at the end of the major frame.

Buffered data from the store is applied to a common circuit data multiplexer which is under control of the scanner logic modules. The READOUT clock, generated by the Scanner Logic, increments a readout counter in the buffer which points to the next bit to be read out. The SPILL clock acts as just another readout clock pulse if the stored occupancy signal indicates the need for a spill (high occupancy). If the stored occupancy signal indicates the need for a stuff (low occupancy) then the SPILL clock signal inhibits the next READOUT clock pulse.

At the outgoing (receive) side data is again read into an eight bit buffer store by the READ-IN clock signal. Over the course of a major frame a stuff or spill indicator word is decoded. Decode of a stuff indicator word results in an

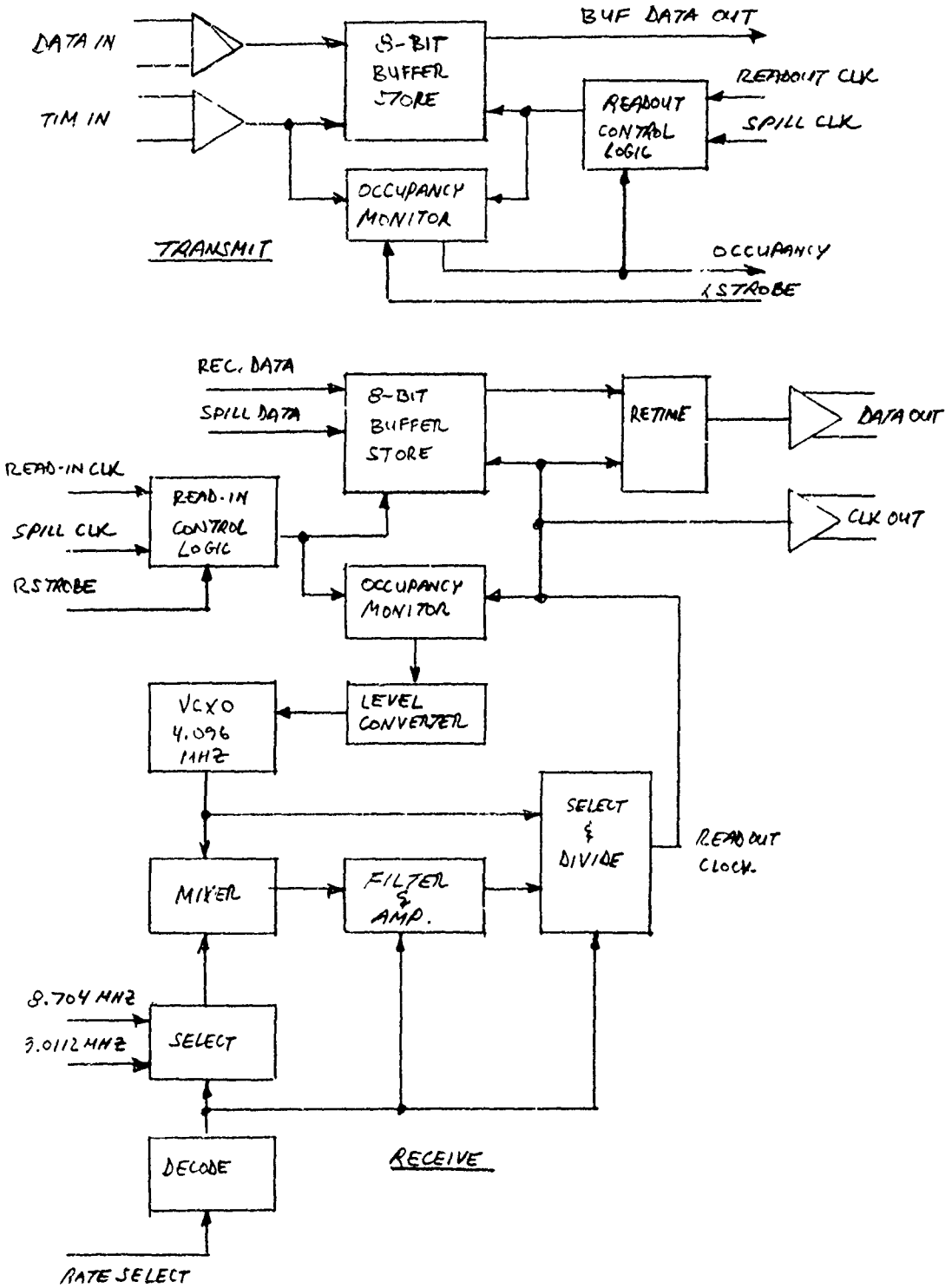


Figure 9-12. Group Logic Module

RSTROBE pulse. This will inhibit the receive side SPILL clock from reading SPILL DATA into the buffer and also inhibit the next READ-IN clock. If there was no RSTROBE pulse then by default the SPILL clock will read in accompanying SPILL DATA. In this manner a data bit is allowed to enter the receive buffer if, and only if, it was originally part of the data stream applied to the multiplexer side input.

Outgoing data is read out of the buffer under control of the timing smoothing circuitry. A binary level control voltage based on the buffer occupancy is applied to the 4.096 MHz voltage controlled crystal oscillator (VCXO). The 4.096 MHz output of the VCXO may be used directly for one of the required rate families. For the 4.9152 MHz rate the VCXO output is mixed with the 9.0112 MHz i-f and the difference frequency recovered in a crystal filter. The 4.608 MHz rate family uses the 8.704 MHz i-f mixed with the 4.096 MHz VCXO output and a second crystal filter. The VCXO or filter output is applied to a timing countdown chain and the appropriate output is used as the readout clock for the buffer store. The RATE SELECT input from the front panel switch assembly controls selection of the appropriate i-f signal, if required, and the divider output from the timing countdown chain to produce the required read-out rate.

9.3.2 TRANSMIT RATE GENERATOR MODULE

The function of the Transmit Rate Generator Module is to provide switch selectable outgoing (transmit) mastergroup timing, generate the transmit scanner clock and from it a full complement of group rate timing signals synchronous to the multiplexer clock. Transmit mastergroup timing may originate from an external station clock at 16 or 32 kHz, receive mastergroup timing at 18.72 of 9.36 MHz, or internal oscillator with ± 5 parts per million stability. A block diagram of the Transmit Rate Generator Module is shown in Figure 9-13.

There are two operating control switches on this module and provision for one strap option. The CLOCK MODE A switch selects master or slave timing reference for the outgoing mastergroup. If the Transmit Mastergroup timing is referenced to an external source this switch must be set to the 'slave' position. The CLOCK MODE B switch is used to select station clock or receive mastergroup timing as the external reference timing. The strap option for

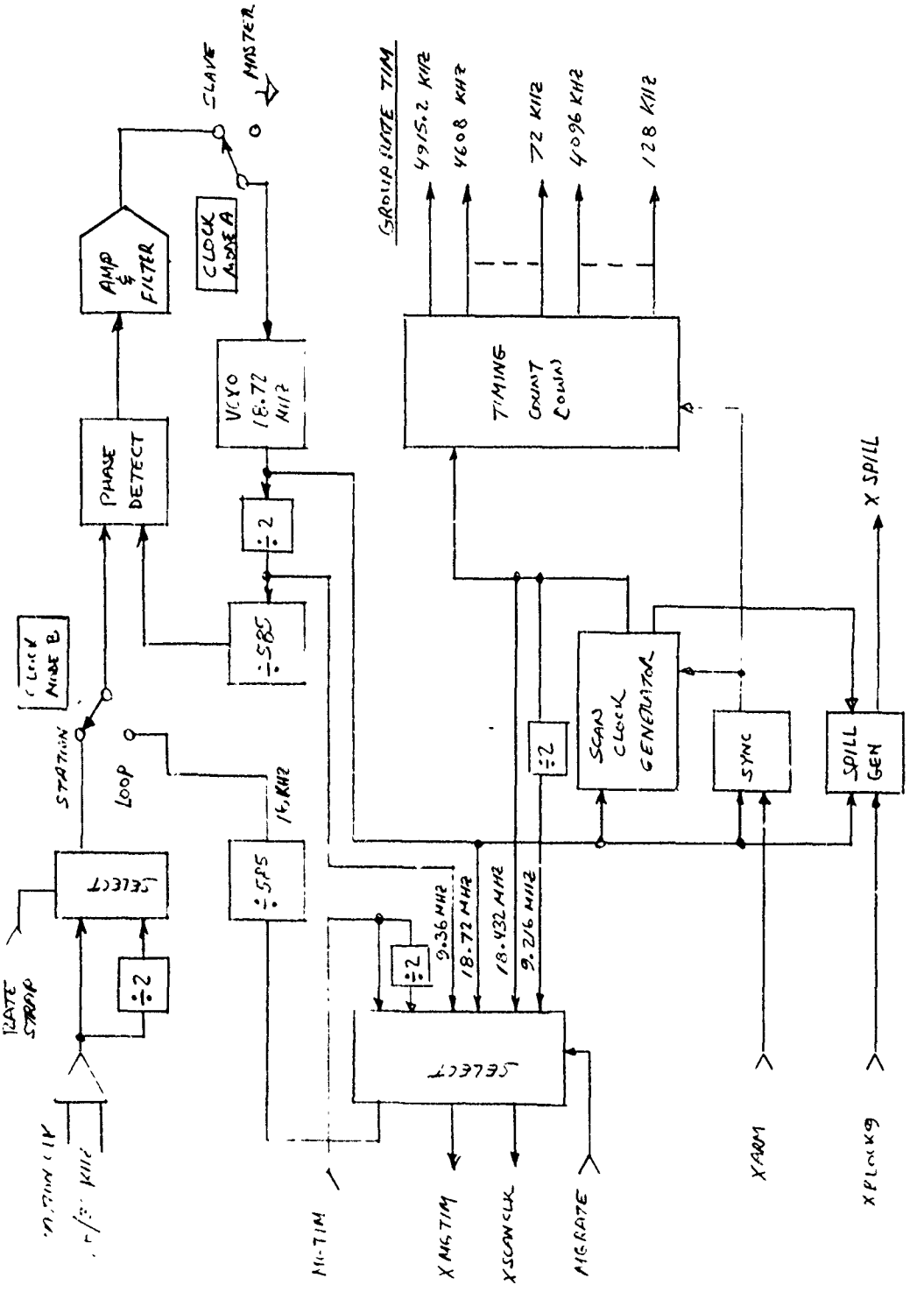


Figure 9-13. Transmit Rate Generator Block Diagram

station clock selects 16 or 32 kHz mode. For any operating mode the voltage controlled crystal oscillator (VCXO) ouput provides transmit mastergroup timing, XMGTIM. An input logic signal, MGRATE, controls selection of high or low mastergroup rate signals.

The 18.72 MHz output of the VCXO drives the scan clock generator. The scan clock generator produces a 18.432 MHz output synchronous to the 18.72 MHz input by deleting four consecutive input clock pulses in each count of 260. In each multiplex block of 1300 bits the high speed scan clock will have five gaps of four consecutive 18.72 MHz clock pulses. The output of the scan clock generator is routed off card as XSCANCLK to drive the scanner modules. The scan clock generator also drives a set of timing dividers to produce the 15 group rate timing signals.

The gap in the scan clock is a time when the associated Scanner Logic is inactive. Hence the spill clock may be positioned within one of the scan clock gaps. The gap is four high speed time slots duration. The spill pulse may then be positioned so that it is not immediately adjacent to the read-in or read-out pulse applied to any Group Logic module. The spill generator produces a spill pulse in block nine of the multiplex frame during the scan clock gap immediately prior to the overhead interval.

The circuits of the Transmit Rate Generator are keyed to the multiplex frame by a transition on the input XARM signal which originates on the Format Generator module. This produces a sync pulse which is nominally at the start of the overhead interval in block nine of the multiplex frame.

9.3.3 RATE SELECTOR MODULE

The Rate Selector module is used to select the appropriate group rate timing signals under control of the multiplexer set front panel RATE SELECT switch assembly for application to a set of Scanner modules. A block diagram of the Rate Selector module is shown in Figure 9-14. Two identical modules are required, one to select the Transmit group rate timing signals and another for receive timing.

The addition of this common function card and the relocation of the Rate Select switches allows a failed Group Logic module to be removed without affecting other active groups.

9.3.4 SCANNER MODULE

The Scanner Module provides demand assignment of multiplex time slots to each active traffic port on the basis of the nominal traffic rate applied to the port input. The Scanner operates at the aggregate traffic rate, i.e., 18.432 MHz for the high rate mastergroup A block diagram of the Scanner Logic is shown in Figure 9-15.

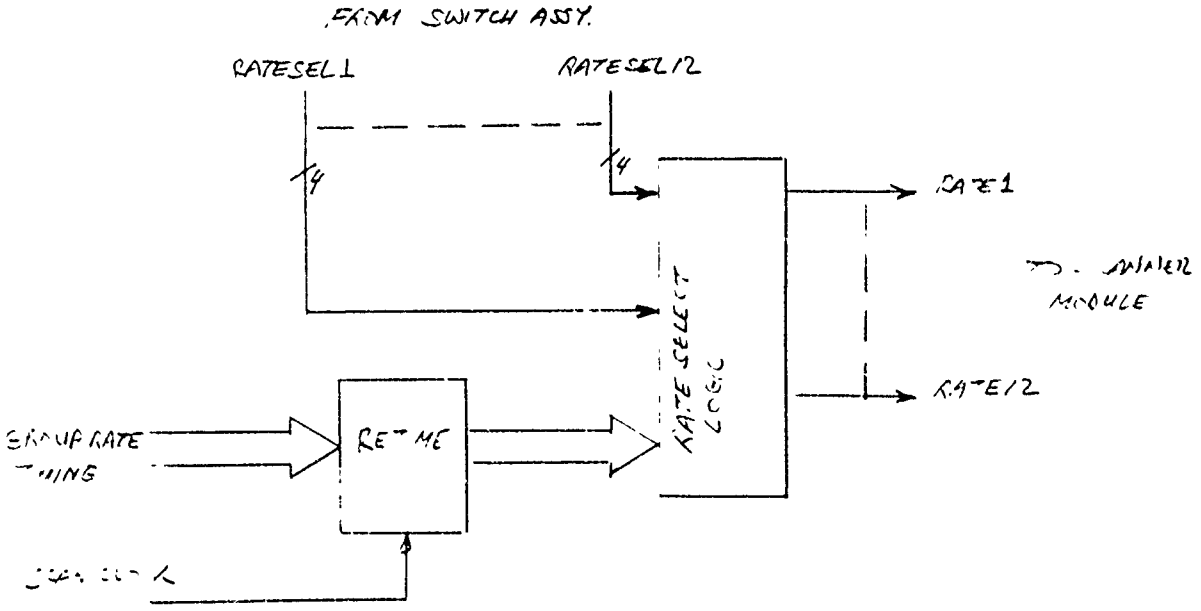


Figure 9-14. Rate Selector Block Diagram

The scanner can service one request for service in each scan clock interval. A particular channel is serviced when its selected nominal channel rate timing signal makes a transition during a scan clock interval. If two or more channels simultaneously demand service, then the request at the lowest port number is given priority and other requests remain pending. This level of priority remains

in effect so long as no input port has more than one request pending. When any port has more than one request pending the level of priority is shifted so that the lowest number port with more than one request pending is given highest priority and serviced first. The scanner is insensitive to more than two pending requests. In addition, consecutive multiplex time slots cannot be assigned to the same port number.

Each scanner logic PCB processes six traffic channels. In the 12-channel MGM two identical scanner cards are required for the transmit function, and another two identical scanner cards are required for the receive function.

Each of the six input timing rate signals are applied to six identical port processing circuits which format a service request. The service request is then steered to one or the other of two integrated circuit priority encoders which, if enabled, generate the address of the lowest number active input. The address is then decoded so that an appropriate signal can be fed back to the port processor to terminate the request.

In order to study the operation of the scanner in detail, let us consider a simplified three-channel scanner. A block diagram is shown in Figure 9-15. If there are no double requests pending for any channel, then the double request priority encoder "E" output is low, and the address select mux will select the two-bit address corresponding to the lowest number active input. If, however, there are any double requests pending, then the double request priority encoder "E" output is high and the address select mux will select the two-bit address corresponding to the lowest number active input with a double request pending. The "E" output also disables the single request address decode circuit which inhibits the servicing of any single requests.

Figure 9-16 is a graphical representation of how the scanner determines the format in which the channels are multiplexed. Each channel's clock is retimed on the scanner card and negative-going transitions are represented by arrows. Each arrow is a request for service. Channel 3 has the highest rate and channel 1 has the lowest. Assume that there exists one scan clock interval when all three channels have a request for service. This occurs during time

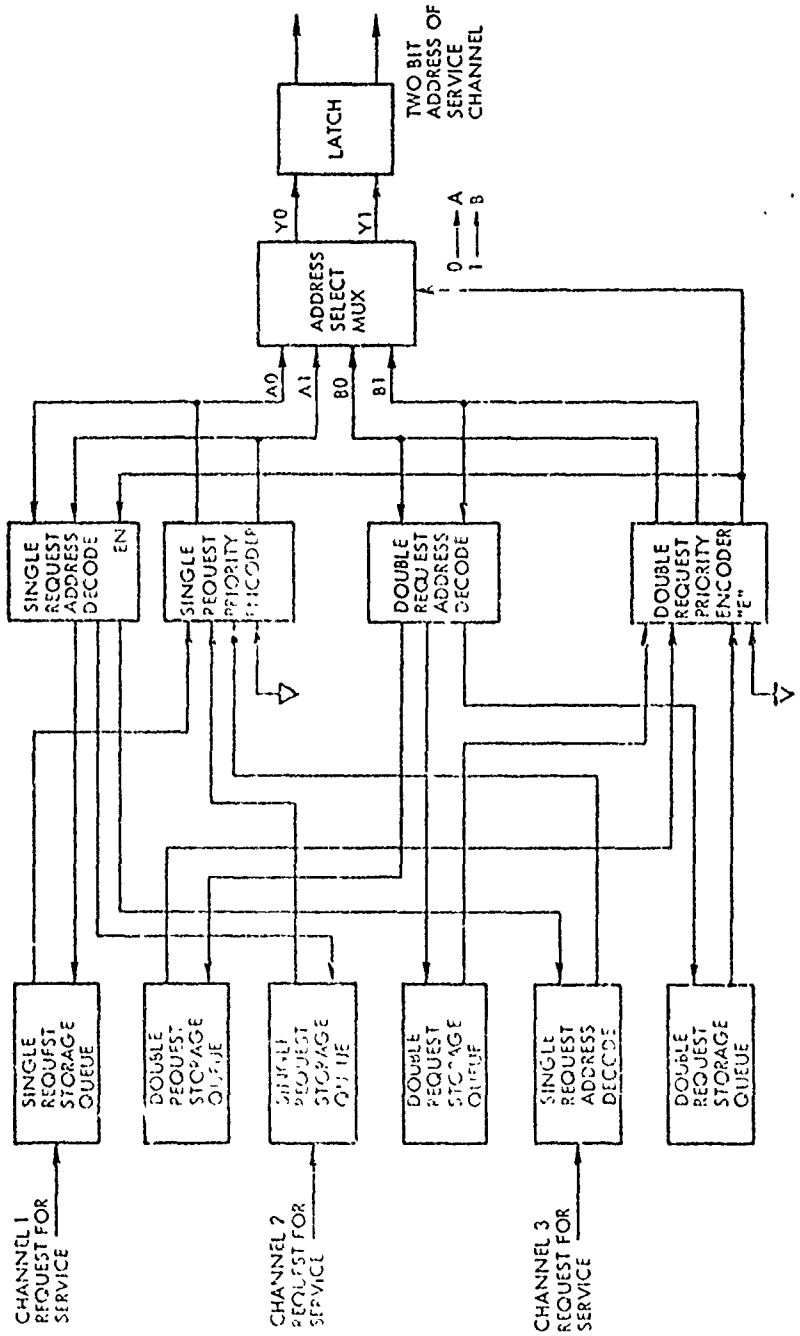


Figure 9-15. Three-Channel Scanner

	REQUESTS FOR SERVICE																								
CHANNEL 1	↑							↑								↑								↑		
CHANNEL 2	↑				↑				↑				↑					↑				↑				
CHANNEL 3	↑			↑			↑			↑			↑			↑			↑				↑			
CHANNEL SERVICED		1	2	3	4*	2	3	4*	1	2	3	4*	3	2	3	1	3	2	4**	3	4**	2	1	3		
CHANNEL 1	X				X										X							X			
CHANNEL 2	X	X			X				X				X				X				X					
CHANNEL 3	X	X	X	X	X	X	X	X	X	XX	X	X	X	X		X			X			X	X			
TIME SLOT	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{16}	T_{17}	T_{18}	T_{19}	T_{20}	T_{21}	T_{22}	T_{23}		

NOTE: Channel 4 is a dummy channel.

4* Here channel 4 is serviced because channel 3 may not occupy two adjacent

4** Here channel 4 is serviced because there are no requests for service pending during this time slot.

X = Single Request XX = Doulbe Request

Figure 9-16. Scanner Formatting

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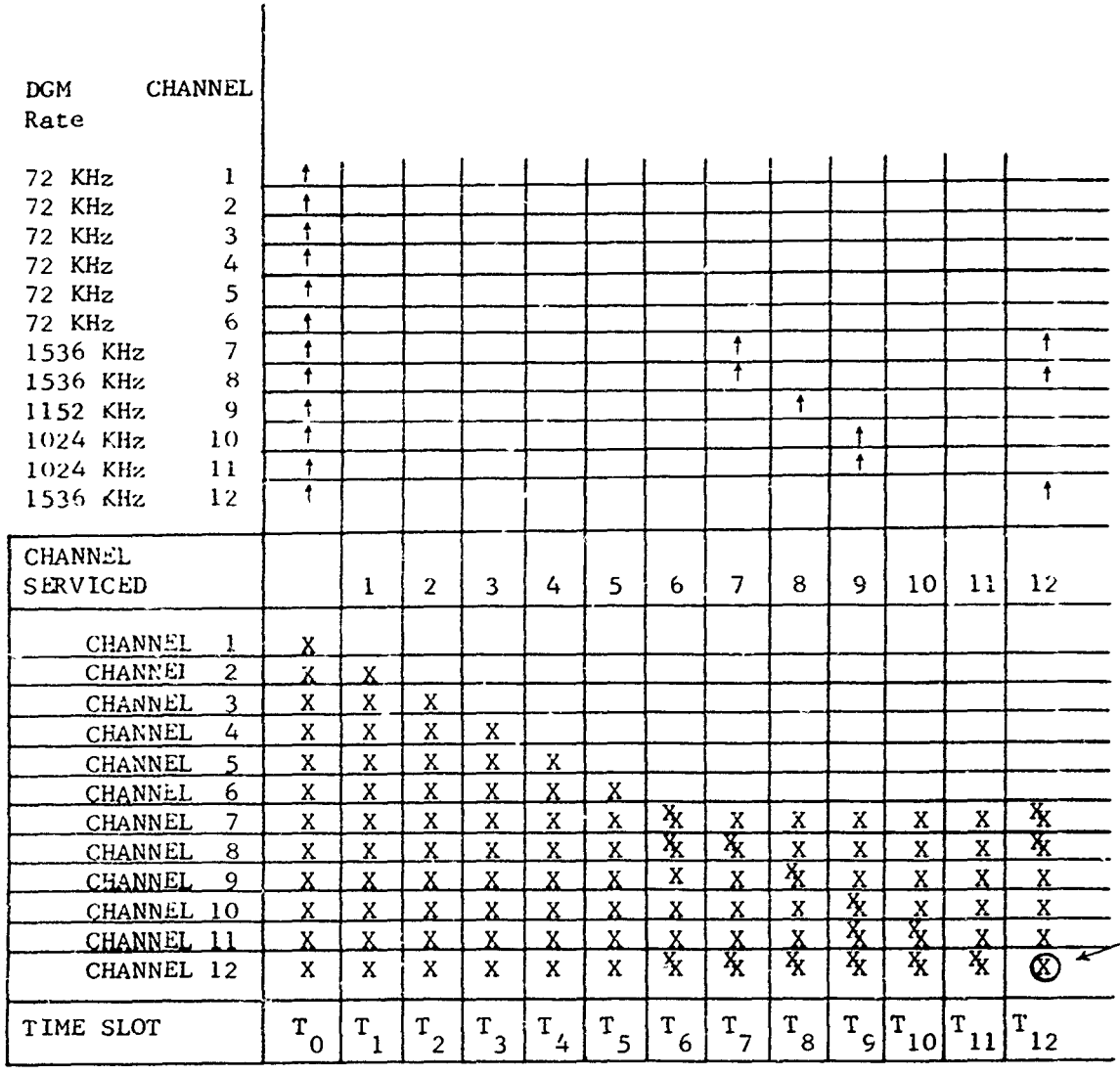
slot TØ in the diagram. During this time slot, all three channels have a single request pending. Channel 1 is the lowest numbered active port and is serviced during time slot T1. Channels 2 and 3 still have single requests pending. Channel 2 is serviced during time slot T2. In time slot T3 channel 3 receives another request for service. Channel 3 now has a double request pending and since there are no lower numbered channels with double requests pending, channel 3 is serviced and now has a single request pending. During time slot T4, channel 3 is the only channel with a single request pending, but since no channel may be serviced in two consectuvie time slots, an unused (dummy) channel 4 is serviced. This dummy channel is also serviced during time slot T18 when no channel has any requests pending.

As a second example, let us now consider two six-channel scanner cards and see how certain rate combinations which do not exceed the maximum aggregate rate will cause a scanner failure. Figure 9-17 illustrates this failure. Notice that in time slot T6, channel 12 has a double request pending which does not get serviced until time slot T12 because lower numbered channels 7 through 11 have their double requests serviced first. During time slot T12 a failure occurs because as channel 12 is having its double request serviced, a third request for service occurs. Since the scanner card has no way of storing this triple request, it is lost and channel 12 will only have a single request pending instead of a double one.

9.3.5 FORMAT GENERATOR MODULE

The Format Generator module performs multiplexing and combining of both traffic and overhead data to format the outgoing mastergroup data stream. A block diagram of the Format Generator module is shown in Figure 9-16.

Buffered data from the Group Logic modules is applied to a data multiplexer which interleaves data under control of the input scan address. The latter is formed by the Scanner modules. The resultant aggregate traffic data



X = Single Request XX = Double Request

Figure 9-17. Scanner Failure

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stream at 18.432 (9.216) Mb/s is continuously read into a 20 bit buffer. This data is read out of the buffer at 18.72 (9.36) Mb/s throughout the portion of the multiplex frame allotted to traffic data, i.e., 1280 time slots in each block of 1300 mastergroup time slots. During the remaining 20 bit overhead interval of each multiplex block data is read from the overhead data format generator. The traffic and overhead data combine to form the outgoing mastergroup bit stream.

The input mastergroup timing (XMGCLOCK) drives a mod-1300 counter which defines a multiplexer block. The last 20 bits of each block define the overhead interval. The output of the multiplex block counter in turn drives a mod-9 block counter which counts out the nine blocks of a multiplex frame. The block nine output in turn toggles a flip-flop to define a major frame.

During the 20 bit overhead interval of each multiplex block the overhead format logic assembles the appropriate 20 bit overhead block which is transmitted as part of each 1300 bit multiplex block. The overhead block assembly is under the combined control of the mod-1300 block counter, mod-9 frame counter, and major frame flip-flop. Overhead information to be assembled varies from block to block and consists of:

a. Multiplex frame code

b. Stuff or spill code for each of 12 groups

c. Spill data

d. Voice Orderwire Data (VOW)

e. Telemetry Orderwire Data (TOW)

The resultant overhead format is as shown in Figure 9-2.

Some timing and control signals are also generated on this module to synchronize the operation of other modules. Occupancy strobe pulses are issued to Group Logic modules which interrogate and latch the contents of the transmit buffer occupancy monitor. The resultant information determines whether a stuff or spill indicator word will be transmitted in a given block. The spill pulse from the Transmit Rate Generator is also gated with the major frame

flip-flop to form the common spill pulse for Groups 1-6 and another for Groups 7-12. The appropriate spill clock will then latch spill data into the overhead format logic. The XARM signal transition is nominally produced at the start of the overhead interval in Block 9 of the multiplex frame. This is used to key the operation of the Transmit Rate Generator module to the multiplex frame. The XBLOCK9 signal is also used by the Transmit Rate Generator to key the placement of the spill pulse in the multiplex frame.

9.3.6 RECEIVE RATE GENERATOR MODULE

The function of the Receive Rate Generator module is to generate the receive scan clock and a full complement of group rate timing signals synchronous to the incoming mastergroup clock. Also located on this card are two temperature compensated crystal oscillators which operate at 9.0112 MHz and 8.704 MHz to provide the i-f signals for the Group Logic receive timing smoothing circuits. A block diagram of the Receive Rate Generator is shown in Figure 9-18.

One operating control switch, MASTERGROUP RATE, is located on this module. This selects a logic level used to control selection of low (9.36 MHz) or high (18.72 MHz) mastergroup rate.

The primary drive signal to this module is incoming mastergroup timing at 18.72 or 9.36 MHz. The drive signal to the scan clock generator must be at 18.72 MHz. Hence for the low rate mastergroup the incoming mastergroup timing is first doubled and then applied to the scan clock generator. The operation of the scan clock, sync and spill generators and timing countdown chain are virtually identical to the circuits of the Transmit Rate Generator. In this case the circuits of the Receive Rate Generator are keyed to the multiplex frame by a transition on the input RARM signal which originates on the Framing module. This transition nominally occurs at the end of the overhead interval in Block 9 of the multiplex frame. The receive spill pulse generator is keyed to a signal transition on the Framing module produced at the start of Block 1 of the multiplex frame. This results in a spill pulse generated during the first scan clock gap interval following multiplex Block 9.

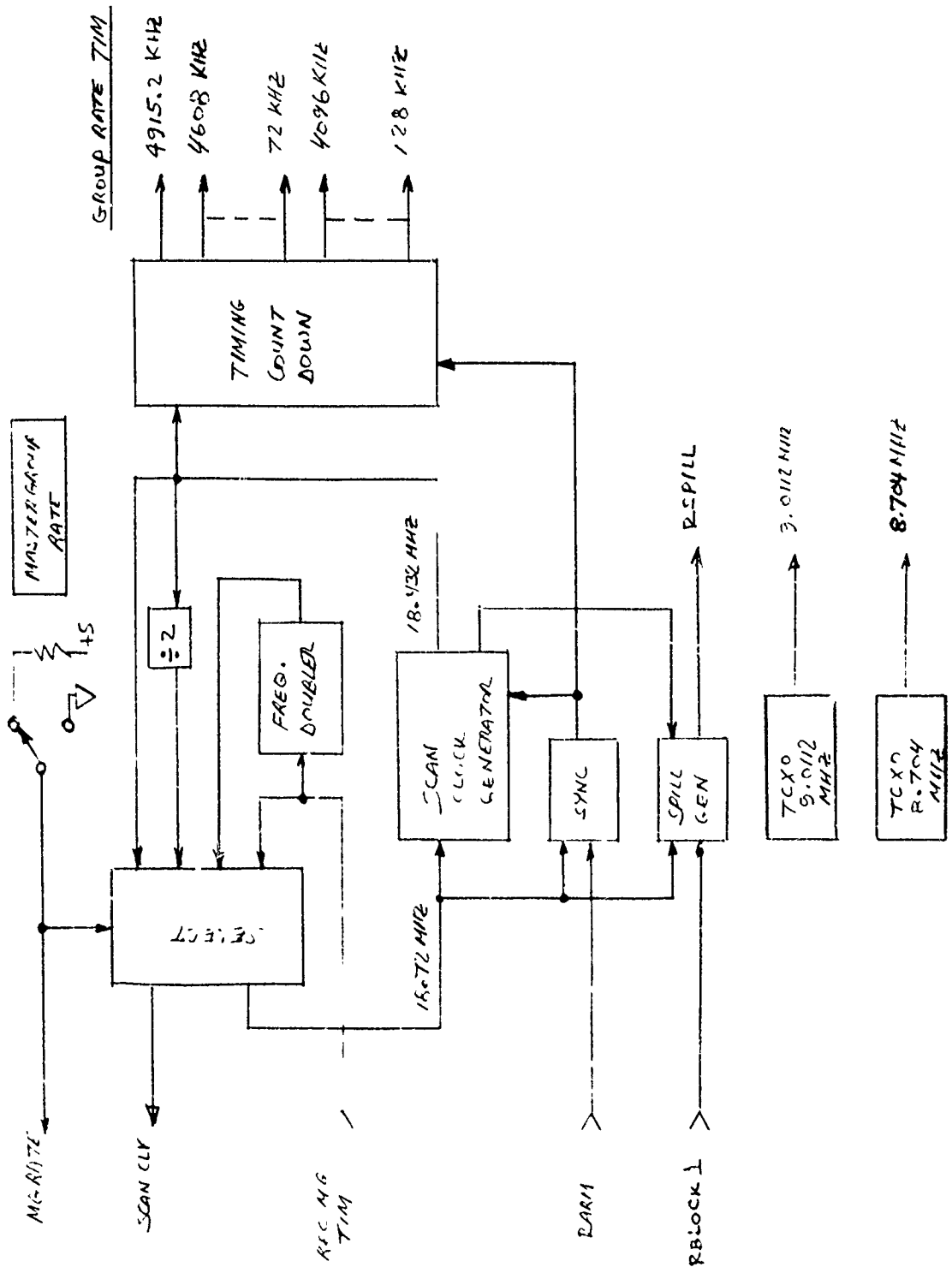


Figure 9-18. Receive Rate Generator Block Diagram

9.3.7 FRAMING MODULE

A block diagram of the Framing module is shown in Figure 9-19. This module is used to synchronize the incoming mastergroup bit stream to the local multiplex block and frame counters so that traffic and overhead data can be identified and decombined.

Incoming mastergroup data and timing, MGDATA and MGTIM, are interfaced to TTL logic levels and applied to a ten bit input shift register. The mastergroup clock RECTIM and retimed data RECDATA are then routed off-card for use by other modules. Gating at the shift register parallel outputs allows decoding of error-free stuff (STF), spill (SPL), and multiplex frame (MFC, $\overline{\text{MFC}}$) codes which are used by the frame acquisition and maintenance control circuits.

In the initial frame acquisition mode the mod-1300 multiplex block counter is held at a state which allows each mastergroup time slot to be tested until a stuff, spill, or multiplex frame code is detected. Upon detection of such a code the mod-1300 block counter is released to that the appropriate overhead channel time slot can be tested again 1300 time slots later. Ten consecutive correct samples are required for entry into the frame maintenance mode. In addition, when the MFC or $\overline{\text{MFC}}$ is detected, then the mod-9 multiplex frame and mod-2 frame counters are released.

In the frame maintenance mode the multiplex codes (MFC and $\overline{\text{MFC}}$) are monitored to detect loss of frame. In every sample of 16 frames, 11 or more successful frame code indications must be received to prevent re-entry into the frame acquisition mode wherein search is allowed. A TTL compatible Frame Search Inhibit signal can be applied to the module to squelch frame search. A frame alarm relay dc closure is also routed off-card to signal loss of frame.

The parallel data outputs from the input ten bit shift register are also strobed into two latches by appropriate strobes from the multiplex block counter. The Overhead Data Latch stores spill data bits and orderwire data words for the Group Logic and Orderwire modules, respectively. Another latch and counter perform a majority vote decode on the incoming stuff/spill indicator word. If a stuff indicator is decoded, then a STFSTROBE signal is issued to the appropriate Group Logic module.

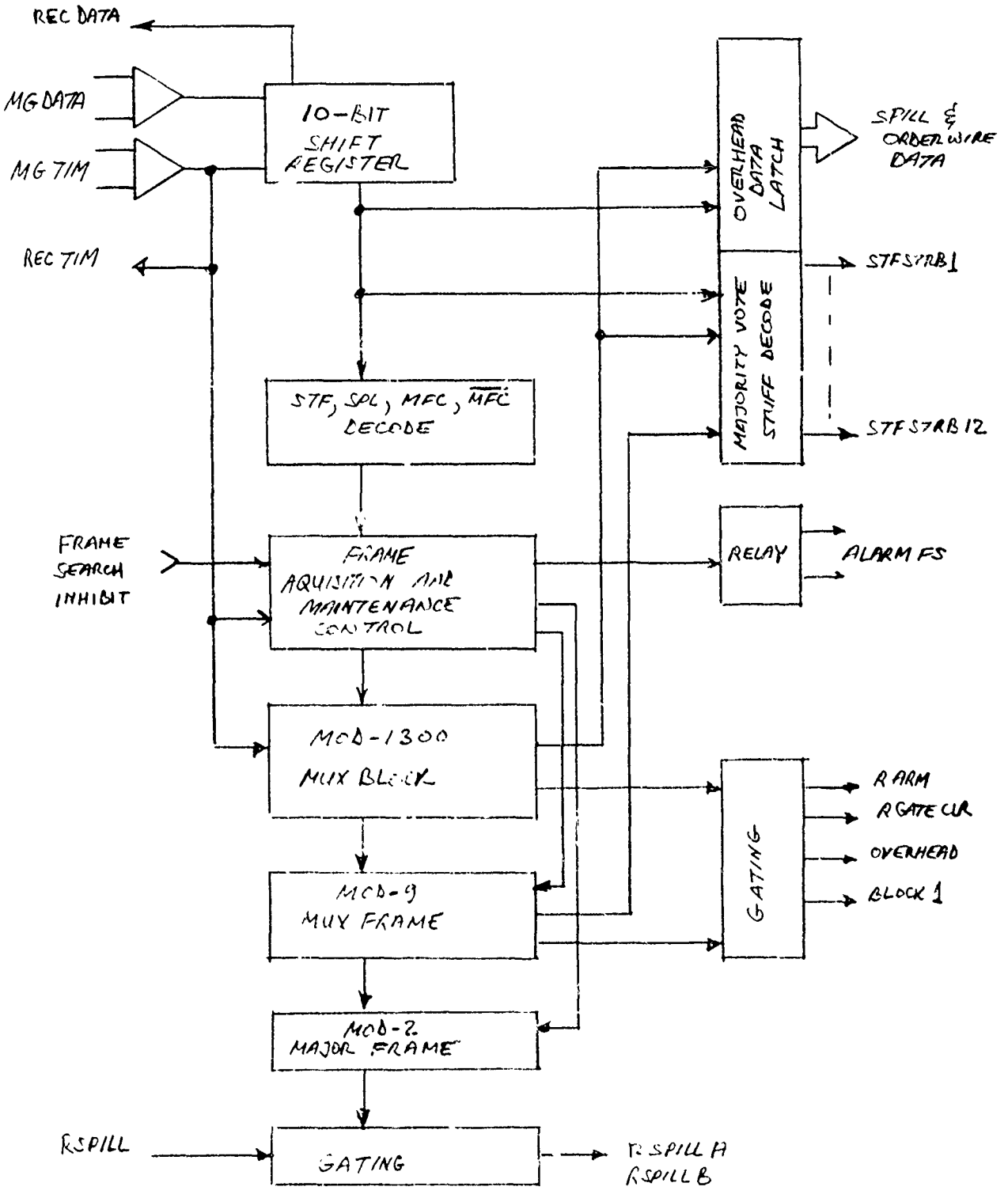


Figure 9-19. Framing Module Block Diagram

Several timing and control signals are also generated which synchronize the operation of other modules. The RARM signal is produced at the end of the overhead interval in Block 9 of the multiplex frame. This is used to key the operation of the Receive Rate Generator to the multiplex frame. The Block 1 signal transition is also used by this module to key the placement of the spill pulse with respect to the multiplex frame. The spill clock returned from the Receive Rate Generator is then gated with the major frame flip-flop to form the common spill pulse for Groups 1-6 and another for Groups 7-12. The OVERHEAD and RGATECLR signals are used by the Receiver Mastergroup module to control and synchronize operation of its traffic data buffer.

9.3.8 MASTERGROUP RECEIVE MODULE

The primary function of the mastergroup receive module is to demultiplex the receive mastergroup data stream into its constituent data channels. This card also contains specialized BITE circuitry which monitors the performance of the equipment Scanner logic cards. A block diagram of the Mastergroup Receive module is shown in Figure 9-20.

Receive mastergroup data and timing from the Framing module are applied to a 20 bit aggregate data buffer. Data is read into the buffer throughout each 1300 bit block except during the 20 bit overhead interval. An overhead gate signal from the Framing module inhibits data read-in during the overhead interval. Data is read out of the buffer throughout each 1300 bit block by the receive scan clock which originates on the Receive Rate Generator module. Identical receive scan clock signals also drive the receive scanner logic modules which produce a scan address during each scanner clock interval. The receive scan address identifies the channel associated with the traffic bit currently being read out of the buffer.

In the high rate mastergroup mode, the mastergroup clock is a continuous 18.72 MHz whereas the scan clock averages 18.432 MHz over a block interval. The latter signal is derived from the mastergroup clock by deleting four adjacent mastergroup clock pulses in every group of 260 mastergroup clock pulses. Over each block interval of 1300 mastergroup time slots exactly 1280 traffic bits are

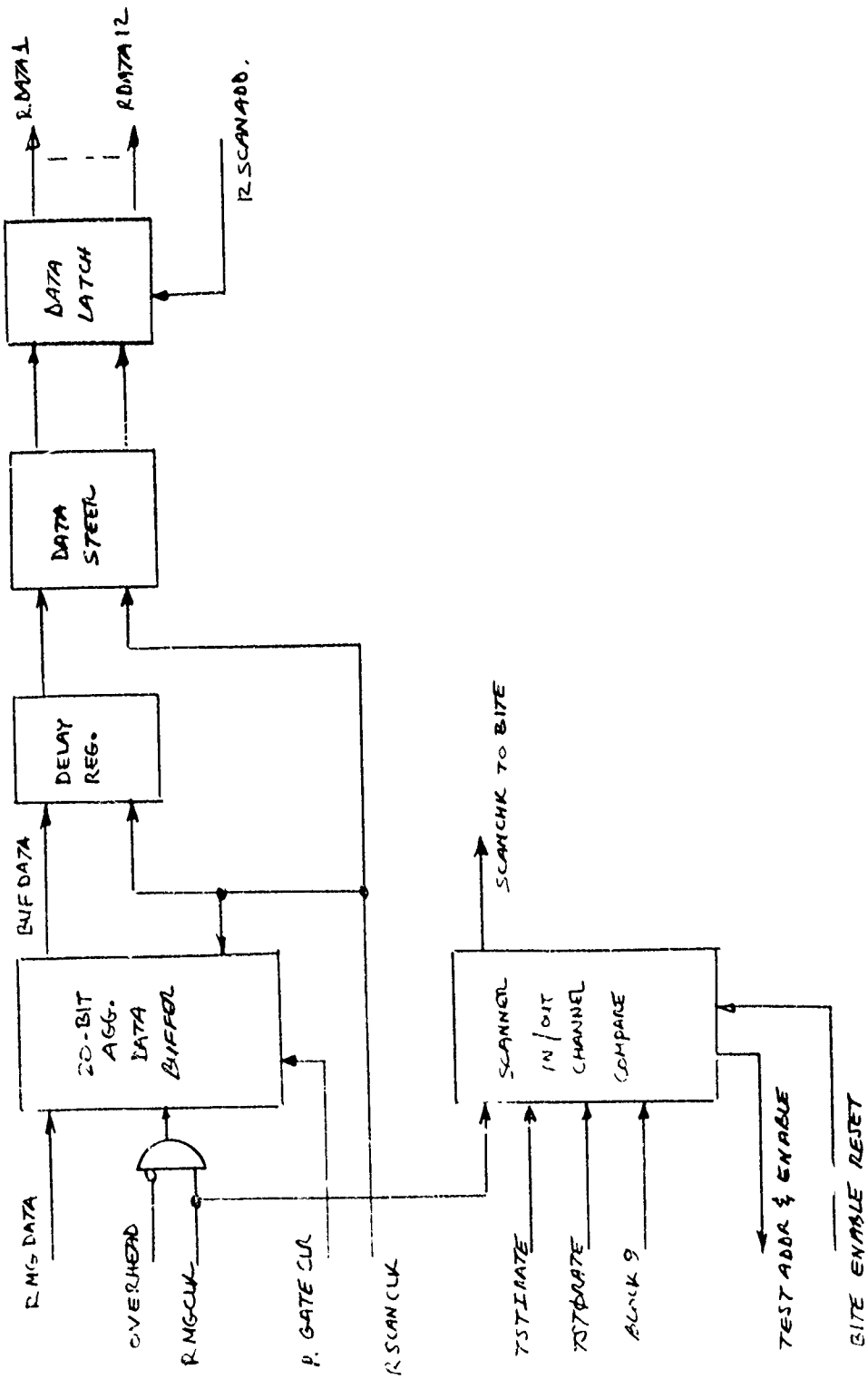


Figure 9-20. Mastergroup Receive Block Diagram

read into the buffer and 1280 traffic bits are read out. However, with respect to an 18.72 MHz timing reference, there is a 20 bit gap in the read-in of data during the overhead interval, and five gaps of four time slots in the read-out over a block interval; hence, the requirement for the 20 bit buffer. Similar conditions apply for the low rate mastergroup mode.

Buffer read-in and read-out is synchronized after each overhead interval by the RGATECLR signal which also originates on the Framing module. At the end of an overhead interval, all data from the past block has been read-out of the buffer. The first four bit data word of the new block is read into the buffer four times slots after the end of overhead. The first read-out trails the read-in by one scan clock interval. This interval is four time slots wide because the scan clock gap is positioned to that point in the frame. During each subsequent scan clock gap, the buffer occupancy increases by four bits. The 20 bit accumulation which has built up during the traffic interval of the block is then read-out during the overhead interval during which time no data is read-in.

Data read-out of the buffer is then nominally delayed by one scan clock interval to line up with the latched incoming scan address. The scan address then steers the data into a corresponding channel data latch. This latched data is then read into the corresponding Group Logic card by a read-in clock formed on the scanner logic card.

As indicated in the block diagram, this card also contains specialized BITE circuitry which monitors each of the four equipment scanner logic cards. Each input channel on a scanner card is presented with the nominal rate for that channel. Over a multiplex frame interval (nine blocks) the number of scan addresses assigned to that channel must be in one-to-one correspondence with the number of nominal rate transitions. There may not be a one-to-one correspondence over a shorter time interval because requests can be kept pending while one or more higher priority channels are being serviced.

The input and resultant output rates for each scanner channel are connected to a pair of multiplexers on each scanner logic card. Then outputs are Tri-State connected and accessed by the scanner BITE circuitry via the TSTIRATE and

TSTORATE inputs on the mastergroup receive card. The particular scanner logic card and channel within the card being accessed is determined by the TESTADDR and ENABLE signals.

Two multiplex frames are required to test each channel of a scanner logic card. Failure of any channel is latched and reported over the BITE bus on a scanner logic module basis. This circuit may also be used during equipment setup to detect a frame overflow condition.

9.3.9 ORDERWIRE MUX/DEMUX MODULE

The function of the Orderwire module is to provide a capability for two full duplex digital orderwire channels. Both channels must be bit synchronous to the multiplexer set clock. However, the static phase of the incoming data transitions is arbitrary. Each orderwire channel may operate at 16 or 32 kb/s, switch selectable.

A block diagram for one full duplex channel of the Orderwire module is shown in Figure 9-21. Both orderwire channels are identical. Incoming data is level converted to standard TTL levels and applied to a transition detector and an input shift register. Detected data transition preset an autophasing counter to produce a bit rate clock with transition centered in the data interval. This clock loads data into the input shift register and increments the mod-5 serial-parallel control counter. After each five bit data word is assembled it is transferred into a data storage register for subsequent readout in the overhead channel of the multiplex frame. The inverse process takes place at the demultiplex side. five bit wide data word may be read into a storage register at the end of block 1 through block 8. The particular strobe set is dependent both on the mastergroup rate and the orderwire channel rate. The data word is then parallel loaded into an output shift register upon command of a mod-5 control counter. The output shift register generates serial output data at the selected orderwire rate. Outgoing timing accompanies the data.

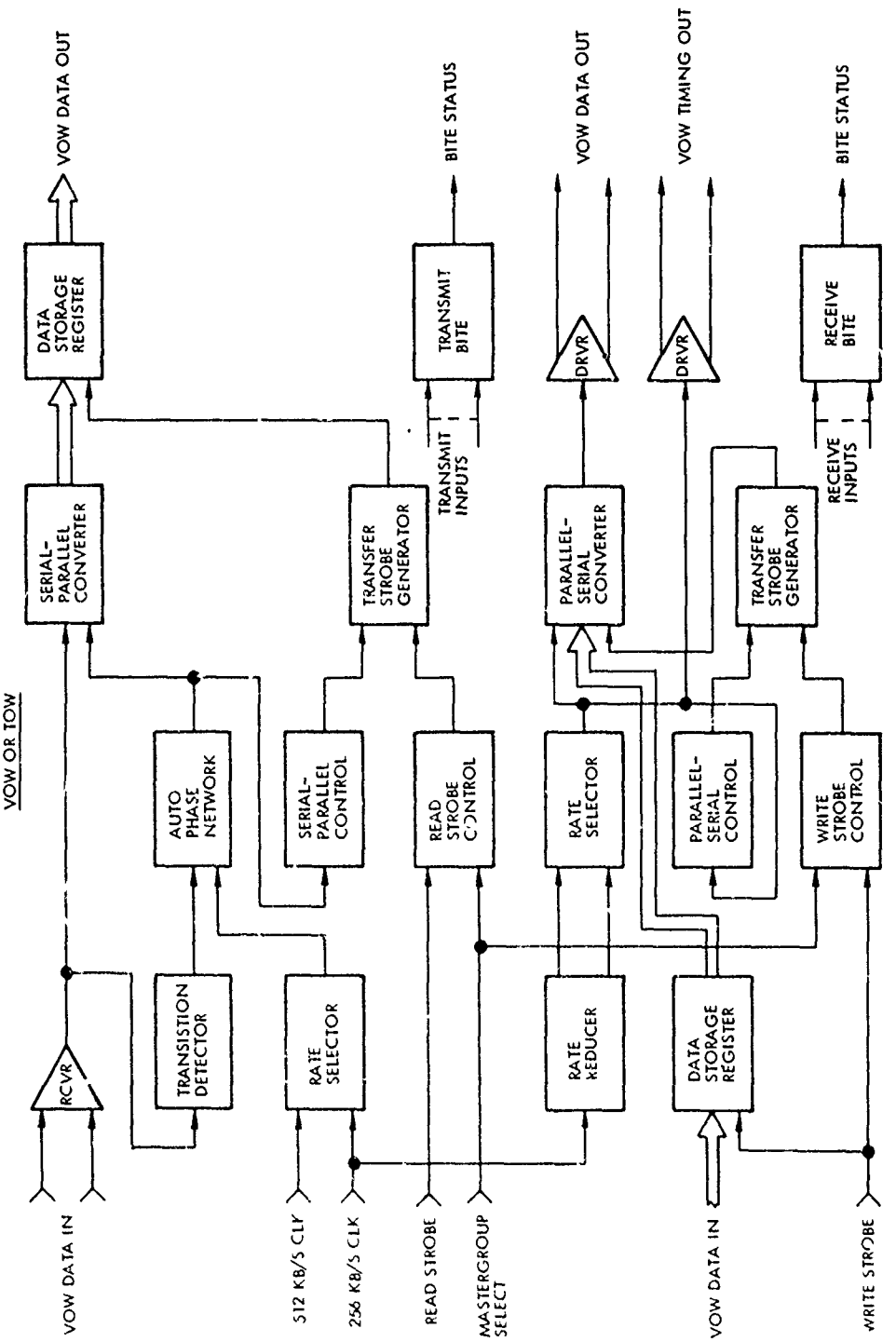


Figure 9-21. Orderwire Block Diagram

9.3.10 SWITCH ASSEMBLY

An equipment front panel switch assembly allows one of 15 possible group rates, or the "not in use" condition to be selected for each of the 12 possible group inputs applied to the MGM. A separate Inhibit switch is also provided for each of the 12 group inputs which is used to inhibit the BITE alarm and disable outgoing traffic for the associated group. This feature allows a particular rate combination to be setup without having active traffic on all groups included in the combination.

9.3.11 BITE MODULE

The MGM uses a standard DGM BITE module to monitor signals in and out of the unit and internal circuits. The BITE module generally allows isolation of failures to a particular printed circuit card or lowest replaceable unit (LRU). The BITE module provides two dc closure summary type alarm indications (S and SA). A visual summary alarm lamp driven by the BITE module is provided on the power supply front panel.

9.3.12 HFE

The MGM design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are incorporated onto the accessible edge of the PCB's. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Figures 9-22 and 9-23 show layouts for the front and rear of the MGM.

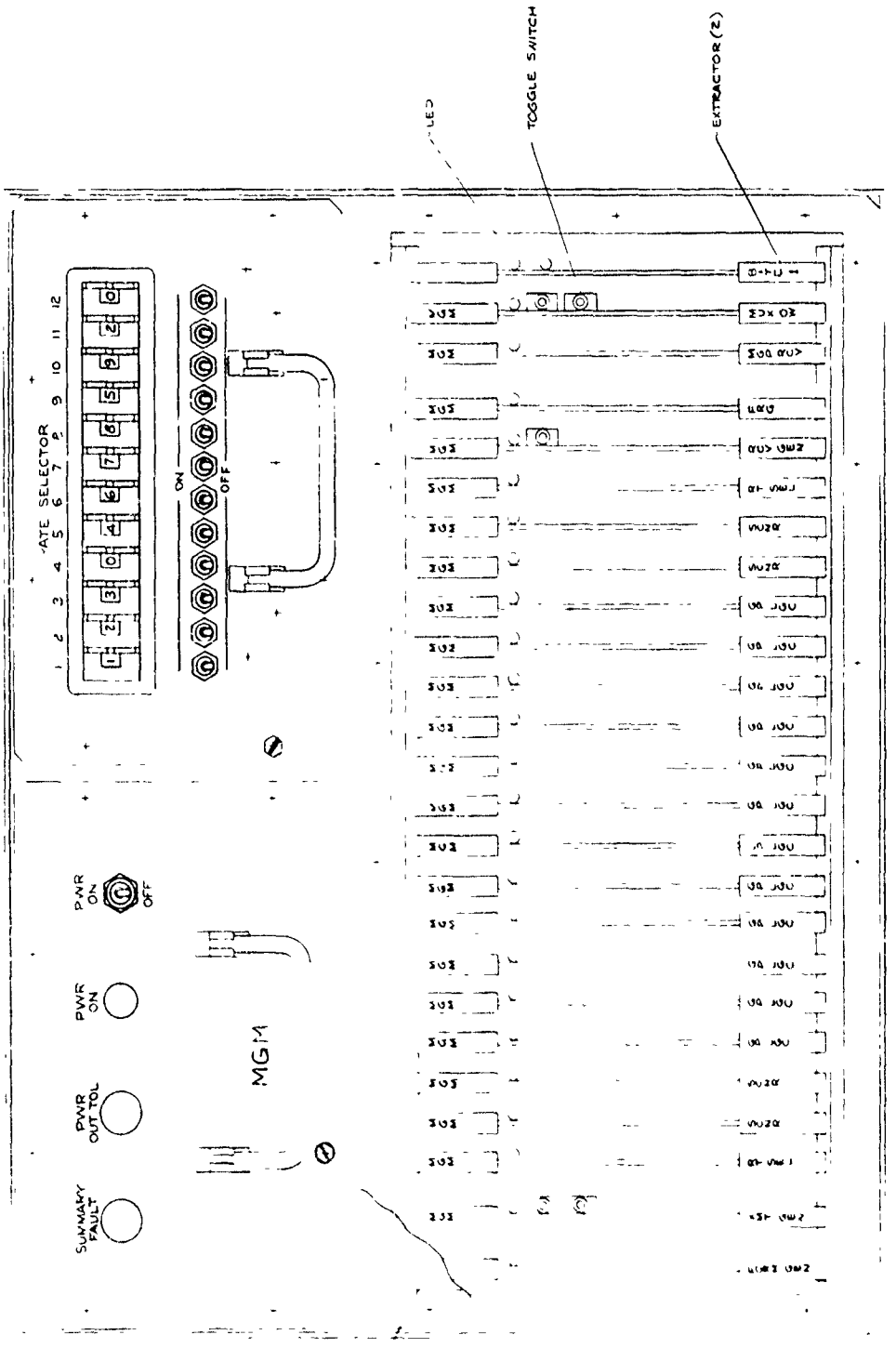


Figure 9-22. MGM Front Panel Layout

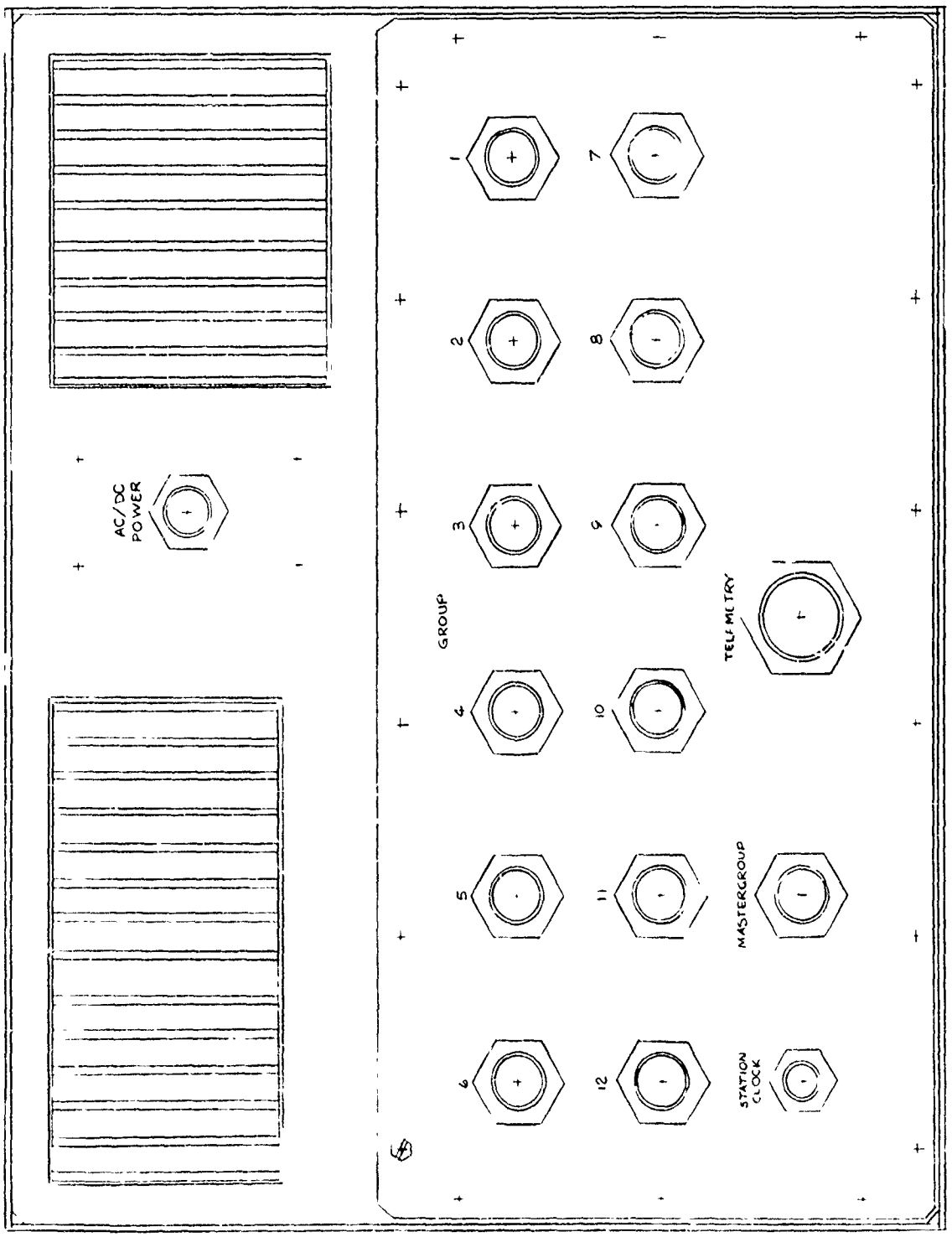


Figure 9-22. MGM Rear Panel Layout

SECTION 10

GROUP MODEM

The Group Modem (GM) carries traffic at various rates between 72 Kb/s and 4915.2 Kb/s. Three types of modulation are employed; conditioned diphase, bipolar, and dipulse. In some instances an orderwire channel must be provided, and in other cases a telemetry channel must also be provided.

10.1 DESIGN GOALS AND REQUIREMENTS

Functional requirements for the Group Modems are summarized in Table 10-1.

10.1.1 DIPHASE GM

The Diphase GM handles traffic at the following rate: 72, 128, 144, 256, 288, 512, 576, 1024, 1152, 1536, 2048, 2304, 4096 and 4608 kb/s. Balanced NRZ signals are accepted at the equipment side and are converted to unbalanced conditioned diphase at the cable side. Various lengths of CX-11230 cable may be driven, depending upon the data rate as follows:

Rate (kb/s)	Maximum Dist. (km)
Up to 576	3.2
1024 to 2304	1.6
4096 and 4608	0.8

At rates of 256 kb/s or higher, the GM also must handle an orderwire channel and a telemetry channel. The orderwire may be either a VINSON, which is a 16 kb/s digital signal, or an analog signal whose band is 300 to 3400 cps. It is desirable that the analog orderwire channel use only passive components in the GM. The telemetry channel is a 2 kb/s balanced NRZ signal.

TABLE 10-1

GROUP MODEM FUNCTIONAL REQUIREMENTS

Function		Modem		
		Diphase	Dipulse	[illegible]
Group Rates kb/s		128, 256, 512, 1024 2048, 4096 - 72, 144, 288, 576, 1152, 2304, 4068 - 1536	288, 576, 1152, 2304	[illegible]
Equipment Side Interface		Balanced NRZ data and Timing		
Line Side Interface (Unbalanced)	Modulation	Conditioned Diphase	Dipulse	[illegible]
	Distance	3.2 km @ 576 kb/s 1.6 km @ 2304 kb/s 0.8 km @ 4608 kb/s	1.6 km	0.8 km
	Cable	CX-11230	CX-11230	CX-[illegible]
	Rate	Same as Group Rate	2304 kb/s	[illegible]
	Power	-	dc loop back	[illegible]
	Eqpt	RLGM, RMC,	TD-754 TD-206	TD-[illegible] TD-[illegible]
Orderwire		One channel for 2 kb/s telemetry and 16 kb/s digital or 300-3400 Hz analog	Analog compatible with TD-754	Analog compatible with TD-[illegible]
BITE & Telemetry		BITE locates faults to a single plug-in module.		
Timing Options		a) Transmit timing derived from related clock. b) Transmit timing derived from receive group signal.		
MTBF		6000 hrs		
Power		115 V ± 10% at 50, 60, and 400 Hz or 28 V + 4, -6 V dc, 120 watts max.		
Size		8.5 h x 12 d x 1 3/4 w for 19" rack mount		
Weight		15 kg.		

Note: Diphase Modem and Dipulse Interface have a Black Station clock output at the Group Rate on the Equipment Side.

A Station Clock output is available on the equipment side at the group rate, and is derived from the recovered timing on the receive side.

10.1.2 DIPULSE GM

The dipulse GM handles traffic on the equipment side at rates of 288, 576, 1152 and 2304 Kb/s, and in each case transmits data over the cable at 2304 Kb/s. Balanced NRZ signals are accepted at the equipment side and are converted to dipulse signals for transmission over CX-11230 cable at distances up to 1.6 Km for unrepeatered systems. When used with a repeatered cable syste, loopback of the incoming power feed is provided. Also, an analog orderwire channel can be handled by the dipulse GM. A high transmit level is required for the repeatered case, so therefore the orderwire will not be passive.

10.1.3 BIPOLAR GM

The bipolar GM handles traffic at 4.9152 Mb/s. Balanced NRZ signals are accepted at the equipment side and are converted to bipolar signals to be transmitted over CX-11230 cable at distances up to 0.8 Km in an unrepeated system. When used with a repeated cable system, loopback of the incoming power feed is provided.

Also, an analog orderwire (300 to 1700 Hz) must be transmitted over the cable. A high transmit level is required for the repeated case, so that orderwire will not be passive.

10.2 DESIGN APPROACH

The original concept of the Group Modem was that it could contain any mix of various GM's and rates, with a maximum of 12 GM PCB's per case (see Figure 10-1). Due to the complexity of the diphase GM and the PCB area required by various filters, the circuitry cannot be located on one PCB. Since the diphase GM requires two PCB's, it has a maximum capability of six GM's per case.

The diphase GM employs a type of Frequency Division Multiplexing, where for rates of 256 KHz or higher, the diphase data is put on the cable without a filter, the VINSON and telemetry signals are combined digitally and transmitted at baseband through a low pass filter. Other approaches have been considered, a TDM approach, a space division multiplex approach, and a multisampling approach. These approaches are discussed in paragraph 2.1.2.

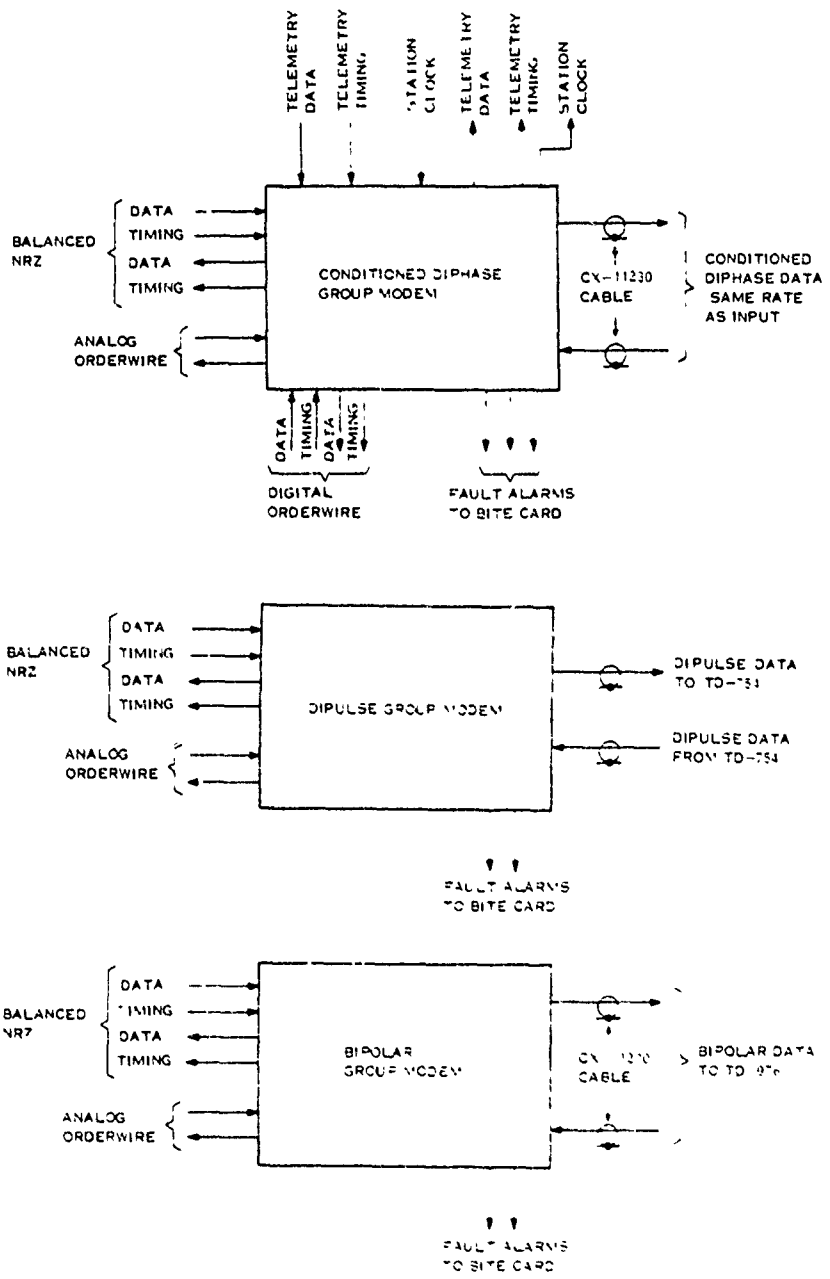


Figure 10-1. Group Modem Block Diagram

The dipulse GM design concept is fairly straightforward. as the orderwire is comparatively simple. Here, the audio is put at baseband and the dipulse occupies the upper end of the frequency spectrum.

The bipolar GM design concept is similar to the diphase GM concept, except for the different waveform and bit rate at the cable interface.

10.3 DETAILED DESIGN DESCRIPTION

10.3.1 DIPHASE GM TRAFFIC CIRCUITS

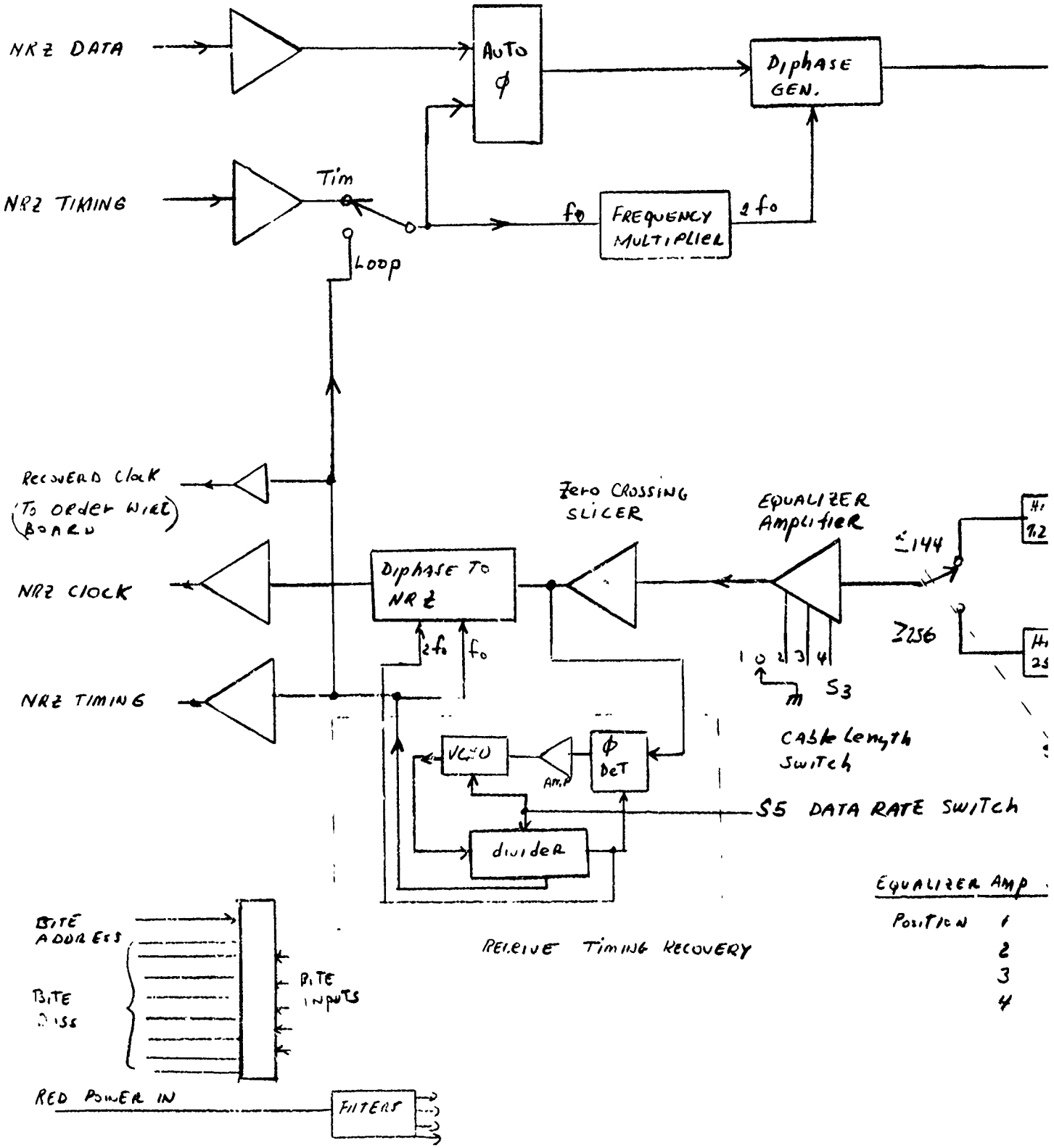
Equipment side inputs to the diphase GM are balanced NRZ data, timing and station clock. Balanced inputs are terminated in 100 ohms. Figure 10-2 shows a block diagram of the diphase GM, traffic circuits.

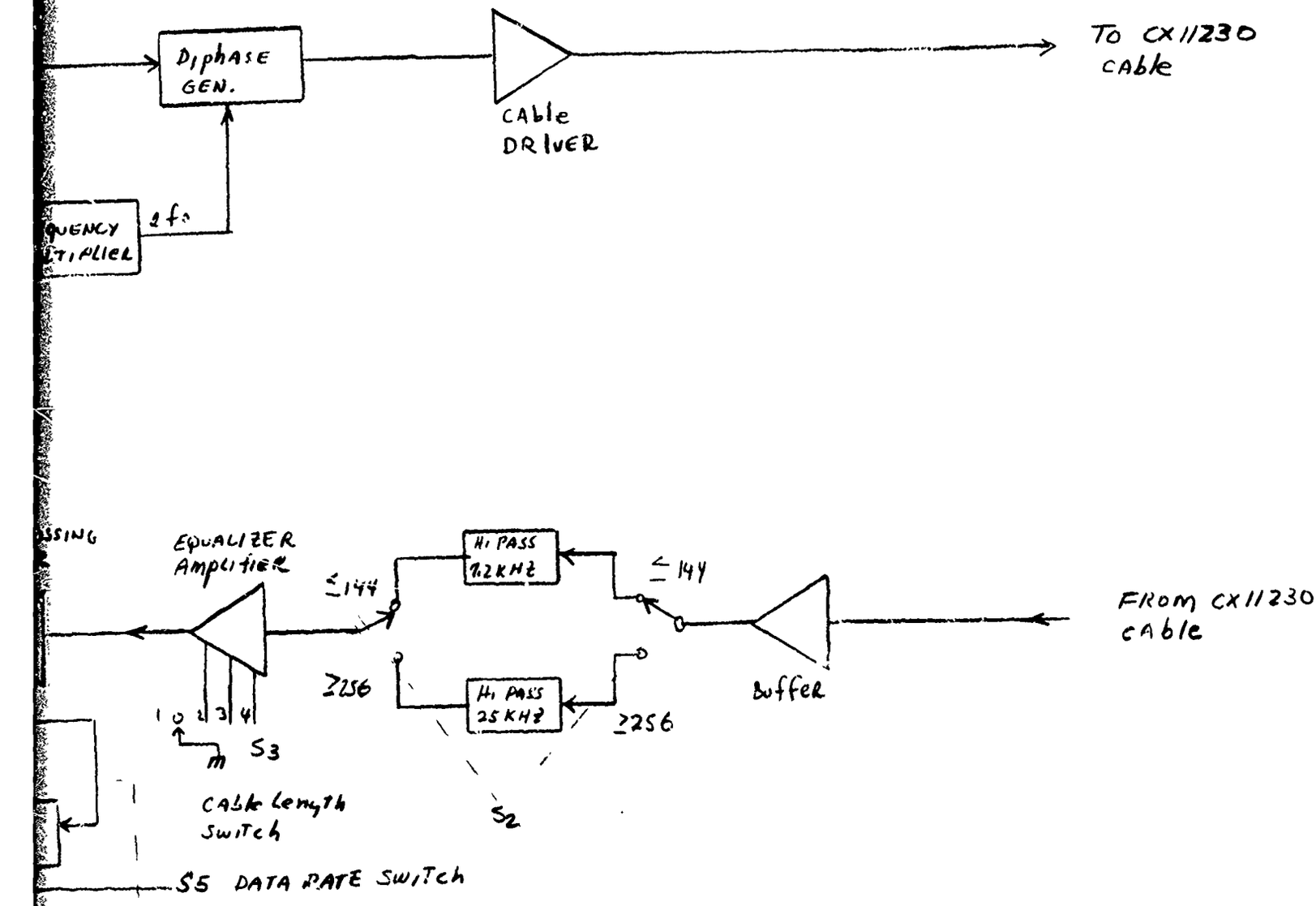
Since data is to be retimed by the recovered clock, an automatic phasing circuit is required to compare the phase of the recovered clock with that of the input group data. In this manner, the proper phase of the recovered clock can be used to retime the data.

The transmit timing utilizes either the equipment NRZ timing (TIM) or the timing recovered from the received cable data (loop). This option is switch selectable.

The incoming NRZ data is converted to diphase using the 2 f_o clock generated by using both the positive and negative transitions of the incoming data rate clock. The diphase generator output drives a cable driver which in turn delivers 3 Vpp to the CX 11230 cable.

Diphase data received from the CX11230 cable enters the board via a buffer. The buffer output drives a two pole high pass filter which is used to separate the diphase data and the orderwire signals. The high pass filter cutoff frequency is switch selectable at 7.2 kHz or 25 kHz.


NRZ DATA
AUTO φ
DIPHASE GEN.
NRZ TIMING
Tim
Loop
fo
FREQUENCY MULTIPLIER
2 fo
RECOVERD CLOCK
(To order wire board)
NRZ CLOCK
NRZ TIMING
DIPHASE TO NRZ
Zero Crossing SLICER
EQUALIZER Amplifier
≤144
≥256
1 0 2 3 4
m
S3
CABLE Length Switch
VCXO
AMP
φ DET
divider
S5 DATA RATE SWITCH
BITE ADDRESS
BITE INPUTS
RED POWER IN
FILTERS
RELAY TIMING RECOVERY
EQUALIZER AMP
Position 1
2
3
4



EQUALIZER AMP SWITCH S3

POSITION	1	0 cable Length
	2	≥ .4km < .8Km
	3	≥ .8km < 1.6 KM
	4	≥ 3.2 KM

Figure 10-2. Conditioned Diphase Traffic Circuits

The filter output drives an equalization amplifier. The equalization amplifier is designed to equalize the maximum cable length flat, to the maximum bit rate, for that length according to the following table:

Max Cable Length (km)	Max Frequency (kHz)
3.2	576
1.6	2304
0.8	4608

Figure 10-3 shows the frequency response for the cable up to the maximum frequency to which it will be equalized. The equalizer is a single pole and is switched according to cable length. The equalizer is switched out for the situation where there is 0 cable length such as during loopback at the GM case. The other three switch positions are utilized for the .8, 1.6 and 3.2 km cable lengths.

The output of the equalizer drives a zero axis crossing detector. The output of the axis crossing detector drives a timing recovery phase lock loop, and a diphase to binary converter.

The timing recovery loop utilizes a crystal VCXO which has two center frequencies (9216 kHz and 8192 kHz). The VCXO center frequency is selectable via a control input that responds to logic levels. The VCXO frequency selection is a function of whether the group rate is a multiple of 144 kHz or 128 kHz.

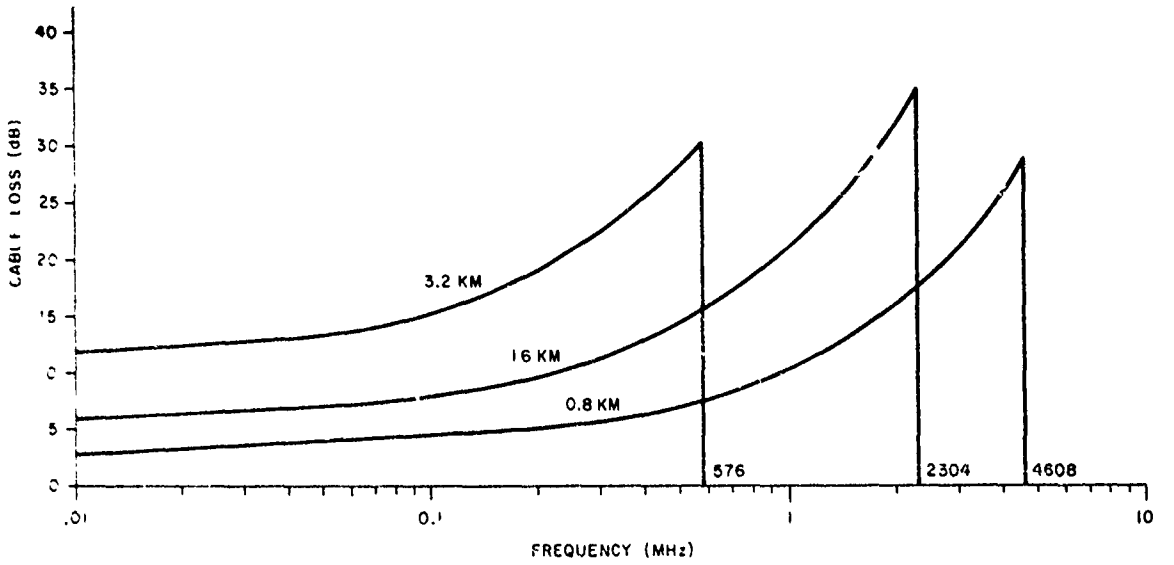


Figure 10-3. Attenuation of CX11230 Cable

The VCXO output is either passed straight through or divided as a function of the rate code switch. (See Figure 10-4 Diphase Group Modem Receive Timing Recovery). The rate selector is controlled by the rate switch. Table 10-2 lists the group rates and the rate codes generated by the 16 position rate switch. The same rate codes are proposed for the TGM and MGM with code 15 reserved for 4915.3 kHz.

The output of the timing recovery divider is compared to the incoming data in a D Flop Phase Detector. The resulting phase comparison is filtered in the amplifier that follows and applied to the control inputs of the VCXO. The timing recovery yields a data rate clock f_o and a 2 times data rate clock $2 f_o$. These clocks are required by the diphase to binary conversion circuits that follow the zero axis crossing detector (see Figure 10-5).

10.3.2 DIPHASE GM ORDERWIRE CIRCUITS

Equipment side VINSON data and telemetry data enter the modem via balanced NRZ inputs. The VINSON and telemetry data signals are compared to

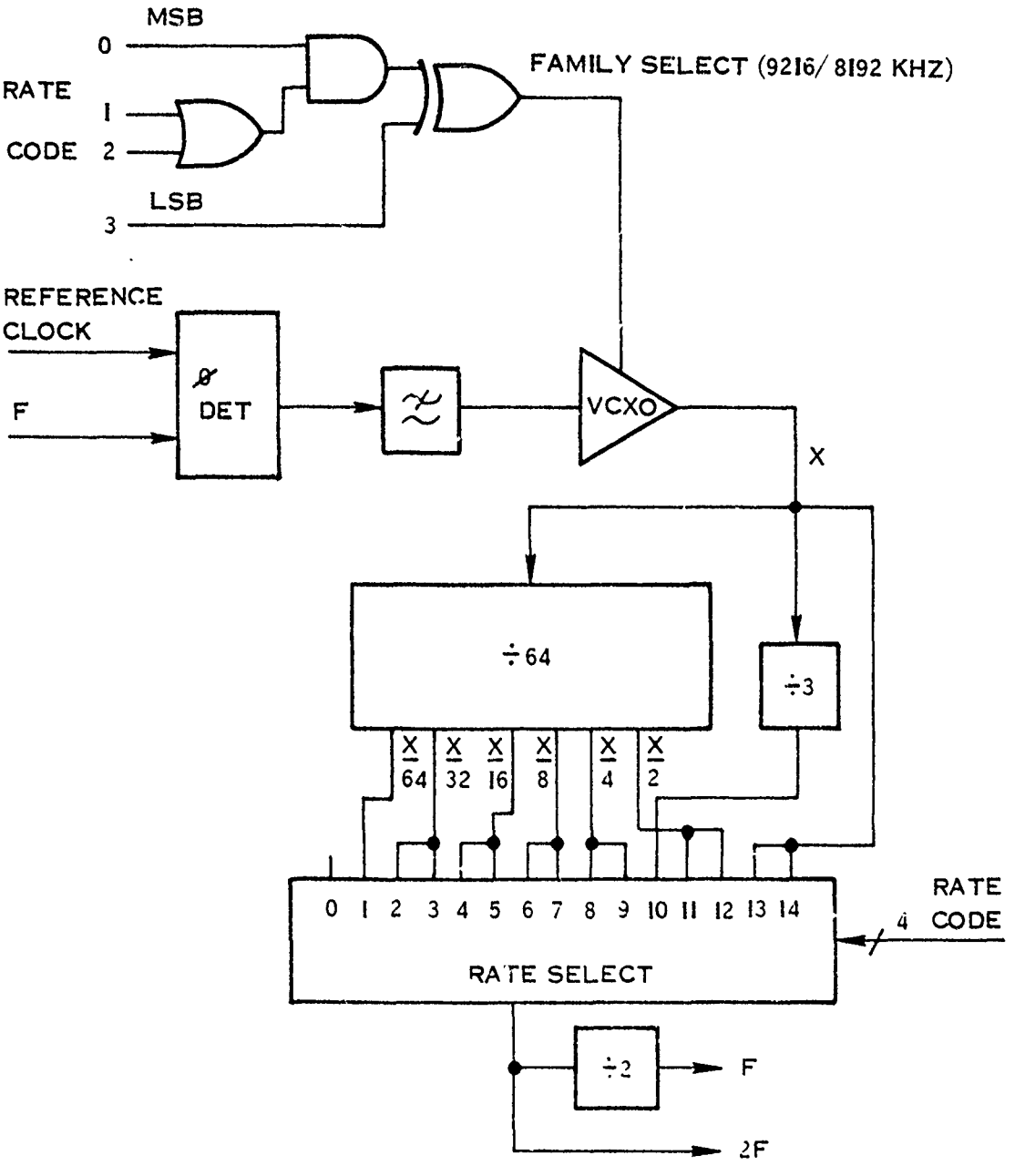


Figure 10-4. Diphase Group Modem Receive Timing Recovery

TABLE 10-2

DIPHASE GROUP TIMING

Rate Number	Rate Code	Rate (kHz)	Rate Family
0	0000	OFF	-
1	0001	72	A
2	0010	128	B
3	0011	144	A
4	0100	256	B
5	0101	288	A
6	0110	512	B
7	0111	576	A
8	1000	1024	B
9	1001	1152	A
10	1010	1536	A
11	1011	2048	B
12	1100	2304	A
13	1101	4096	B
14	1110	4608	A

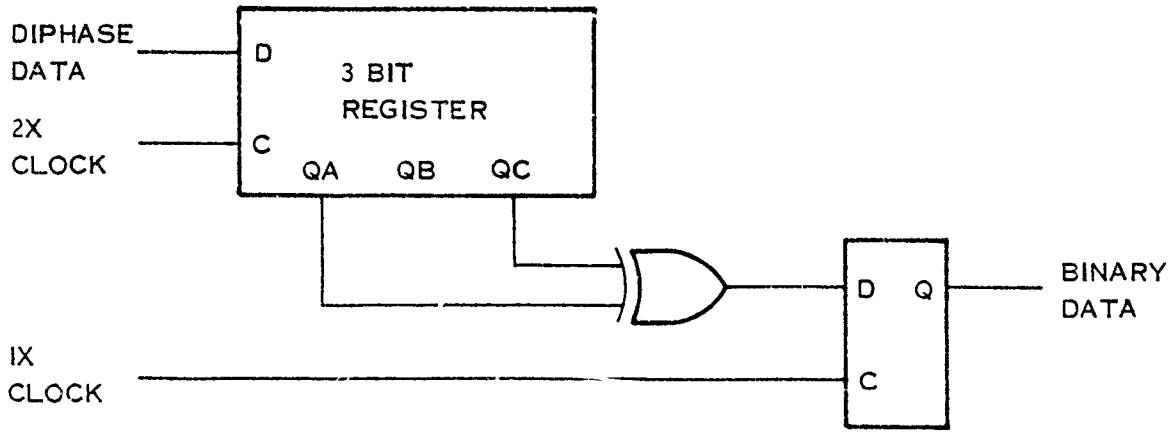


Figure 10-5. Diphase to Binary Converter

16 kHz and 2 kHz clocks, respectively, in an autophase circuit. The 16 kHz and 2 kHz clocks are generated by dividing the 32 kHz station clock. The autophase circuit establishes a clock phase that is used to sample the incoming data (see Figure 10-6).

The method for retiming randomly phased data with recovered clock is shown in Figure 10-7. This circuit uses two "one-shot" circuits to test the phase of the data relative to the recovered clock. The first one-shot generates a test window which is 2T nanoseconds in width following a positive transition of the data input. The second one-shot delays the retiming clock by T nanoseconds. If the delayed clock falls within the test window, a JK flip-flop changes state and inverts the retiming clock, changing its phase by half a bit time. The second retiming flip-flop is always clocked with the station clock so that the output data phase is independent of the phase of the input data.

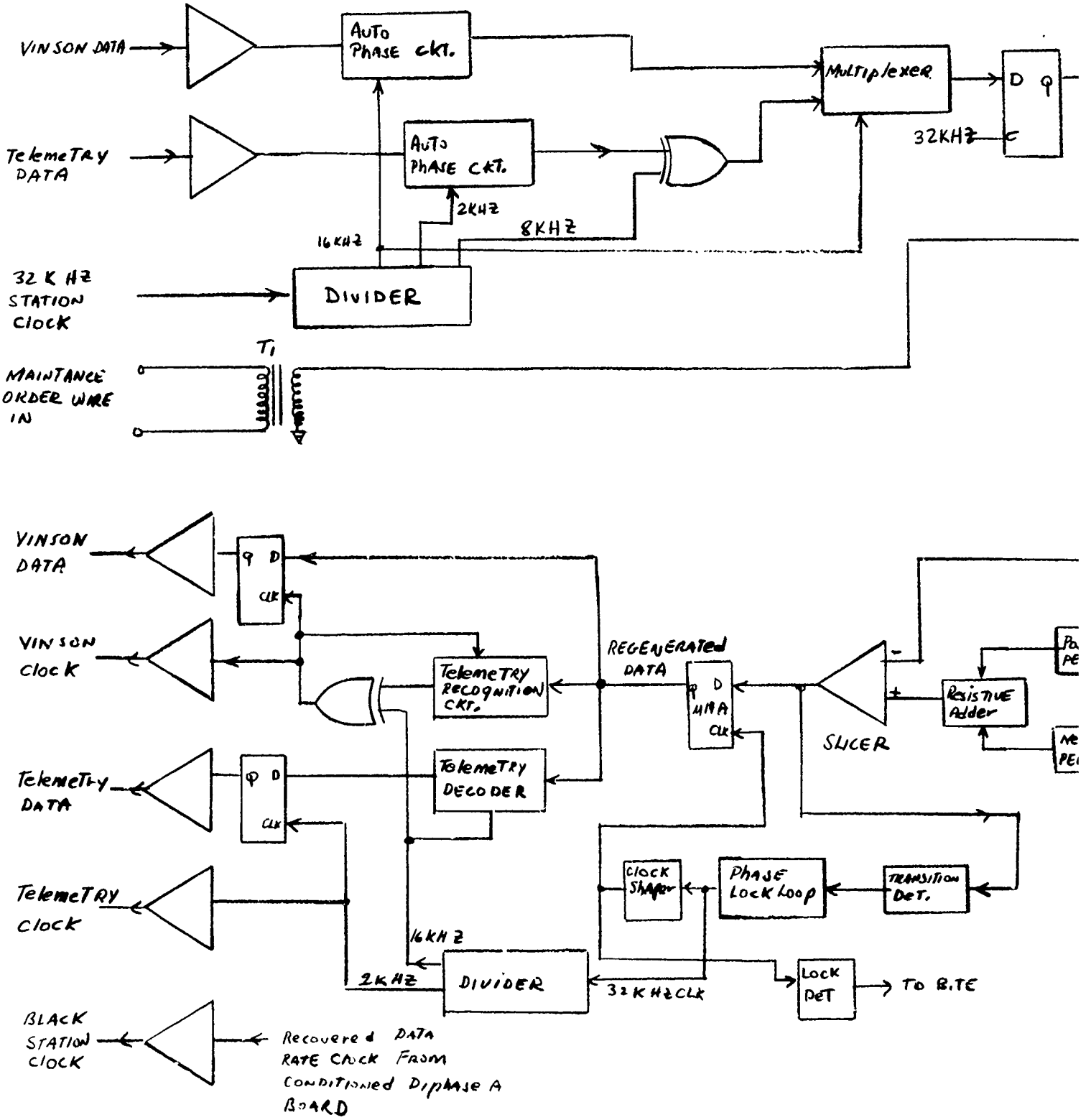
The output of the telemetry autophase circuit is summed in an exclusive or gate with an 8 kHz clock. The 8 kHz clock is phased such that it is set low (digital 0) at the transitions of the telemetry data.

The resulting telemetry added to the 8 kHz clock, and the Vinson data are multiplexed together at a 32 kHz rate. Alternate samples are taken of telemetry and Vinson data. The multiplexer output is retimed and put on the CX11230 cable via a driver followed by a low pass filter. The filter is a 4-pole butterworth with a 20 kHz cutoff. The orderwire level into the cable is 1 volt peak-to-peak.

The switch S_1 selects the orderwire type used, position SOW selects the secure orderwire and position MOW selects the maintenance orderwire. The maintenance orderwire may be used at all diphase traffic rates. The secure orderwire may be used at diphase traffic rates of 256 kb/s or greater.

The maintenance orderwire enters the modem through transformer T_1. The transformer output is applied directly to the cable through a series resistor used to maintain the proper audio termination. The maintenance orderwire is passive and can be used without power applied to the GM.

Receive digital orderwire signals from the CX11230 cable enter the modem via a buffer. The analog maintenance orderwire enters the modem through an audio transformer.


VINSON DATA
AUTO PHASE CKT.
MULTIPLEXER
D Q
32KHZ
C
TELEMETRY DATA
AUTO PHASE CKT.
2KHZ
8KHZ
16KHZ
32 K HZ STATION CLOCK
DIVIDER
T1
MAINTANCE ORDER WIRE IN
VINSON DATA
VINSON CLOCK
TELEMETRY DATA
TELEMETRY CLOCK
BLACK STATION CLOCK
Q D
CLK
TELEMETRY RECOGNITION CKT.
TELEMETRY DECODER
REGENERATED DATA
D
UMA
CLK
SLICER
RESISTIVE ADDER
CLOCK SHAPER
PHASE LOCK LOOP
TRANSITION DET.
16KHZ
2KHZ
DIVIDER
32KHZCLK
LOCK DET
TO B.TE
Recovered DATA RATE CLOCK FROM CONDITIONED DIPHASE A BOARD

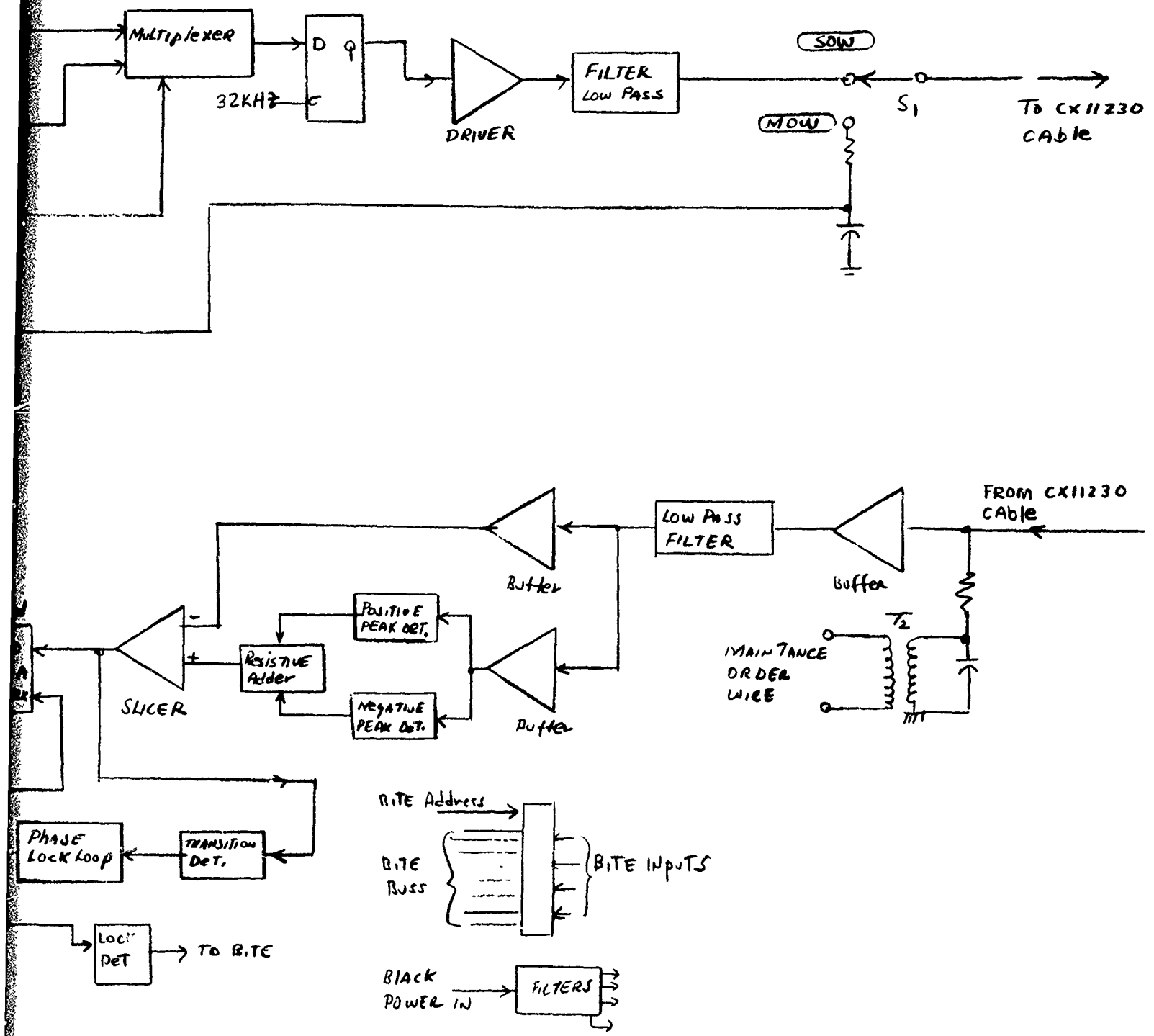
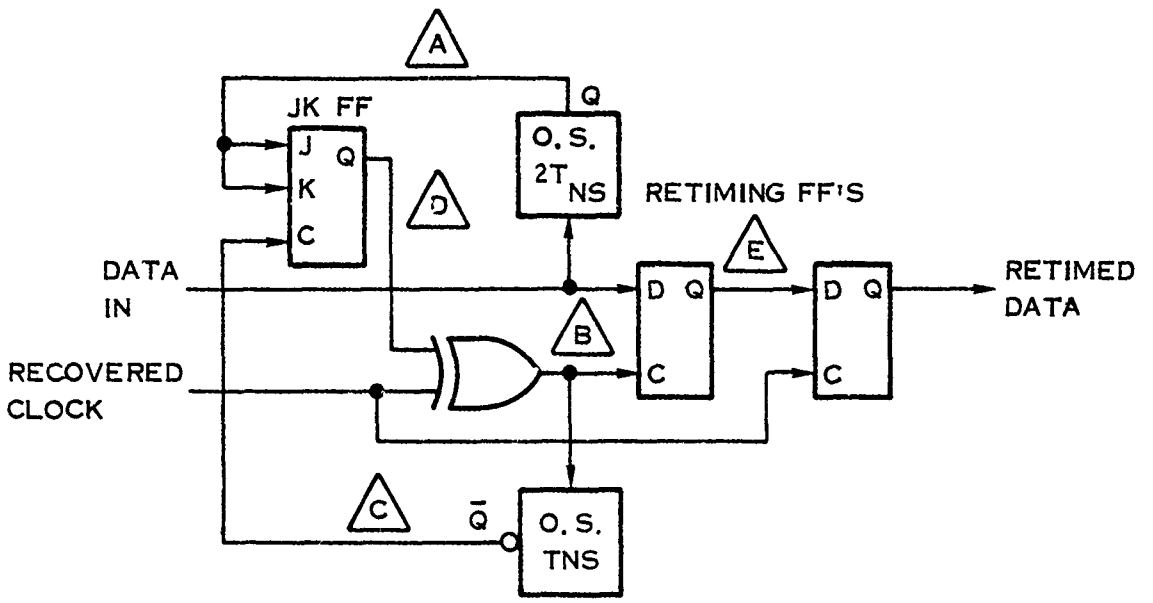


Figure 10-6. Conditioned Diphase Orderwire Circuits



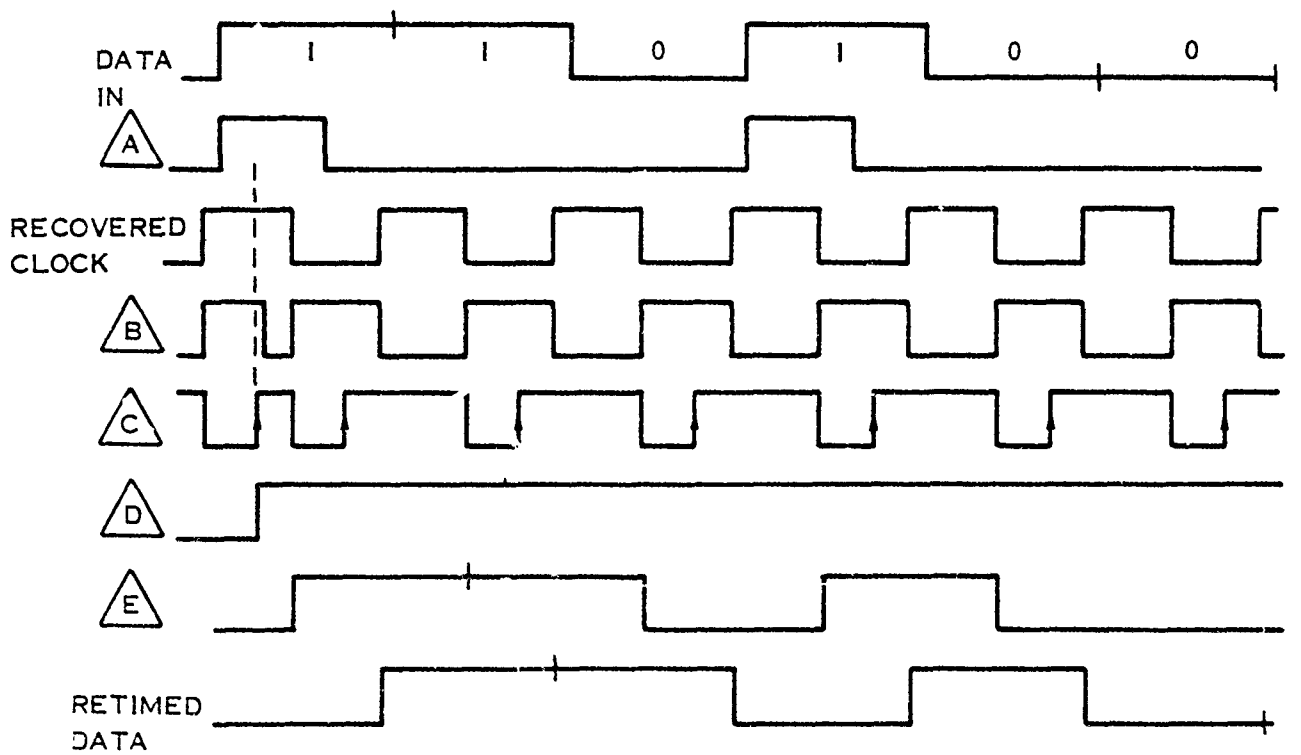


Figure 10-7. Autophase Circuit Block Diagram

The incoming cable signal is passed through a low pass filter that separates the composite digital orderwire and diphase traffic. The filter output is fed to two buffers. One buffer drives a positive and negative peak detector. The outputs of these peak detectors is summed in a resistive adder and the mean voltage is used as the digital data slicing level. The other buffer drives the data slicer.

The sliced data output is fed into a data transition detector. A phase lock loop is used to extract timing from the data transitions.

The output of the pulse lock loop is shaped by a clock shaper. The regenerated data is fed into a telemetry recognition circuit. The telemetry recognition circuit performs the function of separating the multiplexed Vinson and telemetry data. The recognition technique makes use of the fact that in an error free environment the telemetry signal contains no more than two ones or two zeros in a row. The separation is performed as follows: The data bit sampled is assumed to be telemetry. The time slot is continually examined for 8 logic 1's or 8 logic 0's in a row. If either of the above tests is successful, the channel is recognized as being Vinson (see Figure 10-8).

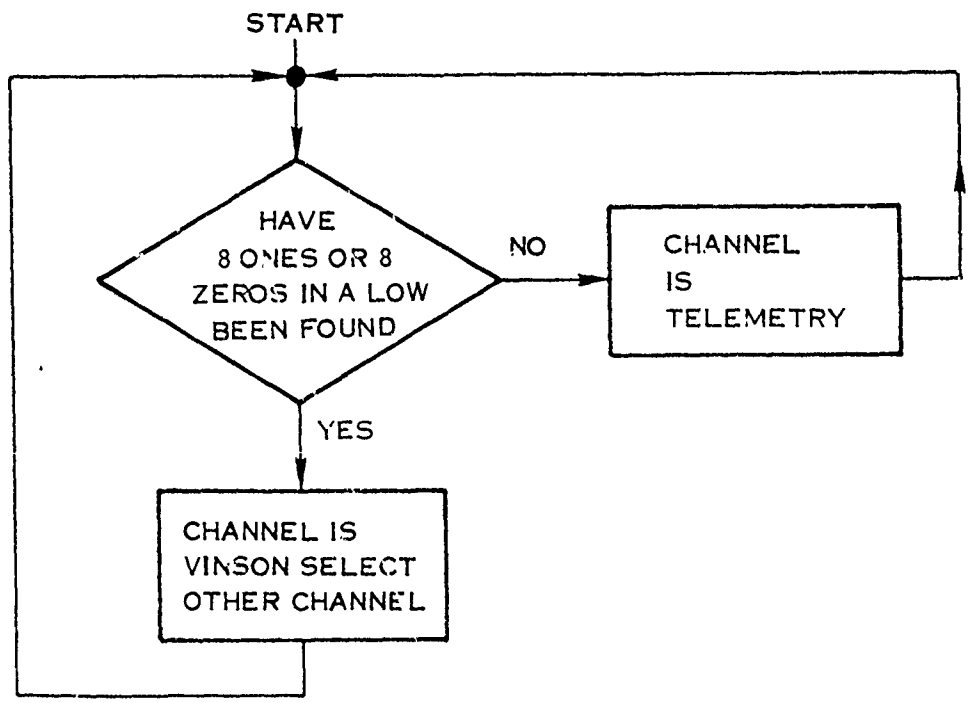


Figure 10-8. Telemetry Recognition Logic

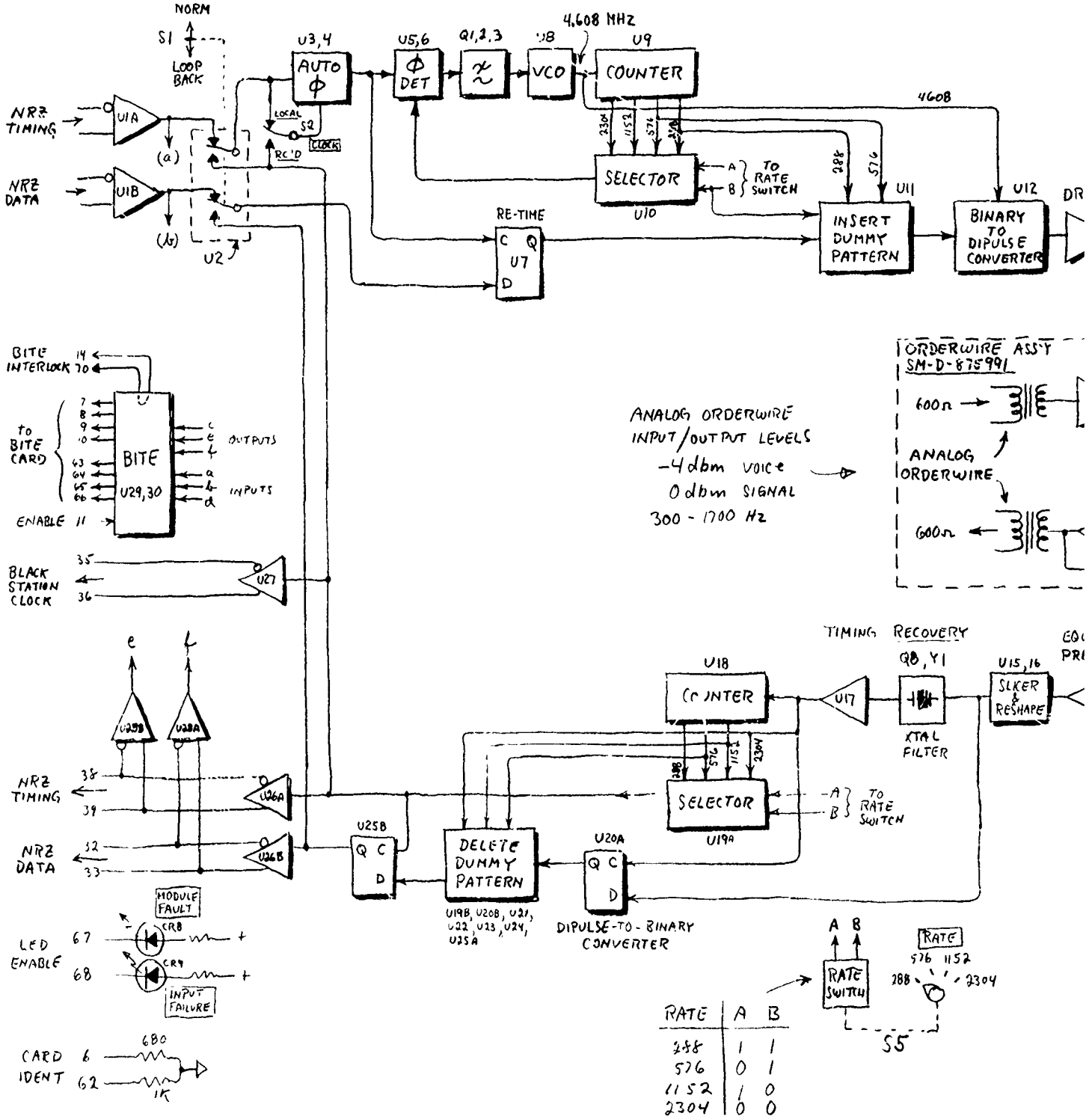
The telemetry data is regenerated in the telemetry decoder circuit. Two ones in a row in the telemetry data stream denotes a low to high logic transition. Two zeros in a row denotes a high to low logic transition. The regenerated telemetry data along with its associated clock are put out on the equipment side balanced NRZ interface.

The Vinson data is retimed with the 16 kHz clock and both clock and data are put out on the equipment side on balanced NRZ interfaces.

10.3.3 THE DIPULSE MODEM

Figure 10-9 is a block diagram of the dipulse modem. A simplified block diagram of the Cable Orderwire is included to show how it connects to the Dipulse modem. Balanced NRZ data and timing inputs are connected via shielded twisted pair to separate line receivers U1. The TTL outputs of U1 go to switch U2 which selects either local data and timing (the NORMAL condition) or the received data and timing from the remote TD-754 multiplexer (the LOOP BACK condition). U2 is shown as a DPDT mechanical switch which is functionally the same as the actual TTL logic gates in U2, but is easier to follow when describing the circuit. Timing signals go to an Auto-Phase circuit U3, 4 where they are compared with timing from a remote TD-754 (when S2 is in the RCD position) and the proper phase is automatically selected for retiming the data to the remote clock. When S2 is in the LOCAL position, local timing is unaffected by the Auto-Phase circuit. Data is retimed in U7 and then processed in a Dummy Pattern Insert Circuit U11. The various rates required for dummy pattern insert and binary-to-dipulse conversion are derived from the input timing in a phase locked oscillator and counter circuit comprising U5, 6, 8, 9 and 10. Switch S5 sets selector U10 to the input rate. This circuit supplies rates of 4608, 2304, 1152, 576, and 288 kHz.

The Dummy Pattern Insert circuit (see Figure 10-10) interleaves a 288 kHz pattern with 288 and 576 kb/s data to meet the requirements of the TD-754 multiplexer to which the modem is connected. This insert circuit is active only at the 288 and 576 kb/s data rates. The 1152 and 2304 kb/s data pass through unchanged. The processed signal that appears at the output of U11 is converted to 2304 kb/s dipulse in converter U12. A driver amplifier Q4, 5, 6 buffers the converter from the low impedance cable, and L1, C19 differentiate the output square waves to get the desired dipulse waveshape on the cable. A building-out network


NORM
S1
LOOP BACK
U3,4
AUTO Φ
U5,6
Φ DET
Q1,2,3
VCO
U8
4.608 MHz
U9
COUNTER
4608
NRZ TIMING
U1A
(a)
NRZ DATA
U1B
(b)
U2
LOCAL
S2
CLOCK
RC'D
2304
1152
576
288
SELECTOR
U10
A
B
TO RATE SWITCH
RE-TIME
C Q
U7
D
U11
INSERT DUMMY PATTERN
U12
BINARY TO DIPULSE CONVERTER
DR
BITE INTERLOCK
14
70
to BITE CARD
7
8
9
10
63
64
65
66
BITE
U29,30
c
e
f
OUTPUTS
a
b
d
INPUTS
ENABLE
11
BLACK STATION CLOCK
35
36
U27
ORDERWIRE ASSY
SM-D-875991
600Ω
ANALOG ORDERWIRE
600Ω
ANALOG ORDERWIRE INPUT/OUTPUT LEVELS
-4 dbm VOICE
0 dbm SIGNAL
300 - 1700 Hz
TIMING RECOVERY
Q8, Y1
U15,16
SLICER & RESHAPE
XTAL FILTER
U17
U18
COUNTER
e
f
U28B
U28A
NRZ TIMING
38
39
U26A
NRZ DATA
32
33
U26B
U25B
Q C
D
DELETE DUMMY PATTERN
U19B, U20B, U21, U22, U23, U24, U25A
U20A
Q C
D
DIPULSE-TO-BINARY CONVERTER
U19A
SELECTOR
A
B
TO RATE SWITCH
MODULE FAULT
LED ENABLE
67
68
CR8
CR9
INPUT FAILURE
CARD IDENT
6
62
680
1K
A B
RATE SWITCH
RATE
576 1152
288 2304
55
RATE | A | B
288 | 1 | 1
576 | 0 | 1
1152 | 1 | 0
2304 | 0 | 0

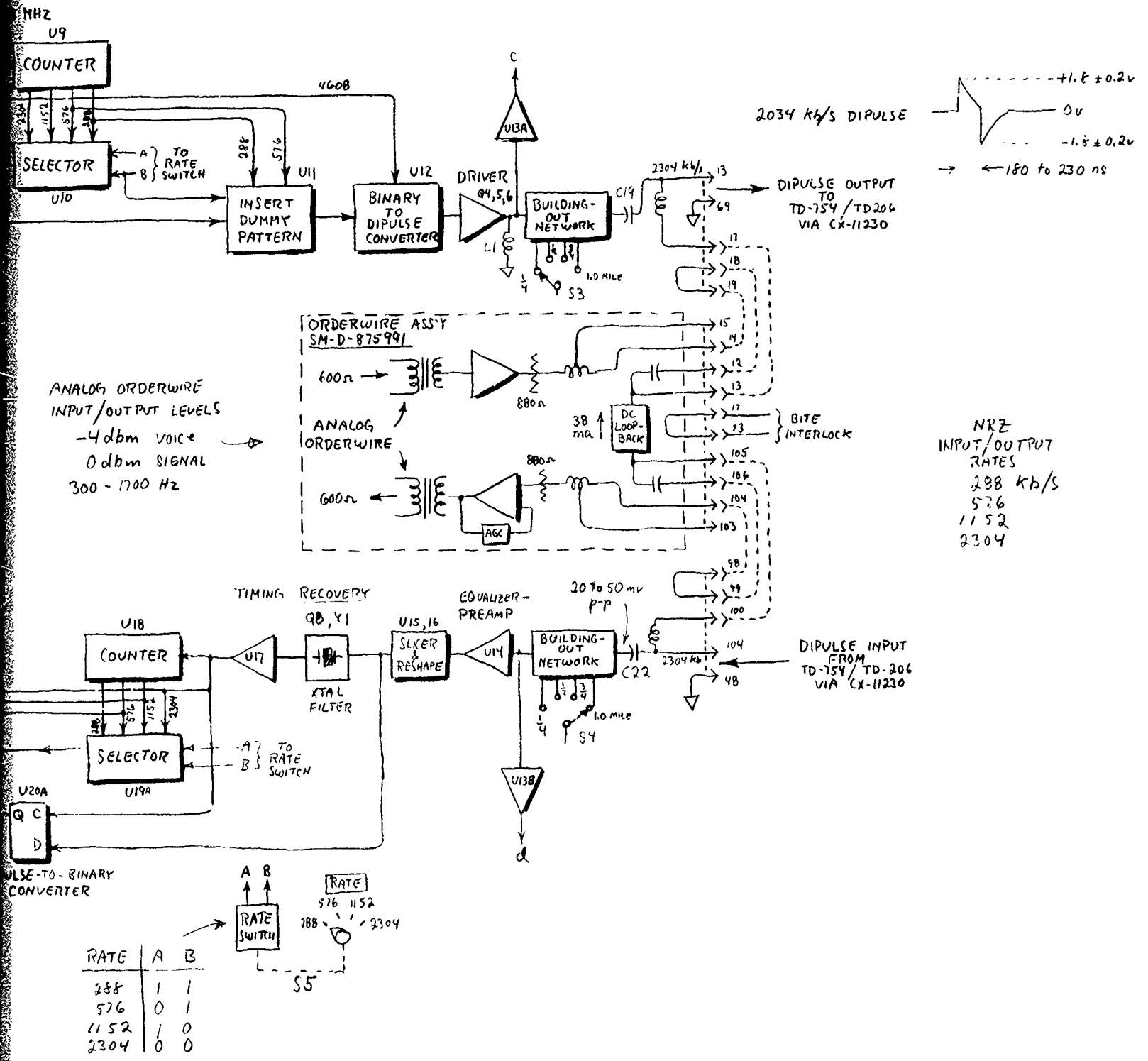
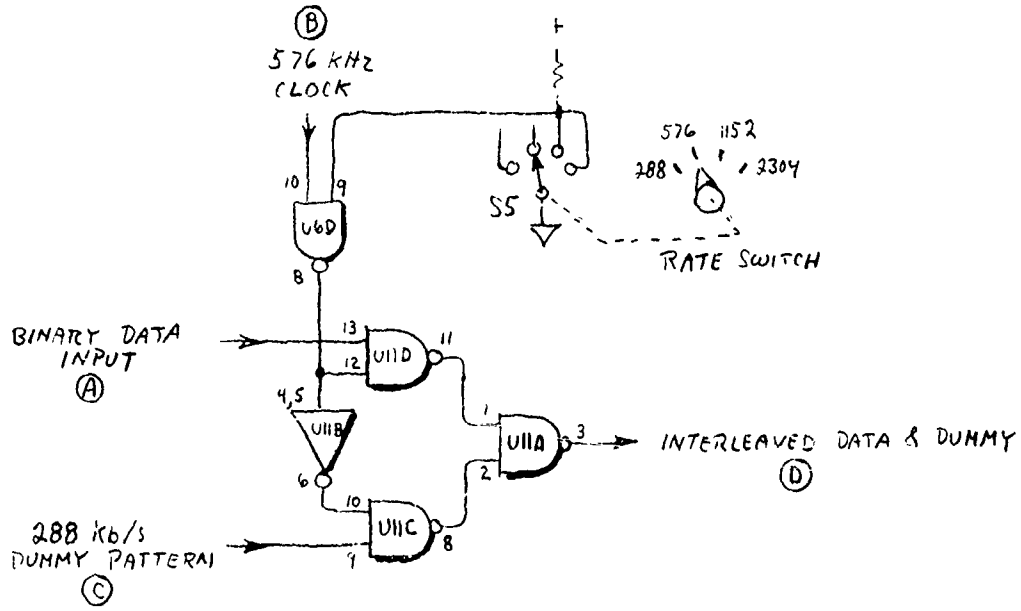


Figure 10-9. Dipulse Modem



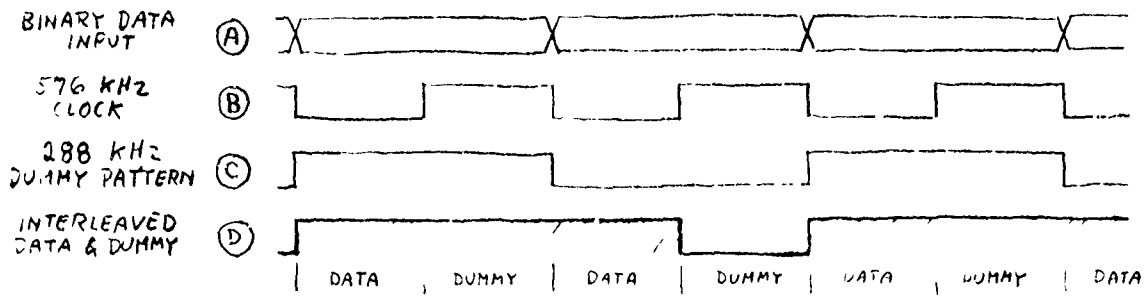


Figure 10-10. Dipulse Modem Dummy Pattern Insert Circuit

(Figure 10-11) compensates for various lengths of cable. Switch S3 sets the network to simulate CX-11230 cable in increments of 1/4 mile up to one mile.

Incoming Dipulse signals from a remote TD-754 (or TD-206 restorer) through a mile of CX-11230 cable are processed in the receive circuits comprising U14 through U25. A building-out network identical to that used in the transmitter assures that the input signal level and shape is always the same as that received through one mile of cable even though the actual cable length may be less. An equalizer-preamplifier U14 compensates for distortion of the signal caused by the attenuation versus frequency characteristic of the cable and amplifies the signal to a level suitable for reshaping in the slicer U15, 16.

Timing is recovered from the data by means of narrowband crystal filter Y1, Q8 that is tuned to the 2304 kHz diphase rate. U17 converts the sinewave output of the filter to TTL logic levels to drive counter U18 and Dipulse-to-Binary Converter U20A. Rate switch S5 sets multiplexer U19 to select the original data rate from outputs of counter U18. A "D" flip-flop U20A converts the reshaped

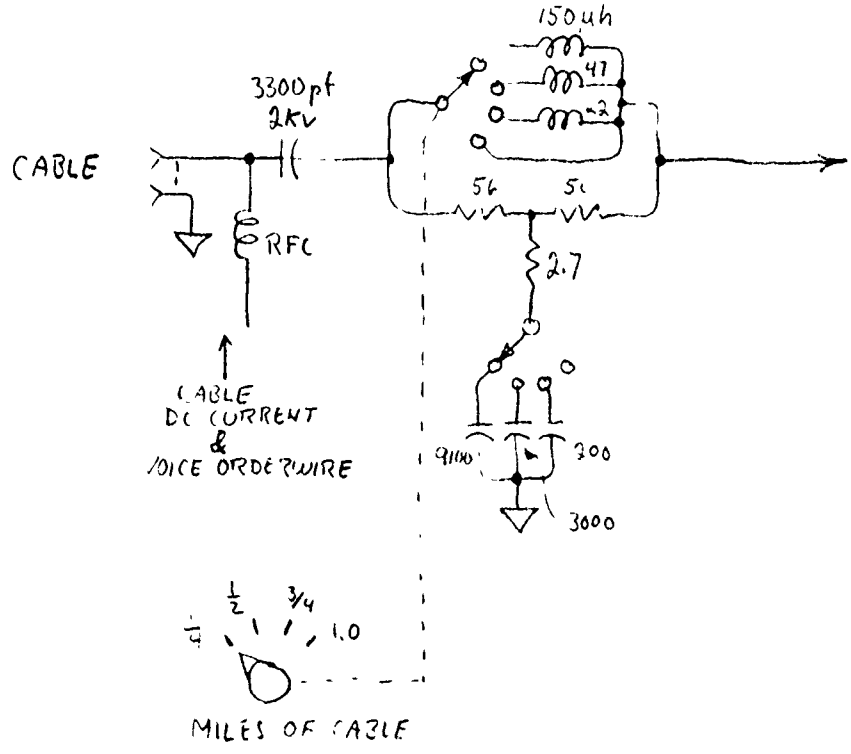


Figure 10-11. Building-Out Network for Dipuise Modem

dipulse output from the slicer U15, 16 to binary data at TTL logic levels for processing in a Delete Dummy Pattern circuit comprising U19 through U25. This circuit examines the incoming signal to determine the presence and location of a dummy pattern that is interleaved with the data by the remote TD-754 when only one 12 channel PCM input is present. This occurs only at the 576 and 288 kb/s rates, and the delete circuit is active only at these rates. The circuit then removes the interleaved dummy and restores the original binary data which is then retimed in U25B. Dual line driver U26 converts the TTL data and timing to balanced NRZ to interface with the shelter equipment.

Built-in test facilities provide monitoring of all input and output signals, both data and timing. A detector in the phase locked loop disables the dipulse output should an out-of-lock condition occur. All monitored points report to a separate BITE module in the Group Modem where the various samples are checked for activity. Lack of activity at any input will cause the BITE module to light LED CR9 on the Dipulse Modem. Failure of output activity will similarly cause CR8 to light. An interlock connection to the companion orderwire card will also cause a module fault alarm should this card be missing or be plugged into the wrong slot. Switch S1, which controls logic switch U2, permits loop-back of the received data and timing to the originating remote TD-754 for system tests.

A separate NRZ output for the received timing provides BLACK station clock through line driver U27.

The orderwire card must be used with the Dipulse card to provide loop-back of the dc cable current (required when TD-206 restorers are used) and analog voice communication on the cable. The same orderwire card is used with the Bipolar Modem, which requires a different value of loading coil inductance. A tapped loading coil is used for this purpose and the interconnections with the Dipulse and Bipolar modems (shown in Figure 10-9 and later in this Section Figure 10-15) are arranged to automatically select the proper loading coil inductance.

The Dummy Pattern Delete Circuit

The Dipulse modem must remove the dummy pattern that is interleaved with the data in the TD-754 multiplexer at the 576 and 288 kb/s rates. The data formats

for the four dipulse rates is shown on Figure 10-12. The dummy pattern delete circuit (Figure 10-13) is essentially the same as that used in the TD-754. Figure 10-14 shows the timing of some of the signals for a data rate of 576 kb/s.

Referring to Figures 10-13 and 10-14, the received reshaped dipulse input (A) and recovered 2304 kHz clock (B) are applied to a Dipulse-to-Binary converter, D flip-flop U20A, which recovers the interleaved data and dummy (C). The problem is to remove the dummy pattern from (C) so that the original binary data appears at (E). This is accomplished by applying a 576 kHz square wave of phase shown by (D) on Figure 10-14, to the clock input of U20B, whose Q output will be the original data (E_D on Figure 10-14). If the positions of the data and dummy in the interleaved signal are reversed, then it is necessary to reverse the polarity of (D) to recover the data. The function of the remainder of the dummy pattern delete circuit (U21 through U24) is to decide which part of the interleaved pattern at (C) is dummy and which part is data, and then apply the proper phase of (D) to U20B to recover data and delete the dummy. This is done as follows: The manually operated rate switch S5 is set to the data rate; 576 in this example. Signals are switched by an integrated circuit multiplexer U19 controlled by S5. U19 is shown as a selector switch to simplify the diagram. Functionally it is the same as the multiplexer. The output of U19A retimes the recovered data (E) in U25B. U19B selects the output (D) of exclusive OR gate U21A which passes the 576 kHz output of binary counter U18 unchanged, or reverses its polarity depending on the state of the second input, pin 10 of U21. If pin 10 is low, (D) is not inverted, and the clock input to U20B will appear as (D) on Figure 10-14 and the output (E) will be the original data (E_D). If pin 10 is high, (D) is inverted, and the U20B clock input will appear as shown at ($\overline{D}$) on Figure 10-14. In this case, the output (E) will be the dummy pattern ($E_{\overline{D}}$).

The circuit must decide which polarity of (D) is required to recover data and not the dummy pattern. The procedure is as follows: D (or $\overline{D}$ depending on whether U21A is inverting or not) is divided by 2 in U22A. The output will be 288 kHz or 288 kHz shifted 90° in phase (F_D or $F_{\overline{D}}$ on Figure 10-14). Signal F clocks U22B on alternate bits. If these alternate bits are data, there will be activity at (G) and retriggerable one-shot U24's $\overline{Q}$ output will switch low and stay there, leaving the state of flip-flop U25 unchanged to maintain the condition that

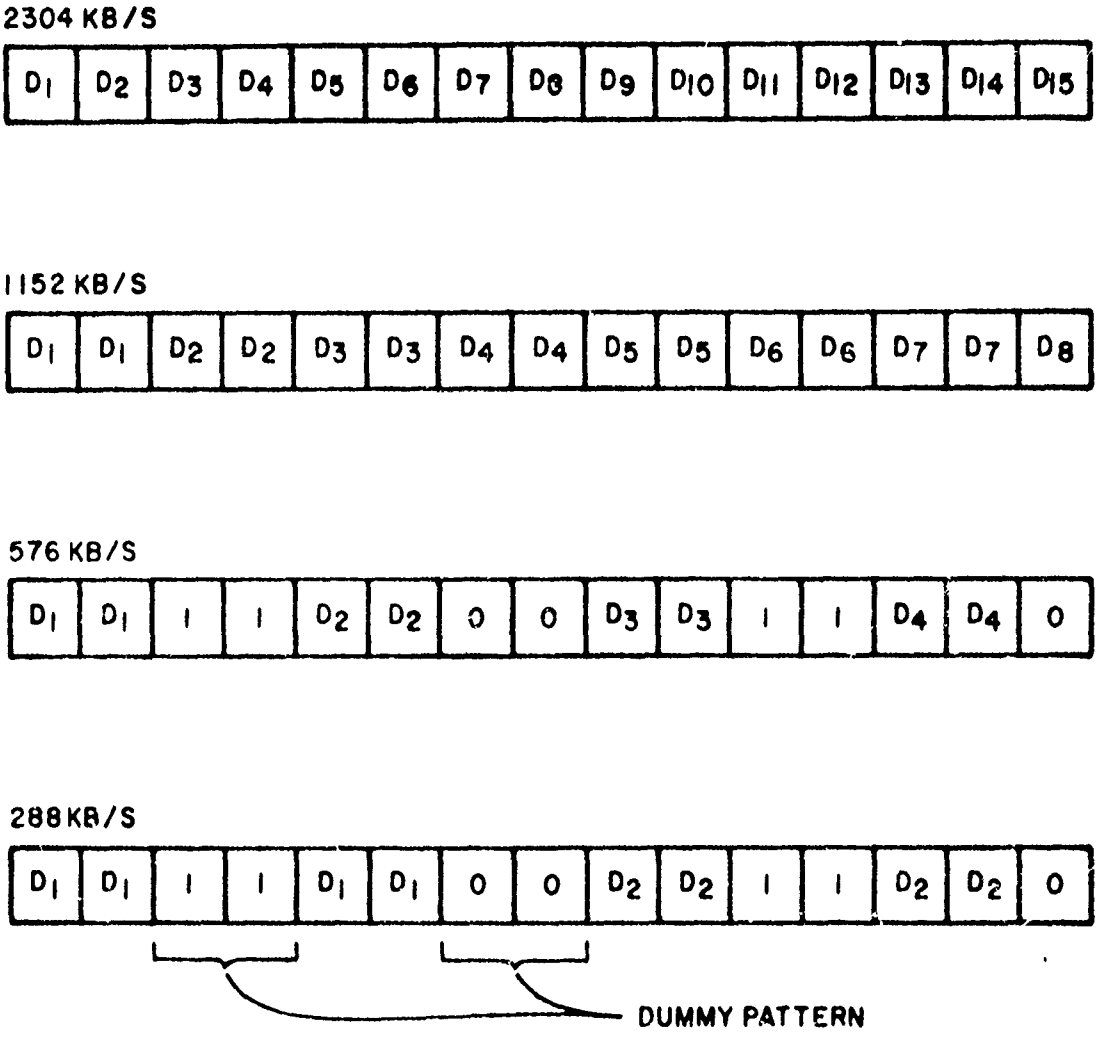
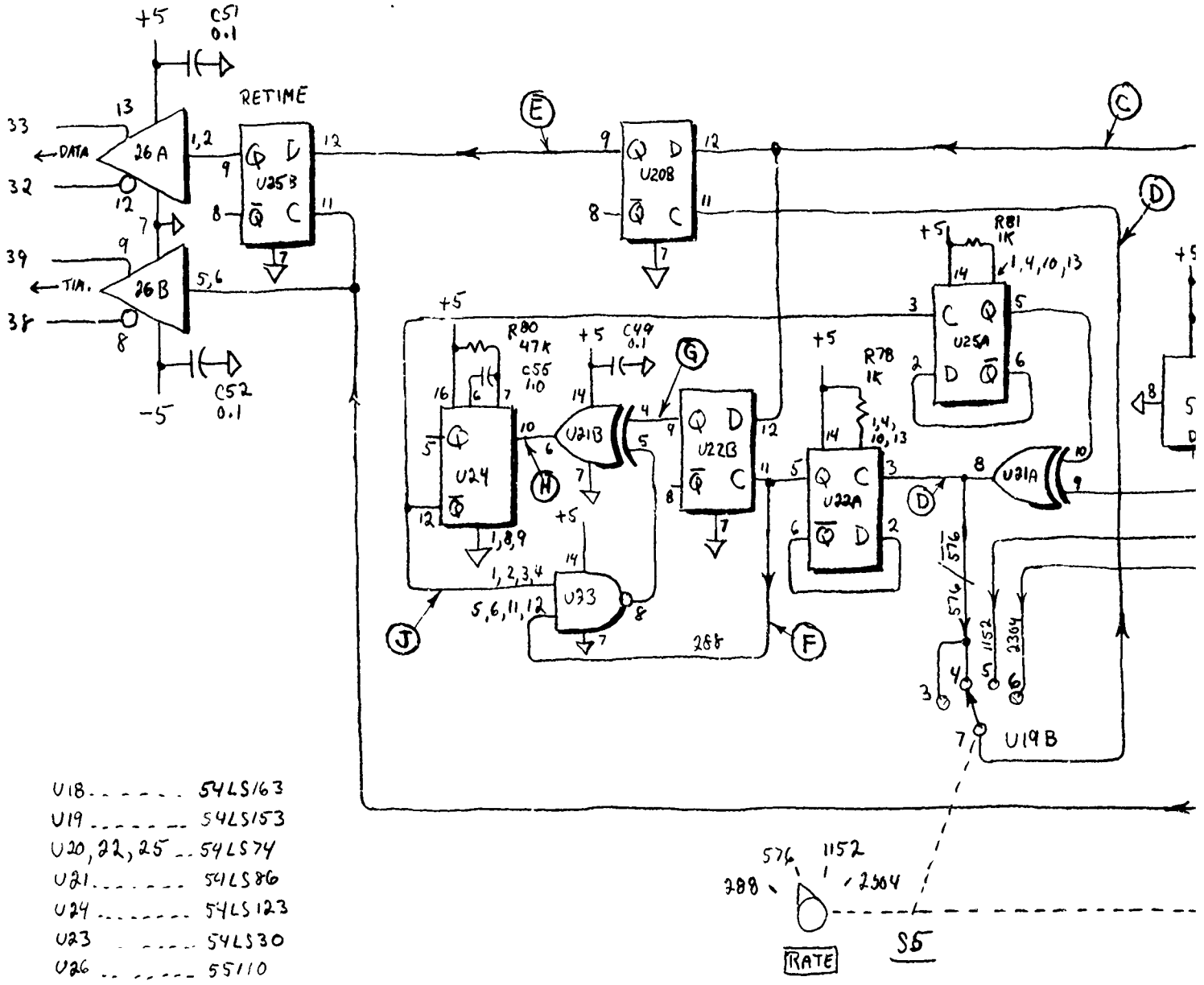


Figure 10-12. Dipulse Group Modem Data Formats



U18 . . . . . 54LS163
U19 . . . . . 54LS153
U20, 22, 25 . . 54LS74
U21 . . . . . 54LS86
U24 . . . . . 54LS123
U23 . . . . . 54LS30
U26 55110

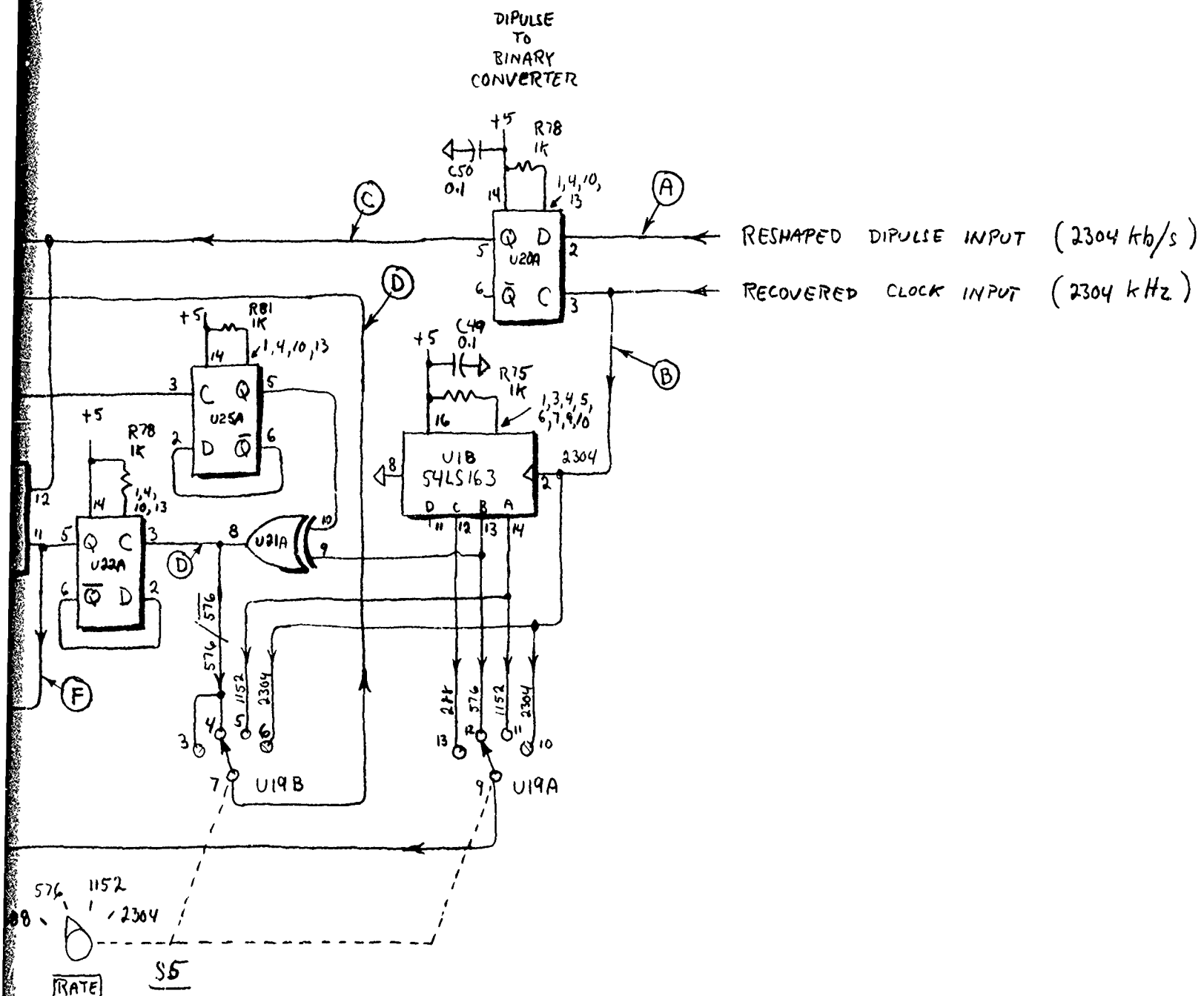


Figure 10-13. Dummy Pattern Delete Circuit

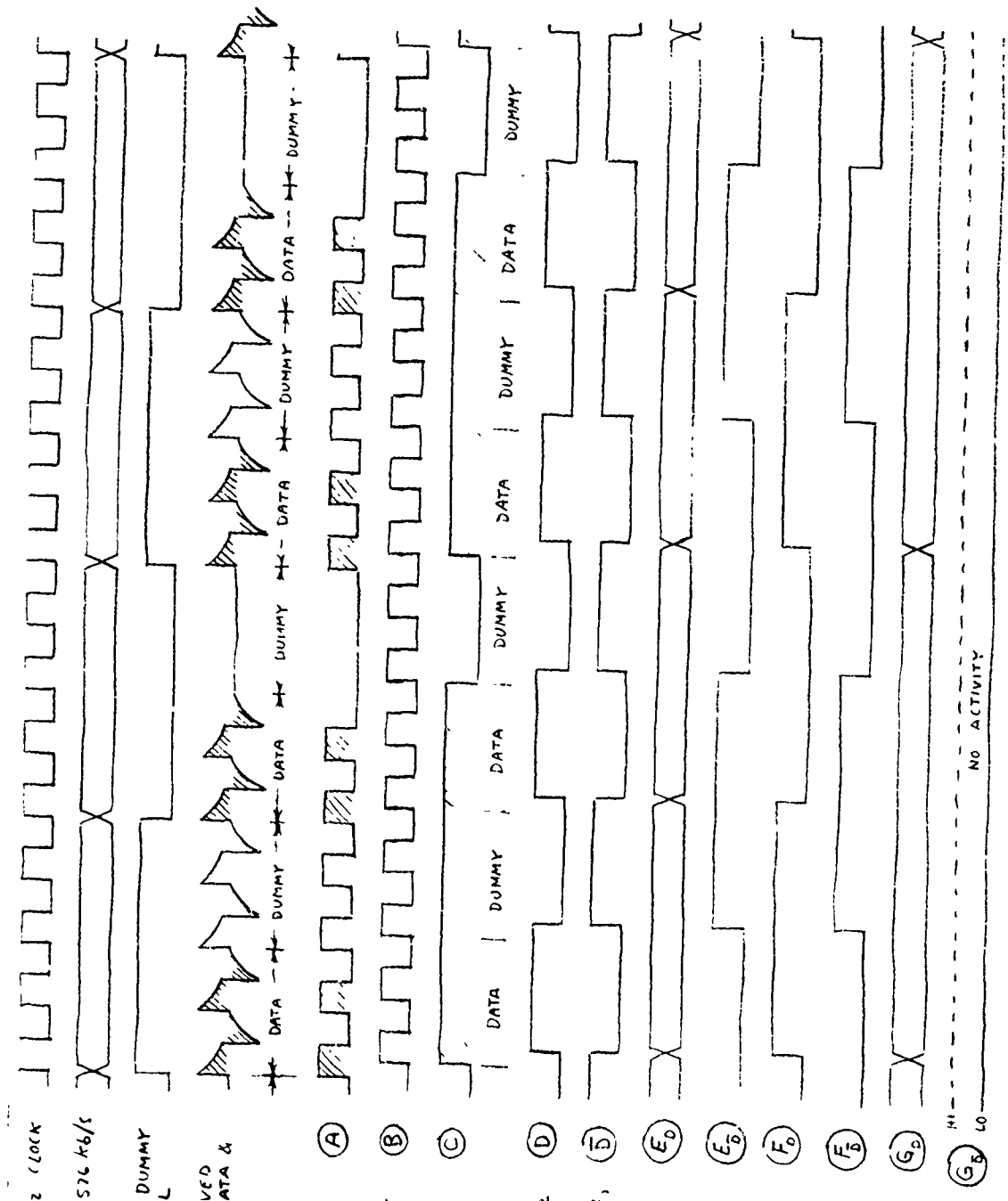


Figure 10-14. Dummy Pattern Delete Circuit Timing Diagram

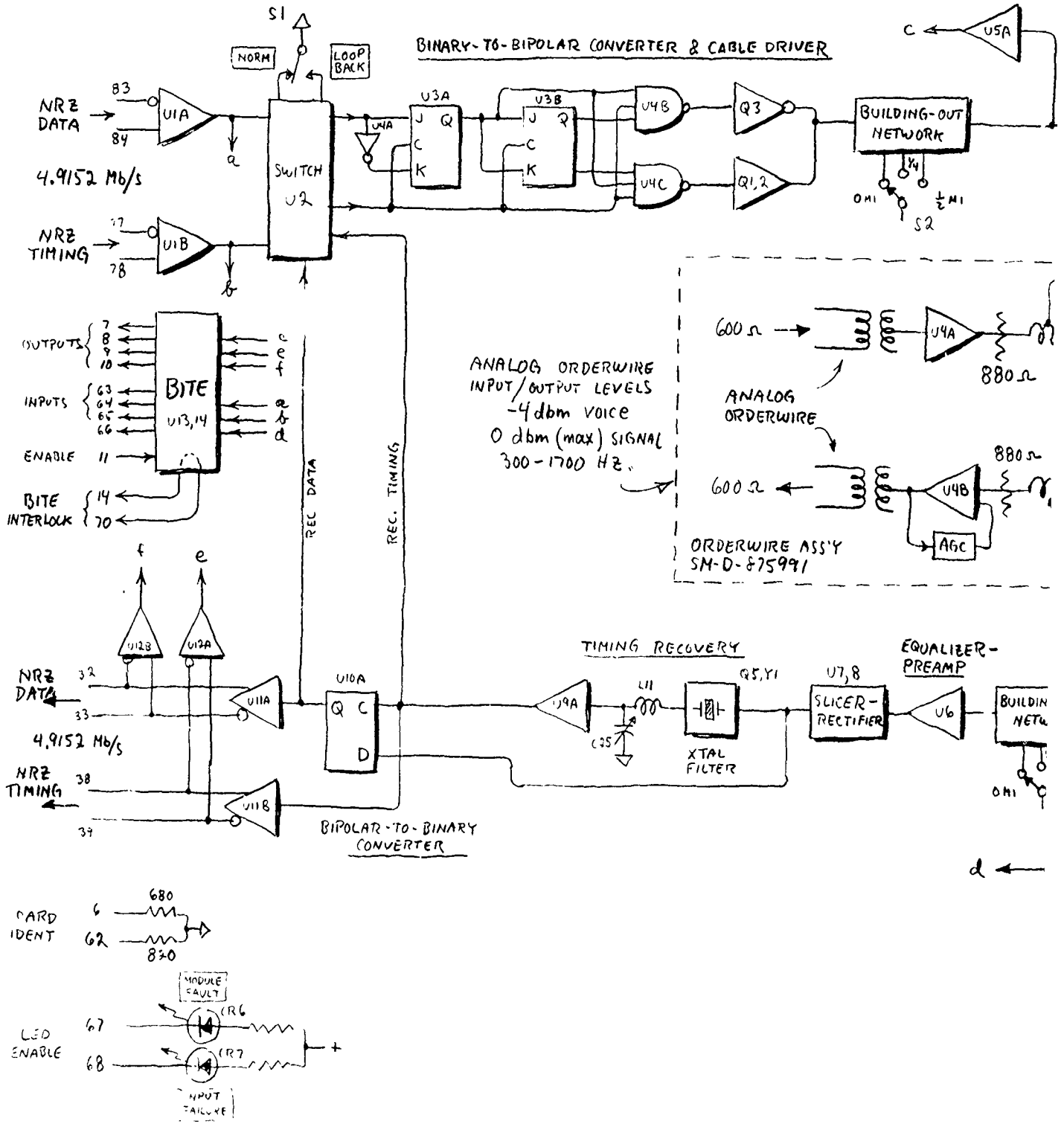
recovers data. If the polarity of D is not correct to recover data, U22B will be clocked on alternate dummy pattern bits. The dummy pattern is a 288 kHz square wave, so alternate bits will be either all ones or all zeros and no activity will appear at G and hence at H. One-shot U24 will re-set itself causing its $\overline{Q}$ output to go high. This positive transition will toggle U24A to the opposite state which causes U21A to reverse the polarity of (D), making U20B select data instead of dummy. At the same time the 288 kHz output of U22A will shift 90^{o} to clock U22B on alternate data bits instead of dummy, causing activity at (H) which sets the $\overline{Q}$ output of U24 low. This high to low transition has no effect on U25A, so the level at pin 10 of U21A does not change, leaving the circuit in the proper state to continue recovering data.

The purpose of U23 is to prevent the circuit from locking itself in the dummy recovery mode in the absence of data (data all ones or all zeros). If the period of all ones or all zeros is longer than the holding time of one-shot U24, U24 will change state causing (J) to go high which enables Gate U23 to pass (F) to U21B so that activity will appear at (H) and U24 $\overline{Q}$ output will switch low again. If data inactivity persists, the circuit will cycle at a rate determined by the holding time of U24 until data is restored.

10.3.4 THE BIPOLAR MODEM

Referring to Figure 10-15, balanced NRZ data and timing are converted to TTL levels in dual line receiver U1. Both signals pass through logic switch U2 to a Binary-to-Bipolar Cable Driver circuit U3, U4, Q1, Q2, and Q3. A cable building-out network (Figure 10-16) that can be set with switch S2 to simulate 0, 1/4 or 1/2 mile of cable is used to obtain a fixed signal level and waveshape at the remote TD-976 multiplexer (or TD-982 restorer) through 1/4 or 1/2 mile of cable. The zero miles building-out network permits operation when the TD-976 is connected locally through very short cables.

Received Bipolar signals pass through an identical building-out network to an equalizer/preamplifier U6 that compensates for the distortion of waveshape caused by the cable, and increases the signal to the level required by the slicer-rectifier U7,8 (see Figure 10-17). The output of the slicer-rectifier drives a timing recovery circuit and a Bipolar-to-Binary converter U10A. Timing recovery is accomplished with a narrowband crystal filter in the same manner as in the Dipulse Modem. The timing output of U9A and rectified bipolar output of U8 drive D flip-flop U10A which converts the bipolar signal to binary at TTL


BINARY-TO-BIPOLAR CONVERTER & CABLE DRIVER
S1
NORM
LOOP BACK
NRZ DATA
83
84
U1A
4.9152 Mb/s
NRZ TIMING
77
78
U1B
SWITCH U2
U4A
U3A
U3B
U4B
U4C
Q3
Q1,2
BUILDING-OUT NETWORK
U5A
C
OMI
±MI
S2
OUTPUTS
INPUTS
ENABLE
BITE INTERLOCK
BITE U13,14
REC DATA
REC. TIMING
ANALOG ORDERWIRE INPUT/OUTPUT LEVELS
-4 dbm VOICE
0 dbm (max) SIGNAL
300-1700 Hz.
600 Ω
880 Ω
U4A
U4B
AGC
ANALOG ORDERWIRE
ORDERWIRE ASS'Y SM-D-875991
U12B
U12A
U11A
U11B
U10A
NRZ DATA
4.9152 Mb/s
NRZ TIMING
BIPOLAR-TO-BINARY CONVERTER
TIMING RECOVERY
U9A
L11
C25
Q5,Y1
XTAL FILTER
U7,8
SLICER-RECTIFIER
EQUALIZER-PREAMP
U6
CARD IDENT
680
820
MODULE FAULT
CR6
CR7
INPUT FAILURE
LED ENABLE
+

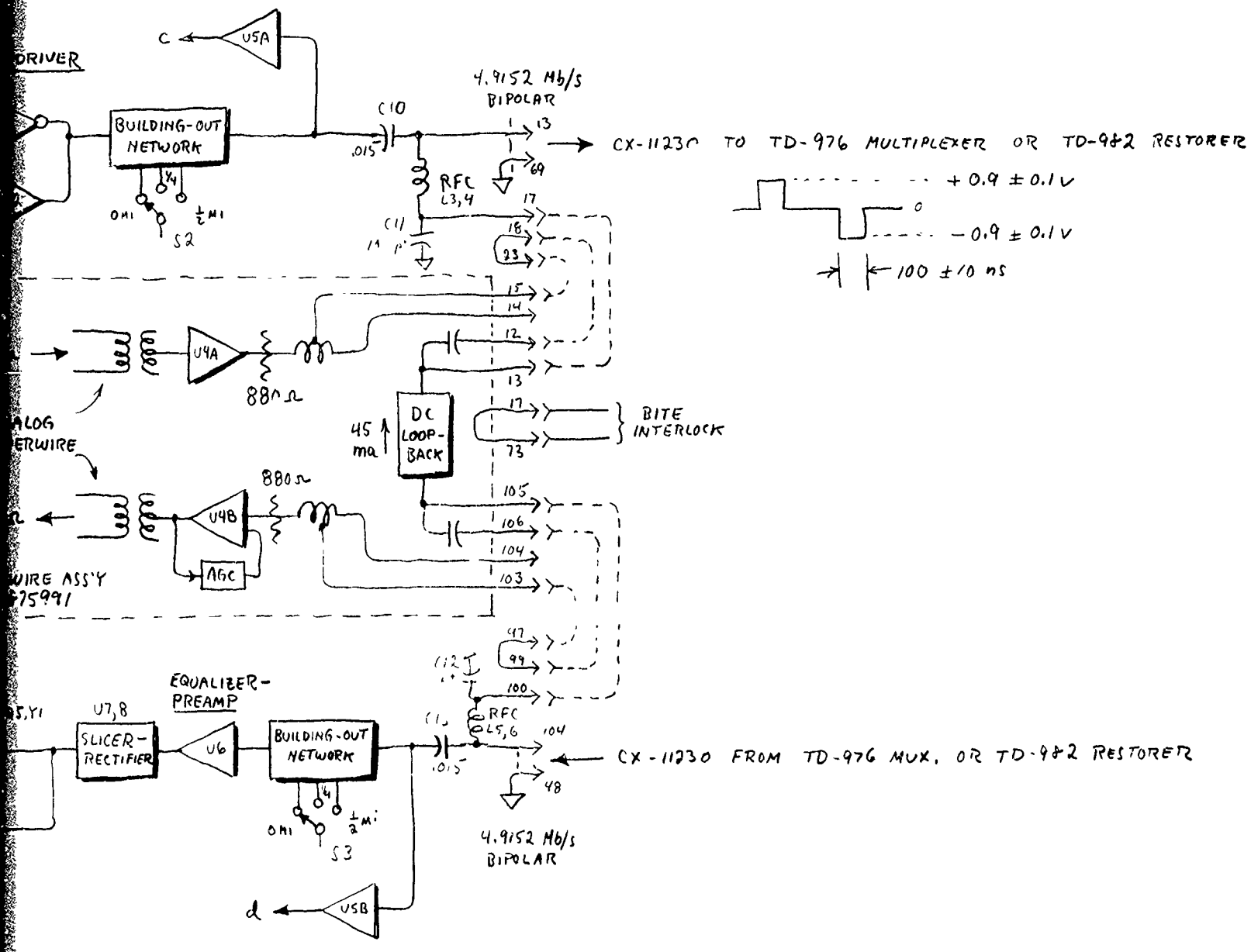


Figure 10-15. Bipolar Modem Block Diagram

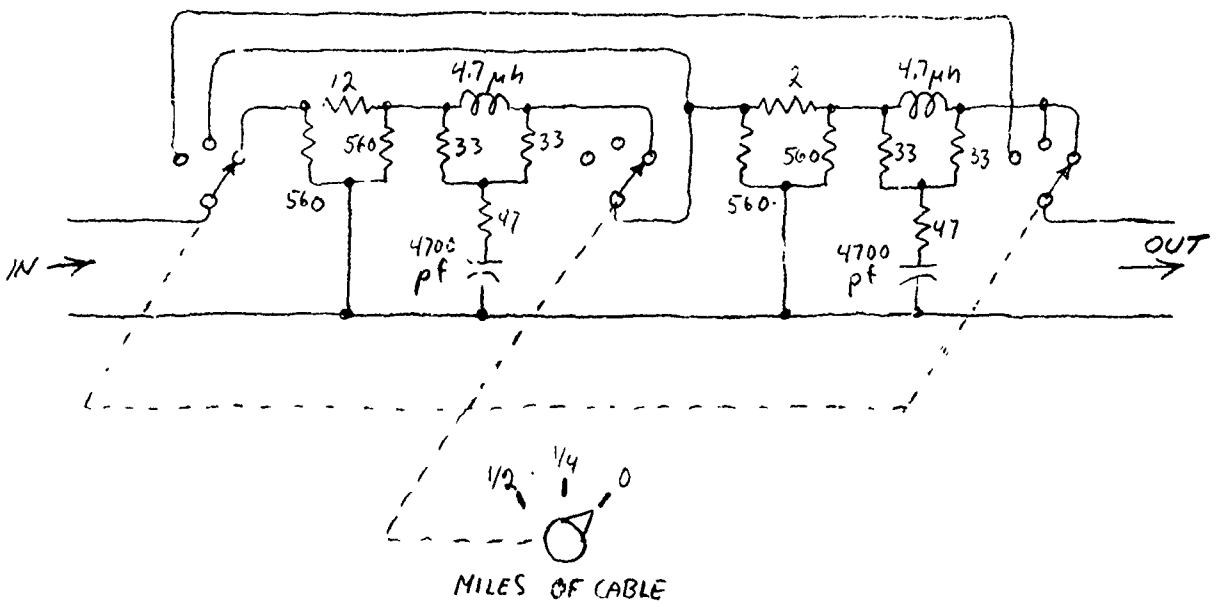


Figure 10-16. Building-Out Network for Bipolar Modem (Transmit and Receive)

levels. Dual line driver U11 provides balanced NRZ data and timing to the shelter equipment. The received data and timing can be looped back to the originating TD-976 equipment through logic switch U2 by placing control switch S1 in the loop-back position.

BITE and the analog orderwire are handled in the same manner as in the Dipulse modem.

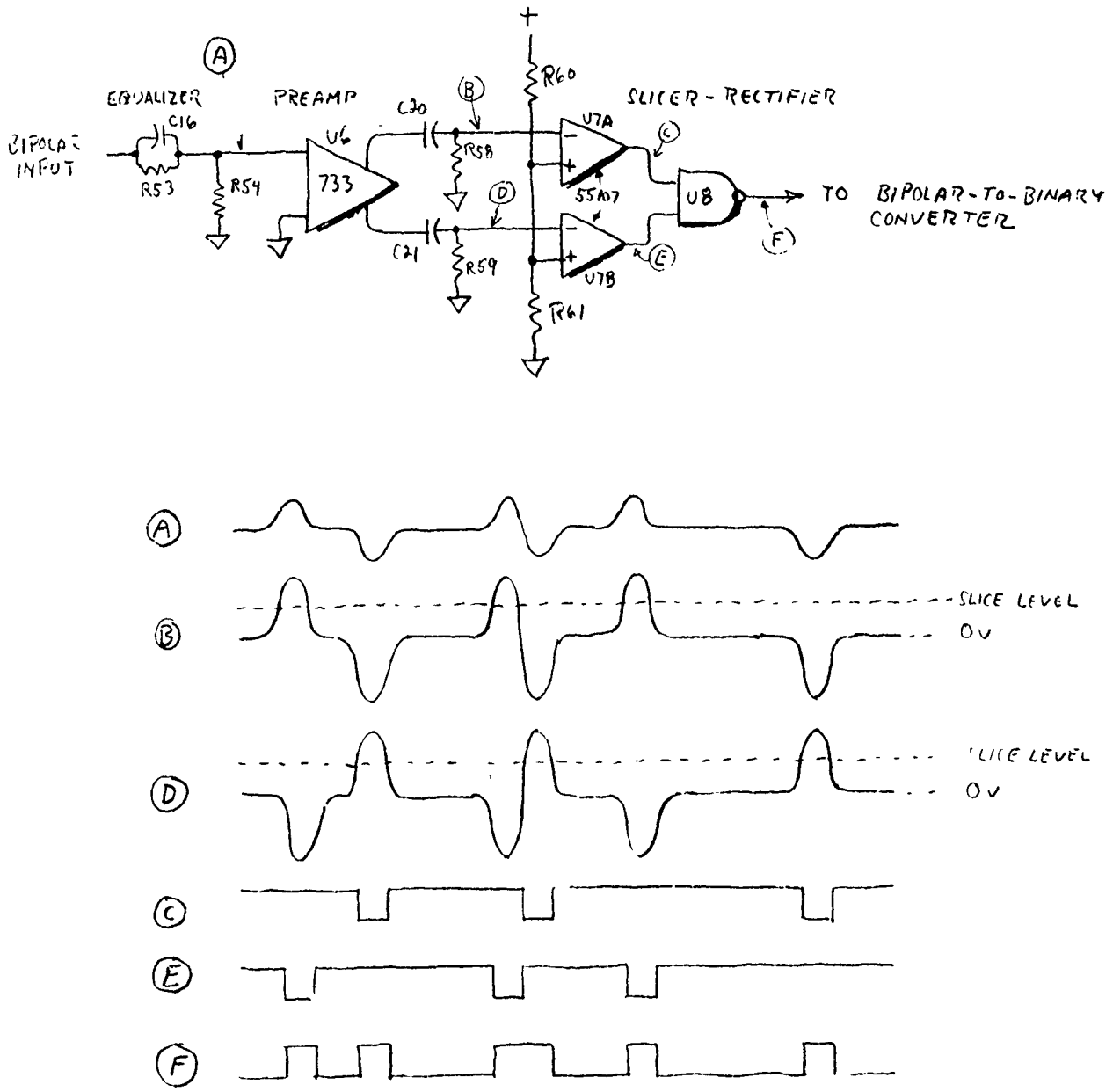


Figure 10-17. Bipolar Receiver Preamp and Slicer-Rectifier

10.3.5 THE CABLE ORDERWIRE MODULE

The block diagram of the Orderwire module is shown on the diagrams of the Dipulse and Bipolar Modems, Figures 10-9 and 10-15. This unit provides a balanced 600 ohm 4-wire interface to the shelter voice circuits. On the cable side it provides half loading inductances and 880 ohm resistive loads to properly terminate each cable. High voltage blocking capacitors separate the voice signals from the dc cable supply voltage, and a DC Loop-Back circuit (Figure 10-18) passes the cable supply current while presenting a high impedance to the voice and signaling frequencies. A BITE interlock jumper completes the output BITE circuit on the companion modem so that a missing orderwire card will cause an alarm. The gain of the transmit amplifier is fixed to provide the required drive level at the cable input to satisfy both the TD-754 and the TD-976 multiplexers. The receive amplifier employs automatic gain control that gives a fixed output test tone level of -4 dBm for an input voltage range from 16 volts to 0.08 volt RMS.

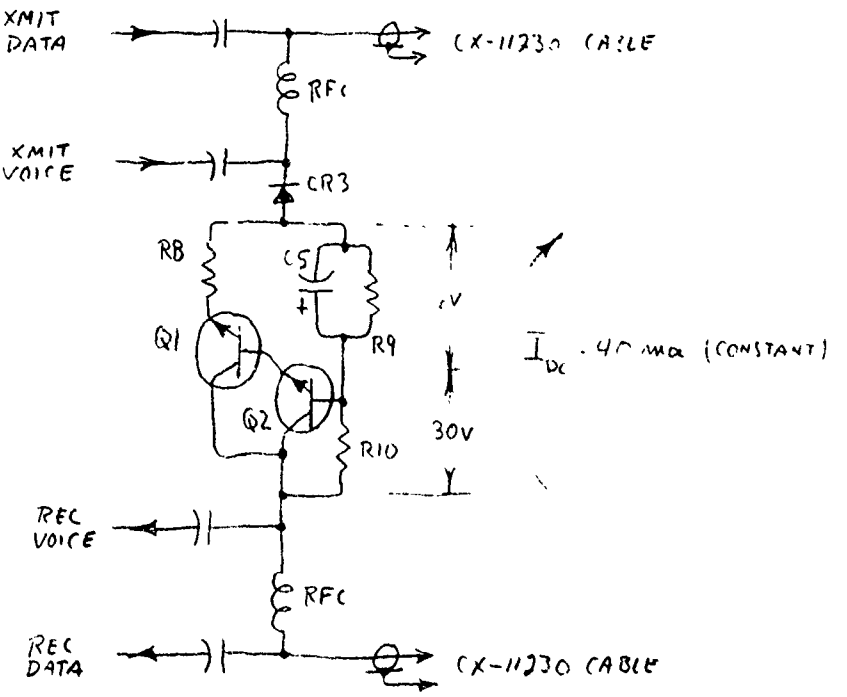


Figure 10-18. Cable Current Loop-Back

10.3.6 BITE (BUILT-IN TEST EQUIPMENT)

Various points within each GM are monitored for proper operation, such as activity detection on inputs and outputs, phase locked loop in-lock monitors, etc. These points enable fault isolation to a single PC board. An LED indication is provided on each panel for fault isolation.

10.3.7 EMI

The equipment side signal lines into and out of this device are balanced. This interface relies on balance as its primary means of EMI suppression. The external cables connected here are shielded twisted pairs, such as RG-108, so a high degree of suppression can be maintained. There is a wide range of bit rates on these lines, from 72 to 4195.2 Kb/s, and waveshaping suitable for the highest rate would be ineffective at the lowest. There are auxiliary signals for orderwire and telemetry that are also balanced. These will use waveshaping and be carried externally in multipair cable. The full duplex telemetry channel has a rate of 2 kb/s. The digital orderwire has a rate of 16 kb/s. There is a station clock line which will be balanced for tempest reasons and a floating alarm line which

appears as a balanced line. All the above equipment side signals are digital and have the basic $(\sin x/x)^2$ spectral shape. There is also an analog orderwire of nominal bandwidth of 4 kHz and a balanced four wire line with a test tone level of -4 dBm. The diphase signal has a $(\sin^{2=}X/\bar{X})^2$ shape. The PCM signal is $(\sin x/x)^2$, the dipulse is $(\sin x/x,^2$ through a high pass filter. The bipolar signal is $(\sin x/x)^2$ (1-cos 4x).

The power line has a single EMI filter specified for dc, 50 Hz, and 400 Hz making it larger than a conventional filter, but smaller than two filters. The power line filter has an integral power line connector which gives far better filter performance as installed on the unit and saves additional space.

10.3.8 HFE

The Group Modem design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by ..-B1-2202-0013 performance specification.

The initial setup controls required to configure the equipment to system requirements are incorporated onto the exposed edge of the PCB's. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification. This unit has rear mounted connectors which require sequential connect/disconnect during installation/removal due to size and space limitations. The GM front and rear panel layouts are shown in Figure 10-19 and 10-20.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472.

10.3.9 RELIABILITY DESIGN

The Group Modem case has a specified MTBF of 6000 hours. Up to six Group Modems can be installed in the Group Modem case, in any desired combination of the three types of Group Modems: Conditioned Diphase, Dipulse, Bipolar. Table 10-3 shows the predicted failure rate for each type of Group Modem, and the worst combination Group Modem case.

The failure rate data source used in the reliability prediction was MIL-HDBK-217B, dated 20 September 1974. The environment was ground, fixed; the outside ambient temperature was 40°C. The IC junction temperature (Tj) was calculated based on the power dissipation. The quality level for IC's was B-1, i.e.: MIL-STD-883, Method 5004, Class B.

TABLE 10-3

GM RELIABILITY

	$\lambda \times 10^{-6}$	MTBF
Diphase Group Modem	59.3	16,872
Dipulse Group Modem	54.4	18,379
Bipolar Group Modem	52.1	19,179
GM (worst combination)	150.3	6,655

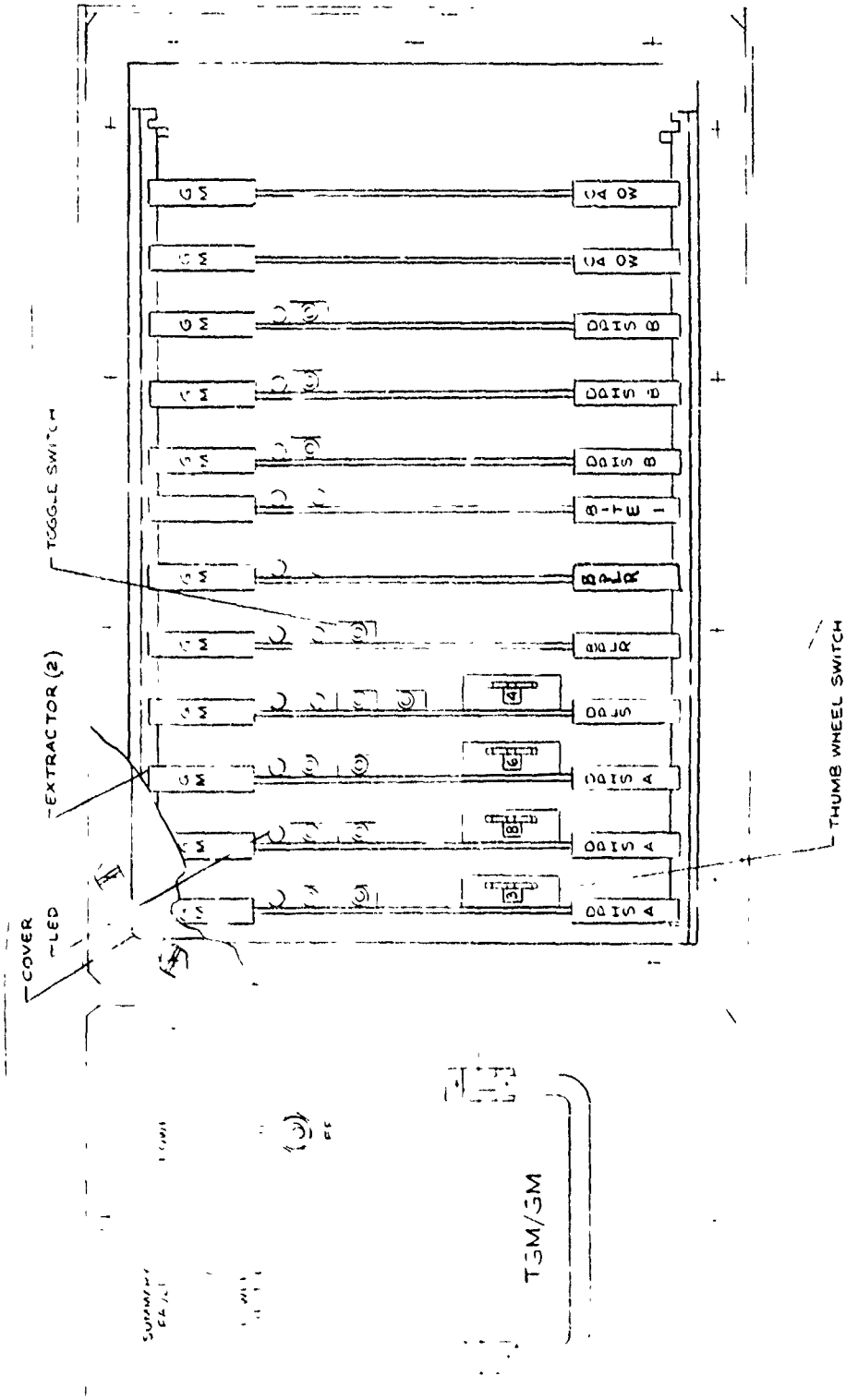


Figure 10-19. GM Front Panel Layout

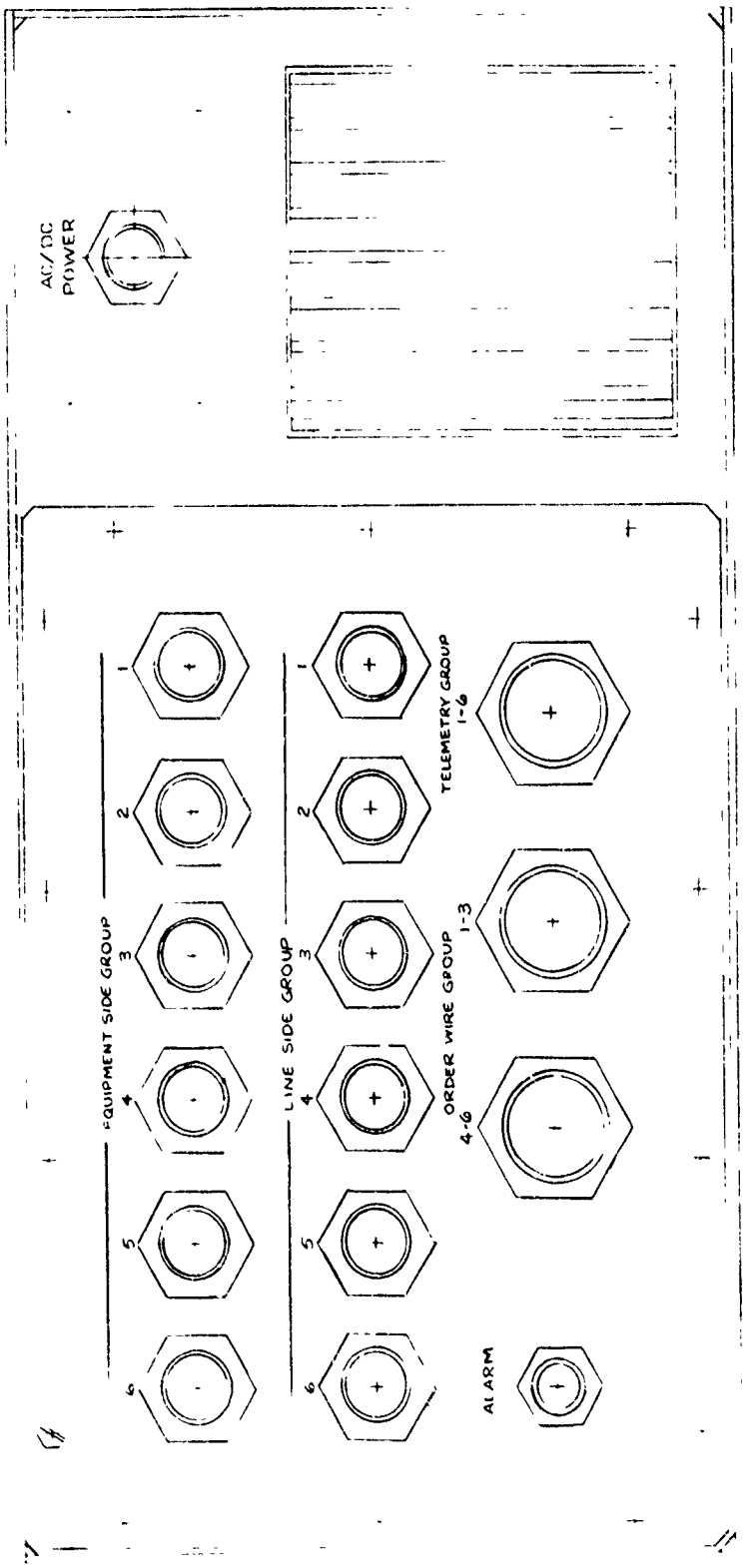


Figure 10-20. GM Rear Panel Layout

SECTION 11

CDM

11.1 DESIGN GOALS AND REQUIREMENTS

The CDM design approach outlined in paragraphs 11.2 and 11.3 meets all the system performance goals of the DGM Specification TT-B1-2202-0013. As discussed in paragraph 2.2, the key to meeting the system function requirements is time division multiplexing of the 2.0 kb/s telemetry and 16 kb/s VINSON signals.

This approach offers the least design risk and is the only feasible approach capable of meeting the full 64 km range requirements of the low speed system. Specific functional requirements are listed in Table 11-1.

On the equipment side, the CDM can interface directly with an LGM, TED, TCM, another CDM, MGM, Group Modem, or radio equipment. On the line side, the CDM interfaces through CX-11230 with another CDM for distances less than the PR spacing or with the appropriate PR for greater distances. Restorer power is provided on the same cable.

Other required interfaces to the CDM are: (1) external ac and dc power; (2) external clock; (3) maintenance orderwire; (4) VINSON; and (5) telemetry at 2 kb/s and BLACK station clock.

11.2 CDM DESIGN APPROACH

Figure 11-1 illustrates the formats of both CDM units. Circuit block diagrams are shown in Figures 11-2 through 11-5. Both units are identical on a functional basis, comprising six printed circuit cards and plug-in power supply. Three panels, orderwire transmit, orderwire receive, telemetry, and the power supply are common. Other features are:

a. Synchronous transmission of all input group rates

b. Digital transmission of 16 VINSON data and 2.0 kb/s telemetry, providing full 64 km range

TABLE 11-1

CDM FUNCTIONAL REQUIREMENTS

Group Rates	LS 0.072 to 2.048 Mb/s HS 4.096 to 18.720 Mb/s
Equipment Side Interface	Balanced NRZ and timing
Line Side Interface	Unbalanced conditioned diphase, 2 Vpp into 62 ohms LS rate 2.304 mb/s, HS rate 19.200 mb/s LS range 0-64 km CX 11230 (1.6 km repeater spacing) HS range 0-8 km CX 11230 (0.4 km repeater spacing) Power Feed - constant current
Orderwire	16 kb/s digital (VINSON)
BITE	Locates equipment faults to single replaceable subassembly
Telemetry Transmission	2 kb/s telemetry subchannel, balanced NRZ and timing
Black Station Clock	72 to 2048 kHz (LS CDM) balanced 4.096 and 4.608 MHz (HS CDM) balanced
Timing Options	From internal received group. From related clock. Timing maintenance for 0.5 seconds
MTBF	6000 hours
Power	115 Vac ±10%, 50 to 400 Hz or 22 to 32 Vdc, 150 Watts maximum
Size	8-1/2 H x 12 D x 19-inch W, Rack Mount
Weight	15 kg maximum

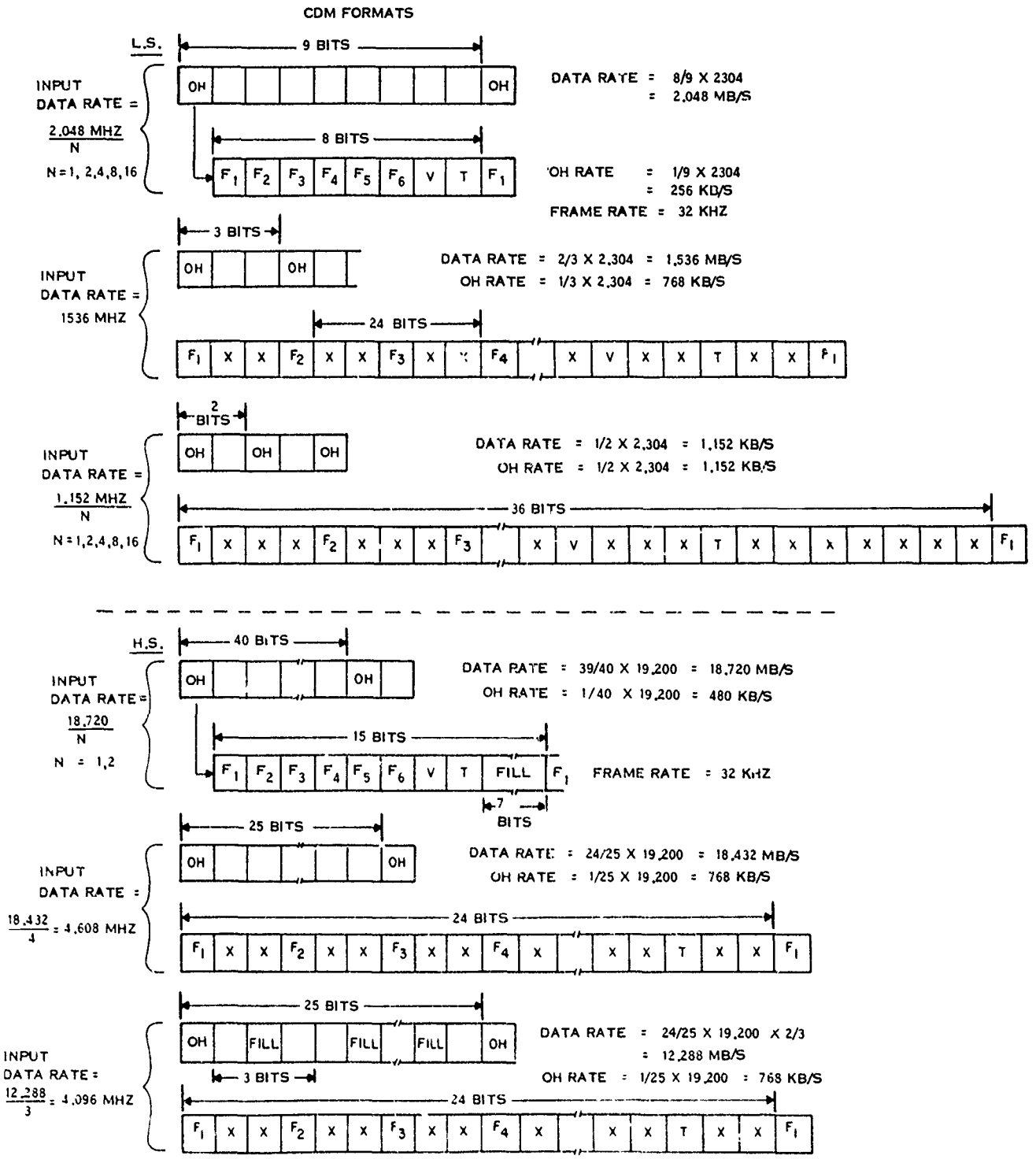


Figure 11-1. CDM Block Diagram and Formats

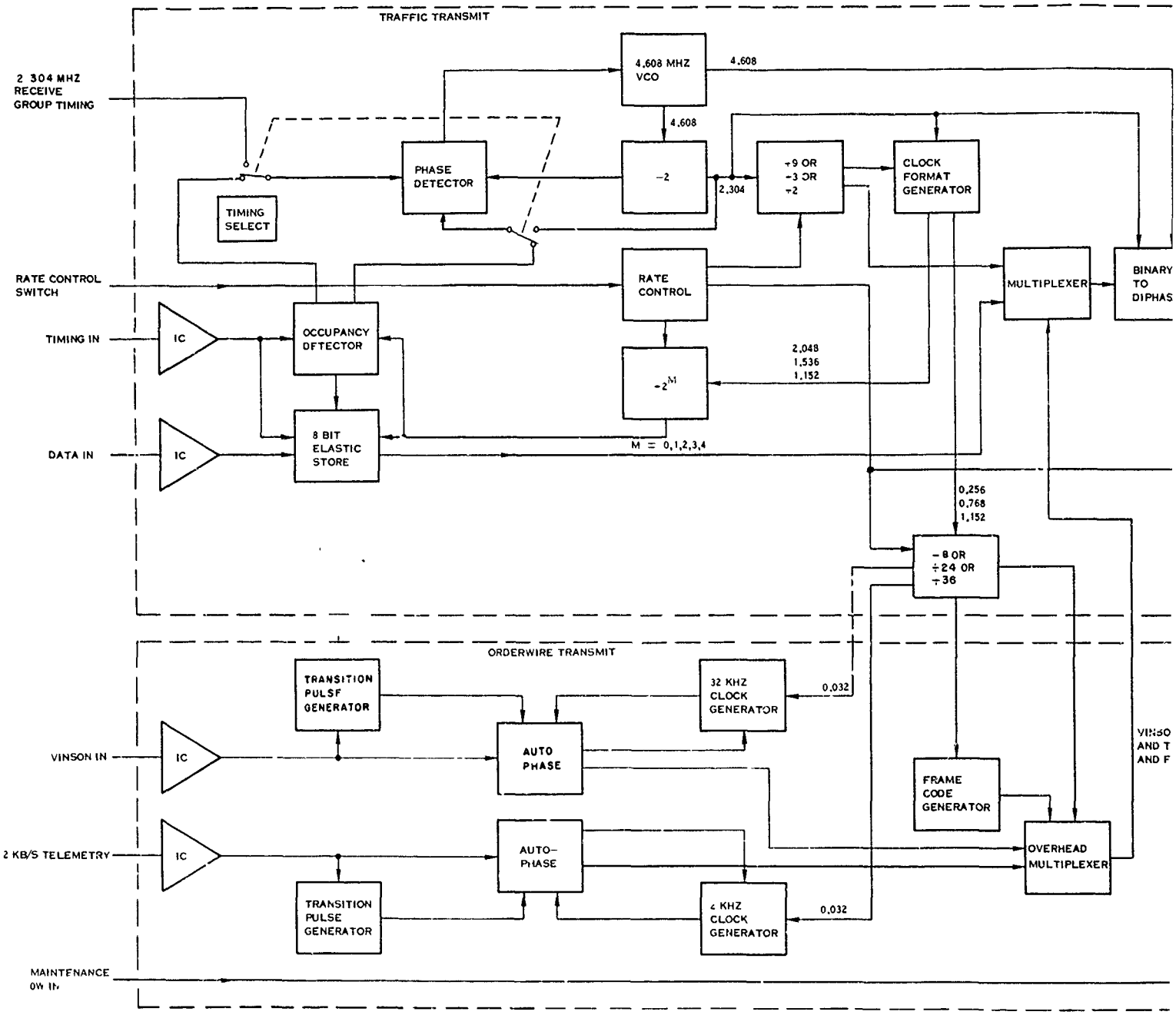

TRAFFIC TRANSMIT
2 304 MHZ RECEIVE GROUP TIMING
4,608 MHZ VCO
4,608
4,608
PHASE DETECTOR
-2
2,304
÷9 OR ÷3 OR ÷2
CLOCK FORMAT GENERATOR
TIMING SELECT
RATE CONTROL SWITCH
RATE CONTROL
MULTIPLEXER
BINARY TO DIPHAS
TIMING IN
IC
OCCUPANCY DETECTOR
2,048
1,536
1,152
-2^M
DATA IN
IC
8 BIT ELASTIC STORE
M = 0,1,2,3,4
0,256
0,768
1,152
- 8 OR ÷24 OR ÷36
ORDERWIRE TRANSMIT
TRANSITION PULSE GENERATOR
32 KHZ CLOCK GENERATOR
0,032
VINSON IN
IC
AUTO PHASE
FRAME CODE GENERATOR
VINSO AND T AND F
2 KB/S TELEMETRY
IC
AUTO-PHASE
OVERHEAD MULTIPLEXER
TRANSITION PULSE GENERATOR
4 KHZ CLOCK GENERATOR
0,032
MAINTENANCE OW IN

Figure 1

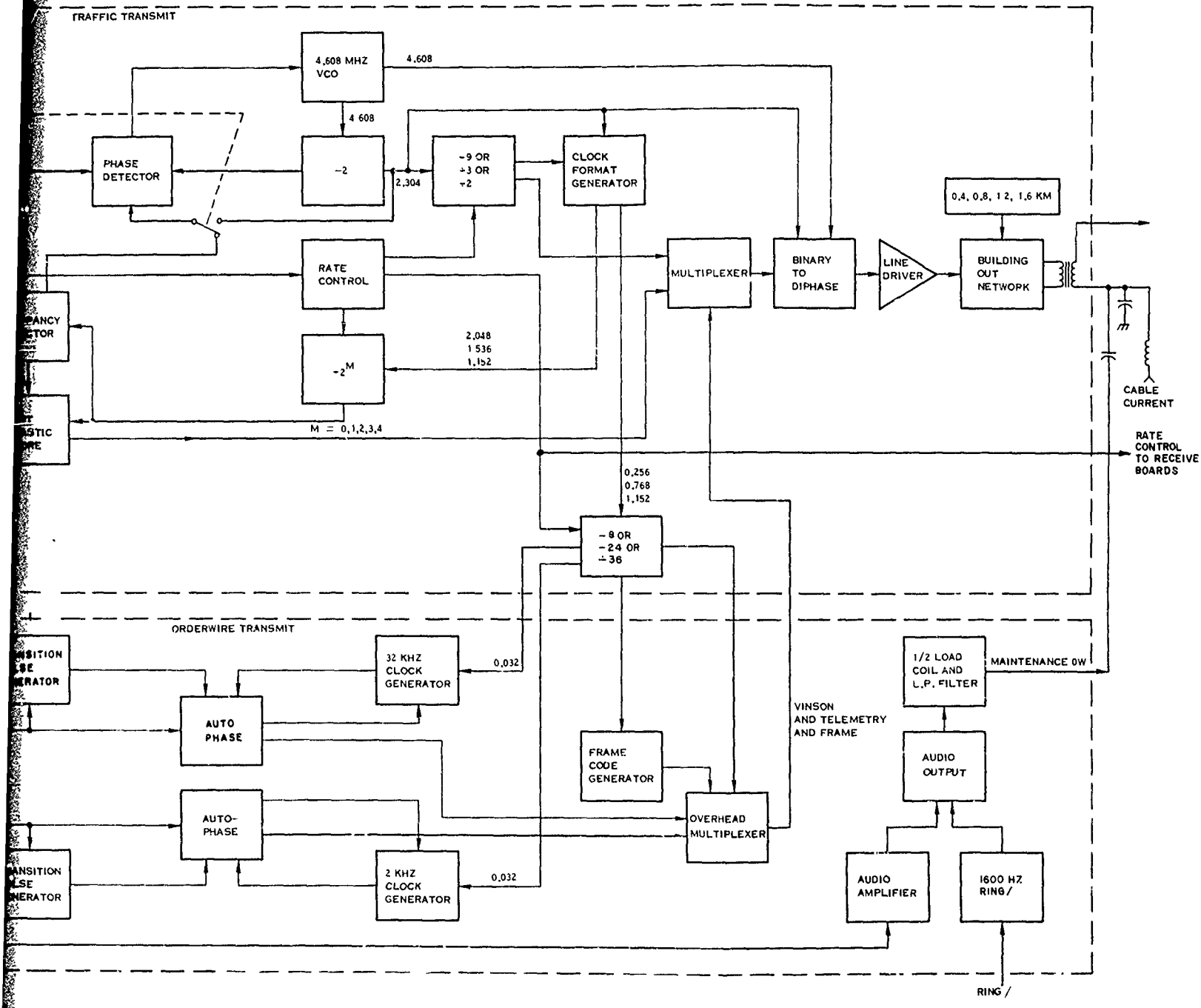
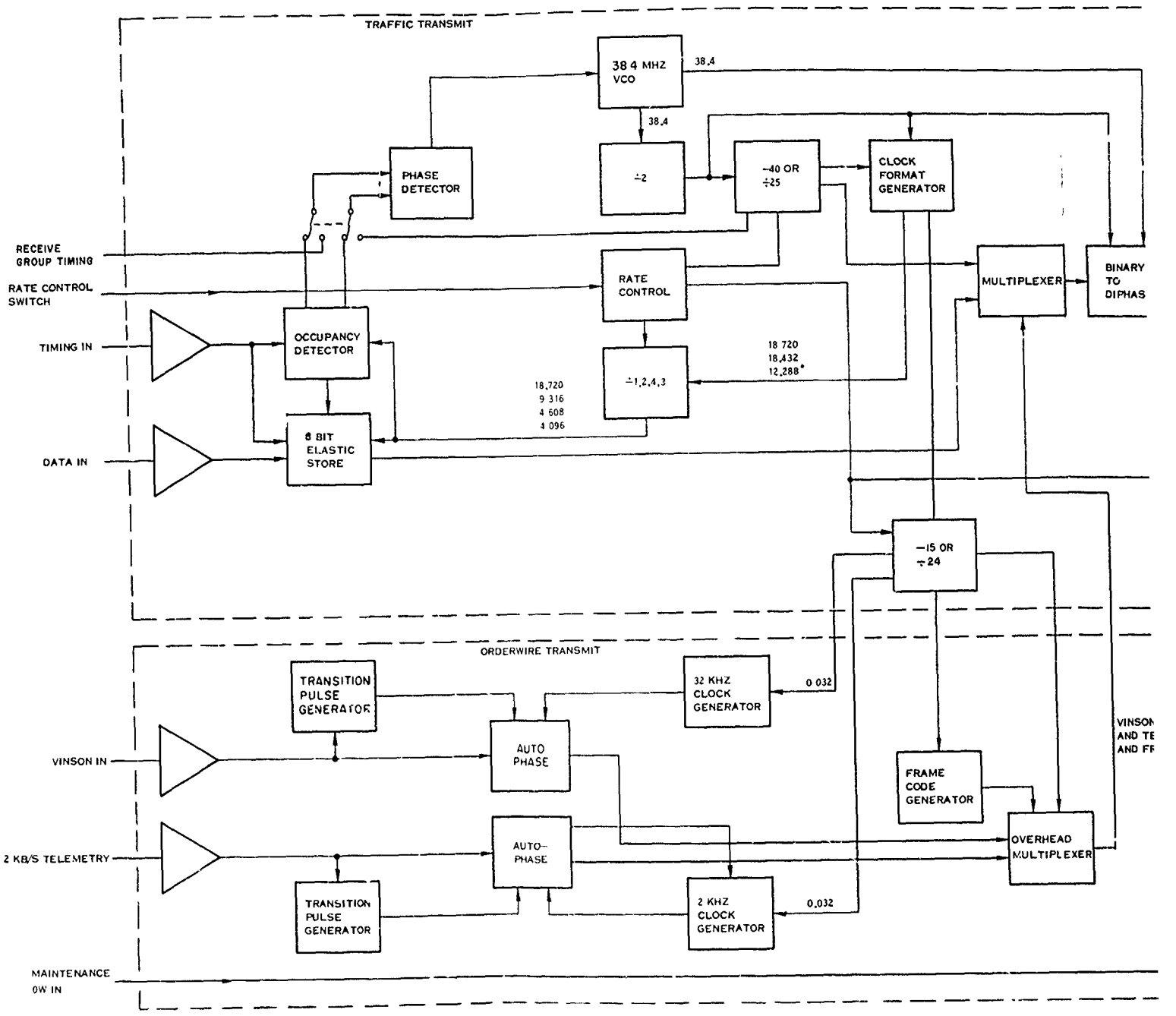


Figure 11-2. LS CDM Transmit Circuits


TRAFFIC TRANSMIT
38 4 MHZ VCO
38,4
38,4
÷2
÷40 OR ÷25
CLOCK FORMAT GENERATOR
PHASE DETECTOR
RECEIVE GROUP TIMING
RATE CONTROL SWITCH
RATE CONTROL
MULTIPLEXER
BINARY TO DIPHAS
TIMING IN
OCCUPANCY DETECTOR
18 720
18,432
12,288*
÷1,2,4,3
18,720
9 316
4 608
4 096
DATA IN
8 BIT ELASTIC STORE
÷15 OR ÷24
ORDERWIRE TRANSMIT
TRANSITION PULSE GENERATOR
32 KHZ CLOCK GENERATOR
0 032
VINSON IN
AUTO PHASE
FRAME CODE GENERATOR
VINSON AND TE AND FR
2 KB/S TELEMETRY
AUTO-PHASE
OVERHEAD MULTIPLEXER
TRANSITION PULSE GENERATOR
2 KHZ CLOCK GENERATOR
0,032
MAINTENANCE OW IN

Figure

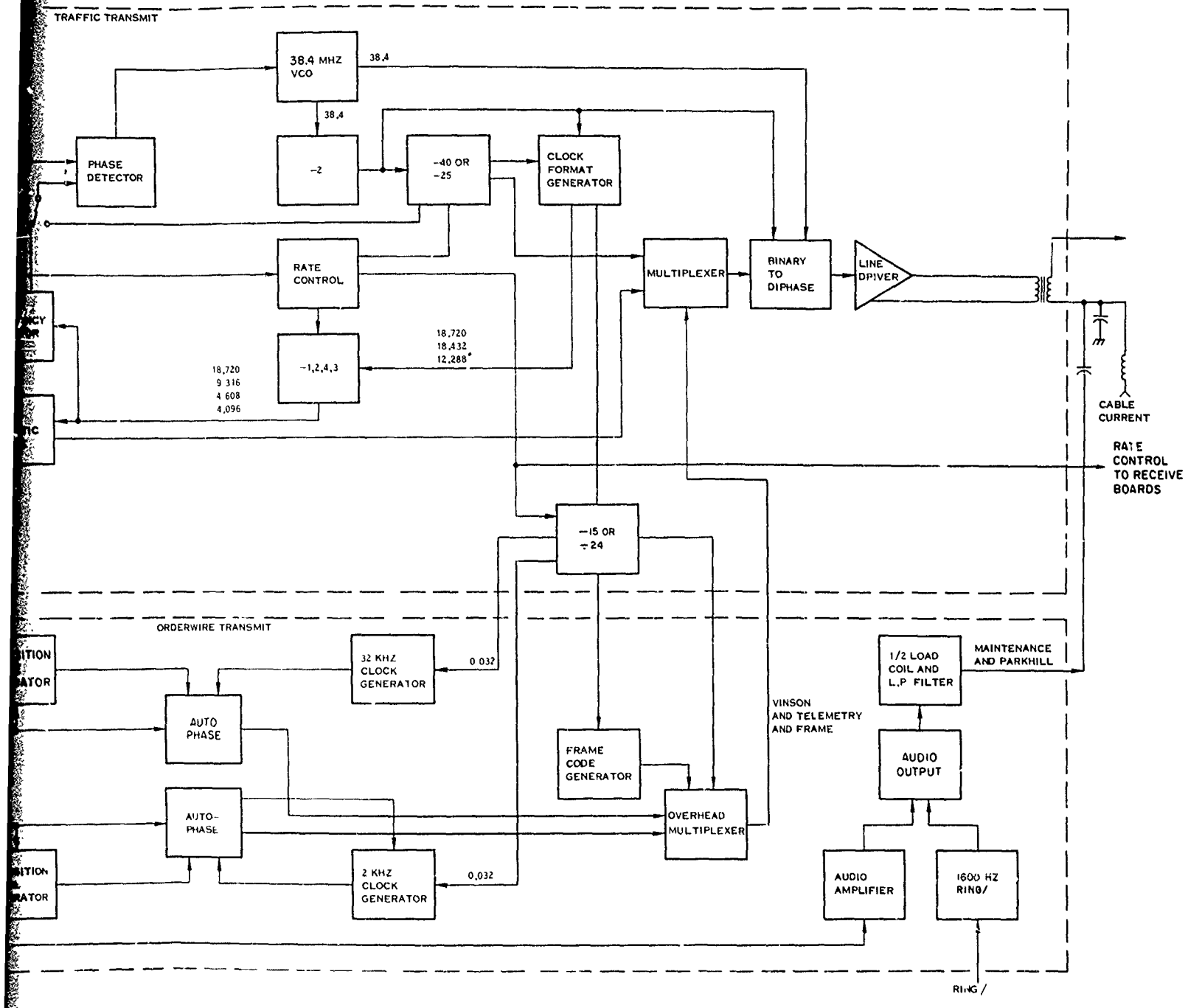
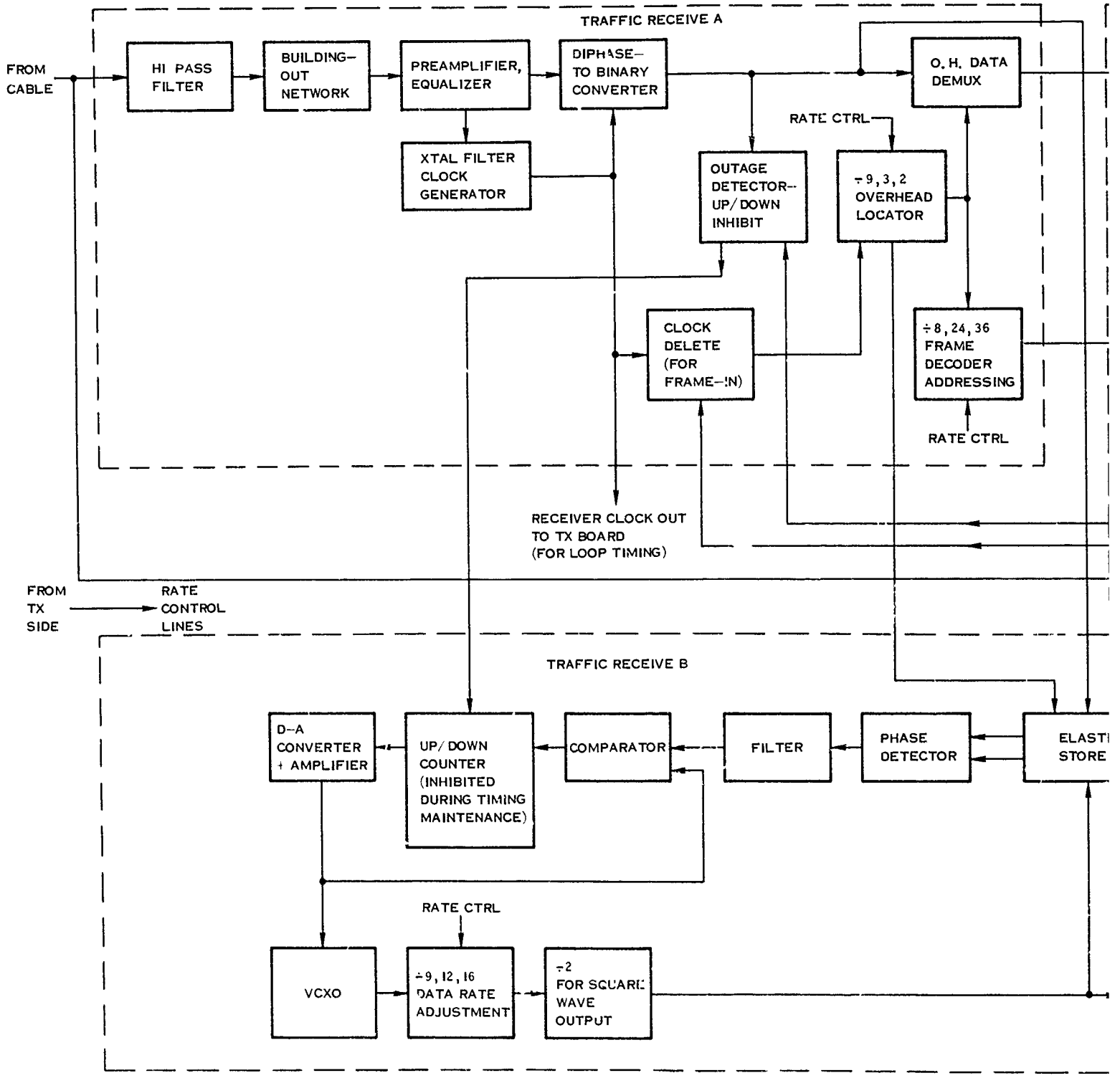


Figure 11-3. HS CDM Transmit Circuits


TRAFFIC RECEIVE A
FROM CABLE
HI PASS FILTER
BUILDING-OUT NETWORK
PREAMPLIFIER, EQUALIZER
DIPHASE-TO BINARY CONVERTER
O.H. DATA DEMUX
RATE CTRL
XTAL FILTER CLOCK GENERATOR
OUTAGE DETECTOR-UP/DOWN INHIBIT
÷9,3,2 OVERHEAD LOCATOR
CLOCK DELETE (FOR FRAME-IN)
÷8,24,36 FRAME DECODER ADDRESSING
RATE CTRL
RECEIVER CLOCK OUT TO TX BOARD (FOR LOOP TIMING)
FROM TX SIDE
RATE CONTROL LINES
TRAFFIC RECEIVE B
D-A CONVERTER + AMPLIFIER
UP/DOWN COUNTER (INHIBITED DURING TIMING MAINTENANCE)
COMPARATOR
FILTER
PHASE DETECTOR
ELASTI STORE
RATE CTRL
VCXO
÷9,12,16 DATA RATE ADJUSTMENT
÷2 FOR SQUARE WAVE OUTPUT

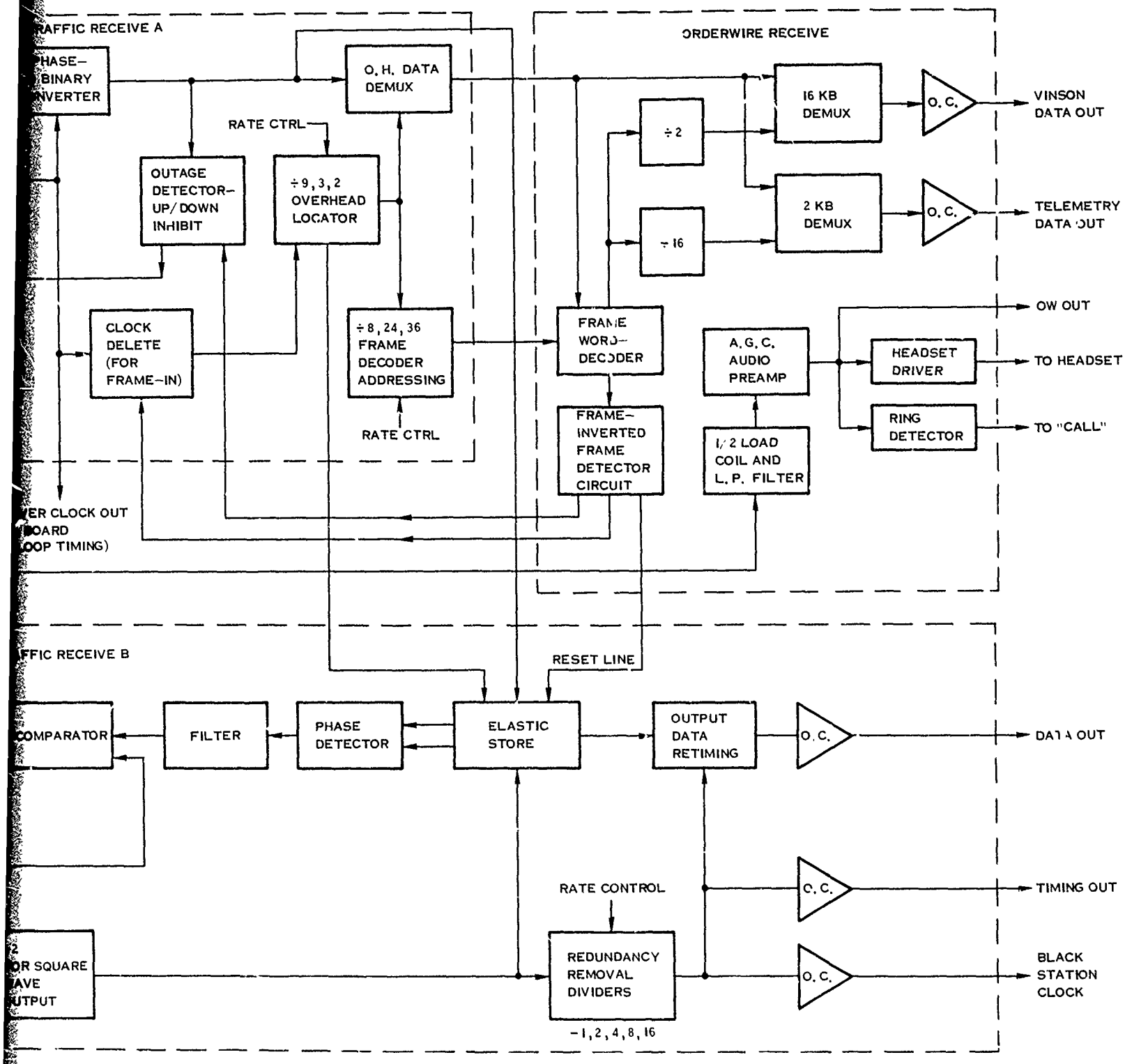
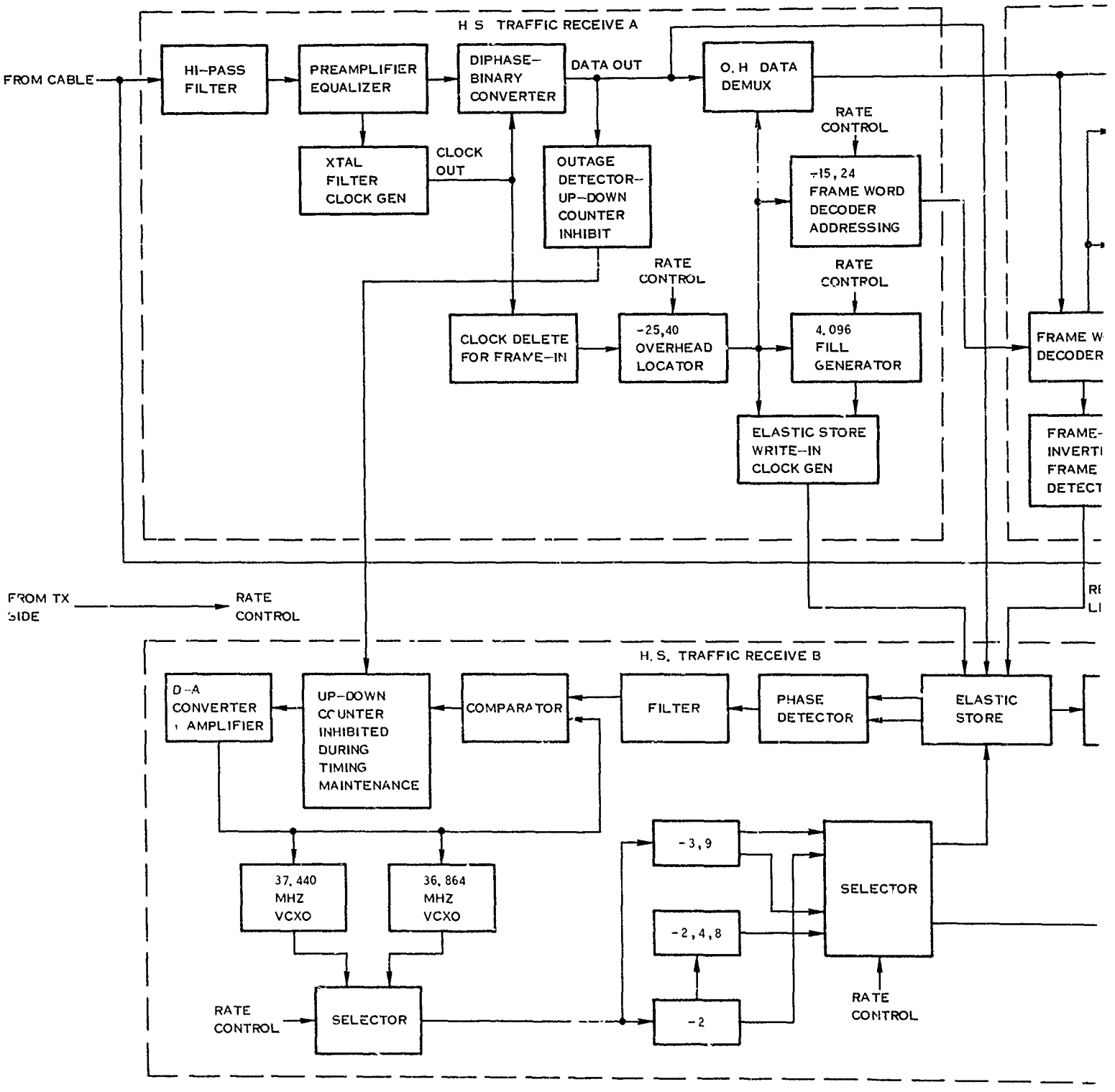


Figure 11-4. LS CDM Receive Circuits


H S TRAFFIC RECEIVE A
FROM CABLE
HI-PASS FILTER
PREAMPLIFIER EQUALIZER
DIPHASE-BINARY CONVERTER
DATA OUT
O. H DATA DEMUX
RATE CONTROL
XTAL FILTER CLOCK GEN
CLOCK OUT
OUTAGE DETECTOR-UP-DOWN COUNTER INHIBIT
+15, 24 FRAME WORD DECODER ADDRESSING
RATE CONTROL
RATE CONTROL
CLOCK DELETE FOR FRAME-IN
-25,40 OVERHEAD LOCATOR
4.096 FILL GENERATOR
FRAME W DECODER
ELASTIC STORE WRITE-IN CLOCK GEN
FRAME- INVERTI FRAME DETECT
FROM TX SIDE
RATE CONTROL
H. S. TRAFFIC RECEIVE B
D-A CONVERTER + AMPLIFIER
UP-DOWN COUNTER INHIBITED DURING TIMING MAINTENANCE
COMPARATOR
FILTER
PHASE DETECTOR
ELASTIC STORE
37, 440 MHZ VCXO
36, 864 MHZ VCXO
-3, 9
-2, 4, 8
-2
SELECTOR
SELECTOR
RATE CONTROL
RATE CONTROL

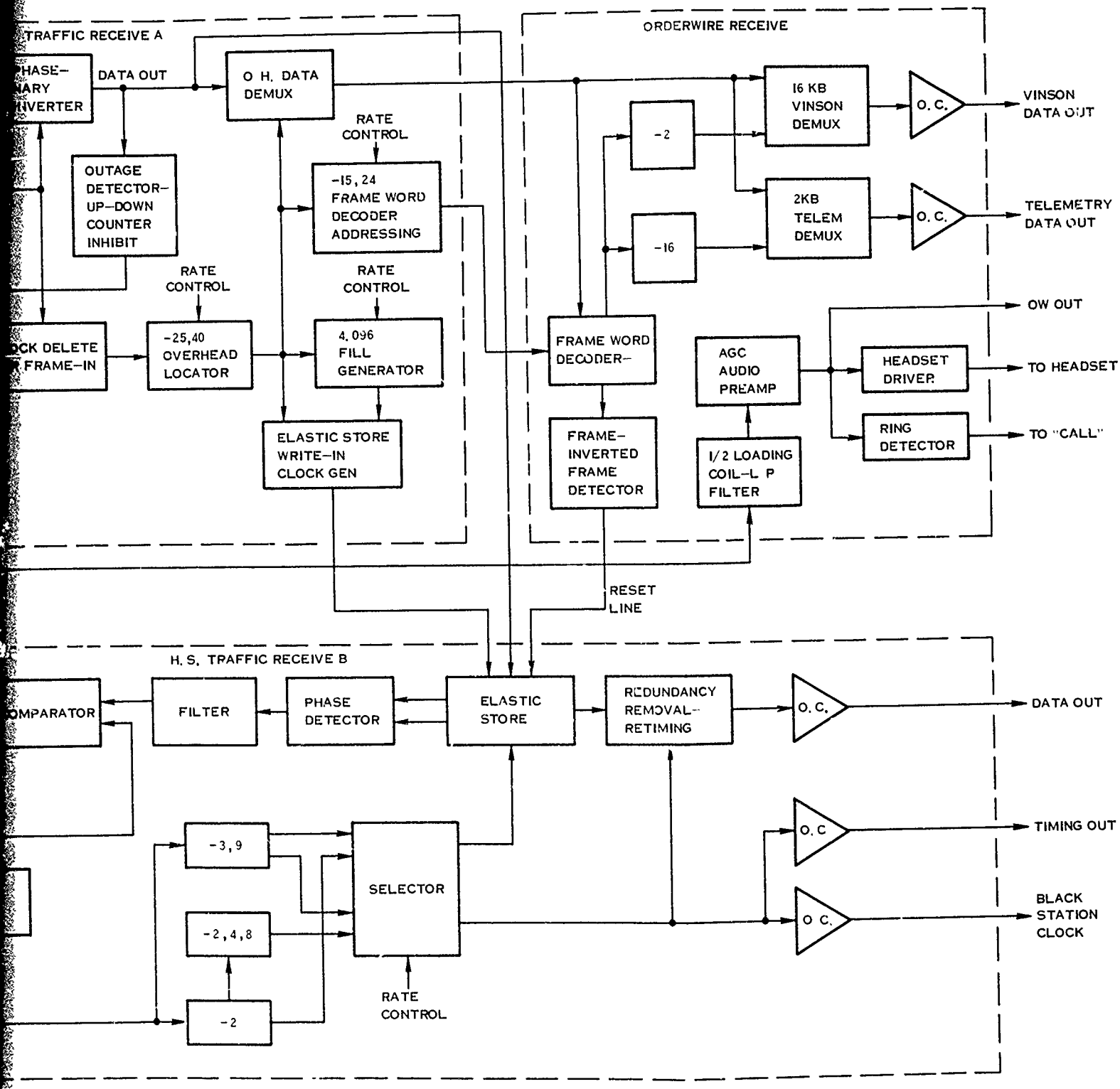


Figure 11-5. HS CDM Receive Circuits

c. All data timings derived from received diphase signals, therefore not dependent on actual data content

d. Digital storage timing maintenance circuit to meet 0.5 second outage requirements

The keys to meeting all system requirements are: (1) the multiplexed wideband transmission of all input digital data signals and (2) a 1.7 kHz maintenance orderwire.

Within the fixed line rate, the ratio of overhead and traffic data is adjusted to provide a data transmission rate harmonically related to the input rate. For the LS CDM specified input group rates, three formats are required. In all formats, the six bit frame code, 16 kb/s VINSON data, 2.0 kb/s telemetry comprise eight bits of the overhead. The overhead frame rate is always 32 kHz.

For repeatered systems, the bandwidth of the LSCDM maintenance orderwire channel is 300 to 1700 Hz. For the HSCDM the bandwidth is 300 to 3400 Hz.

The three HS CDM formats are also similar. However, for the 4.096 mb/s input, additional fill bits are required. The required effective transmission rate is obtained by filling every third bit in the 24 data bit format. Formatting of the overhead provides the six bit frame, two 32 kb/s channels, and the required fill for a 32 kHz frame rate.

The CDM power supply provides the ±12 volt and 5 volt dc voltages required for internal operation. Additionally, a constant current source supplies power for the repeatered cable system. Two output currents are available to allow the use of a common power supply for both cable systems. Facilities are provided for locating faulty PRs in the cable system.

11.2.1 CDM TRANSMIT CIRCUITS

The CDM transmit circuits consist of two PCBs, Traffic Transmit and Orderwire Transmit.

Figure 11-2 illustrates the LS CDM transmit circuit design which implements the formats. The basic 4.608 MHz clock required by the unit is generated with a PLL from either the Elastic Store Occupancy or 2.304 MHz received group timing. The clock format generator provides a 2.304 MHz timing signal with gaps, with effective bit rates of 2.048 or 1.536 or 1.152 MHz. From these three rates a divide-by-2^M counter (M is selected according to the rate) generates a timing signal at a frequency equal to the input rate.

An eight bit elastic store accommodates the gaps in the unit timing and provides an automatic phase function for the input signals. The data read out of the elastic store is then multiplexed with the overhead data. The overhead data is generated from a 0.256, or 0.768 or 1.152 MHz clock (depending on the format) from the clock format generator. A programmable counter provides 32 kHz timing signals used to generate the 16 kHz VINSON and 2.0 kHz clocks used for reading in the input data. Signals from this counter are used to multiplex the overhead data signals.

Although the 16 kb/s VINSON signal is asynchronous, it has been synchronized in an external buffer. Two automatic phase circuits are provided, one for the synchronous 16 kb/s VINSON and one for the synchronous 2.0 kb/s telemetry data. This avoids sampling the incoming data during a transition. The two data signals and frame are multiplexed together and then multiplexed with the elastic store data. The frame code and its inverse are alternately transmitted to provide a 16 kHz reference, to be used by the Receive boards for timing maintenance resynchronization.

The composite 2.304 mb/s data signal is converted to diphase and applied to the CX-11230 cable with the cable current and analog orderwire. Switch attenuators provide cable building out in 400M increments to allow the use of shortened cable systems or loopback operation.

The maintenance orderwire signal is amplified and applied to the cable through a low pass filter and half-loading coil section. This provides filtering and proper impedance match required in a loaded cable system. Included in the orderwire circuits is a 1600 Hz ring generator. This gives the operator ring capability.

The HS CDM transmit circuits are shown in Figure 11-3. Functionally they are equivalent to the LS CDM circuits basically differing in clock rates and counter moduli. This approach enables use of a common transmit orderwire module.

11.2.2 CDM RECEIVE CIRCUITS

Figure 11-4 illustrates the LS CDM receive circuits. Three PCBs, Traffic Receive A and B and Orderwire Receive perform the receive functions. Low pass filtering separates the maintenance voice signal from the digital data. A high pass filter provides the digital data to the preamp and equalizer circuits. The building out network allows the use of shortened cable lengths or loopback operation. Pulses generated from the equalized data signal zero crossings provide the 4.608 MHz spectral line necessary for clock recovery by 4.608 MHz crystal filter. The line data is then regenerated and converted back to NRZ binary with the recovered timing signal. The clock format generator generates the clock signals required for demultiplexing the digital data. These circuits are similar to the transmit circuits except for the clock delete circuits. This allows for examining all data bit positions to locate the frame codes within the overhead channel.

The demultiplexed family rate group data and associated clock are applied to the elastic store readin circuits on Receive B boards. Also applied to the elastic store is a 16 kHz signal derived from the alternate frame code. Essentially this enables the frame signal to synchronize the reference clock for the timing maintenance PLL. A 36.864 MHz (and also 37.44 MHz in the HSCDM) TCVCXO and programmable counters provide all the family rates for the elastic store read-out. The PLL uses an A/D converter to provide a quantized control voltage to the TCVCXO. When an outage is sensed, the A/D circuit is inhibited maintaining the TCVCXO control voltage (and frequency) for the outage duration. After the outage, the outage detector provides a slight delay re-enabling these circuits to allow for frame-in.

Programmable counters remove the redundancy from the data read-out of the elastic store and provide the related square wave timing signal.

The receive orderwire digital circuits provide the frame detector and programmable counters for demultiplexing the 2.0 kb/s telemetry and 16 kb/s VINSON signals. The inverted frame word is detected and generates a 16 kHz timing pulse which the Receive Traffic boards use to resynchronize their elastic stores after a timing outage.

The maintenance orderwire is terminated and separated from the composite cable signal and applied to the audio preamplifier. An AGC loop provides the correct headset level. Also a 1600 Hz ring detector generates the CALL alarm whenever the 1600 Hz ring signal is detected.

Figure 11-5 illustrates the HS CDM receive circuits. Again, except for rates and counter moduli the digital circuits are functionally equivalent to the LS CDM receive circuits. The most significant difference is in the group timing recovery circuits. Here, circuit speed limitations make it impossible to generate one clock rate from which all group timing can be derived directly. However, with two TCVCXO's and programmable counters, the group rates are synthesized from the input diphase signal. Therefore, these group clocks are also independent of the group data content.

The orderwire circuits are identical, except for counter moduli to the LS CDM. Therefore, one common design is used.

11.2.3 BITE AND TELEMETRY CIRCUITS

The CDM Bite board supplies S, SA and LS alarm indications to external equipment, and in addition will activate fault LED's on each card, LED on the bite board for loss of cable signal, and a summary fault lamp on the front panel.

The PR fault location approach utilizes the techniques developed by Raytheon in the TD754-TD-206 cable systems. PR operation is monitored by detecting the output signal to the cable. If a normal output is present, the PR is assumed good and an electronic switch shorts a resistor, connected in series with the power feed. With no output, the failed restorer and all subsequent restorers in the system switch in their fault locating resistors increasing the cable voltage.

However, direct measurement of this voltage is not accurate enough to determine the faulty restorer. Instead a resistance substitution technique and null meter are used.

When a restorer fault is suspected, the CDM operator inhibits transmission of cable traffic. This inserts all PR resistors in series with the cable current. A null meter, connected at a high impedance tap and variable current sink, obtains a measure of this cable voltage. Traffic is resumed, and all PR's before the failed unit short out their series resistor. Since transmission is conditioned diphase, no special dummy pattern is required to guarantee sufficient activity. Resistors are then switched in to return the cable voltage to the initial measured value. When the null is obtained, the number of good PR's before the fault can be determined. The resistance is switched in unit and decade increments giving the operator a direct reading. Since the voltage is built back to the original value and null technique is used, the accuracy of this method is independent of current regulation and metering errors. This approach has been proven accurate to ± 1 restorer in the TD754-TD206 40 mile system.

11.2.4 CDM POWER SUPPLY

See Section 14.

11.2.5 EMI

The line side of the CDM connects ultimately to CX-11230 cable which terminates on the shelter wall. This is a coaxial cable with very light shielding and the overall shield has very little EMI suppression. In order to keep this cable from radiating harmonics of the diphase and to reduce susceptibility to cable pick-up, it is advisable to add additional LP filtering at the input and output. This still gives acceptable system performance because this unit must deal with the frequency sensitive loss in the cable, and the additional waveshaping required for EMI suppression is less serious than this.

The equipment side signal lines into and out of this device are balanced. This balance is the primary means of EMI suppression. The external cables connected here are shielded twisted part, such as RG-108, so a high degree of suppression can be maintained. There is a wide range of bit rates on these lines, from 72 to 2048 kb/s (LS CDM) and 4.096 to 18.720 mb/s (HS CDM), and waveshaping suitable for the highest rate would be ineffective at the lowest. There are auxiliary signals for orderwire and telemetry that are also balanced. These use waveshaping and are carried externally in multipair cable. The full duplex telemetry channel has a rate of 2 Kb/s. The VINSON orderwire has a rate of 16 Kb/s. Most equipment side signals are digital and have the basix $(\sin x/x)^2$ spectral shape. There is also a maintenance orderwire of nominal bandwidth of 1.7 KHz and a balanced four wire line with a test tone level of -4 dBm. The diphase cable signal is $(\sin^2 x/x)^2$.

The power line has a single EMI filter specified for dc, 60 Hz, and 400 Hz making it larger than a conventional filter, but smaller than two filters. The power line filter has an integral power line connector which gives far better filter performance when installed on the unit and saves additional space.

11.2.6 RELIABILITY DESIGN

The CDM's have a specified MTBF of 6000 hours. This is equivalent to 166 failures in 10^6 hours. The reliability predictions and demonstrated results are summarized in Table 11-2.

TABLE 11-2

CDM RELIABILITY

Unit	Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
HSCDM	6000	12,732	20,000
LSCDM	6000	12,241	6,800

11.3 CDM DETAIL DESIGN

11.3.1 TRANSMIT CIRCUITS

Much of the CDM block diagram functions are implemented easily with available integrated circuits. Areas which required special design parameters or unique implementation include:

a. Phase locked loop circuitry

b. Elastic stores

c. VINSON auto phase

d. Telemetry auto phase

11.3.1.1 Phase Locked Loops

Two phase locked loop (PLL) designs are required for the CDM transmit circuits, a 4.608 MHz for the LS CDM and a 38.4 MHz for the HS CDM. All timing signals required by the transmit circuits are then derived from these clocks. Specific design constraints imposed on the PLL are the dc loop gain, bandwidth and lock in range.

For the LS CDM the input can be either the Elastic Store Occupancy or the received group timing at 2.304 MHz. The latter requires a divider of two to give a 2.304 MHz reference for the PLL.

For the HS CDM the input can be related timing from the input elastic store or received group timing. To avoid fm modulation of the 38.4 MHz timing, the PLL bandwidth should be less than the lowest rate into the phase detector. This is 512 kHz.

The elimination of the station clock timing option has made the PLL design relatively uncritical, since the necessity for high division ratios is eliminated and with it the chance of elastic store overflow. A $\pm$360 degree phase detector is used.

11.3.1.2 Elastic Stores

The elastic store is used in the CDM to provide two functions, to provide an automatic phase circuit for the synchronous data inputs and to accommodate the timing gaps generated by the clock format circuits. Figure 11-6 illustrates the effective timing signals generated by these circuits. As shown, pulses are deleted to generate the basic group and overhead rates. The exact group rates are then generated by the $\div 2^M$ counter circuits. For the worst cases, the timing gaps produce an elastic store occupancy excursion approaching one bit.

For the automatic phase circuit the elastic store occupancy can only be set with an uncertainty of one bit. Also the initial setting of the store can occur at any portion of the normal excursion of the elastic store occupancy. Figure 11-7 illustrates the worst case elastic store occupancies around the setting threshold.

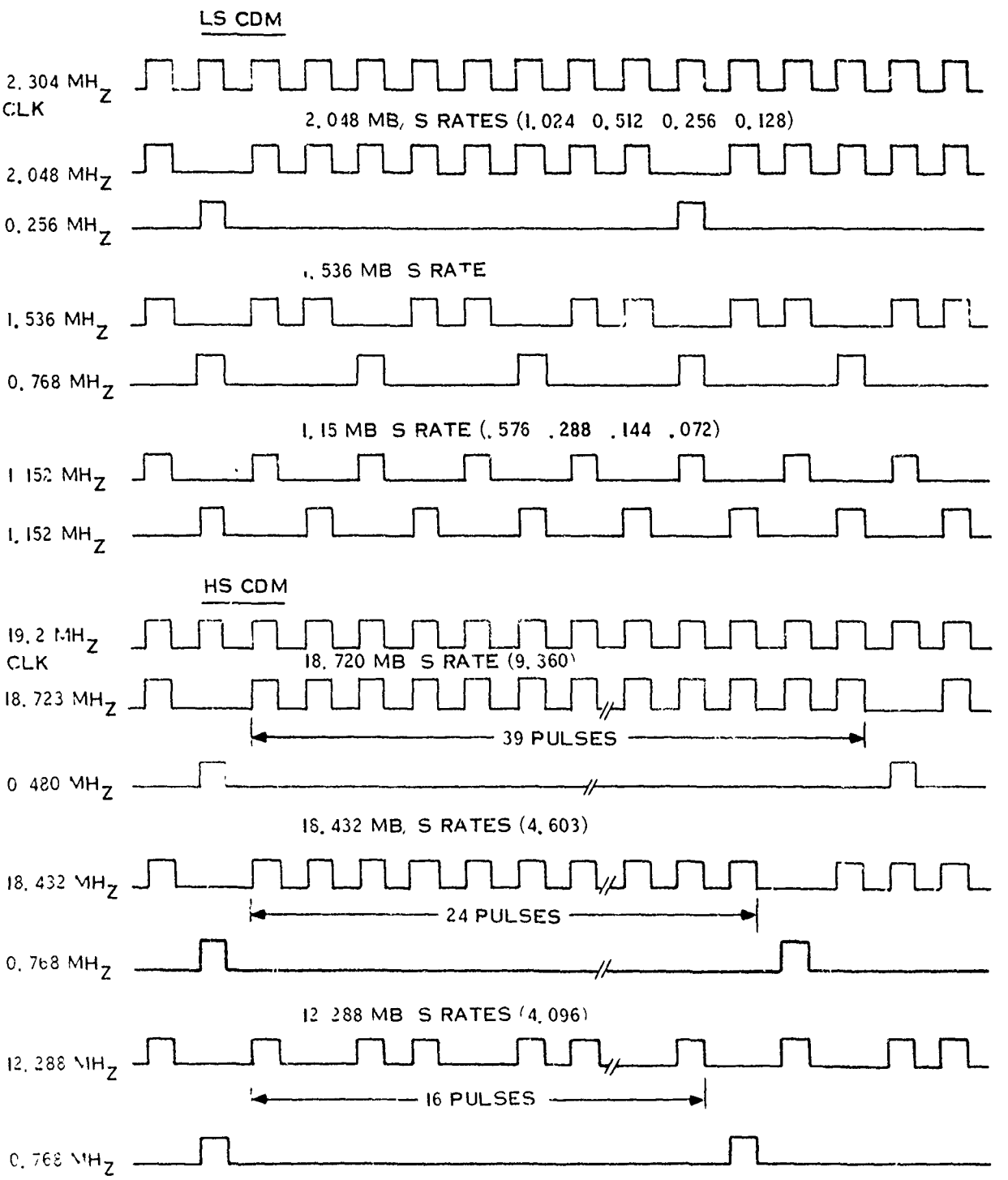


Figure 11-6. Clock Format Generator Waveforms

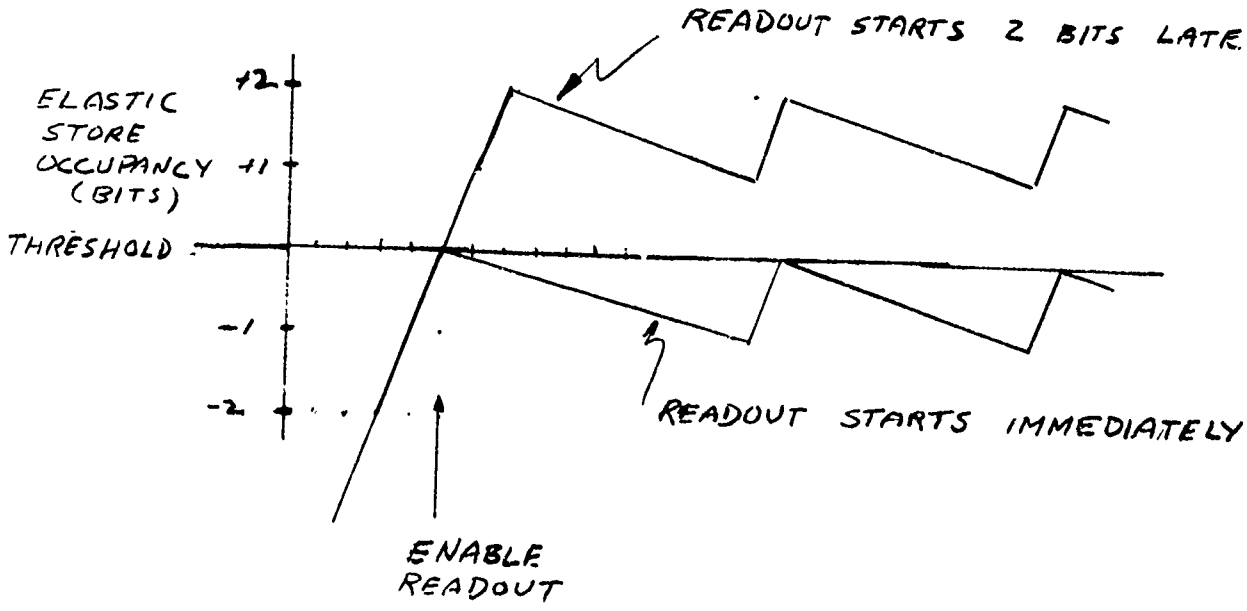


Figure 11-7. Worst Case Elastic Store Occupancies

The worst case above the threshold occurs when the store threshold is set just after a readout would have occurred. Therefore the store occupancy increases by approximately one bit before a readout can occur. Additionally, if a gap is present at this time, there is no readout and the elastic store gains another bit occupancy. The readout then starts and gives the normal "sawtooth" occupancy curve. Since the clocks are all synchronized, the occupancy curve never varies.

For the worst case below the threshold, assume a readout occurs immediately after the threshold is reached. Additionally, if the readout gap had just occurred, the store will continue to deplete one bit. The readout gap then brings the occupancy back to the threshold. As before, the occupancy path normally never varies. Therefore the store size must be greater than three bits. A 4-bit store is possible but requires a setting threshold of 1.5 bits to center the tolerance. Additionally, limit thresholds are required to reset the store if the limits are ever reached. As stated this normally never happens. However, there are events such as loss of BCI which could cause occupancy shifts in the store. Because of this and for ease of implementation, the minimum store size is six bits. For the LS CDM, use of a 9338 multiport register makes an eight bit elastic store an attractive design approach, though the device is too slow for the HS CDM.

Another demand is placed on the High Speed elastic store by the MGM. Instead of having a fixed-frequency output clock, it switches between two clocks offset high and low of the nominal rate. Tandeming of MGM's in a system can lead to lengthened dwells on the high or low clock, with a resulting filling or depletion of the HS CDM elastic store. The HS CDM phase-locked loop cannot track the deviations since its range is limited for the timing maintenance feature. To accommodate this an SSI eight-bit elastic store is used, which system analysis shows to be adequate. With the received group clock option, auto phase operation is as follows.

Initially with power turn-on or with no signal the activity detector output is at a zero maintaining U13-B cleared and U9 loaded to "3". When the detector goes to a logic "1", U13-B is enabled. U13-A already has Q=1 so when counter U11 makes the transition from state 7 to 0; U13-B is clocked to a "1" and counter 9 starts up in state 3. Thus initially the read and write states of the elastic store are well offset.

U5 detects states 6 and 7; and after a flip-flop delay this becomes states 7 and 0 on the write side. This creates a guard zone of two bits, for if the readout transition 7 to 9 falls within the zone, U13-B is clocked low and reinitializes U9 as above.

11.3.1.3 VINSON Auto Phase

The VINSON Auto Phase circuit is similar to the telemetry auto phase circuit discussed in paragraph 11.3.1.4.

11.3.1.4 2.0 kb/s Telemetry Auto-Phase Circuit

Figure 11-9 illustrates the design approach for the 2.0 kb/s telemetry data automatic phase circuit. Since this data is transmitted redundantly at 32 kb/s, 16 phases of 2.0 kHz are possible for sampling the incoming data. The sampled data is then simply gate sampled by the 32 kHz pulse assigned to the telemetry data slot. This signal is then multiplexed with the other overhead data.

The VINSON and telemetry auto phase circuits have a basic similarity. The 32 kHz frame clock is divided down to the proper sampling rate, 16 and 2 kHz respectively, and gating is used to create a sampling clock and a guard zone around it. Meanwhile a transition detector puts out pulses at the edges of the data

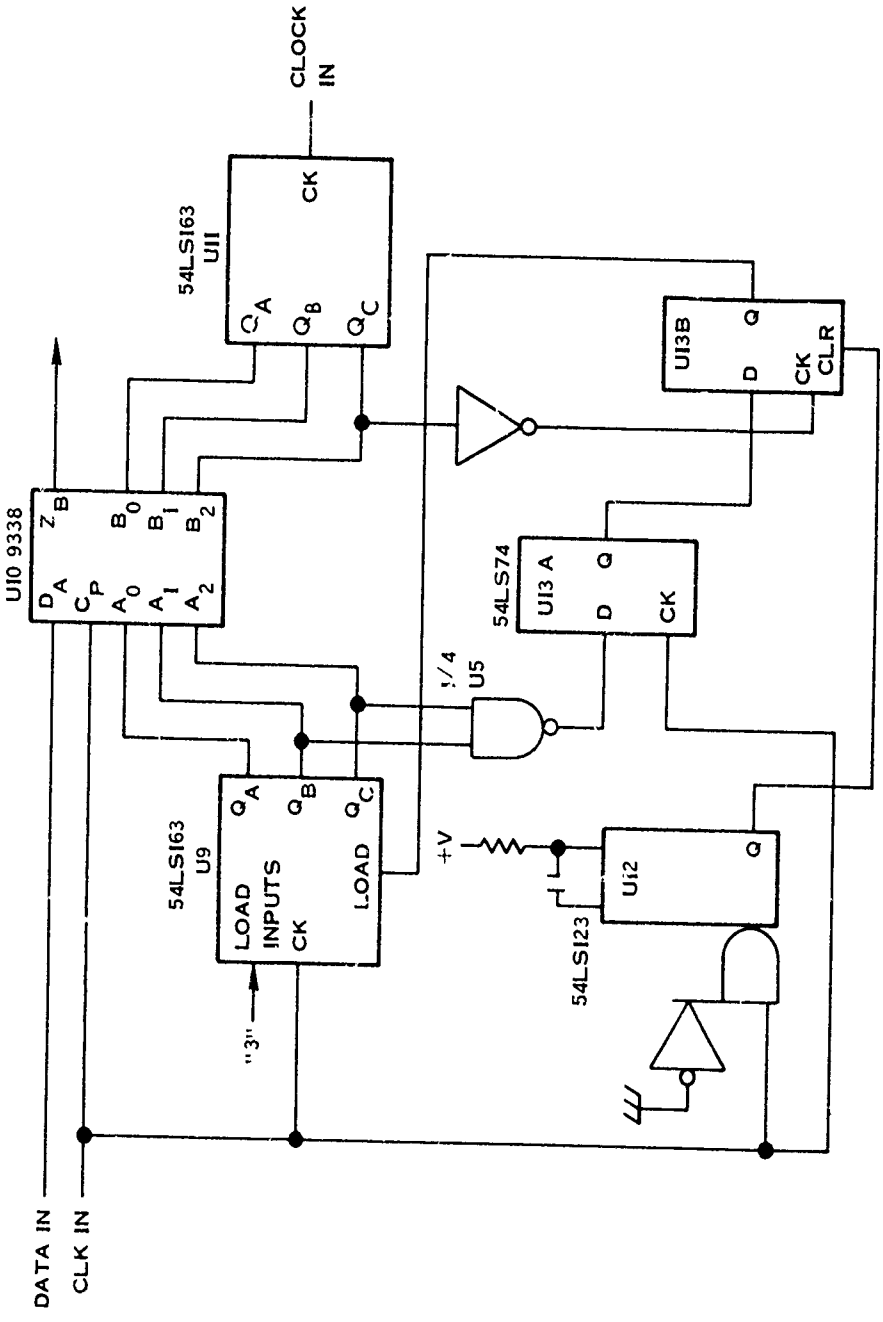


Figure 11-8. Elastic Store

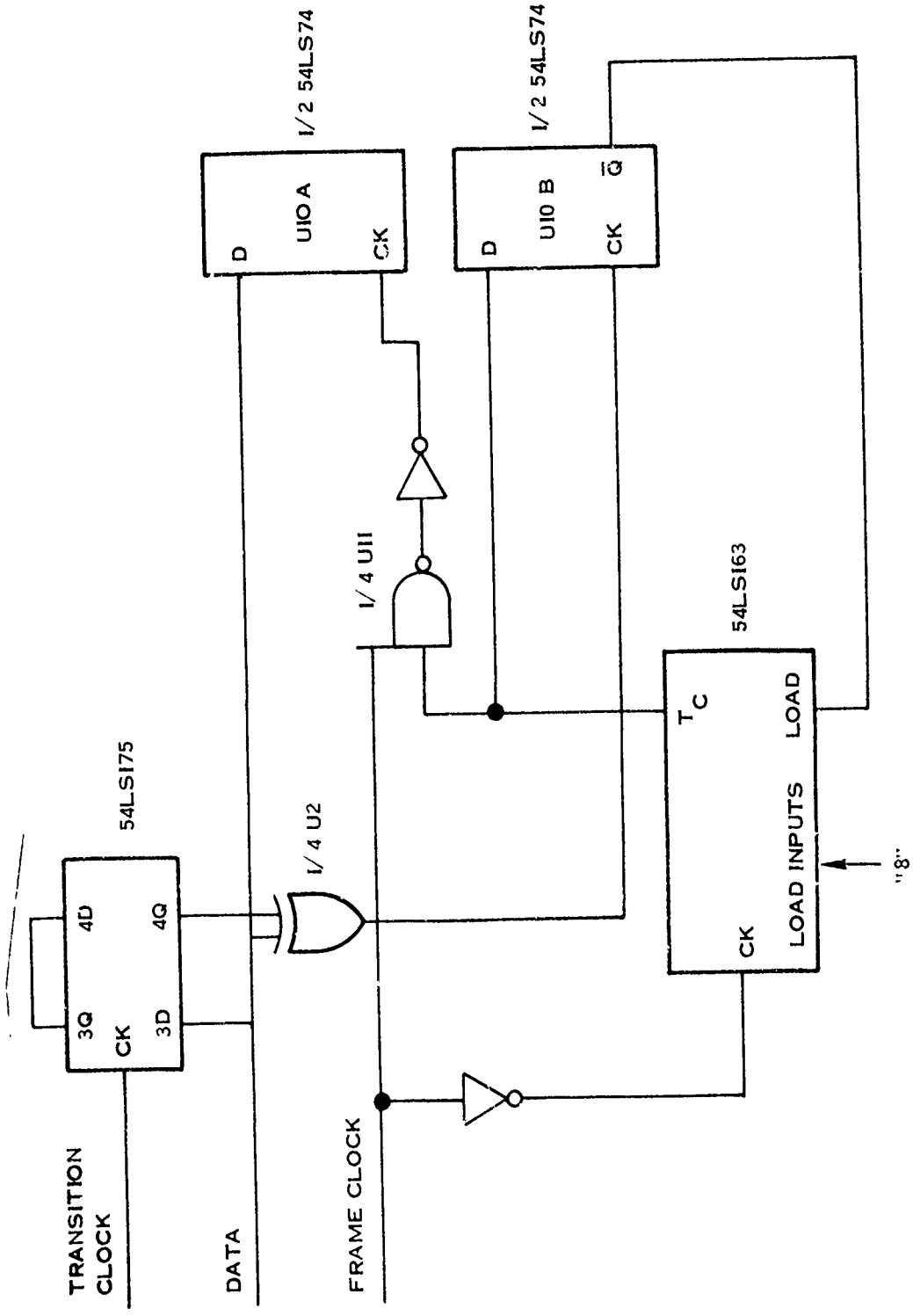


Figure 11-9. Telemetry Auto Phase Circuit

bits; if one of these pulses enters the guard zone the divider is reset and the sampling point shifted by one-half bit. Only the telemetry auto phase will be described in detail.

The 32 kHz frame clock is divided by 16 in U4; its carry output T_c selects the positive-going edge of the next frame clock to sample the data in U10-A at a 2 kHz rate. This positive-going clock edge falls in the center of the T_c pulse. Two kilobit data enters a two stage shift register U3, where it is clocked through at approximately 500 kHz by the transition clock. At a data transition the input and output of the shift register will differ for about a microsecond, creating a transition pulse at the output of exclusive-OR U2. This clocks U10-B; if the clocking occurs during the T_c carry pulse, (which acts as a guard zone around the data sampling clock) counter U4 is reinitialized to move the sampling point half a bit.

11.3.2 RECEIVE CIRCUITS

The following areas of the CDM receive circuitry are discussed:

a. Cable input circuits and regenerator
b. Trimming maintenance circuits
c. Framing circuits
d. Group demultiplexing and timing recovery

11.3.2.1 Cable Input and Regenerator

The design approach for the CDM cable input circuits and regenerator is virtually similar to their counterparts in the PR's. These circuits are discussed in detail in paragraph 12.3. The additions to the pulse restorer circuitry are: a cable input activity detector for BITE purposes, a diphase-binary converter using a shift register with gating, and an outage detector for timing maintenance using one-shots.

11.3.2.2 Timing Maintenance Circuit

The Timing Maintenance approach (A/D converter) uses an elastic store controlled PLL. The phase reference is derived from the 16 kHz alternate frame clock. This allows the use of less critical VCXO's to meet the 500 ms outage requirement.

With the use of Figure 11-10, the A/D approach can be analyzed to determine the outage performance. As shown the total phase detector range is ± and the

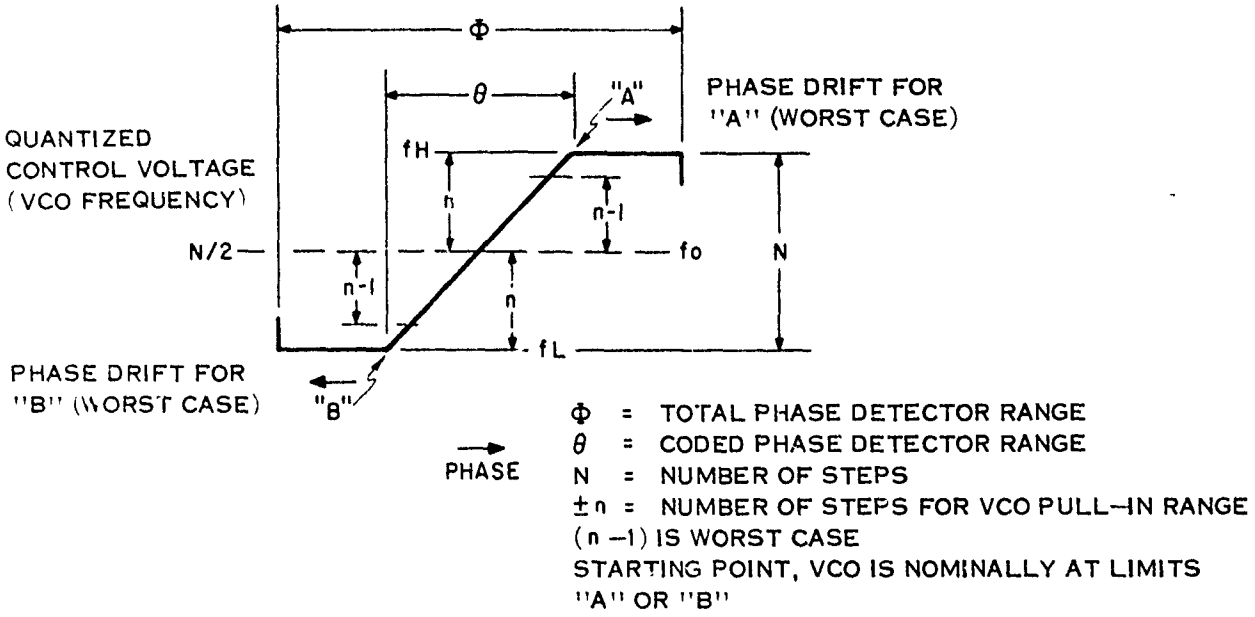


Figure 11-10. Timing Maintenance PLL Considerations

control voltage is quantized to N steps. The coder range corresponds to a phase range of θ radians. In normal operation it is assumed that the required control voltage varies by only one step. In effect, the actual frequency is derived by time averaging of two very close frequencies. The worst case occurs when the VCO is just marginally below the maximum offset. Additionally it is assumed that the outage occurs when the last sample was one step below the actual limit frequency.

The frequency error of one step is then:

$$\frac{\Delta F}{n} = \frac{\Delta F}{\frac{N}{2}} = \frac{2\Delta F}{N} \qquad (1)$$

where

$\pm\Delta f$ = pull range of VCO

and the phase error (ϕ_e) is

$$\phi_e = \frac{4\pi\Delta f}{N} \qquad (2)$$

the total phase drift allowable before the phase detector range is exceeded, thus causing a loss of BCI is:

$$\frac{\Phi-\theta}{2} \tag{3}$$

to calculate the worst case outage time (TWC) before a loss of BCI

$$TWC \times \phi_e = \frac{\Phi-\theta}{2} \tag{4}$$

solving for TWC

$$TWC = \frac{N}{8\pi\Delta f} (\Phi-\theta) \tag{5}$$

During an outage the timing output from the data regenerator dies out and the phase detector cannot have a frequency memory. Therefore a $\pm\pi$ type (set-reset) flip-flop is the best choice. For this detector, with an 8 bit elastic store and $\theta=0.4\Phi$, the worst case timing outage allowable is:

$$TWC_L = \frac{306}{\Delta f} \text{ (LS CDM)} \tag{6}$$

For a 6 bit elastic store and $\theta=0.4\Phi$

$$TWC_H = \frac{229.5}{\Delta f} \text{ (HS CDM)} \tag{7}$$

With a maximum elastic store rate of 2.048 MHz and a $\pm$20 ppm pull in range VCXO, the worst case outage for the LS CDM is:

$$TWC_L = \frac{306}{20 \times 2.048} = 7.47 \text{ sec} \tag{8}$$

With a maximum elastic store rate of 18.72 MHz and a $\pm$20 ppm pull in range VCXO, the worst case outage for the HS CDM is:

$$TWC_H = \frac{229.5}{20 \times 18.72} = 0.613 \text{ sec.} \tag{9}$$

Therefore the 8 bit A/D converter approach (6 bits in the HSCDM) with $\pm$20 ppm pull in range VCXO's meets the system requirements.

11.3.2.3 Framing Circuits

The CDM format all utilize a six bit frame code multiplexed in the overhead data. To acquire frame, six bits (at the frame rate) are searched to determine if the code or its inverse is present. For all rates and formats, the frame is

generated at the 32 kHz rate. If the six bits do not correspond to the frame code, a skip pulse is generated and six other bits are checked.

To determine if the true frame has been found, 7 tests are required. For the six bit frame and its inverse, the simulation probability of 1/32. The simulation probability for consecutive tests is $(1/32)^7$. As can be seen, the false frame probability is quite small. A threshold of n = 5 correct frame codes out of seven is required to stay in frame. For the LS CDM a maximum of 72 frame locations must be searched during frame-in, while for the HS CDM 600 frame locations are the maximum. This gives maximum average frame in times of 2.4 ms and 19.1 ms for the LS CDM and HS CDM, respectively. Note that the CDM framing is not dependent on failures or degraded performance of the radio.

The frame code for the CDM is 110010.

11.3.2.4 Group Demultiplexing and Timing Recovery

Once frame is established, the positions of all data bits are known and the digital signals are readily demultiplexed using conventional digital techniques. However in the LS CDM for the 2.048 kHz and 1536 kHz family rates the demultiplexed signals are period distorted. This effect is worse for the 2048 kHz and 1536 kHz group rates, where the distortion is almost one bit. Therefore the signals must be buffered.

The problem is similar in the HS CDM except all family rates have distorted data bits. Worst case is for the 18.720 Mb/s group rate.

Buffering of the demultiplexed data is accomplished with an 8 bit (LS CDM) or 6 bit (HS CDM) elastic store and a PLL utilizing the store occupancy to derive "smoothed" timing. The PLL bandwidths are low enough to eliminate effects of the input period distortion. Since store occupancy controls the PLL, no overflow reset is required. There is a 16 kHz reset pulse synchronized with reception of an inverted frame code, which re-establishes the input address waveform to the elastic store after a timing outage.

11.3.3 HFE

The CDM design incorporates the requirements of MIL-STD-1472 to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements will be incorporated onto the accessible edge of the PCB's, with the exception of the building out DIP-switch, which is mounted on the PC board. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connectors are located on the rear of the case and are positioned to ensure maximum accessibility. The front panel layouts of the HS CDM and LS CDM are shown in Figures 11-11 and 11-12. The rear panel layouts are identical and is shown in Figure 11-13.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472.

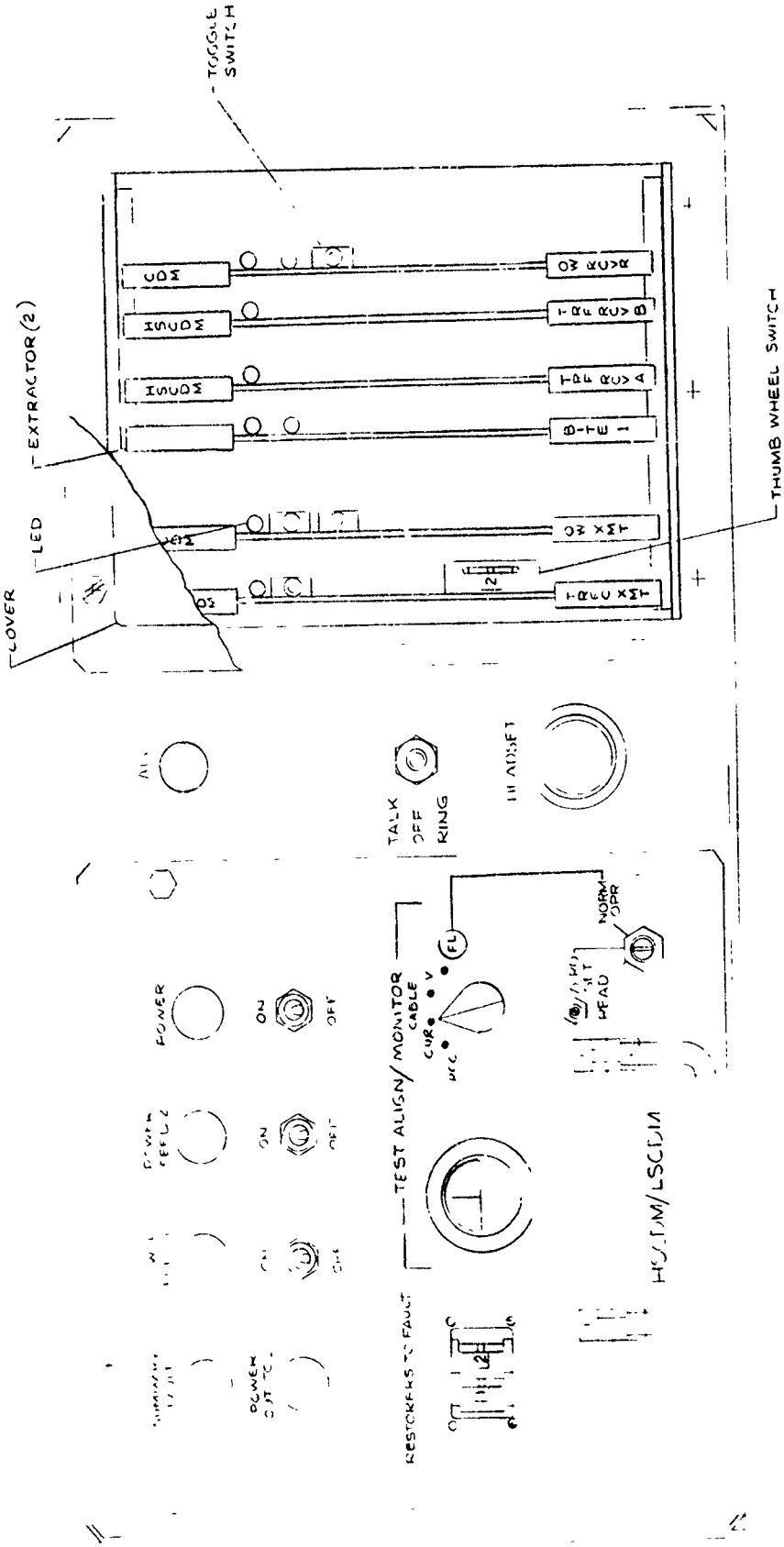


Figure 11-11. High Speed CDM Front Panel

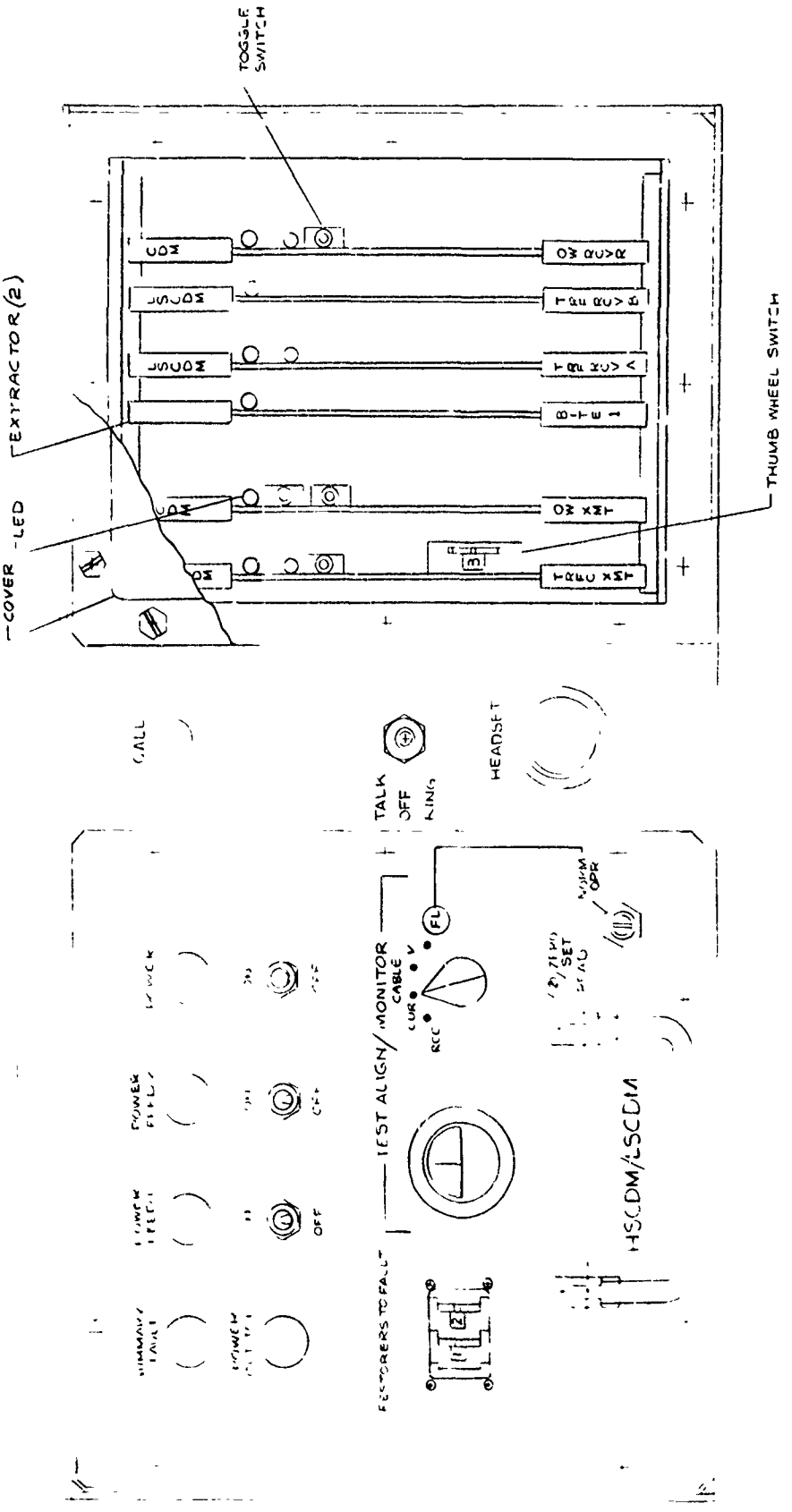


Figure 11-12. Low Speed CDM Front Panel

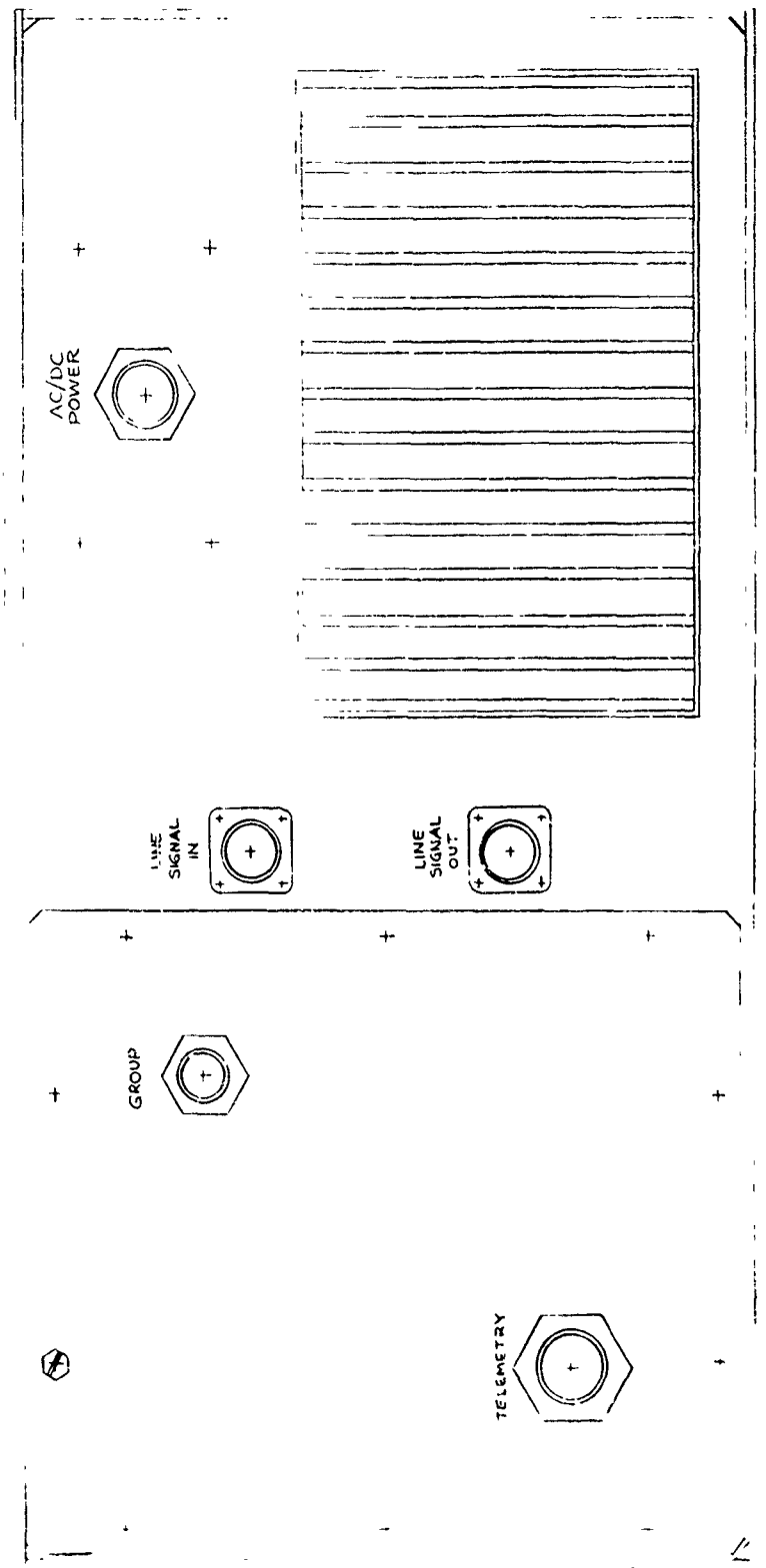


Figure 11-13. High and Low Speed CDM Rear Panel

SECTION 12
PULSE RESTORERS

12.1 DESIGN GOALS AND REQUIREMENTS

Two types of pulse restorers were developed on the DGM program, a low speed pulse restorer (LSPR) and the high speed restorer (HSPR). These units, used with the LS CDM or HS CDM respectively, provide extended range repeatered cable systems. Both units provide identical functions for the DGM systems. They are:

a. Regenerate and retime the conditioned diphase data signal (2 Mb/s and 19 Mb/s rates for the LSPR and HSPR, respectively).

b. Passively pass 300 to 1700 Hz maintenance orderwire signal and provide loading coil to minimize cable loss.

c. Provide COU access to the maintenance orderwire.

d. Provide means for location of faulty restorer at the CDM.

Specific design parameters and requirements are:

a. Spacing 1.6 km (1 mile) low speed
0.4 km (1/4 mile) high speed

b. Maximum system length
64 km (40 mile) low speed
8 km (5 mile) high speed

c. Cable type CX-11230

d. Signal characteristics

DATA, low speed conditioned diphase, 2.304 Mb/s, 2 VPP into 62Ω

DATA, high speed conditioned diphase, 19.200 Mb/s, 1.5 VPP into 62Ω

e. Cable power LS 40 mA at 750 Vdc max
HS 80 mA at 350 Vdc max

f. Maintenance orderwire access to COU

g. MTBF - 50,000 hrs minimum

12.2 PR DESIGN APPROACH

Figures 12-1 and 12-2 illustrate the block diagram design approach of the LSPR and HSPR respectively. As shown, the designs are similar. The high speed system has 1/4 mile repeater spacing and a five mile length. Figure 12-3 illustrates the loaded cable characteristics for the high speed system.

In the LSPR, the composite cable signal from a one mile section of CX-11230 is separated into two paths; diphase data, and maintenance orderwire and cable current. Separation is accomplished with passive filters.

A high pass filter separates the diphase data and applies the resultant signal to the EQUALIZER preamp. The high pass cutoff frequency is 30 kHz. This does not degrade the diphase "eye" opening appreciably and was chosen to provide the necessary isolation between the maintenance orderwire and diphase data signals. Figure 12-4 illustrates the effect of high pass filtering on the diphase "eye" opening. Note the good experimental agreement with computer models.

The EQUALIZER preamp provides approximately 35 dB of gain and the required frequency response to compensate for one mile of CX-11230 cable. With excessive high pass filtering, one equalizer design for maximum eye opening and minimum zero crossing jitter is not possible. Reduced eye closure worsens the signal to noise performance while zero crossing jitter introduces "pattern" sensitivity in the recovered timing signal. A severe example would occur if all diphase "1's" or "0" were transmitted for an appreciable time, followed by complimentary or normal random data. Here the sample timing would be initially displaced from the optimum at the start of the random data. With the smaller "eye" created by high pass filtering this would increase the noise susceptibility and possible cause data errors. Unfortunately, the above data patterns are typical during other DGM equipment frame-in routines.

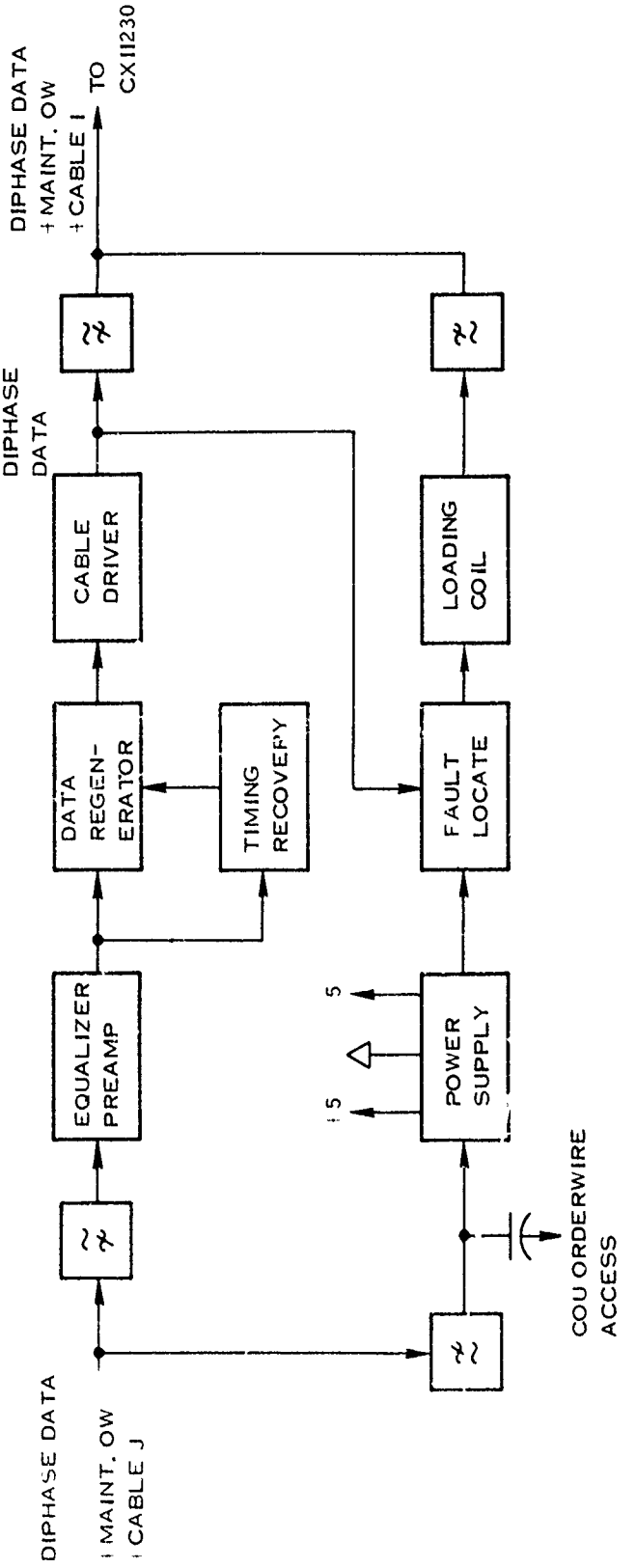


Figure 12-1. LSPR Block Diagram

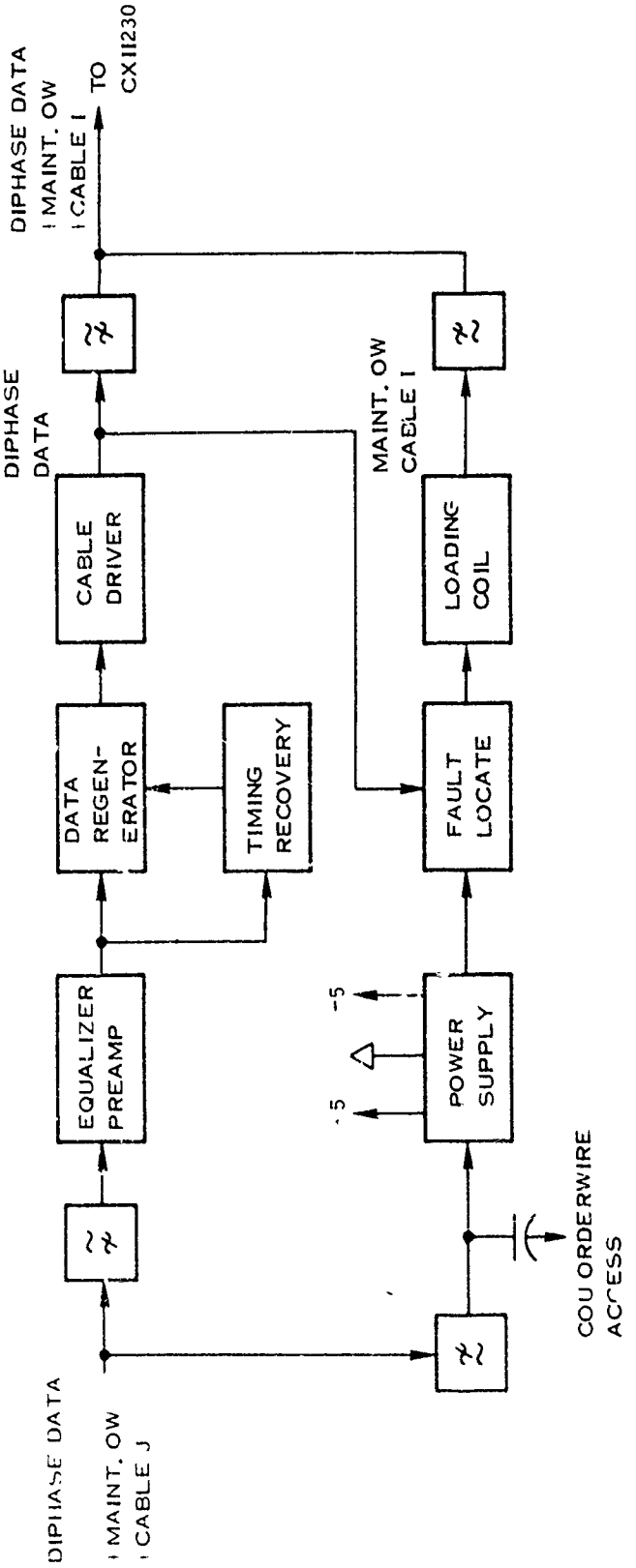


Figure 12-2. HSPR Block Diagram

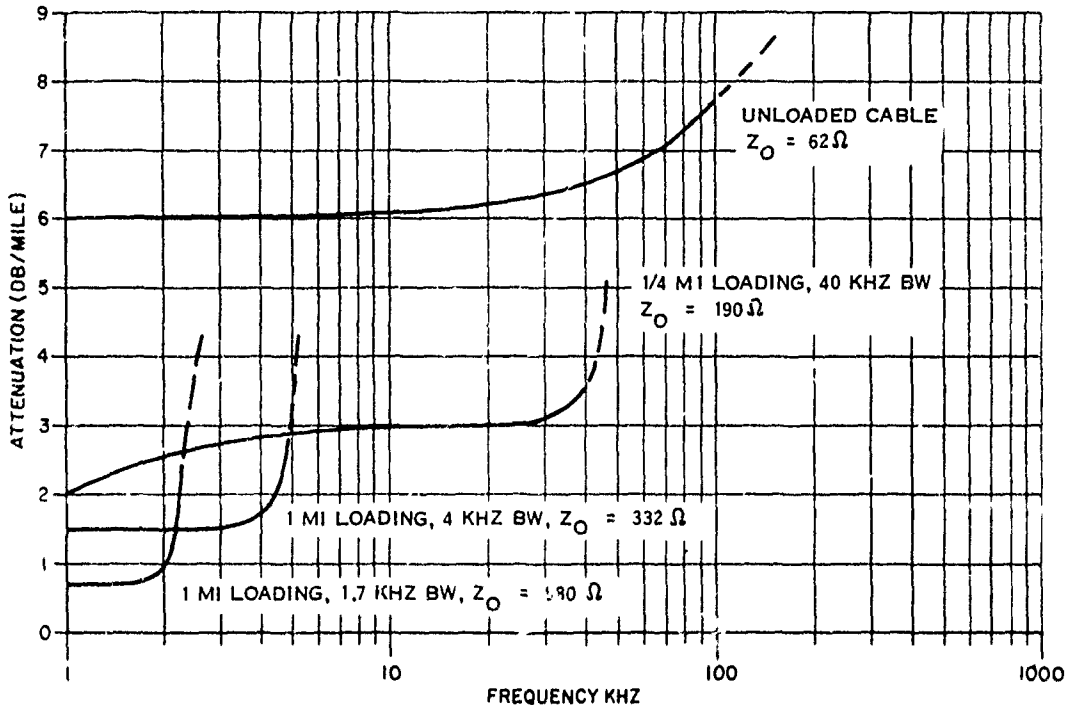


Figure 12-3. Loaded Cable Attenuation

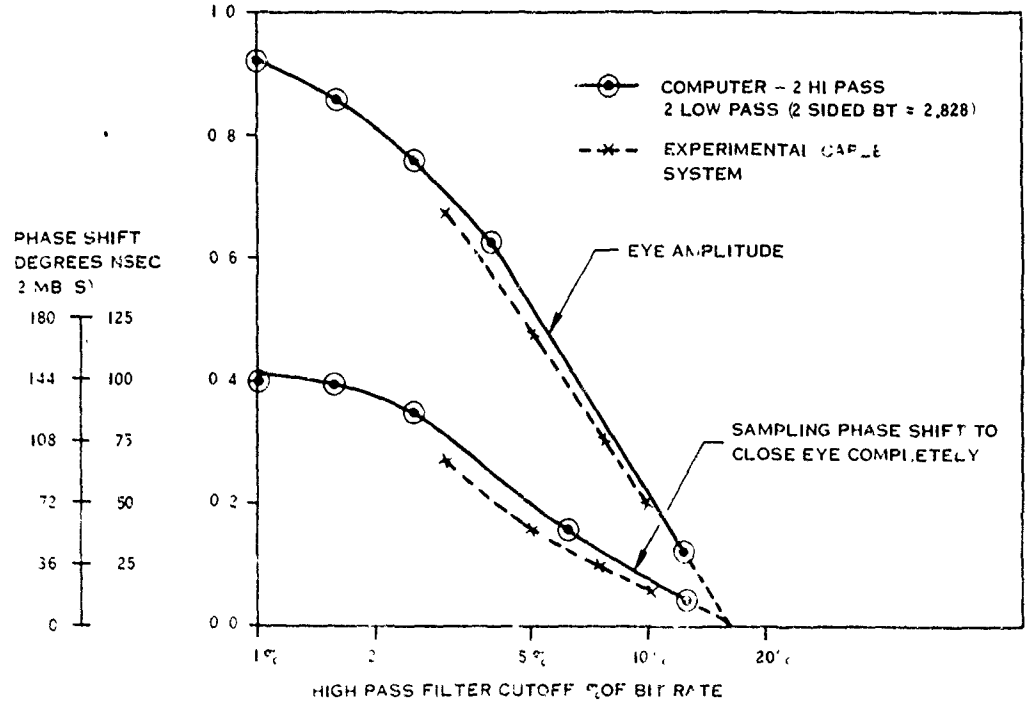


Figure 12-4. Eye Parameters vs Hi Pass Filter Cutoff

Two design approaches are available, a compromise equalization or separate equalization for the data and timing recovery. Obviously, the latter is more complex and with the severe size, power, weight restrictions in the restorer, the compromise equalization is preferred. Compromise equalization is feasible and has worked well with severe data patterns. This approach was chosen.

After equalization, the recovered timing at twice the data rate samples the equalized data signal to regenerate the conditioned diphase signal. This is applied to a cable driver which supplies, through another high pass filter, the diphase data to the CX-11230 cable. The transmit high pass filter is required to enable recombining the diphase data with the other cable signals.

A second signal path passes the cable current and maintenance orderwire signals. A low pass filter provides this separation. The restorer dc voltages are derived from the cable current with zener diodes. The HSPR and LSPR design will use +5 and -5V. The maintenance orderwire signal effectively bypasses the supply due to the low zener impedance and filter capacitors. The dc current flows through the FAULT LOCATE circuit. Basically, this is a resistor shunted by a transistor switch. If the diphase data output is not present, the switch opens inserting an additional series resistance in the cable current path. By using a resistor substitution technique and traffic interrupt routing, the source CDM can locate the faulty restorer to ± 1 mile over the full 40 mile span. Again the maintenance orderwire bypasses this circuit. Since this approach requires all restorers to lose traffic after the faulty one, it is imperative that no data be regenerated from noise by the data circuits. This will be accomplished by providing slicing thresholds in the timing recovery circuits.

The loading coil passes the dc cable current and provides an inductance to artifically increase the characteristic impedance of the line at the maintenance orderwire frequencies. For this system, the line impedance is raised to 430 ohms giving a 300 to 1700 Hz flat pass band with a loss of approximately 1.0 dB/mile. The maintenance orderwire and cable current signals are then recombined (through a low pass filter) with the other cable signals.

The HSPR design approach is similar except relatively less high pass filtering is required to maintain adequate isolation between the data and orderwire signals. Therefore, normal equalization does give good eye openings and zero crossings. Conceptually the timing is recovered and data regenerated and applied to the cable as in the LSPR.

The maintenance orderwire and cable current are separated with a low pass filter and processed by circuitry similar to the LSPR. The power supply voltages are +5 and -5V. The diphase data controls the transistor switch in the FAULT LOCATE circuits. Again threshold circuits are required in the timing recovery circuits to insure that no output is present with no input signal. The loading coil now selected to provide the same loaded line impedance as in the LS system, with 1/4 mile spacing provides somewhat less attenuation and a 3400 Hz orderwire band. These signals are then recombined with a low pass filter.

12.2.1 EMI

The restorer data output has additional low pass filtering (similar to the CDM) to reduce harmonic radiation and susceptibility to cable pickup (see paragraph 11.2.5). Filters are incorporated on the orderwire connector signals for EMI suppression.

12.2.2 RELIABILITY DESIGN

The PR has a specified MTBF of 50,000 hours. This is equivalent to 20 failures in 10^6 hours. The reliability predictions and demonstrated results are summarized in Table 12-2.

TABLE 12-2

PR RELIABILITY

Unit	Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
HSPR	50,000	157,978	130,000
LSPR	50,000	146,413	130,000

12.3 DESIGN DETAILS

12.3.1 HIGH PASS FILTER AND EQUALIZER PREAMP

Figures 12-5 a and b show the high pass filter input and equalizer preamplifier design for the PR's. Basically the preamplifier must equalize the cable losses

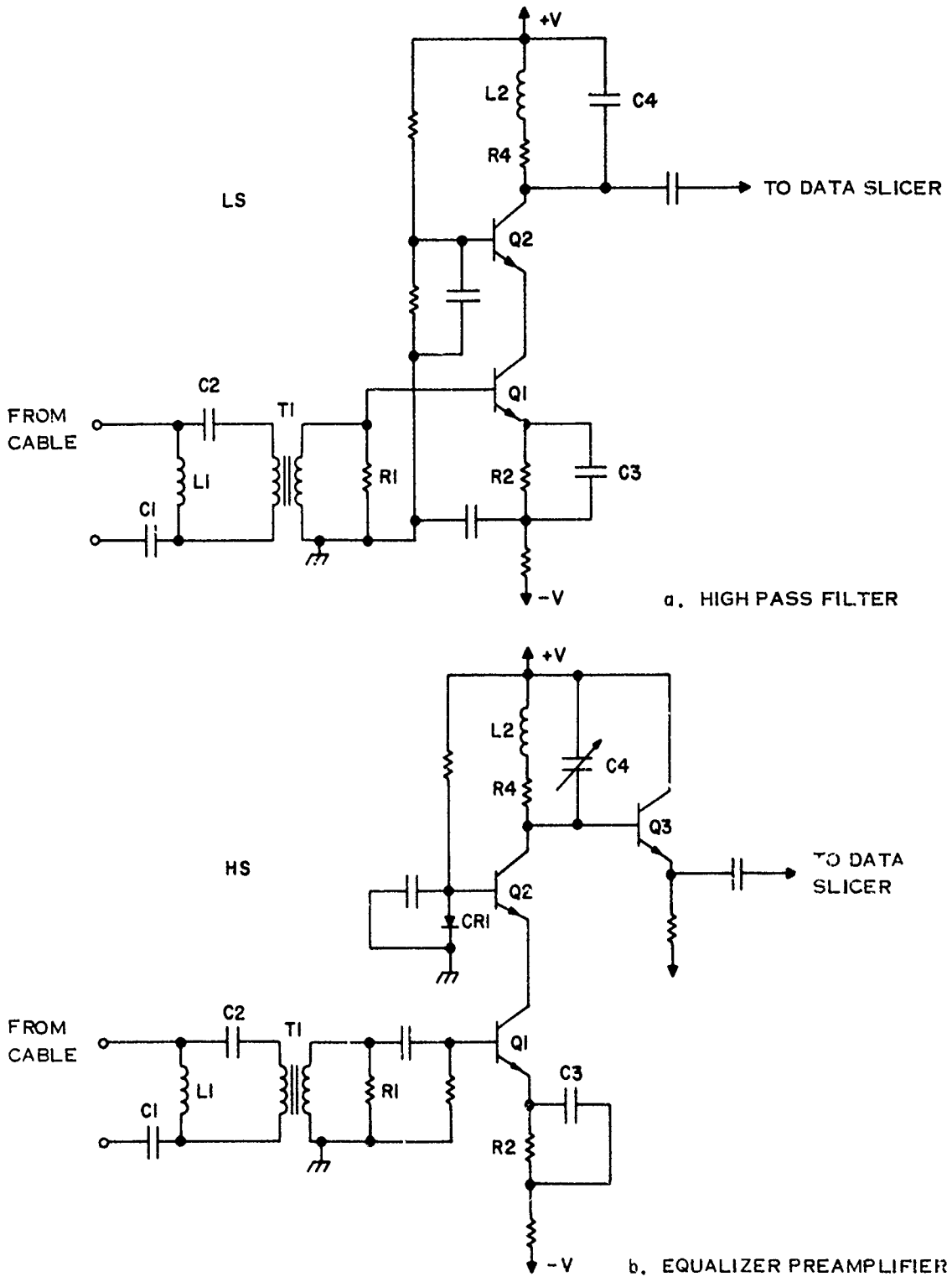


Figure 12-5. High Pass Filter and Equalizer Preamp Circuitry Design

for one mile of CX-11230 in the LSPR and 1/4 mile CX-11230 in the HSPR (Figure 12-6). New measurements indicated near end crosstalk (NEXT) is a less serious factor in the high speed system than originally thought. The length differences and rate differences combine so that the overall response required to equalize is similar in both PR's except for the actual break frequencies. However, the high speed case generally requires more care and lower impedance levels.

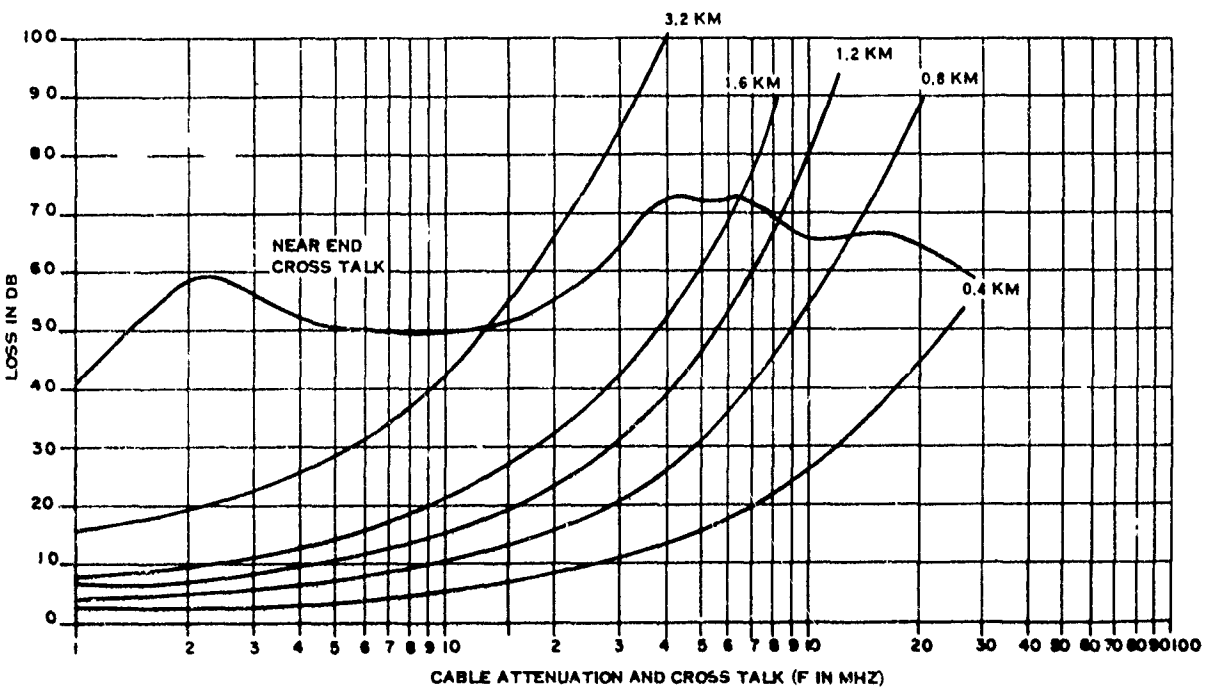


Figure 12-6. Cable Attenuation and Crosstalk (F in MHz)

To insure that the 3-pole Butterworth high pass filters (C1, C2, L1) give the desired response, the input impedance at T1 matches the cable impedance and provides a relatively constant resistance over the frequency band of interest (approximately 0.13 times the bit rate to the bit rate). This is provided by transformer T1 and R1 as the loading of amplifier stage. Transistors Q1 and Q2 comprise a cascade amplifier stage. This circuit has had all the advantages of a common emitter stage and gives a good isolation of output to input. This allows large stage gains without "Miller" multiplication of the transistor collector to base capacitance. Although not critical in the LSPR, this is important in the high speed design. Also, there may be advantages in an eventual hybrid design if the configurations are similar.

The first breakpoint is determined by the R2, C3 combination. Breakpoint frequencies are 450 kHz and 4.6 MHz for the LSPR and HSPR, respectively. Capacitor C3 is chosen so its impedance at maximum equalization frequency is greater than the transistor input base impedance (h_{ib}). This provides degeneration and offers gain stability. The second breakpoint is determined by the Q2 collector circuit comprising R4, L2, and C4. The resonant frequency of this combination determines the maximum frequency equalized (usually slightly above the bit rate) while the effective Q determines the magnitude of the gain increase. Figure 12-7 shows a photo of the equalized signal for a three percent cutoff high pass filter with the circuit. For the LSPR, a 1.3 percent filter gives better equalization and provides adequate data and orderwire isolation. The HSPR preamp differs from the LSPR by the addition of CR1 in the base circuit of Q2. CR1 is added to stabilize the operating point of Q2 over temperature. Q3 serves as Buffer Stage to prevent loading of the tuned circuit in the collector of Q2.

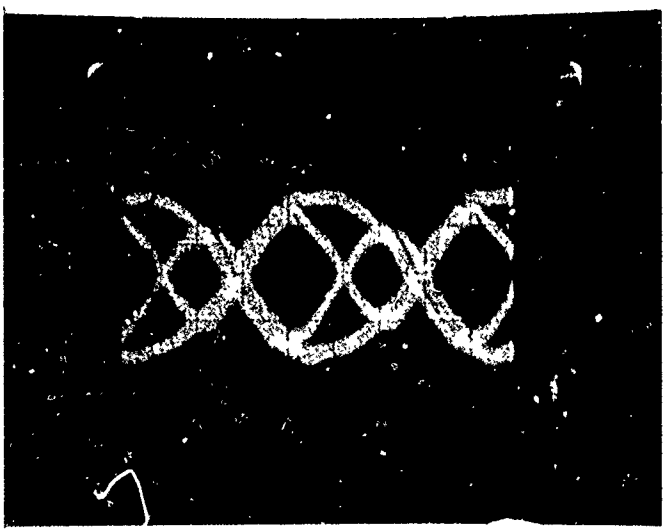


Figure 12-7. Equalized Eye, 3 Percent High Pass Filter

In the HSPR the equalizer signal will be shifted to MECL levels directly while in the LSPR the slicer provides TTL levels. This enables the use of a "D" flip flop sampling circuit in either PR.

12.3.2 TIMING RECOVERY CIRCUITS

The timing recovery (see Figures 12-8 a and b) derived from the received signal, the twice bit rate clock necessary for regeneration of the diphase data signal. Since the normal diphase signal contains no energy at this rate, a non-linear timing recovery technique is required. The preferred approach generates pulses (0.25 the pulse width wide) for each signal zero crossings. This provides the maximum timing energy and the least sensitivity to the actual signal amplitude. The approach is basically the same for the low and high speed model. Pulses must be generated from the sliced data, and from these pulses timing are extracted. The pulses are produced by the full wave rectifier composed of Transistors Q3 and Q4. The Emitter-Base junction of the differentially driven transistor is used as the non-linear element; the collectors are strapped to yield the full wave rectification. This circuit is an inefficient rectifier in the sense that unless the input signals exceed 2 times VBE of the transistor, there is no output. This provides for noise immunity to prevent timing energy from being recovered with no input data.

The crystal filter timing recovery circuit shown, evolved after an unsuccessful attempt was made to use an LC timing recovery network. Important criteria for selection of the timing recovery approach are frequency stability and bandwidth. For a given stability, the Q should be selected as low as possible to avoid excessive phase shifts of the sampler clock. However, the Q must be sufficient to avoid excessive AM with normal data signals. For conditioned diphase loaded Q's of 20 are adequate. A conservative estimate for the phase shift due to drift for a single tuned circuit is $\Delta\phi = \frac{DQ}{4}$, where $\Delta\phi$ is the phase shift in fractions of a bit, D is fractional drift and Q is the loaded Q of the timing filter. For Q = 20 and D = $\pm$0.02 ($\pm$2%) $\Delta\phi$ = 0.1 bit. This is good, although with the degraded "Eye" shown in Figure 12-7 it does give a 2 dB S/N penalty. Preliminary testing showed, however, that the LC circuit had a jitter which would be too much for a 40 mile system. Therefore, a crystal filter approach was adopted.

The resultant pulses from the pulse generator are fed to Y1, C1 in the LSPR and L1, L2 in the HSPR. In both models the adjustment of C1 is necessary to tune out the stray capacitance of the crystal. This is a one time adjustment made

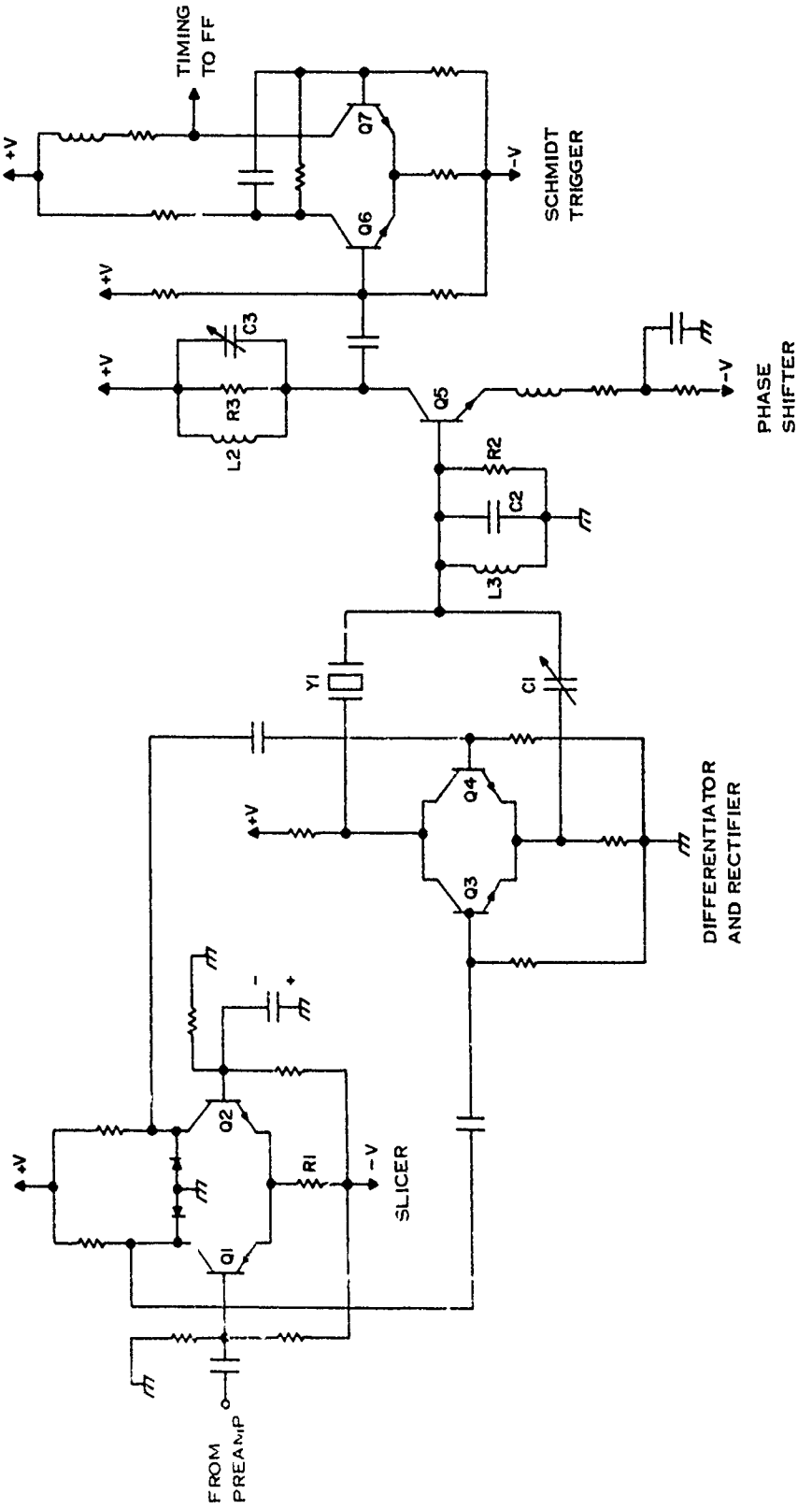


Figure 12-8a. LSPR Timing Recovery

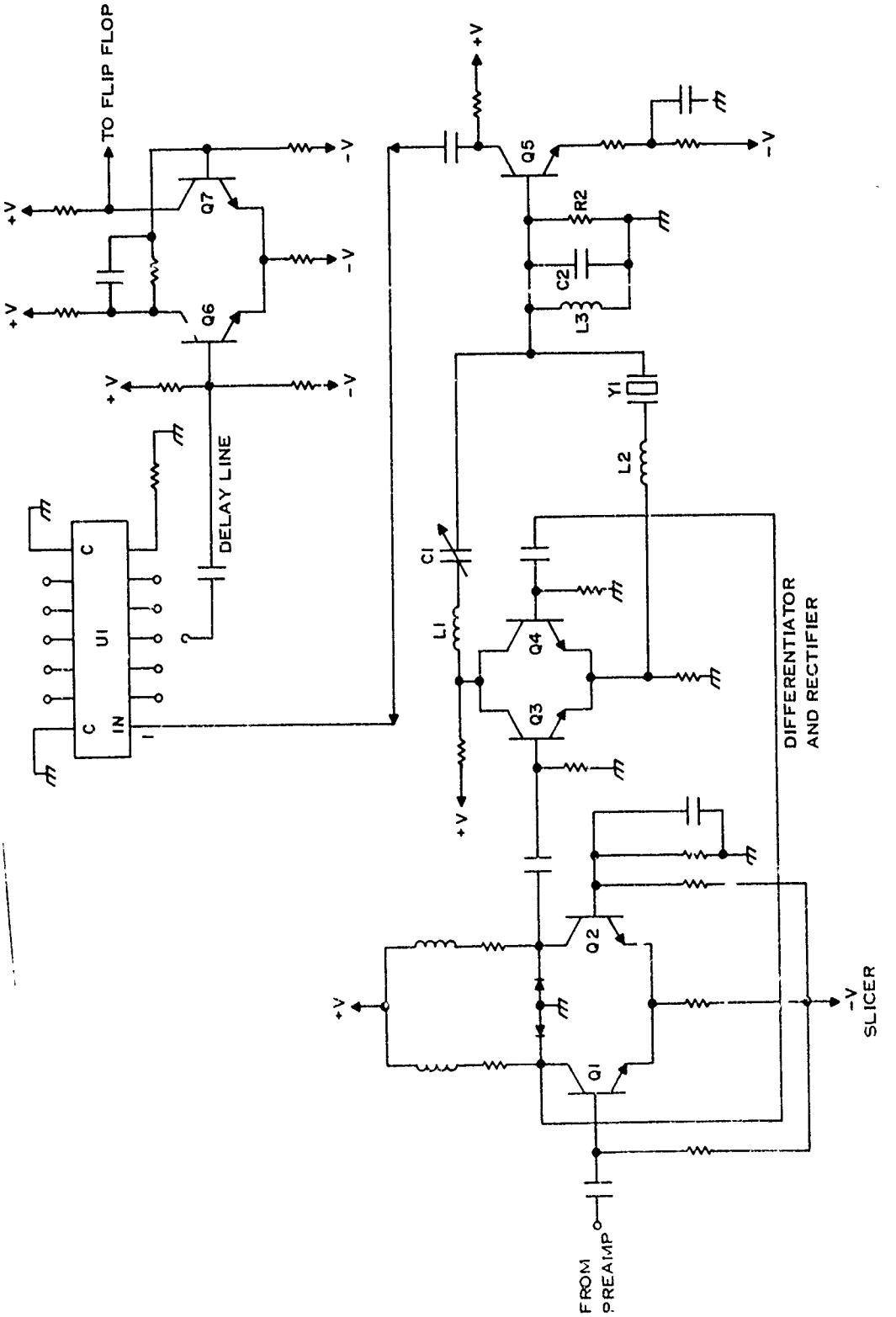


Figure 12-8b. HSPR Timing Recovery

at the factory. The output of the crystal is followed by an RLC bandpass filter (R2, L3, C2) to provide out of band rejection of any spurious crystal response as well as lowering the Q of the crystal filter.

In order that the recovered clock phase be aligned with the optimum sampling point in the data bit, some form of phase adjustment must be provided to compensate for component delay variations. This adjustable phase shift is provided by U1 (in the HSPR) which is a tapped delay line. Q5 is a buffer amplifier providing gain between the timing recovery filter output and the tapped delay line. The delay line has a total phase shift of 140 degrees with taps every 14 degrees. In the LSPR this adjustment is made at the tuned amplifier and phase shift circuit composed of Q5, L2, R3, and C3. This circuit has worked well and provides a relatively constant output over the adjustment range.

The resultant sine wave signal is ac coupled to the SCHMITT Trigger in both repeaters which has been designed to provide a leading edge of the clock at the positive going zero crossing. This minimizes phase shift with variation in sine wave amplitude.

12.3.3 CABLE DRIVER AND HIGH PASS FILTER

The PR's will use a single ended driver to generate the diphase signal to the cable (Figure 12-9). A single transistor circuit is used to enable easy detection of a no signal condition required for fault location. In the LSPR, to reduce the supply current requirements, the output switch is connected across both supply voltages. A series resistor provides short circuit protection and with the damping diode (CR1) provides a resistive output suitable for designing the high pass filters. However, the smaller signal gives less immunity against the external noise threat. A 2 VPP signal will be used in the LSPR as it has proved to be acceptable in the TD-206 cable system. A 1.5 VPP signal will be used in the HSPR. The 3-pole Butterworth high pass filter comprises L1, C1 and C2.

In the HSPR, the MECL flip flop draws an appreciable amount of current from the -V supply. To provide efficient utilization of the power available from the constant current supply, it is best to balance the current loads on both supplies. Therefore, the cable driver is supplied from the +V supply alone. Circuit

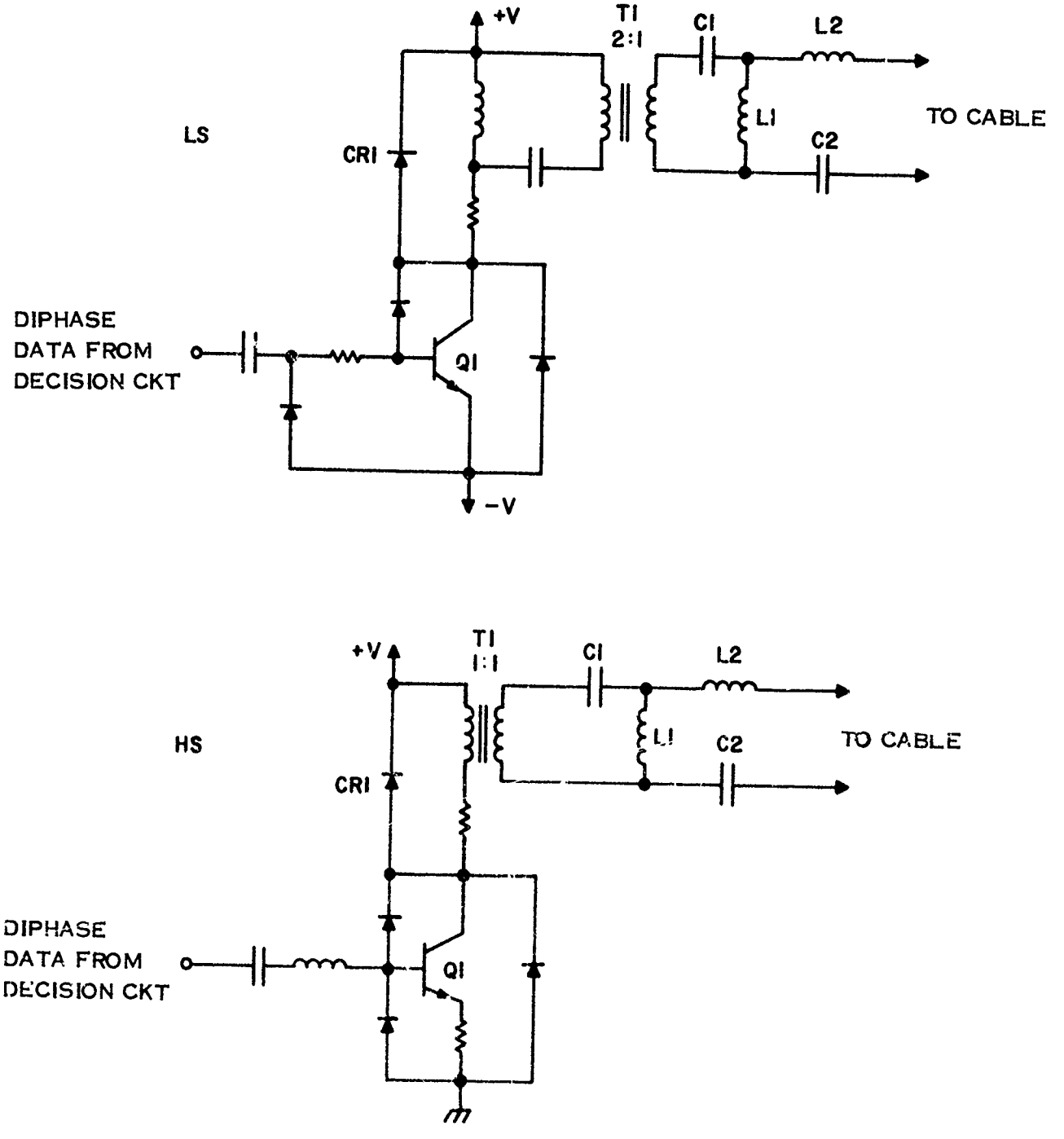


Figure 12-9. PR Output Drivers

considerations are otherwise identical except at the high speed rate, storage time of the transistor switch becomes a problem. To avoid saturation, a hot carrier diode is connected across the collector and base of the transistor driver (Q1). Except for the circuit values, the high pass filter approach is identical with the LSPR.

Other considerations of the driver output are the EMP protection circuits. Low voltage TRANSORBS and diodes are sufficient for this purpose.

12.3.4 DATA REGENERATOR CIRCUITS

The diphase signal is regenerated by sampling the data signal "eye" and storing this decision until the next "eye" is sampled. This requirement is best implemented with a D type flip flop. No discrete version of this circuit function has proved to be size, power, or cost competitive with the IC versions. Therefore, the LSPR will use a TTL 54LS74, and the HSPR will use an MECL MC 1222 for this function.

12.3.5 POWER SUPPLY

The PR power supplies are derived (with regulator diodes) from the constant current supplied by the CDMS. The use of the IC flip flop dictates a +5V supply in the LSPR and a -5V supply in the HSPR.

Low voltage avalanche diodes (LVA) will be used rather than normal zener diodes. In the 4 to 10V range, these devices exhibit considerably sharper breakdown characteristics than zener diodes, giving better regulation and requiring less current. The ±5V supplies are directly derived from a 5.1V device. LVA's have been successfully used in the recent TD-206 redesign program.

	Voltage	Current
LSPR	+5.1, -5.1	40 mA
HSPR	+5.1, -5.1	80 mA

12.3.6 FAULT LOCATION CIRCUITS

The fault location circuits use peak detector to monitor the diphase output. This detector controls the transistor switch, shunt resistor combination connected in series with the cable current. As signal levels are relatively low, and

to minimize power consumption, hot carrier diodes will be used in the peak detector circuits. These reduce the voltage drive requirements of the detectors.

12.3.7 LOADING COILS

As stated previously (paragraph 12.2) loading coils are required in each restorer to provide the required orderwire passband characteristics. Inductance values for these coils are:

LSPR - 57.0 mH
HSPR - 14.8 mH

SECTION 13

CABLE ORDERWIRE UNIT (COU)

13.1 DESIGN GOALS AND REQUIREMENTS

The Cable Orderwire Unit (COU) provides voice communication on the high-speed and low-speed cable systems from any junction or Pulse Restorer (PR) to the Cable Driver Modems (CDM's) at each terminal. The COU permits measurements to be made to determine the condition of the PR and cable system. These measurements include the cable dc supply current and voltage, the level of the diphase signals into and out of the PR, and the internal battery voltage. A 4-wire interface with the GM, RMC, RLGM, and RLGMCD is also provided.

The unit is simple, reliable, self contained, and easy to use. The design features:

a. Uniform battery loading so that both batteries are replaced at the same time

b. No switching of the through-coaxial circuit, to avoid discontinuities in the cable system

c. AGC in the voice frequency receive amplifier

d. Push-to-talk (PTT) operation of the orderwire to conserve battery power and eliminate hybrid circuits

e. A combined signaling oscillator and detector

f. A push-off battery switch that automatically disconnects the battery when the cover is closed

g. Storage space for the headset and cables

13.1.1 PERFORMANCE GOALS

Measurements

a.	Internal battery:	yellow zone on meter from full scale (18 V) to 70% of full scale (12.6 V).
b.	Cable voltage:	meter indicates V; 1000 V full scale.
c.	Cable current:	meter indicates milliamperes; 100 mA full scale.
d.	Diphase signal level (input to, and output from restorer):	0.02 V p-p input 2.0 V p-p output meter indicates mid-scale ±10% of full scale for acceptable level (green zone).
e.	Meter accuracy:	±5% @ + 25°C.

Orderwire

a.	Cable impedance (loaded):	430Ω
b.	Transmit level (voice and signaling) on each cable:	+10 dBm
c.	Receive level:	-24 to +26 dbm.
d.	Signaling frequency:	1600 Hz ±32 Hz.
e.	Frequency Response:	±3 dB, 300 to 1700 Hz.

13.1.2 DESIGN APPROACH

Figures 13-1 through 13-5 show how the COU is used. Access to the orderwire is provided at any PR through the COU orderwire cable as shown in Figure 13-1. This connection can be made without disturbing the traffic through the PR, but no metering is possible.

The COU can be connected at a cable junction as shown on Figure 13-2. There is no restorer at this point so the measured signal levels will not be the same as at a PR but the cable supply current measurement and the orderwire are unaffected.

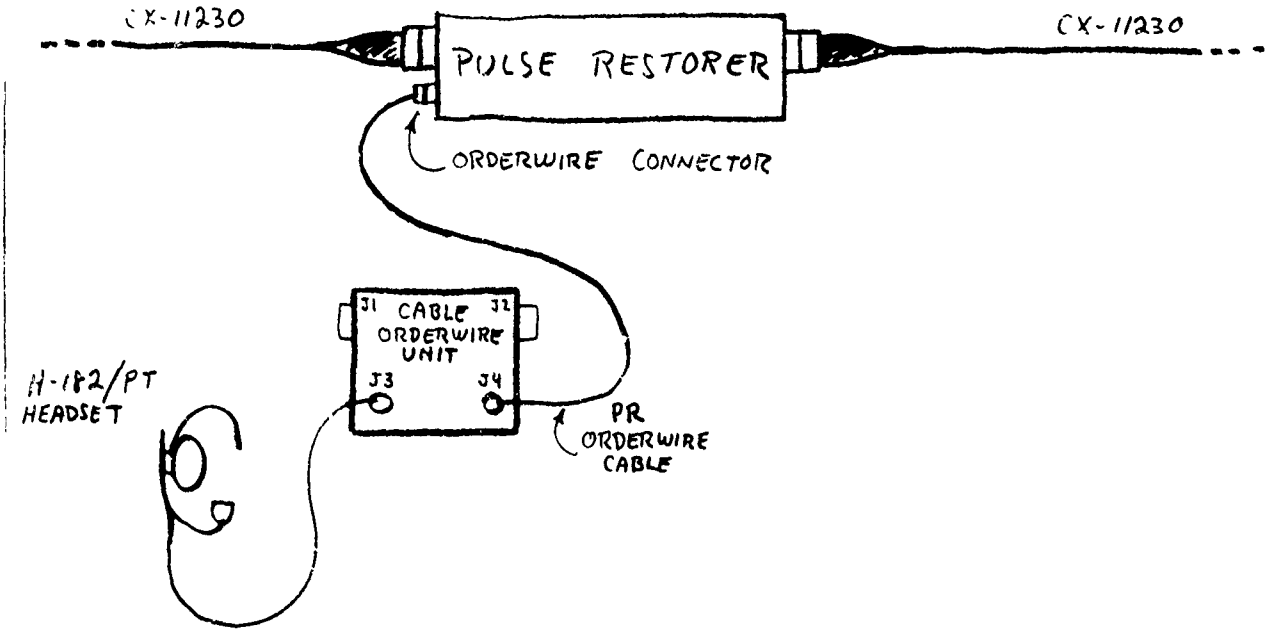


Figure 13-1. Orderwire Connection to an Active Restorer (No Metering)

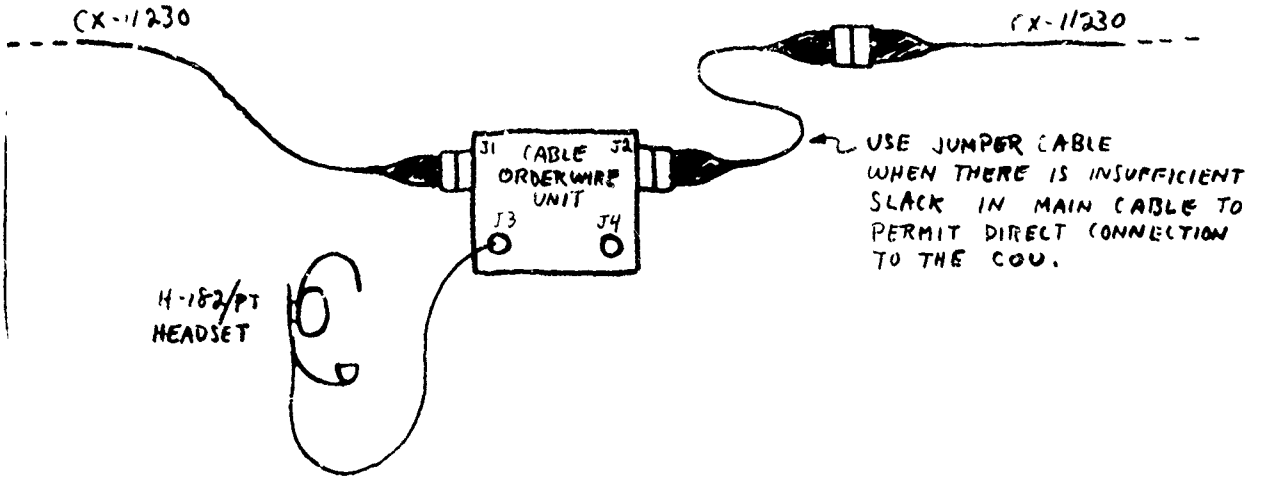


Figure 13-2. Connection at a Cable Junction (Orderwire and Metering)

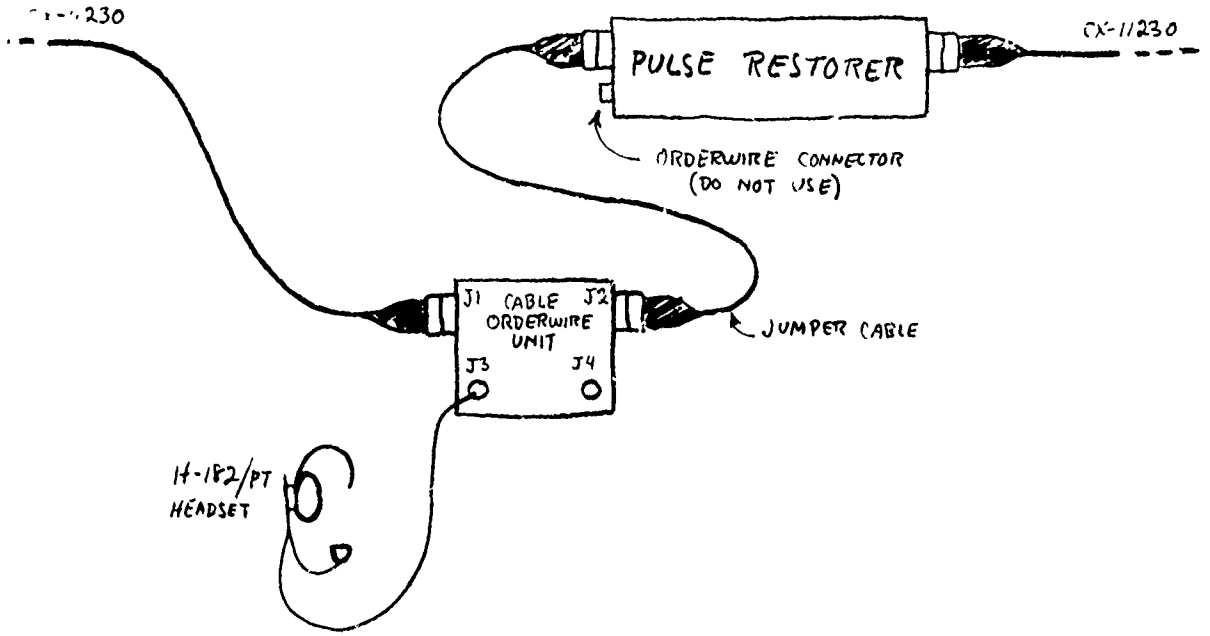


Figure 13-3. Connection to West Side of Restorer (Orderwire and Metering)

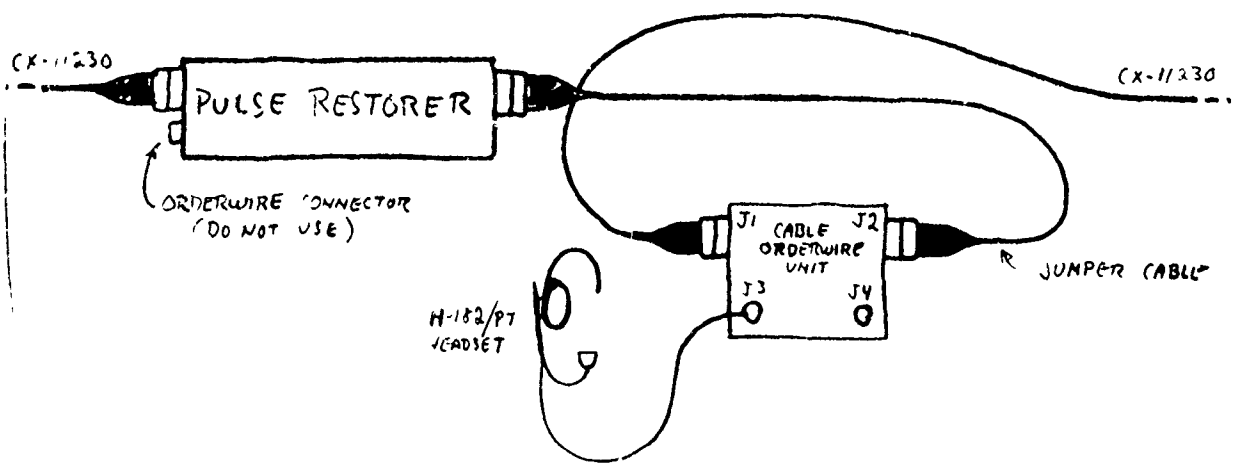


Figure 13-4. Connection to East Side of Restorer (Orderwire and Metering)

Figures 13-3 and 13-4 show the connections at a PR. The cable circuit must be broken to make this connection, which normally would be made only on a faulty system, and after the cable power supply had been shut off. The orderwire and full metering facilities are available to check the condition of the PR. The signal levels to and from the PR on each side ("west" and "east") are measured by making the connections as shown.

The COU is connected to the GM, RMC, RLGM, and RLGMCD through a special cable as shown on Figure 13-5.

Figure 13-6 shows the front panel layout.

13.1.3 DESIGN DESCRIPTION

A simplified schematic of the COU is shown on Figure 13-7. In this example, the COU is connected to the "West" side of the PR. Incoming signals from the west pass through J1 to J6 which connects to the metering printed wiring board (PWB). High frequency diphase signals are coupled through C1 to J2 where they are connected to the Pulse Restorer via a jumper cable. The dc cable current flows through rf chokes L1 through L4 and resistor R4. The dc voltage developed across R4 is used to measure the cable current with meter M1. Resistors R3, R4 and R5 are selected for a full scale meter reading of 100 mA, so that the value of cable current (45 mA for the low speed system and 60 mA for the high speed system) is read directly. Bypass capacitors C3 and C4 keep rf out of the meter circuit. Resistors R6 through R9 provide a full scale voltage reading of 1000 volts on the meter. R23 gives a full scale reading of 18 V for monitoring the battery supply.

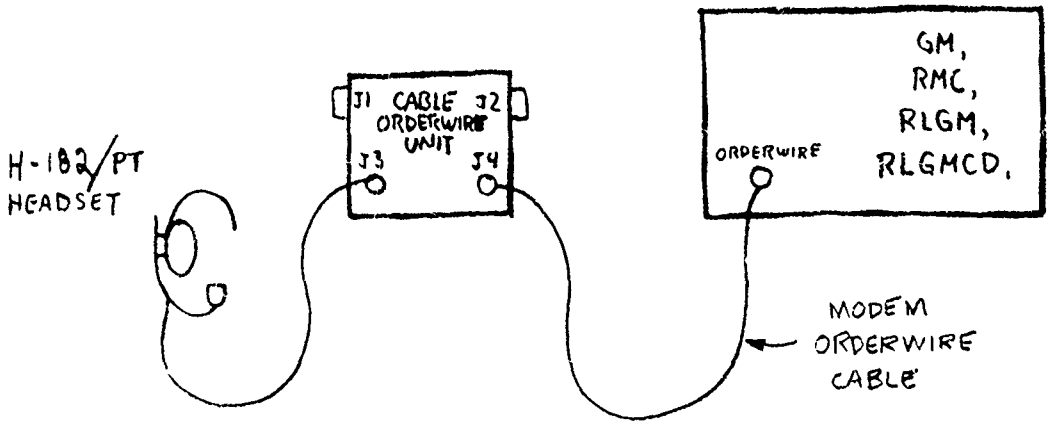


Figure 13-5. Orderwire Connection to DGM Modems

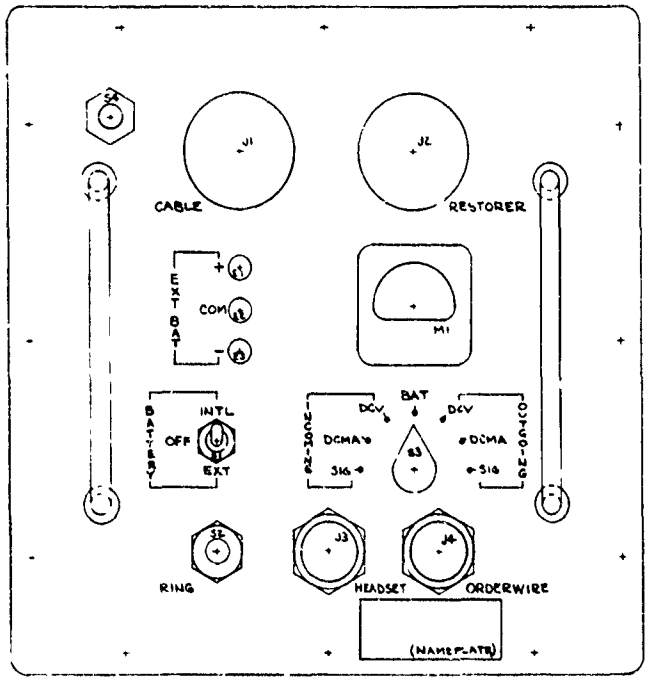


Figure 13-6. Front Panel Cable Orderwire Unit

A sample of the high frequency diphase signal is coupled to an Incoming Signal Detector through C2. This detector consists of an input bandpass filter, a broadband amplifier and a rectifier. A normal input signal produces a reading in the "green zone" on the meter.

Low frequency signals pass through chokes L1 and L2 to a high voltage blocking capacitor C17 and a relay K1. When K1 is in the receive/standby position (de-energized, as shown) the low frequency signals are connected to the Receive Amplifier U2A via R22.

The Receive Amplifier includes automatic gain control to compensate for wide variations in input level. The Receive Amplifier drives the earphone in the H-182/PT headset, and its output is also connected to a Signaling Detector U2B, U3 and Q7 through contacts on relay K2. The signaling detector responds to a 1600 Hz signaling tone (but not to voice) to energize a buzzer DS-1.

To transmit a signaling tone, the operator presses the RING switch S2 on the front panel. This energizes relay K2 to switch the U3 circuit from detector to oscillator, the output of which goes to Transmit Amplifier U1, Q1 through Q4.

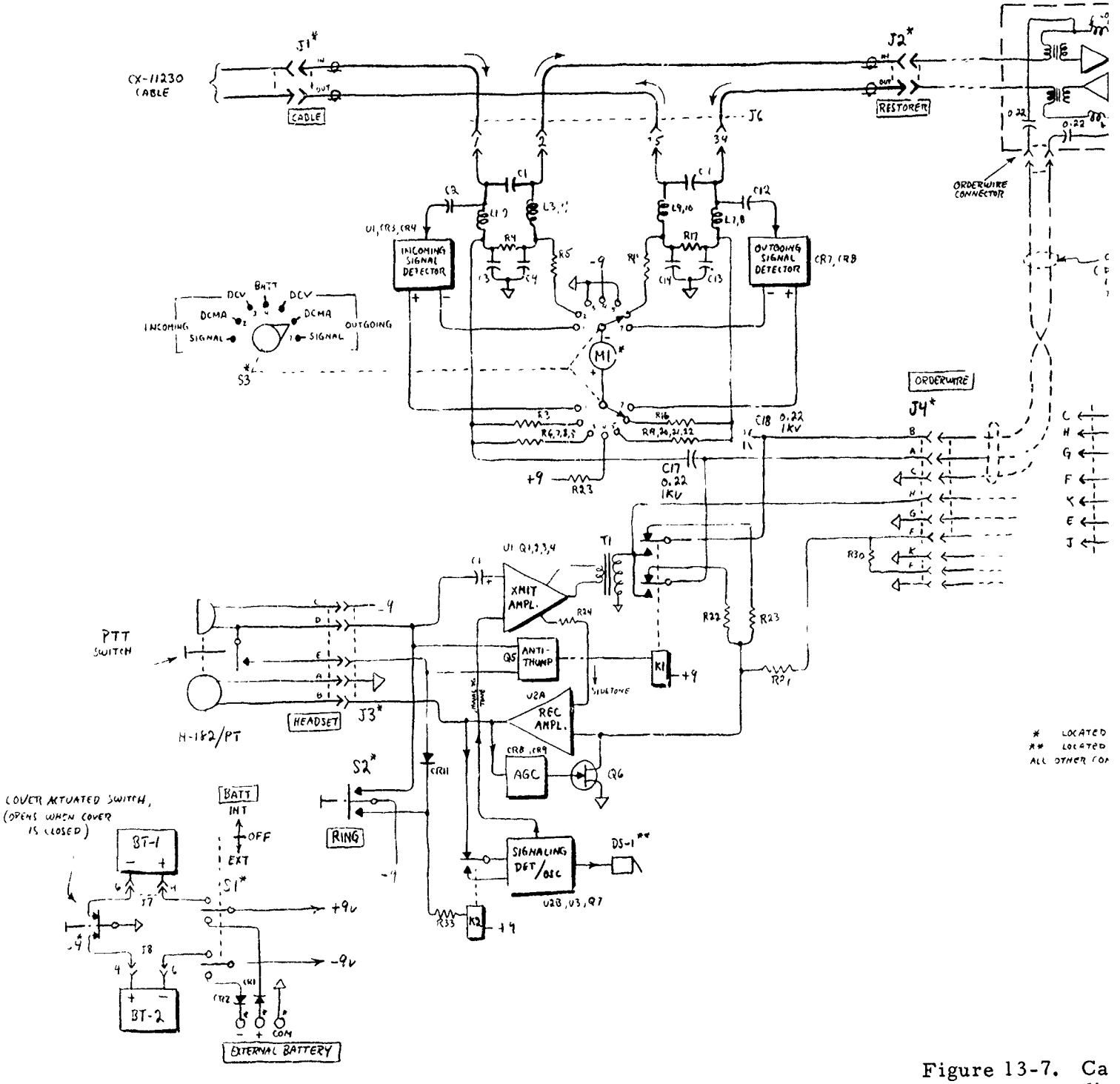


Figure 13-7. Ca
Sir

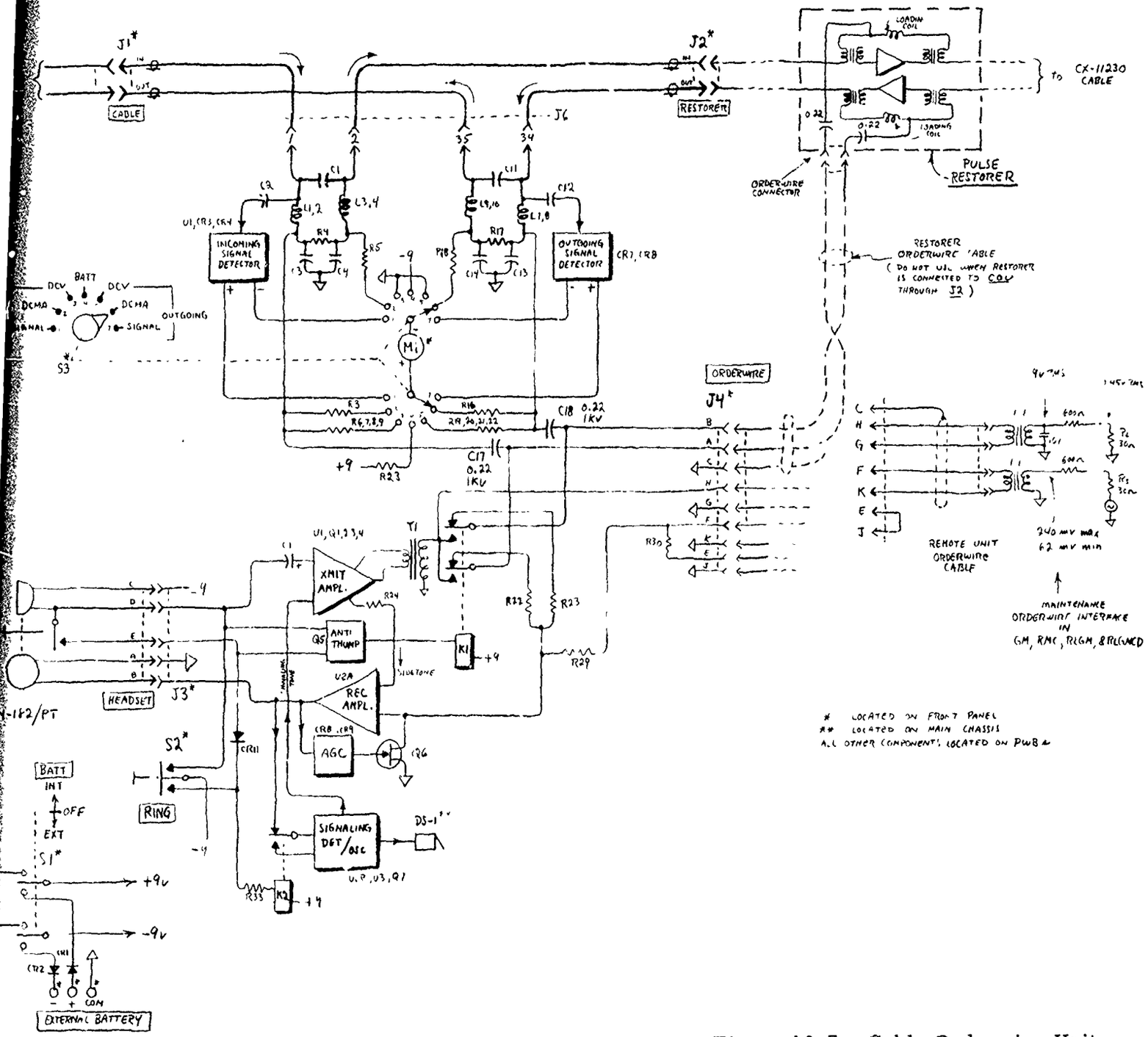


Figure 13-7. Cable Orderwire Unit Simplified Schematic

2

S2 also energizes relay K1 to transfer the cable circuit from the receive Amplifier to the Transmit Amplifier which drives both cables simultaneously in both directions.

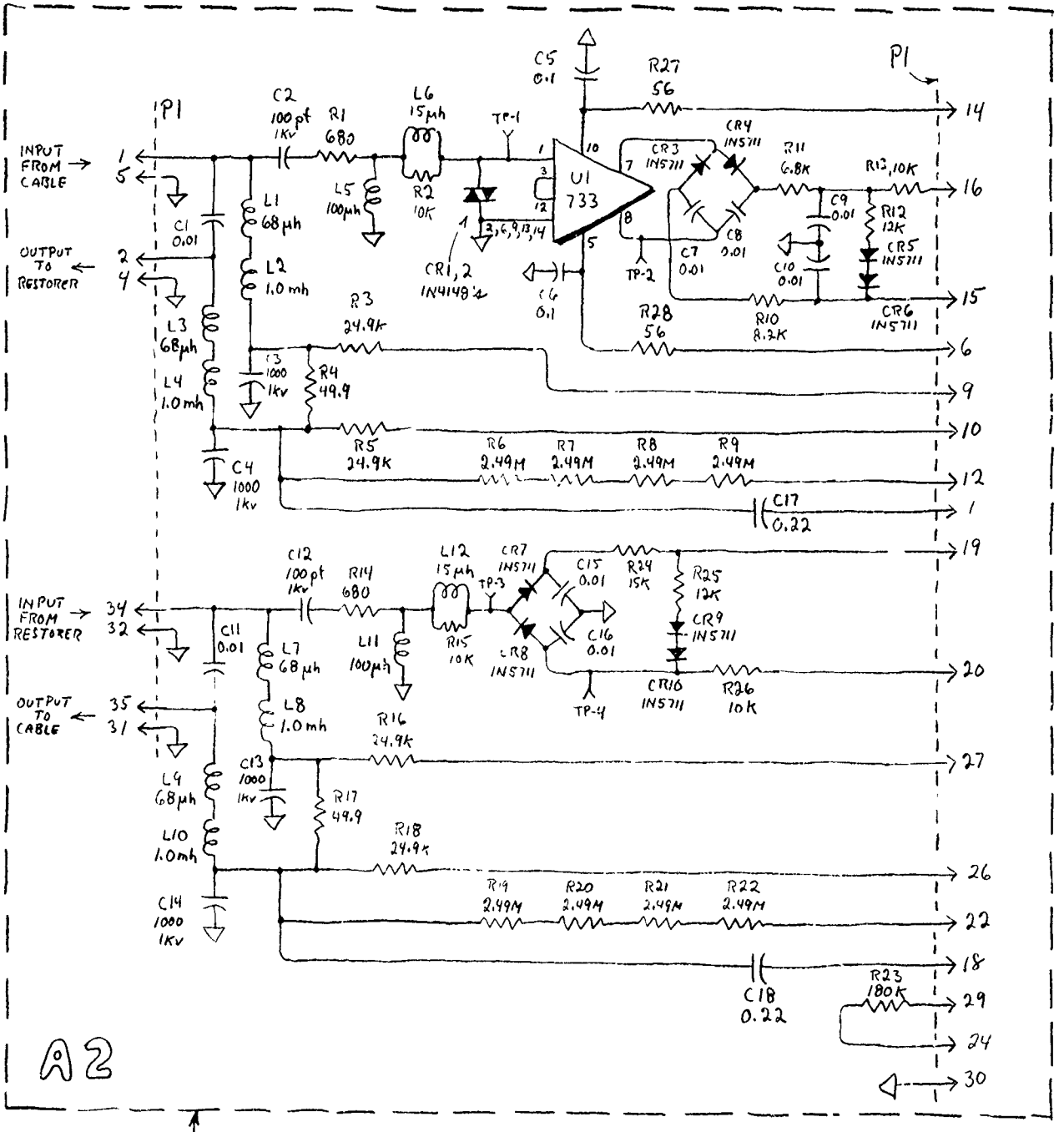
When talking on the orderwire, the operator pushes the Push-to-Talk (PTT) switch on the H-182/PT headset. This energizes K1 and the carbon microphone to provide talking power and to transfer the cables to the Transmitter Amplifier output. Sidetone is provided through R24.

The outgoing cable from the PR is connected to the COU circuits in a manner similar to the incoming cable. High frequency outgoing signals pass through C11. C12 couples a sample of these signals to the Outgoing Signal Detector CR7, CR8 which performs the same functions as the Incoming Signal Detector except that no amplification is needed. L6 and L7 pass dc and low frequency signals to the metering circuits and orderwire.

13.1.4 DETAILED DESIGN DESCRIPTION

Referring to Figure 13-8 (the Metering Card Schematic), the incoming Diphase Signal Detector comprises a broadband video amplifier U1 and associated components. High voltage coupling capacitor C2 and inductor L5 form a high pass filter that has a response peak at the low speed diphase rate. Inductor L6 and the shunt capacitance of CR1, 2 and U1 comprise a low pass filter with a response peak at the high speed diphase rate. This results in a bandpass characteristic that separates the diphase signals from the orderwire. A voltage gain of 100 in U1 increases the 20 millivolt peak-to-peak input signal to 2 volts to drive a voltage doubler rectifier CR3, CR4, C7, C8. Hot carrier diodes are used here to maximize the dc output voltage. R10, 11, and 13 are the meter multiplier resistors that set the meter reading to mid scale (green zone) for a normal signal level. Diodes CR1 and CR2 protect the input of U1 from damage caused by transients on the cable.

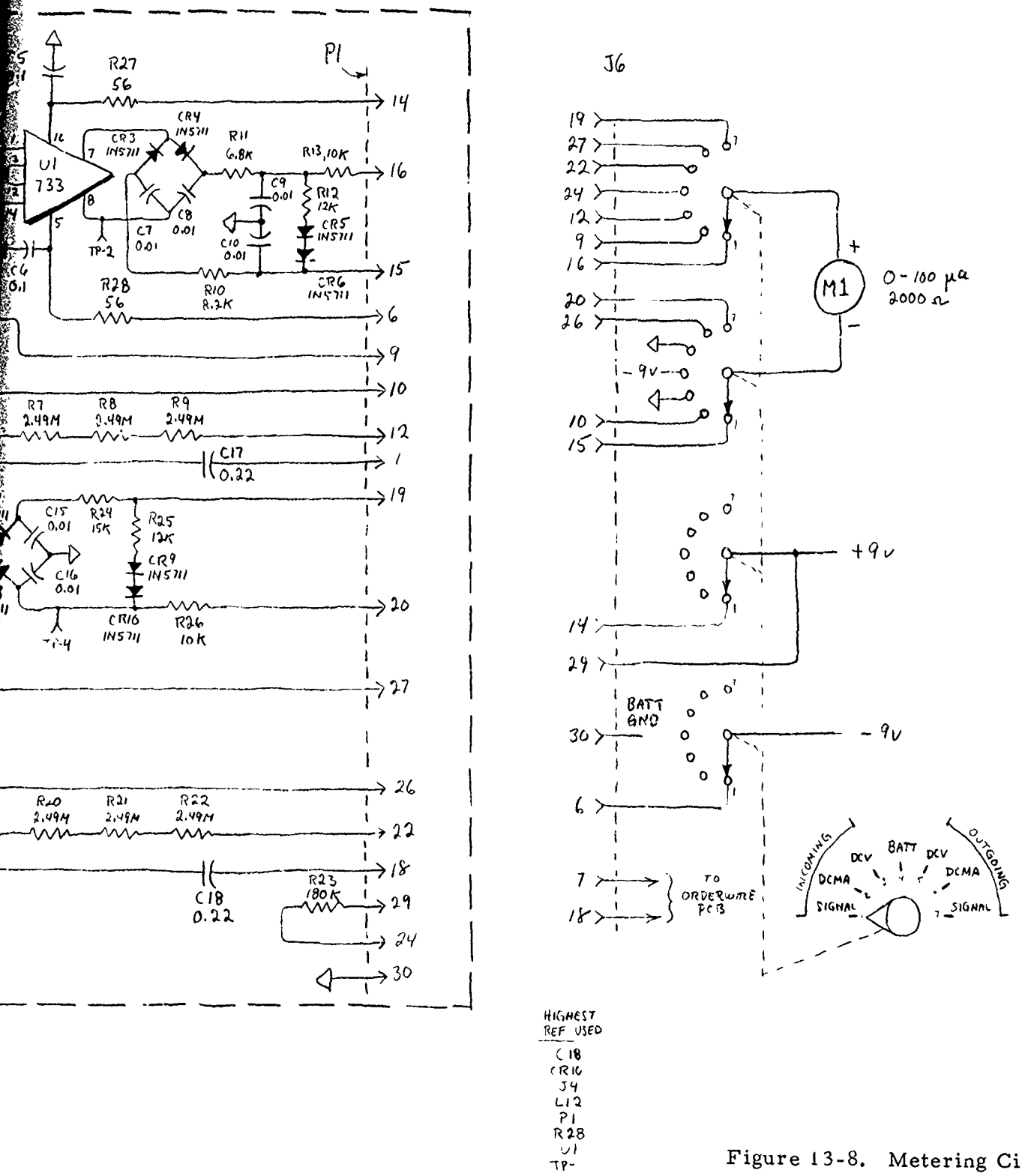
The Outgoing Diphase Signal Detector (see circuit between C12 and R26 on the schematic) is essentially the same as the incoming detector but without the amplifier.



SCHEMATIC ASS'Y 876114 876005

HIGHEST REF USED

C18
CR10
J4
L12
P1
R28
U1
TP-



HIGHEST REF USED
C18
CR10
J4
L12
P1
R28
U1
TP-

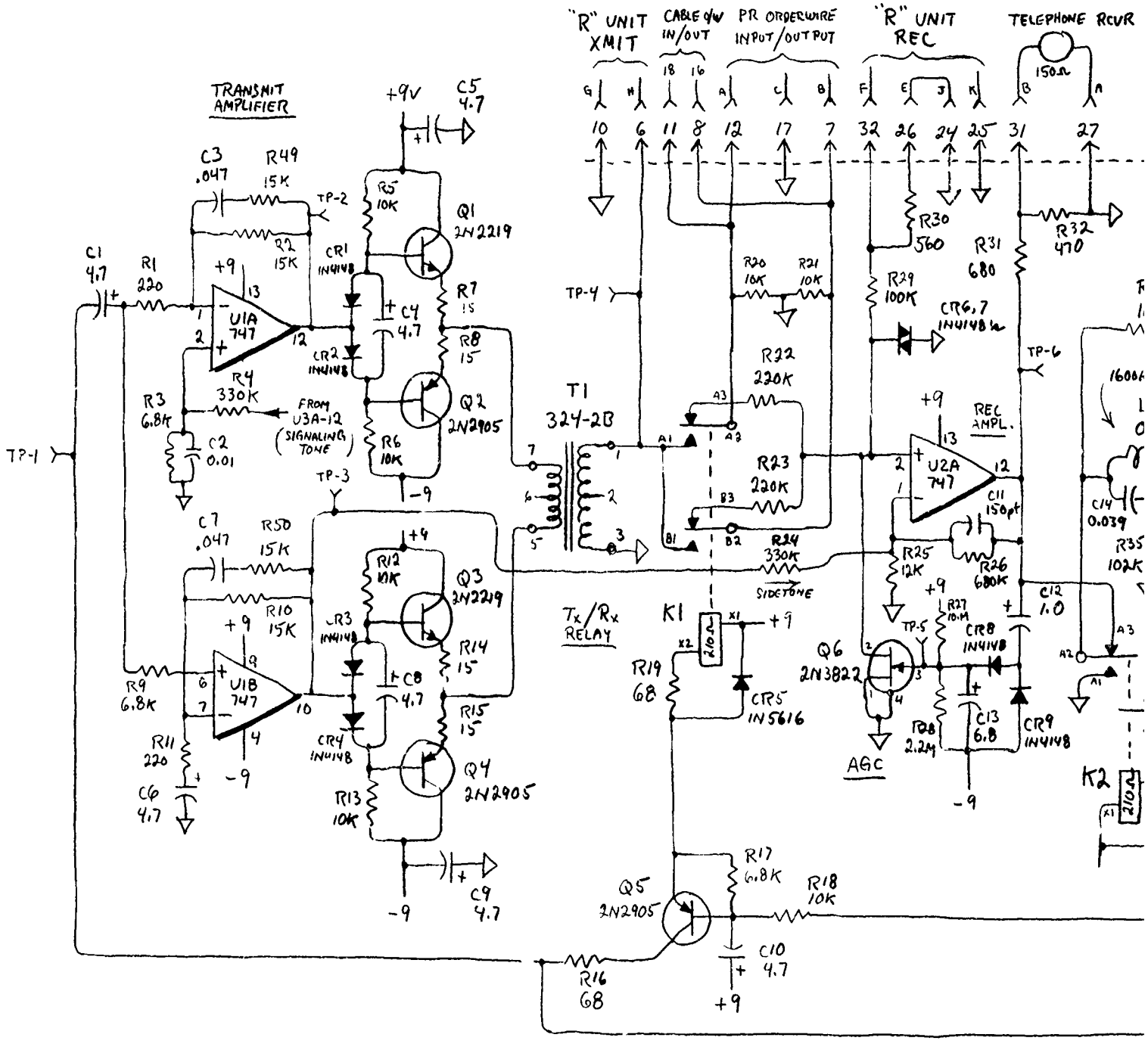
Figure 13-8. Metering Circuit Card Assembly Schematic

Figure 13-9 is the schematic of the Orderwire Card. The Transmit amplifier U1, Q1, 2, 3 and 4 is a high output impedance bridge amplifier. The Receive amplifier U2A uses an FET as the variable element in a voltage controlled attenuator. The output of U2A is rectified in a voltage doubler to produce the control voltage for the FET which makes up the automatic gain control circuit. The Receive Amplifier drives the telephone headset earphone and the Signaling Detector.

The Signaling Detector consists of a Bridged-T null network L1, C14, C15 and R35 and two operational amplifiers, U3A and U3B. At frequencies other than the 1600 Hz resonant frequency of the Bridged-T the signal voltage applied to both inputs of U3A is the same in phase and amplitude, so the output is nearly zero. U3B, however, will amplify the output of the Bridged-T; CR12 rectifies this output and the resulting positive dc is applied to the inverting input of U2B. The output of U2B will be negative under these conditions to cut off Q7 and de-energize the buzzer. When a 1600 Hz signaling tone is received, the output of the Bridged-T goes to zero (or nearly so) and no signal appears at the non-inverting inputs to U3A and U3B. The inverting input of U3A does have a signal applied however, which is amplified and then rectified to supply a positive dc to the noninverting input of U2B to switch positive to turn on Q7 and energize the buzzer. Voice signals will not operate the buzzer because, even though there may be 1600 Hz components in the voice frequency spectrum tending to turn the buzzer on, the greater amount of energy in the spectrum that is amplified by U3B will turn U2B off to prevent it.

The Signaling Detector is converted to a Signaling Oscillator when relay K2 is actuated. The junction of L1 and C14 is grounded and the output of U3A is fed back to C14, C15 through R34 to form a Colpitts oscillator, the output of which is connected to the Transmit Amplifier through R4.

The COU Control Panel schematic is shown on Figure 13-10. Two 9 volt BA-5599 batteries supply dc power. A switch S1 selects the internal battery or an external supply, or shuts the unit off. A cover actuated switch S4 disconnects the batteries when the cover is closed.


TRANSMIT AMPLIFIER
"R" UNIT XMIT
CABLE q/w IN/OUT
PR ORDERWIRE INPUT/OUTPUT
"R" UNIT REC
TELEPHONE RCVR
+9V
C5 4.7
C3 .047
R49 15K
R2 15K
TP-2
C1 4.7
R1 220
U1A 747
R4 330K
R3 6.8K
C2 0.01
TP-1
FROM U3A-12 (SIGNALING TONE)
CR1 IN4148
CR2 IN4148
C4 4.7
R5 10K
Q1 2N2219
R7 15
R8 15
Q2 2N2905
R6 10K
-9
TP-3
T1 324-2B
C7 .047
R50 15K
R10 15K
U1B 747
R9 6.8K
R11 220
C6 4.7
R12 10K
Q3 2N2219
CR3 IN4148
R14 15
C8 4.7
CR4 IN4148
R15 15
Q4 2N2905
R13 10K
C9 4.7
Tx/Rx RELAY
K1
R19 68
CR5 IN5616
Q5 2N2905
R17 6.8K
R18 10K
C10 4.7
R16 68
TP-4
R20 10K
R21 10K
R22 220K
R23 220K
R24 330K
SIDETONE
R30 560
R31 680
R32 470
R29 100K
CR6,7 IN4148
TP-6
REC AMPL.
U2A 747
C11 150pf
R25 12K
R26 680K
C12 1.0
R27 10.M
TP-5
Q6 2N3822
AGC
CR8 IN4148
R28 2.2M
C13 6.8
CR9 IN4148
150Ω
K2
10 6 11 8 12 17 7 32 26 24 25 31 27
G H 18 16 A C B F E J K B A

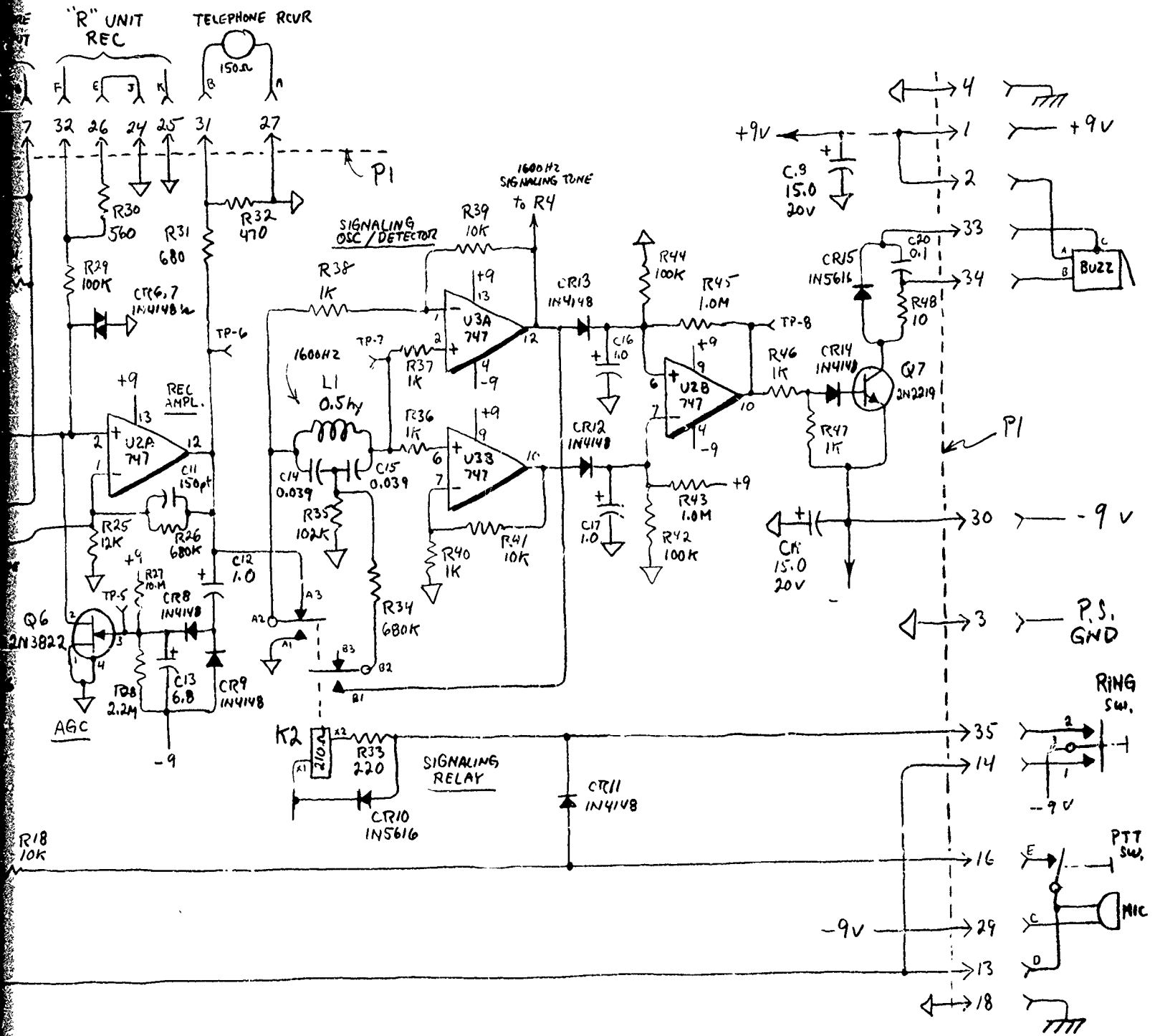
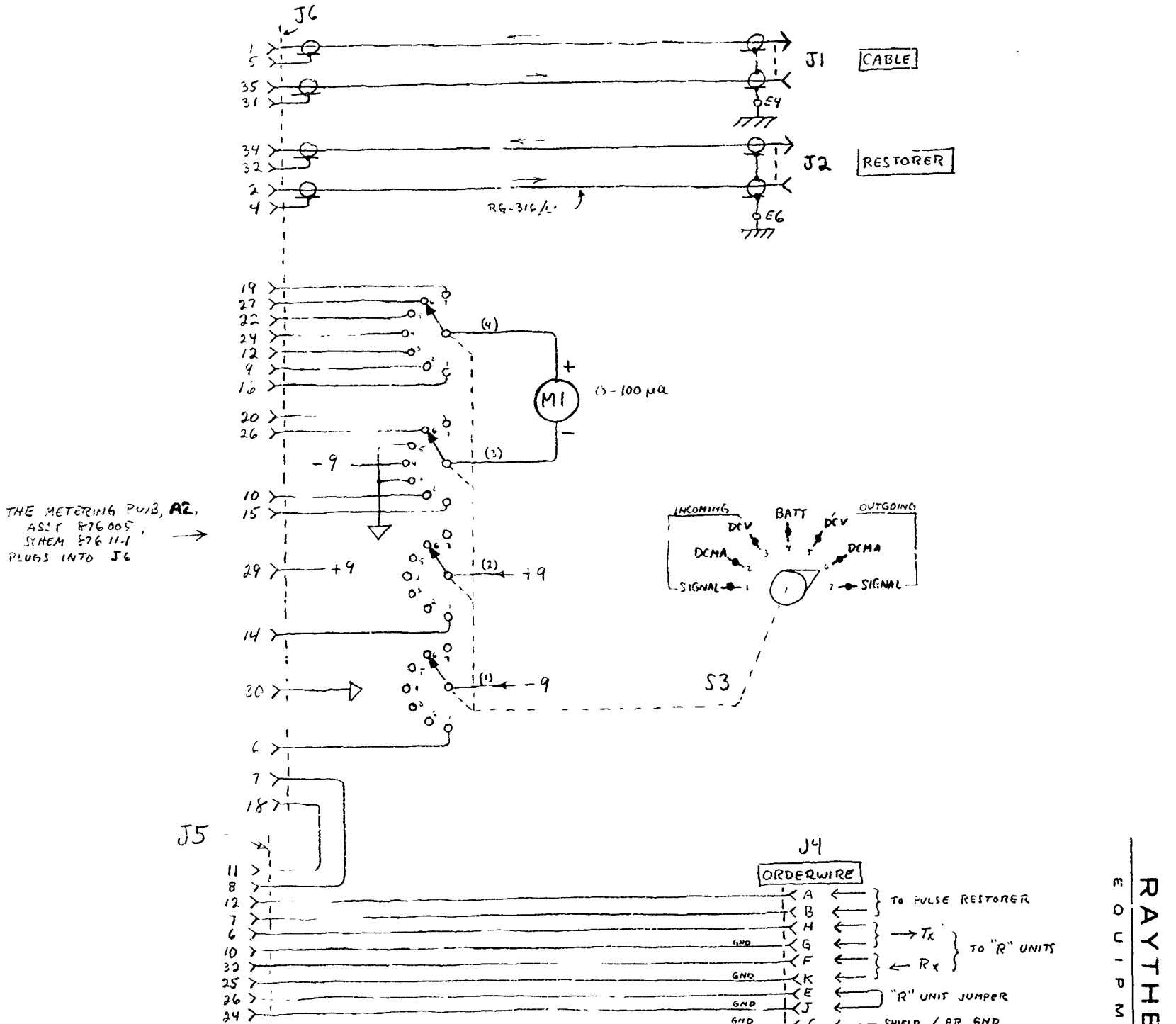


Figure 13-9. Orderwire Circuit Card Assembly Schematic



RAYTHEON EQUIPMENT

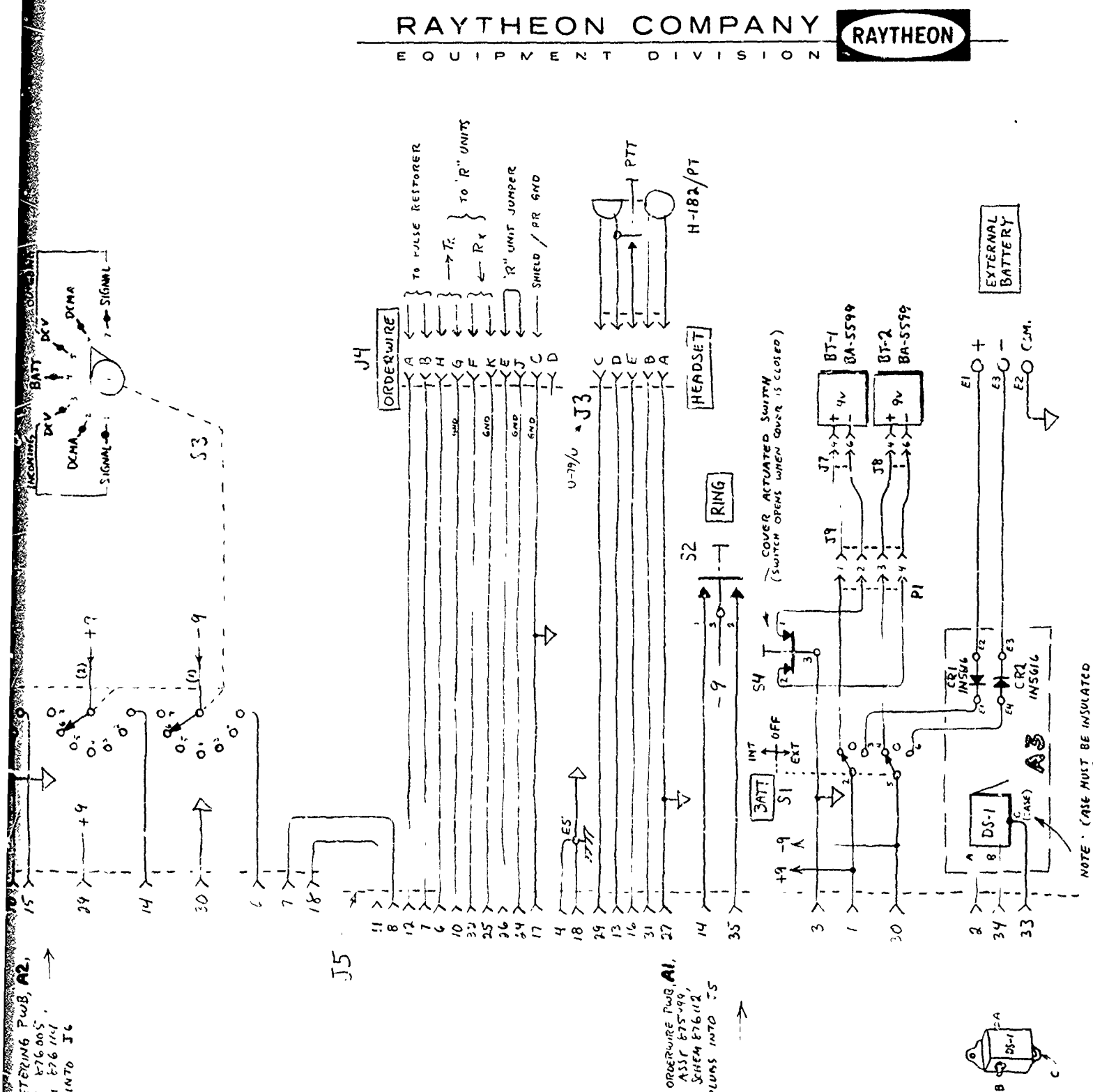


Figure 13-10. COU Control Panel Schematic

SECTION 14

POWER SUPPLIES

14.1 DESCRIPTION

Each equipment has its own plug-in power supply to generate all of the dc voltages required for operation. Switching regulators are required to meet size and weight requirements and to improve electrical efficiency. Keltec Florida, a division of Aiken Industries was the successful bidder for the power supply subcontract. Keltec has designed and built power supplies for the DVM and EDM units. The power supplies plug in from the front and the heatsink extends out the rear of each DGM equipment except the RLGM which does not require heatsinking to the outside.

All power supply outputs are protected against short circuits and overvoltage. The constant current power supplies for the CDM's and the 180 volt RLGM power feed supply has shut down and discharged the cable voltage upon interruption of cable current. Isolation has been provided between DSVT power feed circuits so that they can be switched ON or OFF separately and a short on one line has not caused shut down of the other power feeds. The 180 volt RLGM power feed is designed to shut down when short circuited and to periodically try to restart.

14.2 DESIGN APPROACH

Figure 14-1 shows the functional elements required to configure all of the DGM equipment power supplies. Each of the DGM equipments was designed to operate from either 120 Vac or 28 Vdc power. The RLGM was also designed to operate from 180 Vdc. The 28 Vdc requirement was subsequently deleted, except for the RMC, RLGM, and LSCDM. Each equipment also requires ± 5 and ± 12 or ± 10 Vdc outputs.

The LGM, RLGM and RMC power supplies provide 55 volts power feed to DSVT's. Power feed to the high and low speed pulse restoreres is generated by a constant current regulator in the CDM power supplies.

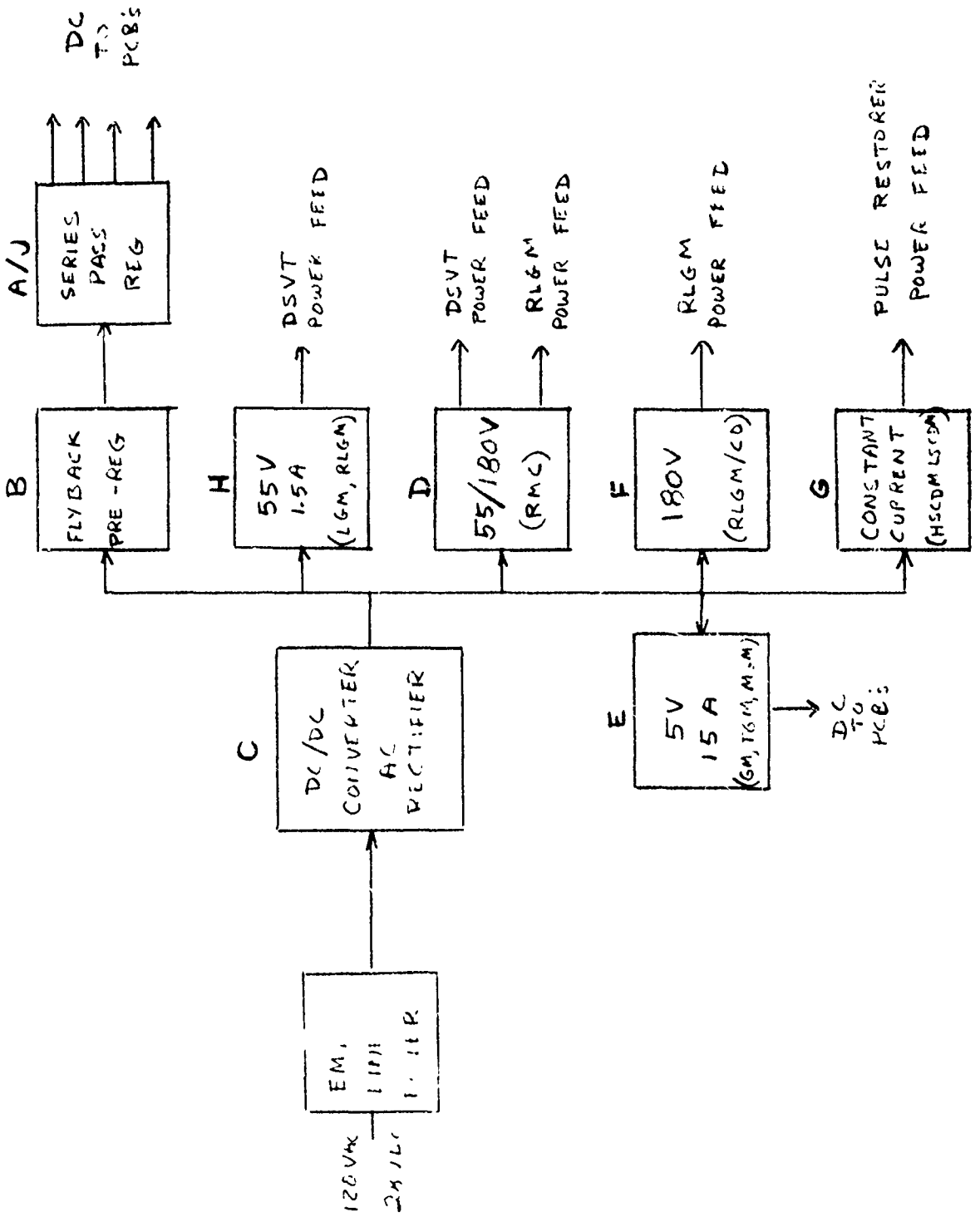


Figure 14-1. Power Supply, Functional Element

The power line is protected by a circuit breaker with separate sensing of ac or dc overload current. The RMC and RLGM power supplies have integral EMI filters and EMP protection. Each power supply contains four or more printed circuit board modules. These modules have a metal heatsink bracket for mounting high power dissipation devices. The heatsink bracket on the module is fastened to the rear heatsink of the power supply by hardware to ensure good heat transfer. Table 14-1 lists the modules used in each DGM power supply.

14.2.1 DC TO DC CONVERTER (MODULE C) (Figure 14-2)

This module is used in all DGM equipment power supplies for operation from 28 Vdc. Automatic switch over to the dc to dc converter occurs when a dc input is sensed. The converter steps up the input voltage to approximately 150 volts. In the ac mode of operation, this 150 Vdc is obtained by rectifying the ac input voltage.

The C module also contains the drivers for the POWER OUT OF TOLERANCE lamp, a fault signal to the equipment BITE card, and the SA alarm relay. A radiation detector on this module shuts down the power supply on detecting a nuclear event.

The power transformer output is rectified by a bridge rectifier circuit. This is the same bridge rectifier circuit that handles the 120 Vac input.

This module also has a nuclear detection circuit that senses electromagnetic pulses (EMP) and shuts down all circuitry in the event of an extreme EMP condition. Module C also senses undervoltages in the +150 Vdc circuits. When an unvervoltage condition is detected, the POWER OUT TOL lamp on the front panel is illuminated.

Tests indicate that the dc to dc converter is at least 85 percent efficient. The overall efficiency of the power supplies is less with a 28 Vdc input because of the losses in the dc to dc converter. EMI tests have shown that power line conduction limits are met in either the ac or dc mode. Tests were made with power line filters from two vendors.

TABLE 14-1

POWER SUPPLY USAGE

Keltec	LGM	RLGM	RMC	TGM/GM	CDM	RLGMCD	MGM
	Sylvania			Raytheon			
Module	-1	-3	-4	-1	-2	-3	-4
A	X			X	X	X	X
B	X	X	X	X	X	X	X
C	X	X	X	X	X	X	X
D			X				
E				X			X
F						X (2 Req)	
G					X		
H	X	X					
J		X	X				
K				X			X
Quant. EDM	36	18	16	79	114	38	37

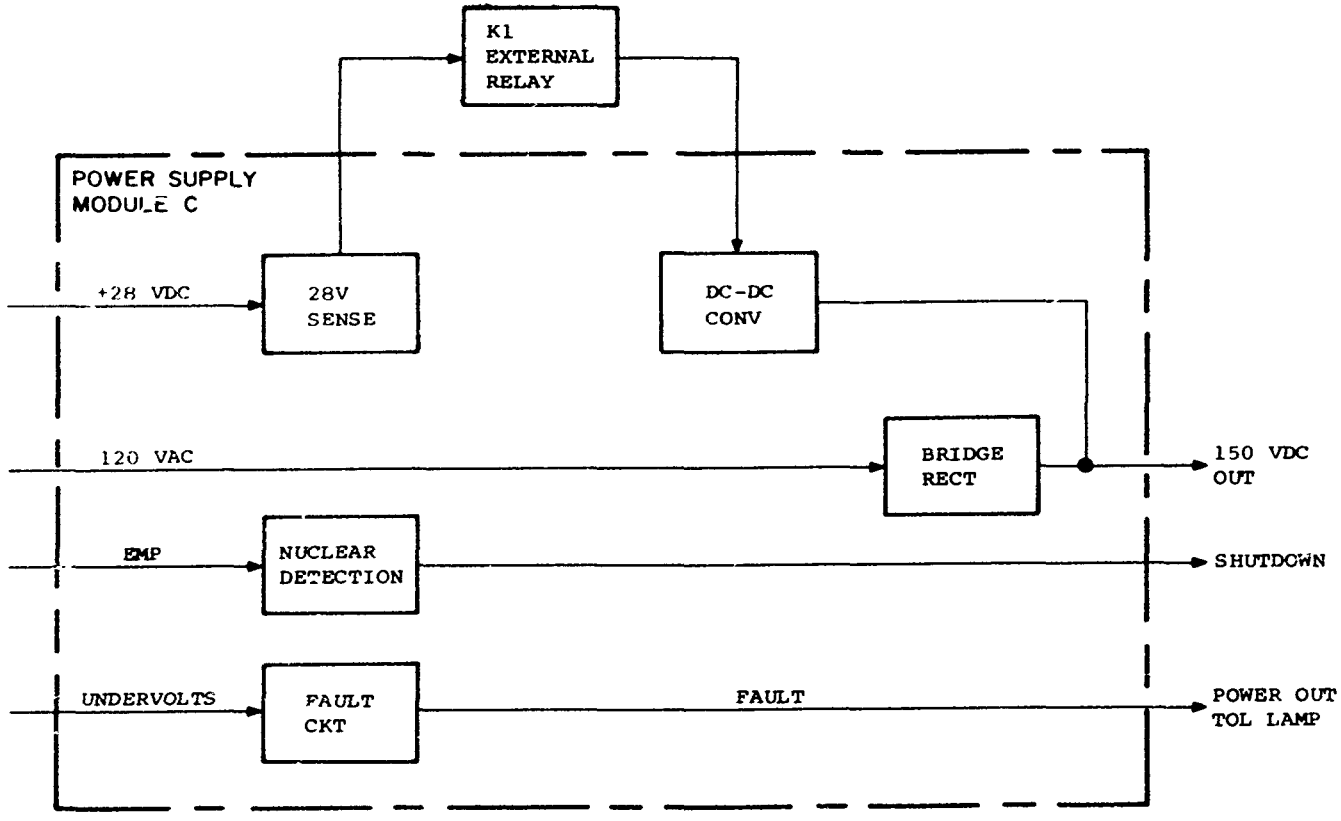


Figure 14-2. Power Supply Module C, dc-dc Radiation Detection, Block Diagram

14.2.2 POWER SUPPLY MODULE B, INTERNAL DC SUPPLY (Figure 14-3)

This module accepts the 150 VDC from module C. The inputs are fed to transformers T1 and T3 which operate in the flyback regulator mode (Fig. 14-4). This mode is essentially an energy storage mode. The energy is stored in a transformer primary during the first alternation of a power transistor (ON). The energy is delivered to the load during the next alternation of the power transistor (OFF).

With two interleaved flybacks, one is delivering energy to the load, while the second is storing energy from the DC source. Regulation is achieved by modulation during the ON time of the power transistors (Q5 and Q6).

Polarities of the T2 transformer windings are such that while Q5 is on, Q6 is off. Transistor Q5 is clocked on the off at a 20 KHz rate by oscillator U1. While Q6 is on, current flows from the +150 VDC source through T1, T2, and T3 to the 150 Vdc common return. At the same time, voltage is being induced into the secondary windings of T1. The winding polarities of T1 are such that all the rectifying diodes are reversed biased while Q6 is on. No output voltage is produced during this alternation.

Voltage comparator U3 receives a sample of the unregulated DC output. This is compared with the E REF voltage. The compared sample is sent to U2 which compares this sample with a ramp voltage. The resultant output causes a shut down and HI current signal output to illuminate the POWER OUT TOL on the front panel.

Undervolts and overvolts detection will also inhibit transformers T1, T2, and T3 thereby shutting down the power supply.

14.2.3 POWER SUPPLY MODULE A, $\pm$5, $\pm$10 VDC SUPPLIES (Figure 14-5)

This module accepts unregulated $\pm$8 Vdc and $\pm$16 Vdc inputs from module B and produces regulated $\pm$5 Vdc, and +10 Vdc output voltages. The unregulated inputs are regulated by series pass transistors controlled by sensing amplifiers referenced to E REF. Each output circuit has an overvoltage sensor that triggers a silicon controlled rectifier (SCR) that in turn crowbars the output.

Each output voltage is also monitored by a voltage comparator. The undervoltage output signal of the comparator is sent to the control panel to illuminate the POWER OUT TOL indicator.

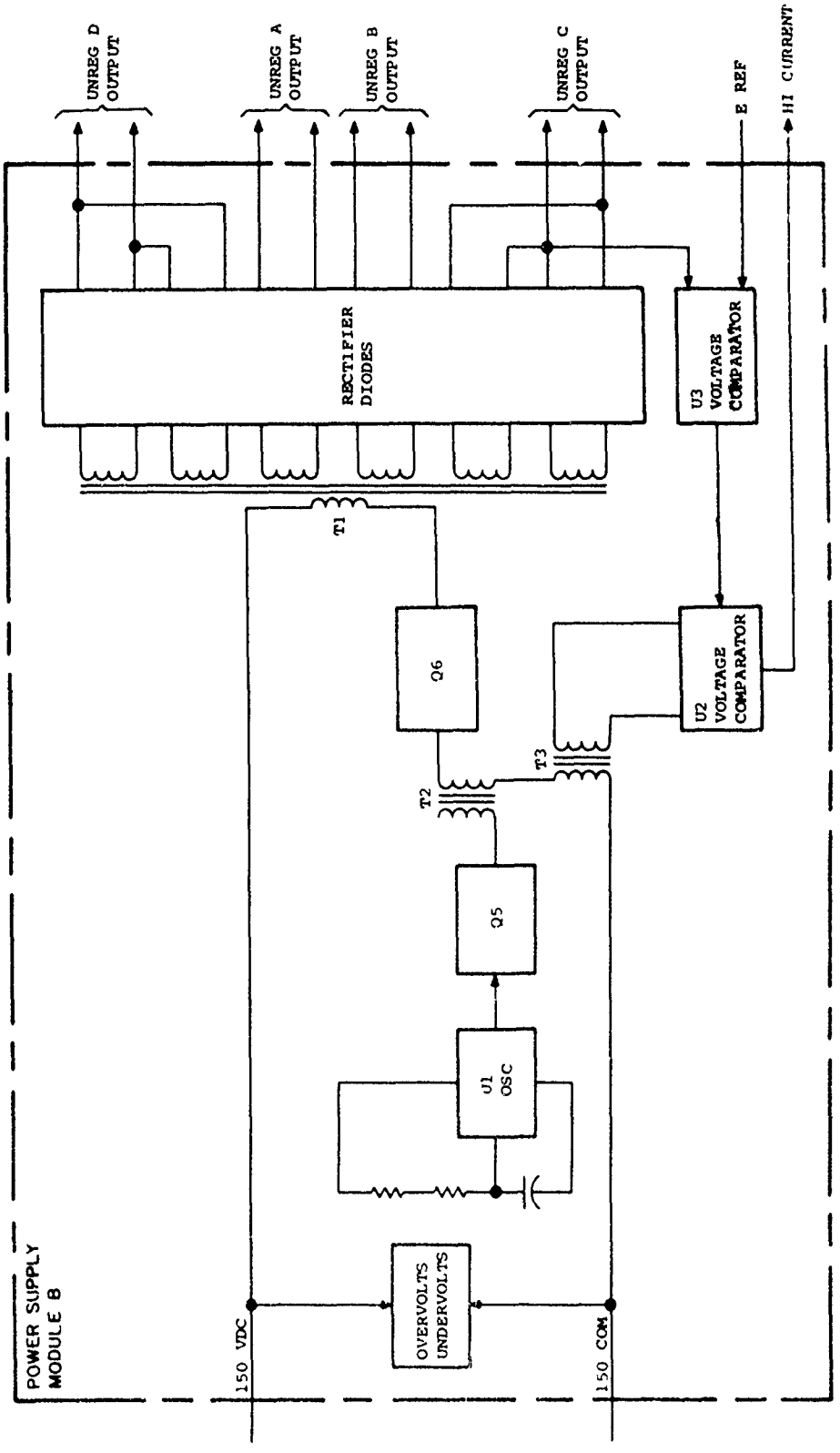


Figure 14-3. Power Supply Module B, Block Diagram

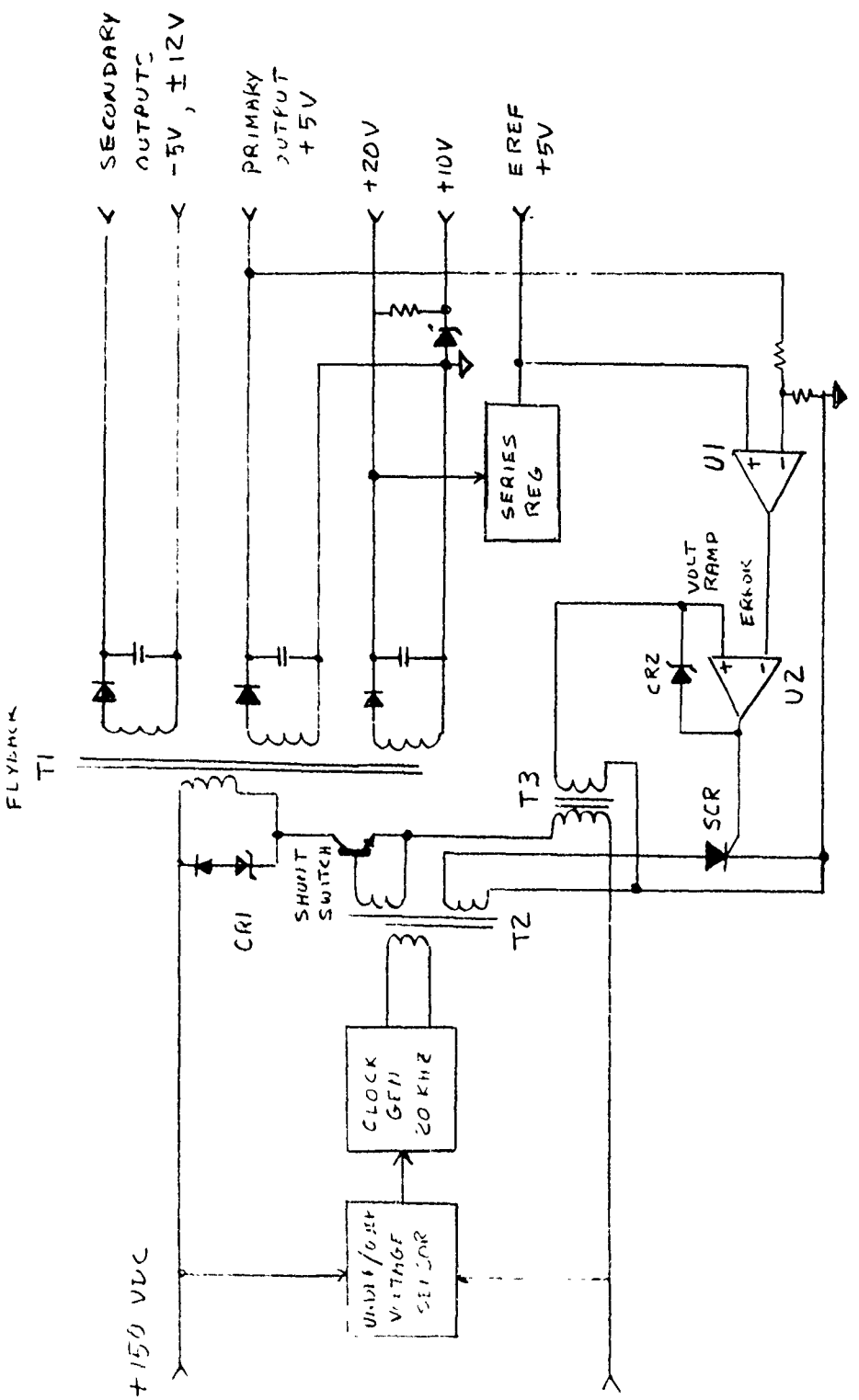


Figure 14-4. Multiple Output Flyback Switching Preregulator

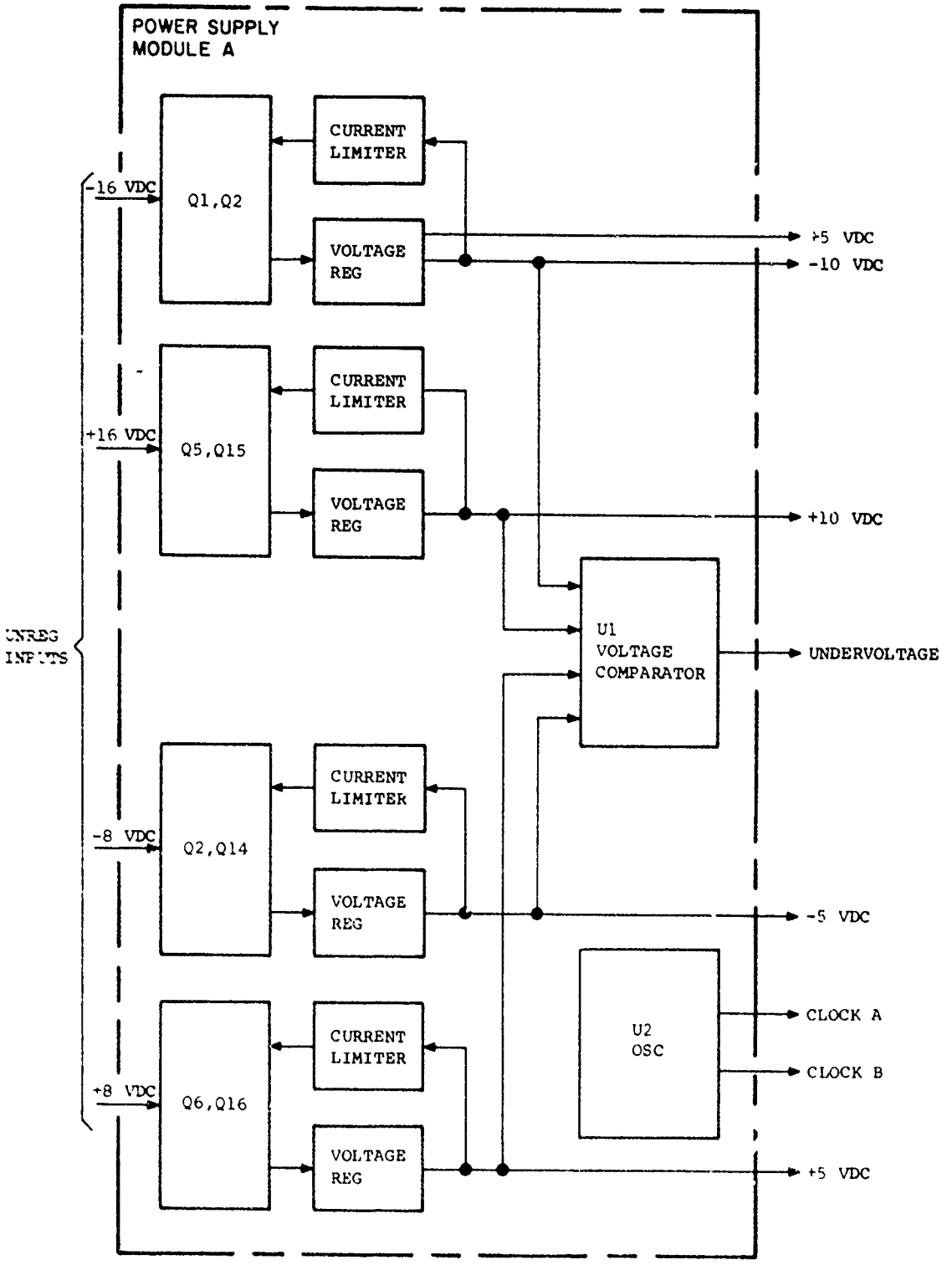


Figure 14-5. Power Supply Module A, Block Diagram

14.2.4 POWER SUPPLY MODULE D, +55, +180 VDC POWER SUPPLY (Figure 14-6)

This module accepts an E REF signal, a 20 Vdc reference signal, and a clock pulse from module B. The 150 Vdc power input is received from module C.

The clock pulse gates Q1 ON and OFF. While Q1 is ON the clock pulse passes through T1 and gates Q3 OFF. The polarities are such that when Q1 is ON, Q3 will always be OFF and vice versa.

While Q3 is ON current from the +150 Vdc input line flowed through T2, Q3, and T3 respectively to the 150 Vdc return line.

The voltage at the +55 Vdc output will not be seen at this time because of the rectifying diode during this clock alternation. However, the field surrounding T2 will build up.

Current flow through T3 induced a positive going ramp to U1 comparator. The second input to U1 comparator comes from a second comparator U2. The two inputs to U2 comparator are the E REF signal and the 55 Vdc output via a voltage adjust potentiometer.

The output of the U1 comparator will fire an SCR thereby shorting the primary of T1 and causing the field to collapse around T1. This action will turn Q3 OFF and it will remain off until the next clock pulse.

With Q3 OFF the field of T2 collapses thereby inducing a voltage that passed through the rectifying diode that is then filtered. This filtered output is the +55 Vdc output via a voltage adjust potentiometer.

A +55 Vdc overvoltage comparator U3 is used with an E REF input to fire an SCR (for cut-off) when the voltage exceeds a limit set by the voltage adjust potentiometer input to the comparator.

A -55 Vdc undervoltage comparator is used in the same manner; the undervoltage uses the U2 comparator to feed an undervoltage driver circuit.

The 180 Vdc power supply operates in a manner similar to the 55 Vdc power supply. Circuitry is provided to give warning when the 180 Vdc source (output voltage) drops below 180 Vdc. When this occurs, Q6 turns on.

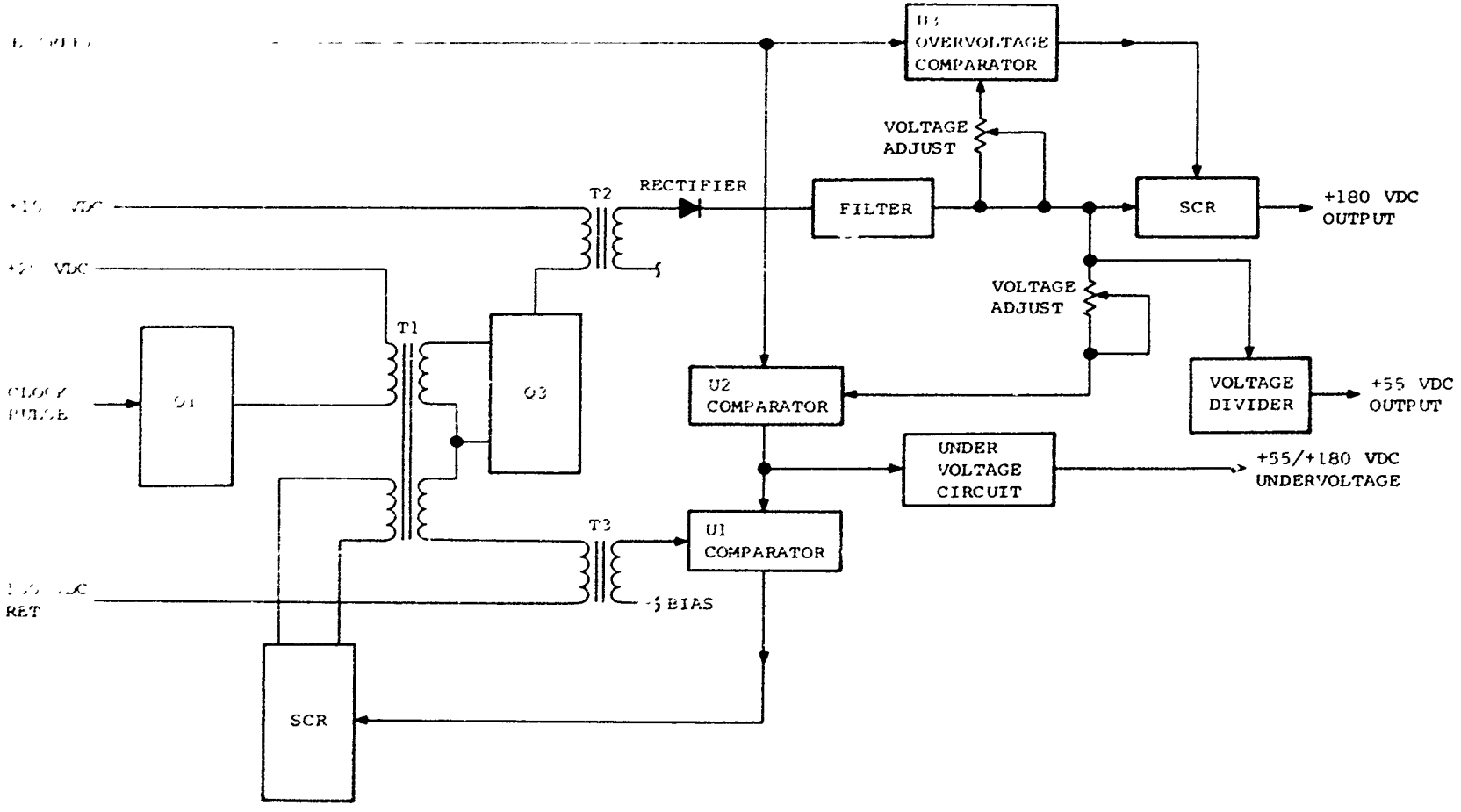


Figure 14-6. Power Supply Module D, Block Diagram

NOTE

When an external short occurs, the 180 Vdc power supply will shut down. After repairing the problem, shut the RMC 180 Vdc power supply OFF then turn it back on to reset internal crowbar circuits.

14.2.5 POWER SUPPLY MODULE F (Figure 14-7)

The two F modules supply 180 Vdc at 300 mA to the remote TD-1233/TTC's. Each module has a separate ON/OFF switch. The voltages from the operating F modules are monitored by the POWER OUT TOL lamp. An open circuit on the 180 V load caused the regulator to inhibit the output and light the 180 V fault lamp. This module is identical to the 180 volt regulator on the D module. Two F modules are used in the RLGM/CD power supply.

14.2.6 POWER SUPPLY MODULE TYPE H DSVT POWER FEED (Figure 14-8)

This module contains a flyback converter for generating +55 Vdc to power the DSVT's. Filtering and voltage protection for this output is also provided. The operation of this module is similar to the type B module. Up to 16 DSVT's can be powered by this module which is used in the LGM and RLGM.

14.2.7 PULSE RESTORER POWER FEED (MODULE G) (Figure 14-9)

This module generates 40 watts of constant current output for powering the HSPR or LSPR. When the power supply is plugged into a LSCDM the constant current is regulated at 40 milliamperes. In an HSCDM the same module is strapped to regulate at 90 milliamperes. The regulator shuts off and the load capacitance is discharged if the output voltage exceeds 1000 volts due to an open cable or a power supply malfunction. A separate ON/OFF switch and fault lamp is provided for the constant current into a load which varies 40 to 1 depending on cable system length. The duty cycle of the flyback switch only varies with the square of the output power rather than linearly as with most switching regulators. Therefore, a 40 to 1 load change requires less than a 7 to 1 change in switching regulator duty cycle.

Module G accepts +150 Vdc and +20 Vdc inputs through the flyback converter-regulator principle is explained in paragraph 14.2.2 (Module B). A clock input is used to set up the timing for the flyback circuit.

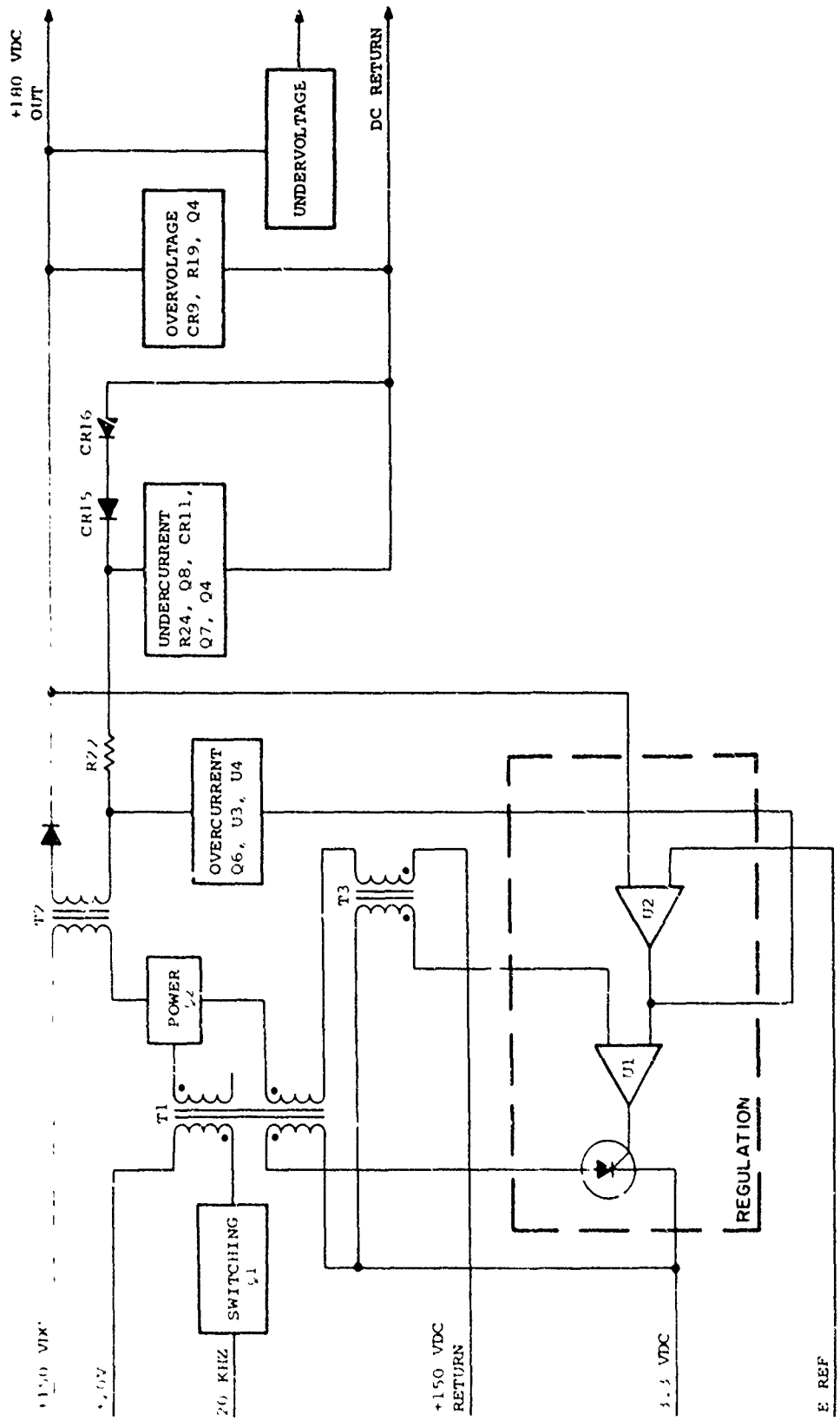


Figure 14-7. Power Supply Module F, Block Diagram

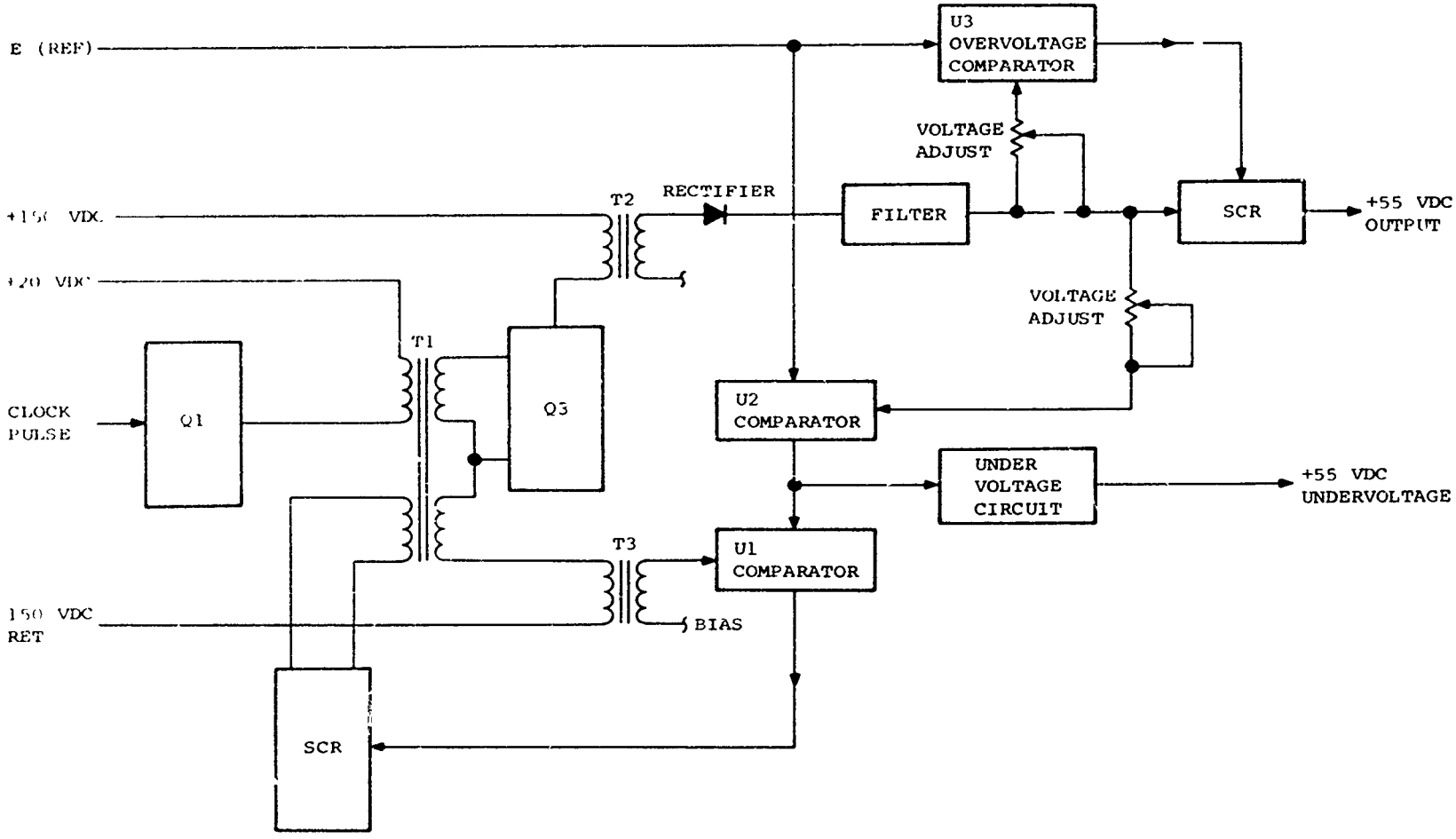


Figure 14-8. Power Supply Module Type H DSVT Power Feed

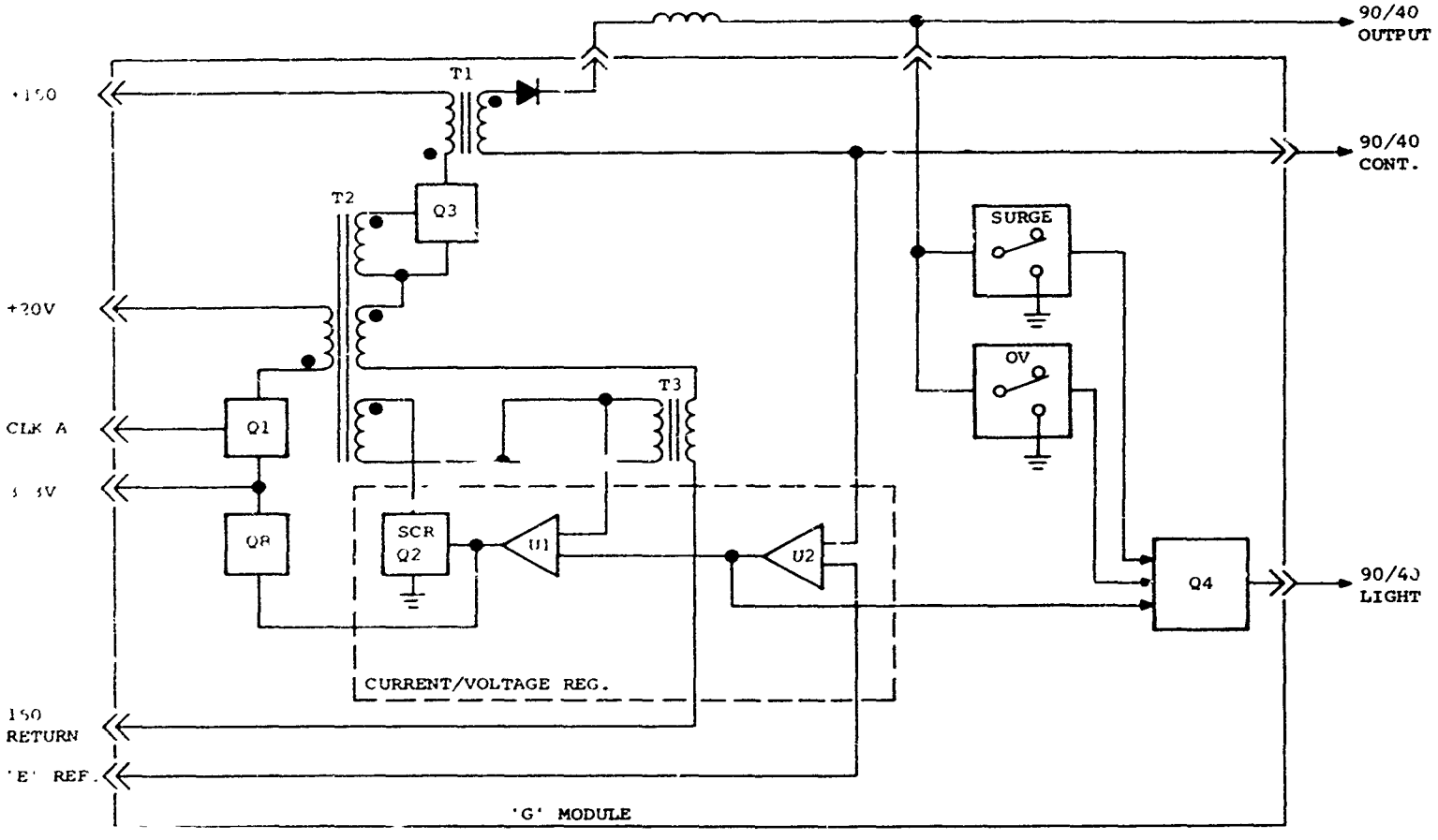


Figure 14-9. Power Supply Module G, Block Diagram

14.2.8 POWER SUPPLY MODULE E, +5 VOLT DC SUPPLY (Figure 4-10)

Module E accepts +150 Vdc and +20 Vdc inputs and through the flyback converter-regulator principle outputs regulated +5 Vdc. The flyback converter-regulator principle is explained in paragraph 2-12. Two time interleaved flyback circuits are used for high current (15 Amp). A clock input is used to set up the timing for theflyback circuit. The control circuits for the two flyback circuits are on module K.

14.2.9 POWER SUPPLY MODULE TYPE J (Figure 14-11)

Four series regulators and undervoltage sensing BITE circuits are contained on the J module. These regulators provide load isolation and current limiting in addition to tighter regulation than provided by the B type module. The input voltage to each regulator is line regulated by the flyback pre-regulator on module B. A clock generator on module J sets the switch frequency for the flyback converter on the H module. This module also provides the over and undervoltage protection circuits utilized by +55 Vdc which is used by the DSVT's. The +55 Vdc output is obtained from this module.

14.2.10 POWER SUPPLY MODULE K, +5 Vdc SUPPLY CONTROL (Figure 14-12)

Module K receives the +5 Vdc input from module E together with a constant reference voltage from module E. These two inputs are compared in U4, and the resultant -5 Vdc output is sent two places. The primary output is sent external to the module for distribution. The second output is used as an input to comparator U3.

A ramp voltage is the second input to comparator U3 (E REF) from module B. The two inputs are compared and a pulse is produced whenever the rising ramp equals 5V. The comparator output pulse turns off the clock circuits for the remainder of the present alternation. The clock outputs control the timing for the circuits of module E.

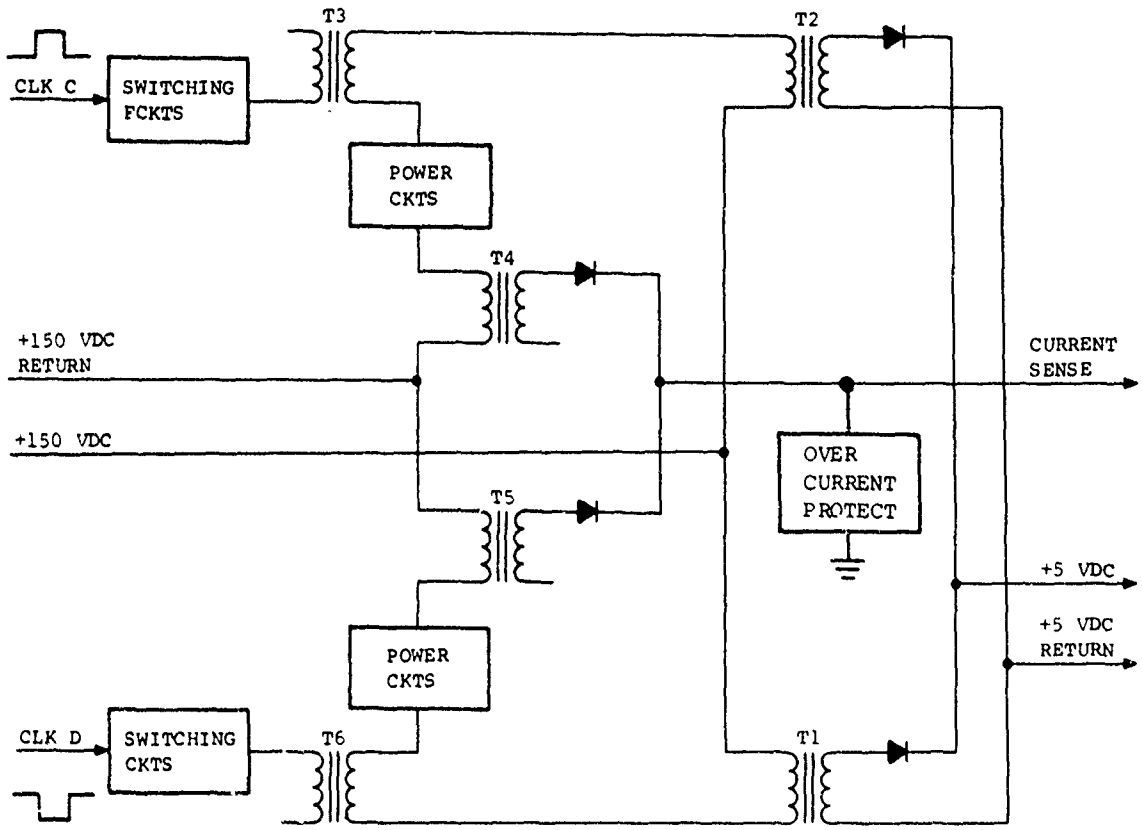


Figure 14-10. Power Supply Module E, Block Diagram.

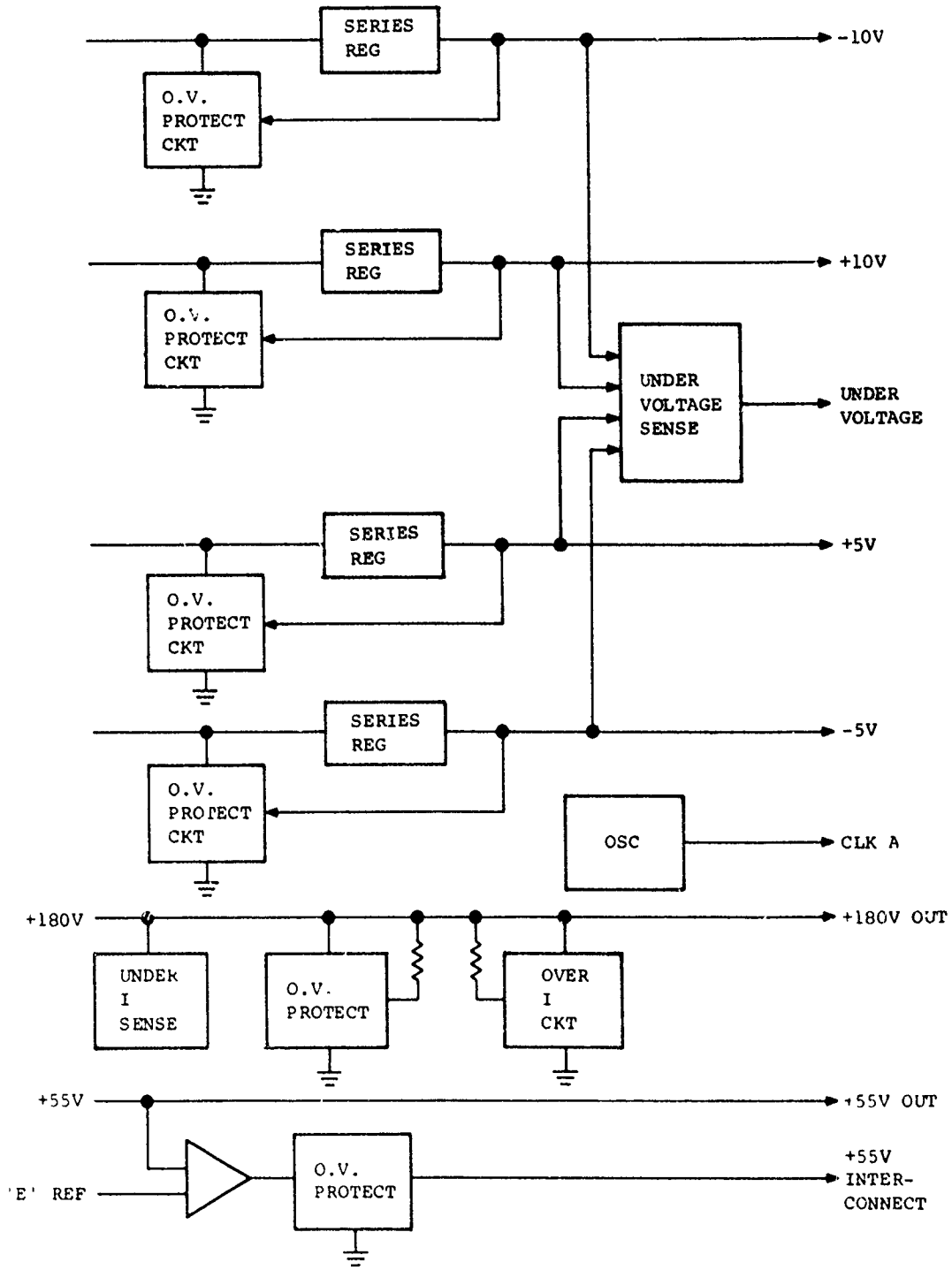


Figure 14-11. Power Supply Module J, Block Diagram

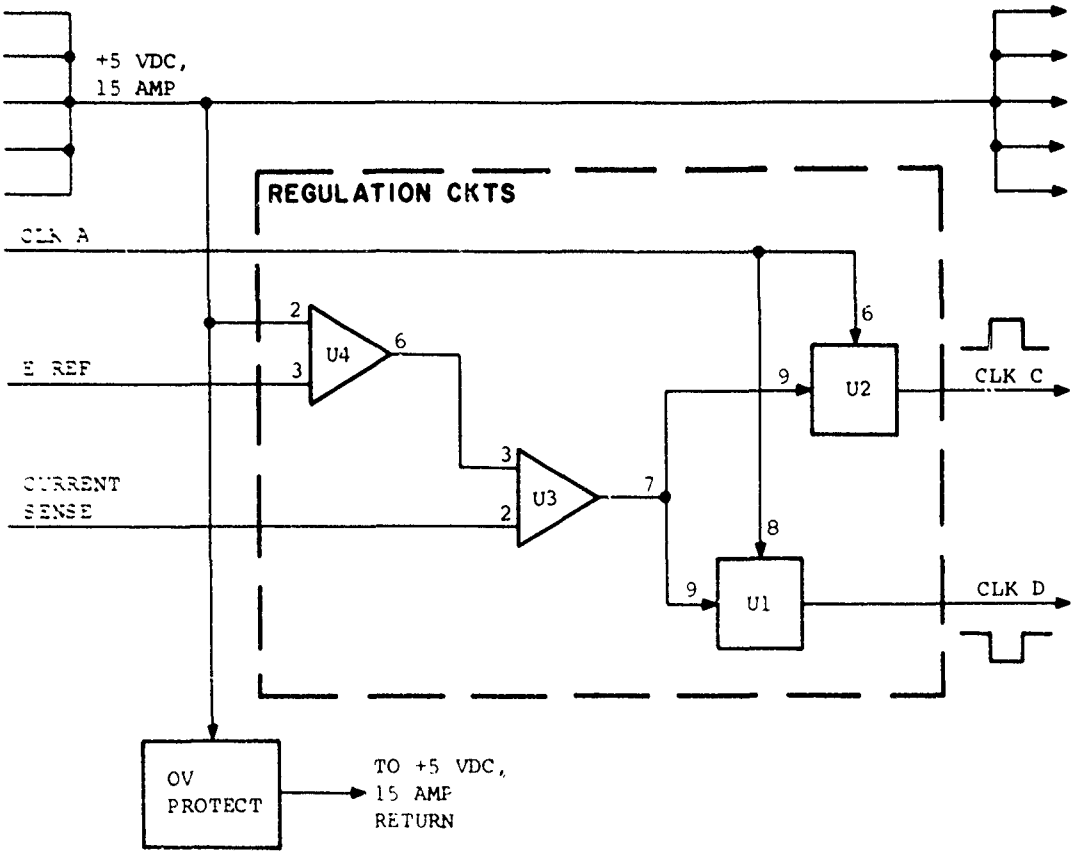


Figure 14-12. Power Supply Module K, Block Diagram

14.3 EMI

The power supply assembly is shielded to reduce radiated EMI from the switching regulators. The front and rear of the power supply opening is gasketed to prevent leakage out of the DGM equipment cases. The ac or dc prime power connector is an integral part of the power line filter to prevent EMI pickup in wiring between the filter and the connector. The power line filter is rated for the maximum dc current and ac voltage. This results in a filter larger than required for either ac or dc operation but smaller than two separate ac and dc filters. Front panel switches and indicators are shielded.

14.4 RELIABILITY

Table 14-2 lists the reliability prediction for the power supplies giving the predicted failure rates with full power feed requirements.

TABLE 14-2

POWER SUPPLY FAILURE RATES PER MILLION HOURS

Unit	Prediction
LGM	26.8
RLGM	26.8
RLGM/CD	31.7
RMC	30.7
TGM	26.8
MGM	26.8
GM	26.8
CDM	30.7

During the Reliability Demonstration, there were more than 120,000 power supply operating hours, with a single failure.

SECTION 15

MECHANICAL DESIGN

15.1 SHELTER MOUNTED UNITS

15.1.1 CASE DESIGN

All DGM shelter mounted units are packaged in dip-brazed equipment cases 8-1/2" high by 12" deep by 17.25" wide except the MGM which is 14" high by 12" deep by 17.25" wide and fabricated from 6000 series aluminum alloy plate and extrusions. It has been Raytheon's experience that dip-brazing yields the most practical and versatile method to obtain good working tolerances and a good production yield for equipment case/chassis of this type, while providing cost effective joint design for suppression and control of EMI and RFI. The physical characteristics are contained in Table 15-1.

The equipment case is designed to accept mounting brackets in accordance with SC-B-627147; the four bracket mounting holes are located 3-3/16 inches back from the front edge of the case on both sides. Two carrying handles are mounted to the equipment case forward of the mounting brackets and positioned so as not to interfere with the ability to rack-mount the equipment in a standard electronic rack having dimensions conforming to MIL-STD-189.

Captivated, 10-32 thread, blind inserts are provided in the wall of the case for the rack-mounting brackets.

The shelter mounted equipment case/chassis (see Figure 15-1) is an integral assembly conforming to MIL-T-4734, constructed of aluminum alloys bonded by dip brazing techniques. Materials, parts and processes are in accordance with MIL-P-11268. Finishes are in accordance with MIL-F-14072; the unit is painted light grey enamel in accordance with TT-E-529, color #26250 in accordance with FED-STD-595; front panel marking is Group I in accordance with MIL-M-13231.

The equipment case is divided into two major compartments, one for the power supply and one for the plug-in PCB assemblies. The compartments are separated by a vertical shield to aid an isolation of signals and improve heat regulation. All plug-in subassemblies, i.e., power supply and PCBs are replaceable

TABLE 15-1

PHYSICAL CHARACTERISTICS

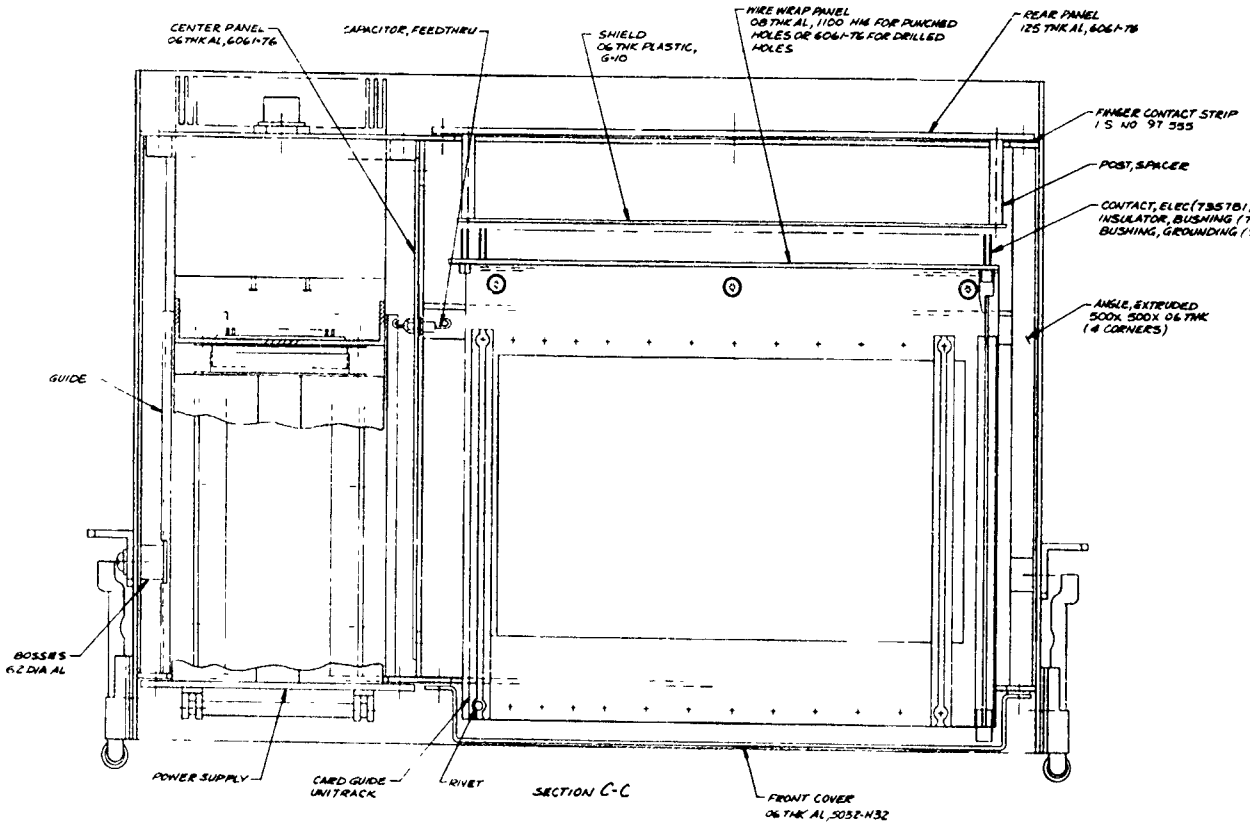
	TYPE	CASE DIMS, IN (H x W x D)	CASE VOL (FT^3)	PS WIDTH (IN)	NO. OF PCB'S	WEIGHT LB. SPEC	WEIGHT LB. ACT	WT DENSITY (#/FT^3)	PWR* DISS (WATTS)	PWR DENSITY ($WATT/IN^3$)	REMARKS
SHELTER UNITS											
TGM	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	4	11	35.3	37.0	36.3	62	0.035	PCB QTY INCL TEMP
GM	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	4	13	37.5	40.0	37.7	76	0.043	
RLGM/CD	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	7	4	33	31.2	30.6	165	0.094	
HSCDM	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	7	6	33	35.5	34.8	63	0.035	
LSCDM	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	7	6	33	35.3	34.3	44	0.025	
MGM	SHELTER	14x$17\frac{1}{4}$x12	1.68	4 (Horiz)	25	50.7	60.1	35.8	176	0.061	
LGM	SHELTER	$8\frac{1}{2}$x$17\frac{1}{4}$x12	1.02	4	13	37.5	37.0	36.3	139	0.079	SYLVANIA
REMOTE UNITS (SYLVANIA)											
PMC	REMOTE	W/O C $8\frac{1}{2}$x$17\frac{1}{4}$x13 W/C 12x21x19	1.10 2.77	4	12	43.0	44.0	40.0	150	W/O C 0.079	NUCLEAR; 4 FT DROP
RLGM	REMOTE	W/O C $8\frac{1}{2}$x$17\frac{1}{4}$x13 W/C $8\frac{1}{2}$x$17\frac{1}{4}$x13	1.10 2.77	4	7	35.7	37.0	33.6	37	W/O C 0.019	NUCLEAR 4 FT DROP
RESTORER UNITS											
HSPR	REMOTE	4.0 DIA x 10 LG	0.07	-	2	7.5	6.9	98	1.1	0.01	20 FT DROP
LSPR	REMOTE	4.0 DIA x 10 LG	0.07	-	2	7.5	6.9	98	0.4	≈ 0	20 FT DROP
TEST SET											
COU	PORTABLE	12 x 11 x 11	0.84	BATT	2.0	22.0	25.6	30.5	3.0	≈ 0	4 FT DROP

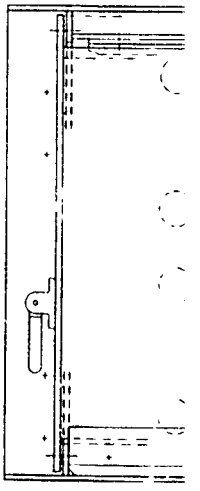
*TOTAL PWR DISS FOR UNIT: INCLUDES A 15% SAFETY FACTOR
TOTAL PWR DISS SHOWN INCLUDES POWER DISSIPATED ON THE POWER SUPPLY HEAT SINK

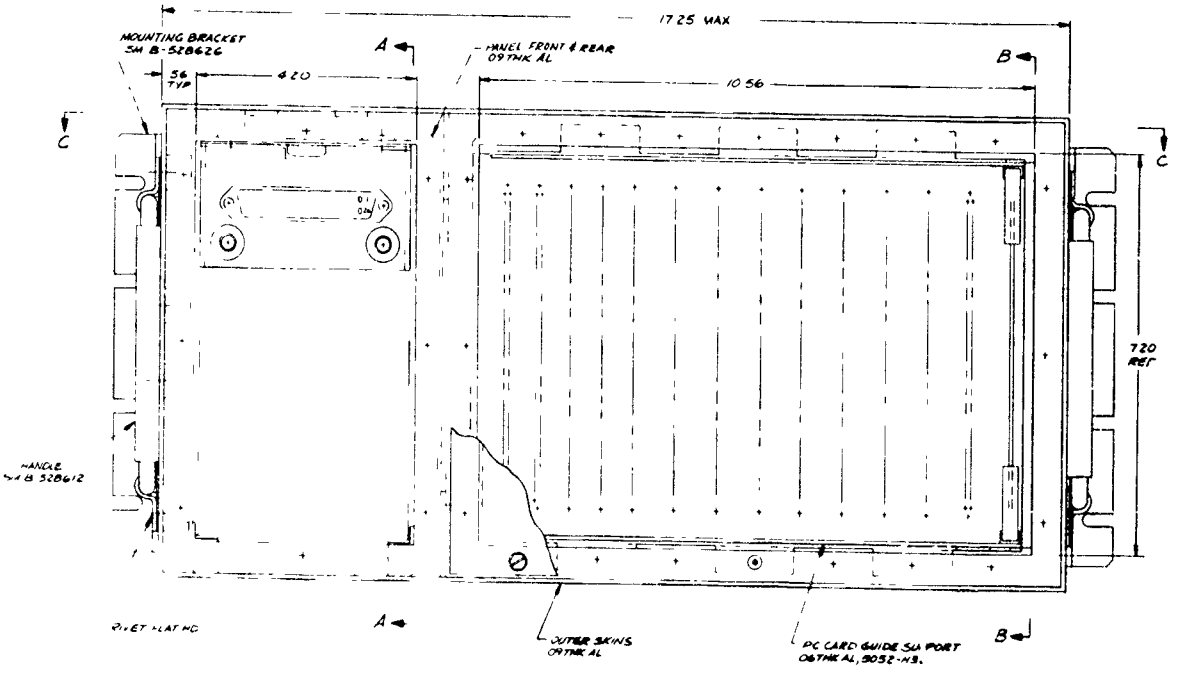
RAYTHE

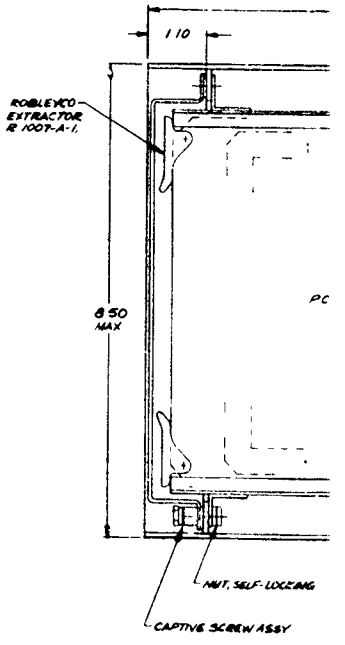
EQUIPME

NOTES
1 DIP BRAZE PER MIL
2 MATERIAL MILL SHALL
ALUMINUM EXCEPT
3 FINISH E613 PER SP
ELECTRICALLY CONC
4 EXTERIOR SURFACE
LIGHT GRAY COLOR M
FED-STD-595
5 YER LAPING AREA
PANEL AND POWER
TO BE MASK PRIOR
6 HEAT TREATMENT
61 AIR COOL AFTER B
AT 350°F FOR 6 T
62 MECHANICAL PRO
QQ-A-250/11 FOR









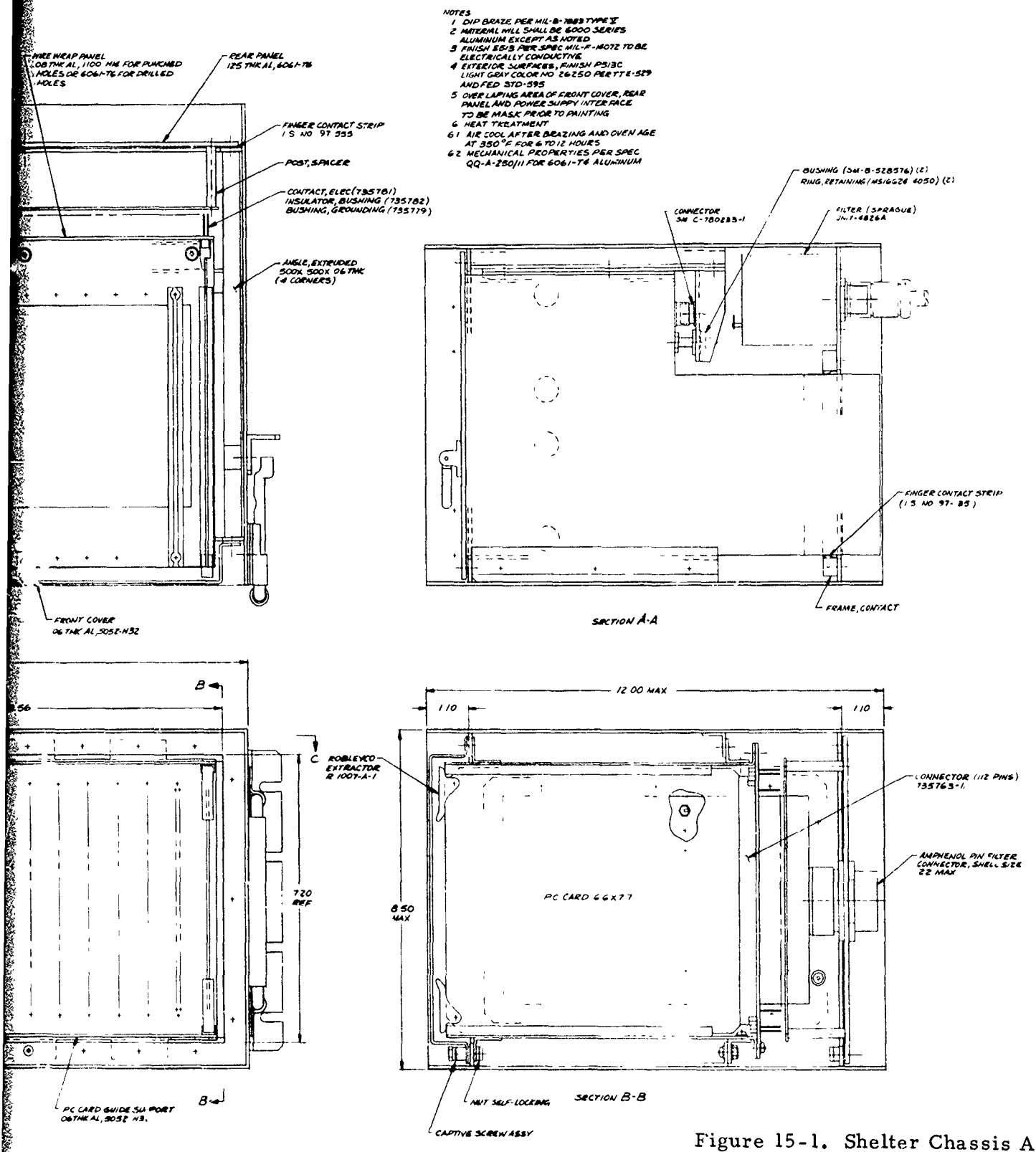
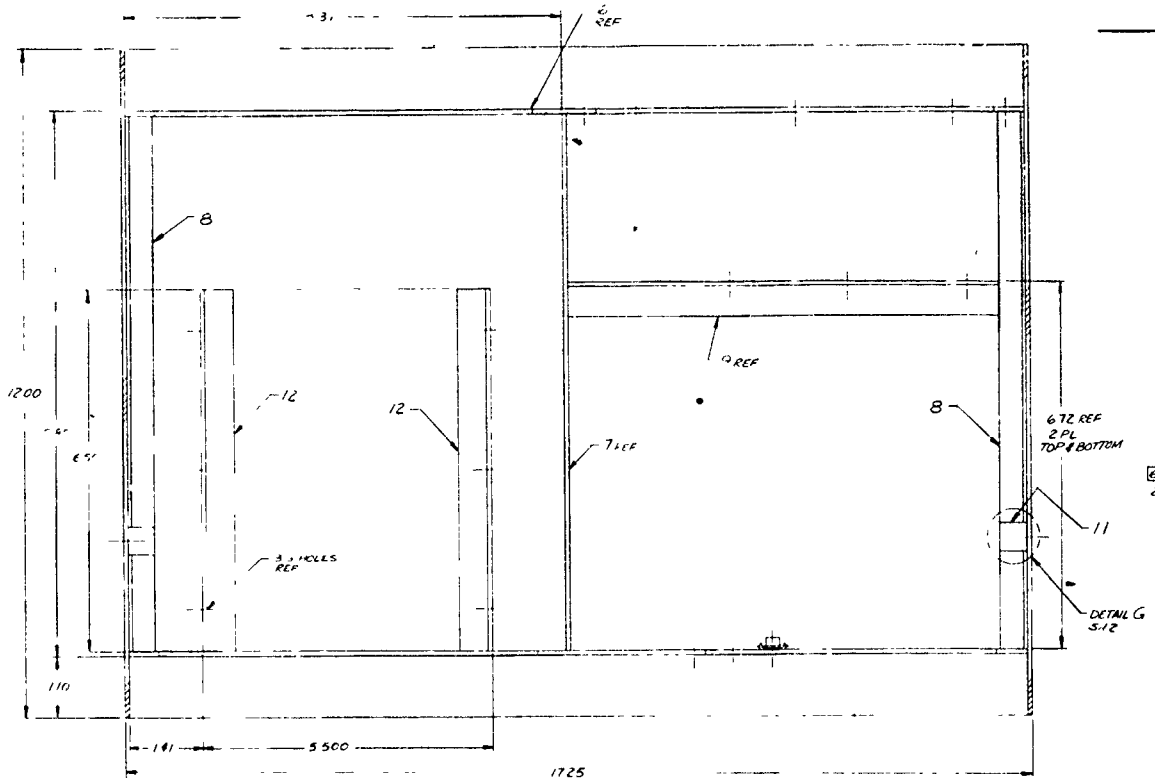
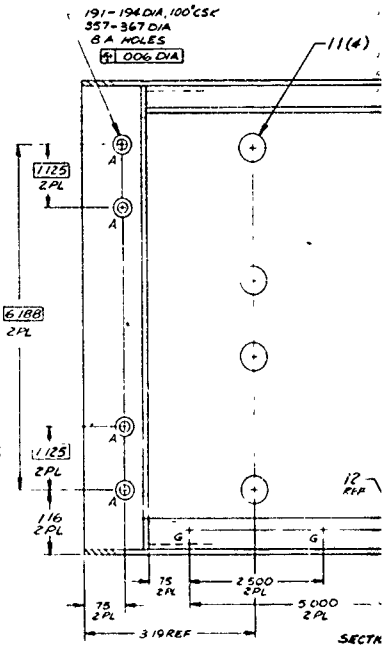
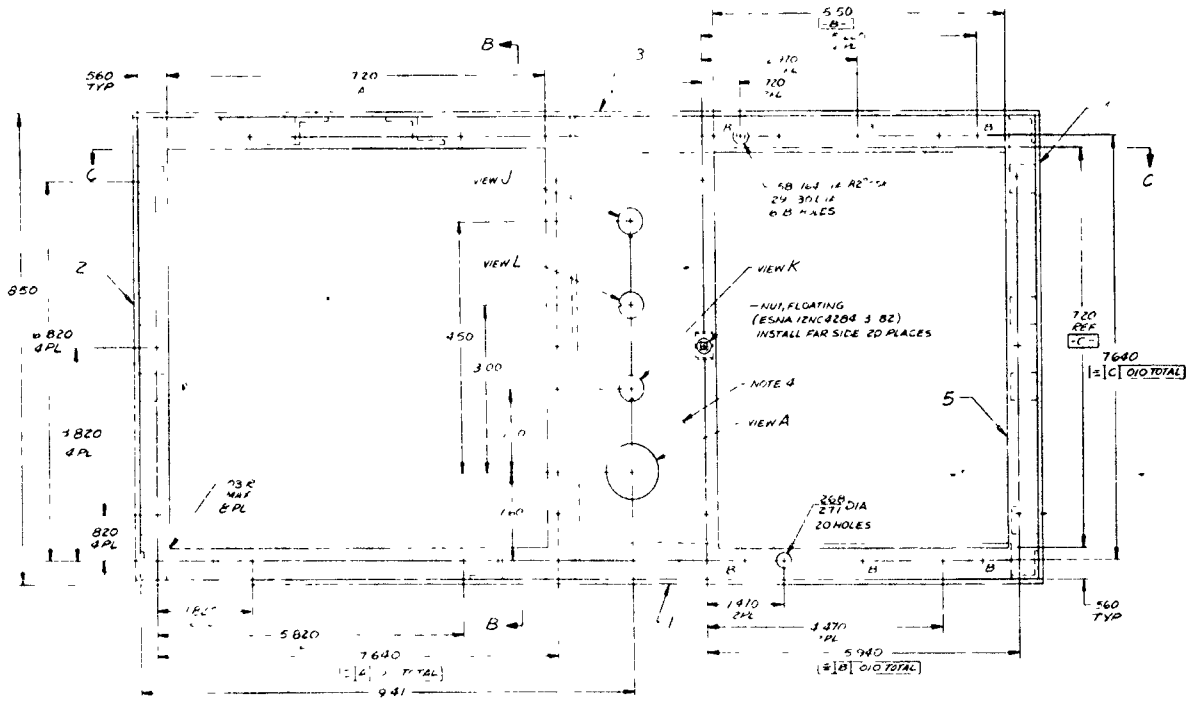


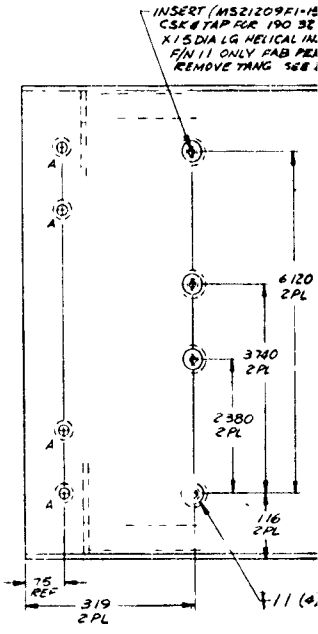
Figure 15-1. Shelter Chassis Assembly (TGM, GM, LGM) (Sheet 1 of 2)

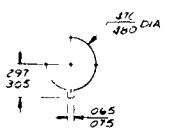




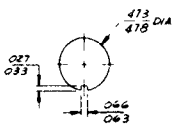
SECTION C-C



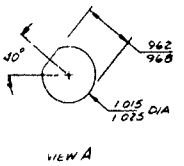




VIEW J
SCALE 2/1



VIEW K
VIEW L ROTATE AS SHOWN
SCALE 2/1



VIEW A

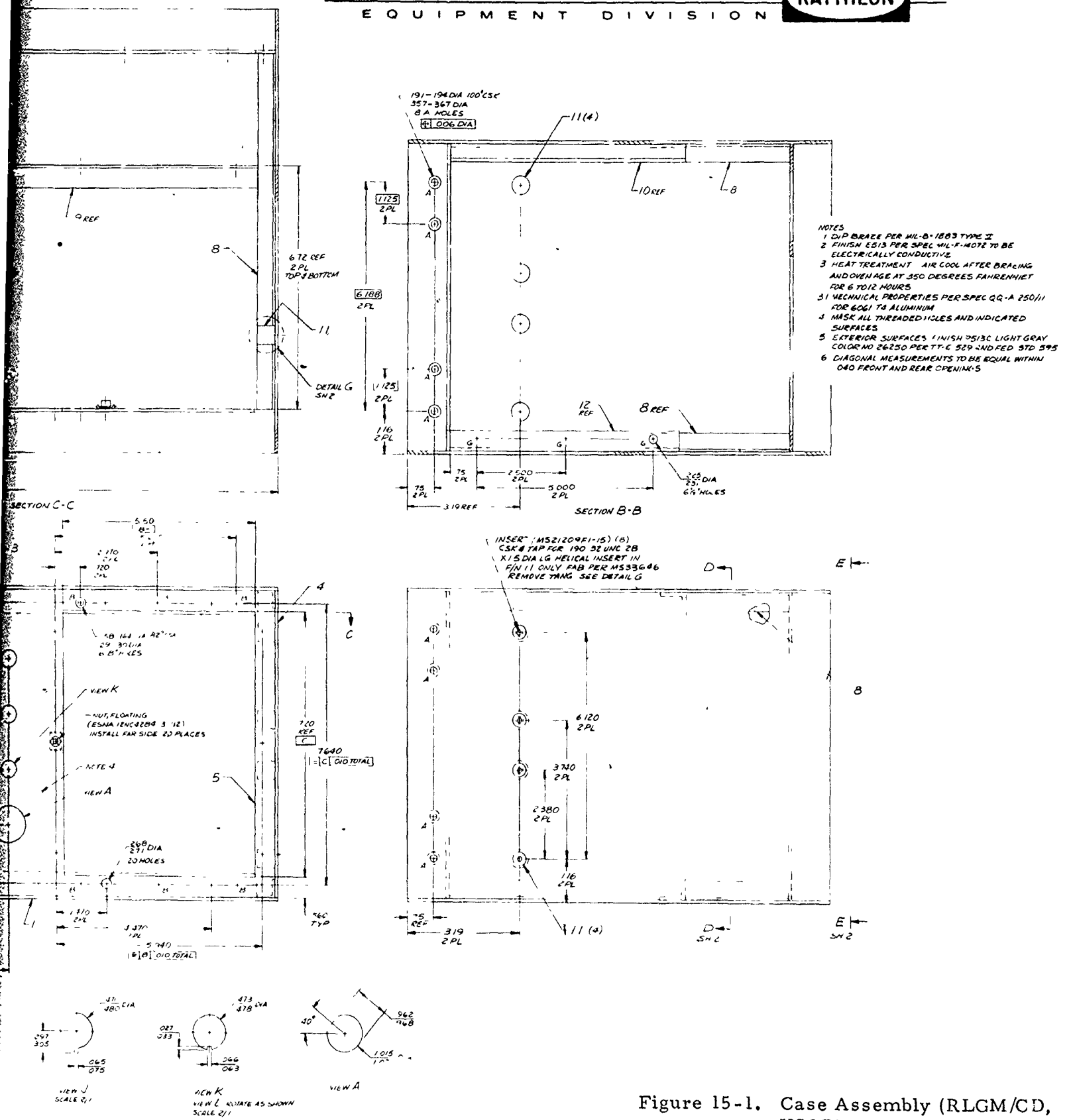


Figure 15-1. Case Assembly (RLGM/CD, HSCDM, LSCDM)
(Sheet 2 of 2)

from the front of the unit. A removeable RFI gasketed cover complete with captive hardware encloses the PCB compartment.

All normal operational and hookup connectors are located on the rear surface of the unit. A rear cover provides major maintenance and initial installation access to the wiring of the wirewrapped panel. All operational controls are mounted on the front panel immediately accessible to the operator. Localized fault locating is provided on each plug-in subassembly (see Figures 15-2 through 15-5).

15.1.2 PRINTED CIRCUIT CARD DESIGN

The DGM shelter mounted and remote equipments with the exception of the COU and the PRS use a standard sized plug-in PCB. The standard panel features a 112 pin male blade connector and two panel extractors (see Figure 15-6). The outer surfaces of the PCB contain mounting pads around component lead holes, and these outer layers serve as protective barriers to avoid circuit damage due to mishandling. The inner layers consist of two signal layers, a voltage layer and a ground layer. The voltage and ground layers or planes are relatively full layers of copper and enhance the removal of heat from the component directly to the PCB guide system and eventually to the outer case structure.

The board size is 6.6 by 7.7 inches excluding connector: the same board is used in the remote and shelter units to maintain complete interchangeability of the common circuits which occur in LGM, RLGM and RMC. Each PCB features two stainless steel keying/guide pins integral with the connector; the orientation of the pins is selected from the master Keying chart (see Figure 15-7).

The keying bushing will be inserted in the corresponding mating receptacle in the W/W plate. A selection of a sintered stainless steel keying bushing has been made to prohibit any chance of overriding the keying features and cause possible damage to the PCB.

An alphanumeric matrix for the location of DIPS was established which predetermines the location of the DIP to a grid pattern 0.7 by 1.0 inches. The grid allows adequate space between DIPs for interconnections and discrete components such as diodes, resistors and capacitors while maintaining established locations

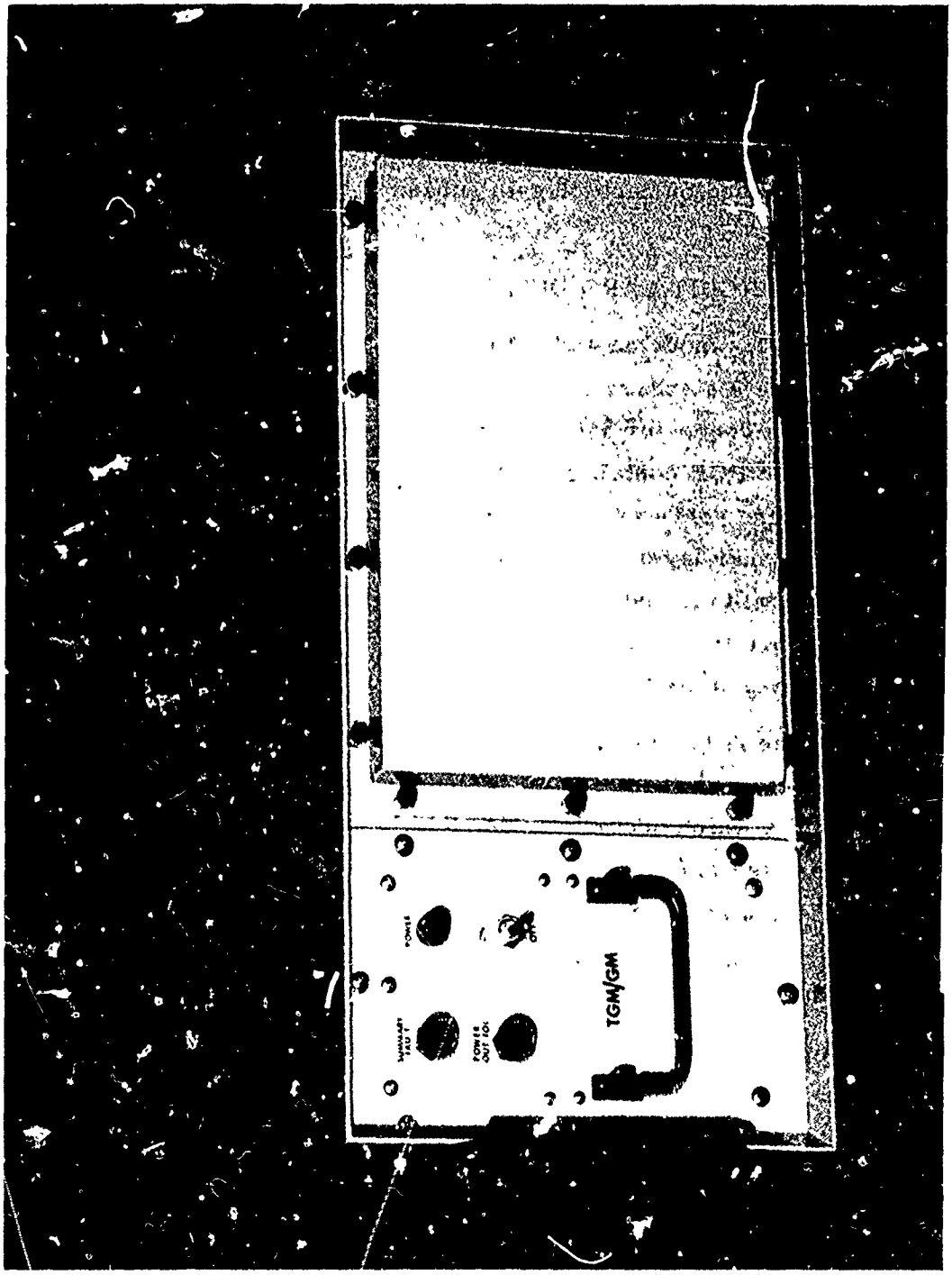


Figure 15-2. TGM, GM Unit Configuration

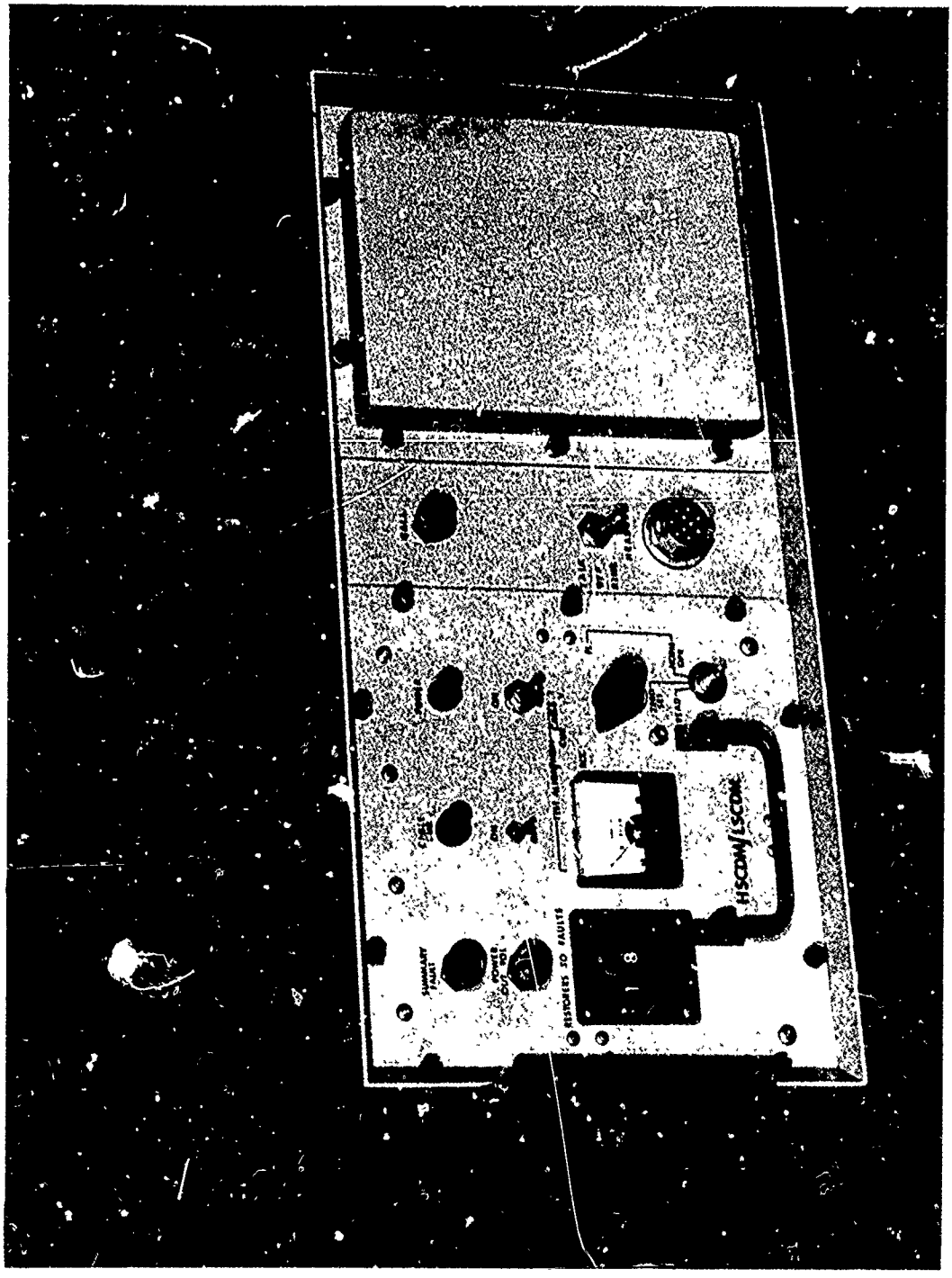


Figure 15-3. LSCDM, HSCDM Unit Configuration

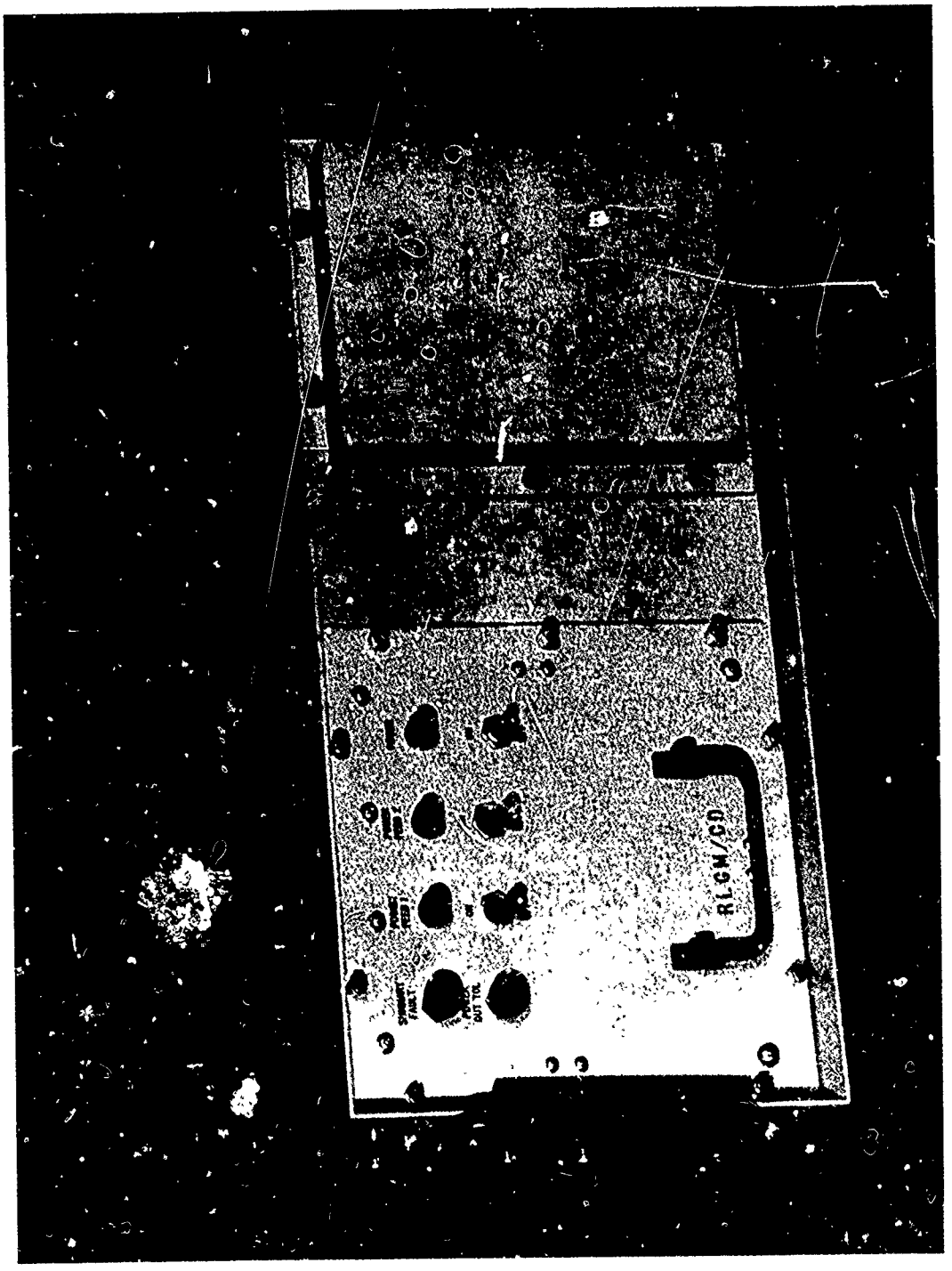


Figure 15-4. RLGM/CD Unit Configuration

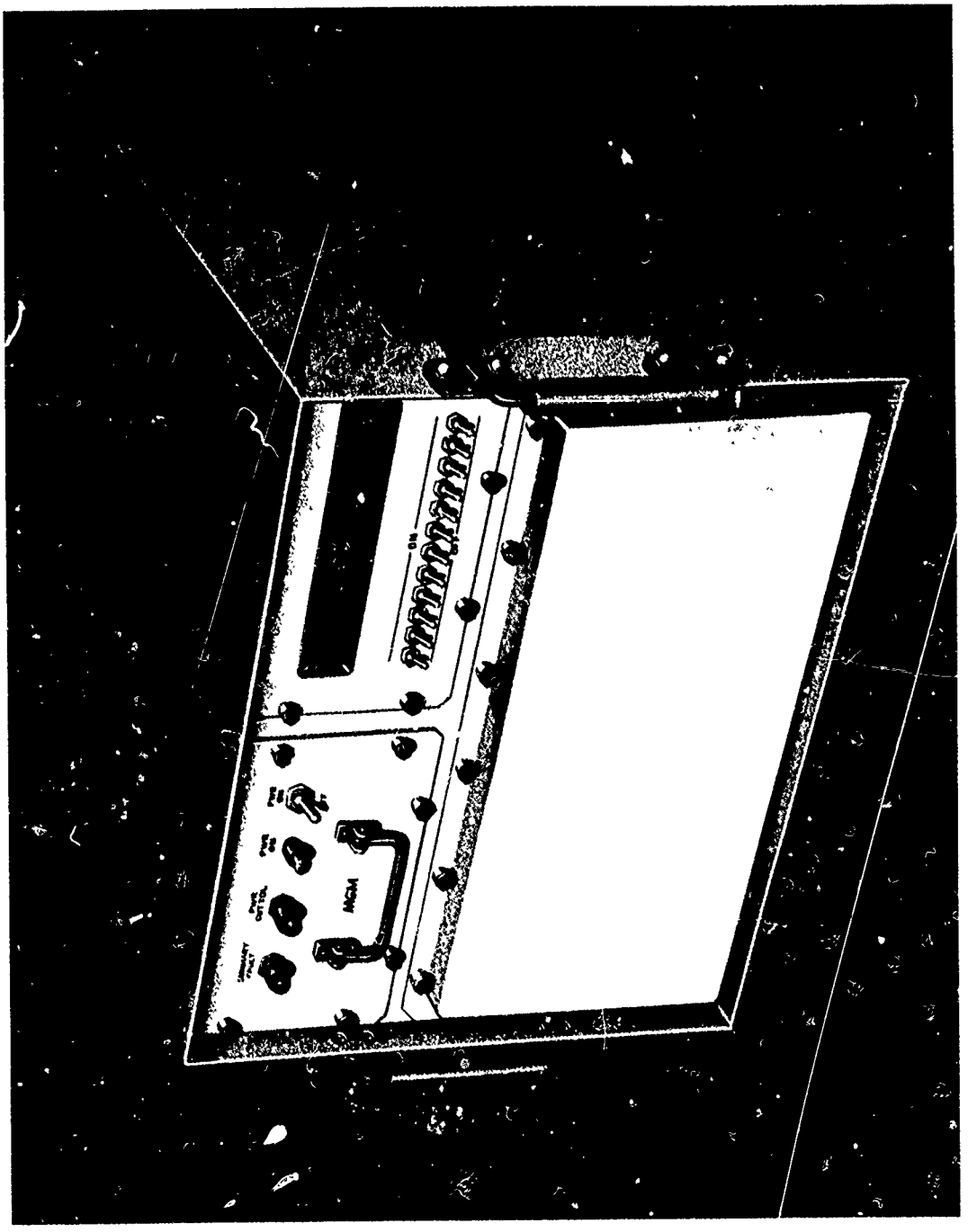
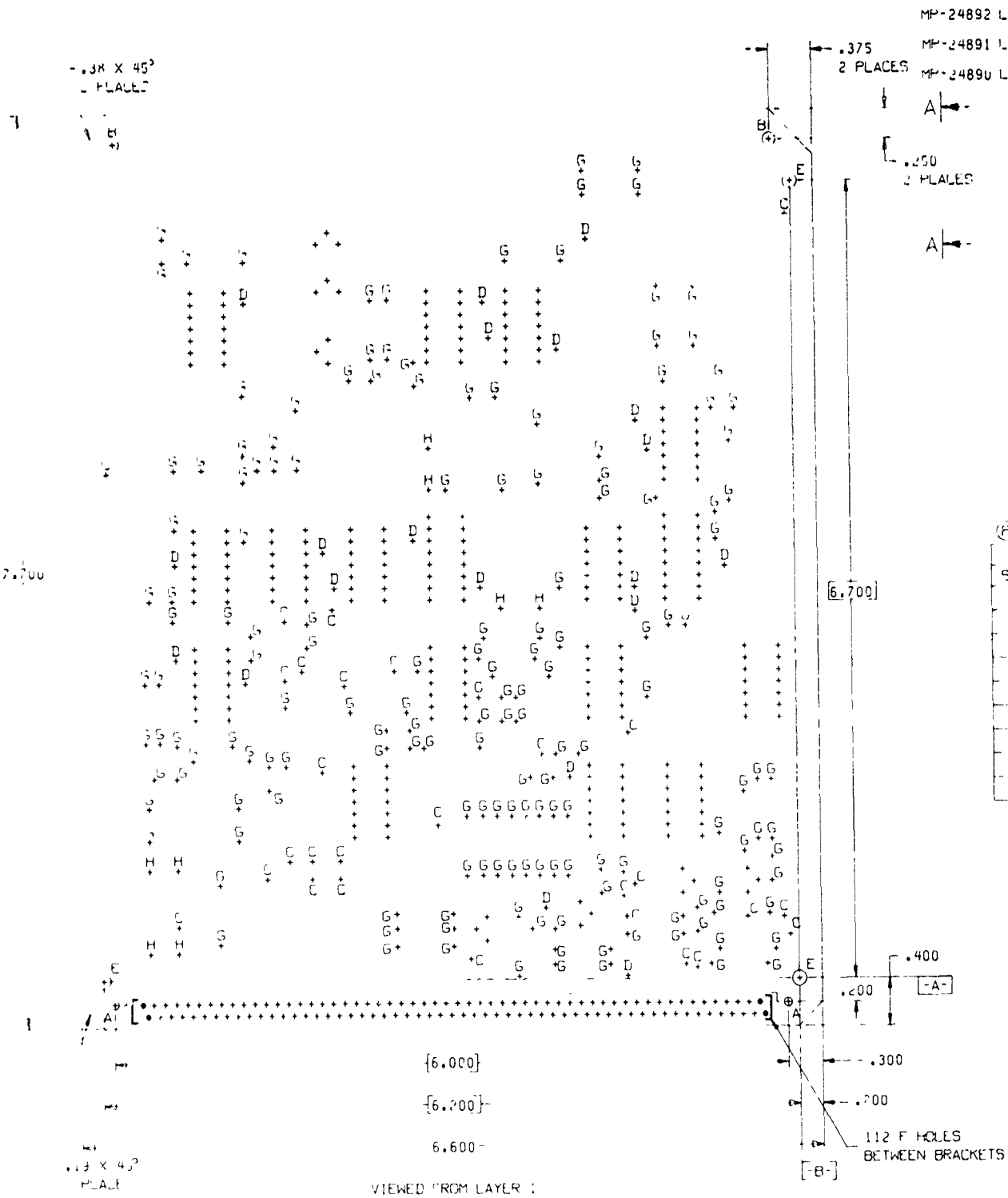


Figure 15-5. MGM Unit Configuration

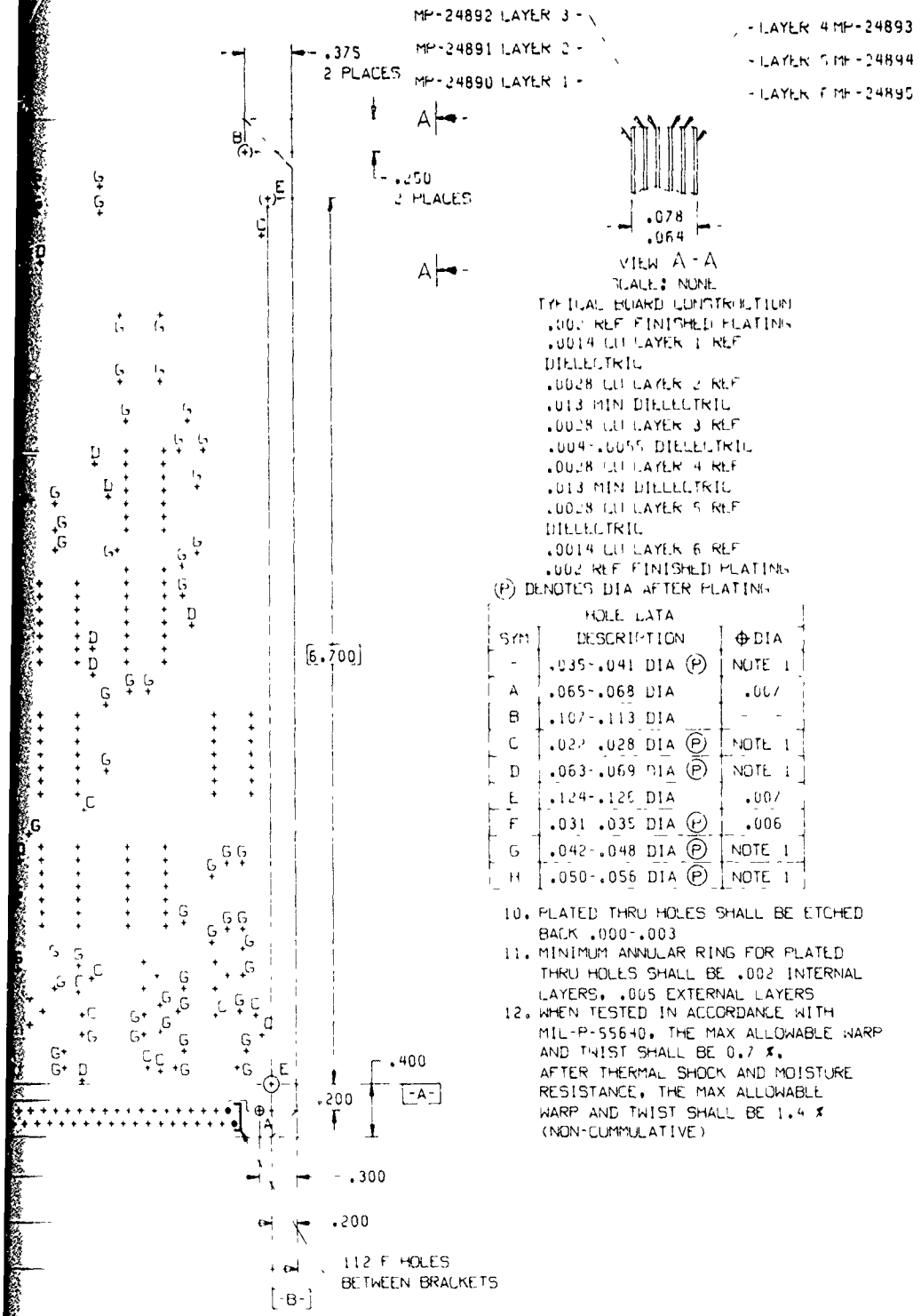


TYPICAL BOARD CONSTRU
.002 REF FINISHED PL
.0014 CU LAYER 1 REF
DIELECTRIC
.0028 CU LAYER 2 REF
.013 MIN DIELECTRIC
.0028 CU LAYER 3 REF
.004-.0055 DIELECTRI
.0028 CU LAYER 4 REF
.013 MIN DIELECTRIC
.0028 CU LAYER 5 REF
DIELECTRIC
.0014 CU LAYER 6 REF
.002 REF FINISHED PL

(P) DENOTES DIA AFTER PLAT

HOLE DATA		
SYM	DESCRIPTION	
-	.035-.041 DIA (P)	N
A	.065-.068 DIA	
B	.107-.113 DIA	
C	.026-.028 DIA (P)	N
D	.063-.069 DIA (P)	N
E	.124-.126 DIA	
F	.031-.035 DIA (P)	
G	.042-.048 DIA (P)	N
H	.050-.056 DIA (P)	N

10. PLATED THRU HOLES SHA
BACK .000-.003
11. MINIMUM ANNULAR RING
THRU HOLES SHALL BE .
LAYERS, .005 EXTERNAL
12. WHEN TESTED IN ACCORI
MIL-P-55640, THE MAX
AND TWIST SHALL BE 0.
AFTER THERMAL SHOCK A
RESISTANCE, THE MAX A
WARP AND TWIST SHALL
(NON-CUMMULATIVE)



TYPICAL BOARD CONSTRUCTION
.001 REF FINISHED PLATING
.0014 CU LAYER 1 REF
DIELECTRIC
.0028 CU LAYER 2 REF
.013 MIN DIELECTRIC
.0028 CU LAYER 3 REF
.004-.0055 DIELECTRIC
.0028 CU LAYER 4 REF
.013 MIN DIELECTRIC
.0028 CU LAYER 5 REF
DIELECTRIC
.0014 CU LAYER 6 REF
.002 REF FINISHED PLATING

Ⓟ DENOTES DIA AFTER PLATING

HOLE DATA

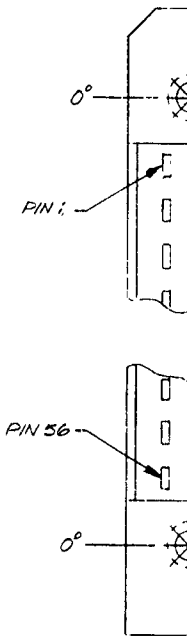
SYM	DESCRIPTION	⊕ DIA
-	.035-.041 DIA Ⓟ	NOTE 1
A	.065-.068 DIA	.007
B	.107-.113 DIA	- -
C	.027-.028 DIA Ⓟ	NOTE 1
D	.063-.069 DIA Ⓟ	NOTE 1
E	.124-.126 DIA	.007
F	.031-.035 DIA Ⓟ	.006
G	.042-.048 DIA Ⓟ	NOTE 1
H	.050-.056 DIA Ⓟ	NOTE 1

10. PLATED THRU HOLES SHALL BE ETCHED BACK .000-.003
11. MINIMUM ANNULAR RING FOR PLATED THRU HOLES SHALL BE .002 INTERNAL LAYERS, .005 EXTERNAL LAYERS
12. WHEN TESTED IN ACCORDANCE WITH MIL-P-55640, THE MAX ALLOWABLE WARP AND TWIST SHALL BE 0.7 %, AFTER THERMAL SHOCK AND MOISTURE RESISTANCE, THE MAX ALLOWABLE WARP AND TWIST SHALL BE 1.4 % (NON-CUMMULATIVE)

NOTES:
1. UNDIMENSIONED HOLES SHALL BE LOCATED ON GRID INCREMENTS FROM DATUMS -A- AND -B- WITHIN .010 DIA OF TRUE POSITION UNLESS OTHERWISE SPECIFIED
2. MATERIAL:
   2.1 BASE LAMINATE: COPPER CLAD, GLASS BASE, EPOXY RESIN (GF), 2 OUNCE COPPER ON INTERNAL LAYERS, 1 OUNCE COPPER ON EXTERNAL LAYERS, SHALL BE IN ACCORDANCE WITH MIL-P-55617
   2.2 BONDING AGENT: PREPREGNATED E STAGE EPOXY GLASS CLOTH, SHALL BE IN ACCORDANCE WITH MIL-P-55636 (TYPE GF)
3. BASIC GRID INCREMENT IS .025 AT 1/1 SCALE
4. FOR MANUFACTURING PURPOSES ONLY, ANY REPRESENTATION SHALL NOT BE REPRODUCED TO OR FROM A REPRODUCIBLE THAT IS MADE FROM OTHER THAN A STABLE BASE MATERIAL PER MIL-I-8700, TYPE II, OR EQUIVALENT
5. COMPOSITE MULTILAYER BOARD SHALL COMPLY WITH MIL-P-55640
6. LAYER TO LAYER REGISTRATION OF ALL TERMINAL AREAS SHALL BE WITHIN .010 OF EACH OTHER
7. PLATE HOLES AND EXTERNAL LAYERS .001 MIN COPPER PER MIL-C-14550 FOLLOWED BY TIN-LEAD ELECTRO-PLATE PER MIL-P-55640
8. MASTER PATTERN OF PRINTED WIRING MP-24890 THRU MP-24895 WILL BE SUPPLIED BY U.S. ARMY ELECTRONICS COMMAND ATTN: AMSEL-PE-EL, FORT MONMOUTH, NEW JERSEY
9. MINIMUM CONDUCTOR WIDTH FOR INTERNAL AND EXTERNAL LAYERS .010 MINIMUM CONDUCTOR SPACING FOR INTERNAL AND EXTERNAL LAYERS .010

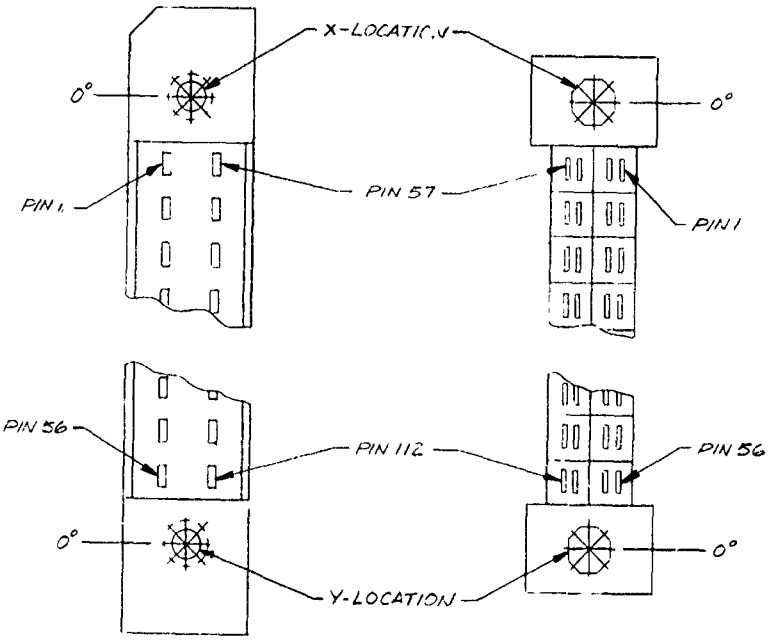
Figure 15-6. Typical PCB Detail

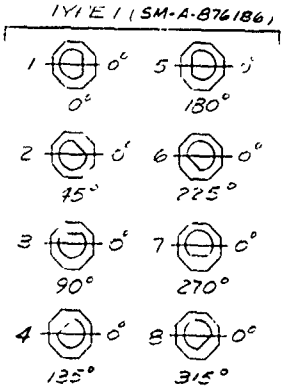
PART NO.	CIRCUITCARD ASSY	USED IN	PCB IDENT	KEYING FEATURE Y-LOCATION PIN TYPE	KEYING FEATURE Y-LOCATION ORIENTATION	KEYING FEATURE X-LOCATION PIN TYPE	KEYING FEATURE X-LOCATION ORIENTATION	WIRE WRAP PANEL KEYING FEATURE Y-LOCATION INSERT TYPE	WIRE WRAP PANEL KEYING FEATURE Y-LOCATION ORIENTATION	WIRE WRAP PANEL KEYING FEATURE X-LOCATION INSERT TYPE	WIRE WRAP PANEL KEYING FEATURE X-LOCATION ORIENTATION
SM-E-876650	TIMING GEN	LGM	TMGGEN	1	1	1	1	1	1	1	1
SM-E-876662	BITE A	LGM	BITE A				2				2
							3				3
SM-E-876638	INTERFACE	LGM	INTFC				4				4
SM-E-876658	LOOP MODEM	LGM	LP MDM				5				5
							6				6
SM-E-876686	MUX/DEMUX	LGM	MUX				7				7
SM-E-876642	GROUP FRAMING	LGM	GP FRG		1		8		1		8
SM-E-876654	GROUP MODEM	LGM	GP MDM		2		1		2		1
SM-D-875941	GROUP MUX/DEMUX	TGM	GP MUX				2				2
-875942	TIMING	TGM	TMG				3				3
875944	SUPERGROUP A	TGM	SUPGPA				4				4
875945	MICRO CONTROLLER	TGM	MKRO C				5				5
875947							6				6
875948	BITE		BITE				7				7
875949	TEMPEST BUFFER	TGM	TEM BUF		2		8		2		8
875954	CABLE DRIVER	RIGM/CD	CA DRVR		3		1		3		1
875955	MASTERGROUP RECEIVE	MGM	MGP RCV				2				2
875958	GROUP LOGIC	MGM	GP LGC				3				3
875959	FORMAT GEN	MGM	FORM GEN				4				4
875961	FRAMING	MGM	FRG				5				5
875962	OW MUX/DEMUX	MGM	MUX OW				6				6
875969	COND DIPHASE A	GM	DPHS A				7				7
875971	DIPULSE	GM	DPLS				7				7
875972	BIPOLAR	GM	BPLR		3		7		3		7
875976	TRAFFIC XMT HS	HSCDM	TRFC XMT		4		2		4		2
875977	TRAFFIC RCV A HS	HSCDM	TRF RCV A				3				3
875979	ORDERWIRE TRANSMIT	CDM	OW XMT				4				4
875980	ORDERWIRE RECEIVE	CDM	OW RCV				5				5
875985	TRAFFIC RCV A LS	LSCDM	TRF RCV A				6				6
875986	TRAFFIC XMT LS	LSCDM	TRFC XMT				7				7
875991	CABLE ORDERWIRE	GM	CA OW		4		8		4		8
SM-D-875992	COND. DIPHASE B	GM	DPHS B		3		7		3		7
SM-D-876004	TRAFFIC RCV B HS	HSCDM	TRF RCV B		5		2		5		2
876006	SUPERGROUP TIMING	TGM	SUPGPT				3				3
876007	SCANNER	MGM	SCNR				4				4
876008	RATE SELECT	MGM	RT SEL				5				5
876009	TRANSMIT RATE GEN	MGM	XMT GEN				6				6
876010	RECEIVE RATE GEN	MGM	RCV GEN		5		7		5		7
876139	CONVERTER, SIGNAL DATA	GM	CONV		3		7		3		7
876258	CABLE INTERFACE	RIGM/CD	CA INTFC		6		1		6		1
876265	TRAFFIC RCV B LS	LSCDM	TRF RCV B				2				2
SM-D-876269	SUPERGROUP B	TGM	SUPGR B				3				3
SM-D-876000	GROUP MUX	103	GP MUX				4				4
875947	RECEIVE TIMING	103	RCV TIM				5				5
876024	TRANSMIT TIMING	103	XMT TIM				6				6
8844454	REGENERATOR	103	REGEN				7				7
876111	DEMUX	103	DEMUX		6		8		6		8
SM-D-876173	EUROCOM	103	EUR		7		1		7		1
							2				2
							3				3
							4				4
							5				5
							6				6
							7				7
					7		8		7		8
					8		1		8		1
							2				2
							3				3
							4				4
							5				5
							6				6
							7				7
				1	8	1	8	1	8	1	8



PRINTED
(CONNEC

	WIRE WRAP PANEL KEYING FEATURE			
	Y-LOCATION		X-LOCATION	
	INSERT TYPE	ORIEN-TATION	INSERT TYPE	ORIEN-TATION
1	1	1	1	1
2				2
3				3
4				4
5				5
6				6
7				7
8		1		8
1		2		1
2				2
3				3
4				4
5				5
6				6
7				7
8		2		8
1		3		1
2				2
3				3
4				4
5				5
6				6
7				7
7				7
7		3		7
2		4		2
3				3
4				4
5				5
6				6
7				7
8		4		8
7		3		7
2		5		2
3				3
4				4
5				5
6				6
7		5		7
7		3		7
1		6		1
2				2
3				3
4				4
5				5
6				6
7				7
8		6		8
1		7		1
2				2
3				3
4				4
5				5
6				6
7				7
8		7		8
1		8		1
2				2
3				3
4				4
5				5
6				6
7				7
8	1	8	1	8





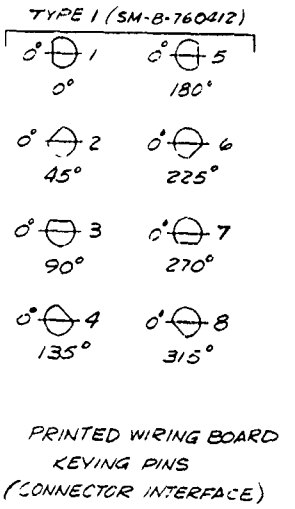


Figure 15-7. Master Keying Chart

compatible with automatic insertion equipment. The standard DGM PCB has a DIP density capability of 61 ICS and a workable surface area, excluding the connector and extractors, of 49.5 inches square. The PCBs are designed to meet MIL-STD-275C, and MIL-P-55640 as applicable (see Figure 15-8).

15.1.2.1 Connector Description

The printed circuit board connector system used in the DGM equipments is a two piece type connector system of proven reliability and quality and is adaptable to low cost - high volume production. This connector system is the same as used on a number of previous and current Raytheon programs including TDMA (SATCOM); SAM-D (MICOM); AEGIS (Navy); TARTAR-D (Navy), AN/TPQ-31 (Marine Corps); etc. (see Figure 15-9).

15.1.2.2 Extractor

The extractors selected are molded nylon and assembled to the PCB via spring pins. In selecting the extractor particular attention was given to strength for PCB removal, surface area for aiding insertion, and marking area for uniquely identifying each PCB and its respective unit. To verify the adequacy of the extractor Raytheon conducted an ultimate load test, which is described in the following paragraphs.

15.1.2.2.1 Test Method

- Extraction Test (see Figure 15-10)

A typical DGM PCB (multilayer) was placed in a loading fixture and inserted into a wirewrap plate (simulated PCB - plate configuration). A tensile load was applied to the plastic PCB extractors by means of a Draw Bar Linkage. Force required to extract PCB was recorded.

- Ultimate Load Test

The typical DGM PCB was secured to the loading fixture. A tensile load was applied to the plastic PCB extractors by means of the Draw Bar Linkage. Load was applied until the retaining pivot pin of the extractor bent/ejected. Hardened drill rod was used to replace the extractor pin and tensile load was applied until the drill rod sheared through the PCB. Forces were recorded for each failure mode.

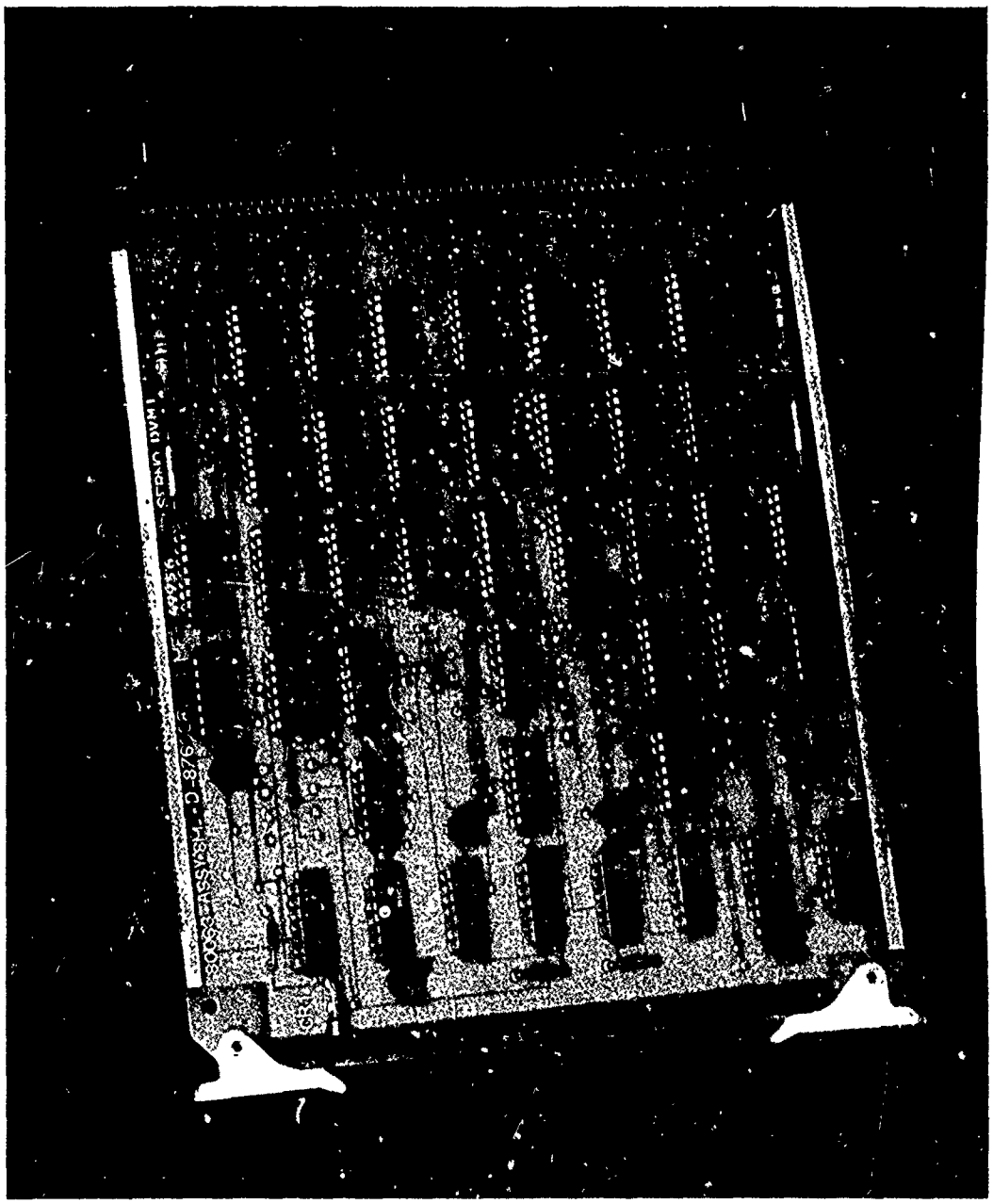


Figure 15-8. Typical PCB Assembly (6 Layer)

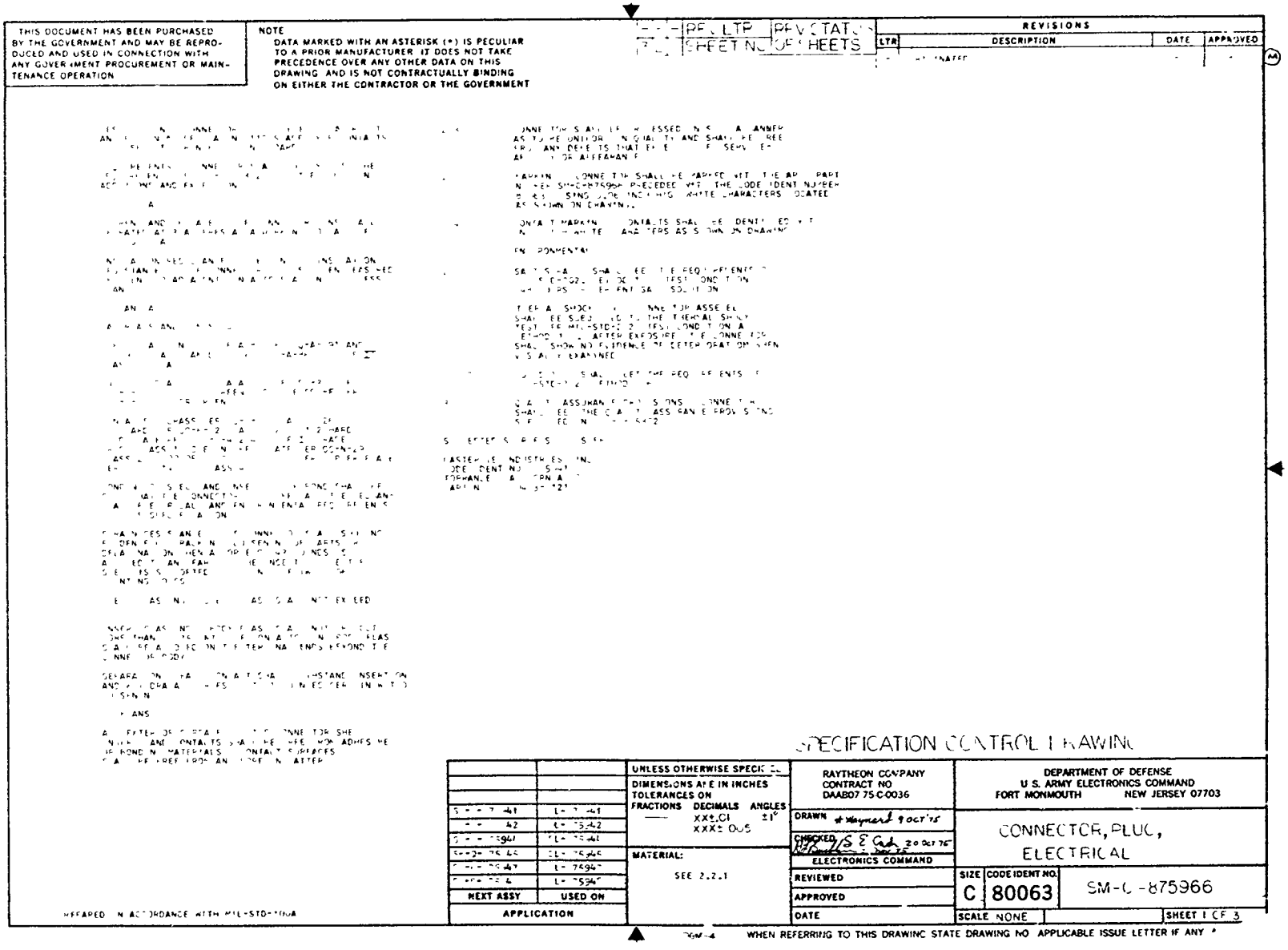


Figure 15-9. 112 Pin Electrical Connector (Sheet 1 of 3)

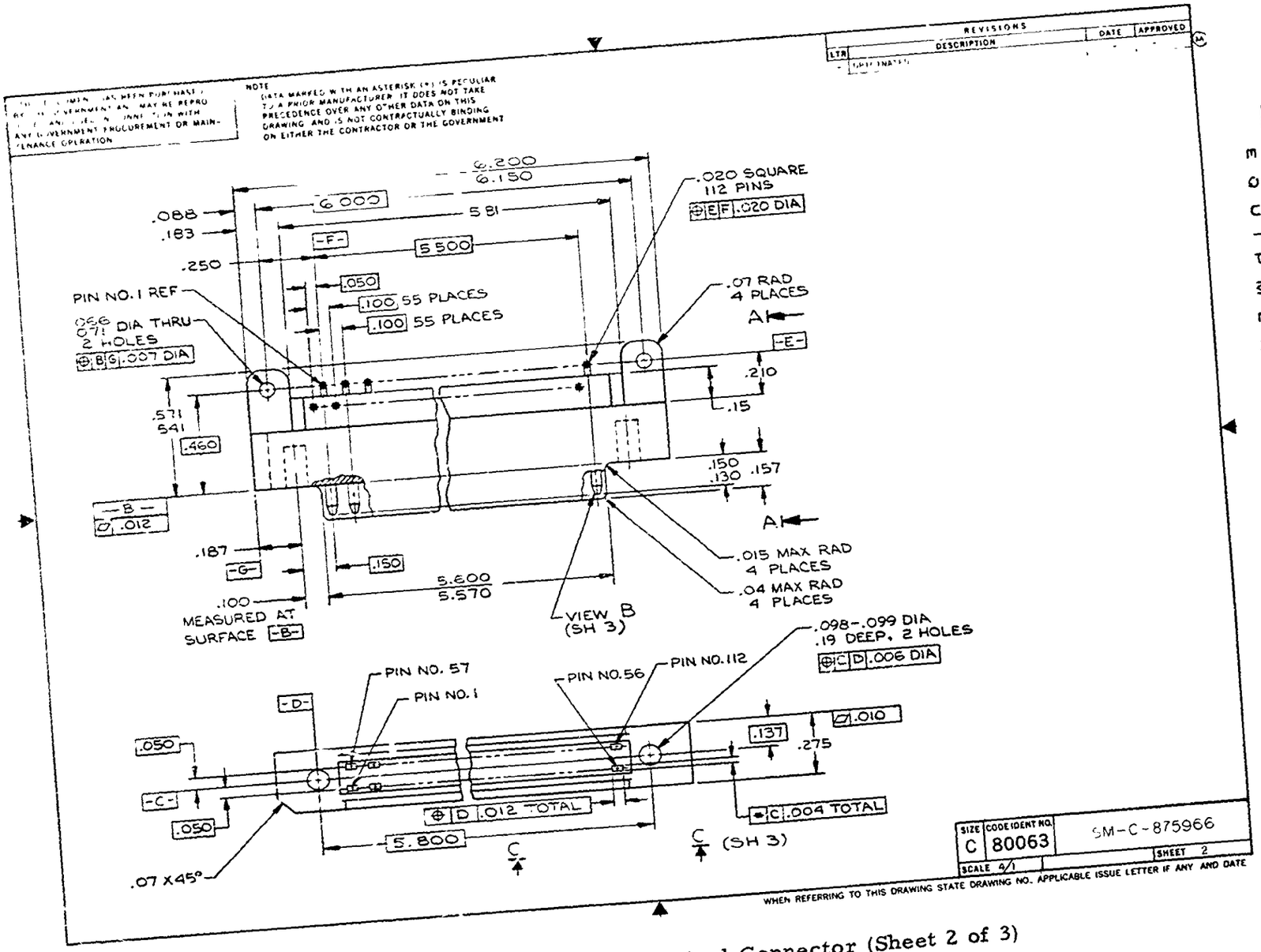


Figure 15-9. 112 Pin Electrical Connector (Sheet 2 of 3)

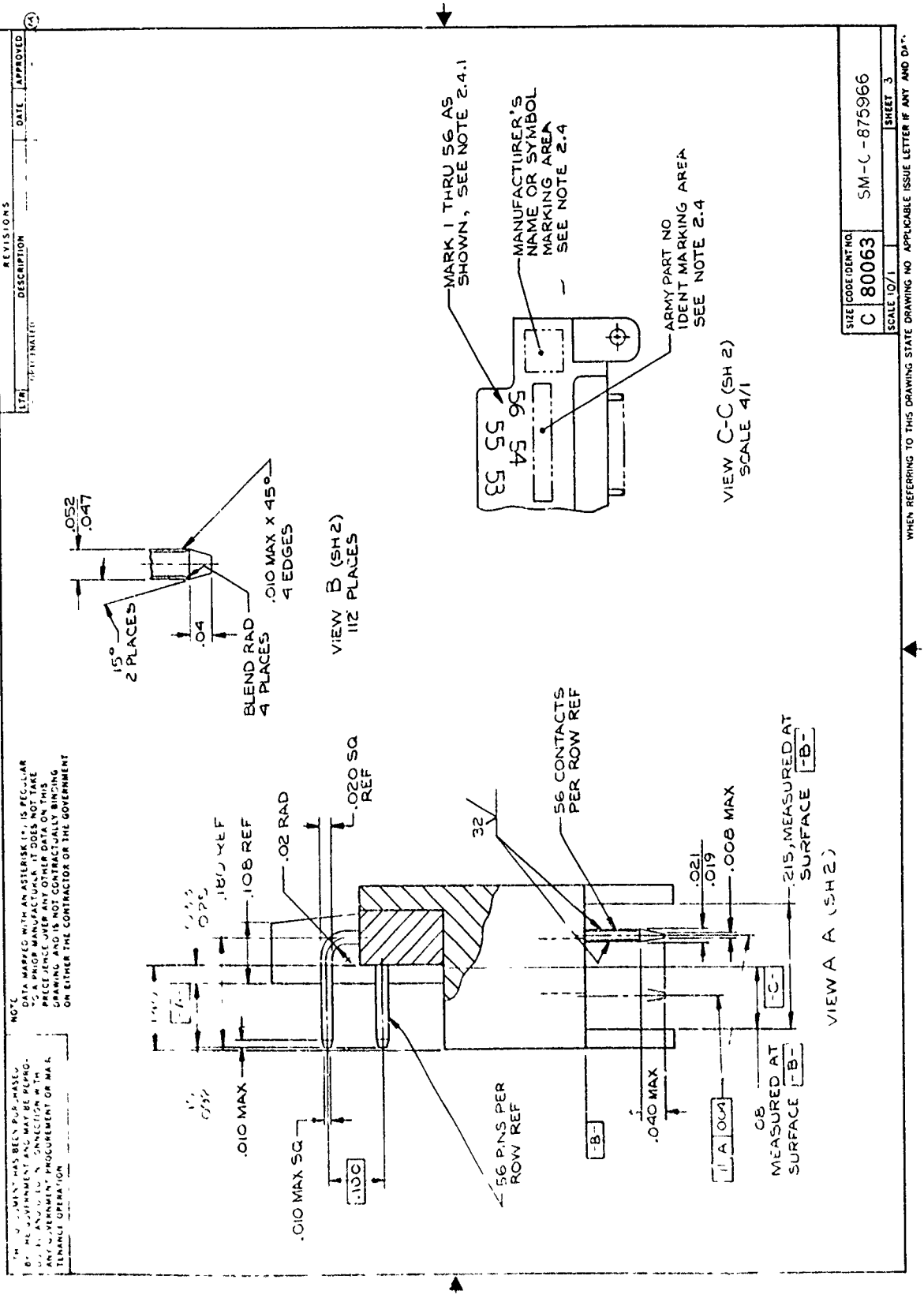


Figure 15-9. 112 Pin Electrical Connector (Sheet 3 of 3)

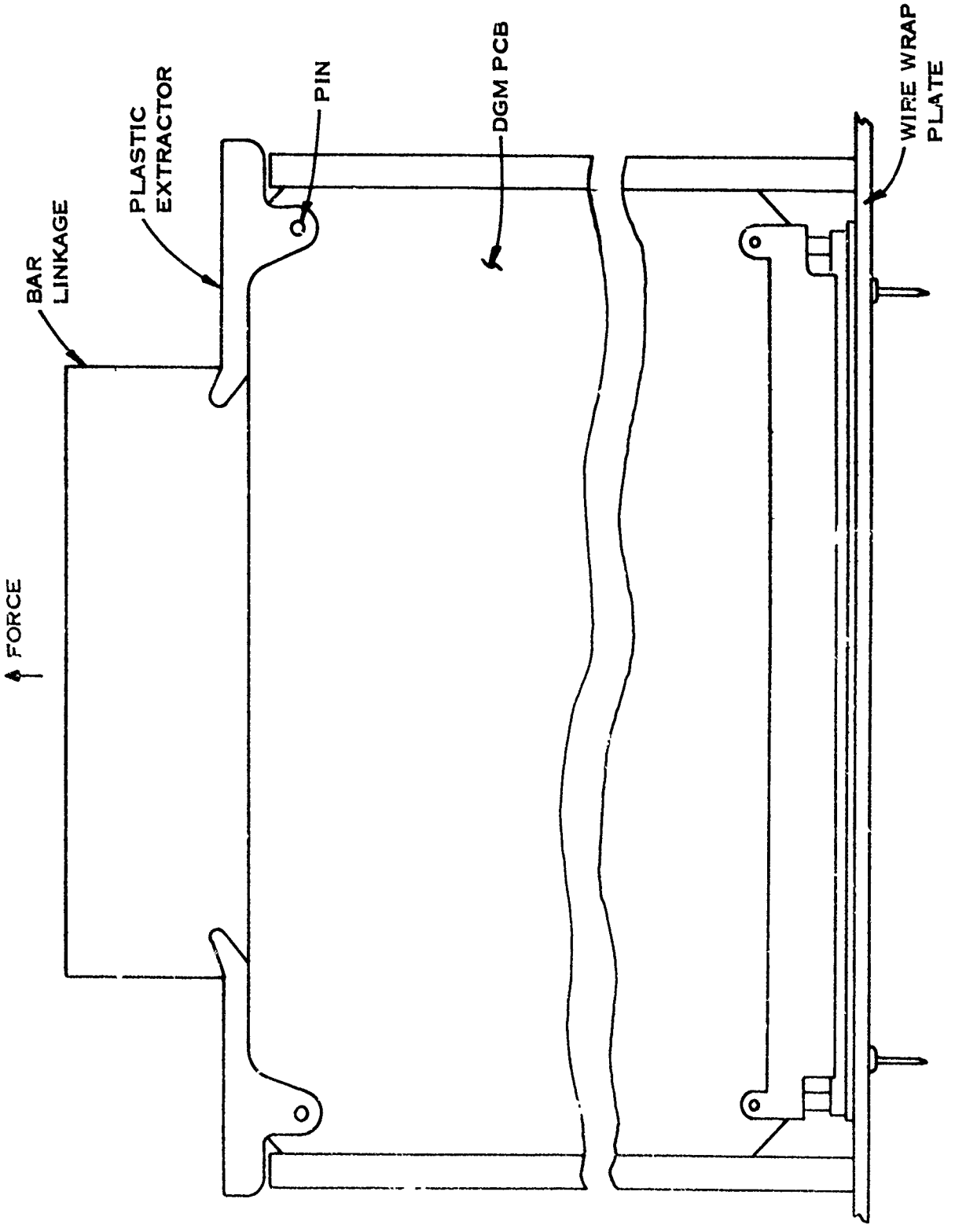


Figure 15-10. PCB Test Setup

15.1.2.2.2 Test Results (see Figure 15-11)

- Extraction Load

  Varies from 8 to 12 pounds.

- Ultimate Loads

  (1) Retaining/Pivot Pin Ejected: 256 pounds
  (2) PCB Tear-Out Failure: 303 pounds

15.1.2.2.3 Conclusion

- Extraction Loads

PCB extraction force of 8 to 12 pounds meets the requirements of MIL-STD-1472.

- Ultimate Loads

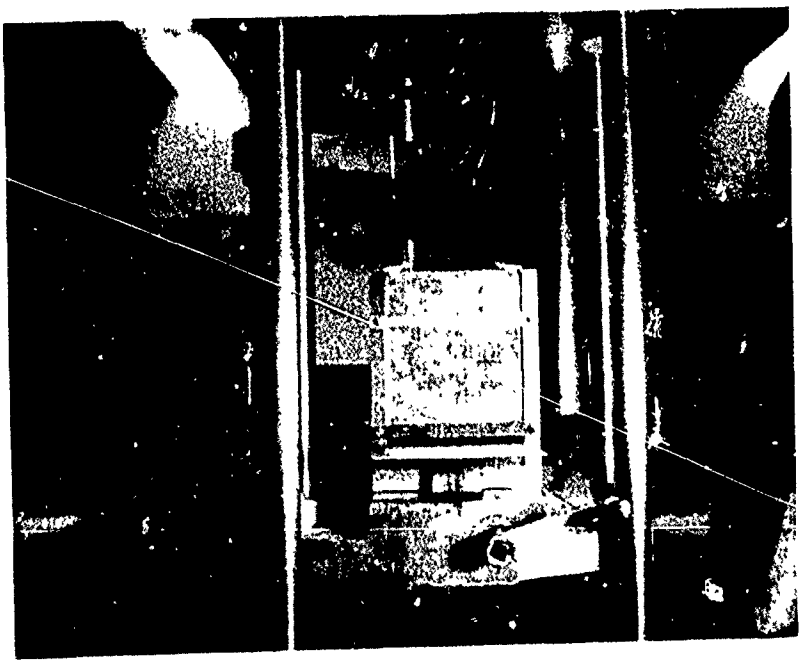
DGM plastic extractors have more than adequate strength including a large safety factor.

Primary failure mode (i.e., pin bends/ejects) is a desirable feature. In the event of misuse the pin fails, but the PCB is not damaged. Repair consists of replacing the pin.

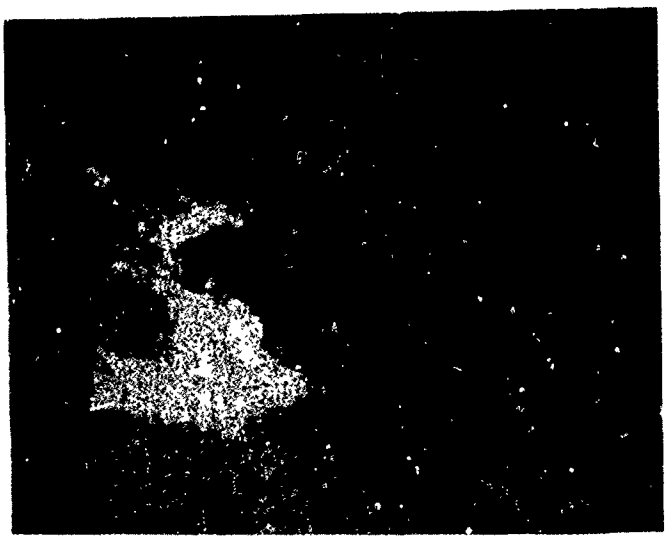
15.1.2.3 PCB Guide

The PCB guide system was selected primarily in an attempt to provide a thermal path from the PCB to the equipment case. The guides are Be Cu, rivited to a support plate which in turn is mounted to the equipment case via brackets and hardware. The guide assembly is aligned to the w/w plate connectors and provide mechanical support for the PCB during insertion and withdrawal.

Forward of the PCB guide is a nylon marker which provides initial alignment, coding, and marking surface for the identification of the proper PCB used in that location. The coding provision is a raised portion of the plastic marker which prohibits the erroneous insertion of a PCB 180 degrees from the proper insertion orientation (see Figure 15-12).

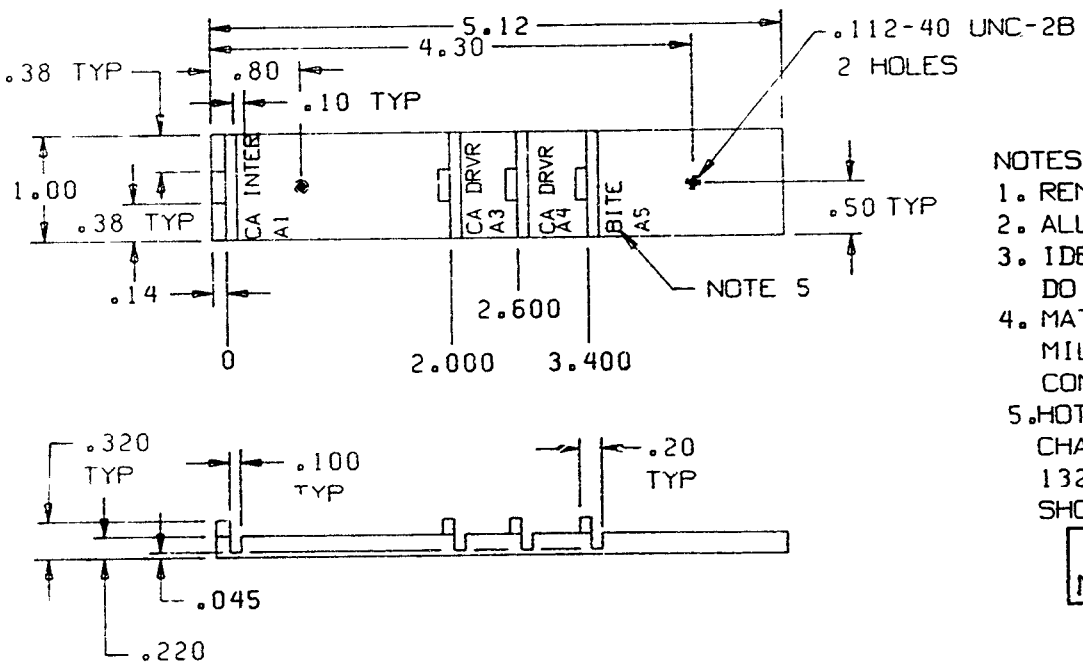


a. Extraction Test



b. PCB Failure

Figure 15-11. Test Fixture



NOTES:

1. REMOVE BURRS AND BREAK SHARP EDGES
2. ALL INSIDE CORNERS .010 R MAX
3. IDENTIFY PER MIL-STD-130. DO NOT MARK THE PART
4. MATERIAL: PLASTIC, MOLDING MIL-M-20693, TYPE III, COMPOSITION A, GRADE E
5. HOT DIE STAMP .09 HIGH BLACK CHARACTERS, GROUP I, PER MIL-M-13231. LOCATE APPROXIMATELY WHERE SHOWN.

THIS DRAWING IS MAGNETIC TAPE CONTROLLED

RAYTHEON COMPANY
EQUIPMENT DIVISION
RAYTHEON

Figure 15-12. Marker, Identification

15.1.2.4 Chart, PCB Locations

A marking and location system has been established for DGM which uses the forward surface of the PCB extractors, the marker strip forward of the PCB guides (see previous paragraphs), and a locator chart. The locator chart (see Figure 15-13) is a decal attached to the outside surface of the PCB cover which identifies all internal PCBs, their switches and functions including rate selections, and fault indicators. The decal is capable of being marked by grease pencil by the operator to identify the internal switch settings, frequency rates, or operating conditions without the removal of the cover. Each unique unit has its own PCB chart.

15.1.3 THERMAL DESIGN

15.1.3.1 Approach

Raytheon's approach to an acceptable thermal design of the DGM equipments is based on the development of necessary guidelines at critical points of hardware design and their verification on the basis of empirical data obtained from a thermal model simulating the thermal conditions within the units.

15.1.3.2 Preliminary Thermal Analysis

During the DGM Proposal Phase, Raytheon performed a preliminary thermal analysis using a computerized heat transfer program (HEATNET) and the CDC time-sharing Kronos 2 system. The results of this analysis was used as a guide to establish the basic design for the DGM equipments and to select parts/subassemblies. It is noted that this basic approach for analysis was used by Raytheon for the TD-1065 High Speed Serial Data Buffer developed under Contract DAAB07-73-C-0071, the results of which were within 3°C from predicted to actual measurements. The DGM shelter mounted equipments closely resemble the physical size, shape, partitioning and fabrication methods of the TD-1065. Therefore, the same basic thermal analysis could be applied to these equipments with a high degree of confidence in the results.

Other design techniques to be used were:

- Use of MIL-Grade, selected components, i.e., 125°C IC's; materials to withstand solar radiation effects and high-low temperature degradations.

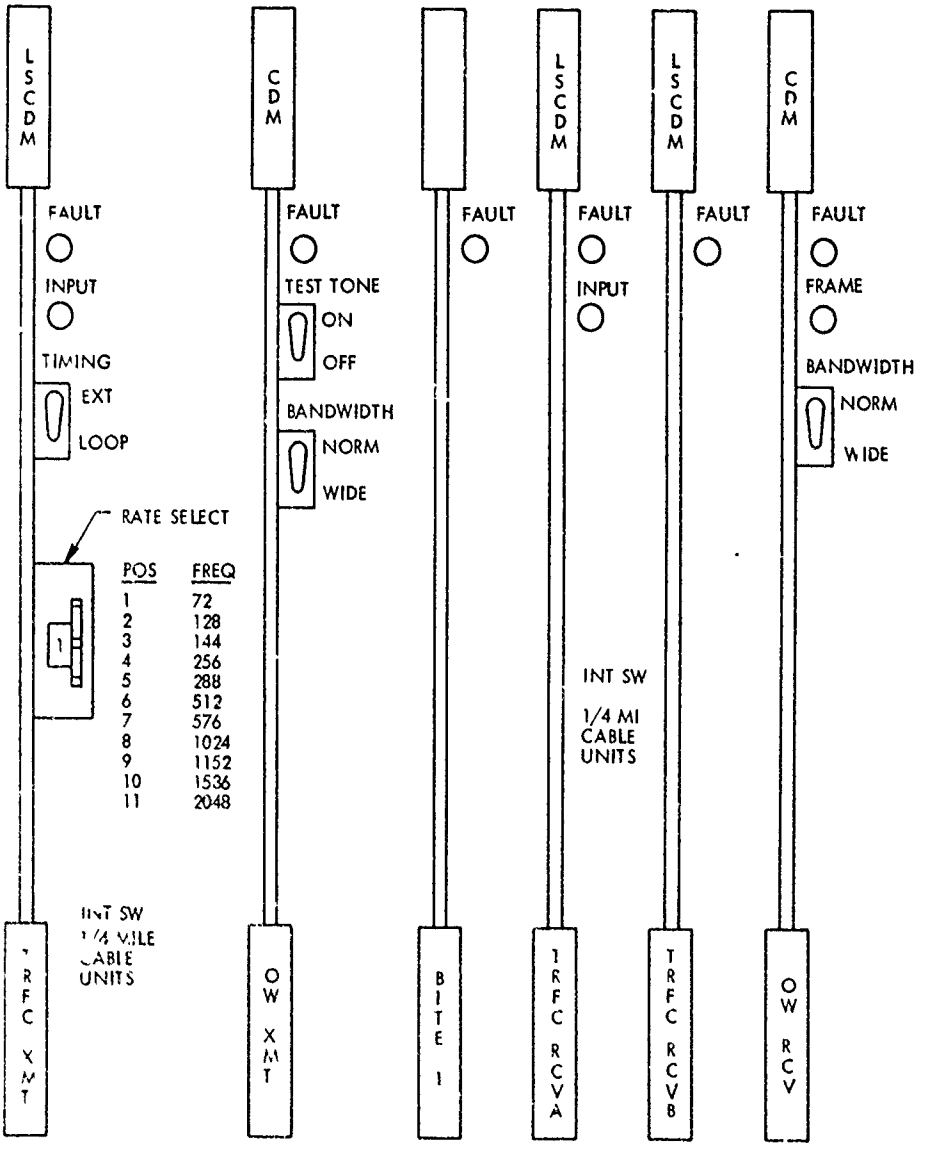


Figure 15-13. PCB Locator Chart Decal

- Closed loop convection cooling with direct-to-ambient conduction and convection cooling for PS.
- Metals and plastics selected for specific proven qualification at extreme low temperature; i.e., polycarbonate used has been recorded serviceable after 24 hour exposures at -80°F.
- Use of silicone rubber seals and gaskets rated not to set at levels as low as -70°F.

The preliminary thermal analyses were subsequently updated for the DGM shelter type units in an effort to establish thermal guidelines for use:

a. in the many tradeoff studies which were to be made

b. by the mechanical designer in selecting the configuration and the key parts (e.g., card guides) of the units

c. by the system engineer/circuit designer in "partitioning" the units.

Based on the analysis the following gross levels were established:

a. Case Power Dissipation Levels

1. Maximum: 85 watts
2. Design Goal: 65 watts

b. PCB Power Dissipation Levels

1. Maximum: 4 watts
2. Design Goal: 2.5 watts

In addition, three sets of curves (Figures 15-14 through 15-16) were developed to further guide the design engineers in the early phases of equipment design.

a. Total Internal Heat Dissipated

The three curves shown in Figure 15-14 are average internal air temperature versus heat dissipated for several different configurations.

1. Curve One (0% Conduction without openings in case) represents the upper boundary condition for a fully enclosed shelter unit and would be approached if little or no conduction was provided from the heat source to the case skin.

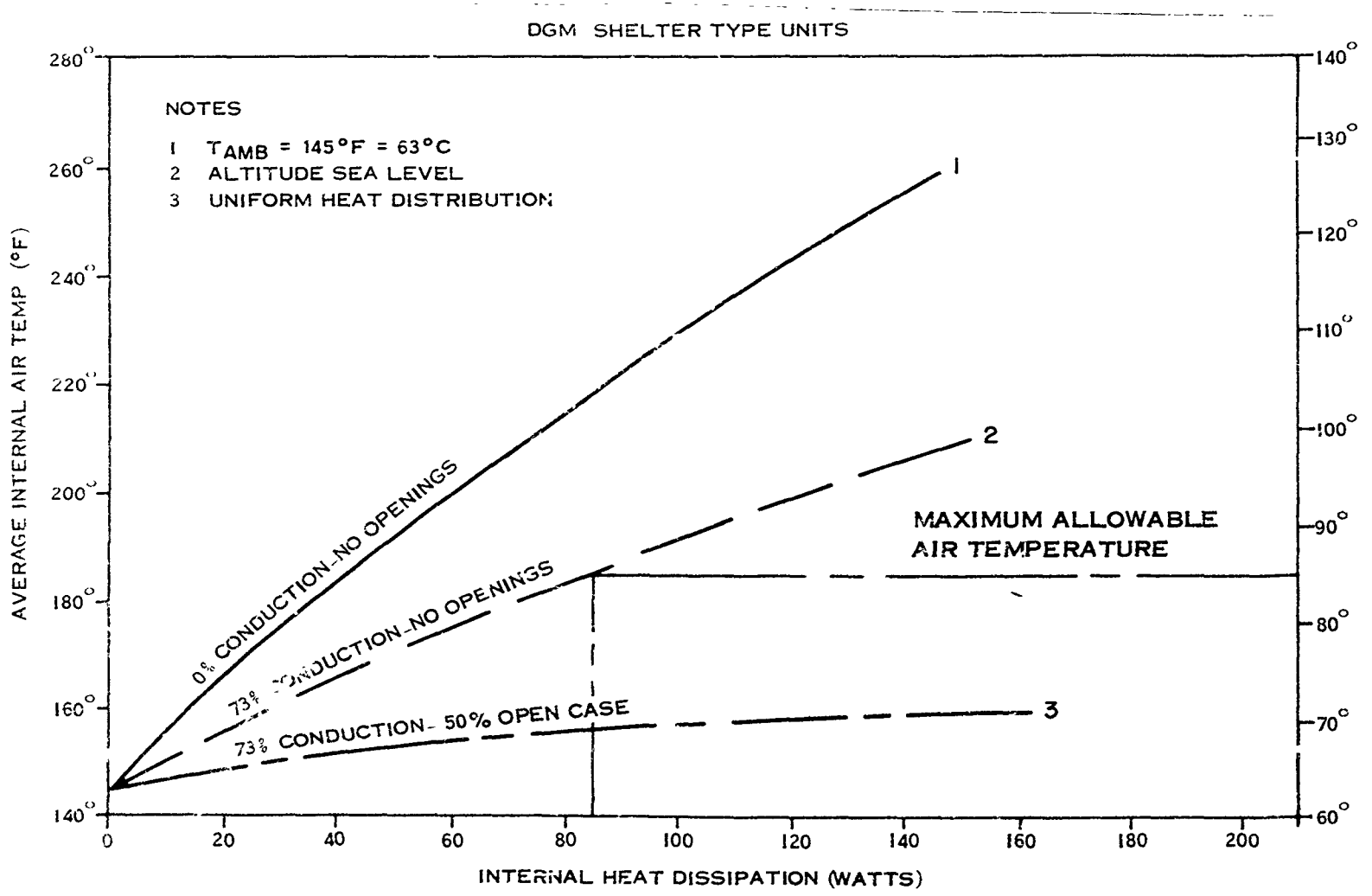


Figure 15-14. Average Internal Temperature vs. Internal Heat Dissipated

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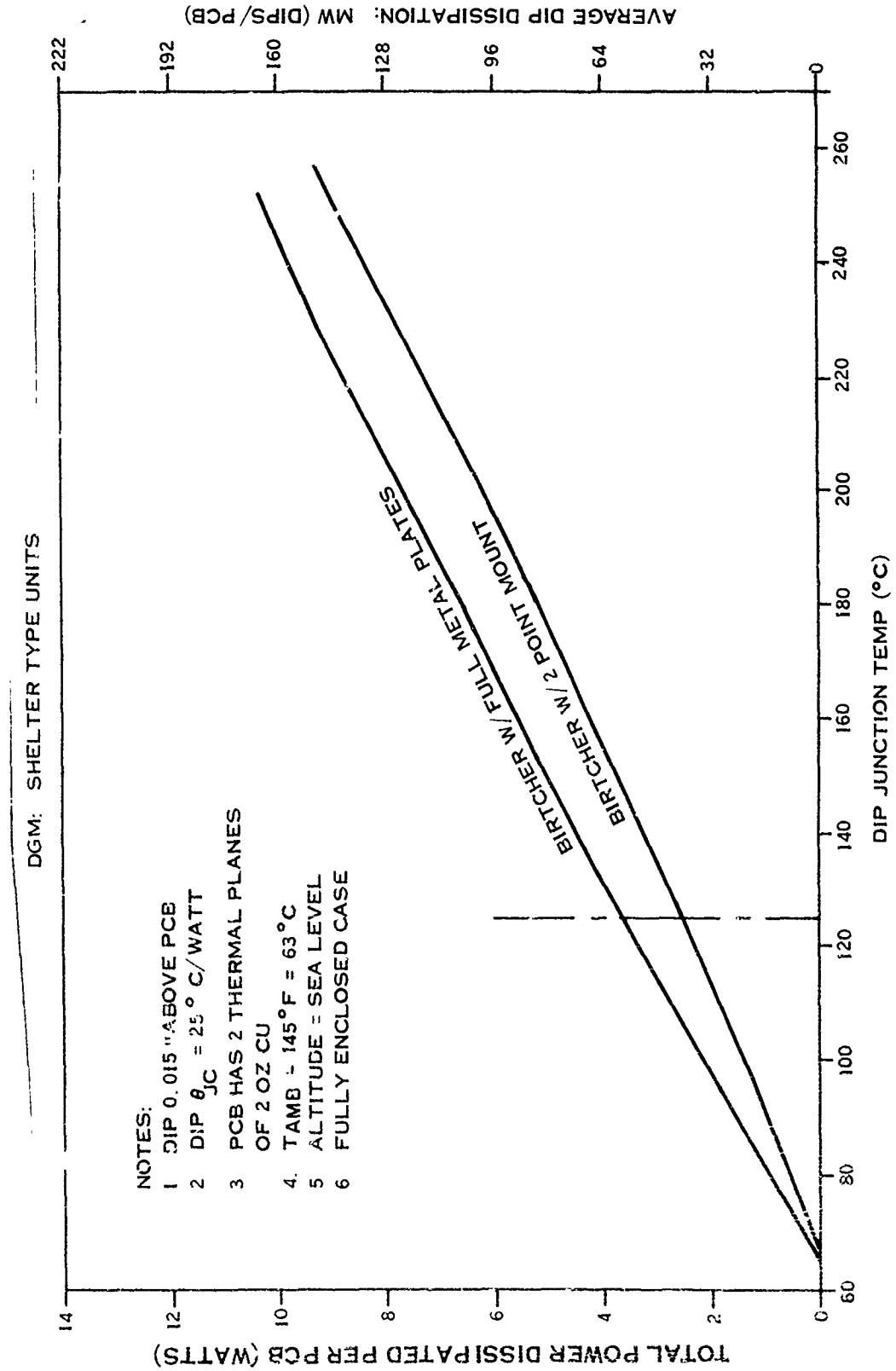


Figure 15-15. PCB and DIP Heat Dissipated vs. Junction Temperature

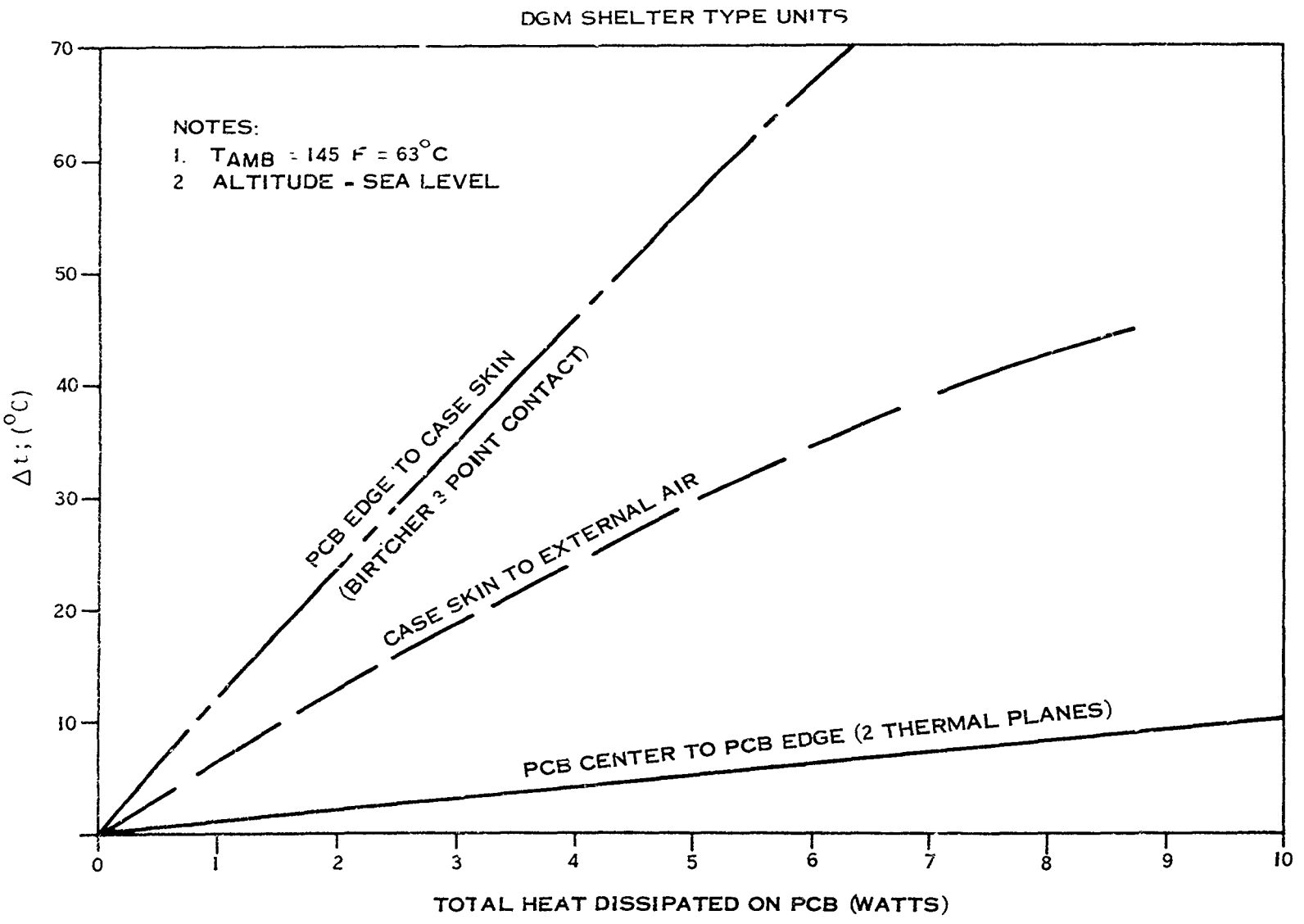


Figure 15-16. Temperature Difference vs. Total PCB Heat Dissipated

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2. Curve Two (73% Conduction without openings in case) represents the lower boundary condition for a fully enclosed shelter type unit and requires excellent conduction paths from the heat source to the case skin (e.g., use of thermal planes; conductive card guides; many contact points between the card guides and the case).

3. Curve Three (73% Conduction with 50% openings in case) is the same as Curve Two except for the top and bottom of the case being 50% perforated or 50% open to vertical air flow (natural effects only). This was considered a backup approach in the event we were forced to handle large heat loads. The principle disadvantage are the added costs to include openings which are EMI tight, and the EMI problem in general.

The absolute maximum internal air temperature, based on a rather quick review of some components and supplies was established at 100°C; however, at least at the outset 85°C was selected as the upper limit to be used as the design guide. Should we actually approach this level in the final design, careful review of all components was planned to insure satisfactory part selection/ equipment operation.

b. Printed Circuit Boards (PCB's)

The two curves shown in Figure 15-15 represent boundary conditions for the fully enclosed shelter unit. Assuming a maximum DIP junction temperature 125°C, total allowable power dissipation on a PCB was 4.0 watts or approximately 64 mW per DIP on the basis of a 61 DIP PCB.

The above condition assumed three PCB's located side-by-side 0.6-inch apart, with each PCB dissipating the same amount of heat (no lateral heat transfer). In special cases more than 4.0 watts per PCB could be handled by locating a "hot" PCB between two "cold" PCB's or "cold" surfaces. Similarly, the DIP (or several DIPs) which dissipates more than 64 mW may require special treatment such as an individual heatsink and/or a location facing a "cold" surface.

c. Temperature Difference versus PCB Heat Dissipated

The three curves shown in Figure 15-16 represent thermal impedances at different points of a PCB.

1. PCB Center to PCB Edge - This curve is relatively flat and indicates that the conduction from the center of the PCB to the PCB edge is excellent (due primarily to the two thermal planes, i.e., the voltage and ground planes). Not much total improvement will be achieved by reducing this impedance; therefore no further efforts were required in this area.

2. Case Skin to External Air - This is primarily a function of the case size and finish which are essentially beyond Raytheon control. No further effort was planned.

3. PCB Edge to Case Skin - This is a steep curve and accordingly represents the key to the thermal problem.

Careful attention to detail design/construction was indicated to maintain the power dissipation per PCB and IC within stated limits and to provide the necessary thermal conduction and convection paths required to retain junction temperatures below 125°C.

15.1.3.3 Shelter Equipments Characteristics

As a result of design progress since the completion of the Preliminary Thermal Analysis, it has been possible to update physical and thermal characteristics of the shelter equipments. The data used for design is tabulated in Tables 15-2 and 15-3.

In addition, worst case conditions projected within each of the units insofar as IC's are concerned have been identified and are given in Table 15-4.

The information so accumulated was subsequently used to determine the existence of any possible critical areas within the equipments from a thermal point of view. The procedure followed in and the results of this determination are discussed in paragraphs 15.1.3.4 through 15.1.3.6, inclusive.

15.1.3.4 Thermal Model

A thermal model was constructed to provide a means of verifying analytical results by actual measurements of prevailing temperatures at critical equipment points under different conditions of power dissipations within a unit.

TABLE 15-2

SHELTER EQUIPMENTS CONFIGURATIONS

Unit	Type	Case Dimensions in (H x W x D)	Number of PCB's	Power* Dissipation (watts)	Power Density (watt/in^3)
TGM	Shelter	8-1/2 x 17-1/4 x 12	11	73	0.04
GM	Shelter	8-1/2 x 17-1/4 x 12	13	65	0.035
RLGM/CD	Shelter	8-1/2 x 17-1/4 x 12	4	52	0.03
HSCDM	Shelter	8-1/2 x 17-1/4 x 12	6	56	0.03
LSCDM	Shelter	8-1/2 x 17-1/4 x 12	6	49	0.027
MGM	Shelter	14 x 17-1/4 x 12	25	154	0.088

*Total power dissipation for unit includes a 15 percent safety factor. Total power dissipation shown includes power dissipated on the power supply heatsink.

TABLE 15-3

SHELTER EQUIPMENTS POWER DISSIPATIONS

Unit	PCBs	Power Supply		Total Unit	Inside Unit
		Internal	Heatsink		
LGM(SYL)	19.8	25.1	25.1	70.0	44.9
MGM	100.1	27.0	27.0	154.1	127.1
GM	42.0	11.3	11.3	64.6	53.3
TGM	47.3	12.8	12.7	72.8	60.1
HSCDM	23.8	16.1	16.1	56.0	39.9
LSCDM	19 8	14.5	14.5	48.8	34.3
RLGM/CD	13.2	19.4	19.3	51.9	32.6

Note: Based on limited measurements to date, power estimated values shown above are conservative by approximately 15 percent.

TABLE 15-4

WORST CASE POWER DISSIPATION PER PCB

Unit	Number of PCB's	Highest Power Dissipation among PCB's		Highest Power Dissipation among IC's	
		PCB	Watts	IC	mW
TGM	11	Microcontroller SM-D-875945	6.71	54LS175	60
GM	13	Dipulse SM-D-875971	4.09	54S86	315
RLGM/CD	4	Cable Interface SM-D-876258	3.60	-	-
HSCDM	6	Traffic Rec B SM-D-876004	8.01	54S163	635
LSCDM	6	Traffic Rec B SM-D-876265	4.38	54S163	635
MGM	25	Format Generator SM-D-875959	8.89	54S163	635

An actual TGM case was modified by removing its top and bottom surfaces and replacing them with flat sheets of aluminum chromated on one side and painted black on the other. This modification made it possible to determine any possible benefit that could be derived from altering the surface finish.

Removing the top surface also provided a means to simulate the larger MGM case by the addition of an upper section to the basic case.

Heat sources were located with the thermal model such as to make it possible to vary the heat distribution and its amount within the unit, with thermocouples located at critical points to measure temperatures prevailing at them, including those IC's located at different points of a PCB and dissipating anywhere from 100 to 335 mW each, with and without heatsinks. Data was taken and recorded in the following pages.

The results were subsequently plotted in Figures 15-17 through 15-20, inclusive.

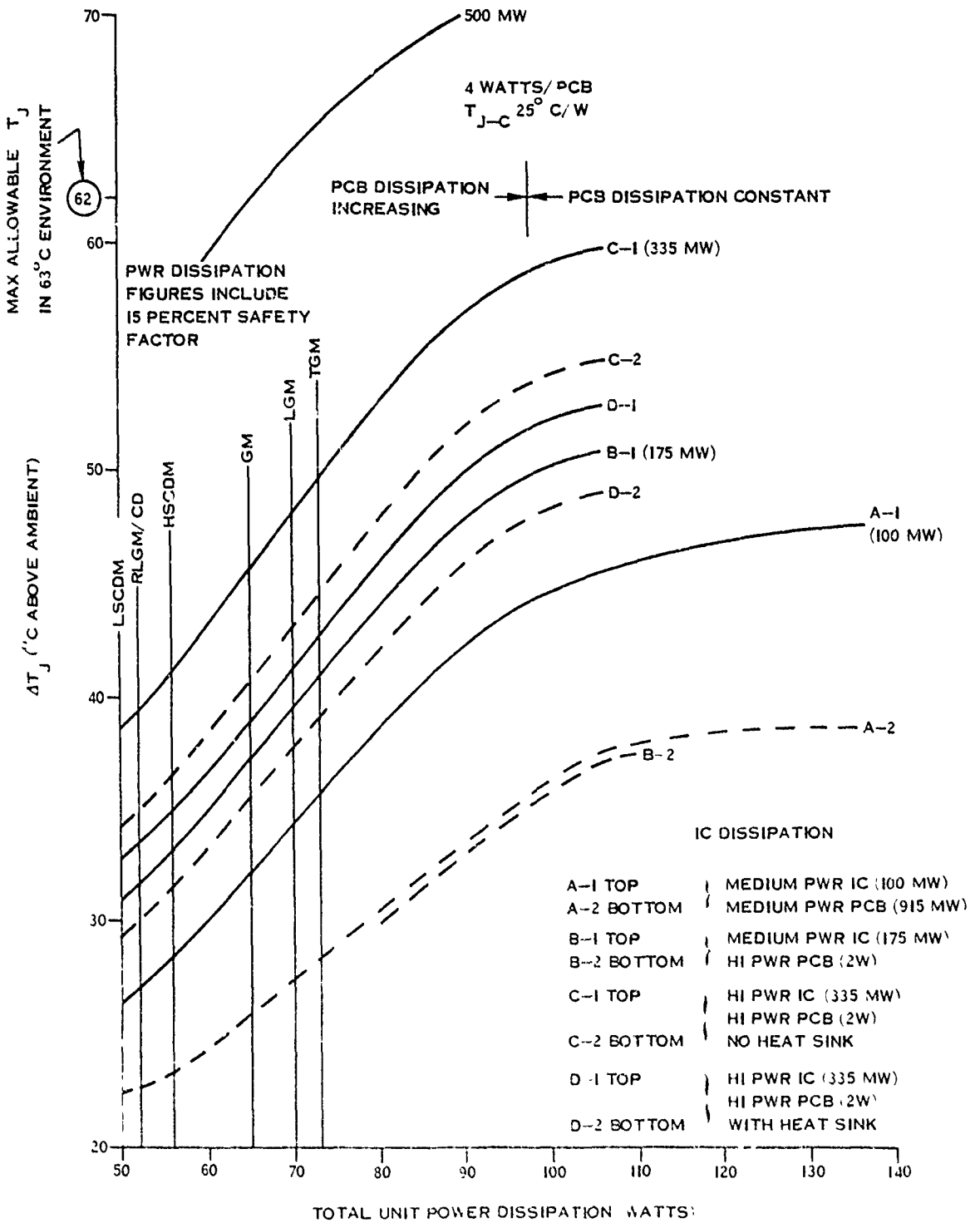


Figure 15-17. IC Junction Temperature Versus Unit Power Dissipation

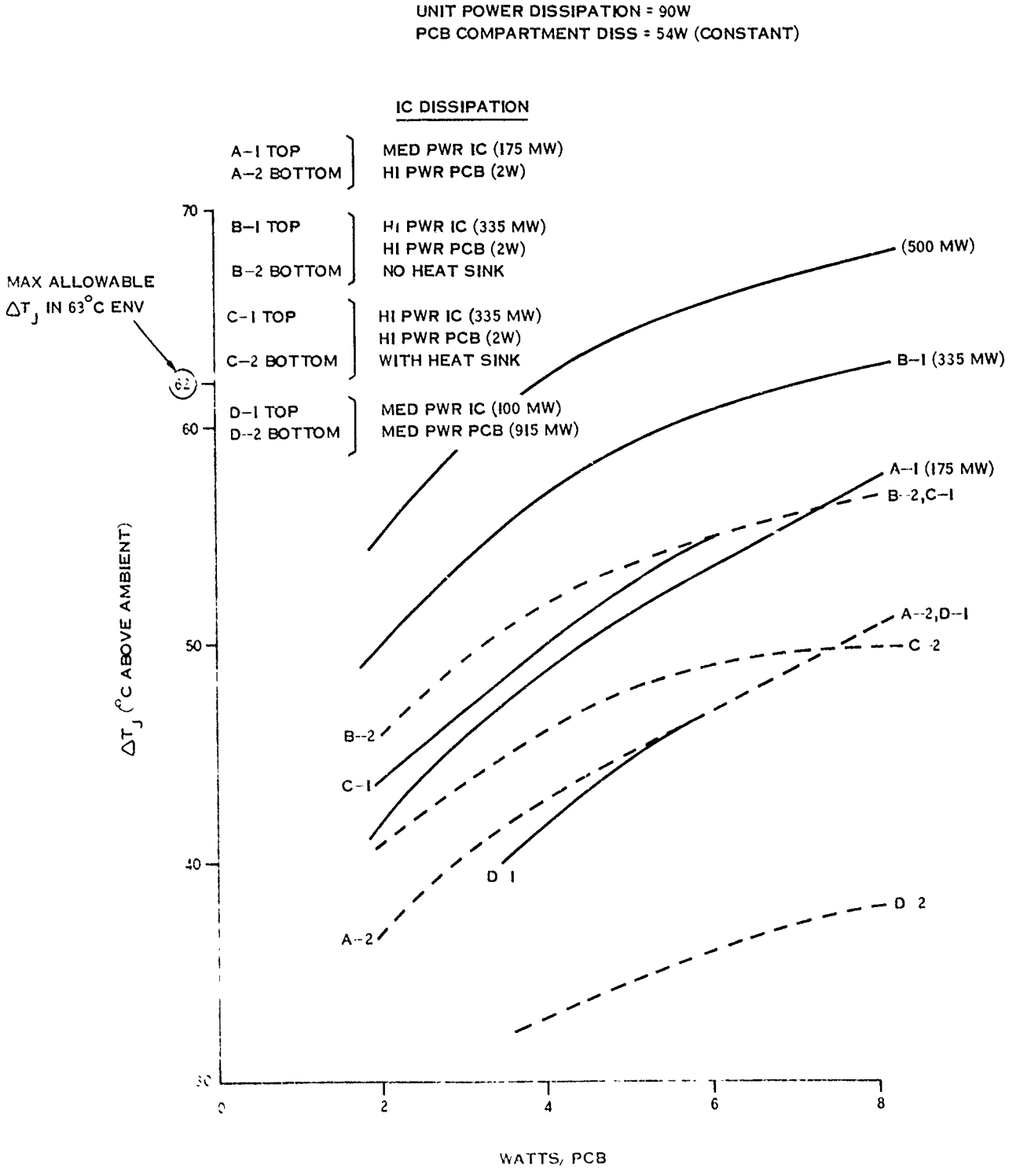


Figure 15-18. IC Junction Temperature Versus PCB Power Dissipation

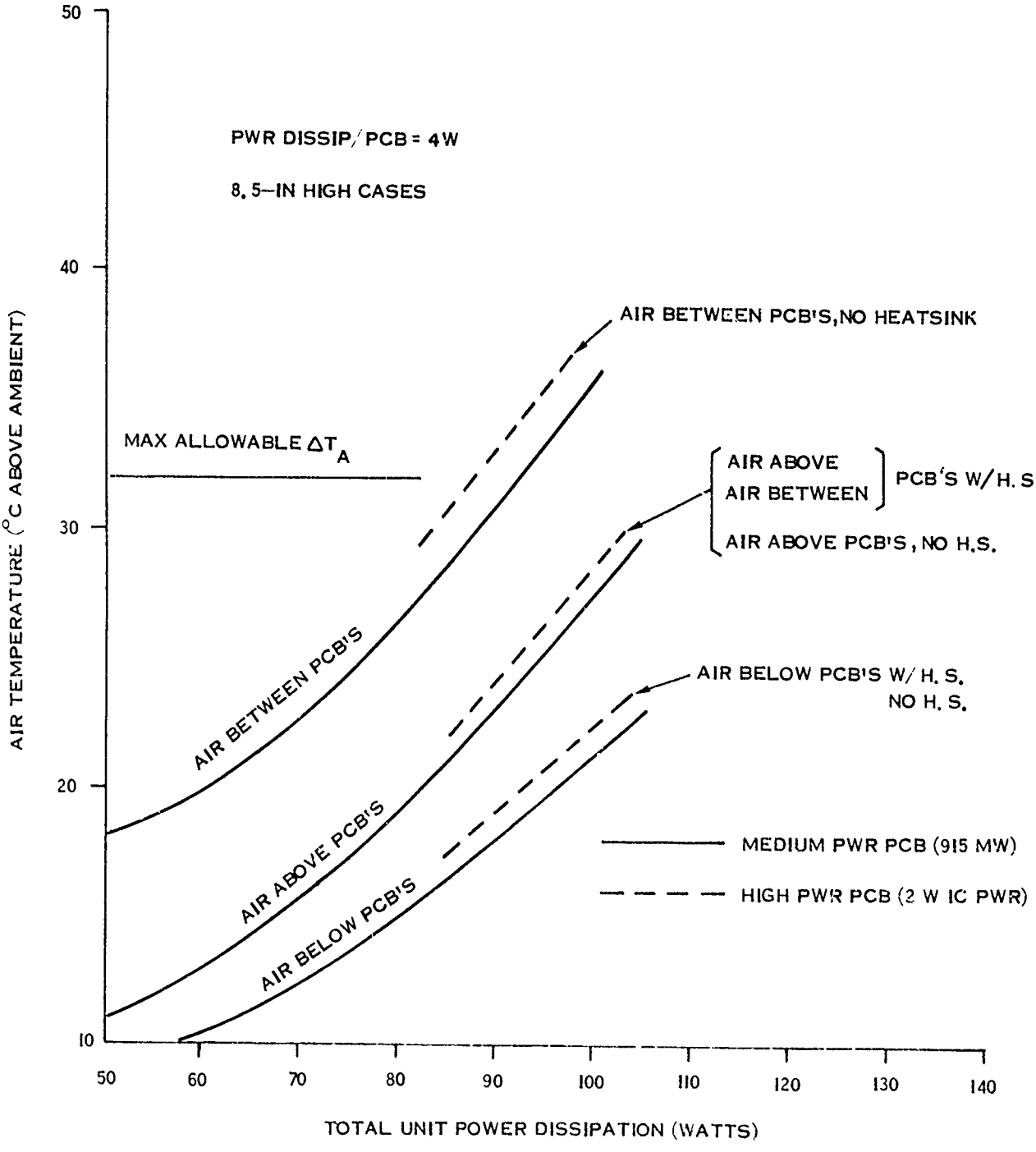


Figure 15-19. Internal Air Temperature Versus Unit Power Dissipation (Power Dissipation/PCB = 4W)

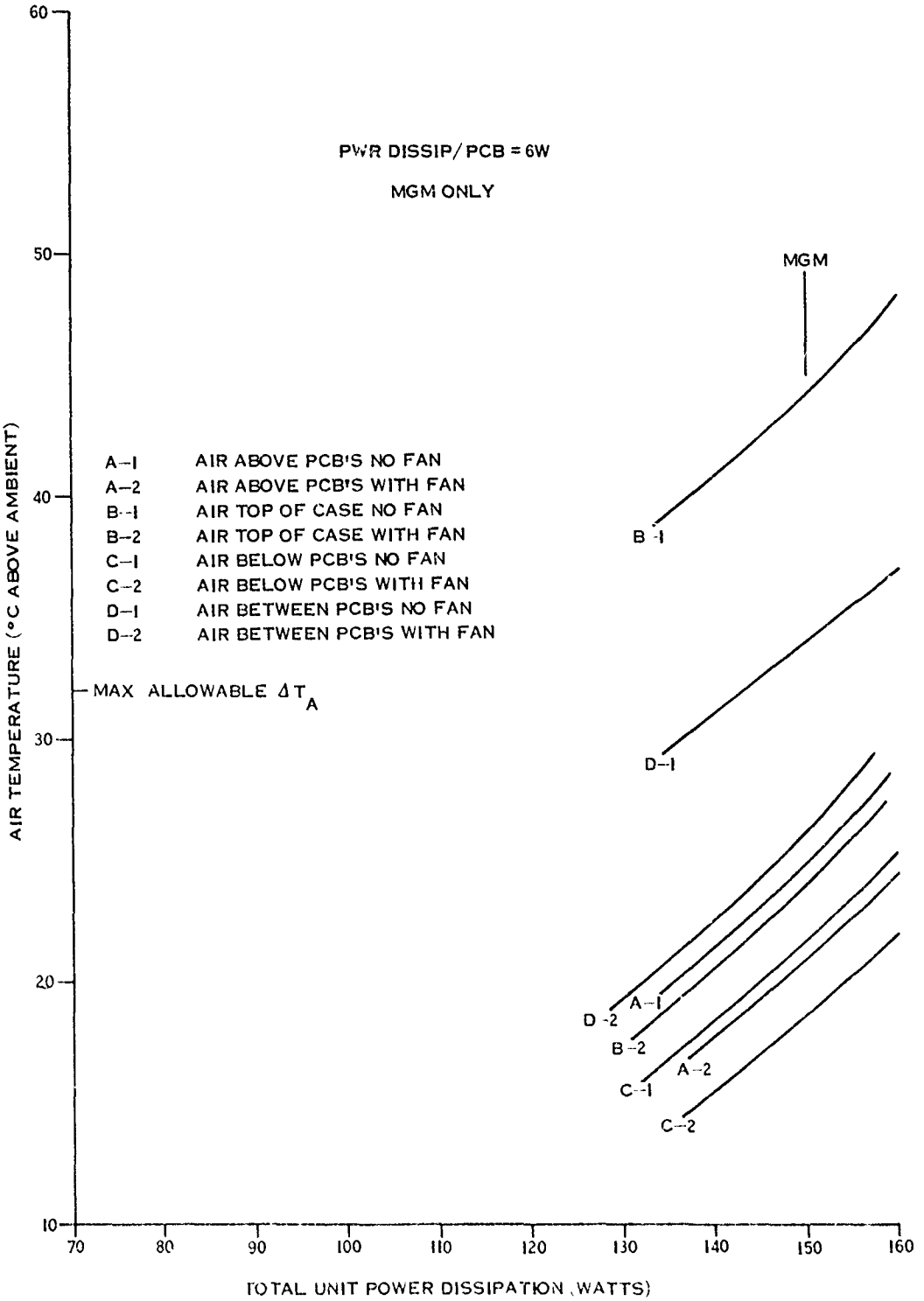


Figure 15-20. Internal Air Temperature Versus Unit Power Dissipation (Power Dissipation/PCB = 6W)

15.1.3.5 Thermal Characteristics of Shelter Equipments

The results of the thermal experiments were then interpreted for the conditions projected for the DGM shelter equipments, with total unit dissipations taken from Table 15-3 and worst case conditions from Table 15-4.

The results plotted in Figures 15-21 and 15-22, and identifying expected critical junction temperatures under these worst case conditions, show all of them falling below the allowable maximum of 125°C, provided heatsinks are added in high power applications.

The results also indicated the necessity of using a fan with the MGM or else the junction temperature may rise as much as 13°C to an unacceptable figure in excess of the limit. They also suggest that, as long as a fan is used as well as heatsinks in critical locations, the internal power dissipation could go up another 10 to 15 watts without causing the junction temperature to exceed the allowable limit.

It should be noted that power dissipations assumed provided a 15 percent safety factor.

15.1.3.6 Conclusions

It can be safely stated that the design of the 8.5-inch high units is sound from a thermal point of view and that, with selective use of heatsinks, design and performance goals will be attained.

It also became clear that a low noise, low power fan had to be used inside the MGM located in the compartment above the PCB's to circulate the air. In addition, buffers were provided so as to direct the coolant air more efficiently past identified hot spots.

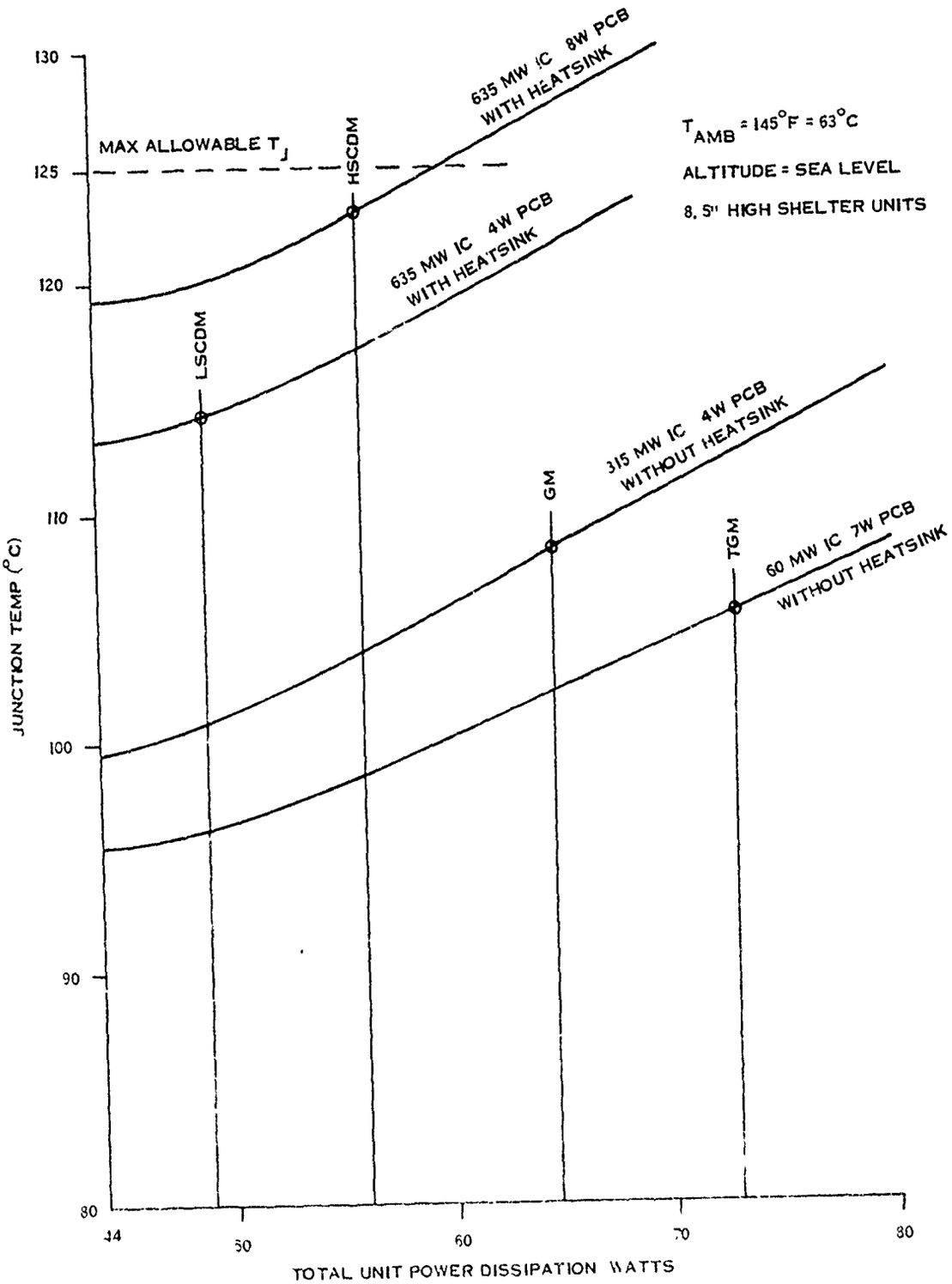


Figure 15-21. Junction Temperature Versus Unit Power Dissipation (8.5" High Shelter Unit)

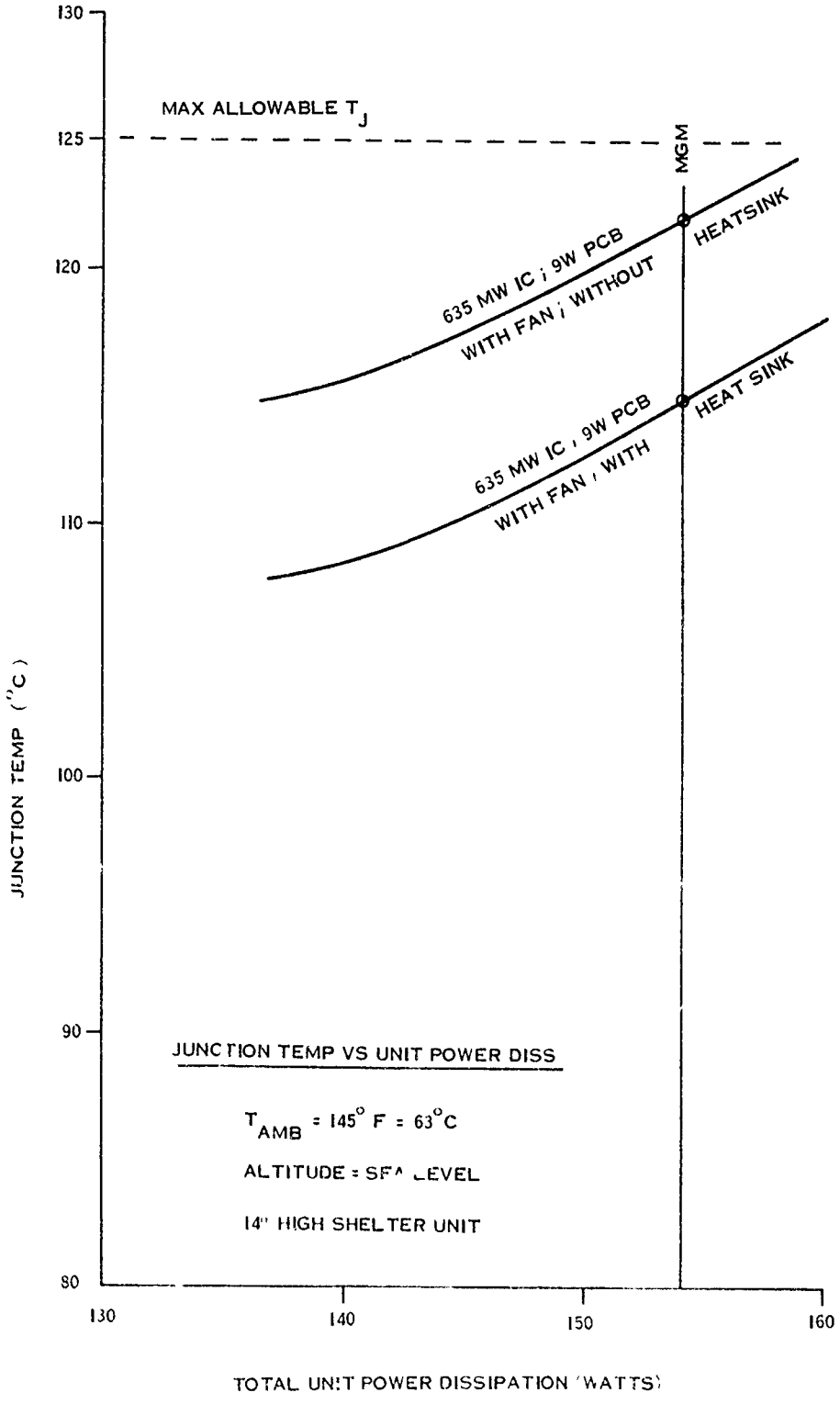


Figure 15-22. Junction Temperature Versus Unit Power Dissipatio. (14" High Shelter Unit)

15.1.4 SHOCK AND VIBRATION

15.1.4.1 General

There are two major areas of concern when considering the design of the equipment to survive vibration and shock: dynamic stresses in the structure, and response of the structures and enclosed elements. Dynamic stresses always represent potential problems since material fatigues at stresses well below the yield strength of the mechanical/electrical part or wire connection. Also, excessive deflections between mating or adjacent parts due to resonant response can cause interference and/or subsequent damage.

Raytheon has acquired considerable experience over the years with this type of equipment and has developed guidelines and standards to be used to achieve a lightweight vibration and shock-resistant design. These guidelines and a brief discussion of each are presented below:

a. Natural frequencies of major structural items to be as high as practical with 60 Hz being the minimum. It is virtually impossible to design manportable/transportable equipment of this type which has no resonances within the range of service frequencies (5 to 200 Hz). Within the constraints of size and weight, the frequency should be as high as possible with the major structural elements having natural frequencies greater than 60 Hz.

b. Resonance conditions were analyzed and the stress levels were maintained at safe working levels. Static limit load factors are applied to static structural analysis so that the resulting stresses do not exceed the yield strength of the material and thereby ensure that the equipment will function in the dynamic environment.

The limit load factors were determined from the vibration and shock requirements of MIL-STD-810 and from an estimate of damping in the structure.

c. Printed circuit board natural frequencies must be at least 1.4 times greater or less than the predominate chassis natural frequency. Parts are located on the board so as to minimize the effects of the part weight (i.e., heavy parts near edges and corners). Relatively large parts (filters, equalizers, etc.) are mounted to the board with threaded fasteners. Relatively small parts (resistors, capacitors, etc.)which weight more than 1/2 ounce are "strapped" to the board so as not to depend upon their leads for support.

d. Cantilevered brackets are to be avoided whenever possible. If they must be used, they are to be carefully designed and analyzed so as to achieve an extremely high natural frequency (200 Hz design goal).

Protective features such as bumpers or mechanical extensions are used to preclude the damage to any part during servicing, handling, or shock. Individual subassemblies also feature protective elements and careful placement within the outline of the subassembly such that the delicate components are protected by the structure, "roll over" handles, or by other components which can take rough handling without damage.

Knobs, connectors and hardware are recessed within the structure for protection. Any protrusion from the basic case/chassis is limited to rack mounting angles and hook-up cables. Structures and protective features are designed sufficiently rugged to withstand rough handling and normal servicing conditions.

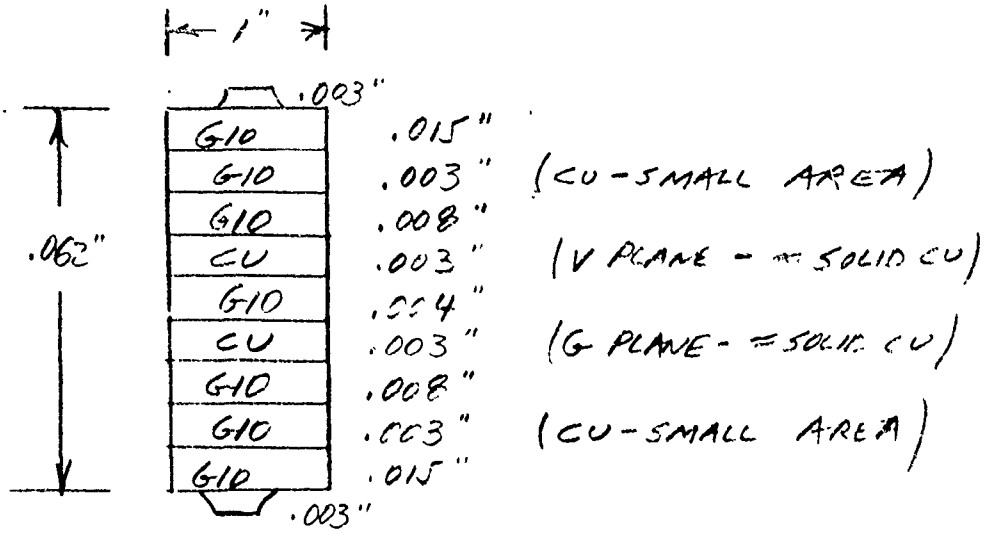
15.1.4.2 Printed Circuit Board Analysis

An analysis has been prepared to determine the stress levels and the maximum displacements for the standard printed circuit boards used in the Shelter Mounted DGM units. Results are given below and the detailed analysis is given in the succeeding pages.

Natural Freq:	Displ. Vibration Conditions: 0.061 in.
Displ. 15 g shock: 0.074 in.	Margin of Safety: 3.14 minimum

OGM STANDARD P.C. BOARD (AEL-SK

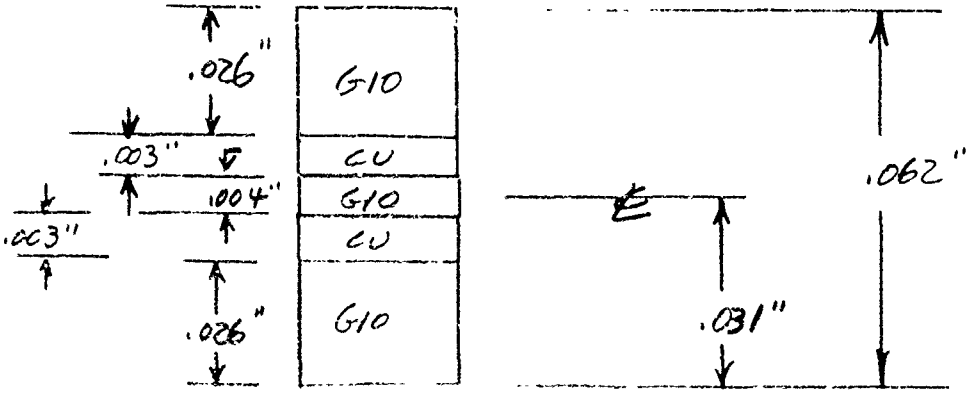
SECTION PROPERTY (MLB) – NO SCALE



FOR G10 $E = 1.85 (10)^6$ PSI

FOR CU $E = 17.0 (10)^6$ PSI

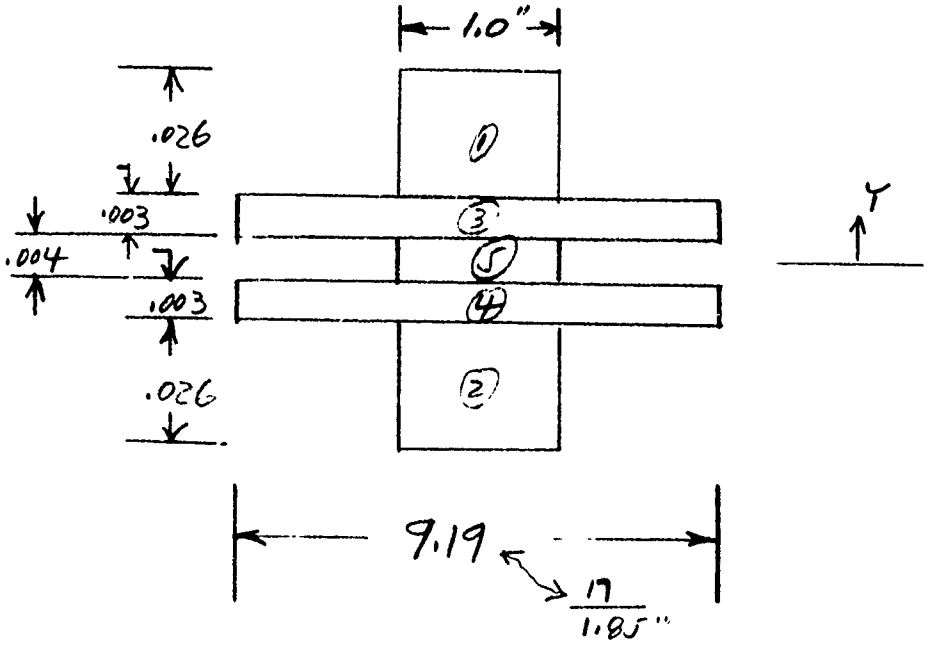
EQUIVALENT SECTION



FORM NO. 48-0380

CALC Horrar | REV | DATE | CLASS'N.

TRANSFORMED SECTION (IN TERMS OF GIC)



	A	Y	AY	$AY^2(10)^6$	$I_{ox}(10)^6$
①	.026	+.018		8.424	1.4647
②	.026	-.018		8.424	1.4647
③	.02757	+.0035		.3377	.0207
④	.02757	-.0035		.3377	.0207
⑤	.004	0	0	0	.0053
	.11114		0	17.5234	2.9761

$$I = |17.5234 + 2.9761|(10)^{-6} = 20.50(10)^{-6} \text{ IN}^4/\text{IN}$$

$$EI = (1.85)(20.50) = 37.925 \text{ LB-IN}^2/\text{IN}$$

$$f_{b_{GIC}} = \frac{M(.031)}{(20.50)(10)^{-6}} = 512(M) \quad (M = \text{IN-LB/IN})$$

$$f_{b_{CU}} = \frac{M(.005)(17)}{(20.50)(10)^{-6}(1.85)} = 2241(M) \quad (M = \text{IN-LB/IN})$$

CALC. Hannan | REV | DATE | CLASSIF.

FORM NO. 48-0380 RAYTHEON

SOLID G10 SECTION

$$I = \frac{(.062)^3}{12} = 19.86(10)^{-6} \quad IN^4/IN$$

$$EI = (1.85)(19.86) = 36.74 \quad 16\text{-}IN^2/IN$$

$$f_{b\,G10} = \frac{(M)(.031)}{(19.86)(10)^{-6}} = 1561(M) \quad (M = IN\text{-}lb/in)$$

LET $\varepsilon_{cu} = \varepsilon_{G10}$ (AT PAD AREAS)

THEN

$$f_{t_{cu}} = (f_{b_{G10}})\left(\frac{E_{cu}}{E_{G10}}\right)$$

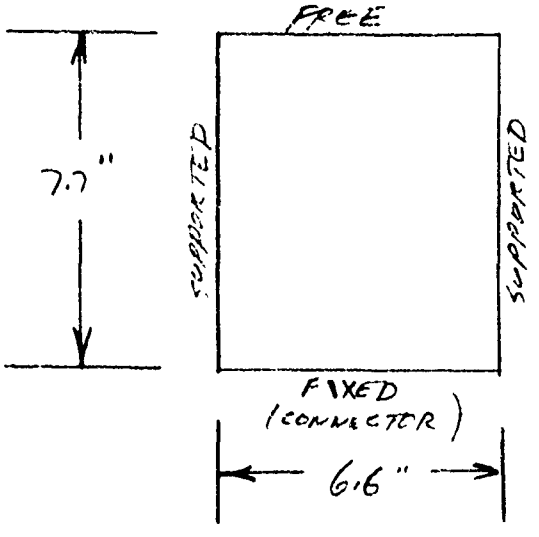
$$f_{t_{cu}} = \left(1561\right)\left(\frac{1.7}{1.85}\right)(M) = 14,344(M)$$

FORM NO. 48-0380

CALC. Horra | REV | DATE | CLASSIF.

f_N MODE 2

$\mu = .12$ G10



$W_T = 300$ GRAMS

$a = 6.6"$

$b = 7.7"$

$$D = \frac{Et^3}{12(1-\mu^2)} = \frac{(EI)_{G10}}{(1-\mu^2)}$$

$$D = \frac{37.925}{(1-.12^2)} = 38.48 \quad \text{lb-in}$$

$$\rho = \frac{W}{gA} = \frac{(300)}{(453.6)} \Big/ (386)(6.6)(7.7) = 0.00003372$$

$$f_N = \frac{\pi}{2}\left[\frac{D}{\rho}\left(\frac{1}{a^4} + \frac{.608}{a^2b^2} + \frac{.126}{b^4}\right)\right]^{1/2}$$

RAYTHEON FORM NO. 48-0380

CALC. Hamar | REV | DATE | CLASSIF.

f_N MODEL (CONT.)

$$f_N = \frac{\pi}{2}\left[\frac{38.48}{.00003372}\left(\frac{1}{6.6^4} + \frac{.609}{6.6^2 7.7^2} + \frac{.114}{7.7^4}\right)\right]^{1/2}$$

$$f_N = 47.4 \text{ Hz}$$

CONSIDER 3 EDGES SUPPORTED & RUBBER EDGE FREE

$$f_N = \frac{\pi}{2}\left(\frac{D}{\rho}\right)^{1/2}\left(\frac{1}{4b^2} + \frac{1}{a^2}\right)$$

$$f_N = \frac{\pi}{2}\left(\frac{38.48}{.00003372}\right)^{1/2}\left[\left(\frac{1}{4\times 7.7^2}\right) + \frac{1}{6.6^2}\right]$$

$$f_N = 45.6 \text{ Hz}$$

CONSIDER 4 EDGES SIMPLY SUPPORTED

$$f_N = \frac{\pi}{2}\left(\frac{D}{\rho}\right)^{1/2}\left(\frac{1}{a^2} + \frac{1}{b^2}\right)$$

$$f_N = \frac{\pi}{2}\left(\frac{38.48}{.00003372}\right)^{1/2}\left[\left(\frac{1}{7.7^2}\right) + \left(\frac{1}{6.6^2}\right)\right]$$

$$f_N = 66.8 \text{ Hz}$$

RAYTHEON FORM NO. 45-4380

CALC. Horton | REV | DATE | CLASSIF.

f_N Modes (cont.)

3 EDGES SUPPORTED 1 EDGE FREE FIXED

$$f_N = \frac{\pi}{2}\left[\frac{D}{\rho}\left(\frac{2.40}{b^4} + \frac{2.32}{a^2 b^2} + \frac{1}{a^4}\right)\right]^{1/2}$$

$$f_N = \frac{\pi}{2}\left[\frac{38.48}{.00003372}\left(\frac{2.45}{7.7^4} + \frac{2.32}{\{7.7^2\}\{6.6^2\}} + \frac{1}{6.6^4}\right)\right]^{1/2}$$

$$f_N = 77.3 \text{ Hz}$$

RAYTHEON FORM NO. 48—0380

CALC. | REV | DATE | CLASSIF.

f_N SUMMARY

CASE	f_N (Hz)
GUIDES SUPPORTED SCANNER FIXED RUBBER FREE	47.4
GUIDES SUPPORTED SCANNER SUPPORTED RUBBER FREE	45.6
ALL EDGES SUPPORTED	64.6
3 EDGES SUPPORTED SCANNER FIXED	77.3

BEST ESTIMATE)

$f_N \simeq 60$ Hz

CALC. Horio. | REV | DATE | CLASSIF.

RAYTHEON FORM NO. 4K-0380

[illegible]

VIBRATION

[illegible] 5 [illegible] - 5 Hz (CYCLE)

[illegible]

5 ½ [illegible] PER AXIS

SHOCK

15 G'S HALF SINE 11 MS PULSE

3 SHOCKS IN A AXIS

[illegible]

MIL-STD-810B, METHOD 516.1
PROC. V.

[illegible] 516.1 PROC. 2

RESPONSE LOADINGS

VIBRATION

$Q = 15$

$N = (1.5)(15) = 22.5$ G's

SHOCK

$Q = 1.8$

$N = (1.8)(15) = 27.0$ G's

RAYTHEON FORM NO. 48-0380

CALC. Harron | REV | DATE | CLASSIF

DYNAMIC BENDING MOMENT

$$\sigma_0 = \frac{W G_{out}}{a b}$$

$$\sigma_0 = \frac{\left(\frac{300}{453.6}\right)(27)}{(7.7)(6.6)} = 0.3514 \quad lb/in^2$$

$$\gamma = 0.12 \quad (G10)$$

$$M = \frac{\sigma_0 \left[\frac{\gamma}{(7.7)^2} + \frac{1}{(6.6)^2}\right]}{\pi^2 \left[\frac{1}{(7.7)^2} + \frac{1}{(6.6)^2}\right]^2}$$

$$M = \frac{(.3514)\left[\frac{0.12}{(7.7)^2} + \frac{1}{(6.6)^2}\right]}{\pi^2 \left[\frac{1}{(7.7)^2} + \frac{1}{(6.6)^2}\right]^2}$$

$$M = .5607 \quad in\text{-}lb/in$$

FORM NO. 48—0360

CALC. Harrison | REV | DATE | CLASSIF.

DYNAMIC LOADING CASE 2

G10

$f_{b_{GIO}} = 1561 / (.1607) = 9715$ Hz

ALUMINUM SIDE PLATE (HOLES IN BOARD)

$F_{cu} =$ [illegible]

$M.S. = \frac{3[illegible]}{1.5(1.11)(9715)} - 1 =$ HIGH

C.U

$f_t = 14744 / (.5607) = 8043$ Hz

$F_{cu} =$ [illegible] psi

$M.S. = \frac{10,000}{(1.5)(8043)} - 1 = 3.14$

DYNAMIC DISPLACEMENT

$Z_c = \frac{9.8 G_{OUT}}{f_n^2} = \frac{(9.8)(1.0)}{(60)^2} = .0735"$ S.A.

RAYTHEON FORM NO. 4R-0340

CALC. Harmon | REV | DATE | CLASSIF.

SOLID GLC PLATE - STATIC ANALYSIS

1ST MODE

$b = 6.6$

$a = 7.7$

$\alpha = \frac{6.6}{7.7} = .8571$

$\alpha^2 = .7347$

$\nu = .6297$

STRESS

$$f_L = \frac{.3514 (6.6)^2 (.75)}{1.062)^2 (1 + 1.61 \{.6297\})}$$

* $f_b = 1483$ PSI

DEFLECTION

$$c = \frac{(.1422)(.3514)(6.6)^4}{1.85 (10)^6 (1.062)^3 (1 + 2.21 \{.6297\})}$$

* $\delta = .0899$ IN

* FOR COMPARISON PURPOSES ONLY.

FORM NO. 48-0380

RAYTHEON

CALC. Harmon | REV | DATE | CLASSIF.

15.1.4.3 Vibration and Shock Tests for Shelter Units

Vibration and Shock testing of the above equipment were performed in accordance with paragraph 4.2.6.2.8 of TT-B1-2202-0013 and were handled in the following manner:

a. Fixture Design Analysis and calculations are consistent with acceptable practices within the discipline, which result in the fixture complying with test criteria identified below.

b. Tool control procedures apply to all fixtures or jigs in accordance with Raytheon General Policies and Procedure #61-4350-142 in conjunction with any specific Government agency requirements.

c. Formalized drawings are required for all fixtures or jigs in accordance with MIL-D-1000. These drawings were approved by the cognizant Raytheon engineer prior to release for fabrication bids.

The following procedure standardizes all fixture designs. Resonance surveys were performed on each new fixture configuration prior to vibration test. Once the requirements of this standard are met, no further fixture resonance investigations were necessary. A 17,500 force pound electrodynamic shaker system was set aside for these tests.

15.1.4.3.1 Fixture Evaluation Procedures

Sine surveys were performed in each of the three orthogonal axes with each fixture system assembled in the test configuration. The survey consisted of: 1g, 5 Hz to 200 Hz, 1 oct/min. Prior to fixture surveys an accelerometer response survey was performed on all accelerometers scheduled to be utilized for these tests.

a. For this survey all accelerometers were mounted in one direction on the shaker. One accelerometer controled the performance of the sine survey noted above. All acceleration responses were taped and plotted according to Section 2.

b. Primary areas of investigation were crosstalk of the fixture system and verification of vibration input at the mounting points of unit under test and conformed to MIL-STD-810.

c. Fixture evaluations were performed utilizing the actual unit or a mass simulating at least the mass weight distribution and CG of the actual test unit.

d. Required data was obtained by the use of tri-axial clusters of accelerometers at the most remote mounting points of the specimen.

The orientation of these accelerometers was identical to the orthogonal axis designations for the test specimens.

e. The responses of these accelerometers was examined to ensure that motion in any orthogonal transverse direction (cross talk) produced by the fixture does not exceed the vibration input levels. (MIL-STD-810)

15.1.4.3.2 Sine Survey Criteria

a. Data acquisition and reduction. The following procedure also applied to actual test item configurations.

b. Data acquisition and reduction. A minimum of four input and cross axes instrumentation points were used. In addition, capability to provide response data of up to 18 response locations on the package was provided as necessary.

c. Accelerometer noise analysis was performed immediately prior to the first sine survey. The analysis consisted of taping outputs of the accelerometers (mounted in their correct location on the package) while the shaker system is completely turned on and ready to run except for the gain which remains in the minimum position and the oscillator at 5 cps or less.

d. Accelerometer outputs were simultaneously and continuously taped on magnetic tape utilizing a tape recorder with a frequency response of at least 0 to 2500 cps at the recording speed which is to be used.

e. Data at all locations were plotted directly and continuously from the tape producing plots of amplitude (g pk) vs frequency f (Hz).

f. All taped data were stored at least until Qualification Vibration Tests are completed to allow analysis of wave shapes should the need arise.

g. Data Acquisition and Reduction. The combined accuracy of the data acquisition and play back system was within 10 percent of the true values for both peak g's and frequency.

15.1.4.3.3 Shock Test Fixtures

The shock fixture was capable of applying the specified (MIL-STD-810B) shock in each of six directions along three axes with no ringing that would cause peaks greater than the specified input level at frequencies up to 2 kHz. This will be demonstrated by a Polaroid® photograph of the input shock pulse at each input location. The instrumentation used to observe the pulse was unfiltered to 2 kHz.

15.1.4.3.4 Shock Tests

The shock pulse also was recorded on magnetic tape at each of the input locations and at least two other response locations in the package for a minimum of six instrumentation points.

15.1.4.3.5 Instrumentation

Vibration Tests. Tri-axial clusters described consisted of commercial tri-axial piezoelectric accelerometers mounted on the appropriate faces of a small mounting cube. This cube is subsequently mounted at the desired location on the test specimen or fixture.

15.1.4.3.6 Vibration Tests

The test items were subjected on all three orthogonal axes to the following tests:

* Test Level - 1.5 g (as limited by 1" P-P displacement)
  Frequency Range - 5-200-5 Hz log sweep at 1 oct/min
  Time Schedule - 5-1/2 hours/axis
  Sweep Rate - 5-200-5 Hz in 12 minutes

*The level becomes 1.5 g at 5.4 Hz or 1.277 g at 5 Hz

The units were functionally tested before and after dynamic tests in accordance with an approved test procedure.

Bench handling shock tests were also performed on these equipments in accordance with MIL-STD-810B, Method 516, Procedure II.

15.1.5 EMI DESIGN

15.1.5.1 General

The shelter mounted equipment is designed to meet the applicable requirements of MIL-STD-461. A power line filter integral with an external hook-up connector is mounted on the rear panel adjacent to an external grounding stud. All access covers, power supply front panel, connectors and external mounted components are gasketed and/or electrically and mechanically bonded to control RFI. Conductive finishes are selected from MIL-F-14072. The units are designed and constructed with adequate provisions for bonding the unit to a subsystem ground plane. Bonding is not accomplished through screws connecting the equipment to mounting racks. Bonding jumpers are of the solid metal type and as short as possible. However, in no case is the length to width ratio of the jumper in excess of 5 to 1. Bonding techniques employed do not impede maintainability nor adversely affect interchangeability. Surfaces being bonded together are prepared by removing all anodic film, grease, paint, lacquer, dirt or other foreign and high resistance materials or agents from the immediate area to insure negligible rf impedance between the adjacent metal parts. Upon completion of the bonding assembly and ascertainment of the specified 2.5 milliohm bonding impedance, the completed assembly refinished in accordance with MIL-F-14072. Other interconnecting cables re-
of the specified 2.5 milliohm bonding impedance, the completed assembly is
refinished in accordance with MIL-F-14072. Other interconnecting cables requiring a cross shield have a minimum of 90 percent shield coverage. The conductive finish and employing an EMI backshell that provides for peripheral bonding of the shield. When shielding alone is employed and design requirements cannot be met, pin filter connectors would also be used. All panel mounted

connectors and components and the panel mating surfaces are free of non-conductive finishes and provide positive bonding and grounding with mating connectors and equipment ground plane. The bonding dc resistance of all connectors and panel mounted components will not exceed 2.5 milliohms.

The gasketing systems employed for the shelter mounted equipments do not require rain or immersion seals and will use beryllium copper spring finger stock. The rear access panel over the W/W plate is gasketed by spring finger stock as is the rear protrusion of the power supply. Captive hardware is located around the periphery of the covers and panels spaced to provide adequate RFI compression without causing unnecessary hardware removal to gain access to the subassemblies for replacement. Shield plates between subassemblies as required to provide additional isolation of circuits. Coaxial cables and feed through capacitors are used as required to control critical signal runs. A detailed EMI design plan is outlined in the following paragraphs.

15.1.5.2 EMI Envelope

The outer surface of each unit is defined as the EMI envelope for design purposes (see Figure 15-23). To illustrate this envelope, imagine constructing an enclosure by welding one-half inch steel sheet together. Before welding the last sheet, the electronics and batteries are placed inside. The enclosure becomes RF tight as soon as the last sheet is welded in place. From a practical standpoint though, this configuration would not be very useful, because components was designed with sufficient RF integrity to maintain the required shielding effectiveness. The shielding of each enclosure was determined when the com-
effectiveness. The shielding of each enclosure
ponent parts of each are fully defined.

15.1.5.3 Unit Enclosure

Each unit housing was designed and constructed to provide the required shielding effectiveness. The impedance between any two points on the housing

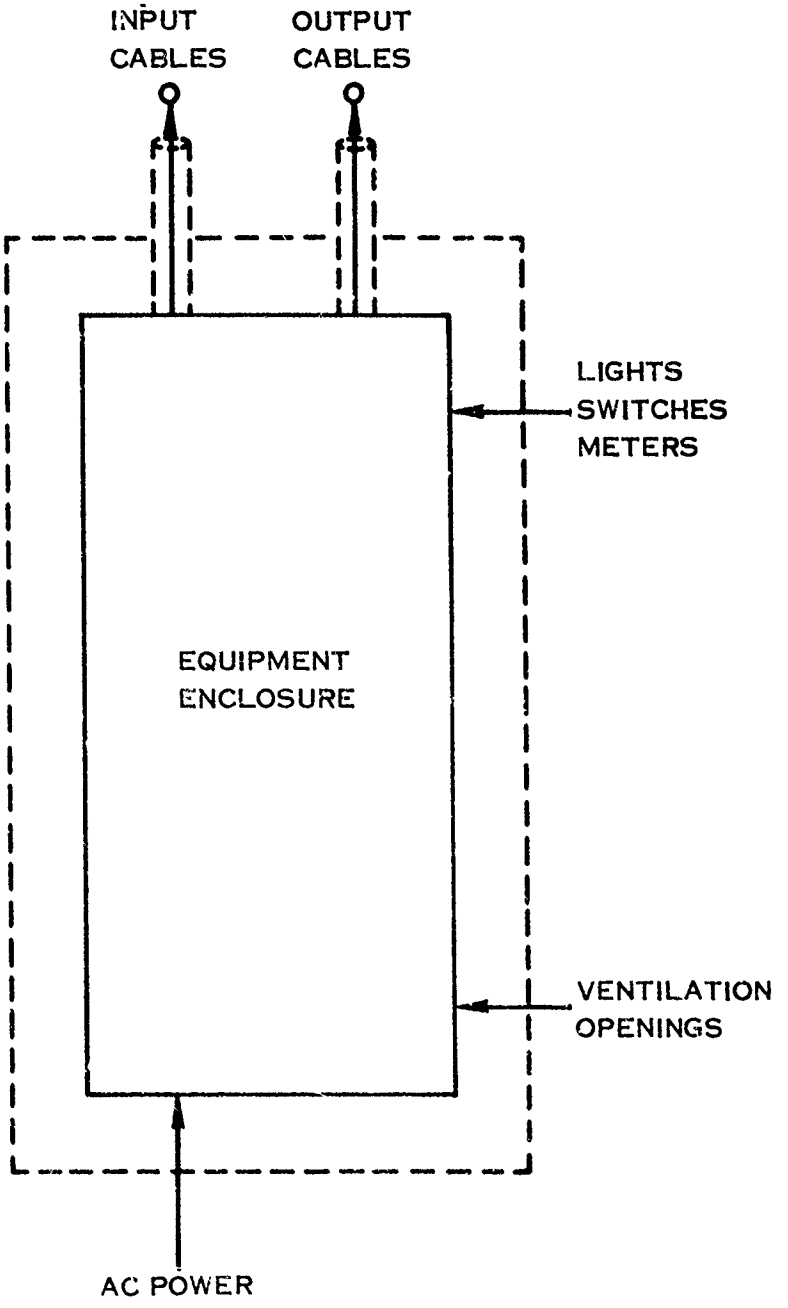


Figure 15-23. EMI Envelope

should be constant and as low as possible at any frequency. This is accomplished by using highly conductive mating surfaces, close mechanical tolerances, and rigid construction.

15.1.5.4 Grounding

Each unit utilizes a multi-point ground, i.e., all signals within the unit are referenced to a large, easily accessible, low impedance surface area, specifically, the equipment housing. Ideally a conductor which has zero impedance can conduct infinite current with no differences in potential across the conductor. This type of grounding scheme minimizes common impedance sharing between circuits and provides maximum effectiveness from filters, shields, and decoupling networks. Certain high level currents within the system are routed through return wires as required. Each unit is provided with a power safety ground through its I/O connectors. Bonding impedances are less than 10 milliohms measured at dc. A diagram of this approach is shown in Figure 15-24.

15.1.5.5 Ventilation

Where cooling air is required, honeycomb filters are used. For natural convection and radiational cooling, perforations in the case are used. Aluminum honeycomb is used for air openings - Omnicell (Tradename) is a configuration which has proven reliable as an RF attenuator (>80 dB) up to 10 GHz.

15.1.5.6 Printed Circuit (PC) Boards

PC boards with ground planes and more than three chassis ground connections are far superior to those with grounds which are interspersed among the interconnecting etches. The ground plane minimizes common impedance sharing between circuits on the board and also acts as an RF shield to reduce board-to-board coupling. When multi-layer PC boards are used, a ground plane is a practical necessity, and is used.

15.1.5.7 Internal Wiring

In an equipment which processes only digital signals, the internal wiring arrangement is less critical, since practically any configuration is adequate However, when an equipment processes digital, analog, and high-level continuous

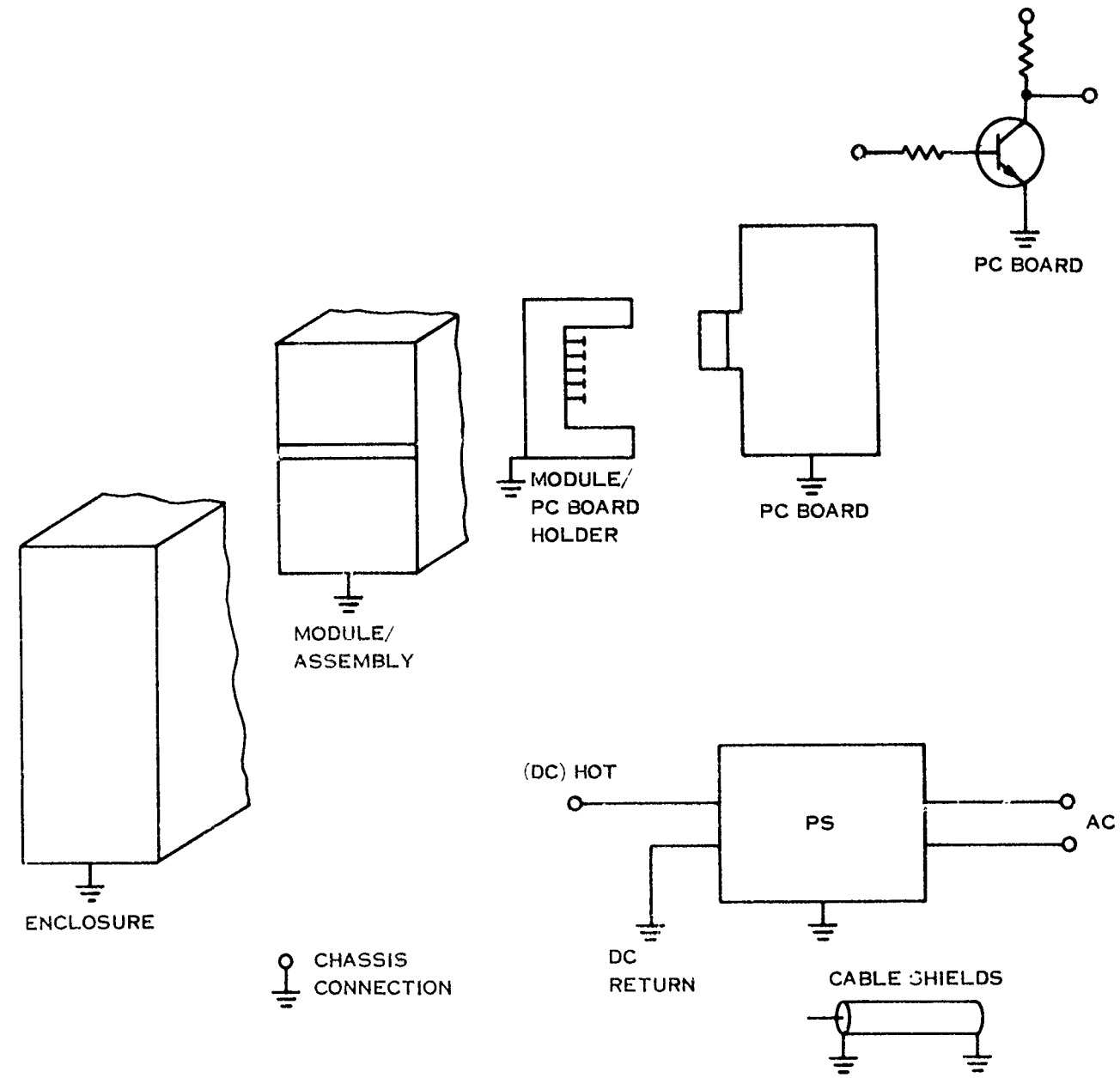


Figure 15-24. Overall Grounding Philosophy

wave (CW) signals, the layout becomes critical because of coupling within the wire harnesses. The two factors which reduce cable coupling are use of shielded cables which are properly terminated, and physical separation.

15.1.5.8 Switches and Indicators

Switches and indicators become radiators of EMI through pickup on their associated wires. These coupled signals can be eliminated at the switch or the indicator by using bulkhead-mounted filters. However, the best method to eliminate radiation is to shield the indicator or to ground the shaft of the switch. For the DGM equipments, all external switches will utilize grounded shafts and all indicators and push-button switches will be shielded.

15.1.5.9 Connectors

Coaxial terminations (BNC, N, TNC, etc.) are installed properly, i.e., no paint or other insulation material between the connector and the mounting surface. The coaxial shields are terminated, using all wire strands, in 360 degrees.

15.1.5.10 Power Supplies

In an equipment, the power supplies (AC/DC or DC/AC) are a prime source of EMI in that they are inherently noisy and are conductors of the signals processed within the equipment. In accordance with preferred design practice, power supply noise and operational signals at the power supply input were reduced to the lowest possible levels through design. This resulted in lower insertion losses for the power-line filter, which reduces filter size and cost. A solid-grounding approach helps reduce power supply noise.

15.1.5.11 Filter Installation

There are two major criteria involved with filter installation. First, the output wires must be isolated (shielded) from the input wires by at least the insertion loss of the filter; that is, if the attenuation of a filter as 1 MHz is 60 dB, then the output wires must be isolated from the input wires by at least 60 dB. Second, the case of the filter must be referenced to the same ground point as the signals it will attenuate; that is, the RF impedance between the installed filter

and the signal reference must be as close to zero as possible. This type of filter installation achieves maximum insertion loss from the filter.

15.1.5.12 Access Doors/Panels

Access doors/panels are perhaps the most difficult parts of an enclosure to design for 60 dB or more of shielding effectiveness. For this reason, their use is minimized in this program and where required, is kept as small as possible.

15.1.5.13 RF Gasket Screw Spacing

Screw spacing for the mating surfaces is selected in accordance with Figure 15-25.

15.1.5.14 Required Shielding Effectiveness

The highest, intentionally processed digital signal within the system is 20 MHz at 3 volts. Assuming a square wave (worst case) the envelope of the Fourier Spectrum for this signal is shown in Figure 15-26 (solid line). If the space loss (Figure 15-27) subtracted from this level, then the field intensity, at one meter, is defined (dotted line). The space loss has been determined through past test experience. Thus the standard case must provide 80 dB of shielding at 20 MHz decreasing to 20 dB at 1 GHz. Since shielding effectiveness improves below 10 MHz, no requirements need be specified.

15.1.5.15 EMI Design

a. Shielded Enclosure - Each unit enclosure is designed to provide 80 dB of shielding effectiveness. This provides sufficient attenuation to reduce all radiated signals to levels below the MIL-STD-461A limits. The details of these enclosures are discussed below. An exploded view of unit frames are shown in Figure 15-28. The basic frame is dip brazed construction-tion. The front and back covers were sealed with an RF gasket (finger stock) and bolted into place. All gasket mating surfaces were finished with iridite to prevent corrosion, but this finish will not degrade the shielding effectiveness as the gasket will bite into the frame when the covers are secured.

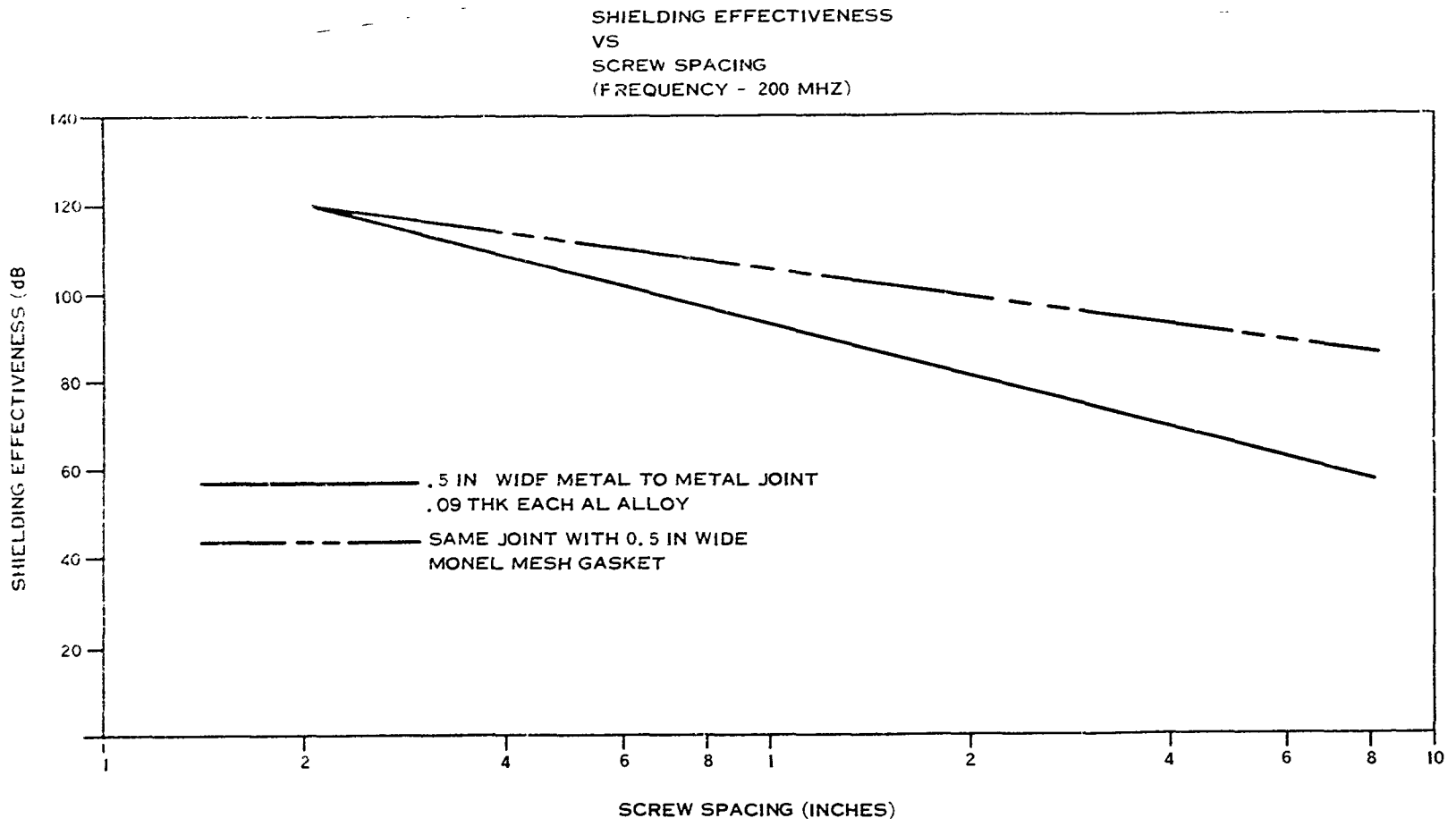


Figure 15-25. Shielding Effectiveness vs. Screw Spacing (Frequency = 200 MHz)

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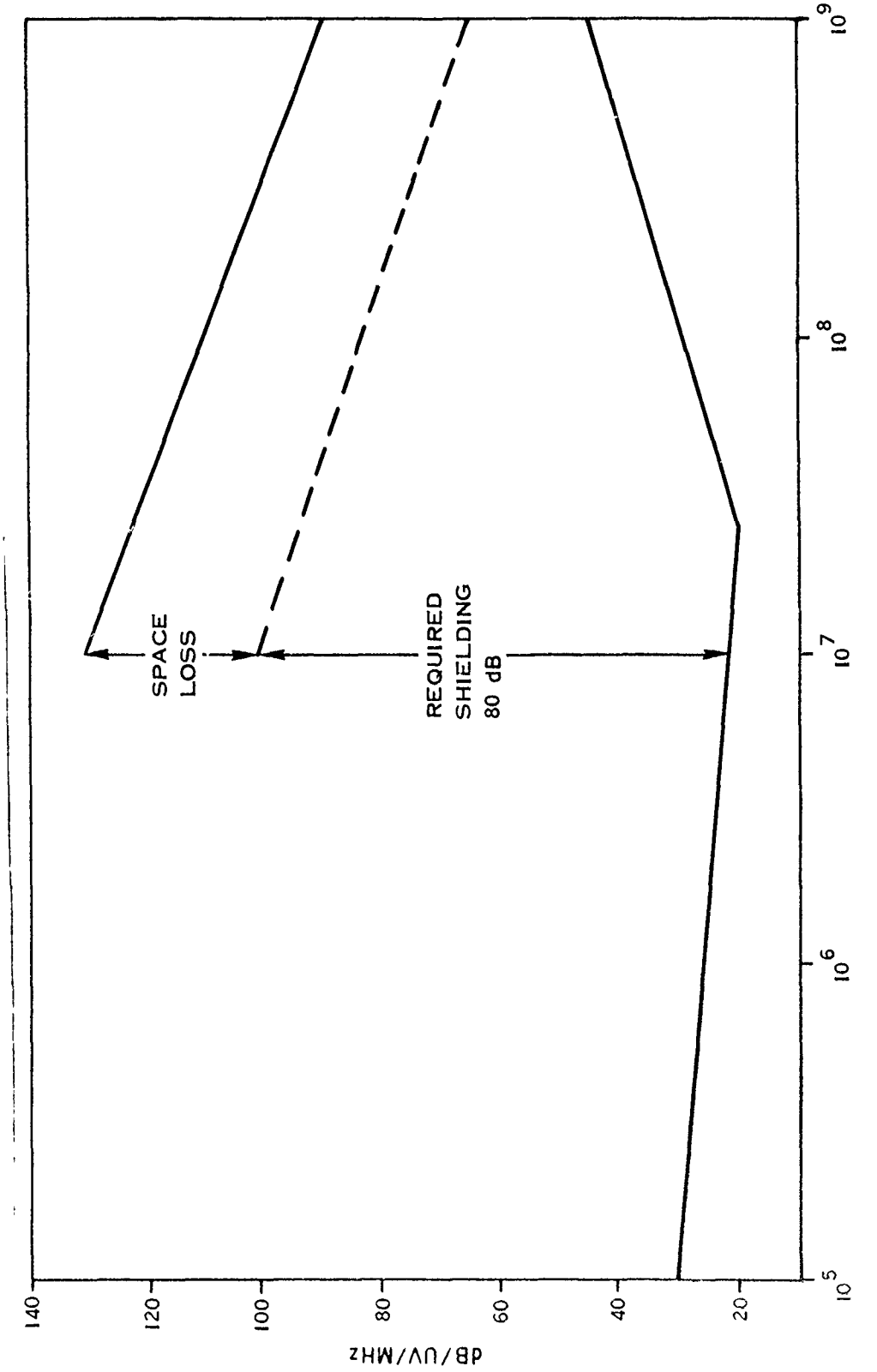


Figure 15-26. Determination of Required Shielding

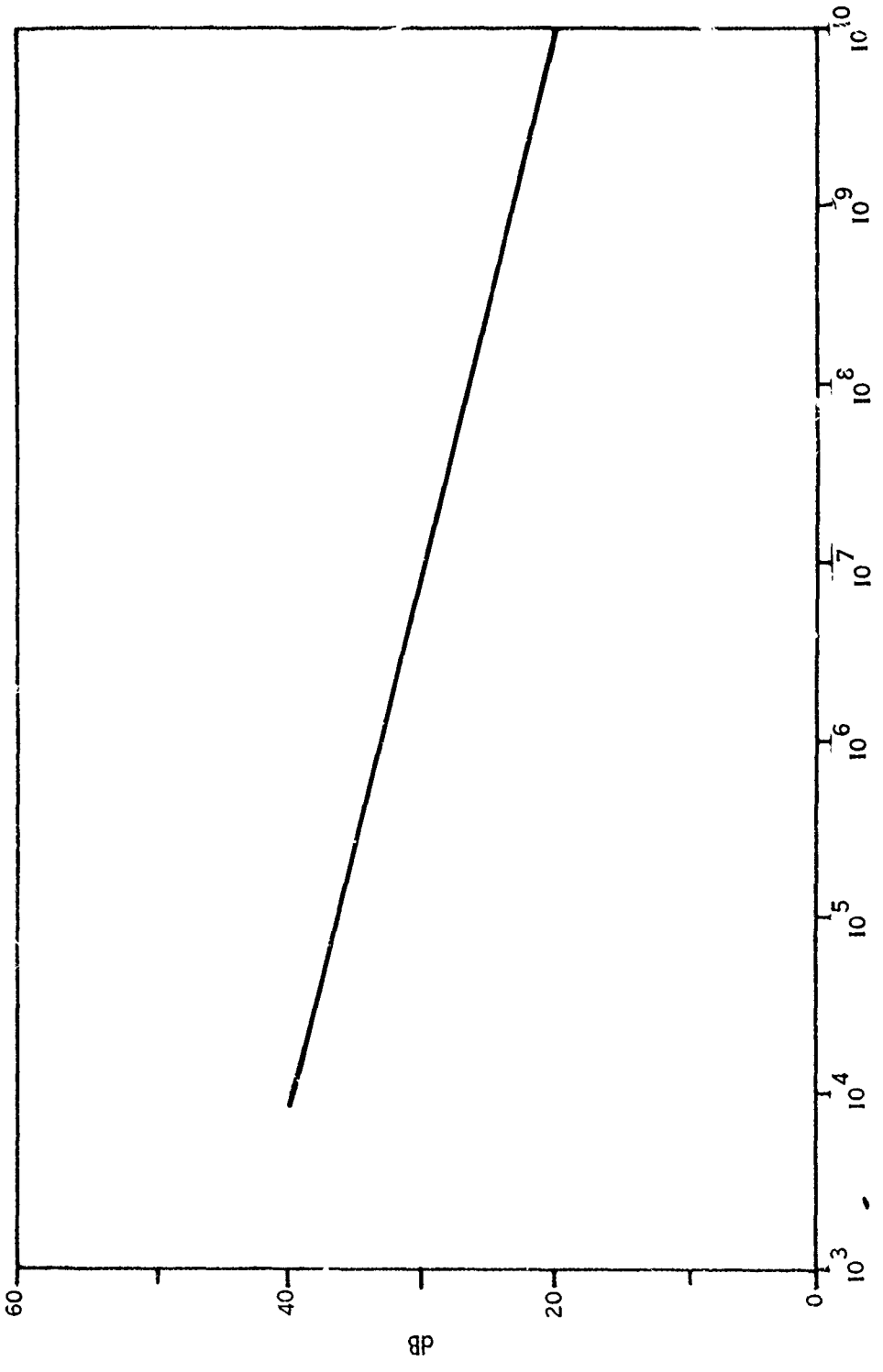
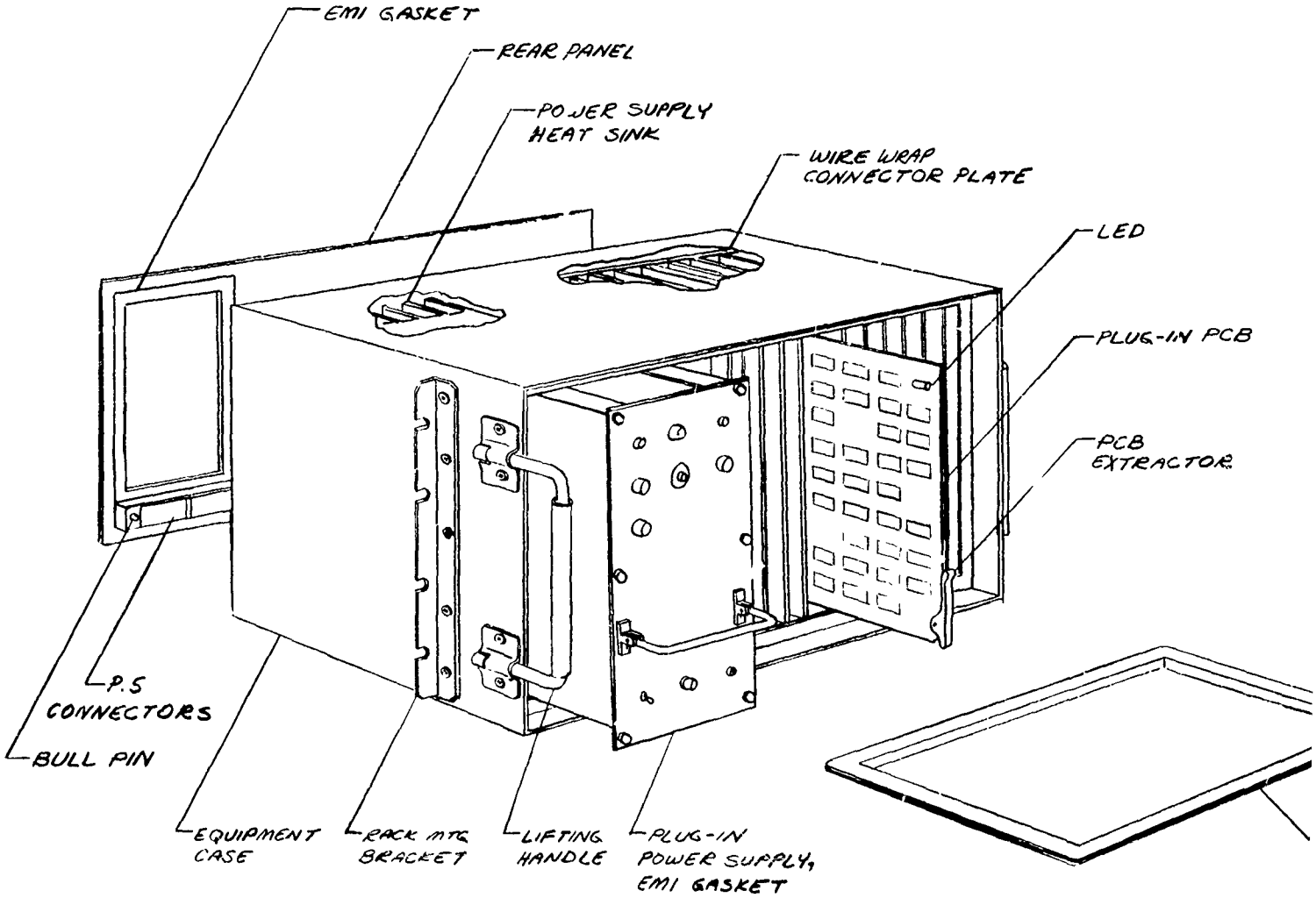
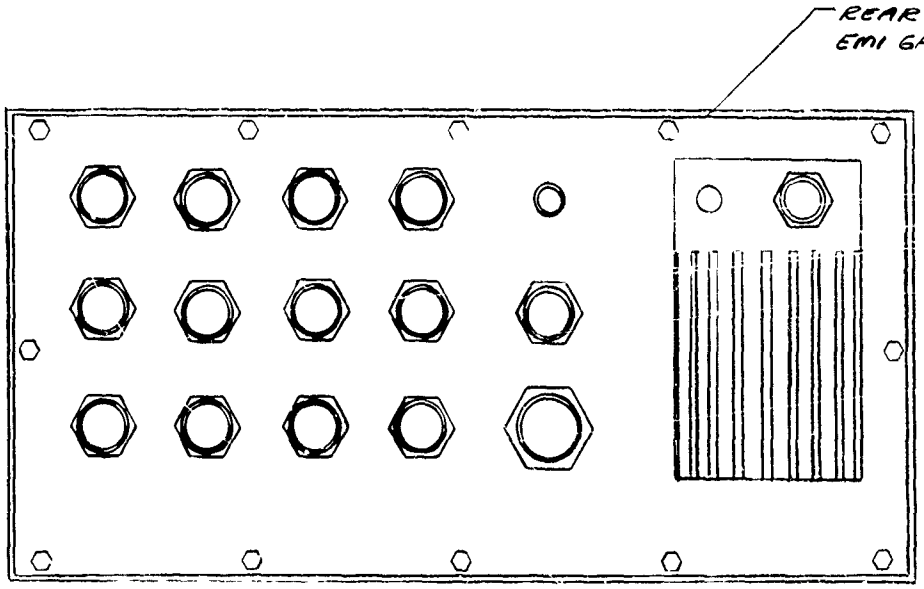


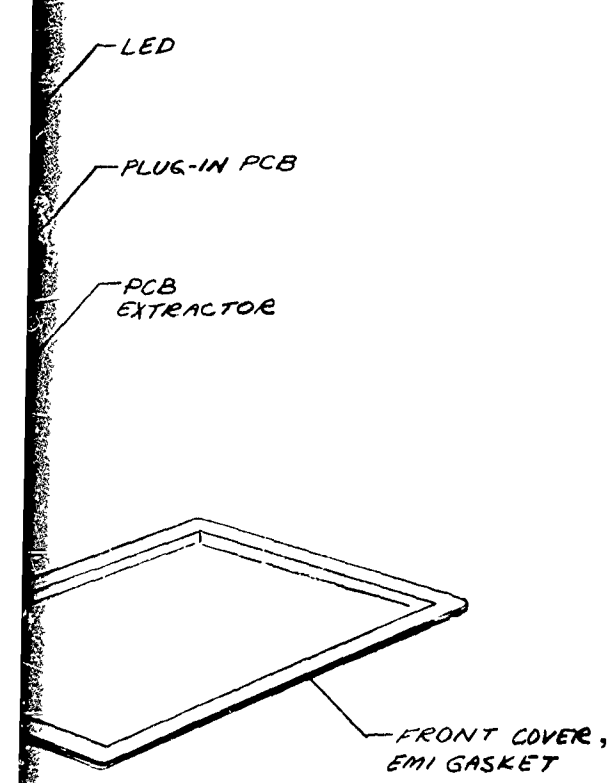
Figure 15-27. Electric Field Space Loss (1 meter)

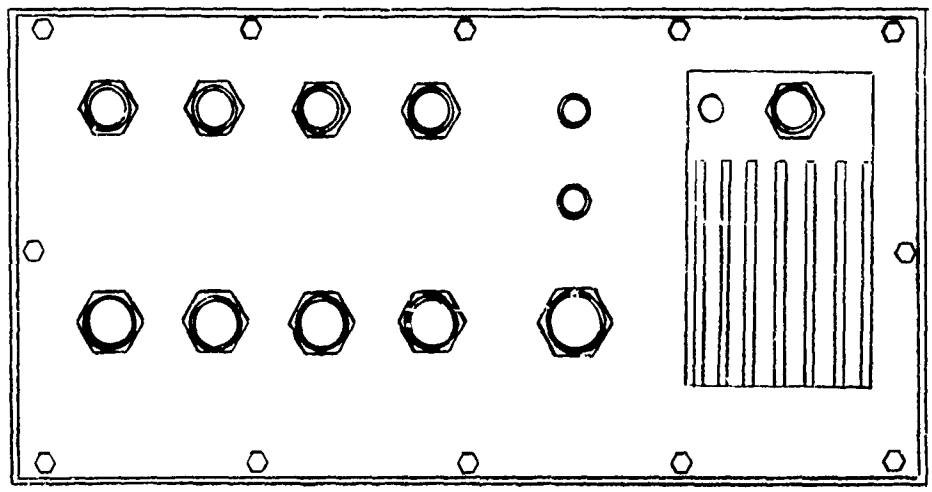




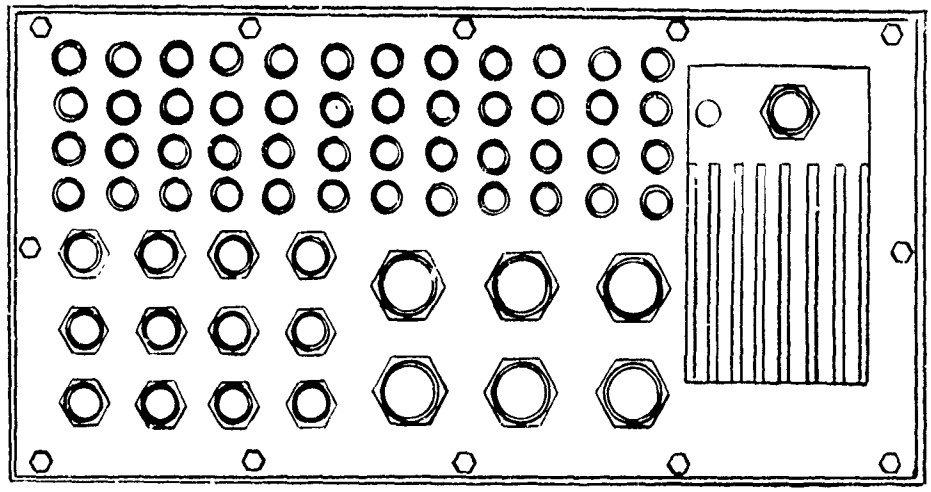
Note: See i
unit section
tails on fro
panels (i. e.
of componei
etc.)

MCM REAR PANEL
HFB-24





TGM REAR PANEL
HFB-23



GM REAR PANEL
HFB-25

Note: See individual unit sections for details on front and rear panels (i.e., location of components, marking, etc.)

Figure 15-28. TGM, MGM, GM Physical Design

The basic unit design has demonstrated adequate shielding capability for meeting the requirements of MIL-STD-461A on programs such as TD-1065, KG-27 and TD-660.

b. TGM, MGM, GM, LM, LGM, CDM & RLGM/CD - The TGM, MGM, GM, LM, LGM, CDM & RLGM/CD is designed as shown in Figures 15-28 and 15-29. The unit frames, front cover, and rear panels are basically designed the same. The difference in the back covers is strictly the number of connectors each has. The gaskets for the back covers is finger stock as shown in Figure 15-30. It was found during EMI testing of the TD-1065 that finger stock on the back covers insures a good metal to metal contact between the cover and unit frame, thus insuring that the cable shields which terminate on the back covers are at the same ground potential as the unit frame.

The front covers have spring fingers as shown in Figure 15-30. All lights, meters and switches are shielded to insure RF tight enclosure integrity. All cables are either double shielded twin coax or RG-108 whose shields will be terminated around 360 degrees.

15.1.6 HUMIDITY, SALT ATMOSPHERE, FUNGUS

Humidity and salt atmosphere conditions as invoked and characterized by the MIL-STD-810B tests can result in moisture migration and penetration and a high level of corrosion. To achieve a humidity/corrosion resistant design, the following design criteria are being used through all levels of design:

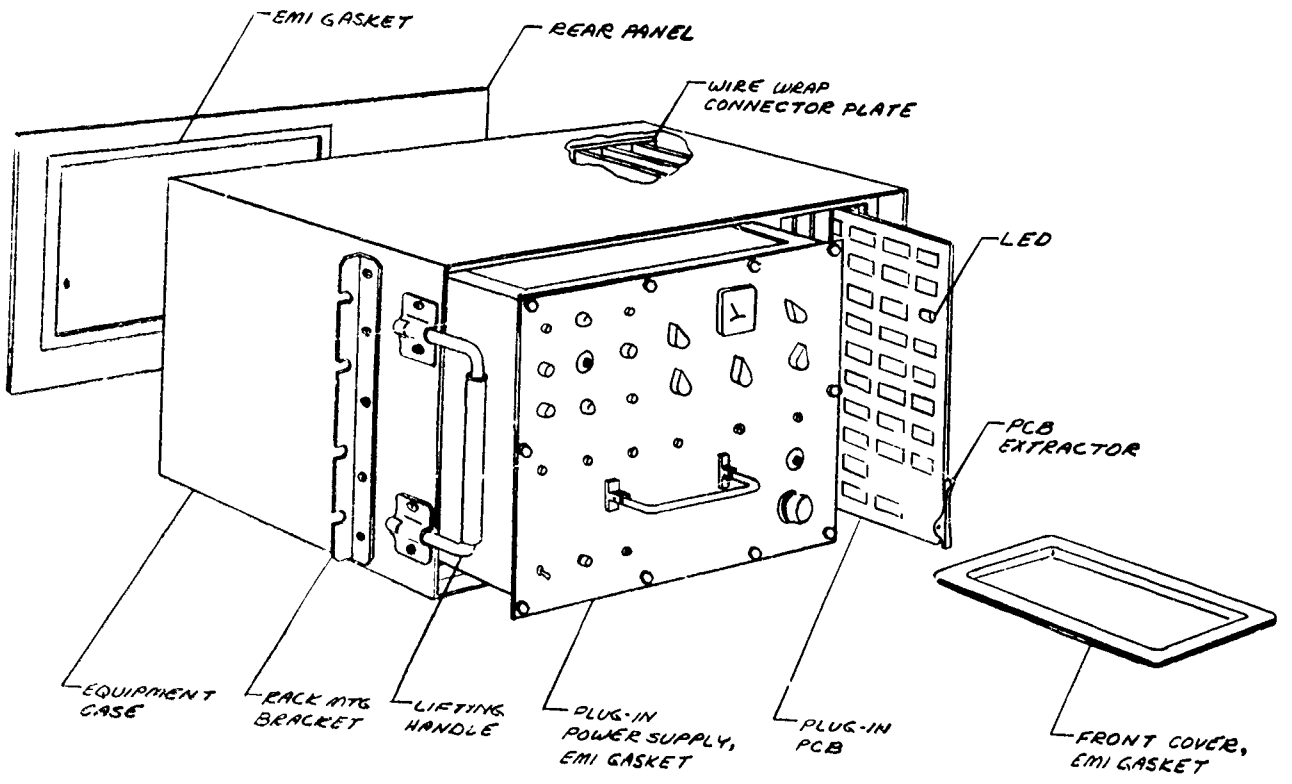
a. Use of non-metallic materials which are non-hygroscopic or have very low water absorption characteristics.

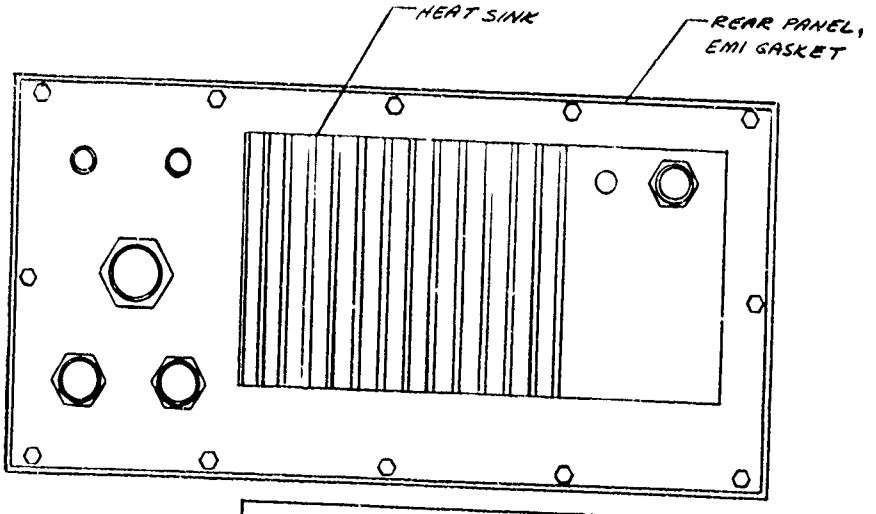
b. Observance of the compatible couple requirements of dissimilar metals.

c. Use of protective finishes to increase corrosion resistance of metals.

d. Corrosion resisting stainless steels for hardware.

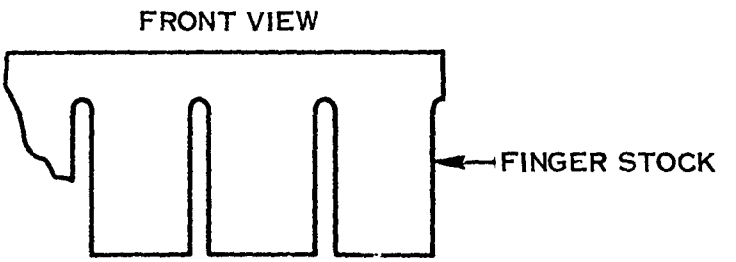
e. All active semiconductor devices hermetically sealed.

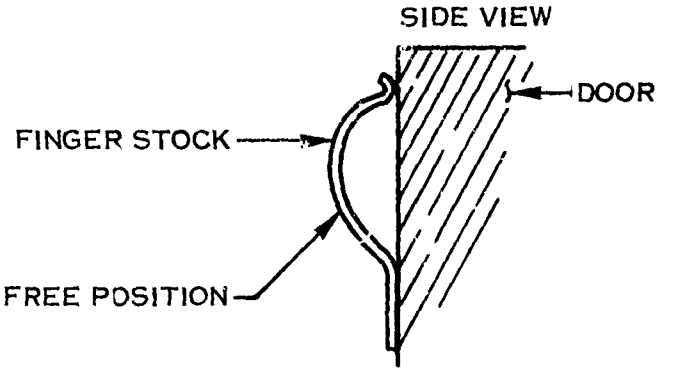




Note: See individual unit sections for details on front and rear panels (i.e., for component location, marking, etc.)

Figure 15-29. CDM Physical Design





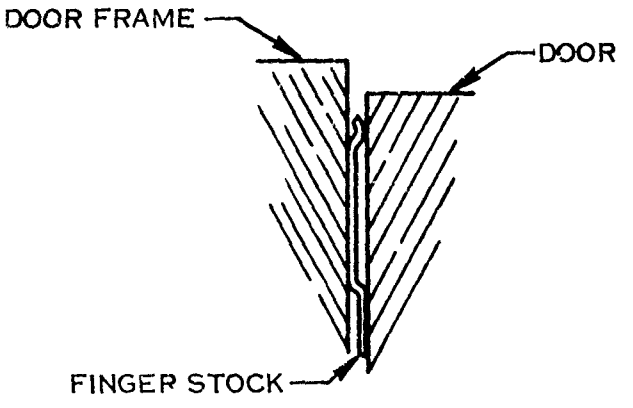


Figure 15-30. RF Gasket Configuration

f. Use of conformal coatings (per MIL-I-46058) for printed circuits to protect against corrosion and to inhibit short circuiting due to humidity and/or dust.

g. Careful attention in the selection of traditionally troublesome components such as potentiometers and coils.

h. Careful control of printed circuit board materials and fabrication processes.

i. Use of non-nutrient materials in accordance with MIL-STD-454B, Requirement 4, e.g., G10 Series PC Cards.

j. Sealed and pressure relieved case design.

k. Gasketed covers.

15.1.7 POWER SUPPLY INTEGRATION

The power supply is designed as a separable plug-in subassembly mating with a rack and panel style connector at the rear and mounting via captive hardware at the front of the equipment case. A finned (heat sink) rear panel of the power supply protrudes through a gasketed opening in the equipment rear panel to transfer heat directly from the power supply to ambient air. All operational controls are mounted on the front surface of the power supply. Spring finger type gasket provides the conductive interface between the front panel of the supply and the equipment case. Spring finger stock provides the conductive interface at the rear of the case where the power supply protrudes through into ambient air.

15.1.8 AN/GRC-103 MODEM

15.1.8.1 AN/GRC-103 Modem Case Design

The AN/GRC-103 Modem Unit physical design is shown in Figure 15.1.8-1. It is in full conformance to the physical characteristics outlined in Chapter 15 for shelter mounted units and in physical appearance, size and configuration greatly resembles the GM and TGM Units shown in Figure 15-2. The actual dimensions, weight, power dissipation, and environmental requirements are listed in Tables 15.1.8-1, -2, and -3.

15.1.8.2 Detail Part Design

The various parts, components or assemblies used in the configuration of this unit are described as follows:

a. The case is identical to the part used in the GM and TGM Units unmodified.

b. The power supply is the same identical unit used in the GM and TGM units unmodified.

c. PCB's are new design, but are fully conforming to the standard outline as described in Paragraph 15.1.2 and shown in Figures 15-8, 15-9, and 15-10. Special consideration was given to control the heat within the component limits so as not to decrease the MTBF of the unit.

d. The card guide system will be the same concept as described in Paragraph 15.1.2.3. The guide pitch is unique for this design and incorporates a connection technique for mounting the barrier/divider used in separating the RED and BLACK PCB compartments.

e. Wire-wrap plate design is similar to other like units except that the so-called BLACK compartment circuit card connectors and wiring was separated from the RED compartment circuit card connectors and wiring. This separation includes a separate power and ground bus bar system for the RED and BLACK PCBs.

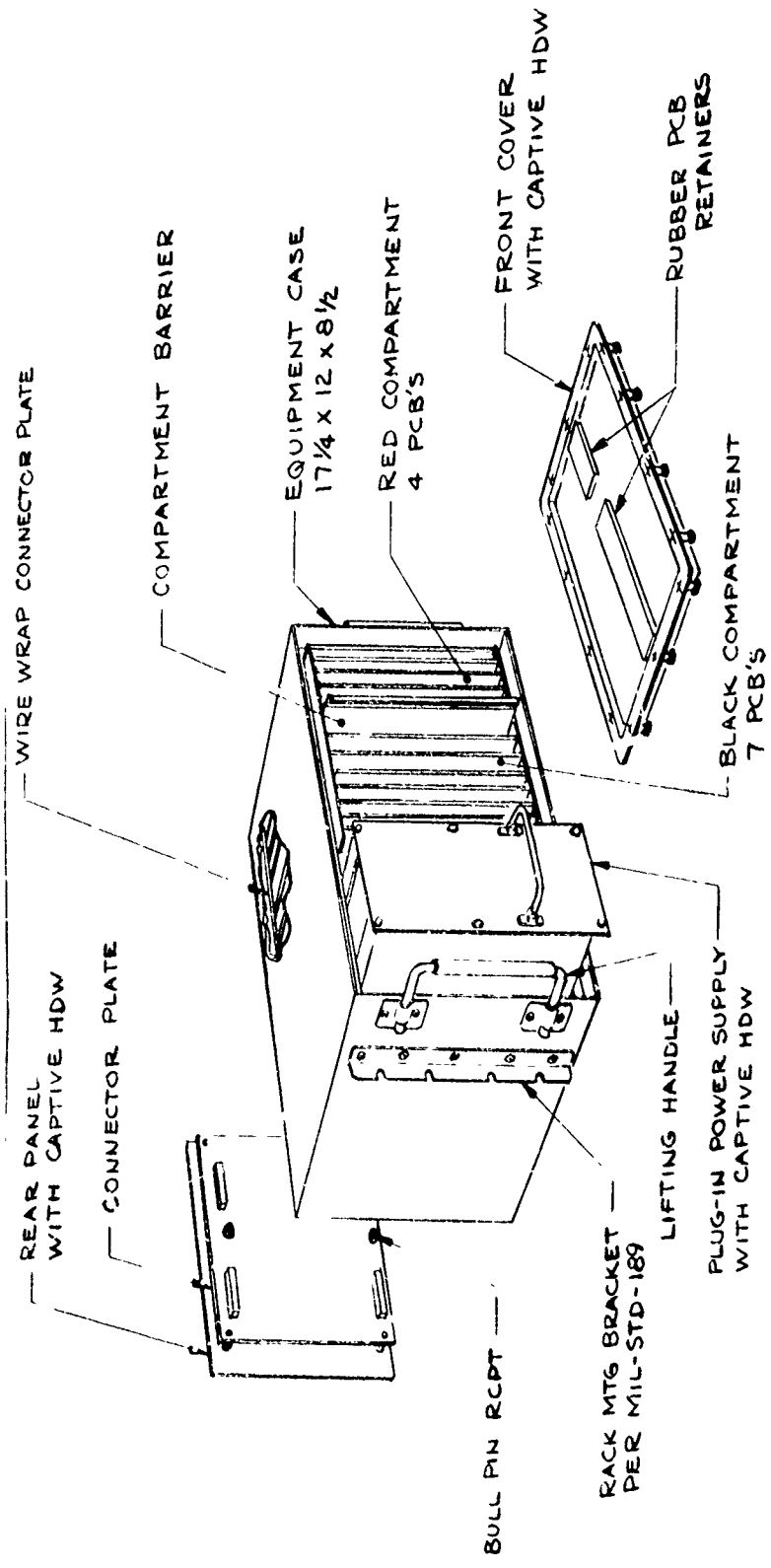


Figure 15.1.8-1. AN/GRC-103 Physical Design

Table 15.1.8-1. Physical Characteristics, GRC-103 Modem

Case Dim /Inches	Case Vol. /ft^3	Wt. of Unit /lbs	PS Type	No. of PCB's	Power Dissipation /watts	Power Density /watts/in^3
8.5H x 17.25W x 12.0D	1.02	37.6	4.0 Plug-In	11	62	0.035

Table 15.1.8-2. Weight Distribution, GRC-103 Modem

Case Complete Less PS, PCB and Compartment Barrier Hardware - lbs	Power Supply /lbs	PCB's /lbs	Miscellaneous, Divider and Compartment Barrier Hardware/lbs
20.0 lbs	9.0	0.65 Avg x 11 = 7.15	1.35

Table 15.1.8-3. Environmental Conditions, GRC-103 Modem

Temperature		Altitude		Humidity, Dust, Salt Fog, Fungus, Vibration and Shock and Transportability
Operating	Non-Operating	Operating /ft	Transport cond/ft	
-25°F to +145°F	-70°F to 160°F	10,000	40,000	Same Requirements as DGM Rack Mount Equipment (See Table 15-8)

f. Rear connector panel configuration is shown in Figure 15.1.8-1 and 15.1.8-2. The BLACK compartment connectors are grouped to provide separation from the RED compartment connectors on the rear panel and will also feature wiring separation and isolation of the connectors which mate with the wire-wrap plate assembly. In the BLACK compartment connector panel area, an RFI tight module case, approximately 3" x 2" x 1" deep is employed to filter the signal to the Radio I/O, see Figure 15.1.8-3.

g. The front cover design is the same as other like units except that the decal will be unique to illustrate the subassemblies and functions of the 103 Modem.

15.1.8.3 Special Design Considerations

The main design effort on this unit was to effect an adequate BLACK/RED compartment separation. Care was also taken to provide for critical signals which carry high frequencies and their interconnections to circuit card connectors and input/output connectors.

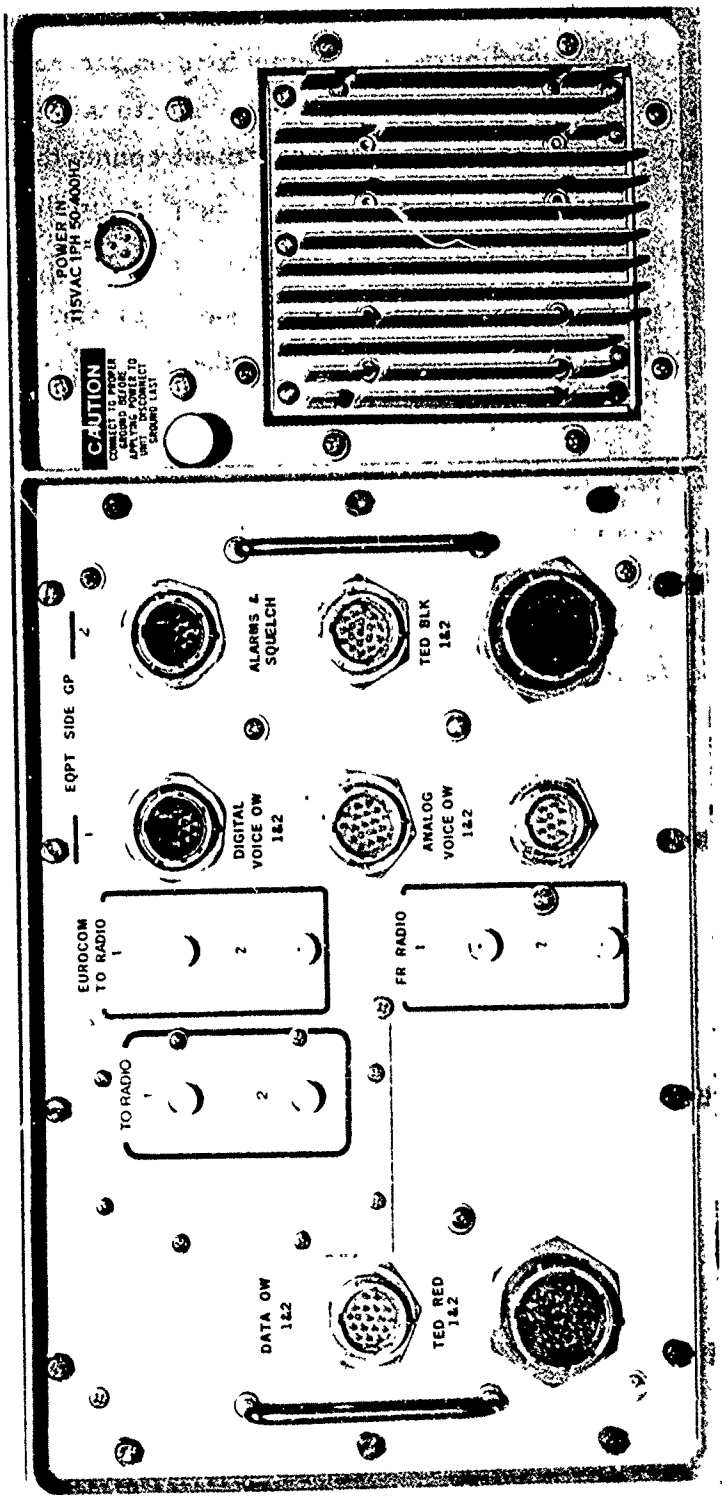


Figure 15.1.8-2. AN/GRC-103 Rear Panel Configuration

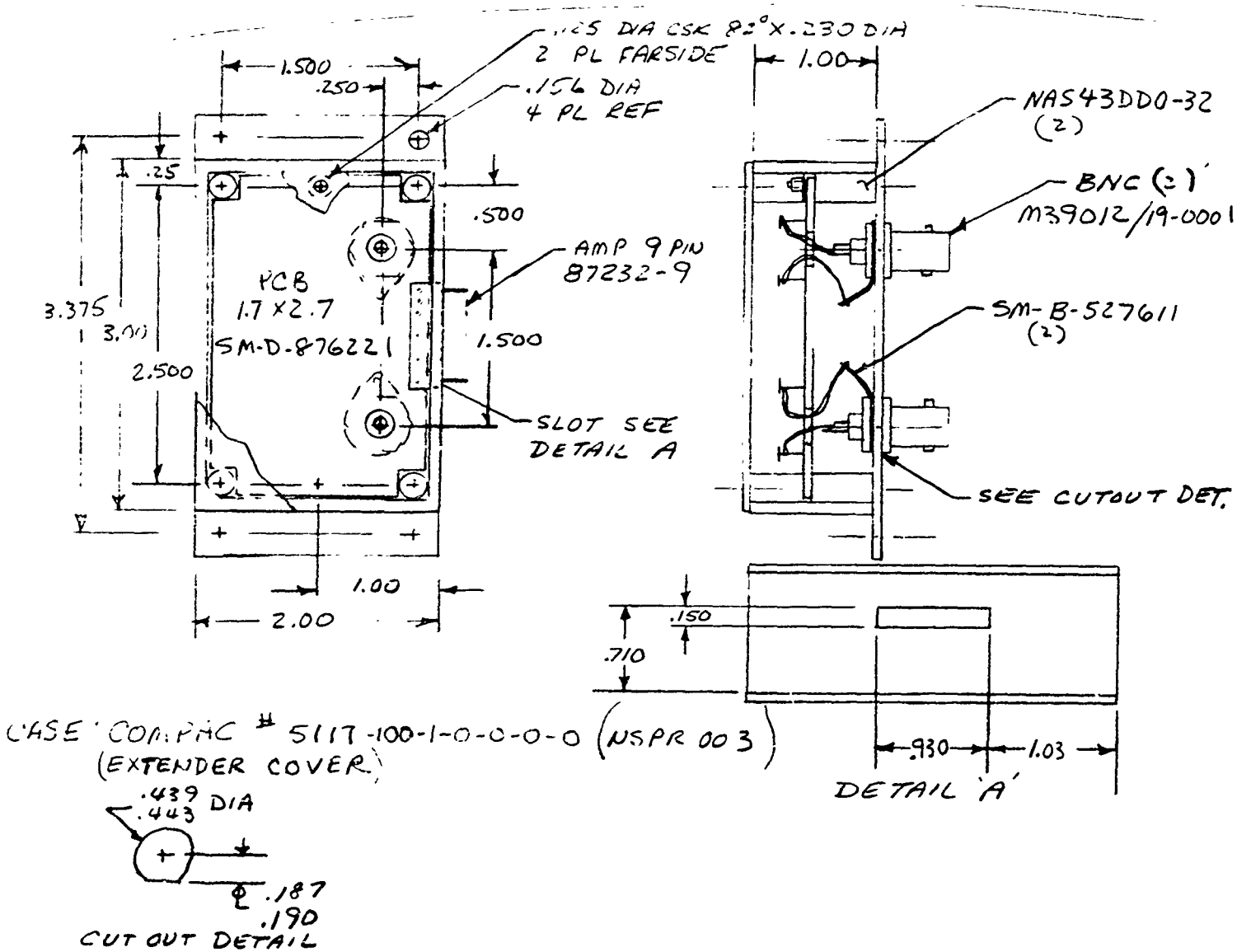


Figure 15.1.8-3. Coax Assembly (AN/GRC-103)

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15.2 PULSE RESTORER UNITS

15.2.1 CASE DESIGN

After successful qualification and field testing of the TD-206 B/G pulse restorer and a re-evaluation of the priority for the weight specification, Raytheon utilized a similar basic case design philosophy for the LS and HS pulse restorers (see Figure 15-31).

The body and covers were investment casted employing alloy Al A356-T6 to maximize the strength to weight ratio. Modifications to the basic TD-206 B/G to improve performance and reduce cost are as follows:

a. Integrate the UG-1837/U connector shell into the cast body to delete the heavy stainless steel connector mounting nuts which require a special spanner wrench, and eliminate an EMI and water seal.

b. Use the smallest possible orderwire connector.

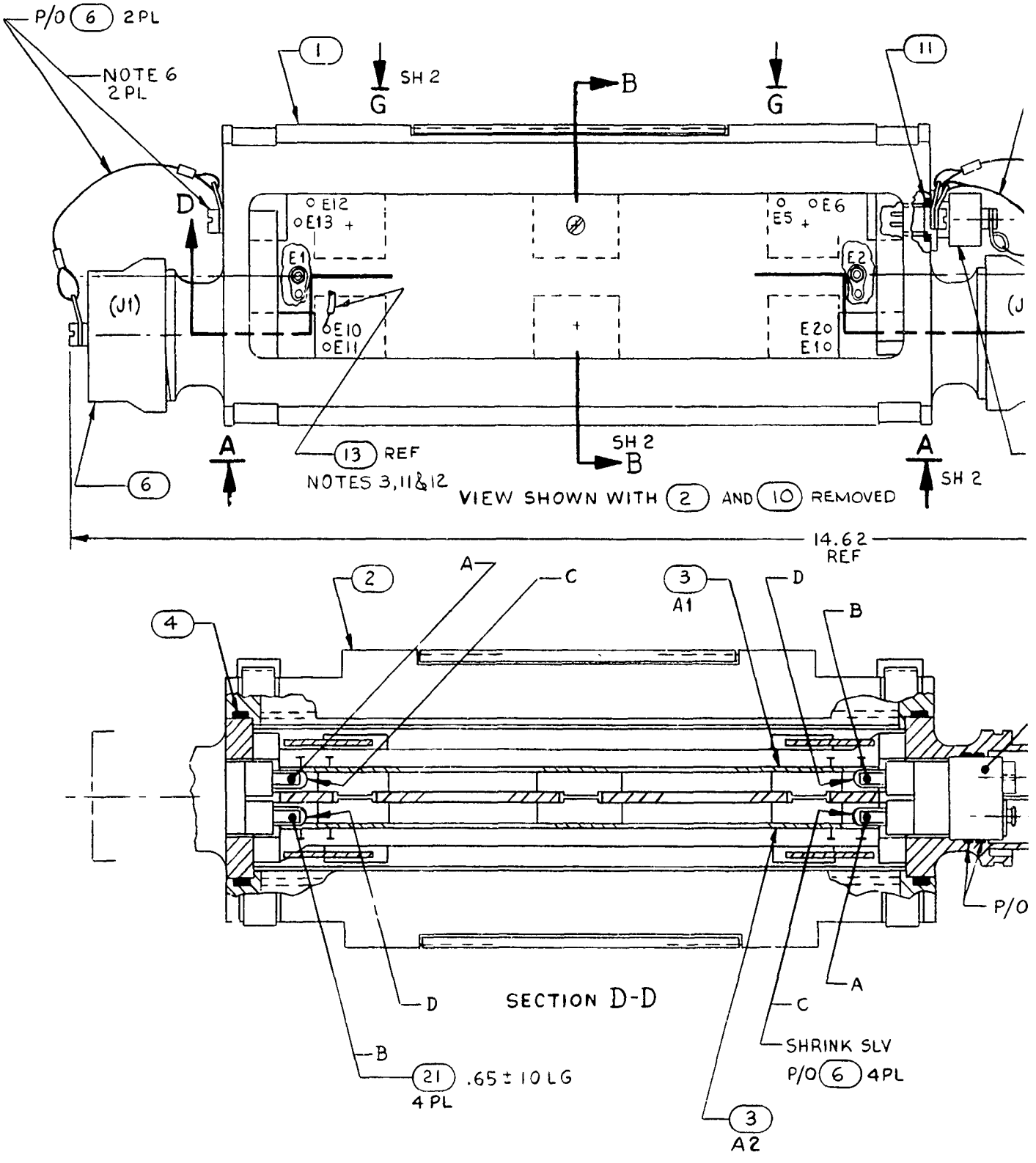
c. Use clamps to secure the covers to the housing and thereby improve producibility and reduce weight.

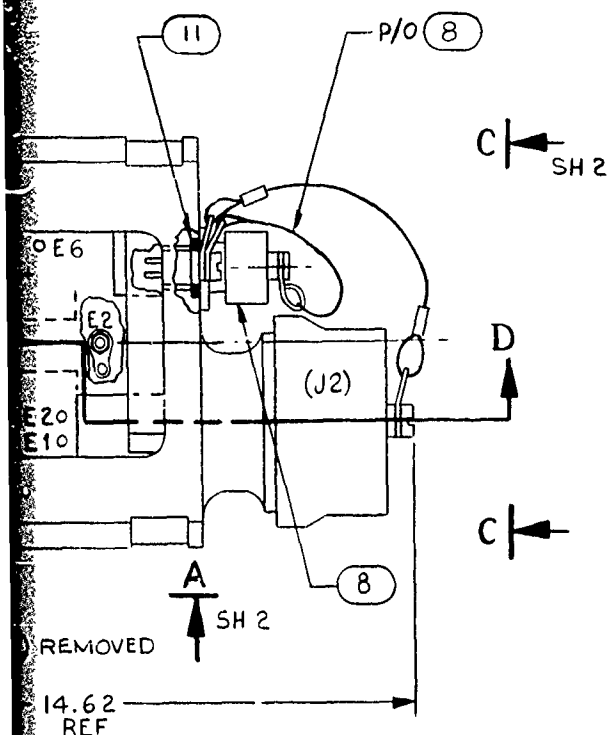
15.2.2 CARD DESIGN

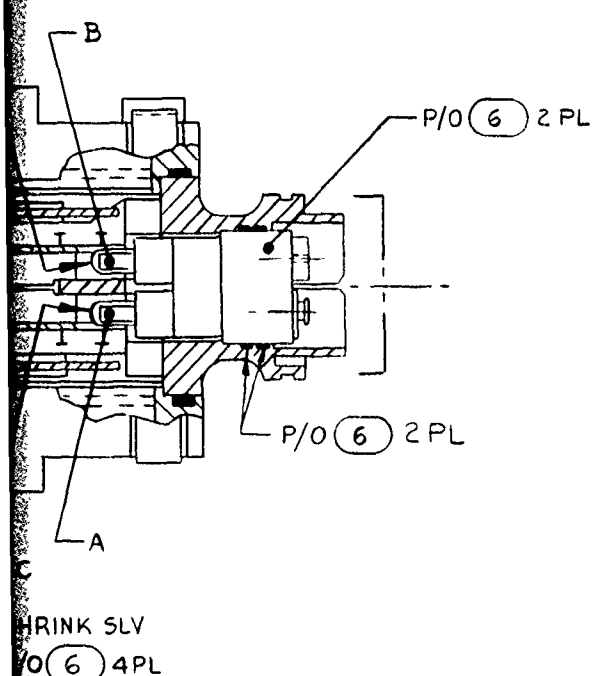
Because of interference considerations, both the LSPR and HSPR contain two identical PCB's separated by the aluminum center wall of the housing to provide the required bi-directional capability. Electrical connections to the boards are made via solder terminals and service loops to allow for ease of assembly and repair. Where large components are mounted, additional mechanical support is provided as part of the card assembly for structural integrity. The three layer HSPR card is shown in Figure 15-32.

15.2.3 WEIGHT ESTIMATES

The weight breakdown is shown in Table 15-5.


P/O (6) 2PL
NOTE 6
2PL
(1)
SH 2
G
B
G
(11)
D
E12
E13
E1
E6
E5
E2
(J1)
E10
E11
E20
E10
A
(13) REF
NOTES 3,11&12
SH 2
B
A
SH 2
(6)
VIEW SHOWN WITH (2) AND (10) REMOVED
14.62
REF
(2)
A
C
(3)
A1
D
B
(4)
P/O
D
SECTION D-D
A
C
B
SHRINK SLV
P/O (6) 4PL
(21) .65 ± 10 LG
4 PL
(3)
A2



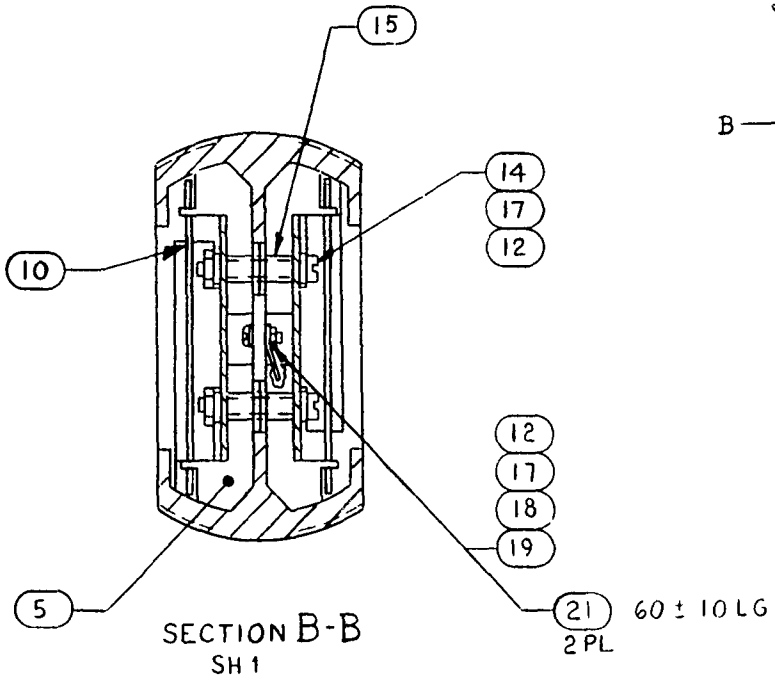


HRINK SLV
/O 6 4PL

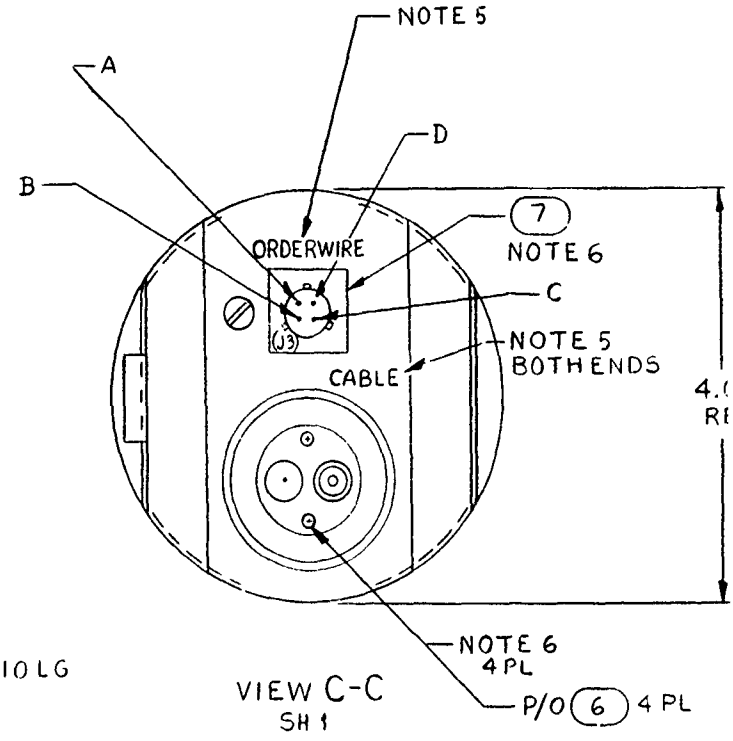
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. FOR SCHEMATIC DIAGRAM SEE SM-D-876106
3. FABRICATE AND ASSEMBLE PER SM-C-526772
4. TEST IN ACCORDANCE WITH SM-A-876107
5. MARK .12 HIGH BLACK CHARACTERS, GROUP II OR III PER MIL-M-13231. LOCATE APPROXIMATELY WHERE SHOWN
6. APPLY FIND NO. 22 AND 23 TO THREADED SECTIONS OF SCREWS (P/O FIND NO. 6) AND FIND NO. 7
7. SPACE TO BE PROVIDED AFTER THE SERIAL NUMBER, TO ADD A SUFFIX LETTER IF REQUIRED BY CONTRACT
8. PEEL ADHESIVE BACKING FROM FIND NO. 9 & 27. ORIENT AND LOCATE CENTRALLY AS SHOWN ON FIND NO. 2 & 1 RESPECTIVELY
9. ASSEMBLE FIND NO. 25 AND FIND NO. 26 PER QQ-S-781 TO A TENSION OF 280 ± 20 LBS
10. MARK SERIAL NO. PER NOTE 5
11. STRIP .38 AND TIN
12. STRIP .12 AND TIN

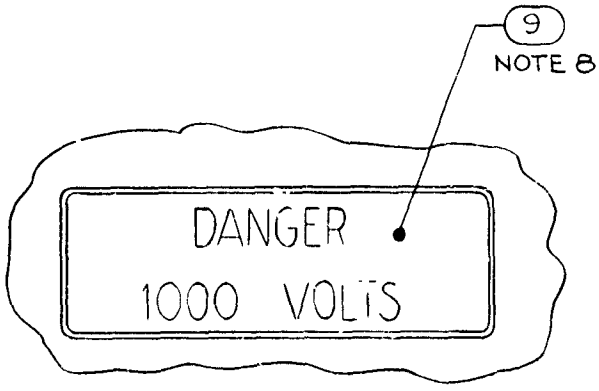
Figure 15-31. Low Speed Pulse Restorer (Sheet 1 of 2)



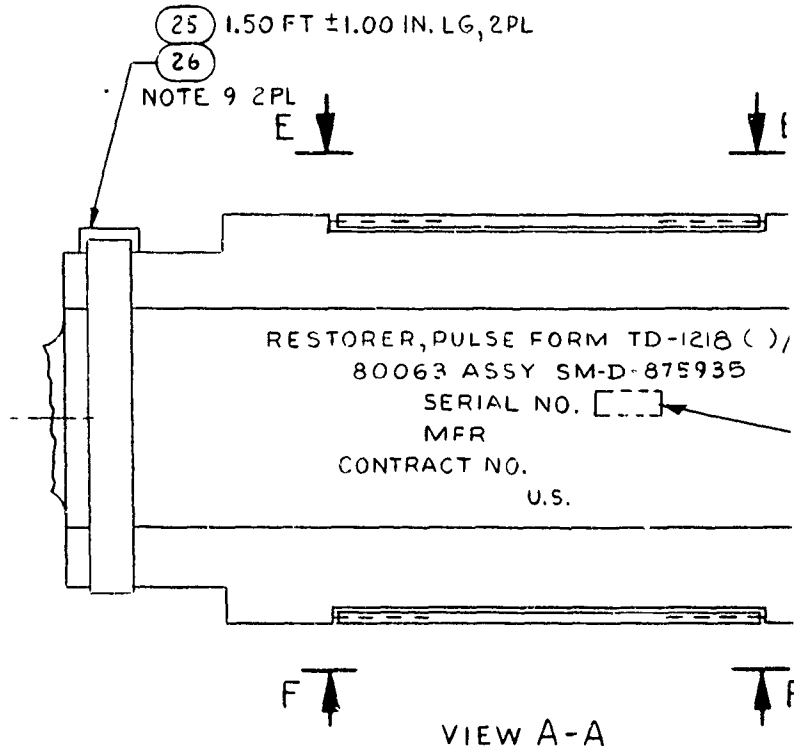
SECTION B-B
SH 1



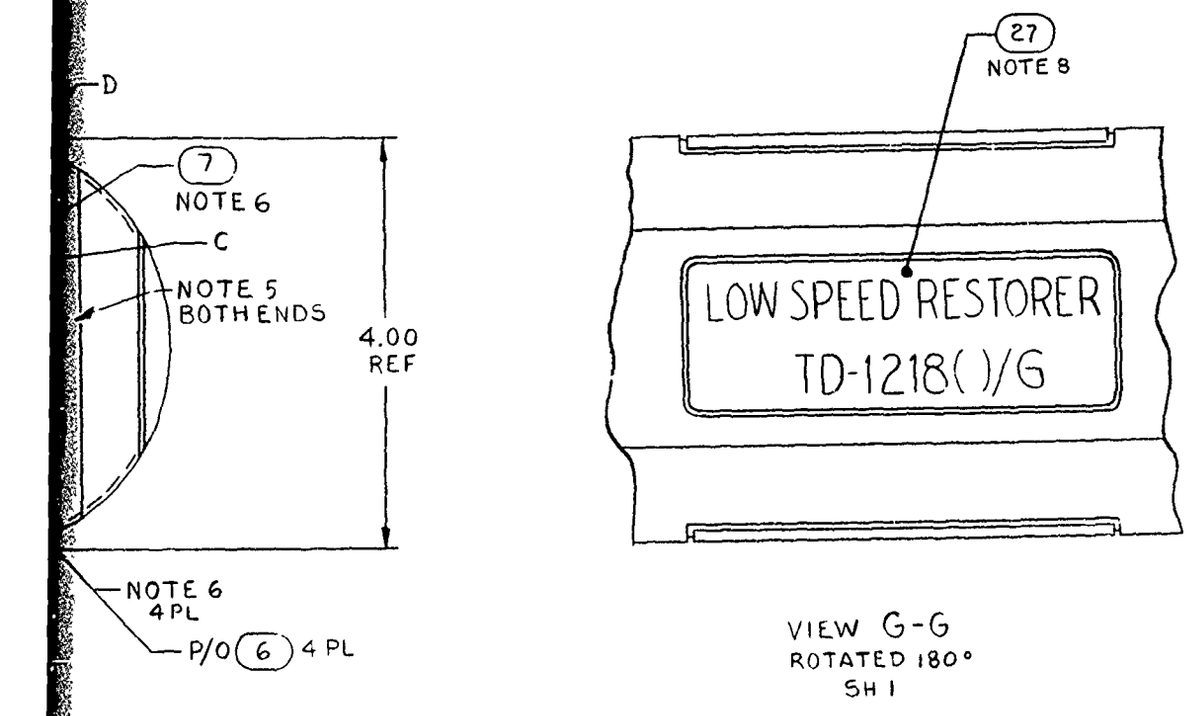
VIEW C-C
SH 1



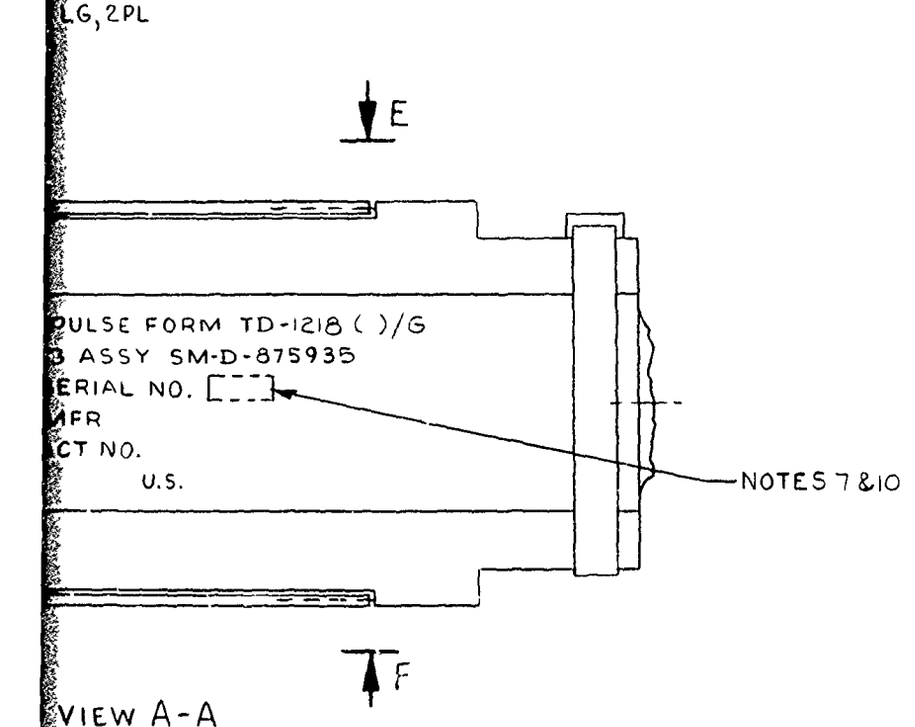
VIEWS E-E & F-F



VIEW A-A
SH 1



VIEW G-G
ROTATED 180°
SH 1

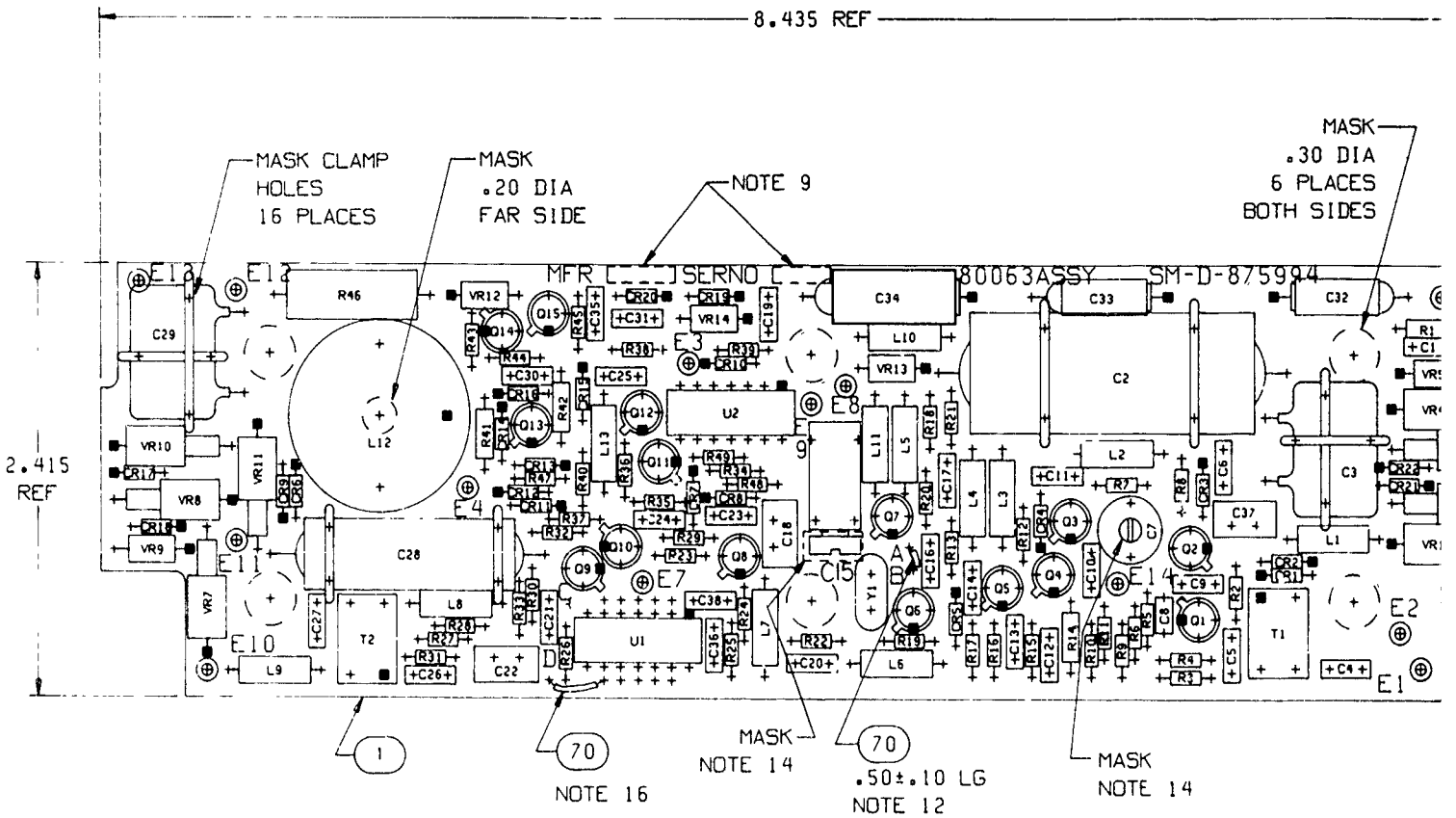


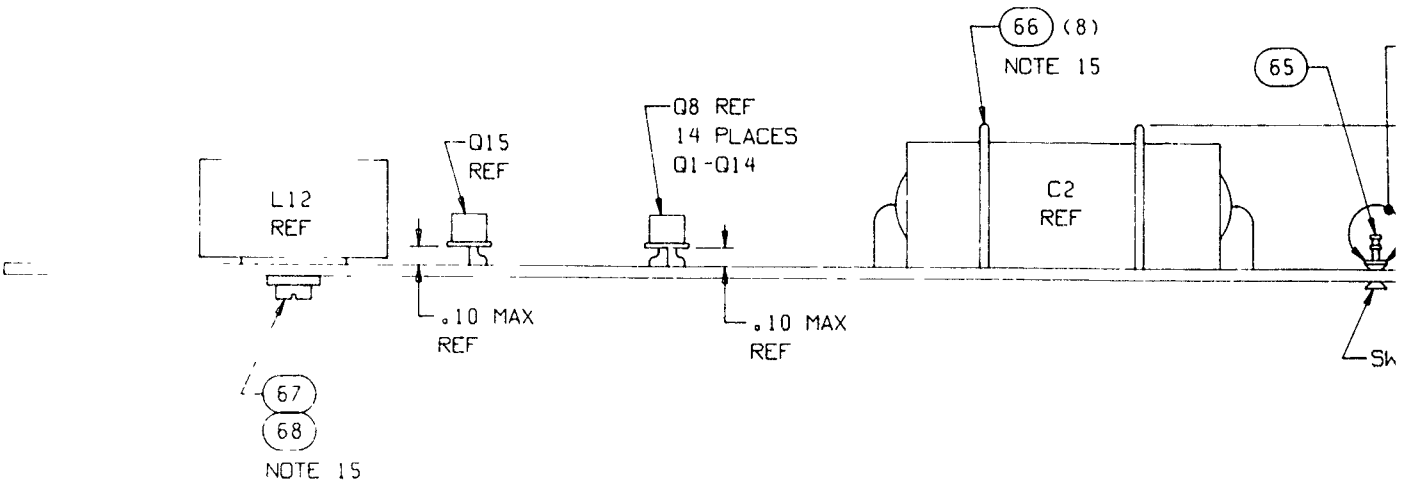
VIEW A-A
SH 1

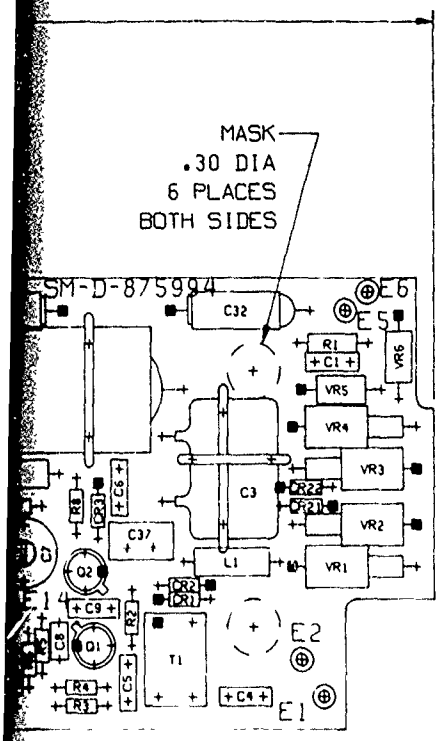
JUMPER LIST

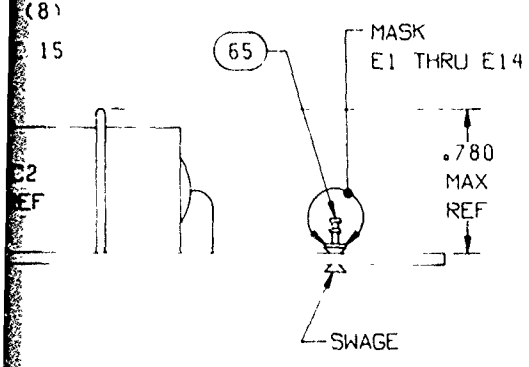
WIRE NO.	FIND NO.	DESCRIPTION			FROM		TO		NOTES
		AWG	COLOR	LENGTH	ATTACH PART FIND NO.	REF DES	ATTACH PART FIND NO.	REF DES	
1	13	20	RED	1.50	NOTE 12	J1-A	NOTE 11	A1E10	
2	28		ORN		12	J1-B		A2E1	
3	29		BLK		11	J1-C		E1	
4	29		BLK		11	J1-C		A1E11	
5	30		GRA		11	J1-D		E1	
6	30		GRA		11	J1-D		A2E2	
7	13		RED		12	J2-A		A2E10	
8	28		ORN		12	J2-B		A1E1	
9	29		BLK		11	J2-C		E2	
10	29		BLK		11	J2-C		A2E11	
11	30		GRA		11	J2-D		E2	
12	30		GRA		11	J2-D		A1E2	
13	31		WHT		12	J3-A		A1E6	
14	32		GRN		12	J3-B		A1E5	
15	33		YEL		12	J3-C		A2E13	
16	34	20	BRN	1.50	NOTE 12	J3-D	NOTE 11	A2E12	

Figure 15-31. Low Speed Pulse Restor
(Sheet 2 of 2)


8.435 REF
MASK CLAMP HOLES 16 PLACES
MASK .20 DIA FAR SIDE
NOTE 9
MASK .30 DIA 6 PLACES BOTH SIDES
2.415 REF
MFR SERNO 80063ASSY SM-D-875994
MASK NOTE 14
70 NOTE 16
70 .50±.10 LG NOTE 12
MASK NOTE 14


66 (8) NOTE 15
65
Q8 REF 14 PLACES Q1-Q14
Q15 REF
L12 REF
C2 REF
.10 MAX REF
.10 MAX REF
67
68
NOTE 15





12. ASSEMBLE FIND NO. 70 BETWEEN HOLES A AND B AFTER TEST
13. ALL COMPONENTS TO BE MOUNTED SO THAT A PORTION OF THE COMPONENT BODY IS AS CLOSE TO THE PRINTED WIRING BOARD AS PRACTICAL, WITH THE FOLLOWING EXCEPTIONS
    13.1 DUAL-IN-LINE PACKAGES TO BE MOUNTED .010 MIN-.060 MAX ABOVE SURFACE OF BOARD
    13.2 TRANSISTORS SHALL BE MOUNTED .10 MAX ABOVE SURFACE OF BOARD
14. APPLY FIND NO. 69 PER MIL-E-22118 TO AREAS SHOWN AFTER TEST
15. ASSEMBLE FIND NO. 66, 67 AND 68 AFTER CONFORMAL COAT
16. ASSEMBLE FIND NO. 70 BETWEEN EITHER HOLE C AND APPROPRIATE HOLE AT PIN 2, 3, 4, 5 OR 6 OF U1 OR HOLE D AND APPROPRIATE HOLE AT PIN 9, 10, 11, 12 OR 13 OF U1 AFTER TEST

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. ASSEMBLE AND SOLDER PER MIL-P-55640, OR FLOW SOLDER PER MIL-S-46844
3. MASK INDICATED AREA AND APPLY FIND NO.71 .001-.003 THK TO ALL EXPOSED SURFACES OF THE BOARD
4. WHEN REQUIRED, HAND SOLDER PER MIL-STD-454 REQUIREMENT 5
5. FOR SCHEMATIC DIAGRAM SEE SM-E-876104
6. COMPONENT ORIENTATION SYMBOL:
   6.1 ■ DENOTES EMITTER OR PIN 1 OF TRANSISTORS, POSITIVE END OF POLARIZED CAPACITORS, CATHODE END OF DIODES, AND PIN 1 OF MULTILEAD DEVICES
7. MARK .09 WHITE CHARACTERS USING NONCONDUCTIVE MATERIALS PER MIL-M-13231, GROUP II, LOCATE APPROX AS SHOWN
8. TEST IN ACCORDANCE WITH SM-A-876105
9. MARK MFR CODE IDENT AND SERNO PER NOTE 7
10. THE HIGHEST COMPONENT ABOVE SURFACE OF BOARD IS C2 WITH FIND NO. 66 MAX AT .780
11. IDENTIFICATIONS WITHIN COMPONENT OUTLINES, ON LEADERS, OR IN PARENTHESIS NOT TO BE MARKED

Figure 15-32. High Speed Circuit Card Assembly

TABLE 15-5

PULSE RESTORER WEIGHTS (LBS.)

Components	Target	Actual
Housing	2.38	2.29
Covers (2)	2.00	2.12
Modified UG-1837/U Connector Assys (2)	0.61	0.60
Shock Mounts (4)	0.85	0.64
Gaskets (2)	0.09	0.07
OW Connector and Cap Assembly	0.04	0.04
CCA's (2)	0.86 LS/0.95 HS	0.66 LS/0.68 HS
CCA Mounting Hardware (6)	0.06	0.06
Straps and Seals (2)	0.18	0.11
Miscellaneous (Decals, Lugs, Hardware, and Wire)	0.05	0.05
Total	7.12 LS 7.21 HS	6.64 LS 6.66 HS
Specified Maximum Weight is 7.5 Lbs. (3.4 kg)		

15.2.4 THERMAL DESIGN

15.2.4.1 General

The pulse restorer units dissipate relative low power and the thermal design is not considered critical. Power dissipations are:

High Speed PR: 3.4 watts maximum
Low Speed PR: 1.3 watts maximum

A thermal analysis to determine the maximum internal temperature for the units when exposed to the worst case thermal ambient (125°F air temperature plus 360 BTU/HR/FT^2 of solar radiation) has been performed and is given in the section below.

15.2.4.2 Thermal Analysis Pulse Restorers

a. Conditions, operating

1. Temperature: -50°F to +125°F
2. Solar Radiation: 360 BTU/hr/ft^2

b. Power dissipated = *4 Watts (Max) = 12.8 BTU/hr

*Use 4 watts; will yield conservative results

c. Configuration

For analysis purposes, assume the restorer be a cylinder 4.0 inches diameter by 12 inches long.

d. Assumptions

1. The restorer is suspended by the cables. Then there is no conduction path from case to ground or other surface. (This will yield conservative results.)
2. No heat is conducted away by the cables. (This will yield conservative results.)
3. The effects of 360 BTU/hr/ft^2 of solar radiation in a 125°F (52°C) ambient is to in essence raise the temperature from 125°F (52°C) to 160°F (71°C). (Ref.: Performance Spec. paragraph 4.2.6.3.1)

   Note: This is considered to be conservative for this type of item.

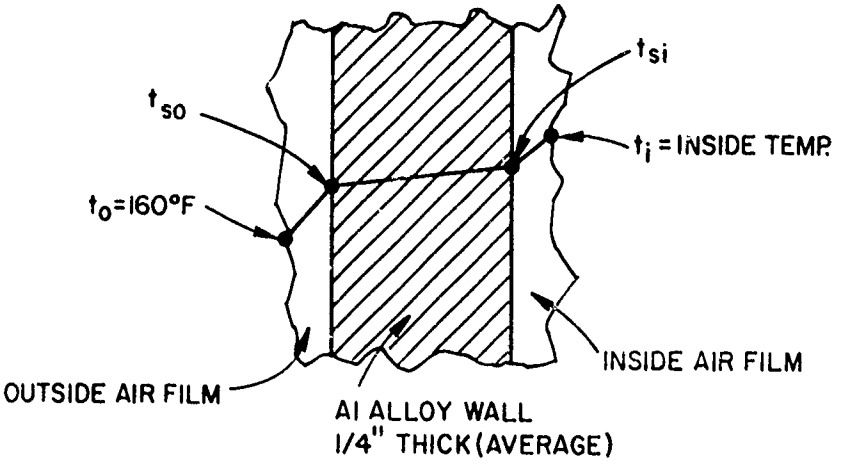
e. Calculations

1. Surface Area

   $A_s = \pi DL = \pi(4.0)(12.0)$

   $A_s = 150 \text{ in}^2 = 1.05 \text{ ft}^2$

2. Thermal Resistances/Profile



(a) Assume 50% convected through walls.

(b) Assume still air ($f_o = f_i = 1.65$)

$$\frac{1}{U} = R = \frac{1}{f_o} + \frac{X}{k} + \frac{1}{f_i}$$

where:

U = overall film coefficient

f_o = film coefficient outside

f_i = film coefficient inside

X = wall thickness

k = thermal conductivity of wall

$$\frac{1}{U} = \frac{1}{1.65} + \frac{.25/12}{131} + \frac{1}{1.65} \quad \left(\frac{.25}{12} \approx 0\right)$$

$$= 0.606 + 0 + 0.606$$

$$\frac{1}{U} = 1.212$$

$$U = .825$$

$$\frac{Q}{2} = UA\Delta t$$

$$6.4 = (1.05)(0.85)(\Delta t)$$

$$\Delta t = 7.2^{\circ}F \approx 8.0^{\circ}F$$

$$\therefore t_{so} = 160 + \frac{8.0}{2} = 164^{\circ}F$$

heat radiated

$$Q_R = .172\ eAF_a \left[\left(\frac{T_{so}}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4 \right]$$

$e = 0.9,\ A = 1.05\ ft^2,\ F_a \approx 1.0$

$$Q_R = .172(.9)\ (1.05)\ (1)\left[\left(\frac{164 + 460}{100}\right)^4 - \left(\frac{160 + 460}{100}\right)^4 \right]$$

$$= .162 \left[(6.24)^4 - (6.20)^4 \right]$$

$$Q_R = .162\ (1510.0 - 1477.6)$$

$$Q_R = .162\ (32.4)$$

$$Q_R = 5.3\ BTU/hr$$

This should be 6.4 BTU/hr, but this is close enough.

f. Conclusions

1. The internally dissipated heat for the worst case combination of conditions will raise the internal temperature approximately $8^{\circ}F$
2. Components should be selected for operation in a $76^{\circ}C$ ($166^{\circ}F$ ambient).

g. Local Conditions

1. Potential local conditions or hot spots were analyzed using a $76^{\circ}C$ ($166^{\circ}F$) ambient.
2. Key components were reviewed as the design progressed to ensure no local problem developed.

15.2.5 SHOCK AND VIBRATION

15.2.5.1 General

The service condition controlling the mechanical design is the dynamic load and resulting stresses developed from the 20-foot free fall drop test. Particularly vulnerable to these forces are the electrical components mounted on the printed wiring boards located within the structure as well as the housing itself. Two major areas were encountered with the original restorer and must be analyzed; (1) a structural analysis of the main housing, and (2) response analysis of the electrical components due to the impact loading on the housing.

15.2.5.1.1 Housing

The restorer housing is the main structural member and subjected directly to the impulse loading. Careful consideration was given to its design, particularly to factors which differentiate the impact problems from the problem of static design that include:

a. Manner of load application.

b. Structural characteristics, including deflections and stresses and effect of form and shape

c. Properties of materials as applicable to impact design.

Manner of Load Application. Three general features of the load application process are important in determining the resulting stresses and deflections in the housing: (1) time application of the load, (2) shape of load-time curve, and (3) number of repetitions of the load. If the time required for the load to rise from zero to the maximum (time application of load) is a small fraction of the fundamental natural period of vibration of the housing, then the important characteristic of the load-time curve is not its shape or maximum value of the load but the impulse which equals the area under the load-time curve. In actual cases of dynamic loading, the shape of the load-time curve is as much influenced by the dynamic response of the structure as by the nature of the load. Only experimental methods can determine this load-time relationship. However, for the preliminary analysis, previously obtained experimental data taken from drop tests on the first generation restorer was used.

Number of repetitions of the load is of concern insofar as fatigue strength of the part is concerned. In designing the restorer for this service, since six drop tests are required, a special requirement is to hold to a minimum the mass of the component as well as the mass of the parts supported, as actual loading under shock results from inertial reactions of these masses.

Structural Characteristics. Under impact loading, the restorer housing will absorb a certain amount of kinetic energy, which is temporarily stored in the structure in the form of potential energy of deformation. In other words, the resistance to impact loads is proportional to the amount of energy that can be stored. In the design of the housing, two important considerations are emphasized; (1) parts for impact loads will be designed to have the maximum volume of material stressed to the highest existing stress, and (2) surface irregularities causing stress concentration will be kept to a minimum.

Properties of Material. Strength and ductility are the major material properties considered in designing the housing for impact loading. It is a design requirement that the housing will not deform permanently when subjected to the 20-foot drop test, and consequently the material yield strength will be used as the design criteria. Under this requirement of no permanent deformation, it is quite feasible to use castings if stress concentrations are kept to a minimum.

Another important property in designing for impact resistance is the modulus of elasticity of the material. The strength of the housing is measured by its ability to absorb energy without permanent strain. The maximum stress in the housing is proportional to the square root of the modulus divided by the volume. Thus, if the housing is made of aluminum having a modulus of 10,000,000 psi, it will have an impact resistance of $\sqrt{3}$ times that of the housing if it were made of steel with a modulus of 30,000,000 psi, provided the volume is constant.

Impact Without Damping. Preliminary analysis on the proposed design indicates that relatively large deceleration exists on impact without external damping. This deceleration is determined by considering that the summation of the decelerating force-deflection diagram must equal the kinetic energy (KE) at impact, which in turn equals the potential energy (PE). For a restorer weight of five pounds,

$PE = (20)(12)\,5 = 1200$ in. lb.

Simply, on impact, the restorer impacting surface represents a compression member, and therefore the deflection (Y) of this impacting surface must react according to:

$$Y = \frac{PL}{AE}$$

where

P = applied load in pounds
L = length before loading in inches
A = area before loading in square inches
E = modulus of elasticity in pounds/in^2

and then

$$PE = KE \int_0^{Y_{max}} Pdy.$$

Solving this equation for the maximum load, it is found that P_{max} is approximately equal to 36,000 pounds. From Newton's second law, $P_{max} = ma$.

$$P_{max} = W(G_{max})$$

$$G_{max} \approx 7200 \text{ g's}$$

The results of this preliminary analysis agree with previous experimental and analytical data obtained on the original TD-206, a similarly designed equipment.

Even though a damping tube shows large reductions in shock loads, the same reduction at component level, the most critical area, can be achieved through internal isolation. Consequently, the approach taken is that external damping (rubber tube) on the housing is not used with inherent savings in weight, size and product cost, and improved storage and handling capability. Through extensive analysis and test, the housing is designed to survive the drop test without structural failure by eliminating major stress concentrations and keeping weight to a minimum. Considering manufacturability, maintainability, and shielding effectiveness, a cast structural member is the best candidate to answer all objectives of performance and cost in production.

15.2.5.1.2 Electronic Components

The response (deflection) of the components depends upon the damping and the natural frequency or period of the component support part. Features of the exciting function which are of particular interest are maximum amplitude, time duration and approximate shape. The peak value of pulse amplitude is an index to the intensity of dynamic loading, while the duration of the pulse is characteristic of its frequency effect. Both of these parameters must be known to obtain the response of the components.

Each component within the housing will respond in some degree to a pulse loading because it has both mass and stiffness. Intensity of the response, however, depends on how close the component structural frequency is to the forcing frequency. During the design analysis, natural frequencies of the components will be determined. If natural frequencies coincide with the forcing frequency, steps will be taken to reduce the stress levels by increasing component natural frequencies and changing the supporting structure cross section by maximizing the section modulus, the most efficient way to reduce stresses resulting from impact loading.

For definition purposes, consider the restorer to have a hard axis (printed circuit cards vertical on impact) and a soft axis (printed circuit cards horizontal on impact). Maximum response of the components occurs when the transmitted deceleration lies in the vertical or horizontal planes. Deflections and consequently stresses will depend on the ratio of the natural frequencies of the printed circuit cards to the forcing function. This forcing function will be determined by experiment. However, for the preliminary analysis, previously determined drop test data can be used. This results in a deceleration time pulse for a ten-foot drop test conducted on the previously designed restorer, where the accelerometer was attached directly to the printed circuit board. Based on previous data and observations, loads in the plane of the printed circuit boards are more significant than loads normal to the boards, as the former cause bending stresses on component attachments and the latter cause extension stresses.

Each component and the method of mounting was analyzed individually to determine whether or not it will survive the impact load without damping. It was found necessary on the basis of test and analysis, to provide damping and/or additional structural support to the critical components.

15.2.5.1.3 Structural Analysis

Analytical models of the components are selected based upon the fragility level and the transmitted impact. The models define weight, geometry and stiffness distributions at a series of nodes which in total describe the physical component. By using NASTRAN, a computerized structural dynamic program, the analytical models can be solved for natural frequencies and mode shapes. From the shock spectra data determined experimentally, loads can be selected for the appropriate frequencies and a detailed stress analysis of the individual part completed.

NASTRAN is a digital computer program for static and dynamic structural analysis by the finite element approach. The program embodies a lumped element approach wherein the distributed physical properties of a structure are represented by a model consisting of finite idealized substructures or elements that are interconnected at a finite number of grid points to which loads are applied. All input and output data pertain to the idealized structural model.

A serious problem in dynamic analysis is the definitio.. reasonable finite element model. Since the computing times for dynamic problems can easily be an order of magnitude greater than that required for static problems, the selection of a model that is adequate for the solution but not too large is an important consideration. NASTRAN provides for both the modal method and the direct method of dynamic problem formulation. In the modal method, the vibration modes of the structure in a selected frequency range are used as degrees of freedom, thereby reducing the number of degrees of freedom while maintaining accuracy in the selected frequency range. In the direct method, the degrees of freedom are simply displacements at grid points. The direct method will usually be more efficient for problems in which the bandwidths of the direct stiffness matrix is small and for problems with dynamic coupling in which a large fraction of the vibration modes are required to produce the desired accuracy. For

problems without dynamic coupling, that is for problems in which the matrices of the modal formulation are diagonal, the modal method will frequently be more efficient even though a large fraction of the modes are needed. The choice of method is one of the important user decisions.

15.2.5.1.4 Test Program

The importance of test programs cannot be emphasized strongly enough, as the impact pulse cannot be accurately defined in magnitude, duration and form in any other way. Simply, the purpose of the test was to acquire drop test response data (real time shock input and shock spectrum) for the purpose of evaluating models with and without damping and using this response data in the analysis for evaluating component reaction.

Each test model was instrumented with miniature accelerometers and dropped from a height of 20 feet onto a four foot by four foot by two inch thick fir platform. A sufficient number of drops was made to obtain correlative data. In addition, photographs were taken of the real time shock inputs for detailed study. This real time input is the actual deceleration level obtained from the drop tests and, due to the nature of the test, are of a non-repeatable nature.

15.2.5.2 Preliminary Analysis

An analysis has been prepared to determine stress/acceleration levels, and maximum displacements for the printed circuit board in the Pulse Restorer when subjected to the 20 foot drop test. This analysis was coupled with previous analysis and test data to establish the design conditions; results are summarized below.

15.2.5.2.1 Previous Test Results

The results obtained include the real time shock acceleration levels measured on the G10 boards and the shock spectrum associated with this pulse for a five percent damped single degree of freedom system. This data was obtained in three orthogonal axes for locations on the G10 boards. The unit was dropped in various orientations with the unit logitudinal axis being approximately parallel to the ground during impact, and perpendicular to the ground during end drops.

15.2.5.2.2 Development of Component Structural Loads

The prediction of detailed component structural loading for this type of system and environment is extremely difficult on an analytical basis alone; therefore, the previous tests explained above were used in the development of representative component loads.

Test results obtained on the previous "hard" mounted design indicate a real time acceleration level of 2500 to 4000 g's exists on the component boards when the unit is subjected to the twenty foot drop test. It is reasonable to estimate the same level would exist on the present design if it were "hard" mounted. It is now possible to calculate at the equivalent spring rate supporting the boards if they are considered as a single degree of freedom system. This spring rate would account for the stiffness of the wooden test fixture, structural housing, and G10 boards themself. This procedure was followed and a spring rate of 11,719 pounds per inch was calculated, for the "hard" mounted design.

In order to reduce the component loads, an isolation system was used. This system was designed so that the energy of the isolated mass due to the drop height can be absorbed without exceeding the displacement requirements due to clearances. This isolation system has a spring rate of 12,569 pounds per inch in a direction normal to the boards. The isolation system can be thought of as a second spring in series with the initial spring calculated from the test data. Since the two spring rates are now known an equivalent spring rate for the system can be calculated. This was calculated to be 5,065 pounds per inch. Now using the equivalent spring rate, real time accelerations or the boards can be predicted. The detailed calculations of these analysis are summarized in Table 15-6.

15.2.5.3 Drop Height-Effect on Component Loading

The results of a study for the direction normal to the boards are presented in Figures 15-33 and 15-34. Curves (1) and (2) of Figure 15-33 show the difference between using and not using the isolation system. It can be seen that a

TABLE 15-6

STRESS/ACCELERATION SUMMARY

Item	Direction of Response		
	X1 Lateral to Component Bd.	X2 Perpendicular to Component Bd.	X3 Parallel to Length of component Bd.
Isolation System Linear Spring Rate (lb/in.)	10,896	12,569	9,577
Isolation System Natural Frequency (Hz)	344	370	323
Displacement of Isolated mass due to drop test (in.) (clearance required)	(.191)	.169	.191
Estimated real time acceleration imparted to board from drop tests (G's)	1,735	1,800	1,677
Estimated maximum response to govern individual component design (G's)	2,000	2,000	2,000

20.0 foot drop with an isolated system is equivalent to a 10.4 foot drop without the isolation system in terms of the loadings applied to the components.

Figure 15-34 shows drop height versus "G" forces on the boards considering the non-linearity of the isolation system. These results are not dramatically different from the linear spring results of Figure 15-33.

The design for the High Speed and Low Speed Pulse Restorer is similar to that of the TD 206 B/G. Using these values, a curve of weight vs drop height was generated and is illustrated in Figure 15-35.

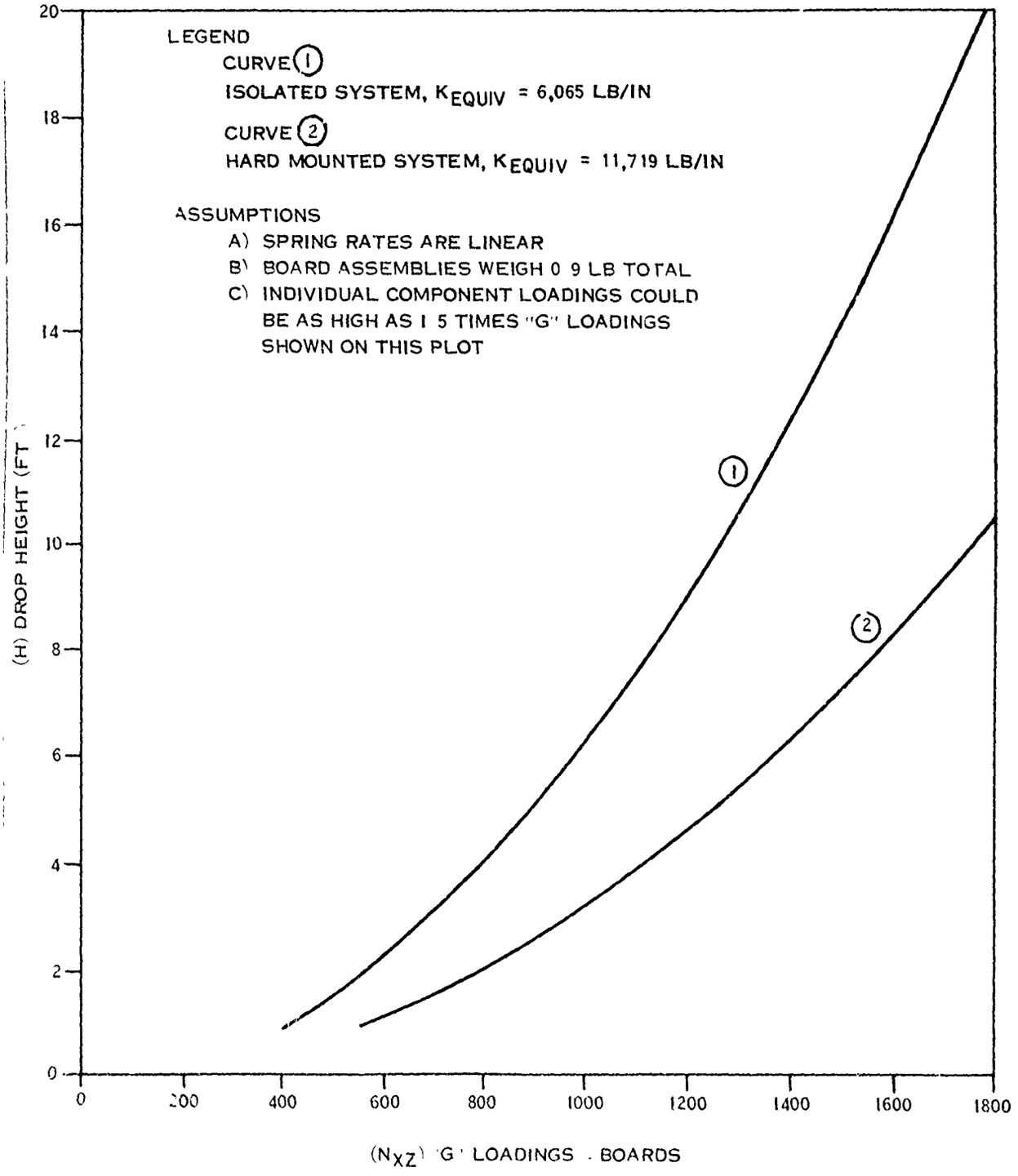


Figure 15-33. Plot of Drop Height vs. "G" Forces on Board (Linear Spring Rates) - X_2 Direction (Normal to Board)

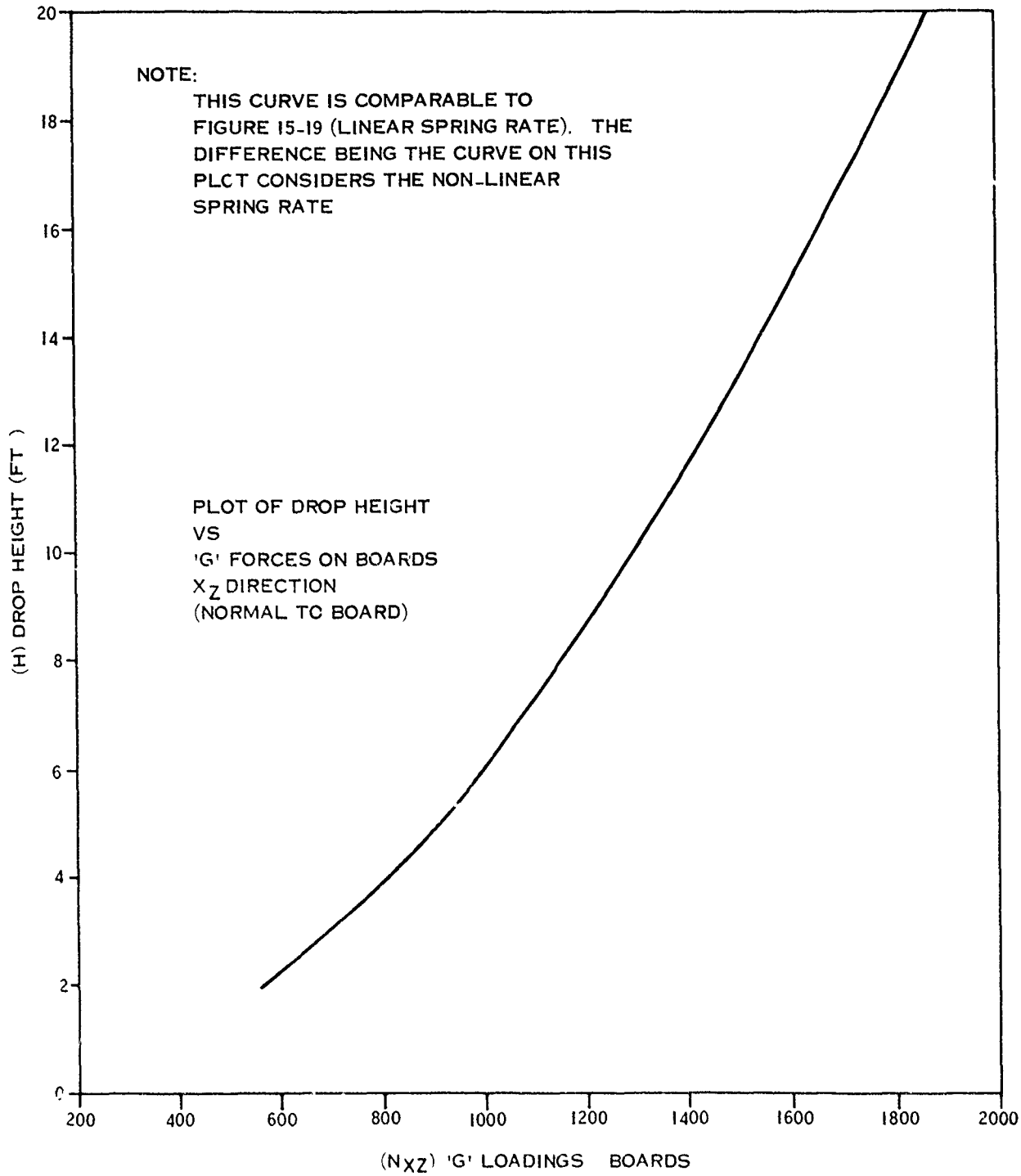


Figure 15-34. Plot of Drop Height vs. "G" Forces on Board (Non Linear Spring Rates) - X_2 Direction (Normal to Board)

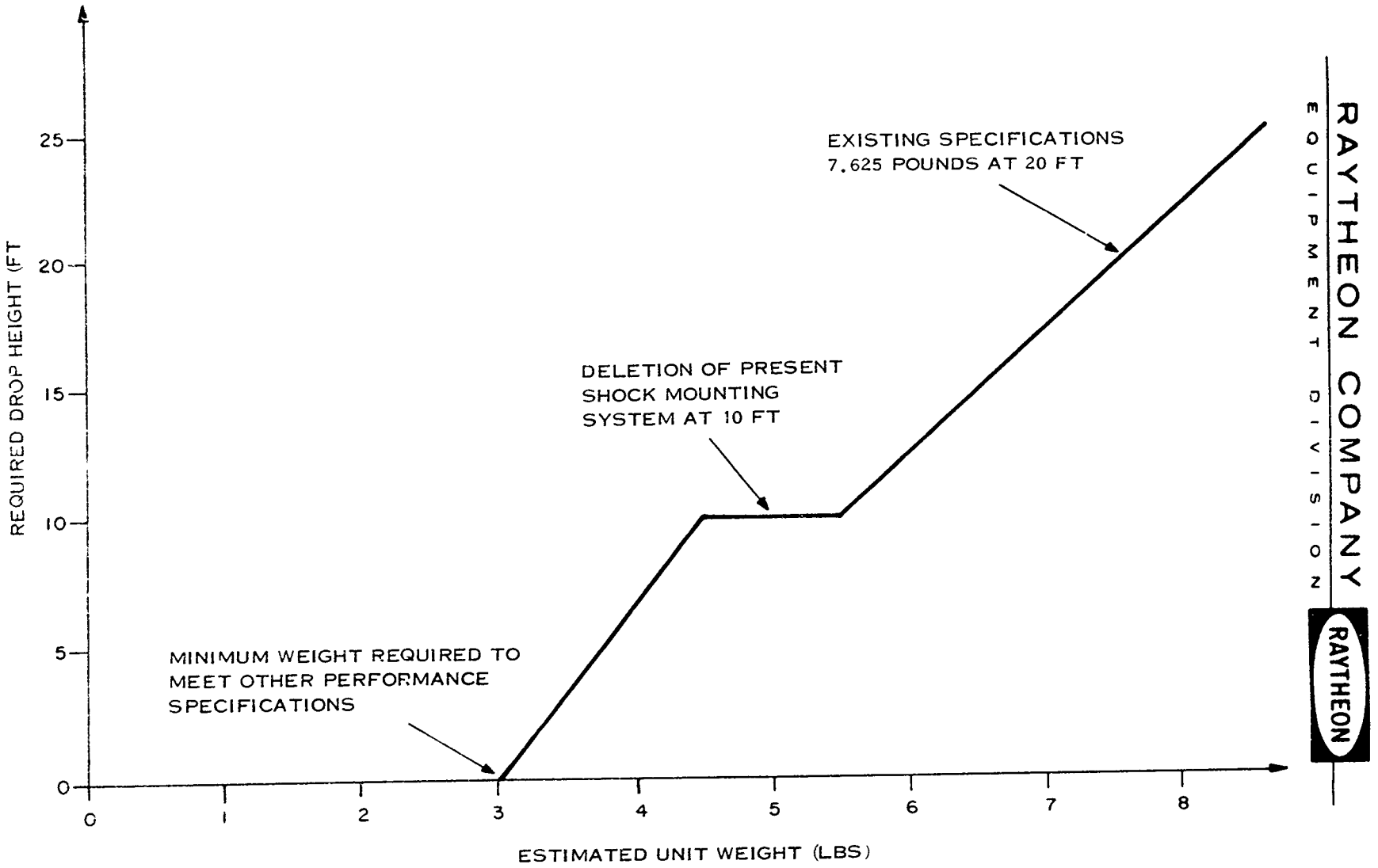


Figure 15-35. Estimated Restorer Weight vs Required Drop Height

15.2.6 EMI DESIGN

15.2.6.1 General

The EMI design principles discussed in paragraph 15.1.5 for the Shelter mounted units are applied to the Pulse Restorers as well. Differences or special considerations relative to the Pulse Restorers are discussed below.

15.2.6.2 Gasket

The Pulse Restorers are of a cylindrical design with two removable covers (see Figure 15-36). The basic design is the same as used on the TD-206 B/G which successfully passed the EMI tests. Each cover is identical in size and construction and contains a groove for the sealing gasket. The groove design provides for a positive stop to avoid excessive pressure and the stiff cover design provides uniform pressure to insure good contact at all surfaces. A conductive "O" type gasket is used to provide the necessary EMI seal and a water seal to insure watertightness when submersed in three feet of relatively cold water.

15.2.6.3 Finish/Connector Mounting

Other aspects of the EMI design are the conductive finish, E512 per MIL-F-14072, and integration of the cable connector shells into the main housing. These features greatly reduce the resistance at the respective mechanical interfaces.

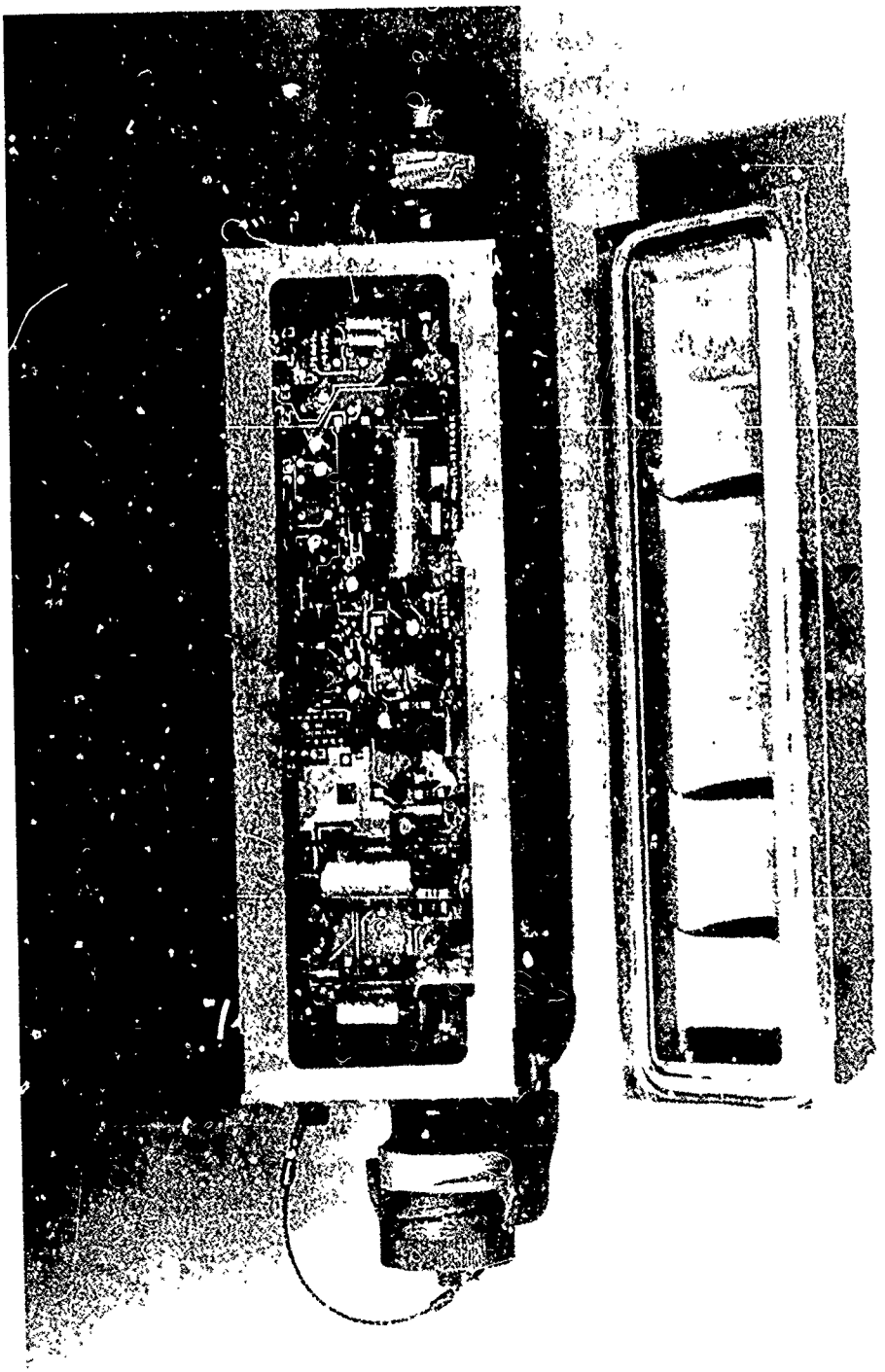


Figure 15-36. DGM Pulse Restorer

15.2.7 OTHER ENVIRONMENTAL CONDITIONS

The following environmental requirements for the Remote Unattended Pulse Restorer (PRs) influence the design beyond those previously listed under Shelter Mounted Equipments, and the 20 foot drop test previously discussed.

The PRs are designed for immersion to a depth of three feet, and are fully operable while unattended in inclement weather conditions, including rain, dust, snow, sleet, etc. The electronics are sealed from the outside ambient via combination RFI and water tight resilient gaskets at all openings/penetrations. An "O" ring type gasket is used under the two covers and a positive stop is provided to avoid "gasket set".

Raytheon is casting the housing with the cable connector shells as integral parts. This eliminates an opening and an "O" ring at each of the two connectors and thereby simplifies the immersion design. Also, because the shell dimensions which provide an O-ring seal around the plastic insert are now machined (as opposed to die cast in the standard UG-1837/U connector) these seals (occasionally problem areas in TD-206 B/G design) are greatly improved.

15.3 COU

15.3.1 CASE/CHASSIS DESIGN

The COU combination case is designed to meet MIL-T-4734; parts, materials and processes will be selected in accordance with MIL-P-11268. The case center section is fabricated from aluminum sheet and extrusions welded or bonded together, while the covers (top and bottom) are fabricated from ABS and aluminum extrusions bonded together. The covers feature the female halves of the sealing extrusions and immersion-tight gasket, latches, half of the separable hinges, protective/shock absorbing bumpers, and air pressure relief valves. The case center features the male half of the sealing extrusions, latch receptacles, a carrying handle, a sling, and half of the separable hinges. The top extrusion in the case center provides a flange for mounting the chassis on a rain/EMI gasket. The bottom extrusion in the case center provides a flange, to which is welded a shear plate. A fully sealed battery compartment is included in the case center. This compartment and the two BA-5599( )/U batteries held there are accessible through

a rain tight door on the bottom shear plate. Because of possible build up of corrosive gases from the battery, the compartment is vented directly to the atmosphere through a pressure relief valve.

The electrical connection between chassis and batteries (case) is accomplished via a bullpin guided connector.

The plug in chassis of the COU includes the front panel and is fabricated from various aluminum sheet and extruded alloys designed to support and contain the electronics. The chassis is a welded assembly to insure structural integrity. Accessibility for assembly and repair will be a main feature of the chassis.

The COU is finished in accordance with MIL-F-14072, painted olive drab, color #24087 of FED-STD-595, except the front panel will be #26250. Front panel marking will be Group I, conforming to MIL-M-13231. The selection of electronic parts, devices and related electronic techniques, technologies and electronic materials, including microelectronic, is in accordance with MIL-P-11268. Moisture-resistant controls and front panel components is used in conjunction with gaskets and additional sealing to enable the COU to be operational during inclement weather.

15.3.2 CARD DESIGN

The COU only contains two double sided PCB's approximately 30 in^2 in size. Electrical connections to the card are made via a two piece connector. In order to restrict shock levels and deflections experienced by the components to safe levels, the boards will be adequately supported in all planes and individual components may be supported by clamps. Also, to allow for easy extraction the board assemblies include extracting levers.

15.3.3 THERMAL

The power dissipated in the COU is only 0.15 watts continuous, and 3.0 watts for extremely short periods. It was estimated that the temperature rise within the enclosure due to equipment heat will be less than 1°C and may be neglected.

Accordingly, then the internal temperature will be that induced by the 125°F ambient air and the solar radiation, which will result in an internal temperature of 160°F maximum. Components were selected to be compatible with this temperature level.

15.3.4 EMI DESIGN

15.3.4.1 General

The EMI design principles discussed in paragraph 15.1.5 for the Shelter Mounted Units are applied to the Cable Order Wire Unit. Differences or special considerations relative to the COU are discussed below.

15.3.4.2 Front Panel

The front panel of the COU is rain tight in the operational position. Accordingly the front panel to case gasket is a combination EMI and water type gasket.

Similarly all front panel components (switches, lights, meters, etc.) and the penetration of the panel for these components are treated for water tightness as well as EMI.

15.3.5 OTHER ENVIRONMENTAL CONDITIONS

The following environmental conditions for the Cable Orderwire Unit influences the design beyond those previously discussed for the Shelter Units and the 48" transit case drop test which is discussed in paragraph 15.4.

15.3.5.1 Rain/Immersion

The units are fully closed units which maintain thermal control by natural cooling techniques. This eliminates the need for openings in the case and greater simplifies the mechanical design/configuration for exclusion of rain, dust, sand, etc. In essence, the problem becomes one of treating the front panel and its components and the penetrations of the panel by these components to exclude the rain. Also the battery compartment is rainproof.

This is accomplished by (1) selecting parts (e.g., lamp holders connectors, switches, etc.) which are sealed type components, (2) using gaskets at each panel penetration, (3) achieving a relatively uniform gasket pressure (5 to 10 psi) between the panel and the case. Gaskets/seals are designed to minimize gasket set due to excessive bolt pressure and the low temperature conditions.

15.4 RLGM and RMC

See Volume II.

15.5 SUMMARY OF ENVIRONMENTAL REQUIREMENTS AND TESTS

A summary of the environmental requirements and the corresponding environmental tests for all DGM units is presented in Table 15-8.

Environmental Condition \ Unit	Shelter Mounted Equipments LGM, LM, TGM, MGM, GM, CDM/LS, CDM/HS, RLGM/CD		Unattended Remo HSPR, I	
	Design Requirement (Spec. Para. 3.2.5.1)	Test Requirement (Spec. Para. 4.2.6.2)	Design Requirement (Spec. Para. 3.2.5.2)	
High Temperature	145°F Operating 160°F Non-Operating	MIL-STD-810B, Method 501, Proc. II, Step 4 to be 160°F and Step 7 to be 145°F.	+125°F plus solar radiation of 360 BTU/Hr/FT^2 Operating, +160°F Non-Operating.	MIL-S Step 4 160°F radiat
Low Temperature	-25°F Operating -70°F Non-Operating	MIL-STD-810B, Method 502, Proc. I, Step 2 to be -70°F for 2 hours minimum after stabilization and Step 4 to be -25°F.	-50°F Operating -70°F Non-Operating	MIL-S Step 2 mum be -5(
Altitude	10,000 ft Operating 40,000 ft Non-Operating. Maximum rate of change 2500 ft/min.	MIL-STD-810B, Method 500, Proc. I, Step 2 shall be 40,000 ft. Rate of change shall not exceed 2500 ±250 ft/min.	10,000 ft Operating 40,000 ft Non-Operating. Maximum rate of change 2500 ft/min.	MIL-S Step 2 shall
Humidity	Prolonged tropical exposure. Operating and Non-Operating.	MIL-STD-810B, Method 507, Proc. II, Step 6 measurement to be taken in last 5 hours of last cycle.	Prolonged tropical exposure. Operating and Non-Operating.	MIL-S Step 6 last 5
Dust	Blowing dust particles. Operating and Non-Operating.	MIL-STD-810B, Method 510, Proc. I, Steps 1, 2 and 3 wind velocity shall be limited to 200 ±100 ft/min.	Blowing dust particles with wind speeds of 35 knots for remote equipment. Operating and Non-Operating.	MIL-S
Salt Fog	Salt-Sea Atmosphere. Non-Operating.	MIL-STD-810B, Method 509, Proc. I Operating Configuration.	Salt-Sea Atmosphere. Non-Operating.	MIL-S Opera
Fungus	No fungus nutrients. Non-Operating.	MIL-STD-810B, Method 508, Proc. I.	No fungus nutrients. Non-Operating.	MIL-S
Vibration and Shock	Vehicular transport over rough roads and cross-country terrain, common carrier transport servicing. Non-Operating.	Vibration 1.5 g's, 5-200-5 Hz cycle, sweep rate 12 minutes, 5-1/2 hours per axis. Shock 15 g half sine 11 ms pulse, 6 shocks per axis, bench handling. MIL-STD-810B, Method 516.1, Proc. V.	Common carrier transport. Non-Operating.	Bounc Proc. 5-200 utes,
Shock Drop	-	-	Rough handling, 6 drops from 20 ft.	MIL-S excep
Rain Fall	-	-	-	
Immersion	-	-	At a depth of 3 ft for 2 hours. Non-Operating.	MIL-S imme shock

Table 15-8. DGM Equipment Environmental Design and Test Requirements

Unattended Remote Equipments HSPR, LSPR		Remote Equipments RLGM, RMC, COU	
Design Requirement c. Para. 3.2.5.2)	Test Requirement (Spec. Para. 4.2.6.3)	Design Requirement (Spec. Para. 3.2.5.3)	Test Requirement (Spec. Para. 4.2.6.4)
plus solar radiation BTU/Hr/FT^2 Oper- +160°F Non-Operating.	MIL-STD-810B, Method 501, Proc. II, Step 4 to be 160°F and Step 7 to be 160°F (this includes the effects of solar radiation).	+125°F plus solar radiation of 360 BTU/Hr/FT^2 Operating, +160°F Non-Operating.	MIL-STD-810B, Method 501, Proc. II, Step 4 to be 160°F and Step 7 to be 160°F (this includes the effects of solar radiation).
Operating Non-Operating	MIL-STD-810B, Method 502, Proc. I, Step 2 to be -70°F for 2 hours minimum after stabilization and Step 4 to be -50°F.	-50°F Operating, -70°F -70°F Non-Operating	MIL-STD-810B, Method 502, Proc. I, Step 2 to be -70°F for 2 hours minimum after stabilization and Step 4 to be -50°F.
ft Operating ft Non-Operating. um rate of change /min.	MIL-STD-810B, Method 500, Proc. I, Step 2 to be 40,000 ft. Rate of change shall not exceed 2500 ±250 ft/min.	10,000 ft Operating 40,000 ft Non-Operating. Maximum rate of change 2500 ft/min.	MIL-STD-810B, Method 500, Proc. I, Step 2 to be 40,000 ft. Rate of change shall not exceed 2500 ±250 ft/min.
ged tropical ex- . Operating and perating.	MIL-STD-810B, Method 507, Proc. III, Step 6 measurements to be taken in last 5 hours of last cycle.	Prolonged tropical exposure. Operating and Non-Operating.	MIL-STD-810B, Method 507, Proc. III, Step 6 measurements to be taken in last 5 hours of last cycle.
g dust particles with peeds of 35 knots mote equipment. ting and Non-Operating.	MIL-STD-810B, Method 510, Proc. I.	Blowing dust particles with wind speeds of 1750 ft/min. Operating and Non-Operating.	MIL-STD-810B, Method 510, Proc. I.
ea Atmosphere. perating.	MIL-STD-810B, Method 509, Proc. I, Operating Configuration.	Salt-Sea Atmosphere. Non-Operating.	MIL-STD-810B, Method 509, Proc. I, Operating Configuration.
gus nutrients. Operating.	MIL-STD-810B, Method 508, Proc. I.	No fungus nutrients. Non-Operating.	MIL-STD-810B, Method 508, Proc. I
on carrier transport. Operating.	Bounce MIL-STD-810B, Method 514.1, Proc. XI, Part 2. Vibration 1.5 g's, 5-200-5 Hz cycle, sweep rate 12 minutes, 5-1/2 hours per axis.	Field transportation by military vehicles and rough handling. Non-Operating.	Bounce MIL-STD-810B, Method 514.1, Proc. XI, Part 2. Vibration 1.5 g's, 5-200-5 Hz cycle, sweep rate 12 minutes, 5-1/2 hours per axis.
handling, 6 drops 20 ft.	MIL-STD-810B, Method 516.1, Proc. II, except 6 drops from 20 ft.	Rough handling, 26 drops from 4 ft.	MIL-STD-810B, Method 516.1, Proc. II, (4 ft drop).
-	-	Heavy precipitation with intermittent wind operating.	MIL-STD-810B, Method 506, Proc. I, operated in last 10 minutes of 30 minute period.
depth of 3 ft for 2 hours. Operating.	MIL-STD 810B, Method 512, Proc. I, immersion before and after vibration/ shock testing.	At a depth of ft for 2 hours. Non-Operating.	MIL-STD-810B, Method 512, Proc. I, immersion before and after vibration/ shock testing.

15.6 ENVIRONMENTAL TESTS

Each DGM equipment was tested in accordance with the requirements of paragraph 4.2.6 and Table III of the specification. The tests performed, the sequence of tests, and the number of test samples to be used are described in the following paragraphs, quoted from MIL-STD-810.

"Prior to conducting any environmental condition tests, the equipment shall be operated under the following conditions: temperature $77^{\circ} \pm 5^{\circ}$F; humidity 50 $\pm 5\%$; and barometric pressure corrected to between 28 and 32 inches of mercury. Data will be recorded to provide criteria for checking satisfactory performance during and at the conclusion of each of the environmental condition tests when required. The operational tests will be in accordance with MIL-STD-810." Figure 15-37 is the proposed environmental test schedule.

"The tests have been sequenced in accordance with Table III (Test Sequence for Limited Sample Size) of TT-B1-2202-0013. Parallel testing has been utilized wherever possible, e.g., combining units for exposure to the climatic environments, to achieve the most efficient use of personnel and facilities within the sequencing constraints of Table III of TT-B1-2202-0013. Two of each unit will be used for these tests. A larger test sample size may be used depending upon the availability of EDM equipments at the start of the PQT program. Also a number of units may be combined for exposure to the climatic environments dependent upon program and test schedules at the time of test."

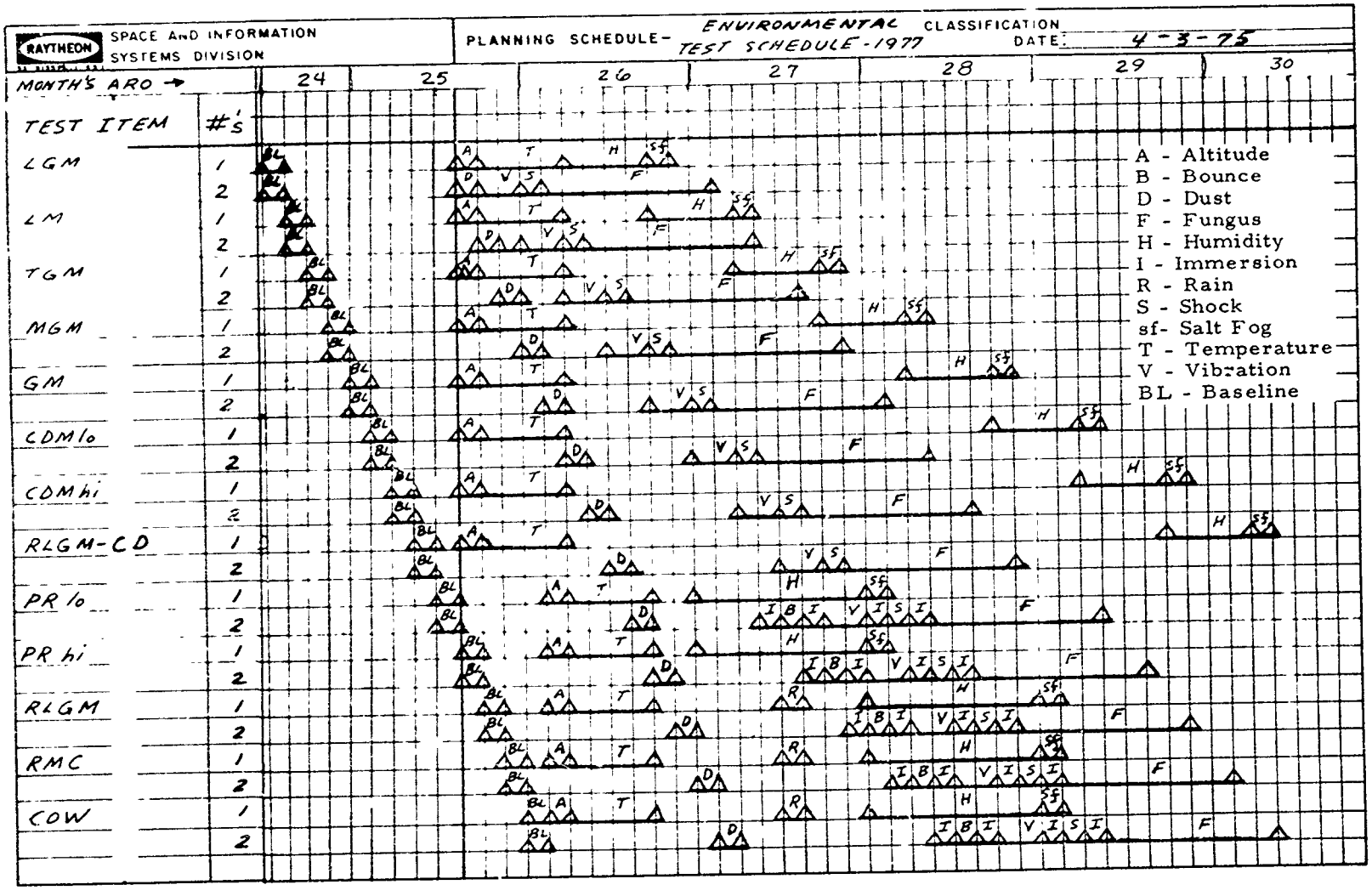


Figure 15-37. Environmental Test Schedule

SECTION 16

MAINTAINABILITY

16.1 GENERAL

All DGM units which provide communication functions share essentially a single packaging concept consisting of a power supply and a number of PCB assemblies in each unit. These units, or boxes, have requirements for $\overline{M}_{ct}$ of 15 minutes or less and $M_{max\ ct}$ of 30 minutes (95th percentile). Units which are exempted from the maintainability requirement either do not provide a primary communication function (cable orderwire unit) or are repaired by replacement (High Speed Pulse Restorer and Low Speed Pulse Restorer).

With the common physical packaging and built-in fault detection, DGM units falling under the maintainability requirement have essentially the same MTTR at the organizational level. A preliminary maintainability estimate for MTTR, used here synonymously with $\overline{M}_{ct}$, showed that DGM units furnished by Raytheon would have no difficulty in meeting the $\overline{M}_{ct}$ requirement of 15 minutes maximum, for fault diagnosis, repair, and checkout. Administrative delay time is not included when determining corrective maintenance time.

16.2 SPECIAL MAINTENANCE FEATURES

Raytheon's designs for the DGM family of units exceeded the M_{ct} requirement of TT-B1-2202-0013, by a significant margin. This was made possible by incorporating those maintainability features which provide:

- Quick means of detecting and isolating faults to the replaceable assembly level and using LED indicators on power supply assemblies and PCB assemblies.
- Ease of access to all replaceable assemblies in units located at the operating site.
- Speed of assembly interchange and checkout.

None of the features requires special skill levels to implement - all are well within the capabilities of service personnel using the equipment at organizational level. In addition, repairs to DGM replaceable assemblies at depot or repair locations are facilitated by the test points and fault LEDs on assemblies which require troubleshooting.

16.3 MAINTAINABILITY PROGRAM TASKS

The maintainability program for the DGM family of units was based on MIL-STD-470 as required by paragraph 4.1 of the DGM SOW. Program tasks elements which were included are as follows:

16.3.1 MAINTAINABILITY PROGRAM PLAN

This was submitted as CDRL and defines the maintainability program milestones and planned activities in accordance with the requirements of MIL-STD-470.

16.3.2 DESIGN REVIEWS

Design reviews are an integral part of EDL's approach to equipment design. They provide an additional program vehicle for validation of equipment design prior to the production phase. The Policies and Procedures on design reviews currently in effect at EDL will be followed as they apply to the appropriate phases of design activity.

The design reviews will be conducted with Raytheon management and with the procuring agency to influence the design decision-making processes at an optimal time considering dollar and schedule impact. Product Assurance personnel will contribute constructively toward design improvement in reliability, maintainability, and maintenance cost. Published minutes of meetings, listing recommendations and requirements for further study close the loop on the design review process.

Review of design plans, engineering drawings, and specifications is conducted to insure that the fault monitoring, ease of maintenance safety, test equipment and tool guidelines are adhered to in the hardware design and major vendor purchase specifications. The focus of this effort is to prevent maintainability design discrepancies which may lead to problems. Design tradeoffs will be evaluated on the maintainability merits. Maintainability information will be inputted to formal and informal design reviews.

16.3.3 MAINTAINABILITY ANALYSIS

This task involves allocation of quantitative M requirements to all significant functional levels of equipment and evaluation of the degree of achievement of M design requirements. Maintainability predictions and periodic updates will be performed to determine that the evolving design conforms to allocated maintainability values. This was accomplished by compiling all the basic data required in making a prediction for each DGM unit. The basic data include task times for fault location, fault isolation, LRU access and removal, replacement and checkout. Also included are effects of tools, manpower and failure rates for weighting repair times in the MTTR computation. Predictions for $\overline{M}_{ct}$ and $M_{max\ ct}$ were also computed. Prediction procedure III of MIL-HDBK-472 was applied. Preventive maintenance (PM) procedures were defined and evaluated against PM requirements. These data were submitted as part of the Maintainability Report, CDRL item F009 through F021, less F019.

16.4 MAINTAINABILITY DEMONSTRATION

16.4.1 MAINTAINABILITY DEMONSTRATION TEST PLAN

A Maintainability Demonstration Test Plan was written in accordance with MIL-STD-471 Test Method 1, Plan B as defined per paragraph 4.2.9.1 of specification TT-B1-2202-0013 and submitted as CDRL F024.

16.4.2 MAINTAINABILITY DEMONSTRATION TEST.

Upon approval of the Maintainability Demonstration Test Plan, the test was conducted in accordance with MIL-STD-471 paragraph 4 and with the approved plan at the Equipment Division Laboratories.

16.4.3 MAINTAINABILITY DEMONSTRATION TEST REPORT

At the completion of the Maintainability Demonstration Test, a final report was written and submitted as CDRL F005.

SECTION 17

NUCLEAR DESIGN

This information is contained in the Technical Report Final Type-Nuclear CDRL Seq. No. G001, dated 13 February 1979. The Technical Report is classified.

SECTION 18
EMI DESIGN

18.1 SHIELDED ENCLOSURE

Each unit enclosure is designed to provide 80 dB of shielding effectiveness. This provides sufficient attenuation to reduce all radiated signals to levels below the MIL-STD-461A limits. The details of these enclosures are discussed below. An exploded view of unit frames are shown in Figure 18-1. The basic frame is dip brazed construction. The front and back covers are sealed with an RF gasket (finger stock, see Figure 18-2) and bolted into place. All gasket mating surfaces are finished with irridite to prevent corrosion, but this finish has not degraded the shielding effectiveness as the gasket bits into the frame when the covers are secured.

The basic unit design has demonstrated adequate shielding capability for meeting the requirements of MIL-STD-461A on programs such as TD-1065, KG-27, and TD-660.

All lights, meters, and switches are shielded to insure rf tight enclosure integrity. All cables are either double shielded twin coax or RG-108 whose outer shield will be terminated in 360 degrees.

18.2 FILTER SELECTION

Each unit has a power line filter with a 3 dB point at 2.8 KHz, 36 dB at 10 kHz, and 80 dB from 50 kHz and beyond. Based upon past experience on TD-660 and TD-1065, these filters insure that no EMC problems will occur when tested with either 50 Hz or 400 Hz power.

18.3 RMC AND RLGM EMI DESIGN

A combination case is used to package the RMC and RLGM electronics and is designed as an integral electronics chassis and equipment case. The case is an aluminum wraparound with extruded front and rear seal interfaces mating through quick release latches to front and rear energy absorbing, vacuum foamed ABS-polycarbonate covers.

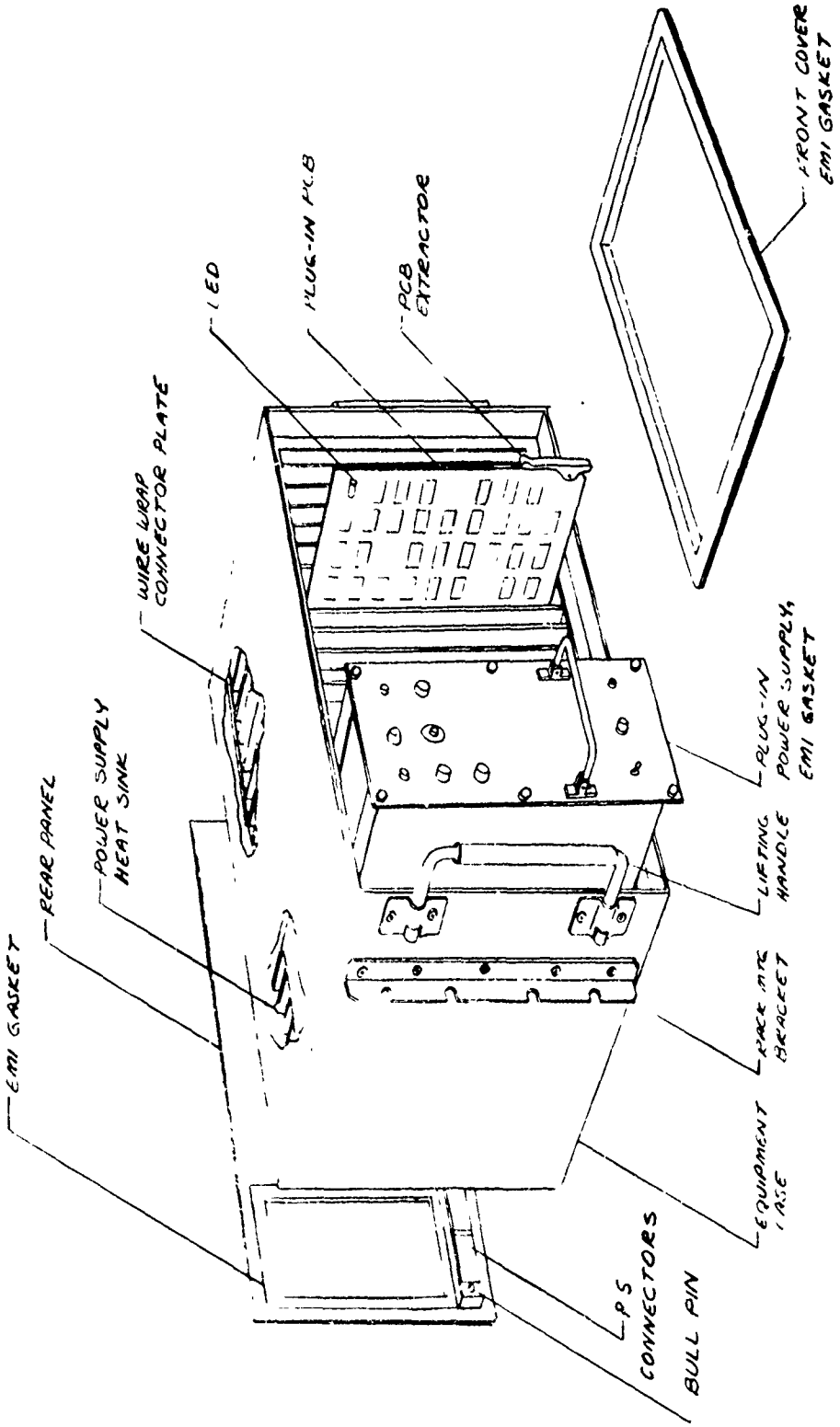


Figure 18-1. Exploded View of Unit Frames

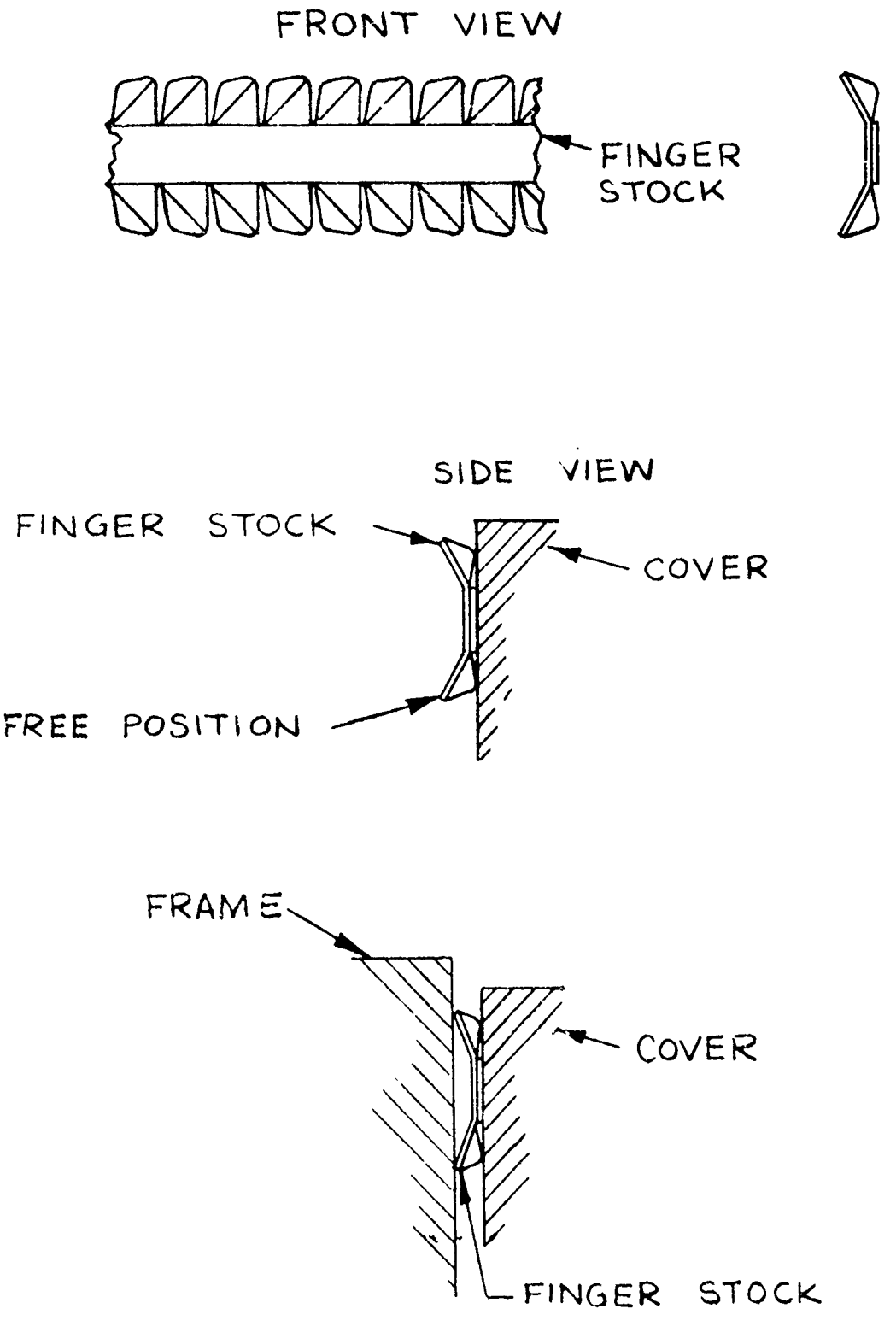


Figure 18-2. RF Gasket Configuration

Electronics are removable from the front, allowing replacement of plug-in PCBs and power supply without removing the unit from the rack. The power supply is installed from the front with the aid of guide rails and pins engaging a rear mounted connector. All operational controls are located on the front panel of the supply (see Figure 18-1). A combination EMI and environmental gasket is provided on panels and covers. The units are designed to provide 80 dB of shielding at 20 MHz. The EMI/dust seal is an EMI and environmental type gasket, Instrument Specialties Company "Sticky Fingers".

The rear mounting plate provides all I/O connectors and a cutout to allow the power supply heat sink to protrude through. MS connectors will be harnessed to the wire-wrap plate and the power supply. Access to the rear connectors is not required during unit operation.

Size of the RMC and RLGM will be 8-1/2 x 12 inches, compatible to 19-inch rack mount width.

The power line filters have the following attenuation characteristics:

Frequency	Insertion Loss
2.8 kHz	3 dB
10 kHz	36 dB
50 kHz	80 dB

The EMI design of the RMC and RLGM is similar to that of the switchboard SB-3614-TT which successfully met the requirements of MIL-STD-461A.

18.4 CABLE SYSTEM EMI

Ninety percent of all the energy in the 19 Mb/s high speed restorer and 2.304 Mb/s low speed restorer signals are contained in the first ten (10) harmonics. Therefore, in order to reproduce these signals, the first ten harmonics must be passed, i.e., for the high speed frequencies up to 200 Mb/s and 23 MHz for the low speed. For this reason, Raytheon's design used output filters which have a 3 dB point at 200 MHz for the high speed restorer and 30 MHz for the low speed restorer.

The Fourier spectrum of the waveshape associated with the high and low speed restorers is shown in Figure 18-3. The expected emission levels, with the filter insertion loss characteristics included, are compared to the MIL-STD-461A, Notice 4, limit as shown in Figures 18-4 and 18-5. The shaded area is the expected shielding effectiveness of the cable shield. The space loss is subtracted from this level, then the field intensity at one meter is defined. The space loss has been determined through past test experience.

Past experience (TD-206) has demonstrated that the GFE cables associated with the pulse restorers, CX-11230, do not have sufficient shielding to meet the requirements of MIL-STD-461A, Notice 4,

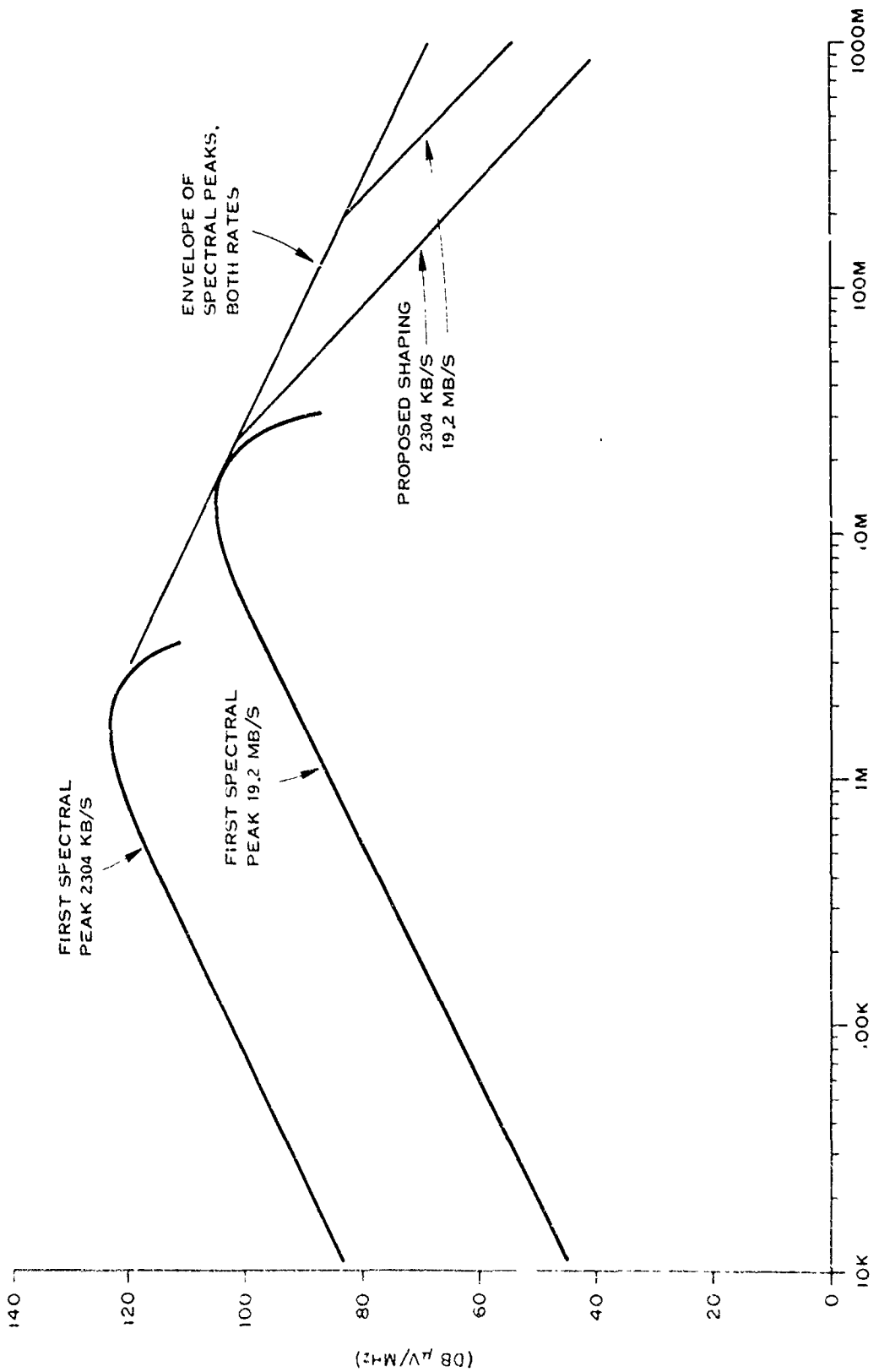


Figure 18-3. Spectral Density of Diphase Signals

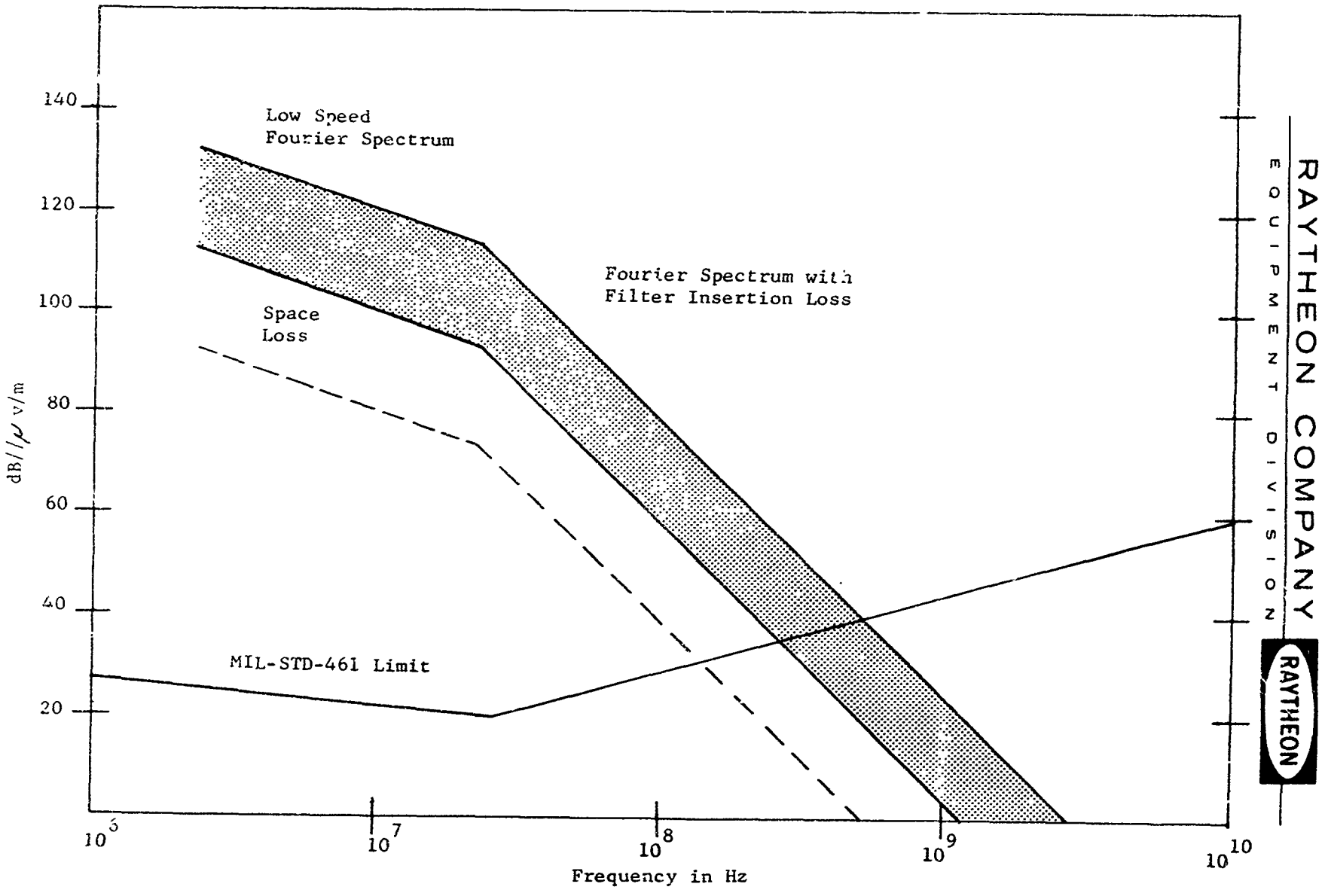


Figure 18-4. Low Speed Fourier Spectrum

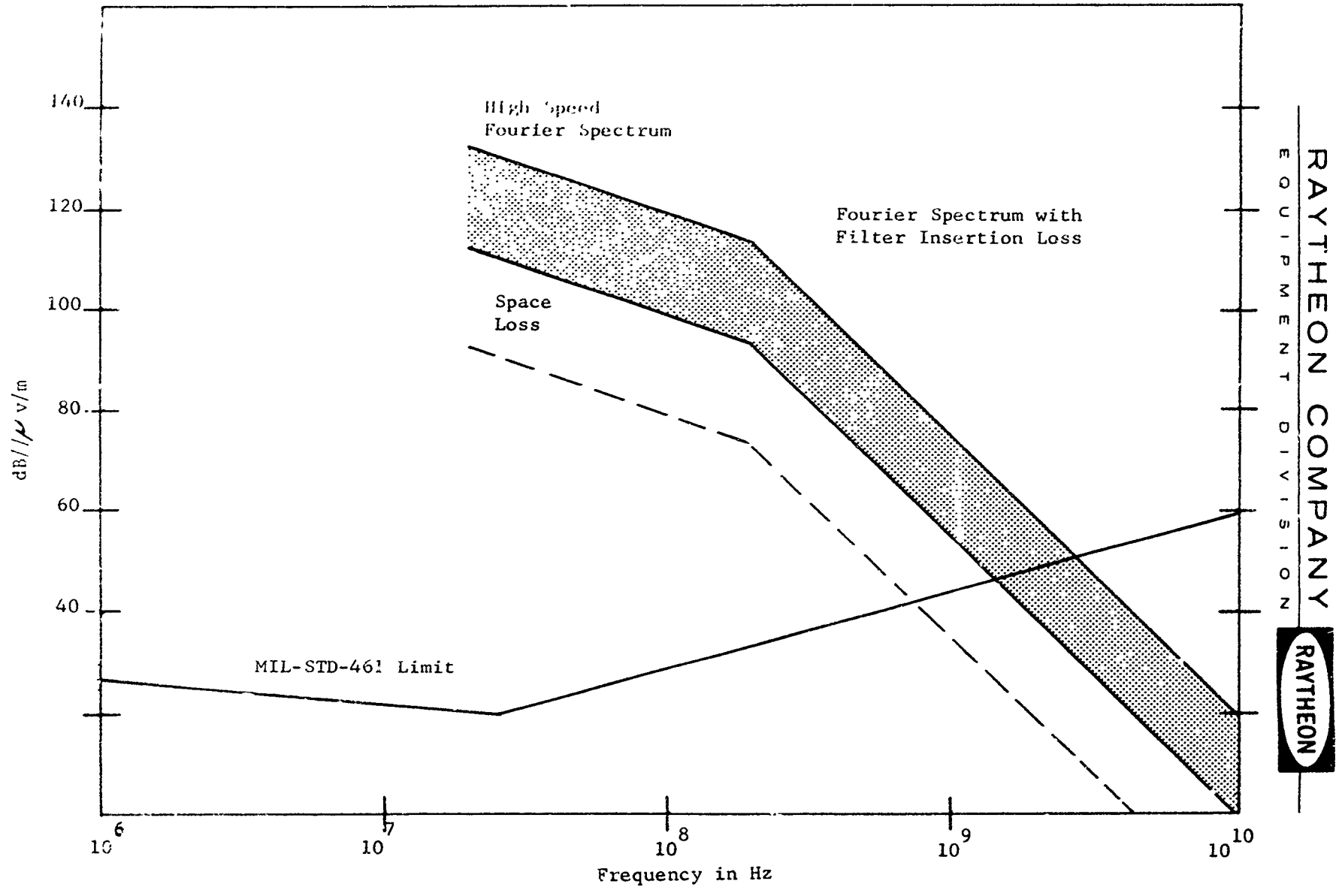


Figure 18-5. High Speed Fourier Spectrum

SECTION 19

BITE CARD

The Bite card is used by each of the DGM units to locate faults internal to the unit, to detect the loss of signal from the CX-11230 cable and to provide the appropriate alarm activating signals. Internal faults are isolated to the card or replaceable module level. The card functions are adapted for each of the five units by addressing a stored program. All the programs are stored in one onboard 512 x 8 bit PROM. The appropriate unit program is addressed by hard wiring a three bit code on the Bite connector of the unit.

The program for each unit is 64 words long. This is enough to accommodate the requirements of the most complex unit, the MGM, which at present requires at least 48 words, for the 24 cards to be monitored for faults. This excludes the Bite card which has its own internal fault monitoring circuit.

The Bite card enables the following indicators in various combinations depending on the type of fault.

a. Summary fault lamp (unit front panel)

b. Individual card LED

c. Loss of unit input LED on the Bite card

d. Relay contacts S, SA and LS which are made available external to the unit through a connector.

A block diagram of the Bite card is shown in Figure 19-1. Signals to be processed are carried on an eight line buss. An address line is provided to select the card to be tested. A card under test can route both fault monitoring points and unit input signals to the Bite card. A card fault is stored in a latch if an input signal is missing or there is a loss of signal at the fault monitoring point. When a fault is detected the summary fault lamp is enabled and the appropriate relay contacts are activated after a one second delay. The LED enable line is activated for the card with the fault, and if the fault is due to a missing input, an LED on the Bite card is also activated. The faults are priority encoded on the

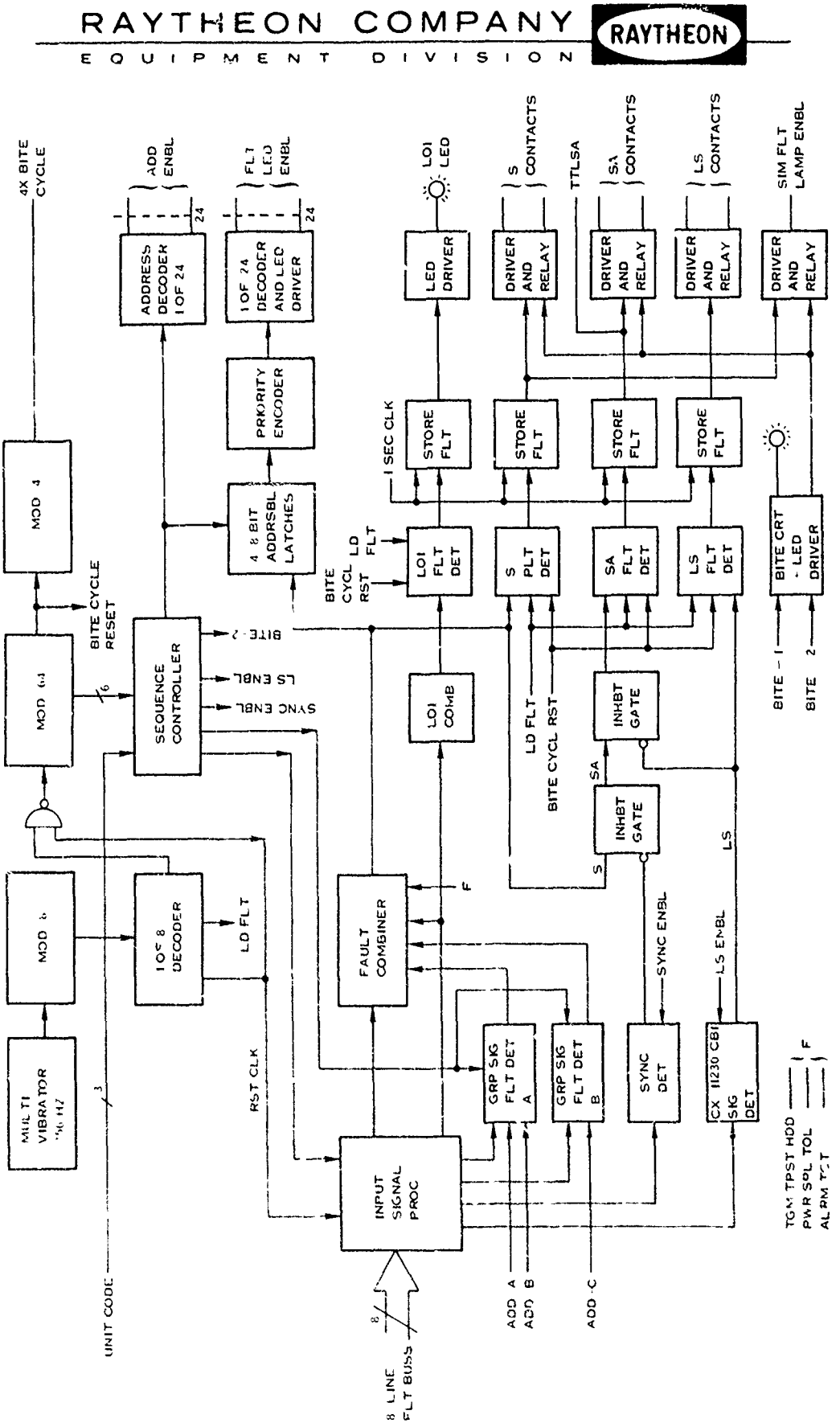


Figure 19-1. Bite Circuit Block Diagram

basis of an address assigned to the card. Address 1 has the highest priority with the following addresses having successively lower priority down to Address 24.

Timing for the Bite circuit is independent of the unit timing. A 256 Hz clock is generated using a multivibrator. The 256 Hz is counted down in a mod-8 counter. The output of the mod-8 counter is decoded. Two outputs of the decoder are combined to form a 64 Hz clock. The 64 Hz clock is applied to the mod-64 counter which addresses the PROM. The PROM is addressed twice at the start of the dwell time of each card under test. This is because it takes two words out of the PROM to set up the processing conditions for each card. The first word out of PROM is loaded into an eight bit latch. This word enables the address lines. The second word out of the PROM directly enables the signal input processing circuits. The mod-64 counter counts down the 64 Hz to 1 Hz. The 1 Hz clock is used to implement a one second timer. The dwell time at each card is 31.25 milliseconds and the Bite cycle time is 1 second. The 1 second clock is further counted down to produce a pulse which repeats at a 4 second rate.

19.1 INPUT SIGNAL PROCESSING

There are four signal processing options which are made up of combinations of activity detectors and direct inputs. The activity detectors can monitor activity of signals ranging from 18 MHz to 100 Hz. On a direct input a "1" on the buss is "no fault" and a "0" is a "fault". Direct inputs on buss inputs will latch to the fault condition if the signal goes to a "0" during the dwell time. These inputs can be used to detect the out-of-lock condition of a phase-locked-loop.

The desired signal processing combinations are obtained by programming the detectors of lines 5, 6, 7, and 8 to accept either active signals or direct inputs. Buss lines one through four are always connected to activity detectors. These detectors can be inhibited by programming the BB ENBL line out of the PROM to a "0" if a four bit buss line is desired. The PROM bits which select the combinations are IP1 and IP2.

With the combinations available the number of active buss lines can be programmed from one to eight. For example, for a one line buss, BB INHBT is set to "0" and IP1 and IP2 are set to 01 respectively, thereby making BB5 the only active input. BB6, BB7 and BB8 operate as if dc inputs are present.

19.2 UNIT INPUT SIGNALS

Unit input signals are applied singularly or in pairs to detectors five and six and only in pairs to seven and eight. The signal from the CX-11230 cable is routed to the Bite card on line seven. Buss input seven has an additional detector enabled by the LSENBL from the PROM.

A loss of input is treated like any other fault except that the LOI LED on Bite card is also enabled. Loss of cable signal enables the LS alarm and inhibits the SA alarm. On cards which do not have unit inputs, detectors five through eight can be used to monitor circuit faults.

19.3 BOARD IDENTIFICATION

Cards within a unit are identified as either common or group gards in order to program the BRD ID bit. When a group card is removed from the unit or when it is idle the Bite should not go into alarm. To make this happen a "0" must be on buss line eight and the BRD ID but must be a "1". The BRD ID bit for a common card is a "0". When it is removed from the unit the Bite will alarm.

19.4 SPECIAL SIGNALS

Units which have framing circuits as in the MGM and TGM should apply the out of sync indicator to line six. The sync detector output is applied to a storage register which is enabled by SYNC ENBL from the PROM. If an out of sync is detected the S faults to the SA alarm are inhibited.

There are signals in the MGM and TGM units which are detected on the group card but must signal a failure on a common card if the signal is missing and the group is in use. These signals are applied to detectors one and two. Two separate storage registers on the outputs of the detectors are activated by programming the GRP SIG ENBL to a one. The status of the signals are stored as the BITE sequences through the group cards. After the last group card is checked, an address line is enabled and the contents of the group signal status registers are transferred to the register which stores the common card fault.

The common card address is applied to the group signal status registers by wiring an ADD line to ADD-A, ADD-B and ADD-C. ADD-A and ADD-B inputs are OR'd. This makes it possible to check the group status register twice within the Bite sequence and have the contents transferred to ADD-A and then to ADD-B.



The following separate inputs are provided. In each case a "1" is "no fault" and a "0" is a "fault".

a. TGM TEMPEST Module Fault (TGM TPST MOD)

b. Power Supply Out of Tolerance (PWR SPL TOL)

c. Alarm Test (ALRM TST)

The ALRM TEST enables the S, SA and LS alarms.

APPENDIX A

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APPENDIX A

IC CROSS INDEX

Specification Number	Description	Manufacturer's Part Number
SM-A-876190	Quad 2 Input NOR	54LS02
SM-A-876191	Triple 3 Input NOR	54LS27
SM-A-876192	Triple 3 Input AND	54LS11
SM-A-876193	Quad 2 Input Excl OR	54LS86
SM-A-876194	2 Wide 2 Input AND/OR Invert	54LS51
SM-A-876195	Quad 2 Input NAND	54LS37
SM-A-876196	Dual 4 Input Positive NAND Buffer	54S40
SM-A-876197	Quad 2 Input OR	5428
SM-A-876198	Dual D Flip-Flop	54LS74
SM-A-876199	6 Bit Register Common Clear	54LS174
SM-A-876200	Quad D Flip-Flop	54LS175
SM-A-876201	Dual J-K Flip-Flop	54LS112
SM-A-876203	3 to 8 Line Decoder	54LS138
SM-A-876204	8 Input Multiplexer	54LS251
SM-A-876205	8 Bit Data Selector	54LS151
SM-A-876206	8 Input Multiplexer	54S151
SM-A-876207	Dual 4 Input Multiplexer	54LS153
SM-A-876209	Quad 2 Input Data Selector/Mux	54LS158
SM-A-876210	8 Input Multiplexer	54S251
SM-A-876211	Quad 2 Input Data Selector/Mux	54S158
SM-A-876212	4 Bit Shift Register	54LS194
SM-A-876213	4 Bit Shift Register	54S195

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Specification Number	Description	Manufacturer's Part Number
SM-A-876214	4 Bit Shift Register	54LS195
SM-A-876215	8 Bit Parallel Out Shift Register	54LS164
SM-A-876219	Quad Set-Reset Latch	54LS279
SM-A-876220	4 Bit Comparator	54LS85
SM-A-876222	4 Bit Sync Up/Down Counter	54LS191
SM-A-876223	Sync Binary Counter	54LS163
SM-A-876226	4 Bit Counter	54LS293
SM-A-876227	16 Bit Shift Register	54LS170
SM-A-876228	Line Driver	55109
SM-A-876231	256 X 4 RAM	93L422DM
SM-A-876232	1024 X 1 RAM	93L425
SM-A-876233	512 X 8 Bit Bipolar Prom	5341-1
SM-A-876234	16 X 4 FIFO	9403
SM-A-876236	Linear Differential Video Amp	733
SM-A-876237	4 Bit Bipolar Microprocessor	AMD2901
SM-A-876238	Bipolar Microprocessor Sequencer	AMD2909
SM-A-876273	Priority Encoder	9318
SM-A-876282	Dual Comparator	52514
SM-A-876285	Quad 2 Input OR	54LS32
SM-A-876286	Sync 4 Bit Up/Down Counter	54LS193
SM-A-876287	Quad 2 Input AND	5408
SM-A-876288	Dual Voltage Controlled Multivibrator	MC4324
SM-A-876289	Digital to Analog Converter	MC1508
SM-A-876290	Analog to Digital Control Circuit	MS1507

APPENDIX A
(Continued)

Specification Number	Description	Manufacturer's Part Number
SM-A-876295	8 Bit Priority Encoder	4532
SM-A-876300	Dual 4 to 1 Line Multiplexer	54S153
SM-A-876301	Quad 2 Input AND	54LS08
SM-A-876365	4 Bit Sync Binary Counter	54LS161
SM-A-876389	8 Bit Multiple Port Register	9338
SM-A-876390	3 to 8 Line Decoder	54S138
SM-A-876398	Sync 4 Bit Binary Counter	93S16
SM-A-876399	4 Bit Binary Full Adder	54LS283
SM-A-884399	Quad 2 Input NAND	54500
SM-A-884402	Hex 1 Input Inverter	54S04
SM-A-884494	Quad 2 Input NOR	54502
SM-A-884405	Dual D Type Flip-Flop	54574
SM-A-884407	Quad D Type Flip-Flop	54S175
SM-A-884422	Triple 3 Input Positive AND Gate	54S11
SM-A-876843	Dual J-K Flip-Flop	54S112
SM-A-876870	Voltage Comparator	AM1500
SM-A-876873	CMOS J-K Type Flip-Flop	4027
SM-A-876874	CMOS D Type Flip-Flop	4013
SM-A-876876	CMOS Dual 4 Bit Up Counter	4520
SM-A-876877	CMOS Up/Down Counter	4029
SM-A-876878	CMOS Hex Buffer	4050
SM-A-876878	CMOS Quad 2 Input OR	4071
SM-A-876880	CMOS 2 Input NAND	4011
SM-A-876881	CMOS BCD to Decimal Decoder	4028

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Specification Number	Description	Manufacturer's Part Number
SM-A-876882	CMOS Quad 2 Input AND	4081
SM-A-876885	CMOS Triple 3 Input AND	4073
SM-A-876887	CMOS Dual 4 Input NAND	4012
SM-A-876889	CMOS Quad AND/OR Select	4019
SM-A-876890	CMOS Triple 3 Input NAND	4023
SM-A-876891	CMOS 12 Stage Ripple Carry Binary Counter Divider	4040
SM-A-876897	CMOS Dual 4 Input OR	4027
SM-A-876898	CMOS, 8 Bit Addressable Latch	4724
SM-A-876899	CMOS Quad Exclusive OR	4070
SM-A-876900	CMOS Hex D Type Flip-Flop	40174
SM-A-876901	CMOS 8 Channel Data Selector	4512
SM-A-876905	Dual J-K Flip-Flop	54LS112
SM-A-876906	Op Amp	LM118
SM-A-876907	CMOS, Binary Counter	40161
SM-A-876908	CMOS Hex Inverter, Buffer	4049
SM-A-876909	CMOS Hex Inverter	4069
SM-A-876921	CMOS Dual 2 Wide, 2 Input AND/OR Invert Gate	4085
SM-A-876923	CMOS 3 State Hex Buffer	40097
SM-A-876924	CMOS Inverting Buffer	40098
SM-A-838046	Hex Inverter	54LS04
SM-A-838048	Dual D Type Flip-Flop	54LS74
SM-A-838055	8 Input NAND Gate	54LS10
SM-A-838061	Quad D Type Flip-Flop	54LS175

APPENDIX A
(Continued)

Specification Number	Description	Manufacturer's Part Number
SM-A-838074	Quad 2 to 1 Data Selector	54LS157
SM-A-838084	Sync Up/Down Counter	54LS191
SM-A-838086	Dual Op Amp	747
SM-A-838096	Quad Line Driver	2616
SM-A-838128	Hex Inverter	54S04
SM-A-838129	Quad 2 Input NAND	54S00
SM-A-838134	Quad D Type Flip-Flop	54S74
SM-A-838186	Analog Mux/Demux	4053
SM-A-838261	Operational Amplifier	LH0002
SM-A-838905	Dual J-K Flip-Flop	54LS112
SM-D-780174	Phase Locked Loop	4046
M38510/30001 BCB	Quad 2 Input NAND	54LS00
M38510/30003 BCB	Hex Inverter	54LS04
M38510/30005 BCB	Triple 3 Input NAND	54LS10
M38510/30007 BCB	Dual 4 Input NAND	54LS20
M38510/30009 BCB	8 Input NAND	54LS30
M38510/00302 BCB	Quad 2 Input NAND	5437
M38510/10102 BCB	Dual Operational Amplifier	747
M38510/10401 BCB	Line Receiver	55109
M38510/30203 BCB	Quad 2 Input NAND	54LS38