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THE IMPACT OF VHSIC ON AIR FORCE SIGNAL PROCESSING

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THE IMPACT OF VHSIC ON AIR FORCE SIGNAL PROCESSING

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ABSTRACT

The functional characteristics of VHSIC-I and VHSIC-II as they affect Air Force signal processing systems are discussed. The Air Force has identified a number of system candidates for VHSIC application. These fall into three categories: "nice-to-have," "need-to-have," and "needed-to-have earlier." Examples of the impact of a VHSIC-like capability on each of the three categories are discussed, and vice versa, with emphasis on the last of the three categories because it is the one that imposes the most stringent demands on future VHSIC chip designs and architectures. However, the "nice to have" applications are not a luxury since they serve two very useful purposes: (1) to indicate that the VHSIC design approaches are valid and prolific in their applications and (2) to provide early pay-off for the VHSIC effort plus applicational feedback to the designers. It is shown here that VHSIC-I can satisfy today's requirements, and,as presently forecast, VHSIC-II can meet 1980 requirements, and, only if extreme care is taken in architecture and chip design, can 1990 requirements be met with 1990 VHSIC's. The impacts of software/hardware/architectural tradeoffs, VHSIC system reliability, and future signal-processing systems design and commonality are discussed.

INTRODUCTION

The objective of the Department of Defense (DoD)-initiated Very High Speed Integrated Circuits (VHSIC) program is to support the requirements of military systems in the mid-eighties and beyond*. Major emphasis will be on future military functions and military environments for which there are no comparable commercial or industrial markets; especially where high-speed/high-throughput signal processing is required. To meet these objectives, much smaller size and power consumption combined with increased reliability and real-time system output are required, requiring, in turn, both higher chip complexities and higher clock rates. In addition, tougher military environments will have to be tolerated, for longer periods of time, imposing additional fault-tolerance constraints on chip and system design and suggesting on-chip redundancy and built-in test. Furthermore, the desire to take advantage of mass production to simplify supply and logistics support and reduce unit costs imposes commonality requirements on the chips used and militates against chip customization. This, as will be shown, imposes severe requirements on chip design and architecture and will accelerate the trend towards software customization versus hardware.

Two generations of VHSIC chips are to be developed:

VHSIC-I - 1.25 micrometer feature size capable of 100,000 equivalent gates per chip, system implementation scheduled for mid 80's.

VHSIC-II - 0.5 - 0.8 micrometer feature size capable of 300,000 equivalent gates per chip, system implementation scheduled for late 80's or early 90's.

The speed density product figure-of-merit goal will be greater than 10^7 gate-MHz.

The Air Force proposed an initial set of potential candidates for VHSIC implementation as have the Army and Navy.

*The program is motivated by the judgment that industry is not presently oriented towards DoD's current and future integrated circuit (IC) needs in terms of availability, price, function, and specifications.

These candidates arose out of a survey of present and future Air Force needs. They represent a range of requirements from "nice-to-have" (systems which have been, or could be, built using conventional available technology, but, because of numbers, cost, space, reliability, power, or anticipated future growth would benefit from VHSIC), through "need-to-have" (where a future system requirement cannot be met without timely VHSIC, or equivalent, availability), to "needed-to-have earlier" applications (those where today's system requirements cannot be met without VHSIC, or equivalent, circuitry.) By the time the VHSIC's needed today (e.g. VHSIC-I) are available, it is highly probable that the last type of system's requirements will have outgrown them. Thus, as will be discussed later, it is critical that VHSIC (or equivalent) chip design and architecture allow for projected or unanticipated functional and system growth.

In each case, the candidates were chosen based on several important criteria: (1) the specific application should be prolific, i.e. lead to a number of derivative uses, (2) projected chip commonality would be a major objective, (3) the applications chosen could validate design approaches taken and feed back critical information to the VHSIC designers, and (4) the candidate systems would benefit tangibly from VHSIC and, in the more-needed cases, be critically-dependent on VHSIC's (or equivalent) to meet system requirements.

Using these criteria, the "nice-to-have" candidates are more than icing on the cake. They will add to production volume. The impact of VHSIC on these systems and their derivatives can be readily quantified, primarily in terms of improved performance, system life, growth and life-cycle cost. Thus, they will provide early demonstrations of utility (i.e. pay-off) as initial justification for the VHSIC effort, as well as feedback to the VHSIC design and architecture efforts. Conversely, the impact of VHSIC on the other two categories of systems cannot be quantified; it is an all-or-nothing issue. Without VHSIC (or equivalent), the operational requirements for these systems cannot be met and the Air Force will be unable to perform those critical signal processing functions represented by these systems.

"Nice-to-Have" VHSIC Applications

Three candidates are proposed here:

(1) Shrinking an Existing General Purpose Computer,

(2) Advanced Power Management Systems,

(3) Radar Signal Processor for the Airborne Warning and Control System (AWACS).

The first two are typical "nice-to-have" applications. They involve shrinking existing medium-to-large scale data processors, with all the well-known attendant life-cycle cost and performance advantages. However, the AWACS application is one in which VHSIC will help overcome a cost barrier; cost being the primary deterrent to the upgrading of the radar system's performance. The impact here is an enhanced radar capability, primarily in terms of added ECCM capability and types, classes and numbers of targets that can be tracked. These verge on "need-to-have" requirements. The AWACS application could represent the prototype of a family of advanced airborne sensor processors and as such could provide valuable design feedback and an early VHSIC demonstration of utility. The estimated shrink potential of VHSIC for the AWACS radar signal processor is shown in Table 1.

TABLE 1

AWACS "SHRINK" POTENTIAL

RADAR SIGNAL PROCESSOR

	CURRENT TECHNOLOGY	VHSIC
NUMBER IC'S	7,500	6 to 10
GATE COMPLEXITY	150,000	150,000
POWER (W)	5,000	4 to 50
SIZE (Ft^3)	30	0.1
WEIGHT (LBS)	500	< 10
MTBF (HRS)	100	YEARS
COST ($)	$1 to 2 million	$10 to 100 thousand

"Need-To-Have" VHSIC Applications

Four candidates in this category were identified:

(1) Advanced Medium Range Air-To-Air Missile (AMRAAM),

(2) Advanced Cruise Missile,

(3) JTIDS Communications and Signal Processor,

(4) The Advanced On-Board Signal Processor (AOSP) for advanced space-based radar and electro-optical sensor systems.

All of these fall into the class where size and cost are critical and in the case of the first two, the impact of VHSIC is so critical as to determine whether the system is feasible or not.

In the case of the JTIDS Class 2 fighter terminals, processing power and speed, size, cost, weight, and power are important factors but not so critical as to make or break the system. The impact of VHSIC would be primarily on the Class 3 terminal, the so-called "man pack" terminal, where, even with reduced capability, size and power constraints are formidable. This is illustrated in Table 2, where the estimated VHSIC shrink potential has been computed for the signal and communication processor portions of the JTIDS Class 1 terminal, a terminal of greater capability than even the Class 2 terminal. The resulting VHSIC processor is small enough to meet the requirements of the Class 3 terminal; yet it possesses the processing power of the Class 1 terminal. Thus, in addition to allowing the Class 3 terminal specifications to be more than met, VHSIC could lead to a 'classless' JTIDS terminal where a common signal processor could meet the manpack, fighter, and large terminal requirements with minimal size and power.

TABLE 2

JTIDS "SHRINK" POTENTIAL

SIGNAL & COMMUNICATION PROCESSOR

	CURRENT TECHNOLOGY	VHSIC
NUMBER IC'S	3,500	6 to 20
GATE COMPLEXITY	350,000	350,000
POWER (W)	1,000	8 to 60
SIZE (Ft^3)	1.5	0.1
WEIGHT (LBS)	81	<10
MTBF (HRS)	350	YEARS
COST* ($)	$175,000	<$10,000

*COST DOES NOT INCLUDE AIRCRAFT INSTALLATION

The power of a practical AOSP will be critically dependent on weight, size, power requirements, processing power and speed. Revolutionary system architectural concepts are needed for this application. The degree of success of this project will be closely linked to the success of the VHSIC (or equivalent) program. In turn, this will determine whether or not the space sensors to be serviced can indeed meet the target-detection, flexibility, accuracy, speed, data-handling, and failure characteristics required to make them feasible.

"Needed-to-Have Earlier" VHSIC Applications

The example here is the Programmable Signal Processor for Advanced Airborne All-Weather Tactical Strike. Before an assessment of what VHSIC will and will not do to impact such signal processors and vice versa, a baseline must be established. Current state-of-the-art capabilities versus present and future requirements will be assessed and then contrasted with the VHSIC program objectives.

As shown in Figure 1, the airborne radar of today is comprised essentially of an antenna, transmitter, receiver and a rather large "number cruncher" to give it versatility and flexibility.

TYPICAL RADAR SYSTEM COSTS DISTRIBUTION

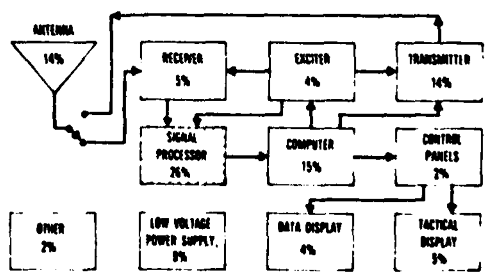

Figure 1

Note that 40% of the total system cost is in digital processors, of which 25% is in the signal processor. (As electronically-scanned antennas are implemented, these percentages will increase even more.)

Parameters of typical signal processing hardware installed in aircraft now are given in Table 3. Unfortunately, the machine represented here is not fast enough to accomplish the multimode tactical radar mission requirements of today listed below:

(1) Air/Air Search Track

(2) Identification Friend or Foe (IFF)

(3) Air/Ground Synthetic Aperture Radar (SAR)/ Ground Moving Target Detection and Track (GMTI)

(4) Terrain Following/Terrain Avoidance (TF/TA)

TABLE 3

TYPICAL FLYING PROCESSOR

ARCHITECTURE:	PIPELINE/PARALLEL PIPES 1.2 MBIT MEMORY
ARITHMETIC:	COMPLEX (12 BITS + j12 BITS)
SPEED:	70 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	4000
POWER:	1 KW
SIZE:	~ 1 CUBIC FT

The characteristics of a machine to meet these four major tactical modes are shown in Table 4 (assuming the same architecture as Table 3). The question logically is how close are we to meeting these objectives with current state-of-the-art technology.

TABLE 4

REQUIRED MACHINE FOR FOUR TACTICAL MODES

ARCHITECTURE:	PIPELINE/PARALLEL PIPES 12.5 MBIT MEMORY
ARITHMETIC:	COMPLEX (12 BITS + j12 BITS)
SPEED:	200 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	1000
POWER:	1 KW
SIZE:	~ 1 CUBIC FT

The Air Force has developed advanced development R&D class machines utilizing LSI ECL with the characteristics of Table 5.

As is most readily observed the current machines fall short of requirements in all respects except size. The 3 KW power dissipation is too high for use in a tactical fighter.

Another interesting parameter of this R&D machine is that it requires 14-layer printed circuit boards with terminated transmission line signal paths due to the use of ECL technology. Needless to say, this is not an inexpensive machine.

TABLE 5

ADVANCED DEVELOPMENT R&D MACHINE PARAMETERS

ARCHITECTURE:	PIPELINE/PARALLEL PIPES 12.5 MBIT MEMORY
ARITHMETIC:	COMPLEX (12 BITS + j12 BITS)
SPEED:	180 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	2500
POWER:	~ 3 KW
SIZE:	1 CUBIC FT

Now that we have determined that current technology has not provided a machine that can meet today's requirements, let us explore what can be reasonably expected of VHSIC-I. It is not unreasonable to expect by 1983, machines of the performance of Table 6, assuming that the architecture is the same as before. It is obvious that this machine will meet the requirements for the four specified radar modes of today's tactical fighter, Table 4. Thus by 1983 we can reasonably expect processors to be available that meet today's requirements for the case of the multimode radar of the tactical fighter.

TABLE 6

VHSIC I PROCESSOR

ARCHITECTURE:	PIPELINE/PARALLEL PIPES 12.5 MBIT MEMORY
ARITHMETIC:	COMPLEX (12 BITS + j12 BITS)
SPEED:	200 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	500
POWER:	1 KW
SIZE:	1 CUBIC FT

Now let us explore the 1980 requirements for this same fighter. One other mode is added to the ones stated before: a high resolution wide-swath reconnaissance mode. The machine required to do this job is specified in Table 7.

TABLE 7

TACTICAL FIGHTER WITH RECONNAISSANCE

ARCHITECTURE:	? 16 BILLION BITS MEMORY
ARITHMETIC:	FLOATING POINT
SPEED:	2000 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	1000
POWER:	1 KW
SIZE:	1 CUBIC FT

Table 8 shows what we can reasonably expect from

VHSIC II (or equvalent) using 0.5 micron technology by the late 1980's to 1990.

TABLE 8

VHSIC PHASE II MACHINE

ARCHITECTURE:	? MEMORY 16 BILLION BITS
ARITHMETIC:	FLOATING POINT
SPEED:	2000 MOPS (MULTIPLIES AND ADDS)
IC COUNT:	500
POWER:	1 KW
SIZE:	1 CUBIC FT

Thus, we deduce that by 1990 with VHSIC II (or equivalent) the Air Force can meet its 1980 requirements. In order to do better, better utilization of the VHSIC chip technology will have to be accomplished. The issue then in this class of applications is not what will the impact of VHSIC on Air Force signal processing requirements be but that, without VHSIC (or equivalent) the Air Force cannot meet its objectives. However, in order to have a chance of meeting these requirements, careful chip architectural and circuit design will have to be undertaken so that in 1990 we don't have to say that "we now have the capability to meet the Air Force's 1980 requirements," or, that "the 1990 requirements will be met with devices to be available in the year 2000."

Architecture and Chip Design

VHSIC I will provide the capability to shrink today's systems, i.e. it will meet 1979 requirements in 1983. The effectiveness of VHSIC II is going to depend upon the architectural effort, foresight, and ingenuity applied to their design. The chip technology is there, the architecture is not. So, let's not fall into the trap of meeting 1980's needs in 1990. An architectural design blockbuster is needed. Unfortunately, we need the architecture as soon as possible.

There are two schools of thought on the architectural design effort:

> One says - take a job to be done (most probably the toughest one) and evolve an architecture to do it. If possible, it should also be able to do a plethora of lesser jobs.
>
> The second says - design the most advanced but realizable architecture and show that it can do the jobs needed.

Which is better? It's hard to say. The first one is more direct but the goal may be unreachable and then what do you have? The second seems to allow for more innovation and serves a broader class of users; but it may fall short of the mark for the toughest user; it may have to evolve a next generation architecture in an attempt to meet his needs. However, there is no assurance that his needs can be solved through evolution if they weren't considered in the initial design phase.

In any case, it can be said that the chips will be composed of a replication, many times over, of a basic gate element. What should the design of this element be and how should these elements be tied together? What degree of flexibility or programmability is best? The hardware-software tradeoff and the type of software used are critical.

Impacts on Operating and Maintenance (O&M/Costs)

The very fact that VHSIC will lead to order of magnitude increases in the number of gates per chip (VHSIC-I - 100,000, VHSIC-II - 300,000) and speed density products ($>10^7$ gate - MHz) will result in a corresponding increase in system reliability and reduction in cost (if the chips used are in large volume production), unless the system complexity grows at the same rate as the technology. This tendency is touched on below.

Both of the characteristics are illustrated in Figures 2 and 3.

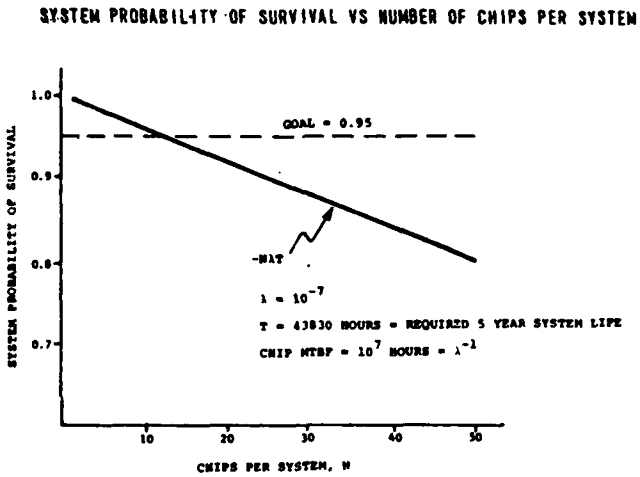

Figure 2

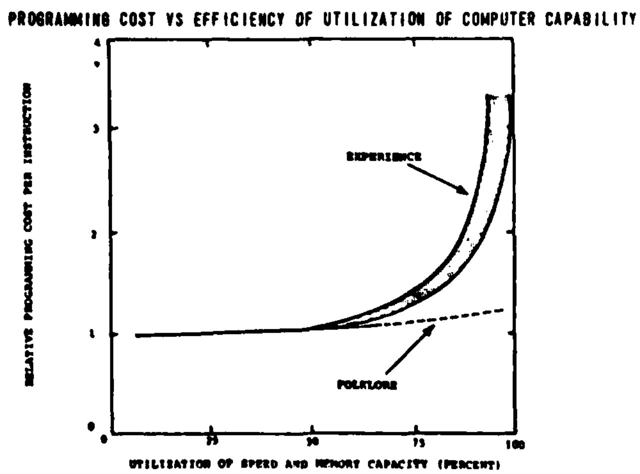

Figure 3

Figure 2* illustrates that for chips of the same MTBF (which is generally true for mature chips of the same technology operated within tolerance limits), the system reliability (in terms of probability of surviving 43830 hours or five years of operation) is inversely proportional to the number of chips in the system, N. The major failure mechanism is in the chip interconnections. Figure 3** shows that programming efficiency increases with decreasing efficiency of use of the processor and/or its memory. In other words, programmers can be more careless if they have excess speed and memory capacity available; they don't have to be as clever in their program design. This indicates that we wish to oversize our computer and memory capability.

Human behavior seems to militate against both of these factors - the human tendency is to use or fill-up whatever computer capacity is available and not allow ourselves the luxury of being hardware inefficient to obtain efficiency in programming effort. The goal of being hardware-inefficient is also in apparent conflict with the need in multimode-tactical radar signal-processing discussed earlier where the system requirements dictate that we get as much processing power out of VHSIC as possible.

Despite these factors, some authorities hope that the power of VHSIC will be so great that natural inefficiency in usage will result. A more logical approach is to aim for more efficient software design since we can assume that the uses will always eventually approach or outstrip capacity.

This is examined further in the next section.

However, if, in fact, the same signal-processing tasks are to be accomplished, the processor with the greater speed (and/or memory capacity) will provide lower cost per instruction (Figure 3) and, for two computers with the same processing power (number of gates), the one possessing the larger chips will be more reliable since fewer chips will be needed (Figure 2).

In addition, the luxury, in many applications, of being able to afford an excess of logic elements due to the potential low-cost per-gate means that liberal redundancy in component usage and throw-away maintenance can often be more readily achieved with VHSIC (or equivalent) thus reducing field maintenance cost. Also, if the chips can be designed to satisfy a large applications base, logistic and spares costs can be reduced considerably.

Architecture, Growth, Commonality, Software

While it looks as though VHSIC phase II technology will meet Air Force requirements of device density, there is a gap in the capability to utilize the device technology at the systems level. This is evident if one looks at the high speed signal processors of today. By and large these machines are of complex pipeline architecture, and are designed to execute a "butterfly" per clock cycle. Because these machines are basically synchronous in nature, it is almost impossible to program them at anything higher than an assembly language level and maintain efficiency. Moreover, while these machines are designed primarily for digital filtering, many current applications in high-speed systems require the data dependent branch instructions that the pipeline machines do not have. Ideally, what is desired are new architectures that will meet system "number crunching" requirements, are programmable in a Higher Order Language (HOL), and make optimal use of VHSIC technology. In order to achieve these goals, it is a necessity that the technologies of parallel architectures and efficient real time HOL's be pursued in order to feed VHSIC phase II.

To state the requirements simply: New computing machines must be developed whose architectures are optimized to meet the sensor processing requirements, are programmable in a real time HOL, and that take advantage of the best features of VHSIC (or equivalent).

The challenge will be to achieve the capability to utilize the power of VHSIC chips efficiently and yet have affordable software and hardware costs. This implies commonality of hardware (i.e. a basic chip architecture for many applications) and ease and low cost of programming. Also, since the VHSIC technology will be an evolving one, this should be taken into account in the design of chip architectures.

It will be necessary to undertake an intensive signal processing-driven design effort to integrate chip architecture design and software design so that the full potential of VHSIC can be realized. HOL's and standard software appropriate to signal processing are needed. Signal processing tasks are highly-structured, repeatable, and generally predictable. Software development aids and multi-level simulation tools are required to assist in system design.

Conclusions

In some cases VHSIC (or equivalent) will offer speed, software, cost, size, power, O&M, reliability, and life advantages to Air Force signal processing systems; in other cases, Air Force systems needs cannot be met without VHSIC (or equivalent technologies); and, in the most difficult applications, even VHSIC will not meet Air Force signal processing needs without major architectural and software advances. The recursive process whereby early "nice-to'have" applications provide feedback to the chip architectural design efforts and validate the results is an important factor in achieving later success. The message to be derived here is that VHSIC technology development must be coupled with a significant effort in software and architectural (hardware) design in order to:

(1) Satisfy the most demanding needs,

(2) Assure that the chip sets produced are widely applicable to achieve the cost efficiencies of large production runs and,

(3) To provide for growth and evolution to meet even more stringent future needs.

In the final analysis, the question is not what is the impact of VHSIC (or equivalent capability) on Air Force Signal Processing, but what are the consequences of not having this capability.

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