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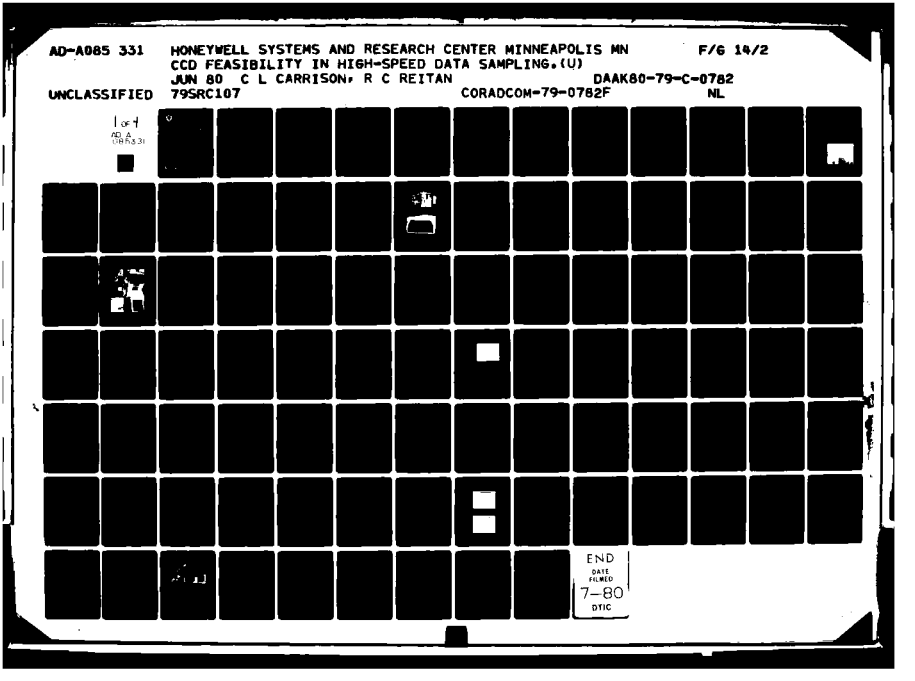

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CORADCOM-79-0782-F

CCD FEASIBILITY IN HIGH-SPEED DATA SAMPLING

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The primary objective of this program was to prove the feasibility of using CCD delay lines for high-speed data sampling at 10 MHz, with 12-bit accuracy. Such a sampler would have broad applicability in ATE systems of the future. The vehicle for this study was a CCD high-speed sampler developed on Honeywell IR&D using the 2178 CCD developed at the Honeywell Solid State Electronics Center.

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The high-speed sampler was incorporated into a data acquisition system using a SYM-1 microcomputer. This system was used to measure device parameters including noise, leakage, transfer efficiency, and linearity. These measurements have shown not only that CCDs are a viable technology for high-speed sampling but that the technology is capable of higher speed performance and is ready to be applied to today's ATE problems.

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SECTION I

INTRODUCTION AND SUMMARY

This report documents the results of CCD feasibility in a high-speed data sampling program. During this program, we not only have achieved our objective of demonstrating the feasibility of CCDs for fast sampling, but have actually used such a system to characterize the CCD device itself. We have measured CCD noise performance approaching the limit of a 12-bit A/D converter and have measured linearity better than 0.5% full scale at 10 MHz sampling rates. For both linearity and noise measurements, the limit reached was in our test equipment and not in the CCD device. We believe we are now ready to extend the speed capabilities of the system and apply it to Army ATE needs.

Our original intent in this program was to characterize the 2178 CCD to determine the feasibility of using CCDs for high-speed sampling. The 2178, which was developed by the Honeywell Solid State Electronics Center for IR imaging applications, was considered a good candidate for study, though not an optimum configuration. The 2178 was to be studied using the Honeywell CCD fast sampler developed for this purpose on a Honeywell Avionics ATE IR&D program.

Early in the fast-sampler program, it became obvious that performing the required measurements with the speed and accuracy needed could not be done with any conventional test equipment. To overcome this problem, the fast sampler was integrated into a fast-sampling system using a

SYM-1 microcomputer. This system, equipped with read-out and plotting routines, performed measurements on the CCD devices which were previously impossible.

Despite our initial suspicions to the contrary, the 2178 device has proven to be well-suited to ATE applications. The noise, linearity, leakage, and transfer efficiency performance of the device appear to be more than adequate for 12-bit performance at speeds in excess of 10 MHz. In addition, it appears that it is feasible to use this device for sampling applications at speeds in excess of 60 MHz.

The CCD fast-sampling technology is now ready to be tested against real Army ATE requirements. A system employing this technique with the proper excitation electronics and system software can replace a myriad of the individual units previously used in ATE systems.

SECTION II

CCD FAST-SAMPLER DESCRIPTION

THE 2178 CCD

The 10 megahertz, 12-bit fast-sampling system which Honeywell has developed relies on the ability of a CCD shift register to sample and store analog data. The device selected for this application was the Honeywell 2178 SSC, a photomicrograph of which is shown in Figure 1. Although not originally designed for this application, it was felt that the 2178 would be a good vehicle for feasibility demonstration, since the device could meet the speed requirement because of its buried channel construction. Our

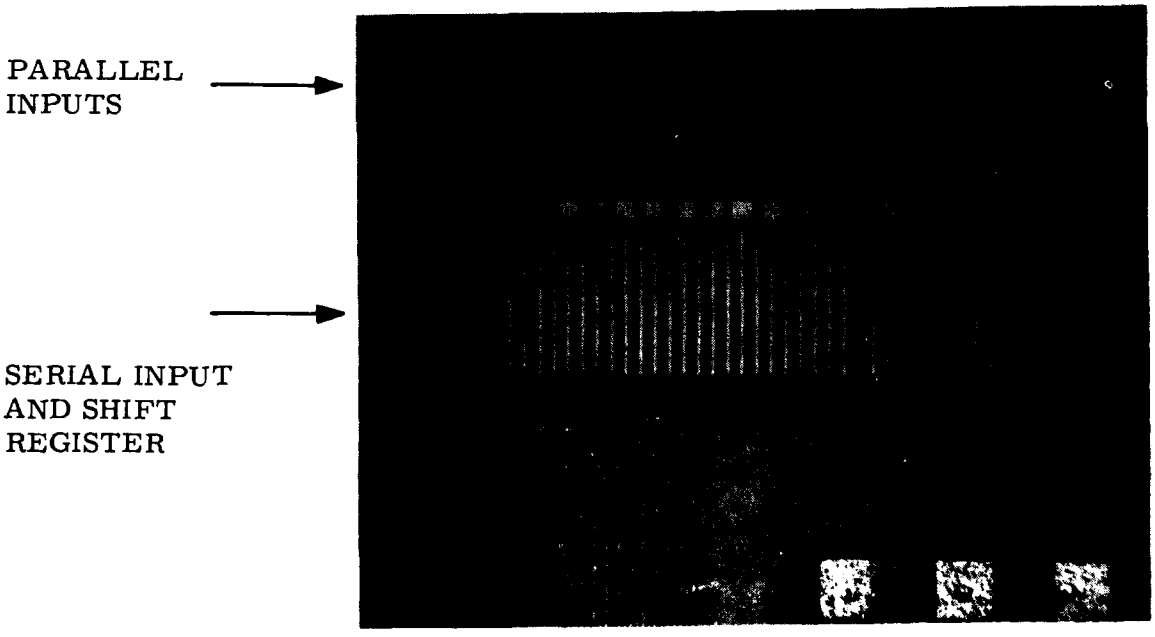


Figure 1. Photomicrograph of the 2178 128-Stage MUX (Input and first 20 stages shown)

test results have shown, however, that the 2178 is more than a demonstration vehicle and can be used in actual fast sampling-hardware.

The 2178 was originally designed as a multiplexer for IR imaging application and consisted of a number of test structures, all fabricated using the same mask set. The structure used for the fast sampler is the 128-stage SSC. This circuit was designed to be a 128-input parallel to serial multiplexer as can be seen in the schematic (Figure 2). For the fast-sampling application the 128 parallel inputs are left floating, and the ϕt transfer gate is tied to substrate potential to isolate the parallel inputs from the shift register, leaving a single 128-stage series shift register.

The serial input circuit on the 2178 consists of three gates and a diffusion which can be connected in various configurations to give a number of input

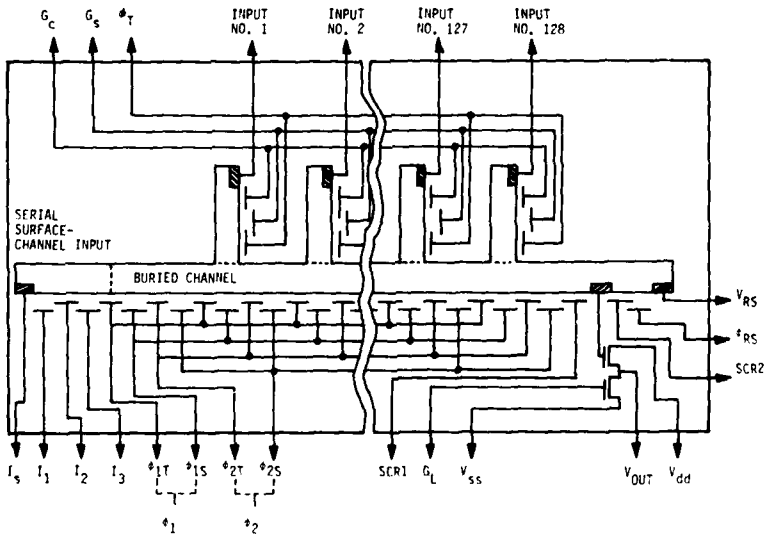


Figure 2. Schematic of Standard Source-Coupled Multiplexer

characteristics. For the fast sampler a diode cut-off input configuration is used because of its speed characteristics. As shown in Figure 3, this circuit uses the diffusion as a constant potential source of charge which fills the area under the I_1, I_2, and I_3 gates with charge when the I_1 gate is clocked on. The charge under the I_2 and I_3 gates, which is proportional to the voltage applied to them, is cut off from the input diffusion when the I_1 gate is clocked off. The falling edge of I_1 acts as the aperture, and once I_1 has turned off, the signal charge is stored under I_2 and I_3 independent of further changes in the voltage on I_3. When the ϕ_{1T} gate is clocked high, all the charge under the I_3 gate is transferred into the shift register. The charge under the I_2 gate, which is stored at a higher potential than the potential of the I_3 gate, is also transferred into the shift register. Although the circuit could be operated without the I_2 gate, the gate acts as a screen between the clock on the I_1 gate and the signal which is present on the I_3 gate.

The shift register section of the 2178 is a 4-ϕ structure. The ϕ_{1T} and ϕ_{2T} electrodes have a built-in ion-implanted potential barrier under them, which creates a potential well under the ϕ_{1S} and ϕ_{2S} electrodes; as a result, only two clock phases are required (Figure 4). The charge is transferred from the ϕ_1 electrode pair when the ϕ_2 electrode is clocked high and will remain there when the electrode is returned to its ground state because of the built-in barrier. In normal low speed operation the ϕ_{1T} and ϕ_{1S} electrodes would be connected to the same driver, as would the ϕ_{2T} ϕ_{2S} pair. In our application the ϕ_{1T} and ϕ_{2T} electrodes are excited with the same signal, but they are fed from separate drivers, because this halves the capacitive load on the drivers.

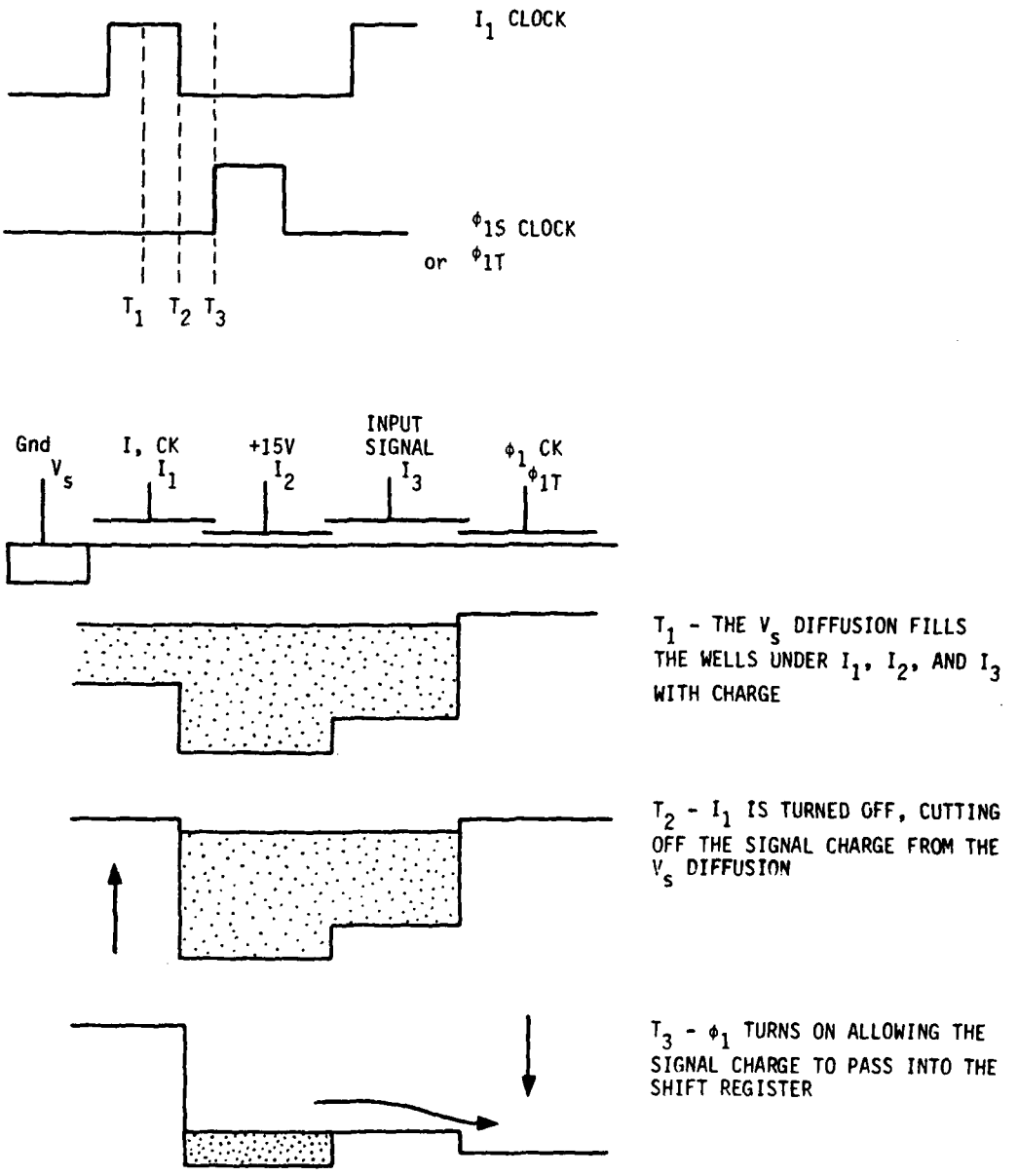


Figure 3. Input Circuit Operation

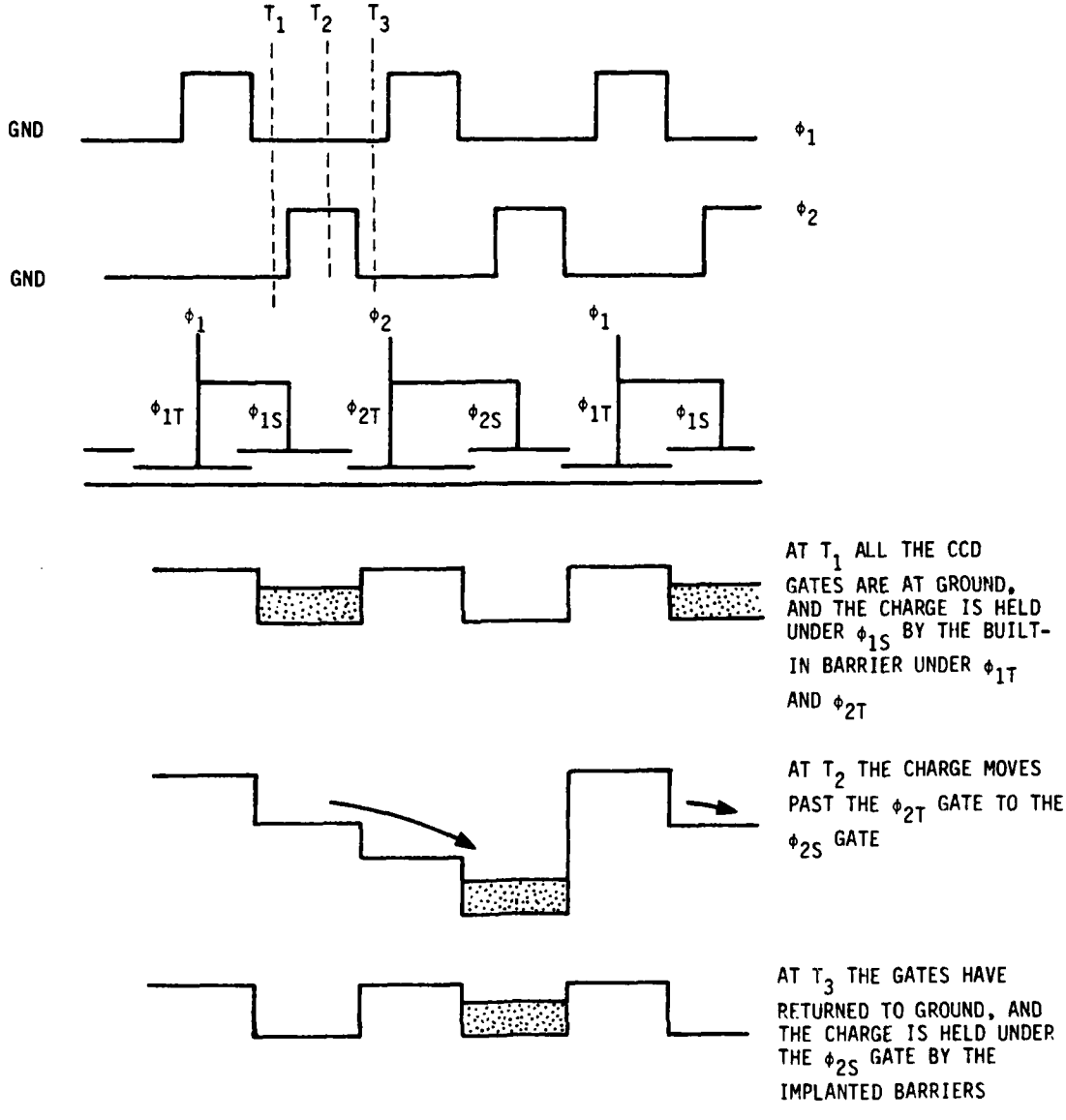


Figure 4. Shift Register Operation

The output circuit of the 2178 is a conventional floating diffusion circuit with two DC screens and a source follower. Operation of the circuit is depicted in Figure 5. The charge from the last well in the shift register is transferred over the DC screen 1 electrode onto the floating diffusion, which has been preset to a known DC voltage. The signal charge causes the node voltage to go negative by an amount proportional to the amount of charge in the well. This voltage is coupled to the output pin through the source follower which has extremely high input independence. The floating diffusion is then reset to the DC reset level when the ϕ_{RS} electrode is turned on.

THE FAST-SAMPLER CIRCUIT

To create a self-contained fast sampler, the 2178 CCD was incorporated in a single unit containing an input buffer, clock drivers, output buffer, 12-bit A/D converter, and the necessary timing and control logic. A picture of the final unit is shown in Figure 6, a block diagram in Figure 7, and the circuit schematics in Figures 8a, b, and c.

For the measurements which were made with the fast sampler, the input buffer proved to be more trouble than it was worth and was discarded early on. The problem was the oscillations created in the op amp when it was exposed to the clock waveforms radiated in the box. Better shielding and power supply filters should fix these problems, although a new design may be required for signal preconditioning in a deployable unit. For our tests a 50 ohm resistor was tied from the input gate (I_3) to ground to give the proper termination for input signals, and analog data was applied directly to the CCD.

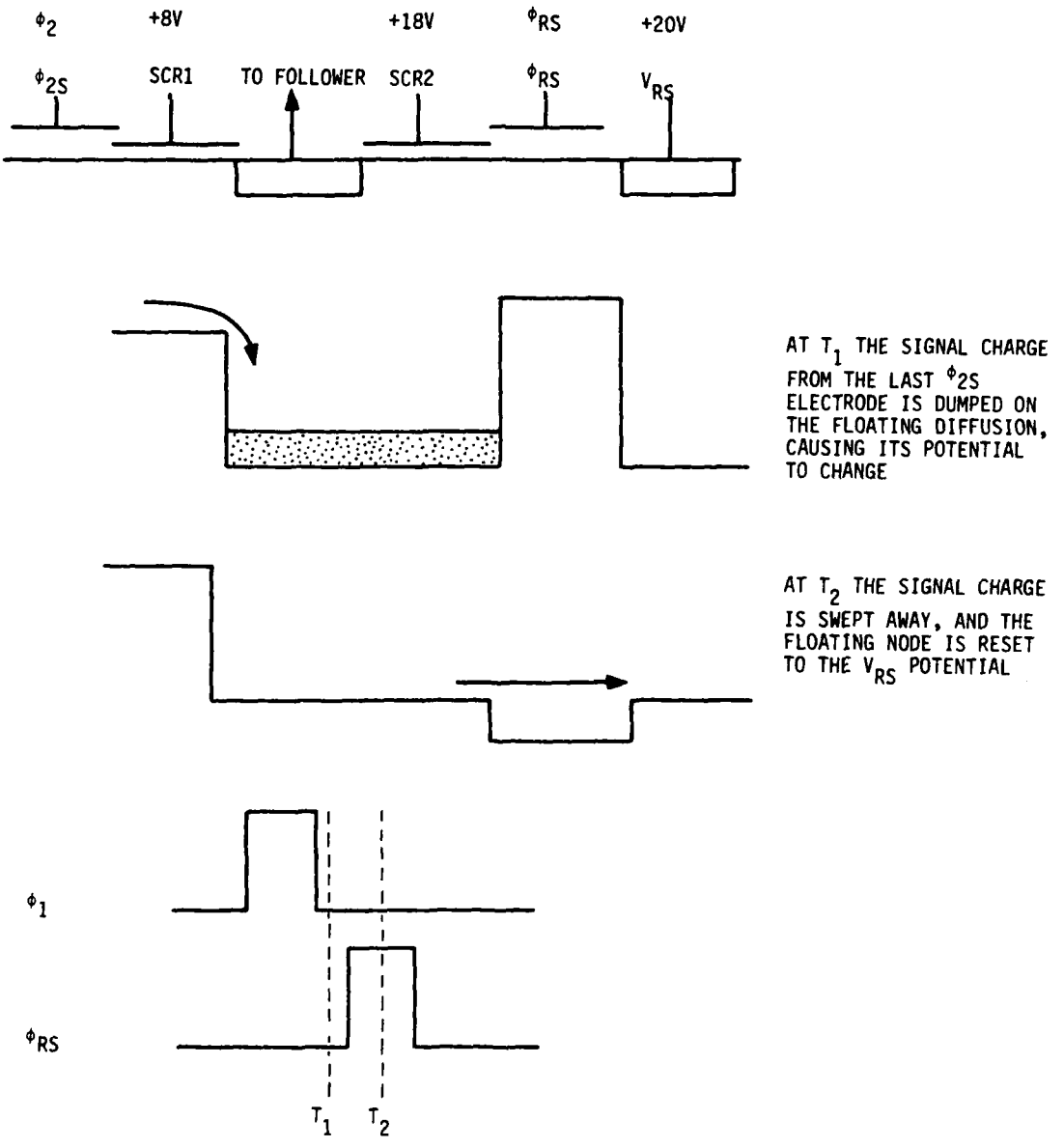


Figure 5. Output Circuit Operation

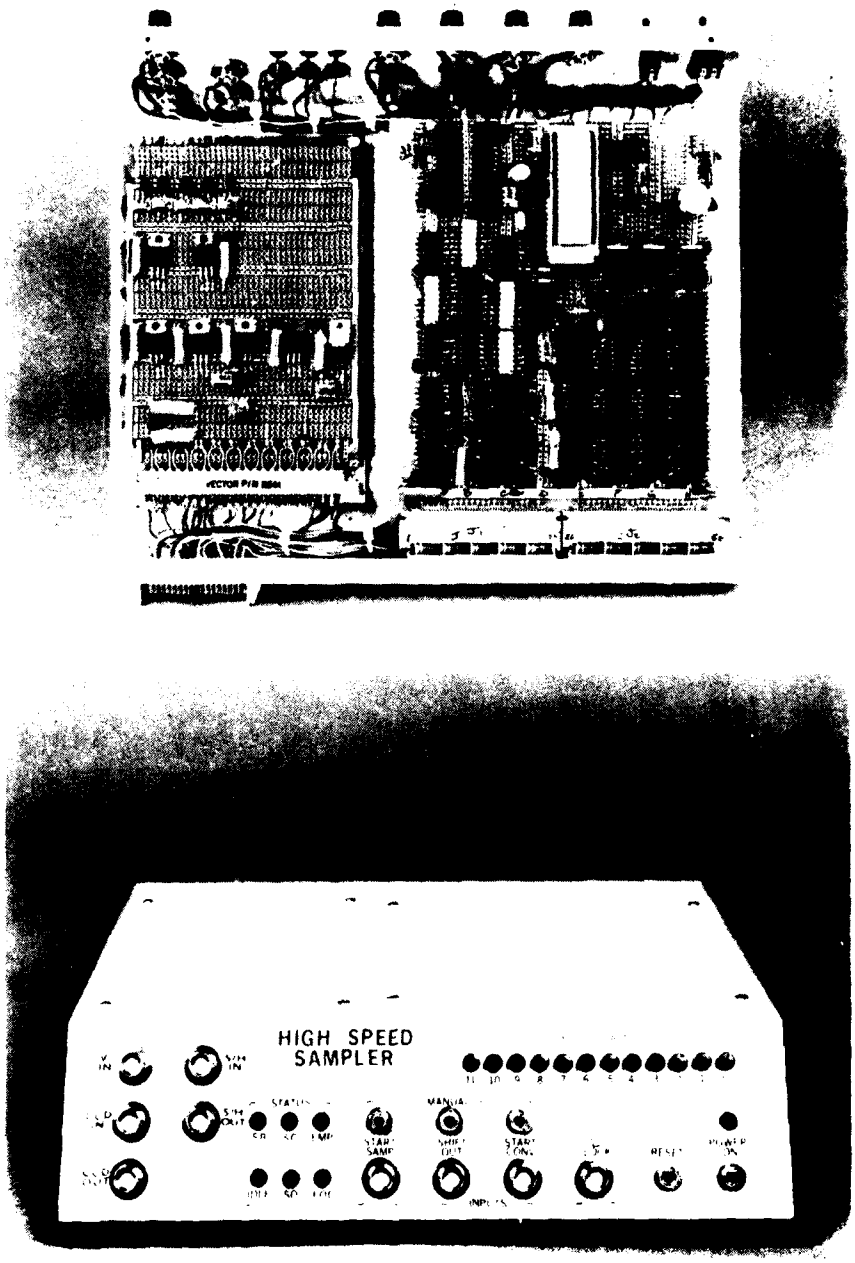


Figure 6. The Honeywell CCD Fast Sampler

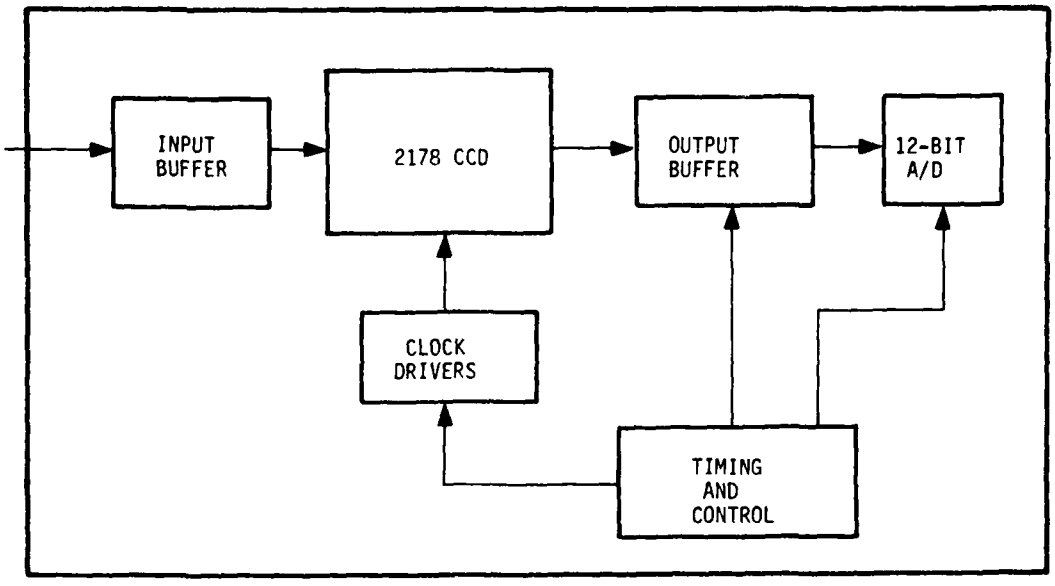


Figure 7. Fast-Sampler Block Diagram

Clock drivers for the CCD were commercially available MOS memory drivers. The drivers operated satisfactorily for clock rates up to 12 MHz; however, beyond this frequency the rise and fall times of the device were too slow and clock overlap occurred. The A/D converter selected for this application was selected primarily on the basis of availability and conversion speed, and its high power consumption proved to be a problem. The heat generated within the A/D proved to be a problem and a fan was required to cool the A/D to get adequate noise performance.

The output buffer in the CCD fast sampler consists of an amplifier, a double-correlated sampler (DCS), and a sample and hold circuit. As we

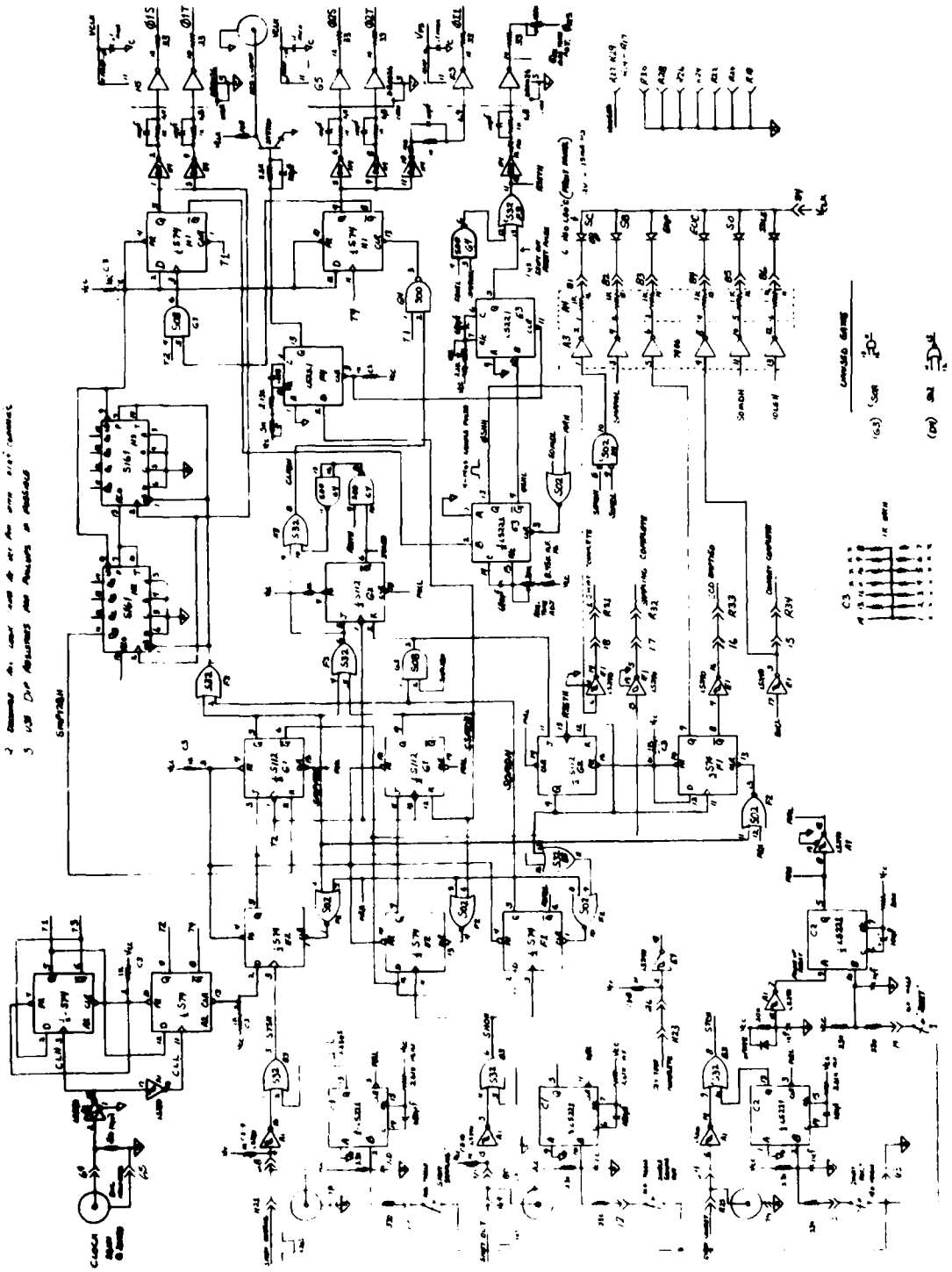


Figure 8a. Fast Sampler Logic and CCD Board

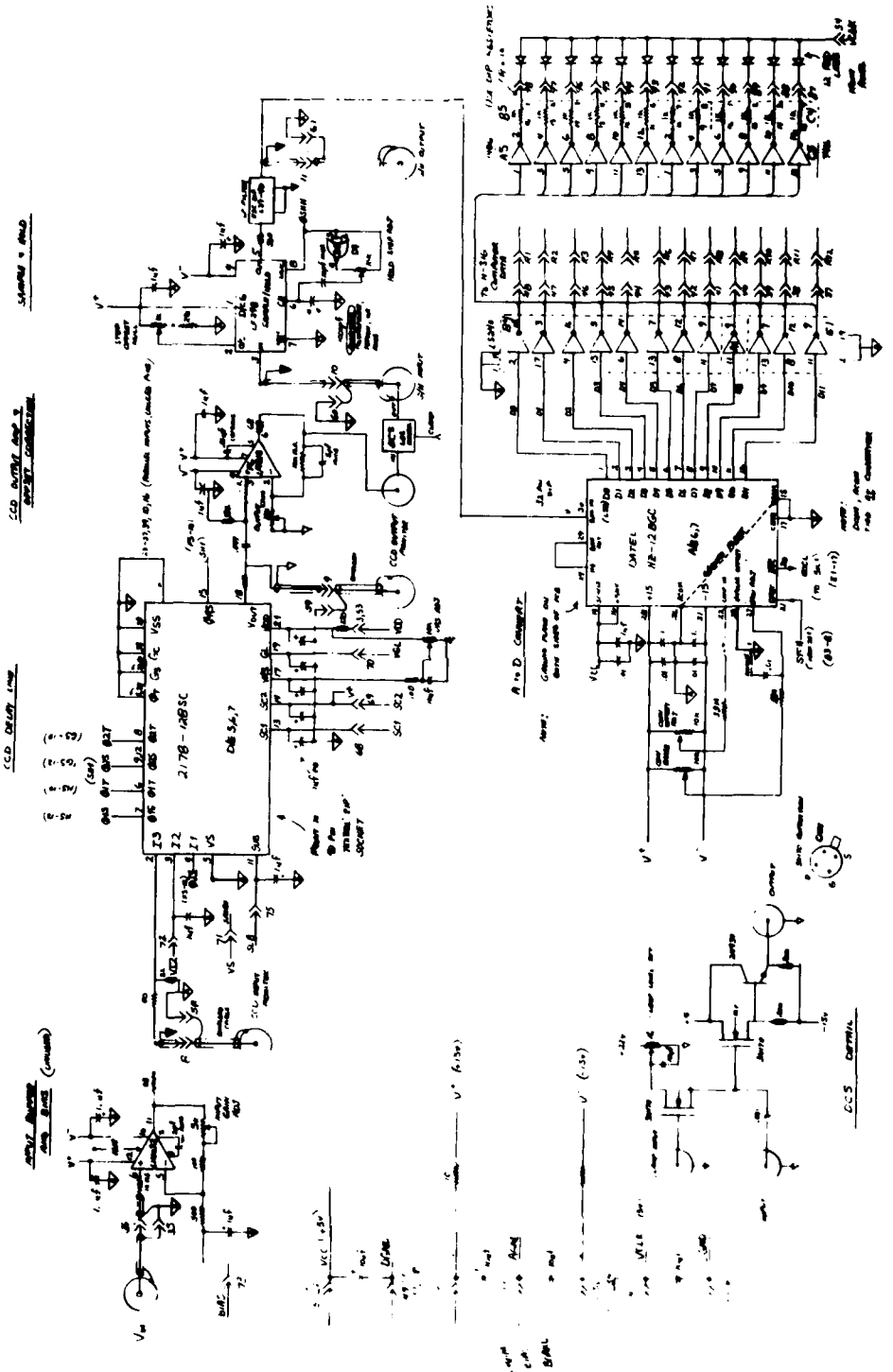


Figure 8b. Fast Sampler Logic and CCD Board (continued)

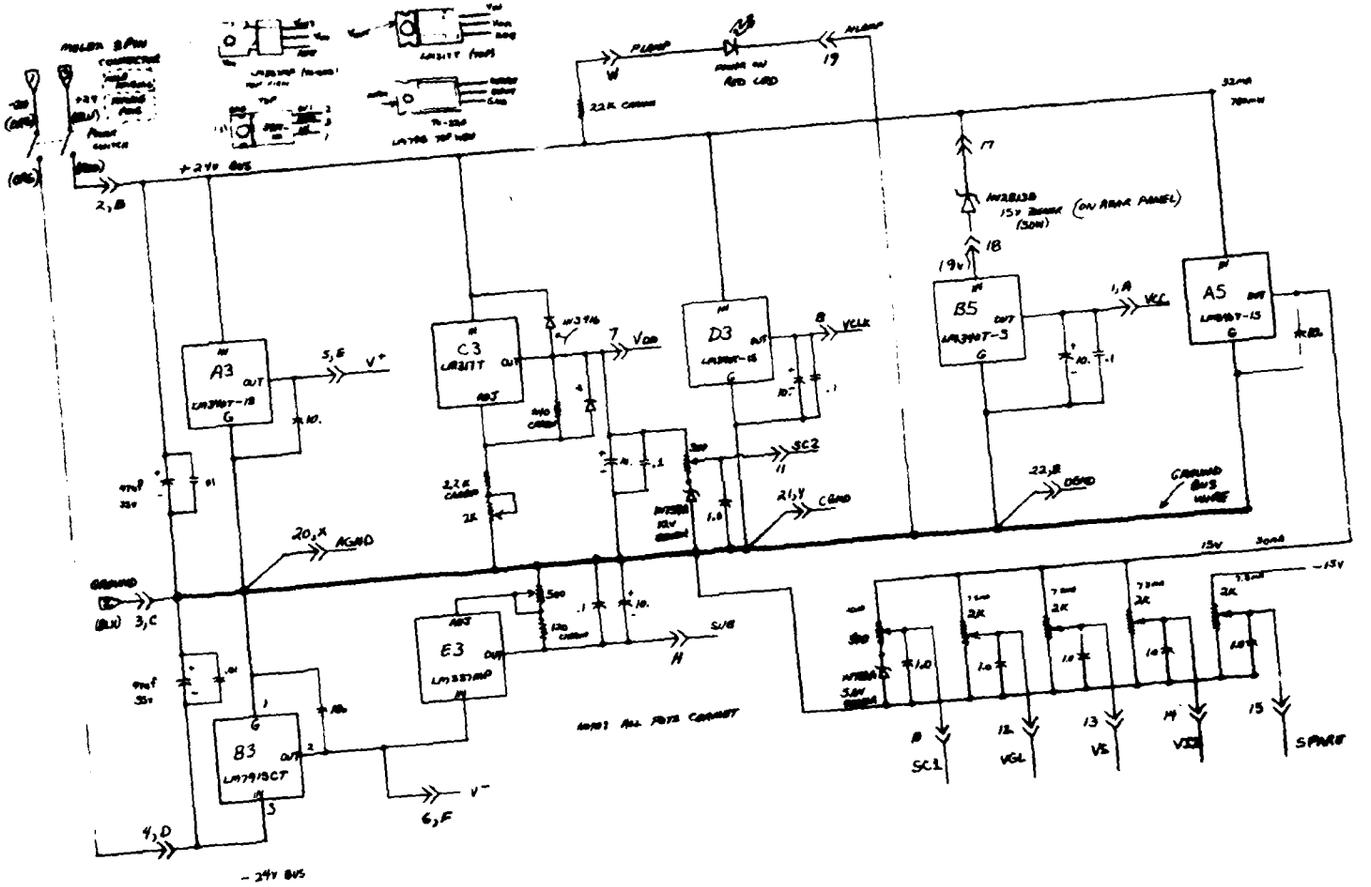


Figure 8c. Fast Sampler Logic and CCD Board (concluded)

will discuss in "Noise and Dynamic Range Performance" under Section III, the double-correlated sampler was added to remove charge-sloshing noise generated in the output circuit of the CCD. The circuit uses an AC-coupled signal from the CCD and responds to changes in the output voltage caused by the signal charge packets. Since the DCS input is AC coupled, its output DC level is independent of the DC level out of the CCD. Although it would seem that DC information must be lost in an AC-coupled system, the DC information is in fact present at the clock frequency, and the double-correlated sampler acts to "alias" this information back to its original DC form.

The timing and control circuitry synchronizes the external commands with the internal timing, generates the timing waveforms for the double-correlated sampler, sample and hold, and A/D converters, and generates the CCD clock waveforms. The machine is designed to operate in four basic modes or states: idle, sampling, wait, and shift out. These states and the transitions between them are shown in Figure 9. Three external commands control the state of the machine: start sampling, shift out, and reset.

The start sample pulse causes the sampler to switch into the sampling mode until 128 samples have been taken, at which time the machine automatically goes into the wait mode. Upon receiving the first shift out pulse, the machine will switch to the shift out mode, read a single analog sample to the A/D converter, and perform the conversion. On each subsequent shift out pulse, the next available sample is read and converted

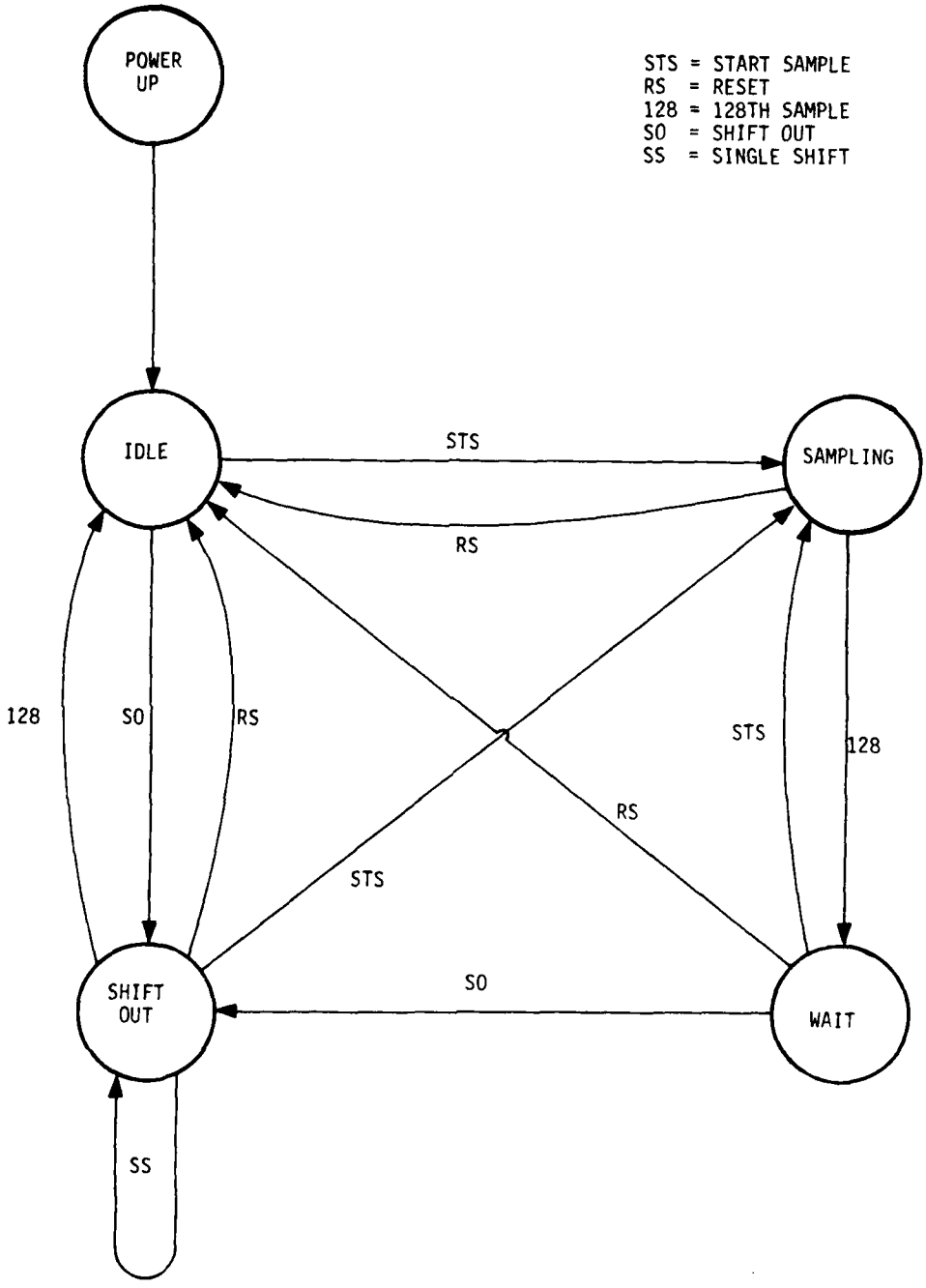


Figure 9. Tester State Diagram

until the 128th sample is taken. Upon receiving the 128th shift out pulse, the sampler shifts to the idle mode, in which the CCD shift register clocks are exercised to remove leakage charge from the channel. The reset command will return the machine to the idle mode from any other state.

THE FAST-SAMPLER SYSTEM

Operating the fast sampler and recording the data from it require a digital computer. For the tests which were performed for this program, machine availability was a far more important consideration than computational speed. Therefore, we selected the SYM-1 microcomputer to perform the system control and data processing functions. A diagram of the complete fast-sampling system which includes a CRT display, teletype, waveform generator, and the CCD fast sampler is shown in Figure 10, and a picture of the system is shown in Figure 11.

The SYM-1 Microcomputer

As mentioned above, the SYM-1 serves as the primary system controller, data processor, and human interface for the prototype sampling system. A block diagram of the SYM is shown in Figure 12. Our machine is equipped with monitor program in read only memory (ROM), as well as the optional BASIC high level interpreter in ROM. The monitor serves as the highest level executive operating system software source. Its functions include the cassette tape and CRT interfacing, as well as providing a command directory for BASIC and the operator. The SYM is also equipped

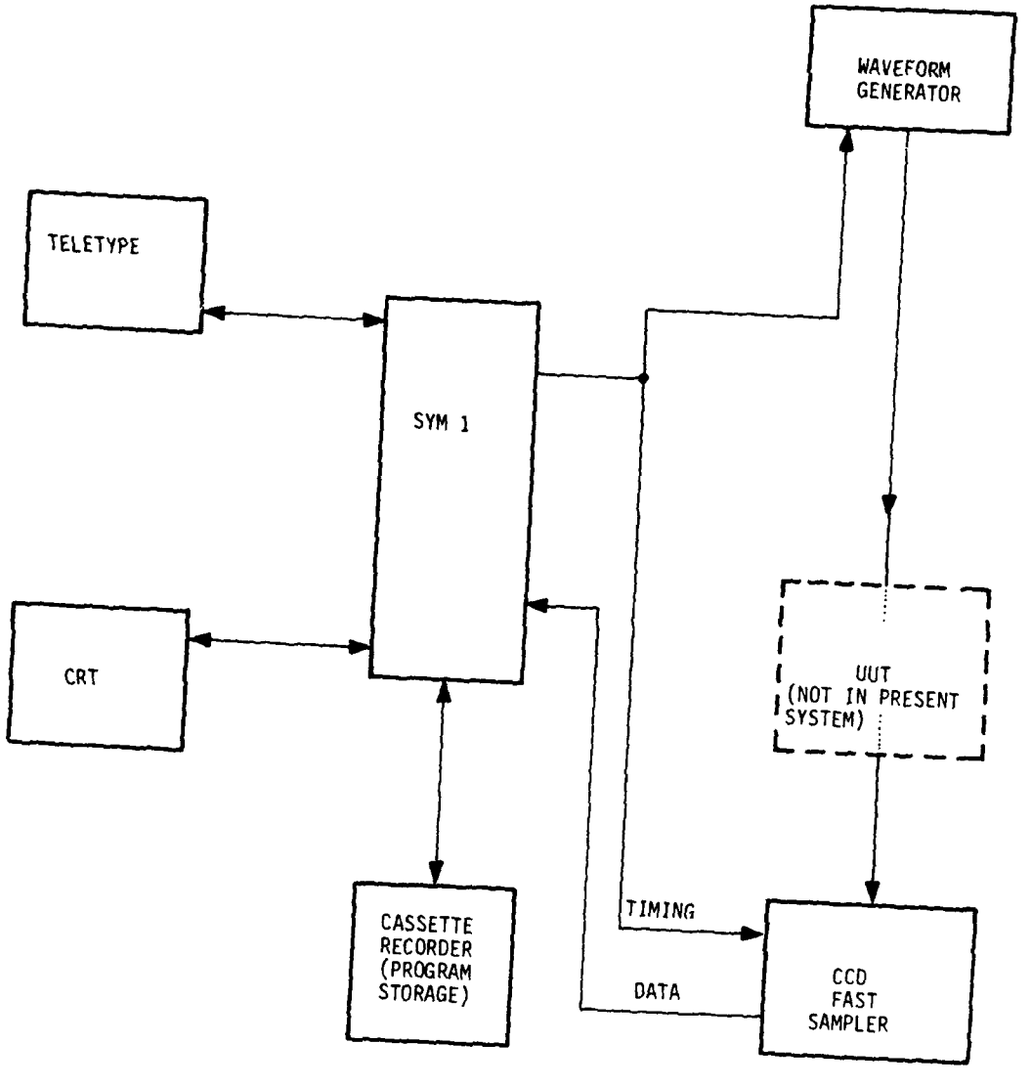


Figure 10. CCD Fast-Sampler System

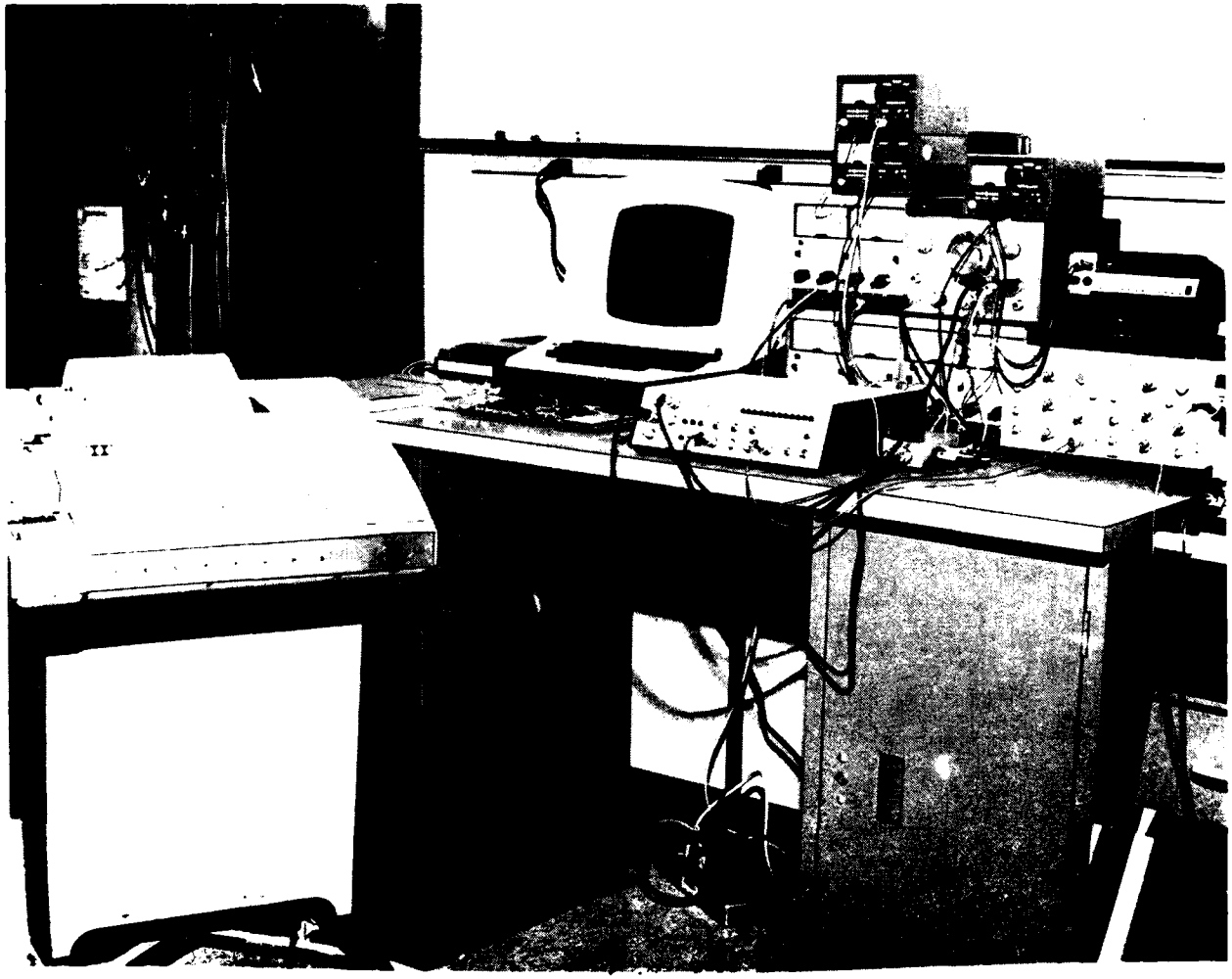


Figure 11. Complete Fast-Sampling System Including a CRT Display, Teletype, Waveform Generator, and the CCD Fast Sampler

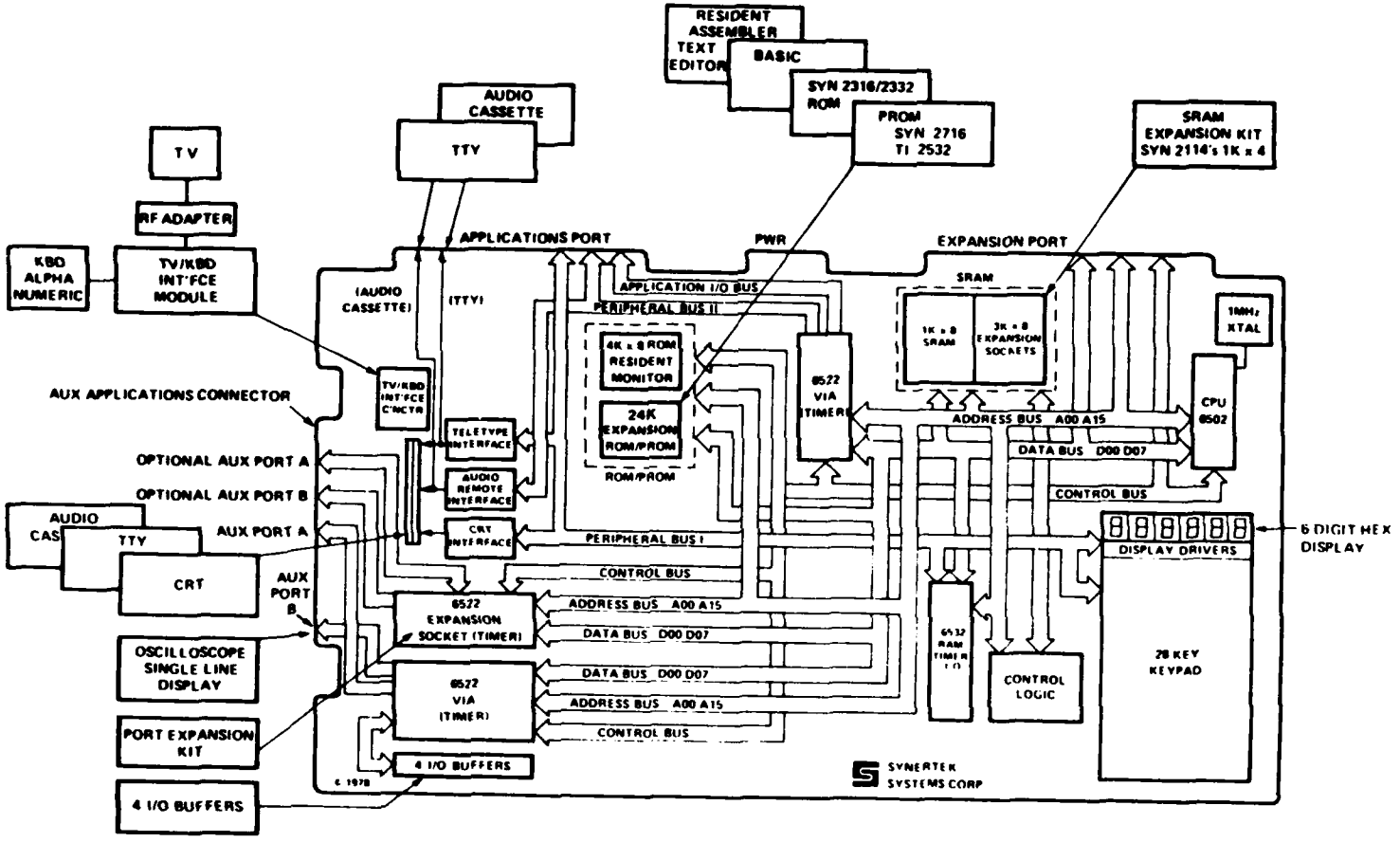


Figure 12. Functional Block Diagram

with 4096 bytes (1 byte = 8 bits) of random access memory (RAM) which is used for user program storage. The built-in versatile interface adapters (VIAs) on the SYM board are what allowed very simple, fast interfacing of it to the output of the A/D converter in the Fast Sampler. These units provided a 16-bit parallel, memory-mapped data transfer path for the sampler outputs and handshake lines as described earlier. The last important aspect of the SYM in the system is its built-in cassette tape interface. This feature allowed us to develop all system software in RAM and then store it on tape for later use. As an added benefit, it also serves as a permanent storage medium for the fast-sampler data output.

System Design Approach

Designing and integrating the microcomputer with the fast sampler to form a functional unit involved three important steps:

1. Design the electrical interface for the A/D converter digital output and control to the SYM-1 parallel I/O ports.
2. Design an assembly language/machine code program to handle the sampling initiation and data read-in to computer at high speed.
3. Design a BASIC source code program working under monitor control that works with the fast-sampler digital data after it has been put in RAM by the program in step 2. This BASIC code must provide a meaningful display of the sampler outputs and form the control architecture for further processing algorithms and user command interface.

The software/hardware hierarchy of the fast-sampler system is shown in Figure 13. We next describe the three designs above in some more detail. This will lead us to the role and impact on the system which results from this software approach, the performance constraints imposed, and its future potentials.

The SYM Fast-Sampler Electrical Interface

The fast sampler generates a total of 128 12-bit binary numbers for each pass through its "sampling" state. (Figure 9). Since the SYM is basically an 8-bit computer, we are required to represent each 12-bit point by 2 bytes of SYM memory. The user VIA on the SYM allows us to transfer two 8-bit bytes in parallel format at memory-read speeds. The VIA also has four control lines over which we can exercise software control. As a result, we have a 20-bit I/O interface to the fast sampler over which we can send data and exchange handshake control of the signals start sampling, sampling complete, shift out, convert complete, CCD empty, and reset empty (Figure 14).

This scheme of memory-mapped parallel I/O was chosen for its relatively high speed and simplicity. Other I/O schemes such as direct memory access (DMA) or asynchronous serial transmission were considered but rejected since the SYM does not support DMA, and serial I/O is much too slow.

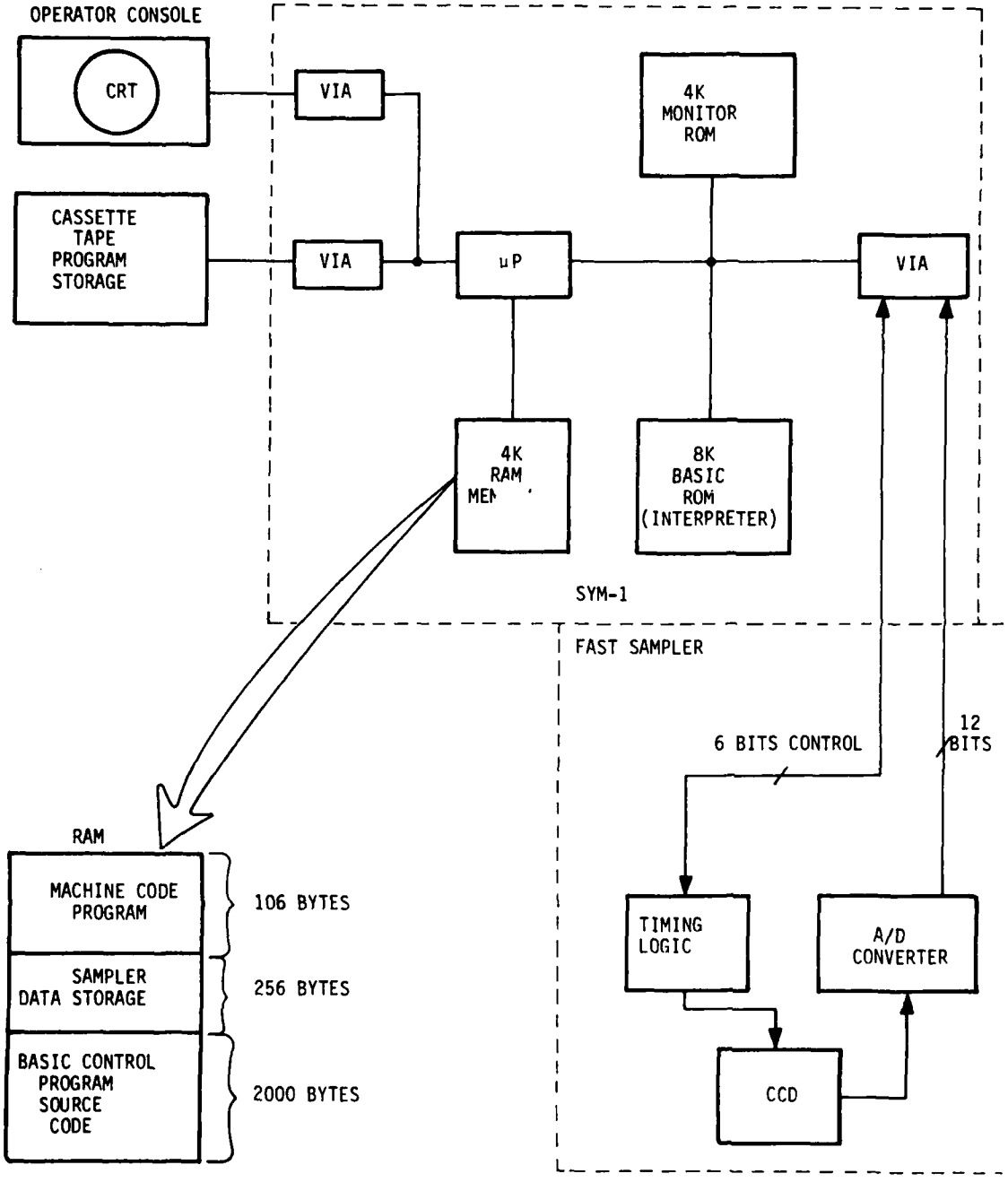


Figure 13. The Fast-Sampler Hardware/Software System Detail

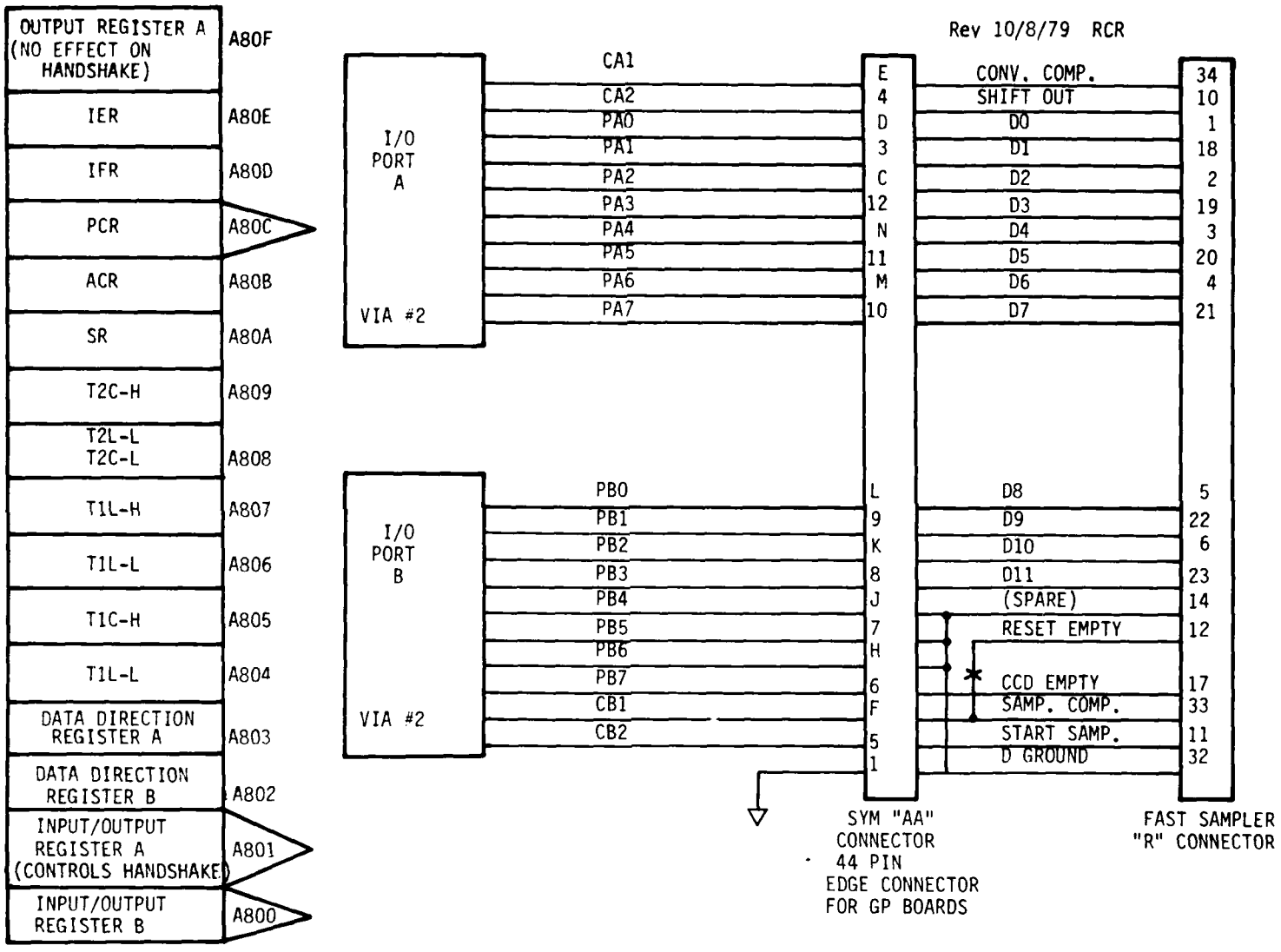


Figure 14. Fast-Sampler SYM-1 Interface Connections

The Machine-Code Data Acquisition Program

The process of actually sequencing the fast sampler through the tester states in Figure 9 is accomplished through a 106-byte machine-code program whose flow chart is shown in Figure 15. This program is called each time the user desires to capture a new 12.8 μsec segment of the input waveform. Control is passed to the routine via the SYM monitor from the BASIC control/display program. Some important aspects of this code segment include the following:

1. It is full handshaking; all commands to the fast sampler are expected to generate a reply from it. This fast-sampler reply is waited upon before the next state is initiated.

2. Since each data point is read as two bytes, the absolute minimum time between shift outs is determined by the time to execute two memory reads and two memory store instructions. Because the SYM has a 1 μsec machine cycle and the read/writes taking place require four machine cycles each, the lower limit of the shift out period is 16 μsec. Because of the handshake testing necessary, the true period is near 38 μsec.

3. The machine code places the new data set in a contiguous 256-byte block RAM. In this way, the BASIC control/display program is entirely isolated from the actual fast-sampler control and data acquisition process.

The assembly code listing for the data acquisition program is in Figure 16. This program is written in the assembly language for the Synertek 6502

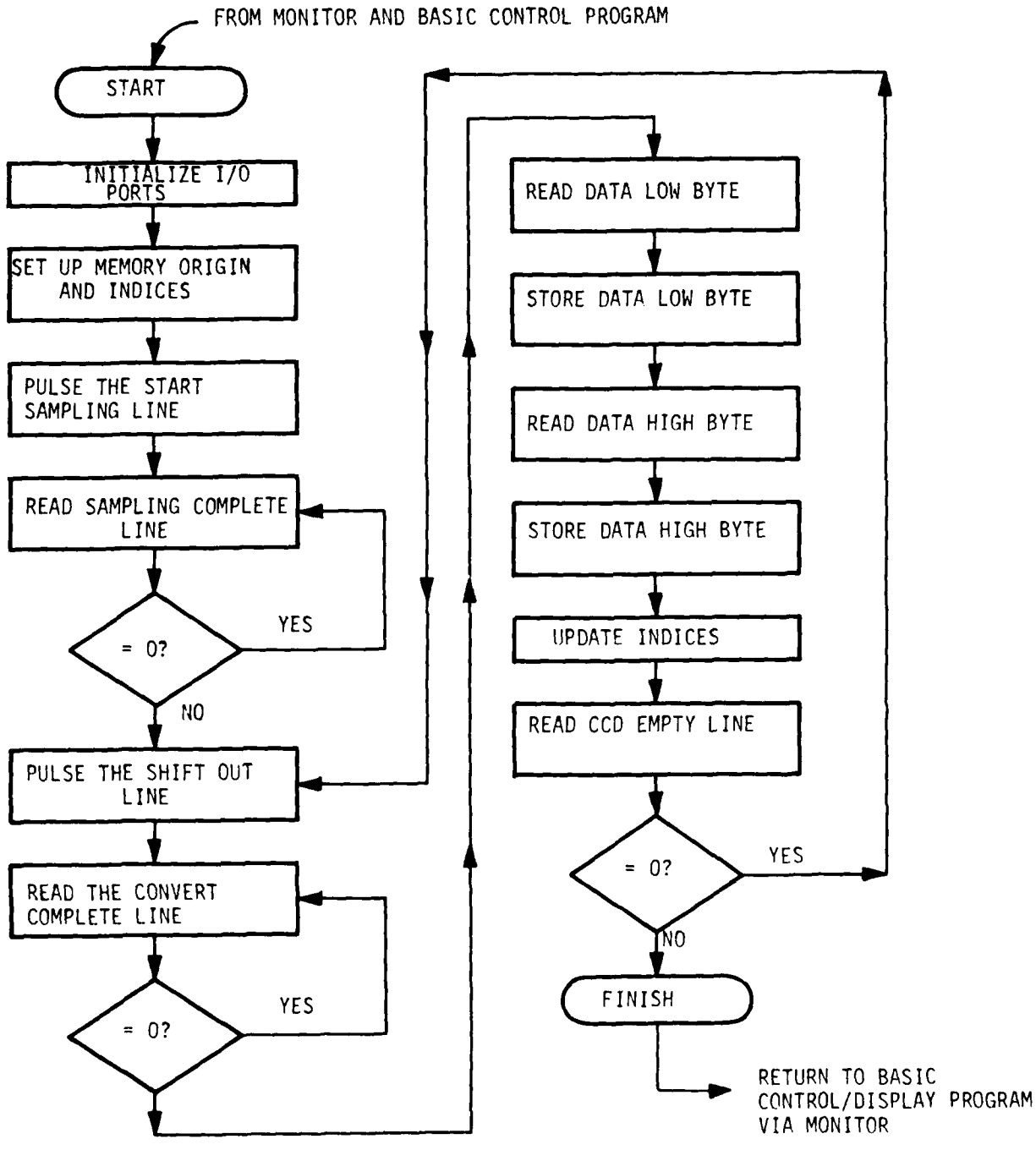


Figure 15. Data Acquisition Machine Code Program Flow Chart

ADDR	INSTRUCTIONS B1	B2	B3	LABEL	MNEMONIC	OPERAND	COMMENTS
--					* =	$A800	VIA #2 BASE ADDRESS
A800				VIA2	* =	*	
A800				IORB2	* =	* +1	I/O REGISTERS A, B
A801				IORA2	* =	* +1	
A802				DDRB2	* =	* +1	DATA DIRECTION REGISTERS A, B
A803				DDRA2	* =	* +1	
A804				TIM2	* =	* +7	TIMER CONTROL (UNUSED)
A80B				ACR2	* =	* +1	AUXILIARY CONTROL REGISTER
A80C				PCR2	* =	* +1	PERIPHERAL CONTROL REGISTER
A80D				IFR2	* =	* +1	INTERRUPT FLAG REGISTER
A80E				IER2	* =	* +1	INTERRUPT ENABLE REGISTER
A80F				ORA2	* =	* +1	OUTPUT REGISTER (UNUSED)
				ZERO	=	$ 0	VALUE ZERO
0F00					* =	$ 0F00	SET DATA BLOCK ORIGIN TO $ 0F00
1000				DBLK	* =	* + $0100	RESERVE 256 BYTES FOR DBLK
				ENTRY	* =	$ 0E60	SET ORIGIN OF PROGRAM START
0E60	A9	00			LDA	# ZERO	ZERO ACCUMULATOR
0E62	8D	03	A8		STA	DDRA2	SETUP DATA DIRECTION REGISTERS
0E65	8D	02	A8		STA	DDRB2	FOR INPUT MODE
0E68	8D	0C	A8		STA	PCR2	CLEAR PERIPHERAL CONTROL REGISTER
0E6B	8D	0B	A8		STA	ACR2	CLEAR AUXILIARY CONTROL REGISTER DISABLE LATCH

Figure 16a. Data Acquisition Assembly Code

ADDR	INSTRUCTIONS			LABEL	MNEMONIC	OPERAND	COMMENTS
	B1	B2	B3				
0E6E	78				SEI		DISABLE INTERRUPTS
0E6F	A9	92			LDA	#92	LOAD IER MASK
0E71	8D	0E	A8		STA	IER2	PUT IER IN SET MODE
0E74	A9	6D			LDA	#6D	ENABLE IRQ FOR CONV. COMP. OR SAMP. COMP.
0E76	8D	0E	A8		STA	IER2	
0E79	AD	01	A8		LDA	IORA2	CLEAR PENDING INTERRUPTS
0E7C	AD	00	A8		LDA	IORB2	
0E7F	A9	AB			LDA	#AB	SET PCR SO INTERRRUPTS ARE EDGE
0E81	8D	0C	A8		STA	PCR2	TRIGGERED (FALLING ON SAMP. COMP
0E84	4C	00	0E		JMP	ACQ	AND RISING ON SHIFT COMP.) AND
					* =	$ 0E00	JUMP TO ACQUISITION CODE
0E00	A9	00		ACQ	LDA	# ZERO	
0E02	AA				TAX		ZERO MEMORY INDEX
0E03	8D	00	A8		STA	IORB2	PULSE CB2 LINE TO ST. SAMPLING
0E06	AD	0D	A8	TSTF1	LDA	IFR2	
0E09	10	FB			BPL	TSTF1	TEST FOR SAMPLING COMPLETE
0E0B	AD	00	A8		LDA	IORB2	CLEAR INPUT IF DONE
0E0E	AD	01	A8		LDA	IORA2	COMMAND FIRST SHIFT OUT
0E11	AD	0D	A8	TSTF2	LDA	IFR2	
0E14	10	FB			BPL	TSTF2	TEST FOR CONVERT COMPLETE
0E16	AD	00	A8		LDA	IORB2	GET HIGH ORDER BYTE
0E19	30	0F			BMI	FINISH	TEST FOR CCD EMPTY

Figure 16b. Data Acquisition Assembly Code (continued)

ADDR	INSTRUCTIONS			LABEL	MNEMONIC	OPERAND	COMMENTS
	B1	B2	B3				
0E1B	A8				TAY		SAVE HIGH ORDER BYTE
0E1C	AD	01	A8		LDA	IORA2	GET LOW ORDER BYTE AND RESHIFT
0E1F	9D	00	0F		STA	DBLK, X	STORE LOW ORDER BYTE
0E22	E8				INX		MOVE STORAGE INDEX
0E23	98				TYA		RETRIEVE HIGH ORDER BYTE
0E24	9D	00	0F		STA	DBLK,X	STORE HIGH ORDER BYTE
0E27	E8				INX		MOVE STORAGE INDEX
0E28	D0	E7			BNE	TSTF2	BRANCH AND WAIT FOR SHIFT COMP.
0E2A	29	7F		FINISH	AND	#7F	MASK OUT CCD EMPTY BIT 7
0E2C	A8				TAY		SAVE HIGH ORDER BYTE
0E2D	A9	AF			LDA	#AF	
0E2F	8D	0C	A8		STA	PCR2	DISABLE AUTO RESHIFT OUT
0E32	AD	01	A8		LDA	IORA2	GET LOW ORDER BYTE,RESET INTRPT.
0E35	9D	00	0F		STA	DBLK, X	STORE LOW ORDER BYTE
0E38	E8				INX		MOVE POINTER
0E39	98				TYA		RETRIEVE AND
0E3A	9D	00	0F		STA	DBLK, X	STORE HIGH ORDER BYTE
0E3D	A9	A8			LDA	#AB	
0E3F	8D	0C	A8		STA	PCR2	REENABLE SHIFT-OUTS
0E42	60				RTS		RETURN TO MONITOR AND BASIC
							CONTROL PROGRAM

Figure 16c. Data Acquisition Assembly Code (concluded)

microprocessor used by the SYM-1. The actual machine code in hexadecimal format as it appears in memory is shown in Figure 17.

BASIC Control Program

The BASIC program used for system control and data display is listed in Figure 18 and is flow charted in Figure 19. A state diagram for the program is shown in Figure 20. Upon starting the system the operator is instructed to actuate the sampling subroutine. Once the sampling routine is complete, the operator has a choice of four formats for reading out the data: decimal-converted binary code, voltage-converted binary code, low-resolution plot, and high-resolution plot. The decimal-converted binary and voltage-converted binary data are self-explanatory. The low-resolution plot is a plot of the entire dynamic range of the A/D converter,

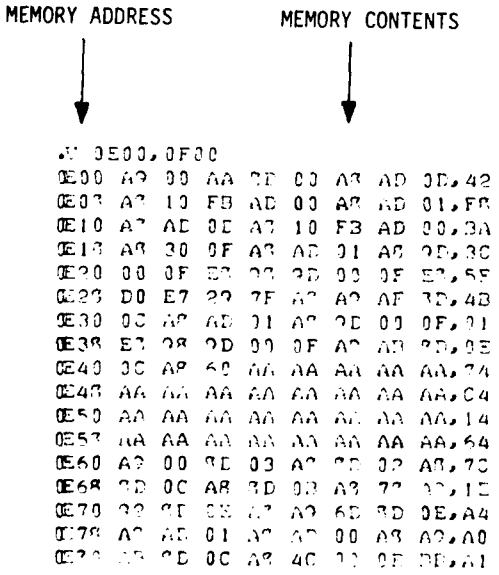


Figure 17. Machine Code for Data Acquisition Program

```
10 PRINT"FAST SAMPLER DATA ACQUISITION/DISPLAY PGM V1.0"
15 PRINT
20 NULL 1
25 INPUT"TYPE A 1 AND C/R TO TAKE DATA?";I
30 IF I<>1 THEN 20
40 I=USR(&"0E60",&"0000")
45 GOTO 40
50 DBLK=&"0F00"
60 DEF FNZ(V)=20.*LOG(V)/LOG(10.)
70 PRINT "SAMPLING COMPLETE--SELECT OUTPUT TYPE CODE":PRINT
80 PRINT"0 FOR BINARY DATA LIST"
90 PRINT"1 FOR CONVERTED VOLTAGE DATA LIST"
100 PRINT"2 FOR LINE PRINTER PLOT":PRINT"3 FOR NEW DATA"
102 PRINT"4 FOR HIGH RESOLUTION PLOT"
105 PRINT"C/R ONLY TO QUIT"
110 INPUT"TYPE OUTPUT CODE AND C/R";I
115 IF I=4 THEN GOTO 350
120 IF I<>0 AND I<>1 AND I<>2 AND I<>3 THEN PRINT"BAD CODE":GOTO 110
130 ON I+1 GOTO 140,160,260,20
140 FOR IND=0 TO 254 STEP 2
150 GOSUB 500:PRINT D,:NEXT IND
155 PRINT:GOTO 110
160 MAXV=-10000.:MINV=10000.:SUMV=0.
170 FOR IND=0 TO 254 STEP 2
180 GOSUB 500:GOSUB 530:PRINT V,:SUMV=SUMV+V
190 IF V<MINV THEN MINV=V
200 IF V>MAXV THEN MAXV=V
210 NEXT IND
220 VRANG=MAXV-MINV:VMEAN=SUMV/128.:PRINT
230 DA=FNZ(VRANG/SQR(2.)):PRINT
240 PRINT"VMAX=";MAXV,"VMIN=";MINV,"VRANGE=";VRANG
250 PRINT "VMEAN=";VMEAN,"RANGE IN DBV=";DA:GO TO 110
260 PRINT:PRINT TAB(25)"VOLTAGE PLOT"
270 PRINT "0.0" TAB(60) "+5.0"
280 FOR I=1 TO 71:PRINT"-";:NEXT
290 FOR IND=0 TO 254 STEP 2
300 GOSUB 500:X=71*D/4095.:PRINT TAB(X)"*"
305 NEXT IND
310 GO TO 110
350 PRINT "PRESENT LOWER LIMIT=";0
351 INPUT "DESIRED LOWER LIMIT?=";0
360 PRINT 0 TAB(60) 0+60
370 FOR I=1 TO 71:PRINT "I";:NEXT
390 FOR IND=0 TO 254 STEP 2
390 GOSUB 500:X=D-0
392 IF X<0 THEN X=0
393 IF X>71 THEN X=71
394 PRINT TAB(X)"*"
395 NEXT IND
400 GOTO 110
420 SUMV=0
425 FOR IND=0 TO 254 STEP2
430 GOSUB 500
435 SUMV=SUMV+D:NEXT IND
440 VAVE=SUMV/128
445 PRINT"COUNT=";INT(VAVE);TAB(20):INPUT"INPUT VOLTAGE=";M
455 I=1
460 GOTO 30
500 A1=DBLK+IND:A2=A1+1
505 D=PEEK(A1)+256.*PEEK(A2)
510 RETURN
530 V=5*D/4096
540 RETURN
550 END
```

Figure 18. BASIC Program for System Control and Data Display

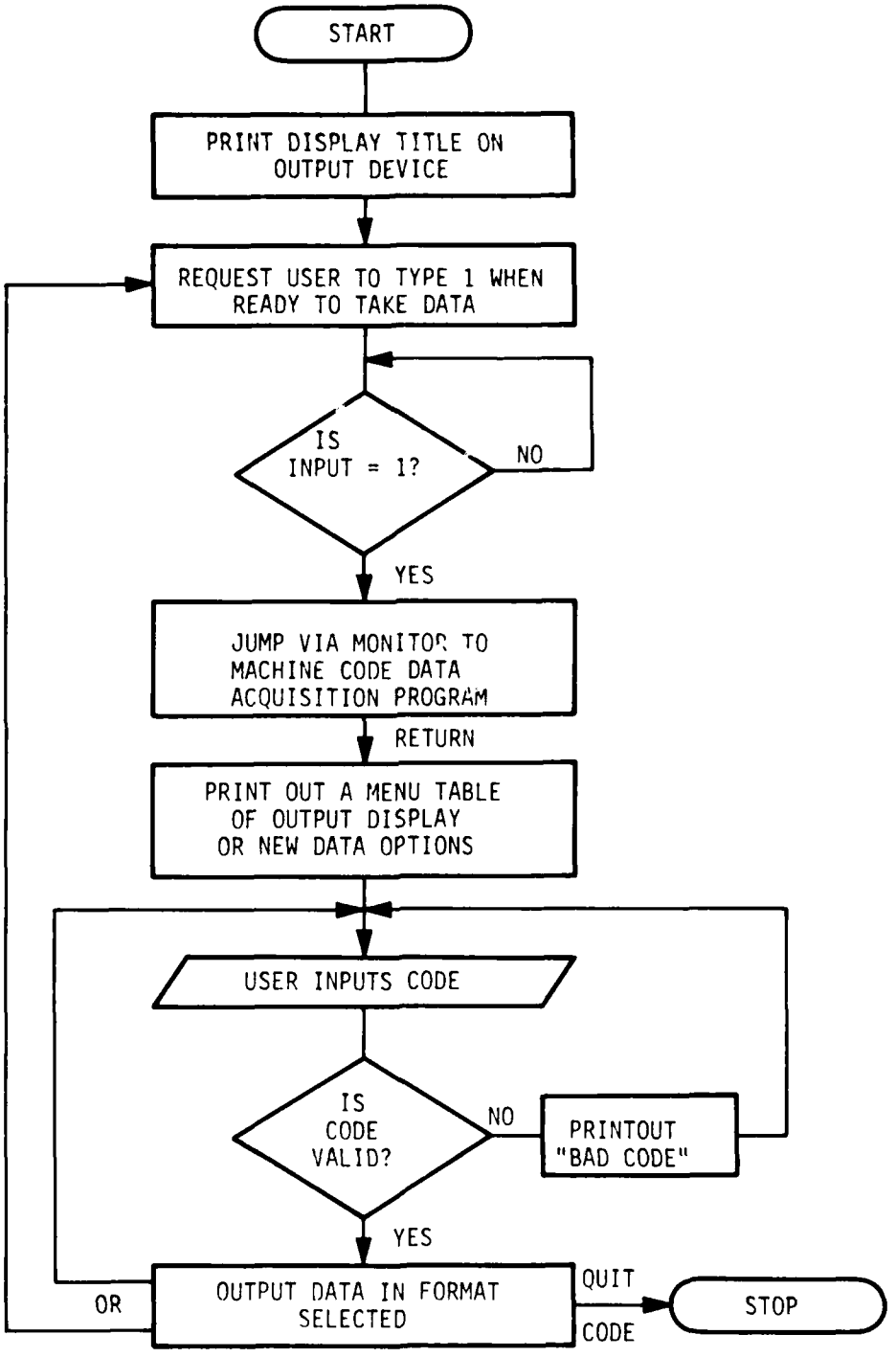


Figure 19. BASIC Flow Chart for System Control and Data Display

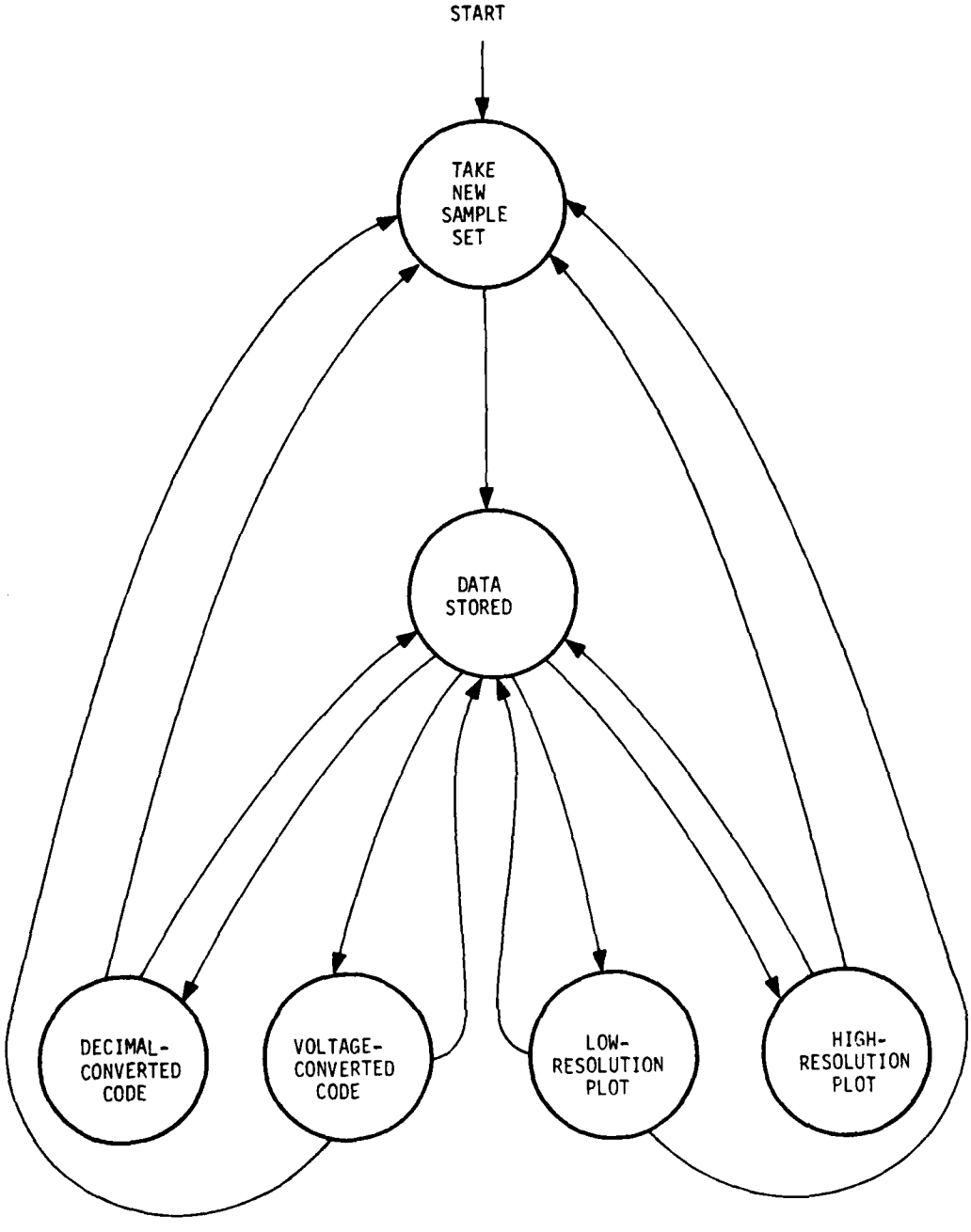


Figure 20. State Diagram for Fast-Sampler System

which gives a resolution of about 70 millivolts. The high-resolution plot looks at a specified 72-bit window of the A/D converter output giving a resolution of 1.2 millivolts. These readout routines represent only a minimum system, and it took considerable restraint to not develop signal-processing algorithms to demonstrate the machine's true capabilities. Programs to perform spectral analysis, low-pass filtering, and rise-time measurements are just a few of those which can be done on this machine.

System Software/Hardware Tradeoffs

The way in which the system software is designed and implemented affects several performance characteristics of the overall fast sampler:

1. Shift out speed from the CCD determines, in part, the useful available dynamic range (see "Leakage Measurements" under Section III). The shift out speed is a function of both the method of data transfer and the hardware performance. Figure 21 shows the tradeoffs involved.

2. The machine word size affects data transfer speed and the numerical accuracy in results of any signal processing beyond data recording/display.

3. The address range of the microprocessor determines the maximum amount of RAM/ROM which can be used. The SYM addresses 65,536 bytes of memory which is sufficient for all but the most ambitious tasks. (An in-place FFT algorithm requires only 3000 bytes.)

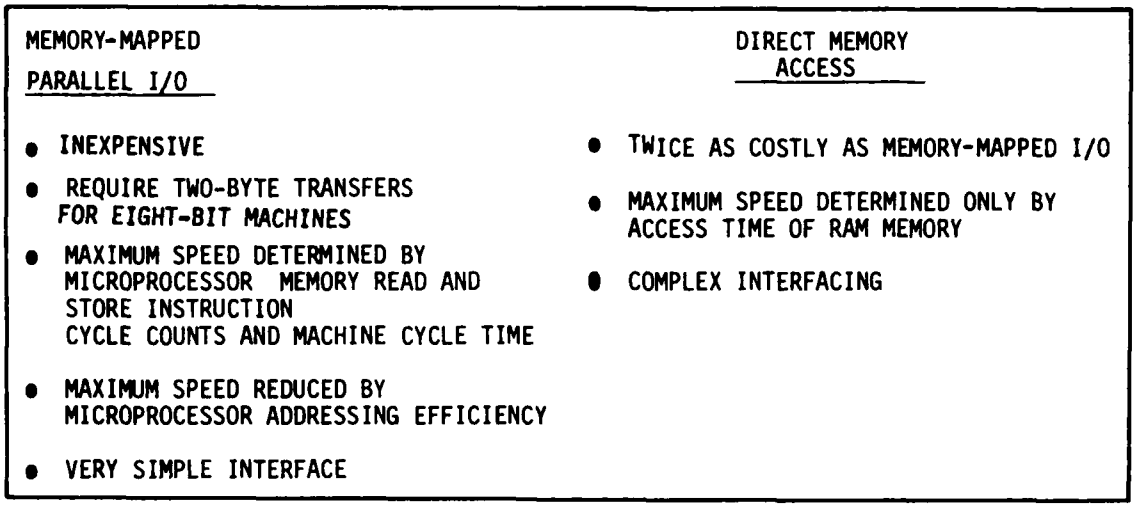


Figure 21. Computer System Digital Data Input Methods: System Tradeoffs

4. The programming language used affects overall computation speed. We programmed the data acquisition in machine code for high speed. The control/display program in BASIC is interpretive and runs nearly a factor of three slower than if it were written in machine code. Signal-processing speed is traded off against the ease of using BASIC coding.

Recommended Computer/Software Approach for Future ATE Fast Sampler

As we have seen, there are a number of design tradeoffs available in specifying the computer portion of a deployable fast-sampler system.

Below are our recommendations for a versatile digital control/processor for CCD fast sampling.

1. Use a 16-bit machine to eliminate the present 2-byte transfer time of an 8-bit machine for 12-bit data.

2. Use a microprocessor which supports Direct Memory Access for sampler-to-computer data transfer speed which is limited only by the A/D converter.

3. Use EPROM or mask-programmed ROM for all program storage. This still allows the system to be field configurable for various ATE applications.

4. Perform all signal-processing algorithms in a higher level, machine-codable, non-interpretive language such as FORTRAN, Pascal, or even DOD-ADA. This will allow optimum test response time and promotes ultimately better software documentation, especially if a structured language such as Pascal or ADA is used.

5. Floating point representation of numeric data in signal-processing algorithms using 16-bit mantissa and 8-bit exponents is recommended. This will assure virtually no roundoff error in processes such as the inplace FFT. (The SYM BASIC used this type of numeric representation.)

A system with 28K words of EPROM and 8K words of RAM memory should prove sufficient for most potential ATE application programs envisioned at this time. See Section IV.

SECTION III

TEST RESULTS

NOISE AND DYNAMIC RANGE PERFORMANCE

There are three primary sources of noise in CCDs: input circuit noise, transfer noise, and output circuit noise. Measurements of the 2178 have shown that the most easily isolated noise source is the output circuit, since it is the only circuit function which can be operated by itself. It was also found that the output circuit contributed the majority of the system noise and that input and transfer noise could be observed only after methods to reduce output noise were employed.

In most conventional treatments of CCD output noise, the primary noise source is considered to be the reset noise described by the following equation:

$$V_{noise} = \sqrt{\frac{2}{3}\frac{KT}{C}}$$

where K is Boltzmann's constant, T is absolute temperature, and C is the capacitance of the output node. For the 2178 device, the theoretical noise is -118 dBV for a clock frequency of 100 kHz and a band width of 100 Hz. However, the measured output noise of the 2178 device was close to -90 dBV. The source of this noise was found to be charge-sloshing noise due to inexact charge splitting as the ϕ_{RS} gate is turned off as shown in Figure 22. The amount of noise generated by this phenomenon is highly

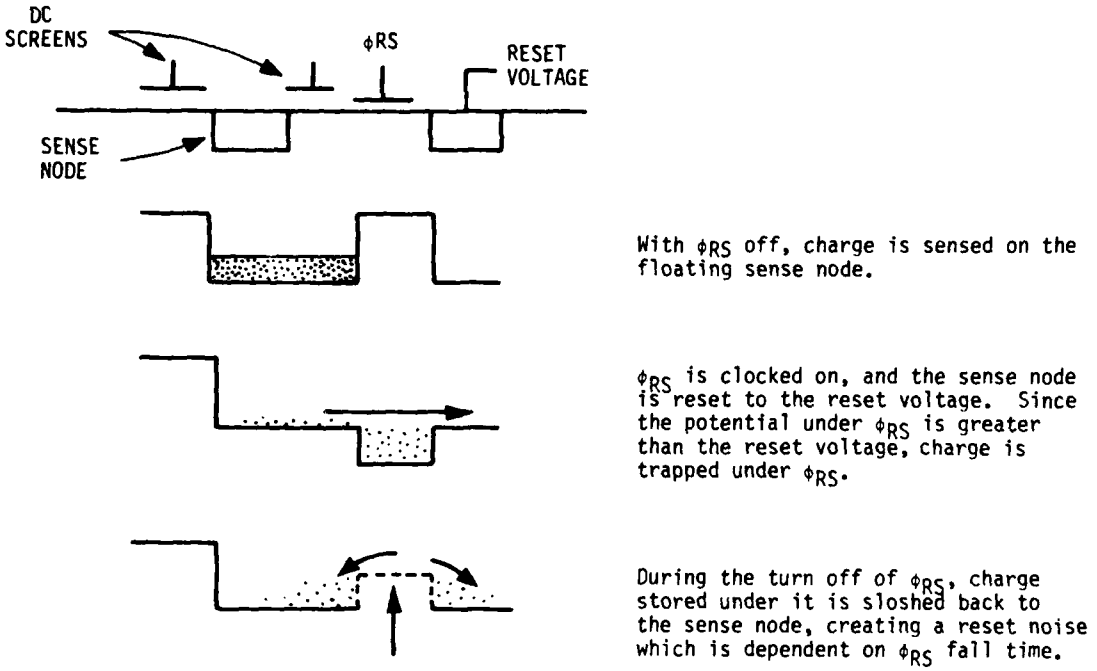


Figure 22. Charge-Sloshing Noise Generation in the 2178 CCD

dependent upon the fall time of the ϕ_{RS} gate. This is demonstrated in Figure 23 which shows the noise out of the 2178 CCD with ϕ_{RS} fall times of 50 nanoseconds and 2 μsec. A 20 to 25 dB noise improvement can be observed. A similar result can be obtained by reducing the voltage on ϕ_{RS} so that a minimum of charge is stored under it.

In an actual fast sampler, it is highly desirable not to have to specify the ϕ_{RS} fall time and amplitude to reduce system noise. It was therefore decided to employ a double-correlated sampling circuit to reduce output noise (Figure 24). By using an external reset clamp, this circuit measures only the output charge packet. The circuit therefore removes the charge-sloshing noise without dependence upon clock waveform control. As we

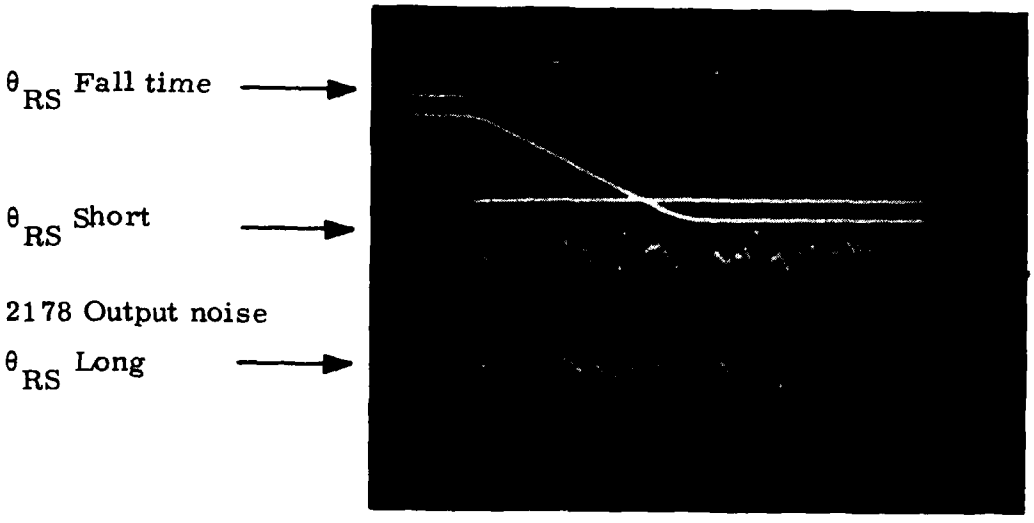
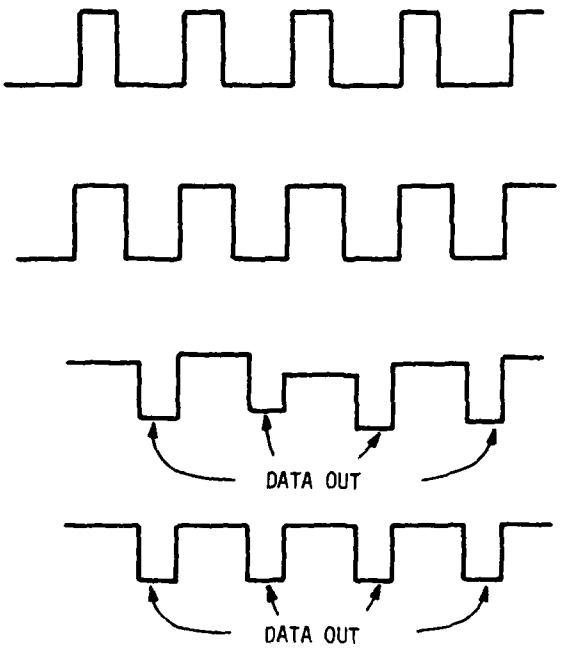


Figure 23. 2178 Output Noise Fluctuation Caused by Changing ϕ_{RS} Fall Time

discussed in the circuit description of the system, this circuit also will set the proper DC level for the A/D converter because its output is not dependent upon the DC level out of the CCD device. Using the double-correlated sampler, therefore, makes changing CCD devices a much easier process since no DC output adjustment is required.

Input and transfer noise were much harder to measure in this application since no continuous waveforms are available for sampling. In addition, since no noise measurement can be made except at the output node, input and transfer noise must be measured together and separated by inference. In addition to these problems, in the existing fast sampler, the input circuit was not RF-shielded at the input to the CCD. We presently feel that this



A. CCD Reset Pulse

The CCD output mode is reset to a reference voltage when this pulse is high.

B. ϕ Clamp

This pulse overlaps the CCD reset pulse, allowing the low noise Fet to "absorb" the reset noise.

C. CCD Output

With a DC input, the CCD output varies because of the noise on the reset voltage. (Noise exaggerated in diagram.)

D. Double-Correlated Sampler Output

The low noise Fet has absorbed the reset noise, and the charge packets with identical amplitudes are represented as the same output voltage.

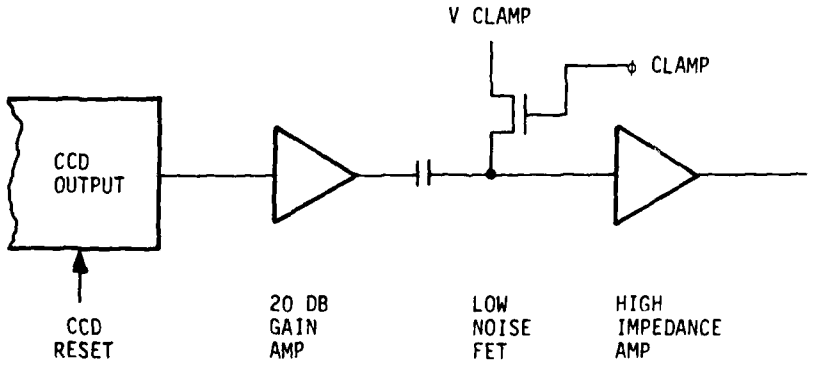
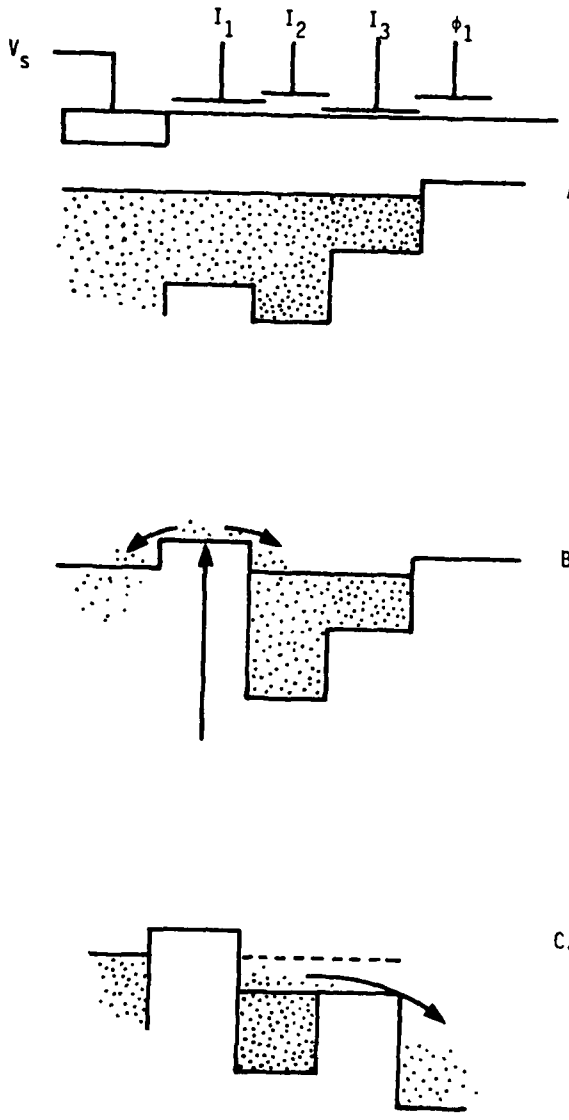


Figure 24. Double-Correlated Sampler Operation

should have been done, since the input sensitivity is approximately 500 micro volts per bit, depending on the output gate setting with a bandwidth of 5 MHz.

The most significant way to measure the input and transfer noise using a CCD fast sampler is to put a DC into the CCD and plot the output of the fast-sampling system on the sensitive scale. Using this technique, it was found that the dominant input noise source is also a sloshing noise created by the movement of charge when the I_1 gate is turned off, as shown in Figure 25. As mentioned regarding reset noise, one would expect that the input noise due to a sloshing phenomenon would be dependent upon the voltage swing of the I_1 gate. Such an experiment was conducted and the results are shown in Figures 26 and 27. These results confirmed the sloshing noise theory in two ways. First, the output of the circuit appears far less noisy for a 5-volt I_1 pulse than for a 15-volt pulse. Second, the DC charge level decreased when using a 5-volt pulse, which would indicate significantly less charge being moved into the input well when the I_1 gate turns off. (The slow, downward shift from start to end on these plots is due to leakage current and will be explained in that section.)

No further noise measurements were taken, since it was found that to make this measurement, it was necessary to cool the A/D converter and that we appear to have reached the noise limit of the A/D converter in its present configuration. It is recommended that in future systems a more temperature-stable A/D converter design be used. RFI shielding of the converter is also highly recommended. We do feel that with this device,



A. With ϕ_1 off and I_1 on, the V_s diffusion acts as a source of charge

B. The I_1 gate is turned off, causing the charge to spill toward both sides of it. The uncertainty of this spilling causes partition or "sloshing" noise

C. The ϕ_1 gate is turned on, allowing signal charge (proportional to I_3-V_s potential) and partitioned charge into the CCD register.

Figure 25. Partition Noise Generation on the Input Circuit

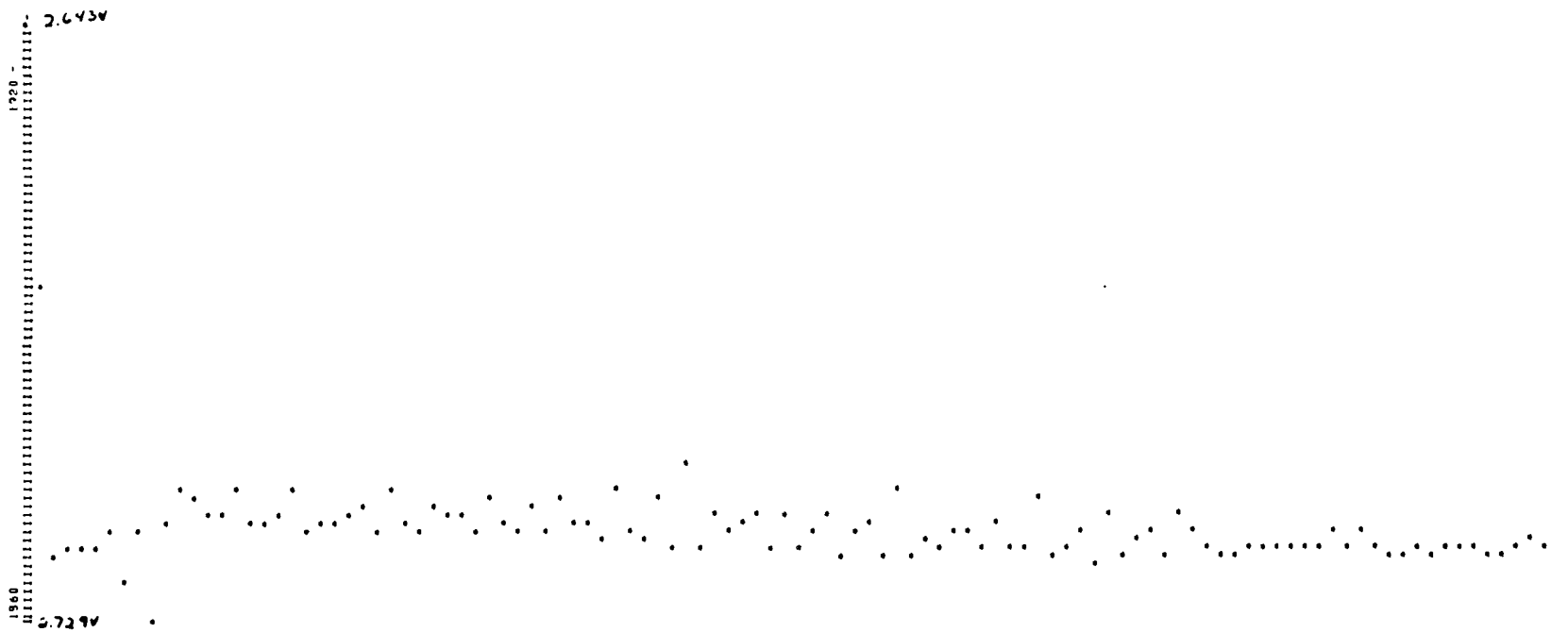


Figure 26. Fast-Sampler Output/DC Input: ϕI_1 Pulsing From 0 to +15V

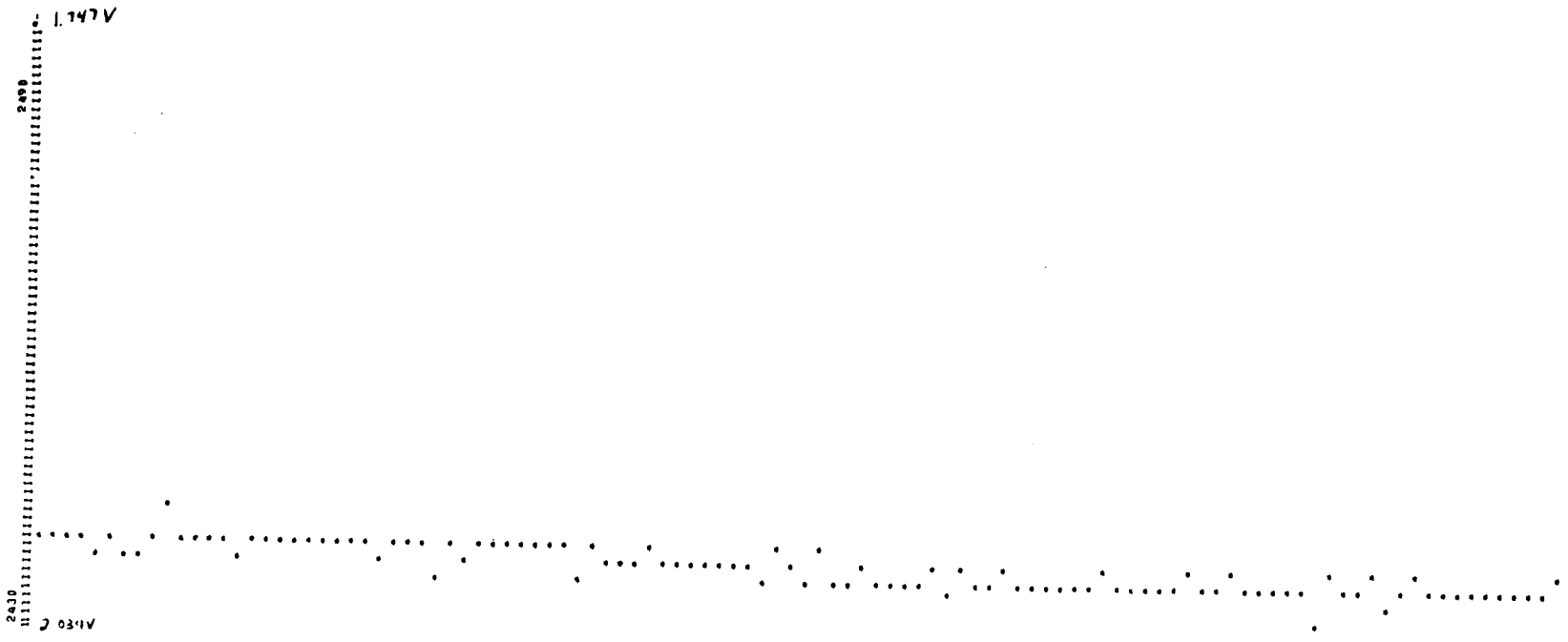


Figure 27. Fast-Sampler Output/DC Input: ϕI_1 Pulsing From 0 to +5V

we have reduced the noise of the CCD and the associated circuitry to that required for 12-bit resolution and that a simple repackaging and DC compensation will produce a fully operational 12-bit, 10 MHz system.

It is difficult to demonstrate the full dynamic range of the CCD sampler on any single display, so to demonstrate its capabilities two single cycle sine waves two orders of magnitude different in amplitude were sampled, stored, and displayed. Figure 28 shows a 1.9 μsec 33 mV peak-to-peak sine wave displayed at one digit/line with an offset of 3120 counts. One digit/line corresponds to an output sensitivity of 1.22 mV/line and input sensitivity of 500 μV/line. The plotter was then set to display the entire A/D output for full scale which corresponds to an output sensitivity of 70.4 mV/line. Figure 29 is a plot of this same 30 mV waveform displayed on this reduced sensitivity scale. The top of the waveform appears only because the DC level of the waveform was offset toward the top of the particular 70 mV window in which it fell. The input amplitude and offset were then changed and a new sample stored. A 4V peak-to-peak sine wave on the reduced sensitivity scale is shown in Figure 30.

LINEARITY MEASUREMENTS

High-speed sampling using CCDs requires linearity of the CCD and its associated input and output circuitry over the operating range of interest for both AC and DC signals. Figure 31 is a plot of the output code vs input voltage of the high speed sampler with a DC input. For this measurement the gain of the post CCD amplifier was reduced to bring the entire output swing of the CCD on scale. It can be seen from this plot that the CCD is extremely nonlinear under near empty and near full operating

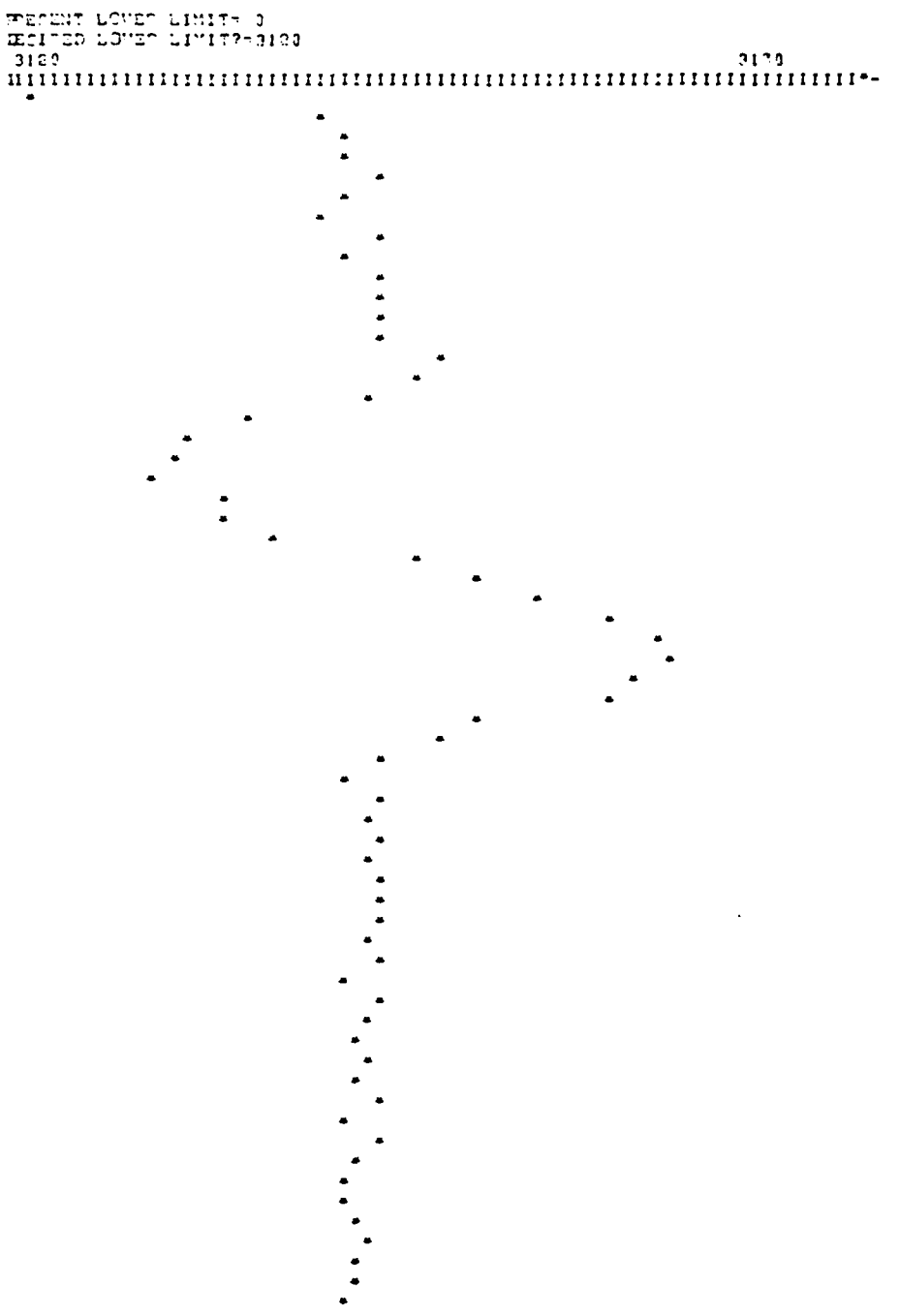


Figure 28. A 1.9 μsec 33 mV Peak-to-Peak Sine Wave

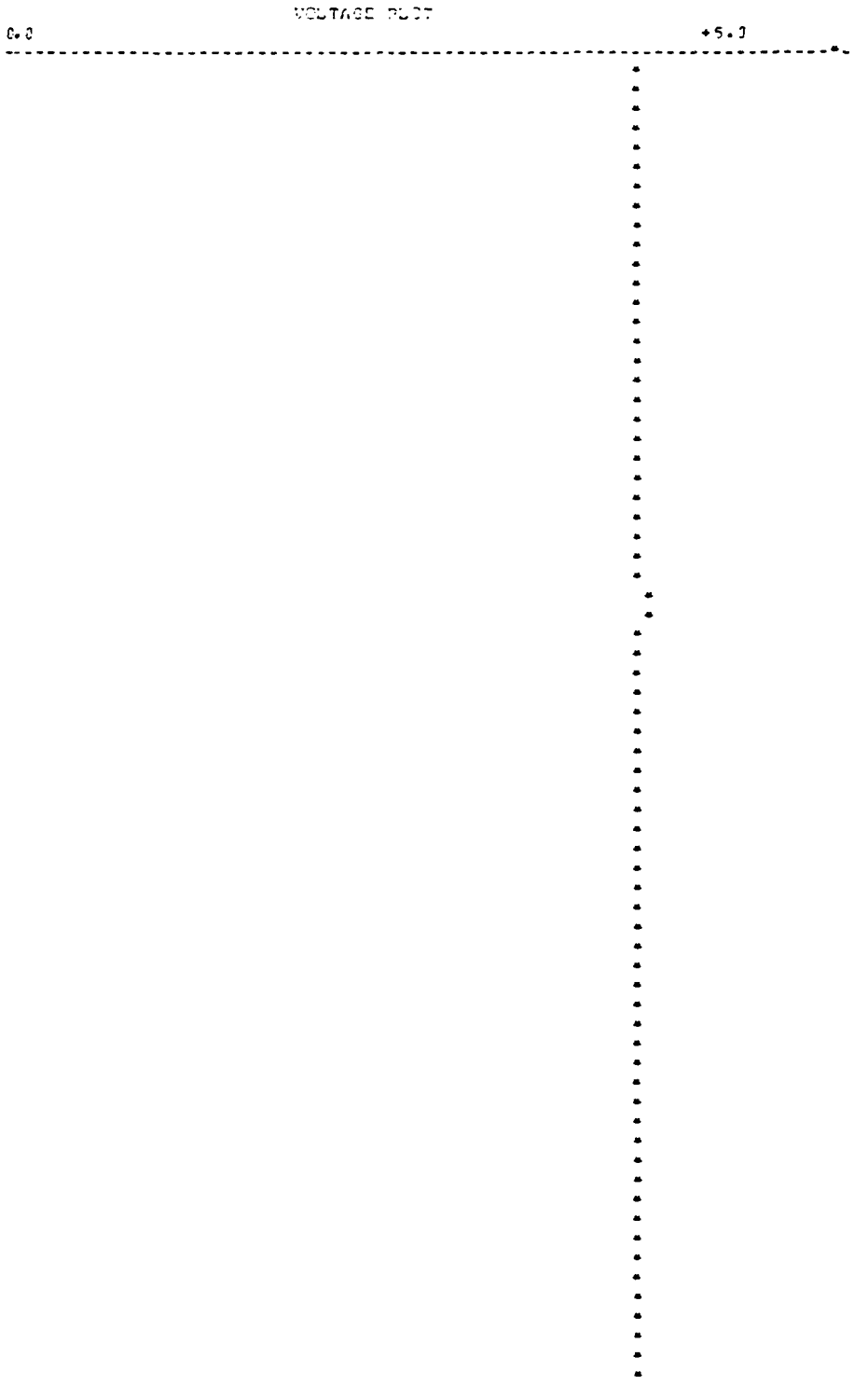


Figure 29. A Plot of a 30 mV Waveform

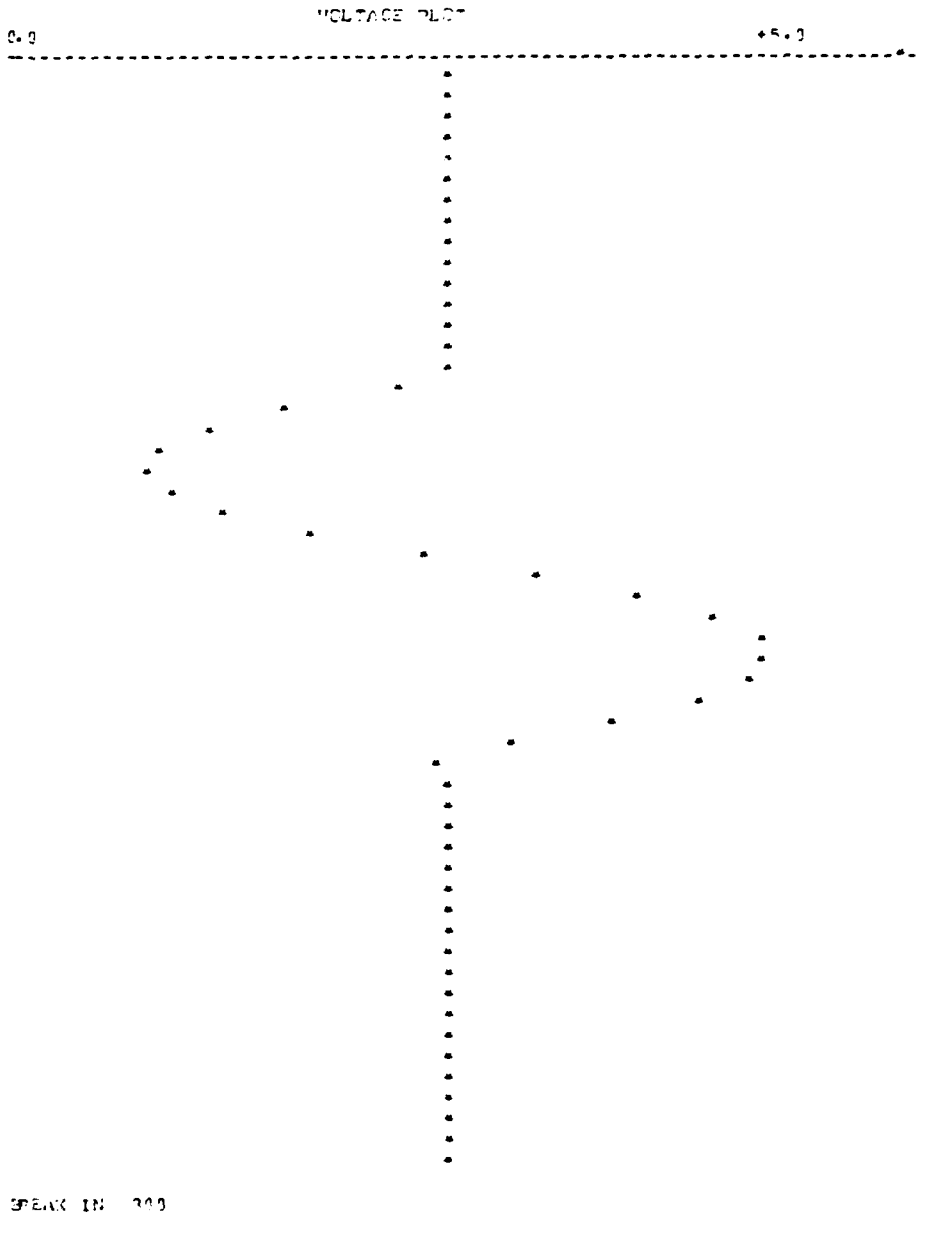


Figure 30. A 4V Peak-to-Peak Sine Wave, 10 MHz Sampling Rate

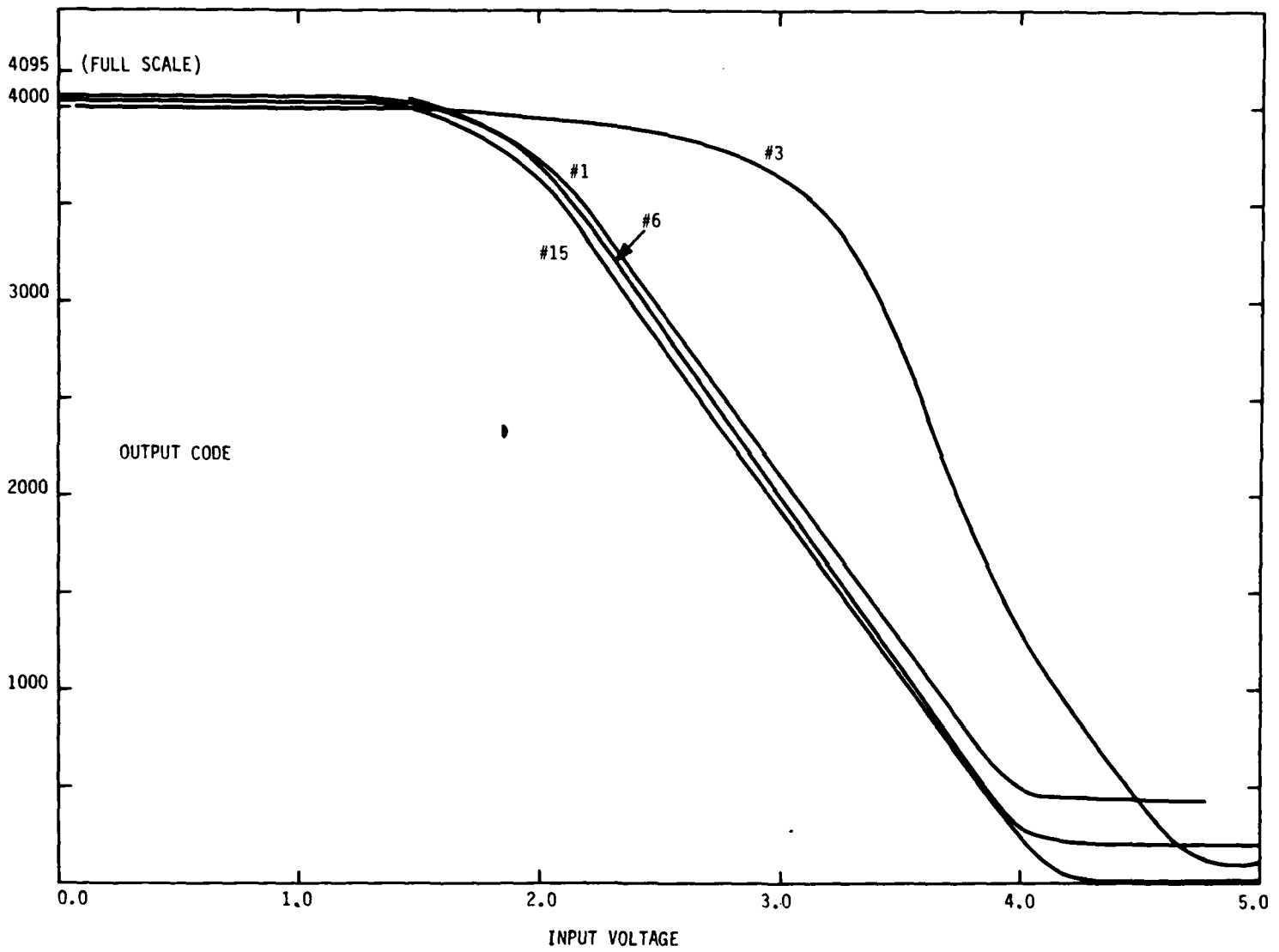


Figure 31. DC Input Linearity Test

conditions, but it appears very linear over a significant portion of its operating range. It is also obvious that device #3 is defective.

A similar test was performed to measure dynamic performance using a 0 to +5V ramp function which was synced with the start sample pulse. The ramp length was set to be just less than the sample interval (12.5 μsec). The results of this test are shown in Figure 32. It can be seen that this data is very similar to the DC data with nonlinearities near empty and full well and a highly linear region between these two extremes.

To get a more accurate measure of linearity over the linear portion of the curve, two end points were selected and a linear curve of the form

$$V_{out} = V_{offset} - K V_{in}$$

was constructed, where V_{offset} is the output voltage with $V_{in} = 0$, and K is the system gain. This process was repeated for each set of DC and dynamic device characteristics. (Device #3 was excluded because it is defective.) Figure 33 shows the error between actual measured data and the straight line approximation for input voltage range of 2.2 to 3.8. The most obvious thing about this plot is that the dynamic tests demonstrate a definite pattern while the DC results have a scatter larger than the error actually measured. The DC error was found to be due to the temperature instability of the output amplifier (not the CCD). During the time the input voltage was being changed, the DC operating point was moving, causing measurement errors greater than the DC nonlinearities. Obviously, the output circuit was temperature stable for the 6.3 milliseconds required to read out the dynamic data.

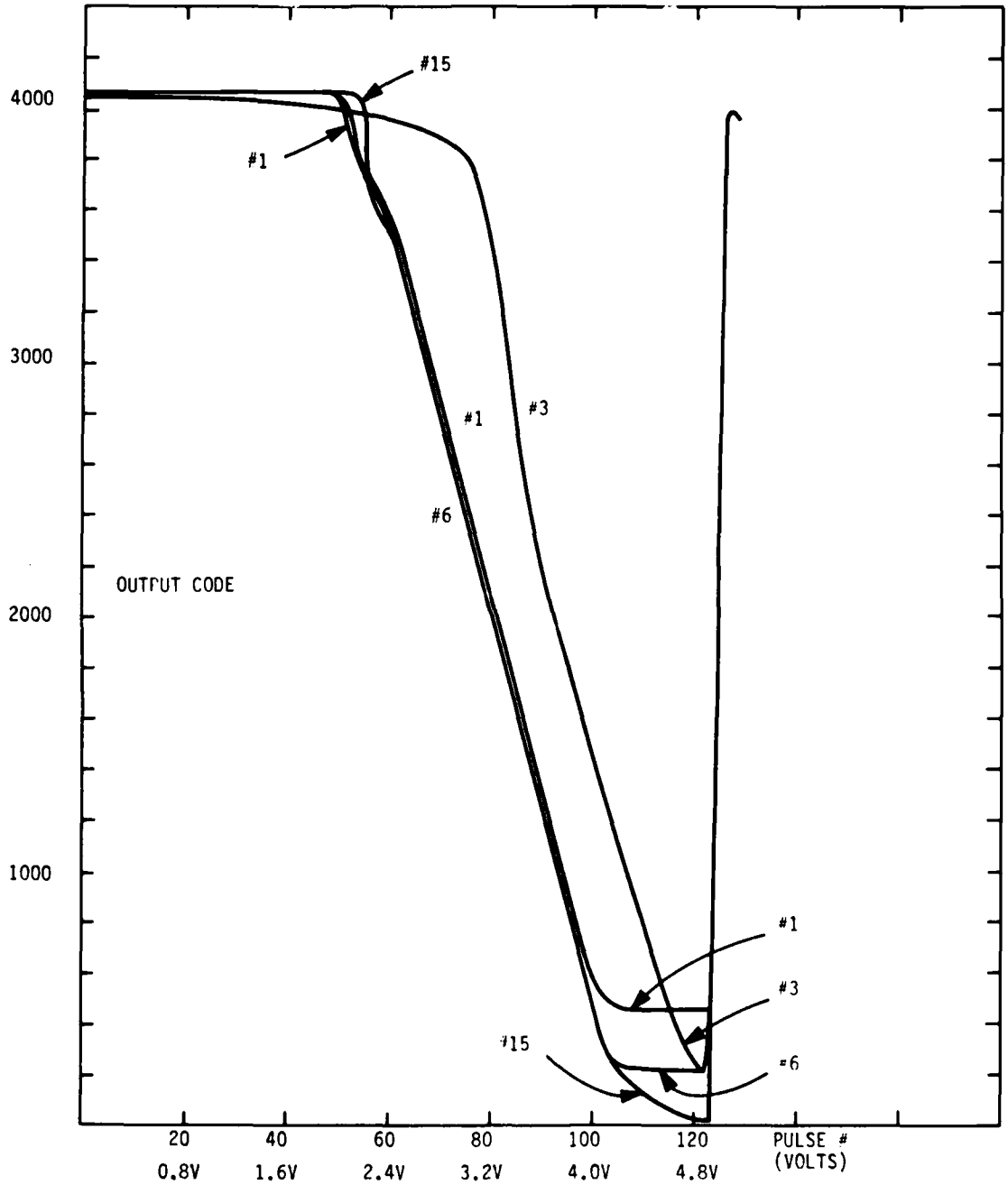


Figure 32. Ramp Input Linearity Test

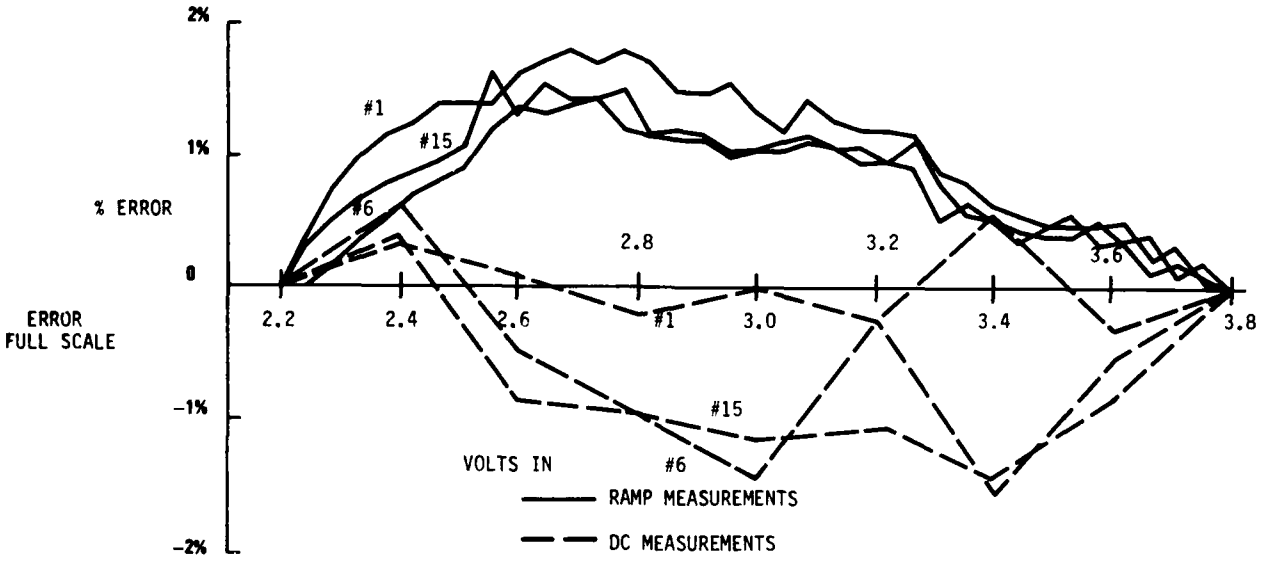


Figure 33. Closeness of Fit to a Straight Line (2.2-3.8 *Volt Ramp* and DC Inputs)

Looking at the dynamic data it appears that the most nonlinear part of the curve occurs between 2.2 and 2.6V at the input of the device. This should mean that by using only that part of the curve between 2.6 and 3.8V, even better linearity characteristics should be obtained. Figure 34 shows the closeness of fit to a straight line in that interval. The nonlinearity error has been reduced by a factor of four to five as a percentage of full scale. Actually, the linearity is probably significantly better than that shown in Figure 34, since the noise of the ramp generator caused significant fluctuations in the measured values, and the ramp generator linearity is specified to only 1.0% full scale, which was 4 volts in this case.

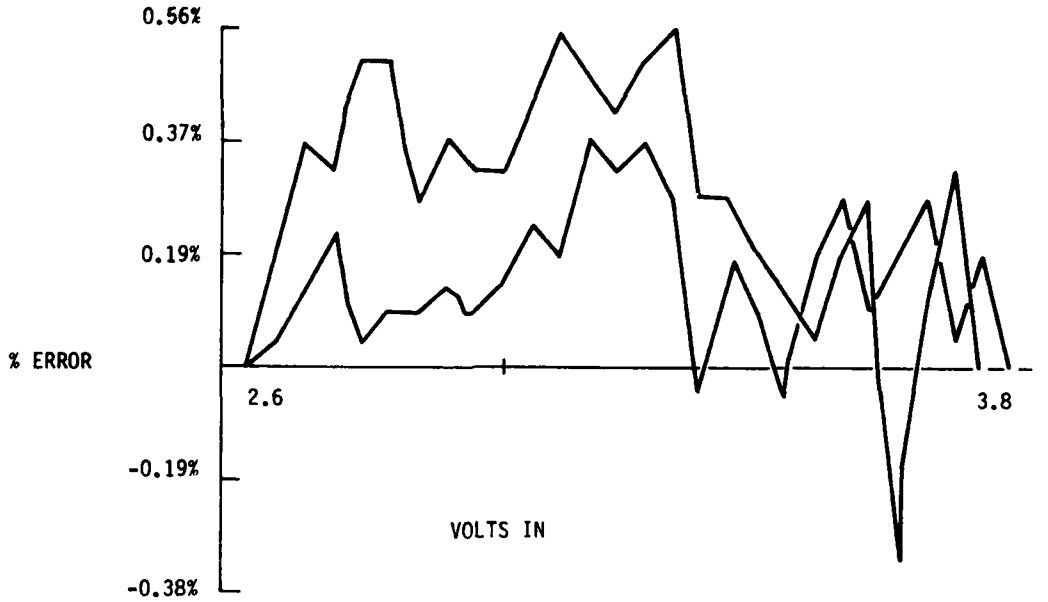


Figure 34. Closeness of Fit to a Straight Line
(2.6-3.8 Volt Ramp Inputs)

From these results it appears that the linearity of the CCD can be improved by using operating regions near full well and that if greater linearity is needed, the operating range can be reduced until the desired linearity is achieved. Reduction of the operating region will, however, reduce dynamic range somewhat. In our example, linearity was increased by a factor of four (12 dB) with a reduction in operating range of only a factor of .75, a reduction in dynamic range of only 2.5 dB. For applications where extreme linearity is needed, the CCD response can be stored in a look-up table and the nonlinearity factored out to achieve near perfect linearity.

LEAKAGE MEASUREMENTS

Leakage current is the term used to describe the thermal generation of hole-electron pairs in and near the CCD well. The hole half of this pair is accelerated toward the substrate where it appears as a majority carrier substrate current. The electron is forced into the CCD well where it is indistinguishable from the signal charge.

In applications such as analog delay lines, where each packet of charge spends the same amount of time at all storage locations as it passes through, the leakage current will appear as a uniform background charge. However, in the fast-sampling application, some charge packets remain in the CCD much longer than others because of the fast input and slow output clock rates. As shown in Figure 35, the effect of this is to cause a stairstep in the output voltage starting with the first sample, where the size of each step is proportional to the amount of leakage in the well where that charge packet was located at the end of the sample interval. This assumes that the leakage charge collected during the sampling interval is negligible with respect to the charge collected during the readout interval. This is a safe assumption since the read-in rate is 500 times the read-out rate.

CCD leakage current is measured in the fast-samping system by turning off the input circuit and adjusting the output DC to be on scale at the A to D converter. Figure 36 shows the output voltage for 128 samples on three devices at room temperature. Figures 37 and 38 are plots made under similar conditions with the device cooled to 0°C and heated to 100°C. The

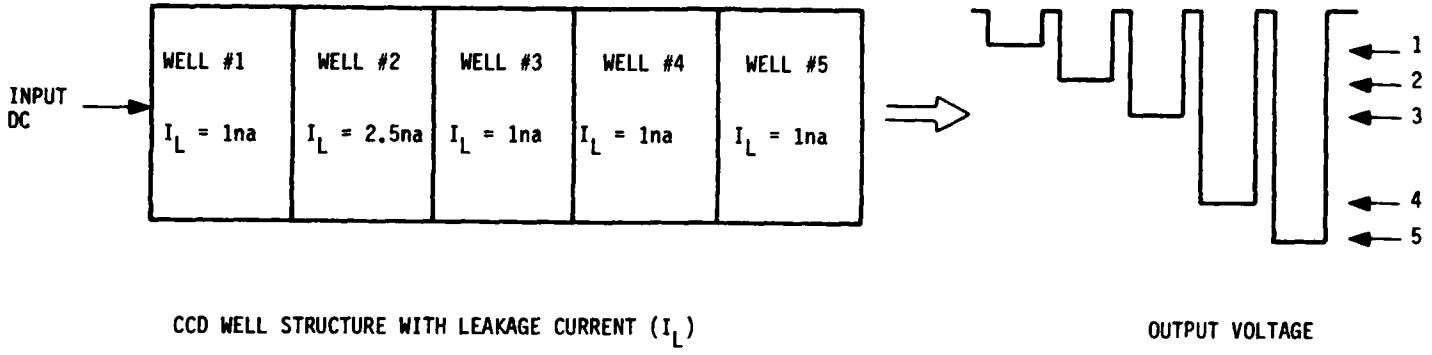


Figure 35. The Effect of CCD Leakage Current on the Fast-Sampler System

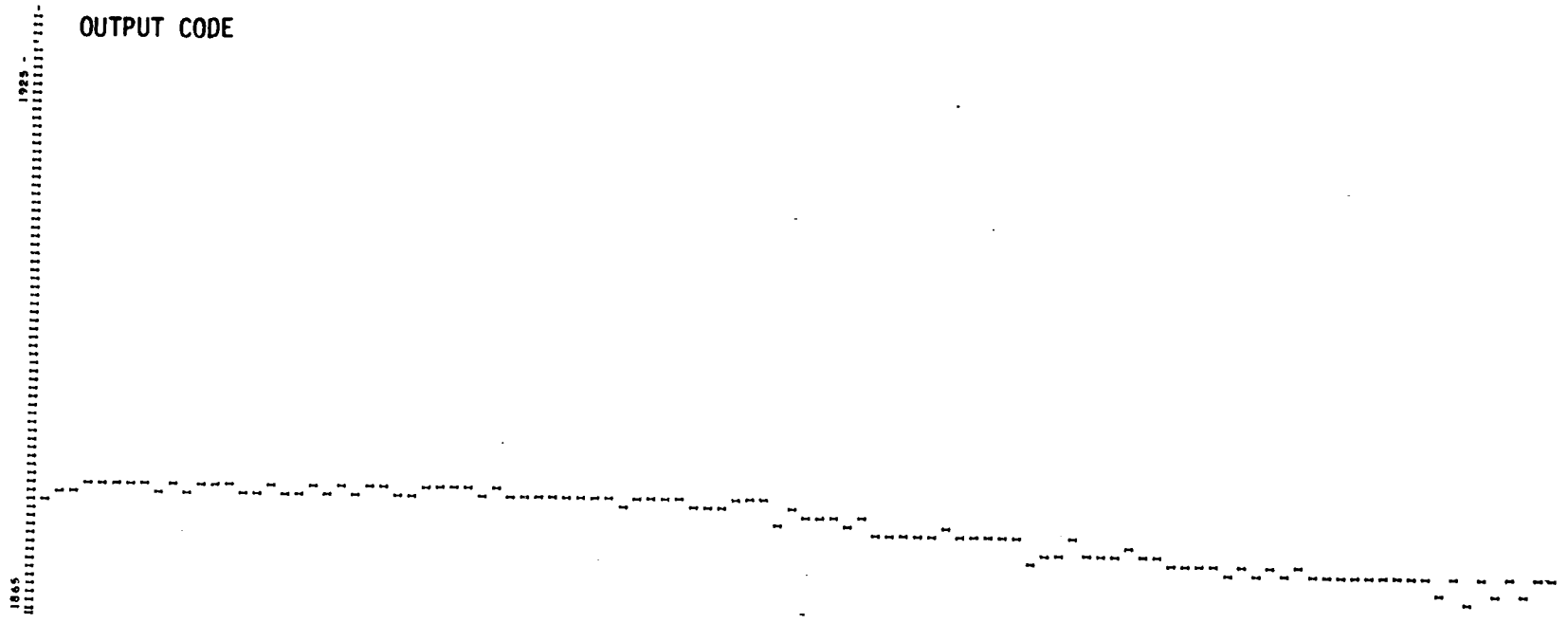


Figure 36a. Room Temperature Output, Input Turned Off: Device #1

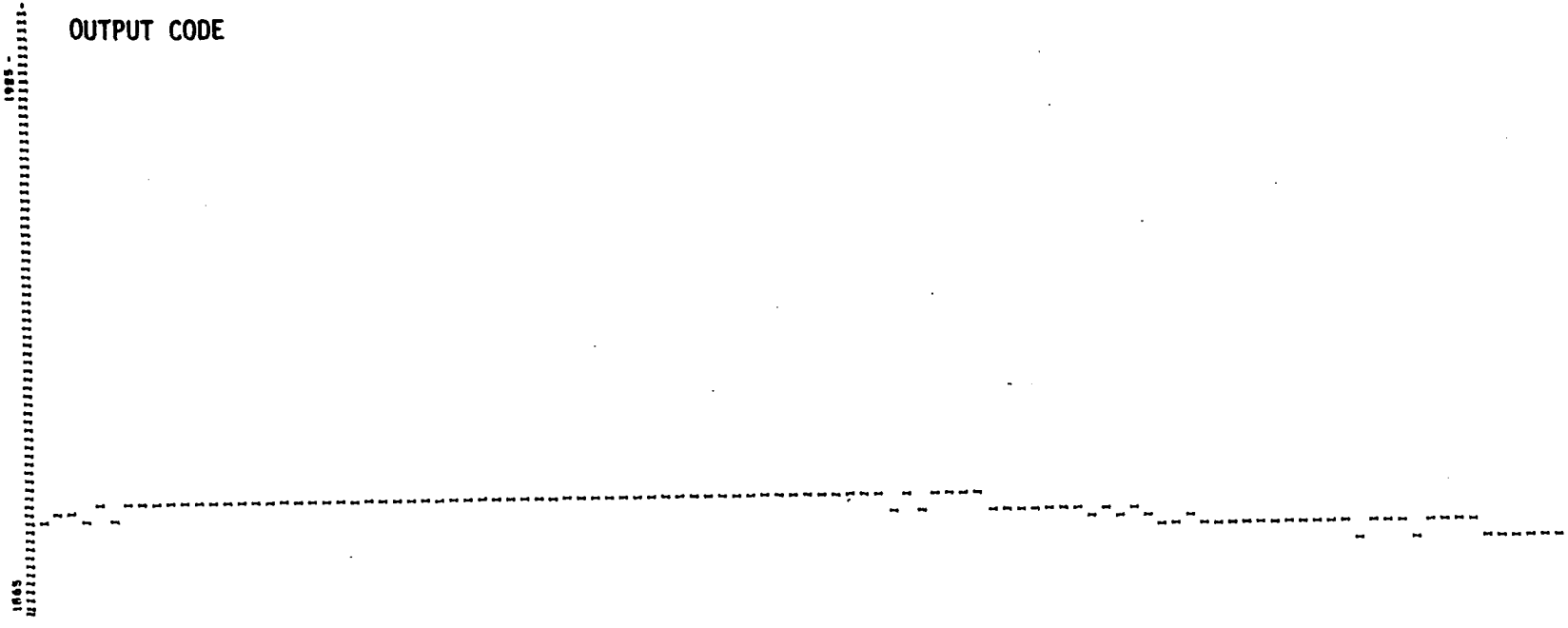


Figure 36b. Room Temperature Output, Input Turned Off: Device #9

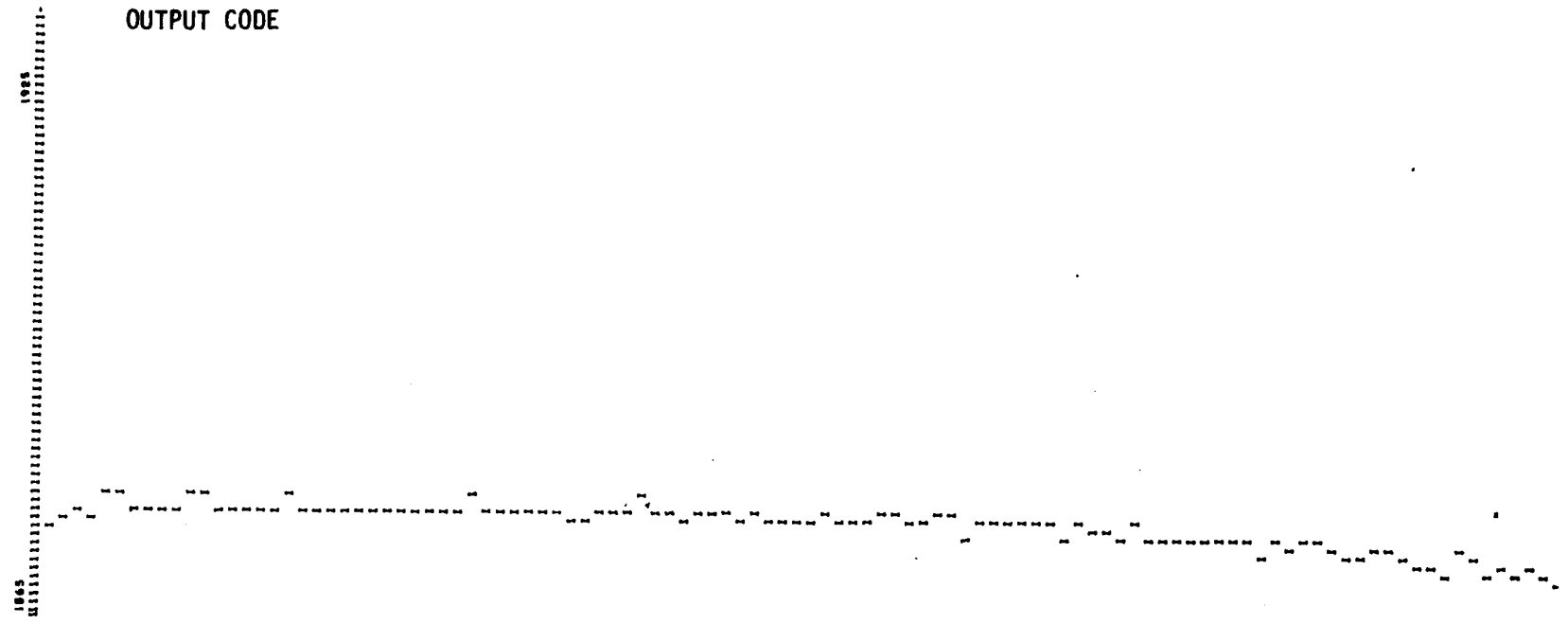


Figure 36c. Room Temperature Output, Input Turned Off: Device #15

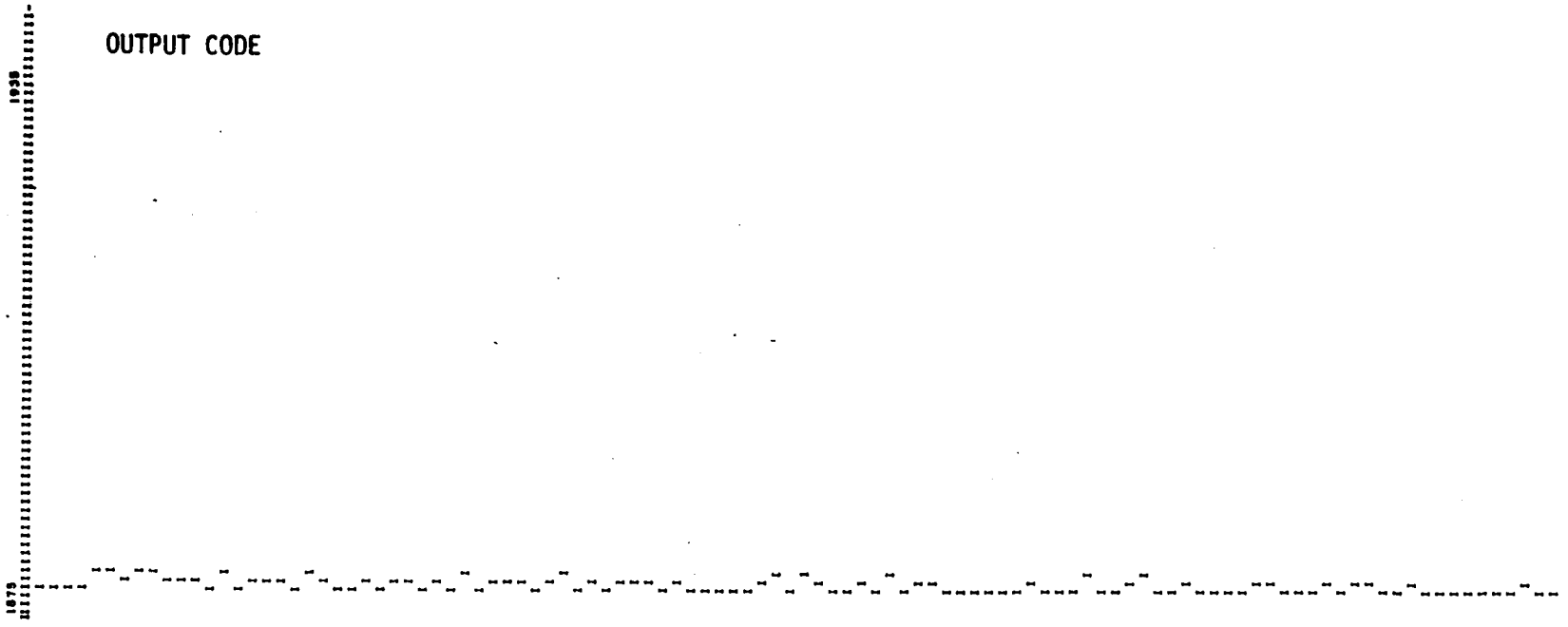


Figure 37a. Output at 0°C, Input Turned Off: Device #1

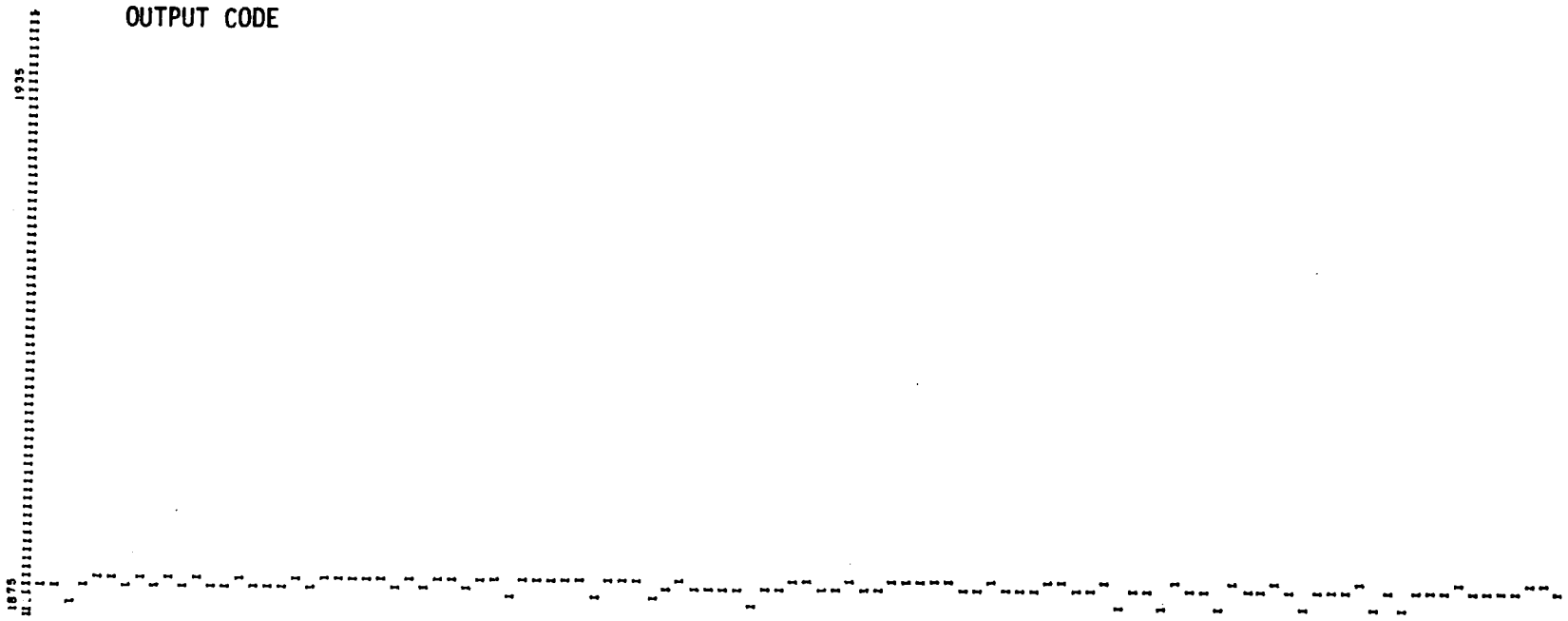


Figure 37b. Output at 0°C, Input Turned Off: Device #9

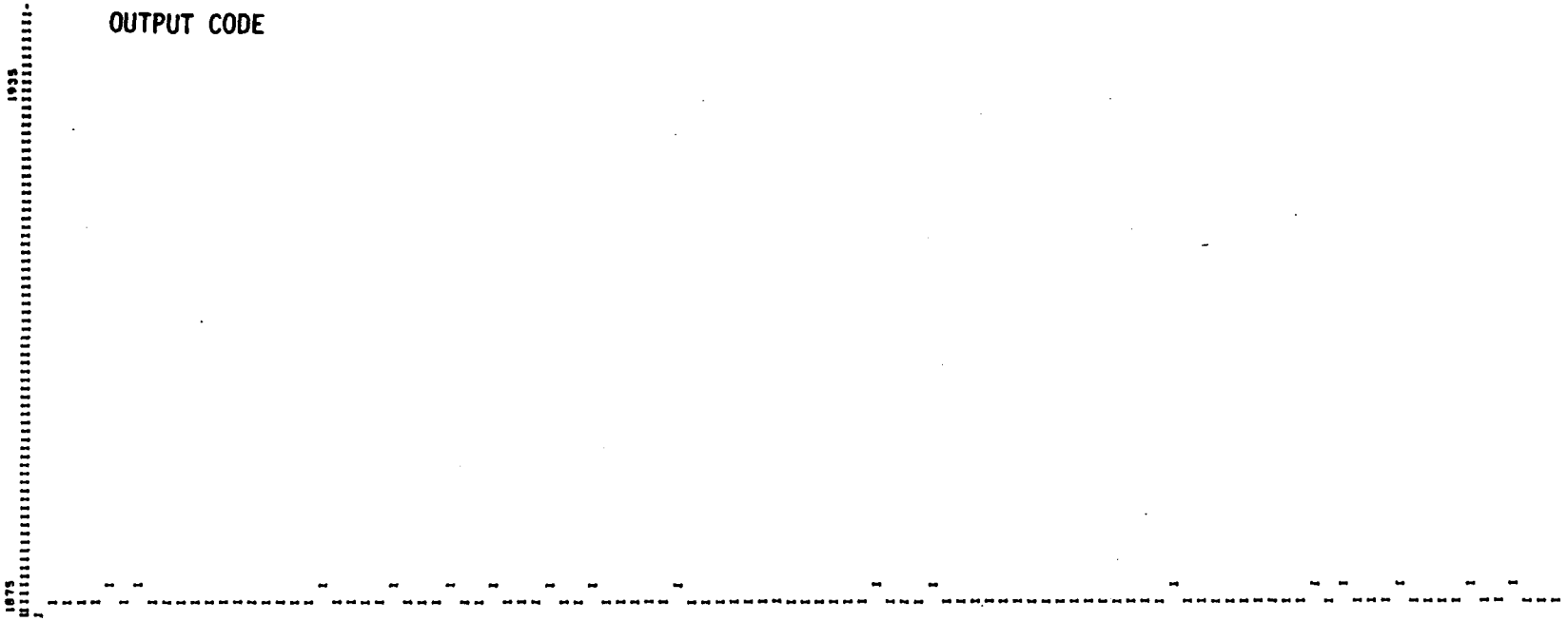


Figure 37c. Output at 0°C, Input Turned Off: Device #15

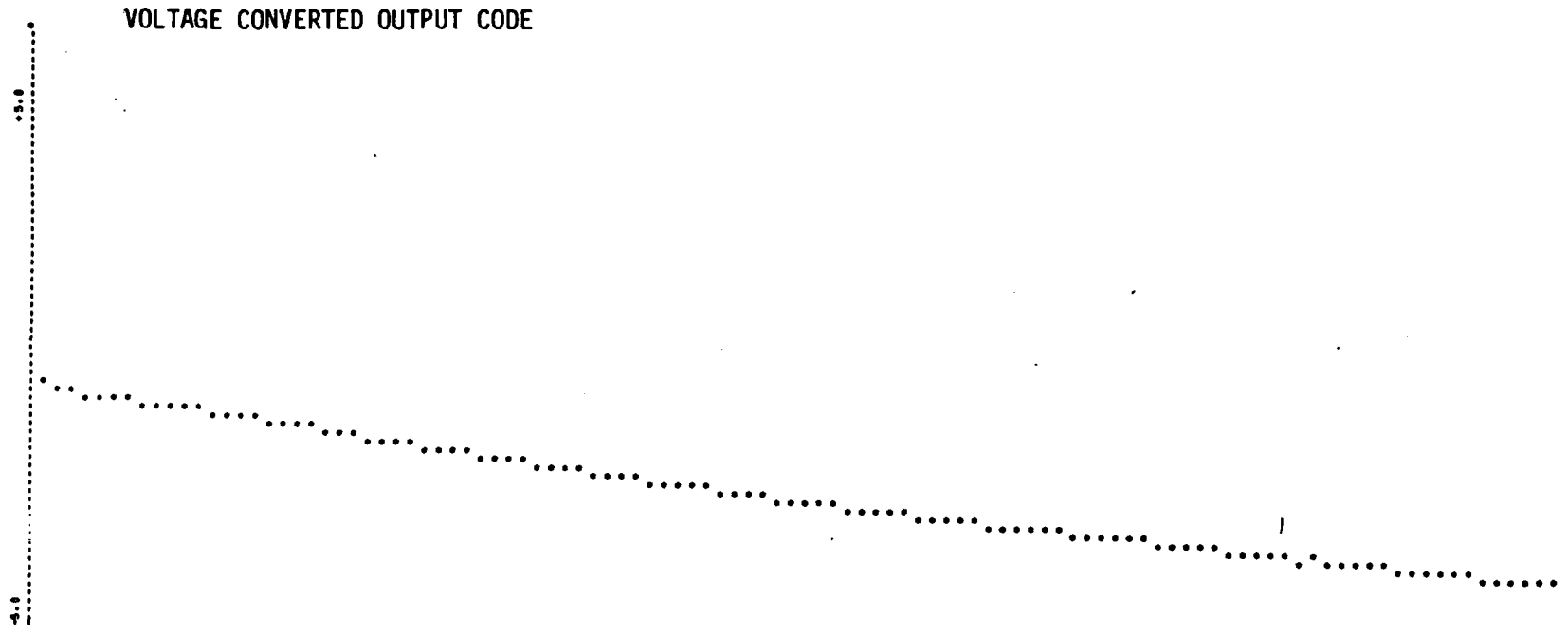


Figure 38a. Output at 100°C, Input Turned Off: Device #1

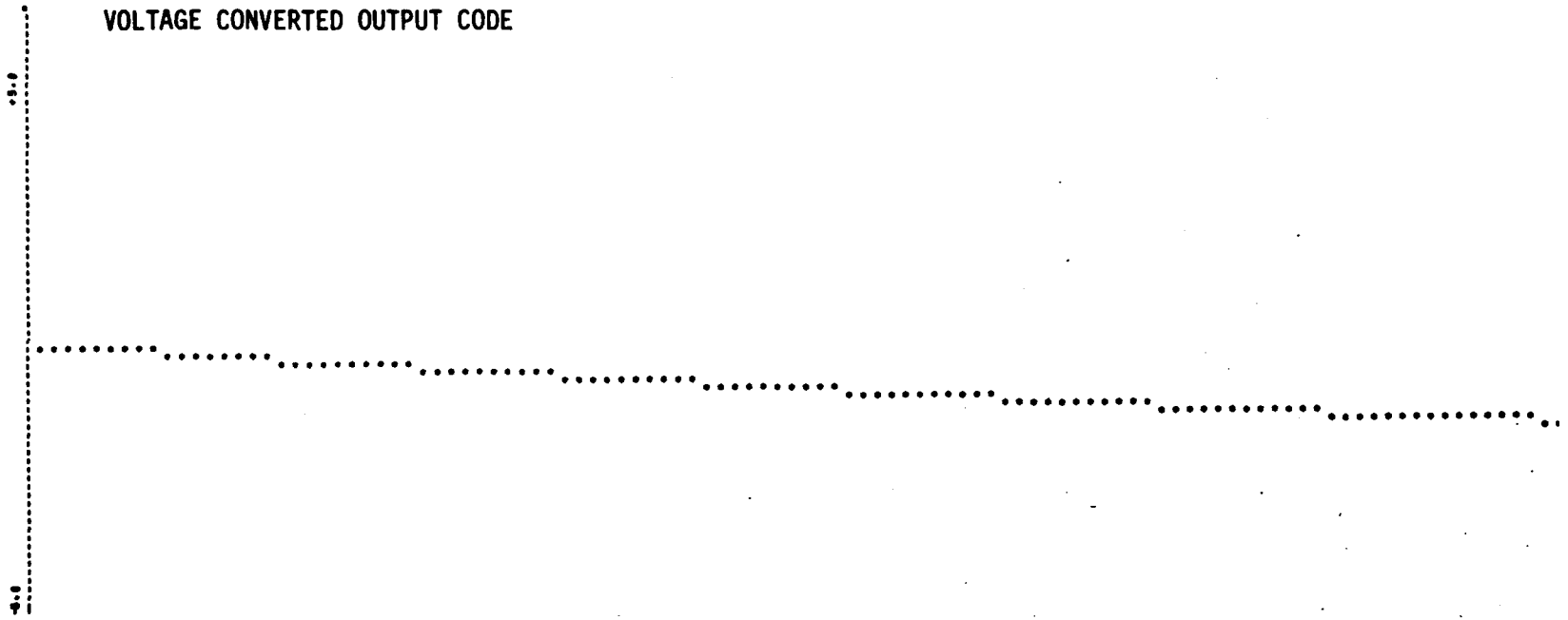


Figure 38b. Output at 100°C, Input Turned Off: Device #9

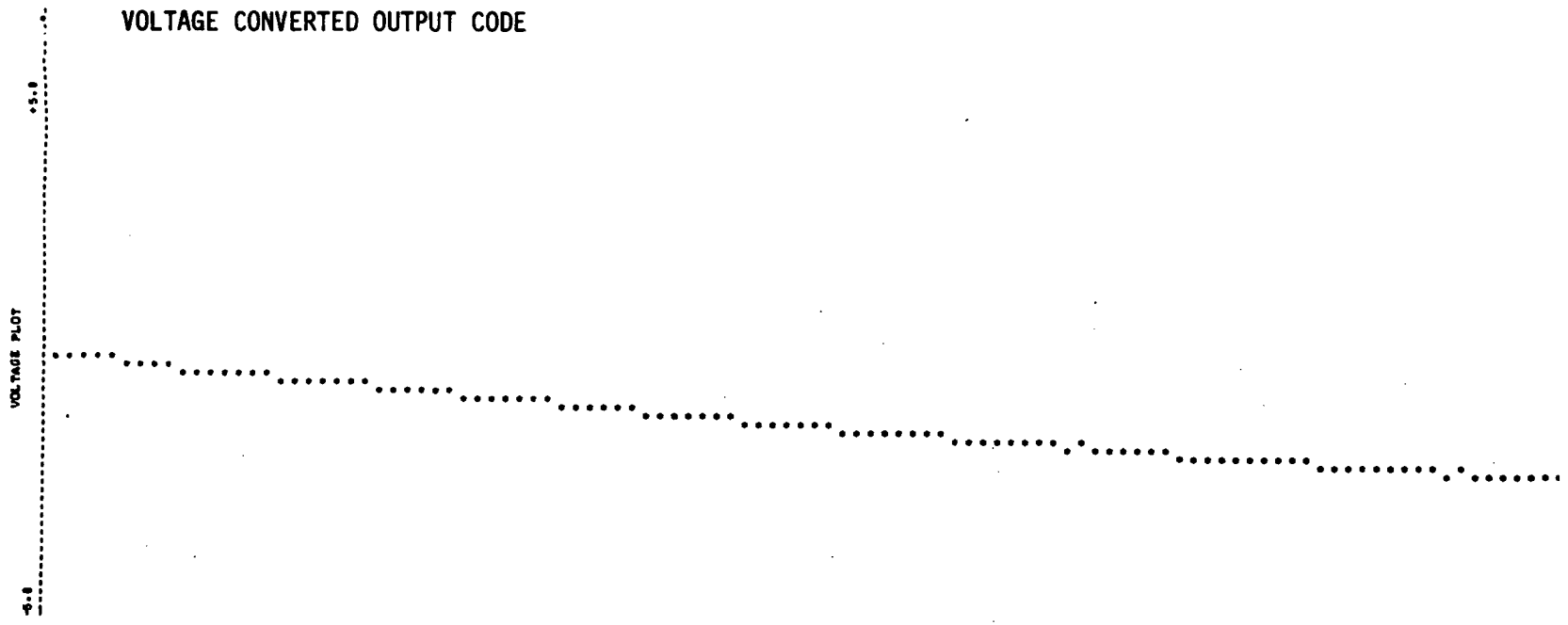


Figure 38c. Output at 100°C, Input Turned Off: Device #15

100°C plots had to be made on the less sensitive scale because the leakage charge in this case was a significant portion of the CCD well size. It is apparent from these results that device #1 has nearly twice as much leakage current as devices #9 and #15. There is also an apparent disparity between the high temperature and room temperature results in that at 100°C, the wells near the output end of the device appear to leak more than those near the input end, causing a convex curve, while at room temperature the wells near the output appear to leak less, causing a concave shape. The reason for this disparity is that the assumption of a uniform leakage current independent of the amount of charge in the well is incorrect. In actual practice, as a well fills with charge, some of the generation-recombination centers which cause leakage are filled, and therefore, the leakage rate drops. This effect is observed only when a significant portion of the well is filled, as is the case at 100°C. The concave shape at room temperature is also somewhat suspect and may be due to slight variations in the post-CCD amp and double-correlated sampling circuitry.

In our existing fast-sampling system, the CCD read-out rate is limited by the cycle time of the microcomputer system and not by the CCD or the A/D converter. The cycle time for data acquisition is approximately 40 microseconds, while the A/D conversion time is approximately 10 microseconds. Therefore, by reducing the cycle time of the digital interface to 10 μsec, the read-out rate can be increases by a factor of four, reducing the leakage by a factor of four. This factor of four reduction is all that is required to achieve full 12-bit performance at room temperature for most of our existing devices.

Although in our present system there is observable leakage current even at room temperature, it should be pointed out that this does not preclude use of the device to full 12-bit accuracy. The leakage charge present in each well of the CCD can be measured during a calibration cycle and stored. When a data sample is taken, the leakage value associated with each sample can be removed to compensate for this error, restoring the true input value at each location. There are limitations on the temperature range over which this technique can be used, since the leakage current has a shot noise associated with it. For the 2178 device, this shot noise should not be a problem until the well is near 1/4 full of charge, which is approximately the leakage which occurred in device #15 at 100°C. The CCD fast sampler should therefore be operable to temperatures up to 100°C if a DC calibration is performed before sampling. This calibration feature can easily be built into the hardware.

As a further measure of the leakage characteristics of the 2178, the devices were operated at a clock rate of 250 Hz. Since a well fills up to approximately .25% of full well at 25 kHz, the wells should fill to 25% at 250 Hz. Unfortunately, the computer-sampler interface had a timing problem at this low clock rate and would not operate. Therefore, the CCD was operated in the shift-out mode continuously at 250 Hz and the CCD output read directly. Figure 39 shows a 30-Hz triangle wave at the output of the device. Figure 40 shows the output of the device with the input turned off. Because the full well output of the CCD is approximately two volts, the 500 millivolt output signal indicates that the leakage is indeed 25% full well. Since in

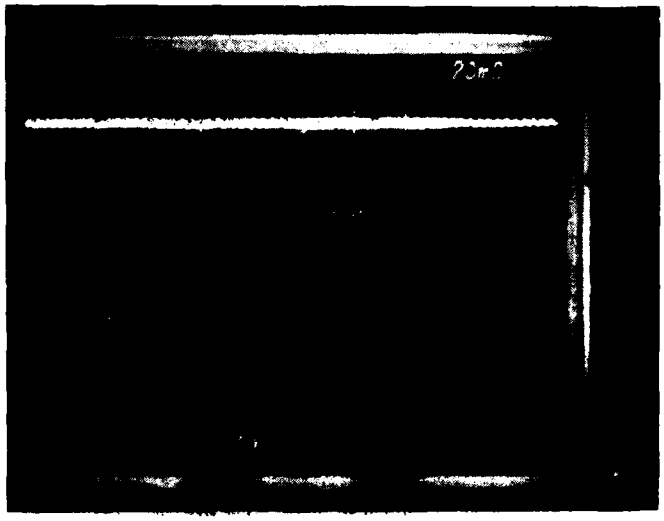


Figure 39. CCD Output: 30-Hz Triangle Wave
at a 250-Hz Clock Rate, Room Temperature

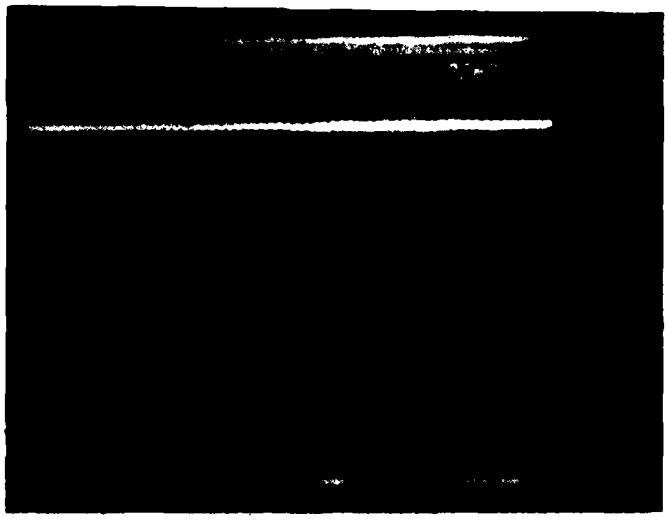


Figure 40. CCD Output: Input Turned Off
250-Hz Clock, Room Temperature

normal operation the lower 25% of the well is not used because of its non-linear characteristics, this would indicate that the device should be functional at a 250-Hz clock rate at room temperature.

SPEED AND TRANSFER EFFICIENCY MEASUREMENTS

The objective of this program was to demonstrate the feasibility of 10-MHz sampling with 12-bit accuracy using CCDs. It appears in retrospect that these objectives were perhaps not aggressive enough and that still greater speeds are attainable with the 2178 CCD. At the present time the fast sampler has been operated at sampling rates in excess of 12 MHz with no significant reduction in device performance. Unfortunately, because the goal for this program was only 10 MHz the clock generating logic and drivers will not operate beyond this frequency. Figure 41 shows a single cycle of a 200-kHz triangle wave sampled at 6 MHz, and Figure 42 shows the same input waveform sampled at 12 MHz. The 12-MHz sample shows two glitches which were generated when the clocking logic skipped a count; however, no CCD malfunction occurred. (We did, however, forget to blow the fan on the A/D converter; hence, the large noise level).

When operating CCDs at high frequencies, one of the main parameters of interest is transfer efficiency--the ability of the device to move a charge pocket from one well to the next without loss. One of the best ways to measure transfer efficiency is to apply a square wave or step function and observe the charge left behind from the first well erronously measured in the second. Figure 43 shows the response of the fast sampler to a large

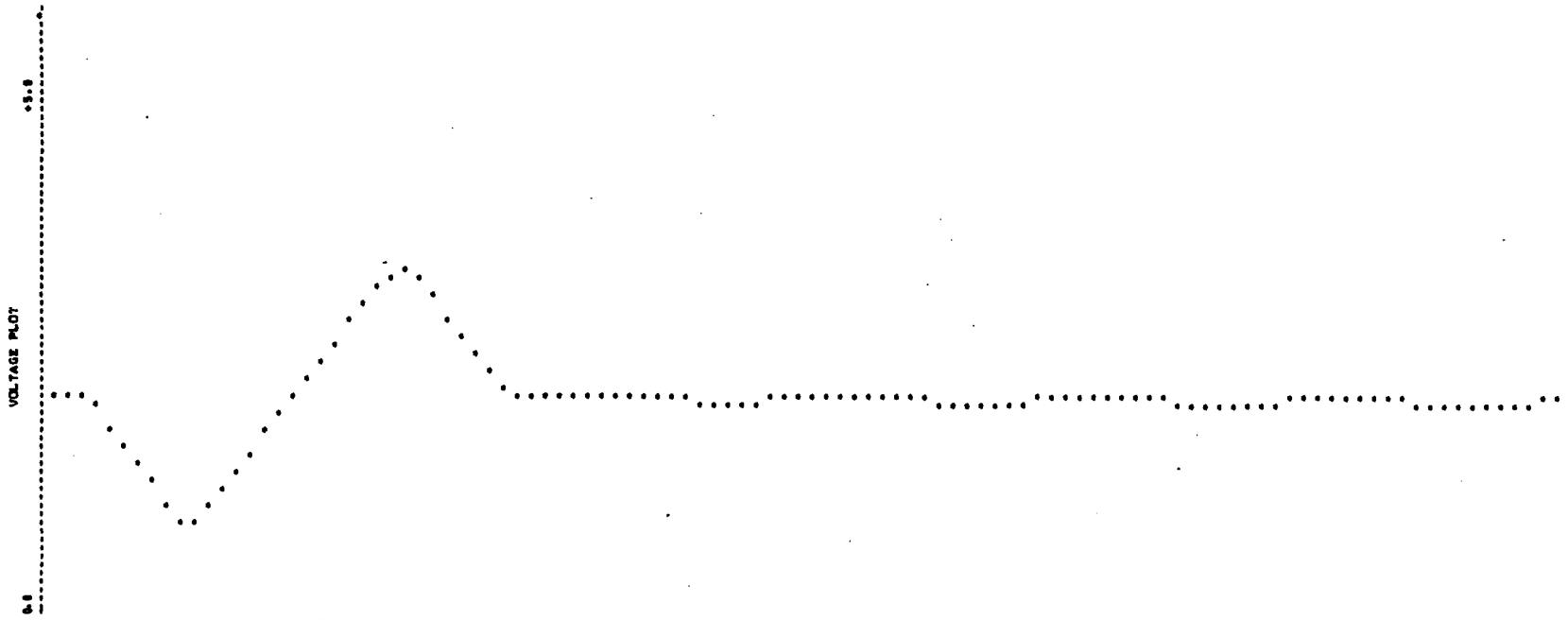


Figure 41. 200 kHz (5.0 μsec) Triangle Wave Sampled at 6 MHz

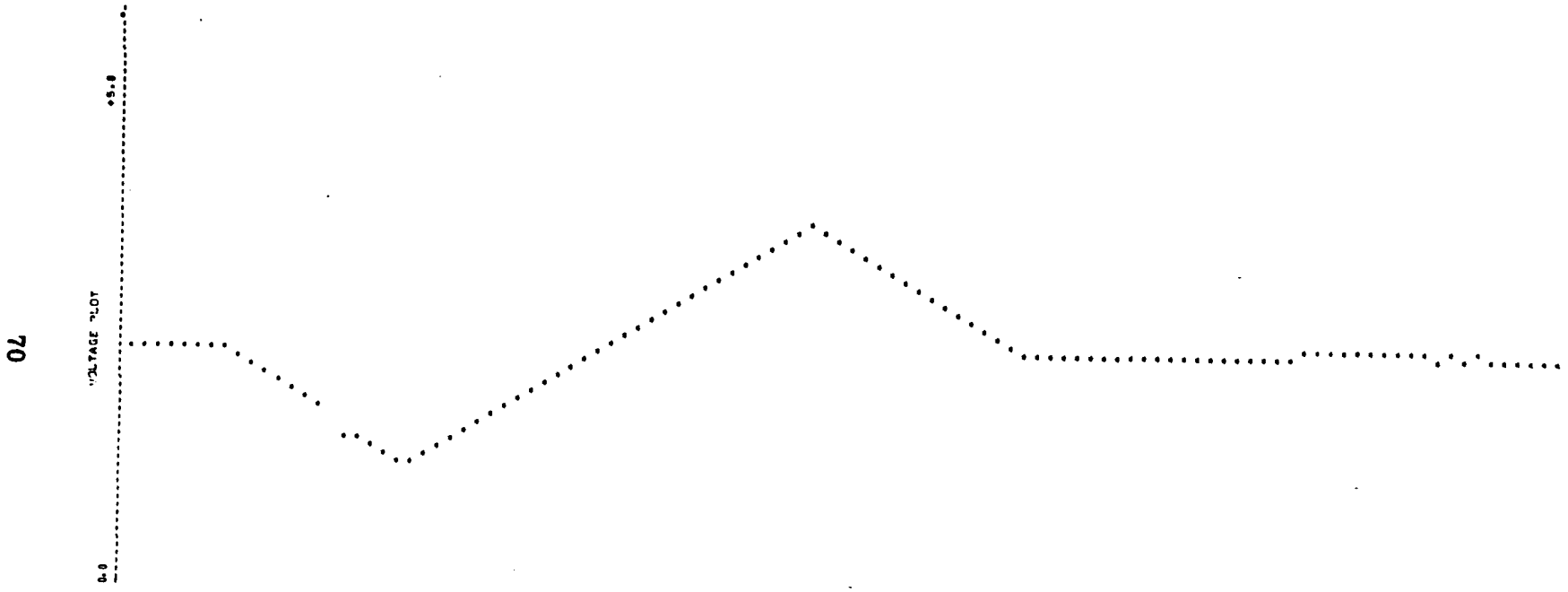


Figure 42. 200 kHz (5.0 μsec) Triangle Wave Sampled at 12 MHz

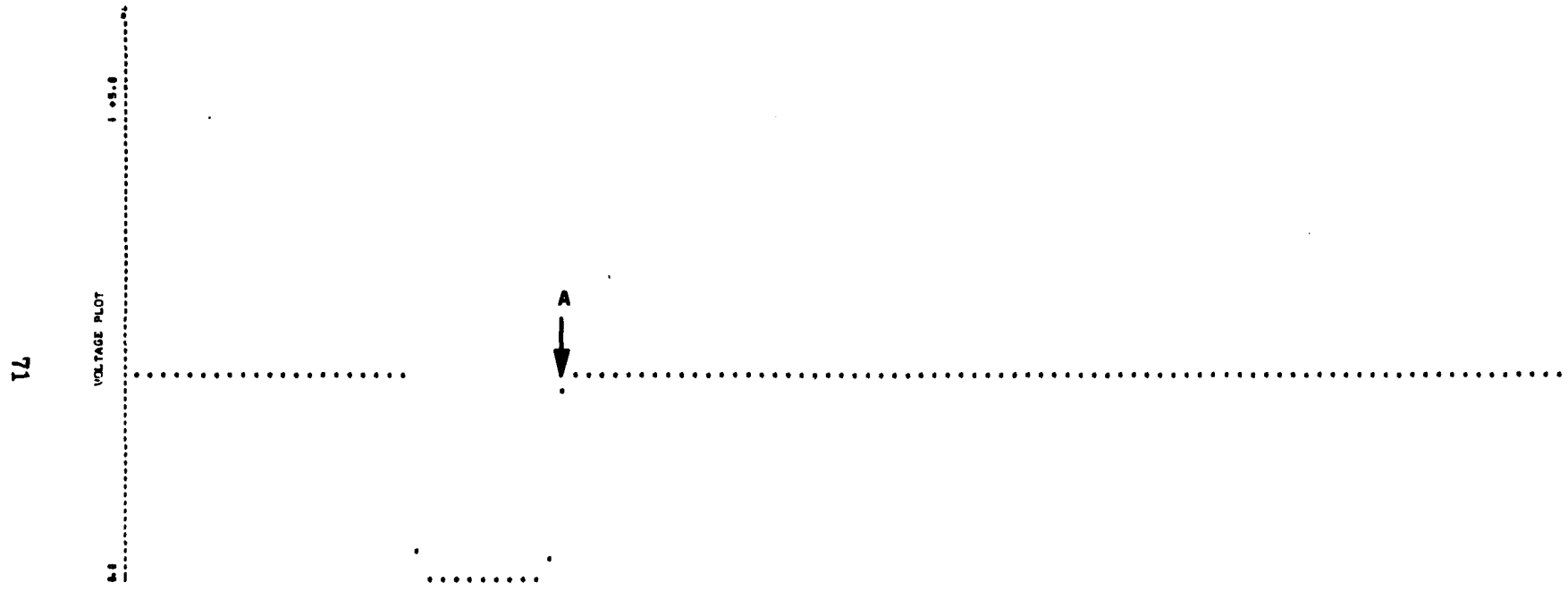


Figure 43. Large Signal Square Wave Response at 10 MHz Clock Rate

value square wave. The leading and trailing edges appear to have some rounding, but this is probably due to the rise and fall times of the input pulse. The true measure of transfer efficiency is the small signal occurring after the pulse, labeled A, which is two divisions in amplitude. This is about 8% of the square wave height and about 3% of the charge in the well, and it indicates a transfer efficiency of .9999%. This transfer efficiency should be more than adequate for the ATE application unless extremely accurate measures of high amplitude, rapidly changing waveforms are needed. This should not occur unless the device is used to sample waveforms at frequencies near its high frequency limit,--that is, half the clock rate. Figure 44 shows the results of a similar test using a 50-millivolt input pulse. Unfortunately, the signal source in this case was quite noisy; however, the square wave response of the device appears quite good.

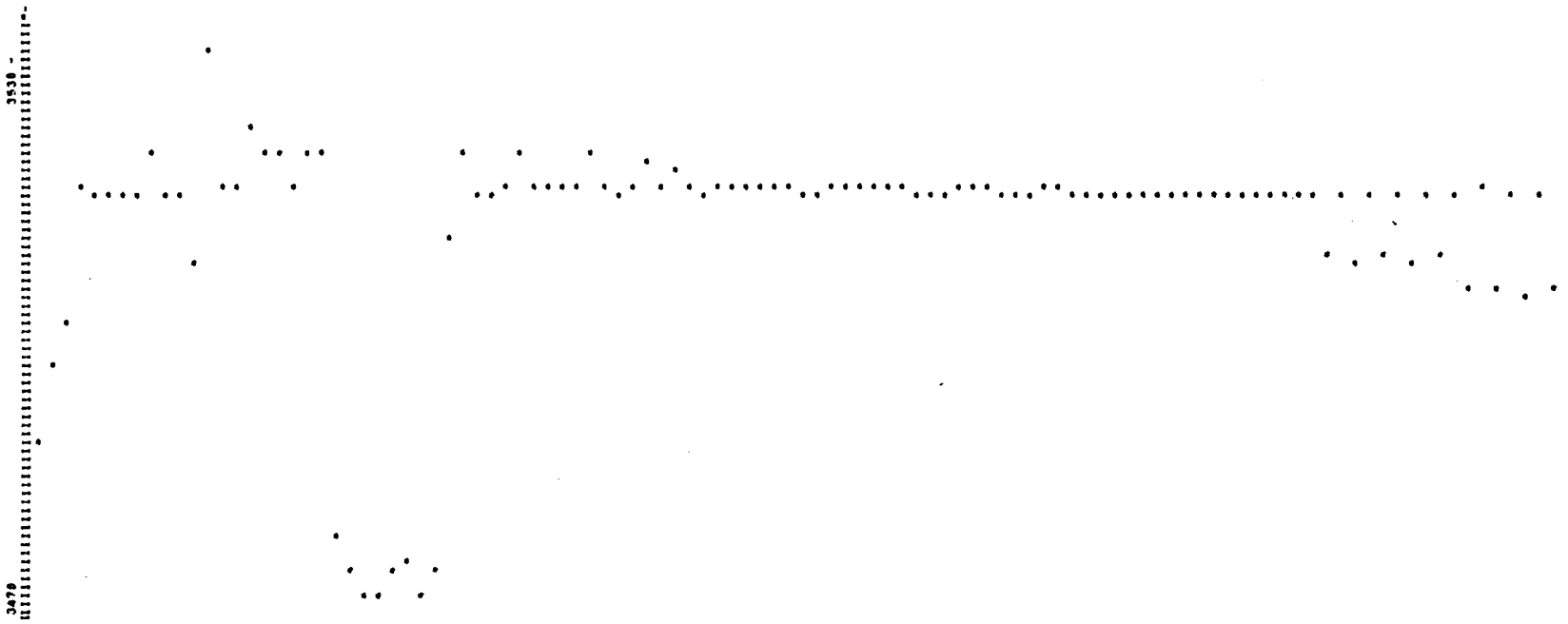


Figure 44. Small Signal Square Wave Response at 10 MHz Clock Rate

SECTION IV

RECOMMENDATIONS FOR A DEPLOYABLE FAST-SAMPLING SYSTEM

During this program we have had considerable hands-on experience with the Honeywell CCD fast-sampling system. Our studies have brought us to the conclusion that this technology can best be utilized when integrated into an intelligent sampling module. Such a module would contain a programmable signal source, an input buffer-multiplexer, a fast sampler, and a microcomputer. This module, shown in Figure 45, would be similar to our existing fast-sampling system with the addition of a programmable signal source, input buffer, and software tailored to perform a variety of ATE functions.

This intelligent sampling module could be used over a broad range of ATE applications in the two configurations shown in Figure 46. One or a few of these modules could be used in small man-portable ATE systems. These small systems could operate under the control of a single microcomputer and could be used for in-field test and repair. For larger fixed ATE systems, the intelligent sampling module could be used as an adjunct to the control computer in an ATE system. Data taking and preprocessing functions can be performed within each module under system control, thus distributing the processing load throughout the system.

The next step in the evolution of this technology is to build an intelligent sampling module and test it against a real Army need. An example module

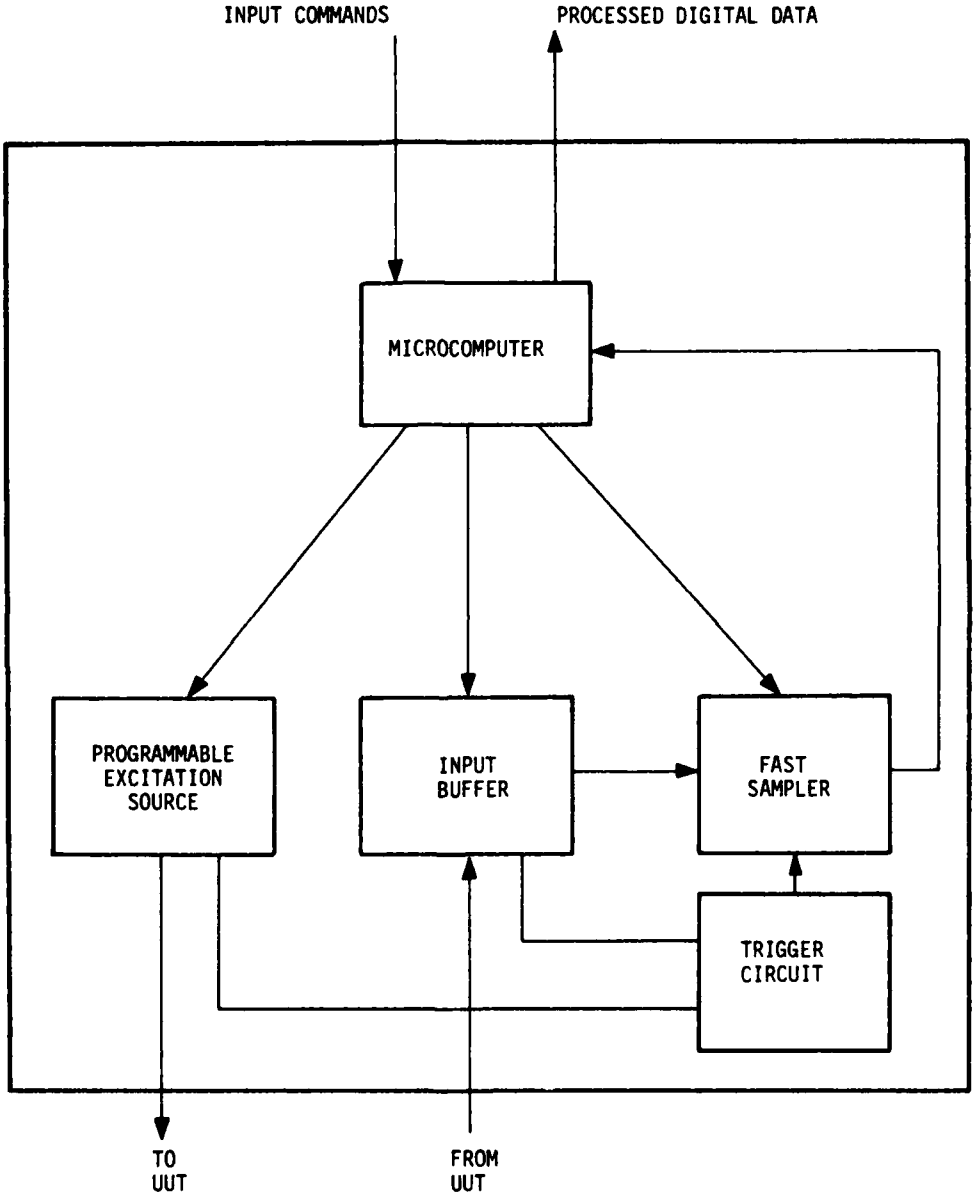
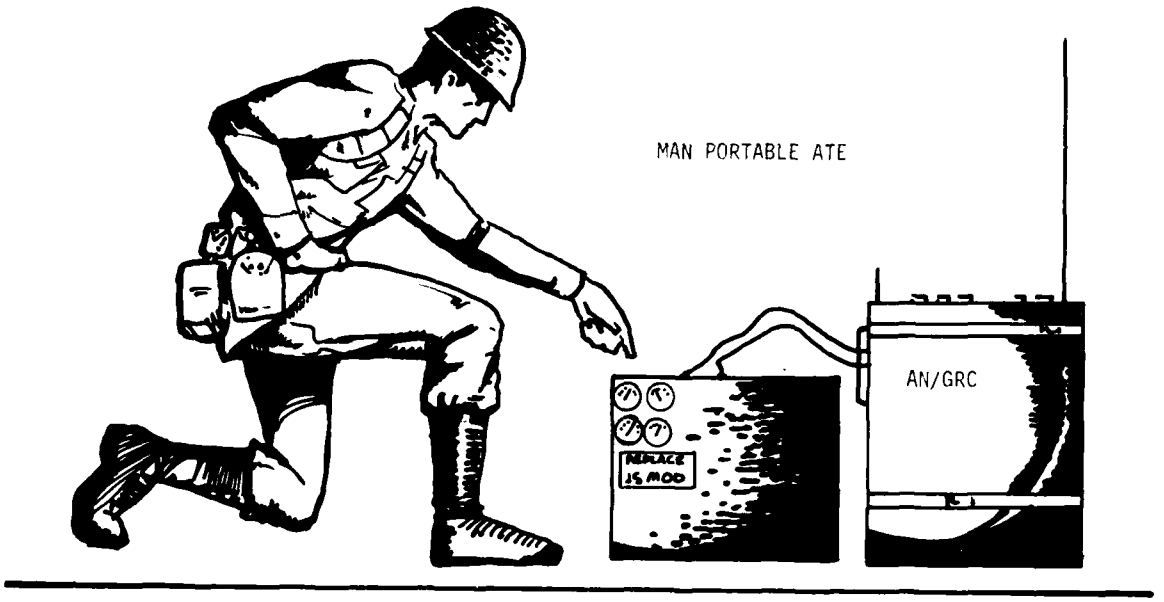


Figure 45. The Intelligent Fast-Sampling Module



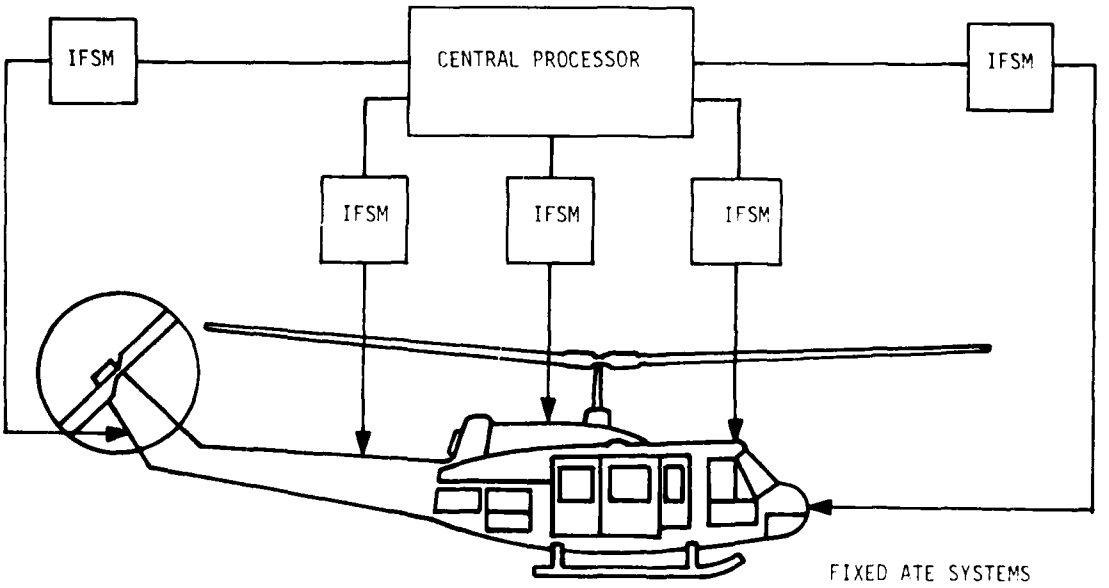


Figure 46. Uses for the Intelligent Fast-Sampling Module (IFSM)

is shown in Figure 47. The module would be equipped with a programmable excitation source, perhaps using CCD technology to develop the required signals. The module would contain as many as eight CCD registers which could be multiplexed to take 1024 consecutive samples of a single input or 128 samples of eight concurrent inputs. The sample rate would be programmable to all sampling rates within the limits of the CCD device. For optimum utility, the module should be equipped with software for spectral analysis, timing measurements, and CCD calibration. It should be tailored to, and tested against, test requirements for Army systems.

Once developed, the intelligent sampling module will perform the function of a large number of conventional instruments, with lower power, less weight, and lower cost. It will bring ATE out of the lab and into the field.

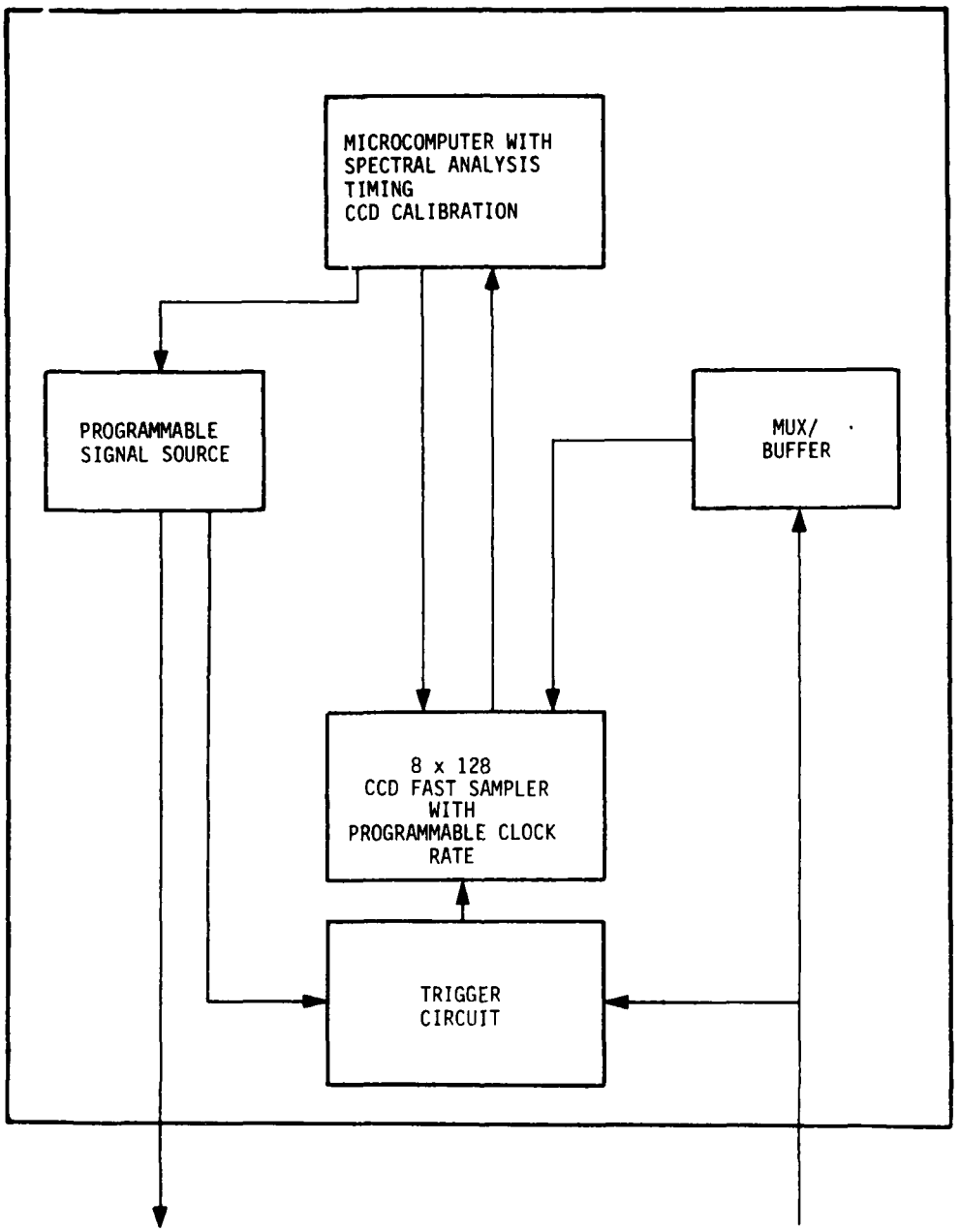


Figure 47. The Next Generation IFS Module

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