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MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM OF ELECTR--ETC(U)

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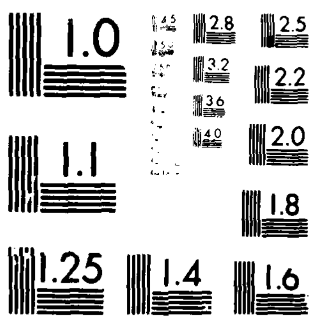

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Research and Development Technical Report
DELET-TR-78-2935-2

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MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM ON ELECTRICALLY ALTERABLE READ ONLY MEMORY

Richard L. Wiker

HONEYWELL INC.
13350 U.S. Highway 19
St. Petersburg, FL 33733

April 1980

Second Interim Report for period 15 January 1979 - 15 December 1979

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Comparison of MNOS Device performance, device type selection, development of screening tests, and test plan.

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DEPARTMENT OF THE ARMY
US ARMY ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY
FORT MONMOUTH, NEW JERSEY 07703

DELET-IB-D

16 June 1980

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Gentlemen:

We understand that Appendix B of our Research and Development Technical Report, DELET-TR-78-2935-2, is not reproducible. This report entitled, "Military Adaptation of Commercial Item (MACI) Program on Electrically Alterable Read Only Memory", was distributed by Honeywell, St. Petersburg, Florida, under contract DAAB07-78-C-2935.

Appendix B contains solely computer print-out raw data and is not essential for reading the main part of the report. It is therefore suggested that you omit Appendix B from your reproduced copies and instead, substitute the following statement:

"Appendix B contains the computer print-out of AC and Functional Screen Tests on the 3400 device and is omitted for technical reasons in this copy. Persons interested in these data are requested to contact the ERADCOM project engineer, Mr. Herbert L. Mette, 201-544-4995, or write to the address indicated in box 11 of the DD 1473 Form of this report".

Sincerely yours,

Herbert L. Mette
HERBERT L. METTE, Leader
Advanced IC Techniques Team

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1.0 INTRODUCTION

The objectives of the MACI Program originally stated in Interim Report No. DELET-TR-2935-1 are restated below. The significance of this program has been further heightened by the expanded use of commercial MNOS Memory Devices in military systems. This has resulted in increased interest in detailed information on the technology and test methods. The MACI-EAROM Program brings much of the practical applications information developed in military systems development together in a usable form for those seeking this data.

The MACI-EAROM Program (Military Adaptation of a Commercial Item for Electrically Alterable Read Only Memories) is designed to study commercially available MNOS Memory Devices of the EAROM/WAROM (Word Alterable Read Only Memory) type and determine which, if any, are suitable for use in military sytems. The results will show (1) which device/devices are feasible for military use (2) the range of conditions of that use and its correlation to the expressed optimum device characteristics indicated by the military applications survey.

Due to the unique MNOS characteristics, and the fact that none of the available devices are specified to military range conditions, the objectives of the MACI program are different from others. In this case, a practical military specification must be developed which is suitable to the MNOS characteristics.

The well established MIL-883, Class B screening normally used for semiconductor devices is used for measuring those parameters which are similar to more conventional memory devices.

The objectives of the MACI-EAROM Program are:

a) Determine the range and type of military applications for MNOS EAROM/WAROMS and the features and parameters most significant in these applications.

b) Determine who is making MNOS devices, which devices are available and should be investigated.

c) Determine the status of MNOS memory device vendors, their support for these devices and future plans.

d) Develop test plans for, procure and functionally test candidate MNOS memory devices to determine their suitability for identified military applications.

e) Perform package studies on all candidate devices to determine mechanical suitability to military applications.

f) Perform a comparative study of the results of all previous testing and analysis and with ERADCOM concurrence select a device type or types which are optimum for future military slash sheet development.

g) Develop a screening test plan for the selected device/devices and procure parts.

h) Develop a preliminary slash sheet specification and test plan to verify device/devices against the specification.

i) Perform screening and slash sheet testing on sufficient parts to verify slash sheet and screening test.

j) Deliver 50 parts tested and screened to ERADCOM meeting the slash sheet requirements (50 of each type, if multiple types).

k) Deliver to ERADCOM the following items:

1. Prospective Military Slash Sheet of selected part.

2. Screening procedures for selecting commercial parts that will meet military requirements.

3. Final report detailing results of the MACI program, explanatory information not covered in specifications and recommendations for future programs involving MNOS and/or other memory technology (including information on new MNOS memory devices that mature after the selection process is complete).

2.0 SCOPE

This report covers the conclusion of the preselection phase, the selection of the final devices and the development of the Test Plan for the final phase. Delays in the procurement of the preselection phase devices caused a delay in the First Interim Report. The Second Interim Report is timed to provide a logical conclusion of the preselection phase tied to a logical break point in the development of the slash sheet and screening tests. The following general tasks are covered:

- Program Plan status

- Background (ie: to provide some independence of use to this report)
- Current status of selected devices and potential new devices.
- Performance characteristics of MNOS Memory devices (review of preselection phase results combined with new test results)
- Results of MNOS unique characteristics testing
- Development of screening test plan for endurance test
- Packaging test results
- Comparison of MNOS devices in the form of a matrix showing the relative results of previous tests
- Conclusions drawn from the comparative results
- Preliminary test plans for screening selected parts
- Plans for the remainder of this MACI Program and suggested areas for potential new programs

3.0 PROGRAM PLAN

Figure 3-1 shows the MACI EAROM program plan with the shaded areas indicating the areas either completed or determined unnecessary due to adequate packaging for military use of the selected devices.

Upon completion of the preselection phase of the program ERADCOM approval was given for the selected memory devices and sufficient parts to meet the program requirements were ordered according to an agreed upon quantity for each type.

Package testing was completed and the devices were determined to be suitable for military use from a mechanical standpoint. It was therefore determined that repackaging was unnecessary.

Test plan development was completed for both device types in the preliminary form. These will now be submitted for ERADCOM approval and finalization. These were developed for both normal memory procedures and MNOS specific procedures.

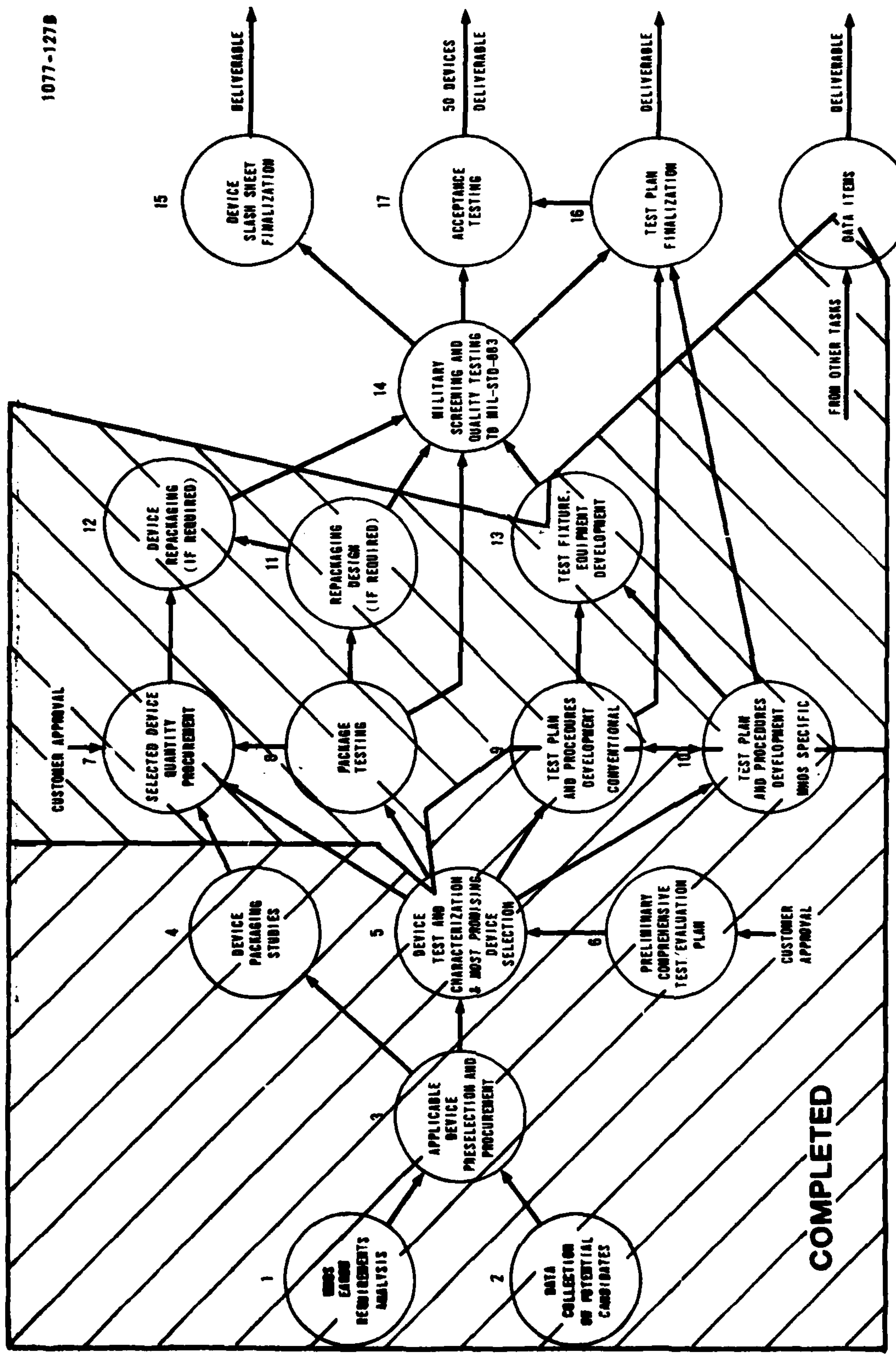


FIGURE 3-1. MACI-MNOS EAROM PROGRAM

While test fixtures and software have been developed and fabricated for both the 2810 EAROM and the 2451/3400 WAROM delivery of parts has been slow. 2810 Parts ordered from Nitron and NCR (NC7810 from Nitron) have resulted in only a partial shipment from Nitron (40 of 225 parts) within two months of the originally promised date of delivery. No 2810 parts from NCR have been received. The delay in delivery is mostly due to high demand for the parts (internal for NCR) and insufficient production capacity at present to meet that demand. Since Nitron is relatively new to producing 2810's (NC7810) start-up and available resource problems plague their current ability to ship parts. While General Instruments is also producing 2810's they are confining their output to High-Rel parts which makes these parts unsuitable for MACI application. The current lapse in availability of 2810's appears will be eliminated in the near future, but the present situation has resulted in Honeywell requesting permission of ERADCOM to revert back to a single candidate device for slash sheet development and delivery of parts. It was requested to select the NCR2451/ER3400 as the final device for this program. ERADCOM accepted this request. The slash sheet development and test plan for the 2810 will be delivered to ERADCOM without the fifty (50) quality tested parts.

4.0 BACKGROUND

The first Interim Report (report No. DELET-TR-78-2935-1 dated October 1979) of the MACI-EROM (Military Adaptation of a Commercial Item for Electrically Alterable Read-Only Memories) Program explained the objectives of the program and how the first phase was developed and carried out. This report consisted of the following:

- The Program Plan
- The development and results of a Military Applications Survey of MNOS Devices.
- Criteria to be used in selecting the final device/ devices.
- Analysis of Available Device Vendors and their capability, current status and inspection procedures.
- Data and analysis of Available Device Performance characteristics such as access time, cycle time, power supply current and radiation resistance.

- Analysis and testing of device packaging and chip layout.
- Conclusions and comparative analysis of available MNOS memory devices.

While extensive results were shown in that report, comparative testing was not complete at the time it went to publication. This report will add the results of the completed comparative testing to the results covered in the initial report and show in matrix form the basis for selection of the final devices.

In addition to the comparative results, additional testing of the selected devices has been performed and reported on in this document. It must be understood by those reading both reports that the data base for the results shown and conclusions drawn is quite narrow. The testing was for the most part performed on less than thirty (30) devices and usually of one lot. Due to the limited resources of the MACI program no extensive characterization was possible. Those wishing to use these results should confirm them with analysis and testing of their own with a more applicable sample of devices.

While the results shown in the first report are accurate based on the data presented some of the testing and analysis philosophy may require clarification. While in some areas facts are implied without being stated. For instance threshold decay prediction used in retention measurement is shown tied almost solely to the written threshold ("0" as defined in the report). The primary reason for this is the inability to measure the normal decay rate of the erased threshold ("1") in a reasonable time period from the time of writing the device. This results from the "Tri-Gate" structure of the memory cell where the thicker oxide areas of the gate region determine the threshold in the high conductance state. The thin oxide region is driven toward depletion and does not control the device threshold until sufficient discharge of stored electrons has occurred to increase the threshold beyond the static threshold value created by the thick oxide region. Figure 4-1 below shows the effect.

The effective device threshold becomes the larger of the superimposed values resulting in the decay of the "1" threshold not being able to be measured until long after the write time (ie: @ $\approx 2 \times 10^6$ seconds in the above example). Assuming the end of life retention points are properly chosen by the device vendor the ("0") written V_T will reach its end of recognition point before the ("1")

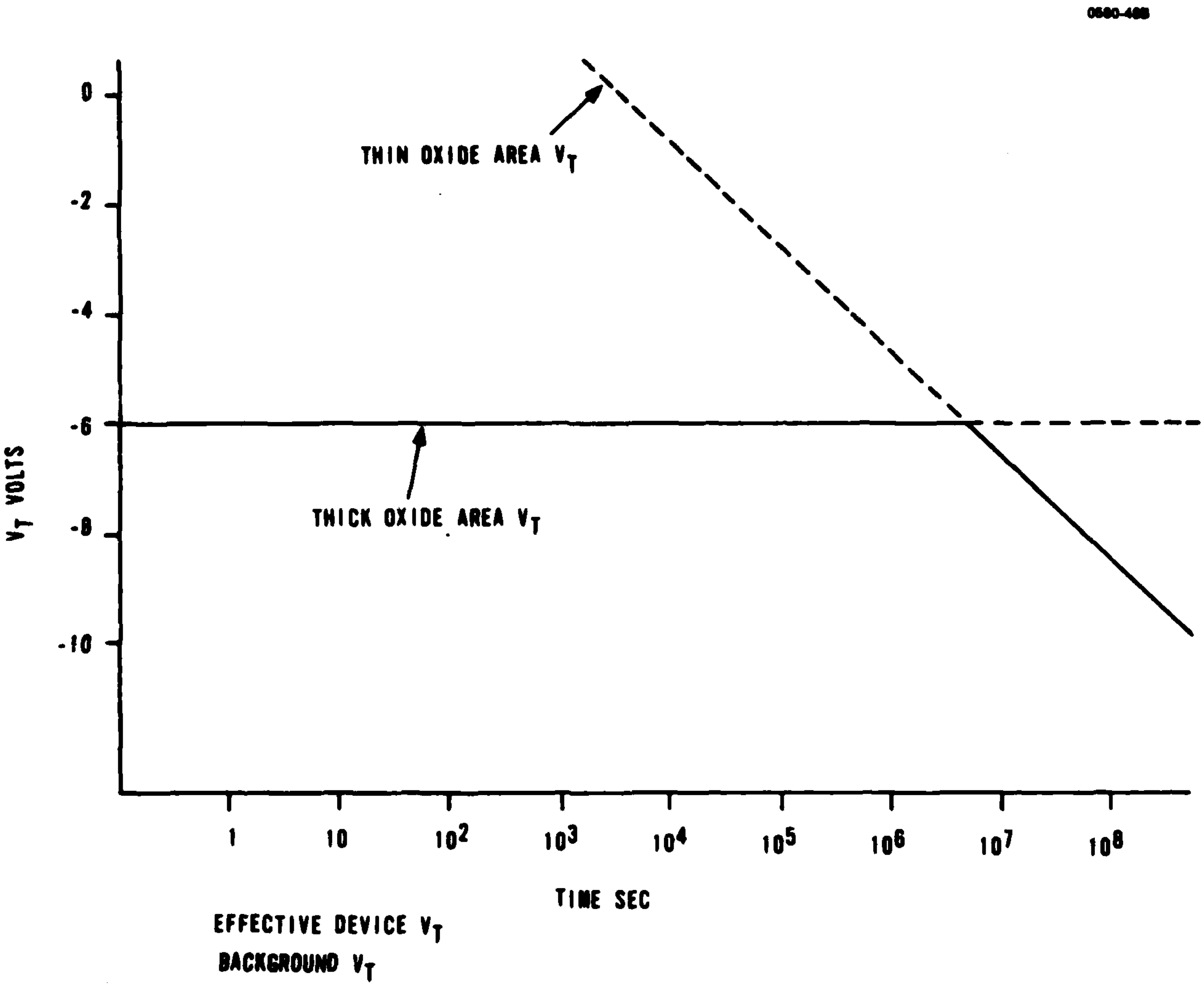


FIGURE 4-1. ERASED V_T PLOT

erased V_T. This is especially true since margin for read disturb effects must be allowed in the "1" V_T margin. The "1" V_T is disturbed by reading while the "0" V_T is enhanced.

Some feedback regarding the First Interim Report has been received. The method of predicting the retention by extrapolating a best fit Lin-Log curve to predetermined end of retention points was shown in Section 8.1. The selected end points are shown on Page 8-4 for 2810 and 2401 EAROMs. some typographical errors clouded the point of the approach. The report reads;

0.2401 - ΔVTI-0 1.5V
0.2801 - ΔVTI-0 1.4V

It should be:

(2401) - ΔV_T(1 to 0) $\leq$ 1.5V

(2801) - ΔV_T(1 to 0) $\leq$ 1.4V

The ΔV_T voltages shown were developed from the following procedure:

- Erase each EAROM with specified ERASE conditions.
- Write each EAROM using a standard specified "Hard" write (checkerboard pattern).
- "Soft" ERASE each EAROM using reduced voltage and time with respect to specified ERASE conditions.
- Read the memory to determine any change in data using specified conditions (or potential system conditions if different). The V_M voltage used in this procedure is of special significance as it will affect the level of the end point. If no data has changed state, repeat the last two operations.
- If a switch in data is detected (multiple reads are performed to insure against intermittent or soft changes) the threshold (MIN) values of the "1 and 0" levels are read. The difference between ΔV_{TI} and ΔV_T is used as the end of retention point.

This method was developed due to lack of available data from the vendors regarding correlation of the threshold measured by the V_M method and the actual end of retention point. In addition, it is a method any user can perform using standard off-the-shelf devices without having access to internal package chip outputs.

The values shown are worst case values determined from the available devices using -5.0V as a V_M input level (specified value) during the reading portion of the test. The results obtained are conservative with regard to the actual in-situ results that can be expected in system use.

This report will further clarify the reasons for the device selection indicated in the First Report and fill in some holes in the data on the selected device characteristics to provide a better applications background.

5.0 MEMORY DEVICE STATUS

The status of several of the candidate devices has changed significantly since last reported. Some of these changes are as follows:

- The NC7053 has been temporarily dropped by Nitron and is not presently available. A new design will be available shortly.
- General Instruments is not currently making a commercial version of the 2810 but plans to in the future if demand is significant.
- General Instruments is making a High-Rel (Military) version of the 2810.
- The price quoted for NC7810 in the earlier report is lower than the current price from Nitron. 225 devices were ordered with the price quoted (9/27/79) at $22.75/ea as compared to the $18.00 price originally quoted on 6 June 1979.
- NCR2810 (from NCR) are in current short supply and only available in small quantities. Orders are being taken for August 1980 delivery.
- General Instruments has reorganized their applications section with significant improvement in that function resulting.
- With NCR and GI shifting to LPCVD Nitride improved nitride thickness control is anticipated. One result that is required of potential users is to recharacterize new parts to determine performance changes resulting from nitride quality and thickness changes. Read disturb, retention, and endurance characteristics should be particularly affected.

- Anticipated Japanese 16K parts (Hitachi) have not yet arrived on the available market place.
- New interest from military sources in use of MNOS in recording systems and radiation resistant applications has been noticed.

Otherwise the status of MNOS devices in military applications and current availability hasn't changed from the initial report. The best devices for future military applications still appear to be the NCR/ER2810 (ie: NC7810) and the NCR2451/ER3400 from a vendor availability outlook. The 2451/3400 is currently more available than the widely used 2810. NC7451 Nitron's version of the 2451 is not yet available (January 1980).

6.0 MEMORY DEVICE PERFORMANCE CHARACTERISTICS

A review of some of the previously reported results is shown in Section 6.1 with some new data shown in Section 6.2.

6.1 Review of Device Performance Characteristics

Some of the MNOS device performance characteristics are highlighted in Figures 6-1 through 6-13 and Table 6-1. These illustrations cover the following performance characteristics:

- Access time - all devices (Figure 6-1).
- Power Supply Current - NCR2451 (Figure 6-2).
- Power Supply Current - GI3400 (Figure 6-3).
- Power Supply Current - NCR2810 (Figure 6-4).
- Power Supply Current - GI2401 (Figure 6-5).
- Radiation Dose Rate/Retention Tests for NCR2451 (short circuit) - Figure 6-6.
- Radiation Dose Rate/Retention tests for NCR2451 (Biased) - Figure 6-7.
- Radiation Dose Rate/Retention tests for GI3400 (short circuit) - Figure 6-8.
- Radiation Dose Rate/Retention tests for GI3400 (Biased) - Figure 6-9.

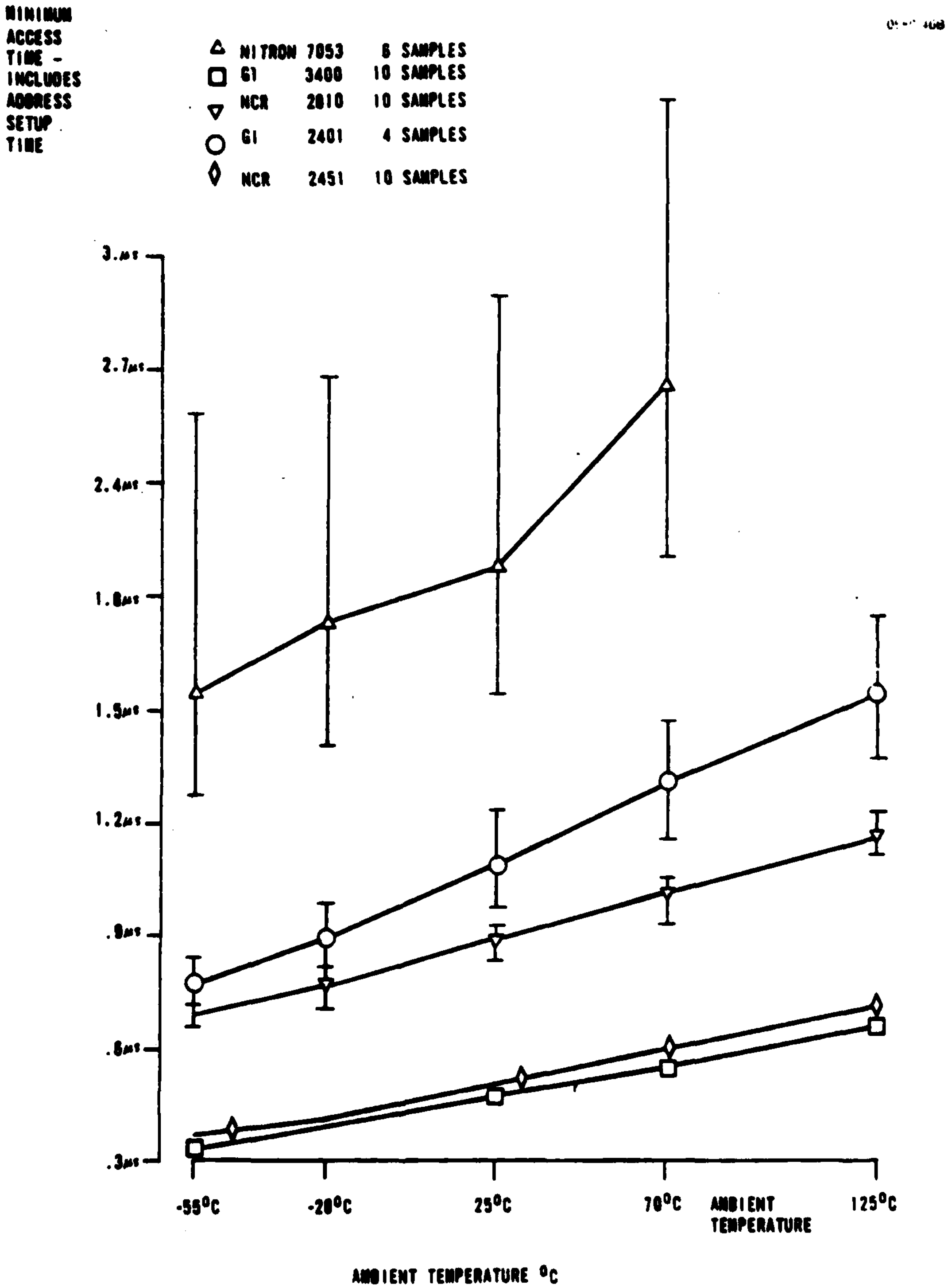


FIGURE 6-1. ACCESS TIMES COMPOSITE

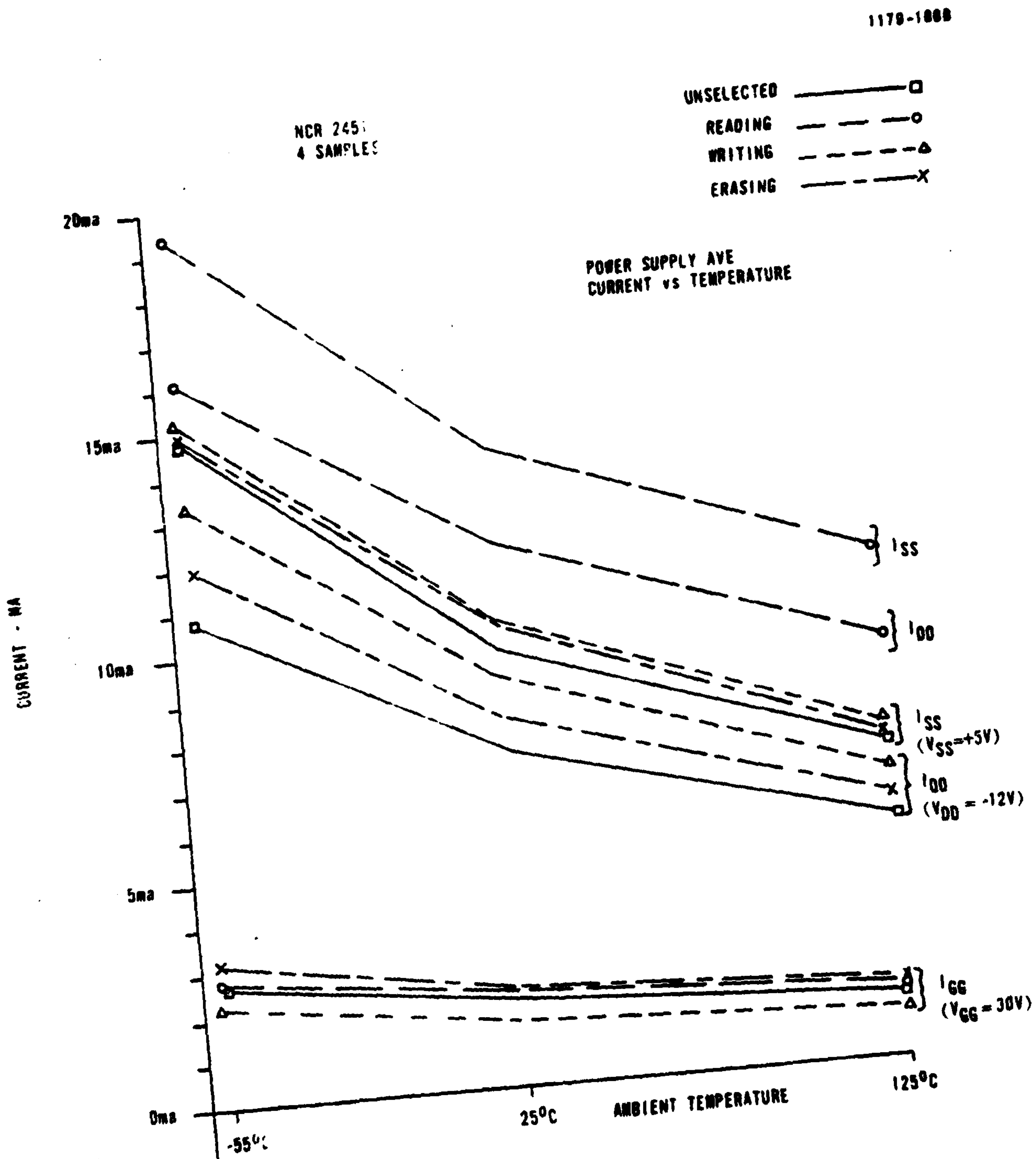


FIGURE 6-2. AVERAGE POWER SUPPLY CURRENT VERSUS TEMPERATURE (AMBIENT) FOR NCR 2451

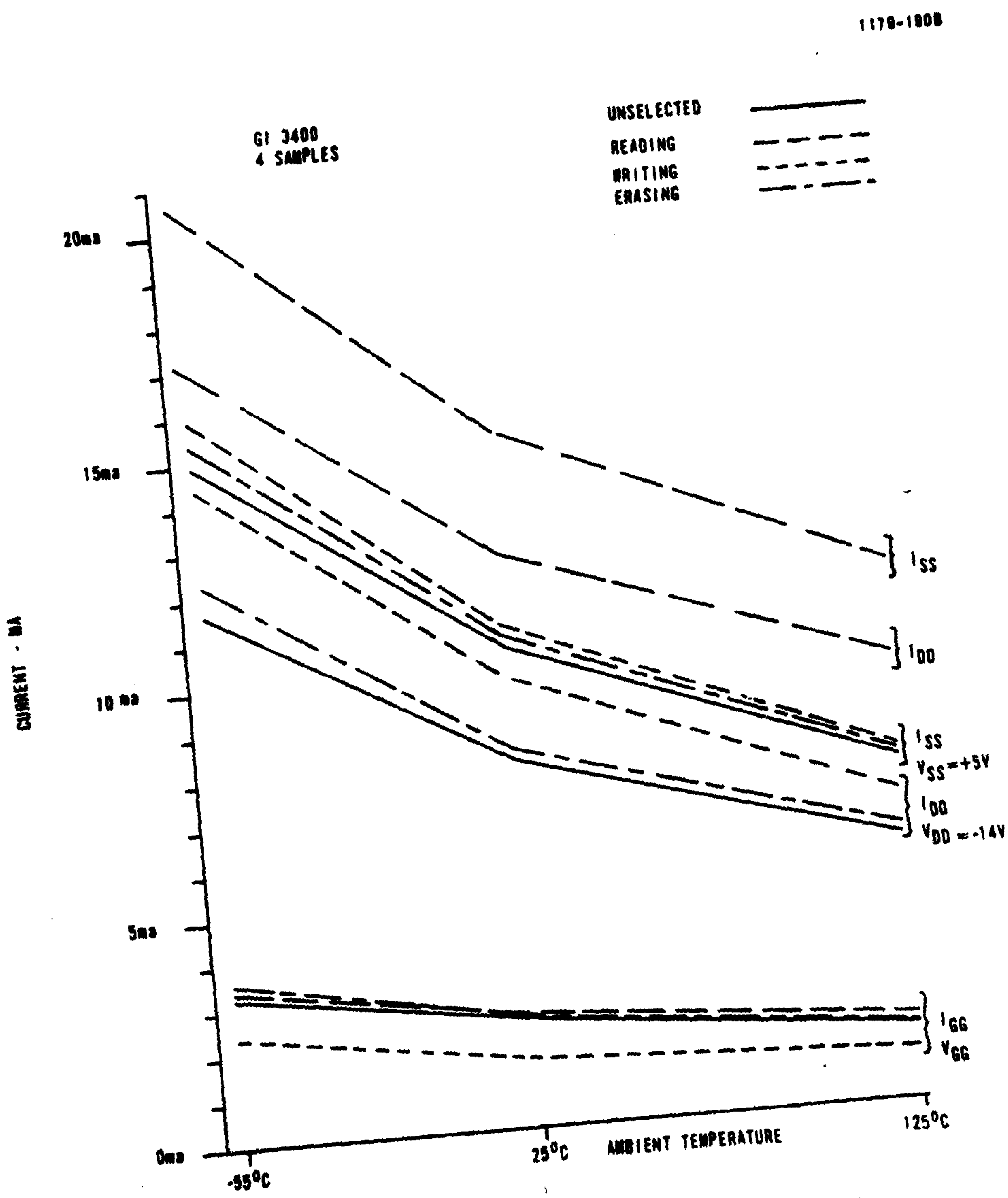


FIGURE 6-3. AVERAGE POWER SUPPLY CURRENT VERSUS TEMPERATURE (AMBIENT) FOR NCR 3400

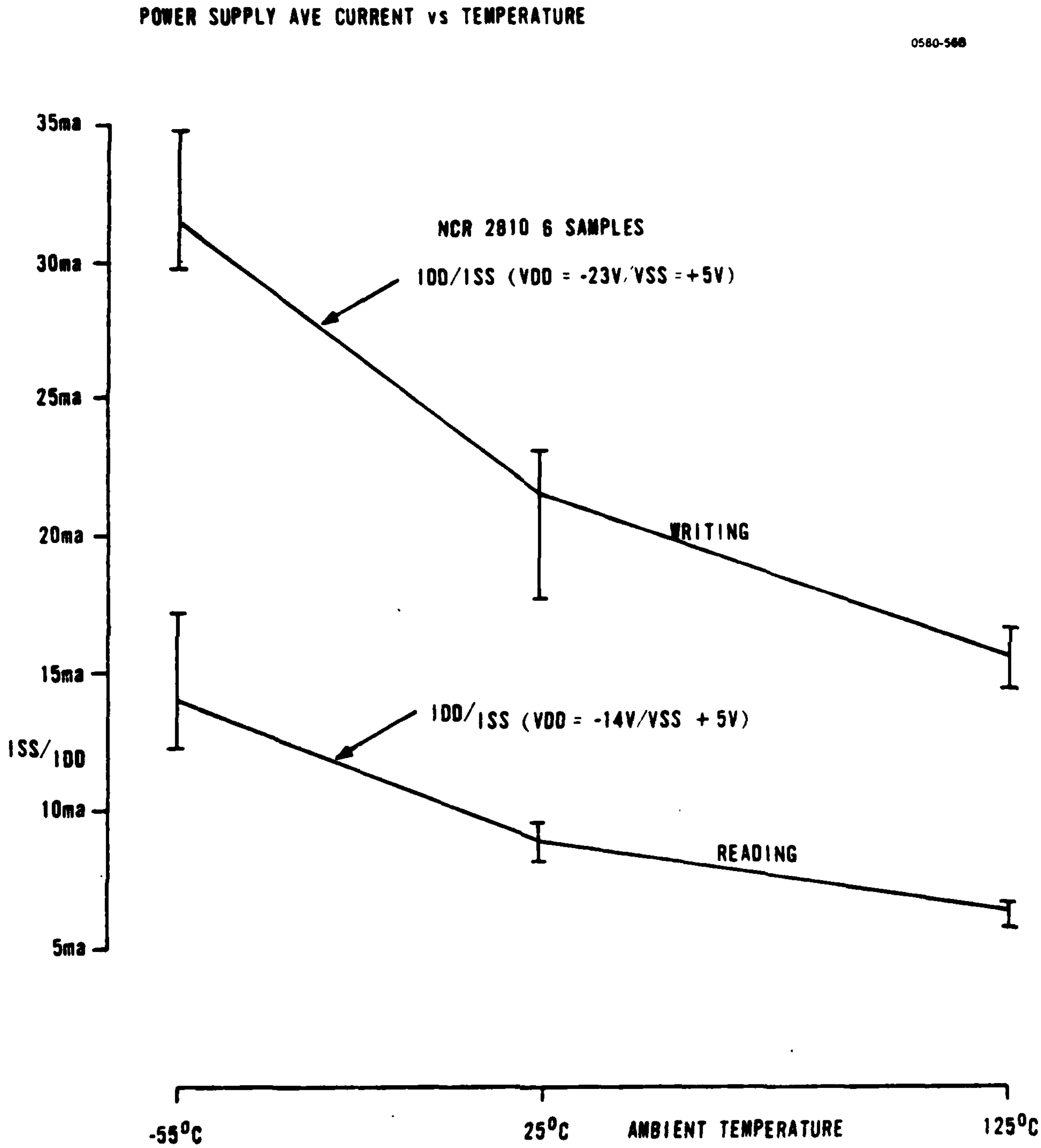


FIGURE 6-4. AVERAGE POWER SUPPLY CURRENT VERSUS TEMPERATURE (AMBIENT) FOR NCR 2810

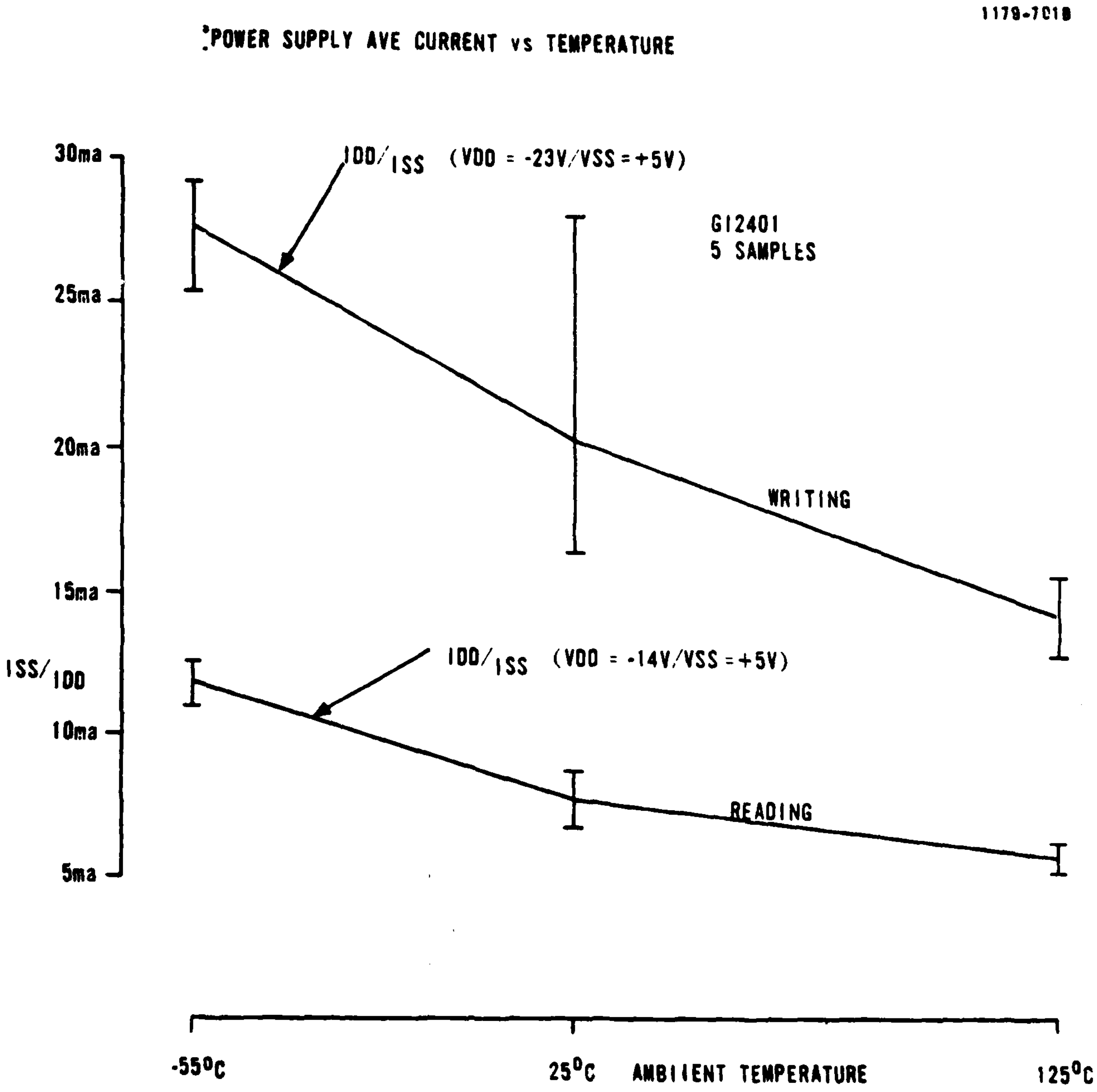


FIGURE 6-5. AVERAGE POWER SUPPLY CURRENT VERSUS TEMPERATURE AMBIENT FOR GI2401

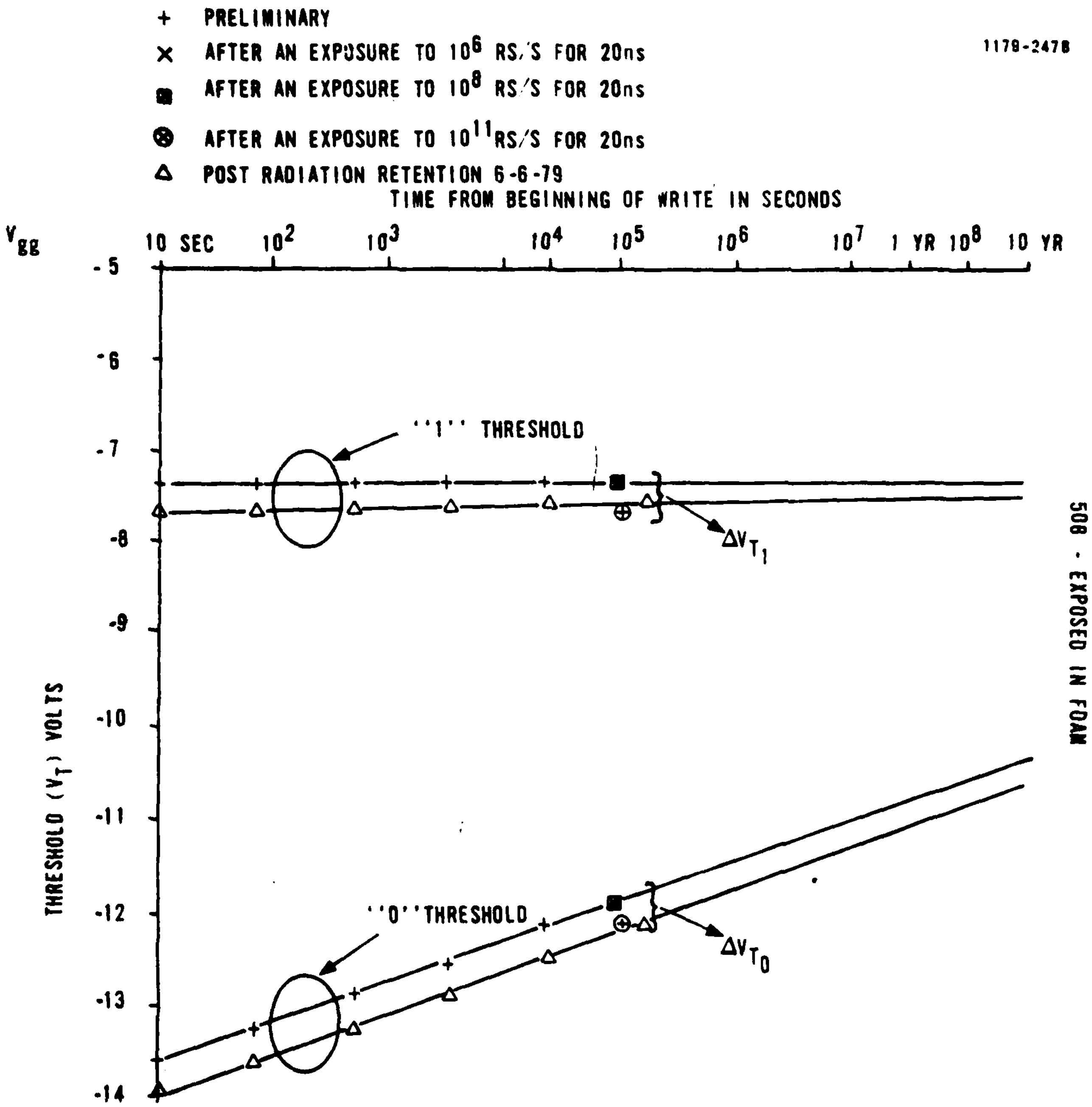


FIGURE 6-6. RADIATION EXPOSURE TESTING OF NCR2451 (SHORT CIRCUIT UNBIASED STATE)

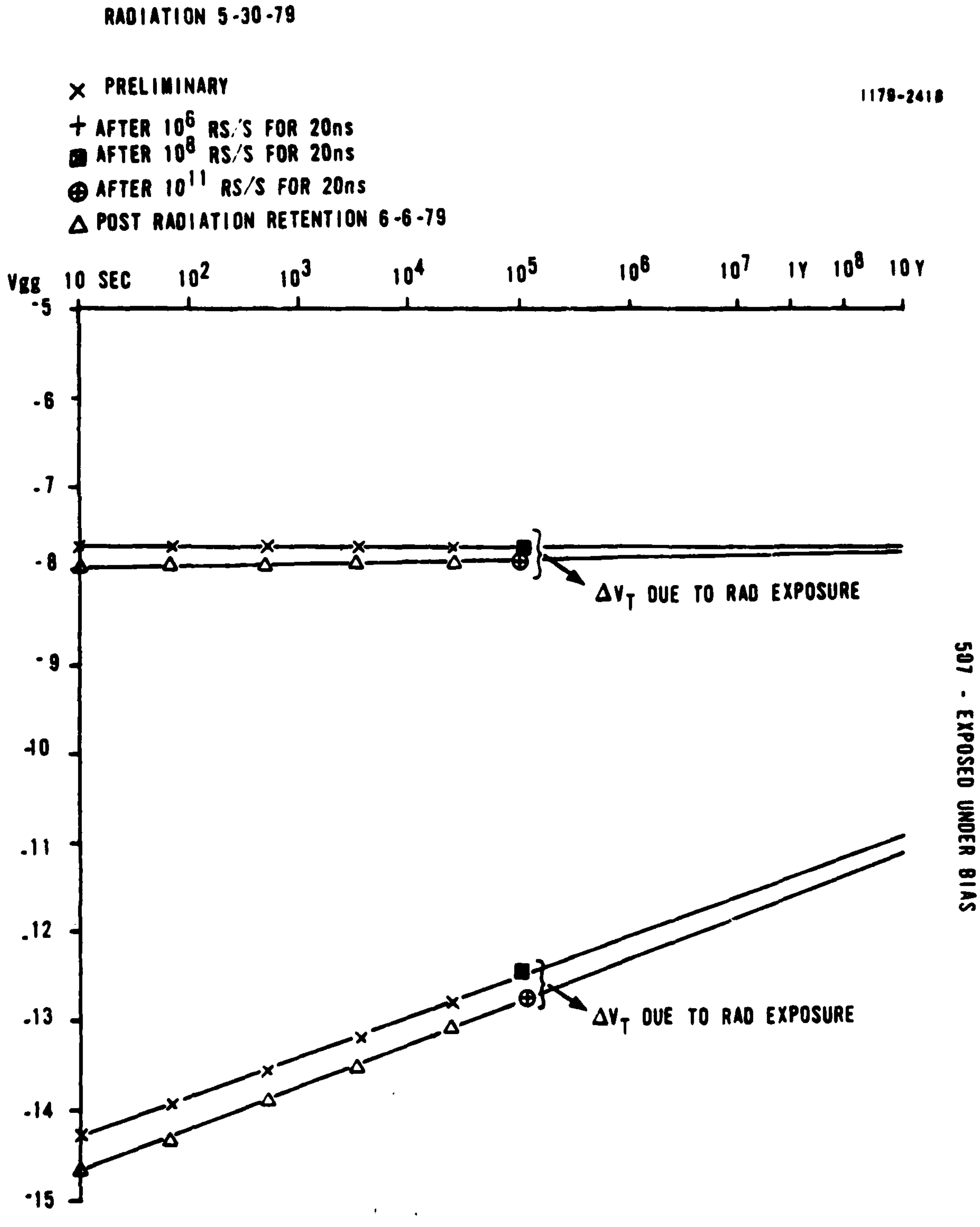


FIGURE 6-7. RADIATION EXPOSURE TESTING OF NCR2451 (BIASED STATE)

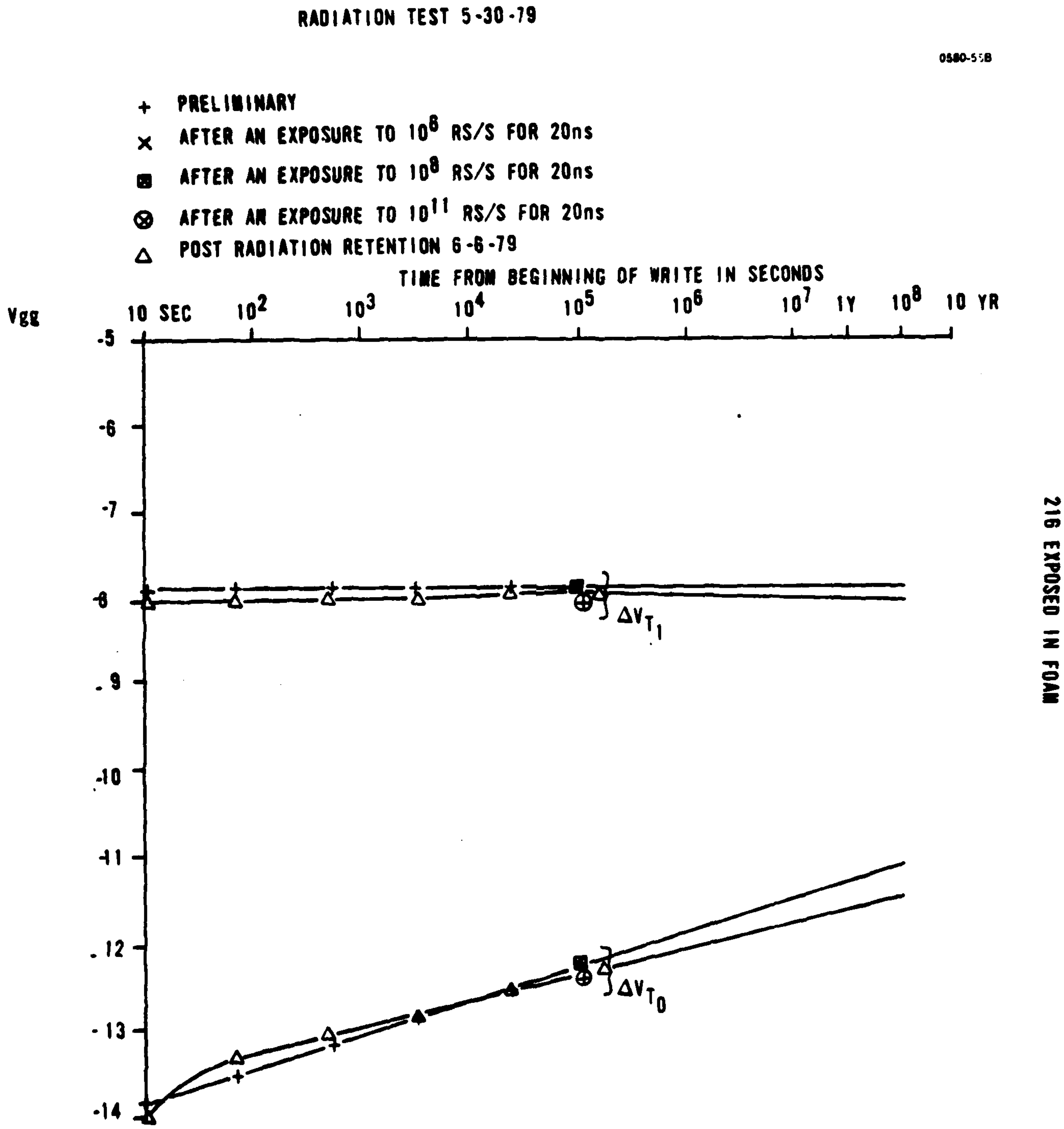


FIGURE 6-8. RADIATION EXPOSURE TESTING OF GI3400 (SHORT CIRCUIT UNBIASED STATE)

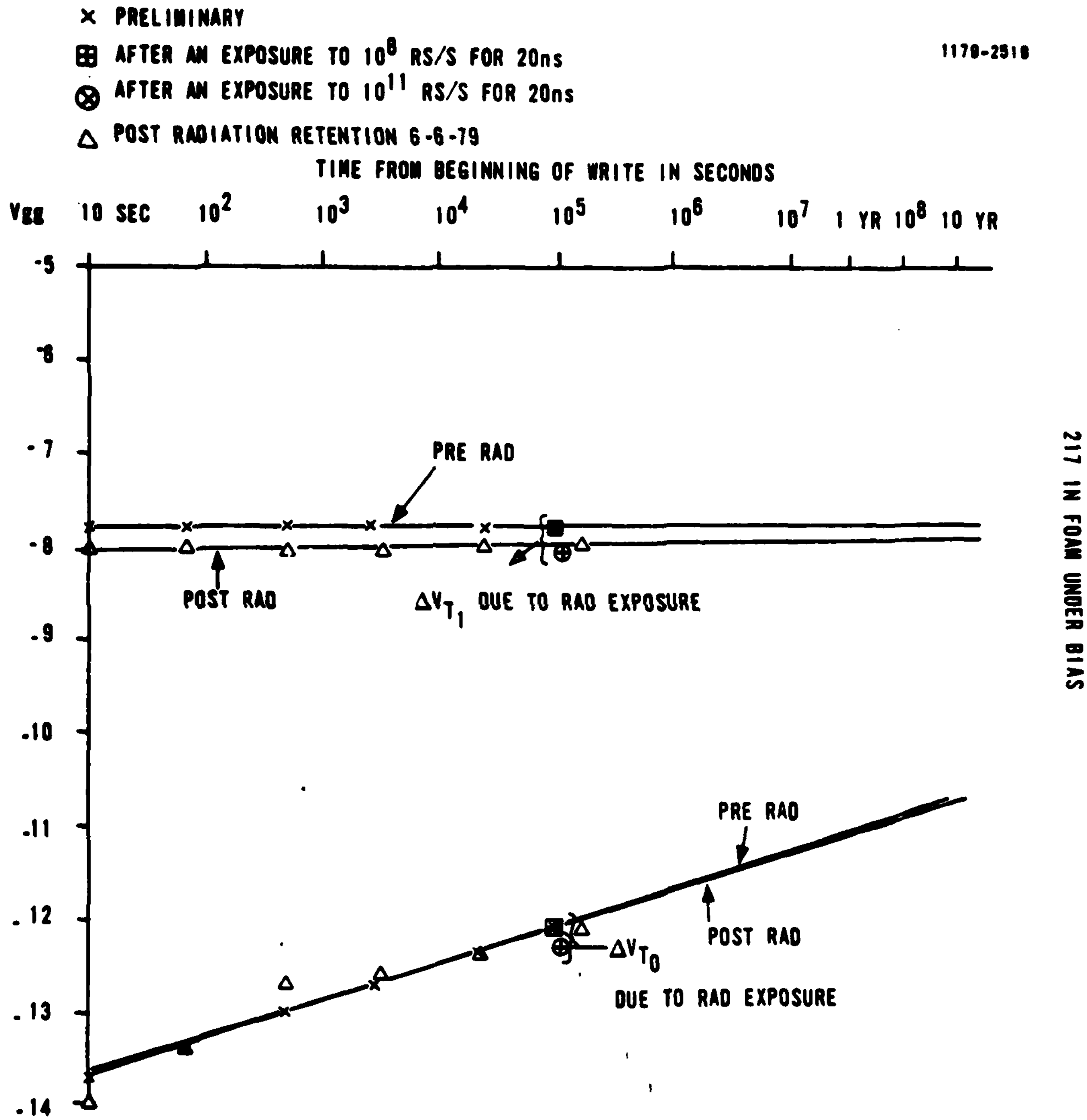


FIGURE 6-9. RADIATION EXPOSURE TESTING OF GI3400 (BIASED STATE)

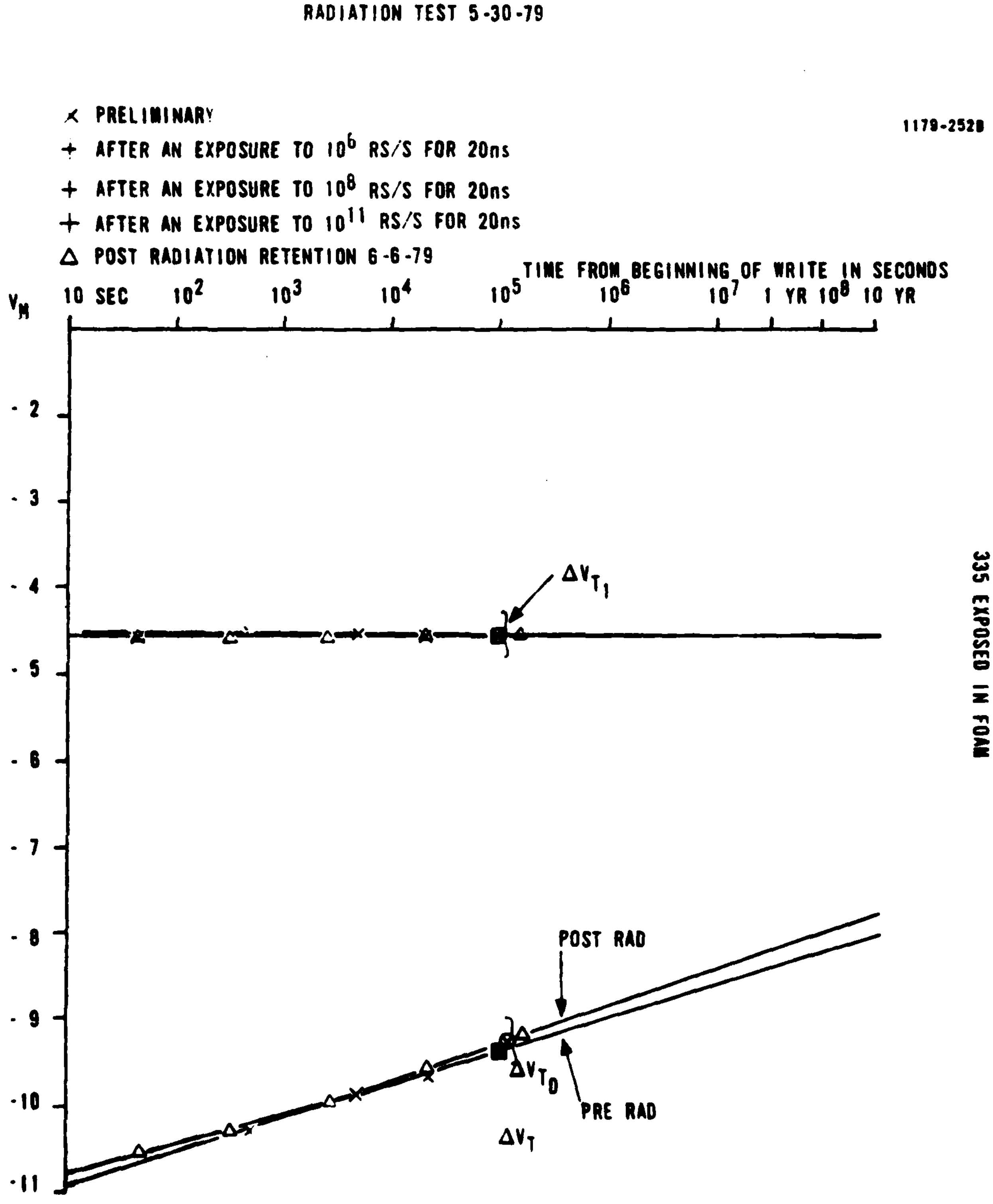


FIGURE 6-10. RADIATION EXPOSURE TESTING FOR NCR2810 (SHORT CIRCUIT UNBIASED STATE)

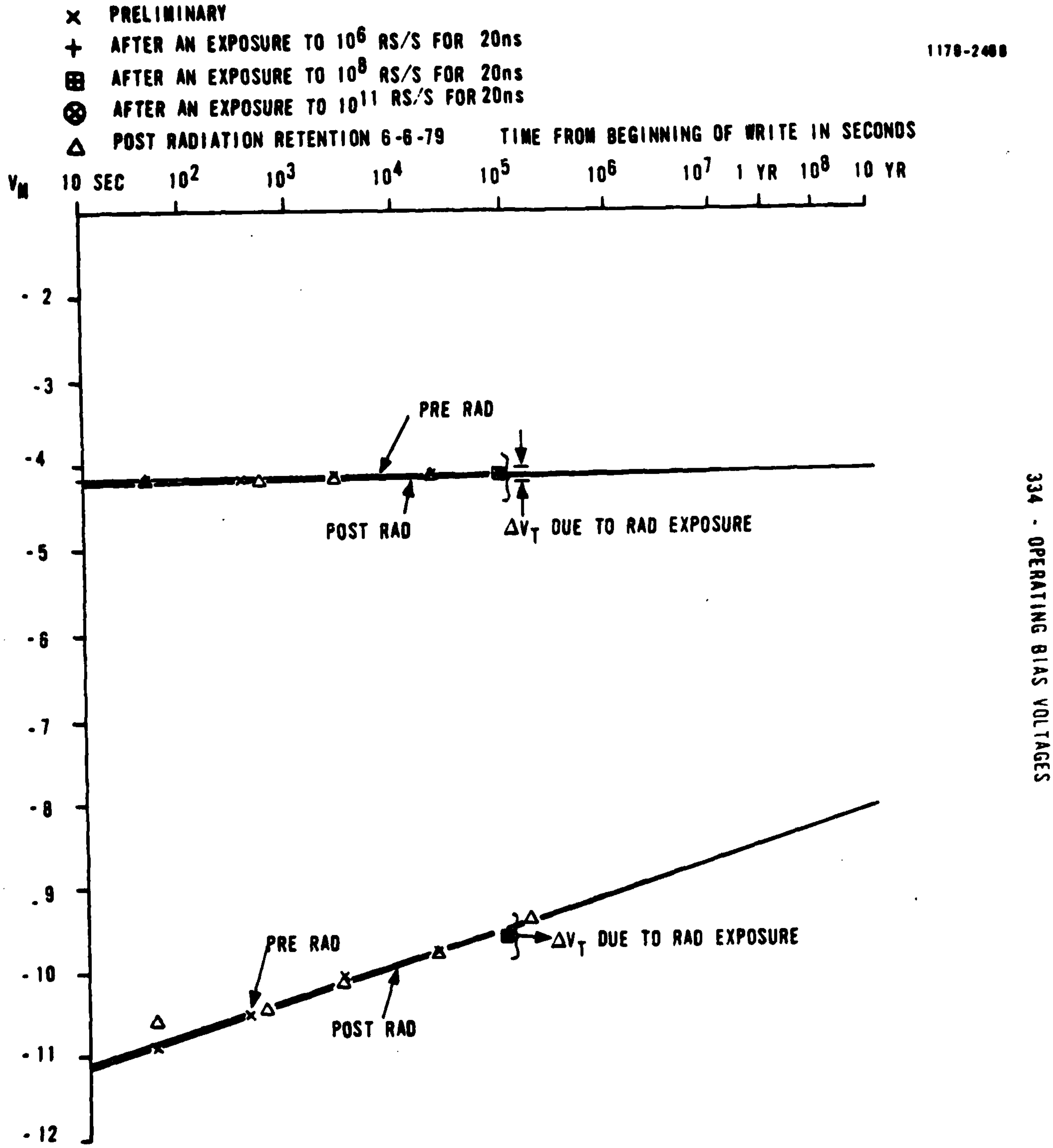


FIGURE 6-11. RADIATION EXPOSURE TESTING FOR NCR2810 (BIASED STATE)

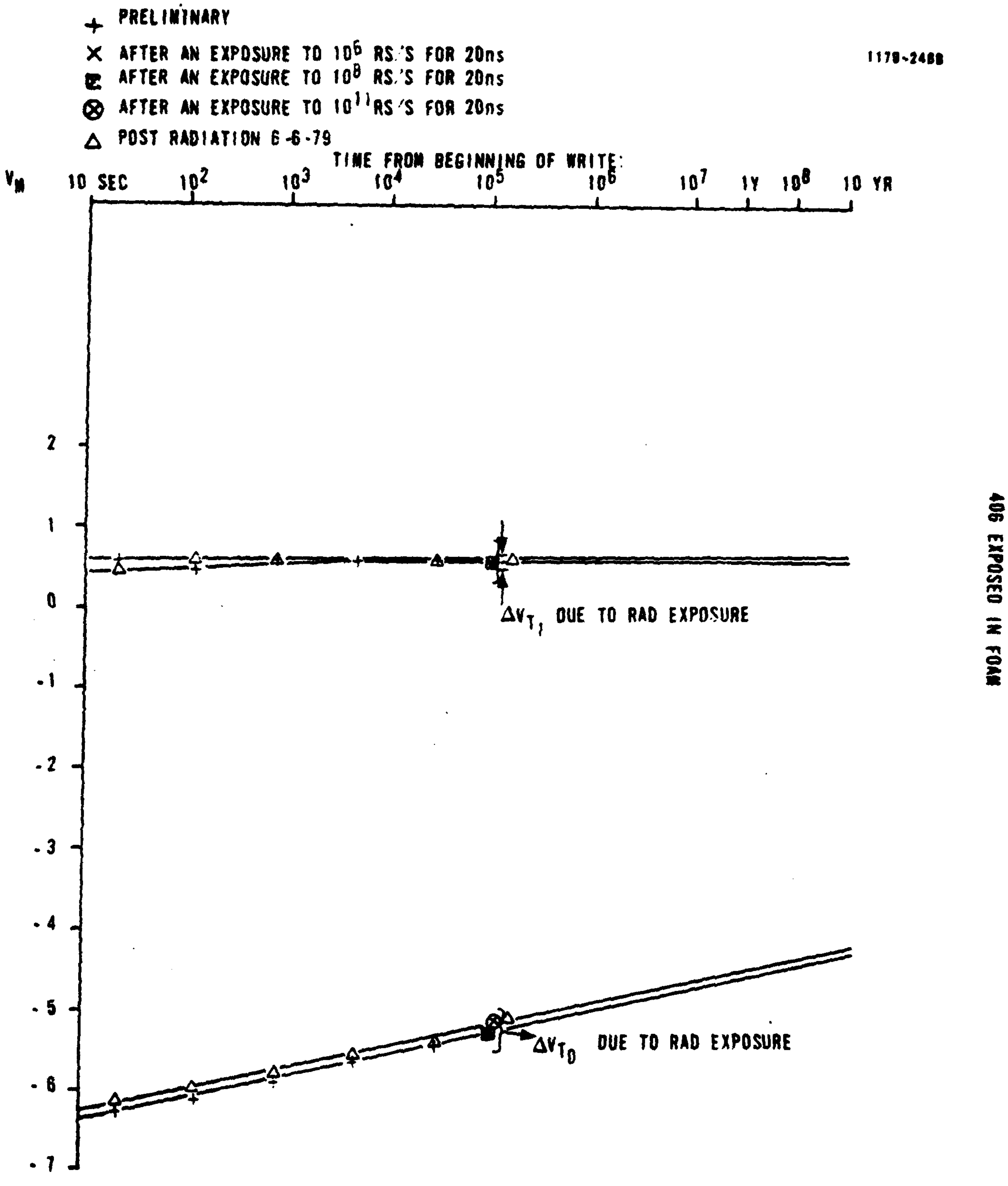


FIGURE 6-12. RADIATION EXPOSURE TESTING OF GI2401 (SHORT CIRCUIT UNBIASED STATE)

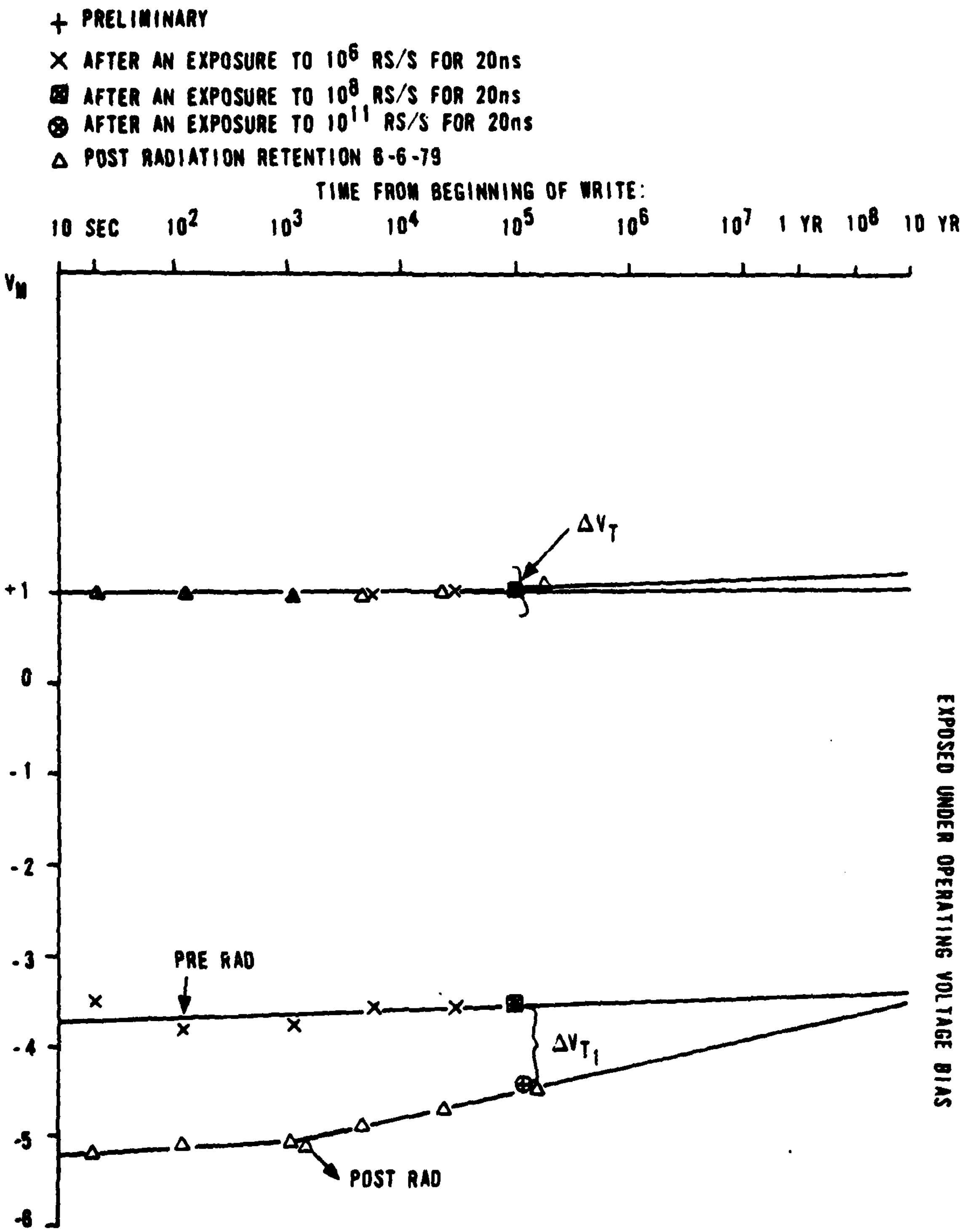


FIGURE 6-13. RADIATION EXPOSURE TESTING OF GI2401 (BIASED STATE)

- Radiation Dose Rate/Retention tests for NCR2810 (short circuit) - Figure 6-10.
- Radiation Dose Rate/Retention test for NCR2810 (Biased) - Figure 6-11.
- Radiation Dose Rate/Retention tests for GI2401 (short circuit) - Figure 6-12.
- Radiation Dose Rate/Retention test for GI2401 (Biased) - Figure 6-13.
- Results of Dose Rate Testing of MNOS Devices - Table 6-1.

These figures and table show the highlights of the First Interim Report testing for memory performance characteristics. The results clearly show the 2451/3400 and 2810 to be applicable for military use and the best choices of those parts observed.

6.2 Static Electrical Tests

These tests were not previously reported on in the last Interim Report.

6.2.1 Objective

The objective was to measure static (DC) electrical characteristics of MNOS devices over military temperature range (-55°C to +125°C), examine effects of temperature and determine most suitable device for military applications.

6.2.2 Procedure

Fifteen devices of each of the five part types were acquired for the static tests. The tests were performed using a Fairchild 5000 automatic memory tester and a Temptronics Thermostream TP450A for temperature control. Devices were tested at -45°C, 0°C, 25°C, 70°C, and 125°C ambient. Due to the time required for the thermostream to reach -55°C, 45°C was used for low temperature measurements. All devices were tested at manufacturer's recommended operating conditions over this temperature range.

6.2.3 Results

Average results for each part type are displayed in Tables 6-1 through 6-4. The vendor specification value is shown for comparison. Graphs of specific parameters versus temperature are included.

When tested to vendor commercial temperature range limits, the 2810 is the only type in which all devices passed all tests[1] over the full military temperature range. Three devices out of thirty 2451/3400 device samples and zero out of fifteen 7053 device samples passed over military temperature range. The 2451 and 3400 type devices are combined because of similar data results.

6.2.3.1 Power Supply Current

All devices met the vendor specifications for power supply current at all temperatures except the 3400 devices, V_{DD} supply current, chip deselected. Supply current is discussed in more detail in the dynamic performance section of the MACI preselection report.

6.2.3.2 Leakage Currents

6.2.3.2.1 Input and Output Leakage Currents

The input and output leakage currents were well below the vendor specification limits on all devices tested over all temperatures.

6.2.3.2.2 Erase Substrate Leakage Current

The erase substrate leakage current on the 2810 and 2401 was well below the vendor specification at all temperatures. The leakage current among devices varied greatly, however. The minimum and maximum erase substrate leakage currents from the sample devices are shown for each device type in Tables 6.3 and 6.4. This is useful in comparing nitride thickness, and therefore endurance, which has been shown to be related to erase substrate leakage current.

6.2.3.3 Data Output Voltages

Of the devices passing the data output voltage tests, all device types were withn vendor specification and standard TTL logic levels. Timing problems which occurred due to limitations of the tester being used rendered some readings unreliable. These were discarded and not included in this comparison.

(1) Data output voltages are not included here due to timing problems during testing which rendered some readings unreliable.

TABLE 6-1. RESULTS OF RADIATION TESTING OF MNOS DEVICES FOR MACI - EAROM PROGRAM

Device	Rad Exp.	Total Dose	Initial V_T Ones	Initial V_T Zeros	Change V_T Ones	Change V_T Zeros	Retention Pre	Retention Post	Average Change V_T/Decade-Zeros Pre	Average Change V_T/Decade-Zeros Post
	10^6	0.02	0.58	-5.14	0	0				
2401 #406	10^8	2.02	0.58	-5.14	-0.2	0	1.49 $\times 10^{20}$	1.72 $\times 10^{20}$	0.2774	0.2763
	10^{11}	2002.02	0.56	-5.14	0	0.033				
	10^6	0.02	-7.7	-12.48	0	0.02				
2501 #507	10^8	2.02	-7.7	-12.45	0.02	0.01	1.15 $\times 10^{11}$	2.36 $\times 10^{11}$	0.4584	0.4773
	10^{11}	2002.02	-7.88	-12.72	-0.22	-0.28				
3400 #217	10^8	2.0	-7.8	-12.1	0	0.02	4.75 $\times 10^9$	5.01 $\times 10^9$	0.4237	0.3700
	10^{11}	2002.0	-7.8	-12.08	-0.22	-0.18				
	10^6	0.2	-4.14	-9.5	0	0				
2810 #334	10^8	2.02	-4.11	-9.5	0	0.02	4.19 $\times 10^{14}$	8.28 $\times 10^{14}$	0.4143	0.4207
	10^{11}	2002.02	4.14	-9.5	-0.02	0.03				

TABLE 6-2. DC PARAMETERS 7053

DEVICE TYPE: 7053

Test	Symbol	Conditions $V_{SS} = 5.0V = -V_{DD}$	Pins	Vendor Spec.	-45°C	0°C	25°C	70°C	125°C	Un
V_{CC} Supply Current	I_{CC}		V_{CC}	25 or 30 max.	17.67	15.05	12.97	11.25	9.16	mA
V_{DD} Supply Current	I_{DD}		V_{DD}	25 max.	16.20	12.28	9.92	8.56	6.94	mA
V_P Supply Current	I_P		V_P	5.0 max.	3.05	2.53	2.57	2.41	2.14	mA
Input Load Current	I_{IL}	$V_{IN} = V_{CC}$	$A_0 - A_6$ $\overline{R}$ $\overline{W}$	10 max.	2.86	2.37	2.16	1.80	1.49	µA
Input Load Current	I_{IL}	V_{IN} = GND	$A_0 - A_6$ $\overline{R}$ $\overline{W}$	350 max.	355	294	262	229	239	µA
Input Load Current	I_{IL}	$V_{IN} = V_{CC}$	E	10 max.	37.47	26.76	20.15	17.03	12.42	µA
Input Load Current	I_{IL}	V_{IN} = GND	$\overline{E}$	350 max.	216	174	162	149	132	µA
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA @ 25V	$D_0 - D_7$ $\overline{CS}$	0.6 max.	.246	.288	.282	.320	.371	V
Output High Voltage	V_{OH}	$I_{OH} = 100\mu A$	$D_0 - D_7$ $\overline{CS}$	2.4 min.	4.52	4.56	4.54	4.49	4.44	V
Chip Select Low Current	I_{CSL}	$0 \leq VCS \leq 0.8$	$\overline{CS}$	0.2 min	5.37	4.74	4.52	3.96	3.48	mA
Chip Select High Current	I_{CSH}	$2 \leq VCS \leq V_{CC}$	$\overline{CS}$	2.2 min.	13.49	12.05	11.40	10.01	8.80	mA

TABLE 6-3. DC PARAMETERS 2451/3400

DEVICE TYPE: 2451/3400

Test	Symbol	Conditions V_{SS} = 5.0V	Pins	Vendor Spec.	-45°C	0°C	25°C	70°C	125°C	Uni
Data Output High Voltage	V_{OH}	I_{OH} = -2 mA	D_0-D_3	3.5 min.	4.86	4.86	4.86	4.86	4.86	V
Data Output Low Voltage	V_{OL}	I_{OL} = 2 mA	D_0-D_3	0.4 max.	0.110	0.139	0.155	0.177	0.207	V
Control Input Leakage Current	I_{LC}	V_{IN} =-10V	C_0, C_1	-2.0 max	-.0033	-.0035	-.0041	-.0042	-.0052	μA
Data Input Leakage Current	I_{LD}	V_{IN} =-10V	D_0- D_3	-10.0 max.	-.0041	-.0045	-.0062	-.0052	-.0163	μA
V_{SS} Supply Current	I_{SS}	V_{DD} = -12V V_{GG} = -30V Chip Selected	V_{SS}	29.0 max	15.23	11.93	11.23	9.62	8.66	mA
V_{GG} Supply Current	I_{GG}	V_{DD} = -12V V_{GG} = -30V	V_{GG}	-4(2451) -3(3400)	-2.74	-2.06	-1.54	-1.50	-1.31	mA
V_{DD} Supply Current	I_{DD}	V_{DD} = -12V V_{GG} = -30V Chip Selected	V_{DD}	-25.0 max.	-19.11	-16.53	-14.01	-11.03	-8.2	mA
V_{DD} Supply Current	I_{DD}	V_{DD} = -12V V_{GG} = -30V Chip Deselected	V_{DD}	-12(2451) -7(3400)	12.04	-9.58	-8.45	-7.33	-5.97	mA

TABLE 6-4. DC PARAMETERS 2810

DEVICE TYPE: 2810

Test	Symbol	Conditions V_{SS} = 5.0V	Pins	Vendor Spec.	-45°C	0°C	25°C	70°C	125°C	Unit
Input Leakage Current	I_{IN}	V_{IN} = -10V $ØL = V_{DD}$ = -15V	A_0 - A_{10} $\overline{W}$, VM, CS	-2.0 max.	-.0322	-.0352	-.0357	-.0355	-.0963	µA
Ø1 Leakage Current	$I_{Ø1}$	$V_{IN} = V_{DD}$ = -24V $\overline{W}$ = -20V	Ø1	-200 max.	0	0	0	-.21	-7.12	µA
Output Leakage Current	I_O	V_{IN} = -10V, Chip Deselected	D_0 - D_3	-10.0 max.	-.024	-.023	-.026	-.026	-.075	µA
V_{DD} Supply Current	I_{DD}	V_{IN} = -14V Outputs Open Read Mode	V_{DD}	-16 max.	-11.19	-8.88	-8.05	-6.72	-5.72	mA
V_{DD} Supply Current	I_{DD}	V_{IN} = -23V Outputs Open Write Mode	V_{DD}	-30 max.	-4.61	-3.84	-3.53	-3.02	-2.68	mA
Data-Output High Voltage	V_{OH}	TTL or MOS Load CL = 100pf	D_0 - D_3	3.5 min.	4.91	4.95	4.95	4.95	4.93	V
Data-Output Low Voltage	V_{OL}	TTL Load	D_0 - D_3	-1.6 max	-7.79	-7.65	-7.30	-7.29	-6.07	V
Data Output Low Voltage	V_{OL}	MOS Load CL = 100pf		-2 max	-16.38	-13.74	-15.29	-15.03	-14.51	V
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Average)	V_{EE}	-200 max	-3.79	-5.73	-7.56	-12.49	-18.87	µA
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Minimum)	V_{EE}		-0.1	-0.3	-0.3	-0.4	-1.5	µA
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Maximum)	V_{EE}		-14.3	-20.9	-27.6	-48.1	-74.7	µA

TABLE 6-5. DC PARAMETERS 2401

DEVICE TYPE: 2401

SIMILAR TO 2810 EXCEPT IN THESE PARAMETERS

	Symbol	Conditions	Pins	Vendor Spec.	-45°C	0°C	25°C	70°C	125°C	Units
V_{DD} Supply Current	I_{DC}	V_{IN} = -14V Outputs Open Read Mode	V_{DD}	-12 max.	-12.86	-10.22	-9.23	-7.22	-4.75	mA
V_{DD} Supply Current	I_{DD}	V_{IN} = -23V Outputs Open Write Mode	V_{DD}	-25 max.	-22.16	-18.27	-16.66	-13.74	-10.50	mA
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Average)	V_{EE}	-200 max	-.82	-1.08	-1.3	-2.1	-4.98	µA
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Minimum)	V_{EE}		0	-0.1	0	-0.2	-3.2	µA
Erase Substrate Leakage Current	I_{EE}	V_{IN} = -23V $\overline{W}$ = -20V (Maximum)	V_{EE}		-3.2	-3.8	-4.5	-6.4	-9.8	µA

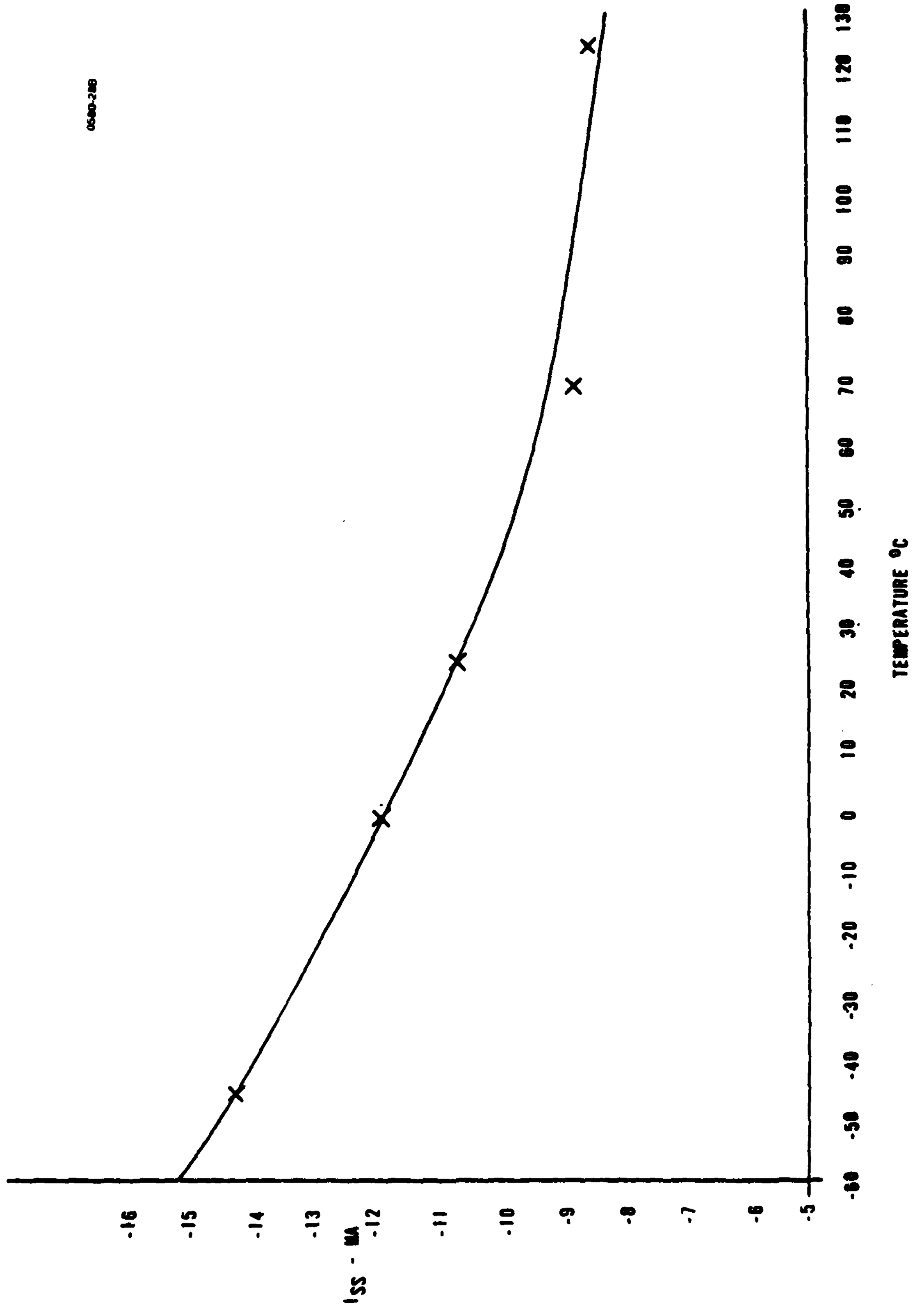


FIGURE 6-14. 2451 V_{SS} SUPPLY CURRENT (I_{SS})

VENDOR SPEC: -29 MA MAXIMUM

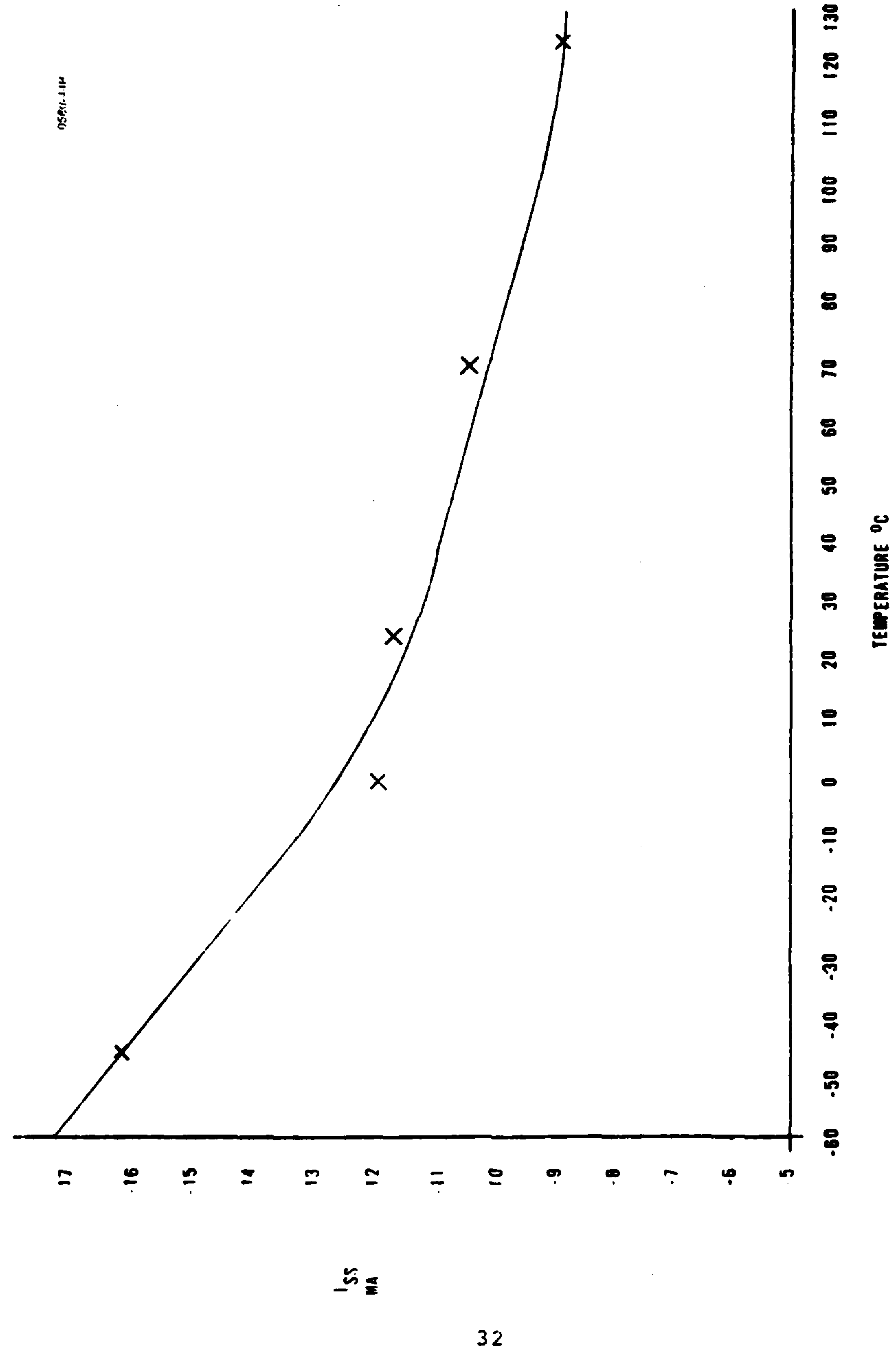


FIGURE 6-15. 3400 V_{SS} SUPPLY CURRENT (I_{SS})
VENDOR SPEC: -29 MA MAXIMUM

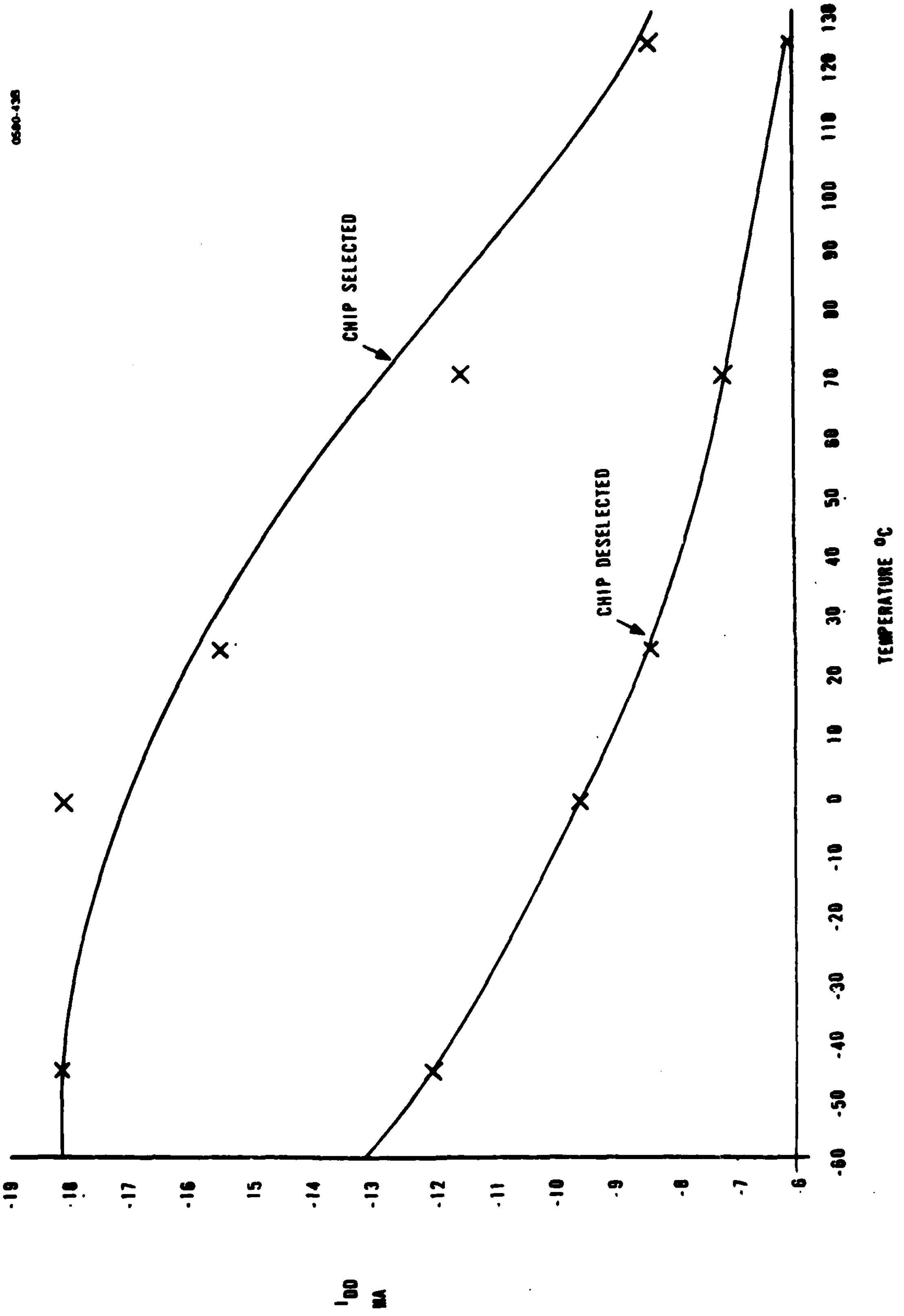


FIGURE 6-16. 3400 V_{DD} SUPPLY CURRENT (I_{DD})
VENDOR SPEC: CHIP SELECTED -25 MA
CHIP DESELECTED -12 MA

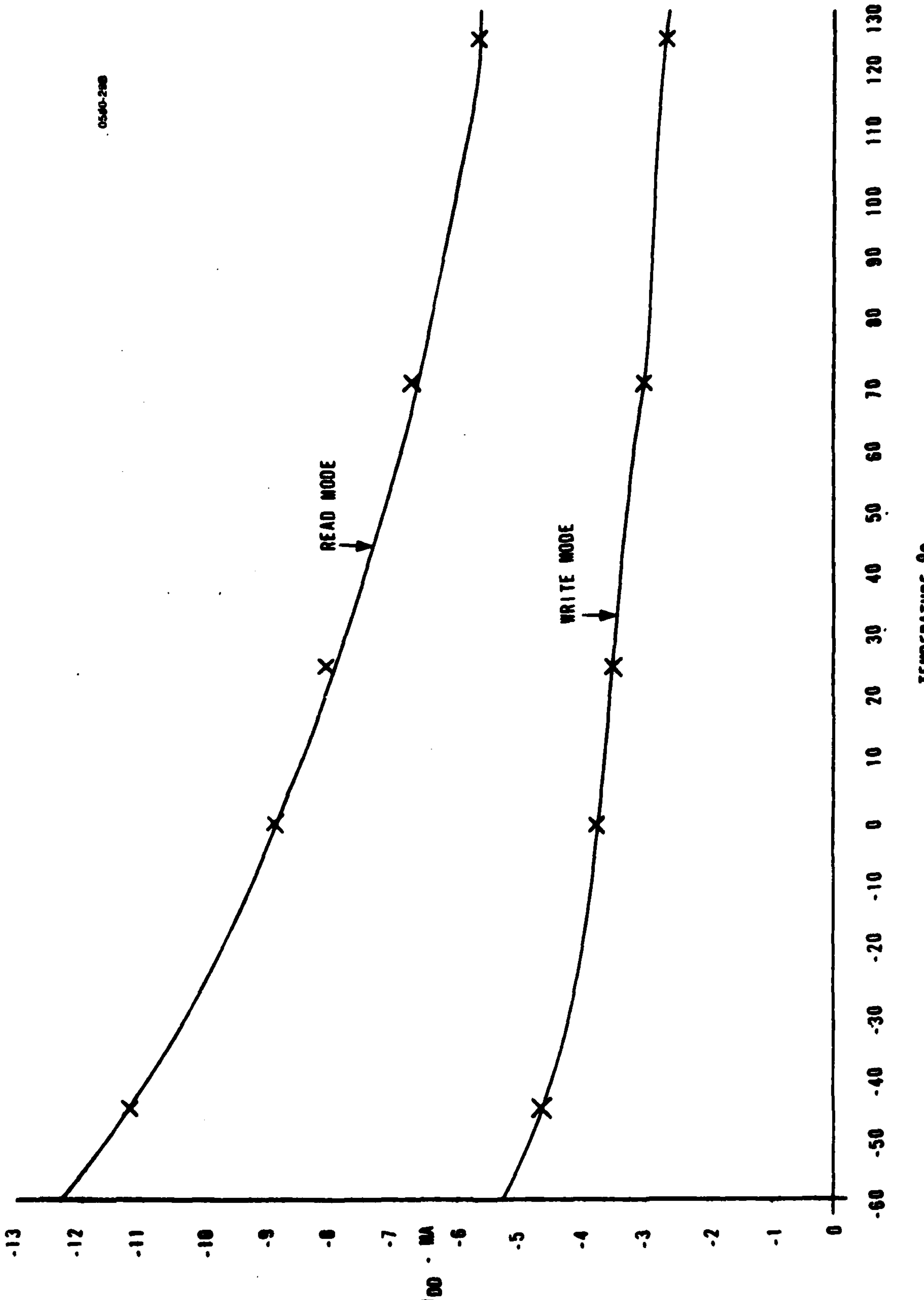


FIGURE 6-17. NCR 2810 V_{DD} SUPPLY CURRENT (I_{DD})
VENDOR SPEC: -16 MA MAXIMUM READ MODE
-30 MA MAXIMUM WRITE MODE

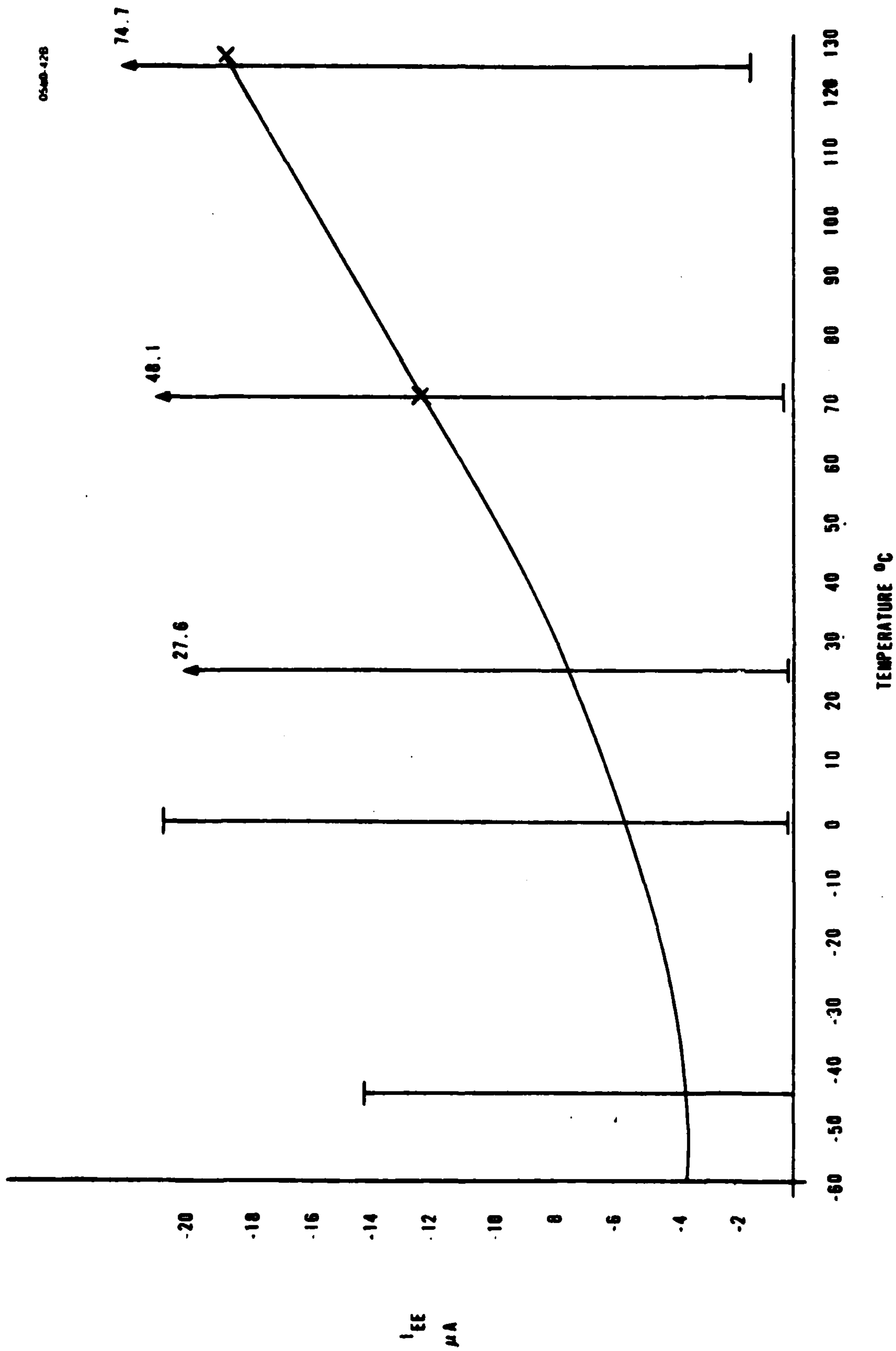


FIGURE 6-18. NCR2810 ERASE SUBSTRATE LEAKAGE CURRENT (I_{EE})

VENDOR SPEC: -200 µA MAXIMUM

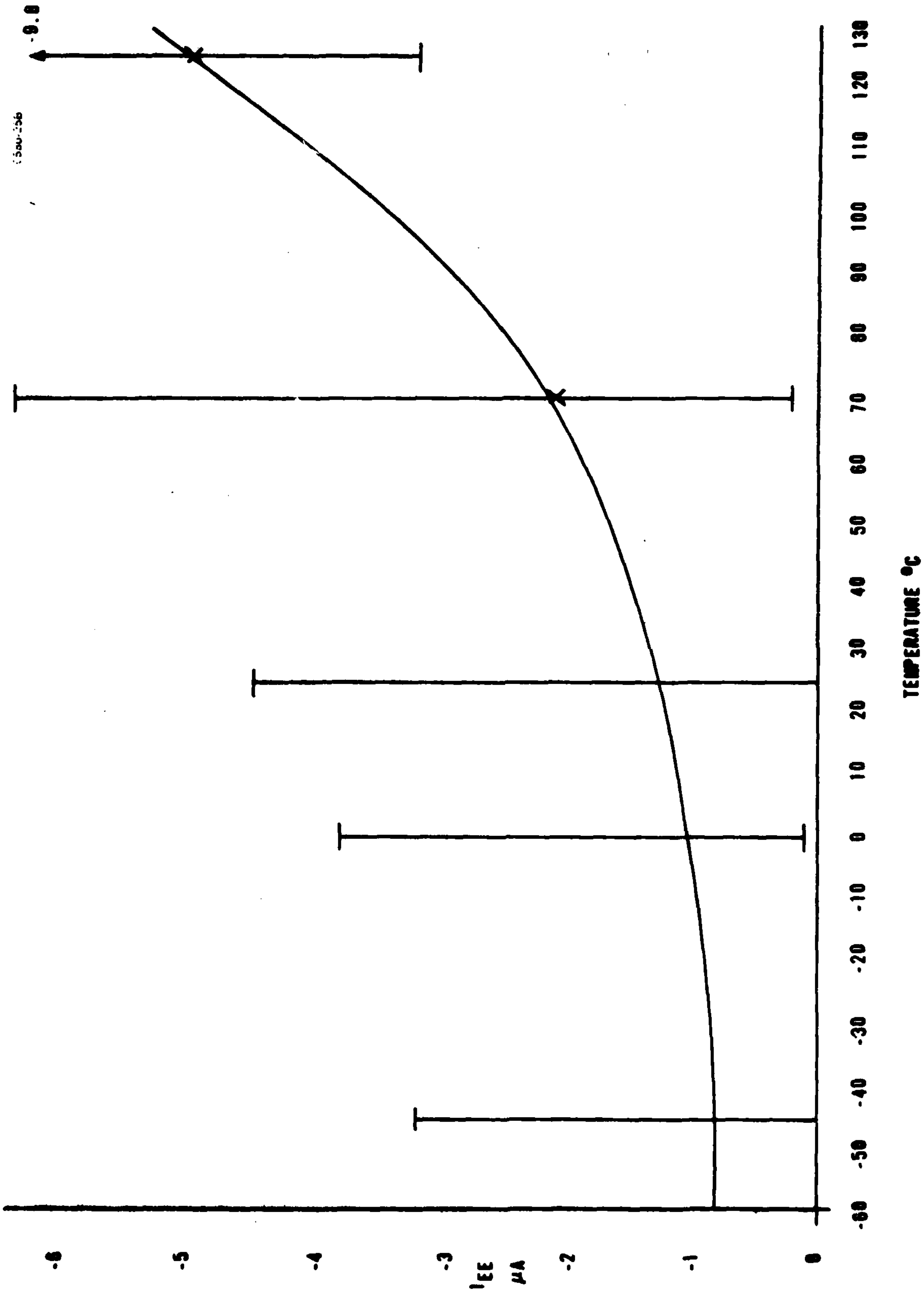


FIGURE 6-19. 2401 ERASE SUBSTRATE LEAKAGE CURRENT
VENDOR SPEC: -200 μA MAXIMUM

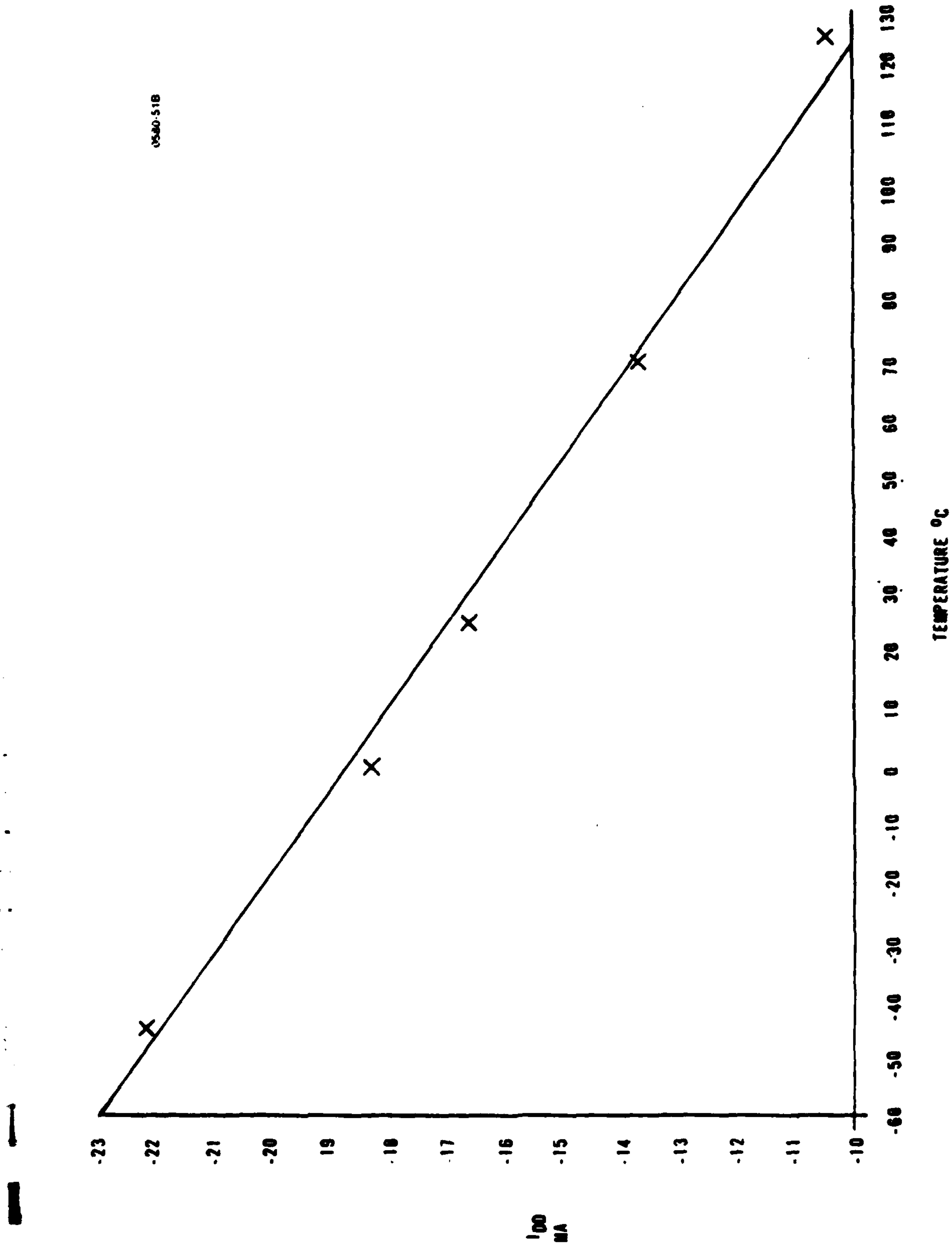


FIGURE 6-20. 2401 V_{DD} SUPPLY CURRENT WRITE MODE
VENDOR SPEC: -25 MA MAXIMUM

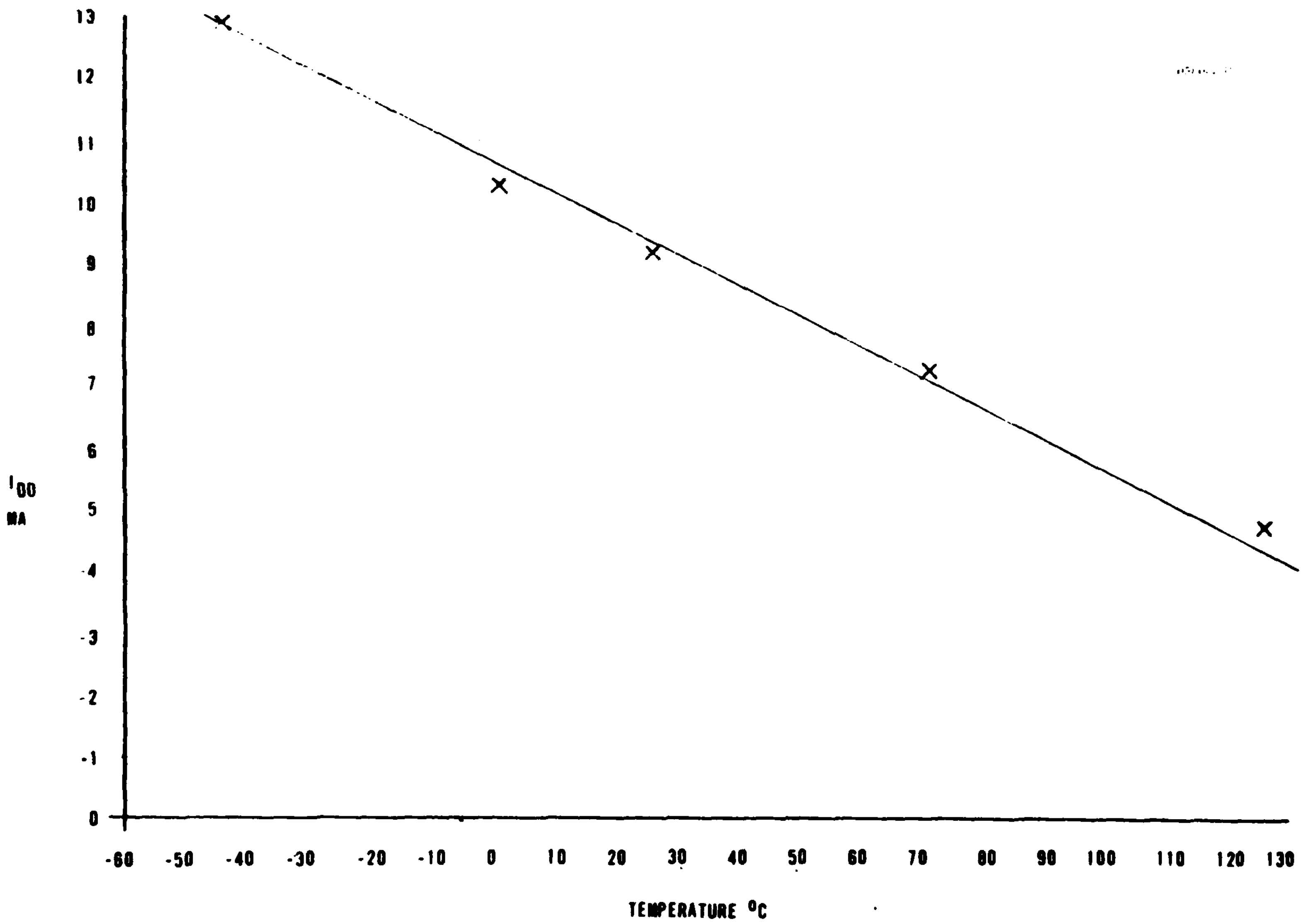


FIGURE 6-21. 2401 V_{DD} SUPPLY CURRENT (I_{DD}) READ MODE
VENDOR SPEC: -12 MA MAXIMUM

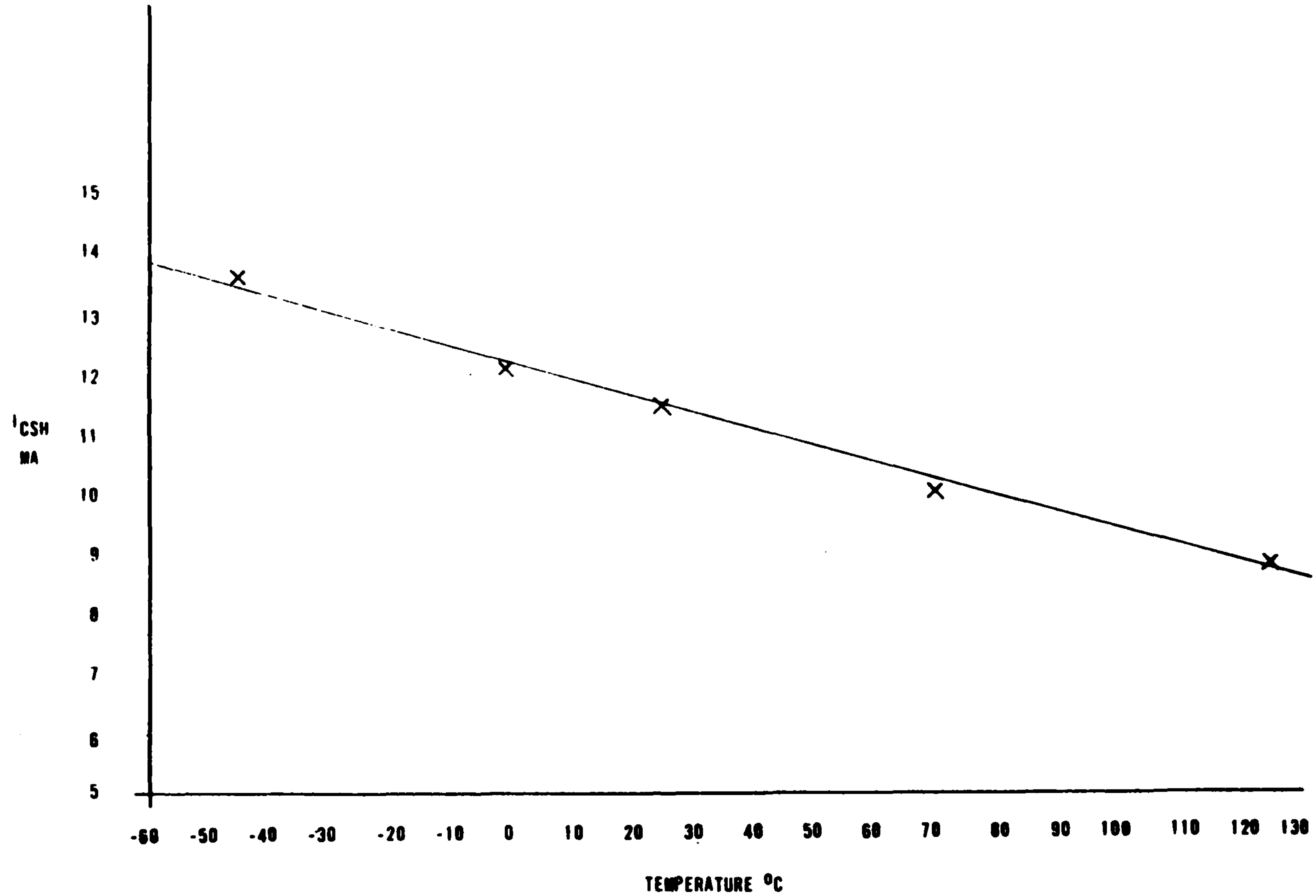


FIGURE 6-22. 7053 CHIP SELECT HIGH CURRENT (I_{CSH})
VENDOR SPEC: 2.2 MA MINIMUM

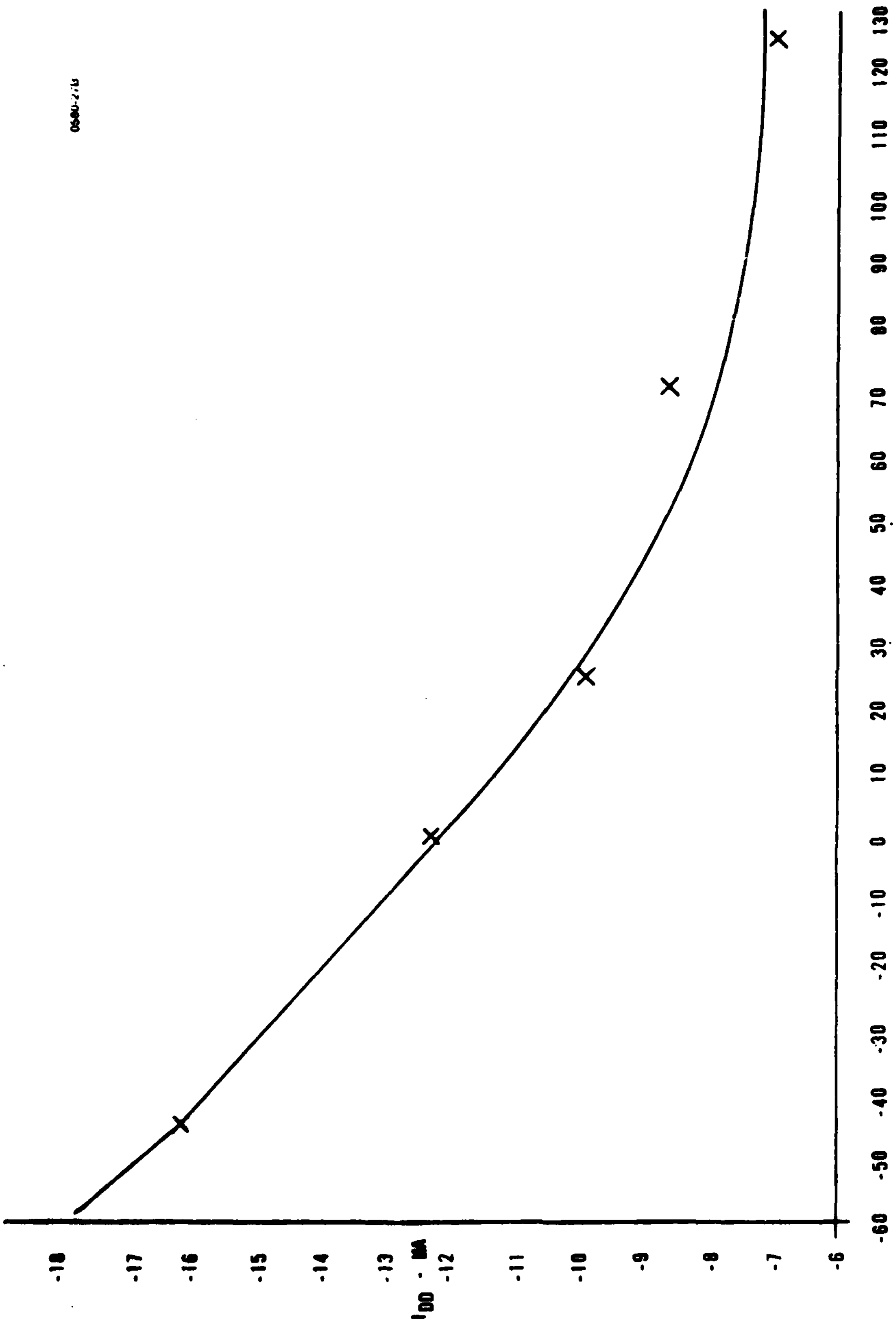


FIGURE 6-23. 7053 V_{DD} SUPPLY CURRENT (I_{DD})
VENDOR SPEC: -25 MA

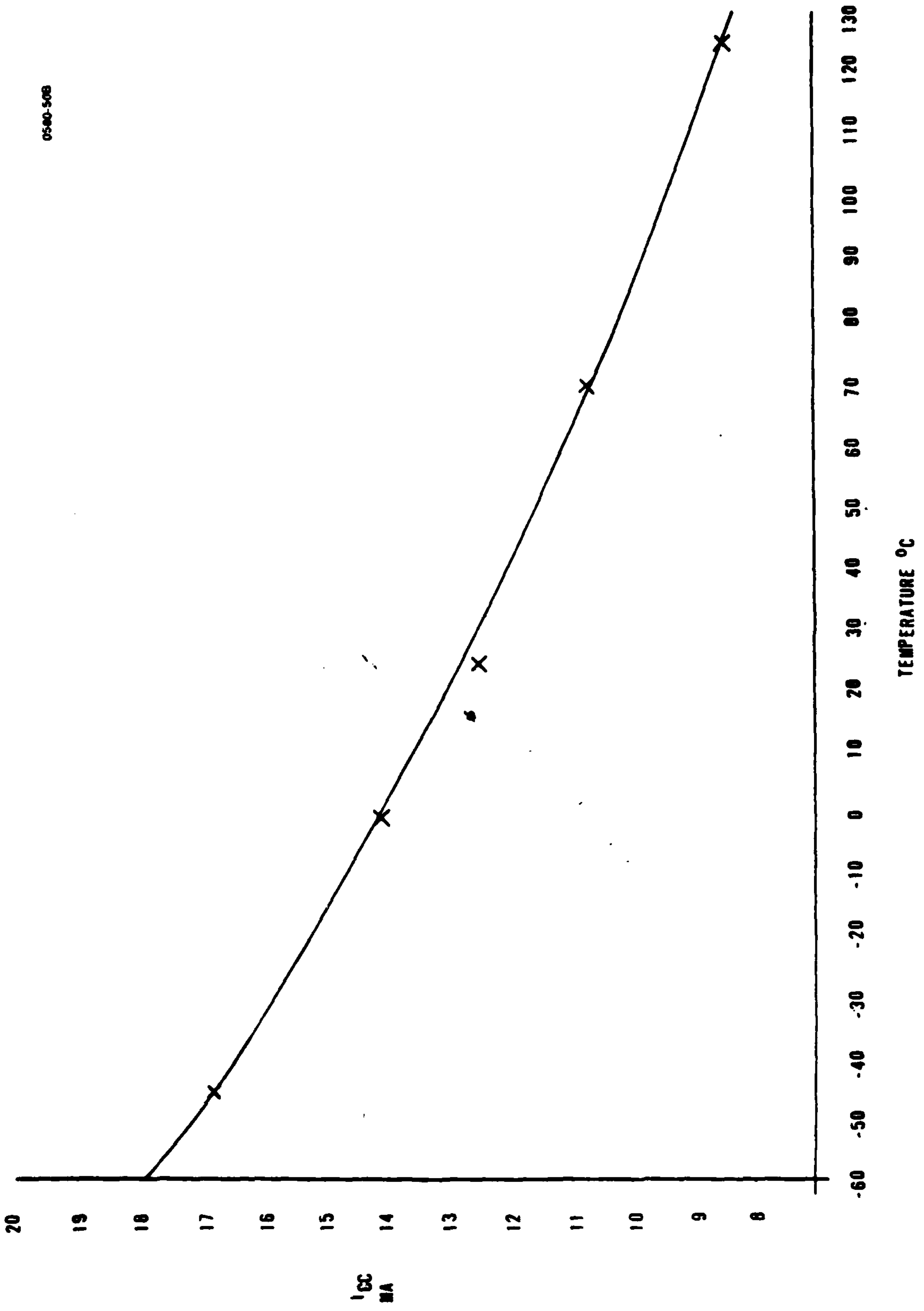


FIGURE 6-24. 7053 V_{CC} SUPPLY CURRENT (I_{CC})
VENDOR SPEC: 30 MA MAXIMUM CHIP SELECTED

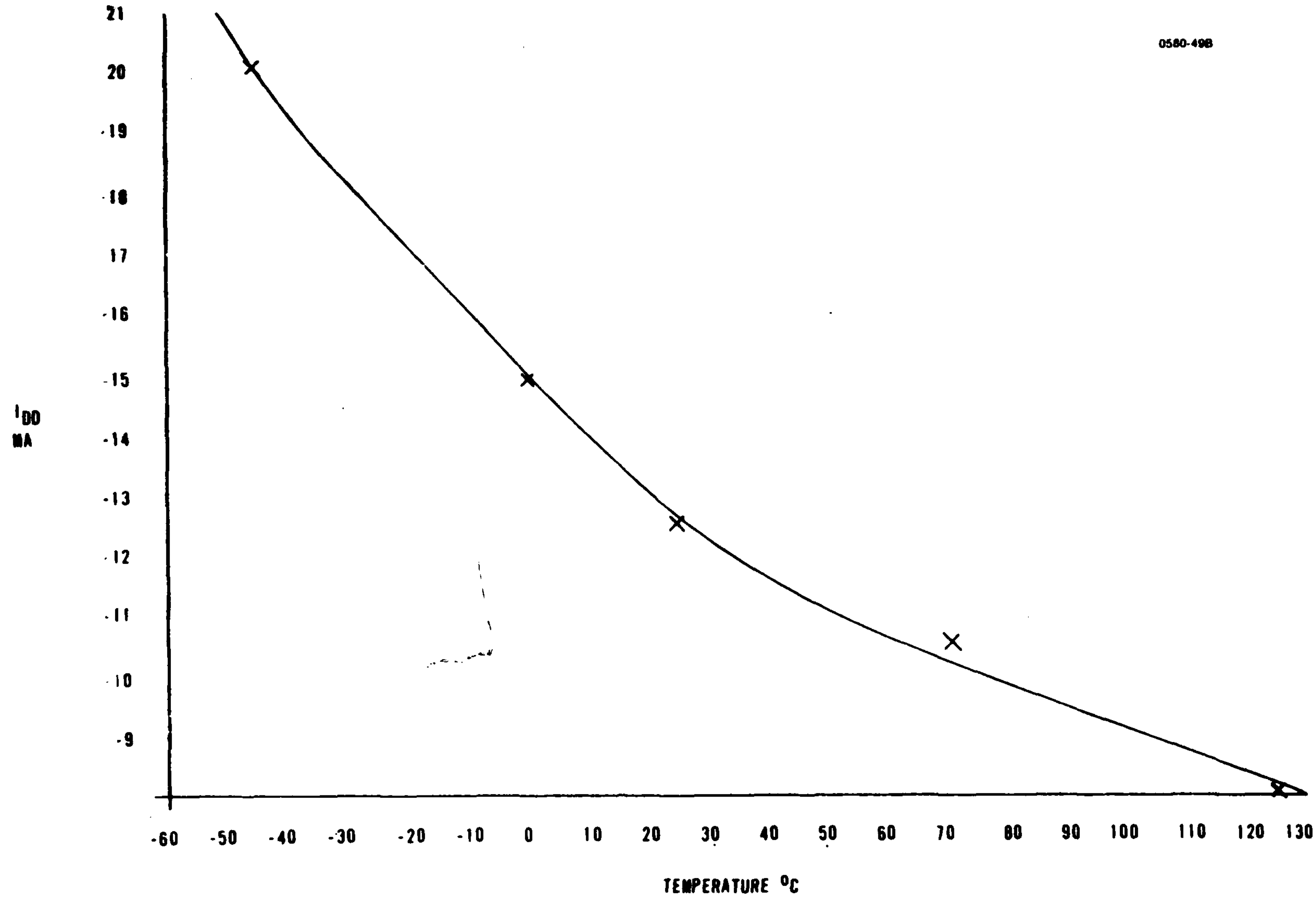


FIGURE 6-25. 2451 V_{DD} SUPPLY CURRENT (I_{DD})
VENDOR SPEC: -25 MA MAXIMUM CHIP SELECTED

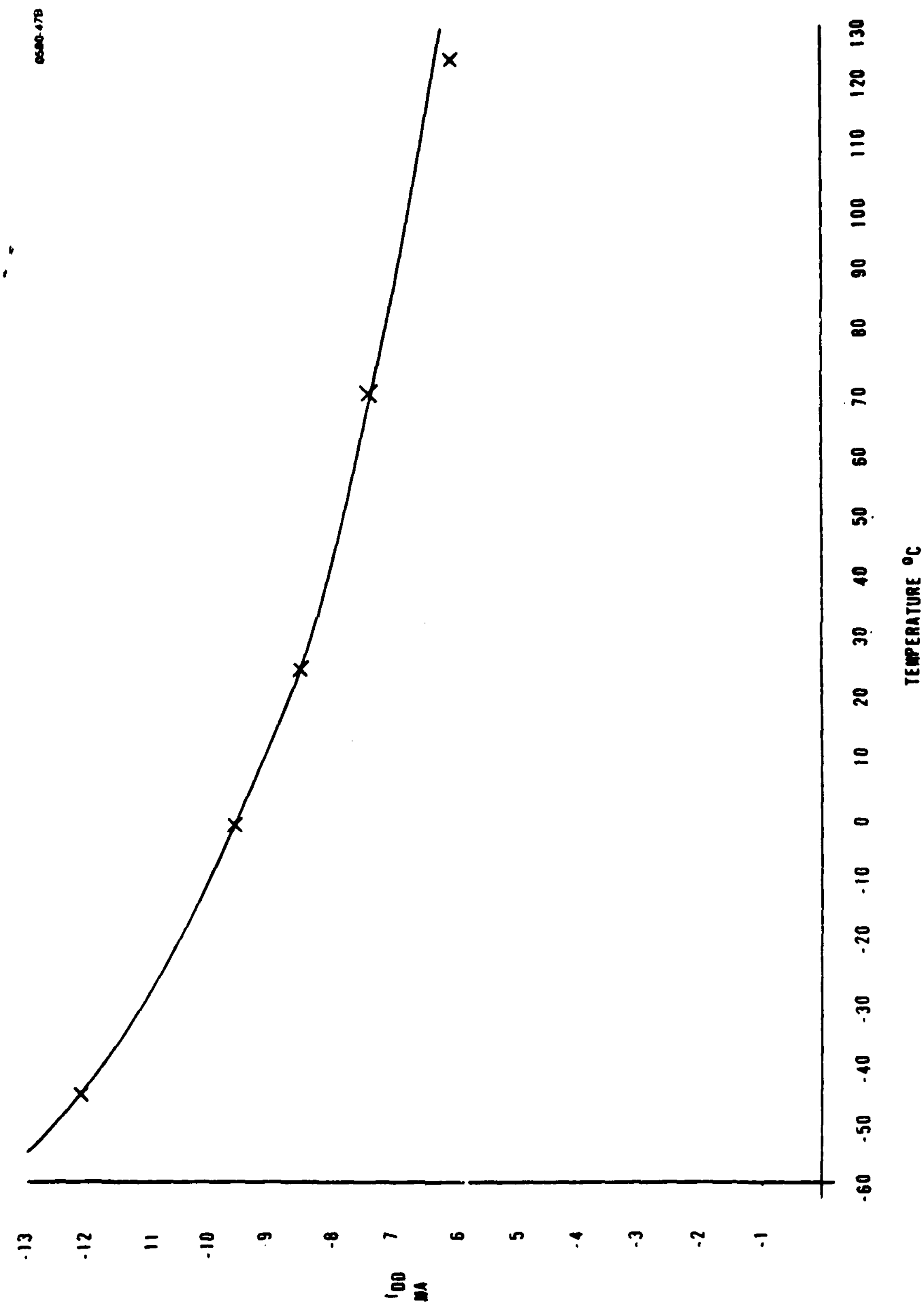


FIGURE 6-26. 2451 V_{DD} SUPPLY CURRENT (I_{DD})
VENDOR SPEC: -25 MA MAXIMUM CHIP DESELECTED

6.2.3.4 Input Load Current

Vendor data for this parameter was specified for the 7053 device type only. For this reason, only the 7035's were tested for this parameter; therefore, no comparison can be made to other devices. The 7053 met the vendor specification at all temperatures on all inputs except the E input. (See Table 6.1).

6.2.4 Conclusions

The vendor specification values for input and output leakage currents seem to be highly conservative ratings. These parameters will be studied in more detail in selected device testing to determine a suitable value to expect without affecting yield.

In cooperation with NCR personnel, the relationship between nitride thickness and endurance (erase/write cycling) was investigated to determine if a practical screening method could be devised. One method suggested by NCR is the measurement of erase substrate leakage current which is inversely related to nitride thickness and hence, endurance. In this way, devices could be graded according to leakage current, in addition to other methods, as having a relatively thick nitride (high endurance) or thin nitride (low endurance). The minimum and maximum current values in addition to the average currents are shown for the 2810 and 2401 types in Tables 6.3 and 6.4 respectively. Erase substrate leakage current can only be measured on these two block erase type devices. According to the data, the 2401 device had lower average leakage currents than the 2810 device. This would tend to indicate that the 2401 has superior endurance characteristics. However, due to the small data base and the large variation of nitride thickness among lots, and within the same lot, further testing with devices from many lots would aid in forming a more definite conclusion. This test will be used for final device characterization to eliminate relatively thin nitride parts. Other endurance tests are covered in the dynamic test section of the MACI preselection report.

In summary, the best device for performance to vendor specifications over the full military temperature range is the 2810 followed by the 2401, 2451/3400 and the 7053, respectively. The 2401 has better endurance characteristics than the 2810, but as mentioned, this conclusion is not totally reliable. All devices met the vendor specifications for power supply currents, however, the 2810 device requires less current per bit followed by the 2401 device. This is demonstrated in the dynamic performance section of the MACI preselection report.

According to dc parameters, the 2810 device type performance is superior to the other tested device types. In order of decreasing performance, the other types chosen are 2401, 2451/3400 and 7053.

6.3 Radiation Resistance

Flash X-Ray testing of all candidate devices was shown in the First Interim Report.

The earlier results of the radiation resistance tests of the MNOS devices showed their performance under flash X-Ray at high dose rates (ie: 1.4 x 10 Rds Sc/Sec/20 ns). Some results from internal Honeywell work and MACI associated tests are shown in Tables 6-4, 6-5, and 6-6. These three tables show GI ER3400 devices (Tables 6-4 and 6-5 in Plastic DIP and Table 6-6 in Ceramic) operated in a normal retention test mode with periodic exposures to varying doses of radiation from a CO.60 source. At the end of 50K rads of total dose, the device was operated at +85°C after storing data for 1.63 x 10^6 seconds. The threshold margins were still in the order of 3 volts.

Figures 6-27 through 6-30 show the plastic devices plotted against time with the total dose exposures shown. While the threshold shows a negative shift in threshold, the reference voltage also shifts correspondingly. The results show little degradation in the retention time due to the 50K rad exposure.

Figures 6-31 through 6-34 show ceramic devices with one exposure to 5K rads. Some problems developed in the devices which were traceable to the lot. The design changed after these devices were built to that of the devices in the plastic DIPs.

Figures 6-35 through 6-42 show schmoo's of the radiated devices taken in the following ways:

- Without rewriting,
- Rewritten.

Figures 6-43 and 6-44 are schmoo's of a similar device unradiated and used as a control device.

These results show that even after 50K rads exposure, these devices operate at room and +85°C close to their specifications. Using this data, a system could be designed using the shifted parameter data to operate in excess of 5 x 10^4 rads.

TABLE 6-4. CO_{60} TESTS 3400 PLASTIC

	No. 1			No. 3			No. 4		
	11-16-79 Write @13:43:00			11-16-79 Write @13:53:00			11-16-79 Write @13:56:00		
	TIME (Sec.)	V_0	V_1	TIME (Sec.)	V_0	V_1	TIME (Sec.)	V_0	V_1
1	10	-15	-7.70	10	-15	-6.74	10	-14.44	-6.40
2	70	-15	-7.70	77	-15	-6.80	70	-13.98	-6.42
3	495	-15	-7.70	500	-15	-6.86	495	-13.58	-6.44
4	3,657	-14.10	-7.70	3,487	-14.50	-6.92	3,493	-13.18	-6.48
5	240,540	-13.26	-7.76	239,940	-13.58	-7.06	239,820	-12.38	-6.59
6	347,040	-13.18	-7.78	346,560	-13.52	-7.08	346,440	-12.30	-6.56
	11-20-79	1st Dose = 5K Rad							
7	358,440	-13.28	-7.92	357,900	-13.66	-7.24	352,780	-12.50	-6.80
8	439,020	-13.02	-7.88	438,420	-13.60	-7.22	438,300	-12.44	-6.80
9	844,380	-12.96	-7.92	843,900	-13.50	-7.26	843,920	-12.34	-6.82
	11-27-79	2nd Dose = 15K Rad							
10	1,035,700	-13.36	-8.40	1,025,160	-13.88	-7.76	1,021,040	-12.90	-7.58
11	1,219,740	-13.26	-8.38	1,219,140	-13.76	-7.78	1,219,140	-12.84	-7.60
	12-3-79	3rd Dose = 15K Rad							
12	1,453,440	-13.60	-8.86	1,452,840	-14.06	-8.28	1,452,720	-13.38	-8.40
13	1,563,780	-13.60	-8.88	1,563,240	-14.08	-8.30	1,563,120	-13.32	-8.02
	14-4-79	4th Dose = 15K Rad							
14	1,573,630	-14.12	-9.56	1,573,080	-14.56	-9.02	1,572,960	-14.04	-9.06
	12-5-79	Heat at 85°C 2 hour							
15	1,634,400	-13.68	-9.52	1,633,800	-14.12	-8.98	1,633,630	-13.64	-9.58

	V_R	V_R	V_R
Initial 11-8-79	-10.33	-10.15	-9.82
Post 1st Dose	-9.96	-9.82	-9.52
Post 2nd Dose	-10.26	-10.18	-10.09
Pre 3rd Dose	-10.26	-10.18	-10.09
Post 3rd Dose	-10.48	-10.44	-10.47
D - 4th Dose	-10.48	-10.44	-10.47

TABLE 6-5. CO_{60} TESTS 3400 PLASTIC

	No. 5 11-16-79 Write @13:58:30 TIME (Sec.)	V_0	V_1	No. 6 11-16-79 Write @14:11:00 TIME (Sec.)	V_0	V_1
1	10	-14.38	-6.52	10	-15	-7.28
2	70	-14.08	-6.54	75	-15	-7.32
3	555	-13.58	-6.54	495	-14.68	-7.36
4	3,487	-13.24	-6.58	3,487	-14.26	-7.40
5	239,670	-12.40	-6.62	238,980	-13.40	-7.50
6	346,380	-12.34	-6.64	345,660	-13.34	-7.52
	11-20-79 1st Dose = 5K Rad					
7	357,690	-12.46	-6.86	357,060	-13.48	-7.72
8	438,150	-12.38	-6.84	437,460	-13.42	-7.72
9	843,630	-12.28	-6.86	842,880	-13.30	-7.74
	11-27-79 2nd dose = 15K Rad					
10	1,024,950	-12.60	-7.44	1,024,200	-13.66	-8.32
11	1,218,870	-12.48	-7.46	1,218,180	-13.48	-8.30
	12-3-79 3rd Dose = 15K Rad					
12	1,452,570	-12.80	-8.00	1,451,820	-13.84	-8.86
13	1,562,970	-12.78	-8.02	1,562,280	-13.80	-8.88
	12-4-79 4th Dose = 15K Rad					
14	1,572,810	-13.20	-8.66	1,572,120	-14.18	-9.56
	12-5-79 Heat at 85°C 1 hour					
15	1,633,530	-12.64	-8.62	1,632,840	-13.64	-9.54

	V_R	V_R
Initial 11-8-79	-10.18	-10.06
Post 1st Dose	-9.84	-9.72
Post 2nd Dose	-10.14	-10.02
Pre 3rd Dose	-10.13	-10.02
Post 3rd Dose	-10.36	-10.25
Pre 4th Dose	-10.36	-10.25

TABLE 6-6. CO_{60} TESTS 3400 PLASTIC

	No. 201			No. 203			No. 221		
	11-16-79 Write @13:22:00			11-16-79 Write @13:25:00			11-16-79 Write @13:28:00		
	TIME (Sec.)	V_0	V_1	TIME (Sec.)	V_0	V_1	TIME (Sec.)	V_0	V_1
1	10	-13.62	-7.72	10	-13.94	-7.72	10	-13.74	-8.80
2	70	-13.34	-7.72	70	-13.66	-7.74	70	-13.40	-8.72
3	510	-12.98	-7.74	495	-13.30	-7.74	495	-13.08	-8.70
4	3,414	-12.60	-7.74	3,487	-12.92	-7.72	3,487	-12.6	-8.66
5	241,920	-11.86	-7.76	241,740	-12.22	-7.78	241,680	-11.94	-8.62
6	348,600	-11.80	-7.85	348,480	-12.16	-7.78	348,360	-11.98	-8.62
	11-20-79 1st Dose = 5K Rad								
7	Shorted on Fixture			359,880	-12.44	-8.18	359,760	-12.30	-9.04
8				ERASED,	RESTARTED	TEST	440,160	-12.22	-9.02
9				1 10	-14.22	-8.10	845,580	-12.14	-9.02
				2 70	-13.04	-8.10			
				3 495	-12.52	-8.10			
				4 403,140	-12.10	-8.12			
	11-27-79 2nd Dose = 15K Rad								
10				NO TEST			1,030,320	-13.22	-10.56

	No. 201 V_R	No. 203 V_R	No. 221 V_R
Initial 6-13-79	-9.08	-9.97	-9.60
Post 1st Dose	-	-10.14	-9.87
Post 2nd Dose	-	-10.58	-10.56

A room temperature fast specification (ie: Ta $\leq$ 850 ns @ V_{DD} = -13 V_{dc} ±5%) is superimposed on the +25°C schmoo's to show the margin after exposure to 50K rads. The normal specification for 0 to +70°C operation is superimposed on the +85°C schmoo's showing the post-rad performance in relationship to that specification.

This testing was performed on the final device selected for delivery to ERADCOM (ER3400/NCR2451) to further define its operation in the military environment.

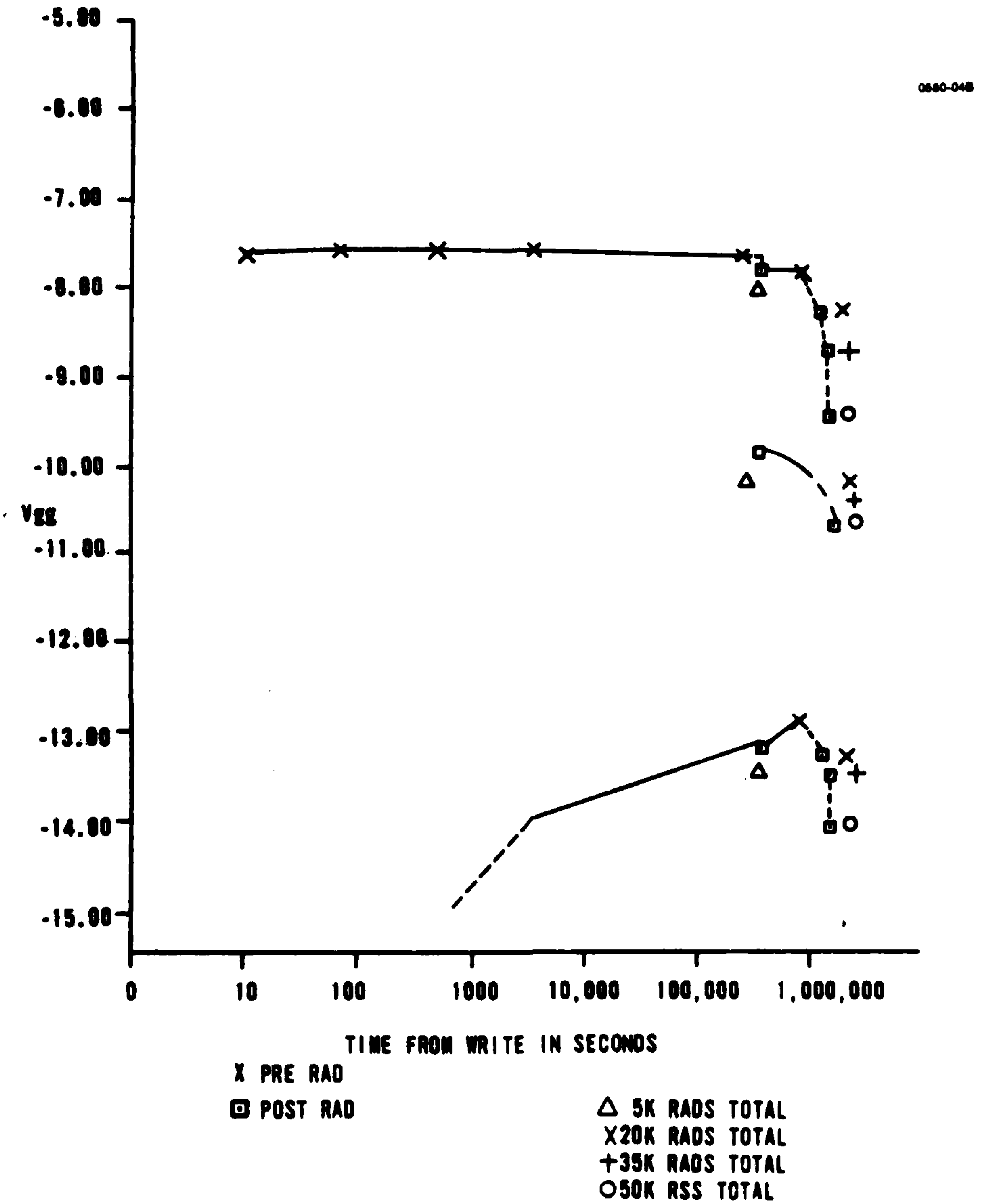


FIGURE 6-27. TOTAL DOSE VERSUS V_T

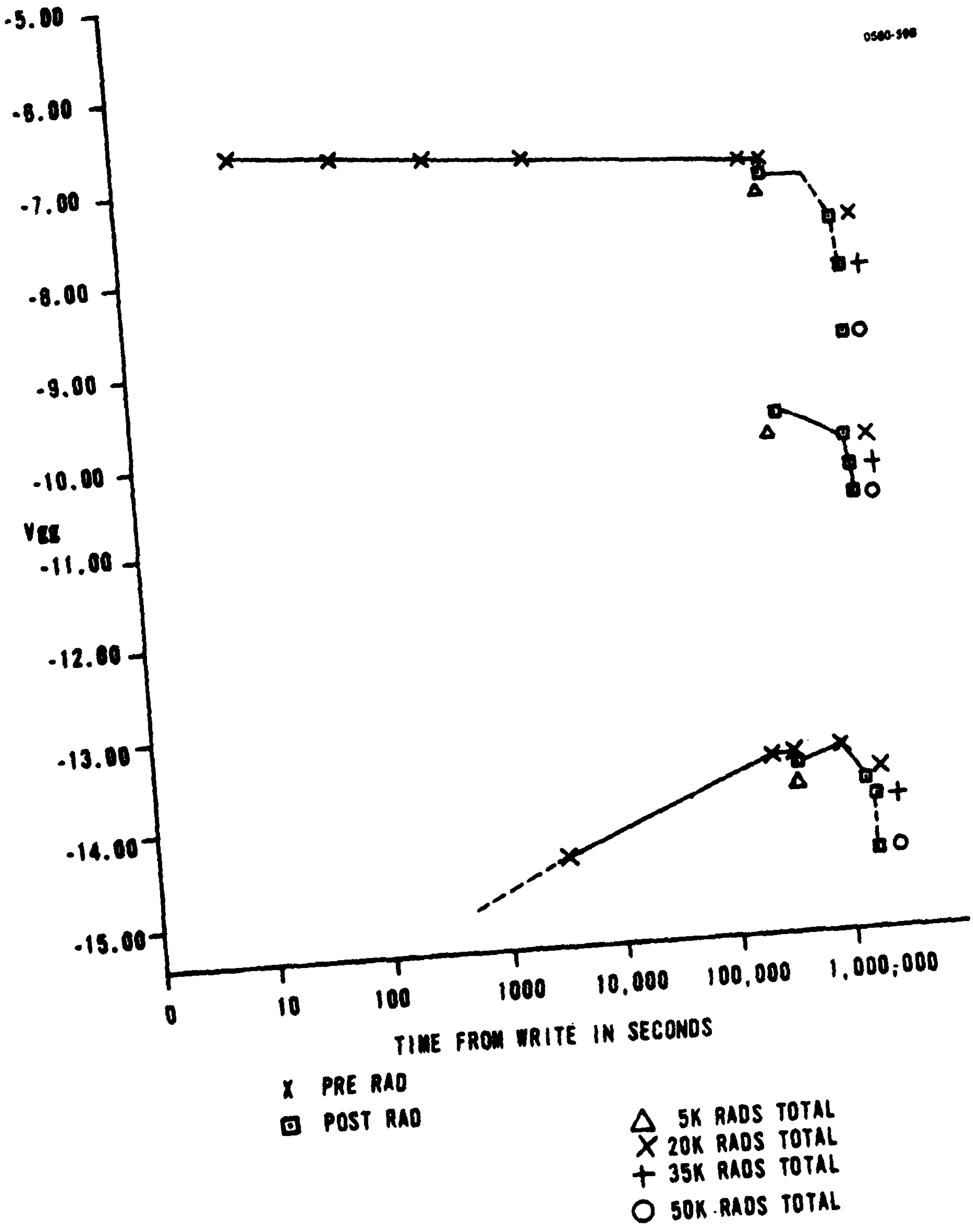


FIGURE 6-28. V_T VERSUS TOTAL DOSE 3400 NO. 3

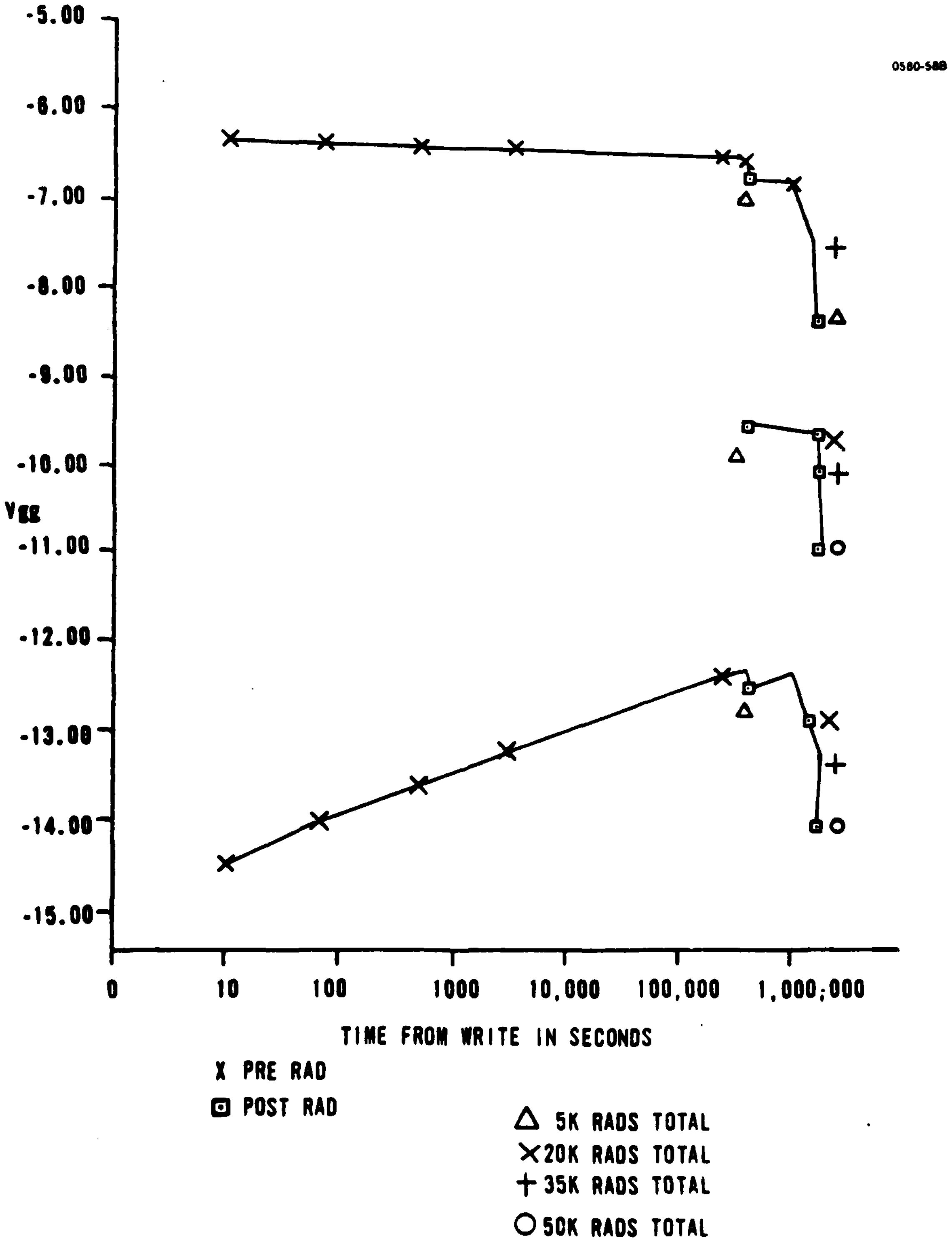


FIGURE 6-29. V_T VERSUS TOTAL DOSE 3400 NO. 4

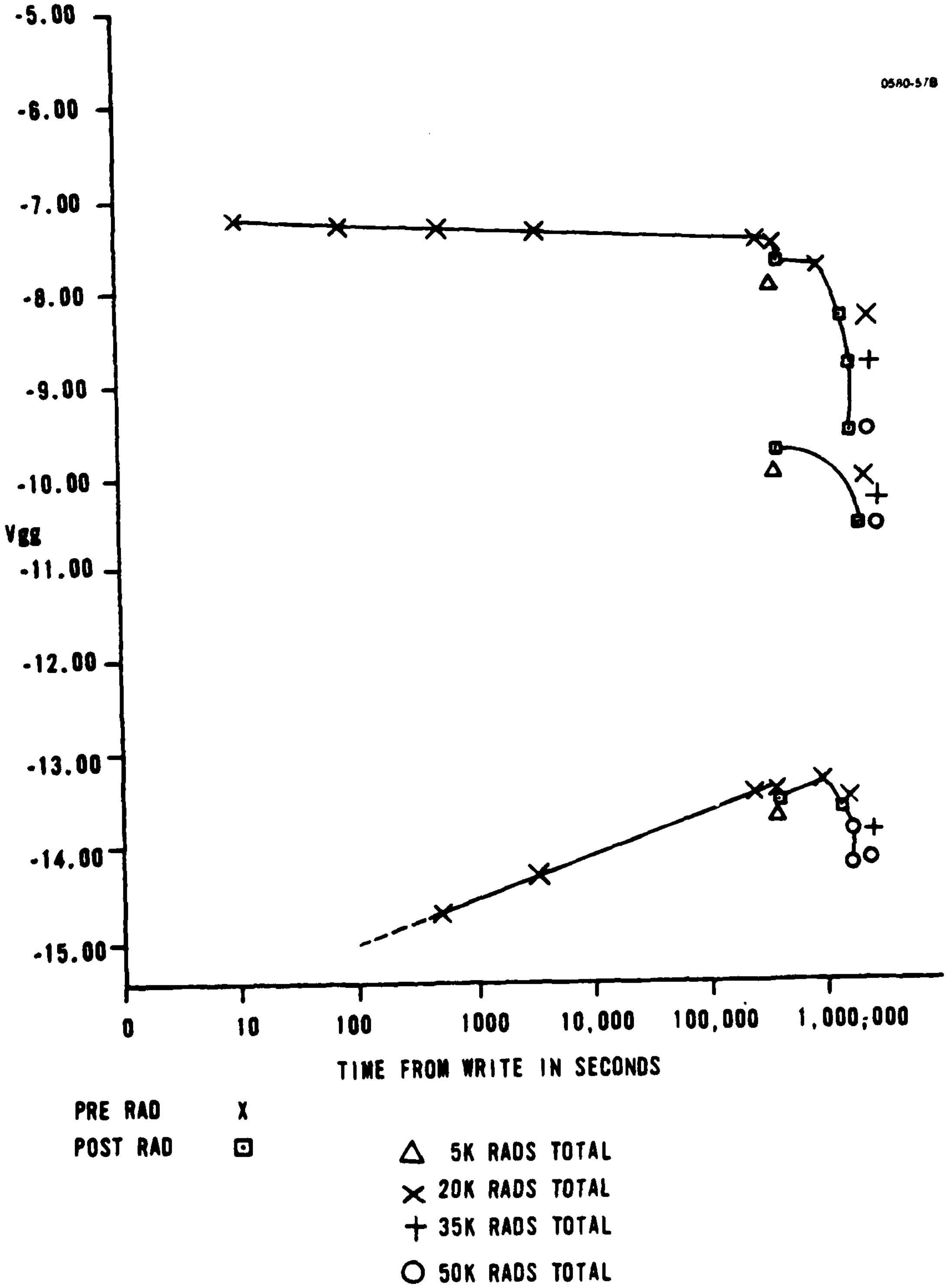


FIGURE 6-30. TOTAL DOSE 3400 NO. 6

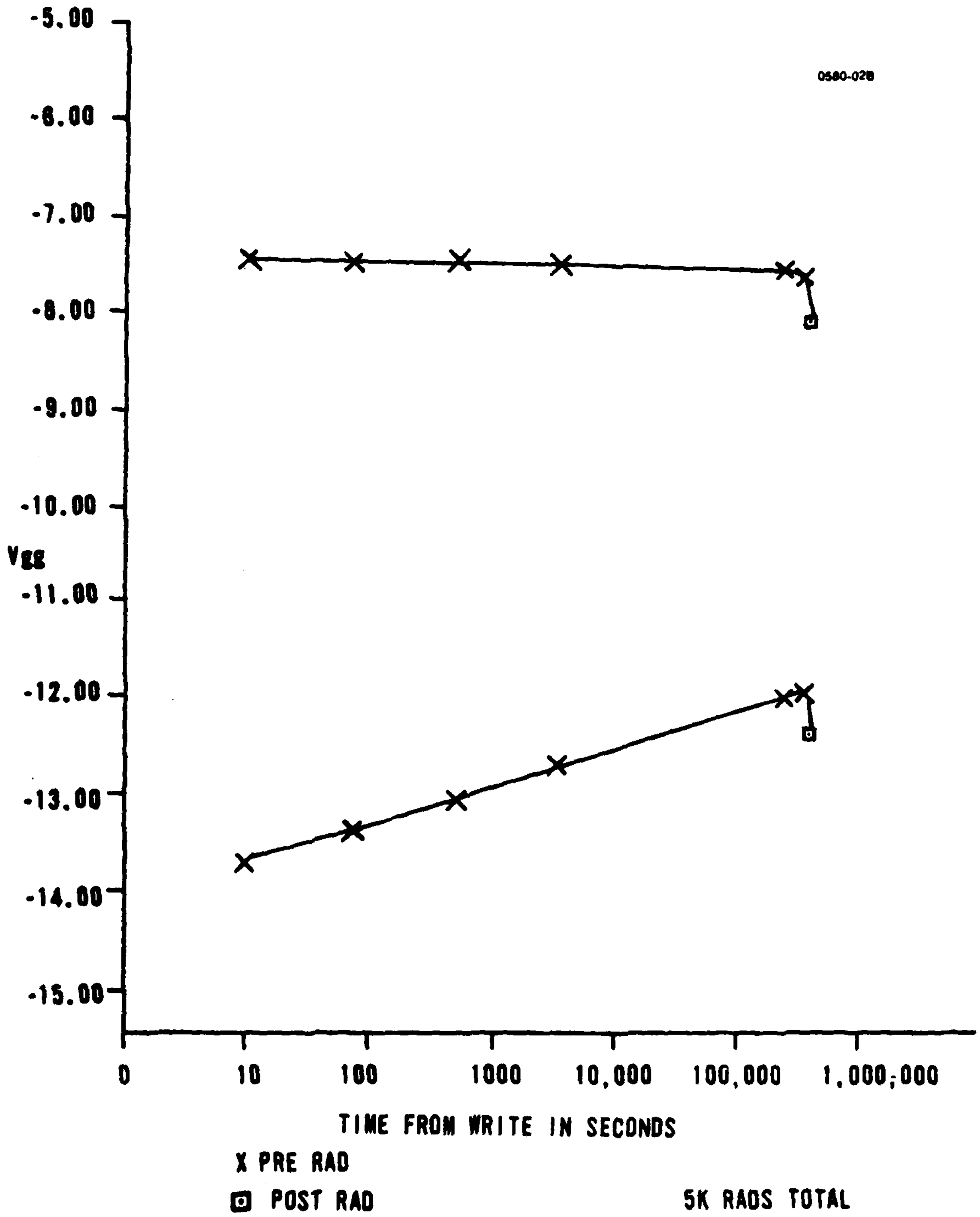


FIGURE 6-31. TOTAL DOSE 3400 NO. 229

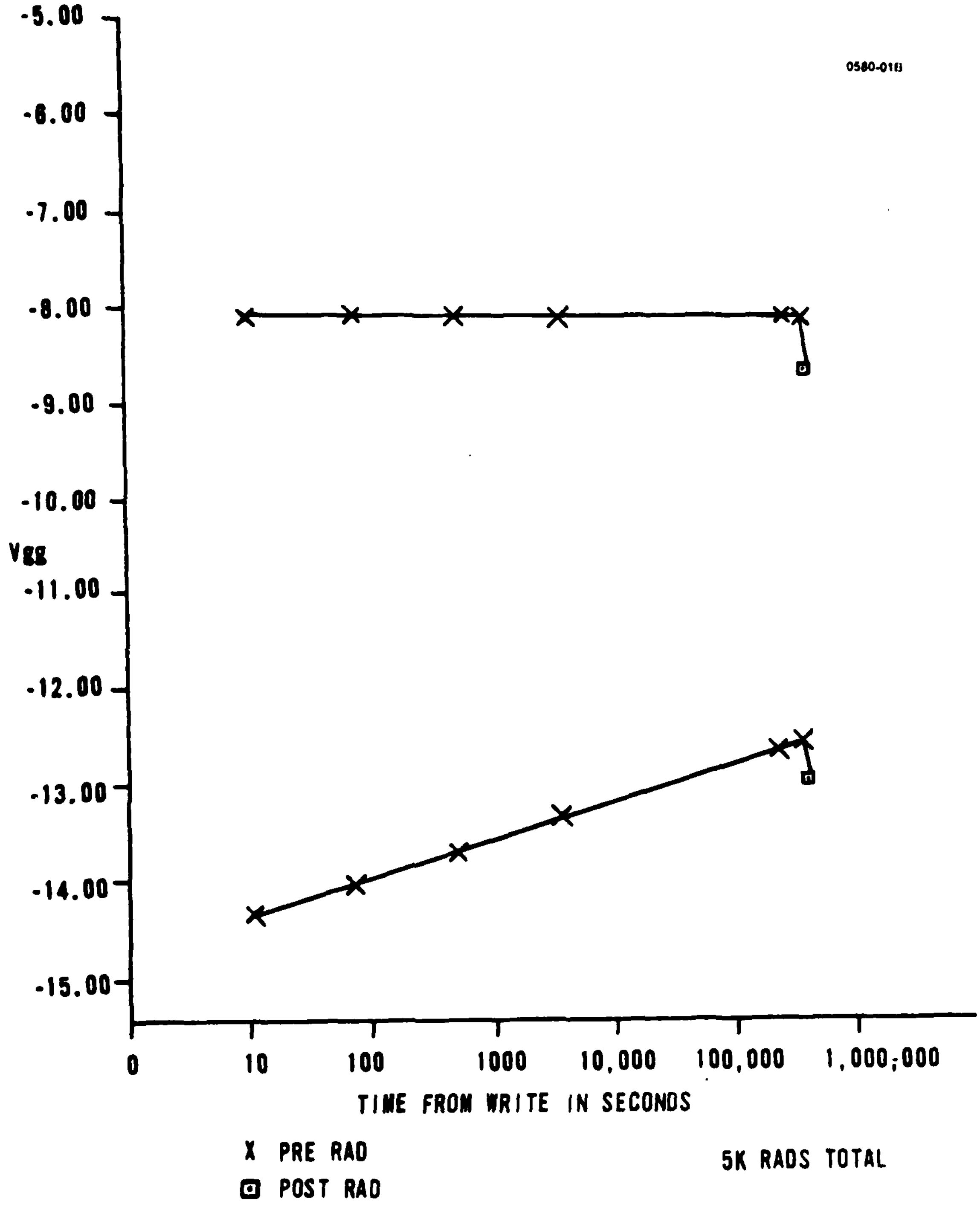


FIGURE 6-32. V_T VERSUS TOTAL DOSE 3400 NO. 228

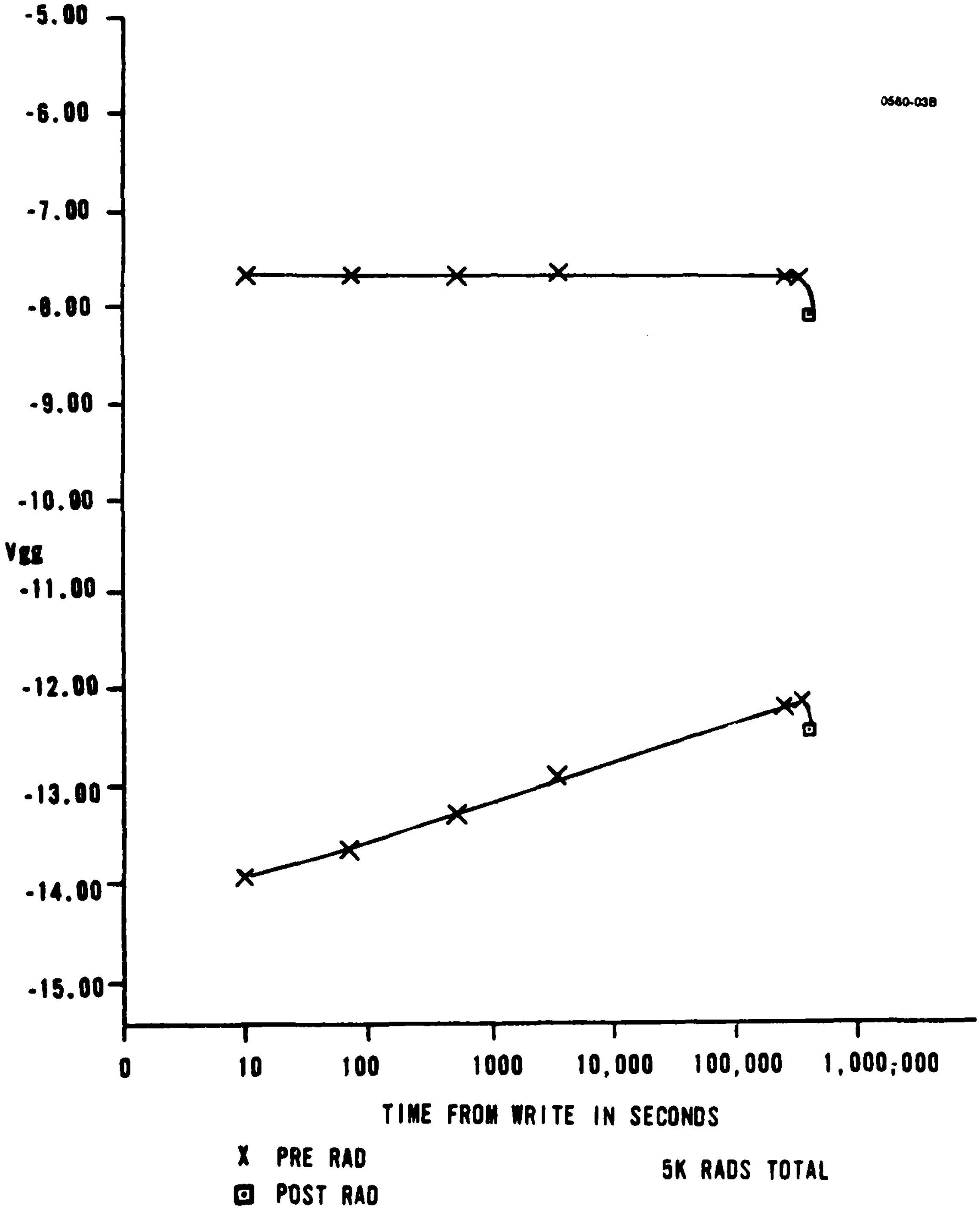


FIGURE 6-33. V_T VERSUS TOTAL DOSE 3400 NO. 203

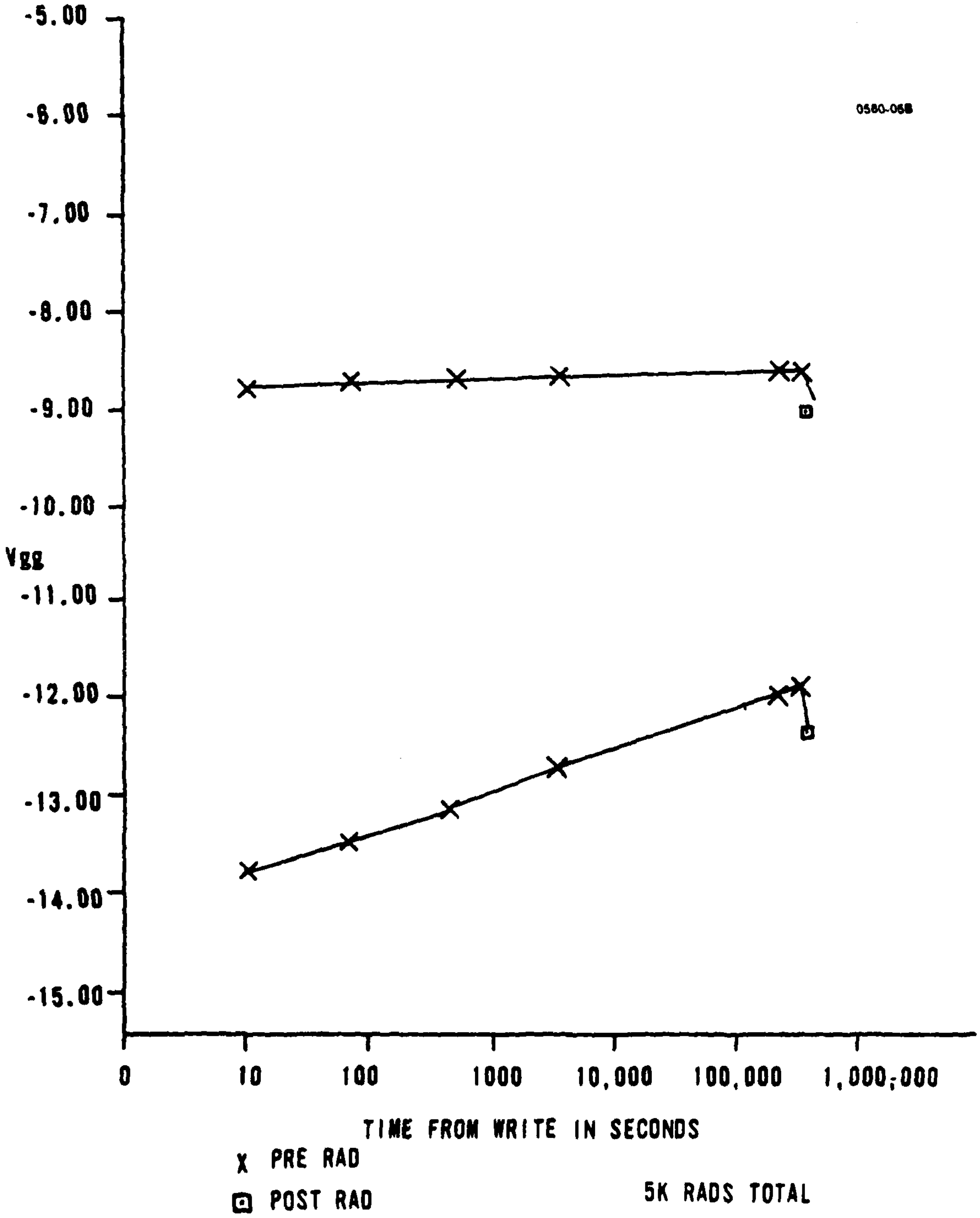


FIGURE 6-34. V_T VERSUS TOTAL DOSE 3400 NO. 221

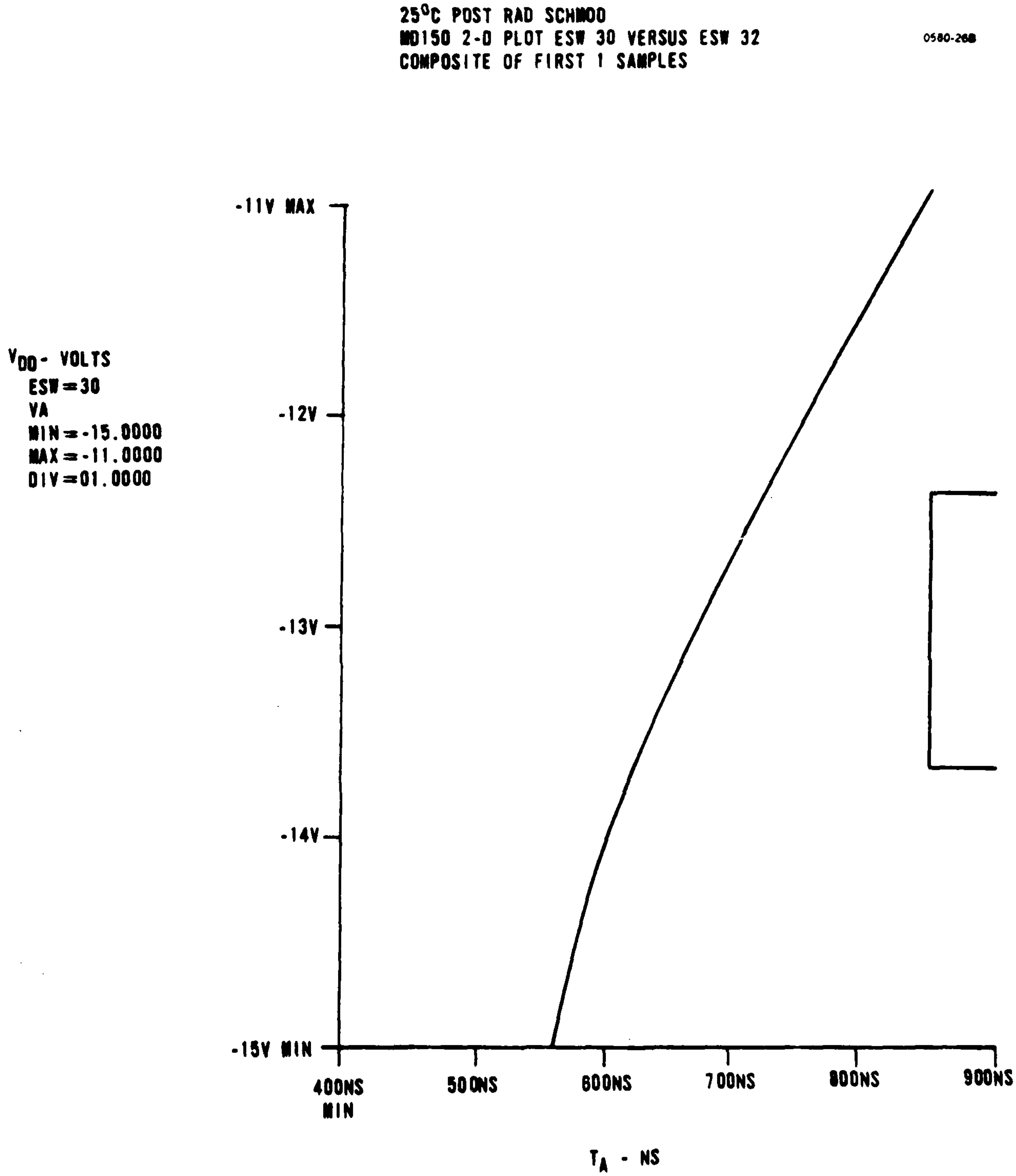


FIGURE 6-35. 3400 NO.3 25°C POST RAD SCHMOO

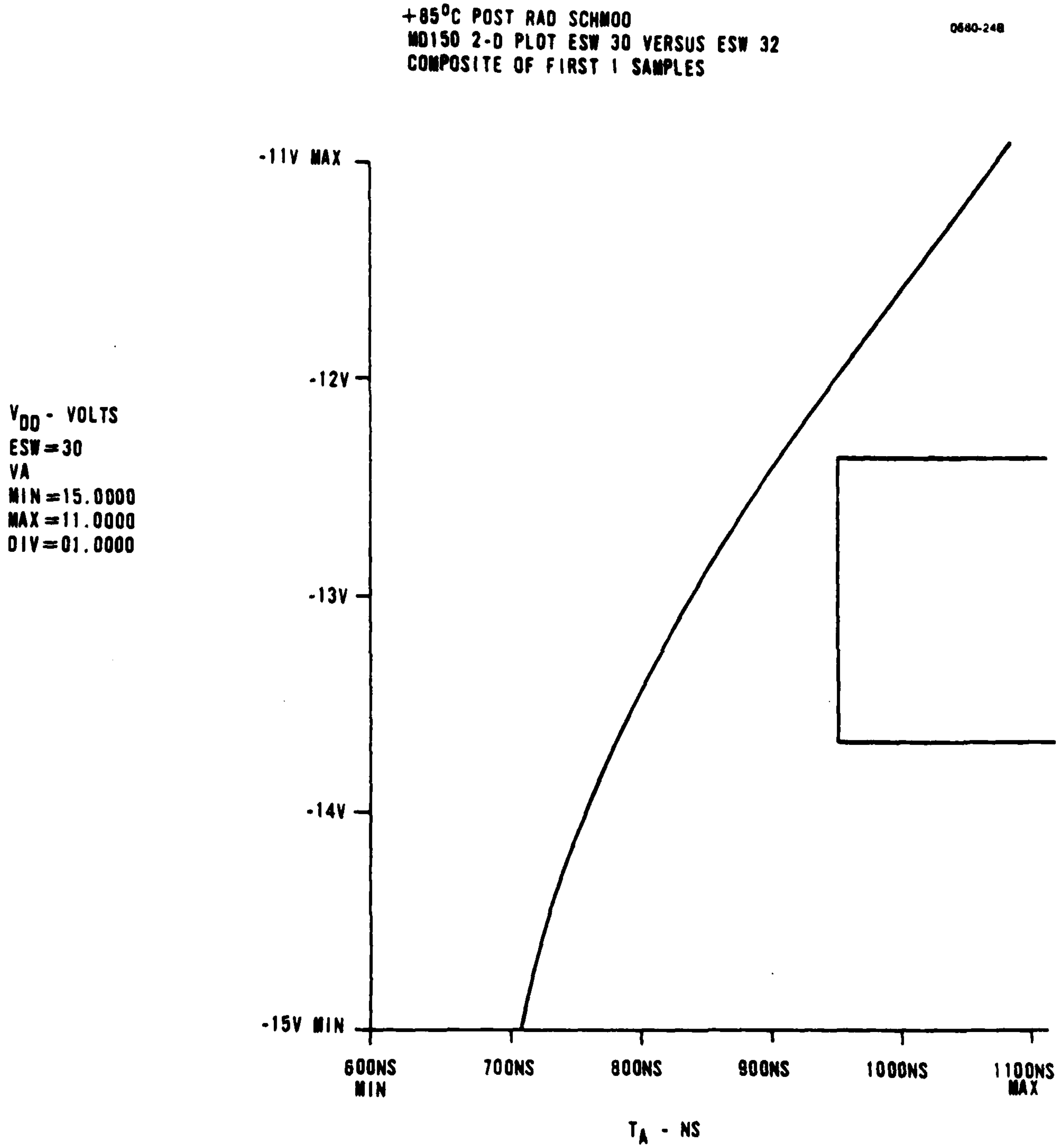


FIGURE 6-36. ER 3400 NO.3 +85°C POST RAD SCHMOO

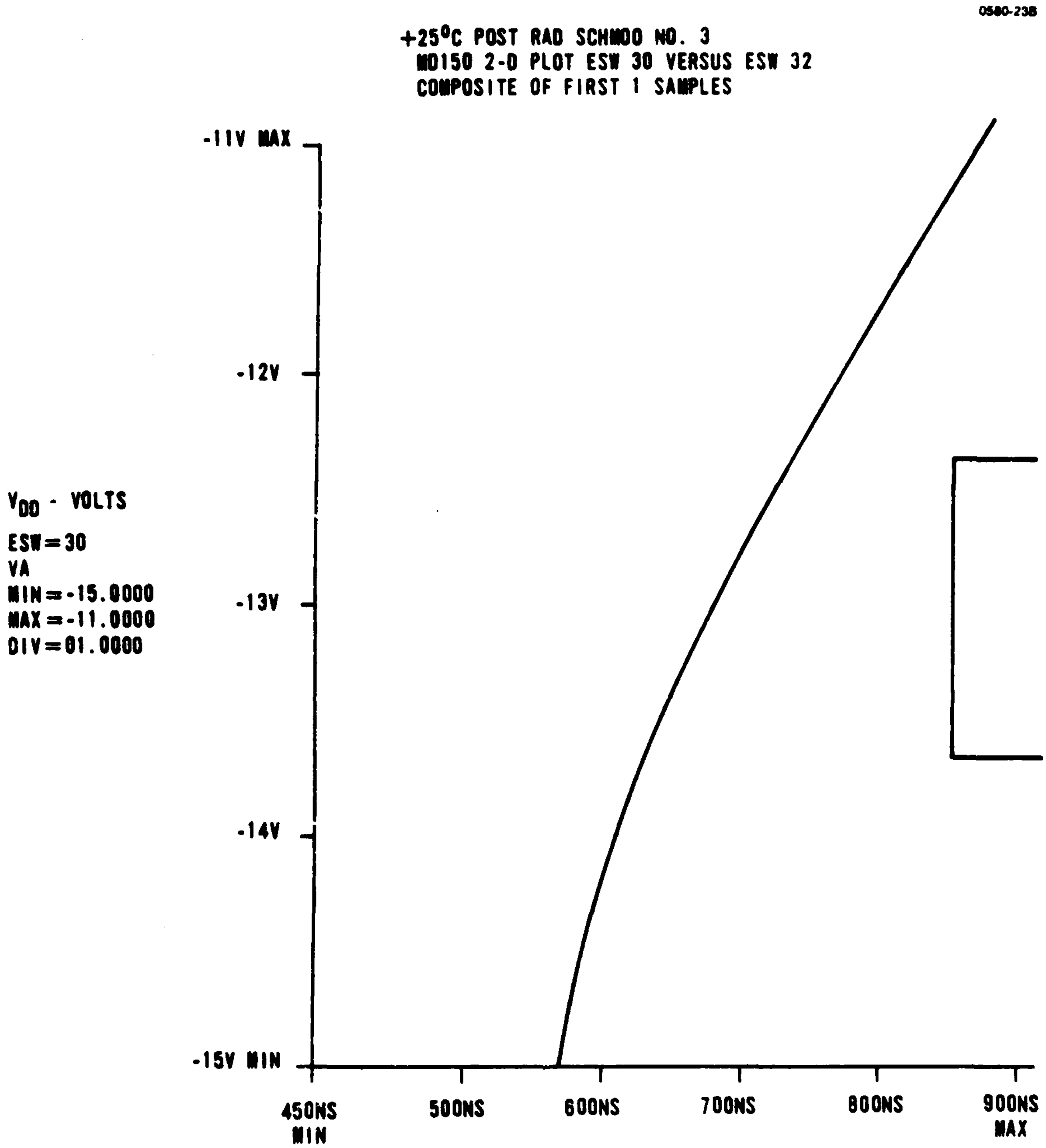


FIGURE 6-37. 3400 NO.3 +25°C POST RAD SCHMOO NO. 3

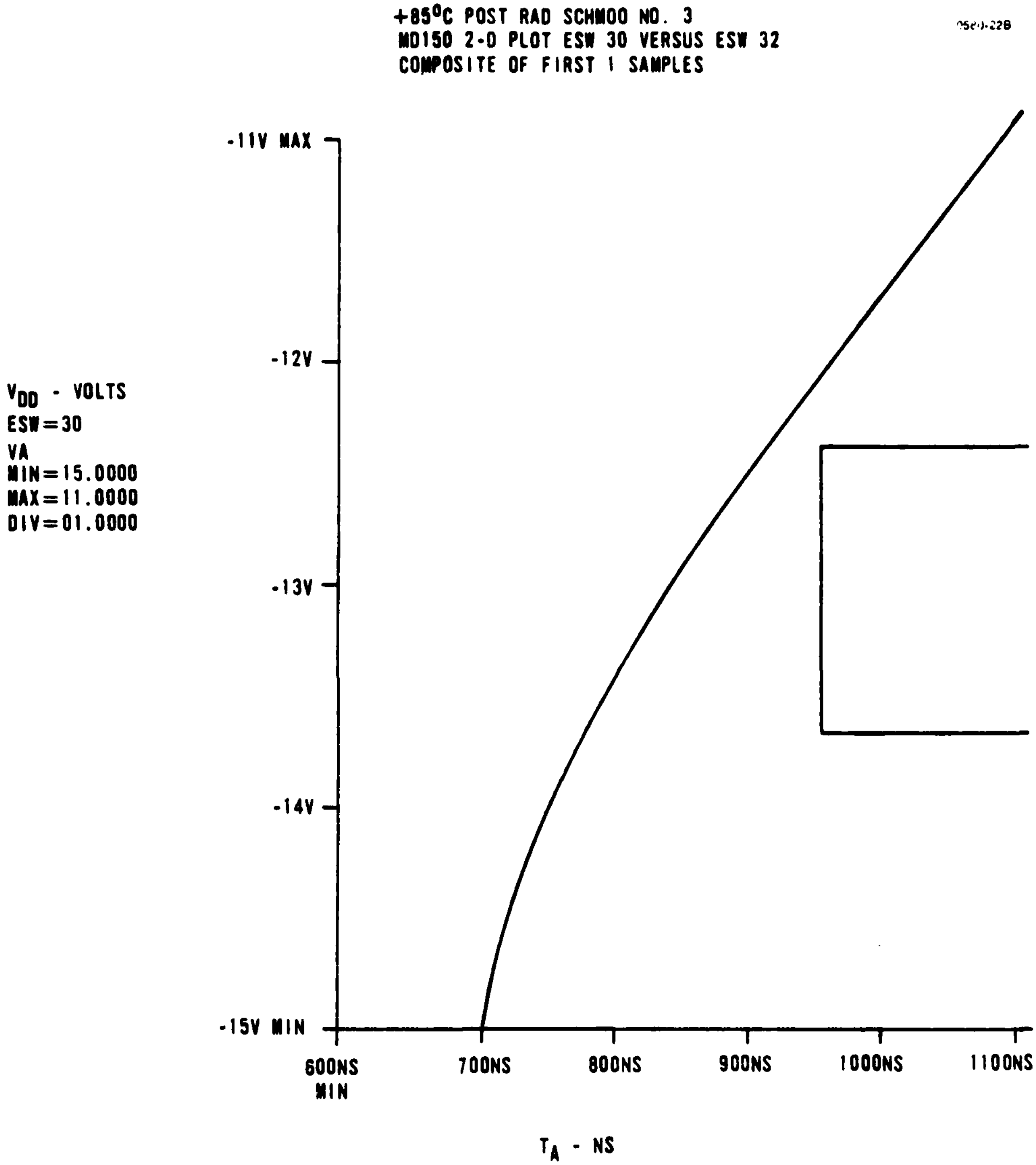


FIGURE 6-38. 3400 NO.3 +85°C POST RAD SCHMOO NO. 3

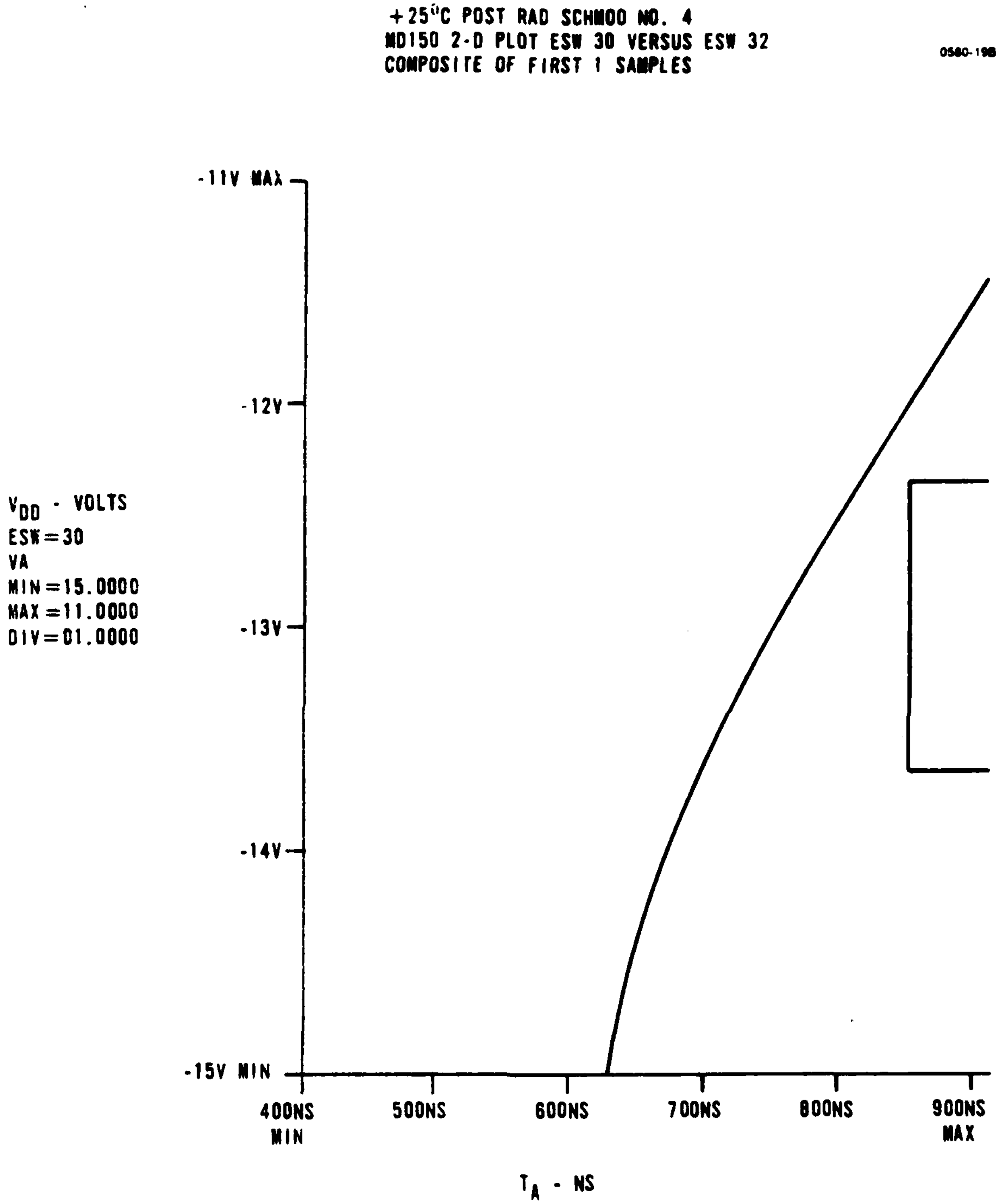


FIGURE 6-39. ER 3400 NO.4 +25°C POST RAD SCHMOO NO. 4

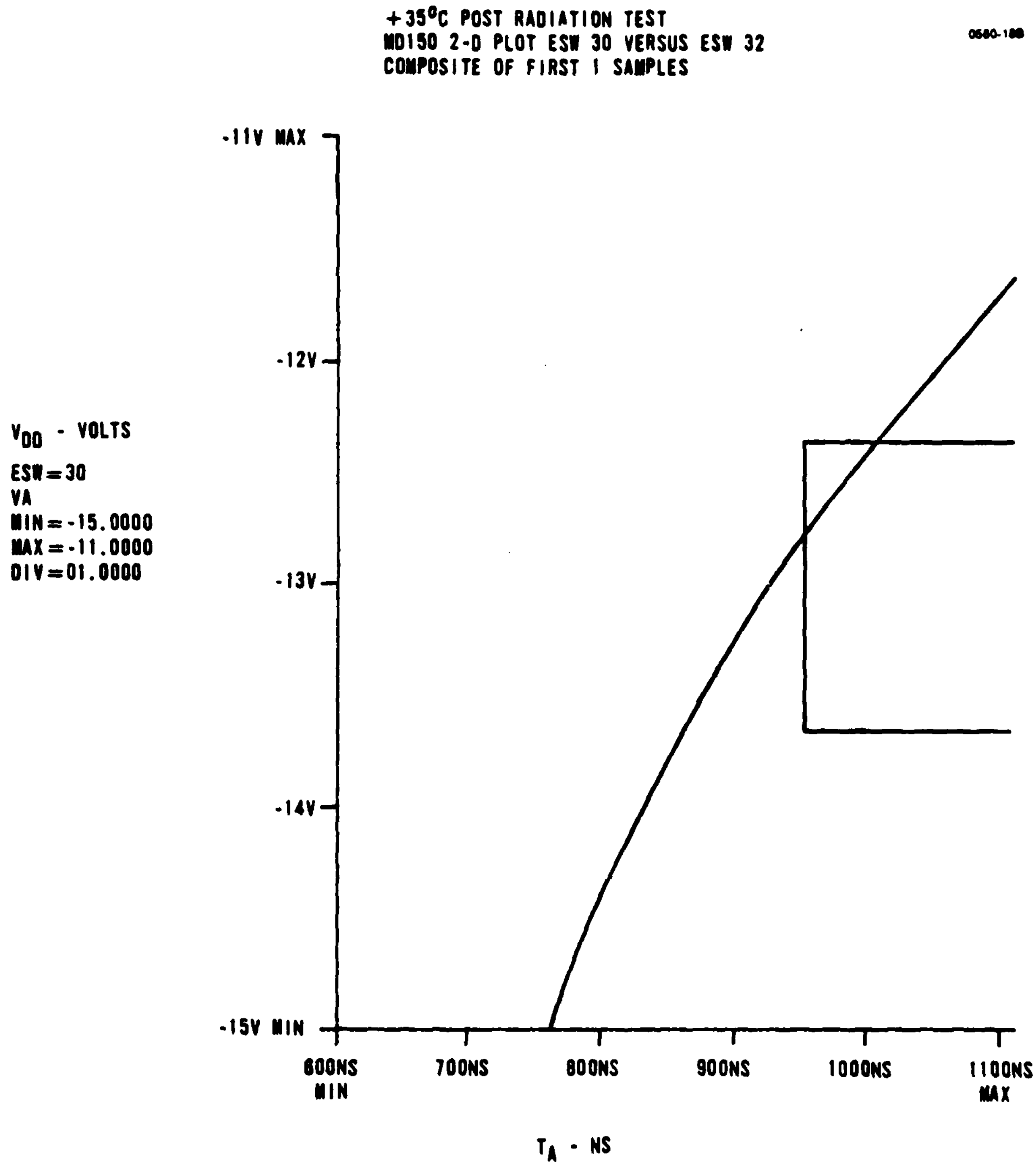


FIGURE 6-40. ER 3400 NO.4 +85°C POST RADIATION TEST

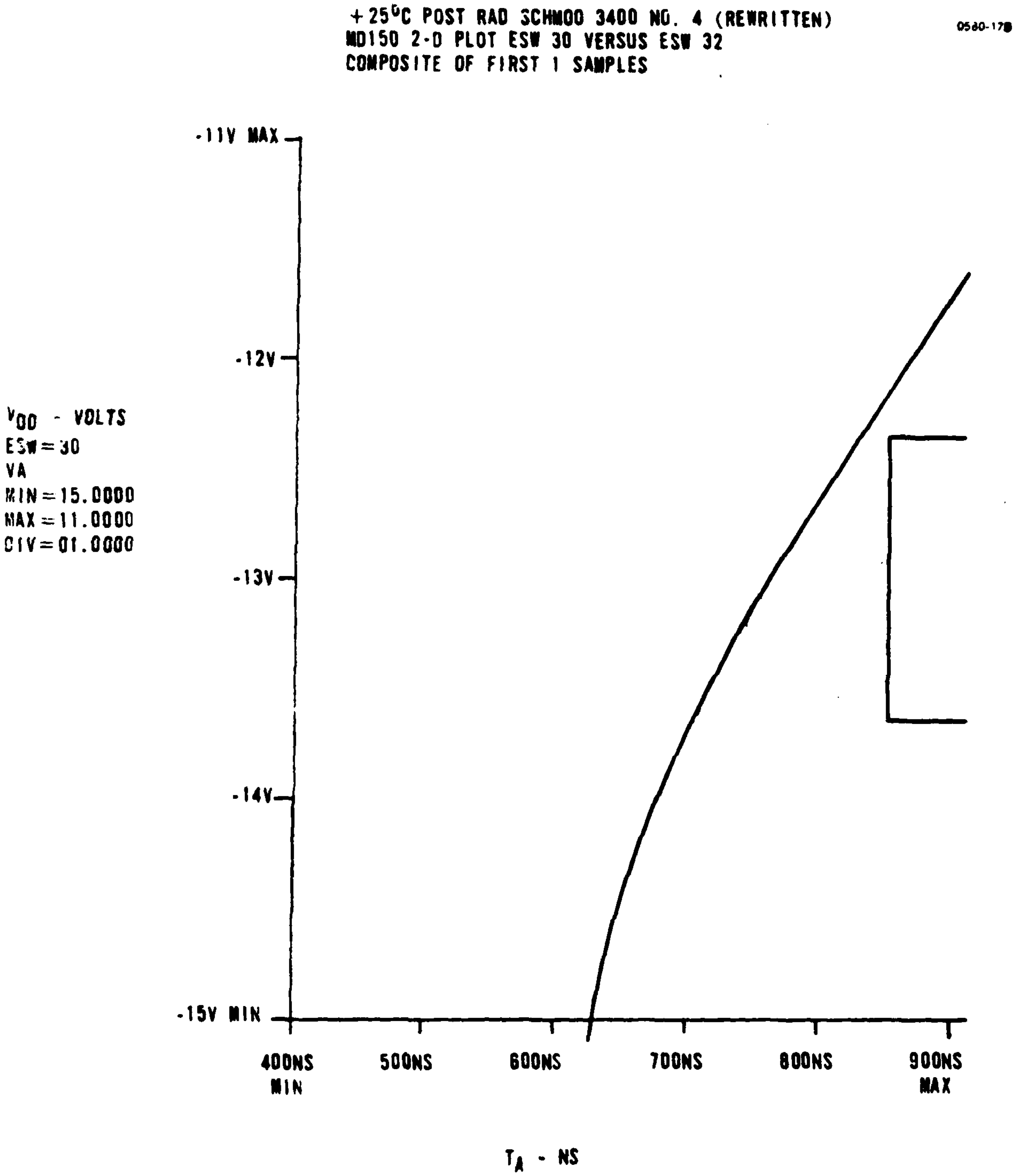


FIGURE 6-41. 3400 NO.4 +25°C POST RAD SCHMOO (REWRITTEN)

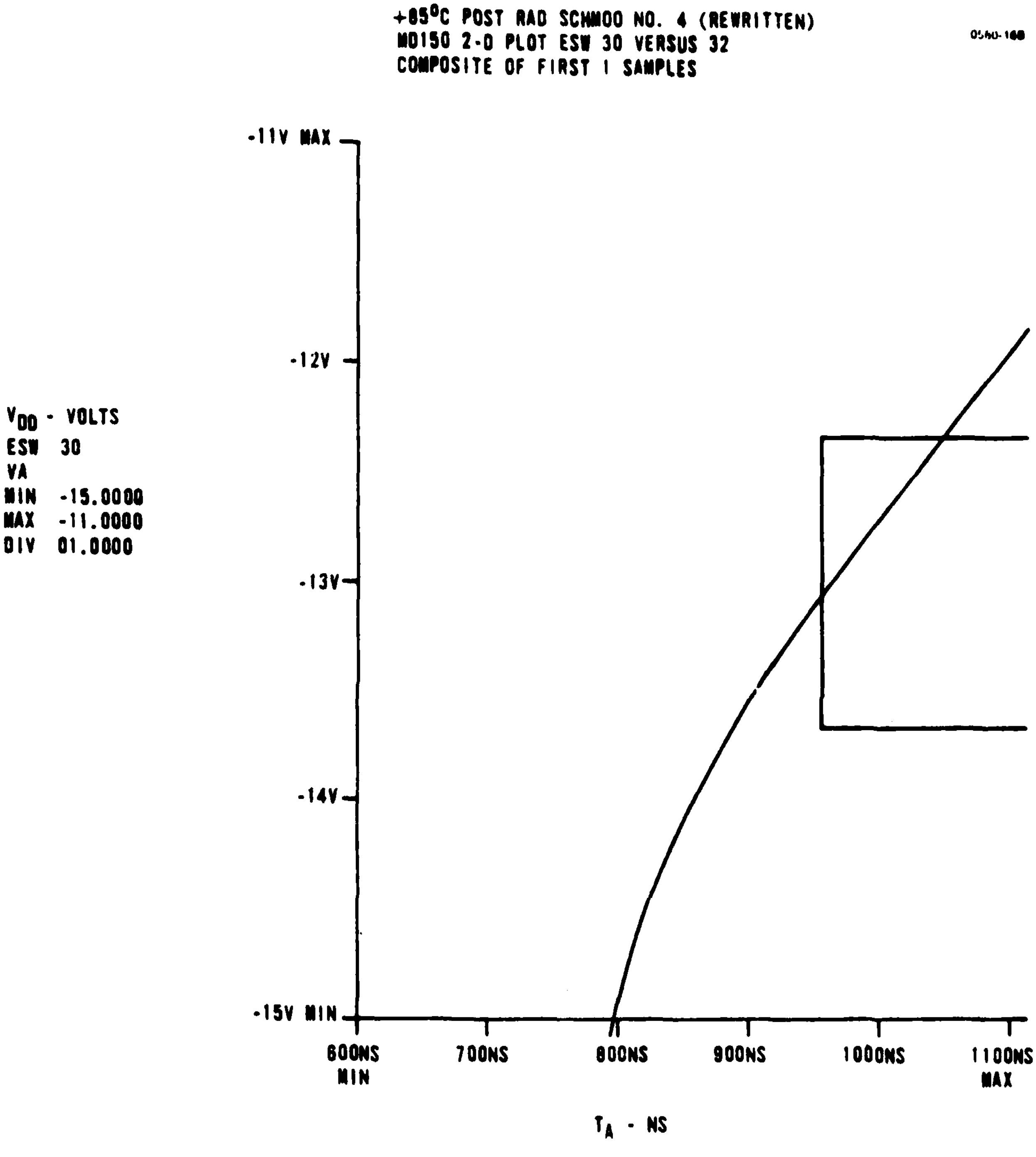


FIGURE 6-42. 3400 NO. 4 +85°C POST RAD SCHMOO (REWRITTEN)

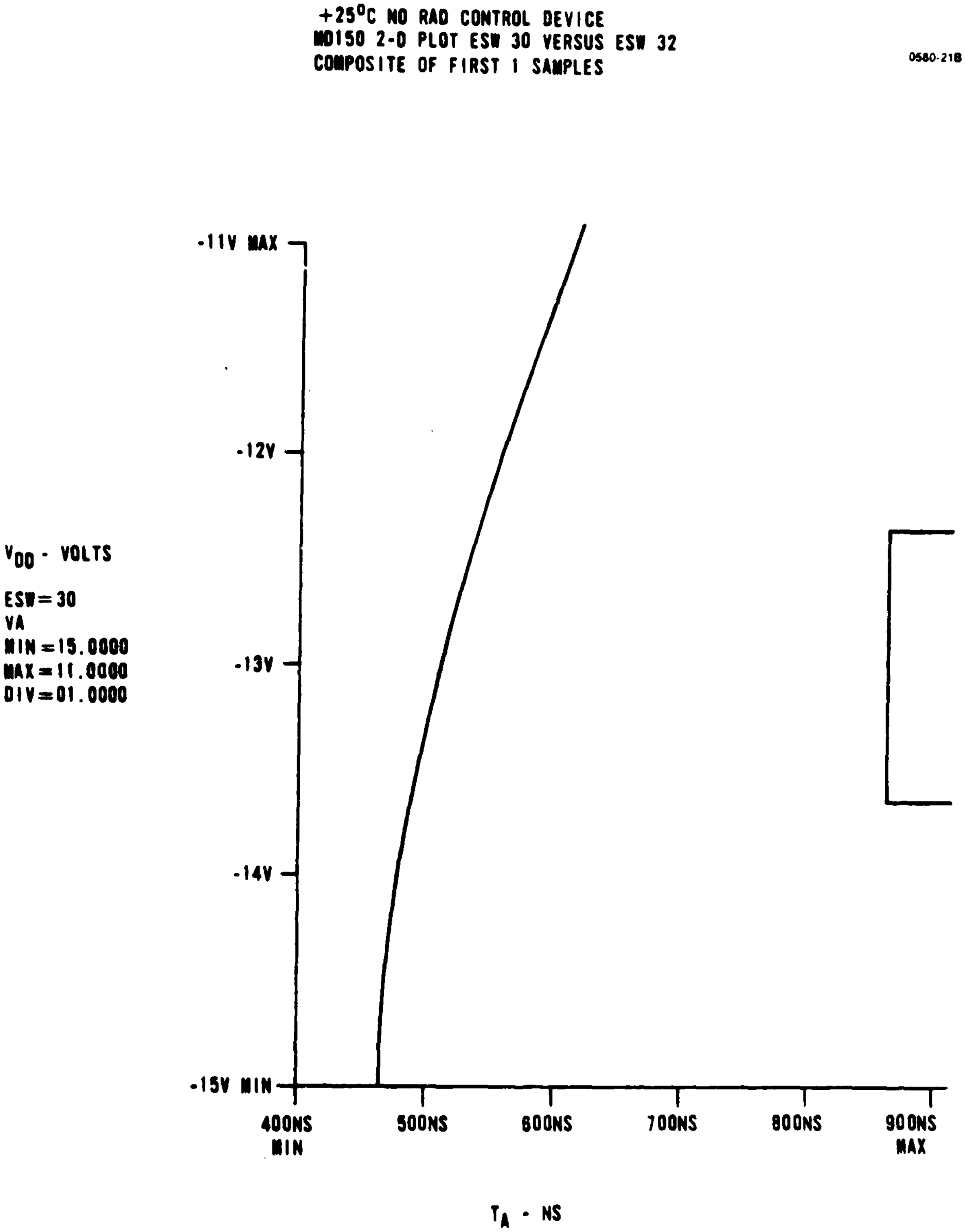


FIGURE 6-43. 3400 NO. 26 +25°C NO RAD CONTROL DEVICE

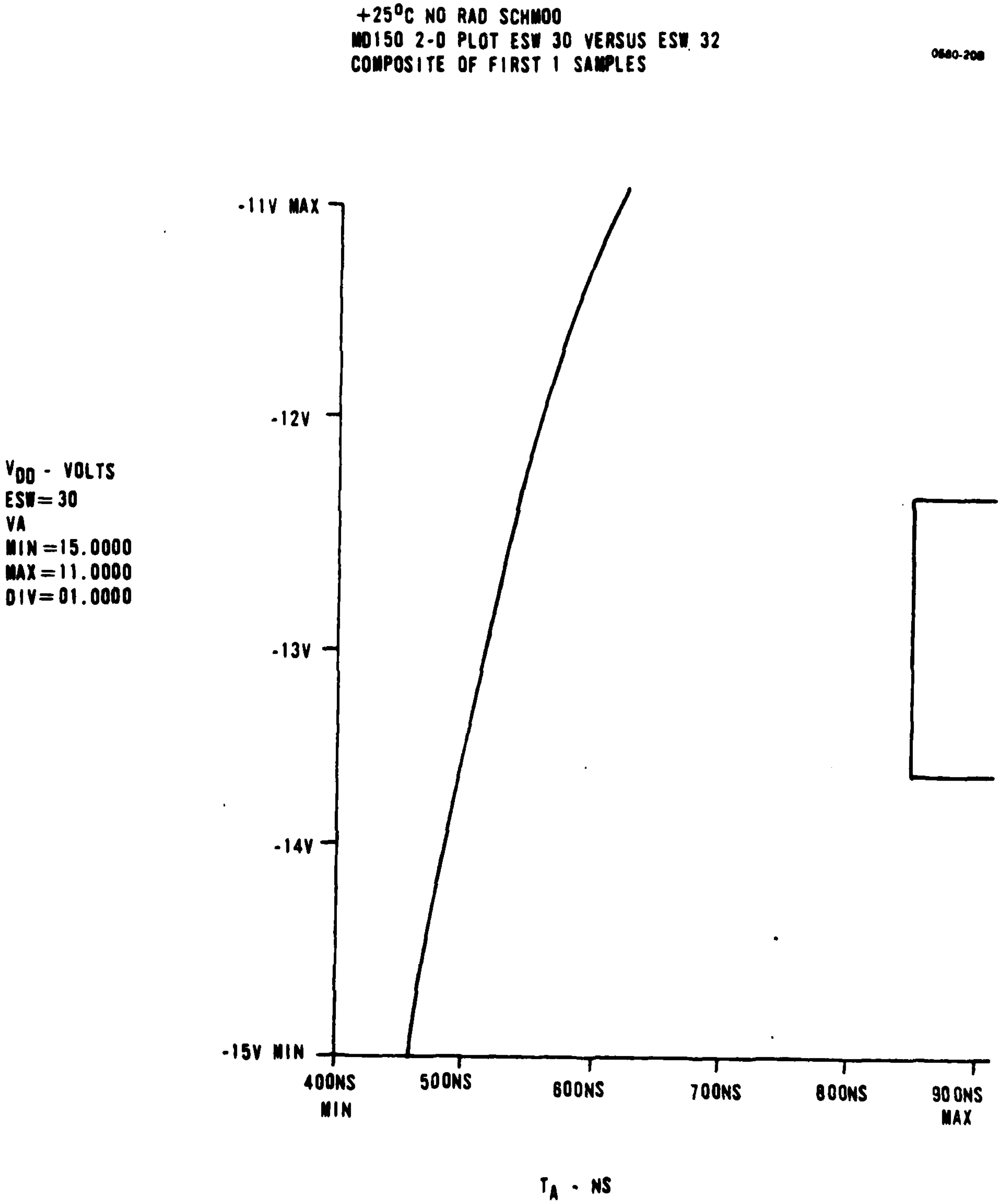


FIGURE 6-44. 3400 NO. 26 +25°C NO RAD SCHMOO CONTROL DEVICE

7.0 MNOS UNIQUE CHARACTERISTICS

In the last report characteristics unique to MNOS (i.e., non-volatile semiconductor memories) were discussed. The characteristics identified were:

- Static Retention,
- Read Disturb Retention,
- Endurance.

Each of these was discussed in some detail in the last report and defined. This report shows some of the parameters related to these characteristics and discusses their influence on testing and applications.

7.1 Static Retention

Some of the parameters tested in this program that influence static retention are:

- Write Bias,
- Write Time,
- Temperature Variation of Reference Voltage.

While these parameters affect retention, they also influence the read disturb retention and endurance.

7.1.1 Write Bias

One method proposed to reduce endurance effects is to reduce the erase and write voltages. In doing this knowledge of the relationship between the write voltage and the resulting threshold values must be known to insure that a full retention characteristic is obtained (or at least a predictable value is known).

Tests were conducted to determine the relationship to the value of the applied write bias to the resulting threshold. In order to further determine characteristics based on the relative "thickness" of the nitride layer the devices tested were segregated by the thickness measurements used in initial testing. It was anticipated that the "thin" nitride parts would write at lower potential and result in "deeper" written V_T's (defined earlier as "0"'s).

Figure 7.1 through 7.6 show that the initial assumptions were somewhat accurate. The thinner parts (Figures 7.1 through 7.3) show that while the resulting thresholds were "deeper" no clear indication of lower writing potential was established. The "thicker" parts saturated at a lower write potential but with a softer threshold. No retention measurement was taken after writing the devices to determine if there was any differences in charge distribution resulting from the soft writing due to limits on the scope of the program. This test is suggested for those interested in pursuing this approach.

7.1.2 Variable Write Time

Since the writing process in MNOS is both voltage and time dependent, one method of varying the threshold level to which the memory transistors are set is by a shortened write cycle. This is particularly important for systems requiring (or desiring) a faster write. Data acquisition and simulated tape or disc systems are good examples of this type application.

While reduced retention can be expected due to the "soft" threshold that results from reduced write times, an enchanced endurance characteristic is expected from the reduced cycle. The possibility of an increased decay slope of retention and reduced high temperature performance should be investigated due to possible changes in charge distribution resulting from the "soft" writing.

Table 7-1 shows the results of write time testing performed with NCR2810's, NCR2457's and GI3400's. Figure 7-1 through 7-14 show the plotted data. Figures 7-1 through 7-3 show the writing characteristic of the NCR2810. Using the thick/thin Nitride grading of the parts it can be seen the "thin" part writes down further and faster than the thicker parts as was expected. The part in Figures 7-4 and 7-5 were previously used in endurance testing and show a fast, deep write characteristic.

Figures 7-6, 7-7, 7-12, 7-13 and 7-14 are examples of "thin" nitride 3400's and 2451's which exhibit the fast write characteristic while Figures 7-8 through 7-11 are relatively thick parts which show a slower write characteristic. All parts arrive at full saturation long before the specified condition indicating use in a system requiring faster writing is practical.

TABLE 7-1. WRITING CHARACTERISTICS

Write Boundary Threshold Voltage

Device										
Period	6 µs	8 µs	10 µs	12 µs	14 µs	16 µs	20 µs	24 µs	28 µs	Timer
T_W	11.2 µs	15.2 µs	19.2 µs	23 µs	27 µs	31 µs	39 µs	47 µs	55 µs	Erased
207	None	None	None	None						10
209	None	None	-11.91	-12.10	-12.26	-12.38	-12.54	-12.64	-12.64	14
211	None	None	-10.26	-10.36	-15.00	-15.00				15
212	None	None	-11.94	-12.28	-12.50	-12.66	-12.88	-13.04	-13.14	11
Period	6 µs	8 µs	10 µs	16 µs	34 µs	32 µs	42 µs			
T_W	11.2 µs	13.2 µs	19.2 µs	31 µs	47 µs	63 µs	83 µs			
Period	None	None	None	-11.68	-12.00	-12.10	-12.30			16
212	-11.98	-12.68	-12.94	-13.08	-13.18	-13.26	-13.78	-13.34	-13.36	10

Device									Plot Data
Period	10 µs	90 µs	170 µs	250 µs	330 µs	410 µs	400 µs	Soft Erase 3/12/79	
T_W	19.2 µs	179 µs	339 µs	499 µs	659 µs	819 µs	979 µs		Write pulse width
2-7	None	-12.18	-12.96	-13.12	-13.20	-13.28	-13.32	53	Plot
209	-11.84	-13.76	-13.50	-13.60	-13.66	-13.72	-13.74	10	Plot
211	-11.28	-16.00	None					4	Endurance
212	-11.92	-13.76	-14.00	-14.10	-14.18	-14.22	-14.26	27	Endurance

TABLE 7-1. WRITING CHARACTERISTICS (Continued)

									Plot Data	
215								4		
227								3		
504	None	-13.12	-13.44	-13.62	-13.72	-13.82	-13.88	8	Plot	
509	-11.88	-13.56	-13.82	-13.16	-13.98	-14.04	-14.10	1	Plot	
514	-11.66	-13.20	-13.44	-13.56	-13.68	-13.66	-13.40	2		
530	-11.69	-13.90	-13.70	-13.88	-13.90	-13.92	-13.98	2	Radiated	
Device										
Period		10	14	18	22	26	30	34	42	Erase
T_W										
509	-11.70	-12.30	-12.58	-12.74	-12.84	-12.94	-12.94	-	13	
511	-11.56	-12.00	-12.30	-12.44	-12.56	-12.64	-12.64	-	13	
504	None	-11.52	-11.84	-12.06	-12.22	-12.34	-12.36	-	13	
530	-11.54	-12.14	-12.42	-12.60	-12.72	-12.82	-19.92	-13.02	17	
Period		10 µs	90 µs	170 µs	250 µs	330 µs	410 µs	490 µs	Soft Erases 7.24.79	
T_W	19.2 µs	179 µs	339 µs	499 µs	659 µs	819 µs	979 µs		Write pulse width	
533	None	-13.30	-13.88	-14.18	-14.38	-14.56	-14.66	12.00	8	Plot
536	None	-13.30	-13.89	-14.20	-14.40	-14.58	-14.72	11.36	9	Plot
541	None	-12.80	-13.34	-13.68	-13.90	-14.04	-14.18	10.93	9	Plot

8.0 COMPARISON MATRIX

Table 8-1 shows comparisons of the preselection devices on many parameters. Values shown in Table 8-1 represent measurements taken in MACI Program and may not reflect vendor specification values.

TABLE 8-1. MNOS DEVICE COMPARISON TABLE

DEVICE TYPE	COMPAT. DEVICES	MILITARY APPL. COST @10K PCS $Bits/Word	MILITARY APPL. DENSITY SPEED/TACC -55 - +125°	RETENTION Static 25°C STATIC +125°	RETENTION BIASED Static +25°C READ DISTURB Scale 1-4	ENDURANCE RETENTION AFTER 10^4 E/W	VENDOR SUPPORT	POWER MW ±25 -55	POWER MW +125 WRITE	DC PARAMETERS GRADED 1 - 5	RADIATION ΔV_T @2K RADS	PACKAGING	V_T READ	COMMENTS
WAROM NCR2451 NCR 1K x 4	NC7451 ER3400	0.3¢/Bit	4K Bits	1.7×10^{10} - 4×10^{10} Sec	8.3×10^8 - 1.7×10^9 Sec	6.5×10^5 to 1.6×10^7	STRONG > 5 YRS	325	260	3	0.28 V	22 PIN CER DIP	YES	Good Performer Fast Second source available
		4	.35µs-.65µs	1.7×10^7 - 1.7×10^8	3			393	227					
ER3400 GI WAROM 1K x 4	NC7451 NCR2451	0.35¢/Bit	4K Bits	1.1×10^{10} - 1.1×10^{11} Sec	No Test	3.2×10^6 to 3.86×10^8	STRONG > 5 YRS	339	283	3	0.18 V	22 PIN CER DIP	YES	Good Performer Fast Second source available
		4	.3µs - .6µs	1×10^8 - 3×10^8 Sec	2			428.5	270					
ER2401 EAROM 1K x 4 GI	NCR2401	0.15¢/Bit	4K	1×10^{18} - 4.7×10^{18} Sec	2×10^{20} - 9.5×10^{21} Sec	1×10^8 to 1×10^{12}	WEAK < 3 YRS	152	114	2	0.033 V	24 PIN CER DIP	YES	No vendor support Slow
		4	.8µs-1.5µs	4.5×10^{12} - 1×10^{17} Sec	4			228	638					
NCR2810 NCR 2K x 4 EAROM	ER2810 NC2810	0.1¢/Bit	8K	2×10^{12} - 2×10^{14} Sec	2×10^{12} - 7×10^{14} Sec	2.5×10^5 to 3.7×10^{11}	STRONG > 5 YRS	190	114	1	0.08 V	24 PIN CER DIP	YES	Best all-around performer Hi-density
		4	.7µs-1.0µs	4.4×10^9 - 1×10^{11} Sec	1			266	638					
NC7053 128 x 8 Nitron WAROM		1.3¢/Bit	1K	No Test	No Test	No Test	UNKNOWN (new design in works)	416	307	5	No Test	No Test	NO	Poor high temperature Performance not available
		8	1.5µs-2.7µs *	No Test	No Test			527	No Test					

9.0 CONCLUSIONS

All the previously performed testing indicates that use of commercial MNOS EAROM's is both feasible and practical in military systems. The primary drawbacks to their use are:

- Limited sources - Relatively minor semiconductor firms are only sources of parts. Combined with lack of interest in OEM sales of some vendors.
- Limited knowledge of technology by military personnel and prime contractors requires overcoming device credibility problems prior to system application.
- Parts not specifically designed for military use requires independent evaluation and characterization.
- Access time is not yet competitive with requirements of a large number of systems.
- Device process and circuit changes require recharacterization with no notice given by vendors about changes when they occur.

The preferred parts for military use are:

- NCR 2810
- Nitron 7810
- ER2810 - G.I.
- ER3400 - G.I.
- NCR 2451
- Nitron 7451.

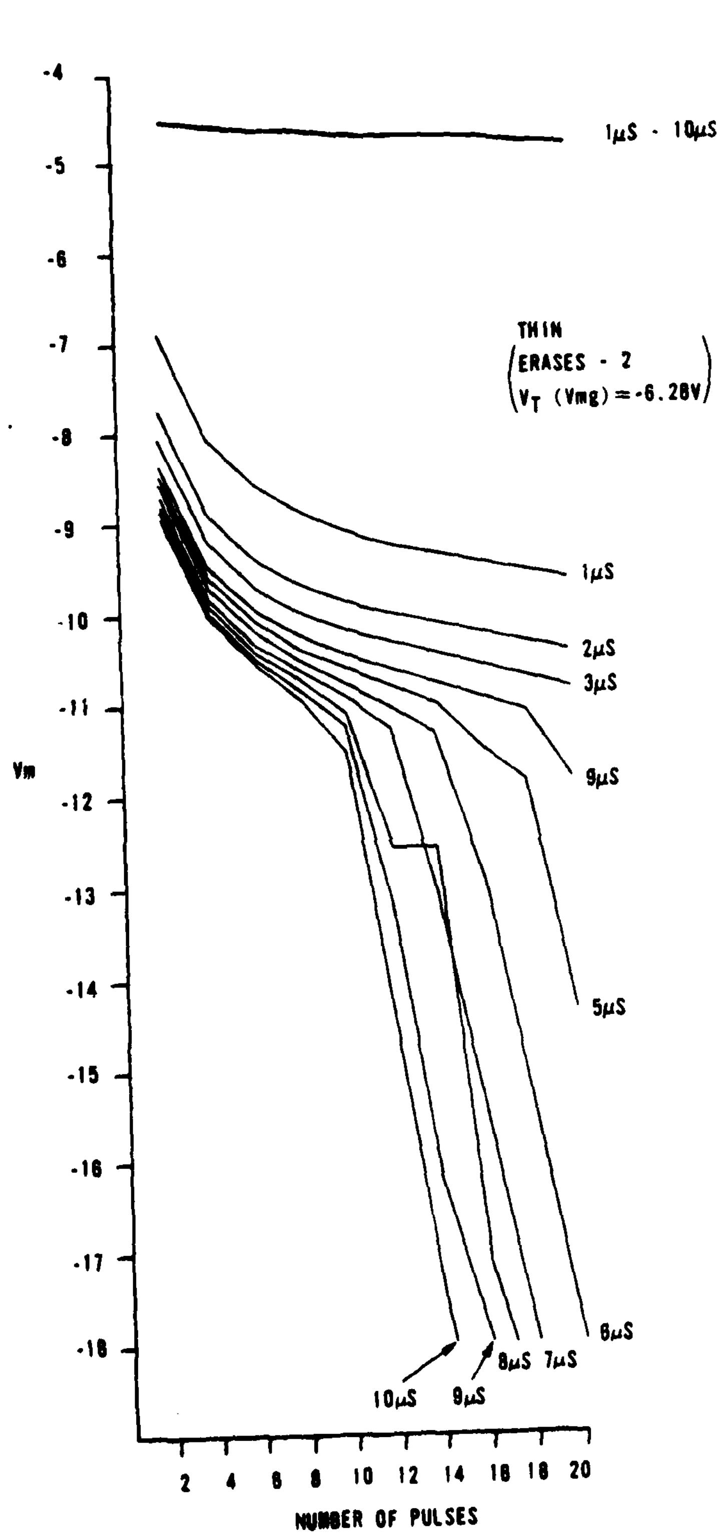
While current results show the NC 7053 (Nitron) currently unsuitable, changes in the sense amplifier design and other improvements indicate it should be considered in future programs.

Of the above parts, the GI 3400 is the most available part and is being produced in a "high rel" version. Since it is pin compatible with the 2451 and 7451 it is multiple sourced and has characteristics that make it suitable for microporcessor applications.

10.0 TEST PLAN

The Test Plan shown below is a preliminary draft of the plan to be used to screen the selected parts for delivery to ERADCOM. The retention limits and a suggested Read/Distrub test approach does not appear in this plan as the details are being finalized.

A new approach to accelerated Read/Distrub testing using the write speed characteristic as an indication of the Read/Disturb characteristic is being investigated to determine the correlation.



(THIN NITRIDE PART - 2 ERASES V_T (VMG)=6.28V

FIGURE 7-1. WRITE WIDTH VERSUS V_T 2810 NO. 318

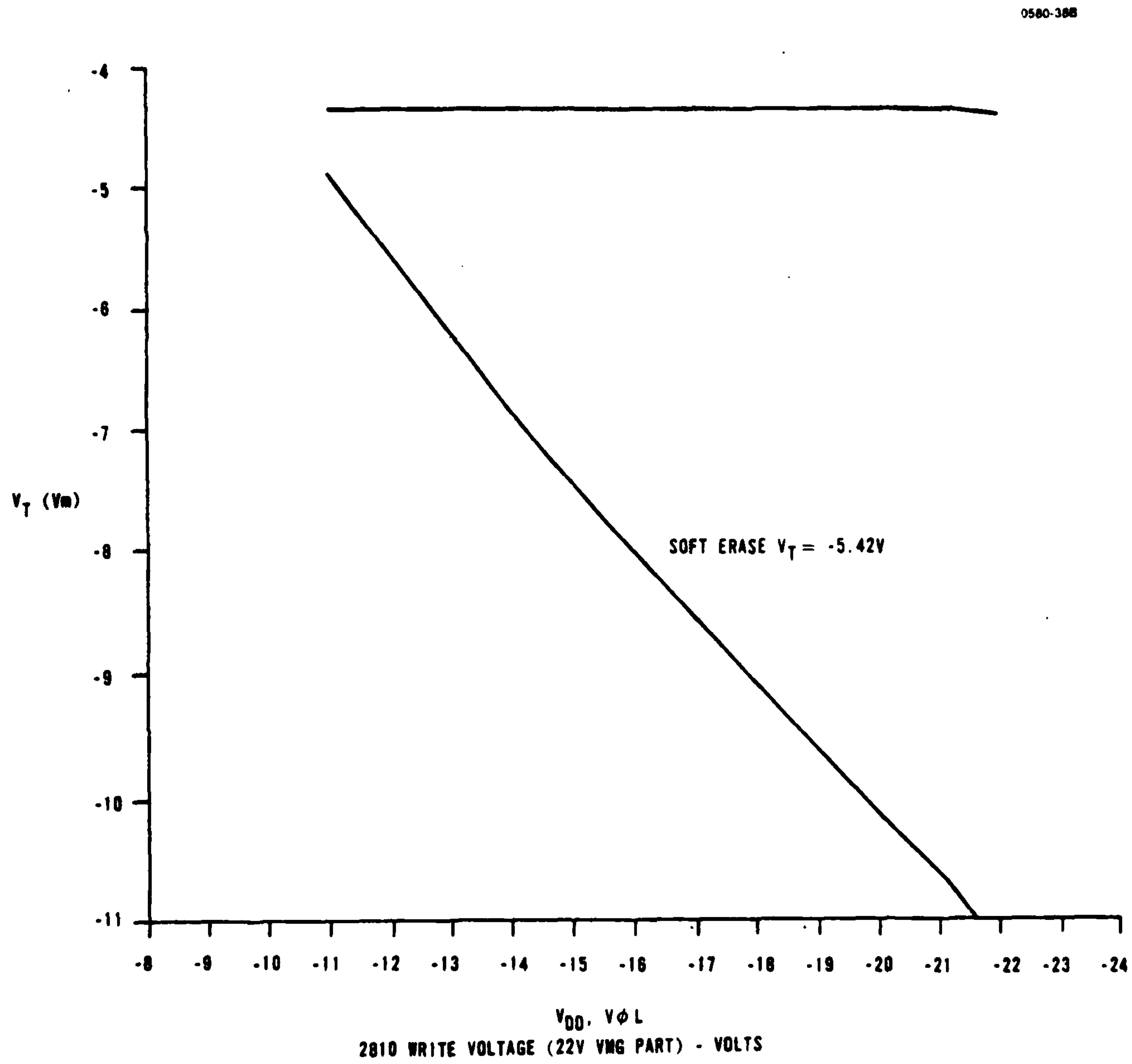


FIGURE 7-1a. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)

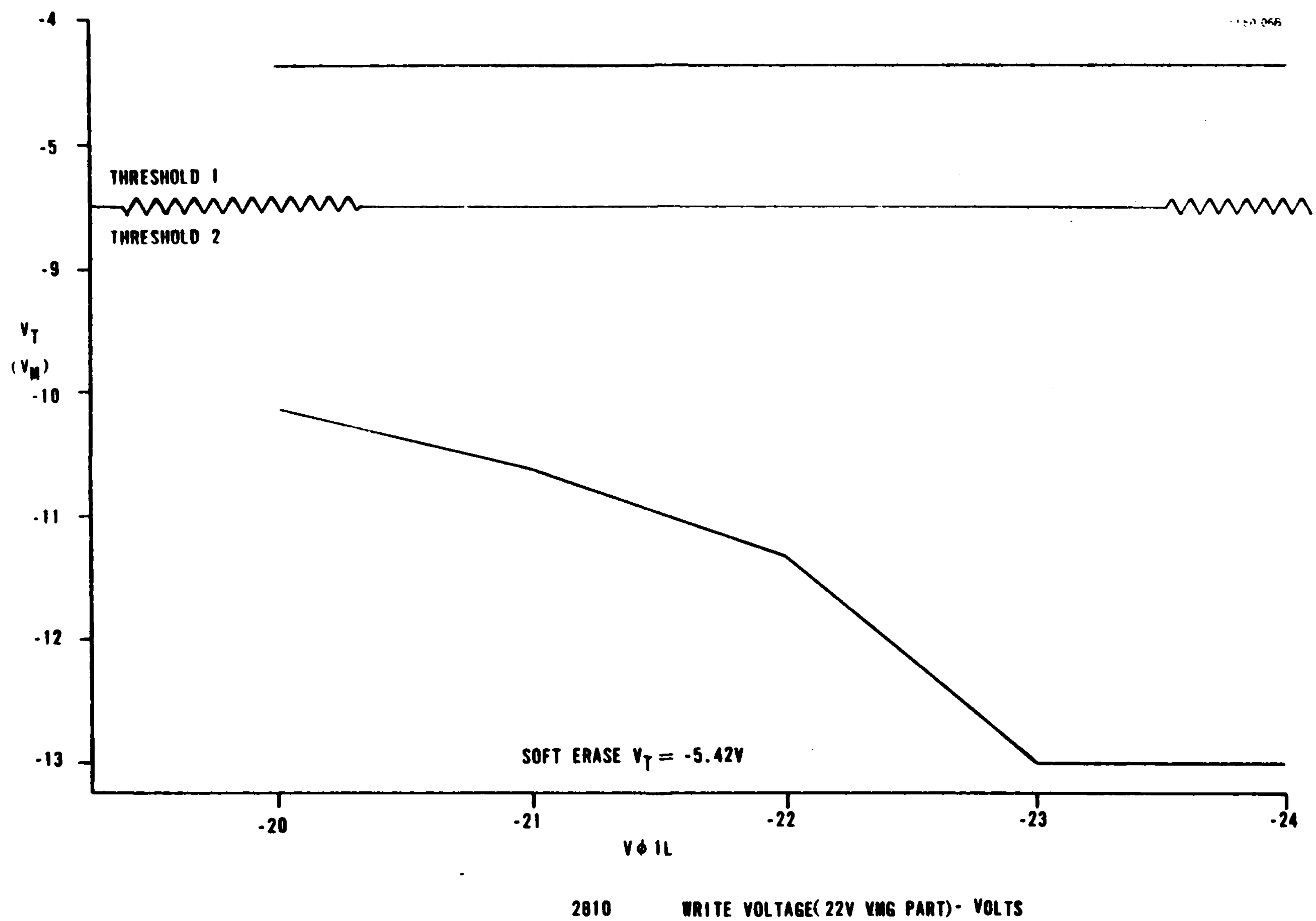
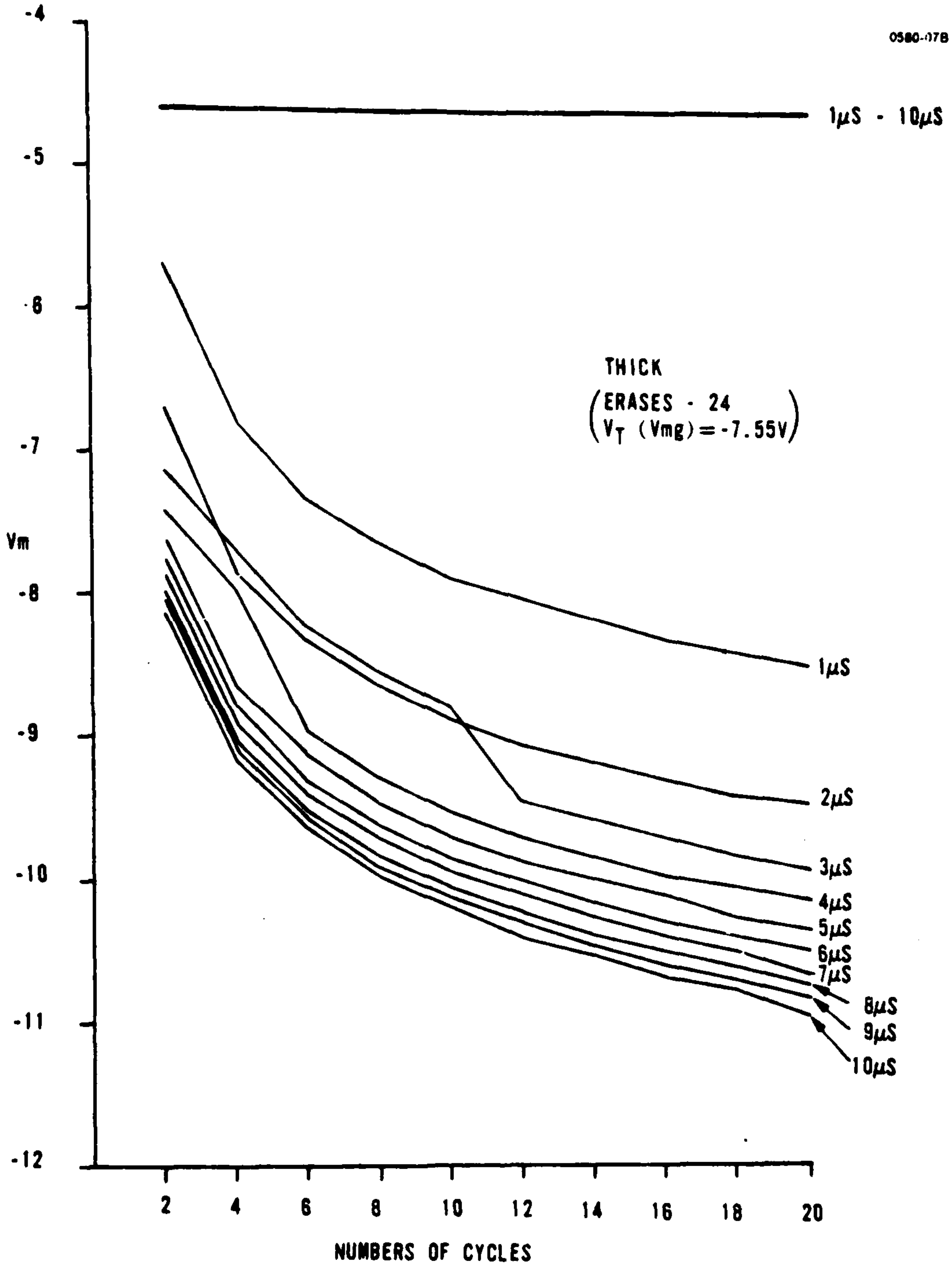


FIGURE 7-1b. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)



(''THICK'' NITRIDE PART - 24 ERASES VMG -7.55V)

FIGURE 7-2. WRITE WIDTH VERSUS V_T 2810 NO. 328

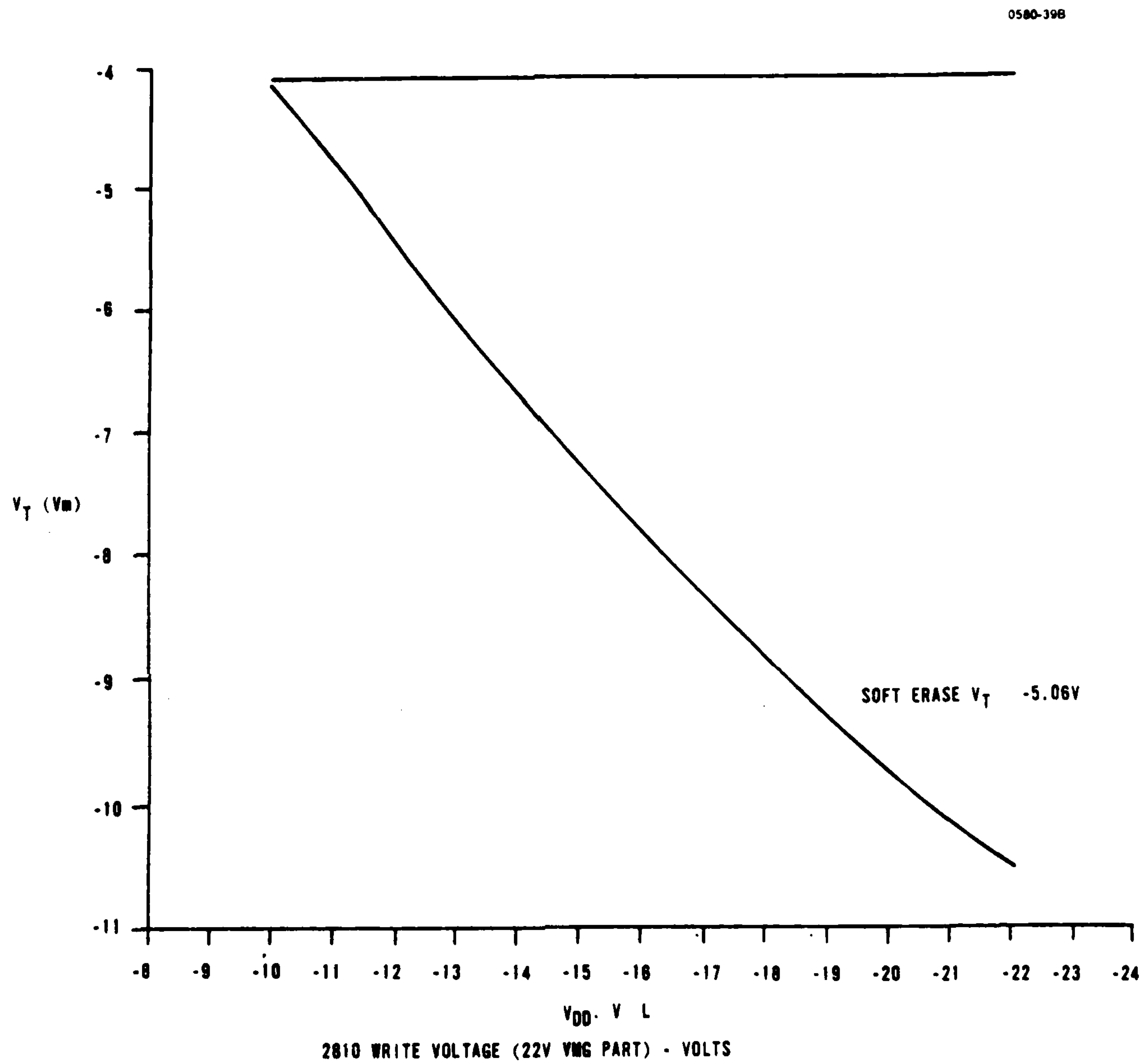


FIGURE 7-2a. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)

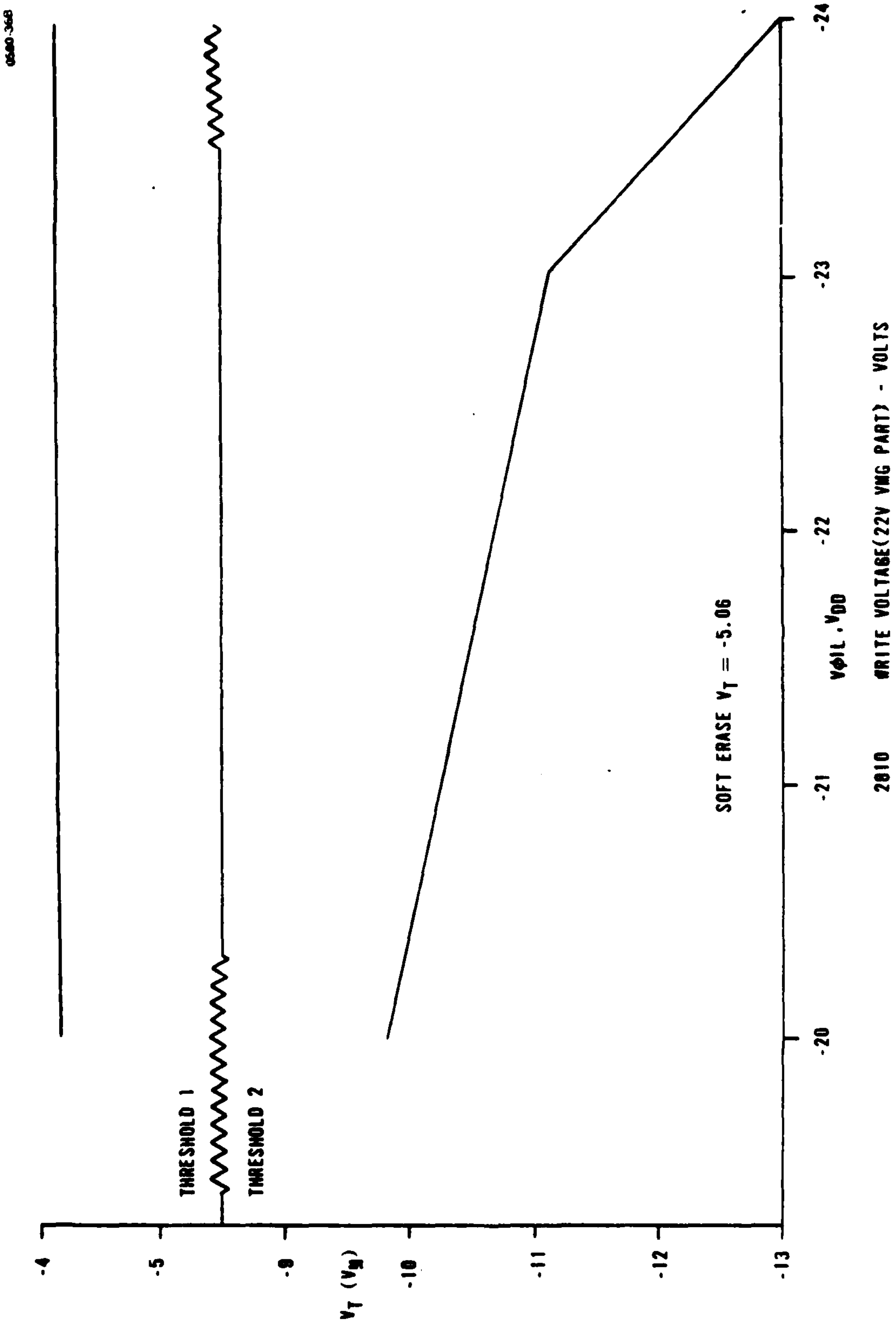
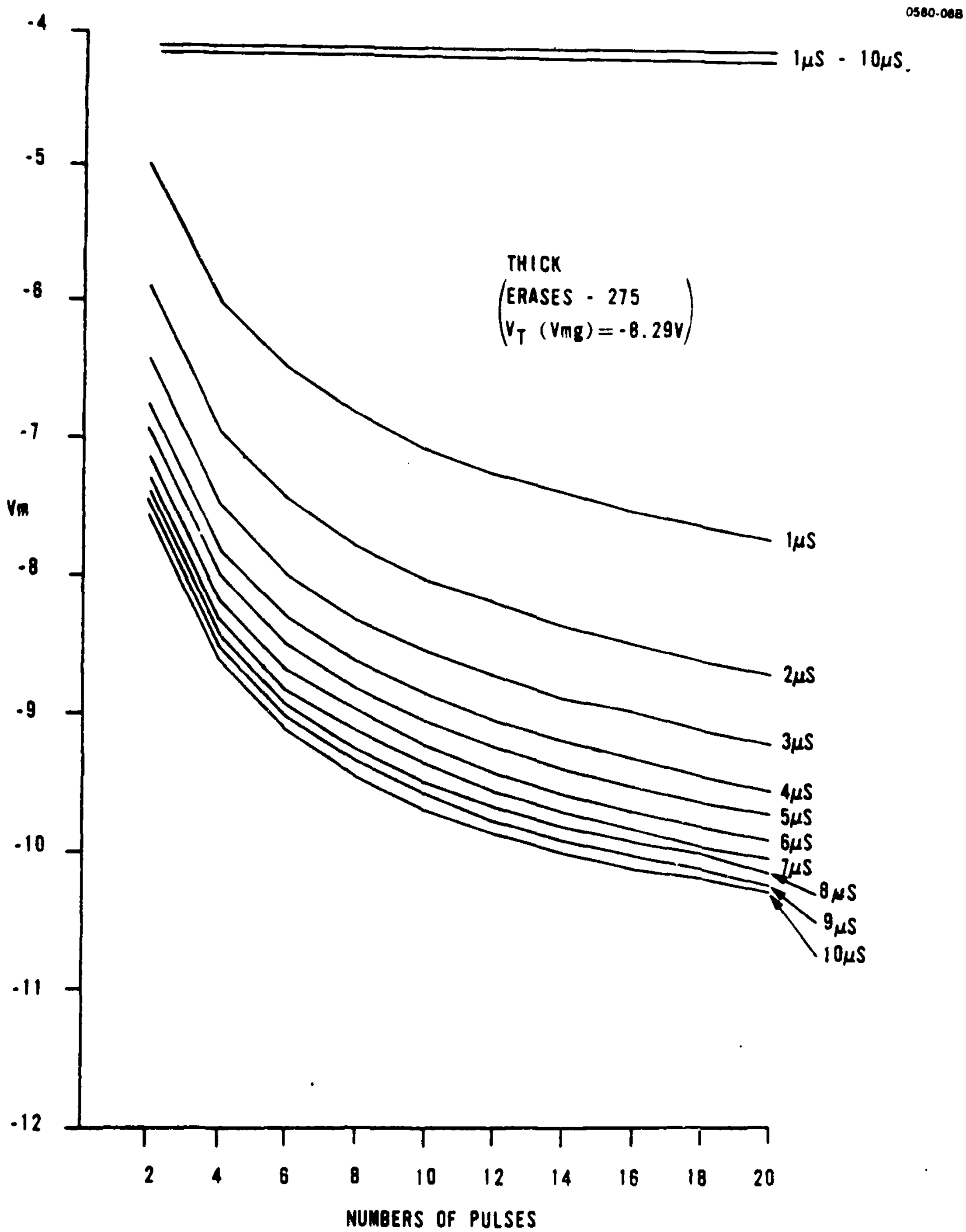


FIGURE 7-2b. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)



(THICK NITRIDE PART - 275 ERASES, VMG - 8.29V)

FIGURE 7-3. WRITE WIDTH VERSUS V_T
2810 VERSUS 333

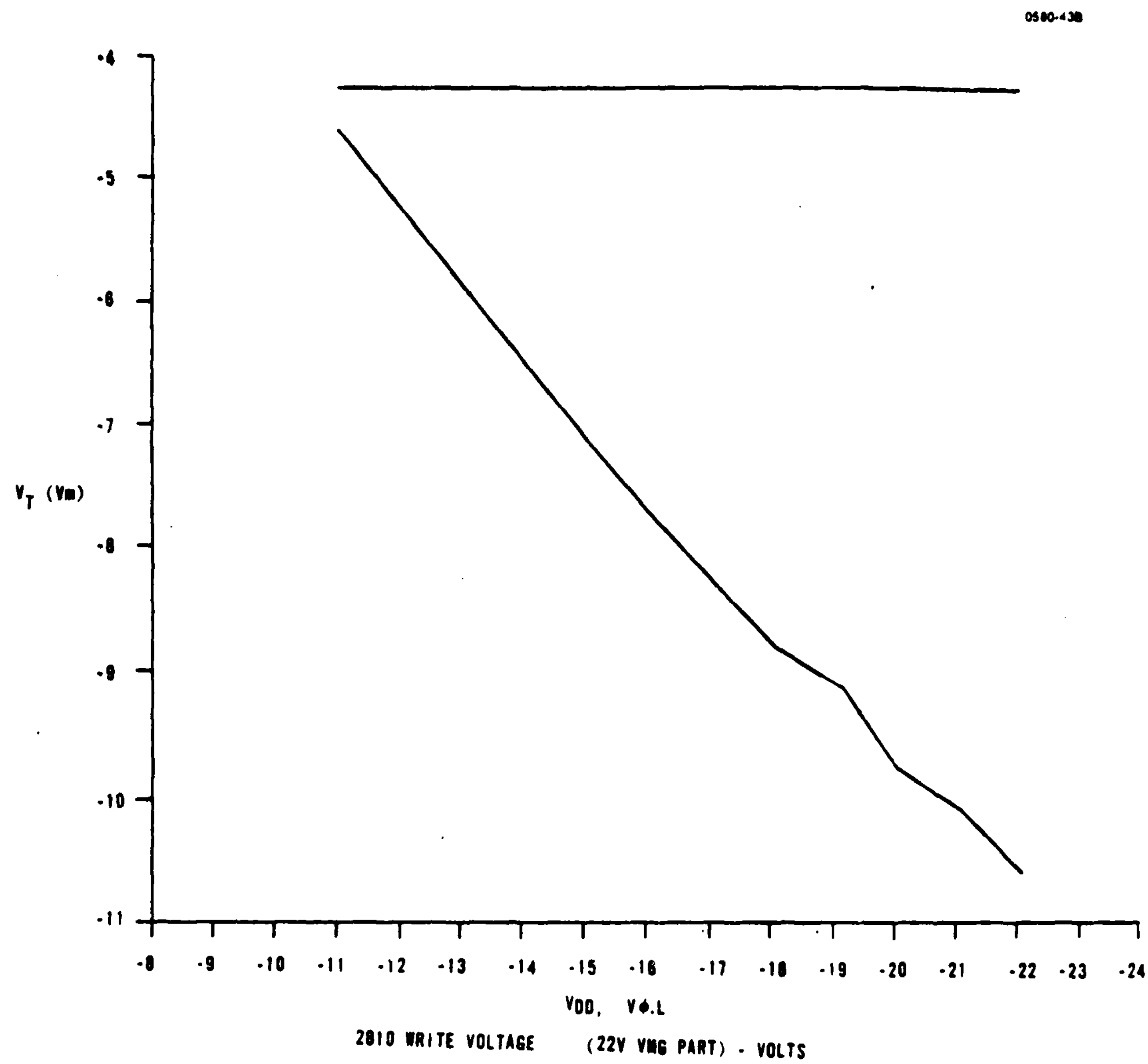


FIGURE 7-3a. WRITE VOLTAGE VERSUS V_T
(THIN NITRIDE PART)

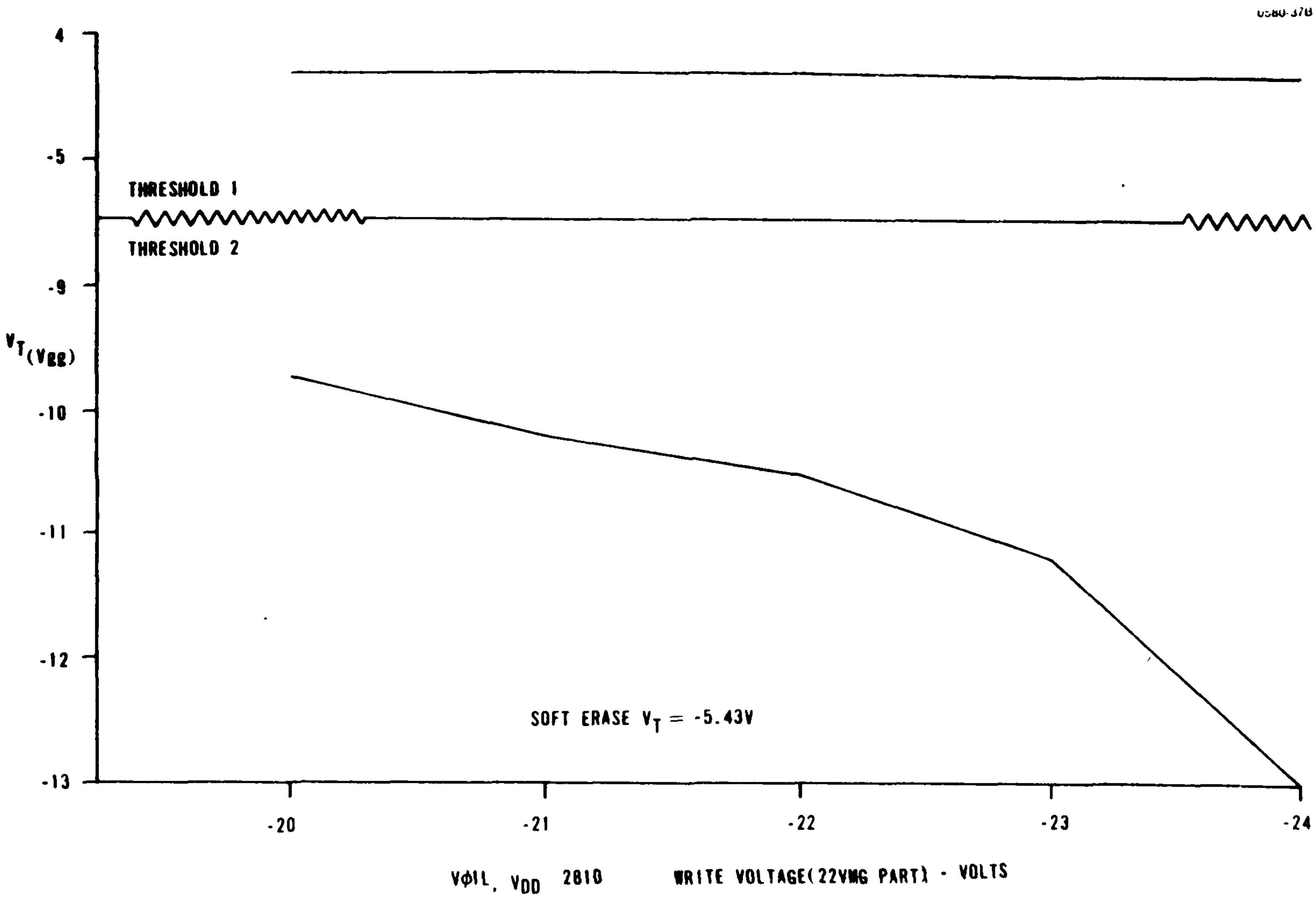


FIGURE 7-3b. WRITE VOLTAGE V_W-V_T
("THIN" NITRIDE PART)

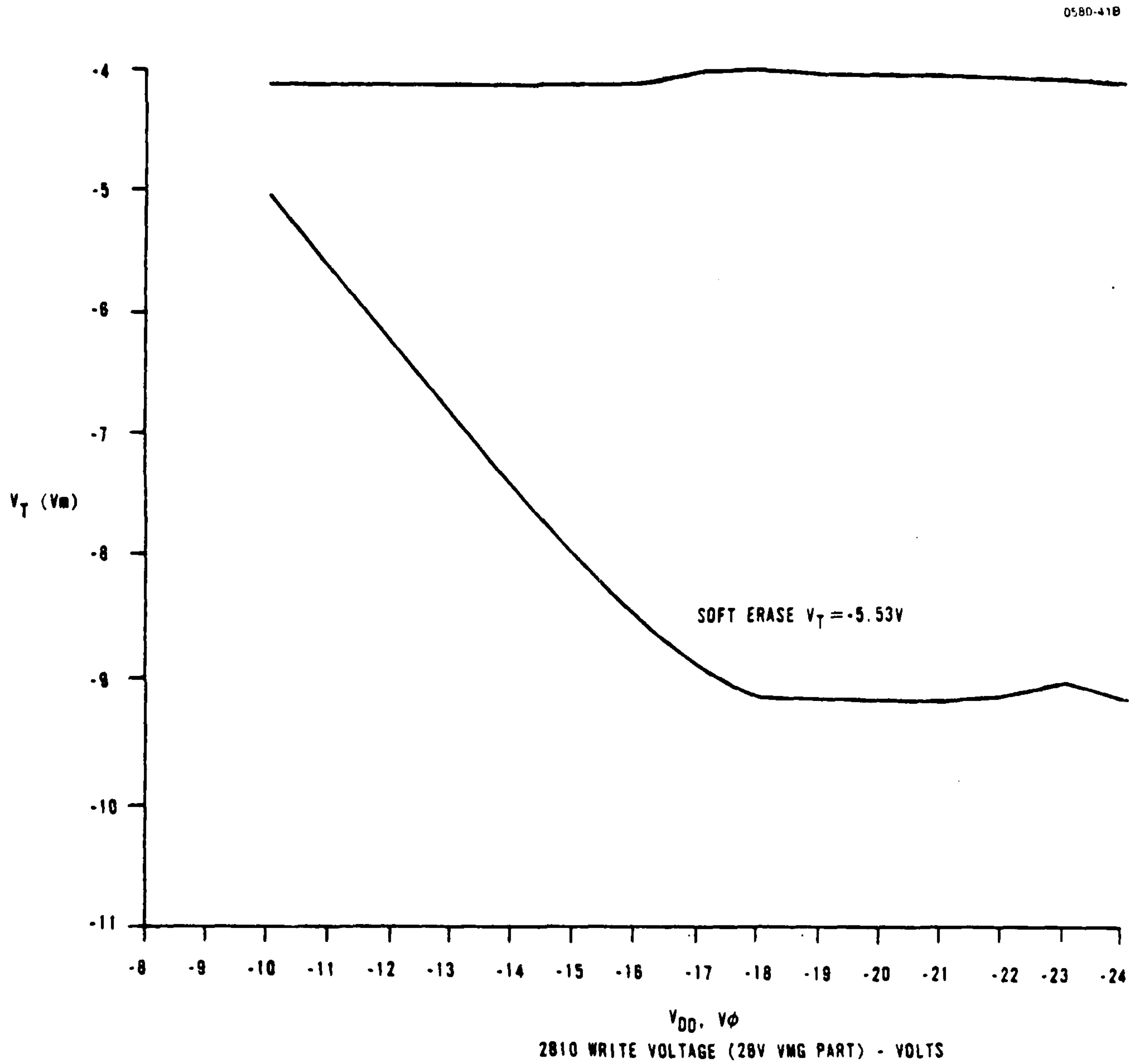


FIGURE 7-3c. WRITE VOLTAGE VERSUS V_T
(THICK NITRIDE PART)

AD-A085 742 HONEYWELL INC ST PETERSBURG FL F/G 15/5
MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM OF ELECTR--ETC(U)
APR 80 R L WIKER, R W CARTER, J MADDOX DAAB07-78-C-2935
UNCLASSIFIED 1079-16060-2 DELET-TR-78-2935-2 NL

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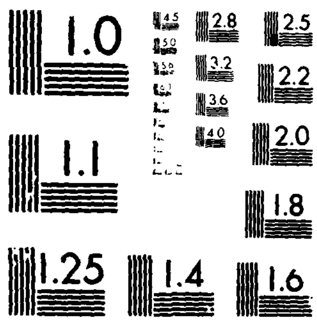


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

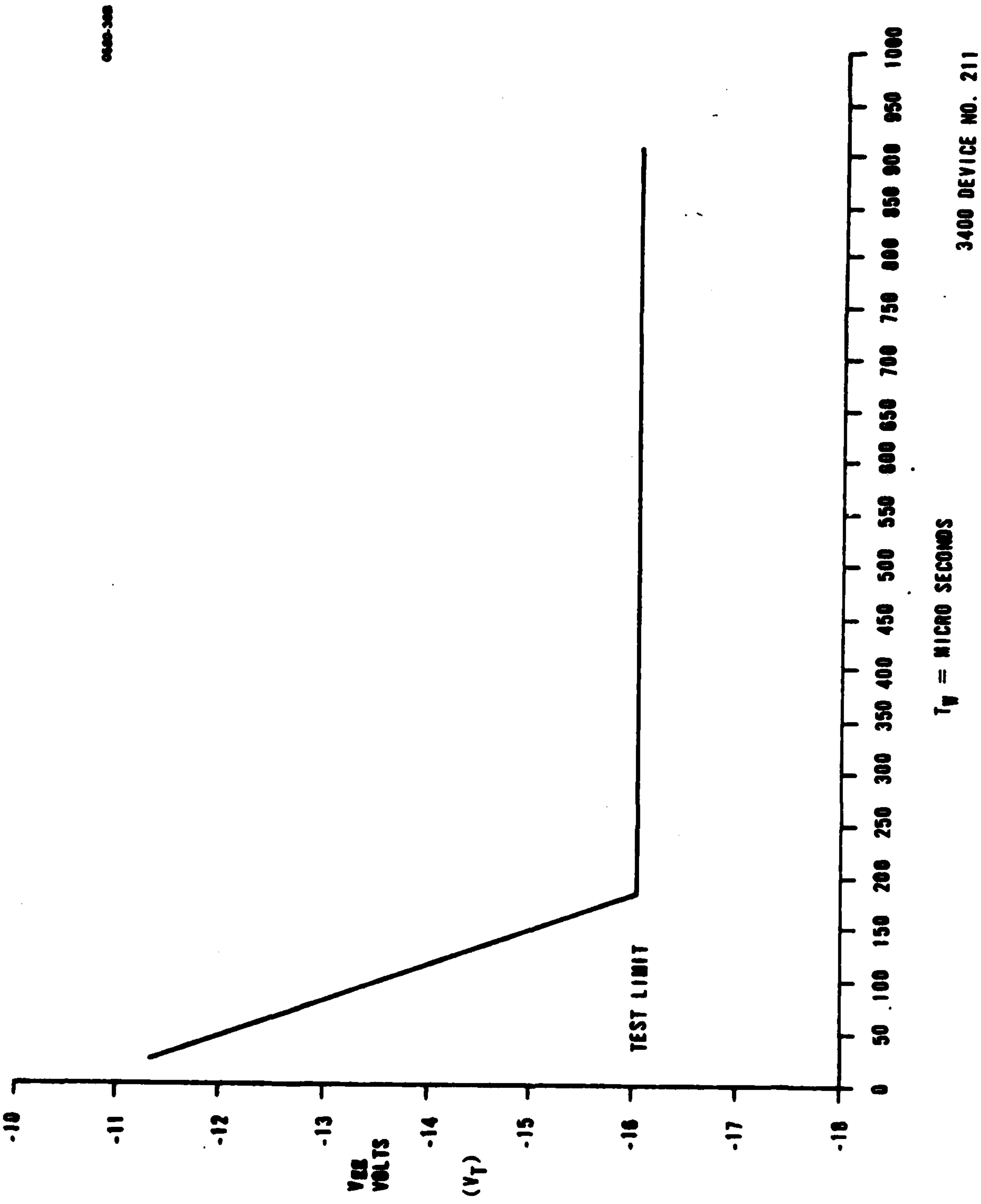


FIGURE 7-4. WRITE WIDTH VERSUS V_T (ENDURANCE DEVICE)

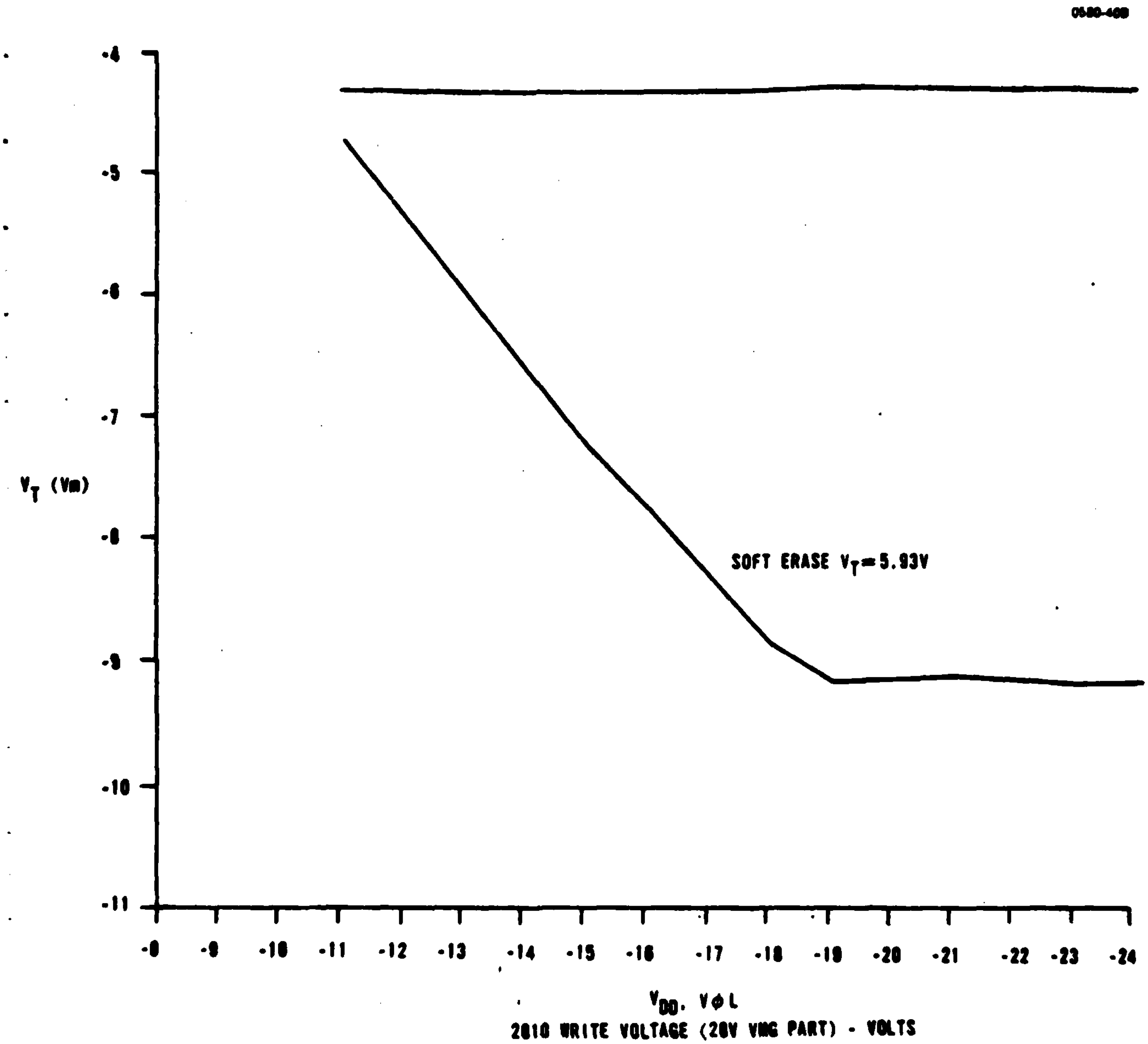


FIGURE 7-5. WRITE VOLTAGE VERSUS V_T
(THICK NITRIDE PART)

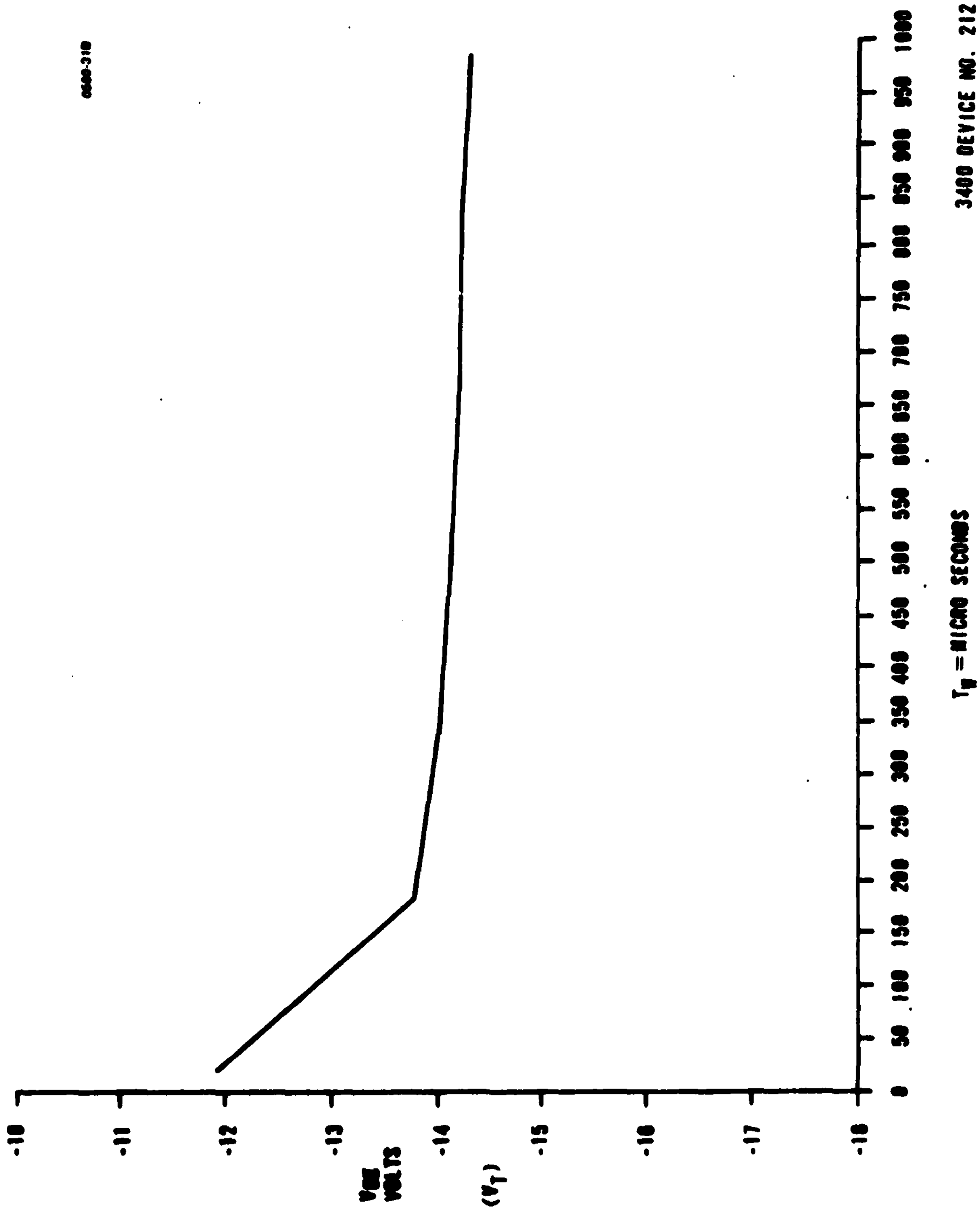


FIGURE 7-5a. WRITE WIDTH VERSUS V_T (ENDURANCE DEVICE)

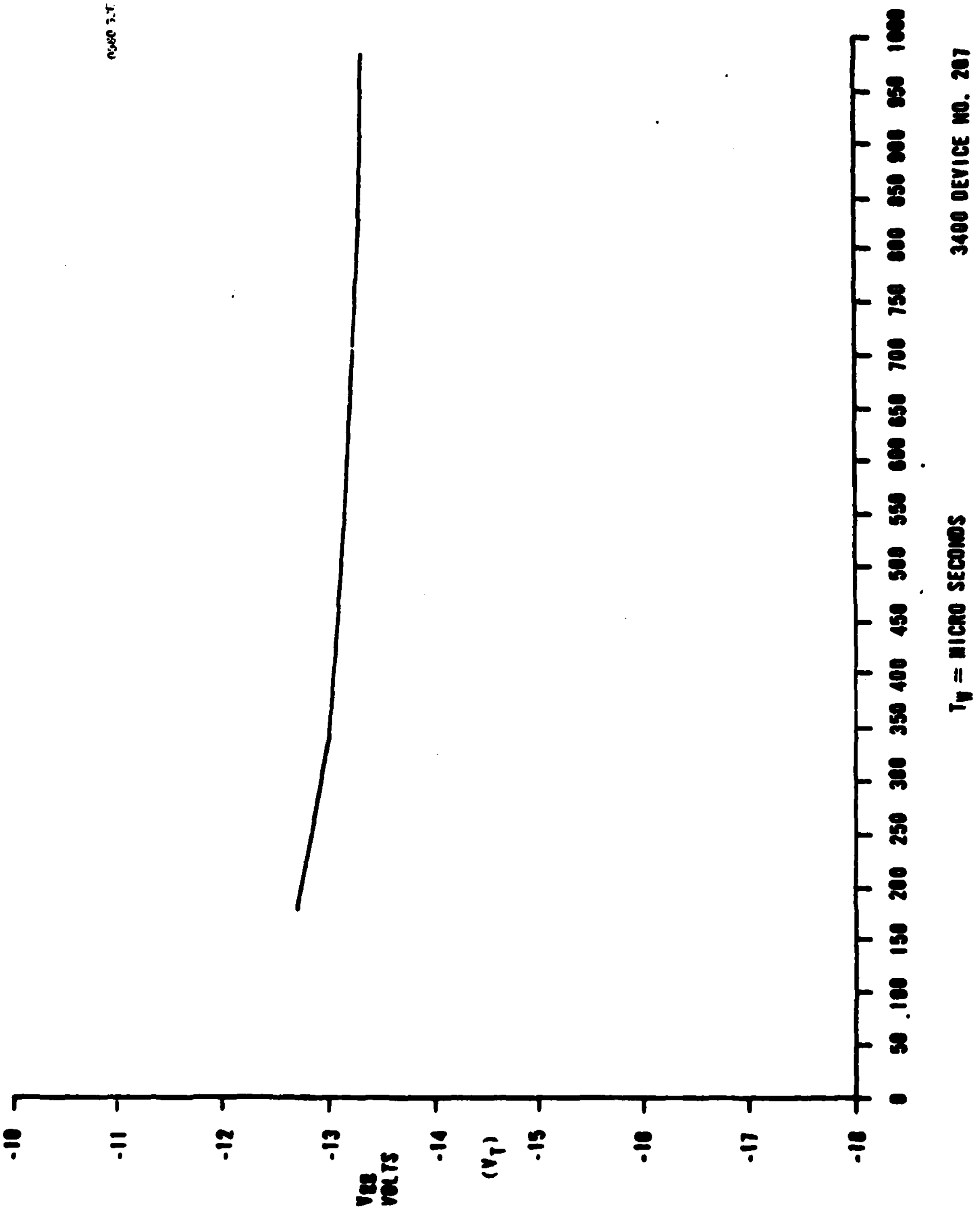


FIGURE 7-6. WRITE WIDTH VERSUS V_T 3400 NO. 207

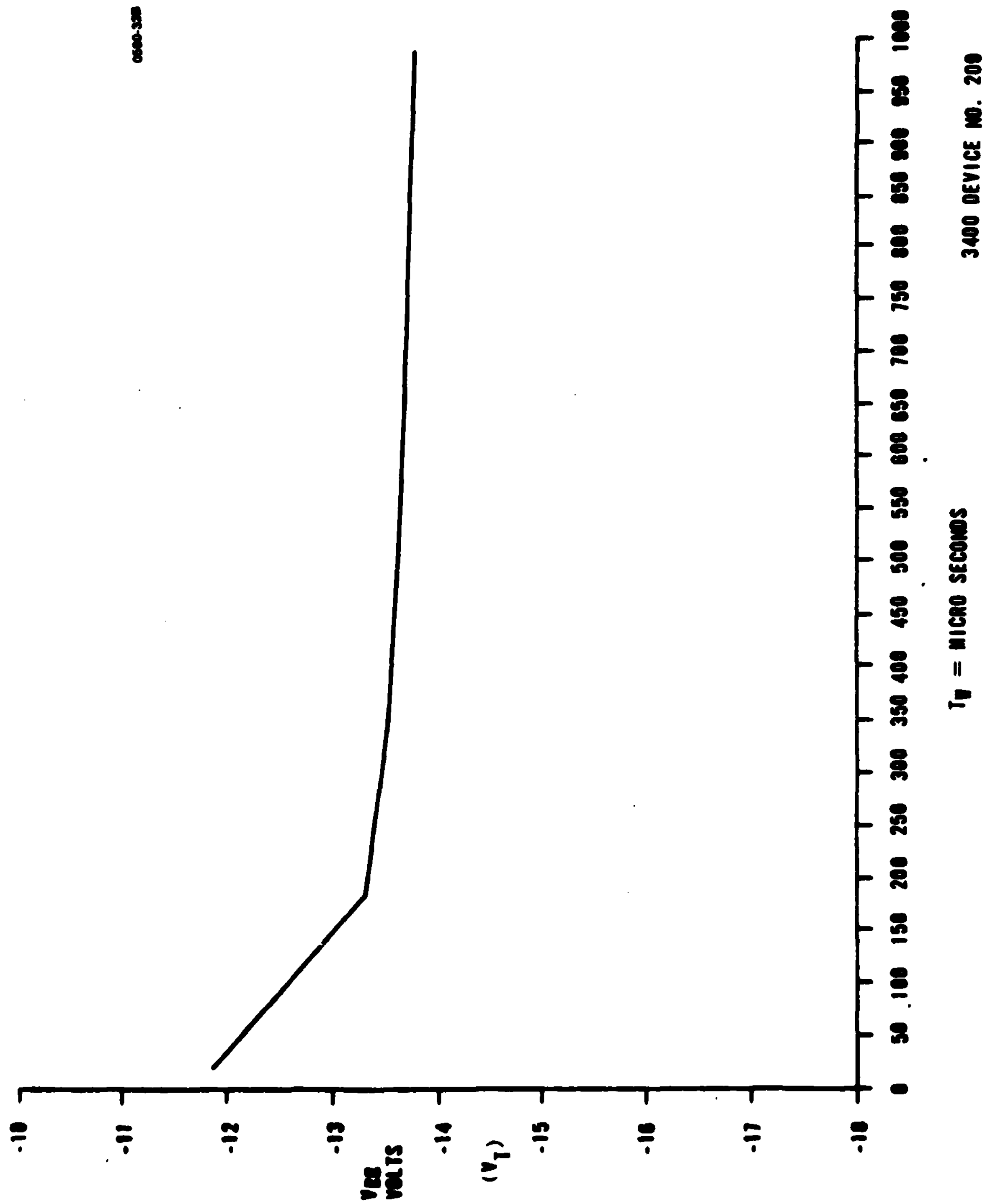


FIGURE 7-7. WRITE WIDTH VERSUS V_T 3400 NO. 209

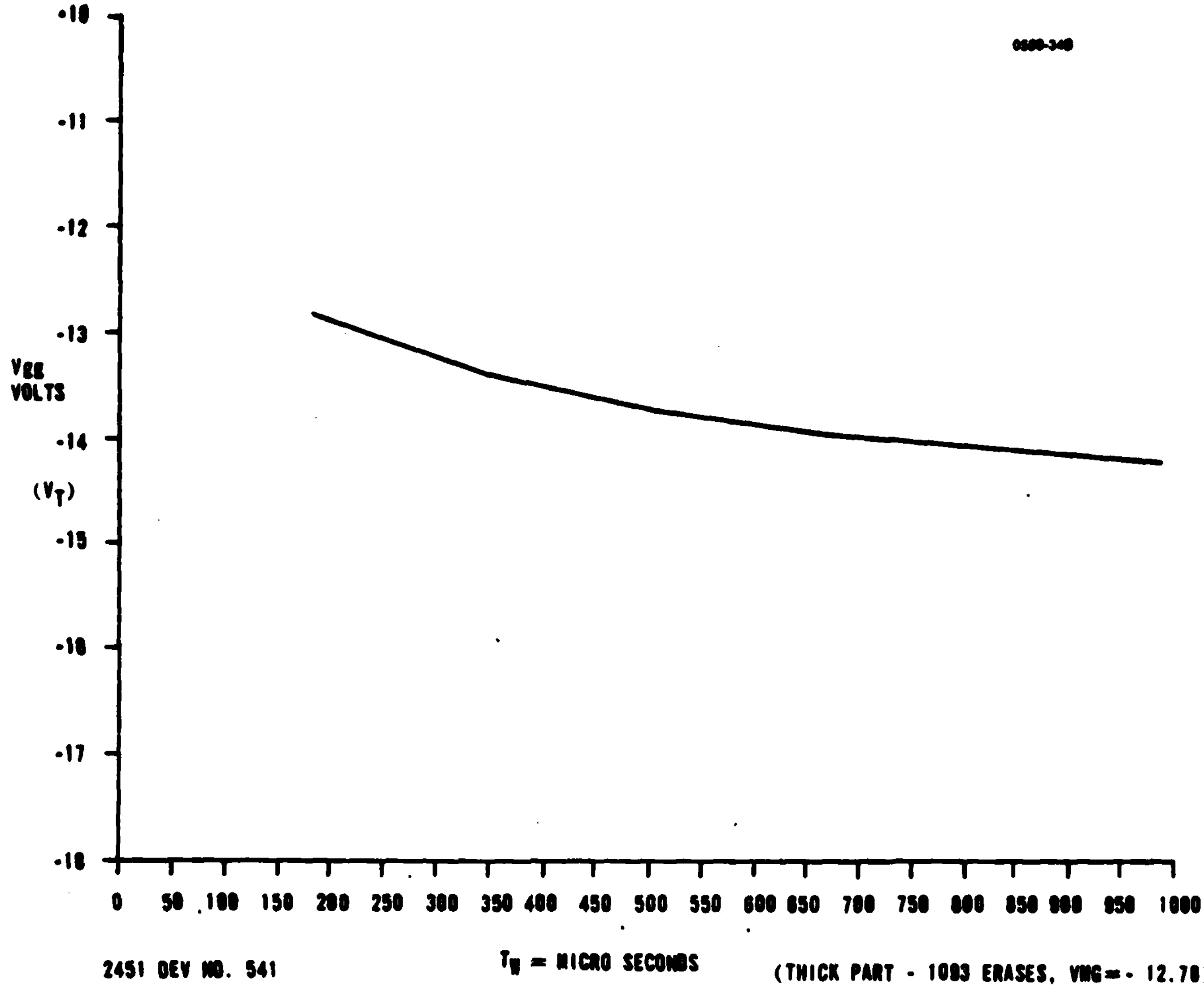


FIGURE 7-8. WRITE WIDTH VERSUS V_T 2451 NO. 541

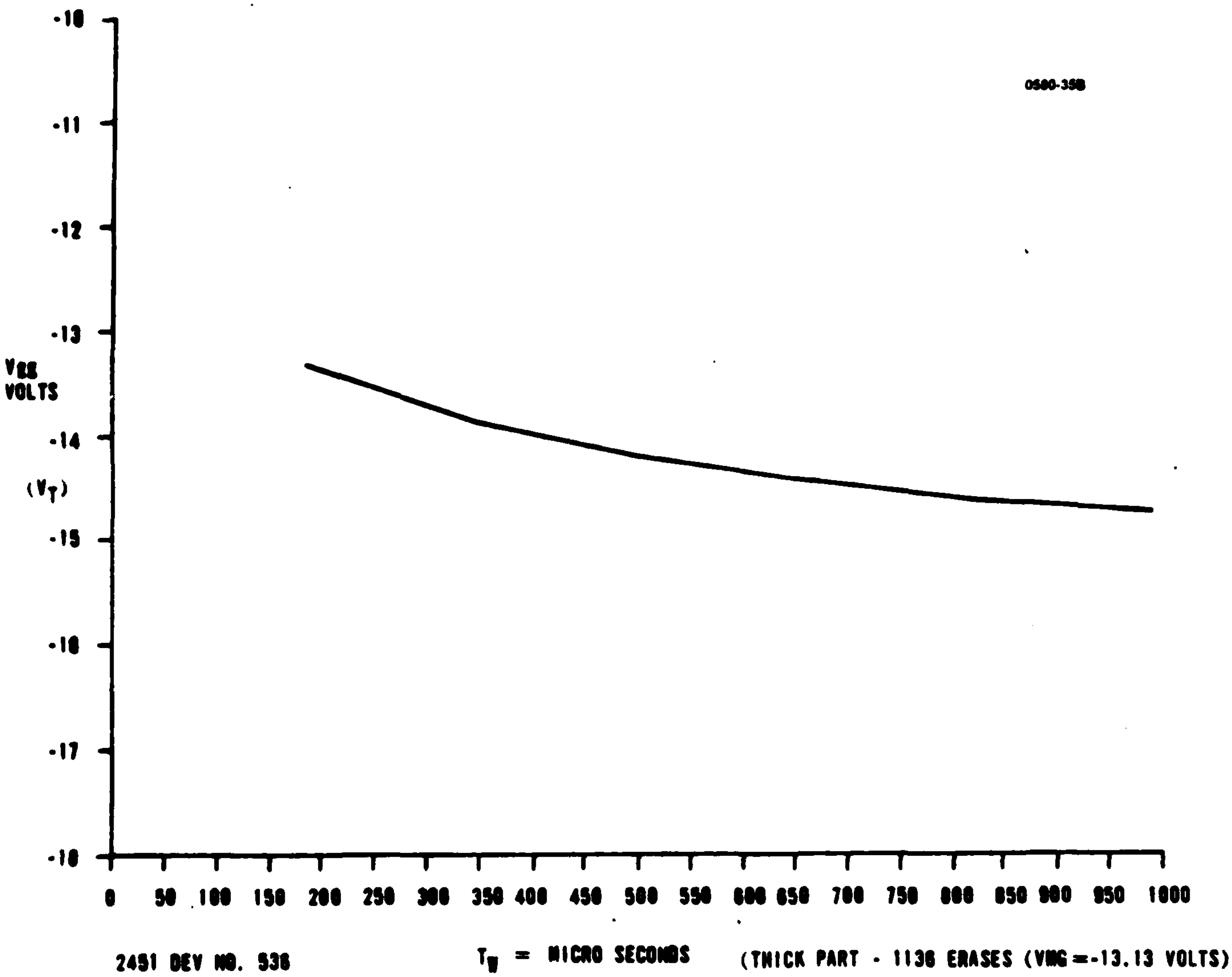


FIGURE 7-9. WRITE WIDTH VERSUS V_T 2451 NO. 536

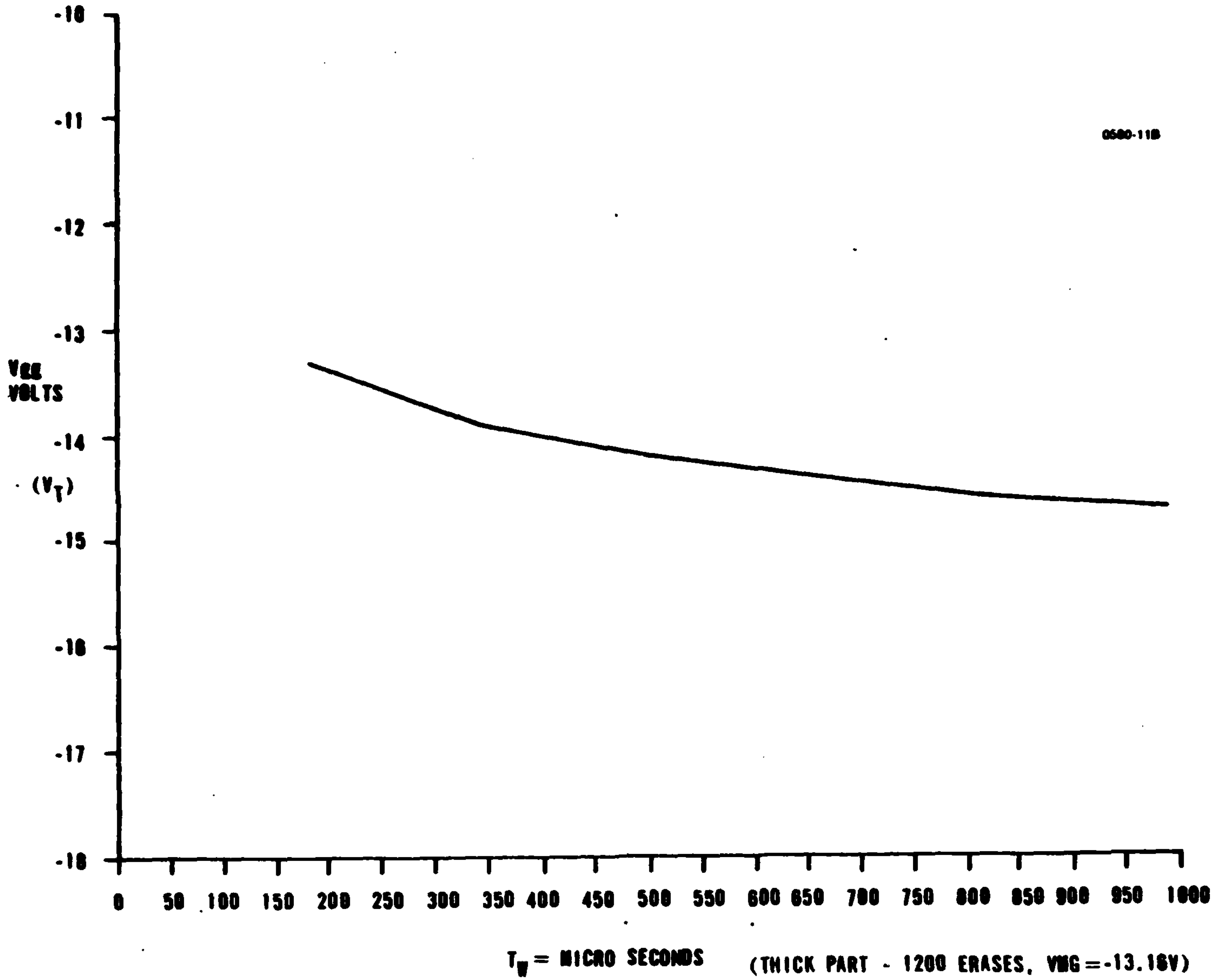


FIGURE 7-10. WRITE WIDTH VERSUS V_T 2451 NO. 533

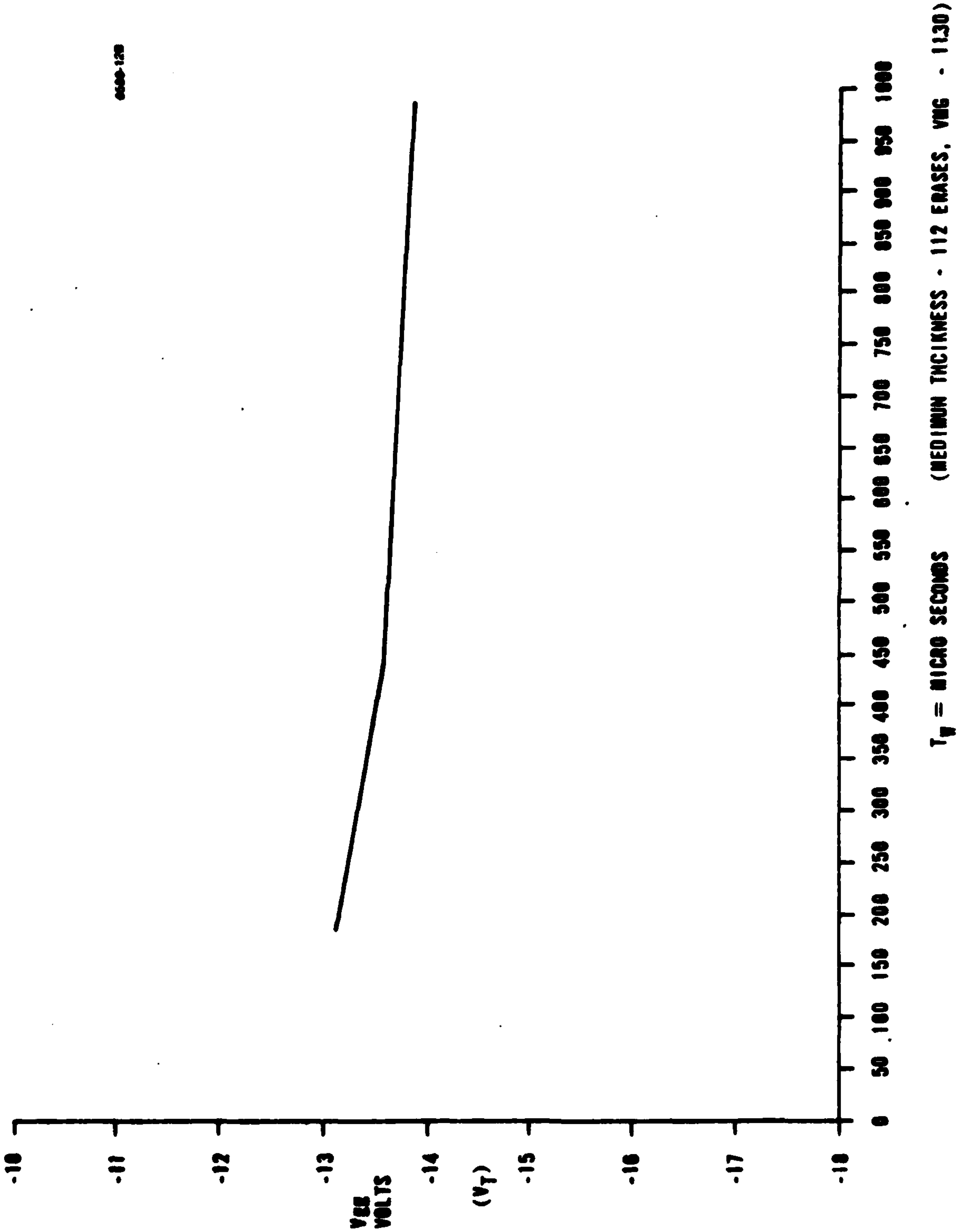


FIGURE 7-11. WRITE WIDTH VERSUS V_T 2451 NO. 504

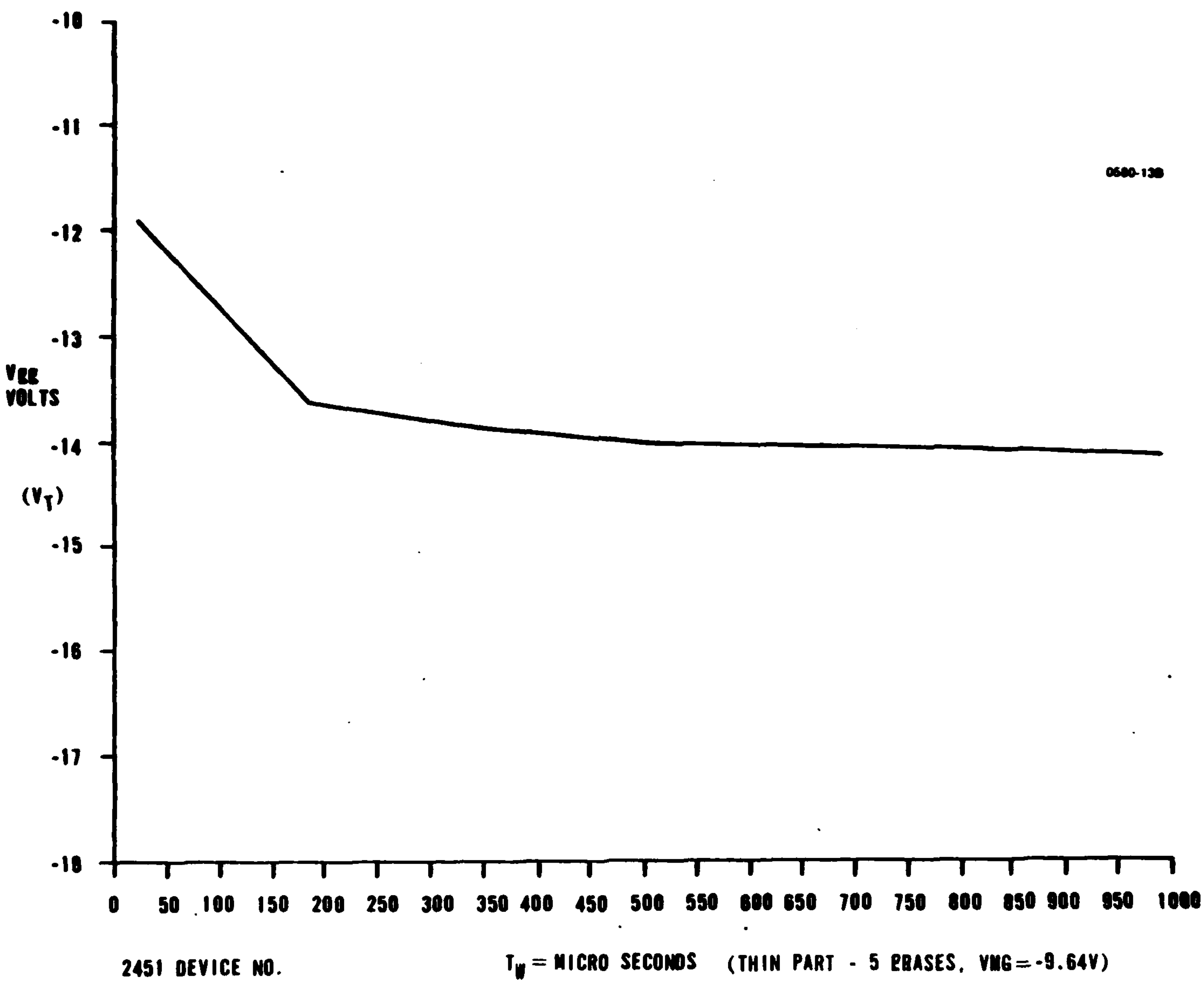


FIGURE 7-12. WRITE WIDTH VERSUS V_T 2451 NO. 509

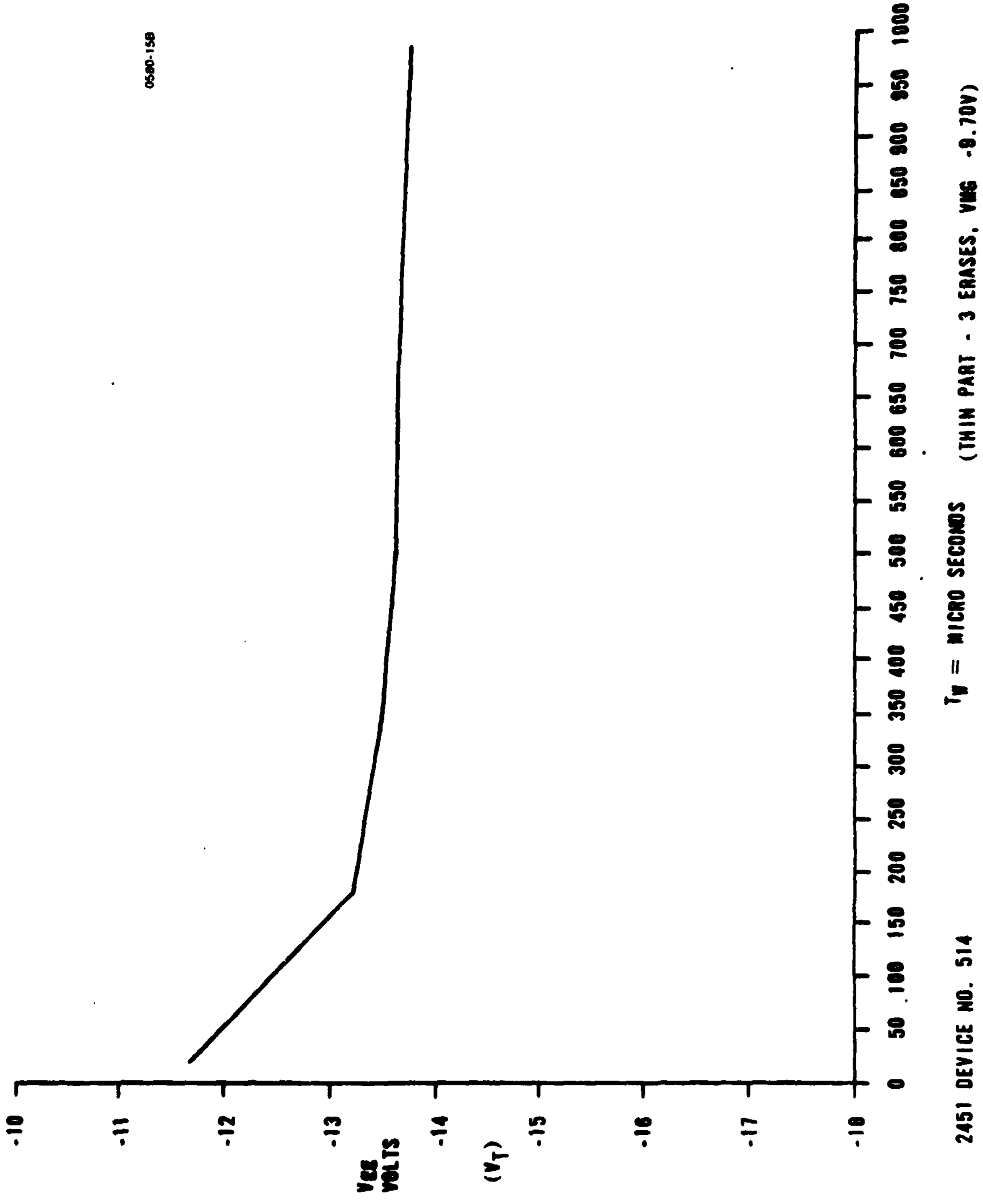


FIGURE 7-13. WRITE WIDTH VERSUS V_T 2451 NO. 514

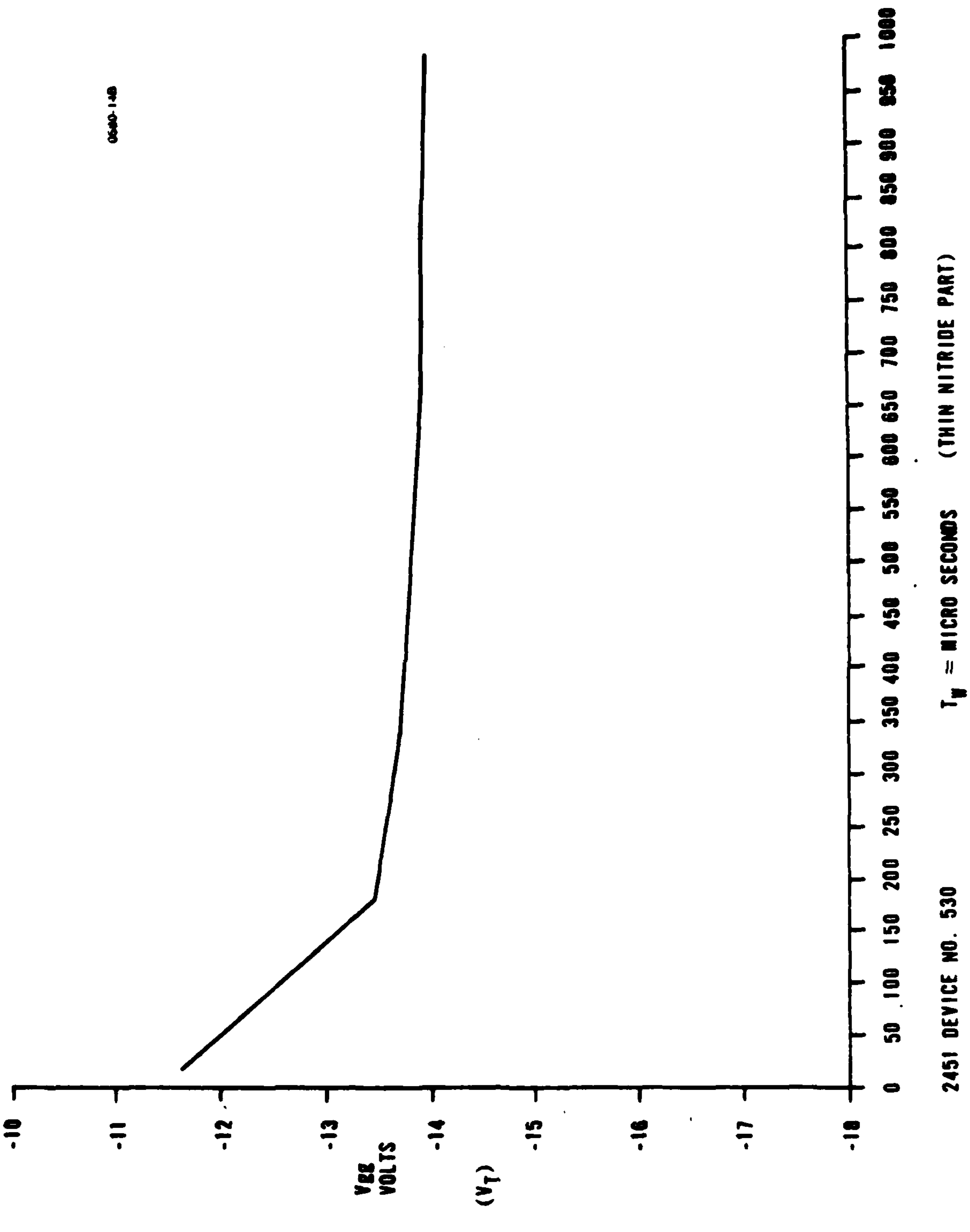


FIGURE 7-14. WRITE WIDTH VERSUS V_T 2451 NO. 530

APPENDIX A

FINAL TEST PLAN

MILITARY ADAPTATION OF A COMMERCIAL ITEM

(MACI)

PROGRAM ON MNOS EAROM(WAROM)

Prepared by:______________________________

R.W. Carter
Component Application Engineer

Approved by:______________________________

R. Wiker
Technical Director

1.0 INTRODUCTION

This final test plan details the test methods and procedures to be used for 100 percent preconditioning, screening and lot quality conformance inspection of commercial MNOS WAROM devices for use in military applications.

The sequence of tests and procedures will be as follows:

A. Device Procurement

B. 100 percent Preconditioning and Screening

C. Lot Quality Conformance Inspection

D. Deliver 50 units

E. Deliver Slash Sheet

F. Deliver Final Report

1.1 Device Type

The device type that was determined to be the most suitable for military applications in the MACI preselection phase is the 3400/2451 1024 X 4 bit Word Alterable Read Only memory (WAROM).

2.0 GENERAL

2.1 Applicable Documents

The following documents of the issue in effect on the date of this test plan, apply to the extent herein.

MIL-M-38510 Microcircuits, General Specification for

MIL-STD-883 Test Methods and Procedure for Microelectronics

2.2 Electrical Tests

2.2.1 DC Parametric Tests

DC Parametric tests will be as specified in Appendix A.

2.2.2 AC and Functional Tests

AC and Functional Tests will be as specified in Appendix B.

2.3 Device Procurement

255 devices total will be procured: 225 - from General Instrument (G.I.), and thirty from National Cash Register (NCR).

3.0 PROCEDURE

Devices will be processed according to the Final Test Plan shown in Figure 3.0.

3.1 100 Percent Preconditioning and Screening

Preconditioning and Screening will be in accordance with method 5004 of MIL-STD-883 Level B and Table 3.1 herein and will be conducted on all devices prior to lot quality conformance inspection. The following conditional Criteria will apply:

a. Burn-in Test - Burn-in circuit of Figure 3.1a will be used.

b. Interim and Final Electrical Tests - Interim electrical tests will consist of the tests specified in Appendix B-1 and B-2 at an amibient of +25°C. After a one hour soak at +125°C, the test specified in Appendix B-3 conducted and the resulting V_T values and time recorded.

   Following Burn-in, Final electrical tests will consist of the tests in Appendix B. The initial test will be that specified in B-3 at +25°C with the threshold and time recorded. The remaining tests will be performed at -55°C, +25°C and +125°C ambient using the tests specified in Appendix A and B-1.

3.2 Quality Conformance Inspection

From the devices which have successfully passed the 100 percent Class B screening, 119 samples will be submitted to the Quality Conformance Inspection requirements specified in Method 5005 of MIL-STD-883. This inspection will be composed of Group B and C tests. Group D (package related) tests were performed in the preselection phase and are not necessary to repeat. The tests and sample sizes for each group are summarized in Tables 3.2.1 and 3.2.2.

3.2.1 Group B Inspection

Group B inspection will be in accordance with Table 3.2.1 herein and as follows:

A. Subgroups 1 and 6: Physical dimensions and internal water vapor content were performed in Group D inspection and are not necessary to repeat here.

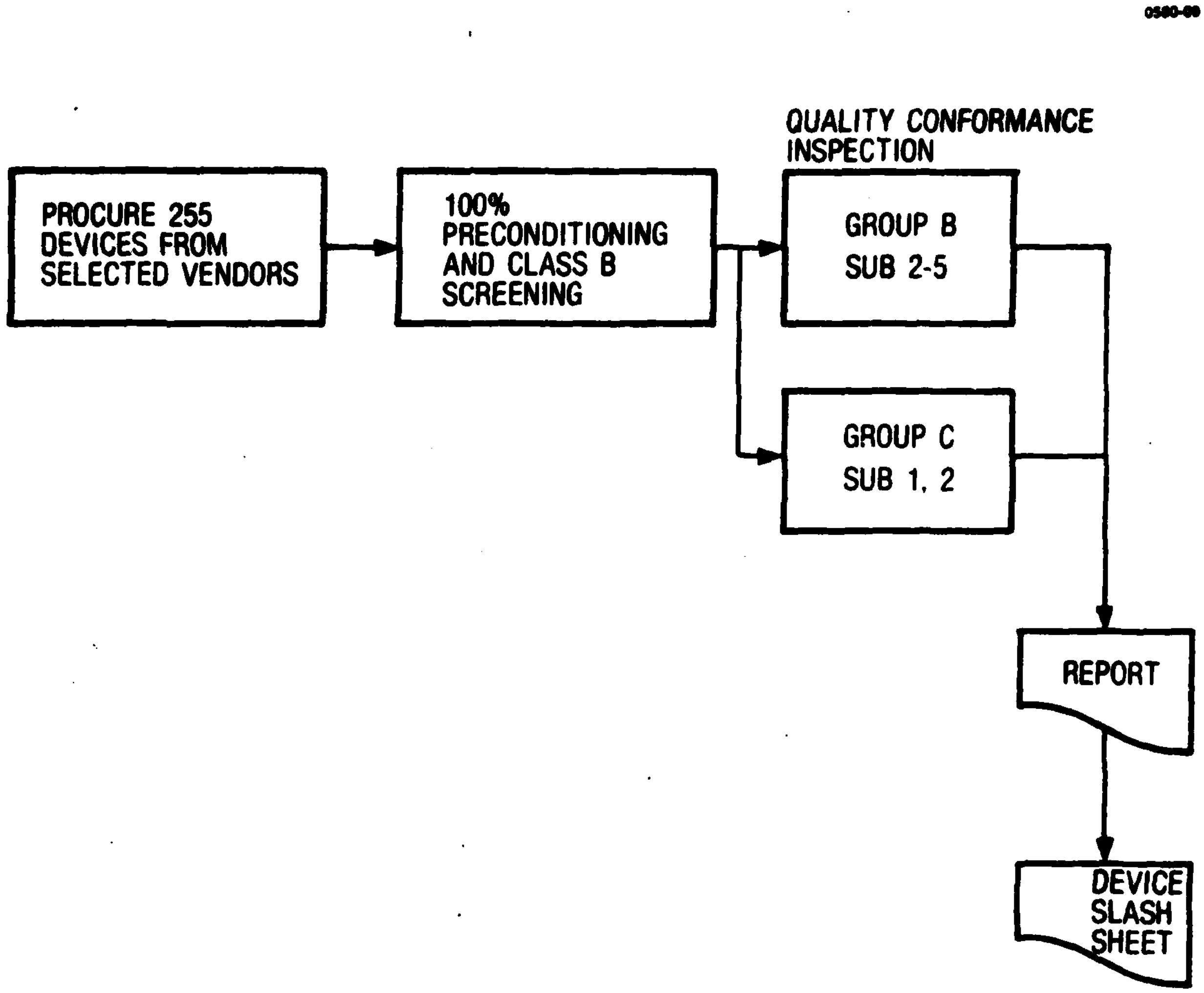


FIGURE 3-0. FINAL TEST PLAN

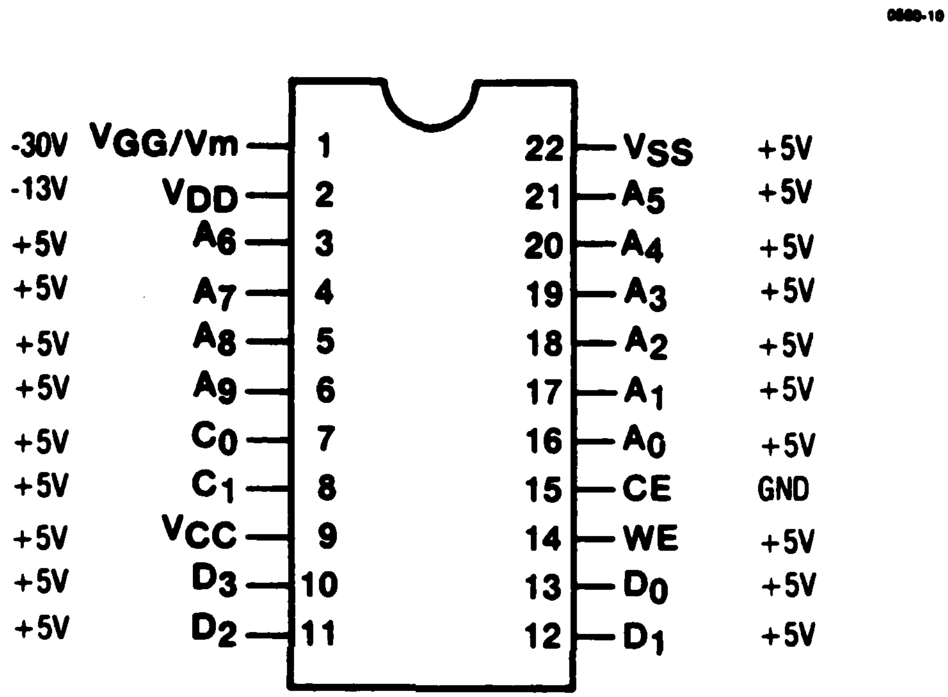


FIGURE 3-1a. BURN-IN CIRCUIT

TABLE 3.1. 100 PERCENT PRECONDITIONING AND CLASS B SCREENING TESTS

Examination of Test	MIL-STD	Method Number	Details
Stabilization Bake, No end point measurements required	883	1008.1	24 hours *1 Condition C
Temperature Cycling	883	1010.2	Condition C *2
Constant Acceleration	883	2001	Condition E Y_1 only
Seal Fine Gross Serialization Soak @ +125°C	883	2020	Condition A or B
Pre-Burn-In Electrical Test Functional Tests AC Tests		See 3.1b	
Burn-In Test	883	1015 See Fig. 3.1a	Condition C 168 hours at 125°C
Final Electrical Test DC Parametrics Functional Test AC Test		See 3.1b	
External Visual	883	2009	

TABLE 3.2.1. GROUP B TESTS 1/

Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD	Sample Size ACC#=0
Subgroup 1				
Physical dimensions 2/	2016		2 devices (no failures)	2
Subgroup 2				
Resistance to solvents	2015		3 devices (no failures)	3
Subgroup 3				
Solderability	2003	Soldering temperature of 260 ±10°C	15	3
Subgroup 4				
Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (no failures)	1
Subgroup 5				
Bond strength Thermocompression	2011	Test conditon C or D	15	10

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.

2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.

TABLE 3.2.2. GROUP C (DIE-RELATED TESTS)

Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD	Sample Size	Accept No.
<u>Subgroup 1</u>					
Steady state life test	1005	Test condition to be specified (1,000 hours at 125°C)	5	77	1
<u>Subgroup 2</u>					
Temperature cycling	1010	Test condition C	15	25	1
Constant acceleration	2001	Test conditon D Y_1 orientation only			
Seal					
(a) Fine					
(b) Gross					
Visual examination	1010 or				
End-point electrical parameters	1011				

B. All devices selected for testing will be programmed with an asymmetric slant pattern. After completion of all testing, the devices will be verified and erased (except those devices submitted for Group C testing).

3.2.2 Group C Inspection

Group C inspection will be in accordance with Table 3.2.2 herein and as follows:

A. End point electrical parameters - End point electrical parameters will be as specified in Appendix B at ambient temperatures of -55°Cm +25°C abd +125°C.

B. Steady State Life Test - Steady State life test will be performed using the circuit of Figure 3.1a.

3.3 Deliverable Devices

Of the remaining devices which have passed Group C inspection (and therefore screening), fifty devices will be selected as deliverable devices.

3.4 Final Report and Slash Sheet

The screening and lot acceptance test results will be presented in a summary report. A MIL-M-38510 type slash sheet will then be developed from this test data.

APPENDIX A

DC PARAMETRIC TESTS

FTCP

NCR 3400 FAIRCHILD 5000

*T 1 VOH

0105007A0000: 021120BA0000: 031300BA0000: 1032AAAAAAA0:

110001A1AAAA: 12A100000000: 215160701300: 251211100000:

2A0750063500: AC0005100012:

*T 2 VOL

110001AAAAAA: 214200701300: 251211100000: AA0540000000:

*T 3 ILC

1032000000A0: 110001100000: 120100000000: 211A00701600:

251718192003: 260405060708: AA2400062000:

*T 4 ILD

110000100000: A11A00701400:

*T 5 ISS

110001000000: A11A00701500:

*T 6 IGG (2451)

110001100000: 211A00701300: 251211100000: AA240006A000:

*T 7 IGG (3400)

10321111AAA0: 110001A00000: 121000000000: 2105007A0000:

AA0F31000000:

*T 8 IDD chip selected

121100000000: 10021111AAA0: 211300F00100: AA2700063000:

*T 9 IDD chip deselected (2451)

10301111AAA0: 211120800200: AA2800062900:

*T 10 IDD chip deselected (3400)

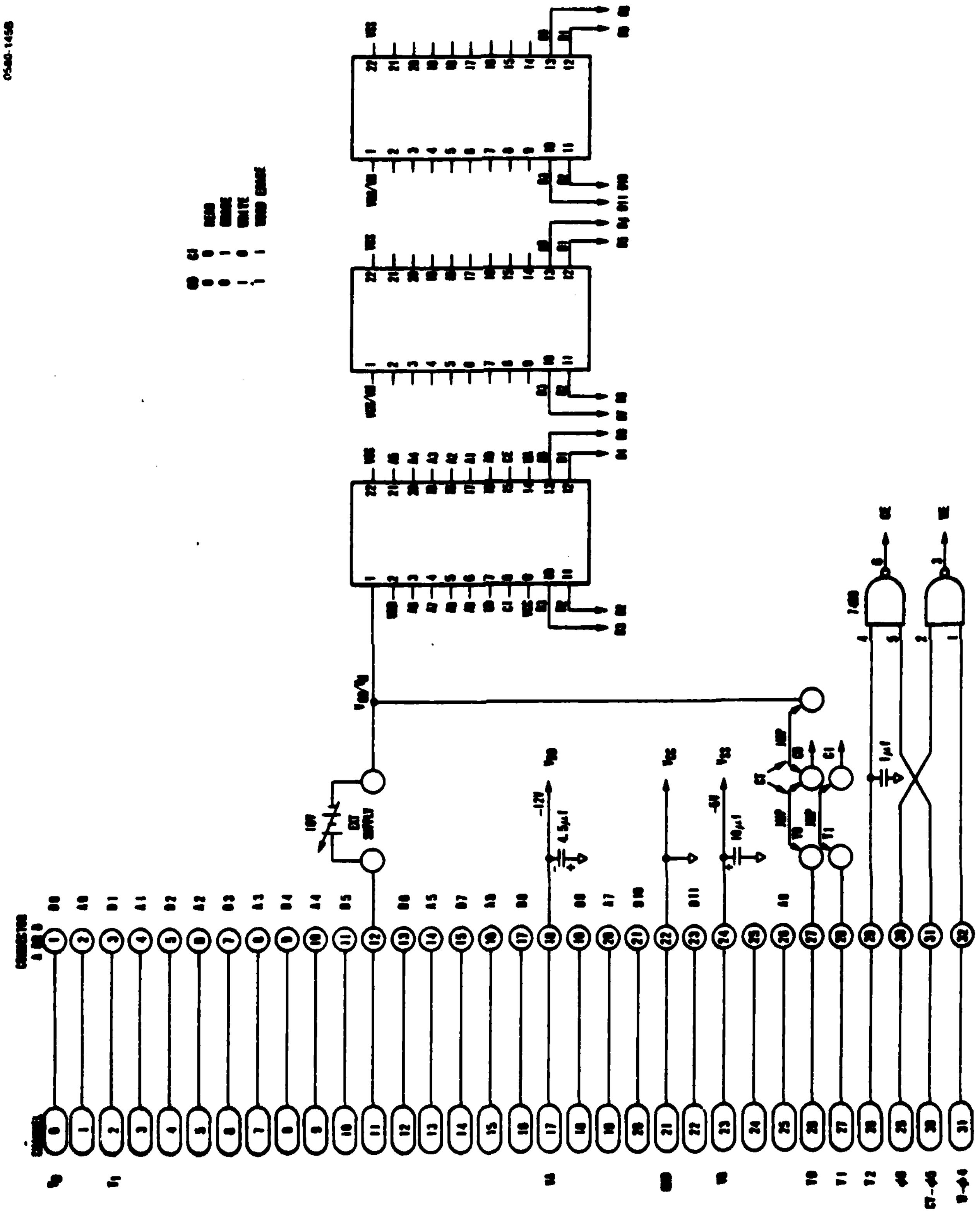
110001100000: AA2700067000:

*T 11

FFFF:

*END OF FILE.

CMD = PB



3400 TEST FIXTURE

Test	Symbol	Conditions $V_{SS} = 5.0V$	Pins	Limits	Units
Data Output High Voltage	V_{OH}	$I_{OH} = -2$ mA	D_0-D_3	3.5 min.	V
Data Output Low Voltage	V_{OL}	$I_{OL} = 2$ mA	D_0-D_3	0.4 max.	V
Control Input Leakage Current	I_{LC}	$V_{IN} = -10V$	C_0,C_1	-0.1 max.	A
Data Input Leakage Current	I_{LD}	$V_{IN} = -10V$	D_0-D_3	-0.1 max.	A
V_{SS} Supply Current	I_{SS}	$V_{DD} = -12V$ $V_{GG} = -30V$ Chip Selected	V_{SS}	29.0 max.	mA
V_{GG} Supply Current	I_{GG}	$V_{DD} = -12V$ $V_{GG} = -30V$	V_{GG}	-4 max.	mA
V_{DD} Supply Current	I_{DD}	$V_{DD} = -12V$ $V_{GG} = -30V$ Chip Selected	V_{DD}	-25.0 max.	mA
V_{DD} Supply Current	I_{DD}	$V_{DD} = -12V$ $V_{GG} = -30V$ Chip Deselected	V_{DD}	-12 max.	mA