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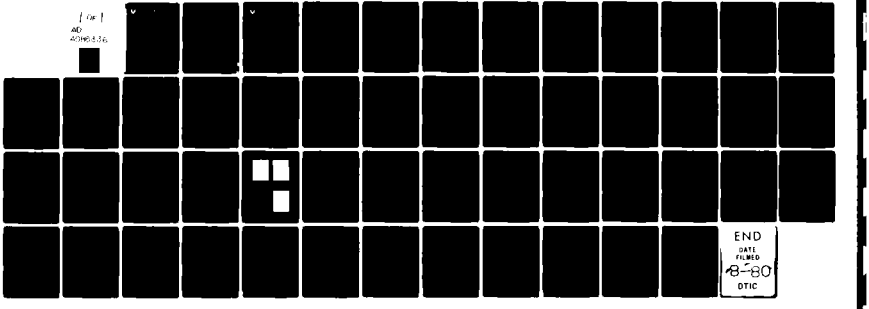

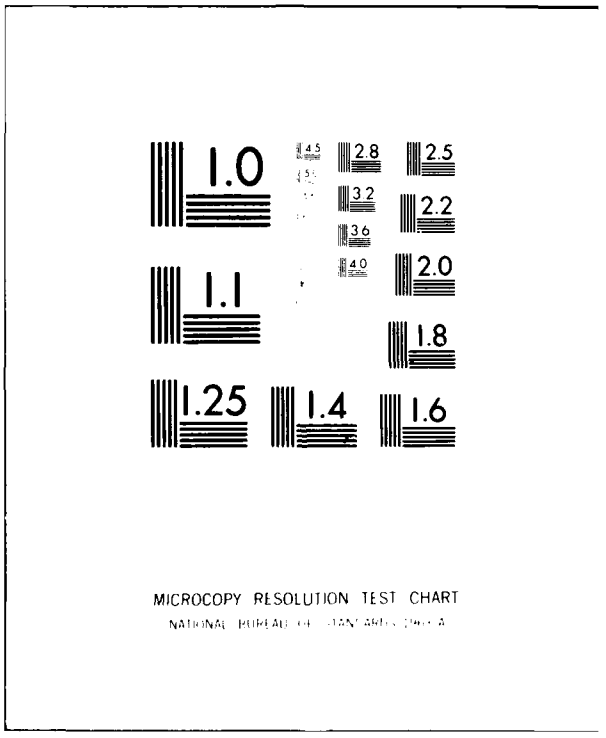
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT

DELET-TR-78-2992-3

SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHESIZER

D. J. Dodson, M. Y. Huang
TRW Inc
One Space Park
Redondo Beach, CA 90278

June 1980

Third Interim Report for Period 1 Oct 1979 - 1 April 1980

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SAW Bandpass Filters

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the program is the development of Surface Acoustic Wave (SAW) oscillator and synthesizer technology. The two year effort is planned as follows: Task I - Development of SAW devices for oscillator applications at microwave (L-band) frequencies. Emphasis to be placed on achieving wideband tuning capabilities, improved oscillator stability performance and reduced power requirements. Task II - Investigate UHF surface acoustic wave devices which can best impact on synthesizer performance parameters such as: switching speed,

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minimum frequency step size, total achievable bandwidth, short, medium and long term stability as well as maximum suppression of spurious mode level. Concurrently promising new synthesizer designs will be studied on the basis of these designs to arrive at target specification in a package providing a significant reduction in size, weight and power consumption.

Since Task I was completed prior tothis reporting period, during the third six months of the program design of the synthesizer circuitry was largely completed. SAW delay line/filters to be used in both the injection locked SAW oscillators and in the SAW Filter Bank have been designed and are being fabricated. The design of the delay lines was based partially on an investigation of the injection locking properties of SAW oscillators. RF/LSI circuitry has been processed and is currently being tested. Tests of the SP4T switch indicate a new package will be required to provide adequate isolation. This package has been designed and is being fabricated. Tests of the mix-and-divide chip have just begun. Design of the Output Module is complete and a breadboard circuit has been tested.

TABLE OF CONTENTS

		Page
1.	SUMMARY	1
2.	PROGRESS	5
	a. Tone Generation Module	5
	(1) Injection Locking Properties of SAW Oscillators	5
	(2) SAW Delay Line Design	13
	b. Synthesizer Module	16
	(1) RF/LSI Switch	16
	(2) Mix-and-Divide Chip	26
	c. Output Module	26
	(1) Frequency Doubler	26
3.	CONCLUSIONS	38

LIST OF FIGURES

Figure No.		Page
1-1	Synthesizer with Independent SAW Oscillators	3
2-1	SAW #1 Amplitude and Phase Response	7
2-2	SAW #2 Amplitude and Phase Response	8
2-3	SAW #5 Amplitude and Phase Response	9
2-4	SAW #6 Amplitude and Phase Response	10
2-5	Oscillator Bandwidth vs Injection Locking Signal Power	11
2-6	Injection Locked SAW Oscillator Bandwidth vs Passband Phase Slope	12
2-7	Split Finger Electrode Configuration	15
2-8	Reflection Coefficient, Channels 1, 2 & 3	17
2-9	Reflection Coefficient, Channel 0 and Output	18
2-10	RF/LSI SP4T Switch, Channel 0	19
2-11	RF/LSI SP4T Switch, Channel 1	20
2-12	RF/LSI SP4T Switch, Channel 2	21
2-13	RF/LSI SP4T Switch, Channel 3	22
2-14	RF/LSI SP4T Switch, Switching Speed	23
2-15	Coplanar Waveguide with Ground Plane	24
2-16	Impedance vs Ground Plane Proximity for Coplanar Waveguide	25
2-17	Output Module	28
2-18	Output Module Gain/Power Distribution	29
2-19	Frequency Doubler Design	30
2-20	Frequency Doubler - Power Out vs Power In	32
2-21	Frequency Doubler - Output vs Frequency	33
2-22	P_{OUT} vs P_{IN} at 704 MHz - Breadboard Output Module	35
2-23	P_{OUT} vs Frequency - Breadboard Output Module	36

LIST OF TABLES

Table No.		Page
1-1	Contract Specifications	2
2-1	SAW Design Parameters	14
2-2	Specification vs Expected Performance	14
2-3	ADM-1 Performance Summary (S/N 002)	27
2-4	Frequency Doubler Requirements vs Capabilities Summary	34
2-5	Frequency Synthesizer Output Module Specifications (+25°C AMB)	37

1. SUMMARY

This report covers the technical progress on program DAAB07-78-C-2992, Surface Acoustic Wave Microwave Oscillator and Frequency Synthesizer, for the period of October 1979 through March 1980. The object of the program is the development of Surface Acoustic Wave (SAW) oscillator and synthesizer technology. The incorporation of SAW technology in oscillators and frequency synthesizers will produce stable, small, light weight, low cost circuits which will be well-suited for tactical employment. The oscillator phase of the program has been completed and the results described in the second Interim Technical Report. This six-month period has been devoted to the development of a frequency synthesizer.

The synthesizer under development will be representative of that required for a JTIDS Class 3 type system. Design goals are shown in Table 1-1. TRW's approach to meeting these requirements is shown in Figure 1-1. As this block diagram indicates, the synthesizer consists of three functional modules: the Tone Generation Module, Synthesizer Module, and Output Module. The Tone Generation Module consists of four SAW oscillators generating 486, 526.5, 567, and 607.5 MHz. These oscillators are injection locked to the output of a comb generator which in turn is driven by a reference 40.5 MHz clock. The outputs of the SAW oscillators are fed to the Synthesizer Module, where they are first filtered in a SAW filter bank and then used to drive RF/LSI mix-and-divide circuitry. RF/LSI circuitry in the Synthesizer Module consists of two circuit types, a SP3T switch and a mix-and-divide chip, each used in four places. The switches select among the tones from the Tone Generation Module and feed the selected tones to the various mix-and-divide chips. The combination of tones provides 81 potential outputs with 1.5 MHz spacings. This output is fed to the Output Module where it is doubled, amplified, and filtered.

During this reporting period progress has been made on the development of each module. A summary of the progress for this period is shown below:

1) Tone Generation Module
   a) An evaluation of the fundamental injection locking properties of SAW oscillators has been completed.
   b) Based on this evaluation, SAW delay lines for the SAW oscillators have been specified, designed, and are being fabricated.

Table 1-1. CONTRACT SPECIFICATIONS

Parameter	Requirement
Frequency Range	1296-1533 MHz
Step Size	3 MHz
Spurious Suppression	-68 dBc
Frequency Stability	1×10^{-9}/sec 1×10^{-8}/month
Phase Noise	65 dBc/Hz @ 100 Hz Offset 80 dBc/Hz @ 1 KHz Offset >120 dBc/Hz @ Noise Floor
Switching Speed	<1.0 μs
Settling Time	<0.1 μs
Output Level	10 dBm ±1 dBm
Size	10 $in.^3$
Power	5W
Voltages	N/S
Digital Control Levels	N/S

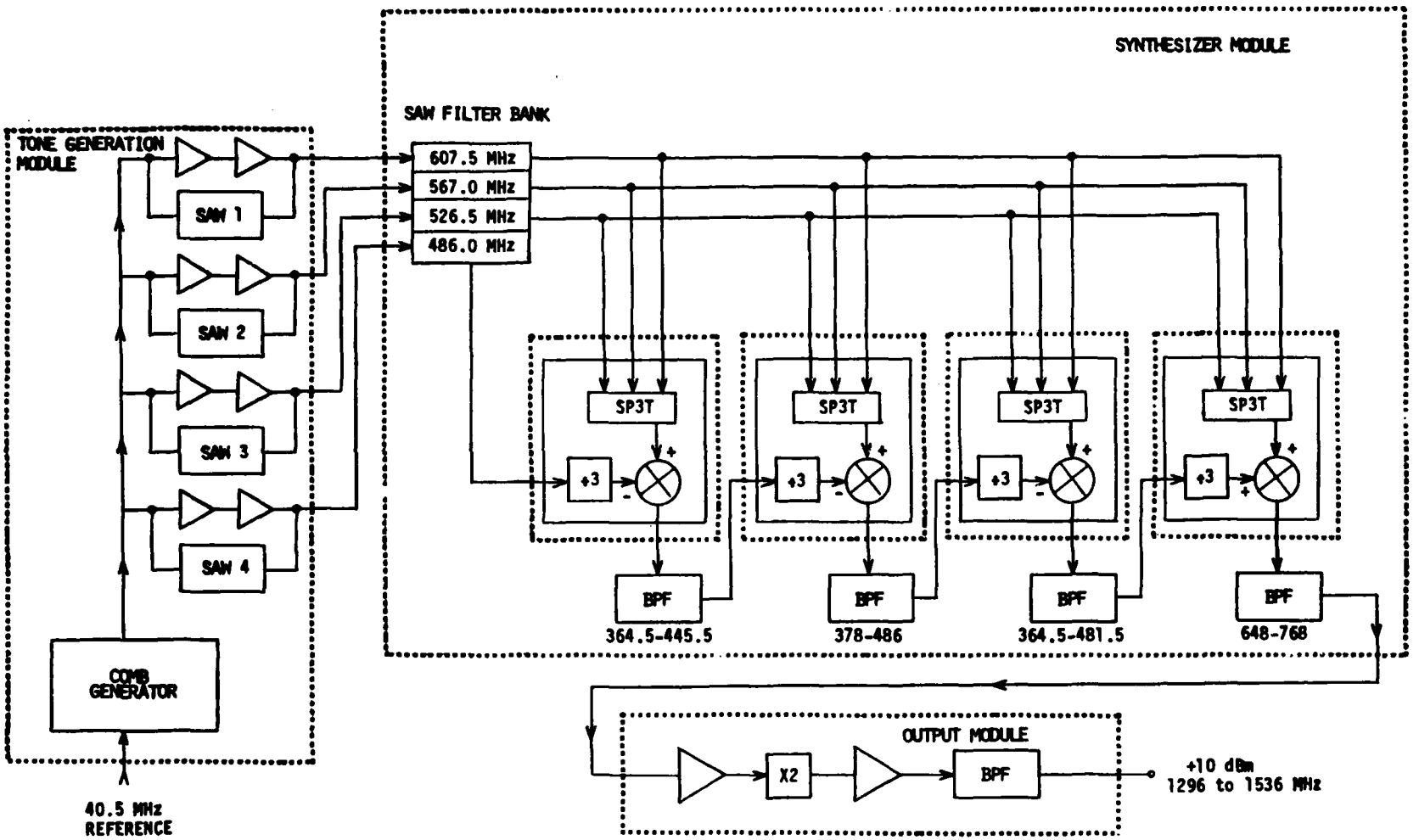


Figure 1-1. SYNTHESIZER WITH INDEPENDENT SAW OSCILLATORS

2) SAW Filter Bank

   a) The SAW filters used in the SAW Filter Bank are identical to the delay lines discussed above. These circuits have therefore been designed and are being fabricated.

3) Synthesizer Module

   a) Processing and testing of the switch are complete. The circuit is now being repackaged.

   b) Test of the mix-and-divide circuit (ADM-1) is in progress.

4) Output Module

   a) Design of the frequency doubler is complete.

   b) Conceptual design of the output module is complete.

   c) Test results on a similar breadboard (non-optimized) module show excellent characteristics.

2. PROGRESS

a. Tone Generation Module

(1) Injection Locking Properties of SAW Oscillators

As part of a parallel independent investigation in this technology area, the injection locking properties of SAW oscillators have been investigated. Injection locking bandwidth is generally expressed in terms of circuit Q and a ratio of injected and oscillator output voltages:

$$BW = \frac{\omega_o}{Q}\left(\frac{E_1}{E_o}\right) = \frac{\omega_o}{Q}\left(\frac{P_1}{P_o}\right)^{1/2}$$

where

E_1, P_1 = injected voltage or power

E_o, P_o = oscillator output voltage or power

ω_o = oscillator frequency

Q = oscillator output circuit Q.

This expression is based on Adler's[1] formulation of injection locking. Taking Adler's theory, we proceeded to modify it for injection locked SAW oscillators. We first note that phase slope is a more suitable measure of SAW filter properties than circuit Q.

Q is defined as the ratio of the oscillator frequency to half power bandwidth.

For a single tuned circuit, textbooks give

$$\tan \phi = 2Q\left(\frac{\omega - \omega_o}{\omega_o}\right)$$

For small angles, the tangent function can be approximated as

$$\phi = 2Q\left(\frac{\omega - \omega_o}{\omega_o}\right)$$

Defining A as the phase slope, $\frac{d\phi}{d\omega}$,

$$A \simeq \frac{\Delta\phi}{\Delta\omega} = \frac{2Q}{\omega_o}$$

[1]Robert Adler, "A Study of Locking Phenomena in Oscillators", Proc. IRE and Waves and Electrons, June 1946, pp. 351-357.

Substituting this relationship into Adler's equation,

$$BW = \frac{2}{A}\left(\frac{P_1}{P_o}\right)^{1/2}$$

However, P_1 and P_o must be carefully defined when applied to a SAW oscillator since power is not injected into the circuit output but at a low power point in the loop. It appears that the significant parameter is the ratio of injected voltage to feedback voltage. With these considerations, injection locking bandwidth for a SAW oscillator can be restated as

$$BW = \frac{2}{A}\left(\frac{P_{INJ}}{P_{FB}}\right)^{1/2} \qquad \text{or}$$

$$\Delta\omega = \frac{1}{A}\left(\frac{P_{INJ}}{P_{FB}}\right)^{1/2}$$

where

$\Delta\omega$ = one-sided injection locking bandwidth (in radians/sec)

A = phase slope

P_{INJ} = injection locking power

P_{FB} = oscillator feedback power at point of injection.

Based on this restatement of Adler's formula, SAW oscillators with delay lines of various phase slope have been characterized. Four oscillators were constructed using SAWs with passbands and phase slopes shown in Figures 2-1 through 2-4. Note the different phase slopes for these delay lines:

SAW No.	°/MHz
1	66.3
2	720
5	1200
6	144

The injection locking properties of these oscillators are shown in Figures 2-5 and 2-6. Figure 2-5 is a plot of measured injection locking bandwidth (two-sided) vs injection locking power for the four SAW filters. Note that increasing phase slope reduces injection locking bandwidth as predicted. Also these curves show the dependence of bandwidth on the square root of power as required by the theory. Figure 2-6 is a plot of the injection locking bandwidth equation with points measured from Figure 2-5 superimposed. This plot clearly shows the excellent agreement of injection locked SAW oscillators to Adler's theory as modified herein.

Figure 2-1. SAW #1 AMPLITUDE AND PHASE RESPONSE

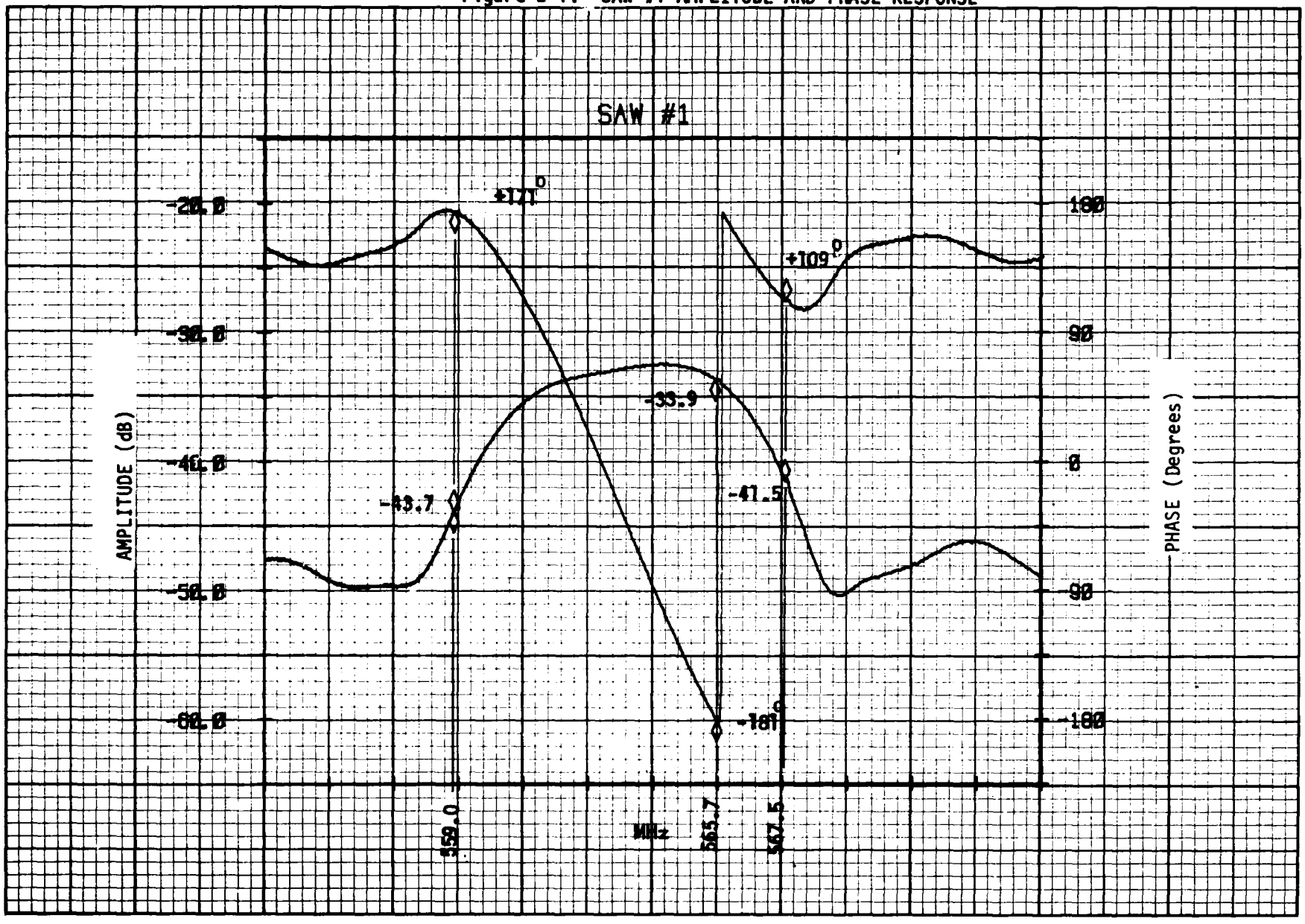


Figure 2-2. SAW #2 AMPLITUDE AND PHASE RESPONSE

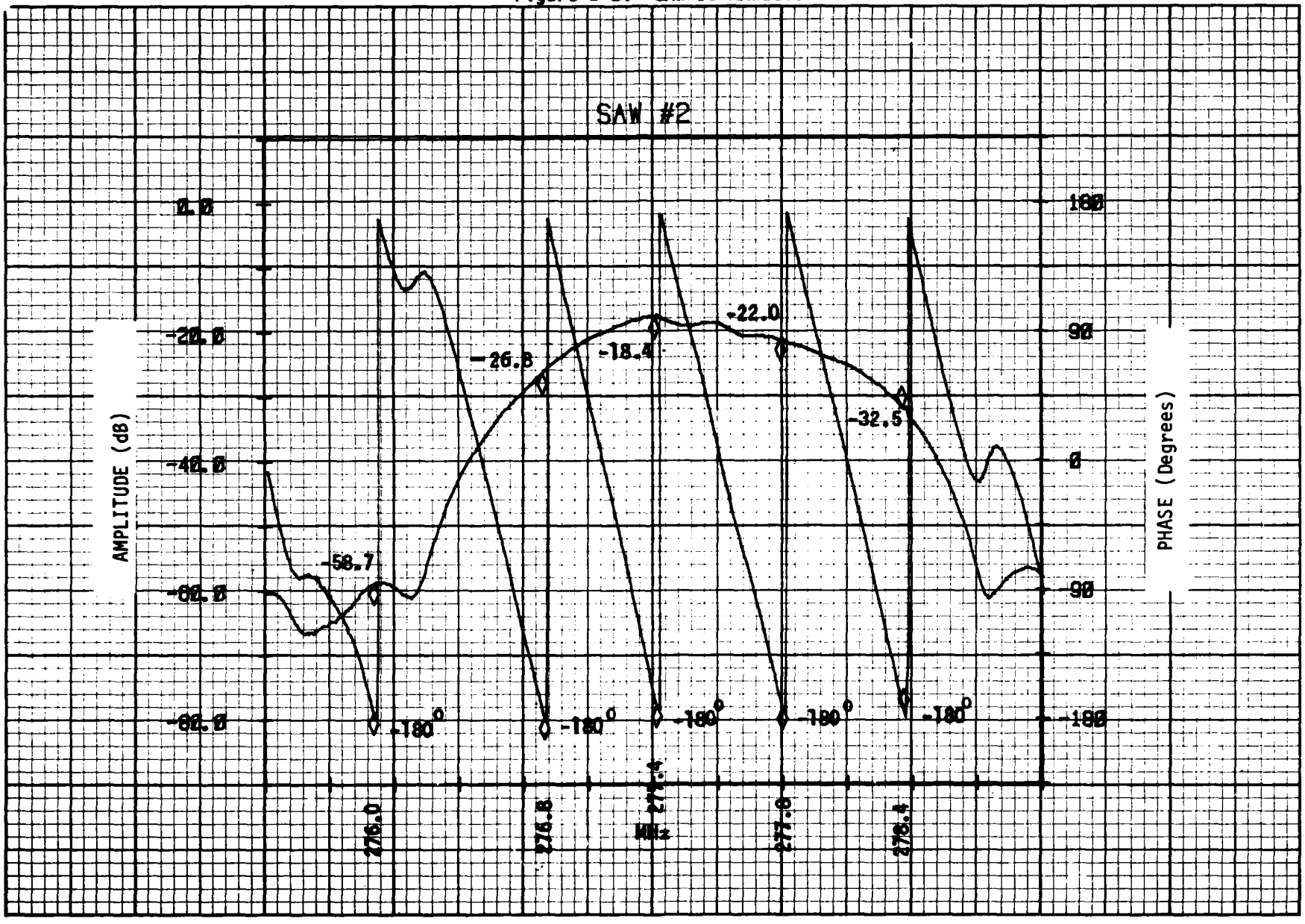


Figure 2-3. SAW #5 AMPLITUDE AND PHASE RESPONSE

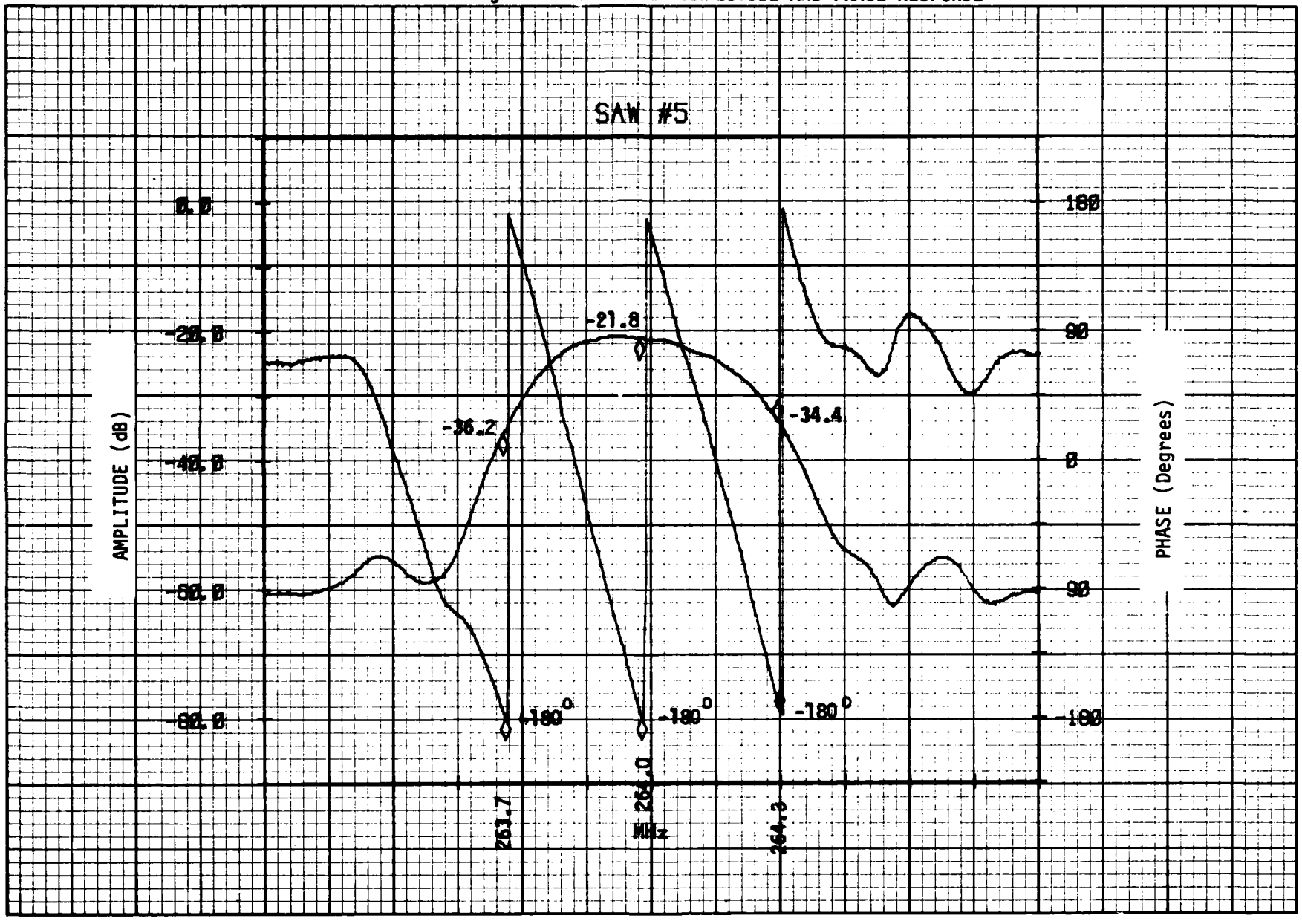


Figure 2-4. SAW #6 AMPLITUDE AND PHASE RESPONSE

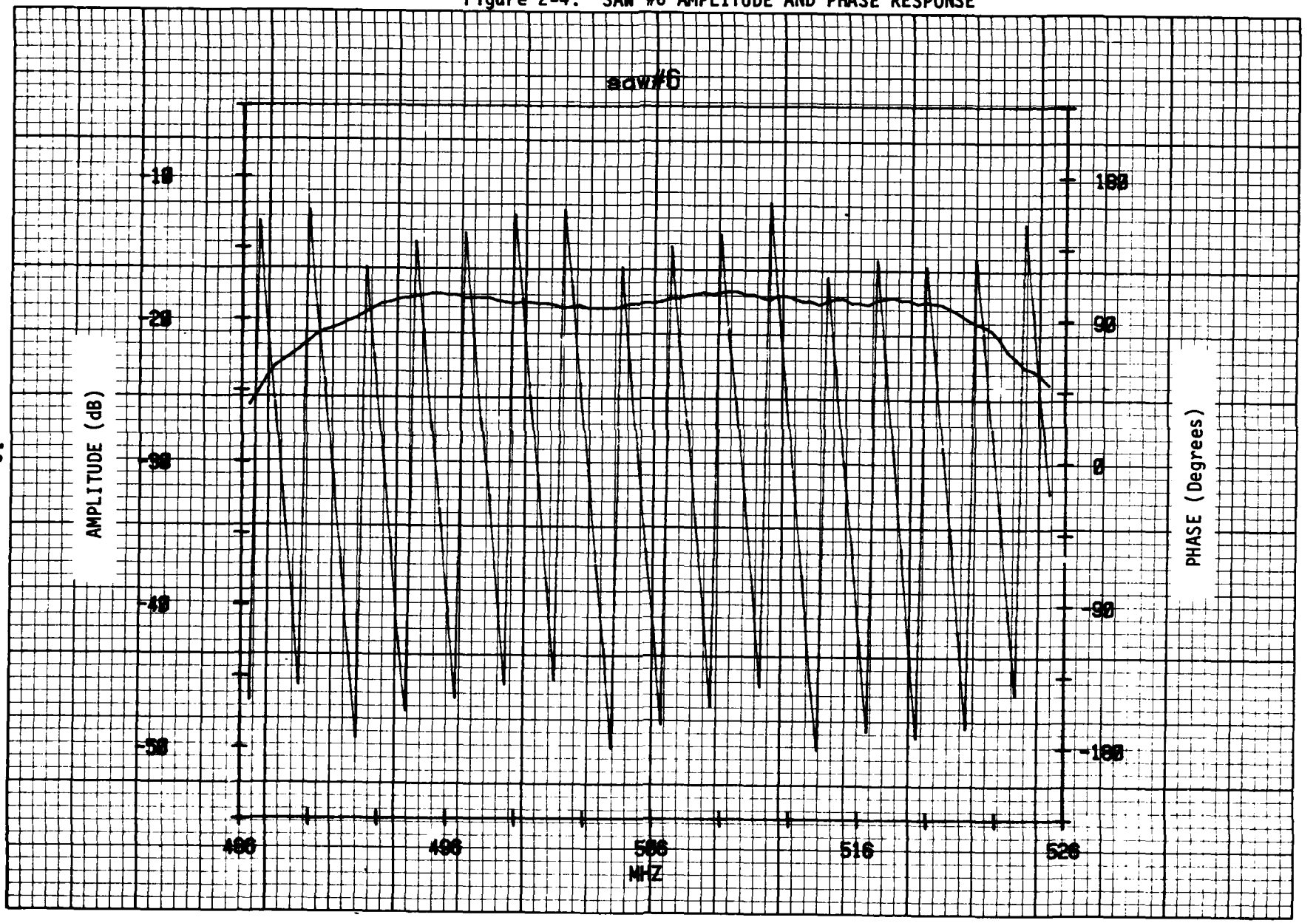


Figure 2-5. OSCILLATOR BANDWIDTH vs. INJECTION LOCKING SIGNAL POWER

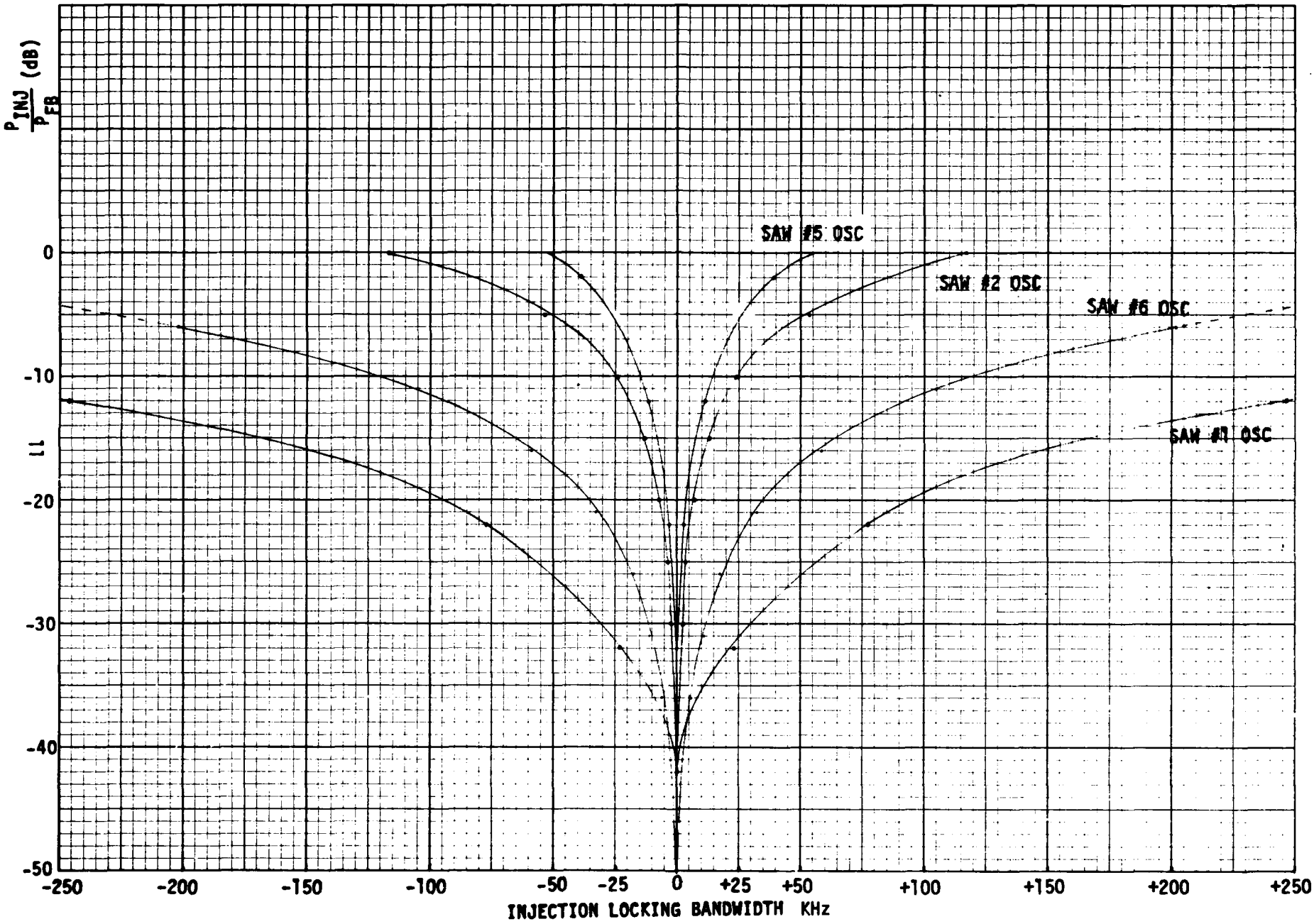
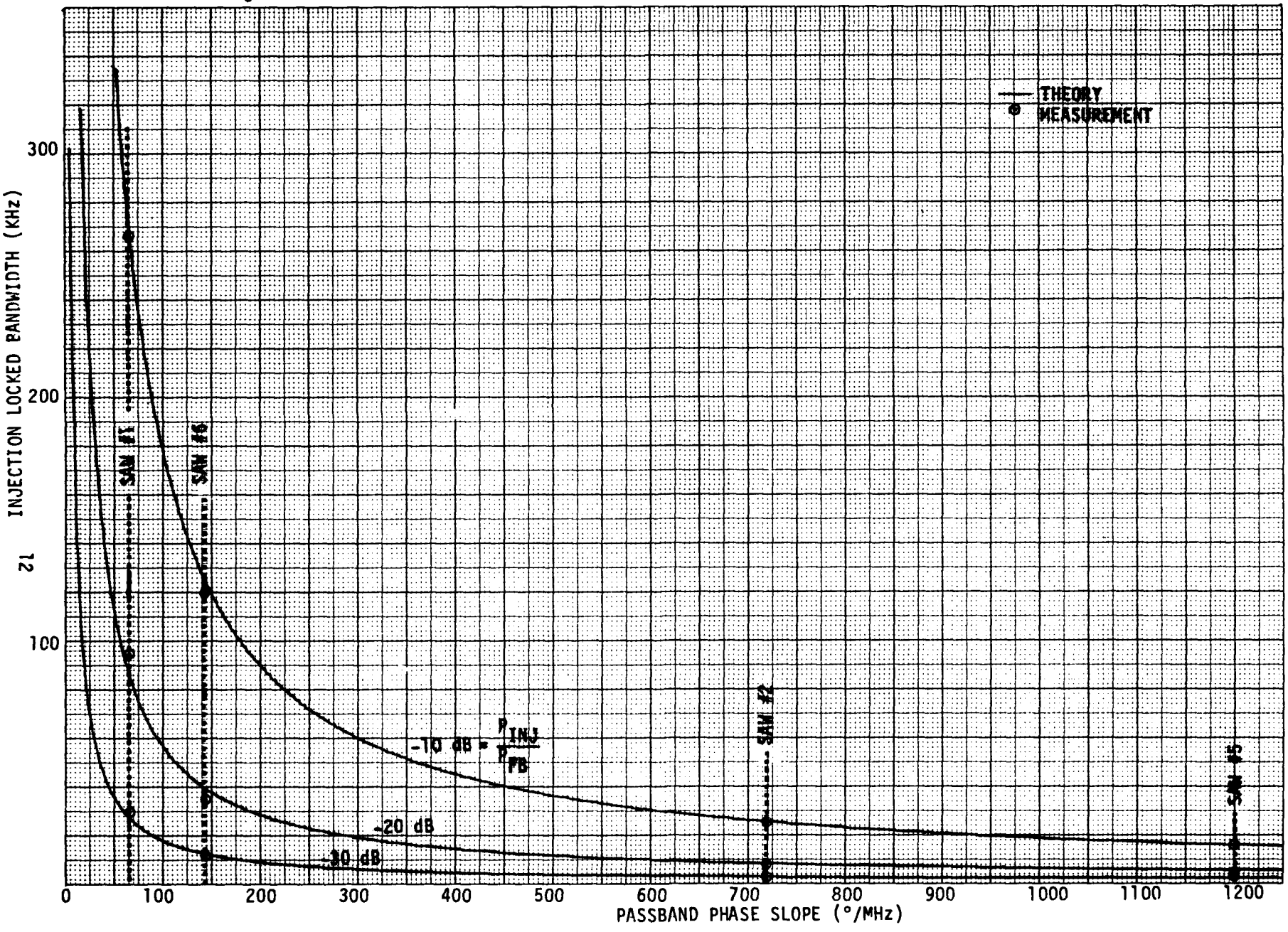


Figure 2-6. INJECTION LOCKED SAW OSCILLATOR BANDWIDTH vs PASSBAND PHASE SLOPE



These measurements have shown that phase slope is a critical parameter in the design of SAW delay lines to be used in injection locked oscillators. Based on these measurements, specifications for the designs of the SAWs for this program have been generated. These designs are discussed in detail in the following section.

(2) SAW Delay Line Design

The SAW devices used in the frequency synthesizer tone generation module consist of four delay lines with center frequencies at 486, 526.5, 567.0 and 607.5 MHz. The specifications for these delay lines are such that techniques used in the design of delay lines for the microwave oscillator part of the program can be directly applicable. In the microwave oscillator SAW delay line design, each delay line consists of two identical transducers with split electrode configuration. The transducers operate at the third harmonic and the finger width stays well within the resolution limit of conventional photolithographic techniques. The design of the present delay lines is identical. One basic design is employed for the four different frequencies by simply scaling the dimensions according to the frequency ratios. The schematic of the delay line configuration is shown in Figure 2-7.

The substrate chosen for these delay lines is CT cut quartz with $\theta = 38°$. The reason for using the CT cut instead of the ST is due to the fact that nearly half of the substrate surface in the SAW delay line region is covered with aluminum metallization. This metallization lowers the turnover temperature or the temperature at which the SAW center frequency exhibits minimum frequency change. With the presence of this metallization, the most temperature stable cut is no longer ST-cut but is CT-cut, when the proper metallization thickness is employed.

The design parameters including the metallization thickness are summarized in Table 2-1. Table 2-2 summarizes the specifications as compared to the expected performance characteristics.

Table 2-1. SAW Design Parameters

Center Frequency (MHz)	No. of Pairs Per Transducer	Acoustic Aperture (λ_0)*	Finger Width (μm)	Center-to-Center Separation Between Transducers (λ_0)	Al Metallization Thickness (Å)
486.0	32	90	2.43	105	750
526.5	32	90	2.24	105	700
567.0	32	90	2.08	105	650
607.5	32	90	1.94	105	600

* λ_0 = Acoustic wavelength at the center frequency.

Table 2-2. Specification vs. Expected Performance

	Specification	Capability
Center Frequency	486.0, 526.5 567.0, 607.5	Compliance
Insertion Loss (dB)	≤ 25 dB Tuned	≤ 24 dB Tuned
Delay Time, τ (usec)	≤ 0.25	0.22, 0.20 0.19, 0.17
3 dB Bandwidth	≤ $1/\tau$*	Compliance

* Condition for single mode operation.

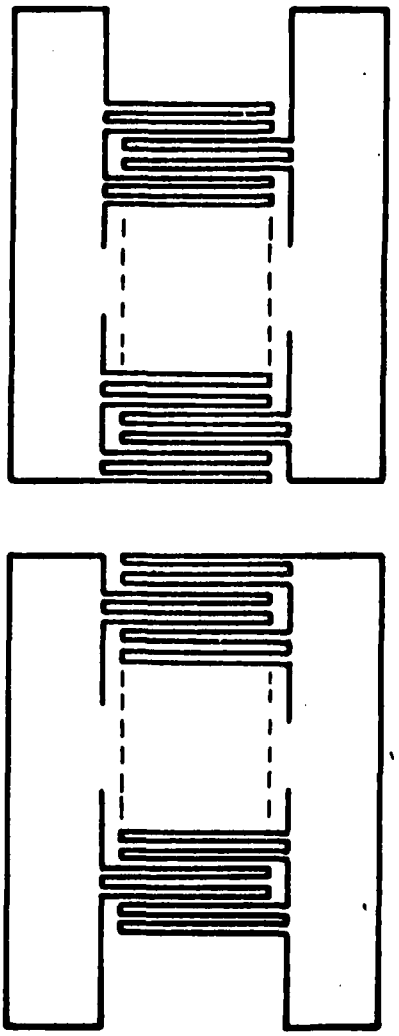


Figure 2-7. Split Finger Electrode Configuration

b. Synthesizer Module

The synthesizer module consists of four identical functions for selecting the desired frequency tone and mixing and dividing this tone. Each function consists of two RF/LSI chips, a switch, and a mix-and-divide (ADM) circuit. Although these two circuit functions could easily have been designed on the same wafer, they were fabricated on two physically separate wafers so additional electrical isolation could be obtained from the physical separation.

(1) RF/LSI Switch

The RF/LSI switch has been processed and tested. The circuit schematics were shown in the Second Interim Report and are not repeated here. The circuit has been designed to be a pin programmable SP3T or SP4T switch. Although the circuit will be used as a SP3T switch in the synthesizer, data on all four inputs is included in this report for completeness. The switch parameters which have been characterized include input and output reflection coefficient, transducer gain, bandwidth, switching speed and isolation.

Reflection coefficients are shown in Figures 2-8 and 2-9. The magnitude of the reflection coefficient for all ports is approximately .88. This represents approximately 13 dB mismatch loss and indicates the switch will require matching networks. Transducer gain is shown in Figures 2-10 through 2-13. In-band gain is between 2 and 5 dB (for an "ON" channel). Once matched, an "ON" channel will provide 15 to 18 dB of gain. Bandwidth is also shown in Figures 2-10 through 2-13. The 3 dB bandwidth is 600 MHz, and the switch shows available gain well beyond 1300 MHz.

Switching speed has been measured to be between 10 and 20 ns. Figure 2-14 shows oscilloscope photographs of both the switch command signal and the switched RF signal. The dot pattern representing the RF signal results from using a sampling scope. The RF signal for these measurements was approximately 500 MHz. Switching speeds of 20 ns are well within the synthesizer requirements.

NAME	TITLE REFLECTION COEFFICIENT, CHANNEL 1,2,3	DWG. NO.
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE

IMPEDANCE OR ADMITTANCE COORDINATES

f = 300-1300 MHz

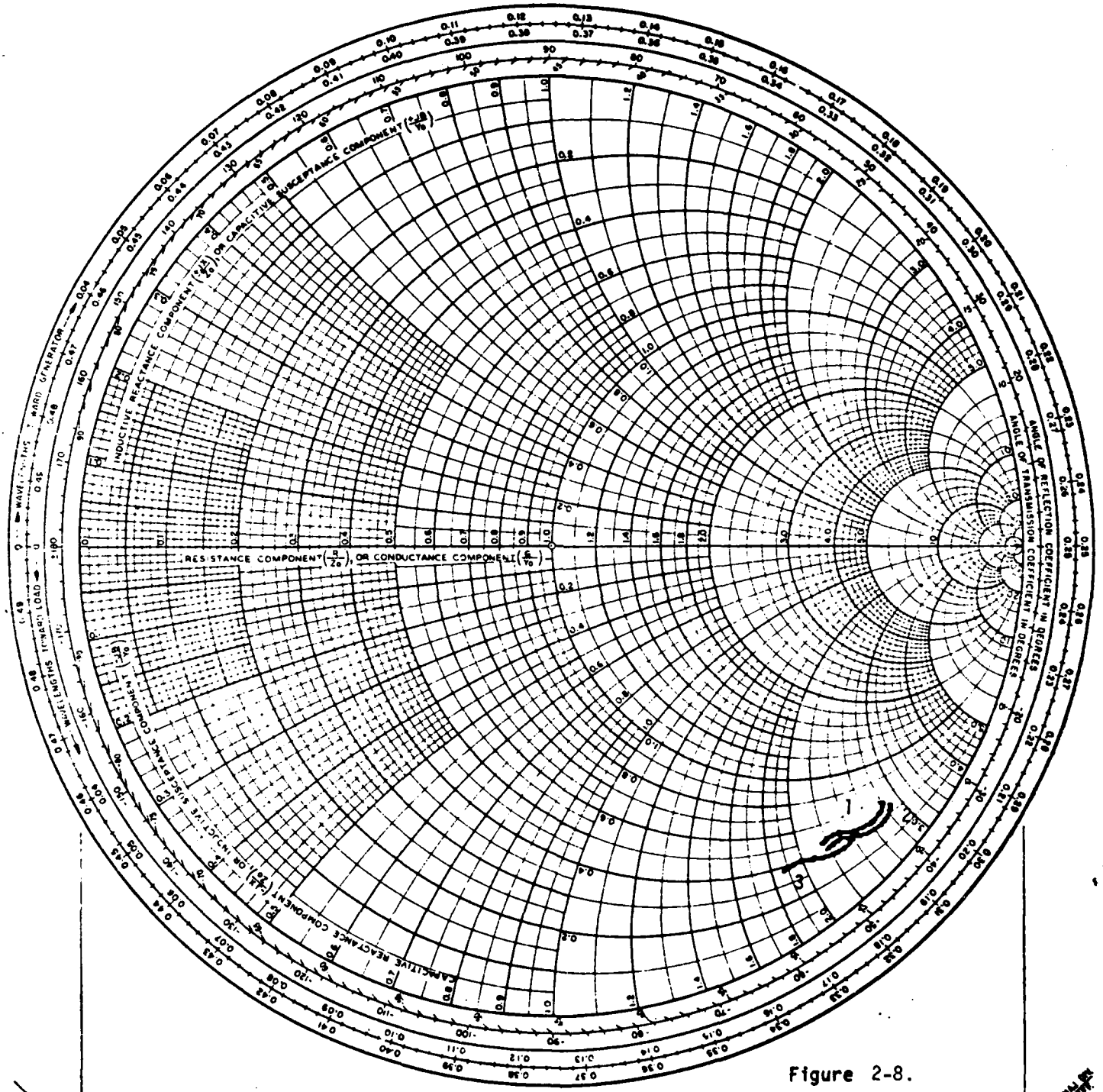
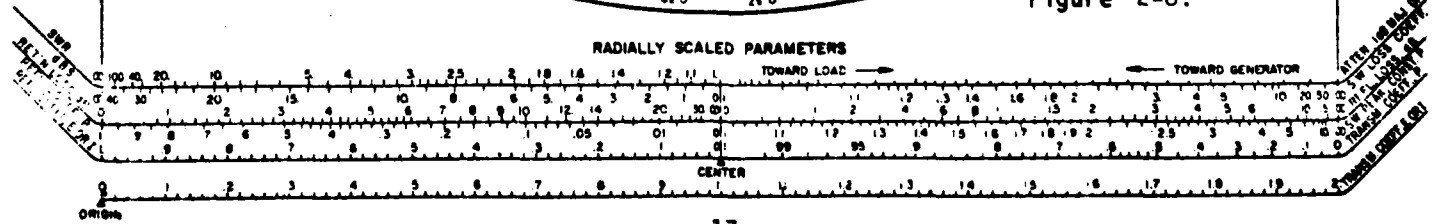


Figure 2-8.



A MEDA-CHART

NAME	TITLE REFLECTION COEFFICIENT, CHANNEL 0 AND OUTPUT	DWG. NO.
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE

IMPEDANCE OR ADMITTANCE COORDINATES

f = 300-1300 MHz

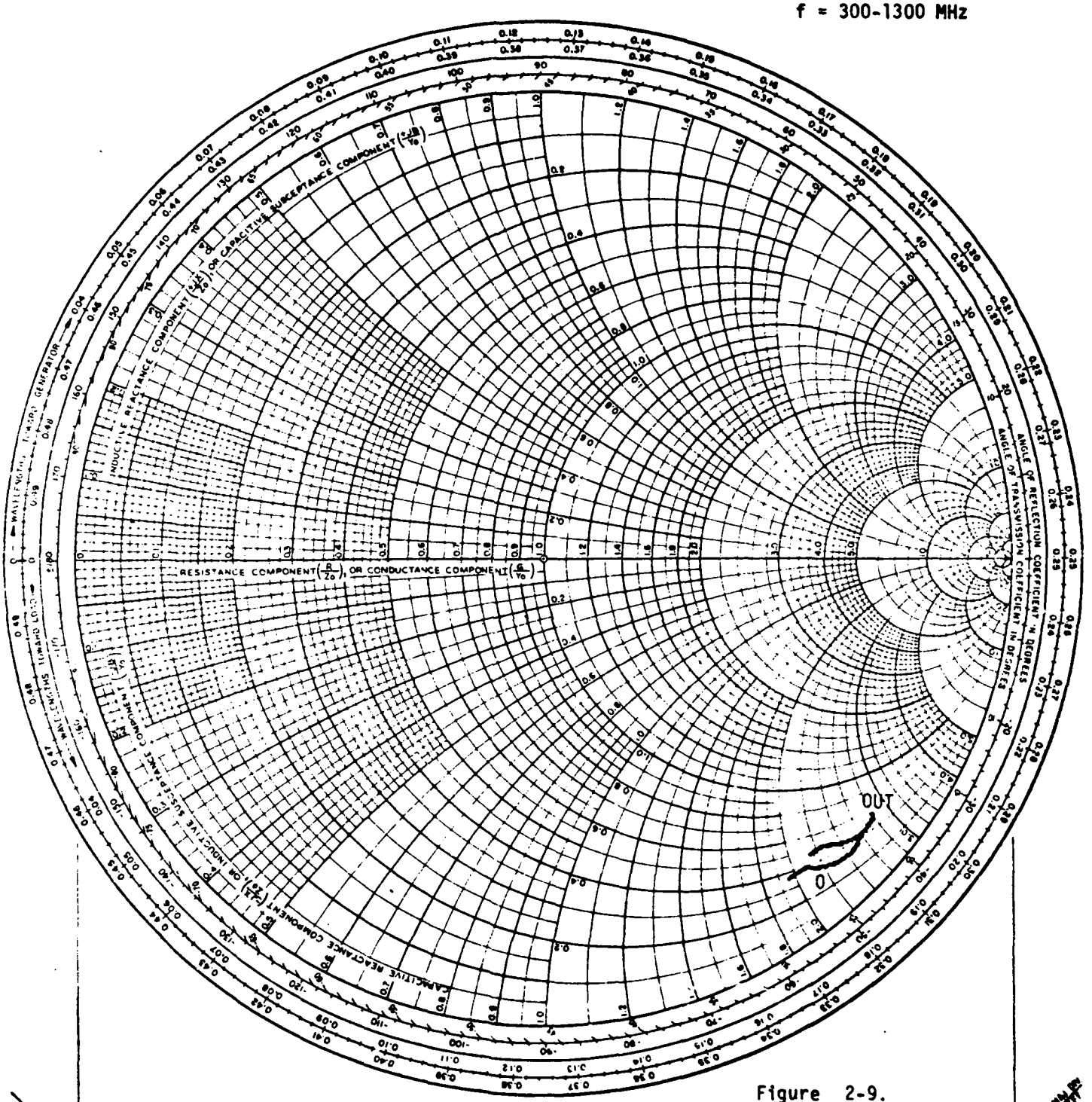
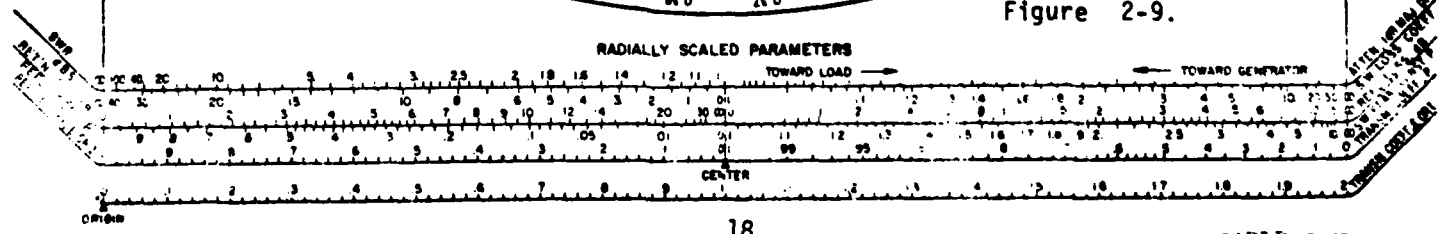


Figure 2-9.



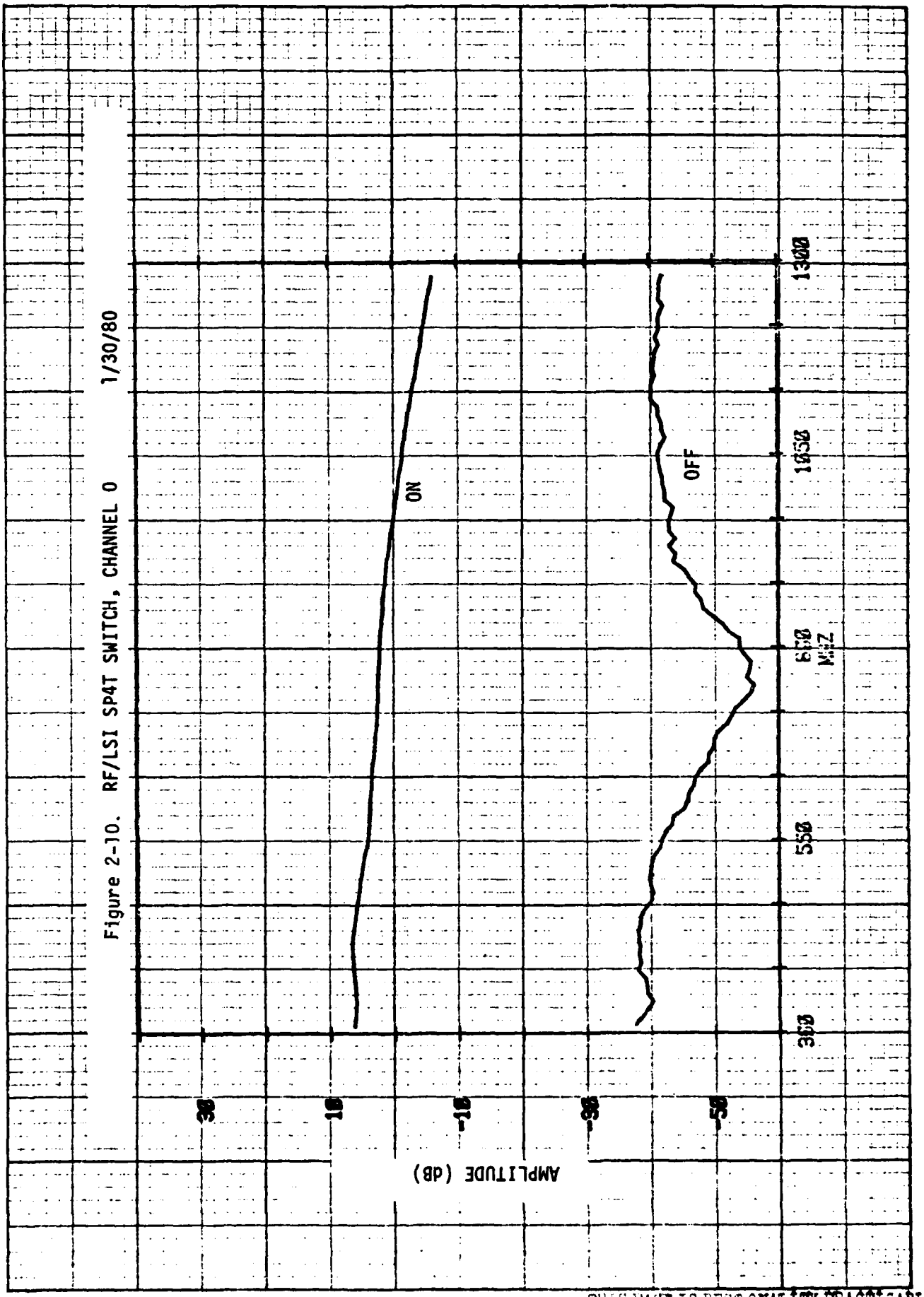


Figure 2-10. RF/LSI SP4T SWITCH, CHANNEL 0

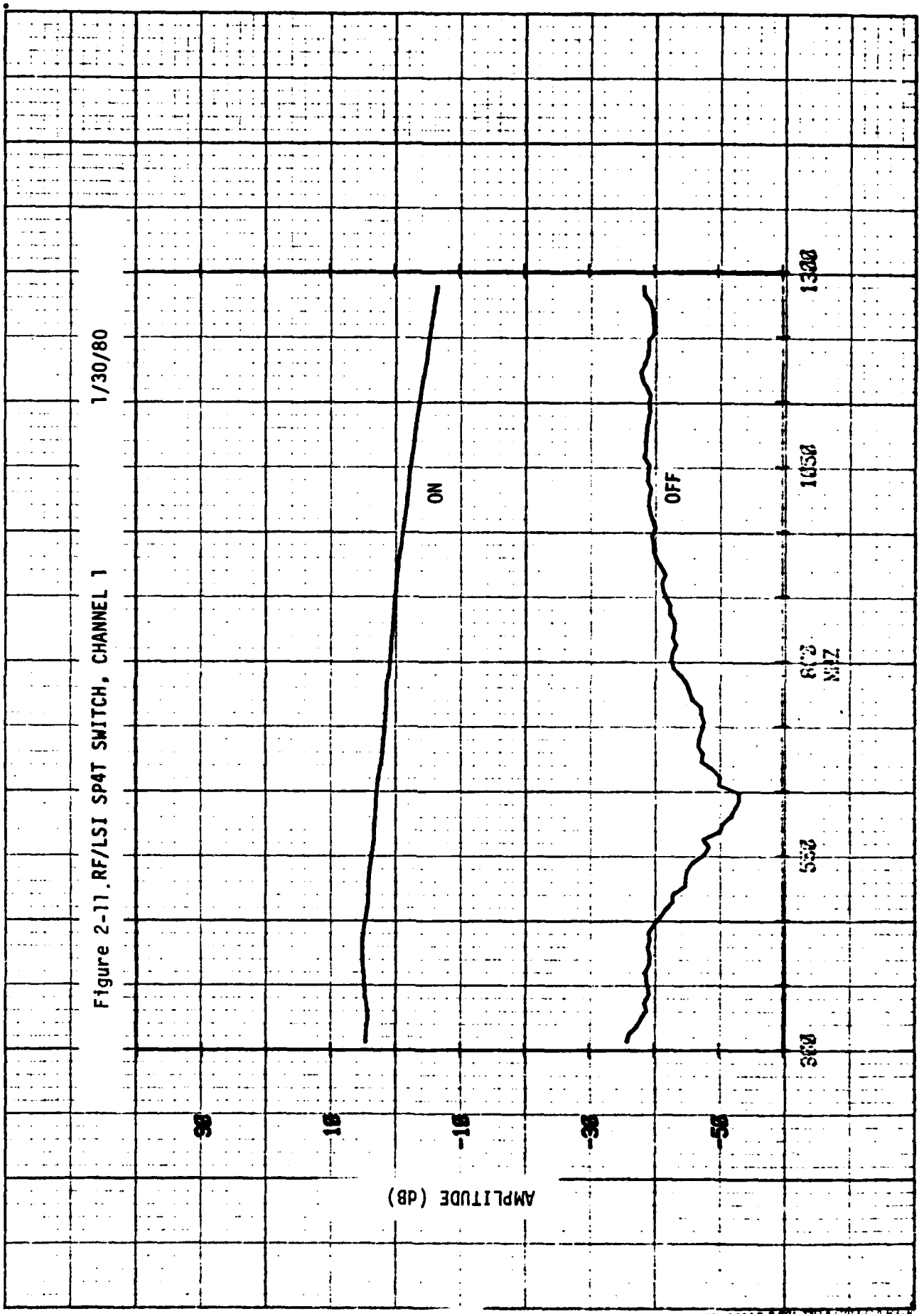


Figure 2-11. RF/LSI SP4T SWITCH, CHANNEL 1

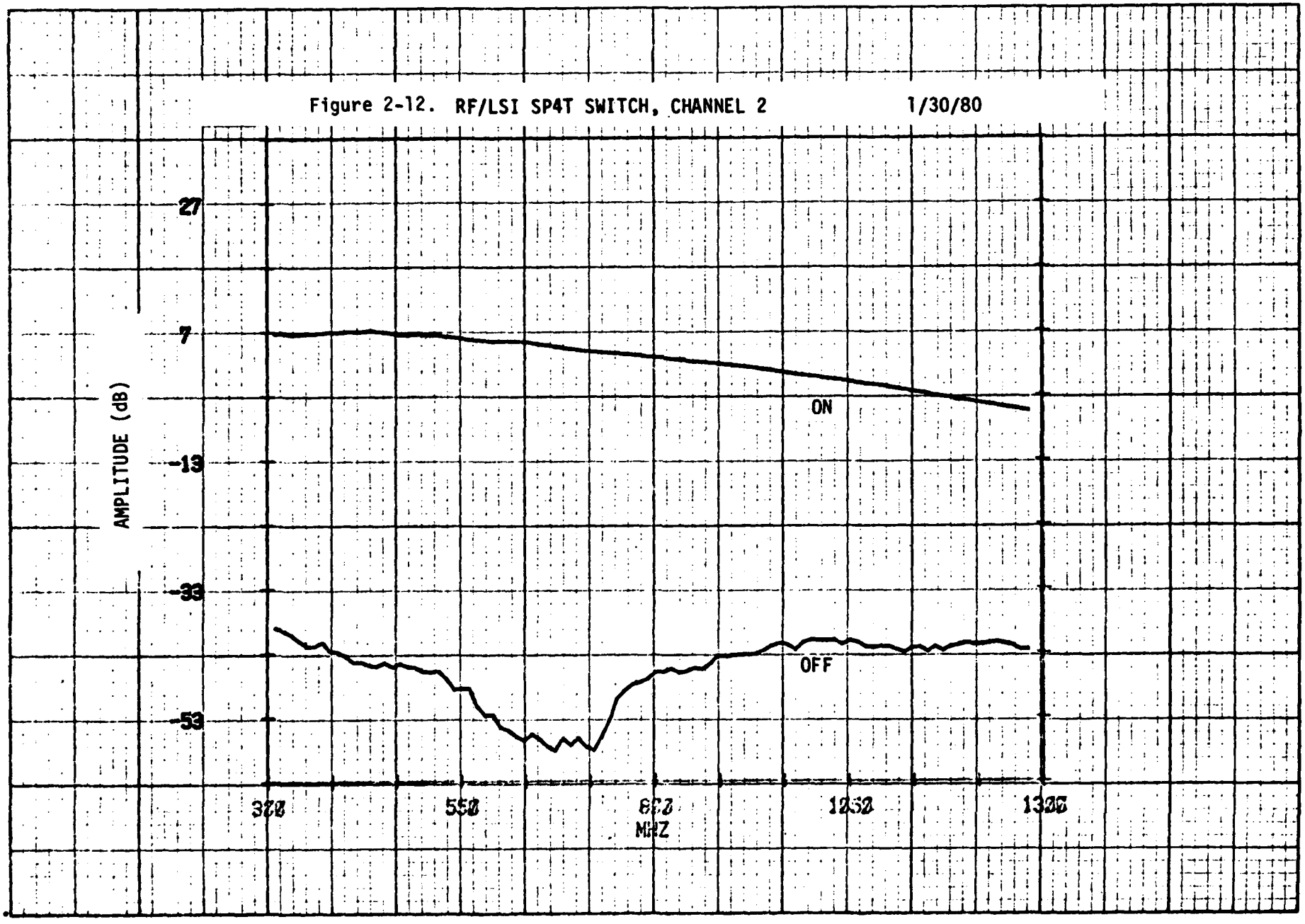
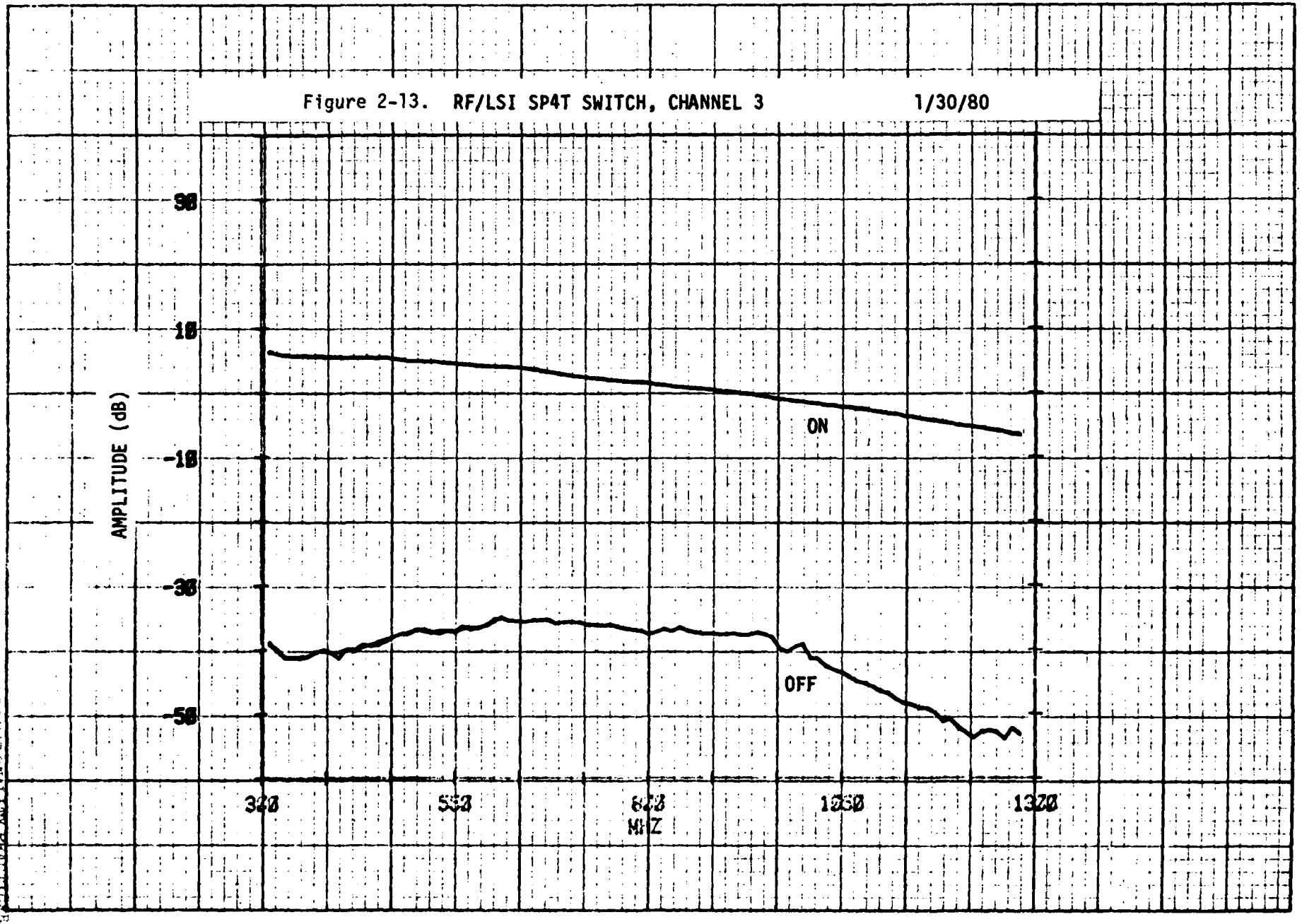
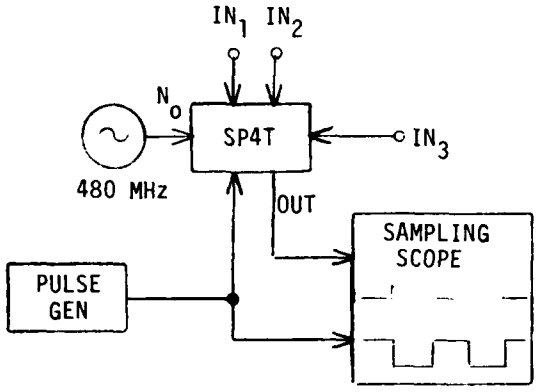
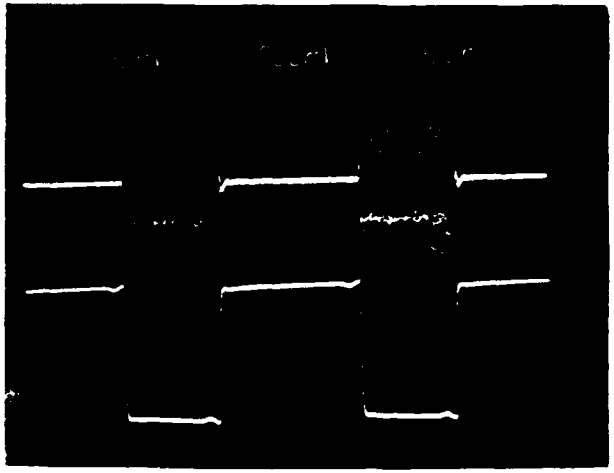
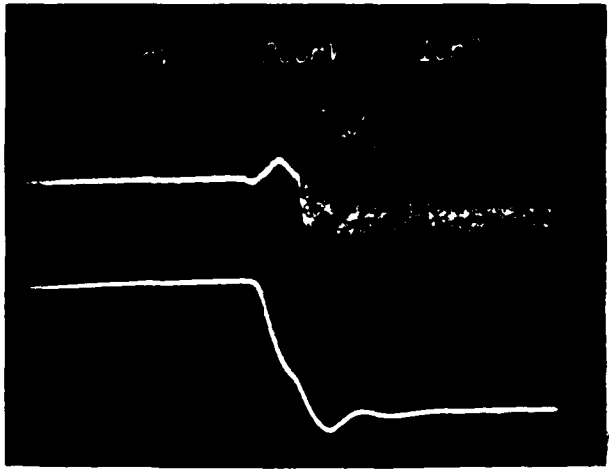


Figure 2-12. RF/LSI SP4T SWITCH, CHANNEL 2 1/30/80
AMPLITUDE (dB)
27
7
-13
-33
-53
ON
OFF
MHZ









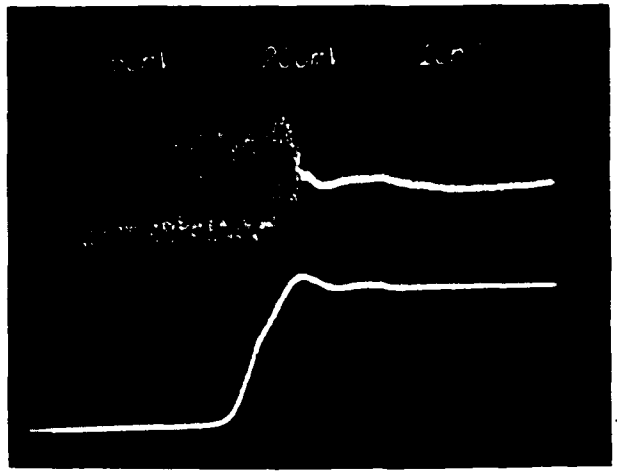


Figure 2-14. RF/LSI SP4T SWITCH, SWITCHING SPEED

Isolation of the switch is far below the expected 70 dB. Measured isolation is typically 40 dB. Since this is far below the computer-predicted performance, tests have been run to evaluate the package isolation, which was found to be only 40 to 45 dB. A new switch package has since been designed and is being fabricated. The new packaging approach consists of the RF/LSI chip mounted on a coplanar waveguide (CPW) substrate. The substrate in turn is mounted in a hybrid package. Tests have been run on the isolation provided by this approach. Isolation in excess of 60 dB is assured. CPW is an ideal medium for launching onto differential RF/LSI circuitry. This transmission medium provides both a signal path and ground path at the chip interface and thereby enhances common mode rejection. Figure 2-15 shows a sketch of a CPW, basically a narrow strip with two ground planes running adjacent and parallel to the strip on the same side of a substrate. Classically, CPWs are characterized by their characteristic impedance and phase velocity calculated by assuming that the dielectric substrate is thick enough to be considered infinite.[1] However, in the current application, a ground plane is used not only adjacent to the conductor but on the other side of the relatively thin dielectric substrate. The analysis to calculate this perturbation has been developed at TRW[2] and is based on a finite difference method with a network elimination technique. Figure 2-16 shows the change in characteristic impedance for the particular geometry described in the figure as the ground plane (L_1) distance is moved closer to the dielectric. Very good agreement has been obtained between measurement and the calculations. By using this packaging concept, total isolation through the switch of more than 70 dB is expected.

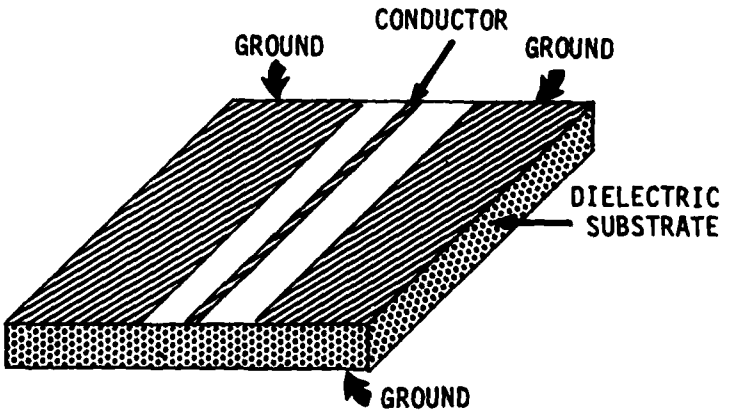


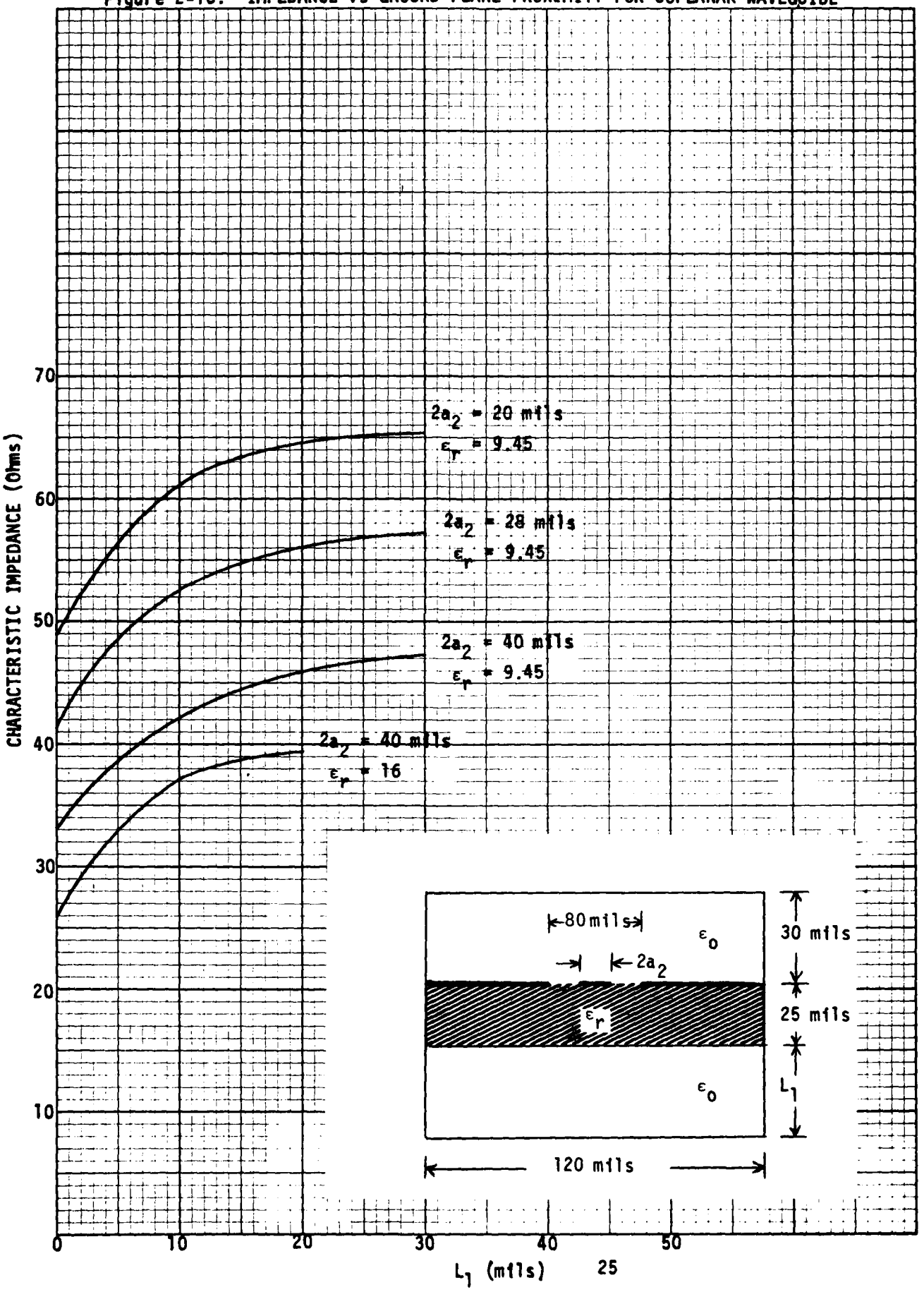
Figure 2-15.

COPLANAR WAVEGUIDE WITH GROUND PLANE

[1] C. P. Wen, "Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications", Vol. MTT-17, pp. 1087-1090, December, 1969.

[2] C. L. Chao, "Computation of Coplanar Waveguides", TRW IOC 76-7327-S-14, June, 1976.

Figure 2-16. IMPEDANCE vs GROUND PLANE PROXIMITY FOR COPLANAR WAVEGUIDE



(2) Mix-and-Divide Chip

The first of the mix-and-divide RF/LSI chips (ADM-1) have been fabricated and tests have just begun. In general, the chip does functionally perform, dividing the reference and mixing with the RF to produce an IF. Table 2-3 shows the preliminary data on the first chip measured (serial number 002). It was discovered that this chip only operates in the ÷3 mode. The spurious levels are higher than expected, but the data is too preliminary for any conclusions. The second chip (serial number 001), is just undergoing tests and does work in both the ÷3 and ÷4 configurations.

c. Output Module

The design of the Output Module is completed and a breadboard similar to the design has been fabricated and characterized. A schematic of the circuit is shown in Figure 2-17. The circuit is used to frequency double and amplify its imput to produce a 1296 to 1536 MHz synthesizer output at a saturated power of +10.3 dBm. Operation of the circuit can be followed through Figure 2-18, which details gain and power distribution for the module. The input amplifier chain is used to amplify the Synthesizer Module output to approximately +13 dBm at the doubler input. The doubler doubles the input frequency with a conversion loss of approximately 12 dB. The amplifier/filter chain following the doubler amplifies the doubler output to a saturated level of approximately +10 dBm and filters out-of-band spurs. Packaged thin film amplifier modules are used to provide the desired gain. Pads shown throughout the module are used to eliminate mismatches between circuits and thereby assure circuit stability. As Figure 2-18 indicates, an input drive level of -22 dBm (minimum Synthesizer Module output power) produces a saturated +10.3 dBm output. Total noise power at the output will be less than -40 dBm.

(1) Frequency Doubler

To minimize cost, complexity, and to improve temperature performance, a passive diode doubler design was chosen. A schematic for the circuit is shown in Figure 2-19. In this design the diodes are driven from RF signals with 180° relative phase. Each of the diodes conducts for half a cycle resulting in full wave rectification. The output waveform is therefore rich in second-order harmonics. The 180° relative phase is provided by driving one diode from the center pin of TL_7 while driving the other from the jacket. Both transmission

I) CONVERSION GAIN/SATURATED POWER: +3 OPERATION P_{LO} = -15 dBm

Case 1: $F_{LO} = F_{RF}$ = 480 MHz

P_{IN} (RF) (dBm)	P_{OUT} (IF) (dBm)	Gain (dB)
-22.0	-17.0	+5.0
-20.0	-15.0	+5.0
-18.0	-13.5	+4.5
-16.0	-12.3	+3.7
-14.0	-11.5	+2.5
-12.0	-11.0	+1.0
-10.0	-10.3	-0.3

F_{IF} = 640 MHz

Case 2: F_{LO} = 480 MHz
F_{RF} = 576 MHz

P_{IN} (RF) (dBm)	P_{OUT} (IF) (dBm)	Gain (dB)
-22.0	-17.7	+4.3
-20.0	-16.0	+4.0
-18.0	-14.45	+3.55
-16.0	-13.20	+2.8
-14.0	-12.30	+1.7
-12.0	-11.80	+0.2
-10.0	-11.40	-1.4

F_{IF} = 736 MHz

II) SPURIOUS SIGNAL LEVELS: +3 OPERATION

Case 1: $F_{LO} = F_{RF}$ = 480 MHz

P_{IN} (LO)	P_{IN} (RF)	Spur
-20 dBm	-20 dBm	~159.5 MHz, -40 dBm
		318.9 MHz, -20.2 dBm
		479.3 MHz, -20.3 dBm
		799.1 MHz, -39.4 dBm
		959.3 MHz, -36.2 dBm
		1119.3 MHz, -43.8 dBm
		1279.1 MHz, -43.7 dBm
		1439.5 MHz, -47.7 dBm

F_{IF} = 640 MHz at -15.9 dBm

Case 2: F_{LO} = 480 MHz
F_{RF} = 576 MHz

P_{IN} (LO)	P_{IN} (RF)	Spur
-15 dBm	-20 dBm	~160.0 MHz, -55.2 dBm
		256.2 MHz, -57.7 dBm
		319.8 MHz, -50.2 dBm
		415.7 MHz, -28 dBm
		479.7 MHz, -48.2 dBm
		575.7 MHz, -26.4 dBm
		639.7 MHz, -49.9 dBm
		800.2 MHz, -55.2 dBm
		895.5 MHz, -49.7 dBm
		959.6 MHz, -46.7 dBm
		991.7 MHz, -57.8 dBm
		1152 MHz, -59.4 dBm

F_{IF} = 736 MHz at -16.20 dBm

III) DC POWER CONSUMPTION: +3 Mode

+5.0 VDC	I(s) = 96.4 mA	P_{IN} = 1.101W Total
-5.0 VDC	I(s) = 71.3 mA	
+10.0 VDC	I(s) = 26.2 mA	

IV. VSWR (MEASURED IN 50 OHM SYSTEM WITH ALTERNATE PORTS TERMINATED IN 50 OHMS).

PIN 2	$\Gamma_{LO\ PORT}$ = 0.07	VSWR = 1.15:1
PIN 6	$\Gamma_{RF\ PORT}$ = 0.84	VSWR = 11.5:1
PIN 12	$\Gamma_{IF\ PORT}$ = 0.25	VSWR = 1.7:1

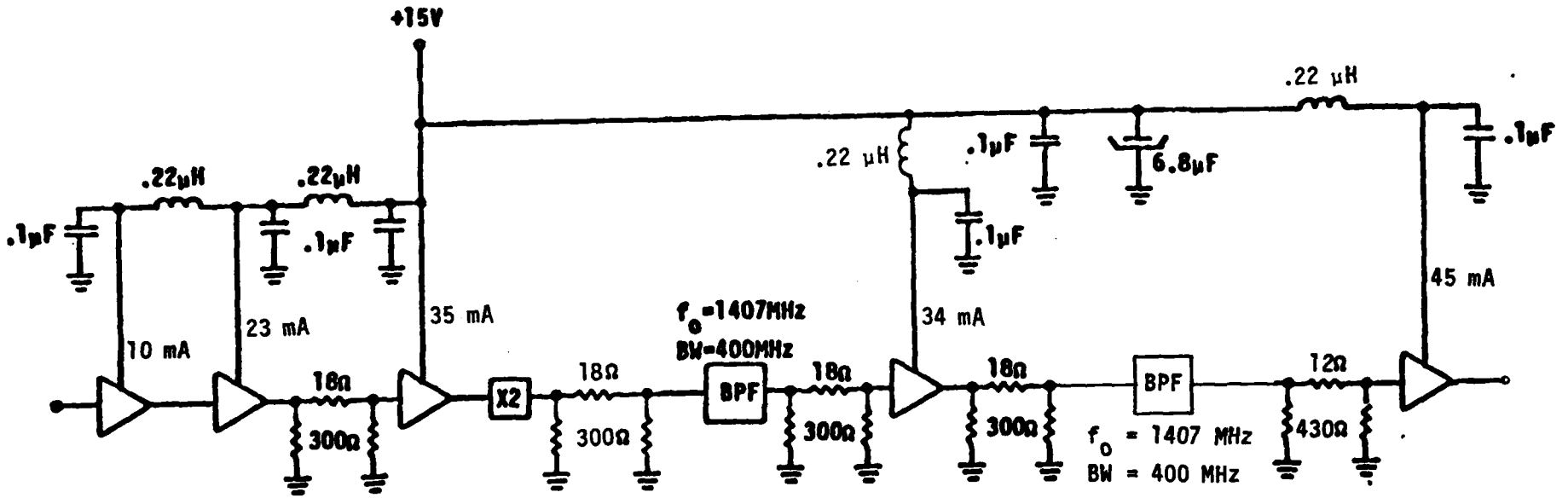
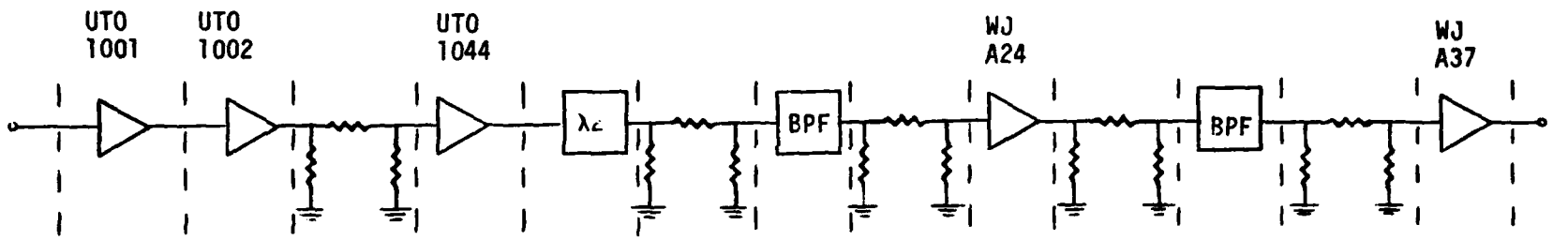


Figure 2-17. OUTPUT MODULE

Figure 2-18.
OUTPUT MODULE GAIN/POWER DISTRIBUTION



GAIN (dB)	+14	+14	-3	+10	-12	-3	-2	-3	+20	-3	-2	-2	+9.3			
P_{SAT} (dBm)	-2	+7		+13					+8				+15.5			
BW (MHz)	1000	1000		1000			400		1500		400		2000			
P_{SIG} (dBm)	-22	-8	+6	+3	+13	+1	-2	-4	-7	+8	+5	+3	+1	+10.3		
NOISE FIGURE (dB)	5.185															
P_{NOISE} (dBm)	-78.8	-64.8	-50.8	-53.8	-43.8	-49.8*	-52.8	-58.8	-61.8	-46.8	-49.8	-51.8	-53.8	-44.5		

*Reflects 12 dB conversion loss and 6 dB noise enhancement.

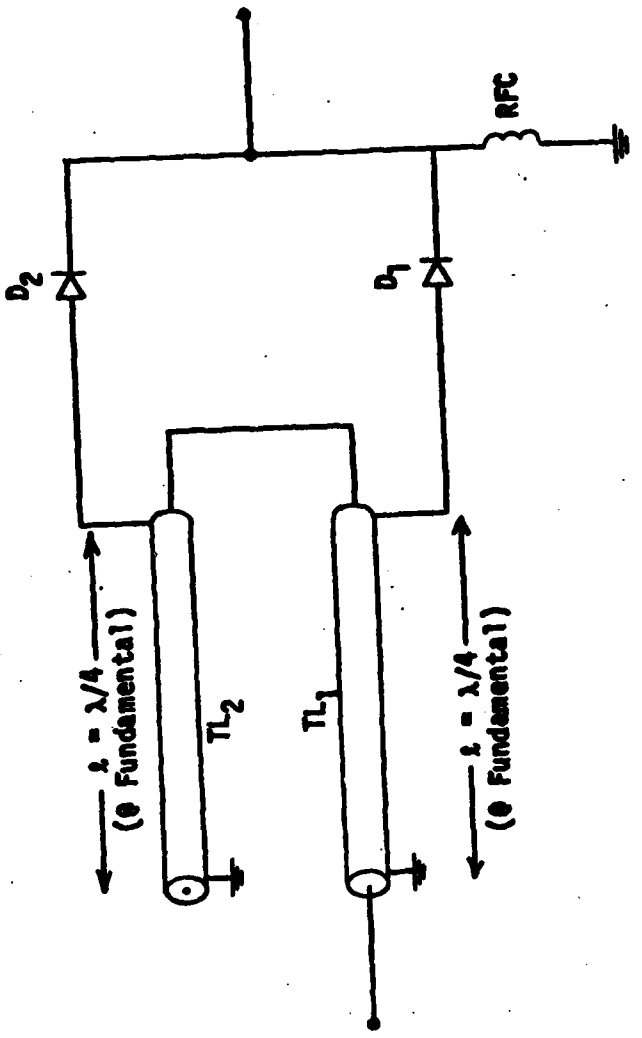


Figure 2-19. FREQUENCY DOUBLER DESIGN

lines also serve as idlers for even-order harmonics and serve to suppress odd-order harmonics. As idlers, the transmission lines provide low impedance paths at odd-order harmonics.

The performance of the doubler is shown in Figures 2-20 and 2-21 and summarized in Table 2-4. The results indicate worst case spur level as -9 dBc for the third-order harmonic. The design has not been optimized for spur rejection to harmonically related spurs. (Unmatched diodes, an unbalanced power split, and improper phase at the diode inputs all contribute to the presence of harmonically related spurs at the output.) The spur performance for the non-optimized design is more than adequate in this circuit application.

Figure 2-20. FREQUENCY DOUBLER - POWER OUT vs POWER IN

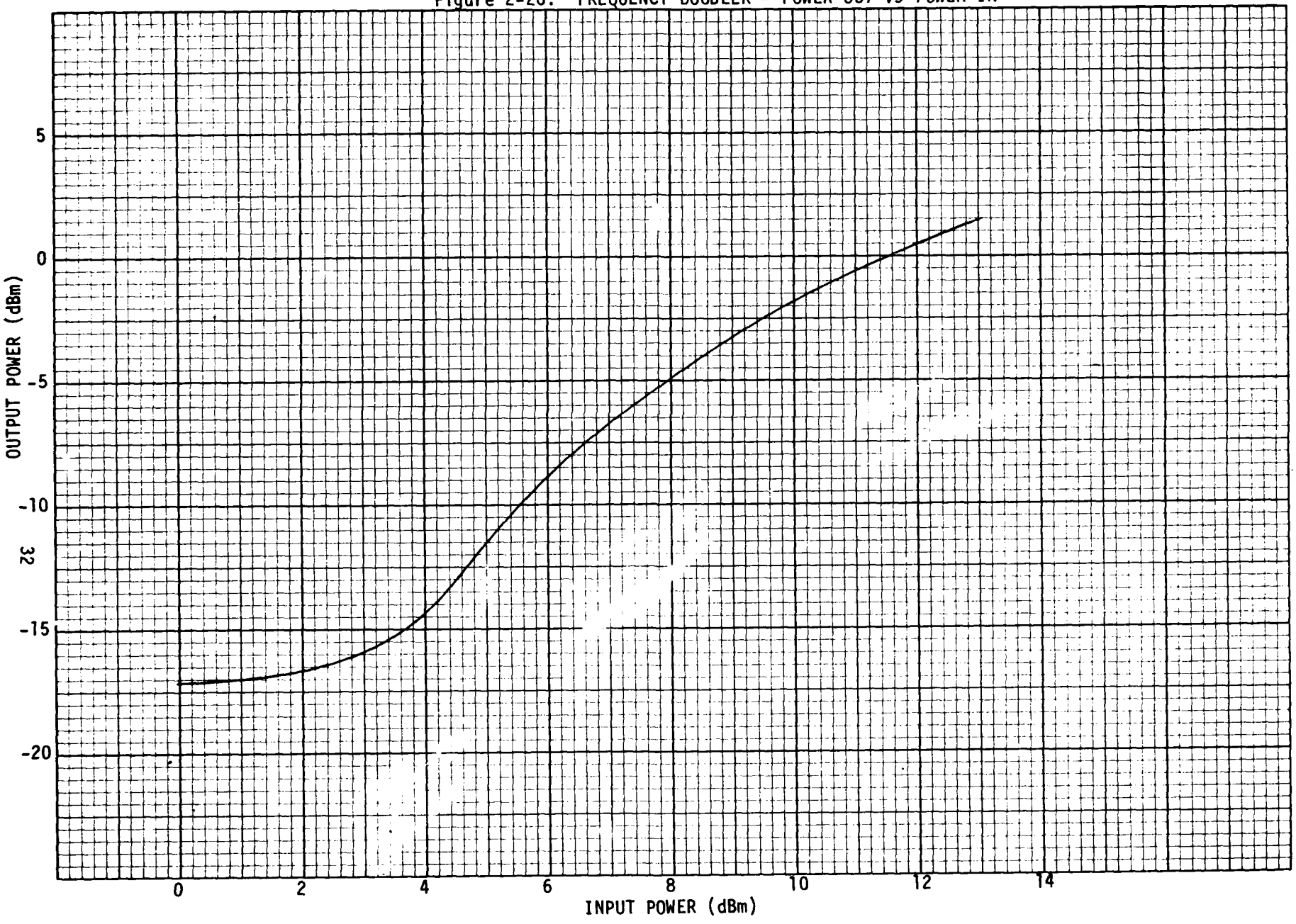


Figure 2-21. FREQUENCY DOUBLER - OUTPUT vs FREQUENCY

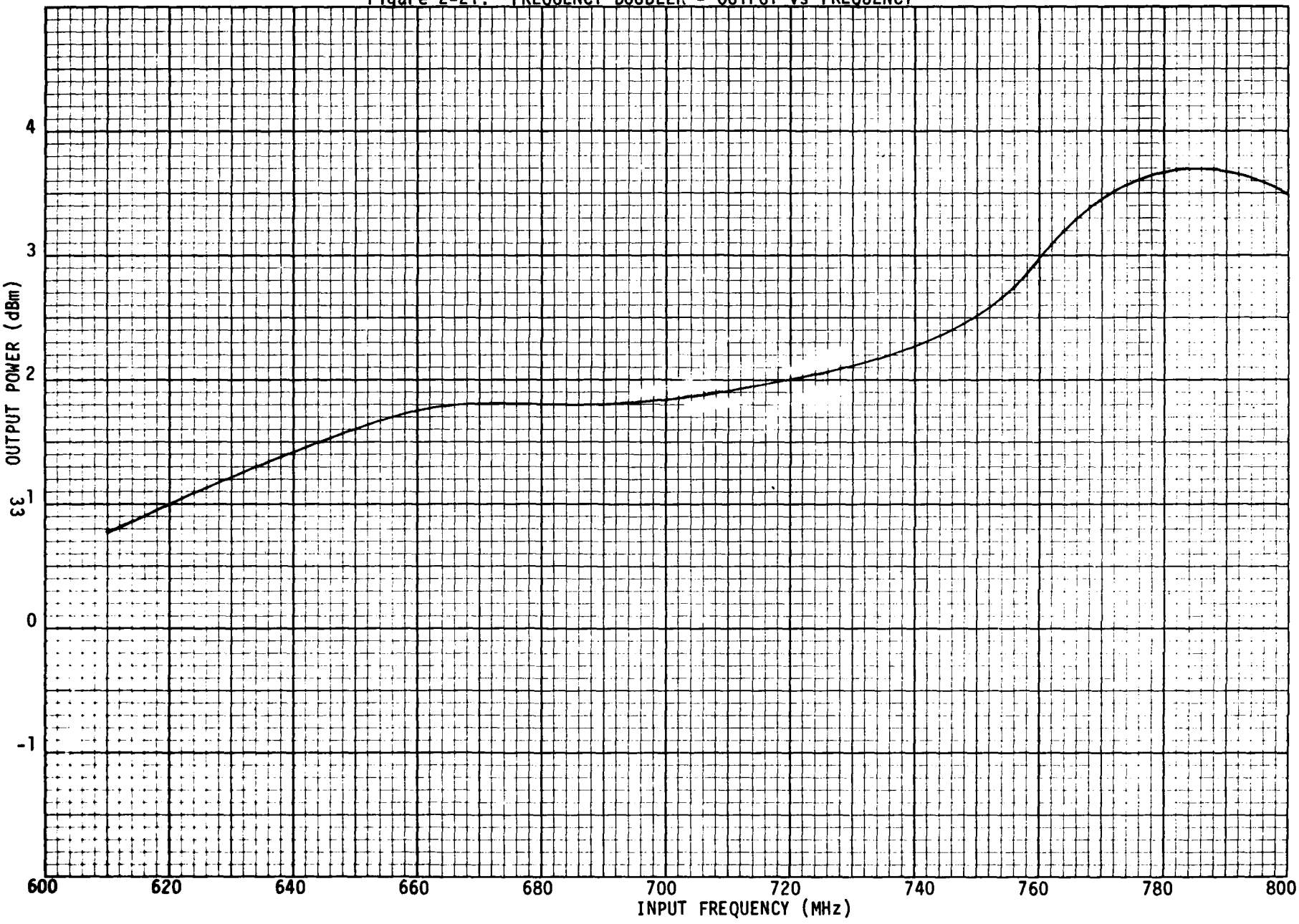


Table 2-4. FREQUENCY DOUBLER REQUIREMENTS VS CAPABILITIES SUMMARY

ITEM NO.	PARAMETER DESCRIPTION	REQUIRED PERFORMANCE	CAPABILITY	COMMENTS
1	Input Frequency	648 -768 MHz	600-800 MHz	
2	Input Drive Level	$\leq$ +15 dBm	+13 dBm typ.	
3	Conversion Loss	<15 dB	11.5 dB typ.	
4	Harmonic Rejection			
	f_1 (Fundamental)	>0 dBc	$\geq$ -11 dBc	Filters follow the doubler to reduce out-of-band spurs.
	f_2 (Times 3)	>0 dBc	$\geq$ -9 dBc	

Figure 2-22. P_{OUT} vs P_{IN} AT 704 MHz - BREADBOARD OUTPUT MODULE

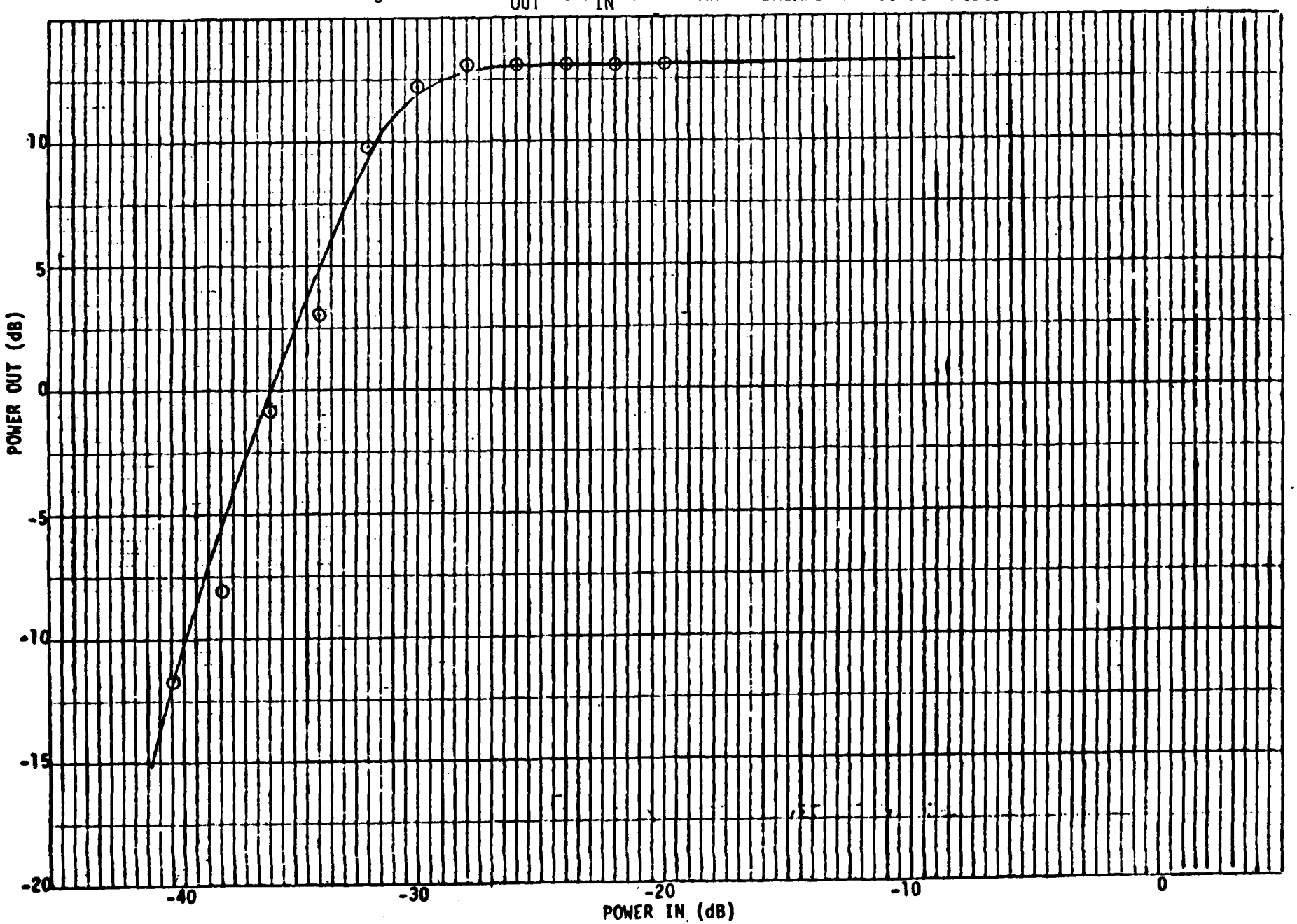


Figure 2-23. P_{OUT} vs FREQUENCY - BREADBOARD OUTPUT MODULE

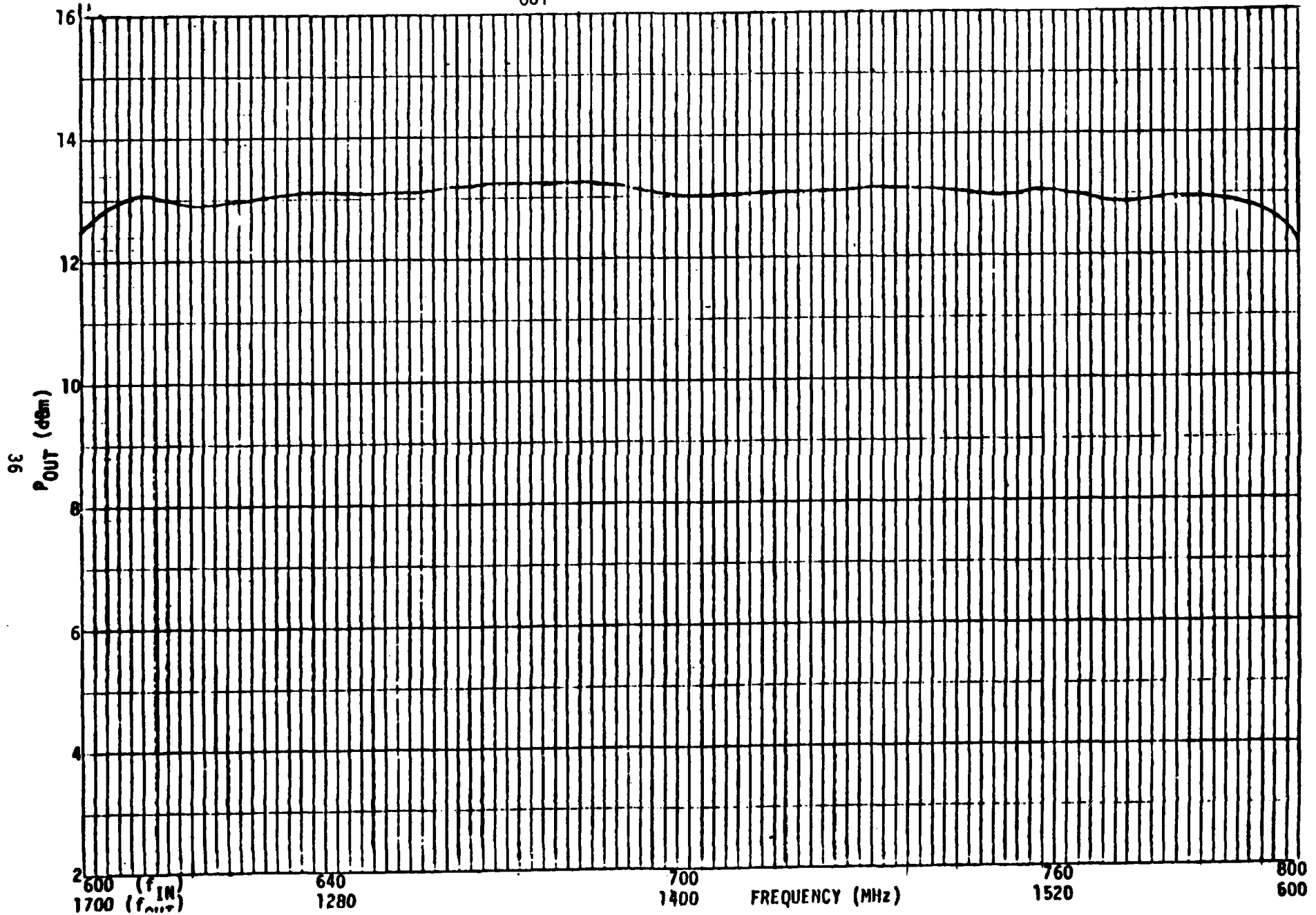


Table 2-5. FREQUENCY SYNTHESIZER OUTPUT MODULE SPECIFICATIONS (+25°C AMB)

ITEM NO.	PARAMETER DESCRIPTION	REQUIRED PERFORMANCE	CAPABILITY	COMMENTS
1	DC Power	Minimum	2.2W	Calculated Power (Breadboard measurement was 3.8 watts).
2	P_{IN} (648 to 768 MHz)	$\geq$ -22 dBm	$\geq$ -26 dBm	Breadboard measurement.
3	P_{OUT} (648 to 768 MHz)	+10.0 $\pm$1.0 dBm	+10.3 $\pm$0.2 dBm	Calculated Value (Breadboard measurement was +13 $\pm$0.2 dBm)
4	Frequency Response			
	-1 dB_L Bandwidth	1296 MHz	1200 MHz	Breadboard measurement.
	-1 dB_H Bandwidth	1536 MHz	1600 MHz	Breadboard measurement.
5	VSWR	$\leq$2.0:1	$\leq$1.9:1	Breadboard measurement.
6	Spurious Response	>-70 dBc	>-65 dBc	Breadboard measurement.

3. CONCLUSIONS AND PROJECTED PLANS

The microwave oscillator portion of this contract has been completed and two units delivered. The two units clearly demonstrated the feasibility of using SAW filters to stabilize the 1680 MHz sources while providing both frequency and amplitude modulation at a half watt output power.

Design of the synthesizer is well under way. Three functional modules are used as the building blocks for the synthesizer. The Tone Generation Module has been conceptualized, a theory for injection locking properties of SAW oscillators formulated and proven by test, and the required SAW filters in the process of mask fabrication. The RF/LSI Synthesizer Modules consisting of the SP3T (SP4T) switch and mix-and-divide (ADM) chips have been fabricated and are in the process of being tested. Preliminary results have been given. The Output Module has been designed; the key component, a frequency doubler circuit, has been fabricated and tested and a paper design of the amplifier stage completed and compared against tests on a similar, though non-optimized, breadboard.

During the next reporting period the synthesizer will be completed. Tasks required as part of this effort include the design, fabrication, and test of a comb generator; processing of SAW delay lines and filters; the design, fabrication, and test of four injection-locked SAW oscillators; the design, fabrication, and test of the Synthesizer Module; and the design, fabrication, and test of the Output Module.

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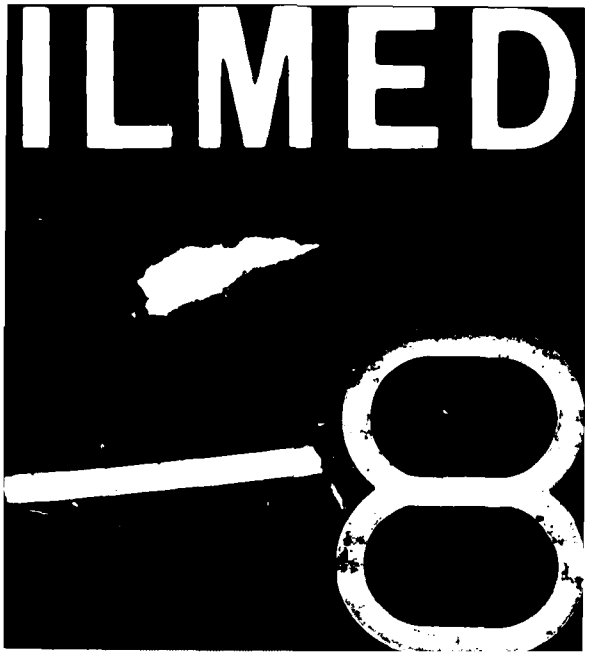
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8