

AD-A086 345

AUBURN UNIV ALA DEPT OF PHYSICS

F/6 9/1

SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)

MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAA629-78-G-0111

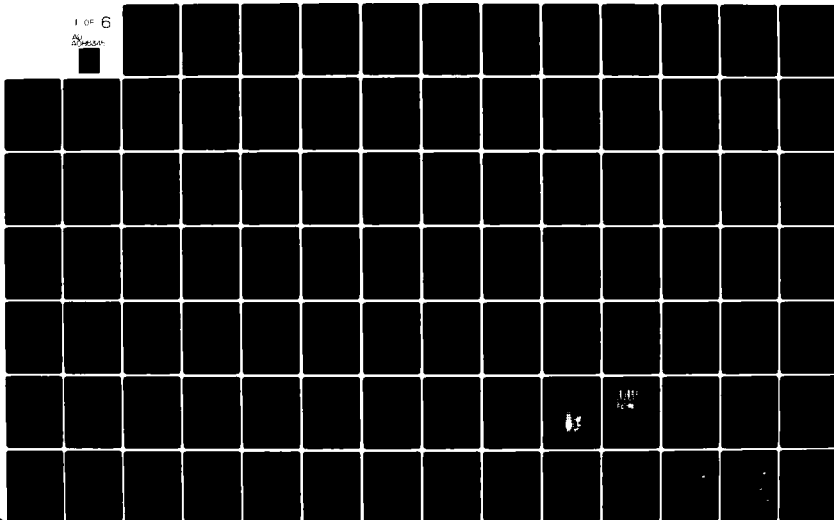
ARO-15840.3-A-EL

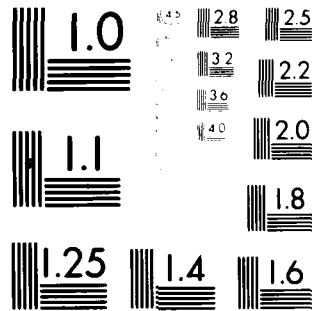
NL

UNCLASSIFIED

1 OF 6

AD-A086 345





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

ADA 086345

1000

ARO 15840.3-A-EL

8 (12)

Second Breakdown Susceptibility of Silicon-On-Sapphire Diodes Having Systematically Different Geometries

Paul P. Budenstein, Aradhana Baruah,
Edward R. Knight, and Fu-Tai Liou

May 30, 1980

U. S. Army Research Office

Grant Nos. DAAG29-77-0189 and DAAG29-78-G-0111

Auburn University

DTIC
ELECTRONIC
JUN 30 1980
A

Approved For Public Release:
Distribution Unlimited.

DDC FILE COPY

80 6 30 174

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
	AD A086345	(9)
4. TITLE (and Subtitle)	5. TYPE OF REPORT & PERIOD COVERED	
6 SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES HAVING SYSTEMATICALLY DIFFERENT GEOMETRIES.	FINAL REPORT, 1 June 1977-31 December 1979	
7. AUTHOR(s)	8. CONTRACT OR GRANT NUMBER(s)	
10 Paul P./Budenstein, Aradhana/Baruah, Edward R./Knight, Fu-Tai/Liou	DAAG29-77-G-0189 DAAG29-78-G-0111 DAAG29-77-G-0189	
9. PERFORMING ORGANIZATION NAME AND ADDRESS	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS	
Physics Department Auburn University Auburn, AL 36849	(16) Defense Nuclear Agency Subtask/Z99QAXT Work Unit 2	
11. CONTROLLING OFFICE NAME AND ADDRESS	12. REPORT DATE	13. NUMBER OF PAGES
U.S. Army Research Office Post Office Box 12211 Research Triangle Park, NC 27709	(11) 30 May 1980	523
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report)	
U.S. Army Missile Research and Development Command Redstone Arsenal, AL 35809	Unclassified	
16. DISTRIBUTION STATEMENT (of this Report)	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
(18) ARO (19) 15840.3-A-EL		
18. SUPPLEMENTARY NOTES		
The findings in this report are not to be construed as an official Department of the Army position, unless so designated by other authorized documents.		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
Second breakdown Non-destructive screening Electrothermal model Geometric defects Current filamentation Silicon-on-sapphire diodes		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)		
Experiments were performed on thin film silicon-on-sapphire (SOS) diodes ($p^+ - n - n^+$) to determine the roles of geometry and doping level (10^{15} to 10^{17} atoms/cm ³) on current configurations, second breakdown susceptibility, and damage morphology. Geometric parameters varied including diode width, n-region length, n-region doping density, diffusion spikes of different sizes, and configurations on the n^+n or p^+n interfaces, contact spikes at the n^+ -metal and p^+ -metal interfaces, and a variety of other current concentration geometries.		

DD

FORM 1 JAN 73

1473

EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

405564

Block 20 Abstract continued

Prior to the present study, the effectiveness of junction defects in reducing resistance to second breakdown was not known. However, it was suspected that such defects might result in "maverick" devices, that is, devices which fail much below their rated electrical parameters.

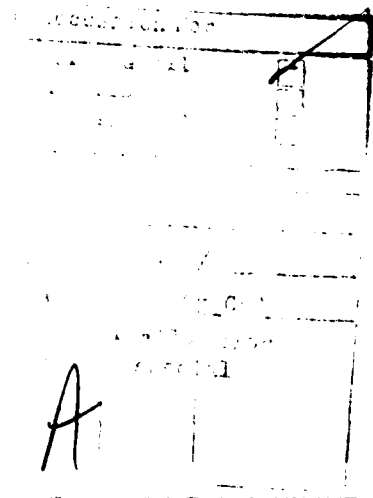
SOS diodes, specially fabricated by Rockwell International, were tested using Sunshine's stroboscopic technique. This method exploits the decrease of the optical transmittancy of silicon with increasing temperature. The dynamic growth of current filaments can be followed in many systems with a time resolution of 0.1 μ s for pulses of 10 μ s duration and spatial resolution of 1 μ m. Most tests were performed using 10 μ s pulses which were obtained from constant current or constant impedance generators. The experimental results show that those irregularities that decrease the length of the n-region cause early growth of filaments and a lowering of the energy threshold to second breakdown. However, defects on the metal-p⁺ and metal-n⁺ junctions have no effect on current configurations. Energy, current, and voltage thresholds were correlated with n-region length, diode width, defect geometry, and doping level. Spikes on the p⁺n and n⁺n junctions lowered energy failure thresholds up to 75% for non-punchthrough diodes and more for diodes in which punchthrough of the n-region occurred. Spikes on the metal-p⁺ and metal-n⁺ junctions had no effect on failure thresholds. The stroboscopic method was not effective for the lower doping levels, but examination of the damage morphology indicated that junction defects, corners, and radii of curvature influence current configurations over a doping density range of 10¹⁵-10¹⁷ cm⁻³. Suggestions are given on test procedures for screening devices to meet preset standards of hardness to second breakdown.

An electrothermal model of the filamentation process in thin film (planar) diodes has been formulated. The model includes junction and bulk electrical behavior, thermal properties of silicon and the sapphire substrate, heat transfer in the plane of the silicon and into the substrate, and external circuit constraints. Dynamical temperature and current profiles, voltage and current waveforms, delay time and energy to the threshold of destructive second breakdown, and other detailed information about the filamentation process are obtained. Calculations have been performed for diodes having an n-region doping density of 10²² atoms/m³, 30 μ m n-region length, and 204 μ m width. The filamentation process is followed to filament temperatures in excess of 1200 K. Then changes occur so rapidly that the computation time becomes excessive. Calculations were performed mostly assuming constant current pulses with durations of 2 to 15 μ s. The average current density at the threshold of second breakdown is about 10⁸ A/m², while the current density in the filament rises above 10⁹ A/m². The influence of spikes on the p⁺n or n⁺n junctions on the second breakdown thresholds have been explored. The results of the model are compared with the experimental results on diodes of similar geometry and the two are found to be consistent. Thus the model can provide useful insight to the designer and user of devices under high electrical stress.

Unclassified

TABLE OF CONTENTS

LIST OF TABLES	iv
LIST OF FIGURES	vi
ACKNOWLEDGEMENTS.....	xix
I. INTRODUCTION	1
II. BACKGROUND ON EXPERIMENTATION	4
- History of the Second Breakdown Problem - Second Breakdown in Bulk Devices - I-V Characteristics in Diodes and Transistors - Time Delay and Related Effects - Hot Spots and Current Channeling - Radiation and Second Breakdown - Damage - Second Breakdown in Silicon-On-Sapphire Diodes - Non-Destructive Screening, Failure - Thresholds, and Related Effects	
III. EXPERIMENTAL METHODS	32
- Stroboscopic Method - Circuit Considerations - Transient Digitizer, Waveform Analysis - Typical Test Sequence - Energy Threshold Measurements - Voltage Threshold Measurements and Damage Morphology - Waveform Surfaces - Device Characterization	
IV. DESCRIPTION OF SPECIMENS	53
- Fabrication Procedure - Device Structures - Standard Reference Structure - Enclosed Reference Structure - Contact Spike to p^+ Region Structure - Contact Spike to n^+ Region Structure - Diffusion Spike on p^+n Junction Structure - Diffusion Spike on n^+n Junction Structure - Half-Size Spike Structure - Four-Terminal Structure - Doping Level Test Structure	



- Interdigitated Structure
- Radius of Curvature Structure
- Processing Test Structure
- Rockwell Devices
- Multiple Spike Structure
- Labeling Scheme
- Device Characterization
- Resistivity Measurements
- Reverse Bias Breakdown Voltage Measurements
- Summary and Discussion

V. RESULTS 84

- Standard Reference Diodes
- Diffusion Spike Diodes (p^+n Junction)
- Diffusion Spike Diodes (n^+n Junction)
- Contact Spike Diodes
- Enclosed Reference Diodes
- Comparison of Standard Reference, Enclosed
- Reference, p^+n Spike, and n^+n Spike Diodes
- Energy Threshold Analysis
- Voltage Threshold Analysis
- Damage Morphology
- Multiple Spike Diodes
- Radius of Curvature Diodes
- Interdigitated Diodes
- Special Tests
- Waveform Surfaces
- Waveform Surface Analysis
- Light Emission
- Heating Patterns Under Forward Bias
- Four-Terminal Structure
- Delay Time
- Hot Spot on the n^+n Junction
- Temperature Measurements

VI. CONCLUSIONS 237

- Heating Patterns
- Energy, Current, and Voltage Thresholds
- Damage Morphology

VII. BACKGROUND 247

- Screening Tests
- Elimination of "Mavericks"
- Reliability Screening
- Design of Devices for Greater Resistance to Second Breakdown

VIII.	ELECTROTHERMAL MODEL FOR CURRENT FILAMENTATION	257
	Diode Configuration for Model	
	Equations of the Model	
	Discussion of Substrate Heat Flow Term	
	Computational Procedure	
IX.	PN JUNCTION J-V-T CHARACTERISTICS UNDER REVERSE BIAS AND HIGH CURRENT DENSITIES	280
	Equations for the Abrupt, Reverse Biased $p^+ - n$ Junction	
	Computational Strategy	
X.	CALCULATED JVT CHARACTERISTICS UNDER REVERSE BIAS	292
XI.	RESULTS OF ELECTROTHERMAL MODEL	320
	Uniform Junction Diodes	
	Current Distributions	
	Temperature profiles	
	Voltage waveforms	
	Time delay for onset of filamentation and for instability	
	Double step pulses	
	Diode with spikes on the p^+n junction	
	Current distributions	
	Temperature profiles	
	Voltage waveforms	
	Delay times	
	Role of film thickness	
	Diode with spikes on the n^+n junction	
	Program modifications	
	Uniform junction diode (modified program)	
	p^+n diffusion spike diode (modified program)	
	n^+n diffusion spike diode (modified program)	
XII.	COMPARISON OF THEORY AND EXPERIMENT	428
	Comparison of Theory and Experiment	
	Principal Features of the Electrothermal Model	
XIII.	IMPLICATIONS	441
	Screening Tests	
	Maverick Devices	
	Screening Methodology	
	Design of Devices for Greater Resistance to Second Breakdown	
	REFERENCES	445
	APPENDIX A. Junction JVT Characteristics Obtained by Baruah	452
	APPENDIX B. Listing of Computer Programs	473

LIST OF TABLES

1. Silicon-on-Sapphire Diode Geometries Used by Budenstein, Pontius, and Smith	23
2. Wafer Labeling Scheme	70
3. Estimations of the N-Region Doping Level	75
4. Numerical Values of the Pre-Failure and Failure Energies of Diodes on Wafers 2-5 and 2-4 with N-Region Widths of 200 μm	113
5. Numerical Values of the Pre-Failure and Failure Energies of Diodes on Wafer 2-4 with N-Region Widths of 30 μm , and of Diodes on Wafer 2-1 with N-Region Widths of 200 μm	116
6. Numerical Values of the Current and Current Density Failure Thresholds of Diodes on Wafers 2-5 and 2-4 with N-Region Widths of 200 μm	119
7. Numerical Values of the Current and Current Density Failure Thresholds of Diodes on Wafer 2-1 with N-Region Widths of 200 μm , and of Diodes on Wafer 2-4 with N-Region Widths of 30 μm	120
8. Voltage Failure Thresholds of Diodes with an N-Region Length of 10 μm	137
9. Voltage Failure Thresholds of Diodes with an N-Region Length of 30 μm	138
10. Voltages Failure Thresholds of Diodes with an N-Region Length of 100 μm	139
11. Voltage Failure Thresholds of Diodes with an N-Region Length of 300 μm , and Multiple Spike Diodes on Wafer 2-5	140
12. Voltage Failure Thresholds of Multiple Spike Diodes on Wafers 2-2, 1-3, and 2-4	141
13. Parameters from Eq. 9.9 in SI units	286

14. Parameters for Eqs. 9.10-9.13 in SI units	286
15. Parameters for Eq. 9.21	290
16. Temperature at which junction becomes resistive for different current densities	303
17. Conditions used in Figs. 105-115	316
18a. Summary of SOS diode simulations by Baruah	322
18b. Simulation parameters for uniform junction diodes	323
18c. Simulation parameters for p ⁺ n spike diodes	323
19. Reference levels for delay times	358
20. Comparison with theory with data from diodes of Wafer 2-4	432
21. Summary of simulation runs with various functional forms of carrier velocity of ionization coefficients	454
22. Results of simulation runs with various functional forms of carrier velocities and ionization coefficients	456
23. Role of doping density of the n region on junction characteristics (T = 300 K, J = 1 × 10 ⁸ A/m ²)	460

LIST OF FIGURES

1. I-V Characteristics Showing Second Breakdown	7
2. Block Diagram of the Apparatus Used for Studying Silicon-on-Sapphire Diodes	33
3. A Silicon-on-Sapphire Diode in Position for Observation of Second Breakdown Phenomena	35
4. Constant Current Circuit	39
5. Constant Current Circuit Using Beam Power Tetrode	42
6. Constant Current Circuit	49
7. Fabrication Procedure	54
8. Wafer and Die Layout	56
9. Die and Individual Device Identification	57
10. Die Layout	58
11. Standard Reference Structure	59
12. Enclosed Reference Structure	61
13. Spike Construction Detail	62
14. Four Terminal Structure	64
15. Doping Level Test Structure	66
16. Interdigitated Structure	67
17. Radius of Curvature Structure	68
18. Impedance of the Doping Level Test Structure Versus Position on the Surface of Wafer 2-2	72
19. Impedance Measurements on Wafers 2-1, 1-3, and 2-4	73
20. Reverse Bias Breakdown Voltage Versus Diffusion Spike Length	77

21. Impedance Versus Length-to-Width Ratio for Forward Biased Standard Reference Diodes from a Single Die on Wafer 2-1	81
22. Breakdown Voltages of a Particular Type Diode on Wafer 2-2	83
23. Reverse Bias Test of a Standard Reference Diode on Wafer 2-5	86
24. Reverse Bias Test of a Standard Reference Diode on Wafer 2-5	88
25. Resistivity as a Function of Temperature for N-Type Silicon	89
26. Junction Voltage Versus Temperature for Different Current Densities Calculated for the Doping Density of 10^{16} cm^{-3}	90
27. Second Breakdown in the Diode in Figs. 23 and 24	94
28. Reverse Bias Tests of Five Different Standard Reference Diodes on Wafer 2-5	96
29. Reverse Bias Tests of Three Standard Reference Diodes on Wafer 2-5	100
30. Reverse Bias Tests of Three p^+n Spike Diodes on Wafer 2-5	103
31. Reverse Bias Tests of Three N^+N Spike Diodes on Wafer 2-5	105
32. Reverse Bias Tests of Two Enclosed Reference Diodes on Wafer 2-5	108
33. Total Energy Input at the Second Breakdown Threshold	112
34. Total Energy Input at the Second Breakdown Threshold Versus N-Region Length for Standard Reference and Diffusion Spike Diodes on Wafer 2-5	113
35. Current Amplitude at the Second Breakdown Threshold Versus N-Region Length for Standard Reference and Diffusion Spike Diodes on Wafer 2-5	117
36. Total Energy Input at the Second Breakdown Threshold for Diodes on Wafer 2-4	121

37.	Total Energy Input at the Second Breakdown Threshold for Diodes on Wafer 2-4	123
38.	Total Energy Input at the Second Breakdown Threshold for Diodes on Wafer 2-1	125
39.	Total Energy Input at the Second Breakdown Threshold as a Function of N-Region Doping Level for Standard Reference and Diffusion Spike Diodes	128
40.	Total Energy Input at the Second Breakdown Threshold as a Function of N-Region Doping Level for Standard Reference and Diffusion Spike Diodes	129
41.	Current Amplitude at the Second Breakdown Threshold as a Function of N-Region Doping Level for Standard Reference and Diffusion Spike Diodes	130
42.	Current Amplitude at the Second Breakdown Threshold as a Function of N-Region Doping Level for Standard Reference and Diffusion Spike Diodes	131
43.	Voltage Waveforms Showing Second Breakdown in Standard Reference Diodes on Wafer 2-5	134
44.	Breakdown Voltage Versus N-Region Length for Standard Reference, P ⁺ N Diffusion Spike, and N ⁺ N Diffusion Spike Diodes on Wafer 2-5	136
45.	Breakdown Voltage Versus N-Region Length for Standard Reference, P ⁺ N Diffusion Spike, and N ⁺ N Diffusion Spike Diodes on Wafer 2-4	143
46.	Breakdown Voltage Versus N-Region Length for Standard Reference, P ⁺ N Diffusion Spike, and N ⁺ N Diffusion Spike Diodes on Wafer 1-3	145
47.	Breakdown Voltage Versus N-Region Length for Standard Reference, P ⁺ N Diffusion Spike, and N ⁺ N Diffusion Spike Diodes on Wafer 2-2	146
48.	Breakdown Voltage, Versus N-Region Length for Standard Reference, P ⁺ N Diffusion Spike, and N ⁺ N Diffusion Spike Diodes on Wafer 2-1	147
49.	Breakdown Voltage Versus N-Region Doping Level for Standard Reference Diodes with N-Region Lengths of 10, 30, and 100 μ m	149

50. Breakdown Voltage Versus N-Region Length for Standard Reference and Enclosed Reference Diodes on Wafer 2-5	150
51. Breakdown Voltage Versus N-Region Length for Standard Reference and Enclosed Reference Diodes on Wafer 2-4	152
52. Breakdown Voltage Versus N-Region Length for Standard Reference and Enclosed Reference Diodes on Wafer 1-3	153
53. Breakdown Voltage Versus N-Region Length for Standard Reference and Enclosed Reference Diodes on Wafer 2-2	154
54. Breakdown Voltage Versus N-Region Length for Standard Reference and Enclosed Reference Diodes on Wafer 2-1	155
55. Damage Morphology Due to 10 μ s Pulses Having Amplitudes Just Above the Damage Threshold	157
56. Filament Locations on the Most Highly Doped Wafer (Wafer 2-5)	158
57. Filament Locations on Wafer 2-4	162
58. Filament Locations on Wafer 1-3	164
59. Filament Locations on Wafer 2-2	165
60. Filament Locations on Wafer 2-1	166
61. Reverse Bias Tests of Three P ⁺ N Multiple Spike Diodes on Wafer 2-5	169
62. Breakdown Voltage Versus Spike Length for Multiple Diffusion Spike Diodes on Wafer 2-5	171
63. Breakdown Voltage Versus Spike Length for Multiple Diffusion Spike Diodes on Wafer 2-4	174
64. Breakdown Voltage Versus Spike Length for Multiple Diffusion Spike Diodes on Wafer 1-3	175

65. Breakdown Voltage Versus Spike Length for Multiple Diffusion Spike Diodes on Wafer 2-5	176
66. Filament Locations on Multiple Diffusion Spike Diodes on Wafer 2-5	178
67. Reverse Bias Tests of Three Radius of Curvature Diodes on Wafer 2-5	181
68. Breakdown Voltage Versus N-Region Length for Standard Reference and Radius of Curvature Diodes on Wafer 2-5	183
69. Breakdown Voltage Versus N-Region Length for Standard Reference and Radius of Curvature Diodes on Wafer 2-4	184
70. Breakdown Voltage Versus N-Region Length for Standard Reference and Radius of Curvature Diodes on Wafer 1-3	185
71. Breakdown Voltage Versus N-Region Length for Standard Reference and Radius of Curvature Diodes on Wafer 2-2	186
72. Breakdown Voltage Versus N-Region Length for Standard Reference and Radius of Curvature Diodes on Wafer 2-1	187
73. Reverse Bias Tests of Two Interdigitated Diodes on Wafer 2-5	190
74. Voltage-Current-Time Surface of a Reverse Biased Standard Reference Diode on Wafer 2-5	194
75. Voltage-Current-Time Surface of a Reverse Biased P ⁺ N Diffusion Spike Diode on Wafer 2-5	197
76. Voltage-Current-Time Surface of a Forward Biased Standard Reference Diode on Wafer 2-5	200
77. I-V Curves Representing a Standard Reference Diode with an N-Region Length of 30 μm and Width of 200 μm on Wafer 2-5	204
78. Attempt to Determine the Onset of Second Breakdown for a Standard Reference Diode on Wafer 2-5	206

79.	Constant Current Pulses of Increasing Amplitude Applied to a Standard Reference Diode on Wafer 2-4	207
80.	Microplasma Emission	209
81.	Forward Bias Tests at Increasing Levels of Excitation on a Standard Reference Diode on Wafer 2-5	215
82.	Forward Bias Tests of a P ⁺ N and N ⁺ N Spike Diode on Wafer 2-5	217
83.	Test of a Four Terminal Diode with the P ⁺ N and N ⁺ N Junctions Open-Circuited	219
84.	Voltage and Current Waveforms of a Standard Reference and a P ⁺ N Spike Diode on Wafer 2-5	222
85.	Energy Versus Delay Time for a Standard Reference and a P ⁺ N Spike Diode on Wafer 2-5	224
86.	Current Versus Delay Time for a Standard Reference and a P ⁺ N Spike Diode on Wafer 2-5	225
87.	Energy Versus Delay Time for Diodes on Wafer 2-5 with Straight P ⁺ N and N ⁺ N Junctions, an N-Region Length of 30 μ m, and a Width of 200 μ m	227
88.	Current Versus Delay Time for Diodes on Wafer 2-5 with Straight P ⁺ N and N ⁺ N Junctions, an N-Region Length of 30 μ m, and a Width of 200 μ m	228
89.	Average Versus Delay Time for Diodes on Wafer 2-5 with Straight P ⁺ N and N ⁺ N Junctions, an N-Region Length of 30 μ m, and a Width of 200 μ m	229
90.	Reverse Bias Test of a Standard Reference Diode on Wafer 2-5	230
91.	Temperature Measurements	233
92.	Temperature Calibration Curve for Silicon Films 0.4 μ m and 0.6 μ m Thicknesses	235

93. Geometry of silicon-on-sapphire diode with uniform junctions	258
94. Division of the diode into elements	259
95. Thermal conductivities of silicon and sapphire as functions of temperature	264
96. Thermal diffusivity of sapphire as a function of temperature	268
97. Schematic diagrams to show the effect of the linear approximation to $\phi(t)$ in the n regions of current strips	271
98. Electron velocity versus electric field at constant temperature	295
99. Hole velocity vs electric field at constant temperature	296
100. Resistivity vs temperature at constant electric field	297
101a. J_{po} vs temperature at constant J and J_{do} vs temperature	298
101b. Intrinsic carrier density vs temperature	298
102. Electron (a) and hole (b) ionization coefficients vs electric field for constant temperatures	299
103. Voltage vs temperature at constant current densities for the junction of n region. The voltage V_n is developed across a strip in the n region having the width of the junction depletion region	300
104. Junction width vs temperature for different current densities	304
105. Electric field vs distance in the depletion layer at constant current density and constant temperature	305
106. Resistivity vs distance in the depletion layer at constant current density and constant temperature	306
107. Electron density as a function of position in the depletion layer at constant current density and constant temperature	307
108. Hole density vs distance in the depletion layer at constant current density and constant temperature	308
109. Electron current density vs distance in the depletion layer at constant current density and constant temperature	309
110. Carrier generation rate due to avalanching vs distance in the depletion layer at constant current density and constant temperature	310

111.	Carrier recombination rate vs distance in the depletion layer at constant current density and constant temperature	311
112.	Electron ionization coefficient vs distance in the depletion layer at constant current density and constant temperature	312
113.	Hole ionization coefficient vs distance in the depletion layer at constant current density and constant temperature	313
114.	Electron velocity as a function of position in the depletion layer at constant current density and constant temperature	314
115.	Hole velocity vs distance in the depletion layer at constant current density and constant temperature	315
116a.	Current distributions at different times for an 8 mA constant current pulse	325
116b.	Current distributions at different times for a 9 mA constant current pulse	326
116c.	Current distributions at different times for a 10 mA constant current pulse	327
116d.	Current distributions at different times for a 10.5 mA constant current pulse	328
116e.	Current distributions at different times for an 11 mA constant current pulse	329
116f.	Current distributions at different times for a 12 mA constant current pulse	330
117a.	Current distributions at different times for a 9 mA pulse showing the early stages of filamentation	331
117b.	Current distributions for the same 9 mA current step as in (a), but at later times. Development of the fine filament is detailed	332
118a.	Current distributions for an 11 mA current step during the early stages of filamentation	333
118b.	Current distributions for the same 11 mA current step as in (a), but at later times. Development of narrow double filaments is detailed	334
119.	Resistivity (ρ) and junction voltage (V_{jun}) as functions of temperature	336
120a.	Temporal development of temperature at various portions of the diode with applied pulse amplitude of 9 mA	337

120b.	Temporal development of temperature at various portions of the diode with applied pulse amplitude of 11 mA	338
121a.	Temporal development of current with pulse amplitudes of 9 mA	339
121b.	Temporal development of current with pulse amplitude of 11 mA	340
122a.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 8 mA	345
122b.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 9 mA	346
122c.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 10 mA	347
122d.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 10.5 mA	348
122e.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 11 mA	349
122f.	Temporal development of temperature profiles for different step amplitudes with current amplitude of 12 mA	350
123.	Voltage waveform for a constant current pulse of 9 mA	352
124a.	Voltage waveforms with current amplitude of 9 mA	354
124b.	Voltage waveforms with current amplitude of 11 mA	355
125.	Voltage waveforms for pulse amplitudes in the range 8-12 mA	357
126.	Delay times for the onset of filamentation and for the onset of instability for different pulse amplitudes	359
127a.	Effect of pulse amplitude on current distributions at constant pulse length of 3.5 μ s	360
127b.	Effect of pulse amplitude on current distributions at constant pulse length of 4.1 μ s	361
127c.	Effect of pulse amplitude on current distributions at constant pulse length of 7.5 μ s	362
127d.	Effect of pulse amplitude on current distributions at constant pulse length of 9.7 μ s	363
128.	Input energy for the onset of filamentation (1) and for the onset of instability (2) as a function of the delay times, τ_{fil} and τ_{ins} , respectively	365

129.	A representative double-step current waveform	367
130.	Current distributions for single and double step pulses of the same duration	368
131.	Current distributions for single and double step pulses	369
132.	Current distributions for single and double step pulses of the same duration	370
133.	Geometry of an SOS diode with three p^+n diffusion spikes	371
134a.	Current distributions of 8 mA at different times in an SOS diode with three p^+n diffusion spikes	373
134b.	Current distributions of 9 mA at different times in an SOS diode with three p^+n diffusion spikes	374
134c.	Current distributions of 10 mA at different times in an SOS diode with three p^+n diffusion spikes	375
134d.	Current distributions of 11 mA at different times in an SOS diode with three p^+n diffusion spikes	376
134e.	Current distributions of 12 mA at different times in an SOS diode with three p^+n diffusion spikes	377
135a.	Temporal development of temperature profiles of a p^+n spike diode for pulse amplitude of 8 mA	379
135b.	Temporal development of temperature profiles of a p^+n spike diode for pulse amplitude of 9 mA	380
135c.	Temporal development of temperature profiles of a p^+n spike diode for pulse amplitude of 10 mA	381
135d.	Temporal development of temperature profiles of a p^+n spike diode for pulse amplitude of 11 mA	382
135e.	Temporal development of temperature profiles of a p^+n spike diode for pulse amplitude of 12 mA	383
136.	Temporal development of temperature at various positions of an SOS diode with p^+n triple spikes with pulse amplitude of 9 mA ...	384
137.	Time development of current in a p^+n triple spiked diode with applied pulse amplitude of 9 mA	385
138.	Voltage waveform for a p^+n spiked diode. The excitation pulse amplitude is 8 mA	387
139.	Voltage waveforms for pulse amplitudes in the range 8-12 mA for a p^+n spiked diode	388

140.	Voltage waveforms for various portions of a p^+n spiked diode. The pulse amplitude is 9 mA	389
141.	Delay time for the onset of filamentation (1) and for instability (2) at various excitation amplitudes for a p^+n spiked diode	392
142.	Input energy for the onset of filamentation (1) and for the onset of instability (2) as a function of the square roots of the delay times, τ_{fil} and τ_{ins} , respectively	393
143.	Current distributions at different times in a p^+n spiked diode when the silicon film thickness is 1.2 μm	395
144.	Temperature profiles of a p^+n spiked diode as they develop in time. Pulse length is 9.12 μs , amplitude is 11 mA, and silicon film thickness is 1.2 μm	396
145.	Voltage waveform for a p^+n spiked diode with silicon film thickness of 1.2 μm . The pulse amplitude is 11 mA	397
146.	Current distributions for p^+n spiked diodes of 0.6 μm and 1.2 μm silicon thickness at pulse amplitudes of 10.5 and 21 mA, respectively	399
147a.	Current distribution at different times in a uniform junction diode for an excitation pulse amplitude of 7 mA. Current distributions at times 0.17, 13.98, 15.98, and 17.78 μs .	401
147b.	Current distributions at different times in a uniform junction diode for an excitation pulse amplitude of 7 mA. Current distributions at times 0.17, 16.98, 17.48, 17.78 μs	402
148a.	Temporal development of temperature profiles of uniform junction diode for a 7 mA pulse amplitude. Temperature profiles at times of 0.17, 13.98, 15.98, and 17.78 μs	403
148b.	Temporal development of temperature profiles of uniform junction diode for a 7 mA pulse amplitude. Temperature profiles at times 0.17, 16.98, 17.48, and 17.78 μs	404
149a.	Temporal development of temperature in a uniform junction diode at a pulse amplitude of 7 mA. Temperature profile of the mid points in the n region of strips with current filaments	405
149b.	Temporal development of temperature in a uniform junction diode at a pulse amplitude of 7 mA. Temperature profiles of the mid points of the n region of strips <u>not</u> containing current filaments	406
150.	Junction and n-region voltage waveforms of the indicated strips of a uniform junction diode excited by a pulse of 7 mA	407

151. Voltage waveform of a uniform junction diode for a pulse amplitude of 7 mA	408
152a. Current distributions in a p^+n diffusion spike diode at the indicated times for a 7 mA pulse amplitude. Current configurations at 0.96, 7.46, 8.56, and 9.67 μs	411
152b. Current distributions in a p^+n diffusion spike diode at the indicated times for a 7 mA pulse amplitude. Current configurations at 0.96, 9.06, 9.56, and 9.67 μs	412
153a. Temperature profiles at the times indicated in a p^+n spike diode for a pulse of 7 mA. The three filaments are located on the strips with spikes. Temperature profiles at 0.96, 7.46, 8.56, and 9.66 μs	414
153b. Temperature profiles at the times indicated in a p^+n spike diode for a pulse of 7 mA. The three filaments are located on the strips with spikes. Temperature profiles at times of 0.96, 9.06, 9.56, and 9.67 μs	415
154. The temporal development of temperature at various portions of a p^+n spike diode with a 7 mA current pulse	416
155a. Junction voltage and corresponding n-region voltage waveforms for a p^+n spike diode. Strips away from spikes	417
155b. Junction voltage and corresponding n-region voltage waveforms for a p^+n spike diode. Strips containing spikes	418
156. Voltage waveform for a p^+n spike diode for a pulse amplitude of 7 mA	420
157. Current distribution in an n^+n spike diode at the indicated times for a pulse amplitude of 7 mA	422
158. Temporal development of temperature profiles of an n^+n diffusion spike diode for a 7 mA pulse amplitude. The three filaments are on the strips with spikes	423
159. The temporal development of temperature at various portions of an n^+n diffusion spike diode. Spikes are located at distances of 50, 102, 174 μm from one edge of the diode	424
160. Junction and corresponding n-region voltage waveforms of strips with spikes in an n^+n spike diode. Spikes are located 50, 102, and 174 μm from one edge of the diode	425
161. Voltage waveform for a 7 mA pulse in an n^+n diffusion spike diode	427
162. Comparison of experimental (E) and calculated (C) waveforms	431

163.	Junction width as a function of doping density at $T = 300$ K and applied current density $J_{\text{applied}} = 1 \times 10^8$ A/m ²	461
164.	Electric field as a function of distance from a $p^+ - n$ junction at various applied pulse amplitudes. $T = 300$ K and doping density $N_D = 1 \times 10^{22}$ atoms/m ³	462
165.	Junction width as a function of applied current densities. $T = 300$ K and $N_D = 1 \times 10^{22}$ atoms/m ³	464
166.	Junction voltage - current density characteristics at various device temperatures. $N_D = 1 \times 10^{22}$ atoms/m ³	465
167.	Alteration of space charge density and of junction width due to an increase in J_{applied} . $T = 300$ K, $N_D = 1 \times 10^{22}$ atoms/m ³ .	466
168.	Graph showing the influence of temperature on thermally generated current carriers and thereby on the reverse saturation current density J_{po} . $N_D = 1 \times 10^{22}$ atoms/m ³	468
169.	Effect of temperature on the spatial gradient of the space charge density. $J_{\text{applied}} = 1 \times 10^8$ A/m ² and $N_D = 1 \times 10^{22}$ atoms/m ³	469
170.	Junction voltage - temperature characteristics at various applied pulse amplitudes. $N_D = 1 \times 10^{22}$ atoms/m ³	470
171.	Electric field profiles as a function of distance from $p^+ - n$ junction at various temperatures. $N_D = 1 \times 10^{22}$ atoms/m ³ and applied current density $J_{\text{applied}} = 1 \times 10^8$ A/m ²	471
172.	Effect of junction temperature on the depletion layer width. $J_{\text{applied}} = 1 \times 10^8$ A/m ² and $N_D = 1 \times 10^{22}$ atoms/m ³	472

ACKNOWLEDGEMENTS

The authors wish to acknowledge the suggestions and support of David Mathews (U.S. Army Missile Research and Development Command), Donald Wunsch and Robert Turfler (BDM Corporation, and Harold Phillips and Larry Greene (Rockwell International). The aid of Helen Knight, Pamela Webb, Trish Ray, Sandra Simmons and Miriam Halen in preparing the manuscript is greatly appreciated.

I. INTRODUCTION

Second breakdown in semiconductor devices occurs through the formation of current filaments under sufficiently high electrical stress. Permanent damage is produced when the temperature of a current filament reaches the melting point. Multiple filaments can form under high amplitude excitation, such as might occur in electrostatic discharge, inductive impulses, EMP, or switching transients. Second breakdown has been shown to be the dominant failure mechanism under impulsive conditions in a wide range of semiconducting devices, including microwave diodes, other diodes, junction transistors, MOS devices, power components, integrated circuit components, silicon devices, GaAs devices, and germanium devices. As devices become smaller, they become more susceptible to damage via second breakdown.

The dynamics of filament formation have been studied in silicon-on-sapphire (SOS) devices through a stroboscopic technique. Both forward and reverse bias observations have been placed into the perspective of an electrothermal mechanism. The features observed in the planar SOS devices are similar to those observed in three-dimensional systems. The previous work on second breakdown has given a good qualitative view of the filamentation process, but more quantitative knowledge has been needed for the development of second breakdown screening techniques, for understanding the nature of maverick devices, and for designing devices with improved resistance to second breakdown.

The onset of current filamentation is sensitive to device geometry, doping, circuital environment and excitation conditions. During the production of a particular group of devices, non-identical devices are obtained because of lack of perfect mask registration, imperfect etching, irregular diffusions, dust and contaminants, lattice strains, variations in the microstructure of the base material, and other reasons. Such effects are very difficult to assess. In order to explore the role of device geometry on second breakdown, an array of p^+-n-n^+ diodes was specially designed and fabricated at Rockwell International. The design allowed the systematic exploration of the roles of device doping, junction length, n-region length, p^+n and n^+n junction spikes, metallization spikes, and configurations producing current crowding.

The initial goals of the present program were:

1. "To assess the relative importance of device geometry, metallization and diffusion spikes, and device doping on second breakdown susceptibility for electrical excitation pulses of 0.1, 1, and 10 μs under both forward and reverse biases."
2. "To apply the results of simultaneously observed filament configuration and voltage and current waveforms to the development of non-destructive screening tests for second breakdown in silicon-on-sapphire diodes."
3. "If time permits, to develop analytical models for the influences of diode geometry, doping, diffusion spikes and metallization spikes on current filamentation under both forward and reverse biases in silicon-on-sapphire diodes. Such models should provide a basis for the design of diodes that are more resistant to second breakdown."

4. "If time permits, to obtain temperature-time mappings of silicon-on-sapphire diodes as filaments are formed. Such mappings will serve as a further guide to the development of theoretical models of filamentation."

A dual experimental-theoretical approach has been pursued. E. R. Knight has performed most of the experimentation, while A. Baruah-Satin has developed most of the theoretical effort. F. T. Liou has contributed to portions of both the experimental and theoretical efforts. Overall direction has come from P. P. Budenstein.

Not all of the goals have been realized. Limitations of circuit geometry and device parameters prevented use of 0.1 and 1 μ s pulses, as contained in Goal 1. Goal 4 was not addressed at all because of lack of time. However, the other goals have been pursued and will form the basis for this report. Part I (based primarily on the doctoral dissertation of E. R. Knight and the M.S. thesis of F. T. Liou) relates to Goal 1, the experimental effort. Part II (based primarily on the doctoral dissertation of A. Baruah-Satin, with an additional contribution by F. T. Liou) relates to Goal 2, screening tests, and to other implications.

II. BACKGROUND ON EXPERIMENTATION

A. History of the Second Breakdown Problem

Second breakdown is a transition to a state of higher conductance which occurs at high current densities in silicon electronic components. This transition may be accompanied by device degradation or destruction, and it is generally regarded as one of the principal failure modes of silicon junction devices subjected to electrical overstresses. Second breakdown is frequently the limiting phenomenon in power transistors that are switched in the presence of inductive loads. The early work of Thornton and Simmons¹ showed that the power level at the occurrence of damage was less than the rated power level of the device under normal operating conditions. Subsequently, Schafft and French², Reich and Hakim³, Dumin⁴, and Sunshine⁵ showed, each by a different method, that current filamentation is an integral part of the second breakdown transition.

In a series of critical reviews, Schafft and French⁶⁻⁹ pointed out that second breakdown is a very general phenomenon, common to junction devices despite the many variations in geometry and doping profile. They concluded that it was primarily a thermal effect, although the abruptness of the transition had suggested to some investigators that the transition is electronic in nature¹⁰⁻¹². Studying second breakdown by applying short, high-amplitude pulses, Schafft and French, Ferry and Dougal¹³, and Melchior and Strutt¹⁴ have shown that there is a delay

time between the application of the pulse and the onset of the second breakdown transition. For a pulse duration less than about 100 μ s, the delay time decreased with increasing pulse amplitude, corresponding to a constant energy input of about 10^{-4} J in the devices considered. Schafft and French interpreted this as a very strong indication of a thermal basis for the second breakdown phenomenon.

Damage accompanying second breakdown occurs through formation of a melt channel^{15,16} or a series of such channels in very high amplitude testing¹⁶. Such channels permanently degrade the device. In some situations, the excitation is removed after the conductance has increased appreciably (due to current filamentation), but before the development of the damaging melt.

Probably the most detailed studies of the mechanism of second breakdown are those of Sunshine^{5,17} and Budenstein, Pontius, and Smith¹⁸⁻²², wherein second breakdown was investigated in silicon-on-sapphire diodes using a stroboscopic technique. Sunshine was able to show the time history of the formation of current filaments and to correlate the second breakdown transition with the propagation of a filament across the high resistance region of the diode. Filament formation was related to the J-V-T behavior of the junction and the resistivity-temperature dependence of the bulk material. However, limitations in geometry and in the method of observation allowed only portions of the filamentation problem to be explored. Budenstein, Pontius, and Smith improved Sunshine's stroboscopic technique and delved further into the details of second breakdown in thin film silicon-on-sapphire diodes. Nucleation of current filaments, filament growth,

and damage through the formation of melt channels were observed and related to the voltage waveforms, geometry, and base layer resistivity.

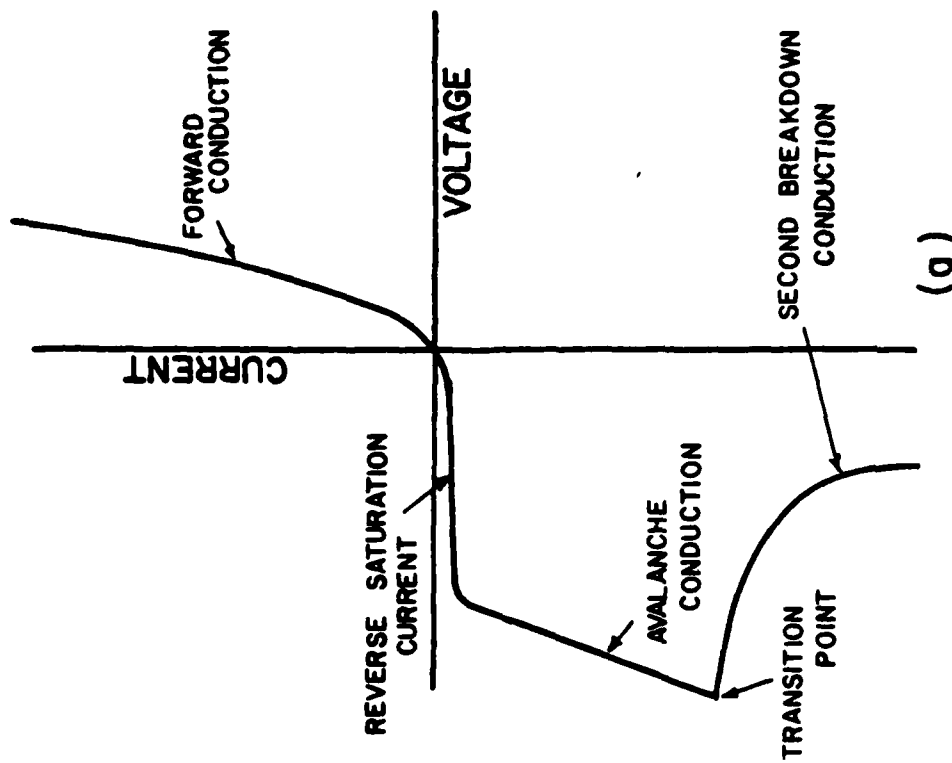
The general problem of filamentation has attracted considerable attention since the work of Ovshinsky²³, although an extensive literature predated his work. This literature is reviewed by Barnett²⁴ with an emphasis on injection phenomena in semiconductors. Muller and Guckell¹¹ have made a simplified analysis of filamentation in connection with second breakdown. Ridley²⁵ discusses filamentation and stability of current configurations from the standpoint of irreversible thermodynamics, invoking the principle of minimum entropy production to identify the steady state. Stable filaments are formed, according to Ridley, when the current configuration is such that joule heating is a minimum. Fabricius²⁶ has explored current filamentation due to electromagnetic forces alone, as in a plasma pinch. He concludes that such effects are not important, except perhaps at very low temperatures. Thus, filamentation is a very common phenomenon, occurring whenever some local region attains a higher conductance than its surroundings.

A more complete history of the second breakdown problem will now be given. Studies on bulk devices will be discussed first, and then the work on silicon-on-sapphire devices by Dumin and Sunshine, and by Budenstein, Pontius, and Smith. Finally, an outline of the present investigation will be given.

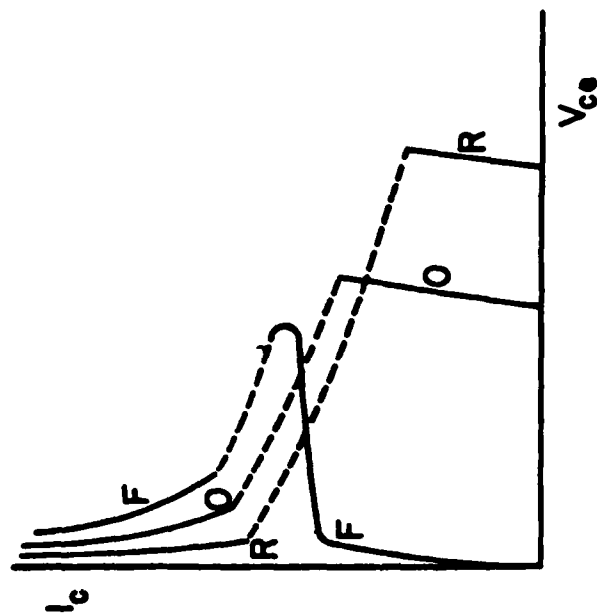
B. Second Breakdown in Bulk Devices

1. I-V Characteristics in Diodes and Transistors

A diode I-V characteristic is shown schematically in Fig. 1a, at a temperature well above room temperature to emphasize the possibility



(a)



(b)

Fig. 1. I-V characteristics showing second breakdown. (a) Diode. (b) Transistor, collector characteristic exhibiting second breakdown, after Schafft and French. For curve F, the E-B terminals are forward biased; for curve O, the base is open; and for curve R, the E-B terminals are reverse biased.

that the reverse saturation current of the diode may be appreciable. Voltage is a single-valued function of the current. Five current regions can be distinguished--forward current, forward second breakdown current (not shown), reverse saturation current, avalanche current, and reverse second breakdown current. When the device is driven hard enough to display the second breakdown current, there is always considerable heating and frequently permanent damage. Hence, a conventional curve tracer operated at 60 Hz generally should not be used for avalanche currents greater than a few milliamperes. With single pulse testing, heating effects can be made smaller. To avoid device damage, the pulse duration must be appropriately shortened as pulse amplitude is increased. Depending on the device under test and the nature of the external circuit, several turnovers may occur in the reverse characteristic, sometimes at relatively low avalanche currents.²⁷ Most of the testing of diodes has been done with square voltage pulses applied across the diode in series with a constant resistance.

The second breakdown features of the I-V characteristics of transistors are more complicated than diode characteristics for several reasons. First, the geometry of the transistor is more complex and probably less homogeneous locally. Second, as the transistor's emitter bias is altered, its current pattern changes.² Third, the primaries for avalanching in the diode are the minority carriers in the lightly doped side of the pn junction, while in the transistor the primaries for base-collector avalanche are the injected carriers from the emitter, which depend on the local bias conditions of the emitter-base junction. Fourth, the emitter-base junction has a nonuniform bias be-

cause of the flow pattern of the base current.²⁸ Schafft and French² have shown that the current distribution in a transistor under forward bias tends to be more uniformly distributed over the collector junction than is the case for reverse bias. Moreover, resistive ballasting can be used in the emitter circuit to enhance the current uniformity under forward bias²⁹, but no effective method (without otherwise degrading performance) has been found to enhance current uniformity under reverse bias. Figure 1b (after Schafft) shows schematically the collector-emitter voltage V_{CE} for different emitter-base bias. The transition from avalanche to second breakdown of the base-collector junction occurs at a lower V_{CE} when the emitter is forward rather than reverse biased.²⁹ Further, the current in the second breakdown mode for a given V_{CE} is greater for forward than reverse emitter bias.

Temperature effects in transistors have been summarized by Pritchard³⁰, Gartner³¹, and Matz³².

2. Time Delay and Related Effects

The time between the application of a large amplitude voltage pulse and the occurrence of second breakdown has been defined as the delay time. It is generally regarded as a thermal effect, but its exact nature has not been established. Thus, Fleming³³ fixes the delay time to be "that time at which the constant junction current density J , as a result of a junction temperature rise, is supported by a junction voltage V of 5 percent less than the breakdown voltage V_B ." The principal justification for such a criterion is that, along with the assumption that the junction I-V characteristic is not a strong function

of temperature and that all heat input is at the junction, it allows computation of delay times of the right order of magnitude. The physical reality of the model, however, is questionable.

Nienhuis²⁹ attempted to characterize device behavior in terms of the time delay to second breakdown. In extensive tests at forward and reverse emitter bias, he studied the current amplitude and delay time for second breakdown using pulses of fixed duration. He found, on reverse bias tests of the emitter, a voltage rise in the V_{CE} voltage just before the onset of the second breakdown. This rise, not reported by others, was independent of the current level at second breakdown and its magnitude was correlated with the delay time. If the voltage were large, the delay time would be long and the resistance to second breakdown good. Nienhuis, assuming that the collector current is nonuniform because of the nonuniformity in the temperature, suggested a phenomenological model for the observed results.

3. Hot Spots and Current Channeling

The evidence for hot spots in transistors prior to the onset of second breakdown comes from direct observations by Reich and Hakim³ using an infrared microscope, from Schafft and French² using temperature sensitive phosphors, from Agatsuma³⁴ using temperature sensitive lacquers, from Chiang and Lauritzen³⁵ using light emission, and from a variety of less direct observations.

Reich and Hakim^{3,36,37} have employed the idea of a transient thermal resistance to explain the "energy dependence" of second breakdown. Thermal resistance is a steady-state concept; it is the temperature

rise (assumed uniform throughout the system) per unit power input. For low power levels in a transistor, the currents are distributed nearly uniformly over the junction areas so the thermal resistance determines the equilibrium temperature for a given power input. However, when hot spots occur, both the current and temperature configurations are drastically altered. If the energy due to a sharp pulse of input power is highly localized, the thermal resistance concept can be applied to the region of localization--a given power input producing a much higher temperature than would be the case for the transistor structure as a unit. Reich and Hakim found different thermal resistances for forward and reverse emitter biases, the thermal resistance being greater for reverse bias. This implies a smaller region is being heated under reverse bias than forward bias, that is, hot spots are more severe with reverse bias. Reich and Hakim concluded, after testing transistors with different doping contours, that hot-spotting was retarded as the product of the resistivity and thickness of the collector material increased.

Schafft and French² used zinc-cadmium sulphide phosphors to indicate the surface temperature distribution on transistors because of the ease of use, speed of response, reproducibility, range of temperature sensitivity, and the low cost of the phosphors. A thin layer of the phosphor powder was mixed with a silicone binder and applied directly to the surface of planar silicon transistors. The phosphor was bathed in ultraviolet radiation from a mercury lamp. As the temperature of the phosphor is increased, the intensity of luminescence decreases and finally goes to zero. Thus, when a transistor carried a nonuniform

current and hence, had a nonuniform temperature, the variations in the emission of the phosphors gave a qualitative picture of the temperature configuration of the system.

Invariably, the current distribution prior to second breakdown was asymmetric and nonuniform at higher currents, the pattern depending strongly upon device geometry. Typically, the application of forward base drives minimized any existing concentrations in current while the application of reverse base drives tended to accentuate existing nonuniformities and to shift them. When second breakdown did occur, the second breakdown current constriction appeared within the region of initial high current density.

The use of the phosphors revealed that the current distribution can be shifted by changes in the base drive, collector current, externally induced potential gradients along the emitter junction, and non-catastrophic damage due to previous entry into second breakdown. Once in second breakdown, a sufficiently large base drive can cause the transistor to switch out of second breakdown and into its normal forward base drive operating mode.

Agatsuma³⁴ coated n-v-n devices with temperature-sensitive paint (Tempilaq) and found that the temperature at the turnover point of the I-V characteristic occurred at about the temperature at which the v-material became intrinsic. This temperature was 170 to 212 °C for 50 ohm-cm, 212 to 253 °C for 27 ohm-cm, and 320 to 343 °C for 3 ohm-cm material. The turnover was not regarded by Agatsuma as second breakdown, but the observation was regarded as very suggestive of the second breakdown mechanism.

Chiang and Lauritzen³⁵ fabricated diodes with a guard ring structure and a thin ($0.5\text{ }\mu\text{m}$) layer of p^+ material over an n -base, the inner diameter of the p -type guard ring being $30\text{ }\mu\text{m}$. This produced a small diode $30\text{ }\mu\text{m}$ across with a minimum of edge effects. Moreover, the p^+ layer was sufficiently thin that avalanche light emission and light emission accompanying filamentation were visible. Thus, the emission patterns could be observed as a function of current amplitude and any changes in localization observed. Filamentation could be observed and correlated with changes in the I - V characteristic. The avalanche voltage V_B was measured as a function of temperature, and a nearly linear plot was obtained between 100 and 800 K, in agreement with Crowell and Sze.³⁸ At the higher temperatures the curves were starting to bend over.

The diodes of Chiang and Lauritzen were highly doped, with a donor concentration in the low resistivity side of about $2 \times 10^{18}\text{ cm}^{-3}$. The temperature at which the intrinsic concentration n_i was equal to the donor density was about 1100 K and the temperature at thermal breakdown was estimated to be about the same value. Thus, they conclude that thermal breakdown occurs when the junction goes intrinsic, as suggested by Melchior and Strutt¹⁴. They develop a phenomenological theory which describes the voltage drop at the intrinsic temperature and also includes, through variation of an areal parameter, filamentation. They conclude that the voltage drop is not associated with formation of a melt, but that local melting is a likely consequence of the transition to a filament. The authors point out their results differ from those

of Dumin and explain the difference in terms of the high doping density of their diodes:

"Dumin proposes a different model for thermal breakdown in his work on thin-film silicon-on-sapphire diodes. Thermal breakdown occurs in his diodes when the injected avalanche carrier concentration becomes comparable to the background doping density. Dumin's model is not applicable to the bulk p-n junction diodes used in our experiments where thermal breakdown occurs when the injected avalanche carrier concentration is still two orders of magnitude below the background doping density."

4. Radiation and Second Breakdown

The electromagnetic spectrum emitted during second breakdown conduction has been extensively investigated by Portnory and Gamble³⁹, Dumin⁴, and Sunshine.⁵ In this section the work of Portnory and Gamble will be described; that of Dumin and Sunshine will be presented in Section II.C.

Portnory and Gamble spectrally analyzed the light emitted by avalanche breakdown, second breakdown, and by resistively heated silicon rods. The light emission during avalanche and that during second breakdown had indistinguishable continuous spectra. Second breakdown in the emitter junction caused the same spectrum as second breakdown of the collector junction. Portnory and Gamble felt their observations could not be explained on a purely thermal basis, but that thermal effects could follow the appearance of an "unstable microplasma" rather than that thermal effects lead into the highly conducting state.

5. Damage

Most investigators of second breakdown conclude that the second breakdown transition is not inherently destructive, but damage occurs only if heat-sinking is inadequate. Damage manifests itself through changes in the I-V characteristics and visual observation of the device. When there is electrical damage, it usually is in the nature of a resistive short-circuit of one or both junctions. Physical damage occurs as melt channels, melting of metallizations, and punchthrough (dielectric breakdown) of passivating layers.¹⁶ Second breakdown, with its characteristic voltage drop and current rise, seems to be connected primarily with the melt channels.

C. Second Breakdown in Silicon-On-Sapphire Diodes

Dumin⁴ and Sunshine^{5,17} and Budenstein, Pontius, and Smith¹⁸⁻²² have performed experiments that yield the most detailed description of second breakdown. Dumin initiated studies of second breakdown using silicon-on-sapphire diodes. The diodes were single crystal silicon thin films grown epitaxially on sapphire substrates with p^+ and n^+ diffusions to create the junction and contact regions. Metallizations were of aluminum. The p^+ - n^+ spacing was made variable from 12.5 to 100 μm in 12.5 μm increments. The distinctive aspect of these diodes is that the current path is transverse to the direction of observation and the junction is observable in its entirety.

Dumin recorded the I-V characteristics of his diodes on a 60 Hz curve tracer while the diodes were being viewed under an optical microscope. Avalanche emission and second breakdown "plasma" emission were

both photographed for different amplitudes of the exciting voltage. To obtain instantaneous I-V characteristics, the diodes were driven by pulsed currents variable in duration from 0.01 to 100 μ s. The repetition rate of the pulses was variable and the decay time at the end of a pulse was about 0.01 μ s.

Radiation emitted from the diodes under pulsed excitation was incident upon a photomultiplier so that the light intensity waveform could be correlated with voltage and current waveforms. The spectrum of the light was analyzed with a spectrometer terminated with the same photomultiplier. A broad-band spectrum was found, the same as that of Portnoy and Gamble.³⁹ Emission from the avalanche microplasma region was only visible under an optical microscope, while the second breakdown radiation from a 25 μ m by 10 μ m plasma was readily visible in a well-lighted room without optical aids.

In a diode having a base resistivity of 0.1 ohm-cm of p-type material, avalanche occurred at 12 V and the reverse saturation current at room temperature was less than 1 μ A. The junction emitted uniformly in the avalanche mode for currents above 5 mA. As the current changed, the emission would correspondingly change. Second breakdown started at 40 V and 25 mA, with an average current density of about 5×10^8 A/m². Just after the onset of second breakdown, the intensity of the avalanche emission dropped, possibly, according to Dumin, because the diode was becoming hot or because the current constriction was forming but was not yet optically visible. At 50 mA and 26 V plasma emission appears at one corner of the diode and avalanche emission over the entire diode cuts off. With a further increase in the current level,

the region of emission grows so that it both broadens and reaches toward the opposite electrode. The second breakdown transition is taken to correspond to the growth of the emission filament across the device. A brightness temperature of 1300 °C was measured with an optical pyrometer at 70 mA and 19 V. Dumin concludes this cannot be the lattice temperature since the diode was operated for 56 hours at 90 mA, 17 V and brightness temperature above 1300 °C with no physical deterioration, loss of light output, or change in the I-V characteristic.

Dumin was unable to follow photographically the time history of the current distribution during a single pulse. Sunshine, using diodes provided by Dumin and working in Dumin's laboratory, developed a stroboscopic technique which does give this time history. Sunshine uses the fact that the light transmission through a thin-film silicon-on-sapphire diode, when illuminated by an external source, is strongly temperature dependent. As the temperature goes up, the transmitted light decreases. Sunshine used as a pulsed light source an aluminum-gallium-arsenide laser (output at 7100 Å at 77 K) synchronized with the constant current pulses that he applied to the diodes. (He is probably the first one doing second breakdown studies who insisted on using constant current pulses rather than constant voltage or, more typically, constant voltage across a network containing the junction device in series with an external fixed resistance. Constant current is a more controlled testing scheme since the voltage across the device is a single-valued function of the current, whereas the current is not a single-valued function of the voltage.) He used repetitive pulses of

100 μ s duration and turned on his laser strobe light at some variable time after the initial rise of the pulse. The strobe was on for 0.01 μ s. By adjusting the position of the strobe light relative to the current pulse, he could examine the current configuration through the light transmittance as a function of time. Unfortunately, the laser source had two problems which made Sunshine's experiments less enlightening than they might otherwise have been. First, changes in optical transmittance could not be correlated directly to temperature because of interference effects. Secondly, the wavelength of 7100 Å is in a region of the spectrum where the eye and photographic emulsions are insensitive, so that image intensification methods had to be used. Image intensification is accompanied by a considerable loss in contrast. Thus, Sunshine's photographs distinguish between "cold" and "hot," the dividing temperature being about 400 °C. Appreciably below this temperature, there is no evidence of heating and appreciably above it, the transmittance of the laser light goes almost to zero. Another limiting factor in Sunshine's experiments was the smallness of his diodes. These covered the same size range as Dumin's and, as will be discussed below, did not reveal the range of phenomena visible with larger diodes. Sunshine studied his diodes under forward and reverse bias, noting that there is a high current transition in each case. Hence, he called both of these second breakdown. Both transitions were associated with current filamentation. In the reverse bias situation, the filament started at the junction and reached into the high resistance side of the junction to the electrode. In the forward bias condition, the filament started well within the interior of the high resistance

region and the junction appeared to play no role at all. Sunshine also made observations on the emitted light from the diodes. These were non-stroboscopic and similar in nature to Dumin's observations. Further, he could measure either light transmittance at a single position as a function of time or light emission at a single position as a function of time. Although he gives no details on these results, he mentions that a temperature resolution better than 10 °C is possible with a spatial resolution of 1 to 2 μm . The results obtained by Sunshine follow.

- a. The growth of current filaments is shown photographically and correlated to voltage waveforms and light emission. Filaments are found for both forward and reverse bias at about the same current levels.
- b. The critical condition for filament formation occurs when the temperature in the high resistance side of the junction reaches a value T_0 where the resistivity of the material is a maximum. The current and voltage in the device when this occurs are referred to as the "threshold" values and are designated by the symbols $I_{th,F}$, $I_{th,R}$, $V_{th,F}$, and $V_{th,R}$ the subscripts F and R referring to the forward and reverse bias conditions.
- c. Current filaments under forward bias develop very gradually in the high resistivity side of the junction. The onset of negative resistance occurs before the filament is clearly distinguishable from its surroundings.

- d. "For dc reverse biases less than $I_{th,R}$, the avalanche process maintains the uniformity of the current flow as the current, and hence the operating temperature are increased. When the bias reaches $I_{th,R}$, the operating temperature in some region in the junction becomes high enough that thermally generated carriers can take over the conduction process, the avalanche is thermally quenched and second breakdown occurs. The negative temperature coefficient associated with the thermally generated current results in the current constricting and flowing through a narrow region in the junction, where the temperature rises significantly. The temperature of the constriction at just above $I_{th,R}$ is typically about 700 °C, although in some diodes it can be much lower. At high biases, the constriction can become molten. The current flow pattern in the ohmic region is determined by the local temperature of the resistive material in series with the junction. The current flow pattern will remain constricted where the local temperature is above T_{Ω} , and will fan out into uniform ohmic conduction where the local temperature is below T_{Ω} .

For reverse bias switching is response to a constant current pulse, the heating is confined to the junction region. The junction avalanches uniformly until its temperature is sufficiently high for it to become thermally unstable. The current then rapidly constricts in the junction. If the temperature of the constriction is greater than T_{Ω} , the high pow-

er density region at the perimeter of the constriction elongates into the ohmic region. If the constriction temperature is less than T_{Ω} , the constriction will not extend itself into the ohmic region, and the current will flow through the constriction in the junction and fan out."⁵

- e. The temperature dependence of avalanche voltage was explored and I-V characteristics deduced using the temperature dependence in the avalanche coefficients of Crowell and Sze.³⁸ The published work of Sunshine does not include the temperature dependence of the reverse saturation current. However, in private conversations in December, 1971, he indicated that the basic thermal instability is due either (depending on the details of the system geometry) to the temperature dependence of the reverse saturation current or the turnover in the temperature-resistivity curve at temperature T_{Ω} .
- f. The time required for the voltage drop of the second breakdown transition and the accompanying voltage drop are connected with the growth of a current filament from junction to electrode on the high resistance side of the junction. The current filament is not accompanied by damage so long as the current pulse amplitude is not too high. (While Sunshine attempted to avoid damage, he indicated in private conversations that only a slight change in pulse amplitude would cause damage and, in the course of his studies, he had damaged many diodes.)

The test specimens used by Budenstein, Pontius, and Smith were diodes fabricated by Rockwell International in epitaxially grown silicon films on single crystal sapphire substrates, polished on both sides. Parameters of the diodes covered a range of junction widths, p^+ , n , and n^+ regions, and resistivities of the n -region. These are summarized in Table 1. The test diodes were mounted on the stage of a modified metallurgical microscope and illuminated from above. The illuminating source was an open electric arc (Xenon Corporation, Nanolamp) whose output pulses were of 20 ns duration and 50 kW peak intensity, with a broad-band spectrum, and repetition rate variable between 0 and 100 pps. The intensity was bright enough that direct microscopic observation and photography were possible without the need for an image intensification scheme such as that used by Sunshine. The broad band source eliminated problems encountered in monochromatic systems, arising from temperature dependent interference effects due to multiple internal reflections in the silicon film and the substrate.

Budenstein, Pontius, and Smith measured the temperature dependence of the transmittance of monochromatic and white light through thin 1.2 μm silicon films of different resistivities. The films were on 10 mil sapphire substrates, polished on both sides. A stainless steel test chamber, fitted at opposite ends with quartz windows and heated by a flow of dry nitrogen, was used for testing. A specimen wafer was mounted in the chamber parallel to the quartz windows, and the intensity of light from an incandescent source (with or without a monochromator) passing through the system was measured with a photomultiplier. The temperature of the film was monitored by a thermocouple in the

TABLE 1.--Silicon-on-sapphire diode geometries used by
Budenstein, Pontius, and Smith.¹⁸

<u>Large Diodes:</u> (Format 1, 21.5 mils wide, 30 diodes on each 0.5" square wafer)	
n-regions:	2 mils long, 21.5 mils wide, 0.9 μ m thick, resistivities 0.88, 0.46, 0.146, 0.064 ohm-cm.
n ⁺ -regions:	21.5 mils square, 0.75 μ m thick, 5 mils from edge of metallization to n-region.
p ⁺ -regions:	21.5 mils square, 0.75 μ m thick, 5 mils from edge of metallization to n-region.
<u>Large Diodes:</u> (Format 2, 21.5 mils wide, 100 diodes on large elliptical wafer)	
n-regions:	vary in length from zero to 1 mil, 21.5 mils wide.
n ⁺ -regions:	21.5 mils square. Contact is made only to the center 1/3 by etching away part of the oxide.
p ⁺ -regions:	21.5 mils square. Contact is made only to the center 1/3 by etching away part of the oxide.
<u>Small Diodes:</u> (4 mils wide, about 1500 diodes on each 0.5" square wafer)	
n-regions:	Lengths of 2 $\frac{1}{4}$, 1 $\frac{1}{2}$, 3/4, $\frac{1}{2}$, 3/8, $\frac{1}{4}$, 1/8, and 1/16 mils. 4 mils wide, 0.9 μ m thick, resistivities of 0.78, 0.39, 0.159, 0.067 ohm-cm in each length.
n ⁺ -regions:	4 mil squares extending only a few microns from the edge of the metallization. 0.75 μ m thick.
p ⁺ -regions:	4 mil squares extending only a few microns from the edge of the metallization. 0.75 μ m thick.

chamber. The white light transmittance was found to approximate a simple exponential function of temperature with slope almost independent of the doping density.

A photographic calibration was made by replacing the photomultiplier with film and making a sequence of exposures at different temperatures, maintaining a fixed exposure time. The contrast range of the film (Polaroid Type 107) was broken into 12 steps, covering an exposure ratio of 91:1 and the temperature range from 25 to 795 °C. Estimates of temperature on stroboscopic photographs were then made by comparison of darkening with the gray scale thus generated.

Temperature profiles across energized diodes on the microscope stage were also made using a photomultiplier to measure the transmitted light intensity over a small area, selected by an aperture in a mask on the image plane of the microscope. Scanning was accomplished by translating the stage, keeping the optical path constant.

A Barnes infrared microscope was used to substantiate the results of these measurement techniques.

In addition to studying the diode with transmitted light, the optical arrangement was used to observe the light emission during avalanche and current filamentation.

The results obtained by Budenstein, Pontius, and Smith follow.

- a. Second breakdown is associated with the growth of a broad high conductance filament across the high resistivity bulk region of the device, followed by the growth of a second narrow filament interior to the first that also bridges the high resistivity region.

- b. Filaments, under reverse bias, are most likely to nucleate in a device with a high current density at a point in the junction. They may, under special conditions, nucleate in the high resistivity region.
- c. Filaments can occur, with sufficient driving current, under forward bias and under reverse bias in junction devices. Filaments can occur in semiconductors in the absence of any junction.
- d. Nucleation of a filament does not cause damage to the device. Nucleation of a filament is accompanied by a subtle drop in device voltage when constant current testing is done. Thus, nucleation is not the second breakdown transition.
- e. Nucleation of a filament in a reverse biased junction occurs when a localized current channel causes a drop in the junction voltage to zero. This drop occurs when the local temperature produces a reverse saturation current density equal to the current density of the applied pulse. The junction internal field has not necessarily reduced to a low value when this condition is met. For conditions normally encountered, the reverse saturation current density is due mostly to minority carriers in the high resistivity side of the junction.
- f. Nucleation of a filament occurs at the same place on repeated pulse tests if the waveforms are identical and the system starts at the same temperature. Nucleation occurs at different points if the applied pulses are varied in amplitude or length. Thus, the major role in determining filament loca-

tions is due to the macroscopic system geometry, heat flow equation and electrical conduction equations.

- g. Upon nucleation of a filament at a point in the junction, current from neighboring regions funnels through the zero-voltage channel. The channel width grows to about $15\text{ }\mu\text{m}$ as the converging current causes further local heating. However, the converging current is accompanied by a spreading resistance which serves as a ballast. A potential gradient is produced along the current lines and, hence, along the junction. Thus the junction voltage changes from zero at the channel to the avalanche voltage about $50\text{ }\mu\text{m}$ away. The junction is non-conducting immediately outside the channel and remains non-conducting until the voltage rises to the avalanche voltage about $50\text{ }\mu\text{m}$ away. Thus, the junction adjacent to a channel is cool and emits no avalanche radiation.
- h. Multiple filaments can be formed in a reverse-biased junction. The higher the amplitude of the exciting current pulses, the greater the density of the filaments.
- i. For a given pulse duration, the number of filaments nucleated under reverse bias increases as amplitude increases, up to a maximum number. Thereafter, the added current density causes the filaments to grow into the high resistivity region. Growth occurs both in length and width as the material adjoining the filament rises in temperature above the maximum in the resistivity-temperature curve. A filament may attain a width of 25 to $75\text{ }\mu\text{m}$ under pulse testing and a temperature at its

center of about 1000 °C. During the growth period, there is an appreciable voltage drop. The growth time is typically greater than 10 μ s. This growth period is frequently defined as second breakdown. No damage occurs during filament growth.

- j. When a broad filament reaches all the way across the high resistivity region, a narrow melt channel grows through the center of the filament and the voltage drops abruptly to a lower value where it stabilizes and the filament stabilizes. The melt channel width, at current densities near threshold, is about 1 μ m. The transition time for growth of the melt channel is typically less than 1 μ s. Formation of a melt channel is the destructive form of second breakdown; it is always accompanied by device damage.
- k. If a current step of relatively low amplitude is applied and filamentation occurs, the system reaches a steady state wherein the filament is quite broad (width increases with decreasing resistivity of the high resistance region; widths of 100 to 150 μ m have been observed). Upon increasing the current amplitude, the filament broadens, gets hotter and the device voltage drops to a new stable value. This can be continued until the voltage falls to about 2/3 of its pre-transition value. With further increase in the current amplitude, massive melting, vaporization, and electrode damage occur. However, there is no second stage of filamentation.
- l. The "critical energy" of Schafft and French is related to that required to raise the temperature, in the presence of the de-

vice heat sink, of the high resistivity region to a value close to the maximum of the resistivity-temperature curve. It is then possible for a filament to grow rapidly across this region. The "delay time" is the time from the beginning of a current pulse to the start of the growth of the filament across the high resistivity region.

D. Non-Destructive Screening, Failure Thresholds, and Related Effects

Tasca et al.⁴⁰ have attempted to develop a non-destructive method for screening devices resistant to second breakdown from those more prone to second breakdown. The intent was to guard against reduced second breakdown resistance when a manufacturer makes small changes in fabrication procedures for a given device type. The authors regarded junction area and reverse bias depletion width as significant parameters. These, in turn, would influence junction capacitance, forward voltage drop, and avalanche voltage. Tests were conducted on 225 IN4148 planar epitaxial passivated diodes fabricated similarly except that three different junction diffusion windows were used: 3, 4.3, and 6 mil square. A correlation was found between the 100 nanosecond breakdown energy and the forward voltage at a forward current of 1 mA. The data presented show that more current is required to bring a device into second breakdown if the device's junction area is large, that is, current density is an important parameter. It is not clear that the method suggested would be useful if the manufacturer changed other aspects of device geometry besides the area. A second screening technique was to measure the energy required for the onset of the non-destructive form of second breakdown using a standard pulse length.

The authors did not give details of the test circuit used, but it probably was not with constant current pulses. Constant current testing, as emphasized by Sunshine, gives better control than does a circuit with constant external impedance.

Brown⁴¹ applied pulses in the range of 3 to 55 ns to high frequency transistors of known geometry in order to (1) determine the junction degradation produced as a function of pulse current, pulse power, and pulse duration; (2) develop a microscopic model for the degradation mechanism; and (3) suggest design modifications that would increase the tolerance of future devices to pulse degradation. The damage, regardless of the terminals used to excite the transistors, always appeared at the emitter-base junction. The apparent failure mechanism was the formation of conducting paths in parallel with the emitter-base junction, probably the result of localized junction melting during the application of a pulse. The author found that the current and power thresholds for damage exhibited power law dependences on the pulse length, a different exponential being required to describe each device. For eight different device types, pulse width dependences from $t_p^{-.17}$ to $t_p^{-.56}$ were obtained for the current at failure, while dependences from $t_p^{-.32}$ to $t_p^{-.84}$ were obtained for the power at failure. No perspective on the pulse length dependence could be given. However, the delay time studies described by Budenstein *et al.*^{17,19} show that the pattern of current filamentation at the threshold of second breakdown is a function of pulse length. They conclude that the filamentation pattern depends strongly upon device geometry, including dynamic thermal characteristics. Brown concludes that the devices most

resistant to second breakdown were those with the largest emitter peripheries and deep emitter diffusions. Experiments were also done on annealing of damage by placing devices in an oven (300 °C for one hour) or by sending currents through the devices in a variety of arrangements (15 minutes). The transistor gain was monitored before pulsing, after damage, and after annealing. Each of the annealing procedures caused some improvement, but the one with the highest currents caused the greatest improvement. The amount of recovery varied with the device. No mechanism for annealing was suggested.

Wunsch and Bell⁴² have developed a model for determining the threshold failure levels of semiconductor devices subjected to electrical pulses with durations of 0.1 to 20 μ s. This model uses linear heat flow theory and the thermal characteristics of the semiconductor to relate threshold power density to delay time. Failure is assumed to occur when the temperature reaches the melting point of the semiconductor material. Average power per unit area and delay time are related by the equation

$$P/A = (\pi k \rho C_p)^{1/2} (T_m - T_i) t_p^{-1/2} \quad (2.1)$$

where

P = Power

A = Junction area

k = Thermal conductivity

t_p = Delay Time

ρ = Density

C_p = Specific heat

T_m = Failure temperature

T_i = Initial temperature

Approximations such as constant thermal conductivity, specific heat, and density are used in the Wunsch-Bell model. The model was applied to experimental results from over 1200 devices of approximately 80 different types. A best-fit to the experimental results gave the semi-empirical relation $P/A = 480t_p^{-1/2}$, where, for t_p in microseconds, P/A is kW/cm^2 . Actual failures on all types of devices tested were within one order of magnitude of Eq. 2.1, and even closer to the semi-empirical relation. Although more exact thermal models exist for special conditions, the Wunsch-Bell model is useful for making quick, order of magnitude estimates of failure thresholds for a wide variety of silicon diodes and transistors.

Budenstein, Pontius, and Smith^{18,20} have described the melt transition in terms of a single heat-transfer coefficient characteristic of the device type. As the melt filament grows, the voltage across the filament (and the device) falls. The threshold current for filamentation varies as $(\rho^{-3/4})$, where ρ is the resistivity of the high-resistance region. Experimental data were presented in support of the model.

E. Scope of the Present Experimentation

Chapter III contains a description of the experimental methods used in this study. Chapter IV describes and characterizes the test specimens. Chapter V presents the experimental results. Chapter VII presents conclusions based on experimental results, and Chapter XIII discusses implications of the experimental results on device screening techniques.

III. EXPERIMENTAL METHODS

The stroboscopic method for observing dynamic temperature distributions in planar silicon-on-sapphire devices was developed by Sunshine^{5,17} and employed in this study as refined by Budenstein, Pontius, and Smith.¹⁸⁻²² A silicon-on-sapphire diode subjected to repetitive electrical pulses is illuminated by a pulsed arc lamp synchronized with the electrical pulses and viewed microscopically. Heating patterns are visible because the optical transmittance of a thin silicon film decreases as temperature increases. Since the silicon becomes less transparent as it gets hotter, dark or opaque areas indicate heating and localization of current.

Figure 2 shows a block diagram of the experimental apparatus used to study diodes under electrical stress. The silicon-on-sapphire wafer containing the test diode is mounted on the stage of an inverted optical microscope (Reichart Research Metallograph "MeF 2X") with probes contacting the diode terminals. An electrical pulse is applied with either a constant current generator or a constant impedance generator. The constant current generator uses a Hewlett-Packard Model 214A pulse generator and either a high voltage transistor (TRS 6006), or a beam power tetrode (4CX350A). The constant impedance generator is a Velonex Model 380 high power pulse generator.

A trigger signal from the pulse generator determines the firing time of the arc lamp (usually Xenon Corp. Model 787B) relative to the

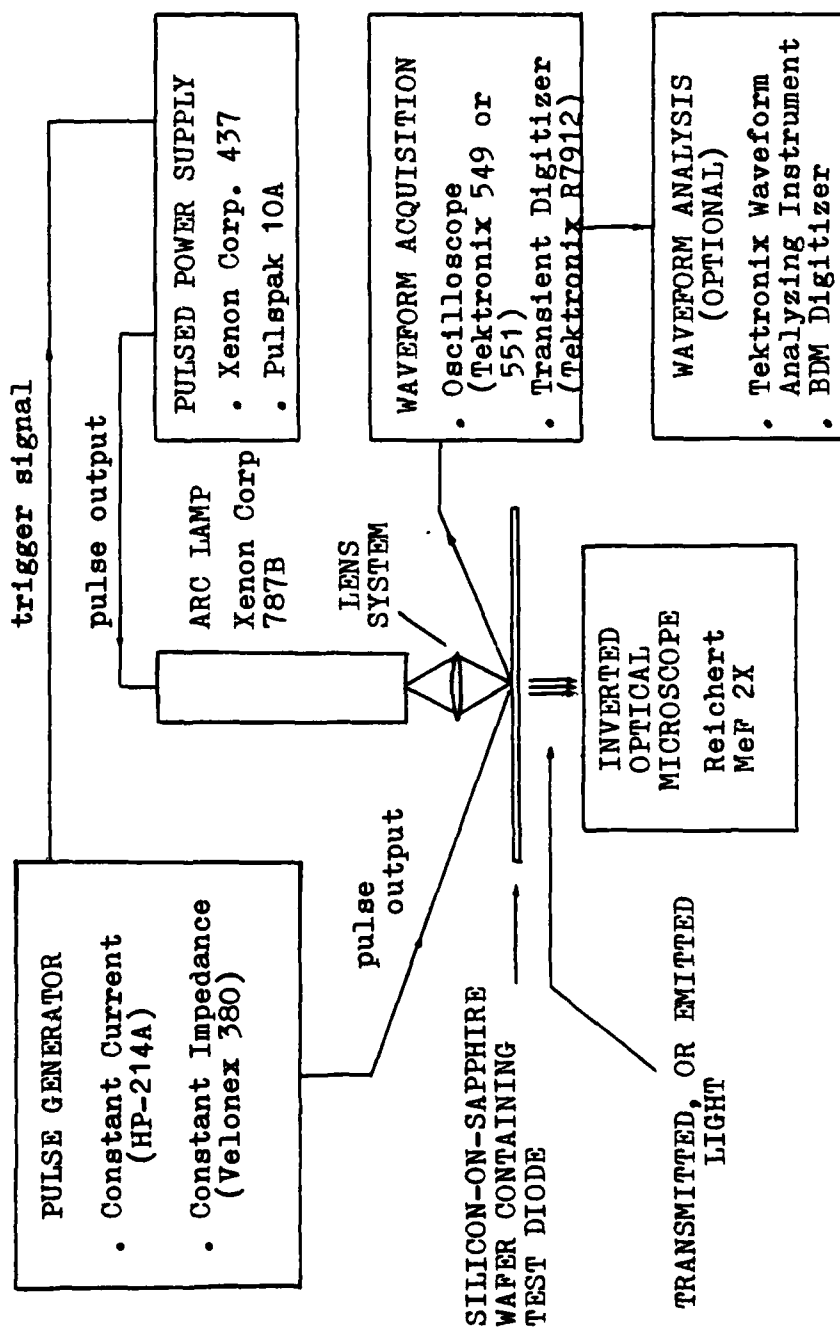


Fig. 2. Block diagram of the apparatus used for studying silicon-on-sapphire diodes.

electrical pulse. The power supply of the arc lamp was a Xenon Corp. Model 437 Nanopulser or a Pulspak 10A pulse generator. Light from the arc lamp is focussed onto the diode through a high quality lens system. The transmitted light is then observed or photographed microscopically. The microscope was also used to investigate light emission from the diode under reverse bias.

The current and voltage waveforms were acquired with an oscilloscope (Tektronix Type 549 or 551) or a transient digitizer (Tektronix R7912). The waveforms were recorded photographically from the oscilloscope, and on floppy disks from the transient digitizer. Hard copies could be made of the waveforms stored on floppy disks. The photographically recorded waveforms were digitized and mathematically processed for about 250 diodes. R. Turfler of the BDM Corporation performed the digitizing and processing. The waveforms stored on floppy disks were analyzed with additional waveform processing equipment from Tektronix.

A Tektronix Type 576 curve tracer (not shown) was used to electrically characterize the diodes. The various components in the block diagram of Fig. 2 will now be discussed in more detail.

A. Stroboscopic Method

A diagram of a silicon-on-sapphire diode on the stage of the Reichert Research Metallograph is shown in Fig. 3. The contact probes are Wentworth Laboratories Model PR-0160 or Model PR-0191. A low power, long working distance stereomicroscope was located above the stage and used to position the probes. The probes have magnetic bases which are firmly held to a steel plate mounted on the microscope stage. The

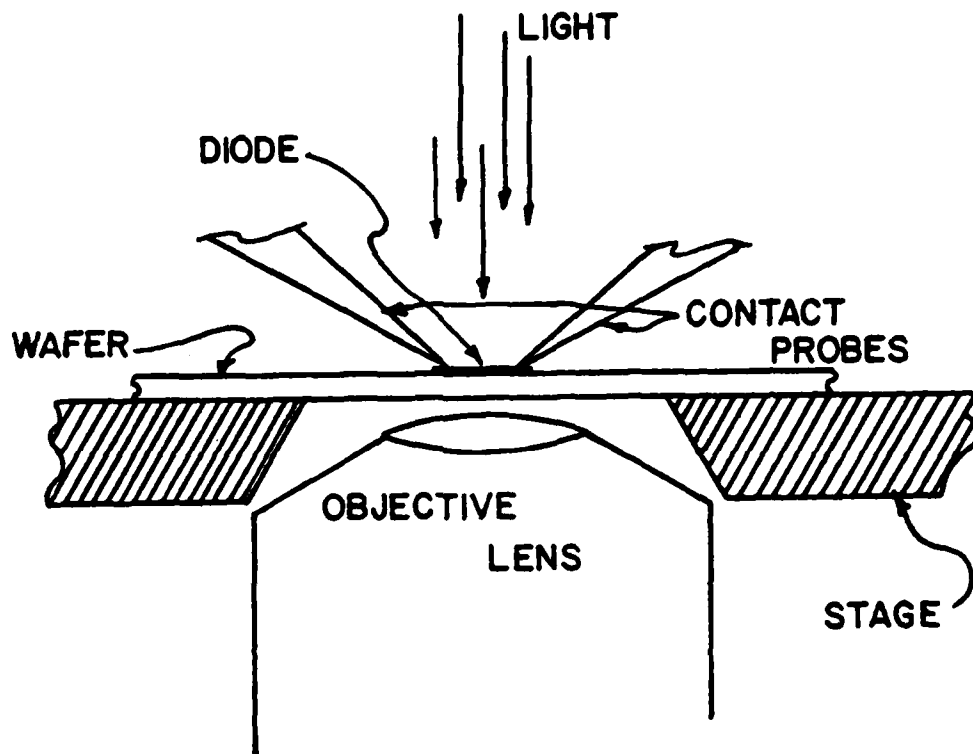


Fig. 3. A silicon-on-sapphire diode in position for observation of second breakdown phenomena. The wafers, probes, and stage are moved as a unit to select the area of observation.

stage could be moved relative to the objective lens by two micrometer adjustments.

The arc lamp was focussed on the wafer surface by a lens and the Reichert condenser lens system. The lamp's intensity of 50,000 W in the visible range is sufficient that no image intensification is required for direct microscope observation. The duration of the Model 787B arc lamp is 20 ns, much shorter than the pulses used to electrically stress the diodes in this study. The experiments were performed at a pulse repetition rate between 10 and 100 per second.

The arc lamp does not fire at exactly the same voltage every pulse, so there is a small amount of jitter relative to the trigger pulse. The amplitude of the jitter depends on the pulse risetime of the arc lamp power supply. The power supply used for most of the tests (Xenon Corp. Model 437) introduced a jitter with a maximum amplitude of about 1 μ s. The Pulsar Associates, Inc. Pulspak 10A had the capability to fire the nanolamp with less than 10 ns jitter. However, most electrical tests were done with pulses 10 μ s in length and jitter was not a problem. The Model 437 could be pulsed at a repetition rate of up to 100 per second whereas the Pulspak 10A allowed a maximum rate of only 10 per second. The convenience of a faster repetition rate was the primary reason for using the Model 437. In addition, some circuit problems occurred with the Pulspak 10A due to the low impedance of the arc lamp, making it unavailable while it was being repaired by the manufacturer.

An important concern is whether the heating pattern changes from one pulse to the next. In general, this does not happen; the temporal

and spatial heating pattern is highly reproducible for a particular diode and pulse condition, as long as the pulse amplitude is kept below the damage threshold.

Another concern is the time for the diode to cool after the pulse ends. Stroboscopic observations obtained by positioning the strobe light after the end of each electrical exciting pulse show that the thermal time constant for diodes 0.4 μm thick is about 1 μs . The pulse repetition rates were low enough that the time between pulses (greater than $10^4 \mu\text{s}$) was long compared to 1 μs .

The heating patterns were photographed on Polaroid Type 667 film, which has an ASA speed rating of 3000. For proper exposure of the film, the integrated transmitted light from 50 to 500 pulses was needed to record a single heating pattern. The number of pulses necessary for an exposure depended on the age of the arc lamp; the light intensity gradually decreased over its lifetime. Visual observations of single pulse heating patterns show no discernable differences from the integrated pulse photographs.

B. Circuit Considerations

Both constant current pulses and voltage pulses were used to study filamentation patterns and breakdown thresholds. Constant current pulses were generated with a high voltage transistor (TRS 6006) or a beam power tetrode (4CX350A). A Hewlett-Packard 214A pulse generator controlled both the transistor and the tetrode. The transistor provided for device voltages up to about 600 V, and the tetrode circuit voltages to 1000 V. Voltage pulses were obtained with a Velonex Model

380 pulse generator. Pulses of approximately 1000 V could be applied to high impedance loads.

Figure 4 shows the constant current circuit with the high voltage transistor. The upper part of the figure shows the circuit configuration for obtaining current waveforms, and the lower part the circuit for voltage waveforms. A three-pole, two position switch was used to change the circuit from current to voltage waveform acquisition; this switch is not shown because it complicates the circuit diagram. The only difference between the two configurations is that the positions of the diode and the 1 k Ω current-measuring resistor have been interchanged, keeping the same polarity on the diode. Interchanging the two components has no effect on the diode waveform characteristics.

The HP-214A pulse generator provides a variable width rectangular pulse which is used to forward bias the emitter-base terminals of the high voltage transistor. The 214A also provides a trigger pulse whose position in time relative to the leading edge of the rectangular voltage pulse can be continuously delayed or advanced up to 10 ms. The trigger output determines the time at which the arc lamp is fired. However, the 214A trigger pulse is inadequate to actuate the trigger input of the Model 437 arc lamp power supply, so the 214A trigger excited a GR Model 1217B pulse generator which provided the required arc lamp trigger pulse. Because of the throughput time of the Model 437, the trigger pulse had to be applied before the 10 μ s exciting pulse applied to the diode.

The waveform acquisition instrument was either a transient digitizer, which is described in Section III.C., or a Tektronix Type 549 or

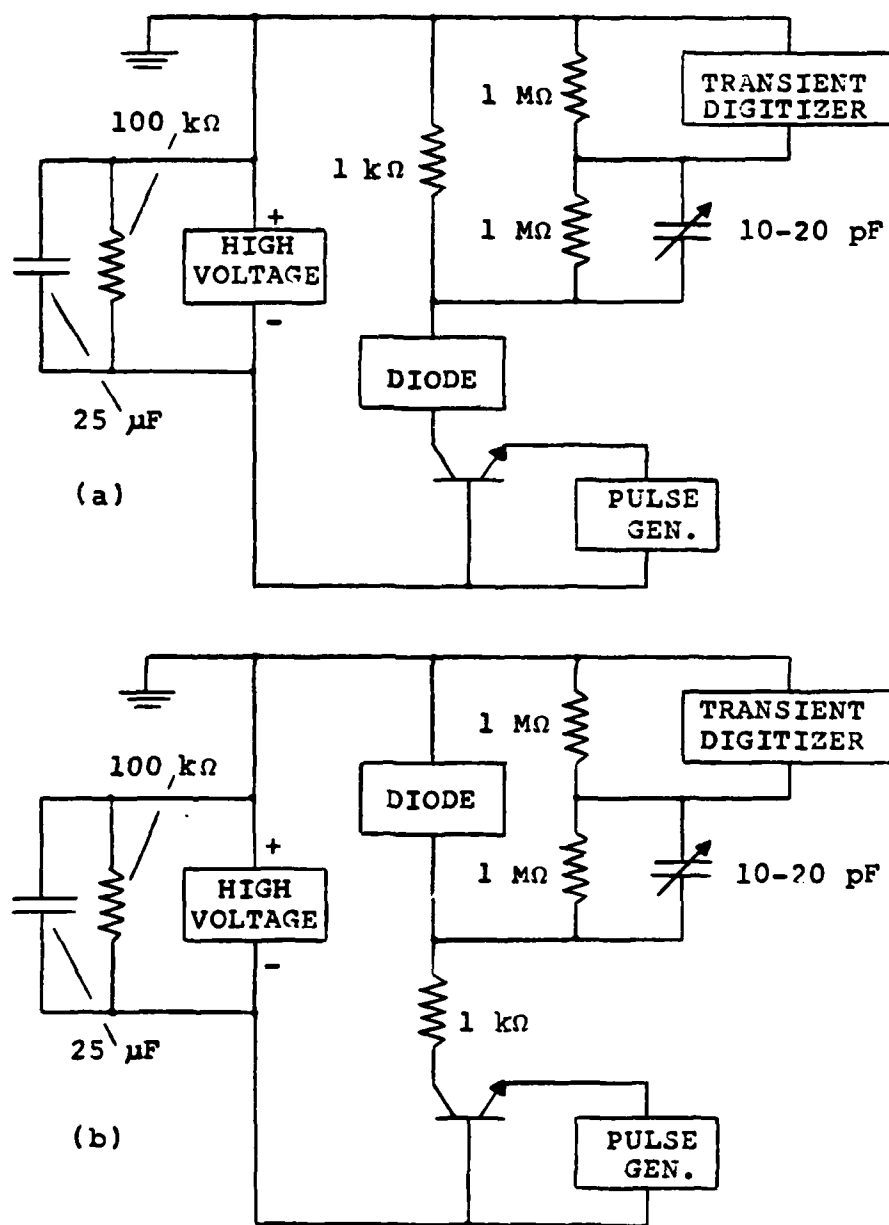


Fig. 4. Constant current circuit. (a) Circuit configuration to observe the current waveform. (b) Circuit configuration to observe the voltage waveform.

551 oscilloscope. It was necessary to keep the transient digitizer and its associated components well grounded. This meant that the HP-214A pulse generator had to be "floated" using an isolation transformer. It was placed in a lucite and fiberboard box with lucite and teflon extenders on the knobs. The trigger signal was isolated by two capacitors.

The high voltage supply (Fluke Model 407D) is connected across the series combination of current-measuring resistor, diode, and transistor. A large capacitor and bleeding resistor (100 k Ω) are parallel with the high voltage supply to eliminate voltage fluctuations.

The transient digitizer was coupled to the circuit by a X10 attenuation probe. However, this attenuation was not sufficient for the highest amplitude waveforms, so a voltage divider is included in the circuit. The voltage divider consists of the two 1 M Ω resistors and a variable trimmer capacitor of 10-20 pF. The trimmer capacitor is necessary to compensate for the input capacitance of the oscilloscope probe. The exact value of the voltage divider was determined from the calibrated reference voltages of one of the oscilloscopes.

The diode is physically connected to the circuit by two coaxial cables which attach to the Wentworth Laboratories Model PR-0191 probes. These cables serve to reduce electrical noise but they also introduce undesirable capacitance, about 100 pF each. This and other stray capacitance cause severe risetime problems if the diode impedance is too high. A slightly modified circuit, described in Section III.F., was used to study high impedance diodes.

The actual firing time of the arc lamp relative to the diagnostic waveforms was established by a small amount of electrical noise from the lamp which appeared on the waveforms.

For higher voltage or higher power, the tetrode circuit shown in Fig. 5 was used. The characteristics of the 4CX350A beam power tetrode indicate that output plate current is nearly constant when the plate voltage is in the 600 - 1500 V range, with a constant screen voltage of 400 V, and with a constant grid bias voltage. The plate current increases from 0 to 1.2 A as the grid bias changes from -45 to 0 V.

The operation of the tetrode and transistor circuits is very similar. The main differences are those which are necessary to accommodate the tetrode circuit requirements; these differences are described below.

The 400 V screen bias is obtained from a voltage divider consisting of the 1.8 M Ω and the 1.2 M Ω resistors. A 1 μ F capacitor is placed in parallel with the 1.2 M Ω resistor to absorb voltage fluctuations. A constant 1000 V is maintained on the high voltage supply (Fluke Model 412B). The 68 k Ω resistor in series with the high voltage supply limits the initial capacitor charging current to less than 30 mA. Grid bias is provided by the combination of the 67 1/2 V battery and the HP-214A pulse generator.

As mentioned previously, voltage pulses were obtained with a Velonex Model 380 high power pulse generator. These pulses were of constant amplitude only for high impedance diodes. The pulse amplitude depends on load impedance, and the diode impedance usually changes during the pulse. Since the Velonex pulser did not have a delayed trigger

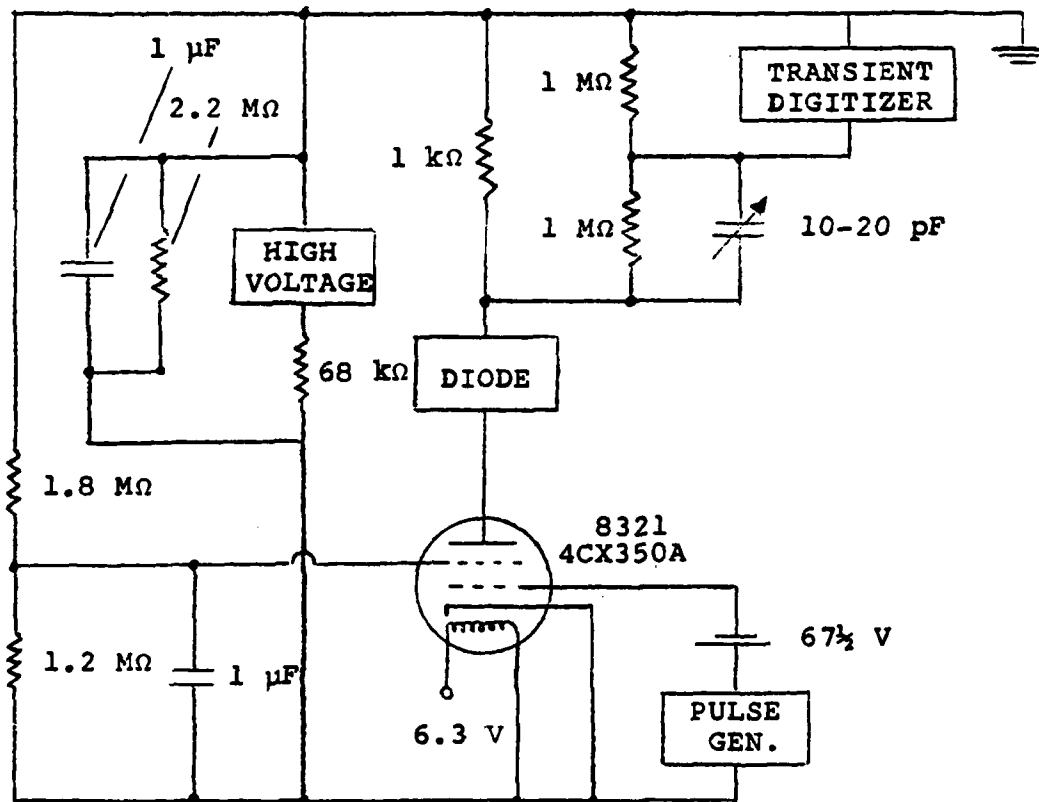


Fig. 5. Constant current circuit using beam power tetrode.

signal, the HP-214A was used to control the trigger inputs of both the arc lamp power supply and the Velonex pulser.

C. Transient Digitizer, Waveform Analysis

During a portion of this study, a Tektronix Digital Waveform Instrument was available. This instrument is ideally suited for recording and processing single-shot events on the time scale of interest in these experiments. It can accept multiple input signals, requiring one R7912 transient digitizer for each signal. The system, more specifically,

1. records the incident pulse in digital form (sampling the pulse 512 times in a single pulse for pulses as short as 5 ns and as long as 1000 μ s.
2. displays the incident pulse on a monitor
3. stores the digital record of the pulse
4. processes the incident pulse as directed (differentiation, Fourier analysis, etc.)
5. displays the output of the central processing unit on a graphics display terminal
6. provides a hard copy of the information displayed on the graphics display terminal

The waveform analyzing instrument consisted of an R7912 transient digitizer to receive and store the incoming waveform, a 632 video monitor to display the waveform, a 4165 controller to analyze the waveform, a 4010 graphics terminal to display processed waveforms and to input instructions, and a hard copy unit to obtain copies of information displayed on the graphics terminal.

The transient digitizer contains the controls which govern the display of the incoming waveform. These controls include vertical and horizontal scale factors, method of triggering, trace intensity, focus, and z-axis modulation. The waveform is stored on a specially-designed tube in the transient digitizer, called a scan converter tube, which contains a matrix of silicon diodes on an single chip. The chip is 1.3 by 0.95 cm with a density of about 800 diodes per linear centimeter. On one side of the chip is a reading gun and on the opposite side is a writing gun. The diodes are either in an uncharged or a charged condition, corresponding to the written or unwritten state, respectively. The charge condition may be changed by the writing beam, which is modulated by the incoming waveform. Thus, waveform information may be stored on the diode array in the form of charged and uncharged diodes, that is, in digital form. This information may then be stored in the 4165 controller memory and on a floppy disk. Because of the finite width of the trace, there will usually be two vertical points for each horizontal point, corresponding to the upper and lower edges of the trace. After storage in controller memory, the waveform may be operated on by "TEK SPS BASIC" functions. TEK SPS BASIC is a modified BASIC language which includes special functions to communicate with the transient digitizer, display graphics data, and process string functions. The waveform, tables, comments, and other information may be displayed on the graphics terminal. This graphics display may then be hard-copied.

A general purpose program was written which would acquire the necessary waveforms, assign a file name to the waveform, and store the

waveform on a floppy disk. The program contains two subroutines. The first acquires correction data to adjust the waveform for defective diodes in the scan converter tube and for geometric distortion effects. The second performs the data corrections. The first subroutine searches the scan converter tube for defective diodes and identifies these diodes in a special array. Then a dot graticule is displayed on the video monitor and digitized into controller memory. The digitized dot graticule is compared to the instrument's internally generated electronic dot graticule and tables of horizontal and vertical constants are prepared to correct the waveform for electron beam distortion. Next the first subroutine acquires a zero-reference trace, that is, a trace with the input grounded. Then it returns control to the main program. The second subroutine rejects defective data, finds the best average of the upper and lower edges of the trace, interpolates missing data when necessary, performs the geometry correction, and uses the zero-reference trace to adjust the waveform amplitude.

The main program was designed to acquire current and voltage waveforms, assign them file names, and store them on floppy disks under the given file names. Comments and other data were also stored with the waveforms. The file name was designed so that it uniquely identified a particular diode.

Several other programs were also used. One was written to take two waveforms, compute their derivatives, their product, and the derivative of the product. If the original waveforms are current and voltage versus time, then the program will compute the derivatives of current and voltage versus time, power versus time, and the derivative of

power versus time. Taking the derivative of an experimental waveform is somewhat difficult because of random noise. Some sort of averaging process is necessary, so the derivatives have poorer resolution than the originals.

D. Typical Test Sequence

In order to investigate diode behavior near the second breakdown threshold, a series of tests correlating waveform shape and n-region heating were performed. A typical test sequence began by verifying that the diode I-V curve was normal. Then the diode was photographed with no current flowing through it; this is referred to as a "zero bias" photograph. Next, the diode was electrically stressed using constant current or constant impedance pulses at a repetition rate between 10 and 100 per second. Initially, the pulse amplitude was set well below the second breakdown threshold. The n-region heating was observed stroboscopically by firing the arc lamp at the end of the pulse. Then the pulse amplitude was increased very gradually, carefully observing any changes in the n-region heating pattern and the shape of the voltage waveform. Both the n-region heating pattern and the voltage waveform were useful in estimating nearness to second breakdown. Hot spots on the p^+n junction and a drop in voltage near the end of the voltage waveform are indications that the diode is on the verge of second breakdown.

When the diode was judged to be as near as possible to destructive second breakdown (melt formation), current and voltage waveforms were taken with either the transient digitizer or an oscilloscope, and a

photograph was taken of the n-region heating pattern. In many cases, diode behavior was interesting enough to require a number of heating pattern photographs, taken at different times during the pulse and at different current levels.

In a few cases, the photographic arrangement of the stroboscopic setup was used to record light emission from reverse biased diodes. The integrated intensity of each pulse is obtained since no shutter was available to stroboscopically examine the emitted light. Normally, it is necessary to integrate over a large number of $10\ \mu\text{s}$ pulses to obtain good photographs (typically several million for diodes with the highest n-region doping level).

The waveforms and other relevant information were recorded on hardcopies and floppy disks with the transient digitizer. Polaroid film was used to record waveforms taken with an oscilloscope. Diodes were tested under forward and reverse bias.

E. Energy Threshold Measurements

Two energies are of interest in determining the total energy input to the diode to bring it to the threshold of second breakdown: the energy input during the maximum amplitude non-destructive pulse, and the energy input necessary to cause failure during the destructive pulse. It was originally thought that two transient digitizers would be available for energy threshold analysis. Unfortunately, the second transient digitizer did not arrive while the digital waveform instrument was on loan to Auburn University. Thus, the Tektronix waveform system could not record two waveforms simultaneously, so much of the useful-

ness of this instrument associated with its ability to perform mathematical manipulation of waveforms was lost. Fortunately, simultaneous voltage and current waveforms could be recorded on film (Polaroid Type 667) using a Tektronix Type 551 dual beam oscilloscope. Zerox copies of the waveform photographs, and related data were sent to R. Turfler of the BDM Corporation for digitizing and computer analysis. The BDM Corporation has developed a data base on impulse damage to many types of devices. The present experiments add to this base, providing data on well-characterized devices. The digitized waveforms and the data computed from them were then analyzed at Auburn.

The constant current circuit described previously could not be used for energy threshold tests on high impedance diodes because pulse risetimes were too long. When a $10\text{ k}\Omega$ resistor was substituted for the diode, the pulse risetime was about $1\text{ }\mu\text{s}$. However, many diodes of interest had impedances much higher than $10\text{ k}\Omega$, with correspondingly increased risetimes. Thus, it was necessary to make circuit modifications.

Figure 6 shows a constant current circuit utilizing a high voltage transistor which has improved risetime characteristics. The circuit operates in basically the same manner as the constant current circuit in Fig. 4. However, there are several significant differences. The diode probes used in the previous circuit were replaced by Wentworth Laboratories, Inc. Model PR-0160 probes, which do not have coaxial cable attachments. In addition, the HP-214A is grounded in this circuit. Both of these changes resulted in pulse risetime improvements by decreasing the stray capacitance of the circuit. Two circuit improve-

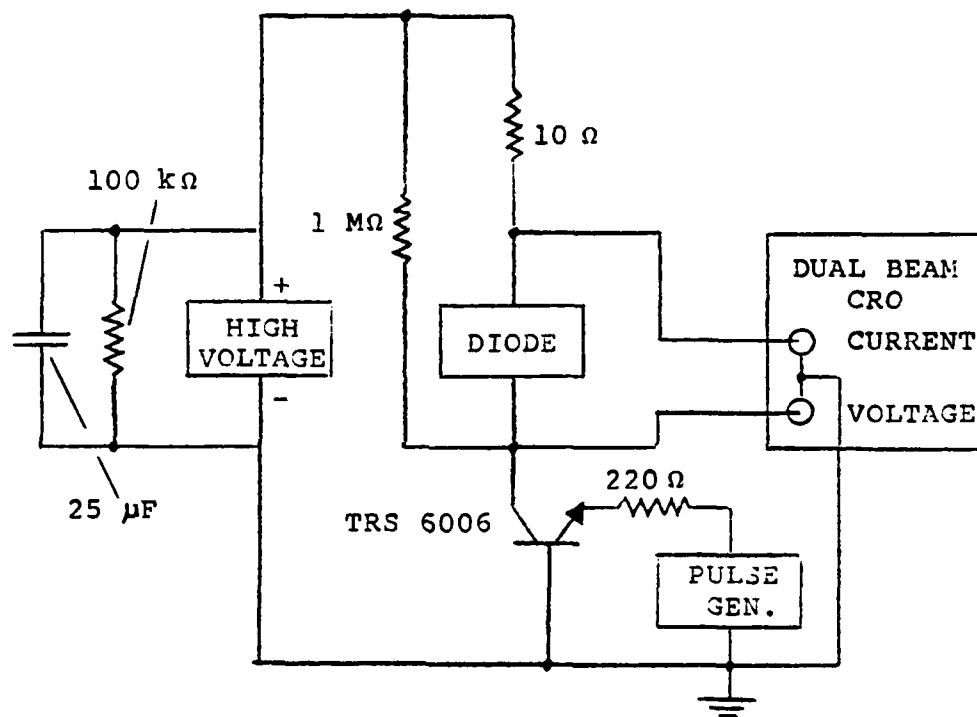


Fig. 6. Constant current circuit. This circuit was used to obtain faster pulse risetimes.

ments were suggested by R. Turfler: the $220\ \Omega$ emitter resistor stabilizes collector current, and the $1\ \text{M}\Omega$ resistor establishes a definite collector bias voltage (when the diode is reverse biased below its avalanche breakdown voltage) through the reverse saturation current of the collector base junction.

Both the current and voltage waveforms were measured relative to the plus side of the high voltage supply, using the "AC ONLY" inputs of the dual beam oscilloscope. The voltage across the $10\ \Omega$ current-measuring resistor is small compared to the diode voltage, so there is no significant error in the voltage waveform.

A typical energy threshold test sequence begins with a reverse bias I-V curve of the test diode, using a Tektronix Type 576 curve tracer. If the diode has a normal I-V curve, then a single constant current pulse having an amplitude less than the failure threshold is applied to the reverse biased diode and the waveforms photographed. The I-V curve is checked to determine if any change has occurred. Then another constant current pulse at a slightly higher amplitude is applied to the diode. In some cases, photographs of the diode heating patterns were also taken. A calibrated dial indicating current amplitude was attached to the HP-214A pulse generator; this dial was an invaluable aid in determining the appropriate pre-failure current level. An I-V curve was also made after the diode had been damaged. Approximately 250 diodes were included in the energy threshold tests.

F. Voltage Threshold Measurements and Damage Morphology

A series of experiments were performed to determine how diode geometry and doping level influence voltage failure thresholds, and the location of the melt filament which forms during the second breakdown transition. A group of diodes from each of the five nominal doping levels were tested with 10 μ s pulses obtained from the Velonex Model 380 pulse generator. The diodes were reverse biased and the pulses were applied to the series combination of the diode and a 1 k Ω resistor; the resistor was necessary to limit damage. Single pulses of increasing amplitude were applied to the diode until second breakdown occurred. The peak voltage during the failure pulse and the endpoints of the melt filament were recorded. Approximately 1500 diodes were included in these tests.

G. Waveform Surfaces

A series of voltage waveforms was obtained from the same diode for a sequence of constant current pulses of increasing amplitude. The current waveforms were also obtained, but only the average value of the current during the pulse was recorded. The motivation was to find any subtle changes of waveform that could be correlated with filamentation phenomena or other features of the second breakdown process. Since current is constant during a given voltage waveform, the data were plotted using the Tektronix waveform instrument as a three-dimensional current-voltage-time surface.

H. Device Characterization

Two methods were used to characterize the diodes in this study: measurements of resistivity, and of reverse bias breakdown voltage. The doping level test structure, a silicon $n^+ - n - n^+$ film with rectangular geometry, was used to calculate resistivity (and to evaluate the uniformity of processing over a wafer surface). The electrical resistance of these structures was measured on each of the dies of several wafers, and plots were made of resistance versus position on the wafer surface. Most of these measurements were made at a dc bias of 5 V; current was measured with a Simpson Model 260 meter. Other dc and curve tracer measurements verified that current was linearly related to voltage in the range in which the measurements were made, and that resistance was not polarity sensitive. The reverse bias breakdown voltages of the diodes were measured with a Tektronix Type 576 curve tracer at a current of 10 μA .

IV. DESCRIPTION OF SPECIMENS

A. Fabrication Procedure

The devices tested in the present study were $p^+n\text{-}n^+$ diodes fabricated in silicon-on-sapphire wafers at the Electronics Research Center of Rockwell International. The starting wafers were obtained from the Union Carbide Corporation with an epitaxial silicon layer of $0.6\text{ }\mu\text{m}$ and n -type doping level of about 10^{14} cm^{-3} . All of the sapphire wafers were sliced from a single boule and polished on both sides. Fabrication began with doping of the n -regions to the desired levels by phosphorous ion implantation. Figure 7 shows part of the processing procedure. However, only steps A-E apply to the fabrication of diodes. During each ion implantation a 1 cm^2 square of the starting wafer was prepared in addition to the test wafer. This square serves as a calibration reference for the stroboscopic experiments. The wafers were processed in two batches, with five wafers to a batch. Each batch was intended to contain one wafer with n -region doping levels of 10^{14} , 10^{15} , 10^{16} , 10^{17} , and $5 \times 10^{17}\text{ cm}^{-3}$. Actual doping levels were measured as discussed later.

The die size for the test array of diodes is 0.430 cm by 0.521 cm . Each die contains 213 test diodes and about 70 dice are on each wafer. The two batches contain a total of about 150,000 diodes. A test array on each die is designed to provide material parameters for the devices.

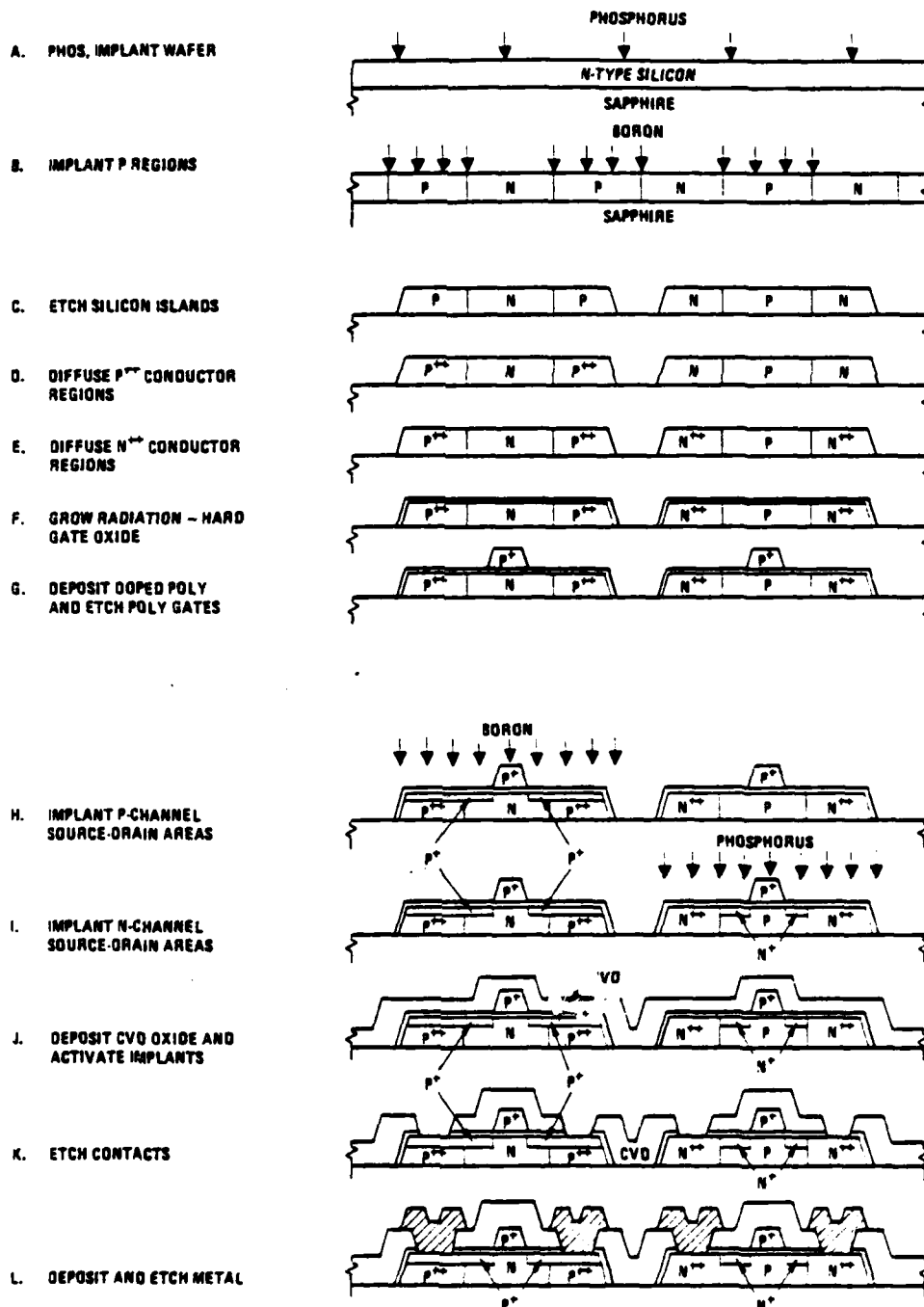


Fig. 7. Fabrication procedure (after Green, Ref. 43).

There were two accidents during the fabrication procedure. A mask error in the first batch left the terminals open-circuited in one type of device, the type intended for measuring the n-region doping level. This error was corrected in the second batch. The second accident occurred when the wafer in the second batch of targeted doping density 10^{16} cm^{-3} shattered during a furnace pull.

The layout of the wafers is shown in Fig. 8a. The blank rectangle, called the "drop out," is used to label the wafer and to locate a particular die. A portion of each wafer was sliced off and retained by Rockwell International as a reference. Figure 8b shows a reflected light photograph of a single die, magnified about 20 times. The various structure types on the die are discussed in Section B.

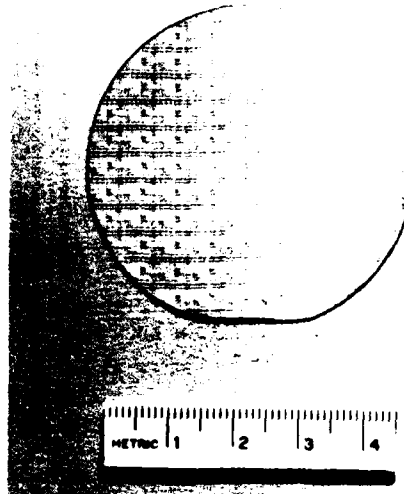
B. Device Structures

Each die included fourteen different structure types. Eleven of these were test arrays, with individual arrays containing up to 51 diodes. The three other structure types consisted of a processing test group, special Rockwell devices, and a test structure for measuring the n-region resistivity. Figure 9 shows the die and individual device numbering schemes. A description of the structure types is given below. Figure 10 shows the positions of the structure types on the die.

1. Standard Reference Structure

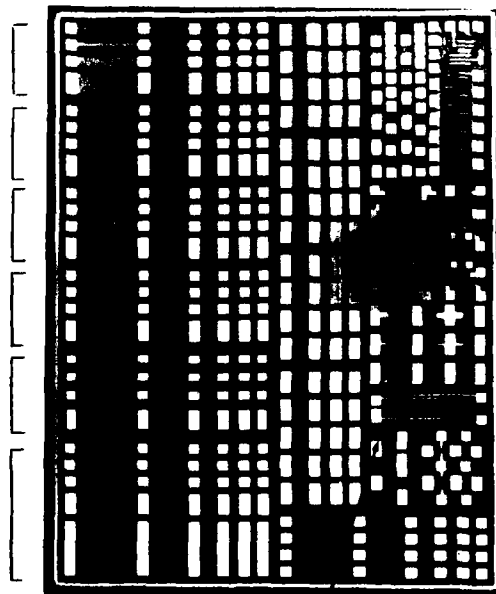
Figure 11 shows the configurations of the 25 diodes of the "standard reference" structure. The rectangular areas which contain large x's represent aluminum contact areas. Diode dimensions included widths of 30, 50, 100, 200, and 500 μm and n-region lengths (spacings between

(a)



(b)

(14) MULTIPLE SPIKES

(06) N^+N
SPIKES(05) P^+N
SPIKES(04) METAL- P^+
SPIKES(03) METAL- N^+
SPIKES(02) ENCLOSED
REFERENCE(01) STANDARD
REFERENCE

(09) DOPING LEVEL TEST STRUCTURE

(13)
ROCKWELL
DEVICES(12)
PROCESSING
TEST PATTERN(11) RADIUS
OF CURVATURE(10) INTER-
DIGITATED(08) FOUR
TERMINAL(07) HALF-
SIZE SPIKES

Fig. 8. Wafer and die layout. (a) Silicon-on-sapphire wafer. (b) Single die.

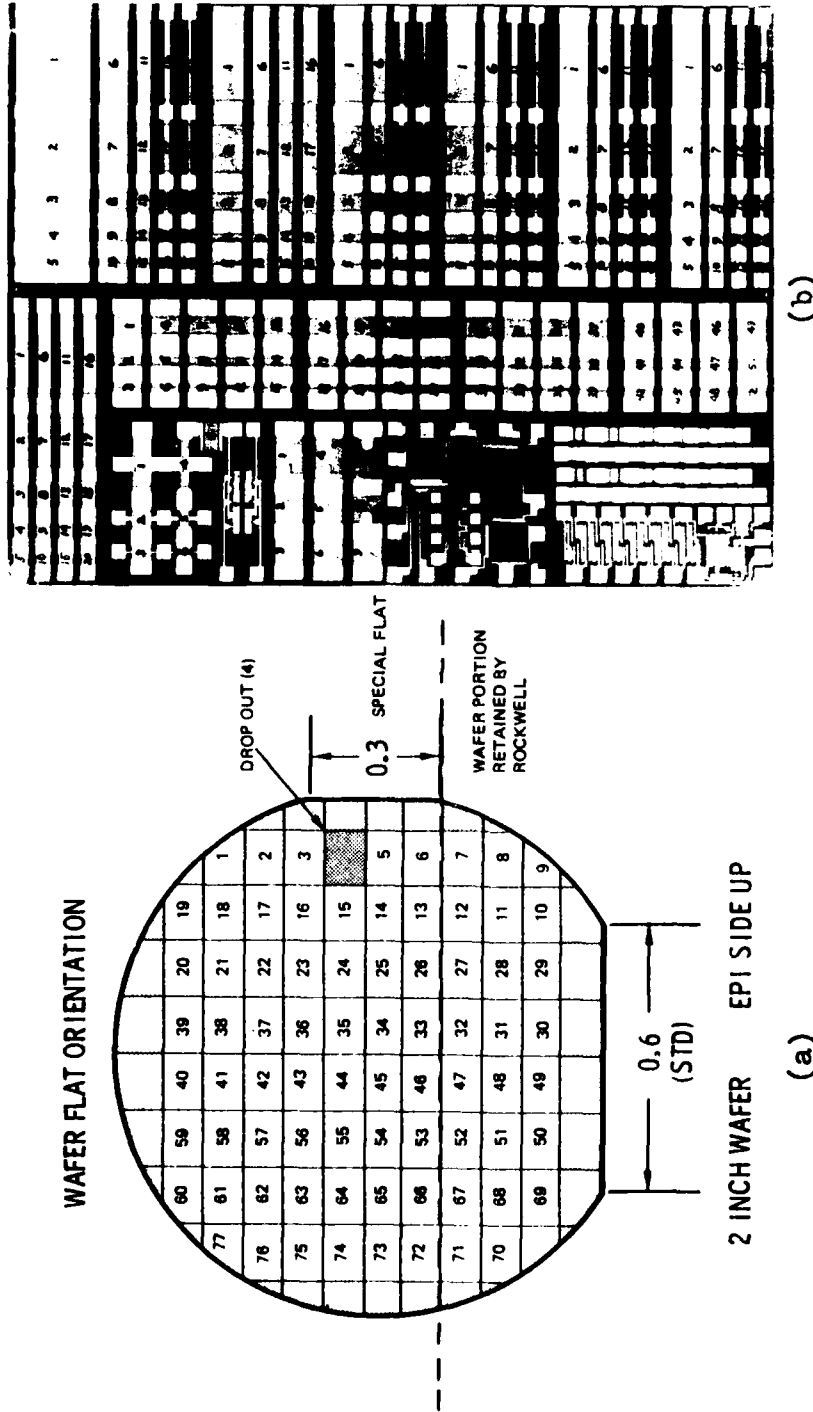


Fig. 9. Die and individual device identification. (a) Die numbering scheme. (b) Individual device numbering scheme.

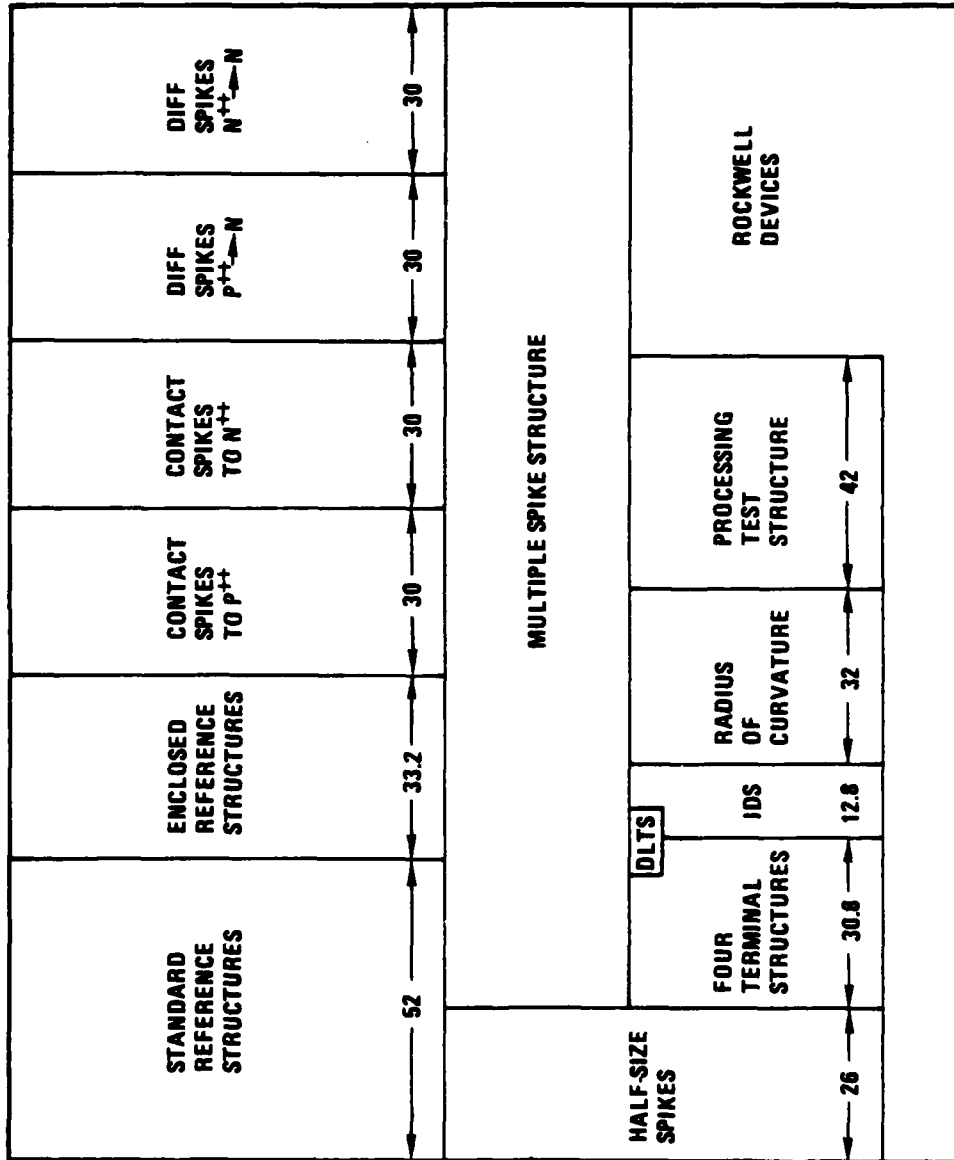


Fig. 10. Die layout. All dimensions are in mils.

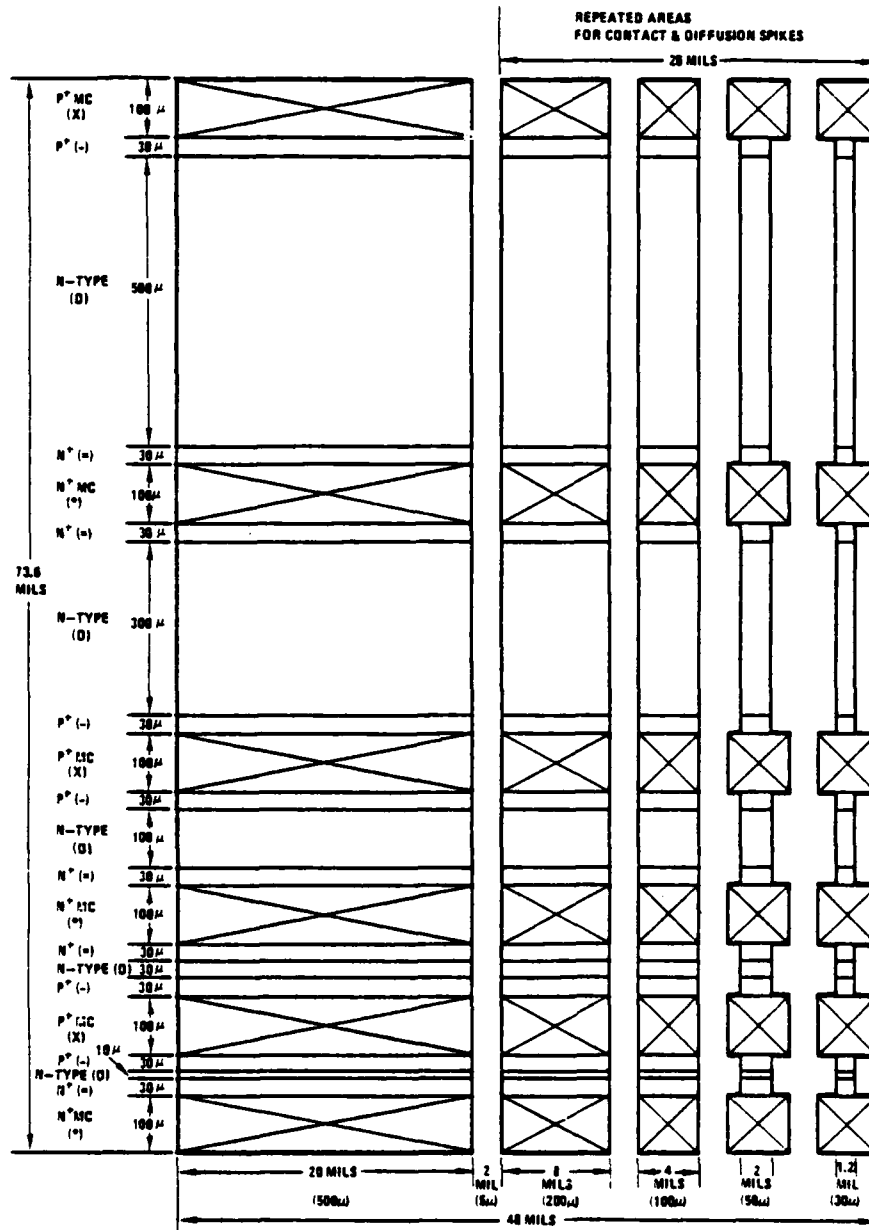


Fig. 11. Standard reference structure (after Green, Ref. 43).

the p^+n and n^+n junctions) of 10, 30, 100, 300, and 500 μm . The widest diodes are the same width as those previously studied by Smith, Pontius, and Budenstein.¹⁸⁻²² These were included to provide continuity with previous experiments. The smallest width was chosen to be comparable in width to existing IC diodes.

2. Enclosed Reference Structure

Figure 12 shows the 20 diodes of the "enclosed reference" structure. The aluminum contacts and the p^+ and n^+ regions are islanded by the n -region. The corners of the islands serve as concentration centers for the current and hence influence the filamentation pattern. The diode dimensions are the same as those given for the standard reference structure except that the 500 μm width is absent.

3. Contact Spike To p^+ Region Structure

One of the concerns of the present study was the evaluation of geometric irregularities at the metal- p^+ interface. In the " p^+ contact spike" structure, a triangular spike 5 μm long is positioned on the metal- p^+ interface. The spike is located about 1/4 of the way from the diode edge so that it will not be in a position of symmetry. Figure 13a shows the spike shape; parts b and c will be discussed in connection with multiple spike diodes. The 5 μm length was chosen because it was believed to be representative of spikes in "maverick" three-dimensional devices. The twenty diodes in this array have the same dimensions as the standard reference diodes except that the 500 μm width is absent.

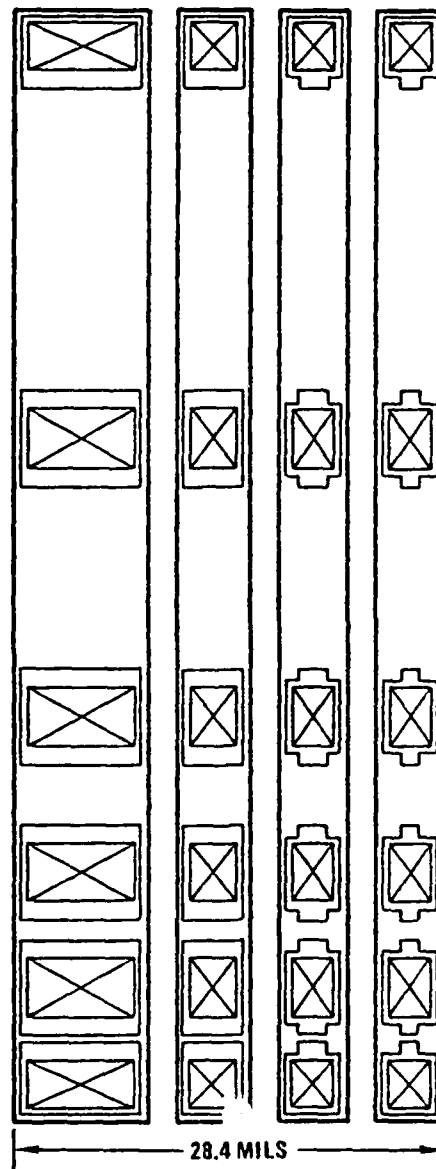


Fig. 12. Enclosed reference structure (after Green.)

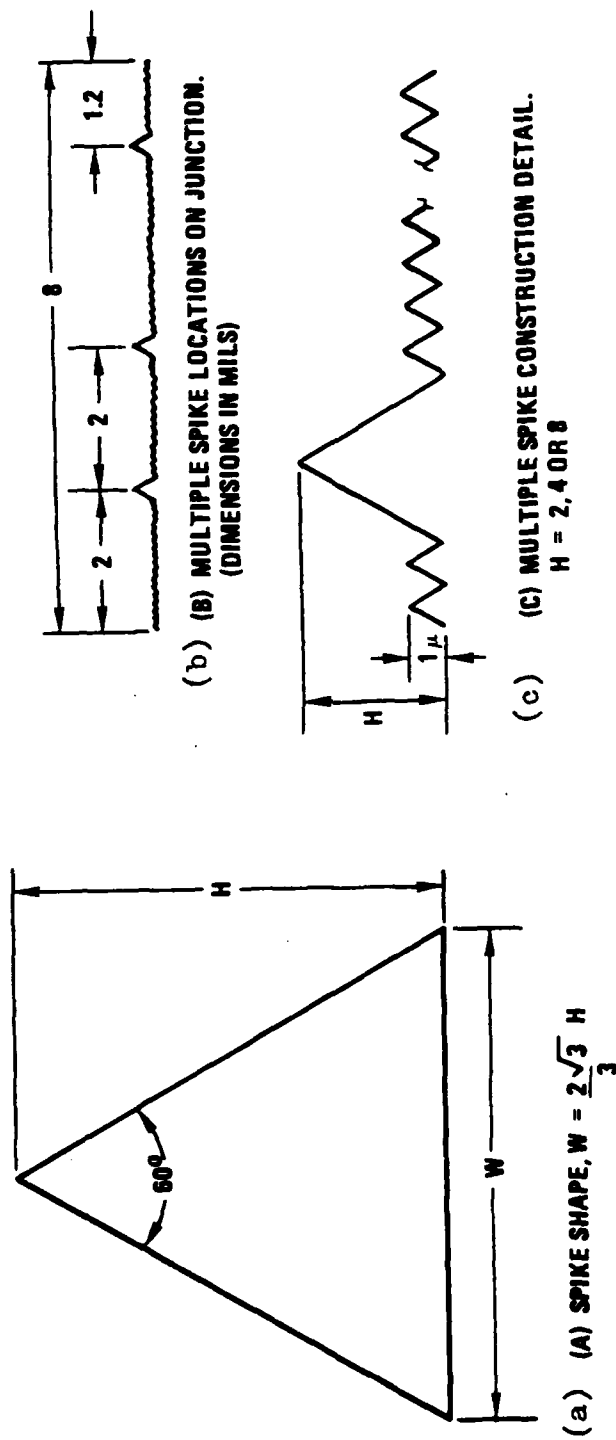


Fig. 13. Spike construction detail. (a) Spike shape for both single and multiple spikes. (b) Location of multiple spikes on the junction. (c) Enlarged view of multiple spikes (after Green, Ref. 43).

4. Contact Spike To n^+ Region Structure

Concerns and device geometry are the same as in Section 3 above, except that the spike is located on the metal- n^+ interface.

5. Diffusion Spike On p^+n Junction Structure

Concerns and device geometry are the same as in Section 3 above, except that the spike is located on the p^+n junction.

6. Diffusion Spike On n^+n Junction Structure

Concerns and device geometry are the same as in Section 3 above, except that the spike is located on the n^+n junction.

7. Half-Size Spike Structure

Devices of a single width, 100 μm , and with n-region spacings of 10, 30, 100, 300, and 500 μm contained a single spike 2.5 μm in length located 1/4 of the way from each diode edge. Spikes are located in different diodes on one of the four interfaces: metal- p^+ , metal- n^+ , p^+n , n^+n . Concerns are similar to those described in Section 3 above. Twenty diodes are in this array.

8. Four-Terminal Structure

Figure 14 shows the diodes with an extra pair of electrodes on the n-region. This four-terminal structure was designed so that a potential applied to the auxiliary electrodes could be used to cause current crowding in a controlled manner. The diodes have n-region lengths of 10, 30, and 100 μm , and widths of 30 and 100 μm . Six diodes are in this array.

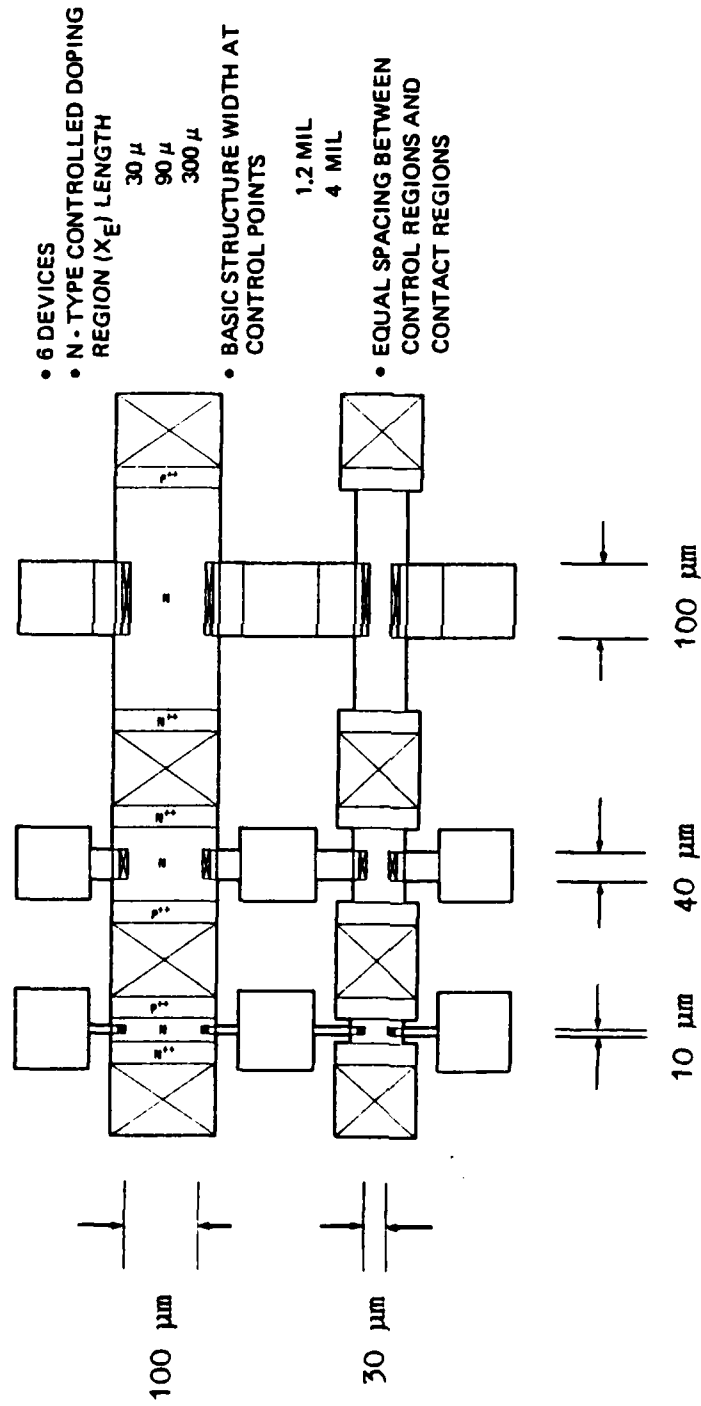


Fig. 14. Four terminal structure (after Green, Ref. 43).

9. Doping Level Test Structure

The structure of Fig. 15 is intended for measuring the sheet resistance of the n-material and thereby to check the doping level and uniformity of processing.

10. Interdigitated Structure

Two structures, shown in Fig. 16, simulate the geometry between fingers of a three-dimensional interdigitated device. These can provide perspective on the pattern of current filamentation in interdigitated junction devices.

11. Radius Of Curvature Structure

A group of nine diodes was designed to simulate the current patterns in three-dimensional diffused epitaxial transistors. The radius of curvature of the p^+ and n^+ islands, and spacing between these islands were the parameters. Figure 17 shows a diagram of the "radius of curvature" diodes. The design sought to minimize series resistances while preserving the proximity of two regions of small radius of curvature. Radii of curvature for the p^+ and n^+ regions are 5, 10, and 30 μm , with both radii being the same for a single diode. The minimum separations of the p^+ and n^+ regions are 10, 30, and 100 μm .

12. Processing Test Structure

As mentioned previously, Rockwell used the processing test structure for electrical characterization of the wafers.

13. Rockwell Devices

The Rockwell devices were not used in the present study.

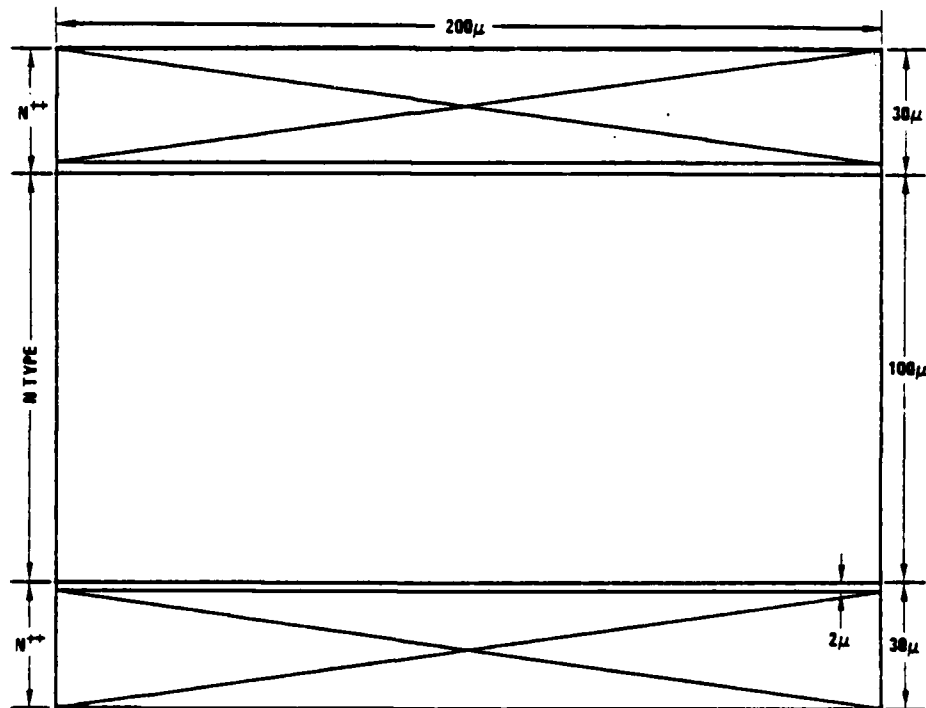


Fig. 15. Doping level test structure (after Green, Ref. 43).

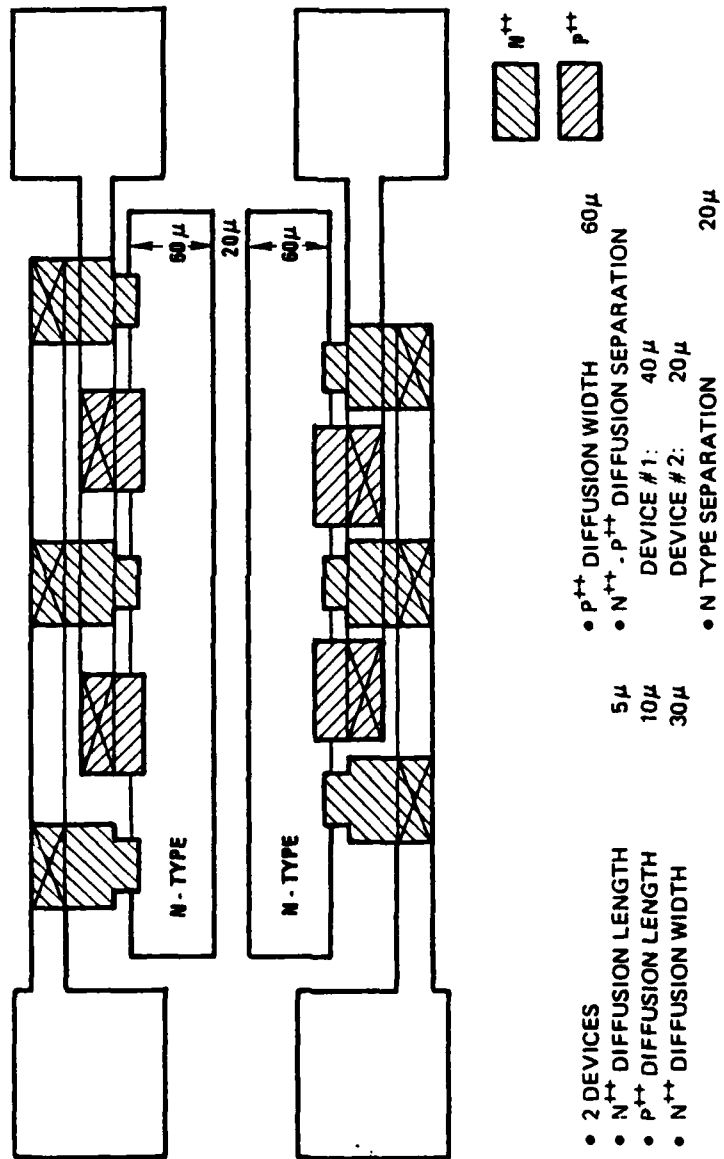


Fig. 16. Interdigitated structure (after Green, Ref. 43).

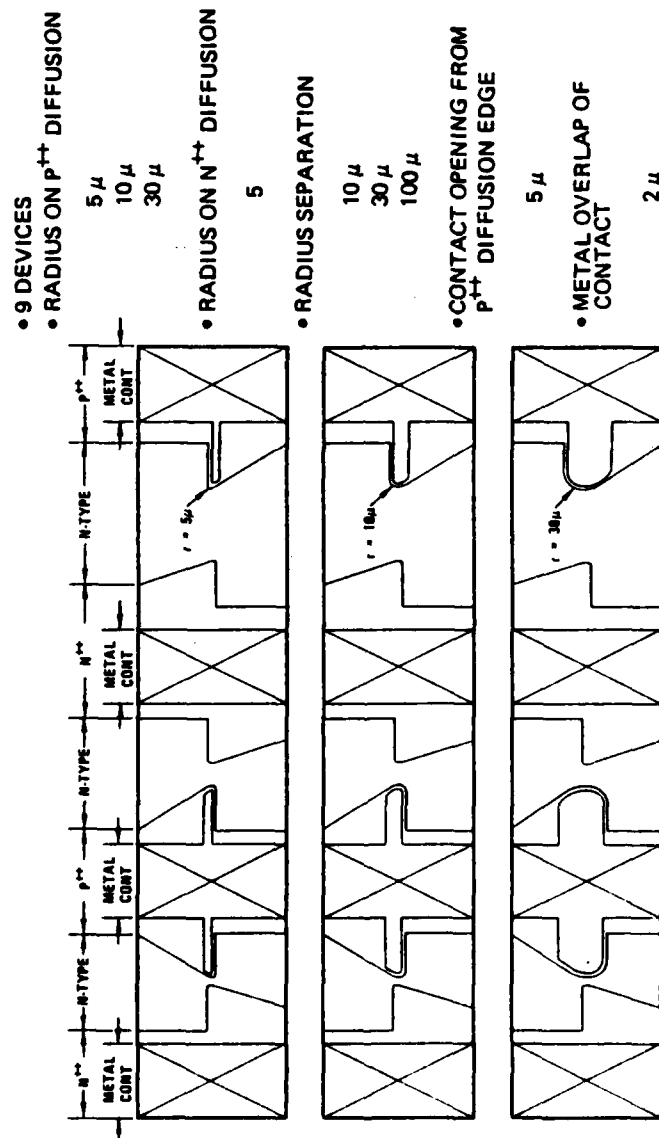


Fig. 17. Radius of curvature structure (after Green, Ref 43).

14. Multiple Spike Structure

Diodes of 200 μm width and with n-region lengths of 10, 30, and 100 μm were fabricated with three triangular spikes on a background of 1 μm triangular spikes. Spike lengths for different diodes are 1, 2, 4, and 8 μm . Figure 13b shows the positions of the three spikes, and Fig. 13c shows the enlarged view of one of the spikes. Spikes are located in different diodes on one of the four interfaces: metal- p^+ , metal- n^+ , p^+n , n^+n . The group also contains reference structures with no spikes. Concerns are similar to those described in Section 3 above. There are fifty-one diodes in this array.

15. Labeling Scheme

The labeling scheme for identifying a particular diode from the test population of approximately 150,000 diodes is given here. A diode was labeled by a code number of the form ABCCDDEE where A, B, CC, DD, and EE are respectively, the batch (1-2), wafer (1-5), die (01-77), structure (01-14), and device (01-51) numbers. A particular wafer will be referred to by its batch number followed by a dash and then the wafer number.

Table 2 relates wafer number to targeted doping level. Figure 9a identifies the die numbers, while Fig. 8b identifies the different structure type numbers. Individual devices are numbered as in Fig. 9b.

<u>WAFER NUMBER</u>	<u>TARGETED DOPING LEVEL (cm⁻³)</u>
1	10 ¹⁴
2	10 ¹⁵
3	10 ¹⁶
4	10 ¹⁷
5	5 x 10 ¹⁷

Table 2. Wafer labeling scheme.

C. Device Characterization

1. Resistivity Measurements

The doping level test structure of Fig. 15 provides one vehicle for estimating the n-region doping level. The doping level is determined by measuring the resistance of this structure, calculating the n-region resistivity, and finding the corresponding impurity concentration from a graph of resistivity versus doping level. The resistivity of the n-type silicon is calculated from the equation

$$\rho = \frac{RWt_{Si}}{L}$$

where

ρ = resistivity (ohm-m)

R = resistance (ohms)

t_{Si} = silicon thickness (m)

W = structure width (m)

L = structure length (m)

Figure 15 shows that W and L are 200 μm and 100 μm , respectively. The initial epitaxial layer thickness was 0.6 μm (0.55 to 0.65 μm) but some

of the silicon was consumed during processing; Rockwell estimates that perhaps 0.4 μm of silicon remains.

A factor which could influence the resistance measurements is the presence of surface charge. Rockwell International has evaluated the role of surface charge as follows.

"An attempt to reduce the effects of surface charge was made by performing an hydrofluoric acid etch of a test chip from each doping level to remove the oxide. The measurements were repeated immediately with no noticeable differences. Thus surface charge effects were excluded as a consideration from the resistivity measurements." (Ref. 43)

In the results which follow, the resistance R was calculated upon applying 5V to the terminals of the doping level test structure and measuring the current with a Simpson Model 260 multimeter.

Figure 18a shows the resistances in kilo-Ohms of all the doping level test structures on Wafer 2-2 (targeted doping level of 10^{15} cm^{-3}). The resistances vary from a maximum of 1.6 $\text{M}\Omega$ on the left side of the wafer to a minimum of 120 $\text{k}\Omega$ on the right side, more than a factor of ten. Figure 18b presents the information of Fig. 18a in a three-dimensional format. The doping level estimated from the data in Fig. 18 ranges from less than 10^{14} cm^{-3} to about $5 \times 10^{14} \text{ cm}^{-3}$.

Figure 19a shows the resistances of all the doping level test structures on Wafer 2-1 (nominal doping density of 10^{14} cm^{-3}). This wafer did not receive an ion implantation. The asterisks indicate a portion of the wafer surface which is discolored. The dice in the discolored area appear to be damaged, and the doping level test structures

(a)

			560	350	510	340		
	410	540	510	590	410	200	230	
	620	530	690	420	390	390	240	150
860	830	580	500	500	510	200	280	200
1200	740	360	600	380	410	180	180	250
1400	790	710	630	420	410	170		120
1600	850	740	820	190	420	160	140	140
1200	1100	930	1000	410	290	130	280	240

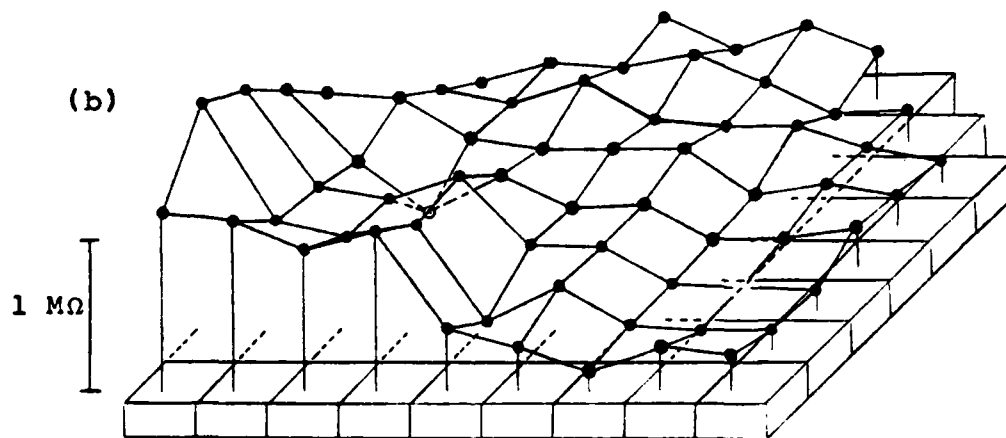


Fig. 18. Impedance of the doping level test structure versus position on the surface of Wafer 2-2. (a) Numerical values of the impedance, in units of $k\Omega$. (b) Three-dimensional plot of impedance versus position.

(a)
WAFER 2-1

			120	120	200	350		
	*	*	130	120	220	1400	180	
*	*	160	150	150	240	420	960	
*	*	190	190	180	280	330	810	440
*	*	260	300	200	270	280	820	1500
*	290	310	350	240	260	390		440
3300	530	380	290	210	240	420	630	1400
1300	760	490	360	330	540			

(b)
WAFER 1-3

			130				
			170				
			140				
140	150	150	140	150	130	140	
			130				
			160				
			170				

(c)
WAFER 2-4

				7.1			
				7.0			
				7.1			
7.4	7.8	7.6	6.5	6.9	6.9	6.9	6.9
			7.1				
			7.8				

Fig. 19. Impedance measurements on Wafers 2-1, 1-3, and 2-4; all numbers have units of $k\Omega$. (a) Impedance of doping level test structures on Wafer 2-1. (b) Impedance of forward biased diode with same geometry as doping level test structure on Wafer 1-3. (c) Impedance of doping level test structure on Wafer 2-4.

do not function normally; some act as short circuits. The maximum and minimum resistances are $3.3 \text{ M}\Omega$ and $120 \text{ k}\Omega$, respectively, indicating a doping level range from less than 10^{14} cm^{-3} to about $5 \times 10^{14} \text{ cm}^{-3}$. Figure 19b contains resistances obtained on diode 8 of the standard reference structure of the sequence of dice shown. The diodes were forward biased at 5V on Wafer 1-3 (targeted doping level of 10^{16} cm^{-3}). This diode has the same n-region geometry as the doping level test structure. One row and one column of dice were tested. Relative position is indicated by the black rectangle, which represents the drop out. The resistances vary from a maximum of $170 \text{ k}\Omega$ to a minimum of $130 \text{ k}\Omega$, corresponding to a doping level of $3 - 5 \times 10^{14} \text{ cm}^{-3}$.

Figure 19c shows the resistances of some of the doping level test structures on Wafer 2-4 (targeted doping level of 10^{17} cm^{-3}). The resistances vary from a maximum of $7.8 \text{ k}\Omega$ to a minimum of $6.5 \text{ k}\Omega$. This indicates a doping level of $1.0 - 1.4 \times 10^{16} \text{ cm}^{-3}$.

Data similar to that shown in Fig 19b, c were also taken on Wafer 2-5 (targeted doping level of $5 \times 10^{17} \text{ cm}^{-3}$). The resistances varied from a maximum of $1.1 \text{ k}\Omega$ to a minimum of $1.0 \text{ k}\Omega$, indicating a doping level of $1.1 - 1.4 \times 10^{17} \text{ cm}^{-3}$.

2. Reverse Bias Breakdown Voltage Measurements

The reverse bias breakdown voltage provides a second method for estimating the doping levels. The doping level is determined by measuring the breakdown voltage, and then finding the corresponding impurity concentration from theoretical calculations of reverse bias breakdown voltage versus impurity concentration. All of the breakdown voltage measurements described below were made with a Tektronix Type 576

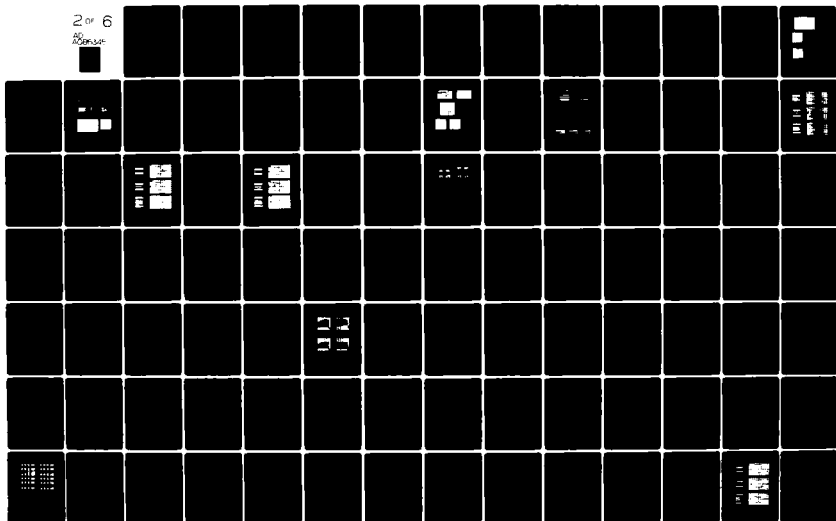
AD-A086 345

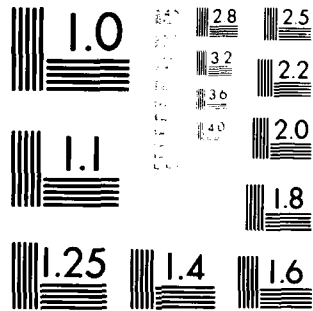
AUBURN UNIV ALA DEPT OF PHYSICS
SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)
MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAAG29-78-6-0111
ARO-15840.3-A-EL NL

UNCLASSIFIED

2 of 6

AD-A086 345





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

curve tracer at a current of $10 \mu\text{A}$. Rockwell International provided part of the data taken on Wafers 2-1, 2-2, and 1-3. Doping levels deduced from resistance measurements and reverse breakdown voltage measurements are compared with targeted doping levels in Table 3. Reverse breakdown measurements will be discussed further in the following paragraphs.

WAFER NUMBER	TARGETED	Doping Level (cm^{-3})	
		FROM RESISTANCE MEASUREMENTS	FROM MEASUREMENTS OF REVERSE BIAS BREAKDOWN VOLTAGE
2-1	1×10^{14}	$(3 \pm 2) \times 10^{14}$	$(3 \pm 2) \times 10^{15}$
2-2	1×10^{15}	$(3 \pm 2) \times 10^{14}$	$(5 \pm 4) \times 10^{15}$
1-3	1×10^{16}	$(4 \pm 1) \times 10^{14}$	$(5 \pm 4) \times 10^{15}$
2-4	1×10^{17}	$(1.2 \pm .2) \times 10^{16}$	$(4 \pm 2) \times 10^{16}$
2-5	1×10^{17}	$(1.3 \pm .2) \times 10^{17}$	$(1.3 \pm .3) \times 10^{17}$

Table 3. Estimations of the n-region doping level. The first two columns show the wafer number and the targeted doping level. The third column shows estimations based on resistance of the doping level test structure (a forward biased diode was used for Wafer 1-3). The fourth column shows estimations based on the reverse bias breakdown voltage.

Breakdown voltage measurements of standard reference, enclosed reference, and radius of curvature diodes were made on Wafer 2-1. The n-region length of all these diodes was $30 \mu\text{m}$. The breakdown voltages ranged from a maximum of 370 V to a minimum of 170 V. Within this range, there was no correlation between breakdown voltage and structure type. Also doping levels deduced from breakdown voltage and resistance of the doping level test structure did not correlate. Additional breakdown voltage measurements were taken on a sample of 30 standard

reference diodes with n-region lengths of 100 μm and widths of 500 μm . The diode widths were large enough to insure that the n-region voltage drop was small compared to the junction voltage drop. The maximum, minimum, mean, and standard deviation of the sample are 290, 135, 198, and 40 V, respectively. There was no definite correlation of these breakdown voltages with the resistance of the doping level test structure on the same die.

The breakdown voltages of all diodes tested on Wafer 2-1 increased while being pulsed by the curve tracer; increases of as much as 50 V were observed. In addition, all of the breakdown voltages obtained by Rockwell International for Wafer 2-1 are followed by a symbol which indicated that "thermal walkout was not entirely stable at the time the measurement was taken." The voltage increases were permanent.

Reverse bias breakdown voltage is a function of the minimum separation between the p^+n and n^+n junctions for the shortest n-region length diodes on Wafer 2-1. Breakdown voltage is plotted as a function of spike length for p^+n and n^+n spike diodes with an n-region length of 10 μm in Fig. 20. The spike lengths are 0, 1, 2, 4, 5, and 8 μm , and the corresponding n-region lengths at the tips of the spikes are 10, 9, 8, 6, 5, and 2 μm . The reverse bias breakdown voltage decreases with increasing spike length for both types of diffusion spikes. For these diodes, the p^+n junction depletion layer extends all the way across the n-region at the breakdown voltage, that is, punchthrough occurs. A similar plot for diodes with an n-region length of 30 μm shows no correlation between breakdown voltage and spike length, except possibly for a spike length of 8 μm . Similar effects were also observed on Wafers 2-2 and 1-3.

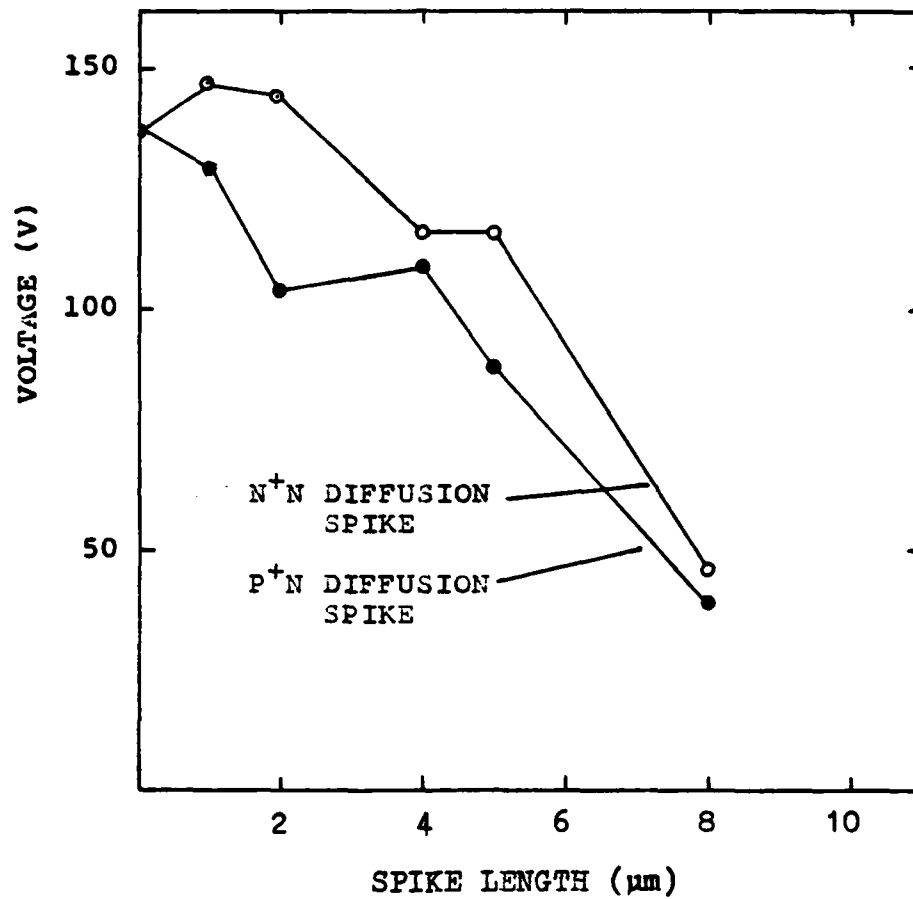


Fig. 20. Reverse bias breakdown voltage versus diffusion spike length. The breakdown voltage was measured at approximately 10 μA reverse current for 10 μm n-region length diffusion spike diodes on Wafer 2-1.

To avoid punchthrough during reverse breakdown voltage measurements for determining doping level, only the 100 μm n-region length diodes were used on the high resistivity wafers (2-1, 2-2, 1-3). The n-region doping level estimations are based on the maximum and minimum breakdown voltages. The n-region doping level estimation for Wafer 2-1 is $1 - 4 \times 10^{15} \text{ cm}^{-3}$. This does not overlap with the resistance estimations, indicating that at least one of the methods is in error.

Breakdown voltage measurements similar to those described for Wafer 2-1 were performed on Wafer 2-2. The maximum breakdown voltage of 30 μm n-region length diodes on Wafer 2-2 was 150 V and the minimum voltage was 50 V, compared to 370 V and 170 V for Wafer 2-1. The 100 μm n-region length standard reference diodes also had somewhat smaller breakdown voltages than corresponding diodes on Wafer 2-1. The maximum, minimum, mean, and standard deviation are, respectively, 263, 67, 108, and 32 V. Almost all of the data from Rockwell International are followed by the "thermal walkout" symbol. The discussion concerning change of breakdown voltage during measurement also applies to diodes on Wafer 2-2. The n-region doping level estimation is $1 - 8 \times 10^{15} \text{ cm}^{-3}$.

Breakdown voltage measurements similar to those described for Wafer 2-1 were performed on Wafer 1-3. The maximum and minimum breakdown voltages of the 30 μm n-region length diodes were 280 V and 150 V, respectively. However, thermal walkout did not occur. The maximum, minimum, mean, and standard deviation of standard rereference diodes with an n-region length of 100 μm are 290, 70, 212, and 52 V, respectively.

Breakdown voltages of these diodes also increased during measurement.

The n-region doping level estimation is $1 - 8 \times 10^{15} \text{ cm}^{-3}$.

The reverse bias breakdown voltages of nearly all diodes on Wafers 2-4 and 2-5 fell into relatively narrow ranges and there was no correlation with structure type or n-region length (breakdown voltages were measured for standard reference and diffusion spike diodes with varying n-region lengths and widths). The sample size was 60 diodes on Wafer 2-4 and 100 diodes on Wafer 2-5. The maximum, minimum, mean, and standard deviation of the sample on Wafer 2-4 are 31.5, 24.0, 28.0, and 1.4 V, respectively. The corresponding values on Wafer 2-5 are 13.1, 11.7, 12.39, and 0.24 V. Doping level estimations are based on the maximum and minimum values. The n-region doping level estimations for Wafers 2-4 and 2-5 are $2 - 5 \times 10^{16} \text{ cm}^{-3}$ and $1.0 - 1.5 \times 10^{17} \text{ cm}^{-3}$, respectively.

3. Summary and Discussion

Table 3 summarizes the doping level estimations based on the resistivity and reverse bias breakdown voltage methods. The first column shows the wafer code number and the second column shows the targeted doping level. The third and fourth columns show the n-region doping level estimations. The two methods agree only for Wafer 2-5. The data in Table 3 indicate a wide variation in the n-region doping level for several wafers. The doping level estimations vary by a factor of five for Wafer 2-4, and by a factor of eighty for Wafers 2-2 and 1-3. In addition, the distributions for Wafers 2-1, 2-2, 1-3, and 2-4 do not overlap, indicating that at least one of the estimations is inaccurate.

Thus, it is not clear how much of the variation in Table 3 is actually caused by changes in the n-region doping level. Deducing doping level from resistance measurements involves assumptions on film thickness, and specimen homogeneity. Available data relating resistivity and doping level pertain to bulk specimens, not thin films. Similarly, junction breakdown characteristics depend on such quantities as the avalanche coefficients, lifetimes, and mobilities, as well as doping levels. In addition, silicon-island edges may affect electrical measurements in silicon-on-sapphire devices. According to Pancholy and Oki:⁴⁴

"Under bias-temperature stress or ionizing irradiation, oxides over island edges may trap charges or indicate mobile ion-induced instability. In some cases the charges result in formation of a conductive path along island edges which may lower the junction breakdown voltage and increase the reverse junction leakage current."

The lack of a strong correlation between resistance of the doping level test structure and reverse bias breakdown voltage indicates that parameters in addition to doping level are involved.

To illustrate the variation among individual devices, the forward bias impedances of standard reference diodes from a single die on Wafer 2-1 are plotted versus the n-region length-to-width ratio in Fig. 21. The forward bias impedances (measured at 10 V and 20 V on a curve tracer) should be proportional to the n-region resistance. The n-region resistance, in turn, should be proportional to the length-to-width ratio. Thus, the plot should be a straight line whose slope gives the

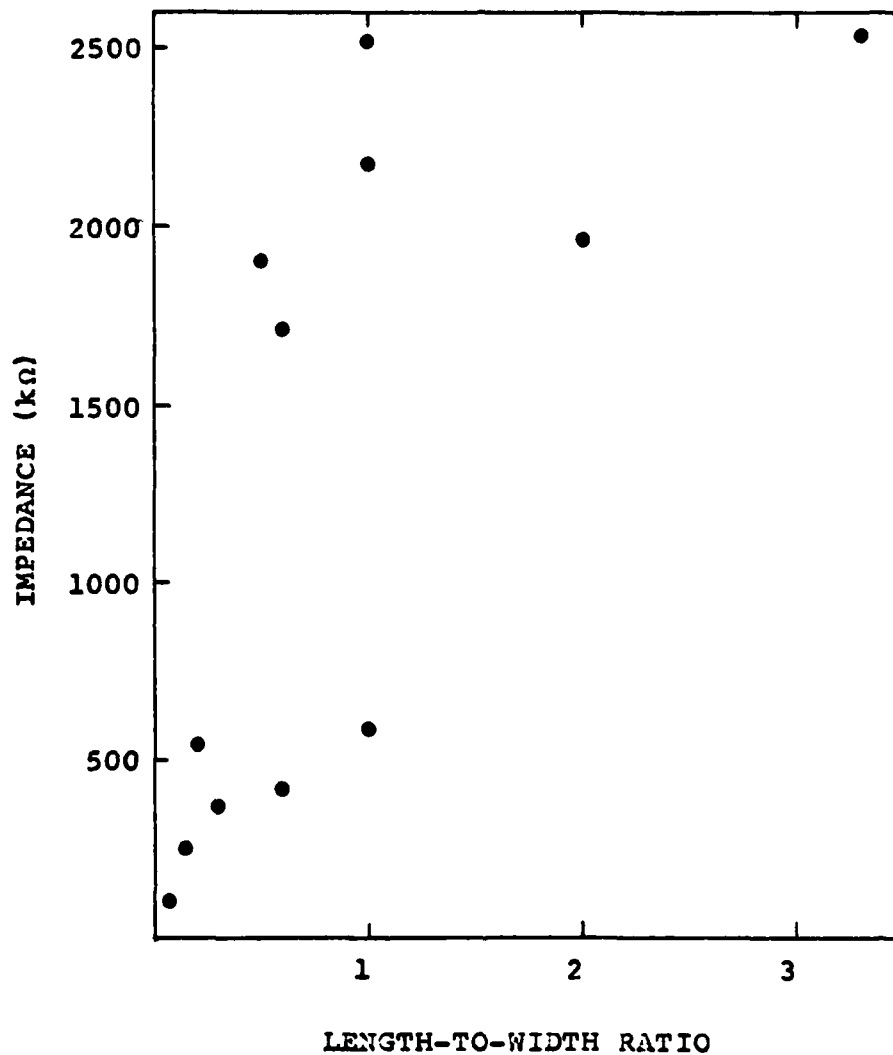


Fig. 21. Impedance versus length-to-width ratio for forward biased standard reference diodes from a single die on Wafer 2-1. The impedances were measured at 10 or 20 V.

sheet resistance, or the "ohms per square," of the n-region. However, there is considerable scatter in the plot.

Another quantity which should be related to the n-region doping level is the voltage threshold for destructive second breakdown under dc reverse bias, that is, the dc reverse bias voltage at which the diode burns out. Figure 22 shows the distribution of dc reverse bias burnout voltages for diode type 14-03 (10 μm n-region length, 200 μm width, straight junctions) on Wafer 2-2. The upper part of the figure shows the statistical distribution of the burnout voltages while the lower part of the figure shows a three-dimensional plot of burnout voltage versus position on the wafer surface. Wafer 2-2 was chosen for this test because it had the most systematic variation of doping level test structure resistance across the wafer surface. Figure 22 should be compared with Fig. 18. There is apparently no correlation between the shapes of the two surfaces.

Thus, it seems that part of the variation in diode electrical properties is attributable to factors other than n-region doping level. Therefore, the n-region doping level estimations must be interpreted with caution.

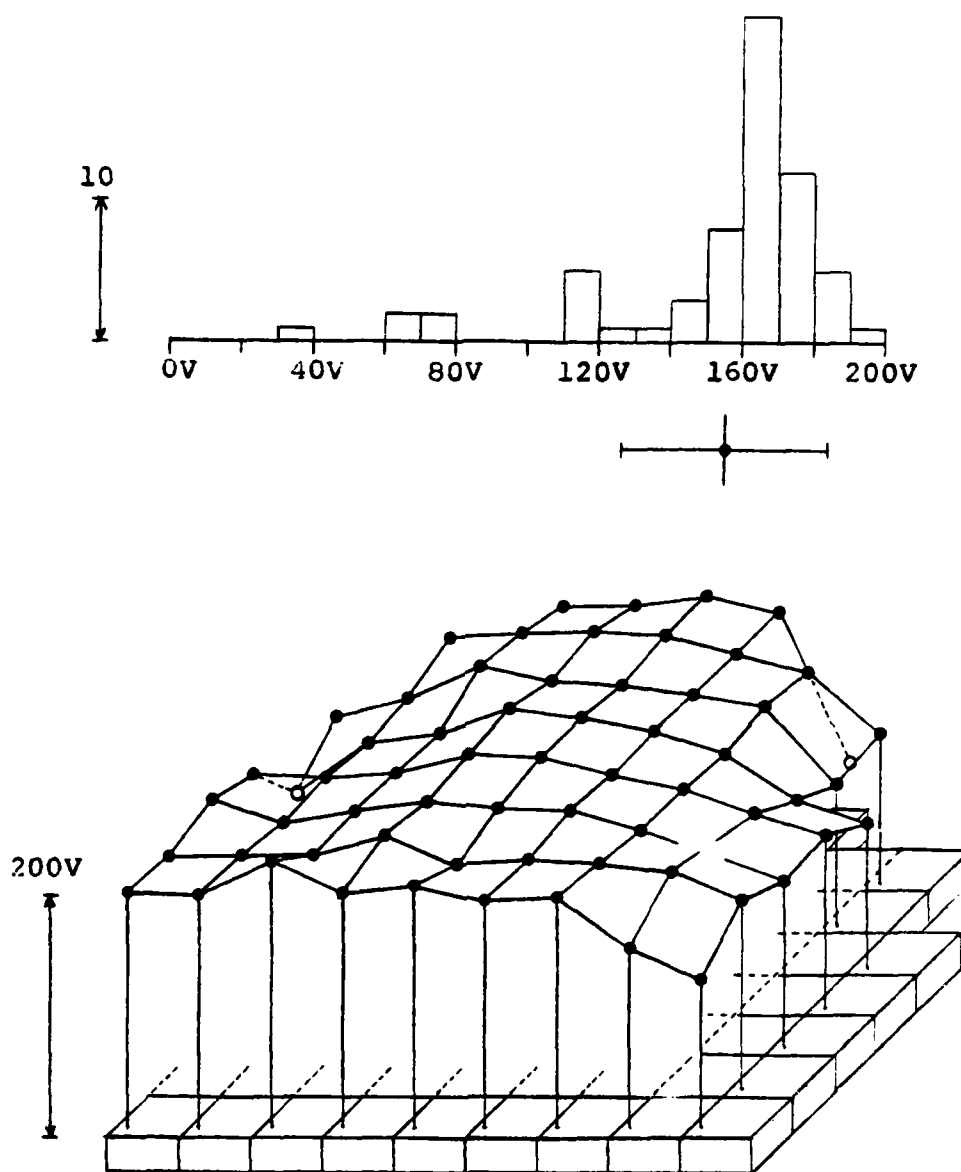


Fig. 22. Breakdown voltages of a particular type of diode on Wafer 2-2. The n-region length of the diode is 10 μm . Top: Histogram showing the frequency distribution of the breakdown voltages. Bottom: Three dimensional plot showing breakdown voltage versus position on the wafer. The diodes were destroyed by dc reverse bias.

V. RESULTS

This chapter presents experimental results which relate second breakdown susceptibility to diode geometry and doping level. Sections A through E discuss the heating patterns observed in standard reference, diffusion spike, contact spike, and enclosed reference diodes. Section F compares properties of standard reference, diffusion spike, and enclosed reference diodes (energy thresholds, voltage thresholds, and damage morphology). Sections G and H discuss radius of curvature and interdigitated devices, respectively. Finally, Section I discusses several special tests, including a correlation of heating patterns with three-dimensional current-voltage-time waveform surfaces.

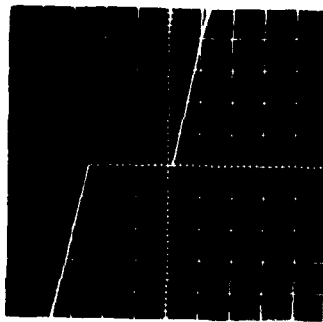
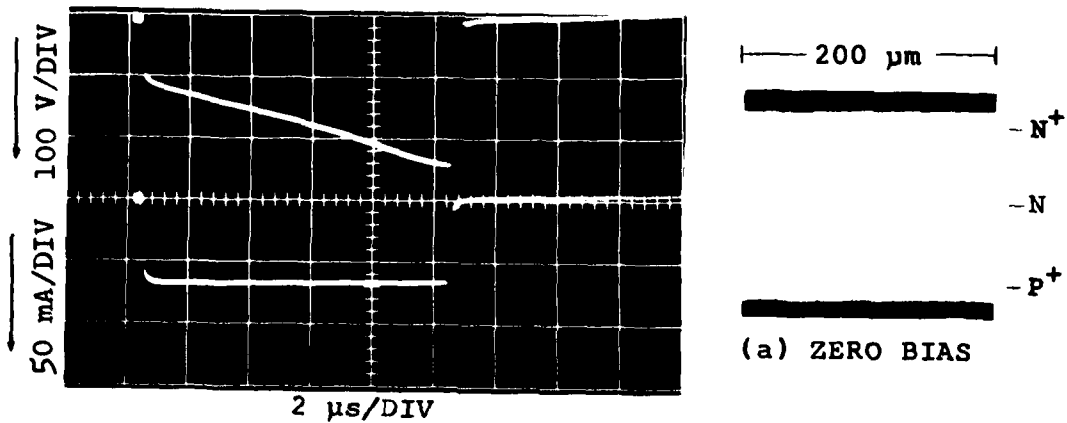
It was discovered early in the study that the experimental results were affected by factors other than diode geometry and doping level. There are often substantial differences among apparently identical devices, possibly resulting from slight process variations introduced during the fabrication procedure. In some cases, these variations are large enough to obscure the effects of deliberately introduced parameters. Therefore, in the results which follow, some of the experimental data are presented and discussed in a statistical manner.

Unless otherwise specified, the tests were performed with pulses 10 μ s in length, and the heating pattern photographs were taken at the end of the pulse.

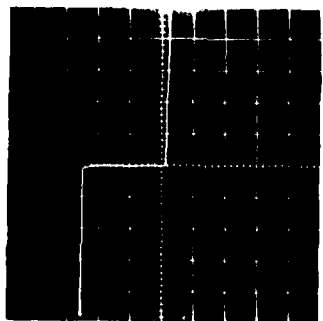
A. Standard Reference Diodes

Before going into the details on geometric and doping effects, the overall phenomena will be described. Emphasis will be on the reverse bias condition, since devices are somewhat more sensitive to second breakdown under reverse bias. Figure 23 shows a test of a standard reference diode on Wafer 2-5. This diode has an n-region length of 100 μm and width of 200 μm . The current and voltage waveforms are shown in the upper left portion of the figure. The upper trace is the voltage waveform, and the lower trace is the current waveform. Current and voltage scales are shown to the left of the waveforms. Note that time increases to the right and both current and voltage increase downward. A zero bias photograph is shown in Fig. 23a, and the heating patterns at 2, 4, 6, 8, 9, and 10 μs after the leading edge of the waveforms are shown in Fig. 23b-g, respectively. Two pre-test I-V characteristics, using different current scales, are shown on the left side of the diagram. Current under forward bias, determined primarily by the resistance of the n-region, is approximately 1.3 k Ω . The lower I-V characteristic, using the more sensitive current scale, shows that the reverse bias current is very small prior to avalanche breakdown at approximately 12 V. Such low reverse saturation current is typical of an undamaged diode.

The current level corresponding to the heating patterns in Fig. 23b-g is about 67 mA (average current density, $8.4 \times 10^8 \text{ A/m}^2$), while the voltage increases from approximately 100 V at the beginning of the pulse to about 240 V at the end. For low current levels, where little temperature rise occurs during a pulse, the voltage waveform parallels



PRE-TEST I-V
1 mA PER VERT DIV
5 V PER HORIZ DIV



PRE-TEST I-V
0.1 mA PER VERT DIV
5 V PER HORIZ DIV

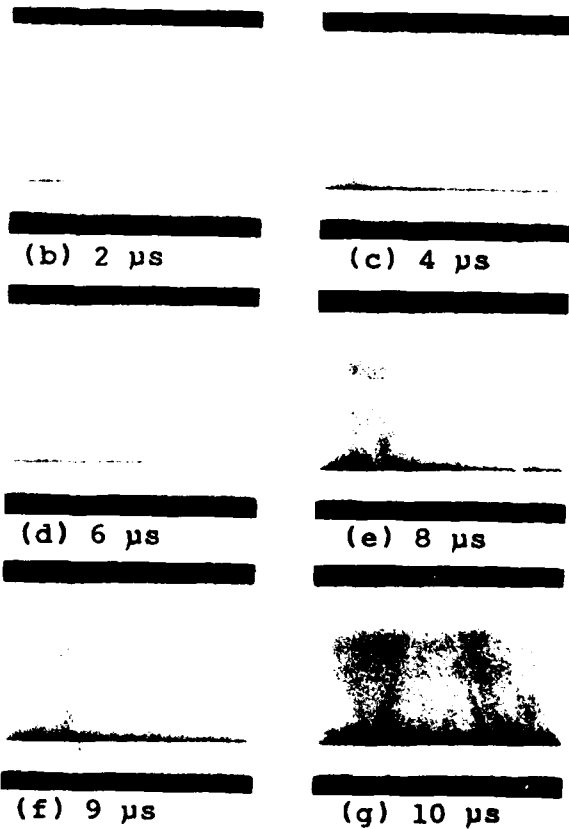


Fig. 23. Reverse bias test of a standard reference diode on Wafer 2-5. The n-region length and width of this diode are 100 and 200 μ m, respectively. Current and voltage waveforms, and two pre-test I-V characteristics are shown on the left side of the figure. (a) Zero bias photograph. (b)-(g) Heating patterns at 2, 4, 6, 8, 9, and 10 μ s after the leading edge of the waveforms.

the current waveform. However, in Fig. 23, both the voltage waveform and the heating patterns indicate a temperature increase during the pulse. The most intense heating occurs at the p^+n junction, and the n -region is heated uniformly. The degree of p^+n and n -region darkening increases continuously throughout the pulse.

A second test on the diode of Fig 23 is described in Fig. 24. The current and voltage waveforms are shown in the lower part of the figure, and the heating patterns at 2, 4, 6, 8, 9, and 10 μs after the leading edge of the waveforms are given in Figs. 24a-f, respectively. This test was performed by increasing the current approximately 3 mA over the level in Fig. 23, to about 70 mA (8.7×10^8 A/m²). The heating pattern in Fig. 24f shows that a hot spot has formed along the p^+n junction at the end of the pulse. The temperature becomes non-uniform because of changes in medium properties with temperature and the geometric dependence of the heat transfer from various portions of the diode.

Two portions of the diode determine the current distribution, the junction region and the high resistivity n -region. The resistivity-temperature dependence of the n -region for different doping densities is shown in Fig. 25. Junction voltage depends on doping density of the n -region, temperature, and current density. Figure 26 shows the voltage-temperature curves for different current densities calculated for the doping density of 10^{16} cm⁻³. Both Fig. 25 and Fig. 26 contain a rising portion and a turnover. The rising portions imply stability toward small increases in temperature, while the falling portions lead toward instability. A steady state can exist during the falling por-

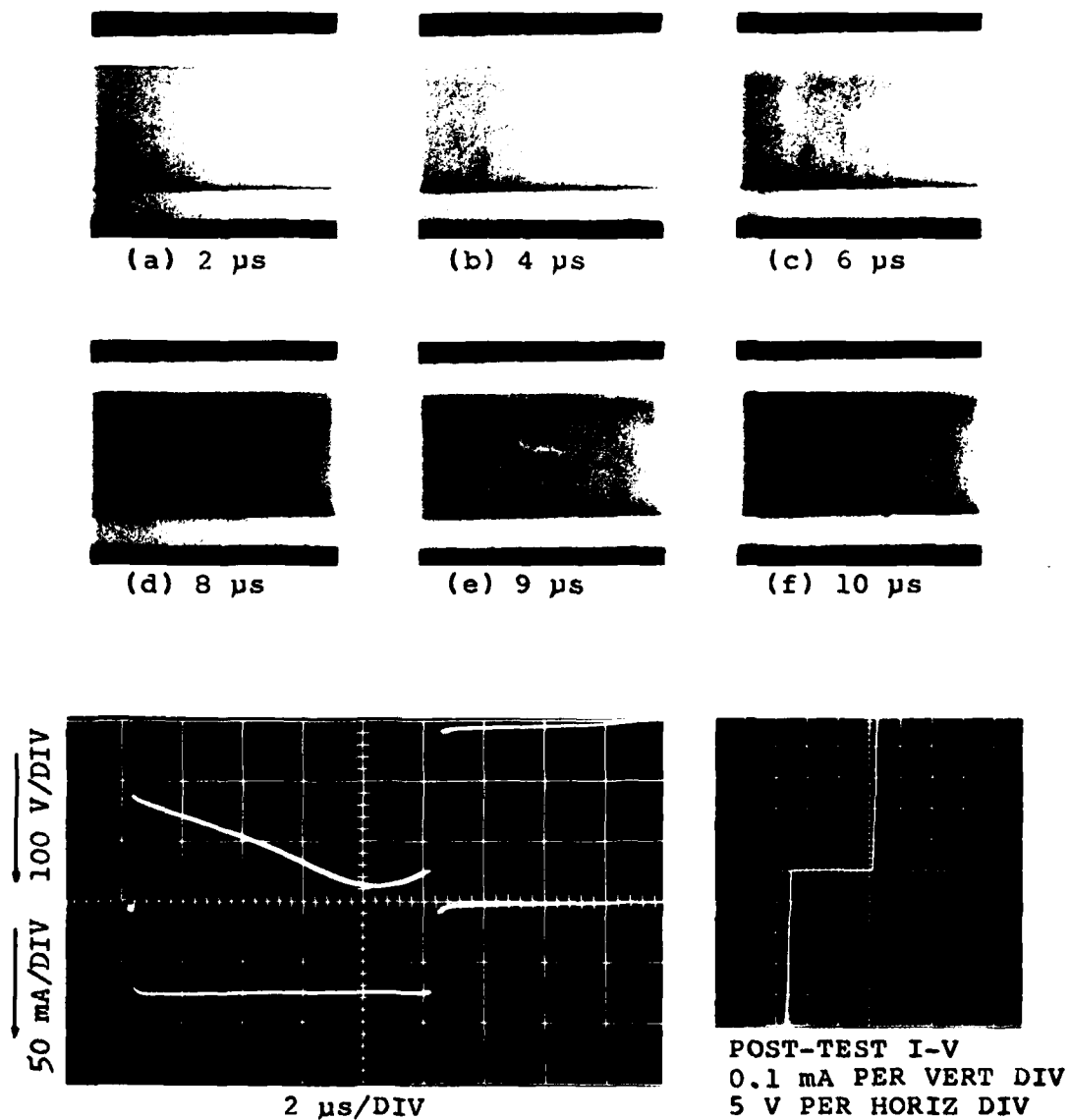


Fig. 24. Reverse bias test of a standard reference diode on Wafer 2-5. This is the same diode as in Fig. 23, at a slightly higher current amplitude. (a)-(f) Heating patterns at 2, 4, 6, 8, 9, and 10 μs after the leading edge of the waveforms. A post-test I-V characteristic is also shown.

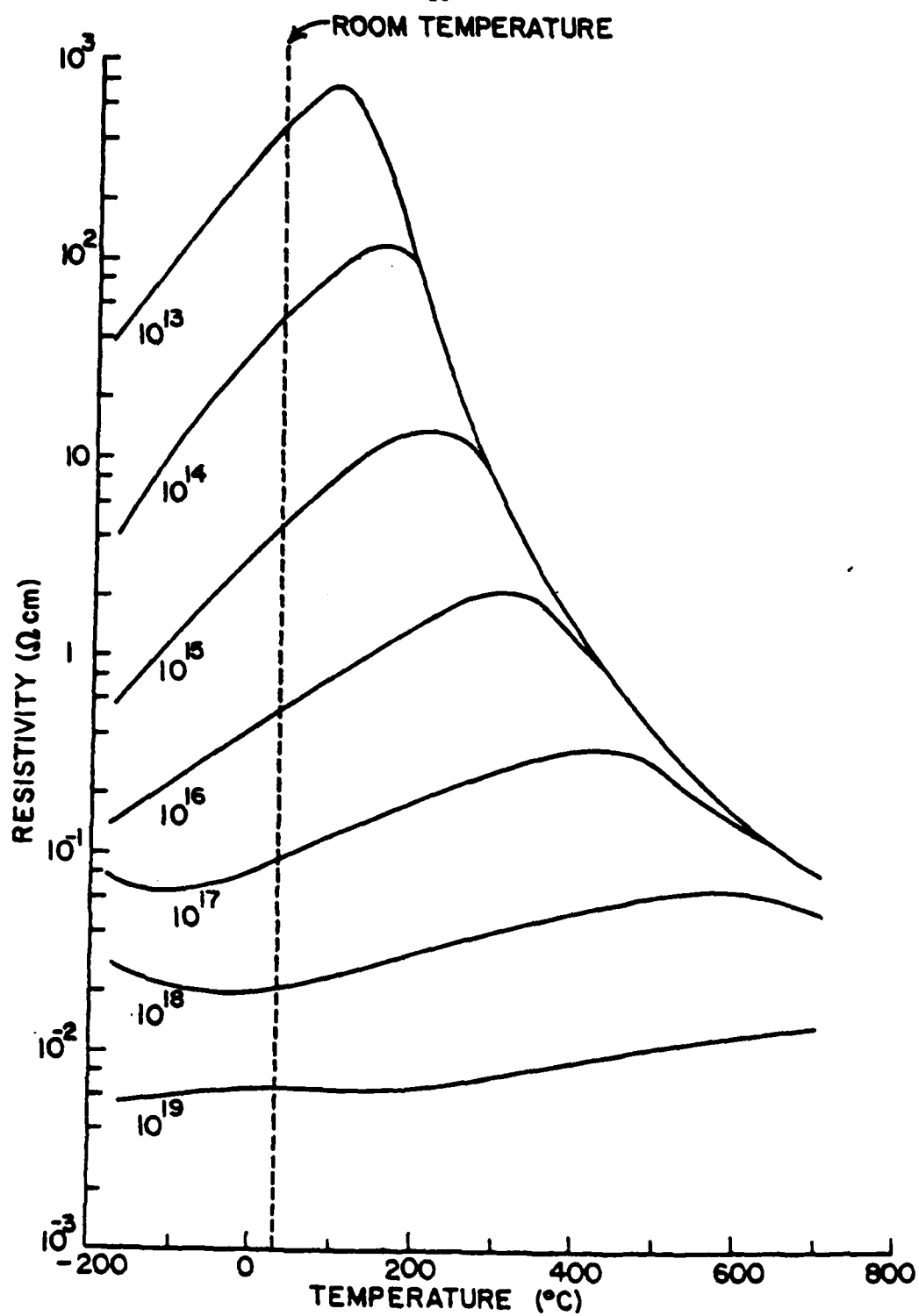


Fig. 25. Resistivity as a function of temperature for n-type silicon (after Runyan, Ref. 45).

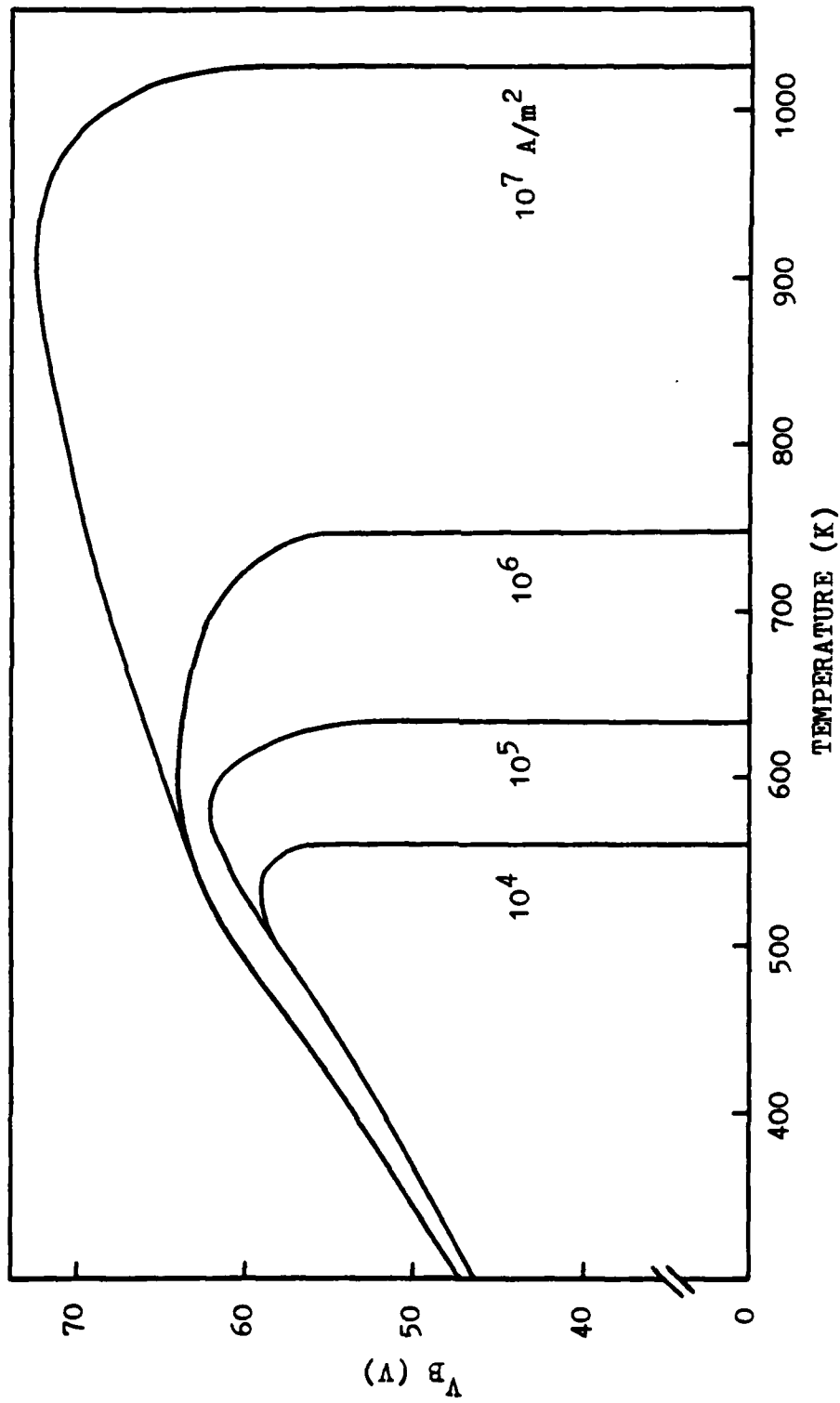


Fig. 26. Voltage-temperature curves for different current densities calculated for the doping density of 10^{16} cm⁻³.

tions if the heat sinking balances the Joule heating. However thermal runaway is virtually inevitable in a current tube having both junction and n-region beyond their turnover points. If only one is beyond turnover, the other can exert a stabilizing control.

Comparison of Fig. 23 and Fig. 24 shows that increased current amplitude is accompanied by more intense heating of the junction and n-region. Both of these require increased voltage to maintain the same current density, thus producing the observed rise in voltage during each current pulse. This behavior continues until some portion of the diode passes beyond the turnover point in either the junction region or the n-region. This may occur first in either region, depending upon the doping level, conditions of excitation, and geometry. In diodes with a highly doped n-region (as in Wafers 1-5 and 2-5) and at the high current densities of the present experiments, the turnover of the junction voltage occurs first. However, in lightly doped diodes, the n-region turnover occurs first.

In Wafer 2-5, the junction turnover precedes the n-region turnover and filamentation starts at the junction site where turnover occurs. As the junction voltage drops at this site, local current increases. Current lines converge on the low impedance junction path until limited by the spreading resistance associated with their convergence. The n-region in series with the junction hot spot receives a higher current and its temperature rises, with the filament growing across the n-region as the converging current lines cause the temperature of the propagating filament to pass through its turnover point. When the n-region is bridged, the filament is no longer ballasted by a high resis-

tance and the temperature rises rapidly to the melting point. The melt transition is accompanied by a further drop in resistance, and is the damage mode of second breakdown.

Only a single hot spot formed in Fig. 24f. However, multiple hot spots can form since part of the current passing through a junction hot spot is collected from the surrounding region. Such current lines are elongated and accompanied by a series spreading resistance. When the voltage associated with this spreading resistance exceeds the junction voltage away from the hot spot, the current lines will no longer bend toward the hot spot. If another junction site reaches its turnover temperature, then another filament will be initiated. The number of filaments is found to depend on diode geometry and conditions of excitation. However, for a particular device and a particular excitation level, the filamentation pattern is highly reproducible.

Device voltage drops as the filaments grow across the n-region, with a further abrupt drop upon formation of the melt filament. If the amplitude of the exciting pulse (assuming constant pulse length) is increased slowly up to the melt transition, then only one melt filament will form. If an appreciable overstress is applied, then multiple filaments can form.

With thin film diodes, the mass of material involved is so small that the events between filament initiation and melt formation occur very rapidly. Thus, in high resistivity diodes, the transition to filaments from nearly uniform conduction occurs during a few nanoseconds, too rapidly to be experimentally resolved. In high resistivity diodes, the n-region reaches the turnover point before the junction. Thus the

junction ballasts the n-region. Current filamentation can occur before the junction region turnover is reached since the hotter portions of the n-region will reach their turnover first and then carry a larger portion of the current as their resistance decreases. This in turn will bring additional current through the local junction region and cause this region to rapidly reach turnover. Ultimate failure is still by formation of a melt filament.

Returning to the waveforms of Fig. 24, a slight voltage drop near the end of the voltage waveform is observed. This voltage drop is a good indication that the diode is on the verge of destructive second breakdown. Near the second breakdown threshold, the n-region current distribution is critically dependent on the pulse amplitude, and it is often difficult to observe hot spots before the melt filaments of destructive second breakdown occur. The post-test I-V characteristic in Fig. 24 indicates that no damage occurred as a result of the high amplitude current pulses.

The type of damage produced by the second breakdown transition is shown in Fig. 27. A series of current pulses of increasing amplitude were applied to the diode in Fig. 23 and Fig. 24. The corresponding voltage waveforms are shown in Fig. 27a. Destructive second breakdown occurs near the end of the highest amplitude voltage waveform. A zero bias photograph taken after the highest amplitude waveform in Fig. 27a is shown in Fig. 27d, revealing a melt filament slightly to the right of the center of the n-region. An I-V characteristic corresponding to Fig. 27d is shown in the lower left portion of the figure. The reverse bias breakdown voltage has been reduced to about 10 V, instead of 12 V.

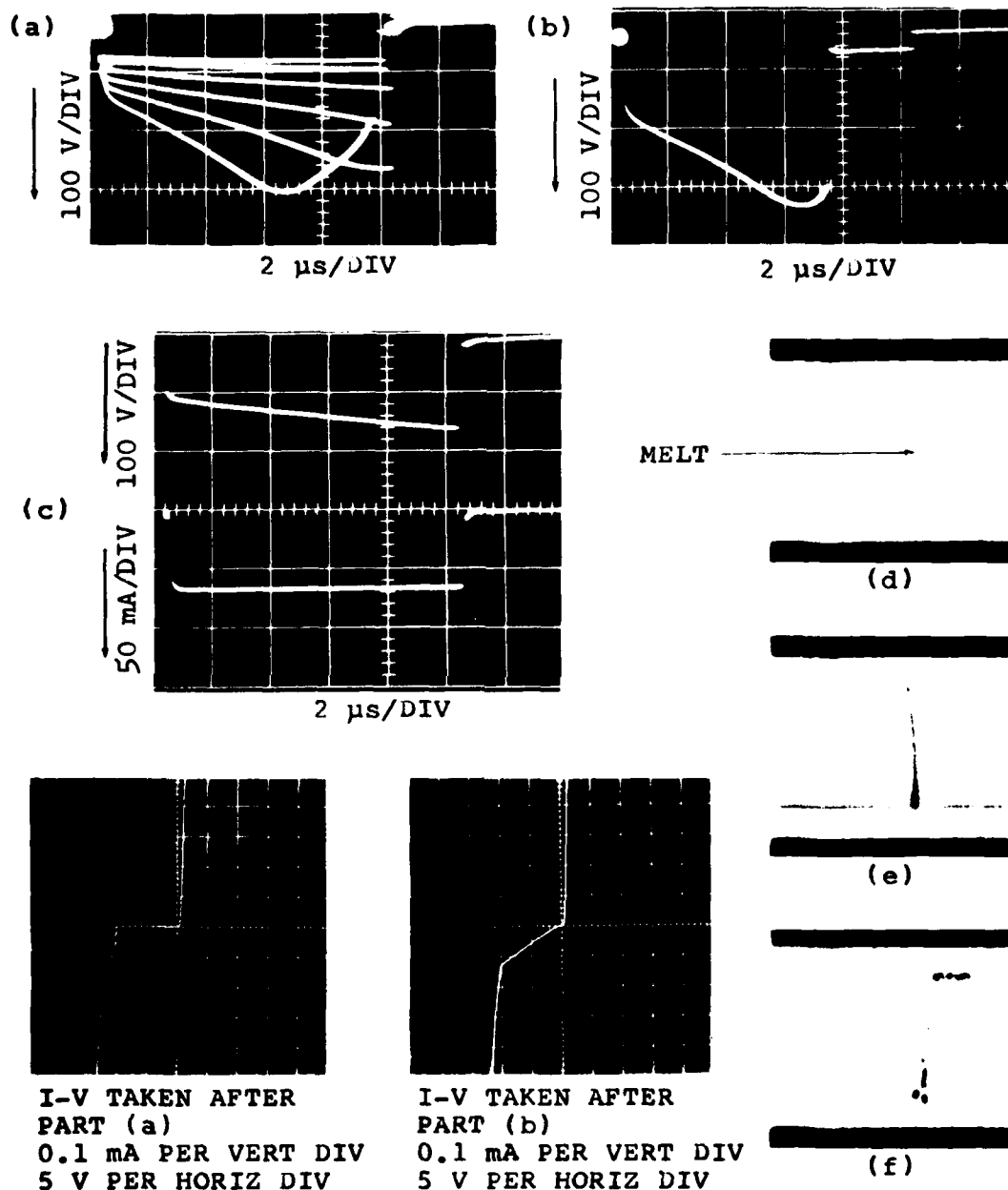


Fig. 27. Second breakdown in the diode in Figs. 23 and 24. (a) Voltage waveforms--second breakdown occurs near the end of the highest amplitude waveform. (b) Repeat of the highest amplitude waveform in part (a). (c) Voltage and current waveforms after second breakdown. (d) Zero bias, after part (a). (e) Heating pattern at the end of the waveforms in part (c). (f) Zero bias, showing damage produced by several hundred high amplitude pulses. I-V characteristics after part (a) and part (b) are also shown.

A second current pulse, at exactly the same amplitude that caused the melt filament in Fig. 27d was then applied to the diode. The corresponding voltage waveform is shown in Fig. 27b, and an I-V characteristic taken after Fig. 27b is shown in the lower portion of the figure. This I-V characteristic indicates that the diode behaves approximately as an 8 k Ω resistor under reverse bias from 0 to about 10 V.

Subsequent to Fig. 27b, the diode was again observed under electrical stress. The current and voltage waveforms are shown in Fig. 27c, and the heating pattern at the end of the pulse is shown in Fig. 27e. There is a filament which extends completely across the n-region, at the same location as the melt filament in Fig. 27d, indicating that this filament behaves as a resistive shunt across the n-region. The current level is only slightly less than that in Fig. 24, but the peak of the voltage waveform is over 100 V less than the peak in Fig. 24. When the current was increased slightly above the level in Fig. 27c, the diode again went into second breakdown, but the waveform shape changed from pulse to pulse and there was additional damage to the n-region. The damage produced by several hundred pulses at an amplitude slightly higher than those in Fig. 27c is shown in Fig. 27f.

The properties of standard reference diodes will now be discussed in more general terms. Figure 28 shows results of reverse bias tests on five different standard reference diodes. All five are from Wafer 2-5, with n-region lengths of 30 μm and n-region widths of 200 μm . Each diode was electrically stressed to the threshold of second breakdown using constant current pulses. Current and voltage waveforms of two of the diodes are shown in the figure, labeled as "Test #1" and

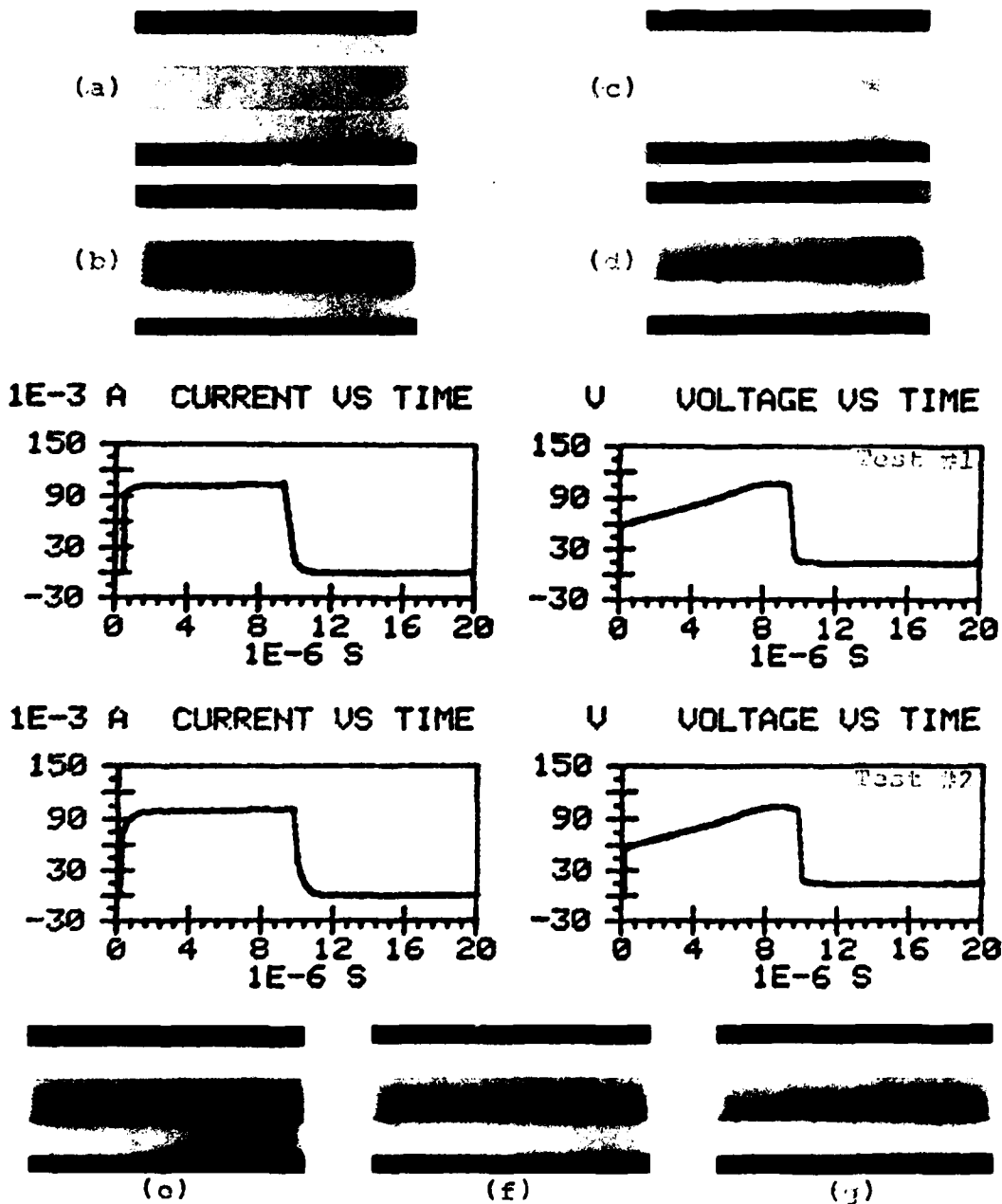


Fig. 28. Reverse bias tests of five different standard reference diodes on Wafer 2-5. (a) Zero bias photograph of the diode in Test #1. (b) Heating pattern at the end of Test #1. (c)-(d) Zero bias and heating pattern photographs of the diode in Test #2. (e)-(g) Diodes with four, five, and six hot spots along the junction, respectively.

"Test #2". The zero bias and heating pattern photographs of the diode in Test #1 are shown in Figs. 28a and 28b, respectively. Figures 28c and 28d show the corresponding photographs for Test #2. There are four hot spots along the p^+n junction in Fig. 28b. These are of different sizes and are nonuniformly spaced. There are also four nonuniformly spaced hot spots in Fig. 28d. Tests on other similar diodes show that the number of hot spots may vary from one to, say, eight. Diodes with four, five, and six nonuniformly spaced hot spots are shown in Figs. 28e-g, respectively.

One of the concerns of this study was to determine whether current and voltage waveforms could be used to anticipate the onset of current filamentation and destructive second breakdown. In a representative test sequence, such as that of Fig. 28, different numbers of hot spots form and the waveforms are very similar, giving no indication of the differences in n-region current distributions. In other tests, there are some differences in the amplitude of the current and voltage waveforms, but these variations have no apparent correlation with the number or location of hot spots on the p^+n junction. Thus, the n-region current distribution in standard reference diodes cannot be inferred from voltage and current waveforms.

For the diodes on Wafers 1-5, 2-5, 1-4, and 2-4 waveforms may sometimes be used to predict the onset of second breakdown. During the greater portion of the voltage waveforms shown in Test #1 and Test #2 of Fig. 28, the voltage increases linearly. This corresponds to an increase in resistivity of the n-region due to heating and an increase in the junction voltage with increasing temperature. Near the end of the

voltage waveforms there is a decrease in slope and a slight voltage drop, similar to that of Fig. 24f. As mentioned previously, this voltage drop is a good indication that the diode is close to the second breakdown threshold, because it always appears at a current level only slightly below that at which hot spots are first visible. However, the voltage drop is often difficult to observe because it occurs so close to the second breakdown threshold.

It is worthwhile at this point to mention one of the results of a previous study conducted by Budenstein, Pontius, and Smith.¹⁸ A group of diodes in that study were geometrically similar to the standard reference diodes of the present study, except for thickness. The present diodes were $0.4\text{ }\mu\text{m}$ thick while the earlier ones were $0.9\text{ }\mu\text{m}$ thick. It was thought that the two groups of diodes would behave in a similar manner. However, in that study, the hot spots were much more uniformly spaced along the p^+n junction. In addition, the number of hot spots could be systematically varied by changing the current level and pulse length. For a short pulse length ($5\text{ }\mu\text{s}$) and a high current level, thirty uniformly spaced hot spots were observed along the junction of a diode $500\text{ }\mu\text{m}$ wide, $75\text{ }\mu\text{m}$ in n -region length, and with a doping level of about $5 \times 10^{17}\text{ cm}^{-3}$. By increasing the pulse length and decreasing the current level, the number of hot spots could be continuously changed from thirty to one. The pulse length for one hot spot was 10 msec. In the present study, however, neither the number nor the location of the hot spots could be varied by adjusting the current level and pulse length. In the thinner devices, microscopic inhomogeneities may determine the filament configuration, while in thicker devices such inhom-

geneities are relatively unimportant and overall diode geometry at each excitation level may determine the filament configuration. The thinner devices would also be more effectively heat-sinked to their sapphire substrates.

Figure 29 shows reverse bias tests of three standard reference diodes on Wafer 2-5. The n-region lengths are, from top to bottom, 10, 30, and 100 μm , and the common diode width is 200 μm . Current and voltage waveforms are shown to the right of each heating pattern. The upper trace of each waveform pair is the voltage waveform, and the lower trace is the current waveform, as in Figs. 23, 24, and 27. Each of the three diodes is close to its second breakdown threshold.

The amplitude of the current waveform is similar for the three n-region lengths, between 70 and 80 mA. Thus, current densities are equivalent, ranging from 8.7×10^8 to 1.0×10^9 A/m². However, the amplitude of the voltage waveform increases considerably as the n-region length increases. This means that both the voltage and energy failure thresholds increase as n-region length increases. Failure thresholds will be discussed quantitatively in Section F.

One hot spot was observed on the p⁺n junctions in the diodes with 30 and 100 μm n-region lengths, while no hot spot (uniform heating) was observed in the n-region of the diode with the 10 μm n-region length. Hot spot formation in standard reference diodes with n-region lengths of 10 μm is very difficult to observe because the current interval between hot spot formation and second breakdown is so narrow that the diode cannot be maintained within that interval long enough to complete a test.

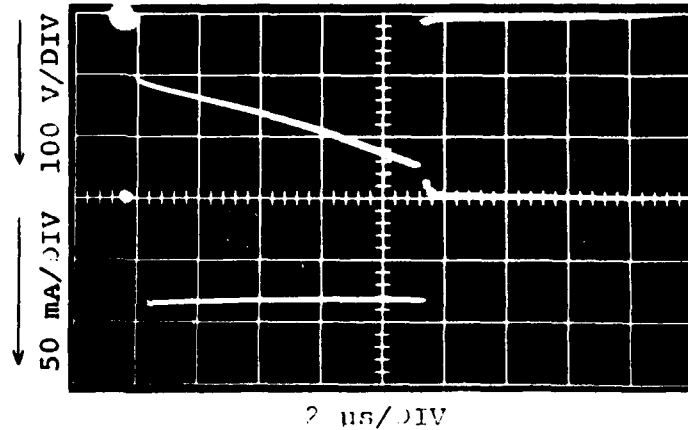
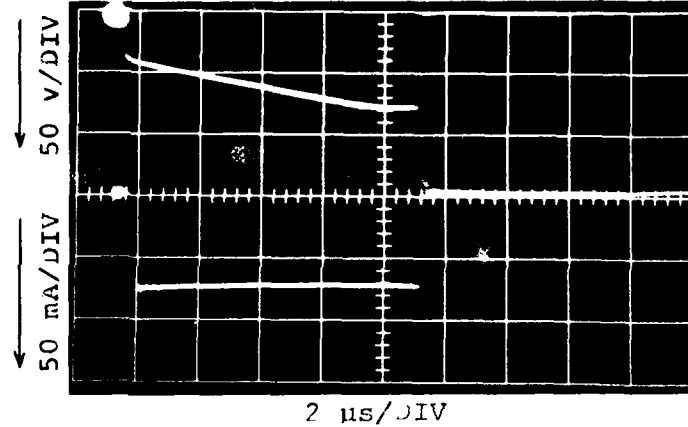
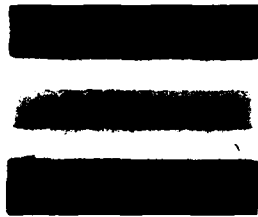
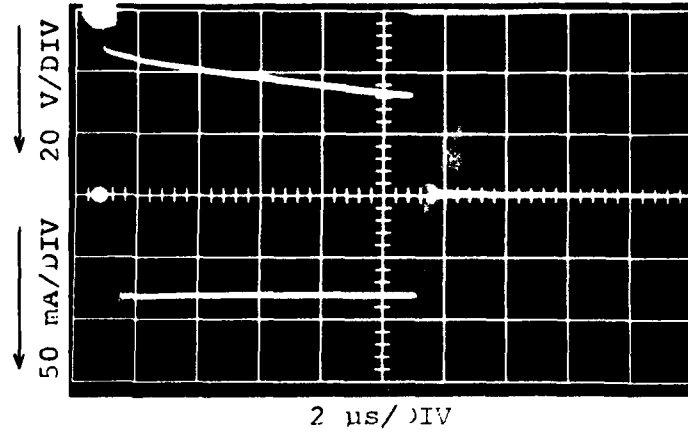


Fig. 29. Reverse bias tests of three standard reference diodes on Wafer 2-5. The n-region lengths are, from top to bottom, 10, 30, and 100 μm . Voltage (upper trace) and current (lower trace) waveforms are shown for each case.

Before proceeding, several general comments should be made concerning forward bias heating patterns, and the role of n-region doping level.

The heating of the n-region tends to be generally uniform under forward bias. However, if the current level is sufficiently close to the second breakdown threshold, then single or multiple filaments may form. These filaments extend most of the way across the n-region, and are usually rather broad compared to the reverse bias hot spots. Forward bias characteristics will be described in more detail during the special test discussion in Section J.

The heating pattern photographs in Figs. 23, 24, 27, 28, and 29 were obtained from diodes on Wafer 2-5. Heating pattern photographs of diodes on Wafer 2-4 show much less darkening at the second breakdown threshold, both of the p^+n junction and the n-region. This occurs because silicon reaches the peak of its resistivity-temperature curve at lower temperatures as the doping density decreases. In addition, the current interval between hot spot formation and second breakdown is narrower, making it more difficult to photograph the hot spots. The narrower current interval results from a stronger dependence of resistivity on temperature at lower doping densities; a small increase in temperature at the peak of the resistivity-temperature curve produces a large decrease in resistivity. If the nominal n-region doping level is less than 10^{17} cm^{-3} , then the darkening of the p^+n junction and the n-region at the second breakdown threshold is very faint. The current interval between hot spot formation and second breakdown is so narrow

that no hot spots have been observed. However, the failure mode, as indicated by the damage morphology, is by formation of a melt filament.

B. Diffusion Spike Diodes (p^+n Junction)

This section describes the heating patterns of diodes having a single spike of 2.5 or 5 μm length located on the p^+n junction. The heating patterns near the second breakdown threshold of three p^+n spike diodes on Wafer 2-5 are shown in Fig. 30. The n -region lengths of these diodes are 10, 30, and 100 μm , from top to bottom. Current and voltage waveforms are shown to the right of the heating pattern photographs.

The spike, which is 5 μm in length, is located on the right side of the 10 and 100 μm n -region length diodes, and on the left side of the 30 μm n -region length diode. There is a single hot spot which forms at the tip of the spike for all three n -region lengths. Observations of other diodes with a single p^+n spike show that a hot spot always forms at the tip of the spike and that there are never multiple hot spots. The same observations also apply to diodes with a 2.5 μm spike. Thus, the spike is very effective in localizing the position at which a hot spot forms and in limiting the number of hot spots to one.

The length of the hot spots in Fig. 30 tends to increase as the n -region length increases. Although somewhat longer hot spots than the ones shown here can be observed, the probability of destroying the diode during the test is increased. Hot spots extending more than 3/4 of the way across the n -region have been observed prior to destructive second breakdown.

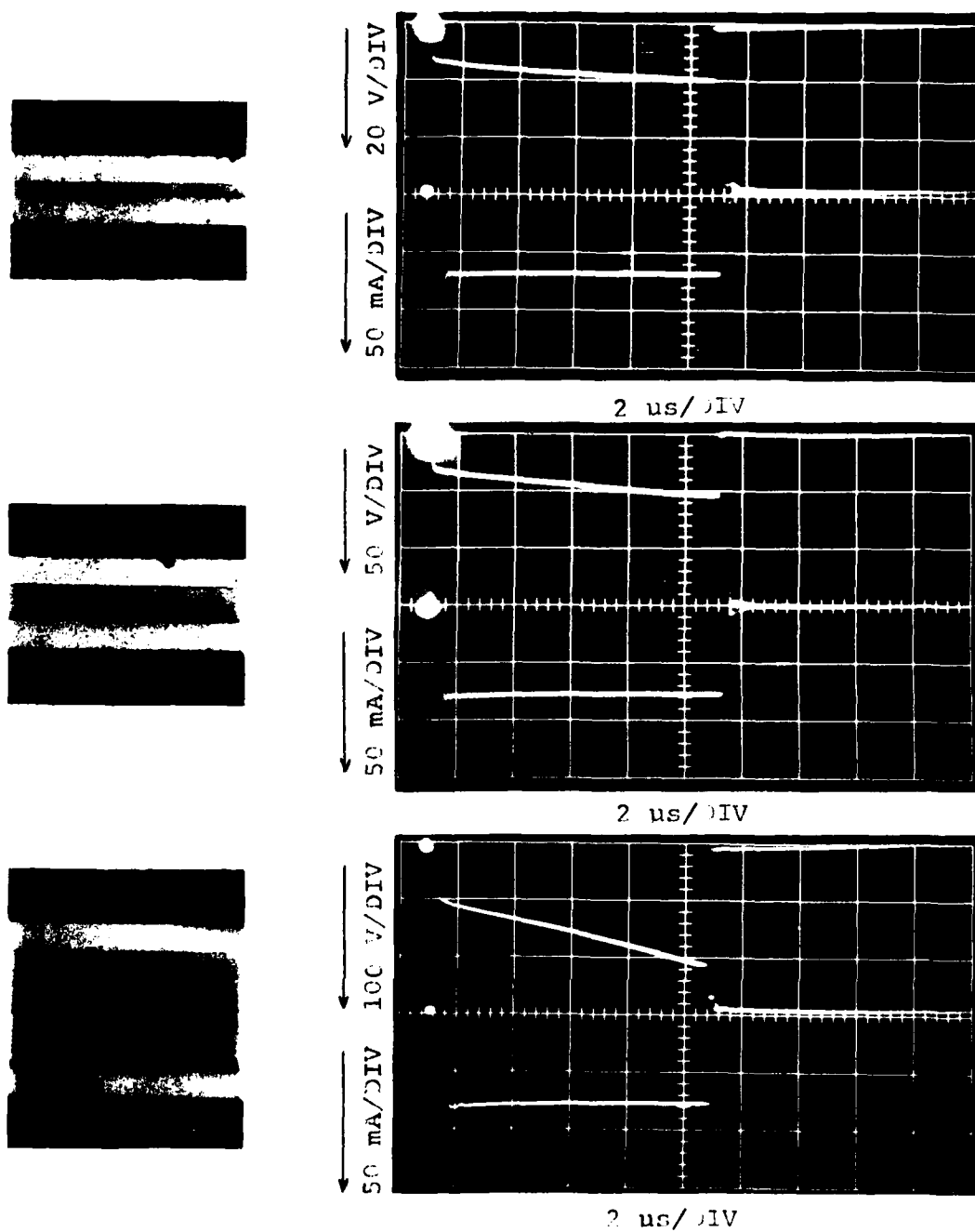


Fig. 30. Reverse bias tests of three p^+n spike diodes on Wafer 2-5. The n -region lengths are, from top to bottom, 10, 30, and 100 μ m. Voltage (upper trace) and current (lower trace) waveforms are shown for each case.

Comments concerning the amplitude of the current and voltage waveforms are similar to those made in connection with the standard reference diodes shown in Fig. 29. Hot spots also form at the tip of the p^+n diffusion spike in diodes on Wafer 2-4. However, for lower doping densities the effect of the spike on the n-region current distribution was not determined because the darkening at the second breakdown threshold is so faint. However, the damage filament occurred at the spike location.

C. Diffusion Spike Diodes (n^+n Junction)

This section describes the heating patterns of diodes having a single spike on the n^+n junction, with a length of either 2.5 or 5 μm . The heating patterns near the second breakdown threshold of three n^+n spike diodes on Wafer 2-5 are shown in Fig. 31. The n-region lengths, widths, and doping levels are the same as for the diodes in Fig. 29 and Fig. 30. Current and voltage waveforms are shown to the right of the heating pattern photographs.

The spikes, for the diodes of Fig. 31, are 5 μm in length, are located on the right side of the 10 and 100 μm n-region length diodes, and on the left side of the 30 μm n-region length diode. The heating of the p^+n junction and the n-region appears fairly uniform for all three n-region lengths. A spot of surface debris on the left side of the 100 μm n-region length diode should not be confused with a hot spot. Observations of other diodes with a single n^+n spike show that the heating of the p^+n junction and the n-region is always very uniform until the diode is quite close to the second breakdown threshold. The

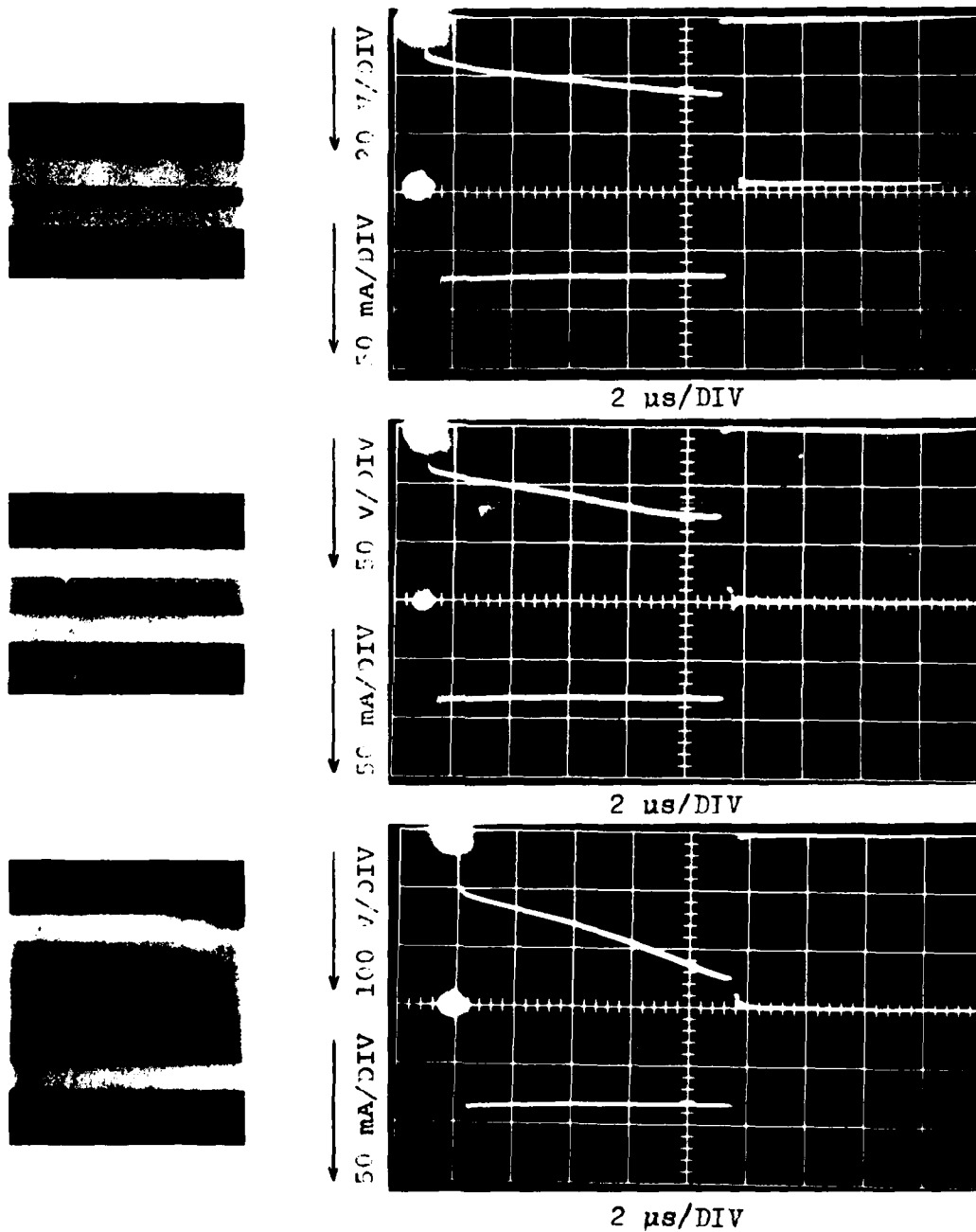


Fig. 31. Reverse bias tests of three n^+n spike diodes on Wafer 2-5. The n-region lengths are, from top to bottom, 10, 30, and 100 μm . Voltage (upper trace) and current (lower trace) waveforms are shown for each case.

current interval between hot spot formation and second breakdown is much narrower for diodes with an n^+n spike than for diodes with a p^+n spike. If the current is increased sufficiently, then a single hot spot forms on the p^+n junction at a point which is usually opposite, or nearly opposite, the n^+n spike. Multiple hot spots have not been observed in diodes with a single n^+n spike. Similar observations also apply to diodes with a $2.5\text{ }\mu\text{m}$ spike. Thus, the n^+n spike limits the number of hot spots to one and influences the hot spot location, although its effect is not observed until the diode is very close to the second breakdown threshold.

Comments concerning the amplitude of the current and voltage waveforms, and the effect of doping level on n-region darkening are similar to those made in connection with the standard reference diodes shown in Fig. 29. However, the formation of hot spots prior to second breakdown was not observed in diodes with an n-region doping density less than that of diodes on Wafer 2-5.

D. Contact Spike Diodes

Diodes with a single spike either 2.5 or $5\text{ }\mu\text{m}$ in length on the metal- p^+ and the metal- n^+ interfaces were also studied; these were referred to as "contact spike diodes." However, there were no discernable differences between the heating patterns of diodes with contact spikes and standard reference diodes. In addition, there were no observable differences between the current and voltage failure thresholds of contact spike and standard reference diodes at any of the five nominal doping levels. Thus, the presence of a contact spike appears to have

no effect on a diode's susceptibility to second breakdown. One minor effect of contact spikes will be mentioned in section V.F.3.

E. Enclosed Reference Diodes

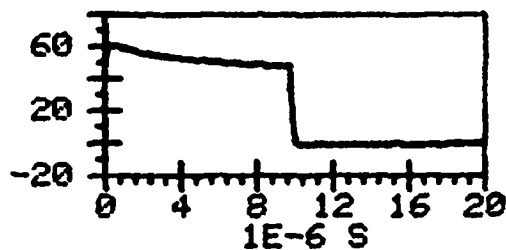
This section describes the heating patterns observed in enclosed reference diodes. In these diodes, the p^+n and n^+n junctions are entirely surrounded by the n-region. Reverse bias tests of two enclosed reference diodes on Wafer 2-5 are shown in Fig. 32. The tests were performed using 10 μs constant voltage pulses which were applied to the series combination of the diode and a current-measuring resistor. A decrease in current during the pulse corresponds to an increase in diode impedance.

The zero bias and heating pattern photographs of one of the diodes are shown in Fig. 32a and 32b, respectively. Figure 32c and 32d show the zero bias and heating pattern photographs of the other diode. The waveforms corresponding to Fig. 32b and 32d are shown in Test #1 and Test #2, respectively. Both of the diodes are fairly close to the second breakdown threshold.

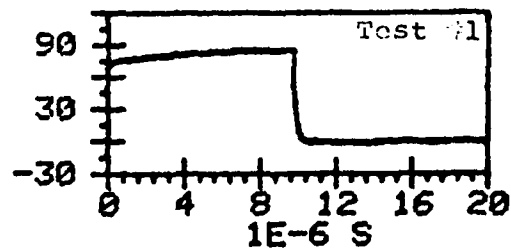
The diode in Test #1 has an n-region length of 30 μm and an n-region width of 110 μm . The width of the p^+n and n^+n junctions is 50 μm , roughly half the n-region width. The n-region heating between the two junctions is fairly uniform in Fig. 32b, but two hot spots have formed on the corners of the protruding portion of the p^+n junction. The dimensions of the diode in Test #2 are the same as the diode in Test #1, except that the length of the n-region in Test #2 is 100 μm . Again, the n-region heating between the protrusions of the two junctions is fairly uniform except for the two hot spots that have formed



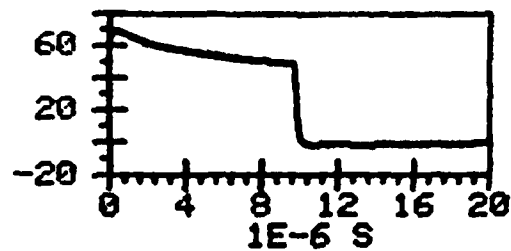
1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME



1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME

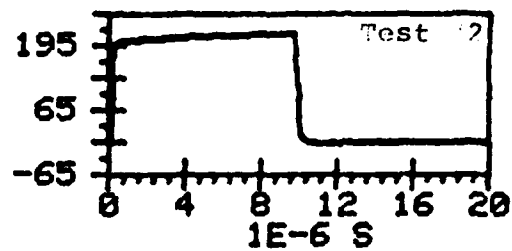


Fig. 32. Reverse bias tests of two enclosed reference diodes on Wafer 2-5. (a)-(b) Zero bias and heating pattern photographs of the diode in Test #1. (c)-(d) Zero bias and heating pattern photographs of the diode in Test #2.

at the corners of the p^+n junction protrusion. These corners of the p^+n junction serve as significant concentration centers for the current, whereas the corners close to the diode edges do not.

The current waveforms of Test #1 and Test #2 are similar, indicating the current densities in the n-regions are distributed in a similar manner for the two n-region lengths. The darkening of the n-region in front of the protrusions is comparable to that of the standard reference and diffusion spike diodes close to their thresholds, so all current densities should be similar. The amplitude of the voltage waveform is much larger in Test #2 than Test #1 because of the increased n-region length in Test #2. This is in agreement with the behavior of the standard reference, diffusion spike, and contact spike diodes already described.

Observations of other enclosed reference diodes show that the corners are less effective in localizing the current distribution when the junction width is a larger fraction of the n-region width. Hot spots may form along the p^+n junction as well as at the protruding corners of the junction. Or hot spots may form along the p^+n junction, with no hot spots at the junction corners.

F. Comparison of Standard Reference, Enclosed Reference, p^+n Spike, and n^+n Spike Diodes

The data presented in this section provide a more quantitative understanding of current filamentation in silicon-on-sapphire diodes than the heating pattern photographs described above. A discussion of energy failure thresholds, voltage failure thresholds, and damage morphology as functions of geometry and doping level is given below.

1. Energy Threshold Analysis

One goal of this study was to evaluate the effect of diffusion spikes on failure energy thresholds. It was anticipated that spikes on either the p^+n or the n^+n junction would reduce the failure thresholds. However, the magnitude of the reduction, and the effects of n-region length, width, and doping level were not known.

The term "failure energy," as it is used here, refers to the energy input necessary to cause second breakdown. If second breakdown occurs before the end of the pulse, then subsequent energy input to the diode is not included in the failure energy. The second breakdown transition is generally quite sharp, so there is no difficulty in determining when it occurs.

In several of the tests of diodes of Wafer 2-5, the voltage and current waveforms indicated the typical change of device impedance that occurs during the second breakdown melt transition. This abrupt change in device impedance corresponded to the growth of a filament completely across the n-region. However, examination of the diodes after repeated exposure to pulse excitation revealed no evidence of filament damage and no changes in I-V characteristics. These diodes all had n-region lengths of 10 and 30 μm , and the two shortest n-region widths, 30 and 50 μm . The current level for this non-destructive second breakdown threshold (which was found to be roughly proportional to n-region width) is not sufficient to form a melt filament. The voltage turnover occurred at a current density of about $1.2 \times 10^9 \text{ A/m}^2$. However, these special geometries are not discussed here. The failure energies described below were recorded during the pulse which damaged the diode's

I-V characteristics. All of the tests were done with constant current pulses 10 μ s in length. The diffusion spike length was 5 μ m.

Figure 33 shows the failure energy thresholds of standard reference and diffusion spike diodes on Wafer 2-5. The n-region width of all these diodes is 200 μ m. The first column shows standard reference diodes, while the second and third columns show p^+n and n^+n spike diodes, respectively. There are three rows which represent, from top to bottom, diodes with n-region lengths of 10, 30, and 100 μ m.

Two energies are shown for most of the diodes tested. The open circles show the total energy input to the diode during the maximum amplitude non-destructive pulse. The closed circles show the failure energy. The individual diodes are displaced horizontally for clarity.

Each of the nine groups of diodes shown here exhibits a range of failure and pre-failure energies. In some cases the failure energy is larger than the pre-failure energy; in other cases the reverse is true. If the failure energy is lower than the pre-failure energy, the increase in pulse amplitude of the failure pulse caused failure to occur early in the pulse. Once a critical current threshold had been exceeded, a small further increase tended to have a large effect in reducing the delay time to second breakdown. Thus, the higher of the two energies may be the more useful quantity for comparing failure thresholds.

Comparison of the energy scales in Fig. 33 shows that failure energies tend to increase as n-region length increases, for both standard reference and diffusion spike diodes. In Fig. 34, the failure energy threshold is plotted as a function of n-region length for standard

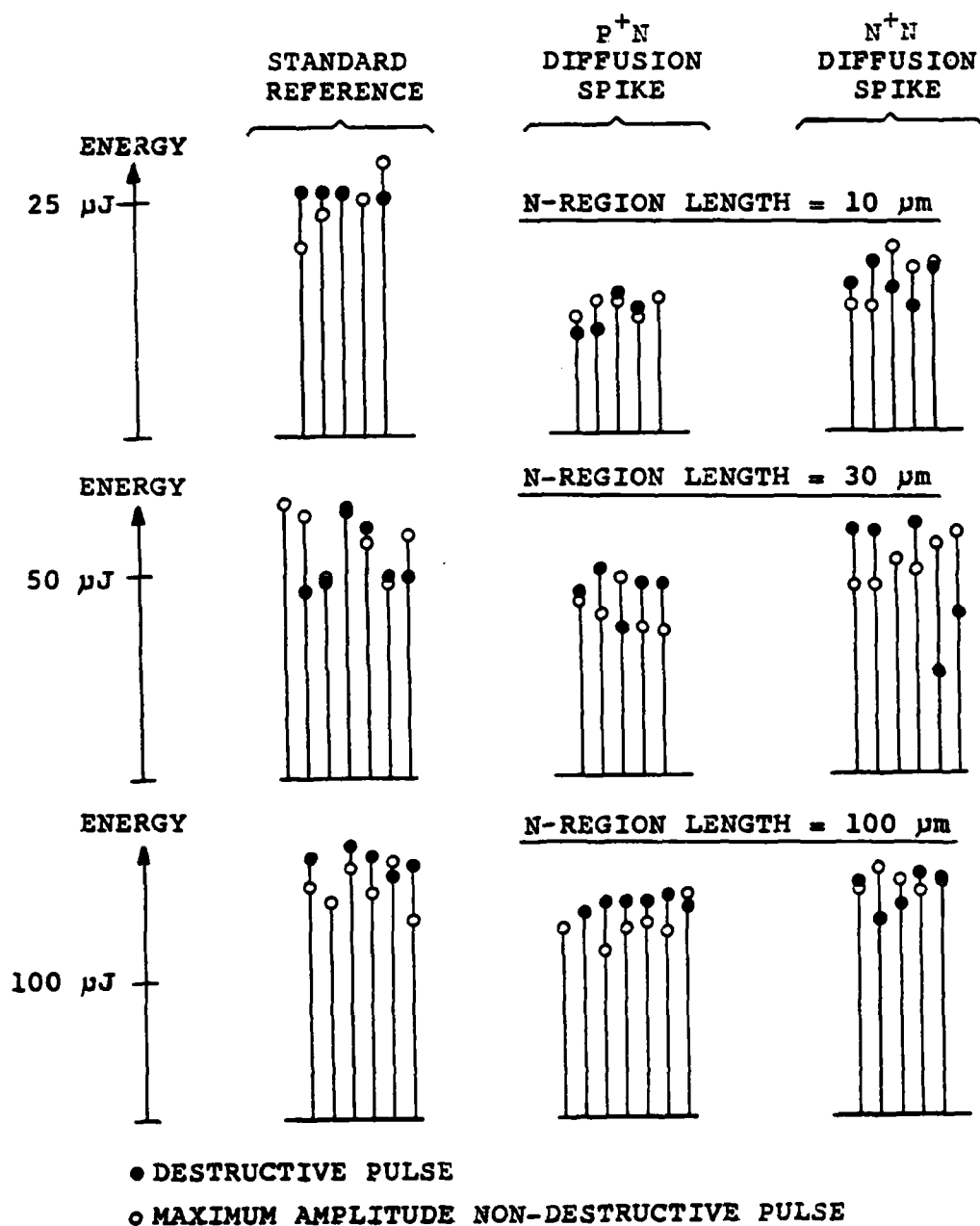


Fig. 33. Total energy input at the second breakdown threshold. These diodes are from Wafer 2-5, and have an n-region width of 200 μm .

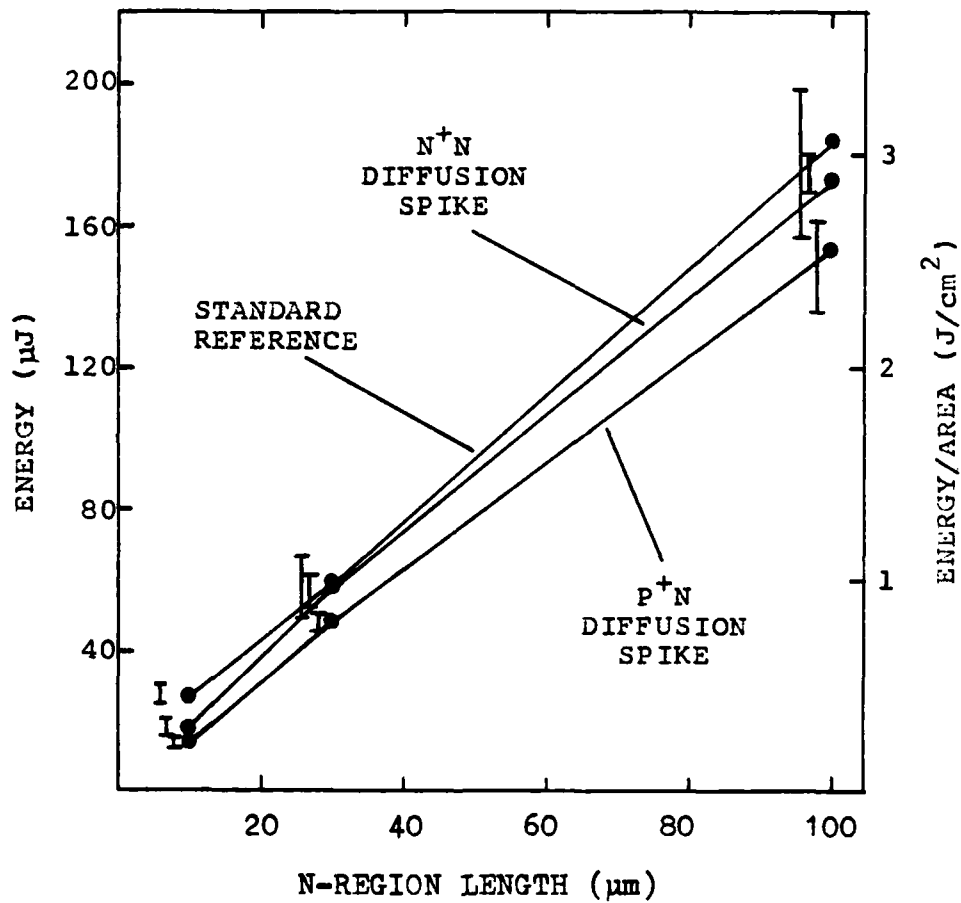


Fig. 34. Total energy input at the second breakdown threshold versus n-region length for standard reference and diffusion spike diodes on Wafer 2-5. Error bars show the maximum and minimum of the measurements.

reference, p^+n spike, and n^+n spike diodes. The individual points in Fig. 34 were obtained by averaging the higher of the failure and pre-failure energies in Fig. 33. Error bars show the maximum and minimum energies included in the average. The size of these overlapping error bars illustrates why it is not feasible to observe general trends from individual measurements.

The diffusion spikes significantly lower the failure energy thresholds of diodes with an n-region length of 10 μm . Diffusion spikes also tend to lower the failure energy thresholds of diodes with longer n-region lengths if they are located on the p^+n junction. However, spikes on the n^+n junction have relatively minor effect on the failure thresholds at longer n-region lengths.

The failure threshold energy increases approximately linearly with n-region length for each of the three curves. Standard reference diodes tend to have the highest failure energy thresholds, while p^+n spike diodes tend to have the lowest. It appears that the major factor affecting failure energy thresholds is the n-region length, while diffusion spikes play a secondary role.

A summary of the pre-failure and failure energies measured on Wafer 2-5, and also on Wafers 2-4 and 2-1, is given in Tables 4 and 5. These tables show the average of the pre-failure and failure energies, and the maximum and minimum energies included in the averages.

Since the energy threshold data were obtained with constant current pulses, they also describe current, or current density, failure thresholds. Figure 35 shows the current failure thresholds of standard reference and diffusion spike diodes on Wafer 2-5 with n-region widths

TABLE 4.--Numerical values of the pre-failure and failure energies of diodes on Wafers 2-5 and 2-4 with n-region widths of 200 μm . Each pre-failure and failure energy is the average of about five measurements. The maximum and minimum energies included in the average are also shown.

FAILURE THRESHOLDS OF DIODES ON WAFER 2-5 WITH AN N-REGION WIDTH OF 200 μm							
	N-REGION LENGTH (μm)	ENERGY (μJ)					
		PRE-FAILURE			FAILURE		
DIODE TYPE		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	25	29	20	26	26	25
P ⁺ N SPIKE	10	13	14	12	13	15	11
N ⁺ N SPIKE	10	16	20	13	16	18	13
STAN. REF.	30	59	67	47	53	65	46
P ⁺ N SPIKE	30	41	49	36	45	51	36
N ⁺ N SPIKE	30	52	59	46	49	62	25
STAN. REF.	100	167	187	144	187	198	176
P ⁺ N SPIKE	100	138	161	121	155	160	149
N ⁺ N SPIKE	100	169	179	163	162	175	142

FAILURE THRESHOLDS OF DIODES ON WAFER 2-4 WITH AN N-REGION WIDTH OF 200 μm							
	N-REGION LENGTH (μm)	ENERGY (μJ)					
		PRE-FAILURE			FAILURE		
DIODE TYPE		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	24	30	8	27	31	23
P ⁺ N SPIKE	10	11	13	9	11	14	7
N ⁺ N SPIKE	10	12	13	11	4	7	1
STAN. REF.	30	51	56	46	52	60	48
P ⁺ N SPIKE	30	27	30	24	29	33	22
N ⁺ N SPIKE	30	25	33	11	11	30	5

TABLE 5.--Numerical values of the pre-failure and failure energies of diodes on Wafer 2-4 with n-region widths of 30 μm , and of diodes on Wafer 2-1 with n-region widths of 200 μm . Each pre-failure and failure energy is the average of about five measurements. The maximum and minimum energies included in the average are also shown.

FAILURE THRESHOLDS OF DIODES ON WAFER 2-4 WITH AN N-REGION WIDTH OF 30 μm							
		ENERGY (μJ)					
		PRE-FAILURE			FAILURE		
DIODE TYPE	N-REGION LENGTH (μm)	AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	3.2	3.8	3.1	3.5	3.8	3.0
P ⁺ N SPIKE	10	1.8	2.2	1.3	1.9	2.1	1.5
N ⁺ N SPIKE	10	1.8	2.1	1.5	1.3	2.1	0.5
STAN. REF.	30	4.9	5.9	4.1	6.7	7.4	6.6
P ⁺ N SPIKE	30	3.9	5.8	2.9	4.5	5.9	2.4
N ⁺ N SPIKE	30	3.8	4.8	2.2	3.7	4.9	1.9

FAILURE THRESHOLDS OF DIODES ON WAFER 2-1 WITH AN N-REGION WIDTH OF 200 μm							
		ENERGY (μJ)					
		PRE-FAILURE			FAILURE		
DIODE TYPE	N-REGION LENGTH (μm)	AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	4.4	6.7	0.3	3.1	6.0	0.6
P ⁺ N SPIKE	10	-	-	-	0.04	0.08	0.03
N ⁺ N SPIKE	10	-	-	-	0.02	0.03	0.01
STAN. REF.	30	9.3	17.8	1.2	7.0	18.3	1.8
P ⁺ N SPIKE	30	4.3	10.9	1.6	2.9	7.6	0.8
N ⁺ N SPIKE	30	2.4	6.2	0.3	2.3	5.5	0.4

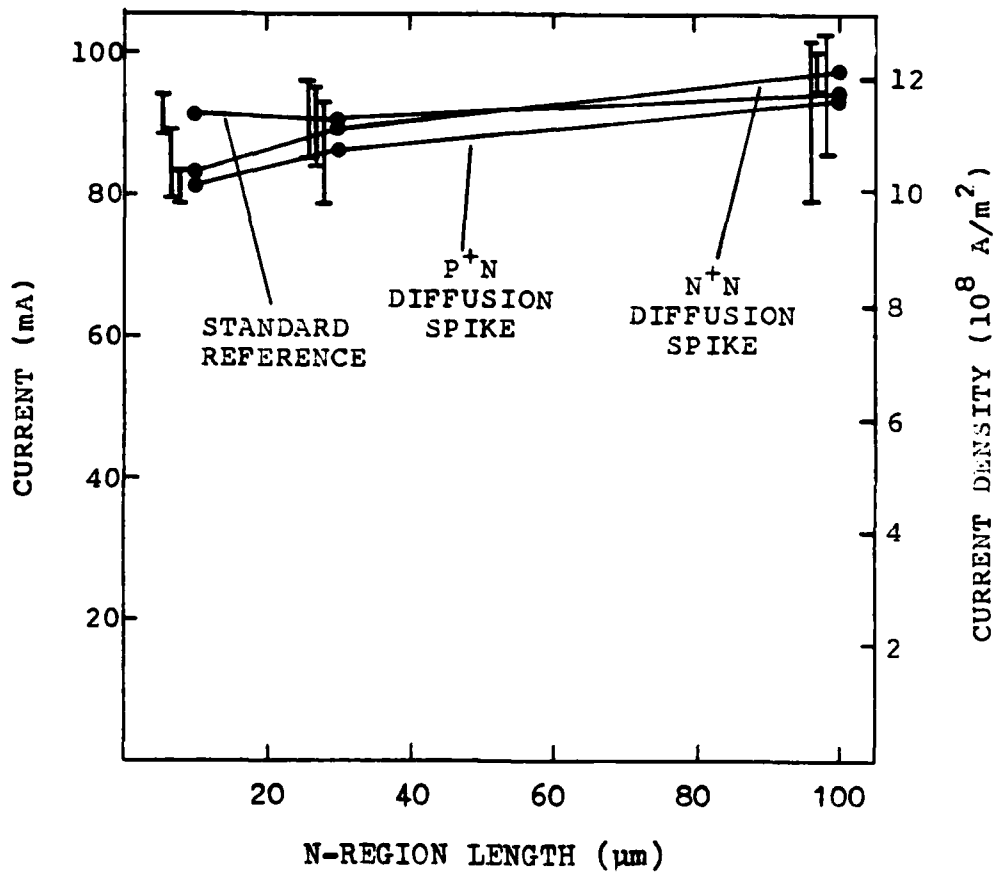


Fig.35. Current amplitude at the second breakdown threshold versus n-region length for standard reference and diffusion spike diodes on Wafer 2-5. Error bars show the maximum and minimum of the measurements.

of 200 μm , the same group as in Fig. 33 and Fig. 34. The three curves are almost horizontal, indicating that the diodes fail at a current density on the order of 10^9 A/m^2 , regardless of n-region length or diffusion spikes.

A summary of the current and current density failure thresholds measured on Wafers 2-1, 2-4, and 2-5 is given in Tables 6 and 7. These tables show the average current and current density failure thresholds, and the maximum and minimum values included in the averages.

Another concern is the effect of n-region doping level on failure thresholds. Figure 36 shows the failure energy thresholds of diodes with an n-region width of 200 μm on Wafer 2-4. This diagram is similar to Fig. 33 except that data for diodes with n-region lengths of 100 μm are not included. The failure threshold energy range of standard reference diodes lies well above the ranges of p^+n and n^+n spike diodes for both n-region lengths. Thus, both types of diffusion spikes seem to be effective in reducing the failure thresholds. Note that the pre-failure energies of the p^+n and n^+n spike diodes are roughly comparable, whereas the failure energies are not. Failure tended to occur earlier in the pulse for the n^+n spike diodes. This may be associated with the relatively low turnover temperature of the n-region resistivity-temperature curve, with the p^+n junction voltage remaining high.

As the n-region length increases from 10 to 30 μm the energy failure thresholds also increase, roughly a factor of two for both standard reference and diffusion spike diodes. Thus, the n-region length is a major factor in determining failure energy thresholds on Wafer 2-4 and

TABLE 6.--Numerical values of the current and current density failure thresholds of diodes on Wafers 2-5 and 2-4 with n-region widths of 200 μm . Each failure threshold is the average of about five measurements. The maximum and minimum values included in the average are also shown.

CURRENT FAILURE THRESHOLDS OF DIODES ON WAFER 2-5 WITH AN N-REGION WIDTH OF 200 μm							
DIODE TYPE	N-REGION LENGTH (μm)	CURRENT (mA)			CURRENT DENSITY (10^8 A/m^2)		
		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	91.2	93.7	88.5	11.4	11.7	11.1
P ⁺ N SPIKE	10	81.3	82.9	78.8	10.2	10.4	9.9
N ⁺ N SPIKE	10	82.9	89.1	79.4	10.4	11.1	9.9
STAN. REF.	30	90.0	95.5	84.8	11.3	11.9	10.6
P ⁺ N SPIKE	30	86.0	92.4	78.5	10.8	11.6	9.8
N ⁺ N SPIKE	30	89.0	94.4	83.8	11.1	11.8	10.5
STAN. REF.	100	93.7	101.0	79.0	11.7	12.6	9.9
P ⁺ N SPIKE	100	92.5	102.0	85.1	11.6	12.8	10.6
N ⁺ N SPIKE	100	97.1	99.4	94.1	12.1	12.4	11.8

CURRENT FAILURE THRESHOLDS OF DIODES ON WAFER 2-4 WITH AN N-REGION WIDTH OF 200 μm							
DIODE TYPE	N-REGION LENGTH (μm)	CURRENT (mA)			CURRENT DENSITY (10^8 A/m^2)		
		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	31.6	34.0	29.7	3.95	4.25	3.71
P ⁺ N SPIKE	10	21.7	23.0	21.0	2.71	2.88	2.63
N ⁺ N SPIKE	10	22.9	24.6	22.0	2.86	3.08	2.75
STAN. REF.	30	31.8	37.3	29.0	3.98	4.66	3.63
P ⁺ N SPIKE	30	24.2	25.6	21.4	3.03	3.20	2.68
N ⁺ N SPIKE	30	24.9	29.6	22.3	3.11	3.70	2.79

TABLE 7.--Numerical values of the current and current density failure thresholds of diodes on Wafer 2-1 with n-region widths of 200 μm , and of diodes on Wafer 2-4 with n-region widths of 30 μm . The maximum and minimum values included in the average are also shown.

CURRENT FAILURE THRESHOLDS OF DIODES ON WAFER 2-1 WITH AN N-REGION WIDTH OF 200 μm							
DIODE TYPE	N-REGION LENGTH (μm)	CURRENT (mA)			CURRENT DENSITY (10^8 A/m^2)		
		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	5.29	9.45	2.26	0.66	1.18	0.28
P ⁺ N SPIKE	10	0.70	0.87	0.46	0.09	0.11	0.06
N ⁺ N SPIKE	10	0.90	0.98	0.81	0.11	0.12	0.06
STAN. REF.	30	5.90	12.80	2.06	0.74	1.60	0.26
P ⁺ N SPIKE	30	3.45	5.92	2.10	0.43	0.74	0.26
N ⁺ N SPIKE	30	2.90	6.18	0.89	0.36	0.77	0.11

CURRENT FAILURE THRESHOLDS OF DIODES ON WAFER 2-4 WITH AN N-REGION WIDTH OF 30 μm							
DIODE TYPE	N-REGION LENGTH (μm)	CURRENT (mA)			CURRENT DENSITY (10^8 A/m^2)		
		AVG.	MAX.	MIN.	AVG.	MAX.	MIN.
STAN. REF.	10	5.00	5.59	4.56	4.17	4.66	3.80
P ⁺ N SPIKE	10	3.60	4.02	3.40	3.00	3.35	2.83
N ⁺ N SPIKE	10	3.64	4.07	2.85	3.03	3.39	2.38
STAN. REF.	30	5.30	5.80	4.88	4.42	4.83	4.07
P ⁺ N SPIKE	30	4.95	5.23	4.26	4.13	4.36	3.55
N ⁺ N SPIKE	30	4.28	4.47	4.01	3.57	3.73	3.34

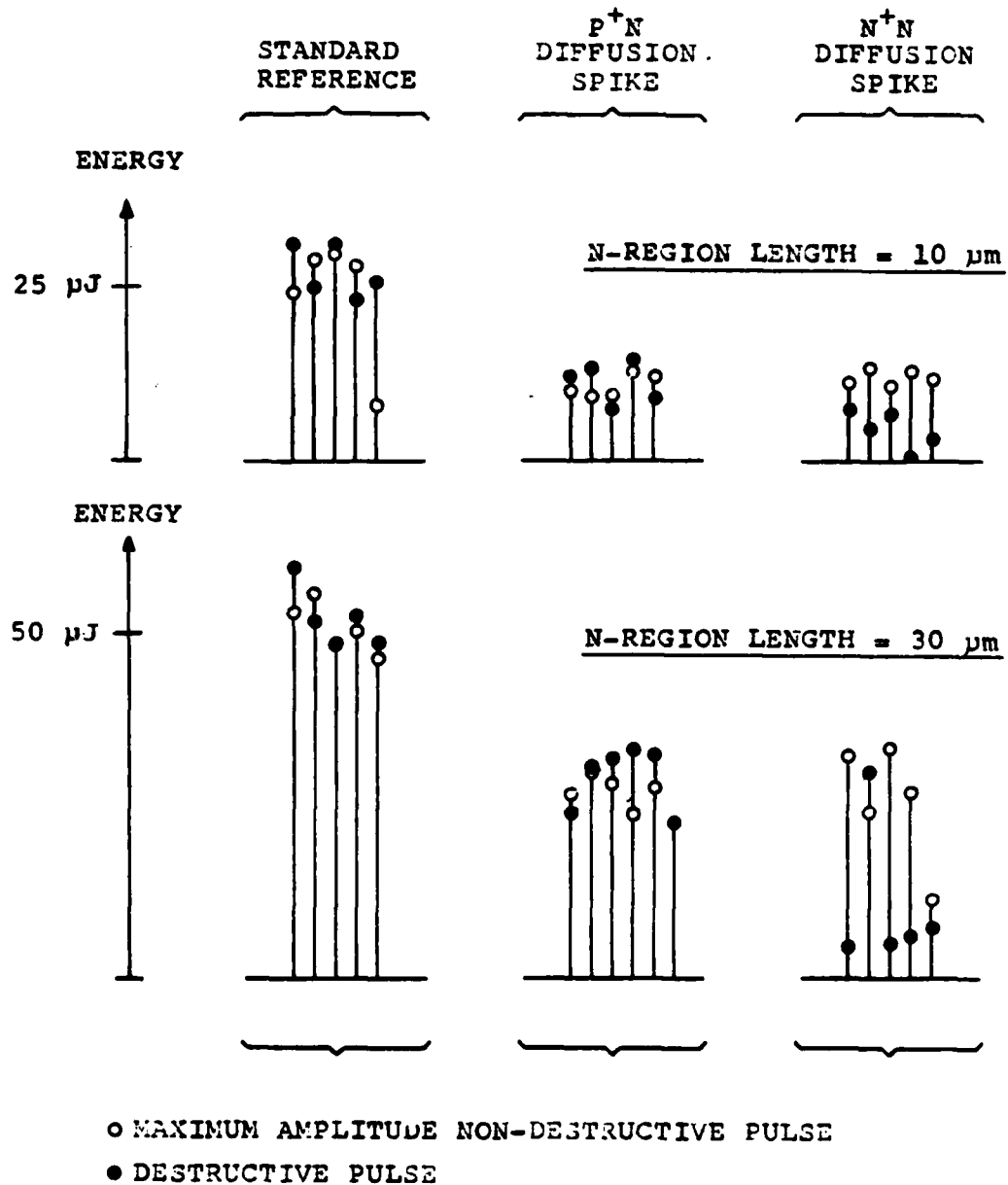


Fig. 36. Total energy input at the second breakdown threshold. These diodes are from Wafer 2-4, and have an n-region width of 200 μm.

Wafer 2-5. Current densities at the failure thresholds are presented in Tables 6 and 7.

The failure thresholds shown in Fig. 36 were obtained from diodes with an n -region width of 200 μm . However, in the diffusion spike diodes, only a small part of this width is occupied by the spike. The spikes are 5 μm in length and about 6 μm wide at the base, so they cover only about 3% of the p^+n or n^+n junction width. If the total diode current at the failure threshold is much larger than the current which flows through the spike, then the spike may have a relatively small effect. Thus, it is important to determine whether the spikes exert a larger influence on failure thresholds when the n -region width is decreased.

The failure energy thresholds of diodes on Wafer 2-4 with an n -region width of 30 μm are shown in Fig. 37. Figure 37 is similar to Fig. 36 in all respects except for the n -region width and the energy scale. The diffusion spikes occupy about 20% of the total n -region width for these diodes.

Again, the failure threshold energy range of the standard reference diodes lies well above the ranges of the p^+n and n^+n spike diodes for the 10 μm n -region length. The failure thresholds of standard reference diodes with a 30 μm n -region length tend to be larger than those of corresponding diffusion spike diodes, but the difference is not quite as large as in Fig. 36. Thus, the n -region width seems to have little effect on the relative importance of diffusion spikes. The energy thresholds are proportional to the n -region width in Figs. 36

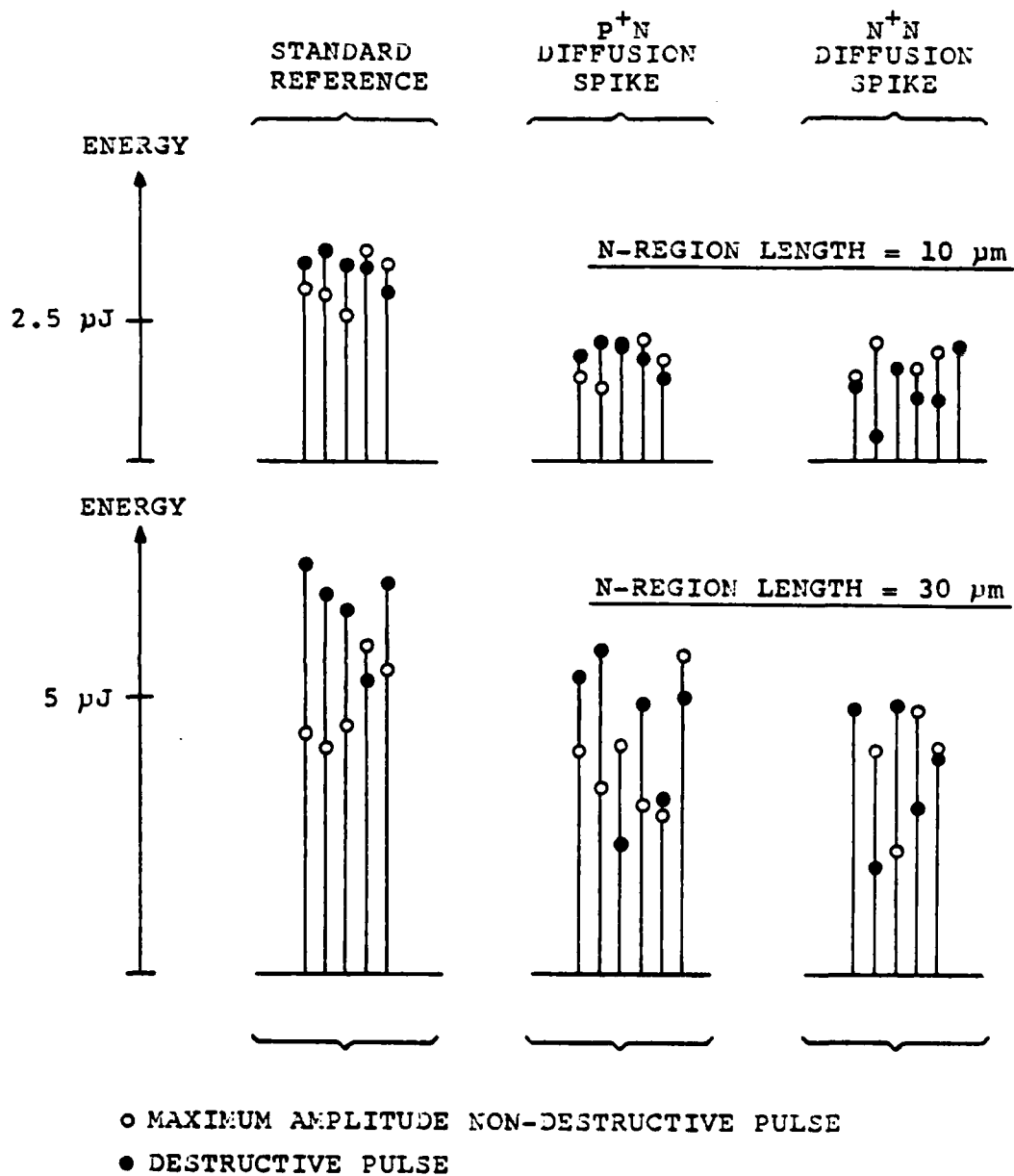


Fig. 37. Total energy input at the second breakdown threshold. These diodes are from Wafer 2-4, and have an n-region width of 30 μm .

and 37, so the spikes have not had a greater influence as width decreased from 200 μm to 30 μm .

Inspection of Table 6 shows that diodes on Wafer 2-4 fail at current amplitudes approximately one-fourth to one-third of those on Wafer 2-5. The data in both Tables 6 and 7 indicate that diffusion spike diodes on Wafer 2-4 tend to fail at current amplitudes slightly less (5-30% in average values) than those of standard reference diodes.

Failure energy threshold data were also taken for diodes with an n-region width of 30 μm on Wafer 2-5. However, as mentioned previously, some of these diodes did not develop a melt filament during the pulse which produced a hot filament through the n-region. Further increase in pulse amplitude would have yielded a melt filament, but this was done in only a few cases. Thus the 30 μm data obtained on Wafer 2-5 are not quite comparable to the 30 μm data of Wafer 2-4.

The failure energy thresholds of standard reference and diffusion spike diodes on Wafer 2-1 are shown in Fig. 38. Figure 38 is similar to Fig. 36 in all respects except for the n-region doping level and the energy scale.

Diffusion spikes have a major effect on the failure energy thresholds of diodes with a 10 μm n-region length. The failure energy thresholds of the diffusion spike diodes are very small in comparison with the standard reference diodes, while the standard reference diodes exhibit a wide range of failure threshold energies, varying as much as a factor of ten. The diffusion spike diodes typically fail during the initial rise of the current and voltage waveforms. The junction depletion width exceeds 10 μm for doping levels less than $2 \times 10^{15} \text{ cm}^{-3}$.

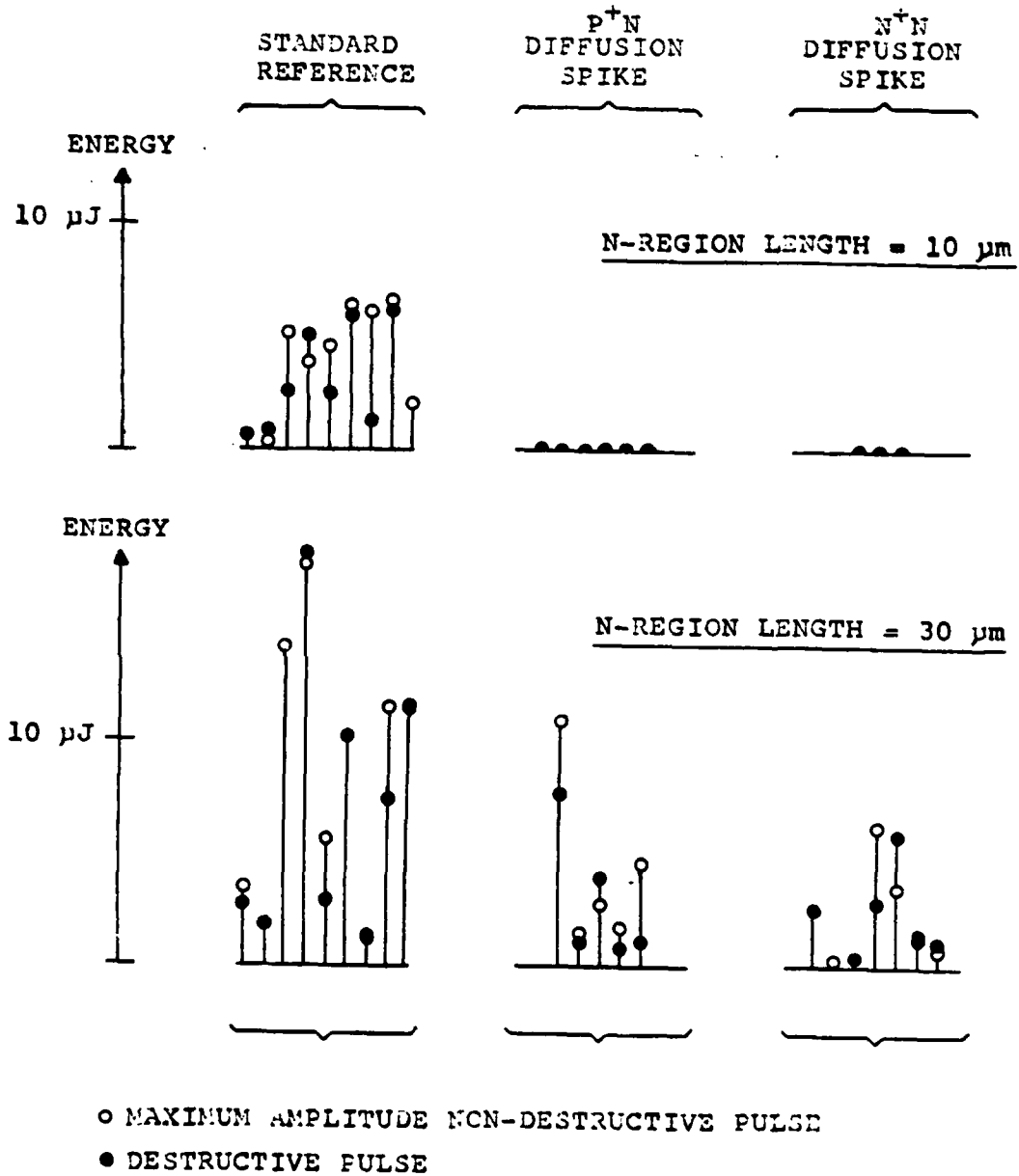


Fig. 38. Total energy input at the second breakdown threshold. These diodes are from Wafer 2-1, and have an n-region width of $200 \mu\text{m}$.

Thus punchthrough exists in Wafer 2-1 for all 10 μ m diodes, with conditions much more severe at the spike positions where the n-region length is reduced to 5 μ m.

Standard reference and diffusion spike diodes with an n-region length of 30 μ m exhibit a wide range of failure energy thresholds. In general, standard reference diodes tend to have higher failure energy thresholds than diffusion spike diodes, but the ranges overlap considerably. It appears that the effect of geometry is partially obscured by non-uniformities in the fabrication processes.

The data in Tables 6 and 7 indicate that the failure current amplitudes of standard reference diodes on Wafer 2-1 vary by a factor of six, and the average current amplitudes are roughly one-fifteenth of those of similar diodes on Wafer 2-5. For an n-region length of 10 μ m, standard reference diodes of Wafer 2-1 fail at an average current amplitude over five times that of diffusion spike diodes. Standard reference diodes of Wafer 2-1 also tend to fail at larger current amplitudes for the 30 μ m n-region length.

The failure threshold energies shown in Figs. 33, 36, and 38 were obtained from diodes with a constant n-region width of 200 μ m. Since three different doping levels are represented in Figs. 33, 36, and 38, these data may be used to investigate failure threshold energy as a function of n-region doping level. However, it is first necessary to make some assumptions concerning the actual n-region doping level. The n-region doping levels of Wafers 2-5, 2-4, and 2-1 were assumed to be given by an average of the doping level estimations in Chapter IV.

The failure threshold energies of standard reference and diffusion spike diodes are plotted as functions of n-region doping level for 30 μm n-region length diodes in Fig. 39, and for 10 μm n-region length diodes in Fig. 40. The corresponding current failure thresholds are shown in Fig. 41 and Fig. 42. The individual points in Fig. 39 and Fig. 40 were obtained by averaging the higher of the failure and pre-failure energies in Figs. 33, 36, and 38. The individual points in Fig. 41 and Fig. 42 were obtained from Table 6 and Table 7. Horizontal error bars show the range of doping level estimations, and vertical error bars show the maximum and minimum energies, or currents, included in the average.

The failure threshold energy of both standard reference and diffusion spike diodes increases as n-region doping level increases in Fig. 39, roughly a factor of five or ten as the doping density goes from 10^{14} to 10^{17} cm^{-3} . Standard reference diodes have the highest failure energy thresholds at all three doping levels. The relative importance of the diffusion spikes appears to vary with doping level. At the two lower doping levels, diffusion spikes lower the failure thresholds almost 50%. However diffusion spikes have less effect at the highest doping level. Diffusion spikes on the p^+n junction significantly lower the failure thresholds, but diffusion spikes on the n^+n junction have almost no effect.

Failure threshold energy also tends to increase as n-region doping level increases in Fig. 40. However, the failure threshold energies of standard reference diodes at the two higher doping levels were very similar. The failure threshold energies of the diffusion spike diodes

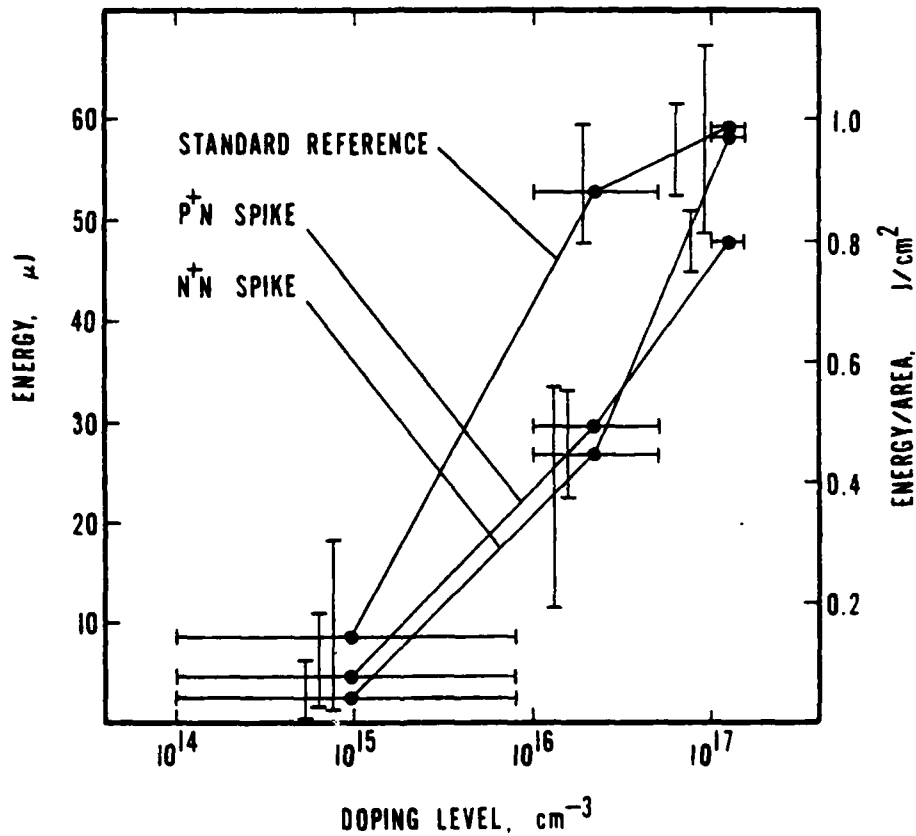


Fig. 39. Total energy input at the second breakdown threshold as a function of n-region doping level for standard reference and diffusion spike diodes. The n-region length and width of these diodes are 30 and 200 μm , respectively. Each point is the average of approximately five measurements. Vertical error bars show the maximum and minimum values included in the average, and horizontal error bars show the range of the doping level estimations.

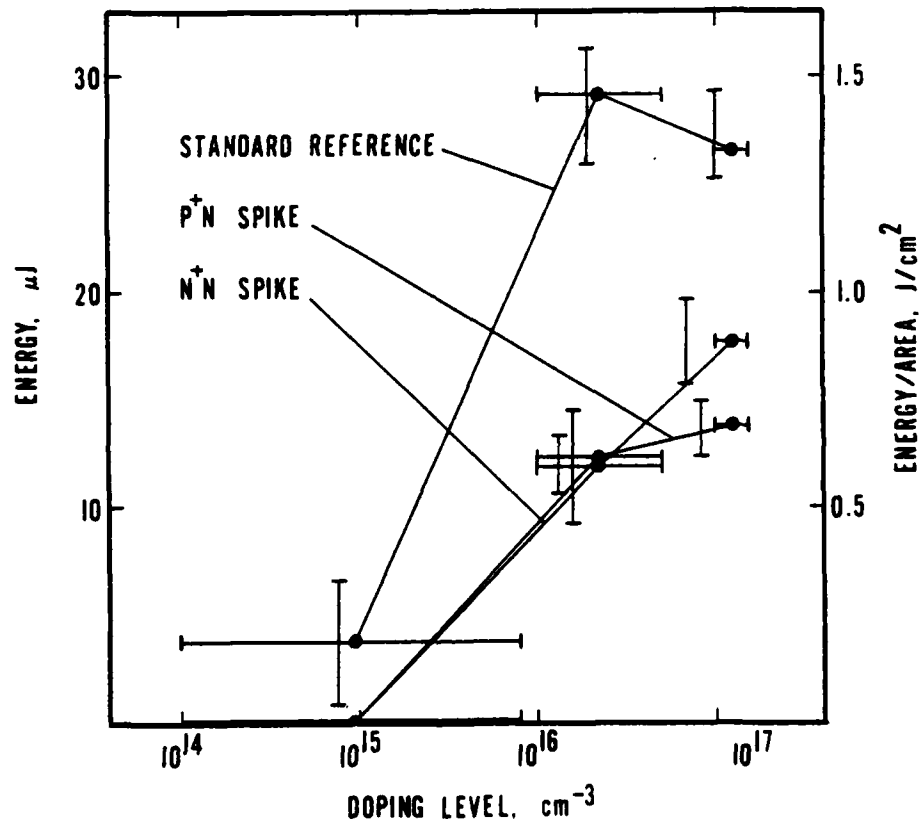


Fig. 40. Total energy input at the second breakdown threshold as a function of n-region doping level for standard reference and diffusion spike diodes. The n-region length and width of these diodes are 10 and 200 μm , respectively. Each point is the average of approximately five measurements. Vertical error bars show the maximum and minimum values included in the average, and horizontal error bars show the range of the doping level estimations.

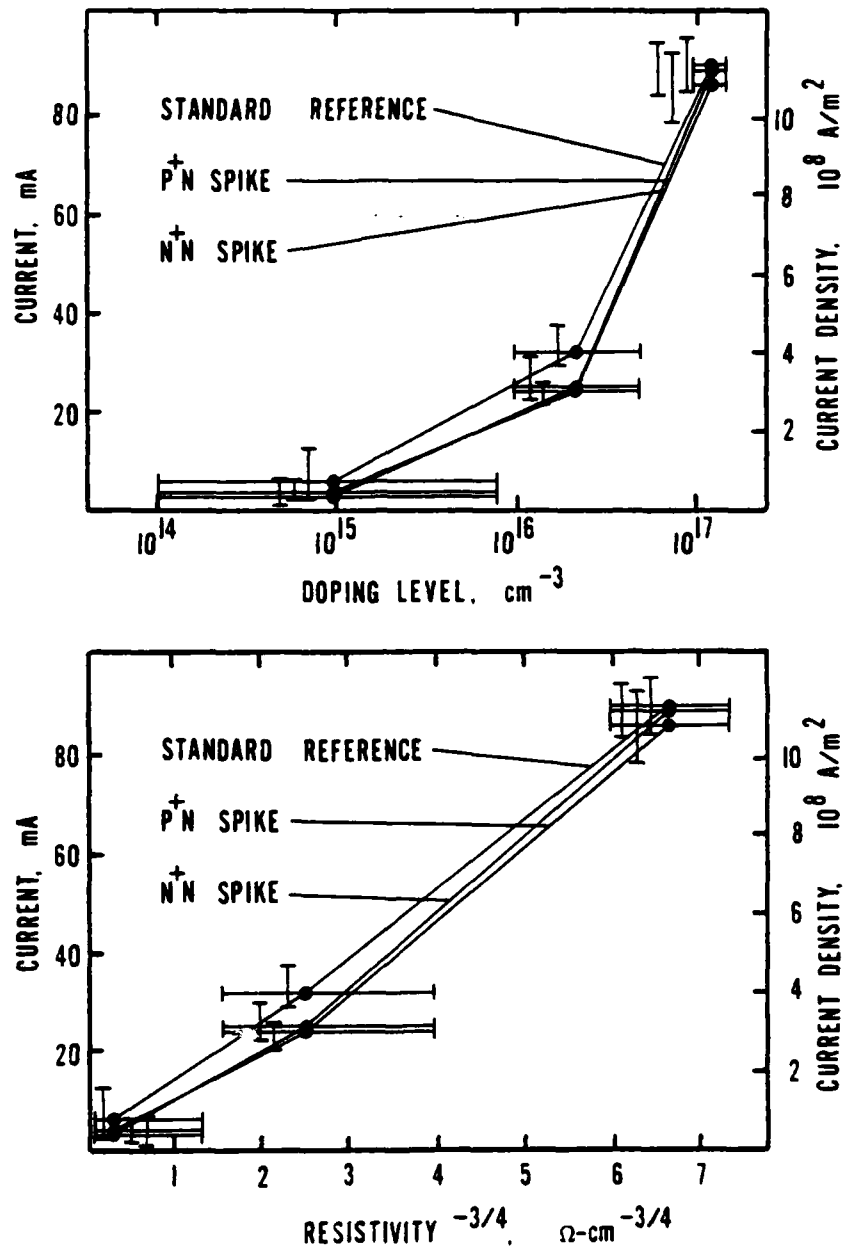


Fig. 41. Current amplitude at the second breakdown threshold as functions of n-region doping level and resistivity for standard reference and diffusion spike diodes (length = $30 \mu\text{m}$, width = $200 \mu\text{m}$). Each point is the average of approximately five measurements. Vertical and horizontal error bars show, respectively, the maximum and minimum values included in the average, and the range of doping level or resistivity estimations.

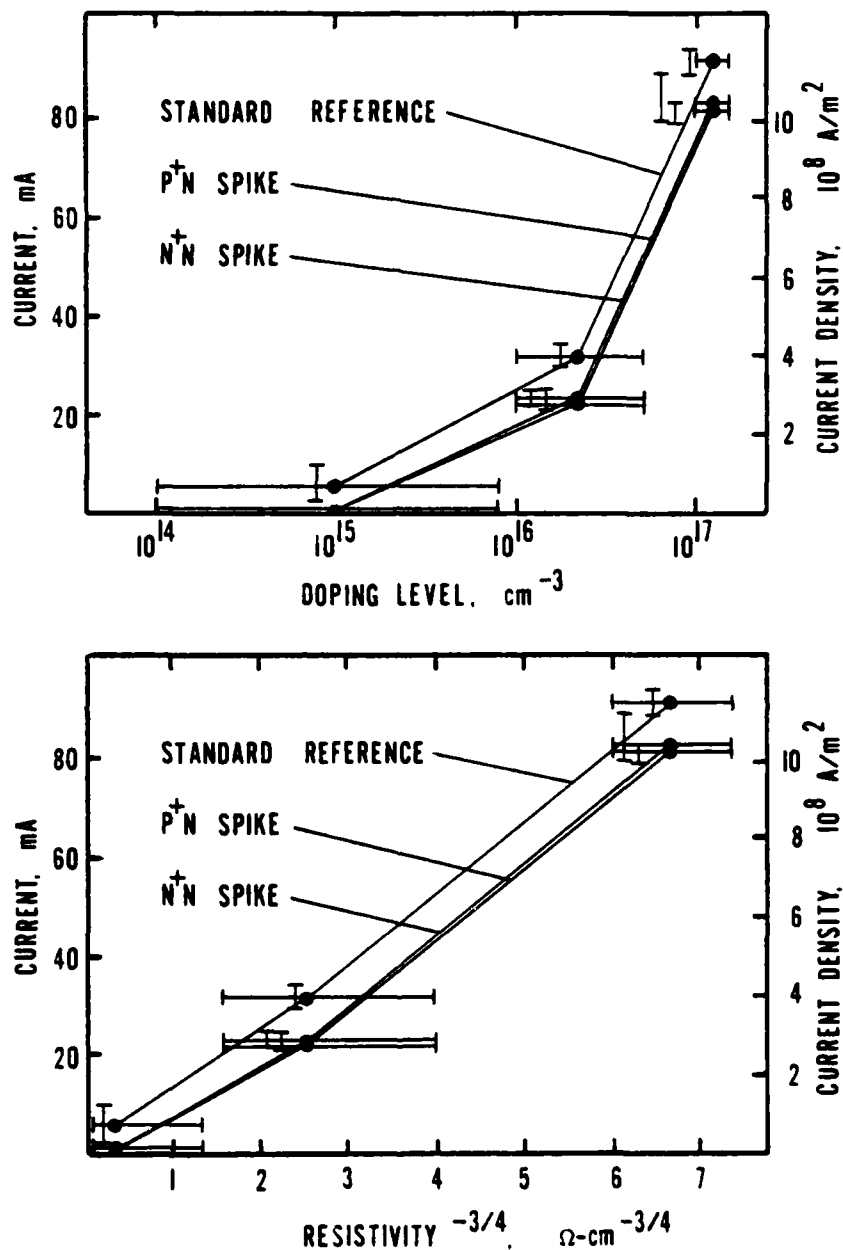


Fig. 42. Current amplitude at the second breakdown threshold as functions of n-region doping level and resistivity for standard reference and diffusion spike diodes (length = 10 μm , width = 200 μm). Each point is the average of approximately five measurements. Vertical and horizontal error bars show, respectively, the maximum and minimum values included in the average, and the range of doping level or resistivity estimations.

are much larger at the two higher doping levels than at the lowest doping level, at least a factor of fifty. The failure thresholds of diffusion spike diodes were less than those of standard reference diodes at all three doping levels.

Figure 41 and Fig. 42 show that the current amplitude at the failure threshold also increases as n-region doping level increases, and that standard reference diodes tend to have higher failure currents than diffusion spike diodes. Diffusion spikes become less effective in reducing failure current thresholds as doping level increases. However, the major factor affecting failure current amplitude is the n-region doping level. Figures 41b and 42b indicate that current thresholds closely follow the $\rho^{-3/4}$ dependence predicted by the Budenstein, Pontius, Smith model.

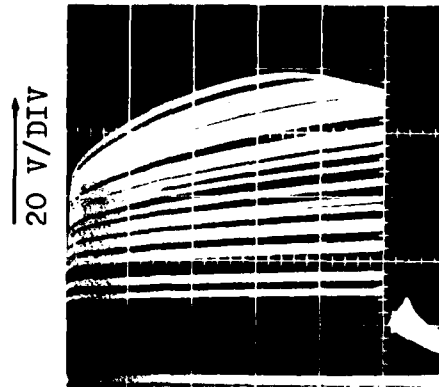
2. Voltage Threshold Analysis

The energy threshold data presented above provide one scheme for evaluating second breakdown thresholds. Both voltage and current waveforms had to be obtained, multiplied together, and integrated to the point where failure had occurred (or to the end of the pulse in cases where the failure threshold is estimated). However, one of the goals of the present effort was to find a tractable method for evaluating second breakdown susceptibility. To this end, voltage thresholds were observed using pulses from a constant impedance generator. In each test, single pulses of gradually increasing amplitude were applied until failure occurred.

Pulses were supplied by a Velonex Model 380 pulse generator to the series connection of a $1\text{ k}\Omega$ resistor and a reverse biased diode. The resistor was included to limit damage so that filament locations could be investigated. The maximum amplitude of the voltage waveform during the failure pulse was taken as the voltage failure threshold. The pulse shape was approximately square on all but Wafers 1-5 and 2-5. In the latter cases, there was a voltage turnover before the end of the damaging pulse. This is shown in Fig. 43 for standard reference and p^+n diffusion spike diodes on Wafers 2-5 and 2-4 with a common n-region length of $30\text{ }\mu\text{m}$ and a width of $200\text{ }\mu\text{m}$. The voltage at this turnover was taken as the voltage failure threshold.

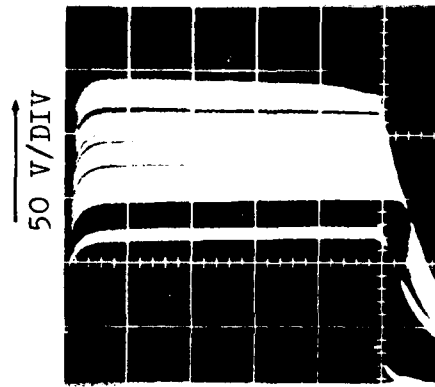
Diodes with varying n-region lengths, widths, and doping levels were tested in eight different structural types. The voltage failure thresholds were strong functions of n-region length and doping level, but voltage was independent of n-region width. Therefore, in the results which follow, n-region width is not further considered. The eight structure types were standard reference, metal- p^+ and metal- n^+ contact spike, p^+n and n^+n diffusion spike, radius of curvature, and multiple spike. The spike length for the contact and diffusion spike structures was $5\text{ }\mu\text{m}$. The multiple spike lengths were 1, 2, 4, and $8\text{ }\mu\text{m}$. In the first six of these structures, approximately twelve diodes were tested at each of three n-region lengths (10 , 30 , and $100\text{ }\mu\text{m}$) on wafers representing each of the five nominal doping densities (Wafers 2-1, 2-2, 1-3, 2-4, and 2-5). Diodes with an n-region length of $300\text{ }\mu\text{m}$ were included on Wafer 2-5. Voltage threshold tests on radius of curvature diodes were similar, except that nine diodes were tested for each

WAFER 2-5
STANDARD REFERENCE



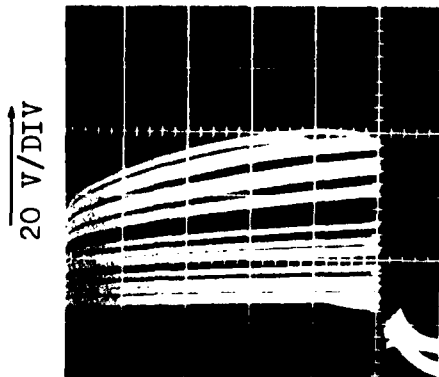
2 μ s/DIV

WAFER 2-4
STANDARD REFERENCE



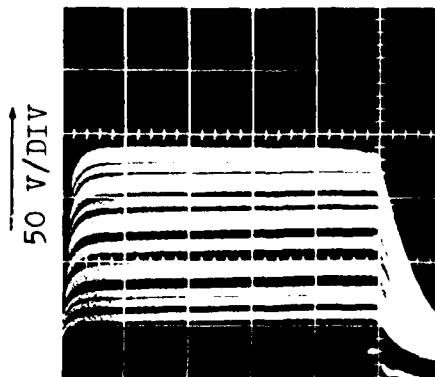
2 μ s/DIV

WAFER 2-5
P⁺N SPIKE



2 μ s/DIV

WAFER 2-4
P⁺N SPIKE



2 μ s/DIV

Fig. 43. Voltage waveforms showing second breakdown in standard reference and p⁺n diffusion spike diodes on Wafers 2-5 and 2-4. Pulses of increasing amplitude were applied to the diodes until damage occurred. The diodes have a common n-region length of 30 μ m and a width of 200 μ m.

n-region length, and only n-region lengths of 10, 30, and 100 μm were tested (since the structure only contains three n-region lengths). In the multiple spike structure, only diodes with p^+n and n^+n diffusion spikes were tested. Three diodes were tested for each n-region length (10, 30, and 100 μm), and for each diffusion spike length. In all, approximately 1500 diodes were included.

The failure voltages of standard reference and diffusion spike diodes on Wafer 2-5 are plotted versus n-region length in Fig. 44. Each point on the diagram is the average of the failure voltages of approximately twelve diodes. Error bars show one standard deviation above and below the mean. The most distinctive feature of Fig. 44 is that the voltage failure thresholds of both the standard reference and the diffusion spike diodes increase approximately linearly with n-region length. The close proximity of the three curves indicates that diffusion spikes do not play a major role in reducing the voltage failure thresholds. However, the voltage threshold distributions of standard reference and p^+n spike diodes are separated by more than one standard deviation for n-region lengths of 10, 30, and 100 μm . This indicates that the p^+n spike has a minor effect in reducing the voltage failure thresholds. A similar effect did not occur for n^+n spike diodes. Most of the error bars in Fig. 44 are too small to be seen clearly. Therefore, this information is also presented numerically in Tables 8-12. Tables 8-12 contain all the voltage threshold data for this and subsequent sections.

The voltage failure thresholds of standard reference diodes closely fit a straight line. A least-squares fit to the data in Fig. 44

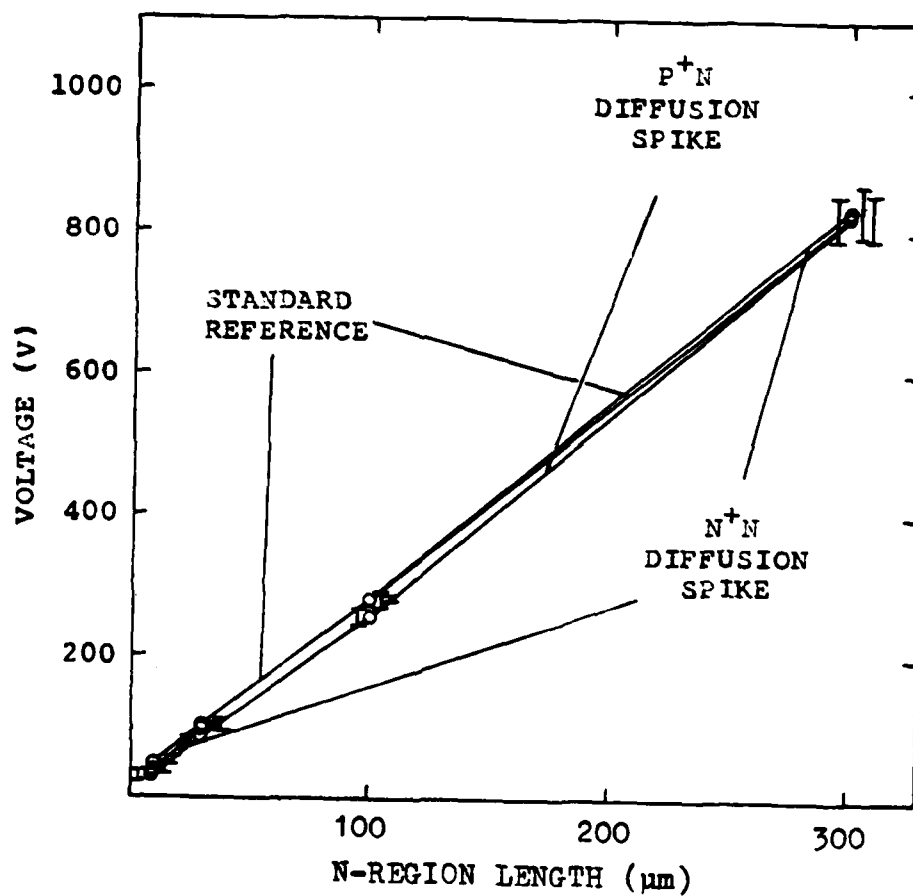


Fig. 44. Breakdown voltage versus n-region length for standard reference, p^+n diffusion spike, and n^+n diffusion spike diodes on Wafer 2-5. Error bars show one standard deviation above and below the mean.

TABLE 8.--Voltage failure thresholds of diodes with an n-region length of 10 μm .

VOLTAGE FAILURE THRESHOLDS OF DIODES WITH AN N-REGION LENGTH OF 10 μm				
NOMINAL DOPING DENSITY (cm^{-3})	WAFER NUMBER	DIODE TYPE	BREAKDOWN VOLTAGE (V)	STANDARD DEV. (V)
10^{14}	2-1	STANDARD REF.	177	4
10^{14}	2-1	ENCLOSED REF.	163	5
10^{14}	2-1	P ⁺ N SPIKE	100	6
10^{14}	2-1	N ⁺ N SPIKE	98	5
10^{14}	2-1	RAD. OF CUR.	191	13
10^{15}	2-2	STANDARD REF.	158	12
10^{15}	2-2	ENCLOSED REF.	150	6
10^{15}	2-2	P ⁺ N SPIKE	70	26
10^{15}	2-2	N ⁺ N SPIKE	72	10
10^{15}	2-2	RAD. OF CUR.	168	10
10^{16}	1-3	STANDARD REF.	179	6
10^{16}	1-3	ENCLOSED REF.	187	9
10^{16}	1-3	P ⁺ N SPIKE	99	6
10^{16}	1-3	N ⁺ N SPIKE	100	5
10^{16}	1-3	RAD. OF CUR.	201	7
10^{17}	2-4	STANDARD REF.	115	4
10^{17}	2-4	ENCLOSED REF.	115	4
10^{17}	2-4	P ⁺ N SPIKE	86	2
10^{17}	2-4	N ⁺ N SPIKE	87	2
10^{17}	2-4	RAD. OF CUR.	129	2
5×10^{17}	2-5	STANDARD REF.	48	2
5×10^{17}	2-5	ENCLOSED REF.	48	3
5×10^{17}	2-5	P ⁺ N SPIKE	30	4
5×10^{17}	2-5	N ⁺ N SPIKE	38	5
5×10^{17}	2-5	RAD. OF CUR.	51	2

TABLE 9.--Voltage failure thresholds of diodes with an n-region length of 30 μm .

VOLTAGE FAILURE THRESHOLDS OF DIODES WITH AN N-REGION LENGTH OF 30 μm				
NOMINAL DOPING DENSITY (cm^{-3})	WAFER NUMBER	DIODE TYPE	BREAKDOWN VOLTAGE (V)	STANDARD DEV. (V)
10^{14}	2-1	STANDARD REF.	355	22
10^{14}	2-1	ENCLOSED REF.	281	21
10^{14}	2-1	P ⁺ N SPIKE	348	26
10^{14}	2-1	N ⁺ N SPIKE	225	18
10^{14}	2-1	RAD. OF CUR.	320	23
10^{15}	2-2	STANDARD REF.	364	42
10^{15}	2-2	ENCLOSED REF.	257	25
10^{15}	2-2	P ⁺ N SPIKE	333	29
10^{15}	2-2	N ⁺ N SPIKE	211	12
10^{15}	2-2	RAD. OF CUR.	299	7
10^{16}	1-3	STANDARD REF.	370	16
10^{16}	1-3	ENCLOSED REF.	319	22
10^{16}	1-3	P ⁺ N SPIKE	336	10
10^{16}	1-3	N ⁺ N SPIKE	223	11
10^{16}	1-3	RAD. OF CUR.	352	25
10^{17}	2-4	STANDARD REF.	248	5
10^{17}	2-4	ENCLOSED REF.	239	7
10^{17}	2-4	P ⁺ N SPIKE	216	12
10^{17}	2-4	N ⁺ N SPIKE	203	4
10^{17}	2-4	RAD. OF CUR.	231	8
5×10^{17}	2-5	STANDARD REF.	104	6
5×10^{17}	2-5	ENCLOSED REF.	105	5
5×10^{17}	2-5	P ⁺ N SPIKE	85	3
5×10^{17}	2-5	N ⁺ N SPIKE	99	3
5×10^{17}	2-5	RAD. OF CUR.	105	3

TABLE 10.--Voltage failure thresholds of diodes with an n-region length of 100 μm .

VOLTAGE FAILURE THRESHOLDS OF DIODES WITH AN N-REGION LENGTH OF 100 μm				
NOMINAL DOPING DENSITY (cm^{-3})	WAFER NUMBER	DIODE TYPE	BREAKDOWN VOLTAGE (V)	STANDARD DEV. (V)
10^{14}	2-1	STANDARD REF.	806	80
10^{14}	2-1	ENCLOSED REF.	822	79
10^{14}	2-1	P ⁺ N SPIKE	833	73
10^{14}	2-1	N ⁺ N SPIKE	731	55
10^{14}	2-1	RAD. OF CUR.	797	87
10^{15}	2-2	STANDARD REF.	823	62
10^{15}	2-2	ENCLOSED REF.	734	56
10^{15}	2-2	P ⁺ N SPIKE	812	83
10^{15}	2-2	N ⁺ N SPIKE	680	96
10^{15}	2-2	RAD. OF CUR.	762	68
10^{16}	1-3	STANDARD REF.	996	85
10^{16}	1-3	ENCLOSED REF.	909	93
10^{16}	1-3	P ⁺ N SPIKE	952	90
10^{16}	1-3	N ⁺ N SPIKE	815	54
10^{16}	1-3	RAD. OF CUR.	947	64
10^{17}	2-4	STANDARD REF.	662	25
10^{17}	2-4	ENCLOSED REF.	631	35
10^{17}	2-4	P ⁺ N SPIKE	633	11
10^{17}	2-4	N ⁺ N SPIKE	541	30
10^{17}	2-4	RAD. OF CUR.	508	27
5×10^{17}	2-5	STANDARD REF.	281	3
5×10^{17}	2-5	ENCLOSED REF.	274	6
5×10^{17}	2-5	P ⁺ N SPIKE	257	11
5×10^{17}	2-5	N ⁺ N SPIKE	279	10
5×10^{17}	2-5	RAD. OF CUR.	227	5

TABLE 11.--Voltage failure thresholds of diodes with an n-region length of 300 μm , and multiple spike diodes on Wafer 2-5.

VOLTAGE FAILURE THRESHOLDS OF DIODES WITH AN N-REGION LENGTH OF 300 μm				
NOMINAL DOPING DENSITY (cm^{-3})	WAFER NUMBER	DIODE TYPE	BREAKDOWN VOLTAGE (V)	STANDARD DEV. (V)
5×10^{17}	2-5	STANDARD REF.	825	29
5×10^{17}	2-5	ENCLOSED REF.	808	21
5×10^{17}	2-5	P ⁺ N SPIKE	822	34
5×10^{17}	2-5	N ⁺ N SPIKE	834	22

WAFER NUMBER	SPIKE TYPE	SPIKE LENGTH (μm)	BREAKDOWN VOLTAGES (V)					
			10 μm		30 μm		100 μm	
			AVG.	STAN. DEV.	AVG.	STAN. DEV.	AVG.	STAN. DEV.
2-5	NONE	0	48	2	105	6	283	3
2-5	P ⁺ N	1	44.2	1.8	93.4	5.8	269	10
2-5	P ⁺ N	2	42.1	1.2	89	5.2	262	7.8
2-5	P ⁺ N	4	37.4	1.3	82.4	4.6	255	8.7
2-5	P ⁺ N	8	22.1	2.4	71.3	6.1	238	7.5
2-5	N ⁺ N	1	46.3	1	96.4	6.2	274	5.8
2-5	N ⁺ N	2	44.8	2	96.6	5.9	272	7.4
2-5	N ⁺ N	4	41.3	2.6	94.9	7.6	271	6.5
2-5	N ⁺ N	8	25.7	1.5	90.9	4.1	269	9.5

TABLE 12.--Voltage failure thresholds of multiple spike diodes on Wafers 2-2, 1-3, and 2-4.

WAFER NUMBER	SPIKE TYPE	SPIKE LENGTH (μm)	BREAKDOWN VOLTAGES (V)		
			10 μm AVG.	30 μm AVG.	100 μm AVG.
2-2	NONE	0	158	302	847
2-2	P ⁺ N	1	139	309	817
2-2	P ⁺ N	2	128	260	817
2-2	P ⁺ N	4	91	302	823
2-2	P ⁺ N	8		294	743
2-2	N ⁺ N	1	133	282	750
2-2	N ⁺ N	2	123	284	717
2-2	N ⁺ N	4	89	207	700
2-2	N ⁺ N	8		198	627
1-3	NONE	0	186	353	1043
1-3	P ⁺ N	1	162	352	1017
1-3	P ⁺ N	2	152	348	1017
1-3	P ⁺ N	4	117	343	1020
1-3	P ⁺ N	8		312	990
1-3	N ⁺ N	1	159	349	1007
1-3	N ⁺ N	2	152	333	1017
1-3	N ⁺ N	4	122	250	873
1-3	N ⁺ N	8		278	810
2-4	NONE	0	114	246	643
2-4	P ⁺ N	1	107	243	637
2-4	P ⁺ N	2	103	247	637
2-4	P ⁺ N	4	92	213	607
2-4	P ⁺ N	8		172	603
2-4	N ⁺ N	1	108	238	635
2-4	N ⁺ N	2	104	238	620
2-4	N ⁺ N	4	93	218	593
2-4	N ⁺ N	8		175	513

gives a slope of 2.68 V/ m, an intercept of 20 V, and a correlation coefficient of 0.99992. The intercept is the sum of the average junction voltage and the series iR -drops of the p^+ and n^+ regions. In Wafer 2-5, with the threshold current density of 8.8×10^8 A/m², the series iR -drop is about 3V for a diode of 200 μ m width. Since the average current density at the failure threshold is largely independent of n -region length, the sum of the p^+n junction voltage and series iR -drop near the failure threshold is also independent of n -region length. With an intercept of 20 V and a series iR -drop of 3 V, the junction voltage at the breakdown threshold is 17 V. This is to be compared to the low current avalanche voltage in Wafer 2-5 of 12 V.

The voltage failure thresholds of standard reference and diffusion spike diodes on Wafer 2-4 are shown in Fig. 45. Comparison with Fig. 44 shows that the voltage failure thresholds of diodes on Wafer 2-5 are roughly half those of corresponding diodes on Wafer 2-4. The failure voltages of standard reference diodes tend to be larger than those of diffusion spike diodes for all three n -region lengths in Fig. 45. In addition, the failure voltages of n^+n spike diodes tend to be less than those of p^+n spike diodes for n -region lengths of 30 and 100 μ m. The mean failure threshold of n^+n spike diodes is roughly 20% less than that of standard reference diodes for all three n -region lengths. The distributions are separated by more than one standard deviation. Although there are large overlaps in the data distributions, the data of Figs. 39, 40, 44, and 45 indicate that p^+n spikes are more effective in reducing both energy and voltage failure thresholds on Wafer 2-5, while the reverse is true on Wafer 2-4. The data for standard reference di-

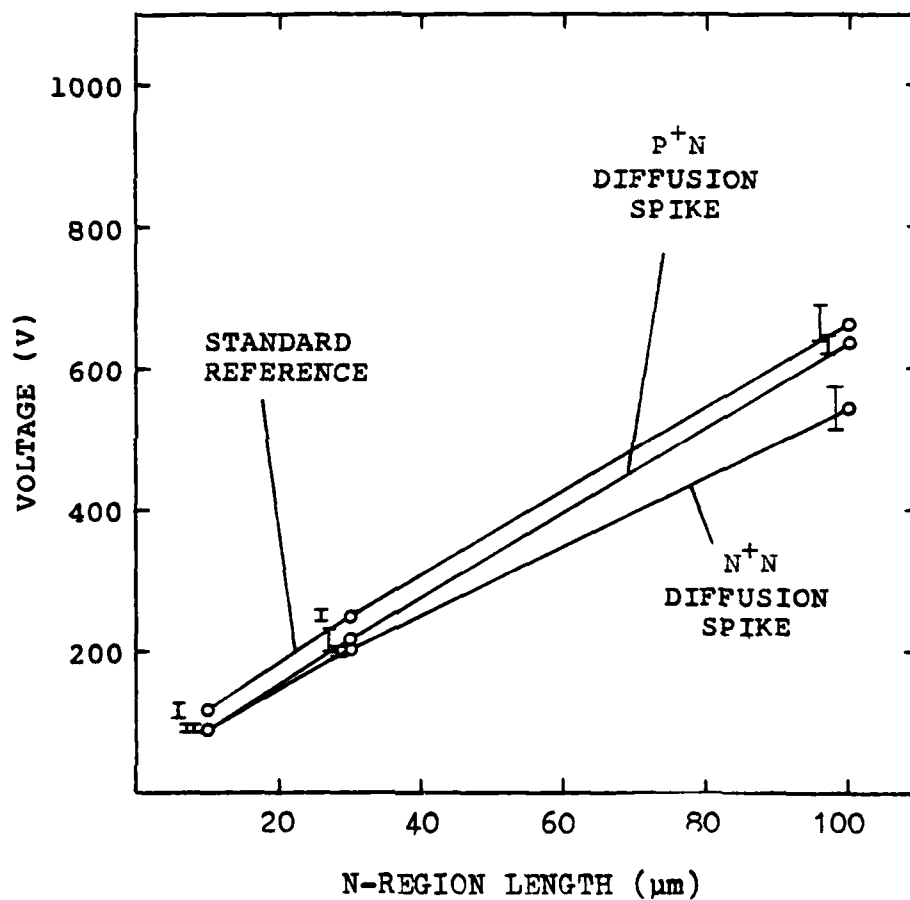


Fig. 45. Breakdown voltage versus n-region length for standard reference, p⁺n diffusion spike, and n⁺n diffusion spike diodes on Wafer 2-4. Error bars show one standard deviation above and below the mean.

odes in Fig. 45 fit a straight line with a slope of 6.04 V/ m, an intercept of 60 V, and a correlation coefficient of 0.9998.

The voltage failure thresholds of standard reference and diffusion spike diodes on Wafers 1-3, 2-2, and 2-1 are shown in Figs. 46, 47, and 48, respectively. Although these three wafers have nominal doping densities which vary by a factor of a hundred, their electrical behavior is very similar, so they are discussed together. There were several 100 μm n-region length diodes on Wafer 1-3 which did not fail at the maximum pulse amplitude of the Velonex pulser (about 1000 V). The two plus signs over points on Fig. 46 indicate that the maximum amplitude setting of the pulse generator was taken as the failure voltage when the diode could not be destroyed.

Several distinctive features common to each of the three plots in Figs. 46, 47, and 48 are discussed below. Diodes with an n-region length of 10 μm are affected almost equally by the presence of either type of diffusion spike; the spike lowers the failure threshold by a factor of approximately one-half. However, diodes with n-region lengths of 30 and 100 μm are not affected equally by p^+n and n^+n spikes. The p^+n spike becomes less effective in reducing the failure threshold as n-region length increases. As indicated by the error bars, there is no significant difference in the failure thresholds of standard reference and p^+n spike diodes with n-region lengths of 100 μm . The n^+n spike exerts a significant influence at an n-region length of 30 μm , since the distribution is separated from that of both standard reference and p^+n spike diodes by more than one standard deviation.

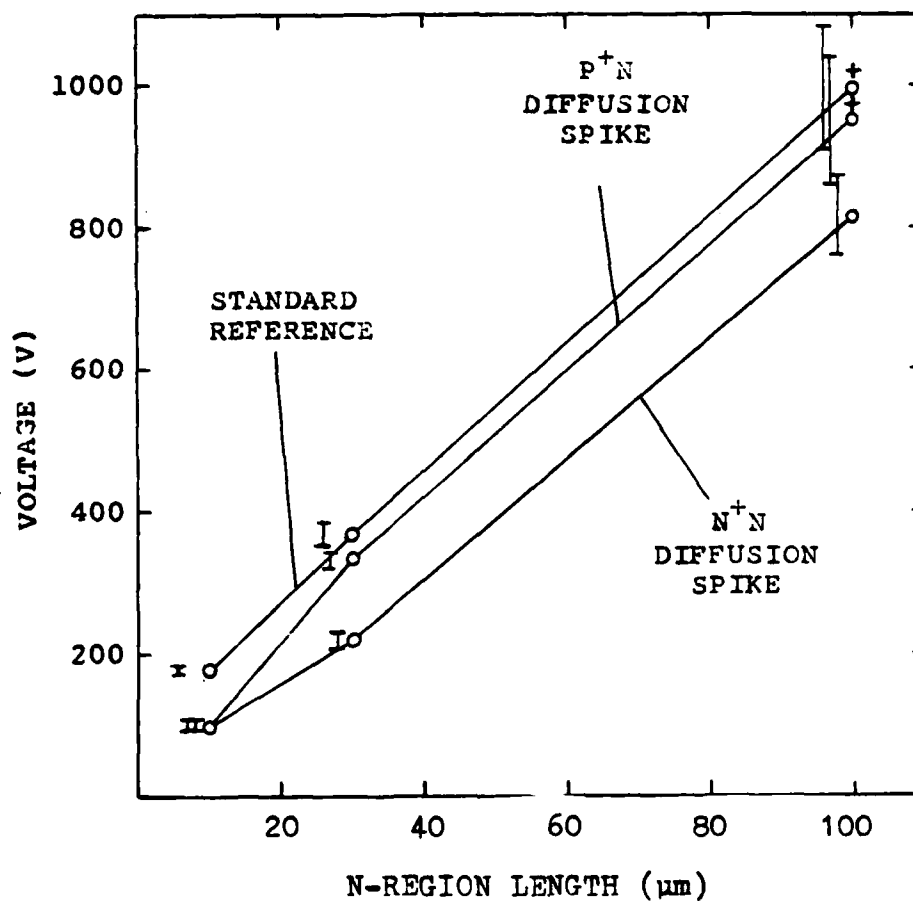


Fig. 46. Breakdown voltage versus n-region length for standard reference, p^+n diffusion spike, and n^+n diffusion spike diodes on Wafer 1-3. Error bars show one standard deviation above and below the mean. The plus sign indicates that some diodes could not be burned out at the maximum amplitude of the pulse generator.

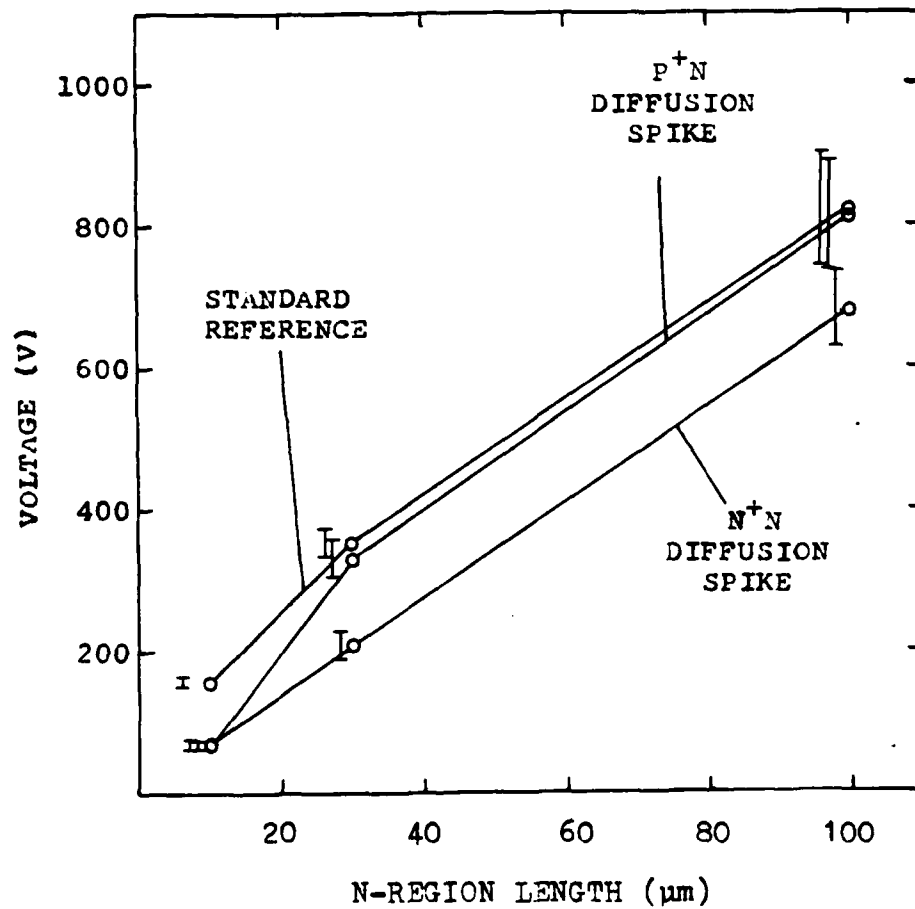


Fig. 47. Breakdown voltage versus n-region length for standard reference, p+n diffusion spike, and n+n diffusion spike diodes on Wafer 2-2. Error bars show one standard deviation above and below the mean.

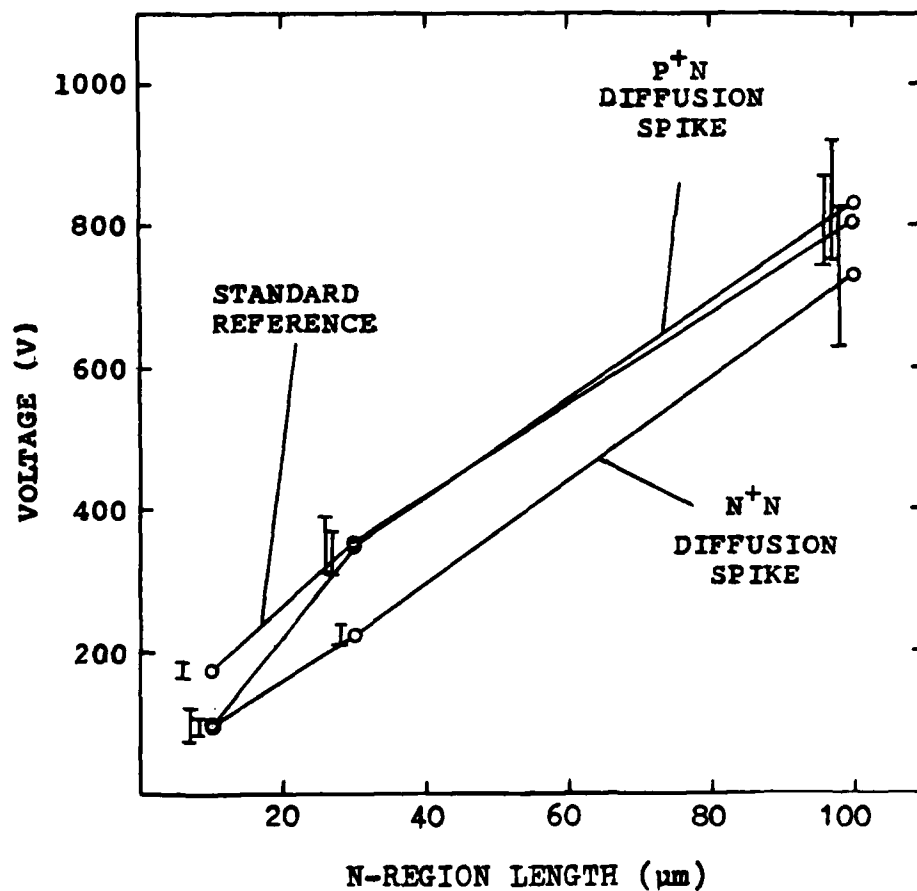


Fig. 48. Breakdown voltage versus n-region length for standard reference, p⁺n diffusion spike, and n⁺n diffusion spike diodes on Wafer 2-1. Error bars show one standard deviation above and below the mean.

The data of Figs. 46-48 were not least-squares fitted because the diodes with 10 μm n-region lengths have different J-V-T characteristics (punchthrough) than diodes with longer n-region lengths. However, for 30 and 100 μm n-region length standard reference diodes, the slopes and intercepts of Figs. 46-48 are 8.9, 6.6, 6.4 V/ μm , and 102, 167, 162 V, respectively.

A plot of voltage failure thresholds of standard reference diodes versus n-region doping level is shown in Fig. 49. These data are from Wafers 2-1, 2-4, and 2-5. Wafers 2-2 and 1-3 were excluded because their doping level estimations are less reliable. The doping level estimations in Fig. 49 are the same as those in Figs. 39-42. The voltage failure thresholds decrease with increasing doping level for each of the three n-region lengths.

The enclosed reference structure and the standard reference structure both have straight p^+n junctions, but the junction is completely islanded by the n-region in the enclosed reference structure. Since protruding corners on the p^+n junction serve as concentration centers for the current, the role of junction corners on voltage failure thresholds was investigated.

The voltage failure thresholds of standard reference and enclosed reference diodes on Wafer 2-5 are shown in Fig. 50. The failure thresholds of both standard and enclosed reference diodes increase approximately linearly with n-region length, and the overlapping error bars indicate that the enclosed reference geometry has no significant effect in reducing the voltage failure thresholds. However, this does not imply that energy failure thresholds are not affected (energy fail-

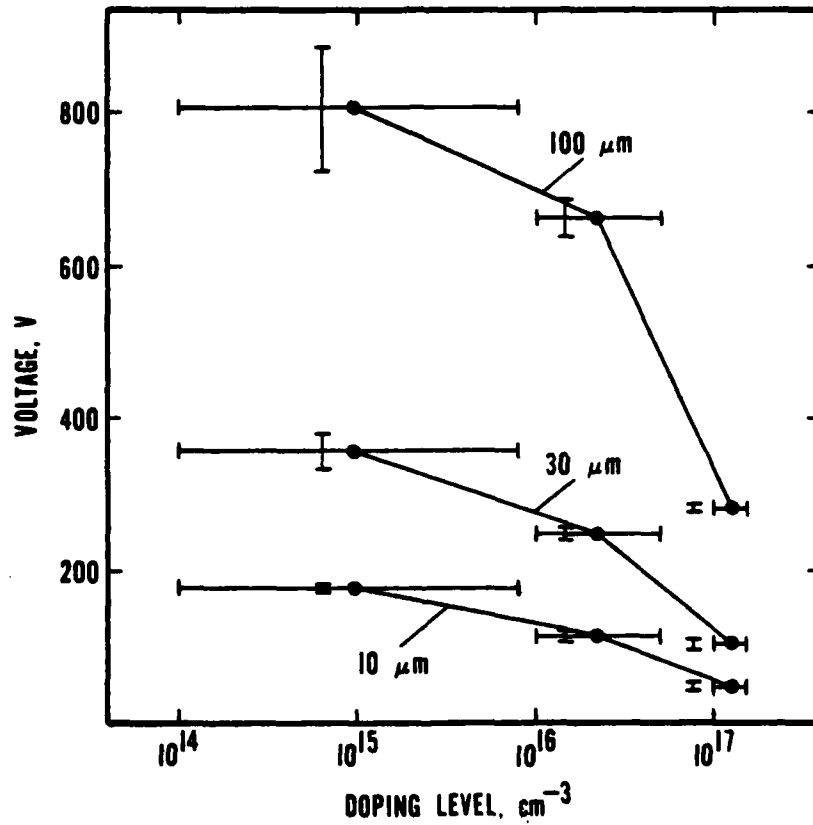


Fig. 49. Breakdown voltage versus n-region doping level for standard reference diodes with n-region lengths of 10, 30, and 100 μm . Vertical error bars show one standard deviation above and below the mean. Horizontal error bars show the range of doping level estimations.

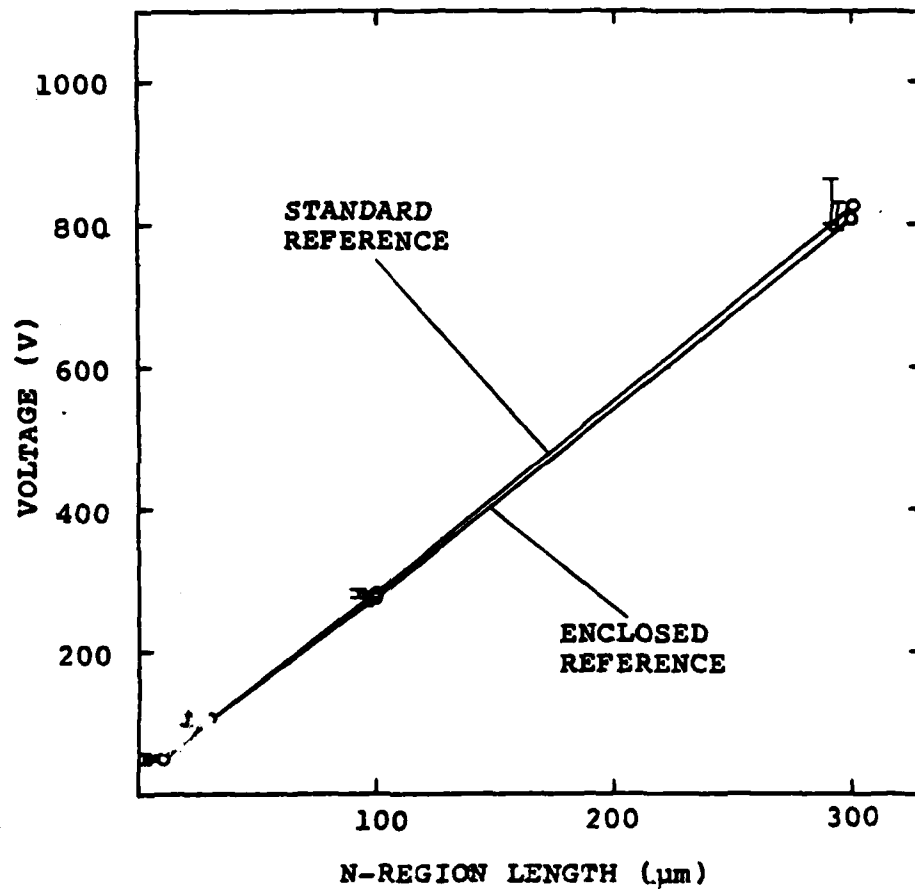


Fig. 50. Breakdown voltage versus n-region length for standard reference and enclosed reference diodes on Wafer 2-5. Error bars show one standard deviation above and below the mean.

ure thresholds were only investigated for standard reference and diffusion spike diodes), since the average current density in front of the protrusions is greater than that on either side of the protrusions.

The voltage failure thresholds of standard reference and enclosed reference diodes on Wafer 2-4 are shown in Fig. 51. The comments made in connection with Fig. 50 also apply to Fig. 51.

The voltage failure thresholds of standard reference and enclosed reference diodes on Wafers 1-3, 2-2, and 2-1 are shown in Figs. 52, 53, and 54, respectively. Again, these three wafers display similar electrical characteristics. The overlapping error bars indicate that there is no significant difference between the voltage failure thresholds of standard and enclosed reference diodes with n-region lengths of 10 and 100 μm , although there is a significant difference for the 30 μm n-region length. The role of spike length in determining voltage failure thresholds will be described in Section V.F.4.

3. Damage Morphology

Damage occurred, in nearly every device tested, by formation of a melt filament across the high resistivity n-region of the device. The location of the melt filament in a diode indicates the portion of the n-region having the highest temperature, and hence the highest current density, at the failure threshold. The melt filament location is related to diode geometry and doping level. In this section, the damage characteristics of standard reference, enclosed reference, and diffusion spike diodes are discussed. These characteristics were determined for the group of 1500 diodes described previously in the voltage threshold tests.

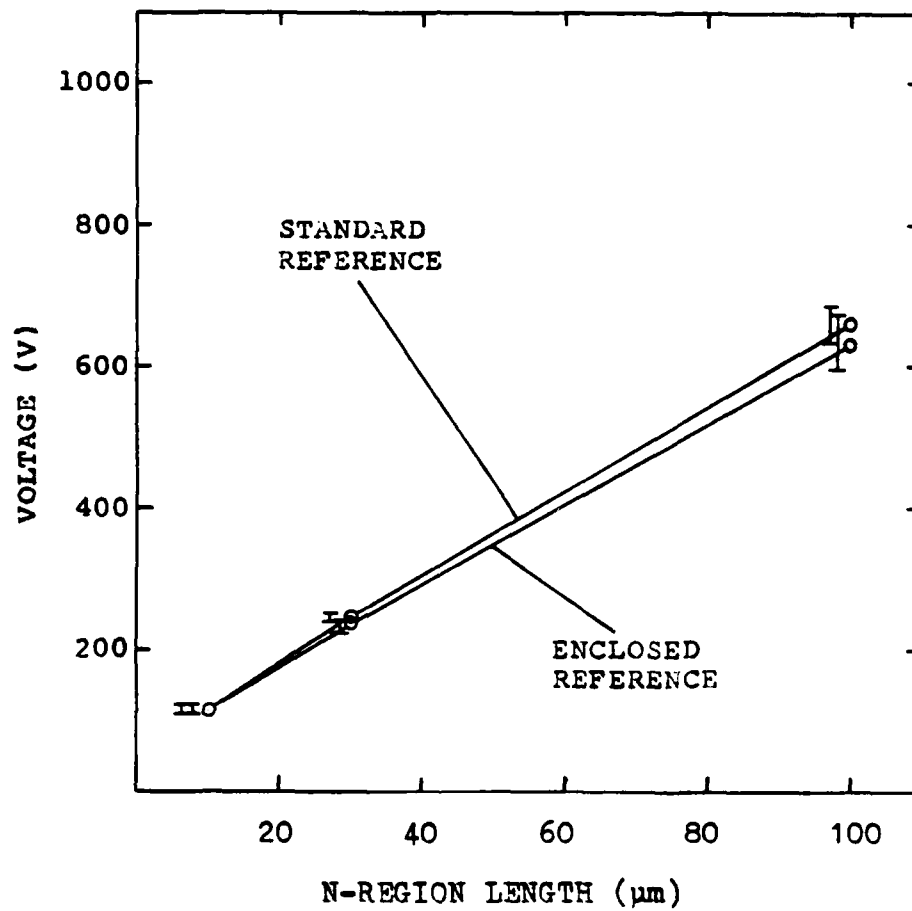


Fig. 51. Breakdown voltage versus n-region length for standard reference and enclosed reference diodes on Wafer 2-4. Error bars show one standard deviation above and below the mean.

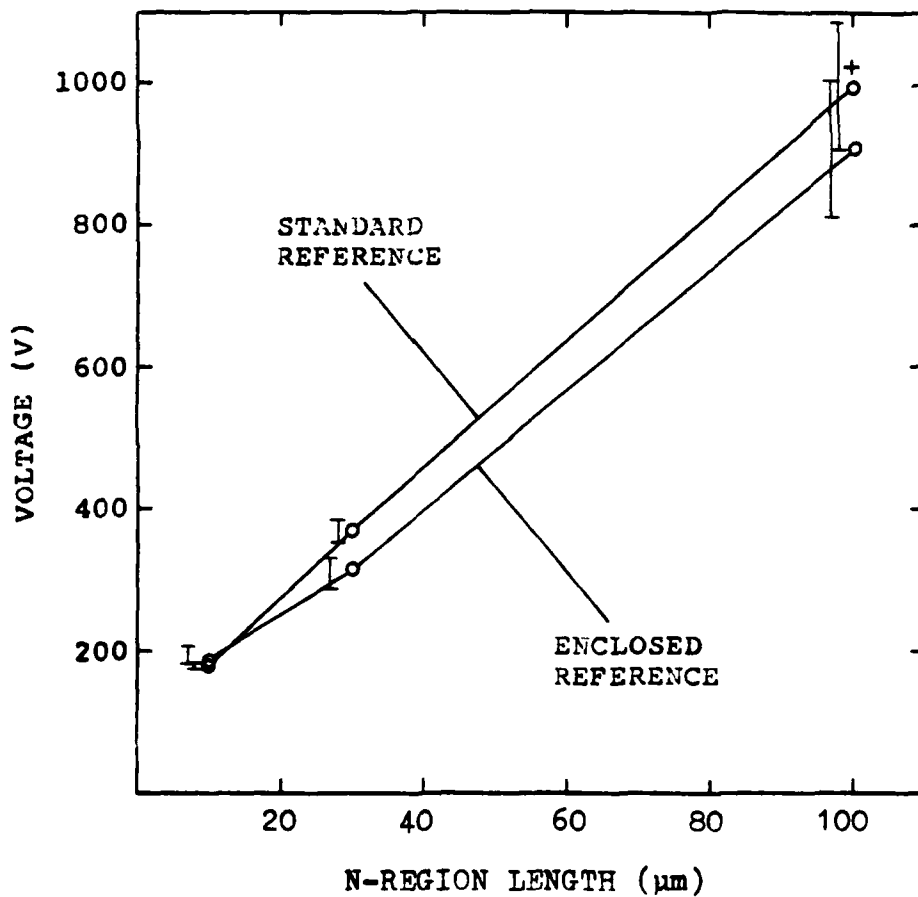


Fig. 52. Breakdown voltage versus n-region length for standard reference and enclosed reference diodes on Wafer 1-3. Error bars show one standard deviation above and below the mean. The plus sign indicates that some diodes could not be burned out at the maximum amplitude of the pulse generator.

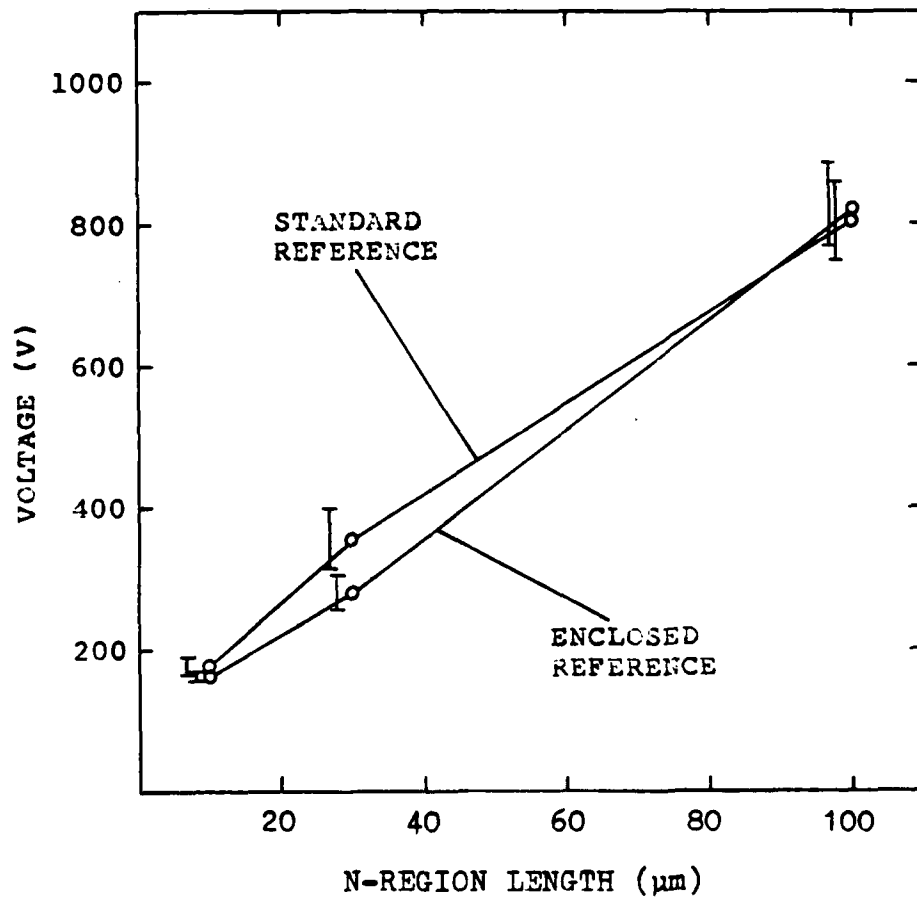


Fig. 53. Breakdown voltage versus n-region length for standard reference and enclosed reference diodes on Wafer 2-2. Error bars show one standard deviation above and below the mean.

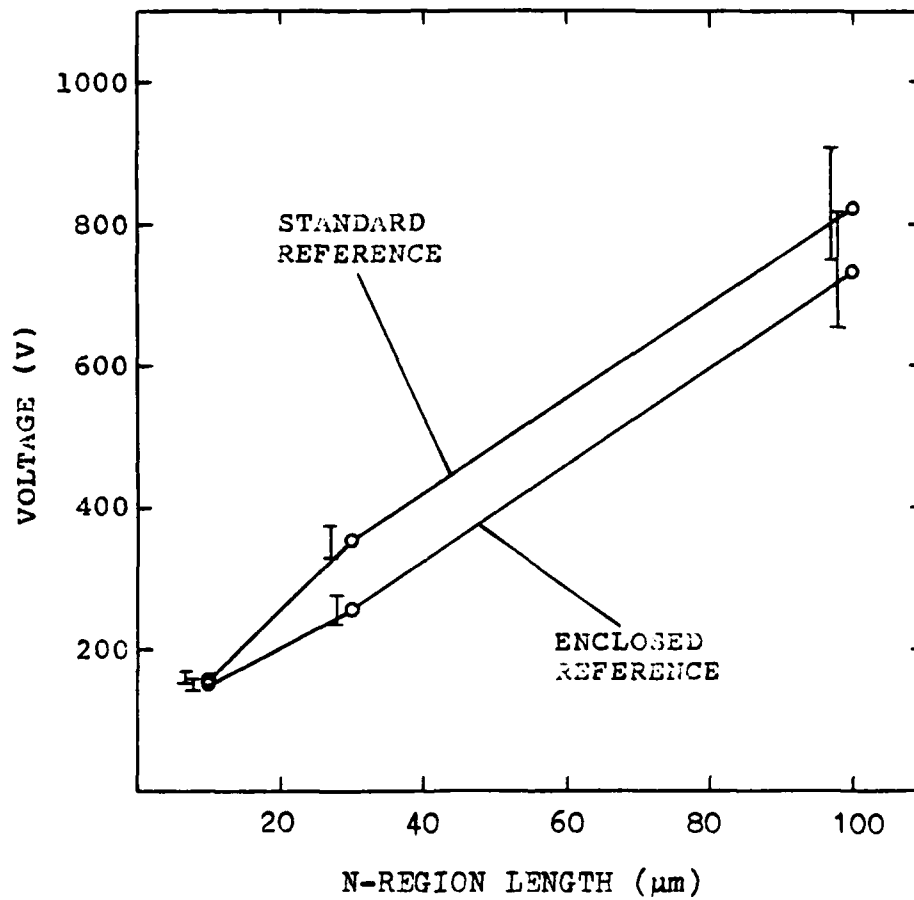


Fig. 54. Breakdown voltage versus n-region length for standard reference and enclosed reference diodes on Wafer 2-1. Error bars show one standard deviation above and below the mean.

Damage morphology from diodes of Wafers 2-4 and 1-3 for standard reference, p^+n spike, and metal- p^+ contact spike structures are shown in Fig. 55. Each group contains eight diodes. The diode on the right side of Fig. 55a with the longest n-region length (100 μm) was pulsed repeatedly after the damaging filament had formed to demonstrate the progressive damage that occurs with continued excitation. Damage of this extent would have occurred for most of the diodes shown in Fig. 55 on the failure pulse if current had not been limited by a 1 k Ω resistor. Figure 55 shows that the amount of damage tends to increase as the n-region length increases, often extending into the p^+ and n^+ areas for the 100 μm n-region length. Sometimes portions of the melt filament are vaporized.

The locations of filaments were investigated statistically by measuring filament endpoints on the p^+n and n^+n junctions for all of the diodes in the voltage threshold tests. Part of these data were then plotted in Figs. 56-60, and in Fig. 66.

Figure 56 shows the filament locations for diodes on Wafer 2-5. Approximately three hundred diodes are represented on this diagram. Each line connects the endpoints of the filament which destroyed a single diode. Numbers on the diagram indicate the number of diodes with filaments at a particular location. The first column shows filament locations for standard reference diodes. The second, third, and fourth columns show filament locations for enclosed reference, p^+n spike, and n^+n spike diodes, respectively. Each row contains diodes of the same n-region length, with rows 1, 2, 3, and 4 (top to bottom) having n-region lengths of 10, 30, 100, and 300 μm , respectively.

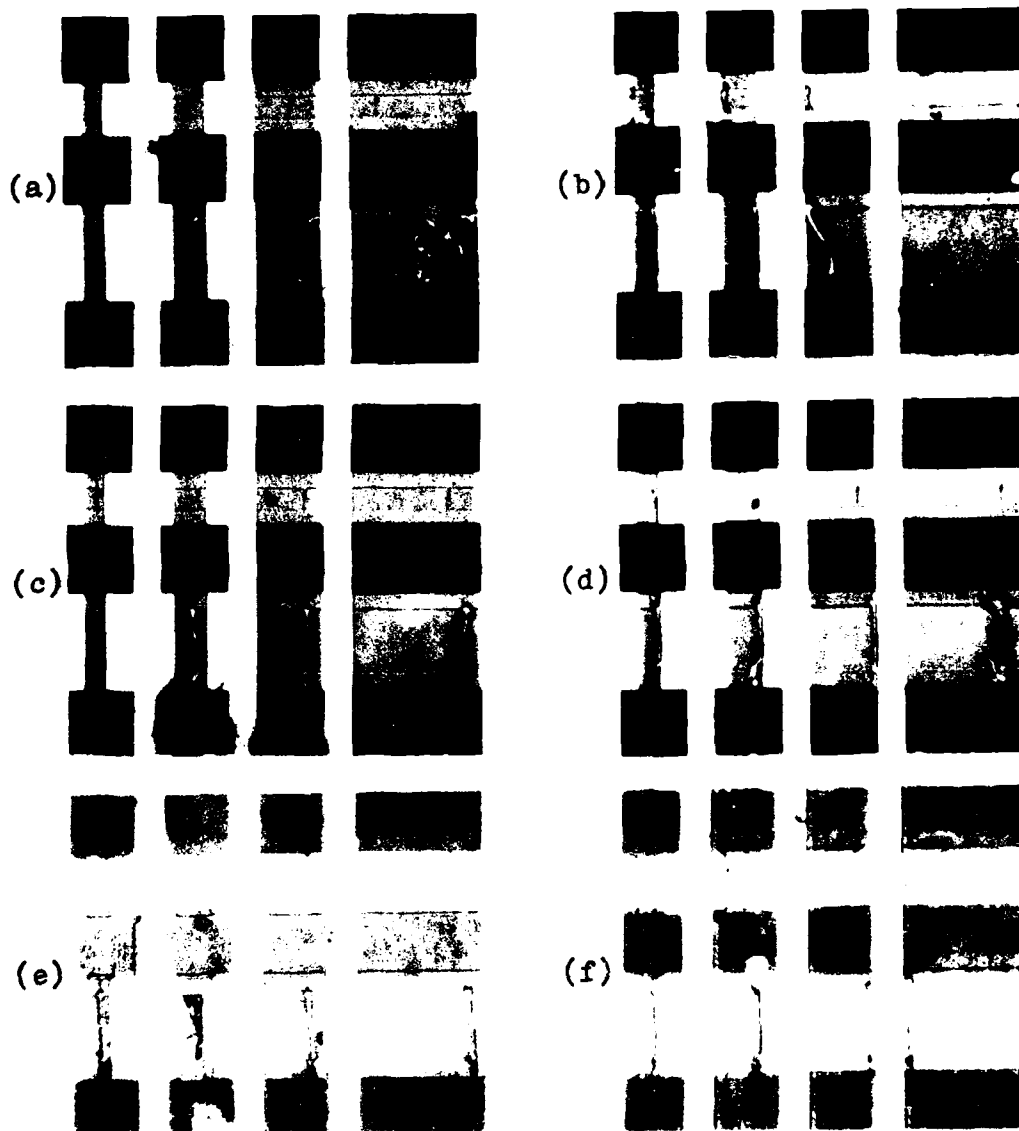


Fig. 55. Damage morphology due to 10 μ s pulses having amplitudes just above the damage threshold. All photographs except one (the diode in part (a) on the right with the longest n-region length) were taken after a single damaging pulse. (a) Standard reference diodes on Wafer 2-4. (b) Standard reference diodes on Wafer 1-3. (c) p-n spike diodes on Wafer 2-4. (d) p-n spike diodes on Wafer 1-3. (e) Metal-p⁺ spike diodes on Wafer 2-4. (f) Metal-p⁺ spike diodes on Wafer 1-3.

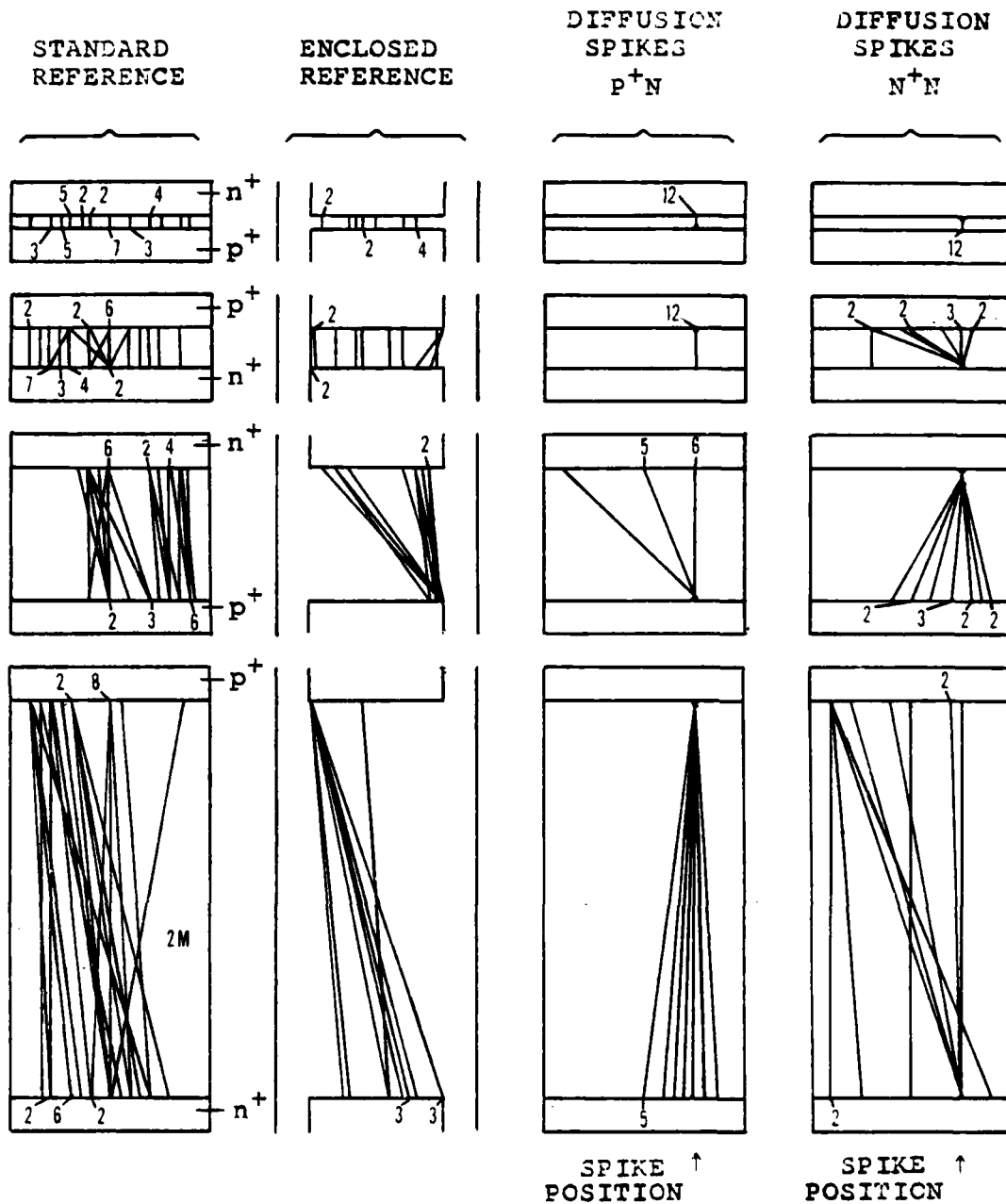


Fig. 56. Filament locations on the most highly doped wafer (Wafer 2-5). The n-region lengths of the above four rows are, from top to bottom, 10, 30, 100, and 300 μ m. The p^+ and n^+ region locations are similar for all diodes in a given row. Arrows show the horizontal position of the diffusion spikes.

In two diodes of Fig. 56 a melt filament did not form, but the metallization was damaged. This does not necessarily damage the p^+n junction, and may be evident only as an increased n-region resistance under forward bias. The two diodes, having the standard reference structure and n-region lengths of 300 μm , are indicated by "2M" on the diagram.

The filament locations shown in Fig. 56 were obtained from diodes with four different n-region widths: 30, 50, 100, and 200 μm . The filaments were drawn at their relative positions along the p^+n and n^+n junctions. For the enclosed reference diodes, wherein the protruding p^+n and n^+n contacts reduce the effective junction width, filaments were drawn relative to their positions along the protrusions. Each of the sixteen schematic diodes in Fig. 56 shows filament locations for all four n-region widths, in approximately equal proportions. Thus, the diode width in Fig. 56 is not significant. Not enough data were taken in these tests to discuss width effects, if any, in a statistically meaningful manner.

There is one other qualification concerning Fig. 56. The data on standard reference diodes of Fig. 56 include filament locations for both standard reference and contact spike diodes, since the contact spikes had no observable effect on the n-region filament locations, I-V characteristics, waveforms, or current configurations. There is an apparent grouping of the standard reference filaments on a particular side of the diode, which alternates from left to right as n-region length increases. This same grouping was observed separately for standard reference and contact spike diodes, in approximately the same de-

gree of importance. Since the contact spike is located on the right side of the diode for each n-region length (in the same horizontal position as the diffusion spikes), the grouping of the filaments is probably not related to the probe positions on the metallization contacts. Although it is possible that a systematic bias was introduced by the method of probe positioning, no such bias was suspected while the experiments were being performed.

It should be mentioned that filaments in contact spike diodes were frequently observed to extend to the metallization spike for the longer n-region lengths. However, the direction of the filament in the n-region usually made an angle with the direction in the highly doped region, suggesting that the contact spike had little effect prior to second breakdown. An example of this behavior is shown in Fig. 55e, for metal- p^+ contact spike diodes on Wafer 2-4 with n-region lengths of 30 and 100 μm . The spike is located on the upper right side of the 30 μm n-region length diodes, and on the lower right side of the 100 μm n-region length diodes. The filaments extend to the metal- p^+ spike for three of the diodes with n-region lengths of 100 μm . These diodes have the three shorter n-region widths.

The enclosed reference diodes in Fig. 56 have randomly distributed filaments for n-region lengths of 10 and 30 μm , but one endpoint of the filament tends to occur on the corner of the p^+n junction for longer n-region lengths. There appears to be some correspondence between the grouping of the standard and enclosed reference diode filaments. The reason for this grouping is not known.

The 5 μm diffusion spikes in Fig. 56 are difficult to see because they are drawn to scale. However, diffusion spikes have an important effect even if they are short compared to the n-region length. In Fig. 56, all of the filaments in the p^+n spike diodes have one endpoint at the tip of the spike. These filaments (initially hot spots) almost always start at the p^+n junction and grow toward the n^+n junction on Wafer 2-5, regardless of diode geometry. In observations of over three hundred diodes on Wafer 2-5, a hot spot originated on the n^+n junction in only one instance. Most of the filaments in n^+n spike diodes have one endpoint at the tip of the spike for n-region lengths of 10, 30, and 100 μm . Some of the n^+n spike diodes with an n-region length of 300 μm also have filament endpoints at the tip of the spike. Thus, both types of diffusion spikes are effective in localizing the current distribution at the second breakdown threshold. At the longest n-region length, p^+n spikes are more effective than n^+n spikes.

The effect of the n-region doping level on energy and voltage failure thresholds has been described previously. The role of n-region doping level on filament locations was also investigated. Figure 57 shows filament locations on Wafer 2-4. This diagram is similar to Fig. 56, except that the vertical scale has been expanded, and only diodes with n-region lengths of 10, 30, and 100 μm are shown.

The filaments in standard reference diodes of Fig. 57 exhibit the same tendency to be grouped on a particular side of the diode as the corresponding diodes in Fig. 56. In addition, all of the filaments in diffusion spike diodes in Fig. 57 have one endpoint at the tip of the spike. The only significant difference between Fig. 56 and Fig. 57 is

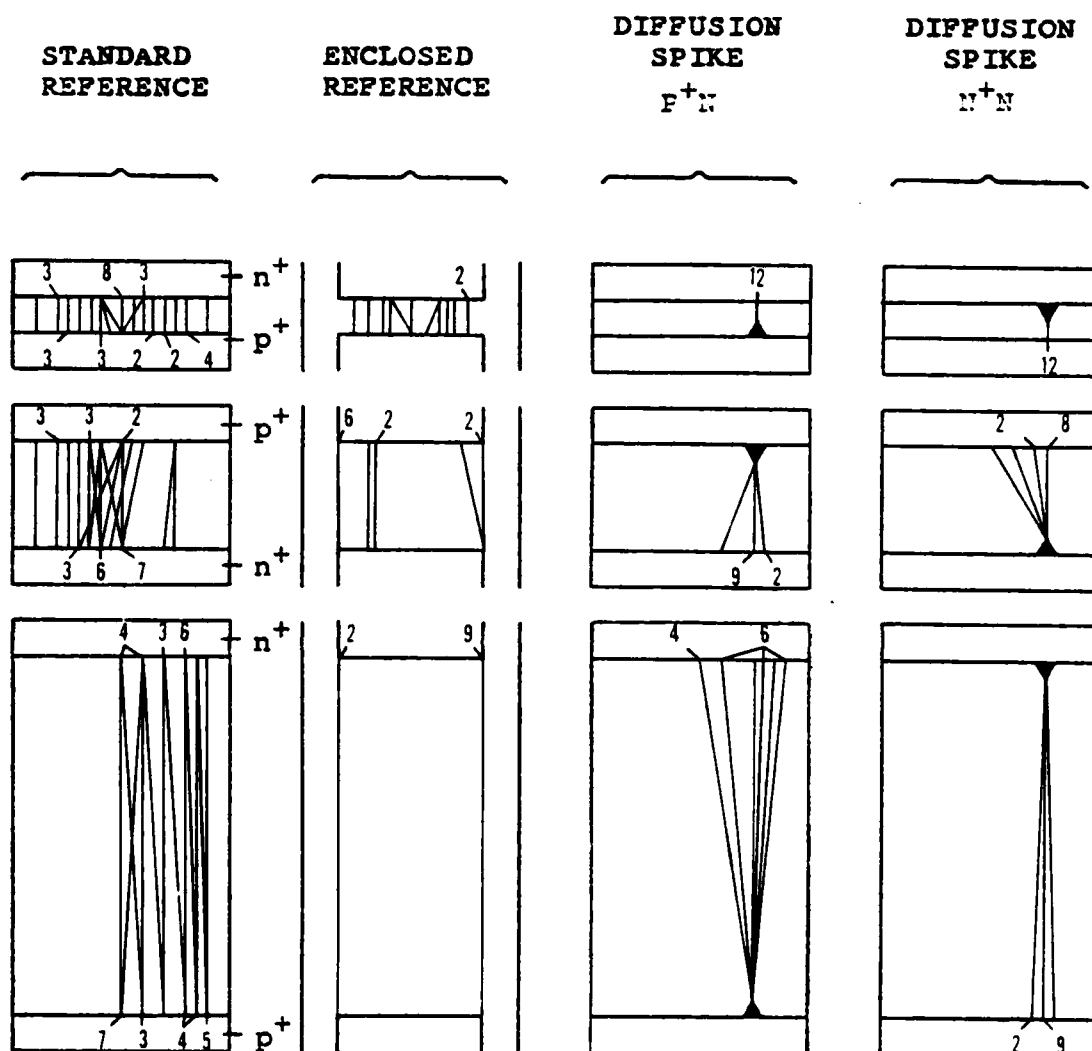


Fig. 57. Filament locations on Wafer 2-4. The n-region lengths of the above three rows are, from top to bottom, 10, 30, and 100 μ m. The p^+ and n^+ region locations are similar for all diodes in a given row.

in the locations of filaments in enclosed reference diodes. The influence of junction corners in determining filament locations is not as strong in Fig. 56 as in Fig. 57. Filaments in enclosed reference diodes of Fig. 57 tend to have endpoints on both the p^+n and n^+n junction corners for n -region lengths of 30 and 100 μm . In general, however, the filament locations in Fig. 56 and Fig. 57 are very similar. Thus, filament locations are insensitive to doping level in the range between the two highest nominal doping densities.

However, there is a transition between the two higher and the three lower doping levels, as illustrated in Fig. 55. Comparison of the filament locations in standard reference, p^+n diffusion spike, and metal- p^+ contact spike diodes on Wafers 2-4 and 1-3 shows that a significant number of filaments lie along the diode edges for diodes on Wafer 1-3. Thus, the diode edges have an important effect in determining filament locations at the lower doping density. This is discussed in more detail below.

The filament locations in Wafers 1-3, 2-2, and 2-1 are shown in Figs. 58, 59, and 60, respectively. These three wafers all display similar damage characteristics and are discussed together. Some of the longest diodes on Fig. 58 could not be destroyed at the maximum amplitude setting of the Velonex pulser; the number of such diodes is shown on the diagram followed by a question mark.

The diode edges have an important effect in each of Figs. 58-60. Most of the filaments in standard reference diodes are along either the left or the right edge of the diode, for all three n -region lengths. In a few cases, the filaments are close to, but not along, the diode

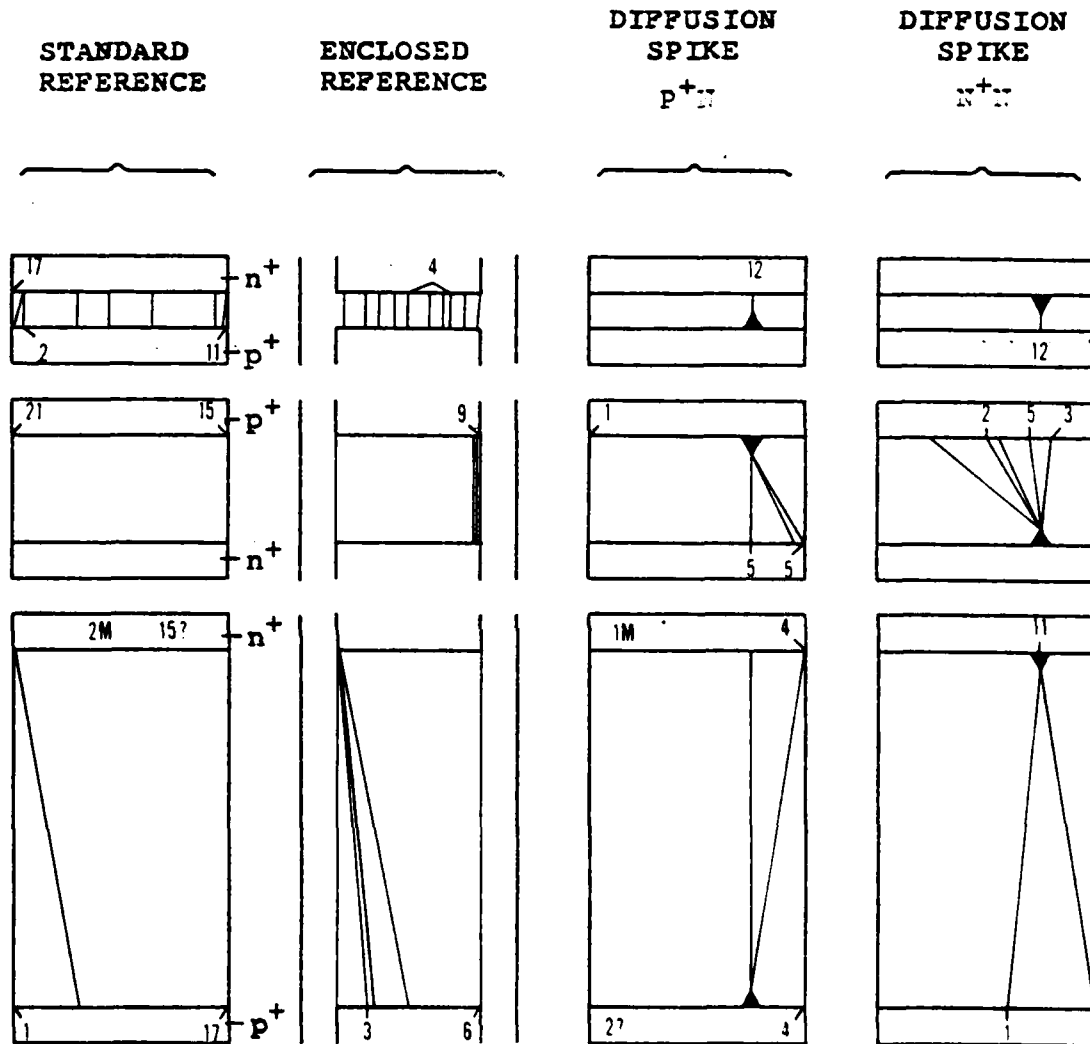


Fig. 58. Filament locations on Wafer 1-3. The n-region lengths of the above three rows are, from top to bottom, 10, 30, and 100 μ m. The p^+ and n^+ region locations are similar for all diodes in a given row.

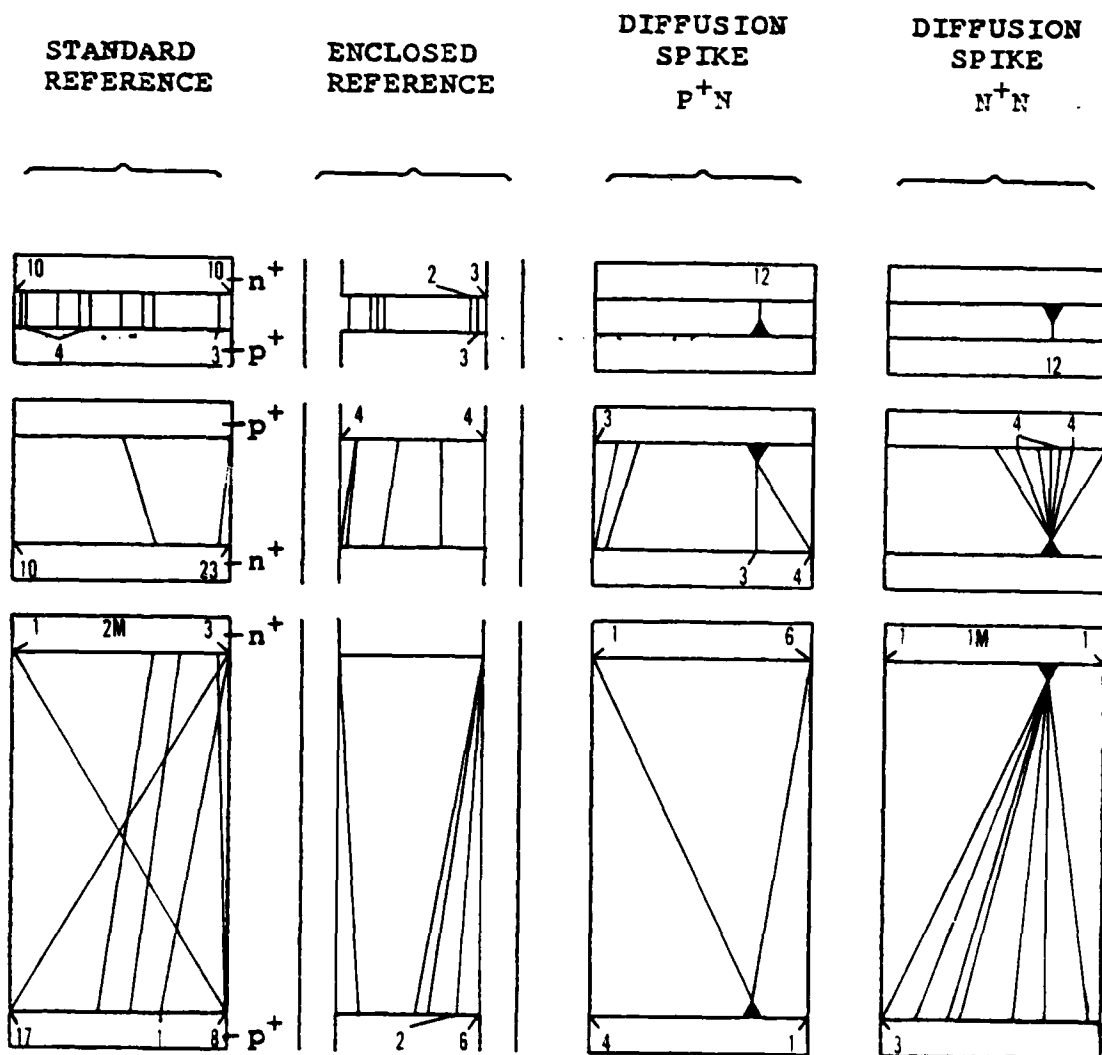


Fig. 59. Filament locations on Wafer 2-2. The n-region lengths of the above three rows are, from top to bottom, 10, 30, and 100 μ m. The p^+ and n^+ region locations are similar for all diodes in a given row.

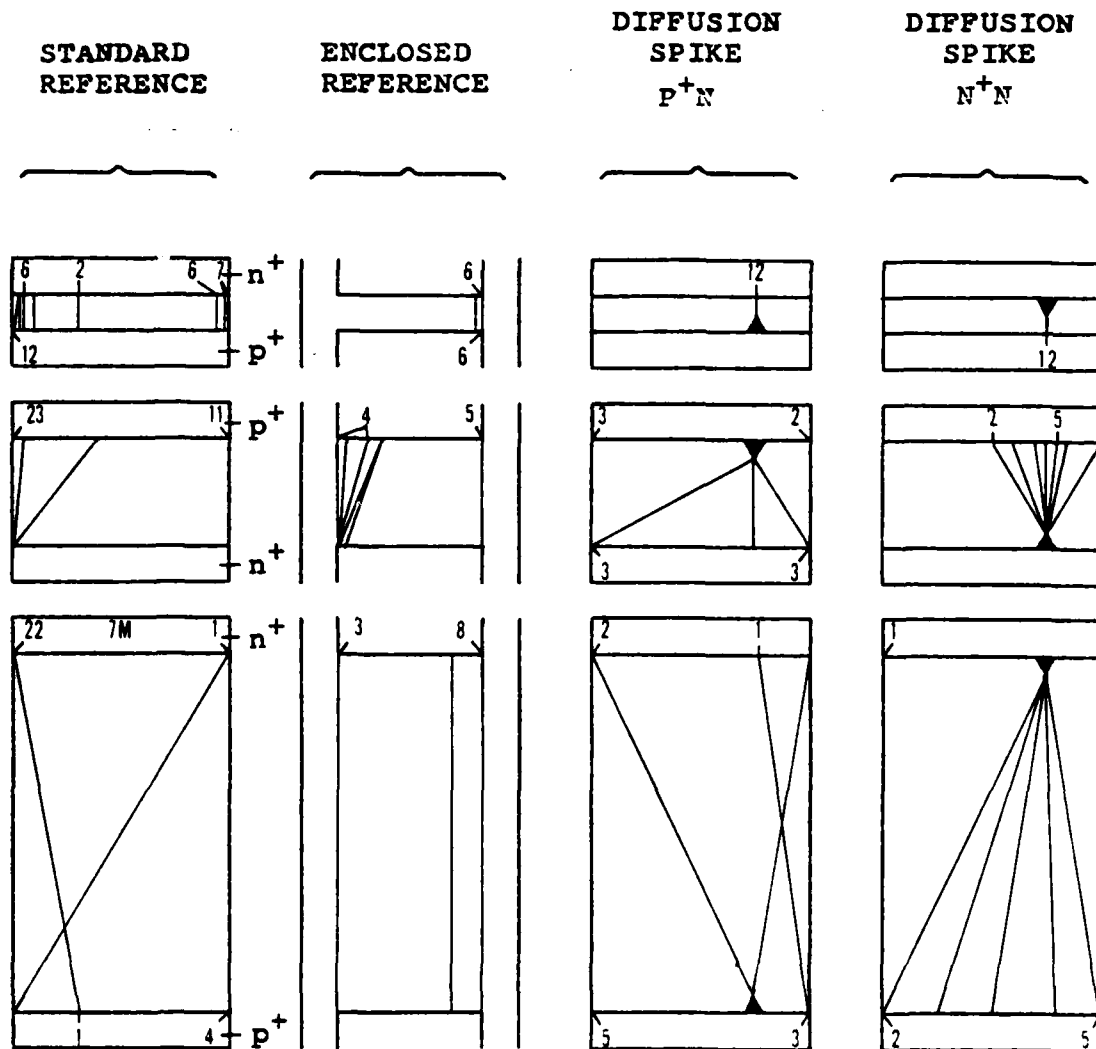


Fig. 60. Filament locations on Wafer 2-1. The n-region lengths of the above three rows are, from top to bottom, 10, 30, and 100 μ m. The p^+ and n^+ region locations are similar for all diodes in a given row.

edges. The p^+n and n^+n spikes still play an important role in determining filament location, but this role is modified by edge effects for n -region lengths of 30 and 100 μm .

The damage morphology is actually more complicated than the simplified diagrams of Figs. 58-60 because these diagrams do not plot the paths of the filaments between their endpoints. For example, the filament starts at a diffusion spike, goes to the diode edge, and runs along the edge to the opposite junction. Filaments in enclosed reference diodes sometimes divide into three fairly straight sections, two connecting the junction corners with the diode edge and the third running along the diode edge. Thus, diode edges have an important effect in standard reference, enclosed reference, and diffusion spike diodes. A possible explanation for this edge preference is that the processing steps cause an increase in conductivity along the diode edge. Properties that distinguish the edges from the remainder of the silicon island include heat sinking, electrical conductivity, diffusion properties, defects in the oxide layer (characteristic of silicon-on-sapphire technology) and the orientation of the silicon surface exposed to the oxide layer^{44,46,47,51}. Not enough data were taken to attempt to correlate filament locations with voltage thresholds. No obvious correlation exists between low threshold and edge damaging filament.

In summary, both junction corners and diffusion spikes have an important influence in determining filament locations for all five nominal doping densities. The diode edges exert an additional influence for the three lower nominal doping densities.

4. Multiple Spike Diodes

The comparison of standard reference and diffusion spike diodes has so far been concerned with single spikes, 5 μm in length, located about 1/4 of the way from the diode edge. Heating pattern, voltage threshold, and filament location tests were also performed using multiple spike diodes, with spikes varying in length from 1 to 8 μm , and with n-region lengths of 10, 30, and 100 μm . The voltage threshold tests were conducted for both types of diffusion spikes, on four different wafers. Heating patterns and filament locations were investigated on Wafer 2-5. Energy and current thresholds were not determined. However, both energy and current thresholds have been described for diodes with no spikes and diodes with 5 μm spikes.

Figure 61 shows reverse bias tests of three p^+n multiple spike diodes on Wafer 2-5. The n-region lengths of these diodes are 10, 30, and 100 μm , from top to bottom. The diodes each have three large spikes, 4 μm in length, on a continuous background of 1 μm spikes. The diodes have a common width of 200 μm . Current and voltage waveforms are shown to the right of the heating patterns. All three diodes are close to their second breakdown thresholds.

In each diode of Fig. 61, the heating is fairly uniform in the n-region, and also along the continuous background of 1 μm spikes. However, there are three hot spots at the tips of the three large diffusion spikes. The amplitudes of the current and voltage waveforms, and the current interval between formation of hot spots and second breakdown, are similar to those of diodes having a single p^+n spike with corresponding geometry and doping level. If the current level is in-

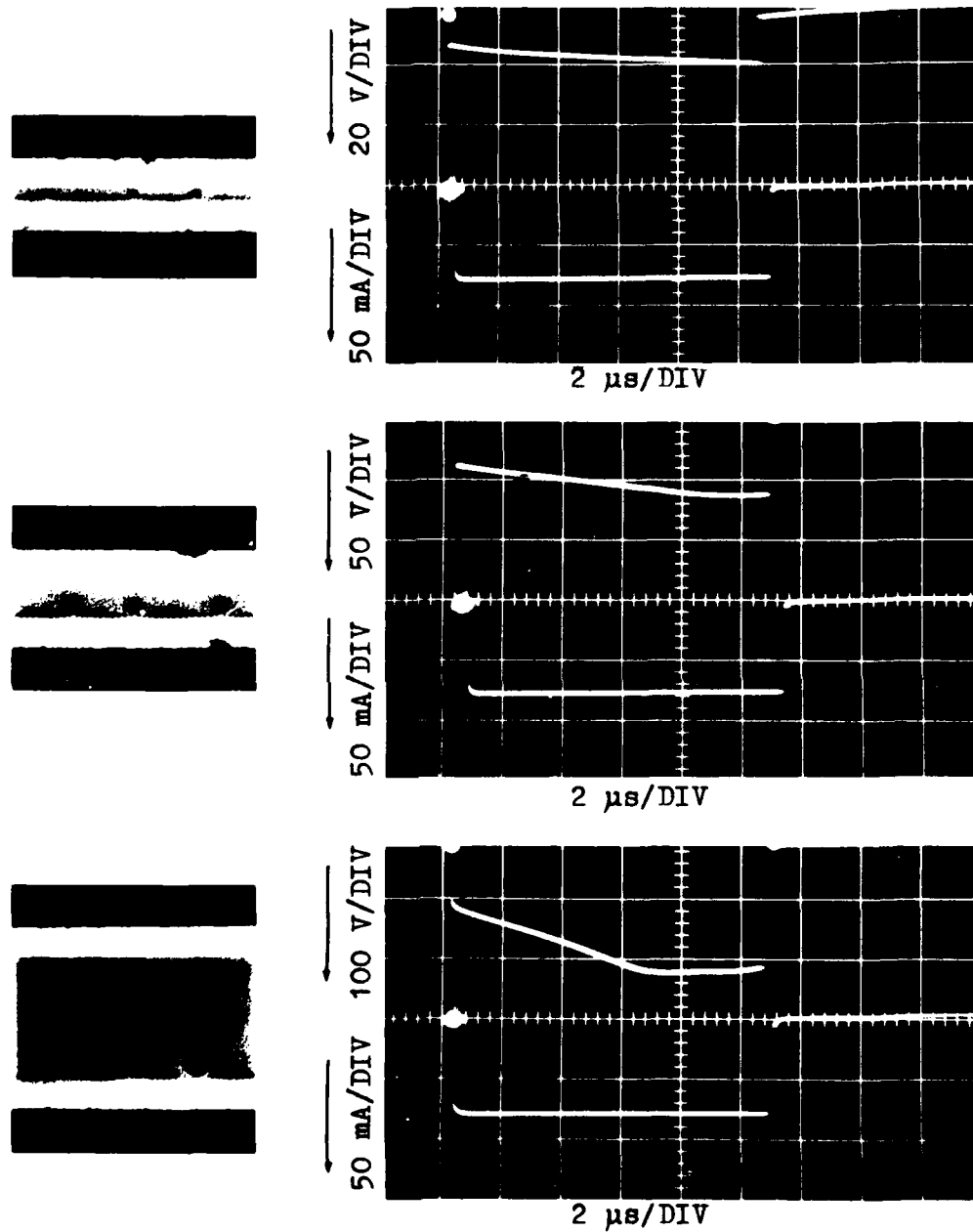


Fig. 61. Reverse bias tests of three p⁺n multiple spike diodes on Wafer 2-5. The n-region lengths are, from top to bottom, 10, 30, and 100 μm. Voltage (upper trace) and current (lower trace) waveforms are shown for each case.

creased sufficiently, one of the hot spots extends all the way across the n-region and a melt filament forms, damaging the diode. This behavior is also typical of p^+n spike diodes with spike lengths from 2 to 8 μm . Hot spots do not form at regular positions along the junctions of p^+n multiple spike diodes having only the continuous background of 1 μm spikes.

The behavior of n^+n multiple spike diodes is similar to that of diodes with a single n^+n spike. The heating pattern is generally very uniform until the diode is close to the second breakdown threshold. Usually, only a single hot spot forms prior to second breakdown, although multiple hot spots have been observed in a few cases. This hot spot tends to be located opposite, or nearly opposite, one of the three large diffusion spikes. If the pulse amplitude is increased slightly, the hot spot extends all the way across the n-region, usually to the tip of the spike, and a melt filament forms, damaging the diode.

Thus, each of the three large diffusion spikes in p^+n multiple spike diodes serves as a concentration center for the current. However, n^+n multiple spike diodes tend to behave as diodes having only a single n^+n spike.

Plots of voltage failure thresholds of multiple spike structures versus spike length were made for four of the five nominal doping densities. Data on diodes from Wafer 2-5 are shown in Fig. 62 for p^+n multiple spike diodes (solid circles) and n^+n multiple spike diodes (open circles). The diodes have n-region lengths of 10, 30, and 100 μm . Each point is the average of eight measurements; error bars show one standard deviation above and below the mean. For a spike length of

AD-A086 345

AUBURN UNIV ALA DEPT OF PHYSICS
SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)
MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAAG29-78-6-0111

F/G 9/1

UNCLASSIFIED

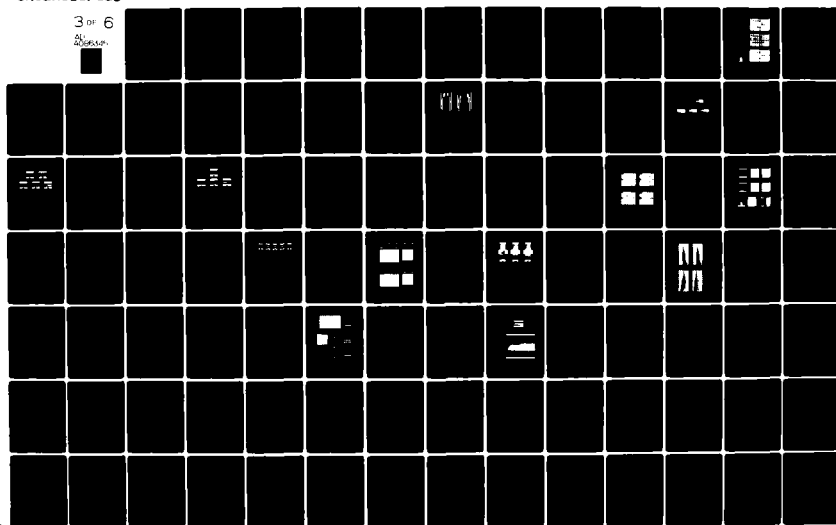
ARO-15840.3-A-EL

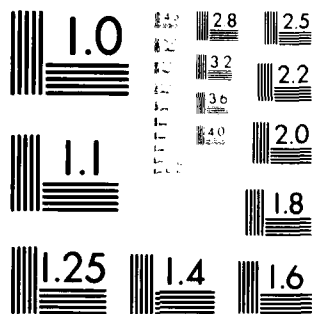
NL

3 OF 6

AL

2000000





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

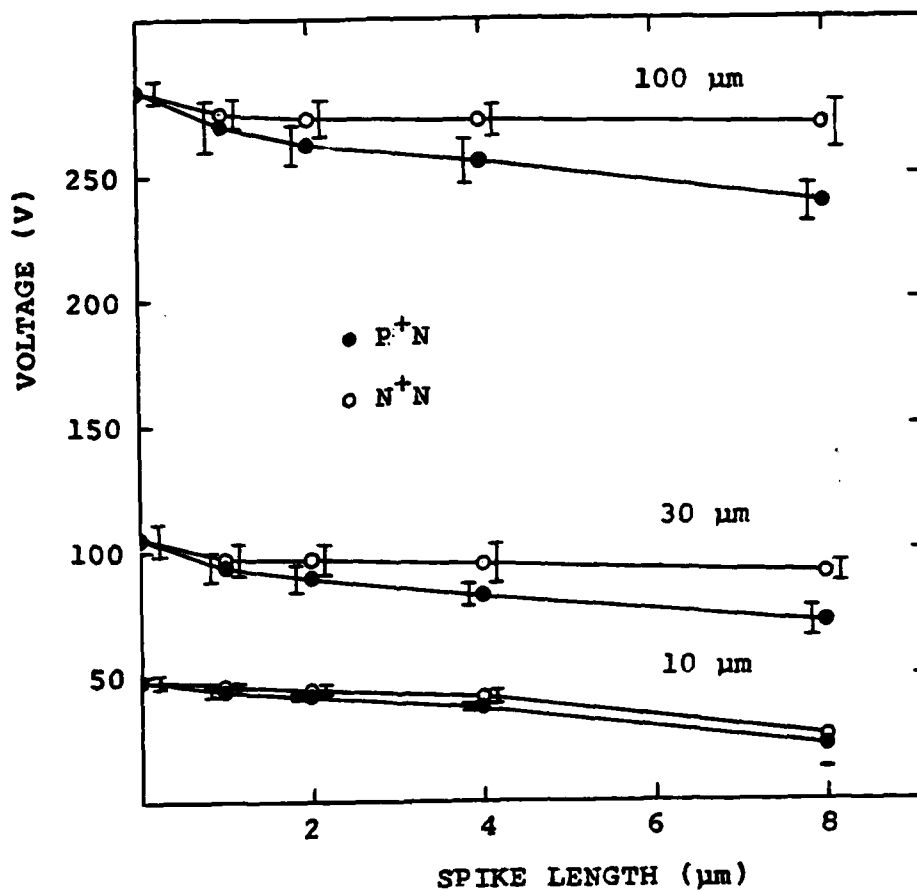


Fig. 62. Breakdown voltage versus spike length for multiple diffusion spike diodes on Wafer 2-5. The n-region lengths for the top, middle, and bottom curves are 100, 30, and 10 μm , respectively. Each point is the average of eight diodes; error bars show the standard deviation of the eight measurements. The minus sign indicates that some diodes were burned out at the minimum amplitude of the pulse generator.

8 μm and an n-region length of 10 μm , some of the diodes failed at the minimum amplitude setting of the Velonex pulser. When this occurred, the minimum setting was taken as the failure voltage. The spike lengths of 2, 4, and 8 μm represent three large spikes on a continuous background of 1 μm spikes. The spike length of 1 μm represents only the continuous background of 1 μm spikes. Voltage failure thresholds of diodes with no spikes along the junction are also shown on this diagram, plotted as a spike length of 0 μm . All of the multiple spike diodes have a constant width of 200 μm .

The dependence of voltage failure thresholds on n-region length is similar for multiple and single diffusion spike diodes. Examination of the data in Tables 8-12 shows that multiple spike diodes with spike lengths of 4 μm fail at voltages which are close to those of corresponding diodes with a single 5 μm spike. Since plots of voltage failure thresholds versus n-region length for single diffusion spike diodes were described in Section V.F.2., similar plots for multiple spike diodes are not presented. The relative importance of the type of diffusion spike, and of spike length on voltage failure thresholds will be examined.

For a 10 μm n-region length there is a significant decrease in voltage failure thresholds with increasing spike length for both types of multiple spike diodes. The depletion width is about 3 μm for the doping level of Wafer 2-5, so that punchthrough occurs at the site of the 8 μm spike for 10 μm n-region length. The voltage threshold decreases slightly with increasing spike length for 30 and 100 μm n-region lengths. However, the voltage failure thresholds of n^+n

multiple spike diodes with different spike lengths are statistically the same for constant n-region lengths of 30 and 100 μm . Figure 62 indicates that p^+n multiple spikes are more effective than n^+n multiple spikes in reducing the voltage failure thresholds on Wafer 2-5.

The voltage failure thresholds of multiple spike diodes on Wafer 2-4 are plotted versus diffusion spike length in Fig. 63. This diagram is similar to Fig. 62 except that individual points represent an average of three measurements, instead of eight. Error bars show the maximum and minimum of the three measurements. Diodes, with 10 μm n-region length and 8 μm spikes, were burned out at the minimum amplitude setting of the Velonex pulser in Figs. 63, 64, and 65.

The voltage failure thresholds of p^+n and n^+n multiple spike diodes are approximately equal for n-region lengths of 10, 30, and 100 μm , except for one condition. There is a significant difference between the two for the 100 μm n-region length when the spike length is 8 μm . The voltage failure thresholds of p^+n and n^+n multiple spike diodes have overlapping ranges for all spike sizes, for 10 and 30 μm n-region lengths. The n^+n multiple spikes are slightly more effective than p^+n multiple spikes in reducing the voltage failure thresholds of diodes on Wafer 2-4. On Wafer 2-5, p^+n multiple spikes were found to be more effective than n^+n multiple spikes in reducing voltage failure thresholds. Single p^+n spikes were also more effective than single n^+n spikes in reducing the voltage failure thresholds on Wafer 2-5, while the reverse was true on Wafer 2-4, as shown in Figs. 44 and 45.

The voltage failure thresholds of diodes on Wafers 1-3 and 2-2 are plotted versus diffusion spike length in Figs. 64 and 65, respectively.

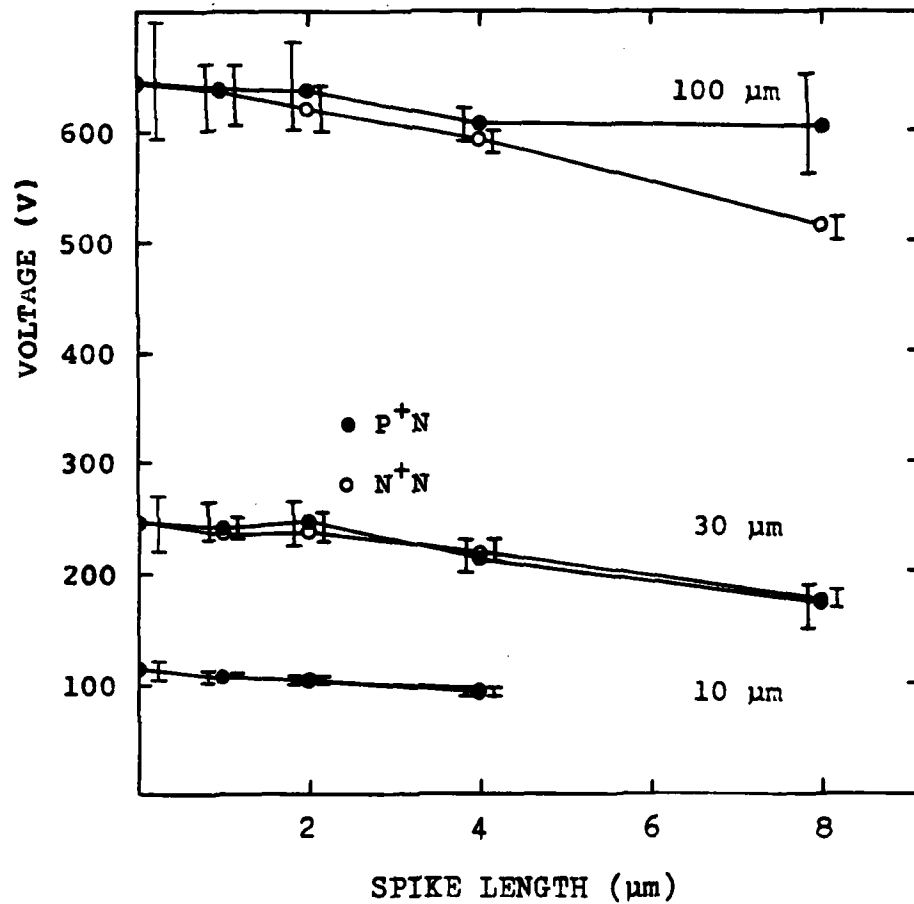


Fig. 63. Breakdown voltage versus spike length for multiple diffusion spike diodes on Wafer 2-4. The n-region lengths for the top, middle, and bottom curves are 100, 30, and 10 μm, respectively. Each point is the average of three diodes; error bars show the maximum and minimum of the three measurements.

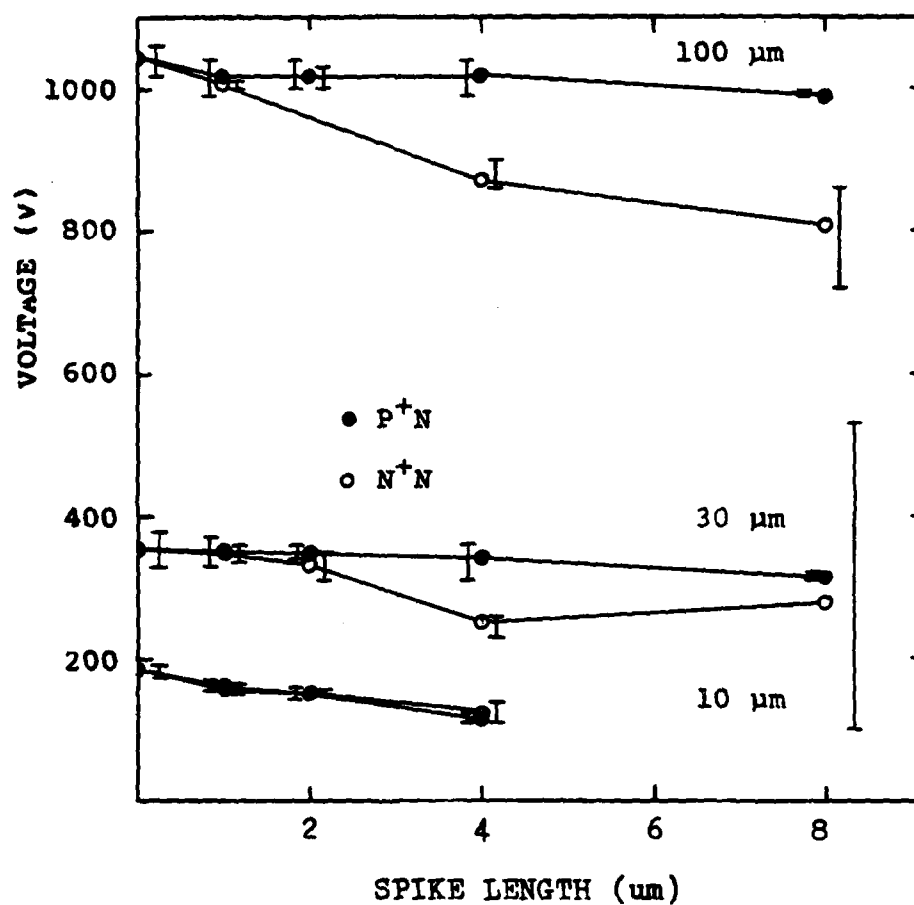


Fig. 64. Breakdown voltage versus spike length for multiple diffusion spike diodes on Wafer 1-3. The n-region lengths for the top, middle, and bottom curves are 100, 30, and 10 μm , respectively. Each point is the average of three diodes; error bars show the maximum and minimum of the three measurements.

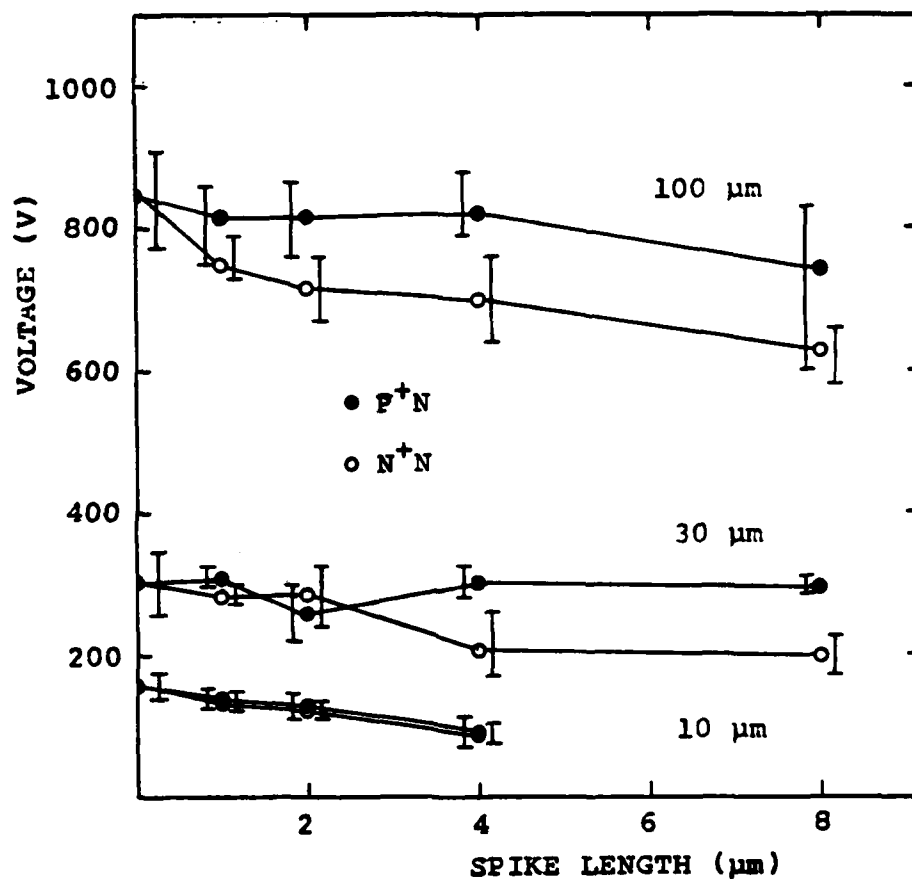


Fig. 65. Breakdown voltage versus spike length for multiple diffusion spike diodes on Wafer 2-2. The n-region lengths of the top, middle, and bottom curves are 100, 30, and 10 μm, respectively. Each point is the average of three diodes; error bars show the minimum and maximum of the three measurements.

Overall features are similar to those of Fig. 63. The n^+n spikes tend to lower voltage thresholds more than p^+n spikes at n -region lengths of 30 and 100 μm . However, the wide spread in portions of the data preclude stronger conclusions.

In summary, increasing spike height decreases voltage thresholds by amounts that depend upon n -region length, doping level, and junction containing the spikes. The voltage failure thresholds of p^+n and n^+n multiple spike diodes for 10 μm n -region length decrease with increasing spike length for all doping densities, and p^+n and n^+n spikes lower the thresholds by the same amounts for the same size spikes. For 100 μm n -region length, p^+n spikes lower the voltage threshold more than n^+n spikes for the highly doped diodes of Wafer 2-5, while the reverse is true for the more lightly doped diodes of Wafers 2-4, 1-3, and 2-2. At the intermediate n -region length of 30 μm , the same reversal occurs, but after the doping density becomes less than that of Wafer 2-4. Multiple spikes lower the thresholds, for a given spike size, doping level, and n -region length, by the same amount as does a single spike.

Filament locations in both p^+n and n^+n multiple spike diodes, with three different n -region lengths, were investigated on Wafer 2-5, but not on other wafers. These data were obtained during the voltage threshold tests described previously and are shown in Fig. 66. The first column shows diodes with a continuous background of 1 μm spikes, while the second through fourth columns show diodes with three larger spikes on a continuous background of 1 μm spikes. The lengths of the three larger spikes are 2, 4, and 8 μm , for the second, third, and fourth columns, respectively. The upper three rows show p^+n multiple

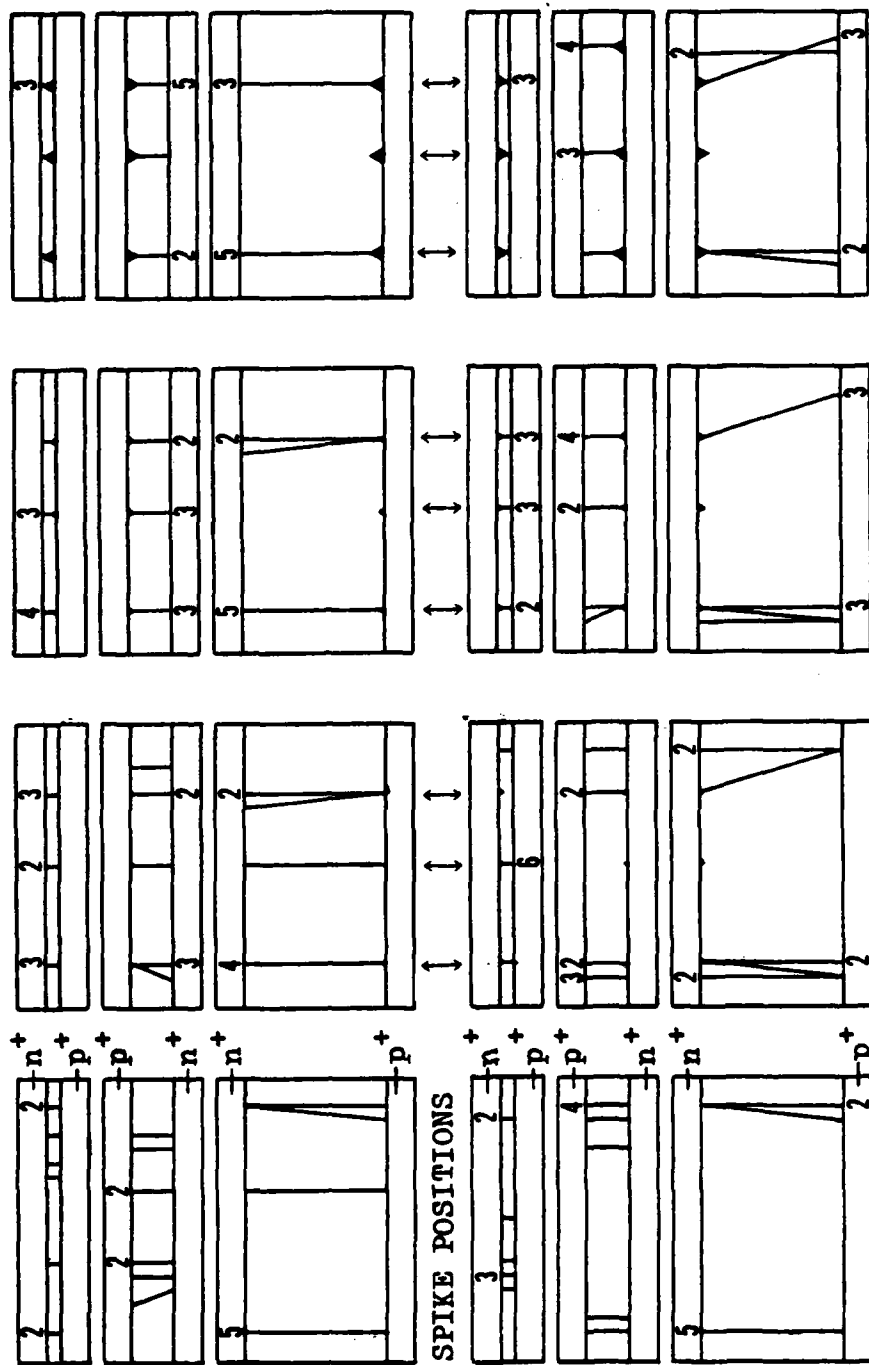


Fig. 66. Filament locations on multiple diffusion spike diodes on Wafer 2-5. The upper three rows are p-n diffusion spike diodes and the lower three rows are n-p diffusion spike diodes. The spike lengths of the above four columns are, from left to right, 1, 2, 4, and 8 μm .

spike diodes with n-region lengths of 10, 30, and 100 μm , while the lower three rows show the corresponding n^+n multiple spike diodes. The n-region length-to-width ratio, and the relative sizes of the diffusion spikes, are drawn to scale for each of the schematic diodes in Fig. 66. As in previous filament location diagrams, numbers above the lines indicate the number of diodes with a melt filament at a particular location. Data on approximately 200 diodes are represented in Fig. 66.

The p^+n multiple spikes are very effective in influencing filament locations in Wafer 2-5. All of the filaments in p^+n multiple spike diodes with spike lengths of 2, 4, and 8 μm , except one, have one endpoint at the tip of one of the three large spikes. In most cases, the filaments are perpendicular to the diode width. The filaments in p^+n multiple spike diodes with only a continuous background of 1 μm spikes are located in more or less random positions.

The n^+n multiple spikes in Wafer 2-5 also influence filament locations, but they are not as effective as p^+n multiple spikes. Most of the filaments in n^+n multiple spike diodes with spike lengths of 4 and 8 μm have one endpoint at the tip of one of the three large spikes. However, only half of the filaments in diodes with a spike length of 2 μm have an endpoint at one of the three large spikes, for n-region lengths of 30 and 100 μm . The filaments in n^+n multiple spike diodes with only a continuous background of 1 μm spikes are located in random positions along the junctions.

Thus, p^+n multiple spikes are effective in influencing filament locations at spike lengths of 2, 4, and 8 μm , and n-region lengths of 10, 30, and 100 μm . Multiple spikes on the n^+n junction influence

filament locations, but 50% of the melt filaments occur elsewhere in multiple spike diodes with spike lengths of 2 μm , and n-region lengths of 30 and 100 μm .

G. Radius of Curvature Diodes

This section describes heating pattern, voltage threshold, and filament location tests performed on diodes with curved p^+n and n^+n junctions. Heating patterns were observed on Wafer 2-5, while voltage thresholds and filament locations were investigated for each of the five nominal doping densities.

The heating patterns close to the second breakdown threshold of three radius of curvature diodes on Wafer 2-5 under reverse bias are shown in Fig. 67. Each diode has a width of 200 μm , and a minimum separation between the p^+n and n^+n junctions of 100 μm . For the p^+n junctions, curvatures are, from top to bottom, 5, 10, and 30 μm . The current and voltage waveforms were obtained with constant current pulses, and are shown to the right of the heating pattern photographs.

A single hot spot is found in each of the three heating pattern photographs at a point on the p^+n junction where the p^+n and n^+n junctions are separated by a minimum distance. The hot spots in each of the three diodes are similar, indicating that the radius of curvature of the p^+n junction does not have a significant effect on either the hot spot shape or size. The heating patterns in Fig. 67 also show that current concentrates near the n^+n junction, in the vicinity of the point where it is closest to the p^+n junction. Observations of other diodes with varying radii of curvature and n-region lengths show that hot spots always form at the point of minimum separation between the

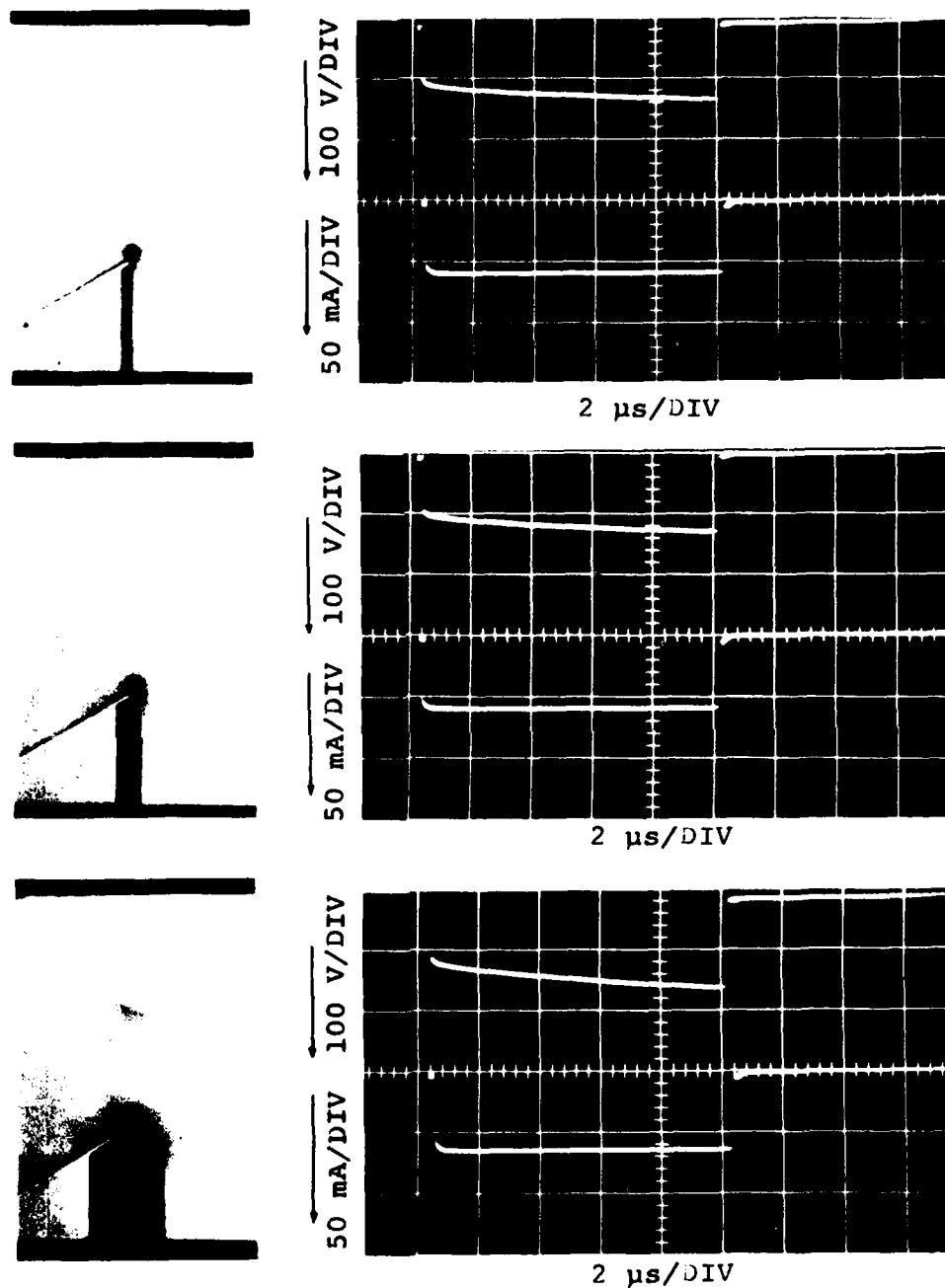


Fig. 67. Reverse bias tests of three radius of curvature diodes on Wafer 2-5. Each diode has a width of $200\text{ }\mu\text{m}$, and a minimum separation between the p^+n and n^+n junctions of $100\text{ }\mu\text{m}$. The p^+n junction curvatures are, from top to bottom, 5 , 10 , and $30\text{ }\mu\text{m}$. Voltage (upper trace) and current (lower trace) waveforms are shown for each case.

two junctions, and that there are never multiple hot spots. Thus, the radius of curvature geometry is very effective in localizing the current distribution near the second breakdown threshold. The voltage and current waveform pairs in Fig. 67 are fairly similar, indicating the diode current, voltage, and energy failure thresholds are independent of p^+n junction curvature in the range considered. However, current and energy thresholds were not measured.

The voltage failure thresholds of standard reference and radius of curvature diodes on Wafers 2-5 and 2-4 are shown in Figs. 68 and 69, respectively. The minimum separation between the p^+n and n^+n junctions was taken as the n -region length for radius of curvature diodes. The individual points showing voltage failure thresholds of radius of curvature diodes are averages of approximately nine measurements, representing three different radii of the p^+n junction. The measurements of voltage failure thresholds in standard reference diodes have been described previously.

The general behavior observed in Figs. 68 and 69 is similar, so these diagrams are discussed together. The voltage failure thresholds of standard reference and radius of curvature diodes are very close for n -region lengths of 10 and 30 μm , indicating that junction curvature does not cause a major reduction in the voltage failure thresholds of these diodes. However, the voltage failure thresholds of radius of curvature diodes with an n -region length of 100 μm are significantly less than those of corresponding standard reference diodes.

The voltage failure thresholds of standard reference and radius of curvature diodes on Wafers 1-3, 2-2, and 2-1 are shown in Figs. 70-72,

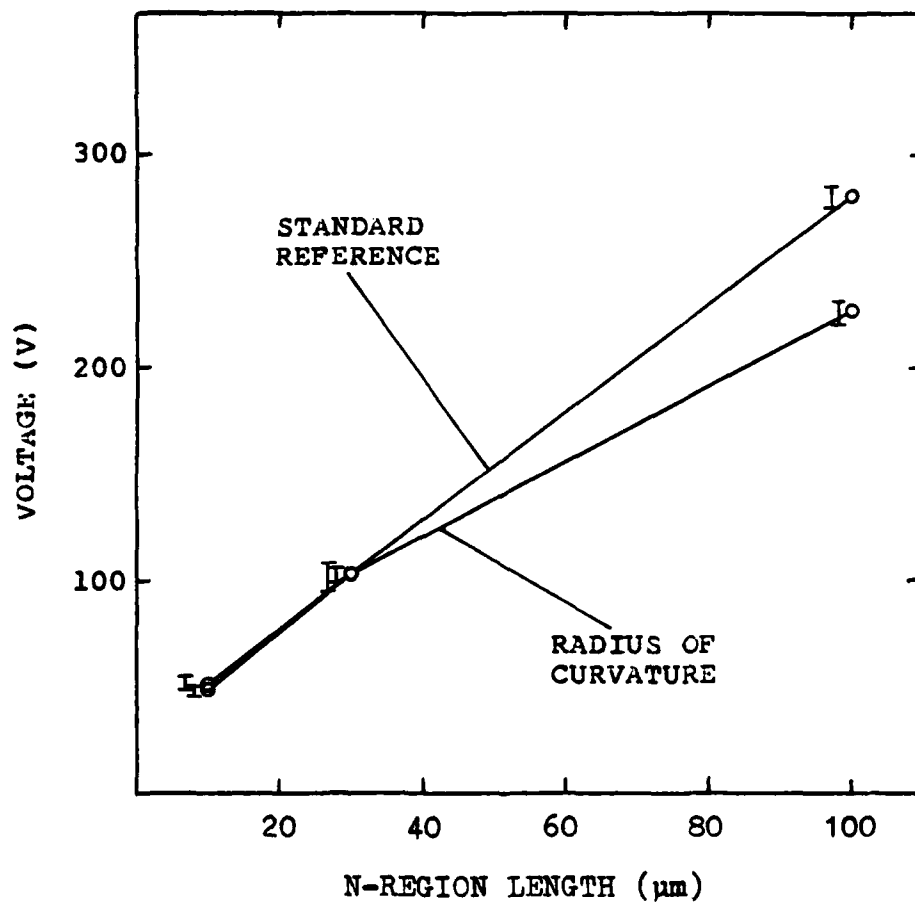


Fig. 68. Breakdown voltage versus n-region length for standard reference and radius of curvature diodes on Wafer 2-5. Error bars show one standard deviation above and below the mean.

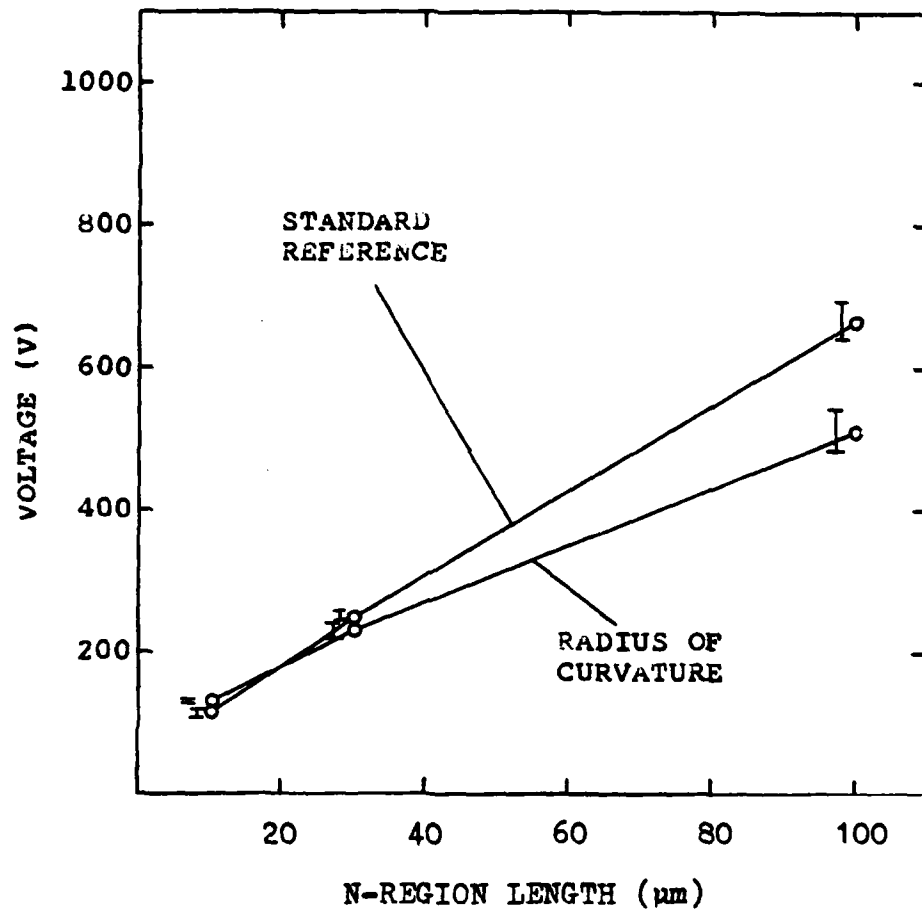


Fig. 69. Breakdown voltage versus n-region length for standard reference and radius of curvature diodes on Wafer 2-4. Error bars show one standard deviation above and below the mean.

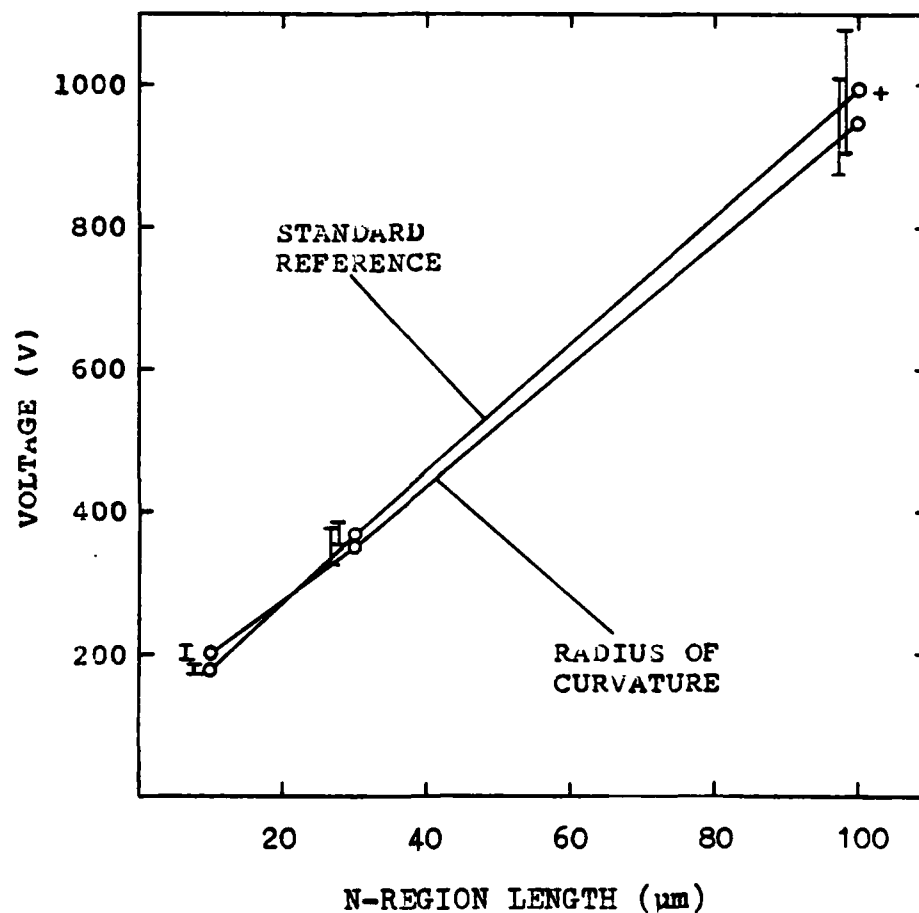


Fig. 70. Breakdown voltage versus n-region length for standard reference and radius of curvature diodes on Wafer 1-3. Error bars show one standard deviation above and below the mean. The plus sign indicates that some diodes could not be burned out at the maximum amplitude of the pulse generator.

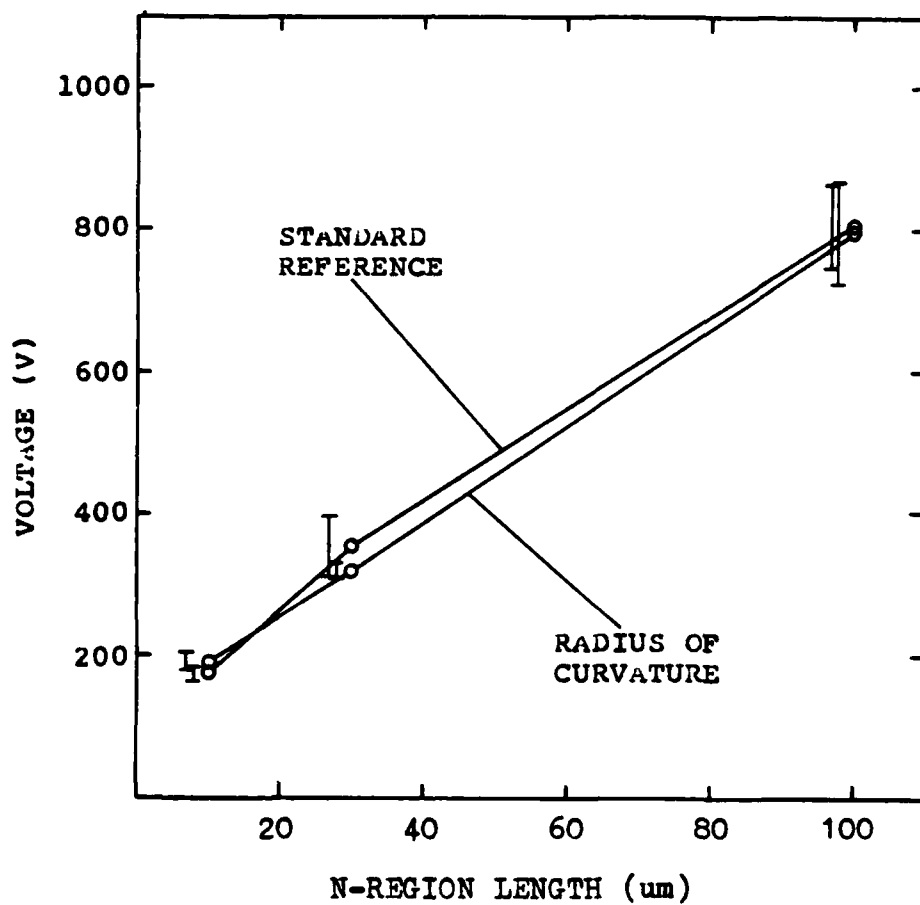


Fig. 71. Breakdown voltage versus n-region length for standard reference and radius of curvature diodes on Wafer 2-2. Error bars show one standard deviation above and below the mean.

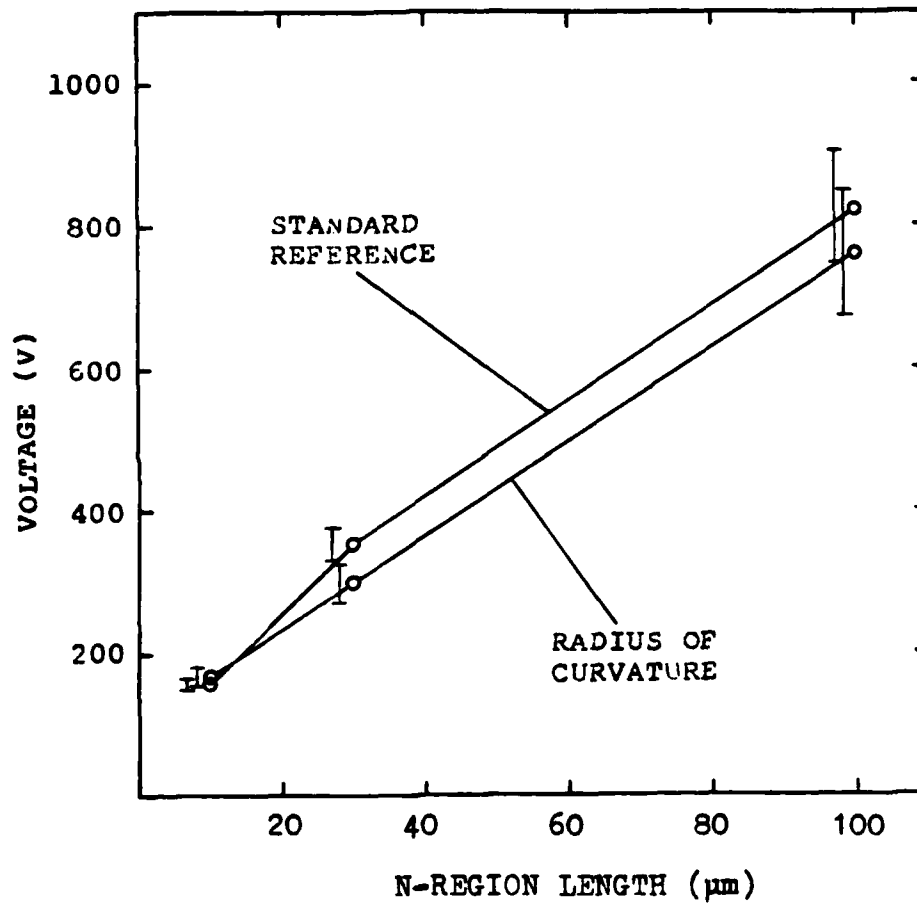


Fig. 72. Breakdown voltage versus n-region length for standard reference and radius of curvature diodes on Wafer 2-1. Error bars show one standard deviation above and below the mean.

respectively. The electrical characteristic of these wafers are similar, as in previous tests, so they are discussed together.

There is no significant difference between the voltage failure thresholds of standard reference and radius of curvature diodes for any of the three n-region lengths shown in Figs. 70-72. Thus, the radius of curvature geometry does not have a major effect in reducing the voltage failure thresholds of diodes with the three lower nominal doping densities.

Filament locations were determined during each of the voltage threshold tests shown in Figs. 68-72. Over one hundred radius of curvature diodes were tested, representing three different n-region lengths, and three different radii of curvature of the p^+n junctions. The filament locations were so consistent that there was no need to plot them in filament location diagrams. Filaments were located along the line separating the p^+n and n^+n junctions by the minimum distance; that is, along the line connecting the centers of curvature of the p^+n and n^+n junctions. The only exceptions to this rule were several diodes which failed by damage to the aluminum metallization. No filaments went along the edges of the diodes for any doping level in the radius of curvature structures. Thus, the radius of curvature geometry is very effective in localizing the current distribution at the second breakdown transition, for all five nominal doping densities.

H. Interdigitated Diodes

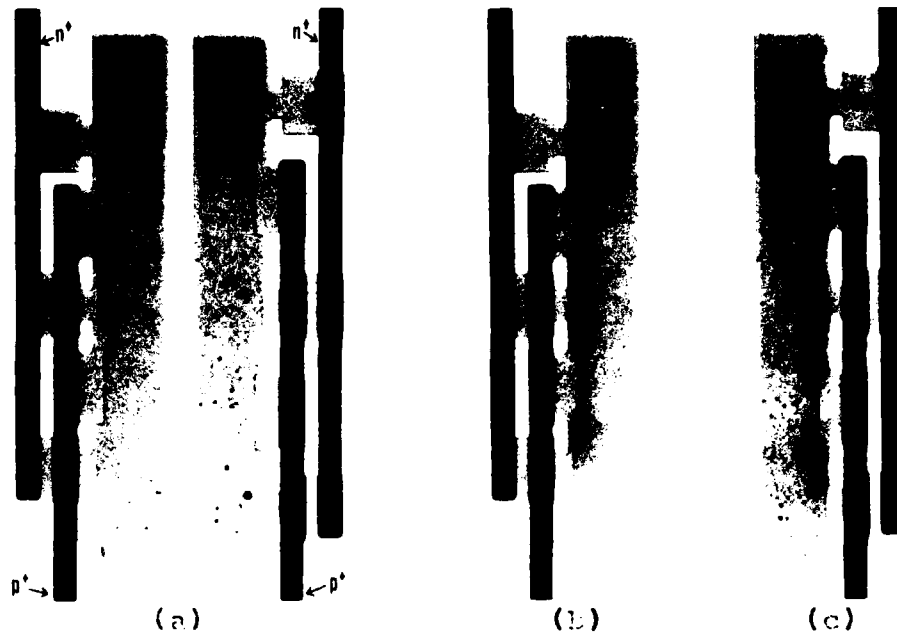
This section describes the heating patterns observed in diodes with an interdigitated geometry on Wafer 2-5. These diodes were de-

signed to simulate the cross section of three-dimensional interdigitated junction devices, which allow increased device current while maintaining relatively low current densities. A non-symmetric geometry implies non-uniform current densities even at low stress levels and also a greater tendency to form filaments at high stress levels.

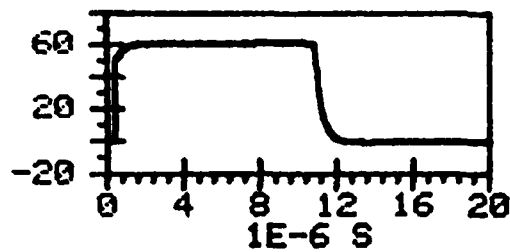
Waveforms and heating patterns of two interdigitated diodes under reverse bias are shown in Fig. 73. The zero bias photograph of both diodes is shown in Fig. 73a, while Fig. 73b and Fig. 73c show the heating pattern photographs at the end of the 10 μ s constant current pulses. The waveforms corresponding to Fig. 73b are shown in Test #1, and those corresponding to Fig. 73c are shown in Test #2.

In the interdigitated diode on the left side of Fig. 73a, the black bar on the left side of the diode is the metallization contact to the three n^+ regions, while the second bar is the metallization contact to the two p^+ regions. The large vertical rectangular region to the right of the metallizations is the n -region of the diode, having a width of 60 μ m and a length of 430 μ m. The n^+ regions extend a horizontal distance of 5 μ m into the n -region, while the p^+ regions extend a distance of 10 μ m. Each of the three n^+ regions has a vertical length inside the n -region of 30 μ m. The two p^+ regions have vertical lengths of 60 μ m inside the n -region. The two diodes in Fig. 73a are separated by a horizontal distance of 20 μ m.

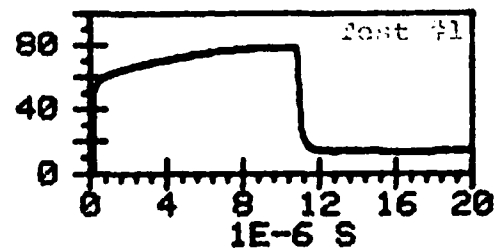
The basic difference between the two interdigitated diodes is the spacing separating the p^+ and n^+ regions. This distance is analogous to the n -region length in other types of diodes. The vertical distance separating the p^+ and n^+ regions of the diode on the left side of Fig.



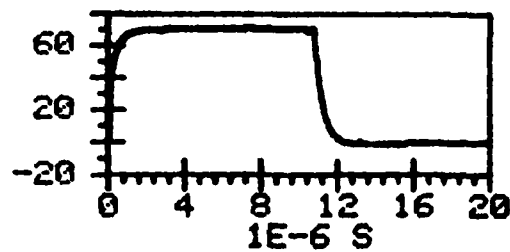
1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME



1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME

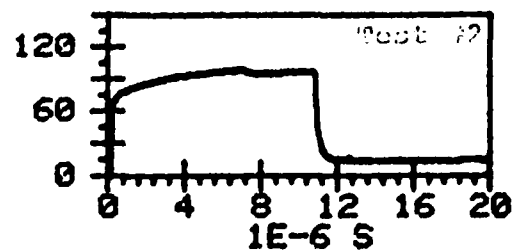


Fig. 73. Reverse bias tests of two interdigitated diodes on Wafer 2-5. (a) Zero bias photograph of both diodes. (b) Heating pattern of the diode in test #1. (c) Heating pattern of the diode in test #2.

73a is 20 μm , while it is 40 μm for the diode on the right. The n-region of the diode on the right side of Fig. 73a has a speckled appearance, which was apparently due to processing and observed in a number of interdigitated diodes on Wafer 2-5. However, it had no apparent effect on device performance.

The waveforms and heating configurations of Fig. 73 were obtained very close to the damage threshold. Heating occurs along the entire length of the p^+n junctions in both Fig. 73b and 73c. Hot spots are present at all four p^+n junction corners and at the corners of the middle n^+n junction in Fig. 73b and 73c. In addition, hot spots appear at the inside corners of the top and bottom n^+n junctions in Fig. 73c. Thus, the highest current densities occur at the corners of the p^+n and n^+n junctions, where field concentration and minimal n-region length occur. Melt filaments connect the corners of the p^+n and n^+n junctions at all five nominal doping densities. No edge effects were observed in interdigitated diodes.

Comparison of Test #1 and Test #2 shows that the voltage waveform corresponding to the heating pattern of Fig. 73c is slightly larger than that corresponding to Fig. 73b. This behavior is consistent with previous observations relating n-region length to voltage waveform amplitude. However, the increase is not as large as expected, based on the spacing between the p^+n and n^+n junctions of 20 and 40 μm . In previous tests, doubling the n-region length roughly doubled the amplitude of the voltage waveform near the second breakdown threshold, but the amplitude is increased only about 25% in Fig. 73. The current level in Test #2 is about 15% higher than that in Test #1, indicating that the

failure energy thresholds of the two diodes are not greatly different.

Failure thresholds and heating patterns of interdigitated diodes were not investigated at doping densities less than that of Wafer 2-5.

I. Special Tests

All of the tests described previously in this chapter were performed under reverse bias, and fell into one of the following four categories: heating patterns, energy thresholds, voltage thresholds, and damage morphology. This section describes the results of additional experiments: three-dimensional plots of diode waveforms correlated with heating pattern photographs, analysis of a waveform surface, photographs of microplasma emission, heating patterns of forward biased diodes, the heating pattern in a four-terminal structure, measurements of delay time, observation of a hot spot on a reverse biased diode's n^+n junction, and temperature measurements.

1. Waveform Surfaces

As discussed earlier in this chapter, current and voltage waveforms are not very useful in determining the onset of current filamentation. However, the waveforms can be used to compute diode impedance as a function of time, and this quantity is sometimes helpful in predicting the onset of filament formation and second breakdown.

In order to investigate waveform behavior in more detail and correlate waveforms to the temperature configurations, a group of diodes were tested over a wide range of pulse amplitudes using the low voltage, constant current test circuit and the Tektronix digital waveform instrument. The graphics capability of the Tektronix instrument was

used to display the waveform data in a three-dimensional format, with current, voltage, and time as the three axes. It was hoped that subtle changes in the waveform surface would provide indications of the onset of filamentation, approach of the failure threshold, and presence of known geometric irregularities (diffusion spikes, for example).

The voltage waveform surface of a reverse biased standard reference diode on Wafer 2-5 subjected to 10 μ s constant current pulses is shown in Fig. 74. This diode has an n-region length of 30 μ m and a width of 200 μ m. A zero bias photograph is shown in Fig. 74a, while Figs. 74b-e show several photographs taken during the test sequence. Lines extending from Figs. 74b-e show the points on the waveform surface at which the photographs were taken. Each of the photographs was taken at the end of a voltage waveform, with the same number of flashes of the arc lamp (approximately 500). Current levels corresponding to the photographs in Figs. 74b-e are listed in the figure caption.

In Fig. 74b (Current = 58 mA, Average Current Density = 7.3×10^8 A/m²) there is only a slight amount of darkening along the p⁺n junction and in the n-region. However, in Fig. 74c ($I = 72$ mA, $J_{avg} = 9.0 \times 10^8$ A/m²) the junction and n-region darkening have increased considerably, indicating substantially more heating. The photographs in Fig. 74d ($I = 79$ mA, $J_{avg} = 9.9 \times 10^8$ A/m²) and Fig. 74e ($I = 80$ mA, $J_{avg} = 10^9$ A/m²) were taken just below the threshold of damage. In Fig. 74d, the junction and n-region heating pattern shows no evidence of filamentation, but Fig. 74e contains four hot spots along the p⁺n junction which extend a short distance into the n-region. When the current level was increased one more step, one of the hot spots extended all

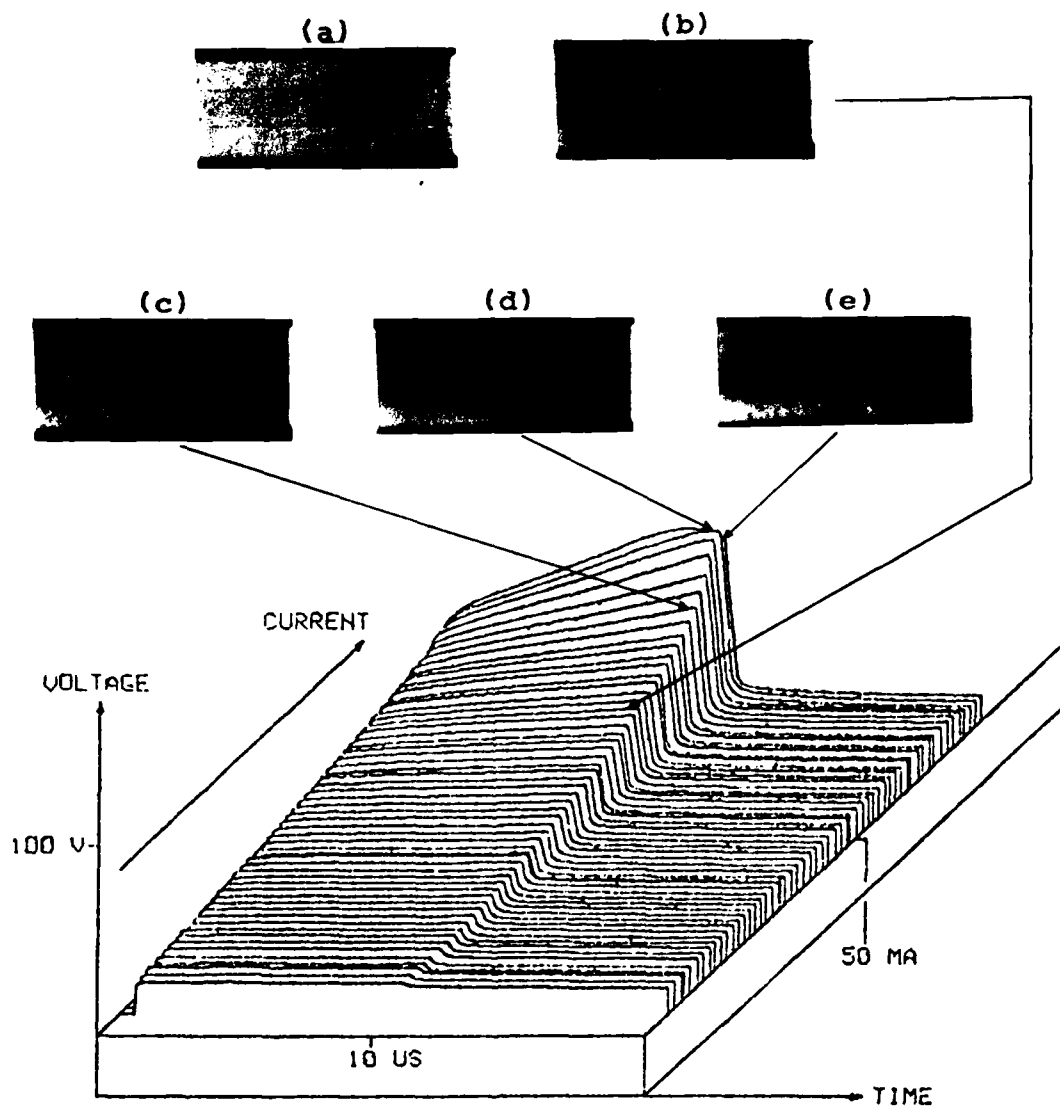


Fig. 74. Voltage-current-time surface of a reverse biased standard reference diode on Wafer 2-5. (a) Zero bias photograph before testing. (b) Current = 58 mA. (c) Current = 72 mA. (d) Current = 79 mA. (e) Current = 80 mA.

the way across the n-region and a melt filament formed, damaging the diode.

Comparison of the heating pattern of Fig. 74e to those in Fig. 28, from similar diodes under similar test conditions, shows that the hot spots in Fig. 74e are not very distinct compared to the ones of Fig. 28. If the current level had been increased very slightly from the level of Fig. 74e, a heating pattern similar to those of Fig. 28 would have been observed. Thus, the standard reference diodes are very close to the second breakdown transition when hot spots form along the p^+n junction.

The waveform surface in Fig. 74 is constructed so that the voltage and time axes are in the plane of the page, while current increases at an oblique angle, into the page. The time axis length is chosen to show the zero level, voltage pulse, and an additional 10 μs after the end of the pulse. The voltage does not decay to zero immediately after the applied pulse ends. Instead, it decays to the reverse bias breakdown voltage in a fraction of a microsecond, followed by a much slower exponential decay with a time constant of about 100 μs . This time constant is associated with the stray capacitance in the circuit and the high impedance of the diode when reverse biased below its avalanche breakdown voltage.

Since the waveform surface shown in Fig. 74 was obtained by plotting the diode voltage waveforms over a wide range of narrowly spaced current intervals, it accurately characterizes the diode under reverse bias and 10 μs constant current pulses. Therefore, if there are general trends in the voltage waveforms which indicate the onset of second

breakdown, these trends should be discernable from the waveform surface.

It is evident that the slopes of the voltage versus time curves increase as the diode current level increases, and that the rate of increase is faster than linear. The slope corresponds to increases with temperature of n-region resistivity and of junction voltage. At the end of the last waveform there is a slight drop in voltage, which is, as discussed previously, a good indication that the diode is on the verge of second breakdown. Unfortunately, there are no obvious changes in the waveform surface prior to the last waveform that would indicate second breakdown is imminent. Thus, waveform surfaces do not appear to be very useful in predicting the onset of second breakdown in reverse biased standard reference diodes. However, the information contained in this waveform surface may be analyzed in a somewhat more productive manner which will be described in Section V.I.2.

The waveform surface of a diode on Wafer 2-5 having a 5 μm diffusion spike on the p^+n junction is shown in Fig. 75. The n-region length, width, and doping level of this diode are similar to those of the standard reference diode in Fig. 74. A zero bias photograph, Fig. 75a, shows the diffusion spike 50 μm from the left side of the diode. In Fig. 75b ($I = 59 \text{ mA}$, $J_{\text{avg}} = 7.4 \times 10^8 \text{ A/m}^2$) the spike is outlined clearly due to heating of the p^+n junction. In Fig. 75c ($I = 70 \text{ mA}$, $J_{\text{avg}} = 8.8 \times 10^8 \text{ A/m}^2$) there is considerable heating of both the p^+n junction and the n-region, and there is a small hot spot above the diffusion spike. The hot spot above the diffusion spike becomes more prominent with further increase in current, as shown in Fig. 75d ($I =$

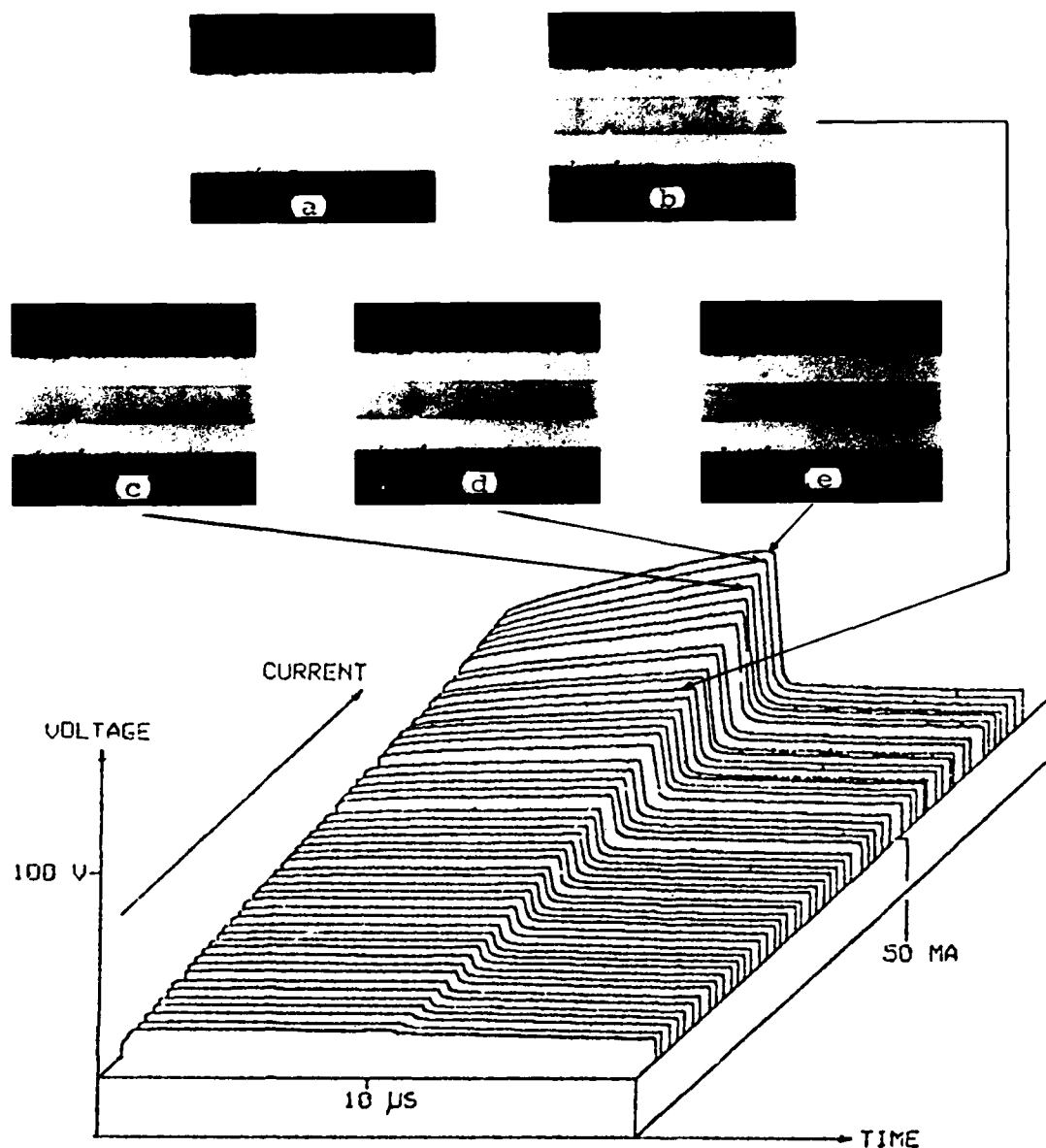


Fig. 75. Voltage-current-time surface of a reverse biased p-n diffusion spike diode on Wafer 2-5. (a) Zero bias photograph before testing. (b) Current = 59 mA. (c) Current = 70 mA. (d) Current = 73.2 mA. (e) Current = 74.5 mA.

73.2 mA, $J_{avg} = 9.15 \times 10^8 \text{ A/m}^2$) and Fig. 75e ($I = 74.5 \text{ mA}$, $J_{avg} = 9.31 \times 10^8 \text{ A/m}^2$). When the current was increased one more step above the level corresponding to Fig. 75e, the hot spot above the diffusion spike extended all the way across the n-region and a melt filament formed, damaging the diode. The current and voltage levels at the second breakdown threshold were slightly less than those of the standard reference diode, in agreement with earlier results concerning energy, current, and voltage failure thresholds.

The heating pattern photographs and the waveform surface indicate that the hot spot above the diffusion spike is present over a wider current interval than the hot spots observed in the standard reference diode of Fig. 74. In Fig. 74, no hot spots were visible until the last waveform ($I = 80 \text{ mA}$, $J_{avg} = 10^9 \text{ A/m}^2$). Thus the p^+n spike causes observable current localization at a current level 6% below the failure threshold, while the uniform junction diode has localization at a current level about 1% below the damage threshold. However, the damage thresholds of the two are the same within the statistical uncertainties of properties of different diodes.

The slopes of the voltage versus time curves in Fig. 75 increase in a very uniform manner as the diode current level increases. There is no indication from the waveform surface of the current level at which the hot spot starts to form, or that second breakdown is about to occur at the last waveform. Thus, the voltage waveform surfaces do not appear to be very useful in predicting the onset of hot spot formation, or second breakdown in p^+n spike diodes.

All of the experiments described previously were concerned with the effects of geometry and doping level on the second breakdown susceptibility of reverse biased diodes. However, experiments were also performed to determine the behavior of forward biased diodes under electrical stress, although not to the same extent as the reverse bias investigations. To illustrate these experiments, the voltage waveform surface and associated heating pattern photographs of a forward biased standard reference diode on Wafer 2-5 are shown in Fig. 76. The n-region length ($30\text{ }\mu\text{m}$) and width ($200\text{ }\mu\text{m}$) of this diode are the same as those of the reverse biased diode of Fig. 74. A zero bias photograph is shown in Fig. 76a, while heating pattern photographs are shown in Figs. 76b-d. The p^+n junction is the lower boundary of the n-region for each of the diode photographs.

The heating pattern of Fig. 76b ($I = 80\text{ mA}$, $J_{\text{avg}} = 10^9\text{ A/m}^2$) indicates that the n-region is almost uniformly heated, but in Fig. 76c ($I = 96\text{ mA}$, $J_{\text{avg}} = 1.2 \times 10^9\text{ A/m}^2$) and Fig. 76d ($I = 104\text{ mA}$, $J_{\text{avg}} = 1.3 \times 10^9\text{ A/m}^2$) the n-region heating is apparently nonuniform. A narrow strip adjacent to the p^+n junction is not significantly heated. This result has been observed in all of the diodes tested on Wafer 2-5 under forward bias for n-region lengths greater than $10\text{ }\mu\text{m}$ (approximately one hundred), regardless of diode geometry. The unheated region, typically 5 to $15\text{ }\mu\text{m}$ in length, tends to lengthen slightly near the diode edges. When the n^+-n-n^+ doping level test structures were electrically stressed, the n-regions along the nn^+ interfaces became heated, suggesting that the above effect is related to the presence of the p^+n junction. For the doping level concentration of Wafer 2-5, the

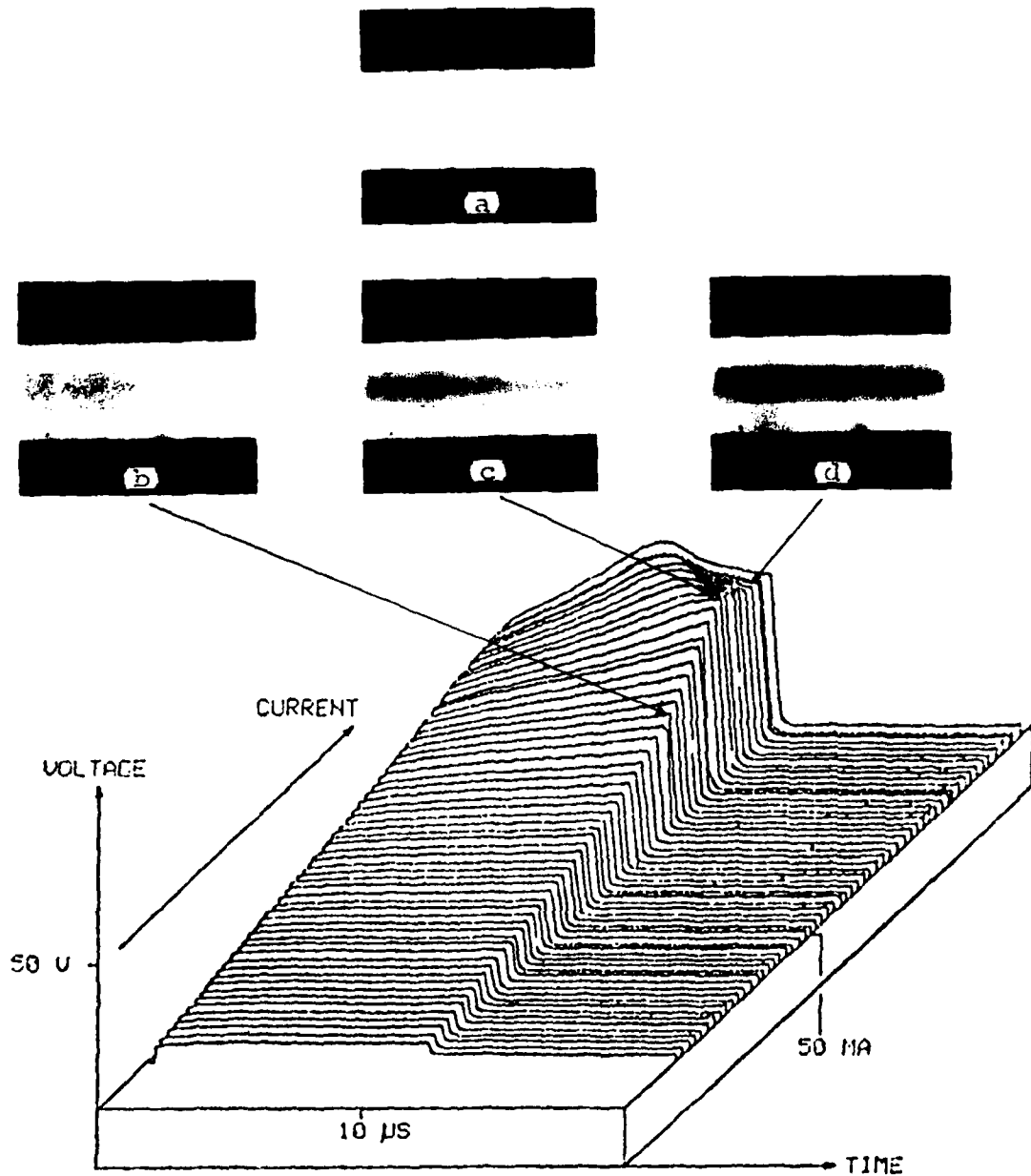


Fig. 76. Voltage-current-time surface of a forward biased standard reference diode on Wafer 2-5. (a) Zero bias photograph before testing. (b) Current = 80 mA. (c) Current = 96 mA. (d) Current = 104 mA.

depletion width is about $0.2\text{ }\mu\text{m}$, considerably less than the width of the cool strip.

Except for the narrow area adjacent to the p^+n junction, the n -region heating shown in Fig. 76d is generally uniform. Since the heating pattern photograph in Fig. 76d was taken at the end of the next to the last waveform, it is evident that the n -region current distribution remains uniform at current levels which are very close to the second breakdown threshold. The same observation also applies to diodes with different n -region lengths and widths, to diodes with contact and diffusion spikes, and to enclosed reference diodes. Diodes with other geometries were not extensively tested under forward bias.

However, if the current level is carefully increased till the diode is on the verge of second breakdown, then the n -region current distribution becomes nonuniform. Typically, one or more broad filaments, which extend most of the way across the n -region, are observed. Several examples of filamentation in forward biased diodes will be described in Section V.I.4.

When the current was increased one more step above the current level of the last waveform in Fig. 76, a melt filament formed, damaging the diode. Observations of heating patterns in other forward biased diodes show that the melt filament in a diode forms at the location of the most prominent nondestructive filament. Melt filaments formed during forward bias second breakdown are similar in appearance to those described previously in the reverse bias damage morphology experiments. Filament locations were not investigated statistically.

There are several distinctive differences in the forward and reverse bias voltage waveform surfaces shown in Figs. 76 and 74. The slopes of the voltage versus time waveforms increase as the current level increases in both Fig. 76 and 74. However, in Fig. 76 a peak appears in the voltage versus time waveforms at a current level corresponding to approximately that shown in Fig. 76c. As the current level increases, this peak becomes more distinct and occurs earlier in the pulse. The peak does not correspond to any apparent change in the n-region heating pattern because the n-region darkens in a uniform manner as the pulse progresses. The maximum amplitude of the voltage waveform is believed to occur when an appreciable portion of the diode's n-region has been heated to the peak of its resistivity versus temperature curve.

The turnover in the voltage waveforms indicates that the diode is approaching the destructive threshold. In Fig. 76, the turnover is first seen at a diode current of 96 mA ($J_{avg} = 1.20 \times 10^9 \text{ A/m}^2$), while a destructive filament forms at 107 mA ($J_{avg} = 1.34 \times 10^9 \text{ A/m}^2$). The initial turnover occurs at a current level about 10% less than the current level at damage. Thus, the voltage waveform is a good indicator that the diode is approaching the damage threshold.

2. Waveform Surface Analysis

The voltage waveform surfaces give a general understanding of diode behavior over a wide range of pulse amplitudes. However, these diagrams condense a large amount of data into a small area, and some of the information is obscured. In particular, waveform surfaces do not

clearly display the relationship between diode current and voltage. One method to exhibit the diode's transient I-V characteristics is to plot cross sections of the waveform surfaces which are perpendicular to the time axis. This eliminates the time dependence, leaving only current and voltage as variables.

The I-V characteristics of a forward biased standard reference diode on Wafer 2-5 are shown in the first quadrant of the graph in Fig. 77. The n-region length and width of this diode are 30 and 200 μm , respectively. The third quadrant shows the I-V characteristics of a reverse biased standard reference diode with similar geometry and doping level. These data were obtained at the beginnings (B) and ends (E) of the voltage waveforms shown in Figs. 76 and 74. The area near the origin in Fig. 77 is the region in which ordinary curve tracer measurements would be made.

The difference between the I-V characteristics at the beginning and end of the waveforms indicates the effect of diode heating. At current levels near the second breakdown threshold, the impedance of the reverse biased diode increases over 50% from the beginning to the end of the waveform. The impedance of the forward biased diode also increases dramatically during the waveform at high current levels, although not as much as the reverse biased diode.

It is interesting to examine the impedance change during the pulse in more detail for the reverse bias case. Since the voltage versus time waveforms were obtained with constant current pulses, the diode impedance at a given time is directly proportional to the instantaneous amplitude of the voltage waveform. Thus, the quantity $V(t) - V(0)$ is

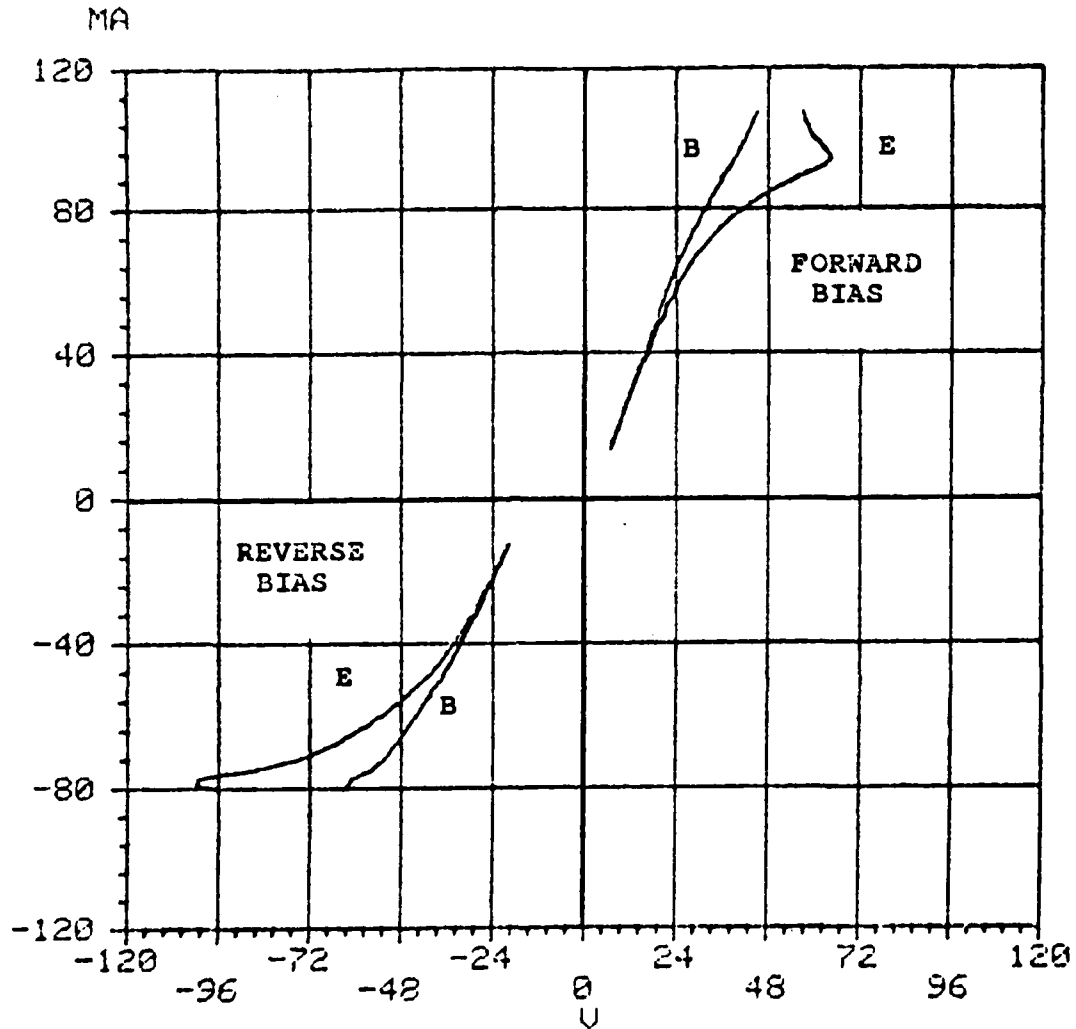


Fig. 77. I-V curves representing a standard reference diode with an n-region length of 30 μm and width of 200 μm on Wafer 2-5. Data were taken at the beginning (B) and end (E) of 10 μs constant current pulses. The area near the origin is where normal curve tracer measurements would be made.

proportional to the impedance change from the beginning of the pulse to some time, t , during the pulse.

The voltage difference between the end and the beginning of the waveforms in Fig. 74 is plotted on a logarithmic scale versus current in Fig. 78. The curve is linear over a wide current range, indicating that the impedance change during the waveform is related to the current level by the equation

$$\ln(\Delta Z) = kI \quad (5.1)$$

where

ΔZ = Impedance change during the waveform

k = Constant

I = Current

At very high current levels this relation departs from linearity; inspection of Fig. 78 shows that the curve is nonlinear in the last four waveforms, or approximately 4-5 mA below the second breakdown threshold. A similar plot for the p^+n spike diode in Fig. 75 also shows a slight departure from linearity prior to second breakdown, but it is smaller than that shown in Fig. 78. Thus, it is possible that the relation between diode impedance and current level may be used to predict the onset of second breakdown in highly doped diodes by indicating a departure from normal behavior. However, Eq. 5.1 does not apply to lower doping levels. Figure 79 shows the waveform shapes for a reverse biased standard reference diode on Wafer 2-4 (length 30 μm , width 200 μm). In Fig. 79a, there is a turnover in the voltage waveform shortly after the beginning of the pulse. This turnover becomes more distinctive in Figs. 79b-d. The current amplitude in Fig. 79a is 90% of that in Fig. 79d, indicating that the voltage turnover predicts the onset of

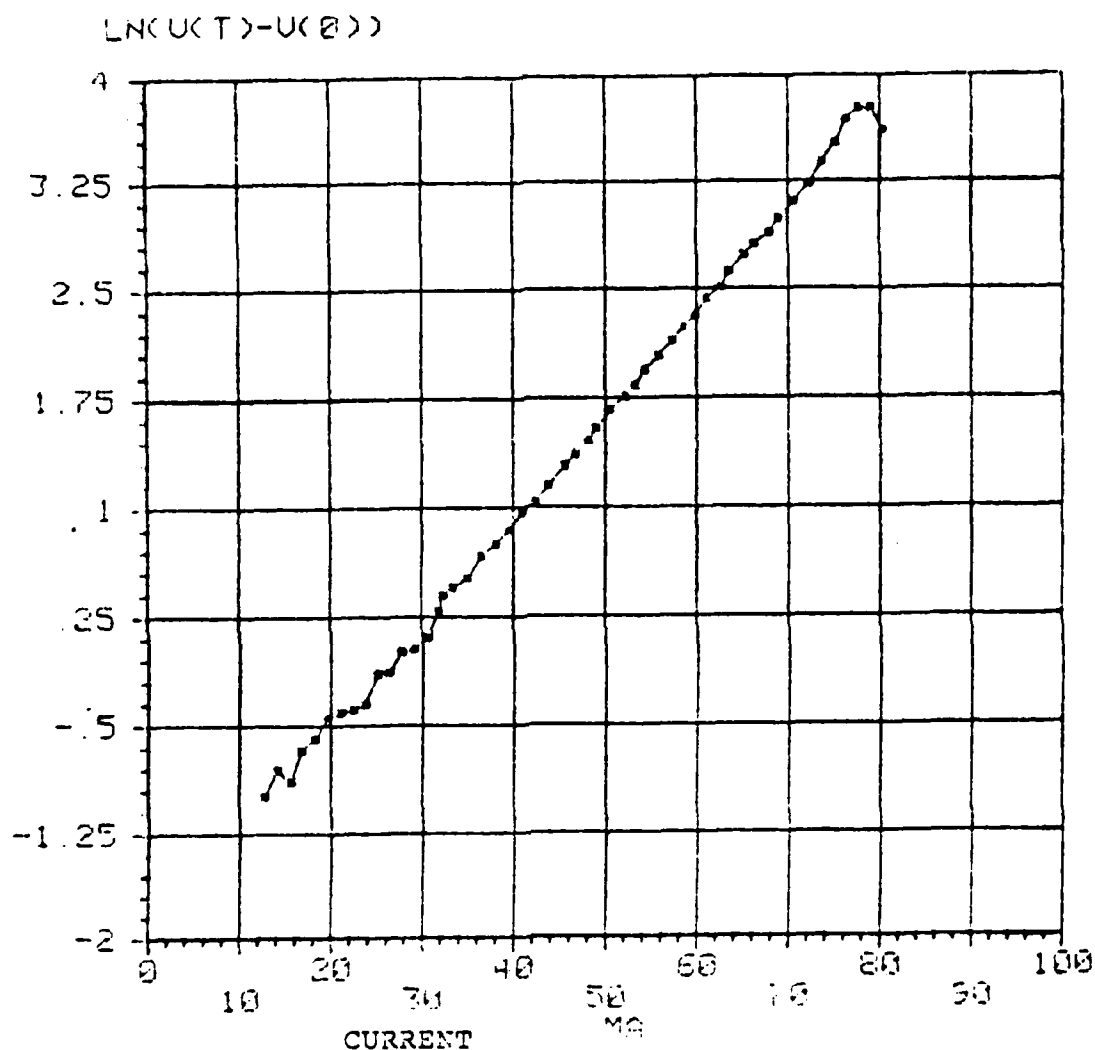


Fig. 78. Attempt to determine the onset of second breakdown for a standard reference diode on Wafer 2-5 (length = 30 μ m, width = 200 μ m). The voltage difference between the beginning and end of constant current pulses is plotted on a logarithmic scale versus current. The departure from linearity in the 75-80 mA current range indicates that second breakdown is imminent.

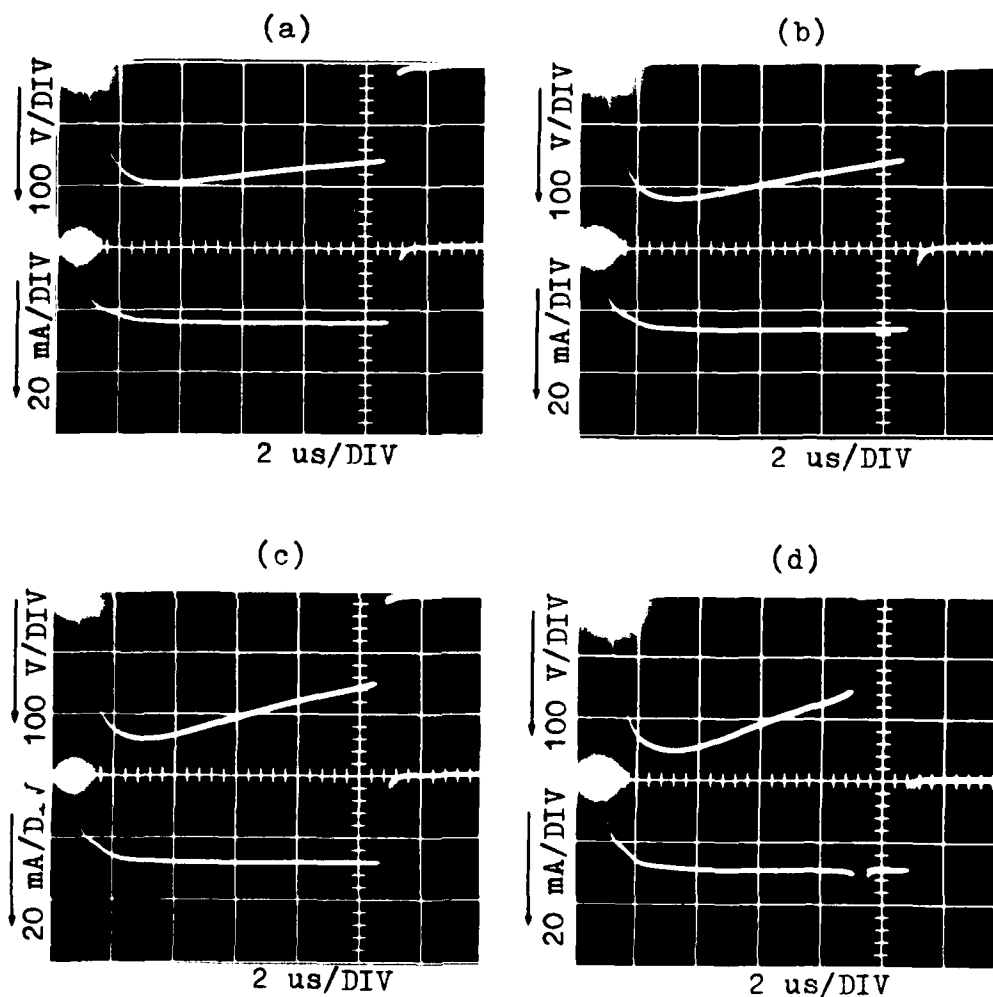


Fig. 79. Constant current pulses of increasing amplitude applied to a standard reference diode on Wafer 2-4. The n-region length and width of this diode are 30 and 200 μm , respectively. Second breakdown occurs in part (d). (a) Current = 24 mA; peak voltage = 200 V. (b) Current = 26 mA; peak voltage = 220 V. (c) Current = 28 mA; peak voltage = 240 V. (d) Current = 29 mA; peak voltage = 250 V.

second breakdown. Similar waveform shapes were observed in p^+n and n^+n spike diodes on Wafer 2-4. The turnover in the voltage waveform gives a better indication of the damage threshold than heating patterns on Wafer 2-4. On Wafer 2-1, the voltage waveform is rectangular at the second breakdown threshold under constant current testing.

3. Light Emission

Visible microplasma radiation is emitted along the p^+n junction during avalanche breakdown. This light emission was photographed under both steady reverse bias and pulse excitation. Photographs were made using a time exposure on the order of minutes under steady reverse bias, and by integrating the light emitted during a large number of waveforms during 10 μ s pulse excitation, typically several million pulses. No attempt was made to investigate the spectrum of the emitted light.

Several examples of light emission in diodes on Wafer 2-5 are shown in Fig. 80. The zero bias photograph of a p^+n spike diode with an n-region length of 100 μ m and width of 200 μ m is shown in Fig. 80a. The light emitted by this diode under a constant reverse bias of 15 V is shown in Fig. 80b; the current is 3 mA ($J_{avg} = 3.8 \times 10^7$ A/m²). The emission pattern has a beaded appearance, which follows the outline of the p^+n junction. The light emission becomes more uniform as the current level increases, as shown in Fig. 80c. The voltage and current amplitudes corresponding to Fig. 80c were 60 V and 20 mA ($J_{avg} = 2.5 \times 10^8$ A/m²). The exposure time for both Figs. 80b and 80c was two minutes using Polaroid Type 667 film (ASA 3000).

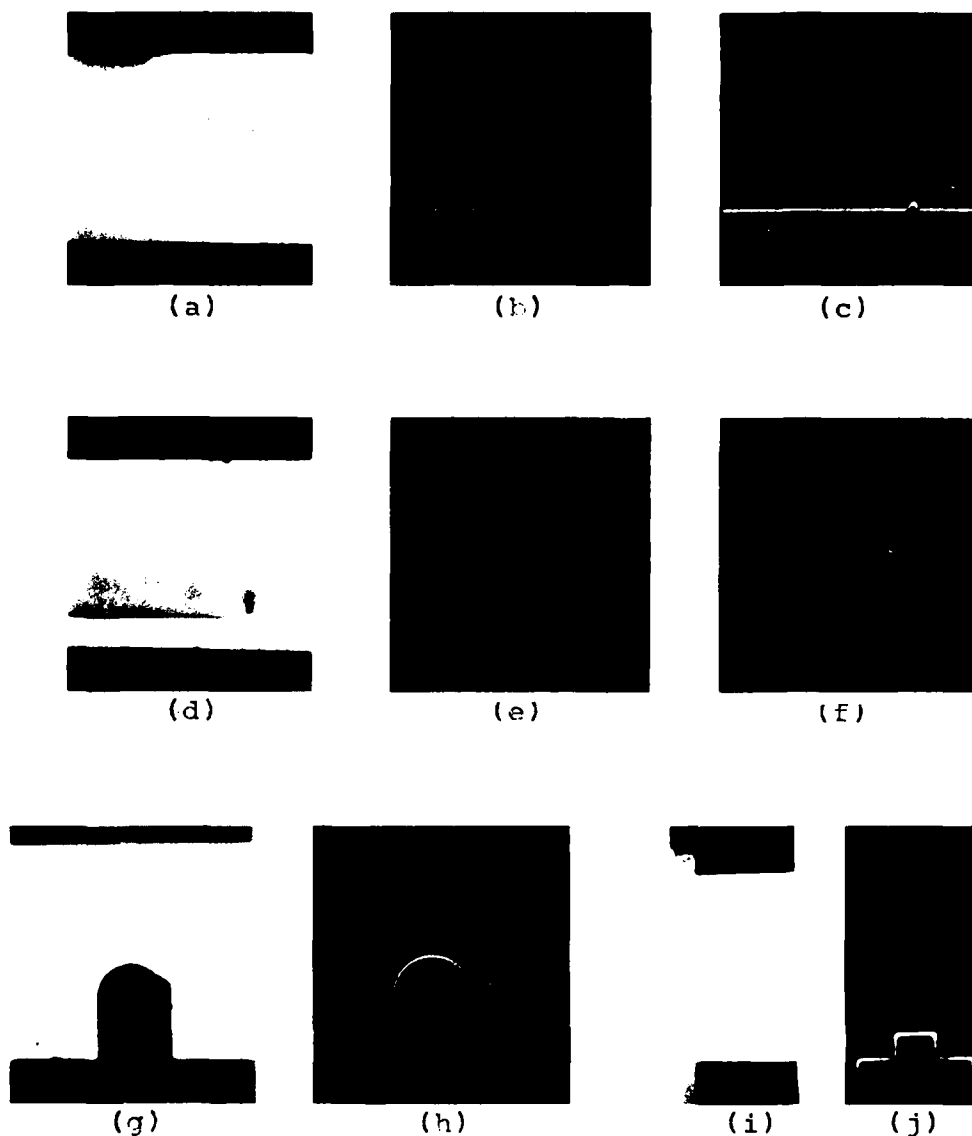


Fig. 80. Microplasma emission. (a) Zero bias photograph of a p^+n spike diode. (b) Emission of the diode in part (a) under 15 V steady reverse bias; current is 3 mA. (c) Emission of the diode in part (a) under 60 V steady reverse bias; current is 20 mA. (d) A p^+n spike diode near the second breakdown threshold. (e) Emission of the diode in part (d). (f) Emission of the diode in part (d) at a much lower pulse amplitude. (g)-(j) Zero bias and emission pattern photographs of a radius of curvature and an enclosed reference diode.

The heating pattern of a p^+n spike diode similar in geometry and doping level to the diode in Fig. 80a-c is shown in Fig. 80d. This photograph was taken with the strobe light at the end of each of a sequence of 10 μ s constant current pulses of amplitude close to the damage threshold. The current and voltage waveforms were similar to those of the corresponding diode in Fig. 30 ($J_{avg} = 1.0 \times 10^9$ A/m²). The light emission during the pulse is shown in Fig. 80e. Approximately four million pulses were applied to the diode to obtain the photograph in Fig. 80e. With a pulse repetition rate of slightly more than 10^3 Hz maintained for 60 min, the total exposure time was about 40 s. A second emission photograph, shown in Fig. 80f, was made at a much lower pulse amplitude using the same exposure. There was only uniform junction darkening in the heating pattern corresponding to Fig. 80f, with no evidence of a hot spot above the diffusion spike. Comparison of Figs. 80e and 80f shows that the emission pattern is more intense at the smaller pulse amplitude, possibly because the silicon is more transparent at a lower temperature and there is less internal absorption of the emitted light. Note that there is no evidence of light emission from the area above the diffusion spike in Fig. 80e. This indicates the hot spot temperature is less than 800 °C since the film is insensitive to infrared radiation.

The remaining two emission photographs in Fig. 80 were included to show that the light emission always follows the outline of the p^+n junction for diodes on Wafer 2-5. The zero bias and emission photographs of a radius of curvature diode are shown in Figs. 80g and 80h, respectively. This diode has an n-region width of 200 μ m and a minimum

separation between the p^+n and n^+n junctions of $10\text{ }\mu\text{m}$. The voltage and current levels corresponding to Fig. 80h are 25 V and 16 mA ($J_{\text{avg}} = 2.0 \times 10^8\text{ A/m}^2$). Light emission is most intense where the junctions are separated by a minimum distance. Comparison of the emission pattern of Fig. 80h with those of Figs. 80b and 80c suggests the current density along the junction in Fig. 80h ranges from about 4×10^7 to $3 \times 10^8\text{ A/m}^2$. The zero bias and emission pattern photographs of an enclosed reference diode are shown in Figs. 80i and 80j, respectively. This diode has an n-region width of $110\text{ }\mu\text{m}$ and a minimum separation between the p^+n and n^+n junctions of $100\text{ }\mu\text{m}$. The voltage and current levels corresponding to Fig. 80j are 60 V and 12 mA ($J_{\text{avg}} = 2.7 \times 10^8\text{ A/m}^2$, based on diode width). The diodes in Figs. 80c, 80h, and 80j are all close to the threshold of second breakdown under steady reverse bias.

The emission patterns of diodes on Wafer 2-4 are similar to those of diodes on Wafer 2-5 but the light intensity is decreased, making it necessary to use longer exposure times to obtain emission pattern photographs comparable to those shown in Fig. 80. For example, an emission pattern photograph similar to that of Fig. 80e requires an exposure of tens of millions of $10\text{ }\mu\text{s}$ pulses at a current density of about $3 \times 10^8\text{ A/m}^2$. Practically, this corresponds to a pulse repetition rate of 10^3 Hz maintained for approximately 10 to 20 hr (36-72 million pulses), giving a total exposure time of 6 to 12 min. At a pulse repetition rate of 10^3 Hz , the light emission can only be seen in a darkened room with a dark adapted eye, and it can not be detected by all observers. Higher pulse repetition rates were not used because the

pulse generator triggered an automatic cutoff when its duty cycle was exceeded.

The emission patterns of diodes on Wafers 2-1, 2-2, and 1-3 are similar, so these wafers are discussed as a group. Under dc reverse bias, the emission patterns are fainter than any of those observed in diodes on Wafers 2-5 and 2-4, and the patterns are never uniform prior to second breakdown. Instead, they have a beaded appearance similar to that of Fig. 80b. In some diodes, there is a large number of emission spots, as in Fig. 80b. However, in other diodes, there may only be two or three emission spots prior to second breakdown. There are often one or two spots at the diode edges, with several nonuniformly spaced spots along the length of the p^+n junction. The corresponding current density is, roughly, $1 \times 10^7 \text{ A/m}^2$. The spots at the diode edges are usually brighter than those along the p^+n junction, and are frequently accompanied by corresponding spots at the edges of the n^+n junction. In p^+n spike diodes there is usually an emission spot at the tip of the spike. After second breakdown occurs under steady reverse bias the n -region is so extensively damaged that the location of the initial damaging filament is unknown. Thus, the experiments on lightly doped diodes give no information relating filament sites to microplasma emission sites. No attempt was made to correlate early microplasma emission sites with filament sites on Wafers 2-4 and 2-5. Diodes on Wafers 2-1, 2-2, and 1-3 were also observed under electrical stress, using 10 μs constant voltage pulses at a repetition rate of $1-3 \times 10^3 \text{ Hz}$ but no light emission could be detected visually. Current was not measured

during these tests but is believed to be similar to the current levels described in Section V.F.1.

4. Heating Patterns Under Forward Bias

The heating patterns observed in a forward biased standard reference diode have been described previously in connection with Fig. 76, but those patterns showed no evidence of current segregation into hot spots or filaments, even at current levels close to the damage threshold. There are two problems which limit the ability to observe filamentation prior to damage under forward bias. One difficulty arises because there is often little contrast between the current filaments and the adjacent n-region near the damage threshold. An additional complication occurs because the current level must usually be closer to the damage threshold than for the reverse bias case, making it difficult to complete a test without destroying the diode. For these reasons, heating patterns were only observed in approximately one hundred forward biased standard reference, enclosed reference, and diffusion spike diodes on Wafer 2-5.

An exception to the difficulties mentioned above occurs for diodes on Wafer 2-5 having n-region lengths of 10 and 30 μm , and widths of 30 or 50 μm . In this group, filaments were observable over a relatively wide current interval below the damage threshold. The current density at the failure threshold is similar to that of diodes with wider n-regions. Broad filaments were seen to extend all the way across the n-region without melt formation, while post-test I-V characteristics and visual examination revealed no damage. Damage did occur through

the familiar melt filaments at just slightly higher excitation levels. Similar behavior (discussed in Section V.F.1) was observed for the same group of diodes under reverse bias. Three tests at increasing levels of forward bias were performed on a standard reference diode of Wafer 2-5 having n-region length and width both equal to 30 μm . A zero bias photograph is shown in Fig. 81a, and heating patterns at the ends of Tests #1-3 are shown in Figs. 81b, 81c, and 81e, respectively. The heating pattern in Fig. 81d was taken near the beginning of Test #3, at a time marked by arrows on the waveforms. The p^+n junction is the lower boundary of the n-region in each photograph. These tests were performed with the constant current circuit shown in Fig. 4.

The heating pattern at the end of Test #1 is uniform except for the narrow area adjacent to the p^+n junction. The current in Test #1 is about 20 mA, and the peak voltage is roughly 90 V. This corresponds to a current density of approximately $1.7 \times 10^9 \text{ A/m}^2$. However, at the end of Test #2, there is a broad filament near the center of the diode which extends all the way across the n-region. The current in Test #2 is about 25 mA ($J_{\text{avg}} = 2.1 \times 10^9 \text{ A/m}^2$), the peak voltage is 95 V, and the peak in the voltage waveform occurs 5 μs after the beginning of the pulse. Observations of the heating pattern at various times during Test #2 showed that the filament began to form several microseconds before the end of the pulse. There is also a single broad filament at the end of Test #3, taken at a current level of roughly 30 mA ($J_{\text{avg}} = 2.5 \times 10^9 \text{ A/m}^2$) and a peak voltage of about 115 V, but this filament is slightly to the left of that in Fig. 81c. The peak in the voltage waveform occurs 3 μs from the beginning of the pulse. Observations of

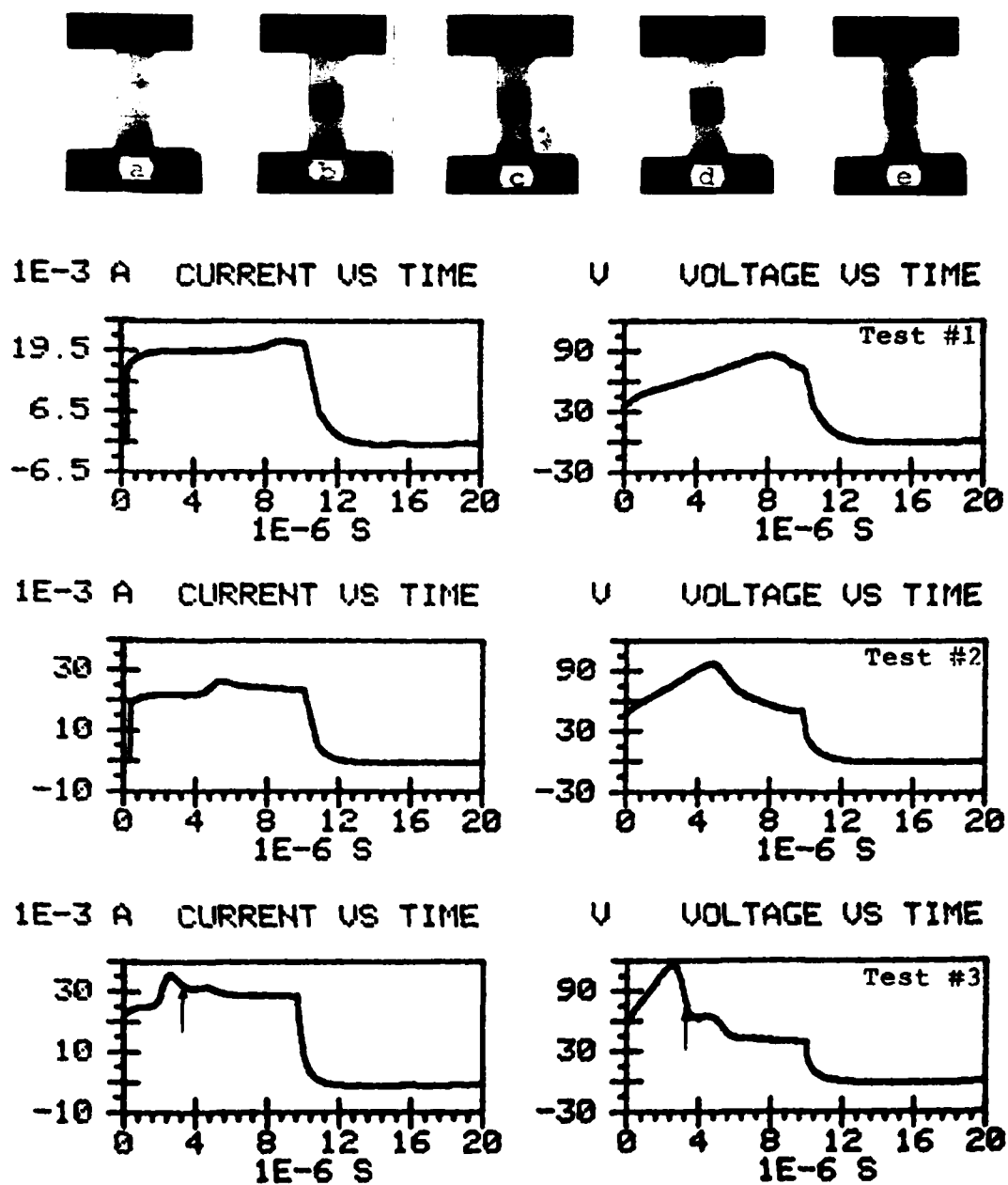


Fig. 81. Forward bias tests at increasing levels of excitation on a standard reference diode of Wafer 2-5. (a) Zero bias photograph. (b) Heating pattern at the end of Test #1. (c) Heating pattern at the end of Test #2. (d) Heating pattern near the beginning of Test #3 (marked by arrow). (e) Heating pattern at the end of Test #3.

the heating pattern near the beginning of Test #3 revealed that there were initially two filaments present, and that the one on the left became dominant as the pulse progressed. After Test #3 was completed, the current level was reduced and Tests #1-3 were repeated, giving exactly the same results as described above. Although the results in Fig. 81 seem to indicate that the number of filaments is a function of current level, attempts to observe more than two filaments by reducing the pulse length and increasing the current amplitude were not successful. Because of risetime limitations, pulse lengths shorter than 1 μ s were not used. Similar results were observed for standard reference diodes with an n-region length of 30 μ m and width of 50 μ m, but not for other geometries. For standard reference diodes with n-region widths of 100, 200, and 500 μ m, there may be from one to, say, ten filaments prior to the damage threshold, often spaced nonuniformly and of unequal sizes. Filament locations were not consistent in similar devices, so the effect of pulse duration was not investigated.

The heating patterns observed in a forward biased p⁺n spike diode on Wafer 2-5 with an n-region length of 30 μ m and width of 50 μ m are shown in the upper part of Fig. 82. The lower part of Fig. 82 shows the corresponding heating patterns in a forward biased n⁺n spike diode with similar geometry and doping level. The zero bias photographs are shown in Figs. 82a and 82f, and the heating patterns at 6, 8, 9, and 10 μ s from the beginning of the pulse are shown in Fig. 82b-e and Fig. 82g-j. The current and voltage waveforms, and a post-test I-V characteristic are shown for both diodes. No device damage occurred during

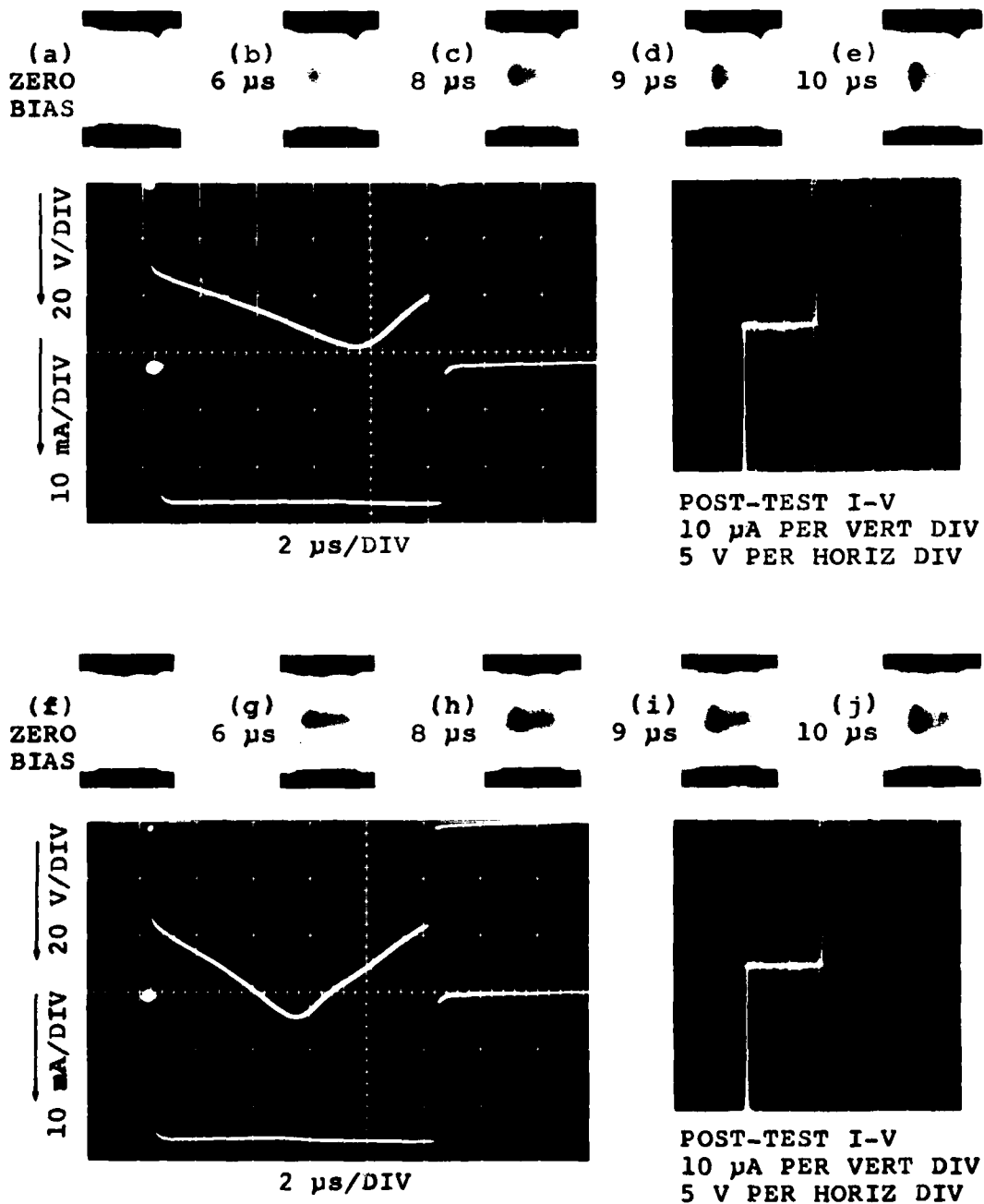


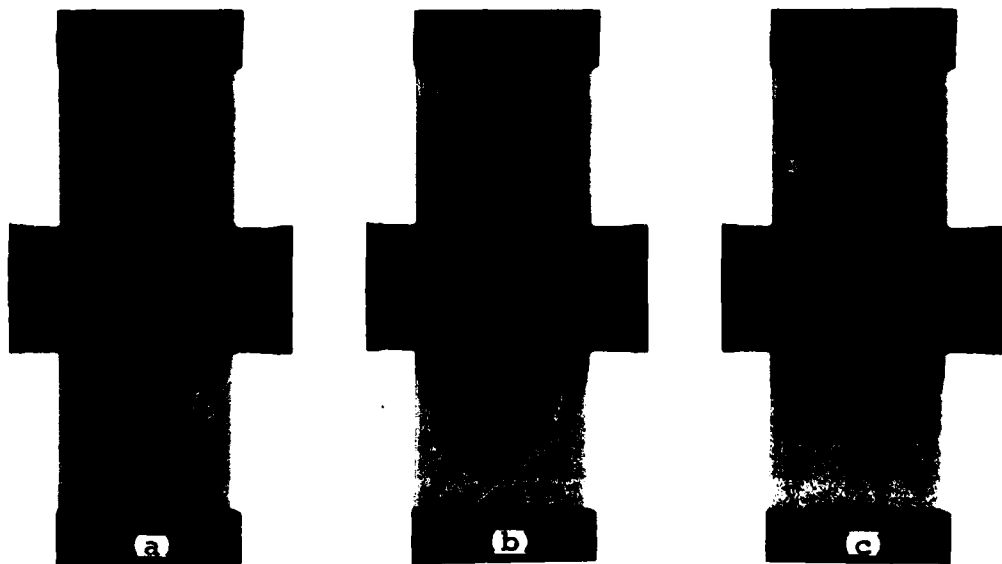
Fig. 82. Forward bias tests of a p^+n and an n^+n spike diode on Wafer 2-5. The upper part of the figure shows the test of a p^+n spike diode, and the lower part shows the test of an n^+n spike diode. (a) and (f) Zero bias photographs. (b)-(e) and (g)-(j) Heating patterns at 6, 8, 9, and 10 μ s from the beginning of the pulse.

these test sequences, as judged from the post-test I-V characteristic and microscopic appearance of the diode.

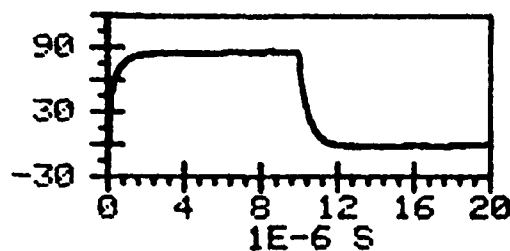
The heating patterns and waveform amplitudes are similar for both diffusion spike diodes. The photographs taken 6 μ s from the beginning of the pulse indicate an approximately uniform heating pattern, while those at 8, 9, and 10 μ s monitor the growth of the filament. The heating patterns at the end of the pulse, Figs. 82e and 82j, show well-defined filaments which extend from the diffusion spike to the opposite junction, at an angle which is not quite perpendicular to the diode width. The waveforms for the p⁺n spike diode indicate a current level of 12 mA ($J_{avg} = 6.0 \times 10^8$ A/m²) and a peak voltage of 56 V, which occurs approximately 8 μ s after the beginning of the pulse. The waveform amplitudes of the n⁺n spike diode are comparable, but slightly higher. The current is 13 mA ($J_{avg} = 6.5 \times 10^8$ A/m²) and the peak voltage is 66 V, which occurs about 5 μ s after the beginning of the pulse. The two examples in Fig. 82 illustrate several general properties of diffusion spike diodes under forward bias. In both p⁺n and n⁺n spike diodes, the filaments are similar in appearance and they occur at the spike, with comparable current and voltage amplitudes.

5. Four-Terminal Structure

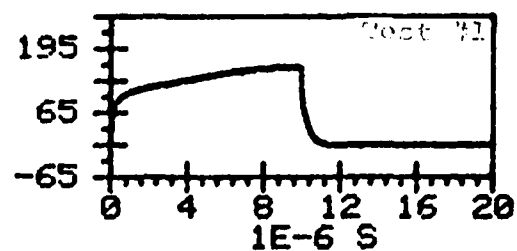
Although the four-terminal structure was not investigated in detail, heating patterns were observed in several of these devices. Figure 83 shows two tests of a four-terminal device on Wafer 2-5 using only the two extra contacts on the n-region as device electrodes, with the p⁺n and n⁺n junctions open-circuited. The zero bias photograph is



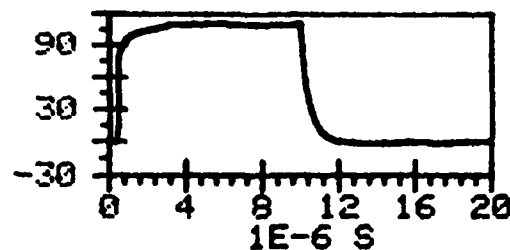
1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME



1E-3 A CURRENT VS TIME



V VOLTAGE VS TIME

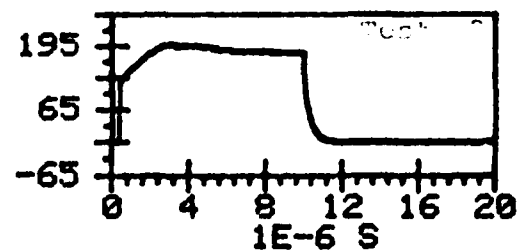


Fig. 83. Test of a four terminal diode with the p^+n and n^+n junctions open-circuited. (a) Zero bias photograph. (b) Heating pattern at the end of Test #1. (c) Heating pattern at the end of Test #2.

shown in Fig. 83a, and the heating patterns at the ends of Test #1 and Test #2 are shown in Figs. 83b and 83c, respectively. The diode is oriented so that the p^+n and n^+n junctions are horizontal, with the p^+n junction at the top electrode and the n^+n junction at the bottom electrode. The two extra electrodes are biased so that the one on the right is positive with respect to the one on the left. The horizontal spacing between the two extra electrodes is $80\text{ }\mu\text{m}$ and the vertical spacing between the p^+n and n^+n junctions is $240\text{ }\mu\text{m}$.

The heating pattern in Fig. 83b was obtained at a current level of 85 mA and a peak voltage of about 160 V. It shows that the electrode corners act as concentration centers for the current. The heating pattern in Fig. 83b, taken at a current level of 110 mA and a peak voltage of about 200 V, shows the heating pattern close to the damage threshold. Here, the hot spots extend further into the n-region and away from the electrodes, at an angle of approximately 45° to the line connecting the electrode corners. Both of the hot spots on the right hand electrode are longer than those on the left hand electrode. Exactly the same heating pattern and waveform shapes were observed when the polarity was reversed, suggesting both that the n-region resistivity is nonuniform, and that the resistances at the metal-semiconductor interfaces are not polarity sensitive.

Although this four-terminal device has some similarity to the enclosed reference geometry, there is a significant difference in the heating patterns. In enclosed reference diodes, hot spots only occur at the corners of the p^+n junction and they do not grow along a line which points away from the n^+n junction. In the four-terminal device,

the highly conductive n^+ and p^+ areas at the top and bottom serve, closely, as equipotential regions which cause the electric field to bulge outward toward these regions. Thus, in similar tests on other four-terminal devices with shorter spacings between the p^+n and n^+n junctions, melt filaments were often observed to extend from the corners of the two extra electrodes directly to one of the diode junctions, both filaments always terminating on the same junction. For a four-terminal structure with a p^+n and n^+n junction spacing of $25\text{ }\mu\text{m}$ and an electrode spacing of $80\text{ }\mu\text{m}$, these filaments are almost perpendicular to the line connecting the electrode corners.

6. Delay Time

Most of the previously described results were obtained by electrically stressing diodes to the threshold of second breakdown with $10\text{ }\mu\text{s}$ pulses. Thus, the length of the maximum amplitude non-destructive pulse, or delay time, was maintained constant. The stroboscopic method allows the non-destructive determination of thresholds of second breakdown on a single device using different pulse lengths. Thus threshold energy, threshold voltage, and other electrical characteristics can be related to delay time. The voltage and current waveforms of a series of constant current pulses applied to a standard reference and a p^+n spike diode on Wafer 2-5 are shown in Fig. 84. Each diode has an n -region length of $100\text{ }\mu\text{m}$ and a width of $200\text{ }\mu\text{m}$, and the spike length is $5\text{ }\mu\text{m}$. The pulse lengths varied from 10 to $100\text{ }\mu\text{s}$, in $10\text{ }\mu\text{s}$ steps, and were of just sufficient amplitude to bring the diode to the threshold of second breakdown, as determined from observations of hot spots.

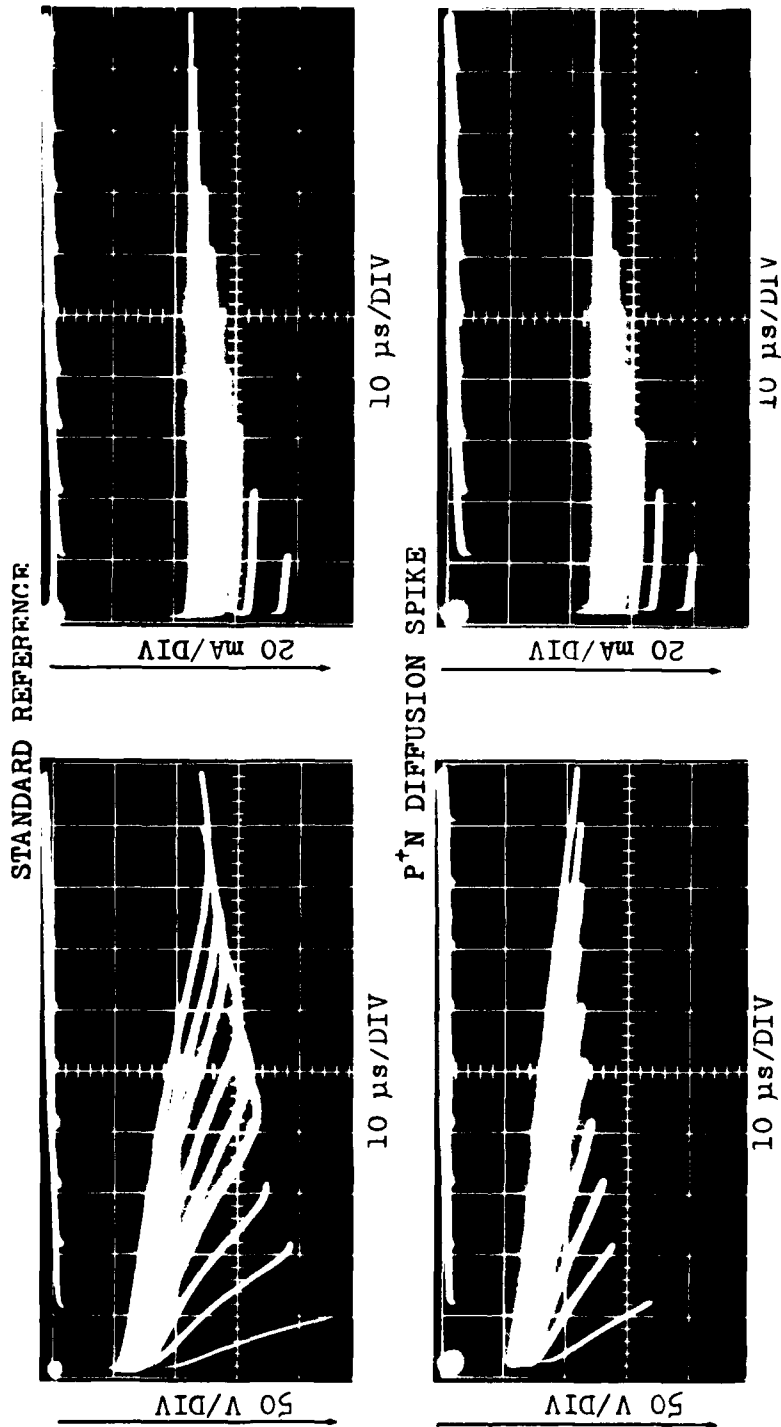


Fig. 84. Voltage and current waveforms of a standard reference and a $p^{+}n$ spike diode on Wafer 2-5. The pulses vary in length from 10 to 100 μ s, and are of just sufficient amplitude to bring the diodes to the threshold of second breakdown. The n-region length and width of both diodes are 100 and 200 μ m, respectively.

There is a definite turnover voltage in most of the standard reference diode voltage waveforms, while those of the p^+n spike diode maintain an approximately constant slope throughout the pulse. In addition, the voltage waveforms of the standard reference diode tend to have a somewhat higher amplitude for corresponding pulse lengths than those of the p^+n spike diode. The amplitudes of corresponding current waveforms are similar for all pulse lengths.

The waveforms in Fig. 84 may be used to calculate the energy input and the current level as functions of delay time. A plot of energy input versus delay time is shown in Fig. 85, and a plot of current level versus delay time is shown in Fig. 86. The plot in Fig. 85 indicates that the energy necessary to bring the diodes to the threshold of second breakdown increases as the delay time increases, and that more energy is required, for corresponding delay times, for a standard reference than for a p^+n spike diode. At the shortest delay times (10 μs), the energy thresholds were the same. The plot in Fig. 86 indicates that the current level necessary to cause second breakdown decreases as delay time increases, with both diodes having the same threshold currents for a given delay time. For large enough delay times, the current level would asymptotically approach the dc breakdown current amplitude. Comparison of Figs. 85 and 86 indicates the voltage at the second breakdown threshold is typically about 25% greater for the standard reference diode than for the p^+n spike diode.

Diodes on Wafer 2-5 with straight p^+n and n^+n junctions, and with n -region lengths and widths of 30 and 200 μm , respectively, were tested to failure with reverse bias constant current pulses varying in dura-

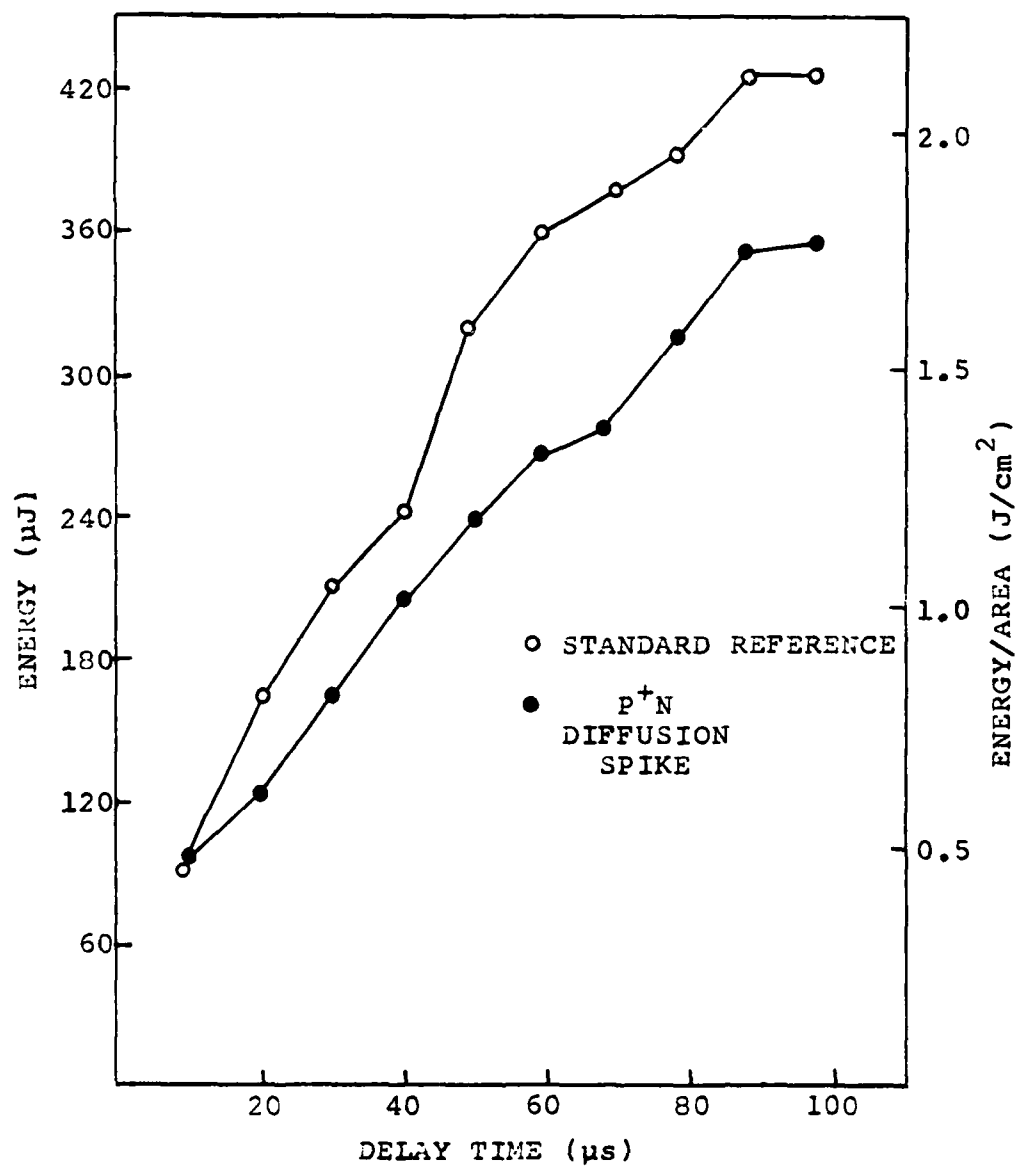


Fig. 85. Energy versus delay time for a standard reference and a p⁺n spike diode on Wafer 2-5. The n-region length and width of both diodes are 100 and 200 μm, respectively.

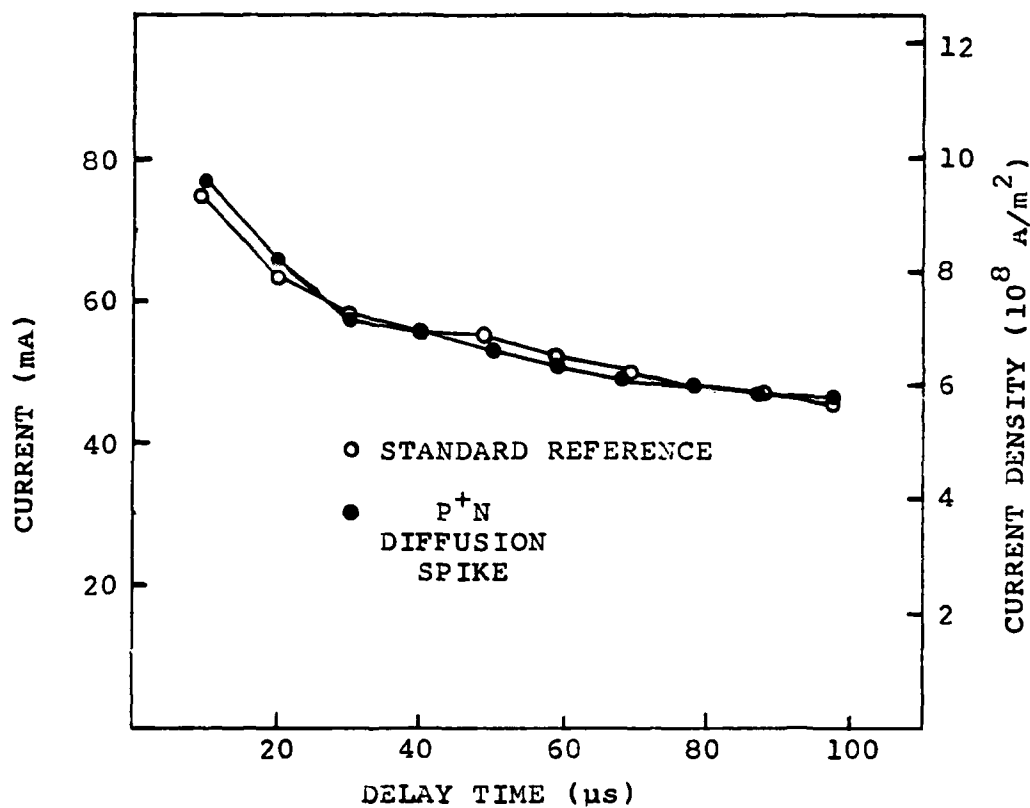


Fig. 86. Current versus delay time for a standard reference and a p⁺n spike diode on Wafer 2-5. The n-region length and width of both diodes are 100 and 200 μm , respectively.

tion from 0.1 to 100 μ s. These were contact spike diodes from the multiple spike structures of four adjacent die. However, as discussed previously, contact spikes do not affect diode performance. Energy, current, and power failure thresholds are shown in Figs. 87, 88, and 89, respectively. The plots in Figs. 87 and 89 are log-log, while that in Fig. 88 is semi-log. Since Figs. 87 and 89 are linear, energy and power are related to delay time by power laws. Least-squares fits to Figs. 87 and 89 show that energy is proportional to $t_p^{-.52}$ and that power is proportional to $t_p^{-.48}$. The correlation coefficient of both curves is 0.998. The power law dependence agrees closely with that in the Wunsch-Bell model of $t_p^{-1/2}$. A plot of the Wunsch-Bell model (Eq. 2.1, with T_m the melting point of silicon) is shown in Fig. 89. The thresholds for experimental data lie about an order of magnitude above the Wunsch-Bell curve, probably as a result of effective power dissipated to the n -region, associated with the efficient heat-sinking to the substrate. The data in Fig. 88 indicate that the current failure thresholds decrease as delay time increases.

7. Hot Spot On The n^+n Junction

Excluding radius of curvature and interdigitated diodes, a nonuniform current distribution on the n^+n junction was observed only once in over 300 diodes tested on Wafer 2-5. The exception occurred for a standard reference diode with an n -region length of 100 μ m and a width of 200 μ m. A test of this diode is shown in Fig. 90. The zero bias photograph is shown in Fig. 90a and heating patterns at 2, 4, 6, 8, 9, and 10 μ s after the leading edge of the 10 μ s pulse are shown in Figs.

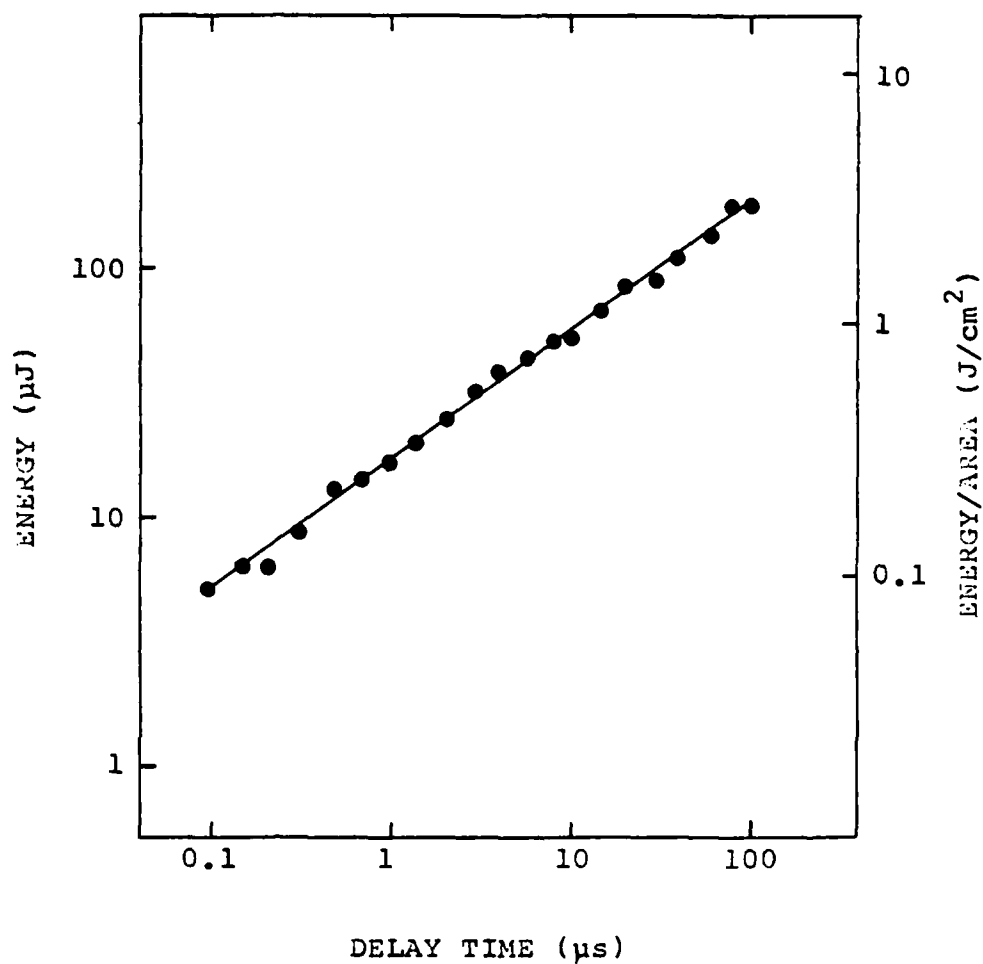


Fig. 87. Energy versus delay time for diodes on Wafer 2-5 with straight p-n and n-n junctions, an n-region length of 30 μm , and a width of 200 μm .

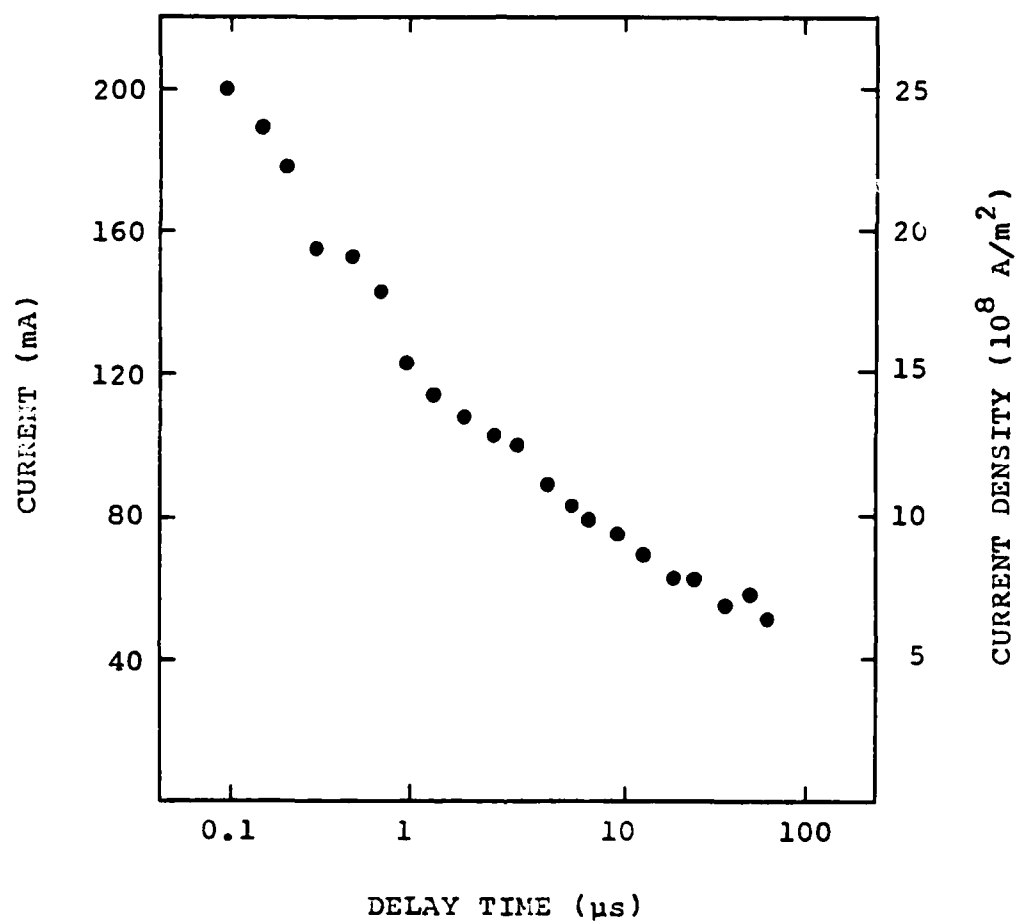


Fig. 88. Current versus delay time for diodes on Wafer 2-5 with straight p-n and n-n junctions, an n-region length of $30 \mu\text{m}$, and a width of $200 \mu\text{m}$.

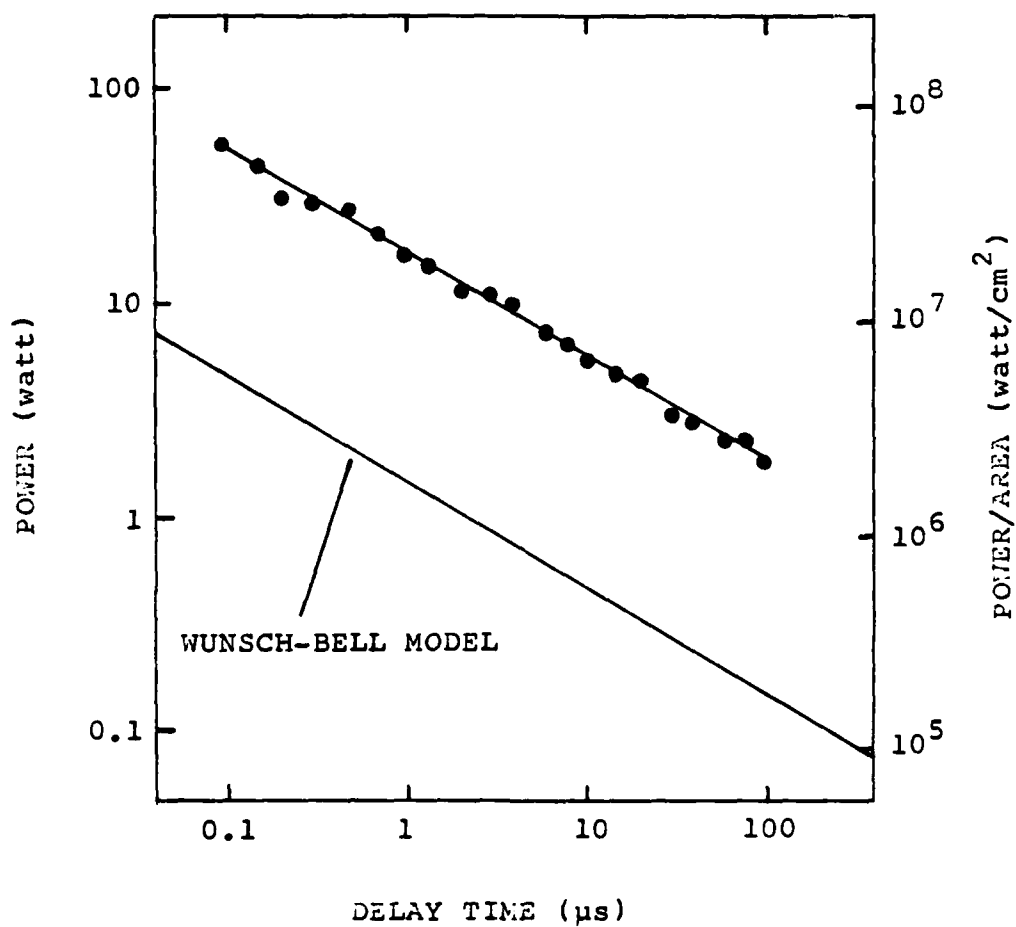


Fig. 89. Average power versus delay time for diodes on Wafer 2-5 with straight p^+n and n^+n junctions, an n-region length of 30 μm , and a width of 200 μm .

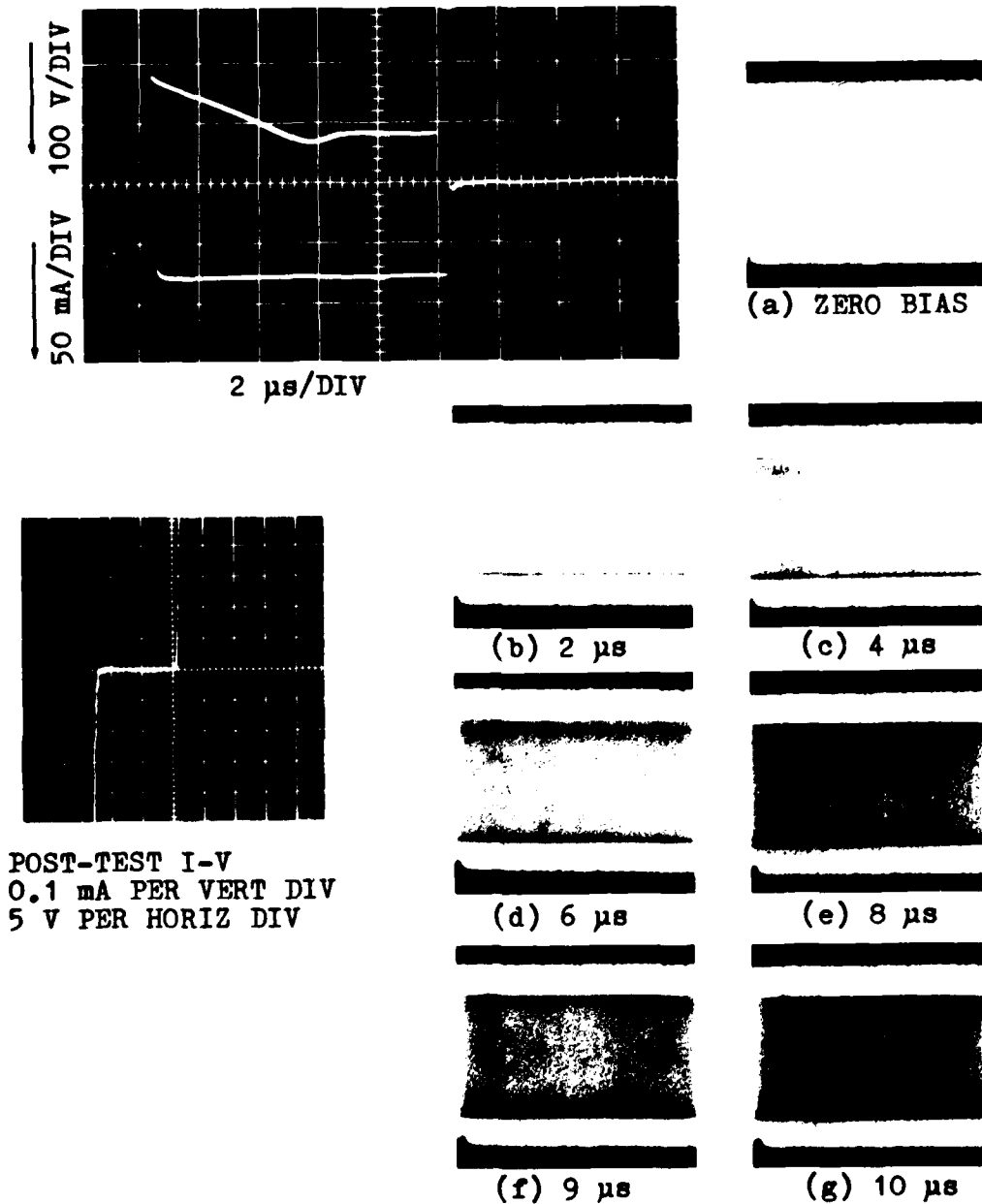


Fig. 90. Reverse bias test of a standard reference diode on Wafer 2-5. There is a hot spot on the n⁺n junction but only uniform heating on the p⁺n junction. The n-region length and width of this diode are 100 and 200 μ m, respectively. Current and voltage waveforms, and a post-test I-V characteristic are shown on the left side of the figure. (a) Zero bias photograph. (b)-(g) Heating patterns at 2, 4, 6, 8, 9, and 10 μ s after the leading edge of the waveforms.

90b-g, respectively. Current and voltage waveforms and a post-test I-V characteristic are also shown in Fig. 90. The p^+n junction is the lower boundary of the n-region for each of Figs. 90a-g. Figure 90 may be compared with Fig. 24, which was obtained for a diode of similar geometry under similar testing conditions.

The p^+n junction and n-region heating in Figs. 90b-d appears normal, but in Figs. 90e-g a hot spot forms on the left side of the n^+n junction and there is uniform heating along the remainder of the n^+n junction. Along the p^+n junction the heating is more intense than along the n^+n junction, but there is no hot spot. The voltage waveform also displays an unusual feature. A turnover occurs in the waveform about halfway through the pulse and then the voltage levels out. Normally, the turnover indicates that the diode is on the verge of second breakdown; it would not be expected to survive the remaining three microseconds to the end of the pulse. The current level is about 78 mA in Fig. 90, compared to 70 mA in Fig. 24, but the peak in the voltage waveform is slightly less. In Fig. 24, the peak voltage is about 260 V, while the peak voltage in Fig. 90 is about 230 V. Thus, the pre-failure energy thresholds are not greatly different. Comparison of the voltage waveform shapes in Figs. 90 and 24 shows similarity until about 6 μ s after the leading edge of the pulse, about 2 μ s before the hot spot appears. A second test of this diode at a current level of 70 mA showed normal waveform behavior and uniform heating along the p^+n junction, with no heating along the n^+n junction. A post-test I-V characteristic taken after the tests described above indicated that the diode behaved normally and that no damage had occurred.

Thus, it is possible for current constriction to exist along the n^+n junction of a diode, while only uniform heating occurs on the p^+n junction. However, this situation is very unlikely; based on the single event in the present study, the probability is on the order of 0.003.

8. Temperature Measurements

A stroboscopic photograph records the light transmitted through a specimen during the time of illumination by the strobe lamp. For the highly doped diodes of Wafer 2-5, stable configurations could be observed below the damage threshold at any position of the strobe light (duration 20 ns) relative to the applied 10 μ s current pulses. As shown in Fig. 91a, both the n -region and the junction depletion region become appreciably less transmitting. Just below the breakdown threshold, four temperature regions can be distinguished: those with no observable temperature rise (p^+ and n^+ regions of the test diode and the transparent regions of nearby diodes), partially darkened n -region, darkened junction region, and darkened filaments.

To convert darkness of film to temperature required a two-stage calibration procedure. First the film was calibrated with 15 different exposure steps. Then the transmittance of the specimen had to be measured as a function of temperature. This was performed by photographing the light transmitted through a homogeneous film of silicon 0.6 μ m thick on a sapphire substrate. The calibration specimen was part of the same batch of material as used in fabricating the devices and its doping level was that of Wafer 2-5. The stroboscopic lamp was the

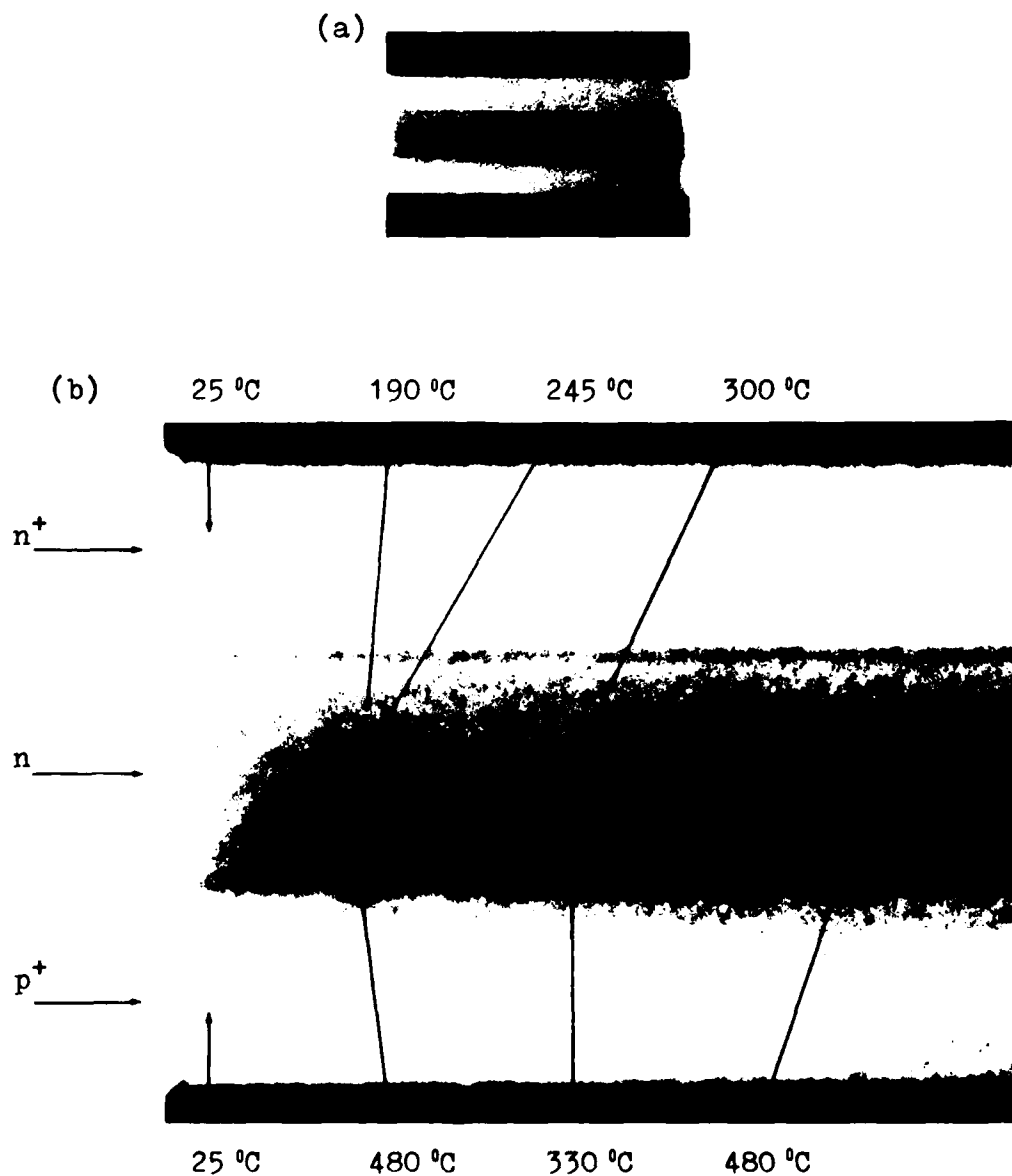


Fig. 91. Temperature measurements. (a) Heating pattern in a 30 x 200 μm reverse biased standard reference diode on Wafer 2-5. (b) Temperature map of the filament on the left side of part (a) and of the region near this filament.

light source during both parts of the calibration procedure. Temperature was controlled by passing a hot stream of argon gas about the specimen, which was located inside a steel cell with quartz windows. The transmitted light was recorded photographically on the same film (Polaroid Type 667) as used in the exposure calibration and regular experiments. A sequence of exposures was taken using 100 flashes of the strobe light for each temperature condition. The film darkening for each was then compared with that of the exposure calibration of the film and the relative exposure versus temperature data plotted on semi-log paper (see Fig. 92). The calibration curve, however, could not be applied directly to estimating the temperature of the current configurations because the diode fabrication procedure involved steps that thinned the silicon film. Finished devices are estimated by the group that fabricated them to be $0.4\text{ }\mu\text{m}$ thick. If the optical linear absorption coefficient is known at one temperature, then the calibration curve for the $0.6\text{ }\mu\text{m}$ film can be used to obtain the calibration curve for the $0.4\text{ }\mu\text{m}$ thick devices. Optical data were obtained from Ref. 50 ($\alpha = 1.05 \times 10^4/\text{cm}$ at 25 K for a wavelength of 500 nm) and the $0.4\text{ }\mu\text{m}$ calibration curve is also shown in Fig. 92. The ordinate, which represents relative exposure, is taken to be 100 for both thicknesses at room temperature ($25\text{ }^\circ\text{C}$).

Figure 91b contains a crude temperature map of the filament on the left side of Fig. 91a and of the region near this filament. Each temperature was measured by comparing local film darkening with the calibration films (to obtain relative exposure) and then, with room temper-

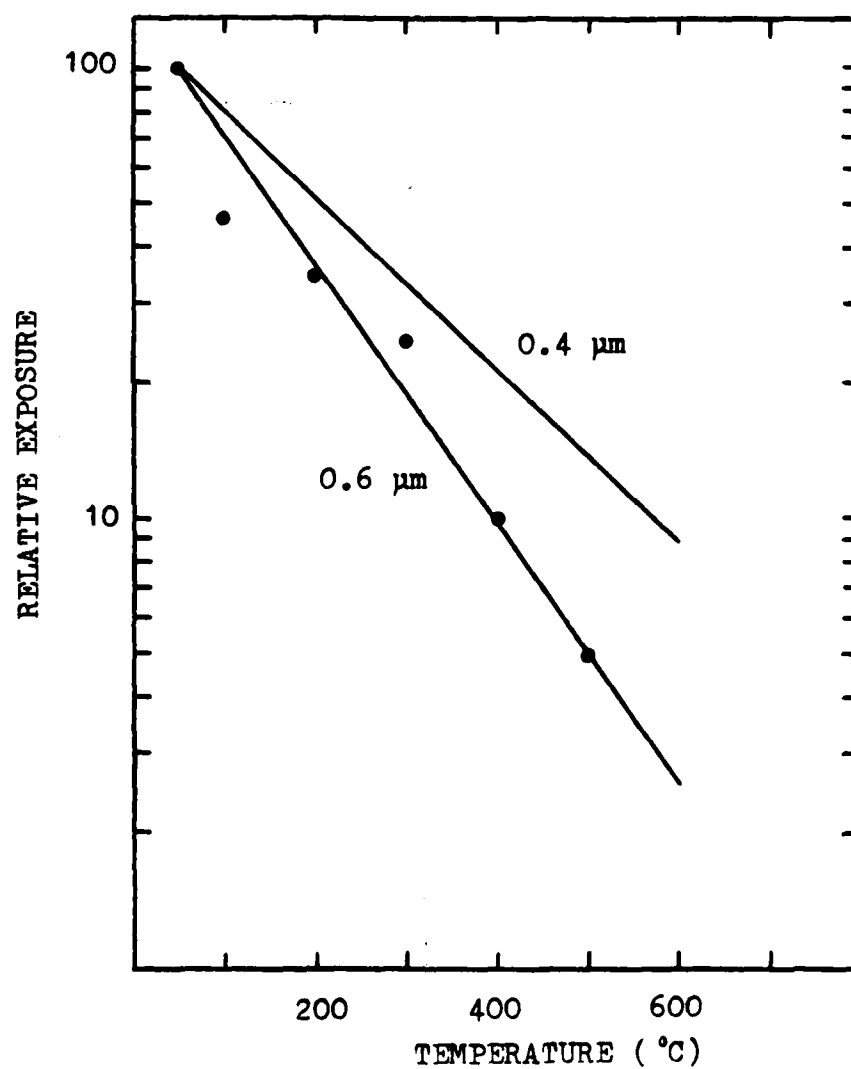


Fig. 92. Temperature calibration curve for silicon films 0.4 μm and 0.6 μm thicknesses.

ature as a reference, using the $0.4\text{ }\mu\text{m}$ curve of Fig. 92 to obtain the local temperature.

The peak temperature occurs at the base of the filament and is estimated to be $(480\pm30)\text{ }^{\circ}\text{C}$. The junction immediately adjacent to each filament is cool, indicating the current is channeled into the filament, and the junction is non-conducting adjacent to the filament. Figure 91 was obtained close to the damage threshold with the strobe light positioned at the end of each exciting pulse. For the present diodes, which have such small mass, the final transition to the destructive melt occurs very rapidly once the filament reaches across the n-region. The darkening at the base of each of the filaments of Fig. 91 is judged to be the same, so all are at the temperature $(480\pm30)\text{ }^{\circ}\text{C}$. If the filaments were about $200\text{ }^{\circ}\text{C}$ hotter, their self-emission would be strong enough to be observed photographically. However, even with more than 10^6 excitation pulses, no self-emission pattern from the filaments was obtained. This provides some confirmation on the temperature calibration. In the earlier experiments with films $1\text{ }\mu\text{m}$ thick, visible light from hot spots was photographed.¹⁸ The absence of such visible self-emission near the second breakdown threshold is attributed to the unusually effective heat sinking and the low heat capacity of the present devices.

VI. CONCLUSIONS

The present study extends the previous studies of Budenstein et al.¹⁸⁻²² by exploring the role of diode geometry on second breakdown susceptibility. In the previous work, only diodes with rectangular geometries were investigated. The present purpose was to extend the knowledge of second breakdown phenomena, and to determine how geometry and doping level affect susceptibility to second breakdown. The principal conclusions of the present study are presented in this chapter. These conclusions are divided into three general groups: heating patterns in Section A; energy, current, and voltage thresholds in Section B; and damage morphology in Section C. Since diode behavior was critically dependent upon n-region doping level, and variable among similar devices, a brief summary of device characterization is given below.

Resistivity and reverse bias breakdown voltage measurements were used to estimate n-region doping level. These methods were in agreement on Wafer 2-5, indicating a doping level of $(1.3 \pm .3) \times 10^{17} \text{ cm}^{-3}$. However, on Wafer 2-4 resistivity measurements indicated a doping level of $(1.2 \pm .2) \times 10^{16} \text{ cm}^{-3}$, while reverse breakdown measurements indicated $(4 \pm 2) \times 10^{16} \text{ cm}^{-3}$. These estimations do not overlap, and vary by a factor of five, indicating that at least one is in error. On Wafers 1-3, 2-2, and 2-1, all resistance measurements indicated a doping level of $(3 \pm 2) \times 10^{14} \text{ cm}^{-3}$, while all reverse breakdown measurements indicated $(5 \pm 4) \times 10^{15} \text{ cm}^{-3}$. Thus, there appear to be only three

distinct doping levels. In addition, the breakdown voltages of diodes on Wafers 2-1, 2-2, and 1-3 tend to "creep" upward during curve tracer measurements. This creeping of the I-V characteristic is to be distinguished from the damage caused by second breakdown and the resulting melt filament. Second breakdown is equivalent to placing a resistive short circuit across the junctions, yielding a high reverse leakage current and a large reduction in the reverse bias breakdown voltage.

Unless otherwise specified, the conclusions of this chapter relate to reverse biased diodes tested with 10 μ s pulses, and in Section A, to constant current tests of diodes with the highest n-region doping level (Wafers 1-5 and 2-5).

A. Heating Patterns

1. Second breakdown is associated with the growth of a hot spot completely across the high resistivity n-region of the diode and the subsequent formation of a damaging melt filament, regardless of whether the junctions are straight, curved, contain geometric defects, or contain corners. The hot spot temperature in diodes 0.4 μ m thick is about 500 °C.

2. Single or multiple hot spots may form along the p⁺n junction of a standard reference diode. These hot spots are typically spaced nonuniformly and have fixed positions in a given diode, for the diodes of the present study (thickness = 0.4 μ m). However, in similar, but thicker (0.9 μ m) diodes of a previous study¹⁸, hot spots were almost uniformly spaced and their number could be systematically increased by

increasing current amplitude and shortening pulse length. Microscopic inhomogeneities may determine current configurations in the thinner diodes.

3. In a single p^+n spike diode, a single hot spot forms at the tip of the spike. In multiple p^+n spike diodes containing three large spikes, a hot spot forms at the tip of each large spike. Hot spots do not form at other locations.

4. In a single n^+n spike diode, a single hot spot forms on the p^+n junction at a point which is usually opposite the spike. In multiple n^+n spike diodes containing three large spikes, there is usually a single hot spot, which forms opposite one of the large spikes. However, multiple hot spots similar to those in standard reference diodes can form in multiple n^+n spike diodes.

5. Hot spots tend to form only at the two protruding corners of the p^+n junction in enclosed reference diodes. However, if the junction width is close to the n -region width, then hot spot locations are similar to those in standard reference diodes.

6. A single hot spot forms in radius of curvature diodes. The hot spot is situated at the point on the p^+n junction where the p^+n and n^+n junctions are separated by a minimum distance.

7. Hot spots form on p^+n junction corners in interdigitated diodes. Current concentration also occurs at the n^+n junction corners. Thus, the highest current densities are at the corners of the p^+n and n^+n junctions, where field concentration and minimal n -region length occur.

8. Under forward bias, second breakdown is associated with the constriction of current into a broad filament which extends most of the way across the n-region, and the subsequent formation of a damaging melt filament interior to this broad filament.

9. Prior to filament formation under forward bias there is a narrow area adjacent to the p^+n junction which is not significantly heated, for diodes with n-region lengths of 30 μm or greater. This unheated region is typically 5 to 15 μm in length.

10. Single or multiple filaments may form in a forward biased standard reference diode, usually spaced nonuniformly. Single filaments form in forward biased p^+n and n^+n spike diodes; the filament extends from the spike to a point on the opposite junction. Single or multiple filaments may form in forward biased enclosed reference diodes.

11. The p^+n junction and n-region darkening at the second breakdown threshold is much less intense for diodes of Wafer 2-4 with a measured doping level of $(3 \pm 2) \times 10^{16} \text{ cm}^{-3}$. For diodes with measured doping levels of roughly 10^{15} cm^{-3} , the darkening is so faint that it is almost undetectable. Reduced darkening at the second breakdown threshold occurs because silicon reaches the peak of its resistivity-temperature curve at lower temperatures as the doping density decreases.

12. A hot spot may form on the n^+n junction. However, this was observed only once in over 300 diodes.

13. The current interval between formation of a hot spot and second breakdown is typically about 1% of the total current at failure for

standard reference diodes. However, for p^+n spike diodes the current interval between hot spot formation and second breakdown may be as much as 10% of the failure current amplitude. On Wafer 2-4, this current interval is narrower, less than 1% of the failure current for both standard reference and p^+n spike diodes. The current interval between hot spot formation and second breakdown for diodes on Wafers 1-3, 2-2, and 2-1 is so narrow that damage always occurred before hot spots were observed.

14. Almost any p^+n or n^+n junction irregularity has an effect on current configurations near the second breakdown threshold. Current concentrates at p^+n junction spikes, opposite n^+n junction spikes, at p^+n junction corners, at p^+n and n^+n junction corners of interdigitated diodes, and on curved p^+n junctions at the point closest to the n^+n junction. However, metal- p^+ and metal- n^+ spikes have no effect on current configurations near the second breakdown threshold.

B. Energy, Current, and Voltage Thresholds

1. The total energy input at the second breakdown threshold increases approximately linearly with n-region length for both standard reference and diffusion spike diodes on Wafer 2-5, with slopes of $1.6 \pm .2 \mu\text{J}/\mu\text{m}$ for diode widths of $200 \mu\text{m}$. The $5 \mu\text{m}$ diffusion spikes lower the average failure thresholds of diodes with an n-region length of $10 \mu\text{m}$ roughly 50%, but the reduction is 30% or less for longer n-region lengths, with p^+n spikes more effective than n^+n spikes in lowering failure thresholds. The n-region length is more important than diffusion spikes in determining failure energy thresholds of diodes on Wafer 2-5, for n-region lengths greater than $10 \mu\text{m}$.

2. The current amplitude (for devices of the same width and parallel junction geometry) at the second breakdown threshold is largely independent of n-region length and the presence of diffusion spikes for diodes on Wafer 2-5 tested with constant current pulses. The average current density at the failure threshold is about 10^9 A/m^2 .

3. The $5 \text{ }\mu\text{m}$ diffusion spikes lower the average energy failure thresholds of diodes on Wafer 2-4 with n-region lengths of 10 and $30 \text{ }\mu\text{m}$ roughly 25-50%. The corresponding current amplitudes at failure are reduced roughly 5-30% (constant current pulses). The current density at the failure threshold is typically $(3.5 \pm .5) \times 10^8 \text{ A/m}^2$.

4. The average energy failure thresholds of diodes on Wafer 2-1 with an n-region length of $10 \text{ }\mu\text{m}$ are reduced a factor of 1/100 by the presence of $5 \text{ }\mu\text{m}$ diffusion spikes. Such a device, in a group of uniform junction devices, would be classified as a "maverick." The large reduction in energy threshold is caused by punchthrough of the n-region, and indicates the vulnerability to junction inhomogeneities of semiconductor devices containing thin layers with low doping levels. However, punchthrough is a voltage dependent effect and energy threshold data may overestimate its importance. The voltage failure thresholds of $10 \text{ }\mu\text{m}$ n-region length diodes are reduced about 50% by the presence of $5 \text{ }\mu\text{m}$ diffusion spikes. The $5 \text{ }\mu\text{m}$ diffusion spikes lower average energy failure thresholds of diodes on Wafer 2-1 with an n-region length of $30 \text{ }\mu\text{m}$ roughly 50-75%. The corresponding current failure thresholds are reduced 50-60%, with average current densities in the range $(5 \pm 2) \times 10^7 \text{ A/m}^2$.

5. Voltage failure thresholds increase in an approximately linear manner as n-region length increases for standard reference, p^+n and n^+n single and multiple spike, enclosed reference, and radius of curvature diodes for each of the five nominal doping densities. For standard reference diodes, the increase is $2.7 \text{ V}/\mu\text{m}$ on Wafer 2-5, $6.0 \text{ V}/\mu\text{m}$ on Wafer 2-4, and $(8 \pm 2) \text{ V}/\mu\text{m}$ on Wafers 1-3, 2-2, and 2-1.

6. Average current density failure thresholds for similar geometries increase as the n-region doping level increases 10^{14} to 10^{17} cm^{-3} , while voltage failure thresholds decrease. The current threshold is approximately proportional to $\rho^{-3/4}$, where ρ is the n-region resistivity. The effect of diffusion spikes on current thresholds is smaller than that of n-region doping level. However, the increase in current thresholds is partially cancelled by the decrease in voltage thresholds in the determination of failure energies. Thus, diffusion spikes have a larger relative importance on energy failure thresholds than on current and voltage failure thresholds.

7. Voltage failure thresholds increase as n-region length increases, and as n-region resistivity increases. This supports Reich and Hakim's conclusion that hot-spotting is retarded as the product of resistivity and thickness of the collector material increases. Energy failure thresholds increase as n-region length increases, but decrease as n-region resistivity increases.

8. Under reverse bias constant current tests, a turnover in the voltage waveform indicates that the diode is close to the second breakdown threshold.

9. There is often wide variation in the energy and current failure thresholds of similar devices at the lower doping levels. However, there is less variation in the voltage failure thresholds.

10. Power versus delay time follows the power law dependence $t_p^{-1/2}$ predicted by the Wunsch-Bell model for diodes on Wafer 2-5 with straight p^+n and n^+n junctions and with n -region lengths of 30 μm and widths of 200 μm . Data cover delay times between 0.1 μs and 100 μs . Energy failure thresholds increase as $t_p^{1/2}$. Other geometries were not investigated.

11. In the voltage threshold tests, there was often a substantial difference in the statistical distributions of failure voltages of standard reference, p^+n spike, and n^+n spike diodes. In some cases, the voltage two standard deviations above the spike diode distribution was less than the voltage two standard deviations below the standard reference diode distribution. This suggests a simple screening technique to eliminate a substantial percentage of spike diodes from a group containing standard reference and spike diodes: application of a single constant voltage pulse with an amplitude two standard deviations below the mean failure voltage of the standard reference diodes. Approximately 2% of standard reference diodes are destroyed by this screening technique (those with abnormally low failure thresholds), but a larger percentage of spike diodes are destroyed (in some cases, almost 100%). The remaining diodes are undamaged. The practical appli-

cation of such a screening technique is discussed in Chapter XIII.

12. Spikes on the metal- p^+ or the metal- n^+ junctions have no effect on diode failure thresholds.

C. Damage Morphology

1. Damage occurs, with greater than 98% probability, by formation of a melt filament across the high resistivity n-region of the diode. The remaining diodes fail by damage to the aluminum metallization.

2. Filaments in standard reference diodes on Wafers 2-5 and 2-4 occur in random locations for n-region lengths of 10 μm , but tend to be grouped on one side of the diode for longer n-region lengths. On Wafers 1-3, 2-2, and 2-1 filaments tend to lie along one of the diode edges.

3. Filaments in p^+n and n^+n spike diodes tend to have one endpoint at the tip of the spike. Part of the filament path may lie along the diode edges on Wafers 1-3, 2-2, and 2-1.

4. Filaments in enclosed reference diodes tend to have one or both endpoints on the protruding junction corners, but this tendency decreases with decreasing n-region length. Part of the filament path may lie along the diode edges on Wafers 1-3, 2-2, and 2-1.

5. Filaments in radius of curvature diodes are straight and connect the p^+n and n^+n junctions at the points of minimum separation. The threshold current density, as judged by microplasma emission, is about the same in the region of smallest separation as in uniform junction diodes with the same separation.

6. Filaments in interdigitated diodes connect the p^+n and n^+n junction corners.

PART II. THEORY

VII. BACKGROUND

Behavior of semiconductor devices is generally believed to be adequately described by the simultaneous solution of Maxwell's equations and the heat conduction equation, with proper constitutive equations. In practice, the complex geometry of devices, need for dynamical solutions, and uncertainties in the constitutive equations make rigorous solutions impossible for realistic situations. Thus there is need to modify these equations with appropriate approximations that will simplify calculations and yet retain the main physical characteristics of the device. Solutions must include the constraints imposed by the circuit environment of the device. Following is a brief description of such efforts.

A. Semiconductor Device Simulation

Shockley's initial approach to pn junction theory⁵¹ was to divide a one-dimensional device having an abrupt metallurgical transition from p region to n region into two distinct types of regions: those that are nearly field-free (major portions of the p and of the n region) and those that are dominated by the space charges of the ionized impurities (the junction depletion region). The continuity equation, with both field and diffusion terms, was solved in each field-free region for a chosen junction current. In the space charge region, Poisson's equation was solved with the condition that the electric field be continu-

ous at the edges of the depletion region. Carrier concentrations were determined by Fermi statistics with the aid of quasi-Fermi levels for holes and electrons in the regions where both diffusion and field effects were important. Various other works^{52,53} performed along the same direction met with limited success. With rapid progress of semiconductor technology, such simplified and largely intuitive methods proved to be inadequate for dealing with transistor geometries (such as narrow base regions) and real doping profiles (graded junctions) and the need to treat the device as a whole became apparent. This could only be done by numerical solutions. Over the past decade or so, a host of numerical methods for the solution of both one and two-dimensional semiconductor problems have been reported. Early treatments were isothermal, with no dynamic temperature effects.

Gummel⁵⁴ developed a self-consistent, iterative scheme for the case of one-dimensional, steady-state transistor calculations. His work was based on the assumption that electron concentration, hole concentration and electric field define the state of the semiconductor. His basic equations are given below in terms of their normalized equivalents.

Gummel, following Shockley, used quasi-Fermi levels for electrons and holes as a strategy for including field and diffusion effects in a mathematically convenient manner. Definitions of the quasi-Fermi potentials ϕ_n and ϕ_p in units of kT/q are:

$$p = e^{\phi_p - \psi} \quad (7.1a)$$

$$n = e^{\psi - \phi_n} \quad (7.1b)$$

where

k Boltzmann constant

T device temperature

q electronic charge

n_i intrinsic carrier concentration

ψ electrostatic potential in units of kT/q

ϕ_p hole quasi-Fermi potential in units of kT/q

ϕ_n electron quasi-Fermi potential in units of kT/q

p hole concentration in units of n_i

n electron concentration in units of n_i

His expressions for current densities of electrons and holes, which include both diffusion and field terms, are (in units of $(qD_0n_i)/L_D$):

$$J_p = - \frac{D_p}{D_0} \left[\frac{d}{dx} (e^{\phi_p}) \right] e^{-\psi} \quad (7.2a)$$

$$J_n = \frac{D_n}{D_0} \left[\frac{d}{dx} (e^{-\phi_n}) \right] e^{\psi} \quad (7.2b)$$

where

J_n electron current density

J_p hole current density

D_p hole diffusion constant

D_n electron diffusion constant

D_0 a reference diffusivity

L_D a unit length $(= \frac{kT}{q^2 n_i})$

ϵ permittivity of silicon

If recombination of minority carriers is taken into account, the current density gradients as they occur in the continuity equation become:

$$-\frac{dJ_p}{dx} = \frac{dJ_n}{dx} = \frac{L_D^2}{D_0 n_i} U \quad (7.3)$$

where

$$U = n_i \frac{e^{\phi_p - \phi_n} - 1}{\tau_p (e^{-\phi_n} + e^{\phi_t}) + \tau_n (e^{\phi_p - \psi} + e^{-\phi_t})} \quad (7.4)$$

τ_p lifetime of excess holes

τ_n lifetime of excess electrons

ϕ_t energy level of recombination center.

Poisson's equation, relating electrostatic potential to space charge density, is shown by Gummel to reduce to

$$\frac{d^2 \psi}{dx^2} = e^{\psi - \phi_n} - e^{\phi_p - \psi} - N \quad (7.5)$$

where

N ionized impurity concentration in units of n_i ,

positive for donors and negative for acceptors.

Determinations of ϕ_p and ϕ_n were made from ψ by considering Eq. 7.2.

For ϕ_p

$$\frac{d}{dx} (e^{\phi_p}) = -J_p \gamma_p e^{\psi} \quad (7.6)$$

where

$$\gamma_p = D_0/D_p$$

Integrating Eq. 7.6

$$e^{\phi_p(x)} = \int_0^x J_p(t) \gamma_p(t) e^{\psi(t)} dt + \text{constant} \quad (7.7)$$

By finding proper values for J_p and the constant of integration such that ϕ_p has the correct value at the boundaries, ϕ_p is completely determined. Likewise, ϕ_n can be determined. His iteration scheme consisted of choosing a current density and making an initial guess at the electrostatic potential, calculating hole concentration using Eqs. 7.7 and 7.5 and then obtaining a new and better approximation for the electrostatic potential from Poisson's equation and hole concentration from the previous step. Continued iterations of the above scheme were carried out until the required convergence was obtained. Even though Gummel's work was later found to be inadequate for high reverse-bias conditions, it still forms the foundation of numerous other semiconductor device simulation techniques.

De Mari⁵⁵ extended Gummel's work to solve the case of high reverse-bias conditions. The equations used are shown below, with all quantities normalized as in Gummel.

$$J_n(x) = \frac{1}{\gamma_n(x)} \left[n(x) \frac{d\psi(x)}{dx} - \frac{dn(x)}{dx} \right] \quad (7.8a)$$

$$J_p(x) = \frac{1}{\gamma_p(x)} \left[p(x) \frac{d\psi(x)}{dx} + \frac{dp(x)}{dx} \right] \quad (7.8b)$$

$$\frac{d^2\psi(x)}{dx^2} = n(x) - p(x) - N(x) \quad (7.9)$$

$$\frac{dJ_n(x)}{dx} = -U(x) \quad (7.10a)$$

$$\frac{dJ_p(x)}{dx} = U(x) \quad (7.10b)$$

Equations 7.10a and 7.10b imply that

$$\frac{dJ}{dx} = 0, \text{ and } J = J_n(x) + J_p(x) \quad (7.11)$$

where

J total current density

U generation-recombination law

$\frac{1}{\gamma_n}$ electron mobility

$\frac{1}{\gamma_p}$ hole mobility

The model was suitable for arbitrary doping profiles, generation-recombination laws, mobility dependencies and boundary conditions. De Mari also treated a one-dimensional pn junction under arbitrary transient conditions using the time-dependent version of the same equations. Thus, given an arbitrary current or voltage input signal as a function of time, field and related quantities were obtained as functions of both time and position⁵⁶. Later, a finite difference approximation was used by Scharfetter and Gummel for the one-dimensional transient case⁵⁷. Various other one-dimensional models treated special situations, such as diffused junctions⁵⁸, heavy recombination rates⁵⁹, and bipolar semiconductor devices⁶⁰. Also worth mentioning is a very efficient and general program devised by Hachtel, Joy and Cooley⁶¹ for bipolar device modelling, design and performance projection. All of the above were isothermal solutions.

An iterative scheme based on Gummel's first work was extended to two-dimensional dc transistor simulation by Slotboom⁶². Vandorpe and Xuong⁶³ devised a model valid for any two-dimensional semiconductor device and obtained results for MOS transistors, bipolar transistors, and pn junctions that are very reliable. The set of transport equations they used included surface effects and was workable even under condi-

tions of high applied voltages. Similarity of semiconductor transport flow equations with those of incompressible liquids gave rise to a new solution of the time-dependent semiconductor transport equations that is especially suitable for FETs.⁶⁴

Reiser,⁶⁵ and Lee, Lomax and Haddad⁶⁶ have written review articles of existing literature on semiconductor device simulation techniques. More recently, calculations that predict the internal behavior of power transistors operating under steady-state but non-isothermal conditions have been published.⁶⁷ Proceedings of a conference on modeling semiconductor devices, held recently (1977) in Switzerland, provides a good indication of current progress in this field.⁶⁸

B. Current Filamentation

Current filamentation is a phenomenon in which a region having relatively uniform current density switches so that the current density becomes very non-uniform, with one or more localized highly conducting channels.

Tauc and Abraham⁶⁹ noticed heavy currents through hot gaps in the potential barrier while investigating thermal breakdown in avalanching silicon pn junctions. They concluded that the switching on the junction from normal avalanche breakdown into the higher conductance state was caused by the high temperature at a small part of the junction. The potential across the local hot spots was assumed to drop to zero, allowing a large current. The major part of the device current passed through the gap and provided the necessary Joule heating needed to maintain the high temperature. They assumed that normal avalanche

breakdown can lead to this kind of breakdown if it is energetically more economical.

The first conclusive experimental evidence of filament formation was shown by Melingailis and Milnes.⁷⁰ Doped germanium bars at liquid helium temperature (to keep thermal energy low in comparison with impurity activation energy) of 4.2 K were pulsed with 5 μ s, low repetition rate, constant voltage pulses. Increase of current after ionization, a gradual voltage rise and an eventual saturation of the current at high fields were noted. They concluded that filament diameter changes with density of uncompensated impurities ($N_D - N_A$) and also with current. Ridley²⁵ discussed filamentation from the standpoint of irreversible thermodynamics and analyzed the conditions for both current-controlled and voltage-controlled specific negative resistance in a slab of material that was initially electrically isotropic. He pointed out that a differential negative resistance causes instability in the material and the material splits into regions of different electrical conductivity in an attempt to reach stability. Subsequent formation of current filaments (high-field regions in the case of voltage-controlled negative resistance) then creates stable states. The state having the least Joule heating is the preferred one out of all the electrically possible states. This preference eventually leads to optimum sizes for filaments. Various other studies involve such diverse topics as prediction of stable current filaments in avalanching p - i - n diodes,⁷¹ realistic modeling of $P^+ - n - n^+$ diodes to study the influence of device parameters on current density at which negative resistance sets in,⁷² filament current density profiles and total filament

current as a decreasing function of the applied voltage in avalanching $p^+ - i - n^+$ diodes¹¹ and rapid and reversible transition between highly resistive and conductive states effected by an electric field.²³

Barnett and Milnes⁷³ were the first to observe space-charge limited current filaments in single crystal silicon experimentally. A comprehensive chapter on current filamentation in semiconductors has been written by Barnett.²⁴

In another study by Wilson, Hill and Mathews⁷⁴ the method of finite elements has been applied to analyze two-dimensional currents in a pn junction before, during and after second breakdown. Special operating conditions, such as current crowding, can be included in this procedure. However, the method was not actually utilized in calculations because of its complexity. Specific studies have also been made in various other areas such as filamentation in homogeneous thin silicon films,¹⁹ second breakdown and current distribution in transistors,² avalanching and second breakdown current distribution in SOS diodes,¹⁷ single and multiple filaments in SOS diodes during second breakdown.²⁰ Formation of high-current filaments in GaAs IMPATT diodes have been directly shown by Olson⁷⁵ to be a natural consequence of operation in a negative resistance region. Another simple two-dimensional thermal model of an avalanche diode chip, put forth by the same author, produces current filaments as stable current distributions.⁷⁶ It also yields temperature profiles across the chip area with a local temperature rise high enough to melt silicon (m. p. 1683 K).

From the above review, it is apparent that in the past, simplifications have been made by focussing attention on a restricted aspect of the overall problem. Each of the special solutions has provided some special, useful insight. None, however, have been sufficiently wide in scope to give the desired broad perspective.

In this study, a comprehensive model for describing current filamentation in planar (silicon-on-sapphire) $p^+ - n - n^+$ diodes is presented. The intent of the model is to provide improved perspective on the role of junction irregularities, n-region length and doping density on current configurations under reverse or forward biases. The model can be applied for different circuital constraints and it yields device waveforms, temperature distributions, and other detailed information. The model is an outgrowth of one developed by Pontius, Smith and Budenstein²⁰ to describe current filamentation in a thin homogeneous silicon film on a sapphire substrate.

VIII. ELECTROTHERMAL MODEL FOR CURRENT FILAMENTATION

The proposed electrothermal model seeks to describe filament growth in $p^+ - n - n^+$ SOS diodes subjected to high amplitude pulses. The model is applicable to forward and reverse biases, to different circuit constraints, and different device parameters. In the present work, the model will be applied to diodes having straight junctions and junctions with spikes subjected to reverse bias constant current pulses of 1-15 μs duration.

A. Diode Configuration for Model

For purposes of calculations, the SOS diode is divided into regions as shown in Fig. 93. Four principal regions can be distinguished: p^+ region, $p^+ n$ depletion region, n region, and n^+ region. The width of the diode is divided into N uniform strips that run the length of the diode. Each strip, in turn, is subdivided into M segments, as indicated in Fig. 94a. The p^+ and n^+ portions of each strip are taken to be single segments because their high electrical conductivities preclude appreciable thermal effects during the conditions of concern here. Each strip has its n region divided into many small segments. The segment adjacent to the $p^+ n$ interface is the junction depletion region. The subscript j is used to identify the strips and the subscript k is used to identify the segments.

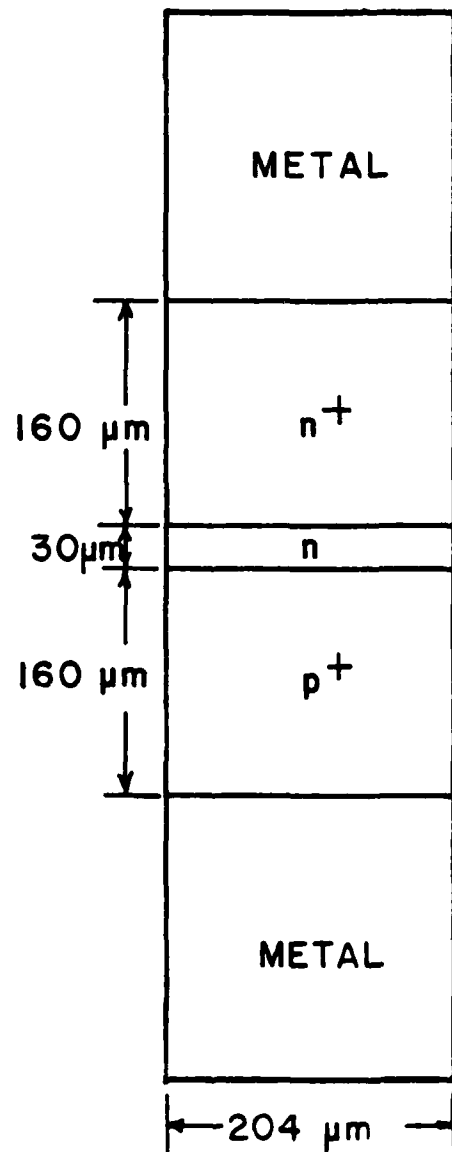


Fig. 93. Geometry of a silicon-on-sapphire diode with uniform junctions.

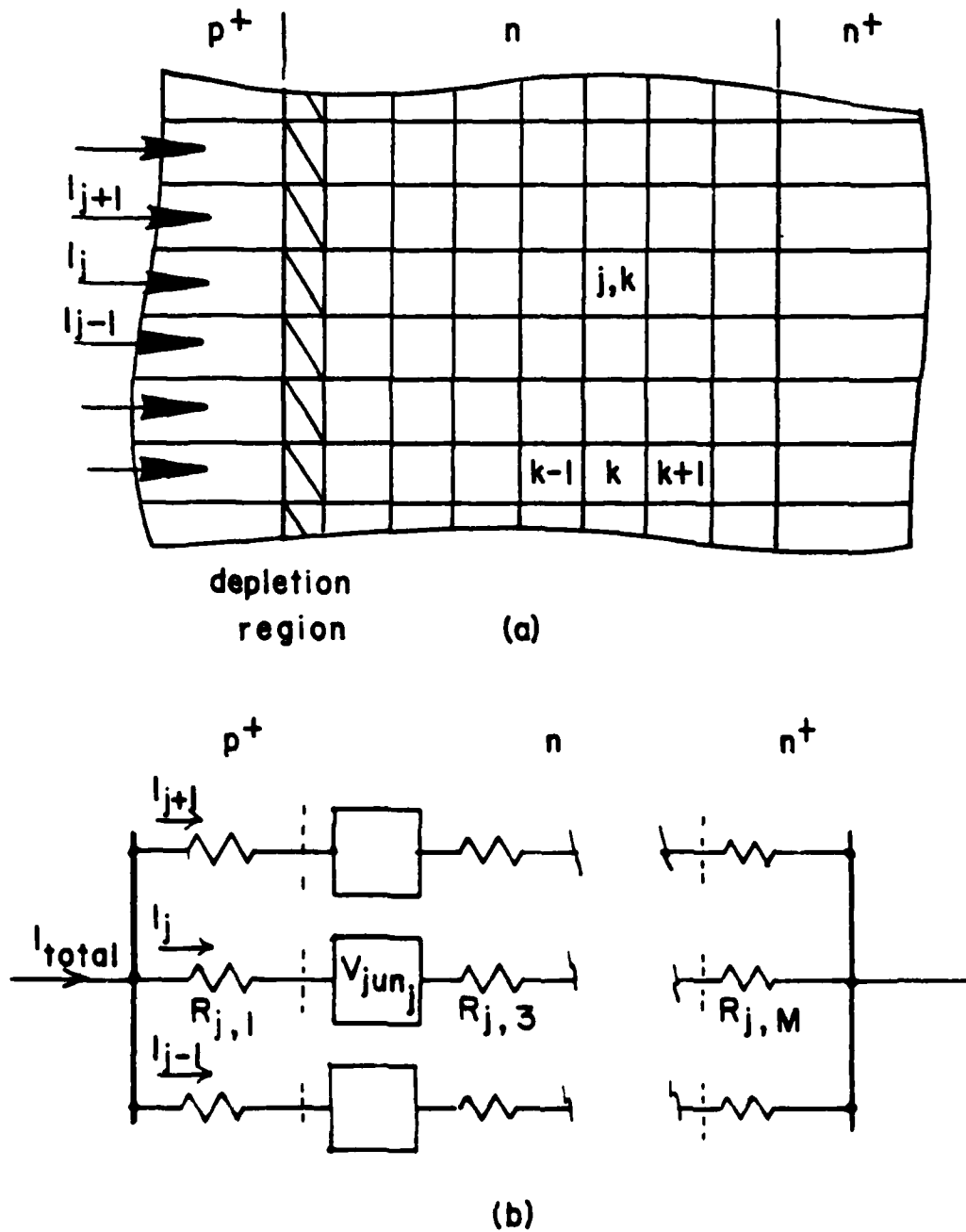


Fig. 94. Division of the diode into elements. (a) Longitudinal strips are identified by the index j . Each of the j strips is subdivided into M segments, which are specified by the index k . (b) Electrical network employed in the electrothermal model to represent the diode.

B. Equations of the Model

The depletion region is governed by Poisson's equation, continuity equation and the related constitutive equations. These equations, when solved with proper boundary conditions, yield the junction voltage as functions of current density and temperature. Due to the importance of this region in the overall electrothermal model, all of Chapters IX and X are devoted to solving and analyzing, respectively, the problem of a one-dimensional p^+n junction. Thus, throughout the remainder of this chapter, the junction voltage is assumed to be a known function of current density and temperature.

The properties of the junction and of the other segments are temperature dependent. The proposed electrothermal model is solved by means of a two-step progression, each time step requiring first the solution to the electrical problem and then the thermal. At time $t=0$, the temperature of all parts of the diode is assumed constant and set equal to that of the substrate.

A one-dimensional description is used for the electrical conduction in each strip. (Thus the present model does not include the effect of the spreading resistance associated with current lines converging on a junction hot spot.) An electrical network is used to represent the reverse biased, subdivided diode of Fig. 94a, as shown in Fig. 94b. A step current is applied at time $t = 0$. Initially, the current divides equally among all the strips as the temperature is the same in all strips. The sum of the currents in all of the strips must add up to the total current I_{tot} at all times,

$$I_{\text{tot}} = \sum_{j=1}^N I_j \quad (8.1)$$

At every instant of time, the voltage across any strip of the diode must be the same as that across any other strip and equal to the terminal voltage V_{tot} . The terminal voltage is a function of time because of changes in the electrical properties of the system with temperature.

$$V_1 = V_2 = \dots = V_j = V_{j+1} = \dots = V_{\text{tot}} \quad ,$$

where the voltage across the j th strip is

$$V_j = (V_{\text{jun}})_j + I_j \sum_{k=1}^M R_{j,k} \quad (8.2)$$

Here $R_{j,k}$ is the resistance of the k th segment of the j th strip and $(V_{\text{jun}})_j$ is the voltage across the junction of the j th strip and is obtained as delineated in Chapter IX.

The thermal portion of the problem is solved by equating the increase in internal energy in each small segment to the algebraic sum of the heat added to that element from the four surrounding elements, the substrate and the Joule heating of the segment during the previous time interval (Eq. 8.3).

$$\begin{aligned} c_{j,k} m_{j,k} \Delta T_{j,k} &= \Delta Q_{j,k} \\ &= \Delta Q_{j,k+1;j,k} + \Delta Q_{j,k-1;j,k} \\ &+ \Delta Q_{j+1,k;j,k} + \Delta Q_{j-1,k;j,k} \\ &+ \Delta Q_{s;j,k} + I_j^2 R_{j,k} \end{aligned} \quad (8.3)$$

where $c_{j,k}$ specific heat capacity of silicon

$m_{j,k}$ segment mass

$\Delta T_{j,k}$ increase in temperature of segment (j,k) during time interval

$\Delta Q_{j,k}$ heat added to segment (j,k) during time interval

Here the heat added to the element j,k by element j,k+1 is designated as $\Delta Q_{j,k+1;j,k}$. Thus, the first four terms on the right hand side of Eq. 8.3 represent the heat gained by the j,k segment from its four nearest neighboring strips. The fifth term is the heat added (negative) to the element j,k from the substrate, while the last term expresses Joule heating. The heat transfer to the substrate will be discussed further in the next section.

The functional form of the lateral heat exchange terms on the right hand side of Eq. 8.3 is based on the expression for one-dimensional heat conduction, i.e.,

$$\Delta Q_{j,k+1;j,k} = K_{Si}(T) A_{j,k+1;j,k} \frac{T_{j,k+1} - T_{j,k}}{\Delta x_{j,k+1;j,k}} \quad (8.4)$$

where

$K_{Si}(T)$ thermal conductivity of silicon

$A_{j,k+1;j,k}$ cross sectional area for heat transfer from element j,k+1 to element j,k

$\Delta x_{j,k+1;j,k}$ effective distance between elements j,k+1 and j,k

$T_{j,k+1} - T_{j,k}$ temperature difference between the j,k+1 and j,k elements.

Thus, for example, to calculate $\Delta Q_{j,k+1;j,k}$, the area $A_{j,k+1;j,k}$ will be the product of film thickness and the length of the side common to elements j,k+1 and j,k. $\Delta x_{j,k+1;j,k}$ is taken to be approximately the

center-to-center distance between elements $j,k+1$ and j,k . In practice, there is a very delicate balance among the terms in Eq. 8.3 and it is necessary to select the Δx 's properly. Experiments provide guidance on this selection. In diodes having a thickness of $0.6 \mu\text{m}$ and element dimensions of $4 \mu\text{m}$ by $4 \mu\text{m}$, $A_{j,k+1;j,k} = 2.4 (\mu\text{m})^2$ and $\Delta x_{j,k+1;j,k} = 2 \mu\text{m}$.

Thermal conductivity of a material is a decreasing function of temperature. The experimental thermal conductivity data plotted in Fig. 95, taken from Ref. 77 for silicon and Ref. 78 for sapphire, were used in the present computer program.

The edge of the device is assumed to stay at constant temperature. This leads to a temperature gradient between the longitudinal strips. An additional temperature gradient arises along each strip because of the thermal dissipation at the junction (reverse bias condition) and the higher resistivity of the n region compared to that of the p^+ and n^+ regions.

Thus, to summarize the overall approach taken in solving the electrothermal problem, the following steps are executed.

- (1) Set all elements (j,k) equal to the substrate temperature T_s .
- (2) Assume a trial current distribution. For the case of uniform initial temperature and the geometry of Fig. 93, the current divides equally among the N strips. For a non-uniform initial temperature configuration, the trial current density is the starting point for an iterative procedure to establish the current distribution.

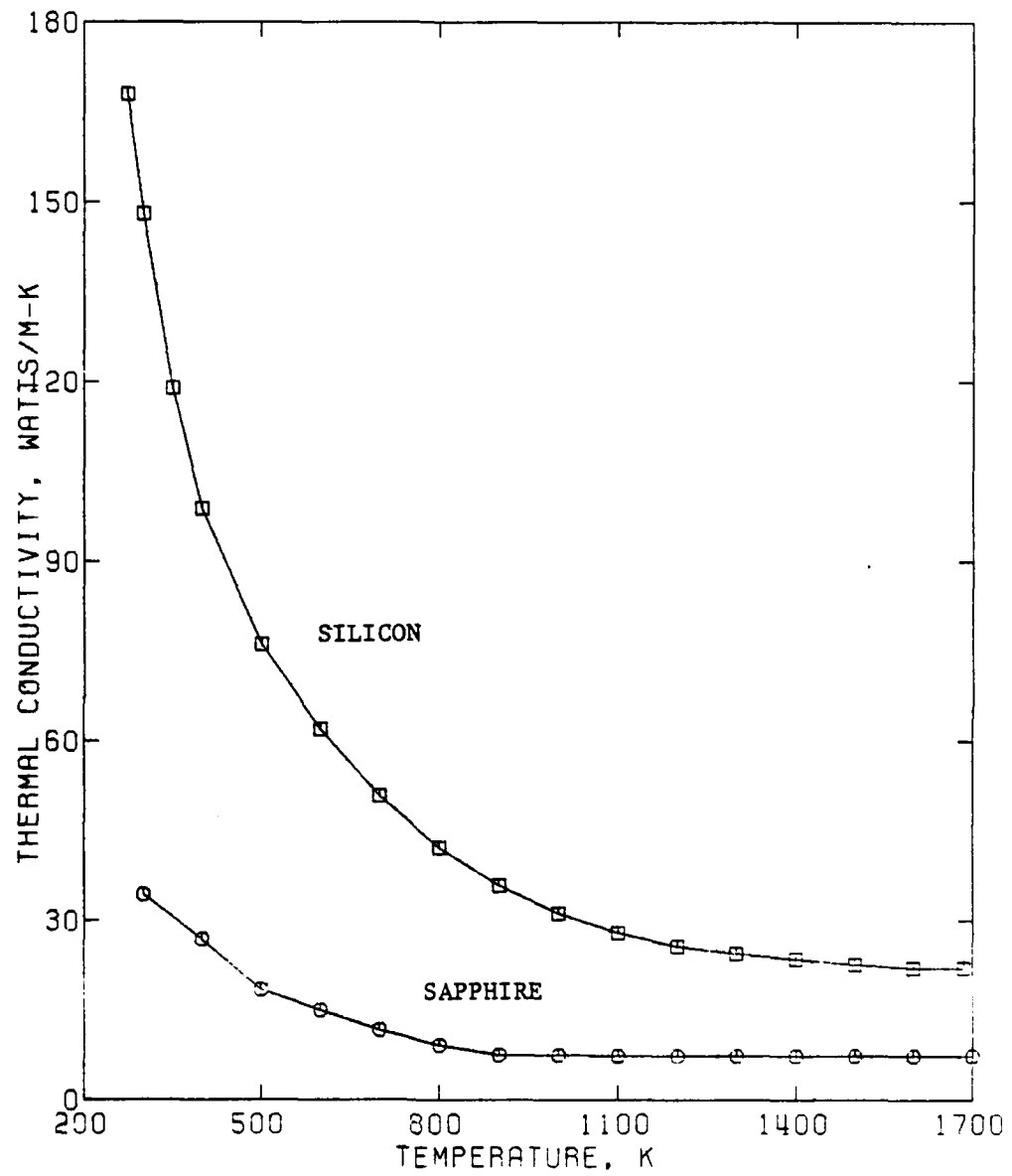


Fig. 95. Thermal conductivities of silicon and sapphire as functions of temperature. (Ref. 77, 78)

- (3) Solve for thermal effects by calculating the heat added to each element from its four nearest neighbors and the substrate, and the Joule heating of the element. Thus the temperature of each element is modified and the device exhibits a new temperature profile.
- (4) Compute the material parameters for each element at the new temperature.
- (5) Obtain a new current distribution in the strips using the material properties of the new temperature distribution. An iterative procedure is used to obtain the new current distribution.
- (6) Repeat steps (3) through (5), in that order.
- (7) Terminate the solution at the end of the desired pulse length, or when a portion of the device reaches the melting point, or when the solution becomes unstable due to the extremely rapid growth of current filaments during the time increments prescribed.

C. Discussion of Substrate Heat Flow Term

Amongst all the terms in the above energy exchange equation (Eq. 8.3), the substrate heat transfer term, $\Delta Q_{s;j,k}$, is the most complex and requires a detailed discussion. Below is an approximate, but believed to be physically meaningful, method for calculating this term.

Heat transfer rate to the substrate is given by

$$\left(\frac{dQ}{dt}\right)_{s;j,k} = -K_{sa}(T) A_{s;j,k} \left(\frac{dT}{dz}\right)_{s;j,k} \quad (8.5)$$

where

- z space coordinate, with the sapphire-silicon interface located at $z=0$, and the sapphire being in the region of positive values of z .
- $K_{sa}(T)$ thermal conductivity of the sapphire substrate (temperature dependent)
- $A_{s;j,k}$ area across which heat flows from element j,k into the substrate
- $(\frac{dT}{dz})_{s;j,k}$ temperature gradient evaluated at the interface of element j,k and the substrate.

The term $\Delta Q_{s;j,k}$ of Eq. 8.3 is then

$$\Delta Q_{s;j,k} = - K_{sa}(T) A_{s;j,k} (\frac{dT}{dz})_{s;j,k} \quad (8.5a)$$

The difficulty arises in accurately determining the quantity $(dT/dz)_{s;j,k}$ in Eq. 8.5a. Various investigators (79,80) have circumvented this problem by using an alternative expression to Eq. 8.5a, such as a simple law of cooling,

$$\frac{dQ}{dt} = - \frac{\Delta T}{\theta_R} \quad (8.6)$$

where θ_R is a constant called the thermal resistance and ΔT is the temperature of the element at the surface minus the temperature of the infinite substrate far from the surface. Comparison of Eqs. 8.6 and 8.5 shows that $\theta_R = \Delta z / KA$, where z is to be chosen so that $\Delta T / \Delta z$ is the proper temperature gradient. However, in a time dependent situation, there is no single Δx that will provide the correct temperature gradient for all times, so that Eq. 8.6 is incapable of properly describing the heat transfer to the substrate.

AD-A086 345

AUBURN UNIV ALA DEPT OF PHYSICS

F/G 9/1

SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)

MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAAG29-78-G-0111

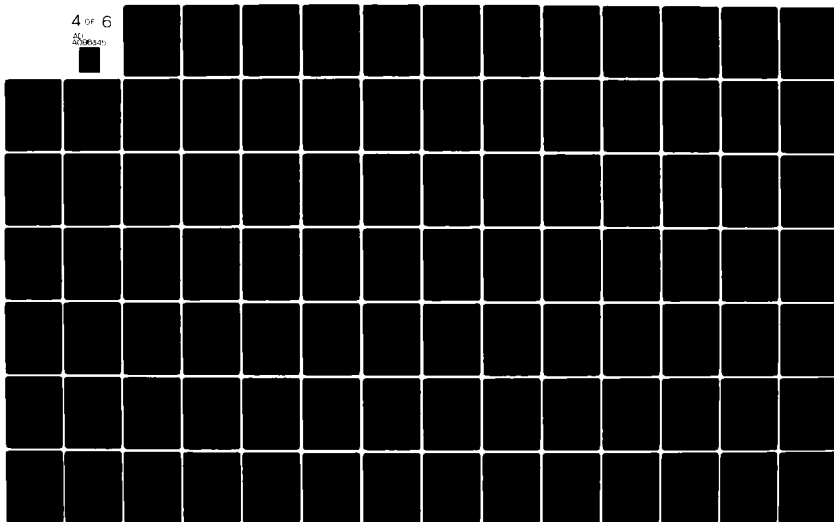
ARO-15840.3-A-EL

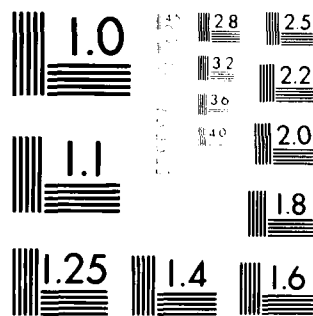
NL

UNCLASSIFIED

4 of 6

AV
ADDRESS





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Carslaw and Jaeger⁸¹ have discussed the problem of linear heat flow into a semi-infinite solid when the surface temperature is a known function of time ($\phi(t)$) and the interior is initially at temperature $T = 0$. The assumption is made here that the direction of heat flow within the substrate is perpendicular to the diode surface at each segment and that heat transfer can be described by the one-dimensional heat conduction equation,

$$\frac{\partial T}{\partial t} = x(T) \frac{\partial^2 T}{\partial z^2} \quad (8.7)$$

where x is the thermal diffusivity.

The spatial dependence of the thermal diffusivity is not included in Eq. 8.7. However, the temperature dependence of the thermal diffusivity, taken from Ref. 82 and shown graphically in Fig. 96, is incorporated in the computer program. Equation 8.7, with the boundary conditions given in Eq. 8.8, determines the temperature profile in the substrate beneath each segment at each instant.

$$\begin{aligned} \text{At time } t = 0, T &= 0 \text{ for all } z > 0 \\ \text{and } T &= \phi(t) \text{ at } z = 0 \end{aligned} \quad (8.8)$$

Notice that T is the temperature measured with respect to that of the substrate at $t = 0$. T will be referred to as the "relative temperature". The solution to the above equation (Ref. 83) in the interior is

$$T = \int_0^t \phi(\lambda) \frac{\partial}{\partial t} F(z, t-\lambda) d\lambda,$$

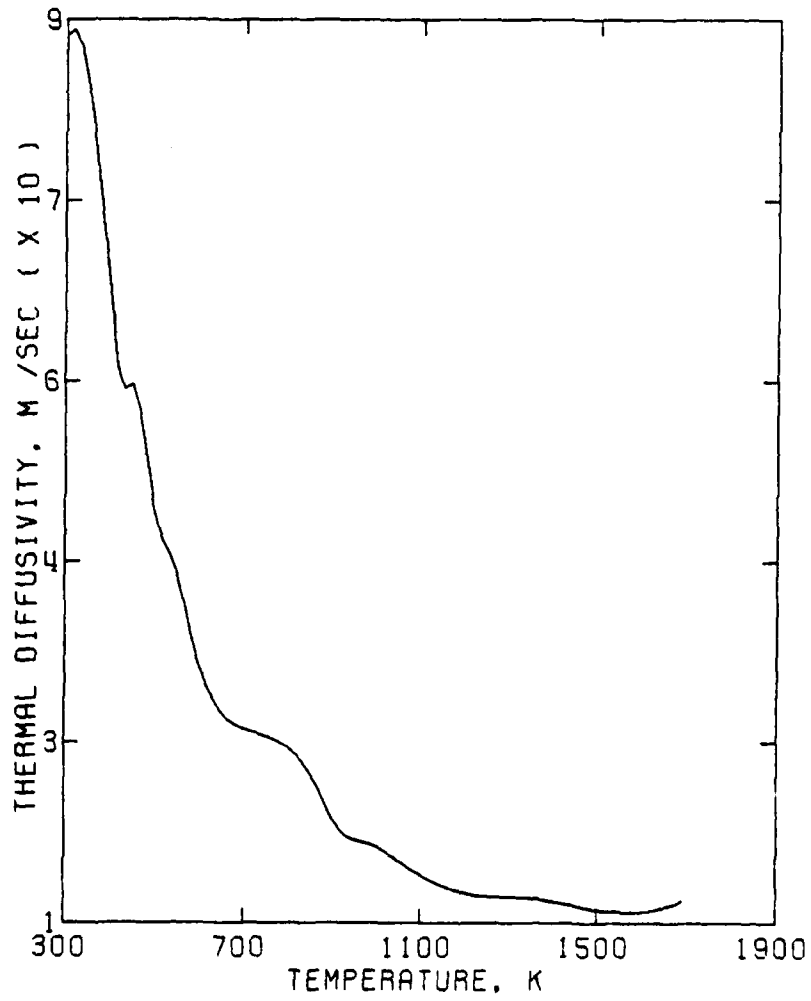


Fig. 96. Thermal diffusivity of sapphire as a function of temperature. (Ref. 77)

where

$$F(z, t-\lambda) = \frac{2}{\pi^{1/2}} \int_{\xi_0}^{\infty} e^{-\xi^2} d\xi$$

and

$$\xi_0 = (z/2) [\chi(t-\lambda)]^{-1/2}.$$

In this case

$$\frac{\partial}{\partial t} F(z, t-\lambda) = \frac{z}{2 (\chi(t-\lambda)^3)^{1/2}} \exp(-z^2/(4(t-\lambda)))$$

The expression for T becomes

$$T = \frac{z}{2(\chi\pi)^{1/2}} \int_0^t \phi(\lambda) \frac{\exp\left[-\frac{z^2}{4(t-\lambda)}\right]}{(t-\lambda)^{3/2}} d\lambda$$

Putting

$$\frac{z}{2[\chi(t-\lambda)]^{1/2}} = \mu,$$

we have

$$t-\lambda = \frac{z^2}{4\chi\mu^2}$$

and

$$T = 2\pi^{-1/2} \int_{\mu_0}^{\infty} \left(t - \frac{z^2}{4\mu^2}\right) \exp(-\mu^2) d\mu \quad (8.9)$$

where

$$\mu_0 = (z/2) (\chi t)^{-1/2}$$

In the electrothermal problem, the function $\phi_{jk}(t)$ is different for each segment and is determined for each segment only as the solution develops. Further, the shape of this function is different for different segments. However, the storage of $\phi_{jk}(t)$ for each segment and subsequent evaluation of the temperature gradient at the surface

increases substantially the memory requirements and greatly increases the computation time of the program. In the present computer program, the device has been divided into segments that form a 51×9 , two-dimensional, double precision array. Thus, for a pulse of $10 \mu\text{s}$ duration and time step of 10^{-8} s, determination of $\phi_{jk}(t)$ exactly for each segment at every time step requires storage of 1000 additional 51×9 arrays. On-line disk storage of such a large number of arrays alone would require about 3.6 Mb of computer memory as opposed to the 256Kb actually used. Likewise, computation time would be considerably increased due to the additional numerical integrations that would have to be performed on each segment at each time step. Thus, an approximation scheme has been developed for evaluating $\phi_{j,k}(t)$.

The functional form for $\phi_{jk}(t)$ will be assumed to be the same for all segments and all times. The function $\phi_{jk}(t)$ used at time step n ($n=\text{integer}$) is,

$$t < 0 \quad \phi_{jk,n}(t) = 0 \quad (8.10)$$

$$0 < t < n \quad \phi_{jk,n}(t) = (b_{jk,n})t$$

where $b_{jk,n}$ is chosen differently for each segment and each time interval (see Fig. 97). Time dependence of the temperature function $\phi_{jk,n}(t)$ is quite complex and has to be approximated if solutions are to be obtained within reasonable CPU time and with modest core usage. The linear dependence is chosen because of its ability to approximate both the gradual rise and gradual fall of segment temperatures by an equivalent change in the slope $b_{jk,n}$ of the $\phi_{jk}(t)$ - t curve. This is

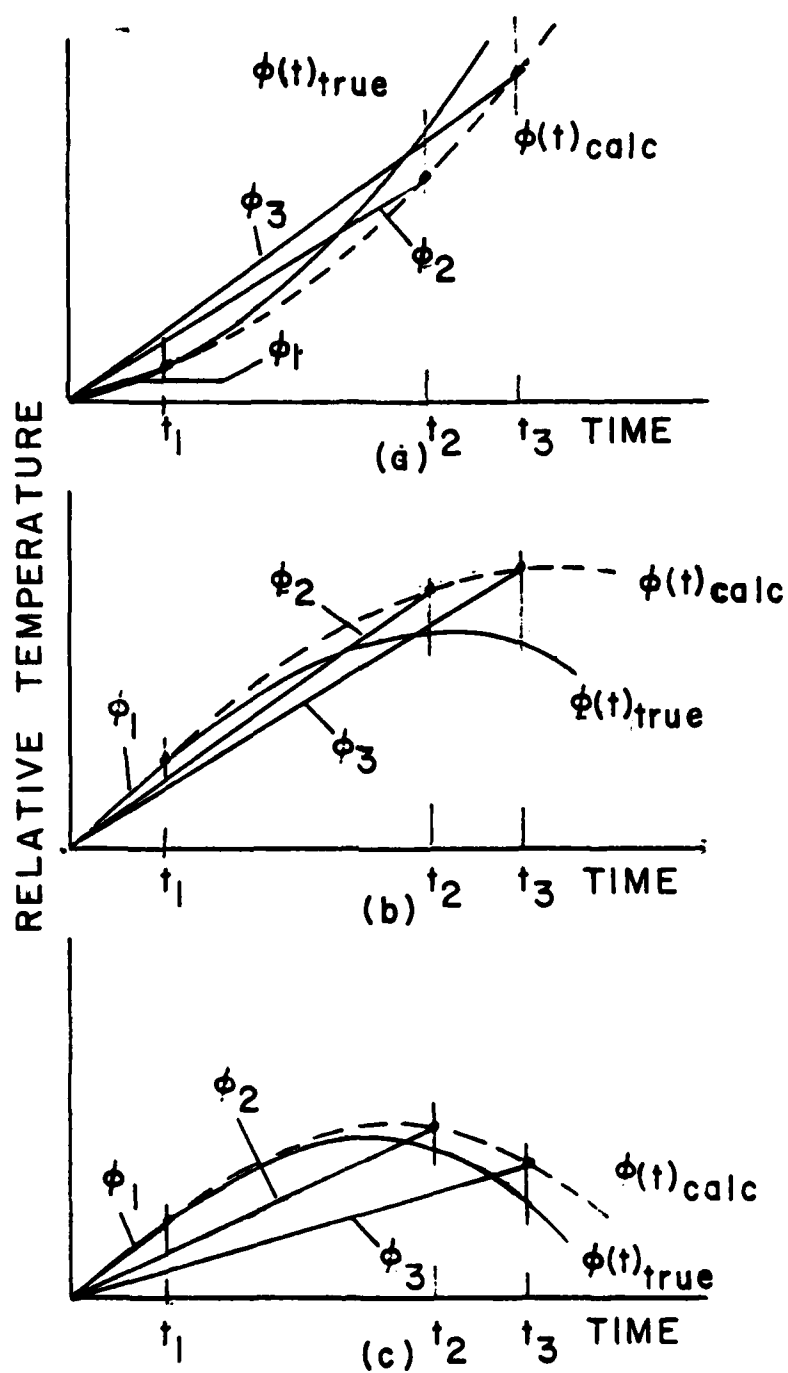


Fig. 97. Schematic diagrams to show the effect of the linear approximation to $\phi(t)$ in the n regions of current strips at (a) a filament site, (b) an intermediate strip, and (c) a strip near the edge. The true $\phi(t)$ is labelled $\phi(t)_{\text{true}}$, while the surface temperature calculated in the course of the solution is labelled $\phi(t)_{\text{calc}}$. The linear functions, $\phi_1 = b_1 t$, $\phi_2 = b_2 t$, and $\phi_3 = b_3 t$, are the approximations used at times t_1 , t_2 and t_3 , respectively.

illustrated in Fig. 97 for two segments, jk and $j'k'$. The temperature of segment jk increases with time while the temperature of $j'k'$ increases and then decreases. The different approximate functions are shown graphically. The slope $b_{jk,n}$ is selected for segment j,k at time $n\tau$ by the expression

$$b_{jk,n} = \frac{T_{jk,n} - T_{\infty}}{n\tau} \quad (8.11)$$

where τ is the size of the time interval employed in the solution, n is the number of the particular time interval, $T_{jk,n}$ is the temperature at time $n\tau$ of segment j,k , and T_{∞} is the relative substrate temperature deep inside the semi-infinite substrate. Then the surface temperature will have the form

$$\phi_{jk,n}(t) = (b_{jk,n})t = \frac{(T_{jk,n} - T_{\infty})}{n\tau}t \quad (8.12)$$

Thus, if $\phi(t)$ is chosen to be a linear function of time, then an analytical expression can be obtained for the temperature gradient and Eq. 8.9 becomes, for $\phi(t) = bt$

$$\begin{aligned} T &= \phi(t) \left\{ \left(1 + \frac{z^2}{2\chi t}\right) \operatorname{erfc} \frac{z}{2(\chi t)^{1/2}} - \frac{z}{(\pi \chi t)^{1/2}} \exp\left(-\frac{z^2}{4\chi t}\right) \right\} \\ &= 4\phi(t) i^2 \operatorname{erfc} \frac{z}{(4\chi t)^{1/2}} \\ &= 4bt i^2 \operatorname{erfc} \frac{z}{(4\chi t)^{1/2}} \end{aligned} \quad (8.13)$$

where

$$\operatorname{erfc} w = 1 - \operatorname{erf} w$$

$$i^2 \operatorname{erf} w = \frac{1}{4} [(1 - \operatorname{erf} w) - 2w(\frac{1}{\pi^{1/2}} e^{-w^2} - w + w \operatorname{erf} w)]$$

$$\operatorname{erf} w = \frac{2}{\pi^{1/2}} \int_0^w e^{-\zeta^2} d\zeta$$

The derivative of Eq. 8.13 with respect to z when evaluated at $z = 0$ gives the desired temperature gradient for computing the substrate heat transfer. Thus, for a particular segment j,k ,

$$\left. \frac{(dT)}{dz} \right|_{s;j,k} \bigg|_{z=0} = - \frac{2\phi_{jk}(t)}{(\pi \chi t)^{1/2}} \quad (8.14)$$

On close inspection of Eq. 8.12, it will be apparent that a predicament exists in the actual determination of the temperature function $\phi_{jk}(t)$. At time step n , $T_{jk,n}$ is known from the previous computing cycle. To determine $T_{jk,n+1}$ at the time step $n+1$ requires evaluation of the heat transfer terms during the time interval n to $n+1$. These terms require the temperature gradients during the n to $n+1$ time interval. A two-step procedure was developed for approximating $b_{jk,n}$ and for determining the temperature distribution from the previous temperature distribution and new current distribution. This procedure will now be given. To obtain the thermal solution at time $(n+1)\tau$, it is assumed that the electrical solution and temperature distribution are known at time $n\tau$. An approximation to the temperature change during time interval $(n+1)\tau - n\tau$ is obtained for each diode segment by using Eq. 8.3 with the current obtained in time step $n\tau$ and the temperatures of that time step. This is used to compute an approximate temperature change for each element, as indicated in Eq. 8.15.

$$\begin{aligned}
c_{j,k} m_{j,k} \Delta T'_{j,k} &= \Delta Q'_{j,k} \\
&= I_j^2 R_{j,k} \tau + \Delta Q_{s;j,k} + \Delta Q_{j,k+1;j,k} \\
&\quad + \Delta Q_{j,k-1;j,k} + \Delta Q_{j+1,k;j,k} + \Delta Q_{j-1,k;j,k}
\end{aligned} \tag{8.15}$$

$$\Delta T'_{j,k} = \frac{\Delta Q'_{j,k}}{c_{j,k} m_{j,k}} \tag{8.15a}$$

From this, a revised temperature is estimated for each element

$$T'_{jk,n+1} = T_{jk,n} + \Delta T'_{j,k} \tag{8.16}$$

The new time dependent relative temperature at the surface $\phi_{j,k;n+1}$ is calculated next

$$\phi_{jk,n+1}(t) = b_{jk,n+1} t \tag{8.17}$$

where

$$b_{jk,n+1} = \frac{T'_{jk,n+1} - T_{\infty}}{(n+1)\tau}$$

Then from Eqs. 8.17, 8.14 and 8.5a, the substrate heating term at the time $(n+1)\tau$ takes on the form given below

$$(\Delta Q_{s;j,k})_{n+1} = -2 K_{sa}(T) A_{s;j,k} \frac{(T'_{jk,n+1} - T_{\infty})t}{(\pi \chi t)^{1/2} (n+1)\tau} \tag{8.18}$$

The approximate temperatures $T'_{jk,n+1}$ for each segment as obtained with Eq. 8.16 are used in Eq. 8.3 for evaluating the lateral heat transfer terms. Thus, Eq. 8.3 yields for each j,k element a new $\Delta T_{j,k}$. The temperature of the j,k element at time $(n+1)\tau$ is taken to be $T_{jk,n+1} = T_{jk,n} + \Delta T_{j,k}$. Once the temperature distribution at time

$(n+1)\tau$ is known, the system parameters at this temperature can be calculated and the new current distribution obtained.

D. Computational Procedure

A set of initial conditions is selected: doping density of the n region, current amplitude, number of longitudinal strips, initial temperature, length of the time increments and the pulse duration. For devices free of junction spikes, the current at first divides evenly among the longitudinal strips because all strips have the same properties. The voltage across the diode is, by Eq. 8.2, the sum of the incremental voltages across each portion of a single strip. Once the strip currents and incremental voltages are determined, Eq. 8.3 is used to determine the temperature rise in each element. The new temperature of each element is the old temperature plus the temperature change. Using this temperature and the known resistance-temperature relation, the new resistance is computed.

The new temperatures are not uniform over the diode because of the boundary condition at the diode edge (edge temperature equals that of the substrate) and the high temperature produced by the avalanching (reverse bias assumed) diode in the junction region. Thus the current distribution will no longer be uniform and an iterative procedure is required to determine how the current is distributed after the first time increment has passed. This cannot be accomplished analytically because the junction voltage not only depends on the junction temperature but also on the junction current density. Thus, a trial current distribution is first assumed. This distribution is chosen to be the

same as the previous distribution. Each strip voltage is then computed. These will differ slightly from each other because the trial distribution is not correct for the new circuit parameters. The new distribution is arrived at by the iterative procedure listed below as part B of the computer program. Generally, the number of trial solutions is around 10. The new temperatures are then computed and the process repeated.

Computations for a particular simulation run were terminated if device terminal voltage dropped suddenly and remained at a low level (signifying completion of filamentation) if computation became meaningless due to lack of convergence, or if the temperature in any portion of the device reached 1685 K, the melting point of silicon. The structure of the computer program follows.

A. Parameter specification

1. Initialize all constants and parameters.
2. Specify the size of the spatial mesh.
3. Set the temperature, $T(J,K)$, of all elements to the substrate temperature (300 K in the present work).

B. Solution of electrical problem assuming step current input

1. Calculate the resistance $R(J,K)$ at $T(J,K)$ for each element (all J,K) and the total resistance, $STPRS(J)$, for every strip (all J).
2. Calculate the junction voltage, $VJN(J)$, for every J using the known temperatures and trial currents.

3. Compute the terminal voltage, $V(J)$, for every J

$$V(J) = VJN(J) + I(J)*STPRS(J),$$

where $I(J)$ is the strip current. The $V(J)$ will not, in general, be equal because the assumed current distribution is, in general, incorrect.

4. Obtain an estimate of the device terminal voltage, $VTOT$ (see Eqs. 8.1, 8.2)

$$VTOT = \left\{ ITOT + \sum_J VJN(J)/STPRS(J) \right\} / \sum_J (1/STPRS(J)),$$

where $ITOT$ is the excitation pulse amplitude.

Start Iteration Loop

5. Calculate the new $I(J)$ using the new $VTOT$ and the old $VJN(J)$

$$I(J) = (VTOT - VJN(J))/STPRS(J)$$

6. Calculate the new $VJN(J)$ using the new $I(J)$

$$VJN(J) = f(I(J), ND, T(J, K))$$

7. Calculate the new $V(J)$ using the new $VJN(J)$ and $I(J)$

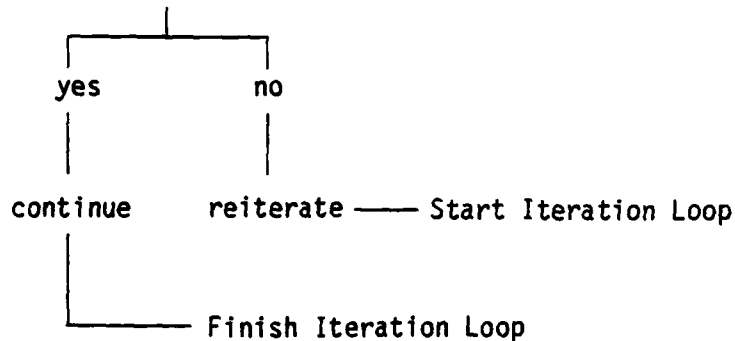
$$V(J) = I(J)*STPRS(J) + VJN(J)$$

8. Calculate
 - a. sum of all $I(J)$, $CITOT$

b. $VTOT$

Test a. $ABS(V(J) - VTOT) < \delta_1$ for all J

b. $ABS(CITOT - ITOT) < \delta_2$



C. Determine new temperature distribution

1. Calculate the changes in temperature due to electrical and thermal processes

(a) Determine approximate change in energy $\Delta Q'(J,K)$ and hence $\Delta T'(J,K)$ from the known current, known temperature distribution, and known substrate heat flow term of the previous time interval.

(b) Obtain an intermediate temperature distribution $T'(J,K) = T(J,K) + \Delta T'(J,K)$ for the purpose of determining substrate heat flow term for the present time interval.

(c) Calculate the change in energy $\Delta Q(J,K)$ for the present time as all terms in Eq. 8.3 are now known. Then,

$$\Delta T(J,K) = (\Delta Q(J,K)) / (\text{segment mass} * \text{specific heat capacity of silicon})$$

where $\Delta Q(J,K)$ = heat gained from surrounding segments -
heat lost to the substrate + Joule heating due to current.

2. Calculate new temperature, $T(J,K)$, for every element J,K

$$T(J,K) = T(J,K) + \Delta T(J,K)$$

Write Results of Present Time Step

$$\text{Time} = \text{Time} + \text{Tau}$$

Go Back to Start of Time Increment Loop (step B)

The SOS diode considered was 204 μm wide, 350 μm long and had a silicon film thickness of 0.6 μm . The geometry and dimensions used for calculations were chosen to be similar to those of devices being studied experimentally (see Part I). The n region was 30 μm long and contained 51 longitudinal strips, each 4 μm in width. Each longitudinal strip was further divided into 9 segments. The two in the p+ and n+ regions were 160 μm long. The width of the n depletion region was set according to the results of the J-V-T calculations, and the remaining portion of the n-region was divided into six equal segments (each about 4 μm long).

The SOS diodes were subjected to constant current pulses of 8 to 12 mA amplitude and 1 to 15 μs duration. Average current densities ranged from 6×10^7 to 9×10^7 A/m². These current densities led to current densities during filamentation in excess of 10^9 A/m².

All programs associated with this section were written in FORTRAN IV and, on an average, took about 7 minutes of CPU time for every microsecond of pulse length. In all cases, the required memory usage for the IBM 370/158 machine was less than 256K.

IX. PN JUNCTION J-V-T CHARACTERISTICS UNDER REVERSE BIAS AND HIGH CURRENT DENSITIES

The second breakdown problem involves the junction at unusually high current densities and unusually high temperatures. In the course of second breakdown the current density at the site of the damage filament may increase from about 10^7 A/m² to 10^9 A/m² as the junction temperature goes from 300 K to 1685 K, the melting point of silicon. Questions arise on the temperature dependences of the avalanche coefficients, saturation velocities of holes and electrons, carrier lifetimes, mobilities and other parameters. As temperature rises, thermally generated carriers entering the junction become increasingly significant and, at sufficiently high temperatures, the junction voltage drops toward zero at all current densities. The role of thermal effects, however, is quantitatively different depending upon the current density. High current densities imply higher voltages and greater depletion widths. The role of current density, in turn, depends upon the velocity of the carriers within the junction region. If this velocity is small, current density modifies the space charge distribution. Further, this effect occurs at lower current densities when the doping level in the n-region is low.

Other investigators have computed J-V-T characteristics of pn junctions at various current densities, n-region doping densities and bulk temperatures. Causey and Rayburn⁷⁹ simulated time dependent thermal breakdown conditions in silicon pn junctions with n-region doping density

of 10^{23} atoms/ m^3 . The device was driven by a constant current source of strength 10^5 A/ m^2 in a reverse bias mode. In their simulation, junction temperatures up to 700 K were obtained. A theoretical study of pn junction behavior made by Sze⁸⁴, yielded J-V-T characteristics at low current densities of 10^5 A/ m^2 and at temperatures up to 500 K. More recently, Ward⁸⁵ did extensive numerical calculations of temperature-dependent static characteristics for a p^+n diode with 3×10^{21} atoms/ m^3 as the doping concentration of the n-region. Computations were also made on SOS diodes with n-region doping density of 8×10^{22} atoms/ m^3 and temperatures of 300-650 K. Behavior of reverse biased p^+-n-n^+ junctions subjected to short duration high current pulses have been analyzed by Neudeck.⁸⁶

Junction characteristics are calculated in the present study because junction J-V-T characteristics are not presented elsewhere over the broad ranges of temperature, current density, and n-region doping needed for the second breakdown problem.

A. Equations for the Abrupt, Reverse Biased $p^+ - n$ Junction

The size of the space-charge region of a p^+n junction depends on the concentrations of uncompensated donors and acceptors and the strength of the applied electric field. The junction region is a distributed electric dipole in an otherwise neutral system. The space charge in the p^+ region (doping density about 10^{26} atoms/ m^3) is concentrated in an extremely narrow negative layer (10^{-4} μm thick) adjoining the junction. On the other hand, the space charge region in the more lightly doped n-region may extend for many micrometers from the

metallurgical junction. Thus the behavior of an abrupt p^+n junction is determined by its n -region. At high current densities, the charge on the carriers can appreciably modify the space charge distribution within the junction. The coordinate system origin is taken to be the edge of the depletion region on the n -side and the metallurgical junction is located at $x = +w$, where w is the width of the depletion layer in the n region.

The junction behavior for a one-dimensional pn junction under reverse bias is determined by the following equations.⁷²

Poisson's equation in one-dimension:

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} = \frac{q}{\epsilon} (p - n + N_D - N_A) \quad (9.1)$$

where

- E x -component of the electric field
- x space coordinate
- ρ total charge density
- ϵ dielectric permittivity
- q magnitude of the electronic charge
- p density of holes
- n density of electrons
- N_D density of ionized donors
- N_A density of ionized acceptors

Continuity equations (including thermal generation, recombination and avalanche generation):

$$\frac{dJ_n}{dx} = U - G \quad (9.2)$$

$$\frac{dJ_p}{dx} = G - U \quad (9.3)$$

where

J_n electron current density

J_p hole current density

U thermal rate of generation and recombination of electron-hole pairs

G avalanche rate of generation of hole-electron pairs

The functions J_n , J_p , U and G are taken to be

$$J_n = q|v_n|n + qD_n \frac{dn}{dx} = q|v_n|n \quad (9.4)$$

$$J_p = q|v_p|p - qD_p \frac{dp}{dx} = q|v_p|p \quad (9.5)$$

$$U = \frac{q(n_i^2 - np)}{(p+n_i)\tau_n + (n+n_i)\tau_p} \quad (9.6)$$

$$G = q[\alpha_n |v_n|n + \alpha_p |v_p|p] \quad (9.7)$$

where

v_n average speed of electrons in a field E

v_p average speed of holes in a field E

D_n electron diffusion constant ($= (kT/q)\mu_n$: Einstein Relation)

D_p hole diffusion constant ($= (kT/q)\mu_p$: Einstein Relation)

k Boltzmann's constant

μ_p hole mobility

μ_n electron mobility

$\frac{dn}{dx}$	electron density gradient
$\frac{dp}{dx}$	hole density gradient
n_i	intrinsic equilibrium carrier density at temperature T
τ_n	lifetime of excess electrons in the n-region
τ_p	lifetime of excess holes in the n-region
α_n	avalanche coefficient for the generation of electron-hole pairs by an incident electron
α_p	avalanche coefficient for the generation of electron-hole pairs by an incident hole

Carrier densities in the junction region become non-uniform at high current densities and this gives rise to gradients in electron and hole current densities and, hence, diffusion currents. These diffusion currents are neglected in Eq. 9.4 and 9.5 because, at the high fields where appreciable gradients of charge density exist, the electric field terms still dominate the diffusion terms. Thus in numerical calculations of the drift and the diffusion terms at a current density of 10^8 A/m², the diffusion terms of Eq. 9.4 and 9.5 were smaller by two orders of magnitude compared to the electric field terms. The current densities, J_p and J_n , combine to give the total current density J , that is,

$$J = J_p + J_n \quad (9.8)$$

The particle velocities and avalanche coefficients are functions of both electric field and temperature. At low electric fields, the carrier velocity in the depletion region of a pn junction is dictated primarily by the semiconductor lattice temperature. The field imparts kinetic energy to the carriers, and they, in turn, transfer it to the

lattice atoms through collision. At low fields the drift velocity of the carriers is insignificant compared to the mean thermal velocity, but at high fields, the drift velocity becomes comparable to the thermal velocity. Also at high electric fields, scattering of electrons by optical phonons limits the drift speed of carriers. This limiting (saturation) speed at 300 K is about 1×10^5 m/s for electrons and 7×10^4 m/s for holes.³⁸ At fields above 10^7 V/m, electron and hole multiplication can occur but the average speeds appear to be the saturation speeds. Both the mobilities and saturation speeds are temperature dependent. The doping level and field dependences of the electron and hole mobilities have been described in an empirical equation by Scharfetter and Gummel⁵⁷. Equation 9.9 is their expression, modified to include a temperature factor (see p. 39, Ref. 84).

$$\mu_p(T, N_D, E) = \frac{\mu_0 \left(\frac{300}{T} \right)^n}{\left\{ 1 + \frac{N_D}{N_D/S + N} + \frac{(E/A)^2}{E/A + F} + (E/B)^2 \right\}^{1/2}} \quad (9.9)$$

The parameters in Eq. 4.9 (in SI units) for electron and hole mobilities are given in Table 13.

	μ_o ($\frac{m^2}{V-s}$)	S (dimensionless)	N (m^{-3})	A (V/m)	F (dimensionless)	B (V/m)	n (dimensionless)
Holes	.048	81	4×10^{22}	6.1×10^5	1.6	2.5×10^6	2.7
Electrons	.1400	350	3×10^{22}	3.5×10^5	8.8	7.4×10^5	2.5

Table 13. Parameters from Eq. 9.9 in SI units.

Sze (Ref. 84, pp. 39, 40, 57) offers a somewhat different expression

$$\mu(T, N_D, E) = \frac{\mu_o \left(\frac{300}{T} \right)^n}{\left[1/2 \left(1 + \left\{ 1 + \frac{3\pi}{8} \left[\frac{\mu_o \left(\frac{300}{T} \right)^n E}{C_s} \right]^2 \right\}^{1/2} \right)^{1/2} \right]} \quad (9.10)$$

where (in SI units) the parameters for holes and electrons are given in Table 14. C_s is the speed of sound.

	μ_o ($m^2/(V-s)$)	C_s (m/s)	n (dimensionless)	v_s (m/s)
Holes	$0.3284 - .01283 \log_{10} N_D$	9.03×10^3	2.7	0.75×10^5
Electrons	$0.8956 - .03594 \log_{10} N_D$	9.03×10^3	2.5	1.05×10^5

Table 14. Parameters for Eqs. 9.10 - 9.13 in SI units.

Equations 9.9 and 9.10 can be used to compute the carrier drift velocities, v_n and v_p , at fields less than those that produce velocity saturation. That is,

$$v_p = \mu_p E \quad (9.11a)$$

$$v_n = -\mu_n E \quad (9.11b)$$

The temperature dependences of the saturation velocities⁸⁷ are given by

$$v_p = v_{sp} (300/T)^{1/2} \quad (9.12a)$$

$$v_n = v_{sn} (300/T)^{1/2} \quad (9.12b)$$

If Eqs. 9.09 or 9.10 are used in Eqs. 9.11, and the velocities in Eqs. 9.11 equated to the corresponding velocities in Eqs. 9.12, then the electric fields can be determined (for each carrier temperature and doping level) at which the saturation velocities are reached. Both Eq. 9.9 and 9.10 are approximate expressions developed for systems having temperatures close to room temperature. They are applied in the present work over a broad temperature range because of lack of better expressions. They give similar results and both have been used at different phases of the present study. For the high field case, Eq. 9.10 is easier to work with than Eq. 9.9. The field at the saturation threshold using Eq. 9.10 is

$$E_{sat} = \frac{v_s^2}{4C_s \mu_o} \left(\frac{3\pi}{2} \right)^{1/2} \left(\frac{300}{T} \right)^{1-n} \quad (9.13)$$

Values of the constants of Eq. 9.13 for holes and for elections are given in Table 14. For fields up to (E_{sat}) for holes, the hole drift velocity, is given by Eq. 9.11a. For fields in excess of E_{sat} for holes, the hole drift velocity is given by Eq. 9.12a. Similarly, Eq. 9.11b and 9.12b give the electron drift velocity for fields less than

and greater, respectively, than E_{sat} for electrons. The field and temperature dependences of the electron and hole velocities are shown in Figs. 98 and 99, respectively, in Chapter X.

The lifetimes, τ_n and τ_p , were taken to be equal and constant³⁷, with

$$\tau_n = \tau_p = 1 \times 10^{-6} \text{ s}$$

This time is long compared to the transit time of about 10^{-11} s. In trial runs taken with $\tau_n = \tau_p = 1 \times 10^{-8}$ s, appreciable junction widening and rise of junction voltage occurred at high current densities.

The intrinsic carrier density n_i that appears in Eq. 9.6 is

$$n_i^2 = k_i T^3 \exp \left(- \frac{E_g}{kT} \right), \quad (9.14)$$

where

$$k_i = 1.5 \times 10^{45} \text{ m}^{-6} \text{ K}^{-3}.$$

The continuity equations employed, Eqs. 9.2 and 9.3, do not contain the time derivatives, $\frac{\partial n}{\partial t}$ and $\frac{\partial p}{\partial t}$. Thus, steady state solutions are obtained.

Eliminating J_p using Eq. 9.8, Eqs. 9.1 and 9.2 become

$$\frac{dE}{dx} = \frac{1}{\epsilon} \left(\frac{J}{v_p} + \frac{1}{v_n} - \frac{1}{v_p} \right) J_n + \frac{q}{\epsilon} (N_D - N_A) \quad (9.15)$$

$$\frac{dJ_n}{dx} = (\alpha_n - \alpha_p) J_n + \alpha_p J + U \quad (9.16)$$

$$\text{At the boundary } x = 0, J_{n0} = J - J_{p0}. \quad (9.17)$$

Equations 9.15 and 9.16 are then solved simultaneously to obtain the electric field, charge distribution, rate of avalanche generation, rate of thermal generation, and other features of the conduction process.

In reverse bias and moderate temperatures, the current in the junction is provided by carriers created by the avalanche mechanism.

The avalanches are initiated by minority carriers that enter the junction from both the p^+ and n regions. However, since $np=n_i^2$ for a semiconductor in thermal equilibrium, the n region is far more influential than the p^+ region in introducing minority carriers into the junction. For moderate temperatures, the junction characteristics are very insensitive to the size of the entering minority carrier current density J_{p0} from the n region. However, at elevated temperatures J_{p0} increases by orders of magnitude. At sufficiently high temperatures, J_{p0} becomes comparable to the total junction current, avalanche becomes less and less important, and the junction voltage drops. With further increase in temperature, $J_{p0} = J$, and the junction voltage drops to a small value limited by the resistance of the junction. The temperature dependence of J_{p0} is given in Eqs. 9.18-9.20.⁵⁷ Here J_{p0} includes both a field term and a diffusion term,

where

$$J_{p0}(T) = qE\mu_p(T)p_n(T) + q \left(\frac{D_p(T)}{\tau_p} \right)^{1/2} p_n(T) \quad (9.18)$$

$$D_p(T) = \frac{kT}{q} \mu_p(T) \quad (9.19)$$

$$p_n(T) = \frac{2n_i^2}{N_D} (1 + \sqrt{1 + 4(n_i/n_D)^2})^{-1} \quad (9.20)$$

The expression used for μ_p is that of Eq. 9.9.

The temperature and electric field dependences of the ionization coefficients are taken from Ref. 38.

$$\alpha = (1/\lambda) \exp(Ax^2 + Bx + C) \quad , \quad (9.21)$$

where the parameters are defined in Table 15.

TABLE 15

Parameters for Eq. 9.21

$$A = 11.5 r^2 - 1.17r + 3.9 \times 10^{-4}$$

$$B = 46 r^2 - 11.9r + 1.75 \times 10^{-2}$$

$$C = -757 r^2 + 75.5r - 1.92$$

$$r = \left(\frac{E_r}{E_i} \right) \tanh (E_r/2kT)$$

E_r = Energy of the Raman optical phonon (1.0×10^{-20} J)

$$E_i = 1.5 E_g$$

E_g = Band gap (1.77×10^{-19} J for silicon)

For α_n (electron ionization coefficient):

$$x_n = \frac{E_i}{qE \lambda_n} \quad n = \frac{E_i}{qE \lambda_n}$$

$$\lambda_n = 7.6 \times 10^{-9} \tanh \frac{E_r}{2kT}$$

For α_p (hole ionization coefficient):

$$x_p = \frac{E_i}{qE \lambda_p}$$

$$\lambda_p = 4.7 \times 10^{-9} \tanh \frac{E_r}{2kT}$$

B. Computational Strategy

Calculations were done on an IBM 370/158 machine using the fourth order Runge-Kutta double precision method of integration and CSMP3 as the main programming language. (Various other integration methods such as trapezoidal, Milne's, rectangular, STIFF and Simpson's were explored but Runge-Kutta seems to have yielded the most accurate results in the shortest time.) To solve the relevant differential equations

simultaneously, a particular starting value of each of the variables J , T , N_D and J_n was chosen. Integration was started at a point in the n region which was assumed to be the edge of the junction region. The field at this point is the same as that in the remainder of the n region. For a current density J , this boundary field is $E = J/\sigma$. Here σ is the conductivity of the n region. The minority carrier density at the edge of the junction in the n region is J_{p0} and the corresponding boundary value for use in Eqs. 9.15 and 9.16 is the J_{n0} identified in Eq. 9.17.

X. CALCULATED JVT CHARACTERISTICS UNDER REVERSE BIAS

A set of constitutive relations must be chosen before JVT characteristics can be calculated. In the course of the present work, certain decisions were made which were later regarded as inferior. However, the calculations of the electrothermal model were performed with the original JVT results and not sufficient time was available to rerun all of the situations. Fortunately, the method used gave adequate results up to about 500 K. But it contained a condition that forced the junction voltage to drop to its resistive limit at 800 K. Such a drop in voltage should occur at different temperatures, depending upon the current density. The peculiar shape of the JVT curves at the higher temperatures made us re-examine our procedures. This led to the following six program modifications:

1. The temperature dependence of the electrical conductivity in the n region outside the junction had been neglected. This temperature dependence was included in the modification, using the data from Runyan⁴⁵. This was a significant modification since it altered the computed value of the electric field in the n region and thereby the number of minority carriers drawn into the junction from the n region.
2. In the original calculation, the diffusion term for the minority carriers entering the junction was neglected. In the modification, this current is included with the field drift

current. The diffusion term becomes increasingly important as temperature rises. Not only does it become larger, but the field drift term becomes less significant (because the increase in electrical conductivity with temperature (at elevated temperatures) requires less field to sustain a particular current density in the n region).

3. The expressions originally used for the avalanche coefficients go to zero at 800 K. These equations were approximations to the theoretical results of Baraff⁹⁰ and should not have been used above about 500 K. The modified treatment uses another approximation, also based on Baraff's theory, that does not have the artificial cutoff (Eq. 9.21). This produces a very significant change in the JVT characteristics, since the junction voltage and junction width tend to go to infinity as the temperature approaches 800 K in the originally used expressions. The expressions used in the modification show a gradual decrease in the avalanche coefficients with rising temperature, and avalanche occurs above 800 K with no anomaly in the region about 800 K.
4. In the original calculation, the expression for the hole concentration in the n region was based on the assumption that the electron carrier density in this region was equal to the donor density. However, this is not a good assumption because of the rise in electron carrier density due to thermally induced band-to-band transitions. This significantly alters

the value of the minority carrier current introduced into the junction at elevated temperatures.

5. The original calculation assumed that the carriers were at their saturation velocities (taken as temperature dependent) when in the junction region. The modification includes both the field and temperature dependences of the carrier velocities.
6. The temperature dependence of the electron and hole mobilities at high temperatures do not seem to be well established. The theoretical discussion of Sze⁸⁴ was taken as the basis for using a different expression for the high temperature mobilities than had been used in the earlier calculations.

In the present chapter, the more recently calculated JVT characteristics are presented and discussed. These are believed to better represent the system than did the original calculations. However, since the electrothermal model calculations were based on the old JVT calculations, these are presented in Appendix A.

JVT characteristics were obtained under reverse bias for a doping density of 10^{22} atoms/m³, temperatures from 300 to 1300 K, and current densities from 10^4 to 10^8 A/m². Figures 98 to 102 show the temperature and field dependences for hole and electron velocities, n-region resistivity, carrier current density entering the junction from the n region, intrinsic carrier density, and the ionization coefficients.

Calculated JVT characteristics are shown in Fig. 103. For current densities up to 10^6 A/m² (Fig. 103a), there is an initial rise in voltage with increasing temperature that is associated with the

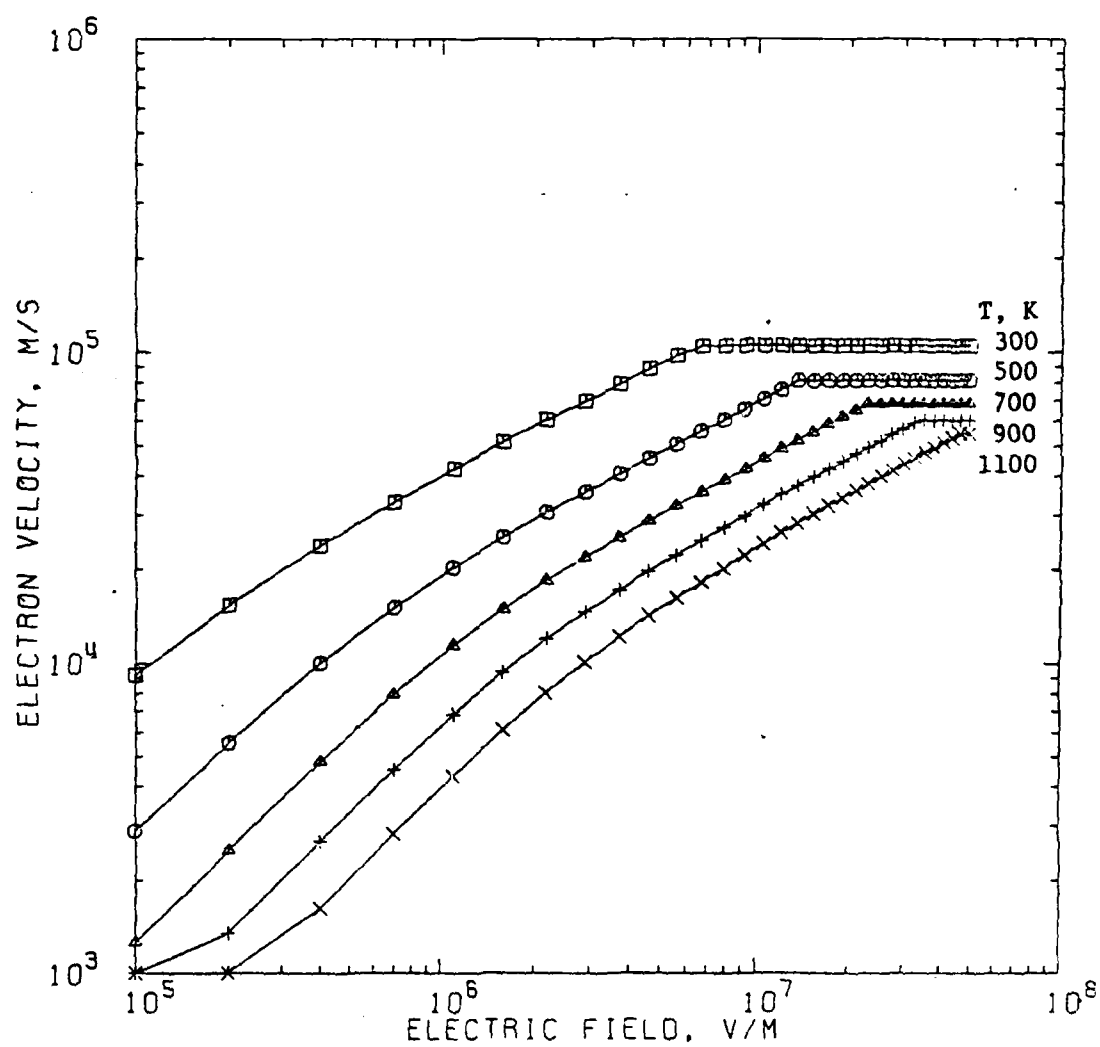


Fig. 98 . Electron velocity versus electric field at constant temperature.

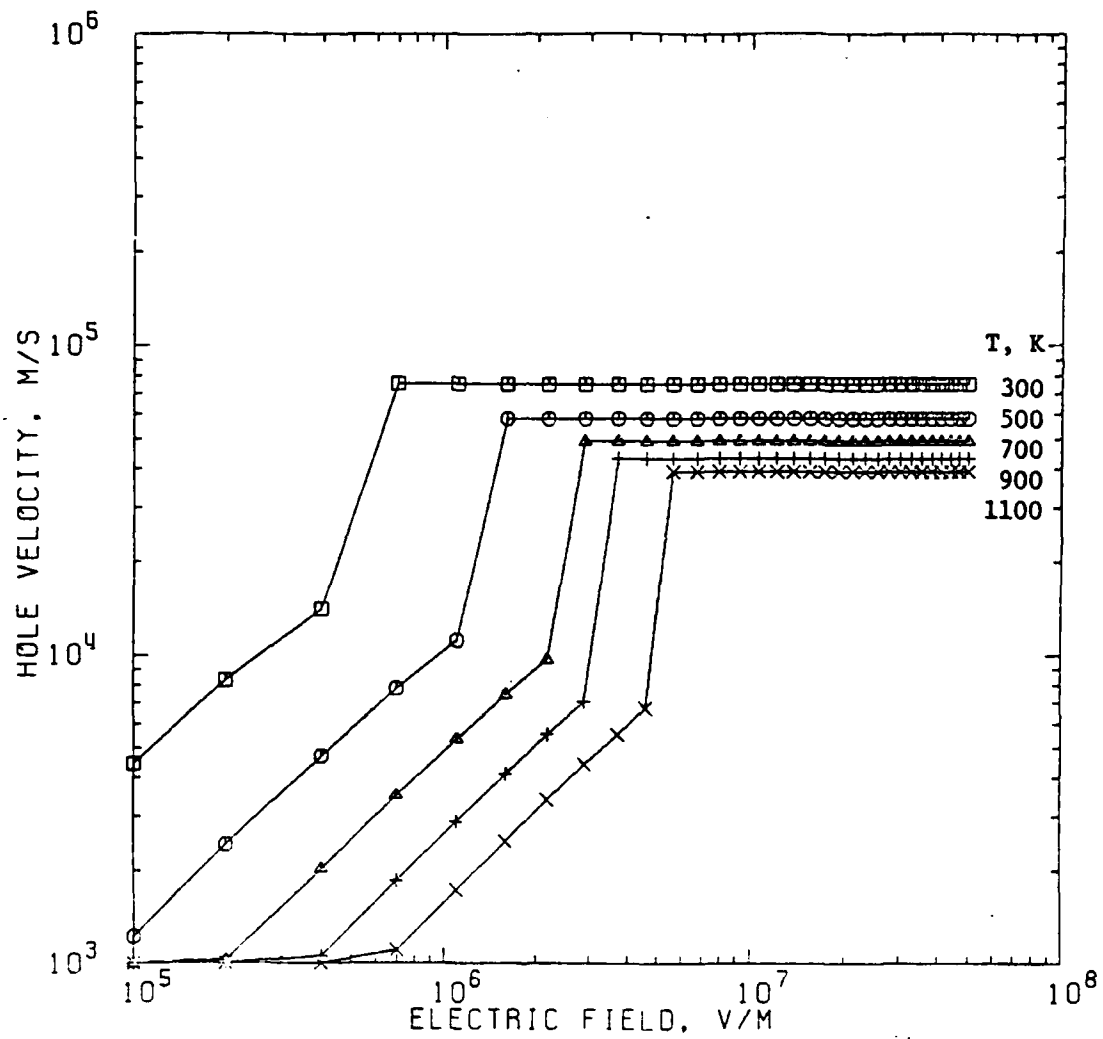


Fig. 99 . Hole velocity vs electric field at constant temperature.

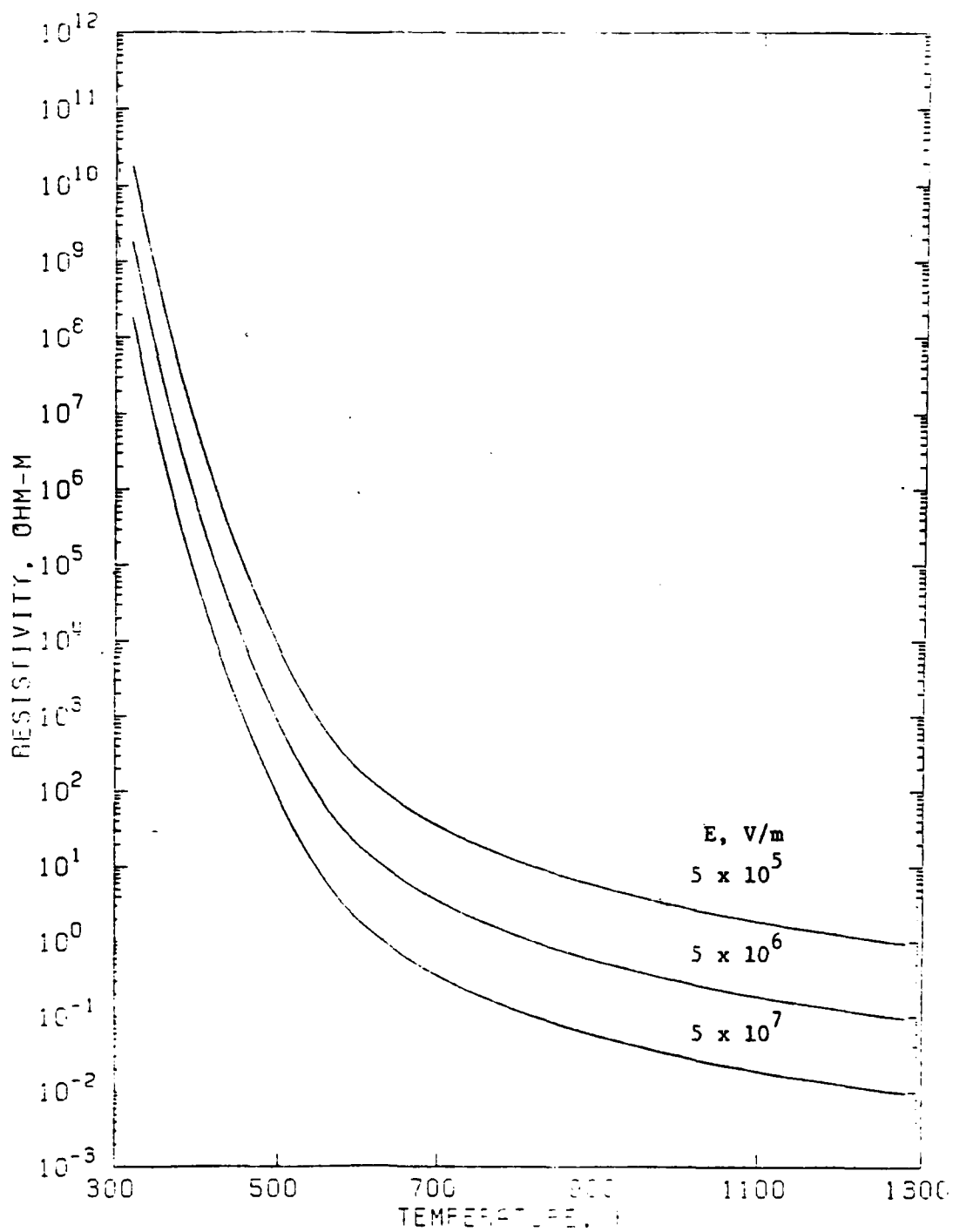


Fig. 100. Resistivity vs temperature at constant electric field.

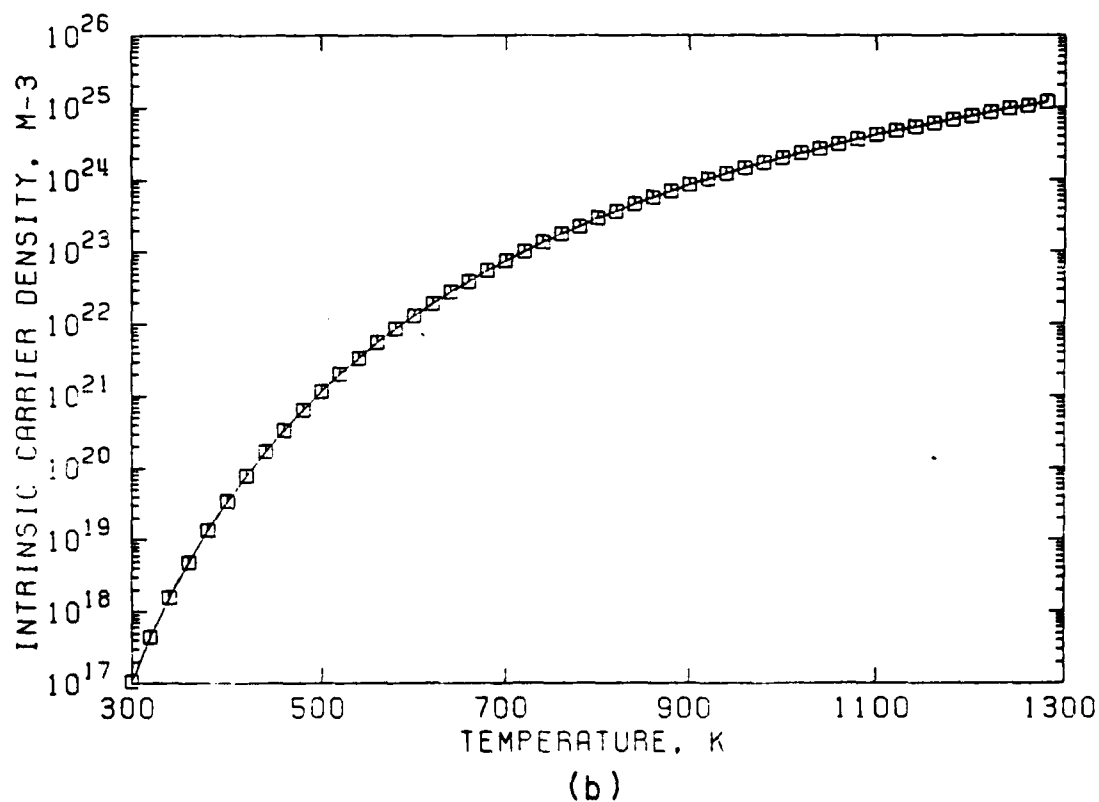
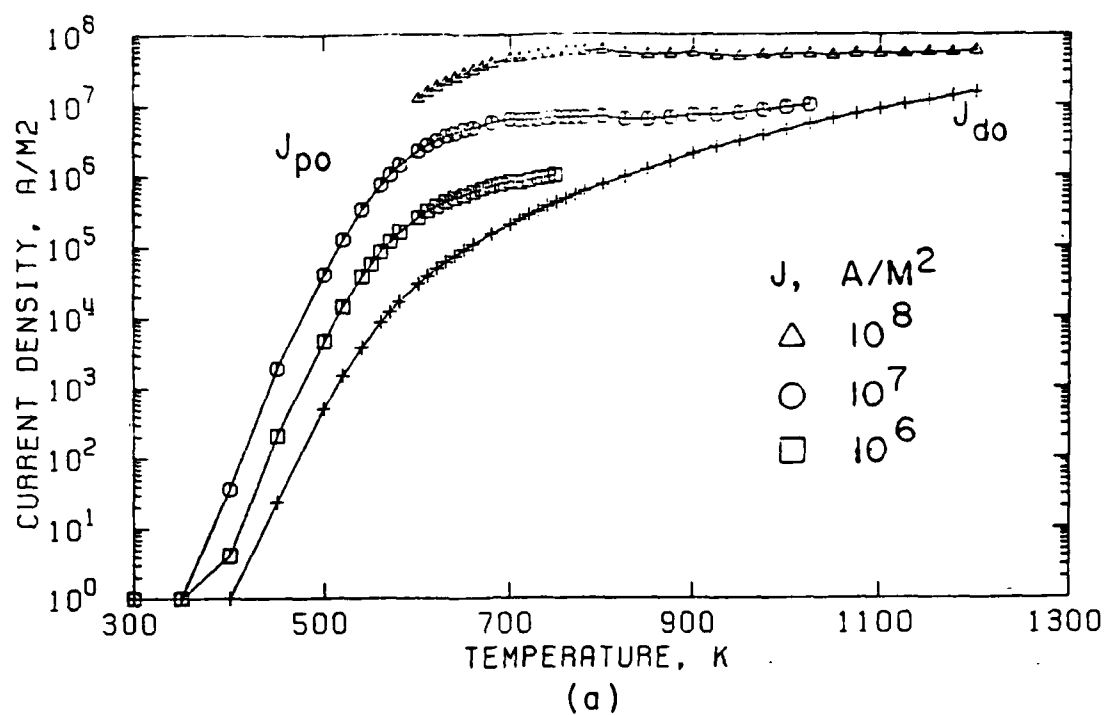
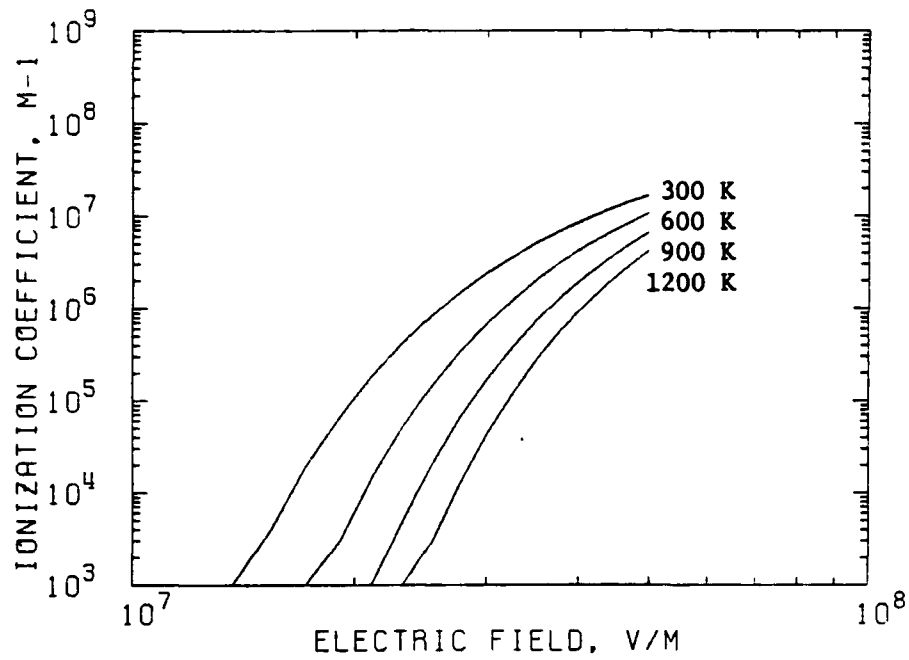
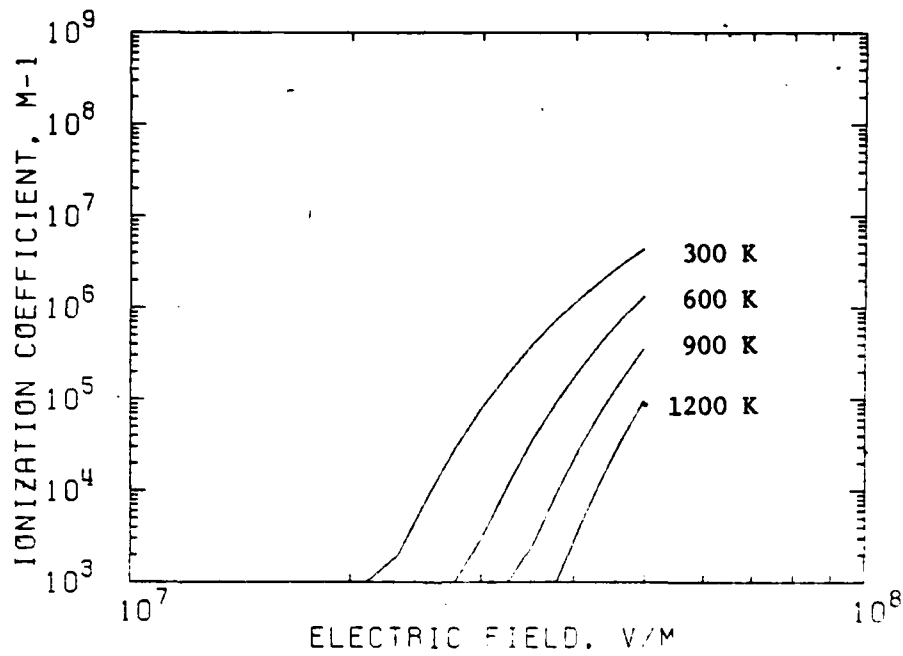


Fig. 101. (a) J_{po} vs temperature at constant J and J_{do} vs temperature. (b) Intrinsic carrier density vs temperature.

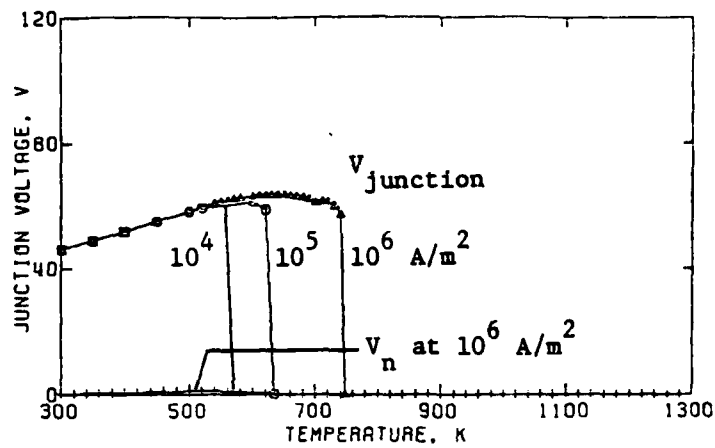


(a)

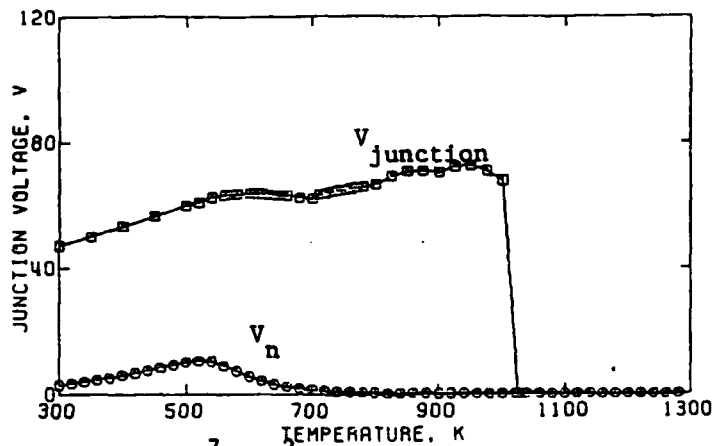


(b)

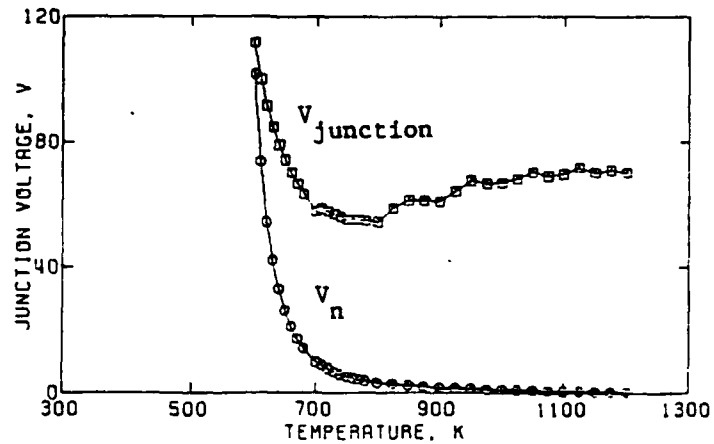
Fig. 102. Electron (a) and hole (b) ionization coefficients vs electric field for constant temperatures.



a. $J = 10^4, 10^5, 10^6 \text{ A/m}^2$.



b. $J = 10^7 \text{ A/m}^2$.



c. $J = 10^8 \text{ A/m}^2$.

Fig. 103. Voltage vs temperature at constant current densities for the junction and n region. The voltage V_n is developed across a strip in the n region having the width of the junction depletion region.

temperature dependences of the ionization coefficients. The drop in voltage in each case occurs as the density of thermally generated carriers entering the junction from the n region provides a current density that approaches that of the applied pulse.

The same general behavior is found when the current density is 10^7 A/m² (Fig. 103b), but in this case the temperature at which the voltage drops is found to be very sensitive to the n-region electrical conductivity in the high temperature region. Several factors are simultaneously present: a decrease of the ionization coefficients, a rapid rise in the electrical conductivity of the n region, a concomitant decrease in the electric field in the n region, a decrease in the current density of holes entering the junction from the n region (that is, J_{f0} decreases), and a modification of the space charge in the junction due to the high density of carriers and their relatively low saturation velocities at elevated temperatures. Thus, for example, in a temperature region where the n-region conductivity is increasing at a rate of about 100 percent per 50 K temperature rise, an increase in the value of n-region conductivity by a factor of two at 750 K will cause the current density J_{p0} to exceed J and the junction voltage to plunge to its resistive limit. The apparent scatter in the breakdown voltages calculated at the current density of 10^7 A/m² can be attributed to the scatter in the values chosen for n-region conductivity. These were obtained from interpolation of graphical data in Runyan.⁴⁵

Calculations of junction characteristics at 10^8 A/m² in the room temperature regime was not possible using the methodology of lower current densities. The extremely high current density gave rise to a

net negative space charge in the junction region and values of the other variables that were felt to be meaningless. The experimental work wherein the amplitude of the applied current pulse was gradually increased from average current densities well below 10^6 A/m^2 to average current densities above 10^8 A/m^2 showed gradual changes in waveforms, with no indications of anomalous behavior at high current densities. Thus some modifications of the underlying theory are believed to be necessary. A simple modification that will give solutions is to relax the assumption that the carriers have the assumed saturation velocities at the high fields necessary to sustain current densities of 10^8 A/m^2 and above. If the carrier velocities are assumed to be sufficiently large that the space charge is determined primarily by the donor atoms of the n region, then plausible solutions are again obtained. At higher temperatures more holes are drawn into the junction from the n region. These influence the space charge density in a significant fashion so that solutions using the methodology of the lower current densities again become possible. This occurs at 600 K, and then only if the minimum speed of the electrons is chosen so that the n region space charge remains positive. However, in this case, it is not necessary to hypothesize a speed greater than the saturation speed assumed in the underlying theory. The junction voltage obtained at 600 K is 112 V, much higher than the junction voltage of 64 V at 600 K and 10^7 A/m^2 . The high voltage at 600 K is associated with the temperature dependence of the mobility of the junction carriers. For comparison, the curves marked R in Figs. 103 a, b, c show the voltage across a segment of the

n region having the same width as the junction at current densities of 10^6 , 10^7 and 10^8 A/m², respectively.

Table 16 shows the temperature at which the current density J_{po} equals J for each of the current densities of the JVT calculations.

Figure 104 presents the dependence of the depletion layer width on temperature for the conditions of Fig. 103. Except for the region of anomalously high junction voltages between 600 and 670 K at the current density of 10^8 A/m², the widths are in the range of

Table 16
TEMPERATURE AT WHICH JUNCTION BECOMES RESISTIVE
FOR DIFFERENT CURRENT DENSITIES

CURRENT DENSITY (A/m ²)	TEMPERATURE WHEREIN $J_{po}=J$ (K)
10^4	563
10^5	633
10^6	748
10^7	1025
10^8	?

(2.9 ± 0.6) μ m. In calculations with the electrothermal model, the junction was represented with a constant width to simplify the heat transfer calculations. However, the actual junction widths could be included in the electrothermal model.

Figures 105 to 115 show the spatial dependences of the electric field, charge density, electron density, hole density, electron current density, avalanche generation rate, thermal generation and recombination rate, electron ionization coefficient, hole ionization

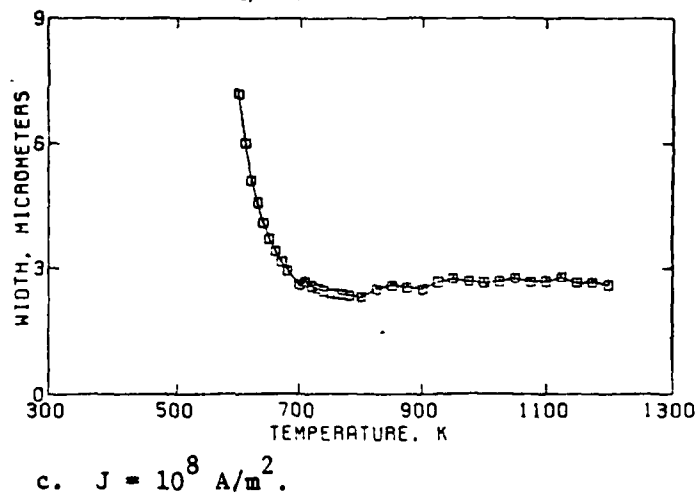
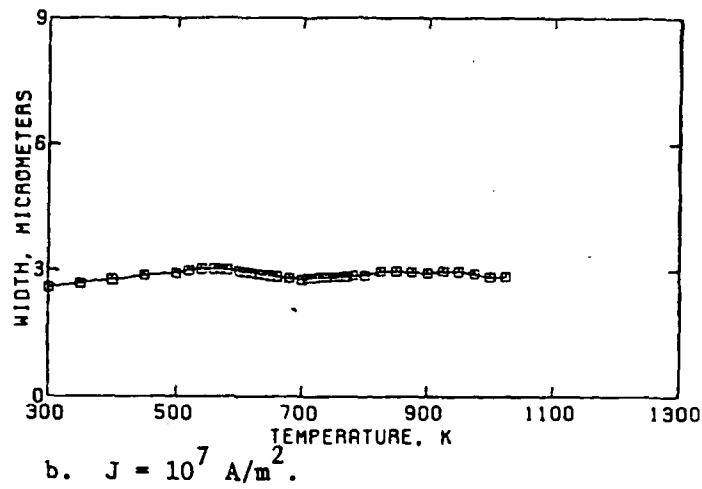
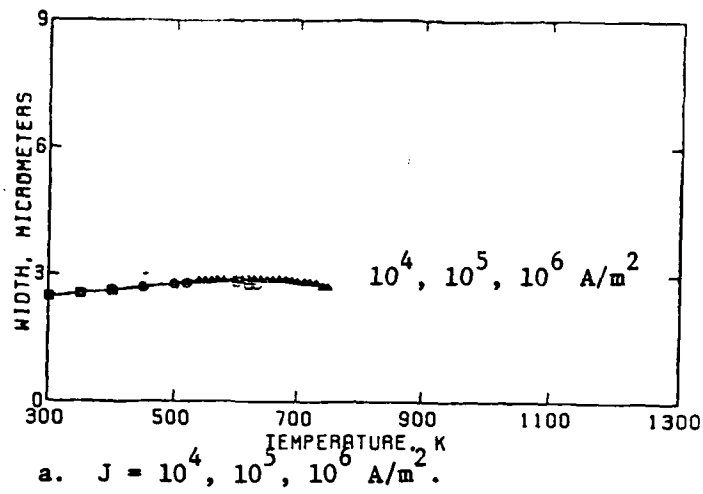


Fig. 104. Junction width vs temperature for different current densities.

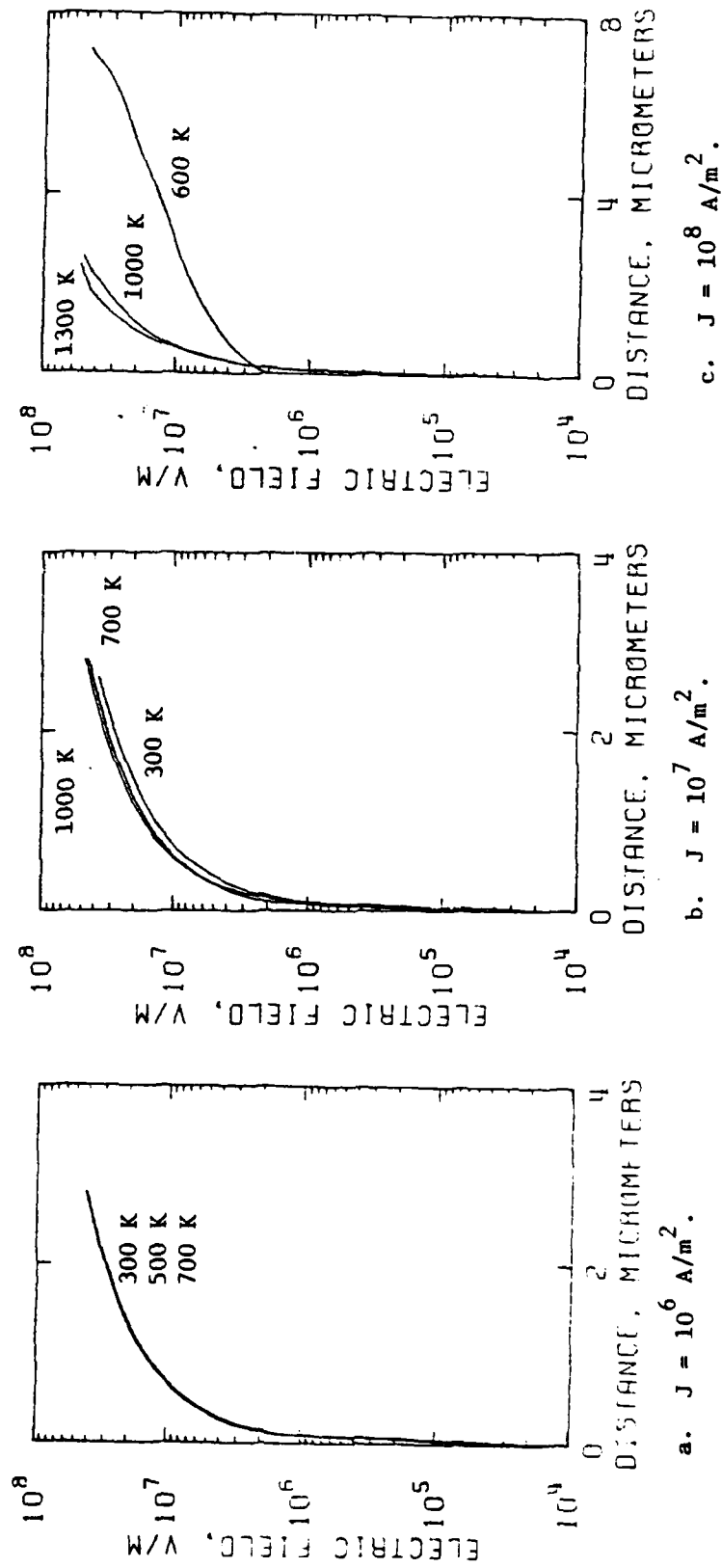


Fig. 105. Electric field vs distance in the depletion layer at constant current density and constant temperature.

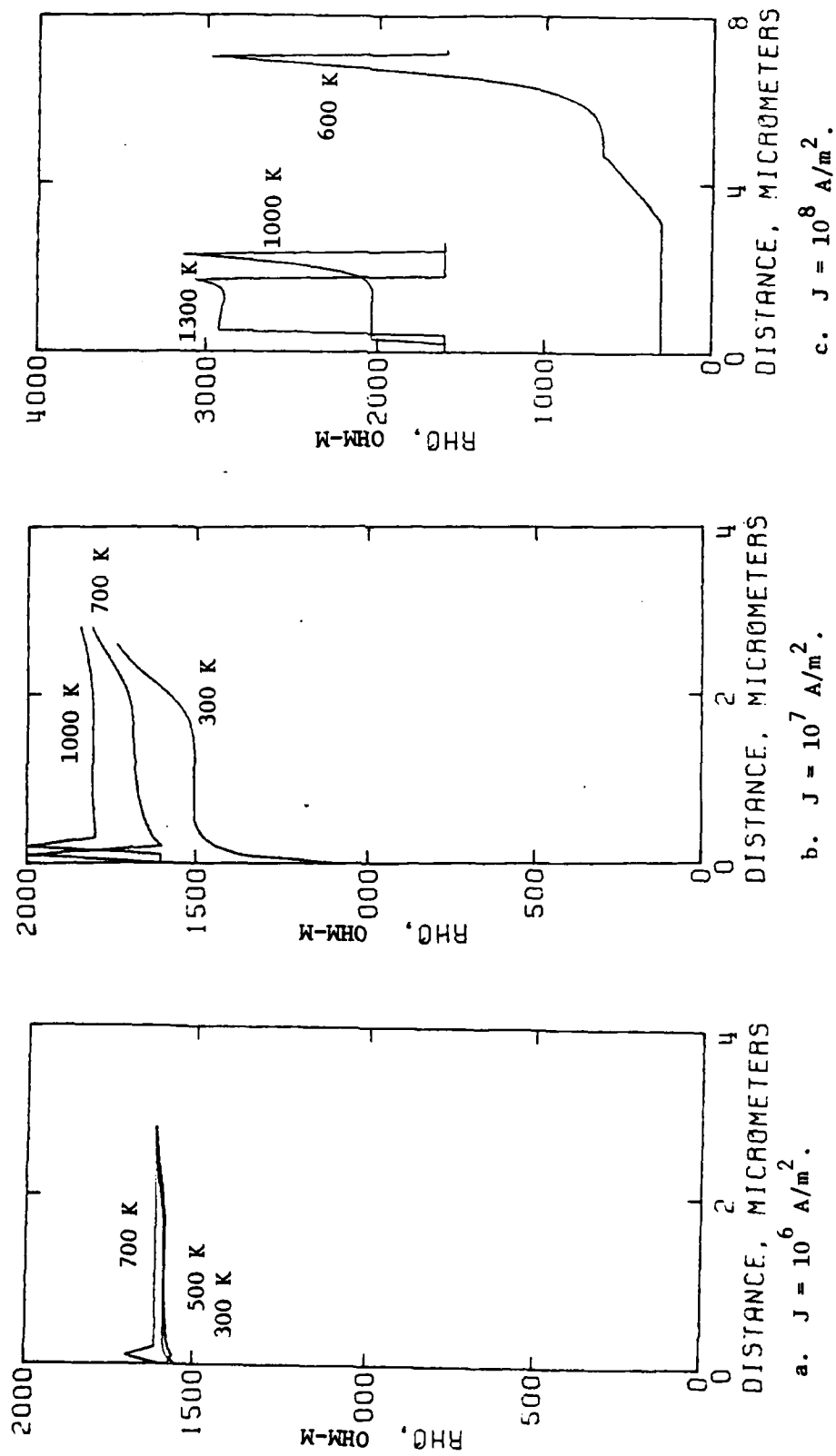


Fig. 106. Resistivity vs distance in the depletion layer at constant current density and constant temperature.

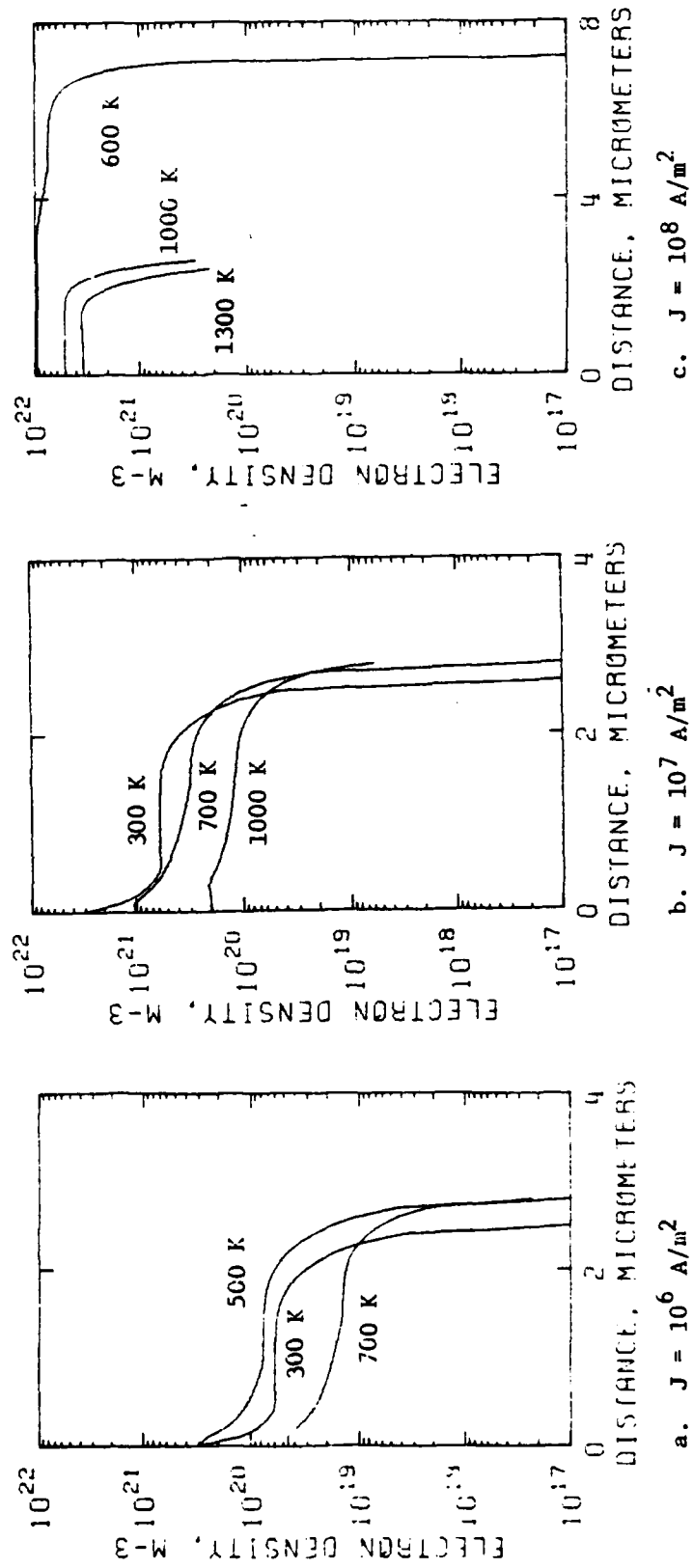


Fig. 107. Electron density as a function of position in the depletion layer at constant current density and constant temperature.

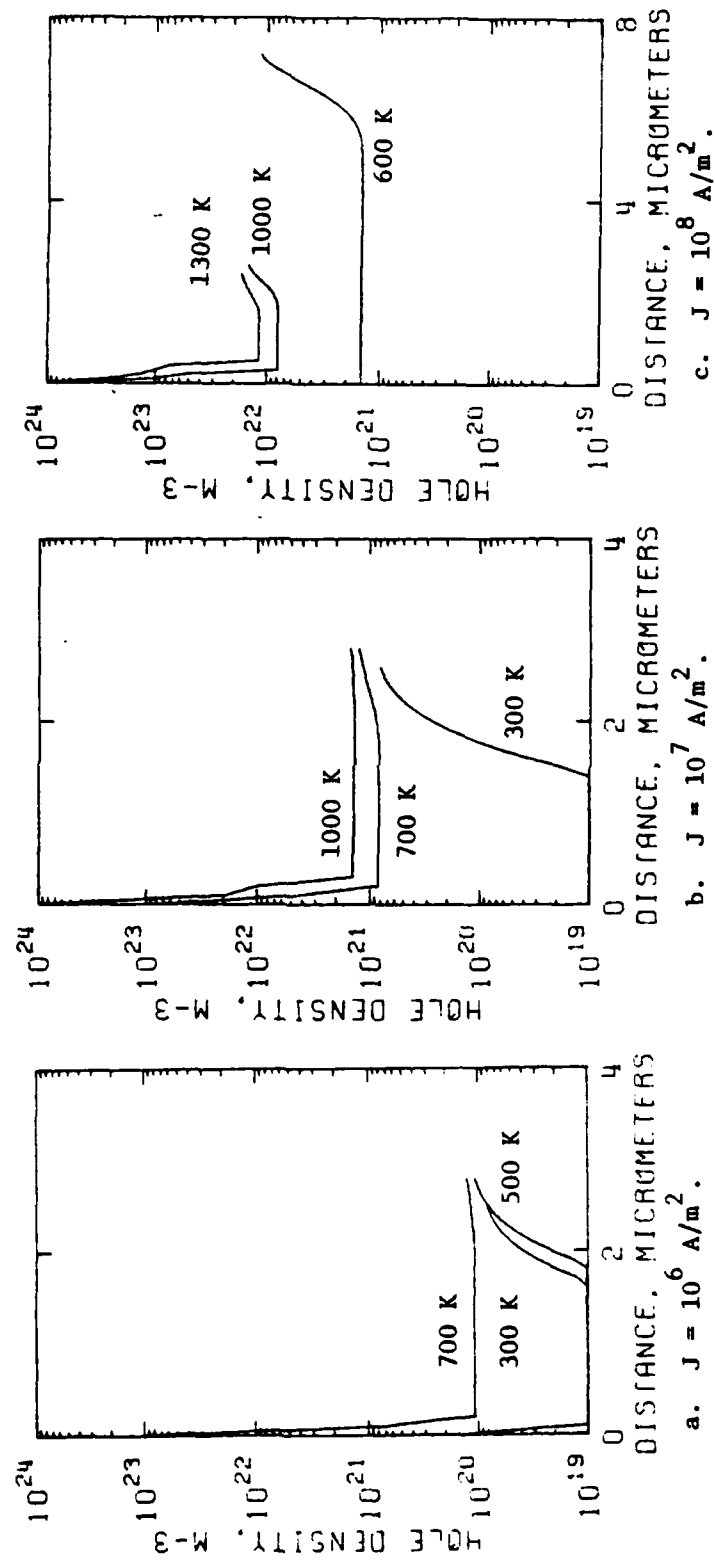


Fig. 108. Hole density vs distance in the depletion layer at constant current density and constant temperature.

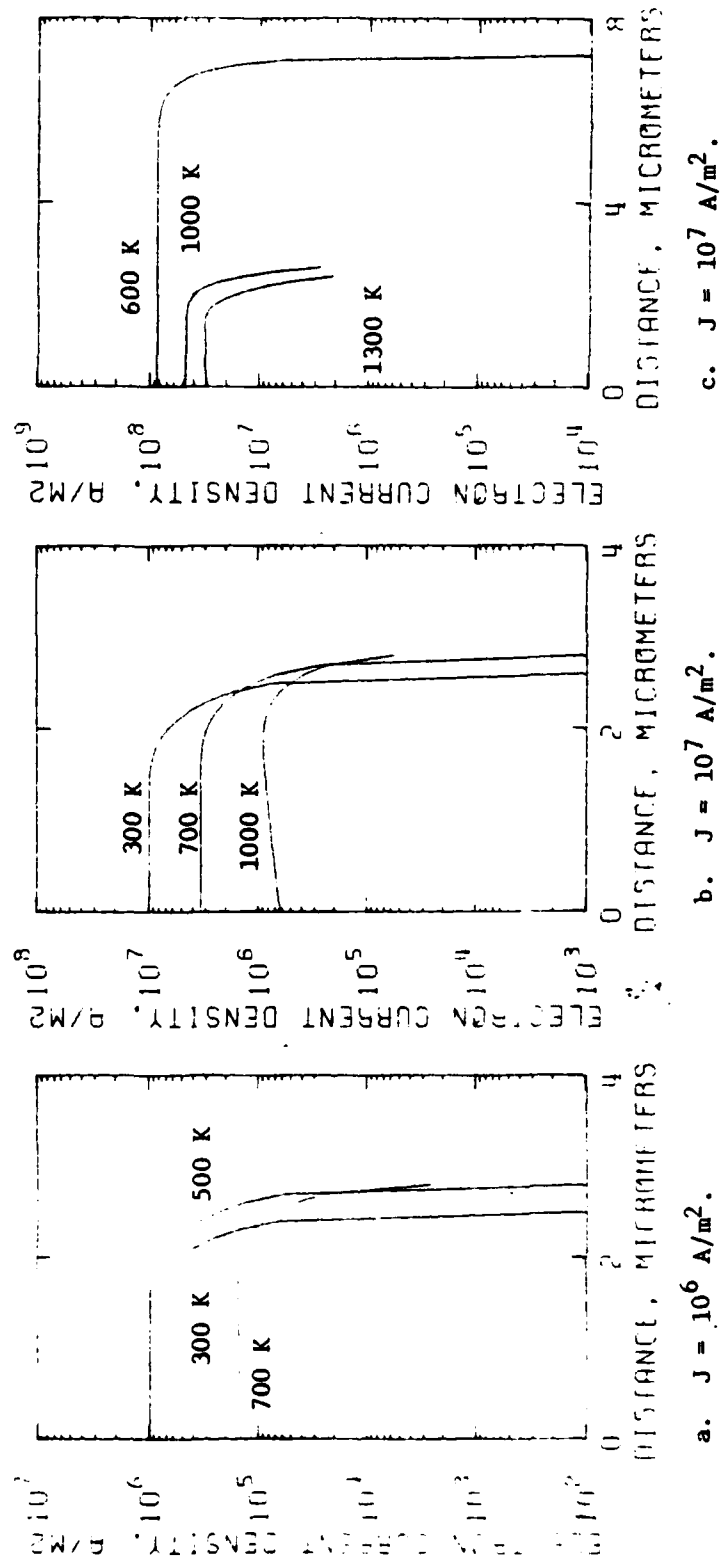


Fig. 109. Electron current density vs distance in the depletion layer at constant current density and constant temperature.

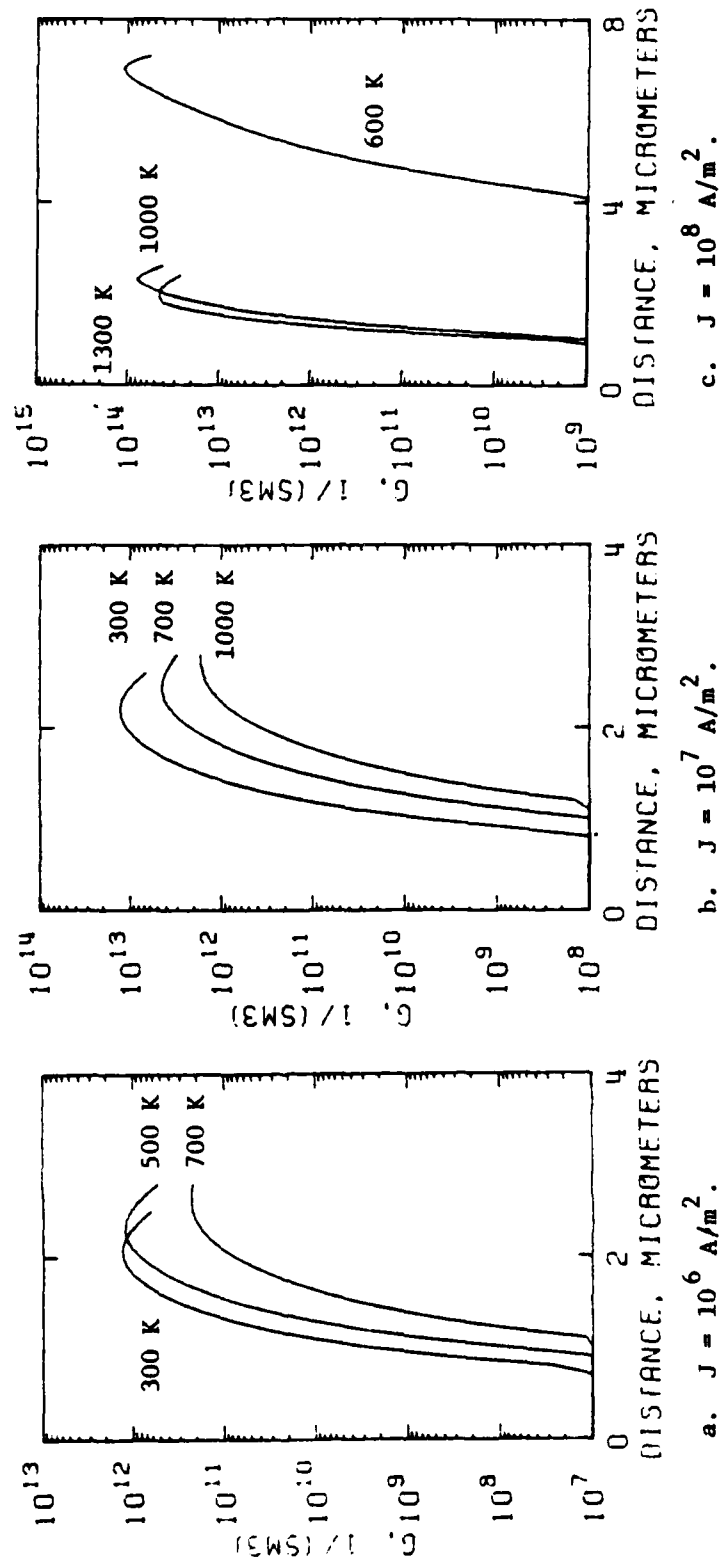


Fig. 110. Carrier generation rate due to avalanching vs distance in the depletion layer at constant current density and constant temperature.

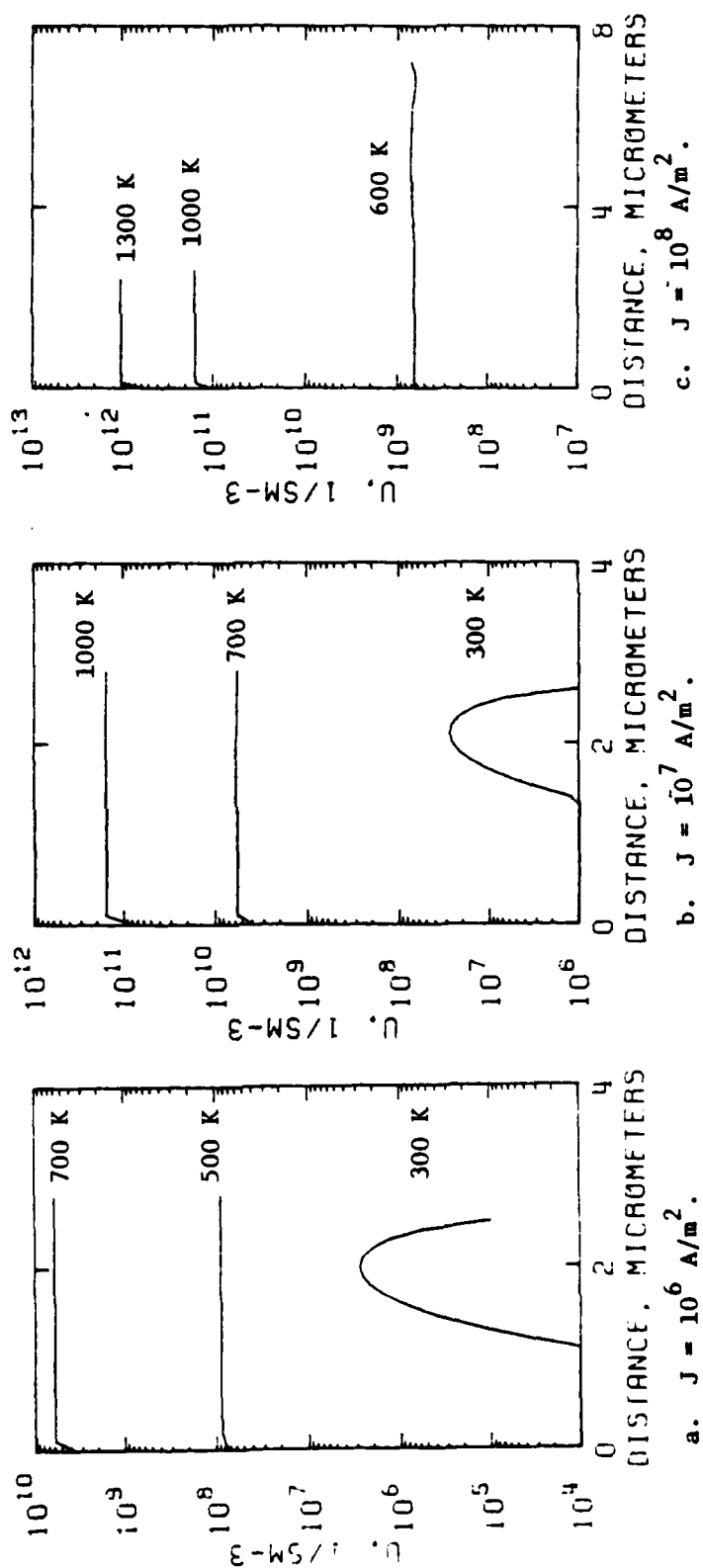


Fig. 111. Carrier recombination rate vs distance in the depletion layer at constant current density and constant temperature.

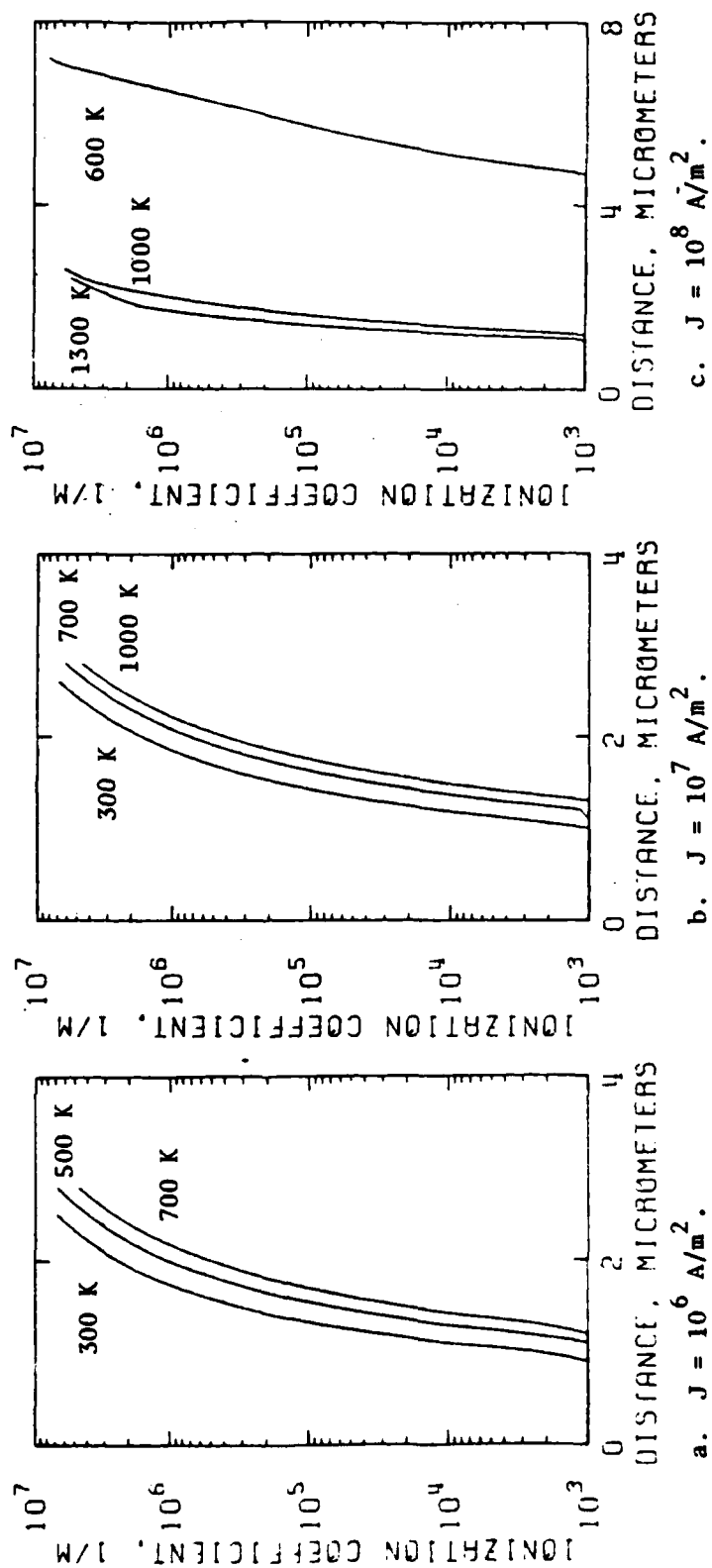


Fig. 112. Electron ionization coefficient vs distance in the depletion layer at constant current density and constant temperature.

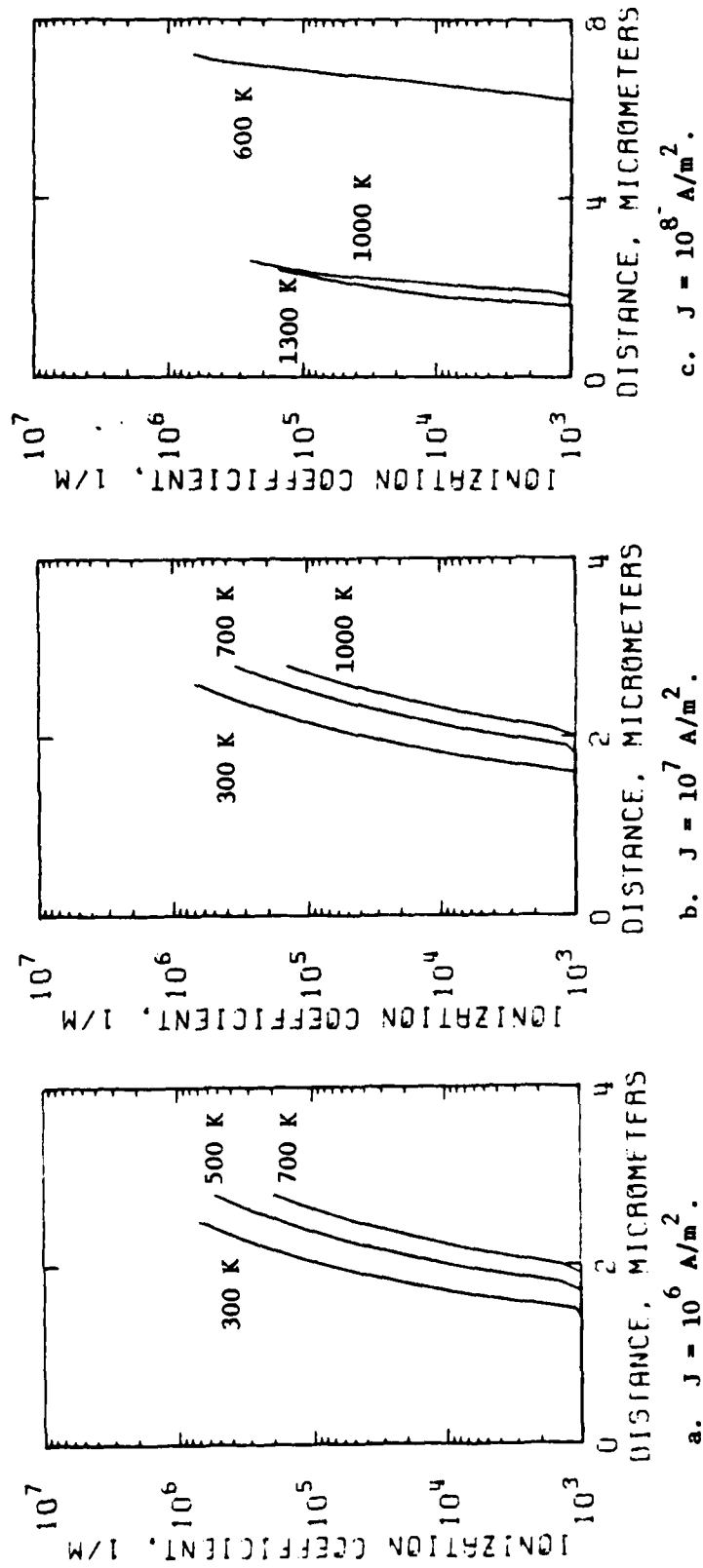


Fig. 113. Hole ionization coefficient vs distance in the depletion layer at constant current density and constant temperature.

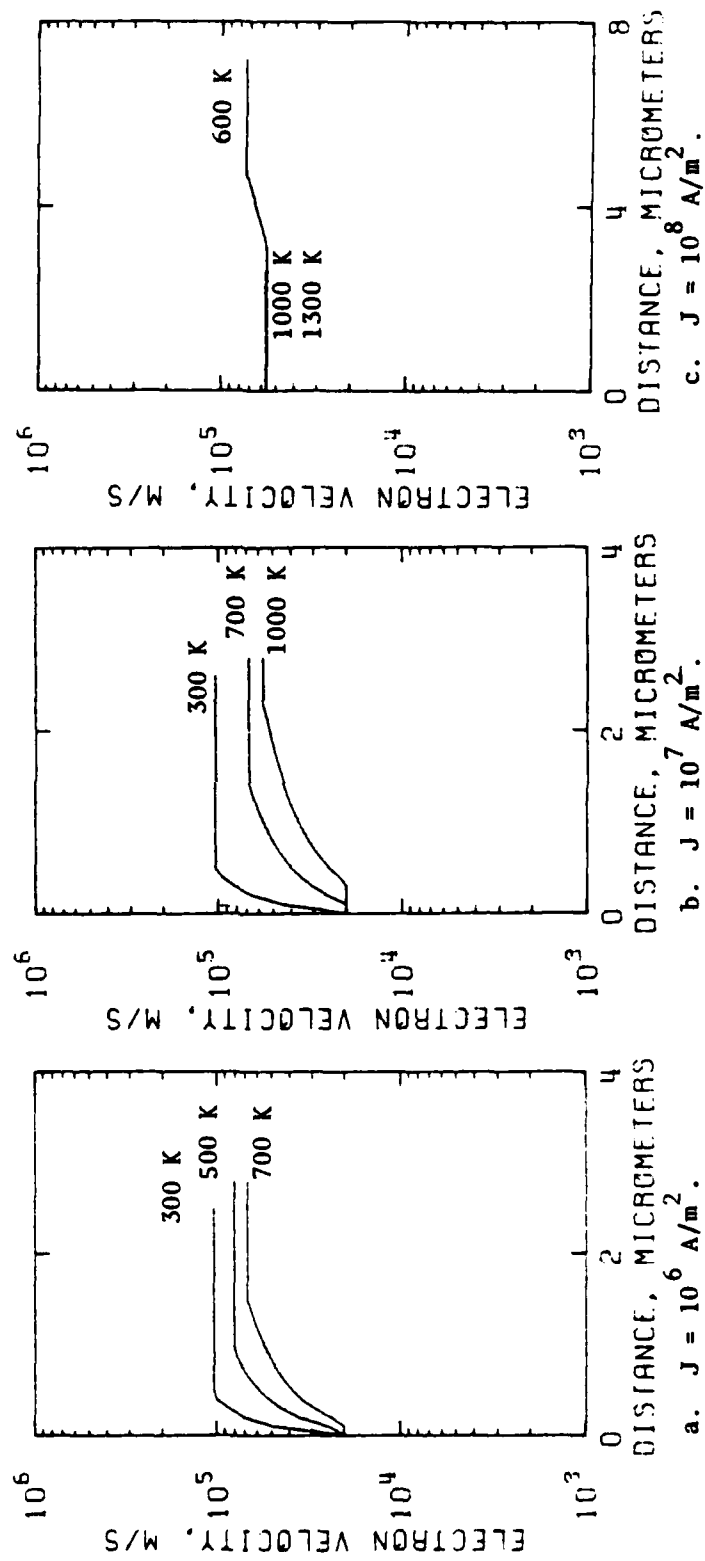


Fig. 114. Electron velocity as a function of position in the depletion layer at constant current density and constant temperature.

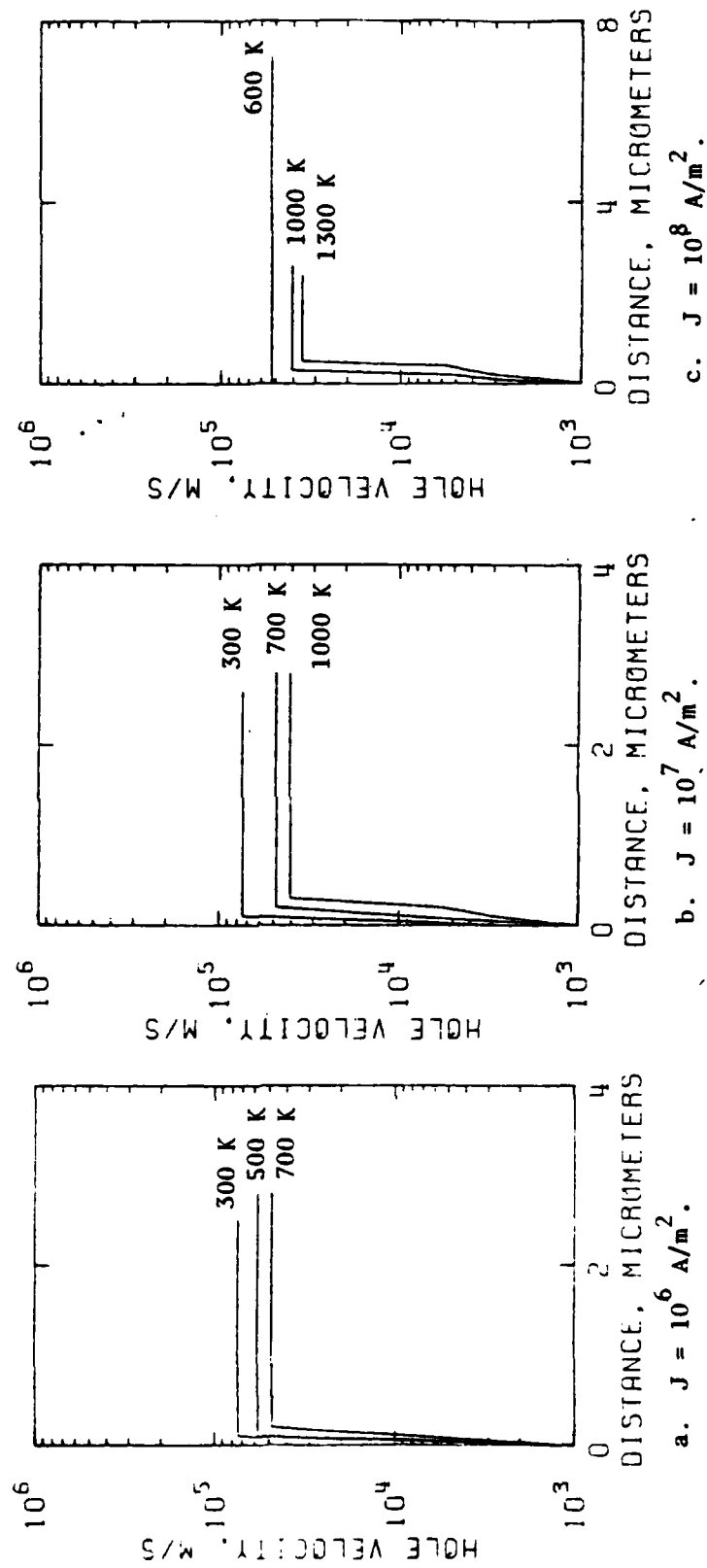


Fig. 115. Hole velocity vs distance in the depletion layer at constant current density and constant temperature.

coefficient, electron speed, and the hole speed for the conditions listed in Table 17.

TABLE 17
CONDITIONS USED IN FIGS. 105-115

CURRENT DENSITY (A/m^2)	TEMPERATURES (K)
10^6	300, 500, 700
10^7	300, 700, 1000
10^8	600, 1000, 1300

Figures 105a,b, and c show the electric field configurations for current densities of 10^6 , 10^7 , and $10^8 A/m^2$, respectively. In each case, for all of the temperatures listed in Table 17, the electric field increases monotonically from the edge of the depletion region ($x = 0$) on the n-region side of the junction. Figures 105-115 show parameters from $x = 0$ to the metallurgical junction. The maximum electric fields in all cases shown, where the junction must avalanche to supply the requisite carrier density, are about $5 \times 10^7 V/m$ and are attained at the metallurgical boundary.

The net charge density in the junction depletion region is shown in Fig. 106. In obtaining JVT characteristics under reverse bias conditions, the natural boundary condition to assume at $x = 0$ is that the electric field at $x = 0$ is the same as the electric field required to sustain the current density J in the n region away from the junction. If this condition is used, along with the generally accepted values for mobilities and conductivities, a negative space charge arises at the

lower temperatures even at relatively low current densities. This generates a nonsensical solution. For example, at 300 K and 10^6 A/m², the electron speed in the n region is about 150 m/s, while a speed of 625 m/s is required with a doping density of 10^{22} atoms/m³ if the space charge is to be non-negative at the edge of the n-region depletion width. If the boundary condition is altered slightly so that the net charge density at the boundary is zero, then meaningful solutions are obtained. A nearly equivalent procedure, and one that is very convenient in practice when many different conditions are being explored, is to choose a minimum electron speed for the junction region that yields a zero or small positive value of total charge density at the junction edge. Thus, for example, for 300 K and 10^6 A/m², minimum electron speeds of 10^3 and 2×10^4 m/s give rise to junction voltages of 46.32 and 46.34 V, respectively. In the present calculations the minimum electron speeds that were used were 10^3 m/s for current densities of 10^4 and 10^5 A/m², 2×10^4 m/s for current densities of 10^6 and 10^7 A/m², and 5.7×10^4 m/s for a current density of 10^8 A/m². In Fig. 106a, the flatness of the curves shows that the mobile charges contribute very little to the net space charge. The mobile carriers contribute significantly, however, at higher current densities, with holes playing a greater role at the higher temperatures. The hole velocities are smaller than the electron velocities, so each hole contributes more to the space charge than a single electron. Also, at elevated temperatures, the hole current injected at the n-side of the junction becomes an important part of the total current. Each of these effects tends to preserve the positive space charge in the n region. Thus the space

charge region appears to have meaning even at 1300 K for the current density of 10^8 A/m^2 and doping density $10^{22} \text{ atoms/m}^3$. Electron and hole densities are shown in Figs. 107 and 108.

The electron current density is displayed in Fig. 109. At the lower temperatures, the current is almost completely carried by electrons until the metallurgical junction is approached. Examination of the electric field configurations of Fig. 105, the avalanche generated current in Fig. 110, the thermally generated current within the junction in Fig. 111, and the ionization coefficients in Figs. 112 and 113 provide the needed perspectives. Avalanche is restricted to the high field region close to the metallurgical junction. The avalanche process is needed for the junction to be able to provide the necessary current level. At higher temperatures a large portion of the current is carried by the holes introduced from the n region. Thus the electron current through the junction is correspondingly reduced. Examination of the thermal generation/recombination term shows that recombination is the dominant process. Thus the change in the number of thermally activated carriers is associated with the injection process from the n region and not volume generation within the junction.

Examination of the magnitudes of the ionization coefficients for electrons and holes, Figs. 112 and 113, shows that holes do not play a major role in initiating ionization.

Electron and hole speeds are shown throughout the junction region for ranges of current densities and temperatures in Figs. 114 and 115, respectively. Holes are found to be at their saturation velocity through most of the junction, for all current densities. However the

electrons can be significantly below their saturation velocities for a large portion of the junction at the lower current densities and higher temperatures.

After reviewing the above calculations, one is left with the feeling that the pn junction under high reverse currents and at elevated temperatures is not as well characterized as is necessary for the second breakdown problem.

XI. RESULTS OF ELECTROTHERMAL MODEL

Silicon-on-sapphire diodes were analyzed with particular stress on the effect of device geometry and excitation conditions on current filamentation leading to the second breakdown transition under reverse bias. Variations in device geometry included silicon film thickness and junction contour (uniform junction, p^+n junction with spikes, and n^+n junction with spikes). The excitation conditions, that were varied include pulse length, pulse amplitude, and pulse shape (single step and double-step pulses). Computer simulations of SOS devices yielded temporal development of current distributions and of temperature distributions of the diodes. It also provided device terminal voltage as a function of time. The information obtained from these computer calculations is analyzed in this chapter. The features of interest are: location of filaments (correlation with the excitation step amplitude, pulse duration and device geometry), conditions when filaments are initiated (junction region temperature and n-region temperature), onset of instability leading to formation of melt, delay time for initiation of filaments (correlation with voltage waveform and current amplitude), and delay time for onset of instability (correlation with voltage waveform and current amplitude).

Calculations on the uniform junction and on the p^+n junction with spikes were performed by Baruah⁸⁸, while those on the n^+n spikes were performed by Liou⁸⁹. Results will be presented in the sequence:

uniform junctions, p^+n spike junctions. Comparisons will be made along the way evaluating the role of spikes. Chapter XII relates the theoretical results to the experimentation of Part I.

In this chapter, SI units are used exclusively. The following parameters were employed by Baruah.

Initial temperature	300 K
Time increment	.01 μ s
n-region length	30 μ m
p^+ , n^+ region lengths	160 μ m
Junction depletion layer width	4 μ m
Diode width	204 μ m
n-region doping density	10^{22} atoms/ m^3
p^+ , n^+ regions doping density	10^{26} atoms/ m^3
Silicon film thickness	.6, 1.2 μ m
Excitation pulse amplitudes	8-21 mA
Minimum pulse length	.87 μ s
Maximum pulse length	11.32 μ s
Diffusion spike height	0.20, 0.32, 4.0 μ m

Tables 18a, b and c indicate the special parameters employed in the uniform junction and p^+n spike junction calculations of Baruah.

TABLE 18a

SUMMARY OF SOS DIODE SIMULATIONS BY BARUAH
(pulse shape = constant current step)

Run No.	Pulse Amplitude (mA)	Pulse Length (μ s)	Peak Terminal Voltage (V)	Filament Current Density (gA/m^2)	Filament Temperature (K)	Number of Filaments
Structure with no defects						
1	8	11.32	463	1.18	1117	1
2	9	9.74	519	1.68	1277	1
3	10	7.49	577	1.71	1293	1
4	10.5	4.88	610	2.04	1268	2
5	11	4.10	639	2.19	1325	2
6	12	3.50	693	2.40	1481	2
7	9,11	6.92,8.62	519	0.987	1065	1
8	10,10.5	4.89,7.28	577	1.46	1310	1
9	10,11	6.49,7.78	577	1.73	1364	1
10	11	9.88	327	0.879	546	x
Structure with triple spikes on p^+n junction						
11	8	6.60	452	1.51	1340	3
12	9	4.91	507	1.26	1119	3
13	10	3.29	567	1.24	1101	3
14	10.5	3.28	600	1.29	1113	3
15	11	2.91	629	1.34	1119	3
16	12	1.79	690	1.63	1115	3
17	11	9.59	323	2.19	1188	3
18	21	1.88	611	2.90	1279	3
19	8	5.88	483	0.43	1305	3
20	12	5.08	754	2.00	1408	3

TABLE 18b
SIMULATION PARAMETERS FOR UNIFORM JUNCTION DIODES

Run No.	Film Thickness (μm)	Pulse Shape for Double-step Pulses
1	0.6	—
2	0.6	—
3	0.6	—
4	0.6	—
5	0.6	—
6	0.6	—
7	0.6	—
8	0.6	9 mA (0-6.92 μs), 11 mA (6.92-8.62 μs)
9	0.6	10 mA (0-4.89 μs), 10.5 mA (4.89-7.28 μs)
10	1.2	10 mA (0-6.49 μs), 11 mA (6.49-7.78 μs)

TABLE 18c
SIMULATION PARAMETERS FOR p^+n SPIKE DIODES

Run No.	Film Thickness (μm)	Spike Height (μm)
11	0.6	4.0
12	0.6	4.0
13	0.6	4.0
14	0.6	4.0
15	0.6	4.0
16	0.6	4.0
17	1.2	4.0
18	1.2	4.0
19	0.6	0.20
20	0.6	0.32

A. Uniform Junction Diodes

1. Current Distributions

Figures 116a-f (Runs 1-6) show current distributions over the device area at various times for a given pulse amplitude. Each of the figures relates to one of the excitation amplitudes in the range 8-12 mA and shows time development of filamentation. For example, in Fig. 116a, for $I_{tot} = 8$ mA (average current density = 6.67×10^7 A/m²), current distributions are shown at times 2.83, 5.65, 8.48 and 11.32 μ s. From the figures, it can be generalized that, for a given amplitude, shorter times produce little or no filamentation, an intermediate time creates a broad filament while further increase in time results in distinct current constrictions. Once the intermediate broad filament is formed, the process develops rather quickly. The rapid transition is demonstrated more vividly by showing more closely spaced contours as in Figs. 117a,b (Run 2) and Figs. 118a,b (Run 5) for pulse amplitudes of 9 and 11 mA, respectively. The current distributions in Figs. 117a and 118a are at times just before filamentation, while those in Figs. 117b and 118b are at times just after filamentation. For example, in the case of 9 mA, the growth rate of the maximum current density within the filament is about 2.5 times faster after filamentation when compared to its growth before filamentation.

Formation of double filaments is a striking feature of increasing current amplitude. Single channels occur at 8, 9 and 10 mA, but double filaments are found at 10.5 mA and above. The single filaments are always located centrally with respect to the device width, while the double filaments are situated symmetrically about the center (the

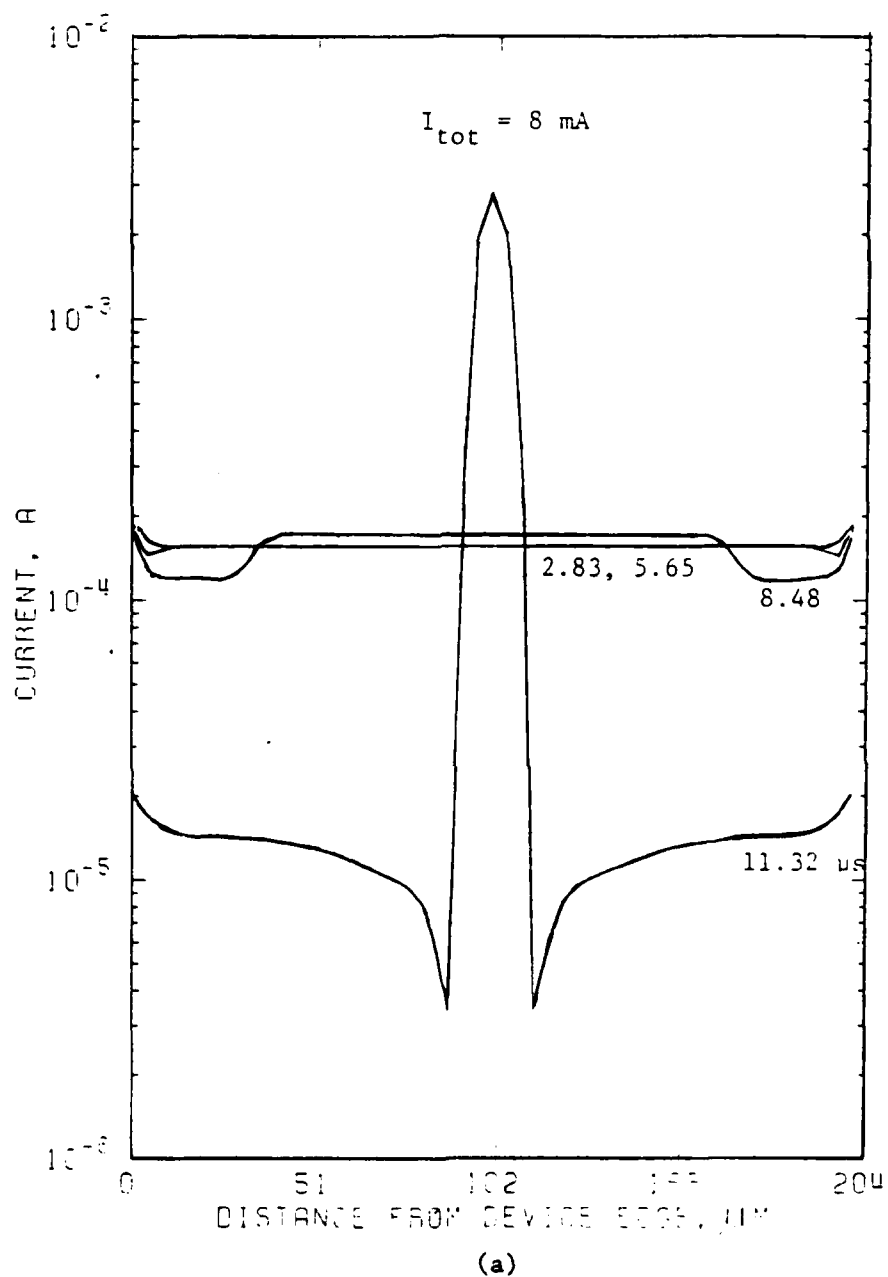


Fig. 116. Current distributions at different times for constant current pulses. (a) 8 mA, (b) 9 mA, (c) 10 mA, (d) 10.5 mA, (e) 11 mA, (f) 12 mA.

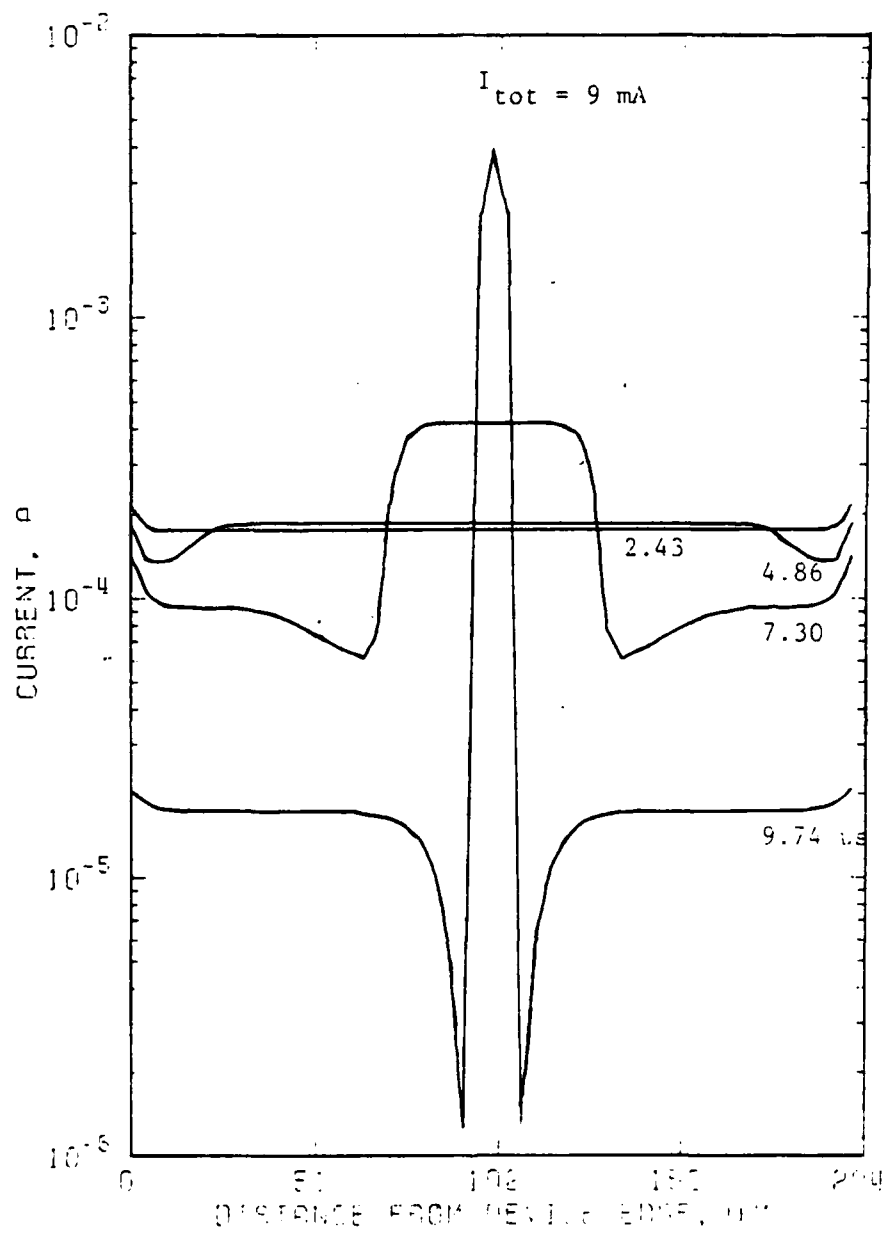


Fig. 116 (b)

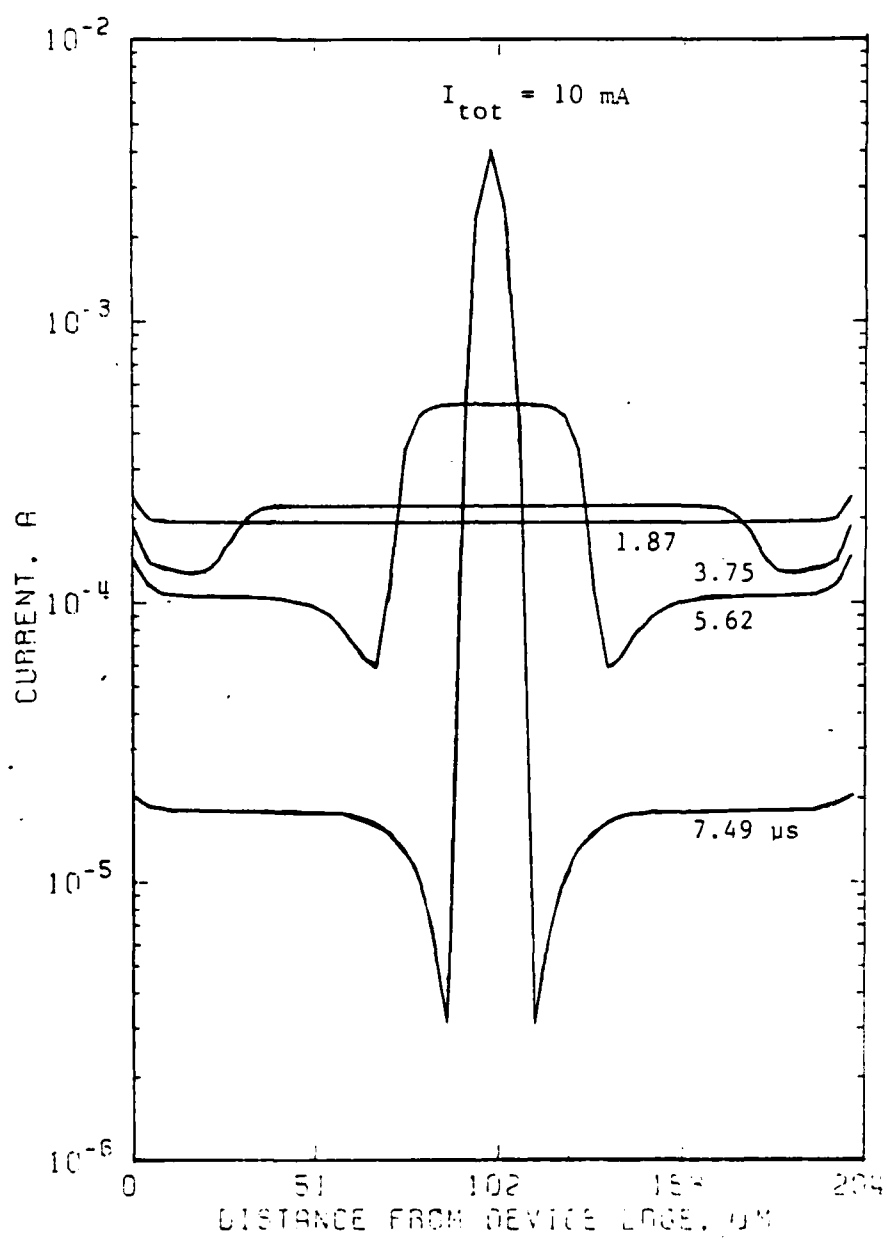


Fig. 116 (c)

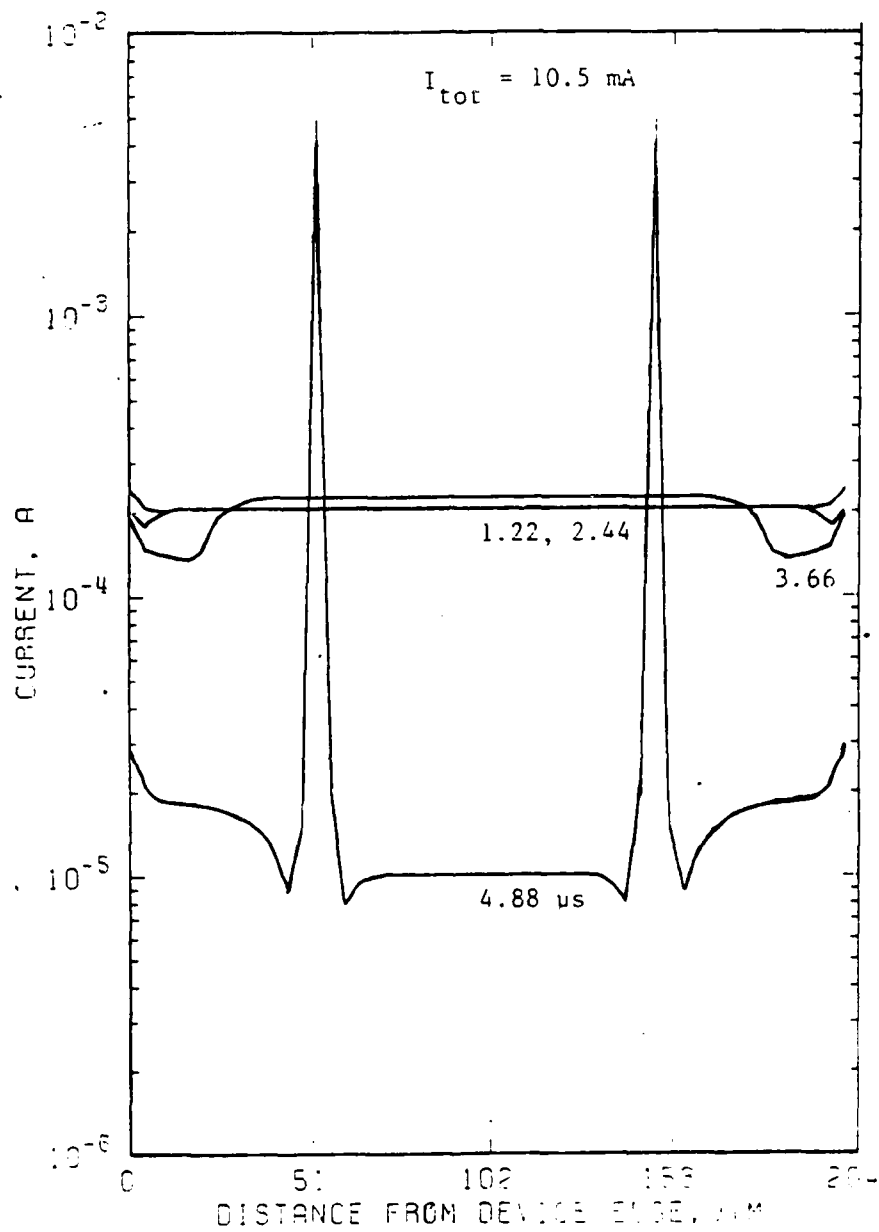


Fig. 116 (d)

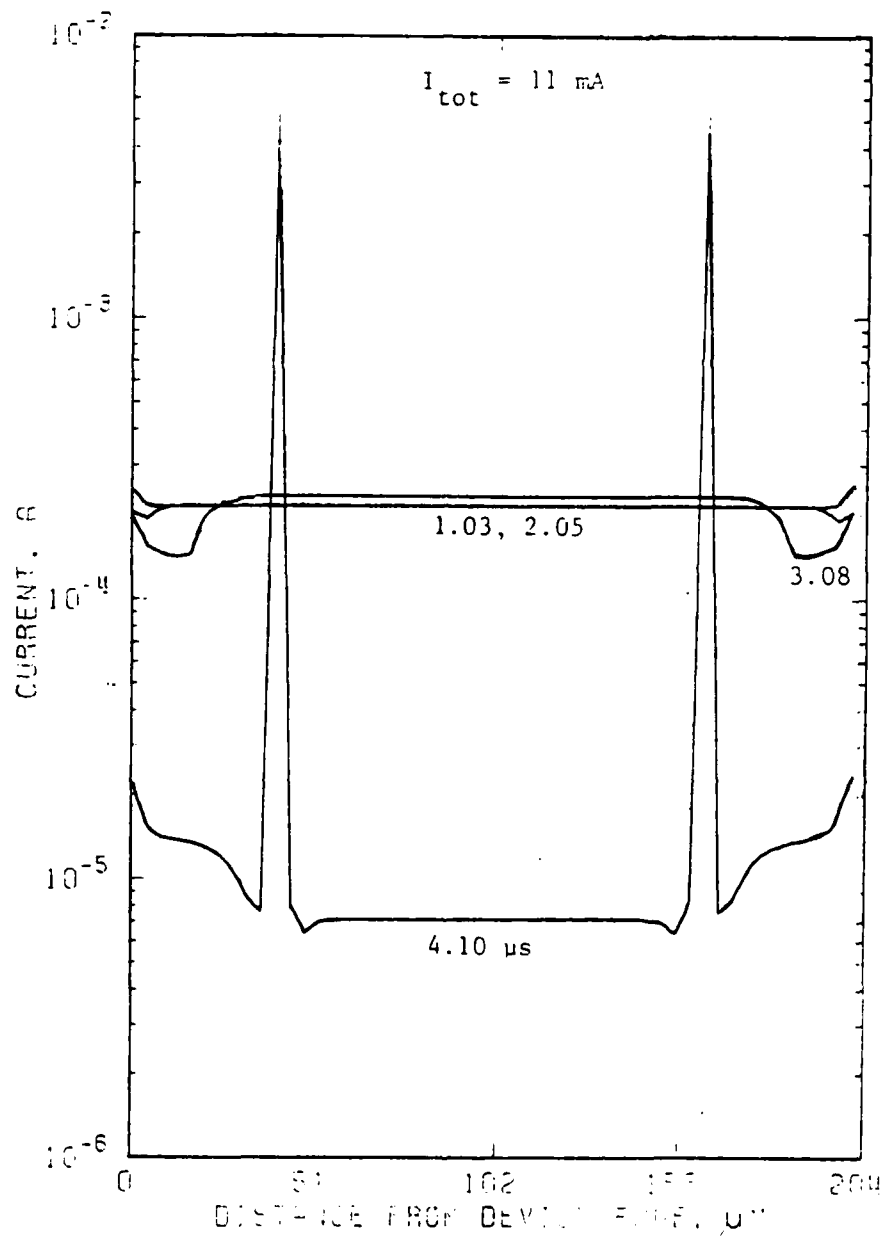


Fig. 116 (e)

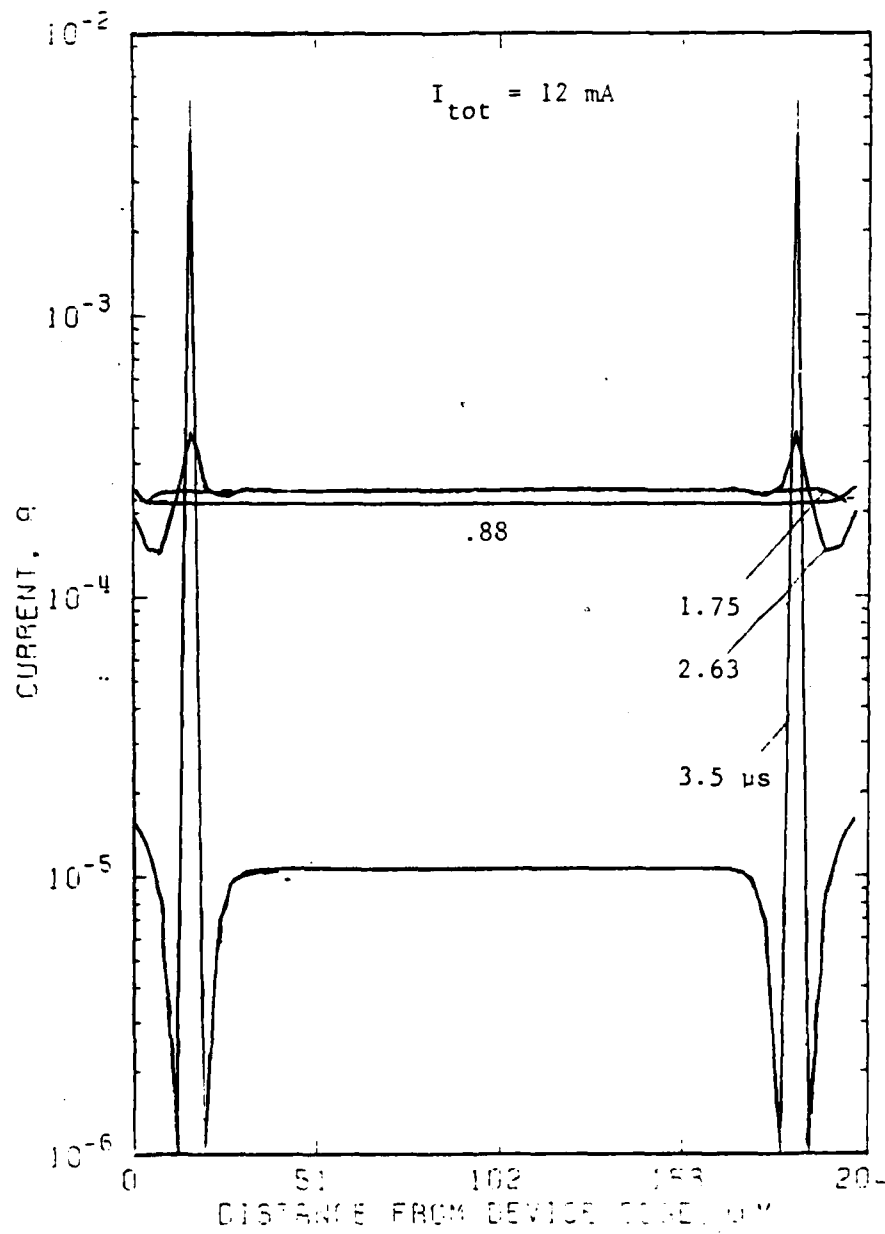


Fig. 116 (f)

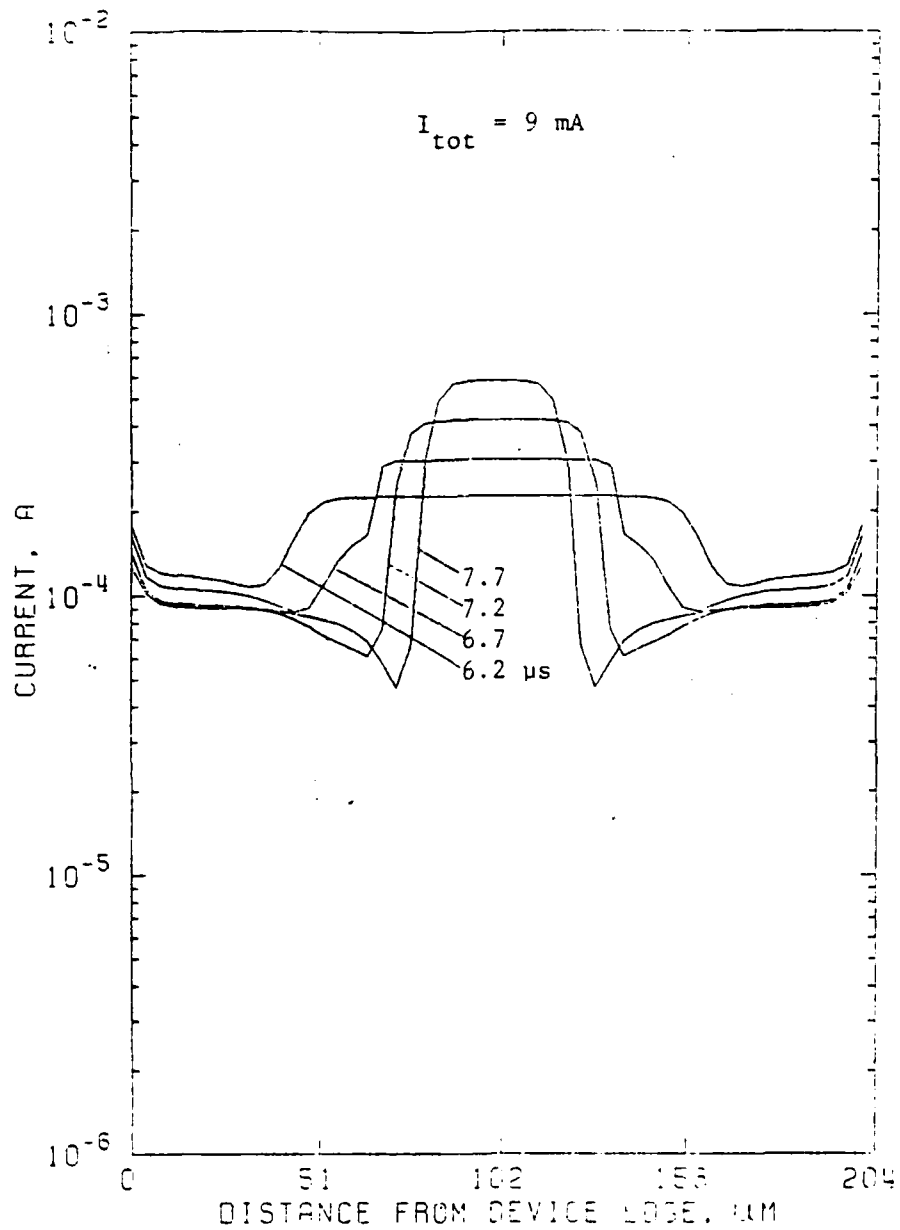


Fig. 117 (a) Current distributions at different times for a 9 mA pulse showing the early stages of filamentation.

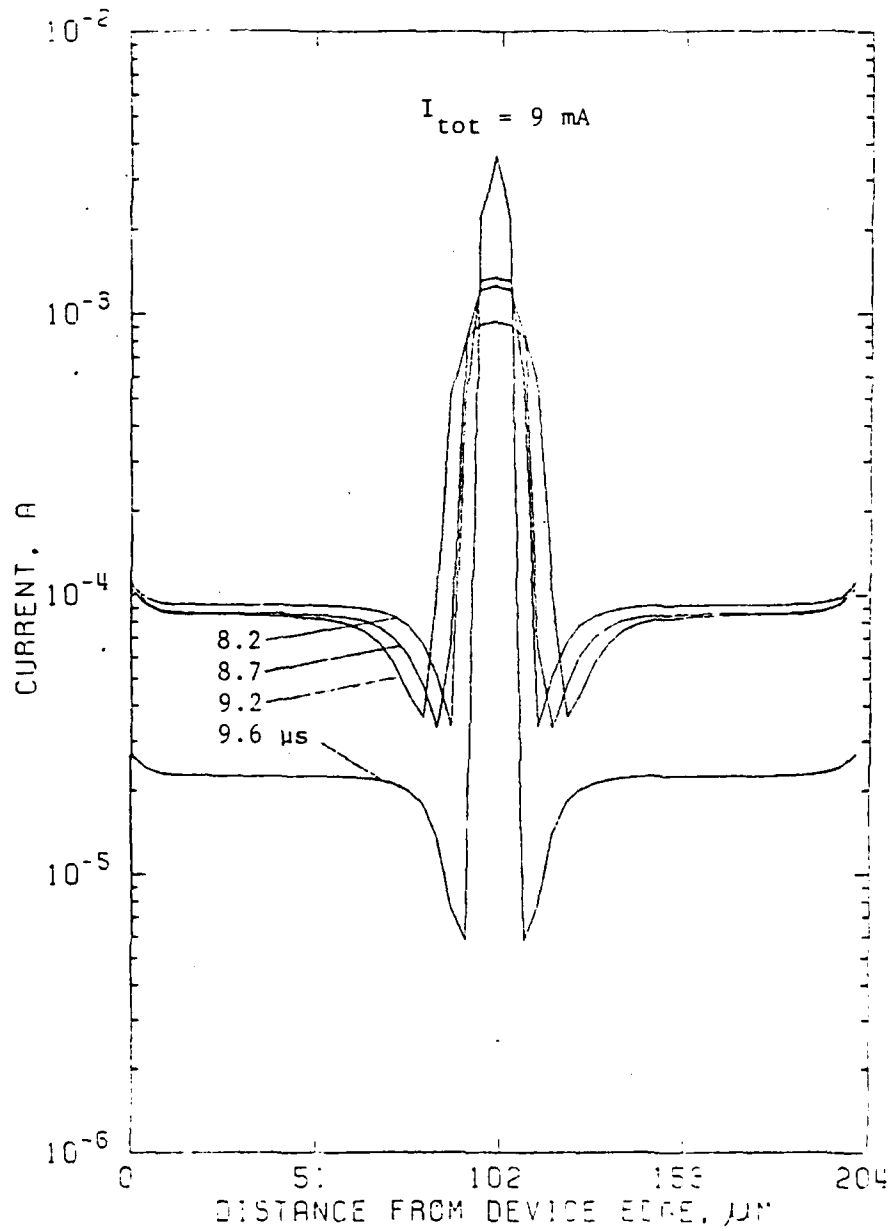


Fig. 117 (b) Current distributions for the same 9 mA current step as in (a), but at later times. Development of the fine filament is detailed.

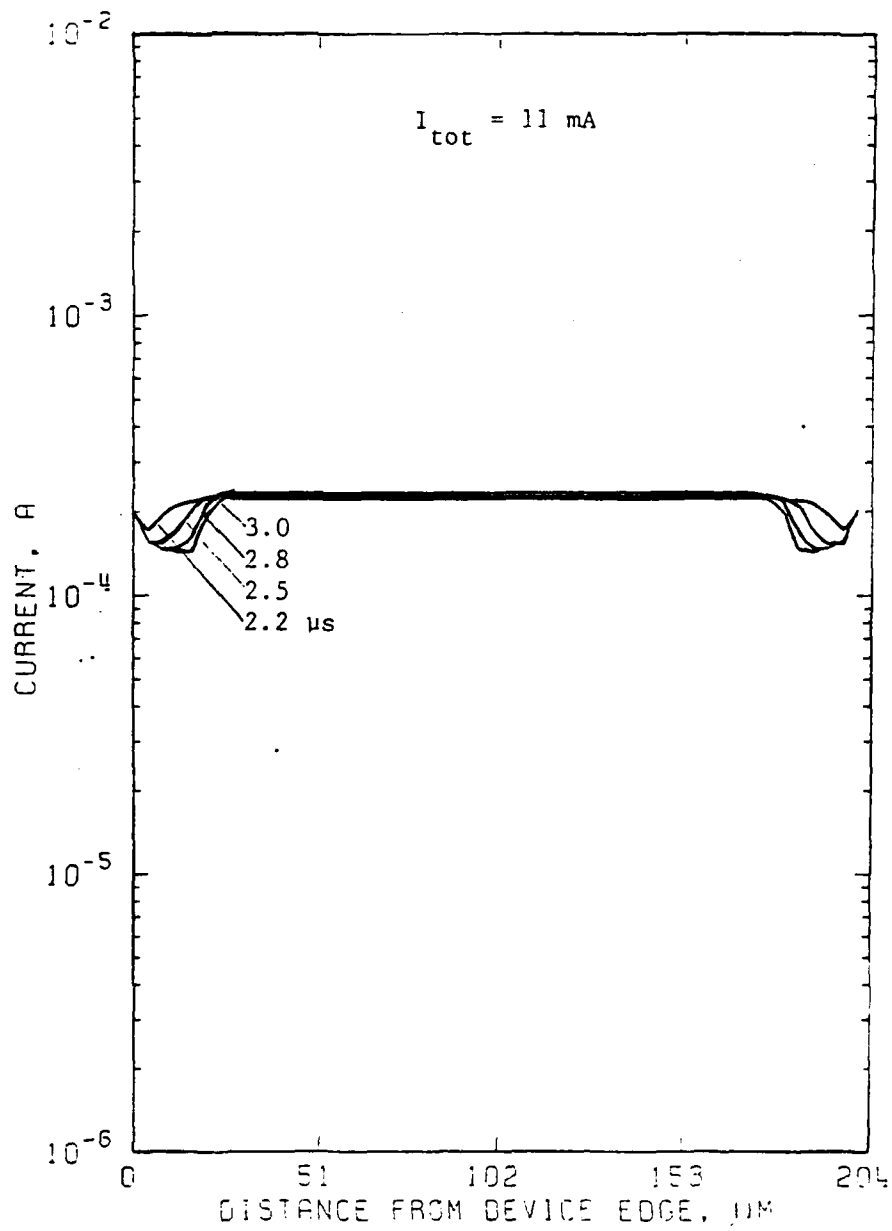


Fig. 118 (a). Current distributions for an 11 mA current step during the early stages of filamentation.

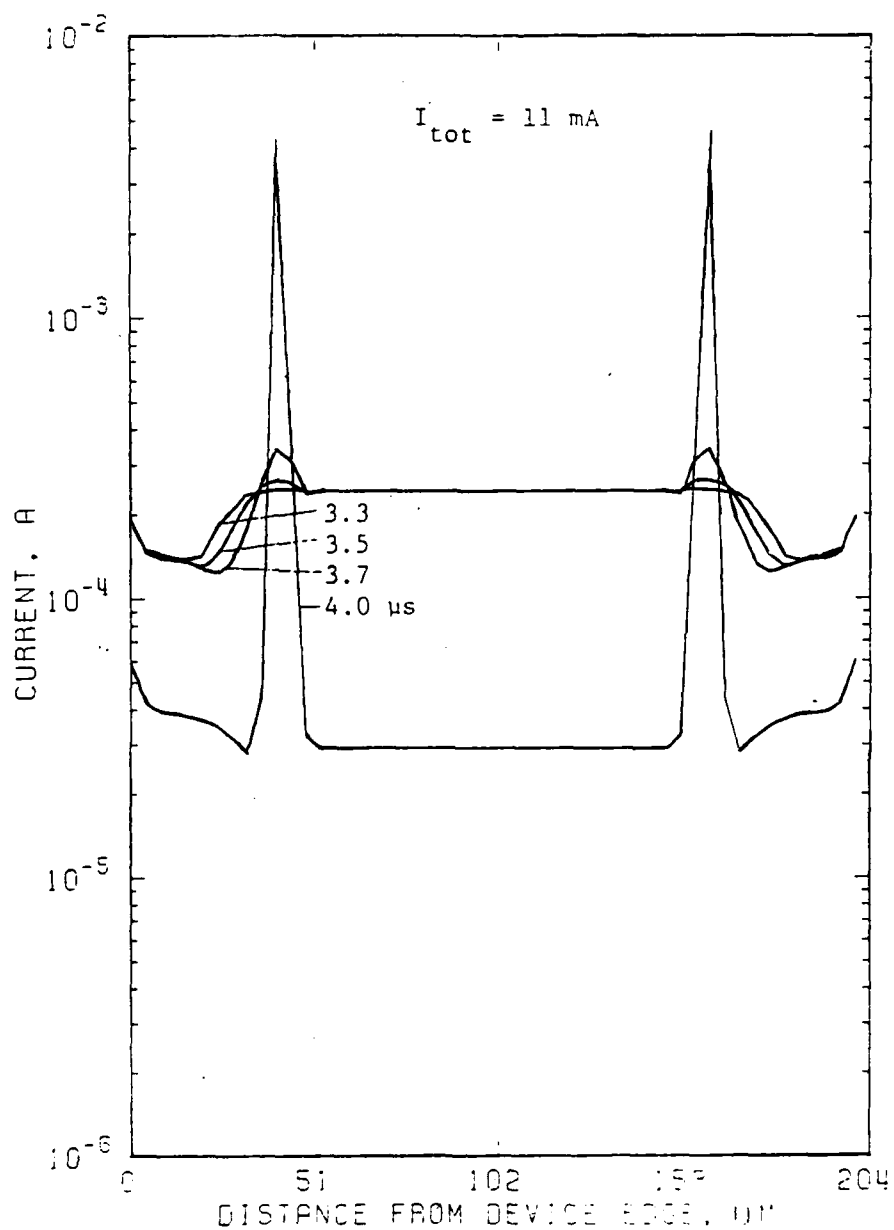


Fig. 118 (b). Current distributions for the same 11 mA current step as in (a), but at later times. Development of narrow double filaments is detailed.

system is symmetric about its center line). Higher amplitude tends to widen the interfilamentary distance and, for both single and double filaments, to narrow their widths. Thus the width at half maximum of the central filament at 8 mA current at $t = 11.32 \mu\text{s}$ is about $17 \mu\text{m}$, while the corresponding width at pulse end for a 12 mA current is $4 \mu\text{m}$ (the mesh width). As an example of changing interfilamentary distances, the separation is $95 \mu\text{m}$ at 10.5 mA (Fig. 116d), $118 \mu\text{m}$ at 11 mA (Fig. 116e), and $166 \mu\text{m}$ at 12 mA (Fig. 116f). Peak current densities inside the filaments intensify with increasing applied amplitude and range in Fig. 116 from 1.18×10^9 to $2.40 \times 10^9 \text{ A/m}^2$.

The reasons for single and double filaments at low and high device currents, respectively, are not obvious. The discussion that follows is based on the analysis of Figs. 117a,b, 118a,b, 119, 120a,b, 121a,b, 124a,b, and 125. Figure 119 shows the junction JVT characteristics and the resistivity-temperature curve for the n-region. The dominant feature for the present geometry is the initial rise in resistivity up to the temperature $(T_m)_R$ and the subsequent drop in resistivity above this temperature.

In Fig. 120a the temperature-time history associated with the growth of the single filament of Fig. 116b is examined, while Fig. 120b displays the temperature-time history of filament growth in the double filament system of Fig. 116e. In Fig. 120a three portions of the device are considered: the n-region (1) and the junction (2) of the strip in the center of the filament site ($102 \mu\text{m}$ from the edge), the n-region (3) and the junction (4) of a strip adjacent to the filament ($94 \mu\text{m}$ from the edge) where the current after filament formation is a minimum,

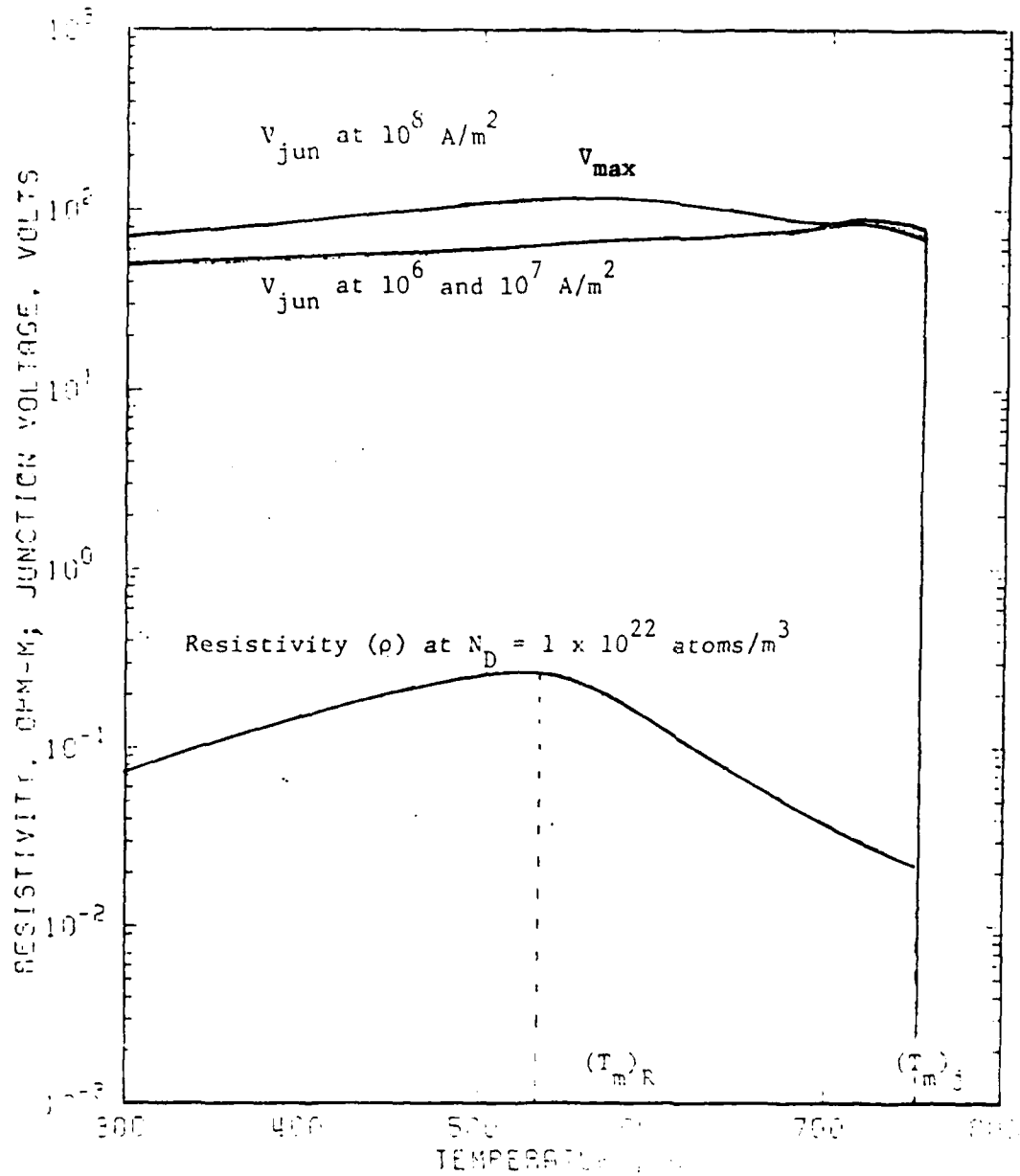


Fig. 119. Resistivity (ρ) and junction voltage (V_{jun}) as functions of temperature. The resistivity curve is for a field of $1 \times 10^5 \text{ V/m}$ and doping density of $1 \times 10^{22} \text{ atoms/m}^3$ while the junction voltages are plotted at applied current densities of 10^6 , 10^7 , and 10^8 A/m^2 . $(T_m)_R$ is the peak temperature of the resistivity curve and $(T_m)_J$ is the temperature at which the junction voltage drops to its resistive limit.

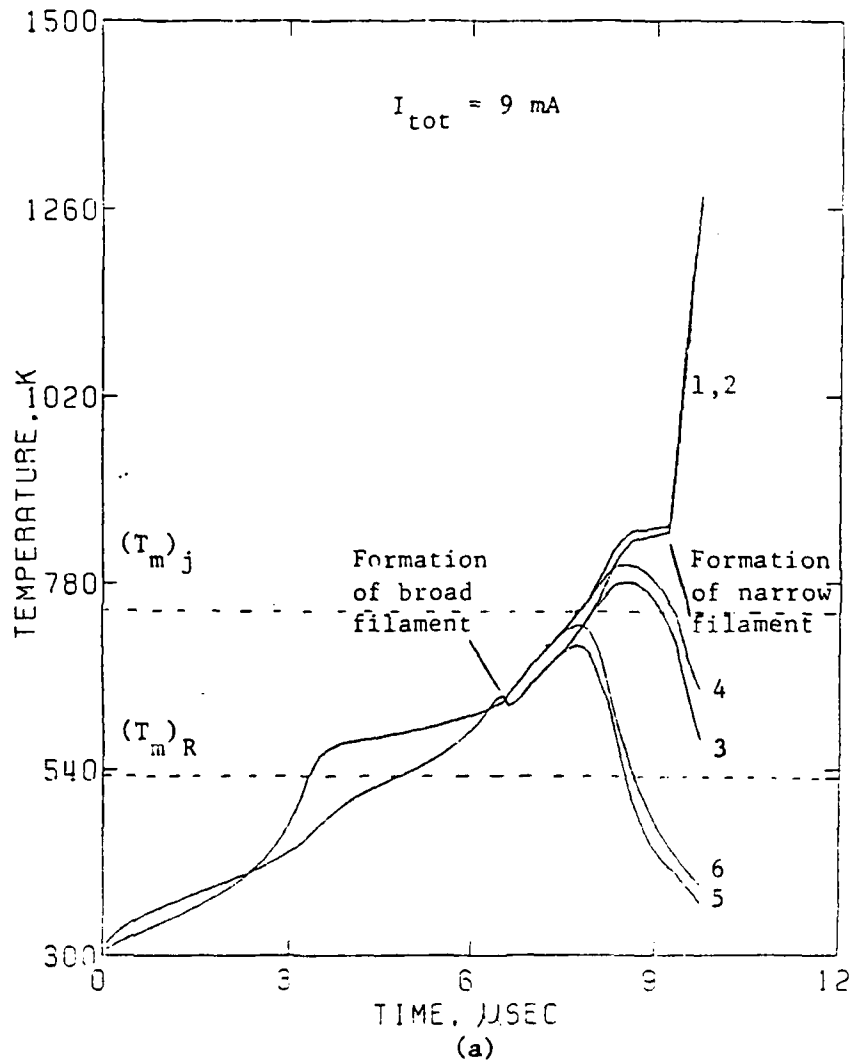


Fig. 120. Temporal development of temperature at various portions of the diode, namely, at a filament site in the junction (1) and the n region (2), near the filament (where the current is a minimum) in the junction (3) and the n region (4), and farther away from the filament in the junction (5) and the n region (6). The applied pulse amplitudes are: (a) 9 mA, (b) 11 mA.

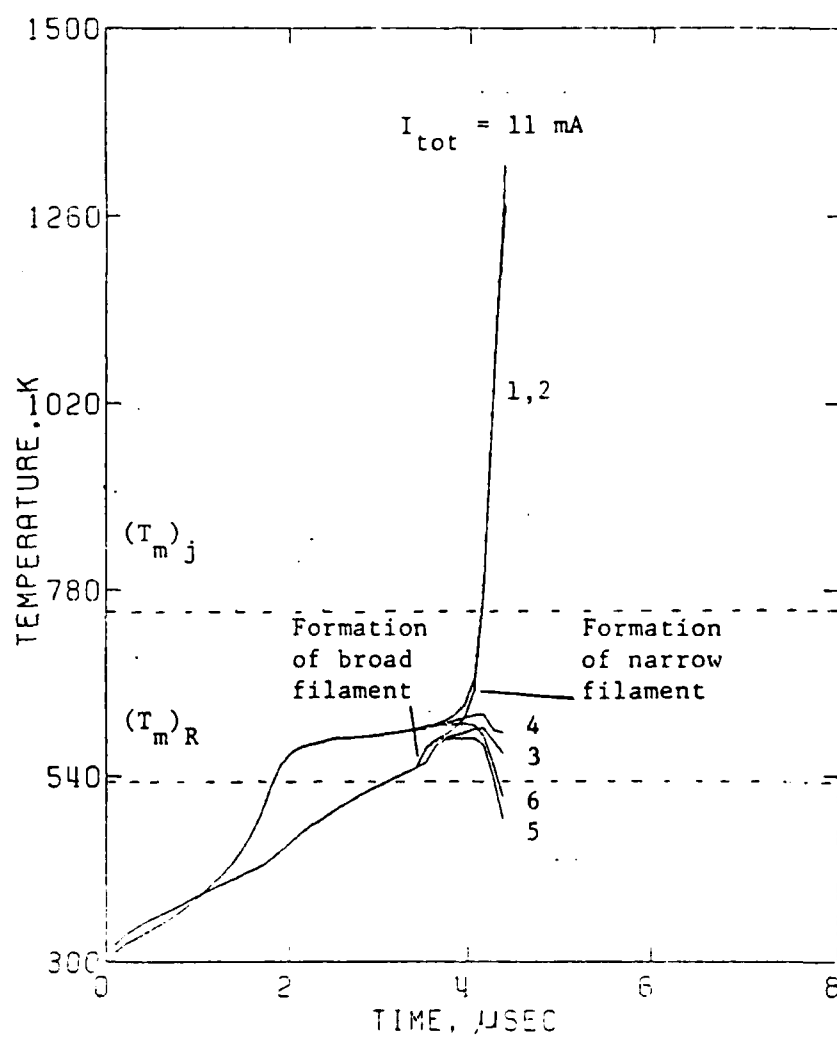


Fig. 120 (b)

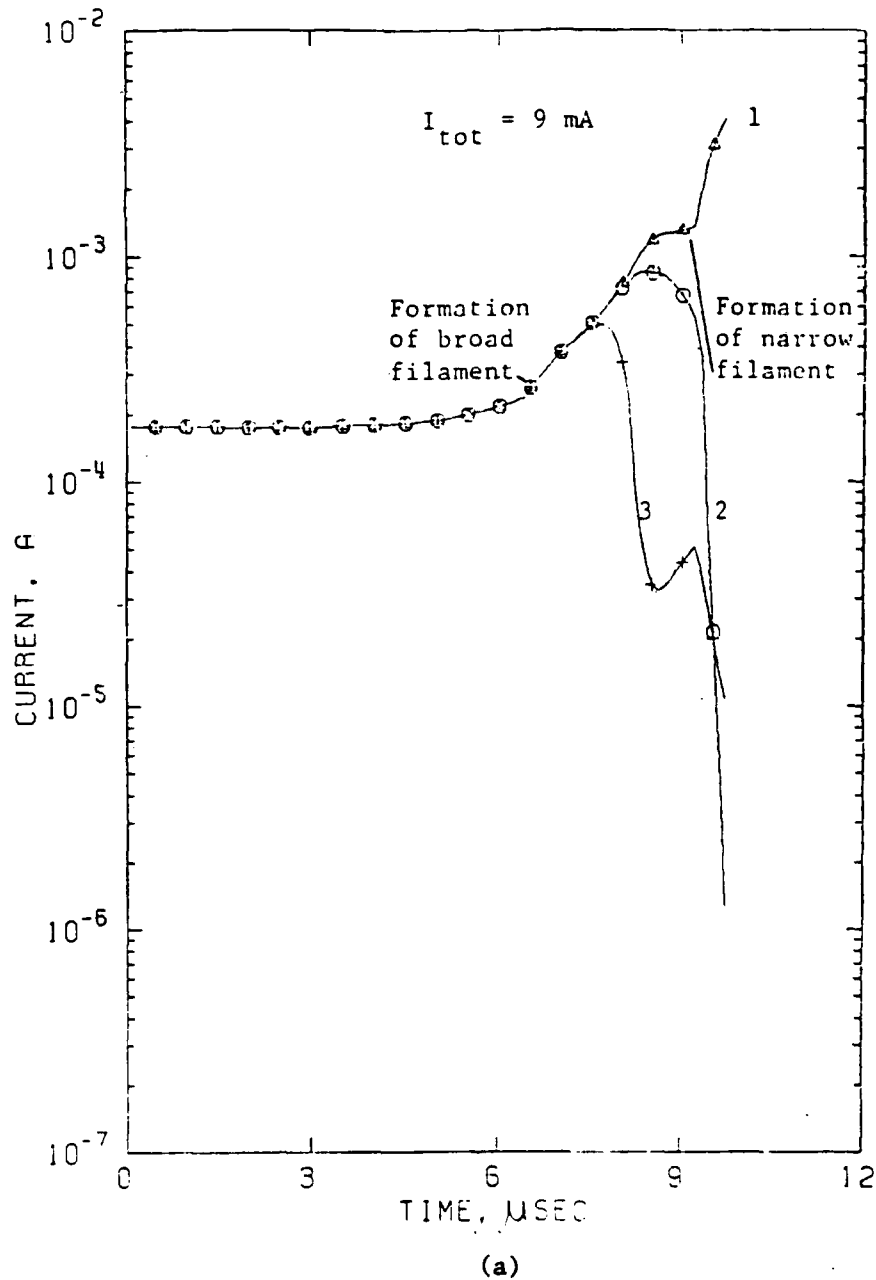


Fig. 121. Temporal development of current (1) at a filament site, (2) adjacent to a filament where the current is a minimum, and (3) at a site farther away from the filament. Pulse amplitudes are: (a) 9 mA, (b) 11 mA.

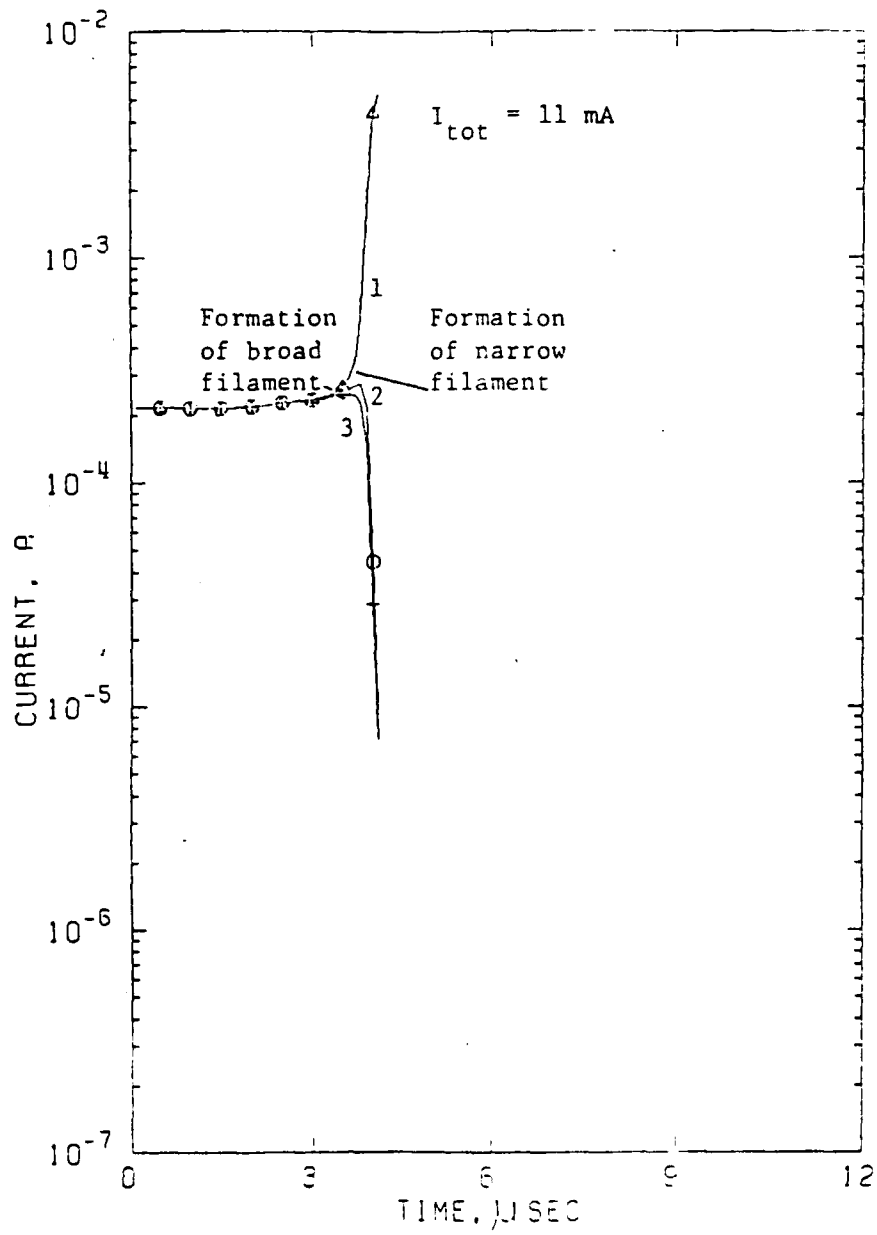


Fig. 121 (b)

and the n-region (5) and junction (6) of a strip farther removed from the current filament (86 μm from edge). In Fig. 120a, the knees in Curves 1,3,5 at 3.5 μs are associated with the transition of most of the n-region over $(T_m)_R$ (see Fig. 116b and the voltage waveform in Fig. 123). Once above $(T_m)_R$ less voltage is required to sustain the same current (see Fig. 121a), so the heating rate decreases. The formation of a broad filament starts at the inflection in the junction curves (Curves 2, 4, 6 of Fig. 120a). The temperature of the junction is then about 600 K, just slightly above that of the peak junction voltage at the current density of 10^8 A/m^2 . The voltage waveform of Fig. 123 experiences a change in slope toward lower voltages at this time. All of the curves of Fig. 120a are plausible if the location of the central filament is taken as the hottest part of the device throughout the pulse.

In Fig. 120b, the temperature-time histories are shown at sites of a filament (48 μm from diode edge) in a double filament system, at a nearby current minimum (44 μm from the diode edge), and at a locale further removed (32 μm from the diode edge). Examination of the temperature-time data of Fig. 120b reveals one significant feature: the temperature at the site of the double filament rises faster than at other parts of the diode just after its junction passes through the peak of the $V_{\text{jun}} - T(J = 10^8 \text{ A/m}^2)$ curve at 580 K. A runaway condition then causes the formation of the filament.

The time history of the current in the device is considered in Figs. 121a,b for the runs of Figs. 120a,b respectively. The same portions of the device as in Figs. 120a,b are analyzed: the filament

site (1), the site adjacent to the filament (2) where current is a minimum, and a site (3) farther away from the filament site. Initially, the current is distributed uniformly in all the three longitudinal strips considered. When the temperature in the n-region goes over $(T_m)_R$ in the filament strip, that strip takes a greater share of the total current. The current in the strip farther away from the filament (Curve 3) decreases correspondingly. The runaway condition is accelerated as the junction voltage drops at 760 K and as the intrinsic region is reached at about 810 K. The current in the strip adjacent to the filament (Curve 2) falls correspondingly, with its fall accelerated by its increasing resistivity as $(T_m)_R$ is approached from above.

Thus the picture that emerges is the following. During the early part of the pulse, the temperature distribution is nearly uniform in the junction except at the edges. Yet a very slight temperature gradient exists, with the center tending to be the hottest region. Thus current is forced from the center region outward. Depending upon the detailed time history in each region, it is possible for an outer location to become hotter than the central region. If this occurs as the outer region is passing through the peak of the junction voltage-temperature curve (see the 10^8 A/m^2 curve in Fig. 119), then more current is drawn into the outer region and a filament develops there rather than in the center of the diode. If the current amplitude is low, the rise in temperature in the outer region will occur until the current distribution becomes nearly uniform, but the bias produced by the cool edges will keep the central region the hottest part of the diode. When the current amplitude is very high, however, the hottest portion at the critical

transition at $V_{\max}$ can occur away from the center. The systematic movement of the spread in the locations of the two filaments with increasing pulse amplitude can now be understood.

Multiple filaments were described in the experiments of Refs. 18-20. The convergence of current lines at a junction nucleation site in a highly doped diode gives rise to a potential gradient parallel to the junction boundary. Accompanying the converging current lines is a spreading resistance. The further away that a current line is from the junction channel, the higher the spreading resistance of that line. Thus a condition is reached some distance from a filament where current lines will go straight across the device, through another portion of the junction, and not through the original channel. If the temperature at another junction position became high enough, then another filament would start at the new junction hot spot. However, the double filaments of the present model do not arise for this reason, but rather because of the delicate balance imposed by the shapes of the resistivity-temperature and junction voltage-temperature curves and the detailed temperature history of the entire n region. The present model does not include the convergence of currents from different strips. After some thought, it is believed that the present model cannot be readily modified to include convergence of current filaments.

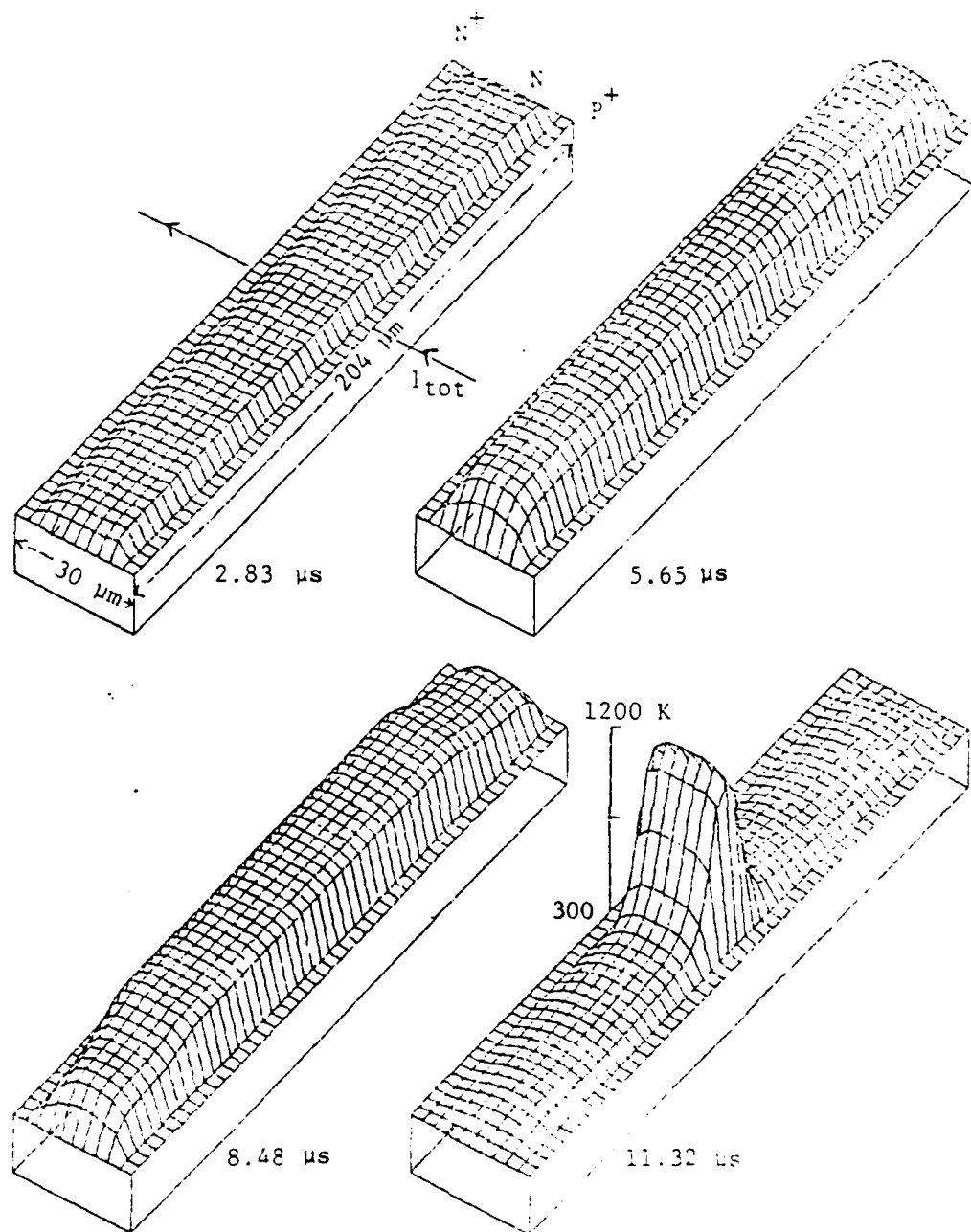
2. Temperature profiles

The electrical conductivity of the n^+ and p^+ regions is sufficiently high that these regions experience little temperature rise

during the times of interest. Thus the temperature profiles that follow will show only the junction and n region.

Figures 122a-f (Runs 1-6) contain temperature profiles for various excitation pulse amplitudes. The profile of Fig. 122a at $t = 5.65 \mu\text{s}$ shows that the temperature of the n region is almost uniform except at the edges. This temperature, 500 K, is close to the turnover temperature of the n region resistivity-temperature curve. As the pulse continues, the temperature difference between the central region and the edges becomes accentuated. The cooler regions move inward, while more and more current funnels through the hot central region. The resistivity of this central region continues to decrease and its width decreases, thus producing a filament. Inside the thermal filament shown in Fig. 122a at time $t = 11.32 \mu\text{s}$, the temperature is 1173 K while the cooler areas are at about 300 K. In other filaments, temperatures as high as 1480 K (melting point of silicon is 1683 K) have been calculated.

The final stages of the filament growth occur so rapidly that large changes in temperature take place during a single time step of the computation and in a space interval less than that of the spatial mesh. Calculations then become unstable. However, it is not fruitful to reduce the time step and spatial mesh sizes to prevent this instability since the computation time then becomes prohibitive. Experiments show that the temperature rapidly rises until the center of the filament melts. The melt has a conductivity about 20 times that of the high temperature solid and it permanently damages the device.



(a) $I_{\text{tot}} = 8 \text{ mA}$.

Fig. 122. Temporal development of temperature profiles for different step amplitudes. Current amplitudes are: (a) 8 mA, (b) 9 mA, (c) 10 mA, (d) 10.5 mA, (e) 11 mA, (f) 12 mA.

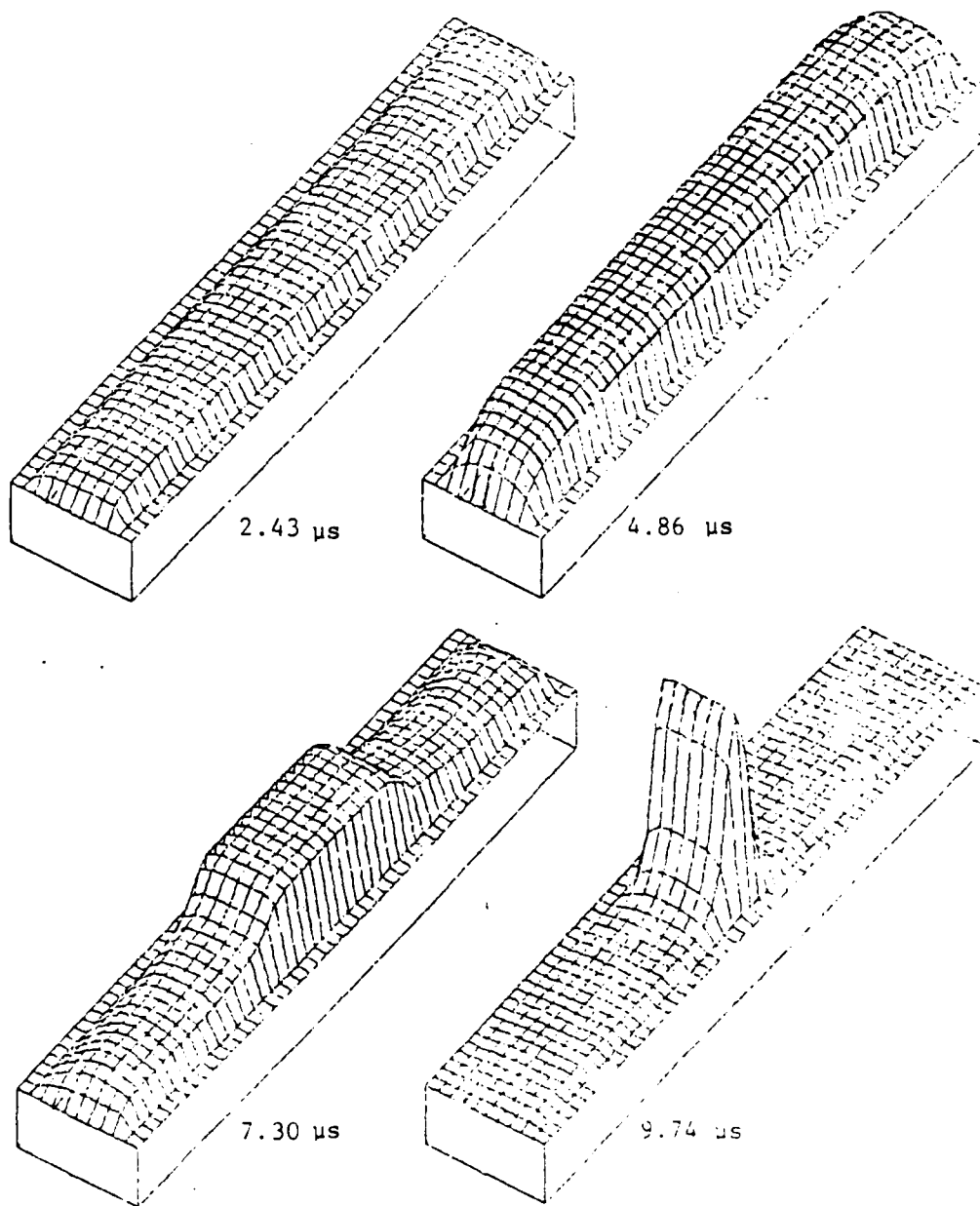


Fig. 122 (b) $I_{\text{tot}} = 9 \text{ mA}$.

347

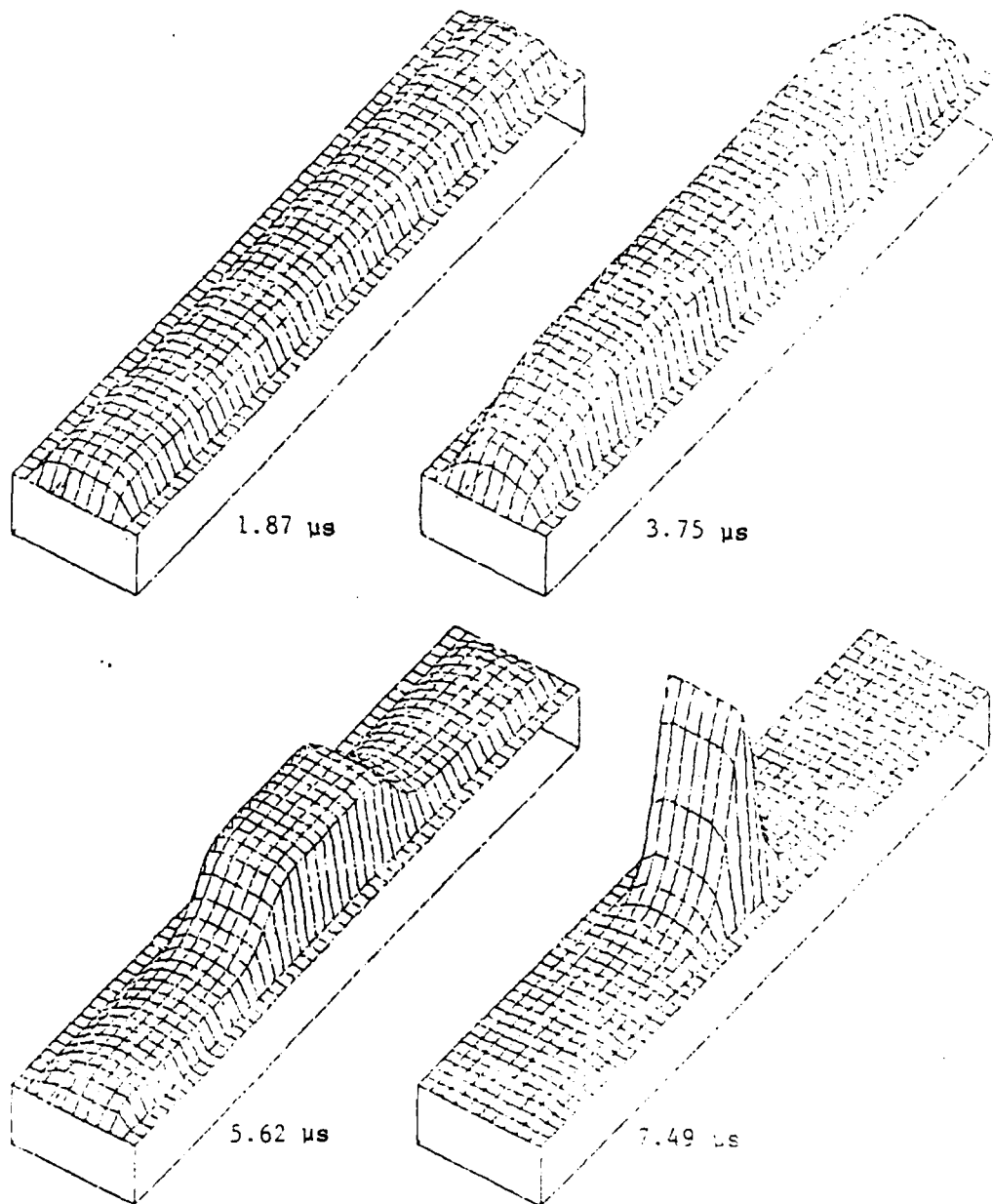


Fig. 122 (c) $I_{\text{tot}} = 10 \text{ mA}$.

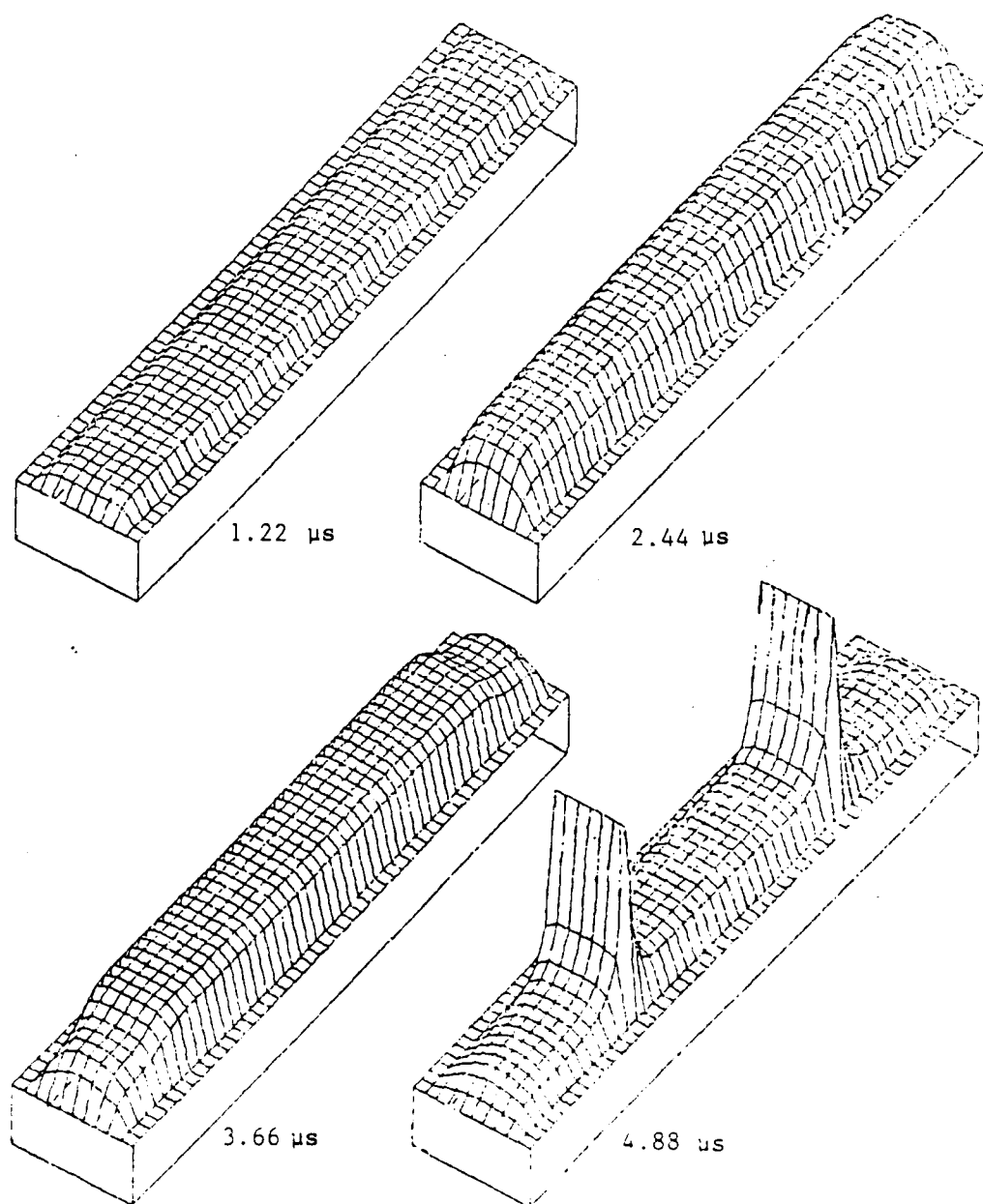


Fig. 122 (d) $I_{\text{tot}} = 10.5 \text{ mA}$.

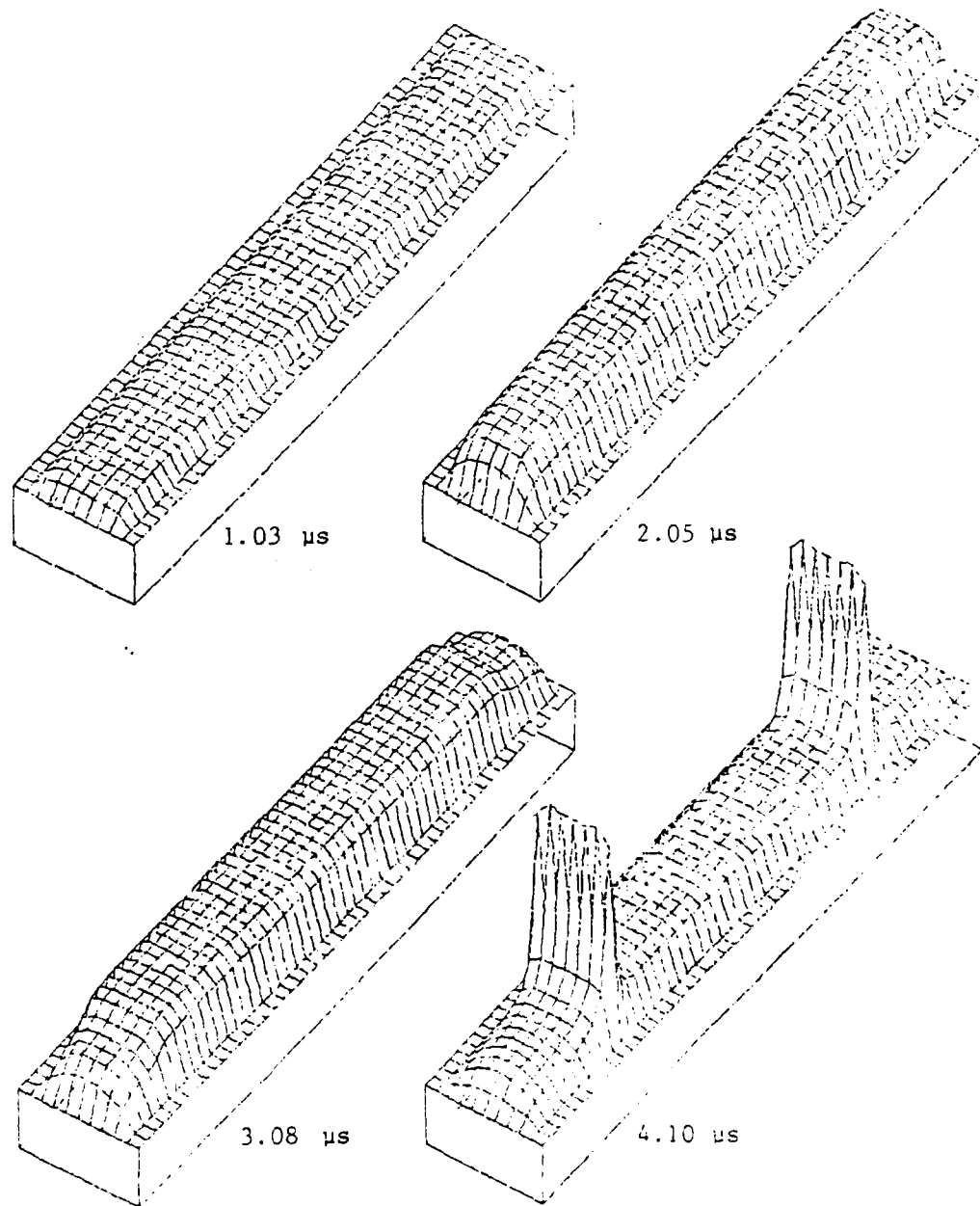


Fig. 122 (e) $I_{\text{tot}} = 11 \text{ mA}$.

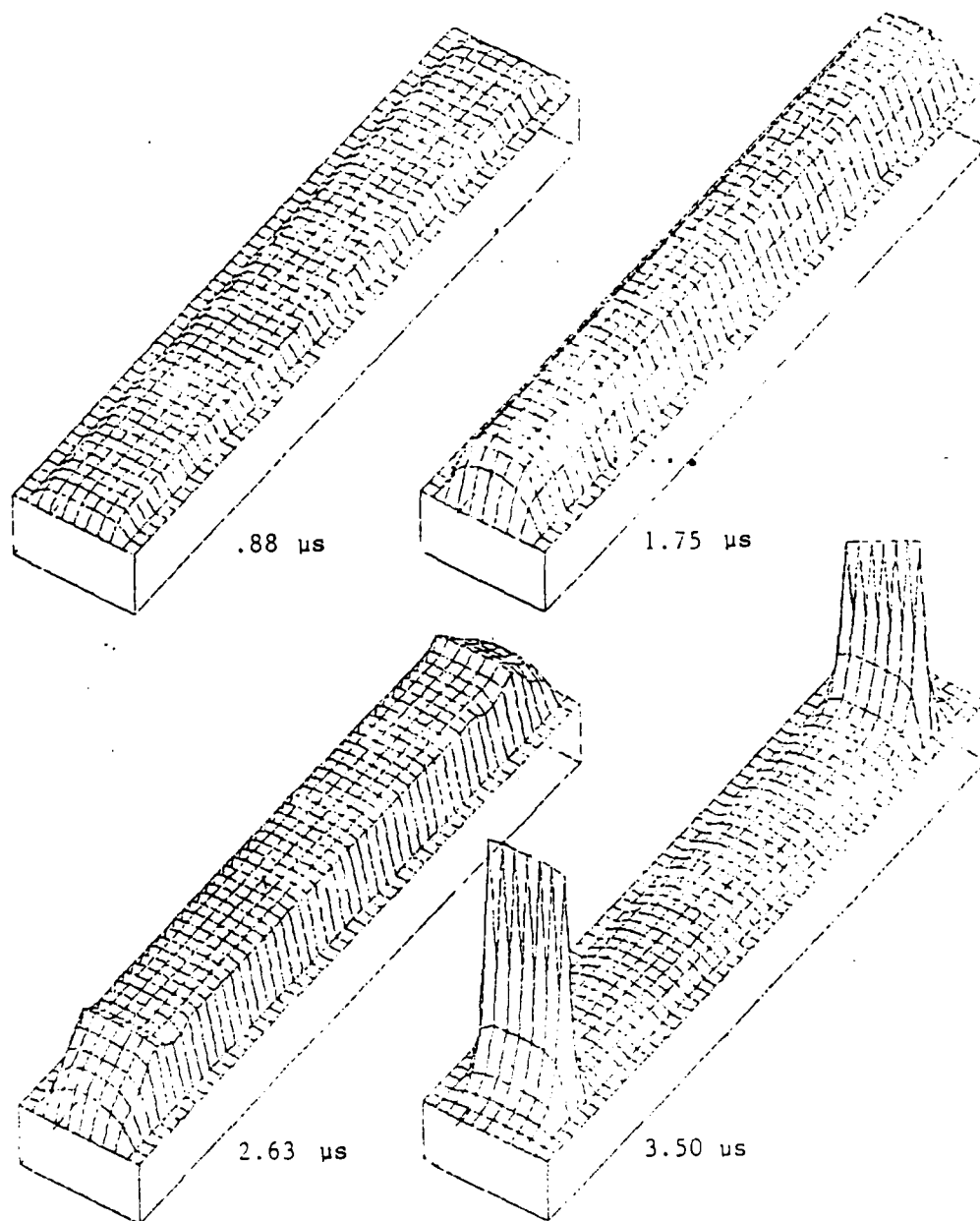


Fig. 122 (f) $I_{\text{tot}} = 12 \text{ mA}$.

3. Voltage waveforms

Figure 123 shows the temporal growth and ultimate collapse of device terminal voltage of Run 1 at an amplitude of 8 mA. The J-V-T behavior of the junction, the resistivity-temperature curve (Fig. 119) of the bulk region characteristics determine the details of the filamentation process. Their influence can be seen in the voltage waveforms in which three regions and a fixed point called the turnover point can be distinguished. Initially, the device voltage rises due to curtailed ionization in the junction region and the positive slope of the ρ -T curve. A state of almost uniform heating is maintained during this interval (see Fig. 122a at times 2.83 μ s and 5.65 μ s). Attainment of the peak of the resistivity curve next defines a voltage maximum (V_{peak}). Immediately after this peak the resistivity begins to fall, and a broad filament initiates and develops, accompanied by a gradual voltage drop. This is the second stage of filamentation. The third stage is characterized by an almost vertical drop in voltage as the current filament narrows, rising rapidly both in current density and temperature. As indicated earlier, the formation of the melt channel, which is the destructive stage of second breakdown, could not be achieved in the computer simulation. This transition, however, is accompanied by an abrupt drop in voltage because the resistivity decreases by a factor of about 20 in the melt transition.

The influence of the junction will be examined in Fig. 123. Soon after time $t = 0+$, the junction region attains a temperature of 315 K while the rest of the n-region lags at 306 K (Region A). The trend

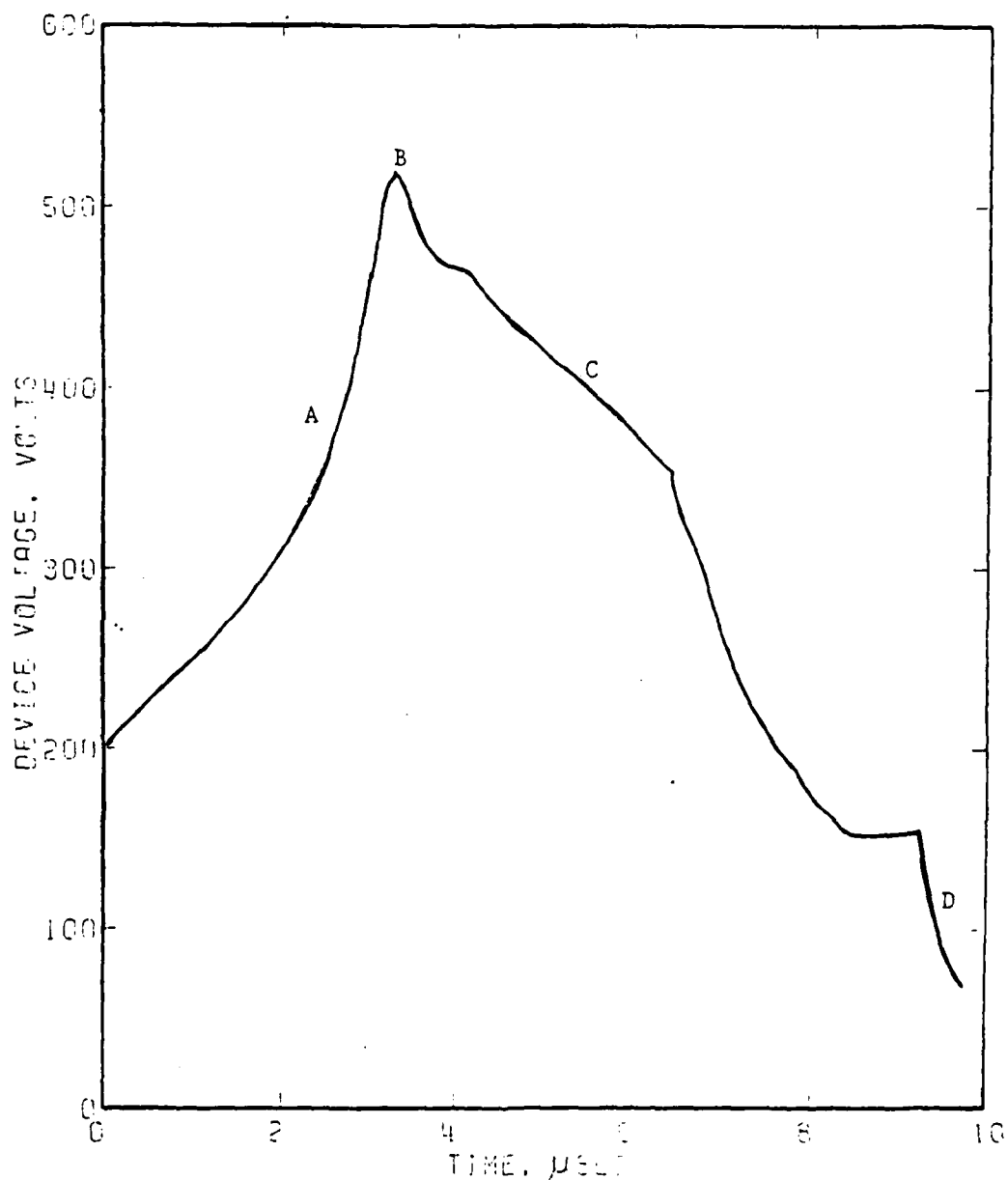
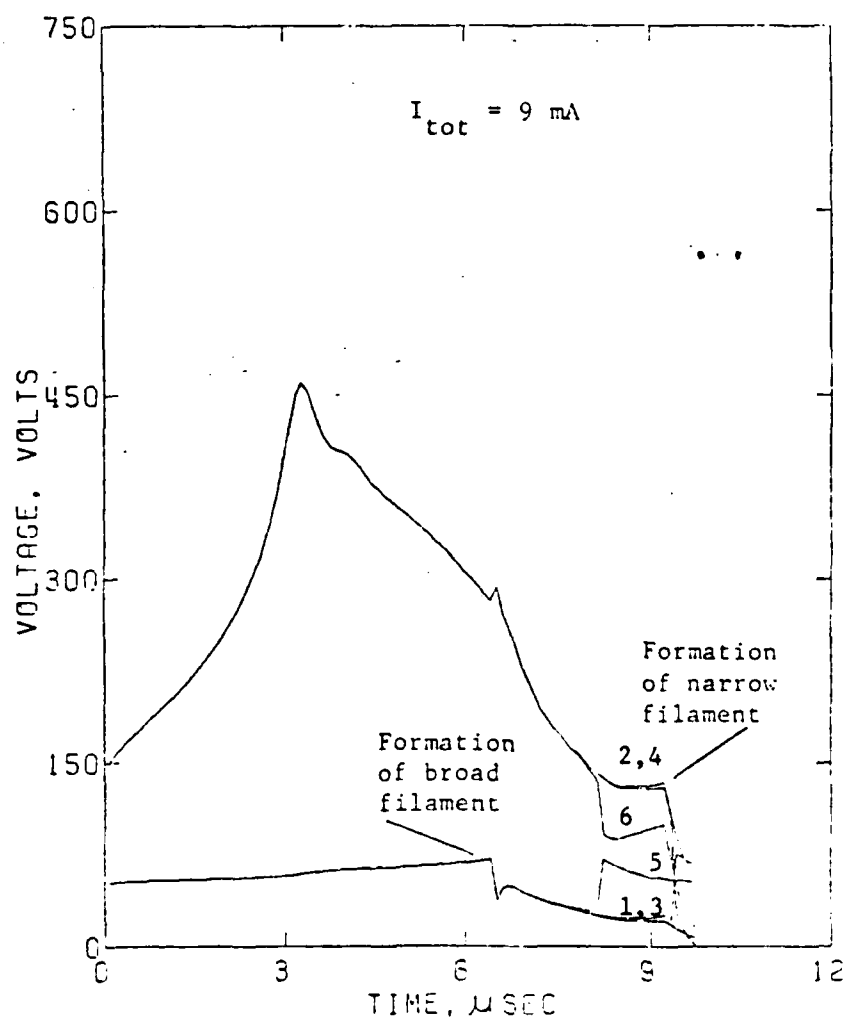


Fig. 123. Voltage waveform for a constant current pulse of 9 mA. The rise in voltage in region A is associated with the rises in n-region resistivity and junction voltage with increasing temperature. The n-region resistivity reaches its maximum value at B. In region C the broad filament forms, and in region D the narrow filament grows.

continues at first, but the increase in n-region resistivity with constant pulse current causes the n region to become hotter than the junction at 3.29 μs . When the n region reaches the turnover temperature (Point B) at 5.10 μs , with the device voltage peaking at 463 V, the junction is still not sufficiently hot for its voltage to drop appreciably. In Region C, the junction voltage changes only slightly. The junction voltage at the location of the filament drops sharply toward zero at $t = 10.04 \mu\text{s}$, the onset of Region D.

Figure 124 a (Run 2, $I_{\text{tot}} = 9 \text{ mA}$, $J_{\text{AVG}} = 7.5 \times 10^7 \text{ A/m}^2$), shows the time history of the n region (1) and junction (2) voltages at a central filament site (102 μm from edge), n region (3) and junction (4) voltages at a site adjacent to the filament where current is a minimum (94 μm from edge), and n region (5) and junction (6) voltages at a site farther away from the filament (86 μm from edge). These are the locations discussed earlier in connection with Figs. 120a and 121a. The abrupt drop in both junction voltages at 6.5 μs is associated with passing over the maximum of the upper ($J = 10^8 \text{ A/m}^2$) V_{jun} -temperature curve of Fig. 119. The abrupt rise in junction voltage at a site away from the filament is associated with the growth of the broad filament. This growth reduces the current elsewhere, leading to a rise in junction voltage as the temperature drops toward that of V_{peak} and a fall in n-region voltage. The latter is the combined effect of less current, but increasing resistivity as cooling proceeds above $(T_m)_R$. The narrow filament begins at about 8 μs as the junction voltage drops in the filament strip. Figure 124b shows the time history of the junction



(a)

Fig. 124. Voltage waveforms at the junction (1) and across the n region (2) at a filament site, junction (3) and n region (4) at a site adjacent to a filament, and junction (5) and n region (6) at a site farther away from the filament. Current amplitudes are: (a) 9 mA, (b) 11 mA.

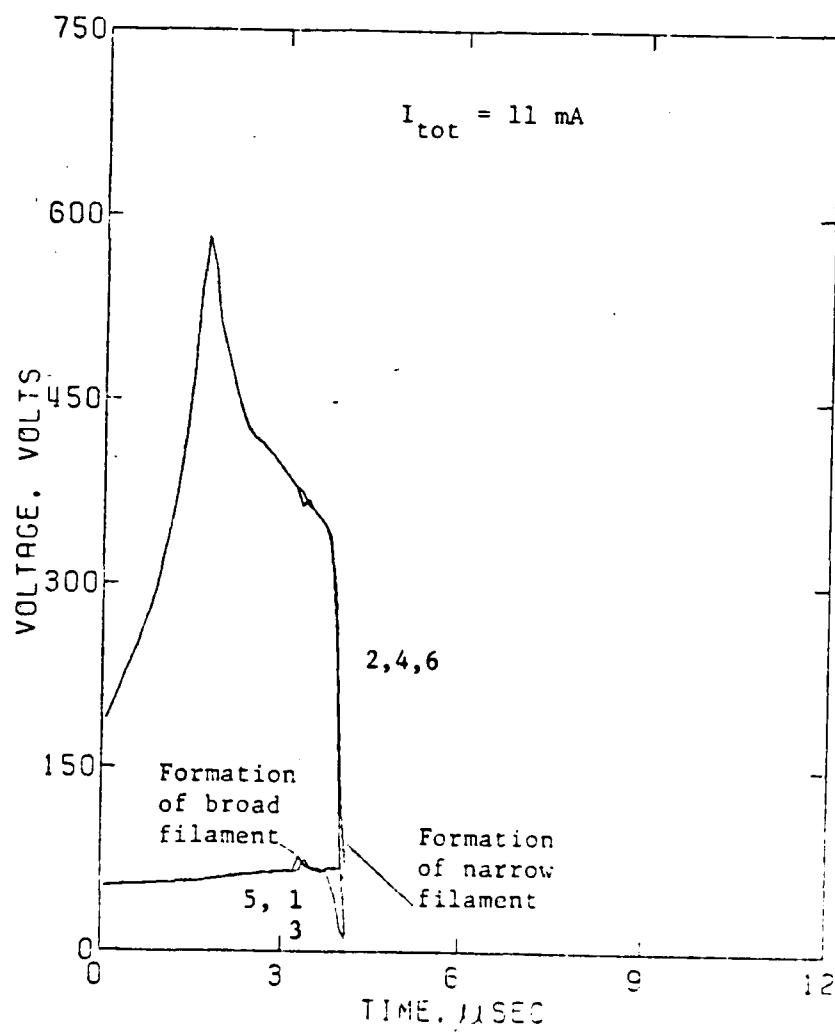


Fig. 124 (b)

and n-region voltages for an increased excitation amplitude of 11 mA. The sites of interest are the n region (1) and junction (2) at the filament (48 μm from the edge), the n region (3) and the filament (4) adjacent to the filament (44 μm from the edge), and the n region (5) and the filament (6) farther away from the filament (32 μm from edge). The positions are those of Figs. 120b and 121b.

Figure 125 (Runs 1-6) shows the voltage waveforms for various excitation pulse amplitudes as functions of time. All waveforms have the same general features. High amplitude, short duration current pulses are accompanied by voltage pulses with high peak values.

4. Time delay for onset of filamentation and for instability

The temperature-time history of each portion of a device depends on the balance between energy input and heat conduction from that portion. The observation that there is always a delay time before second breakdown occurs led to the idea that some minimum amount of energy, called the "triggering energy", must be dissipated in the device before second breakdown will occur (1). Thus a delay time has been defined as the time between the application of a large amplitude pulse and the onset of second breakdown. The critical energy is associated with the heat capacity of the n region and the peak of the temperature-resistivity curve. In this study, two types of delay times have been distinguished, one for the onset of filamentation (τ_{fil}) and the other for instability (τ_{ins}). Two reference levels, one each for the two delay times, have been chosen arbitrarily and are shown below in Table 19.

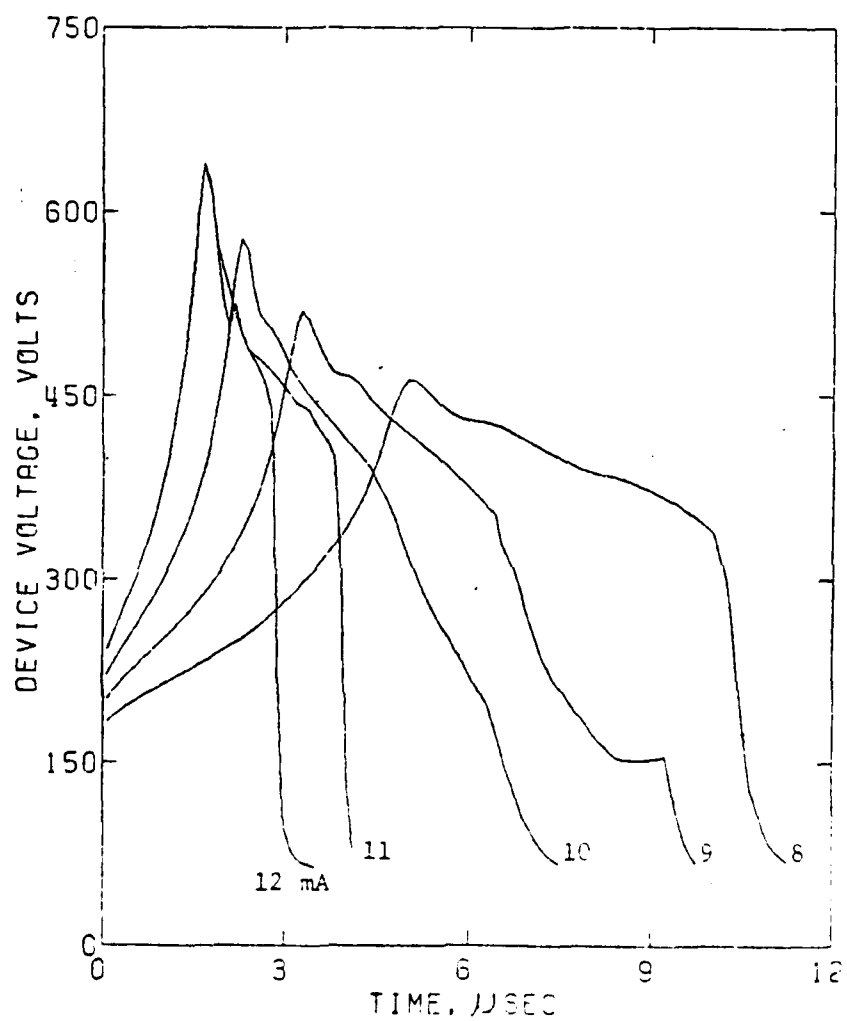


Fig. 125. Voltage waveforms for pulse amplitudes in the range 8 - 12 mA.

TABLE 19
REFERENCE LEVELS FOR DELAY TIMES

Run No.	Film Thickness (μm)	Pulse Amplitude (mA)	Applied Current Density (10^9 A/m^2)	Reference Level for Filamentation (10^9 A/m^2)	Reference Level for Instability (10^9 A/m^2)
1	.6	8	.065	.130	1.30
2	.6	9	.073	.146	1.46
3	.6	10	.082	.164	1.64
4	.6	11	.090	.180	1.80
5	.6	12	.098	.196	1.96
18	1.2	21	.086	.172	1.72

Delay time τ_{fil} is defined as the time at which the current density inside the filament increases by a factor of 2 over the average current density, and τ_{ins} is defined as the time at which the current density increases by a factor of 20 over the average current density.

Figure 126 shows the delay times as functions of applied pulse amplitude. The time delays decrease approximately linearly as amplitude increases. The time between the onset of filamentation and the onset of instability was greatly reduced for double filaments.

Each of the set of curves in Figs. 127a-d compare current distributions at fixed times using the data of Runs 1-6. Thus in Fig. 127a, the configurations are given at time $t = 3.5 \mu\text{s}$ for current amplitudes of 8-12 mA. These are the configurations that would occur if each pulse were terminated at $3.5 \mu\text{s}$. Figs 127a-d cover pulse lengths of 3.5, 4.1, 7.5, and $9.7 \mu\text{s}$. It is seen that pulses of shorter durations can sustain higher current amplitudes. This lends weight to the concept of a minimum energy input required for the second breakdown

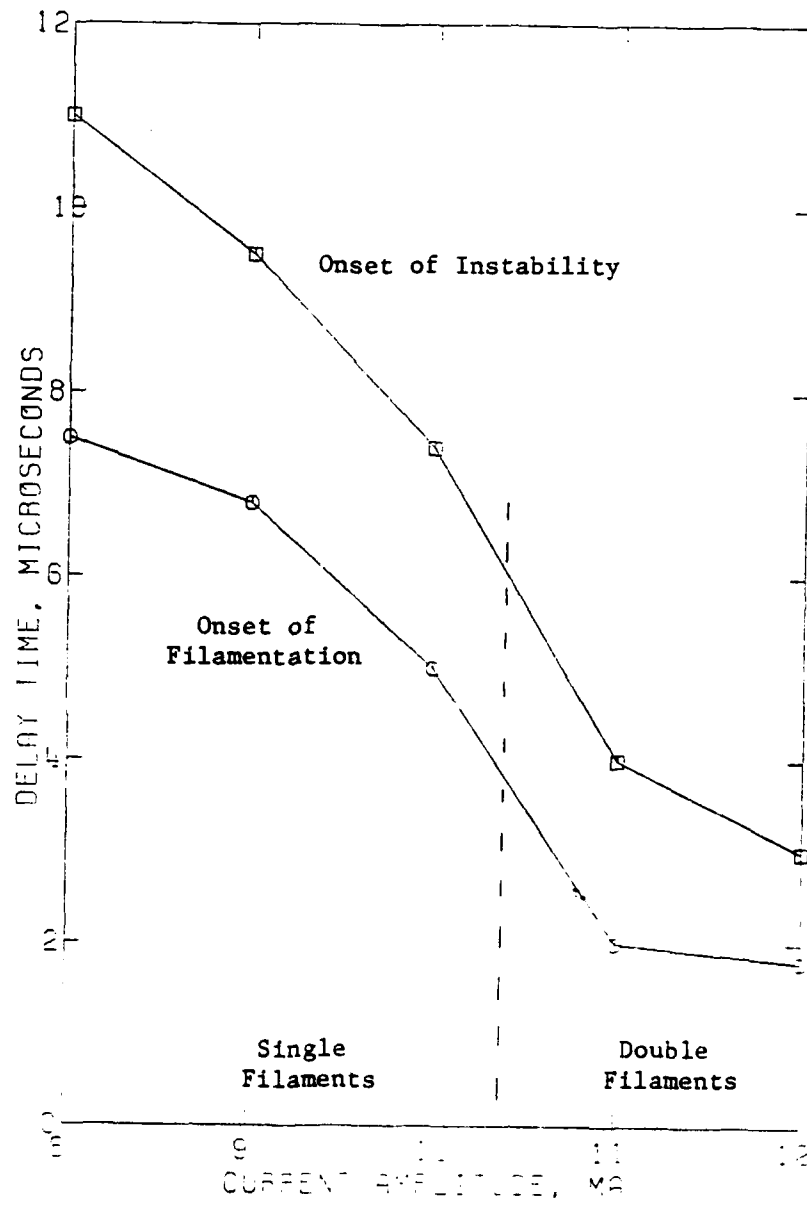


Fig. 126. Delay times for the onset of filamentation and for the onset of instability for different pulse amplitudes.

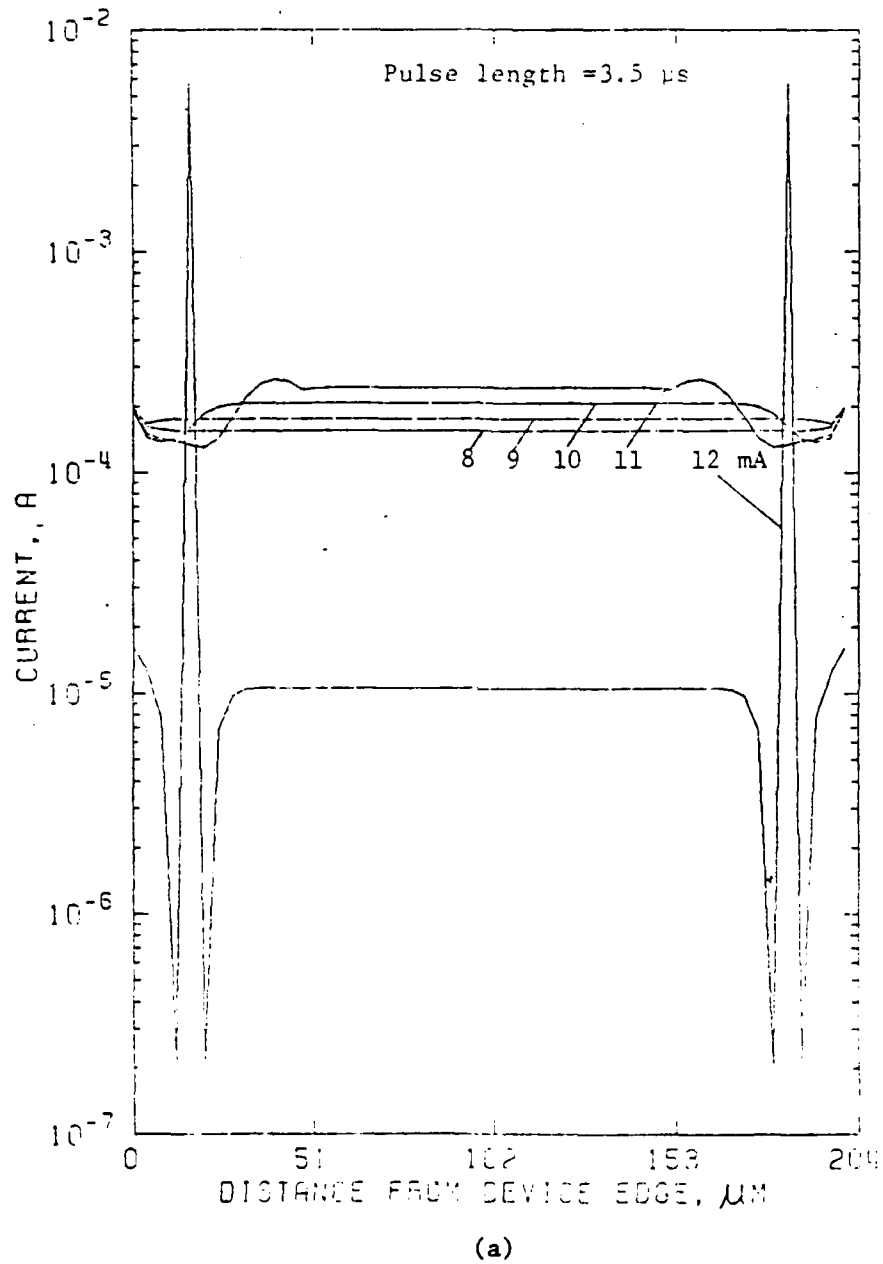


Fig. 127. Effect of pulse amplitude on current distributions at constant pulse length. Pulse lengths are: (a) 3.5 μ s, (b) 4.1 μ s, (c) 7.5 μ s, (d) 9.7 μ s.

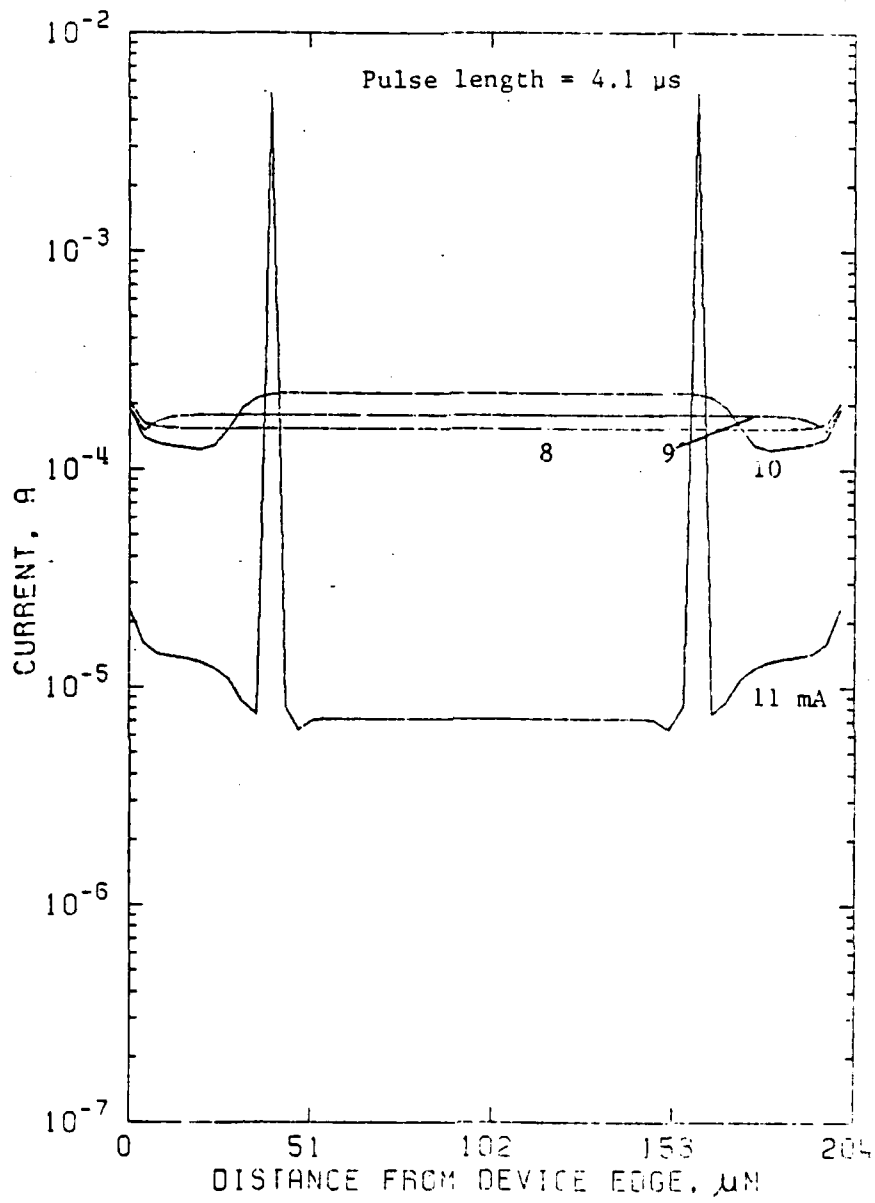


Fig. 127 (b)

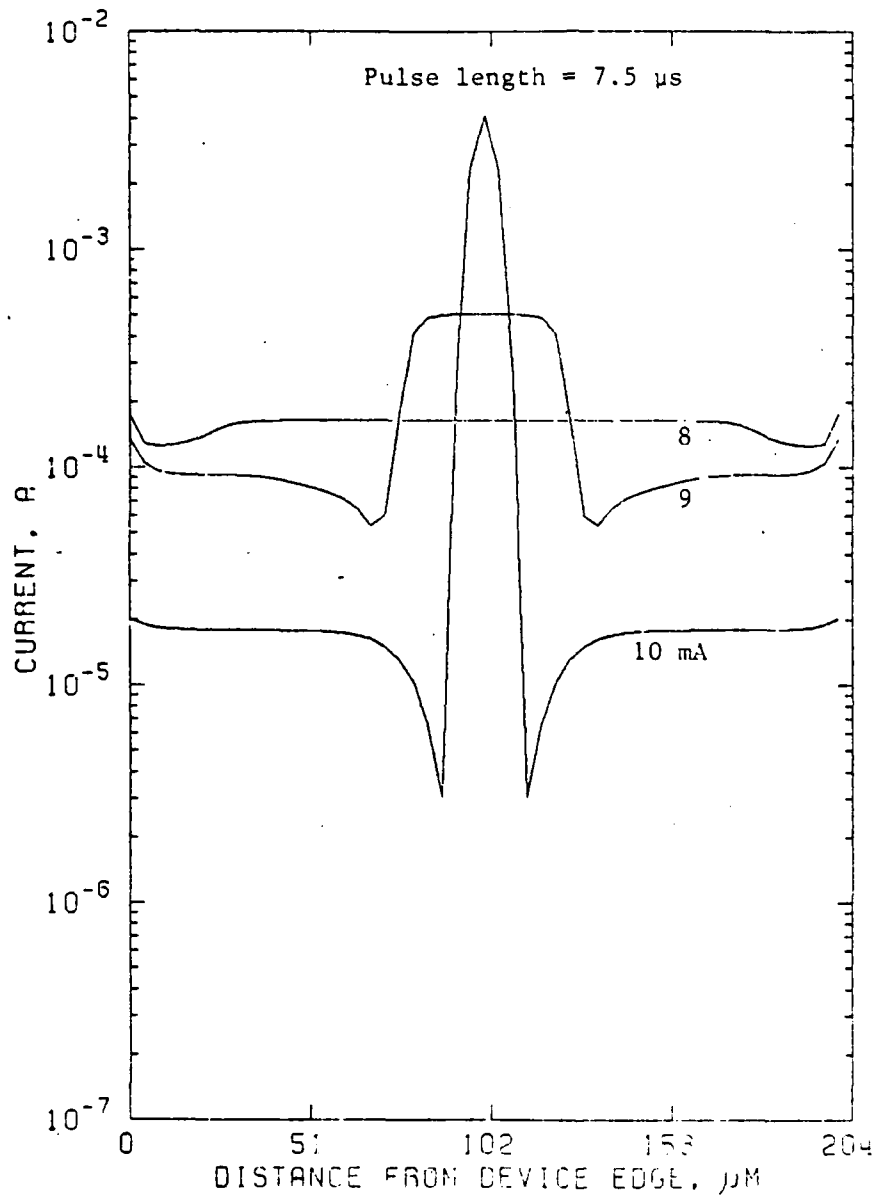


Fig. 127 (c)

AD-A086 345

AUBURN UNIV ALA DEPT OF PHYSICS

F/G 9/1

SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)

MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAAG29-78-6-0111

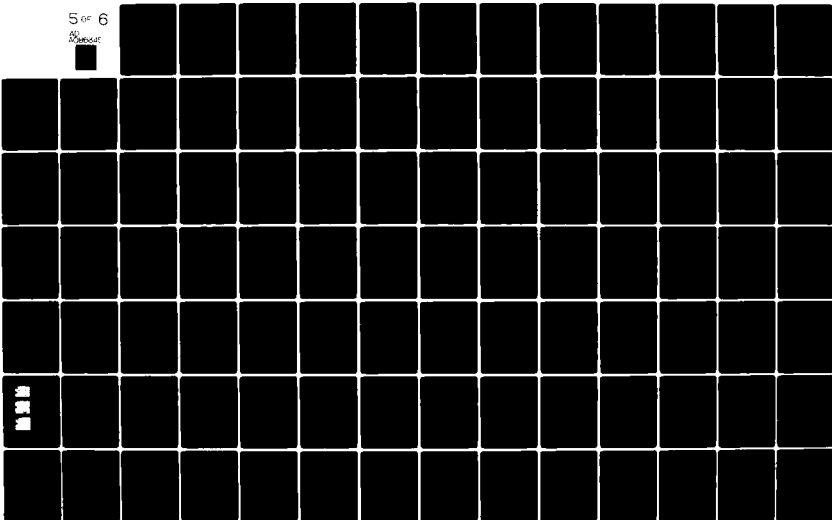
ARO-15840.3-A-EL

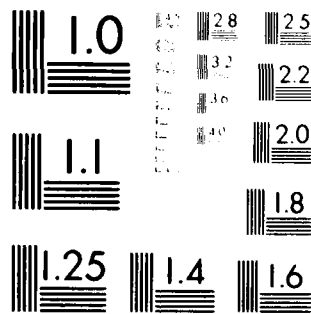
NL

UNCLASSIFIED

5 of 6

5 of 6





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

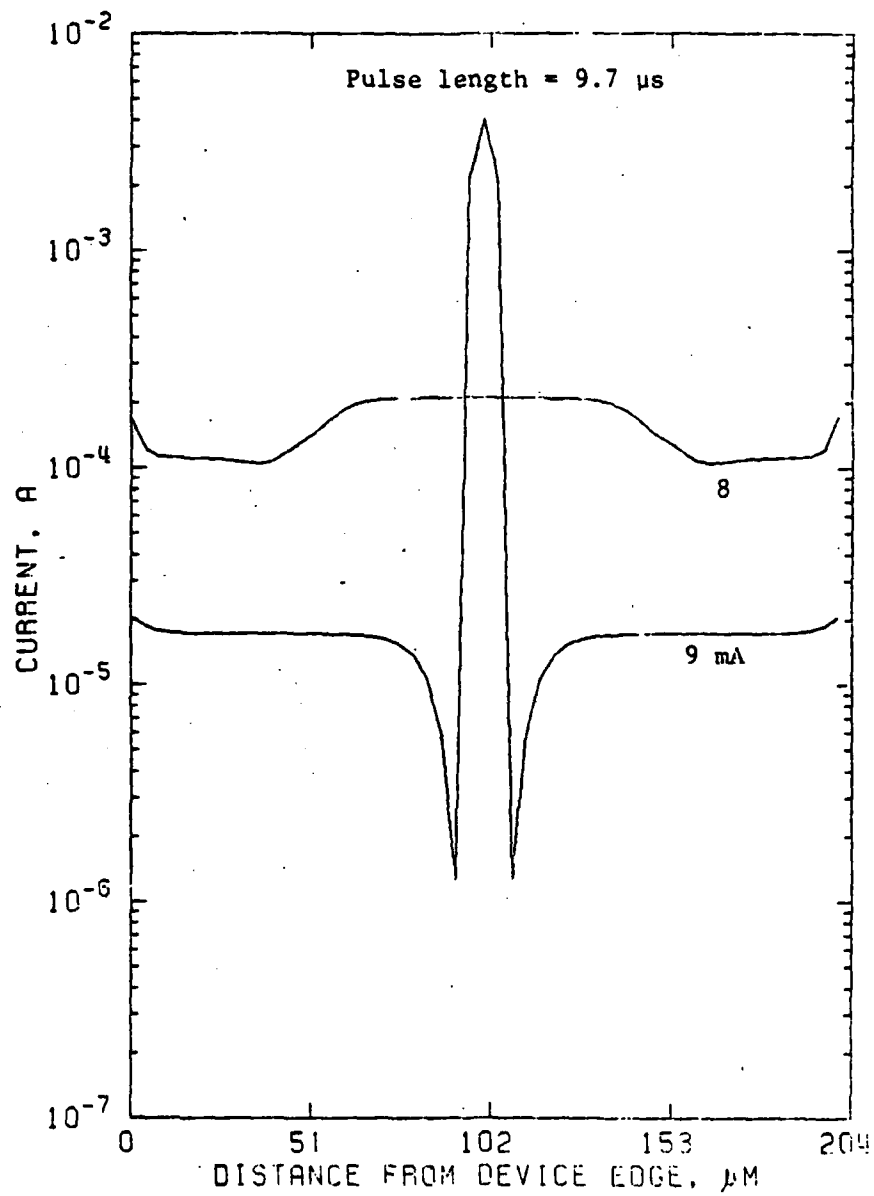


Fig. 127 (d)

transition. For a given current, the input energy for the onset of filamentation and for instability are computed by evaluating the energy added to the device prior to the characteristic times, τ_{fil} and τ_{ins} , respectively. Figure 128 shows the input energies as functions of the square root of delay times. As the delay time increases, the energy requirement for filamentation and for instability increases. Once filamentation has been initiated, only a small additional amount of energy is required to reach the runaway condition.

5. Double step pulses

In the experiments of Ref. 64, the filamentation pattern varied with pulse amplitude. The calculations here on uniform specimens have yielded single and double filaments at low and high current densities, respectively. In the experiments, some tests were made with pulses that had an initial rise to one amplitude, then a rise to a second level. The filamentation pattern changed from that characteristic of the first level to that of the second level, the transition occurring during the thermal constant of the system - a few microseconds. Also, the results of a double-step current pulse give a perspective on the behavior of the device if a constant voltage pulse were applied. As heating occurs in a constant voltage pulse, the current will first decrease. At sufficiently high temperatures, however, the current would rise. A two-step current pulse during filamentation can thus be used to approximate a constant voltage pulse.

Three cases of applied two-step current pulses were investigated, with step heights of 9-11, 10-10.5 and 10-11 mA. In each case, the

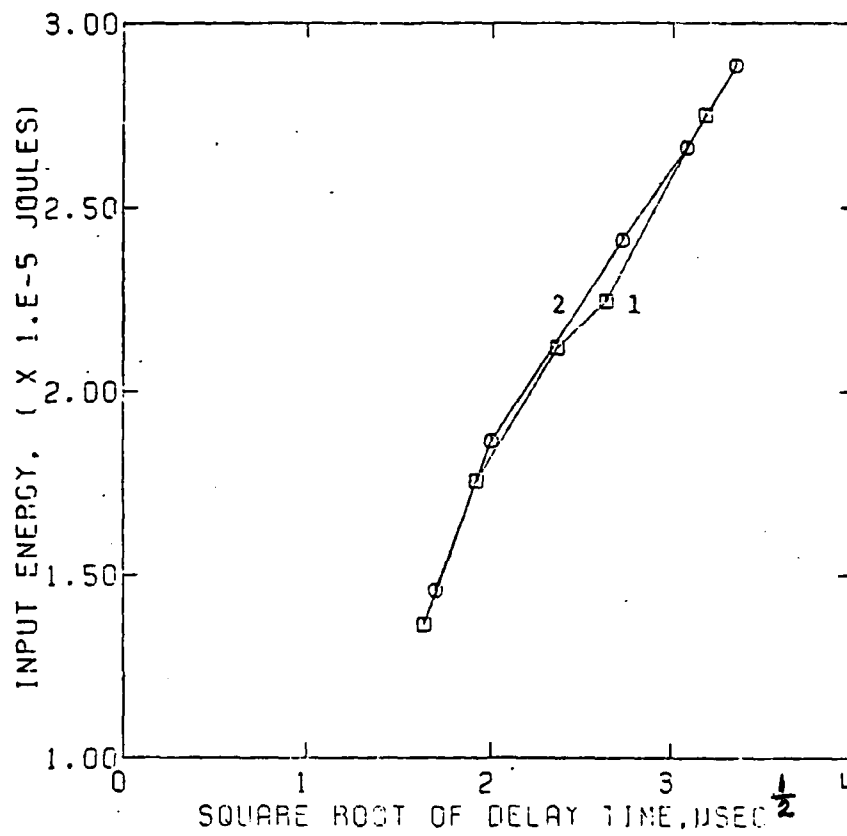


Fig. 128. Input energy for the onset of filamentation (1) and for the onset of instability (2) as a function of the delay times, τ_{fil} and τ_{ins} , respectively.

second step was added at a time after the voltage peak was reached. The lower step amplitudes were chosen for their single filament property when acting alone, while the higher steps were chosen because they displayed double filaments when applied alone. A representative, double-step current waveform is shown in Fig. 129 while current distributions are given in Figs. 130-132 for Runs 7-9. It is apparent that application of the second step at such an advanced stage of filamentation does not affect the original current distribution to any noticeable extent. Delay times τ_{f11} and τ_{ins} are shorter for a double-step pulse when compared to the corresponding delay time of the second level when acting alone. For example, in the case of 9-11 mA double-step, delay time τ_{f11} is 6.92 μ s. But when single step pulse of 11 mA is applied, the equivalent delay time is 3.70 μ s. Only single filaments are obtained in each case. Thus, for the conditions employed, the filamentation pattern for constant current and constant voltage pulses is similar.

B. Diode with spikes on the p⁺n junction

1. Current distributions

Filamentation in SOS diodes with deliberately introduced junction spikes is being studied experimentally concurrently with the present work. The experimental devices have triangular spikes. To simulate these diodes the geometry of Fig. 133 is used. For ease in computer programming, the spike head was made flat instead of being pointed as is the case in actual diodes. In the present model, which does not allow for current convergence across strips, there is no effect of a

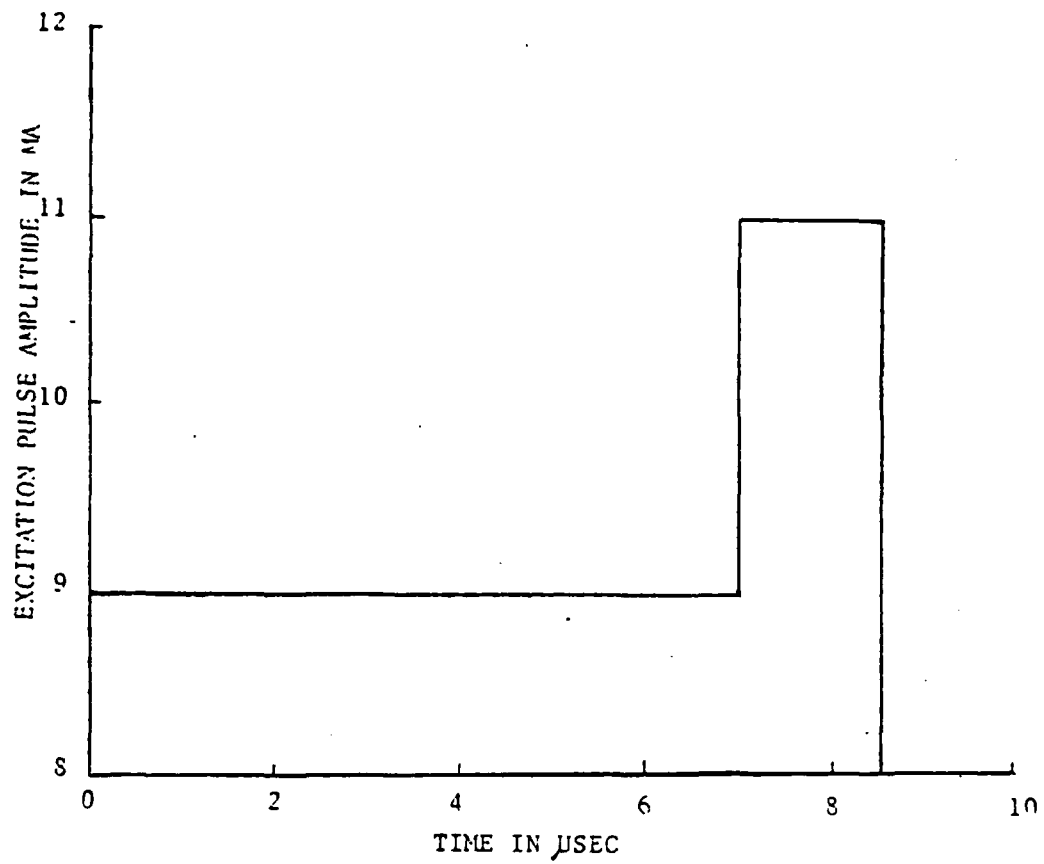


Fig. 129. A representative double-step current waveform.

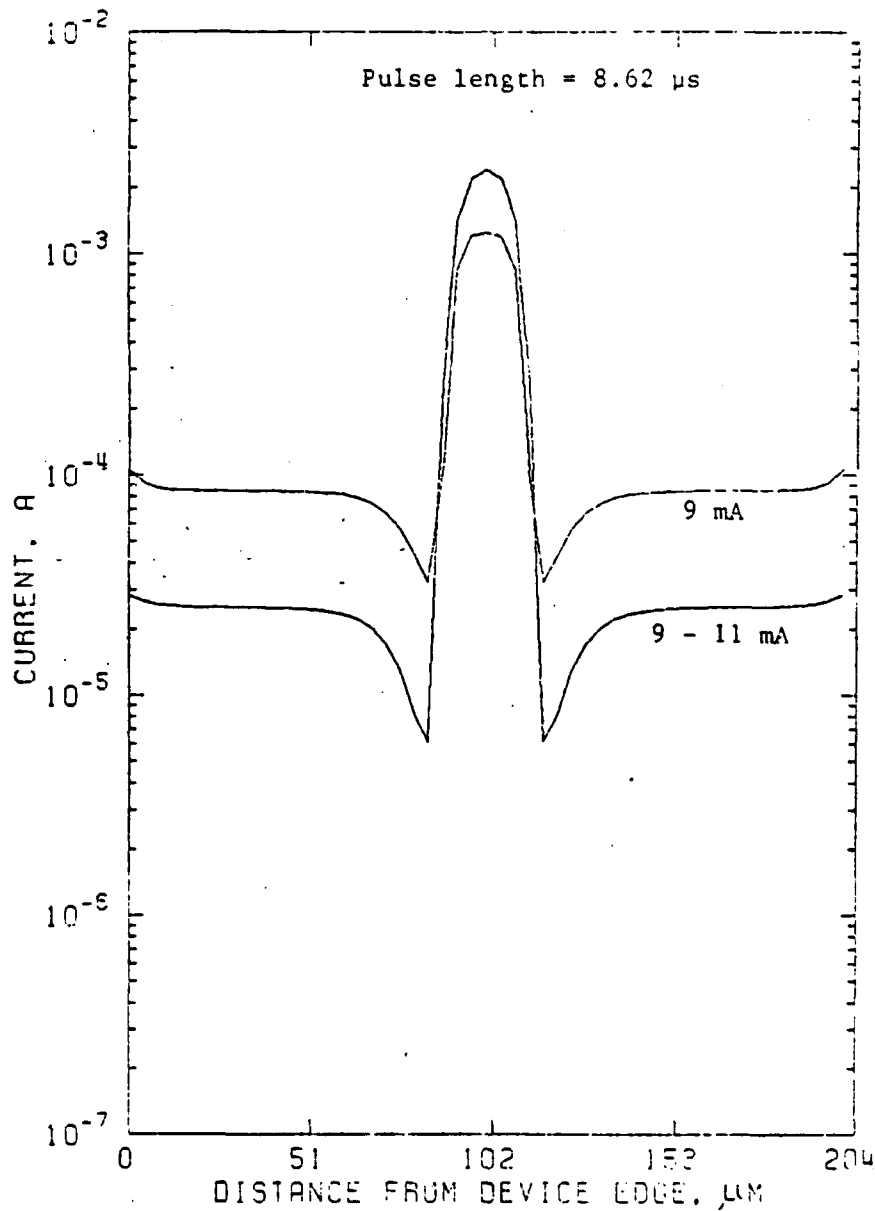


Fig. 130. Current distributions for single and double step pulses of the same duration. The single step pulse has an amplitude of 9 mA and a duration of 8.62 μ s. The double step has an amplitude of 9 mA for the first 6.90 μ s and an amplitude of 11 mA for an additional 1.72 μ s.

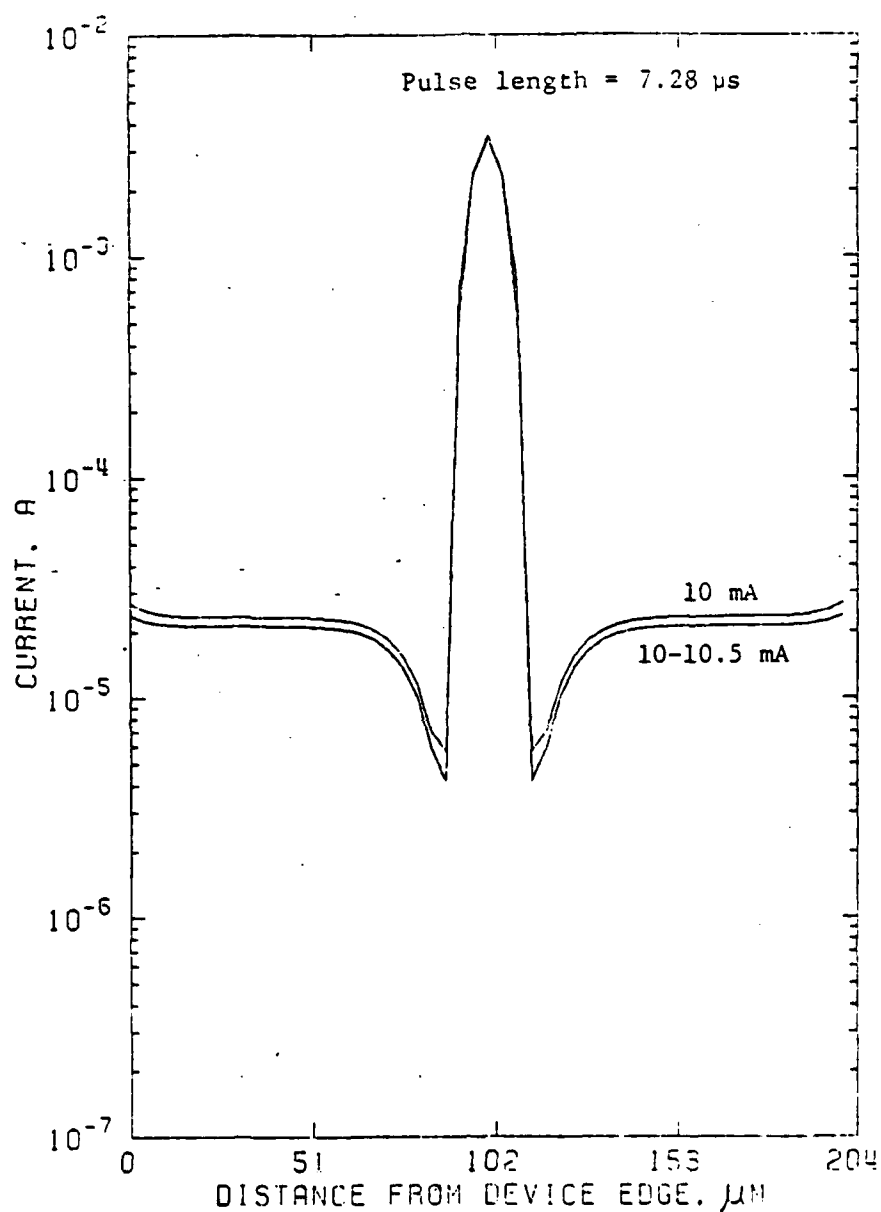


Fig. 131. Current distributions for single and double step pulses. The single step pulse has an amplitude of 10 mA and a duration of 7.28 μs . The double step pulse has an amplitude of 10 mA for the first 4.89 μs and an amplitude of 10.5 mA for another 2.39 μs .

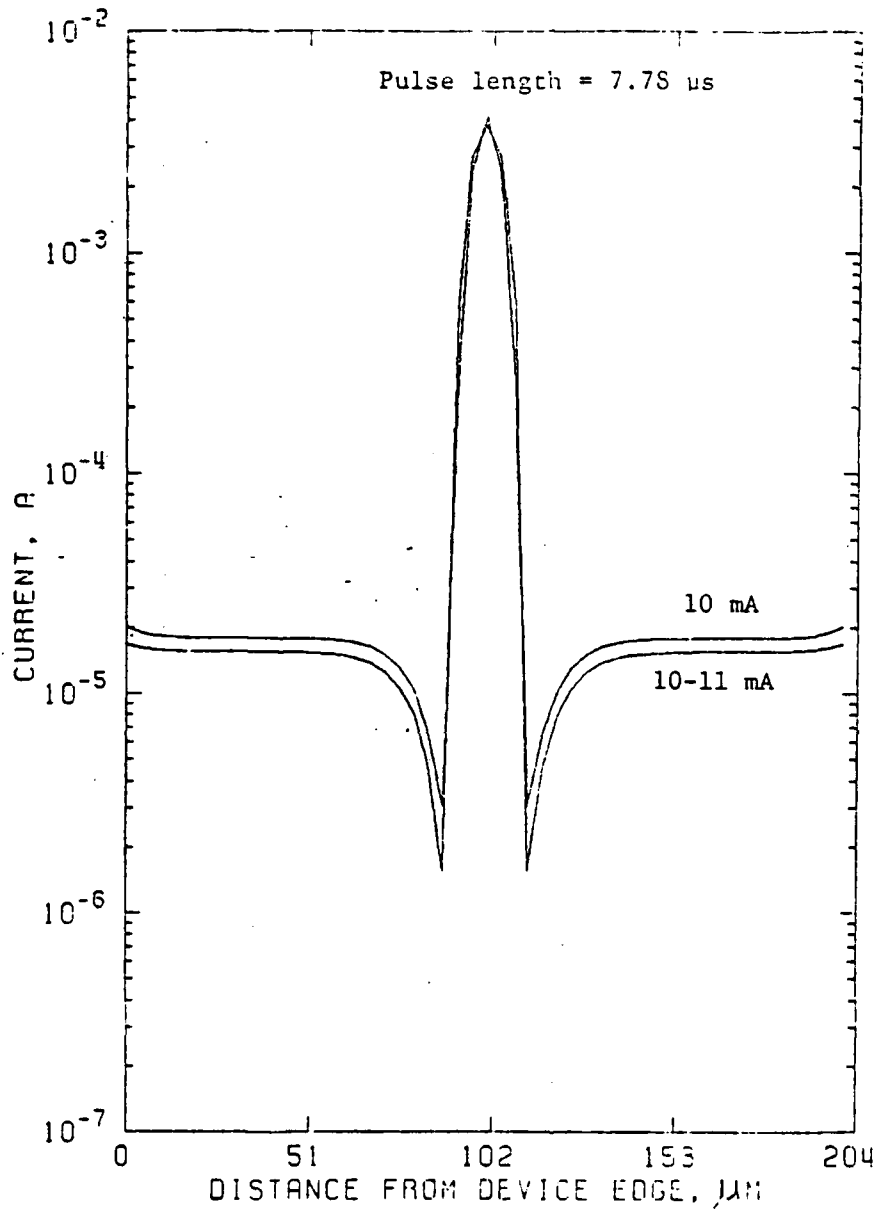


Fig. 132. Current distributions for single and double step pulses of the same duration. The single step pulse has an amplitude of 10 mA and a duration of 7.78 μs . The double pulse has an amplitude of 10 mA for the first 6.49 μs and an amplitude of 11 mA for another 1.29 μs .

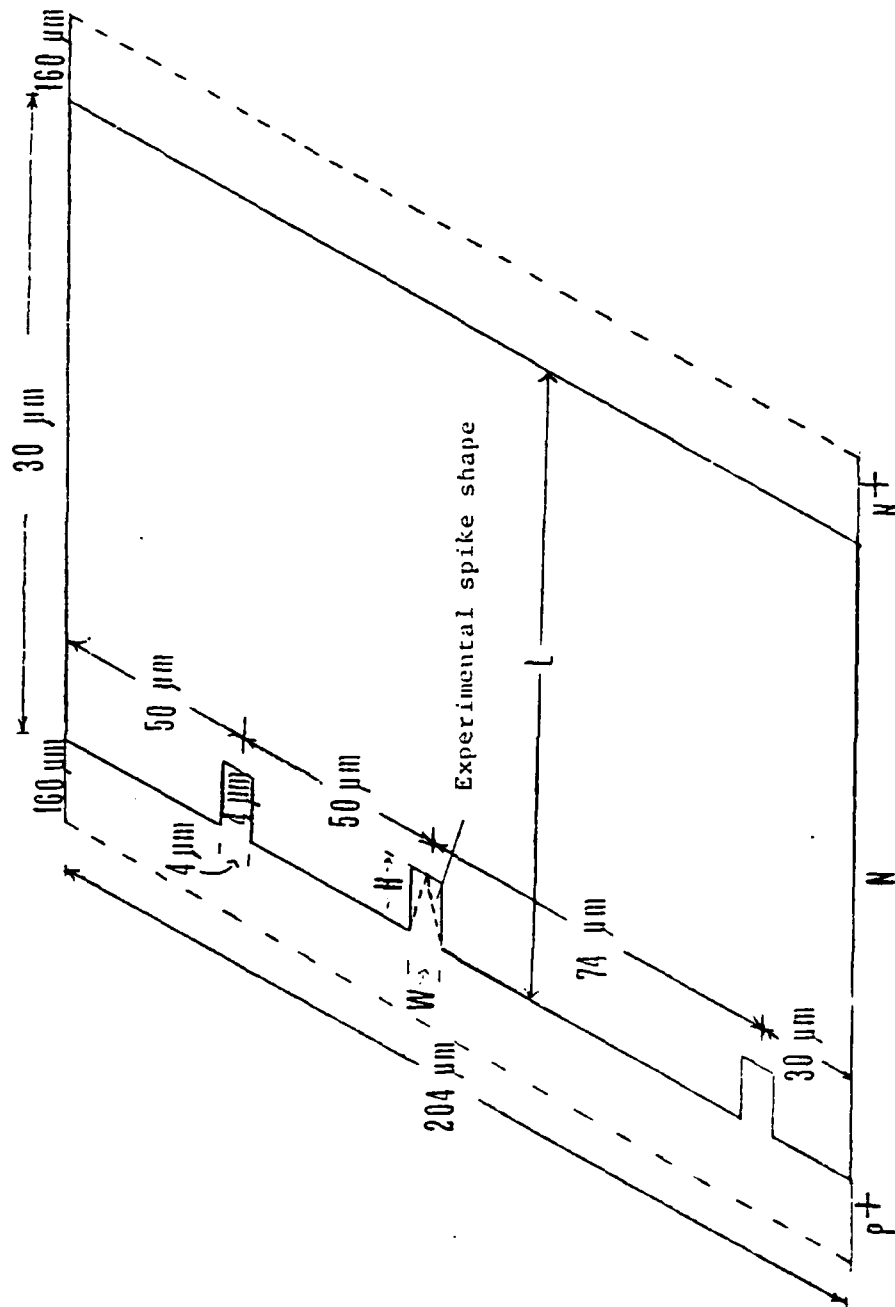


Fig. 133. Geometry of an SOS diode with three p^+n diffusion spikes.

sharp corner. The effect of the spike is to decrease the length of the n region in the strip with the spike relative to the length of the n region of surrounding strips. In another numerical investigation¹⁹, the effect of the presence of a small inhomogeneity on a thin silicon film without a junction was studied. The analysis showed that a filament occurs along the center line of a homogeneous rectangular strip. When an inhomogeneity in the form of a small intrusion is located off center, a filament forms, not at the center and not at the intrusion, but between the two. Olson⁵² theorized that if defects are regarded as localizations of altered dc conductance, then they could be expected to function as nucleating centers for thermal filaments. He also remarked that since a filament in an ideal chip forms at the center, perhaps a defect near the center of the chip would be more likely to cause premature filamentation than a defect near the edge.

Figures 134a-e (Runs 11-16) show current distributions over a diode containing diffusion spikes. In each figure, a particular curve represents the current configuration at a particular time for a constant excitation amplitude. All of the filaments formed at the three junction spikes. Additionally, it can be seen that right from the onset of the pulse, the spikes start acting as nucleation sites facilitating filament formation to a great extent. For 8 mA, the current density within the filament closest to the edge was lower (1.05×10^8 A/m²) than the other two (1.61×10^9 A/m² and 1.51×10^9 A/m²) at time 6.6 μ s. The same was also true for 9 mA current pulse. However, at 10 mA and above, all three filaments attained the same peak current density.

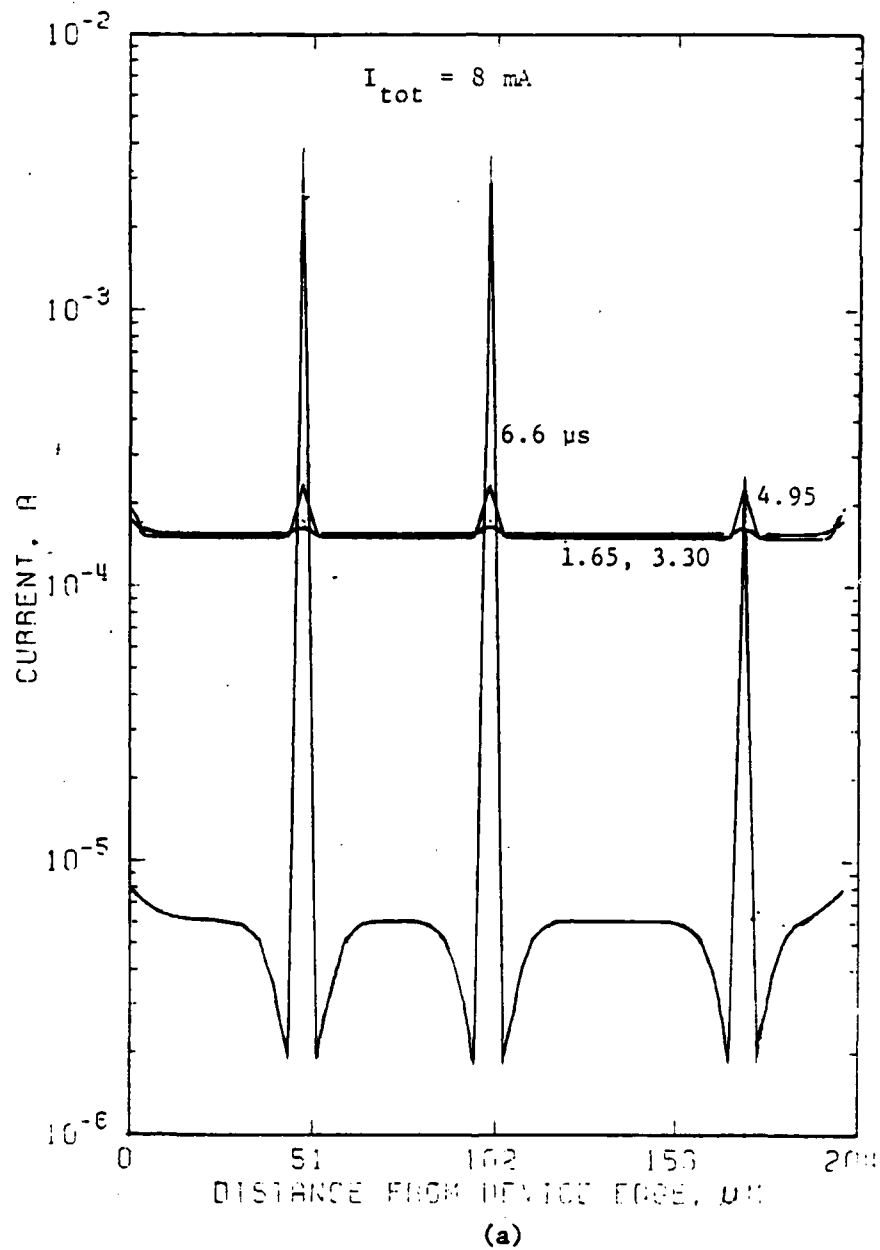


Fig. 134. Current distributions at different times in an SOS diode with three p-n diffusion spikes. Total currents are: (a) 8 mA, (b) 9 mA, (c) 10 mA, (d) 11 mA, (e) 12 mA.

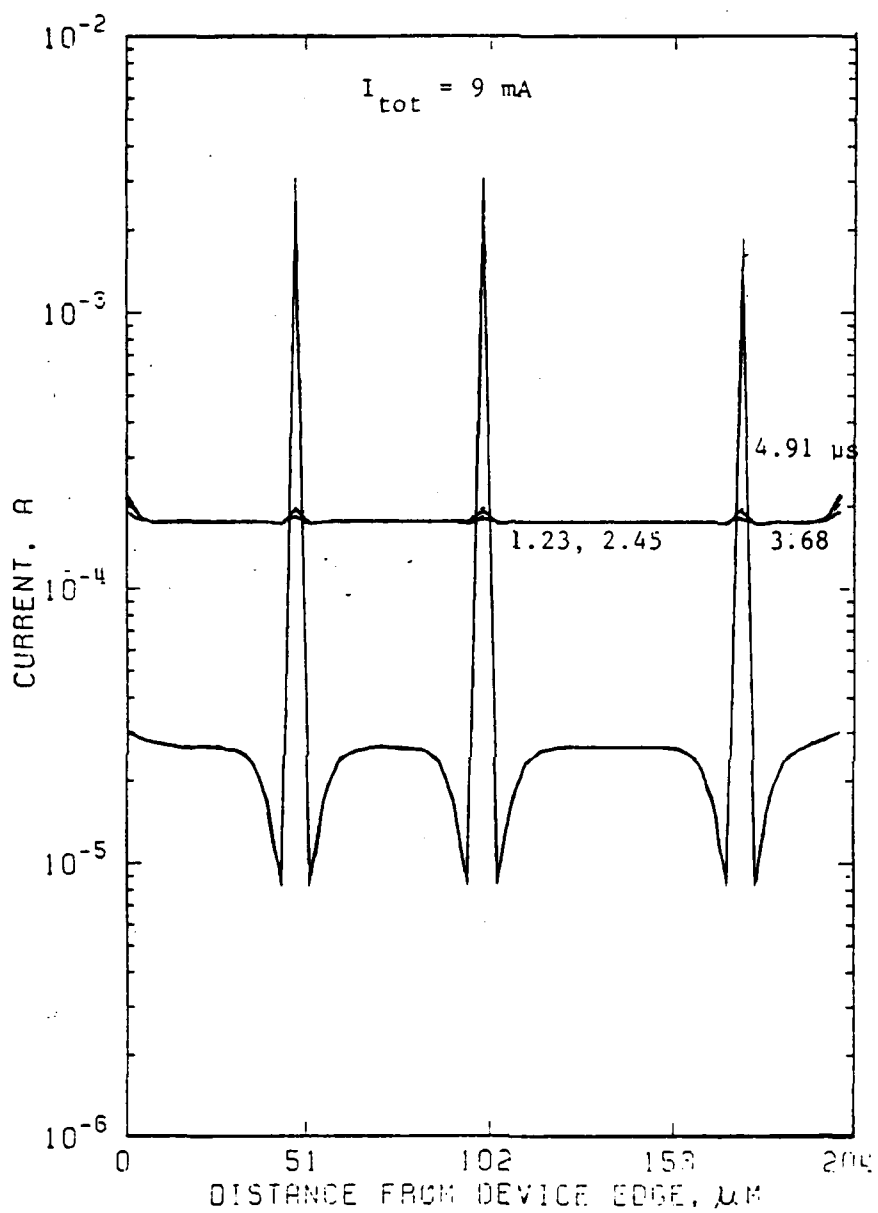


Fig. 134 (b)

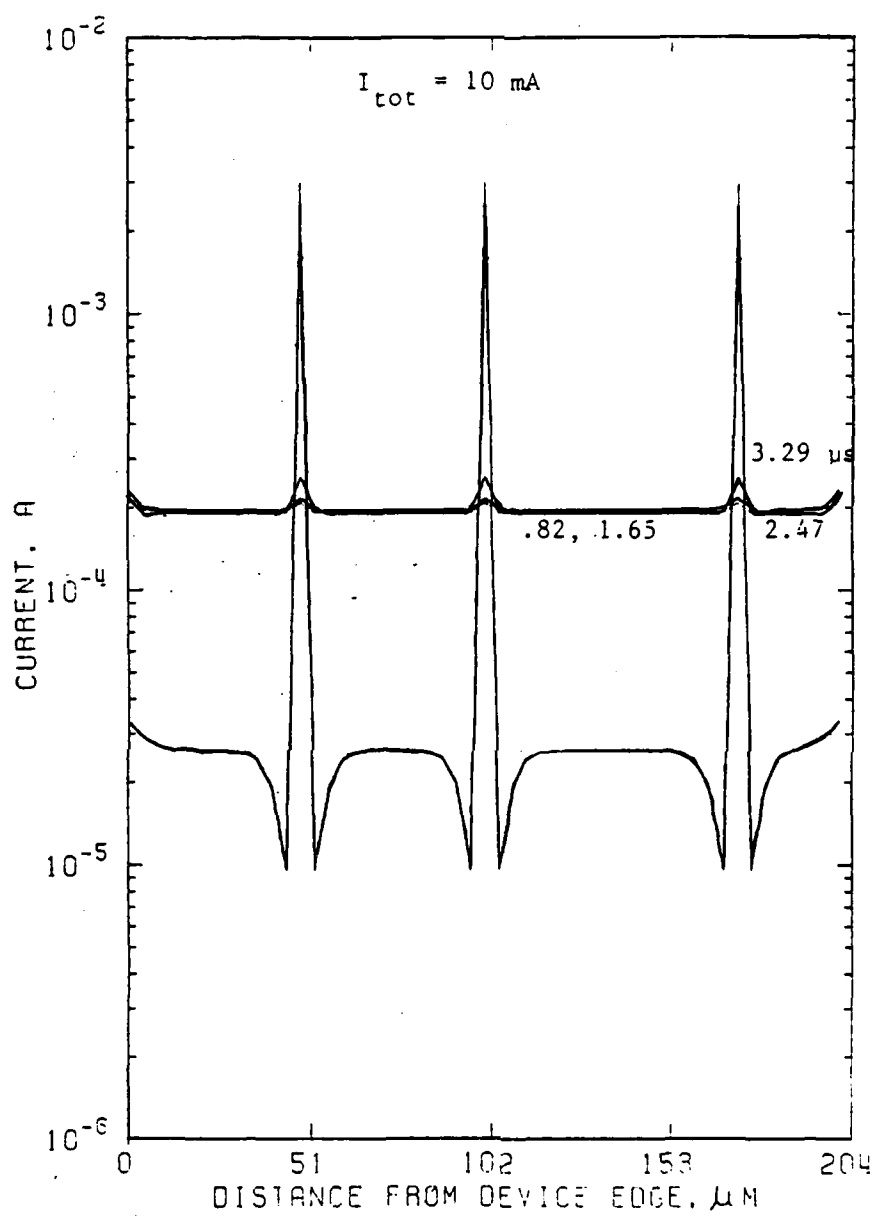


Fig. 134 (c)

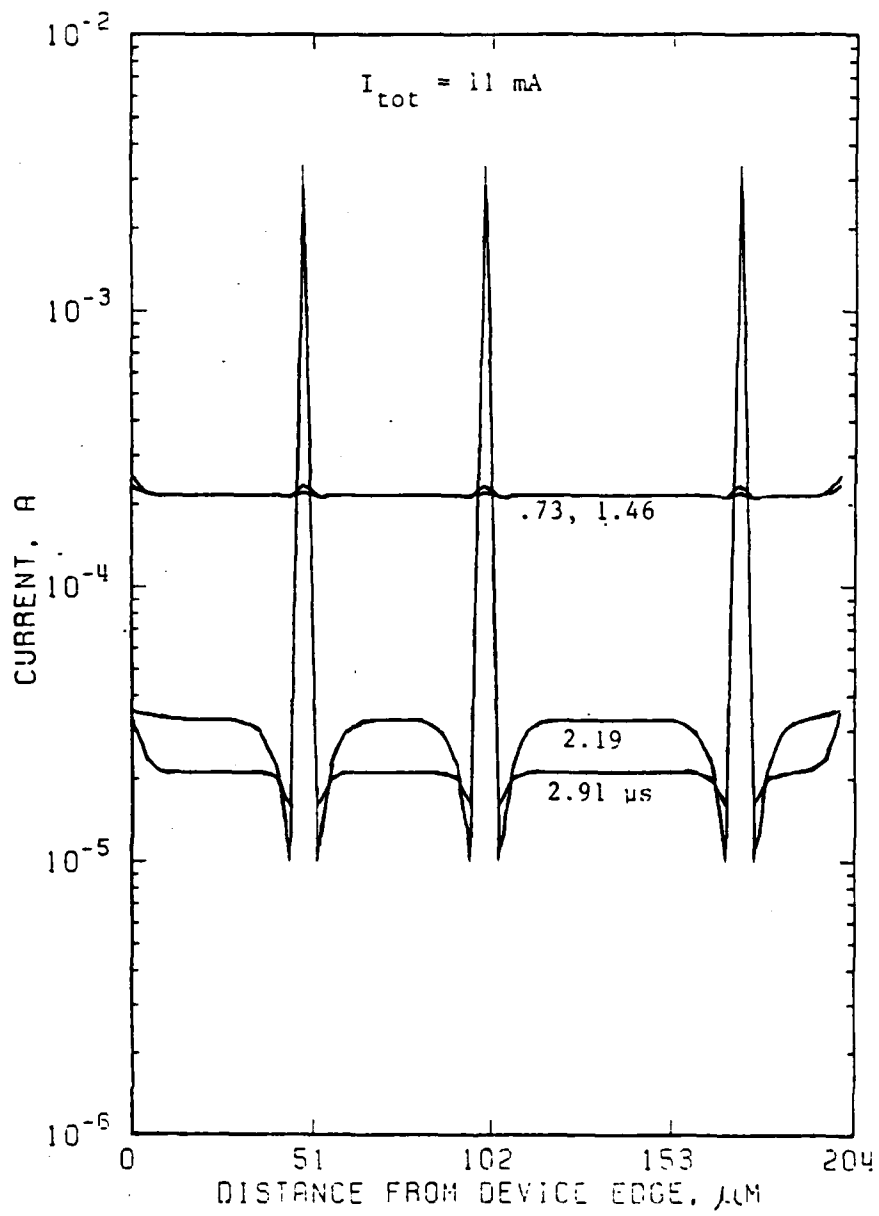


Fig. 134 (d)

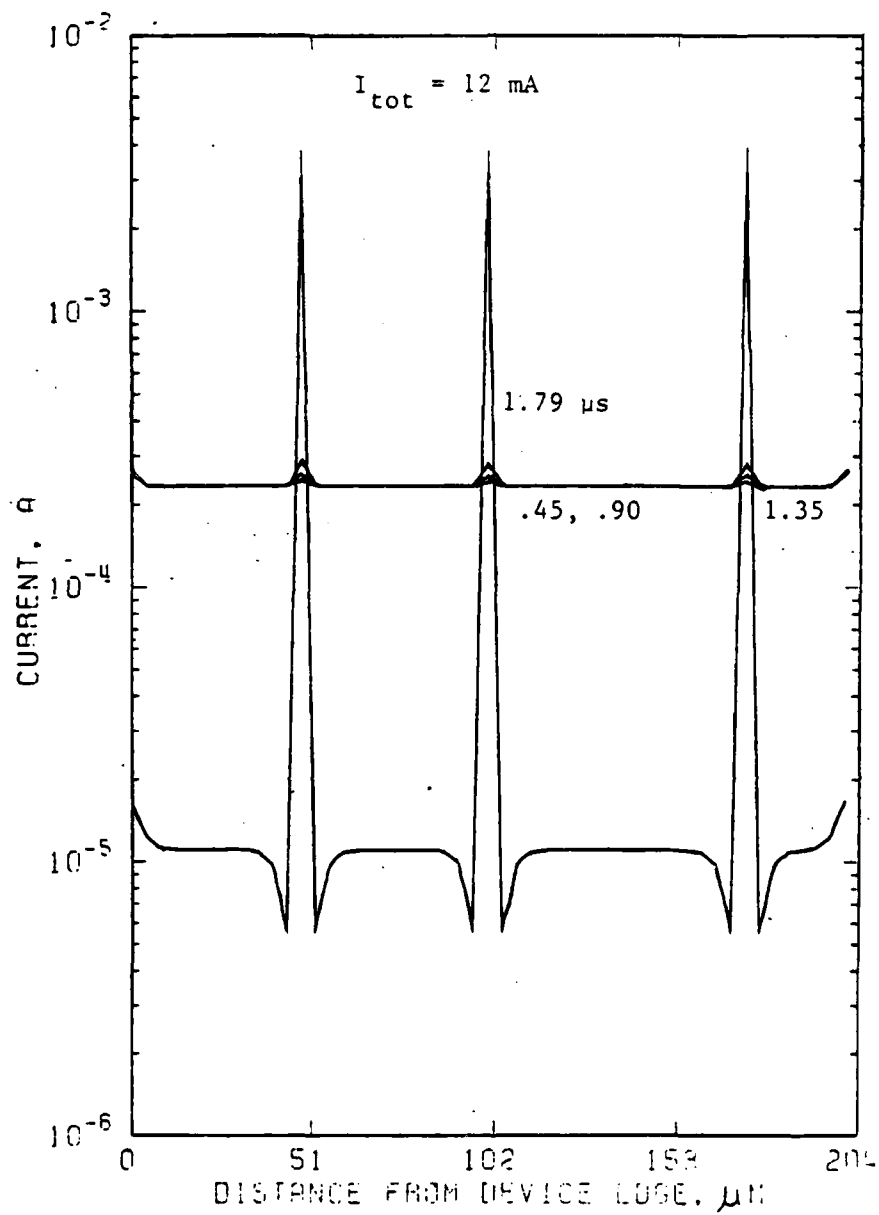
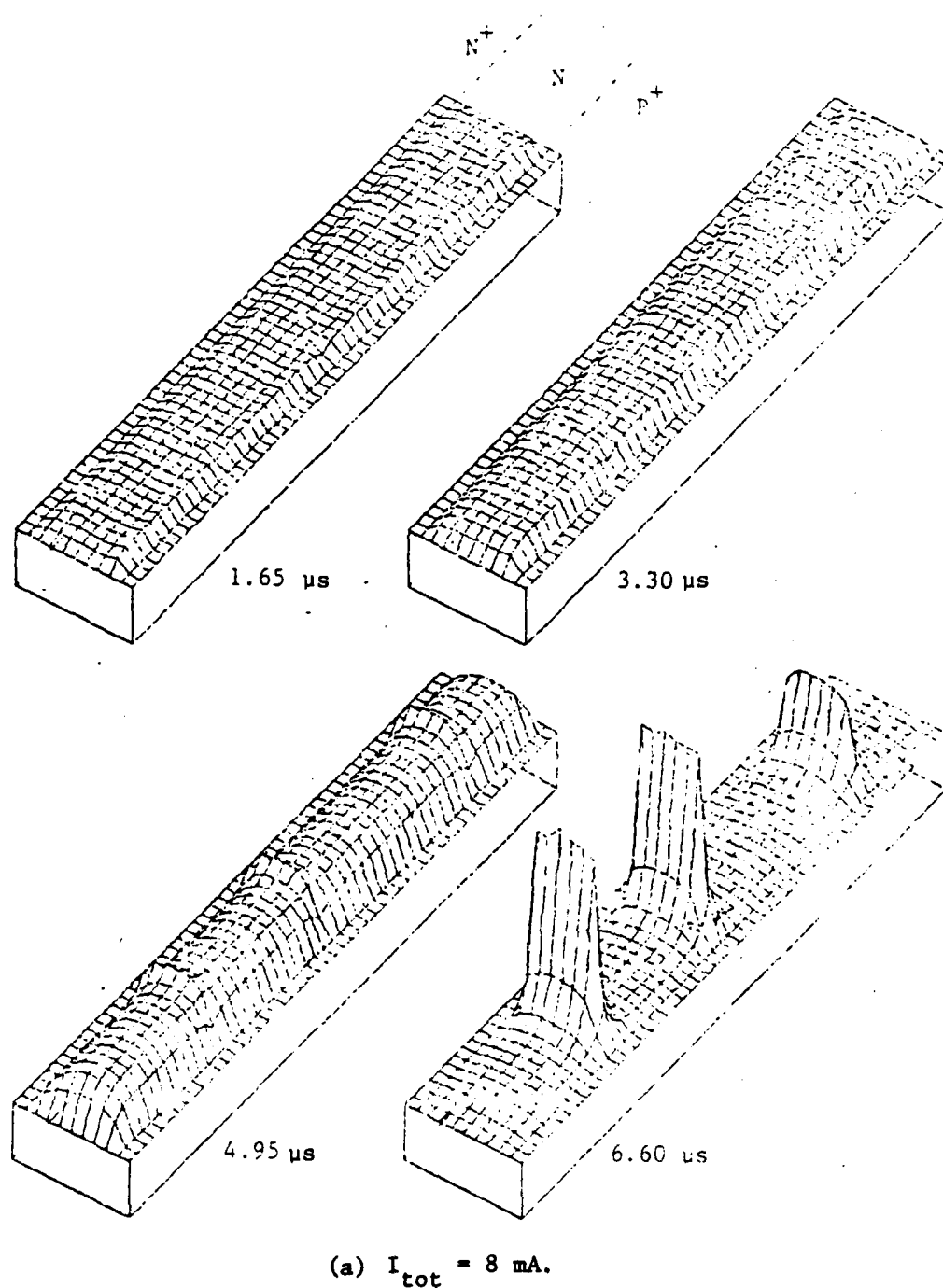


Fig. 134 (e)

Comparison can be made of the time required for filaments to form (see Table 19 for criterion for filament formation) at a particular current amplitude for diodes with and without spikes. For example, at an excitation amplitude of 10 mA, delay time τ_{fil} is 5.58 μ s for a diode with straight junction while for a spiked diode it is reduced to 2.49 μ s.

2. Temperature profiles

Figures 135a-e (Runs 11-16) show thermal profiles at various excitation pulse amplitudes and times for diodes with triple spikes. These profiles follow the corresponding current distributions in showing three thermal filaments nucleating at spike sites. From these figures it appears that the n region does not get nearly as hot prior to filament growth when spikes are present. Thus spike growths influence the threshold for filamentation. The temperature-time and current-time histories are shown in Figs. 136 and 137, respectively, for one filament of Run 15. As in the case of uniform junctions, the regions of concern are, the n region (1) and the junction (2) region of the strip in the center of the filament (52 μ m from edge), the n region (3) and the junction (4) of a strip adjacent to the filament site (56 μ m from edge) where the current is a minimum, and the n region (5) and junction (6) of a strip farther removed from the current filament (68 μ m from edge).



(a) $I_{\text{tot}} = 8 \text{ mA}$.

Fig. 135. Temporal development of temperature profiles of a p^+n spike diode for pulse amplitudes of (a) 8 mA, (b) 9 mA, (c) 10 mA, (d) 11 mA, (e) 12 mA.

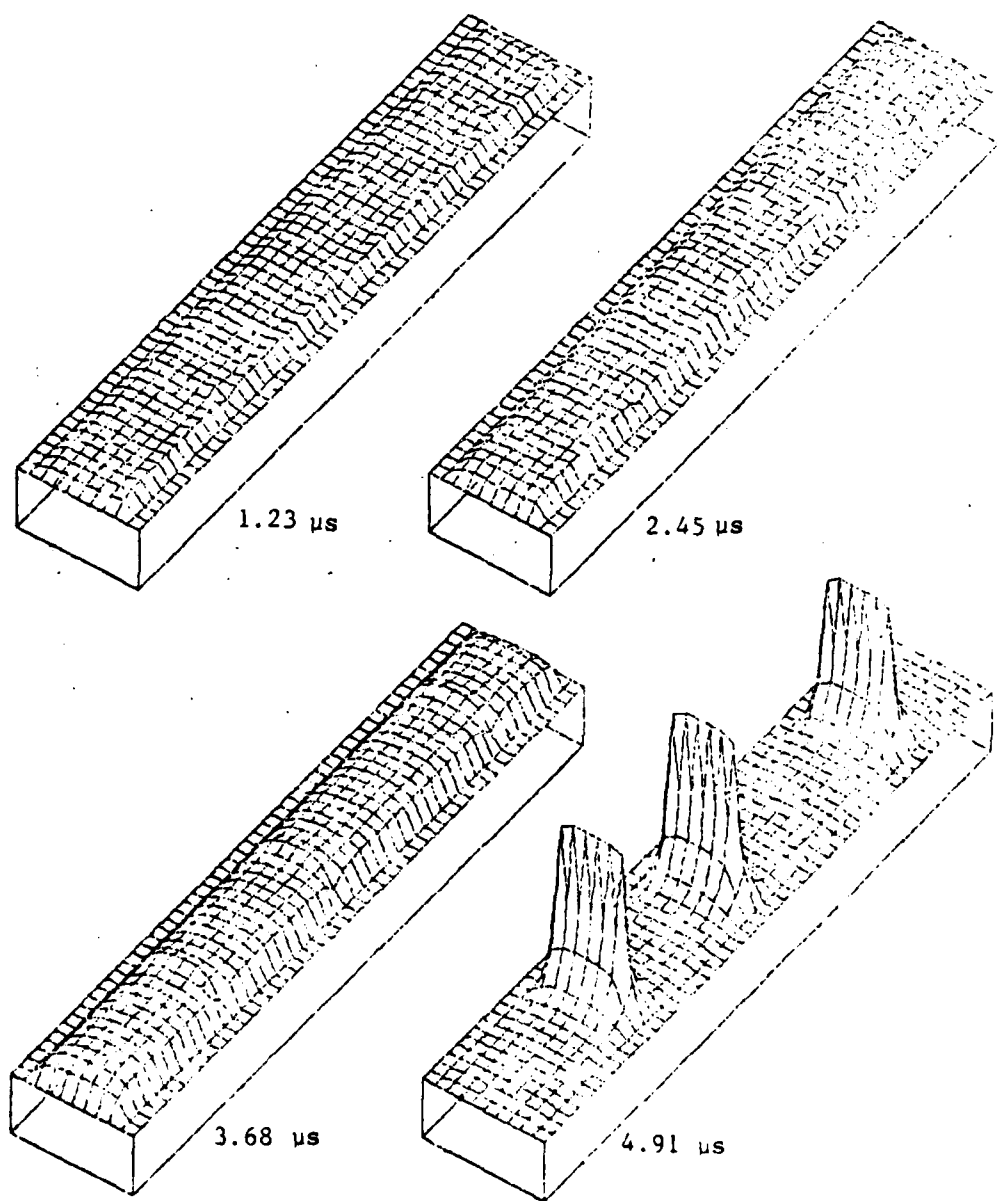


Fig. 135 (b) $I_{\text{tot}} = 9 \text{ mA}$.

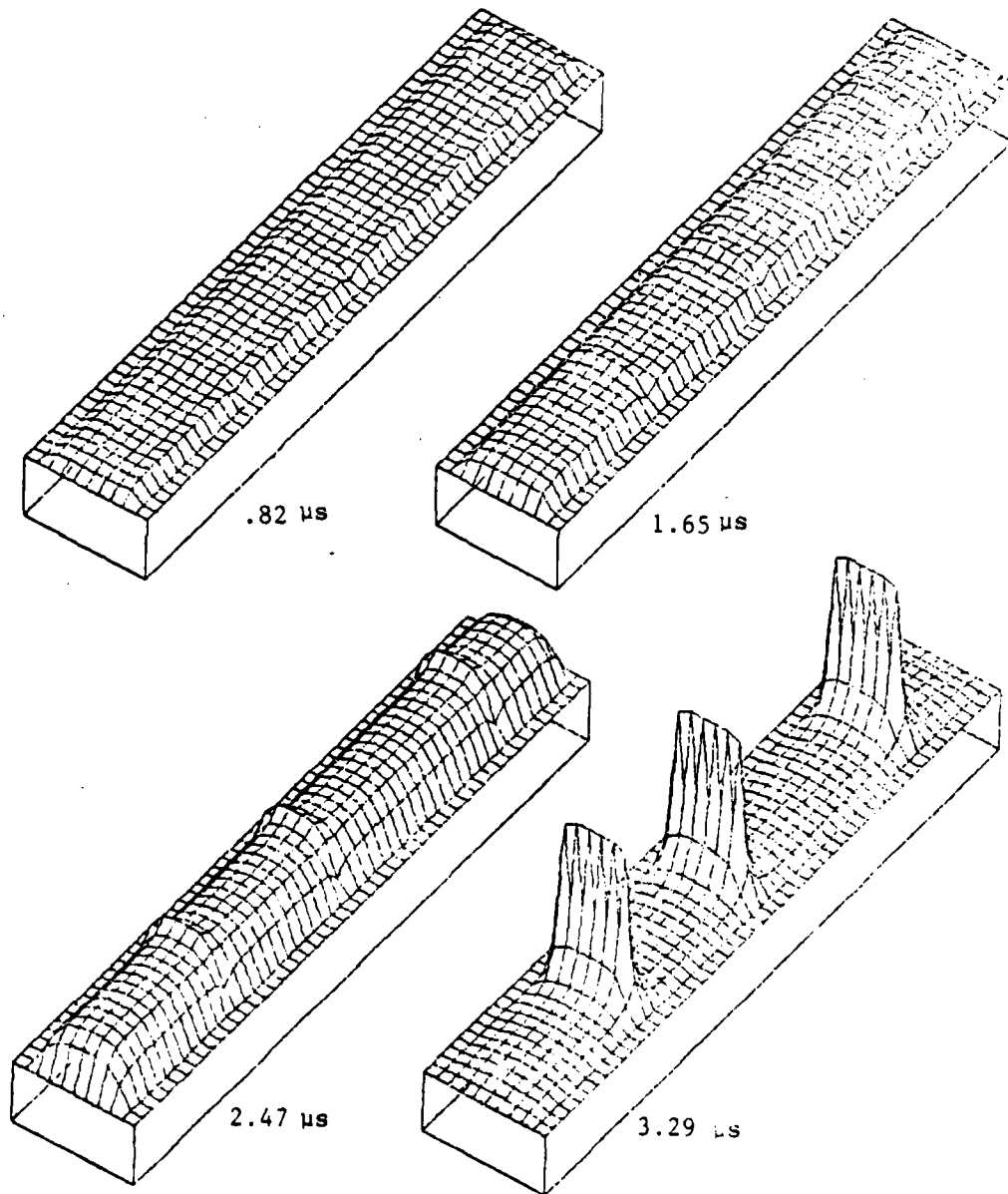


Fig. 135 (c) $I_{\text{tot}} = 10 \text{ mA}$.

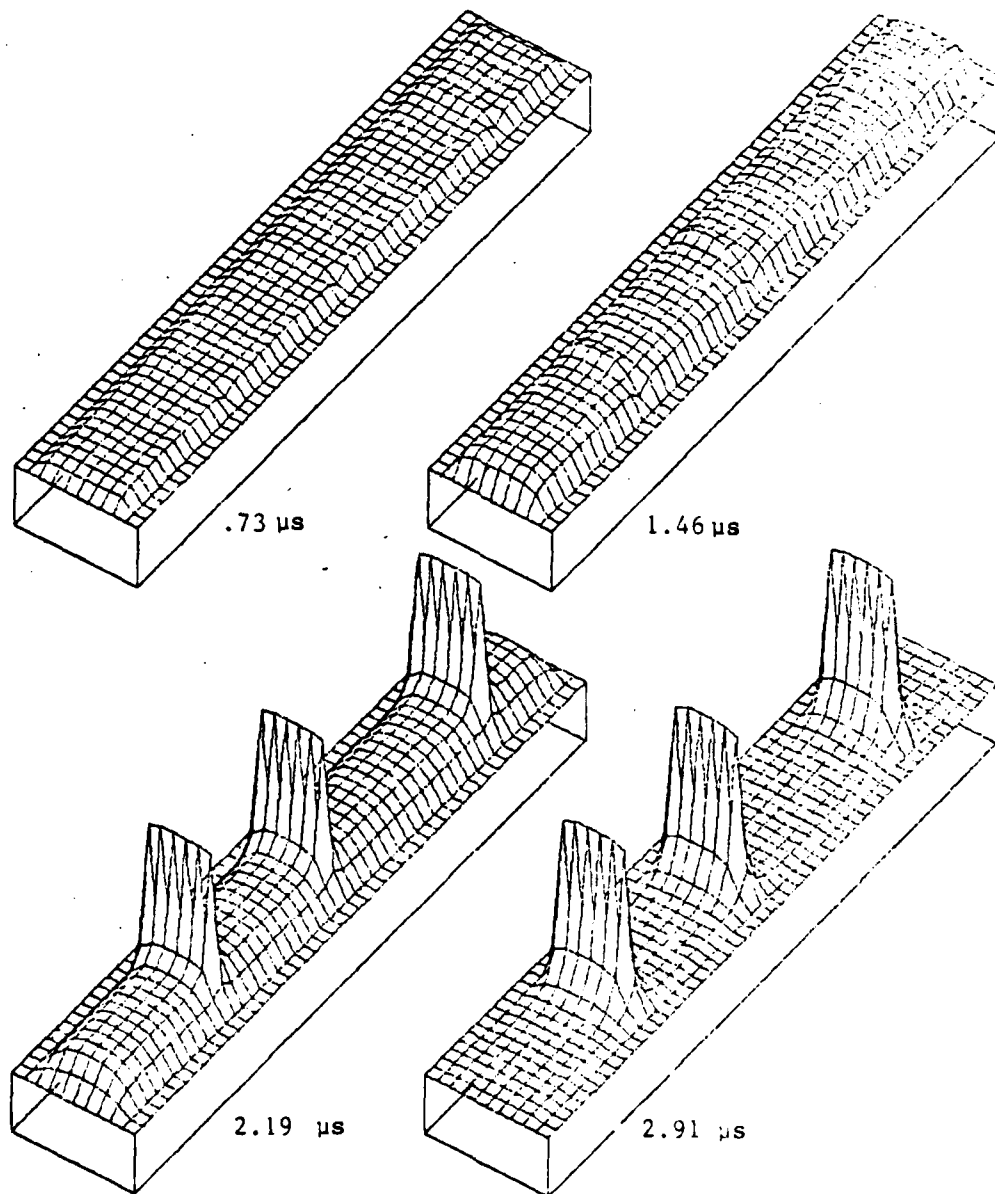


Fig. 135 (d) $I_{\text{tot}} = 11 \text{ mA}$.

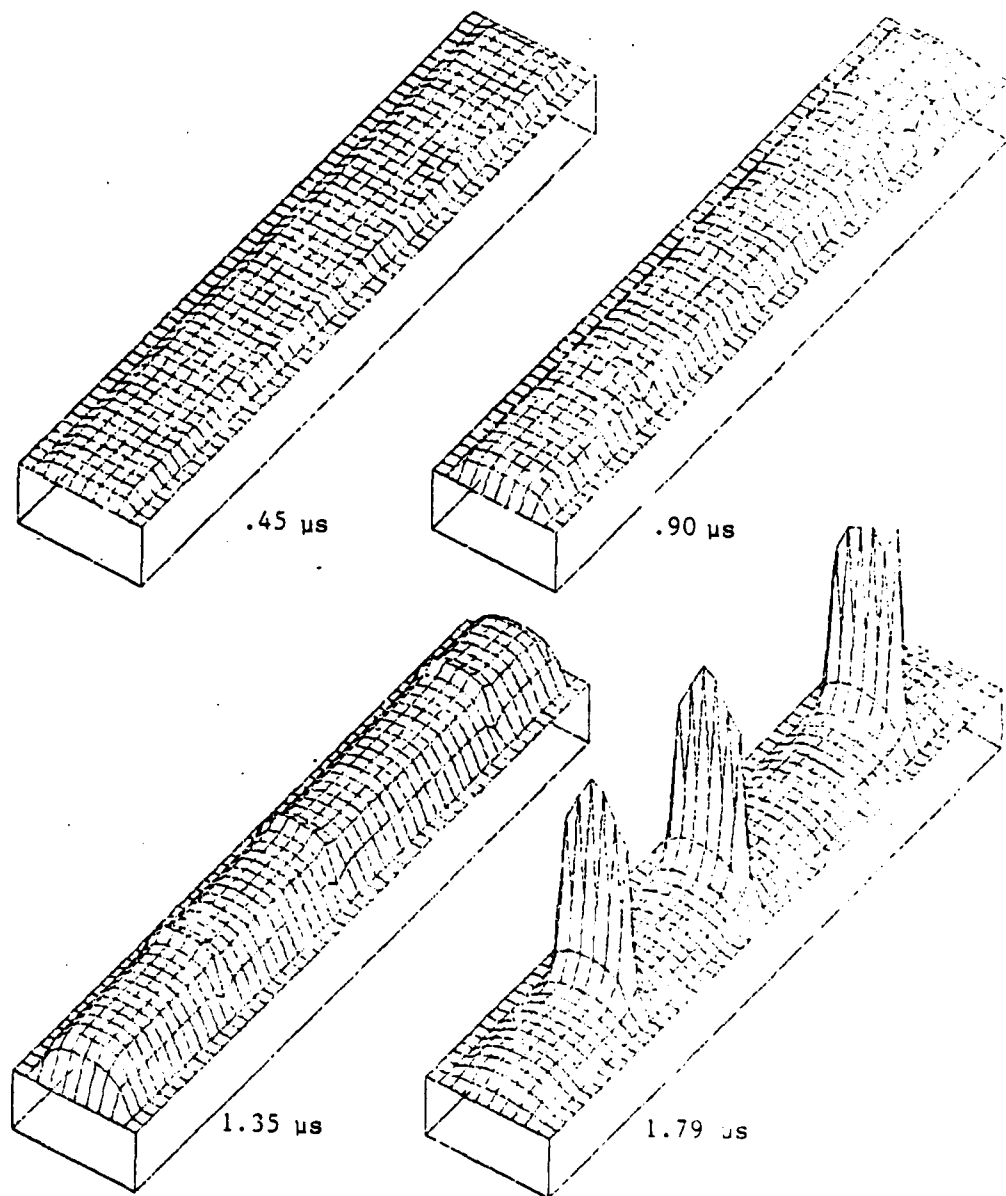


Fig. 135 (e) $I_{\text{tot}} = 12 \text{ mA}$.

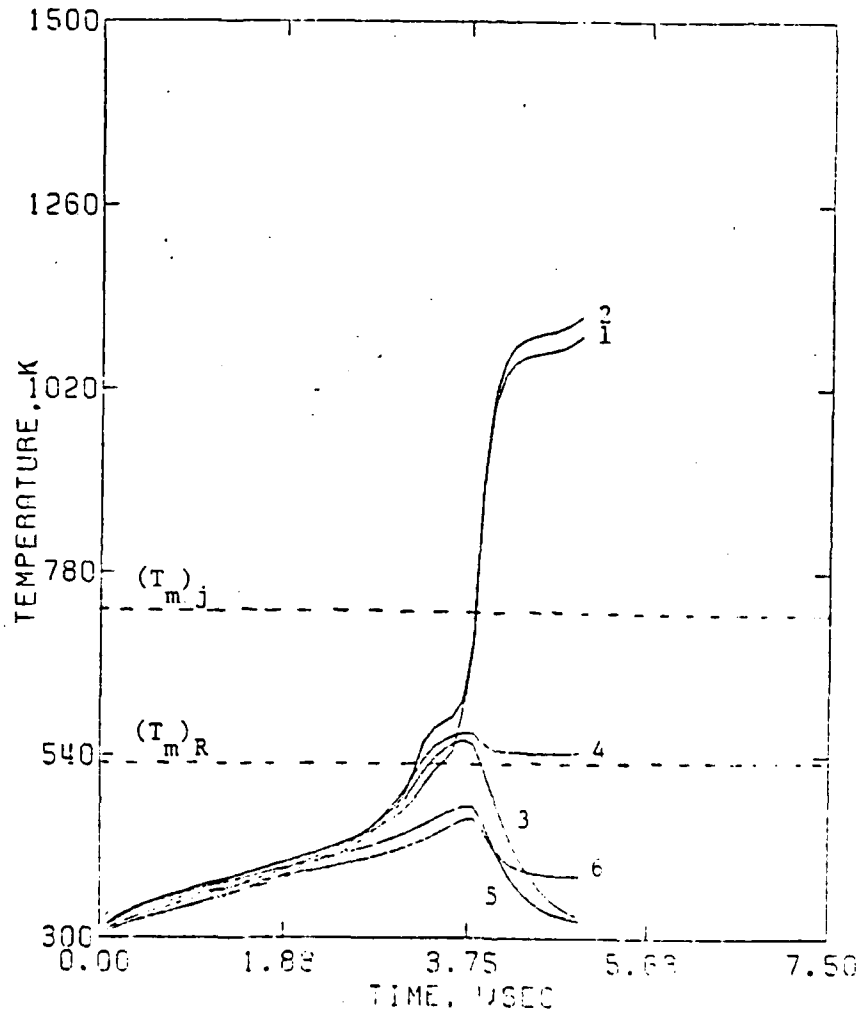


Fig. 136. Temporal development of temperature at various positions of an SOS diode with p-n triple spikes. Temperatures at a filament site in the junction (1) and n region (2), adjacent to the filament (where the current is a minimum) in the junction (3) and n region (4), and farther away from the filament in the junction (5) and in the n region (6). The pulse amplitude is 9 mA.

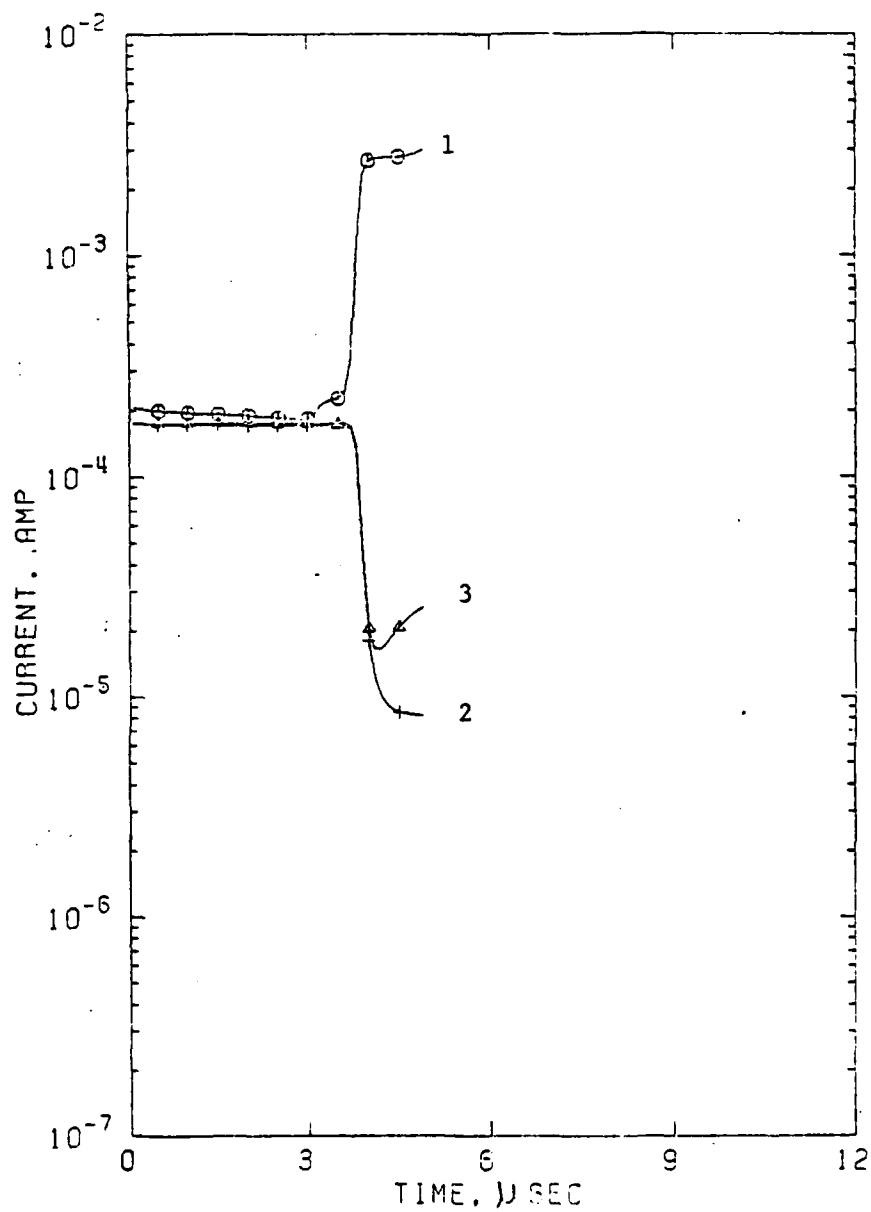


Fig. 137. Time development of current in a p^+n triple spiked diode (1) at a filament site, (2) adjacent to the filament (where current is a minimum), and (3) at a site farther away from the filament. The applied pulse amplitude is 9 mA.

3. Voltage waveforms

Voltage waveforms are shown in Figs. 138 and 139 for the runs of Figs. 134 (a-e). The shapes of these curves are similar as a group but differ in one respect from those of the diodes with straight junctions discussed earlier. Here, the voltage drop after attaining V_{peak} was almost vertical and showed no region similar to Region C of Fig. 123. Figure 140 shows voltage waveforms across the n region and across the junction at the positions used in Fig. 136. The localization provided by the geometric variation intensifies the growth rate of the filaments, so that instability is reached at an earlier time compared with smooth junction devices at the same current amplitude. Alternatively, if pulse duration is maintained the same, filament instability occurs at a lower pulse amplitude in the presence of spikes. This will be discussed further in connection with delay times for filamentation and for instability. In the case of junction spikes, no initial broad filament could be discerned. Current localization begins immediately, before thermal effects come into play. The major portion of the device never becomes as hot as it does in the absence of junction spikes. If the spikes are less than some critical size, they will no longer dominate the filamentation process. This critical size can be estimated by equating the decrease in strip resistance of the n region due to the decrease in n region length associated with the spike with the increase in resistivity accompanying the temperature rise in the strip. (The increased resistance due to temperature ballasts the strip).

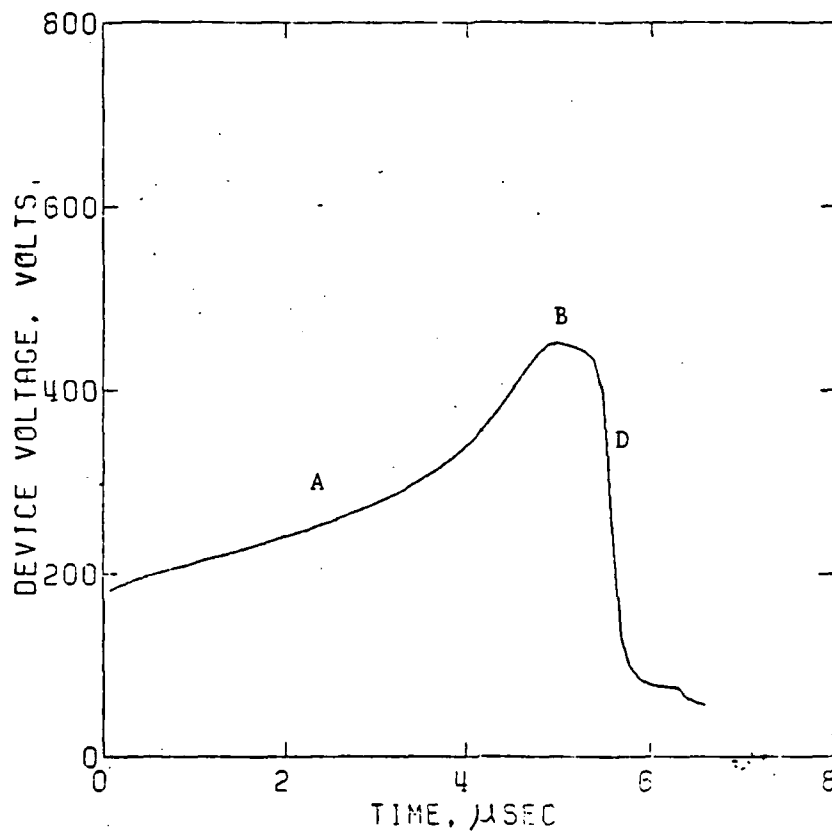


Fig. 138. Voltage waveform for a p⁺n spiked diode. The excitation pulse amplitude is 8 mA. An abrupt drop in voltage occurs after point B, thereby eliminating region C (see Fig. 123) where growth of a broad filament occurs in a uniform junction diode.

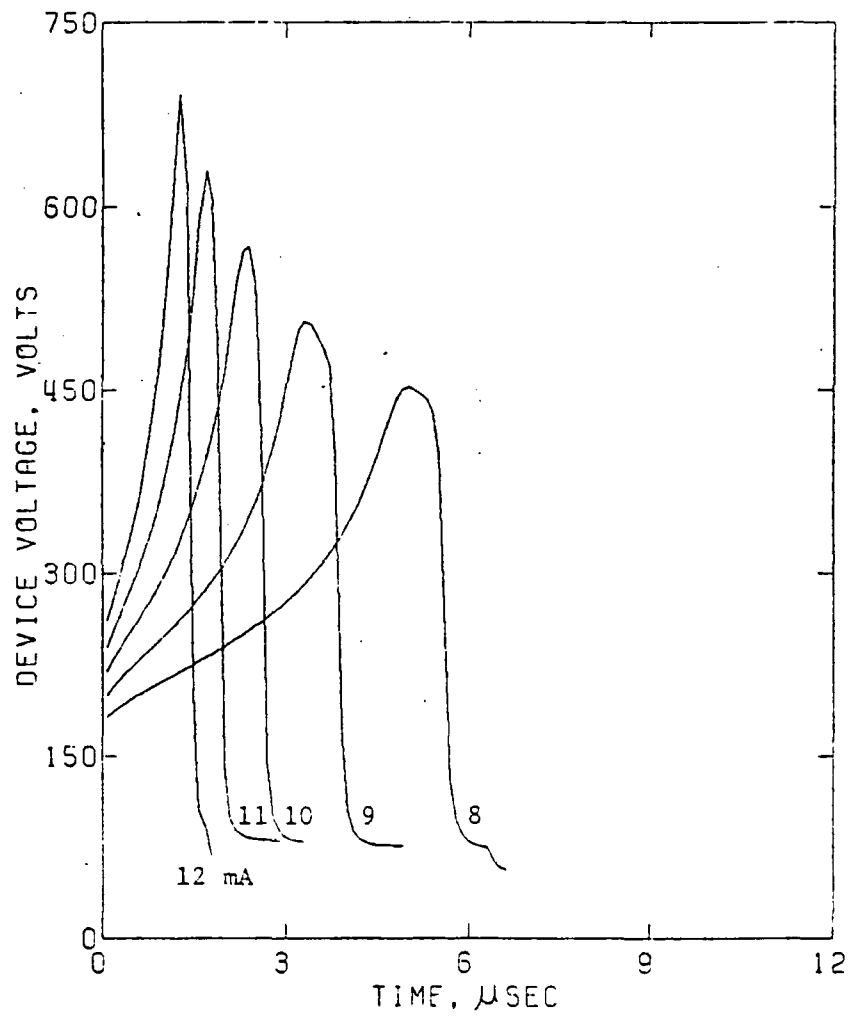


Fig. 139. Voltage waveforms for pulse amplitudes in the range 8 - 12 mA for a p n spiked diode.

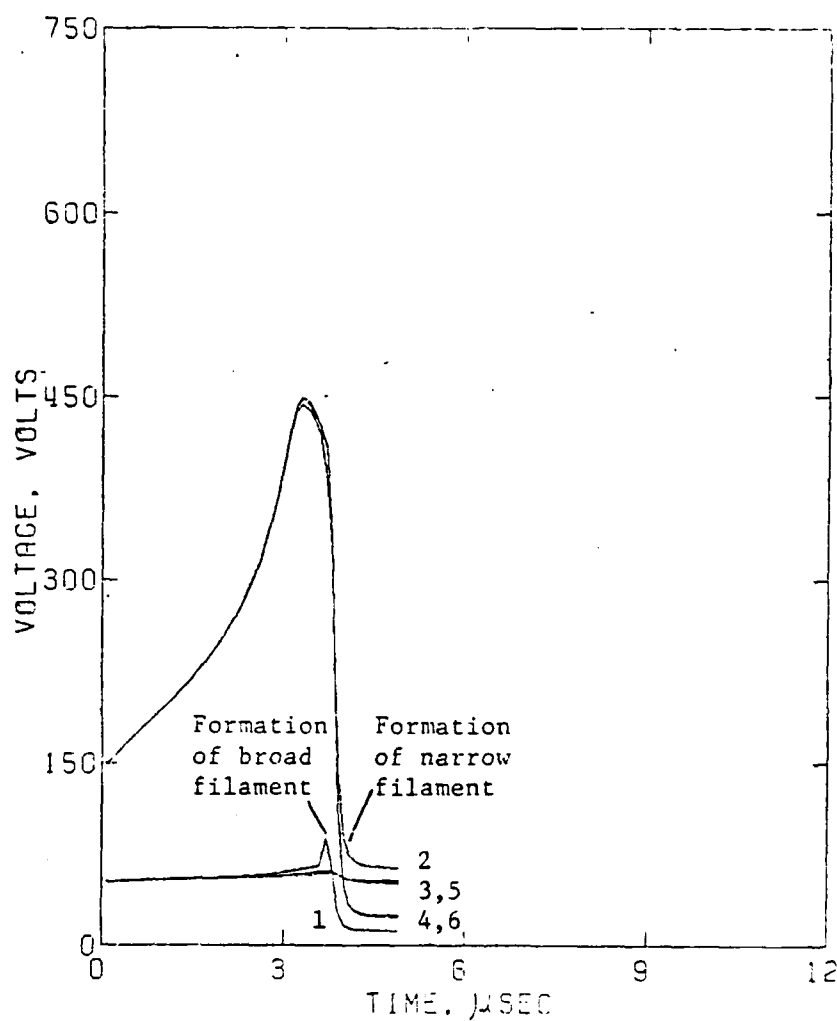


Fig. 140. Voltage waveforms for various portions of a p^+n spiked diode. The junction (1) and n region (2) waveforms at the filament site, junction (3) and n region (4) waveforms at a site adjacent to the filament, and junction (5) and n region (6) waveforms at a site farther away from the filament site are shown. The pulse amplitude is 9 mA.

If the n-region length is L , the spike height H , strip width W , and film thickness d (see Fig. 133), the resistance decrease to the spike is

$$(\Delta R)_{\text{slope}} = - \rho \frac{H}{Wd}$$

The resistance increase due to the temperature change from T to $T + \Delta T$ in the length $(L-H)$ that ballasts the spike is

$$(\Delta R)_{\text{ballast}} = \left(\frac{d\rho}{dT}\right)_T \Delta T \frac{(L-H)}{Wd}$$

At the critical condition $(\Delta R)_{\text{slope}} + (\Delta R)_{\text{ballast}} = 0$

$$- \rho \frac{H}{Wd} + \left(\frac{d\rho}{dT}\right)_T \frac{\Delta T (L-H)}{Wd} = 0$$

and

$$H = \frac{\left(\frac{d\rho}{dT}\right)_T L \Delta T}{\rho + \left(\frac{d\rho}{dT}\right)_T \Delta T}$$

The derivative $(d\rho/dT)_T$ is greater at the initial ambient temperature than at higher temperatures. The size of ΔT for a particular time step depends on the current amplitude, n region doping density, and the length of the time step. In the present calculations, for conditions during the early part of the pulse, a time step of $0.01 \mu s$ and an n region doping density of 10^{22} atoms/ m^3 , a plausible expression for ΔT is

$$\Delta T = k I_{\text{tot}}$$

where k is equal to 91.25 K/A for 8 mA , and 121.66 K/A for 12 mA for n region doping of 10^{22} atoms/ m^3 and step size of $.01 \mu s$. The expression

for the critical value of spike height becomes

$$H = \frac{\left(\frac{d\rho}{dT}\right)_T^k I_{\text{tot}} L}{\rho + \left(\frac{d\rho}{dT}\right)_T^k I_{\text{tot}}}$$

If the change in ρ due to the temperature rise is small compared to ρ itself during the time step, then

$$H \approx \frac{1}{\rho} \left(\frac{d\rho}{dT}\right)_T^k L I_{\text{tot}}$$

The size of the critical spike is thus proportional to the fractional change in resistivity with temperature at ambient temperature, the length of the n region, and the current amplitude. For the present diodes

$$\frac{1}{\rho} \left(\frac{d\rho}{dT}\right)_{300} = 9.7 \times 10^{-3} \text{ K}^{-1}; L = 30 \text{ } \mu\text{m}$$

Thus, at a current of 8 mA, the critical spike height is estimated to be 0.20 μm , while at 12 mA, it is 0.32 μm . To this end, runs 19 and 20 were made with these critical spike heights at .20 and .32 μm , respectively, and in each case, three distinct narrow filaments at the spike sites were observed. Additional runs should be taken for spike heights less than the critical size to test the validity of the above analysis.

4. Delay times

Delay times for the onset of filamentation and the onset of instability (see Table 19 for definitions) are plotted as functions of excitation pulse amplitudes in Fig. 141. Figure 141 shows that the time interval between onset of filamentation and instability is about 1 μs , and independent of amplitude. Thus the onset of filamentation is a

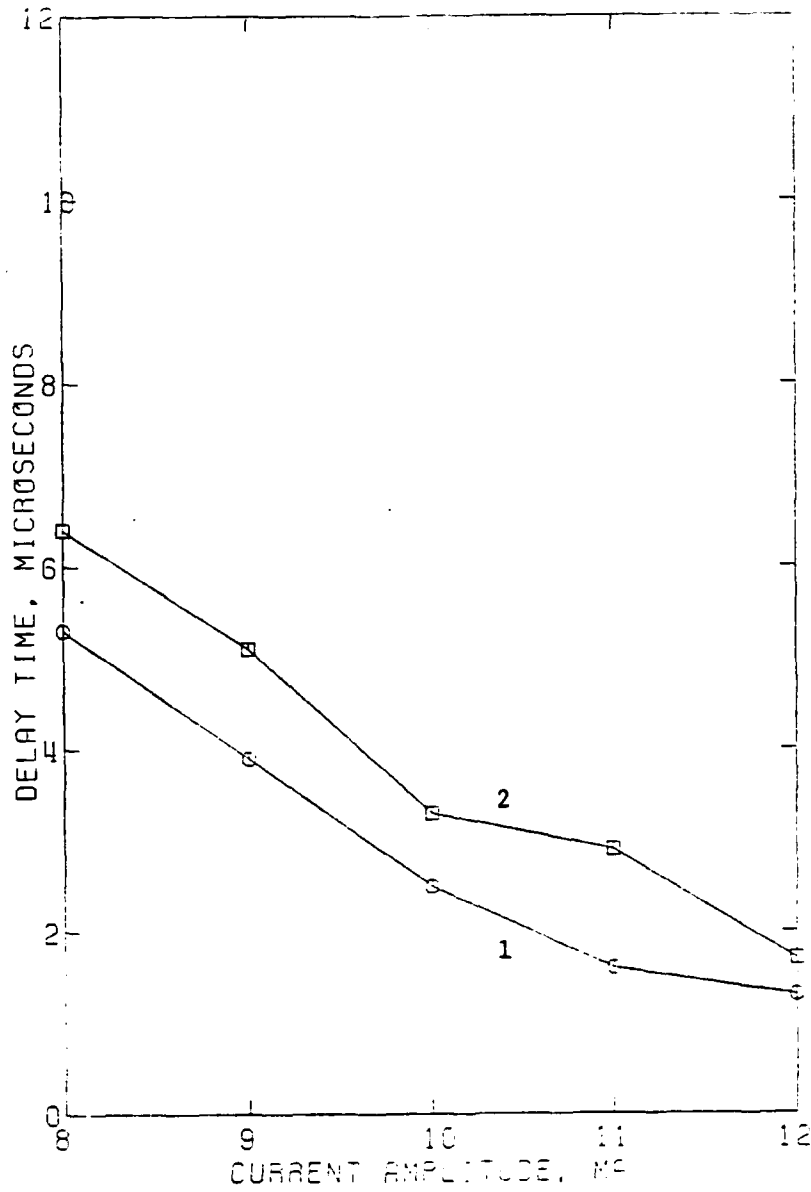


Fig. 141. Delay time for the onset of filamentation (1) and for instability (2) at various excitation amplitudes for a p^+n spiked diode.

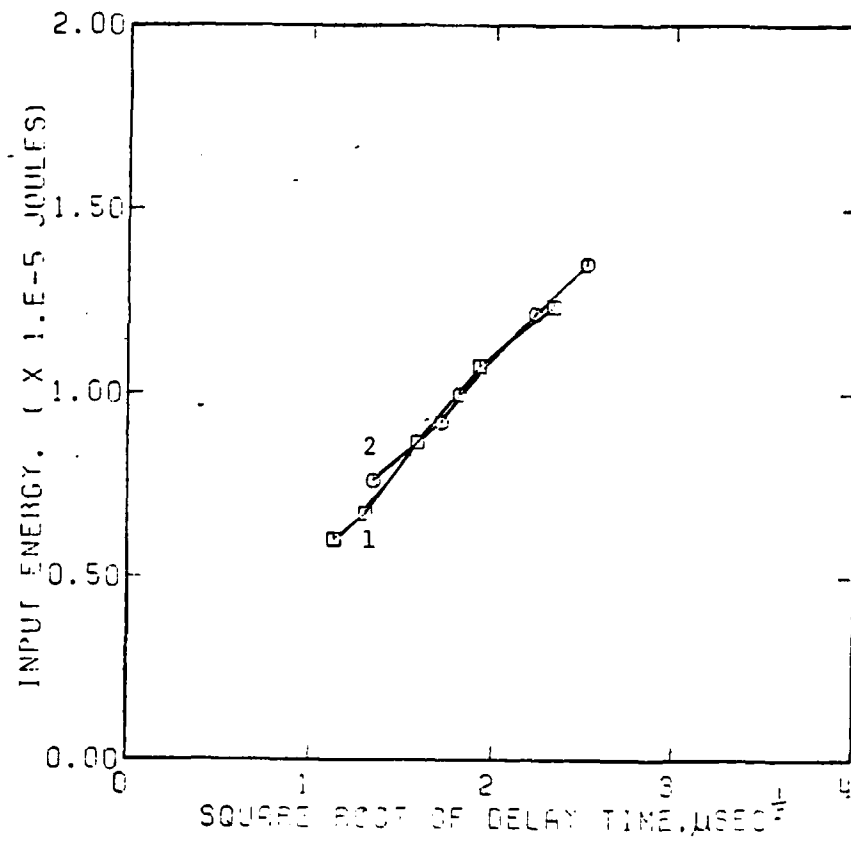


Fig. 142. Input energy for the onset of filamentation (1) and for the onset of instability (2) as a function of the square roots of the delay times, τ_{fil} and τ_{ins} , respectively.

good indicator that the threshold of damage is about 1 μ s away in the pulse. The input energies for filamentation and for instability are shown in Fig. 142 as functions of the square root of delay time. Comparisons of both delay times and input energies for the cases of straight and inhomogeneous junctions show, for junctions with spikes, that delay times are shorter and the input energy requirements are smaller. For example, at an excitation pulse of 10 mA, the delay time and input energy for filamentation are 5.58 μ s and 2.120×10^{-5} Joules, respectively, for a uniform diode. The same quantities for a triple spiked diode are 2.492 μ s and 0.866×10^{-5} Joules, respectively. Thus it can be concluded that presence of inhomogeneities facilitates filamentation to a large extent by lowering the minimum energy requirement and by decreasing the time delay for onset of filamentation for a given current amplitude (or, equivalently, lowering the current amplitude for the same delay time).

5. Role of film thickness

All of the data discussed so far have been based on diodes 0.6 μ m thick. Computations were also performed for diodes having a thickness of 1.2 μ m at a current level of 11 mA, one for a diode with no defects and the other for a diode with three junction spikes as above. No filaments formed during the 9.59 μ s pulse in the uniform junction diode. Filaments occurred at the spikes locations in the spiked structure, as indicated in Figs. 143 and 144.

The voltage waveform for 1.2 μ m thickness and junction spikes is shown in Fig. 145. The shape is similar to that of the 0.6 μ m diode, but region C is less prominent and the small ripples are almost absent.

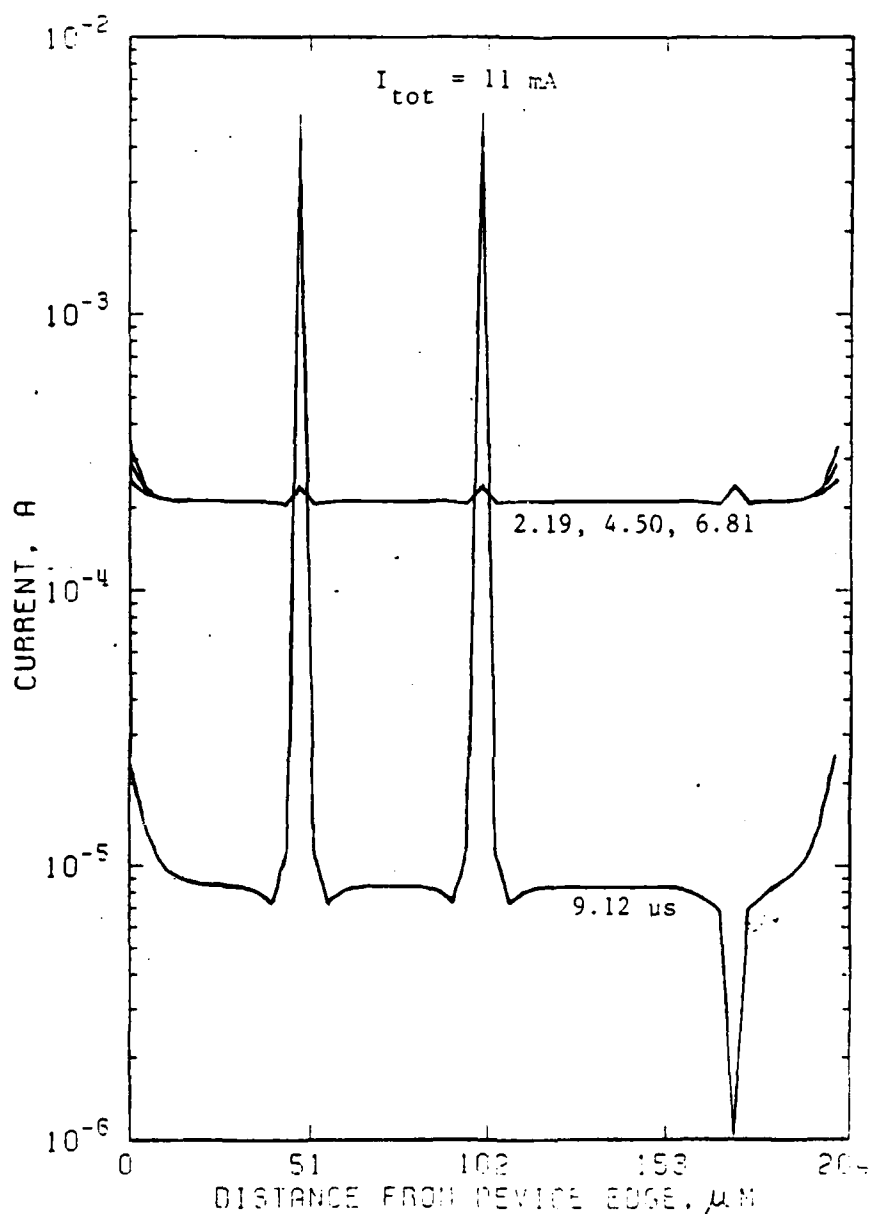


Fig. 143. Current distributions at different times in a p^+n spiked diode when the silicon film thickness is $1.2 \mu\text{m}$. The current in the third spike is lower than that of its surrounding region because of its higher n region temperature (see Fig. 144). Total current is 11 mA, and average current density is $4.49 \times 10^7 \text{ A/m}^2$.

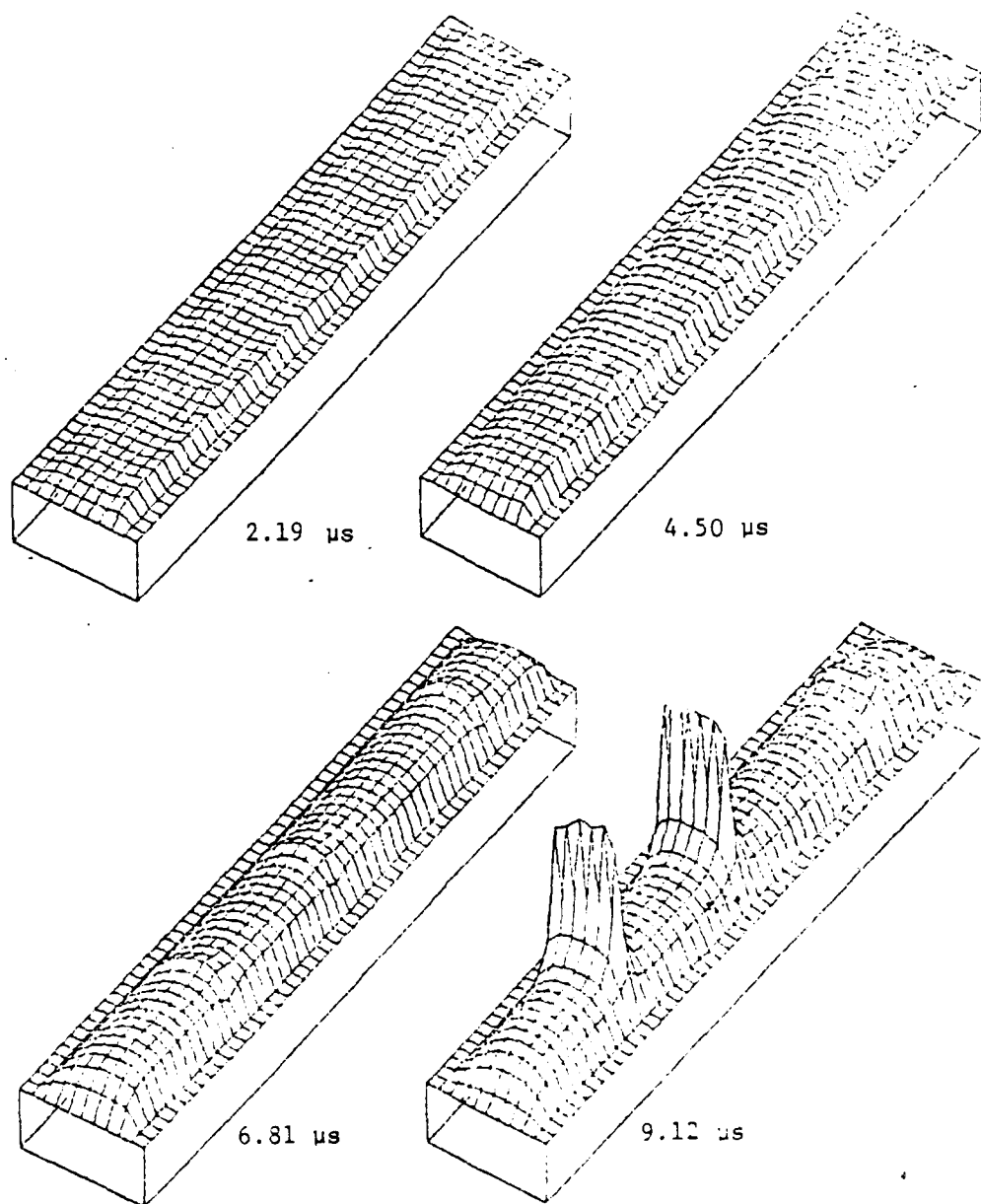


Fig. 144. Temperature profiles of a p^+n spiked diode as they develop in time. Pulse length is 9.12 μs , amplitude is 11 mA, and silicon film thickness is 1.2 μm .

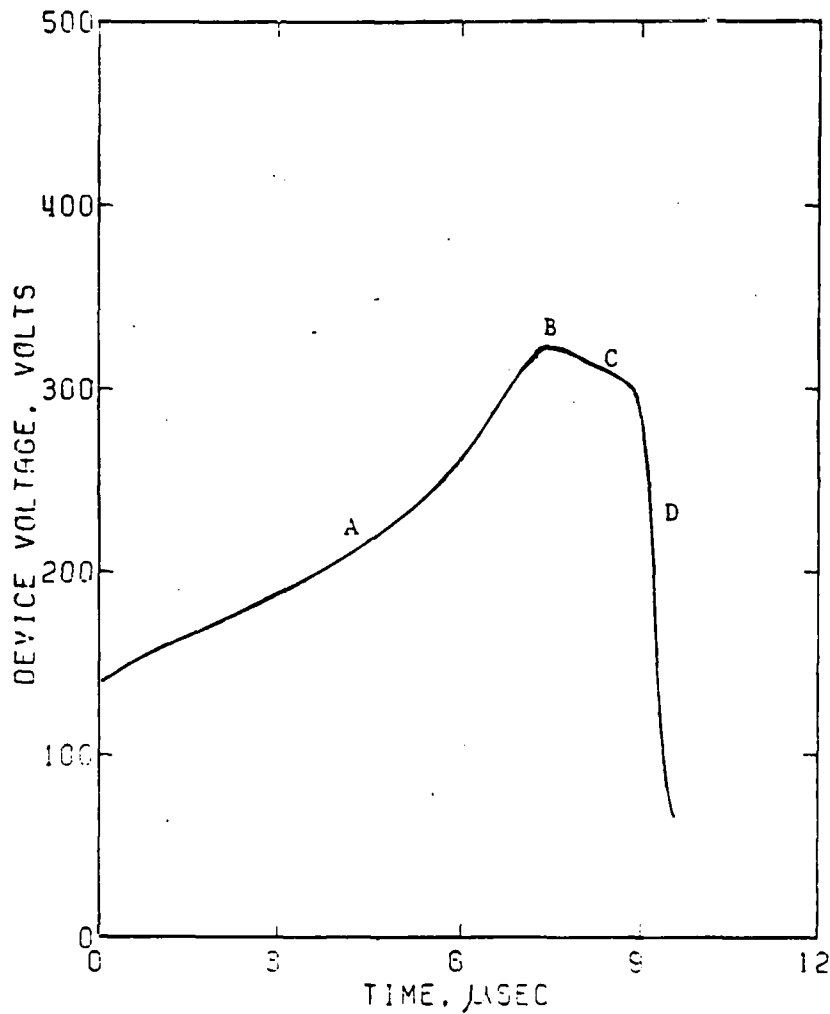


Fig. 145. Voltage waveform for a p^+n spiked diode with silicon film thickness of $1.2 \mu\text{m}$. Here region C is clearly discernible, but the waveform is more like those of Fig. 139 (p^+n spike, $0.6 \mu\text{m}$ thickness) than that of Fig. 123 (uniform junction, $0.6 \mu\text{m}$ thickness). The pulse amplitude is 11 mA.

Current distributions are compared in Fig. 146 for spiked diodes 0.6 μm and 1.2 μm thick at $t = 1.88 \mu\text{s}$, each diode being excited by a pulse of the same current density of $.086 \times 10^9 \text{ A/m}^2$. Only the run for the 1.2 μm diode was able to produce filaments in 1.88 μs .

C. Diode with spikes on the n^+n junction

1. Program modifications

Calculations on diodes with spikes on the n^+n junction were performed by modifying the p^+n spike programs developed by Baruah. While the modifications were being made, a revised set of JVT characteristics was being produced. Although these were not completed in time to be included, they suggested that the junction width used by Baruah, 4 μm , may have been too wide. As indicated in the discussion of JVT characteristics, at high current densities solutions are obtainable only at temperatures above 600 K (high density of thermally generated carriers) or a high velocity for carriers is hypothesized. Although the junction width is a known function of temperature and current density, utilization of a variable junction width would complicate computation of the heat transfer to the junction element and each surrounding element. However, Liou took the junction width to be 3 μm . He also developed an analytical interpolation scheme to replace the interpolation program used by Baruah to obtain junction voltage. This change removed some spurious oscillations that had been occurring in the solutions of the model.

To allow comparison of the n^+n spike calculations with uniform junction and p^+n spike calculations, Liou used his interpolation scheme and 3 μm junction width to calculate the uniform junction and p^+n spike junction for the 7 mA excitation current. These results will be presented before going to the n^+n spike junction diodes.

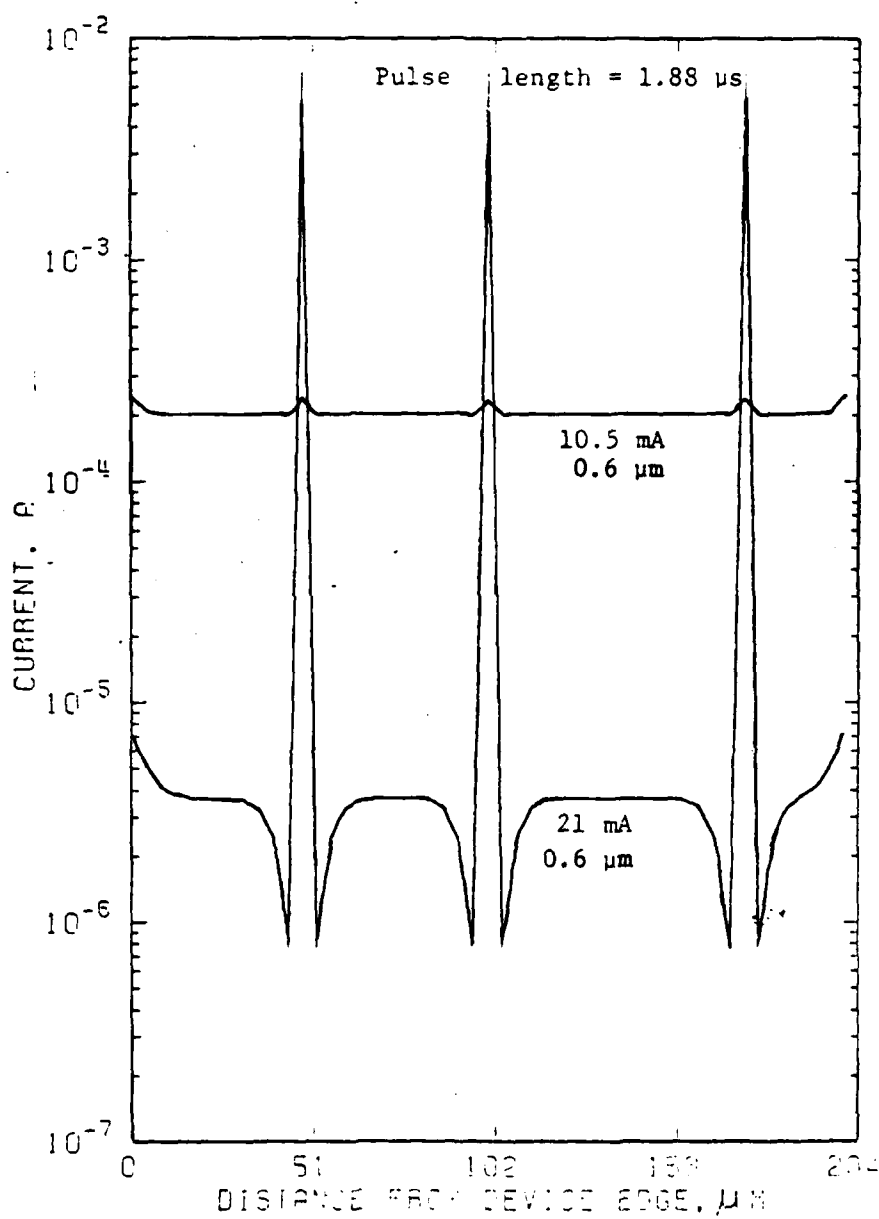


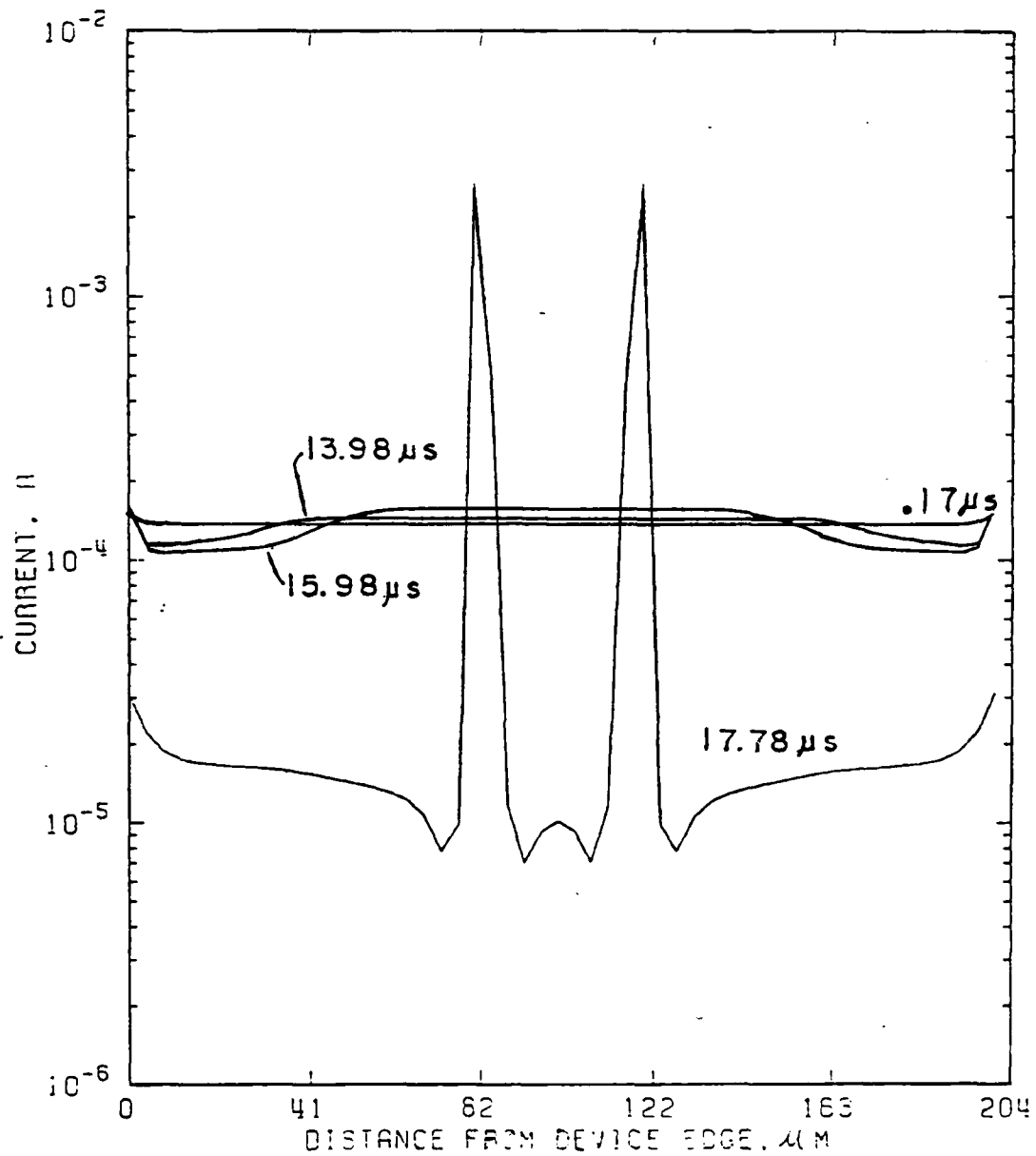
Fig. 146. Current distributions for p⁺n spiked diodes of 0.6 μ m and 1.2 μ m silicon thickness at pulse amplitudes of 10.5 and 21 mA, respectively. In both cases the average current density is 8.58×10^7 A/m² and pulse duration is 1.88 μ s.

2. Uniform junction diode (modified program)

Figures 147-151 show the results of a 7 mA excitation pulse amplitude for a uniform junction diode. The current distributions at various times are shown in Figs. 147a,b.

At 0.17 μs from the beginning of the pulse, the current is almost constant through all strips on the diode. At 13.98 μs , a broad filament is beginning to form, becoming better defined by 15.98 μs . From that time conductance changes rapidly. At 16.98 μs (Fig. 147b) the broad filament has been broken into two filaments, each with a fine structure. These evolve rapidly with the fine structure almost gone by 17.48 μs . The calculations have to be terminated at 17.78 μs because conditions are then changing too rapidly to obtain stable solutions. The filaments then have a peak current density about ten times higher than the original current density and about 100 times higher than the current density of the remainder of the diode.

Figures 148a and b show three-dimensional, temporal development of temperature profiles in the n region. They show that the growth of thermal filaments coincides with the growth of current filaments shown in Figs. 147a and b. At 0.17 μs , the junction was at a uniform temperature except at the diode edges and has a higher temperature than that of the n region. Evolution of the broad filament, times 13.98 and 15.98 μs , is shown. At 16.98 μs (Fig. 148b) the double filaments with the fine current structure are seen to exhibit a corresponding thermal distribution. These filaments rapidly sharpen, as shown in the profiles of 17.48 and 17.78 μs . The temperature of the peaks at 17.78 μs is 1100 K, while that midway between a peak and the diode edge is about



(a)

Fig. 147. Current distributions at different times in a uniform junction diode for an excitation pulse amplitude of 7 mA.

(a) Current distributions at times 0.17, 13.98, 15.98, and 17.78 μs .

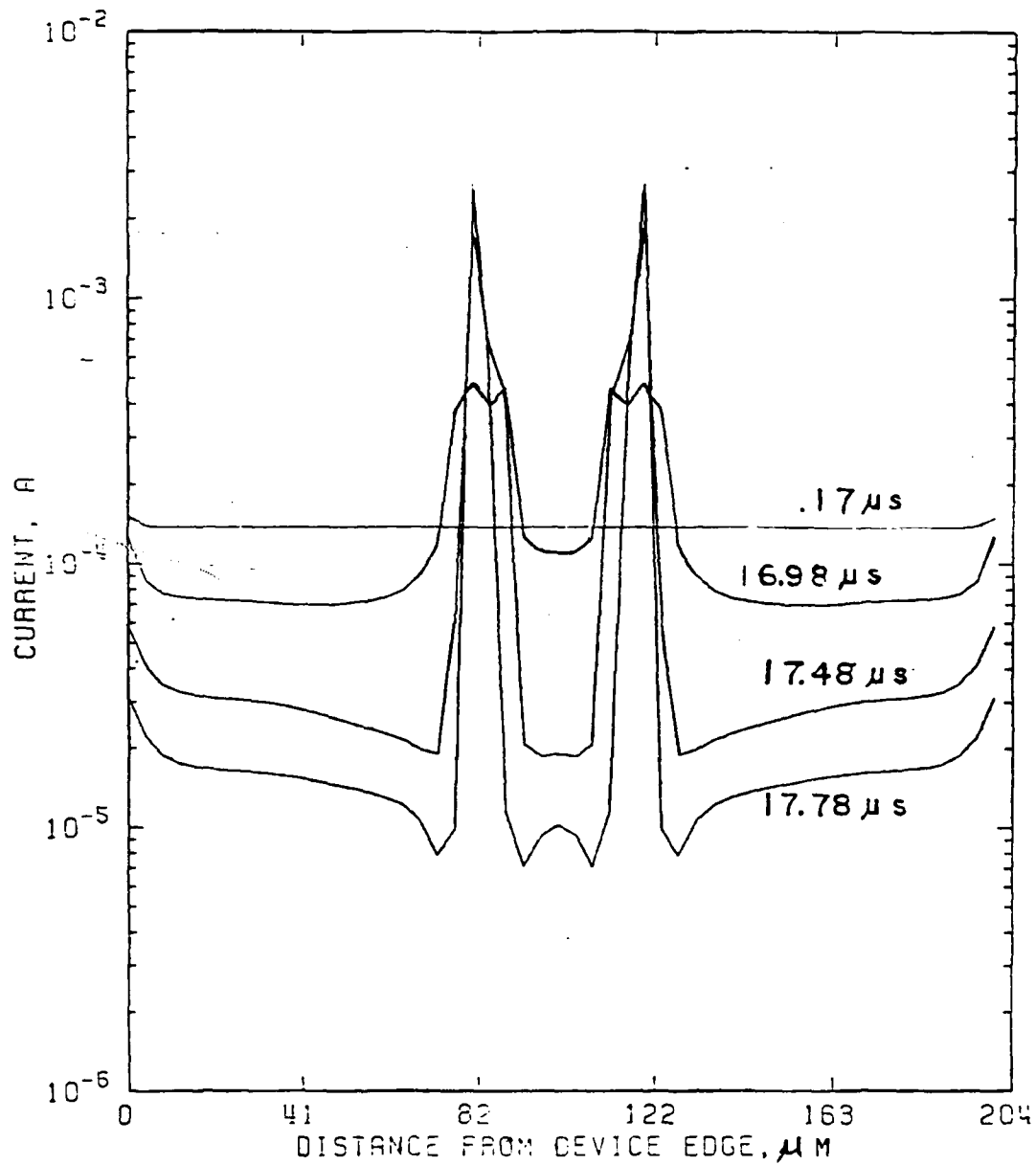


Fig. 147 (b). Current distributions at times 0.17, 16.98, 17.48, 17.78 μs .

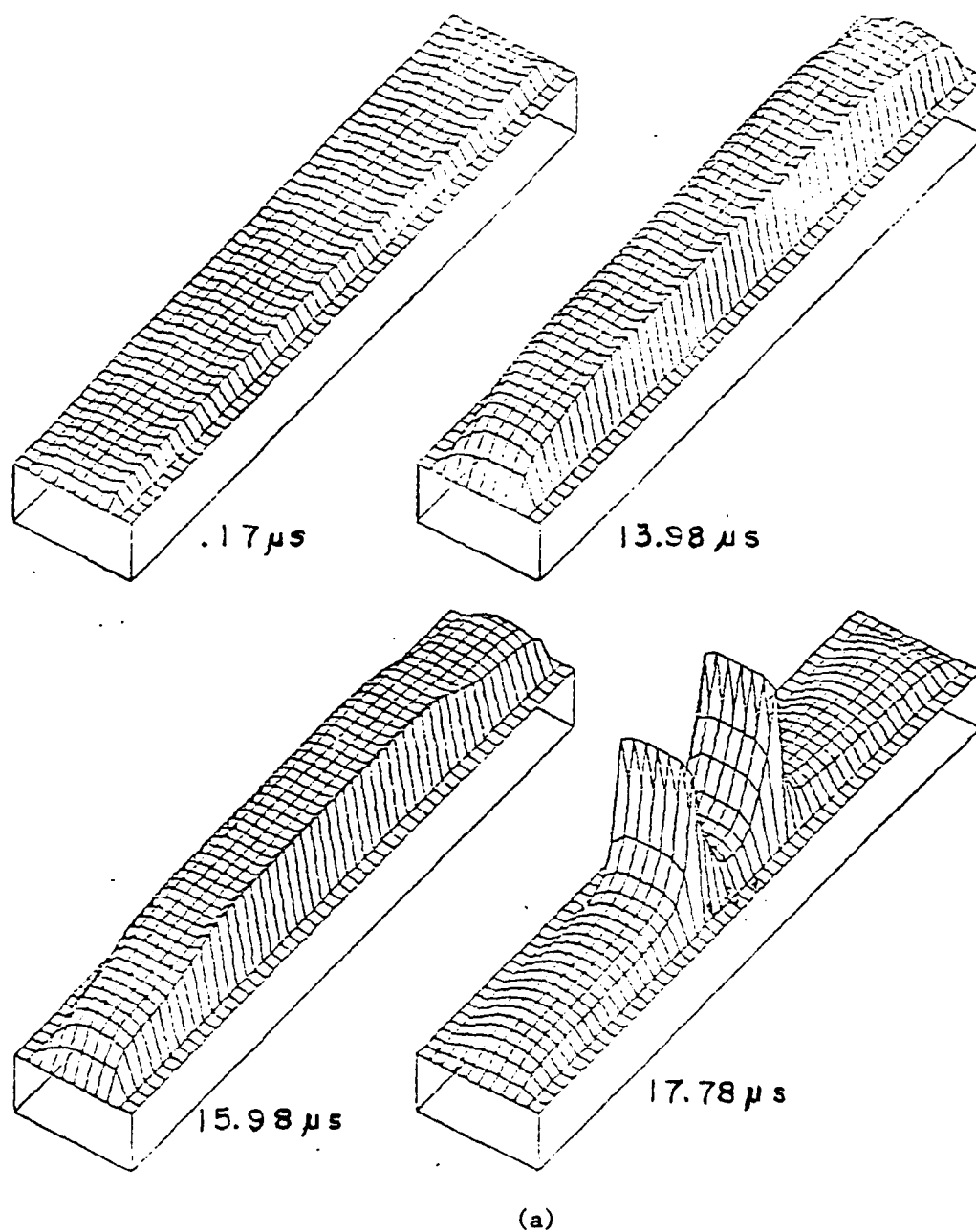


Fig. 148. Temporal development of temperature profiles of uniform junction diode for a 7 mA pulse amplitude. Note the higher temperatures of the junction region compared to the n region prior to the development of the double filaments.
(a) Temperature profiles at times of 0.17, 13.98, 15.98 and 17.78 μs .

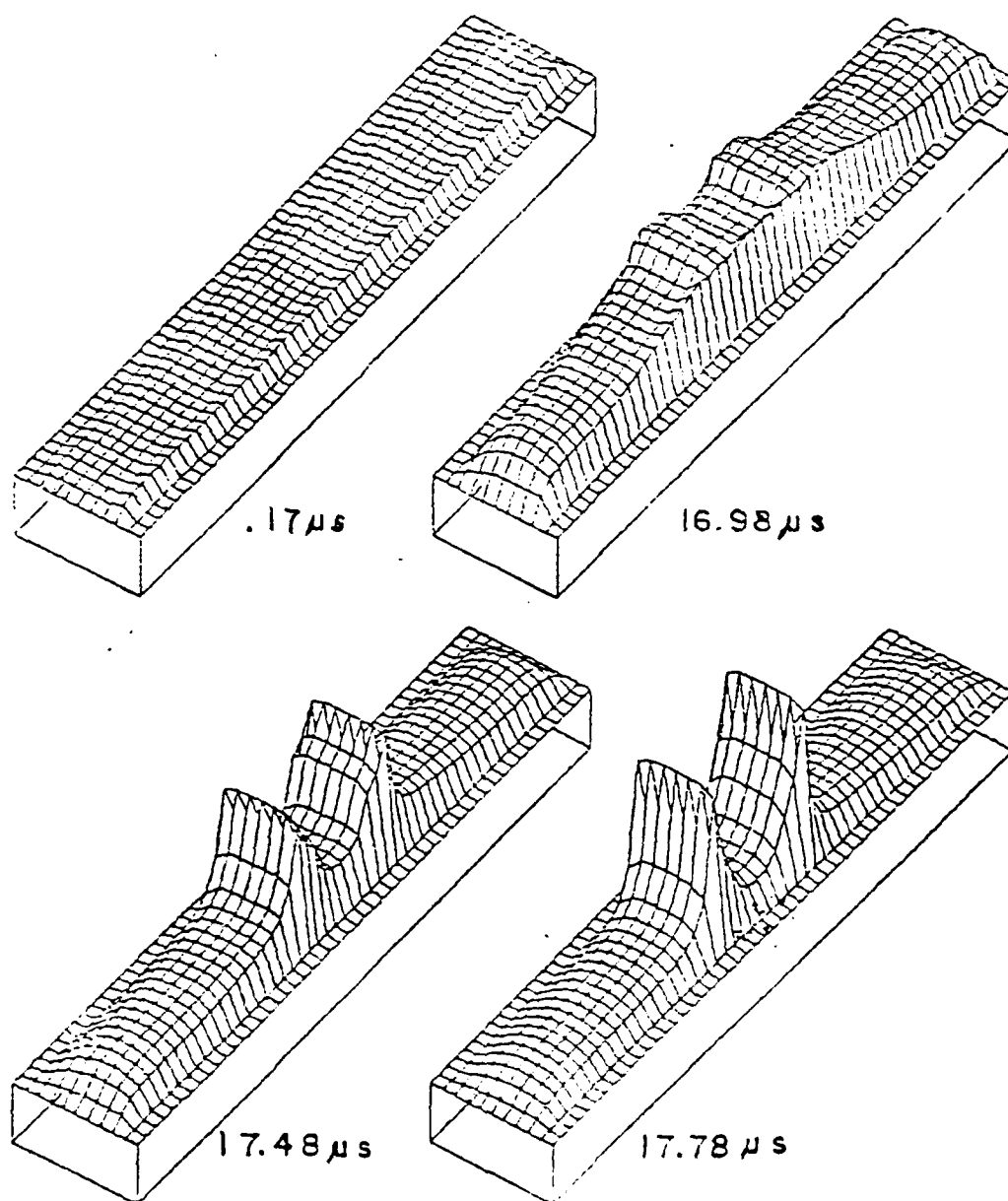
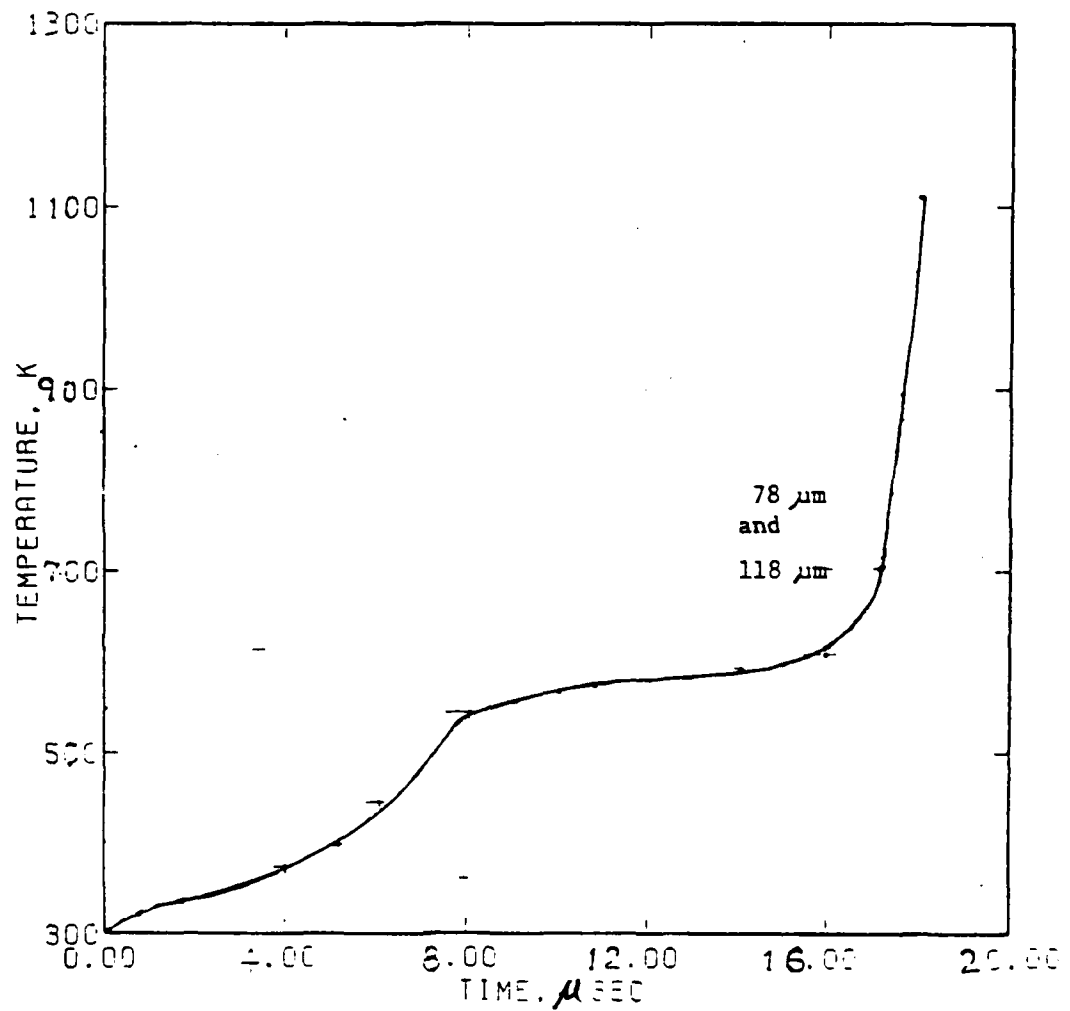


Fig. 148 (b). Temperature profiles at times 0.17 , 16.98 , 17.48 , and $17.78 \mu s$.



(a)

Fig. 149. Temporal development of temperature in a uniform junction diode at a pulse amplitude of 7 mA.
(a) Temperature profile of the mid points of the n region of strips with current filaments (78 and 118 μm from the device edge).

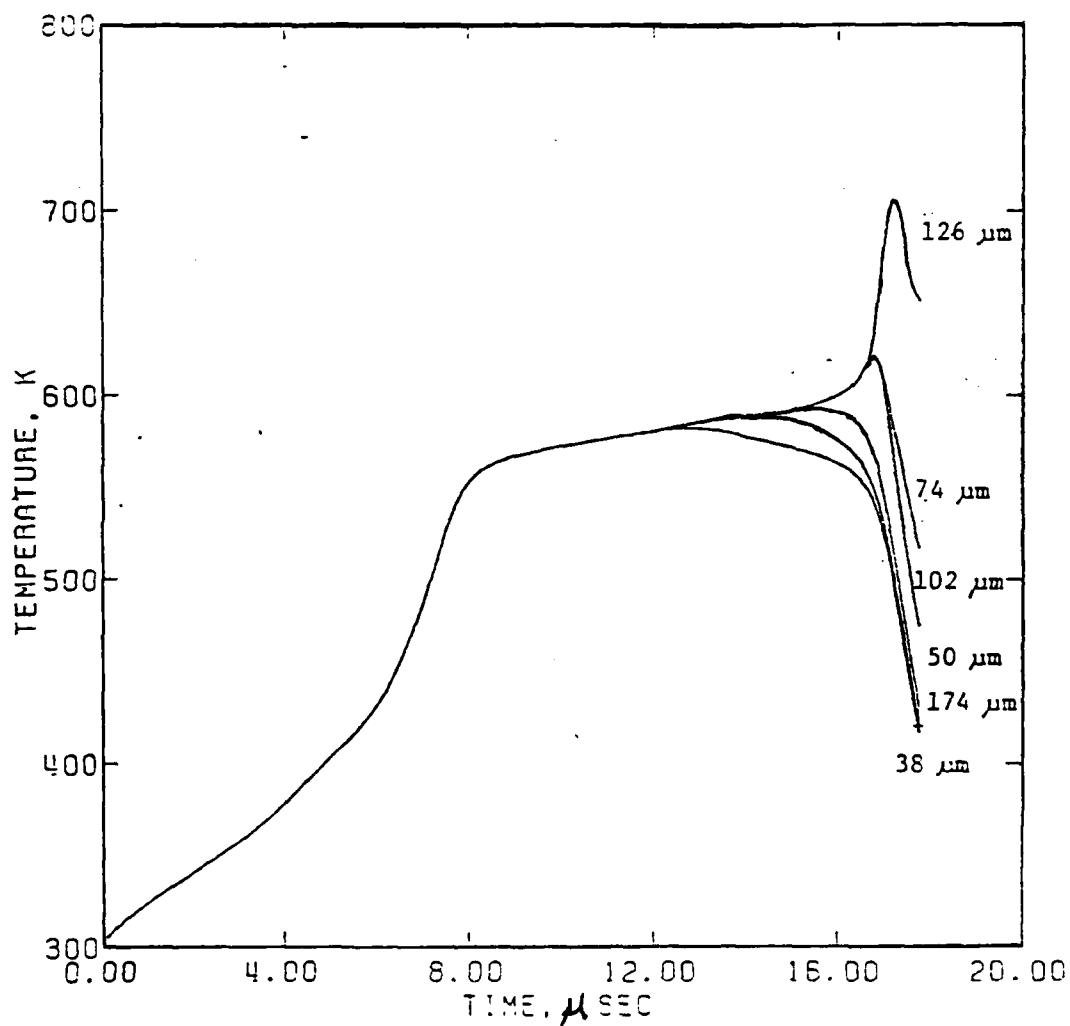


Fig. 149 (b). Temperature profiles of the mid points of the n region of strips not containing current filaments (filaments are located 78 and 118 μm from the diode edge).

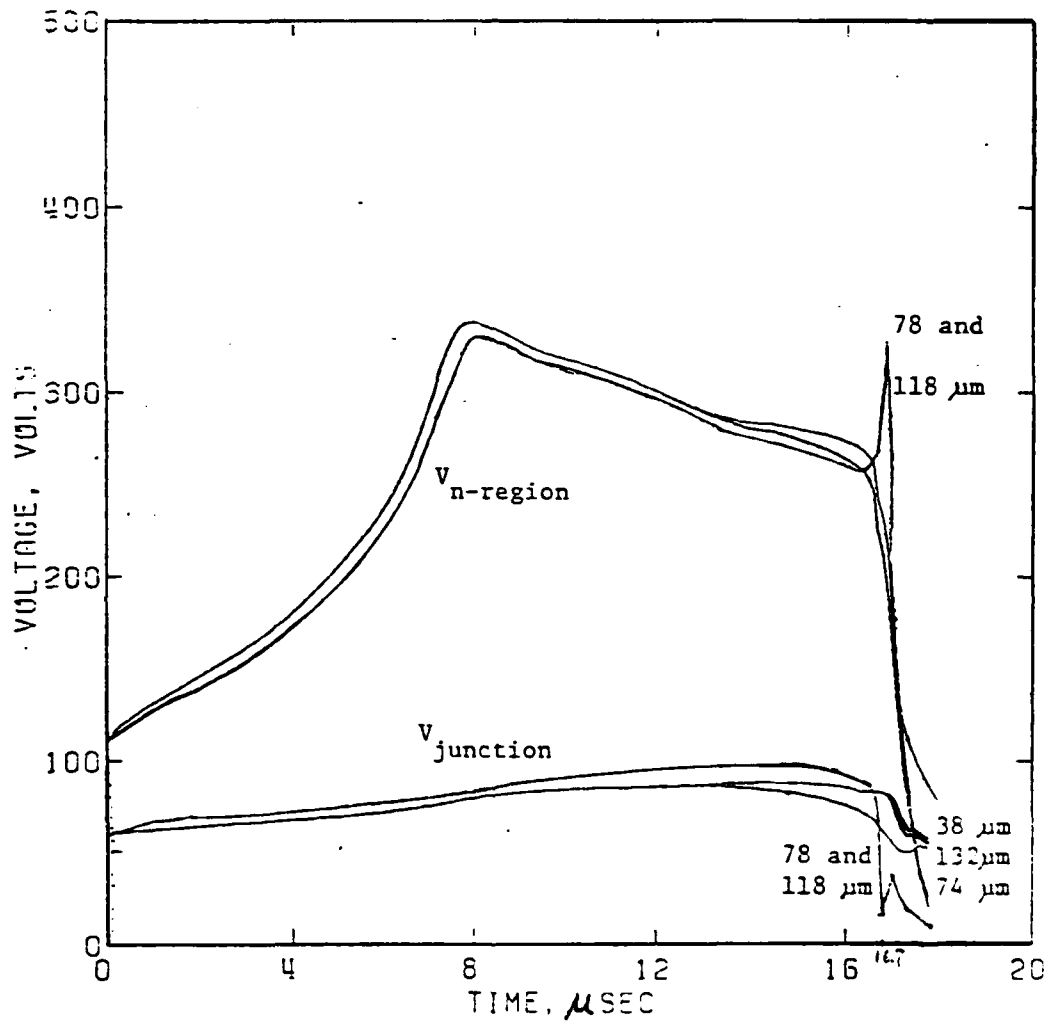


Fig. 150. Junction and n-region voltage waveforms of the indicated strips of a uniform junction diode excited by a pulse of 7 mA. Filaments form at 78 and 118 μm .

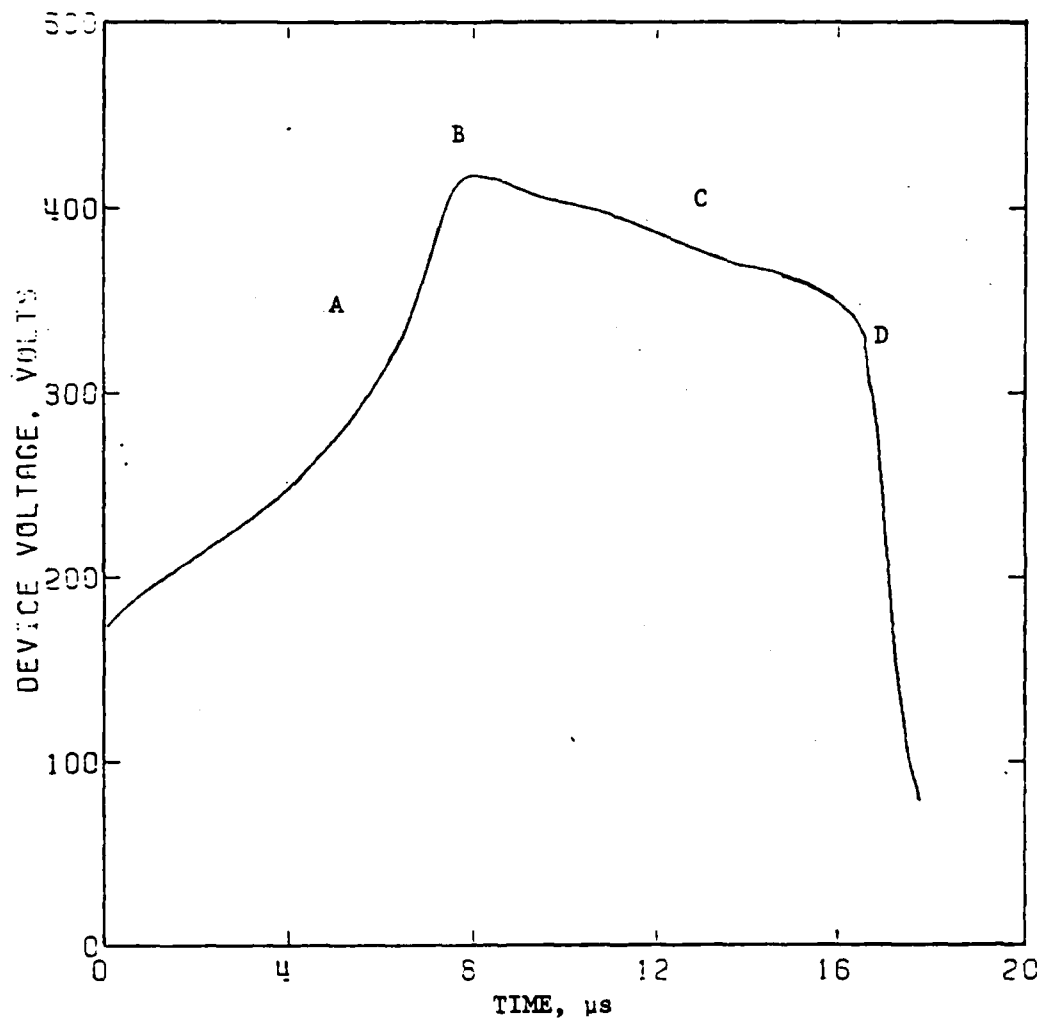


Fig. 151. Voltage waveform of a uniform junction diode for a pulse amplitude of 7 mA.

430 K. The appearance of a double filament at the low current level of 7 mA (compare to the lowest value of Baruah, 8 mA) is a surprise, since Baruah obtained double filaments only at higher levels of excitation.

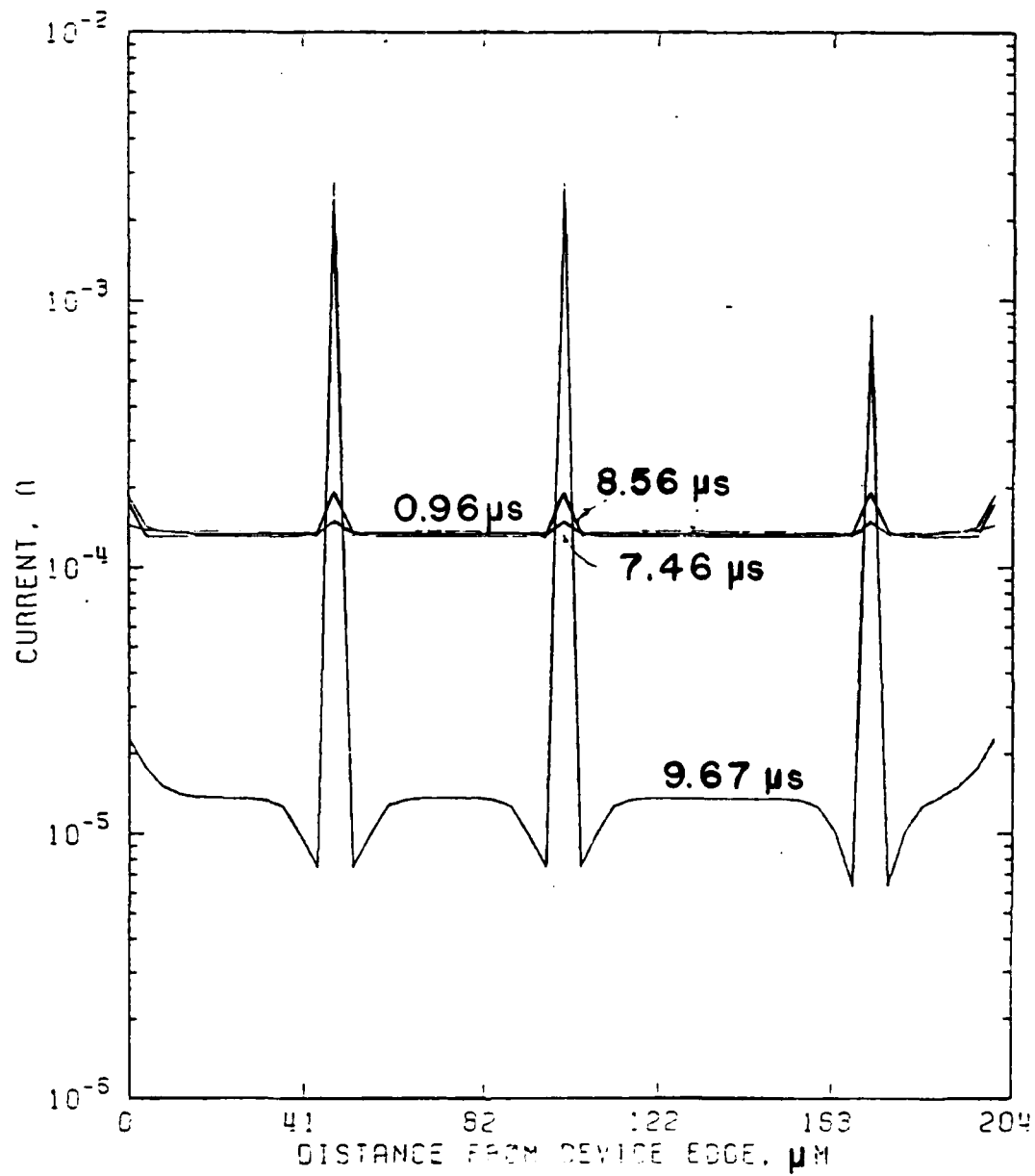
The temporal development of the temperature configuration throughout the n region is shown in Figs. 149a,b. Each curve describes the temperature-time history at the center of the n region of a particular strip. The distances show the locations of the strips from the left hand side of the diode. Figure 149a shows the temperature development at the filament locations while Fig. 149b shows those away from the filaments. The temperatures of these strips increase in the same manner until $t = 12 \mu\text{s}$. Then, the changes of the filamentation process take place, with heating at the filament locations and cooling elsewhere. Fig. 150 shows the junction voltages and the n-region voltages of various strips located away from the filaments (34, 74, 134 μm) and strips with filaments (82 and 118 μm). It may be seen that the junction voltages of the filament strips are higher than those without filaments, while the n-region voltages are lower. In this case the growth of the filament is clearly correlated to the drop in junction voltage at the filament site when the temperature at the junction goes to its fall-off value of 760 K (see Fig. 119). Comparison of the above curves with the corresponding ones of Baruah shows that changing the junction width from 4 μm to 3 μm has increased the junction temperature significantly so that the junction now plays a more dominant role in the filamentation process. Comparison of theory and experiment suggests that the 3 μm distance gives better agreement with experiment than does the 4 μm width.

Figure 151 shows the temporal development of the terminal voltage of the diode. In region A the diode is heating in both the n region and junction region with the n-region temperature coefficient of resistivity increasing with temperature. At point B the bulk resistivity of the n-region is a maximum and the diode voltage reaches a maximum of 418 V. In region C there is further heating of the n region, with the temperature coefficient of resistivity now negative. Growth of the broad filament starts at 12 μ s. Finally in region D rapid growth of the double filaments occur.

The voltage waveform of Fig. 151 may be compared with that in Fig. 125 at 8 mA obtained by Baruah. It is seen that the voltage waveform of the 7 mA calculation is very similar to that of the 8 mA calculation, with (as they should be) the times for the peak, broad filament, and sharp filaments being longer for the 7 mA case than for the 8 mA. Thus, one must regard the differences in the filament structure as being due to rather small differences in the course of the two solutions.

3. p^+n diffusion spike diode (modified program)

Figures 152-156 show the results of a 7 mA excitation pulse amplitude for a p^+n diffusion spike diode. The spike shape and locations were shown in Fig. 133. The current distributions at various times are shown in Figs. 152a and b. At 0.96 μ s from the beginning of the pulse, the current is uniform except for the edges and spike locations. At 7.46 μ s, the current distribution is almost unchanged. Between 7.46 μ s and 8.56 μ s, the current in the spikes increases three-fold. At 9.06 μ s strong current filaments have been formed at the spike locations.



(a)

Fig. 152. Current distributions in a p⁺n diffusion spike diode at the indicated times for a 7 mA pulse amplitude.

(a) Current configurations at 0.96, 7.46, 8.56, and 9.67 μs .

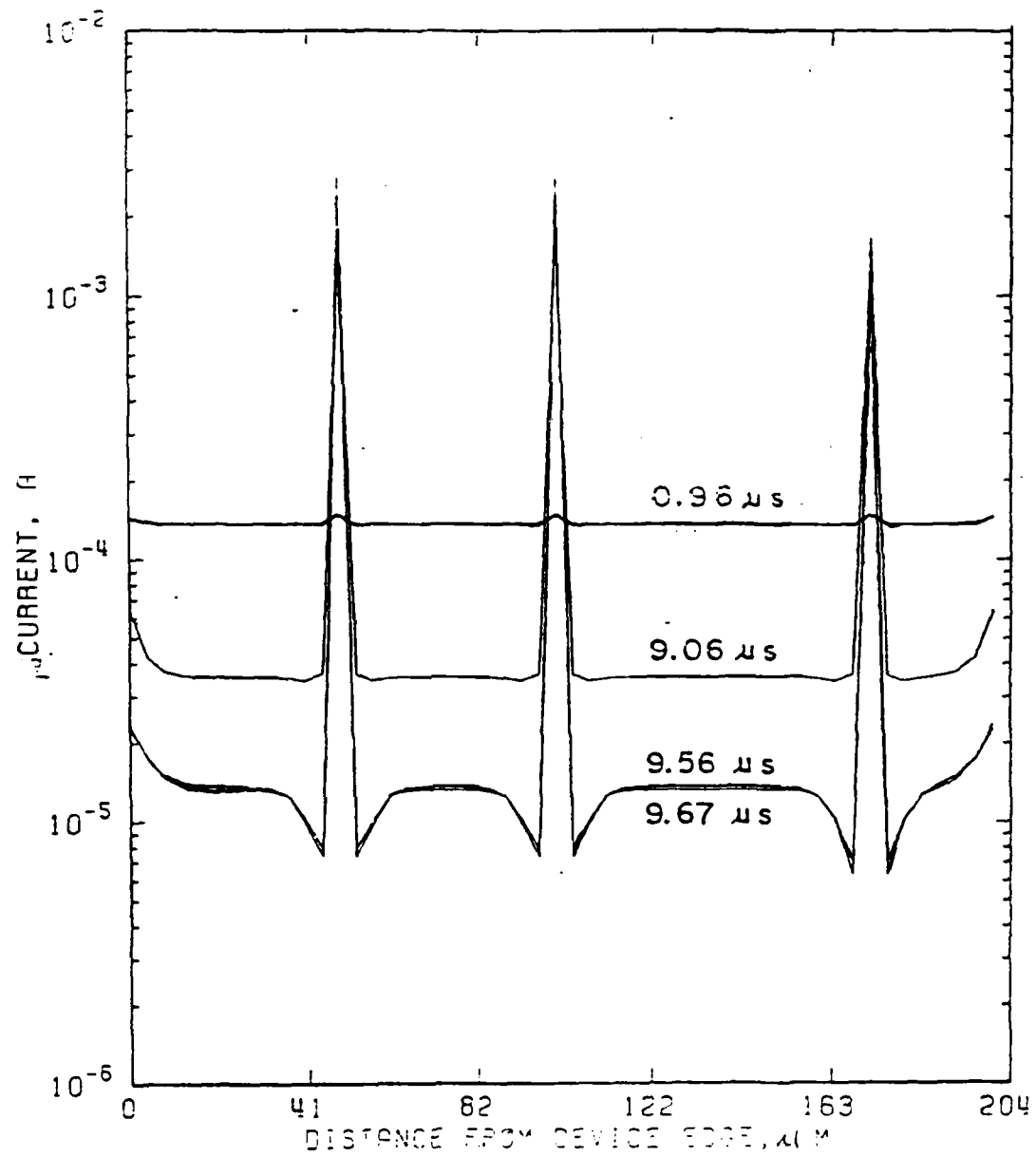


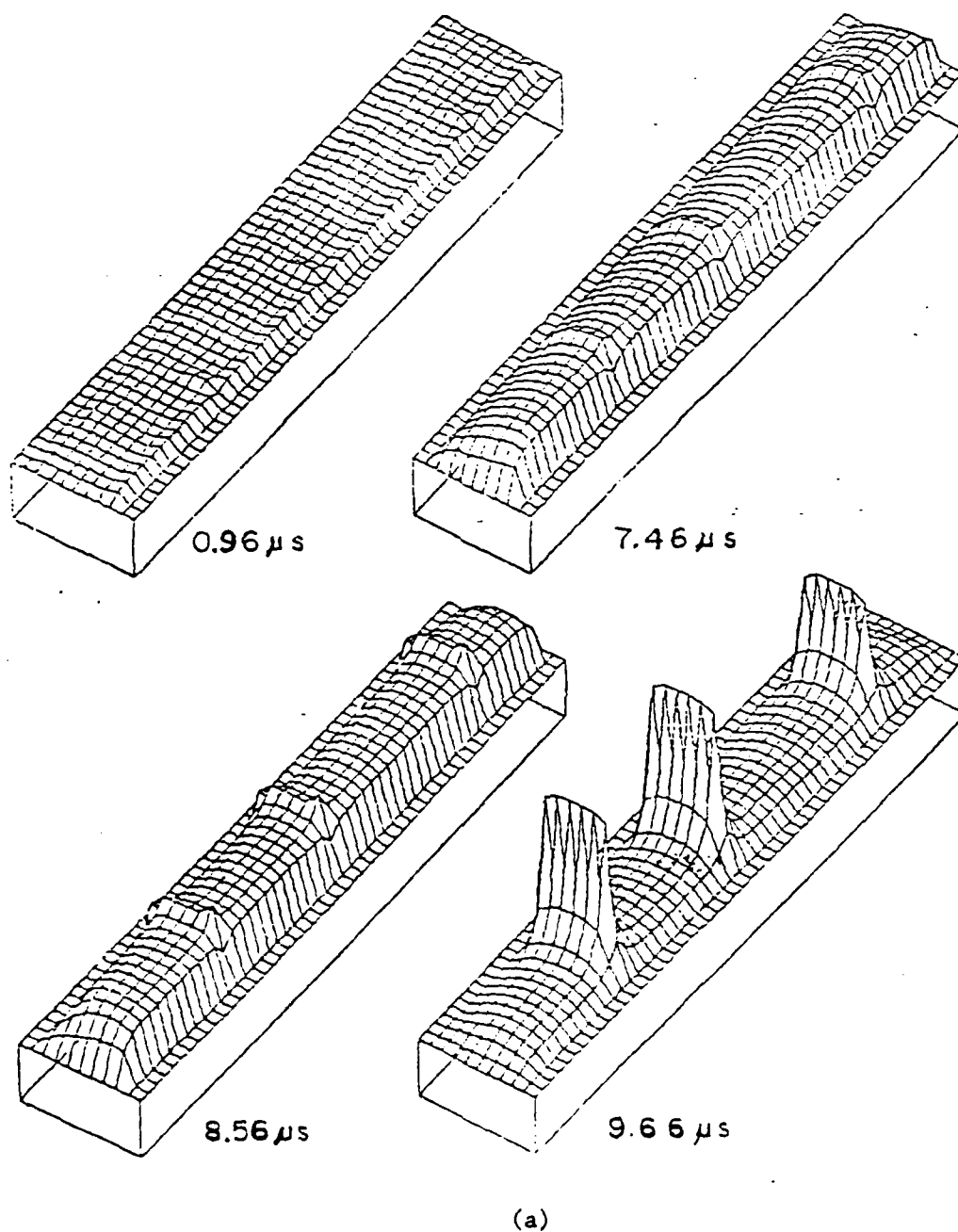
Fig. 152 (b). Current configurations at 0.96, 9.06, 9.56, and 9.67 μs .

Their further growth is shown by the current configurations at 9.56 and 9.67 μs .

Figures 153a and b show three dimensional, temporal development of temperature profiles corresponding to the current distribution of Figs. 152a,b. They show that the growth of thermal filaments correlates with the growth of the current filaments. At 0.96 μs the n region is almost uniformly heated except for small peaks at the spike locations and cooler edges. The junction was a little hotter than the n region. At 7.46 μs and 8.56 μs , the same pattern persists except that the temperature of the n region in the non-spike locations exceeds the temperature of the junction at these locations. The peak of the temperature resistivity curve at the spike locations occurs between times of 8.56 and 9.06 μs . The thermal profiles during the period of rapid growth of filament current are in the 9.06-9.67 μs figures. As filament temperature rises, the temperature elsewhere falls.

The temporal development of the temperature of the center of the n region for various strips is shown in Fig. 154. The strips at 50, 102, and 174 μm are on the spike locations, while 38, 74 and 126 μm are strips off the spikes. The curves of Fig. 154 show that the temperatures of the strips with spikes are a little higher than those of the strips off the spikes before the filaments were formed. As the filaments grew, the temperatures of the strips on the spikes also increased rapidly, while the temperatures of the strips off the spikes decreased.

Figures 155a,b show the junction and n-region voltages of strips off and on the spikes, respectively. The junction voltages of the strips containing the spikes become lower than those of the strips off



(a)

Fig. 153. Temperature profiles at the times indicated in a p^+n spike diode for a pulse of 7 mA. The three filaments are located on the strips with spikes.

(a) Temperature profiles at 0.96, 7.46, 8.56, and 9.66 μs .

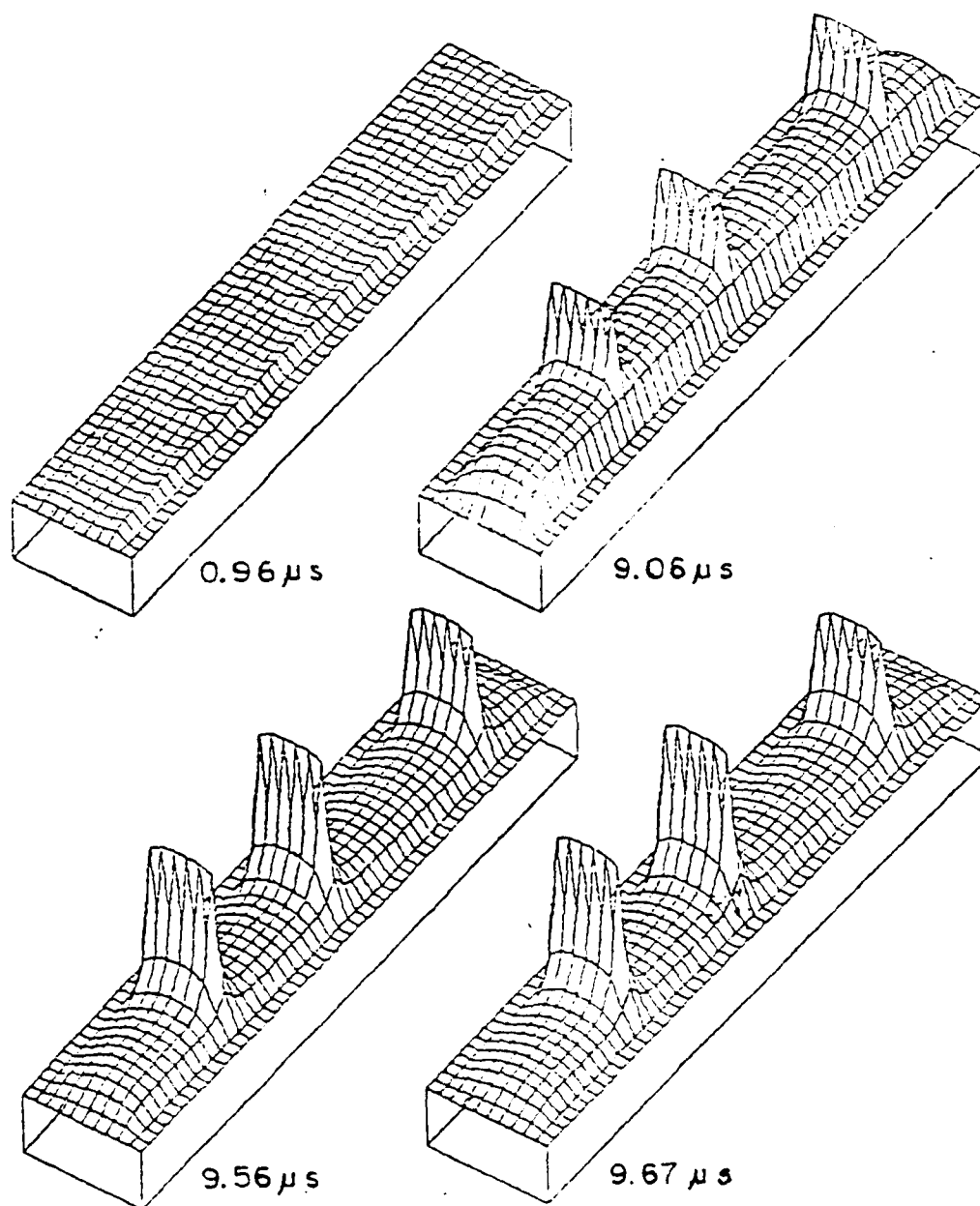


Fig. 153 (b). Temperature profiles at times of 0.96, 9.06, 9.56 and 9.67 μs .

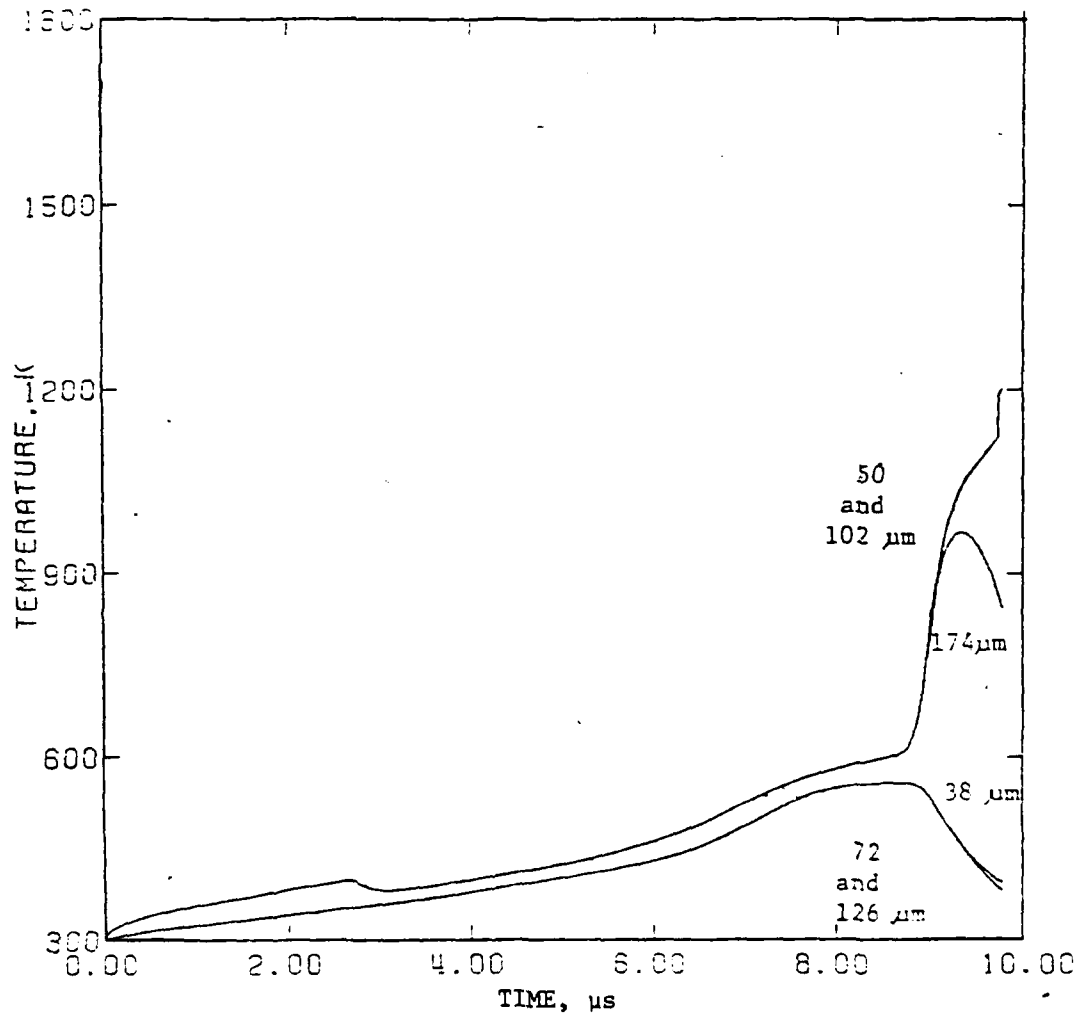
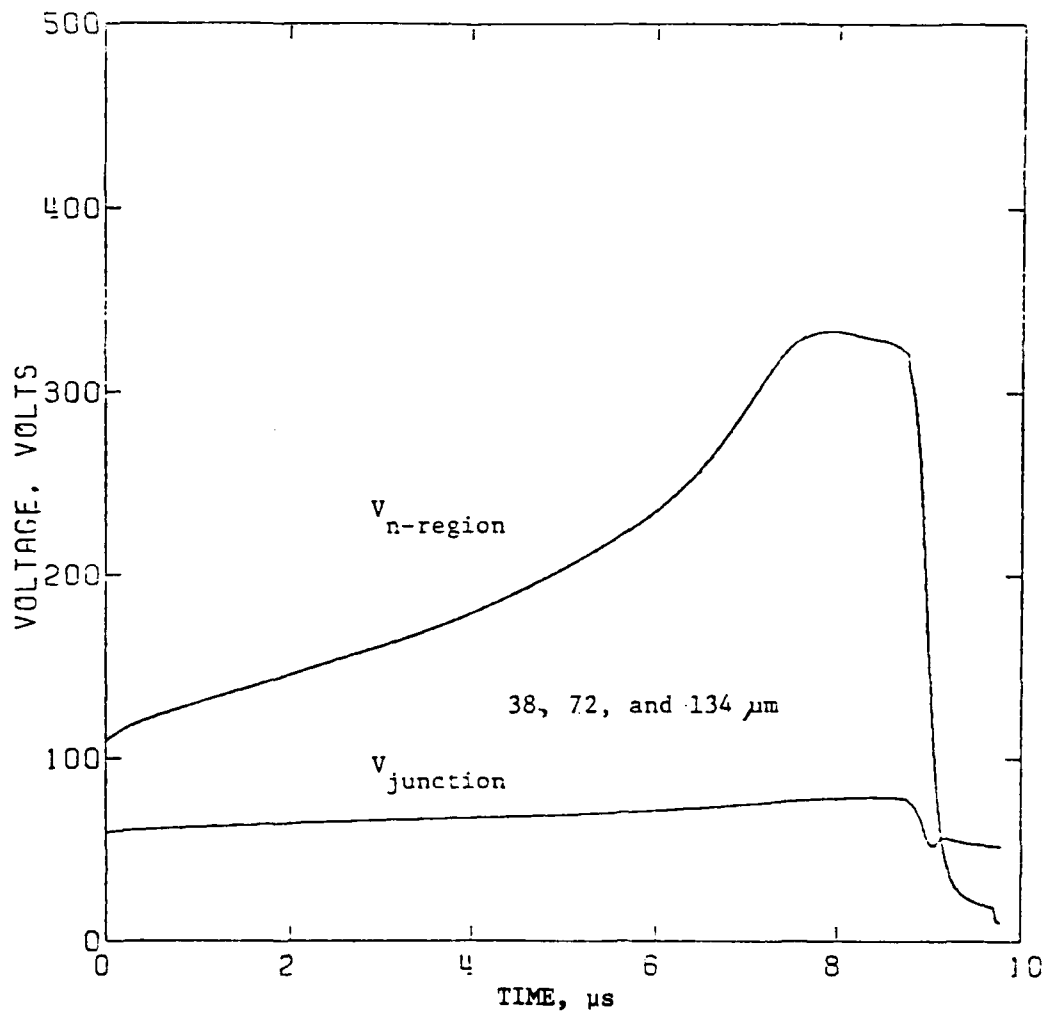


Fig. 154. The temporal development of temperature at various portions of a p⁺n spike diode with a 7 mA current pulse. Spike locations are 50, 102 and 174 μm. Temperatures are measured midway across the n region.



(a)

Fig. 155. Junction voltage and corresponding n-region voltage waveforms for a p+n spike diode.
(a) Strips away from spikes.

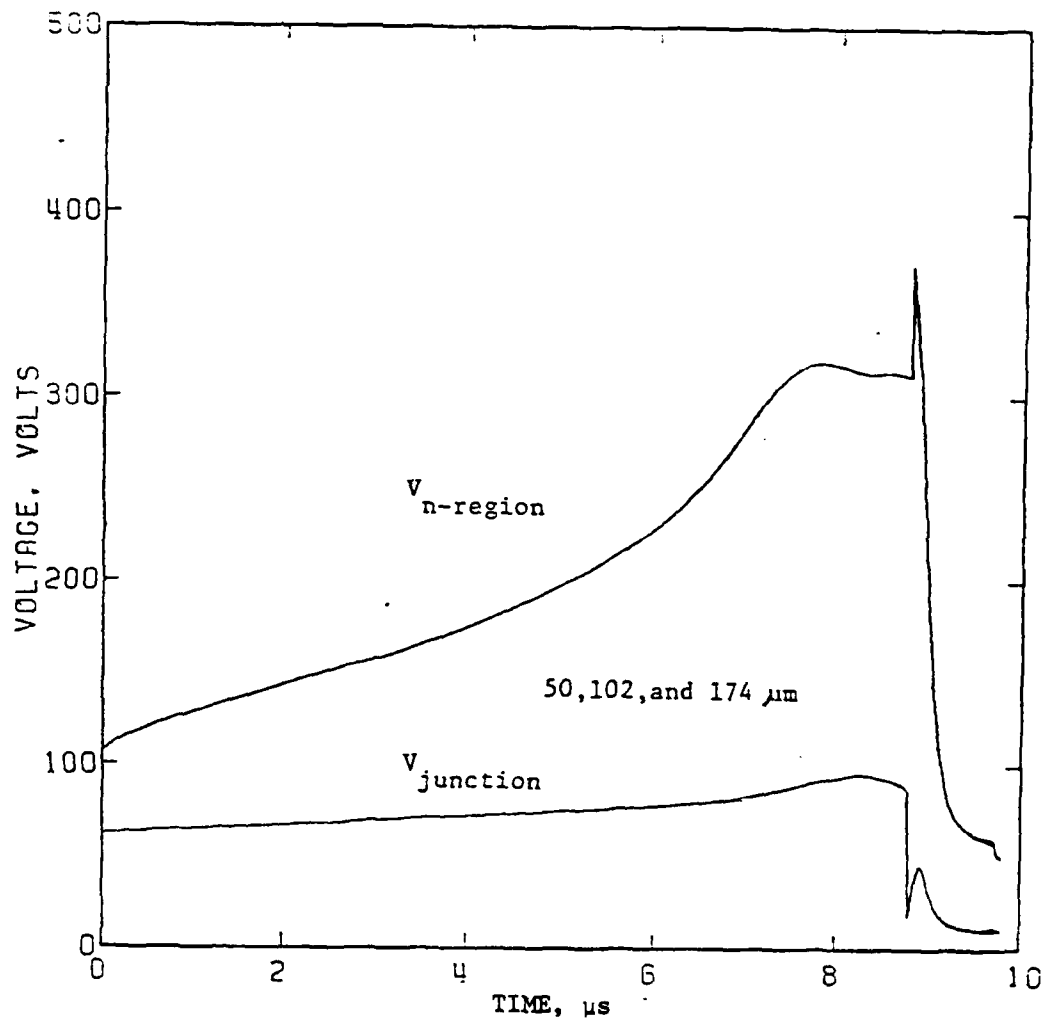


Fig. 155 (b). Strips containing spikes.

the spikes at the end of pulse. In both cases there are voltage drops as the filaments occurred. At the filament locations the voltage falls because of the high minority carrier injection at elevated temperatures, while away from the filaments the junction voltage falls because of the lowering of the junction temperature. Figure 156 shows the temporal development of the terminal voltage of the diode. In region A there is no heavy concentration of current at the spike locations, gradual heating of the n region, and a positive temperature coefficient of resistivity, similar to region A of the uniform junction case. Point B is 408 V, about 10 V lower than that of the uniform junction diode under 7 mA pulse amplitude. Region C is much shorter than that of the 7 mA uniform junction diode (Fig. 151). The current and the temperature of strips with spikes rise much faster than those of the other strips in region C. Thus the filaments grow up earlier than those of the uniform junction diode.

The voltage waveforms of Baruah for p^+n junction spike diodes and pulse amplitudes in the range 8-12 mA are shown in Fig. 139. In each case filaments formed at spikes, similar to the 7 mA pulse just described. The voltage waveforms of diodes with spikes are virtually identical to those without spikes at corresponding levels of excitation up to the cutoff point of the spike diode waveforms. Thus the energy threshold for destructive breakdown is significantly larger for the uniform junction at a particular current level. At the same time, the voltage thresholds (measured by the peak voltages) are virtually the same for a particular level of excitation. Delay times are signifi-

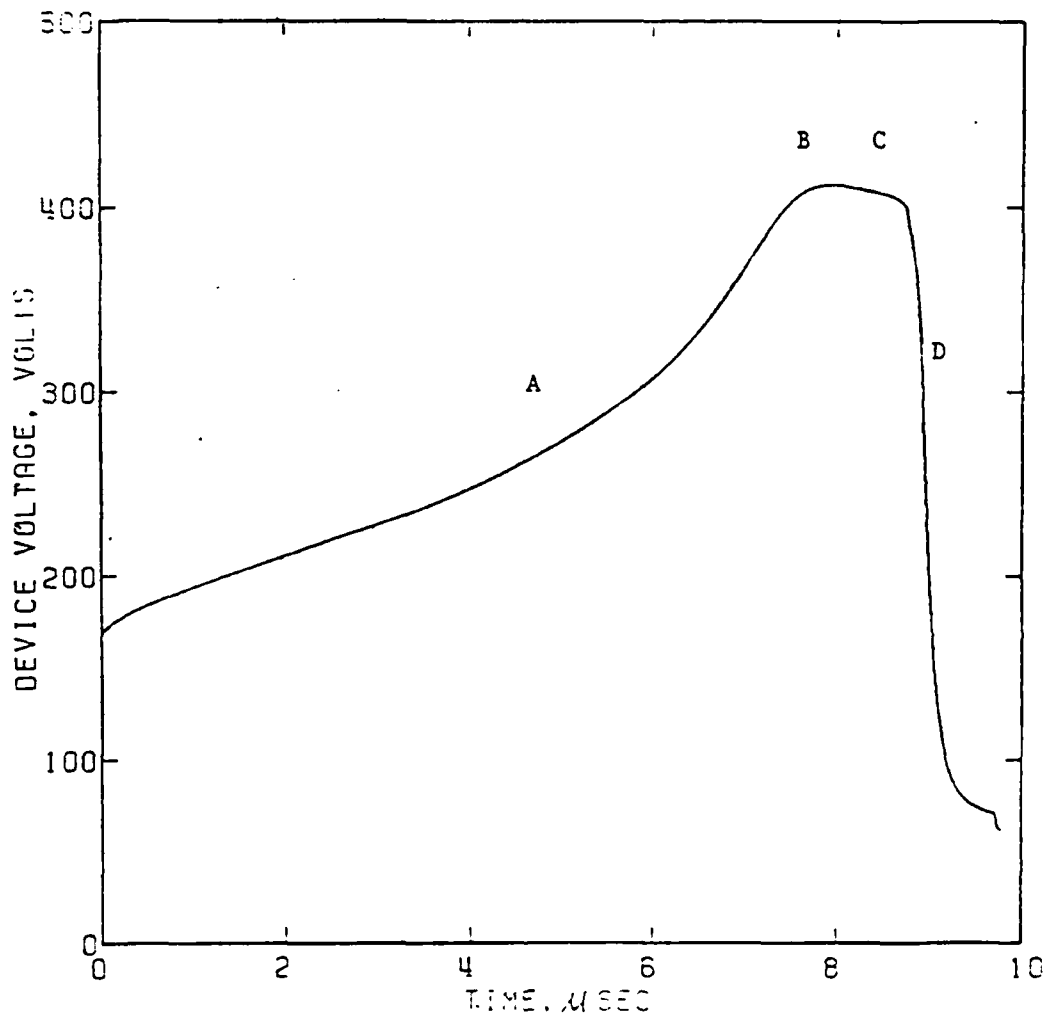


Fig. 156. Voltage waveform for a p⁺n spike diode for a pulse amplitude of 7 mA.

cantly shorter for the spiked diodes at a particular level of excitation.

4. n^+n diffusion spike diode (modified program)

Figures 157-161 show the results of 7 mA excitation pulse amplitude for an n^+n diffusion spike diode. The spike shape and the strips on which they are located are the same as in Fig. 133, but the spikes are on the n^+n junction. Figure 157 shows the current distributions at various times. Upon comparing Fig. 157 and Fig. 152b, current filaments are found to be better formed at the time 9.06 μ s for the n^+n diffusion spike diode than they are for the p^+n diffusion spike diode. The corresponding temperature profiles shown in Fig. 158 also show this feature at 9.06 μ s (p^+n diffusion spike results are shown in Fig. 153). The temperatures of the strips without spikes fell as the filaments formed at the strips with spikes.

The temporal development of the temperature for various strips is shown in Fig. 159. The strips 50, 102 and 174 μ m are the spike locations, while 38, 74 and 126 μ m are strips without spikes. As the current in the filaments increased at the spike sites, the temperatures of the strips with spikes also increased rapidly, while the temperatures of the strips without spikes decreased. All the temperatures of the strips are higher than those of a p^+n diffusion spike diode at the corresponding time. Also the temperatures of spikes at 50 and 102 μ m are higher than those of the corresponding spikes in Fig. 154. Fig. 160 shows that the junction and n-region voltage waveforms have the same shape as those in Fig. 155b for the p^+n diffusion spike diode. The de-

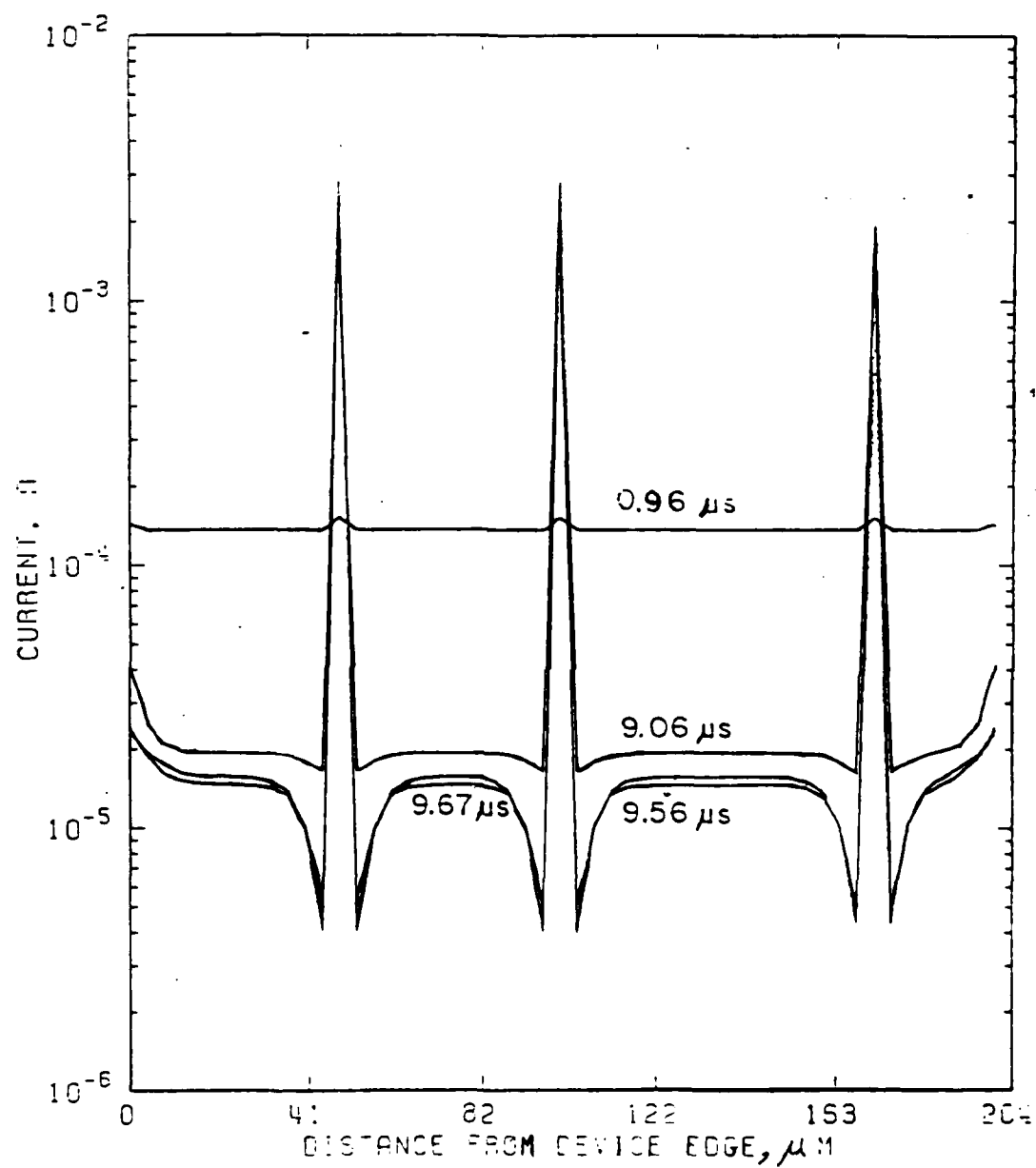


Fig. 157. Current distributions in an n^+n spike diode at the indicated times for a pulse amplitude of 7 mA.

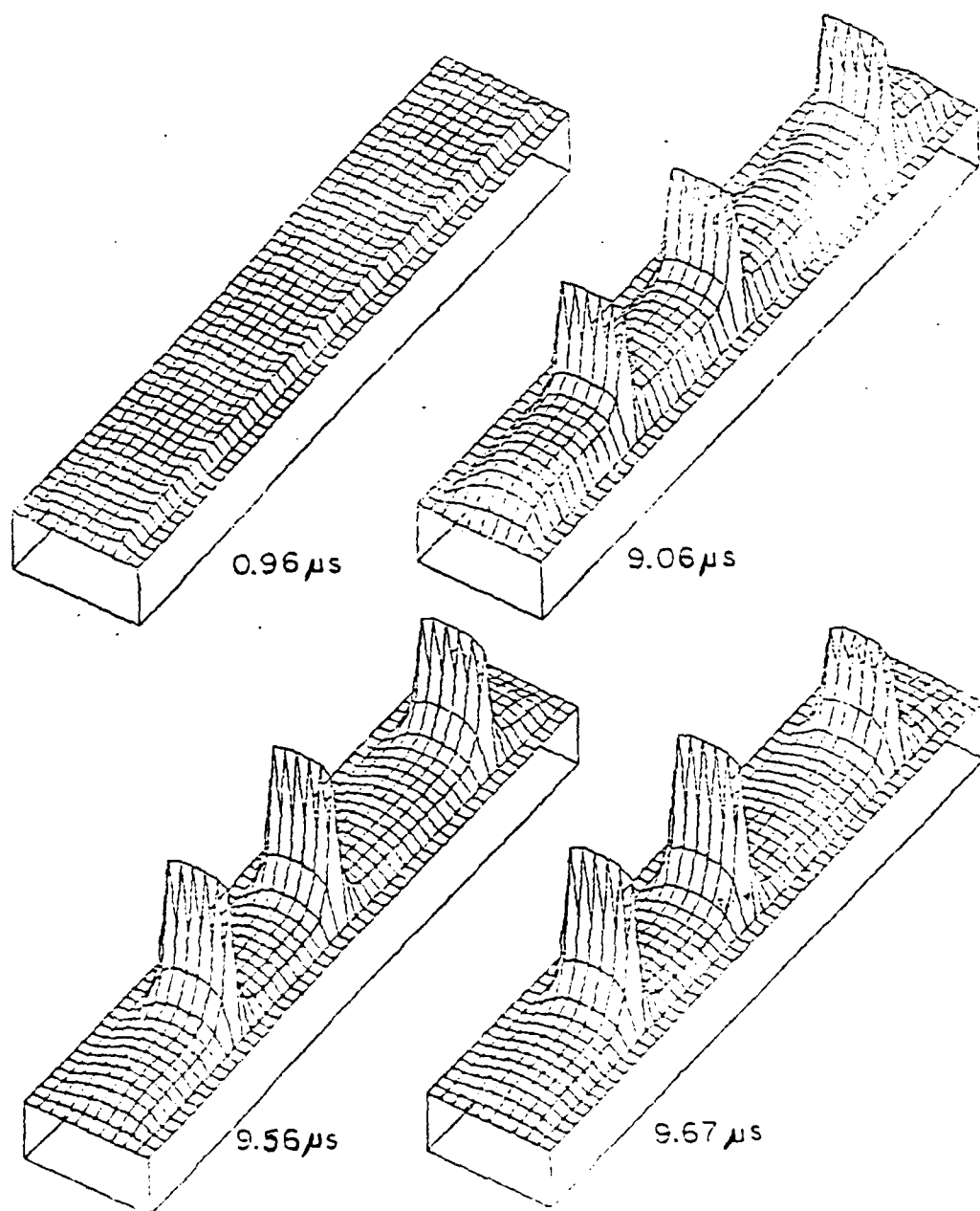


Fig. 158. Temporal development of temperature profiles of an n^+n diffusion spike diode for a 7 mA pulse amplitude. The three filaments are on the strips with spikes.

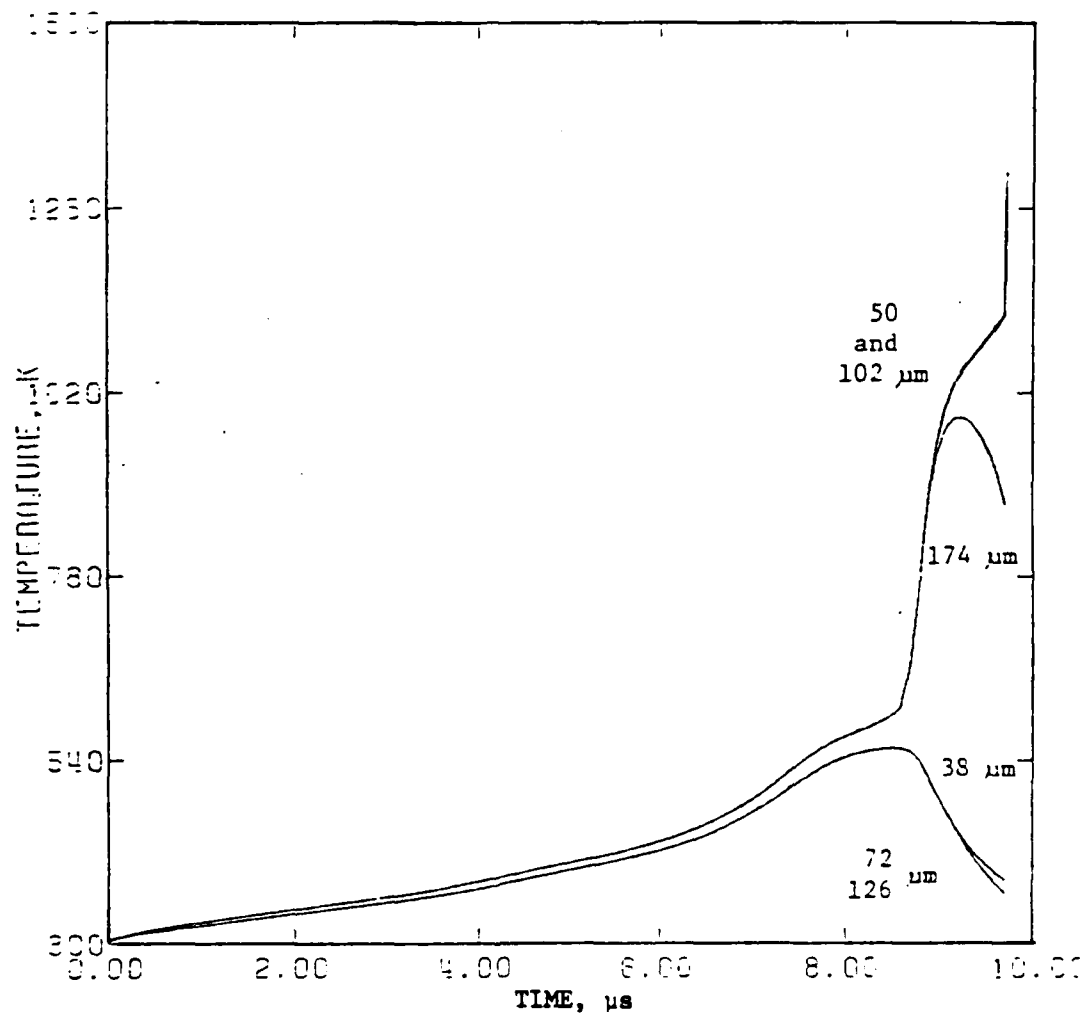


Fig. 159. The temporal development of temperature at various portions of an n^+n diffusion spike diode. Spikes are located at distances of 50, 102, 174 μm from one edge of the diode.

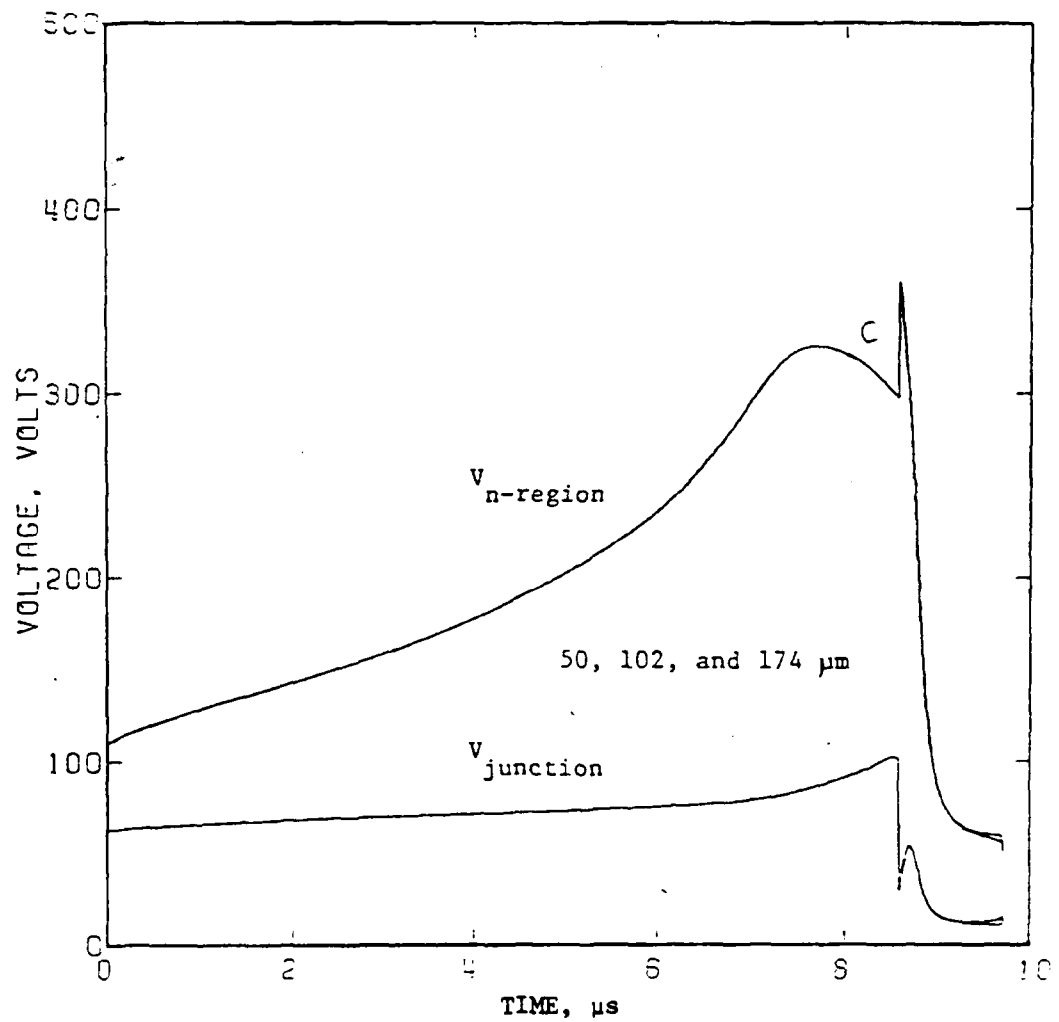


Fig. 160. Junction and corresponding n-region voltage waveforms of strips with spikes in an n^+n spike diode. Spikes are located 50, 102, and 174 μm from one edge of the diode.

vice terminal voltage waveform is shown in Fig. 161. Regions A and D are almost the same as those of the p^+n diffusion spike diode. Point B is 408 V, the same as that of Fig. 156. However, Region C is $0.18 \mu s$ shorter than that of the p^+n diffusion spike diode. This means that the current filaments of the n^+n diffusion spike diode are formed earlier than those of the p^+n diffusion spike diode shown in Fig. 157.

The filamentation process is virtually identical for the p^+n and n^+n spike diodes. At first sight it appears the two should be identical because the n region lengths of the strips with spikes are the same. However, there is a difference in the heat transfer equations that accounts for the slight behavioral difference. The comments concerning, energy thresholds, voltage threshold, and delay time made in the previous section comparing uniform junction and p^+n spike junction diodes hold for uniform junction and n^+n spike diodes.

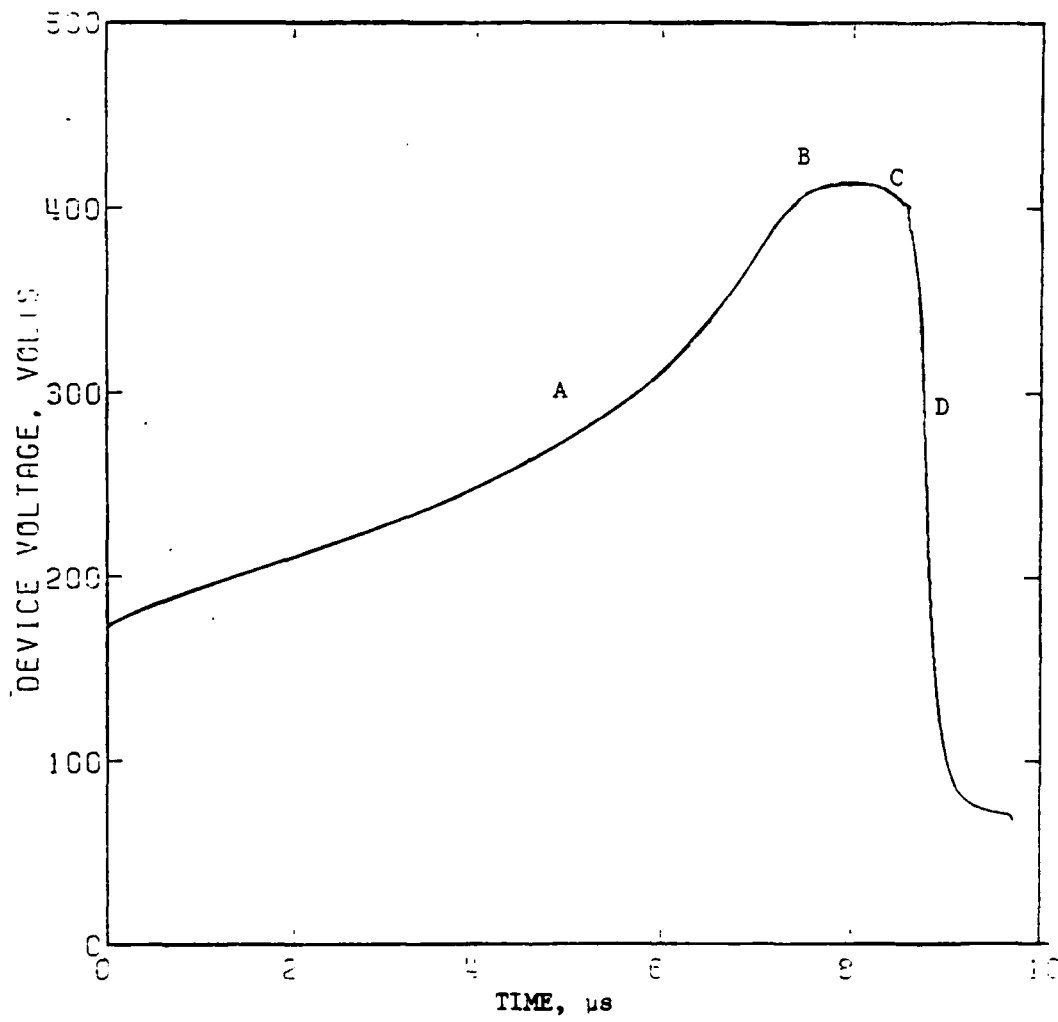


Fig. 161. Voltage waveform for a 7 mA pulse in an n^+n diffusion spike diode.

XII. COMPARISON OF THEORY AND EXPERIMENT

The results of the electrothermal model of Chapter XI will be related to the experimental results of Chapter V in Sec. A. In Sec. B the principal features of the electrothermal model will be summarized, while Sec. C will give recommendations for additional work that should be done to properly explore the range of second breakdown effects that can be treated by the model.

A. Comparison of Theory and Experiment

Comparison of theory with experiment can be made with diodes of similar geometry, i.e., for uniform junctions and for junctions with p^+n or n^+n spikes. The silicon layer thickness of the starting wafers was $0.6\text{ }\mu\text{m}$, while that of the completed devices was $0.4\text{ }\mu\text{m}$. The theoretical calculations were started before the devices were fabricated and the silicon thickness was taken to be $0.6\text{ }\mu\text{m}$. Thus the heat transfer to the substrate should be slightly more efficient in the thinner films of the experiments than the heat transfer calculated. Other considerations aside, one anticipates that a theoretical diode and an experimental diode will behave similarly if the current density of the theoretical diode is slightly less than that of the experimental.

The donor density for the n region used in the calculations was 10^{22} atoms/m^3 , which corresponds most nearly to the doping density of Wafer 2-4 (donor density estimated to be $(1.2 \pm 0.2) \times 10^{22}$ from re-

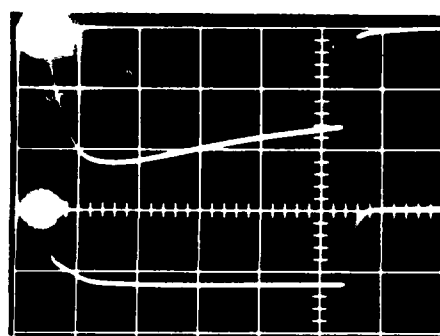
sistance measurements and $(4 \pm 2) \times 10^{22}$ atoms/m³ from avalanche voltage breakdown measurements, Tables 3 and 20). In the experimental diodes there is a transition region from the sapphire surface of 0.1 to 0.2 μm wherein the crystal structure of the silicon is relatively imperfect. In this layer the carrier mobilities should be reduced, the ionization coefficients decreased, and the lifetimes of holes and electrons reduced. These are associated with the scattering of carriers at the defect sites. A similar enhanced scattering occurs in a more highly doped system due to the impurity atoms. However, in the more highly doped system, there is also an increase in the number of carriers. The increased scattering due to crystalline imperfections, in the absence of other effects, should cause the experimental diodes to behave similar to theoretical diodes of slightly lower doping level. The true doping levels of the experimental diodes are not known; only those deduced from resistivity measurements and from low level reverse breakdown voltage measurements (Table 3) are available.

The quantities that can be compared include the voltage waveforms at corresponding current densities, temporal growth of filaments, filament configurations, breakdown thresholds (energy and current density), and delay times.

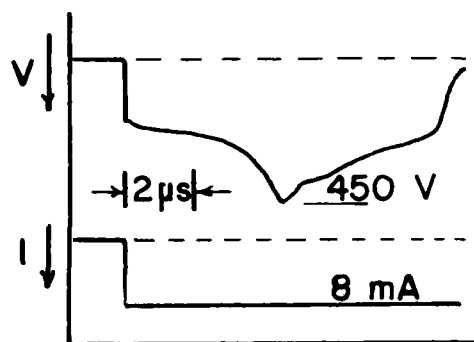
Figure 43 shows the experimental voltage waveforms for uniform junction diodes and diodes with p⁺n diffusion spikes from Wafers 2-4 and 2-5. Calculated waveforms are found in Figs. 125 and 151 for uniform junction diodes, in Figs. 139 and 156 for p⁺n spike diodes, and in Fig. 161 for an n⁺n spike diode. The diodes of Wafer 2-4 are closest in doping density to those of the calculations. Data from the above

figures and from Tables 4 and 6 can be used to compare calculated and experimental results. This is done in Fig 162 and Table 20. Figure 162 includes two waveforms not shown previously, waveforms for p^+n and n^+n spike diodes subjected to constant current pulses at the threshold of destructive second breakdown.

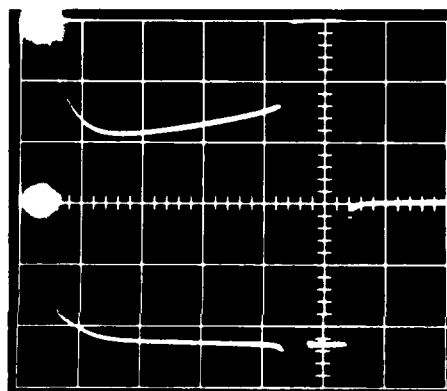
Comparison of the voltage waveforms (all for constant current pulses) reveals a gradual rise in voltage to the peak value in the theoretical curves and a steep rise in the experimental cases. The rise-time of the experimental curves corresponds to the circuit time constant and is not related to the diode characteristics. The peaks of the theoretical curves occur at voltages about twice those of the corresponding experimental curves, while the current levels of the calculated curves are smaller than those of the experimental waveforms by a factor of 3.5. An examination of Figs. 122 and 140 shows that the peak voltage for each of the theoretical waveforms is divided approximately 9:1, n region to junction. Suppose that the n region resistance were decreased by a factor of four in the theoretical diodes by increasing the doping level to 4.0×10^{22} atoms/ m^3 , consistent with the value $(4 \pm 2) \times 10^{22}$ atoms/ m^3 obtained from the avalanche voltage measurements. The voltage peak is associated with the peak of the resistivity-temperature curve of the n region of the diode. Both the shape of the resistivity-temperature curve and the temperature of the peak depend upon the doping level, with the peak shifting to lower resistivities and higher temperatures at higher doping densities. Thus a detailed calculation is needed to make an exact determination of the peak voltage and current in the theoretical diode of higher doping level when



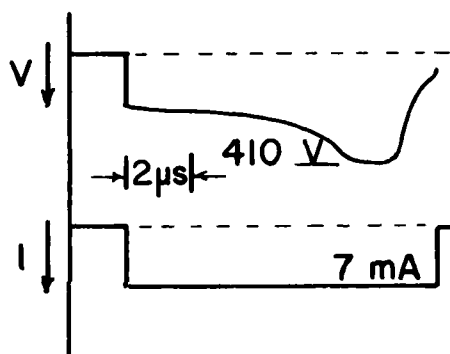
(a)



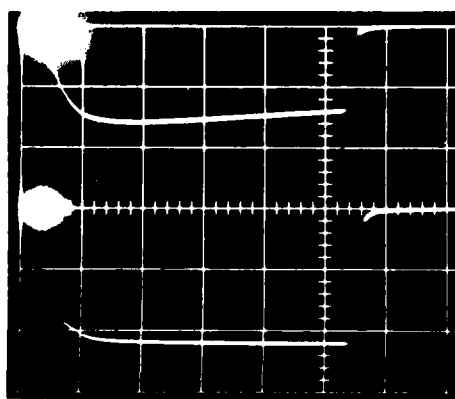
(b) time



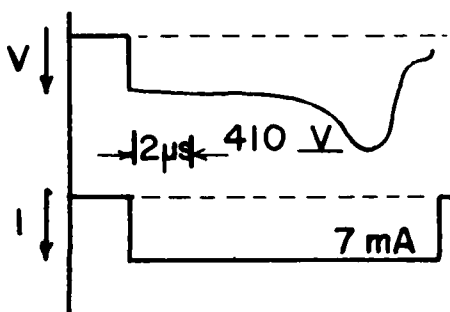
(c)



(d) time



(e)



(f) time

Fig. 162. Comparison of experimental (E) and calculated (C) waveforms. (a) Uniform junction (E), (b) uniform junction (C), (c) p-n spike junction (E), (d) p-n spike junction (C), (e) n-n spike junction (E), (f) n-n spike junction (C). For the experimental waveforms, voltage is the upper waveform and the scales are 100 V/div, 20 mA/div for (a), 10 mA/div for (c) and (e), and 2 μ s/div.

Table 20. Comparison of theory with data from diodes of Wafer 2-4.

	Uniform junction diodes		p n spike diodes		n n spike diodes	
	Theory	Experiment	Theory	Experiment	Theory	Experiment
Doping level (m^{-3}) Resistivity data Breakdown data	1×10^{22}	$(1.2 \pm 0.2) \times 10^{22}$ $(4 \pm 2) \times 10^{22}$	1×10^{22}	$(1.2 \pm 0.2) \times 10^{22}$ $(4 \pm 2) \times 10^{22}$	1×10^{22}	$(1.2 \pm 0.2) \times 10^{22}$ $(4 \pm 2) \times 10^{22}$
N-region length (μm)	30	30	30	30	30	30
Diode width (μm)	204	204	204	204	204	204
Silicon thickness (μm)	0.6	0.4	0.6	0.4	0.6	0.4
I (threshold) (mA)	9	32 ± 3	7	24 ± 2	7	25 ± 3
J_{AVG} (threshold) (10^8 A/m^2)	0.75	4 ± 0.4	0.58	3.0 ± 0.3	0.58	3.1 ± 0.4
Prefailure energy (μJ)	27	51 ± 5	19	27 ± 3	18	25 ± 7
Delay time for sharp filament (μs)	9.2	9.8	8.8	9.8	8.6	9.8
Delay time to destruction (μs)	10	10	10	10	10	10

the diode is at the threshold of destructive second breakdown for a 10 μ s pulse. However, a rough estimate of conditions at the higher doping level can be made if it is assumed that the power input at the theoretical voltage peak is the same for both doping levels. Let subscript 1 be used to describe the waveform parameters calculated for doping density 1.0×10^{22} atoms/ m^3 and subscript 2 to describe the estimated parameters associated with the doping density of 4.0×10^{22} atoms/ m^3 . Then the assumption is that $P_1 = P_2$ at the peaks of the respective voltage waveforms. The n-region resistivities will be designated R_1 and R_2 and it is assumed that $R_1 = 4R_2$, i.e., at the (different) temperatures of the peak voltages the resistances of the n regions are in the ratio of the n-region doping levels. An examination of Fig. 25 suggests that this is approximately correct. Then the peak voltage V_2 and the current I_2 can be predicted.

$$P_1 = P_2$$

$$V_1^2/R_1 = V_2^2/R_2 = V_2^2/(R_1/4) \quad \text{Thus } V_2 = 1/2V_1 \text{ and } I_2 = 2I_1$$

Thus, increasing the doping level by a factor of four decreases the theoretical peak voltage by a factor of two and increases the current by a factor of two. The voltage obtained is then consistent with the experimental value, while the current is too small by a factor of 0.6. Considering the approximate nature of the assumptions for the extrapolation to the higher doping density, the agreement suggests that the experimental diodes have doping densities about four times those of the theoretical diodes.

The dropoff in voltage a few tenths of a microsecond before the end of each of the calculated waveforms accompanies the growth of a

narrow filament. A similar drop occurs in the experimental waveforms (see Fig. 79d), but the drop is even more rapid than that calculated and it continues through the melt transition.

The theoretical waveforms also contain some fine structure that is not present experimentally. Microscopic inhomogenities in the diodes could wash out the fine structure, so the experimental and theoretical results are not inconsistent.

Both the theory and the experiments show that filaments are produced when the current amplitude is sufficiently high. At current amplitudes close to the threshold for destructive second breakdown, the theory indicates growth of a single filament or of double filaments across the n region in uniform junction diodes. A single filament is always along the symmetry axis of the diode, while double filaments are symmetrically located about the symmetry axis. In the experiments appreciable heating of the n region allowed one to anticipate the threshold for destructive second breakdown. However, filaments were observed in only a few cases during their growth stages and these appeared very close to the end of the excitation pulse. Only a single filament, randomly located, was observed in each diode. In the calculations, the narrow filament(s) grew just a few tenths of a microsecond before the end of the pulse at the threshold of second breakdown. Thus the features of filament growth are similar in theory and experiment. Double filaments symmetric about the symmetry axis of the diode have been observed in the uniform junction diodes of Wafer 2-5.

The summary of damage morphology given in Fig. 57 for Wafer 2-4 shows that filament locations in uniform junction diodes are randomly

located. Both the theory and the experiments show that the narrow filaments start very close to the end of the pulse for a near-threshold pulse and that these narrow filaments evolve very rapidly. The cause of the double filaments in the theory is thought to be associated with the detailed evolution of the temperature configuration, which makes it possible for a junction region away from the center of the device to become more conducting than the center of the device. In a real device there are geometric irregularities in local doping level and thickness that could readily determine the locations of the single filament and preclude the formation of double filaments.

Theory and experiment agree in their results on diodes containing spikes on the p^+n or n^+n junctions. The spike locations serve as regions of current concentration from the beginning of each exciting pulse. Spikes on the p^+n junction are much more effective in localizing the current distribution early in the pulse than are spikes on the n^+n junction. However, until the n region and the junction have become sufficiently heated, the voltage waveforms of spiked diodes are similar to those of uniform junction diodes excited with the same current densities. Growth of the narrow filaments start earlier in spiked diodes than in uniform junction diodes excited with comparable current densities. If the pulse amplitude is chosen so that the threshold for destructive second breakdown occurs at the end of pulses of the same length (same delay time), the amplitude of these pulses will be less for spiked diodes than for uniform junction diodes. Table 20 presents quantitative comparisons of the theoretical and experimental current, current density, and total energy input at the threshold for destruc-

tive second breakdown for uniform junction and spiked diodes. The current and current density thresholds of spiked diodes are 78% and $(75 \pm 17)\%$ of those for uniform junction diodes for theoretical and experimental diodes, respectively. The corresponding percentages for the threshold energies are 70% and $(51 \pm 20\%)$. Both theory and experiment show that spikes on the p^+n junction and spikes on the n^+n junction modify the current configuration in virtually the same manner.

The delay times to the threshold of destructive second breakdown have been determined experimentally (Figs. 84-89) and theoretically (Figs. 126, 129, 141, 142). In each case the input energy has been found to vary as the square root of the delay time, consistent with the Wunsch-Bell model. The current threshold is consistent with the $\rho^{-3/4}$ dependence predicted by Budenstein, Pontius and Smith.

In the diodes of Wafer 2-5, filaments are observed to originate at junction sites and to grow into the n region. This is the behavior described in Sec. C of Chapter II. In the few cases where filaments could be observed in diodes of Wafer 2-4 during their growth, these filaments also originated at the junction and grew into the n region. Both the calculations performed by Baruah and those of Liou (using a narrower junction width than Baruah) indicated that the junction played an important role on the initiation of growth of the narrow filament. In addition, Liou's results showed a stronger temperature gradient during the prefilamentation stage between junction and n region, with the junction being the hotter region. The experimental data also shows the junction region to be hotter. Thus the estimate of junction width used by Liou ($3 \mu\text{m}$) is probably better than that used by Baruah ($4 \mu\text{m}$). The

larger width is encountered in the calculation of the JVT characteristics at high current densities and high temperatures. This is just the region where there is reason to doubt the validity of the constitutive equations. Thus the present work points to a need to better characterize the high temperature behavior of the system. With regard to the present electrothermal model, this suggests the basic model is capable of giving still better results if the proper constitutive equations could be used.

In making comparisons between the theory and the experimental results, no use was made of the data on voltage thresholds. The reason for this is that the theoretical calculations were performed with a constant current constraint, while the voltage threshold data were obtained with a constant impedance generator. Figures 43 and 79 show waveforms for the constant impedance generator circuit and the constant current circuit, respectively. These voltage waveforms are sufficiently different that it was felt that the calculated results could only be compared with the experimental ones with the constant current pulses.

B. Principal Features of the Electrothermal Model

1. An electrothermal model has been developed and explored which describes current filamentation in a planar thin film device. The computer code that accomplishes this requires only modest CPU times (several minutes per microsecond of test pulse) and modest core storage (256K). Heat transfer is included in a more rigorous manner than in most approximate models.

2. The model yields detailed current profiles, temperature distributions, voltage waveform and other detailed features of the filamentation process. Calculations have been carried for narrow filament temperatures above 1200 K.
3. The model can be applied, with minor programming changes, to describe device behavior under different circuital constraints.
4. The model can be applied, with minor changes, to forward bias conditions.
5. The roles of a range of device inhomogenieties can be explored. These inhomogenieties may be in the junction contours, in local thickness of the silicon film, or in a combination of these.
6. The model has detailed the conditions leading up to filamentation, filament nucleation, evolution of the narrow filament, and the final rapid growth of the narrow filament toward the melt transition--the damage mode of second breakdown.
7. The model has been shown to be effective in exploring the roles of defects in the form of spikes on the p^+n or the n^+n junctions on filament geometry, time scale of the filamentation effects, locations of filaments, delay times, energy threshold for destructive second breakdown, current density thresholds for destructive second breakdown, and detailed features of the conduction process. The latter include the time histories of the junction voltage, junction temperature, n-region temperature, and of other quantities.

8. The principal limitation of the model is associated with the restriction that the current lines must remain parallel. Thus situations involving convergence of current lines cannot be treated properly.

C. Recommendations for Additional Work

The electrothermal model should be applied to a wider range of conditions. A minimal set of such conditions would be the geometries of the present experiments with doping levels corresponding to those of Wafers 2-1 and 2-5. The JVT characteristics would have to be generated over the desired temperature and current density ranges for each of the doping levels of 1.0×10^{23} atoms/m³. Judging from the experience obtained in the present calculations, difficulties will be encountered in these calculations because of the uncertainties of the constitutive equations. However, the existing base of data upon which results can be referred provides a useful guide on meaningful choices of the constitutive equations.

After the above calculations have been performed, the model should be applied to a number of different conditions. These include forward bias computations for the situations done in reverse bias. Experimental data are available for comparison. Then a number of different geometric variations should be explored. These could include systematic variation of the n region length of a single diode to simulate a curved junction, variation of the doping density of the n region at local sites adjacent to the p⁺ region, variation of the n region length with

and without spikes on the junctions (including n-region lengths small enough so that punchthrough occurs), and variation of the spike height.

With the information provided by the above, perspectives should be obtained that will be useful to semiconductor device designers concerned with electrical overstress effects in a wide range of device types.

XIII. IMPLICATIONS

A. Screening Tests

1. Maverick Devices

One goal of the present study is to determine whether any of the geometric parameters explored could give rise to failure thresholds an order of magnitude lower than might be anticipated. Devices with an unexpectedly low threshold are generally referred to as "mavericks." Only one situation was found which led to maverick behavior. If the n-region length is decreased to the point where device fabrication fluctuations cause punchthrough to occur under the high electrical stress encountered in reverse-bias second breakdown, the failure correspondingly shortened. Diffusion spikes on either the p^+n or the n^+n junction on a junction contour which would normally be free of punchthrough could then produce mavericks. The significant feature of the spikes, however, is not their sharpness, but rather the n-region length at the spike location. Thus smooth contours of the p^+n and n^+n junctions with n-region length suitable for punchthrough will yield mavericks. If these contours also contain spikes, the thresholds will be still lower. As the dimensions of devices become ever smaller, slight errors in positioning of the fabrication masks can lead to the conditions that cause mavericks.

2. Screening Methodology

A second goal is to suggest a screening technique which will identify diodes that can meet some preset standard for the threshold of destructive second breakdown. The technique should not damage devices that pass the screening test. The present study provides some perspectives. Two damage modes have been distinguished. About 98% of the devices have been damaged through second breakdown, i.e., through the formation of a melt filament that bridges the n region of the diode. More important for the purposes of screening tests is the degradation of the reverse saturation current level and the more gradual transition to low level avalanche conduction subsequent to damage. Thus a screening test should involve taking an initial low level I-V curve, then a single high level stress at the predetermined level (measuring both voltage and current waveforms so that an energy threshold criterion can be employed), and finally a diagnostic low level I-V curve to ascertain whether the reverse current level has increased appreciably. A constant impedance generator provides a greater amount of damage if damage does occur during the test pulse, so the decision on the presence of damage is unambiguous. The damage of a solidified melt filament formed close to its threshold is electrically equivalent to placing a resistive short circuit of several thousand ohms across the p^+n junction. In about 2% of the diodes tested, damage to the electrodes was observed microscopically before the threshold of second breakdown. The devices were not normally affected in their terminal characteristics by the limited metallization damage. Metallization damage only occurred in diodes with the longest n-region lengths (100 μm , or longer) and the

level of the excitation pulses when damage occurred was comparable to that of the second breakdown threshold.

A decision must be made concerning the amplitude of the test pulse, its duration, and on the circuit environment during the test. In chapter V the application of a single 10 μ s pulse from a constant impedance generator having an energy amplitude chosen to be two standard deviations below the mean failure threshold of standard reference diodes would usually produce second breakdown to about 2% of the standard reference diodes and to virtually all of the diodes with p^+n or n^+n spikes. The high resistivity diodes displayed so much scatter in their energy threshold data that a criterion different from the above might have to be employed.

To use the above approach it is necessary to determine the mean failure threshold and standard deviation for each type of device. The pulse characteristics for the test should be chosen, if possible, to be similar in duration to those expected when the device is in its use environment.

B. Design of Devices for Greater Resistance to Second Breakdown

The results in Chapter V indicate that almost any deviation from a uniform p^+n or n^+n junction results in a nonuniform current distribution during high amplitude pulse testing, and that failure thresholds may be lowered as a result of the nonuniformities. Maverick devices can occur if the n -region length is so small that junction irregularities produce punchthrough.

It may be easier in some cases to achieve a given resistance to second breakdown by adjusting doping level than by altering device geometry. If a device is required to sustain a high reverse voltage, then a low n-region doping level is needed. On the other hand, if the device must maintain a high current density (either in forward or reverse avalanche conduction), then a high n-region doping level is needed. In the intermediate situations, there will be a tradeoff between voltage and current sustaining capabilities, and device geometry. For a specified geometry and a fixed length for the exciting pulses, as the n-region doping level is increased (resistivity decreased), the energy threshold for second breakdown increases, the current density threshold increases, and the voltage threshold decreases. The data in Chapter V indicate the relative importance of these quantities.

REFERENCES

1. C. G. Thornton and C. D. Simmons, "A New High Current Mode of Transistor Operation," IEEE Trans. Electron Devices ED-5, 6-10 (1958).
2. H. A. Schafft and J. C. French, "Second Breakdown and Current Distributions in Transistors," Solid-State Electronics 9, 681-688 (1966).
3. B. Reich and E. B. Hakim, "Secondary Breakdown Thermal Characterization and Improvement of Semiconductor Devices," IEEE Trans. Electron Devices ED-13, 734-737 (1966).
4. D. J. Dumin, "Emission of Visible Radiation from Extended Plasma in Silicon Diodes during Second Breakdown," IEEE Trans. Electron Devices ED-16, 479-485 (1969).
5. R. A. Sunshine, Avalanching and Second Breakdown in Silicon-on-Sapphire Diodes, Technical Report PRRL-70TR-245, RCA Laboratories, Princeton, NJ (1970).
6. H. A. Schafft and J. C. French, "Second Breakdown in Transistors," IEEE Trans. Electron Devices ED-9, 129-136 (1962).
7. H. A. Schafft and J. C. French, "Breakdown Characteristics of Semiconductor Materials," Electro-Technology 75, 77-82 (1965).
8. H. A. Schafft and J. C. French, "A Survey of Second Breakdown," IEEE Trans. Electron Devices ED-13, 613-618 (1966).
9. H. A. Schafft and J. C. French, "Second Breakdown --A Comprehensive Review," Proc. IEEE 55, 1272-1288 (1967).
10. P. L. Hower and V. G. K. Reddi, "Avalanche Injection and Second Breakdown in Transistors," IEEE Trans. Electron Devices ED-17, 320-335 (1970).
11. M. W. Muller and Henry Guckel, "Negative Resistance and Filamentary Currents in Avalanching Silicon p^+-i-n^+ Junctions," IEEE Trans. Electron Devices ED-15, 560-568 (1968).
12. P. P. Budenstein, A Survey of Second Breakdown Phenomena, Mechanisms, and Damage in Semiconductor Junction Devices, Report No. RG-TR-70-19, U.S. Army Missile Command, Redstone Arsenal, AL (1970).

13. D. K. Ferry and A. A. Dougal, "Input Power Induced Thermal Effects Related to Transition Time Between Avalanche and Second Breakdown in p-n Silicon Junctions," IEEE Trans. Electron Devices ED-13, 627-629 (1966).
14. H. Melchior and M. J. O. Strutt, "Secondary Breakdown in Transistors," Proc. IEEE 52, 439-440 (1966).
15. A. C. English, "Physical Investigation of the Mesoplasma in Silicon," IEEE Trans. Electron Devices ED-13, 663-667 (1966).
16. J. D. Holder and V. W. Ruwe, Statistical Component Damage Study, Report No. RG-TR-71-1, U.S. Army Missile Command, Redstone Arsenal, AL (1970).
17. R. A. Sunshine and M. A. Lampert, "Stroboscopic Investigation of Thermal Switching in an Avalanche Diode," Appl. Phys. Lett. 19, 468-470 (1971).
18. P. P. Budenstein, D. H. Pontius, and W. B. Smith, Second Breakdown and Damage in Semiconductor Junction Devices, Technical Report No. RG-TR-72-15, U.S. Army Missile Command, Redstone Arsenal, AL (1972).
19. D. H. Pontius, W. B. Smith, and P. P. Budenstein, "Filamentation in Silicon-on-Sapphire Homogeneous Thin Films," J. Appl. Phys. 44, 331-340 (1973).
20. P. P. Budenstein, D. H. Pontius, and W. B. Smith, "Second Breakdown and Damage in Junction Devices," IEEE Trans. Electron Devices ED-20, 731-744 (1973).
21. D. H. Pontius, W. B. Smith, A. Baruah, and P. P. Budenstein, Second Breakdown in the Presence of Intense Ionizing Radiation, Technical Report No. RG-75-24, U.S. Army Missile Command, Redstone Arsenal, AL (1974). 22. D. H. Pontius, P. P. Budenstein, and W. B. Smith, "Effects of Ionizing Radiation on Second Breakdown," Solid-State Electron. 16, 1073-1077 (1973).
23. S. R. Ovshinsky, "Reversible Electrical Switching Phenomena in Disordered Structures," Phys. Rev. Lett. 21, 1450-1453 (1968).
24. Allen M. Barnett, "Current Filament Formation," Semiconductors and Semimetals, Injection Phenomena, Vol. 6, Edited by R. K. Willardson and A. C. Beer, Academic Press, NY, pp. 141-201 (1970).
25. B. K. Ridley, "Specific Negative Resistance in Solids," Proc. Phys. Soc. (London) 82, 954-956.
26. E. D. Fabricius, The Mechanism of Second Breakdown in Transistors, (D. Eng. Sc., Newark College of Engineering, 1968).

27. T. Asakawa and N. Tsubouchi, "Second Breakdown in MOS Transistors," IEEE Trans. Electron Devices ED-13, 811-812 (1966).
28. N. H. Fletcher, "Some Aspects of the Design of Power Transistors," Proc. IEEE 43, 551-559 (1955).
29. R. J. Nienhuis, "Second Breakdown in the Forward and Reverse Base Current Region," IEEE Trans. Electron Devices ED-13, 655-662 (1966).
30. R. L. Pritchard, "Thermal Effects in Transistors," Electrical Characteristics of Transistors, McGraw-Hill Book Company, NY, pp. 576-649.
31. W. W. Gartner, "Temperature Dependence of Junction Transistor Parameters," Proc. IEEE 45, 662-680 (1957).
32. A. W. Matz, "Thermal Turnover in Germanium p-n Junctions," Inst. of Electrical Engineers, Paper No. 2431R, Vol. 104B, 555-564 (1957).
33. D. J. Fleming, "Thermal Breakdown Delay Time in Silicon p-n Junctions," IEEE Trans. Electron Devices ED-19, 94-97 (1971).
34. Takashi Agatsuma, "A Characterization Technique for Second Breakdown in Ge Alloyed Junction Transistors," IEEE Trans. Electron Devices ED-13, 748-753 (1966).
35. K. L. Chiang and P. O. Lauritzen, "Thermal Instability in Very Small p-n Junctions," IEEE Trans. Electron Devices ED-17, 782-787 (1970).
36. B. Reich and E. B. Hakim, "Hot Spot Thermal Resistance in Transistors," IEEE Trans. Electron Devices ED-16, 166-169 (1969).
37. B. Reich and E. B. Hakim, "Effect of Collector Design on Hot Spot Formation and Second Breakdown in Transistors," IEEE Trans. Electron Devices ED-16, 224-225 (1969).
38. C. R. Crowell and S. M. Sze, "Temperature Dependence of Avalanche Multiplication in Semiconductors," Appl. Phys. Lett. 9, 242-244 (1966).
39. W. M. Portnoy and F. R. Gamble, "Fine Structure and Electromagnetic Radiation in Second Breakdown," IEEE Trans. Electron Devices ED-11, 470-477 (1964).
40. D. M. Taxca, J. C. Peden, and J. Miletta, "Non-Destructive Screening for Thermal Second Breakdown," IEEE Trans. Nucl. Sci. NS-19, 57-67 (1972).

41. W. D. Brown, "Semiconductor Device Degradation by High Amplitude Current Pulses," IEEE Trans. Nucl. Sci. NS-19, 68-75 (1972).
42. D. C. Wunsch and R. R. Bell, "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Voltages," IEEE Trans. Nucl. Sci. NS-15, 244-259 (1968).
43. L. G. Green, SOS Electrical Overstress Investigations, Final Report, Contract No. DNA001-77-C-0145, Rockwell International Corp., Electronics Research Center, Miraloma Ave., Anaheim, CA (1978).
44. R. K. Pancholy and T. J. Oki, "C-MOS/SOS Gate-Protection Networks," IEEE Trans. Electron Devices ED-25, 917-925 (1978).
45. W. R. Runyan, Silicon Semiconductor Technology, McGraw Hill Book Company, NY (1965).
46. B. L. Buchanan, D. A. Neamen, and W. M. Shedd, "SOS Device Radiation Effects and Hardening," IEEE Trans. Electron Devices ED-25, 959-970 (1978).
47. S. N. Lee, R. A. Kjar, and G. Kinoshita, "Island-Edge Effects in C-MOS/SOS Transistors," IEEE Trans. Electron Devices ED-25, 971-978 (1978).
48. A. B. Glaser and G. E. Subak-Sharpe, Integrated Circuit Engineering, Addison-Wesley Publishing Co., Reading, MA (1977).
49. Diode configurations were jointly determined by D. C. Wunsch and D. Alexander of the BDM Corp., H. Philips and L. Green of Rockwell International, D. Mathews of the U.S. Army Missile Command, and P. P. Budenstein of Auburn University.
50. H. A. Weakliem and D. Redfield, "Temperature Dependence of the Optical Properties of Silicon," J. Appl. Phys. 50, 1491-1493 (1979).
51. W. Shockley, "The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors," Bell Syst. Tech. J. 28, 435-489 (1949).
52. J. M. Early, "Design Theory of Junction Transistors," Bell Syst. Tech. J. 32 1271-1312 (1953).
53. R. D. Middlebrook, An Introduction to Junction Transistor Theory, John Wiley and Sons, N. Y., (1957).
54. H. K. Gummel, "A Self-Consistent Iterative Scheme for One-Dimensional Steady-State Transistor Calculations," IEEE Trans. Electron Devices ED-11, 455-465 (1964).

55. A. De Mari, "An Accurate Numerical Steady-State One-Dimensional Solution of the P-N Junction," *Solid-State Electron.* 11, 33-58 (1968).
56. A. De Mari, "An Accurate Numerical One-Dimensional Solution of the P-N Junction Under Arbitrary Transient Conditions," *Solid-State Electron.* 11, 1021-1053 (1968).
57. D. L. Scharfetter and H. K. Gummel, "Large-Signal Analysis of a Silicon Read Diode Oscillator," *IEEE Trans. Electron Devices* ED-16, 64-77 (1969).
58. V. Arandjelovic, "Accurate Numerical Steady-State Solutions for a Diffused One-Dimensional Junction Diode," *Solid-State Electron.* 13, 865-871 (1970).
59. T. I. Seidman and S. C. Choo, "Iterative Scheme for Computer Simulation of Semiconductor Devices," *Solid-State Electron.* 15, 1229-1235 (1972).
60. O. G. Petersen, R. A. Rikoski and W. W. Cowles, "Numerical Method for the Solution of the Transient Behavior of Bipolar Semiconductor Devices," *Solid-State Electron.* 16, 239-251 (1973).
61. G. D. Hachtel, R. C. Joy and J. W. Cooley, "A New Efficient One-Dimensional Analysis Program for Junction Device Modeling," *Proc. IEEE* 60, 86-98 (1972).
62. J. W. Slotboom, "Iterative Scheme for 1-and 2-Dimensional D.C. Transistor Simulation," *Electron. Lett.* 5, 677-678 (1969).
63. D. Vandorpe and N. H. Xuong, "Mathematical 2-Dimensional Model of Semiconductor Devices," *Electron. Lett.* 7, 47-50 (1971).
64. M. Reiser, "Difference Methods for the Solution of the Time Dependent Semiconductor Flow Equations," *Electron. Lett.* 7, 353-355 (1971).
65. M. Reiser, Computing Methods in Semiconductor Problems, Part 1, Edited by G. Goos and J. Hartmanis, Springer-Verlag, NY (1973).
66. C. M. Lee, R. J. Lomax and G. I. Hadad, "Semiconductor Device Simulation," *IEEE Trans. Microwave Theory Tech.* MTT-22, 160-177 (1974).
67. S. P. Gaur and D. H. Navon, "Two-Dimensional Carrier Flow in a Transistor Structure Under Nonisothermal Conditions," *IEEE Trans. Electron Devices* ED-23, 50-57 (1976).
68. Conf. Modelling Semiconductor Devices (1977), (Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland) (abstract only -25.60B -23908).
69. J. Tauc and A. Abraham, "Thermal Breakdown in Silicon P-N Junctions," *Phys. Rev.* 108, 936-937 (1957).

70. I. Melngailis and A. G. Milnes, "Filamentary Impact Ionization in Compensated Germanium at 4.2°K," J. Appl. Phys. 33, 995-1000 (1962).
71. M. W. Muller, "Current Filaments in Avalanching PIN Diodes," Appl. Phys. Lett. 12, 218-219 (1968).
72. H. C. Bowers, "Space-Charge-Induced Negative Resistance in Avalanche Diodes," IEEE Trans. Electron Devices ED-15, 343-350 (1968).
73. A. M. Barnett and A. G. Milnes, "Filamentary Injection in Semi-Insulating Silicon," J. Appl. Phys. 37, 4215-4223 (1966).
74. H. B. Wilson, J. L. Hill and D. Mathews, Feasibility of Using Finite Elements in Analysis of Second Breakdown in Semiconductor Devices, Technical Report RG-73-14, U.S. Army Missile Command, Redstone Arsenal, AL (1973).
75. H. M. Olson, "Thermal Runaway of IMPATT Diodes," IEEE Trans. Electron Devices ED-22, 165-168 (1975).
76. H. M. Olson, "DC Thermal Model of Semiconductor Device Produces Current filaments as Stable Current Distributions," IEEE Trans. Electron Devices ED-24, 1177-1184 (1977).
77. Thermal Conductivity of Metallic Elements and Alloys, The TPRC Data Series 1, Edited by Y. S. Touloukian, R. W. Powell, C. Y. Ho and P. G. Klemens, IFI/PLENUM, NY p. 339 (1970).
78. Ceramics, Handbook of Thermophysical Properties of Solid Materials III, Edited by A. Goldsmith, T. E. Waterman and H. J. Hirschhorn, The Macmillan Company, NY p. 37 (1961).
79. W. D. Raburn and W. H. Causey, Determination of Semiconductor - Junction Vulnerability to Second Breakdown, Technical Report 200-93, U.S. Army Missile Command, Redstone Arsenal, AL (1975).
80. R. A. Sunshine, Avalanching and Second Breakdown in Silicon-on-Sapphire Diodes, Ph.D. Dissertation, Princeton University (1970).
81. H. S. Carslaw and J. C. Jaeger, Conduction of Heat in Solids, Clarendon Press, Oxford, p. 50 (1959).
82. Thermal Diffusivity, The TPRC Data Series 10, Edited by Y. S. Touloukian, R. W. Powell, C. Y. Ho and M. C. Nicolaou, IFI/PLENUM, NY, p. 385 (1973).
83. H. S. Carslaw and J. C. Jaeger, Conduction of Heat in Solids, Clarendon Press, Oxford, p. 61 (1959).

84. S. M. Sze, Physics of Semiconductor Devices, John Wiley and Sons, NY, p. 110 (1969).
85. A. L. Ward, "Calculations of Second Breakdown," IEEE Trans. Nucl. Sci. NS-24, 2357-2360 (1977).
86. G. W. Neudeck, "Reverse-Biased $p^+-n^- - n^+$ Junction at Extreme Currents," Electron. Lett. 11, 397-398 (1975).
87. J. F. Gibbons, "Introduction to Papers on Carrier Drift Velocities in Silicon at High Electrical Field Strengths," IEEE Trans. Electron Devices ED-14, 37 (1967).
88. A. Baruah, A Computer Model for Current Filamentation in Second Breakdown of Silicon-on-Sapphire Diodes, Dissertation, Auburn University, 1979.
89. F.-T. Liou, Role of Diffusion Spikes and Specimen Geometry on Second Breakdown in SOS Diodes, M.S. Thesis, Auburn University, 1979.
90. G. A. Baraff, "Ionization Rates for Hot Electrons in Semiconductors," Phys. Rev. 128, 2507 (1962).

Appendix A. Junction JVT Characteristics Obtained by Baruah

All of the following solutions assume reverse bias conditions. No solutions could be obtained when (1) doping density was below 10^{22} atoms/m³, (2) temperature was above 750 K, or (3) the current density was above 10^8 A/m². The reverse saturation current is due to thermally generated minority carriers from either side of the junction, i.e.,

$$J_{\text{sat}} = J_{\text{po}} + J_{\text{nw}}$$

Until the temperature is hundreds of degrees above room temperature, J_{po} is large compared to J_{nw} because the p^+ region is far more strongly doped than the n region. If the total current density J is small and the temperature is allowed to increase, there is a temperature at which

$$J = J_{\text{po}} + J_{\text{nw}} \pm J_{\text{po}}$$

The junction voltage drops as this temperature is approached. If the temperature increases enough, the Fermi levels of the n and p^+ regions approach the same positions relative to their conduction and valence band edges and the material behaves in a purely resistive manner. If the temperature is low and the current density J is high, then conduction through the junction depends upon carriers generated by the avalanching (or tunneling) processes. Avalanche generation is the more important mechanism in junctions having a depletion width in excess of $100 \text{ \AA}$, as is the case in the systems considered here. At high current

densities, the avalanche generated carriers appreciably modify the space charge distribution in the junction and the junction voltage is found to fall as J increases. At low doping densities, solutions are possible for lower current densities as the avalanche generated carriers cannot modify the space charge distribution in the junction region to any great extent.

Computed J-V-T junction characteristics obtained using the functions listed in Table 21 are given in Table 22. The aim here was to select a particular combination of ionization coefficients and carrier velocities from the various existing functional forms such that a physically meaningful set of J-V-T curves for the junction could be obtained. The somewhat arbitrary criterion used for this choice was based upon the stability of the solutions. With this criterion, Run No. 1 was selected, and accordingly, all subsequent discussions are based on the J-V-T curves obtained using the functions employed in this run.

J-V-T characteristics were calculated for the following ranges of the indicated parameters.

N region doping density	10^{22} atoms/m ³
Applied current density	10^6 - 10^8 A/m ² in steps of 10 A/m ²
Junction temperature	300-800 K in steps of 100 K

Each solution yielded the electric field configuration, charge density configuration, hole and electron current distribution, and electric potential configuration as well as a point on the J-V-T plot.

TABLE 21

SUMMARY OF SIMULATION RUNS WITH VARIOUS FUNCTIONAL FORMS
OF CARRIER VELOCITY AND IONIZATION COEFFICIENTS

Run Number	Velocity, Reference	Ionization Coefficient, Reference
1.	$v_{n1} = f(T)$ $v_{p1} = f(T)$ (92)	$\alpha_{n1} = f(E, T)$ $\alpha_{p1} = f(E, T)$ (91)
2.	$v_{n1} = f(T)$ $v_{p1} = f(T)$ (92)	$\alpha_{n2} = f(E, T)$ $\alpha_{p2} = f(E, T)$ (38)
3.	$v_{n1} = f(T)$ $v_{p1} = f(T)$ (92)	$\alpha_{n3} = f(E)$ $\alpha_{p3} = f(E, T)$ (86)
4.	$v_{n1} = f(T)$ $v_{p1} = f(T)$ (92)	$\alpha_{n4} = f(E, T)$ $\alpha_{p4} = f(E, T)$ (79)
5.	$v_{n2} = v_{no}$ $v_{p2} = v_{po}$ (87)	$\alpha_{n1} = f(E, T)$ $\alpha_{p1} = f(E, T)$ (91)
6.	$v_{n2} = v_{no}$ $v_{p2} = v_{po}$ (87)	$\alpha_{n4} = f(E, T)$ $\alpha_{p4} = f(E, T)$ (79)

where (in MKS units)

$$v_{n1} = v_{no} \left(\frac{300}{T} \right)^{1/2}; \quad v_{no} = 1.05 \times 10^5$$

$$v_{p1} = v_{po} \left(\frac{300}{T} \right)^{1/2}; \quad v_{po} = 0.75 \times 10^5$$

$$v_{n2} = v_{no}; \quad v_{p2} = v_{po}$$

TABLE 21--Continued

$$\alpha_{n1} = 7.03 \times 10^7 \cdot 1 - 2 \times 10^{-3}(T - 300) \exp \left(\frac{-1.23 \times 10^8}{E} \right)$$

$$\alpha_{p1} = 1.58 \times 10^8 \cdot 1 - 2 \times 10^{-3}(T - 300) \exp \left(\frac{-2.03 \times 10^8}{E} \right)$$

$$\alpha_{n2} = \frac{1}{n} \exp \left((11.5 r^2 - 1.17 r + 3.9 \times 10^{-4}) x^2 + (46 r^2 - 11.9 r + 1.75 \times 10^{-2}) x_n \right)$$

$$\alpha_{p2} = \frac{1}{p} \exp \left((11.5 r^2 - 1.17 r + 3.9 \times 10^{-4}) x^2 + (46 r^2 - 11.9 r + 1.75 \times 10^{-2}) x_p \right)$$

$$n = 7.6 \times 10^{-9} \tanh \frac{E_r}{2kT}$$

$$p = 4.7 \times 10^{-9} \tanh \frac{E_r}{2kT}$$

$$r = \frac{\langle E_r \rangle}{E_i}$$

$$x_n = \frac{E_i}{qE} \frac{1}{n}$$

$$x_p = \frac{E_i}{qE} \frac{1}{p}$$

$$\langle E_r \rangle = E_r \tanh \frac{E_r}{2kT}$$

$$E_i = 3/2 E_g$$

$$E_g = \text{bandgap in Silicon } (1.77 \times 10^{-19} \text{ Joules})$$

$$E_r = \text{energy of Raman optical phonon } (.1 \times 10^{-19} \text{ Joules})$$

$$\alpha_{n3} = 3.8 \times 10^8 \exp \left(\frac{-1.75 \times 10^8}{E} \right)$$

$$\alpha_{p3} = 2.25 \times 10^9 \exp \left(\frac{-3.26 \times 10^8}{E} \right)$$

$$\alpha_{n4} = 2.25 \times 10^9 \cdot 1 - 1 \times 10^{-4}(T - 300) \exp \left(\frac{-3.26 \times 10^8}{E} \right)$$

$$\alpha_{p4} = 3.80 \times 10^8 \cdot 1 - 1 \times 10^{-4}(T - 300) \exp \left(\frac{-1.75 \times 10^8}{E} \right)$$

TABLE 22

RESULTS OF SIMULATION RUNS WITH VARIOUS FUNCTIONAL FORMS
OF CARRIER VELOCITIES AND IONIZATION COEFFICIENTS

Applied Current Density (10^7 A/m ²)	Bulk Temperature (K)	Junction Width (μ m)	Maximum Electric Field (10^7 V/m)	Junction Voltage (volts)
Run No. 1 (for parameters see Table 21)				
0.1	300.0	2.57	3.86	49.6
0.1	400.0	2.68	4.03	53.8
0.1	500.0	2.83	4.25	60.0
0.1	600.0	3.04	4.57	69.3
0.1	700.0	3.28	4.95	81.2
0.1	750.0	3.30	5.01	82.7
0.5	300.0	2.61	3.87	50.1
0.5	400.0	2.73	4.04	54.6
0.5	500.0	2.89	4.27	61.0
0.5	600.0	3.09	4.58	69.9
0.5	700.0	3.27	4.96	80.7
0.5	750.0	3.24	5.05	81.7
1.0	300.0	2.66	3.88	50.8
1.0	400.0	2.79	4.04	55.4
1.0	500.0	2.96	4.27	61.9
1.0	600.0	3.16	4.59	70.9
1.0	700.0	3.27	5.00	80.6
1.0	750.0	3.17	5.10	80.5
5.0	300.0	3.19	3.92	57.0
5.0	400.0	3.47	4.09	63.5
5.0	500.0	3.81	4.35	72.5
5.0	600.0	3.94	4.69	81.1
5.0	700.0	3.32	5.22	81.1
5.0	750.0	2.80	5.50	75.3
10.0	300.0	4.57	3.99	72.1
10.0	400.0	5.66	4.18	87.2
10.0	500.0	7.24	4.42	108.9
10.0	600.0	6.79	4.80	113.6
10.0	700.0	3.63	5.48	85.8
10.0	750.0	2.67	5.99	75.8
Run No. 2 (for parameters see Table 21)				
0.1	300.0	2.32	3.49	40.4
0.1	400.0	2.42	3.64	43.9
0.1	500.0	2.51	3.77	47.2
0.1	600.0	2.59	3.89	50.3
0.1	700.0	2.60	3.93	51.0
0.1	750.0	2.50	3.79	47.5

0.5	300.0	2.36	3.49	40.9
0.5	400.0	2.46	3.63	44.3
0.5	500.0	2.57	3.78	48.2
0.5	600.0	2.64	3.89	50.9
0.5	700.0	2.60	3.94	50.9
0.5	750.0	2.44	3.80	46.3
1.0	300.0	2.41	3.50	41.6
1.0	400.0	2.53	3.65	45.4
1.0	500.0	2.64	3.79	49.0
1.0	600.0	2.71	3.91	51.9
1.0	700.0	2.60	3.96	50.9
1.0	750.0	2.38	3.82	45.4
5.0	300.0	2.94	3.55	47.9
5.0	400.0	3.23	3.70	54.2
5.0	500.0	3.53	3.86	60.9
5.0	600.0	3.52	3.99	63.1
5.0	700.0	2.65	4.05	50.9
5.0	750.0	2.05	3.99	40.3
10.0	300.0	4.37	3.61	64.2
10.0	400.0	5.61	3.77	81.9
10.0	500.0	7.42	3.92	107.2
10.0	600.0	6.72	4.08	103.7
10.0	700.0	2.96	4.19	55.4
10.0	750.0	1.90	4.17	38.2

Run No. 3 (for parameters see Table 21)

0.1	300.0	2.61	3.93	51.2
0.1	400.0	2.62	3.94	51.5
0.1	500.0	2.62	3.94	51.5
0.1	600.0	2.60	3.91	50.7
0.1	700.0	2.51	3.79	47.5
0.1	750.0	2.34	3.56	41.6
0.5	300.0	2.66	3.94	52.0
0.5	400.0	2.67	3.95	52.2
0.5	500.0	2.67	3.94	52.0
0.5	600.0	2.65	3.92	51.4
0.5	700.0	2.50	3.79	47.1
0.5	750.0	2.29	3.57	40.8
1.0	300.0	2.71	3.94	52.6
1.0	400.0	2.73	3.95	52.9
1.0	500.0	2.74	3.94	52.9
1.0	600.0	2.71	3.92	52.1
1.0	700.0	2.50	3.81	47.1
1.0	750.0	2.23	3.59	39.8
5.0	300.0	3.30	4.00	60.5
5.0	400.0	3.46	4.01	62.4
5.0	500.0	3.61	4.01	64.2
5.0	600.0	3.46	4.00	61.6
5.0	700.0	2.54	3.94	47.2
5.0	750.0	1.93	3.77	35.8

10.0	300.0	4.84	4.05	79.1
10.0	400.0	5.86	4.08	90.7
10.0	500.0	7.27	4.09	105.7
10.0	600.0	6.32	4.09	94.4
10.0	700.0	2.80	4.06	50.3
10.0	750.0	1.79	3.97	34.1

Run No. 4 (for parameters see Table 21)

0.1	300.0	2.61	3.87	50.1
0.1	400.0	2.72	4.04	54.5
0.1	500.0	2.87	4.26	60.6
0.1	600.0	3.07	4.57	69.7
0.1	700.0	3.27	4.96	80.7
0.1	750.0	3.27	5.04	82.3
0.5	300.0	2.57	3.87	49.6
0.5	400.0	2.68	4.03	53.9
0.5	500.0	2.83	4.26	60.1
0.5	600.0	3.03	4.56	69.0
0.5	700.0	3.28	4.96	81.2
0.5	750.0	3.31	5.01	83.0
1.0	300.0	2.66	3.88	50.8
1.0	400.0	2.77	4.04	55.0
1.0	500.0	2.92	4.26	61.2
1.0	600.0	3.12	4.59	70.5
1.0	700.0	3.27	4.98	80.7
1.0	750.0	3.22	5.07	81.4
5.0	300.0	3.19	3.93	57.0
5.0	400.0	3.32	4.09	61.7
5.0	500.0	3.50	4.33	68.8
5.0	600.0	3.59	4.66	76.8
5.0	700.0	3.30	5.14	81.3
5.0	750.0	2.98	5.37	78.9
10.0	300.0	4.57	3.99	72.1
10.0	400.0	4.74	4.14	77.7
10.0	500.0	4.97	4.39	86.0
10.0	600.0	4.67	4.74	90.4
10.0	700.0	3.48	5.32	84.4
10.0	750.0	2.91	5.77	81.0

Run No. 5 (for parameters see Table 21)

0.1	300.0	2.57	3.87	49.6
0.1	400.0	2.57	3.87	49.6
0.1	500.0	2.58	3.88	49.9
0.1	600.0	2.56	3.85	49.2
0.1	700.0	2.44	3.69	44.9
0.1	750.0	2.22	3.37	37.3
0.5	300.0	2.61	3.87	50.1
0.5	400.0	2.61	3.87	50.1
0.5	500.0	2.62	3.89	50.5
0.5	600.0	2.59	3.86	49.6
0.5	700.0	2.44	3.67	44.9
0.5	750.0	2.19	3.38	36.3

AD-A086 345

AUBURN UNIV ALA DEPT OF PHYSICS

F/G 9/1

SECOND BREAKDOWN SUSCEPTIBILITY OF SILICON-ON-SAPPHIRE DIODES H--ETC(U)

MAY 80 P P BUDENSTEIN, A BARUAH, E R KNIGHT DAAG29-78-G-0111

ARO-15840.3-A-EL

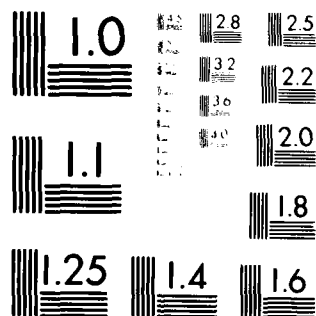
NL

UNCLASSIFIED

6 of 6

2014-2015

END
DATE
FILMED
8-80
DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

1.0	300.0	2.65	3.88	50.8
1.0	400.0	2.66	3.88	50.8
1.0	500.0	2.67	3.89	51.1
1.0	600.0	2.63	3.87	50.1
1.0	700.0	2.43	3.67	44.6
1.0	750.0	2.16	3.40	36.6
5.0	300.0	3.19	3.92	57.0
5.0	400.0	3.20	3.95	57.4
5.0	500.0	3.20	3.95	57.5
5.0	600.0	3.04	3.93	55.0
5.0	700.0	2.45	3.81	44.8
5.0	750.0	1.97	3.55	34.6
10.0	300.0	4.57	3.99	72.1
10.0	400.0	4.58	3.99	72.4
10.0	500.0	4.57	4.00	72.5
10.0	600.0	3.99	3.99	65.7
10.0	700.0	2.58	3.91	46.4
10.0	750.0	1.89	3.74	34.4

Run No. 6 (for parameters see Table 21)

0.1	300.0	2.81	4.22	59.3
0.1	400.0	2.81	4.22	59.3
0.1	500.0	2.81	4.22	59.3
0.1	600.0	2.69	4.04	54.4
0.1	700.0	2.33	3.52	40.9
0.1	750.0	2.00	3.03	30.3
0.5	300.0	2.86	4.21	60.0
0.5	400.0	2.87	4.22	60.4
0.5	500.0	2.87	4.22	60.4
0.5	600.0	2.73	4.04	54.9
0.5	700.0	2.33	3.52	40.9
0.5	750.0	1.98	3.05	30.2
1.0	300.0	2.94	4.22	61.6
1.0	400.0	2.94	4.21	61.6
1.0	500.0	2.94	4.22	61.6
1.0	600.0	2.78	4.03	55.7
1.0	700.0	2.33	3.53	40.9
1.0	750.0	1.95	3.06	29.7
5.0	300.0	3.72	4.17	74.9
5.0	400.0	3.72	4.17	74.9
5.0	500.0	3.72	4.18	75.1
5.0	600.0	3.35	4.03	65.0
5.0	700.0	2.39	3.62	42.3
5.0	750.0	1.79	3.20	28.6
10.0	300.0	5.84	4.11	109.2
10.0	400.0	5.85	4.12	109.6
10.0	500.0	5.82	4.12	108.9
10.0	600.0	4.70	4.01	86.0
10.0	700.0	2.59	3.71	45.8
10.0	750.0	1.74	3.38	29.1

Role of Doping Density

Increased doping of the n region decreases the depletion layer width sharply, as shown in Table 23 and Fig. 163. The spatial distribution of the electric field at a high current density (10^8 A/m^2) and low temperature (300 K) is found to be highly non-linear, as is evident from Fig. 164. All impurities are assumed to be ionized at room temperature. An increase in doping density of the n region will increase the positive space charge concentration in the depletion region, thereby constricting the depletion layer. For the same current density and temperature, the maximum electric field (3.98×10^7 at 10^{22} , 6.32×10^7 at 10^{23} and $9.91 \times 10^7 \text{ V/m}$ at $5 \times 10^{23} \text{ atoms/m}^3$) changes only slightly for large changes in doping density because a small change in field causes a large change in ionization.

TABLE 23

ROLE OF DOPING DENSITY OF THE N REGION ON JUNCTION CHARACTERISTICS
($T = 300 \text{ K}$, $J = 1 \times 10^8 \text{ A/m}^2$)

Doping Density ($10^{22} \text{ atoms/m}^3$)	Junction Width (μm)	Maximum Electric Field (10^7 V/m)	Junction Voltage (volts)
1.	4.50	3.98	72.15
10.	0.432	6.32	13.40
50.	0.132	9.91	6.52

Role of Applied Current Density

In Fig. 164, field contours are shown at various strengths of the applied current density for $N_D = 10^{22} \text{ atoms/m}^3$ and $T = 300 \text{ K}$. At high-

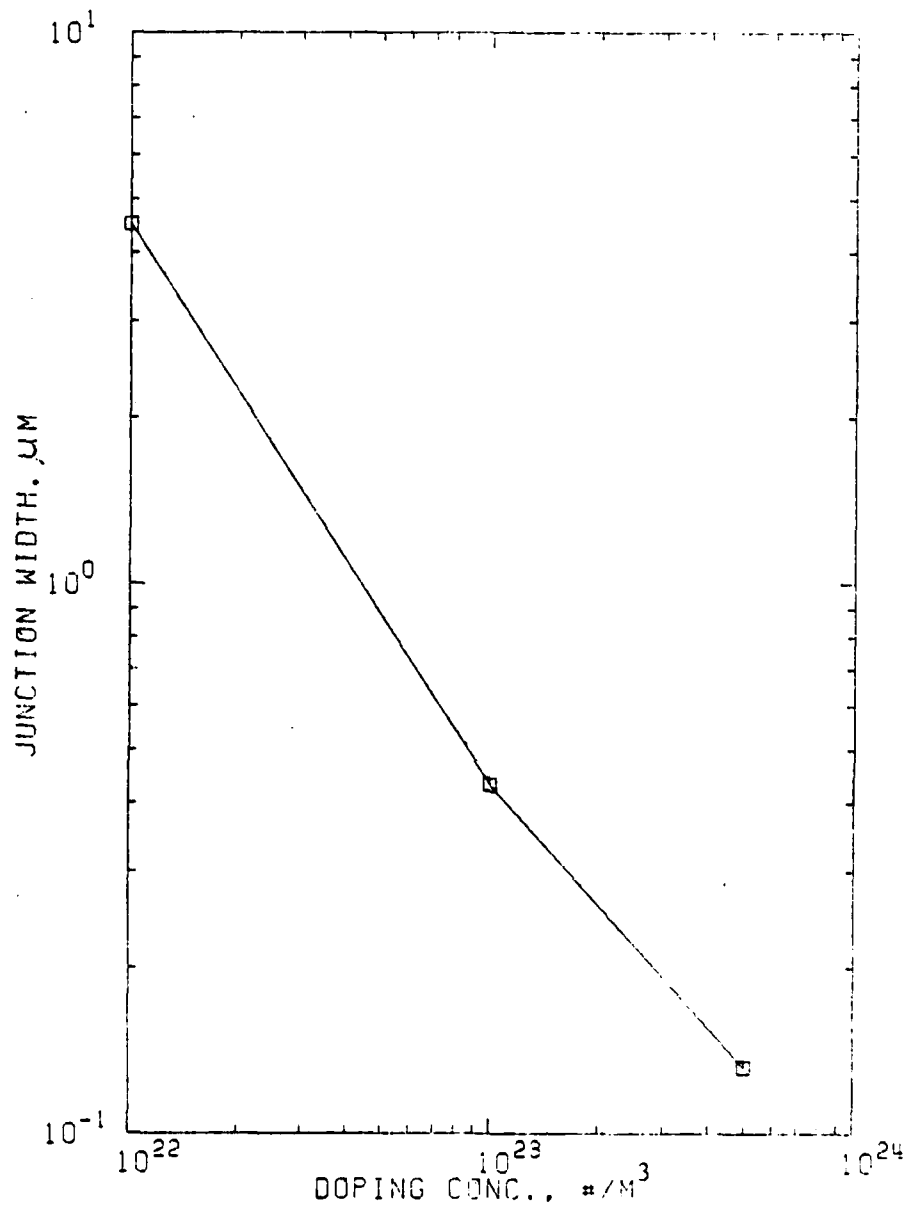


Fig. 163. Junction width as a function of doping density at $T = 300 \text{ K}$ and applied current density $J_{\text{applied}} = 1 \times 10^8 \text{ A/m}^2$.

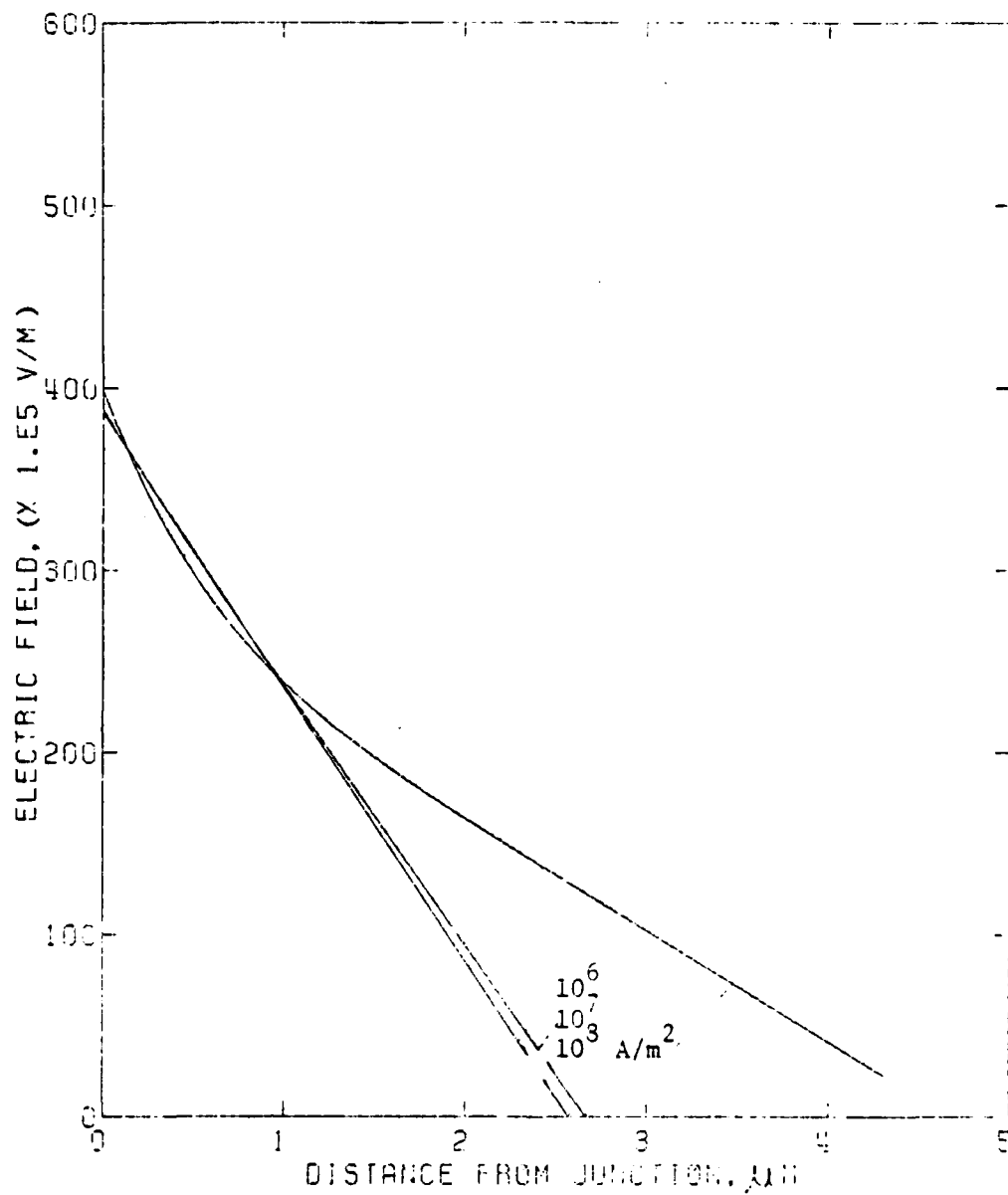


Fig. 164. Electric field as a function of distance from a $p^+ - n$ junction at various applied pulse amplitudes. $T = 300 \text{ K}$ and doping density $N_D = 1 \times 10^{22} \text{ atoms/m}^3$.

er current densities, the number of avalanche generated carriers must increase correspondingly. Then in order to sustain the constant current, the depletion region must widen (Fig. 165) to "expose" the required number of space charges. The electric field profile spreads out further and the area under the field curve, which is the junction voltage, also becomes larger. The J-V curve of Fig. 166 shows this trend at temperatures that are low to moderate. At high temperatures, however, other factors play an important part and cause deviation from this pattern of behavior. This will be discussed in the next section. Fig. 167 shows the spatial distribution of fixed space charges as current density increases. The maximum electric fields do not change much (3.86×10^7 at 10^6 , 3.88×10^7 at 10^7 and 3.98×10^7 V/m at 10^8 A/m²) with increased current densities. This is due to the highly non-linear relationship between field and the ionization coefficients according to which even minor changes in the electric field are capable of affecting major changes in ionization.

Role of Temperature

Experimental evidence strongly suggests that the high conductances of both junction and bulk regions are associated with temperature increases. The principal temperature dependent quantities are the ionization coefficients in the junction region and the reverse saturation current density J_{p0} in the n region outside the junction. Junction voltage tends to rise with temperature due to the former and fall with temperature due to the latter. At low temperatures, the decrease in ionization rate dominates, while at high temperatures the thermal de-

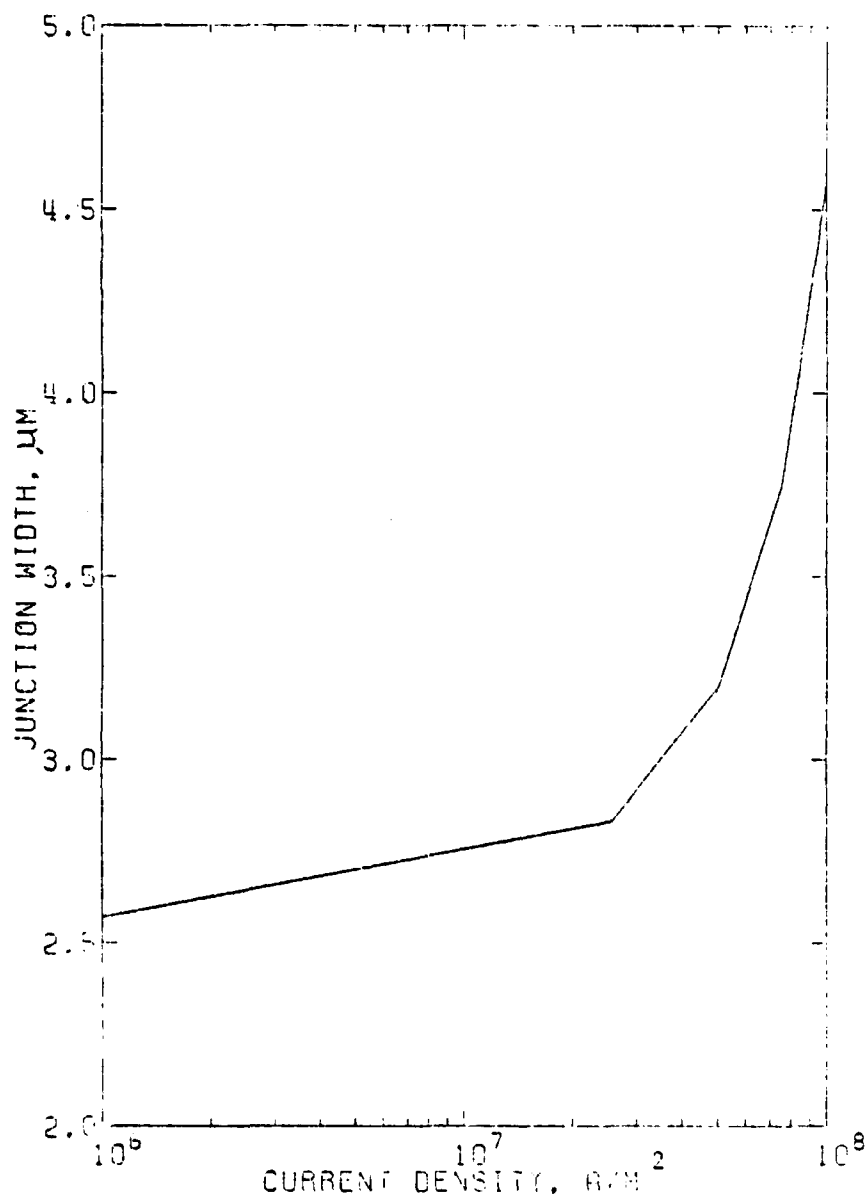


Fig. 165. Junction width as a function of applied current densities.
 $T = 300 \text{ K}$ and $N_D = 1 \times 10^{22} \text{ atoms}/\text{m}^3$.

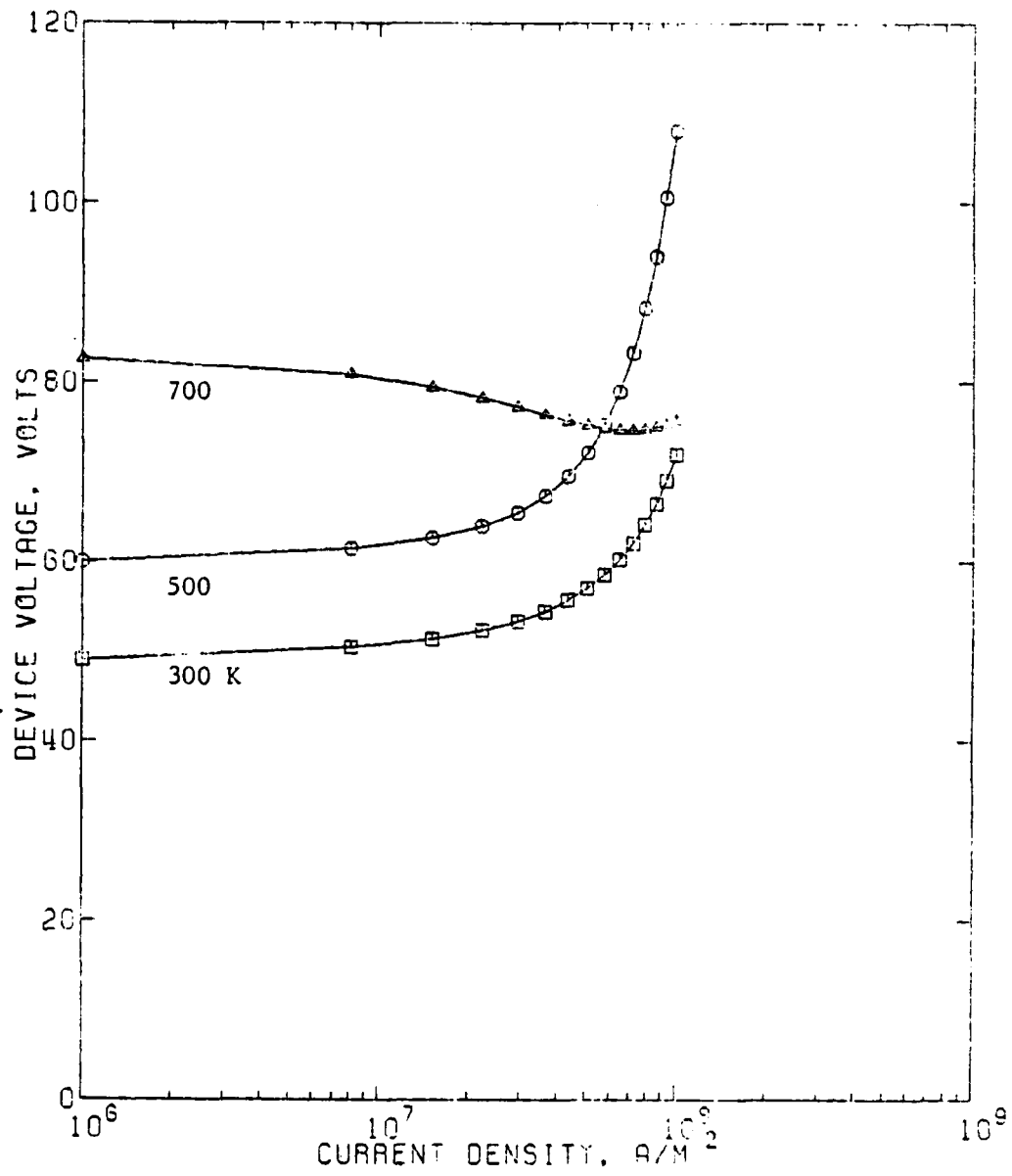


Fig. 166. Junction voltage - current density characteristics at various device temperatures. $N_D = 1 \times 10^{22}$ atoms/m³.

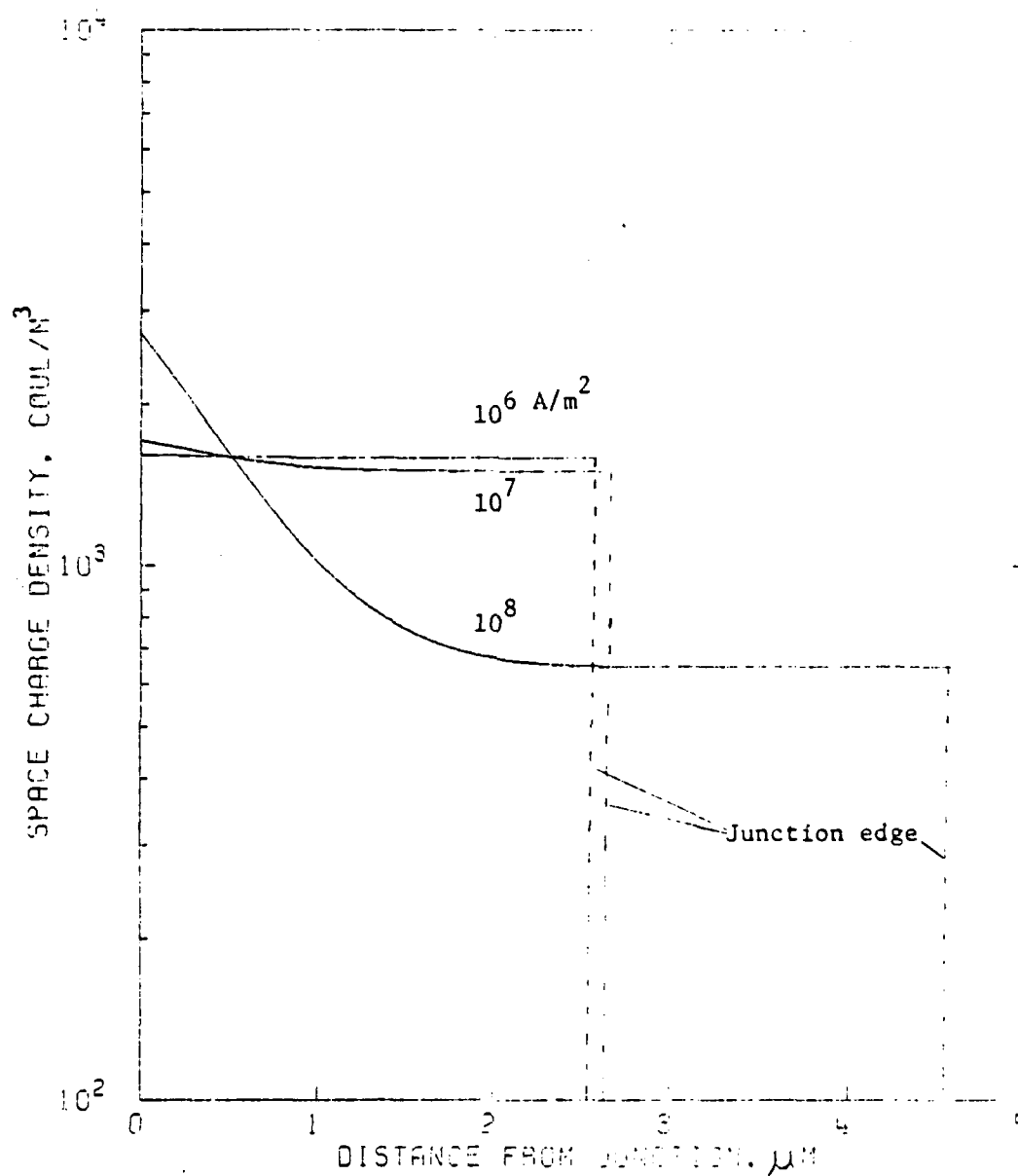


Fig. 167. Alteration of space charge density and of junction width due to an increase in J_{applied} . Note the elongated junction width at 10^8 A/m^2 . $T = 300 \text{ K}$, $N_D = 1 \times 10^{22} \text{ atoms/m}^3$.

pendence of reverse saturation current density takes control. Figure 168 shows the temperature dependence of J_{p0} . At low applied current, this minority carrier current is a diffusion current. But as the second breakdown stage is approached, presence of higher fields in the bulk region tends to make J_{p0} field controlled. Figure 169 shows the effect of temperature on the spatial gradient of space charge density. The combined temperature effects of ionization coefficients and reverse saturation current can be seen in the voltage-temperature plot of Fig. 170. This contrasting relationship also explains the spatial field distribution in Fig. 171 and the change in junction width in Fig. 172.

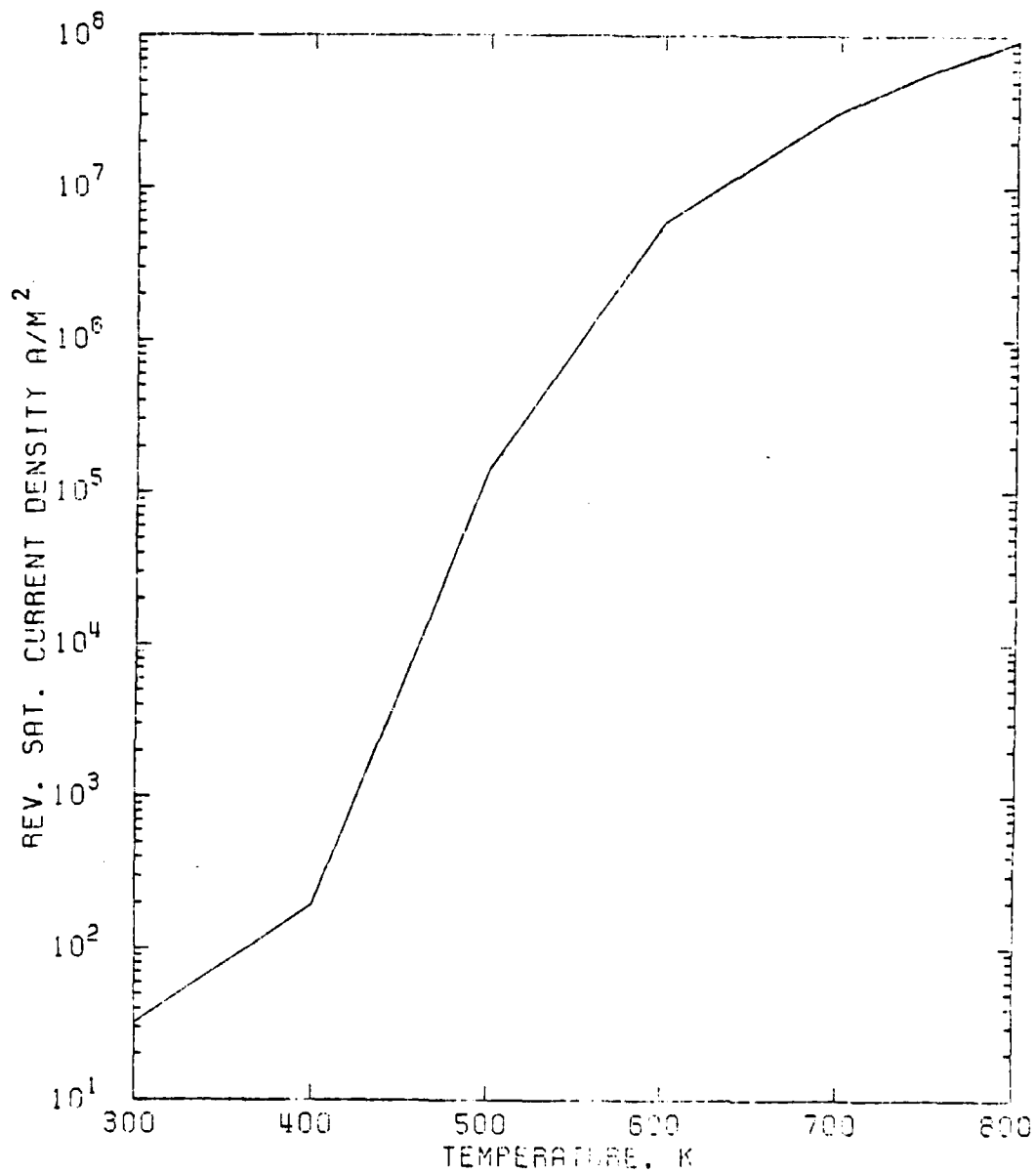


Fig. 168. Graph showing the influence of temperature on thermally generated current carriers and thereby on the reverse saturation current density J_{po} . $N_D = 1 \times 10^{22}$ atoms/ m^3 .

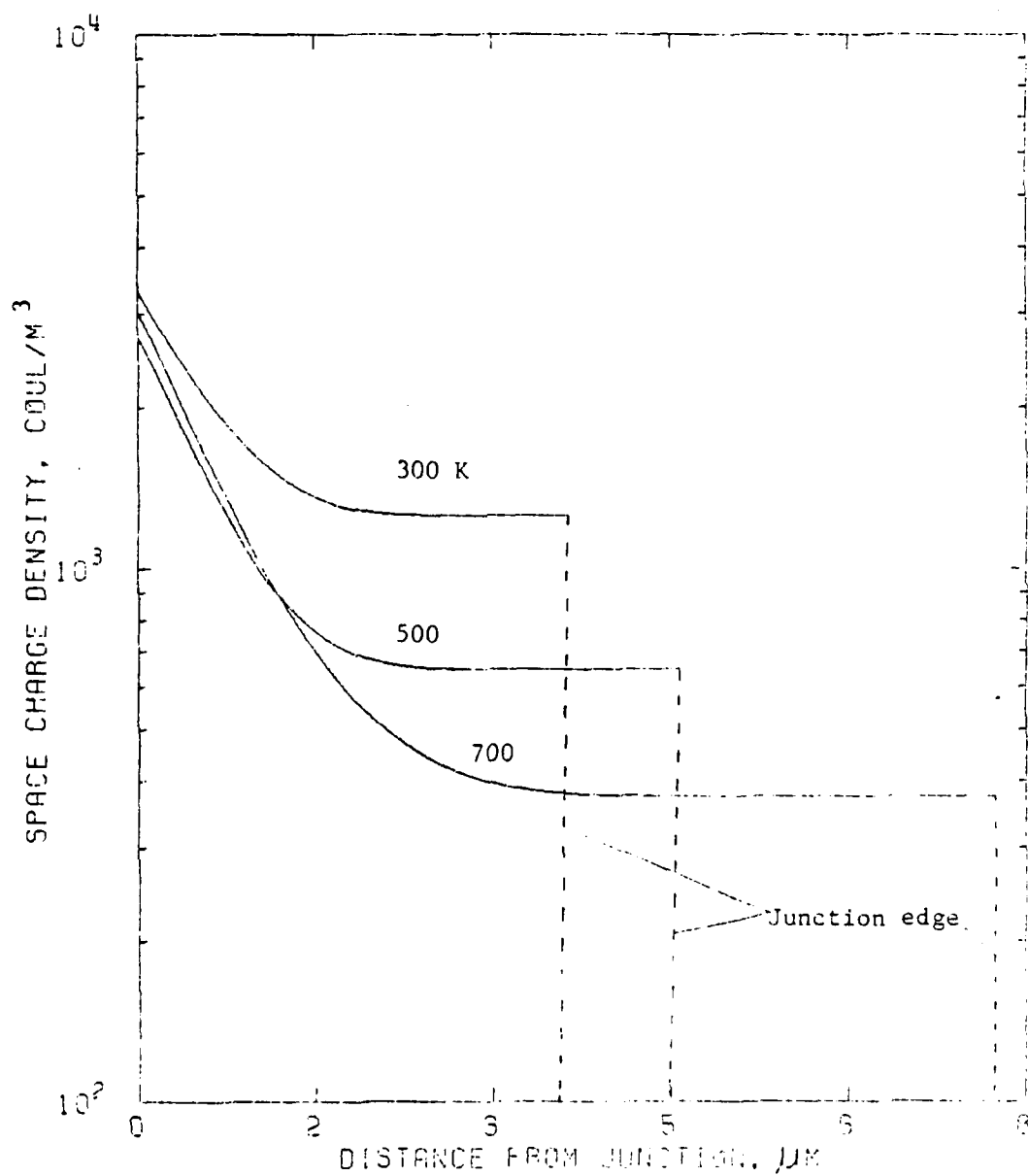


Fig. 169. Effect of temperature on the spatial gradient of the space charge density. $J_{\text{applied}} = 1 \times 10^8$ A/m² and $N_D = 1 \times 10^{22}$ atoms/m³.

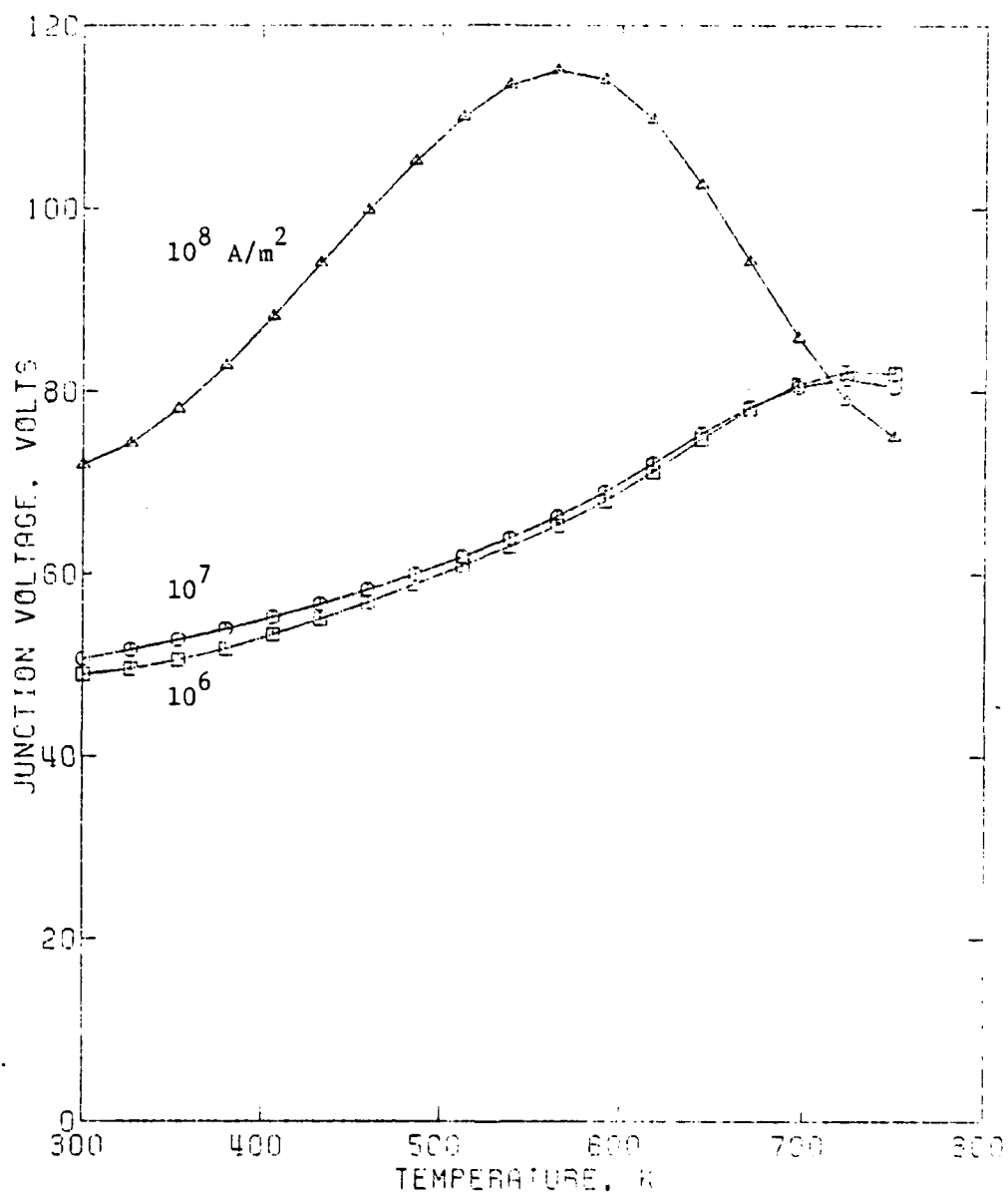


Fig. 170. Junction voltage - temperature characteristics at various applied pulse amplitudes. $N_D = 1 \times 10^{22}$ atoms/m³.

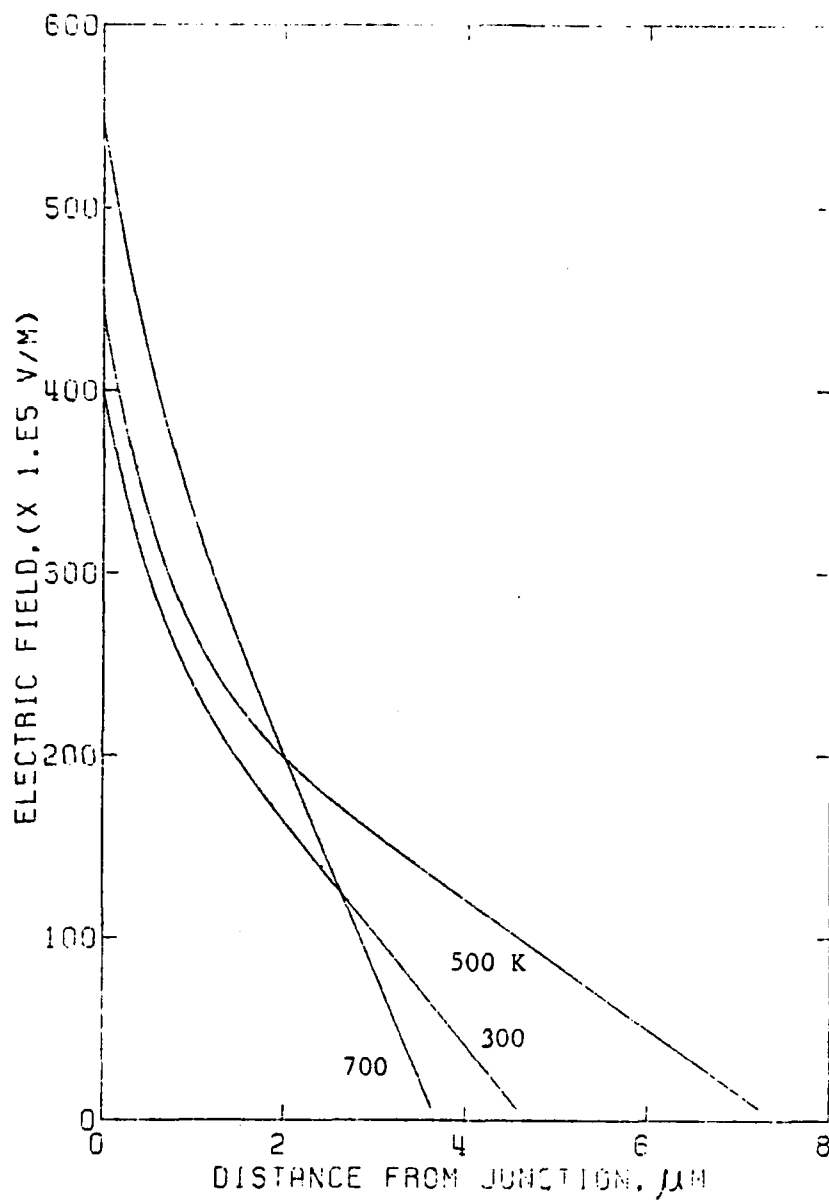


Fig. 171. Electric field profiles as a function of distance from p⁺-n junction at various temperatures. $N_D = 1 \times 10^{22}$ atoms/m³ and applied current density $J_{\text{applied}} = 1 \times 10^8$ A/m².

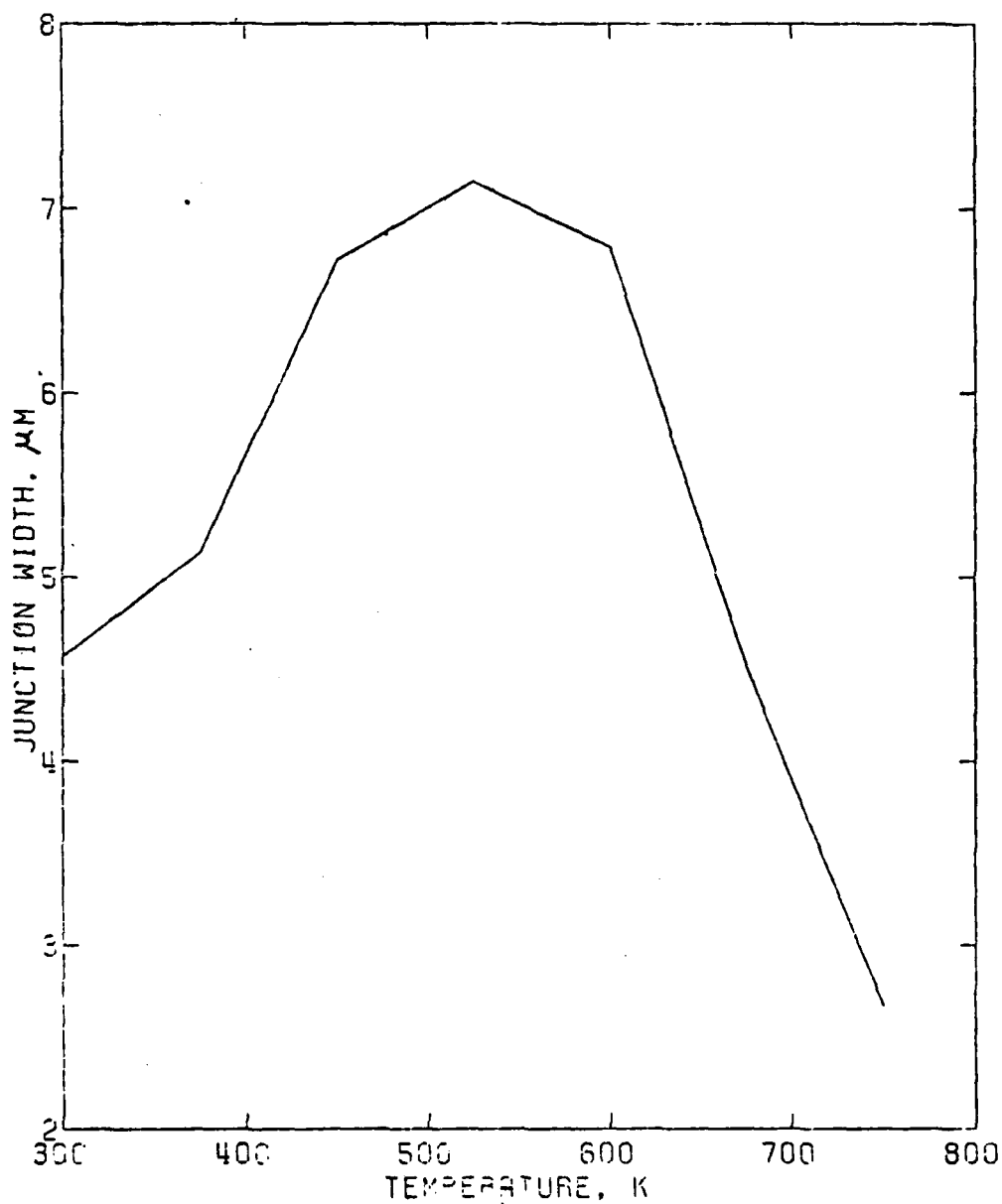


Fig. 172. Effect of junction temperature on the depletion layer width. $J_{\text{applied}} = 1 \times 10^8 \text{ A/m}^2$ and $N_D = 1 \times 10^{22} \text{ atoms/m}^3$. Temperature dependences of both ionization coefficients and thermally generated carriers combine to produce the plot shown here.

APPENDIX B
LISTING OF COMPUTER PROGRAMS

1. JVT program of Chapter IX
2. JVT program of Appendix A
3. Electrothermal model, uniform junction
4. Electrothermal model, n^+n spikes

1. JVT Program of Chapter IX


```

//N22J16H JOB (PS443,22),'BLUDENSTEIN',REGICK=256K,ACTIFY=PS443PE
//*JGBPARM TIME=959,LINES=19K
// EXEC CSMP3
//FT13F001 DD SPACE=(3500,(100,100))
//FT16F001 DD DSN=PS443.PLTJ16H,DISP=(NEW,CATLG),
//      UNIT=DISK,LABEL=RETPD=9,SPACE=(TRK,(5,5),RLSE),
//      DCB=(RECFM=FB,LRECL=176,BLKSIZE=3520)
//CCMPRINT DD SYSCUT=A
//SYSPRINT DD SYSCTL=A
//CSMP3.SYSIN DD *
INITIAL
RENAME TIME=XP,DELT=DELXP,FINTIM=FINXP
* ALL VALUES IN MKS UNITS
* RELAXATION TIME TAKEN AS 1.0E-6 SECONDS FOR HOLES AND ELECTRONS.
* INT. N+N TO NP+ SIDE.
METHOD RKSDP
  PARAM DA=9.99E-4,J=1.0E06
  * PARAM T=(300.0,350.0,400.0,450.0,500.0,520.0,540.0,550.0)
  * PARAM T=(560.,570.,580.,600.,610.,620.,630.,640.,650.,660.,
  * PARAM T=(680.,700.,710.,720.,730.,740.,750.,760.,770.,780.,800.)
  * PARAM T=(800.,825.,850.,875.,900.,925.,950.,975.,1000.)
  PARAM T=(300.0,500.00,700.00)
  * PARAM SIGMAB=2.0E3,ND=1.E20
  * PARAM SIGMAB=2.1E1,NC=1.E21
  PARAM NC=1.E22
  * PARAM SIGMAB=1.1E3,ND=1.E23
  * PARAM SIGMAB=2.8E3,ND=5.E23
  * ISTEP=IFIX(0.0)
  PARAM EPSILN=1.0E-10,...
  SIGMAA=9.52E4,...
  NA=1.0E26,...
  NDD=0.5E26,...
  ER=0.1008E-19,...
  K=1.38E-23,...
  EI=2.164E-19,...
  PLMDAO=4.70E-9,...
  NLMDAO=7.60E-9,...
  Q=1.6E-19
  EB=J/SIGMAB
  PARAM MUCP=480.,AP=6.1E3,BP=2.5E4,AP=4.E16,SP=81.,FP=1.6,...
  KI=1.5E45,EG=1.7696E-19
  NI=SQRT(KI)*(T**1.5)*EXP((-EG)/(2.E0*K*T))
  EK=EB*1.E-2
  NK=NC*1.E-6
  MOBP=(1.+MOBP1+MCBP2+MCBP3)
  MOBP1=NK/((NK/SP)+NP)
  MCBP2=(EK/AP)**2/((EK/AP)+FP)
  MOBP3=(EK/BP)**2
  MUNIEP=MUOP/SQRT(MOBP)
  MUP=(1./T**2.5)*MUNIEP*1.E-4*1.5738E6
  AVER=ER*TANH(ER/(2.C*K*T))
  R=AVER/EI

```

```

F1=11.5*R*R-1.17*R+3.9E-4
F2=46.0*R*R-11.5*R+1.75E-2
F3=-757.0*R*R+75.5*R-1.92
NLMDA=NLMDAC*AVER/ER
PLMDA=PLMDAO*AVER/ER
R1=2.0*NI*NI/ND
R2=1.0+4.0*NI*NI/(ND*ND)
R3=SQRT(R2)

PN=R1/(1.0+R3)
RTDCT=2.528E3/T**C.75
PROCEDURE JPO,JNO,JDO,JFO=FUNCT(Q,EB,MUP,PN,J,RTDCT)
    JFO=Q*EB*MUP*PN
    JDO=Q*RTDCT*PN
    JPC=JDO+JFC
    IF(JPO.GE.J) CALL FINISH
    JNO=J-JPC
ENDPRO
EPC=T**1.6/(0.01856C-1.5720E-4*ALOG10(ND))
ENC=T**1.5/(7.0234E-3-2.8184E-4*ALOG10(ND))
MUOPH=(0.3284-0.01283*ALOG10(ND))*((300.0/T)**2.6)
MUONH=(.8556-C.03594*ALOG10(ND))*((300.0/T)**2.5)
PROCEDURE SIGMAB=FUNCT(T)
    IF(T.EQ.300.0) SIGMAB=189.0
    IF(T.EQ.350.0) SIGMAB=133.0
    IF(T.EQ.400.0) SIGMAB=109.0
    IF(T.EQ.450.0) SIGMAB=77.0
    IF(T.EQ.500.0) SIGMAB=63.10
    IF(T.EQ.520.0) SIGMAB=53.0
    IF(T.EQ.540.0) SIGMAB=47.5
    IF(T.EQ.560.0) SIGMAB=45.0
    IF(T.EQ.570.0) SIGMAB=45.0
    IF(T.EQ.580.0) SIGMAB=45.0
    IF(T.EQ.600.0) SIGMAB=47.32
    IF(T.EQ.610.0) SIGMAB=49.0
    IF(T.EQ.620.0) SIGMAB=52.0
    IF(T.EQ.630.0) SIGMAB=55.0
    IF(T.EQ.640.0) SIGMAB=59.0
    IF(T.EQ.650.0) SIGMAB=63.0
    IF(T.EQ.660.0) SIGMAB=68.0
    IF(T.EQ.670.0) SIGMAB=73.0
    IF(T.EQ.680.0) SIGMAB=79.0
    IF(T.EQ.690.0) SIGMAB=85.0
    IF(T.EQ.700.0) SIGMAB=91.73
    IF(T.EQ.710.0) SIGMAB=111.0
    IF(T.EQ.720.0) SIGMAB=125.0
    IF(T.EQ.730.0) SIGMAB=139.0
    IF(T.EQ.740.0) SIGMAB=154.0
    IF(T.EQ.750.0) SIGMAB=167.88
    IF(T.EQ.760.0) SIGMAB=188.0
    IF(T.EQ.770.0) SIGMAB=208.0
    IF(T.EQ.780.0) SIGMAB=228.0
    IF(T.EQ.790.0) SIGMAB=248.0
    IF(T.EQ.800.0) SIGMAB=273.84
    IF(T.EQ.825.0) SIGMAB=385.0
    IF(T.EQ.850.0) SIGMAB=500.0

```

```

      IF(T.EQ.875.C) SIGMAB=588.0
      IF(T.EQ.900.C) SIGMAB=690.
      IF(T.EQ.925.0) SIGMAB=909.0
      IF(T.EQ.950.C) SIGMAB=1111.0
      IF(T.EQ.975.C) SIGMAB=1250.0
      IF(T.EQ.1000.0) SIGMAB=1429.0
      IF(T.EQ.1025.C) SIGMAB=1667.0
      IF(T.EQ.1050.0) SIGMAB=2000.0
      IF(T.EQ.1075.0) SIGMAB=2174.0
      IF(T.EQ.1100.C) SIGMAB=2500.0
      IF(T.EQ.1125.0) SIGMAB=2941.0
      IF(T.EQ.1150.C) SIGMAB=3125.0
      IF(T.EQ.1175.C) SIGMAB=3571.0

      IF(T.EQ.1200.C) SIGMAB=3846.C
      IF(T.EQ.1225.0) SIGMAB=4348.0
      IF(T.EQ.1250.0) SIGMAB=4651.0
      IF(T.EQ.1275.C) SIGMAB=5000.0
      IF(T.EQ.1300.C) SIGMAB=5263.0

ENDPRO
NOSORT
WRITE(6,80) ND,J,EB,EPC,ENC
80 FORMAT(1X,4HND =,1PE11.3,3X,3HJ =,1PE11.3,3X,4HEB =,1PE11.3,3X,...
      5HEPC =,1PE11.3,3X,5HENC =,1PE11.3)
      WRITE(6,90) JDC,JFO,JPO,T,SIGMAB
      90 FORMAT(1X,5HJDC =,1PE11.3,3X,5HJFO =,1PE11.3,3X,5HJPO =,1PE11.3,
      3X,3HT =,1PE11.3,3X,8HSIGMAB =,1PE11.3)
      WRITE(6,190) MUF,MUCPH,MUONH
      190 FORMAT(1X,5HMUF =,1PE11.3,3X,7HMUCPH =,1PE11.3,3X,7HMUCNF =,...
      1PE11.3)
      PXP=-1.E-11
      SORT
      DYNAMIC
      PRCCEDURE E,JN=FUNCT(XP,EB,JNO)
      IF(XP.LT.1.CE-9) E=EB
      IF(XP.LT.1.OE-9) JN=JNO
ENDPRO
JP=J-JN
EM=ABS(E)
NX=E/(C*EM*NLMDA)
PX=E/(Q*EM*PLMDA)
PROCEDURE ALPHAP,ALPHAN=FUNC(NX,PX,NLMDA,PLMDA,F1,F2,F3)
      IF(XP-1.OE-8) 20,20,30
      20 CONTINUE
      ALPHAP=0
      ALPHAN=0
      GO TO 40
      30 CCNTINUE
      ALPHAP=(1.0/PLMDA)*EXP(F1*PX*PX+F2*PX+F3)
      ALPHAN=(1.0/NLMDA)*EXP(F1*NX*NX+F2*NX+F3)
      40 CCNTINUE

```

```

ENDPRO
DJNDXP=U-G
U=(1.0E6*(NI*NI-N*P))/(P+N+2.0*NI)
G=ALPHAN*JN+ALPHAP*JP
PROCEDURE VP,VN=FUNC(EM,T,EPC,ENC,ND,MUOPH,MUCNH)
  IF(EM.GE.EPC) VP=+0.75E5*SQRT(300.0/T)
  IF(EM.GE.EPC) GO TO 125
  RGCTP=SQRT(0.5*(1.+SQRT(1.+1.444E-8*MLOPH*MLOPH*EM*EM)))
  IF(EM.LT.EPC) VP=MUCPH*EM/RGCTP
125 IF(EM.GE.ENC) VN=-1.05E5*SQRT(300.0/T)
  IF(EM.GE.ENC) GO TO 135
  ROOTN=SQRT(0.5*(1.+SQRT(1.+1.444E-8*MUCNH*MUCNH*EM*EM)))
  IF(EM.LT.ENC) VN=-MUONH*EM/ROOTN
  IF(VN.GT.-2.0E4) VN=-2.0E4
135 CONTINUE
ENDPRO
P=JP/(C*VP)
N=-JN/(Q*VN)
NCSORT
JN=INTGRL(JNG,CJACXF)
IF(JN.GT.J) JN=J
W=J/VP+JN*(1.0/VN-1.0/VP)
CND=C*ND
IF(CND-W). 37,37,38
37 W=0
38 CONTINUE
DEDXP=(Q/EPSILN)*ND+(1./EPSILN)*W
E=INTGRL(EB,DECXF)
V=INTGRL(O,E)
RHO=EPSILN*DECXP
IF(ABS(JP).GE.(0.99*ABS(J))) CALL FINISH
*IF(.NOT.(KEEP.EQ.1.AND.IFIX(XP).EQ.ISTEP)) GO TO 10
*CALL DEBUG(10,0.0)
*ISTEP=ISTEP+IFIX(1.E-7)
10 CONTINUE
IF(KEEP.NE.1) GO TO 100
*WRITE(6,106) XP,PXP
*106 FORMAT(1X,2E14.7)
IF(XP.LT.PXF) GO TO 100
WRITE(16,110) T,XP,E,V,RHO,JP,JN,P,N,NI,ALPHAN,ALPHAP,U,G,VP,VN
110 FORMAT(16E11.4)
PXP=XP+1.0E-07
100 CONTINUE
SORT
TERMINAL
TIMER FINXP=1.0E-5,PRDEL=1.E-07,DELMIN=1.0E-18
PRINT E,V,RHO,JP,JN,P,N,NI,ALPHAN,ALPHAP,U,G,VP,VN
*PLCTTING ROUTINE
OUTPUT E
PAGE LOG,MERGE
END
STOP
//

```

2. JVT Program of Appendix A

```

//N21J14A JGB (FS443,5R),BARUAH,REGION=128K,NCTIFY=PS443AB
/*ROUTE PRINT RMT1
/*JGBPARM TIME=C55,LINES=19K
// EXEC CSMP3
//FT13FC01 DD SPACE=(3500,(100,100))
//COMPRINT DD CUMMY,DISP=(NEW,DELETE)
//SYSPRINT DD CUMMY,CISP=(NEW,DELETE)
//CSMP3.SYSIN DD *
INITIAL
RENAME TIME=XP,CELT=CELXP,FINTIM=FINXP
* ALL VALUES IN MKS UNITS
* INT. N+N TO NP+ SIDE.
METHOD RKSDP
  PARAM DA=9.99E-4,J=1.0EC4,T=(300.,400.,500.,600.,700.,750.,...
    800.,850.,900.)
  * PARAM SIGMAB=2.0E0,ND=1.E20
  * PARAM SIGMAB=2.1E1,ND=1.E21
  * PARAM SIGMAB=1.6E2,ND=1.E22
  * PARAM SIGMAB=1.1E3,ND=1.E23
  * PARAM SIGMAB=2.8E3,ND=5.E23
  * ISTEP=IFIX(0.0)
  * PARAM EPSILN=1.06E-10,...
  SIGMAA=9.52E4,...
  NA=1.0E26,...
  NDD=0.5E26,...
  ER=0.1008E-19,...
  K=1.38E-23,...
  PLMDAC=47.E-10,...
  NLMDAC=76.0E-10,...
  EI=2.164E-15,...
  Q=1.6E-19
  EB=J/SIGMAB
  PARAM MUOP=480.,AP=6.1E3,BP=2.5E4,NP=4.E16,SP=81.,FF=1.6,...
  KI=1.5E45,EG=1.7696E-19
  NI=SQRT(KI)*(T**1.5)*EXP((-EG)/(2.E0*K*T))
  EK=EB*1.E-2
  NK=ND*1.E-6
  MOB P=(1.+MOBP1+MOBP2+MOBP3)
  MCBP1=NK/((NK+SP)+NP)
  MCBP2=(EK/AP)**2/((EK/AF)+FP)
  MOBP3=(EK/BP)**2
  MUNIEP=MUOP/SQRT(MOEP)
  MUP=(1./T**2.5)*MUNIEP*1.E-4*1.5738E6
  PN=(-ND)/2.+SQRT((ND**2/4.)+NI**2)
  JPO=Q*EB*MUP*PN
  NOSORT
  IF(JPO.LE.0.0) JPO=1.0
  SCRT
  JNO=(J-JPC)
  DYNAMIC
  JP=J-JN
  AVER=ER*TANH(ER/(2.E0*K*T))
  NX=EI/(Q*EM*NLMDA)
  PX=EI/(C*EM*PLMDA)
  *REFERENCE: A.L.WARD,IEEE TRANSC. NUC. SC. DEC'76

```

```

BETA=2.E-3
EE=EM*1.E-2
XLPHAP=1.58E6*(1.E0-BETA*(T-300.E0))*EXP(-2.03E6/EE)
XLPHAN=7.03E5*(1.E0-BETA*(T-300.E0))*EXP(-1.23E6/EE)
ALPHAP=XLPHAP*1.E2
ALPHAN=XLPHAN*1.E2
PLMDA=PLMDAC*(AVER/ER)
NLMDA=NLMDAC*(AVER/ER)
R=AVER/EI
DJNDXP=-(ALPHAN*JN)-(ALPHAP*JP)
JN=INTGRL(JNO,DJNDXP)
EM=ABS(E)
ABSRHO=ABS(RHC)
ABSJ=ABS(J)
ABSJP=ABS(JP)
ABSJN=ABS(JN)
N=-JN/(Q*VN)
P=JP/(Q*VP)
VN=-1.05E5*SQRT(300.E0/T)
VP=+.75E5*SQRT(300.E0/T)
V=INTGRL(0.,E)
RHO=EPSILN*DEDXP
E=INTGRL(EB,DEDXP)
DEDXP=(C/EPSILN)*ND+(1./EPSILN)*(J/VP+JN*(1./VN-1./VP))
NOSORT
IF(RHO.LE.0.0.OR.ABS(JP).GE.(.9*ABS(J))) CALL FINISH
*IF(.NOT.(KEEP.EQ.1.AND.IFIX(XP).EQ.1STEP)) GO TO 10
*CALL DEBUG(10,C.C)
*1STEP=1STEP+IFIX(1.E-7)
10 CONTINUE
TERMINAL
TIMER FINXP=9.99E-4,PRODEL=1.E-06,DELMIN=1.0E-18
PRINT E,V,RHO,JP,JN,N,NI,ALPHAN,ALPHAP
END
STOP
//

```

3. Electrothermal Model, Uniform Junction


```

IMPLICIT REAL*8 (A-F,O-Z)
DOUBLE PRECISION I,ITCT,NA,NC,NDD
DIMENSION T(53,11),R(53,11),STPRS(53),I(53),DCSUM(53,11),
$VJ(53),CLCGIC(53),STPV(53),TERM2(53,11),TAP(53,11)
$,STPMS(53,11)

```

```

NSTPS=20
JR=53
JRBY2=(JR+1)/2
KC=11
KCJ=3
KC1=KC-1
KCJP1=KCJ+1
KC2=KC-2
JR1=JR-1
JR2=JR-2

```

C
C

```

ITOT=12.00-3
STPLNJ=4.00-6
CP=930.00
NA=1.0026
NC=1.0022
NDD=5.0025
DNSTY=2.3303
STPWCH=4.00-6
FLMTHK=0.00-6
STPARA=STPWCH*FLMTHK
STPLN1=160.0-6

```

C
C

```

STPLN2=(3.00-5-STPLNJ)/6.
STPVL1=STPLN1*STPARA
STPVLJ=STPLNJ*STPARA
STPVL2=STPLN2*STPARA
STPMS1=DNSTY*STPVL1
STPMSJ=DNSTY*STPVLJ
STPMS2=DNSTY*STPVL2
TS=300.00

```

C INITIALIZE ALL STRIPS TO SUBSTRATE TEMPERATURE 'TS'.

C
C
C

```

TIME=C.00
DO 5 J=1,JR
I(J)=ITCT/JR2
DO 10 K=1,KC
T(J,K)=TS
DCSUM(J,K)=0.00
10 CONTINUE
5 CONTINUE
DO 15 J=2,JR1
RS=C.00

```

```

DO 20 K=2,KC1
  IF(K.LE.2) CALL CALCRS(STPLN1,NA ,T(J,K),R(J,K))
  IF(K.EQ.KCJ) R(J,KCJ)=0.00
  IF(K.GT.KCJ.AND.K.LE.KC2) CALL CALCRS(STPLN2,ND,T(J,K),R(J,K))
  IF(K.GT.KC2) CALL CALCRS(STPLN1,NCD,T(J,K),R(J,K))
  RS=RS+R(J,K)
20 CONTINUE
  DLOGID(J)=DLOGIC(I(J)/STPARA)
  CALL CALCVJ(T(J,KCJ),VJ(J),DLOGID(J),ITER)
  IF(VJ(J).GT..0500) GO TO 14
  CALL CALCRS(STPLNJ,ND,T(J,KCJ),R(J,KCJ))
  VJ(J)=I(J)*R(J,KCJ)
14 STPRS(J)=RS
15 CONTINUE
  VTCT=VJ(12)+(I(12)*STPRS(12))
  WRITE(6,1)VTOT,VJ(12),STPRS(12)
  1  FORMAT(1X,1P3E14.3)
  C  WRITE(6,9)((T(J,K),K=2,12),J=2,JR1)
  C9  FORMAT(1P11E10.3)
  DO 25 J=2,JR1
  DO 30 K=2,KC1
    IF(K.EQ.2) STPMS(J,K)=STPMS1
    IF(K.EQ.KCJ) STPMS(J,K)=STPMSJ
    IF(K.GT.KCJ.AND.K.LE.KC2) STPMS(J,K)=STPMS2
    IF(K.GT.KC2) STPMS(J,K)=STPMS1
30 CONTINUE
25 CONTINUE
  C
  C
  DO 35 ITER=1,NSTPS
  IF(ITER.LE.2) TAU=1.0-9
  IF(ITER.GT.2) TAU=1.0-8
  TIME=TIME+TAU
  WRITE(6,3) TIME, ITER
  3  FORMAT(10X,7H TIME= ,1PE13.4,1X,8H SECCND ,14)
  7  FORMAT(/)
  DO 45 J=2,JR1
  DO 50 K=2,KC1
  VOLT=I(J)*R(J,K)
  IF(K.EQ.2)
    $ CALL DQAP(VOLT,STPLN1,T,J,K,I(J),DQSUM(J,K),STPMS(J,K),
    $ DTAP,TERM2(J,K),ITER)
  IF(K.EQ.KCJ)
    $ CALL DQAP(VJ(J),STPLNJ,T,J,K,I(J),DQSUM(J,K),STPMS(J,K),
    $ DTAP,TERM2(J,K),ITER)
  IF(K.GT.KCJ.AND.K.LE.KC2)
    $ CALL DQAP(VOLT,STPLN2,T,J,K,I(J),DQSUM(J,K),STPMS(J,K),
    $ DTAP,TERM2(J,K),ITER)
  IF(K.GT.KC2)
    $ CALL DQAP(VOLT,STPLN1,T,J,K,I(J),DQSUM(J,K),STPMS(J,K),
    $ DTAP,TERM2(J,K),ITER)
  TAP(J,K)=T(J,K)+DTAP
  C  WRITE(6,606) TAP(J,K),DTAP,K,J
  C606  FORMAT(1X,1P2E10.2,214)

```

```

50  CONTINUE
45  CONTINUE
    DC 55 J=2,JR1
    DO 60 K=2,KC1
    VOLT=I(J)*R(J,K)
    IF(K.EQ.2)
$   CALL DQ(VCLT,STPLN1,TAP,J,K,I(J),DQJK,STPMS(J,K),
$   DCSUM(J,K),TERM2(J,K),ITER)
    IF(K.EQ.KCJ)
$   CALL DQ(VJ(J),STPLNJ,TAP,J,K,I(J),DQJK,STPMS(J,K),
$   DCSUM(J,K),TERM2(J,K),ITER)
    IF(K.GT.KCJ.AND.K.LE.KC2)
$   CALL DQ(VCLT,STPLN2,TAP,J,K,I(J),DQJK,STPMS(J,K),
$   DCSUM(J,K),TERM2(J,K),ITER)
    IF(K.GT.KC2)
$   CALL DQ(VOLT,STPLN1,TAP,J,K,I(J),DQJK,STPMS(J,K),
$   DCSUM(J,K),TERM2(J,K),ITER)
    T(J,K)=T(J,K)+DQJK/(STPMS(J,K)*CP)
    IF(T(J,K).GE.168C.DC) GO TO 36
60  CCNTINUE
55  CCNTINUE
    IF(MOD(ITER,10).NE.0) GO TO 64
    WRITE(6,7)
    WRITE(6,9999)((T(J,K),K=2,8),J=2,25)
9999 FORMAT(1X,1P7E10.3)
    WRITE(6,7)
C   WRITE(6,9)((T(J,K),K=13,23),J=2,JR1)
64  DO 65 J=2,JR1
    RS=0.C
    DO 70 K=2,KC1
    IF(K.EQ.KCJ.AND.VJ(J).GT..05DC) R(J,KCJ)=C.DC
    IF(K.EQ.KCJ.AND.VJ(J).LE..05DC)
$   CALL CALCRS(STPLNJ,ND,T(J,K),R(J,K))
    IF(K.LE.2)
$   CALL CALCRS(STPLN1,NA,T(J,K),R(J,K))
    IF(K.GT.KCJ.AND.K.LE.KC2)
$   CALL CALCRS(STPLN2,NC,T(J,K),R(J,K))
    IF(K.GT.KC2)
$   CALL CALCRS(STPLN1,NDD,T(J,K),R(J,K))
    RS=RS+R(J,K)
C   IF (K.NE.3.OR.K.NE.4) GO TO 70
C   IF (K.EQ.3-CP.K.EQ.4) GO TO 72
C72 WRITE(6,11)T(J,K),R(J,K),J,K
C11 FORMAT(1X,1P2E14.3,4X,2I3)
70  CCNTINUE
    STPRS(J)=RS
65  CONTINUE
    VJBYRS=0.CC
    STPRSI=C.DC
    DO 75 J=2,JR1
    CALL CALCVJ(T(J,KCJ),VJ(J),DLCGID(J),ITER)
    IF(VJ(J).GT..05DC) GO TO 80
    CALL CALCRS(STPLNJ,NC,T(J,KCJ),R(J,KCJ))

```

```

      VJ(J)=I(J)*R(J,KCJ)
80  VJBYRS=VJBYRS+(VJ(J)/STPRS(J))
      STPRSI=STPRSI+(1.00/STPRS(J))
75  CONTINUE
      VTOT=(ITOT+VJBYRS)/STPRSI
      DC 85 ITLCCF=1,10
      CITOT=C.DC
      VJBYRS=0.00
      STPRSI=0.00
      DO 90 J=2,JR1
        I(J)=(VTCT-VJ(J))/STPRS(J)
        IF(I(J).LE.0.00) I(J)=0.00
        IF(I(J).LE.0.00) VJ(J)=VTOT
        IF(I(J).LE.0.00) GO TO 95
        DLOGID(J)=DLOGIC(I(J)/STPARA)
        CALL CALCVJ(T(J,KCJ),VJ(J),DLOGID(J),ITER)
        IF(VJ(J).GT..0500) GO TO 95
        CALL CALCRS(STPLNJ,ND,T(J,KCJ),R(J,KCJ))
        VJ(J)=I(J)*R(J,KCJ)
95  STPV(J)=I(J)*STPRS(J)+VJ(J)
      VJBYRS=VJBYRS+(VJ(J)/STPRS(J))
      STPRSI=STPRSI+(1.00/STPRS(J))
C    WRITE(6,13) I(J),STPRS(J),VJ(J),T(J,4)
C13  FORMAT(1X,1P4E10.3)
      CITCT=CITCT+I(J)
80  CONTINUE
      VTOT=(ITOT+VJBYRS)/STPRSI
17  FORMAT(1P2E10.3)
84  CONTINUE
C    WRITE(6,17) VTOT,CITOT
85  CONTINUE
      IF(MOD(ITER,10).NE.0) GO TO 87
86  WRITE(6,17) VTCT,CITCT
      WRITE(6,19) (STPV(J),J=2,JRBY2)
      WRITE(6,19) (VJ(J),J=2,JRBY2)
      WRITE(6,19) (I(J),J=2,JRBY2)
19  FORMAT(1P13E10.2)
      WRITE(9) TIME,T,R,VJ,I,VTOT,DQSUM,ITER
87  CONTINUE
35  CONTINUE
36  WRITE(9) TIME,T,R,VJ,I,VTOT,DQSUM,ITER
      STOP
      END
C
      SUBROUTINE CALCRS(STPLNG,DCPING,TEMP,RESIST)
      IMPLICIT REAL*8 (A-H,C-Z)
      DOUBLE PRECISION MUOP,NP,MUON,NN,KI,NI,MUNE,MUPE,MUP,MUN
      DOPIN1=DCPING*1.00-6
      STPWDH=4.00-6
      FLMTFK=0.60-6
      STPARA=FLMTFK*STPWDH
      MUOP=480.00
      NF=4.0016

```

```

SP=81.D0
AP=6.1D3
FP=1.6C0
BP=2.5D4
MUCN=1400.CC
NA=3.CD16
SN=35C.DC
AN=3.5D3
FN=8.8D0
BN=7.4D3
C=1.6D-19
EM=1.CD5
EG=1.106DC*1.4D-19
KI=1.5C45
BK=1.38D-23
NI=(KI**0.5D0)*(TEMP**1.5D0)*DEXP(-EG/(2.D0*BK*TEMP))
SQRTM=DSQRT((CCPING/2.D0)**2+NI**2)
MUNE=MUCN*DSQRT(1.D0/(1.D0+DGPIN1/((DGPIN1/SA)+NA)+(EM/AN)**2
$ /((EM/AN)+FN)+(EM/BN)**2))
MUPE=MUCF*DSQRT(1.CD/(1.CD+DGPIN1/((DGPIN1/SP)+NP)+(EM/AP)**2,
$ ((EM/AP)+FP)+(EM/BP)**2))
MUF=MUPE*1.5738C2*(1.D0/TEMP)**2.5
MUN=MUNE*1.5738C2*(1.CD/TEMP)**2.5
RHO=(1.DC/(Q*(MUP*(DOPING/2.D0+SQRTM)+MUN*(-CCPING/2.D0+SQRTM)
RESIST=(R+C*STFLNG)/STPARA
RETURN
END

```

C

C

C BASED ON ITS HEAT TRANSFER TO AND FROM SURROUNDING STRIPS.

```

SUBROUTINE CC(VCLT,STPLNG,TAP,J,K,IJ,DQJK,SMJK,DQSJK,T2JK,ITER)
IMPLICIT REAL*8 (A-H,C-Z)
REAL*4 EPS
DCUBLE PRECISION I,LENGTH,IJ,KSI,KSIC
DIMENSION TAP(53,11)
DIMENSION TS1(17),TS10(17),KSI(17),KS10(17),TSA(17),TSA0(17)
DIMENSION DIFSA(17),DIFSAC(17)
DATA TS10/273.D0,300.DC,350.D0,400.DC,500.DC,600.C0,700.D0,800.D0,
$ 900.D0,1000.C0,
$ 1100.DC,1200.D0,1300.D0,1400.C0,1500.D0,1600.C0,1685.D0/
DATA KSI0/168.D0,148.DC,119.D0,98.9D0,76.2D0,61.9D0,50.8D0,42.2D0,
$ 35.9C0,
$ 31.2D0,27.5DC,25.7DC,24.4D0,23.5D0,22.7D0,22.1C0,22.D0/
DATA TSA0/300.D0,368.D0,403.D0,417.DC,451.DC,504.D0,546.DC,568.D0,
$ 713.DC,871.CC,900.C0,
$ 976.DC,1061.DC,1236.D0,1315.DC,1593.DC,1692.C0/
DATA DIFSA0/.0786D0,.0786D0,.0645D0,.0550D0,.0576D0,.0456DC,
$ .0415D0,.0376D0,
$ .0270D0,.0216DC,.0191D0,.0171D0,.0152DC,.0124D0,.0123D0,.011C0,
$ .012C0/
JR=53
KC=11
TS=300.C0
KCJ=3

```

```

STPLNJ=4.00-C
STPLN2=(3.00-5-STPLNJ)/6.00
STPLN1=16C.D-6
JR1=JR-1
KC1=KC-1
KC2=KC-2
FLMTHK=0.6C-6
STPWCH=4.00-6
IF(ITER.LE.2) TAL=1.D-9
IF(ITER.GT.2) TAU=1.D-8
C=1.000
EPS=.9E0
TEMP=TAP(J,K)
NPNTS=17
TIME=DFLOAT(ITER)*TAL
DO 1 L=1,NPNTS
  TSA(L)=TSAC(L)
  TSI(L)=TSIO(L)
  KSI(L)=KSIO(L)
  DIFSA(L)=DIFSAC(L)*1.D-4
1 CONTINUE
  CALL DACFI(TEMP,TSI,KSI,CONNSI,NPNTS,EPS,IER)
  CALL DACFI(TEMP,TSA,DIFSA,DIFFSA,NPNTS,EPS,IER)
  IF(TAP(J,K).LT.500.DC) CONNSA=58.16DC-(.0795DC*TAP(J,K))
  IF(TAP(J,K).GE.500.DC.AND.TAP(J,K).LE.700.DC)
    $ CONNSA=35.135DC-(.03345DC*TAP(J,K))
  IF(TAP(J,K).GT.700.DC.AND.TAP(J,K).LE.900.DC)
    $ CCNSA=26.38C0-(.020945DC*TAP(J,K))
  IF(TAP(J,K).GT.900.DC) CCNSA=7.3DC
  CP=930.DC
  AT=(FLMTHK*STPLNG*CCNSI)/(2.*STPWCH)
  TERM1=(VOLT*IJ*TAU)/C
C606 FCRMAT(1X,1P3E10.2,2I3)
C WRITE(6,606) IJ,VOLT,SMJK,K,J
C WRITE(6,606) CCNSA,STPLNG,STPWCH,K,J
  IF(J.EQ.JR1) TERM3=AT*TAU*(-TAP(J,K)+TS)*2.D0
  IF(J.NE.JR1) TERM3=AT*TAL*(-TAP(J,K)+TAP(J+1,K))
  IF(J.EQ.2) TERM4=AT*TAU*(-TAP(J,K)+TS)*2.D0
  IF(J.NE.2) TERM4=AT*TAL*(-TAP(J,K)+TAP(J-1,K))
  LENGTH=STPLN2*2.
  CT=(CCNSI*FLMTHK*STPWCH)/(LENGTH)
  IF(K.EQ.KC1) TERM5=CT*TAU*(-TAP(J,K)+TS)
  IF(K.NE.KC1) TERM5=CT*TAU*(-TAP(J,K)+TAP(J,K+1))
  IF(K.NE.2) TERM6=CT*TAU*(-TAP(J,K)+TAP(J,K-1))
  IF(K.EQ.2) TERM6=CT*TAU*(-TAP(J,K)+TS)
  DQJK=TERM1+CCSJK
  DQSJK=T2JK+TERM3+TERM4+TERM5+TERM6
  IF(MOD(ITER,500).NE.0) GO TO 77
  IF(J.NE.2) GC TC 77
  IF(J.EQ.2) GO TO 41
C IF(K.EQ.3.OR.K.EQ.4) GO TO 41
C IF(K.NE.3.OR.K.NE.4) GC TC 77
41 WRITE(6,66)AT,DQSJK,CT
  WRITE(6,67)TERM1,T2JK,TERM3,TERM4,TERM5,TERM6
  WRITE(6,68)DQJK,K,J

```

```

        WRITE(6,65)
66      FCRMAT(1X,1P3E13.3)
67      FCRMAT(1X,1P6E12.3)
68      FORMAT(1X,1PE13.3,1X,13,1X,13)
69      FCRMAT(//)
77      RETURN
      END

C
C
      SUBROUTINE CALCVJ(TEMP,V,Z,ITER)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*4 EPS
      DIMENSION T(6),TT(6)
      DIMENSION V1(6),V2(6),V3(6),V4(6),V5(6),V6(6)
      DIMENSION VV1(6),VV2(6),VV3(6),VV4(6),VV5(6),VV6(6)
      DIMENSION VM(5),ZZ(5),ZO(5)
      DATA ZO/6.00,6.69900,7.00,7.69900,8.00/
      DATA T/300.00,400.00,500.00,600.00,700.00,750.00/
      DATA V1/49.00,53.00,60.00,69.00,81.00,82.00/
      DATA V2/50.00,54.00,61.00,69.00,80.00,81.00/
      DATA V3/50.00,55.00,61.00,70.00,80.66200,80.00/
      DATA V4/57.00,63.00,72.00,81.00,81.00,75.00/
      DATA V5/72.00,87.00,108.00,113.00,85.00,75.00/
      IF (Z.GE.7.99500.OR.TEMP.GE.750.00) GO TO 596
      EPS=C.9E0
      NPNTS=6
      NCURVE=5
      DO 2 J=1,NCURVE
      ZZ(J)=ZO(J)
2      CCNTINUE
      DO 3 J=1,NPNTS
      VV1(J)=V1(J)
      VV2(J)=V2(J)
      VV3(J)=V3(J)
      VV4(J)=V4(J)
      VV5(J)=V5(J)
      TT(J)=T(J)
3      CONTINUE
      DO 5 J=1,NCURVE

      IF(J.EQ.1) CALL DACFI(TEMP,TT,VV1,VM(J),NPNTS,EPS,IER)
      IF(J.EQ.2) CALL CACFI(TEMP,TT,VV2,VM(J),NPNTS,EPS,IER)
      IF(J.EQ.3) CALL DACFI(TEMP,TT,VV3,VM(J),NPNTS,EPS,IER)
      IF(J.EQ.4) CALL DACFI(TEMP,TT,VV4,VM(J),NPNTS,EPS,IER)
      IF(J.EQ.5) CALL CACFI(TEMP,TT,VV5,VM(J),NPNTS,EPS,IER)
C      WRITE(6,65) TEMP,VM(J),J
C65      FCRMAT(1X,1P2E12.2,14)

```

```

5      CCNTINUE
      EPS=3.EC
      CALL CACFI(Z,ZZ,VM,V,NCURVE,EPS,IER)
C      WRITE(6,66) Z,TEMP,V,IER
C66    FORMAT(1X,1P3E12.2,14)
      GC TO 999
      998  V=C.DC
      999  RETURN
      END

C
C
      SUBROUTINE CQAP(VOLT,STPLNG,T,J,K,IJ,DQSJK,SMJK,DTAP,T2JK,ITER)
      IMPLICIT REAL*8 (A-H,C-Z)
      REAL*4 EPS
      DOUBLE PRECISION I,LENGTH,IJ,KS1,KS10
      DIMENSION T(53,11)
      DIMENSION DIFSA(17),DIFSAO(17),TSA(17),TSAC(17)
      DATA TSAO/300.DC,368.DC,403.DC,417.DC,451.DC,504.DC,546.DC,568.DC
      $ 713.DC,871.DC,9CC.DC,
      $ 976.DC,1061.DC,1236.DC,1315.DC,1593.DC,1692.DC/
      DATA DIFSAO/.0786DC,.0786DC,.0645DC,.0590DC,
      $ .C576DC,.C456DC,.0415DC,.0376DC,
      $ .0270DC,.0216DC,.0191DC,.0171DC,.0152DC,.0124DC,.0123DC,.C11DC,
      $ .C12DC0/
      NPNTS=17
      IF(ITER.LE.2) TAU=1.C-9
      IF(ITER.GT.2) TAU=1.D-8
      TEMP=T(J,K)
      DO 1 L=1,NPNTS
      TSA(L)=TSAO(L)
      DIFSA(L)=DIFSAO(L)*1.D-4
1      CCNTINUE
      EPS=1.E-6
      CALL CACFI(TEMP,TSA,DIFSA,DIFSA,NPNTS,EPS,IER)
      C=1.0DC
      TIME=DFLOAT(ITER)*TAU
      IF(T(J,K).LT.500.DC) CONNSA=58.16DC-(.C795DC*T(J,K))
      IF(T(J,K).GE.500.DC.AND.T(J,K).LE.700.DC)
      $ CONNSA=35.125DC-(.C3345DC*T(J,K))
      IF(T(J,K).GT.700.DC.AND.T(J,K).LE.900.DC)
      $ CONNSA=26.38DC-(.02C945DC*T(J,K))
      IF(T(J,K).GT.900.DC) CONNSA=7.3DC
      CP=93C.DC
      TS=300.DC
      TERM1=(VOLT*IJ*TAU)/C
C606  FORMAT(1X,1P3E10.2,2I3)
C      WRITE(6,606) IJ,VOLT,SMJK,K,J
      DTAP=(TERM1+CCSJK)/(SMJK*CP)
      SLOPE=(T(J,K)+DTAP-TS)/TIME
      XTERM=1.DC/DSQRT(DIFFSA*3.1416DC*TIME)
      IF(ITER.EC.1) CTCX=0.CC
      IF(ITER.NE.1) DTDX=-2.DC*SLOPE*TIME*XTERM
      STPWC=4.C-6

```



```

      BT=CCNNSA*STP*DH*STPLNG
C     WRITE(6,6C6) XTERM,SLOPE,DTAP,K,J
      T2JK=(BT/2.)*TAU*CTCX
C     WRITE(6,6C6) BT,DTDX,T2JK,K,J
      IF(MOD(ITER,500).NE.0) GO TO 77
      IF(J.NE.2) GC TC 77
      IF(J.EQ.2) GO TO 41
C     IF(K.EC.3.OR.K.EC.4) GO TO 41
C     IF(K.NE.3.CR.K.NE.4) GC TO 77
41    WRITE(6,68)SLOPE,K,J
      WRITE(6,69)
66    FORMAT(1X,1P3E13.3)
68    FCRMAT(1X,1P1E13.3,1X,13,1X,13)
69    FCRMAT(//)
77    RETURN
      END

```

4. Electrothermal Model, N^+N Spikes

```

      IMPLICIT REAL*8 (A-H,C-Z)
C 'CACFI' IS A SUBROUTINE IN IBM SCIENTIFIC SUBROUTINE PACKAGE (SSP).
C ANY OTHER INTERPOLATION ROUTINE MAY BE USED IN ITS PLACE.
      DOUBLE PRECISION I,ITOT,NA,ND,NDD
      DIMENSION T(53,11),R(53,11),STPRS(53),I(53),DQSUM(53,11),
      $VJ(53),DLGID(53),STPV(53),C2SUBS(53,11),TINT(53,11)
      $,SEGMS(53,11)

C
C ALL CALCULATIONS ARE DONE WITH MKS SYSTEM OF UNITS. NO NORMALIZATION
C OF VARIABLES WAS DONE.
C
C
C MODEL GRID SPECIFICATION
C EACH LONGITUDINAL STRIP HAS INDEX '(J)'
C EACH SEGMENT HAS INDEX '(J,K)'
C
C
C DUE TO THE LARGE AMOUNT OF CPU NECESSARY TO CARRY COMPUTATIONS
C THROUGH 1000 STEPS ALL AT ONCE, SECTIONING OF THE COMPLETE JOB
C IN STEPS OF 200 WAS DONE. AT THE END OF EACH SMALL JOB OF 200 STEPS
C RESULTS WERE STORED ON DISKS AND ACT AS THE INITIAL CONDITIONS FOR
C THE NEXT SMALL JOB OF 200 TIME STEPS. THUS REPLACE LINES 650-1190
C BY LINES 1210-1250.
      NSTPS=210
      JS1=14
      JS2=27
      JS3=45
      JR=53
      JRBY2=(JR+3)/2
      KC=11
      KCJ=3
      KC1=KC-1
      KCJP1=KCJ+1
      KCJP2=KCJ+2
      KC2=KC-2
      JR1=JR-1
      JR2=JR-2
      KC3=KC-3

C
C INITIALIZATION OF CONSTANTS
      ITOT=10.D-3
      SEGLNJ=4.00-6
      CP=930.D0
      NA=1.0026
      ND=1.0022
      NDD=5.0025
      DNSTY=2.3303
      SEGWCH=4.00-6
      FLMTHK=C.6D-6
      SEGARA=SEGWCH*FLMTHK
      SEGLN2=(3.00-5-SEGLNJ)/6.
      SEGLN1=160.D-6

```

```

SEGL1=SEGLN1*SEARA
SEGLJ=SEGLNJ*SEARA
SEGL2=SEGLN2*SEARA
SEGMS1=DNSTY*SEGL1
SEGMSJ=DNSTY*SEGLJ
SEGMS2=DNSTY*SEGL2
TS=300.00

```

C

```

C INITIALIZE ALL STRIPS TO SUBSTRATE TEMPERATURE 'TS'.
C DIVIDE TOTAL APPLIED CURRENT 'ITOT' EQUALLY AMONG ALL LONGITUDINAL
C STRIPS. DETERMINE RESISTANCE 'R(J,K)' OF ALL SEGMENTS AT 'TS'
C EXCEPT THE JUNCTION SEGMENTS I.E. (J,KCJ) FOR STRIP WITH NO SPIKE
C AND (J,KCJP1) FOR STRIP WITH BUILT-IN SPIKE.

```

```

TIME=0.00
DO 5 J=1,JR
  I(J)=ITOT/JR2
  DO 10 K=1,KC
    T(J,K)=TS
    DQSUM(J,K)=C.DC
  10 CONTINUE
  5 CONTINUE
  DO 15 J=2,JR1
    RS=0.00
    DO 20 K=2,KC1

```

C STRIPS WITH SPIKES

```

  IF((J.NE.JS1).AND.(J.NE.JS2).AND.(J.NE.JS3)) GO TO 1
  IF(K.EQ.2) CALL RESIST(SEGLN1,NA,T(J,K),R(J,K))
  IF(K.EQ.KCJ) R(J,K) = 0.0
  IF(K.GT.KCJ.AND.K.LE.KC3) CALL RESIST(SEGLN2,ND,T(J,K),R(J,K))
  IF(K.EQ.KC2) CALL RESIST(SEGLN2,NDD,T(J,K),R(J,K))
  IF(K.GT.KC2) CALL RESIST(SEGLN1,NCD,T(J,K),R(J,K))
  GO TO 11

```

C SPIKE-FREE STRIPS

```

  1 IF(K.LE.2) CALL RESIST(SEGLN1,NA,T(J,K),R(J,K))
    IF(K.EQ.KCJ) R(J,K)=0.0
    IF(K.GT.KCJ.AND.K.LE.KC2) CALL RESIST(SEGLN2,ND,T(J,K),R(J,K))
    IF(K.GT.KC2) CALL RESIST(SEGLN1,NDD,T(J,K),R(J,K))
  11 RS=RS+R(J,K)
  20 CCNTINUE

```

C

```

C JUNCTION VOLTAGE 'VJ(J)' AT TEMPERATURE 'TS' AND AT INITIAL CURRENT
C DISTRIBUTION 'I(J)'

```

```

  DLGID(J)=CLGID(I(J)/SEARA)

```

```

C STRIPS WITH SPIKES AND STRIPS WITHOUT SPIKES ARE TREATED THE SAME
  CALL JNVOLT(T(J,KCJ),VJ(J),DLGID(J))
  IF (VJ(J).GT..0500) GO TO 33
  CALL RESIST(SEGLNJ,ND,T(J,KCJ),R(J,KCJ))
  VJ(J)=I(J)*R(J,KCJ)

```

C SERIES STRIP SPREADING RESISTANCE 'STPRS(J)'

```

  33 STPRS(J)=RS
  15 CCNTINUE

```

```

C
C DEVICE TERMINAL VOLTAGE 'VTCT' WHICH IS THE SAME AS INDIVIDUAL STRIP
C VOLTAGE 'STPV(J)' AT ALL TIMES.
  VTOT=VJ(12)+(I(12)*STPRS(12))
  WRITE (6,2) VTOT,VJ(12),STPRS(12)
2   FORMAT(1X,7H VTCT =,1PE12.3,19H JUNCTION VOLTAGE =,
  $ 1PE12.3,19H STRIP RESISTANCE =,1PE12.3)
C
  N1=1
  N2=NSTPS
C
C DO 555 L=1,1500
C READ((8),END=666) TIME,T,R,VJ,I,VTCT,DQSUM,ITER
C 555 CONTINUE
C 666 N1=ITER+1
C      N2=ITER+200
C
C
C DO 25 J=2,JR1
C MASS 'SEGMS(J,K)' CF EACH SEGMENT
  DO 30 K=2,KC1
    IF(K.EQ.2)          SEGMS(J,K)=SEGMS1
    IF(K.EC.KCJ)        SEGMS(J,K)=SEGMSJ
    IF(K.GT.KCJ.AND.K.LE.KC2) SEGMS(J,K)=SEGMS2
    IF(K.GT.KC2)        SEGMS(J,K)=SEGMS1
  30  CCNTINUE
  25  CONTINUE
C
C
C START TIME INCREMENT 'TAU' LOOP
  DO 35 ITER=N1,N2
    IF(ITER.LE.10) TAU = 1.E-9
    IF(ITER.GT.10) TAU = 1.E-8
    TIME=TIME+TAU
    WRITE(6,4) TIME,ITER
  4   FORMAT(10X,7H TIME =, 1PE13.4,10X,9H INTERVAL,15)
C
C CALCULATE INTERMEDIATE TEMPERATURE 'TINT(J,K)'
  DO 45 J=2,JR1
    DO 50 K=2,KC1
      VOLT=I(J)*R(J,K)
C FOLLOWING WORKS FOR ALL STRIPS, WITH OR WITHOUT SPIKES
      IF(K.EC.2)
        $ CALL DQINT(VOLT,SEGLN1,T,J,K,I(J),DQSUM(J,K),SEGMS(J,K),
        $ DTINT,DQSUBS(J,K),ITER)
      IF(K.EC.KCJ)
        $ CALL DQINT(VOLT,SEGLNJ,T,J,K,I(J),DQSUM(J,K),SEGMS(J,K),
        $ CTINT,DQSUBS(J,K),ITER)
      IF(K.GT.KCJ.AND.K.LE.KC2)
        $ CALL DQINT(VOLT,SEGLN2,T,J,K,I(J),DQSUM(J,K),SEGMS(J,K),
        $ DTINT,DQSUBS(J,K),ITER)
      IF(K.GT.KC2)
        $ CALL DQINT(VOLT,SEGLN1,T,J,K,I(J),DQSUM(J,K),SEGMS(J,K),
        $ CTINT,DQSUBS(J,K),ITER)
      TINT(J,K)=T(J,K)+DTINT
  50  CCNTINUE

```

```

45  CONTINUE
C
C CALCULATE FINAL OR NEW TEMPERATURE 'T(J,K)' FOR ADVANCED TIME 'T+TAU'
  DO 55 J=2,JR1
    DO 60 K=2,KC1
      VOLT=I(J)*R(J,K)
C STRIPS WITH AND WITHOUT SPIKES ARE TREATED THE SAME
      IF(K.EQ.2)
        $ CALL DQ(VOLT,SEGLN1,TINT,J,K,I(J),DQJK,SEGMS(J,K),
        $ DCSUM(J,K),DCSLBS(J,K),ITER)
        IF(K.EQ.KCJ)
          $ CALL DQ(VJ(J),SEGLNJ,TINT,J,K,I(J),DQJK,SEGMS(J,K),
          $ DQSUM(J,K),DQSLBS(J,K),ITER)
          IF(K.GT.KCJ.AND.K.LE.KC2)
            $ CALL DQ(VCLT,SEGLN2,TINT,J,K,I(J),DQJK,SEGMS(J,K),
            $ DQSUM(J,K),DQSLBS(J,K),ITER)
            IF(K.GT.KC2)
              $ CALL DQ(VCLT,SEGLN1,TINT,J,K,I(J),DQJK,SEGMS(J,K),
              $ DQSUM(J,K),DQSLBS(J,K),ITER)
              T(J,K)=T(J,K)+DQJK/(SEGMS(J,K)*CP)
              IF(T(J,K).GE.1680.00) GO TO 177
60  CONTINUE
55  CONTINUE
C
C WRITE NEW TEMPERATURE EVERY 10TH TIME STEP
  IF(ITER.GE.66.AND.ITER.LE.68) GO TO 509
  IF(MOD(ITER,10).NE.9) GO TO 88
509 WRITE(6,6)
6   FORMAT(/)
   WRITE(6,8)((T(J,K),K=2,10),J=2,52)
8   FORMAT(1X,1P9E12.3)
C
C 'STPRS(J)' AT NEW TEMPERATURE
88  DO 65 J=2,JR1
    RS=0.0
    DO 70 K=2,KC1
      IF((J.NE.JS1).AND.(J.NE.JS2).AND.(J.NE.JS3)) GO TO 99
      IF(K.EQ.2)
        $ CALL RESIST(SEGLN1,NA,T(J,K),R(J,K))
        IF(K.EQ.KCJ.AND.VJ(J).GT..0500) R(J,K)=0
        IF(K.EQ.KCJ.AND.VJ(J).LE..0500)
          $CALL RESIST(SEGLNJ,ND,T(J,K),R(J,K))
          IF(K.GT.KCJ.AND.K.LE.KC3)
            $ CALL RESIST(SEGLN2,ND,T(J,K),R(J,K))
            IF(K.EQ.KC3) CALL RESIST(SEGLN2,NDD,T(J,K),R(J,K))
            IF(K.GT.KC3) CALL RESIST(SEGLN1,NDC,T(J,K),R(J,K))
            GO TO 111
99  IF(K.EQ.2)
        $ CALL RESIST(SEGLN1,NA,T(J,K),R(J,K))
        IF(K.EQ.KCJ.AND.VJ(J).GT..0500) R(J,K)=C.00
        IF(K.EQ.KCJ.AND.VJ(J).LE..0500)
          $ CALL RESIST(SEGLNJ,ND,T(J,K),R(J,K))

```

```

      IF(K.GT.KCJ.AND.K.LE.KC2)
      $ CALL RESIST(SEGLN2,ND,T(J,K),R(J,K))
      IF(K.GT.KC2)
      $ CALL RESIST(SEGLN1,NDD,T(J,K),R(J,K))
111  RS=RS+R(J,K)
70   CONTINUE
      STPRS(J)=RS
65   CONTINUE
C
C 'VJ(J)' AT OLD 'I(J)' BUT NEW 'T(J,K)'
      VJBYS=0.00
      STPRSI=0.00
      DC 75 J=2,JR1
      DLOGID(J)=DLOG10(I(J)/SEGARA)
      CALL JNVOLT(T(J,KCJ),VJ(J),DLOGID(J))
      IF(VJ(J).GT..0500) GO TO 133
      CALL RESIST(SEGLNJ,ND,T(J,KCJ),R(J,KCJ))
      VJ(J)=I(J)*R(J,KCJ)
133  VJBYS=VJBYS+(VJ(J)/STPRS(J))
      STPRSI=STPRSI+(1.00/STPRS(J))
75   CONTINUE
C
C 'VTOT' AT NEW 'R(J,K)', NEW 'T(J,K)' BUT OLD 'I(J)'
      VTOT=(ITCT+VJBYS)/STPRSI
C
C START ITERATION LOOP FOR ACCURATE DETERMINATION OF A NEW CURRENT
C DISTRIBUTION 'I(J)'. TESTS FOR CONVERGENCY ON 'I(J)', 'VJ(J)' AND
C 'STPV(J)' WAS NOT IMPLEMENTED DIRECTLY TO SAVE TIME. IT WAS FOUND
C THAT USING 'NLOOP' AS A PARAMETER INITIALLY GIVES A GOOD IDEA AS TO
C THE CONVERGENCY OF THE SUCCESSIVE VALUES.
      NLOOP=10
      DC 85 ITLCCP=1,NLCCP
      CITOT=0.00
      VJBYS=0.00
      STPRSI=0.00
      DO 90 J=2,JR1
      I(J)=(VTOT-VJ(J))/STPRS(J)
      IF(I(J).LE.0.00) I(J)=0.00
      IF(I(J).LE.0.00) VJ(J)=VTOT
      IF(I(J).LE.0.00) GO TO 155
      DLOGID(J)=DLOG10(I(J)/SEGARA)
      CALL JNVOLT(T(J,KCJ),VJ(J),DLOGID(J))
      IF(VJ(J).GT..0500) GO TO 155
      CALL RESIST(SEGLNJ,ND,T(J,KCJ),R(J,KCJ))
      VJ(J)=I(J)*R(J,KCJ)
155  STPV(J)=I(J)*STPRS(J)+VJ(J)
      VJBYS=VJBYS+(VJ(J)/STPRS(J))
      STPRSI=STPRSI+(1.00/STPRS(J))
C
C SUM 'CITOT' OF STRIP CURRENTS 'I(J)'
      CITOT=CITOT+I(J)
90   CONTINUE

```

```

C
C NEW APPROXIMATION TO DEVICE TERMINAL VOLTAGE 'VICT' AT NEW
C 'T(J,K)', NEWLY APPROXIMATED 'VJ(J)' AND 'I(J)'.
      VTOT=(ITCT+VJBYRS)/STPRS1
85   CONTINUE
C
C END OF ITERATION LCCP
C
C PRINT RESULTS OF PRESENT TIME STEP.
      IF(ITER.GE.66.AND.ITER.LE.68) GO TO 409
      IF(MOD(ITER,1C).NE.9) GO TO 166
409  WRITE(6,12) VICT,CITCT
12   FORMAT(1X,7H VTOT =, 1PE10.3,10X,13H ITCT(CALC) =,1PE14.7)
      WRITE(6,14) (STPV(J),J=2,52)
14   FORMAT(1X,14H STRIP VOLTAGE/1X,1P10E13.5)
      WRITE(6,16) (VJ(J),J=2,52)
16   FORMAT(1X,17H JUNCTION VOLTAGE/1X,1P10E13.5)
      WRITE(6,18) (I(J),J=2,52)
18   FORMAT(1X,14H STRIP CURRENT/1X,1P10E13.5)
166  CONTINUE
C
C WRITE RESULTS OF PRESENT TIME STEP ON DISKS FOR STORAGE
      WRITE(9) TIME,T,R,VJ,I,VTOT,CCSUM,ITER
35   CONTINUE
      GO TO 309
C
C END OF TIME INCREMENT LCCP
C
177  WRITE(9) TIME,T,R,VJ,I,VTOT,CCSUM,ITER
309  STOP
      END
C
C CALCULATION OF SEGMENT RESISTANCES 'R(J,K)' FROM MOBILITY AND
C RESISTIVITY THAT ARE TEMPERATURE DEPENDENT.
      SUBROUTINE RESIST(SEGLNG,DCPING,TEMP,RES)
      IMPLICIT REAL*8 (A-H,G-Z)
      DOUBLE PRECISION MUOP,NP,MUON,NN,KI,NI,MUNE,MUPE,MUP,MUN
      DOPIN1=DCPING*1.0D-6
      SEGWDH=4.0D-6
      FLMTHK=0.6D-6
      SEGARA=FLMTHK*SEGWDH
      MUOP=480.0D0
      NP=4.0D16
      SP=81.0D0
      AP=6.1D3
      FP=1.6D0
      BP=2.5D4
      MUCN=1400.0D0
      NN=3.0D16
      SN=350.0D0
      AN=3.5D3
      FN=8.8D0
      BN=7.4D3

```



```

C=1.6C-19
EM=1.0D5
EG=1.106C0*1.6C-19
KI=1.5045
BK=1.38D-23
NI=(KI**0.5D0)*(TEMP**1.5D0)*DEXP(-EG/(2.0D*BK*TEMP))
SQRTM=DSQRT((DCPING/2.0D)**2+NI**2)
MUNE=MUON*DSQRT(1.0D/(1.0D+DCPIN1/((DOPIN1/SA)+AN)+(EM/AN)**2
$ /((EM/AN)+FN)+(EM/BN)**2))
MUPE=MUOP*DSQRT(1.0D/(1.0D+DCPIN1/((DCPIN1/SF)+NP)+(EM/AP)**2/
$ ((EM/AP)+FP)+(EM/BP)**2))
MLF=MUPE*1.5738C2*(1.0D/TEMP)**2.5
MUN=MUNE*1.5738D2*(1.0D/TEMP)**2.5
RHO=(1.0D/(Q*(MUP*(DOPING/2.0D+SQRTM)+MUN*(-DCPING/2.0D+SQRTM)))
RES=(RHO*SEGLNG)/SEGARA
RETURN
END

```

C
C CHANGE IN ENERGY 'DC' OF A SEGMENT BASED ON HEAT TRANSFER TC AND
C FROM ITS SURROUNDING STRIPS.

```

SUBROUTINE CC(VCLI,SEGLNG,TINT,J,K,IJ,CQJK,SEGMJK,DQSJK,
$ DQSUBS,ITER)
IMPLICIT REAL*8 (A-F,O-Z)
REAL*4 EPS
DOUBLE PRECISION I,LENGTH,IJ,KSI,KSIC
DIMENSION TINT(53,11)
DIMENSION TSI(17),TSIC(17),KSI(17),KSIC(17),TSA(17),TSAG(17)
DIMENSION DIFSA(17),DIFSAO(17)

```

C
C EXPERIMENTAL DATA FOR SILICON AND SAPPHIRE THERMAL CONDUCTIVITY
C AS A FUNCTION OF TEMPERATURE.

```

DATA TSIC/273.0D,300.0D,350.0D,400.0D,500.0D,600.0D,700.0D,800.0D
$ 900.0D,1000.0D,
$ 1100.0D,1200.0D,1300.0D,1400.0D,1500.0D,1600.0D,1685.0D/
DATA KSI0/168.0D,148.0D,119.0D,98.90D,76.20D,61.90D,50.80D,42.2D
$ 35.90D,
$ 31.20D,27.90D,25.70D,24.40D,23.50D,22.70D,22.10D,22.0D/
JR=53
KC=11
JR1=JR-1
KC1=KC-1
KC2=KC-2
TS=300.0D
IF(ITER.LE.2) TAL=1.0-9
IF(ITER.GT.2) TAU=1.0-8
SEGLNJ=4.0D-6
SEGLN2=(3.0D-5-SEGLNJ)/6.0D
SEGLN1=160.0-6
FLMTHK=C.6D-6
SEGWDT=4.0C-6
C=1.000
EPS=2.0E0
TEMP=TINT(J,K)
CP=930.0D
NPNTS=17
TIME=DFLOAT(ITER)*TAU

```

C
C DUPLICATION OF THERMAL CONDUCTIVITY DATA TO PREVENT THEIR POSSIBLE
C DESTRUCTION WHEN USED IN SSP INTERPOLATION SUBROUTINE 'DACFI'

DO 5 L=1,NPNTS
TSA(L)=TSAO(L)
TSI(L)=TSIC(L)
KSI(L)=KSIQ(L)

5
C
C
C
CONTINUE

CALL DACFI(TEMP,TSI,KSI,CCNNSI,NPNTS,EPS,IER)
IF(TINT(J,K).LT.500.00) CCNNSA=58.1600-(.079500*TINT(J,K))
IF(TINT(J,K).GE.500.00.AND.TINT(J,K).LE.700.00)
\$ CCNNSA=35.13500-(.0334500*TINT(J,K))
IF(TINT(J,K).GT.700.00.AND.TINT(J,K).LE.900.00)
\$ CCNNSA=26.2800-(.02094500*TINT(J,K))
IF(TINT(J,K).GT.900.00) CCNNSA=7.200
AT=(FLMTHK*SEGLNG*CCNNSI)/(SEGLN2*2.)
DQJOUL=(VOLT*IJ*TAU)/C
IF(J.EQ.JR1) DCJF1K=AT*TAU*(-TINT(J,K)+TS)*2.00
IF(J.NE.JR1) DCJF1K=AT*TAU*(-TINT(J,K)+TINT(J+1,K))
IF(J.EQ.2) DCJMK=AT*TAU*(-TINT(J,K)+TS)*2.00
IF(J.NE.2) DCJMK=AT*TAU*(-TINT(J,K)+TINT(J-1,K))
CT=(CCNNSI*FLMTHK*SEGLN2)/(SEGLN2*2.)
IF(K.EQ.KC1) DQJKP1=CT*TAU*(-TINT(J,K)+TS)
IF(K.NE.KC1) DQJKP1=CT*TAU*(-TINT(J,K)+TINT(J,K+1))
IF(K.NE.2) DQJKM1=CT*TAU*(-TINT(J,K)+TINT(J,K-1))
IF(K.EQ.2) DQJKM1=CT*TAU*(-TINT(J,K)+TS)

C
C TOTAL CHANGE IN ENERGY 'DQJK' FOR EACH SEGMENT
DQJK=DCJF1K+DCJMK
DQSK=DQSLBS+DCJF1K+DCJMK+DCJMKP1+DCJMKM1
RETURN
END

C
C DETERMINATION OF JUNCTION VOLTAGE BY TWO STEP INTERPOLATION.
SUBROUTINE JAVCLT(TEMP,V,Z)
IMPLICIT REAL*8 (A-H,C-Z)
REAL*4 EPS
DIMENSION T(5),II(5)
DIMENSION V1(5),V2(5),V3(5),V4(5),V5(5),V6(5)
DIMENSION VV1(5),VV2(5),VV3(5),VV4(5),VV5(5),VV6(5)
DIMENSION VNI(5),ZC(5),ZZ(5)

C
C DATA OBTAINED FROM ONE-DIMENSIONAL PN JUNCTION SIMULATIONS.
C VN-T ETC. CURVES ARE JUNCTION VOLTAGE - TEMPERATURE CURVES FOR
C A PARTICULAR VALUE OF THE LOGARITHM OF CURRENT DENSITY 'ZC(N)'
C WHERE 'N' TAKES ON VALUES 1-5.

DATA ZC/6.00,6.69900,7.00,7.69900,8.00/
DATA T/300.00,400.00,500.00,600.00,700.00/
DATA V1/49.00,53.00,60.00,68.900,81.00/
DATA V2/50.00,54.00,59.900,69.00,80.00/
DATA V3/50.100,55.00,61.00,70.00,80.66200/
DATA V4/57.00,63.00,72.00,81.00,81.200/
DATA V5/72.00,87.00,108.00,113.00,85.00/

```

C
C
  IF (Z.GE.8.D0.OR.TEMP.GE.700.D0) GO TO 1
  EPS=1.0E0
  NPNTS=5
  NCURVE=5
  DO 5 J=1,NCURVE
    ZZ(J)=ZO(J)
  5  CONTINUE
C
C  DUPLICATION OF VN-T DATA TO PREVENT POSSIBLE DESTRUCTION IN 'CACFI'
  DO 10 J=1,NPNTS
    VV1(J)=V1(J)
    VV2(J)=V2(J)
    VV3(J)=V3(J)
    VV4(J)=V4(J)
    VV5(J)=V5(J)
    TT(J)=T(J)
  10  CONTINUE
C
C  INTERPOLATE A JUNCTION VOLTAGE 'VNI' AT 'T(J,K)' ON EACH CURVE
C  VN-T OF CONSTANT CURRENT DENSITY. THIS SET OF N INTERPOLATED POINTS
C  FORM A CURVE OF VNI-Z, Z BEING THE LOGARITHM OF CURRENT DENSITY,
C  AT CONSTANT SEGMENT TEMPERATURE 'T(J,K)'.
  DO 15 J=1,NCURVE
    IF(J.EQ.1) CALL CACFI(TEMP,TT,VV1,VNI(J),NPNTS,EPS,IER)
    IF(J.EQ.2) CALL CACFI(TEMP,TT,VV2,VNI(J),NPNTS,EPS,IER)
    IF(J.EQ.3) CALL CACFI(TEMP,TT,VV3,VNI(J),NPNTS,EPS,IER)
    IF(J.EQ.4) CALL CACFI(TEMP,TT,VV4,VNI(J),NPNTS,EPS,IER)
    IF(J.EQ.5) CALL CACFI(TEMP,TT,VV5,VNI(J),NPNTS,EPS,IER)
  15  CONTINUE
C
C  INTERPOLATE 'V' AT GIVEN 'Z' ON THE SINGLE VNI-Z CURVE OBTAINED ABOVE
C  AT CONSTANT SEGMENT TEMPERATURE 'T(J,K)'.
  EPS=1.E0
  CALL CACFI(Z,ZZ,VNI,V,NCURVE,EPS,IER)
  GO TO 11
  1  V=C.DC
  11  RETURN
  ENC
C
C
C  DETERMINATION OF TIME DEPENDENT TEMPERATURE FUNCTION 'PHI', AND
C  THE SUBSTRATE HEATING TERM DQSUBS FROM THE SOLUTION OF ONE-DIMENSIONAL
C  LINEAR HEAT FLOW EQUATION.
  SUBROUTINE DQINT(VOLT,SEGLNG,T,J,K,IJ,DQSJK,SEGMJK,DTINT,
  & DQSUBS,ITER)
  IMPLICIT REAL*8 (A-H,C-Z)
  REAL*4 EPS
  DOUBLE PRECISION I,LENGTH,IJ,KS1,KSIC
  DIMENSION T(53,11)
  DIMENSION DIFSA(17),DIFSAC(17),TSA(17),TSAO(17)

```

```

C
C EXPERIMENTAL DATA FOR TEMPERATURE DEPENDENT THERMAL DIFFUSIVITY OF
C SAPPHIRE.
  DATA TSAC/300.00,368.00,403.00,417.00,451.00,504.00,546.00,568.00,
  $ 713.00,871.00,900.00,
  $ 976.00,1061.00,1236.00,1315.00,1553.00,1692.00/
  DATA DIFSA0/.078600,.078600,.064500,.059000,
  $ .057600,.045600,.041500,.037600,
  $ .027000,.021600,.019100,.017100,.015200,.012400,.012300,.01100,
  $ .012000/

C
C
  NPNTS=17
  EPS=1.E-6
  SEGWDH=4.C-6
  CF=93C.00
  TS=300.00
  C=1.000
  IF(ITER.LE.2) TAU=1.D-9
  IF(ITER.GT.2) TAU=1.D-8
  TEMP=T(J,K)

C
C DUPLICATION OF DATA TO PREVENT DESTRUCTION IN 'DACFI'
  DO 5 L=1,NPNTS
    TSA(L)=TSAC(L)
    DIFSA(L)=DIFSA0(L)*1.D-4
5  CONTINUE
  CALL DACFI(TEMP,TSA,DIFSA,DIFFSA,NPNTS,EPS,IER)
  TIME=DFLGAT(ITER)*TAU
  IF(T(J,K).LT.500.00) CCNNSA=58.1600-(.079500*T(J,K))
  IF(T(J,K).GE.500.00.AND.T(J,K).LE.700.00)
  $ CCNNSA=35.13500-(.0334500*T(J,K))
  IF(T(J,K).GT.700.00.AND.T(J,K).LE.900.00)
  $ CCNNSA=26.3800-(.02094500*T(J,K))
  IF(T(J,K).GT.900.00) CCNNSA=7.300
  DQJOUL=(VCLT*IJ*TAU)/C
  DTINT=(DQJOUL+DQSJK)/(SEGMJK*CP)

C
C SLOPE OF THE FUNCTIONAL FORM OF 'PHI'
  SLOPE=(T(J,K)+DTINT-TS)/TIME
  IF(ITER.EC.1) DTDX=0.00
  IF(ITER.NE.1) DTDX=-2.00*SLOPE*TIME*(1.00/(DSQRT(DIFFSA*3.141600
  $ *TIME)))
  BT=CCNNSA*SEGWDH*SEGLAG

C
C DETERMINATION OF SUBSTRATE HEATING TERM FROM 'DTDX' OBTAINED BY
C SOLVING ONE-DIMENSIONAL LINEAR HEAT FLOW PROBLEM.
  DQSUBS=(BT/2.)*TAU*DTDX
  RETURN
END

```

