AD-A086 668 TEXAS INSTRUMENTS INC DALLAS F/G 9/1
RELIABILITY EVALUATION OF GAAS POWER FETS.(U)
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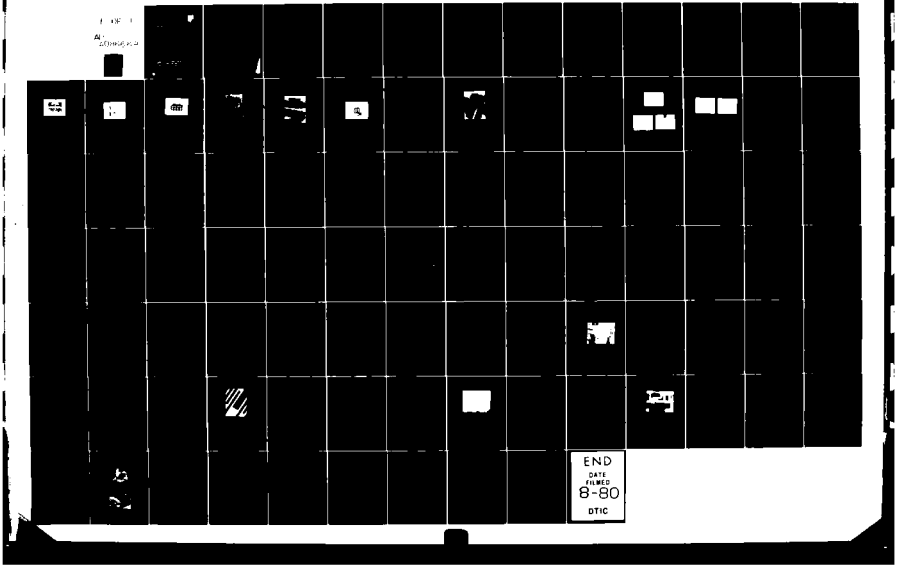

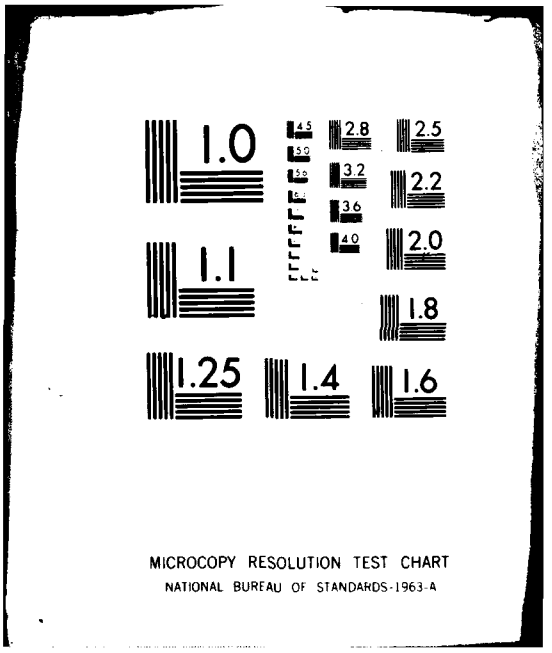
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RADC-TR-80-124
Interim Technical Report
April 1980

RELIABILITY EVALUATION OF GaAs POWER FETs

Texas Instruments, Incorporated

H.H. Hacksty
L.M. Jay

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-80-124	2. GOVT ACCESSION NO.: AD-A086 668
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): RELIABILITY EVALUATION OF GaAs POWER FETs,	5. TYPE OF REPORT & PERIOD COVERED: Interim Report, 7 Nov 78 — 6 Nov 79
6. PERFORMING ORG. REPORT NUMBER: TI-08-80-06	
7. AUTHOR(s): H.M. Macksey, L.W. Joy	8. CONTRACT OR GRANT NUMBER(s): F30602-79-C-0037
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Texas Instruments, Incorporated, 13500 North Central Expressway, Dallas TX 75265	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 23380144, P1
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRP), Griffiss AFB NY 13441	12. REPORT DATE: Apr 80
	13. NUMBER OF PAGES: 82
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Edward J. Calucci (RBRP)
This program was partially sponsored by the Federal Aviation Agency with the aid of Mr. Fred Sakate, ARD-350, Wash DC.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs Field Effect Transistor (FET)
Reliability
Thermal Resistance
Electrical Stress
Environmental Stress
Characterization

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this contract is to assess and establish the reliability and life characteristics of commercially available, medium power GaAs MESFETs and to identify any associated failure mechanisms. The devices chosen for this study were the TI MSX802 and laboratory devices, Dexcel 3615A-P100F, MSC 88002, and NEC 868196. All are hermetically packaged GaAs power FETs with approximately 0.5 W output power. The study includes device physical, electrical (cw and pulsed), and environmental - (over)

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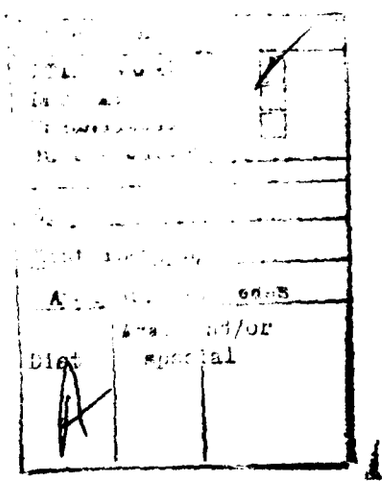
characterization, electrical (cw and pulsed) and environmental stress tests, and failure analysis.

The device physical characterization has been completed and the data are presented. The cw electrical characterization is almost complete, and detailed data are shown for a typical device. No device had significant changes in electrical parameters following operation for 1000 hours at room temperature. The environmental characterization has just begun, and no results are available yet. The results from the cw electrical stress tests, which have been completed, are presented. There are some correlations between the various device structures and the results from different manufacturer's devices. The environmental stress tests have begun, and preliminary results are presented. Most of the effort for the remainder of the program will be spent on completing these tests. The pulse characterization and stress tests have not yet begun. The failure analyses are described along with the test causing the failure.



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SECTION I
INTRODUCTION

This interim report describes Texas Instruments progress during the period from 7 November 1978 through 6 November 1979 on Rome Air Development Center Contract No. F30602-79-C-0037. The objective of this contract is to assess and establish the reliability and life characteristics of commercially available, medium-power GaAs MESFETs and to identify any associated failure mechanisms.

The program consists of several major tasks, as summarized in Figure 1, which is reproduced from TI's proposal. The work done on each of these tasks is discussed below. Efforts on the pulse characterization and stress and the electrical characterization of the devices as oscillators have not yet begun. The environmental characterization work has just begun and is scheduled to be completed over the next two months; however, no data are available yet. Any failure analysis results that have been obtained are discussed along with the characterization or stress tests producing the failure.

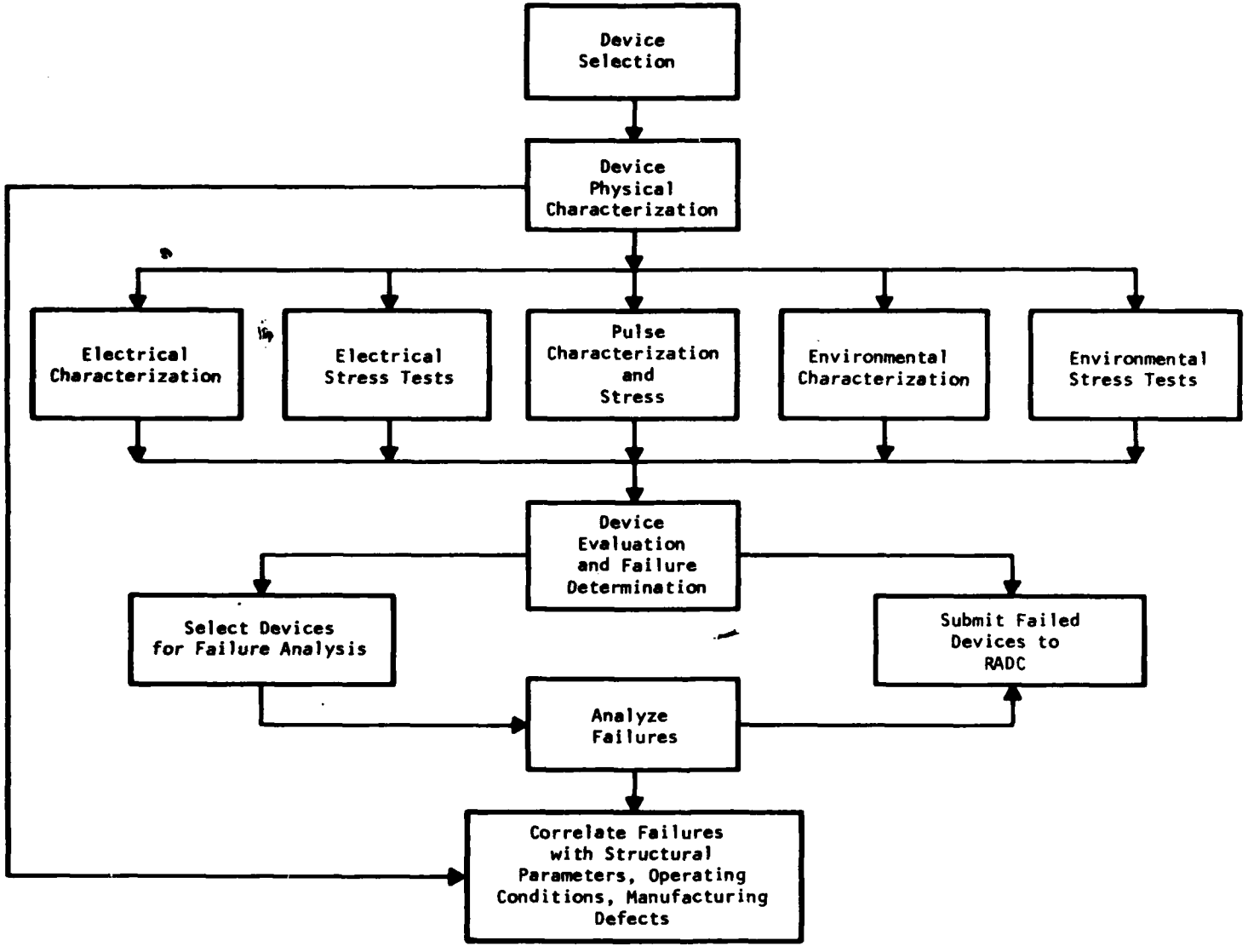


Figure 1 Diagram Illustrating General Approach to GaAs Power FET Reliability Characterization

SECTION II
DEVICE SELECTION AND PHYSICAL CHARACTERIZATION

Only hermetic devices were selected for this study to improve the reproducibility of the results and provide a better indication of the manufacturer's capability. In this way the results would not be clouded by questions of how well the chips were bonded at Texas Instruments. The devices chosen all had 1200 μm to 1500 μm gate width and about 0.5 W rated output power. An attempt was made to choose devices as much alike as possible so that comparisons between different manufacturers would be more valid.

The devices employed were the TI MSX802, a TI laboratory device, NEC 868196, Dexcel 3615A-P100F, and MSC 88002. Their physical characteristics are described below.

A. Device Design

Photographs of the five device types are shown in Figures 2 through 5 and Figure 7. The two TI devices shown in Figures 2 and 3 have the source pads interconnected by bond wires with the gate pads on one side of the chip and drain pads on the other. The Dexcel device shown in Figure 4 also has all connections made by bond wires, but with a different layout than the TI devices. The source pad is at the periphery of the chip, giving a relatively low source lead inductance, but requiring the drain bond wires from the package to pass over the source pad to reach the interior drain pads. The NEC device shown in Figure 5 has source contacts connected to the large peripheral source pad by bridging the gate bus bar with an SiO_2 layer separating the two. This eliminates the need for bond wires to each source pad. Figure 6 is an SEM photograph of one of the source overlays. The source is grounded by a metallization layer applied to the edge of the chip, so no source wires are

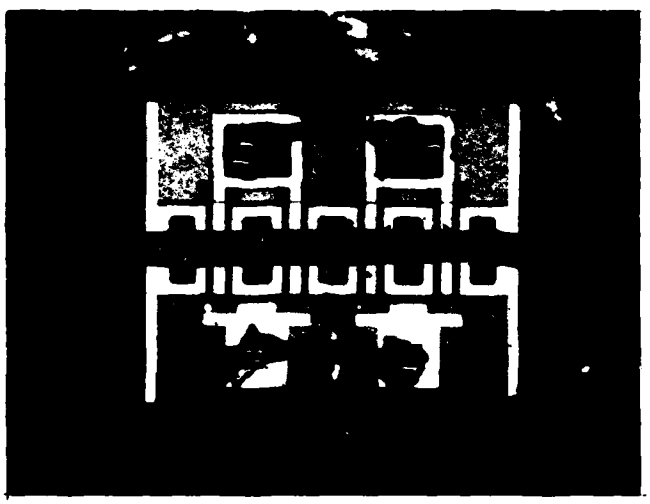


Figure 2 Photograph of TI MSX802 Device

Figure 3 Photograph of TI Laboratory Device

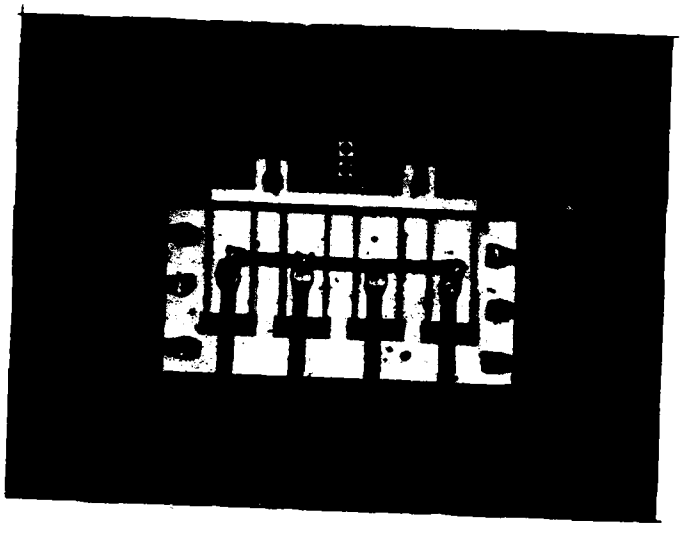


Figure 4 Photograph of Dexcel 3615A Device

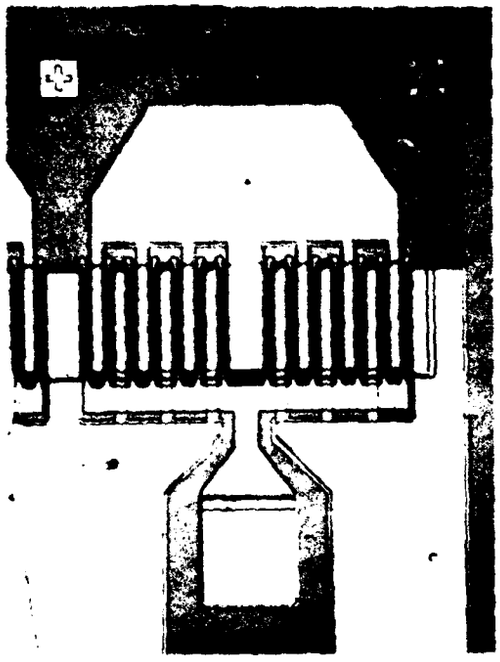


Figure 5 Photograph of NEC 868196 Device

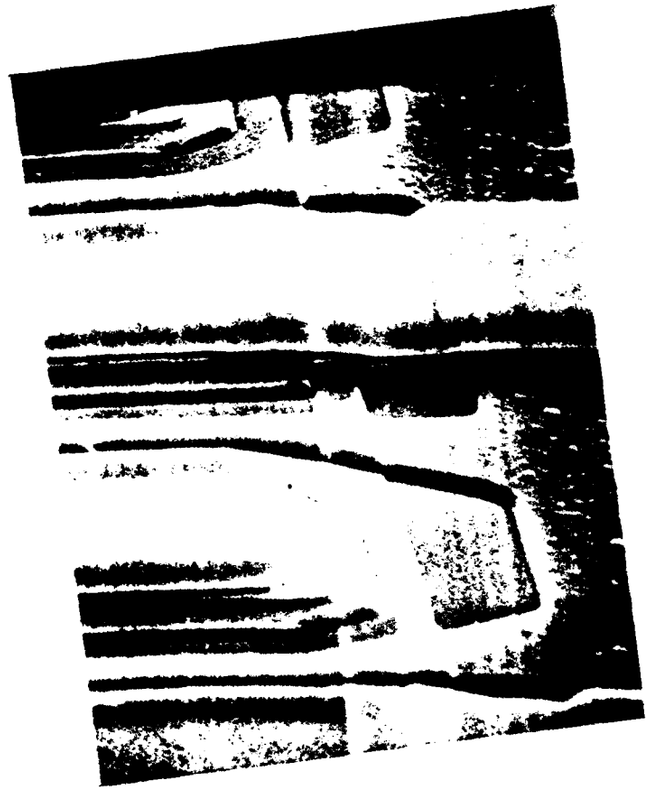


Figure 6 SEM Photograph of Source Overlay on NEC 868196 Device

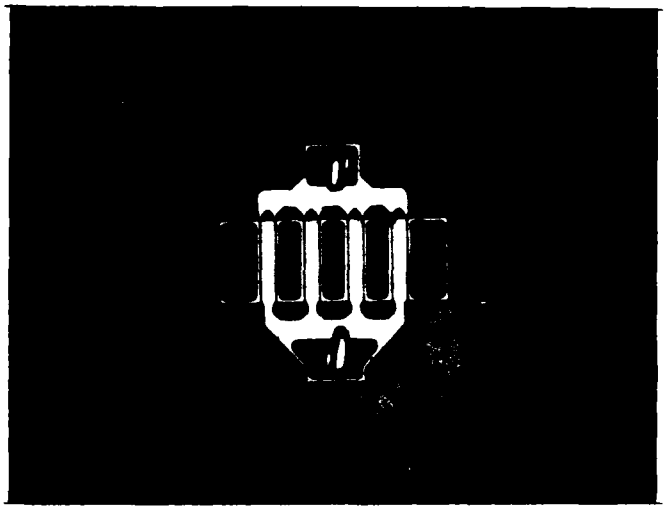


Figure 7 Photograph of Unflipped MSC 88002 Device

needed. The MSC device is different from the others in that it is bonded in a flipped configuration with the plated-up source pads thermocompression-bonded to a raised Au-plated pedestal on the package. Figure 7 is a photograph of an MSC device removed from its package and placed upright. Another difference is that the MSC gate is self-aligned to the source/drain metallization and consequently is difficult to examine for failure analysis. Figure 8 is an SEM photograph of a gate finger near the edge of the device mesa.

Other geometrical parameters of the various devices are summarized in Table 1. These data were obtained from direct measurement of typical devices. Note that the TI production device is the only one with larger than 1 μm gates, and that the MSC device has a very small source-drain spacing due to the self-aligned gate. The NEC devices have relatively small gate-to-gate spacing, which may cause excessive device heating.

B. Device Material Parameters

The material parameters for the various devices are summarized in Table 2. Most of this information was obtained in conversations with the manufacturers. The NEC representative did not know the thickness of the buffer layer or whether any epitaxial layer thinning had been done. The other NEC material data not listed were regarded as proprietary by the manufacturer.

By examining the I-V characteristics of the devices from each manufacturer, further insights can be gained into the material properties. Figure 9 contains photographs of I-V characteristics of typical devices from each manufacturer. The TI devices have higher maximum transconductances than the others due to a combination of high doping level, low parasitic resistance owing to the recessed gate, and high mobility. The Dexcel devices have a high "knee" voltage due to the high parasitic resistance caused by the lack of a recessed gate. The MSC device has a low knee voltage due to the n^+ contacts and the small source-drain separation. In Figure 10 the drain current of these devices is plotted as a function of gate voltage at constant drain voltage. The current is normalized to 1200 μm gate width. The TI devices have

Figure 8 SEM Photograph of Gate Area of MSC 88002 Device

Table I

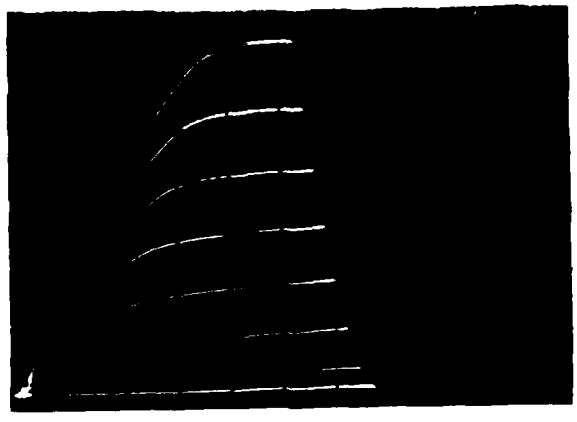
Device Geometrical Parameters

Device Type	Gate Length (μm)	Gate Width (mm)	Gate Finger Width (μm)	Number of Cells	Source-Drain Spacing (μm)	Gate Location	Source Width (μm)	Drain Width (μm)	Chip Thickness (μm)	Chip Size (μm)	Interconnect Scheme
TI MSX802	1.6	1.2	150	2	5	Center	75	25	100	625 x 500	Bond Wires
TI Lab	1.0	1.2	150	1	5	Center	50	25	100	500 x 500	Bond Wires
Dexcel 3615A	1.0	1.5	187.5	1	5	Near Source	45	71	100	700 x 475	Bond Wires
MSC 88002	1.0	1.2	150	1	2	Center	50	25	200	525 x 575	Flip-Mounted
NEC 868196	1.0	1.4	100	1	5.5	Center	15	15	125	375 x 635	Source Overlay

Table 2

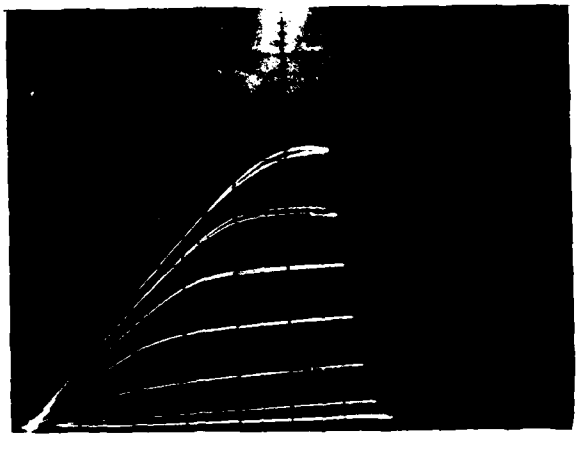
Device Material Parameters

Device Type	Epitaxial Growth Technique	Buffer Layer	Buffer Layer Thickness (μm)	Active Layer Doping Level ($\times 10^{17}$) (cm^{-3})	Active Layer Thickness (μm)	Doping Profile	Presence of n^+ Contacts	Epitaxial Layer Thinning Technique	Active Layer Dopant	Surface Morphology
TI MSX802	VPE	Undoped	1-2	0.8	0.3	Flat	No	Anodic Oxidation	S	Smooth to cloudy
TI Laboratory	VPE	Undoped	1-2	1.2-1.9	~ 0.2	Flat	No	Anodic Oxidation	S	Smooth to cloudy
Dexcel 3615A	LPE	None	-	1-2	~ 0.3	Flat	No	Some etched	Sn	Smooth; some pyramids
MSC 88002	VPE	Undoped	?	~ 1	~ 0.3	Flat	Yes	None	Si	Somewhat cloudy
NEC 868196	VPE	Undoped	?	?	?	?	No	?	?	Smooth



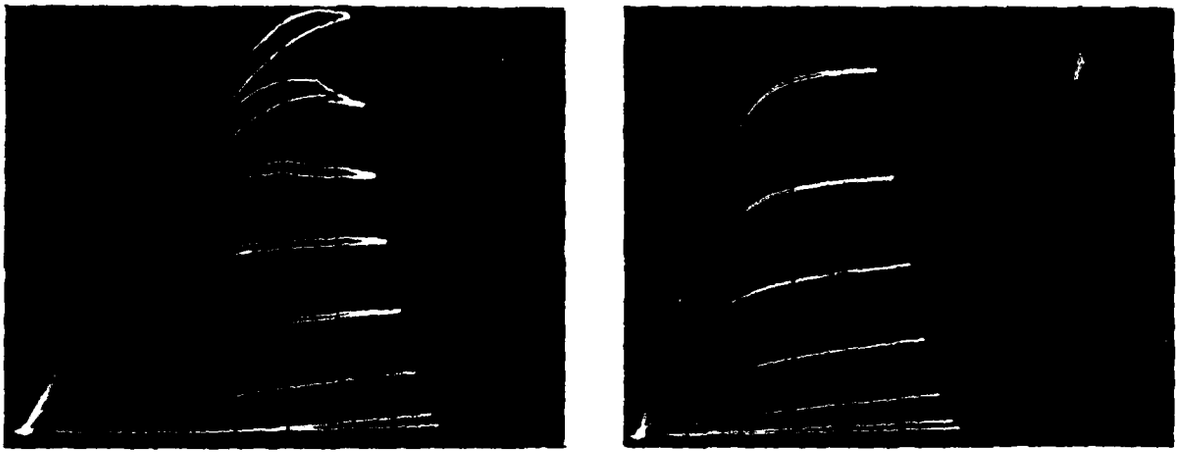
(a) TI MSX802
50 mA/div.
0.5 V/div
0.5 V/step

(b) TI Laboratory
50 mA/div
0.5 V/div
1 V/step



(c) Dexcel 3615A
100 mA/div
0.5 V/div
1 V/step

Figure 9 Current-Voltage Characteristics of Typical Devices



(d) NEC 868196
50 mA/div
0.5 V/div
1 V/step

(e) MSC 88002
50 mA/div
0.5 V/div
1 V/step

Figure 9 (Continued)

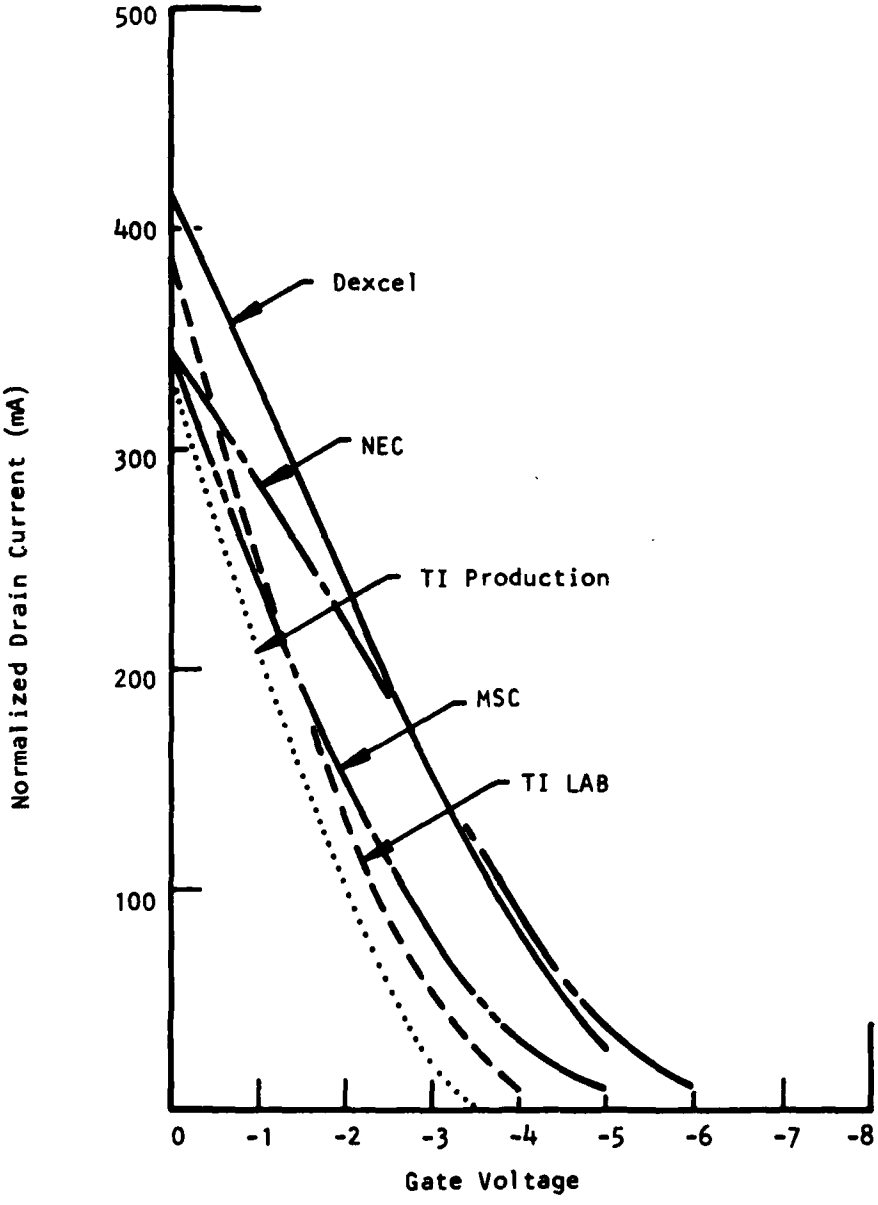


Figure 10 Normalized Saturated Drain Current as a Function of Gate Voltage

the largest slope due to their higher transconductance. The MSC device has the greatest curvature at high gate voltage, which is indicative of a poorer (less sharp) doping transition between active layer and buffer layer (or substrate). The TI Dexcel, and NEC devices are about the same in this respect. The NEC device is very interesting. The transconductance is significantly lower than the others, and careful examination of Figure 10 shows that the curve is actually convex upward between $V_g = 0$ and $V_g = -2$. This could only be caused by a retrograde active layer doping profile (more lightly doped on the surface). The low value of transconductance and high knee voltage [Figure 9(d)] also indicate a relatively low active layer doping level. As will be seen, this doping profile affects the results of the electrical stress tests.

Some interesting data from Table 2 show that all the manufacturers except Dexcel use vapor phase epitaxy ($AsCl_3$ technique) for layer growth and employ an undoped buffer layer. Dexcel uses liquid phase epitaxy and no buffer layer. Another fact that stands out is that MSC is the only manufacturer to use n^+ layers under the source and drain contacts.

C. Device Fabrication

The device fabrication parameters such as metallization types and thicknesses are summarized in Table 3. Most of the data were obtained in conversations with the manufacturers. Where data on metallization thickness were not obtained, measured values were substituted and are denoted as approximate, since the measurements were difficult and not very accurate. Some data on ohmic contact alloy time are missing, but this is not critical, since AuGe/Ni was employed by all manufacturers and the alloy temperature probably does not vary significantly.

It should be noted that the NEC device is the only one with Al gates. The Al is kept from contact with Au bond wires by a TiPt bridge between the bonding pad and the gate fingers. The gates of the TI lab device are defined by e-beam lithography, while all the others are defined by optical

Table 3

Device Fabrication Parameters

Device Type	Mesa Edge (μm)	Ohmic Contact Metal	Ohmic Contact Thickness (μm)	Alloy Cycle	Gate Metal-lization	Gate Metal Thickness (μm)	Gate Fabrication Technique	Additional Metal on Source/Drain (μm)	Gate Recess (μm)	Passivation or Protection	Comments
TI MSX802	0.75 Sharp Edge	AuGe/Ni	0.15	450°C/ 1 min	Ti/Pt/Au	.05/.1/.4	Optical, Lift-Off	0.02 Cr, 0.5 Au, 5 Au Plate	0.1-0.2	Plasma Silicon Nitride	
TI Lab	0.75 Sharp Edge	AuGe/Ni	0.15	450°C/ 1 min	Ti/Pt/Au	.05/.05/.4	e-Beam, Lift-Off	0.02 Cr, 0.5 Au, 5 Au Plate	0.1-0.2	Plasma Silicon Nitride	
Dexcel 3615A	0.25 Sharp Edge	AuGe/Ni	0.2	?	Ti/Pt/Au	.01/.05/.18	Optical, Lift-Off	0.2 Au	None	SiO	
MSC 88002	Gradual	AuGe/Ni	~ 0.2	?	Ti/W/Au	~ 0.5	Self Align	TiPtAu/ TiWAu, 12 Au Plate	~ 0.5	None	
NEC 868196	0.25 Gradual	AuGe/Ni	0.15	450°C	Al	~ 0.4	Optical, Lift-Off	0.4 TiPtAu, 1 Au Plate	0.2	CVD SiO_2	Ti/Pt bridge to gate pad. Recessed area wider than gate.

lithography. The MSC gates are defined by a self-aligned process. The TI devices have a deeper mesa etch than the others. The Dexcel device is the one without a gate recess, and the NEC device has a recessed area $\sim 3\,\mu m$ wide (much wider than the 1 μm gate), which they say increases the drain voltage capability. Each of the manufacturers uses a different passivation material.

D. Additional Characteristics

Several additional characteristics are described in this section. The data are summarized in Table 4. The current-voltage characteristics of all devices tested to date in any way (25 to 30 from each manufacturer) have been photographed. The values of I_{dss} were taken from these photographs and the mean and standard deviations calculated for each manufacturer. In Table 4 the standard deviation divided by the mean is recorded. The Dexcel devices have a high standard deviation, while the NEC devices have the lowest. This value (9.8%) is quite impressive, as these devices were from several different slices, while the TI devices were all from one slice. A low standard deviation in I_{dss} is indicative of good epitaxial layer uniformity and process control.

All the manufacturers employ visual inspection and dc probing of all chips. Texas Instruments is the only manufacturer that does not rf test packaged devices before shipping.

The device thermal resistance is of critical importance for the present study because the MTTF depends on the channel temperature. An accurate MTTF at room temperature cannot be derived unless the channel temperature is known in each of the elevated temperature stress tests. For this reason, extensive thermal measurements have been conducted by a variety of techniques.

The maximum thermal resistance ("typical" in the case of Dexcel) given by each manufacturer is shown in the first column in Table 4. Our best estimates of the actual values are shown in the second column. For upright-mounted

Table 4
Additional Characteristics of GaAs Power FETs

Device Type	Manufacturer's Maximum Thermal Resistance (°C/W)	Measured Thermal Resistance (°C/W)	I_{dss} Uniformity Standard Deviation/Mean (%)	Screening and Quality Control	Cost
TI MSX802	75	44-75	10.3	500 X Visual; dc probe	$125
TI Laboratory	-	45-55	14.6	500 X Visual; dc probe	-
Dexcel 3615 A	40	41	62.0	Low power visual; dc probe; high power visual; rf test	$125
MSC 88002	40	45	15.4	Visual; automatic dc probe many parameters; rf test; IR scan	$130
NEC 868196	60	77	9.8	Visual; dc probe; rf test	$130

devices (all except MSC) the liquid crystal measurement technique was used for the estimate. Most manufacturers who measure thermal resistance use an infrared microscope, but the resolution of such a microscope is only ~ 25 μm (36X objective), and the temperature of a GaAs FET changes by a large amount over 25 μm . The infrared microscope therefore only gives an average thermal resistance over a rather large area. This is satisfactory for comparing devices of similar structures and discovering poorly mounted devices, but not useful as a means of determining the actual channel temperature required in a reliability study. The liquid crystal technique involves placing a thin layer of liquid crystal of known isotropic temperature on top of the chip and applying bias. If the chip is illuminated with polarized light and observed with a correctly oriented polarizer in the reflected light path, any portion of the chip that exceeds that isotropic temperature will become dark. Liquid crystal isotropic temperatures are accurate to better than 1°C and with 375X magnification, the resolution is ~ 1 μm. It is actually possible to see the liquid crystal begin to turn dark in a thin line at the drain edge of the gate stripes. For all of the upright devices the infrared microscope gave a thermal resistance about 65% of that measured by the liquid crystal technique. The results for the individual manufacturers are discussed below.

1. TI Devices

The thermal resistance of a large number of TI production devices was measured by the liquid crystal technique. Several devices had thermal resistances of about 45°C/W, while others ranged up to 75°C/W. The reason for this variation can be seen by examining several plots of temperature as a function of position obtained from an infrared microscope. A device having a thermal resistance to the hottest point of 45°C/W (liquid crystal) was scanned with an infrared microscope. A plot of temperature as a function of position is shown in Figure 11 for 5 V drain bias, 120 mA drain current, and a heat sink at 28°C. Examination of the device photograph in Figure 2 shows that each peak in Figure 11 corresponds to two gate fingers and the drain finger between them; the infrared microscope does not resolve the individual fingers, but only gives an average. The thermal resistance derived from the hottest

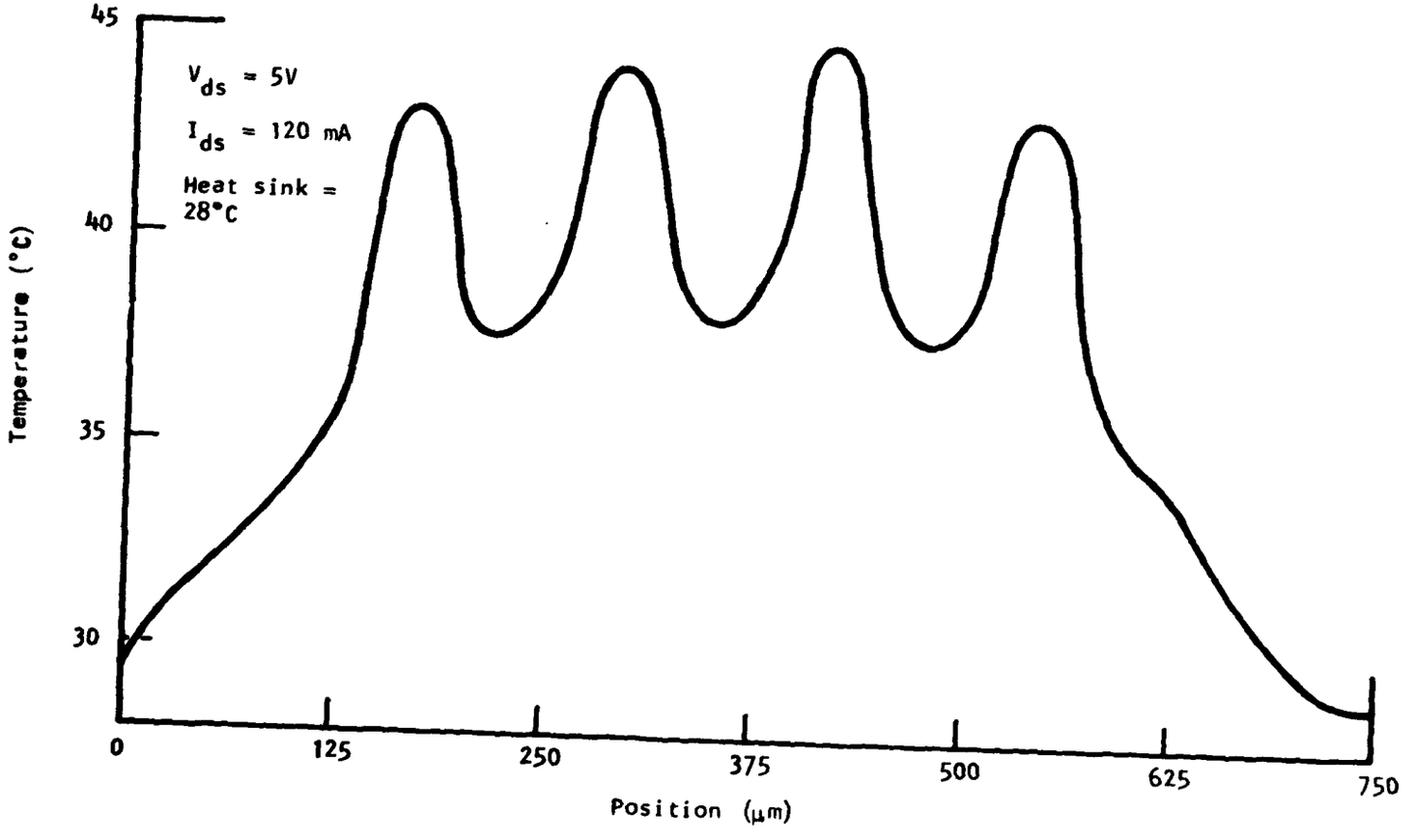


Figure 11 Temperature Distribution of TI MSX802 Device Determined by Infrared Microscope

point of Figure 11 is 28.2°C/W. Figure 11 indicates that the chip is well mounted, since the temperature peaks are nearly the same height, and the center peaks are slightly higher than the end. This may be compared with Figure 12, a temperature profile of an MSX802 chip where the liquid crystal indicating a thermal resistance to the hottest point of 55°C/W. This chip has an uneven temperature distribution, indicating a poor solder joint on one side. Almost every MSX802 device with a thermal resistance higher than the 45°C/W range had such an asymmetric temperature distribution, indicating that those chips were not well mounted. Measurements on TI laboratory devices gave essentially the same results.

2. Dexcel 3615A-P100F

One Dexcel package was opened and the device thermal resistance measured. The liquid crystal gave 41°C/W and the infrared microscope gave the plot of temperature as a function of position shown in Figure 13. The thermal resistance to the hottest point derived from Figure 13 is 26.5°C/W. It is just barely possible to resolve the more widely spaced gates (45 μm rather than the 30 μm of the TI devices). The asymmetrical temperature distribution is an indication of nonoptimum mounting. Based on the TI results for well-mounted chips, the liquid crystal method would give a thermal resistance of 30 to 35°C/W for well-mounted Dexcel chips. The thermal resistance to the hottest point derived from Figure 13 is 26.5°C/W.

3. NEC 868196

One NEC package was opened and the device thermal resistance measured. The liquid crystal indicated 77°C/W, and the infrared microscope gave the plot of tempepature as a function of position shown in Figure 14. The temperature dip in the center is due to the large center drain pad (see Figure 5). It is not known why the left side consists of two peaks instead of one, since the gates are so close they cannot be resolved. The thermal resistance to the hottest point obtained from Figure 14 is 51°C/W. The extreme

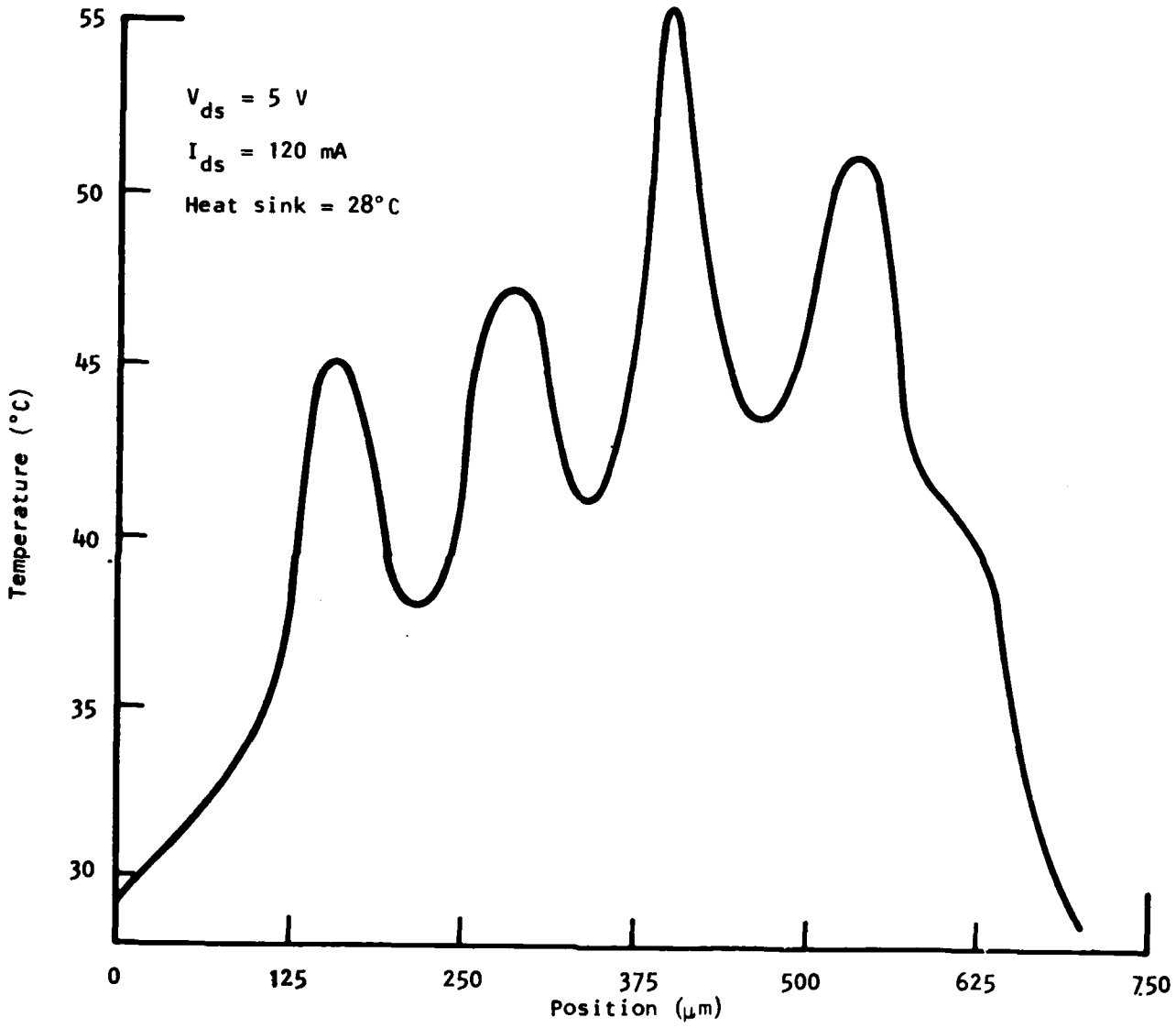


Figure 12 Temperature Distribution of TI MSX802 Device Determined by Infrared Microscope

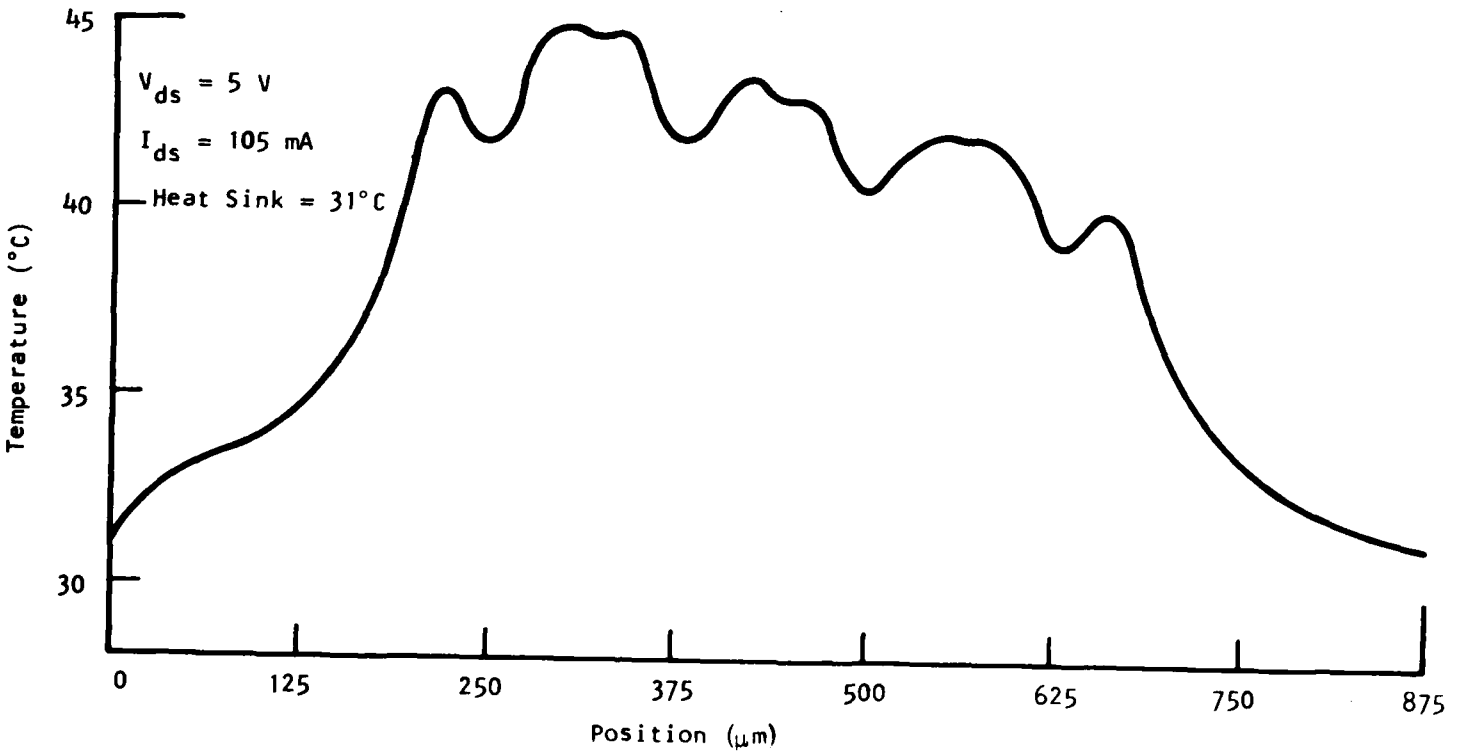


Figure 13 Temperature Distribution for Dexcel 3615A Device Determined by Infrared Microscope

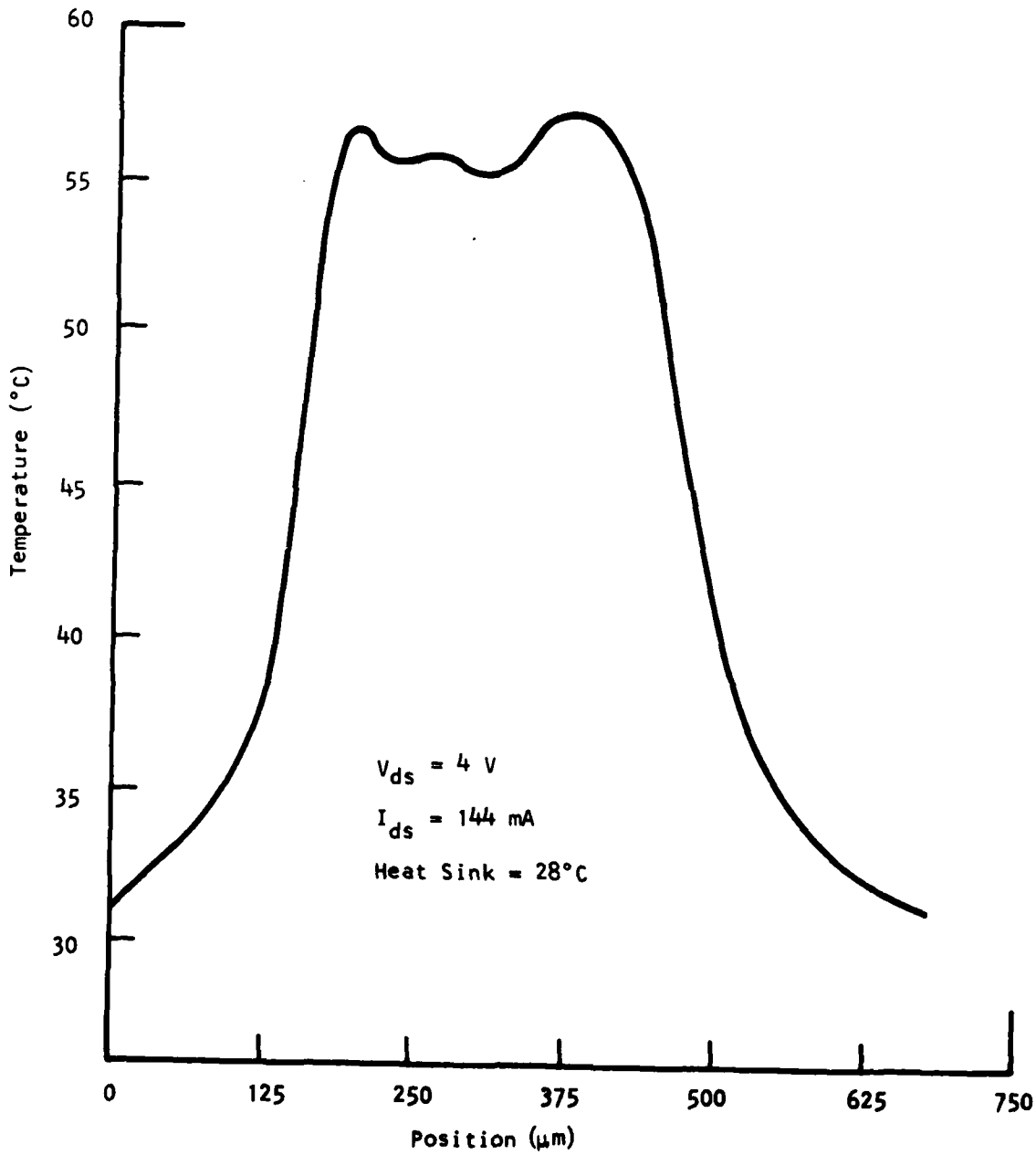


Figure 14 Temperature Distribution of NEC 868196 Device Determined by Infrared Microscope

closeness of the gates is responsible for the higher thermal resistance of the NEC devices than that observed with well-mounted chips from the other manufacturers.

4. MSC 88002

It is difficult to determine the thermal resistance of the MSC devices, since they are flipped and the active area is inaccessible. Liquid crystal applied to the top surface (chip back) indicated a thermal resistance of 23 °C/W. The infrared microscope gave 25 °C/W and indicated very little (<1°C) variation in temperature. Since the gate spacing is similar to that of the TI device, the temperature variation should be somewhat similar. Consequently, the infrared microscope, though good for finding poorly mounted devices, does not give a good indication of actual channel temperature. An electrical technique was therefore devised that is thought to be more accurate. The gate Schottky barrier forward voltage at a given current decreases with increasing temperature. By determining this temperature dependence at a fixed current, pulse techniques can be used to determine device temperature from measured gate forward voltage at that current level. The device is operated under normal conditions for a time long enough to reach thermal equilibrium (a few milliseconds) without heating the package. The device is then turned off, the gate is pulsed to the fixed current level, and the voltage is measured. Operation of pulsed devices indicates that the channel temperature changes in 1 μs or less, so it would be necessary to sample the gate voltage within that time to accurately measure the channel temperature. The present set-up can only attain 4 μs after drain turn-off, but for a given device structure gives data from which actual thermal resistance can be derived. In Figure 15 the thermal resistance measured 4 μs after drain turn-off is plotted as a function of thermal resistance of a number of TI MSX802 devices measured by the liquid crystal technique (assumed accurate). There is a constant 25°C/W offset; i.e., an MSX802 device with 45°C/W would give 20 °C/W by the pulsed technique. Since the MSC device geometry is very similar to the TI MSX802, Figure 15 was used to determine the thermal resistance of MSC 88002 devices. Three such devices gave about 20 °C/W,

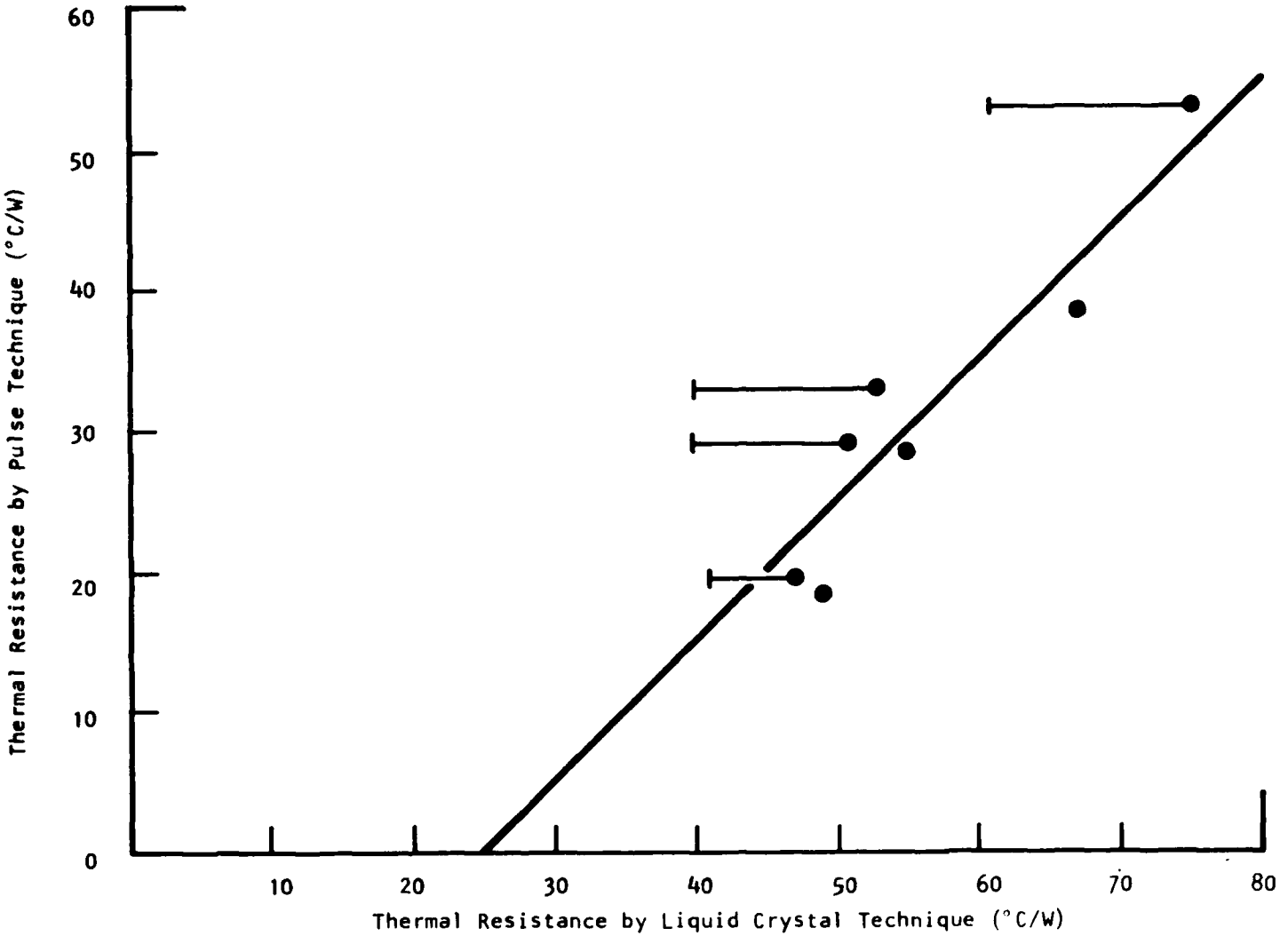


Figure 15 Thermal Resistance of MSX802 Devices Measured by Pulse Technique Compared with Liquid Crystal Technique Measurements

so it was concluded that their actual thermal resistance is ~45°C/W. A number of assumptions must be made in using this technique, but it is believed to give the best estimate of the temperature of the MSC devices.

5. Device Thermal Resistance at Elevated Temperatures

In order to conduct the environmental stress tests most effectively, it is necessary to determine the channel temperature at elevated heat sink temperatures. It is not sufficient to use the known dissipated power and the thermal resistance measured with a room temperature heat sink, since the device thermal resistance increases with temperature due to the reduction in the thermal conductivity of GaAs with increasing temperature. Since the liquid crystal cannot be used at elevated temperatures, the infrared microscope was focused on the hottest spot of each device type and the temperature measured as a function of heat sink temperature. This gives the fractional increase in device thermal resistance with temperature which is used to correct the liquid crystal thermal resistances for higher heat sink temperatures. The thermal resistance measured by infrared microscope as a function of heat sink temperature is plotted for four of the device types in Figure 16. The MSC device is not included because with the flipped structure the measured temperature is not related to the actual temperature in the same way it is with the other devices. The number beside each device type indicates the increase in thermal resistance per °C temperature rise of the heat sink as a percentage of the thermal resistance with a room temperature heat sink. This may be compared with the measured decrease in thermal conductivity of GaAs of ~ 0.3%/°C temperature rise.[1] Calculations show that a given percentage change in GaAs thermal conductivity will cause a somewhat larger change in device thermal resistance. Since the data of Figure 16 are scattered and the measurements are difficult, with a poorly defined relation between the measured (infrared microscope) and actual thermal resistance, it was decided to use an average value of 0.4% increase in thermal resistance per °C temperature rise above room temperature for all devices.

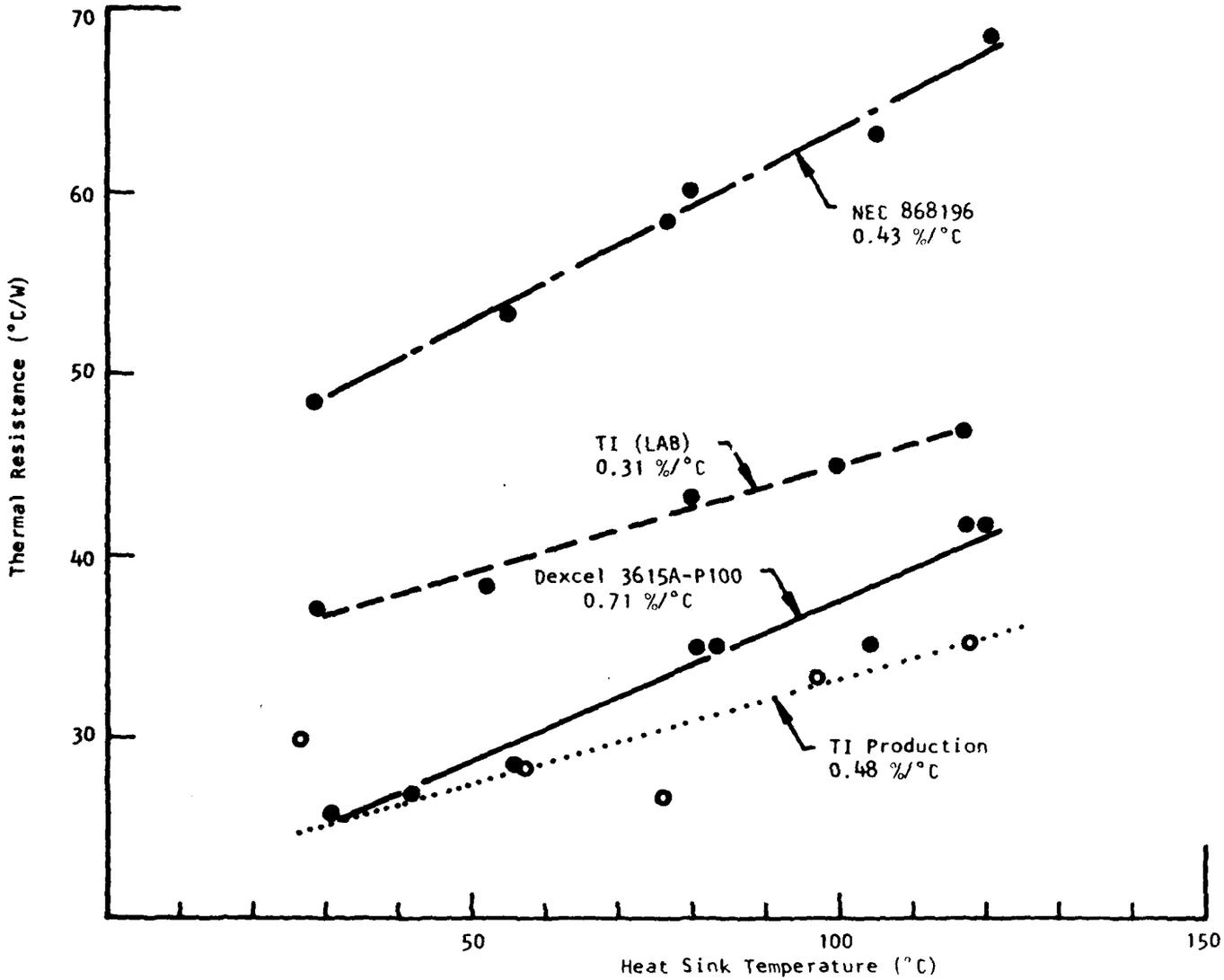


Figure 16 Device Thermal Resistance as a Function of Heat Sink Temperature Determined by Infrared Microscope

SECTION III
ELECTRICAL CHARACTERIZATION

The purpose of these measurements is to establish the long-term stability of GaAs power FETs under normal operating conditions. A number of electrical measurements are made, the devices are operated for 1000 hours under normal operating conditions, and the measurements are repeated. The operating conditions are 8 V drain bias and 20 dBm input power at 8 GHz. Impedance matching circuits are required for each device, as described in Section V.B. The 1000-hour test setup for the amplifiers is the same as described in Section V.A for the elevated temperature stress, except that the heat sink to which the amplifiers are connected is water-cooled and open to the air rather than heated and insulated. In addition, all these devices were driven with GaAs power FET oscillators rather than a Klystron.

A. Measurement Procedures

The measurements of small signal S-parameters, gain, 3 dB bandwidth, and phase linearity were performed using a Hewlett-Packard 9825A calculator-controlled automatic S-parameter measuring setup. These records are kept on a disk, and the measurements can be retrieved at any time. The S-parameters were measured on the total amplifier, not just the devices, since moving the devices from their amplifier circuits to a 50 ohm line set-up and back again would require many bonding and unbonding operations, which would cause undue stress on the devices and circuits. In addition, the devices, would not be mounted in exactly the same place or in exactly the same manner before and after the 1000 hour test.

Rf input, output, and input return power are measured with rf wattmeters connected into the X-band test setup with directional couplers. On the 1000-hour test setup the output power is monitored by having the amplifiers terminated into 50 ohm characteristic impedance power monitors, which are

calibrated to deliver 50 mV for 27 dBm of power output from the amplifiers. This small signal voltage is fed to a 24-channel strip chart recorder whose full-scale deflection is 50 mV.

Noise figure measurements were performed using an AIL automatic noise figure meter. The measurement frequency of the AIL noise figure meter is 30 MHz. Therefore, a Gunn diode oscillator is tuned 30 MHz away from 8 GHz. The two signals are fed to a mixer and then into a 40 dB gain, low noise 30 MHz amplifier before going to the noise figure meter.

Third-order intermodulation measurements were conducted by feeding two oscillators, each followed with a TWT amplifier, into a hybrid T, where the power was combined. The two frequencies were 10 MHz apart. This power then was fed through a variable attenuator to the amplifier being tested, with the output monitored by a spectrum analyzer through a 20 dB directional coupler. By adjusting the variable attenuator, the total input power to the amplifier could be adjusted. The spectrum analyzer was adjusted so that the main signals were at the 0 dB reference level. the third-order intermodulation frequency power level could then be read out as so many dB below the two main signals.

B. Results

Initial measurements and 1000-hour operation have been conducted for all 16 amplifiers (four from each of the four manufacturers). The final measurements have been completed on the first eight, and no significant changes were found in any of the parameters. The output power monitored during the test of the second eight devices also did not change significantly, and little variation is expected in the final electrical measurements.

Data for a typical device, MSC 3J, before and after the 1000-hour test are included in the tables and figures that follow in this section. Similar data exist for each of the amplifiers tested, but these data were not included here due to the lack of significant changes and the large amount of data.

Table 5 is a computer printout of the gain, S-parameters, and deviation from phase linearity from the automatic network analyzer. Table 6 shows the same data after the 1000-hour test. The first two columns are the forward and reverse gain. The next eight are the magnitude and phase of S_{11}, S_{22}, S_{21}, and S_{12}, respectively. The last column is the phase linearity. The data are plotted in Figures 17 through 28. These figures are generated by the automatic network analyzer computer driving an X-Y plotter. They are best compared by superimposing the Before and After data. Figures 17 and 18 show the small signal gain plotted as a function of frequency before and after the 1000-hour test. Figures 19 and 20 are Smith Chart plots of S_{11} before and after the 1000-hour test; Figures 21 and 22 are Smith Chart plots of S_{22} before and after the 1000-hour test; Figures 23 and 24 are polar plots of S_{21} before and after the 1000-hour test; Figures 25 and 26 are polar plots of S_{12} before and after the 1000-hour test; Figures 27 and 28 are plots of the deviation from phase linearity as a function of frequency before and after the 1000-hour test.

The S-parameters at 8 GHz for all of the first eight devices before and after the 1000-hour test are recorded in Table 7. Also included are the small and large signal (20 dBm input power) gain at 8 GHz and the 3 dB bandwidth taken from the gain data. In no case did the gain change by as much as 1 dB, which would be regarded as significant. Some S-parameters of some of the devices appear to have significant changes after the 1000-hour test, but there are periodic variations in the S-parameters as a function of frequency due to electrical discontinuities. Studies of the plot of the S-parameters over the entire frequency range show no significant changes. It may be noted that the 3 dB bandwidth of one or two devices appears to change significantly; however, in those cases the 3 dB bandwidth was larger than the measurement frequency range and was therefore estimated, apparently not accurately.

S-Parameters of Device MSC 3J Before Test

20 MSC 3J;Vg=-2.6;RF IN=-13.5dBm;Id=194mA 05 14 09:39:4

FREQ MHz	GAIN FORWARD	GAIN REVERSE	REFL-MAG FORWARD	REFL-ANG FORWARD	REFL-MAG REVERSE	REFL-ANG REVERSE
30.000	-0.25	-23.70	0.889	-169.8	0.430	3.2
30.000	0.07	-23.17	0.864	-177.8	0.446	-7.5
7200.000	0.45	-22.21	0.831	174.3	0.464	-18.1
7300.000	1.16	-21.35	0.802	166.0	0.486	-29.2
7400.000	1.88	-20.82	0.767	157.3	0.500	-41.8
7500.000	2.57	-20.11	0.712	149.2	0.518	-55.6
7600.000	3.37	-19.22	0.647	141.1	0.531	-71.1
7700.000	4.47	-17.83	0.574	133.3	0.538	-89.9
7800.000	5.45	-16.64	0.471	128.0	0.518	-113.
7900.000	6.27	-16.19	0.350	129.9	0.469	-141.9
8000.000	6.65	-16.40	0.298	149.3	0.386	-176.2
8100.000	6.31	-16.79	0.392	-68.3	0.287	145.1
8200.000	5.18	-17.78	0.523	159.8	0.221	100.4
8300.000	3.73	-19.16	0.619	150.5	0.207	54.3
8400.000	1.99	-21.15	0.671	141.1	0.230	17.4
8500.000	0.42	-22.80	0.706	131.6	0.267	-8.0
8600.000	-1.15	-23.68	0.716	123.3	0.300	-26.6
8700.000	-2.41	-24.49	0.728	114.6	0.329	-41.5
8800.000	-3.59	-25.16	0.736	107.3	0.357	-53.8
8900.000	-4.84	-27.22	0.744	100.6	0.381	-64.0
9000.000	-6.21	-30.52	0.745	92.3	0.402	-73.7

File 20 MSC 3J;Vg=-2.6;RF IN=-13.5dBm;Id=194mA 05/14 09:39:47

FREQ MHz	TRAN-REAL FORWARD	TRAN-IMAG FORWARD	TRAN-REAL REVERSE	TRAN-IMAG REVERSE	D-PHASE FORWARD	FREQ MHz
7000.000	0.504	0.830	0.063	0.019	-15.7	7000.000
7100.000	0.704	0.722	0.069	0.007	-10.9	7100.000
7200.000	0.880	0.578	0.076	-0.014	-5.4	7200.000
7300.000	1.[illegible]	0.401	0.082	-0.025	-0.2	7300.000
7400.000	1.220	0.231	0.081	-0.041	7.8	7400.000
7500.000	1.343	-0.033	0.075	-0.065	13.6	7500.000
7600.000	1.397	-0.467	0.057	-0.093	14.4	7600.000
7700.000	1.357	-0.978	0.027	-0.126	15.0	7700.000
7800.000	1.126	-1.496	-0.008	-0.147	15.6	7800.000
7900.000	0.577	-1.976	-0.064	-0.141	12.8	7900.000
8000.000	-0.417	-2.108	-0.122	-0.090	3.2	8000.000
8100.000	-1.279	-1.623	-0.143	-0.021	-5.9	8100.000
8200.000	-1.633	-0.792	-0.125	0.031	-13.9	8200.000
8300.000	-1.523	-0.204	-0.100	0.047	-14.3	8300.000
8400.000	-1.244	0.185	-0.063	0.061	-12.5	8400.000
8500.000	-0.934	0.480	-0.036	0.063	-13.4	8500.000
8600.000	-0.621	0.618	-0.011	0.065	-13.1	8600.000
8700.000	-0.424	0.629	-0.004	0.059	-6.4	8700.000
8800.000	-0.284	0.597	0.004	0.055	3.0	8800.000
8900.000	-0.140	0.555	0.010	0.042	9.6	8900.000
9000.000	-0.031	0.488	0.021	0.022	16.9	9000.000

Reference Plane Position: (cm) 0.00 0.00
Transmission Length: 0.00 cm
Linearized from: 7000.000 to 9000.000
Electrical Length (cm): 14.90

Table 6

S-Parameters of Device MSC 3J After 1000-Hour Test

FREQ MHz	GAIN FORWARD	GAIN REVERSE	REFL-MAG FORWARD	REFL ANG FORWARD	REFL MAG REVERSE	REFL ANG REVERSE
[illegible]	-0.56	-23.20	0.902	-163.1	0.435	[illegible]
[illegible]000	0.08	-22.58	0.881	-170.9	0.447	4.[illegible]
7200.000	0.45	-22.09	0.856	-179.6	0.457	-15.6
7300.000	1.16	-21.34	0.818	173.3	0.484	-26.6
7400.000	1.98	-20.55	0.775	165.4	0.504	-39.0
7500.000	2.84	-19.58	0.720	157.0	0.528	-52.2
7600.000	3.61	-18.50	0.643	148.9	0.542	-[illegible]
7700.000	4.23	-17.25	0.548	141.3	0.5[illegible]	-67.1
7800.000	5.59	-16.32	0.437	137.5	0.541	110.1
7900.000	6.34	-15.75	0.332	145.2	0.[illegible]	-[illegible]
8000.000	6.49	-15.91	0.326	163.6	0.[illegible]	174.6
8100.000	5.82	-16.82	0.450	168.[illegible]	0.[illegible]	142.[illegible]
8200.000	4.58	-17.97	0.556	162.0	0.[illegible]	94.6
8300.000	3.11	-19.36	0.674	152.4	0.[illegible]	51.7
8400.000	1.59	-20.69	0.[illegible]	143.3	0.[illegible]	20.[illegible]
8500.000	0.09	-22.05	0.[illegible]	135.2	0.[illegible]	-2.1
8600.000	-1.14	-23.49	0.[illegible]	127.0	0.[illegible]	-18.[illegible]
8700.000	-2.30	-24.67	0.[illegible]	119.3	0.[illegible]	-32.[illegible]
8800.000	-3.50	-25.78	0.[illegible]	112.[illegible]	0.[illegible]	-43.5
8900.000	-4.57	-26.92	0.[illegible]	105.[illegible]	0.[illegible]	-52.4
9000.000	-5.40	-27.67	0.[illegible]	[illegible]	0.[illegible]	-62.[illegible]

File 55 MSC 3J: Vd=-2.0: Idss: RF IN=-15dBm 07 12 10:34:0[illegible]

FREQ MHz	TRAN-REAL FORWARD	TRAN-IMAG FORWARD	TRAN-REAL REVERSE	TRAN-IMAG REVERSE	D-PHASE FORWARD	FREQ MHz
000.000	0.506	0.787	0.066	0.020	-15.7	[illegible]000.000
7100.000	0.665	0.735	0.074	0.008	-6.8	7100.000
7200.000	0.843	0.632	0.078	-0.009	0.4	7200.000
7300.000	1.059	0.430	0.081	-0.027	5.9	7300.000
7400.000	1.247	0.141	0.061	-0.047	6.6	7400.000
7500.000	1.372	-0.199	0.075	-0.074	10.1	7500.000
7600.000	1.382	-0.622	0.056	-0.105	12.4	7600.000
7700.000	1.241	-1.168	0.026	-0.135	11.6	7700.000
7800.000	0.895	-1.680	-0.018	-0.152	11.2	7800.000
7900.000	0.227	-2.063	-0.083	-0.140	7.7	7900.000
8000.000	-0.755	-1.971	-0.136	-0.085	-1.3	8000.000
8100.000	-1.427	-1.337	-0.142	-0.024	-9.0	8100.000
8200.000	-1.557	-0.642	-0.124	0.023	-11.4	8200.000
8300.000	-1.428	-0.071	-0.094	0.052	-12.7	8300.000
8400.000	-1.161	0.305	-0.067	0.063	-12.0	8400.000
8500.000	-0.872	0.511	-0.040	0.068	-9.5	8500.000
8600.000	-0.594	0.646	-0.015	0.065	-8.2	8600.000
8700.000	-0.343	0.687	0.003	0.058	-6.0	8700.000
8800.000	-0.170	0.646	0.011	0.050	0.4	8800.000
8900.000	-0.063	0.587	0.017	0.042	10.1	8900.000
9000.000	0.039	0.535	0.022	0.035	18.0	9000.000

Reference Plane Position: (cm) 0.00 0.00
Transmission Length: 0.00 cm
Linearized from: 7000.000 to 9000.000
Electrical Length (cm): 15.20

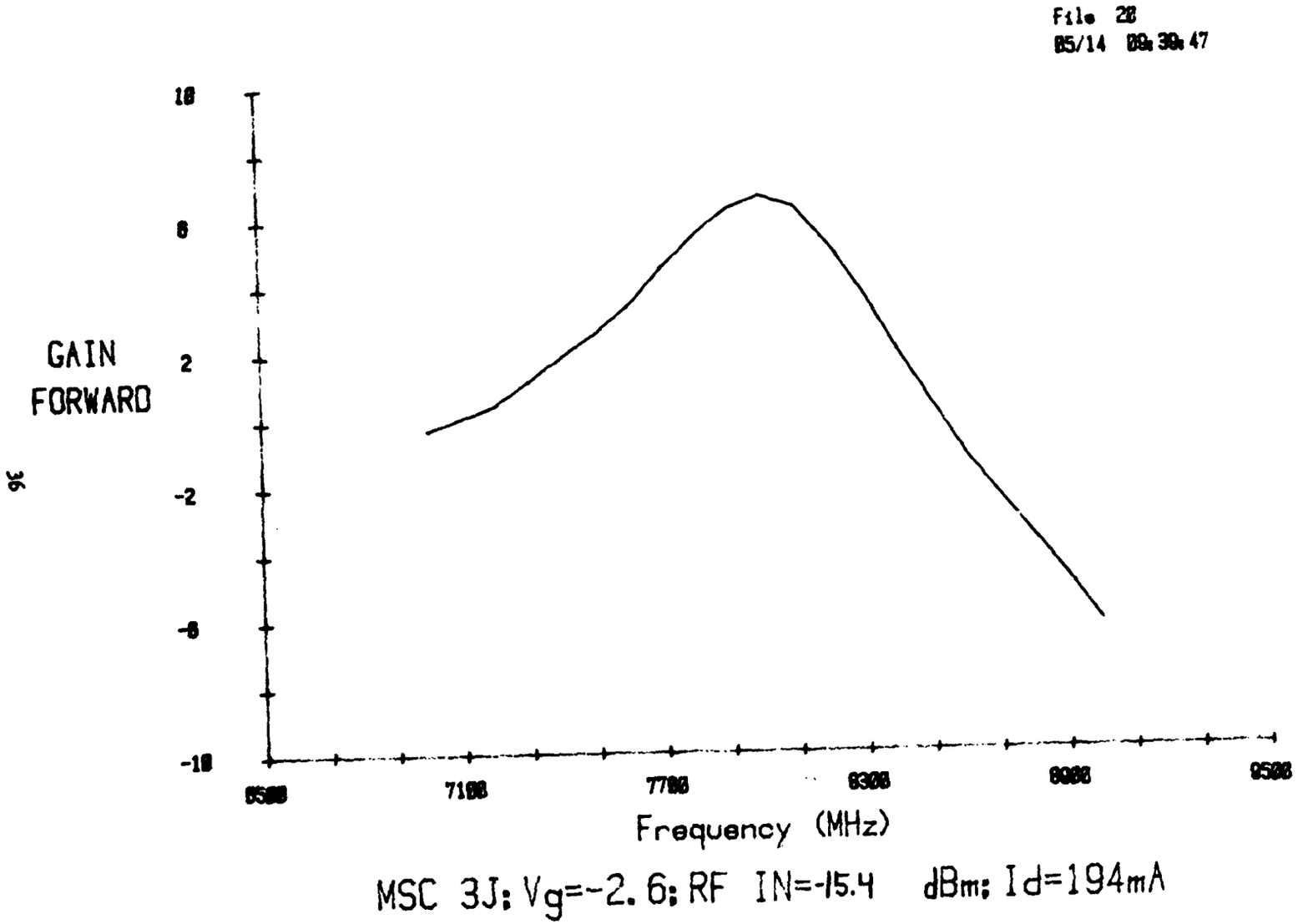


Figure 17 Small Signal Gain of MSC 3J Before 1000-Hour Test

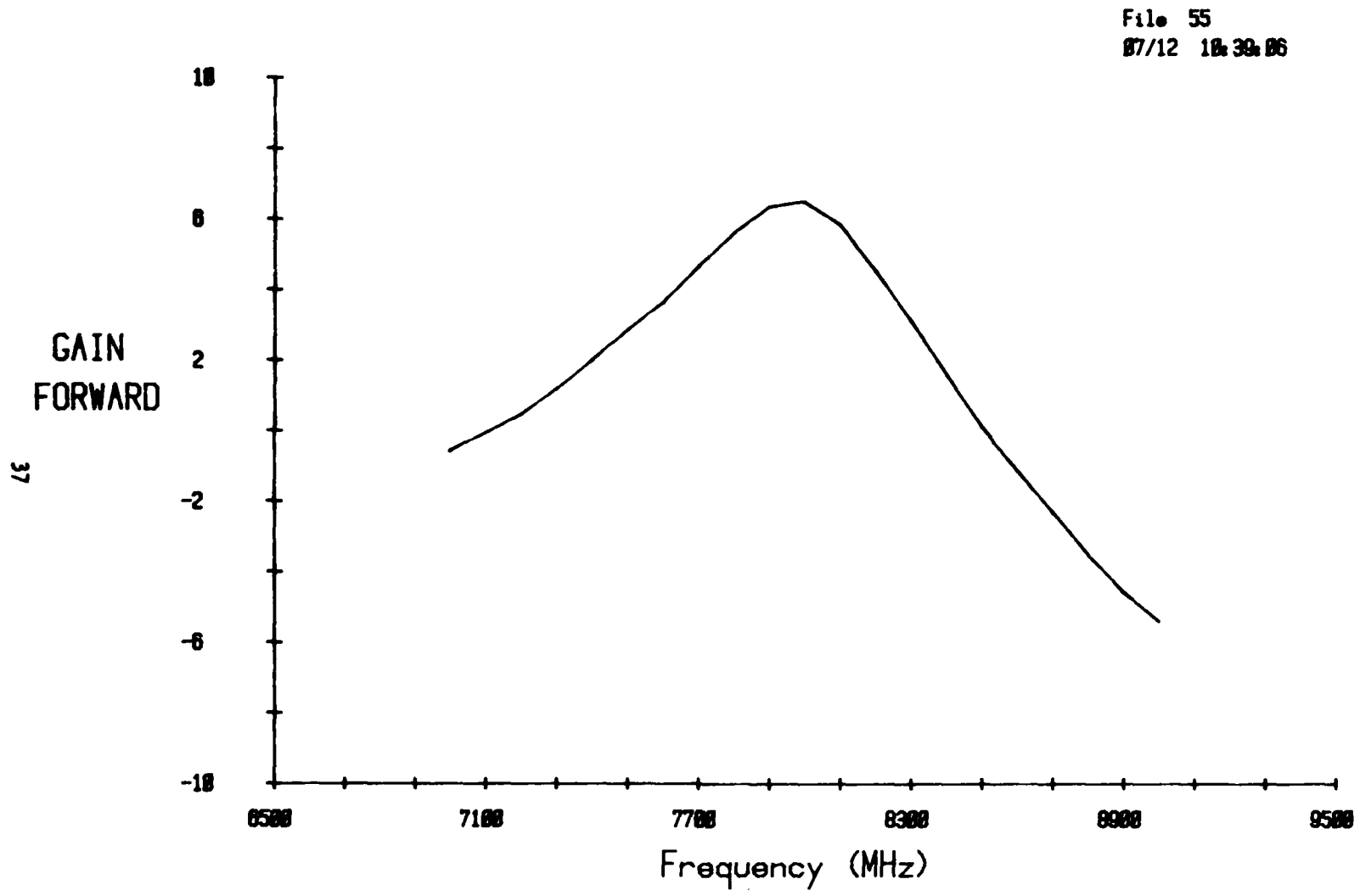


Figure 18 Small Signal Gain of MSC 3J After 1000-Hour Test

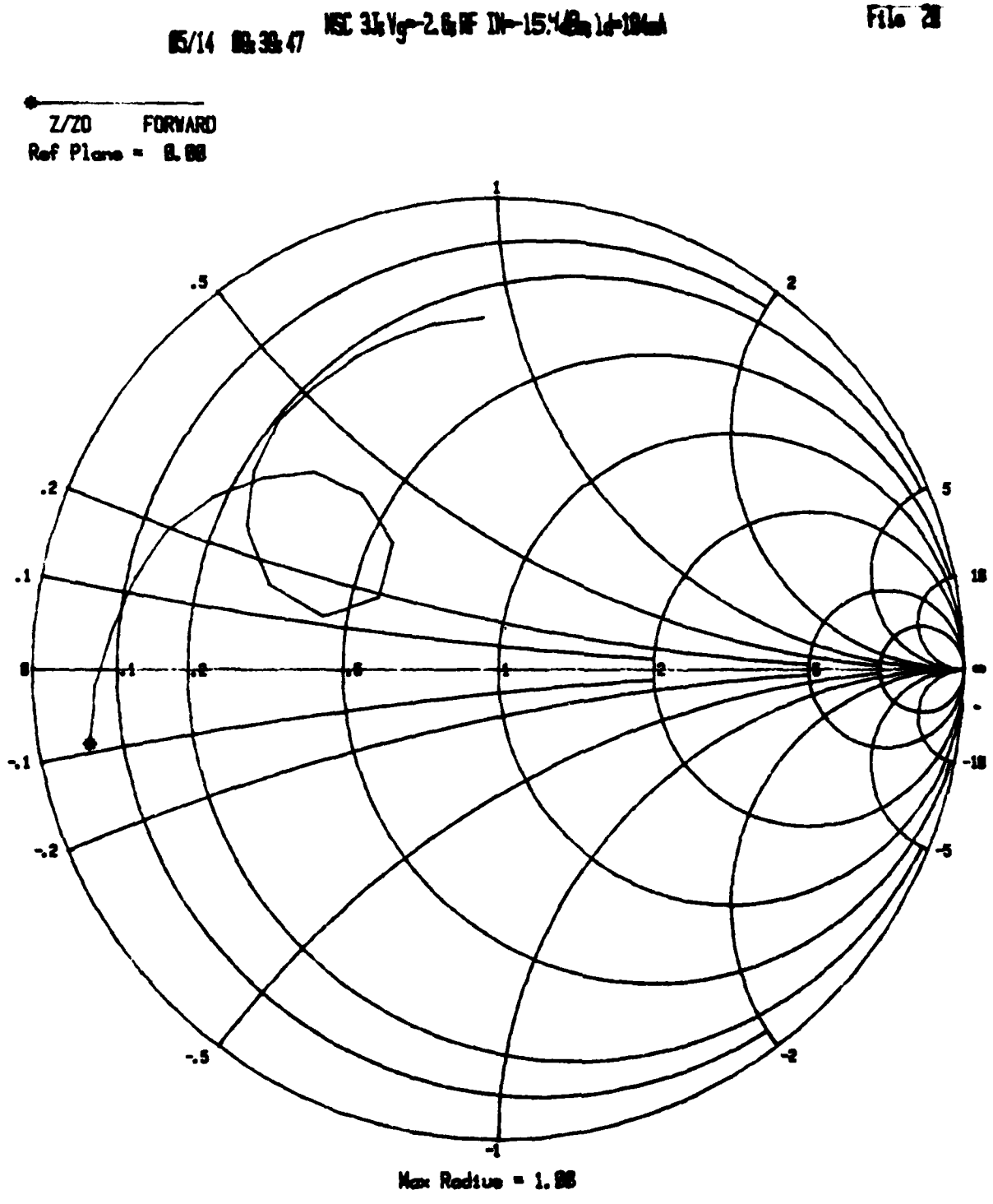


Figure 19 S_{11} Of MSC 3J Before 1000-Hour Test

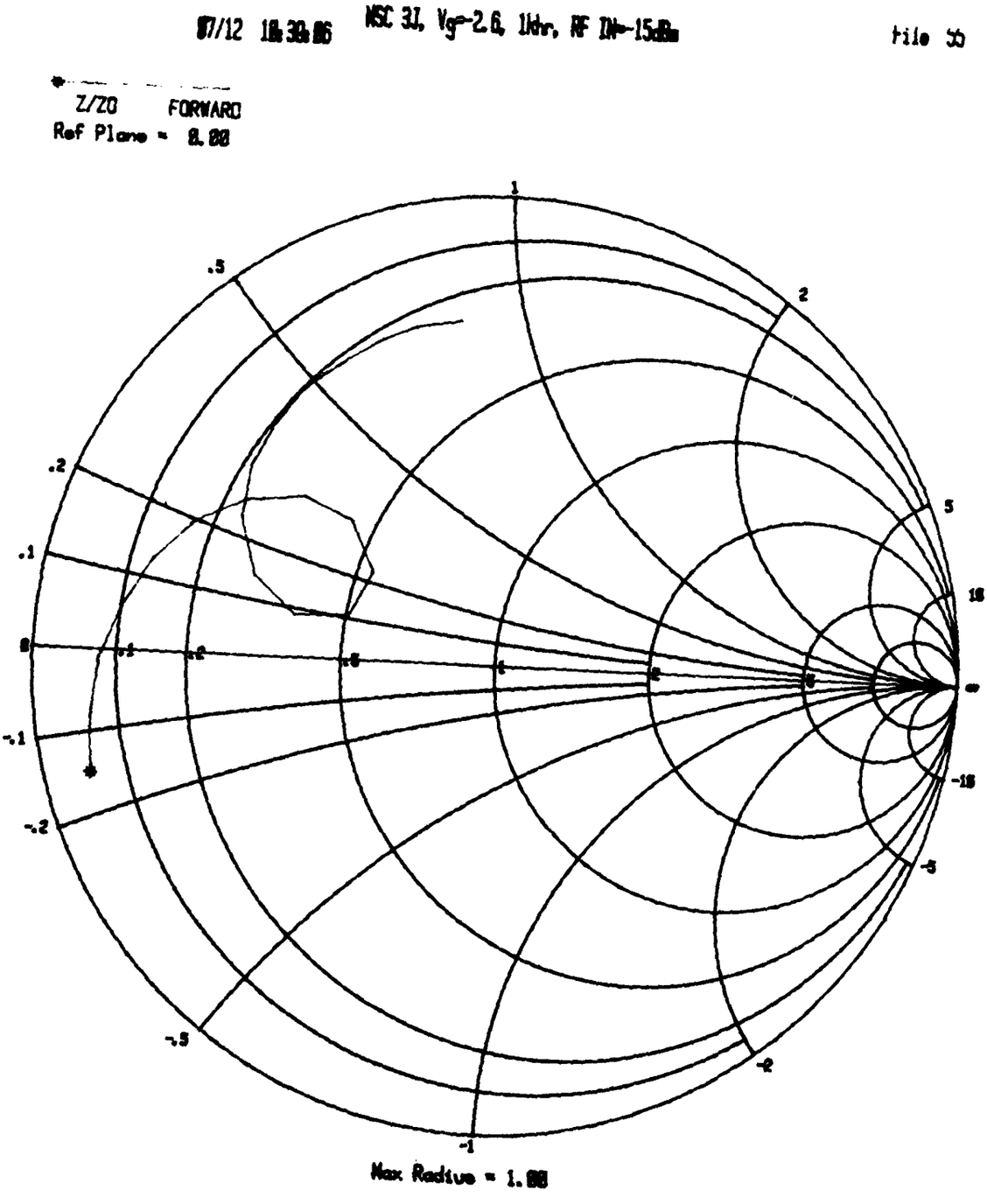


Figure 20 S_{11} Of MSC 3J After 1000-Hour Test

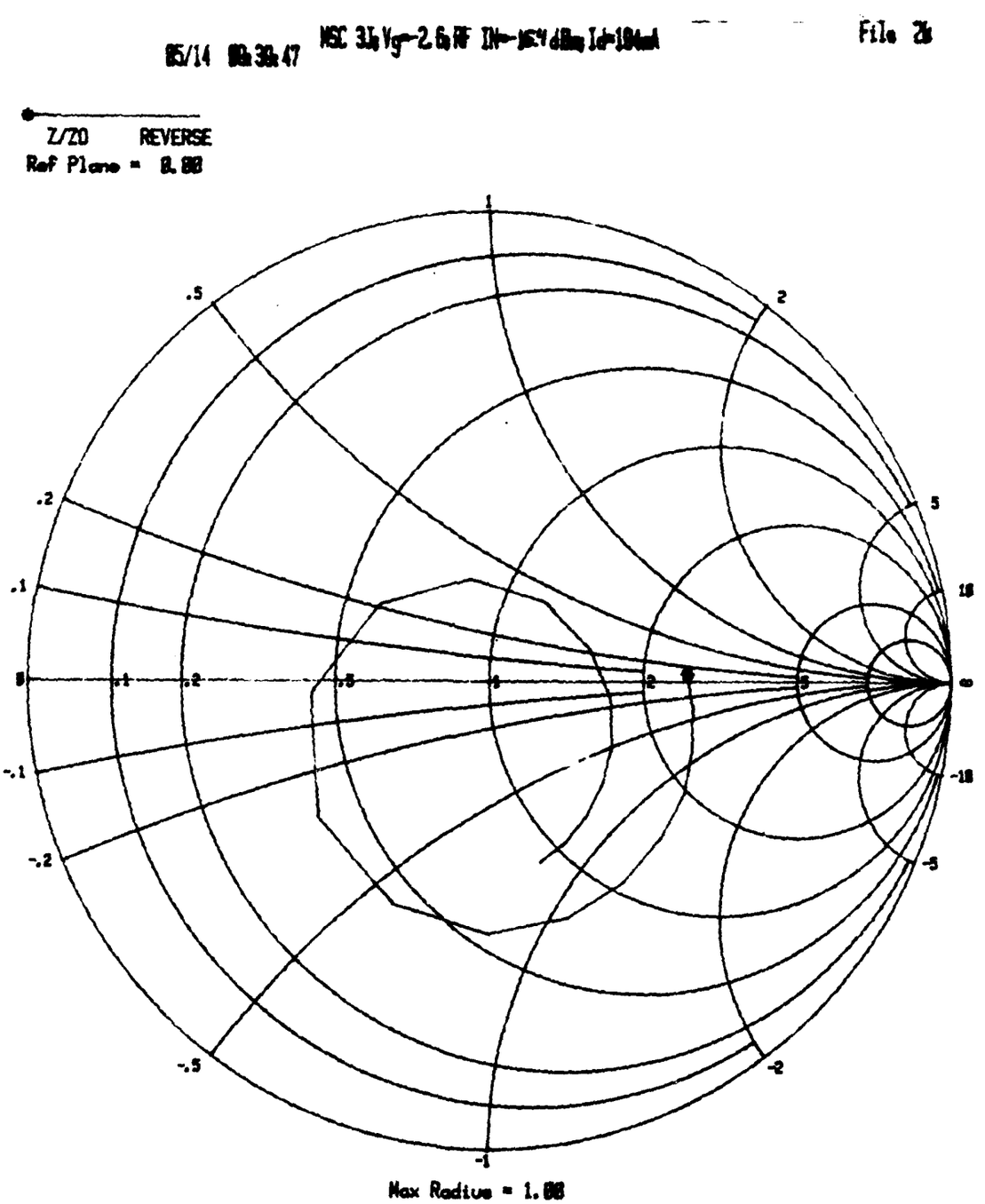
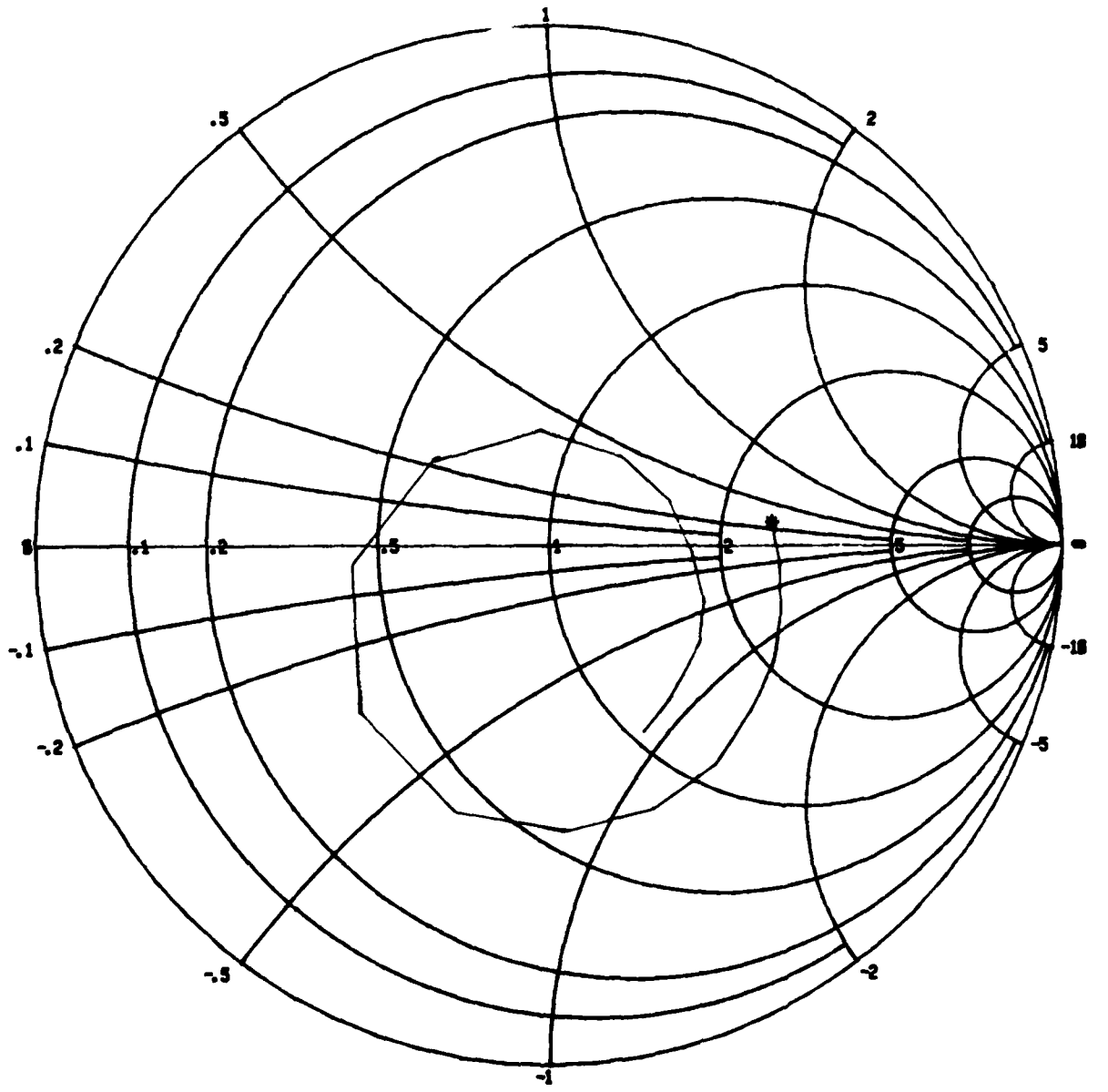


Figure 21 S_{22} Of MSC 3J Before 1000-Hour Test

87/12 18:39:06 MSC 3J, Vg=-2.6, 1Khr, RF IN=-15dBm File 55

Z/Z0 REVERSE
Ref Plane = 0.00



Max Radius = 1.00

Figure 22 S_{22} Of MSC 3J After 1000-Hour Test

05/14 09:39:47 MSC 3J; Vg=-2.6; RF IN=-15.4dBm Id=184mA

S21-R, I FORWARD
Trans Lin = 0.00

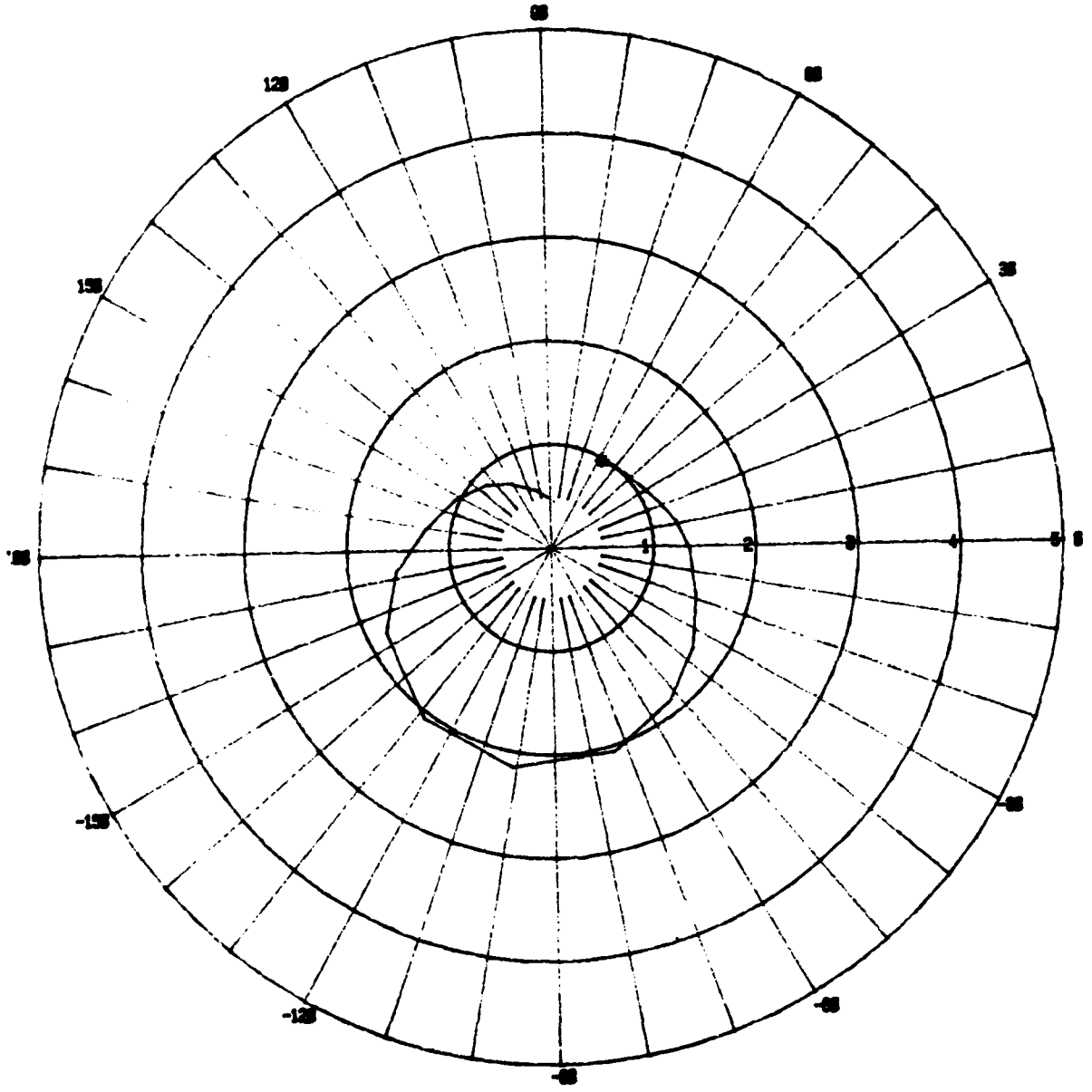


Figure 23 S_{21} Of MSC 3J Before 1000-Hour Test

07/12 16:39:06 MSC 3J, Vg=-2.6, 1Khr, RF IN=-15dBm File 55

S21-R, I FORWARD
Trans Lin = 0.00

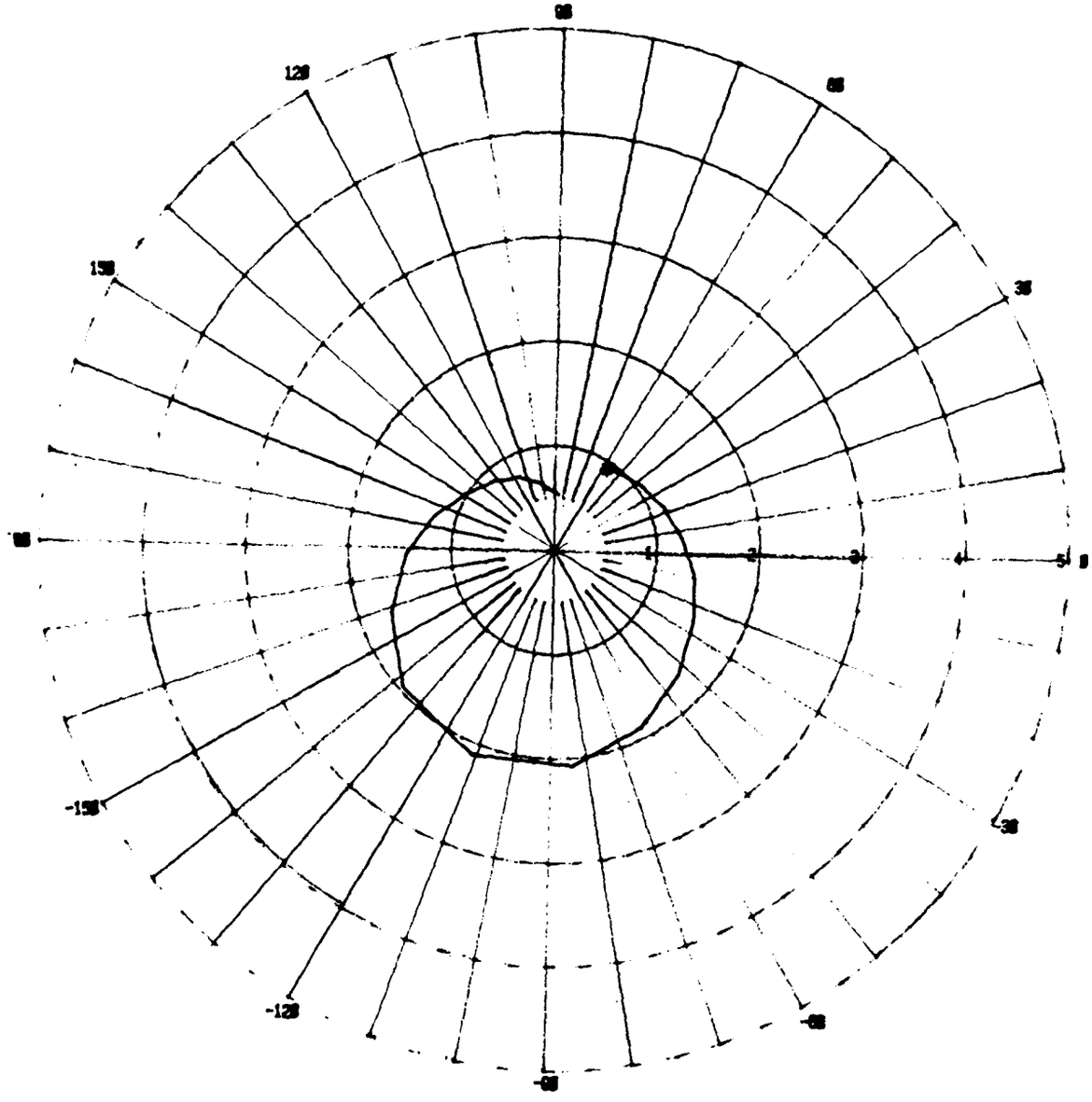


Figure 24 S_{21} Of MSC 3J After 1000-Hour Test

05/14 09:39:47 MSC 3J; Vg=-2.6; RF IN=-15.4dBm; Id=194mA File 2B

S21-R, I REVERSE
Trans Lin = 0.00

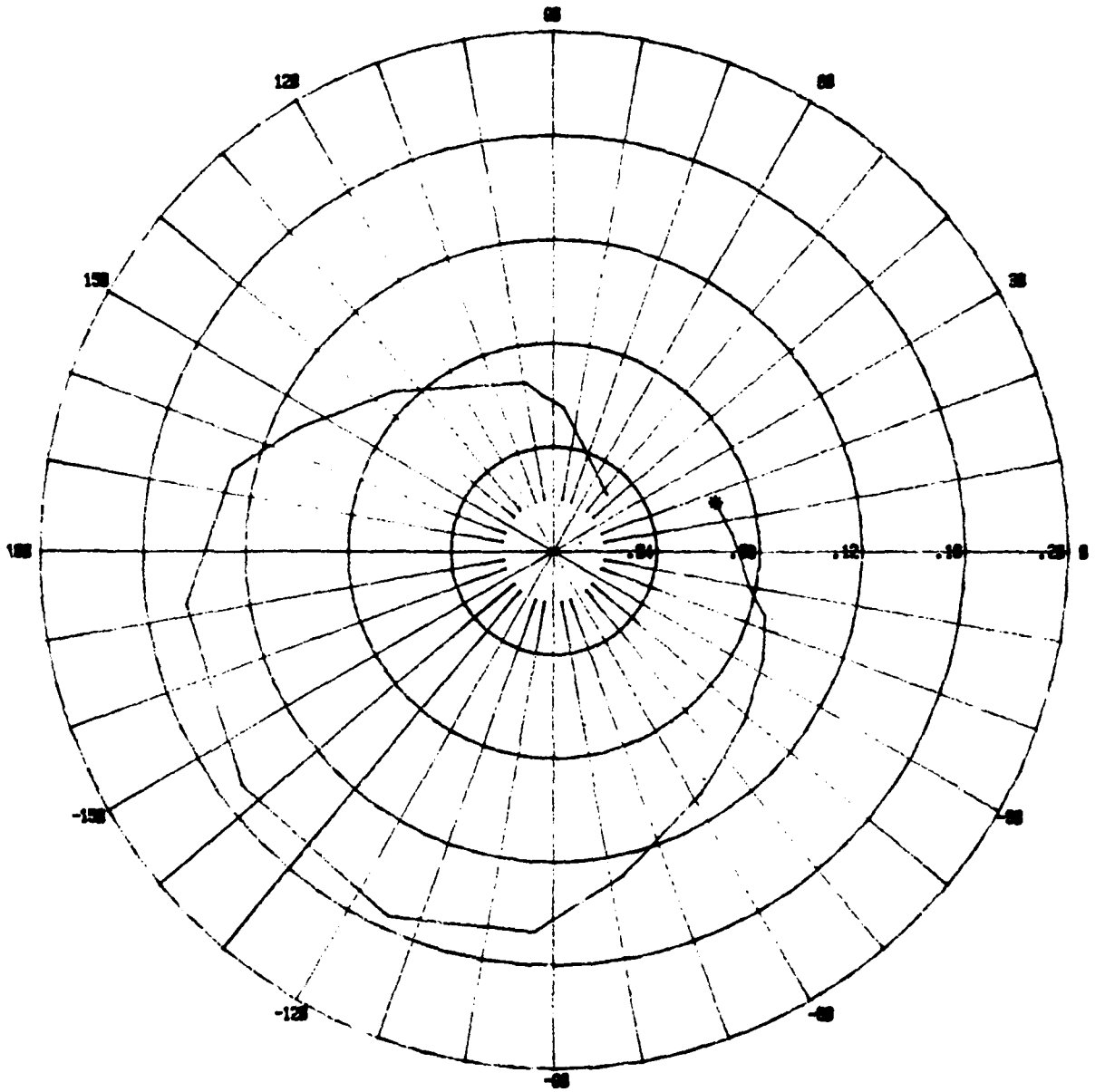


Figure 25 S_{12} Of MSC 3J Before 1000-Hour Test

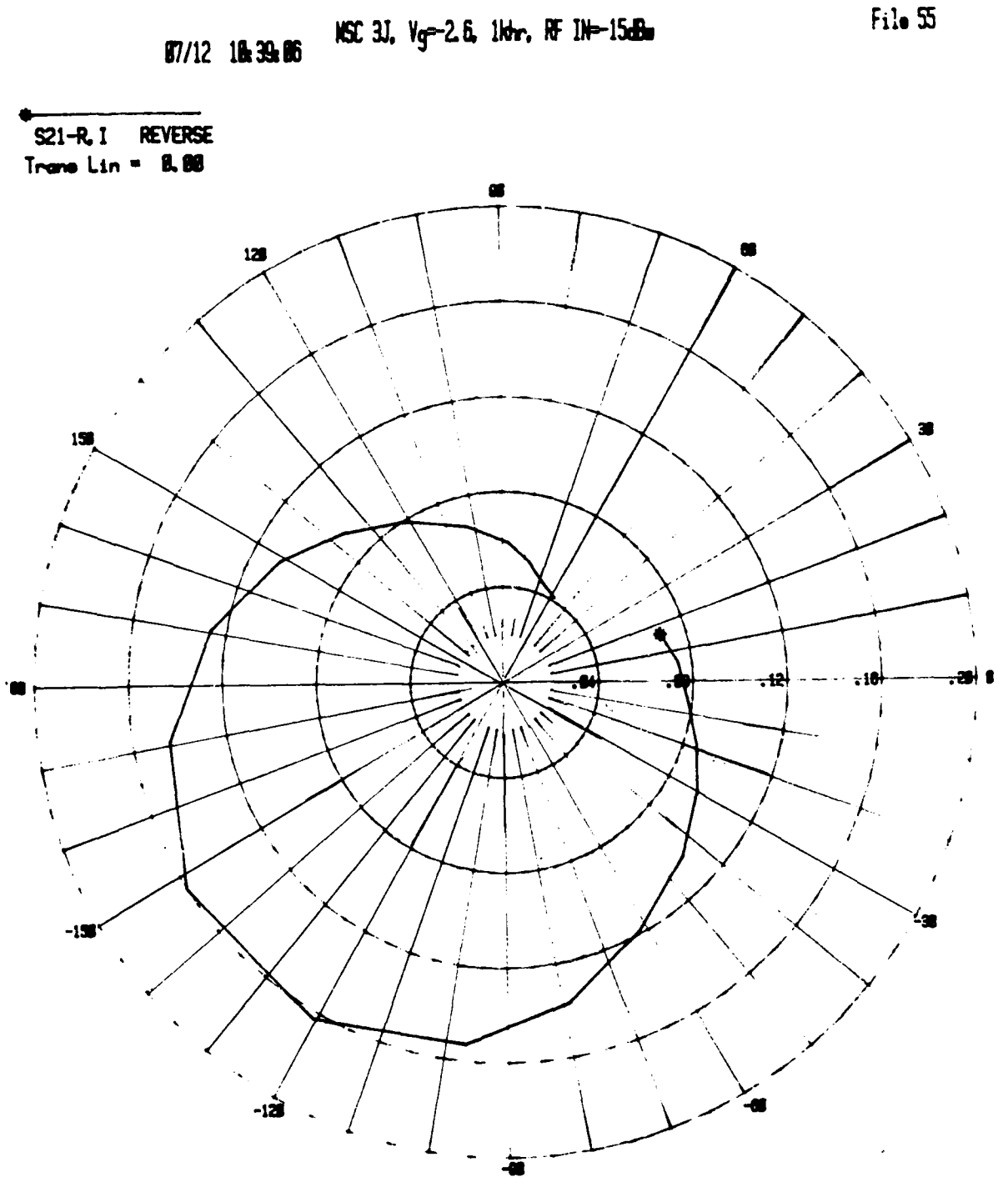


Figure 26 S_{12} Of MSC 3J After 1000-Hour Test

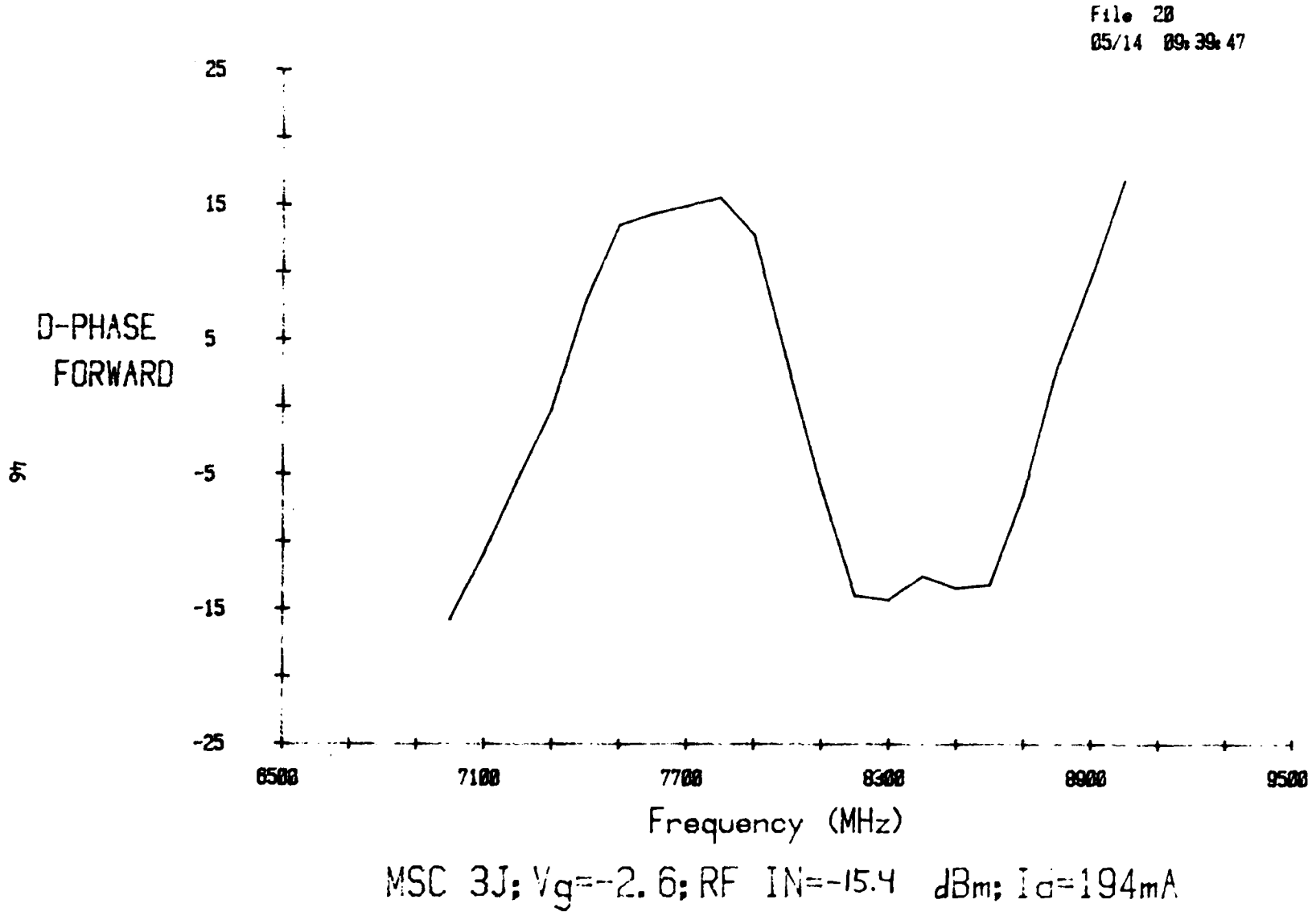


Figure 27 Phase Linearity Of MSC 3J Before 1000-Hour Test

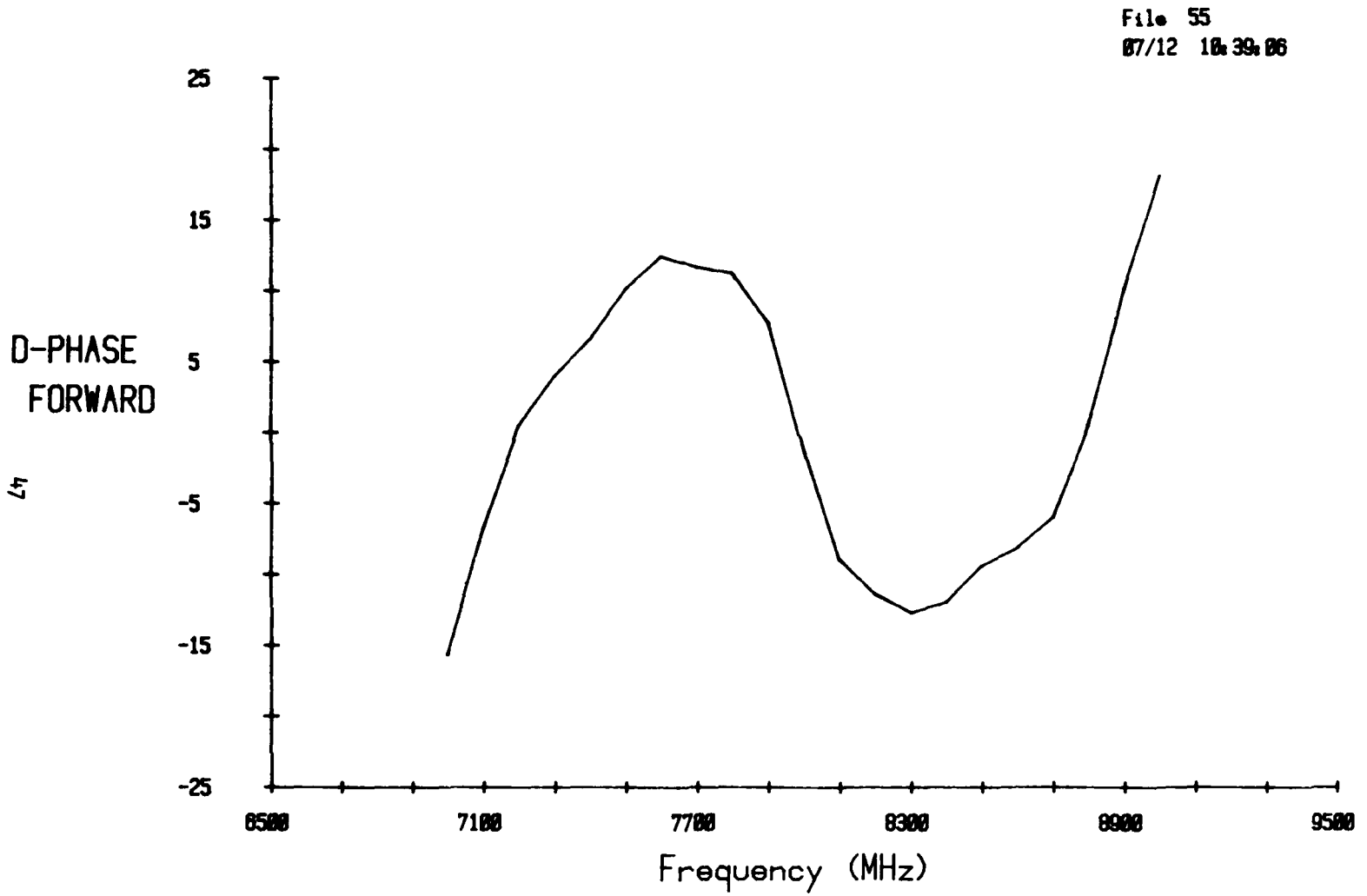


Figure 28 Phase Linearity of MSC 3J After 1000-Hour Test

Table 7

8 GHz Gain, S-Parameters, and 3 dB Gain Bandwidth for Eight Devices

Before and After 1000-Hour Room Temperature Operation

Device No.	Gain Large Signal (dB)		Gain, Small Signal (dB)		S_{11}				S_{22}				S_{21}				S_{12}				3 dB Bandwidth (MHz)	
	Before	After	Before	After	Before		After		Before		After		Before		After		Before		After		Before	After
					Mag.*	Ang.†	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.		
DXL 5	6.3	7.1	7.53	7.63	0.064	-44.6	0.118	-50.5	0.401	166.7	0.382	176.2	2.38	-108.0	2.41	-107.9	0.09	-123.2	0.10	-126.2	1389	1756
DXL 7	4.4	5.0	6.90	7.45	0.086	-102.8	0.140	-86.0	0.725	-178.7	0.763	-161.2	2.21	-118.2	2.36	-119.1	0.06	-113.3	0.06	-112.8	1205	1254
MSC 1J	6.8	7.0	7.42	8.08	0.067	-110.0	0.091	-97.8	0.203	167.0	0.333	168.2	2.35	-86.4	2.53	-84.6	0.19	-129.9	0.19	-130.6	1940	1263
MSC 2J	6.3	6.4	6.59	6.73	0.148	75.8	0.108	74.7	0.148	171.3	0.171	170.8	2.13	-77.1	2.17	-77.6	0.16	-120.6	0.17	-122.6	1399	1441
MSC 3J	6.9	7.0	6.65	6.49	0.298	149.3	0.336	163.6	0.386	145.1	0.386	-174.6	2.15	-101.2	2.11	-111.0	0.15	-143.6	0.16	-148.0	679	689
NEC 8	6.3	6.1	5.07	4.88	0.236	-174.6	0.238	175.0	0.585	129.2	0.680	134.4	1.79	146.8	1.75	141.4	0.09	-163.5	0.08	-99.2	1358	1473
NEC 18	5.2	5.2	6.21	5.92	0.231	150.5	0.246	143.7	0.572	130.2	0.644	136.1	2.04	159.3	1.98	156.5	0.09	-174.0	0.10	-163.9	1408	1426
NEC 21	5.7	-	7.03	-	0.329	158.8	-	-	0.377	153.4	-	-	2.25	168.8	-	-	0.10	-157.7	-	-	1071	-

*Mag. = Magnitude

†Ang. = Angle

The measured amplifier noise figures at 8 GHz before and after the 1000-hour test are given in Table 8, and the third order intermodulation data is given in Table 9. Here, the power of the intermodulation signal in dB below the two main signals is given at three different input signal levels. None of the devices described by Tables 7 through 9 is considered to have changed significantly in any of the parameters measured following the 1000-hour operations. NEC device No. 21 was accidentally destroyed and no data were taken after the 1000-hour operation. Similar data will be compared on the second batch of eight devices and results reported in the future.

Table 8

Noise Figures at 8 GHz Before and After 1000-Hour Room Temperature Operation for Eight Devices

Device No.		Noise Figure (dB) Before	After
DXL	5	8.93	8.91
	7	7.23	7.11
MSC	1J	7.06	7.03
	2J	6.90	7.07
	3J	10.42	10.67
NEC	8	9.14	9.56
	18	9.86	10.33
	21	7.91	-

Table 9

Intermodulation Distortion at 8 GHz Before and After 1000-Hour Operation of Eight Devices at Three Signal Levels

Device No.	IMD (-dBc) 20 dBm input each signal				IMD (-dBc) 17 dBm input each signal				IMD (-dBc) 14 dBm input each signal			
	Lower Side		Upper Side		Lower Side		Upper Side		Lower Side		Upper Side	
	Before	After	Before	After	Before	After	Before	After	Before	After	Before	After
OXL 5	16	13	15	13	18	16	18	16	26	25	26	25
7	15	12	15	12	17	14	16	13	19	15	18	14
MSC 1J	14	12	14	13	17	15	17	16	24	25	24	25
2J	15	13	16	13	19	18	19	17	30	29	30	29
3J	16	14	16	15	21	21	20	22	33	32	31	32
NEC 8	16	14	15	15	20	21	19	22	31	32	29	32
18	15	13	15	14	17	15	16	16	26	22	25	23
21	15	-	15	-	17	-	17	-	23	-	22	-

SECTION IV
ELECTRICAL STRESS TESTS

In each of the five tests, two devices from each manufacturer were stressed to failure to determine their capability to withstand the various stresses. All devices were mounted in a microwave test fixture to remove the heat during the tests and to prevent oscillation when the drain was biased. Steps were taken to prevent device destruction following failure. The stress voltage or current was increased in steps with 1 minute between steps to ensure stabilization at the new conditions. In almost all cases the devices failed as the stress level was being increased. The failure voltage and current recorded are the conditions at the current and voltage step just prior to failure. The tests and results are discussed below.

A. Maximum Drain Voltage

The device gates were grounded and the drain voltage increased in 1 V steps until the device failed. A 50 Ω resistor was put in series with the drain to reduce device destruction following failure. The results are summarized in Table 10. The drain voltage and drain current at failure, V_{ds} and I_{ds}, are noted, along with their product, which is the dissipated power at failure. In addition, the device dc characteristics taken from a curve tracer are also recorded, as they are for the devices in the other four electrical stress tests. I_{dss} is the saturated drain current at zero gate voltage, V_{sat} is the knee voltage at $V_g = 0$, g_m is the maximum transconductance (change in drain current between $V_g = 0$ and $V_g = -1$ V), and V_p is the pinch-off voltage. The TI devices are separated into production (P) and laboratory (L) categories. The major difference is that the production devices have nominal 2 μm gates and the laboratory devices have 1 μm gates.

Several conclusions can be drawn from the results in Table 10. The MSC devices failed at somewhat higher voltages than the others, and the Dexcel devices failed at considerably lower voltages. Discussions in the

Table 10

Maximum Drain Voltage ($V_g = 0$)

Manufacturer	Device Number	I_{dss} (mA)	V_{sat} (V)	$g_m (V_g = 0)$ (mmho)	V_p (V)	Failure Conditions		
						V_{ds} (V)	I_{ds} (mA)	$V_{ds} \times I_{ds}$ (W)
TI (P)	1	290	1.4	125	3	21	200	4.2
TI (P)	2	250	1.6	100	3.5	23	189	4.3
TI (L)	1	335	1.6	135	3	23	181	4.2
TI (L)	2	285	1.6	135	3	21	213	4.5
Dexcel	3	600	2.5	120	8	7	549	3.8
Dexcel	4	570	2.5	115	7.5	7	528	3.7
MSC	1	350	1.5	100	6.5	24	241	5.8
MSC	2	270	1.2	100	5	26	221	5.7
NEC	G35-34 #33	340	2.6	80	4.5	17	239	4.1
NEC	G3X-34 #1	370	2.8	70	6	13	239	3.1

literature[2,3] demonstrate that device failure under these conditions is due to avalanche injection of carriers into the substrate at the drain contact. The maximum drain voltage can therefore be increased by anything that reduces the electric field at the drain contact. This is done with n^+ contacts, gate recess, or the application of negative gate bias. The MSC devices are the only ones with n^+ contacts, and the data of Table 10 show that this is most effective in increasing the drain voltage capability, especially considering that the source-drain spacing of those devices is by far the smallest. The TI and NEC devices had a moderately high drain voltage capability due to their recessed gates; the wider recess of the NEC devices appeared to be somewhat less effective in this respect with $V_g = 0$. The Dexcel devices had low failure voltages, probably due to the lack of a gate recess. The gate length did not affect the maximum drain voltage, as indicated by the fact that the TI 2 μm gate and 1 μm gate devices were about the same.

It is possible to conclude from Table 10 that only the dissipated power causes failure when it reaches $\sim$4 W. If any low current Dexcel devices are available at the end of the program, stress tests will be performed to check this possibility.

In spite of the series resistor, many of the devices in all five stress tests underwent some melting following failure, which partially obscured the failure area. An example is shown in Figure 29, a photograph of TI production device No. 2 from the drain voltage ($V_g \approx 0$) stress test. Upon failure, the gate shorted to the drain through the GaAs. This caused a high current to flow between the gate and drain terminals, producing localized melting of the gate and surrounding GaAs. Previous experience indicates that if the 50 Ω resistor had not been present, the melting would have been much worse, covering a much larger area than included in the entire photograph of Figure 29. There appear to be some dark spots between the gate and drain near the melted area that could be holes in the GaAs. These are similar to published photographs of

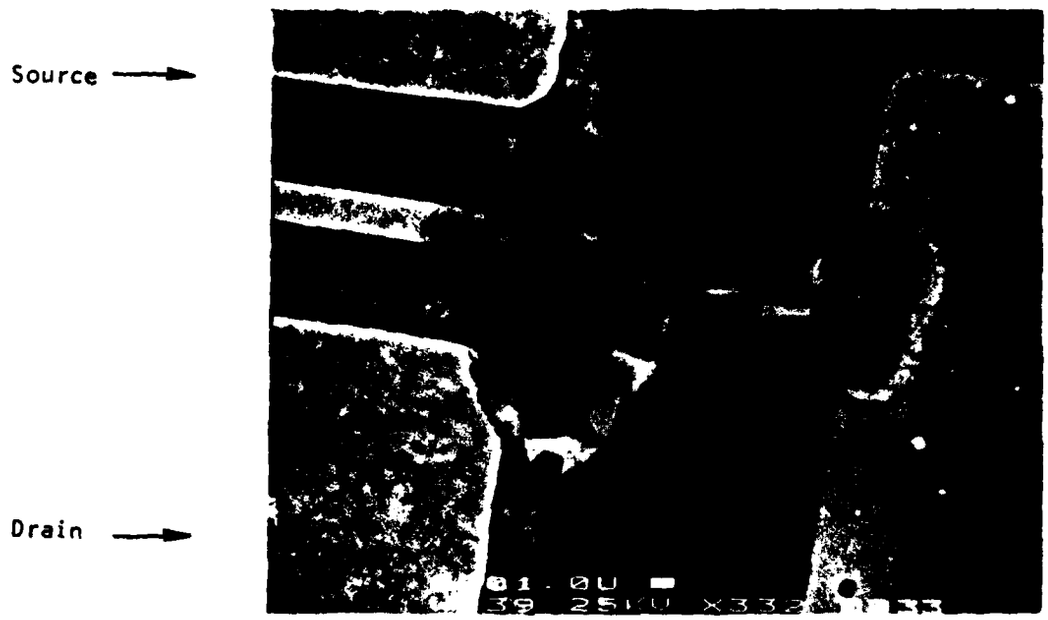


Figure 29 SEM Photograph of Failed TI (Production) Device No. 2

failed devices where the failure was attributed to avalanche injection of electrons into the substrate at the drain contact. Failed devices from other manufacturers had similar morphologies; MSC device active regions could not be observed due to the device structure.

During this test, the drain current was recorded for each drain voltage; the data are plotted in Figure 30. The bumps in the curves near threshold (V_{ds} = 2 to 3 V) were often accompanied by high frequency Gunn oscillations, but these disappeared at higher voltages and did not appear to affect the results.

B. Maximum Drain Voltage Under Operating Conditions

The devices in this test were tuned for maximum output power with 4 dB gain at 8 GHz and 8 V drain bias. The drain voltage was then increased in 1 V steps until failure occurred with a 50 Ω resistor in series with the drain to prevent device destruction. The impedances were rematched at each voltage level to maximize output power and minimize reflected power. In a change from the plan in TI's original proposal, the gate voltage and rf input power were held constant at higher drain voltages at the values employed at V_{ds} = 8 V.

The results are summarized in Table 11. In addition to the drain voltage and drain current at which failure occurred and the power dissipated, the gate voltage is also recorded. Under these conditions the NEC devices failed at the highest drain voltages and the Dexcel devices at the lowest. The MSC devices failed at about the same voltage as with V_g = 0, probably because the n^+ contacts reduce the electric field at the drain contact to such a level that there is no further improvement when negative gate bias is employed. The Dexcel devices still have the lowest drain voltage capability because they lack a gate recess; but again, lower current Dexcel devices should probably be checked for completeness. An unexpected result was that the TI devices failed at drain voltages the same as or lower than was the case with V_g = 0. Perhaps this is because the optimum gate voltage is so low and the value of I_{ds} is so high (60 to 70% of I_{dss}). To clarify this result, additional TI devices

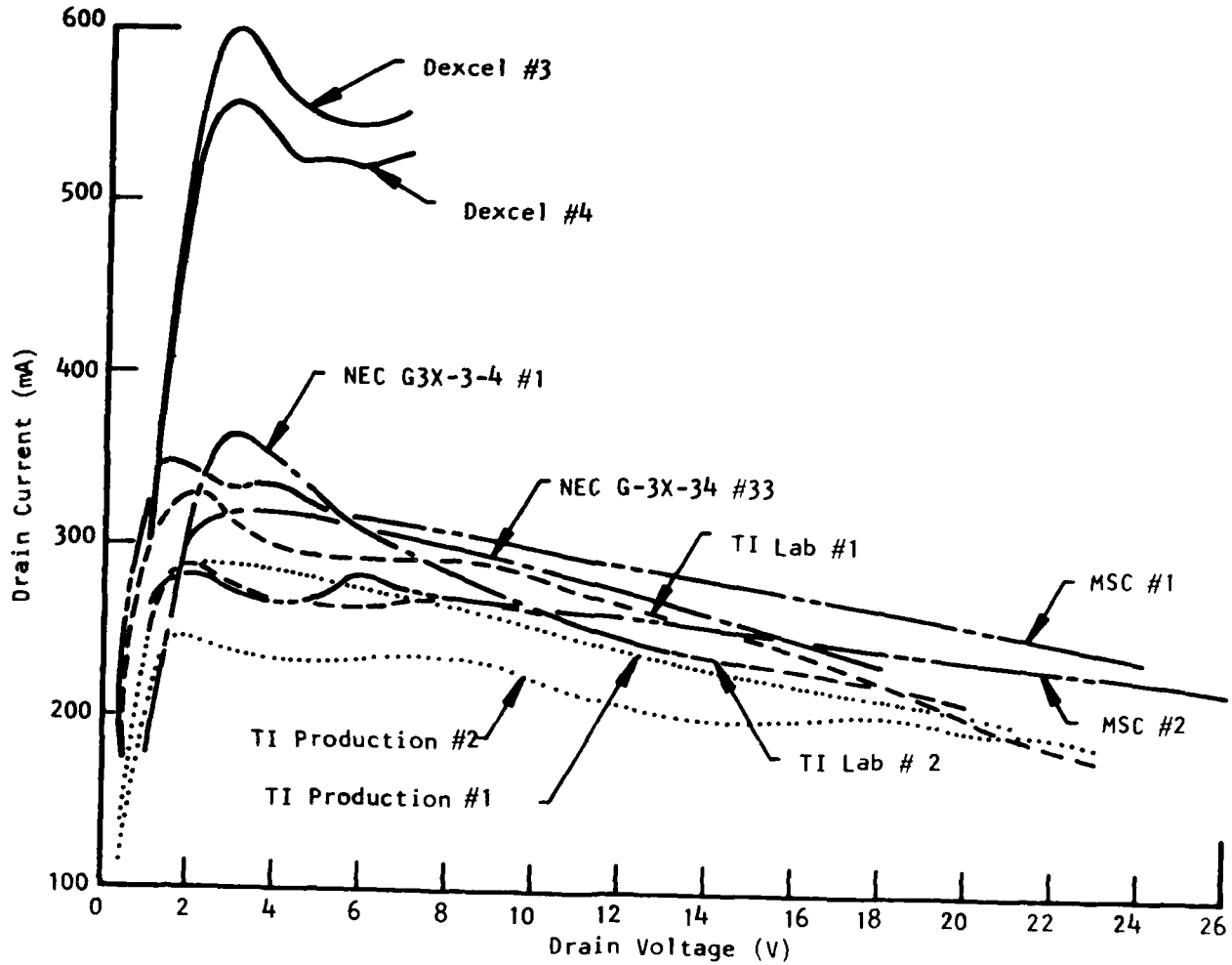


Figure 30 Drain Current as A Function of Drain Voltage with Gate Grounded

Table II

Maximum Drain Voltage Under Operating Conditions

Manufacturer	Device Number	I_{dss} (mA)	V_{sat} (V)	$g_m(V_g = 0)$ (mmho)	V_p (V)	Failure Conditions			
						V_{ds} (V)	I_{ds} (mA)	V_g (V)	$V_{ds} \times I_{ds}$ (W)
TI (P)	3	315	1.6	125	3.5	21	225	-0.8	4.7
TI(P)	4	310	1.8	100	4.5	25	184	-1.0	4.6
TI (L)	3	355	1.7	135	3.5	19	218	-1.3	4.1
TI (L)	4	355	1.7	135	4.5	17	238	-1.0	4.1
Dexcel	22	840	2.6	80	>10	14	298	-5.0	4.2
Dexcel	23	570	2.6	110	7	15	237	-2.5	3.5
MSC	11	410	1.5	90	7	22	218	-1.5	4.8
MSC	12	330	1.5	100	7	25	208	-1.8	5.2
NEC	86M-65 #27	350	2.8	75	5	31	93	-3.9	2.9
NEC	86M-65 #25	350	2.8	75	5	29	117	-3.2	3.4

will be tested before the end of the program if time allows. Although the publications of the NEC manufacturers seem to indicate that the high NEC device drain voltage capability is due to the unique gate recess structure (recessed area much wider than the gate), the $V_g = 0$ results lead to another conclusion. It is thought that the large gate voltage for the NEC devices under operating conditions (drain current only $\sim 0.3\ I_{dss}$) causes a much larger reduction in electric field near the drain contact than with the TI devices. This large gate voltage is thought to be due to the unique NEC doping profile. Although the manufacturers will not verify this, as discussed in Section II, the I-V characteristic implies a quite low active layer doping level and a retrograde profile (more lightly doped on the surface), which would force operation at larger gate voltages for optimum microwave performance. Similarly, it is thought that the large increase in Dexcel drain voltage capability is due to the large gate voltage under operating conditions ($I_{ds} \sim 40\%$ of I_{dss}). The fractional improvement is expected to be even larger than with NEC devices (as is observed), since there is no gate recess to partially reduce the electric field at the drain contact with $V_g = 0$.

Figure 31 shows the drain currents recorded for each drain voltage. Most of the bumps and all of the Gunn oscillations disappeared with the negative gate voltage. Figure 32 shows the output power at 8 GHz plotted as a function of drain voltage for these same devices. The devices were tuned for maximum output power with 4 dB gain at 8 V drain bias, and the input power and gate voltage were kept constant at higher voltages. All the devices peaked at V_{ds} = 10 to 12 V or less, so normally there is no reason to operate them at higher voltages. It is not known if the failure rate at 10 V drain bias is influenced by whether the devices will fail at 20 V or 30 V. It is hoped that the environmental stress tests will answer this question. Note that the NEC devices suffer a severe penalty for using a low-doped retrograde doping profile: they have a 1 to 1.5 dB lower output power than the TI devices in spite of their larger gate width. This has also been observed on TI devices

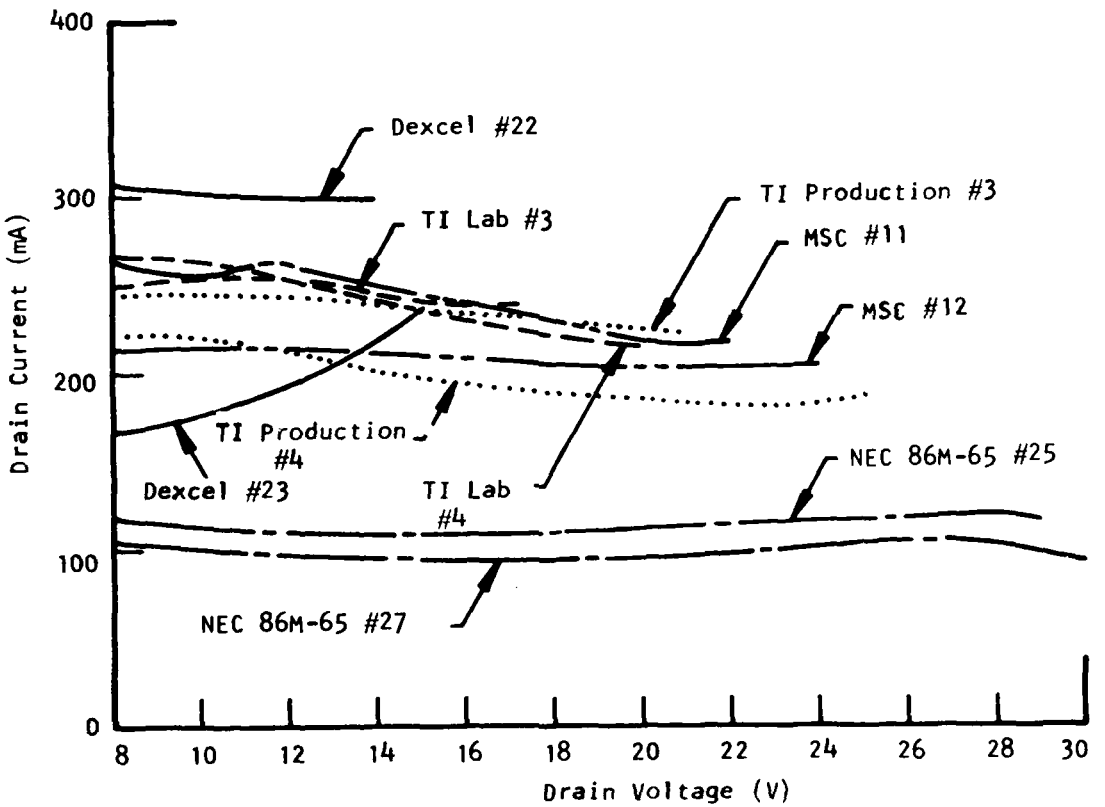


Figure 31 Drain Voltage as a Function of Drain Current with Devices Tuned for Maximum 8 GHz Output Power with 4 dB gain at 8 V Drain Bias

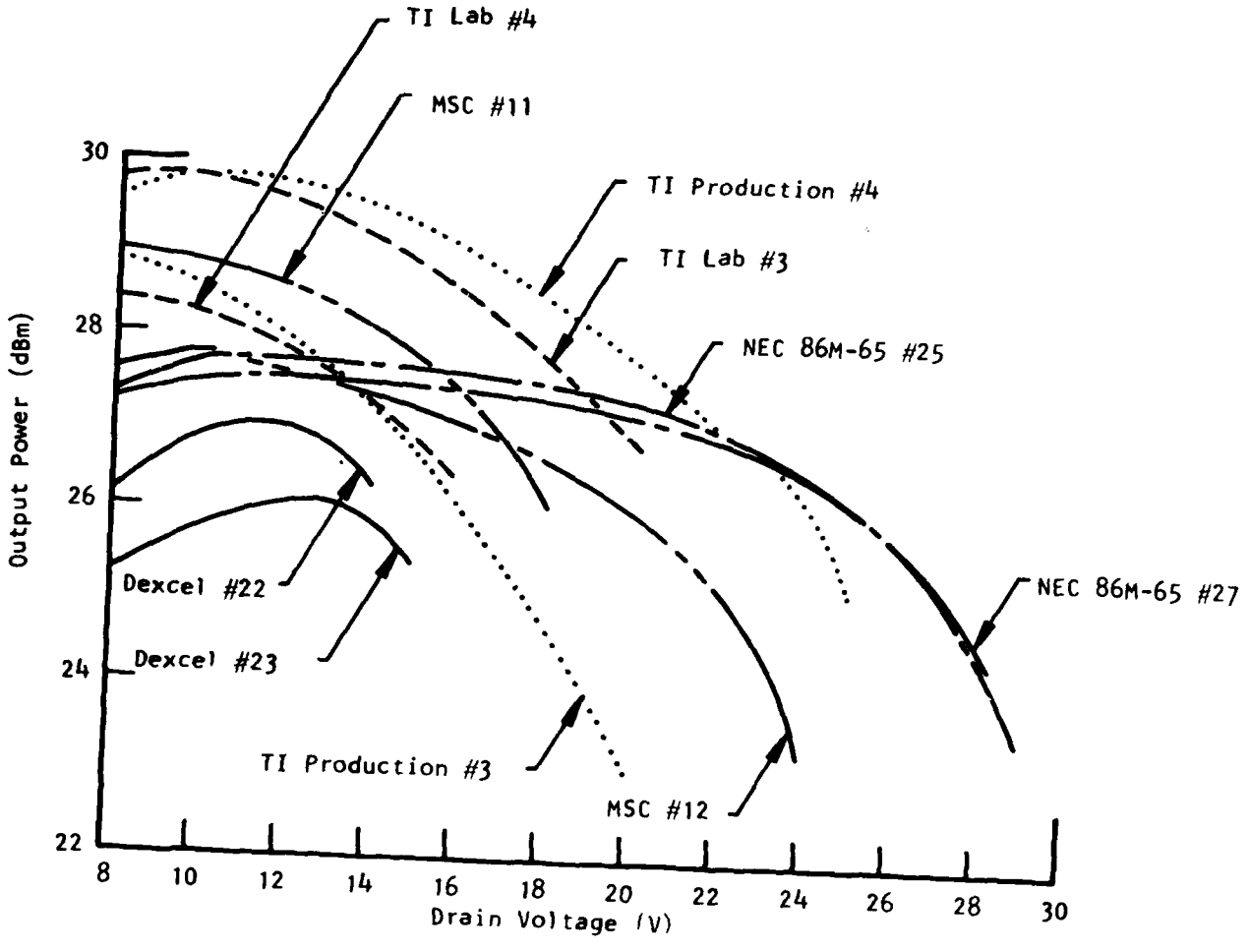


Figure 32 Output Power at 8 GHz as a Function of Drain Voltage

having such doping profiles. The Dexcel devices are quite low in output power due to the lack of a gate recess. This has also been observed on TI devices without a gate recess.

Figure 33 is an SEM photograph of NEC device 86M-65 #25 following failure. There are holes in the GaAs on both sides of one gate stripe. It is not known in what order the holes were made or the dynamics of the failure, but this is evidence for the failure being due to some type of avalanche current in the substrate. It is likely that once the channel was shorted, the gate pad shorted to the drain, resulting in the large melted area on the bottom of the photograph. The other failed devices had similar appearances, but the failure sites were more obscured by localized melting.

C. Maximum Reverse Gate Voltage

The drains of these devices were grounded to the sources and the gate voltage increased (more negative) until the devices failed. A constant current power supply was employed to reduce device destruction following failure. The results are shown in Table 12; the gate voltage and current at failure are recorded along with the dissipated power. The NEC devices had the highest failure voltage, probably due to the low active layer doping level. It is well known that the breakdown voltage of a Schottky barrier on a semiconductor increases as doping level decreases. The two TI production devices were from different slices, with the higher breakdown voltage device being more lightly doped. The TI 1 μm gate devices were not significantly different from the 2 μm devices. The Dexcel devices had considerably lower current than the others. Measurements at TI have shown that low reverse gate current is a property of nonrecessed gates. The low dissipated power of the Dexcel devices at failure demonstrates that this failure is due to the voltage rather than device heating. Figure 34 plots the gate current as a function of gate voltage on a linear scale for the ten devices.

Figure 33 SEM Photograph of Failed NEC 86M-65#25 Device.

Table 12

Maximum Reverse Gate Voltage

Manufacturer	Device Number	I_{dss} (mA)	V_{sat} (V)	$g_m (V_g = 0)$ (mmho)	V_p (V)	Failure Conditions V_g (V)	I_g (mA)	$I_g \times V_g$ (W)
TI (P)	8	285	1.6	125	3	26	140	3.6
TI (P)	10	240	1.6	100	3	36	105	3.8
TI (L)	5	365	1.7	135	3.5	25	140	3.5
TI (L)	6	340	1.7	130	3.5	27	140	3.8
Dexcel	11	480	2.5	115	5	23	20	0.5
Dexcel	12	430	2.4	115	5.5	26	10	0.3
MSC	3	405	1.5	95	7	27	140	3.7
MSC	6	290	1.3	105	6	28	200	5.5
NEC	86M-65 #23	420	2.8	60	7	44	50	2.2
NEC	84M-73A #5	440	2.6	65	8	39	50	2.0

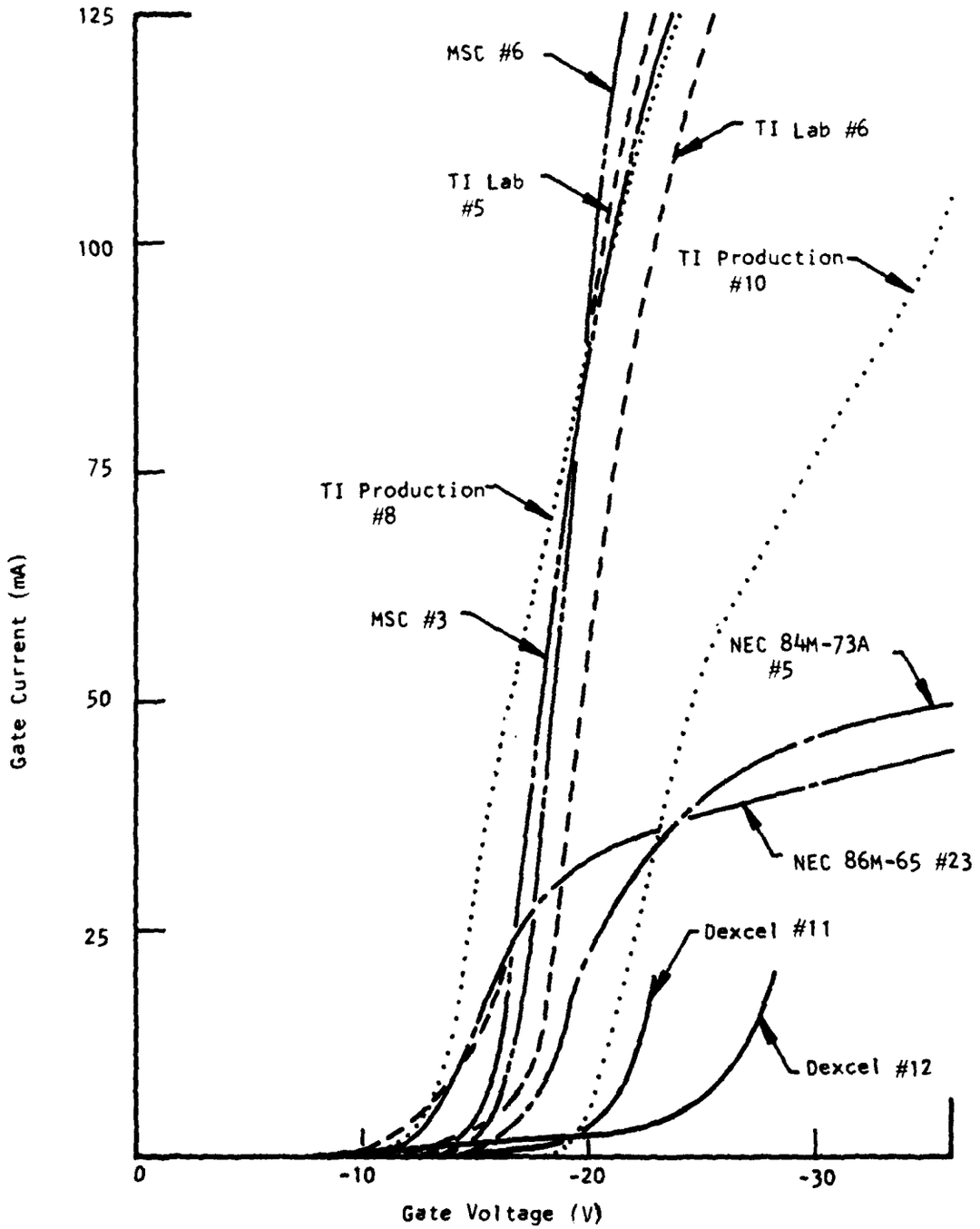


Figure 34 Gate Current as a Function of Negative Gate Bias

Figure 35 is an SEM photograph of TI production device No. 8, which failed following application of high reverse gate voltage. It appears that the gate finger at the top shorted out to the source pad, and then the high current flowing through it caused localized melting. None of the devices examined in the SEM showed the holes in the GaAs that are seen with many failed devices from the previous two tests in which high drain voltage caused failure.

D. Maximum Forward Gate Current

The drain and source of these devices were shorted together, and a positive voltage was applied to the gate. The measured current was increased in 100 mA steps until the devices failed. A 25 Ω resistor was placed in series with the devices to reduce destruction following failure. The current and voltage at failure are recorded in Table 13 along with the dissipated power. There are no large differences in the results among the manufacturers as there were for the other parameters. This failure was probably controlled by heating of the gate metal stripe. This is supported by the observation that the TI production devices that have the greatest gate length also required the highest dissipated power before failing--significantly higher than the TI laboratory devices. It should also be noted that the NEC devices, which were the only ones with aluminum gates, did not fail at lower powers than the Au gate devices. The gate currents are plotted as a function of gate voltage in Figure 36. All the devices are very similar on this semilog plot, with the TI devices having somewhat higher currents at the higher voltage levels. This may be due to higher epitaxial doping or differences in the Schottky barrier, but it was expected that MSC devices would be similar.

An SEM photograph of TI production device No. 11 following failure is shown in Figure 37. It appears that the right-hand gate first failed at the mesa edge and began conducting a high current to the source, resulting in some localized melting. Then, for reasons not apparent, the gate pad shorted to the adjacent source pad, producing a much larger amount of melting and carrying

Figure 35 SEM Photograph of TI Production Device No. 8 Following Failure Due to High Reverse Gate Bias.

Table 13

Maximum Forward Gate Current

Manufacturer	Device Number	I_{dss} (mA)	V_{sat} (V)	$g_m (V_g = 0)$ (mmho)	V_p (V)	Failure Conditions I_g (mA)	V_g (V)	$I_g \times V_g$ (W)
TI (P)	11	275	1.5	125	3	1200	2.4	2.9
TI (P)	12	240	1.7	97	3	1200	2.7	3.2
TI (L)	7	360	1.7	140	3.5	1000	2.0	2.0
TI (L)	8	370	1.7	140	3.5	1000	2.0	2.0
Dexcel	13	560	2.5	110	6.5	800	3.1	2.2
Dexcel	14	700	2.5	120	8	600	2.4	1.4
MSC	7	400	1.3	105	7	700	2.2	1.5
MSC	8	300	1.3	100	~ 7	700	2.3	1.6
NEC	86M-65 #30	390	2.8	65	6	800	2.7	2.2
NEC	84M-73A #4	315	2.7	75	5	700	2.6	1.8

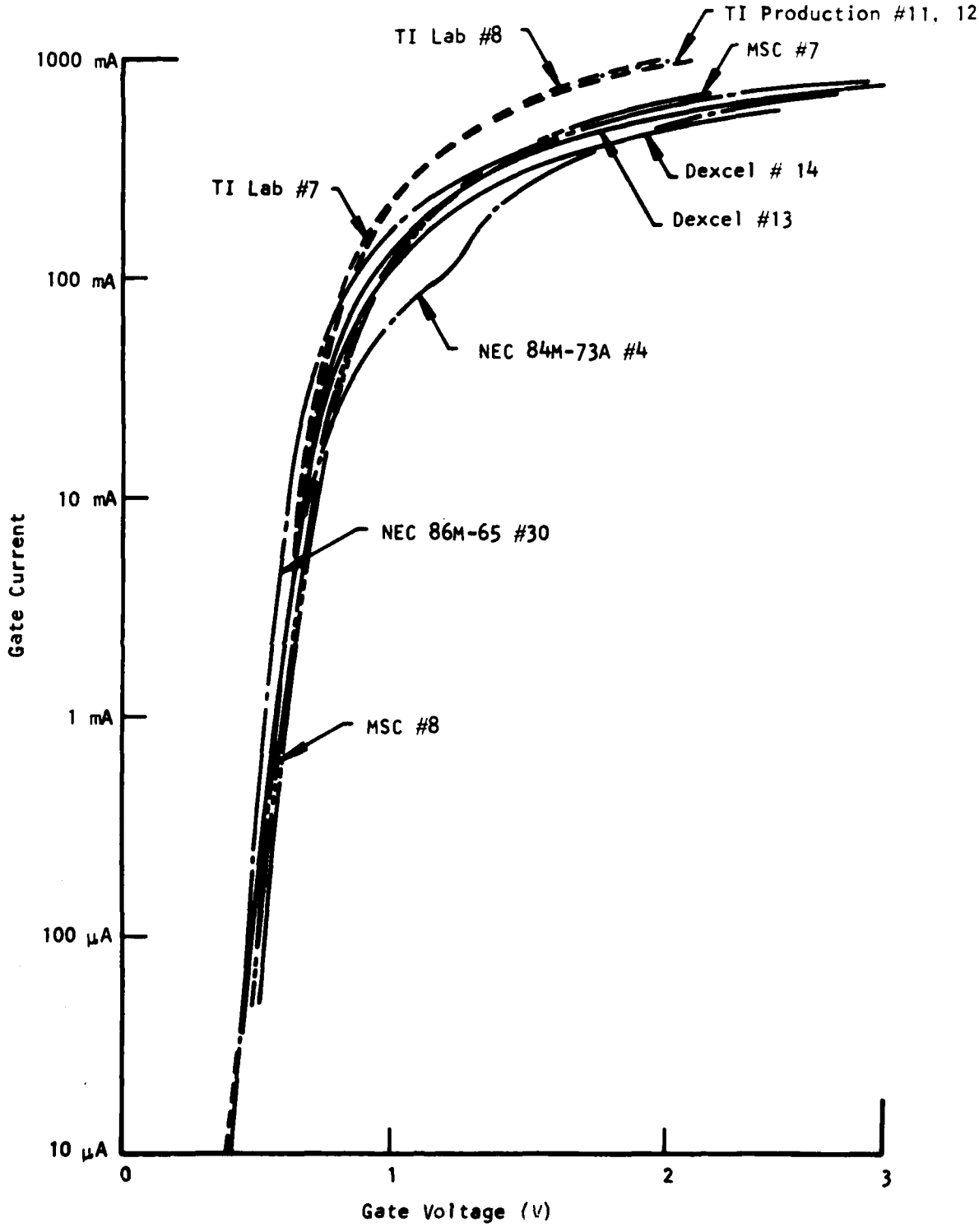


Figure 36 Gate Current as a Function of Foward Gate Bias

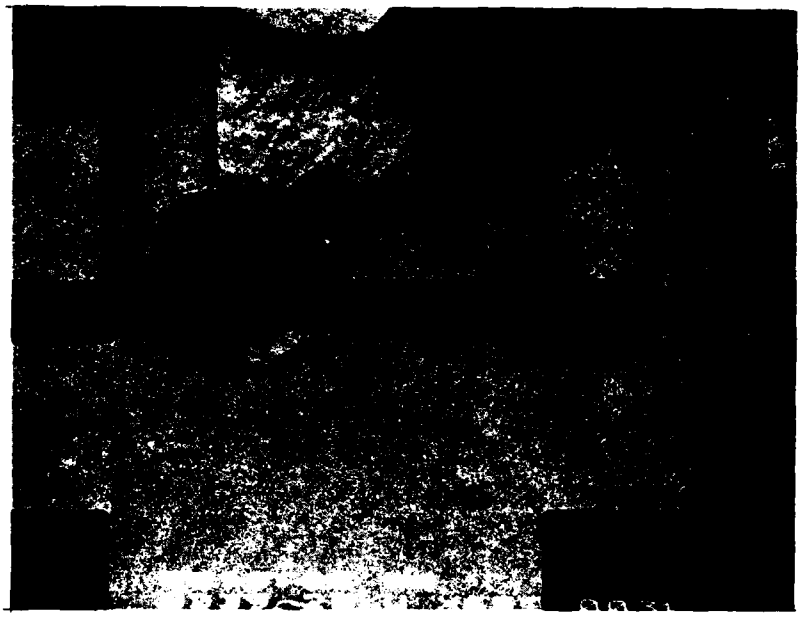


Figure 37 SEM Photograph of TI Production Device No. 11 Following Failure Due to High Forward Gate Current.

most of the current, stopping the melting at the first spot. The reason for two separate shorted areas is not known, but it was a common occurrence for failure due to this stress.

E. Maximum Cw Input Power

These devices were tuned for maximum output power at 8 GHz with 4 dB gain and 8 V drain bias. The rf input power was then increased in 1 dB steps until the devices failed. The circuit impedances were rematched at each power level to maximize output power and minimize reflected power. The maximum input power sustained by each device is recorded in Table 14. There were no significant differences betwen the manufacturers, but this test did demonstrate that these devices can sustain quite high powers before failure. The measured output power is plotted as a function of rf input power in Figure 38. SEM photographs showed that some of the failed devices appeared similar to Figure 37 and some to Figure 33 with holes in the GaAs.

Table 14

Maximum Cw Rf Input Power

Manufacturer	Device Number	I_{dss} (mA)	V_{sat} (V)	$g_m (V_g = 0)$ (mmho)	V_p (V)	Failure Condition P_{in} (W)
TI (P)	5	310	1.6	122	3.5	6.3
TI (P)	6	280	1.8	100	3.5	4.0
TI (L)	9	405	1.8	130	4	4.0
TI (L)	11	420	1.8	135	4	5.0
Dexcel	18	360	2.4	100	5	4.0
Dexcel	21	760	3.0	100	>10	4.0
MSC	9	285	1.4	100	5	6.3
MSC	10	280	1.5	100	5	6.3
NEC	84M-73A #9	385	3.0	55	8	4.0
NEC	86M-65 #28	370	2.8	70	5.5	4.0

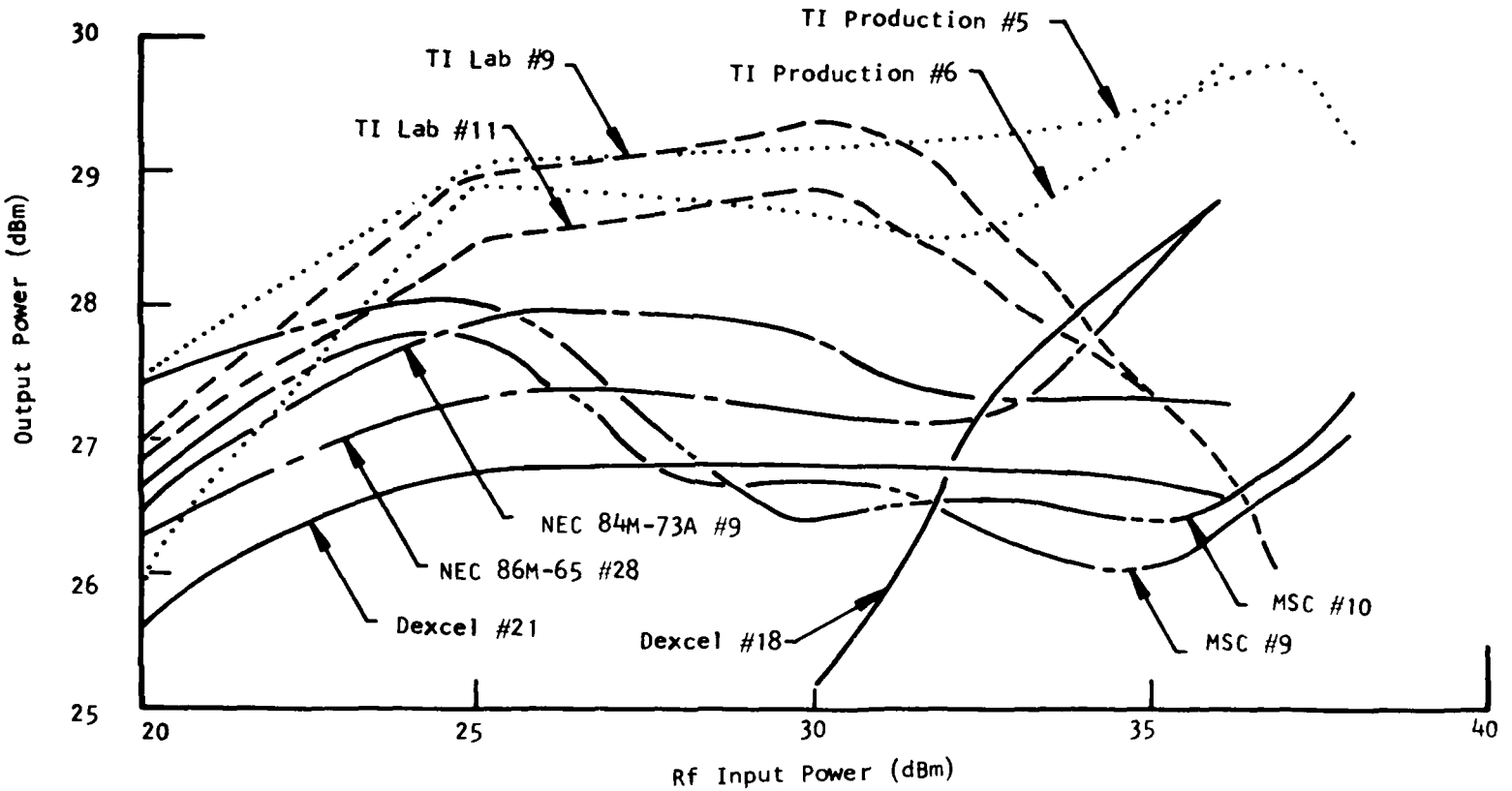


Figure 38 Output Power at 8 GHz as a Function of Rf Input Power with 8 V Drain Bias

SECTION V
ENVIRONMENTAL STRESS TESTS

The environmental tests are the most important tests of the program because they form the basis for determining the device MTTF under normal operating conditions. Four devices at each of three temperatures from each manufacturer are stressed until failure occurs (where failure is defined as 1 dB gain degradation). The devices have 8 V drain bias and 20 dBm 8 GHz input power, which is typical for these devices under normal operating conditions. It is necessary to raise the device heat sink temperatures sufficiently to induce failures in $\leq$ 1000 hours in order to obtain the data in a reasonable length of time. Several devices are scheduled to be stressed with temperature only. In the paragraphs below the elevated temperature test setup is described, and the data obtained from the first tests are discussed.

A. Elevated Temperature Test Equipment

Figure 39 includes two photographs of the present accelerated life test equipment. A photograph of the room temperature setup was in R&D Status Report No. 7. The 24-channel strip chart recorder had been used in other life testing at TI. The multimeter on top of the recorder can be switched to any of the amplifiers to read drain v[illegible]tage and current. The gate voltages are read by probing the individual gate bias lines. The gate current is not monitored.

Amplifiers that have been tuned and measured are attached to an aluminum block containing embedded heaters. Stainless steel coaxial cables are then connected to the eight-way divider on the input side and the Narda power [illegible]s on the output side. Stainless steel was used to keep the heat of the [illegible]ated life testing from the eight-way divider and the power monitors. [illegible] the rigidity of the setup, failed devices (1 dB gain degradation) [illegible]ized until the test is terminated. The bias is removed from the [illegible]s to reduce further degradation, however.

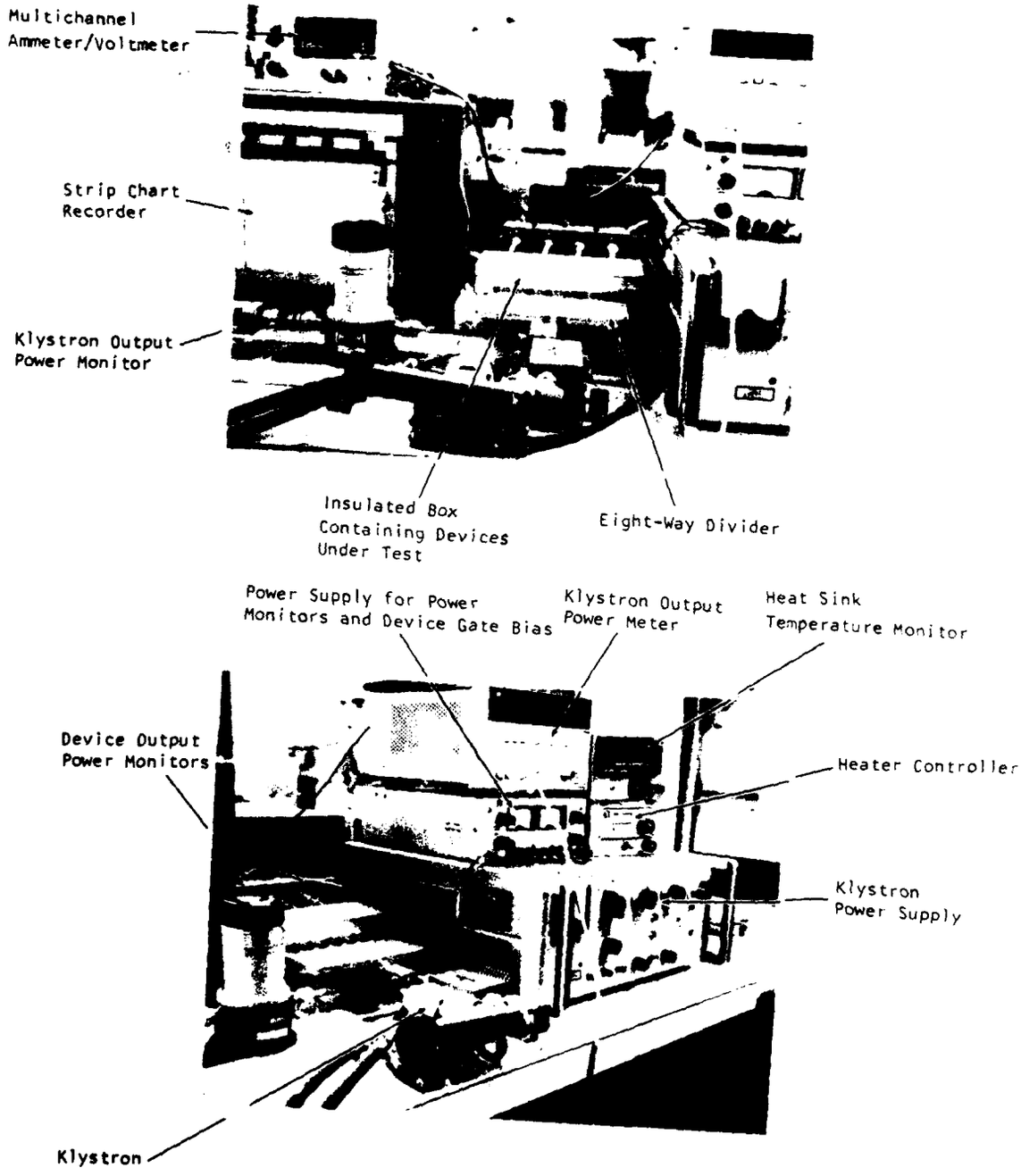


Figure 39 Photographs of Elevated Temperature Life Test Apparatus

The power monitors required an external adjustment for setting the zero point and then were calibrated for 50 mV of voltage output for 27 dBm of power fed to the connector that attaches to the amplifier. Due to the small voltages and ground loops, the calibration points of the monitors would shift, and it was necessary to rewire the monitors to operate from a floating supply and ground the low side of the input to the recorder. This improved the situation, but there still are small changes on the recorder when channels are added or subtracted.

Stable 8 GHz sources with sufficient power (1.5 W) to drive the eight amplifiers through the eight-way divider have been difficult to obtain. An IMPATT diode oscillator degraded rapidly, and high power FET oscillators are more difficult to design than are amplifiers. A 1.5 W klystron is being employed at present, and the possibility of using low power FET oscillators followed by 1.5 W FET amplifiers is being investigated.

On the first accelerated life test 28 V dc flat strip heaters were mounted to the bottom of the test fixture block. A sensistor and associated circuitry were used to control the power applied to the heaters to maintain 150° C. For the second accelerated life test, with a goal of 200° C, a 110 V ac controller and rod type heating elements were obtained. Insulated aluminum bottom and top covers were fabricated to cover the amplifiers and reduce heat loss. Even with this preparation the unit required about two hours to warm up to 200° C. The test fixture mounting block and bottom cover are held above an aluminum base plate by short stainless steel rods, and the base plate underneath the bottom cover became very warm. It is thought that radiation from the cover heated the base plate, drawing away the heat from the fixture. On the next accelerated test a thermal barrier will be inserted between the bottom cover and the base plate to further reduce heat loss.

B. Test Circuit Development

To supply rf power to the devices under test, it was necessary to design matching circuits for the different device types. S-parameters for the Dexcel devices were obtained from the specification sheets, and it was estimated how they would change at large signal levels. Microstrip matching circuitry was then designed with 39.37 mm (0.010 inch) thick alumina using the modified S-parameters. Provision was made on the photomasks of the microstrip circuitry to include small squares of gold so that some adjustment of the matching could be done by attaching gold foil.

Because no data sheets were available for the NEC devices, their small-signal S-parameters were measured on a Hewlett-Packard automatic network analyzer. Again, circuits were designed from adjusted S-parameters, photomasks made, and the devices tuned.

Circuits for the MSC devices were designed from published S-parameters, as were the Dexcel devices.

TI devices were tuned by using existing circuitry from the Dexcel and NEC designs.

For the accelerated life testing the microstrip circuitry was soldered down to Au-plated Cu amplifier blocks with 80% Au/20% Sn (280°C melting point). Bypass capacitors and bias wires were soldered with 96% Sn/4% Ag (221°C melting point). Device packages were screwed down to the amplifier blocks, which were screwed to the Al heater block.

C. Preliminary Results

The first accelerated life test was conducted at 150°C base plate temperature. The results are compiled in Table 15, which lists the power output before and after the 1000-hour test. There were several cases of power degradation greater than 1 dB, but these were always associated with circuit degradation problems and the devices could usually be retuned to near the

Table 15

Power Output at 8 GHz with 20 dBm Input Before and After 1000 Hours at 150°C

Device	P_{out}, dBm Before	P_{out}, dBm After (Fixed Tuned)	Difference (dB)	P_{out}, dBm After (Slide Screw Tuners Used)	Difference (dB)
[1]DXL 16	24.2	25.3	+1.1		
[2]DXL 15	26.9	25.8	-1.1	27.4	+0.5
MSC 5J	27.0	26.6	-0.4		
MSC 6J	26.4	26.4	0.0		
[3]MSC 7J	26.3	19.2	-7.1	25.2	-1.1
[4]NEC 1J	25.2	24.6	-0.6		
NEC 22	25.8	26.1	+0.3		
[5]NEC 24	25.4	24.4	-1.0	25.4	0.0

[1]The 1.1 dB increase was thought to occur because of changes in the circuitry, in such a manner as to better match the FET.

[2]An output power of 27.4 dBm, using slide screw tuners, could be attained. Upon examination it was found that a crack in the alumina had developed that ran under the output microstrip line.

[3]An output power of only 24.2 dBm could be attained, even using slide screw tuners. It was found that the alumina had almost broken away under the output SMA connector pin.

[4]The amplifier output stopped abruptly at eight hundred hours. At the end of one thousand hours, when the amplifier could be looked at under a microscope, it was found that the microstrip high impedance drain bias line had been previously scratched and finally opened. The gap was bridged and the output power measured to within six tenths of a dB of the initial reading.

[5]This amplifier showed some peculiar behavior. It quit at the beginning of the test and although there had been no DC bias voltages applied during the one thousand hours it was still subject to the 150 C base plate temperature. The output power was found to peak at 25.5 dBm for 18.8 dBm input. The gate voltage was changed from -3.3 to -2.62 VDC to optimize the output with 20 dBm input. The output then was 25.4 dBm, which was the original power output level.

original output power with slide screw tuners. The conclusion from this test was that the transistors survived 150 °C, and at least 200 °C will be necessary to obtain sufficient device degradation.

The first 200 °C test is still in progress. Steps were taken to avoid the circuit degradation problems observed during the first 150 °C, 1000-hour test described above. The four Texas Instruments and four Dexcel devices that had been prepared previously for the 200 °C test were remeasured for maximum output power using the slide screw tuners in the X-band setup to ascertain that the devices had indeed been optimally tuned. The Dexcel devices increased only 0.2 dB maximum, and the TI devices increased 0.6 dB maximum. After the amplifiers were tuned and measured, they were put in an oven at 200 °C overnight (no bias) to discover any circuit degradation problems before the actual test. It is thought that this will not significantly affect the device degradation. In addition, care was taken to assure that the SMA connector block did not touch the circuitry and put undue pressure on it during expansion at the higher temperatures. Even with these precautions, one of the TI amplifier microstrip circuitry drain bias lines opened during the first few hours of the 200 °C testing.

It was decided that all devices from a particular manufacturer stressed at a particular temperature should operate at the same drain current so that the dissipated powers and hence the channel temperatures will be identical (assuming device thermal resistances are the same). This is necessary to accurately obtain the MTTF. The gate bias voltages of the eight devices mentioned above were therefore adjusted to give the same drain current for each manufacturer, which was taken as approximately the average of the four drain currents. The output power dropped 0.4 dB at most.

SECTION VI
SUMMARY

The devices chosen for this reliability study were the TI MSX 802 and laboratory devices, Dexcel 3615A-P100F, MSC 88002, and NEC 868196. All are hermetically packaged GaAs power FETs with ~0.5 W output power. The device physical characteristics were obtained from measurements and conversations with the manufacturers, and significant differences between device types are apparent.

Four devices from each manufacturer were electrically characterized, with small signal S-parameters, gain, 3 dB bandwidth, phase linearity, third-order intermodulation, and noise figure being measured. Remeasurement of these parameters on the first eight devices operated for 1000 hours with 8 V drain bias and 20 dBm input power at 8 GHz indicated no significant change in any of these parameters.

All electrical stress tests were completed, and most of the differences between the device types could be associated with differences in device physical characteristics. The failures could usually be explained in terms of failures described in the literature.

The elevated temperature stress tests (environmental stress) have begun, and heat sink temperatures of at least 200°C were found to be necessary to obtain device degradation within 1000 hours. The fabrication of the test setup and high temperature circuits was more difficult than originally thought. Since obtaining sufficient data to extrapolate an accurate MTTF under normal operating conditions for all device types is regarded as the most important part of the reliability study, extensive effort will be expended in this area for the rest of the program.

During the remainder of the program, the electrical characterization measurements will also be completed on the second batch of eight devices that have completed 1000 hours of operation. The electrical characterization will be conducted too on one device from each manufacturer bonded as an oscillator. Two devices from each manufacturer will be characterized as pulsed amplifiers, and two from each manufacturer will be pulse-stressed until failure occurs. Environmental characterization has begun on five devices from each manufacturer and is expected to be completed in the next few months.

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