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AC CONTROLLER FEASIBILITY STUDY. REVISION A.(U)
MAY 79 E LACHOCKI, J B MCMACKIN, C L WHITMAN N62269-78-C-0394
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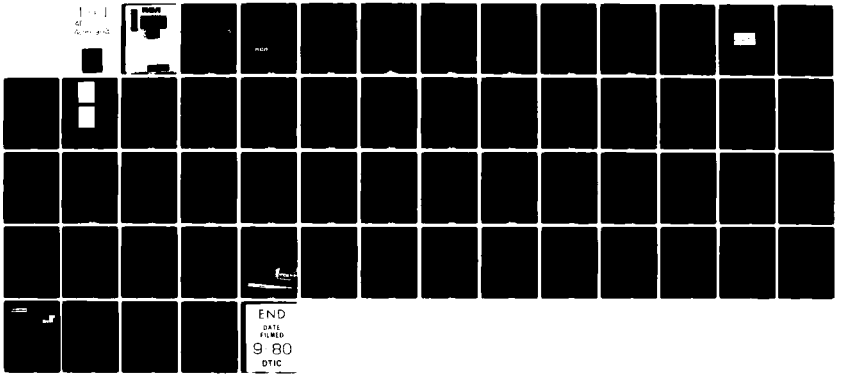

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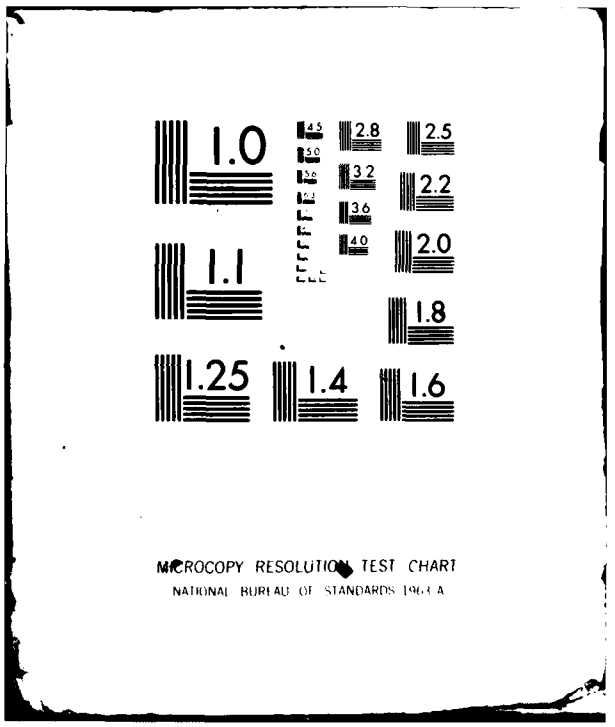
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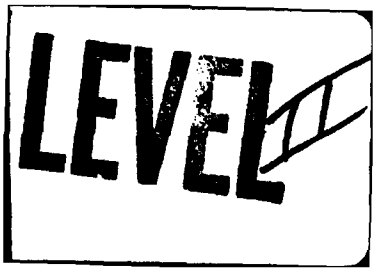
LEVEL II

FINAL REPORT

AC CONTROLLER FEASIBILITY STUDY

PREPARED FOR: NADC
WARMINSTER, PA.

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(9) FINAL REPORT
(6) AC CONTROLLER FEASIBILITY STUDY.
Revision A.

Prepared for: NADC
Warminster, PA.

Contract No. (15) N62269-78-C-0394

(11) 31 May 79

(12) 57

This study compares the AC controller design submitted by NADC vs. specification and spec. modification needed to construct a controller in a module size defined by NADC. Circuit designs are discussed that could be incorporated into a 115 V, 5 A, SSPC and a 26 V, 1 A, module.

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1.0 INTRODUCTION

RCA has completed study and design phases of a DC Power Controller and now continues to deliver 10A,5A,2A and 1/2A units under contract No. N62269-77-C-0413. Many lessons have been learned during this program and this experience will be transferred to the AC Power Controllers study to guide future development efforts.

This report presents design concepts for meeting the established requirements for AC Power Controllers specified in NADC-30-TS-7602 document. Two Solid State Power Controllers (SSPC) were designed: 115V at 5A, 400 Hz and 26V at 1A, 400 Hz. The basic functional requirements for both controllers are as follows:

(a) to provide switching between a power bus and the load,

(b) to carry rated current with a high degree of efficiency,

(c) to provide automatic opening under overload conditions with specified delay characteristic,

(d) to provide isolation for control element, AND

(e) to be capable of being controlled and reset remotely.

Since size is a primary constraint, the design effort was directed towards the 115V controller with the greatest power delivery capability. The lower rated units would utilize identical control circuitry but would take advantage of smaller components in the power switching stage. The components and circuits described in this report are representative of controllers requirements with consideration of suitability for hybridization.

1.1 115 VAC Power Controller Design Consideration

In order to determine the feasibility of constructing a 5 ampere AC controller in a module which has a base of 1.5 by 1.5 inches and a 1.1 inch maximum height, the limitations imposed by the specification NADC-30-TS-7602/03 and spec. modification must first be studied. The impact of implementing the spec. requirements into small and efficient circuitry was broken down into four functional and physical subcircuits. These subcircuits are:

a) Auxiliary power supply - supply DC regulated voltage used for internal control which is derived from the AC supply line

b) Control - level detection and logic used to determine the electrical state of the controller.

c) Input isolation - developes the BIT input impedance and couples the turn on signal to the control circuitry.

d) Power switch - supplies the AC output to the controller load.

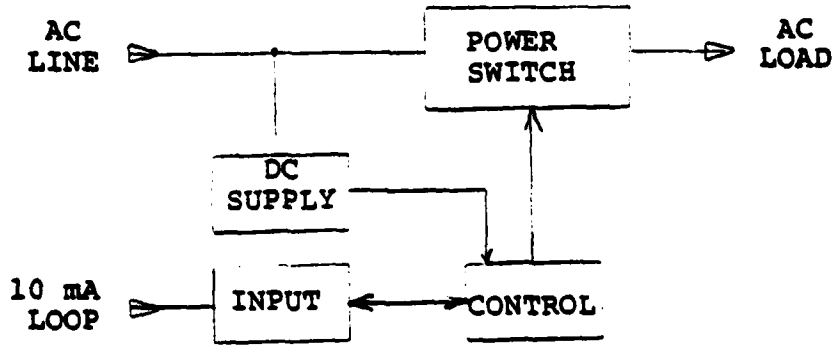


Figure 1.1 SSPC Functional Block Diagram

2 AUXILIARY POWER SUPPLY

The isolated power supply needed to provide low level DC power to the control and drive circuitry would consist of regulated DC-DC converter. To minimize the size and weight of a transformer and filter capacitors, the operation frequency has been increased to 40 kHz.

The basic energy pump regulator used for the proposed DC-DC converter functions as follows:

The control circuit causes transistor switch, Q1, to turn on and off at a predetermined peak current sensed at R1 resistor. With Q1 closed, in a simplified schematic diagram in Figure 1.2, the DC input voltage is impressed across T1 (PR1) and current will increase

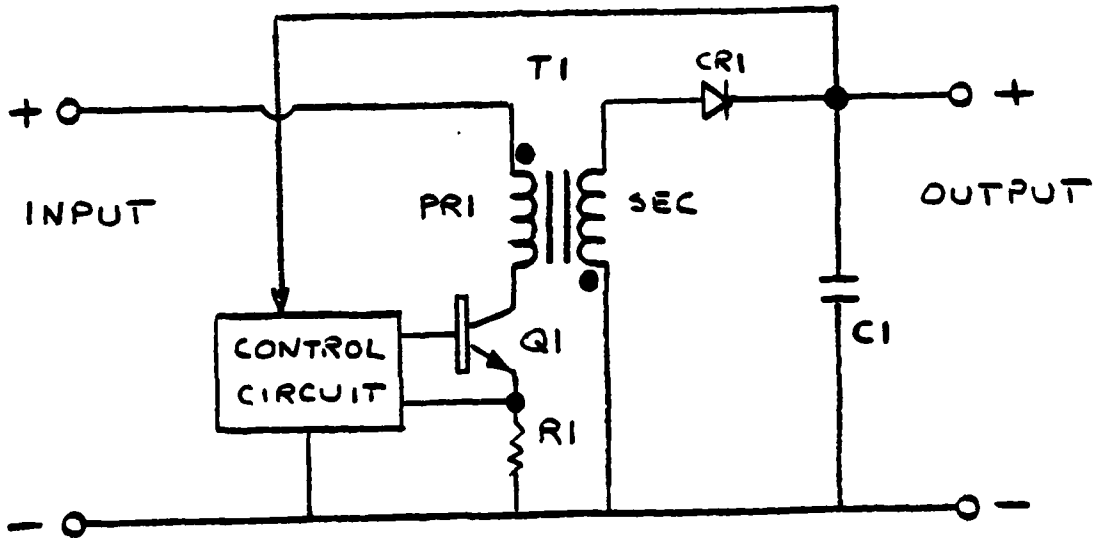


Figure 1.2 Energy Pump Regulator

linearly. As indicated by the polarity dots, the voltages across the windings of the transformer are such that the diode (CR1) is back biased and will not conduct. Therefore, the circuit is inductive and energy is being stored equal to $1/2\ Li^2$. If at some pre-determined instant Q1 is opened, the voltages on all windings will instantly reverse polarity and will rise until a discharge path is found. The primary winding is open, but the secondary will forward bias CR1 diode and allow the energy that was stored to dump into C1 capacitor. The output voltage at C1 is monitored and is used to control the frequency of switching through the control circuit. The output power is transferred to the loads through other parallel secondaries (not shown in simplified schematic) to corresponding diodes and capacitors.

When the output terminals are loaded excessively, frequency of operation increases until waiting period (tw) is equal zero and, as can be seen in Timing Diagram of Figure 1.3, frequency switching will be constant and delivered power will be limited.

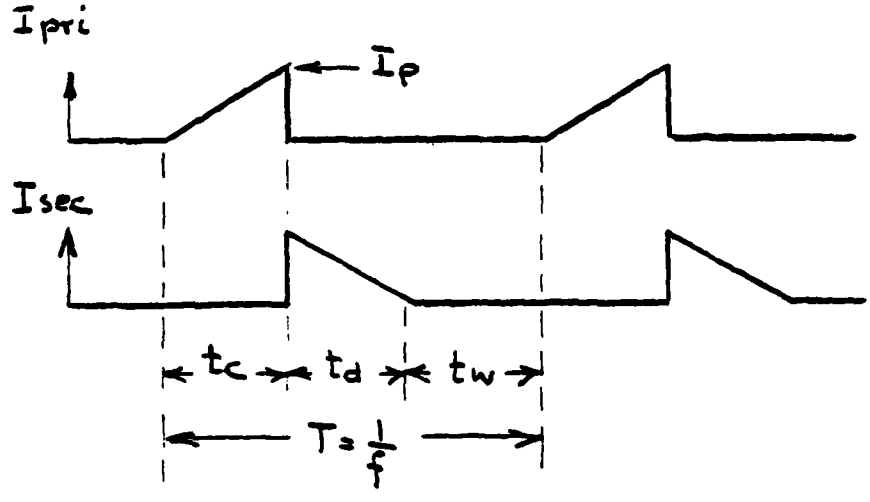


Figure 1.3. Timing Diagram

Variation in the load will cause the waiting period (tw) to change, thus forcing operating frequency to vary widely. The square wave oscillator provides sync pulses to the driver circuit forcing the idle stage to turn on. The on duty cycle is adjusted now by the voltage sensing circuit providing the two step voltage response shown in Figure 1.4.

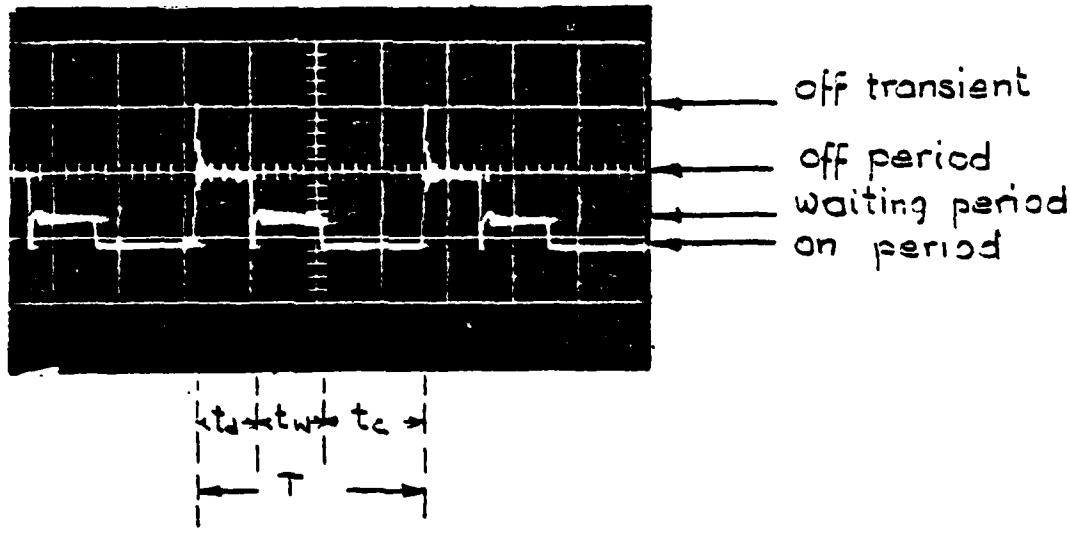


Figure 1.4. Switching Transistor Collector-Emitter Voltage

The output voltage regulation is achieved only by controlling number of pulses in a unit of time. Since at a heavy load more energy is needed, it causes higher switching frequency, which is desired for pulse integration and filtering. At a very light load the operating frequency will become very low, but since the energy level at this time is also low, filtering of such a signal presents no problem.

1.2.1 Circuit Operation

A block diagram of the single-phase energy pump regulator is shown in Figure 1.5.

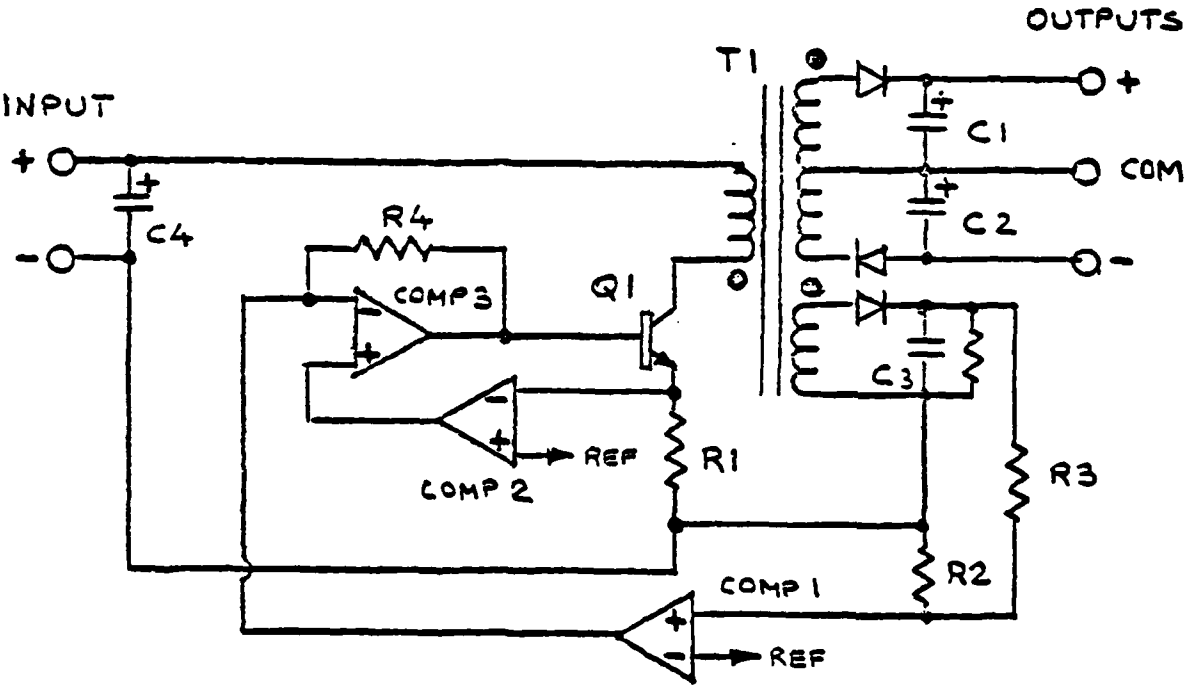


Figure 1.5. Single-Phase Voltage Regulator

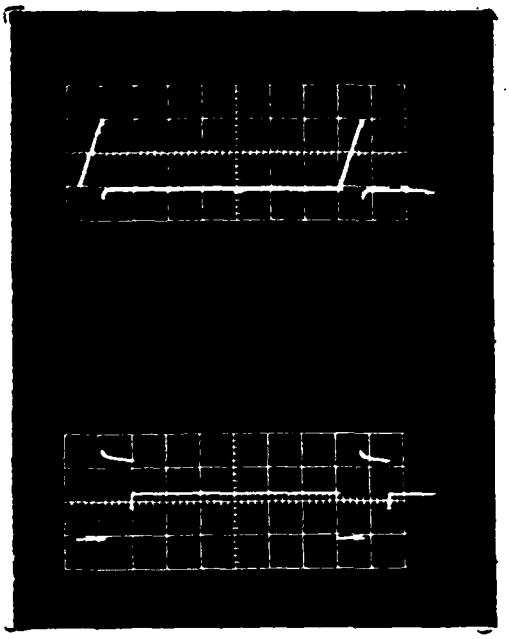
The Q1 transistor triggers on when the output voltage falls below a predetermined level at the voltage divider R2 and R3, and turns off when the current in the transistor Q1 rises to a level set by R1. The energy stored in the transformer is then supplied to the output windings.

When upon completion of the energy dump to the load, the voltage on the filter capacitors exceeds the reference voltage applied to the regulator error amplifier (Comp. 1), then a waiting period will occur before the next charging cycle can start. All secondary windings of transformer T1 are related by the turns ratio, therefore controlling the output voltage of one winding controls all the others. Load change will modify output voltage of the sensing winding and will correct input voltage to comparator 2, effecting switching frequency of Q1 current and energy stored in the inductor. Figure 1.6 is the photograph of collector voltage and current at light and heavy loads.

The schematic of the complete single-phase energy pump regulator is given in Figure 1.7.

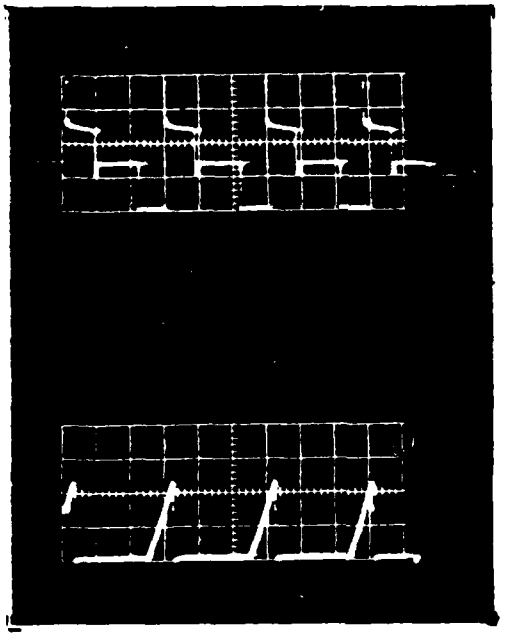
A constant current generator (VR3, Q4) supplies power to a stable voltage reference (VR1).

Q1 transistor turns on main switching transistor Q3. The peak current in this transistor is sensed by R14 and comparator U2 to reset FF U1 and maintain constant energy stored during each pulse. The output voltage is monitored at C6 and is used to set FF U1 if the output voltage is low and thus controls the frequency of switching. Transformer output voltage is sensed by



Collector Current
Vertical: 1A/cm
Horizontal: 20 us/cm
Load 2.8W
Input 28V

Collector Voltage
Vertical: 20V/cm



Collector Voltage
Vertical: 20V/cm
Horizontal: 20 us/cm
Load 6.7W
Input 28V

Collector Current
Vertical: 1A/cm

Figure 1.6 Switching Transistor Collector Characteristics with Load Change

comparator Q2, which prevents transistor Q3 from turning on until the stored energy in the transformer has been transferred to the load.

The circuit alternately stores energy in a linear inductor (T1 primary) in the first half-cycle, and dumps it into the integrator capacitors C6 and C7 in the second half-cycle. This process is repeated at 40 kHz and varies with the load changes as indicated in the photograph in Figure 1.6. The voltage relationship between the sensed winding (3-4) and the other outputs is determined by their turns ratio. This ratio is not related to the primary winding, however, as the primary winding is open-circuited during the energy integration cycle. Output voltage is adjusted by changing reference level at comparator U1 having the inverted input connected to the sensing winding.

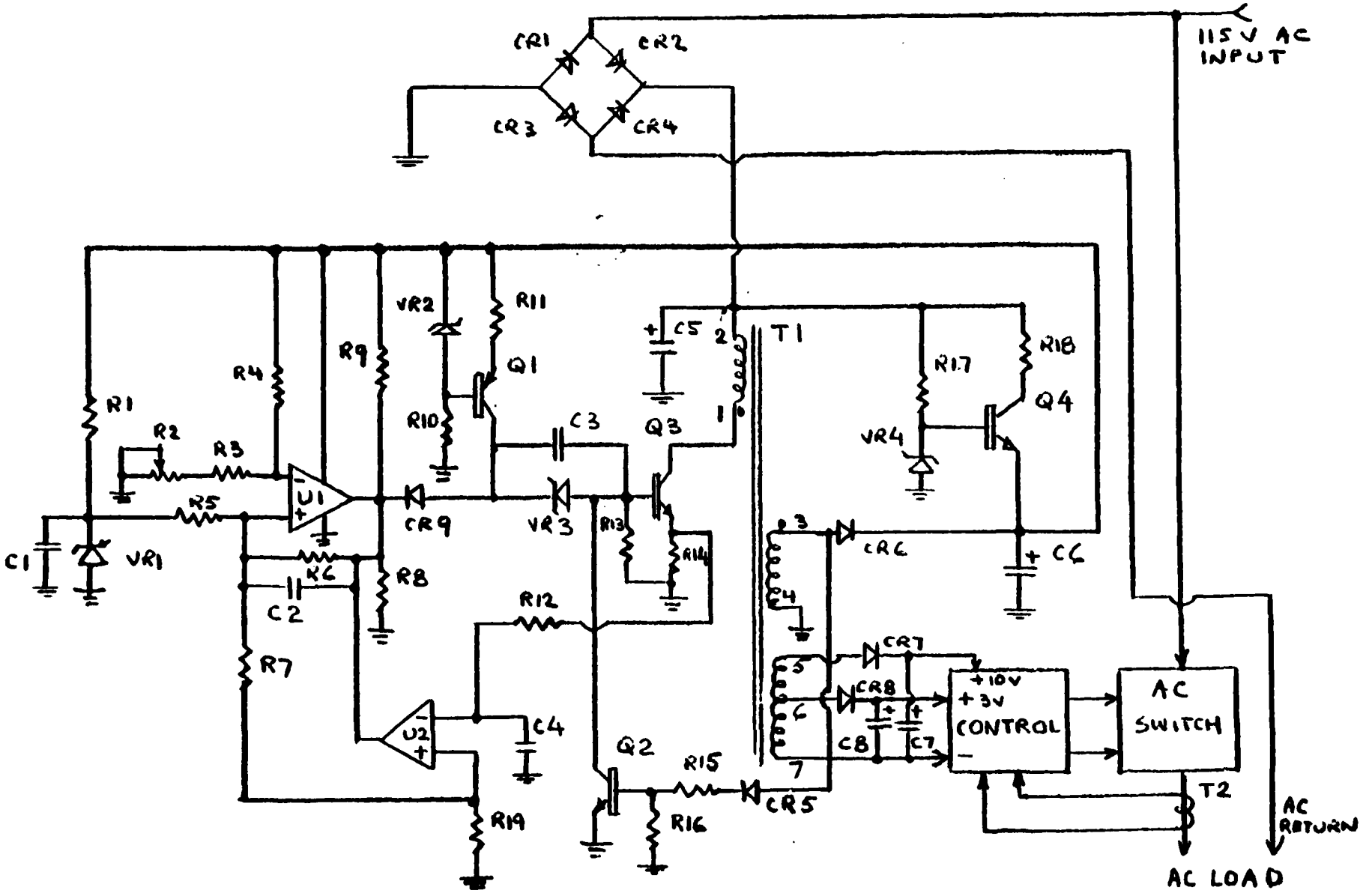


FIG. 1.7 ENERGY PUMP VOLTAGE REGULATOR SCHEMATIC

1.2.2 Analysis and Design Formulas

The energy stored (W) during period of time is defined as power. In an energy pump regulator, the power that can be delivered is determined by the frequency (f) at which the storage takes place.

$$P = Wf \qquad (1)$$

The energy is stored in the form of current in inductor (Lp) of the primary winding of the transformer. The output rectifiers (CR6 and CR7) are back biased during the primary winding conducting time (t_c) and therefore all the primary current is going to develop the stored energy.

$$W = 1/2\ LpI_p^2 \qquad (2)$$

For practical reasons, the series charging resistances consisting of C5 impedance, DC resistance of T1 (1-2), saturation resistance of Q3 (VCE sat) and sensing resistor R13, The charging current can be approximated as a ramp rise determined by the voltage (Ep) across the primary winding (Lp). Charging time (t_c) will be:

$$t_c = \frac{Lp\ Ip}{Ep} \qquad (3)$$

When at the peak current, transistor Q3 is interrupted then the stored energy will cause current to flow in the secondary winding with reversed polarity. The total stored energy will be delivered to the load if integrating capacitors

C6 and C7 have low impedance. The discharge of energy can be approximated by a descending ramp with the slope dependant on secondary (5-6) DC resistance diode (CR7) forward resistance and capacitors impedance. Discharge time (t_d) will then be:

$$t_d = \frac{L_s I_s}{E_s} \qquad (4)$$

where E_s is secondary voltage. This characteristic is shown in Figure 1.8.

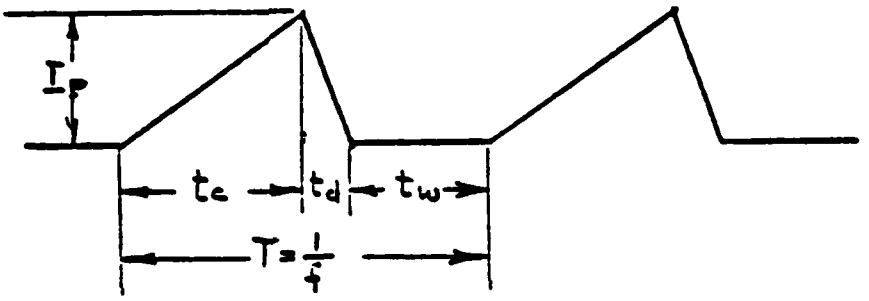


Figure 1.8. Charging Characteristic

Relation between primary and secondary peak currents can be expressed by the following formula:

$$I_p N_p = I_s N_s \qquad (5)$$

where N_p and N_s are primary and secondary number of turns. Using equations (3), (4) and (5), the following relation can be realized:

$$\frac{t_c E_p}{L_p} N_p = \frac{t_d E_s}{L_s} N_s$$

$$\therefore \quad t_d = t_c \frac{N_p E_p}{L_p} \frac{L_s}{N_s E_s} \qquad (6)$$

Maximum power from a given transformer will occur when the waiting time (t_w) is zero and frequency (f) is maximum.

$$\bar{P} = w\bar{E} = \frac{1}{2} L_p I_p^2 \bar{r} = \frac{\frac{1}{2} L_p I_p^2}{(t_c + t_d)}$$

$$\bar{P} = \frac{\frac{1}{2} L_p I_p^2}{t_c \left(1 + \frac{E_p}{N_p} \frac{N_s}{E_s}\right)} = \frac{\frac{1}{2} L_p I_p^2}{\frac{L_p I_p}{E_p} \left(1 + \frac{E_p}{N_p} \frac{N_s}{E_s}\right)}$$

$$\bar{P} = \frac{E_p I_p}{2 \left(1 + \frac{N_p E_p}{L_p} \frac{L_s}{N_s E_s}\right)} \qquad (7)$$

At the instant of current switch-over:

$$W_p = W_s$$

$$\therefore \quad \frac{1}{2} L_p I_p^2 = \frac{1}{2} L_s I_p^2 \frac{N_p^2}{N_s^2}$$

$$L_s = L_p \frac{N_s^2}{N_p^2} \qquad (8)$$

Substitute 8 into 7

$$\bar{P} = \frac{E_p I_p}{2 \left(1 + \frac{N_p E_p}{L_p} \frac{L_p N_s^2}{N_p^2 E_s N_s}\right)}$$

$$P = \frac{E_p I_p}{2\left(1 + \frac{E_p}{N_p}\,\frac{N_s}{E_s}\right)} \qquad (9)$$

The power represented by equation (9) is the maximum power that transformer can deliver including the sum of all outputs and losses of diodes and transformer. At minimum input voltage, the peak charging current must be sufficient to provide the sum of these powers.

To determine the maximum inductance in a primary winding of the transformer (T1), compare equations (1) and (2).

$$\frac{P}{f} = \frac{LI_p^2}{2} \qquad (10)$$

also: $$I_p = \frac{E_p t}{L} = \frac{E_p T}{2L} = \frac{E_p}{2fL} \qquad (11)$$

from equations (10) and (11) -

$$P = \frac{E_p^2}{8fL}$$

or $$L = \frac{E_p^2}{8fp} \qquad (12)$$

1.3 CONTROL CIRCUIT

The differences between the operation of the AC controller system supplied by NADC and the specifications and spec modification to be used to construct the most recent AC controller would require implementing additional control circuitry. The modified controller spec requires operation up to ten times rated load current, with the controller rapidly tripping out, if this current level is exceeded. This would require a detection scheme that would operate over a greater output current range and also monitor the positive and negative half cycles in order to trip out instantly. The design submitted by NADC only had to detect up to three times rated current and would current limit at that maximum level for at least 70 cycles. With this technique, every other half cycle could be monitored for adequate trip time results.

Because of the large range of load current that must be detected, two separate sense coils would be used to detect the over-current trip range and also the minimum current level needed to determine the fault state. (See Block Diagram, Figure 1.9). Each core would be selected so that the upper end of each function's current sense range would be just below the point where the core material would be saturated. Therefore, rapid output transitions could not generate large voltages which could damage the control circuitry.

In order to minimize the quiescent power dissipation, CMOS logic elements would be used in the control circuitry as shown in Figure 1. The control logic would also contain the TRIP state flip-flop as

opposed to implementing this function as part of the input circuit as indicated a part of the NADC supplied design. This would reduce the lag time between detection of the trip condition and the removal of the control signal to the power switch.

The logic circuitry is implemented so that trip sense function will detect peak current excursions during both half-cycles. In contrast, the minimum current detector integrates the sensed output current only during every other half-cycle, in order to simplify the detection scheme. Control trip sense circuitry is shown in Figure 1.11.

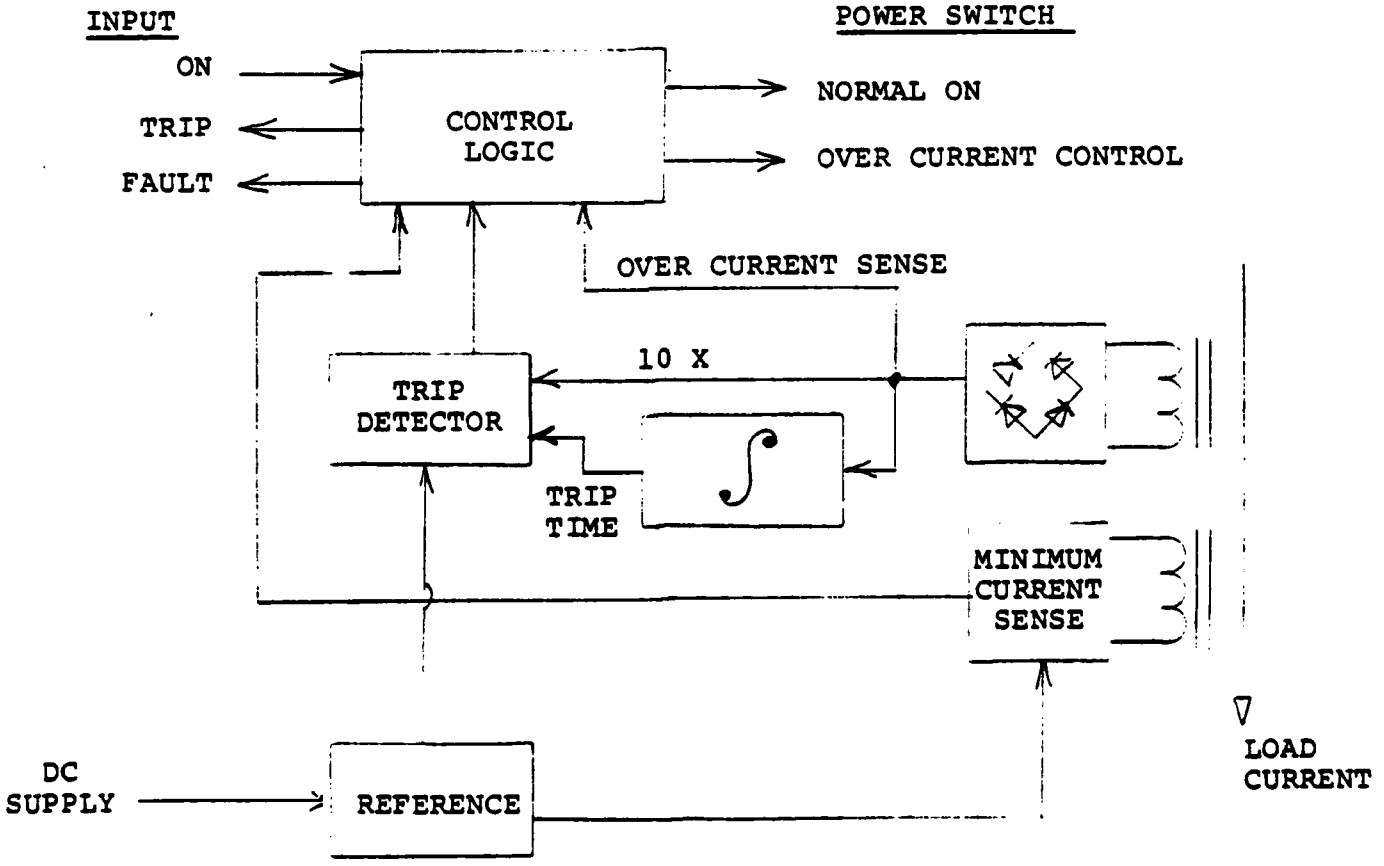


Figure 1.9. 115V AC Solid State Power Controller, Block Diagram

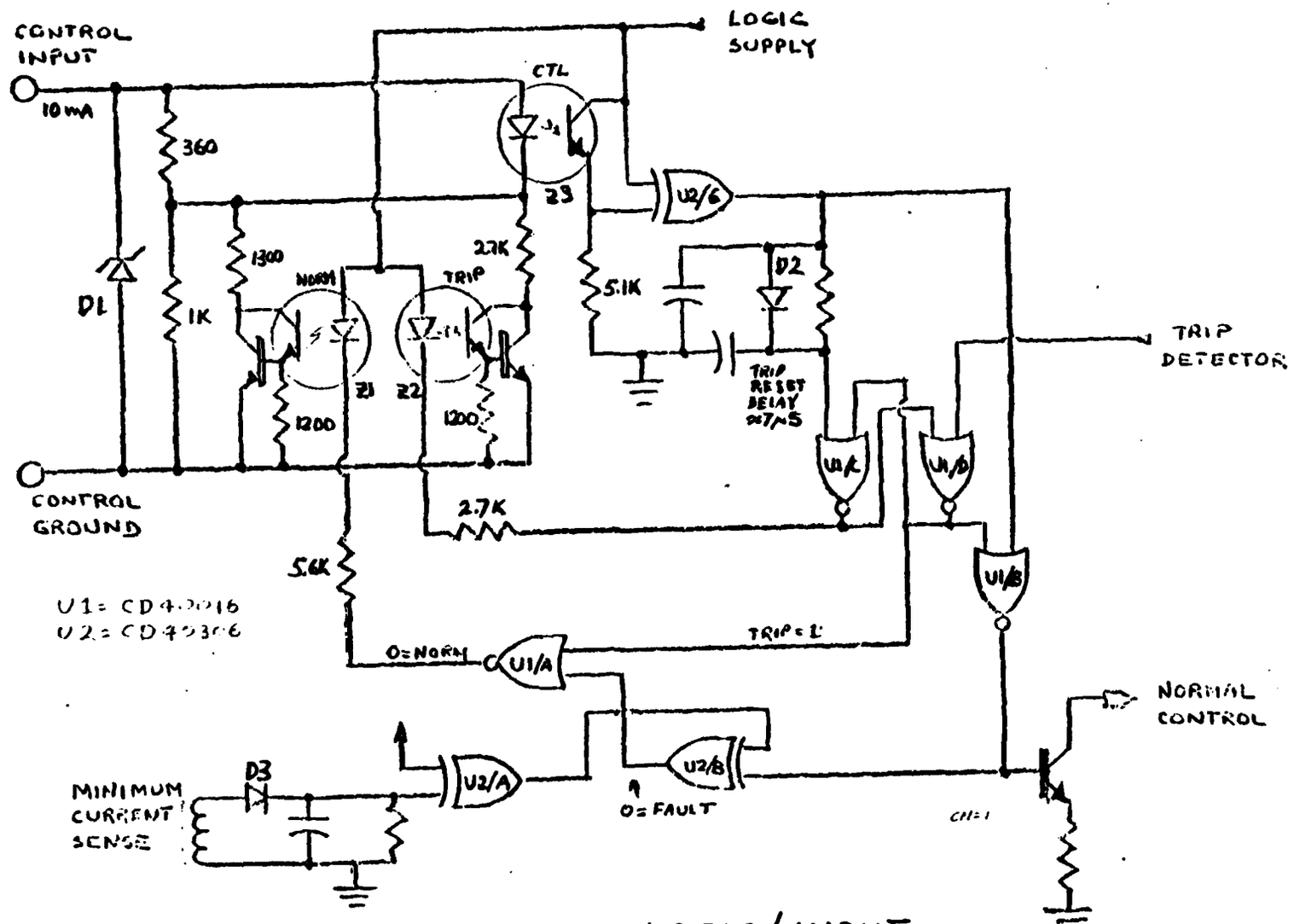


FIGURE 1.10 CONTROL LOGIC/INPUT

1.4 INPUT ISOLATION

Due to size and weight constraints, optocouplers using dual in-line packaging (DIP) cannot be used. Opto-couplers in TO-18 size packages offer the advantages of small size and wide operating temperature range, but generally are not as efficient as the DIP units. Another spec imposed constraint requires 1000 V AC isolation between control and power sections. This further limits opto-coupler selection.

A specification constraint imposed on the input circuit operation is that the BIT signal level must be stabilized within 20 μ seconds after the 10 ma control signal is applied. Previous circuits which use low levels of LED current for opto-coupler in the ON state have had difficulty in meeting the BIT response time over the full temperature range. In order to improve the opto-coupler speed characteristic without increasing the power allocated to drive the opto-coupler, it is suggested that a lower source voltage and therefore, high forward LED current be used for opto-coupler control. This will allow lower value emitter resistors to be used with the photo-transistor which will decrease the effective RC time constant that causes the BIT response lag.

If TIL-120 opto-couplers are used in the input circuit, the single logic supply system could still be used efficiently, since these opto-couplers have better transfer characteristics than the OPI-121 isolators. The disadvantage of the TIL parts is that they will provide only 1000 V DC isolation between the control and power

sections. It is believed that the 1000 V DC potential provides adequate isolation properties; therefore, it is suggested that the specification data sheet explicitly state this isolation limit so that the simpler input circuit could be implemented.

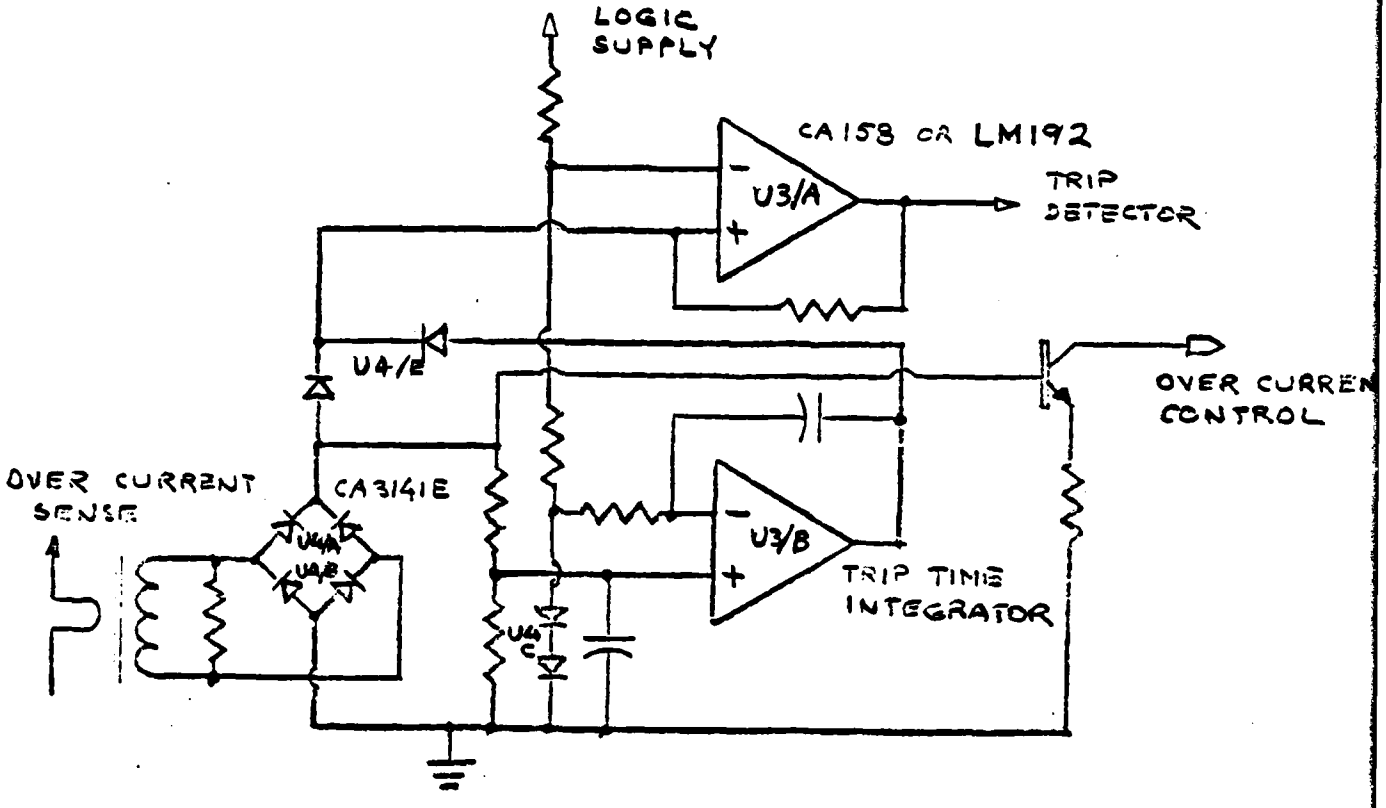


FIGURE 1.11 CONTROL TRIP SENSE

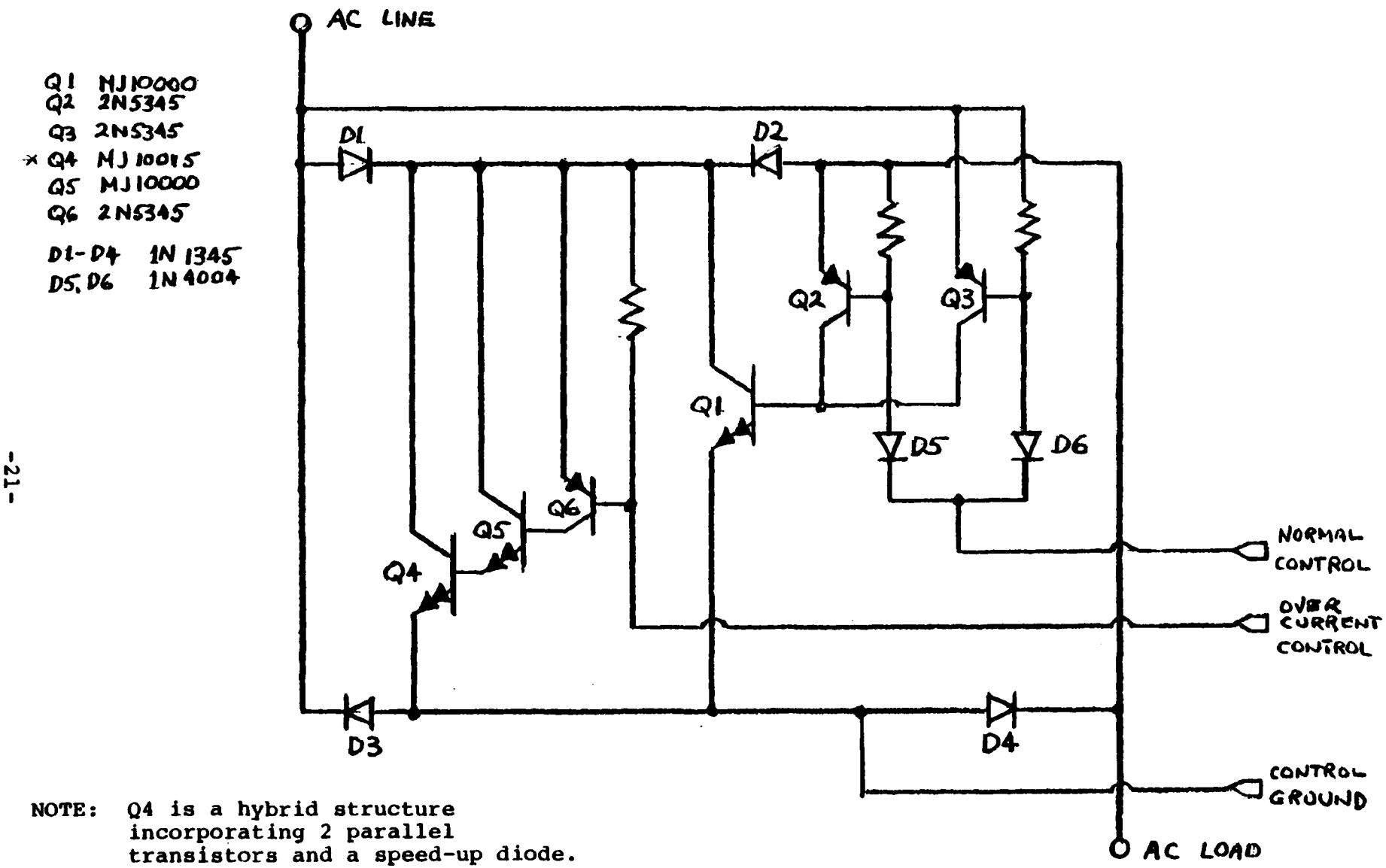
1.5 5A POWER SWITCH

A full wave bridge type of output stage, as shown in schematic diagram, Figure 1.12, would be used in the power switch in order to minimize the DV offset voltage and to also reduce the high power transistor part count.

Specification requirements dictate that the controller must not have a voltage drop greater than ≈3.0V when passing rated load curre In order to achieve this goal with power devices that were considered, and to reduce the burden of driving power from the control, the collector of the drive transistor must be sourced at a higher potential than that of the collector of the pass transistor. This could be accomplished by using two separate drive transistors so that only one is active each half cycle. The emitter of each PNP driver is connected to the anode of the rectifying diodes on the line and load side of the bridge, there obtaining approximately 8 volts advantage when driving the pass transistor. With this technique, the total drop across the power switch would be approximately 2.8 volts.

For operation during an overcurrent condition, a parallel pass transistor is enabled to share the output current. The voltage across the controller is unspecified during overcurrent, therefore, to reduce the component count, a single drive stage is used, which operates for both half cycles.

It should be pointed out that a 10 mv maximum DC offset voltage cannot be guaranteed unless the rectifier bridge diodes are matched. To do this would greatly increase the difficulty in assembling the power switch, since the diodes used would be handled and tested in chip form. If a 1N1345 diode is used, the worst case offset voltage that may occur could be as high as approximately 200 mv



NOTE: Q4 is a hybrid structure incorporating 2 parallel transistors and a speed-up diode.

Figure 1.12 5A Power Switch Schematic

1.5.1 Power Switch Considerations

Two techniques for configuring the output stage were investigated for using the high voltage-high current power transistors under consideration. The first circuit used only one high current pass transistor for both normal operation and the overcurrent condition. This had the initial advantage of reduced part count, but could not be optimized for low voltage drop during normal operation and adequate drive capability when an overcurrent condition occurred. The second configuration consisted of separate pass stages. One stage is optimized to provide approximately a 2.8 volt drop across the switch during normal operation. The second stage would be turned on in parallel when a overcurrent supply up to 50 amps would be required.

Physical and electrical parameters for the pass transistor were examined in order to optimize the hybrid area, thermal dissipation and electrical characteristics. Transistors were selected for a breakdown voltage of greater than 250V, so that the power switch would be able to withstand the long term transients of 180V RMS for 100 ms. Operating characteristics to be compared were h_{FE} at 5A and 50A, leakage current at 120°C, saturation voltage at 5A and base emitter voltage at 5A. In order to be used in a hybrid application, the transistors examined were required to be passivated. Some manufacturers use parallel devices in their package in order to obtain the high operating current. This factor was also taken into consideration, since such devices would have to be handled in matched sets supplied by the manufacturer. Dimensions of the semiconductor area was also compared among devices.

1.6 Mechanical Design

The mechanical outline of the AC Controller is specified to be contained in a 1.5 x 1.5 x 1.1 inch volume. RCA is presenting a design which requires a 36% increase in volume. Final dimensions of AC Controller are 1.5 x 1.8 x 1.25 high, as shown in Fig. 1.13.

The weight of the Controller will correspondingly increase to 3.5 oz. Using the 5A DC Controller as a baseline

5A Controller	2.05
Additional Ht.	.65
Coils	.30
Caps	.10
Component Bd	.35
	3.45 oz.

The internal design, see Fig. 1.15, of the AC Controller consists of a base and termination assembly, the power switch hybrid, which is directly attached to the base, a component mounting board and a back-to-back hybrid assembly which are attached to the internal termination standoffs. A deep drawn cover encloses the entire electomechanical assembly.

The AC Controller is similar to the DC Controller in configuration with the following exceptions.

1. The 4 corner terminals are on a .900 x 1.400 rectangle. This configuration provides a number of advantages:
   a. Terminals are on .450 centers, which will solve the hermeticity problem encountered in the DC Controller design.

b. Maximize the area of the power switch hybrid (1.00 x 1.20).

c. Decrease the thermal density of the controller mounting base.

2. The power switch beryllia substrate is solder mounted directly to the controller base. The controller thermal load produces an average thermal density of 18 watts/sq. in., with peak localized densities which are 5 times higher.

3. A component mounting board 1.25 x 1.50, which will mount large devices, as shown in Fig. 1.14. The items on this board have to be mechanically attached to the board and materials selected for this purpose carefully monitored for their compatibility with the active devices.

4. Two back-to-back mounted hybrids which will be the same size as the component mounting board. The DC power supply will be the top hybrid while control circuitry is located on the bottom hybrid. The opto-couplers, which had been edge mounted in the DC Controller, will be directly mounted to the surface of the control hybrid. Positioning of these devices (TO-18) will be coordinated with the locations of the discrete components located on the component mounting board so as to minimize the height of the overall assembly.

5. In order to ruggedize the unit for the severe vibration requirement, four shear panels will be attached to the edges between elevations .365 and 1.065, see Fig. 1.15. Particular concern will be exercised in mounting of all discrete components, also as the treatment of the basic structure.

A mechanical mock-up will be developed, as was done in the DC Controller design, and vibration testing of the concept will be completed before any final commitment to a design.

PIN	FUNCTION
1	PWR IN
2	PWR GRD
3	PWR OUT
4	CONT GRD
5	CONT

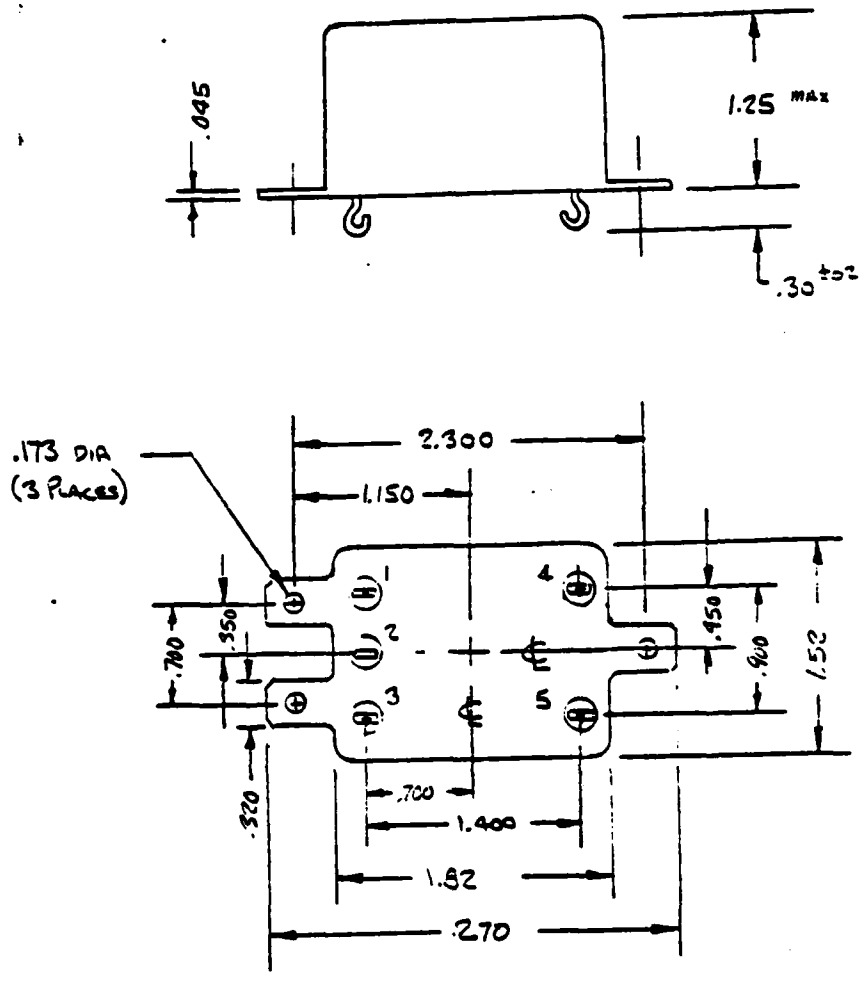
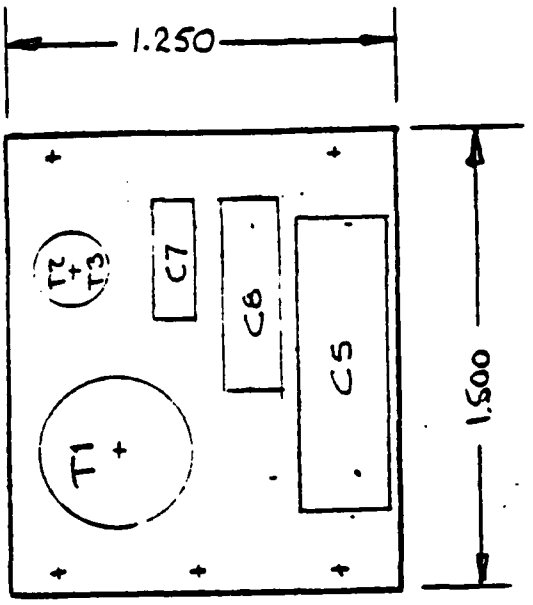


Fig. 1.13. AC Power Controller Outline & Mounting



COMPONENT	HEIGHT
T1	.40
T2	.25
T3	
C5	.281
C7	.135
C8	.188

Fig. 1.14. Component Board

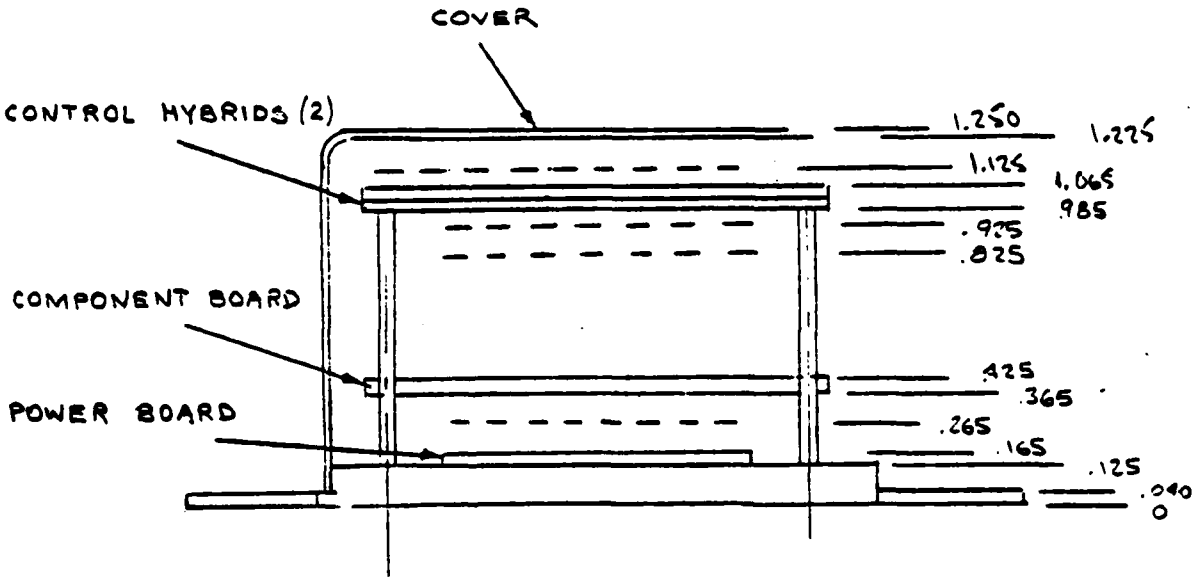


Fig. 1.15. AC Power Controller Vertical Section

Reference Appendix 3.8

1.7 Conclusions to 115V SSPC AC Feasibility Study

The following conclusions are made:

1. A simplification of the auxiliary power supply is possible (see Fig. 7) if a digital control circuit such as Rockwell International Pub. No. P77-883/201 could be adapted instead of analog circuit developed by RCA for DC SSPC. This analog circuit requires highly regulated with low ripple voltages which are isolated from the input control circuit and from AC main power.

   The application of the existing digital control CMOS/SOS/LSI chip would require change of the turn on/off times requirements of 1.5 ms/2.0 ms specification to a zero voltage turn on/off.

2. An elimination of the auxiliary power supply by providing an external DC source for circuitry control, will substantially increase reliability of the SSPC and decrease the cost of the unit.

3. The basic dimensional size of the AC Controller is 1.50 x 1.80 x 1.25, exclusive of mounting and termination devices, and the unit weighs 3.5 oz. RCA has considered all mechanical problems, as imposed by the required circuitry and environmental conditions, in specifying these parameters.

4. The feasibility of packaging concept must be demonstrated through working hardware, where cost and altering specifications could be considered. This is evident in Figure 1.16 which illustrates the increased cost per unit when package size is decreased.

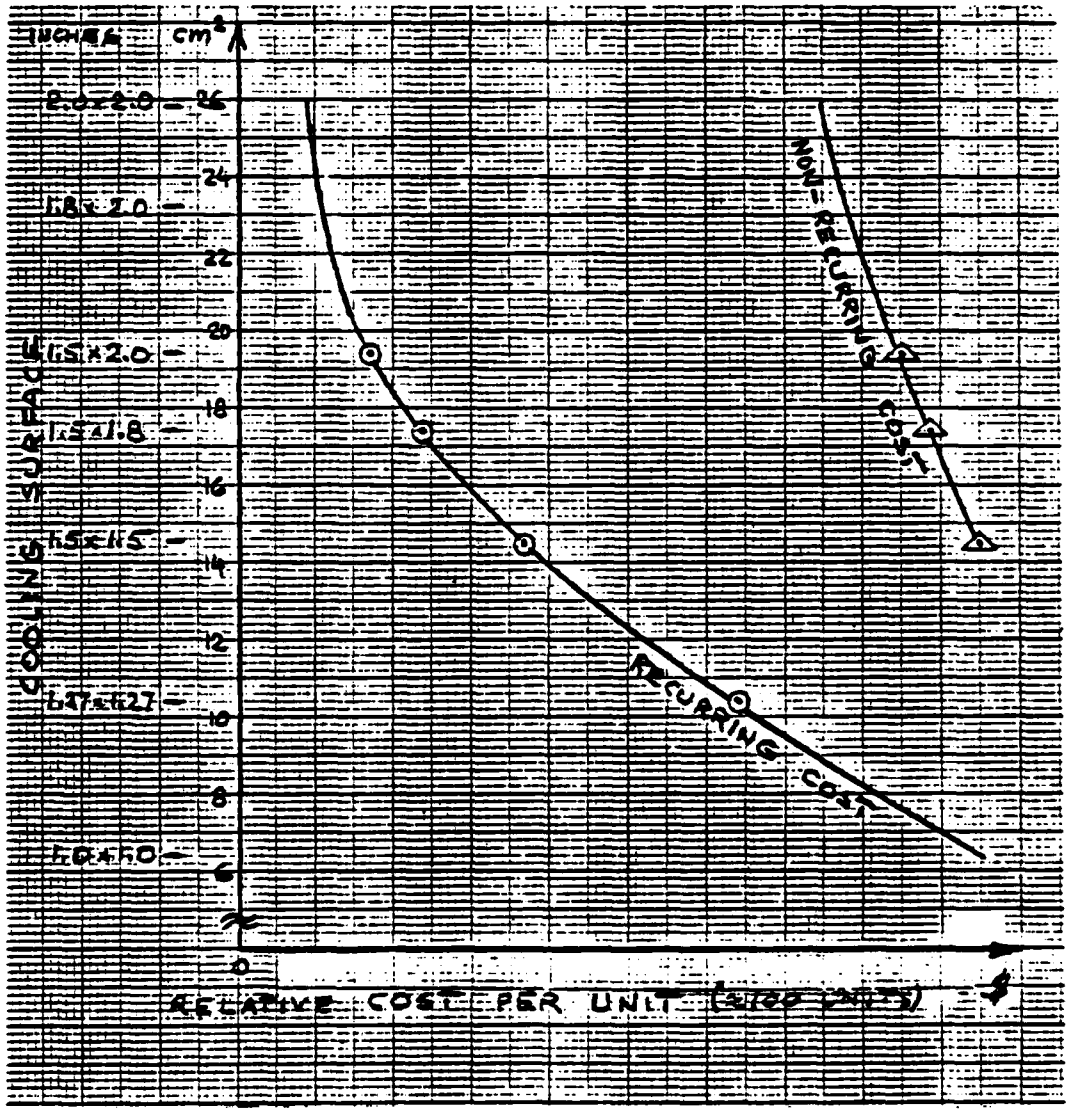


Figure 1.16. Projected Cost/Unit vs. Cooling Surface

2.0 26 VAC POWER CONTROLLER

2.1 Design Considerations

The feasibility of designing a 26V AC Power Controller at 1A current rating in specified module size, (NADC-30-TS-7602/05) is more realistic than a 115V AC part. Mainly, because 26V controller operates at lower power level and operates with zero voltage turn on/off. Small and efficient circuit can be used employing MOSFET transistors and SCHOTTKY diodes. Also, smaller internal power supply can be realized using digital control system to operate and monitor power switch stage.

Power controller feasibility study is broken down into four sections represented in the block diagram of Figure 2.1.

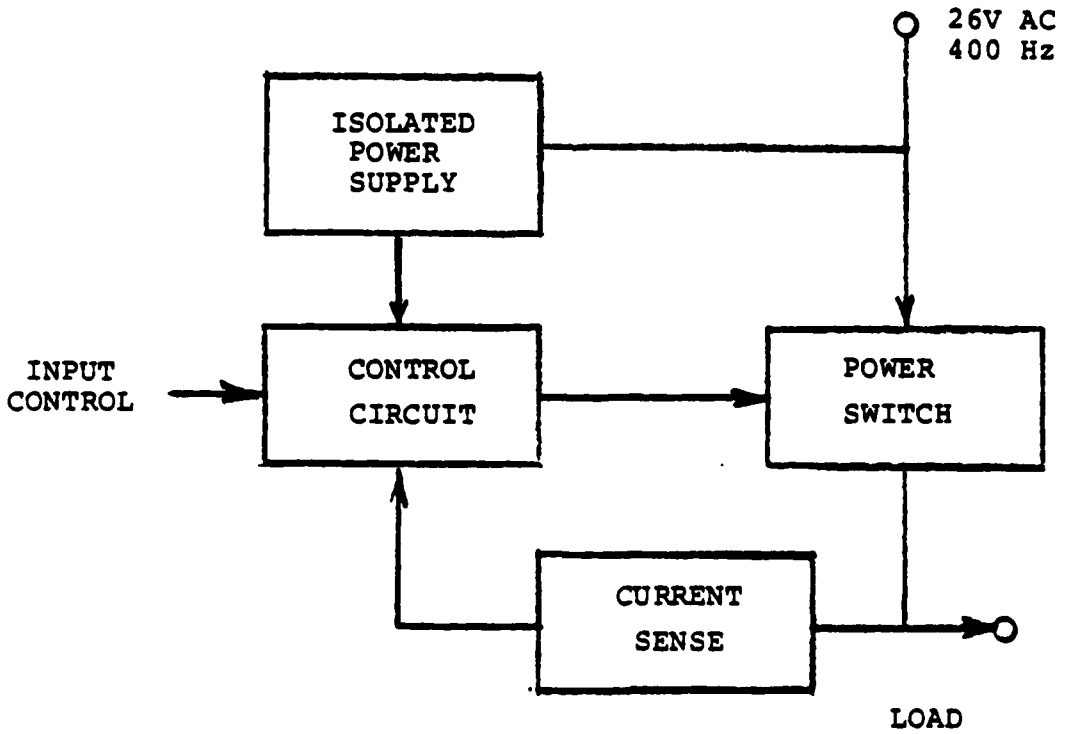


Figure 2.1. 26V Power Controller, Block Diagram

2.2 Power Switch

One serious limitation of the power transistor in AC controller concerns the secondary breakdown energy which severely limits peak current rating of the device when the voltage is high during fault clearing condition. This disadvantage can be eliminated by using power FET. Since the temperature coefficient of the MOS FET drain to source on voltage is positive (a bipolar transistor has negative coefficient), MOS FET draws less current as the device heats up. If the current density increases at one particular point of the channel, the temperature rises and the current decreases. The current automatically equalizes through the chip, so no hot spots are developed. Similarly, current is automatically shared between parallel devices so no ballasting resistors are needed. The other advantages of MOS FET transistors are: a) switching delay time is small, several nanoseconds, about 10 to 200 times faster than a bipolar transistor; b) high input impedance low drive current (typically less than 100 nA) therefore, MOS FET will directly interface with CMOS logic; c) lack of failure from secondary breakdown means that it can withstand high voltage and high current simultaneously, (see Fig. 2.2) so inductive loads are no problem. Two types of MOS FET power transistors are considered for 26V AC Power Controller:

International Rectivier	IRF100	80V @ 16A
Siliconix	VN64GA	60V @ 15A

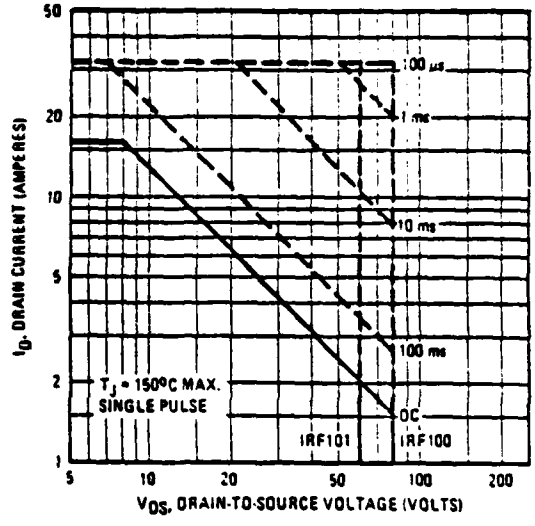


Fig. 2.2. IRF100 – Maximum Safe Operating Area

To simplify the control circuit design or to adapt a digital control circuit, such as Rockwell International Pub. No. P77-883/201, the full-wave bridge configuration shown in Fig. 2.3 will be used. This configuration allows a single

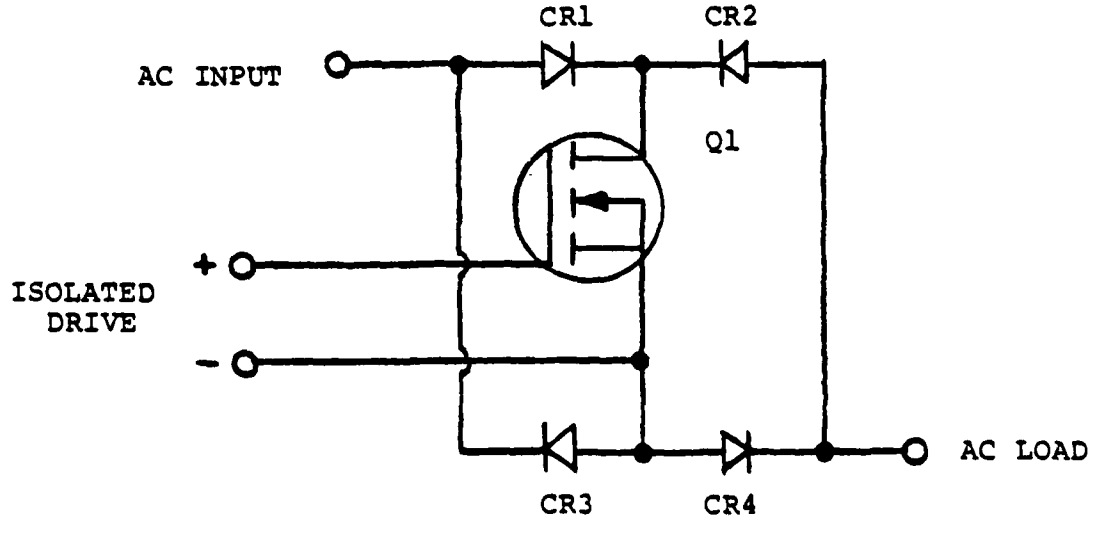
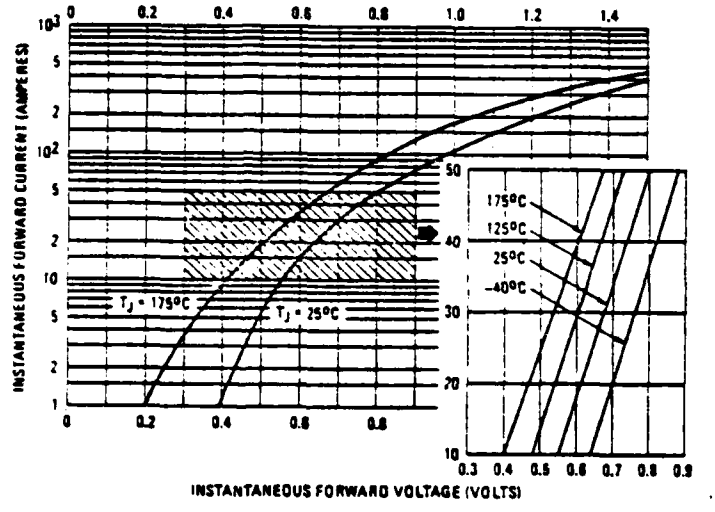


Figure 2.3. Full-Wave Bridge Power Stage

transistor to be used, therefore, minimum DC offset voltage is generated. Voltage drops during nominal current conduction of 1A may reach 2.5V if silicon diodes are used. To meet 1 5V RMS maximum requirements power Schottky diodes are considered for this application using 1N6096 (TRW) or 30FQ045 (International Rectifier) devices with characteristics as shown in Figure 2.4 below.



Maximum Forward Voltage Vs. Forward Current

Figure 2.4. Schottky Diode 30FQ045
Forward Voltage Characteristics

2.3 CONTROL CIRCUIT

2.3.1 Control Circuit Considerations

The control circuit operation requirements for the 26V AC controller differs slightly from the specification requirements for the 115V unit previously described. The 26V controller operation, as characterized in Spec. No. NADC-30-TS-7602/05 would turn on only at the input zero voltage crossing and would turn off at the load zero current crossing. In order to implement these functions, the control circuitry used in the 115V controller could be modified by adding the current and voltage sensing functions plus the logic gating to allow proper turn-on and turn-off.

Another design alternative would be to base the control circuit on the use of a CMOS/SOS/LSI chip developed by Rockwell International Autonetics Group. This is designated as CMOS device 30351 and is described in Rockwell Pub. No. P77-883/201 (included in Appendix) and can perform most of the controller's required monitoring, timing and control functions. In order to incorporate this IC however, two of the NADC specified response times would have to be increased. Because of the internal circuit operation, the turn on signal for the power switch is delayed for 5 m seconds. Including the worst case conditions for line voltage zero crossing at 400 Hz, and the delay through the control input circuitry, the turn on time/turn on delay would, therefore, be between 5 ms and 6.5mseconds. Similarly, since the circuit will only allow the controller to turn off during the positive going, zero load current condition, the

turn off delay would be from 5 ms to 7.75 ms, as shown in Figure 2.5.

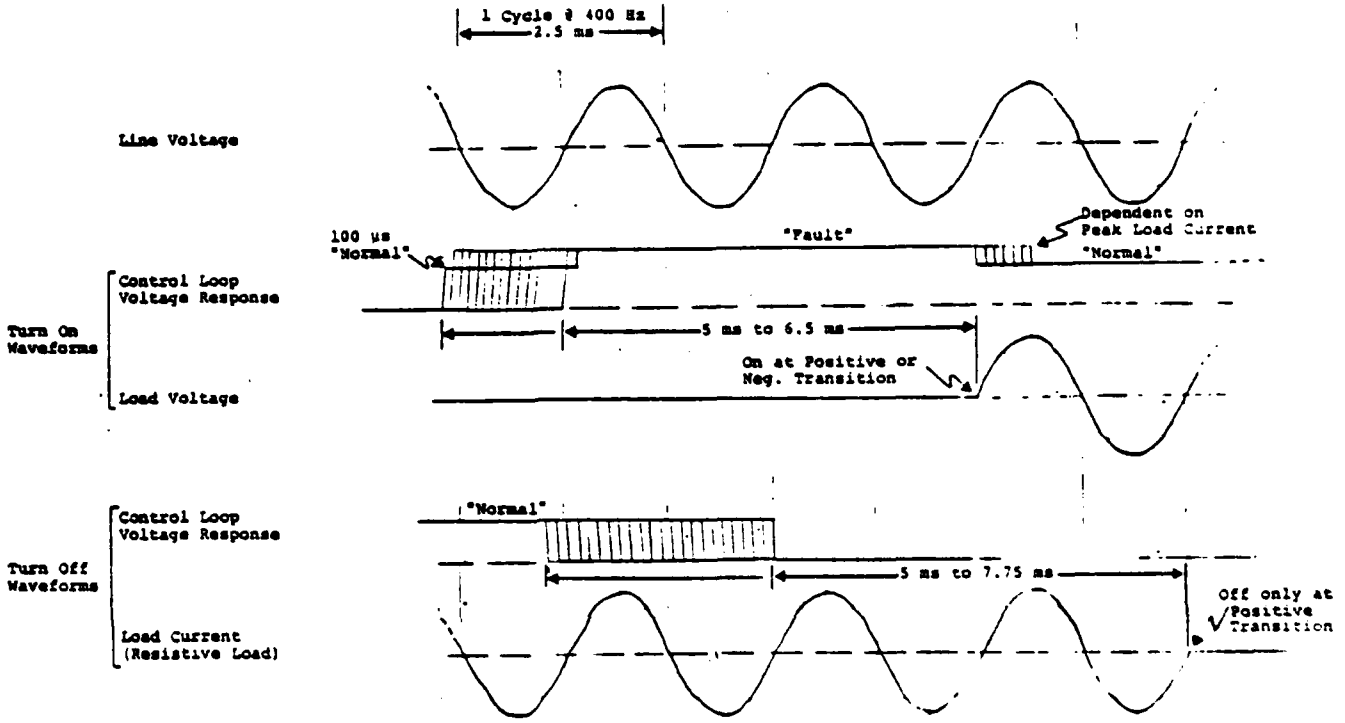


Figure 2.5 Controller Response Time with Rockwell LSI

2.3.2 Control Circuit Design

A control system based on the controller LSI chip requires auxiliary circuitry to properly interface with input and power switch subcircuits. The minimum peripheral interface functions are shown in Fig. 2.6.

The LSI chip requires +12V and -12V supply voltages for proper operation. The auxiliary support IC's would also be supplied from the +12V rail.

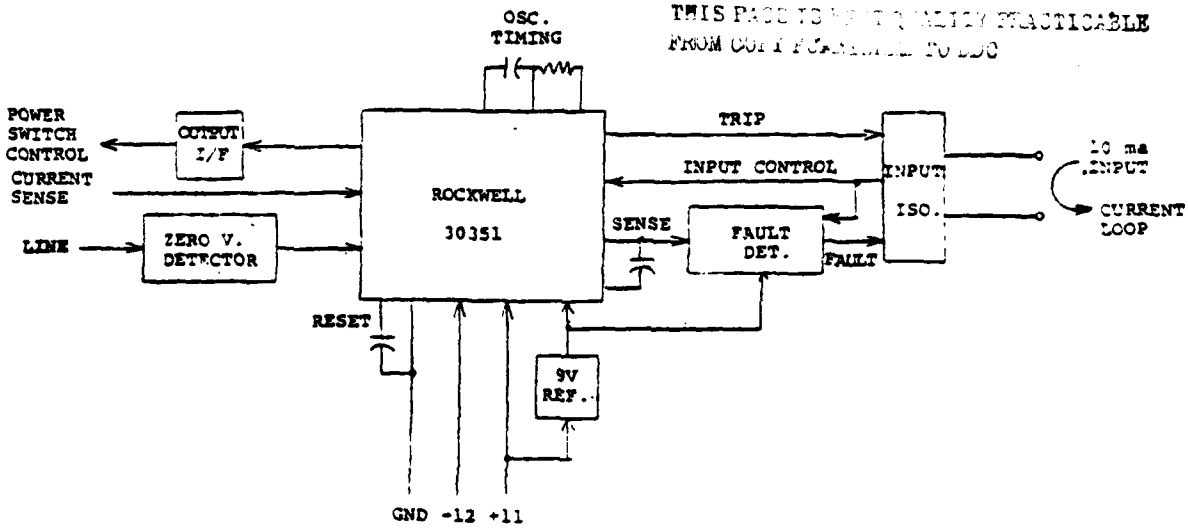


Figure 2.6 Control Circuit Functional Diagram

The input circuitry previously described for 115V AC controller, could interface directly with the trip and control signal lines of the LSI chip. In order to derive the fault signal however, the control signal and an intermediate sensed output would have to be processed and compared as shown in Figure 2.6A.

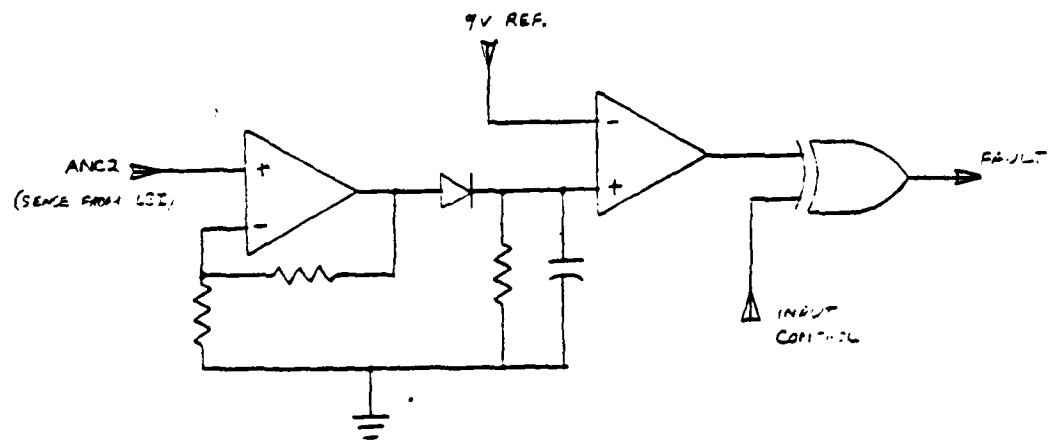


Figure 2.6A Fault Detection Circuit

This circuit will detect and hold for 1.25 msec (90°), the minimum current state. This is necessary if normal zero current crossings are not to generate false fault signals every 180°. Because of this lag, and also due to the delay before turn off, a fault output would exist for 6.25 to 9 msec. Although this would not normally be detected due to the removal of the input control current, subsequent interrogation pulses would indicate the fault state during this interim period, after the control signal is removed. The fault signal would also be generated at turn on for the 5 ms to 6.5 ms latency period between control application and power switch turn on to the peak minimum current level.

The other auxiliary circuit functions could be performed by the addition of just a few additional components. The 9V reference level is derived from the +12V supply line by the use of a zener diode reference, an op-amp and a transistor current source. The line voltage zero crossing detector would be constructed from a rectifier chip and a clipping buffering stage. The interface to the power switch would be achieved by a level conversion stage.

2.4 Internal Power Supply

A small power supply can be provided by using energy pump regulator shown in Figure 1.5. The 26V AC power is rectified in a full-wave bridge to DC and then converted to a pre-regulated ± 12V DC. The intermediate switching frequency is 40 kHz. The number of components is the same as shown in Figure 1.7, although voltage requirements for numerous parts

are diminished since this power supply operates from 26V AC instead of 115V AC.

An alternative approach to power supply is to use 400 Hz transformer, rectifiers, filters and series dissipating regulators. This method requires fewer components and may be less expensive, although power dissipation in regulators and large size of the transformer will present packaging problems.

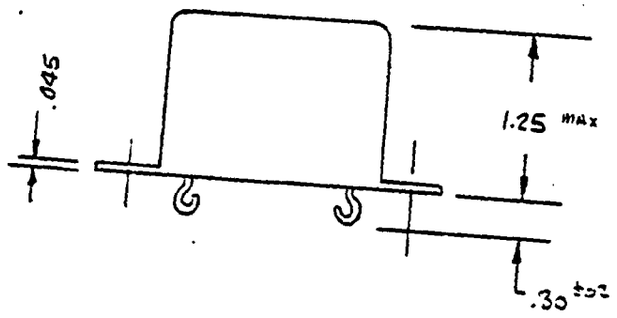
2.5 Current Sensing

Continuous current sensing is provided by current transformers. It will detect current level needed to determine the fault state and over-current trip range. A single coil will be used which may be placed over the output terminal. This coil will provide DC isolation from AC load line, yet it will be capable of sensing both positive and negative pulses.

2.6 Mechanical Configuration

The mechanical construction of the 26v AC controller would be similar to that of the 115v unit described in 1.6. Since the area needed to construct the power switch is reduced by decreasing the component count, the base plate area for a 26v controller can be made smaller than that of a 115v unit. The minimum base plate area that could be used is determined by the glass area needed to isolate the terminal pins from the header plate under the worst case conditions of high altitude and high voltage required by MIL-STD-202E test condition D. This would allow a base plate area of 1.5 X 1.5 inches as shown in Figure 2.7.

PIN	FUNCTION
1	PWR IN
2	PWR GRD
3	PWR OUT
4	CONT GRD
5	CONT



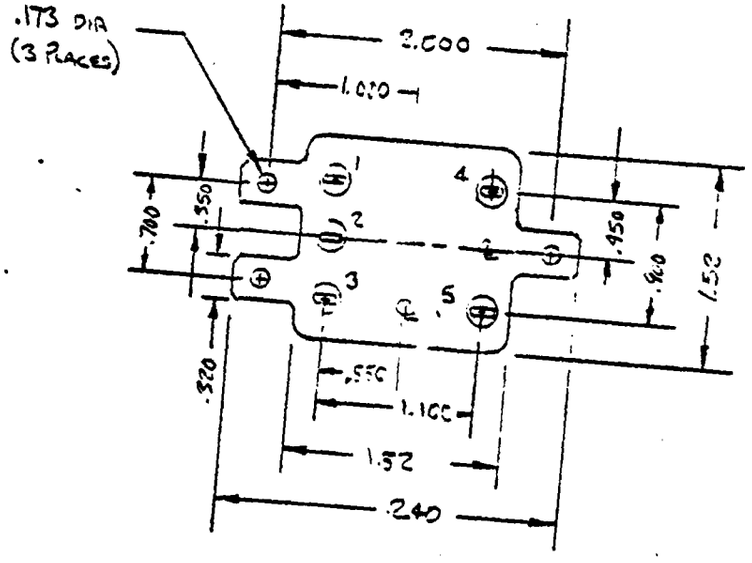


Figure 2.7. 26V AC SSPC Mechanical Configuration

The vertical arrangement of the subassemblies would be the same as that shown for a 115v unit in Figure 1.15. The reduced component count realized by using a Rockwell LSI control chip would keep the control layout density approximately the same as that of the 115v controller type, since the control hybrid area also would decrease if the base plate dimensions are reduced. The smaller base plate area would also decrease the controller weight to approximately 3 ounces.

The above construction technique is similar to that used for previously produced 28v DC controller as shown in Figure 2.8.

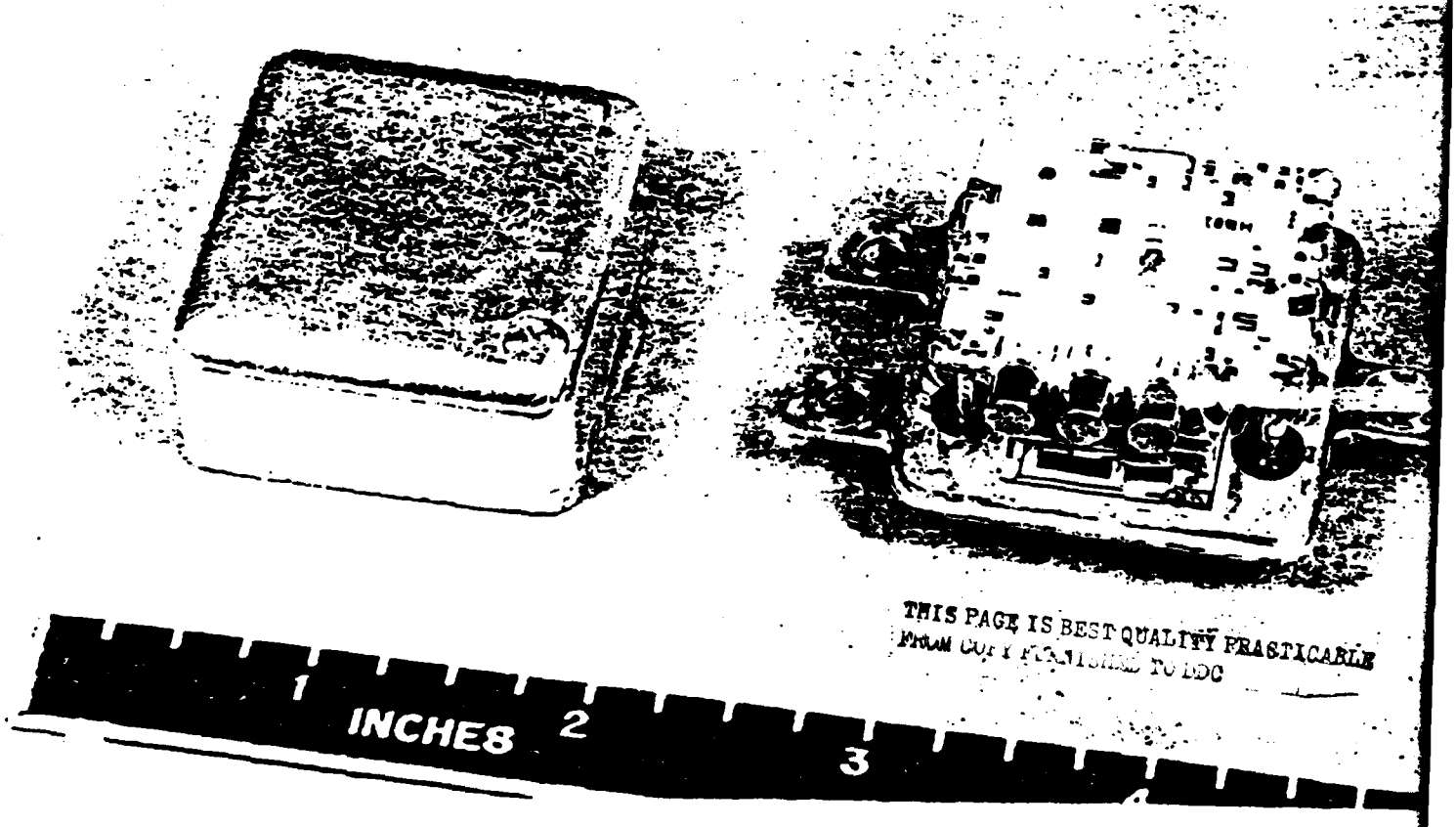


Figure 28 DC Controller Construction

2.7 Conclusions to 26 VAC SSPC

1. Some engineering would be needed to make improvements in the unit assembly.

2. The resulting device would fill most requirements but an effort should be made to reduce cost by simplifying an internal power supply and control circuit designs.

3. Recent improvement of power FET transistor and Schottky diodes with respect to their switching characteristics and current rating, have made possible to adopt these devices for 26V SSPC at 1A application. The MOSFET transistor proposed for this application is under development with several vendors and farther current rating increase is possible, thus, future design of a 5A SSPC is promising.

4. The Rockwell chip would reduce control circuit component count, thus, simplifying fabrication and increasing reliability. In order to use this LSI, the specification limits for response time would have to be increased.

5. The weight of the controller would be approximately 3.0 ounces. Mechanical construction would be similar to the DC Power Controller shown in Figure 2.8.

3.0 APPENDIX

3.1 Drive System, Internal Power Supply

Electrical Analysis

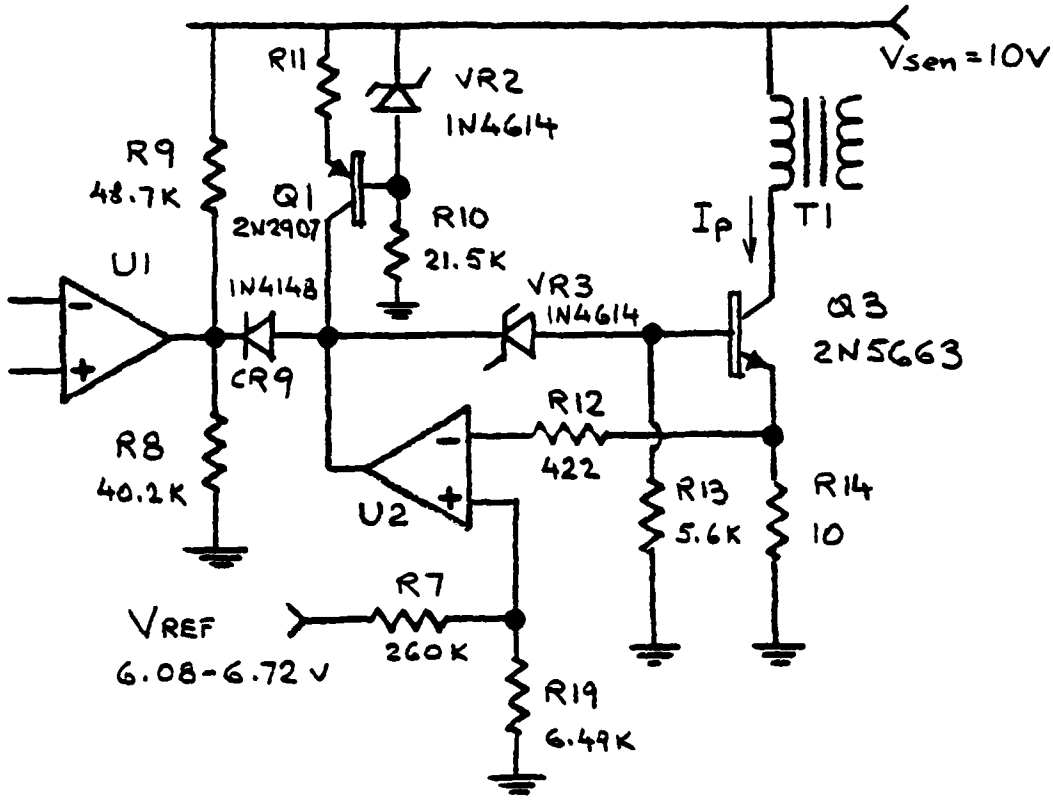


Figure 3.1. Drive System Schematic

Peak current threshold will occur where :

$$I_{E3} \; R_{14} \gg V_{U2(+)}$$

$$IT_1 = \frac{V_{U2(+)}}{R14} \left(\frac{h_{FE3}}{1 + h_{FE3}} \right)$$

$$\bar{V}_{ref} = 6.72V \qquad \underline{V}ref = 6.08V$$

$$\underline{I}_p \text{ (required)} = 14.8 \text{ mA} \quad \text{(See transformer design)}$$

$$V_{R14} = I_p \times R_{14} = 14.8 \times 10 = 148 \text{ mV} = V_{R19}$$

$$I_{R19} = \frac{148 \times 10^{-3}}{6.49 \times 10^{3}} = 22.8 \text{ uA}$$

$$R_7 = \frac{V_{ref} - V_{R19}}{I_{R19}} = \frac{6.08 - 0.148}{22.8 \times 10^{-6}} = 260 \text{ K}$$

$$I_{T1} = \frac{0.148}{10} \left(\frac{20}{1 + 20} \right) = 14 \text{ mA}$$

$$I_{B3} = \frac{I_{T1} + I_{R13}}{\beta 3} = \frac{14 + \frac{0.7 + 0.148}{5.6}}{20} = 0.7 \text{ mA}$$

$$R_{11} = \frac{V_{R2} - V_{BE1}}{I_{B3}} = \frac{1.8 - 0.6}{0.7 \times 10^{-3}} = 1714 \ \Omega$$

3.2 Housekeeping Current Requirement

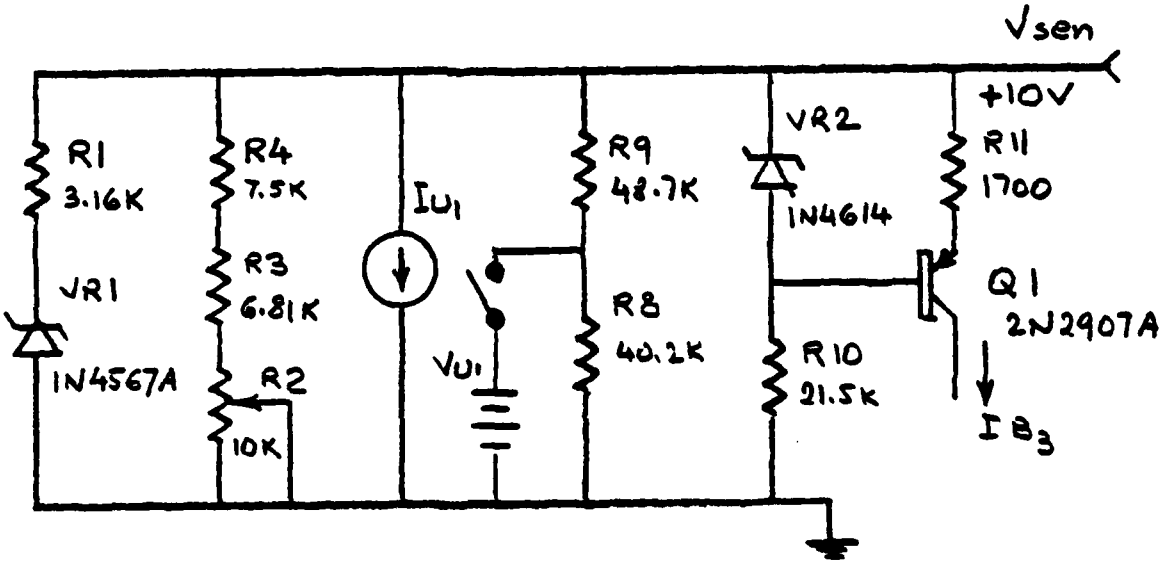


Figure 3.2. Housekeeping Current

$$I_{VR1} = \frac{V_{sen} - V_{VR1}}{R_1} = \frac{10 - 6.4}{3.16 \times 0.98} = 1.162 \text{ mA}$$

$$I_{R4} = \frac{V_{sen}}{R4 + R3} = \frac{10}{(7.5 + 6.81)0.98} = 0.713 \text{ mA}$$

$$I_{U1} = 2 \text{ mA} \qquad I_{B3} = 0.7 \text{ mA}$$

$$I_{R9} = \frac{V_{sen} - V_{U1}}{R9} = \frac{10 - 0.1}{48.7 \times 0.98} = 0.207 \text{ mA}$$

$$I_{VR2} = \frac{V_{sen} - V_{VR2}}{R10} = \frac{10 - 1.8}{21.5 \times 0.98} = 0.389 \text{ mA}$$

$$\bar{I}_{sen} = I_{VR1} + I_{R4} + I_{U1} + I_{B3} + I_{R9} + I_{VR2} = \underline{5.172} \text{ mA}$$

$$\bar{R}_{18} = \frac{\underline{V}_{in} - \bar{V}_{CE4} - \bar{V}_{sen}}{\bar{I}_{sen}} = \frac{150 - 0.4 - 10}{0.00517} = 27 \text{ K}$$

$$R_{17} = \frac{\bar{V}_{in} - \underline{V}_{VR4}}{0.001} = \frac{160 - 8.2}{0.0005} = 304 \text{ K}$$

$$P_{R17} = 0.0005^2 \times 330000 = \underline{82.5} \text{ mW}$$

3.3 Current Transformer XT-14116

Assume: nominal current = 5A RMS

max. = 50A → 11V

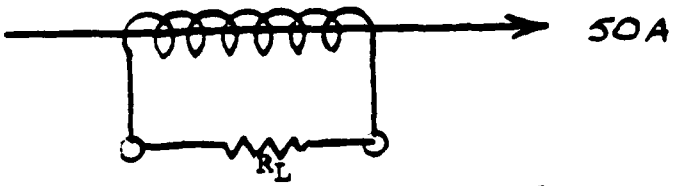


Figure 3.3. Current Transformer

if I_L = 0.1A @ 50A (buss current)

$$N_{sec} = \frac{50}{0.1} = 500 \text{ turns}$$

$$R_L = \frac{11}{0.1} = 110\ \Omega$$

$$V_{R_L\ (5A)} = \frac{5}{500} \times 110 = 1.1V$$

$$P_{R_L} = \frac{1.1^2}{110} = 11 \text{ mW}$$

$$I_L = \frac{5}{500} = 0.01A$$

Use #41 Awg. wire

Wire buildup = 11.6 x 500 = 5800 c mils

$$K = \frac{5800}{14400} = 40\%$$

CORE: YW-40603-TC MAG. INC.

OD = 0.230
ID = 0.120
H = 0.125

3.4 Power Transformer Design (XT-14115)

Assume: P_o = 400 mW, efficiency = 70%

Pin = $\frac{400}{0.7}$ = 571 mW

E_p = 140V

f = 40 kHz

From equation (3) $I_p = \frac{tc\ E_p}{L_p}$

$tc = \frac{1}{2f} = \frac{1}{2 \times 40 \times 10^3} = 12.5$ uS

$L = \frac{140^2}{8 \times 0.571 \times 40 \times 10^3} = 107$ mH

$Ip = \frac{12.5 \times 10^{-6} \times 140}{107 \times 10^{-3} \times 1.1} = 14.8$ mA

if 2 x 55037-A2 cores are used:

$N_{pri} = 1000 \sqrt{\frac{107}{210}} = 714$ turns

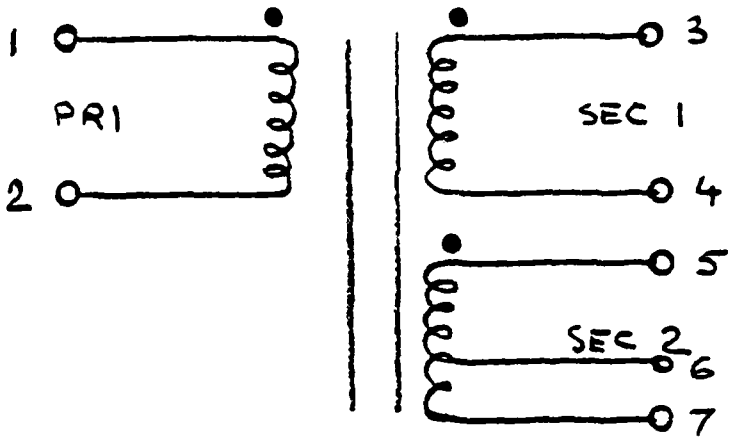


Figure 3.4. Power Transformer

$V_{sec\ 1} = V_{sec\ 2} = 10V$

$N_{sec} = \frac{10 \times 714}{140} = 51$ turns

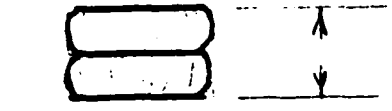
$B_m = \frac{V \times 10^8}{4 \times f \times N \times A} = \frac{160 \times 108}{4 \times 40 \times 10^3 \times 714 \times 0.2} = 700$ gauss

$I_{pri} = \frac{0.571}{140} = 4$ mA use #42 AWG wire

$I_{sec\ 1}$ = 4 mA use #42 AWG wire

$I_{sec\ 2} = \frac{0.4}{10}$ = 40 mA use #34 AWG wire

$K = \frac{10.2\ (51+714)+60.8\times51}{32400}$ = 0.336 < 0.4 O.K.



2(0.156 + 0.044) = 0.40"

0.4 + (2 x 0.05) = 0.5"

Weight = 2 x 1.9 + 2 = 5.8 grams

Available power can be determined from equation (9)

$$P = \frac{E_p I_p}{2\left(1 + \frac{E_p N_s}{N_p E_s}\right)} = \frac{140 \times 14.8 \times 10^{-3}}{2\left(1 + \frac{140 \times 51}{714 \times 10}\right)} = 518\ mW$$

3.5 Filter Capacitors

$$C = \Delta i \times \frac{\Delta t}{\Delta u}$$

where: i = current variation due to load change = 40 mA

t = circuit response time = 25 uS

u = allowable voltage change = 0.1V

$$C_7 = \frac{0.04 \times 25 \times 10^{-6}}{0.1} = 10\ uF\ at\ 20V$$

$$C_6 = \frac{0.004 \times 25 \times 10^{-6}}{0.1} = 1\ uF\ @\ 20V$$

$$C_5 = \frac{0.004 \times 4 \times 25 \times 10^{-6}}{0.5} = 0.8\ uF\ @\ 200V$$

3.6 Tentative List of Parts

3.6.1 Auxiliary Power Supply 115V AC SSPC

DESIGNATION	PART NO.	DESCRIPTION	RATING
C1	M39014/01-1474	Capacitor	0.1 uF
C2	M39014/01-1225	↓	220 pF
C3	M39014/01-1450	↓	4700 pF
C4	M39014/01-1225	↓	220 pF
C5	M39018/01-0668	↓	3.3 uF/200V
C6	M39014/02-1407	↓	1 uF
C7	M39003/06-0067	↓	10 uF/35V
C8	M39003/06-0001	↓	10 uF/6V
CR1-CR4	1N5616	Diode	
CR5	1N4148	↓	
CR6-CR8	1N5802 1N4148	↓	
Q1	2N2907A	Transistor	
Q2	2N2222A	↓	
Q3	2N5663	↓	
Q4	2N3439	↓	
VR1	1N4567A	Zener	
VR2	1N4614	↓	
VR3	1N4614	↓	
VR4	1N4101	↓	
T1	XT-14115	Transformer	RCA
T2	XT-14116	Current Transf.	RCA
U1	LM 193A	Dual Comp.	

3.6.2 Tentative List of Parts 26 VAC SSPC

Internal Power Supply

Designation	Part No.	Description	Rating
C1	M39014/01-1474	Capacitor	0.1 uF
C2	M39014/01-1225	↓	220 pF
C3	M39014/01-1450		4700 pF
C4	M39014/01-1225		220 pF
C5	M39003/06-0067		10uF/35V
C6	M39014/02-1407		1 uF
C7	M39003/06-0049		3.9uF/20V
C8	M39003/06-0049		3.9uF/20V
CR1-CR4	1N5804	Diode	
CR5	1N4148	↓	
CR6-CR8	1N5802		
CR9	1N4148		
Q1	2N2907A	Transistor	
Q2	2N2222A	↓	
Q3	2N5337		
Q4	2N2222A		
VR1	1N4567A	Zener	
VR2-VR3	1N4614	↓	
VR4	1N4101		
T1	XT-14117	Transformer	RCA
T2	XT-14118	↓	RCA
U1	LM193A	Dual Comparator	National

PRELIMINARY DEVICE DESCRIPTION

Rockwell International

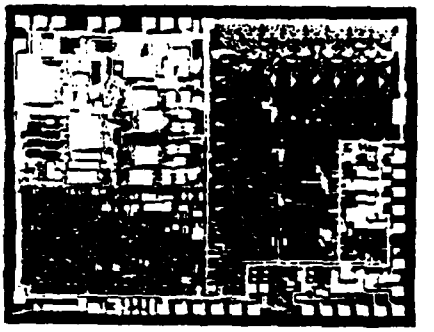
CMOS/SOS/LSI SOLID STATE POWER CONTROLLER

SPECIAL FEATURES

- On-Chip A/D-6 Bit + Sign
- On-Chip Clock Generator with External R-C Control
- Clock Output Driver
- On-Chip Test For Load Voltage Status
- Timed to Reduce Power On Transients
- On-Chip Amplifiers for Low Level Current Sense
- Design Verification Completed for Military Aircraft

TYPICAL ELECTRICAL CHARACTERISTICS

- Zener - Protected Inputs
- Full Dielectric Isolation Provided by Sapphire
- Lower Power < 200 mW
- Inputs Designed for Optimum Noise Immunity with CMOS Circuits
- ±10 VDC to ±13 VDC Bias Range
- -55°C to +125°C Operation



SSPC Photo Microgram

APPLICATIONS

The Solid State Power Controller Monolithic device is intended for use in the control and protection of aircraft electrical systems. Primary applications are the turn on/off of solid state power switches, and computation of the turn off time at which the electrical load exceeds rated current.

GENERAL DESCRIPTION

The primary function of the solid state power control monolithic device is to provide full cycle control of AC power being delivered to an electrical load. This is accomplished by controlling complementary drive outputs through which the power switches can be turned on and off. The desired time for switching the load "ON" is when the line voltage is zero and the desired time for switching the load "OFF" is when the load current is zero. This assures minimum transient on the load and cable wiring.

When primary power is applied to the monolithic circuit, all mode controls and counters are reset to a stand-by mode. The monolithic circuit will then monitor the EXCLUSIVE-OR of the two control signals and the ZERO VOLTAGE CROSSING of the 400 Hertz power.

If the "EXCLUSIVE OR" (INTERNAL LOGIC, TERM "C") of the two controls is true, a five millisecond timer is started and continuously compared with "C" for the full five milliseconds. With the "C" term remaining true, the next positive edge of the ZERO VOLTAGE CROSSING input will cause the DRIVE outputs to be enabled. These outputs may be used to turn the "POWER ON". Three alternate operating modes are possible with the drive outputs "ON". These are overcurrent fast trip, indicated by $I \geq I1$, timed overcurrent trip indicated by $I \geq I2$ and normal turn off by removal of the C term. A functional block diagram is shown in Figure 1.

The instantaneous sensed values of the current (I) being delivered to the load are digitized by the ADC, and if the ADC counter reaches full scale in either positive or negative direction then a FAST TRIP signal is generated. FAST TRIP indicates that a catastrophic overcurrent situation exists. The DRIVE outputs are immediately disabled and a TRIPOUT is generated.

In timed overcurrent tripout mode, the ADC output will be less than full scale and the length of time delay an overcurrent is allowed to exist is determined by the size of the overcurrent. Each 200 usec, one sample from the ADC (I) is used for trip computation. The sample is applied to a single pole digital filter. If any value of I equals or exceeds I2 (minimum current value that will be sensed and added to the accumulator) the accumulator will "add" the magnitude of I. However, if the sampled values of I are less than I2 then the value of I is subtracted from the accumulator. When the accumulator contents are $\geq 2^{14}$, the current vs time relationship has been met. As a result, the circuit will turn off DRIVE and turn on TRIPOUT when the load current exceeds the rated current for a time longer than that shown in Figure 2.

During normal turn off, when the "EXCLUSIVE OR" of the two controls ("C") is false the five millisecond timer is again started and continuously compared with C. With the C term remaining false, the beginning of the next negative half cycle of the load is used to turn off DRIVE. An internal "Low Level Current Sense" Comparator is provided to detect the beginning of the negative half cycle.

A voltage status capability is provided by an internal "Sense Both Half Cycles" Comparator and Status Logic. This circuitry provides for a monitor of the load voltage and generates a STATUS output only if the Load voltage is of proper magnitude and both half cycles are present. STATUS is completely independent of the remainder of the power controller functions.

CMOS/SOS integrated circuit fabrication techniques have moved the solid state power controller monolithic to the forefront of complex, sophisticated components. The monolithic benefits from an advanced but proven integrated circuit process technology which is directly responsible for the high performance characteristics obtainable in this CMOS/SOS device.

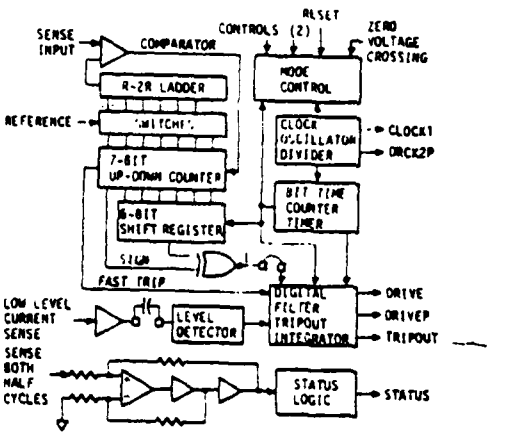


Figure 1. Block Diagram

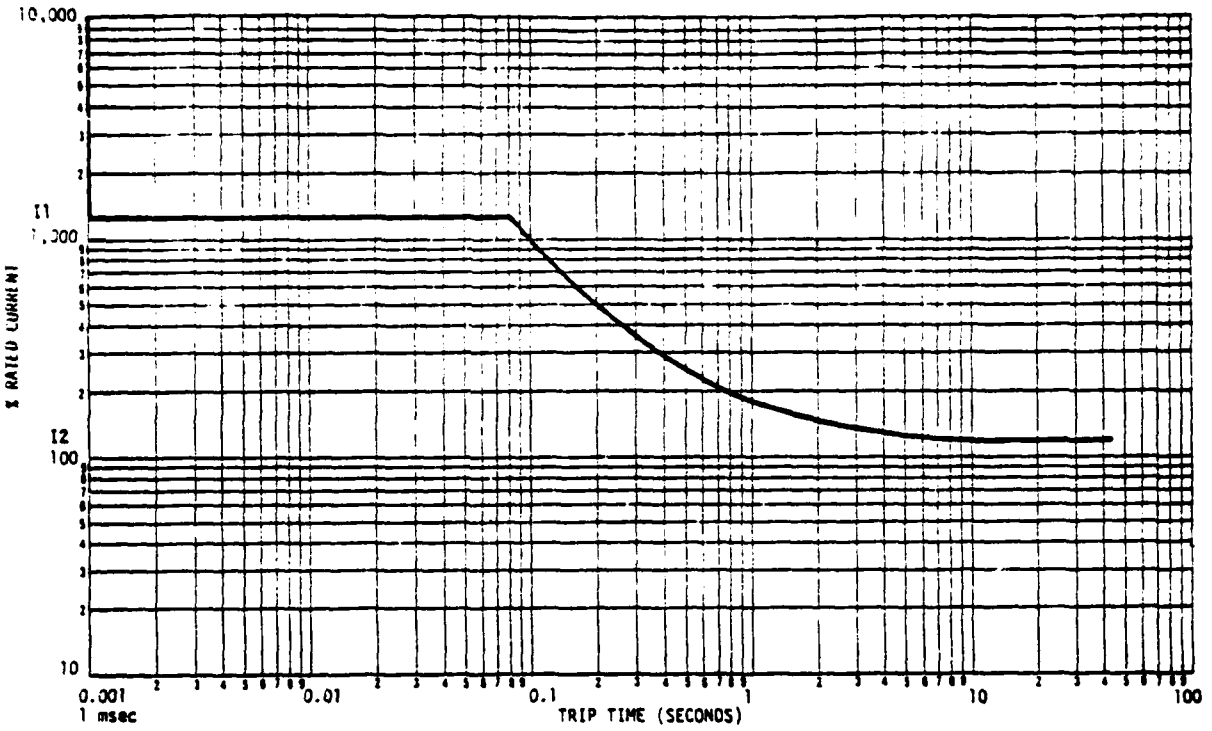
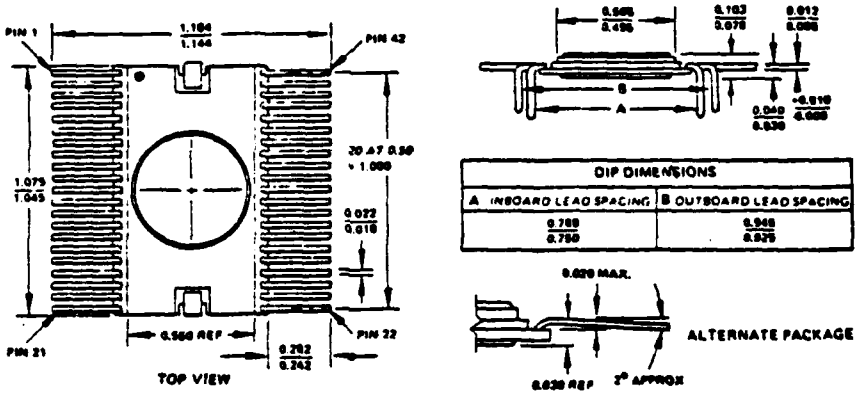


Figure 2. Rated Current vs Trip Time



42 LEAD PACKAGE

PIN CONNECTIONS:
NOTE: PINS ARE NUMBERED COUNTERCLOCKWISE FROM PIN 1, TOP VIEW

PIN	TERM	PIN	TERM	PIN	TERM	PIN	TERM
1	STAOT	12	RT1	23	UPD1	34	
2	ZVC1	13	CT2	24	SENSE	35	GRD
3	CNTRLP	14	RESET	25		36	CTEST
4	NONC	15		26		37	
5	DRIVE	16		27	-12V	38	GRD
6	DRIVEP	17	SHLD	28	VR(+9V)	39	I
7	TRIPOUT	18	+12V	29	VSO	40	I
8	ORCK2P	19	ANC2	30		41	ZIC1
9		20	ANC1	31		42	ZIC2
10	CLOCK1	21	STAT1	32			
11	CT1	22		33			

NOTE: ALSO AVAILABLE IN CHIP FORM

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Pub No. P77-883/201
New Sept. 1977 (150)
Printed in USA

3.8 AC Controller - Size Analysis

PWR DECK

COMPONENT REAL ESTATE

QTY.		
1	Solitron #96Q4	73,000
3	Reston 50 x 100	15,000
4	Pwr Diodes (D1-D4)	40,000
2	Small Sig. Diodes D5 & D6 (40 x 40)	3,200
3	2N5345 (100 X 120)	36,000
2	MJ 10000 (200 x 205)	80,000
2	NC Terminal 100 x 100	20,000
1	Over Current Term. 100 x 100	10,000
1	Normal Term. 100 x 100	10,000
1	Control Term. 100 x 100	10,000
	TOTAL	297,200
30%	Component Contingency	89,160

.386360

DC Controller B_e0

.80 x 1.1 = .8800 IN^2

Packaging factor for AC Controller on DC Contr. B_e0 $\frac{.8800}{.3864}$ = 2.27

Packaging factor for DC Controller (Pwr Deck) = 2.30

30% contingency for additional components to B_e0 1.1 x 1.1 = 1.210 IN^2

Pkg. factor $\frac{1.210}{.3864}$ = 3.13

Package size to accommodate 1.1 x 1.1 B_e0 = 1.5 x 1.8 Foot Pad

PACKAGE HEIGHT

Header thickness			.125
Pwr Deck			
	B_e0	.040	
	Components	.100	
			.140
Spacer			.100
Mechanical Deck			
	Substrate	.060	
	Components	.400	
			.460
Spacer			.100
Logic & Amp Deck			
	(2) Substrates	.075	
	(2) Components	.120	
			.195
Spacer			.100
Cover			.020
		TOTAL	1.250


DA1
FILM