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A STUDY OF METAL-SEMICONDUCTOR CONTACTS ON INDIUM PHOSPHIDE.(U)
MAY 80 G Y ROBINSON F19628-79-C-0016

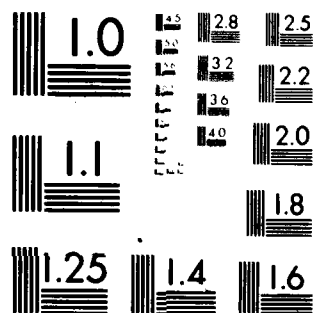
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes the research accomplished during the first eight months of a 20-month program of research on metal-semiconductor contacts to indium phosphide (InP). The Schottky barrier energy and contact resistance are correlated to the metallurgical behavior of metal/InP contacts by using Auger electron spectroscopy. A carefully processed set of samples were used to show conclusively that ϕ_B is greater on p-type InP than on n-type InP. This is shown to be the			

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opposite from the behavior of GaAs and Si Schottky diodes fabricated at the same time using the same process. Several metallic structures have been investigated for use as ohmic contacts to InP. A Ni/Au/Ge system is shown to provide low resistance contacts to n-type InP after heat treatment. For ohmic contact to p-type InP, two metal systems have been tested, but neither system has proven to be suitable for practical InP devices as of yet. Low resistance contacts are found with heat-treated Au/Mg contacts; however, the contact surfaces are non-uniform. Pd was substituted for Au in the Au/Mg contact in order to reduce In-Au alloying. Preliminary results indicate that the contact resistance of the Pd/Mg contacts is high. This may result from MgO formation at the critical InP interface during contact fabrication.

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PERSONNEL

Faculty

G. Y. Robinson, Associate Professor, Principal Investigator

Graduate Students

L. Erickson, Research Assistant

E. Hökelek, Research Assistant

T. Valois, Research Assistant

A. Waseem, Research Assistant

Supporting Staff

W. Smith, Semiconductor Technician

A. Toy, Undergraduate Technician

1. INTRODUCTION

This research program is a experimental study of metal/semiconductor contacts on indium phosphide. The primary objective of the program is to determine the fundamental parameters which control the electrical and metallurgical properties of the metal/InP interface. The principal experimental tools of this research program are electrical measurement of contact barrier energy and specific contact resistance and surface chemical analysis using Auger electron spectroscopy. The results of the program should provide guidelines for development of practical ohmic contacts for use in future InP devices, such as infrared detectors or field-effect transistors.

Metal-semiconductor structures play an important role in the field of microelectronics by providing either ohmic contacts or Schottky-barrier diodes in discrete and integrated circuit devices. The fundamental theoretical understanding of the electrical properties of a rectifying Schottky metal-semiconductor interface is essentially complete; the theory for an ohmic contact is less so but a complete understanding is rapidly developing as a result of recent advances. However, a comparable level of experimental knowledge regarding metal-semiconductor contacts does not as yet exist. This is particularly true for contacts to the III-V compound semiconductors, such as GaAs and InP.

In the case of InP, the limited amount of metal-semiconductor research that has been reported (i.e., see literature review in Section 5.1). With regard to Schottky contacts on InP, early

metal-gate FET research indicated that the barrier energy is low on n-type InP. If this is true, the barrier energy must be high on p-type material, unlike Schottky barriers on the more widely used semiconductors Si and GaAs.

With regard to ohmic contacts on InP, more research has been performed than for Schottky contacts, but the results are limited. Ohmic contacts to any lightly doped semiconductor material can be achieved by use of an intermediate, heavily doped layer (e.g., metal/n⁺/n or metal/p⁺/p structures). However, in InP the fabrication of selected n⁺ or p⁺ regions with high temperature diffusion or other conventional techniques have not yet proven to be practical. Thus, research data has been largely confined to ohmic contact formation on InP using heat-treated vacuum-deposited metal layers. The metal layers usually contain a suitable dopant and the heat treatment is used to drive the dopant into the InP to form the n⁺ or p⁺ layer necessary for low resistance ohmic contacts.

It is the purpose of this research program to study in detail the electrical and metallurgical properties of several metal contacts to InP, with emphasis on the development of ohmic contacts for practical InP devices. Several different composite metal systems have been examined for use as ohmic contact to InP, and the contact barrier energy for n- and p-type InP has been accurately measured in a set of specially prepared Schottky diodes. The results of the later measurements are given in Section 2, where InP is shown to differ substantially from GaAs and Si in its electrical behavior and metal-semiconductor interface formation.

Low resistance ohmic contacts to n-type InP has been obtained using a heat-treated composite metal layer containing Ni, Au, and Ge; the results are described in Section 3. Two composite metal systems have been examined for ohmic contact to p-type InP: Au/Mg (Section 4) and Pd/Mg (Section 5). Neither system has exhibited totally acceptable ohmic contact behavior to p-type InP, primarily because the Mg, a p-type dopant in InP, oxidizes readily during contact fabrication. Finally plans for future research are discussed in Sections 2 and 5.

2. COMPARISON OF ϕ_B FOR InP, GaAs, AND Si

From previous studies of ohmic contacts in this laboratory and from a careful search of the literature, it is apparent that very little data has been collected in a systematic manner for Schottky diodes on InP. In particular, it has not been unequivocally established that $\phi_{Bp} > \phi_{Bn}$ for InP, which would be just the opposite to what is well established for GaAs and Si. This is very important in development of a ohmic contact technology, since ϕ_B has a significant affect on the electrical behavior of a metal-semiconductor contact. Thus we have undertaken a project to carefully measure ϕ_B by several techniques for Schottky diodes fabricated simultaneously on the three semiconductors InP, GaAs, and Si. This section reports in detail a new fabrication procedure and the initial results of the study of Pd Schottky diodes on the three above semiconductors.

2.1 Literature Search

An extensive literature search covering the period 1960-1978 was carried out in an attempt to screen the literature for all available information on metal contacts to InP. Only 13 papers that specifically dealt with the subject could be found and the results reported in these papers are tabulated in Table 2.1. It appears that these studies were mostly directed towards finding a satisfactory ohmic contact to InP and most of them are incomplete. Schottky-barrier energy measurements have been reported for a few metals, but the reproducibility has been very

poor and the barrier energy appears to be strongly affected by the preparation of InP surface prior to metal deposition.

2.2 Experimental Procedure

A new three-level mask set was designed and fabricated, with the aid of a microcomputer, for metal-semiconductor contact studies. The mask set was designed to allow the measurement at the wafer level of Schottky-barrier energy by current-voltage (I-V), capacitance-voltage (C-V), and photoelectric response techniques, as well as the measurement of specific contact resistance on the same chip.

The computer plots of each mask are shown in Fig. 2.1. The dimensions of the unit cell were chosen to maximize the number of cells per unit area, thus producing the maximum number of devices for each InP wafer. The oxide mask shown in Fig. 2.1a is used to etch contact holes in the insulator. The following two masks, shown in Fig. 2.1b and Fig. 2.1c, are metal masks. The metal-contact mask (Fig. 2.1b) is used to mask the first layer of metal whose thickness is usually less than $100 \text{ \AA}$. A thin layer of metal is necessary for photoelectric response measurements since infrared radiation must penetrate through the metal layer in order to excite carriers over the barrier. The largest contact area is used for photoelectric response and capacitance-voltage measurements while the smaller contacts can be used for current-voltage and specific contact resistance measurements. The third-level mask (Fig. 2.1c) is used to mask the second layer of metal whose thickness is 3000 to $10,000 \text{ \AA}$. This layer of metal provides

contact to the first metal layer and is necessary probing the devices. The specifications of the mask-set are given in Table 2.2.

The properties of the metal/InP contacts are strongly dependent on the preparation of InP surface prior to metal deposition;¹⁻¹⁴ therefore, a detailed description of the contact fabrication procedures will be given below.

In order to better understand the nature of the metal/InP interface, both p- and n-type InP wafers along with control wafers of GaAs and Si were processed into Pd/semiconductor contacts. The control wafers of GaAs and Si would later allow comparison of the behavior of Pd/semiconductor contacts on all three semiconductors fabricated at the same time with identical processing steps. Since the interaction of Pd with GaAs and Si is fairly well understood, such a comparison might reveal new information about the metal/InP interface.

The major fabrication procedures can be summarized as:

- a) Formation of SiO_2 on the front side (polished) of the wafers.
- b) Formation of ohmic contacts on the back side of the wafers.
- c) Application of the oxide mask (Fig. 2.1a).
- d) Application of the metal-contact mask (Fig. 2.1b) and Pd deposition.
- e) Application of the metallization mask (Fig. 2.1c) and the Al deposition.

These procedures and the intervening processing steps will be described in detail in the following paragraphs.

The pyrolithic chemical vapor deposition (CVD) of SiO_2 on InP and GaAs wafers was performed at 300°C using a rapid start-up cycle.¹⁴ The resulting SiO_2 layer of $3000 \text{ \AA}$ was uniform in thickness, free of pinholes, and could be etched in a controlled manner. An SiO_2 layer of the same thickness was thermally grown on Si wafers at 1100°C . All wafers were cleaned in a detergent solution and degreased by rinsing in tri-chloro-ethylene, acetone, deionized water, and etched in native oxide and semiconductor etchants prior to SiO_2 formation. These etching sequences are summarized in Table 2.3. Each etching cycle was followed by a thorough rinse in deionized water.

Preceding the deposition of the back contacts, the wafers were etched in the sequences summarized in Table 2.4 after the front side SiO_2 was protected by a film of black wax. A degreasing sequence followed the removal of the wax. The wafers were then immediately placed into a vacuum system and the metal depositions were performed at pressures less than 4×10^{-6} Torr. The composition and the formation conditions of the ohmic back contacts are given in Table 2.5 along with results of tests performed to determine the interaction of the etchants with the contact materials. The tests were conducted on very small pieces scribed from each wafer and the samples were kept in the etchants longer than the wafers were planned to be etched during the fabrication of the test devices. These tests were necessary to establish a fabrication procedure for each Pd/semiconductor contact. The etchants listed in Table 2.5 were determined to be

compatible with Shipley AZ 1350B photoresist, with the exception of the 45 w. % KOH.

The test devices, which consisted of a Pd film of $90 \pm 10 \text{ \AA}$ thickness on the semiconductors and a $3000 \text{ \AA}$ thick Al film for the bonding pads, were fabricated using the three-level mask set described above. In order to avoid the metal-etchant incompatibility problems in a two-metal system, a lift-off photolithography technique¹⁴ was used exclusively to define the metal patterns. Following the photolithography step that defined the Pd patterns on the wafers, the etchants listed in Table 2.6 were applied and the wafers were placed in vacuum within 30 minutes for Pd deposition. Pd evaporation was performed at a pressure of 2×10^{-6} Torr and at the rate of $20 \text{ \AA/sec}$ in an electron beam evaporation system. The substrate temperature during evaporation remained below 26°C .

The lift-off of excess Pd in acetone was followed by the photolithography step which defined the Al patterns. The wafers were baked at 80°C for 25 minutes to dry the photoresist. The substrate temperature during Al evaporation was 34°C . After the lift-off of excess Al in acetone, the wafers were scribed into individual unit cells for electrical and metallurgical analysis of the Pd/semiconductor contacts.

2.3 Results and Discussion

All of the Pd/semiconductor contacts were found to be rectifying and the Schottky-barrier energies were measured with I-V and C-V techniques. The results are summarized in Table 2.7. The

I-V and C-V characteristics of Pd/p-InP contacts were found to be nearly the same over the surface of the wafer. Typical I-V and $1/C^2$ -V plots for this contact are shown in Figure 2.2. We believe that the data of Table 2.7 is conclusive evidence that the ϕ_B (I-V) is higher on p-InP than on n-InP while the opposite is true for the same metal contact on GaAs and Si. Data of this type, where all three covalently bonded semiconductors were used to form Schottky diodes with the same metal at the same time and with the same process scheme, are not available in literature.

Auger electron spectroscopy (AES) and in-situ sputter etching with Ar^+ ions were utilized to examine contact surfaces and to obtain depth-composition profiles of selected samples. The purpose was to obtain correlation to the observed electrical properties.

The largest area contact was used for AES analysis. The electron beam in the AES system could be easily focused in the large contact area and the Pd film could be profiled without interference from the surrounding Al surfaces. All samples were cleaned ultrasonically in methanol for 10 minutes preceeding the analysis. The Pd/semiconductor contacts were analyzed using a 5-kV electron beam to produce the Auger electrons and were sputtered with a 1-kV ion beam at an argon pressure of 5.0×10^{-5} Torr. Special attention was paid to chemical identification of elements and compounds present by noting chemical shifts and characteristic peak shapes in the Auger energy spectra at various depths in the Pd/semiconductor structures.

The Auger peak-to-peak amplitude of each element was converted to atomic percent using standard Auger electron sensitivities of the elements. This data reduction method does not take into account the simultaneous presence of different elements or different chemical states of the same element in the film being analyzed. A computer program was used to convert the raw data to depth-composition profiles.¹⁴

The depth-composition profiles of the 90 ± 10 Å thick Pd film on p- and n-type InP, GaAs, and Si are shown in Figures 2.3, 2.4, and 2.5 respectively.

The bulk of the Pd film and the Pd/InP interface were found to be free of any detectable (i.e. less than 0.6 atomic percent) contamination (Fig. 2.3). Small amounts of zinc and oxygen detected during the analysis were confined to the free surface of the Pd film. The profiles reveal considerable mixing of In and P with Pd although no trace of In or P could be detected on the free Pd surface. Considerable mixing of In and P with Au at 22°C in Au/InP contacts¹⁵ and with the Ag film at temperatures as low as 80°C in Ag/InP structures have been reported.¹⁶ Therefore the presence of In and P in the Pd film was not very surprising since the Pd/semiconductor structures had to be exposed to 80°C temperature for 25 minutes during the last photolithography step. It is further observed in Fig. 2.3 that the highest In to P ratio throughout the contact occurs at the Pd/InP interface. The reasons for the presence of this seemingly In-rich region in the profiles are not clear at this time. The effect may be due to loss of P from the InP surface during processing or it may simply be a

result of non-uniform sputtering of elements at the interface which is possible since P is much lighter than Pd or In. The observation of an In-rich interface region in the AES depth-composition profiles of Ag/InP contacts have also been reported.¹⁷

The comments made about the cleanliness of the Pd/InP contacts are also true for the Pd/GaAs contacts as can be seen in Figure 2.4. However, unlike the Pd/InP contacts, the AES depth-composition profiles of the Pd/GaAs structure show little evidence of mixing of the substrate constituents with the Pd film.

The depth-composition profiles for the Pd/Si contacts (Fig. 2.5) differ significantly from the others discussed so far. The most striking difference is the presence of oxygen throughout the contact structures. In addition to this fact, Pd reacted with Si forming Pd₂Si as evidenced by the characteristic shape of the Si Auger peak at 92 eV.¹⁸ The very small thickness of the Pd film ($90 \pm 10 \text{ \AA}$) and the high reactivity of Si with oxygen in the atmosphere are believed to be responsible for the presence of oxygen in the contact structure. Thicker films of Pd₂Si that are formed by in-situ heat treatment in high vacuum contain oxygen only on the free surface of the Pd₂Si film.¹⁸ The Schottky barrier height energy of $\phi_{BN}(I-V) = 0.711 \pm 0.021 \text{ eV}$ measured for Pd/n-Si system is in very good agreement with the previously published value of $\phi_{BN}(I-V)$ for the clean Pd₂Si/n-Si interface.¹⁸

5.1 Conclusions

As indicated earlier, Pd was evaporated simultaneously on all three semiconductors of both types which were processed at the same time and with the same processing scheme thus making an

unambiguous comparison of all Pd/semiconductor structures possible. The AES depth-composition profiles in Figures 2.3, 2.4, and 2.5 leads to the conclusion that the Pd/InP structure lies somewhere between the reactive Pd/Si system and the seemingly non-reactive Pd/GaAs system. This highly uniform Schottky barrier height data for the Pd/p-InP contact suggests a very clean InP interface which was confirmed by Auger analysis. Finally, the initial data of Table 2.7 shows conclusively that $\phi_{BP} > \phi_{BN}$ for Pd/InP diodes while the opposite is true for Pd/GaAs and Pd/Si diodes. Since the larger the value of ϕ_B , the more resistive the metal-semiconductor contact, it should be more difficult to form low resistance ohmic contacts to p-type InP than to n-type InP. This result is borne out in the next sections.

2.5 Plans for Future Work

Future research will include the measurement of ϕ_B for the Pd Schottky diodes by the photoresponse method. This measurement may help explain the difference between $\phi_R(I-V)$ and $\phi_B(C-V)$ values in Table 2.7 and provide ϕ_R data on the low barrier height interfaces not presently accessible with the C-V technique. In addition, a series of experiments will be conducted to introduce a controlled amount of oxide in the InP, GaAs, and Si diodes and the effect on ϕ_R will be determined. The collection of ϕ_B data for other metals besides Pd will be continued.

Table 2.1

Metal/InP Contacts

Contact	Wafer	Surface Preparation	ϕ_B (I-V) eV	ϕ_B (C-V) eV	Doping (cm ⁻³)	Heat Treatment				Ref.
						Time	Temp.	ϕ_B (I-V)	ϕ_B (C-V)	
1. Au/InP	<110>n	15sec. etch in 0.1%Br in CH ₃ OH	0.40	±0.02	5x10 ¹⁵	----	----	----	----	1
2. Au/Au-Ge/InP 5% Ni by wt.	? n	?	?	?	4x10 ¹⁶	----	----	----	----	2
					5x10 ¹⁷ 2x10 ¹⁸	20-100 sec.	>356 <425°C	Ohmic		
3. Au/Ag-Sn/InP	? n	?	?	?	5x10 ¹⁷ 2x10 ¹⁸	180 270s.	>232 <525°C	Ohmic		2
4. Au-Ti/InP 1% by wt.	<100>	2%Br + CH ₃ OH	?	?	10 ¹⁵ -10 ¹⁶	2min.	250°C	0.51	0.53	3
5. Au/InP	<110>n	Vac. Cleaved	0.43	0.50	?	----	----	----	----	4
	<110>n	Br+CH ₃ OH	0.49	0.57	?	----	----	----	----	
	<110>n	Air-exposed	Ohmic		?	----	----	----	----	
	<110>n	O ₂ -exposed	Ohmic		?	----	----	----	----	
	<110>n	Cl ₂ -exposed	Ohmic		?	----	----	----	----	
6. Au/InP	<100>n	0.5%Br+CH ₃ OH	0.49	----	2x10 ¹⁵	----	----	----	----	5
7. Au/InP	<111>n	0.2%Br+CH ₃ OH	0.74	1.31	3x10 ¹⁷	----	----	----	----	6
	<111>n	-----	0.56	1.03	4.3x10 ¹⁷	----	----	----	----	
	<111>n	-----	0.58	1.10	4.3x10 ¹⁷	----	----	----	----	
	<111>n	9N-HCl (20s.)	0.54	0.84	5x10 ¹⁷	----	----	----	----	
	<111>n	9N-HCl (20s.)	0.43	----	-----	----	----	----	----	
	<100>n	9N-HCl (20s.)	0.49	0.84	1x10 ¹⁷	----	----	----	----	
8. Au/InP	<110>n	Vac. Cleaved	0.43	0.50	3x10 ¹⁵	----	----	----	----	7
	<110>n	1%Br+CH ₃ OH	0.49	0.57	3x10 ¹⁵	10m	100°C	----	0.53	
	<110>n	1%Br+CH ₃ OH	0.49	0.57	3x10 ¹⁵	10m	200°C	----	0.52	
	<110>n	1%Br+CH ₃ OH	0.49	0.57	3x10 ¹⁵	10m	300°C	----	0.28	
	<110>n	1%Br+CH ₃ OH	0.49	0.57	3x10 ¹⁵	10m	400°C	Ohmic		
	<110>n	1%Br+CH ₃ OH	0.49	0.57	3x10 ¹⁵	10m	400°C	Ohmic		
9. Cu/InP	<110>n	Vac. Cleaved	----	0.49	3x10 ¹⁵	----	----	----	----	7
10. Al/InP	<110>n	1%Br+CH ₃ OH	0.47	0.52	3x10 ¹⁵	10m	100°C	----	0.52	
	<110>n	1%Br+CH ₃ OH	0.47	0.52	3x10 ¹⁵	10m	200°C	----	0.52	
	<110>n	1%Br+CH ₃ OH	0.47	0.52	3x10 ¹⁵	10m	300°C	----	0.38	
	<110>n	1%Br+CH ₃ OH	0.47	0.52	3x10 ¹⁵	10m	400°C	----	0.22	
	<110>n	1%Br+CH ₃ OH	0.47	0.52	3x10 ¹⁵	10m	400°C	----	0.22	
11. Ag/InP	<110>n	Vac. Cleaved	0.42	0.47	3x10 ¹⁵	----	----	----	----	7
	<110>n	1%Br+CH ₃ OH	0.48	0.55	3x10 ¹⁵	10m	100°C	----	0.52	
	<110>n	1%Br+CH ₃ OH	0.48	0.55	3x10 ¹⁵	10m	200°C	----	0.45	
	<110>n	1%Br+CH ₃ OH	0.48	0.55	3x10 ¹⁵	10m	300°C	Ohmic		
	<110>n	1%Br+CH ₃ OH	0.48	0.55	3x10 ¹⁵	10m	400°C	Ohmic		
	<110>n	1%Br+CH ₃ OH	0.48	0.55	3x10 ¹⁵	10m	400°C	Ohmic		
12. In/InP	<110>n	Cleave or etch	Ohmic		3x10 ¹⁵	----	----	----	----	8
13. Ag/Sn/In/InP	<?> n	?	?	?	1x10 ¹⁵	?	?	Ohmic		
14. Ag/InP	<001>n	10:1 H ₂ O:HF	?	?	2x10 ¹⁵ (?)	1min.	360 420°C	low	ϕ_{Bn}	9
15. Ag/InP	<001>n	Ar ⁺ ion etch for 1 h. and H.T. at 300 ± 10°C for 30 min.	Ohmic		?	----	----	----	----	10
						----	----	----	----	
						----	----	----	----	
16. Ag/InP	<001>n	Ar ⁺ ion etch and annealing at various temp. and atm.	.43±.02	----	0.5-1x10 ¹⁷	----	----	----	----	11
			.38±.02	----	0.5-1x10 ¹⁷	----	----	----	----	
			Ohmic		0.5-1x10 ¹⁷	----	----	----	----	
17. Au/Zn/Au/InP	? p	matte surf.	?	?	1-10 ¹⁸ -cm	15sec.	475°C	Ohmic		12
18. In-5% Cd/InP	? p	?	?	?	5x10 ¹⁶	5m(?)	400°C(?)	rectifying		13
19. In/InP	? p	?	?	?	5x10 ¹⁶	5m(?)	400°C(?)	rectifying		
20. In-5%/Zn/InP	? p	?	?	?	5x10 ¹⁶	5m(?)	400°C(?)	Ohmic		13
21. Au-2%/Zn/InP	? p	?	?	?	5x10 ¹⁶	5m(?)	400°C(?)	Ohmic		

Table 2.2, Specifications of the Mask-Set

1. Unit cell dimensions: $760\mu\text{m} \times 640\mu\text{m}$
(Including the $20\mu\text{m}$ -wide border)
2. Spacing between unit cells: $150\mu\text{m}$
3. Minimum line width: $10\mu\text{m}$
4. Density: 139 unit cells/cm²
5. Number of contacts per unit cell: 9
6. Contact dimensions (in μm):

- a) 700 x 400
- b) 200 x 150
- c) 100 x 100
- d) 50 x 50
- e) 70 x 20
- f) 35 x 35
- g) 25 x 25
- h) 15 x 15
- i) 10 x 10

Table 2.3, Etch Sequence Prior to SiO₂ Deposition

WAFER	TYPE OF ETCHANT	ETCHANT COMPOSITION	ETCHING TIME
InP	In ₂ O ₃ etch	45w.% KOH H ₂ SO ₄ :H ₂ O ₂ :H ₂ O 3 : 1 : 1	30 min.
	InP etch		5 min.
GaAs	Ga ₂ O ₃ etch	20:1-H ₂ O:HCl NH ₄ OH:H ₂ O ₂ :H ₂ O 20 : 7 : 974	10 sec.
	GaAs etch		60 sec.
Si	SiO ₂ etch	10:1-H ₂ O:HF	5 min.

Table 2.4. Etch Sequence Prior to Back Metal Deposition

WAFER	TYPE OF ETCHANT	ETCHANT COMPOSITION	ETCHING TIME
InP	SiO ₂ etch	10:1-H ₂ O:HF	5 min.
	In ₂ O ₃ etch	45w.% KOH*	30 min.
	InP etch	10w.% HIO ₃ *	3 min.
GaAs	SiO ₂ etch	10:1-H ₂ O:HF	5 min.
	Ga ₂ O ₃ etch	20:1-H ₂ O:HCl	10 sec.
	GaAs etch	NH ₄ OH:H ₂ O ₂ :H ₂ O 20 : 7 : 974	60 sec.
Si	SiO ₂ etch	10:1-H ₂ O:HF	3 min.

*A. R. Clawson, D. A. Collins, D. I. Elder and J. J. Monroe, Technical Note 592: Laboratory Procedures for Etching and Polishing InP Semiconductor, MOSC, San Deigo, California (1978).

Table 2.5, Results of Test of Chemical Resistance of Back Contact

WAFER	ORIENTATION	BACK CONTACT	BACK CONTACT HEAT TREAT. TIME	TEMP	TYPE OF ETCHANT	ETCHING TIME	EFFECT OF ETCHANT ON BACK CONTACT
p-InP	3° off <100> toward <111>	Au/Mg - 1600Å/400Å	5min	500 C	In ₂ O ₃ etch InP etch	60min 30min	No observable change Contact etched away after 32min
n-InP	3° off <100> toward <111>	Ni/Au/Ge - 150Å/520Å/700Å	5min	300 C	SiO ₂ etch	5min	No observable change
p-GaAs	<100>	Au/In - 800Å/500Å	3min	500 C	In ₂ O ₃ etch InP etch	30min 3min	No observable change Contact etched away after 3min
n-GaAs	<100>	Ni/Au/Ge - 150Å/520Å/700Å	2min	500 C	SiO ₂ etch Ga ₂ O ₃ etch GaAs etch	5min 60sec 10min	No observable change No observable change Contact etched away after 10min
p-Si n ⁺ -n-Si	<100> <100>	Al, 6000Å Al, 6000Å	5min 5min	550 C 550 C	SiO ₂ etch SiO ₂ etch SiO ₂ etch	5min 60sec 10min 5min 90sec 90sec	No observable change No observable change No observable change No observable change No observable change No observable change

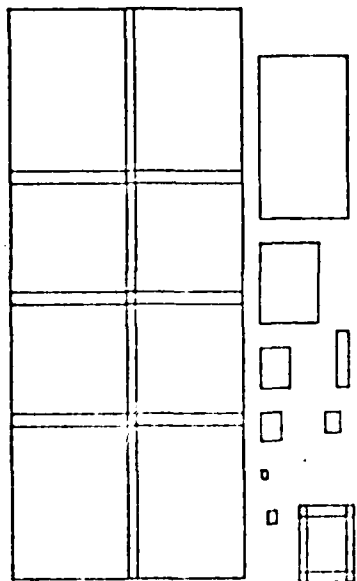
Table 2.6. Etch Sequence Prior to Front Metal Deposition

WAFER	TYPE OF ETCHANT	ETCHANT COMPOSITION	ETCHING TIME
InP	In ₂ O ₃ etch	45% KOH* by weight	30 min.
	InP etch	10% HIO ₃ by weight	30 sec.
GaAs	Ga ₂ O ₃ etch	20:1-H ₂ O:HCl	10 sec.
	GaAs etch	NH ₄ OH:H ₂ O ₂ :H ₂ O 20 : 7 : 974	30 sec.
Si	SiO ₂ etch	9:1-NH ₄ F:HF (40W%) (48W%)	20 sec.

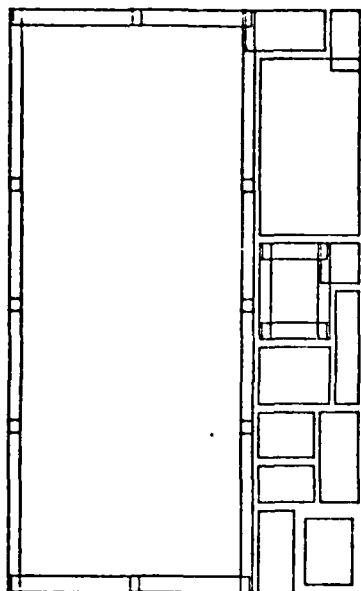
*Since this etchant is not compatible with Shipley AZ1350-B photoresist, it was applied preceeding photolithography.

Table 2.7. Schottky Diodes of Pd

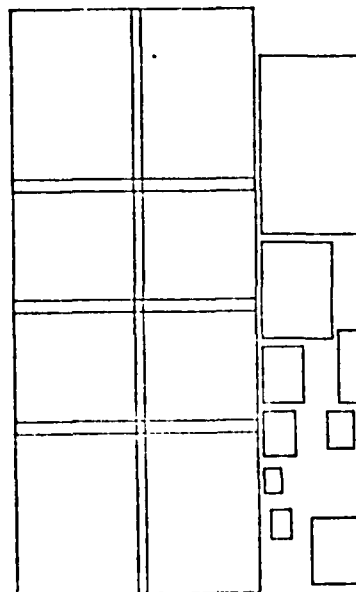
Diode	I-V				C-V		
	ϕ_B (I-V)	Richardson Constant Used (Amp/cm ² /K ²) for I-V	n	No. Devices	ϕ_B (C-V)	$ N_D - N_A $ (cm ⁻³)	No. Devices
p-InP	823 ± 3 meV	60	1.07 ± 0.01	20	895 ± 16 meV	2.12 ± 0.09 × 10 ¹⁷	10
n-InP	454 ± 30 meV	9.8	1.09 ± 0.07	15			
p-GaAs	485 ± 12 meV	74.4	1.09 ± 0.07	15			
n-GaAs	865 ± 5 meV	8.16	1.06 ± 0.02	21	929 ± 46 meV	5.56 ± 0.16 × 10 ¹⁶	10
p-Si	488 ± 57 meV	32	1.77 ± 0.14	10			
n-Si	711 ± 21 meV	112	1.13 ± 0.07	19			



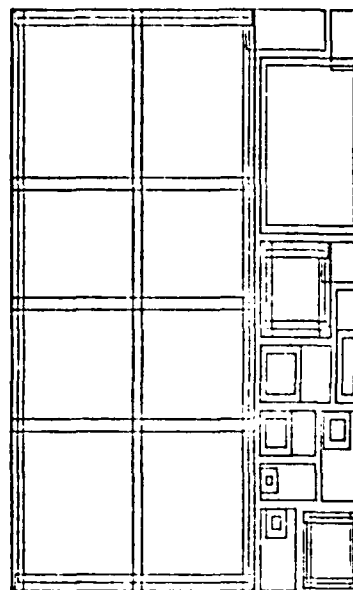
a. Oxide mask



c. Metallization mask
(thick metal)



b. Metal-contact mask
(thin metal)



d. Composite plot of
all three stages

Figure 2.1. Computer generated layout of two-level metal mask.

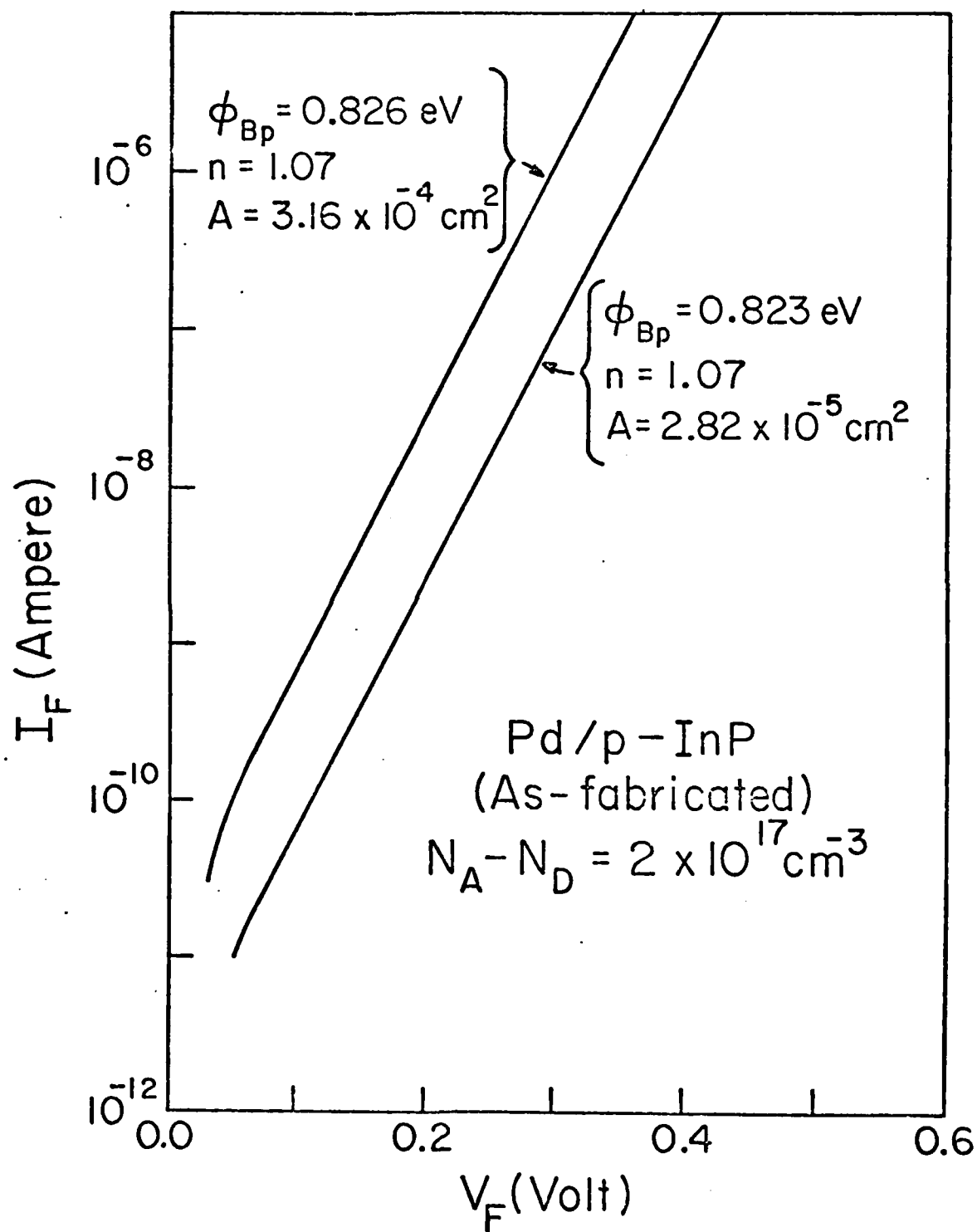


Figure 2.2(a). I-V curve for Pd/pInP diodes.

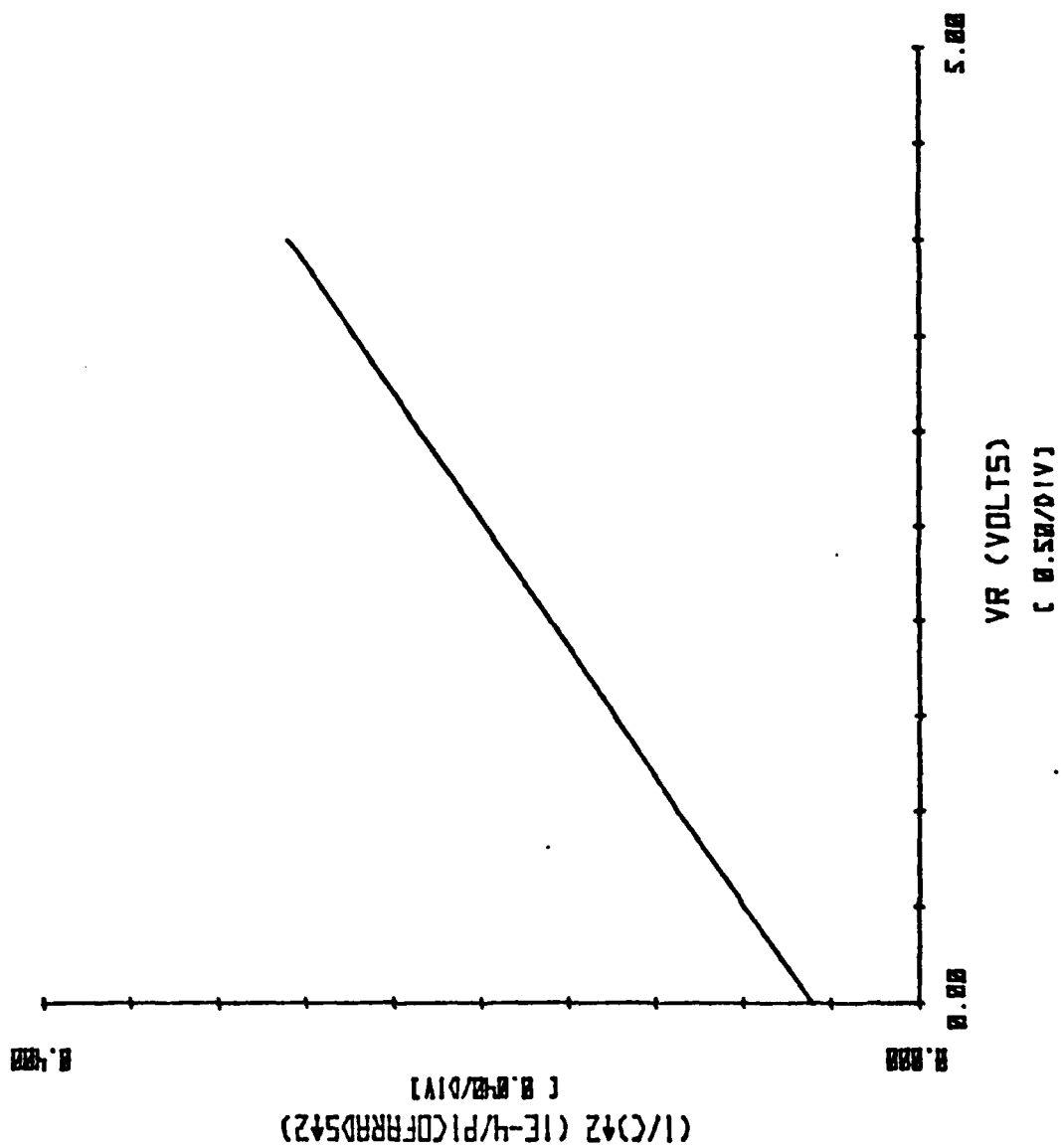


Figure 2.2(b). C-V characteristics of Pd/pInP diodes.

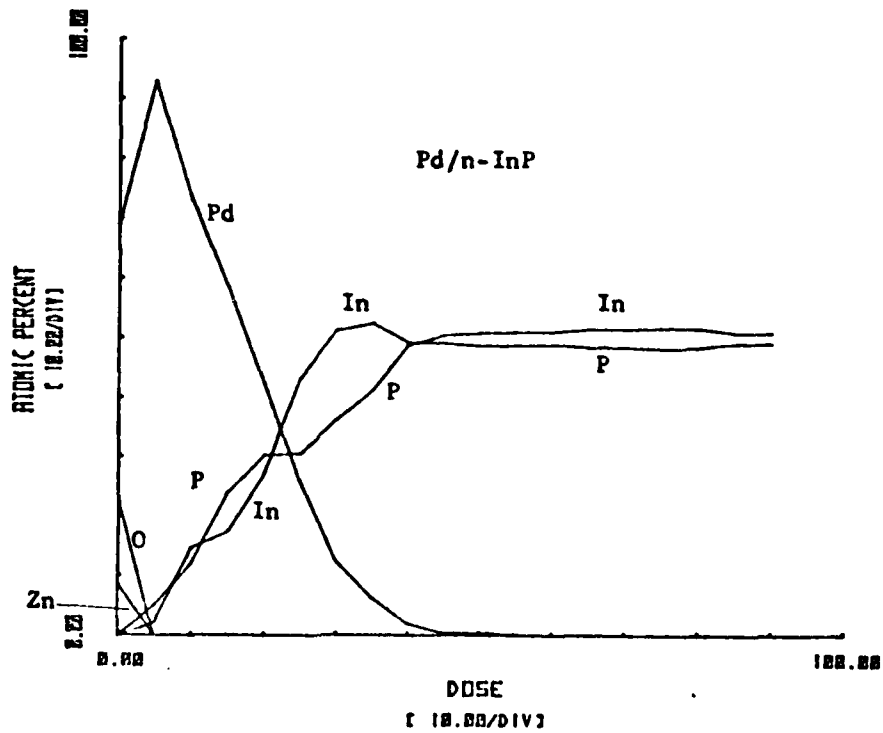
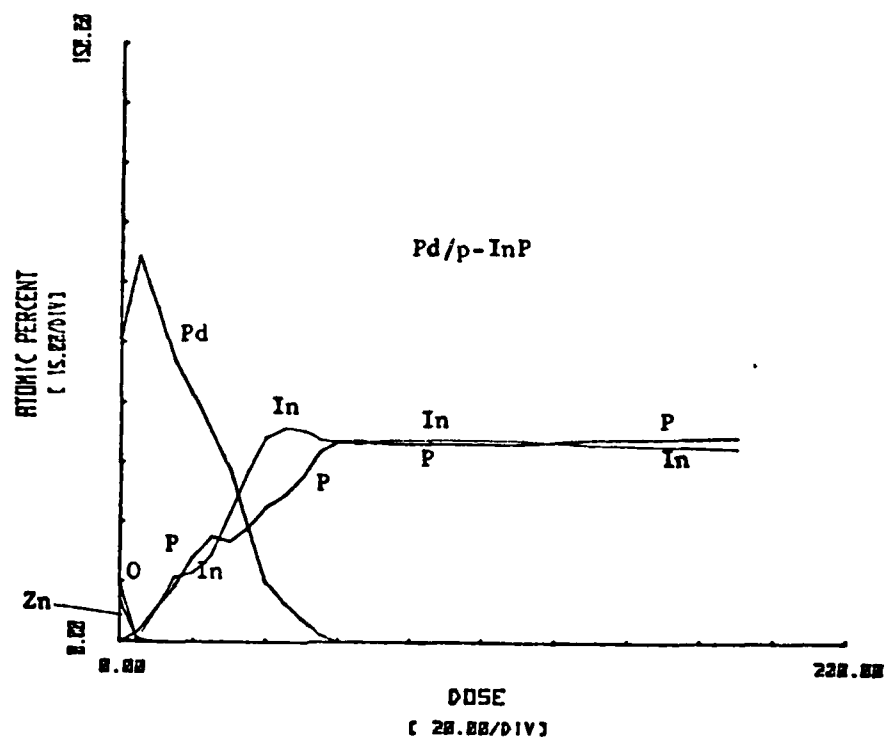


Figure 2.3. Auger-depth profiles of Pd/InP diodes.

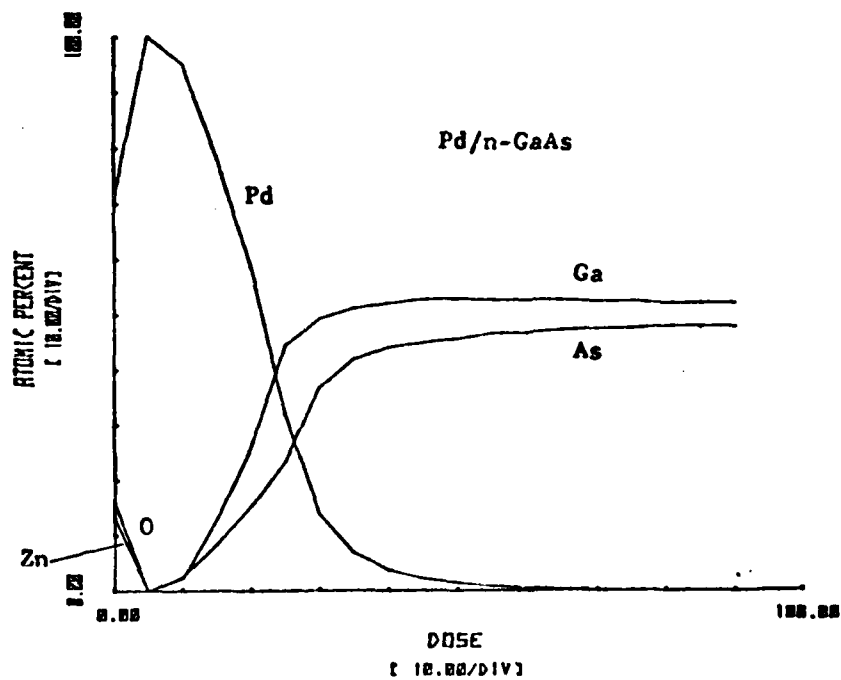
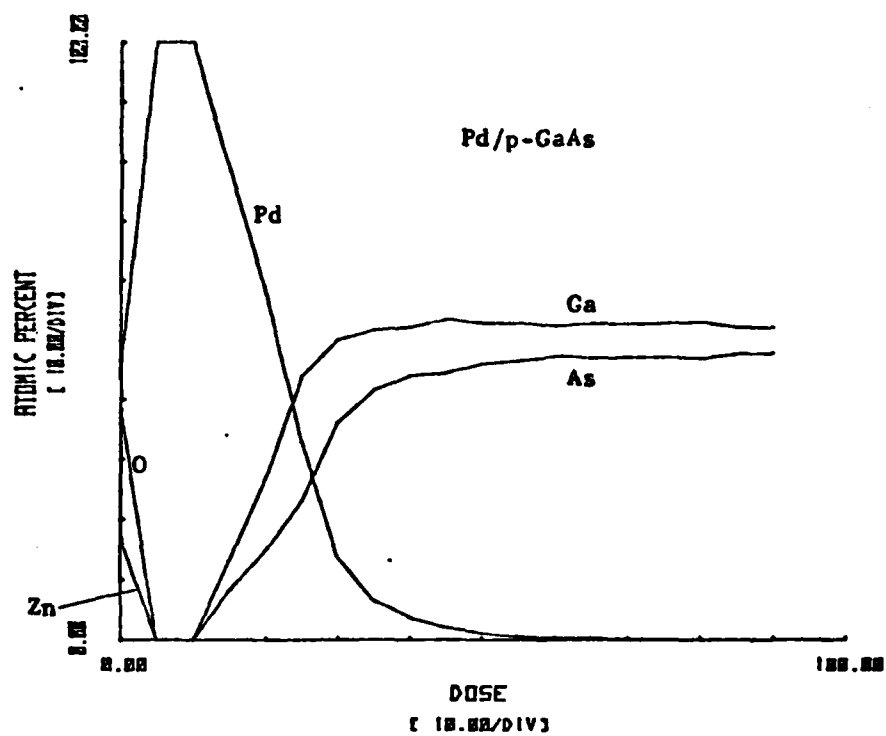


Figure 2.4. Auger-depth profiles of Pd/GaAs diodes.

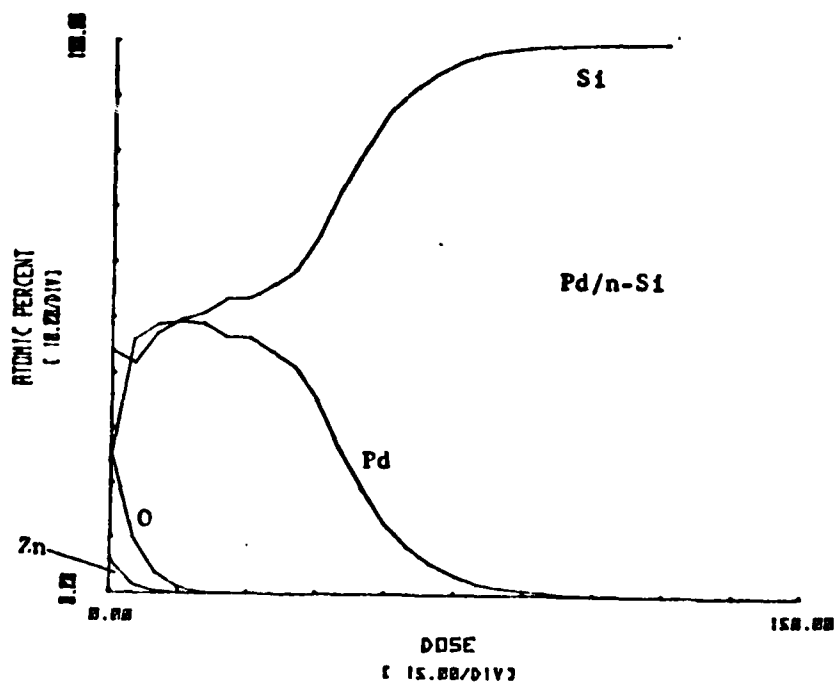
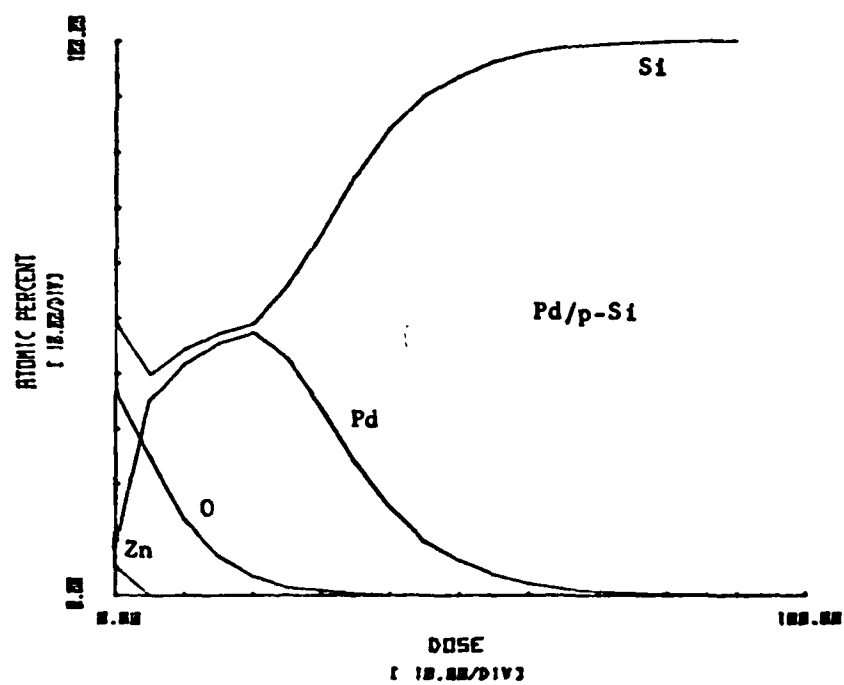


Figure 2.5. Auger-depth profiles of Pd/Si diodes.

3. Ni/Au/Ge CONTACTS ON N-TYPE InP

The most common approach to making ohmic contacts to n-type GaAs has been the alloy regrowth technique. In this technique the contact metal deposited on the GaAs surface contains a n-type dopant. The contact is then heated until a thin layer of GaAs is dissolved. Upon cooling, the semiconductor recrystallizes with a regrown layer containing a high concentration of the dopant. The result is the desired metal/n⁺GaAs/nGaAs structure for ohmic contact. In n-type GaAs, the mostly used metal system is Ni/Au/Ge.²⁰ Ge is a donor, the appropriate Au-Ge mixture melts at 360°C, and Ni is found to improve surface uniformity. This report is concerned with the investigation of the Ni/Au/Ge system applied to n-type InP. Supporting research on the Ni/InP and Au/InP systems was reported in detail the previous annual report and is included below as background information.

3.1 Experimental Procedure

The n-type wafers were of <100> orientation with doping from 10^{16} to 10^{18} cm⁻³. After degreasing, the wafers were etched five minutes in 3:1:1 H₂SO₄:H₂O₂:H₂O. A SiO₂ masking layer of 3000 Å thickness was deposited using pyrolytic chemical vapor deposition at 300°C. Subsequent steps to etch holes in the oxide layer and to define the metal contacts utilized conventional photolithographic techniques. Each metal layer of the multilayered Ni/Au/Ge structure was sequentially deposited using electron-beam evaporation in an ion-pumped vacuum system during the same pump-down. The wafers were maintained below 50°C during deposition.

The metal-semiconductor contact systems will be designated "as-deposited", referring to samples immediately after deposition of metal layers, or "as-fabricated" for those samples where processing subsequent to the metal deposition (i.e., a post-photolithography bake at 150°C/5 min. in air) may have altered the as-deposited structure. Samples that are referred to as "heat treated" were placed in an open-tube furnace with flowing N₂ gas after completion of all fabrication steps.

Characterization of the samples before and after heat treatment, including the correlation of electrical and metallurgical data, involved a number of techniques previously used for the study of ohmic contacts to GaAs.²⁰ Current-voltage measurements were used to obtain Schottky barrier energy ϕ_{Bn} and specific contact resistance r_c , and capacitance-voltage measurements were used to find carrier concentration $|N_D - N_A|$ and ϕ_{Bn} . Auger electron spectroscopy (AES) was used for surface chemical analysis and combined with ion beam etching, for depth-composition profiling of the multilayered thin-film structures.²⁰ Surface morphology was characterized with scanning electron microscopy and optical microscopy. X-ray diffraction analysis was also conducted on specially prepared Ni-Ge films.

3.2 Results and Discussion

The specific contact resistance as a function of heat-treatment temperature for the Ni/Au/Ge/nInP, Ni/nInP, and Au/nInP systems is summarized in Fig. 3.1. Figure 3.2 shows typical AES profiles for both as-fabricated and heat-treated Ni/Au/Ge/nInP

samples. Auger analysis revealed that for samples heat treated up to about 250°C, Ge moves away from the InP interface, through the intervening Au layer, to react with the top Ni layer (see Fig. 3.2a). Changes in the Ge Auger energy spectra and independent X-ray diffraction studies¹⁴ indicated that essentially all of the Ge had reacted to form a layer of NiGe after 5 min. at 300°C. Simultaneously excess Ni diffused to the InP interface (see Fig. 3.2b). The thin interfacial layer of Ni appears to control the contact resistance in the heat-treatment range 250 - 350°C, especially since the sharp drop in r_c for both the Ni/Au/Ge/nInP and the Ni/nInP systems occurred at the same temperature, 300°C, resulting in a minimum in r_c at 325°C. At higher heat-treatment temperatures considerable intermixing of all elements occurred. Contact surfaces became increasingly non-uniform and more scatter in the r_c data was found. No abrupt change in electrical behavior was observed at 360°C, the melting point for the Au-Ge eutectic composition used.

The lowest r_c observed for the Ni/nInP system was $4 \times 10^{-5} \Omega\text{-cm}^2$, heat treated at 325°C, 5 minutes. Specific contact resistances for the Ni/Au/Ge/nInP system were as low as $3 \times 10^{-5} \Omega\text{-cm}^2$ (325°C, 5 min) and $5 \times 10^{-5} \Omega\text{-cm}^2$ (400°C, 2 min) for $|N_D - N_A| = 3 \times 10^{16} \text{ cm}^{-3}$. The Au/nInP system exhibited an as-fabricated barrier energy of $\phi_{Bn} = 0.50 \text{ eV}$ and did not produce acceptable ohmic behavior after heat treatment.

2.3 Conclusions

On n-type material, a film of pure Ni exhibited a low contact resistance after heat-treatment at 325°C. The composite film

Ni/Au/Ge exhibited similar behavior primarily because Ni diffused to the InP interface. Since low resistance contacts were found below the Au-Ge eutectic temperature, the alloy regrowth mechanism responsible for ohmic contact formation in the Ni/Au/Ge/nGaAs system does not apply for Ni/Au/Ge/nInP.

The barrier energy ϕ_{Bn} for all metal systems tested on n-type InP were found to be relatively low (0.1 - 0.5 eV). Thus it was not difficult to obtain ohmic contact behavior. However, the optimum contact system was found to be that of Ni/Au/Ge containing atomically more Ge than Ni. In that case, contacts were of low resistance after a relatively low temperature heat treatment, had smooth surfaces, and required minimal control of the heat-treatment temperature.

This project is complete and no future work is planned.

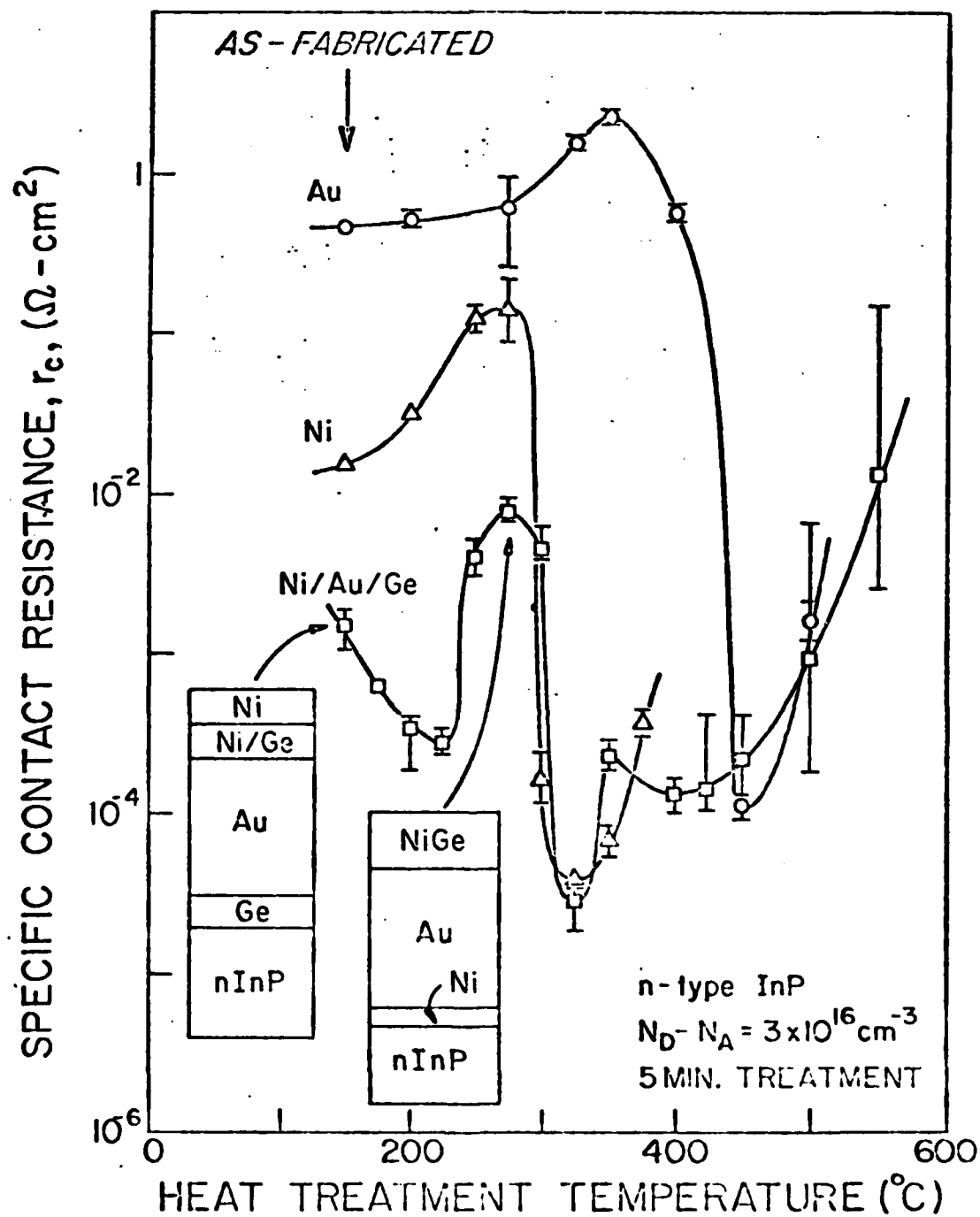


Figure 3.1. Specific contact resistance as a function of heat-treatment temperature for Au, Ni, and Ni/Au/Ge films on n-type InP.

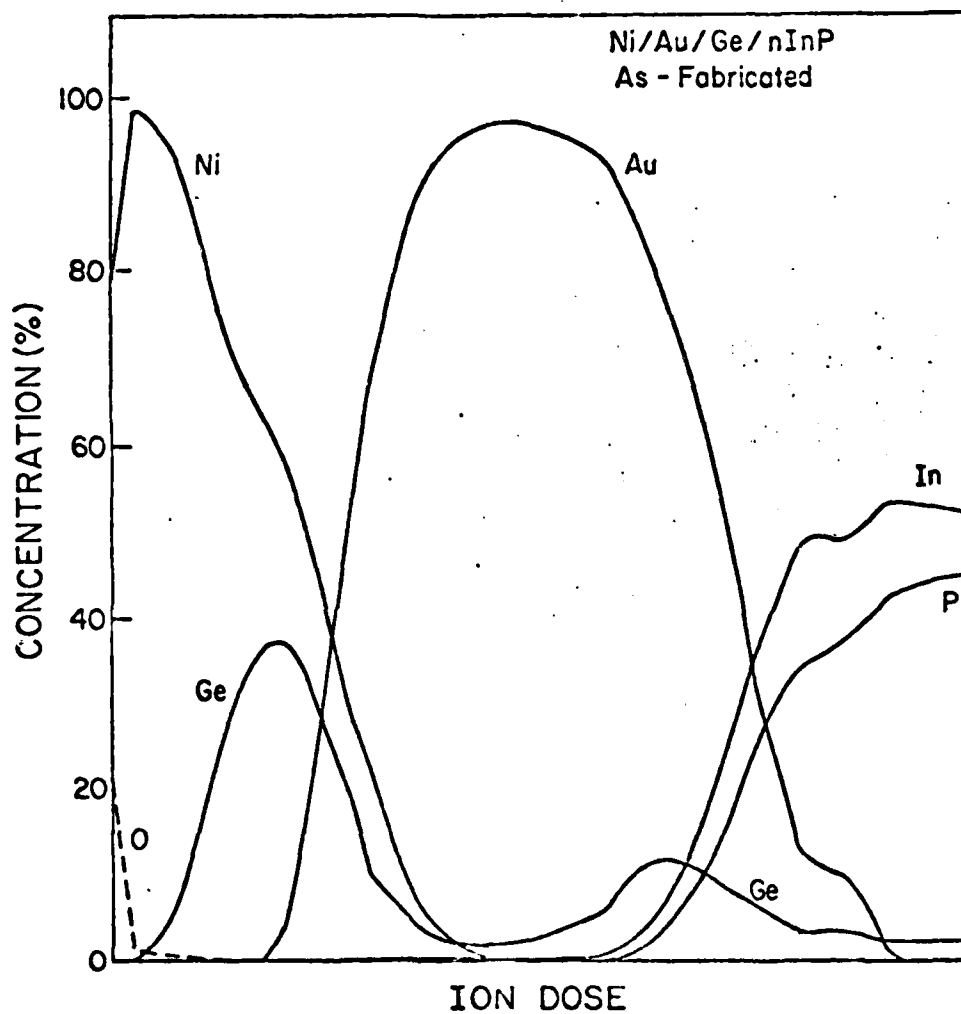


Figure 3.2(a). Auger profile of an as-deposited Ni/Au/Ge/nInP diode.

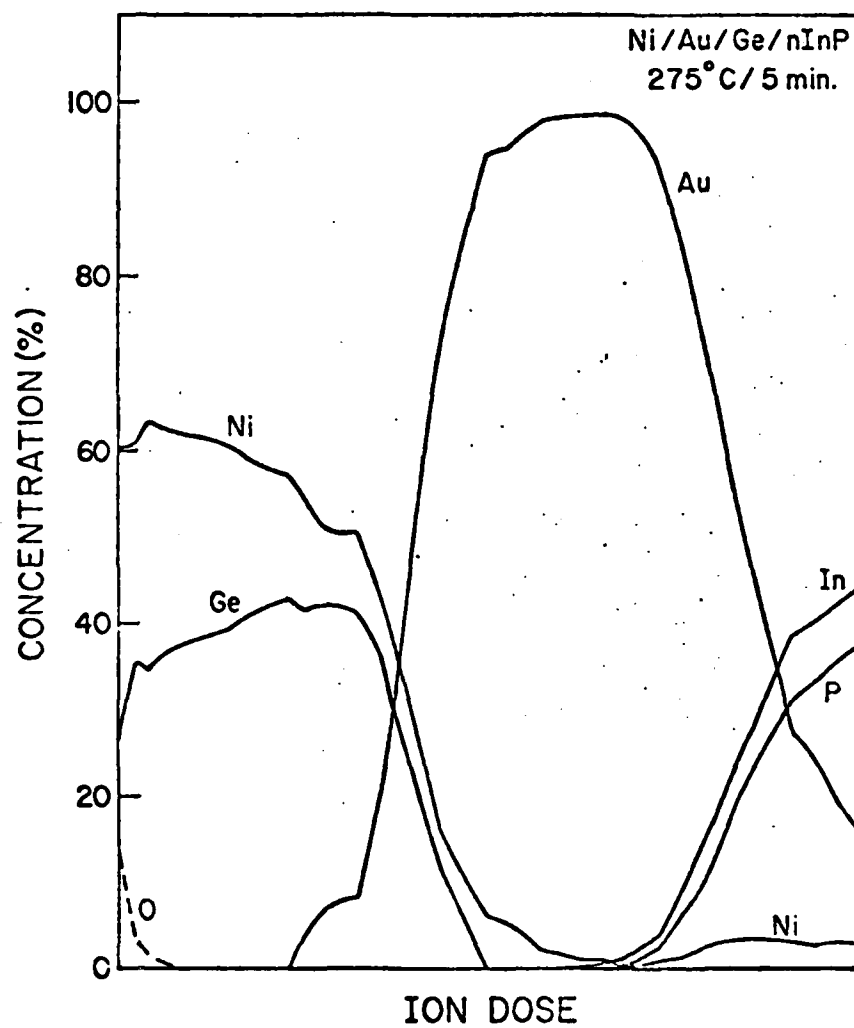


Figure 3.2(b). Auger profile of heat-treated Ni/Au/Ge/nInP diode.

4. Au/Mg CONTACTS ON P-TYPE InP

As discussed in a previous report,¹⁴ we have investigated an alloy contact consisting of Au/Mg multilayer film on p-type InP. This study was completed during the period covered by this annual report and the highlights of the study are reported in this section.

4.1 Experimental Procedure

The p-type InP wafers used in this study were both $\langle 111 \rangle$ and $\langle 100 \rangle$ material of $1 \times 10^{17} \text{ cm}^{-3}$ and $6 \times 10^{17} \text{ cm}^{-3}$ doping. The Mg film was deposited first with a thickness of $400 \text{ \AA}$ followed by a Au film of $1600 \text{ \AA}$ thickness. All contact processing steps was the same as described in Section 3.1.

4.2 Results and Discussion

The electrical characteristics of the as-deposited Au/Mg/pInP samples were typical of Schottky diodes with large barrier energies (i.e., $\phi_{BP} = 0.7$ to 1.0 eV), and in all cases, the contact resistance on p-type InP was much higher than on the n-type material. As shown in Fig. 4.1 the contact resistance for the Au/Mg/pInP system decreases rapidly with increasing heat treatment above 300°C . The lowest contact resistance measured was approximately $1 \times 10^{-4} \Omega\text{-cm}^2$ for $N_A - N_D = 6 \times 10^{17} \text{ cm}^{-3}$ after heat treatment at 446°C for 50 min, which also resulted in the smoothest heat-treated surface.

Figure 4.2 illustrates typical AES profiles of the Au/Mg/pInP system. For the as-deposited samples, Mg was found on the surface of the Au as well as at the InP interface, indicating that considerable migration of the Mg takes place during the Au deposition.

In addition, most of the Mg on the surface, and to a lesser extent at the InP interface, was present as the oxide MgO. The profile for the heat-treated sample of Fig. 4.2b shows a thin MgO layer covering a Au-In layer which covers a region of mixed composition, all covering the InP substrate. The ratio of Au to In in the Au-In layer corresponds to the solubility of In in Au at the temperature of heat treatment.²² Extensive loss of In and P from the substrate was found for samples heat treated above 400°C.

The surface morphology of the Au/Mg/pInP system was found to be strongly dependent on heat-treatment conditions. At or above the Au-In eutectic temperature²² of 457°C, melting takes place during heat treatment, and at 500°C evidence of extensive lateral melting of the Au/Mg film on top of the SiO₂ adjacent to the contact area was found. A significant amount of In was found by Auger analysis in the metal film on top of the SiO₂, indicating appreciable loss of In from the InP substrate at temperatures above 457°C.

4.3 Conclusions

Before heat treatment, contact resistance and Schottky barrier energies were always higher on p-type than n-type InP, unlike Schottky barriers on GaAs and Si. After heat treatment, ohmic contact behavior was observed but with accompanying poor surface uniformity. The latter is probably the result of the high solubility of In in Au at the heat-treatment temperatures used. Based on the results of this study, the heat treated Au/Mg system would be only marginally useful to form ohmic contacts to p-type InP.

The reproducibility of the Au/Mg contacts was poor. This is probably the result of Mg oxidation during Mg deposition. If most or all of the Mg is present as MgO, then little or no Mg is available for incorporation as a p-type dopant in the InP.

This project is complete and no future work is planned.

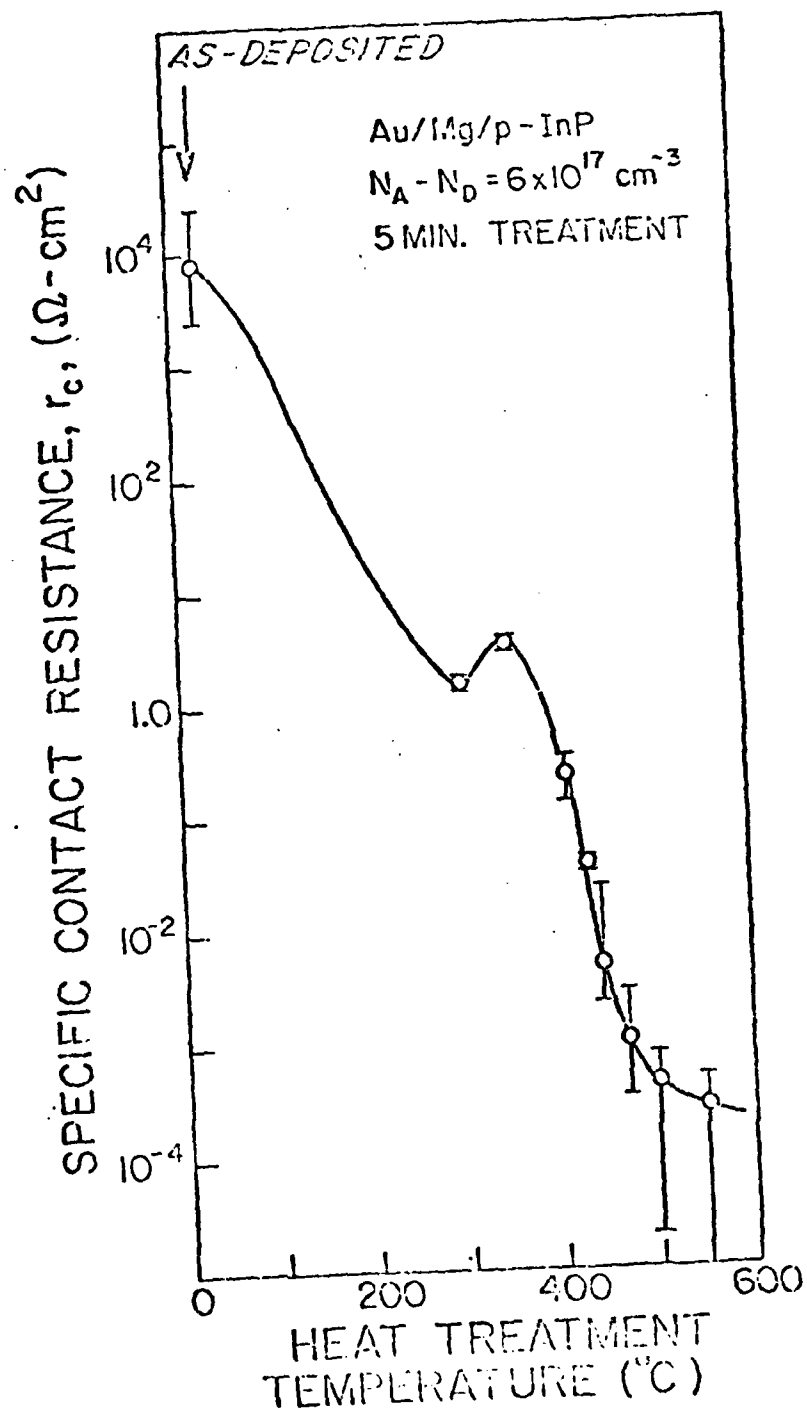


Figure 4.1. Specific contact resistance of Au/Mg/pInP diodes as a function of heat-treatment temperature.

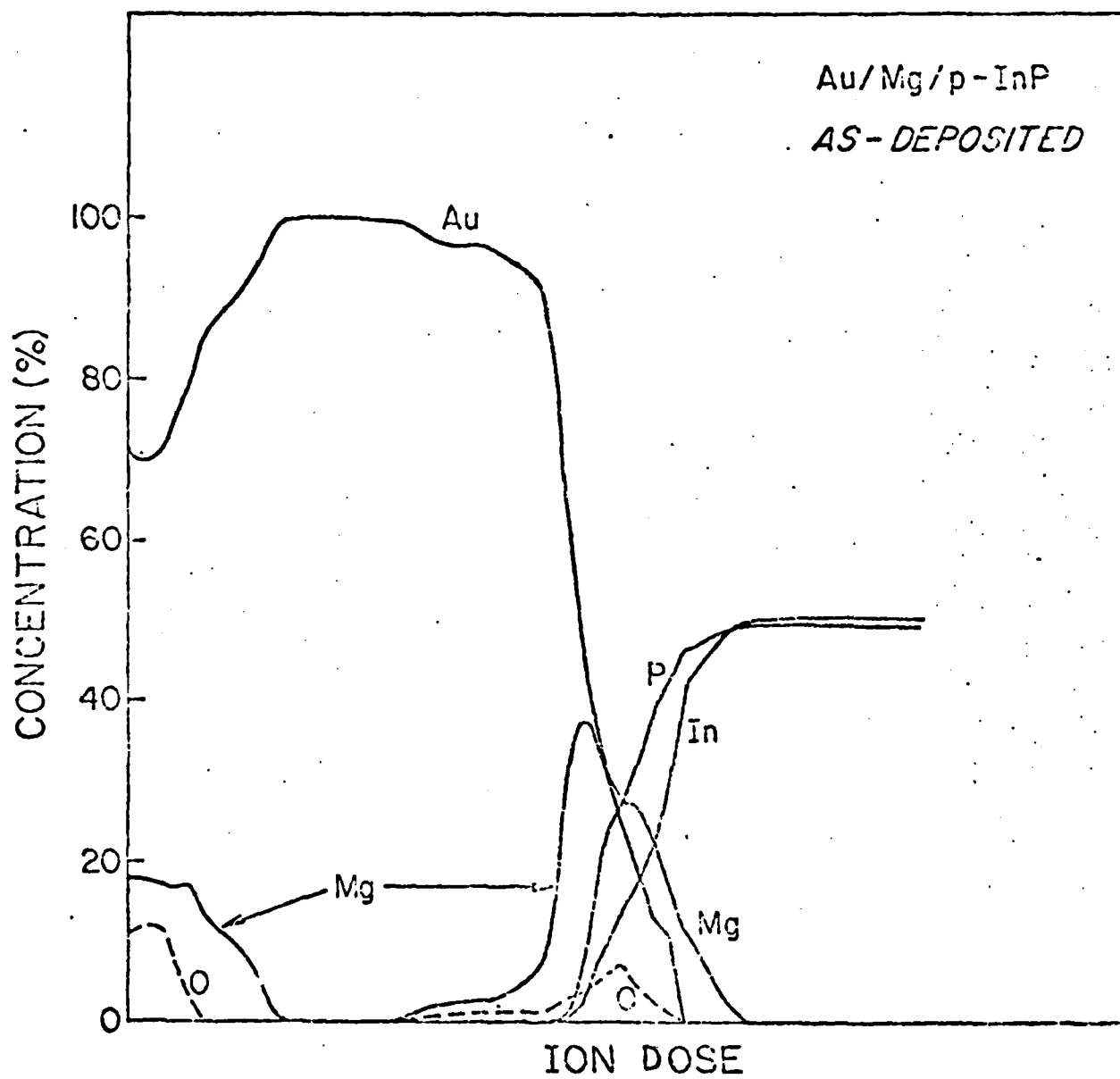


Figure 4.2(a). Auger profile of an as-deposited Au/Mg/plnP sample.

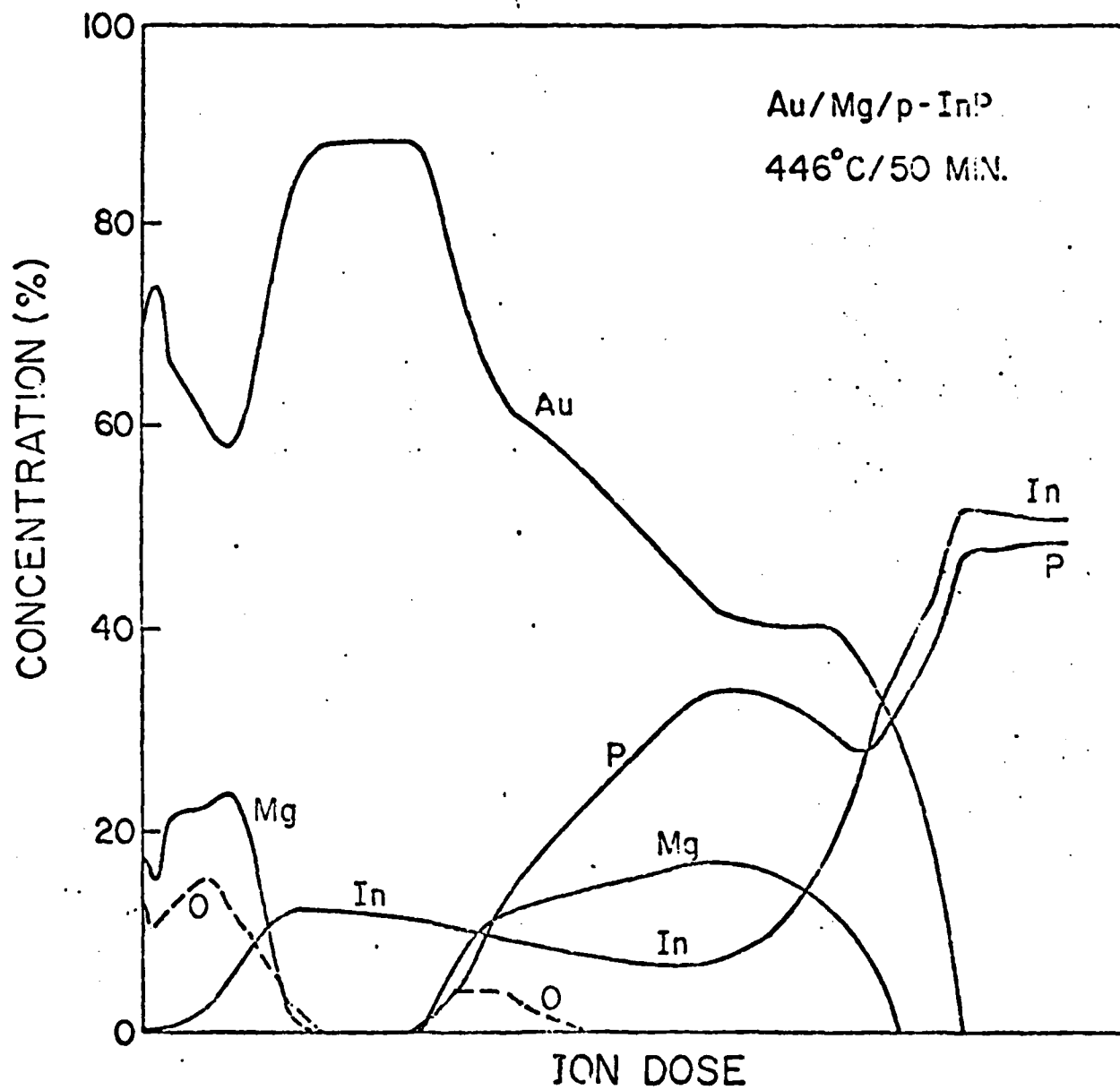


Figure 4.2(b). Auger profile of a heat-treated Au/Mg/pInP sample.

5. Pd/Mg CONTACTS ON P-TYPE InP

In this section we report the use of an alloyed Pd/Mg system for ohmic contact to p-type InP. Based on our previous experience with the Au/Mg system (see Section 4), we chose to examine Pd as an alternative to Au for this study. Pd can be easily vacuum deposited and it does not form a low temperature eutectic with In as was found for Au. Also new methods of cleaning the InP surface prior to film deposition, in hopes of reducing the oxygen available for MgO formation, are described in this section.

5.1 Experimental Procedure

A new mask-set was made similar to the three-level set used for photoelectric barrier height measurements (see Section 2.1). This mask set makes more efficient use of InP surface area and is compatible with the liftoff technique used to define the metal pattern.

Because several new etchants were used, some changes were made in the surface preparation steps of the fabrication procedure from that described earlier. The wafer was placed in the InP oxide etchant (45% wt. KOH) after the contact windows had been opened in the CVD SiO₂, but before the liftoff photolithography step. This is necessary since the KOH will strip the Shipley photoresist used. However, since the InP etchant (10% wt. HIO₃) does not seem to effect the photoresist, it was used after the liftoff photolithography step just prior to placing the wafer in the metal evaporation system. It was hoped that such a surface

preparation procedure will provide a clean interface between the metal and semiconductor.

The metal evaporation deposition was carried out in an ion-pumped vacuum system with a base pressure of 2×10^{-7} Torr. Ti sublimation pumping and high evaporation rates were employed to reduce oxygen gettering by Mg during Mg deposition. An electron beam was used to individually heat the separate hearths which held the Pd and Mg sources. In this manner a multiple layer film consisting of 400 Å of Mg evaporated onto the InP surface, and 1600 Å of Pd evaporated over the Mg film, was deposited in the same pumpdown. After metalization the excess metal was "lifted" off the wafer surface by dissolving the photoresist pattern under the metal films with acetone. The final step was scribing the wafer into individual cells before characterization and heat treatment.

5.2 Results and Discussion

A set of Pd/Mg contacts on p-InP have been fabricated and some preliminary electrical evaluation begun. The InP wafer used was supplied by the Air Force with Zn doping of approximately $2 \times 10^{17} \text{ cm}^{-3}$ and $\langle 100 \rangle$ orientation.

The as-deposited contacts exhibited Schottky diode behavior characterized by a barrier energy (ϕ_{Bp}) of about 0.8 eV, and a diode factor (n) of about 1.9. These values were determined from the current-voltage (I-V) measurement for the contacts, with the assumption of thermionic emission. The value of the Richardson constant used was $60 \text{ A}^2(\text{cm}^2 \text{ K})^{-2}$. The shape of the forward biased I-V curves, as shown in Fig. 5.1, for the as-deposited

contacts made accurate determination of the barrier height and diode factor difficult.

Heat treatments have been made at 300, 400, 500, and 600°C for ten minute periods. The contacts remained rectifying after every heat treatment. The effect of the heat treatments on ϕ_{Bp} and n is listed in Table 5.1 and the effect on the forward biased I-V characteristics is shown in Fig. 5.1. The results of reverse-bias capacitance-voltage measurements made on the same contacts are also listed in Table 5.1. Fig. 5.2 shows a typical doping profile determined by C-V measurements. The net doping $|N_A - N_D|$ obtained from C-V data was found to be uniform with depth at $2.0 \times 10^{17} \text{ cm}^{-3}$.

The surface of the contacts were examined optically with a metallurgical microscope. The as-deposited contacts were silvery in color and had a smooth texture. Adhesion of the metal films was poor, especially to the CVD SiO_2 used to define the contact areas. After heat treatment the contact surface was no longer smooth but had a rough granular texture. The contact regions also darkened in color with increasing heat-treatment temperatures. The reactions at the InP surface appeared quite different from those occurring on the SiO_2 surface surrounding the contacts.

4.3 Conclusions

Although the work on the Pd/Mg contacts is not yet complete, a few preliminary conclusions may be drawn at this point. Initially, the contact resistance is higher than for the Au/Mg case, and the surface adhesion and uniformity is poor after heat

treatment. These effects could result from a chemical reaction between the Pd and the Mg, although not predicted from thermodynamic data.²² An alternative explanation may be oxygen contamination at the Mg/InP interface, since high contact resistance was found in Au/Mg diodes with large amounts of MgO present. This latter explanation may also account for the large discrepancy between $\phi_{Bp}(I-V)$ and $\phi_{Bp}(C-V)$ in Table 5.1.

5.4 Plans for Future Work

Auger analysis will be performed to determine the extent of contamination by oxygen and carbon at the Mg/InP interface in the Pd/Mg/InP diodes. If oxidation of Mg is the principal reason for the poor electrical behavior, a new project will be initiated using an alternative p-type dopant.

Table 5.1. Characteristics of Pd/Mg Contacts on p-type InP

Heat-Treatment Temperature (°C)	I-V		C-V		Surface Appearance
	ϕ_{Bp} (eV)	n	ϕ_{Bp} (eV)	$ N_A - N_D $ (cm ⁻³)	
As-Deposited	0.8	1.9	$1.27 \pm .02$	2.0×10^{17}	smooth, silver
300	0.56 ± 0.02	1.7	1.29	----	slightly granular, silver color
400	0.54 ± 0.03	1.6	1.20	----	granular, brown tint
500	0.49 ± 0.01	1.1	0.4	----	granular, dark brown
600	0.47 ± 0.05	2	----	----	very rough, dark grey

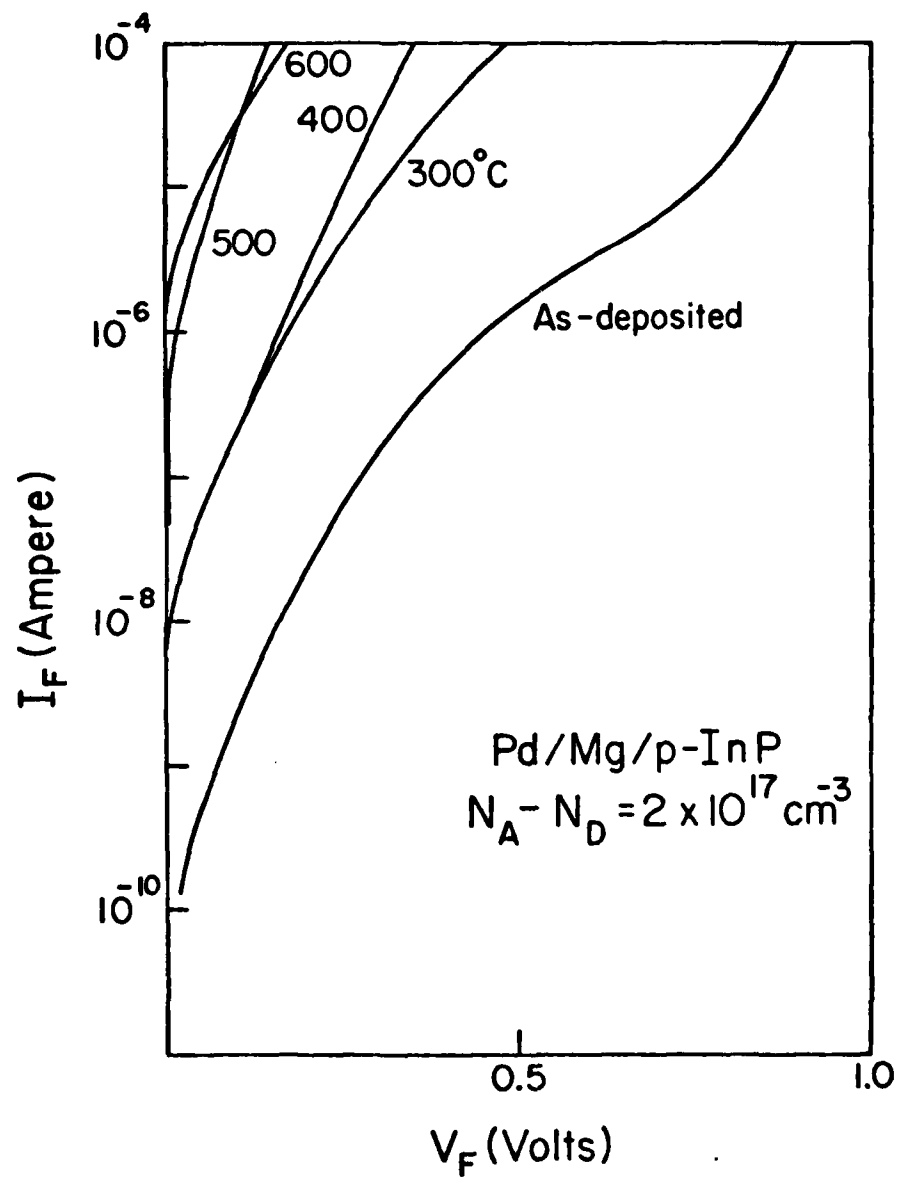


Fig. 5.1. Current-voltage characteristics of typical Pd/Mg/pInP diodes after ten minute heat treatment.

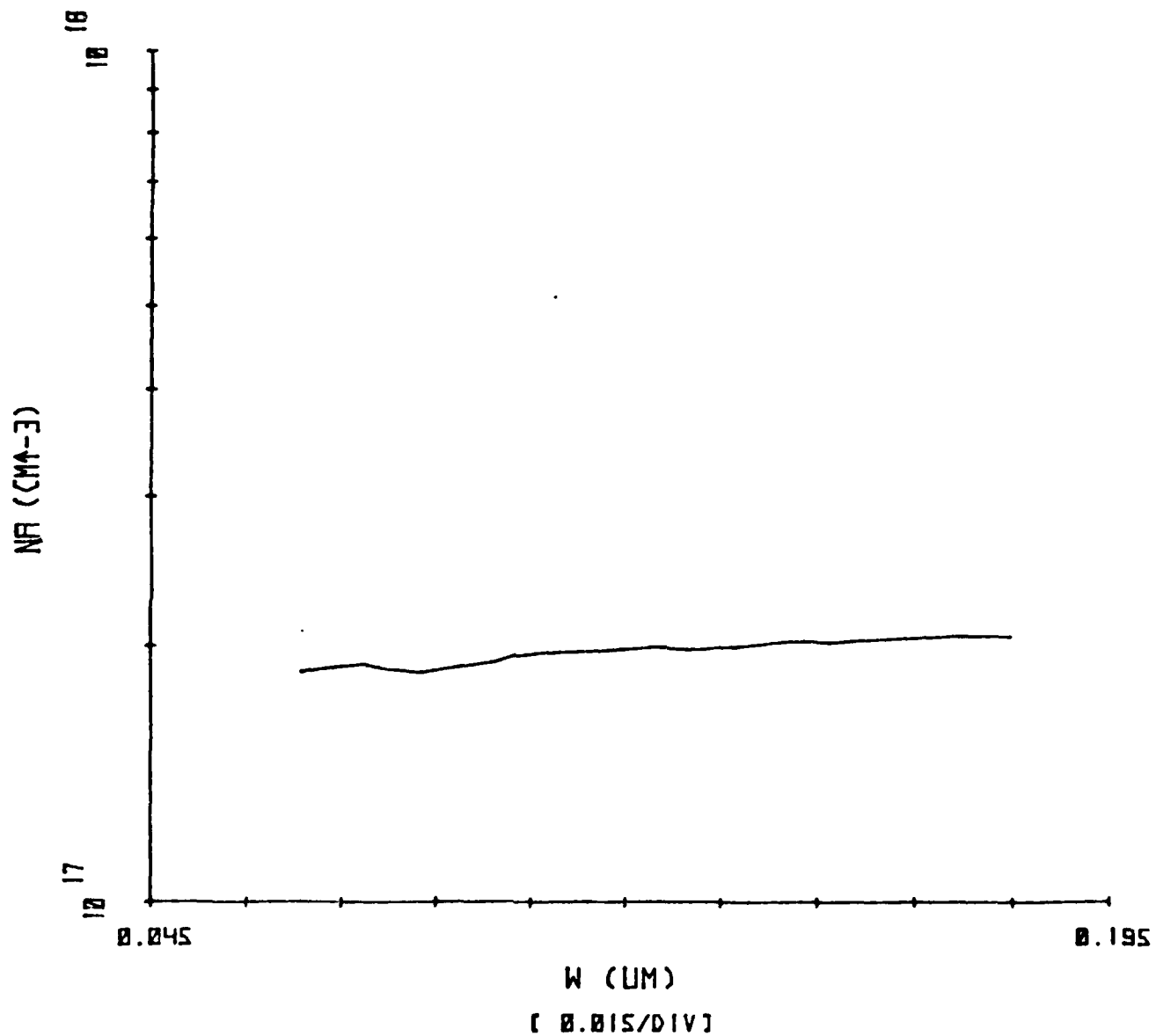


Fig. 5.2. Doping profile of p-InP wafer determined from capacitance-voltage measurements performed on as-deposited Pd/Mg contact.

6. LIST OF PUBLICATIONS

The following scientific papers have been prepared as a result of the research performed under Air Force sponsorship:

1. L. P. Erickson, A. Waseem, and G. Y. Robinson
"Characterization of Ohmic Contacts to InP", Thin Solid Films, (1979). Presented at the International Conference on Metallurgical Coatings, San Diego, CA, April 1979.
2. L. P. Erickson, "Ohmic Ni/Au/Ge Contacts to InP",
MS Thesis, University of Minnesota, 1979.
3. A. Waseem, "A Study of Au/Mg Contacts to InP", MS Thesis,
University of Minnesota, 1979.

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4. R. H. Williams, V. Montgomery, R. R. Varma, A. McKinley, J. Phys. D: Appl. Phys. 10, L253 (1977).
5. O. Wada, A. Majerfeld, Electronics Letters 14, 125 (1978).
6. J. M. Hess, P. H. Nguyen, B. Lepley, S. Ravelet, Phys. Stat. Sol. (a) 46, K55 (1978).
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8. H. T. Mills, H. L. Hartnagel, Electronics Letters 11, 921 (1975).
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