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RADC-TR-80-250, Vol I (of two)
Final Technical Report
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SEM ANALYSIS TECHNIQUES FOR LSI MICROCIRCUITS

Martin Marietta Corporation

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This report consists of two volumes. The general contents of each is as follows:

Volume I - General Information, 1024 Bit Nichrome Link PROM, 1024 Bit AIM PROM, 256 Bit Static RAM. Volume II - 1024 Bit Static RAM, 4096 Bit Dynamic RAM (SIGATE NMOS), 4096 Bit Dynamic RAM (I^2L Bipolar), Summary.

RADC-TR-80-250, Vol I (of two) has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Scanning Electron Microscope (SEM) Applications were developed and demonstrated for determining circuit configuration and organization. These applications employ voltage contrast and Electron Beam Induced Current (EBIC) techniques. Procedures were developed utilizing these applications to evaluate semiconductor memory circuits.

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These procedures provide practical methods for developing die maps, electrical circuit schematics, logic diagrams, device block diagrams and memory array bit maps. The SEM data are used in conjunction with light microscopy data to provide significant improvements in device characterization.

The memory circuits evaluated included PROMS, static and dynamic RAMS that utilized bipolar and NMOS process technologies. A total of seven circuit types were evaluated. Voltage contrast provides visual display of multiple circuit states in a single photograph. This technique is called functional mapping. It provides quick location of circuit components related to a specific functional circuit and accurate portrayal of circuit operation. Also a circuit was developed which provides high frequency functional mapping through beam blanking. EBIC evaluation is limited to bipolar and metal gate MOS because silicon gate MOS experiences severe radiation damage. EBIC identifies the diffusion locations and polarity for a major portion of a memory circuit. It is limited by parallel current paths internal to the device circuit. EBIC was found to be invaluable for schematic development of I^2L circuits.

Intentionally generated failures were utilized to demonstrate the feasibility of utilizing SEM applications for isolating circuit failures. The SEM was shown to be a valuable tool for failure isolation.

SEM operating guidelines recommend parameters and techniques for optimum instrument performance and minimal device degradation during evaluation. Limitations experienced for these applications are described These applications utilize a conventional SEM instrument.

PREFACE

THE WORK DESCRIBED IN THIS REPORT WAS PERFORMED BY THE FAILURE ANALYSIS LABORATORY OF THE MARTIN MARIETTA CORPORATION, DENVER DIVISION. THIS WORK WAS PERFORMED FOR THE RELIABILITY PHYSICS SECTION (RBRP) OF USAF ROME AIR DEVELOPMENT CENTER (RADC) UNDER CONTRACT NUMBER F30602-78-C-0354. THE WORK CONDUCTED WAS DIRECTED BY MR. JOHN BART AND LIEUTENANT MARTIN WALTER OF RADC. WE WOULD LIKE TO EXPRESS OUR APPRECIATION FOR THEIR VALUABLE SUGGESTIONS AND GUIDANCE THROUGHOUT THIS STUDY.

SIGNIFICANT CONTRIBUTIONS WERE MADE BY MS. MICHELE GOLDBERG, MR. RICHARD GIBB, MS. AUDREY COGGINS AND MR. ROY HALL OF THE MARTIN MARIETTA AEROSPACE, DENVER DIVISION, PARTS TECHNOLOGY GROUP.

This report consists of two volumes. The general content of each is as follows:

VOLUME I	General Information
	1024 Bit Nichrome Link PROM
	1024 Bit AIM PROM
	16384 Bit EPROM
	256 Bit Static Ram
VOLUME II	1024 Bit Static RAM
	4096 Bit Dynamic RAM (SIGATE NMOS)
	4096 Bit Dynamic RAM (I^2 Bipolar)
	Summary

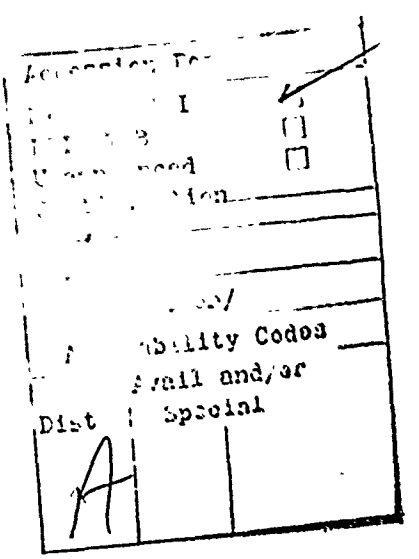


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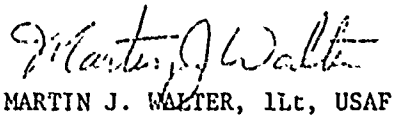
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EVALUATION

This technical report describes the application of the scanning electron microscope (SEM) to the analysis of large scale integrated circuits and the development of SEM methodology which can be used for characterization and failure analysis of these type circuits. This work supports the objectives of TPO R5B, "Solid State Device Reliability", and the associated Project 2338, "Assurance Technology for Electronics". As a following study, a SEM will be employed with an optimized detector to make quantitative voltage measurements for testing integrated circuits under the VHSIC program.

This work advanced the application of the SEM and developed methodology which will provide information critical for testing and failure analysis on LSI microcircuits.



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1.0 INTRODUCTION

The continued increase in semiconductor device circuit complexity has created the need for improved analytical approaches to support the testing and analysis of these circuits. The lack of circuit schematics, logic diagrams, die maps, test pattern sensitivities, and bit maps severely limits device test and screen program development as well as device failure analysis.

This study evaluates the application of the scanning electron microscope (SEM) to the analysis of LSI circuits. Seven semiconductor memory families were evaluated. Included were two bipolar PROMS, one silicon gate NMOS PROM, two bipolar RAMS, and two silicon gate NMOS RAMS. Even though memory devices represent only a portion of the LSI family, many of the applications described in this report can be applied as well to other circuit types.

The objective of this study was to develop SEM methodology for the characterization and failure analysis of memory circuits. The SEM has demonstrated capability for structural and electrical characterization of microcircuits. The SEM imaging capabilities were evaluated to identify practical methods and limitations for circuit characterization and for isolation of circuit failures.

SEM applications were demonstrated to not only be practical but much superior to current methods. Voltage contrast and electron beam induced current (EBIC) provide valuable data which portray circuit operation and describe circuit organization. These applications provide needed improvements for developing detailed circuitry and isolating circuit failures. The applications are demonstrated using seven types of memory circuits. Procedures are developed which describe these applications.

2.0 EVALUATION APPROACH

2.1 SELECTION OF EVALUATION DEVICES

One device type was selected from each of seven groups identified by Rome Air Development Center (RADC). The seven groups were three PROM circuits; fusible link, avalanche induced migration and ultraviolet erasable, and four RAM circuits; static bipolar, static CMOS/NMOS, dynamic MOS, and dynamic bipolar.

Device selection was based on a number of factors. Each device was evaluated with respect to its predicted usage and application in military systems. Data considered for this factor were military part specification status and present and projected Martin Marietta applications. Availability of applicable test programs was also considered. PROM devices require the capability for programming and testing these circuits.

Another factor was the degree of cooperation anticipated from the potential part supplier. Each potential supplier was contacted and the degree of cooperation evaluated. Other factors were coverage of a representative range of memory technology, parts availability and parts cost.

To provide the best evaluation of the SEM failure isolation capabilities, every effort was made to obtain functionally failed devices from the supplier. This was not completely successful because of two problems encountered. One was the reluctance of the suppliers to provide functional failures. Even though a few suppliers agreed to provide failed devices, a second problem was encountered. To be effective in evaluating the isolation of failure by SEM, the failed device must contain a functional failure internal to the chip. It was not practical to obtain devices which contained functional failures. The shortcoming of this approach is that the majority of functional circuit failures are identified and removed at wafer probe. As a result, the evaluation of SEM failure isolation was performed using circuits with intentionally introduced failures.

Five electrically good parts of each part type were considered a minimum quantity required for this study. This would provide 2 parts for circuit characterization, 2 parts for failure isolation, and 1 spare part. In addition the suppliers were requested to provide 5 to 10 mechanical samples of the same part type. These mechanical samples were used for test set-up verification, evaluation of glass passivation removal, and light microscope reference samples.

2.2 DEVICE ELECTRICAL TESTING

The purpose of electrical testing was to verify that the devices used for device characterization perform electrically and functionally per the suppliers specifications. This would avoid the possibility that a circuit malfunction would result in a circuit interpretation error. Electrical testing consisted of DC parameter measurement and functional performance verification. All testing was performed manually at room ambient temperature. DC parametric testing was performed in agreement with the manufacturer's data sheet. Functional testing of the PROM and static RAM devices was performed at 100 kHz to 1 MHz (LSB). The functional test frequency used to verify the dynamic RAMS ranged from 1.0 to 10 MHz. However, for these circuits this basic frequency and submultiples are used to generate the memory refresh signals. Therefore the read/write functional test frequency ranged from 4.0 kHz to 40 kHz. The functional test circuit design used for this study will be described in the following section. The AC switching time tests were not performed. Switching time data were not considered to be relevant to device performance for this study. Functional testing will in effect verify that circuit switching times are adequate to produce correct circuit operation.

Parametric testing was performed only during initial testing of the devices and this data was recorded for each device. Serial numbers were assigned to the devices to provide device/data identification. Functional testing of devices was performed on receipt, post decap, post passivation removal, and at various times during the period of SEM evaluation. Circuit functionality was the primary check used for this study to determine the operational condition of each circuit. This was considered to be the best method for assessing the operational status of the total circuit. It should be pointed out that parametric margins for internal circuits nodes could be compromised during passivation removal or SEM evaluation and not be evident in func-

tional testing. The primary objective is to develop an electrical schematic with reference to a normally functioning device. A functional test at room temperature using typical supply voltages and performed at an operating frequency significantly higher than that used for device characterization was considered to be satisfactory for meeting the objectives of this study.

2.3 FUNCTIONAL TEST CIRCUIT DESIGN

The first step in designing the test circuit was to identify the typical address and timing signals required for static and dynamic memory circuits. The following list identifies these requirements:

All memories (ROMS, PROMS, and RAMS)	Dynamic RAMS
Row and column addressing	Refresh
Chip enable	Write enable (pulsed)
Static RAMS	Data input (pulsed)
Data input	Address enable (pulsed)
Write enable	Row strobe, Column strobe } multiplexed address inputs

The number of active row and column address lines should be selectable to accommodate each device type. The address circuit should also provide the ability to sequentially cycle through all address states one time. This is used to check the memory response to a single write cycle. Following this write cycle the memory array is read to verify that the circuit did respond to the write command and contains the correct programmed data.

The chip enable for static and dynamic circuits can consist of a DC high or low logic level. The functionality of chip enable can be verified by manually switching the applied logic level. Another consideration would be to activate the chip only during the time that the addresses are active. This would be similar to an actual circuit application.

Static RAMS require a data input stimulus which is synchronized with the address least significant bit (LSB). The data input should provide the capability for selecting different data patterns. Such as inputs of all ones, zeros, alternating ones and zeros or zeros and ones. These patterns provide the ability to verify proper write and read operation for each memory cell.

A write enable input must be provided for static RAMS in which the enable occurs when the address and data inputs are valid and stable. A write enable signal needs to be generated for each phase of the least significant bit. This requirement necessitates that write enable be generated from the clock frequency.

Dynamic RAMS require many timing signals for operation. These signal requirements are not generally compatible with those generated for static RAMS. Larger memory devices commonly multiplex row and column address lines to reduce the number of package terminals. A major difference between stat-

ic and dynamic memory circuits is the requirement of refreshing the stored data in dynamic circuits.

Memory refreshing is generally accomplished during row address. Whenever a row is addressed, the memory cells common to that row are refreshed. To ensure maintenance of the total array's memory, a time interval is dedicated to refresh which occurs within the maximum refresh period. Typically the maximum specified refresh period is 2 to 10 ms. This refresh period is based upon operation at the maximum ambient temperature of 70°C. Typical refresh times at 25°C are 0.1 to 1.0 second. Refresh can be sychronized with the address clock and strobed in between address periods.

Another common dynamic memory requirement is the row or column select clocks. These clocks have different identification from part to part but generally have similar purposes. The primary purpose is to provide a basic time reference for circuit operation. The secondary purpose is to control address access for multiplexed addressing. The timing requirements vary widely from part to part. These variations include pulse widths, rise and fall times, and interpulse time relationships. These requirements complicate the design of a functional test circuit. Generally it is necessary to modify the test circuit to meet the individual device waveform and timing requirements. To obtain this necessary flexibility appeared to be a major problem. However through the utilization of a number of frequency dividers and basic digital gates, these requirements can generally be satisfied without much difficulty. Delays between clock events of up to 200 ns can be introduced using the combined propagation delay for multiple gate circuits. The timing usually allowed 40 ns or more margin and it was practical to satisfy these requirements with gate circuits.

The write enable pulse requirements are generally more stringent for dynamic RAMS. These requirements can be met in a manner similar to the row and column select clocks.

The general requirements for functional operation of memory devices and the approach to generation of the necessary input signals have been briefly described. It is hoped this will provide a familiarization to those who have limited experience with memory testing.

The block diagram for the functional test circuit is shown in Figures 1 and 2. TTL logic circuits were used throughout this circuit. Circuits C1 - C5 are 74193 synchronous 4 bit up/down counters. C1 and C2 are dividers which provide the refresh addresses for dynamic RAMS. These divider circuits will provide refresh addressing for up to 8 inputs. C3, C4, and C5 are dividers which provide addresses for the memory circuits. These divider circuits will accomodate up to a combination of 12 row and column addresses. The refresh and address dividers can easily be expanded to accommodate larger memory devices. A switch is provided for selecting operation for static or dynamic memories. In the static mode the refresh dividers are disabled and the clock is applied to the count input of circuit C3. An address cycle counter is provided by the 7473 flip flop. The single cycle operating mode provides the capability for verifying memory write accuracy for a single address cycle. For single cycle mode the clock is supplied to pin 3 of cir-

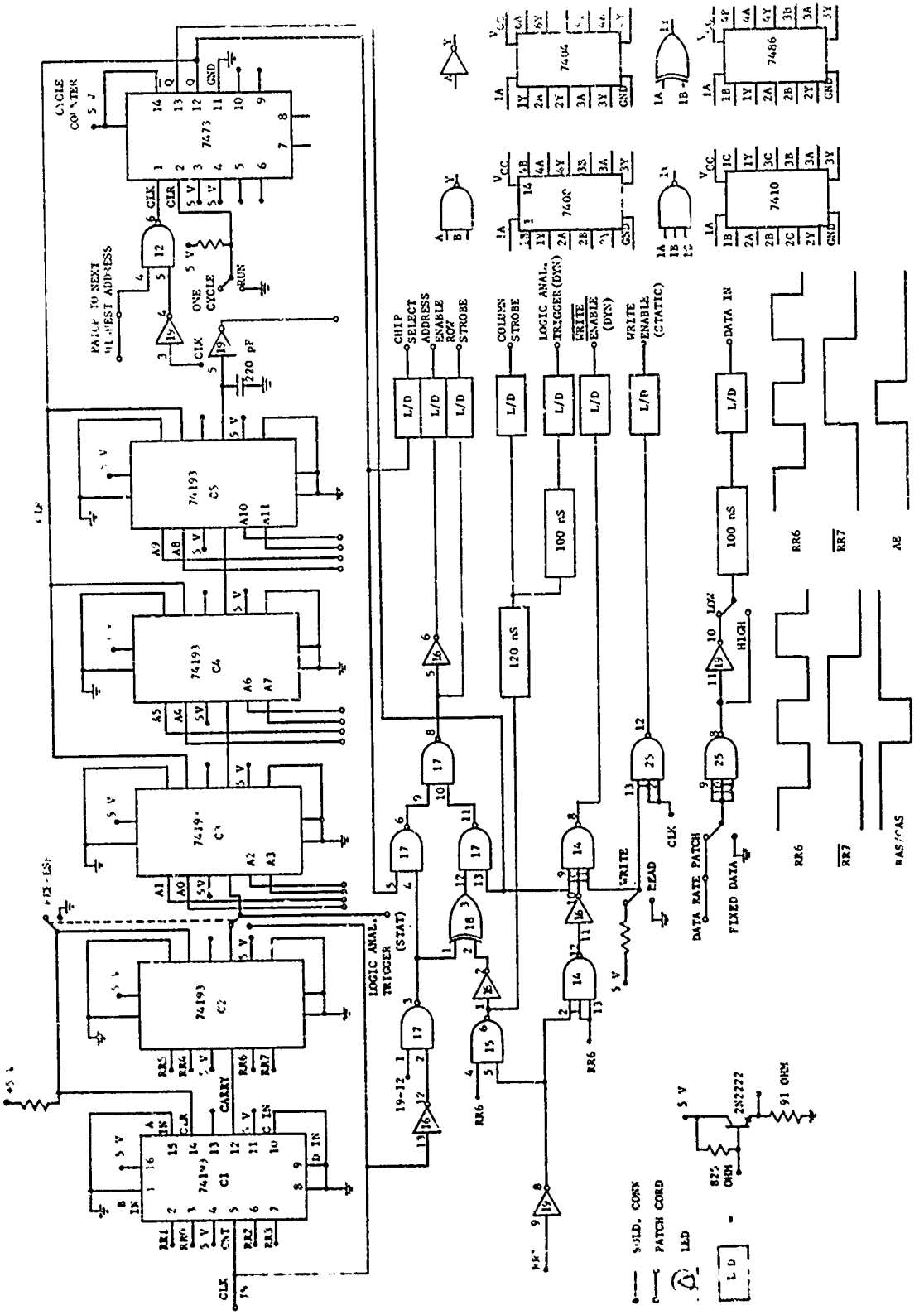


Figure 1 Static and Dynamic Time Encoder

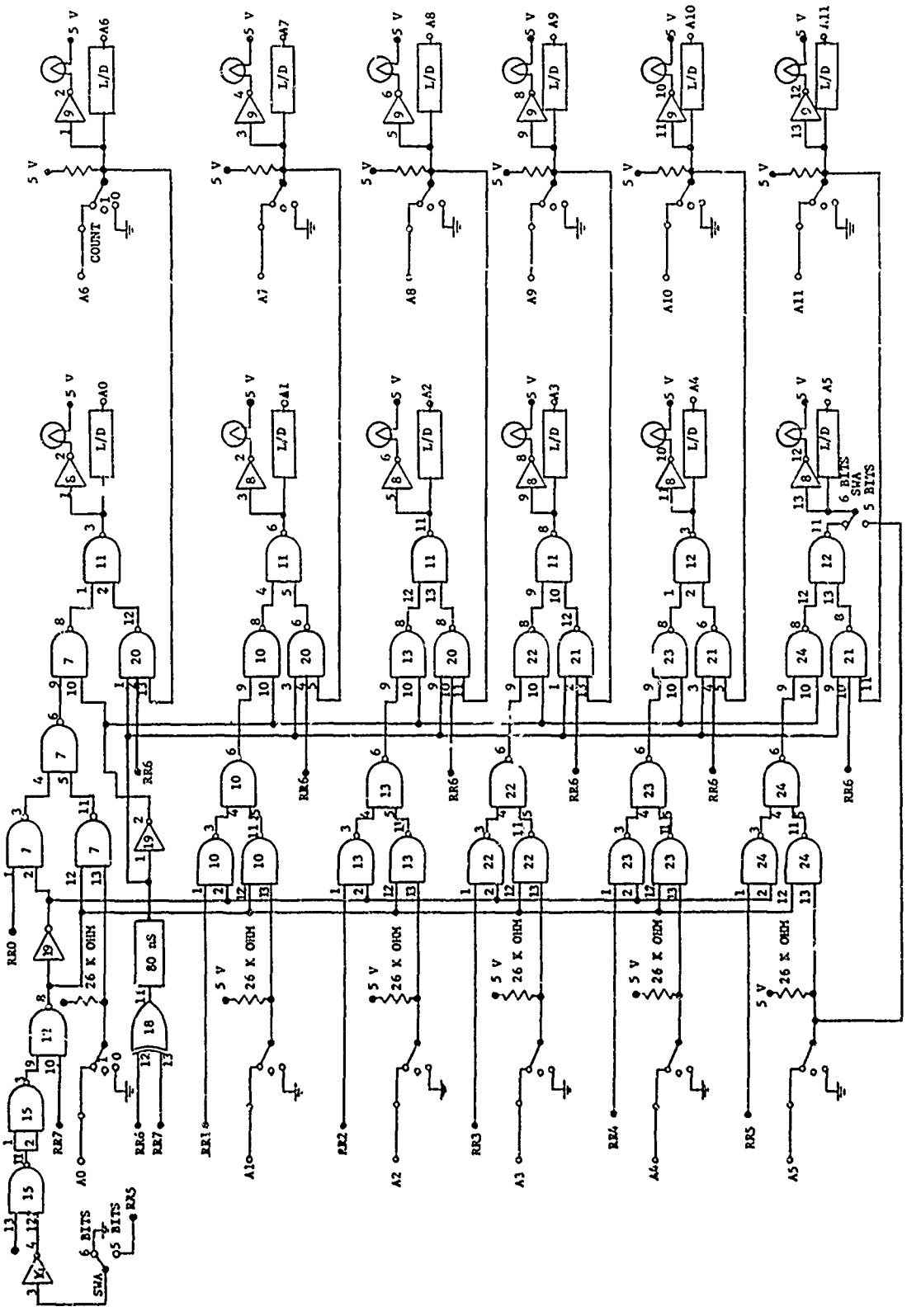


Figure 2 Static and Dynamic Address Encoder

cuit 19, and pin 4 of circuit 12 is connected by patch cord to the next highest address terminal on circuits C3 - C5. For example, if the device being tested is a 1024 x 1 bit RAM, 10 address bits are required to access the complete memory. To obtain one cycle through the complete memory, the patch cord is connected to A10 of circuit C5. With a known data pattern resident in memory, the run/cycle switch is set to cycle. When all address lines are set to zero the memory in test is write enabled and the data format selected. The run/cycle switch is momentarily set to run and returned to cycle. Note: The switch operation must be completed within the complete memory address cycle. When the single cycle is completed, the address counters are disabled and the write enable to the memory in test is manually disabled. The run/cycle switch can be returned to run and the memory data verified.

The memory control waveforms are generated in the bottom half of Figure 1. The chip select or chip enable signal is supplied from the Q output of the cycle counter. This provides a chip disable during single cycle testing. A line driver is included to maintain signal conformation through the test cable to the test device socket.

The row address strobe (NMOS 4096 bit dynamic RAM) and address enable (bipolar 4096 bit dynamic RAM) are generated from signals RR6 and RR7. When RR6 is high and RR7 is low, a low state is generated for CAS. Reference Figure 1. This low state occurs the last quarter of each phase of the A0 address. RAS and AE are generated from the same source. In addition to the read/write function of these signals they must also enable memory refresh. RAS and AE refresh clocking is enabled by the signal applied to circuit 17, pin 1 from circuit 19, pin 12. This signal provides an enable window during the second quarter of each phase of A0 address. During this period the RAS and AE signal is cycled at the system clock rate. These two signals can also be inhibited during the read/write period by the cycle counter circuit. The AE signal is RAS inverted. Two time delay circuits are included in the CAS circuit. One delays CAS to occur within the specified RAS to CAS delayed switching time. The second provides a 100 ns settling time prior to logic analyzer trigger for use on dynamic RAMS. The logic analyzer trigger for static memories is provided by the circuit clock, pin 5 of circuit C3.

Two write enable signals are generated to satisfy the requirements for static and dynamic RAMS. The write enable for dynamic RAMS is generated in the same manner as RAS including the cycle counter inhibit. The write or read mode is selected by a mechanical switch position. The write enable for static RAMS is referenced to the circuit clock. Write enable occurs during the last half of each phase of A0.

The data input signal was developed to provide four different data patterns, all highs, all lows, alternating highs and lows in phase with A0, and alternating highs and lows out of phase with A0. These two alternating data patterns are obtained by patching circuit 25 pins 9, 10, and 11 to A0. Additional alternating data patterns can be generated by patching circuit 25 to other address terminals. The 100 ns delay assures the data input state remains valid until write enable is disabled.

The static and dynamic address encoder is shown in Figure 2. This circuit provides sequential and manual addressing for static and dynamic memories. In addition, it also provides gating for applying refresh signals to row address lines. Refresh clocking is applied to the address lines during the second quarter of each phase for each row address signal. Refresh gating is controlled by circuit 16 pin 4, circuit 15 pins 3 and 11, circuit 12 pin 8, and circuit 19 pin 12. The switch connected to circuit 16 pin 3 provides refresh on 6 row address lines (A0 - A5) when input is at ground; or refresh on 5 row address lines (A0 - A4) with input connected to RR5. Side B of this switch disables the multiplexing of the A5 address line and is located at circuit 8 pin 13. The NMOS dynamic RAM contains 6 row address inputs and the bipolar dynamic RAM contains 5 row address inputs. For the NMOS circuit refresh occurs whenever RR6 and RR7 are high. For the bipolar circuit, refresh occurs whenever RR6 and RR7 are high and RR5 is low. Circuit 18 pin 11 and circuit 19 pin 2 control the row to column address multiplexing. The delay line located between the two circuits provides a delay to ensure address multiplex occurs a sufficient time after the negative transition of RAS. Address lines A0 through A6 are capable of being multiplexed. For circuits not requiring multiplexed inputs the single function address lines are used. Also each address line is capable of being manually forced high or low. These switches are needed during circuit characterization when a limited area of a device is being examined and photographed. They are also valuable during failure analysis and for identifying address sequencing for bit map generation.

The functional test circuit described in the Logic Diagrams of Figures 1 and 2 is shown in Photo 1. In this photograph the address control switches are located along the top. The address output lines are located at the top right. The static and dynamic timing lines are located along the right side.

The complete functional test system used for this study is shown in photo 2. Power is supplied to the functional test circuit and device being tested by the power supplies at the bottom of the equipment rack. Above these power supplies is the generator used to provide the clock frequency for the functional test circuit. Above the functional test circuit is the 10 x 60 pin crosspoint patchboard which provides the pin/function interface with the test device. The test cable can be connected with the device test socket or with the SEM specimen stage. The oscilloscope is used to set clock frequency, to set address and timing signal periods for voltage contrast micrography, and for verifying addressing and test device responses at the patchboard. The logic analyzer (H-P model 1601A) plays a key role in verifying the functional operation for the device being tested. The logic analyzer provides two important display modes. One is the display of address words versus device data output(s). The second is the ability to search, trigger, and display nonconforming address/output data.

2.4 DEVICE FUNCTIONAL TESTING

2.4.1 PROM/ROM TESTING

Functional testing of these devices primarily consisted of verifying programmed memory data by memory address association. This was accomplished by

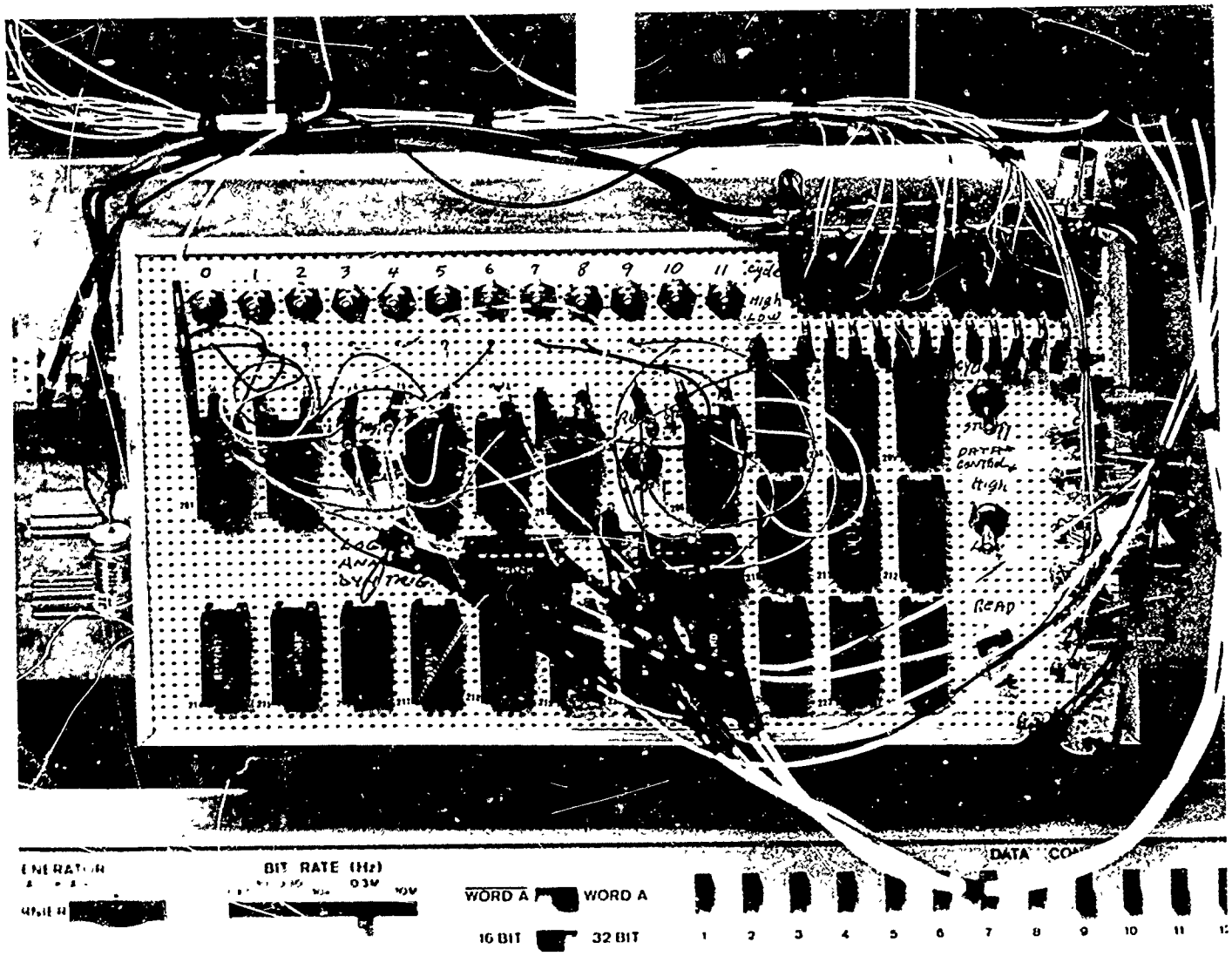


Photo 1 The Functional Test Circuit.

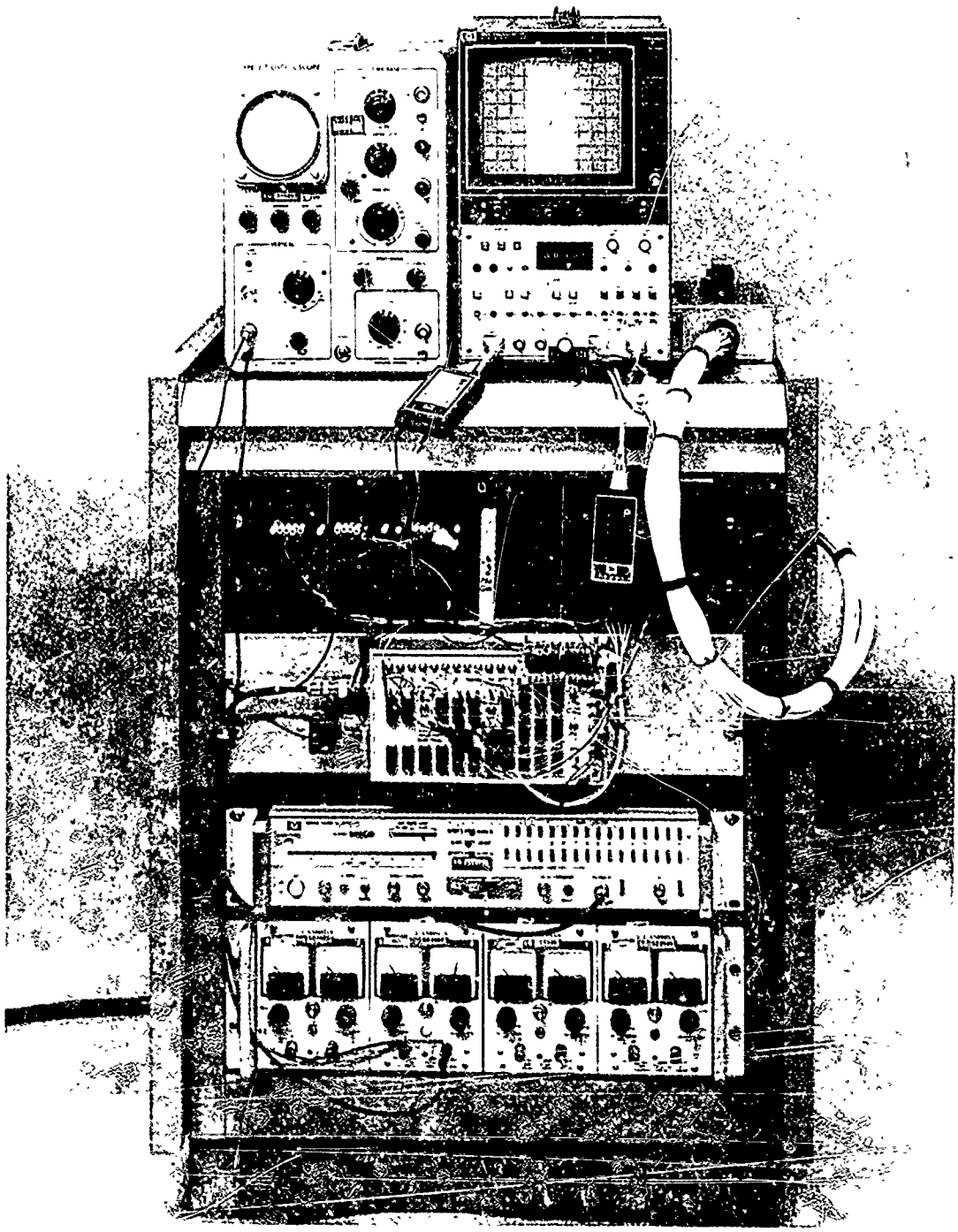


Photo 2 The Complete Functional Test System.

triggering the logic analyzer to display the address/data words sequentially in 16 word groups. The address lines and test device output data line(s) are applied to the logic analyzer signal pods. The trigger word code is set to address zero. The trigger word code for the data output line(s) is set to the off state (don't care). The logic analyzer will display the first 16 address words and their respective data output states. The data output is visually verified with the memory device programmed data sheet. The trigger word is incremented to display the next sequence of address words and output data. This procedure is continued until all memory locations have been verified. If the combined address and data output lines exceed 12 bits, the most significant bit logic levels were manually set for the address lines not monitored by the logic analyzer. This enabled all programmed data to be verified. These tests were performed using an address least significant bit (LSB) frequency of 100 kHz. All data output states are observed for stable output states. If instability is noted the address and timing signals should be checked and verified to be in agreement with the device data sheet. Adequate power supply decoupling should be verified.

2.4.2 RAM TESTING

The functional testing of RAM devices is more involved but the output data verification procedure is less difficult than for ROM devices. A specific data format is first written into memory. This is performed during a single sequential address cycle. At the completion of the write cycle the circuit is write disabled. The written data pattern is then read out and verified. The test consisted of writing all highs, verify; write all lows, verify; write alternating highs and lows, verify; and then write alternating lows and highs and verify. Verification of memory data is accomplished as follows. When all highs were written into memory the logic analyzer trigger word is set so that the address bits are off and data bits are low. If there is more than one output each is trigger tested individually. If there are any low memory data bits the logic analyzer will be triggered and display the data error and memory address. If there is more than one error the complete memory array must be manually scanned and the errors listed. Later model logic analyzers can be programmed to list all errors. This same write and verify procedure is used for written lows. For alternating highs and lows where the data written is in phase with the address LSB, verification is accomplished as follows. The trigger word is set for an address LSB low and data bit high. If no trigger occurs the data has been correctly written and read. This checks half of the memory array. The second half is checked by setting trigger word for address LSB high and data bit low. This same procedure is used for alternating data written out of phase with the address LSB. The trigger word is set so it will trigger on in-phase data. These functional data verification tests can be quickly performed. A more thorough functional test of each memory cell can be performed by writing alternating highs and lows using the data rate of A0 and incrementing up to the device address MSB. For example, for a 1024 bit memory the data rate would begin with 0, 1, 0, 1 and increment to 0, 0, 1, 1 using A1 and continuing up to A9 which would produce 512 0's and 512 1's. This procedure verifies that a single address is not writing data in two or more memory cell locations. The data rate is easily changed by patching the data input circuit 25 pin 9 to the appropriate address clock terminal on circuits C3-C5.

Memory data is verified using the logic analyzer address/data trigger. These functional tests were performed using a typical address LSB of 100 kHz for static memories and 40 kHz for dynamic memories. All data outputs were checked for stability. Dynamic memories were observed for specific data patterns for two to three minutes to verify memory data refresh. Adequate power supply decoupling is very important in obtaining stable device operation. Also clean address and timing waveforms were found to be very important. The signals generated by the functional test circuit required line drivers to provide satisfactory waveform quality.

2.5 DEVICE/SEM INTERFACE

The device/SEM interface used in this study had been developed to support previous integrated circuit applications. This interface is easily adapted to applying signals and power to the test device for voltage contrast, and can be quickly converted to provide device/sample current amplifier (SCA) interconnections for electron beam induced current (EBIC). The interface conversion is accomplished external to the specimen stage. Signals and power are applied to the test device through a 60 pin high vacuum connector on the specimen stage. This connector is compatible with the plug on the functional test system cable. The conversion to EBIC involves removing the plug from the stage and attaching the SCA switch matrix. Photo 3 shows the specimen stage with the 60 pin SCA switch matrix and the 16 pin ground switch matrix in place. Switch closure on the SCA matrix interconnects the selected device terminal(s) and the SCA input. Likewise, switch closure on the ground matrix connects the selected device terminal(s) to ground. The SCA matrix provides minimal lead lengths to minimize stray pick-up.

The device interface inside the specimen stage also should be easily adapted to different styles and sizes of packages. Photo 4 shows the interconnect scheme inside the specimen stage. The 24 pin dual-in-line adapter is shown in the foreground of this photo. The smaller connector provides the ground matrix connection and the larger connector makes connection with the SCA switch matrix or functional test cable. The wire harness is shielded to reduce pickup and charging. The 16 pin dual-in-line adaptor is shown installed in the stage. This interface performed satisfactorily for all seven device types evaluated in this study.

2.6 EVALUATION OF SEM APPLICATIONS

An electrical schematic is necessary in understanding the significance of circuit failures. In less complex circuits the schematics and die maps could be easily developed using light microscopy and photographs. As circuit complexity increases the practicality of developing schematics and die maps using only light optics is lessened. This is basically due to the complications of bookkeeping necessary to keep track of circuit interconnections. Other methods were needed to supplement the light optics data. The SEM applications were evaluated to determine if they can provide these additional methods.

The examination of integrated circuits using voltage contrast has been performed almost since the inception of the SEM. The ability to display low

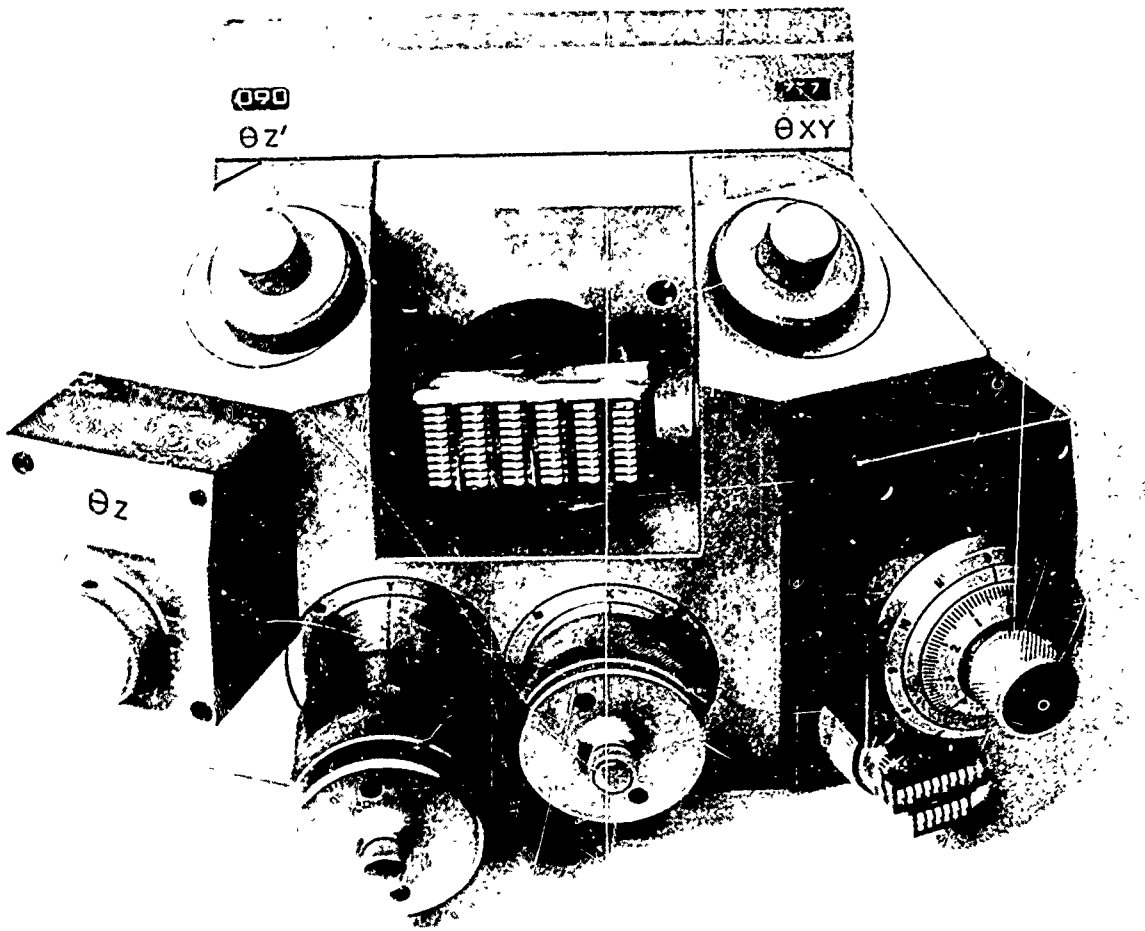


Photo 3 The Specimen Stage Showing the 60 Pin SCA Switch Matrix and the 16 Pin Ground Switch Matrix.

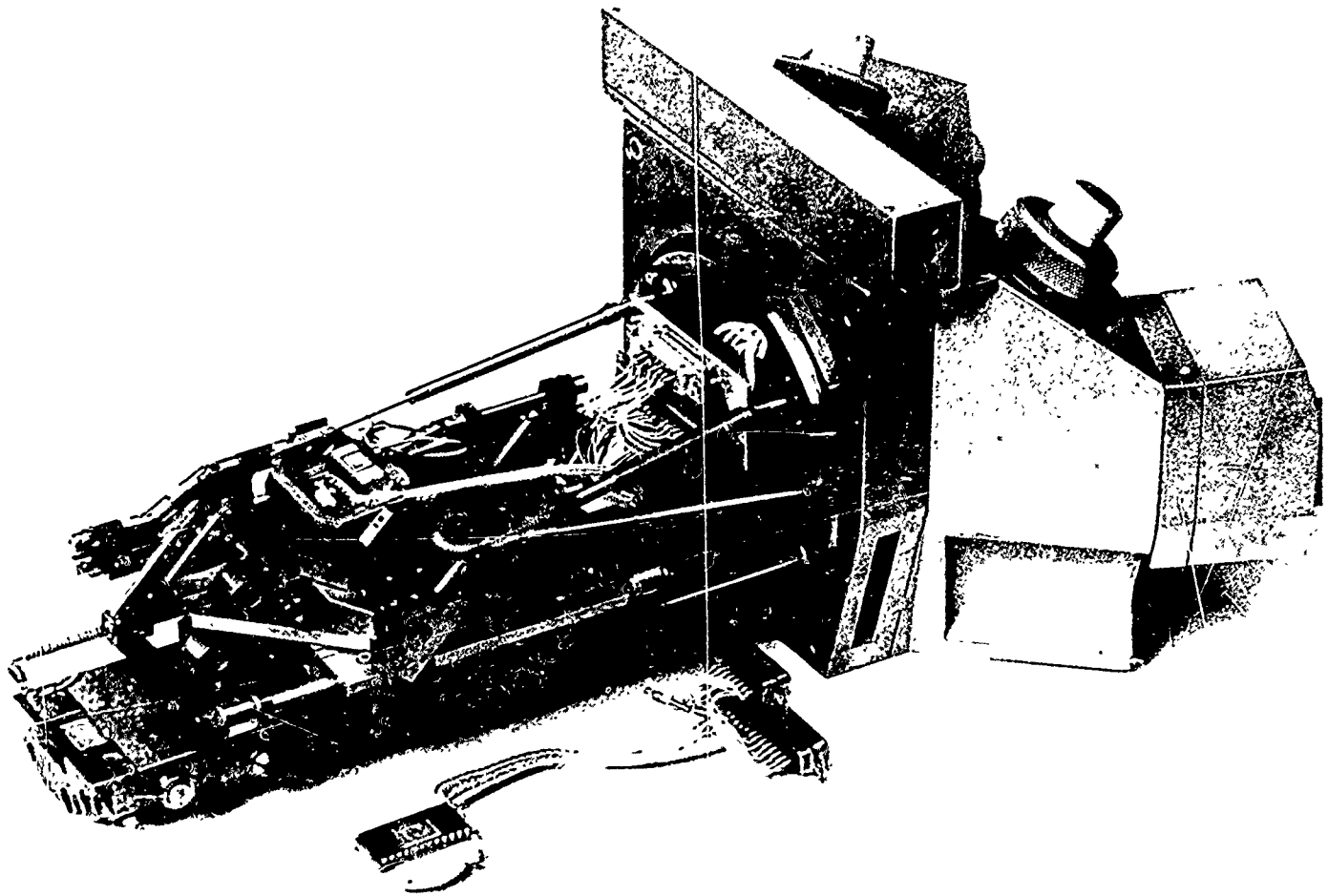


Photo 4 The Specimen Stage Showing the Internal Device Interface.

frequency circuit operation using voltage contrast was demonstrated early in the application of the SEM. This capability has been largely ignored in favor of displaying high frequency circuit operation by stroboscopic beam blanking. Stroboscopic circuit examination generally is performed using TV scan rates. The image typically displays a single logic state for the circuit being examined. These conditions are not well suited to circuit analysis for the purpose of schematic development. Higher scan rates require increased beam currents to improve signal to noise ratios and higher beam currents increase surface charging. Also it is difficult to adapt this data to a hard copy format. In order to document multiple circuit states it would require two or more photographs. The interpretation of circuit state data is complicated by the examination of individual circuit nodes in two or more photographs.

A comparison with the low frequency voltage contrast imaging approach shows it to be more advantageous. It is easily adapted to low speed scan rates as well as TV scan rates. This allows the use of low beam currents. Photographic documentation is routine and a single photographic image can contain dc and multiple circuit states. This provides improved recognition of small delta voltages by adjacent signal contrast striping. Low frequency imaging can be accomplished with a standard SEM instrument. A possible limitation was the practicality of this application to dynamic memory circuits. Examination of both static and dynamic memory circuits during this study has shown low frequency imaging is not only practical but superior. It provides identification of supply busses, multiple frequency display, discrimination of individual circuit boundaries, relative circuit node voltage amplitude, and intracircuit signal phase relationships all in a single photograph. This SEM application can best be described as functional mapping.

In developing an electrical schematic for a chip circuit, there is no single technique that provides complete visibility for locating circuit components and identifying chip organization. Light and electron optics techniques nicely complement one another for circuit characterization. A large amount of information can be obtained by light microscopy. For characterization of small scale integrated circuits light microscopy was sufficient. Medium scale integration required additional time and perserverance, but light microscopy is still practical. Large scale integrated circuits (LSI) and very large scale integrated (VLSI), circuit characterization by light microscopy alone has become impractical. Circuit tracing requires the identificaton of interfacing signal and clock lines which arrive from and depart to circuitry outside the field of view. The bookkeeping for identifying these interfaces require each line be visually traced from the source and appropriately identified. The SEM provides valuable assistance in addressing this problem. The light microscope and SEM together can reduce the cost of circuit characterization.

The light microscope is effective for identifying metal to metal and metal to diffusion contacts, common diffusions by oxide color, and specific diffusion elements; e.g., emitter, base, drain, source, resistor, Schottky clamp, and Darlington cells.

SEM secondary electron imaging (SEI) provides a similar capability to the light microscope. It provides higher resolution and depth of field but does not provide identification of common oxides or examination beneath oxide surfaces.

SEM functional mapping identifies the boundaries for a specific functioning circuit, power supply busses, relative circuit node potentials, interfacing signal and clock lines, and operating signal phase relationships. The functional operation can be photographically documented for visual analysis. This provides an important reference for correlating circuit operation to the developed electrical schematic.

SEM EBIC provides the ability to display the location of diffusions. This SEM mode is limited by parallel circuit paths which prevent external EBIC signal flow. It was shown to be invaluable in the development of I^2L circuit schematics. Also EBIC is capable of locating diffusions obscured by covering metallization. As will be shown later, EBIC examination of silicon gate MOS is not practical due to irradiation damage.

As stated earlier each analytical technique has its strong points and no single technique can satisfy all the requirements for proper and efficient circuit characterization.

2.7 CIRCUIT FAILURE GENERATION

The true test of isolating circuit failures would be to use actual device failures. Therefore a significant effort was made to obtain actual device failures for evaluation. A problem was encountered with this approach in that device failures were not available. There are two primary reasons for this. First and foremost is that device failures which are identified after packaging are to a large majority mechanical failures; e.g., broken wires, open bonds, damaged metallization, cracked die, and out of tolerance electrical parameters. The majority of functional failures which could be used to test an isolation technique are removed at die probe. A few suppliers made a sincere effort to provide typical failures for evaluation. Functional testing of these failures initially showed they would be good candidates for evaluation. When these devices were opened the cause of failure was visually obvious. Of seventeen failed devices obtained none were found suitable for evaluating failure isolation. The second reason was the majority of suppliers refused to provide failed devices. The primary reason given was that data obtained from failures might be misinterpreted or misrepresented.

The other alternative was to intentionally introduce failures into a device. Initially this appeared to be a reasonable approach. What was not realized was mechanical probing leaves an easily observed indication of where the failure is located. This would certainly prejudice the evaluation of the failure isolation technique. Also it was assumed that an internal circuit could be easily damaged. Various attempts to introduce failures produced unsatisfactory results. It was not possible to force the voltage high enough or to sufficiently localize the current to produce localized circuit damage. Even short duration pulses were not successful. This was

primarily due to a multitude of parallel circuit paths which are present in complex circuits. Basically two methods were used to produce functional failures. One was to open metallization and the second was to use a high energy electron beam to irradiate a single transistor. Metallization was opened by masking and etching the conductor open or by mechanical scribing. When scribing the metallization, care was taken to minimize visual evidence. Degradation of circuit operation by irradiation was not successful for bipolar transistors due to circuit margins and irradiation tolerance. Every effort was made to provide a fair evaluation of techniques to detect and isolate failure sites.

3.0 DEVICE CHARACTERIZATION

3.1 EVALUATION METHODS

The objective of this study is to evaluate the application of the SEM to characterization of memory devices. There are a number of possible applications and the intent is to evaluate their advantages and practicality as compared with existing light optic methods. When limitations are encountered they are assessed to determine modifications necessary to overcome or work around the limitation in order to obtain optimum performance. Limitations which cannot be resolved are identified. Applications are evaluated to determine the circuit stimulus requirements for visual observation and photographic documentation. These applications are demonstrated and evaluated using seven types of memory circuits. The results were compiled to provide procedures for utilization of these applications.

3.1.1 ELECTRICAL SCHEMATIC/DIE MAP

Development of the electrical schematic and die map represent the major effort in characterizing device circuitry. It is also the key element in enabling an intimate understanding of circuit operation. This data forms the basis for development of the logical and functional diagrams and bit map for the circuit.

The individual circuit functions were evaluated using voltage contrast, EBIC and SEI in conjunction with light microscopy. The optimum conditions for providing the necessary data for development of the electrical schematic were determined. The circuit definition sequence which should be followed was identified. The recommended procedures for tracing the circuit and developing the electrical schematic and die map are described.

Procedures were developed which are based upon experience gained in analysis and characterization of these memory circuits. These procedures provide guidance in the use of these applications. It is intended that these procedures be applicable for general use with conventional SEM instruments on the majority of memory circuits and other complex digital circuits. The only nonstandard instrument capabilities needed are a sample current amplifier for EBIC imaging and beam blanking for higher frequency functional mapping if desired. Of these two capabilities the sample current amplifier would be more valuable. Special effort was made to provide a procedure which does

not require special instrument modifications, capabilities, or accessories. The instrument used in this study was a Cambridge stereoscan 180. The basic instrument provides TV scanning rates and this instrument also contains beam blanking and a sample current amplifier.

3.1.2 LOGIC DIAGRAM

The logic diagram must be derived from the circuit electrical schematic. The basic purpose is to provide a simplified logical description of circuit operation. Logic diagrams were constructed using basic logic elements to depict circuit operation for functional blocks. There is no established procedure for developing a logic diagram for a circuit. A single circuit can be described logically in numerous configurations and they all can be considered acceptable. A logic diagram should be drawn so that it can be easily evaluated by observation.

3.1.3 FUNCTIONAL BLOCK DIAGRAM

The functional block diagram is also derived from the circuit electrical schematics. The purpose is to provide a simplified description of the overall circuit and identification of the primary signal and control line interconnections. The major circuit functions can be quickly determined from this diagram. For this study the major circuit functions were shown in a block diagram and also located by a block outline on a complete die photo. The photo functional block provides familiarity with the die organization. In the majority of the devices for this study, functional blocks were identifed which were not included on the supplier's data sheet.

3.1.4 BIT MAP

A bit map is a graphical guide for determining the physical position of a memory cell for each row and column address code combination. The bit map can be used to identify adjacent memory cell addresses. These data are required for testing memory circuits for pattern sensitivities. Memory addressing was examined by voltage contrast. It was determined that by using a simple voltage contrast examination procedure, a bit map can be generated in approximately 60 minutes.

4.0 CHARACTERIZATION RESULTS

This section of the report describes the results obtained from the evaluation of seven memory circuits. The text for each part type appears first, followed by the tables, photographs, and figures for that part type. The callout for these data are abbreviated to simplify identification. The major paragraph number is omitted from these callouts. For example, the first photo for the first part type would normally be Photo 4-1-1. To simplify the callout this photo will be identified as Photo 1-1.

4.1 1024 BIT NICHROME LINK PROM (BIPOLAR)

Device Description

This device is a 256 x 4 bit bipolar PROM. The memory array is field programmable with programming accomplished by fusing open thin film nichrome links. The circuit version evaluated contained two chip enable inputs and three state collector outputs. The devices were packaged in a 16 lead ceramic DIP with a ceramic lid.

Electrical Characterization

Ten 1024-Bit Nichrome Link Field Programmable Bipolar PROMs were used for this study. They were received as engineering samples. All devices contained the same programmed pattern and this was obtained from the supplier (Table 1-I).

Upon receipt, eight of the units were electrically tested in accordance with the supplier data sheet. They were serialized to keep individual device identification. The DC parameters were measured and recorded and are listed according to serial number in Table 1-II. All DC parameters were verified to match the vendor specification at room temperature.

The eight devices were functionally tested to verify compliance with the programmed memory pattern. Verification was performed using the memory test circuit in conjunction with a Hewlett-Packard 1601A Logic Analyzer. The analyzer displayed the eight bit address codes and the respective four output data bits. These 12 bits are displayed 16 rows at a time on a CRT. An eight bit trigger word is selected and this is displayed at the top of the screen followed serially by the next 15 words and their corresponding outputs. The trigger word is changed to display 16 words at a time to verify that the outputs match the table supplied by the vendor. All eight devices were found to match the program. The functional test frequency was approximately 100 kHz.

Package Delid and Glass Passivation Removal

This device was packaged in a 16 pin dual in-line ceramic package. The die cavity was exposed by mechanically grinding the lid on a diamond impregnated wheel. When the outline of the cavity was clearly visible the grinding was stopped and a probe was used to break the remainder of the package lid. Care was taken to avoid damage to the die or interconnect wires.

Removal of the glass passivation was first attempted on one of the two devices on which data had not been taken. The device was subjected to 3 minutes of Siloxide Etchant followed by a DI water rinse and an isopropyl alcohol rinse. Siloxide Etchant is made specifically for the selective removal of deposited SiO_2. The etch rate is approximately 40 angstroms per second at room temperature. Three minutes, therefore, removed about 7200 angstroms. The part was found to be fully functional at this time, however, there was a small amount of passivation remaining. An additional 20 seconds

of Siloxide Etchant removed the remaining passivation and left the device functioning properly.

Serial Number 1 was then stripped using Siloxide Etchant for 200 seconds. A photograph of the complete die was then taken (ref Photo 1-1).

Circuit Characterization

S/N 1 was placed in a SEM test socket which provides electrical connection between the device and an external connector on the SEM specimen stage. Complete functional testing could then be performed on the device while viewing its operation using voltage contrast on the SEM.

The acceleration voltage used for the examination was 5 kv. Good quality voltage contrast photographs could be obtained at this level while the effect of the beam on the circuit operation was minimized. Initial familiarization with the circuit was obtained by operating it at low frequencies, 1 to 20 Hz, while observing the address buffers, decode circuits, inputs, outputs and general layout.

Following this familiarization, the individual functional circuits were examined. The first circuit examined was the row address buffer. Photo 1-2 is the voltage contrast micrograph showing the A6 input. This photo was taken with all row address inputs cycling. Input A6 was cycling at 0.7 Hz. The active circuitry involved with this input can easily be identified by the width of the dark and light stripes. The voltage present on the circuit modulated the intensity of the secondary electron image with the dark areas being at the higher voltage and the brightest areas near ground. This same area was photographed on the light microscope, Photo 1-3. In addition, a SEI and an EBIC image of a row address input were taken, Photos 1-4 & 1-5. NOTE: All EBIC images were taken using an acceleration voltage of 15 kv with pin 8 (gnd) at ground; all remaining pins connected to the sample current amplifier. A portion of the junctions are visible; however, in situations where parallel current paths exist for the induced current the junctions are not displayed in the EBIC image. These four photographs were then used to determine the electrical schematic. After the initial attempt at the circuit schematic the operation was reviewed and any questions resolved. The circuit schematic for the row address buffer is shown in Figure 1-1 and the logic diagram is shown in Figure 1-2. The row address inverters utilize Schottky clamped transistors and Schottky diodes. The top half of this circuit generates the inverse of the input logic level. The bottom half of the circuit generates the in phase logic level. There are five row address circuits and each generates two address signals for the row decoder circuits.

The two outputs from each row address then go into the row decode section of the device. The voltage contrast photograph of this section is shown in Photo 1-6 and the light microscope photograph is shown in Photo 1-7. The voltage contrast photo was taken with address A3 cycling at 0.7 Hz and addresses A4 to A7 held at a high state. The EBIC image Photo 1-8, shows the dark row of emitter diffusions within the base diffusion and also the col-

lector diffusion. The secondary electron image (SEI) of this same region is shown in Photo 1-9. The circuit schematic for the row decoder is shown in Figure 1-3 and the logic diagram in Figure 1-4. To address a given row, the six emitter diffusions in the base diffusion must all go high. Five of these emitter contacts are associated with A3 - A7 and the sixth is associated with the decoder used for addressing the two extra rows on this device. These two rows will be discussed in detail later. When the base diffusion goes high, a row is selected and the data in those memory cells can be read. A column must also be addressed to select a particular word in that row. The column address circuitry is described next.

The column address buffer is similar to the row address buffer. The voltage contrast photograph is shown in Photo 1-10 and the light microscope photograph is shown in Photo 1-11. The voltage contrast photo was taken with address A0 cycling at 0.7 Hz. The EBIC image of this area is shown in Photo 1-12 and the SEI in Photo 1-13. In this EBIC image the transistor cells Q1, Q3, and Q4 provide a vivid response while the buffer output transistors Q2 and Q5 are not visible. This is due to the diodes between the collectors and V_{cc}. An EBIC response is obtained from the two diodes D6 and D13 which are connected to V_{cc} through a resistor. However, these same diodes block the EBIC from diodes D7 and D14. The circuit schematic is shown in Figure 1-5 and the logic diagram is shown in Figure 1-6. This is the A0 input and it also goes to an extra column in the memory as will be discussed later. The column address circuits are the same as the row address circuits. The circuits generate an in phase and out of phase signal for the column decode circuit. There are three column address circuits used in this device.

These two outputs from each column address then go into the column decode section of the device. The voltage contrast photograph of this section is shown in Photo 1-14 and the light microscope photograph is shown in Photo 1-15. This voltage contrast photo was taken with column address A0 cycling at 0.7 Hz and A1 and A2 held at a low state. The EBIC image of this area, Photo 1-16, again shows the dark emitter diffusions within the base diffusion. The emitter contacts are easily identified for each decode transistor. This area is also shown in the SEI photograph, Photo 1-17. The circuit schematic is shown in Figure 1-7 and the logic diagram is shown in Figure 1-8. To address a given column, the three emitter diffusions in the large base diffusion must all go high. When these emitters are high, transistor Q1 is turned on and is driven by transistor Q2 through the collector resistor R1. Each column address decodes four separate columns, one in each section of eight bits, which then go to the four individual outputs.

Examination of the memory cell will then allow one to gain an understanding of the interaction between the row decode, the column decode, and the output circuit. The voltage contrast photograph is shown in Photo 1-18 and the light microscope photograph is shown in Photo 1-19. The voltage contrast photo was taken with address A3 cycling at 0.7 Hz with all other address inputs forced high. The circuit schematic is shown in Figure 1-9 and the logic diagram is shown in Figure 1-10. A row of memory cells consists of four groups of eight bits each. These thirty-two bits have a common base contact

which goes to the row decode, a common collector contact which goes to V+ and individual emitters which go the nichrome fusible links. The fusible links are in the shape of an hour glass, and when they are programmed, the necked down portion opens. These NiCr links then go to the column decode lines. If the link is fused open, transistor Q1 in the column decode will have an open collector and the output drive is from transistor Q2 in the column decoder. When the fuse is intact the drive to the output is from V+ on the collector of the memory cell transistor, through the NiCr link and transistor Q1 to the output section.

In the output section, this small voltage difference is amplified into a high or low output condition. The voltage contrast photograph is shown in Photo 1-20 and the light microscope photograph is shown in Photo 1-21. The voltage contrast photo was taken with memory being cycled between words 231 and 239 at 0.7 Hz. The EBIC image Photo 1-22, shows the diffusions in this section and was again taken at 15 kv. EBIC does not show the base diffusions for transistors Q3 and Q4 because the base-collector junctions are paralleled by a resistor as shown in the circuit schematic. The secondary electron image of this area is shown in Photo 1-23. The circuit schematic is shown in Figure 1-11 and the logic diagram in Figure 1-12.

The current flow in R1, Q1 and Q2 is partly controlled by the circuit labeled as the sense amplifier current sink. This circuit is shown in Photo 1-24 and the schematic is shown in Figure 1-13. During normal operation, transistor Q2 is biased on and current flows through it to ground. The remainder of this circuit is discussed in the programming section.

The chip enable circuitry goes to three separate points in the output. When the CE input is high, these points go low and the output is disabled. The impedance looking into the output will be high under these conditions. With the chip enabled, the voltage which appears on the base of Q2 (Figure 1-11) is amplified and inverted twice in reaching the output.

The chip enable section will be covered next. The voltage contrast photograph of this section is shown in Photo 1-25 and the light microscope photograph is shown in Photo 1-26. The voltage contrast photo was taken with CE2 input cycling at 0.7 Hz and CE1 cycling at 0.3 Hz. The EBIC and SEI photographs are shown in Photo 1-27 and 1-28. The EBIC response for the input diodes D3 - D5 and D6 - D8 shows the variations that can be encountered in an interconnected circuit. Even with these limitations it can be a valuable asset. The circuit schematic is shown in Figure 1-14 and the logic diagram is shown in Figure 1-15. Both of these inputs must be low to obtain a high condition on the output line, marked CE in the schematic. CE goes to each of the four outputs as discussed in the last section. If either of the CE inputs are high, transistor Q4 is driven into saturation and its collector goes low.

To program the fusible links on this device, the two chip enable-not lines are taken high, V_{CC} is raised to approximately 12 volts and 10 volts is applied to each of the output pins to open the links. Whichever word is addressed at that time will be programmed. If a high is desired in a specific

memory location, then that output is held low rather than being raised to 10 volts. The voltage contrast photograph of the area involved is shown in Photo 1-29 and the light microscope photograph is shown in Photo 1-30. The voltage contrast photo was taken with output pin cycling zero to 12 volts at 0.7 Hz. There is one of these circuits per output and the star on Photo 1-29 is connected to the column decode circuitry at the star in Photo 1-31. The schematic of this circuit and the other circuits involved in the programming are shown in Figure 1-16.

When the two chip enable not lines go high, the output sections of the chip are disabled. V_{CC} then goes to 12 volts which applies 12 volts to the collectors of the memory cells. The 10 volts on the output breaks down diode D1 in Figure 1-16 and turns transistor Q1 on. This creates a current path through the selected row transistor and the selected column transistor to the forward biased diode D2 and the saturated transistor Q1. This high current fuses open the NiCr link.

Another circuit which is involved during the programming operation was shown in Photo 1-24 and the circuit schematic was shown in Figure 1-13. When V_{CC} goes to 12 volts, the zener diode D1 breaks down and turns on transistor Q1. The voltage then is reduced below that necessary to turn transistor Q2 on. With this transistor off, no current will flow through it during the programming operation and it will not be damaged.

In addition to the circuitry discussed to this point there is additional circuitry which allows the programmability of the chips to be tested without fusing the NiCr links on any of the 1,024 bits that are normally used. There are two extra columns which can be programmed and two extra rows.

The extra columns are labeled A and B and are shown in the voltage contrast photographs, Photo 1-32 and 1-33. Column A in Photo 1-32 has its NiCr links tied to a metallization stripe which is connected to pin 13, CE. Column B in Photo 1-33 is connected to pin 5, AO. In column A there are NiCr links in rows 34 and 33 and then in the odd numbered rows for the next 32. In column B there are NiCr links in rows 34 and 33 and then in the even numbered rows for the next 32. These memory cells can be read out at pins 5 and 13 and there will be a voltage difference between open conditions and the intact fuses.

These memory cells can be programmed by addressing each of the rows with pins 5 and 13 shorted to ground. It is necessary for each of these NiCr links to be fused open or high current will flow into a low input on pins 5 and 13. These extra columns allow all of the rows to be checked for proper addressing.

The extra rows are numbered 33 and 34. In row 34 alternating columns have fuses and opens. In row 33 all of the fuses were initially intact however, they were fused open. This allows each of the columns to be tested for programmability. The circuit which allows rows 33 and 34 to be addressed is shown in the voltage contrast photograph, Photo 1-34, and the light microscope photograph, Photo 1-35. The voltage contrast photo was taken with A7

input cycling zero to 10 volts at 0.7 Hz. The EBIC image is shown in Photo 1-36, and the SEI is shown in Photo 1-37. The EBIC response for transistors Q2 and Q6 show the emitter, base and collector diffusions. As usual the response for the majority of the cells exhibits wide variations. The schematic is shown in Figure 1-17 and the logic diagram in Figure 1-18. The A7 input, pin 15, is raised above the breakdown voltage of diode D1 which is approximately 7 volts and transistor Q1 is turned on. This pulls the metallization stripe low which is tied to rows 1 - 32 and disables them. Also transistor Q4 is turned off so the input to lines 33 and 34 appears as a high condition. Row 33 is addressed with A7 at about 8 volts, and A3 low. Row 34 is addressed with A7 at about 8 volts and A3 and A5 high. With these conditions then A0 - A2 can be cycled to address each of the columns and obtain normal outputs or for programming.

The circuit in the upper part of the row 33, 34 schematic operates as follows. With 5 volts on V_{cc} transistor Q7 is off, transistor Q6 is on and therefore, the collector of Q5 is around 3 volts, keeping rows 1 - 32 enabled. When V+ is raised to 12 volts, Q7 will turn on, Q6 will turn off and the base-collector junction of Q5 will act like a diode with the base being held at 7 volts by diode D7. This assures that rows 1 - 32 are enabled. When A7 is raised to 8 volts then current will flow through R5, the base-collector of Q5 and then through D2 and Q1 to ground.

The chip organization is shown in Photo 1-38. A block diagram is shown in Figure 1-19. The block diagram shows the extra rows and columns which were not included in the vendors data sheet. The die dimensions are 100 mils by 140 mils and the die has aluminum metallization and aluminum ultrasonic bonds. The overall circuit was also viewed using EBIC, (Photo 1-39). This type of presentation allows for rapid location of the different functional areas on the die. It can also be a valuable tool for failure analysis providing determination of a failure location.

A bit map was generated for this chip. This is a simple task when using voltage contrast. The bit map provides the ability to determine the memory bit location for any address. This is shown in Figure 1-20.

Failure Analysis

This section will cover the procedure for producing, analyzing and locating a failure.

A device was electrically measured to verify functionality. It was then opened and the glass passivation chemically removed. The device was rechecked at this time to verify full functionality. thin coating of Tech wax was melted onto the die surface to protect the metallization from a later aluminum etch. Using a mechanical probing station two small areas of wax were removed over metallization stripes. The part was then etched in Aluminum Etchant at 50°C for 30 seconds. This procedure created two open circuits, one between the pull up resistor R2 and the collector of the column decode transistor Q3, and the second between V_{cc} and the collector of the output transistor Q4.

The failure was induced into the device by one person and then the analysis performed by a second person. The analyst was not informed of the damage induced into the part in an attempt to simulate more closely the condition which would exist in a normal failure analysis.

The failure in the column decode circuit would not allow the 011 code to be addressed so the associated output stayed low. This affected 24 words. In Table 1-I wherever the column address is 011 and an output is supposed to be a 1, a 0 would occur. The address words which were in error were noted and the part placed in the SEM. The column decode was examined with the input clock running at 1 to 2 Hz. The failed column was quite apparent. A photograph of the area, Photo 1-40, revealed the open metallization. This photo was taken with A2 input cycling at 0.7 Hz. A higher magnification photograph is shown in Photo 1-41.

The open condition on the output transistor Q4 did not cause a functional failure. The output is shown functioning properly in Photo 1-42 with the open metallization. This photo was taken with the memory being cycled between words 147 and 179 at 0.7 Hz. When the output is low, transistor Q5 is in saturation with the collector current being supplied through R3, the base-emitter of Q4 and D4. When the output is high transistor Q5 is off and the voltage is still present at the output via the same path.

A second device was opened and the same procedure followed. On this device the connection between the memory section base and the row decode base was etched open (ref schematic Figure 1-3). This goes to the half of the memory associated with the Q1 and Q2 output transistors.

The functional test found the output for the row address code 11110 for the Q1 and Q2 outputs to always stay low. This failure was easily confirmed on the SEM with the device slowly cycling through the memory cells.

With this connection open, the common base region for each of the memory cells is left floating and each time a column is addressed and the NiCr link is intact this base region goes high. Photo 1-43 shows several rows being addressed with the failed row appearing dark at the same time. This photo was taken with A0 and A1 low, A6 and A7 high, and A2, A3, A4, and A5 cycling at 0.5 Hz, 0.25 Hz, 0.125 Hz, and 0.065 Hz respectively. Photo 1-44 shows the failed row being addressed and the row to its left alternately being addressed. This photo was taken with A0 and A1 low, A6 and A7 high, and A2, A3, A4, and A5 cycling at 0.5 Hz, 0.25 Hz, 0.125 Hz, and 0.065 Hz respectively. In the memory section no change occurs on the failed row.

TABLE 1-I PROGRAMMED DATA LISTING

INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1	INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	32	0	0	0	0
0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	33	0	0	0	0
0	0	0	0	0	0	1	0	2	0	0	0	0	0	0	1	0	0	0	1	0	34	0	0	0	0
0	0	0	0	0	0	1	1	3	0	0	0	0	0	0	1	0	0	0	1	1	35	0	0	0	0
0	0	0	0	0	1	0	0	4	0	0	0	0	0	0	1	0	0	1	0	0	36	0	0	0	0
0	0	0	0	0	1	0	1	5	0	0	0	0	0	0	1	0	0	1	0	1	37	0	0	0	0
0	0	0	0	0	1	1	0	6	0	0	0	0	0	0	1	0	0	1	1	0	38	0	0	0	0
0	0	0	0	0	1	1	1	7	0	0	0	0	0	0	1	0	0	1	1	1	39	0	0	0	0
0	0	0	0	1	0	0	0	8	0	0	0	0	0	0	1	0	1	0	0	0	40	0	0	0	1
0	0	0	0	1	0	0	1	9	0	0	0	0	0	0	1	0	1	0	0	1	41	0	0	0	1
0	0	0	0	1	0	1	0	10	0	0	0	0	0	0	1	0	1	0	1	0	42	0	0	0	1
0	0	0	0	1	0	1	1	11	0	0	0	0	0	0	1	0	1	0	1	1	43	0	0	0	1
0	0	0	0	1	1	0	0	12	0	0	0	0	0	0	1	0	1	1	0	0	44	0	0	0	1
0	0	0	0	1	1	0	1	13	0	0	0	0	0	0	1	0	1	1	0	1	45	0	0	0	1
0	0	0	0	1	1	1	0	14	0	0	0	0	0	0	1	0	1	1	1	0	46	0	0	0	1
0	0	0	0	1	1	1	1	15	0	0	0	0	0	0	1	0	1	1	1	1	47	0	0	0	1
0	0	0	1	0	0	0	0	16	0	0	0	0	0	0	1	1	0	0	0	0	48	0	0	0	0
0	0	0	1	0	0	0	1	17	0	0	0	0	0	0	1	1	0	0	0	1	49	0	0	0	0
0	0	0	1	0	0	1	0	18	0	0	0	0	0	0	1	1	0	0	1	0	50	0	0	0	0
0	0	0	1	0	0	1	1	19	0	0	0	0	0	0	1	1	0	0	1	1	51	0	0	0	0
0	0	0	1	0	1	0	0	20	0	0	0	0	0	0	1	1	0	1	0	0	52	0	0	0	0
0	0	0	1	0	1	0	1	21	0	0	0	0	0	0	1	1	0	1	0	1	53	0	0	0	0
0	0	0	1	0	1	1	0	22	0	0	0	0	0	0	1	1	0	1	1	0	54	0	0	0	1
0	0	0	1	0	1	1	1	23	0	0	0	0	0	0	1	1	0	1	1	1	55	0	0	0	1
0	0	0	1	1	0	0	0	24	0	0	0	0	0	0	1	1	1	0	0	0	56	0	0	0	1
0	0	0	1	1	0	0	1	25	0	0	0	0	0	0	1	1	1	0	0	1	57	0	0	0	1
0	0	0	1	1	0	1	0	26	0	0	0	0	0	0	1	1	1	0	1	0	58	0	0	0	1
0	0	0	1	1	0	1	1	27	0	0	0	0	0	0	1	1	1	0	1	1	59	0	0	1	0
0	0	0	1	1	1	0	0	28	0	0	0	0	0	0	1	1	1	1	0	0	60	0	0	1	0
0	0	0	1	1	1	0	1	29	0	0	0	0	0	0	1	1	1	1	0	1	61	0	0	1	0
0	0	0	1	1	1	1	0	30	0	0	0	0	0	0	1	1	1	1	1	0	62	0	0	1	0
0	0	0	1	1	1	1	1	31	0	0	0	0	0	0	1	1	1	1	1	1	63	0	0	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

TABLE 1-I (cont)

INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1	INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1
0	1	0	0	0	0	0	0	64	0	0	0	0	0	1	1	0	0	0	0	0	96	0	0	0	0
0	1	0	0	0	0	0	1	65	0	0	0	0	0	1	1	0	0	0	0	1	97	0	0	0	0
0	1	0	0	0	0	1	0	66	0	0	0	0	0	1	1	0	0	0	1	0	98	0	0	0	0
0	1	0	0	0	0	1	1	67	0	0	0	0	0	1	1	0	0	0	1	1	99	0	0	0	1
0	1	0	0	0	1	0	0	68	0	0	0	1	0	1	1	0	0	1	0	0	100	0	0	0	1
0	1	0	0	0	1	0	1	69	0	0	0	1	0	1	1	0	0	1	0	1	101	0	0	0	1
0	1	0	0	0	1	1	0	70	0	0	0	1	0	1	1	0	0	1	1	0	102	0	0	1	0
0	1	0	0	0	1	1	1	71	0	0	0	1	0	1	1	0	0	1	1	1	103	0	0	1	0
0	1	0	0	1	0	0	0	72	0	0	1	0	0	1	1	0	1	0	0	0	104	0	0	1	1
0	1	0	0	1	0	0	1	73	0	0	1	0	0	1	1	0	1	0	0	1	105	0	0	1	1
0	1	0	0	1	0	1	0	74	0	0	1	0	0	1	1	0	1	0	1	0	106	0	0	1	1
0	1	0	0	1	0	1	1	75	0	0	1	0	0	1	1	0	1	0	1	1	107	0	1	0	0
0	1	0	0	1	1	0	0	76	0	0	0	1	0	1	1	0	1	1	0	0	108	0	1	0	0
0	1	0	0	1	1	0	1	77	0	0	0	1	0	1	1	0	1	1	0	1	109	0	1	0	0
0	1	0	0	1	1	1	0	78	0	0	0	1	0	1	1	0	1	1	1	0	110	0	1	0	1
0	1	0	0	1	1	1	1	79	0	0	0	1	0	1	1	0	1	1	1	1	111	0	1	0	1
0	1	0	1	0	0	0	0	80	0	0	0	0	0	1	1	1	0	0	0	0	112	0	0	0	0
0	1	0	1	0	0	0	1	81	0	0	0	0	0	1	1	1	0	0	0	1	113	0	0	0	0
0	1	0	1	0	0	1	0	82	0	0	0	0	0	1	1	1	0	0	1	0	114	0	0	0	0
0	1	0	1	0	0	1	1	83	0	0	0	0	0	1	1	1	0	0	1	1	115	0	0	0	1
0	1	0	1	0	1	0	0	84	0	0	0	1	0	1	1	1	0	1	0	0	116	0	0	0	1
0	1	0	1	0	1	0	1	85	0	0	0	1	0	1	1	1	0	1	0	1	117	0	0	1	0
0	1	0	1	0	1	1	0	86	0	0	0	1	0	1	1	1	0	1	1	0	118	0	0	1	0
0	1	0	1	0	1	1	1	87	0	0	1	0	0	1	1	1	0	1	1	1	119	0	0	1	1
0	1	0	1	1	0	0	0	88	0	0	1	0	0	1	1	1	1	0	0	0	120	0	0	1	1
0	1	0	1	1	0	0	1	89	0	0	1	0	0	1	1	1	1	0	0	1	121	0	0	1	1
0	1	0	1	1	0	1	0	90	0	0	1	1	0	1	1	1	1	0	1	0	122	0	1	0	0
0	1	0	1	1	0	1	1	91	0	0	1	1	0	1	1	1	1	0	1	1	123	0	1	0	0
0	1	0	1	1	1	0	0	92	0	0	1	1	0	1	1	1	1	1	0	0	124	0	1	0	1
0	1	0	1	1	1	0	1	93	0	1	0	0	0	1	1	1	1	1	0	1	125	0	1	0	1
0	1	0	1	1	1	1	0	94	0	1	0	0	0	1	1	1	1	1	1	0	126	0	1	1	0
0	1	0	1	1	1	1	1	95	0	0	0	0	0	1	1	1	1	1	1	1	127	0	1	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

TABLE 1-I (cont)

INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1	INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1
1	0	0	0	0	0	0	0	128	0	0	0	0	1	0	1	0	0	0	0	0	160	0	0	0	0
1	0	0	0	0	0	0	1	129	0	0	0	0	1	0	1	0	0	0	0	1	161	0	0	0	0
1	0	0	0	0	0	1	0	130	0	0	0	1	1	0	1	0	0	0	1	0	162	0	0	0	1
1	0	0	0	0	0	1	1	131	0	0	0	1	1	0	1	0	0	0	1	1	163	0	0	0	1
1	0	0	0	0	1	0	0	132	0	0	1	0	1	0	1	0	0	1	0	0	164	0	0	1	0
1	0	0	0	0	1	0	1	133	0	0	1	0	1	0	1	0	0	1	0	1	165	0	0	1	1
1	0	0	0	0	1	1	0	134	0	0	1	1	1	0	1	0	0	1	1	0	166	0	0	1	1
1	0	0	0	0	1	1	1	135	0	0	1	1	1	0	1	0	0	1	1	1	167	0	1	0	0
1	0	0	0	1	0	0	0	136	0	1	0	0	1	0	1	0	1	0	0	0	168	0	1	0	1
1	0	0	0	1	0	0	1	137	0	1	0	0	1	0	1	0	1	0	0	1	169	0	1	0	1
1	0	0	0	1	0	1	0	138	0	1	0	1	1	0	1	0	1	0	1	0	170	0	1	1	0
1	0	0	0	1	0	1	1	139	0	1	0	1	1	0	1	0	1	0	1	1	171	0	1	1	0
1	0	0	0	1	1	0	0	140	0	1	1	0	1	0	1	0	1	1	0	0	172	0	1	1	0
1	0	0	0	1	1	0	1	141	0	1	1	0	1	0	1	0	1	1	0	1	173	1	0	0	0
1	0	0	0	1	1	1	0	142	0	1	1	1	1	0	1	0	1	1	1	0	174	1	0	0	0
1	0	0	0	1	1	1	1	143	0	1	1	1	1	0	1	0	1	1	1	1	175	1	0	0	1
1	0	0	1	0	0	0	0	144	0	0	0	0	1	0	1	1	0	0	0	0	176	0	0	0	0
1	0	0	1	0	0	0	1	145	0	0	0	0	1	0	1	1	0	0	0	1	177	0	0	0	0
1	0	0	1	0	0	1	0	146	0	0	0	1	1	0	1	1	0	0	1	0	178	0	0	0	1
1	0	0	1	0	0	1	1	147	0	0	0	1	1	0	1	1	0	0	1	1	179	0	0	1	0
1	0	0	1	0	1	0	0	148	0	0	1	0	1	0	1	1	0	1	0	0	180	0	0	1	0
1	0	0	1	0	1	0	1	149	0	0	1	0	1	0	1	1	0	1	0	1	181	0	0	1	1
1	0	0	1	0	1	1	0	150	0	0	1	1	1	0	1	1	0	1	1	0	182	0	1	0	0
1	0	0	1	0	1	1	1	151	0	0	1	1	1	0	1	1	0	1	1	1	183	0	1	0	0
1	0	0	1	1	0	0	0	152	0	1	0	0	1	0	1	1	1	0	0	0	184	0	1	0	1
1	0	0	1	1	0	0	1	153	0	1	0	1	1	0	1	1	1	0	0	1	185	0	1	1	0
1	0	0	1	1	0	1	0	154	0	1	0	1	1	0	1	1	1	0	1	0	186	0	1	1	0
1	0	0	1	1	0	1	1	155	0	1	1	0	1	0	1	1	1	0	1	1	187	0	1	1	1
1	0	0	1	1	1	0	0	156	0	1	1	0	1	0	1	1	1	1	0	0	188	1	0	0	0
1	0	0	1	1	1	0	1	157	0	1	1	1	1	0	1	1	1	1	0	1	189	1	0	0	0
1	0	0	1	1	1	1	0	158	0	1	1	1	1	0	1	1	1	1	1	0	190	1	0	0	1
1	0	0	1	1	1	1	1	159	1	0	0	0	1	0	1	1	1	1	1	1	191	1	0	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

TABLE 1-I (concl)

INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1	INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q4	3	2	1
1	1	0	0	0	0	0	0	192	0	0	0	0	1	1	1	0	0	0	0	0	224	0	0	0	0
1	1	0	0	0	0	0	1	193	0	0	0	0	1	1	1	0	0	0	0	1	225	0	0	0	0
1	1	0	0	0	0	1	0	194	0	0	0	1	1	1	1	0	0	0	1	0	226	0	0	0	1
1	1	0	0	0	0	1	1	195	0	0	1	0	1	1	1	0	0	0	1	1	227	0	0	1	0
1	1	0	0	0	1	0	0	196	0	0	1	1	1	1	1	0	0	1	0	0	228	0	0	1	1
1	1	0	0	0	1	0	1	197	0	0	1	1	1	1	1	0	0	1	0	1	229	0	1	0	0
1	1	0	0	0	1	1	0	198	0	1	0	0	1	1	1	0	0	1	1	0	230	0	1	0	1
1	1	0	0	0	1	1	1	199	0	1	0	1	1	1	1	0	0	1	1	1	231	0	1	1	0
1	1	0	0	1	0	0	0	200	0	1	1	0	1	1	1	0	1	0	0	0	232	0	1	1	1
1	1	0	0	1	0	0	1	201	0	1	1	0	1	1	1	0	1	0	0	1	233	0	1	1	1
1	1	0	0	1	0	1	0	202	0	1	1	1	1	1	1	0	1	0	1	0	234	1	0	0	0
1	1	0	0	1	0	1	1	203	1	0	0	0	1	1	1	0	1	0	1	1	235	1	0	0	1
1	1	0	0	1	1	0	0	204	1	0	0	1	1	1	1	0	1	1	0	0	236	1	0	1	0
1	1	0	0	1	1	0	1	205	1	0	0	1	1	1	1	0	1	1	0	1	237	1	0	1	1
1	1	0	0	1	1	1	0	206	1	0	1	0	1	1	1	0	1	1	1	0	238	1	1	0	0
1	1	0	0	1	1	1	1	207	1	0	1	1	1	1	1	0	1	1	1	1	239	1	1	0	1
1	1	0	1	0	0	0	0	208	0	0	0	0	1	1	1	1	0	0	0	0	240	0	0	0	0
1	1	0	1	0	0	0	1	209	0	0	0	0	1	1	1	1	0	0	0	1	241	0	0	0	0
1	1	0	1	0	0	1	0	210	0	0	0	1	1	1	1	1	0	0	1	0	242	0	0	0	1
1	1	0	1	0	0	1	1	211	0	0	1	0	1	1	1	1	0	0	1	1	243	0	0	1	0
1	1	0	1	0	1	0	0	212	0	0	1	1	1	1	1	1	0	1	0	0	244	0	0	1	1
1	1	0	1	0	1	0	1	213	0	1	0	0	1	1	1	1	0	1	0	1	245	0	1	0	0
1	1	0	1	0	1	1	0	214	0	1	0	0	1	1	1	1	0	1	1	0	246	0	1	0	1
1	1	0	1	0	1	1	1	215	0	1	0	1	1	1	1	1	0	1	1	1	247	0	1	1	0
1	1	0	1	1	0	0	0	216	0	1	1	0	1	1	1	1	1	0	0	0	248	0	1	1	1
1	1	0	1	1	0	0	1	217	0	1	1	1	1	1	1	1	1	0	0	1	249	1	0	0	0
1	1	0	1	1	0	1	0	218	1	0	0	0	1	1	1	1	1	0	1	0	250	1	0	0	1
1	1	0	1	1	0	1	1	219	1	0	0	0	1	1	1	1	1	0	1	1	251	1	0	1	0
1	1	0	1	1	1	0	0	220	1	0	0	1	1	1	1	1	1	1	0	0	252	1	0	1	1
1	1	0	1	1	1	0	1	221	1	0	1	0	1	1	1	1	1	1	0	1	253	1	1	0	0
1	1	0	1	1	1	1	0	222	1	0	1	1	1	1	1	1	1	1	1	0	254	1	1	0	1
1	1	0	1	1	1	1	1	223	1	1	0	0	1	1	1	1	1	1	1	1	255	1	1	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

TABLE 1-1I DC PARAMETERS

1	2	3	4	5	6	7	8	SPEC MIN	SPEC MAX	PIN	MEAS. CONDITION
2.9	2.9	2.8	2.8	2.9	2.8	2.8	2.8	2.4V		12	V_{OH} (V) I_{OH} = 2.0mA
2.9	2.8	2.8	2.8	2.9	2.8	2.8	2.8			11	
2.9	2.9	2.8	2.8	2.9	2.8	2.8	2.7			10	
3.0	2.9	2.8	2.8	2.9	2.8	2.8	2.7			9	
.40	.34	.30	.34	.30	.34	.32	.32		.45V	12	V_{OL} (V) I_{OL} = 15mA
.30	.34	.30	.34	.30	.32	.30	.32			11	
.30	.32	.30	.32	.30	.32	.30	.30			10	
.30	.32	.30	.32	.30	.32	.30	.30			9	
0	0	0	0	0	0	0	0		100µA	12	I_{OHE} (µA) V_{OH} = V_{CC}
0	0	0	0	0	0	0	0			11	
0	0	0	0	0	0	0	0			10	
0	0	0	0	0	0	0	0			9	
0	0	0	0	0	0	0	0		-100µA	12	I_{OLE} (µA) V_{OL} = 0.3V
0	0	0	0	0	0	0	0			11	
0	0	0	0	0	0	0	0			10	
0	0	0	0	0	0	0	0			9	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7		-1.5V	5	V_{CL} (V) I_{IN} = -10mA
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			6	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			7	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			4	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			3	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			2	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			1	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			15	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			13	
-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7			14	

TABLE 1-II (concl)

1	2	3	4	5	6	7	8	MIN	MAX	PIN	MEAS.	CONDITION
0	0	0	0	0	0	0	0		40µA	5	I_{RA} (µA)	"1"
0	0	0	0	0	0	0	0		40µA	6	I_{RA}	"1"
0	0	0	0	0	0	0	0		40µA	7	I_{RA}	"1"
0	0	0	0	0	0	0	0		40µA	4	I_{RA}	"1"
0	0	0	0	0	0	0	0		40µA	3	I_{RA}	"1"
0	0	0	0	0	0	2	0		40µA	2	I_{RA}	"1"
0	0	0	0	0	0	2	0		40µA	1	I_{RA}	"1"
0	0	0	0	0	0	2	0		40µA	15	I_{RA}	"1"
0	0	0	0	0	0	2	0		40µA	13	I_{RE} (µA)	"1"
0	0	0	0	0	0	2	0		40µA	14	I_{RE}	"1"
96µA	89	102	94	113	99	90	84		0.4mA	5	I_{FA} (µA)	"0"
95	89	99	88	109	99	83	82		0.4mA	6	I_{FA}	"0"
86	79	92	82	102	91	78	73		0.4mA	7	I_{FA}	"0"
94	79	92	80	105	95	79	75		0.4mA	4	I_{FA}	"0"
92	75	82	79	99	97	77	74		0.4mA	3	I_{FA}	"0"
93	83	89	79	103	94	77	72		0.4mA	2	I_{FA}	"0"
91	75	87	80	99	93	76	71		0.4mA	1	I_{FA}	"0"
85	76	88	80	99	94	76	72		0.4mA	15	I_{FA}	"0"
58	42	60	58	64	66	52	48		0.4mA	13	I_{FE} (µA)	"0"
54	51	56	60	65	58	47	45		0.4mA	14	I_{FE}	"0"
87	80	85	85	81	77	81	80		130mA	16	I_{CC} (µA)	

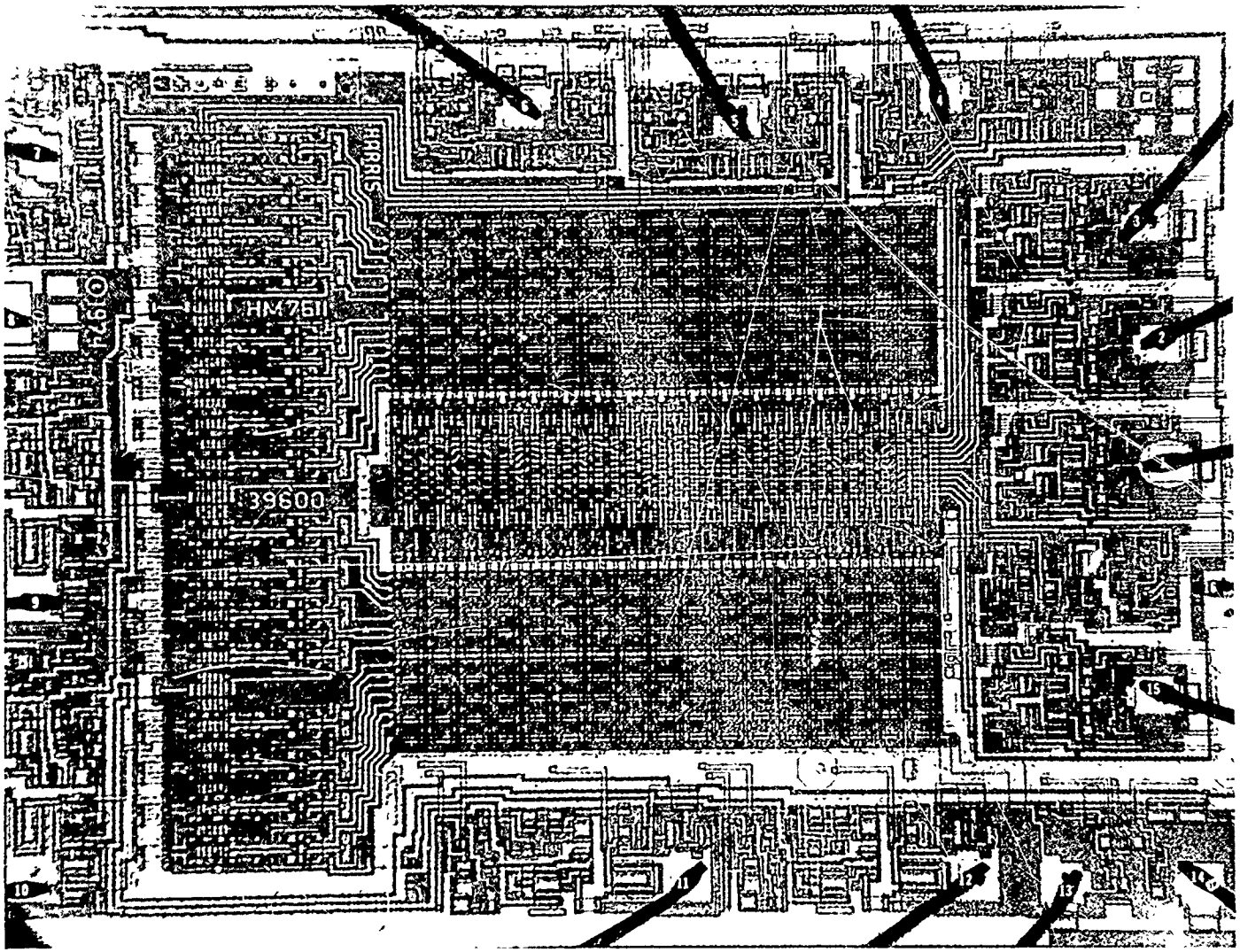


Photo 1-1 The Complete Die and Circuit Pin Identification. Mag. - 40X

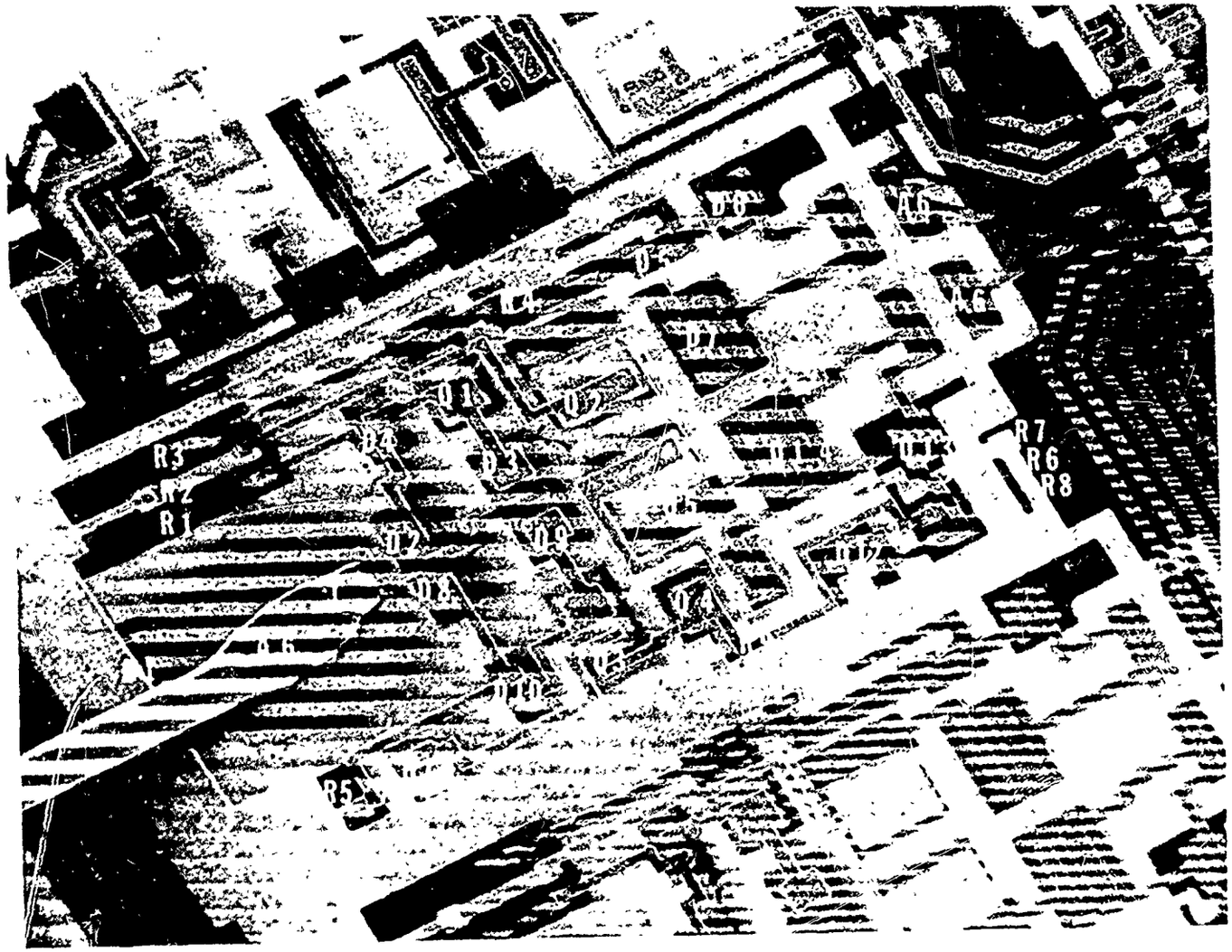


Photo 1-2 Voltage Contrast Micrograph of the A6 Row Address Buffer. Input A6 is Cycling at 0.7 Hz. Note in Upper Right Corner - All Row Address Lines are Operating at Different Frequencies. 5 KV, Mag. - 275X

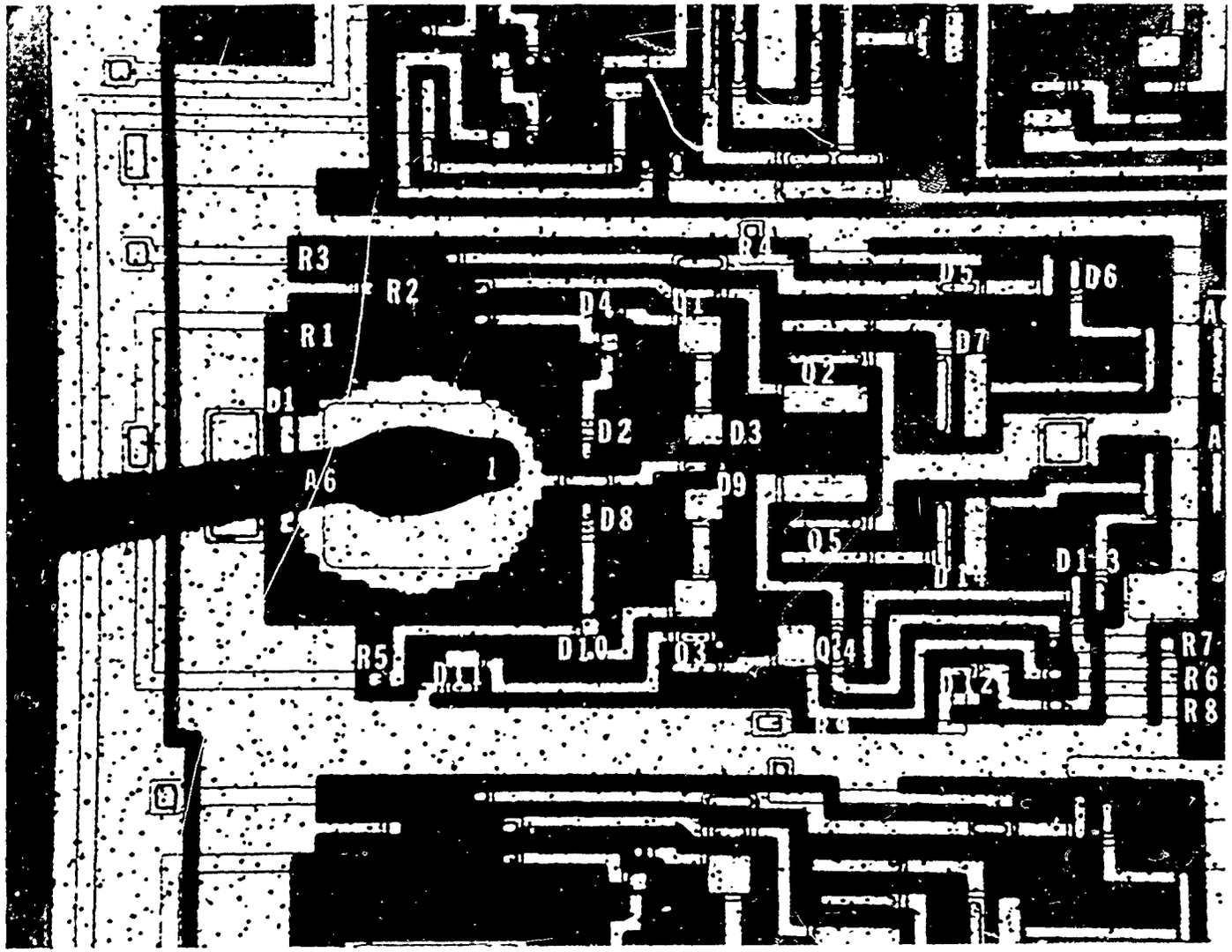


Photo 1-3 Light Photograph of the A6 Row Address Buffer. Mag. - 225X

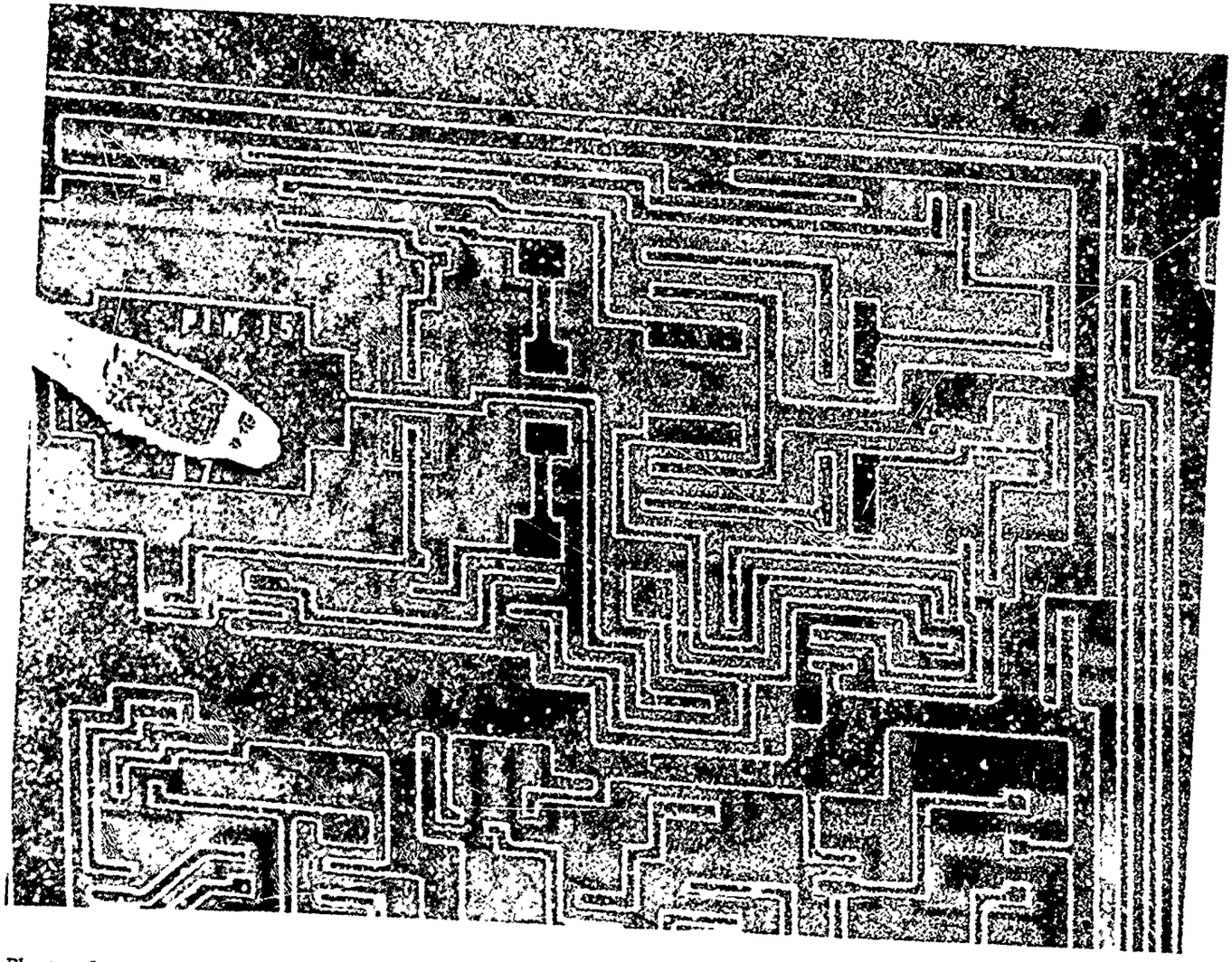


Photo 1-4 Secondary Electron Image (SEI) of A6 Row Address Buffer. This Photo Provides a Reference for the Following EBIC Photo. Mag. - 325X

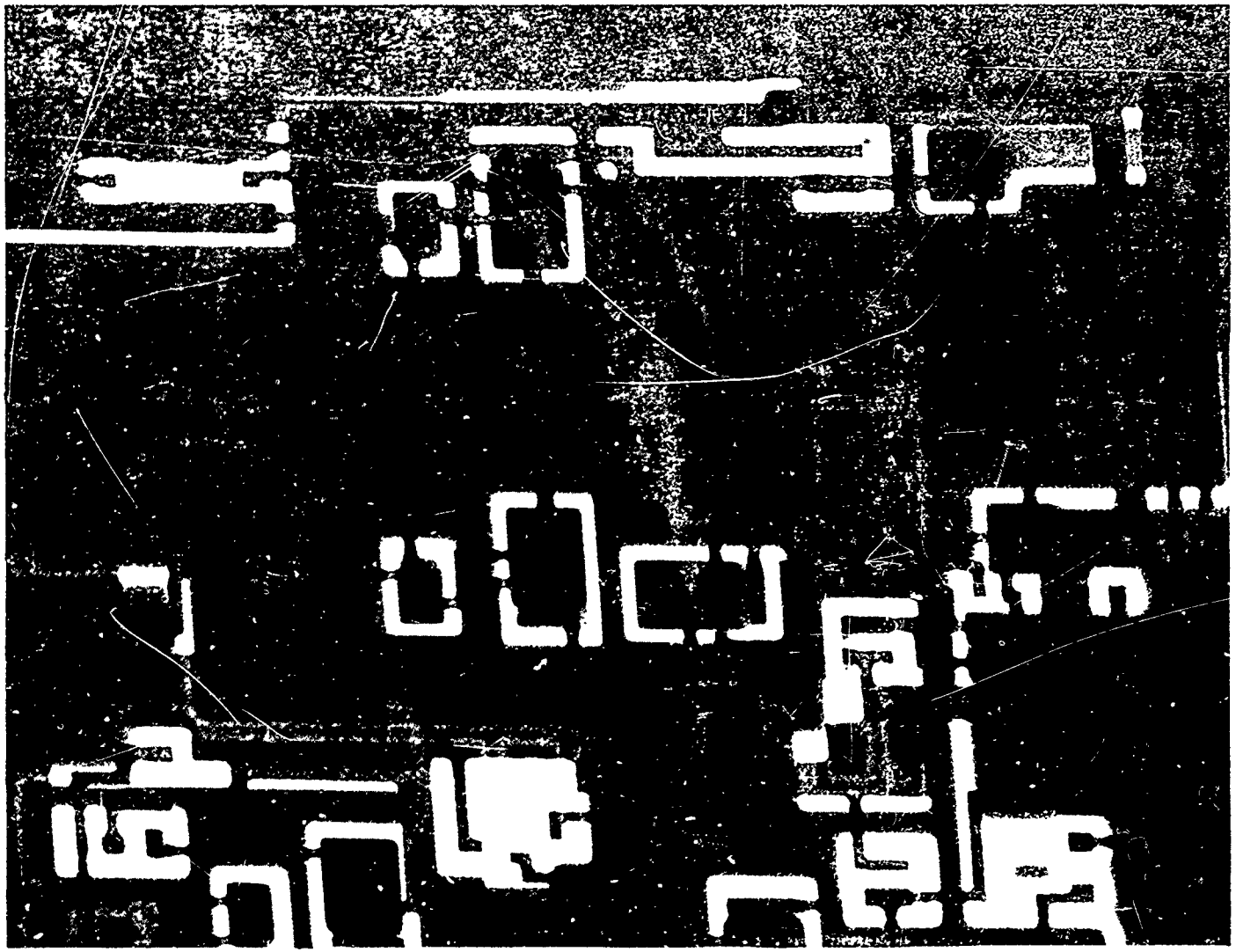


Photo 1-5 Electron Beam Induced Current (EBIC) Image of A6 Row Address Buffer. Pin 16 SCA, Pin 8 Gnd. 15 KV, Mag. - 325X

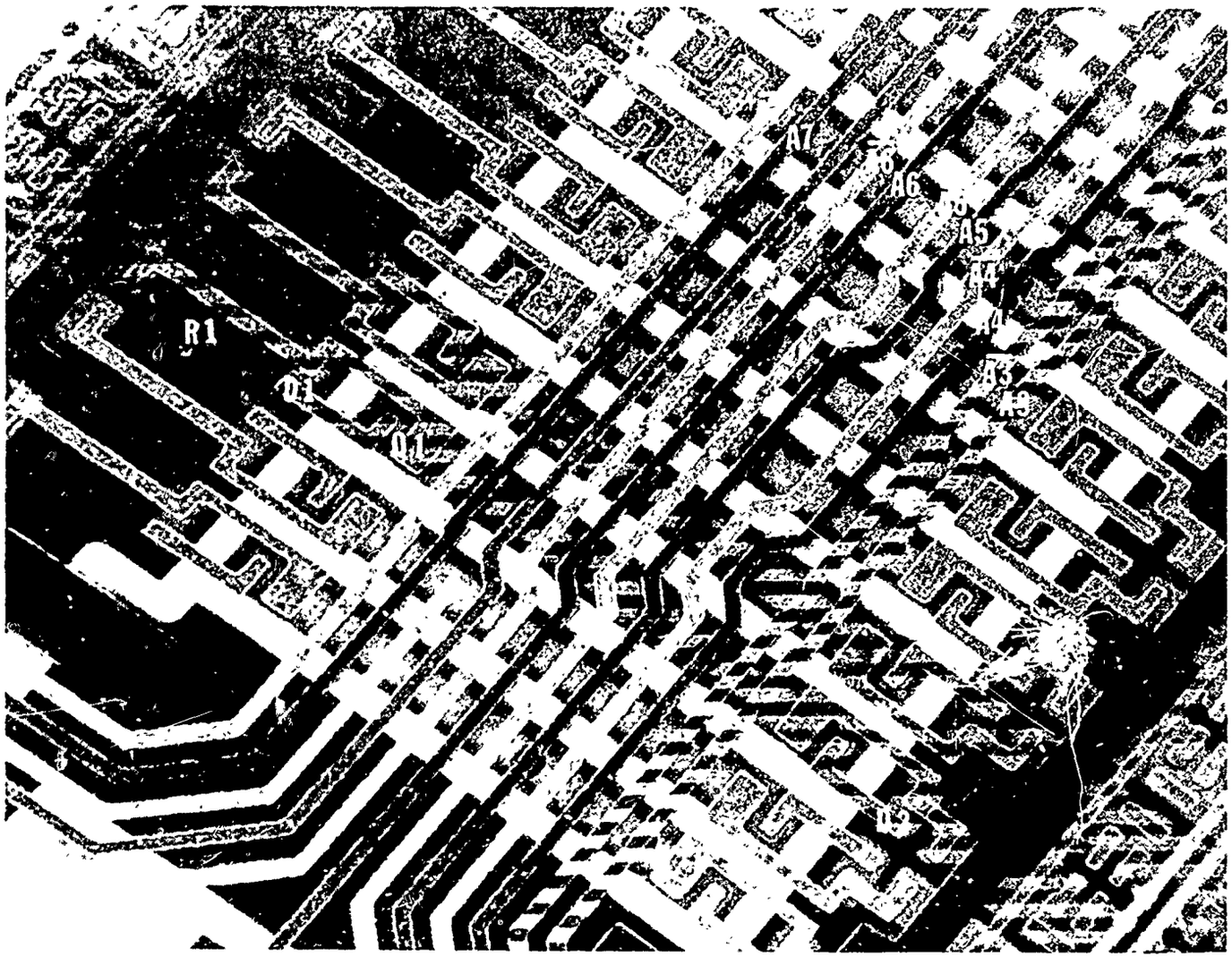


Photo 1-6 Voltage Contrast Micrograph of Row Decode Circuits. The Row Address Busses are Identified and Address A3 is Cycling at 0.7 Hz. 5 KV, Mag. - 385X

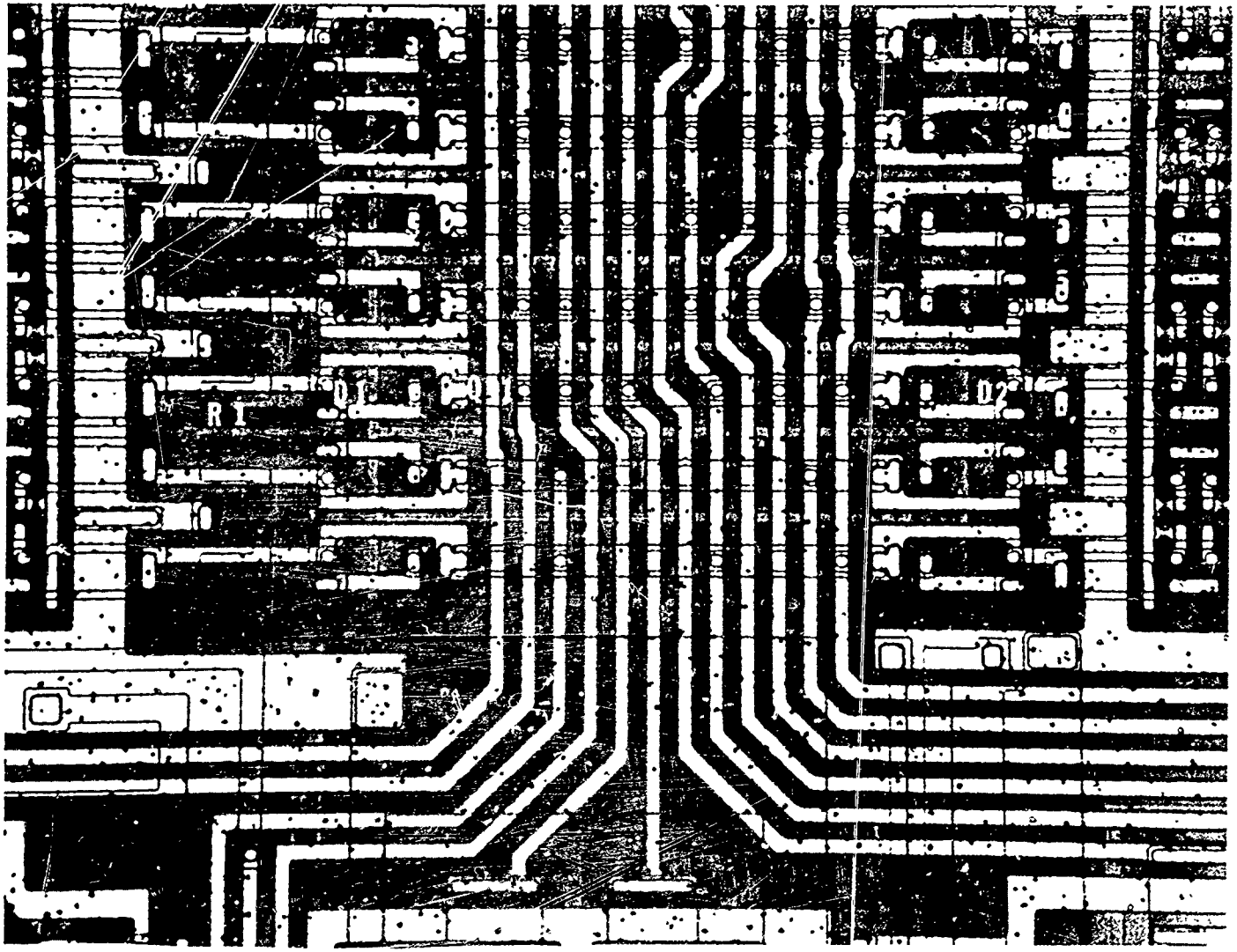


Photo 1-7 Light Photograph of Row Decode Circuits. Mag. - 300X

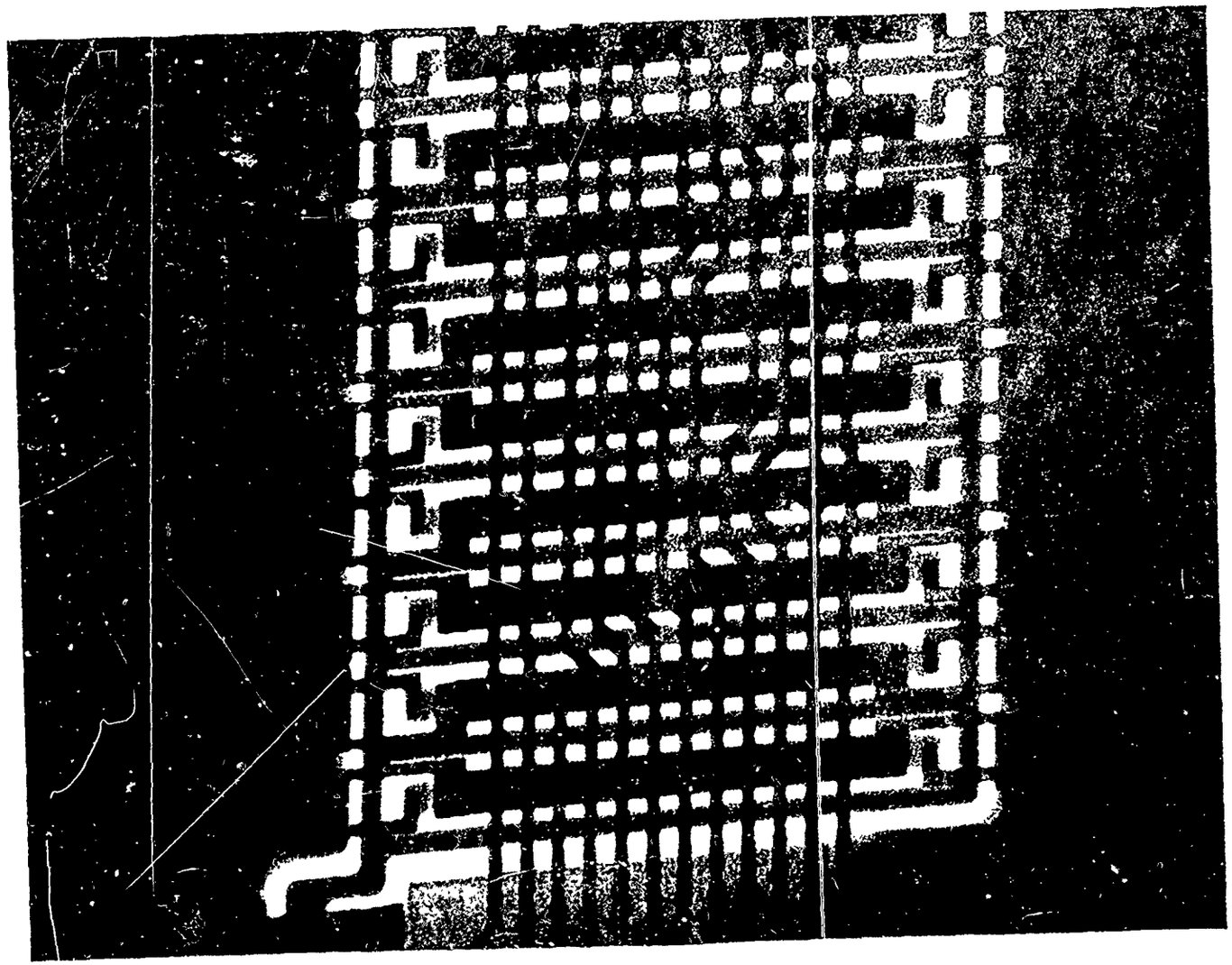


Photo 1-8 EBIC Image for Row Decode Circuits. 15 KV, Mag. - 350X

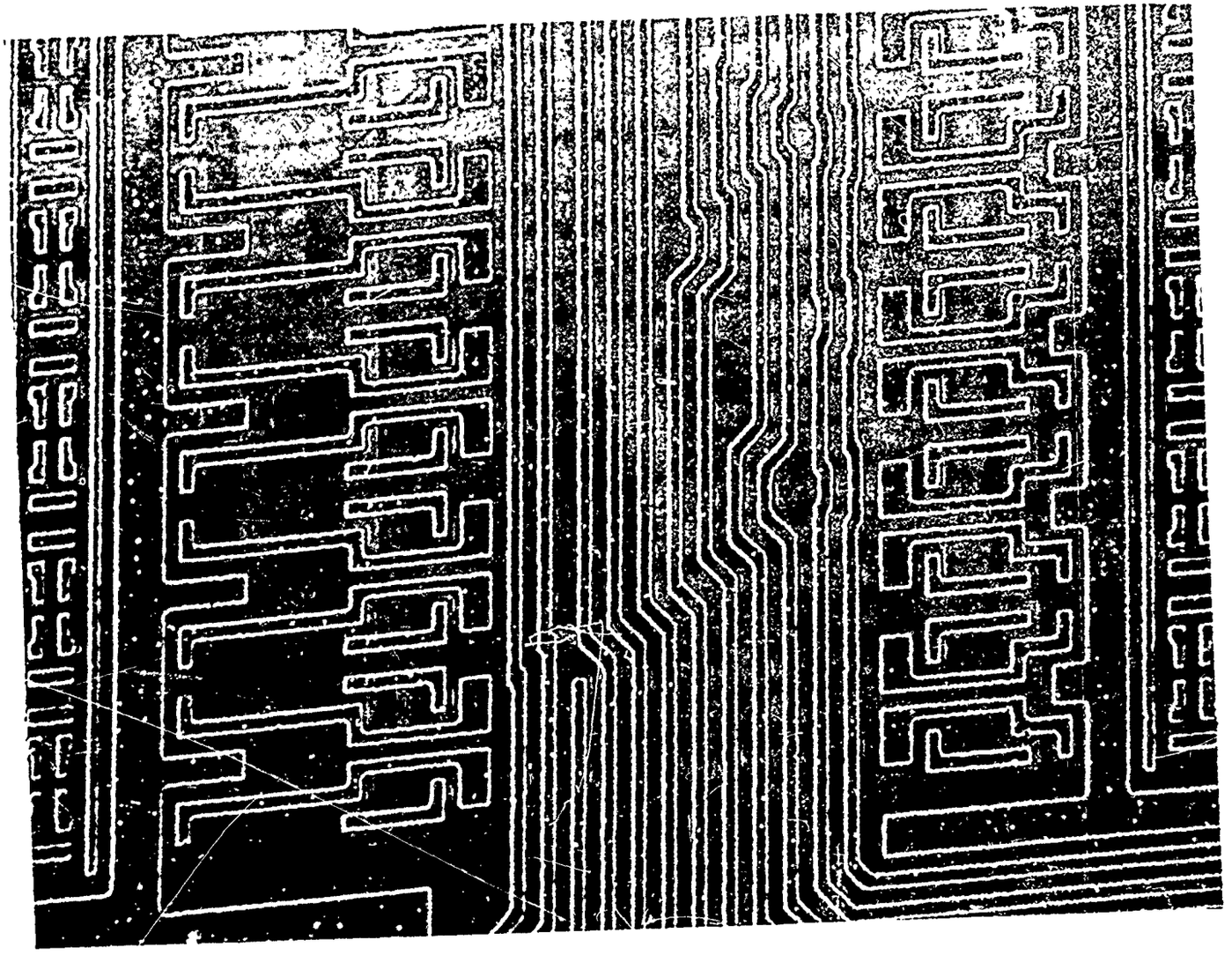


Photo 1-9 SEI of Row Decode Circuit; Same Area as Photo 1-8. Mag. - 350X

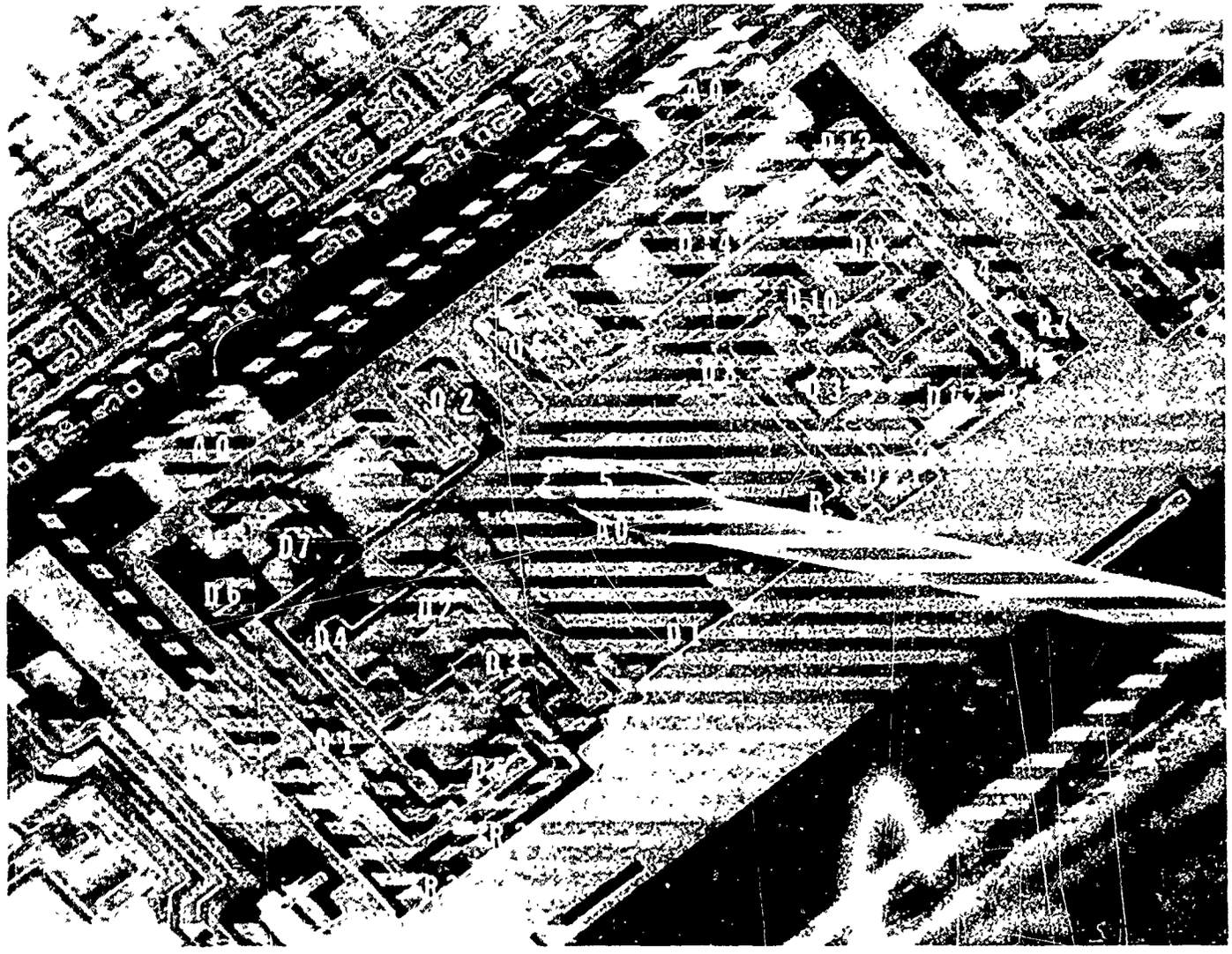


Photo 1-10 Voltage Contrast Micrograph of A0 Column Address Buffer Cycling at 9.7 Hz, 5 KV, Mag - 275X

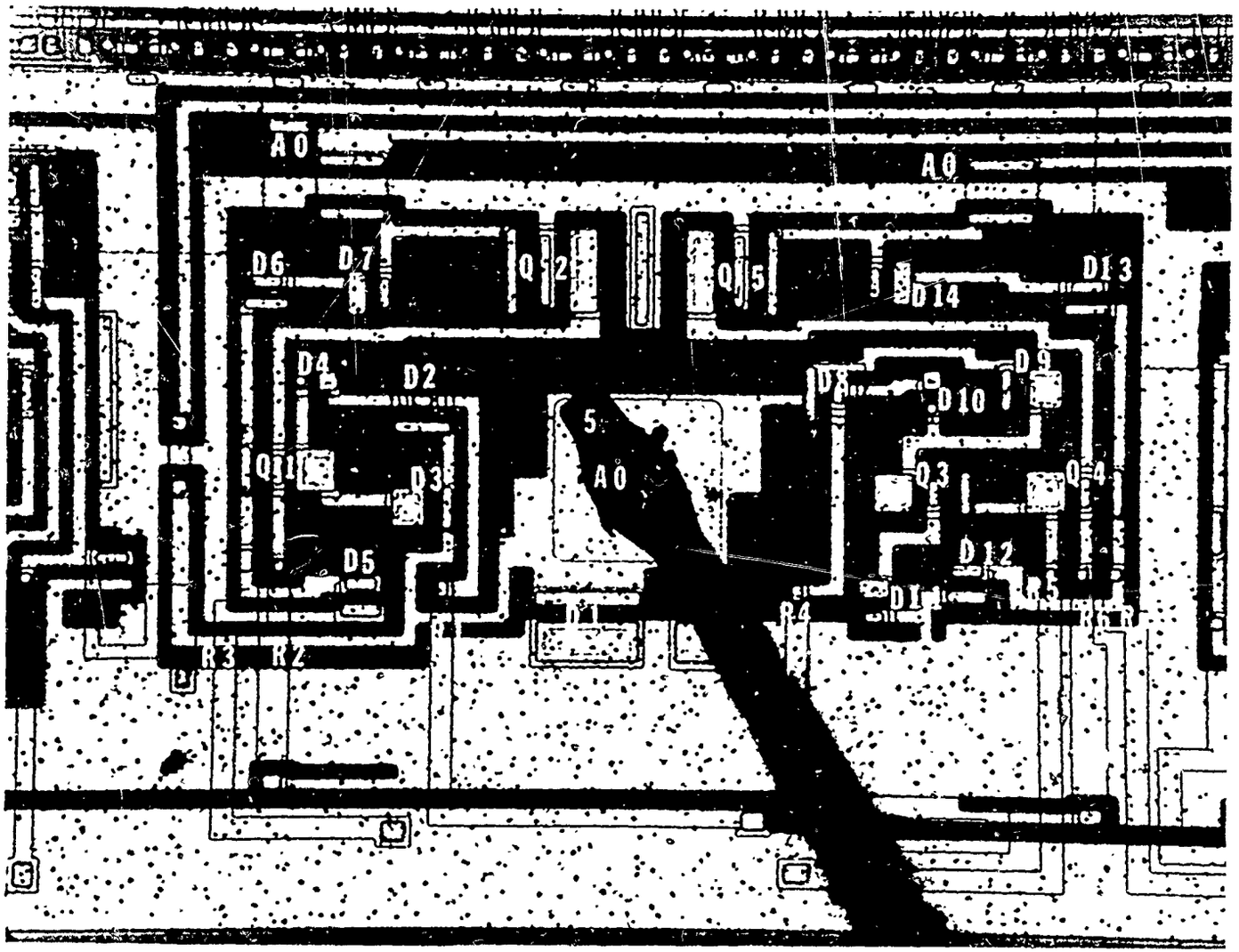


Photo 1-11 Light Photograph of A0 Column Address Buffer. Mag. - 225X

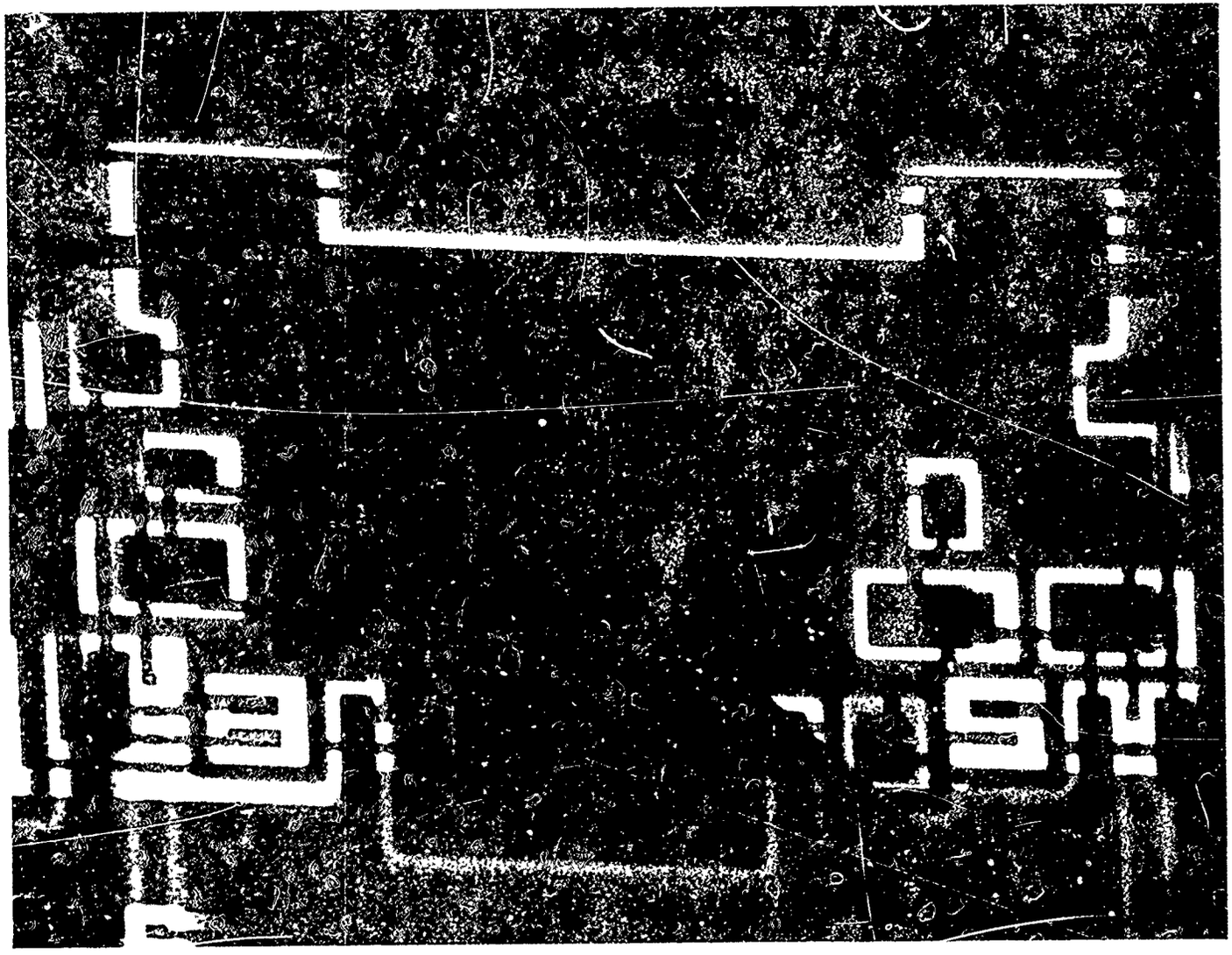


Photo 1-12 EBIC Image of A0 Column Address Buffer. 15 KV, Mag. - 325X

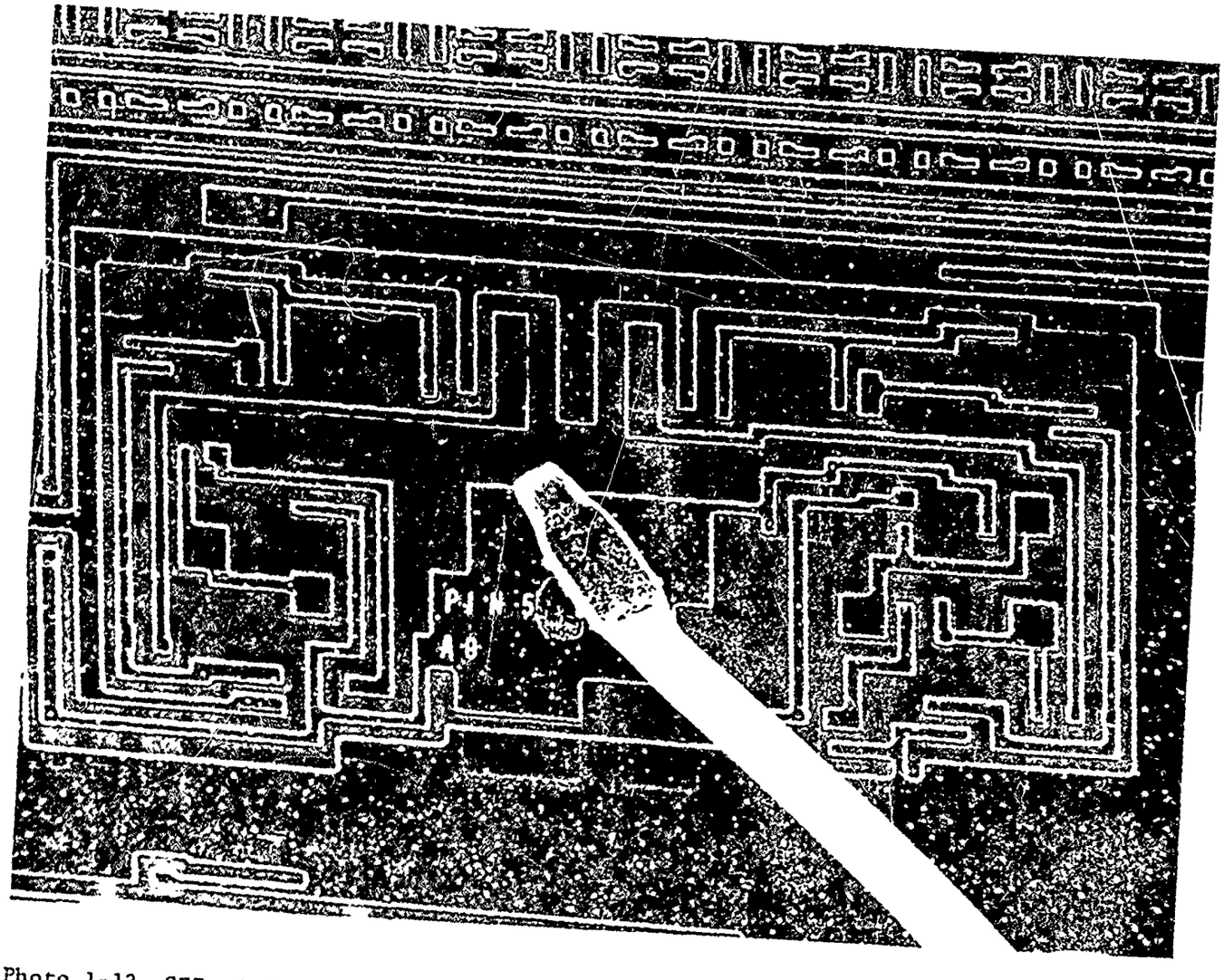


Photo 1-13 SEI of A0 Column Address Buffer; Same Area as Photo 1-12. Mag. - 325X

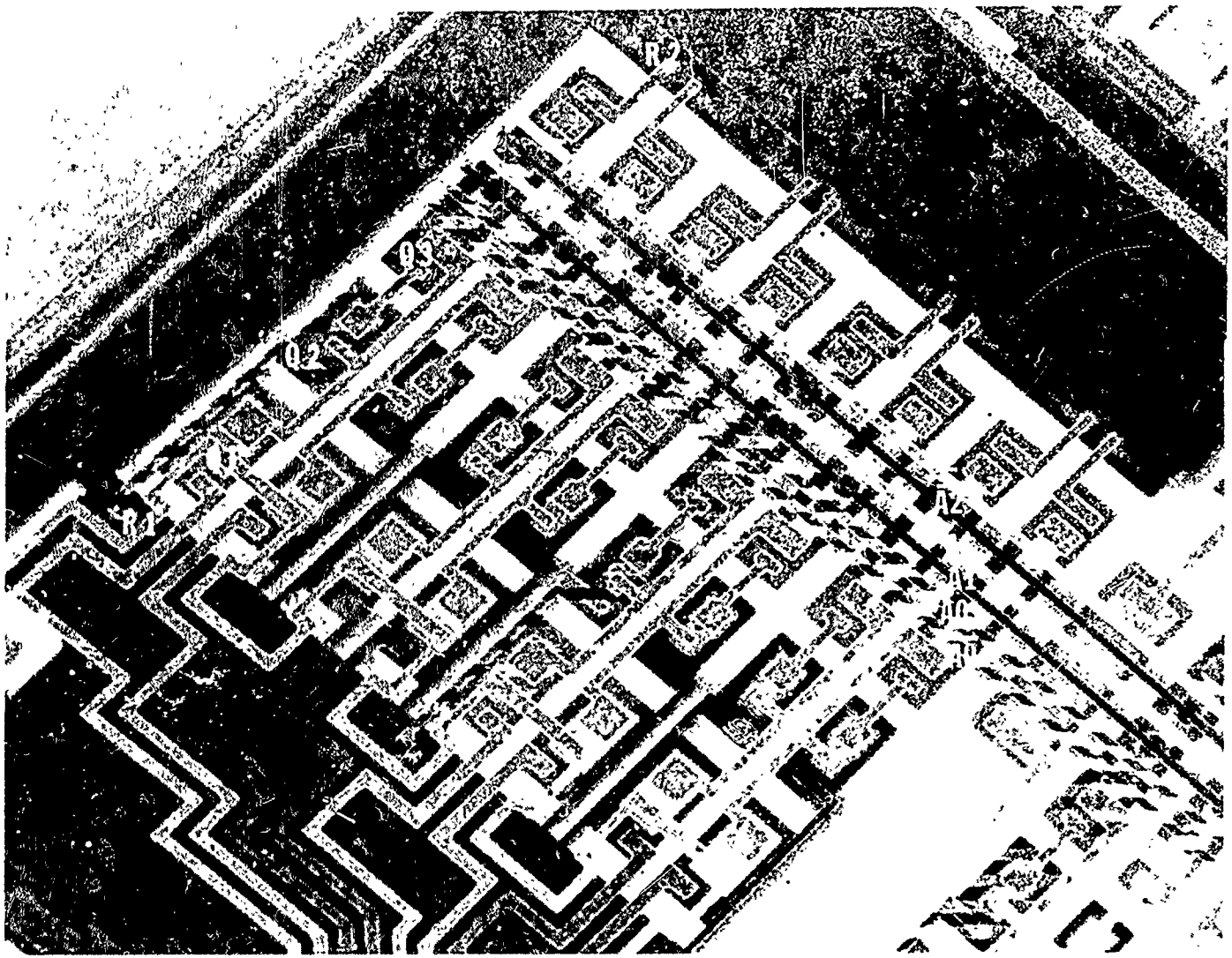


Photo 1-14 Voltage Contrast Micrograph of Column Decode Circuit; Note That Two Columns Are Alternately Being Selected. 15 KV, Mag. - 300X

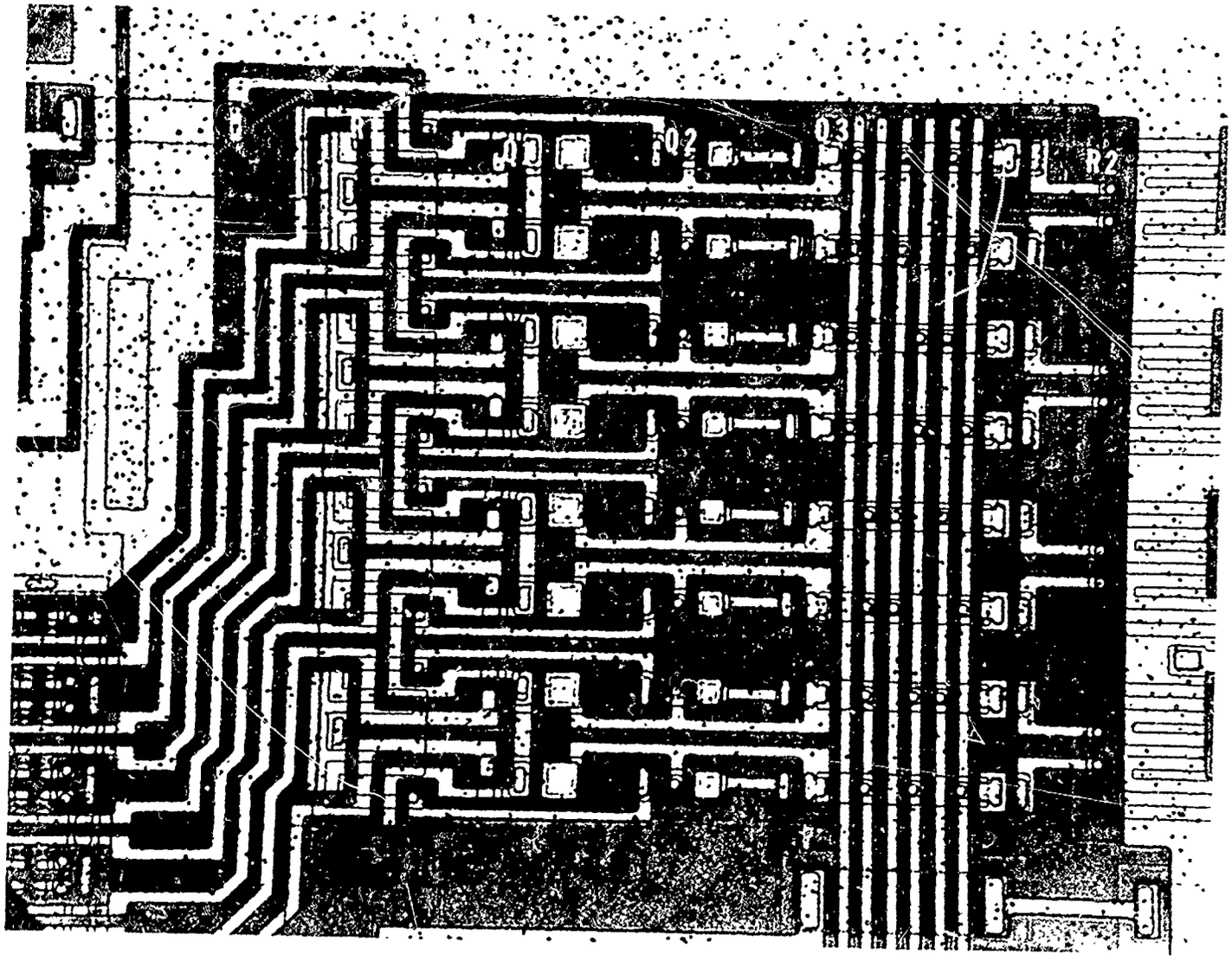


Photo 1-15 Light Photograph of Column Decode Circuit. Mag. - 225X

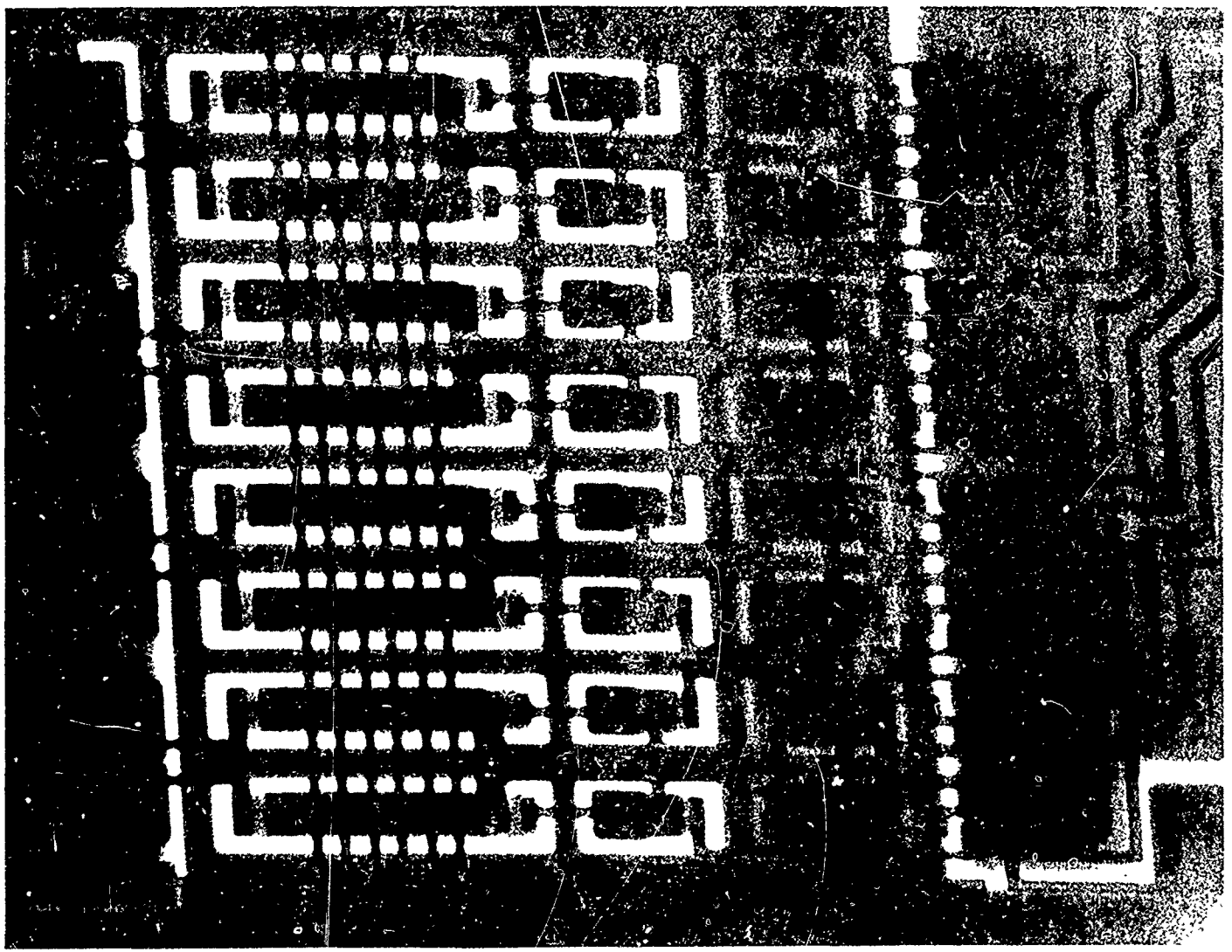


Photo 1-16 EBIC Image of Column Decode; Dark Black Areas are Emitter Diffusions. 15 KV, Mag. - 325X

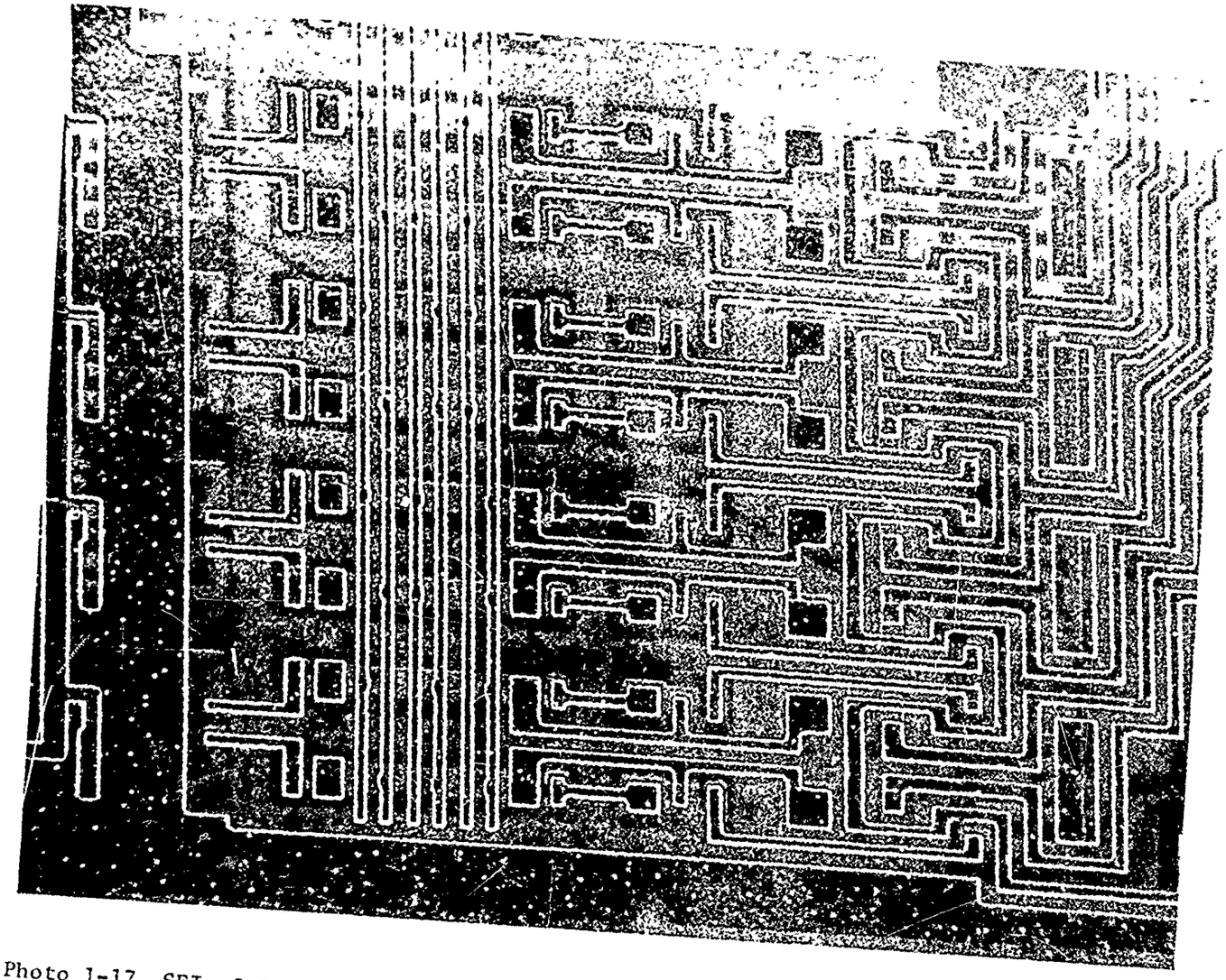


Photo I-17 SEI of Column Decode Circuit; Same Area as Photo I-1 . Mag. ~ 525X

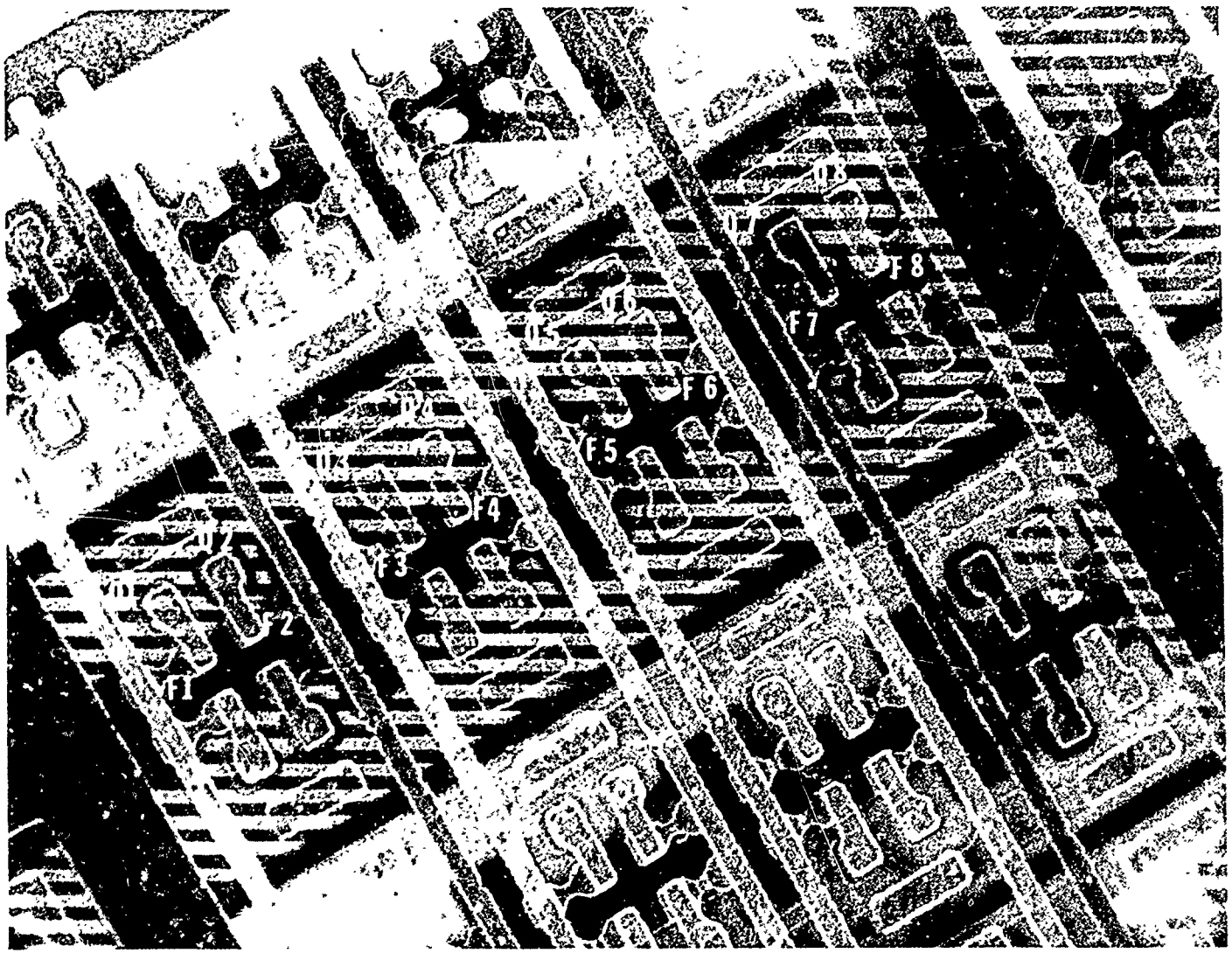


Photo 1-18 Voltage Contrast Micrograph of Memory Cells Showing Transistors and Nichrome Fuses. 5 KV, Mag. - 775X

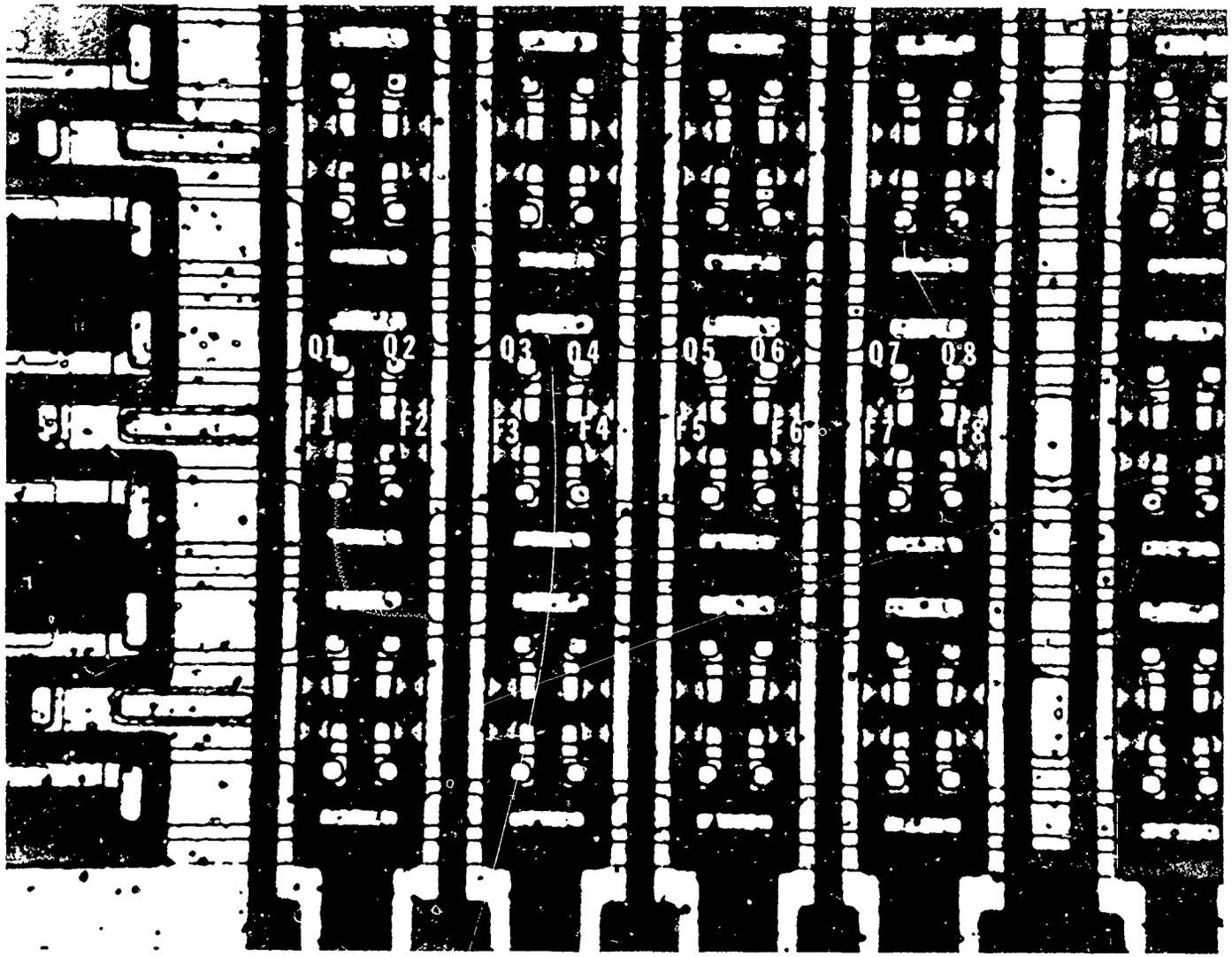


Photo 1-19 Light Photograph of Memory Cells. Mag. - 450X

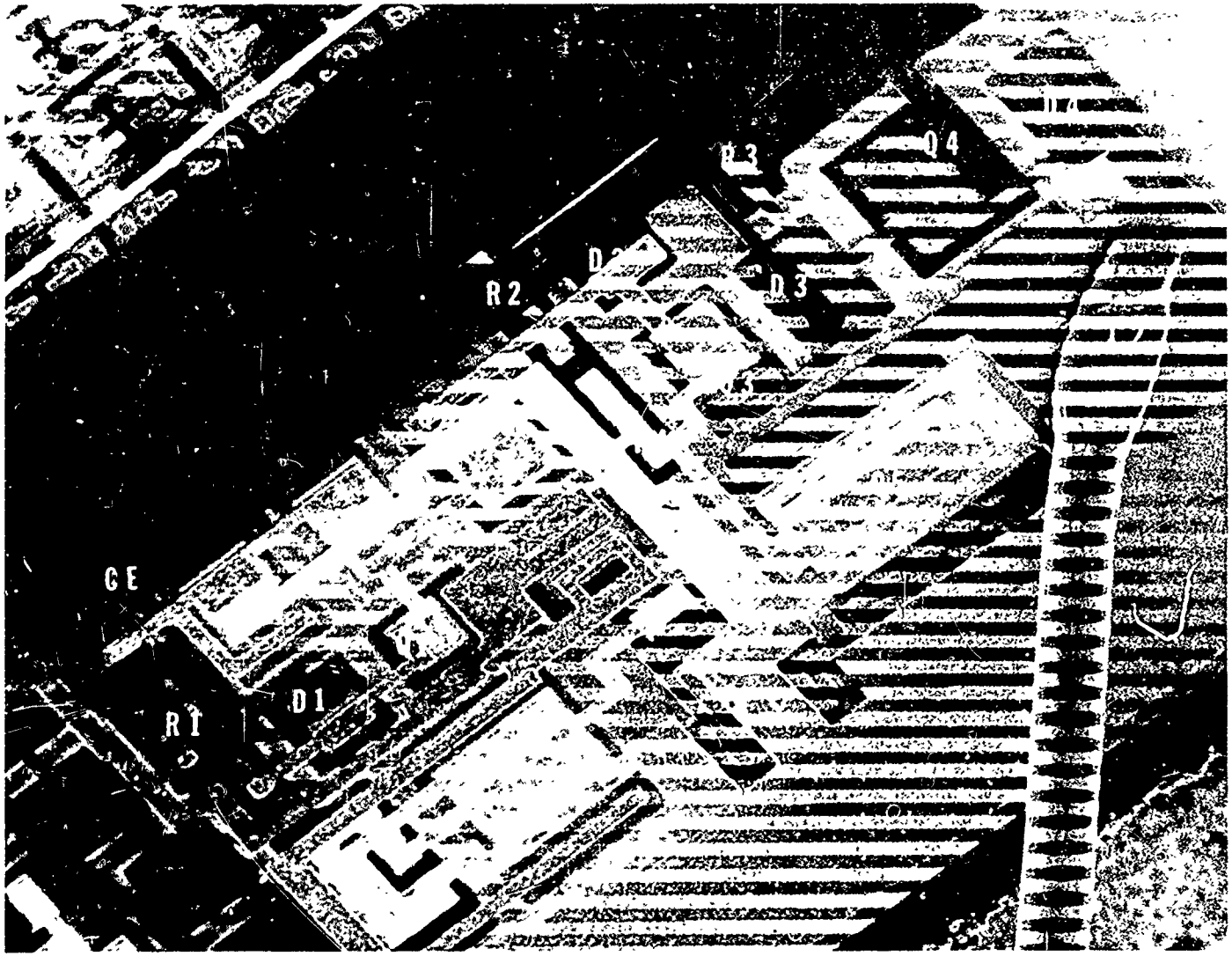


Photo 1-20 Voltage Contrast Micrograph of Output Section. Output Pin is Switching Between a High and a Low State. 5 KV, Mag. - 325X

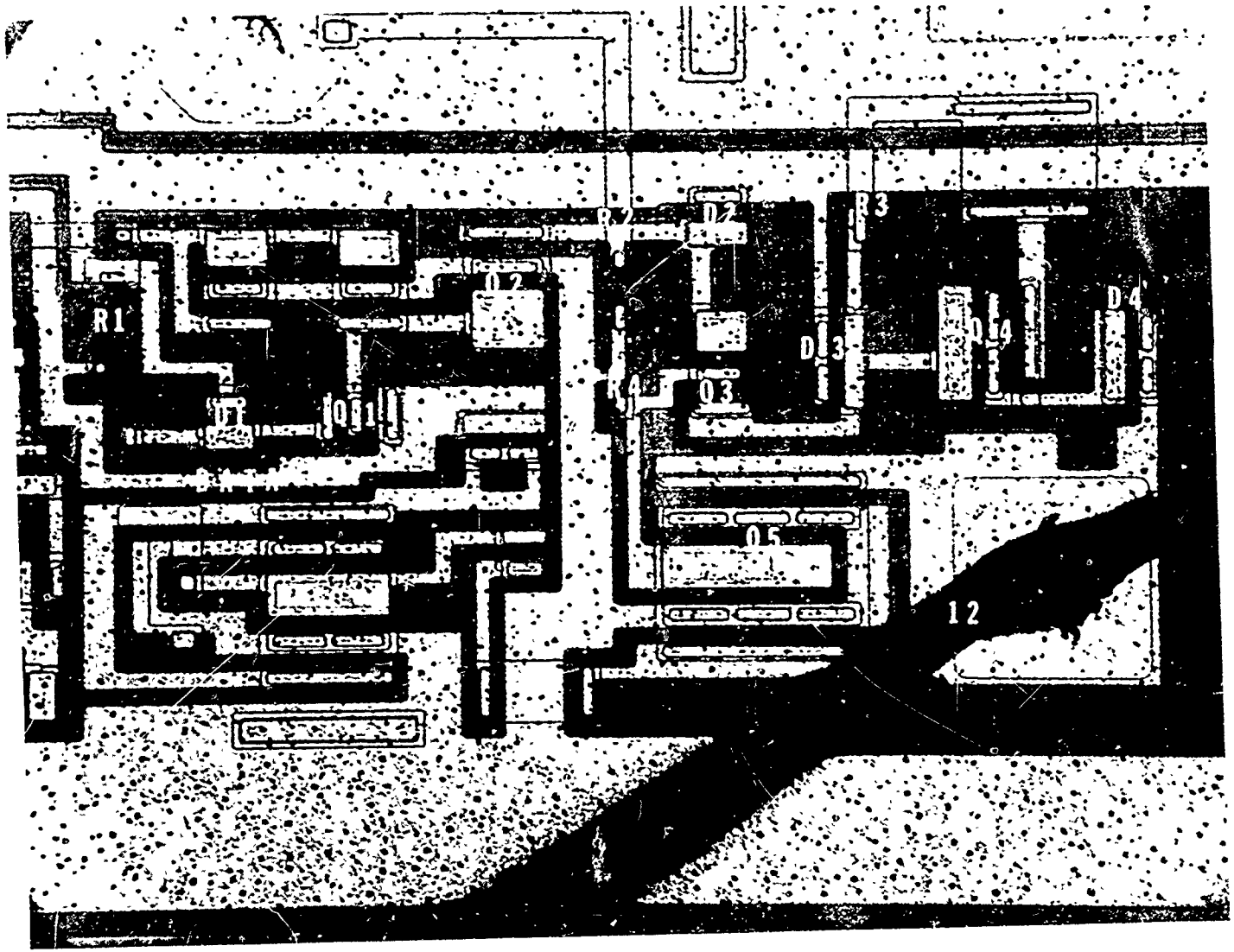


Photo 1-21 Light Photograph of Output Section. Mag. - 175X

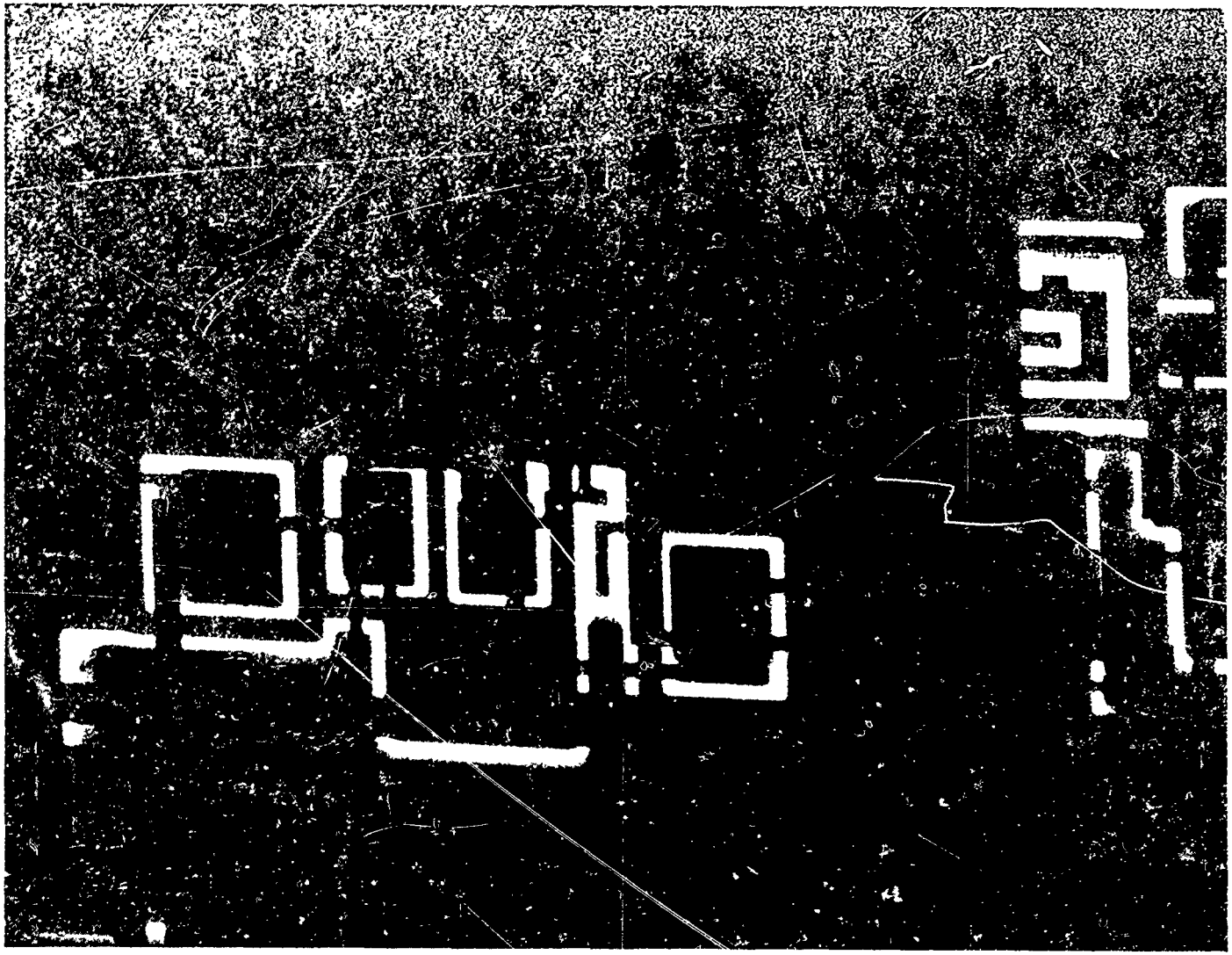


Photo 1-22 EBIC Image of Output Circuitry. 15 KV, Mag. - 325X

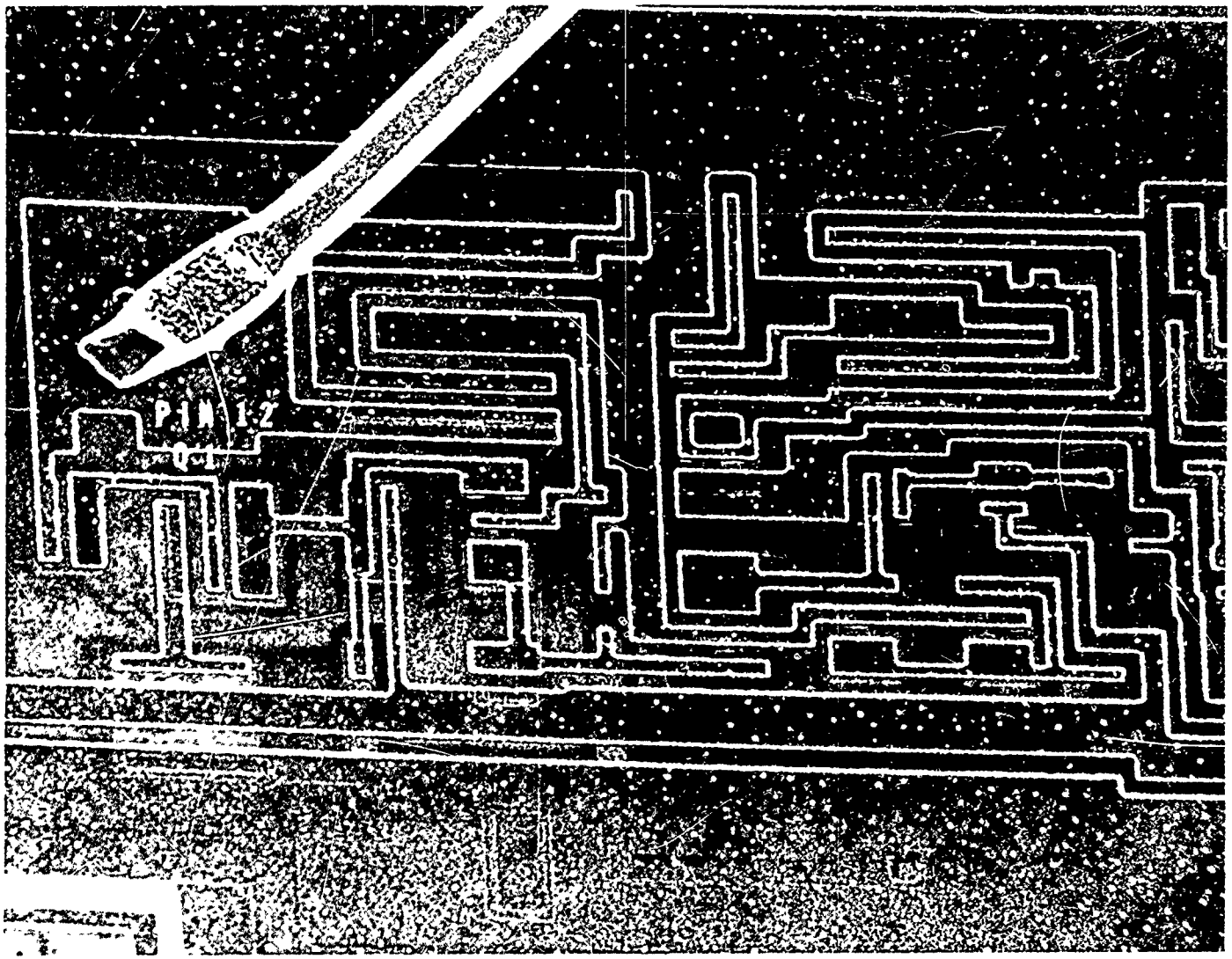


Photo 1-23 SEI of Output Q_1, Pin 12; Same Area as Photo 1-22. Mag. - 325X

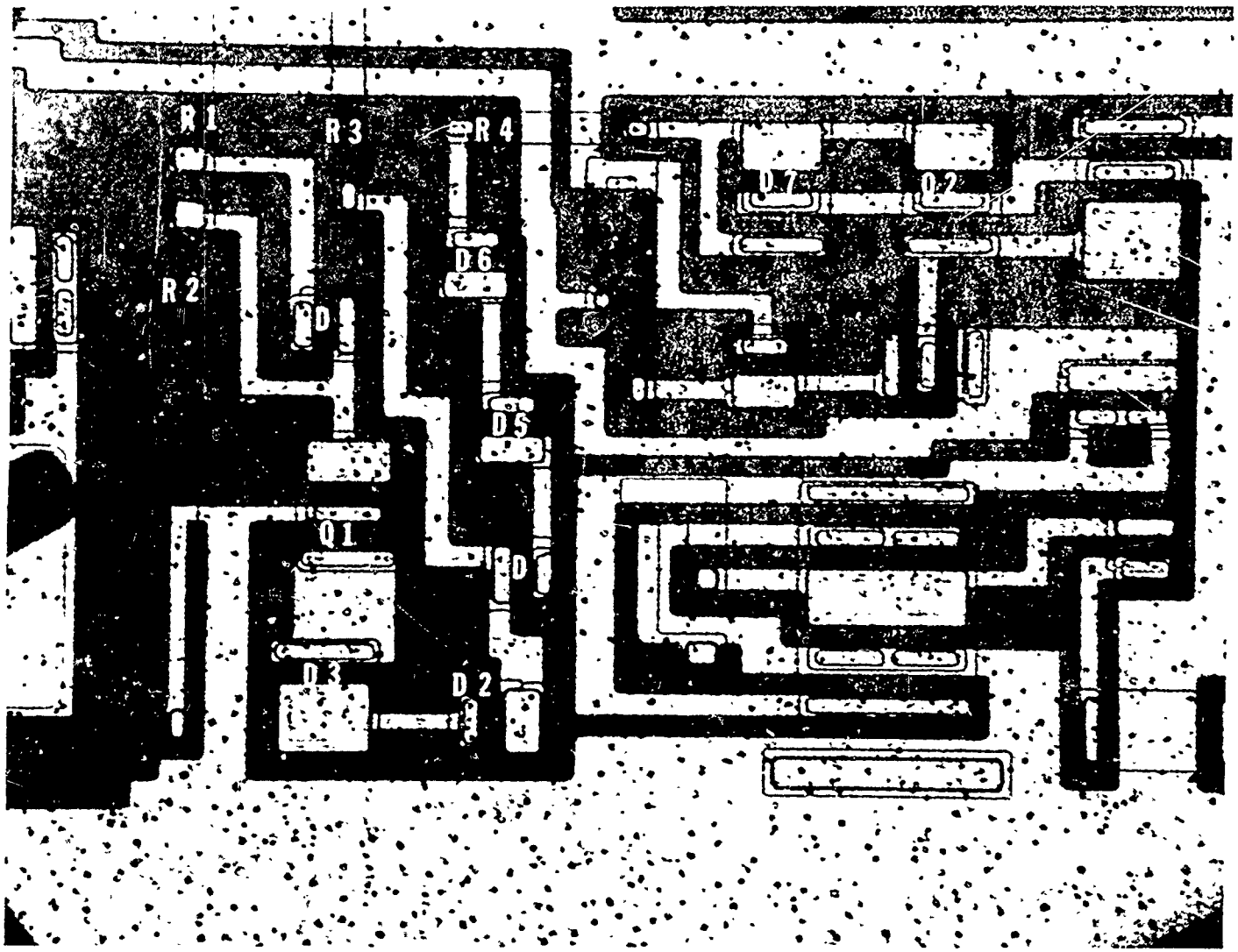


Photo 1-24 Light Photograph of Sense Amplifier Current Sink Circuitry. Mag. - 325X

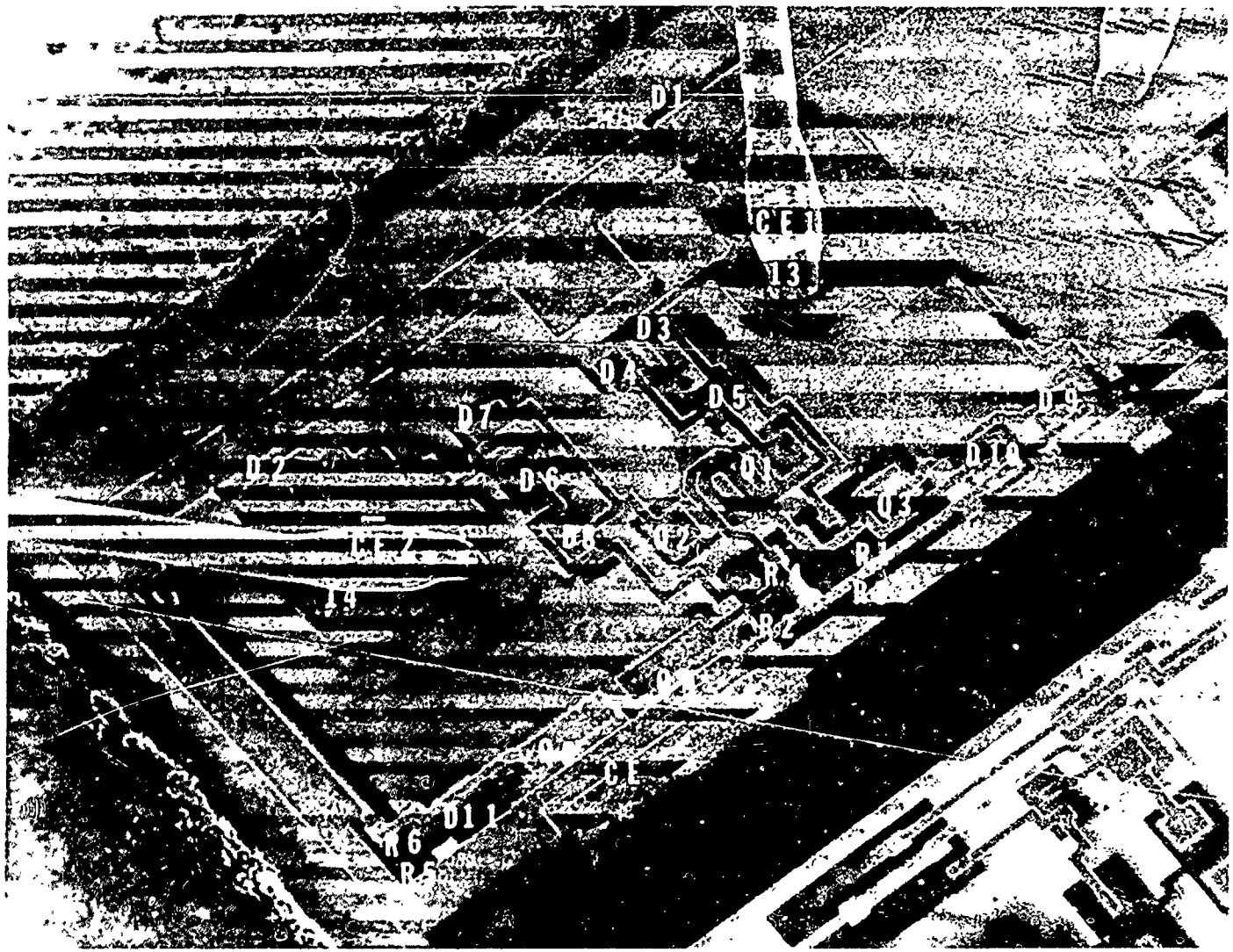


Photo 1-25 Voltage Contrast Micrograph of Chip Enable. CE2 on the Left is Cycling at 0.7 Hz and CE1 is Cycling at 0.3 Hz. 5 KV, Mag. - 250X

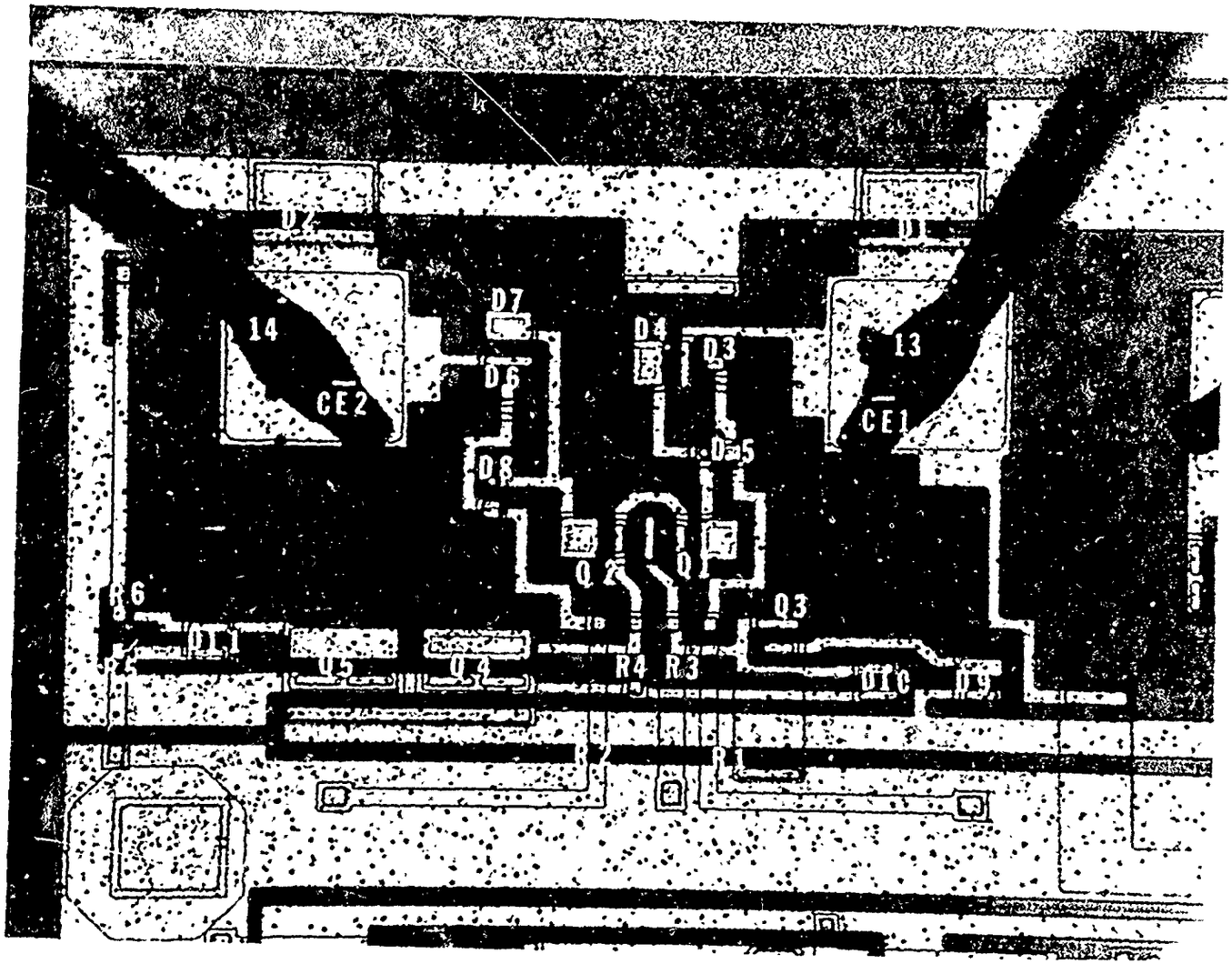


Photo 1-26 Light Photograph of Chip Enable Circuitry. Mag. - 225X

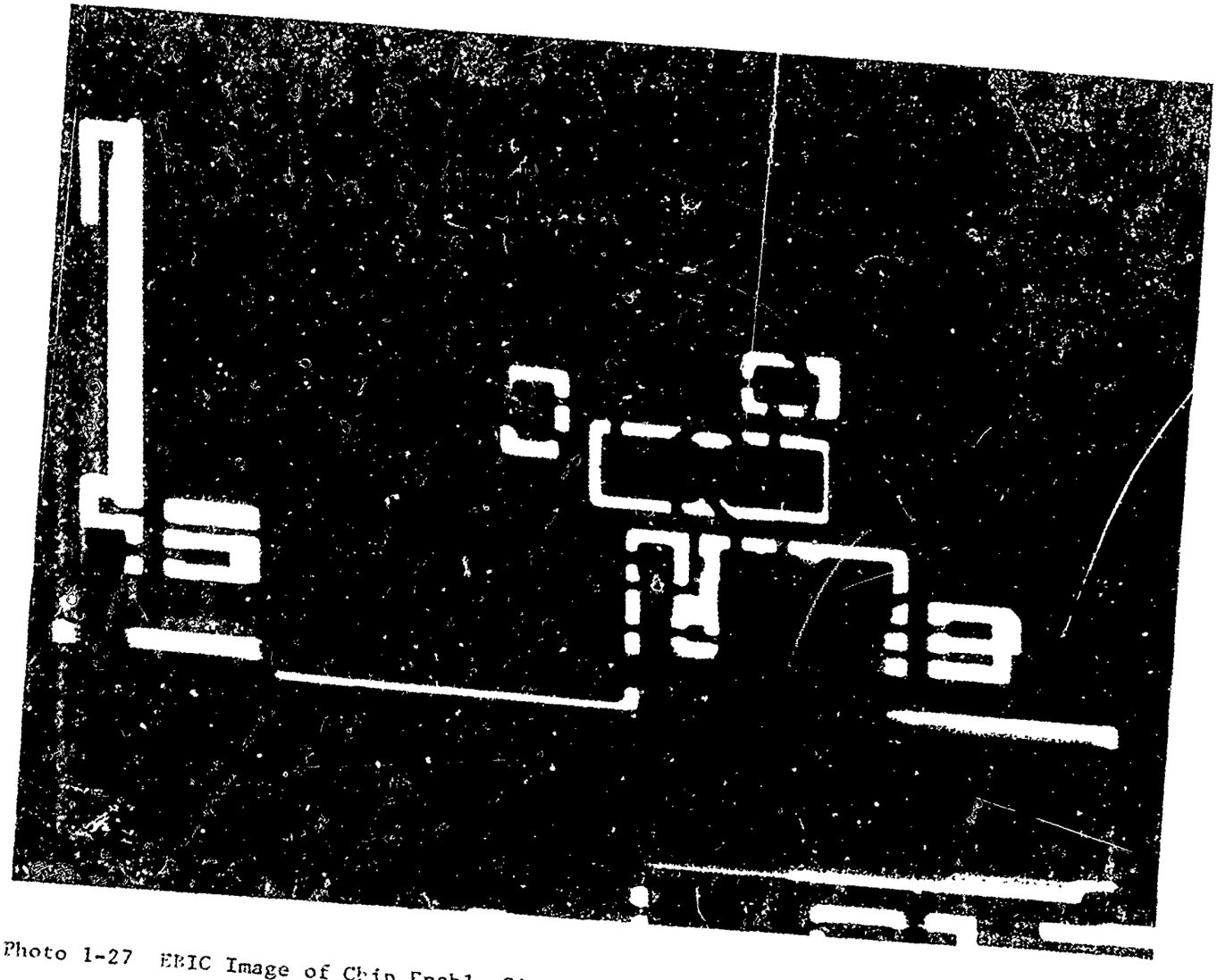


Photo 1-27 EBIC Image of Chip Enable Circuitry. Mag. - 325X

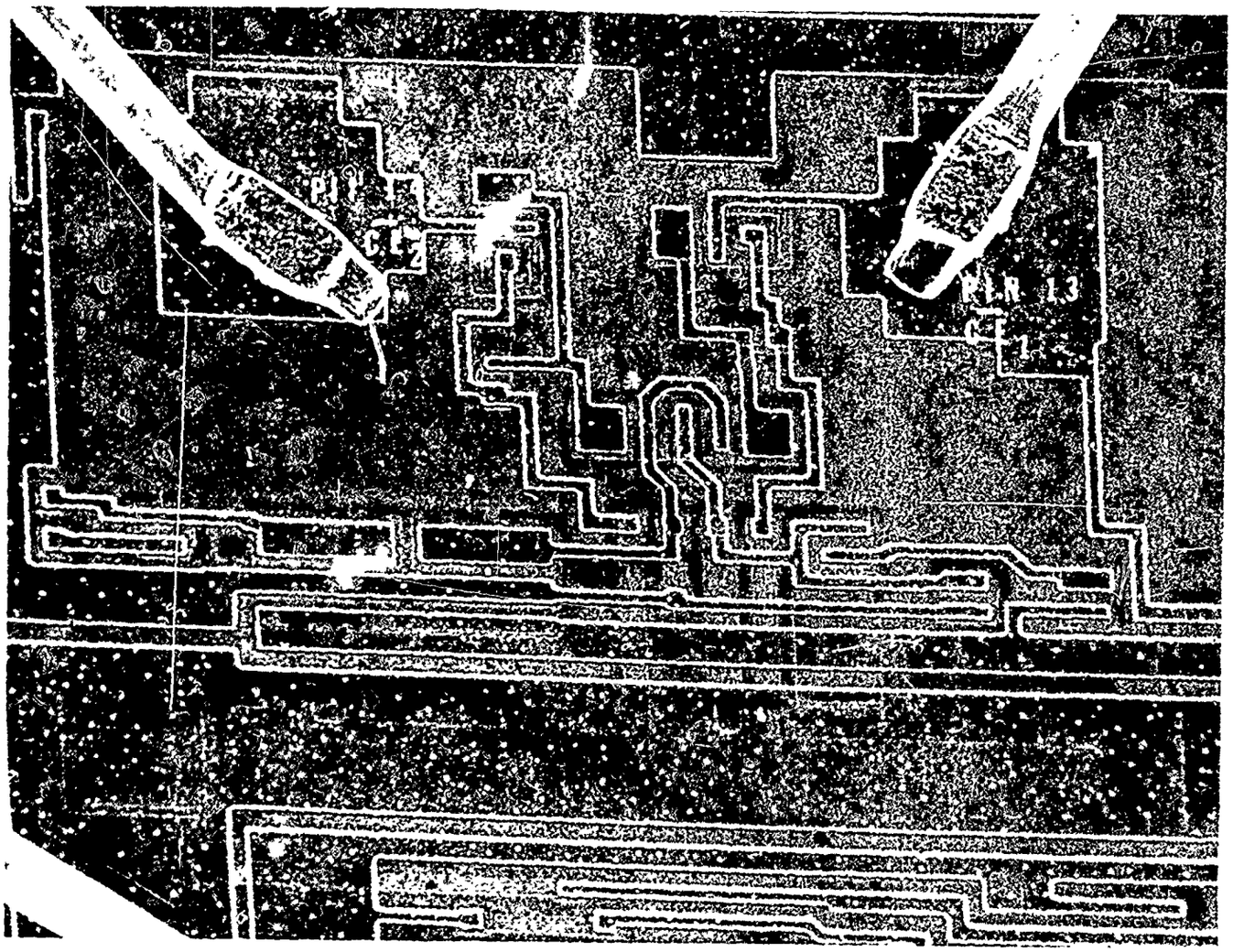


Photo 1-28 SEI of Chip Enable Circuitry Shown in Photo 1-27. Mag. - 325X

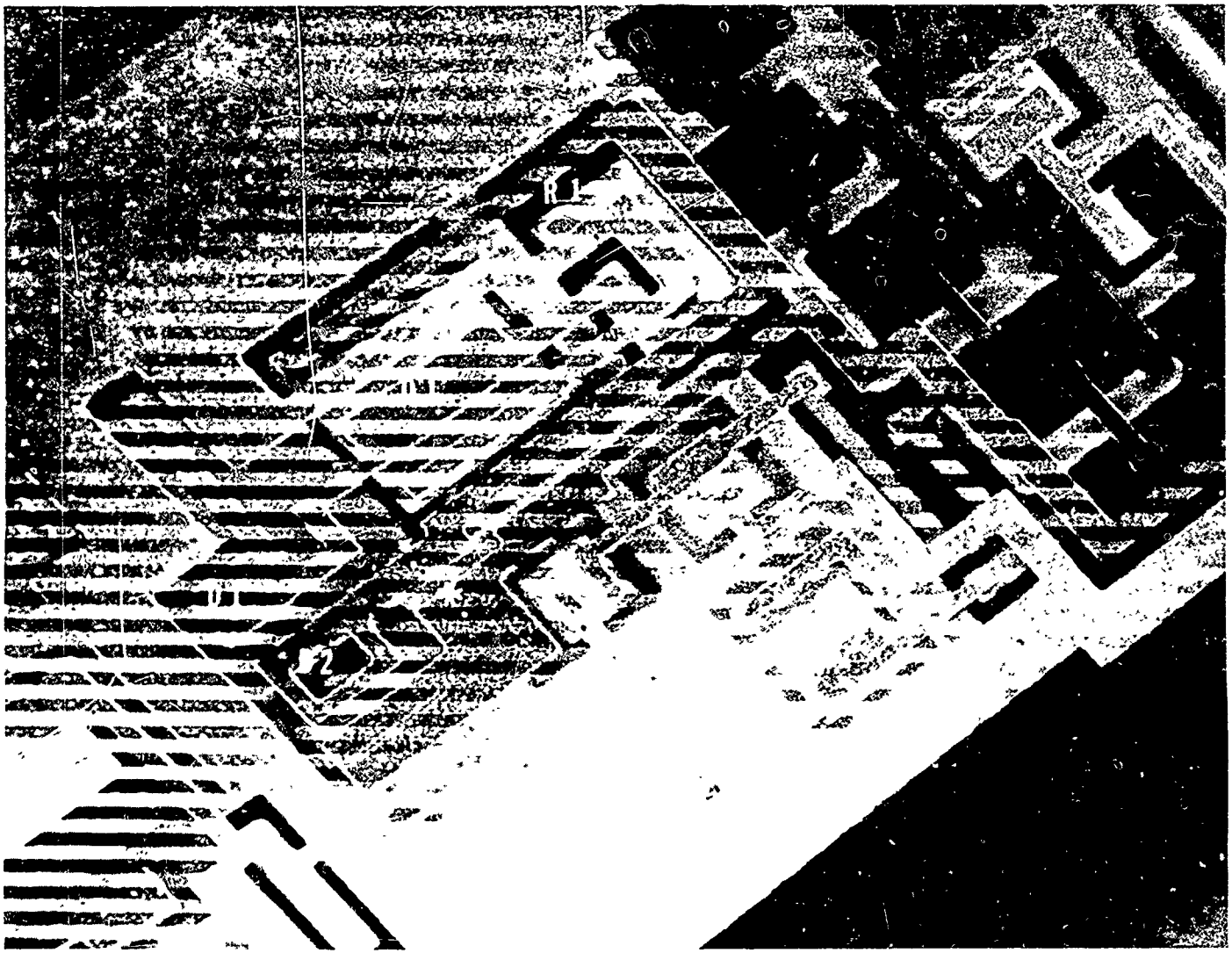


Photo 1-29 Voltage Contrast Micrograph of Program Circuitry (1 Per Output). 5 KV, Mag. - 450X

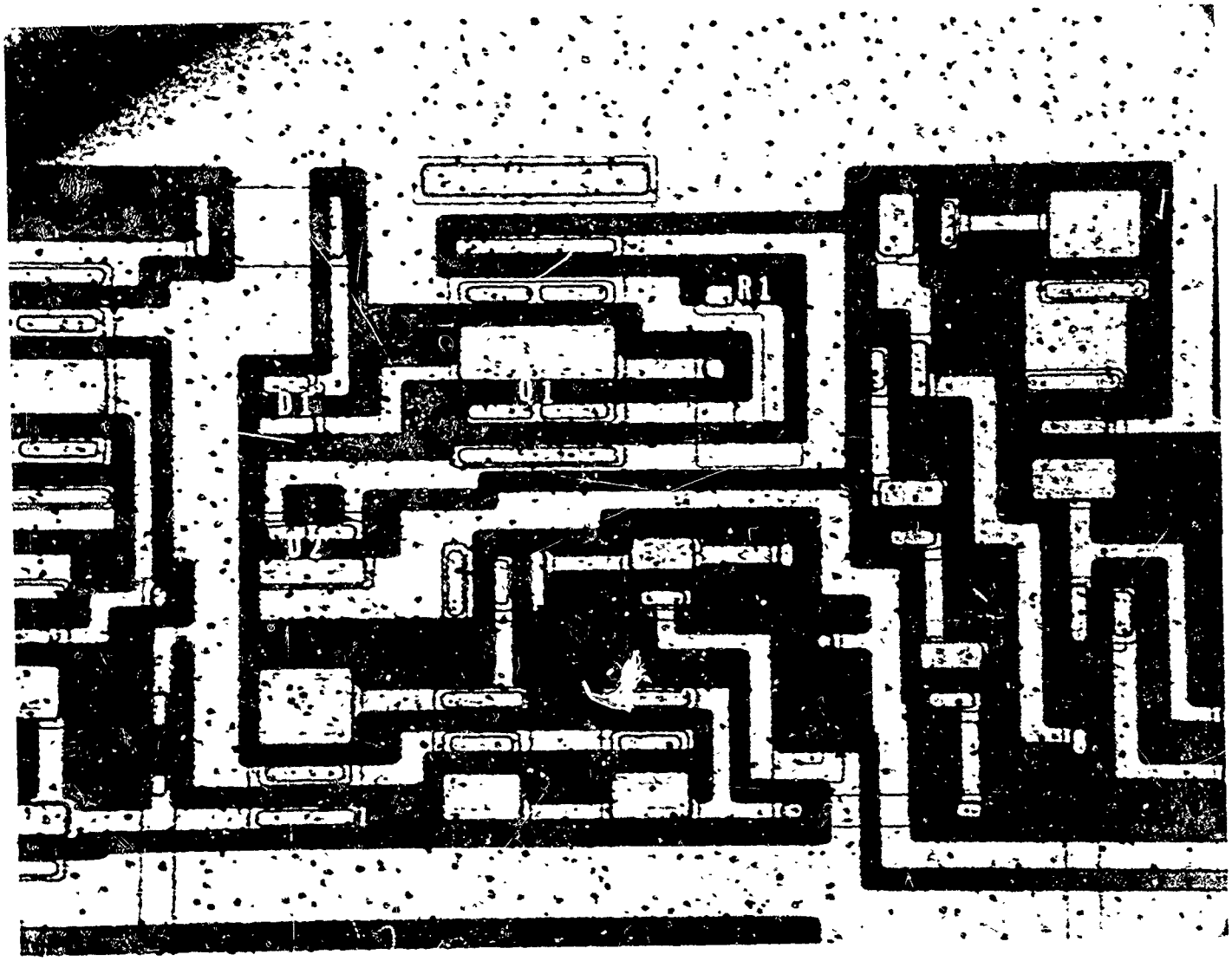


Photo 1-30 Light Photograph of Program Circuitry. Mag. - 350X

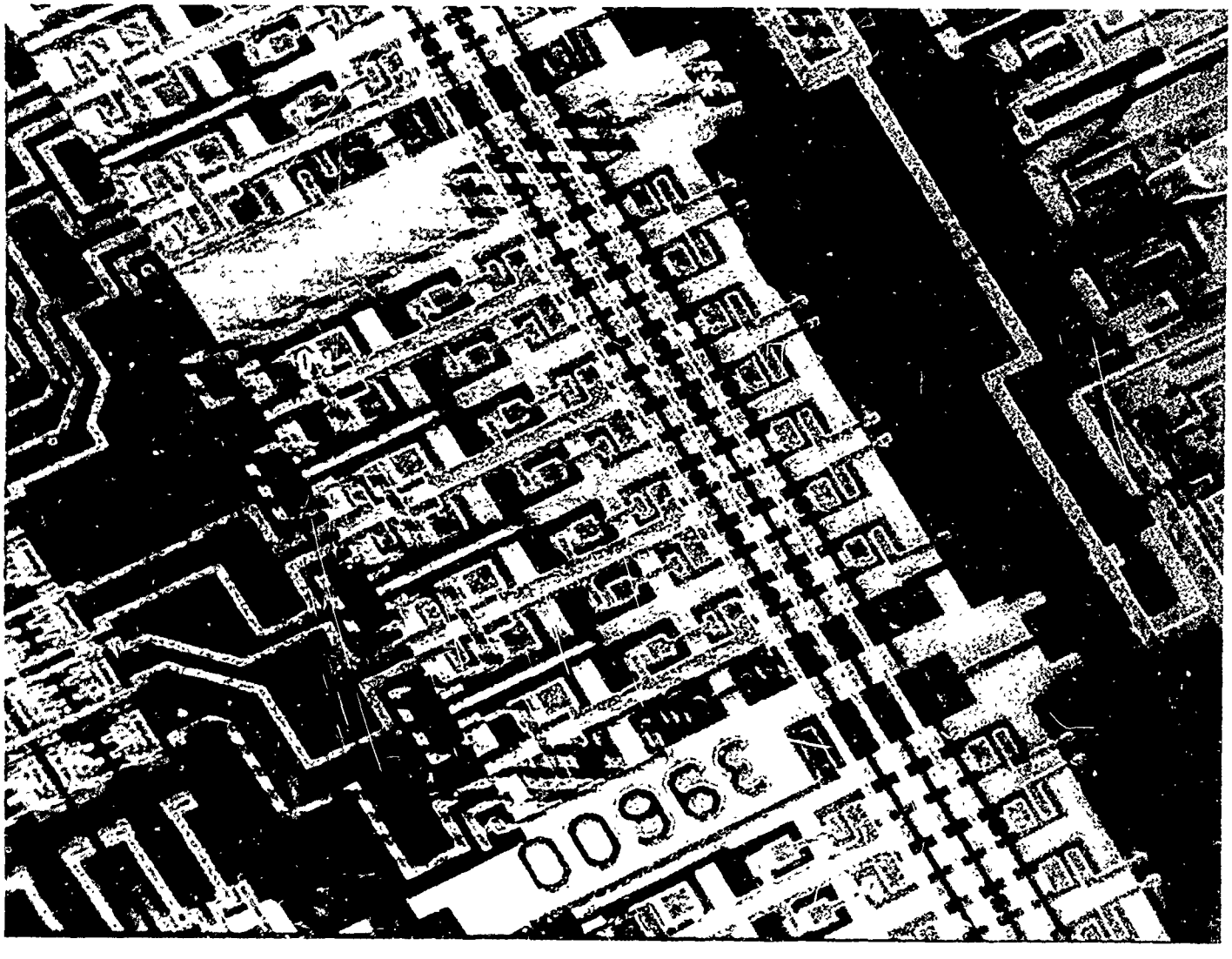


Photo 1-31 Programming Circuit to Column Decode Circuit Interconnection. Line Connected to Column Decode Emitters is Cycling at 0.7 Hz. 5 KV, Mag. - 200X

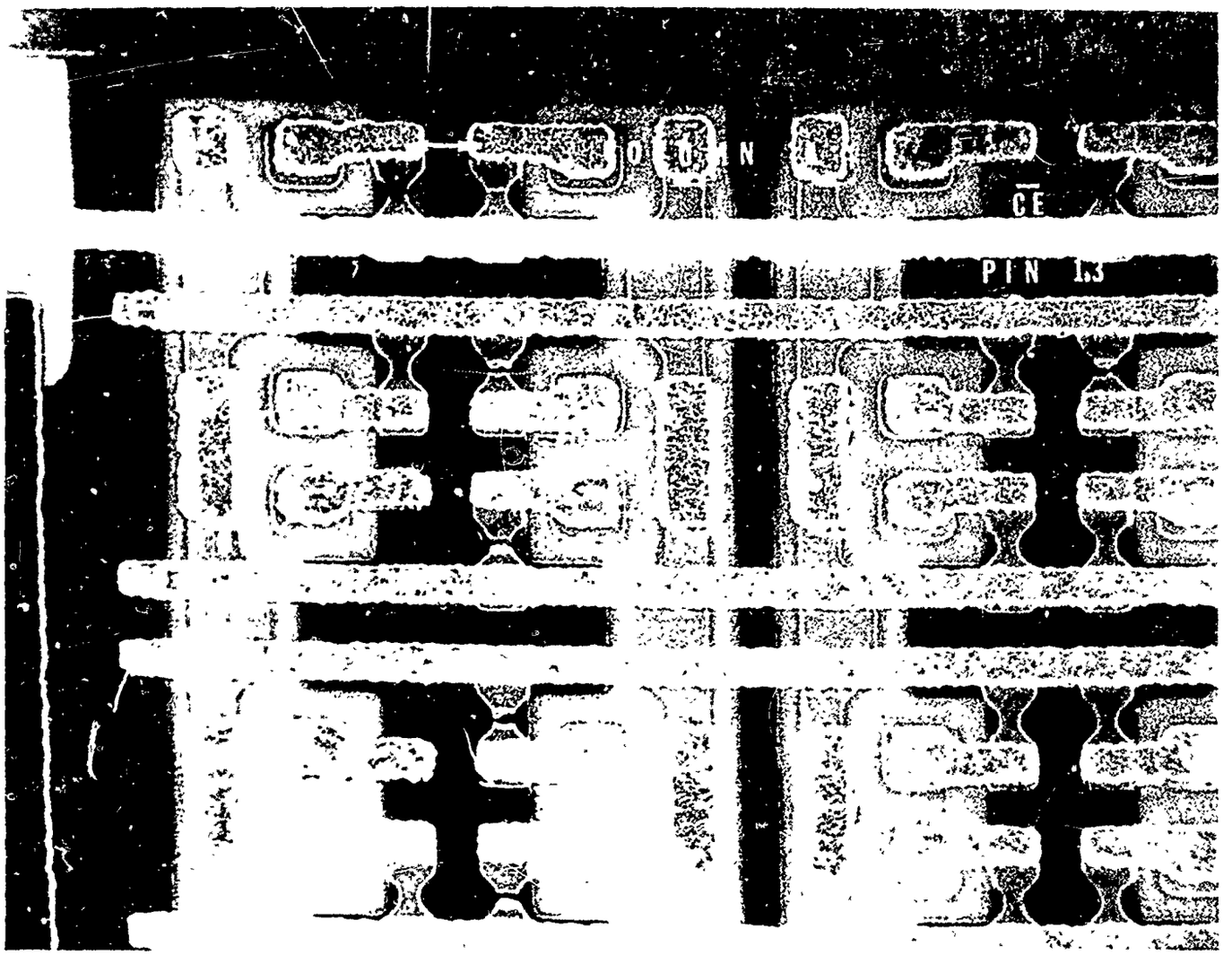


Photo 1-32 Voltage Contrast Micrograph of Column A and Rows 33 and 34. 5 KV, Mag.- 1200X

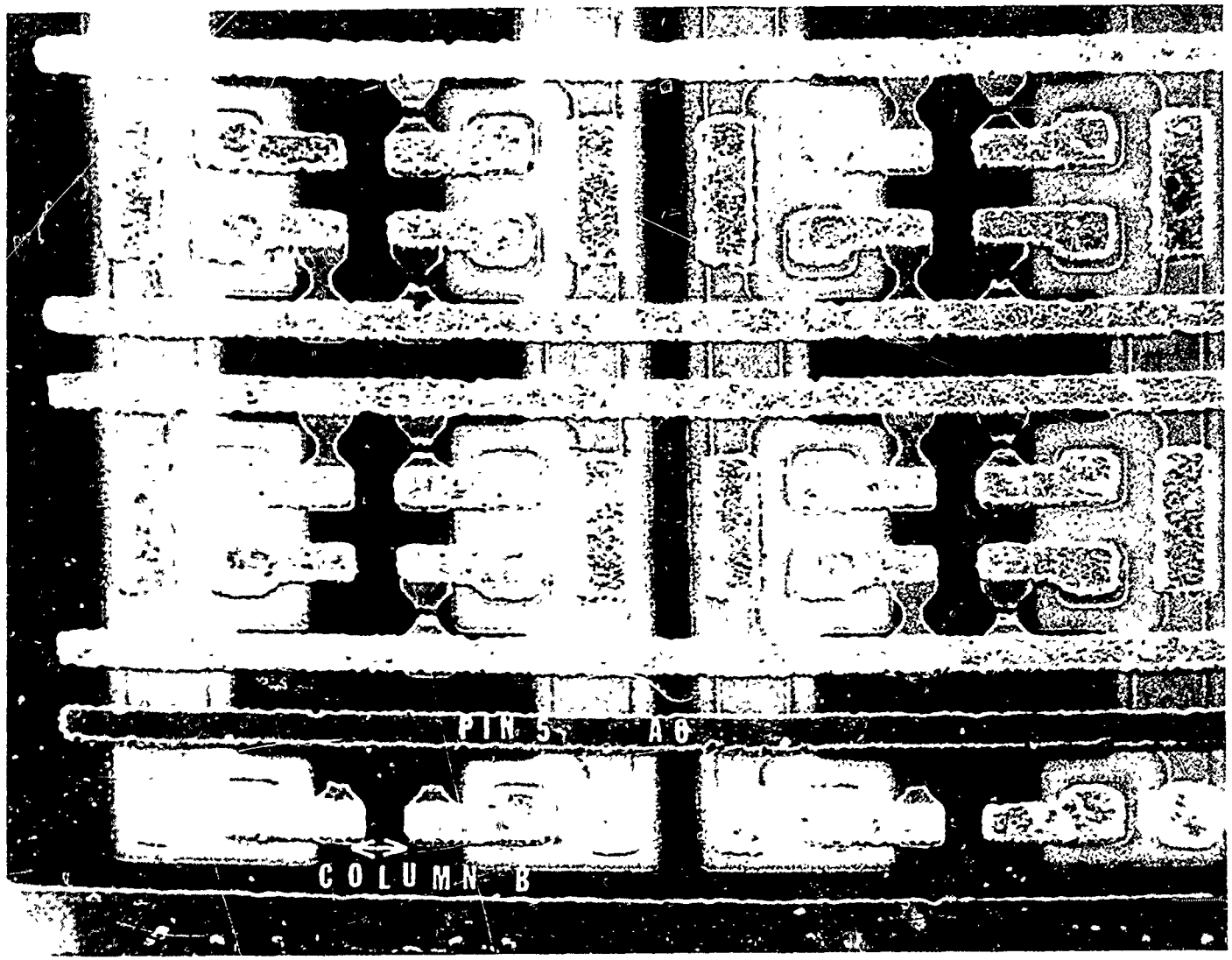


Photo 1-33 Voltage Contrast Micrograph of Column B and Rows 33 and 34. 5 KV, Mag. - 1100X



Photo 1-34 Voltage Contrast Micrograph of Circuitry Used to Address Rows 33 and 34. Pin 15 Addresses This Section. 5 KV, Mag. - 300X

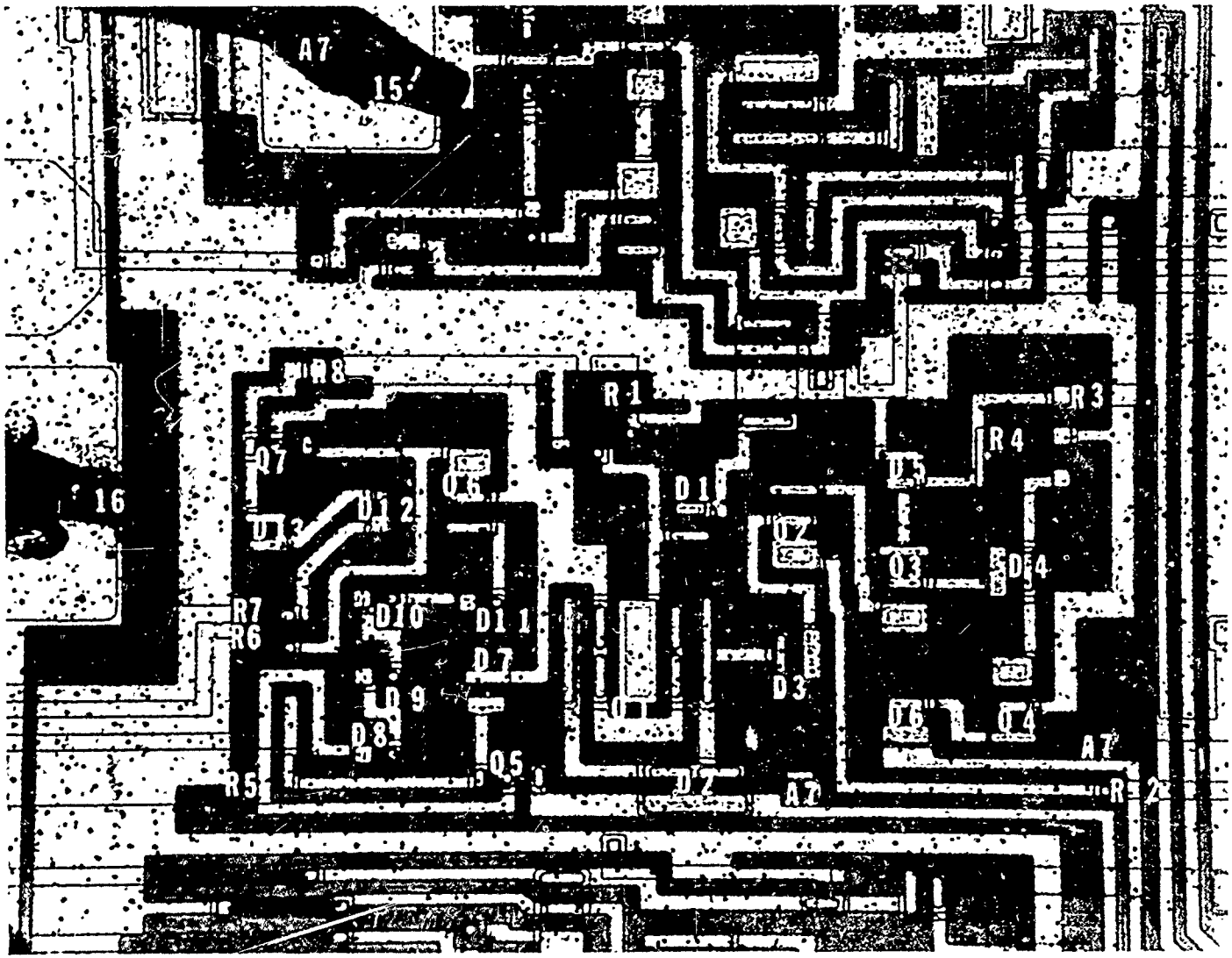


Photo 1-35 Light Photograph of Row 33 and 34 Address Section. Mag. - 225X

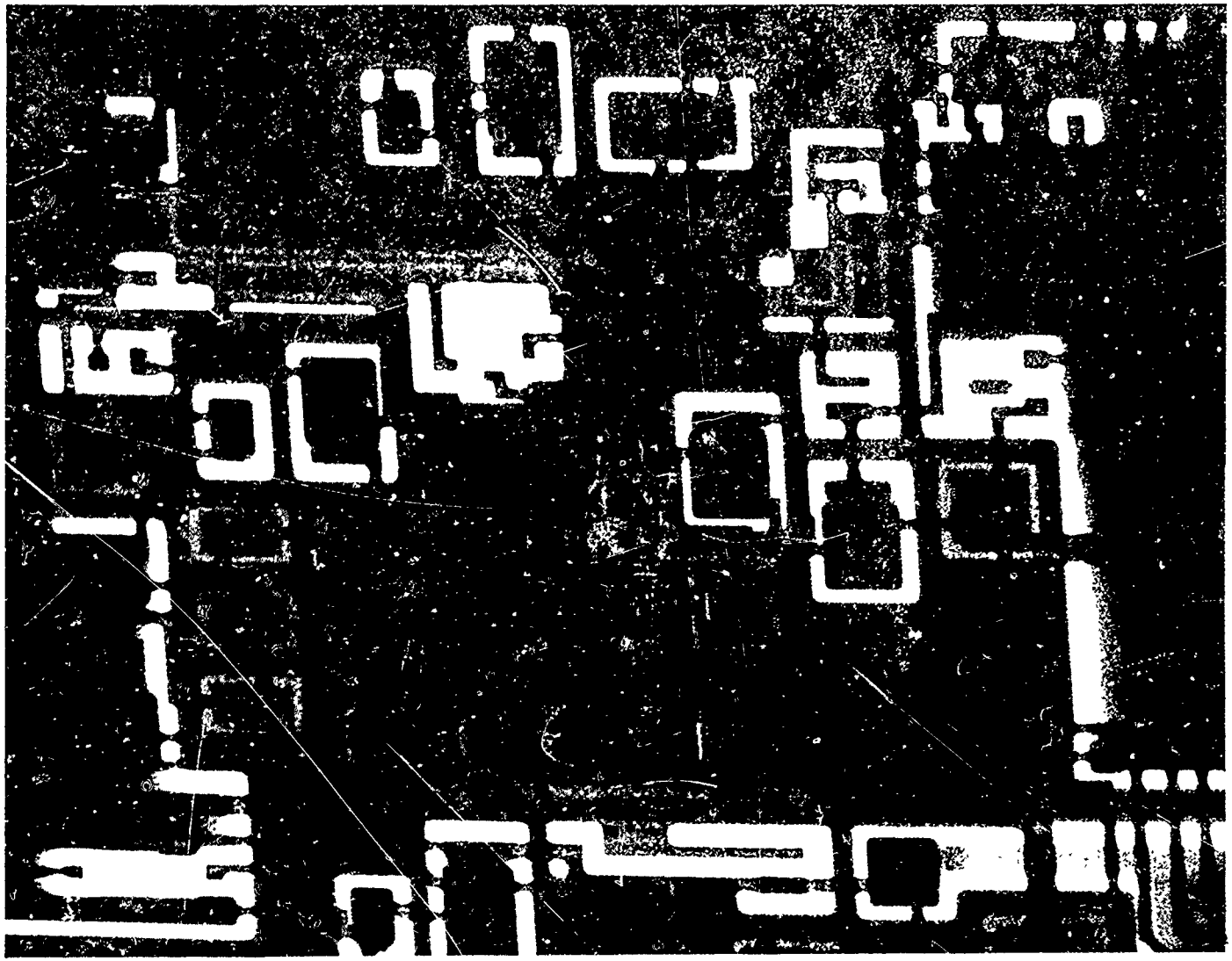


Photo 1-36 EBIC Image of Row 33 and 34 Address Section. 15 KV, Mag. - 325X

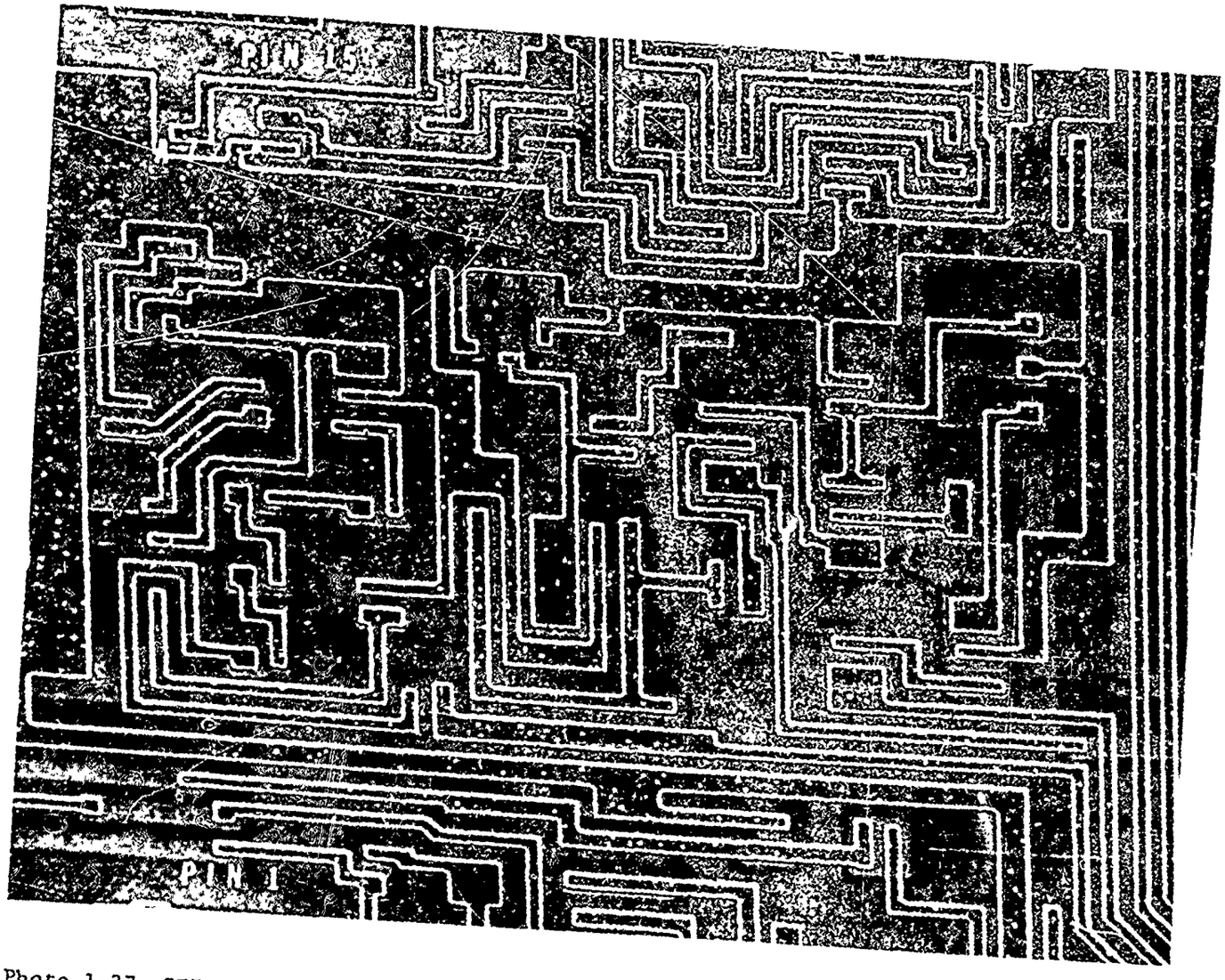


Photo 1-37 SEI of Row 33 and 34 Address Section; Same Area as Photo 1-36. Mag. - 325X

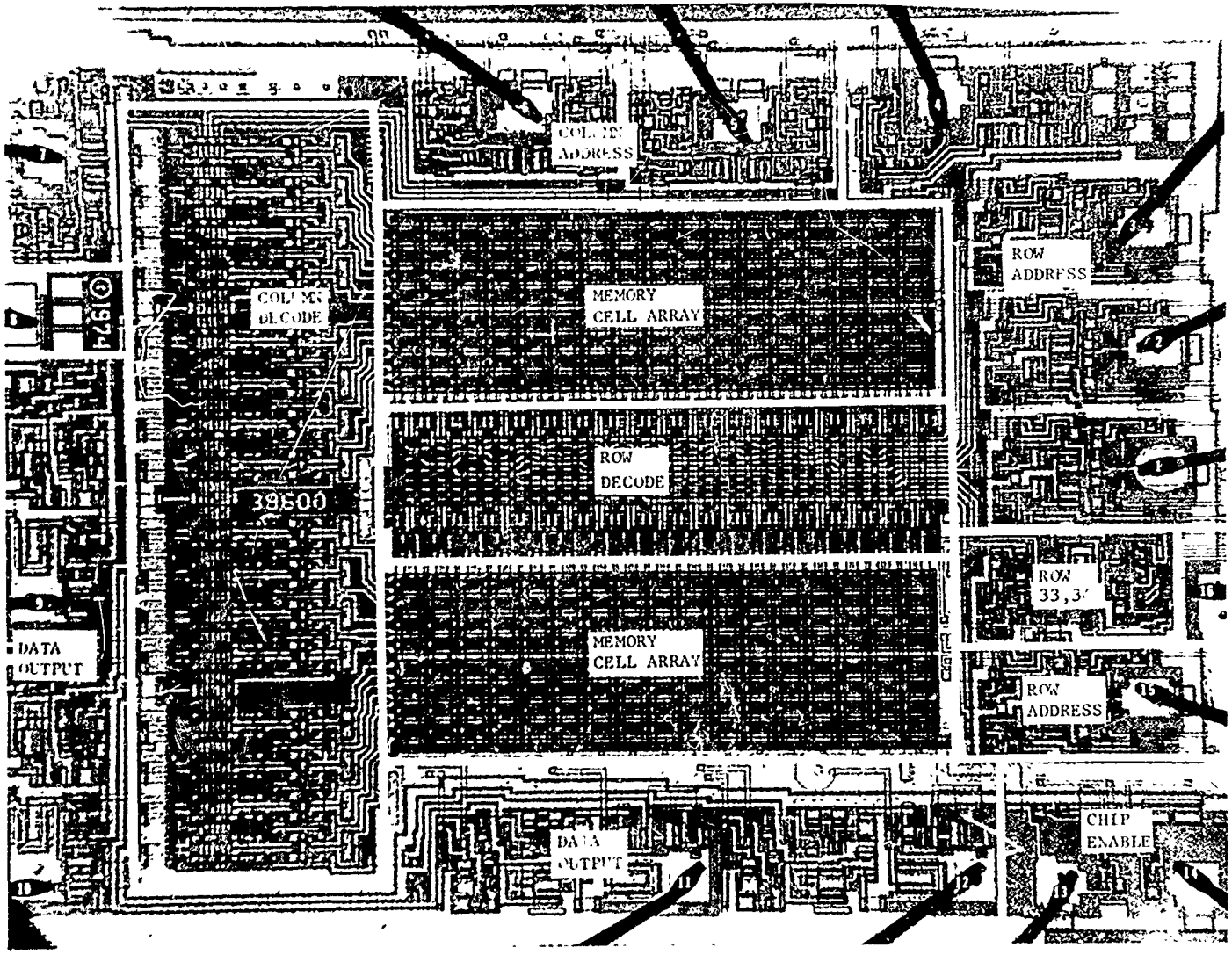


Photo 1-38 Light Photograph of Overall Chip with Functional Sections Identified - 40X

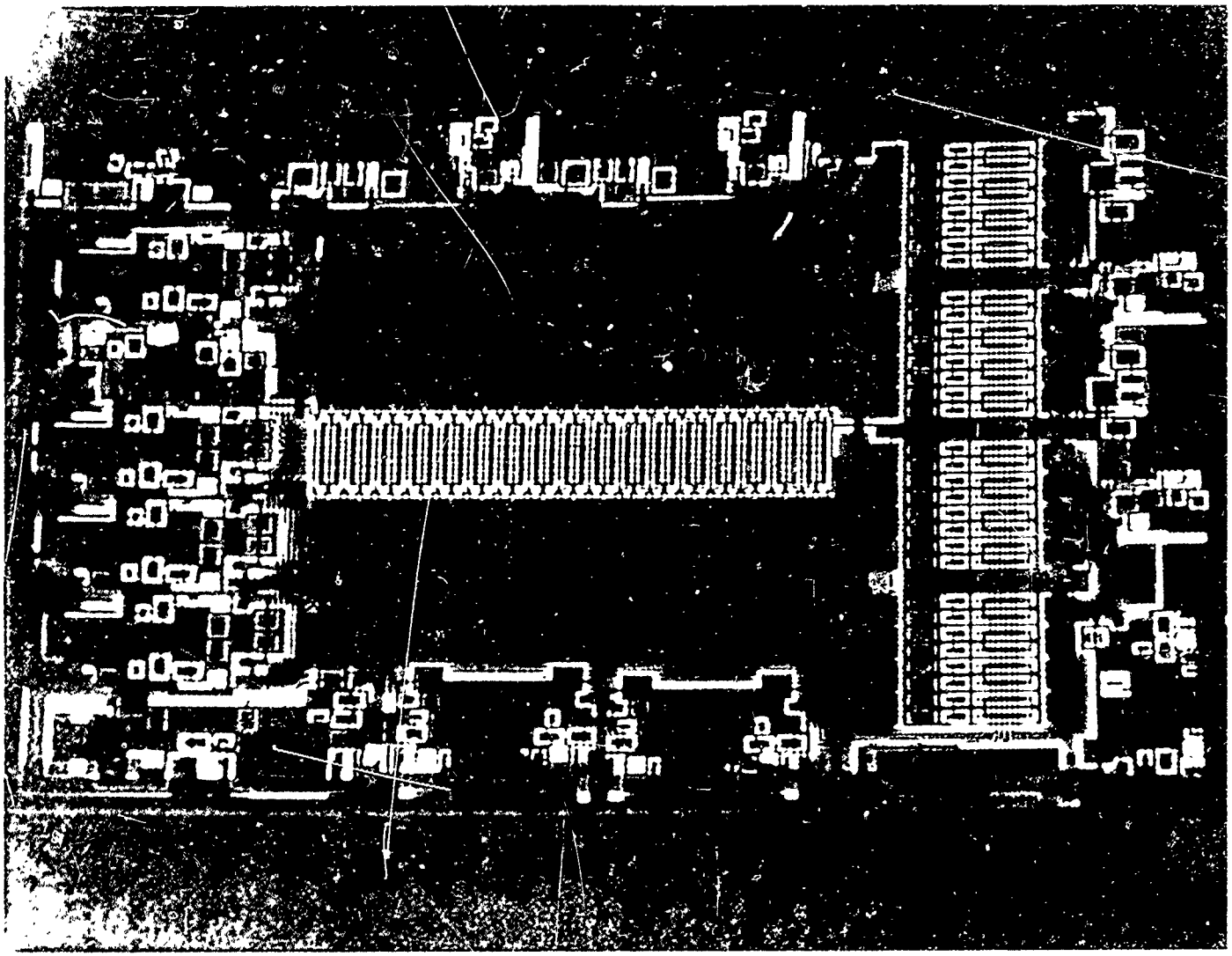


Photo 1-39 EBIC Image of Chip. Different Sections are Easily Discernible. 15 KV, Mag. - 40X



Photo 1-40 Voltage Contrast Micrograph of Failure in Column Decode Circuit. 5 KV, Mag. - 350X



Photo 1-41 Voltage Contrast Micrograph of Open Metallization in Column Decode. 5 KV, Mag. 1200X

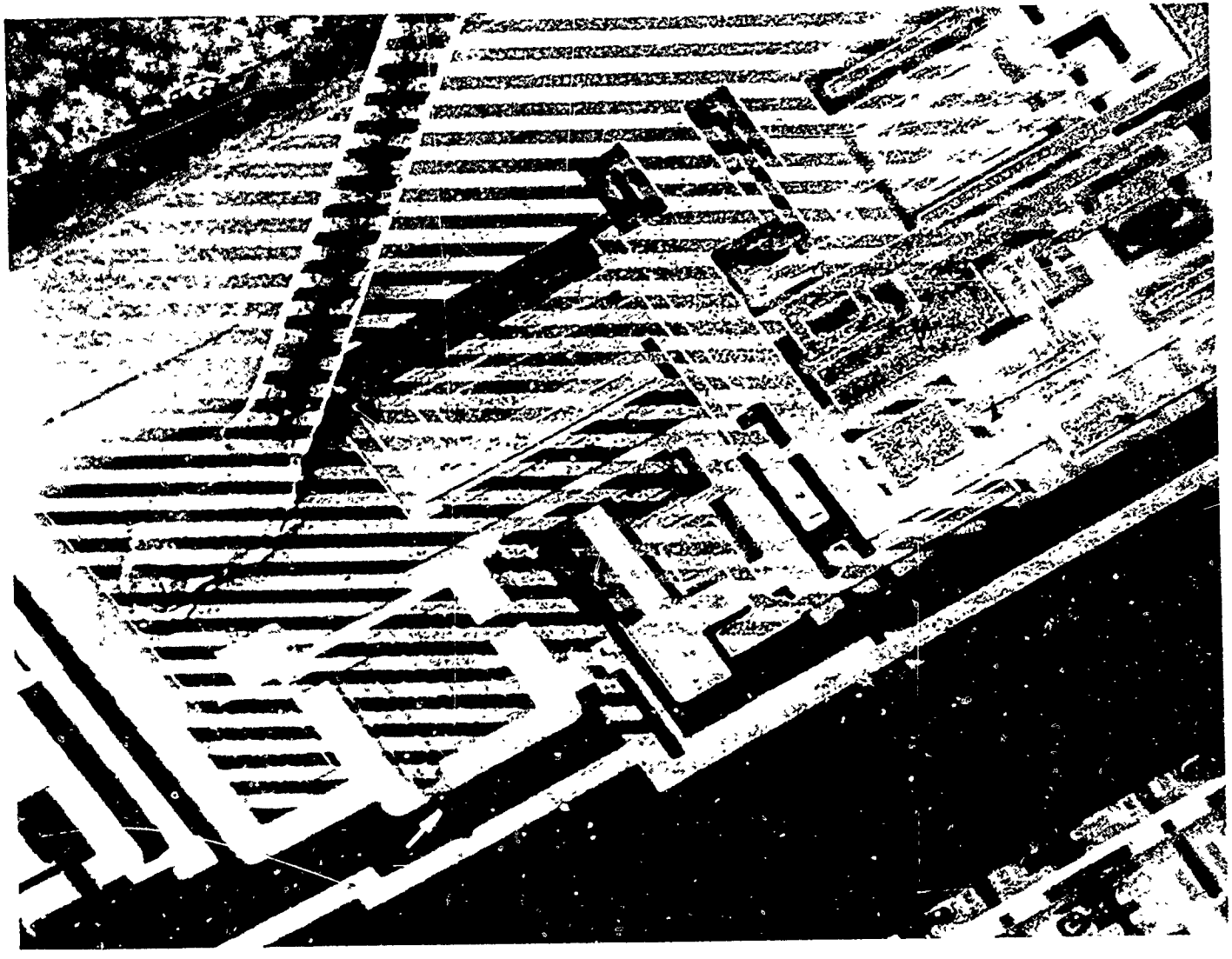


Photo 1-42 Voltage Contrast Micrograph of Output Functioning Properly; With Open Metallization (At Arrow). 5 KV, Mag. - 350X

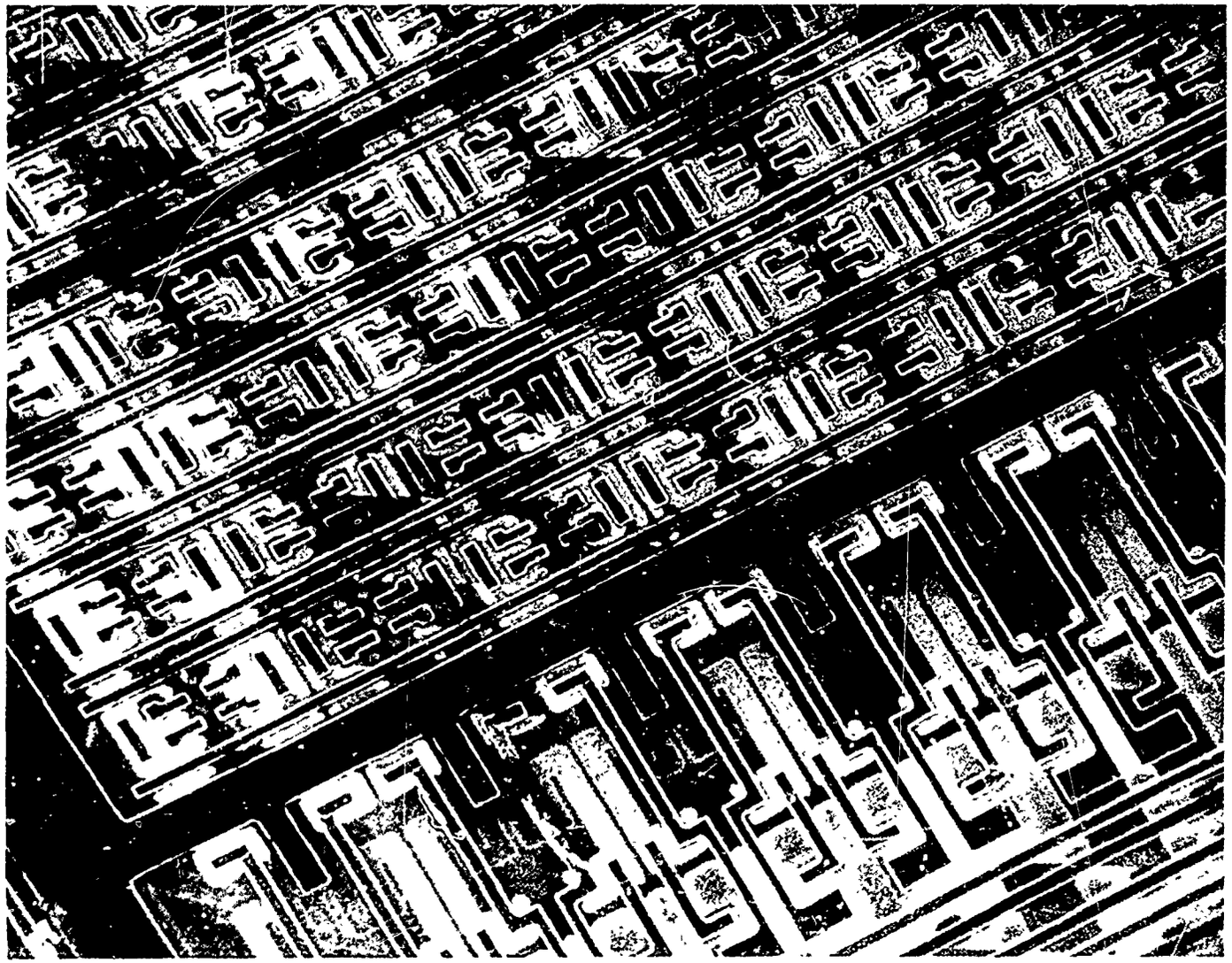


Photo 1-43 Voltage Contrast Micrcgraph of Failed Memory Circuit. Base Region Appears Dark When Other Columns are Addressed. 5 KV, Mag. - 350X

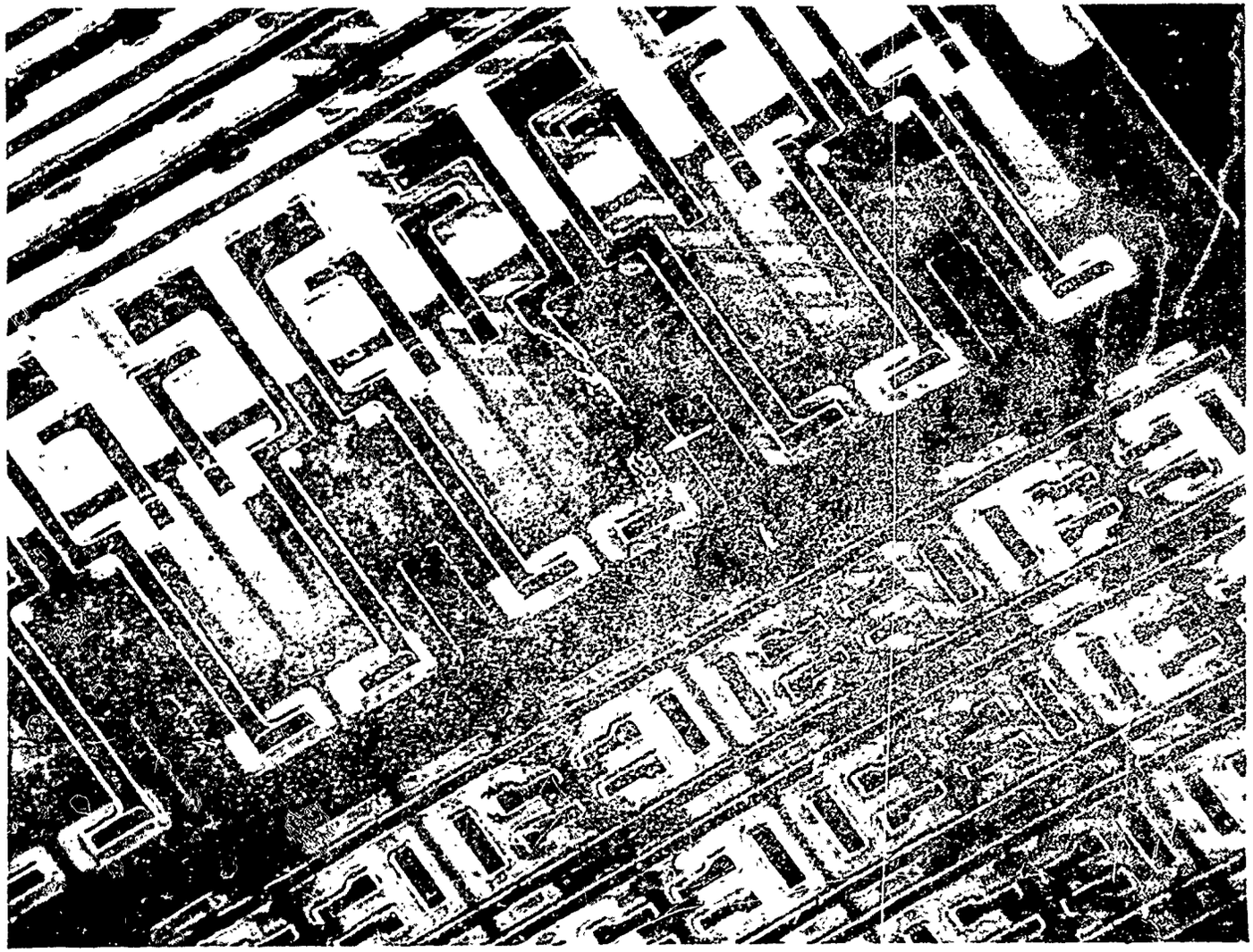


Photo 1-44 Voltage Contrast Micrograph of Open Metallization. Failed Row Cannot be Addressed. 5 KV, Mag. - 570X

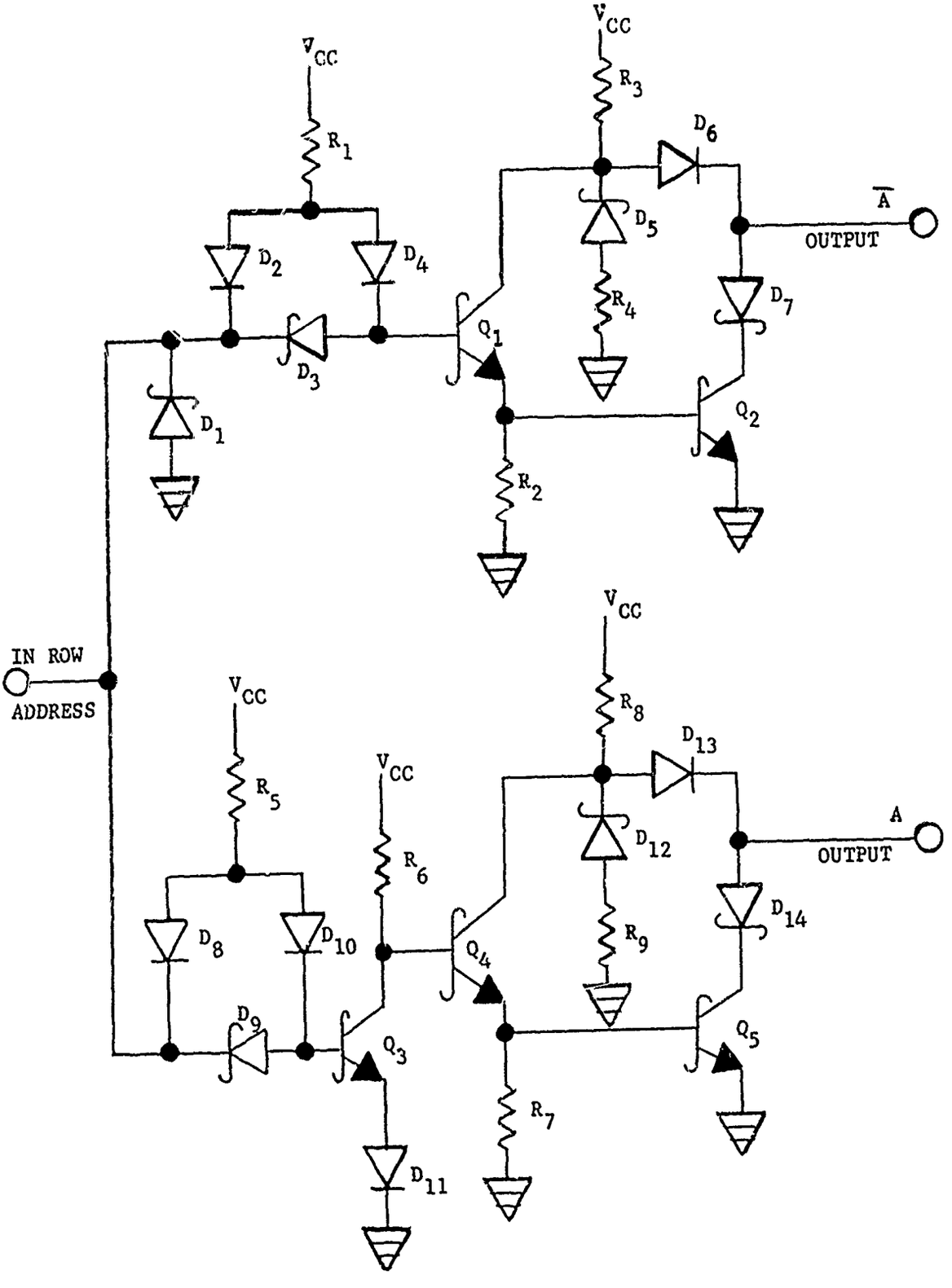


Figure 1-1 Schematic, Row Address Buffer

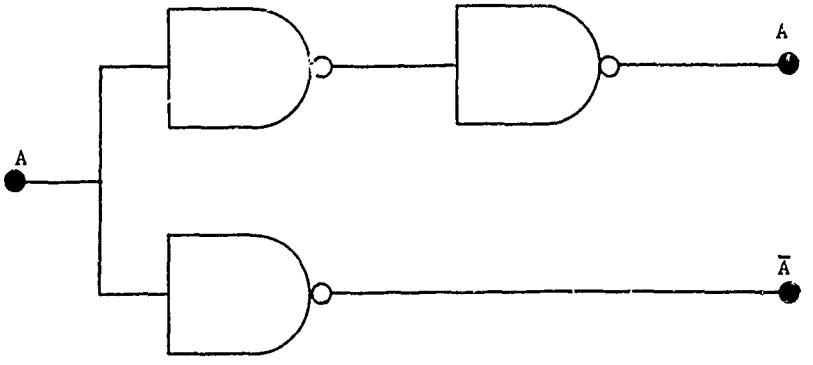


Figure 1-2 Logic Diagram, Row Address Buffer

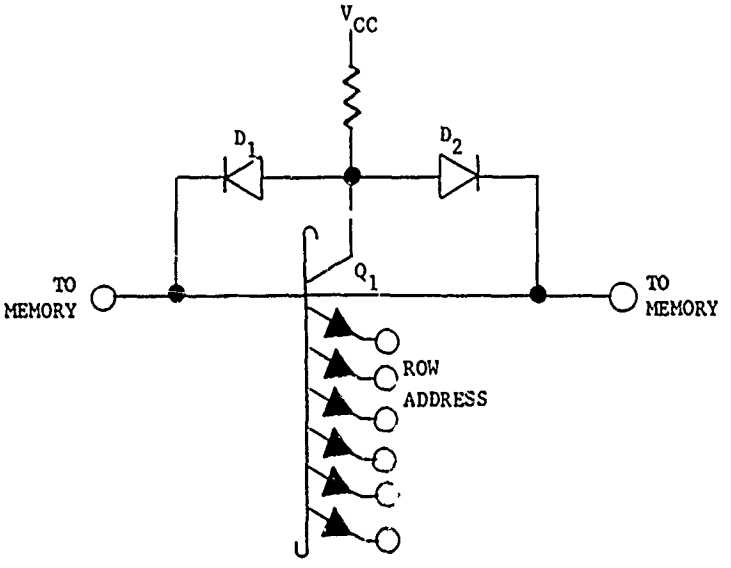


Figure 1-3 Schematic, Row Decode

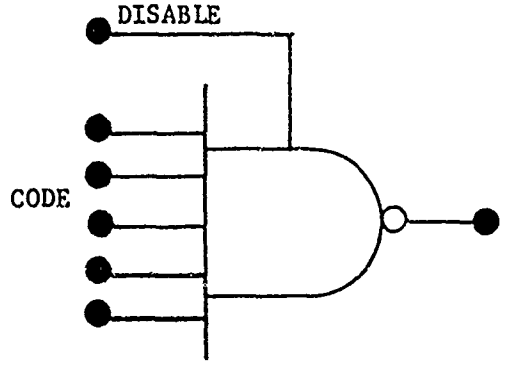


Figure 1-4 Logic Diagram, Row Decode (1 of 32)

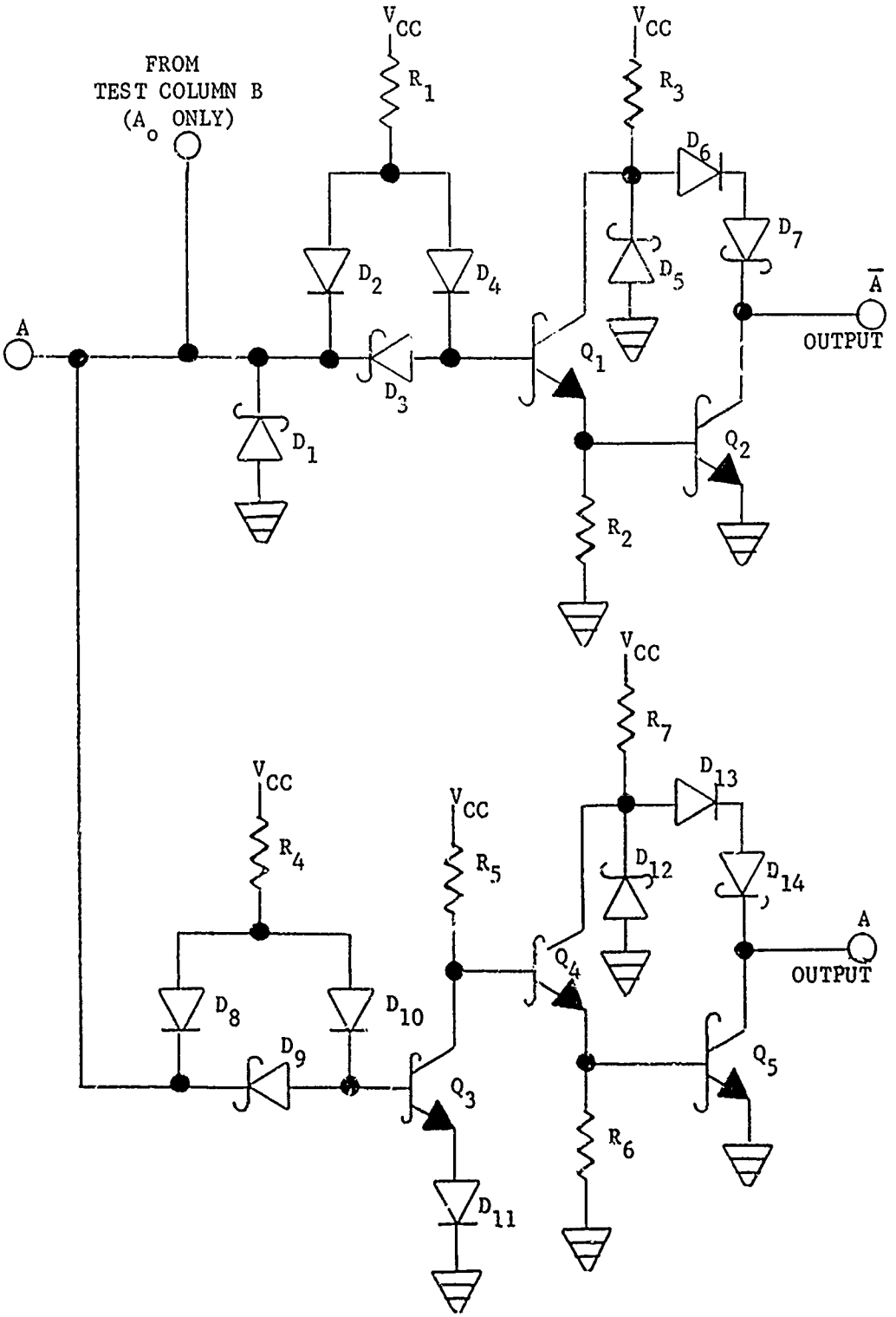


Figure 1-5 Schematic Column Address Buffer

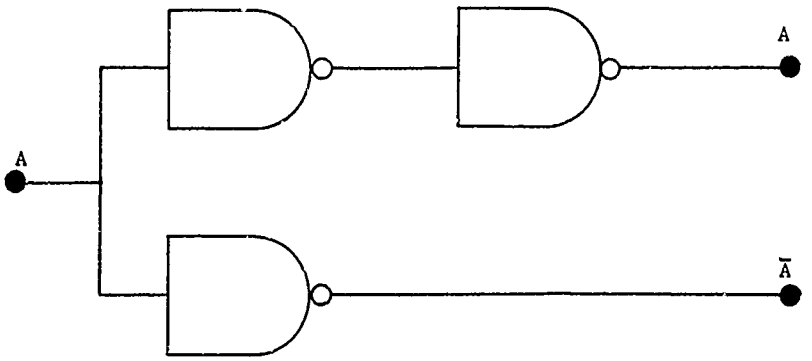


Figure 1-6 Logic Diagram, Column Address Buffer

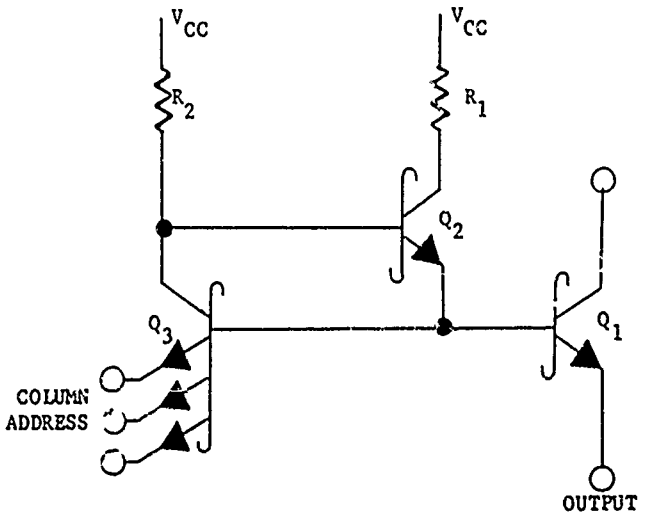


Figure 1-7 Schematic, Column Decode

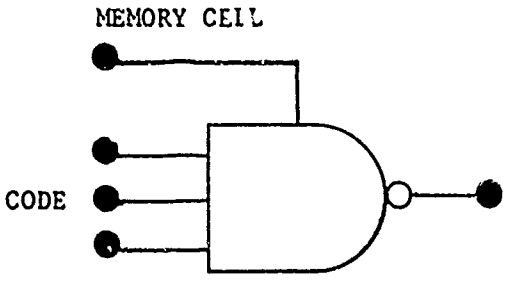


Figure 1-8 Logic Diagram, Column Decode (1 of 8)

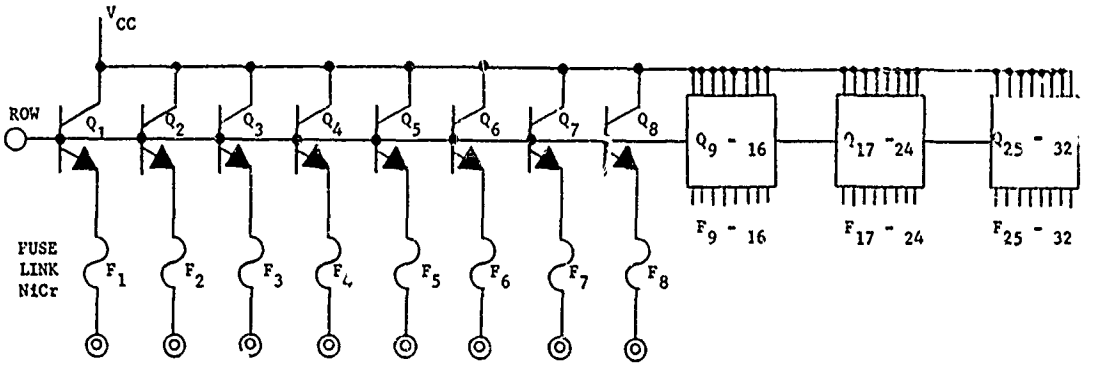


Figure 1-9 Schematic, Memory Cells

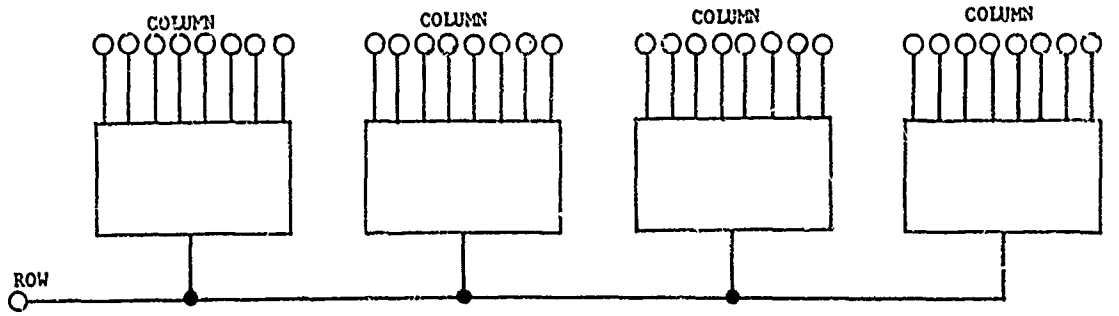


Figure 1-10 Logic Diagram, Memory Cells

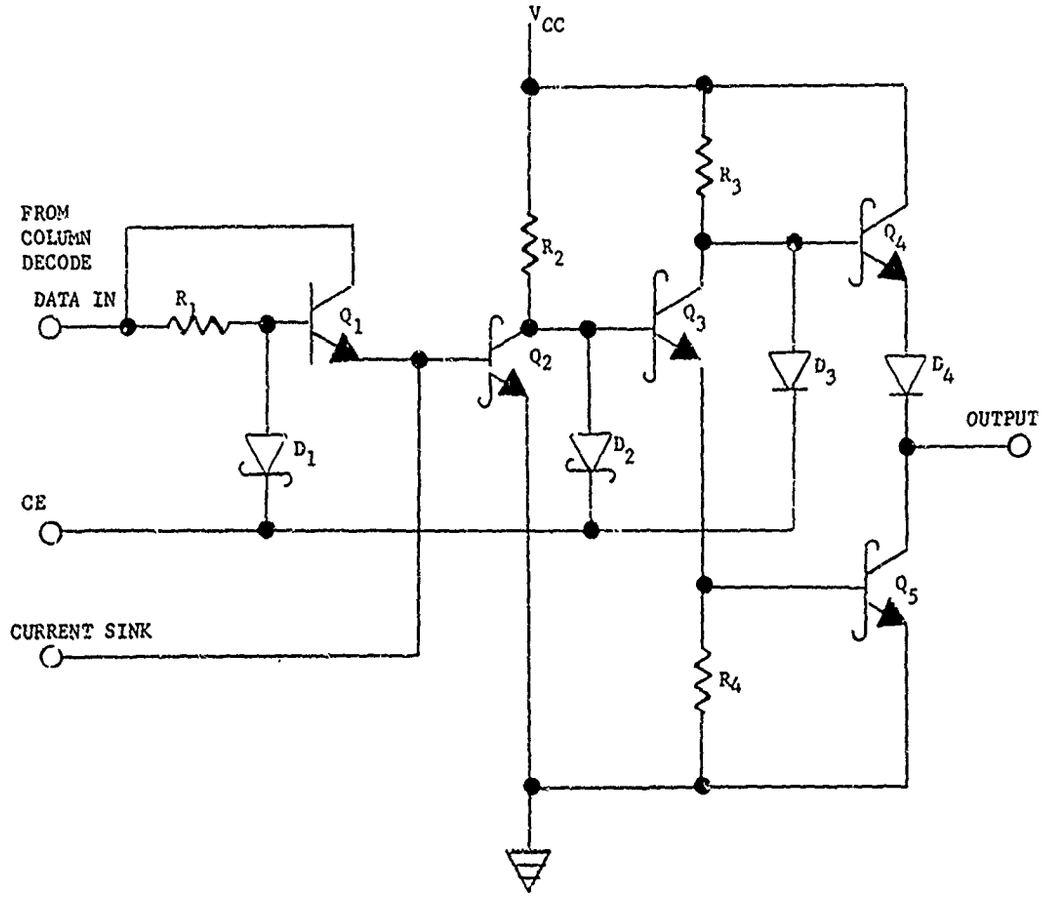


Figure 1-11 Schematic, Output

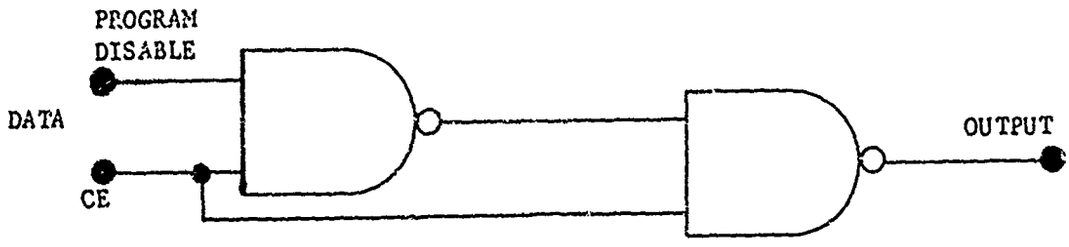


Figure 1-12 Logic Diagram, Output

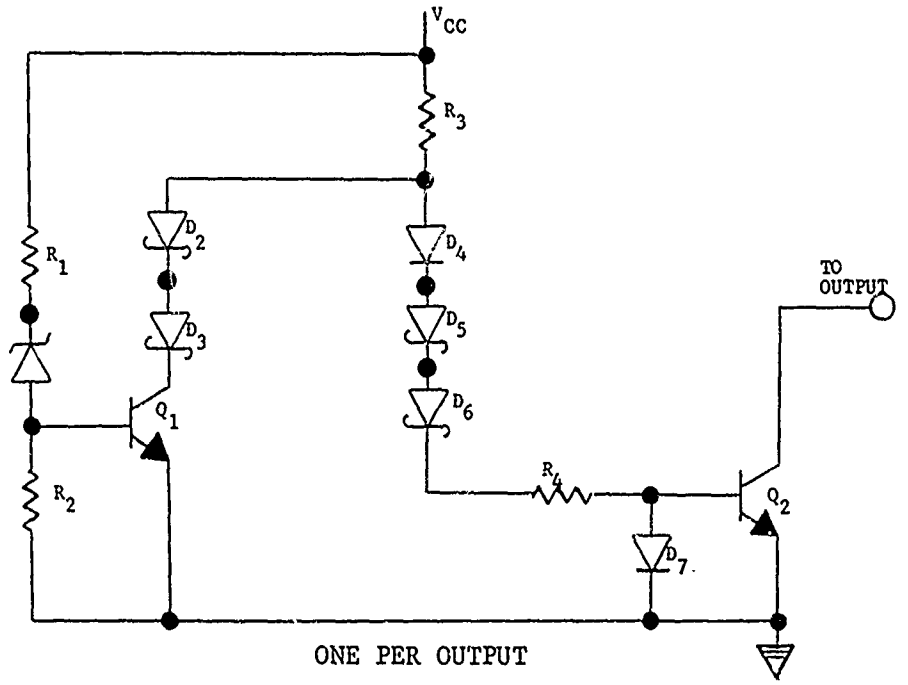


Figure 1-13 Schematic, Sense Amp Current Sink

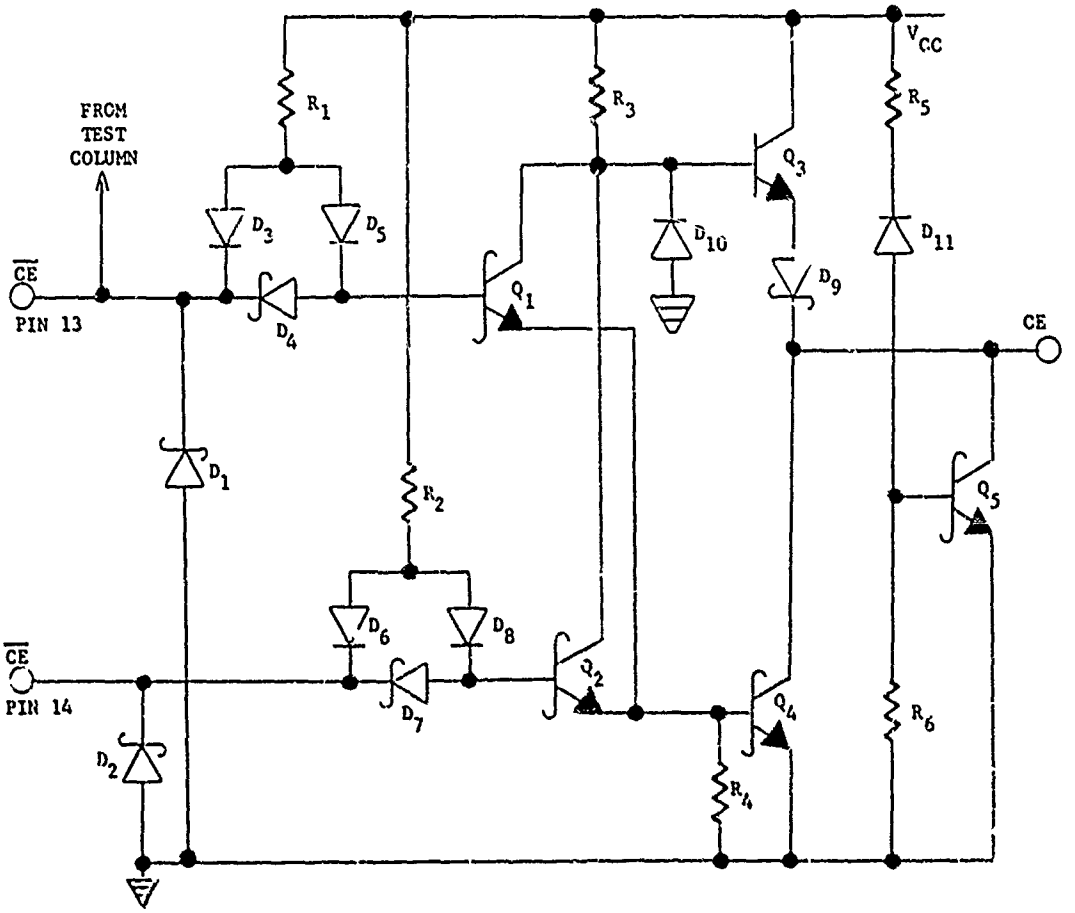


Figure 1-14 Schematic, Chip Enable

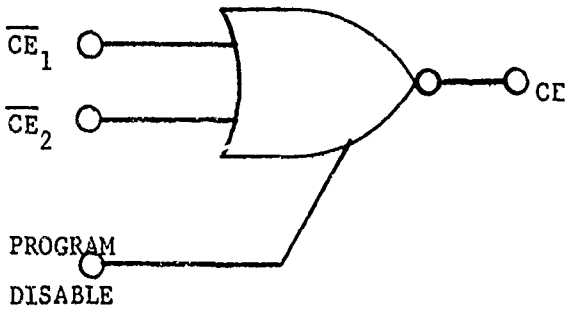


Figure 1-15 Logic Diagram, Chip Enable

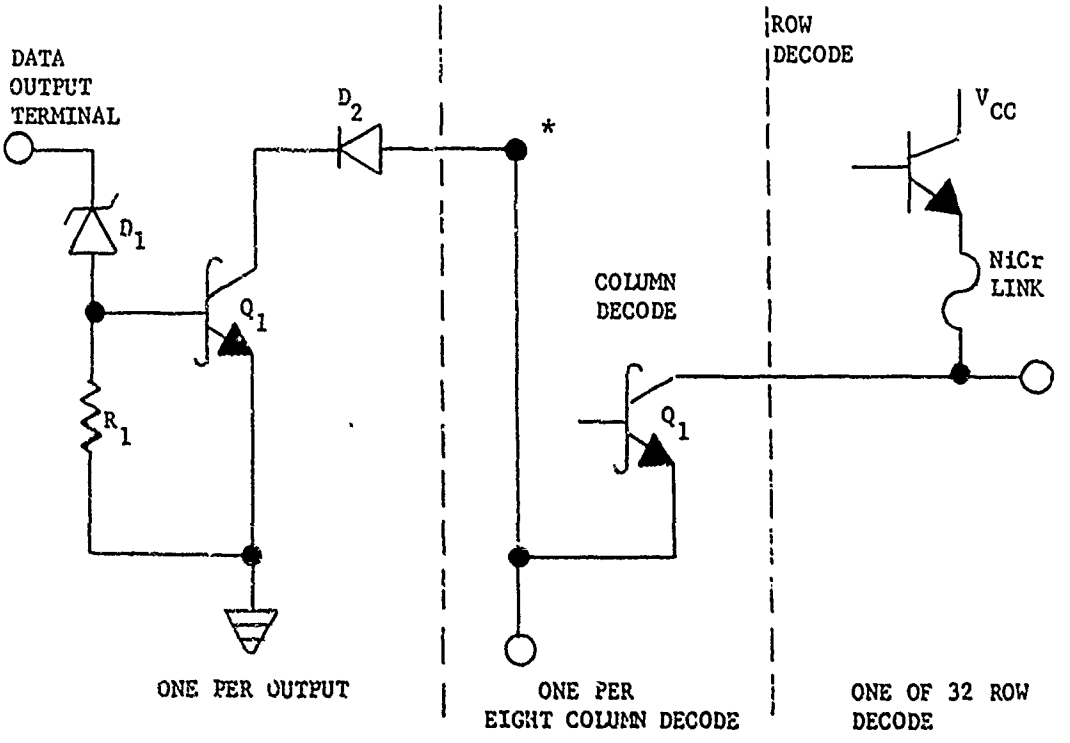


Figure 1-16 NiCr Link Program Circuit

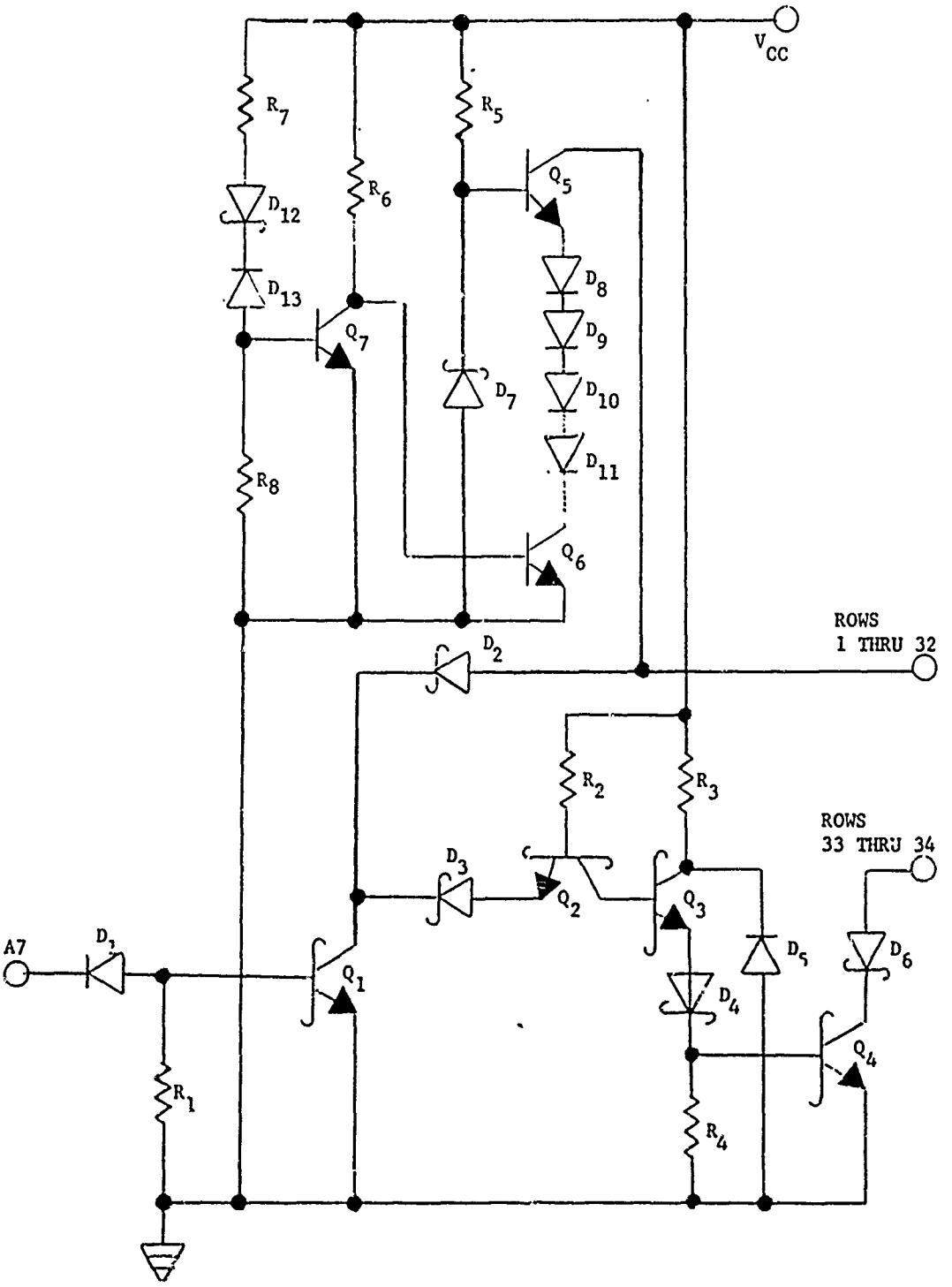


Figure 1-17 Schematic, Row 33 and 34 (Address Inverter)

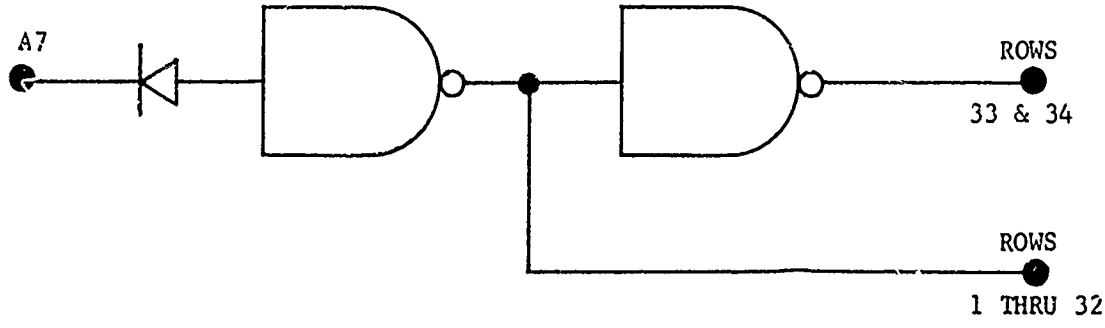


Figure 1-18 Logic Diagram, Row 33 and 34 Address Inverter

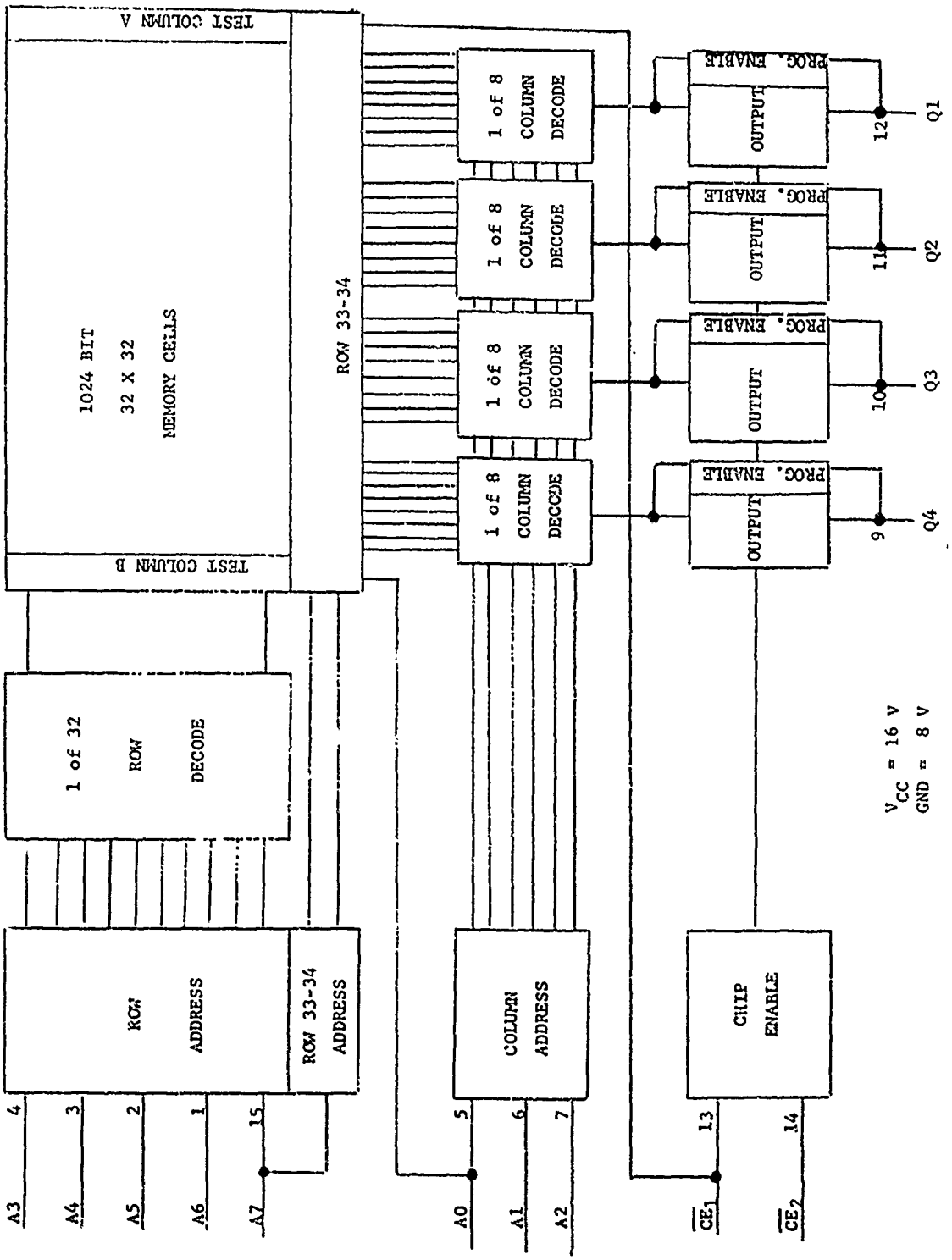


Figure 1-19 Block Diagram

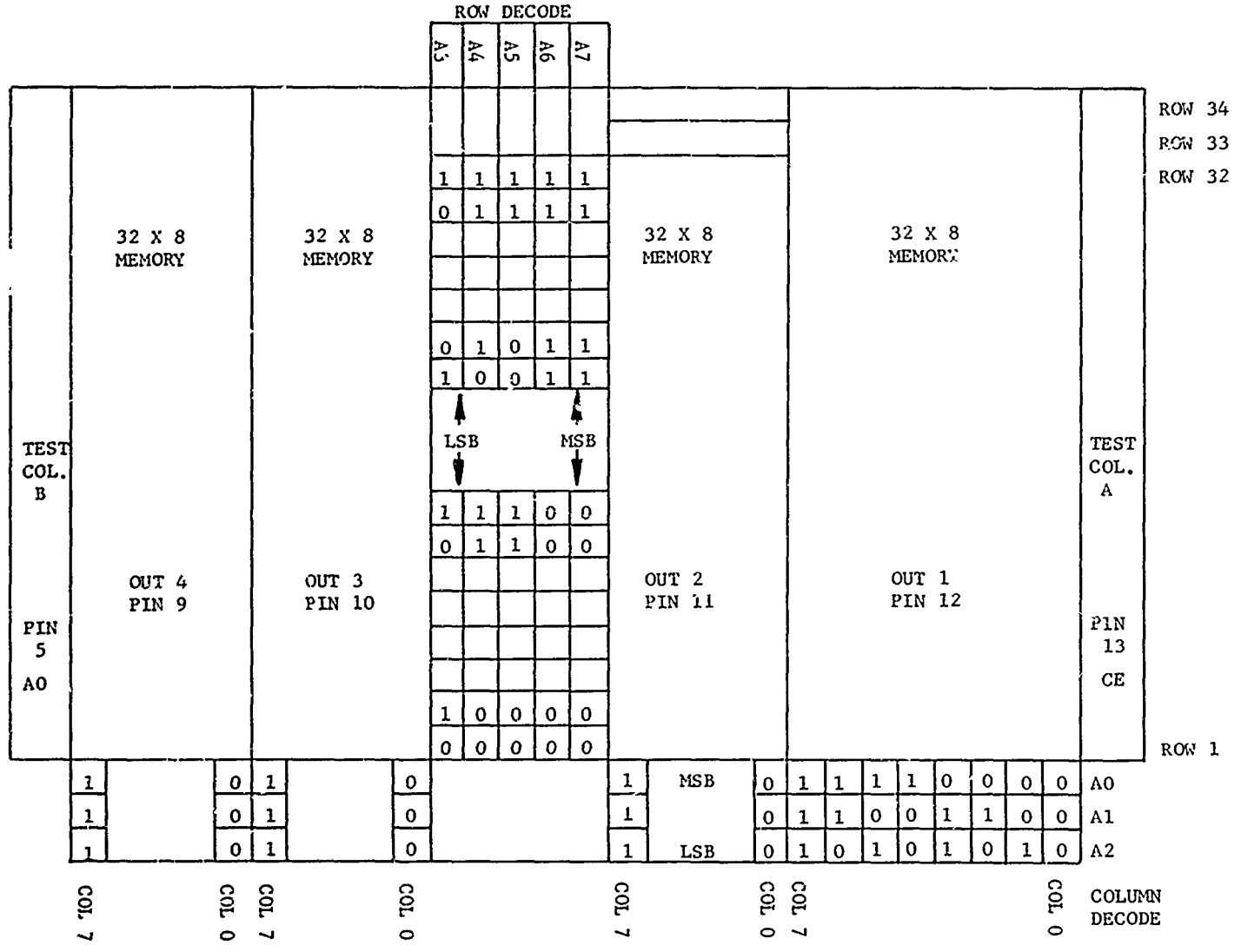


Figure 1-20 Bit Map

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4.2 1024 BIT AIM PROM (BIPOLAR)

Device Description

This device is a 256 x 4 bit bipolar PROM. The memory array is field programmable and programming is accomplished by avalanche induced migration (shorting of memory cell transistor junction). The version evaluated contained two chip enable inputs and an uncommitted collector output. The devices were packaged in a 16 lead ceramic DIP with a ceramic lid.

Electrical Characterization

Ten devices of this part type were used for this program. Five devices were reject samples which were utilized primarily for evaluating die passivation glass removal and electrical test set-up verification and five were devices which had passed supplier electrical testing and had been programmed to comply with Table 2-I.

Upon receipt the five good devices were electrically tested in accordance with the suppliers data sheet. These devices were serialized to provide individual identification. The DC parameters were measured, recorded and listed according to serial number in Table 2-II. All parameters were verified to meet the vendor specifications.

These five devices were functionally tested to verify compliance with the programmed memory pattern. Verification was performed using the memory test circuit in conjunction with a Hewlett-Packard Model 1601A Logic Analyzer. This analyzer displayed the eight bit address codes and the respective four output data bit levels. The analyzer simultaneously displays 16 rows, each serially containing the eight bit address codes and four output data bits. The sequence of 16 rows displayed is controlled manually by an eight bit trigger word which is common to the eight address inputs for the device under test. The repetitive display of 16 address and data bit rows were visually verified to comply with the programmed data table. This required 16 frames of 16 rows each to totally verify each device. All five devices were verified to contain the correct program. The functional test frequency (LSB) was 100 kHz.

Package Delid and Glass Passivation Removal

This device was packaged in a 16 pin dual in-line ceramic package. The package lid was removed by grinding, using a diamond impregnated wheel. When the lid was thinned to about 200 microns, a sharp probe was used to enter the package cavity and remove the lid. Care was used to avoid contacting the interconnect wires or chip.

The chip surfaces and package cavity was flushed with a mild detergent/DI water solution, rinsed with DI water followed by Isopropyl Alcohol and gently dried with dry Nitrogen. This removed the ceramic particles which are introduced during package delid.

Removal of the glass passivation was first evaluated using one of the five reject devices. This device utilizes a two level aluminum conductor system. Both levels have a glass overcoat so it is necessary to remove about 2 microns of glass without damaging the metallization. The etchant selected was a buffered HF which was stopped with Glycerine. This etch was selected to minimize etch attack on the aluminum. The etch used was:

125 ml	Hydrofluoric Acid	48%
25 ml	Nitric Acid	70%
250 ml	Glycerine	

The total etch time was 45 seconds followed by DI water and Isopropyl Alcohol rinses and Nitrogen drying. Although it was not evaluated, it is believed that a water stopped buffered HF would have satisfactorily removed the glass overcoat.

The glass overcoat was removed from device S/N 1 using the selected etchant and etch times. Following glass removal the functionality of the circuit was verified using the same procedure used for initial functional verification. The device functioned properly and programmed data was correct. A photograph was taken to show the complete die (ref Photo 2-1).

Circuit Characterization

Device S/N 1 was inserted into an SEM test socket. The test socket provides electrical connection between the device and an external connector on the SEM specimen stage. All electrical stimuli can be applied to the test device to obtain complete functional operation of the circuit during SEM examination. No special preparation was made to reduce extraneous charging effects from the device package. The general procedure avoided beam landings on non-conductive surfaces of the package to reduce these surface charging effects.

The acceleration voltage used for the SEM was 5 kv. This voltage was selected to reduce the range of the primary electrons and minimize the beam influence on circuit operation. A low acceleration voltage also reduces charging effects on non-conductive surfaces which improves circuit voltage contrast. The beam current at the circuit surface was adjusted to 200pA.

Initial operation of the complete chip was observed while all address lines were exercised. The memory address was sequentially stepped through all 256 address codes. A nominal 5V was supplied to the circuit. CE_1 and CE_2 were held at a low state. Circuit operation was observed with the SEM scanning the chip at a TV rate. The frequency of address codes is adjusted to allow observation of the various circuit operations. This provides the operator with a familiarity of the chips functional organization. This is an important part in developing the electrical circuit schematic. As one analyzes a specific part of the circuit at a higher magnification, you must be familiar with the general circuit organization outside of the field of view.

Once the general overall circuit layout is identified, the next step is to concentrate on defining individual functional circuits. The row address inverter is the first circuit examined. Photo 2-2 shows the voltage contrast micrograph for the A_2 row address inverter circuit. An active address signal (0.5 Hz) was applied only to the A_2 input. The related circuit was easily isolated by the active response to the A_2 input signal.

Positive and negative voltage contrast micrographs are taken of the circuit function to be defined schematically. To supplement the voltage contrast photo, a light microscope photo was also taken (ref 2-3). In addition an EBIC micrograph was taken to delineate the diffusions common to the row address inverter circuits A_0, A_1, and A_2. Photo 2-4 is the secondary electron image (SEI) showing the same area as the EBIC Photo 2-5. The EBIC photo was first obtained using a 10 KEV beam with pin 8 at ground, pins 13 and 14 open and the remaining pins connected to the SEM sample current amplifier (SCA) input. The 10 kev beam did not penetrate the metallization and this produces a discontinuity in the EBIC response where metallization covers the junction. To alleviate this the beam voltage was increased to 15 kev and a second EBIC micrograph was taken. This EBIC image is shown in Photo 2-6. A comparison of Photos 2-5 and 2-6 illustrates the significance of beam voltage. Image contrast is determined by the selected gain of the SCA. To differentiate junctions by EBIC it is necessary that beam generated currents flow through the SCA and ground circuits. Therefore, if two diffusions with a common junction have a parallel current path which has a resistance much less than that of the SCA circuit, the beam generated current will be confined to the lower resistance path. In this case no EBIC response will be visible in the EBIC image. Also, the SCA gain can be responsible for concealing the response for portions of a circuit. For example, if the SCA gain is set too high the large EBIC signals will saturate the SCA and the relative intensities will not be discernable. Likewise, if the SCA gain is too low, the small EBIC signals will be below the SCA threshold and are lost. This is readily observed in Photos 2-5 and 2-6 where base diffusions for the input transistors are visible in Photo 2-5 and not in Photo 2-6. The EBIC photos show the emitter, base and resistor diffusions within a common collector tub. The resistors which terminate with V_{CC} are contained in a common tub above the transistor cells. This illustrates a parallel path which circumvents the SCA circuit. The resistors are P diffusions in an N tub. One end of the resisitors and the N tub are connected to V_{CC}. Therefore, the EBIC does not flow in the SCA circuit and these resistors are not visible in the EBIC photos.

The SEM and light photos were used to follow the signal path and outline the schematic diagram. The voltage contrast intensity provides a qualitative indicator of the circuit node voltage level. For example, the signal applied to the emitter of Q1 in Photo 2-1 is switching from approximately 0.5 to 4.5 volts. The signal present on the base of Q1 is switching between 1.2 to 2.1 volts.

The electrical schematic is developed by following the signal flow through the circuit. The signal amplitude and phase changes provide important insight relative to circuit operation. The EBIC and light photographs provide

additional visual references to cross-check the schematic. As the initial circuit schematic is developed, the circuit components are identified by sequential component numbering and this identification is recorded on one of the photographs. The final circuit schematic is drawn from the initial, to organized and arrange the components into an orderly circuit configuration. At this time, the circuit was reverified and circuit operation was reviewed. If any questions arise, the circuit and schematic were rechecked and the questions resolved. The circuit schematic for the A_2 row address inverters are shown in Figure 2-1. All transistors in these inverters are schottky clamped. The method used to identify a schottky clamped transistor is by light microscope. Because they are shallow diffusions and in many cases covered by metallization, voltage contrast or EBIC were not effective. Light microscope identification was performed with all metallization stripped from the chip. The row address inverter is a basic two inverter circuit which produces an inphase and a complement of the input signal. There are five row address inverters which produce ten binary address signals for row decoding. The logic function for this circuit is shown in Figure 2-2. This is a two inverter circuit.

The same procedure was followed to determine the circuit configurations for the remaining chip circuitry. As the functional blocks are described schematically these portions of the chip are identified accordingly. The circuits were developed from the address inputs through memory to data outputs. Next the memory program and chip enable circuits were described. Following this any remaining circuitry is documented.

The next circuit analyzed was the row address decoder. The vendor's data sheet indicated the device was organized as 256 x 4 bits. An overview of chip operation showed a 32 bit row decode and an 8 bit column decode. This organization agreed with the data sheet block diagram. Voltage contrast examination of the row decode was complicated by a wide second level metallization stripe (V_{CC} buss) overlaying three of the row address lines. This did not prevent signal tracing. The respective address lines can be checked prior to their entrance under the metal stripe and at the output of the decode AND gates. If a discontinuity is encountered which is located in the metallization or interconnections beneath this V_{CC} stripe, it would be necessary to remove the second level metal to locate the failure site.

The voltage contrast micrograph of the row address decoder is shown in Photo 2-7. This photo was taken with a 0.7 Hz signal applied to row input A3. The decoder circuit runs parallel with the memory array. The secondary electron image (SEI) and EBIC micrographs are shown in Photos 2-8 and 2-9. The EBIC photo was taken using the same terminations used for row address and the beam voltage was 15 Kv. In this EBIC photo half of the decode diodes are obscured by overlaying second level metallization. The range of the primary electrons are limited by this increased surface film thickness and therefore this beam energy does not produce an EBIC signal. The decode diode EBIC response in the unobstructed areas does not show the N (emitter) diffusions. The cell isolation junctions, R3 resistors and the Q1 and Q2 emitter diffusions are easily located. The light photograph is shown in Photo 2-10. The schematic showing 1 of the 32 row decoder circuits is shown

in Figure 2-3. The decode circuit utilizes six diodes to form a six input AND gate. Five inputs interface with row address signals and the sixth is a common row decode disable line. The AND gate is followed by a three stage inverter driver. When all decode diodes for one circuit are high, ground is supplied to one memory cell row through transistor Q3. The logic function for the row decoder is shown in Figure 2-4. This circuit is a six input NAND gate.

Next the memory cell circuit was analyzed. Photo 2-11 shows the voltage contrast micrograph of eight memory cells. The row decode supplies a ground path to the addressed memory row. Photo 2-11 shows the addressed row (center) where the common collector is low. The memory cell transistors are multiple emitter-base diffusions in a common collector tub. The base diffusions are floating and the emitters are connected to their respective column decode and column program decode circuits. The SEI and EBIC micrographs are Photos 2-12 and 2-13. The programmed cells (shorted E-B) are evident by their larger appearance which includes both emitter and base. The light photograph of the memory circuit is shown in Photo 2-14. Photos 2-11 through 2-14 show eight of the 32 memory cells in a common row. One cell of each four groups of 8 is addressed by the column address decoder. The column address consists of a sense circuit which determines the logic level on the addressed column line. The programming of the memory cell requires shorting the emitter-base junction. A non-programmed memory cell produces a high logic level on the respective column line and a programmed cell produces a low logic level. Figure 2-5 shows the schematic circuit for the memory cells. Photo 2-11 shows that memory cells Q1, Q4, Q5 and Q8 are programmed low. The emitter-base junctions for these cells have been shorted.

The collectors for the remaining unaddressed row transistors are high and therefore these cells have no influence on the state of the addressed row cells. The logic function for the memory cells is shown in Figure 2-6.

The column address inverters include a larger number of devices than the row address inverters. Photo 2-15 is a voltage contrast micrograph for the A7 column address inverters. A7 (pin 15) is the only active address (0.7 Hz) in this photo. The SEI and EBIC micrographs are Photos 2-16 and 2-17. These photos include both the A5 and A6 address inverters. The EBIC response is similar to that obtained for the row address inverters. The emitter, base and collector diffusions are clearly shown for Q3, Q4, Q6, and Q7. The light photograph of this circuit is shown in Photo 2-18. The column address provides two separate functions. The primary function is addressing the memory to read the programmed data. The secondary function is a one time function. This function is to provide the address coding for programming the device. The majority of the memory program circuitry is separate from the read circuitry. Figure 2-7 is the schematic circuit for the column address inverter. The first two inverter stages provide the two phase read memory address code and the third inverter stage provides one phase of write memory address code. This third inverter stage serves no purpose after the memory has been programmed. The first two inverter stages employ dual emitter and dual collector schottky transistors to increase switching speed. When Q3 is conducting the collector current of Q2 is

shared between the base and collector circuit of Q3. This increases the switching speed over the basic schottky clamped transistor. The logic diagram for the column address circuit is shown in Figure 2-8. This is a three stage inverter circuit.

The column read address is decoded by the 1 of 8 column decoder. This circuit is shown in Photo 2-19 which is a voltage contrast micrograph. In this micrograph, address A5 is being cycled at 0.7 Hz. The column decode circuit serves as a combination decoder/sense amplifier. The SEI and EBIC micrographs are Photos 2-20 and 2-21. There was no EBIC response from the decode diodes although the sense amplifier cells were visible. The light photograph is shown in Photo 2-22. The schematic for this circuit is described in Figure 2-9. The sense amplifier consists of D1, R1 and Q1. Diodes D2, D3 and D4 provide a three input AND gate decoder. If any one of the three inputs are low, the respective sense amplifier is inhibited. With all three inputs high, the sense amplifier is active. When the respective memory cell is programmed low, (shorted E-B), the sense transistor is off, and when the memory is programmed high, the sense transistor is on. All eight sense transistors provide an emitter follower summing junction common to the base of Q9. The only condition which results in sense transistor conduction is all decode diode inputs high and memory cell data bit high. The one of eight decoder and sense amplifier represents one of four identical circuits which interface with each of four output data buffers. The logic diagram for this circuit is shown in Figure 2-10. This is a four input AND gate with the memory sense being one of these inputs.

The programmed data read by the sense amplifiers drives the respective output data buffers. The voltage contrast micrograph for the output data buffer Q0 (pin 12) is shown in Photo 2-23. The voltage contrast candy stripe was obtained by alternating (0.7 Hz) between addresses 214 and 246. Address 214 has been programmed to produce a low state at output Q0 and address 246 is programmed high. The SEI and EBIC micrographs are Photos 2-24 and 2-25. These micrographs show output data buffer D2. The EBIC response locates the emitter, base and collector diffusions for Q2 and Q3. No response was visible for the Q1 diffusions. The light photograph for the output data buffer is shown in Photo 2-26. The circuit schematic is described in Figure 2-11. The output transistor collector is uncommitted. The output circuit is a simple inverter with a chip enable inhibit. The logic level programmed in a memory cell is inverted as it appears at the data output terminal. This signal inversion occurs in the output buffer circuit. The logic function is shown in Figure 2-12.

The metallization stripe which exits the lower corner of pin 12 bond pad, reference Photo 2-23, connects with the memory program driver. The memory programming circuit contains a column decode circuit which is independent of the memory read decode circuitry. The programming pulse characteristics specified by the supplier, state the programming pulse must conform to the following;

Pulse Characteristics	Limits
Amplitude	200 mA ± 5%
Clamp Voltage	28.0V + 0%, -2%
Ramp Rate (dv/dt)	70V/ms max
Pulse Width (15V Points)	7.5ms ± 5%
Duty Cycle	70% min.

Initial evaluation of the memory programming circuits did not recognize the significance of the program pulse requirements with respect to turning "on" the memory program driver. During initial evaluation the programming pulse was limited to 12 volts to prevent altering of the memory program. Voltage contrast examination of the memory program column decoder and driver circuit showed the driver circuit was unresponsive. It was first thought that the driver would respond but the program pulse amplitude would not be capable of memory alteration. This was incorrect. Therefore, to understand the operation of the driver circuit, it was examined by light microscopy. This examination for determining the schematic for the driver circuit was only partially successful. The light photograph is shown in Photo 2-27. The configuration of the driver transistors was difficult to identify because of the unusual diffusion geometries. This required mechanical probing of these diffusions to verify the transistor arrangement. The circuit schematic was developed from a combination of voltage contrast, light microscopy and electrical probe data. The circuit schematic is described in Figure 2-13. As shown by the circuit schematic when all column decode diode cathodes are high, there is no drive provided for the program driver transistor Q1. An evaluation of this circuit and the program pulse requirements indicated Q1 transistor is turned on by the program pulse. The program pulse amplitude would exceed the collector emitter sustained breakdown voltage and thereby provide the drive for Q2 and Q3. Electrical probe data verified the BVCEO is in the area of 20 volts and BVCBO is 35 volts. A voltage clamp circuit was also identified which is connected to the collectors. A voltage contrast micrograph was taken using a program pulse amplitude of 20 volts and is shown in Photo 2-28. This micrograph verifies the program pulse is applied to the addressed memory location at a pulse amplitude of 20 volts or greater. The 20 volt pulse can be seen superimposed on the 5 volt level along the second level metal stripe which connects with the common collector tub. The 5 volt level is supplied by the column read decode/sense amplifier circuit through the driver transistor E-B resistor and B-C junction. If the memory cell has been programmed (E-B shorted) a 5 volt level is not present on that column line. Photo 2-28 shows four E-B diffusions have 5 volts applied and four do not. Photo 2-28 was made while rows 1 and 2 were being addressed (row addresses 00000 and 00001) at one frequency (0.3 Hz) and the program driver was being driven at twice this frequency (0.7 Hz). Therefore, the program driver stripe width is half the row address stripe width. Rows 1 and 2 are immediately adjacent to the program driver Q3 transistors.

The program column decode circuit is similar to the read column decode circuit. Two basic differences are the Q1 base pull-up resistor is omitted and there is no memory sense line. The program column address code is provided through the column address inverters as is shown in Figure 2-7. The inverse

A_x ($\overline{A_x}$) code is generated by an inverter located adjacent to the column address inverters. The complement is generated by a single transistor stage located adjacent to the program column decoder. This single transistor does not have a collector pull-up resistor. The collector is interconnected with the appropriate decode diodes and supplies a high (off) or low (on) state. The operation of this circuit could not be observed by voltage contrast because the collector always has zero potential.

Diode D4 is one of four diodes per driver transistor tub which interconnects with the related data output terminal. This provides the path for the memory program pulse. The 28 volt program pulse is applied to the common collector tub for all eight driver circuits. The driver circuit having all three decode diodes high, goes into sustained breakdown which drives the other two transistors into conduction. This applies the program pulse across the addressed memory cell. The applied voltage breaks down the emitter-base junction of the memory cell. This junction is repeatedly pulsed into breakdown until a shorted junction is sensed at the program pulse (data output) terminal. The sense parameters for a programmed cell (shorted junction) are a maximum of 7 volts at a forced current of 20mA. This constant current supply is voltage clamped at 28 volts. The logic diagram which depicts the memory program circuit is shown in Figure 2-14. Memory programming is performed with the chip enable inputs at a high logic state. The most apparent function of the chip enable circuit is inhibiting the output data stage. This circuit will be described later.

There are two additional circuits common to the chip enable circuits that are not apparent to the application engineer. These circuits have been included to provide the device manufacturer with additional functional test capability. One of these circuit functions was mentioned earlier. This was the program voltage clamp which connects to the memory program driver collectors. The other circuit is a master disable for row decoders 1 through 32. These two circuits presented a challenge in developing the schematic and identifying their purpose. For example, these two circuits are controlled by an abnormal chip enable input signal. The circuit schematic was initially developed using light photographs. The circuit configuration and operation were verified by voltage contrast micrographs. Voltage contrast observation of circuit operation was not possible initially because the stimulus requirements were not known. These two circuits are physically located in different areas of the chip. The voltage contrast micrograph for the master row decoder disable circuit is Photo 2-29 and the light photograph is Photo 2-30. The voltage contrast photo was taken with a 6.0 volt 0.7 Hz square wave applied to CE1 (pin 13). The micrograph and photograph for the memory program voltage clamp circuits are Photos 2-31 and 2-32. Figure 2-15 describes the electrical schematic for these circuits. The two circuits are controlled by applying a 6 volt or greater signal level to one or both of the chip enable inputs (pins 13 and 14).

The row decoder disable output has a common input connection to all 32 decoders. A chip enable input greater than 6 volts produces a low state at Q3 collector which is connected to each of the 32 row decoders. This inhibits the 1-32 row addressing. This same chip enable input disables the memory

program clamp circuit. This circuit is active under normal chip operation. It provides a 14 volt time delayed clamp for the memory program drivers. This limits the program pulse amplitude after the time delay which is required to reach the voltage breakdown (pulse propagation from program driver to clamp circuit plus clamp circuit response time). The application or value of these circuits is not appreciated. They are obviously intended for special testing by the manufacturer. Disabling the 32 row decoders would force the memory cells to a high state. The memory cells produce a high state in the non-programmed state, therefore, no change in state would be observed at the output. The logic diagram for the test circuit disable is shown in Figure 2-16.

A third test circuit was identified. This circuit included an address inverter and a special row of memory. Row 33 contains 16 mask programmed cells and 16 standard open base transistor cells. A part of row 33 is the left row shown in Photo 2-14. This circuit was first recognized while observing sequential memory addressing on the SEM. Further examination showed this was an extra row and was not addressed during the normal address sequence cycle. The row decode circuit was examined to identify the coding required to address this row. The address lines were traced to locate the circuit and signal input. The input was common with row address input A4. This indicated that a special code is required to access row 33. Examination of the input circuit showed the input transistor base was isolated from A4 input by a reverse biased emitter-base junction. To address row 33 requires the normal address code for row 32 (A0 - A4 high) and A4 signal level greater than 7 volts. The circuit operation was verified by voltage contrast. The voltage contrast micrograph was taken with A4 input cycling between 0 and 7 volts at 0.7 Hz. This micrograph is shown in Photo 2-33 and the light photograph is Photo 2-34. The circuit schematic is described in Figure 2-17 and the logic diagram is shown in Figure 2-18. This circuit provides the capability for functional testing non-programmed devices. Without this capability, only the chip enable function and parameter testing would be possible. With the addition of the row 33 test circuit, all functional blocks of this device can be verified functionally with exception of the row address and row decoder functions. Without this capability, it is estimated that 90% of the circuit would be untested when delivered non-programmed. Functional failures would not be detected and such failures are generally at the buyers expense.

The chip enable circuit is the last circuit evaluated for this chip. This circuit provides a data output inhibit when one or both of the chip enable inputs is high. This allows multiplexing paralleled devices where the chip addressing is supplied from a common source and the active output is determined by chip enable coding. The voltage contrast micrograph shows the circuit response in Photo 2-35. A zero to 5 volt 0.7 Hz square wave is applied to the CE2 input (pin 14) in this photo. The SEI and EBIC micrographs are Photos 2-36 and 2-37. This EBIC photo pro ides clear identification of the D1, D2, Q3, Q4 and Q5 diffusions. Very lim ted EBIC responses were obtained from Q1 and Q2. The light photograph of the chip enable circuit is Photo 2-38 and the circuit schematic is described in Figure 2-19. The CE1 and CE2 inputs are pins 13 and 14 and the chip enable output connects with the chip

enable input on each data output stage. Figure 2-20 contains the logic diagram for the chip enable circuit.

The chip organization is shown in Photo 2-39. This chip contains a larger number of functional blocks than would be expected from the vendors data sheet. A block diagram for this chip is shown in Figure 2-21. Memory program circuitry has been separated from read circuitry to reduce exposure to stress during programming. High voltage/high current programming pulses are carried through separate conductors. The die dimensions are 85 x 120 mils. The chip metallization and wire bonds are aluminum. The metallization is primarily single level with a limited amount of second level and the majority of the second level metallization is common to the program circuits. The separate program circuits/metallization is for maintaining the reliability of the primary ROM performance.

The EBIC response was evaluated and documented for the complete chip. Photos 2-40, 2-41, and 2-42 are the overall chip SEI and EBIC photos. These EBIC photos were taken at 10 kv and 15 kv respectively to show the significance of beam acceleration voltage on the EBIC response. Both photos were taken with V_{CC} (pin 16) connected to the SCA and GND (pin 3) connected to ground. The die was initially evaluated using a beam voltage of 10 kv. The 10kv response was somewhat limited to the peripheral circuitry. No response was visible from the memory cells and a limited response was obtained from the two column decoders. The beam voltage was increased to 15 kv and the EBIC response is shown in Photo 2-42. The 15 kv beam produced a significant increase in the chip response. The 5 kv increase has easily doubled the circuit EBIC response. This is consistant with the results obtained from the individual EBIC images for the functional blocks.

A bit map was generated for this chip. Developing a bit map is a simple task when using voltage contrast and a sequential address routine. The bit map provides the ability to determine the memory bit location for any address. This is beneficial for developing test patterns for evaluating crosstalk or pattern sensitivity and locating decode circuits and memory cells for failure analysis. The bit map for this circuit is identified in Figure 2-22.

The memory programming and special test circuits presented the greatest challenge in defining the electrical schematics for the chip functions. The operation and purpose of the anticipated circuits are straightforward and obvious. Before voltage contrast examination was successful for the memory program and special test circuits, it was first necessary to determine how the circuit operated and what stimuli were required to effect operation.

Failure Analysis

To demonstrate the feasibility and practicality of using the SEM in failure isolation a failure was intentionally introduced in a tested good device. The best test for demonstrating this application of the SEM would be in using actual failures as examples. This was not practical because functionally failed devices were not available. Therefore, the approach used was that

a failure was induced by one analyst and testing and SEM isolation was performed by another analyst.

The device used was S/N 3 which had been parametrically and functionally tested and verified good. A failure was induced in this device and given to an analyst for testing and evaluation.

Functional testing of the part showed ouput data errors on all four outputs. The error occurred only when address A2 was low and the output data error was always high. When address A2 was high, output one was always high. The functional tests showed the remaining data was correct for all other addressed combinations including address A2 high. Parameters I_{IH} and I_{IL} for input A2 remained below the maximum specified limits. A speculation was made at this time that the cause of failure was the in-phase A2 address inverter output is staying low. If this condition does exist, no memory rows would be addressed when the A2 address input is low.

The device was placed in the SEM and examined in the voltage contrast mode. With address A2 forced high, address A0 was cycled at 0.7 Hz. The circuit was observed to function properly as shown in Photo 2-43. Address A2 was then forced low with address A0 cycling (addresses 0 and 1). This showed that two memory rows were being addressed simultaneously. This is shown in Photo 2-44. Examination of address A2 inverters showed address line A2 was switching properly but address line A2 stayed high. This is shown in Photo 2-45. The cause of the failure was an open base connection on transistor Q5. Reference the schematic in Figure 2-23.

The reason data output 1 was always high when address A2 input was low, is the programmed data format. In reviewing the format it can be seen that when A2 is low the programmed data sequence becomes the compliment of when A2 is hign. Because two rows are addressed when A2 input is low, two rows are read by the sense amplifier. When two rows are connected simultaneously the programmed memory cell low state dominates. The complimentary program always provided a low state to the sense amplifier. The data output buffer inverts the signal from the sense amplifiers which produced a constant high on data output 1.

The failure which occurred in this device was not the first failure attempted. The first failure attempted was to place the emitter-base junction of Q5 into deep reverse breakdown, using mechanical probes and curve tracer, to degrade the transistor beta. This was not possible because parallel paths prevented reaching the point of reverse breakdown. The second approach used was charging a 180 Pfd capacitor in increments of 25 volts and discharging this energy across the emitter-base junction. Following each discharge the beta was checked for degradation. No degradation occurred until the capacitor charge reached 400 volts. No series current limiting resistor was used. Following the 400 volt discharge the emitter-base junction measured short. Even though this junction was shorted the circuit remained functional. This is due primarily to Q5 and Q6 being connected in a darlington configuration. However, it is expected that the loss of the Q5 driver would affect the switching speed and also the beta margin over the

operating temperature range. During subsequent probing and testing the Q5 base connection was inadvertently opened which produced the failure isolated and identified by voltage contrast. An EBIC micrograph was taken to show the discharge damage site between the emitter and base. The EBIC image is shown in Photo 2-46. The damage site appears as an extension of the emitter diffusion.

A second failure was induced and the device was given to an analyst for testing and evaluation. Functional testing showed output data errors on data output 0. The output remained high for all addresses where A5 was low, A6 was high and A7 was low. There were a total of 16 data errors. In reviewing the programmed data listing (ref Table 2-I) it was determined that the errors occurred between addresses 66 and 93. Because outputs 2, 3, and 4 are programmed high for these same addresses it could not be determined if they were also involved with this failure.

The device was placed in the SEM for voltage contrast isolation. The address inputs were cycled at 0.7 Hz between addresses 69 and 70. This required address A0 be cycled high and low. While cycling the active rows 6 and 7 were examined. This showed that the column 2 line for output 0 was cycling high and low. This line was followed across to the column 2 sense circuit and the failure site was located. The failure was caused by an open metallization stripe on the anode side of diode D3 in the column decode and sense amplifier (ref Figure 2-9). The failure site is shown in Photo 2-47. This photo shows the address 69 data bit zero and address 70 data bit one. This same data is present on all eight column sense lines common to output 0. Because the column decode lines for the remaining seven decoders have at least one decode line low, the sense amplifiers do not respond to this data. Only the decode diode cathodes for column 3 are all high. However, the low state for address 69 does not reach the base of Q3 and Q3 is turned on. This results in a high level at output 0. This open metal failure would produce an error at output 0 for all addresses from 64 to 95 which are programmed low. This is verified by the bit map in Figure 2-22. It would have no effect on the remaining 3 outputs.

This is the failure which had been intentionally introduced into the circuit. The chip had been masked using TEK wax and the stripe had been exposed to aluminum etchant to create this open.

TABLE 2-I PROGRAMMED DATA LISTING

INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q3	2	1	0	INPUT A7	6	5	4	3	2	1	0	ADDR	OUTPUT Q3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	32	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	0	1	33	1	1	1	1
0	0	0	0	0	0	1	0	2	1	1	1	1	0	0	1	0	0	0	1	0	34	1	1	1	0
0	0	0	0	0	0	1	1	3	1	1	1	1	0	0	1	0	0	0	1	1	35	1	1	1	0
0	0	0	0	0	1	0	0	4	1	1	1	1	0	0	1	0	0	1	0	0	36	1	1	1	0
0	0	0	0	0	1	0	1	5	1	1	1	1	0	0	1	0	0	1	0	1	37	1	1	1	0
0	0	0	0	0	1	1	0	6	1	1	1	0	0	0	1	0	0	1	1	0	38	1	1	1	1
0	0	0	0	0	1	1	1	7	1	1	1	0	0	0	1	0	0	1	1	1	39	1	1	1	1
0	0	0	0	1	0	0	0	8	1	1	1	1	0	0	1	0	1	0	0	0	40	1	1	1	0
0	0	0	0	1	0	0	1	9	1	1	1	1	0	0	1	0	1	0	0	1	41	1	1	1	0
0	0	0	0	1	0	1	0	10	1	1	1	0	0	0	1	0	1	0	1	0	42	1	1	1	1
0	0	0	0	1	0	1	1	11	1	1	1	0	0	0	1	0	1	0	1	1	43	1	1	1	1
0	0	0	0	1	1	0	0	12	1	1	1	0	0	0	1	0	1	1	0	0	44	1	1	1	1
0	0	0	0	1	1	0	1	13	1	1	1	0	0	0	1	0	1	1	0	1	45	1	1	1	1
0	0	0	0	1	1	1	0	14	1	1	1	1	0	0	1	0	1	1	1	0	46	1	1	1	0
0	0	0	0	1	1	1	1	15	1	1	1	1	0	0	1	0	1	1	1	1	47	1	1	1	0
0	0	0	1	0	0	0	0	16	1	1	1	1	0	0	1	1	0	0	0	0	48	1	1	1	0
0	0	0	1	0	0	0	1	17	1	1	1	1	0	0	1	1	0	0	0	1	49	1	1	1	0
0	0	0	1	0	0	1	0	18	1	1	1	0	0	0	1	1	0	0	1	0	50	0	0	1	1
0	0	0	1	0	0	1	1	19	1	1	1	0	0	0	1	1	0	0	1	1	51	1	1	1	1
0	0	0	1	0	1	0	0	20	1	1	1	0	0	0	1	1	0	1	0	0	52	0	1	1	1
0	0	0	1	0	1	0	1	21	1	1	1	0	0	0	1	1	0	1	0	1	53	1	1	1	1
0	0	0	1	0	1	1	0	22	1	1	1	1	0	0	1	1	0	1	1	0	54	1	1	1	0
0	0	0	1	0	1	1	1	23	1	1	1	1	0	0	1	1	0	1	1	1	55	1	1	1	0
0	0	0	1	1	0	0	0	24	1	1	1	0	0	0	1	1	1	0	0	0	56	1	1	1	1
0	0	0	1	1	0	0	1	25	1	1	1	0	0	0	1	1	1	0	0	1	57	1	1	1	1
0	0	0	1	1	0	1	0	26	1	1	1	1	0	0	1	1	1	0	1	0	58	1	1	1	0
0	0	0	1	1	0	1	1	27	1	1	1	1	0	0	1	1	1	0	1	1	59	1	1	1	0
0	0	0	1	1	1	0	0	28	1	1	1	1	0	0	1	1	1	1	0	0	60	1	1	1	0
0	0	0	1	1	1	0	1	29	1	1	1	1	0	0	1	1	1	1	0	1	61	1	1	1	0
0	0	0	1	1	1	1	0	30	1	1	1	0	0	0	1	1	1	1	1	0	62	1	1	1	1
0	0	0	1	1	1	1	1	31	1	1	1	0	0	0	1	1	1	1	1	1	63	1	1	1	1
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

1 = High-Level Output Voltage 0 = Low-Level Output Voltage

TABLE 2-I (cont)

INPUT									OUTPUT					INPUT									OUTPUT			
A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0		A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0
0	1	0	0	0	0	0	0	64	1	1	1	1		0	1	1	0	0	0	0	0	96	1	1	1	0
0	1	0	0	0	0	0	1	65	1	1	1	1		0	1	1	0	0	0	0	1	97	1	1	1	0
0	1	0	0	0	0	1	0	66	1	1	1	0		0	1	1	0	0	0	1	0	98	1	0	1	1
0	1	0	0	0	0	1	1	67	1	1	1	0		0	1	1	0	0	0	1	1	99	1	1	1	1
0	1	0	0	0	1	0	0	68	1	1	1	0		0	1	1	0	0	1	0	0	100	1	0	0	1
0	1	0	0	0	1	0	1	69	1	1	1	0		0	1	1	0	0	1	0	1	101	1	1	1	1
0	1	0	0	0	1	1	0	70	1	1	1	1		0	1	1	0	0	1	1	0	102	1	1	1	0
0	1	0	0	0	1	1	1	71	1	1	1	1		0	1	1	0	0	1	1	1	103	1	1	1	0
0	1	0	0	1	0	0	0	72	1	1	1	0		0	1	1	0	1	0	0	0	104	1	1	1	1
0	1	0	0	1	0	0	1	73	1	1	1	0		0	1	1	0	1	0	0	1	105	1	1	1	1
0	1	0	0	1	0	1	0	74	1	1	1	1		0	1	1	0	1	0	1	0	106	1	1	1	0
0	1	0	0	1	0	1	1	75	1	1	1	1		0	1	1	0	1	0	1	1	107	1	1	1	0
0	1	0	0	1	1	0	0	76	1	1	1	1		0	1	1	0	1	1	0	0	108	1	1	1	0
0	1	0	0	1	1	0	1	77	1	1	1	1		0	1	1	0	1	1	0	1	109	1	1	1	0
0	1	0	0	1	1	1	0	78	1	1	1	0		0	1	1	0	1	1	1	0	110	1	1	1	1
0	1	0	0	1	1	1	1	79	1	1	1	0		0	1	1	0	1	1	1	1	111	1	1	1	1
0	1	0	1	0	0	0	0	80	1	1	1	0		0	1	1	1	0	0	0	0	112	0	1	0	1
0	1	0	1	0	0	0	1	81	1	1	1	0		0	1	1	1	0	0	0	1	113	1	1	1	1
0	1	0	1	0	0	1	0	82	1	1	1	1		0	1	1	1	0	0	1	0	114	1	1	1	0
0	1	0	1	0	0	1	1	83	1	1	1	1		0	1	1	1	0	0	1	1	115	1	1	1	0
0	1	0	1	0	1	0	0	84	1	1	1	1		0	1	1	1	0	1	0	0	116	1	1	1	0
0	1	0	1	0	1	0	1	85	1	1	1	1		0	1	1	1	0	1	0	1	117	1	1	1	0
0	1	0	1	0	1	1	0	86	1	1	1	0		0	1	1	1	0	1	1	0	118	0	0	0	1
0	1	0	1	0	1	1	1	87	1	1	1	0		0	1	1	1	0	1	1	1	119	1	1	1	1
0	1	0	1	1	0	0	0	88	1	1	1	1		0	1	1	1	1	0	0	0	120	1	1	1	0
0	1	0	1	1	0	0	1	89	1	1	1	1		0	1	1	1	1	0	0	1	121	1	1	1	0
0	1	0	1	1	0	1	0	90	1	1	1	0		0	1	1	1	1	0	1	0	122	1	1	0	1
0	1	0	1	1	0	1	1	91	1	1	1	0		0	1	1	1	1	0	1	1	123	1	1	1	1
0	1	0	1	1	1	0	0	92	1	1	1	0		0	1	1	1	1	1	0	0	124	1	1	1	1
0	1	0	1	1	1	0	1	93	1	1	1	0		0	1	1	1	1	1	0	1	125	1	1	1	1
0	1	0	1	1	1	1	0	94	1	1	1	1		0	1	1	1	1	1	1	0	126	1	1	1	0
0	1	0	1	1	1	1	1	95	1	1	1	1		0	1	1	1	1	1	1	1	127	1	1	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12		15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

1 = High-Level Output Voltage 0 = Low-Level Output Voltage

TABLE 2-I (cont)

INPUT									OUTPUT				INPUT									OUTPUT			
A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0	A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0
1	0	0	0	0	0	0	0	128	1	1	1	0	1	0	1	0	0	0	0	0	160	1	1	1	1
1	0	0	0	0	0	0	1	129	1	1	1	0	1	0	1	0	0	0	0	1	161	1	1	1	1
1	0	0	0	0	0	1	0	130	1	1	1	1	1	0	1	0	0	0	1	0	162	1	1	1	0
1	0	0	0	0	0	1	1	131	1	1	1	1	1	0	1	0	0	0	1	1	163	1	1	1	0
1	0	0	0	0	1	0	0	132	1	1	1	1	1	0	1	0	0	1	0	0	164	1	1	1	0
1	0	0	0	0	1	0	1	133	1	1	1	1	1	0	1	0	0	1	0	1	165	1	1	1	0
1	0	0	0	0	1	1	0	134	1	1	1	0	1	0	1	0	0	1	1	0	166	1	1	1	1
1	0	0	0	0	1	1	1	135	1	1	1	0	1	0	1	0	0	1	1	1	167	1	1	1	1
1	0	0	0	1	0	0	0	136	1	1	1	1	1	0	1	0	1	0	0	0	168	1	1	1	0
1	0	0	0	1	0	0	1	137	1	1	1	1	1	0	1	0	1	0	0	1	169	1	1	1	0
1	0	0	0	1	0	1	0	138	1	1	1	0	1	0	1	0	1	0	1	0	170	1	1	1	1
1	0	0	0	1	0	1	1	139	1	1	1	0	1	0	1	0	1	0	1	1	171	1	1	1	1
1	0	0	0	1	1	0	0	140	1	1	1	0	1	0	1	0	1	1	0	0	172	1	1	1	1
1	0	0	0	1	1	0	1	141	1	1	1	0	1	0	1	0	1	1	0	1	173	1	1	1	1
1	0	0	0	1	1	1	0	142	1	1	1	1	1	0	1	0	1	1	1	0	174	1	1	1	0
1	0	0	0	1	1	1	1	143	1	1	1	1	1	0	1	0	1	1	1	1	175	1	1	1	0
1	0	0	1	0	0	0	0	144	1	1	1	1	1	0	1	1	0	0	0	0	176	1	1	1	0
1	0	0	1	0	0	0	1	145	1	1	1	1	1	0	1	1	0	0	0	1	177	1	1	1	0
1	0	0	1	0	0	1	0	146	1	1	1	0	1	0	1	1	0	0	1	0	178	1	1	1	1
1	0	0	1	0	0	1	1	147	1	1	1	0	1	0	1	1	0	0	1	1	179	1	1	1	1
1	0	0	1	0	1	0	0	148	1	1	1	0	1	0	1	1	0	1	0	0	180	1	1	1	1
1	0	0	1	0	1	0	1	149	1	1	1	0	1	0	1	1	0	1	0	1	181	1	1	1	1
1	0	0	1	0	1	1	0	150	1	1	1	1	1	0	1	1	0	1	1	0	182	1	1	1	0
1	0	0	1	0	1	1	1	151	1	1	1	1	1	0	1	1	0	1	1	1	183	1	1	1	0
1	0	0	1	1	0	0	0	152	1	1	1	0	1	0	1	1	1	0	0	0	184	1	1	1	1
1	0	0	1	1	0	0	1	153	1	1	1	0	1	0	1	1	1	0	0	1	185	1	1	1	1
1	0	0	1	1	0	1	0	154	1	1	1	1	1	0	1	1	1	0	1	0	186	1	1	1	0
1	0	0	1	1	0	1	1	155	1	1	1	1	1	0	1	1	1	0	1	1	187	1	1	1	0
1	0	0	1	1	1	0	0	156	1	1	1	1	1	0	1	1	1	1	0	0	188	1	1	1	0
1	0	0	1	1	1	0	1	157	1	1	1	1	1	0	1	1	1	1	0	1	189	1	1	1	0
1	0	0	1	1	1	1	0	158	1	1	1	0	1	0	1	1	1	1	1	0	190	1	1	1	1
1	0	0	1	1	1	1	1	159	1	1	1	0	1	0	1	1	1	1	1	1	191	1	1	1	1
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

1 = High-Level Output Voltage 0 = Low-Level Output Voltage

TABLE 2-I (concl)

INPUT									OUTPUT				INPUT									OUTPUT			
A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0	A7	6	5	4	3	2	1	0	ADDR	Q3	2	1	0
1	1	0	0	0	0	0	0	192	1	1	1	1	1	1	1	0	0	0	0	0	224	1	1	1	0
1	1	0	0	0	0	0	1	193	1	1	1	1	1	1	1	0	0	0	0	1	225	1	1	1	0
1	1	0	0	0	0	1	0	194	1	1	1	0	1	1	1	0	0	0	1	0	226	1	0	1	1
1	1	0	0	0	0	1	1	195	1	1	1	0	1	1	1	0	0	0	1	1	227	1	1	1	1
1	1	0	0	0	1	0	0	196	1	1	1	0	1	1	1	0	0	1	0	0	228	1	0	0	1
1	1	0	0	0	1	0	1	197	1	1	1	0	1	1	1	0	0	1	0	1	229	1	1	1	1
1	1	0	0	0	1	1	0	198	1	1	1	1	1	1	1	0	0	1	1	0	230	1	1	1	0
1	1	0	0	0	1	1	1	199	1	1	1	1	1	1	1	0	0	1	1	1	231	1	1	1	0
1	1	0	0	1	0	0	0	200	1	1	1	0	1	1	1	0	1	0	0	0	232	1	1	1	1
1	1	0	0	1	0	0	1	201	1	1	1	0	1	1	1	0	1	0	0	1	233	1	1	1	1
1	1	0	0	1	0	1	0	202	1	1	1	1	1	1	1	0	1	0	1	0	234	1	1	1	0
1	1	0	0	1	0	1	1	203	1	1	1	1	1	1	1	0	1	0	1	1	235	1	1	1	0
1	1	0	0	1	1	0	0	204	1	1	1	1	1	1	1	0	1	1	0	0	236	1	1	1	0
1	1	0	0	1	1	0	1	205	1	1	1	1	1	1	1	0	1	1	0	1	237	1	1	1	0
1	1	0	0	1	1	1	0	206	1	1	1	0	1	1	1	0	1	1	1	0	238	1	1	1	1
1	1	0	0	1	1	1	1	207	1	1	1	0	1	1	1	0	1	1	1	1	239	1	1	1	1
1	1	0	1	0	0	0	0	208	1	1	1	0	1	1	1	1	0	0	0	0	240	1	1	1	1
1	1	0	1	0	0	0	1	209	1	1	1	0	1	1	1	1	0	0	0	1	241	1	1	1	1
1	1	0	1	0	0	1	0	210	1	1	1	1	1	1	1	1	0	0	1	0	242	1	1	1	0
1	1	0	1	0	0	1	1	211	1	1	1	1	1	1	1	1	0	0	1	1	243	1	1	1	0
1	1	0	1	0	1	0	0	212	1	1	1	1	1	1	1	1	0	1	0	0	244	1	1	1	0
1	1	0	1	0	1	0	1	213	1	1	1	1	1	1	1	1	0	1	0	1	245	1	1	1	0
1	1	0	1	0	1	1	0	214	1	1	1	0	1	1	1	1	0	1	1	0	246	0	0	0	1
1	1	0	1	0	1	1	1	215	1	1	1	0	1	1	1	1	0	1	1	1	247	1	1	1	1
1	1	0	1	1	0	0	0	216	1	1	1	1	1	1	1	1	1	0	0	0	248	1	1	1	0
1	1	0	1	1	0	0	1	217	1	1	1	1	1	1	1	1	1	0	0	1	249	1	1	1	0
1	1	0	1	1	0	1	0	218	1	1	1	0	1	1	1	1	1	0	1	0	250	1	1	0	1
1	1	0	1	1	0	1	1	219	1	1	1	0	1	1	1	1	1	0	1	1	251	1	1	1	1
1	1	0	1	1	1	0	0	220	1	1	1	0	1	1	1	1	1	1	0	0	252	1	1	1	1
1	1	0	1	1	1	0	1	221	1	1	1	0	1	1	1	1	1	1	0	1	253	1	1	1	1
1	1	0	1	1	1	1	0	222	1	1	1	1	1	1	1	1	1	1	1	0	254	1	1	1	0
1	1	0	1	1	1	1	1	223	1	1	1	1	1	1	1	1	1	1	1	1	255	1	1	1	0
15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12	15	1	2	3	4	7	6	5	PIN NO.	9	10	11	12

1 = High-Level Output Voltage 0 = Low-level Output Voltage

TABLE 2-II DC PARAMETERS

S/N 1 (good)

V_{cc} = 5.0V

Pin	I_{FA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} I_{OL} = 16mA V_{CE} = 0.4V V	I_{OLK} V_O = 5.5V V_{CE} = 0.4V µA	V_{OH} I_O = -0.4mA V_{CE} = 0.4V V	I_{SC} V_O = 0V V_{CE} = 0.4V mA	V_C I_{IN} = 10mA V	BV_{IN} I_{IN} = 1.0mA V
1	-.477		3.7						-.81	6.8
2	-.460		3.7						-.84	7.9
3	-.455		3.6						-.82	8.8
4	-.451		3.6						-.79	7.9
5	-.460		3.3						-.84	6.8
6	-.450		3.2						-.84	6.8
7	-.464		3.4						-.84	6.8
8	GND	GNL	GND	GND	GND	GND	GND	GND		
9					.404	<.1	3.28	-2.73		
10					.360	<.1	3.27	-2.63		
11					.371	<.1	3.28	-2.65		
12					.375	<.1	3.29	-2.65		
13		-.466		4.6		(≤.2)			-.84	9.1
14		-.460		3.5					-.83	9.1
15	-.484		4.9						-.84	6.8
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}		
I_{cc} (mA)					61.6					

TABLE 2-II (cont)

S/N 2 (good)

V_{cc} = 5.0V

PIN	I_{FA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} I_{OL} = 16mA V_{CE} = 0.4V V	I_{OLK} V_O = 5.5V V_{CE} = 0.4V µA	V_{OH} I_O = 0.4mA V_{CE} = 0.4V V	I_{SC} V_O = 0V V_{CE} = 0.4V mA	
1	-.484		3.2						
2	-.477		3.4						
3	-.470		3.3						
4	-.478		3.5						
5	-.476		3.3						
6	-.463		3.2						
7	-.473		3.4						
8	GND	GND	GND	GND	GND	GND	GND	GND	
9					.368	<.1	3.29	-2.71	
10					.322	<.1	3.28	-2.67	
11					.326	<.1	3.28	-2.67	
12					.319	<.1	3.28	-2.66	
13		-.480		4.6		(≤.2)			
14		-.472		3.8					
15	-.480		4.5						
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	
I_{cc} (mA)					61.7				

TABLE 2-II (cont)

S/N 3 (good)

V_{CC} = 5.0V

PIN	I_{EA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} = 16mA I_{OL} V_{CE} = 0.4V V	I_{OLK} V_O = 5.5V µA V_{CE} = 0.4V	V_{OH} = 0.4mA I_O V_{CE} = 0.4V V	I_{SC} V_O = 0V mA V_{CE} = 0.4V	
1	-.416		3.0						
2	-.404		3.1						
3	-.400		2.9						
4	-.383		3.0						
5	-.390		2.7						
6	-.373		2.8						
7	-.403		3.0						
8	GND	GND	GND	GND	GND	GND	GND	GND	
9					.360	<.1	3.24	-2.38	
10					.318	<.1	3.24	-2.36	
11					.323	<.1	3.24	-2.39	
12					.320	<.1	3.25	-2.39	
13		-.397		3.9		(≤.3)			
14		-.392		3.4					
15	-.415		3.9						
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	
I_{cc} (mA)					52.6				

TABLE 2-II (cont)

S/N 4 (good)

V_{cc} = 5.0V

PIN	I_{EA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} I_{OL} = 16mA V_{CE} = 0.4V V	I_{OLK} V_O = 5.5V V_{CE} = 0.4V µA	V_{OH} I_O = -0.4mA V_{CE} = 0.4V V	I_{SC} V_O = 0V V_{CE} = 0.4V mA	
1	-.463		4.2						
2	-.456		4.2						
3	-.451		4.1						
4	-.440		4.2						
5	-.449		4.1						
6	-.442		4.1						
7	-.453		4.3						
8	GND	GND	GND	GND	GND	GND	GND	GND	
9					.358	$<$.1	3.30	-2.64	
10					.314	$<$.1	3.29	-2.57	
11					.315	$<$.1	3.28	-2.56	
12					.311	$<$.1	3.28	-2.55	
13		-.499		5.6		($\leq$.2)			
14		-.445		4.7					
15	-.460		5.8						
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}	
I_{cc} (mA)					59.1				

TABLE 3-II (cont)

S/N 5 (good)

V_{cc} = 5.0V

PIN	I_{FA} V_A = 0.4V	I_{FE} V_{CE} = 0.4V	I_{RA} V_A = 4.5V	I_{RE} V_{CE} = 4.5V	V_{OL} I_{OL} = 16mA V_{CE} = 0.4V	I_{OLK} V_O = 5.5V V_{CE} = 0.4V	V_{OH} I_O = -0.4mA V_{CE} = 0.4V	I_{SC} V_O = 0V V_{CE} 0.4V	
	mA	mA	µA	µA	V	µA	V	mA	
1	-.488		3.0						
2	-.473		2.9						
3	-.469		2.8						
4	-.457		3.0						
5	-.468		2.8						
6	-.452		2.8						
7	-.466		2.9						
8	GND	GND							
9					.376	<.1	3.27	-2.70	
10					.332	<.1	3.27	-2.64	
11					.335	<.1	3.27	-2.67	
12					.335	<.1	3.28	-2.66	
13		.479		4.0		(≤.2)			
14		.475		3.4					
15	498		4.1						
16	V_{cc}	V_{cc}							
I_{cc} (mA)					61.5				

TABLE 2-II (cont)

S/N 10 (failed)

V_{cc} = 5.0V

PIN	I_{EA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} I_{OL} = 16mA V		
1	-.547		3.1				
2	-.543		3.1				
3	-.537		3.0				
4	-.521		3.2				
5	-.523		2.9				
6	-.525		3.1				
7	-.551		3.3				
8	GND	GND					
9					.388		
10					.358		
11					.353		
12					.367		
13		.541		4.1			
14		.523		3.4			
15	.548		4.2				
16	V_{cc}	V_{cc}					
I_{cc} (mA)					71.8		

TABLE 2-II (cont)

S/N 11 (failed)

V_{cc} = 5.0V

PIN	I_{FA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OL} = 16mA I_{OL} V_{CE} = 0.4V V		
1	-.499		4.9				
2	-.498		4.9				
3	-.485		4.7				
4	-.482		4.7				
5	-.478		4.4				
6	-.463		4.4				
7	-.481		4.7				
8	GND	GND	GND	GND			
9					.366		
10					.324		
11					.322		
12					.333		
13		-.485		7.2			
14		-.481		6.1			
15	-.491		6.9				
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}			
I_{cc} (mA)					66.0		

TABLE 2-II (concl)

S/N 12 (failed)

V_{cc} = 5.0V

PIN	I_{FA} V_A = 0.4V mA	I_{FE} V_{CE} = 0.4V mA	I_{RA} V_A = 4.5V µA	I_{RE} V_{CE} = 4.5V µA	V_{OH} = -0.4mA I_O V_{CE} = 0.4V V		
1	-.457		3.4				
2	-.441		3.4				
3	-.429		3.1				
4	-.417		3.2				
5	-.425		2.9				
6	-.411		2.9				
7	-.428		3.0				
8	GND	GND	GND	GND			
9					.345		
10					.304		
11					.307		
12					.314		
13				4.4			
14		.433		3.7			
15	.453	.436	4.5				
16	V_{cc}	V_{cc}	V_{cc}	V_{cc}			
I_{cc} (mA)					58.3		

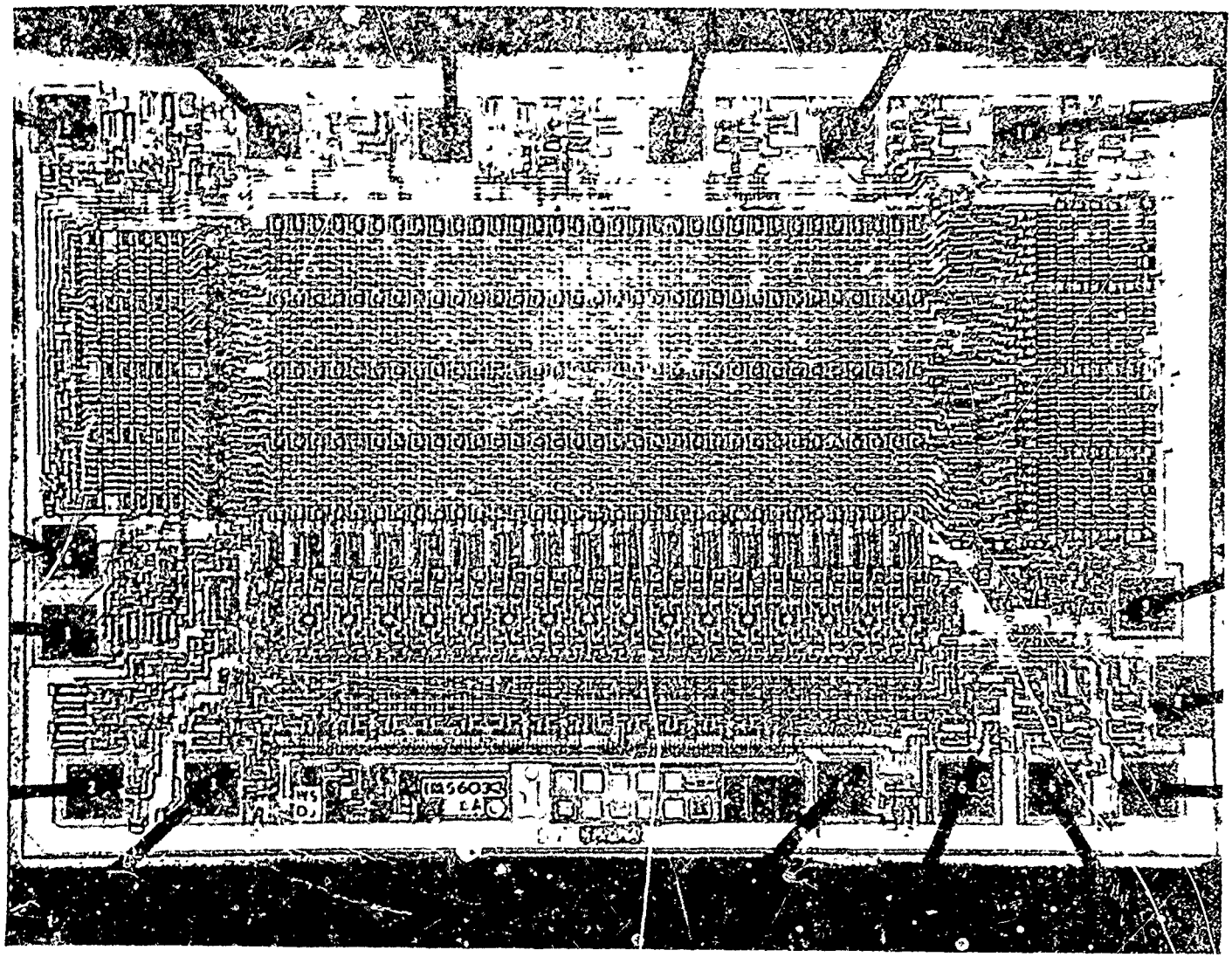


Photo 2-1 The Complete Die. Mag. - 60X

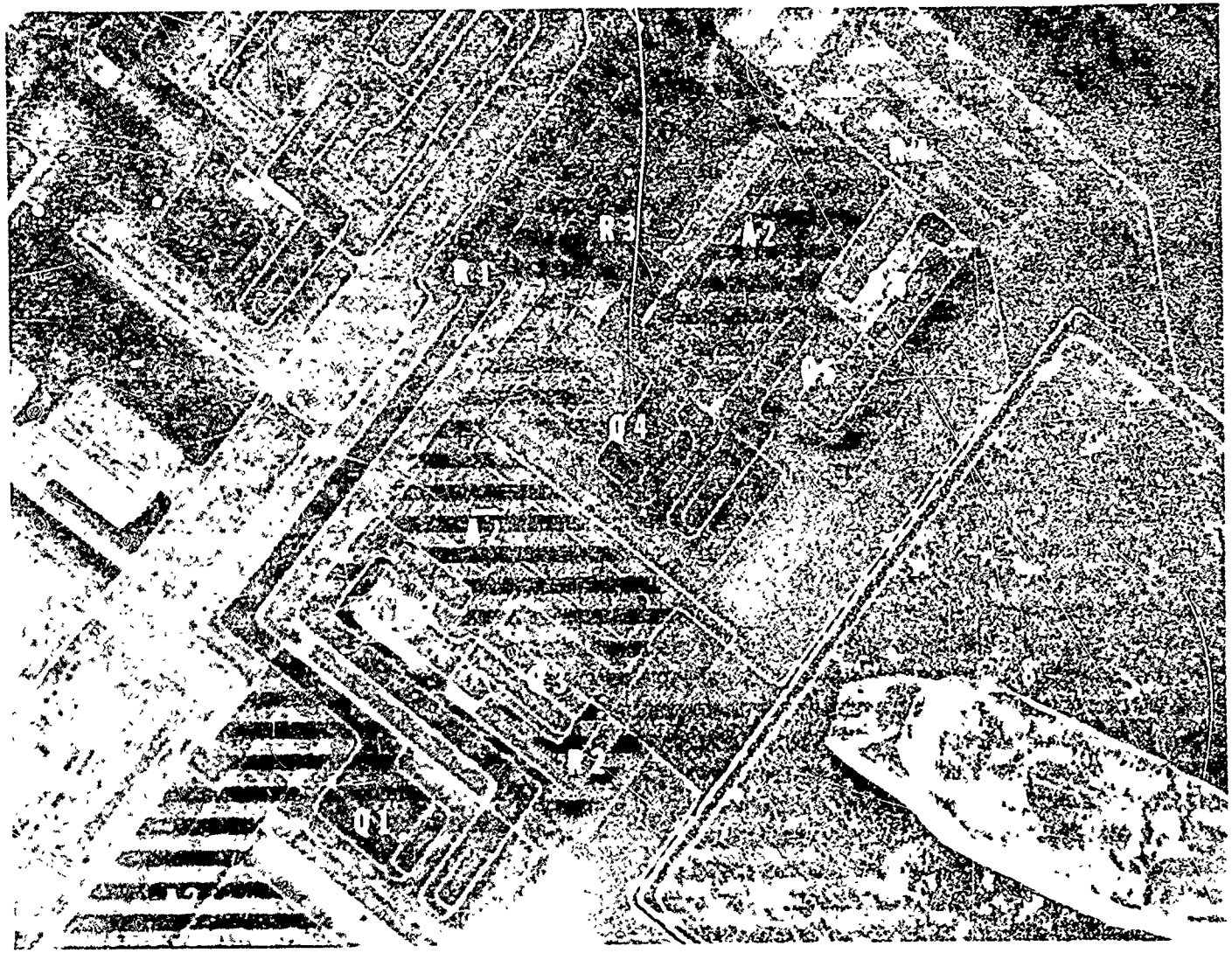


Photo 2-2 Voltage Contrast Micrograph of A2 Row Address Inverter. Input A2, Only, is Going Probed. Mag. - 620X

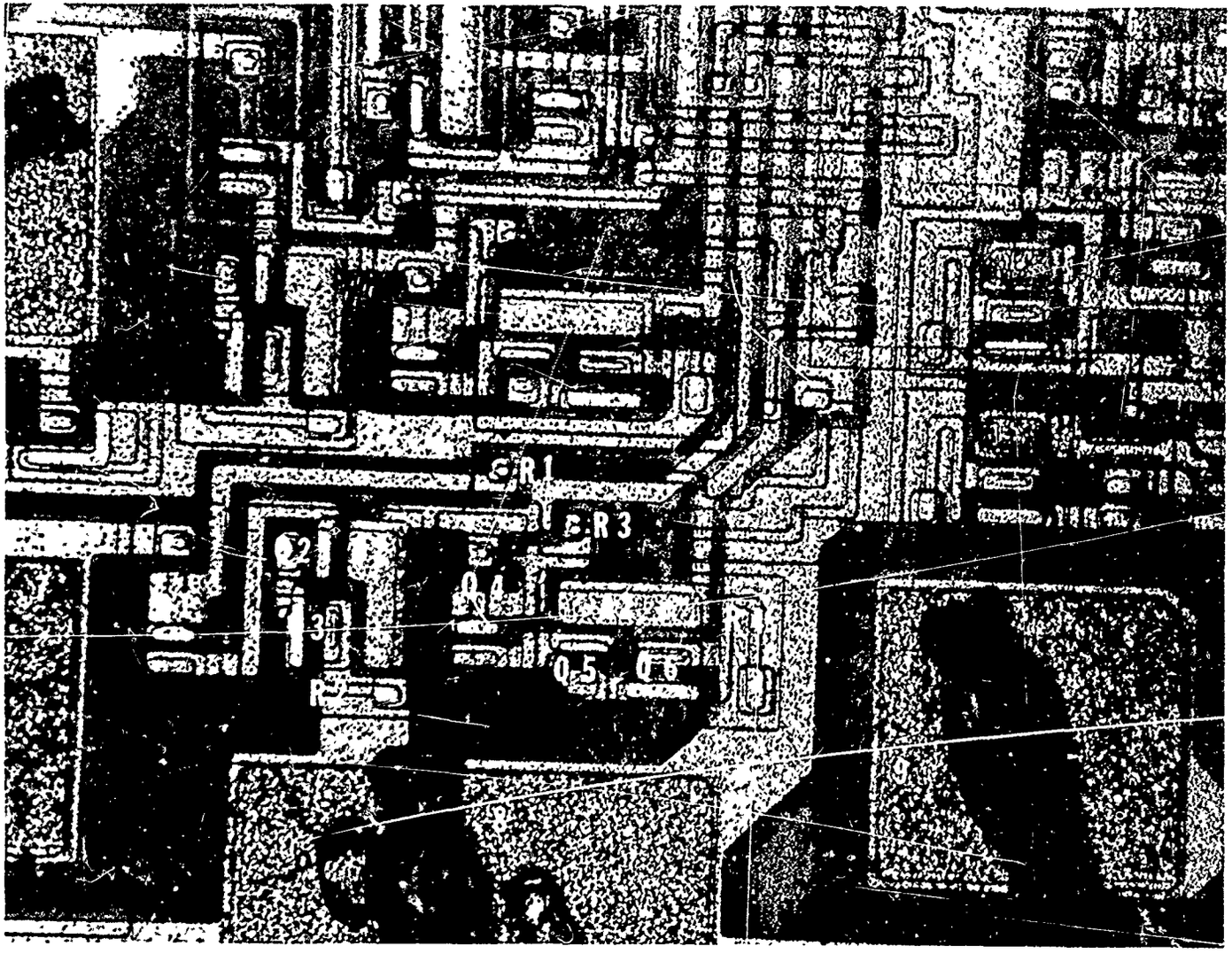


Photo 2-3 Light Photograph of A2 Row Address Inverter. Mag. - 365X

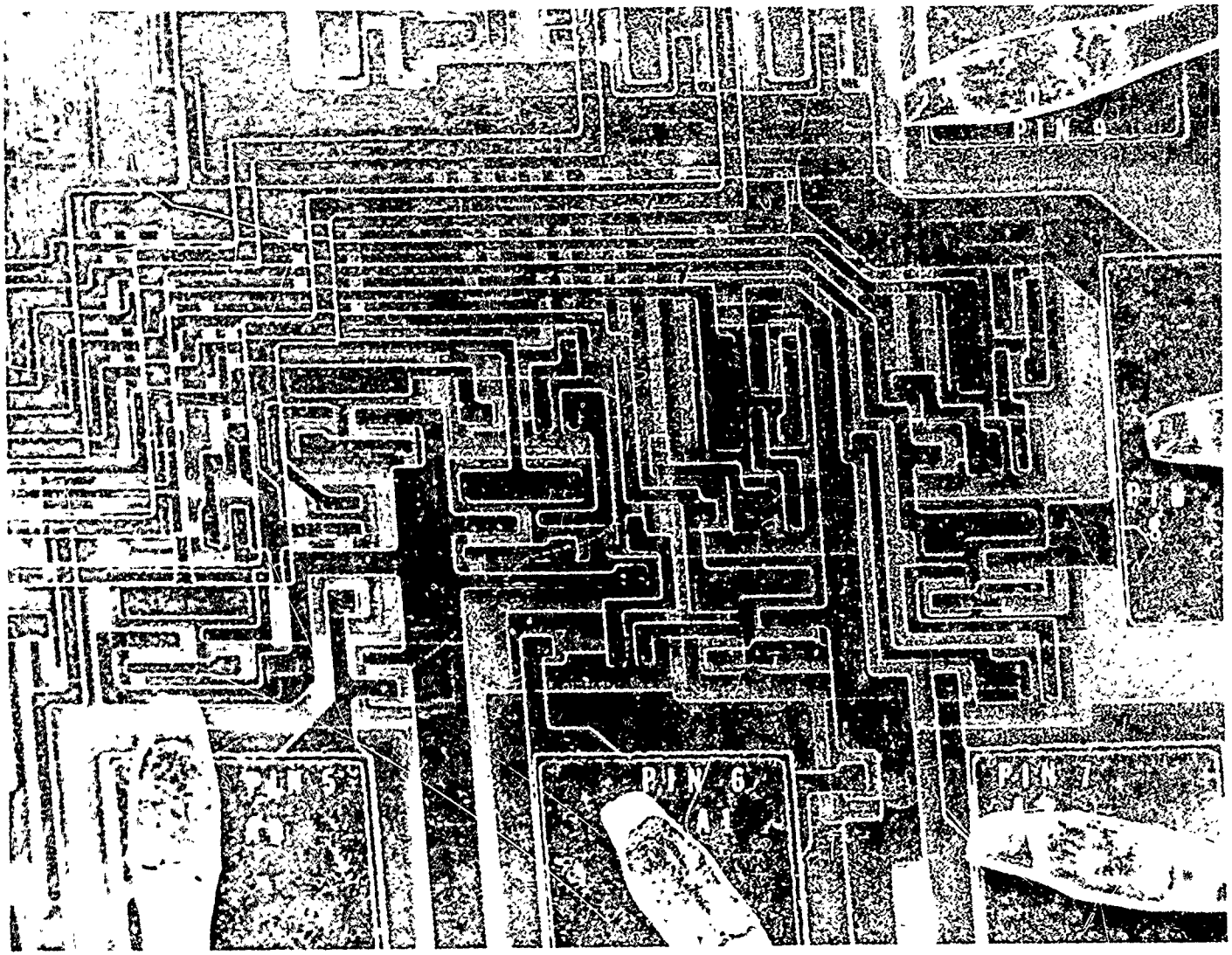


Photo 2-4 SEI Micrograph of A0, A1 and A2 Row Address Inverters. This Includes the Same Area as Photos 2-5 and 2-6. Mag. - 310X

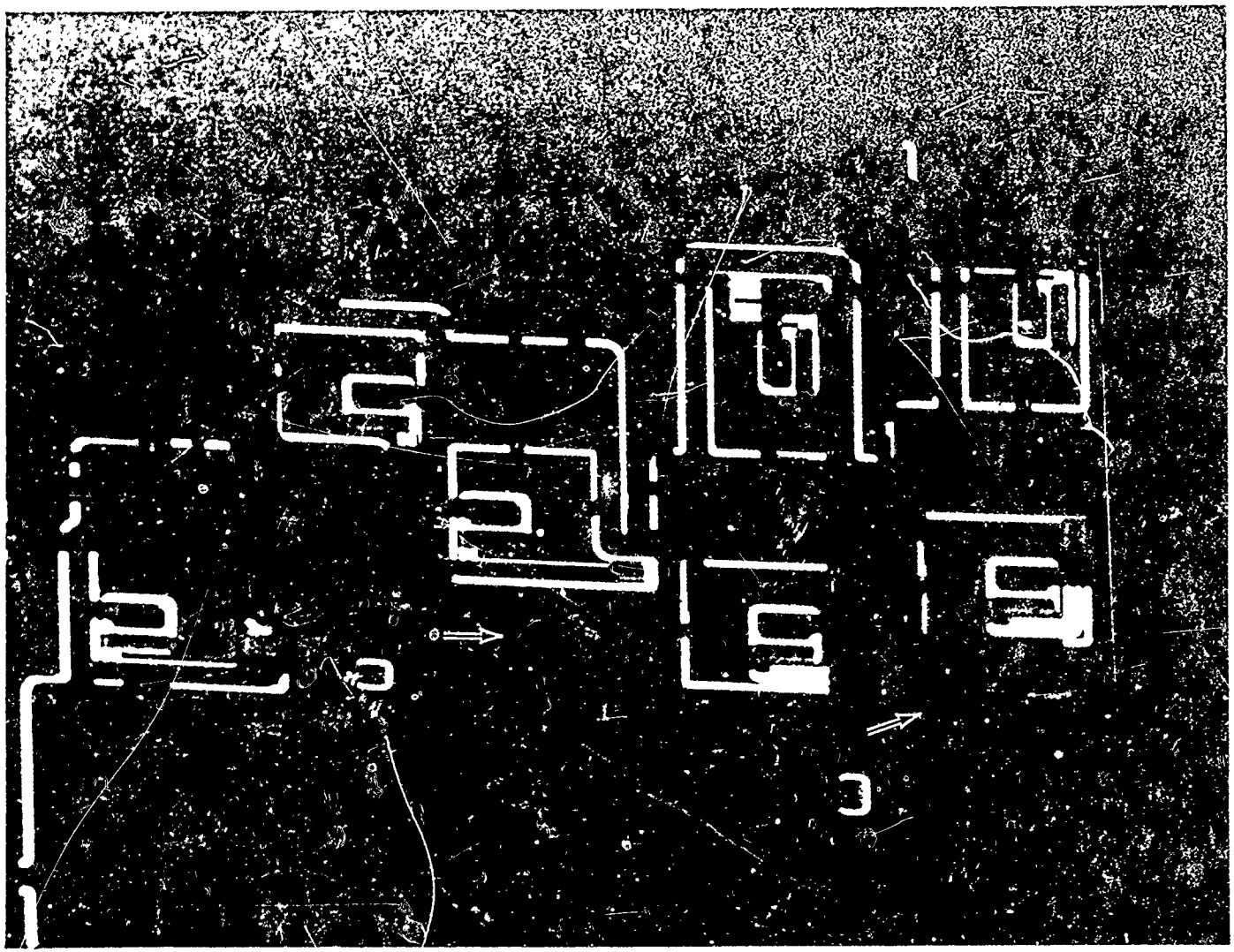


Photo 2-5 EBIC Micrograph of A0, A1 and A2 Row Address Inverters. The Arrows Locate Two of the Input Transistor Cells. 10 KV, Mag. - 310X

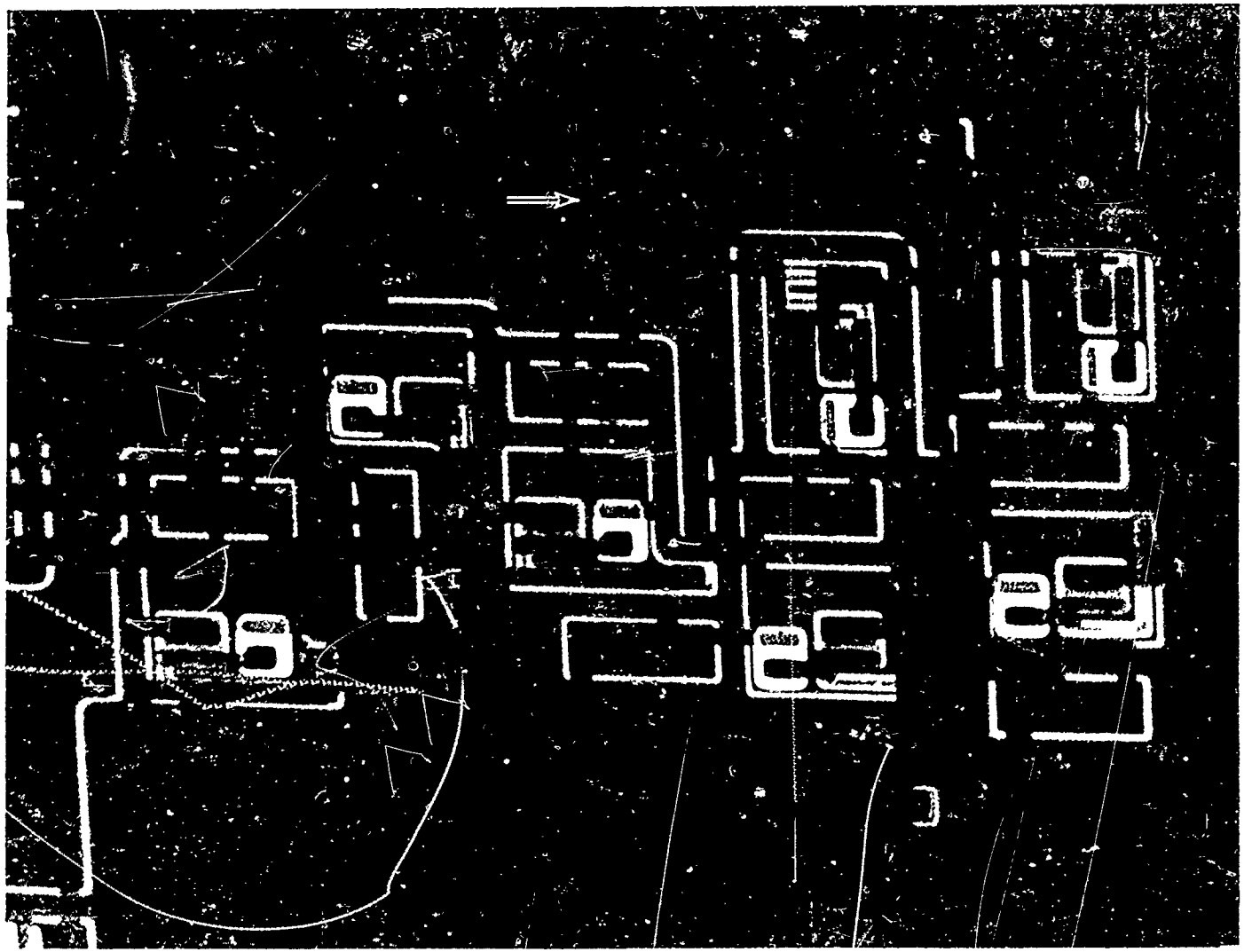


Photo 2-6 EBIC Micrograph of Same Area Shown in Photo 2-5 Using 15 Kv Beam Voltage. This Voltage Penetrates the Aluminum Conductors. Arrow Locates the Collector Resistor Tub Which Shows No EBIC Response. Mag. - 310X

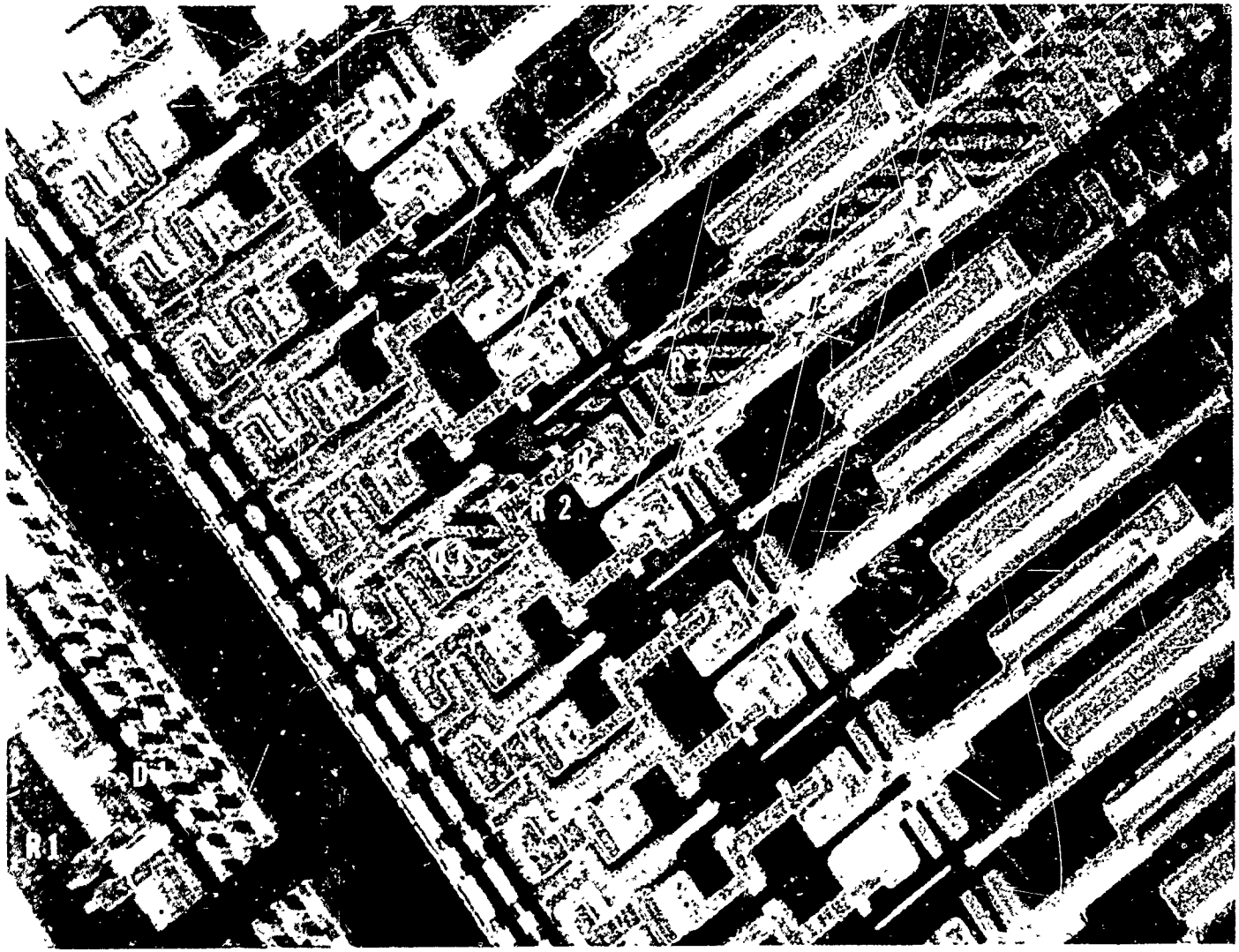


Photo 2-7 Voltage Contrast Micrograph of Row Address Decoder. Device is Being Cycled Between Addresses 245 and 253. Mag. - 350X

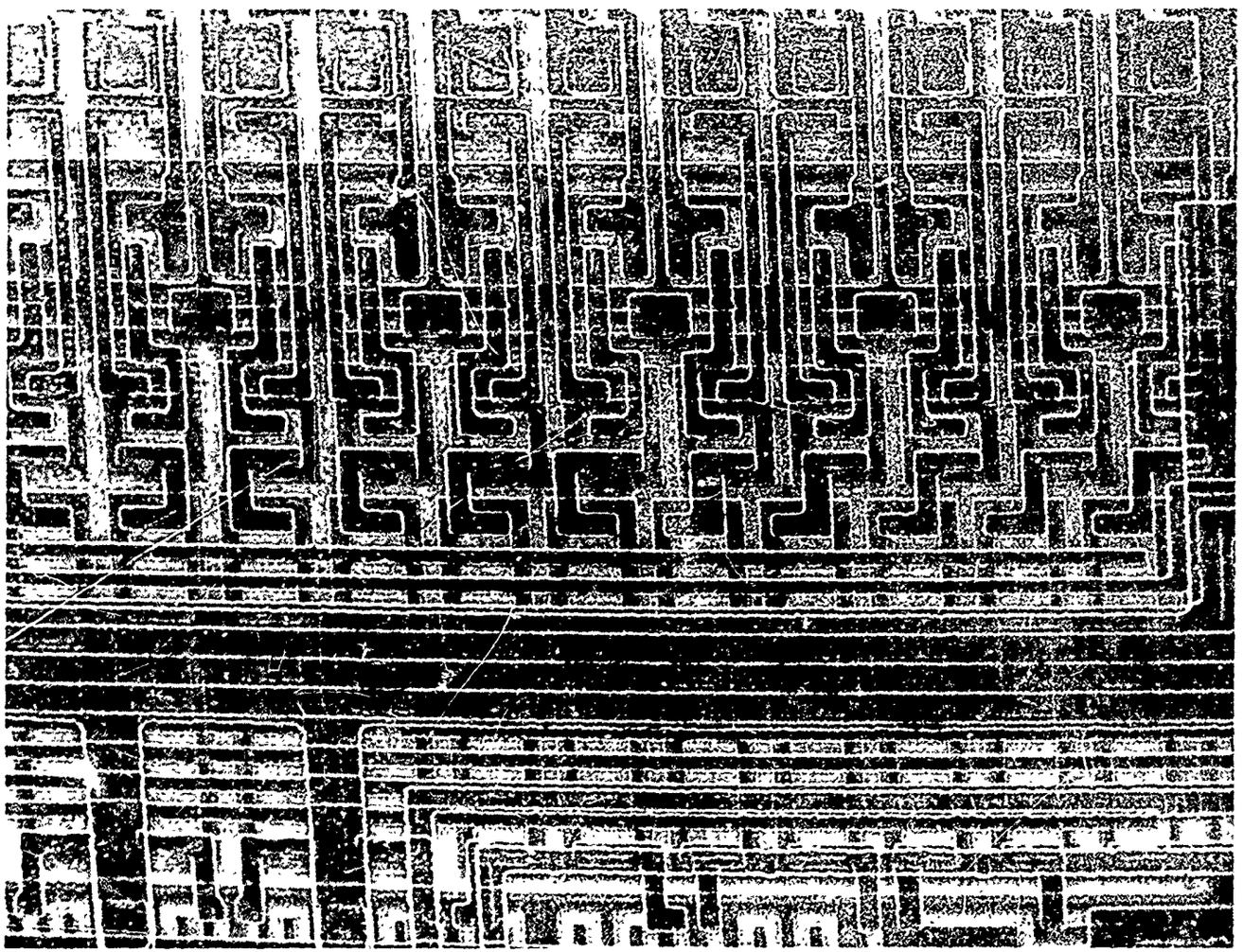


Photo 2-8 SEI Micrograph of the Row Decoders. This is the Same Area Shown in Photo 2-9. Mag. - 350X

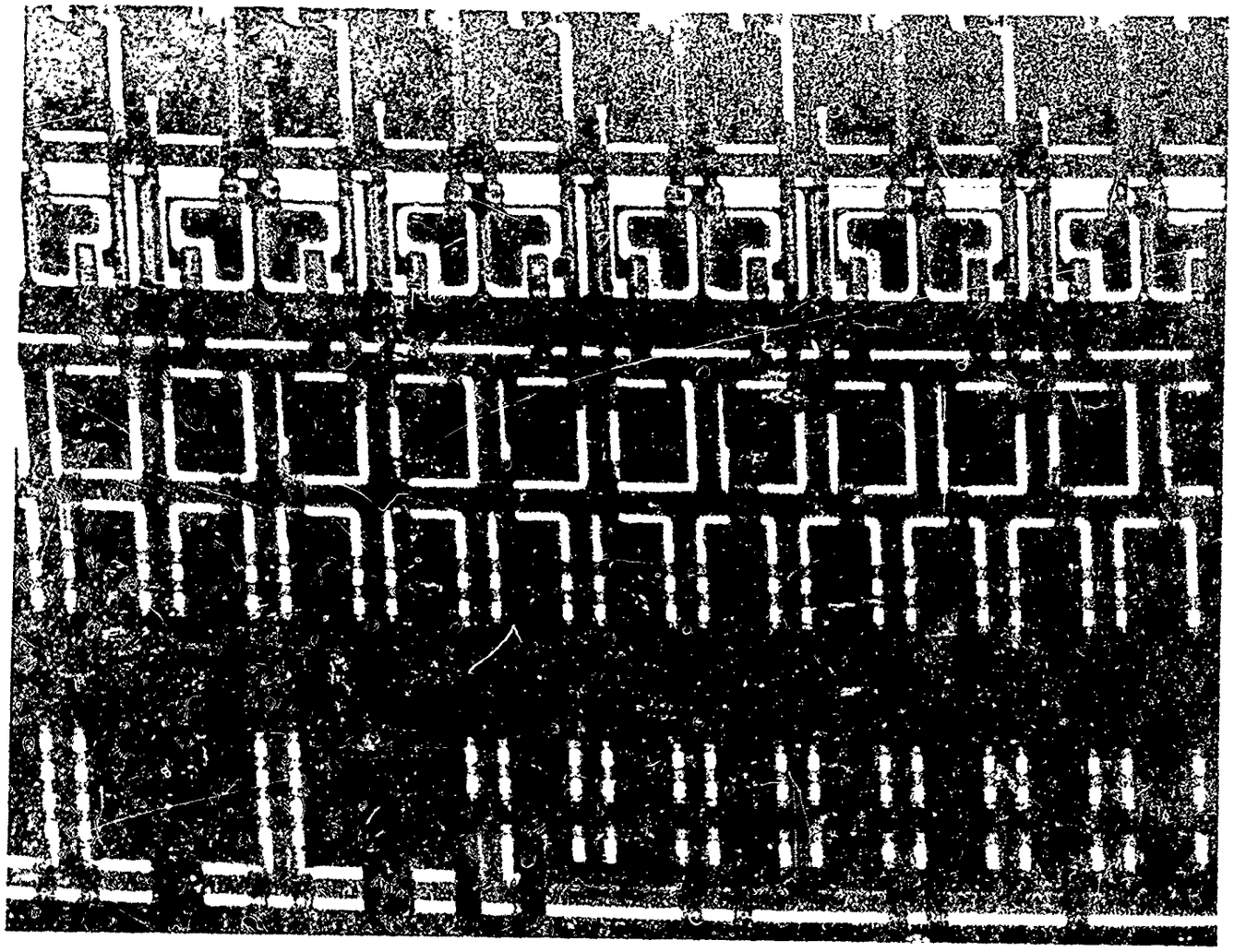


Photo 2-9 EBIC Micrograph of the Row Address Decoders. Beam Voltage is 15 KV. The Beam Voltage Does Penetrate the Second Level Metallization. Mag. - 350X

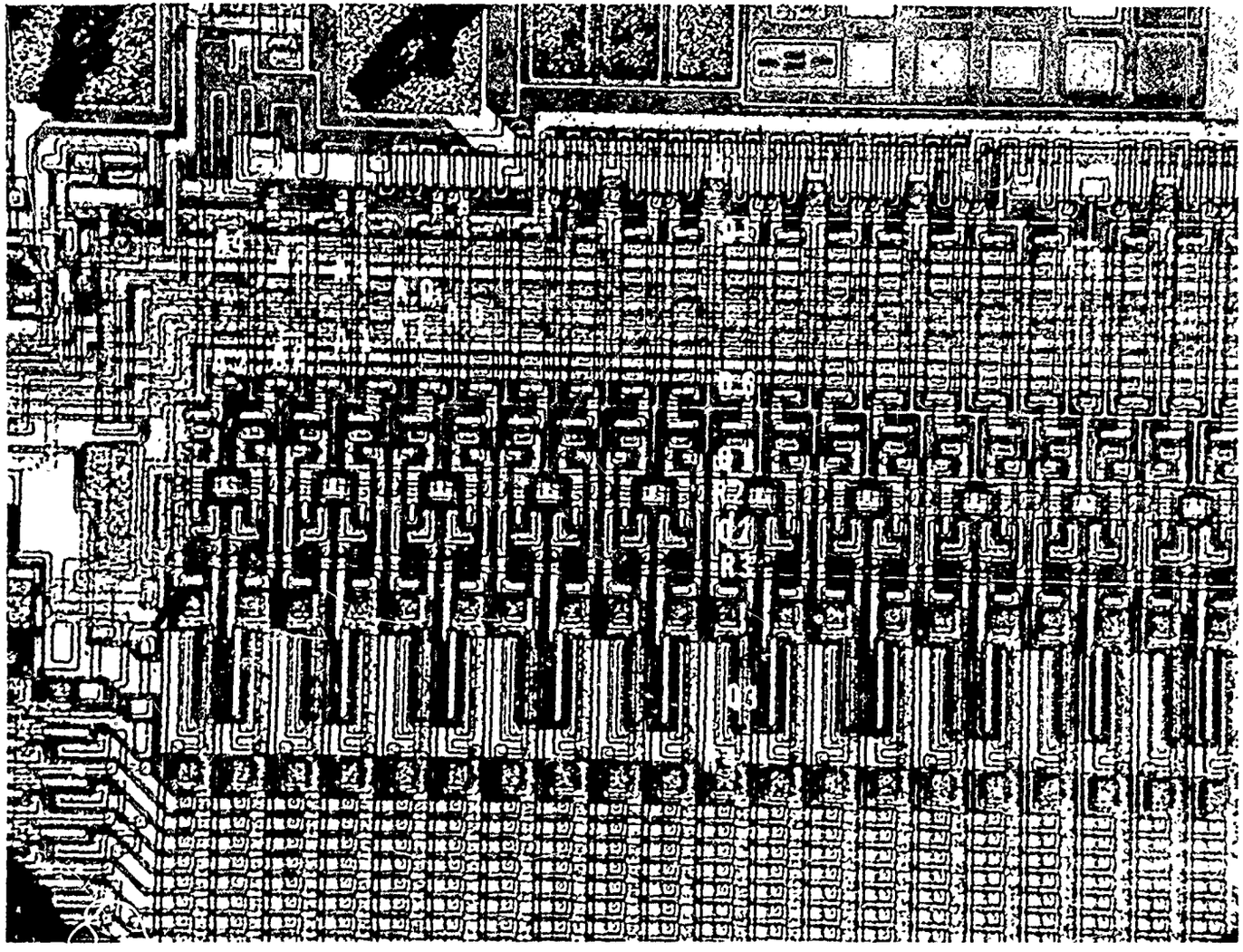


Photo 2-10 Light Photograph of the Row Address Decoders. The Row Address Lines Have Been Identified. Mag. - 175X

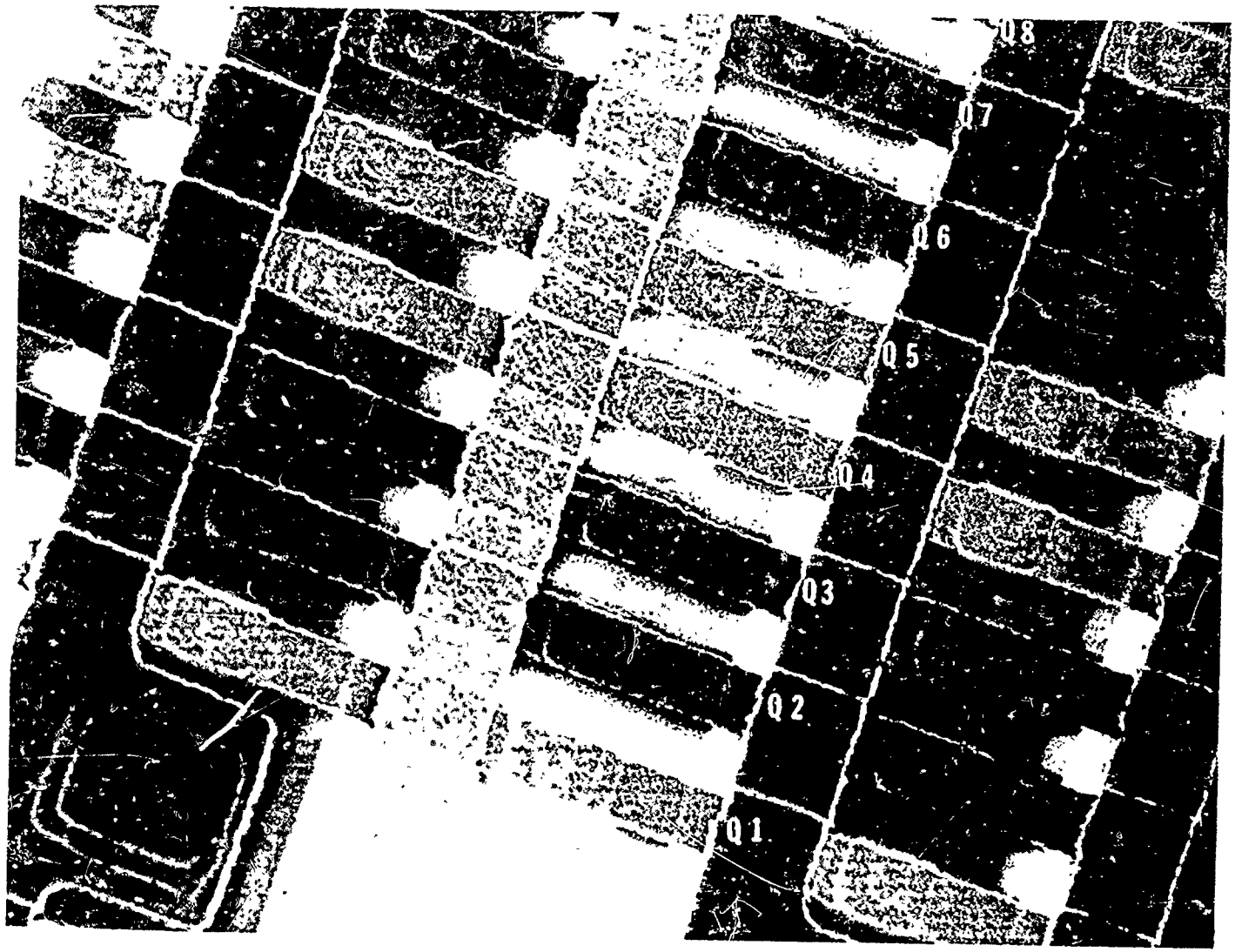


Photo 2-11 Voltage Contrast Micrograph of Memory Cells. The Row of Cells in the Center are Addressed by the Row Decoder. Mag. - 1550X

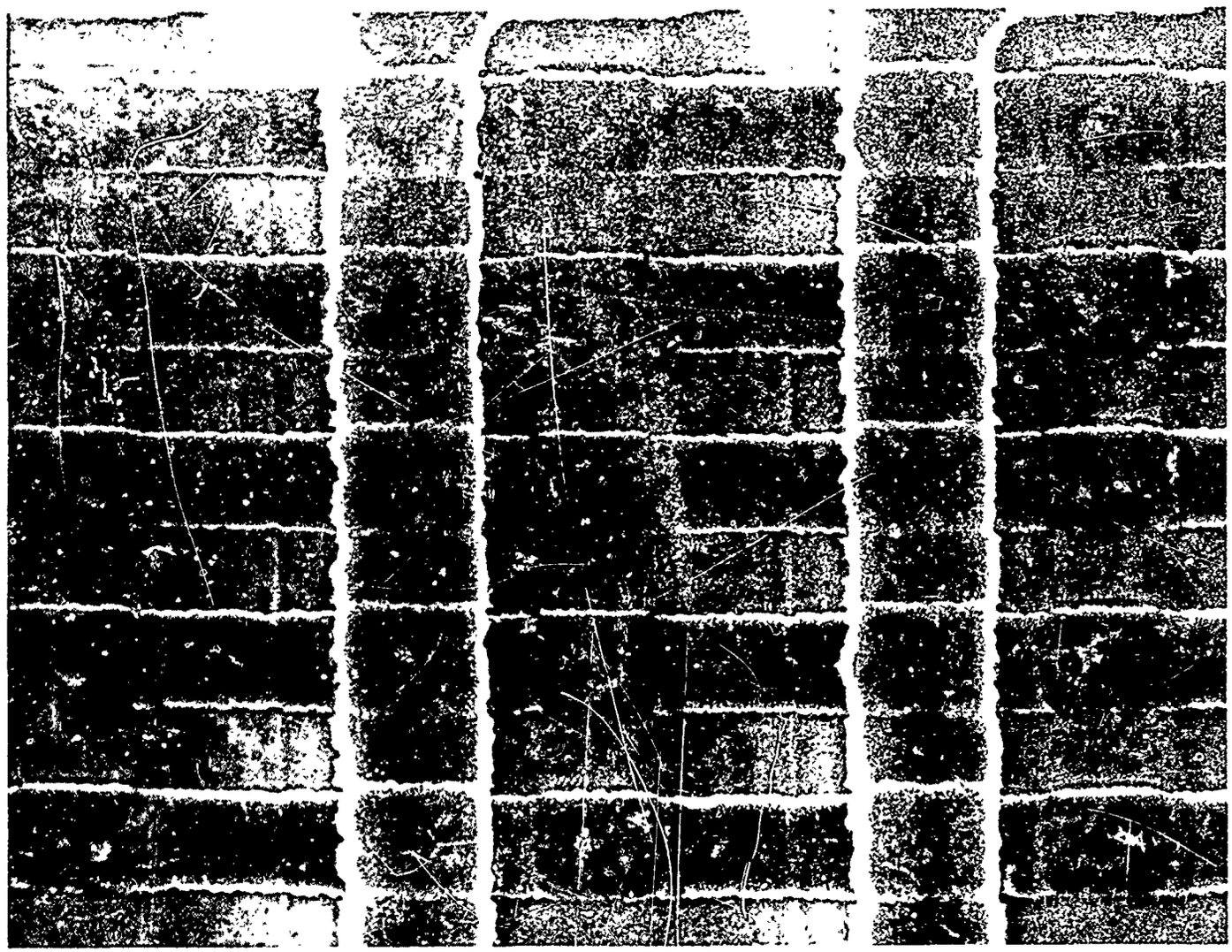


Photo 2-12 SEI Micrograph of 15 Memory Cells. Mag. - 1550X

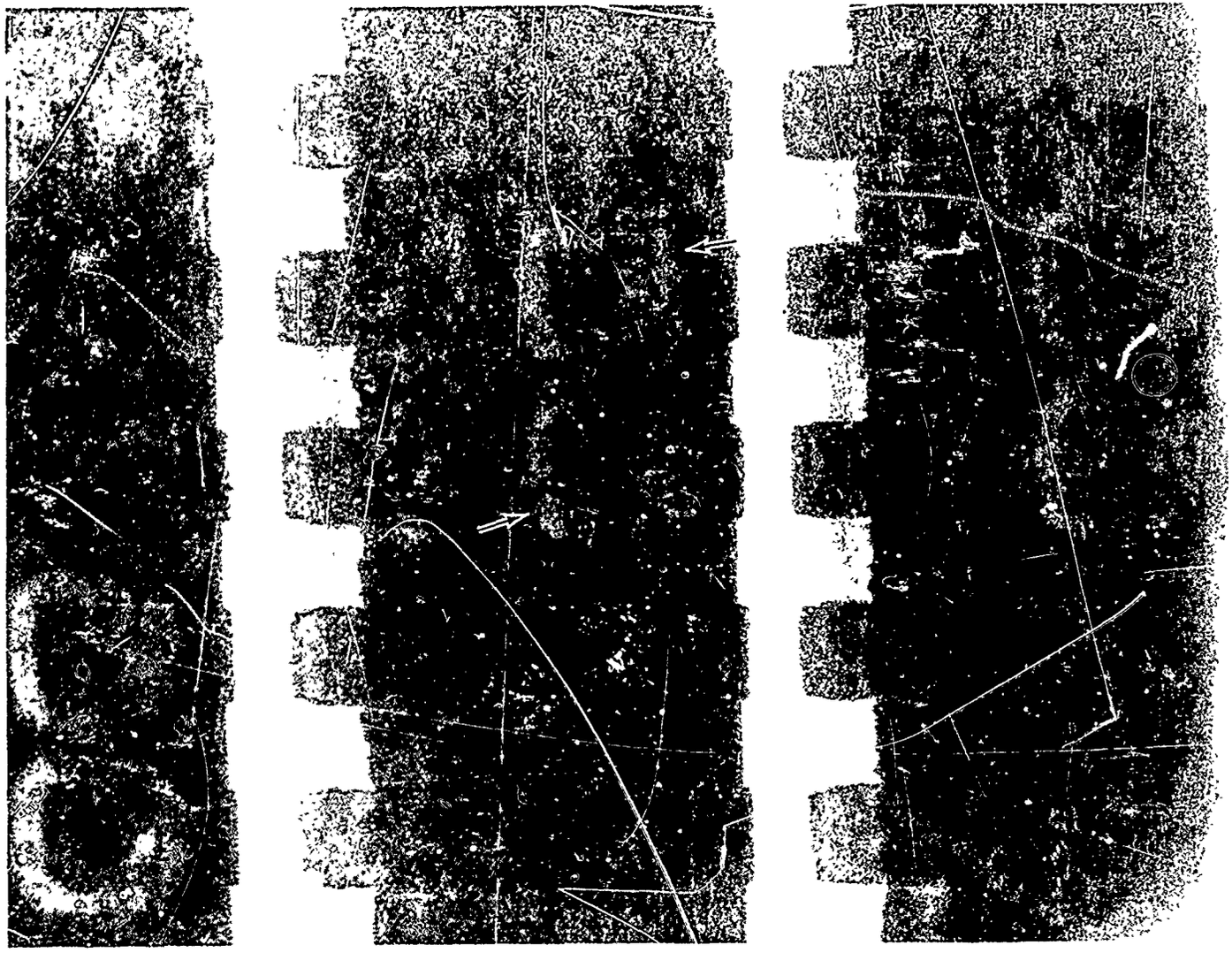


Photo 2-13 EBIC Micrograph Showing Same Area as Photo 2-12. Programmed (Shorted) Cells are Identified by Arrows. Mag. - 1550X

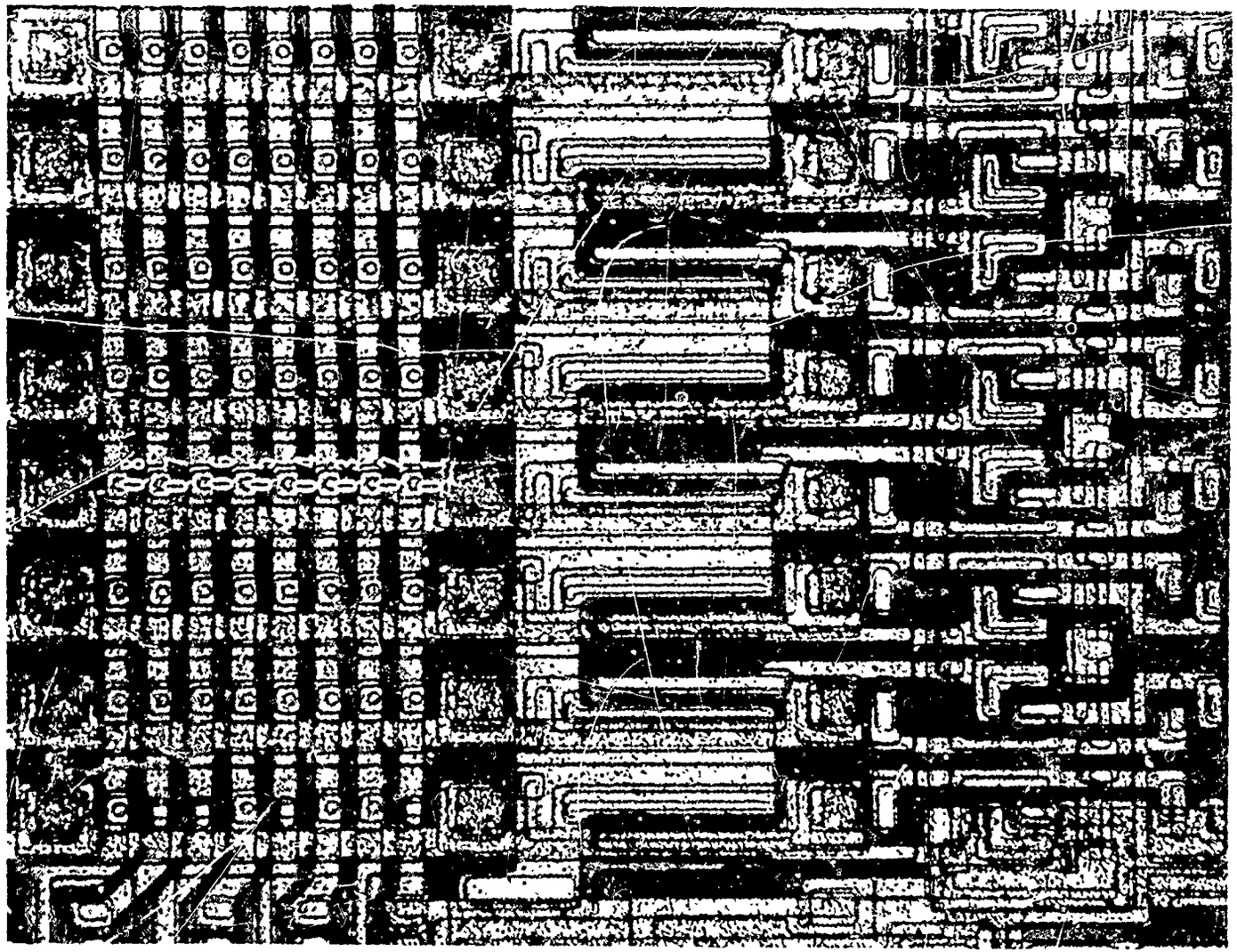


Photo 2-14 Light Photograph Showing One Forth of the Memory Cells for Rows 26 - 33. Row 33 is a Test Row Which is Discussed Later. Mag. ~ 365X

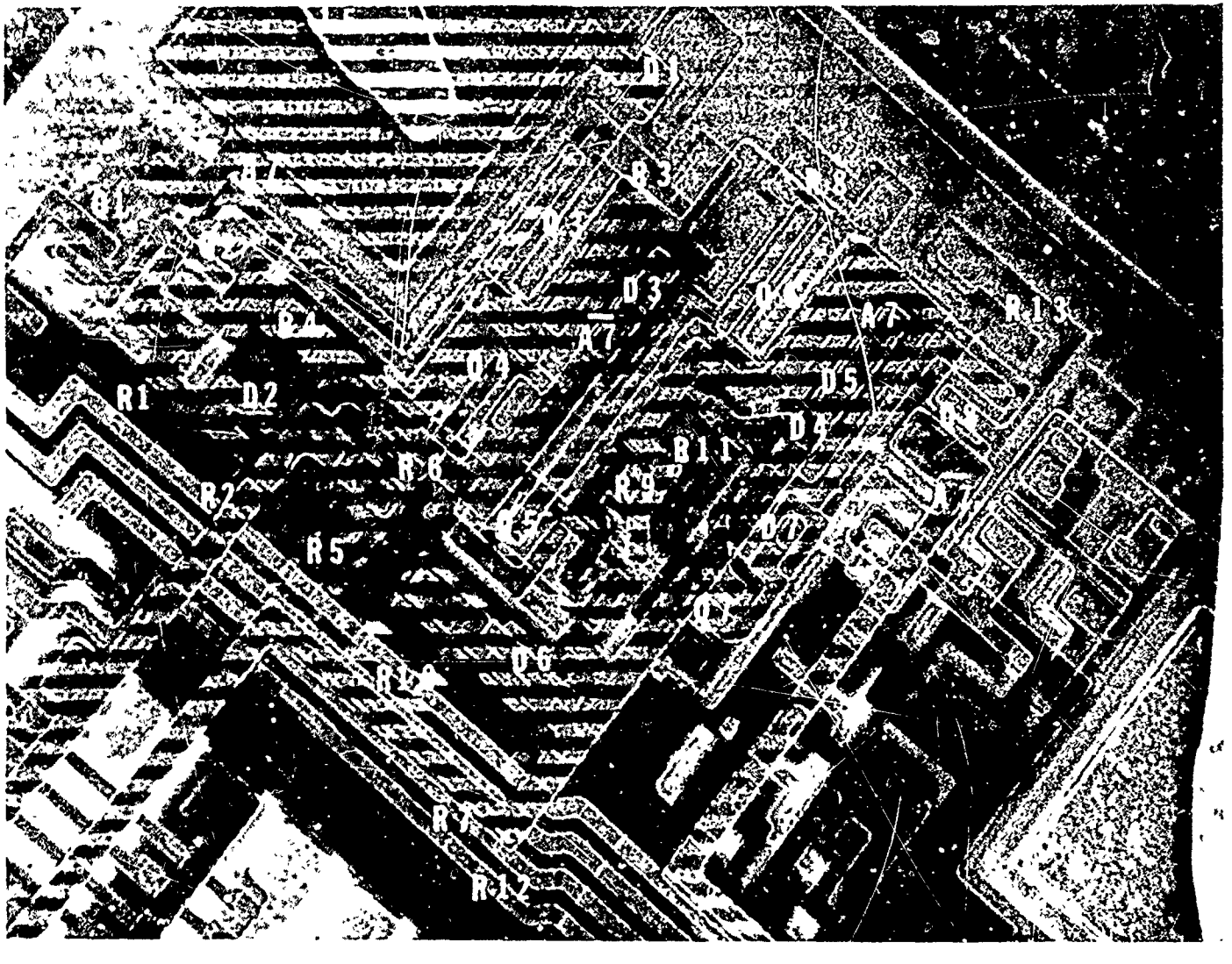


Photo 2-15 Voltage Contrast Micrograph of the A7 Column Address Inverter. The A7 Input is the Only Input Being Cycled. Mag. - 390X

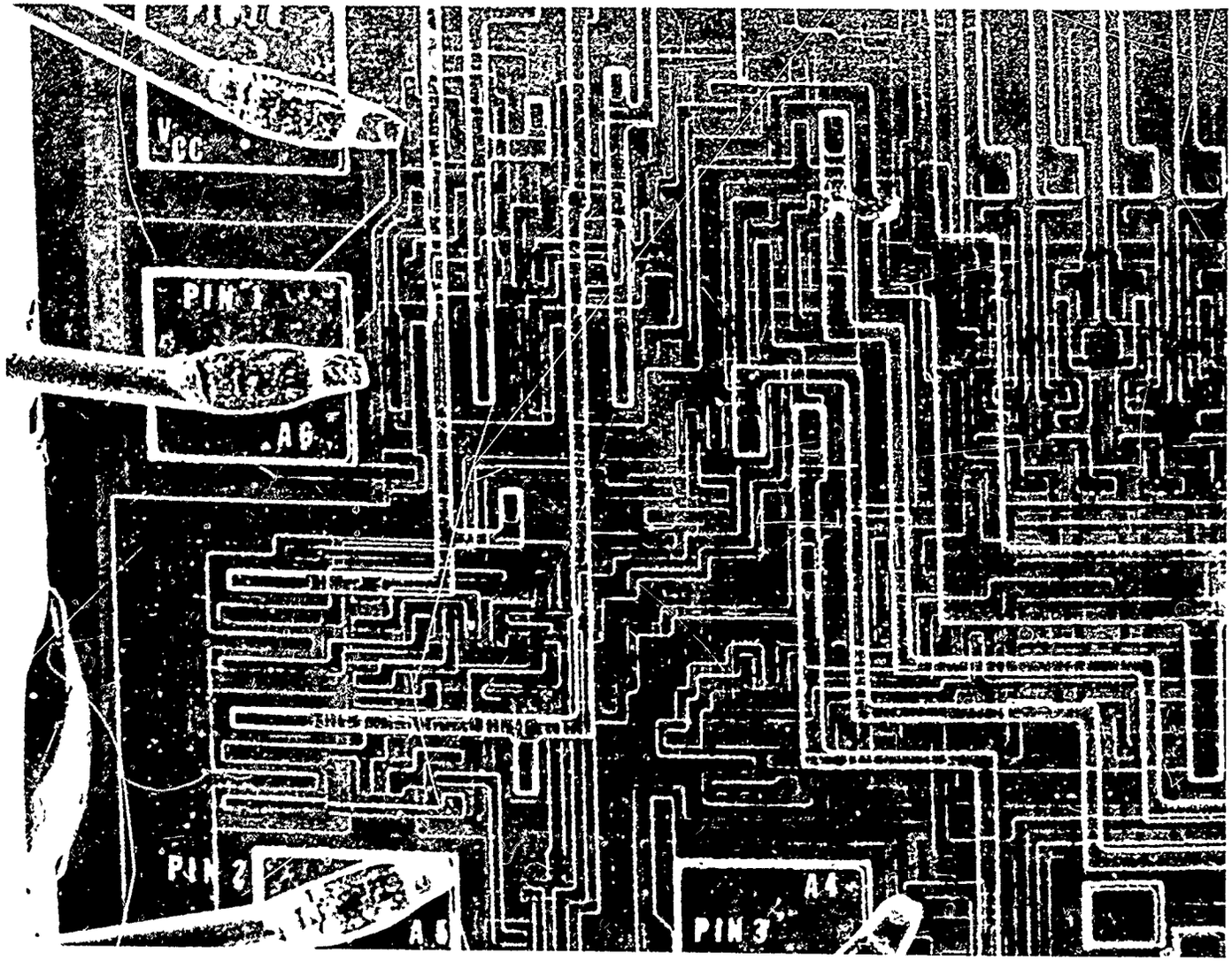


Photo 2-16 SEI Micrograph Showing A5 and A6 Column Address Inverters. Mag. - 235X

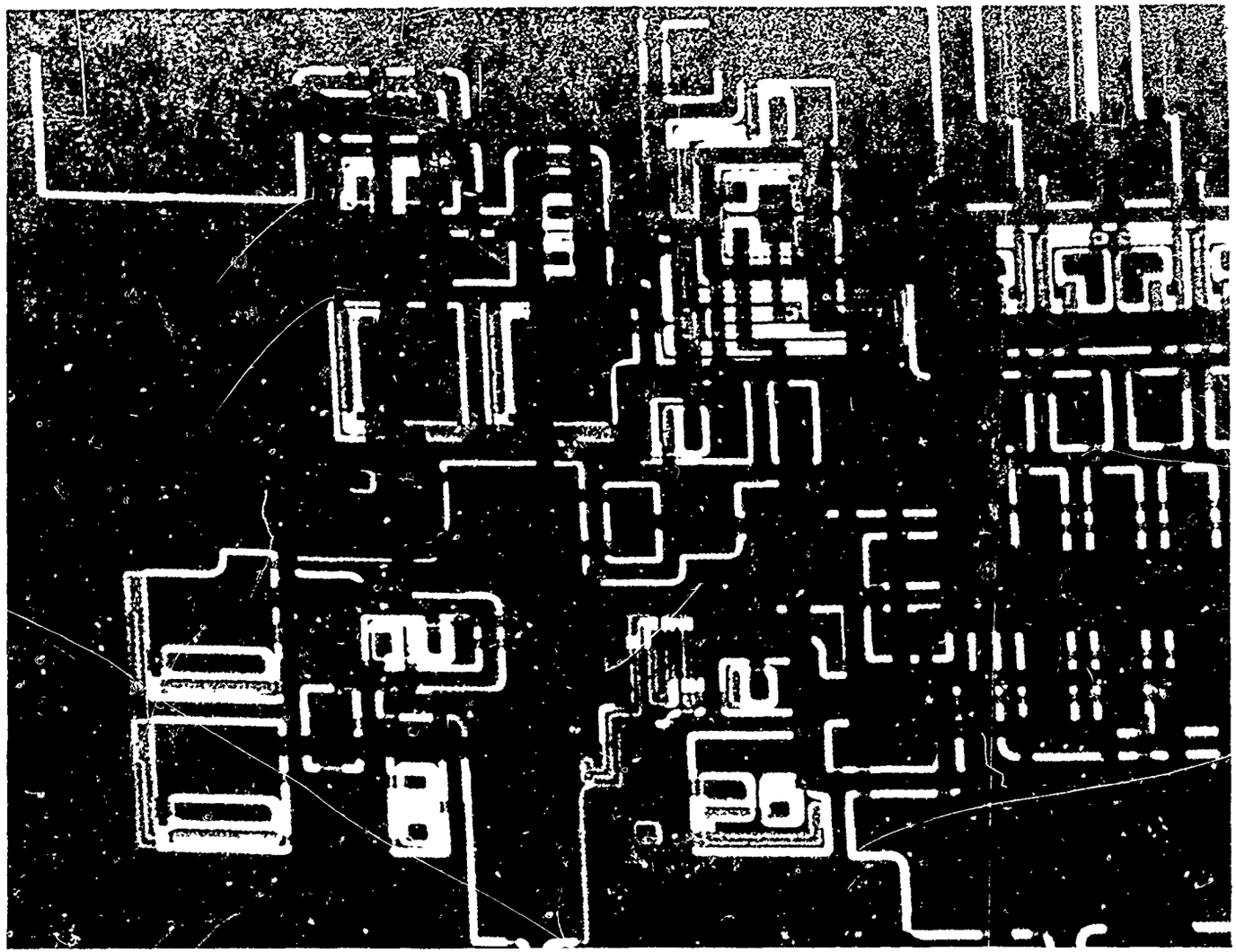


Photo 2-17 EBIC Micrograph of Same Area Shown in Photo 2-16. Beam Voltage is 15 KV. Mag. - 235X

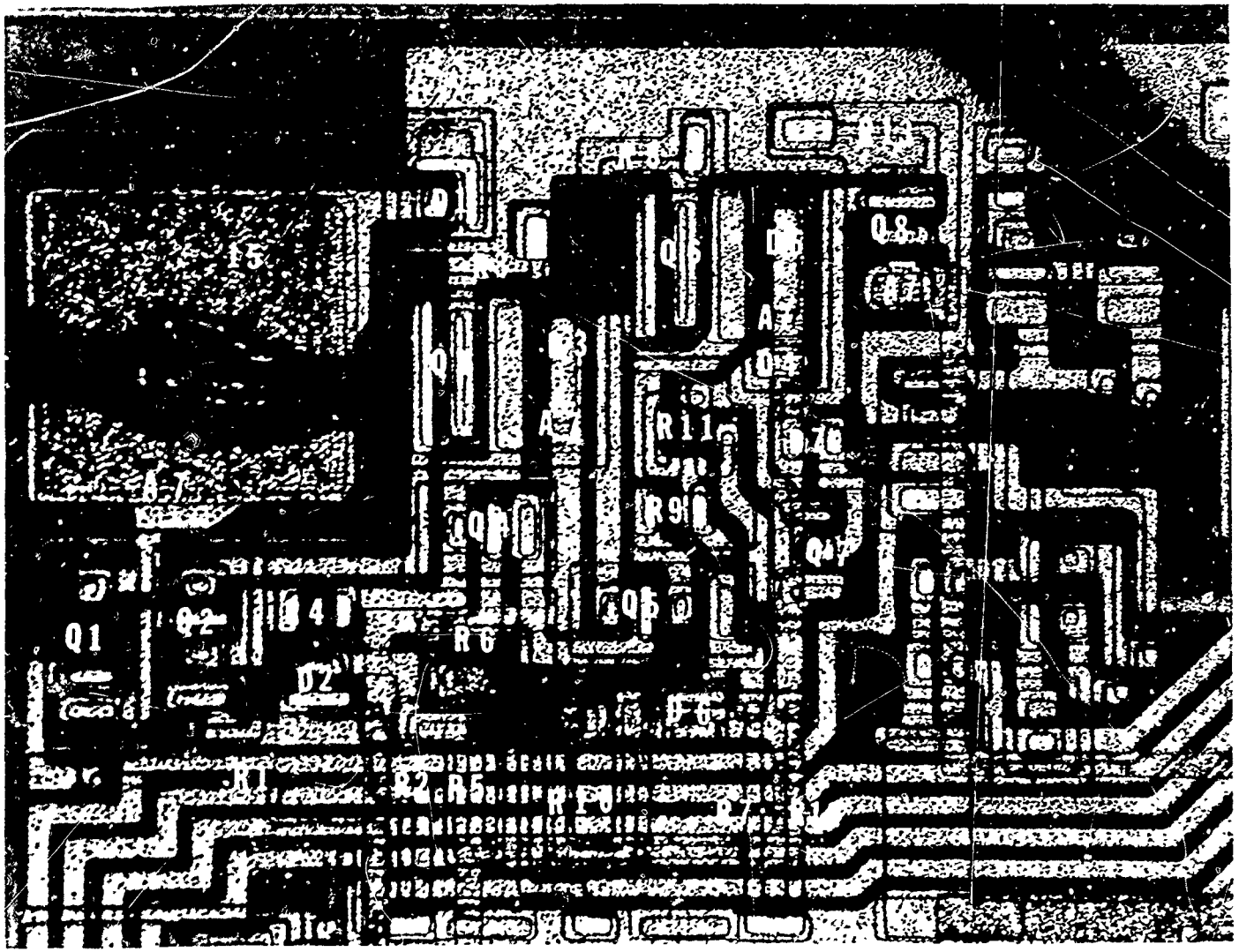


Photo 2-18 Light Photograph of A7 Column Address Inverter. Mag. - 365X

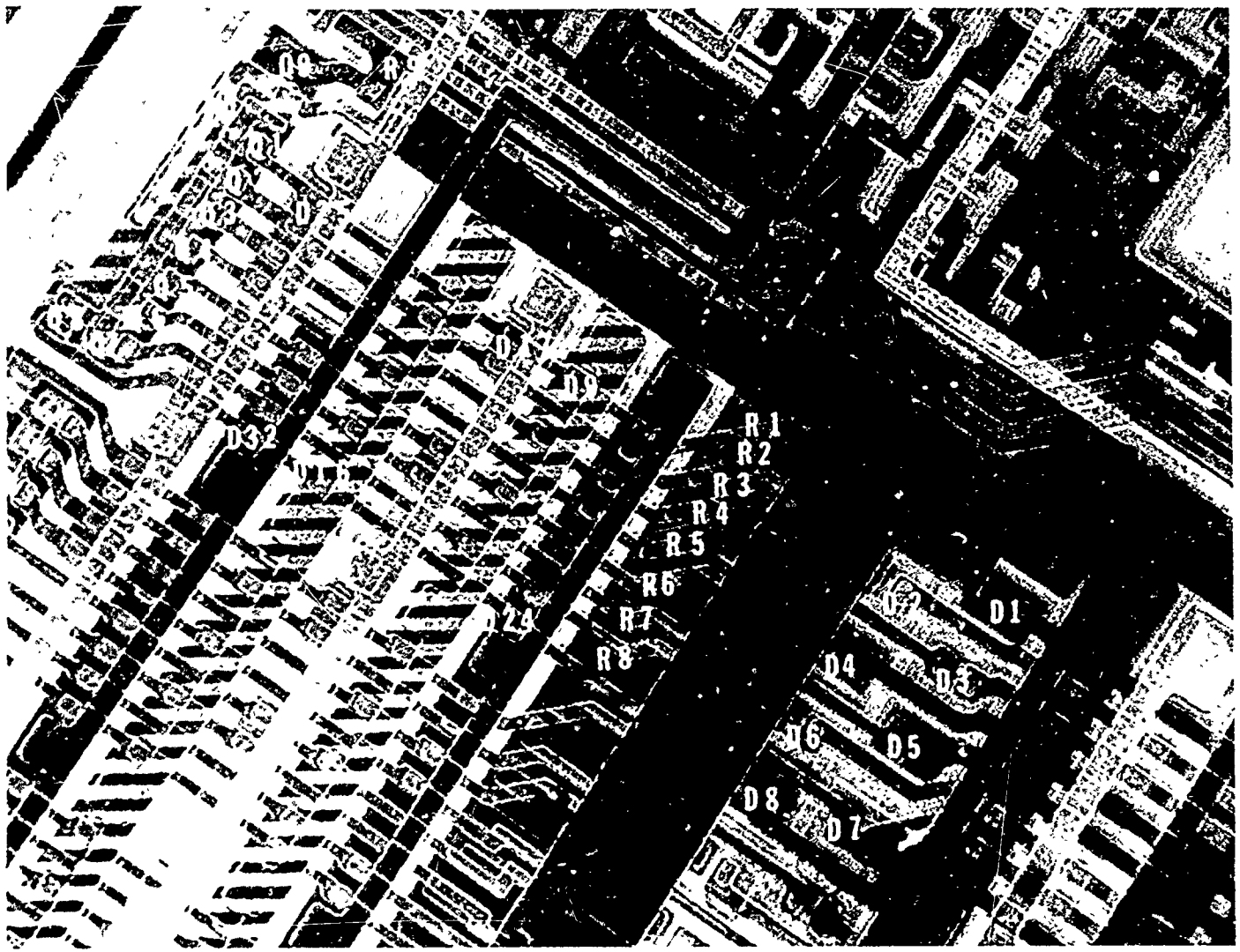


Photo 2-19 Voltage Contrast Micrograph Showing the Column Decode and Sense Amplifier Circuits for Output Q0 (Zero). The Circuit is Being Cycled Between Address 223 and 255. This Alternately Switches Output from a Hi to a Lo Data State. Mag. -350X

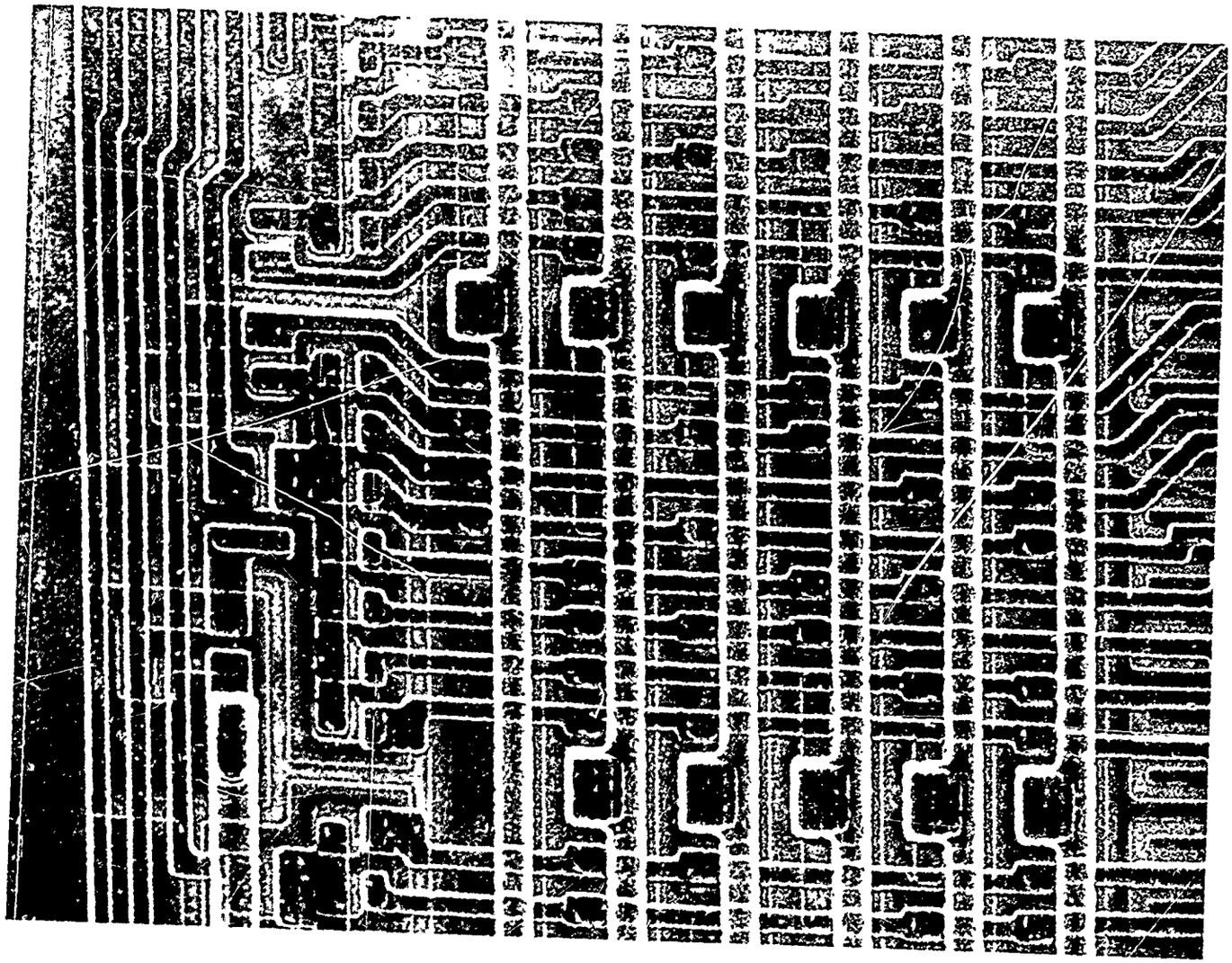


Photo 2-20 SEI Micrograph of the Column Decode and Sense Amplifier for Output Q1. Mag. - 500X

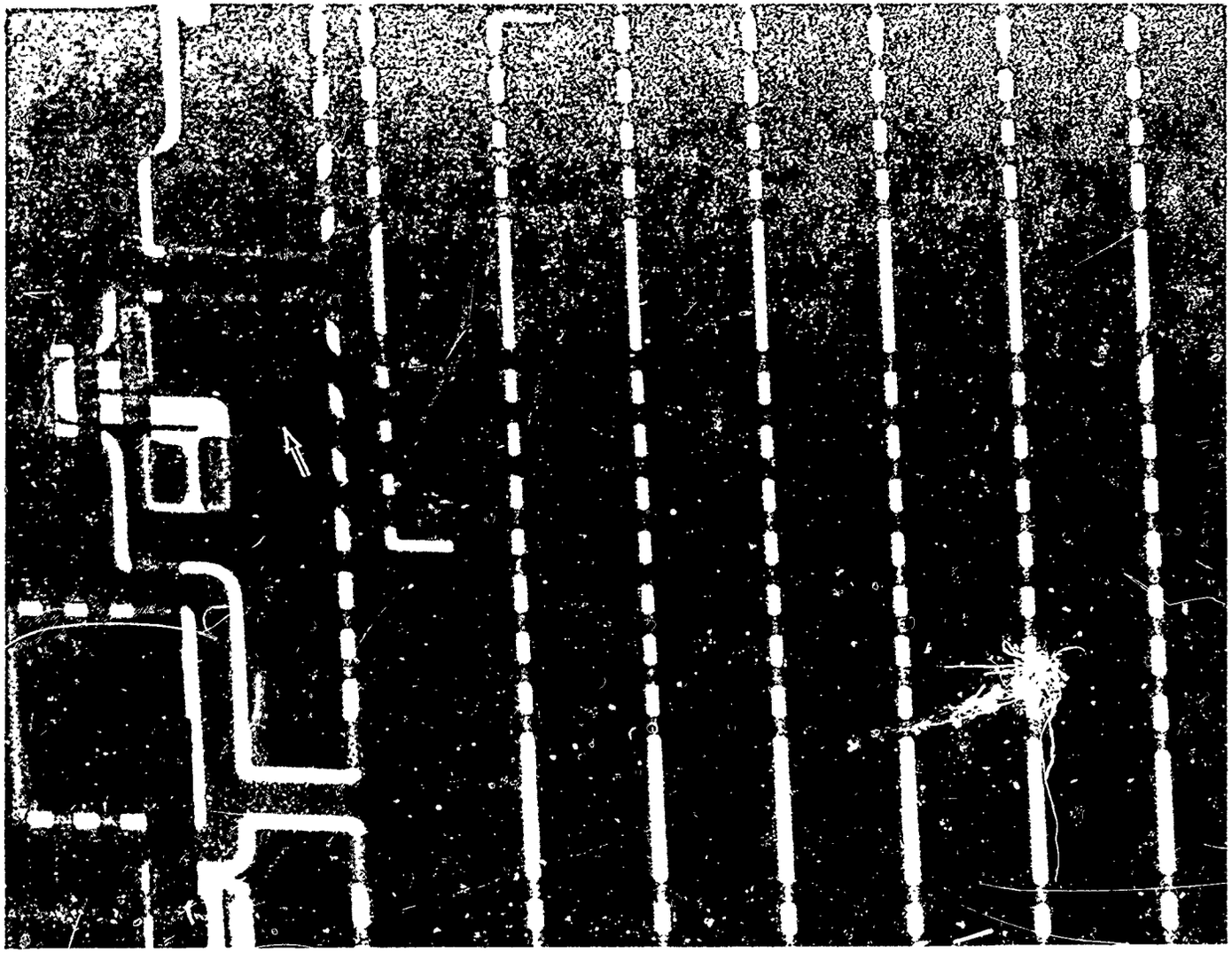


Photo 2-21 EBIC Micrograph of the Column Decode and Sense Amplifier Shown in Photo 2-20. The Arrow Locates the Emitter Diffusions for the Sense Transistor, Mag. - 500X

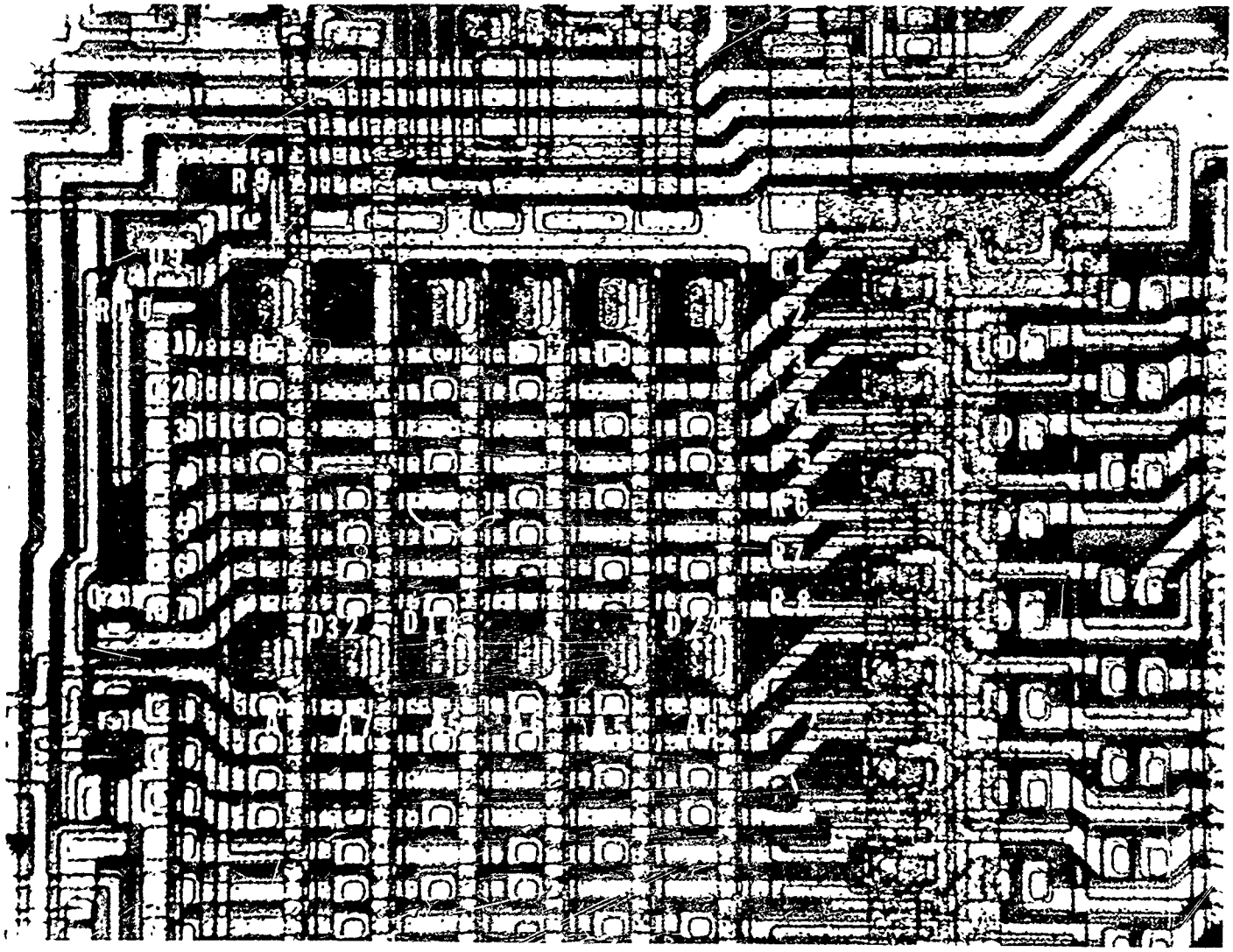


Photo 2-22 Light Photograph Showing the Column Decode and Sense Amplifier for Q0. The Column Address Lines are Also Identified. Mag. - 365X

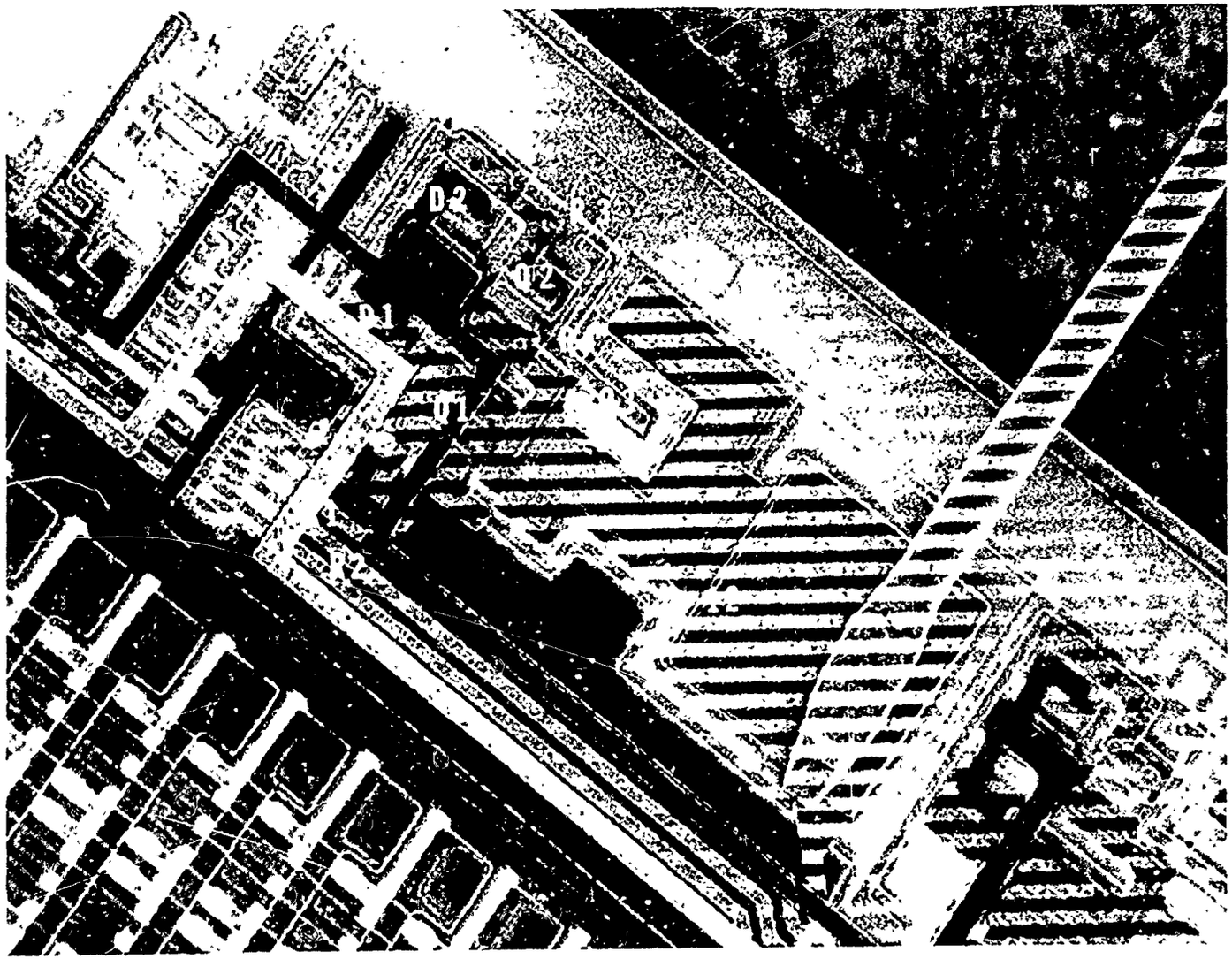


Photo 2-23 Voltage Contrast Micrograph of Data Output Q0. Mag. - 300X

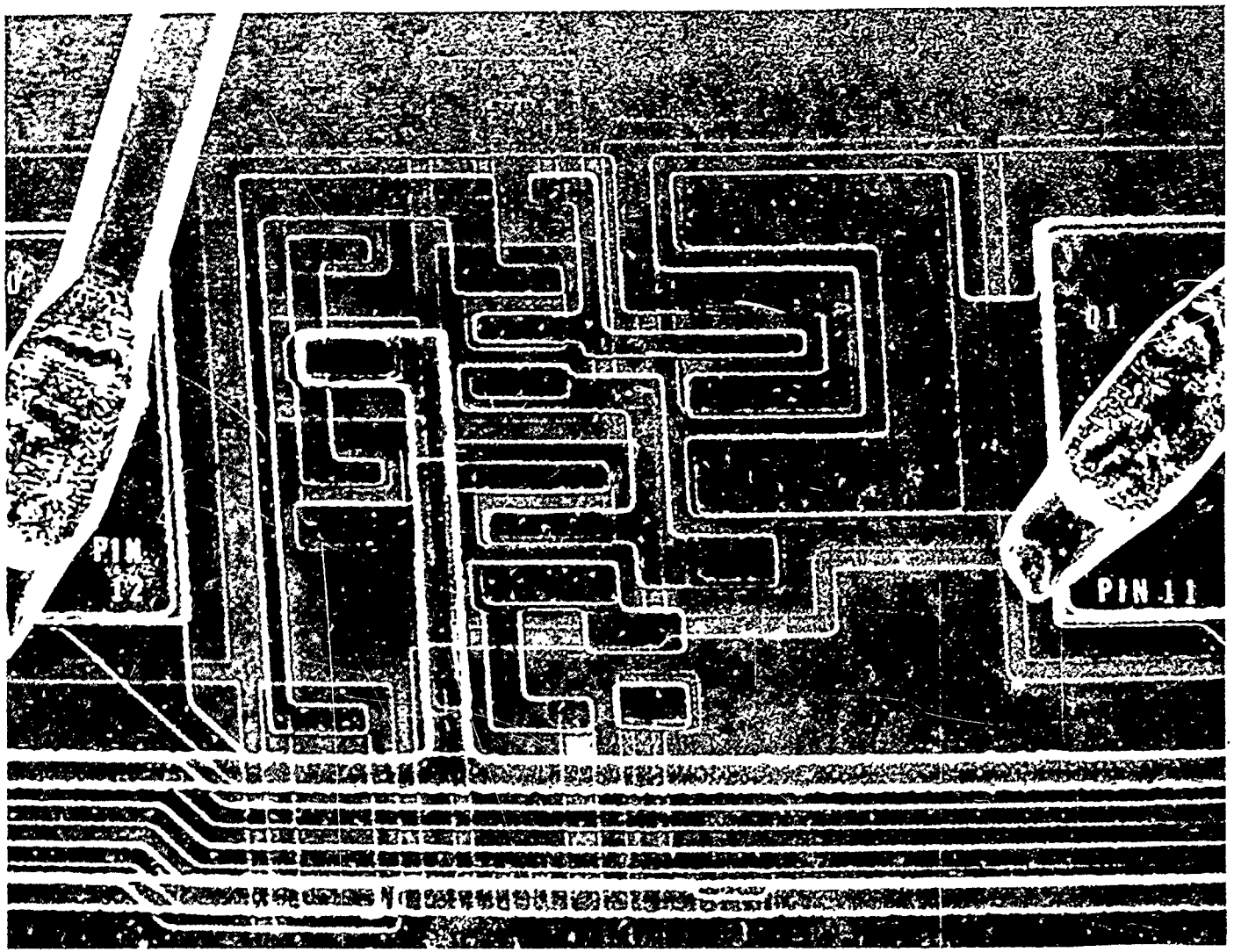


Photo 2-24 SEI Micrograph of Data Output Q1. Mag. - 500X

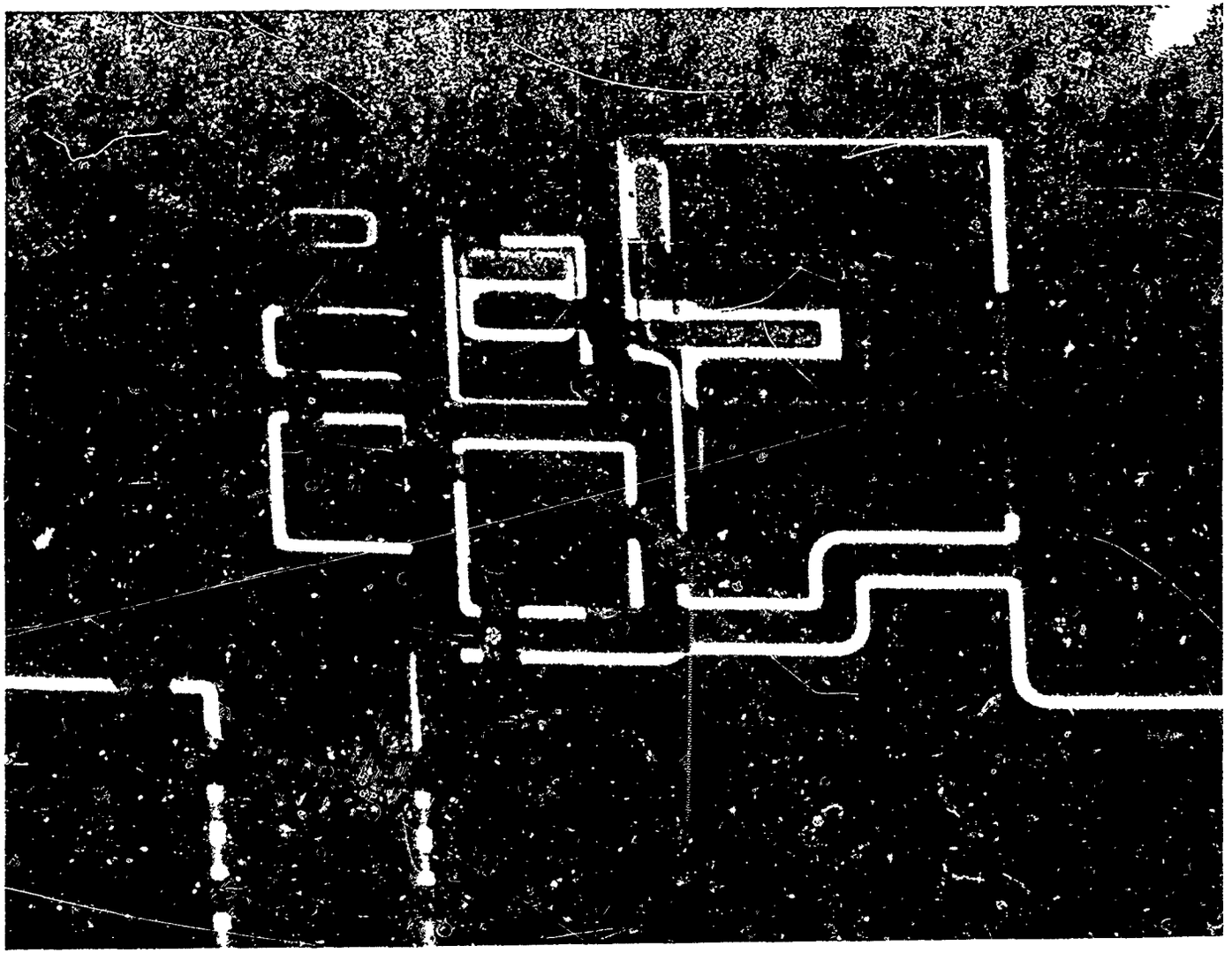


Photo 2-25 EBIC Micrograph of the Same Area Shown in Photo 2-24. Mag. - 500X

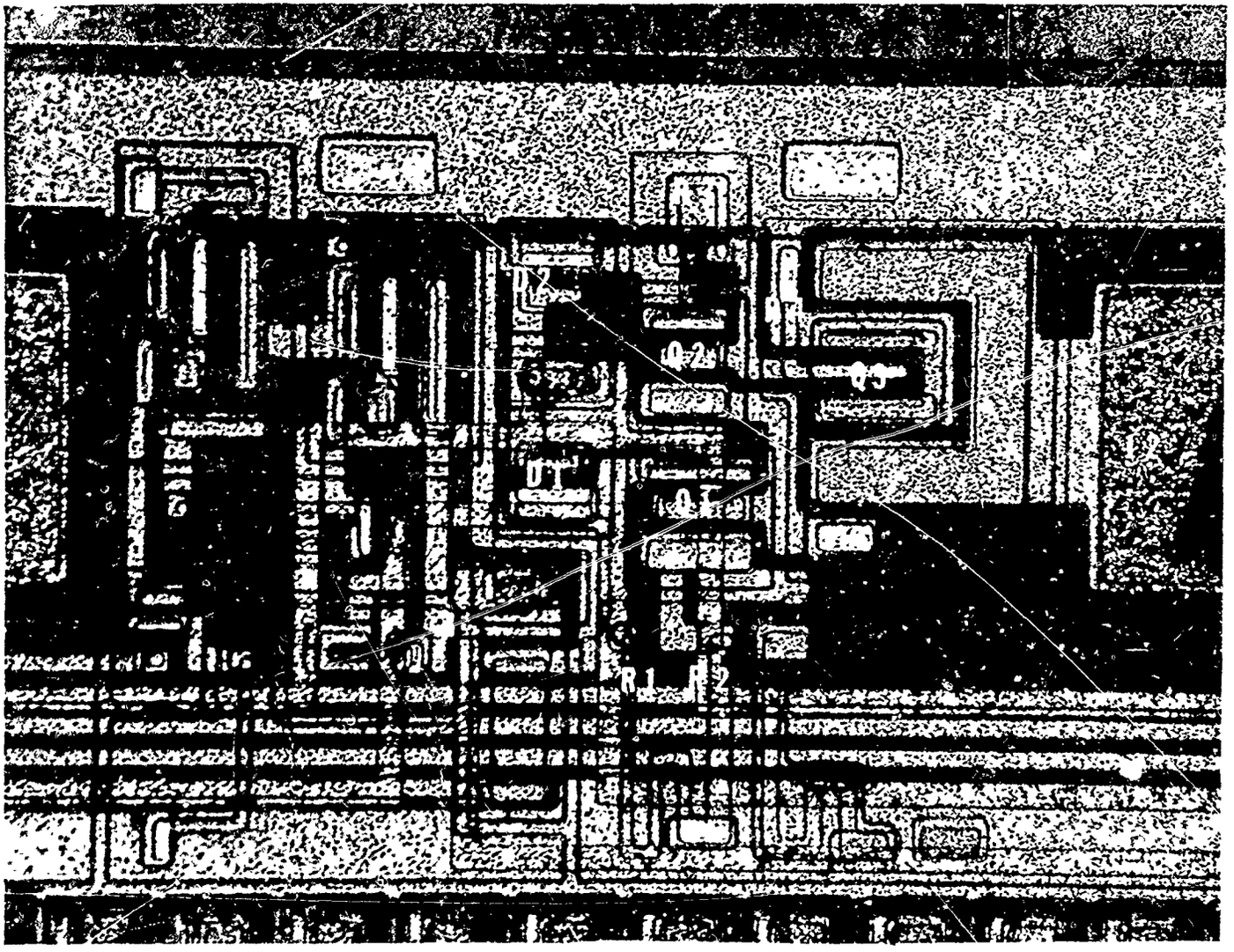


Photo 2-26 Light Photograph of Data Output Q0. Mag. - 365X

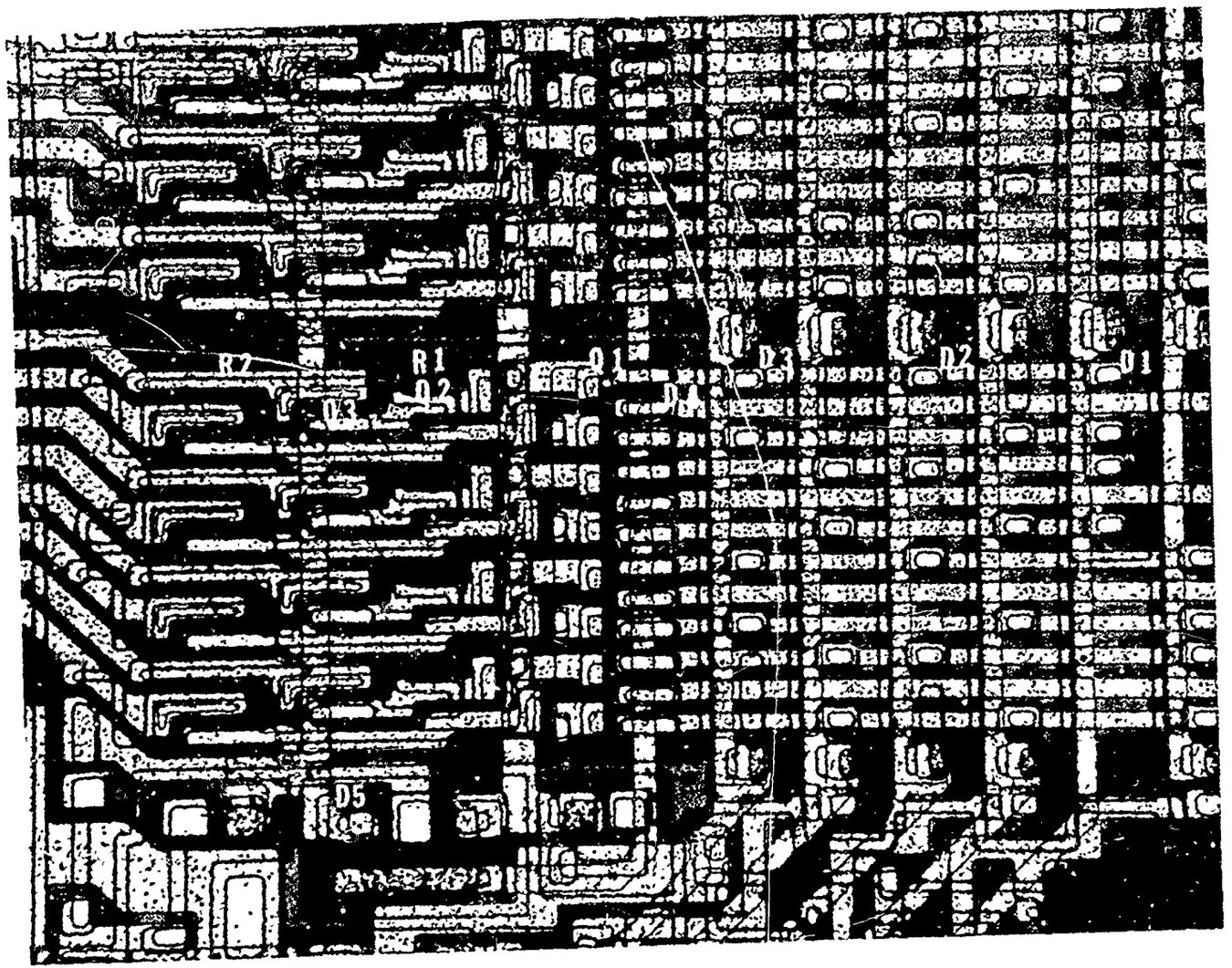


Photo 2-27 Light Photograph of Memory Program Driver and Column Address for Output Q3 Memory. Mag. - 365X



Photo 2-28 Voltage Contrast Micrograph of Memory Program Driver and Column Address for Data Output Q0 Memory. The 20 Volt Program Pulse Amplitude May be Seen Superimposed on 5 Volt Level at Transistor Q3 Collector. Mag. - 310X

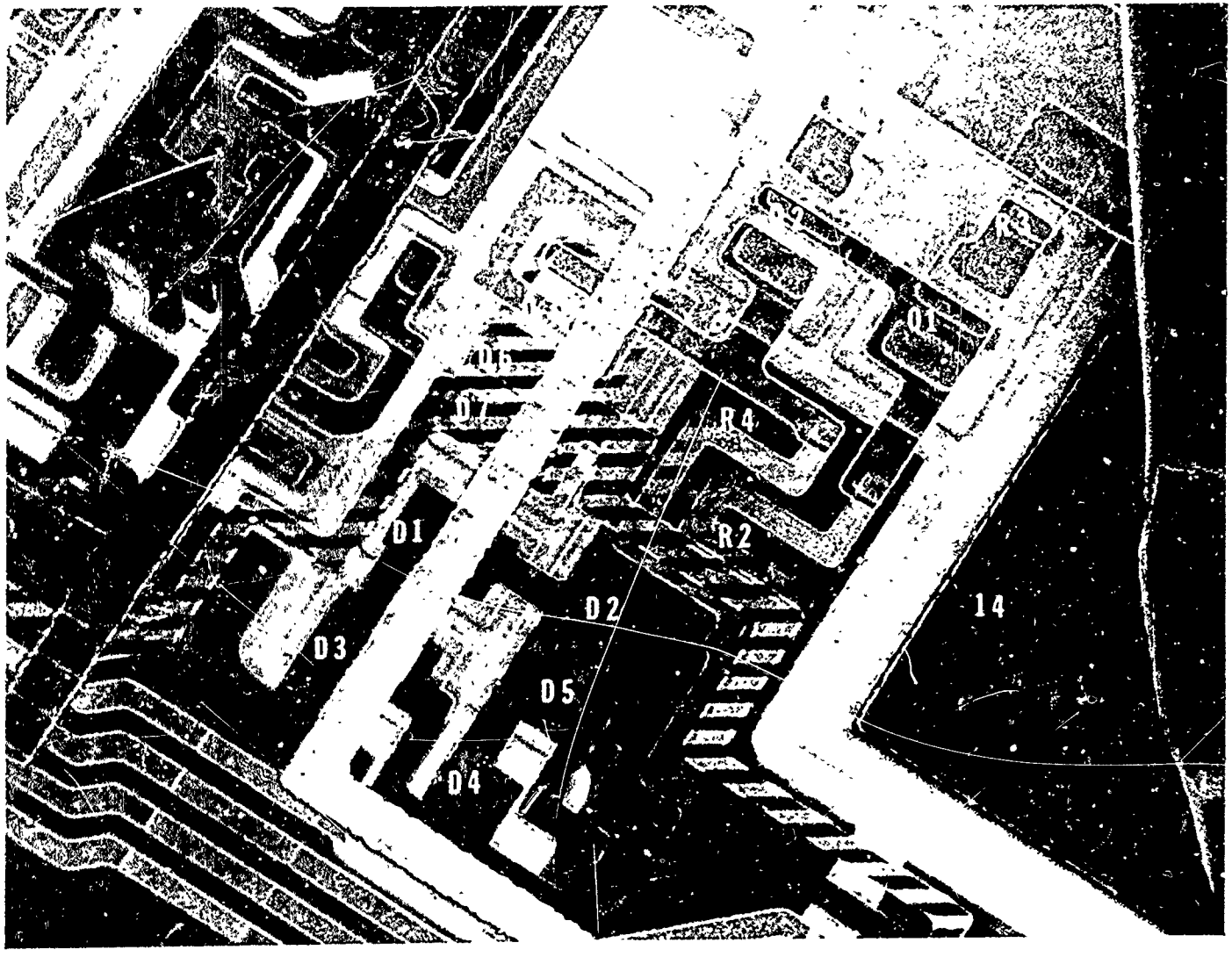


Photo 2-29 Voltage Contrast Micrograph of Master Row Decode Disable Circuit. Mag. - 700X

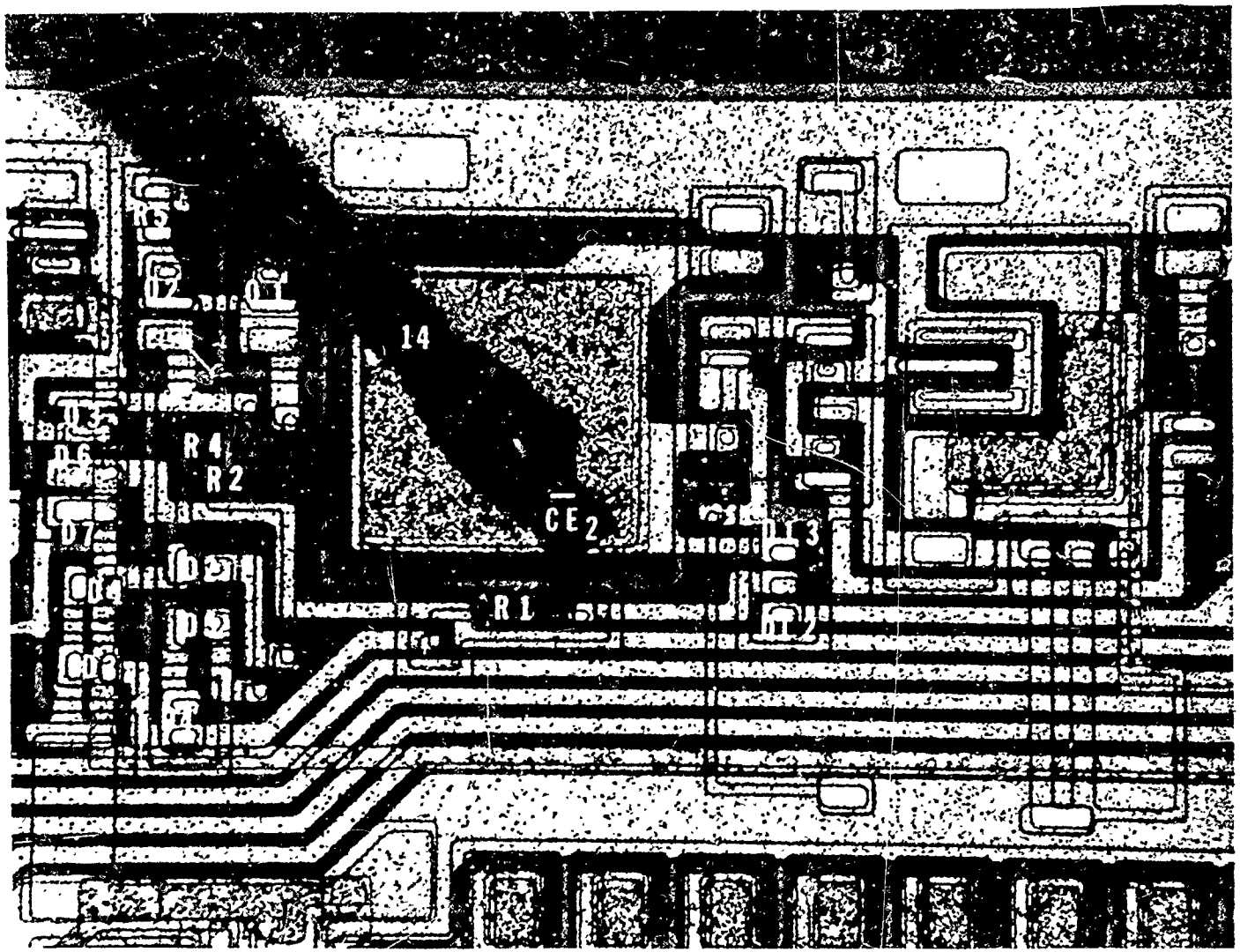


Photo 2-30 Light Photograph of the Master Row Decode Disable Circuit. Mag. - 365X

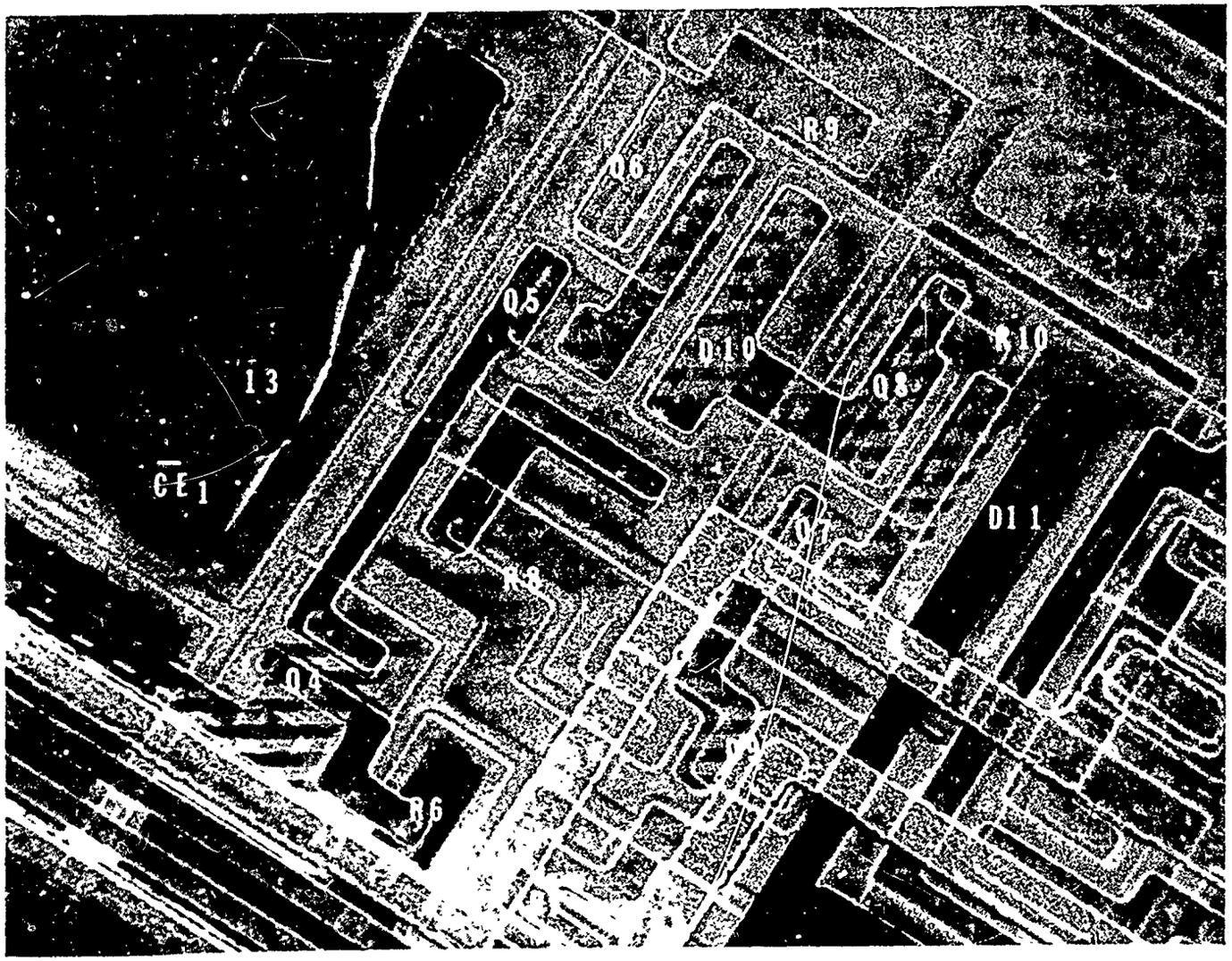


Photo 2-31 Voltage Contrast Micrograph of the Memory Program Voltage Clamp Circuit. Mag. -700X

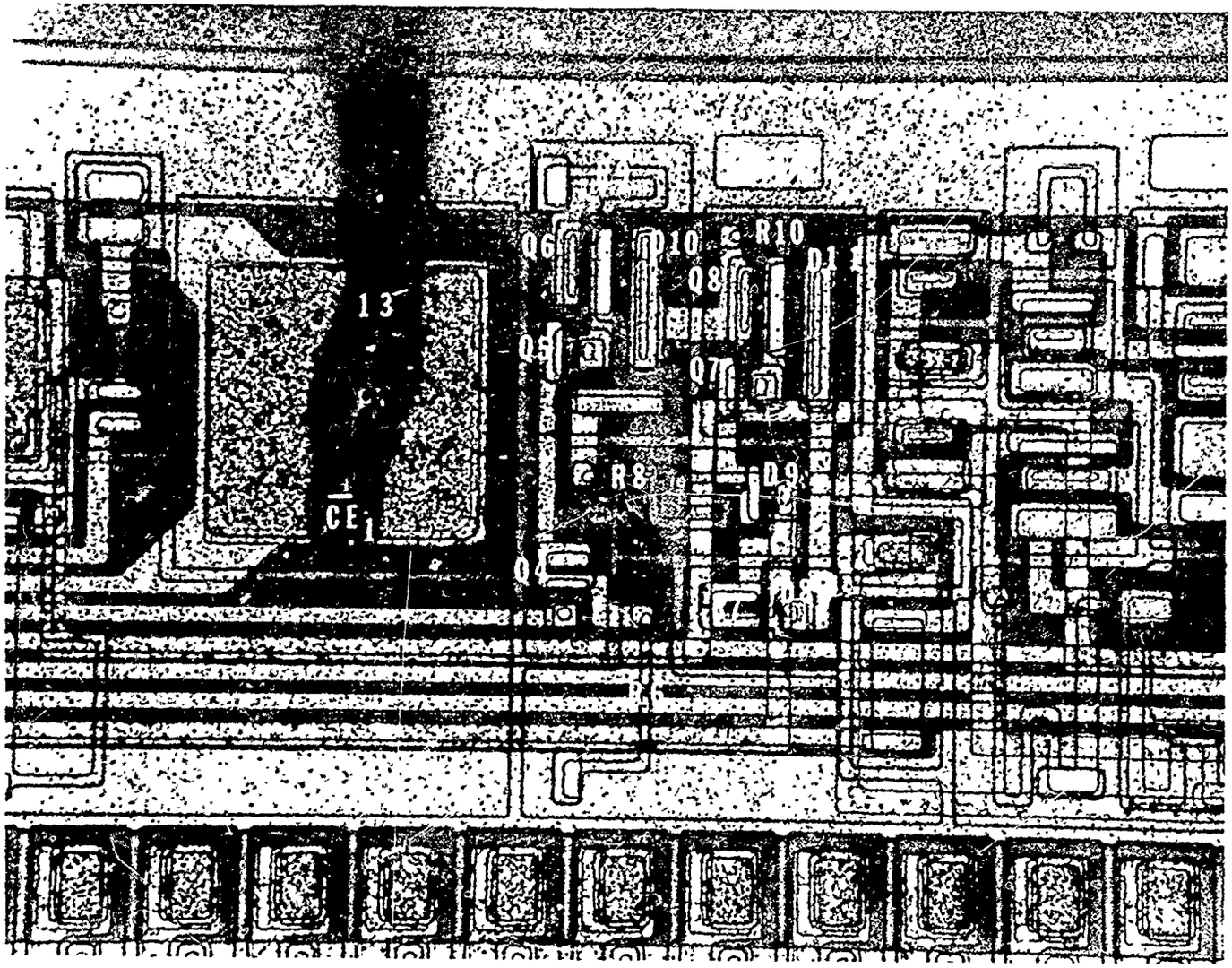


Photo 2-32 Light Photograph of the Memory Program Voltage Clamp Circuit. Mag. - 365X

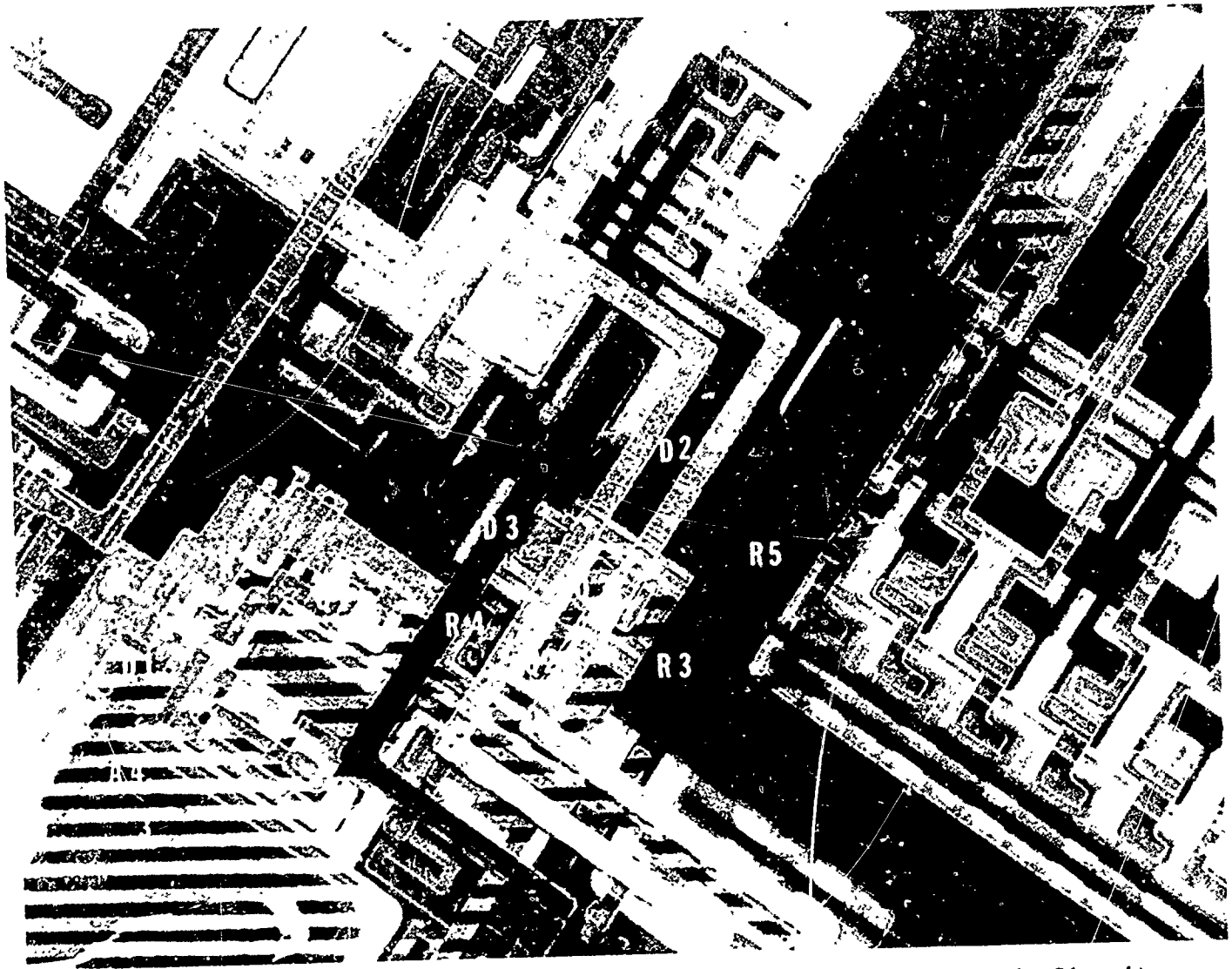


Photo 2-33 Voltage Contrast Micrograph Showing Row 33 Address and Decode Circuits. Address A4 Signal Level is Cycling Between 0 and 8 Volts. Address Row 33 is Shown in Upper Right. Mag. - 350X

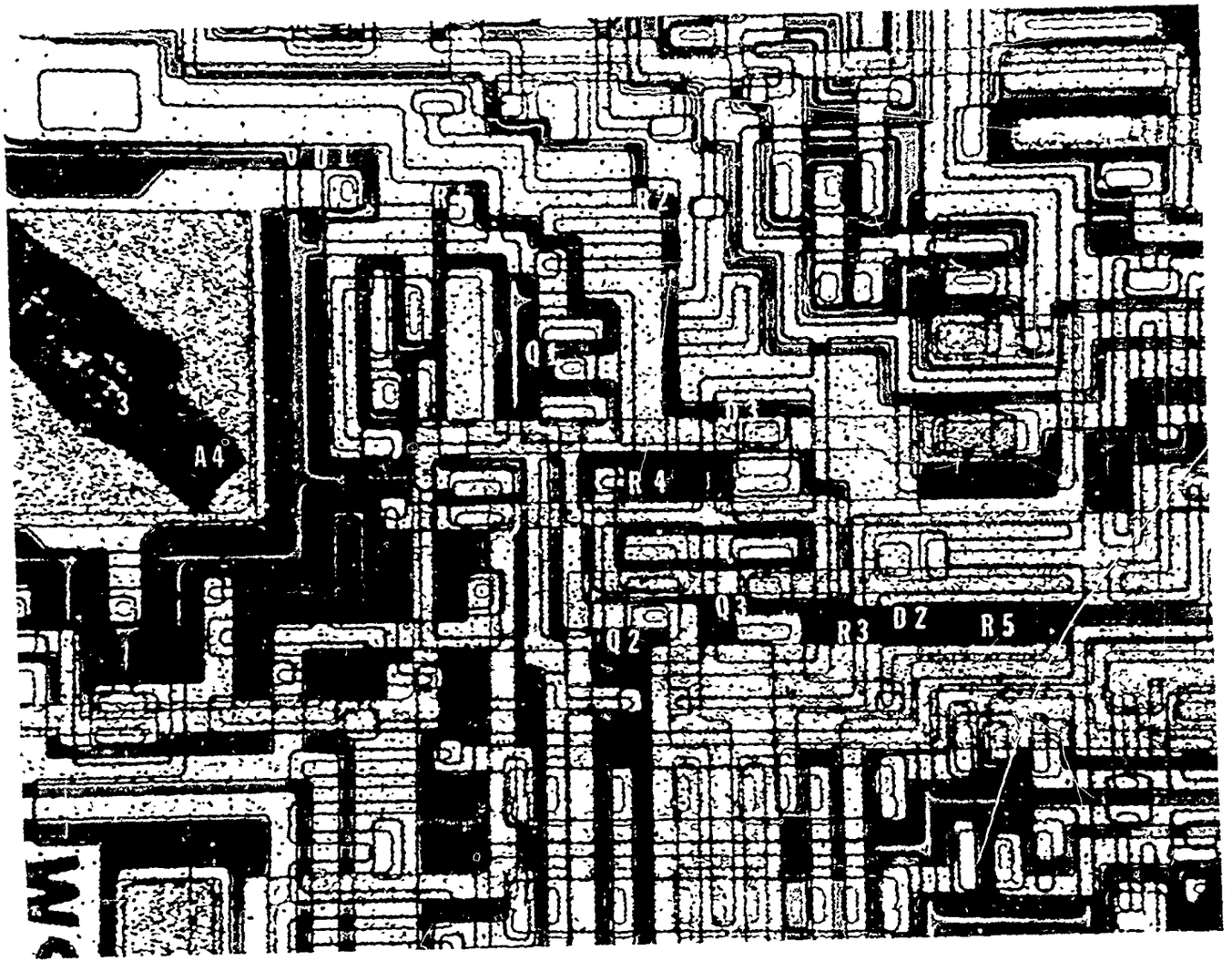


Photo 2-34 Light Photograph of Row 33 Address and Decode Circuit. Mag. - 365X

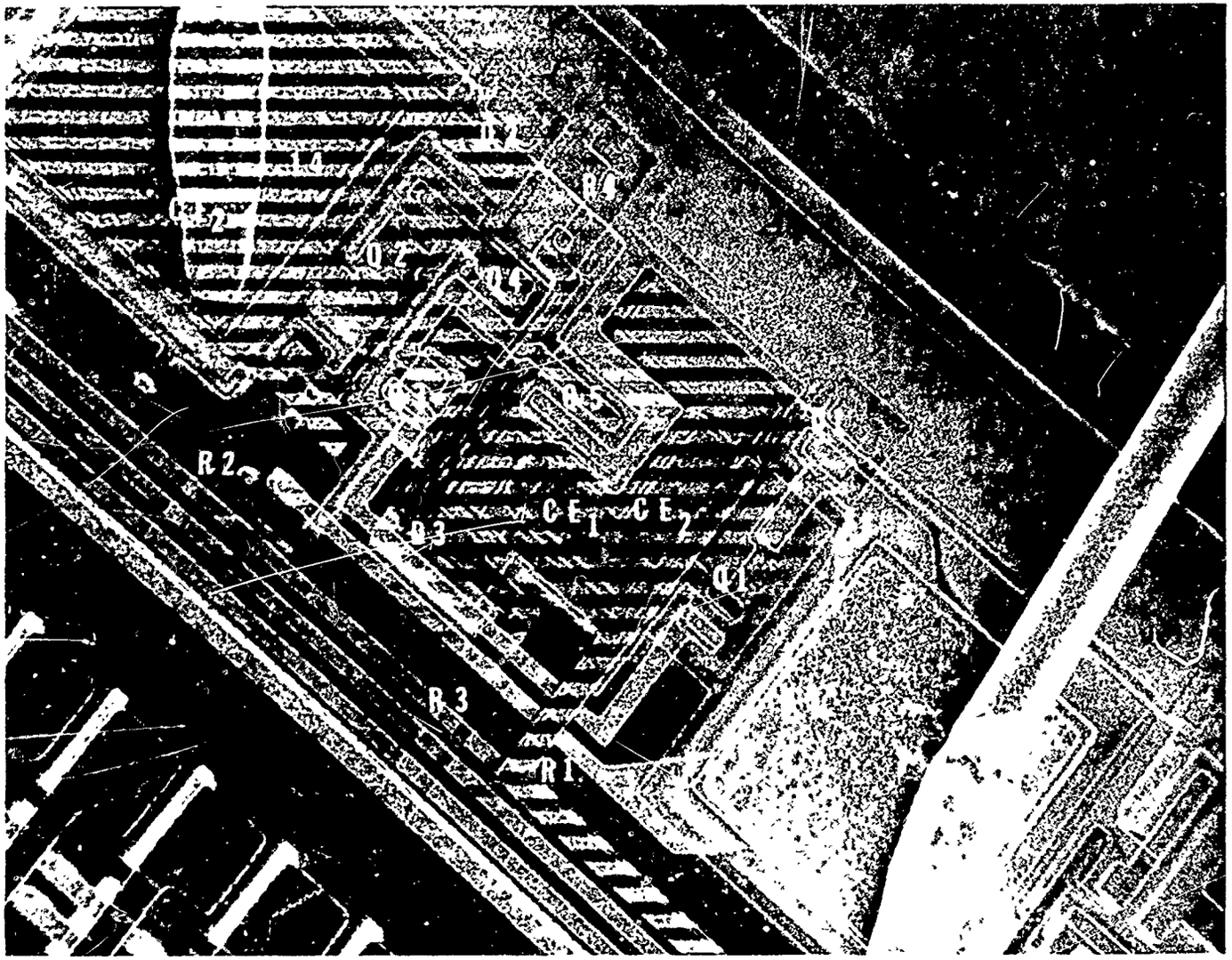


Photo 2-35 Voltage Contrast Micrograph of the Chip Enable Circuit. Mag. - 390X

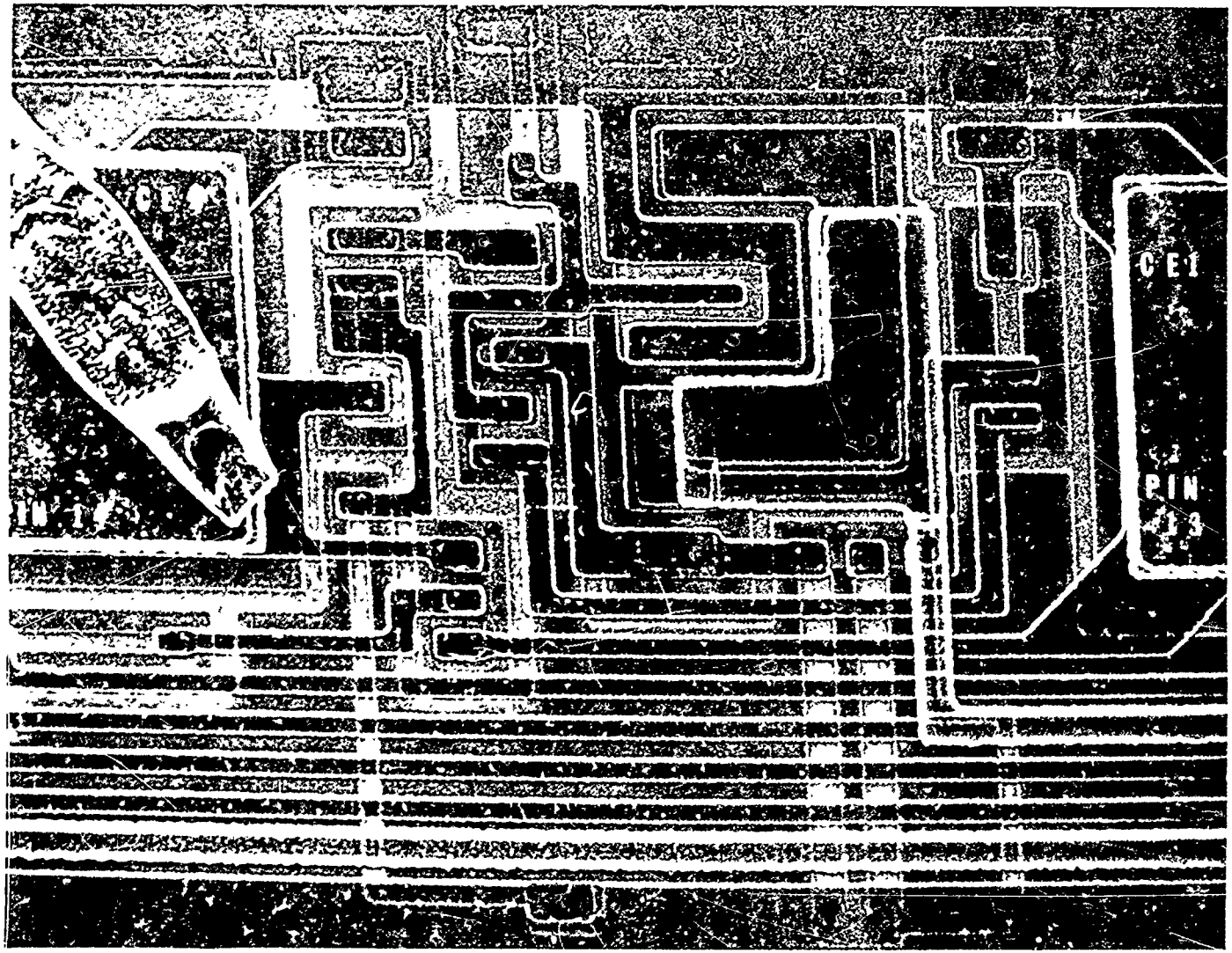


Photo 2-36 SEI Micrograph of the Chip Enable Circuit. Mag. ~ 500X

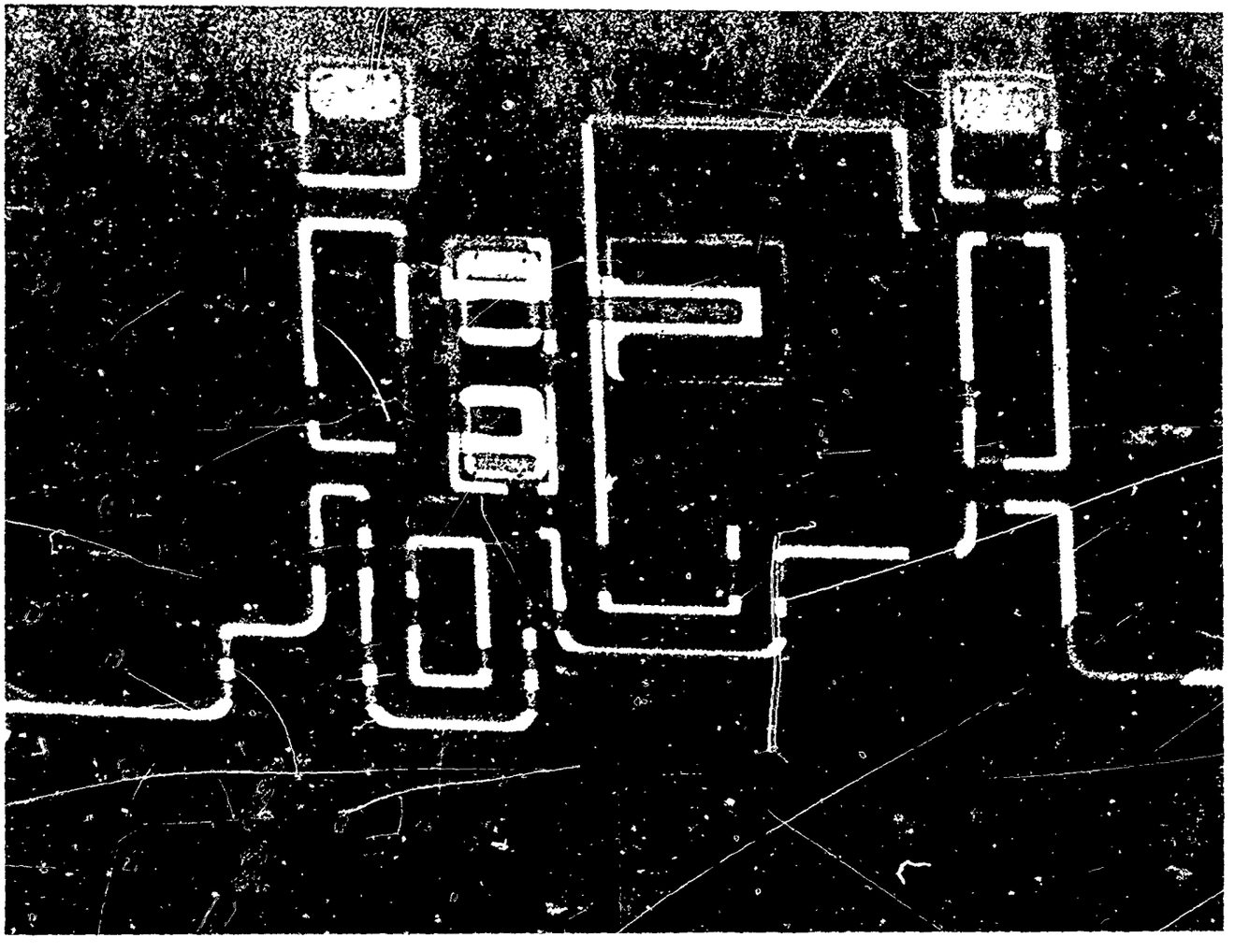


Photo 2-37 EBIC Micrograph of the Chip Enable Circuit. Mag. - 500X

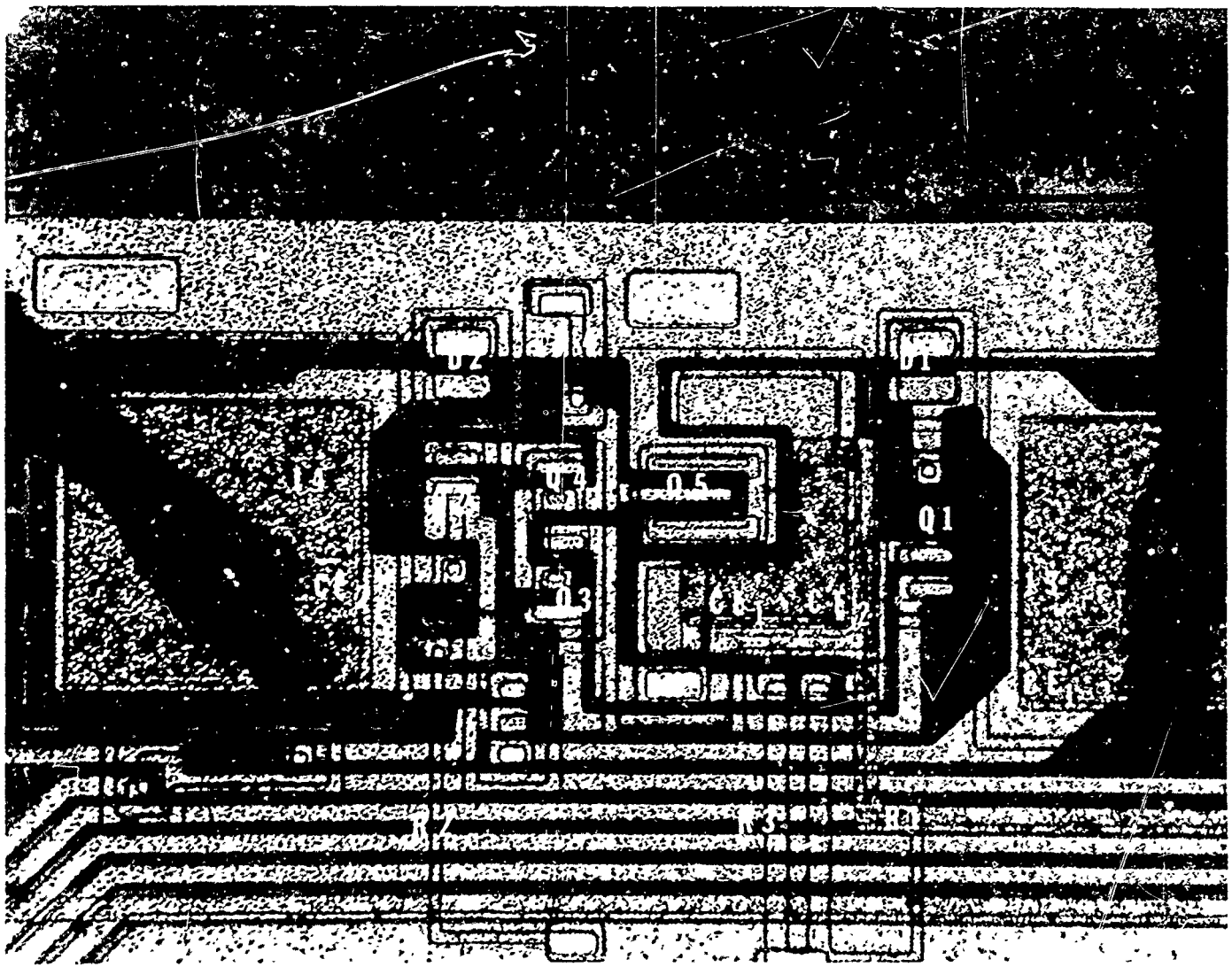


Photo 2-38 Light Photograph of the Chip Enable Circuit. Mag. - 365X

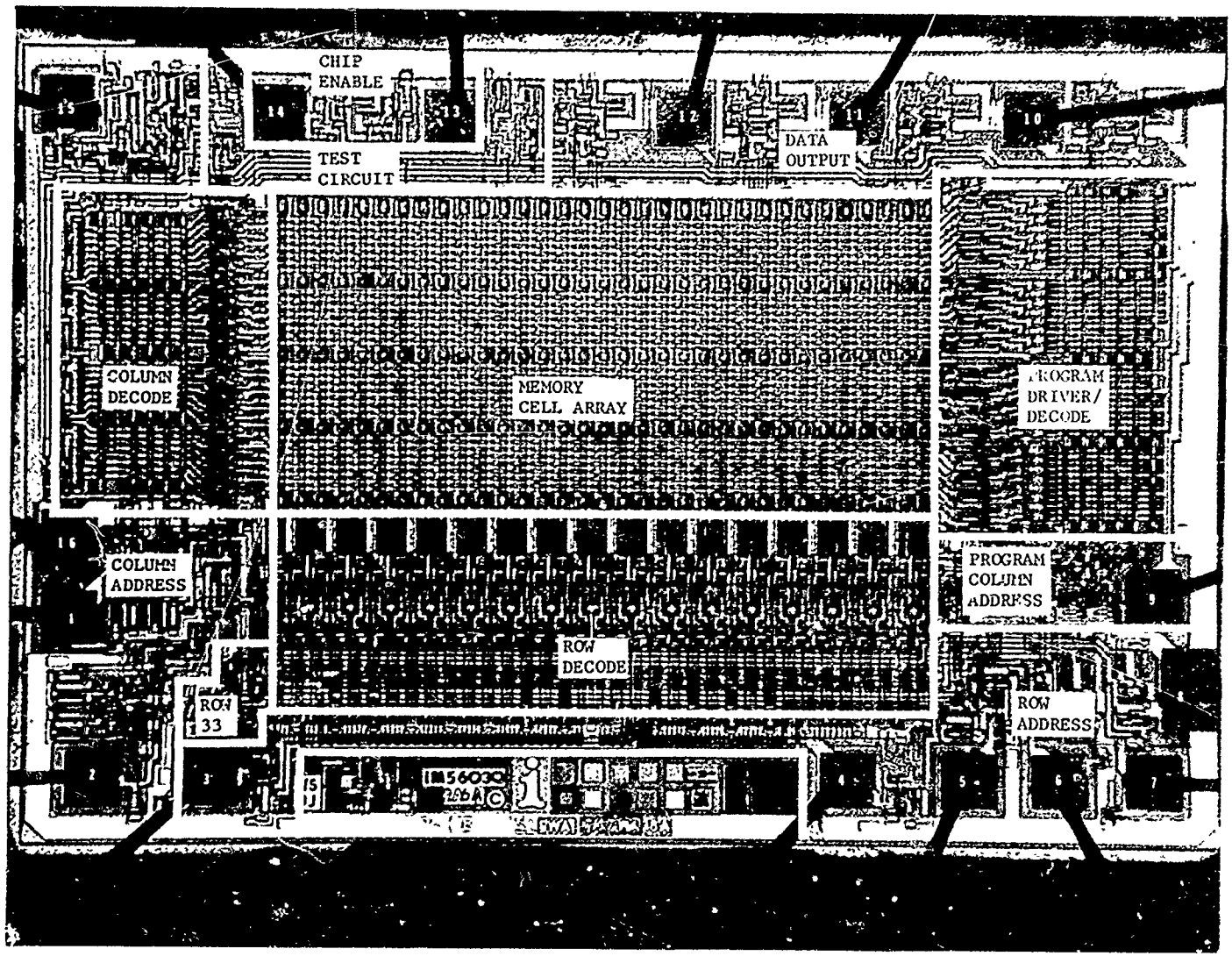


Photo 2-39 Light Photograph of Entire Chip Partitioned to Show Functional Circuit Areas. Mag. - 60X

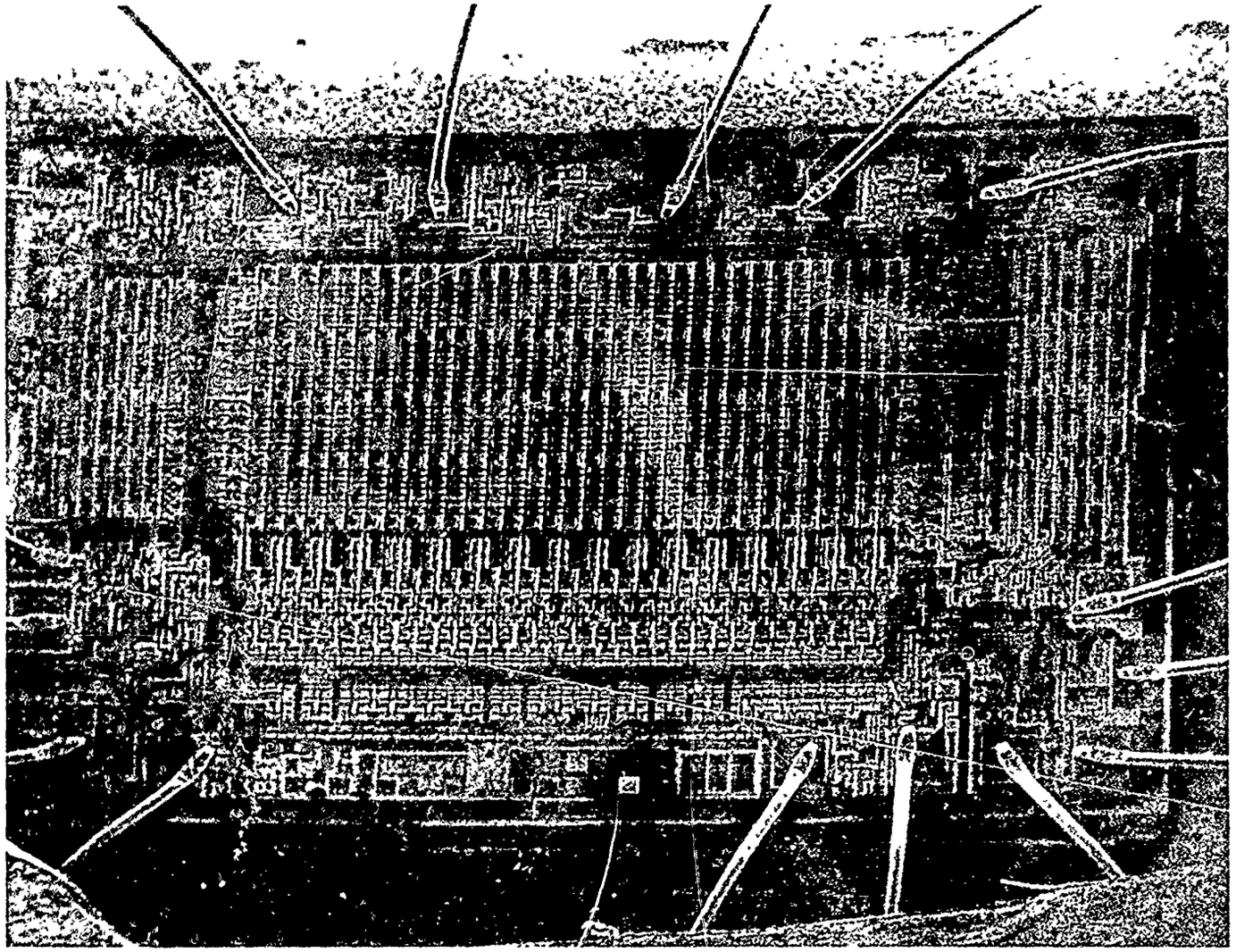


Photo 2-40 SEI Micrograph of Entire Chip. This Provides a Visual Reference for EBIC Photos 2-41 and 42. Mag. - 75X

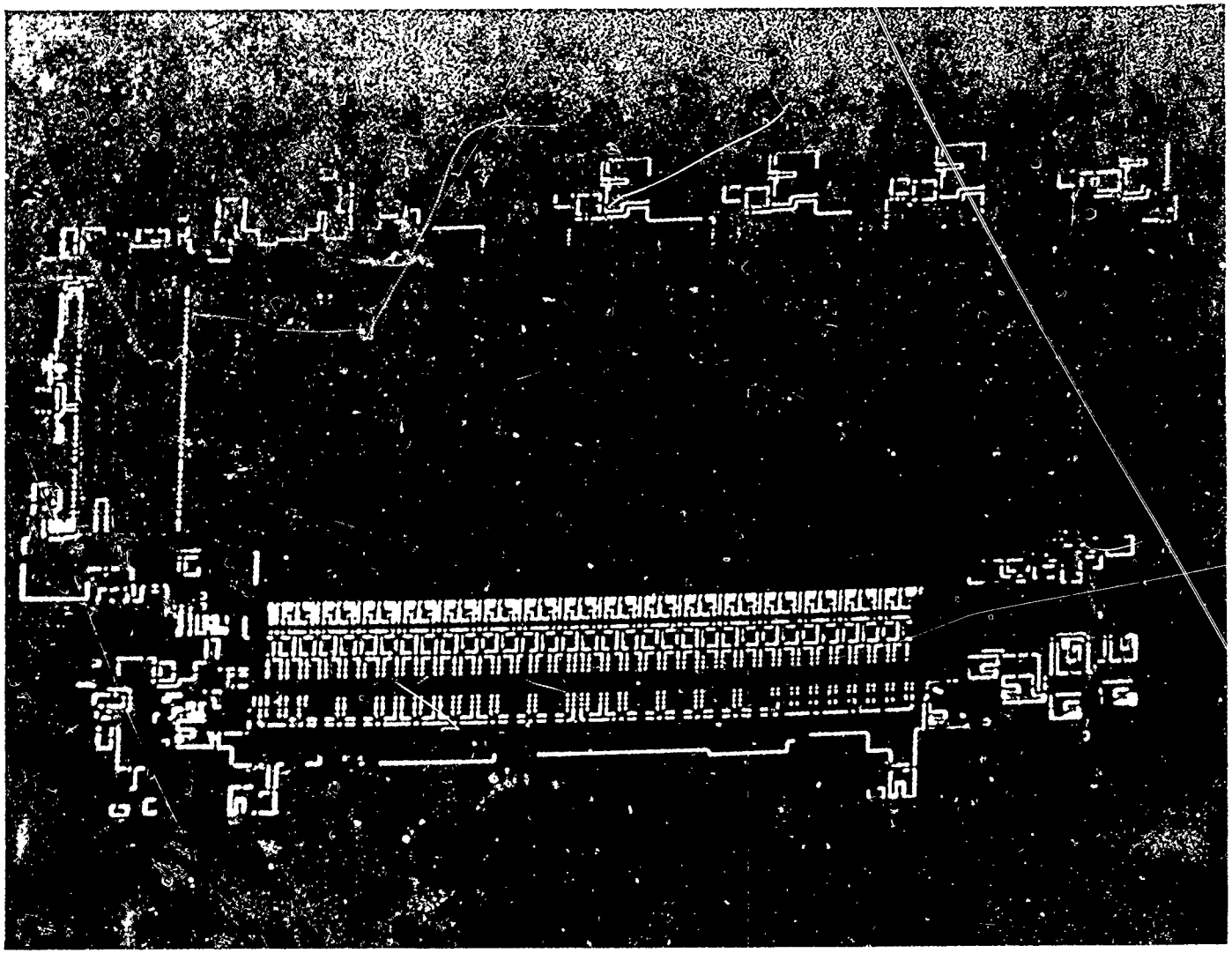


Photo 2-41 EBIC Micrograph of the Entire Chip. Beam Voltage is 10 KV. Mag. - 75X

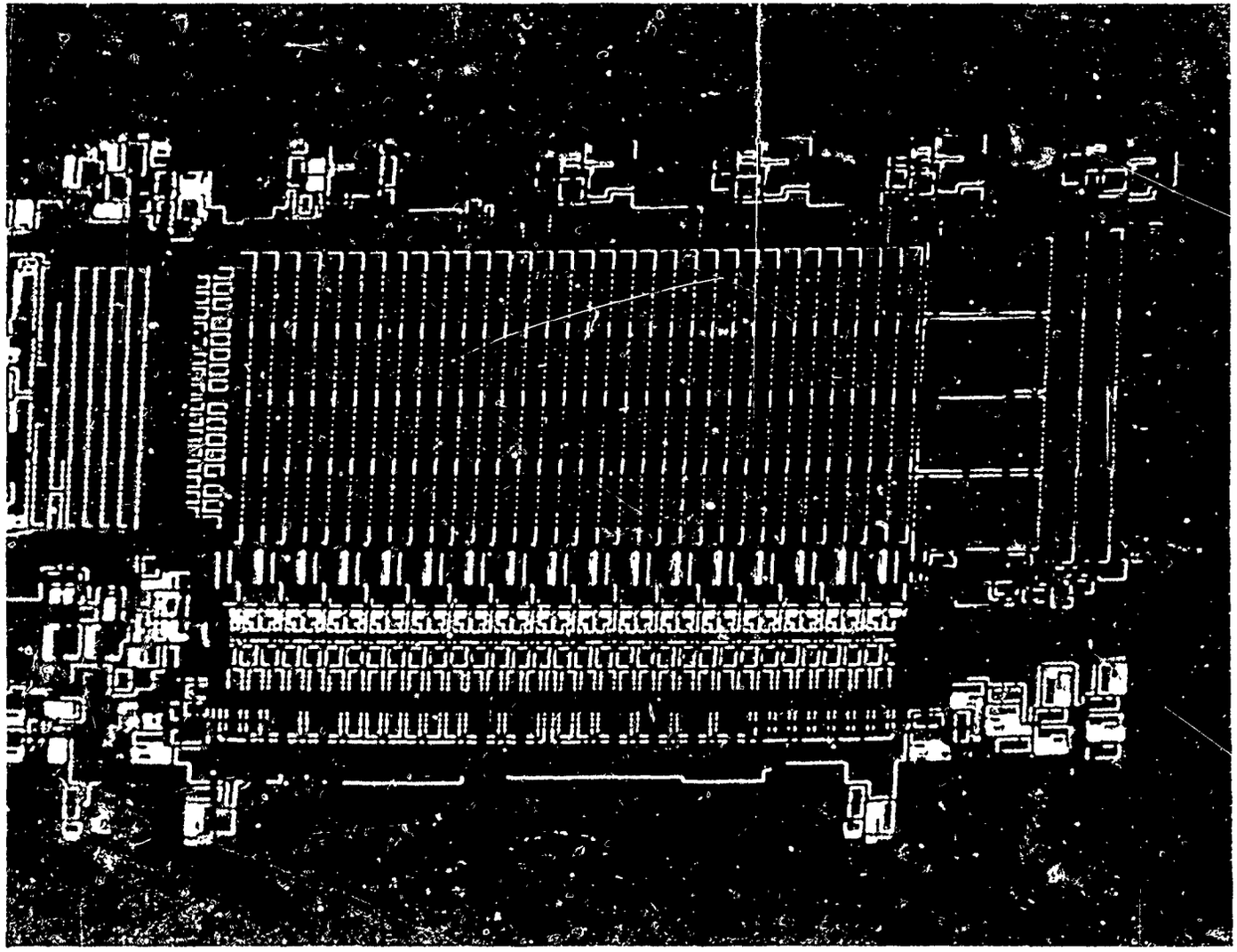


Photo 2-42 ESIC Micrograph of the Entire Chip. Beam Voltage is 15 KV. Mag. - 78X

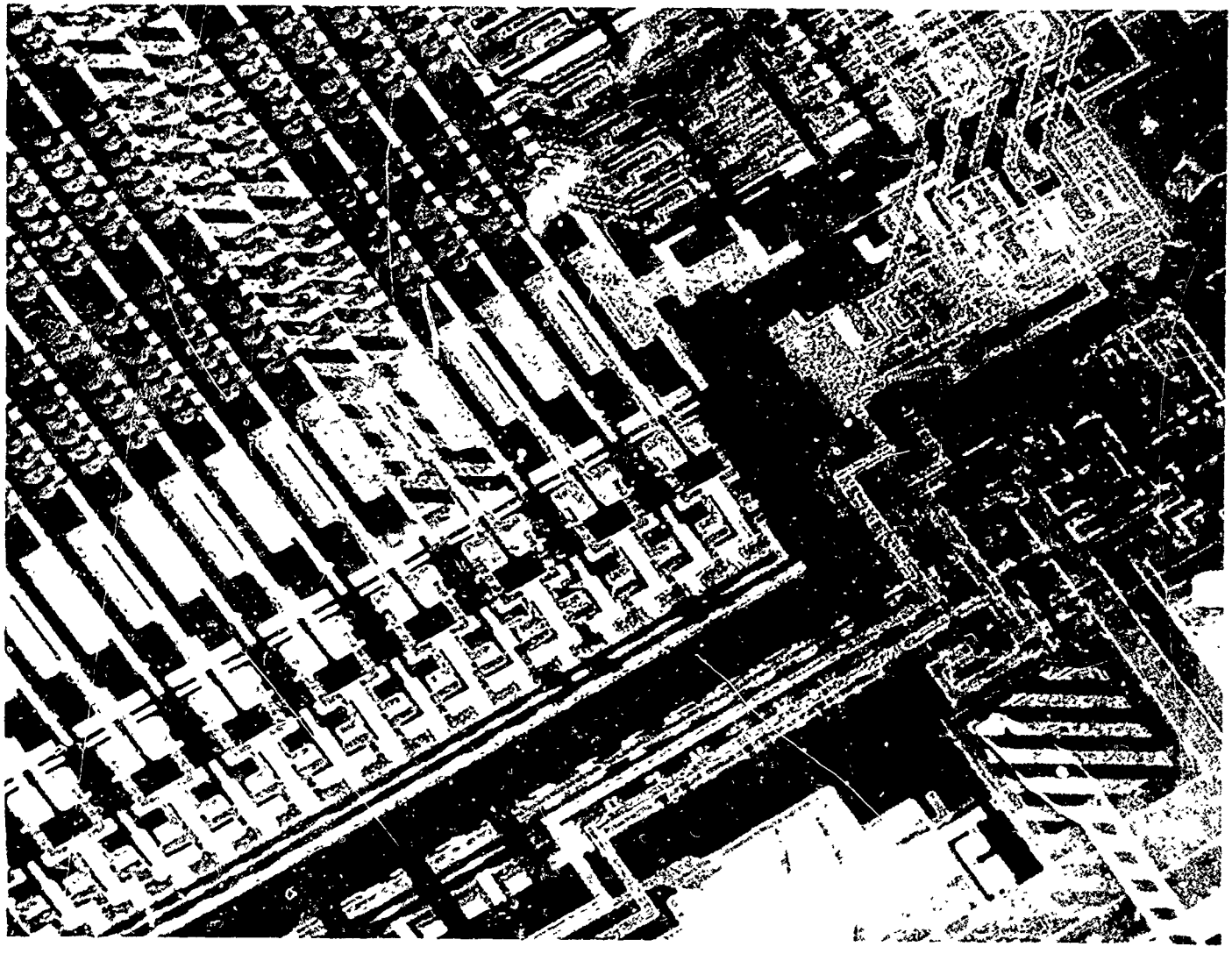
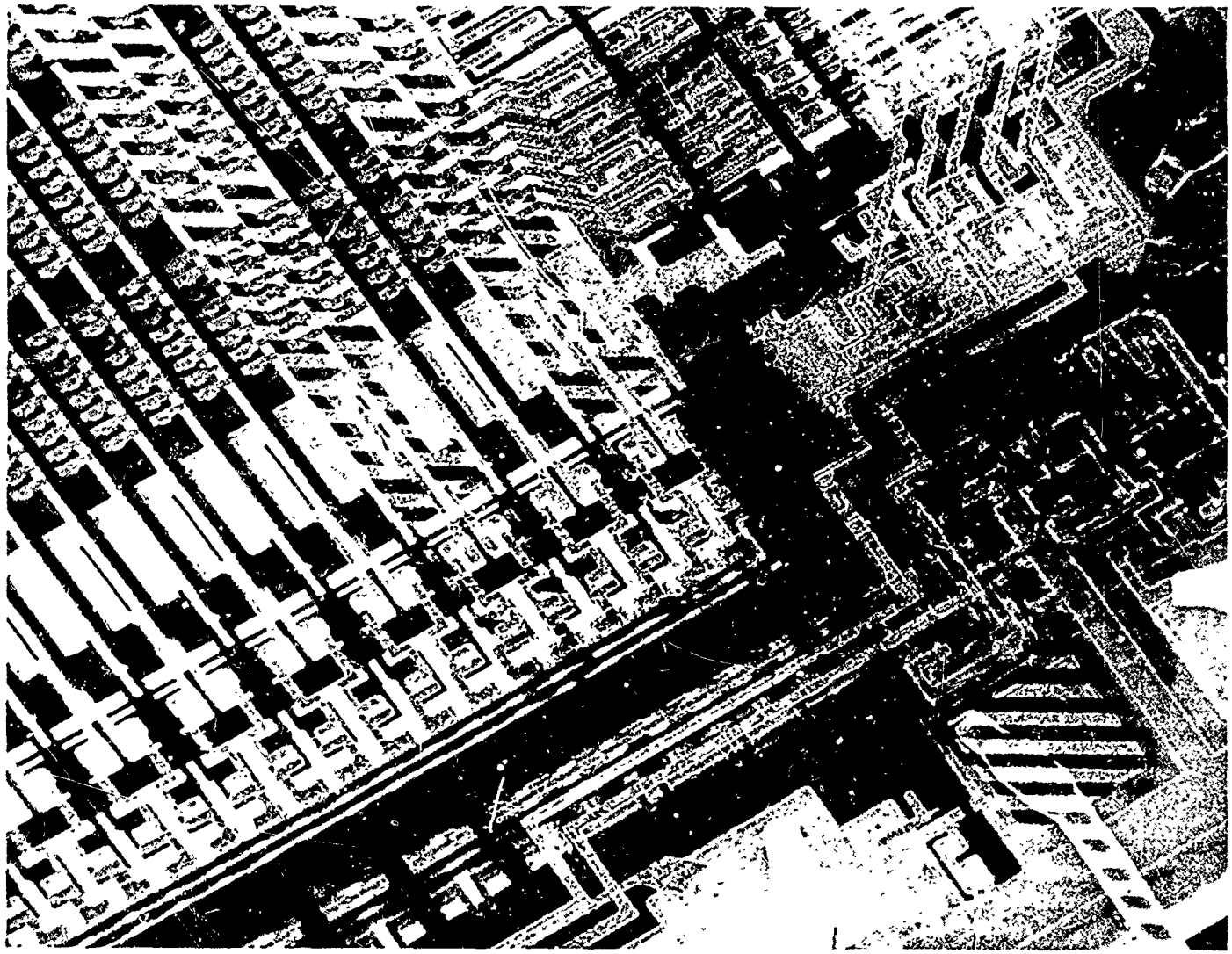


Photo 2-43 Voltage Contrast Micrograph with Circuit Cycling Between Addresses 4 and 5. Memory Rows 4 and 5 are Being Addressed. Mag. - 170X



Pnoto 2-44 Voltage Contrast Micrograph with Circuit Cycling Between Addresses 0 and 1 A Failure is Apparent as Memory Rows 0 and 4 and 1 and 5 are Being Addressed Simultaneously. Mag. - 170X

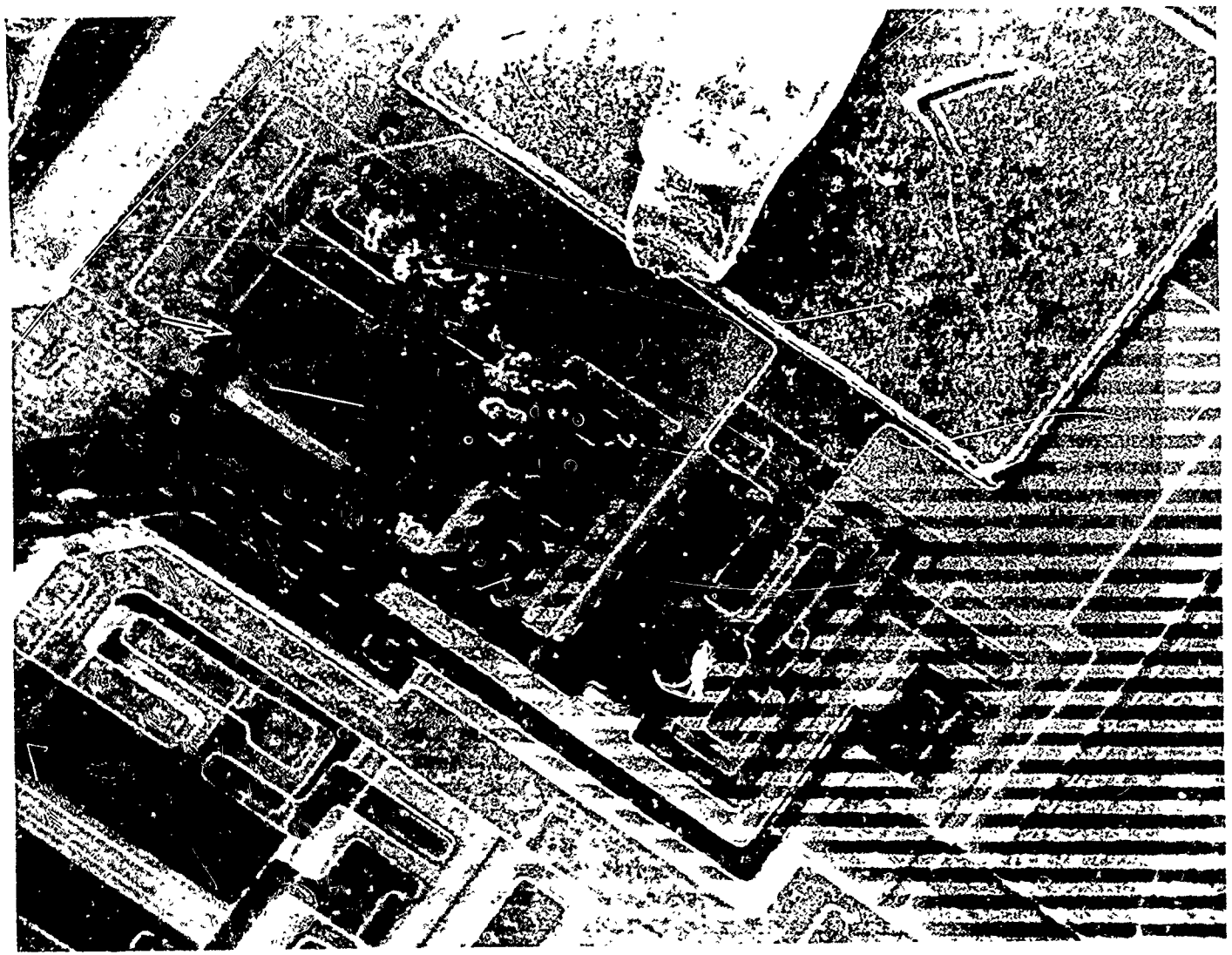


Photo 2-45 Voltage Contrast Micrograph of Row Address Inverter A2. Cycling the A2 Input Fails to Provide a Cycling A2 Address Output (Arrow). This Line Remains High. Mag. - 620X

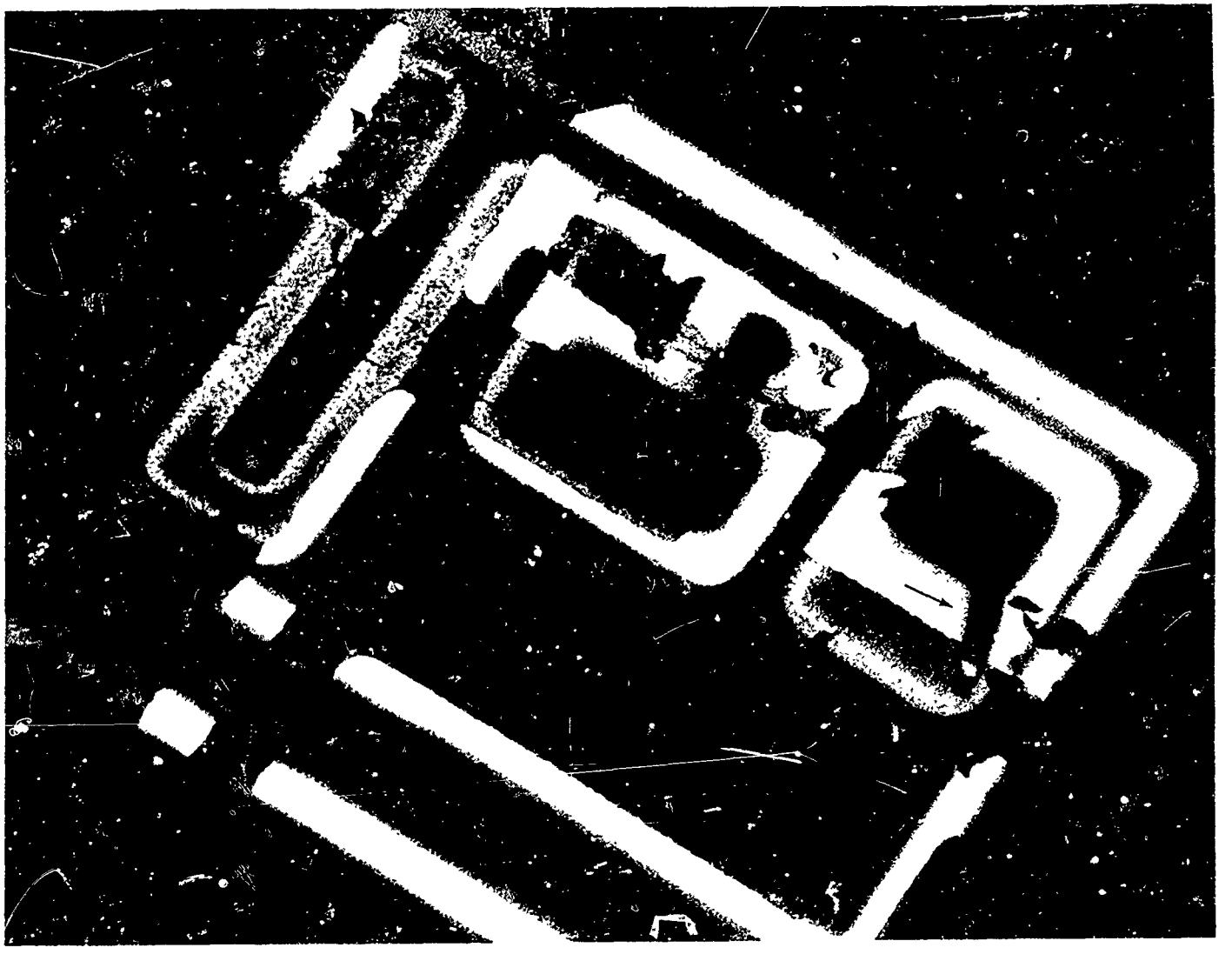


Photo 2-46 EBIC Micrograph of Transistors Q5 and Q6 in the A2 Row Address Inverter. An Emitter-Base Short is Shown by Arrow. Mag. - 1550X

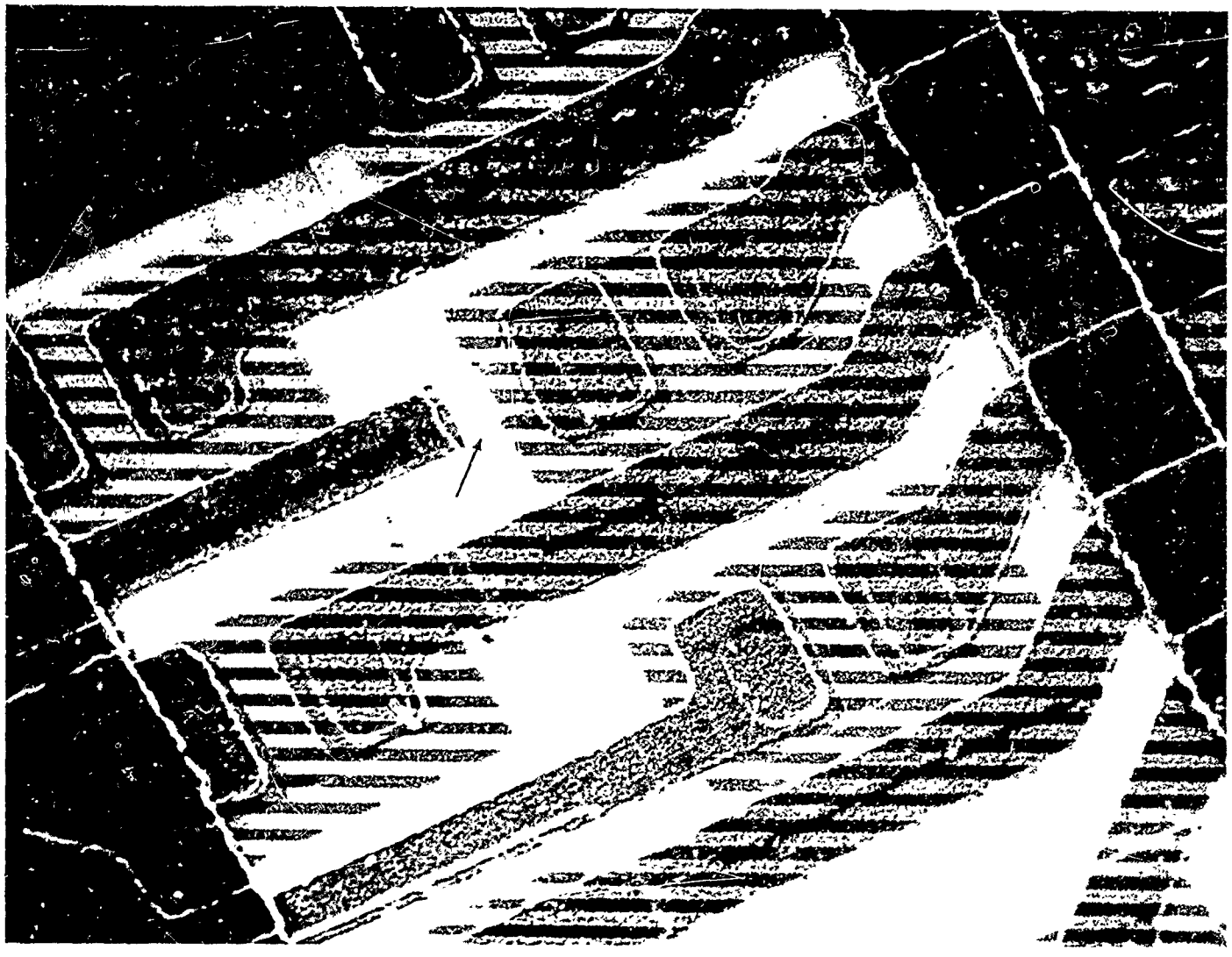


Photo 2-47 Voltage Contrast Micrograph Showing an Open Metallization Stripe at the Anode of Diode D3 (Arrow). Mag. - 1550X

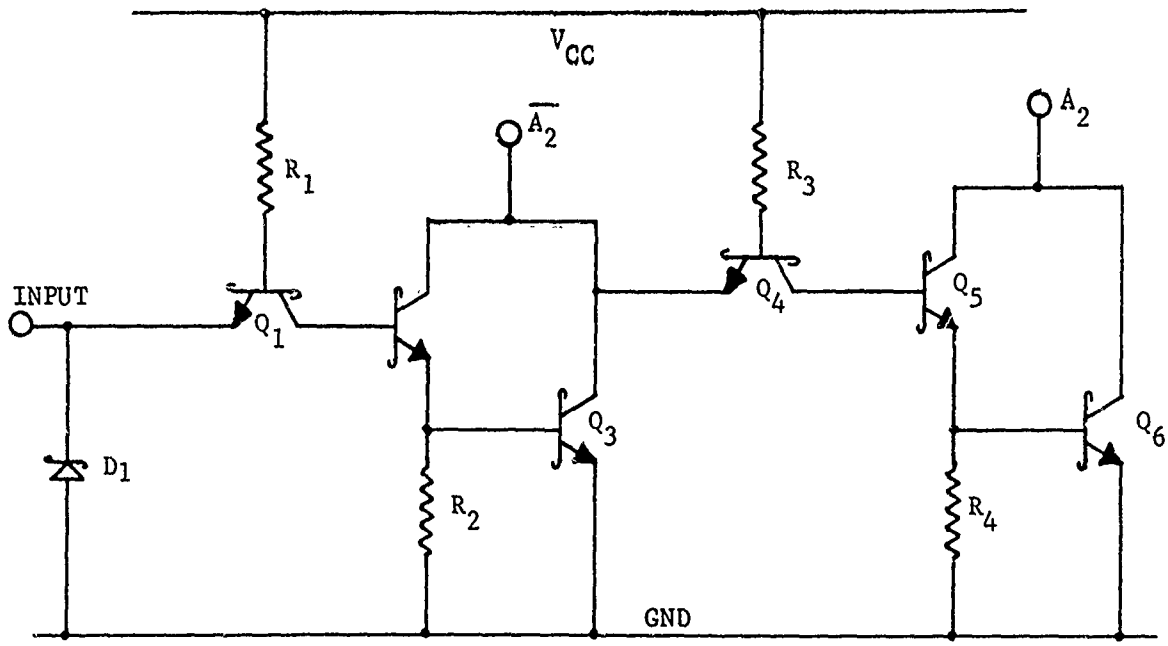


Figure 2-1 Schematic, Row Address Inverter(A2).

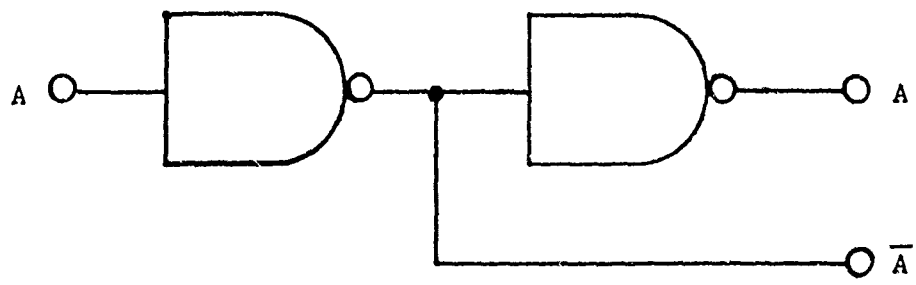


Figure 2-2 Logic Diagram, Row Address Inverter.

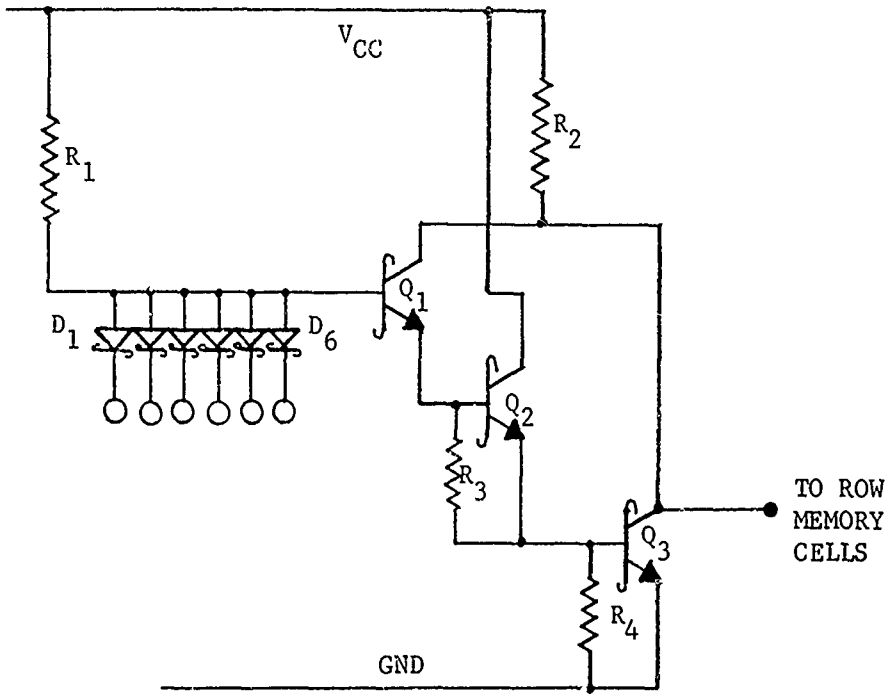


Figure 2-3 Schematic, 1 of 32 Row Address Decoder

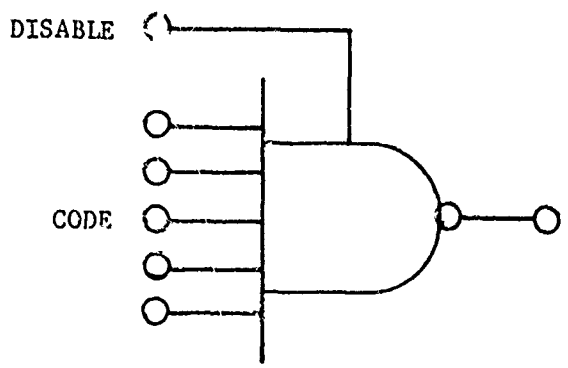


Figure 2-4 Logic Diagram, 1 of 32 Row Address Decoder

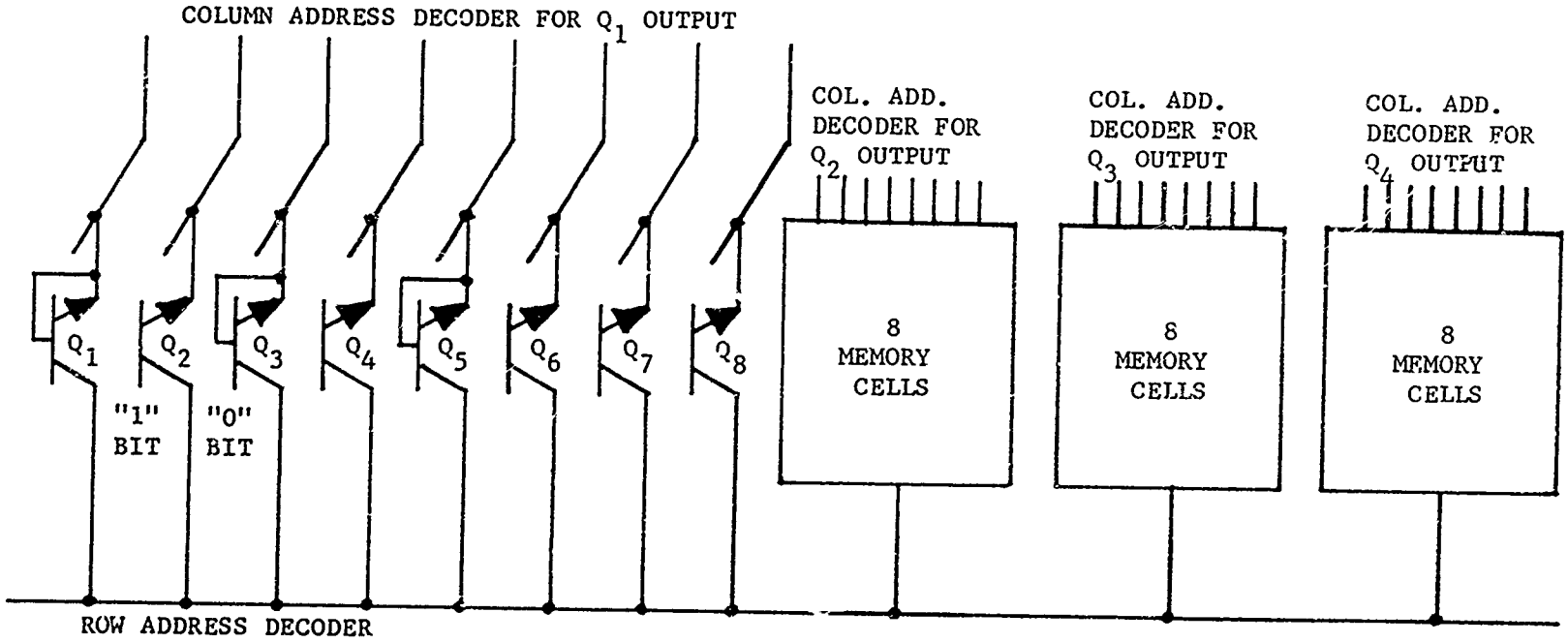


Figure 2-5 Schematic, Memory Cells

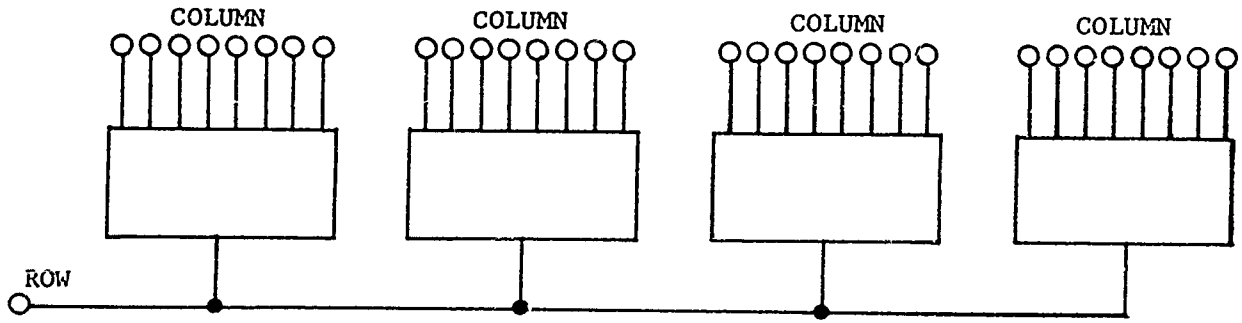


Figure 2-6 Logic Diagram, Memory Cells

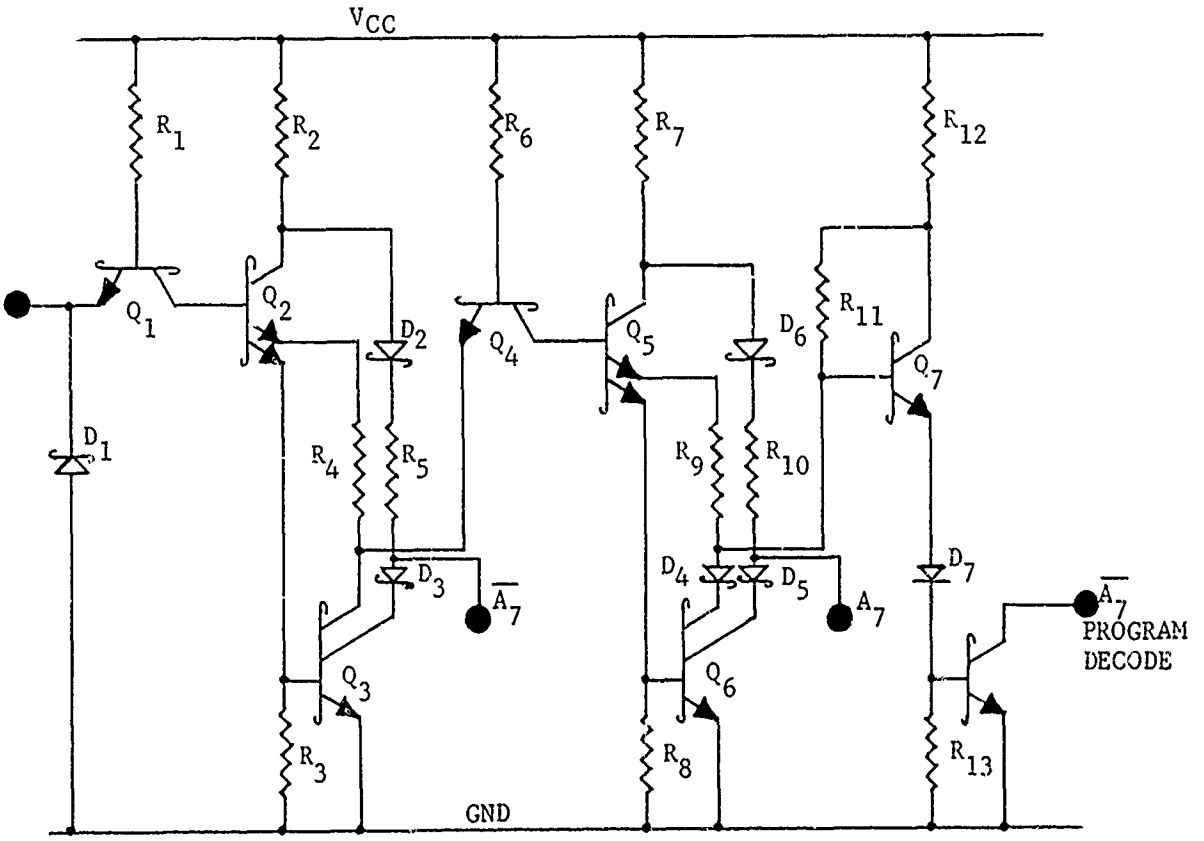


Figure 2-7 Schematic, Column Address Inverter (A7)

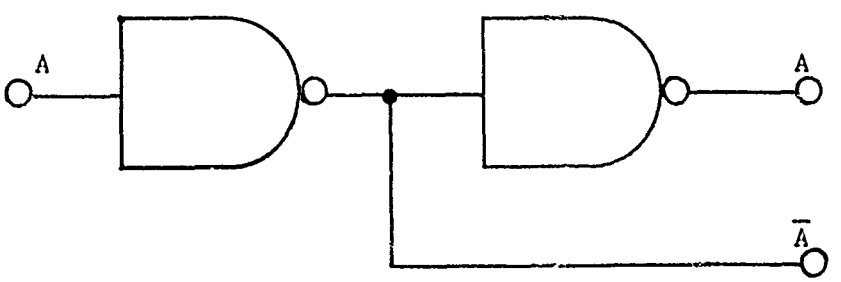


Figure 2-8 Logic Diagram, Column Address Inverter

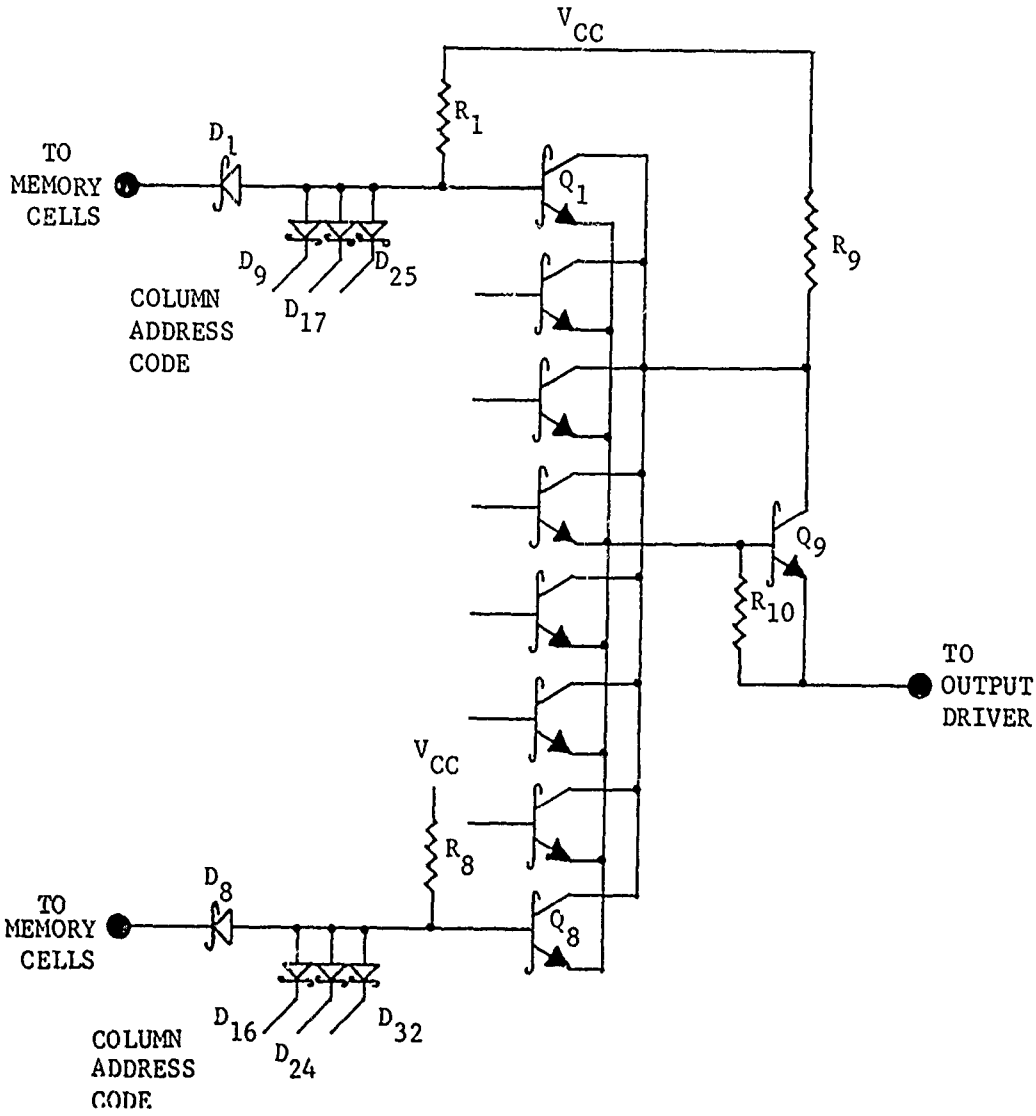


Figure 2-9 Schematic, 1 of 8 Decoder and Sense Amplifier

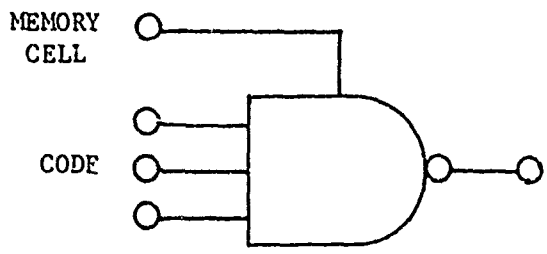


Figure 2-10 Logic Diagram, 1 of 8 Column Decoder

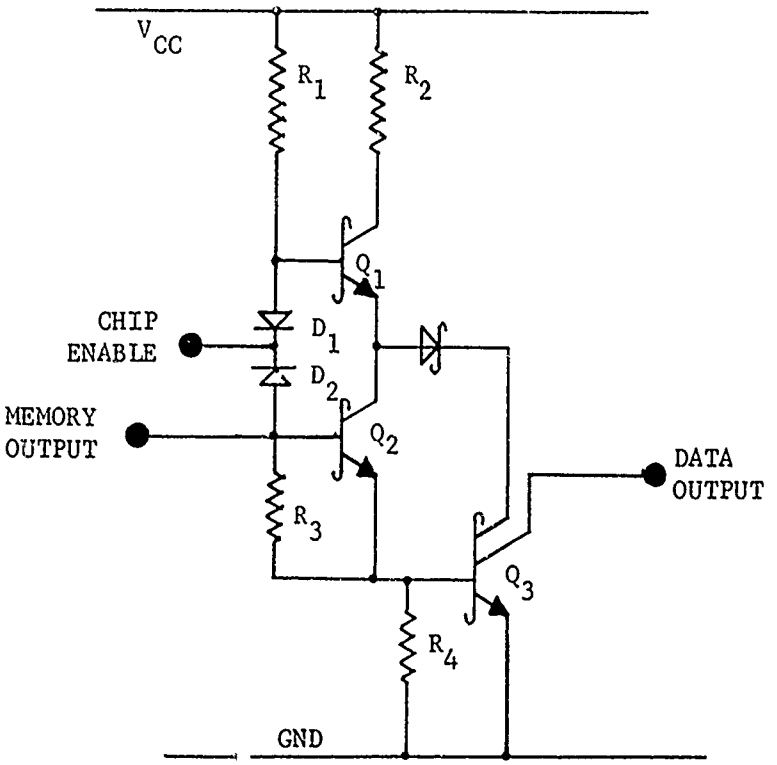


Figure 2-11 Schematic, Data Output Buffer

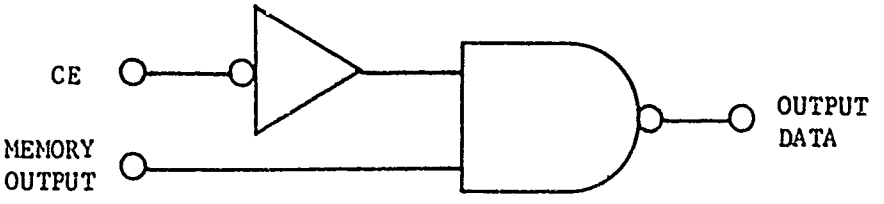


Figure 2-12 Logic Diagram, Data Output Buffer

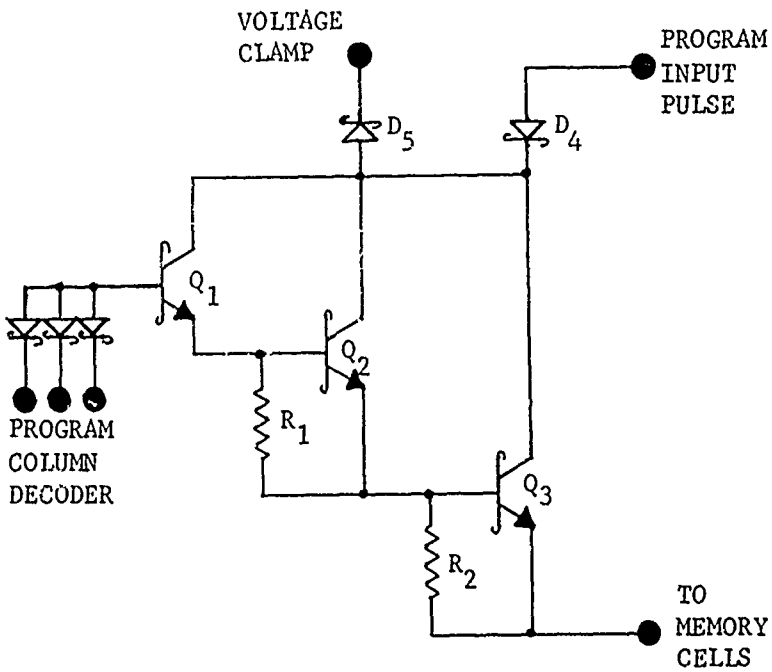


Figure 2-13 Schematic, Memory Program Column Decoder/Driver

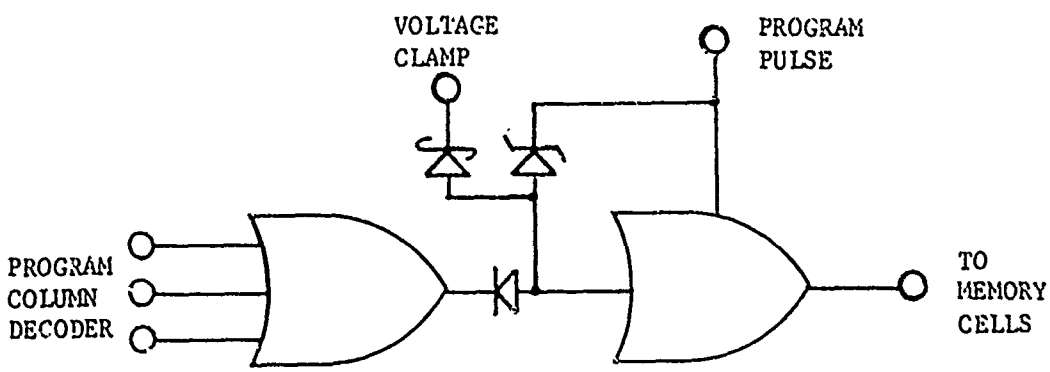


Figure 2-14 Logic Diagram, Memory Program Decoder/Driver

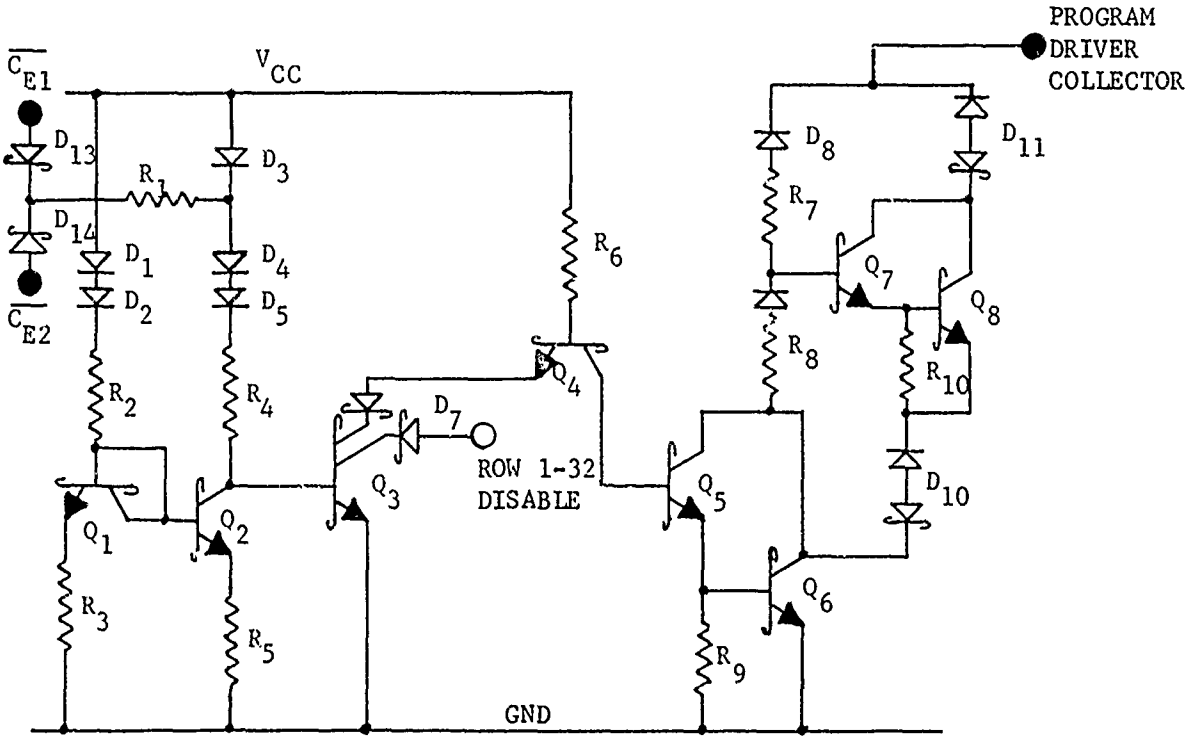


Figure 2-15 Schematic, Test Circuit Disable

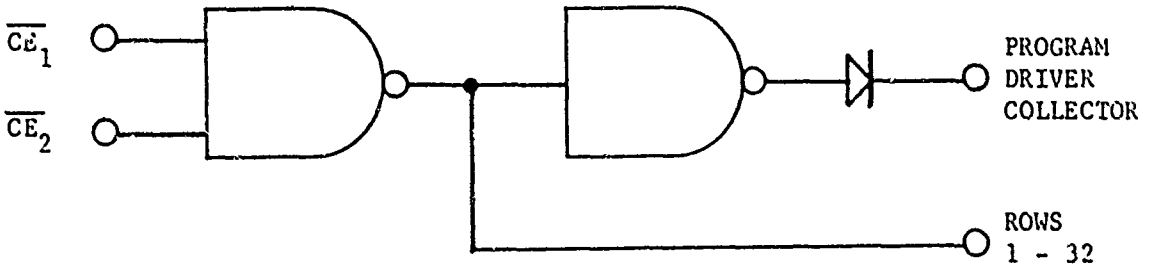


Figure 2-16 Logic Diagram, Test Circuit Disable

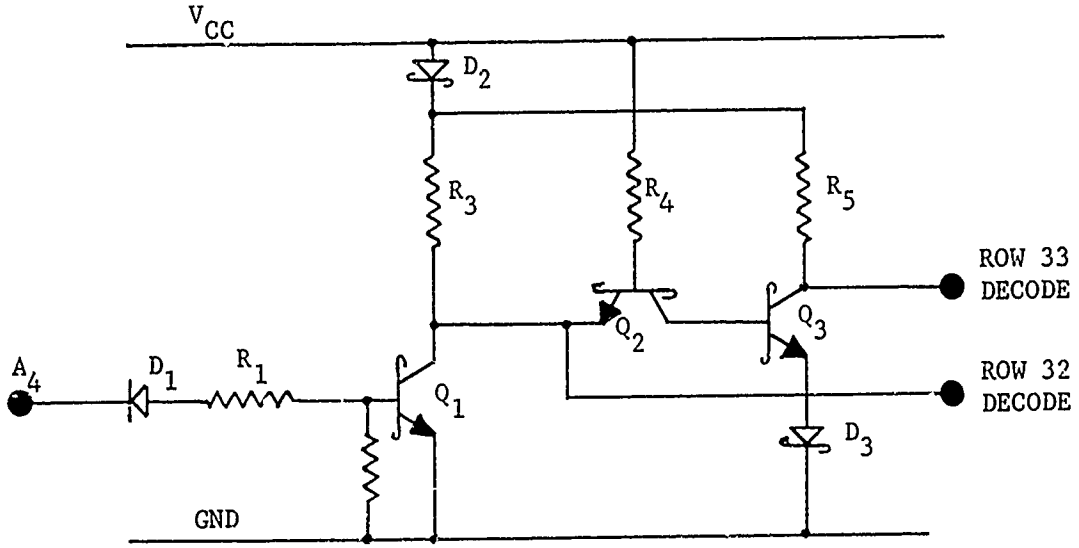


Figure 2-17 Schematic, Row 33 Address (A4 > 7 V)

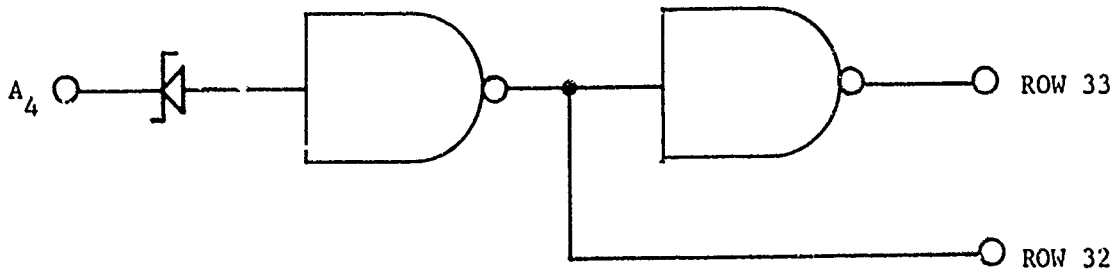


Figure 2-18 Logic Diagram, Row 33 Address Inverter

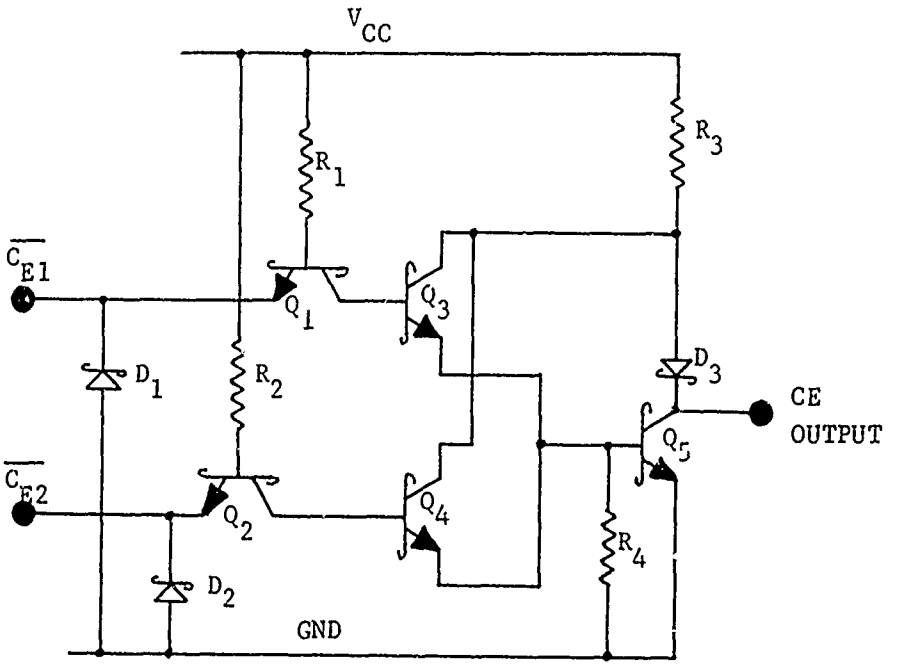


Figure 2-19 Schematic, Chip Enable

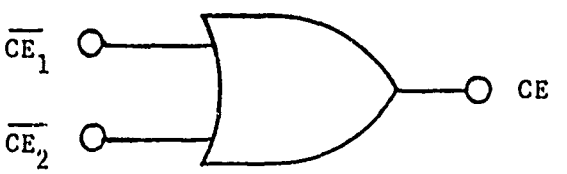


Figure 2-20 Logic Diagram, Chip Enable

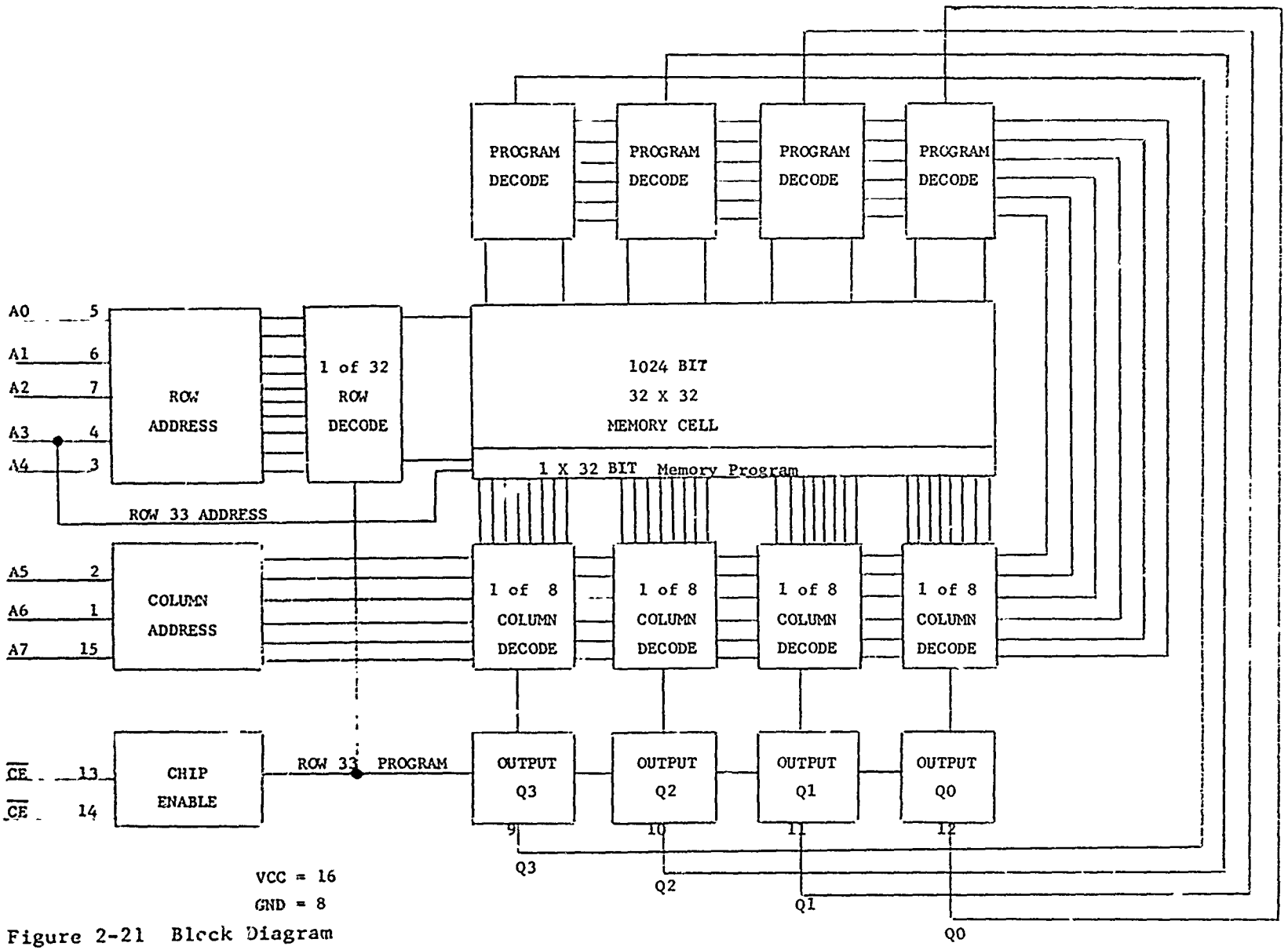


Figure 2-21 Block Diagram

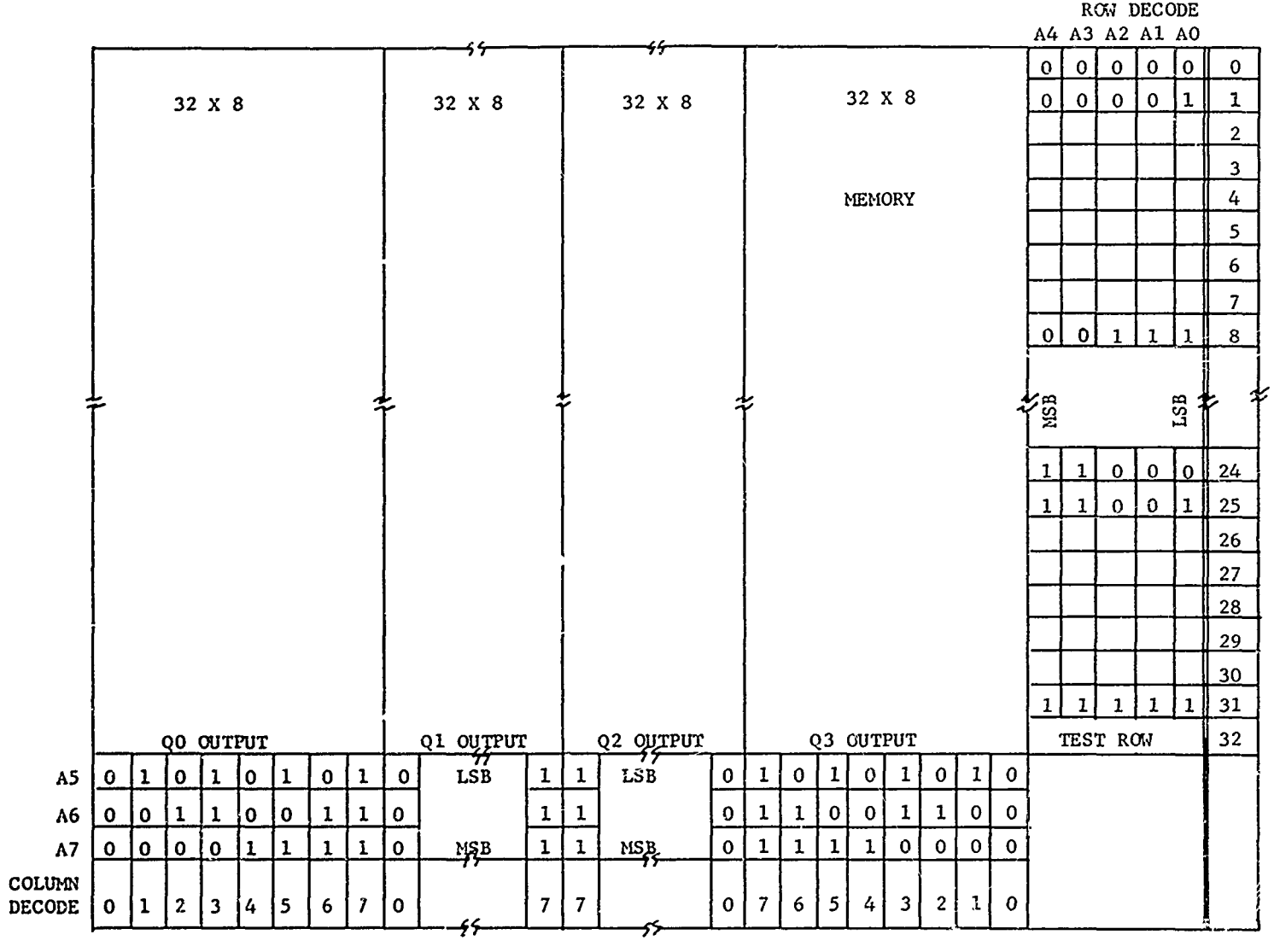


Figure 2-22 Bit Map

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4.3 16384 BIT EPROM (SiGATE NMOS)

UV Erasable PROM

This device is a 2048 x 8 bit silicon gate NMOS ultra-violet light-erasable, electrically programmable read only memory. The outputs are three-state on this device. The package is a 24-pin dual-in-line ceramic package with a transparent lid to allow the device to be erased.

Electrical Characterization

Ten devices of this part type were used for this program. These were serialized and tested in accordance with the suppliers data sheet. Eight of these devices were found to be electrically good and their measurements are shown in Table 3-1.

These devices were then functionally tested as follows. There are 11 input pins and 8 output pins on the devices, so there are 2^{11} possible input words and 2^8 possible output combinations. Therefore, a given word will be used 2^3 times. Two separate bit patterns were written into these devices to fully test each bit. The first pattern was A_0 thru A_7 equal to Q_0 thru Q_7; i.e., the pattern went from 00 to FF eight times. The second pattern was A_3 thru A_{10}, equal to Q_0 thru Q_7; i.e., the pattern was 00 eight times up to FF eight times. Following programming, the data which was written into the devices was verified on the programming equipment. This equipment was a Motorola 6800 Exerciser with a PROM program card. In addition to the programming equipment, the Hewlett-Packard Model 1610A Logic Analyzer was used to monitor the circuit during examination in the SEM.

Package Delid and Glass Passivation Removal

This device is in a 24-pin dual-in-line ceramic package with a transparent window above the die. To open, the window was ground down by using a diamond impregnated wheel. When this window was quite thin, a blade was used to lift an edge and crack the glass. The pieces were then carefully removed with little contamination being introduced and no damage to the leads.

The glass passivation on the devices was partially removed to facilitate the voltage contrast examination. The etchant used was 8 parts NH_4F (40%) to 1 part HF (48%) and took approximately 5 minutes. This 5 minute exposure was too long on some devices and resulted in non-functional parts. On some of the devices after stripping they would operate properly but following erasure they could not be reprogrammed.

S/N 2 was stripped and a photograph of the complete die was taken (ref Photo 3-1). The die has two groups of memory elements with the sense transistors at the ends of these; the row decode in the center, and the remaining decode circuitry, inputs, outputs, and chip select around the periphery.

Circuit Characterization

The voltage contrast evaluation was performed on Serial Number 3. This device was placed in a SEM test fixture which provides electrical connection between the device and an external connector on the SEM specimen stage. Complete functional testing could then be performed on the device while viewing its operation using voltage contrast.

The acceleration voltage used for the voltage contrast examination was 1.3 kv. On this device higher acceleration voltages would erase the memory and if increased further would lead to device failure.

The device was operated at low frequencies; 1 to 20 Hz, while observing the different sections and gaining a familiarity with the device layout. The individual sections were then examined and documented. The first sections to be described are the row and column address buffers. These two buffers are identical so will be discussed together.

The input discussed is A1, pin 7. The voltage contrast image is shown in Photo 3-2. The bonding pad as well as portions of the circuitry are seen to be striped with bright and dark areas. The bright areas indicate portions of the circuit which are at the lowest potential while the dark areas are at the higher levels. This is a three power supply device with V_{BB} equal to -5 V, V_{CC} equal to +5 V, and V_{DD} equal to +12 V. Crossing through the center of the voltage contrast image is the V_{BB} metallization stripe with the V_{CC} stripe directly beneath it. The V_{DD} stripe circles around the perimeter of the labeled circuitry; however, it is extremely difficult to see because it is black against a black background. The portion of the circuitry associated with the A1 input can easily be recognized by the similarity of the bright and dark areas to pin 7. The A1 and A1-not addresses are visible at the top of the photograph and are seen to be out-of-phase. The light microscope image is shown in Photo 3-3. A comparison of the voltage contrast image and the light microscope image demonstrates the amount of information available in the former. The V_{DD} metallization is easier to follow in the light microscope image, however. The schematic of this circuit is shown in Figure 3-1 and the logic diagram is shown in Figure 3-2. By utilizing both the voltage contrast and light microscope images, this circuitry is developed. The signals are traced through the circuit and the transistors identified. This integrated circuit uses n-channel, silicon gate MOS technology.

The address inputs have a diffused resistor R1 to provide input protection. The MOS transistor Q1 goes to ground and is biased off unless the address goes negative. This provides reverse bias protection. The incoming signal goes through three invertor stages to produce an address-not signal and through one additional stage to produce the address signal. Examining the schematic, there are three pull-up sections; e.g., transistors, Q11, Q12, Q13, and capacitor C1. These provide 12 volts for various internal circuit operations as well as for the output. V_{BB} is also available to the output section via the transistor pairs, Q30, Q31, or Q26, Q27. The address input functions at TTL logic levels; however, the first inverter shifts the logic

levels to +12 V and -5 V. The output of the first inverter goes to the gate of Q16. The output of the second inverter goes to the gate of Q20. The output of the third inverter provides the address-not output and provides the input to the gates of Q21 and Q27. The output of the final inverter then provides the address signal to the decode section. The two output signals produced by each of these input addresses then goes to a decode section. The gates marked A, B, and C go to fixed voltage levels and will be discussed at a later point. The row decode uses addresses A4 through A10 and the column decode uses A0 through A3. The row decode will be discussed next.

The voltage contrast images of a portion of the row decode are shown in Photos 3-4 and 3-5. and the light microscope image is shown in Photo 3-6. The signal coming into the decoder in Photo 3-4 is the A7 and A7-not addresses. These signals are at approximately +12 V and -5 V as previously discussed. The signals going to the memory are approximately +5 V and -5 V and are shown in Photo 3-5. The two rows being addressed are visible in this photograph. Only 1 out of the 128 rows will go high at a given time. The light microscope image identifies the A4 through A10 input lines as well as one section of the decode transistors. The schematic for this section is shown in Figure 3-3, and the logic diagram is shown in Figure 3-4. The schematic is for one of 16 similar sections in the decode circuitry. There are eight rows decoded in the schematic while the logic diagram indicates one specific row. The +5 V pull-up is provided by transistors Q1 - Q6 for the section labeled; and then depending on which incoming lines are high and low a specific row will be decoded. As an example to address memory location 1001110 the following conditions must be met: A6, A8-not, A9-not, A10, A7, A5, and A4-not, must all be high, also the opposite phase signals from these addresses must be low. They are A5-not, A6-not, A7-not, A8, A9, A10-not, and A4. This is evident from the schematic.

To select a particular word in the memory, a column must also be addressed. The column decode will be discussed next. This area is shown in the voltage contrast image in Photo 3-7. Address inputs A1 and A1-not are coming in on the left side of the photograph at alternating +12 V and -5 V, and are proceeding through the decode circuitry to two output lines going to the memory. The light microscope image of this area is shown in Photo 3-8. The A0 through A3 address lines are labeled as well as a portion of the decode circuitry. The schematic for the entire column decode circuitry is shown in Figure 3-5, and the logic diagram for addressing one column is shown in Figure 3-6. As seen in the schematic, A2 and A3 are used to select one of 4 sections, followed by A1 selecting one of 8 sections and A0 selecting a given column. The output of this section goes between approximately +12 V and -5 V. To address column 0001, the following conditions must be met: A3-not, A2-not, A1-not, and A0 must be high and A3, A2, A1 and A0-not must be low.

To enable all of the operations on this chip, the chip select-not input must be low. The voltage contrast image of this section is shown in Photo 3-8. The input is the alternating high-low line coming into transistor Q1. The

different DC voltage levels of A, B, C, V_{SS}, V_{BB}, V_{CC}, and V_{DD} are evident on this photograph.

The light microscope image of this area is shown in Photo 3-10. Chip select-not comes into this section as well as going to the output transistor. The schematic is shown in Figure 3-7 and the logic diagram is shown in Figure 3-8. The circuitry shifts the input from its 0 to 5 V level up to a 0 to 12 V level. The input comes through transistor Q1 which is biased on by V_{DD} through a protect resistor, R1, to the drain of the reverse bias protection transistor Q2 and the gate of Q4. The output of the first inverter goes to Q12 while the output of the second inverter is CS-not cut.

In a program mode, the chip select line receives a program pulse of approximately 26 volts for a high which goes directly to the output section. The V_{CC} at this time is at 12 volts.

The memory cell is shown in the voltage contrast image in Photo 3-11 and in the light microscope image in Photo 3-12. The metallization which has the dark and bright stripes is a column which has been addressed and two separate memory locations are being read out. The light microscope photograph shows the column metallization, the polysilicon gate for the rows, and the small dark rectangle at the intersection of the metallization and the polysilicon is the floating gate. The charge on this floating gate determines whether a high or low is at that location. A charge on the gate biases the transistor off and produces a high condition. The schematic of the memory cell (Figure 3-9) is a single transistor with the source tied to -5 V the gate going to the row decode and the drain going to the sense transistor. The sense transistor is also very simple as is discussed next.

The sense transistors are shown in the voltage contrast image in Photo 3-13, and the light microscope image in Photo 3-14. The voltage contrast photograph shows two adjacent columns which are being read. The light microscope photograph labels two of the sense transistors. One sense transistor gate out of 16 is high for each of the 8 outputs. The sense transistor is only a switch as shown in the schematic (Figure 3-10). The logic diagram for this is shown in Figure 3-11.

The sense transistor then goes to one of eight outputs. The voltage contrast image of the output section is shown in Photo 3-15, and the light microscope image is shown in Photo 3-16. For this photograph, A0, A1, A2, A3, A4, and A9 are cycling while A5, A6, A7, A10, and CE-not are low and A8 is high. The output is going from approximately 0 V to 5 V at a 1 second rate. The light microscope image includes more area than the voltage contrast image. This extra circuitry is primarily involved with the programming as will be seen in the schematic. The schematic is shown in Figure 3-12 and the logic diagram is shown in Figure 3-13. CS-not * comes directly from pin 18.

During a read operation, the sense transistor source voltage is inverted twice in reaching the output. In a program operation, the output pin is used as a data input. During the read operation, the first inverter output

goes to transistors Q13 and Q15 gates. The voltage at the drain of transistor Q13 is then inverted by the transistor pair Q25 and Q26 to produce a 0 V or 5 V output. During the programming mode, Q25 and Q26 are biased off by CS-not and the signal at the output goes through three inverters and an AND gate to reach the sense transistor. The input structure is similar to that seen on the other inputs, an input resistor, a reverse bias protect transistor and an inverter gate. The three transistors Q28, Q30, and Q34 are biased on by the signal marked C. Transistor Q36 is biased off by the signal marked B. B is low and C is high during programming as discussed in the next section. The programming is accomplished by addressing a given word and putting a high or low on the output pin. A low is inverted three times and is applied to the gate of Q38 as a high. This high transfers the 26 volt programming pulse to the memory location. The programming consists of depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. The low on the output pin then allows the programming pulse to reach the memory cell and produce a low.

The three points labeled A, B, and C on the various circuits are voltages established by resistor and FET networks. These schematics are shown in Figure 3-14. During normal operation the points were measured and found to be, A = 1.43 V, B = 11.94 V, and C = -4.95 V. During programming V_{CC} is raised from the +5 V to +12 V. In reference generator B this 12 volts will turn on the transistor connected between B and -5 V thus pulling B low. With B low, C will go high since the transistor between -5 V and C will be off. The values measured with V_{CC} = 12 V were A = 3.45 V, B = -4.80 V, and C = 11.92 V.

The chip organization is shown in Photo 3-17. A block diagram is shown in Figure 3-15. The die dimensions are 190 mils by 220 mils; the die has aluminum metallization and aluminum ultrasonic bonds. A bit map was generated and is shown in Figure 3-16. The row and column address lines are identified according to the device layout and not by address bit significance. The address sequence for row addresses A4, A5 and A7 are shown in the first block (top). This sequence is repeated in each of the following blocks. The address sequence for row addresses A6, A8, A9 and A10 is shown in each block and these address states remain constant through each block as shown. The address sequence for column addresses are repeated as shown in Q1 for outputs Q2 through Q8.

Failure Analysis

A failure was produced on S/N 10 by irradiating transistor Q3 of the input buffer A3 on the SEM. An accelerating voltage of approximately 5 kv caused this transistor to fail. As shown in the input buffer schematic, Figure 3-1, transistor Q3 is the first gate to which the incoming signal connects.

The failure analysis was performed by a different person than produced the failure. Electrical measurements found that the same word was addressed when A3 input was high or low. Examination on the SEM using voltage contrast found that transistor Q3 was not following the input signal (Photos

3-18, and 3-19). A properly functioning input was photographed for comparison (Photo 3-20). In Photo 3-19 the bright and dark striped area is the metallization which connects to the polysilicon gate of Q3.

As can be seen in the properly functioning device the diffusion to the right side of the gate should be following the voltage on the gate. This is the common diffusion between transistors Q3 and Q4. This type of analysis is easily performed since a properly functioning address buffer and a failed address buffer on the same device can be examined and compared.

TABLE 3-I DC PARAMETERS

S/N	1	2	3	5	6	7	8	10	V_{IN}=5.5V Pin	Para
	0.0μA	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1	Iin
	↑	↑	↑	↑	↑	↑	↑	↑	2	Iin
									3	Iin
									4	Iin
									5	Iin
									6	Iin
									7	Iin
									8	Iin
	0.0								18	Iin
	0.1								20	Iin
	0.0	↓	↓	↓	↓	↓	↓	↓	22	Iin
	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	23	Iin
									Iin Max=10μA	

TABLE 3-I (cont)

S/N 1	2	3	5	6	7	8	10	V_{out}=5.5V $\bar{S}$= 5V Pin	Para
0.0μA	0.0	0.0	0.0	0.0	0.0	0.0	0.0	9	Ilo
↑	↑	↑	↑	↑	↑	↑	↑	10	Ilo
								11	Ilo
								13	Ilo
								14	Ilo
								15	Ilo
↓	↓	↓	↓	↓	↓	↓	↓	16	Ilo
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	17	Ilo
								Ilo Max =10μA	

TABLE 3-I (concl)

S/N 1	2	3	5	6	7	8	10	Pin Para
23.8 mA	24.7	29.7	29.2	28.2	27.2	29.1	25.9	19 IDD
								IDD Max=65mA
5.7mA	5.8	6.5	6.8	6.3	6.4	6.4	6.0	24 ICC
								ICC Max=12 mA
20.9mA	21.2	24.2	23.8	22.6	24.1	25.2	22.9	21 IBB
								IBB Max=45mA

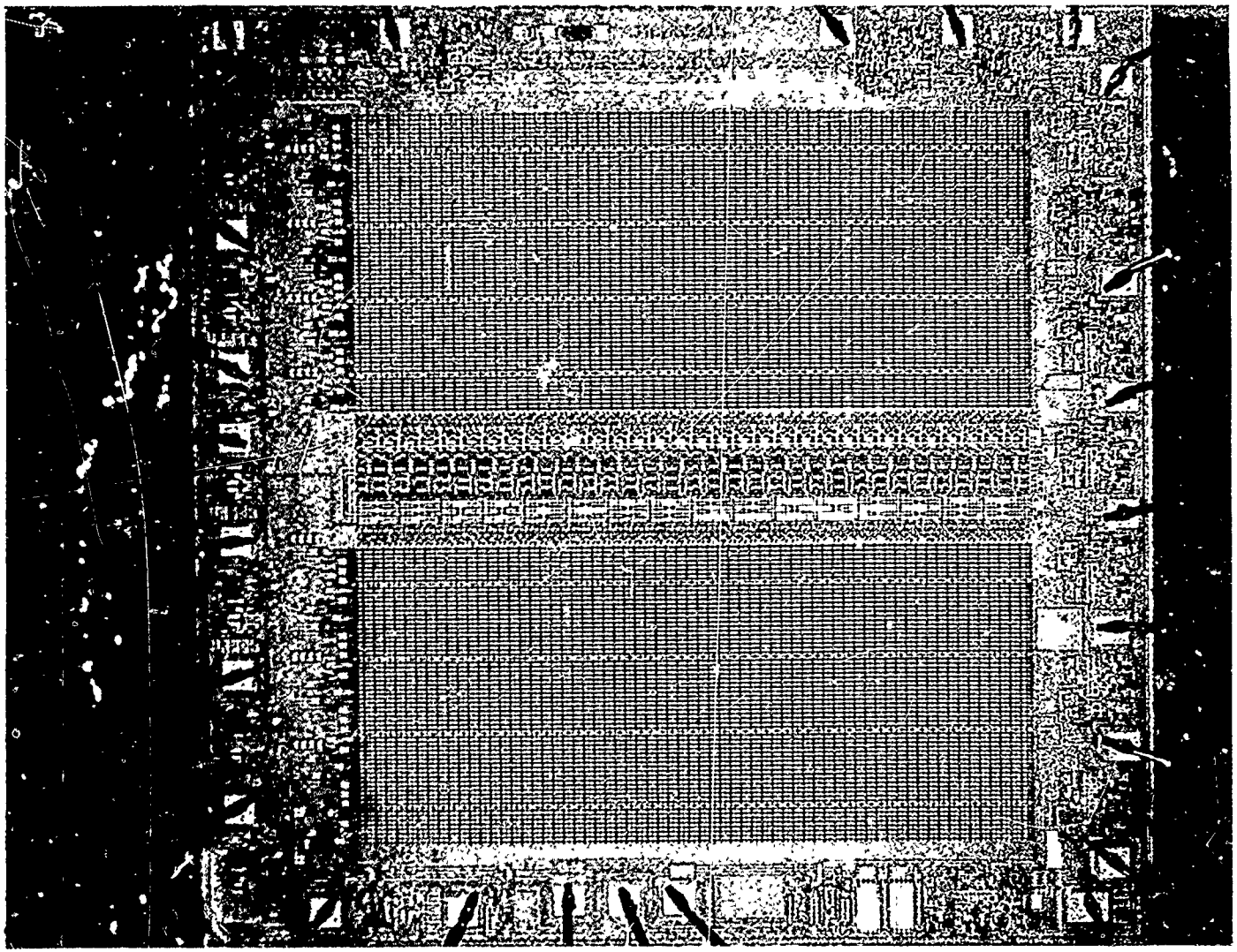


Photo 3-1 Light Photograph of Entire Die, Mag. -

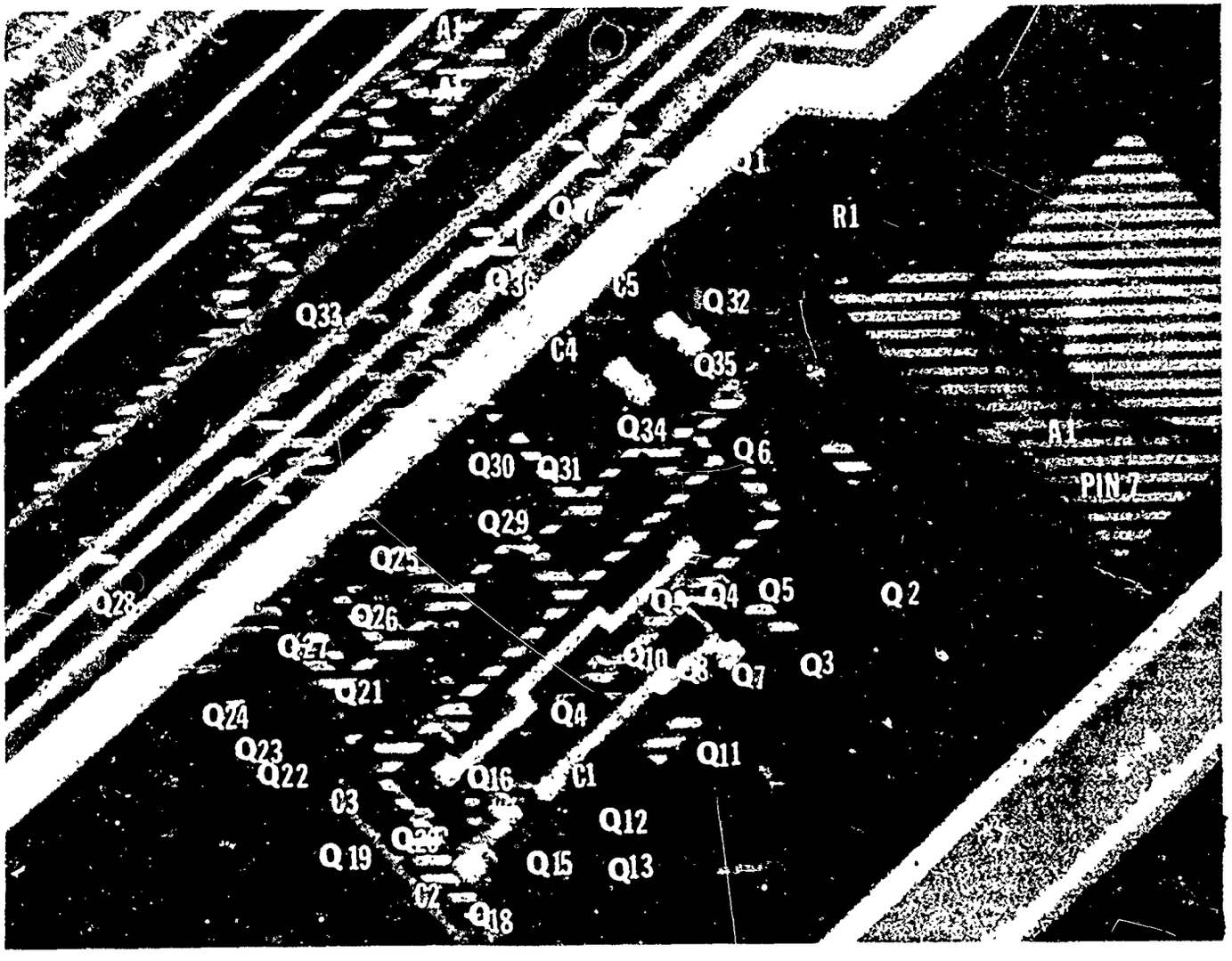


Photo 3-2 Voltage Contrast Micrograph of A1 Input Buffer. Input Pin is Switching from 0 to 5 V. 1.3 KV, Mag. - 400X

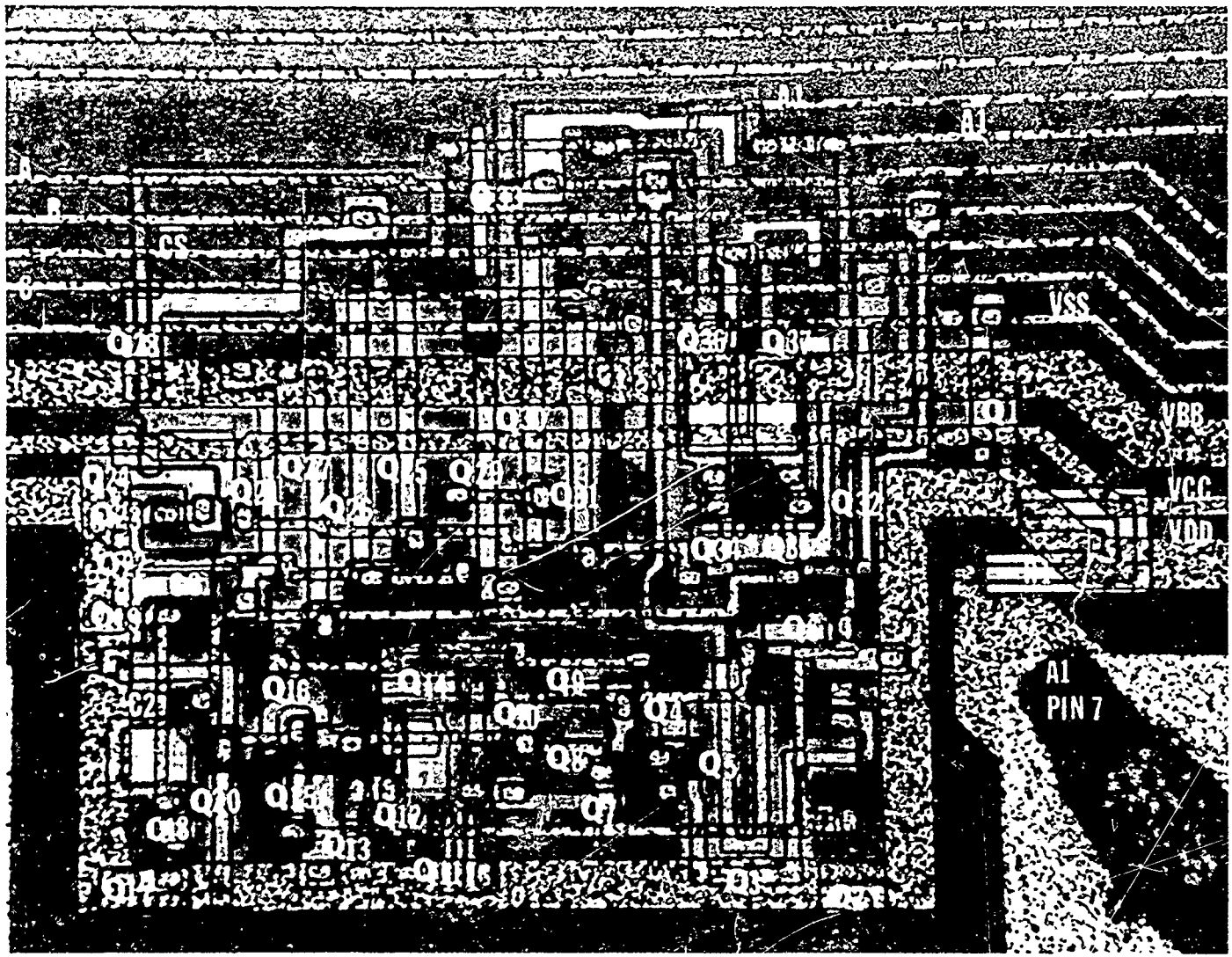


Photo 3-3 Light Photograph of Input Buffer. A Signal on A1 Produces A1 and $\overline{A1}$ as Shown in the Upper Right Corner of the Photograph. Mag. - 350X

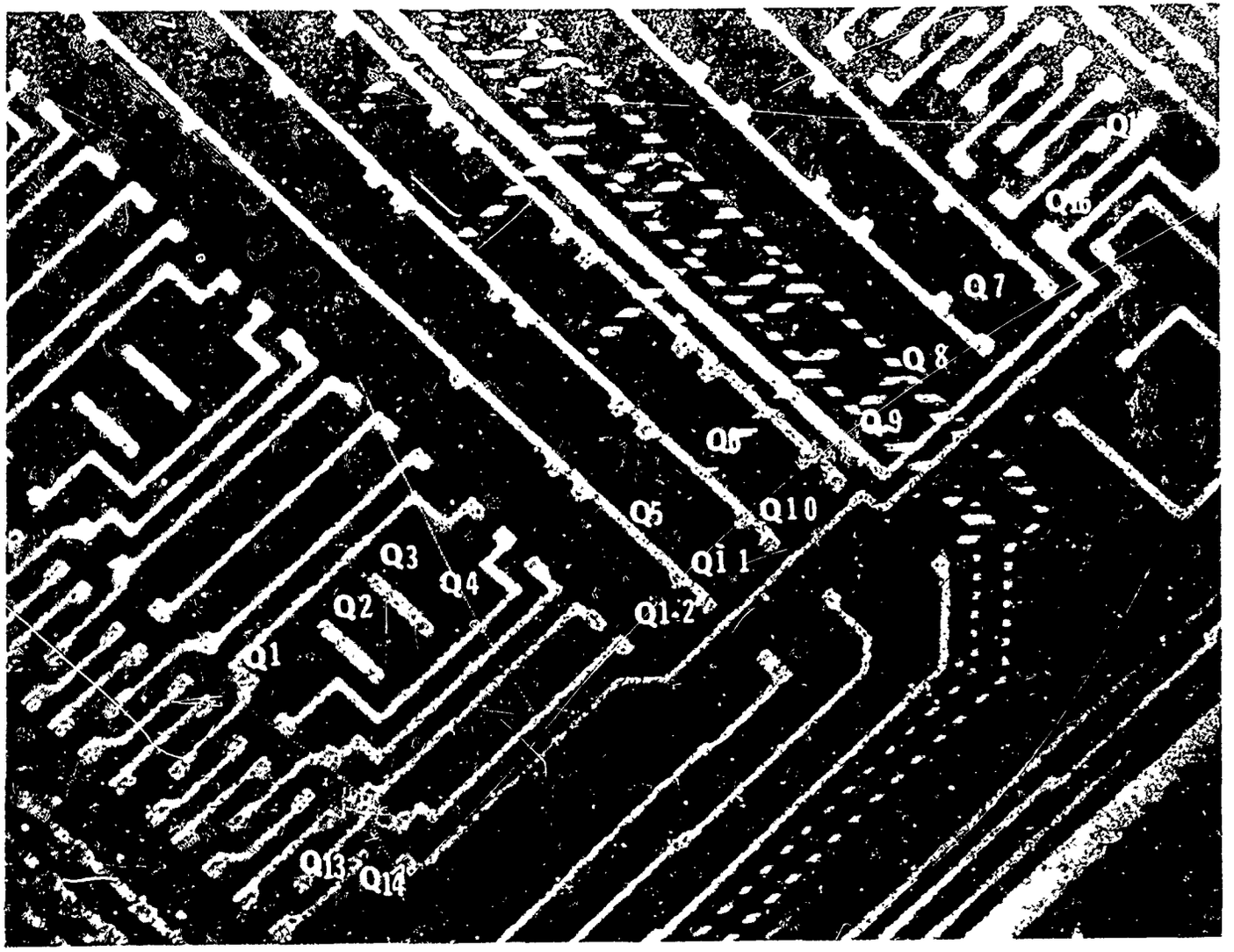


Photo 3-4 Voltage Contrast Micrograph of Row Decode Circuit. A7 and $\overline{A7}$ Inputs are Switching States. 1.3 KV, Mag. - 350X

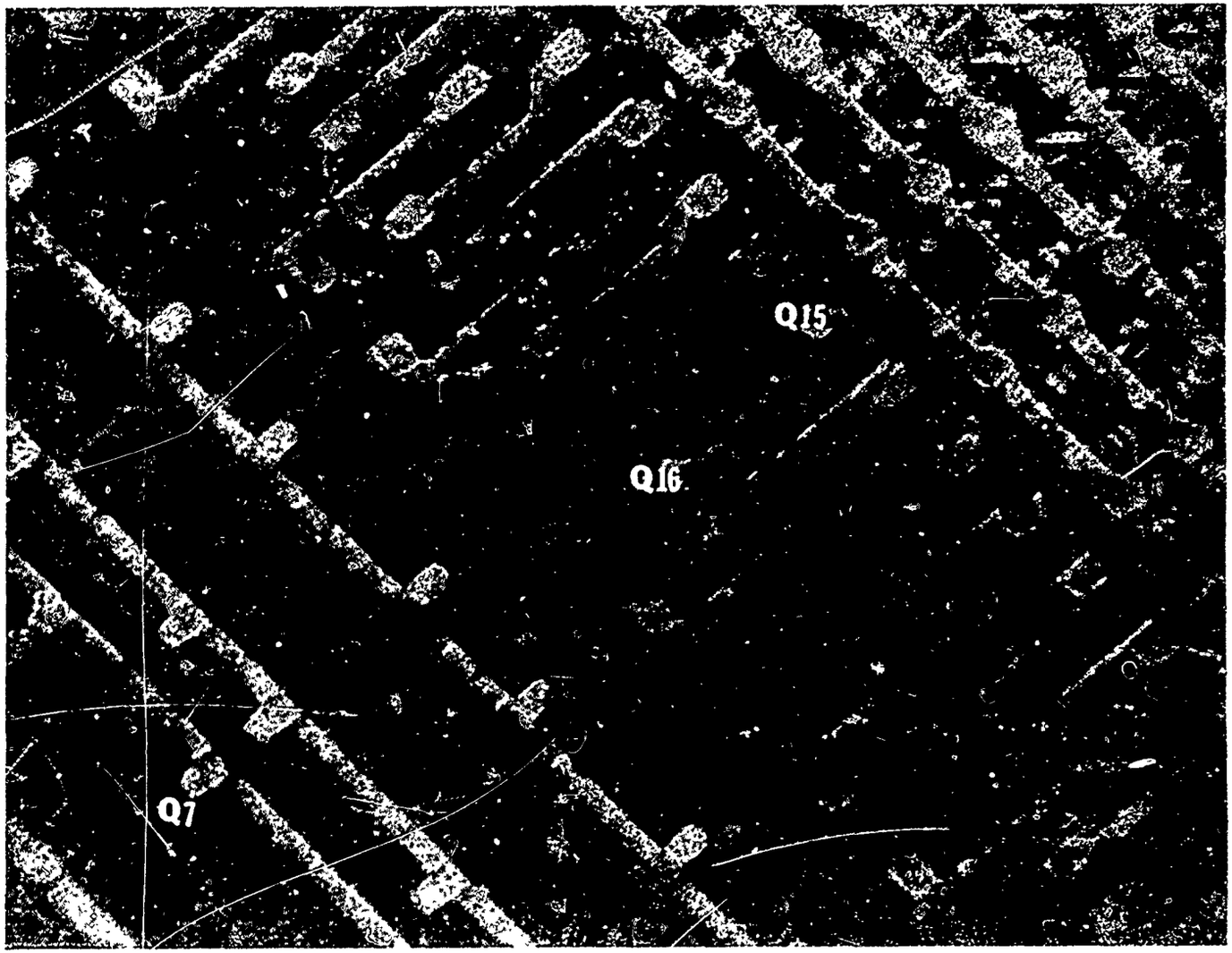


Photo 4-5 Voltage Contrast Micrograph Showing Two Selected Rows. 1.0 KV, Mag. - 700X

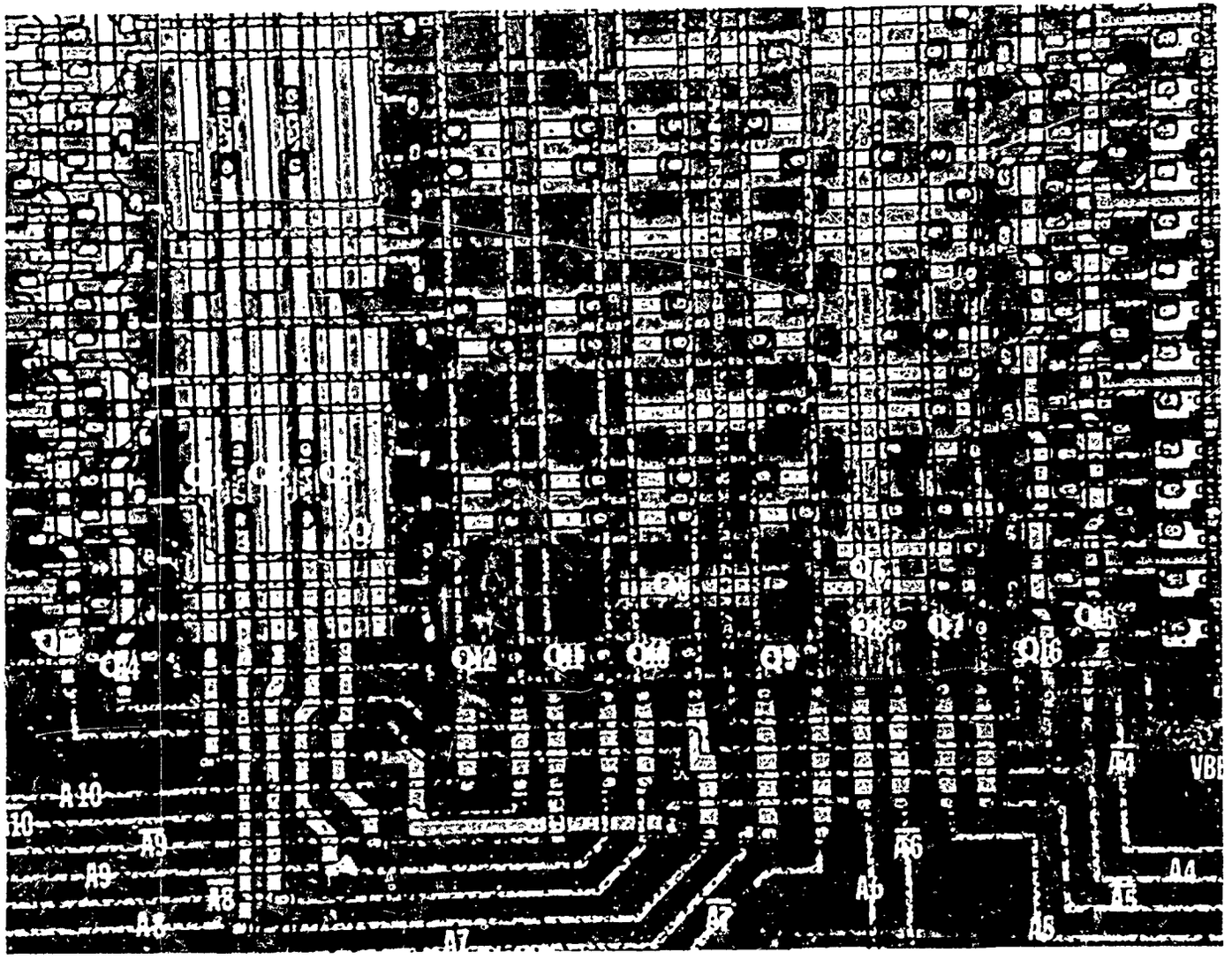


Photo 3-6 Light Photograph of Row Decode Circuit. Input Lines A4 thru A10 are Labeled. Mag. - 300X

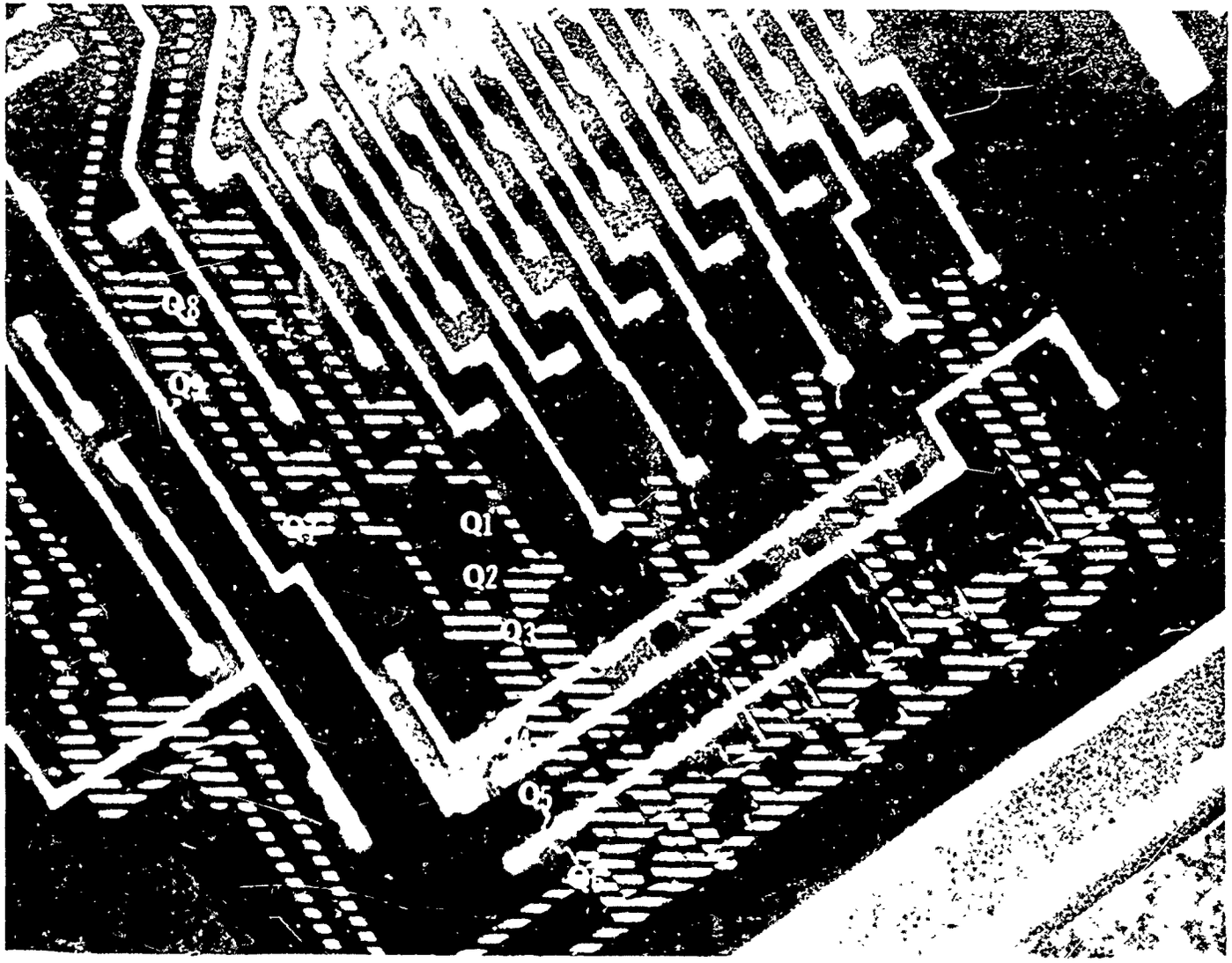


Photo 3-7 Voltage Contrast Micrograph of Column Decode Circuit. Two Columns are Alternately Being Addressed. 1.3 KV, Mag. - 300X

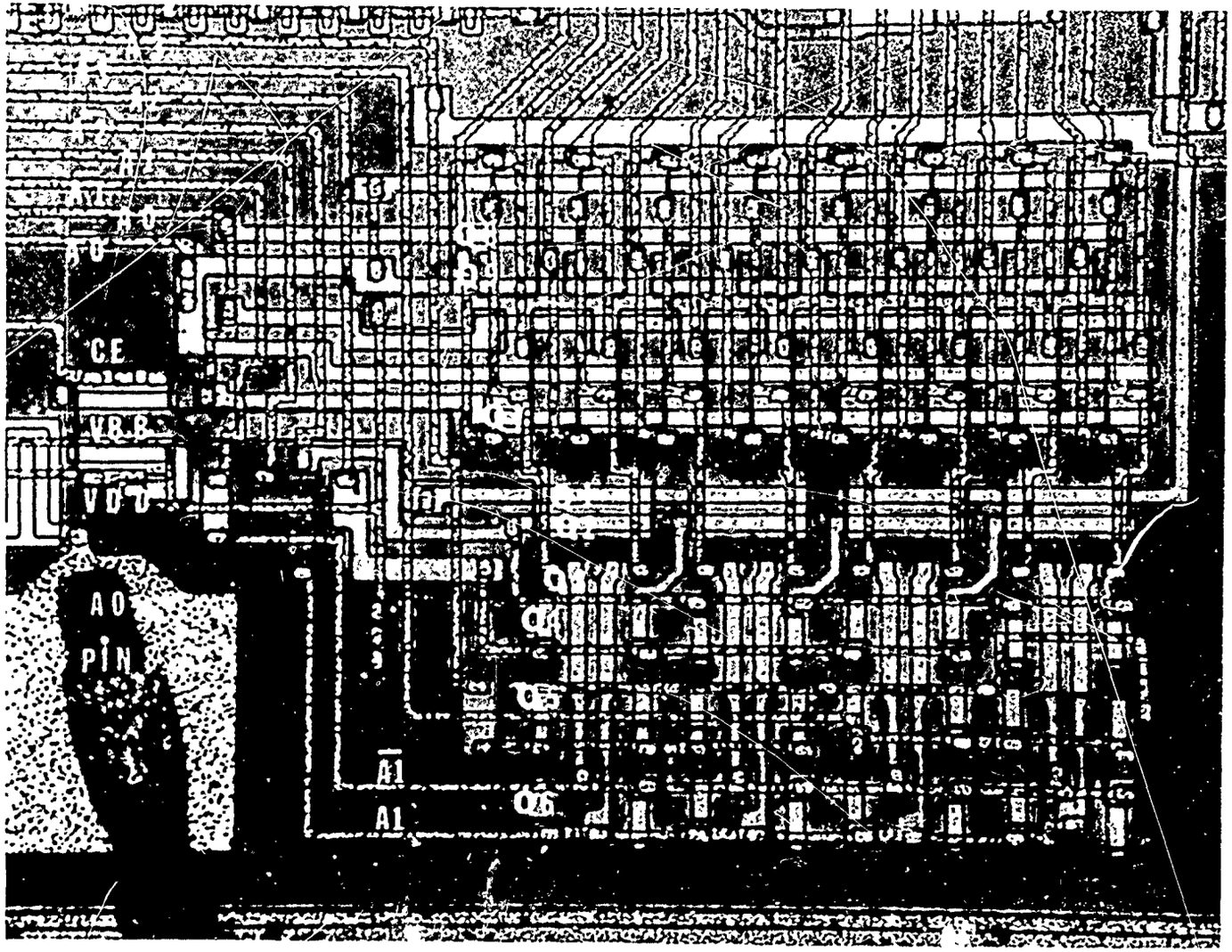


Photo 3-8 Light Photograph of Column Decoder Circuit. Input Lines A0 thru A3 are Labeled. Mag. - 300X

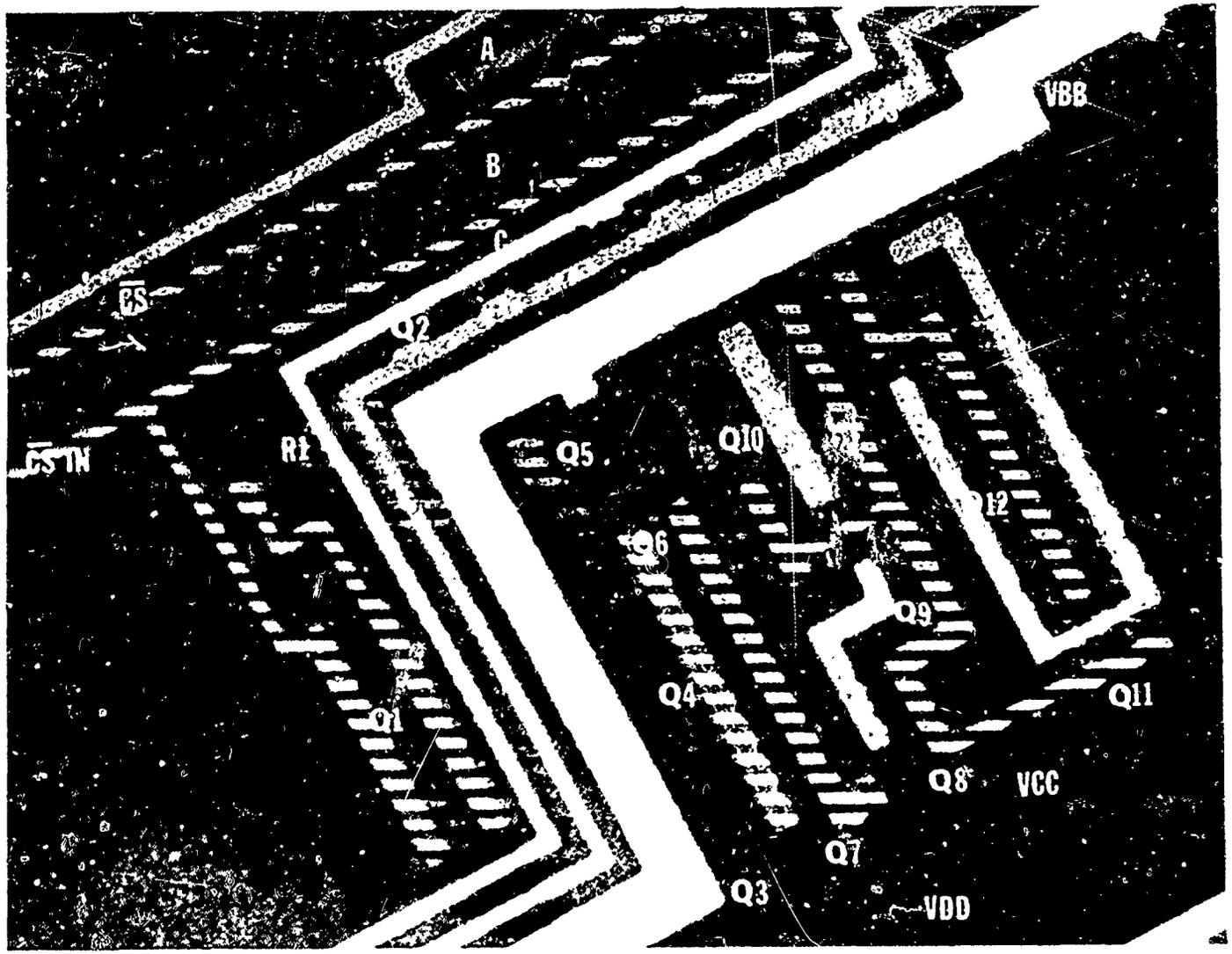


Photo 3-9 Voltage Contrast Micrograph of Chip Select Circuit. Chip Select "Not" IN is a 0 to 5 V Signal and Chip Select "Not" OUT is 0 to 12 V. 1.3 KV, Mag. - 500X

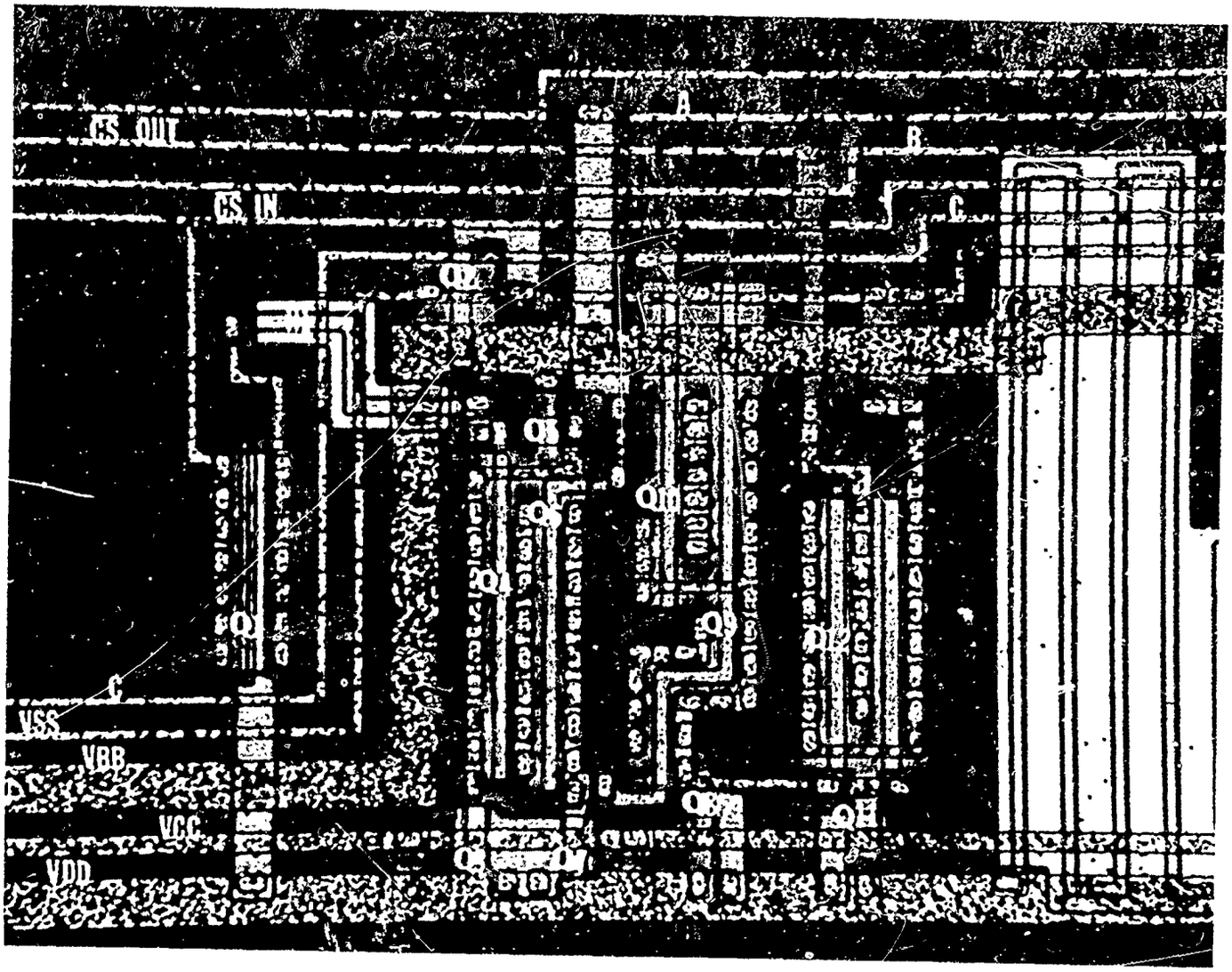


Photo 3-10 Light Photograph of Chip Select Circuit. Mag. - 350X

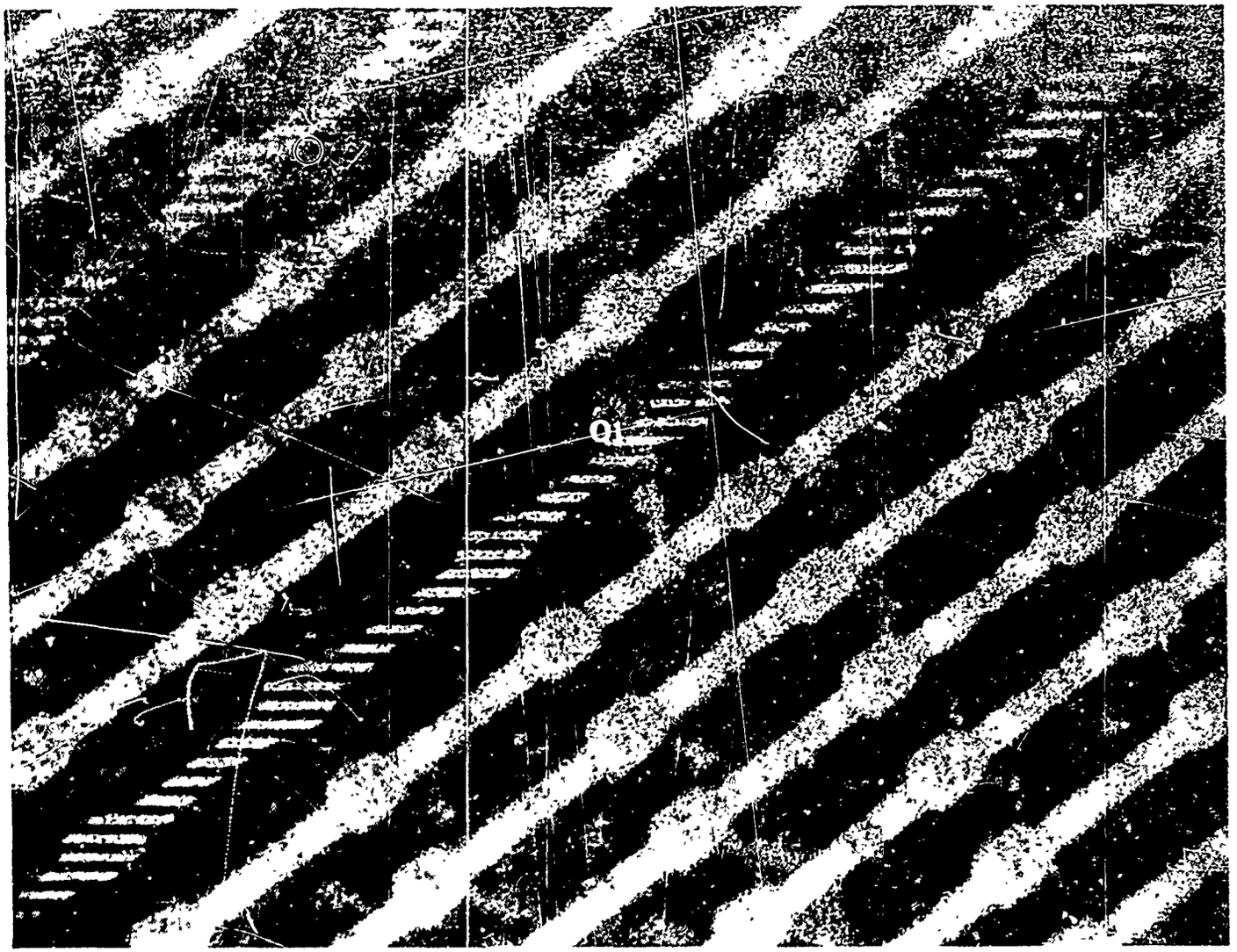


Photo 3-11 Voltage Contrast Micrograph of Memory Area. Striped Line is Column Metallization. 1.3 KV, Mag. - 900X

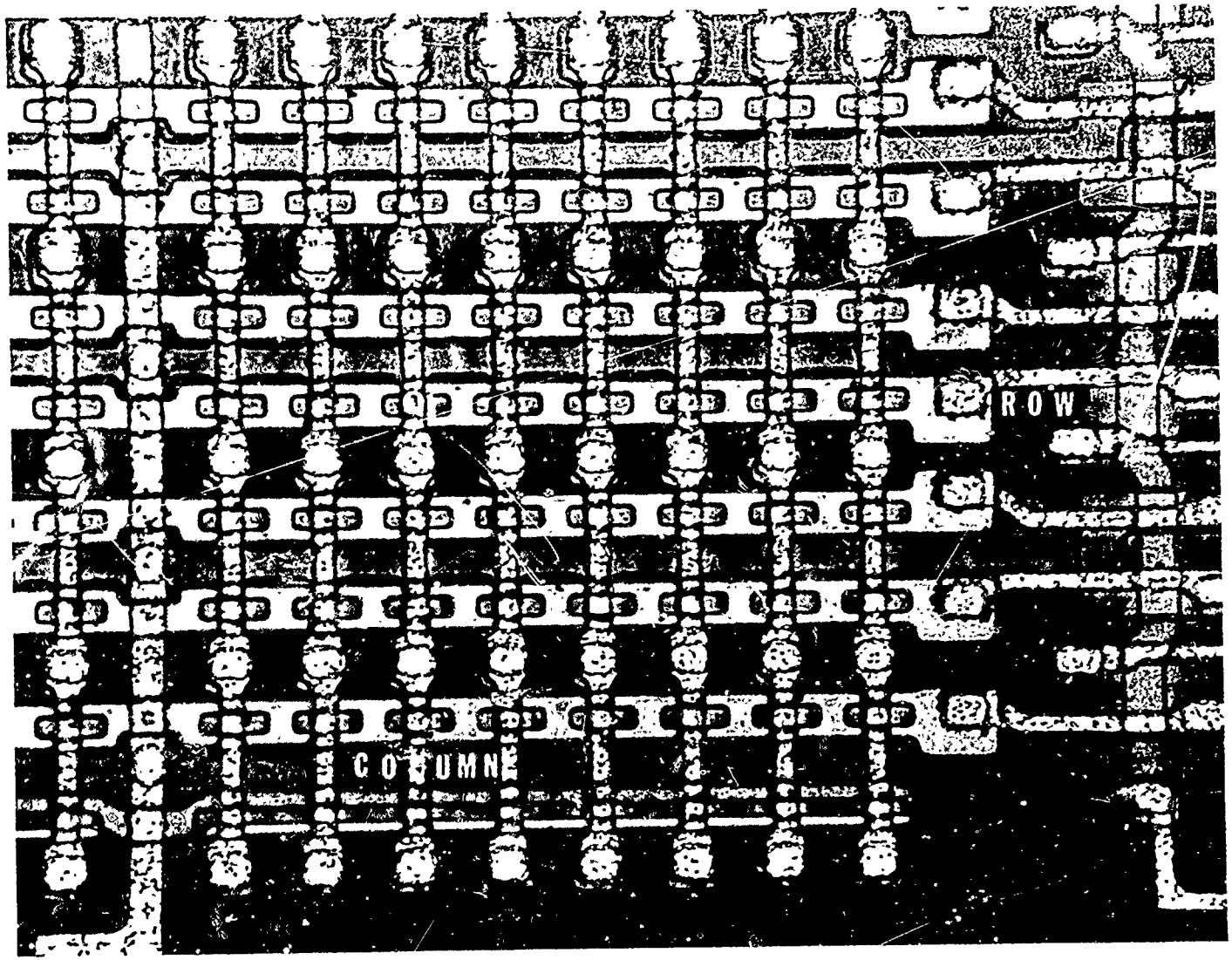


Photo 3-12 Light Photograph of Memory Area. Row Decode Polysilicon is Horizontal and the Column Decode Metallization is Vertical. Mag. - 750X

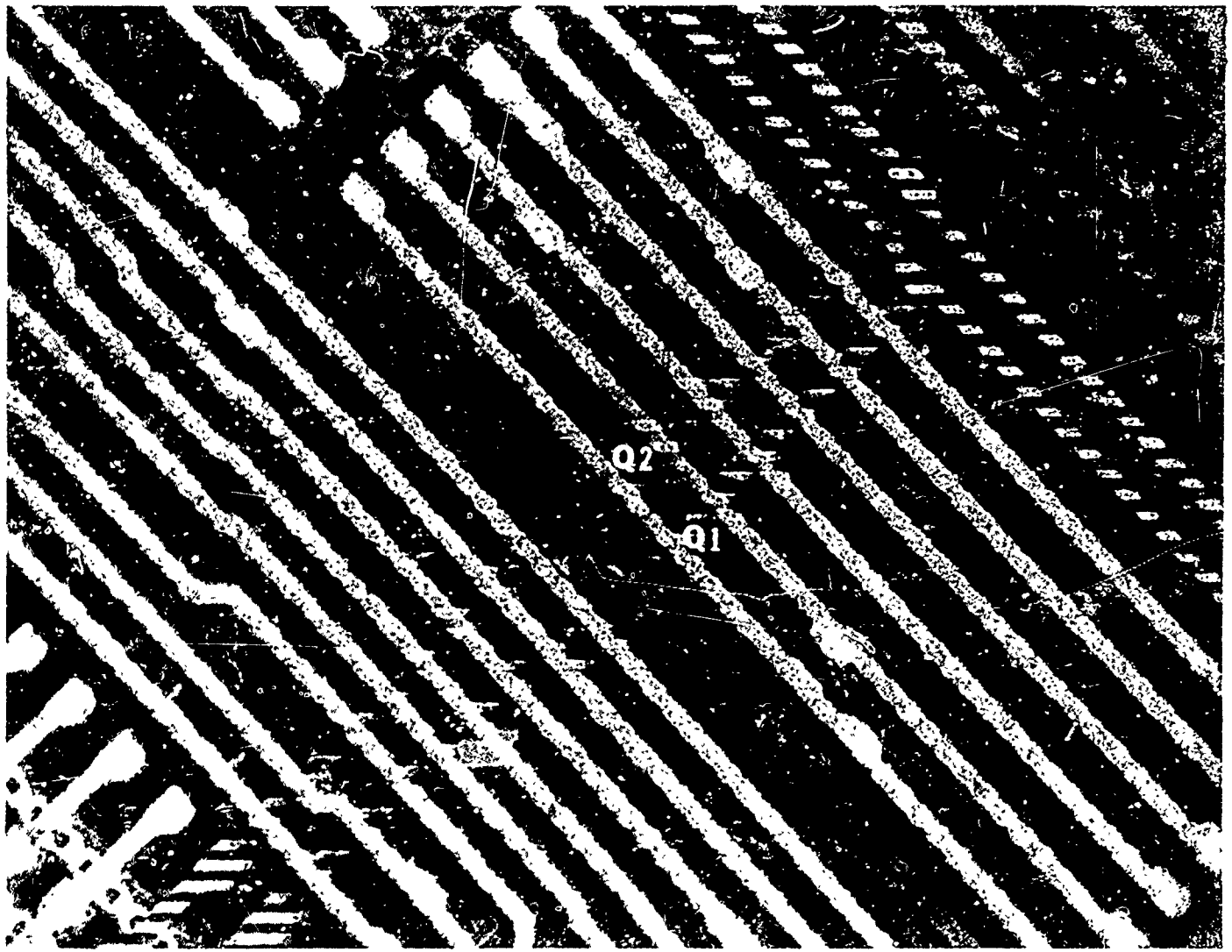


Photo 3-13 Voltage Contrast Micrograph of Sense Transistors. Two Adjacent Columns are Being Read. 1.3 KV, Mag. - 425X

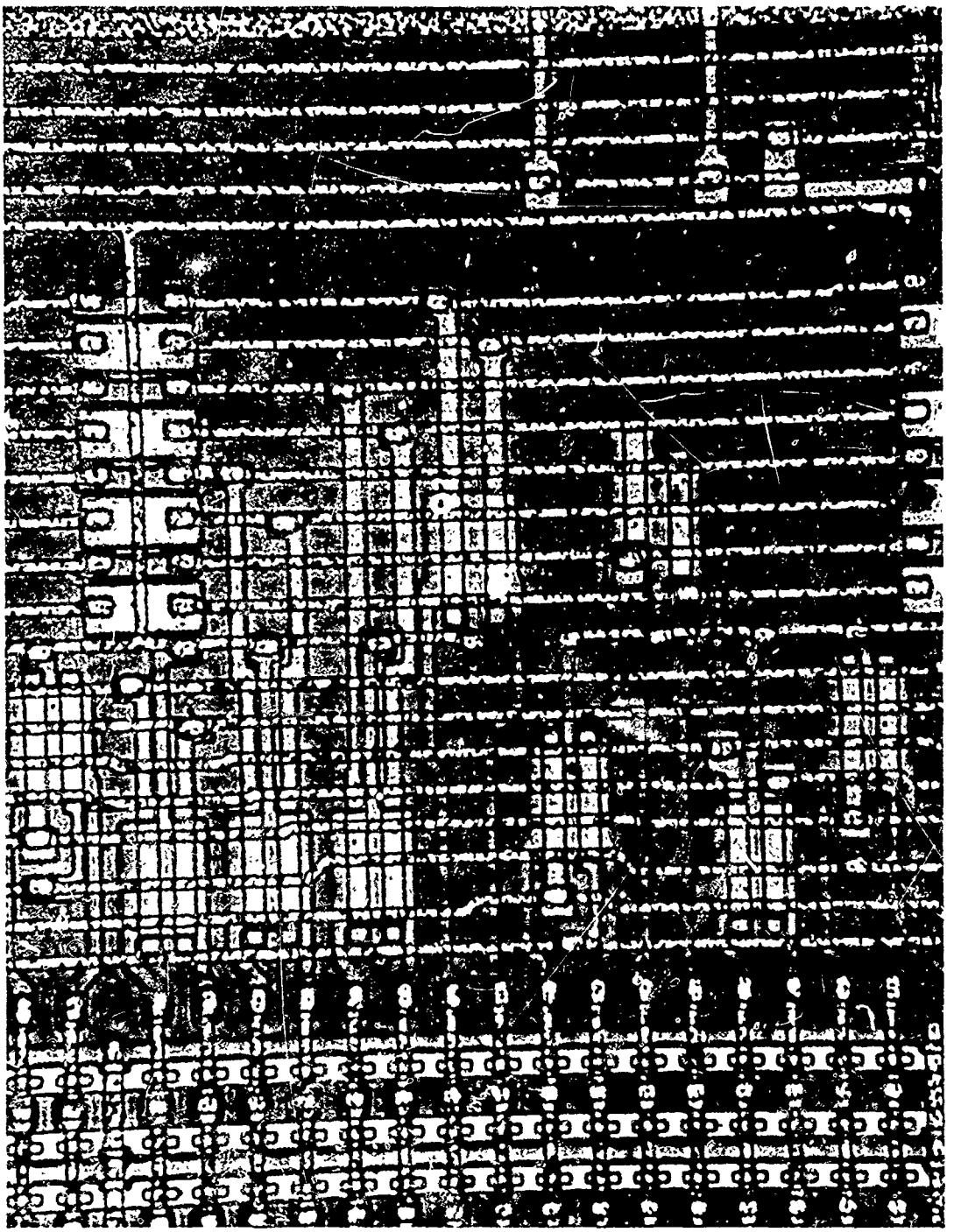


Photo 3-14 Light Photograph of Sense Transistors. Mag. - 350X

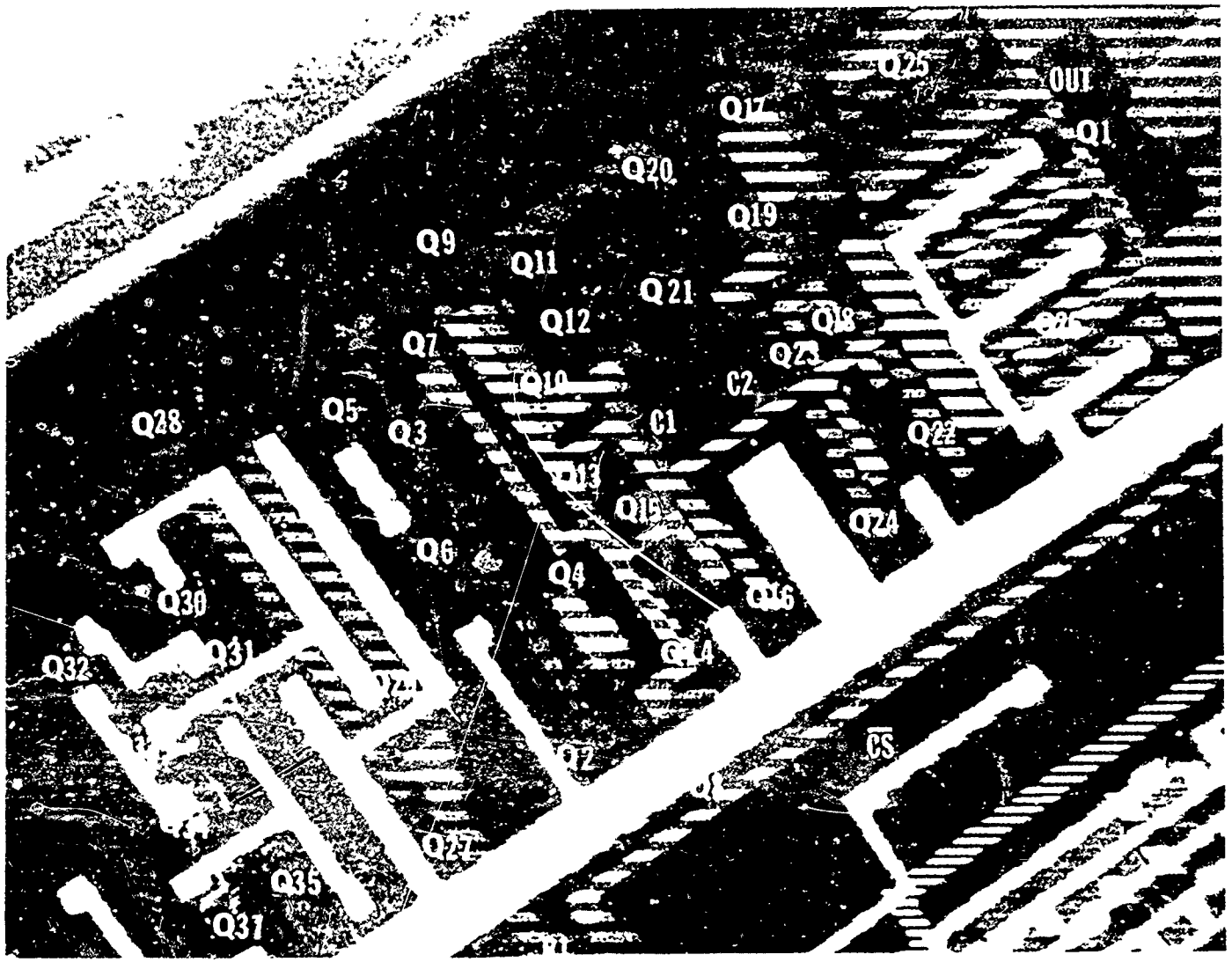


Photo 3-15 Voltage Contrast Micrograph of Output Section. Output in Upper Right Corner can be Seen Going from 0 to 5 V. 1.3 KV, Mag. - 500X

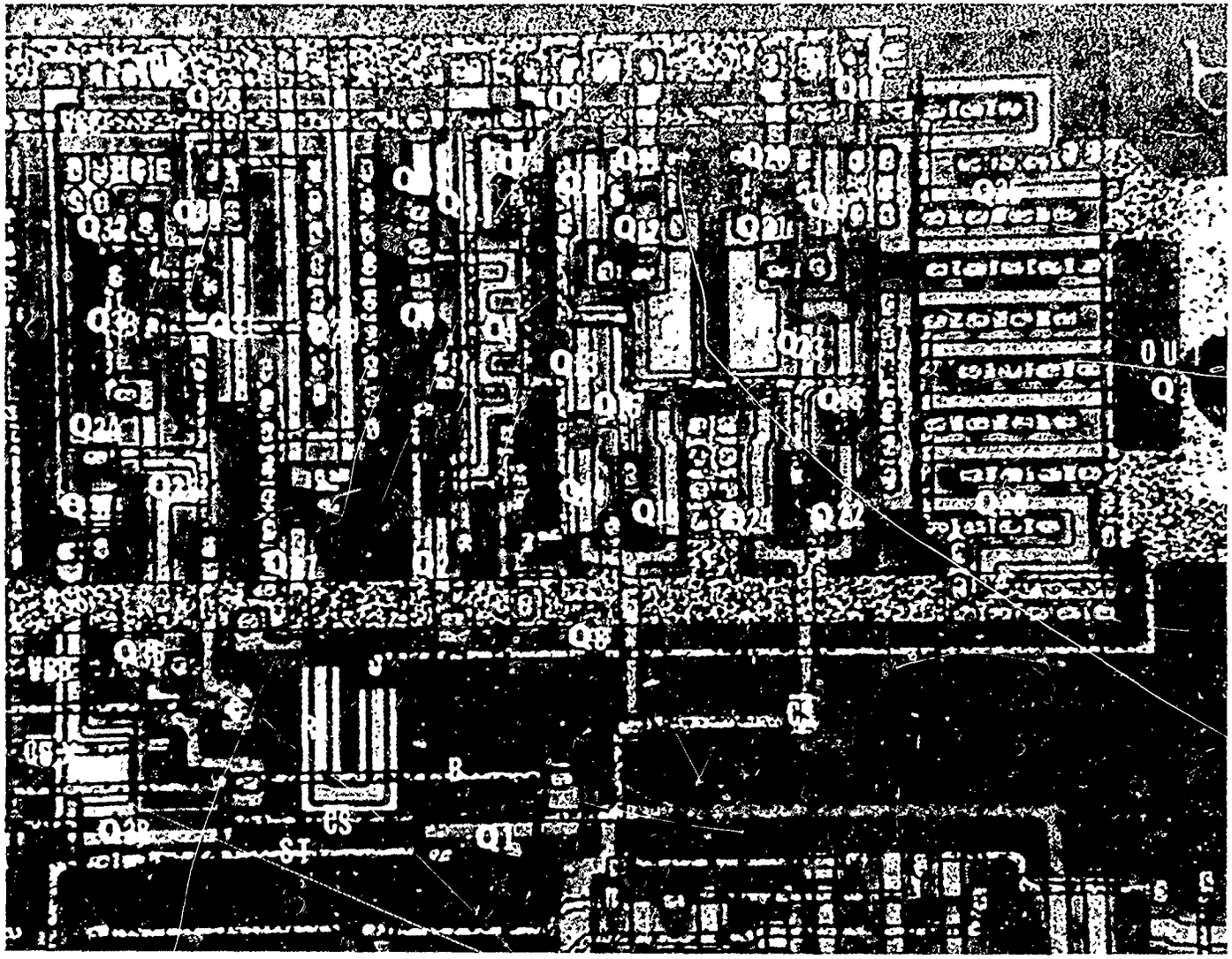


Photo 3-16 Light Photograph of Output Section. Mag. - 350X

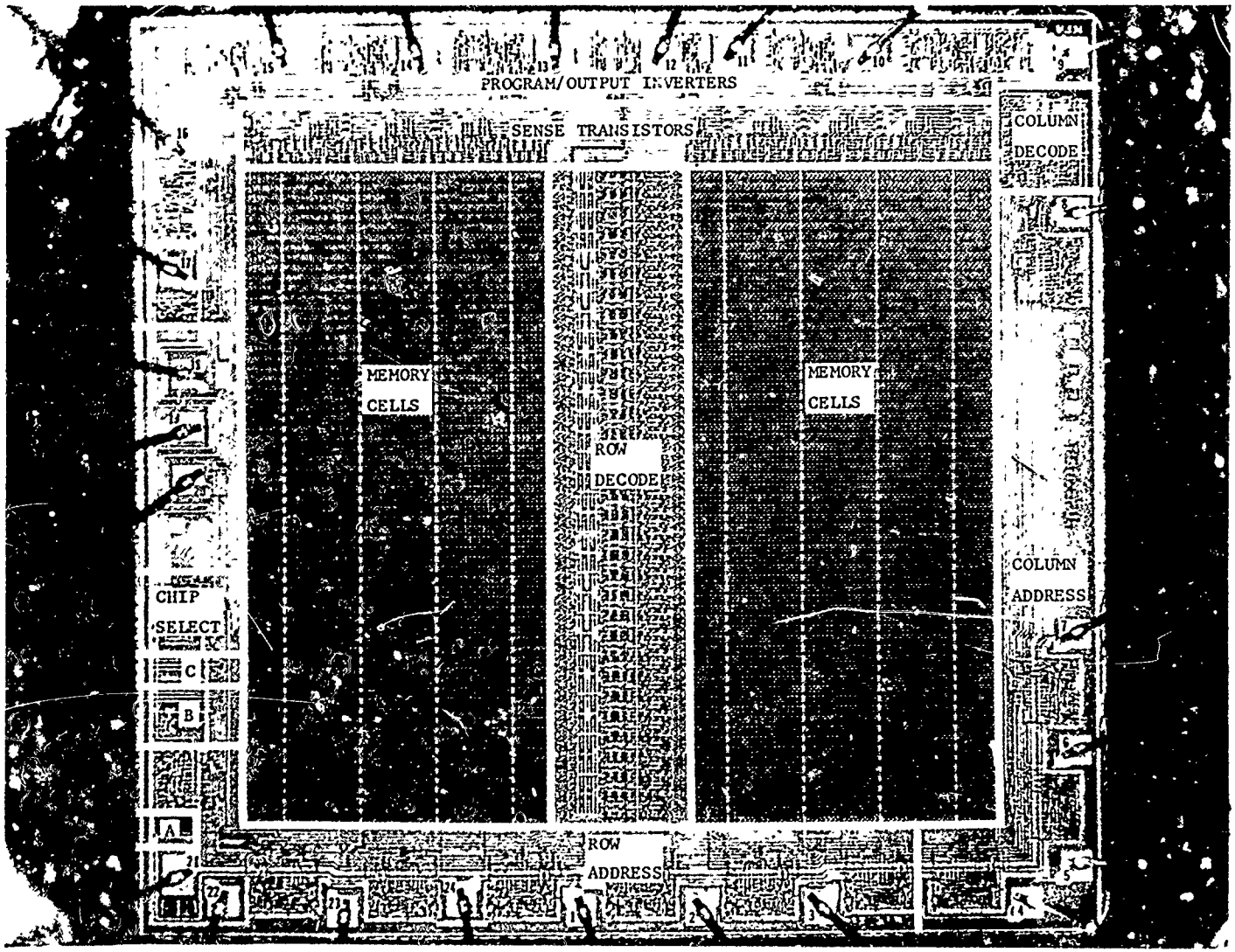


Photo 3-17 Light Photograph of Entire Die. Pins and Functional Areas are Labeled. Mag. -25X

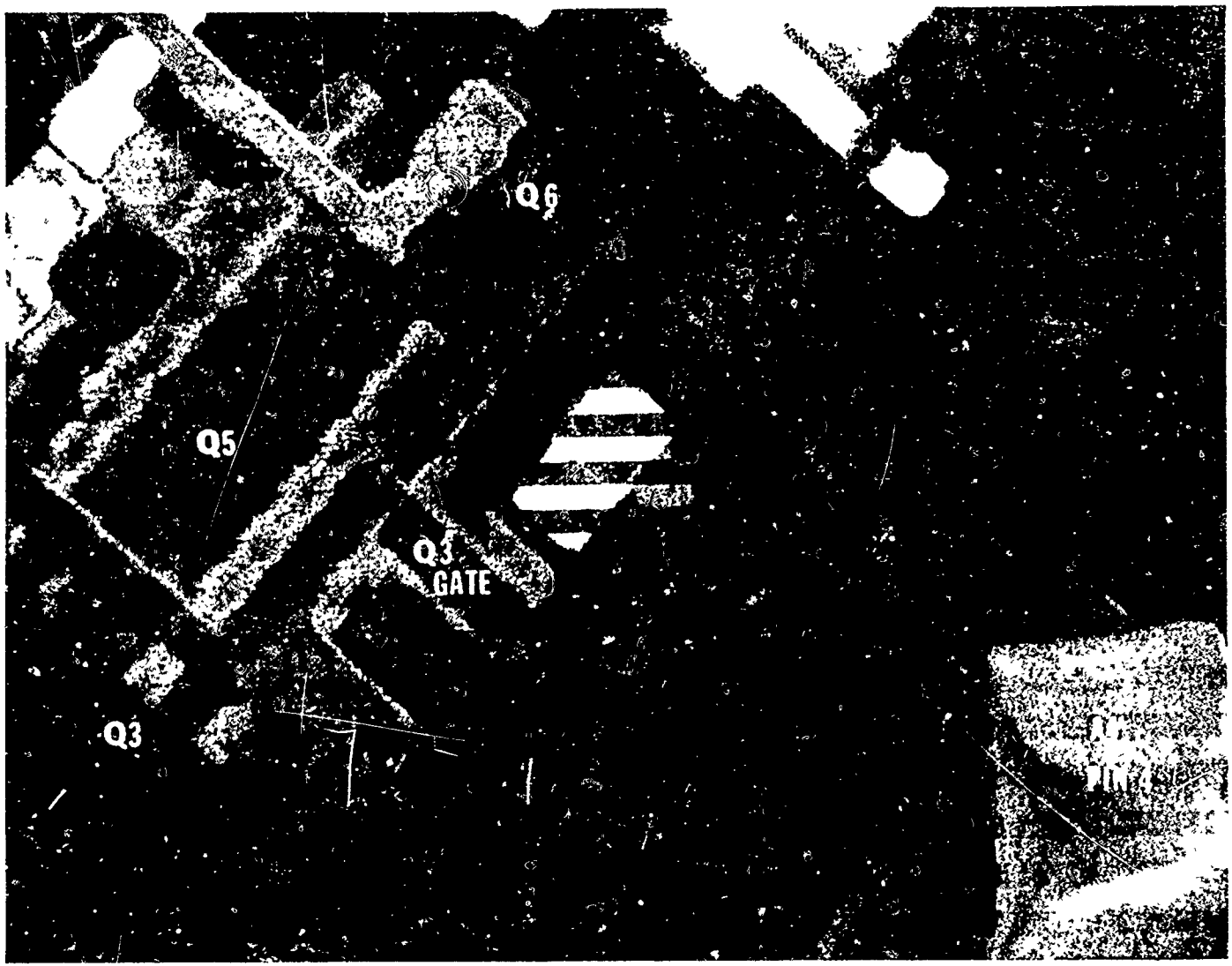


Photo 3-18 Voltage Contrast Micrograph of Failed Input Buffer. Note Appearance of Q_3 Gate. 1.3 KV, Mag. - 1300X

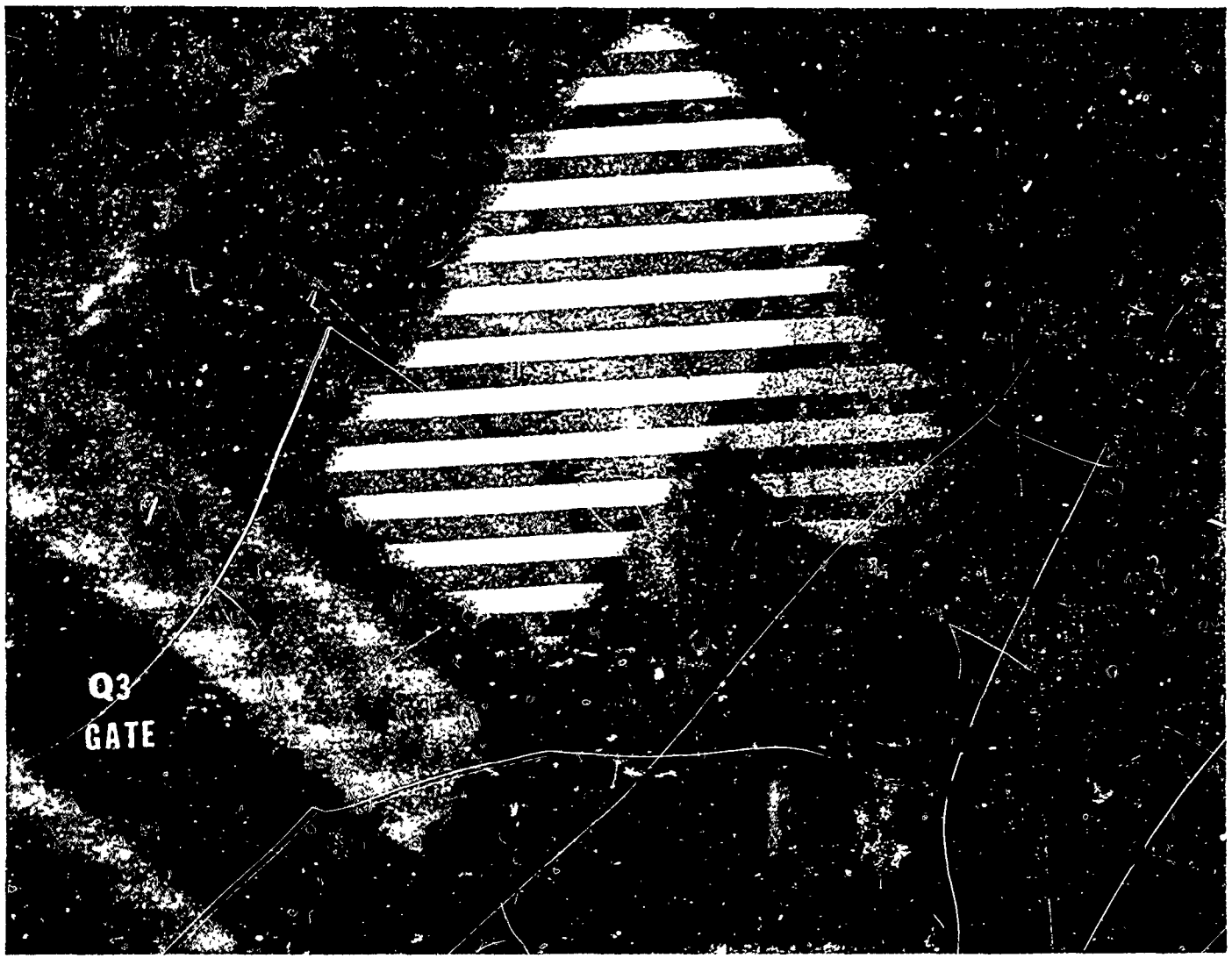


Photo 3-19 Voltage Contrast Micrograph of Failed Transistor. 1.3 KV, Mag. - 4000X

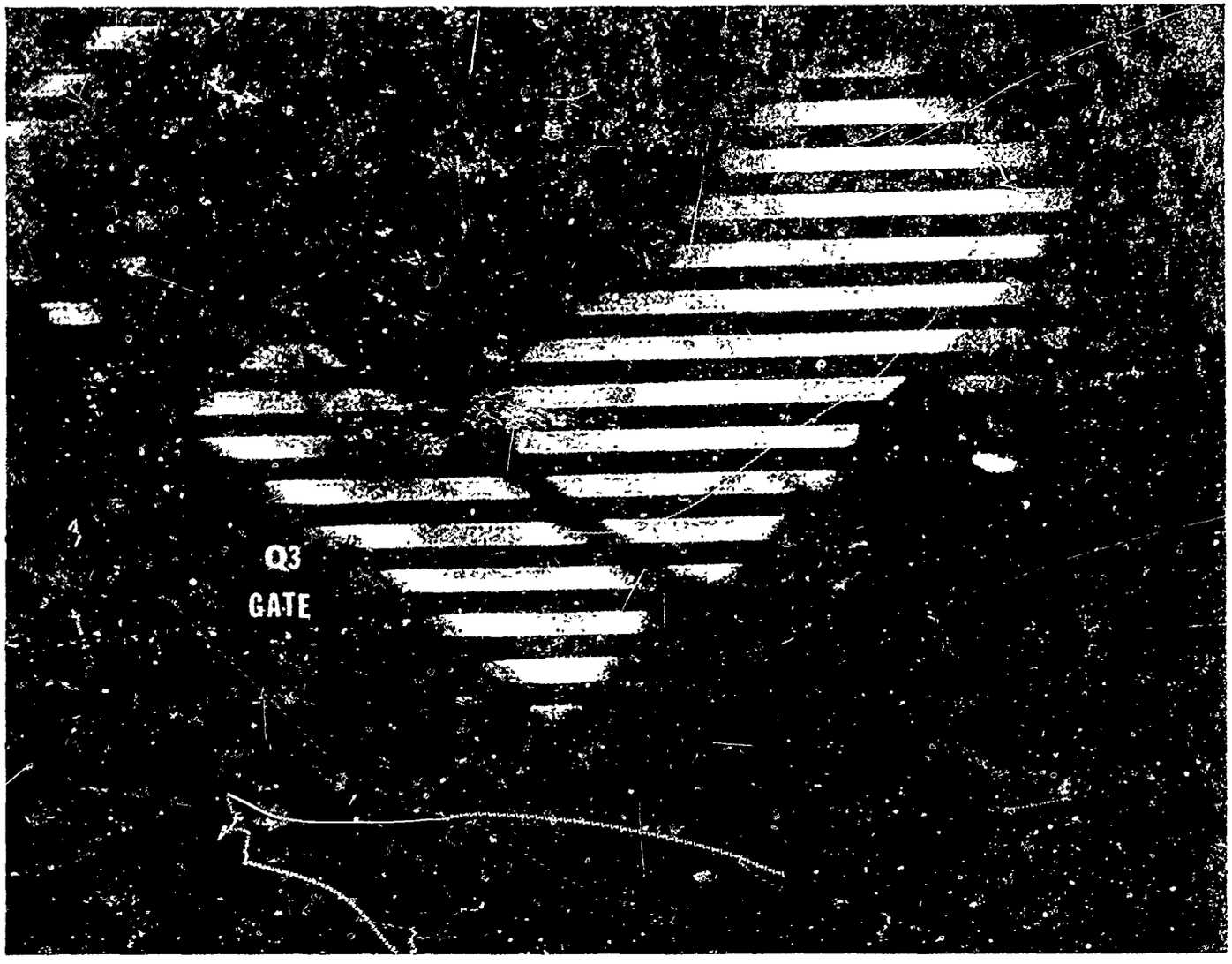


Photo 3-20 Voltage Contrast Micrograph of Properly Functioning Transistor. Compare to Photo 3-19. 1.3 KV, Mag. - 4000X

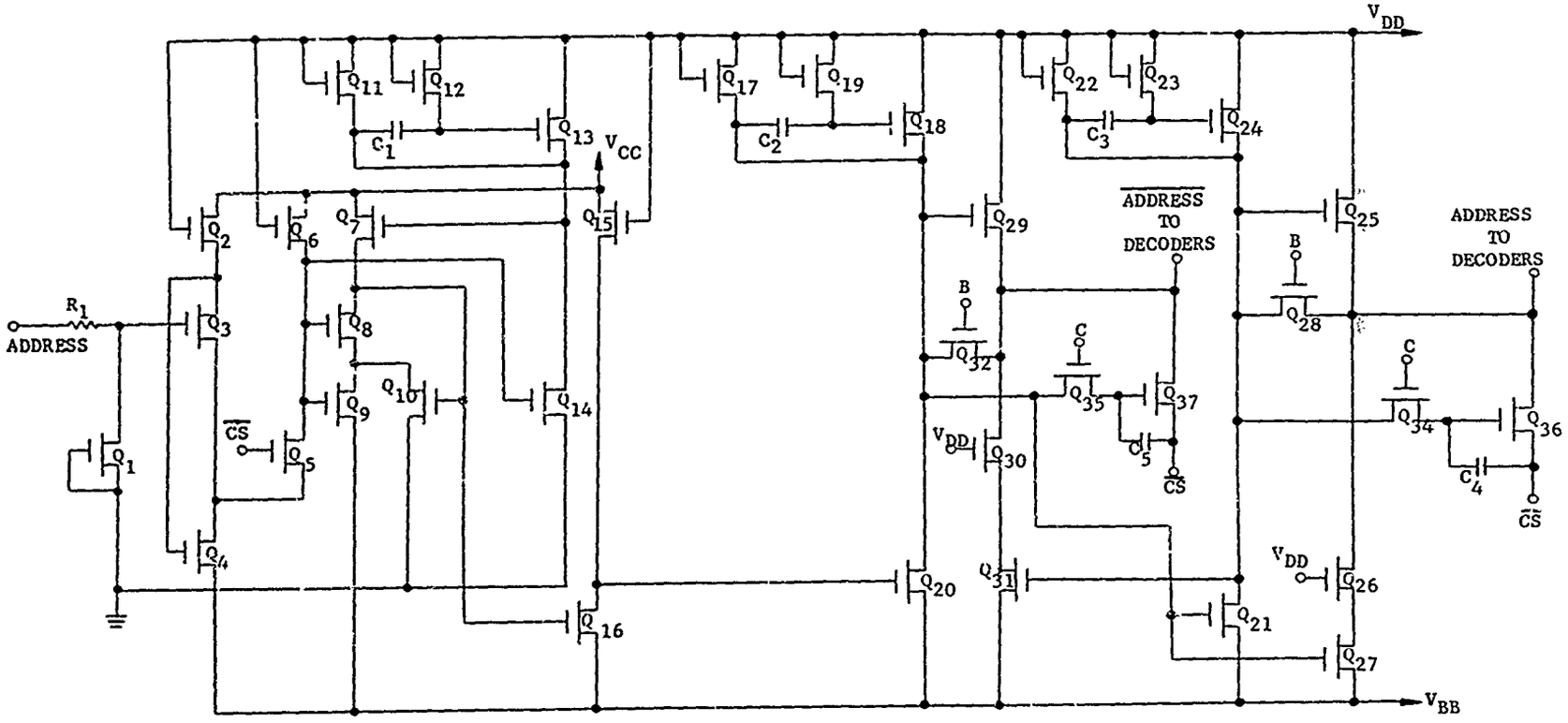


Figure 3-1 Schematic, Row Address Buffer. Column Address Buffer - Identical

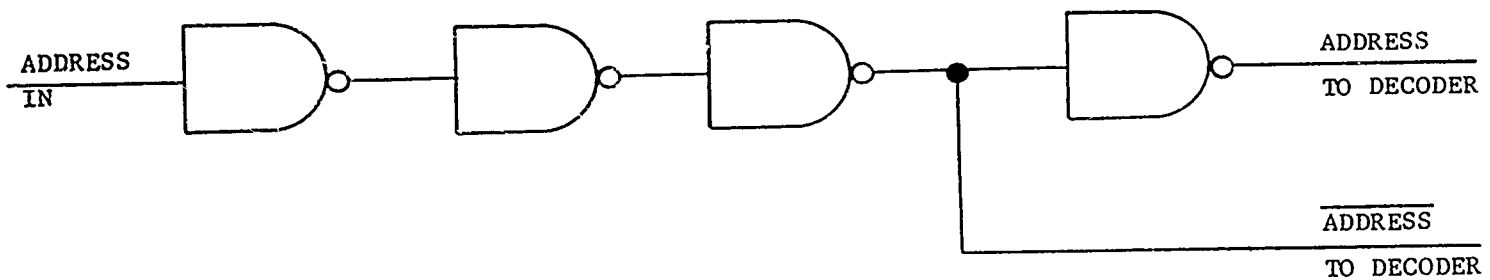


Figure 3-2 Logic Diagram, Address Buffer. Row and Column are Identical.

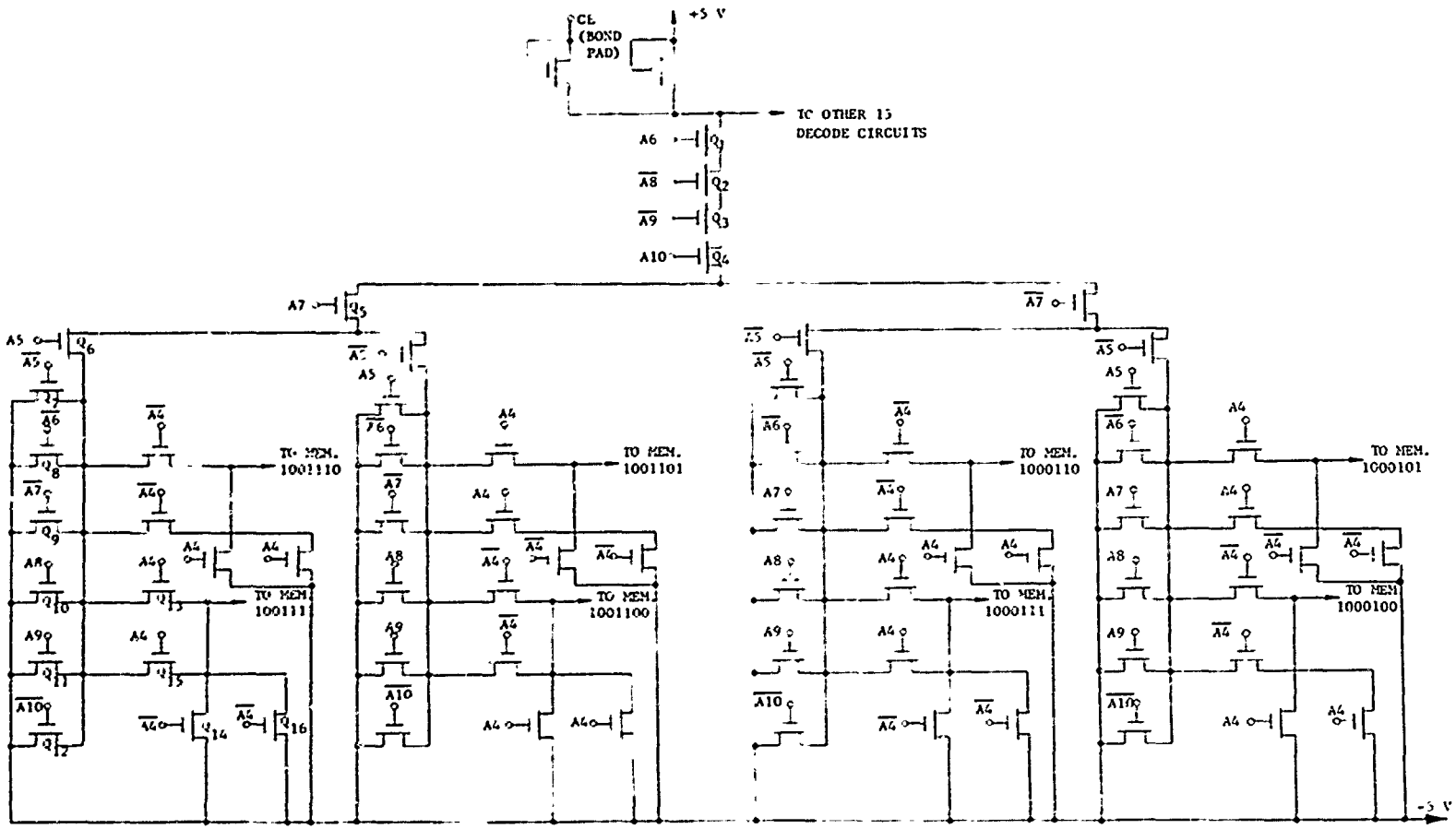


Figure 3-3 Schematic, Row Decode

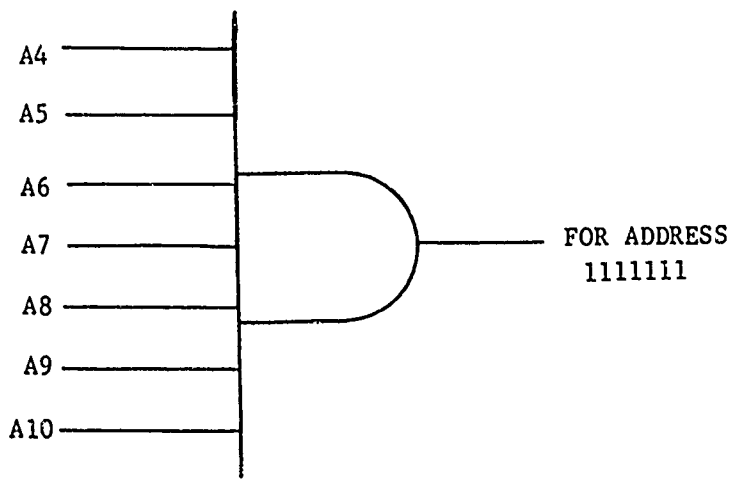


Figure 3-4 Logic Diagram, Row Decode

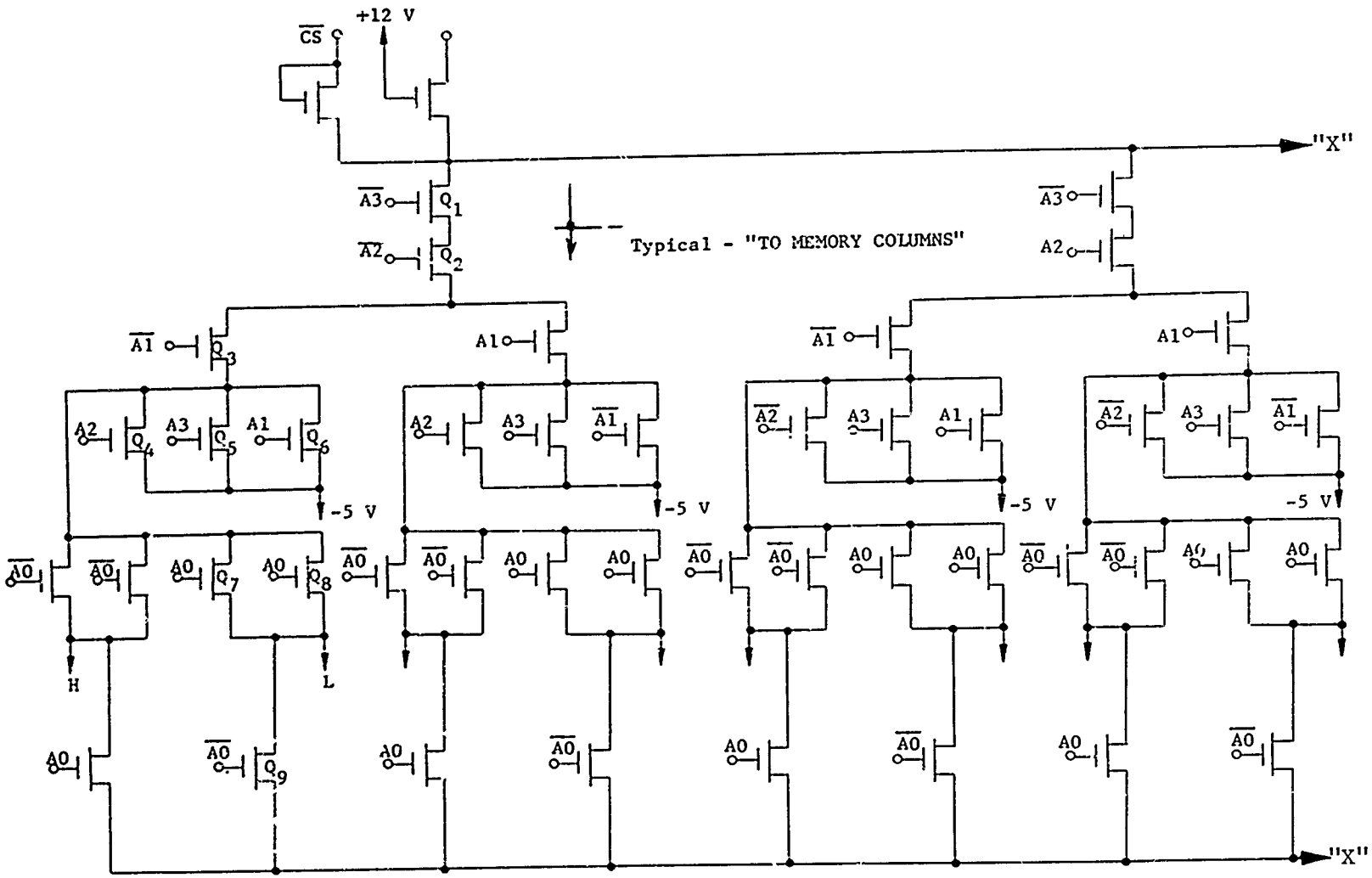


Figure 3-5 Schematic, Column Decode. (continued on next page)

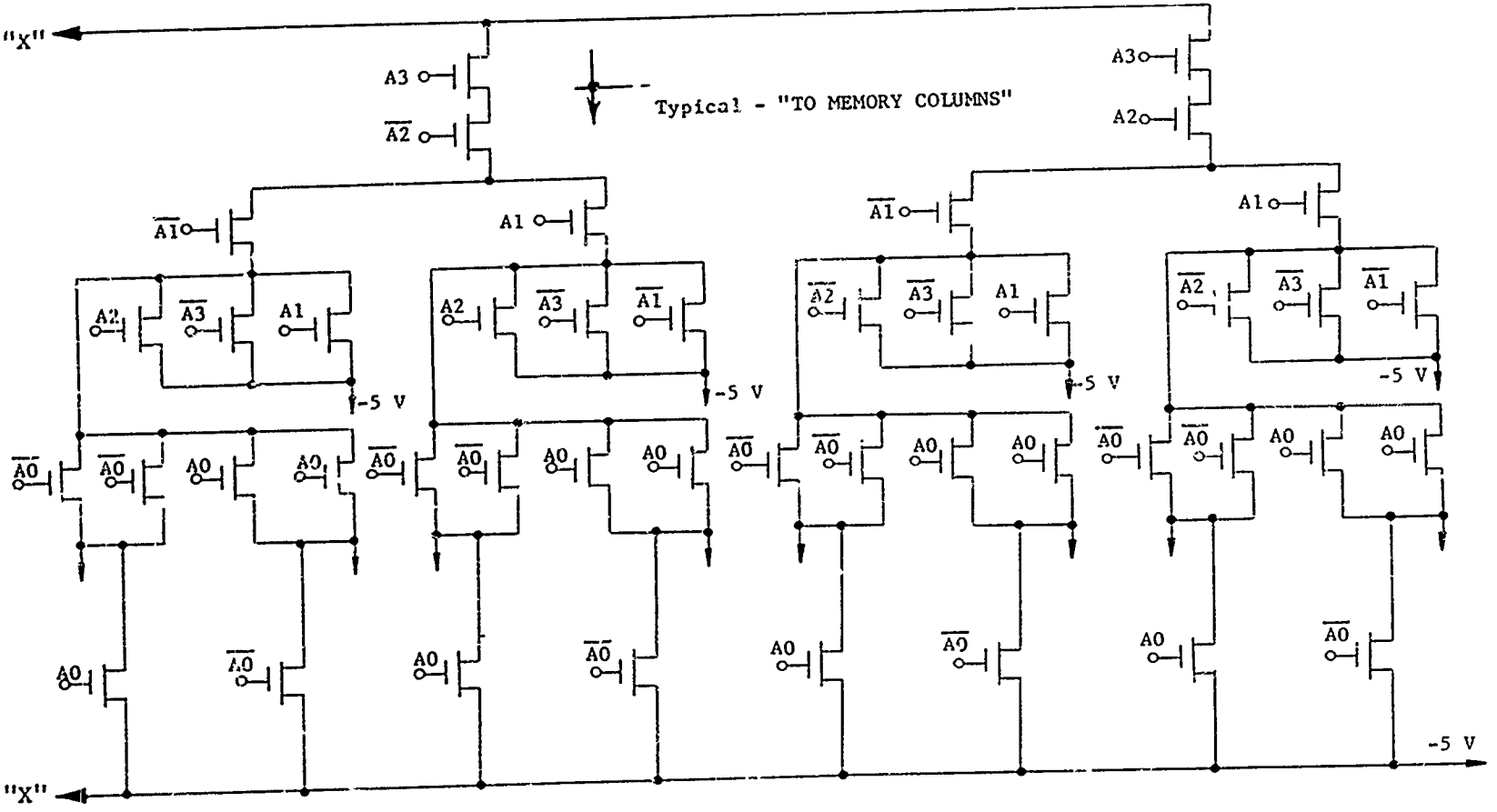


Figure 3-5 (concluded from previous page)

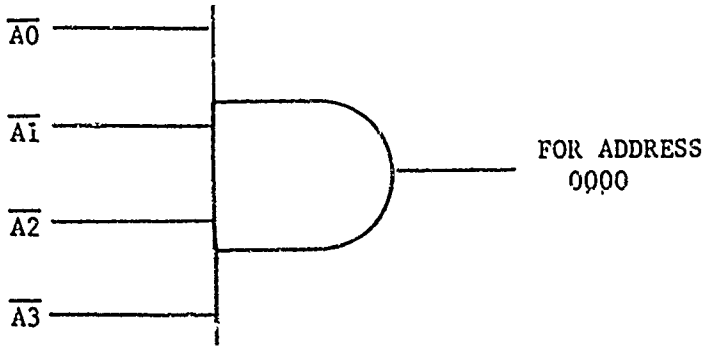


Figure 3-6 Logic Diagram (typ), Column Decode

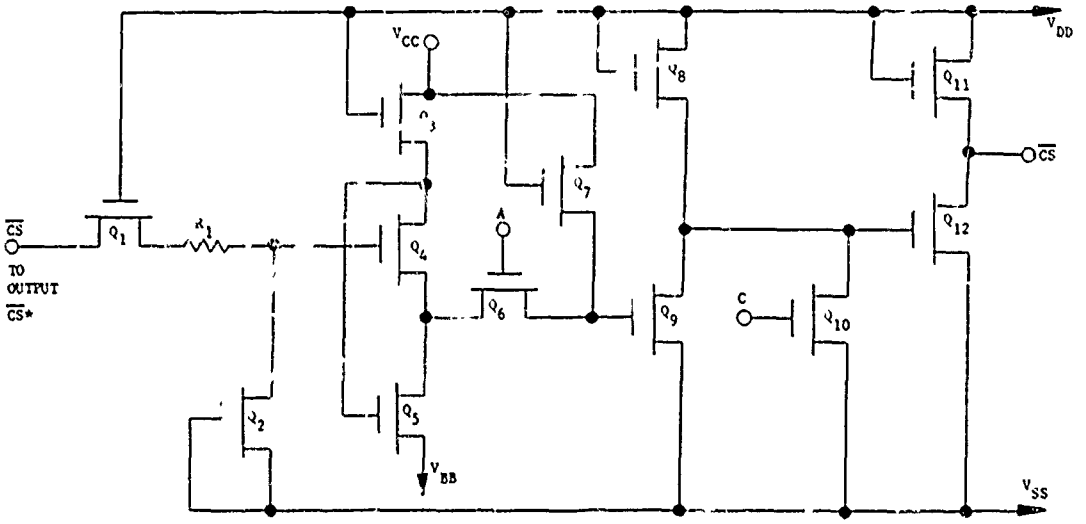


Figure 3-7 Schematic, Chip Select

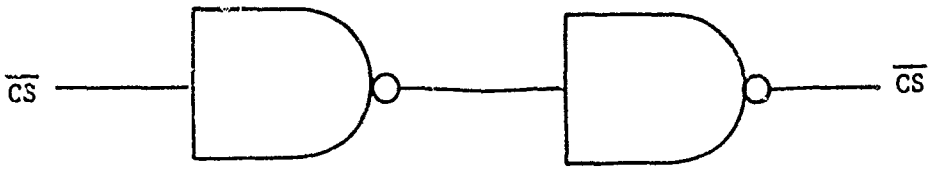


Figure 3-8 Logic Diagram, Chip Select

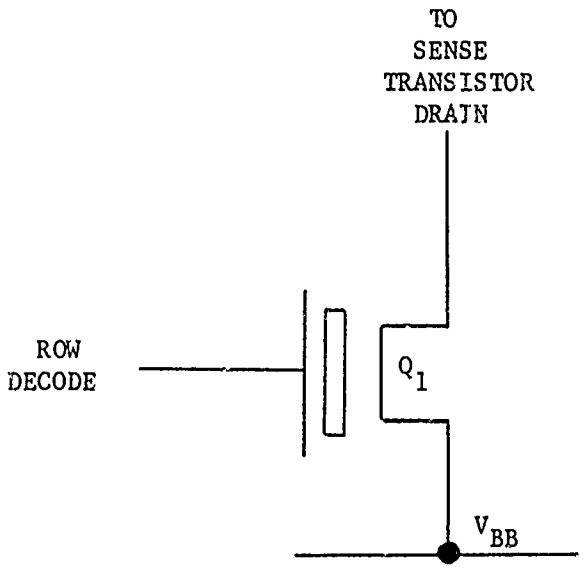


Figure 3-9 Typical Memory Cell

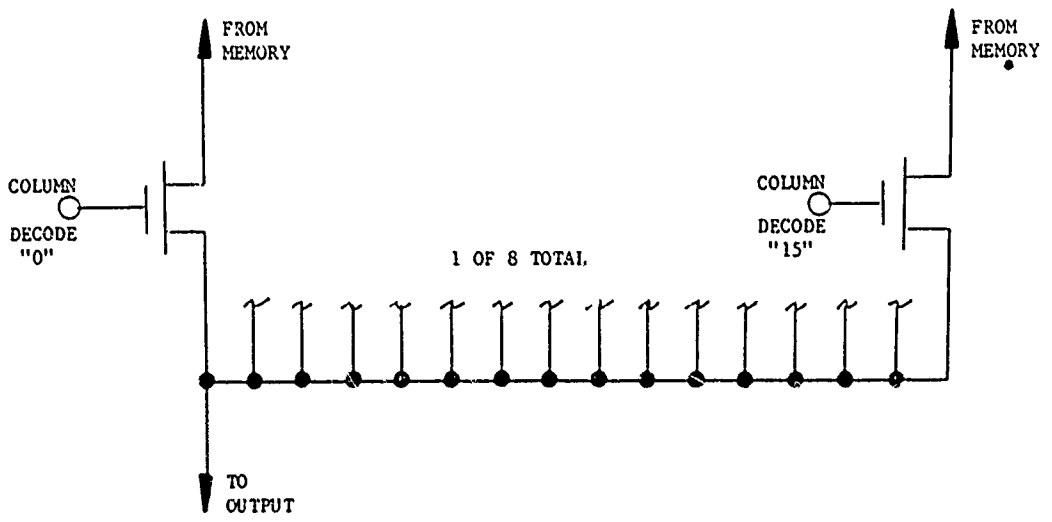


Figure 3-10 Sense Transistor

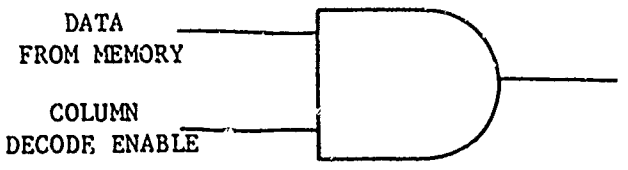


Figure 3-11 Logic Diagram, Sense Transistor

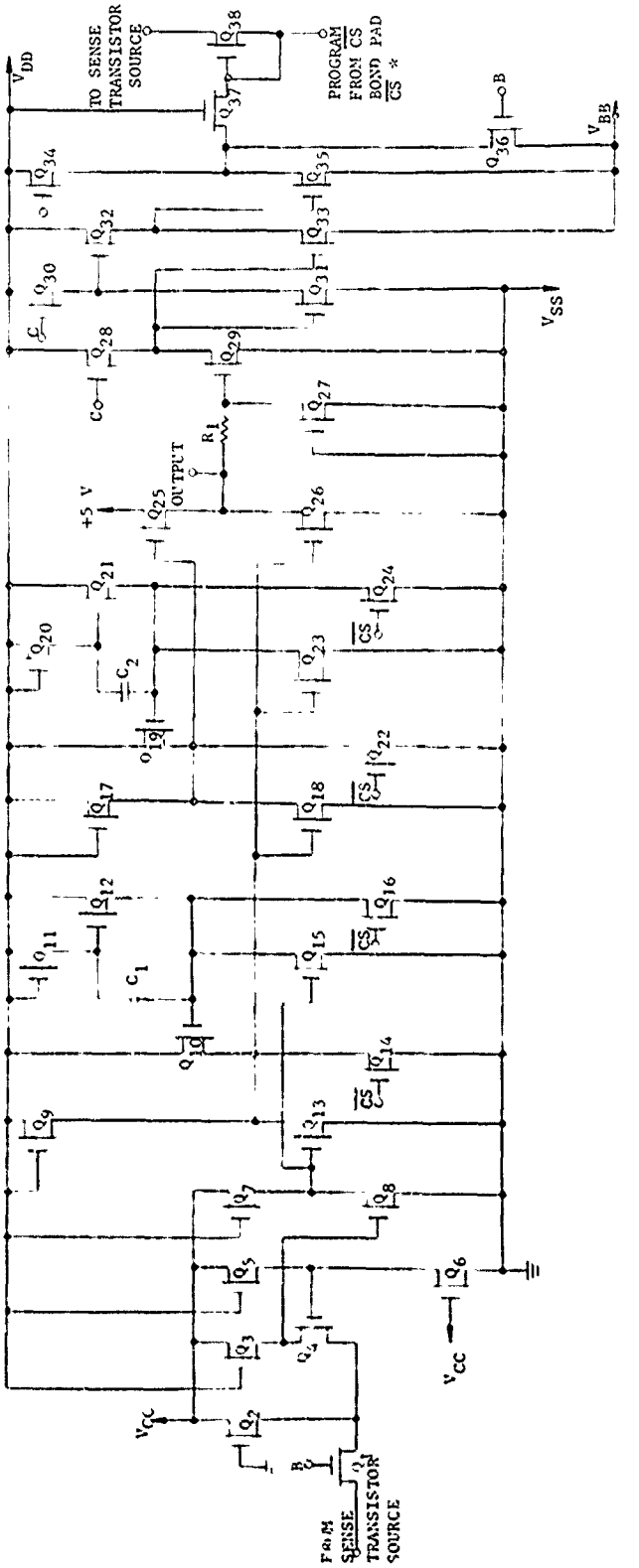


Figure 3-12 Schematic, Output

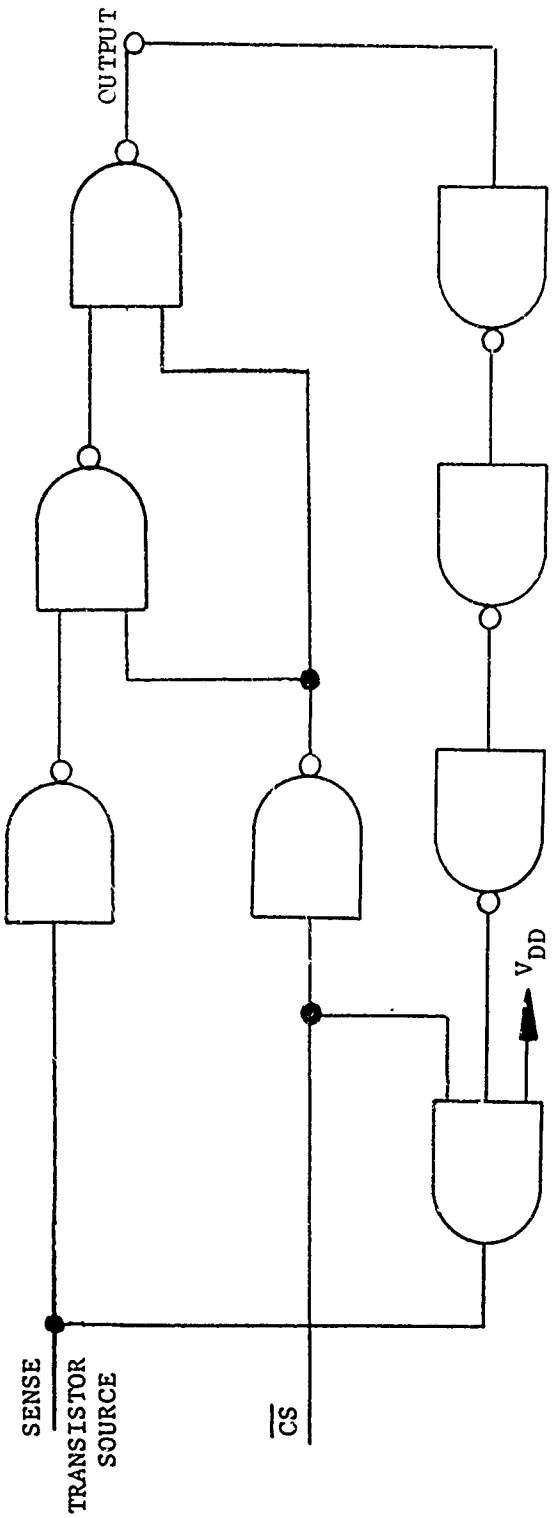


Figure 3-13 Logic Diagram, Output

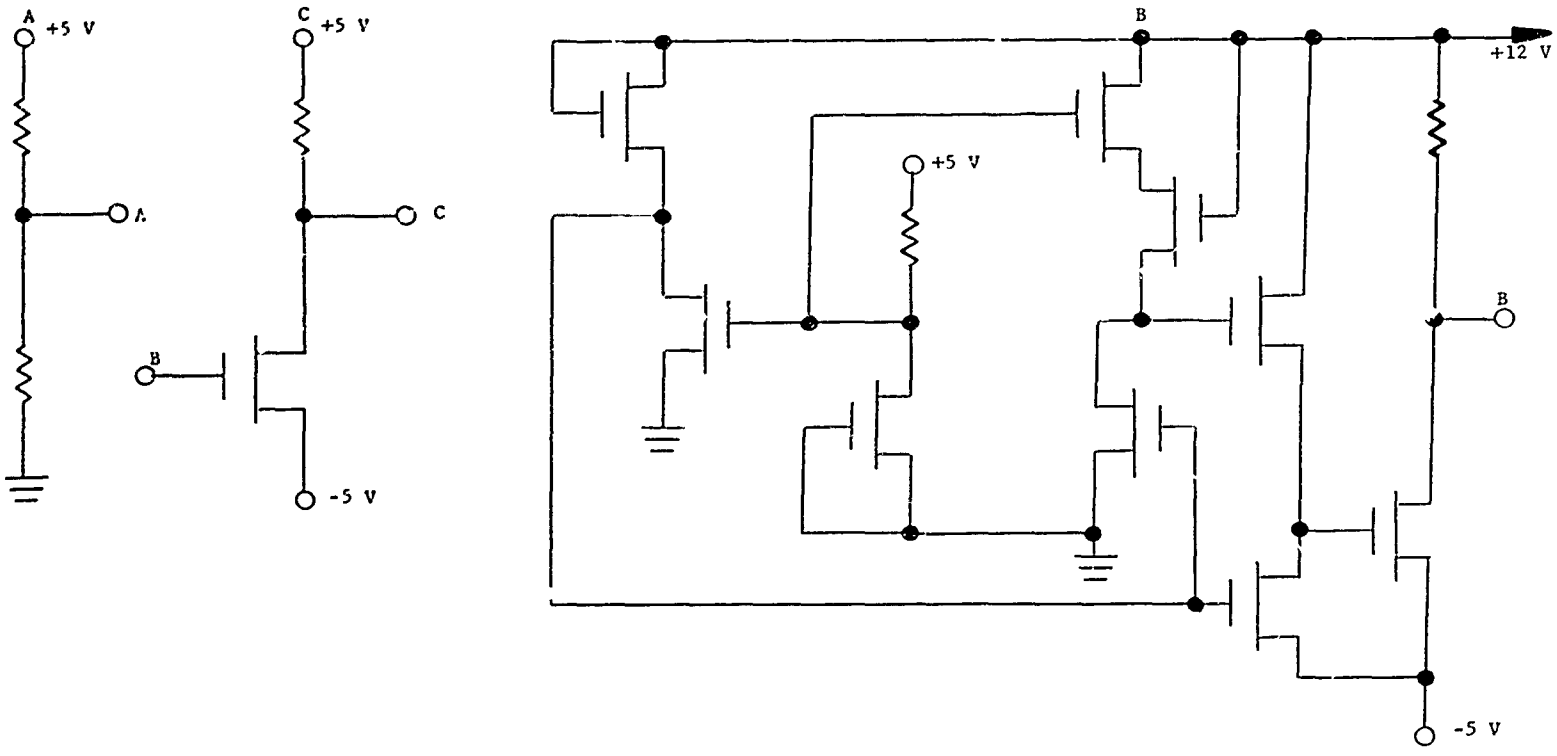


Figure 3-14 Schematic, Reference Generators

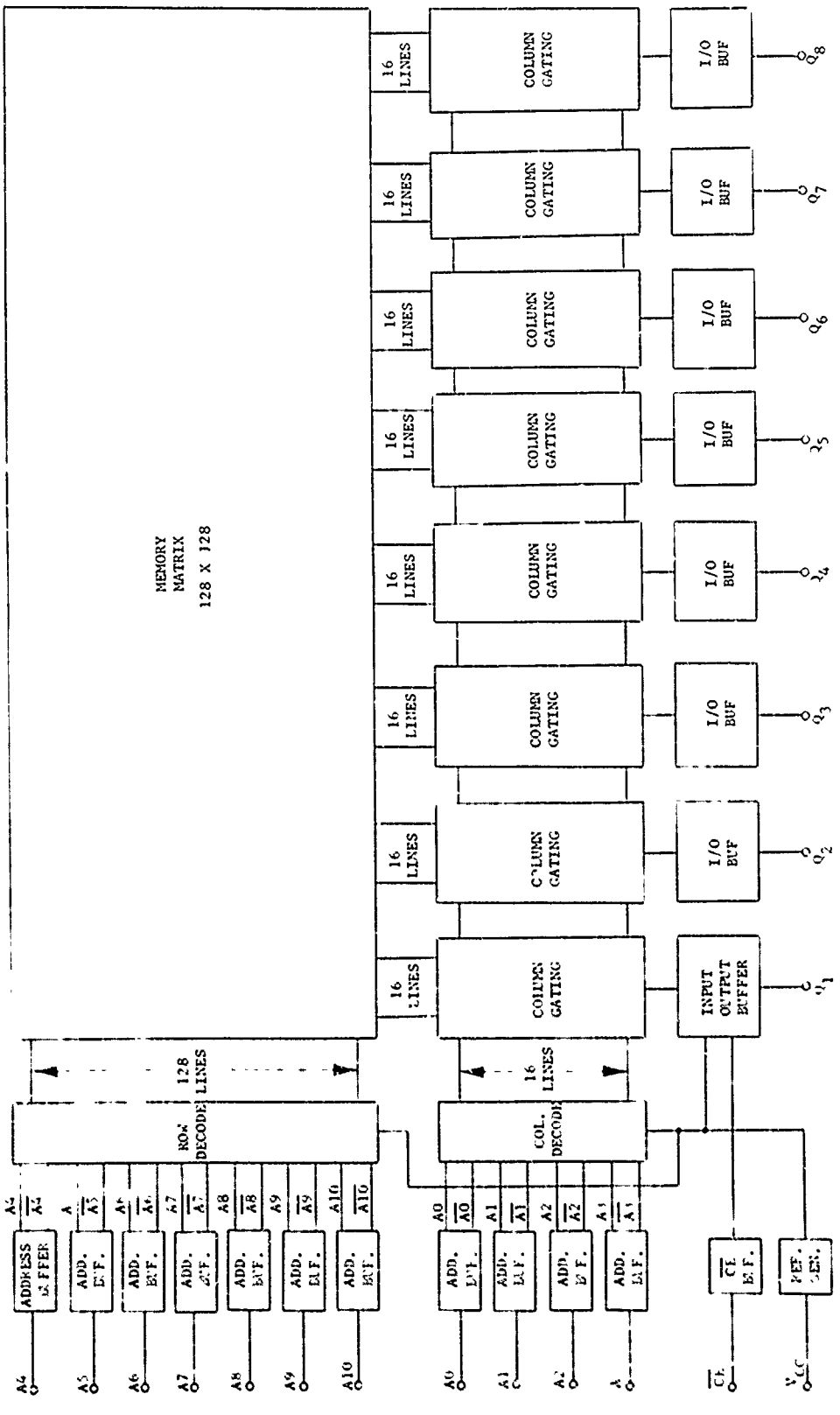


Figure 3-15 Block Diagram

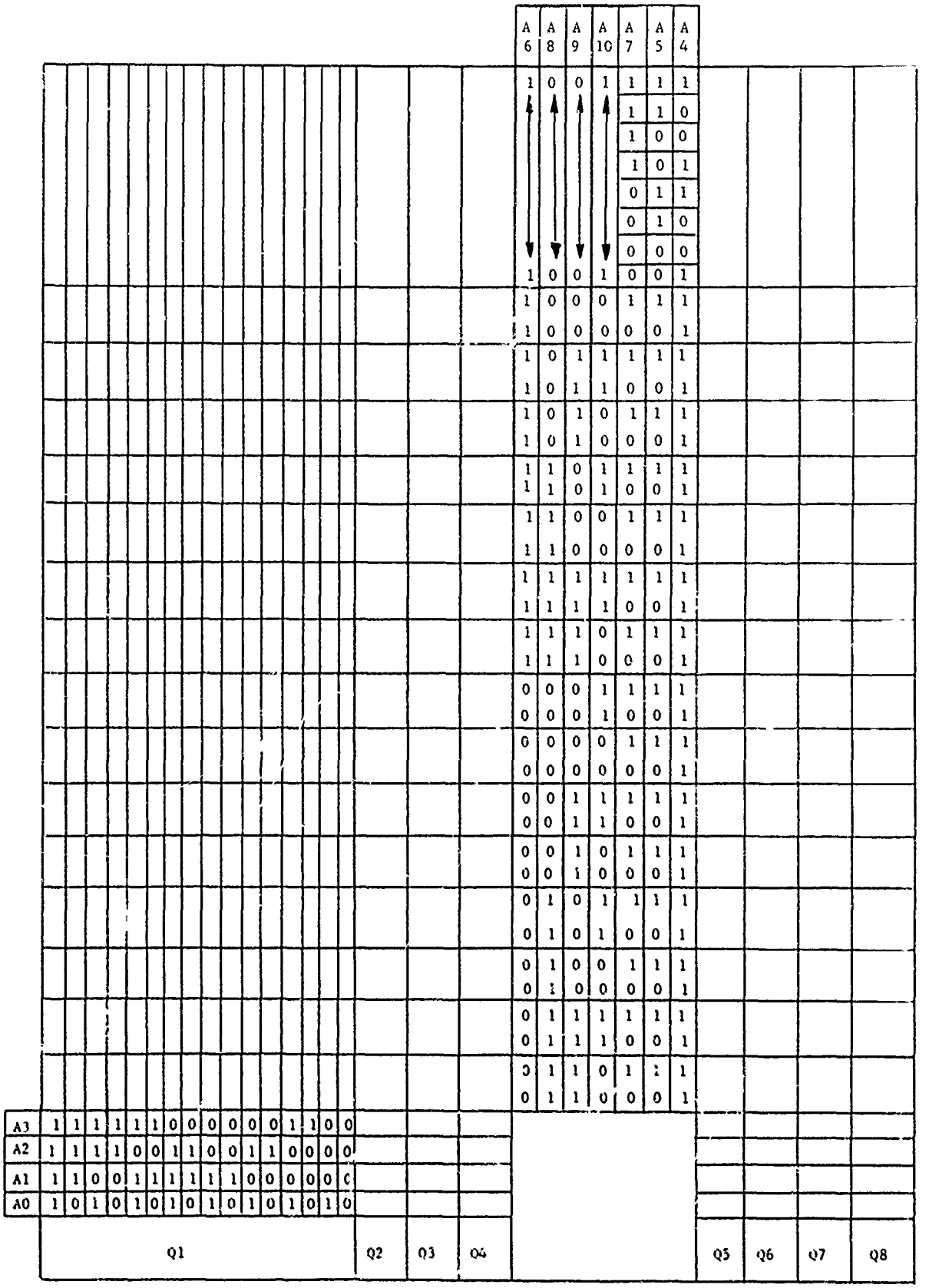


Figure 3-16 Bit Map

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4.4 256 BIT STATIC RAM (BIPOLAR)

Device Description

This device is a 256 x 1 bit high speed Bipolar Static Ram. The version evaluated provides three chip select inputs and a three state output circuit. The device is packaged in a 16 lead ceramic DIP with a KOVAR lid.

Electrical Characterization

Five devices of this part type were used for this program. These were purchased as electrically good devices which had passed the suppliers electrical testing.

The DC parameters were not reverified upon receipt. The five devices were functionally tested to verify proper functional operation. The functional test was performed using the memory test circuit and associated equipment described in the functional test section. The functional test verified that each memory word location could be written into and read out independent of all other word locations. The functional test frequency (LSB) was 100 kHz and all five devices were verified to function correctly.

Package Delid and Glass Passivation Removal

This device package is a ceramic dip with a metal lid. The lid was removed by thinning the metal using a 400 grit abrasive wheel. When the metal lid is thinned to the point of "oil canning" the grinding is stopped. A sharp knife was used to cut through the metal at a corner of this "oil canned" surface. This corner was carefully lifted and the lid was peeled back. Care was taken not to contact the interconnect wires or bond lands.

Cleaning of the chip surface or package cavity is not usually required when using this delid procedure.

The glass passivation was removed using a commercial siloxide etchant. This etchant is prepared specifically for removing deposited glass. The etch rate is estimated to be 40 angstroms per second at room temperature. The first device S/N 2 was etched in 30 second increments followed by DI water and isopropyl alcohol rinses. After each 30 second etch exposure the device was examined at 100X with a light microscope. The objective is to obtain brilliant oxide coloration without severe metallization under cutting. This was achieved after eight 30 second etching steps.

Following glass removal the functionallity of device S/N 2 was verified. The device functioned properly. Photograph 4-1 shows the complete die photo. Some functional circuit blocks are apparent in this photograph. However, as will be seen, the location and identification of individual circuits and transistor cells is much easier and straight forward using voltage contrast.

Circuit Characterization

Device S/N 2 was placed in the SEM using a 16 pin dip test socket and electrical connector and harness assembly. This provides the necessary electrical connections between the test device and an external connector on the SEM specimen stage. The functional test system is then connected with the test device through this external connector. No special device preparation was necessary to reduce extraneous charging effects for voltage contrast examination. The general procedure avoids direct beam landings on non-conductive surfaces of the device packages and test socket. This reduces the influence of these surfaces by decreasing the charge accumulation.

An acceleration voltage of 5 kv was selected for evaluation of this device. Being a bipolar device it is not as susceptible to electron beam influence or irradiation degradation. 5 kv will not disturb circuit operation and it provided good circuit voltage contrast. The focused beam current was adjusted to 200 pA.

Overall circuit operation was observed at TV scan rate while all address lines were exercised sequentially. During observation the address frequency is varied to observe the functioning of the various circuit operations. This provides familiarity with the chips functional organization.

Following familiarizaton, the individual functional circuits were examined. The first circuit examined was the row address inverter. Photo 4-2 shows the voltage contrast micrograph for the Al input. In this photo the signal input is at the left side. This is also a good example which clearly shows the V_{CC} (dark) and ground (light) busses as well as the circuit associated with the Al inverter circuit (candy stripe). This photo was obtained while the Al input (pin 1) was following a 1.4 Hz 5 volt square wave signal. Nominal 5 volts and ground were supplied to the circuit.

A light photograph of the Al circuit is shown in photo 4-3. The inverter outputs are the crossunders which connect with the collectors of Q5 and Q3. Secondary Electron Images (SEI) and EBIC images were photographed for the Al inverter circuit. The SEI photo provides a reference for locating junction response areas from the EBIC photo. The EBIC response is primarily dependent upon the interconnection between the circuit and SEM sample current amplifier (SCA) and the internal circuit configuration of the device under evaluation. Closed loop current paths internal to a device can circumvent the SCA circuit. This internal path cannot be eliminated without opening the circuit paths. However, the detected EBIC response can be changed by selecting different circuit terminal combinations. Photos 4-4 and 4-5 shows the response obtained with terminals 1 and 16 connected to the SCA and terminal 8 connected to ground. The addition of pin 1's connection to the SCA added D1's EBIC response. The acceleration voltage used for EBIC evaluation of this device was 20 kv. The EBIC micrograph shows transistor Q2 is a dual emitter device. Using the four Al circuit photos the circuit was traced and the schematic was generated. The circuit schematic is shown in Figure 4-1. This memory device uses Schottky transistors and in some cases saturation limiting by emitter bypass e.g., Q1 and Q2. The row address inverter cir-

cuits are basic inverters which provide two buffered outputs. One output is in phase with the signal applied to the input and the second is the complement of the input. There are four row address inverters and each generates two address signals. These eight signals are supplied to the row decode inputs. The logic diagram for the row address inverter is shown in Figure 4-2.

The row decode circuit was examined and photographed. The voltage contrast micrograph is shown in Photo 4-6. This photo was made with A_0 and A_1 row address inputs active (A_0 = 1.4 Hz, A_1 = 2.8 Hz). Addresses A2 and A3 were held low. The narrow black line on the base of the decode transistor occurs when all four decode emitters are high. The width of the black stripe is equal to the positive period of the upper address input (A_1). This verifies that row is addressed only for that time period. The light photo for this circuit is Photo 4-7. The row coding can be determined by identifying the four emitter/address interconnections for each row. The address lines contain wider contact pads at each emitter contact window. Photos 4-8 and 4-9 are the SEI and EBIC micrographs for the row decoders. Pin 16 (V_{CC}) was connected to the SCA and pin 8 (gnd) was connected to ground. The bright lines are boundaries of diffusion tubs common or interconnected with V_{CC}. The collector and emitter diffusions for the decode transistors were just visible in the EBIC micrograph. The schematic circuit for a decode transistor is shown in Figure 4-3. The row decode circuits are single transistor cells which contain four emitters. They function as four inputs AND gates. The emitters for each gate are connected to a combination of four different address lines. When this combination of four address lines are all high the memory row common to this decoder is addressed. Using the combination of eight address lines, one of the sixteen decoders is on for each of the sixteen addresses provided by the four bit (A0-A3) row address word. Figure 4-4 is the logic diagram for this circuit.

The memory cell circuit was evaluated next. Photo 4-10 shows the voltage contrast micrograph for two adjacent memory cells. This photo was made with A_0 cycling at 2.6 Hz, A_1, A_2 and A_3 low, A_4, A_5 and A_6 high and A_7 cycling at 5.2 Hz. Alternating ones and zeros had previously been written into memory. In this photo the row decode is located along top left and the column sense amplifier along the top right. In Photo 4-10 the row decode line is identifed as R/D and the sense amp lines as S/A. The voltage contrast signature shows a "1" state resident in the top row of cells and a "0" state in the bottom row. The light photo for the memory cells is Photo 4-11. The cell containing component identification is cell 241. Photos 4-12 and 4-13 are the SEI and EBIC photos of the memory cells. The EBIC photo was made with pin 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. The EBIC photo identifies the collector, base and the row decode emitter location. The sense amp emitter was not visible. EBIC provides a valuable addition to voltage contrast. EBIC can locate junction anomalies and interjunction shorts without the need of mechanical probing. For example, if a row decode emitter were very leaky or shorted to the base, that cell would not exhibit any contrast at this emitter diffusion. The schematic for the memory cell was developed from these photos and is shown in Figure 4-5. The memory cell is a basic bistable flip flop. The transistors are dual emitter. One emitter pair is used to control the cell ad-

dressing for the row. The second emitter pair is used to change the state of the cell or to sense the cell state. The row decode terminal is common to all memory cells in a single row. When the row decode terminal is low, the cell is unaddressed and is maintained in a stable state. When this terminal is high the conduction state of the cell can be changed by writing in a different state or the cell state can be read. Which operation is performed is determined by the sense amplifier. To set the cell to a specific state either sense amp line is forced high and this causes the opposite transistor in the cell to turn on. To read the cell state the difference voltage between the two sense resistors is measured by the sense amplifier. Writing in a high state turns Q1 off and Q2 on. The logic diagram is shown in Figure 4-6.

Next the column address inverter circuit was analyzed. Photo 4-14 is the voltage contrast micrograph for the A_4 inverter. This photo was taken with 1.4 Hz square wave applied to A_4, pin 7. A problem with voltage contrast, which is especially evident on circuits with thermo compression bonds, is bleedover. This is a condition where the voltage potential on an elevated wire influences the secondary electron yield in an area surrounding the wire. The higher the wire height, the greater the area affected. This bleedover is confusing when using voltage contrast for circuit signal tracing. In Photo 4-14 bleedover is evident in the opposite corner from the A_4 wire bond. Also a comparison can be made between Q2 and Q4. The bleedover was reduced by decreasing the height of the wire in bending it over at the ball bond. However the bleedover was still greater than with ultrasonic bonds.

The light photograph of the A4 inverter is Photo 4-15. Identification of Schottky clamped transistors can initially be suspected by overlap of base metallization contacts into collector regions. This overlap is present on transistors Q1 and Q3. In some cases it is necessary to remove the metallization to verify the presence of Schottky diodes. Photos 4-16 and 4-17 are the SEI and EBIC micrographs for the A4 inverter. The EBIC photo was taken with pins 7 (A4) and 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. The isolation diffusions appear wider than they are. This is due to the diffusion length of the silicon substrate. EBIC provides further information which complements the light and voltage contrast data. Using these data the electrical schematic was developed by tracing the circuit paths and documenting the component interconnections. The electrical schematic for the A4 inverter is described in Figure 4-7. This circuit also employs emitter bypasses to increase switching speed. This circuit like the row address circuit produces a two phase address for the column decode and Figure 4-8 shows the logic diagram.

The four column address inverters connect to the column decode circuit. The voltage contrast Photo 4-18 includes the column decode, sense amplifier and memory cell circuits. This photo was taken with column address inputs A4, A5, and A6 high and input A7 cycling at 1.4 Hz. Alternating ones and zeros had been written into memory. The light photograph for this circuit is Photo 4-19. This photo also included the decode, sense amplifier and memory cell circuits. The SEI and EBIC micrographs for the decode circuit are Pho-

tos 4-20 and 4-21. The connections between the address lines and decode cells can be recognized by the wider pads in the address lines visible in Photo 4-20. The EBIC photo was taken with pin 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. This photo shows the diffusions for the decode transistor and some of the sense amp transistors. The schematic for the decode circuit is shown in Figure 4-9. This circuit is similar to the row decode circuit. This circuit is a four input AND gate as shown in Figure 4-10.

The sense amplifier circuit is the next circuit evaluated. Photos 4-22 and 4-23 are the voltage contrast and light photographs. The sense amplifier circuits are typically the most difficult to evaluate because node voltages are very low values and voltage contrast is difficult to obtain. Again it is helpful to use a device which has the metallization removed. The voltage contrast micrograph and light photo are the same photographs used to evaluate the column decode circuit, (ref Photos 4-18 and 4-19). A number of metal mask modifications were noted on this device. Two points are visible at the arrow in Photo 4-22. The modification provides a circuit disconnect with the sense amp output lines. Photos 4-24 and 4-25 are the SEI and EBIC micrographs for the sense amplifier. The SEI photo provides good visibility of the diffusion cells. The diffusion geometries have unusual shapes to accommodate the circuit interconnections. The EBIC image was obtained with pin 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. This image did not produce a very helpful definition of the sense amp transistor diffusions. Using these photographs and light microscope examination of a die with the metallization removed, the schematic was identified. Figure 4-11 is the schematic for the sense amp circuit. The sense amplifier is the heart of the memory circuit. Transistors Q1 and Q2 control the access to a memory column by the comumn decode and chip select busses. Also they provide the inputs for writing data into memory. Q3 and Q4 are the sense transistors and perform the read function. Resistor R7 is not identified on the photographs because it is located outside of the photo field. The logic diagram for this circuit is shown in Figure 4-12.

The next circuit evaluated is the combination of the data input and write enable inverters. The voltage contrast micrograph is Photo 4-26. This photo was taken with a 1.4 Hz square wave signal applied to the write enable input (pin 12) and the data input (pin 13). A severe amount of bleedover is visible in this photo. This produces confusion in tracing the signal flow. Photo 4-27 is the light photograph and Photos 4-28 and 4-29 are the SEI and EBIC photographs for this circuit. With bleedover nullifying much of the voltage contrast usefulness, it was necessary to develop much of the circuit schematic using the data provided by the other three photos. This increased the appreciation for the data usually provided by voltage contrast. However it should also be appreciated that the information provided by each method complements the data of the others. For example, during the process of developing a schematic, each cell is evaluated using all available data. When it appears that a particular cell is a transistor and the emitter, base and collector terminals are identified, this is checked using the remaining data for agreement. Correlation is important as this is the means of cross checking the accuracy of the schematic. Another valuable resource is the

oxide coloration visible with the light microscope. This can provide diffusion commonality between cells i.e., distinguishing base regions from collectors or emitters. This does require the use of uniform glass passivation removal. Using basically the light and SEI photos the schematic was constructed. This data was checked with the voltage contrast and EBIC photos. Figure 4-13 is the schematic developed for the data in and write enable circuit. Schottky diodes are used throughout this circuit. Also transistors Q3 and Q6 provide emitter bypasses for increased speed. The data input inverter generates an in-phase and out of phase signal from that of the input. These output signals connect with the sense amplifiers. The write enable circuit controls the data signal to the sense amplifier. The write enable input must be low to write data into memory. When write enable is high, input data is inhibited and is not applied to the sense amplifier. Also during write enable (input low) the data output circuit is disabled by the write enable not signal. The logic diagram for this circuit is shown in Figure 4-14.

The data read from memory leaves the sense amplifier as two out of phase signals. These two signal phases are converted to a single phase signal by the sense amplifier discriminator. The voltage contrast micrograph for this circuit is shown in Photo 4-30. This photo was taken with alternating ones and zeros written in memory. The memory was addressed through all 256 word locations with the least significant bit frequency of 1.4 Hz. The voltage levels through the discriminator circuit for the most part were below the visual detection level. This required developing the schematic using primarily the light Photo 4-31, the SEI Photo 4-32 and the EBIC Photo 4-33. This is a simple differential detector circuit and can be easily drawn using either the light or SEI photo. The EBIC image for this circuit portrays about one-half of this circuit. This image was photographed with pins 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. Figure 4-15 is the schematic for the discriminator circuit. The Schottky junctions are easily identified for the diodes in the SEI Photo 4-32. The logic diagram for the discriminator is Figure 4-16.

The discriminator output connects with the input of the data output circuit. The voltage contrast photo for the data output circuit is Photo 4-34. This photo was taken while reading alternating ones and zeros from the 256 word locations at an LSB address rate of 2.1 Hz. The voltage contrast data response is visible beginning with transistor Q3. Photo 4-35 is the light photograph of the output circuit. Point "A" is the data input and point "B" is the output circuit disable from the write enable buffer. Photos 4-36 and 4-37 are the SEI and EBIC micrographs for the output circuit. The EBIC photo was made with pins 16 (V_{CC}) and 6 (output) connected to the SCA and pin 8 (gnd) connected to ground. The majority of transistor cells are visible in the EBIC photo. The four photographs were used to develop the output circuit schematic in Figure 4-17. The data output circuit is basically a direct coupled amplifier. The output of the sense amplifier discriminator is a low level signal. The output circuit amplifies this signal and transistors Q8 and Q10 are current drivers required for driving interface circuitry. The output circuit is a three state output, high, low and open. The open circuit or high impedance state is the disable state.

This circuit contains two disable lines. One from write enable which disables the output during data writing. The second is a disable from the chip enable circuit. When the write enable disable line is low or the chip select disable line is high the output goes to a high impedance state. The logic diagram for this circuit is shown in Figure 4-18.

The last circuit to be identified for this chip is the chip select circuit. The chip select has three inputs all of which must be at a low state for the chip to be operational. Photo 4-38 is the voltage contrast micrograph for this circuit. This photo was made with CS_2 and CS_3 held low, CS_1 cycling 0 to 5 volts at 1.4 Hz and a static address was selected to produce a high state at the output. The cycling of CS_3 results in the output pin 6 cycling between a high logic state and an off state. The light photograph for this circuit is Photo 4-39. The two lines which connect with the right hand end of resistors R8 and R9 are the disable lines which connect with the sense amplifiers. Photos 4-40 and 4-41 are the SEI and EBIC photographs for the chip select circuit. The EBIC photo was taken with pin 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground. Most of the transistor cells are visible in the EBIC photo. Using the information contained in these photos, the circuit was traced and a schematic was developed. Figure 4-19 is the schematic for this circuit. This circuit is a basic three input OR gate with three inverted outputs. When any one input is high, one output is used to inhibit the data output stage and two outputs are used to inhibit input data to the sense amplifiers. The logic diagram for this circuit is shown in Figure 4-20.

The chip organization is shown in Photo 4-42. This organization is typical for a RAM device. A block diagram for this device is shown in Figure 4-21. The die dimensions are 104 x 125 mils. The chip metallization is aluminum and utilizes a single level system. The wires are gold with thermocompression bonds. The SEI and EBIC micrographs for the total chip are shown in Photos 4-43 and 4-44. The EBIC photo was taken with pin 12 (WE), pin 13 (DI) and pin 16 (V_{CC}) connected to the SCA and pin 8 (gnd) connected to ground.

A bit map was generated for this chip. The row bit sequence progresses serially from the column side. The column bit sequence jumps back and forth along the column decode side. The bit map is shown in Figure 4-22.

Failure Analysis

A failure was generated in device S/N 2 by scribing open metallization.

The device was then given to a second person for failure analysis. Functional testing identified a problem for memory cells common to column address code 0000 (column 2 end). If all ones or all zeros were written into all memory cells the device displayed a correct memory response. When alternating ones and zeros or zeros and ones were written into memory the cells in column zero displayed data errors. An attempt to further isolate the fault by functional testing was unsuccessful.

The device was placed in the SEM with the accelerating voltage set to 5 kv. The circuit was examined while the column addresses were held at zero and the row addresses were cycled through all 16 rows. During the initial functional testing it had been noted that no data errors occurred when the same logic state had been written into all memory cells. This suggested the sense circuits were operating properly. Also errors had occurred only when data other than all ones or all zeros were written into column zero. The column zero cells were examined first in the SEM. While examining the operation of these cells it was noted that the row decode signal for row 14 was not reaching the cell for word 14. This cell is located in column zero. Photo 4-45 shows that the row decode signal does not reach the word 14 cell. Photo 4-46 shows the row decode metal stripe is open. Initially it was felt that this open was not completely responsible for the failure observed in functional testing. In the memory cell schematic Figure 4-5 it can be seen that if the row decode connection with the cell is open, data will be written into this cell whenever it is written into any other cell within the same column. Also this cell will be read out by the sense amplifier when any other cell in the same column is read. What is confusing is that as two cells containing different logic levels were read out simultaneously, the logic level determined by the sense amplifier was inconsistent. To reverify this the functional test was rerun. Logical ones were written in all memory location. Next a logic zero was written into word 14. All memory cells in column zero were read and all but word 1 read out zero. Next all zeros were written into memory and verified by read out. Then a logic one was written into word 14. All memory cells in column zero were read and all but words 1 and 11 read out one. Additional write sequences were checked where the data in a different cell in column zero was changed. The data read out for the cells in column zero showed many different error patterns. This example shows what kind of difficulty can be experienced when attempting to perform failure isolation solely by functional test results.

The failure identified was the failure which had been intentionally introduced. What was thought to be a straight forward failure to isolate and identify turned out to be quite involved.

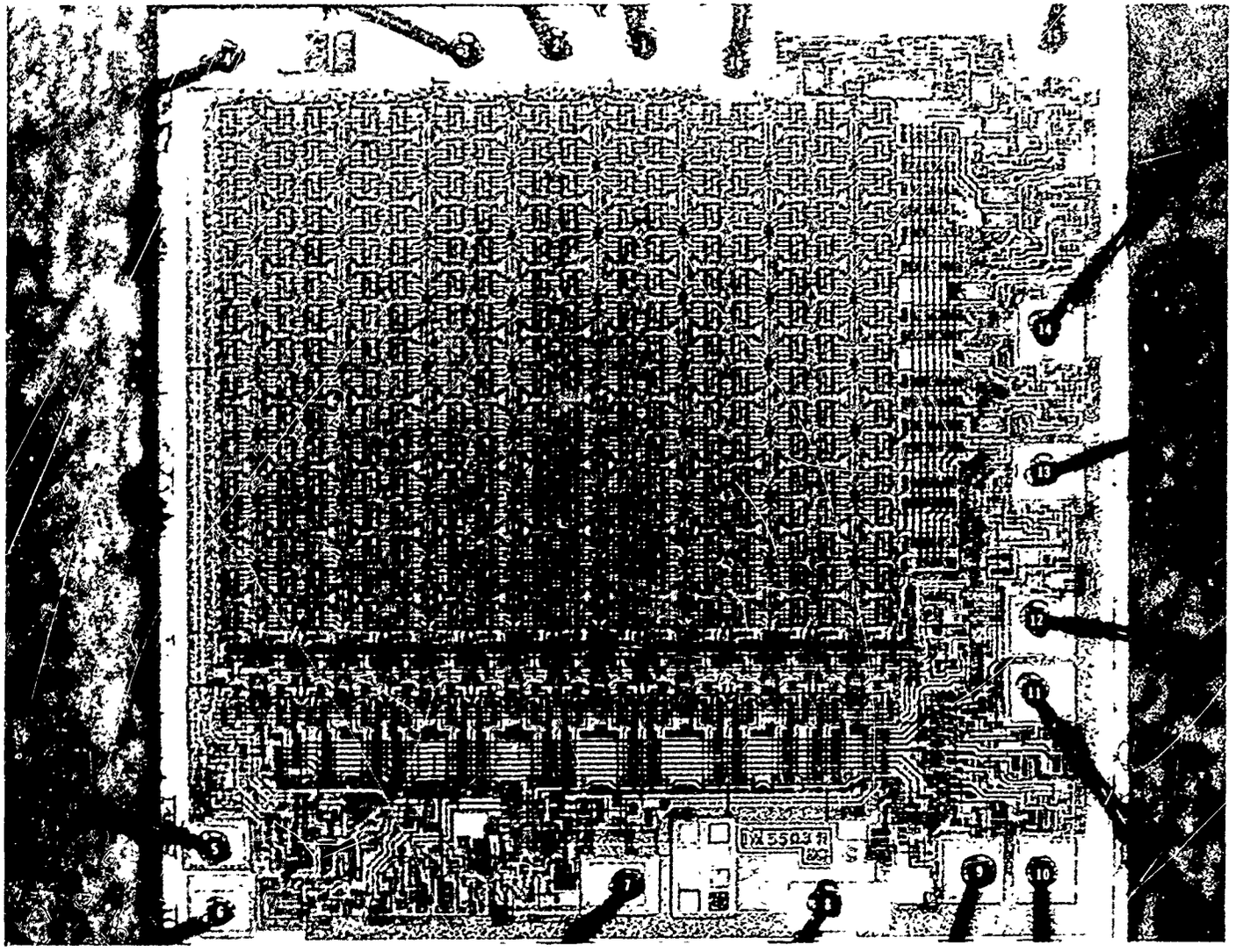


Photo 4-1 Overall View of the Complete Die. Mag. - 45X

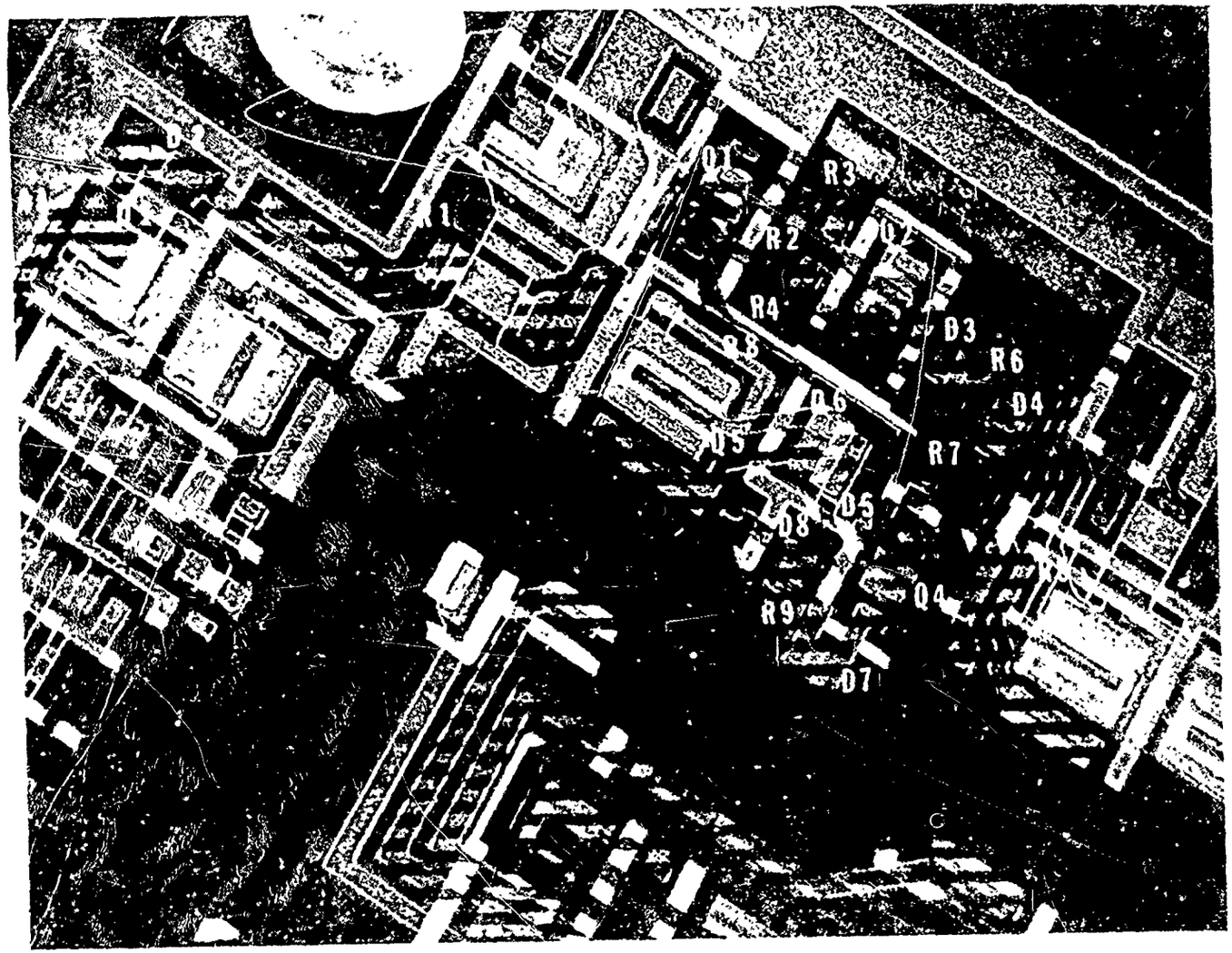


Photo 4-? Voltage Contrast Micrograph of A1 Row Address Inverter. 5 KV, Mag. - 385X

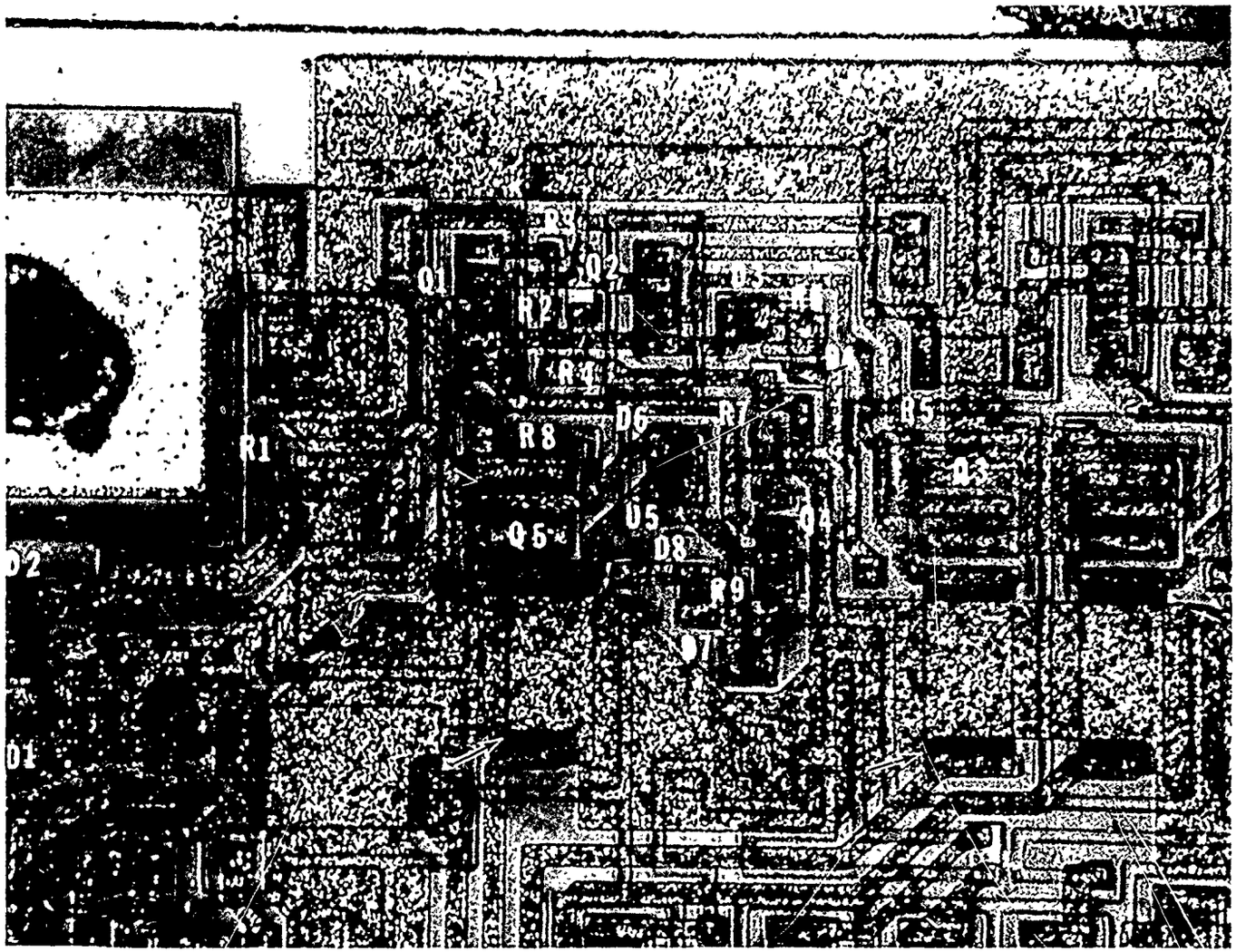


Photo 4-3 Light Photograph of A1 Row Address Inverter. Mag. - 310X

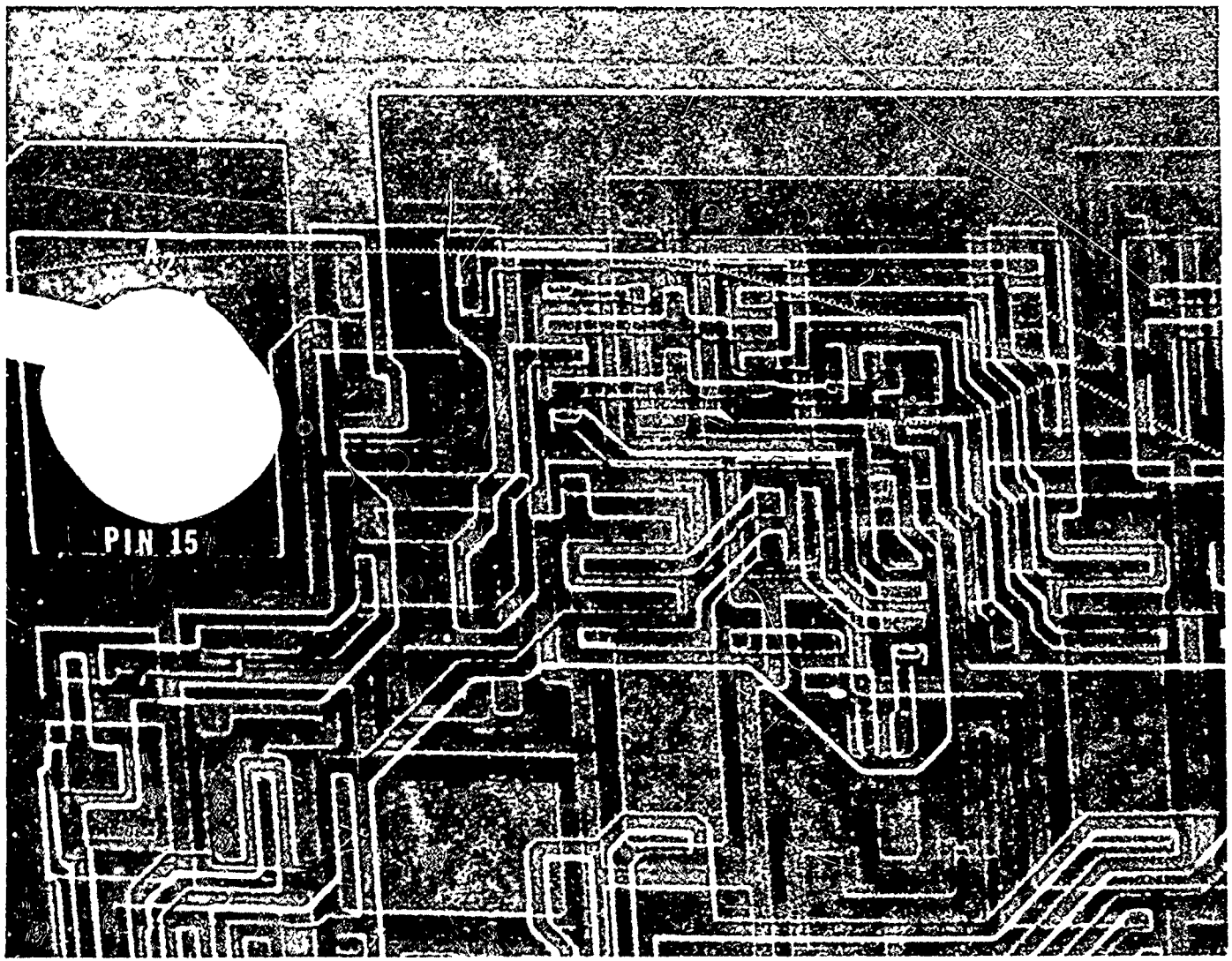


Photo 4-4 SEI Micrograph of Al Row Address Inverter. 20 KV, Mag. - 385X

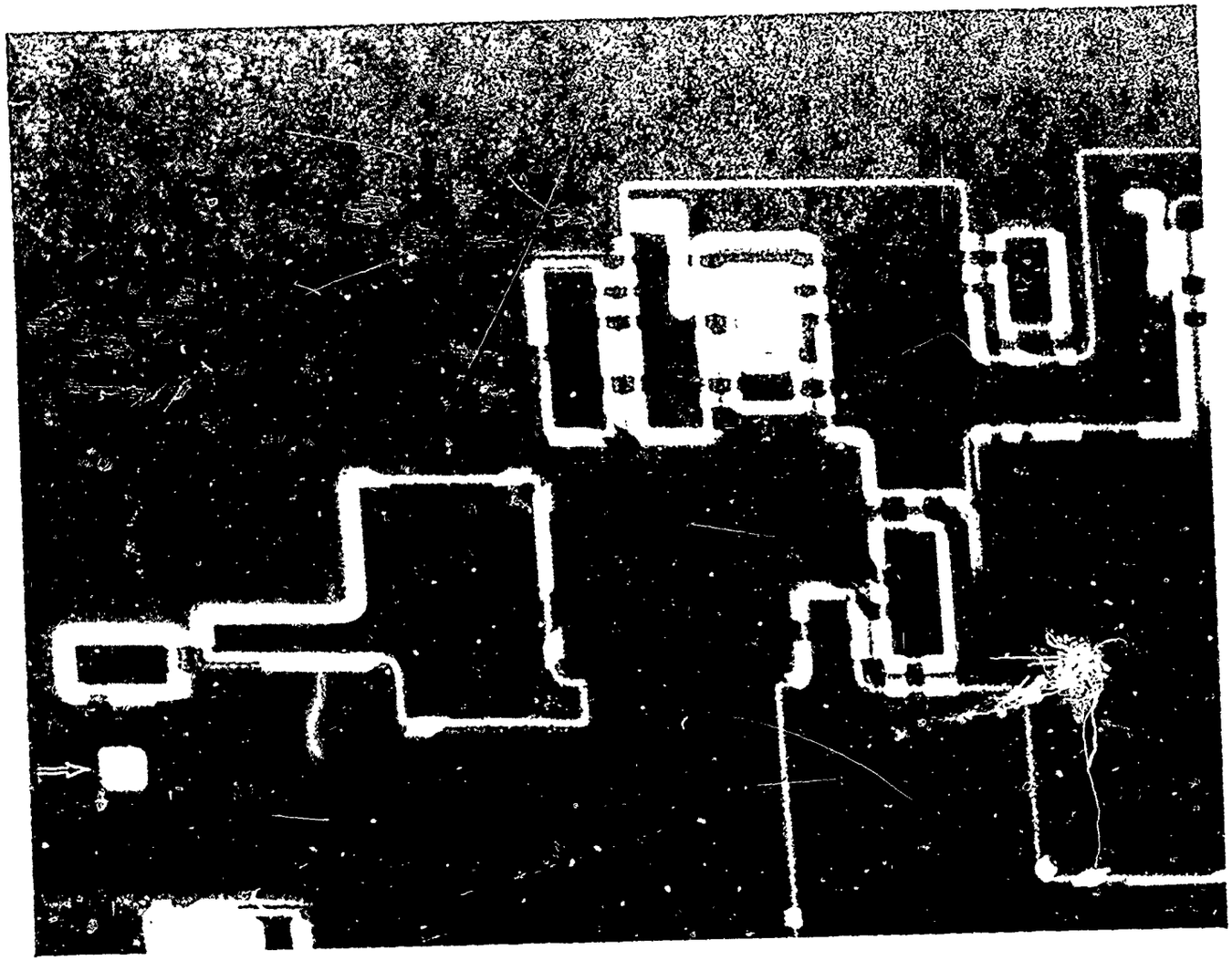


Photo 4-5 EBIC micrograph of 41 Row Address Inverter. Pins 1 and 16 to SCA, Pin 8 to GND. 20 KV, Mag. - 195X

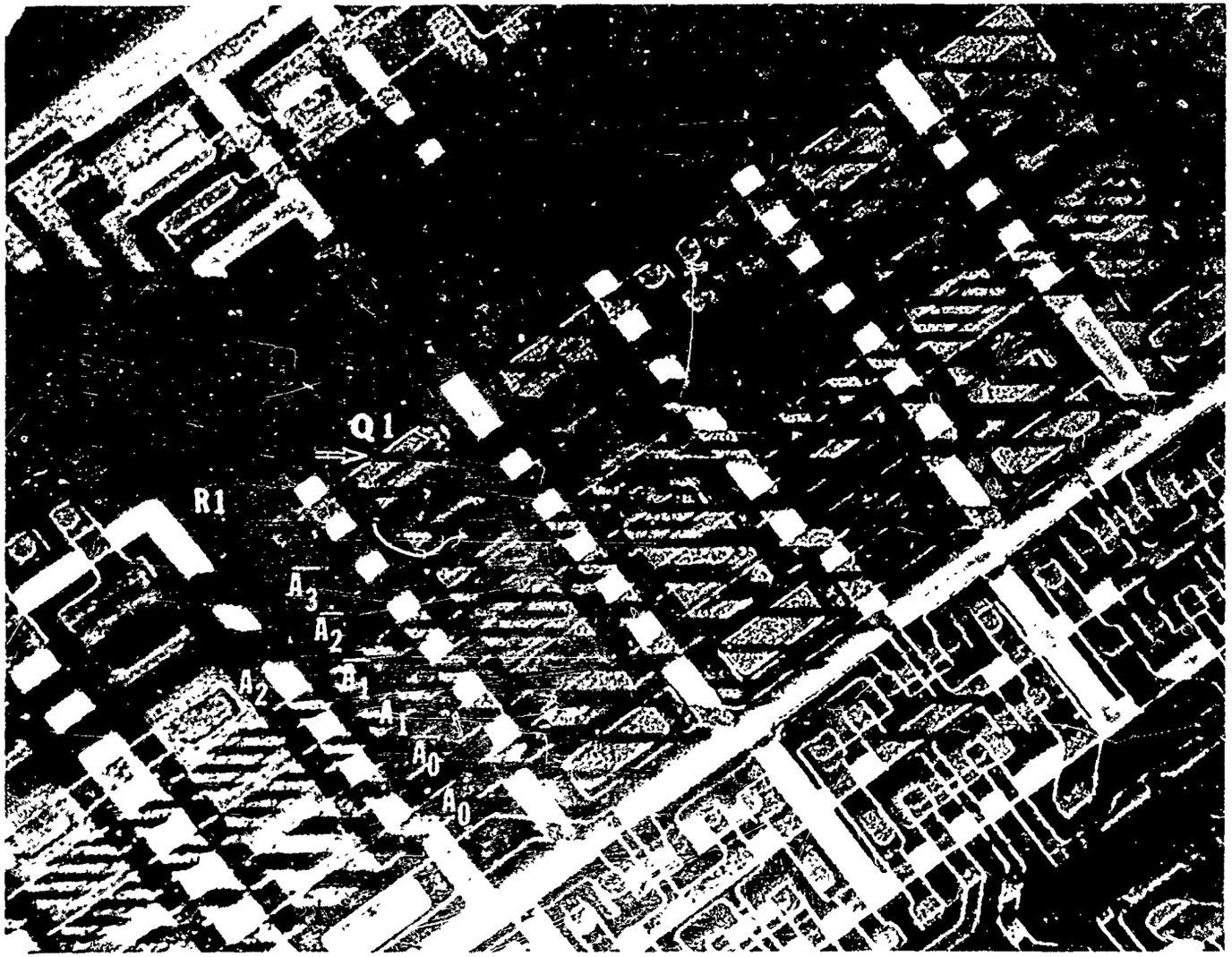


Photo 4-6 Voltage Contrast Micrograph of Row Decode Circuit. Row is Addressed When Base is High (Arrow). 5 KV, Mag. - 575X

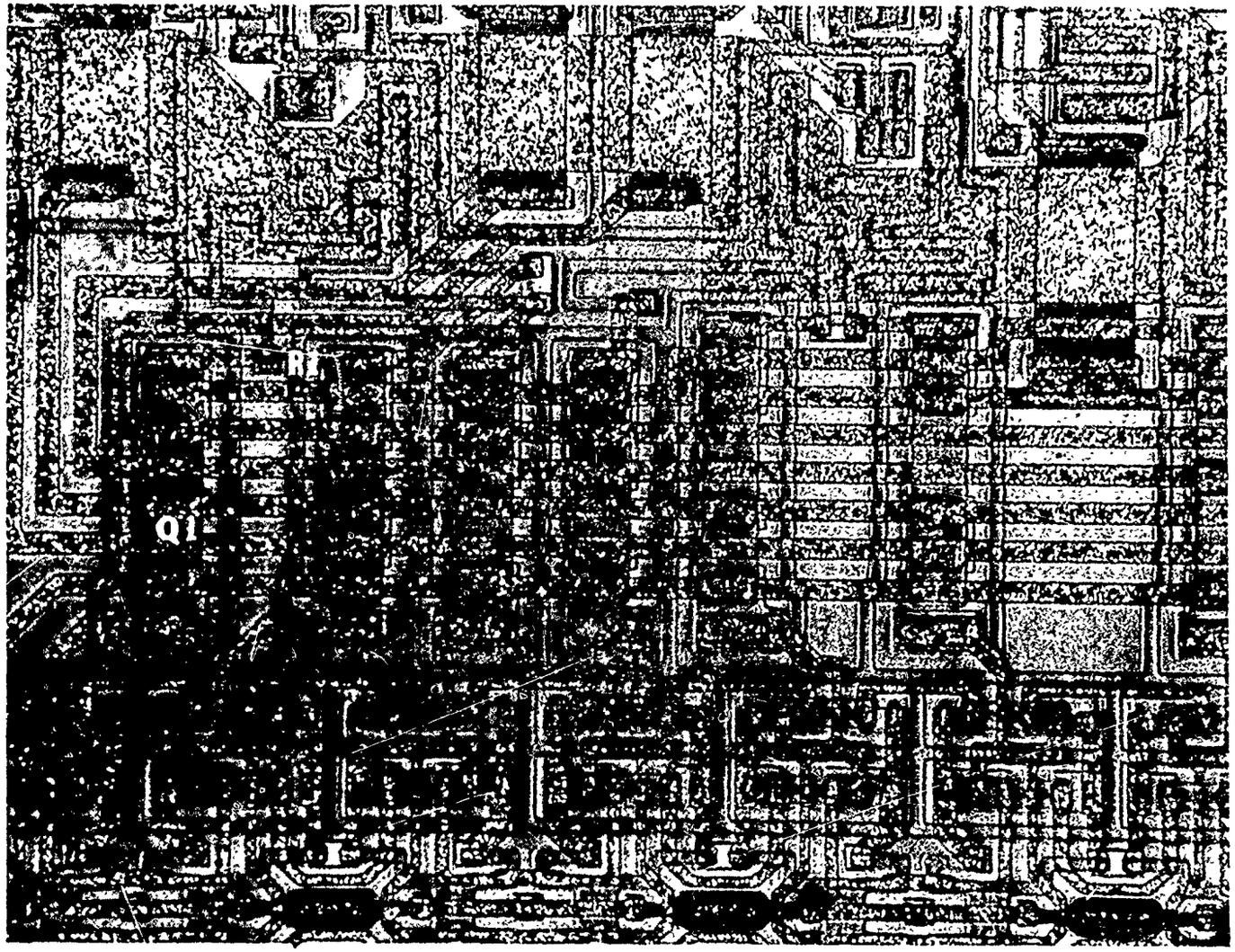


Photo 4-7 Light Photograph of Row Decode Circuit. Mag. - 310X

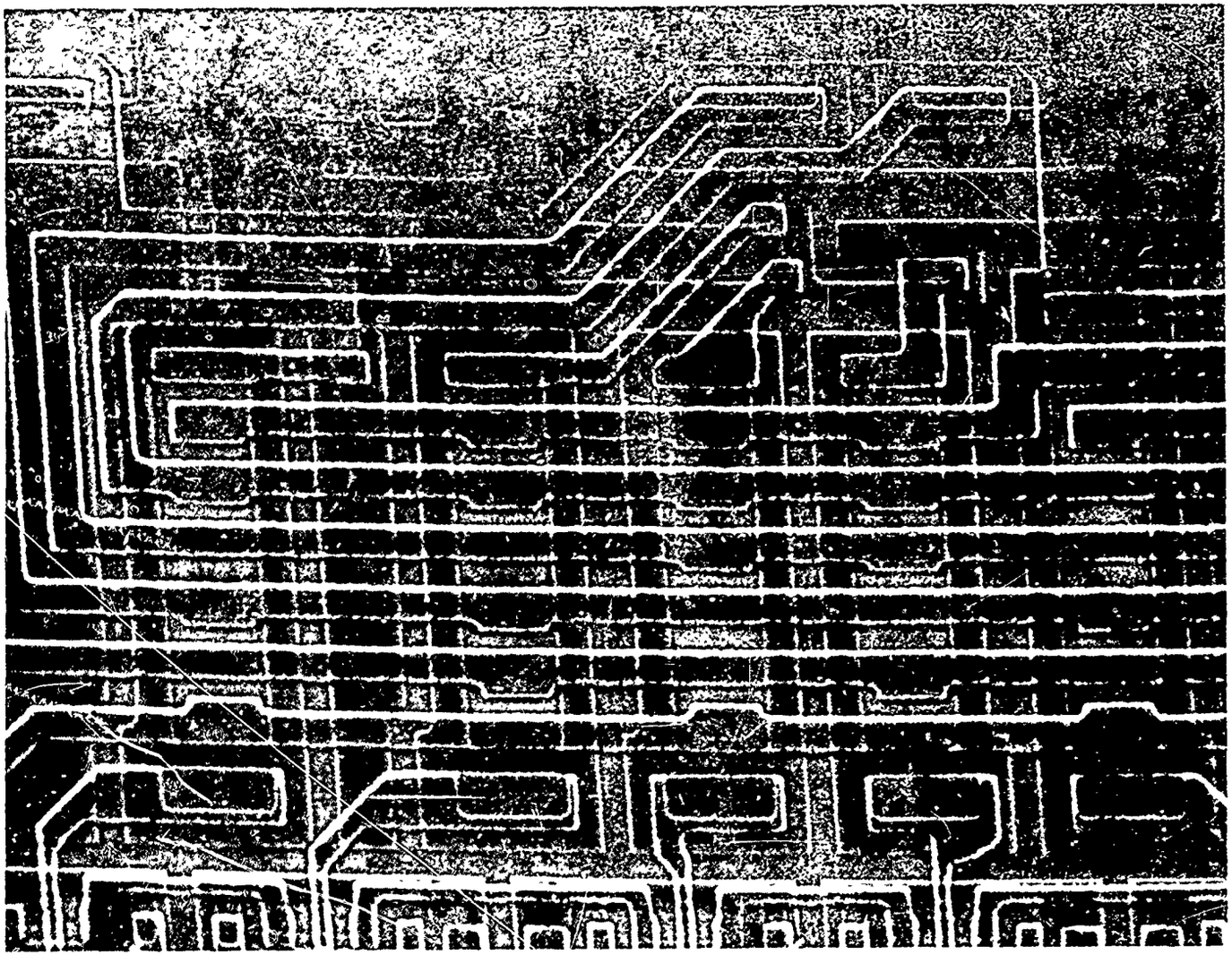


Photo 4-8 SEI Micrograph of Row Decode Circuit. 20 KV, Mag. - 575X



4-9 EBIC Micrograph of Row Decode Circuit. 20 KV, Mag. - 575X

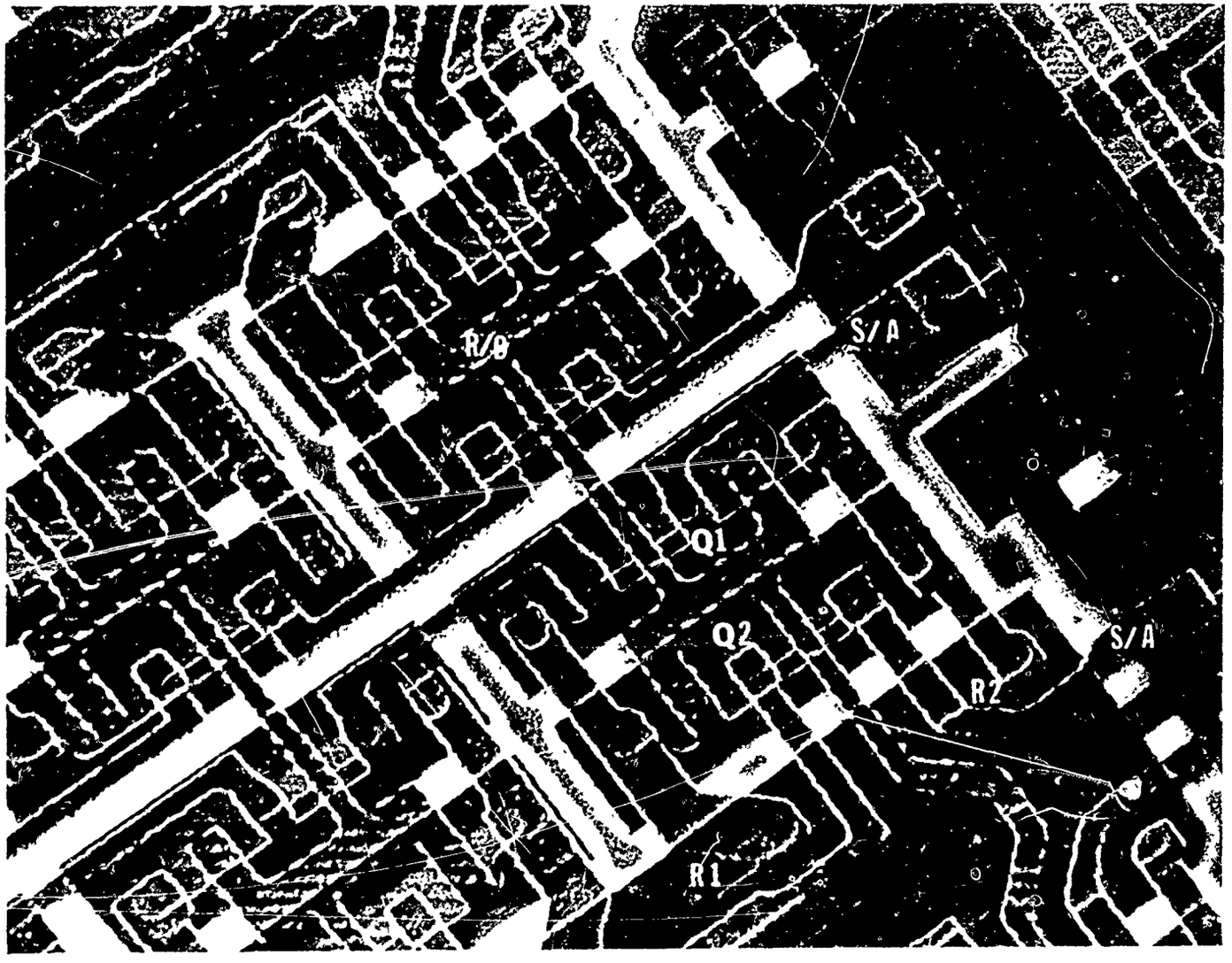


Photo 4-10 Voltage Contrast Micrograph of Memory Cells. 5 KV, Mag. - 930X

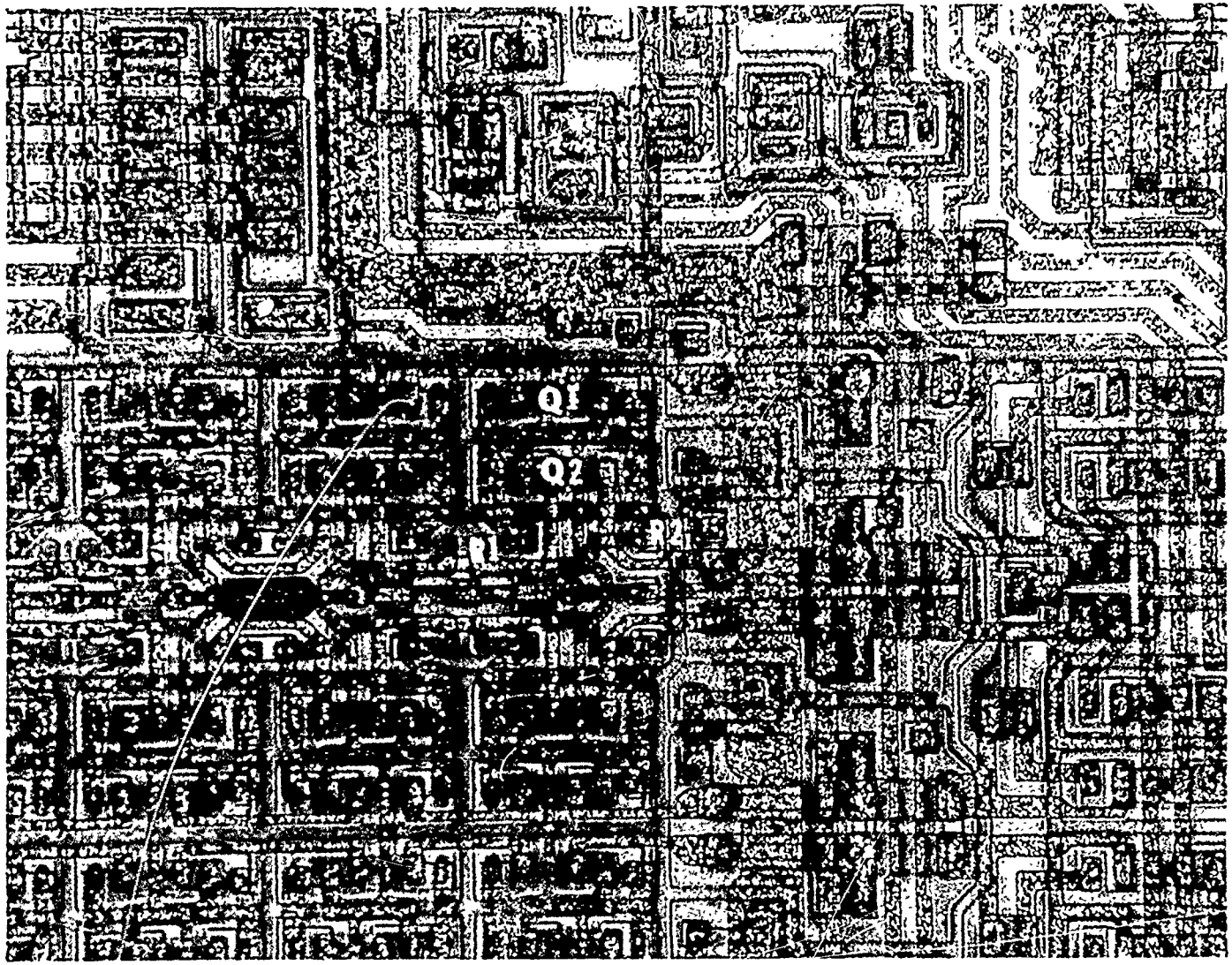


Photo 4-11 Light Photograph of Memory Cells. Mag. - 310X

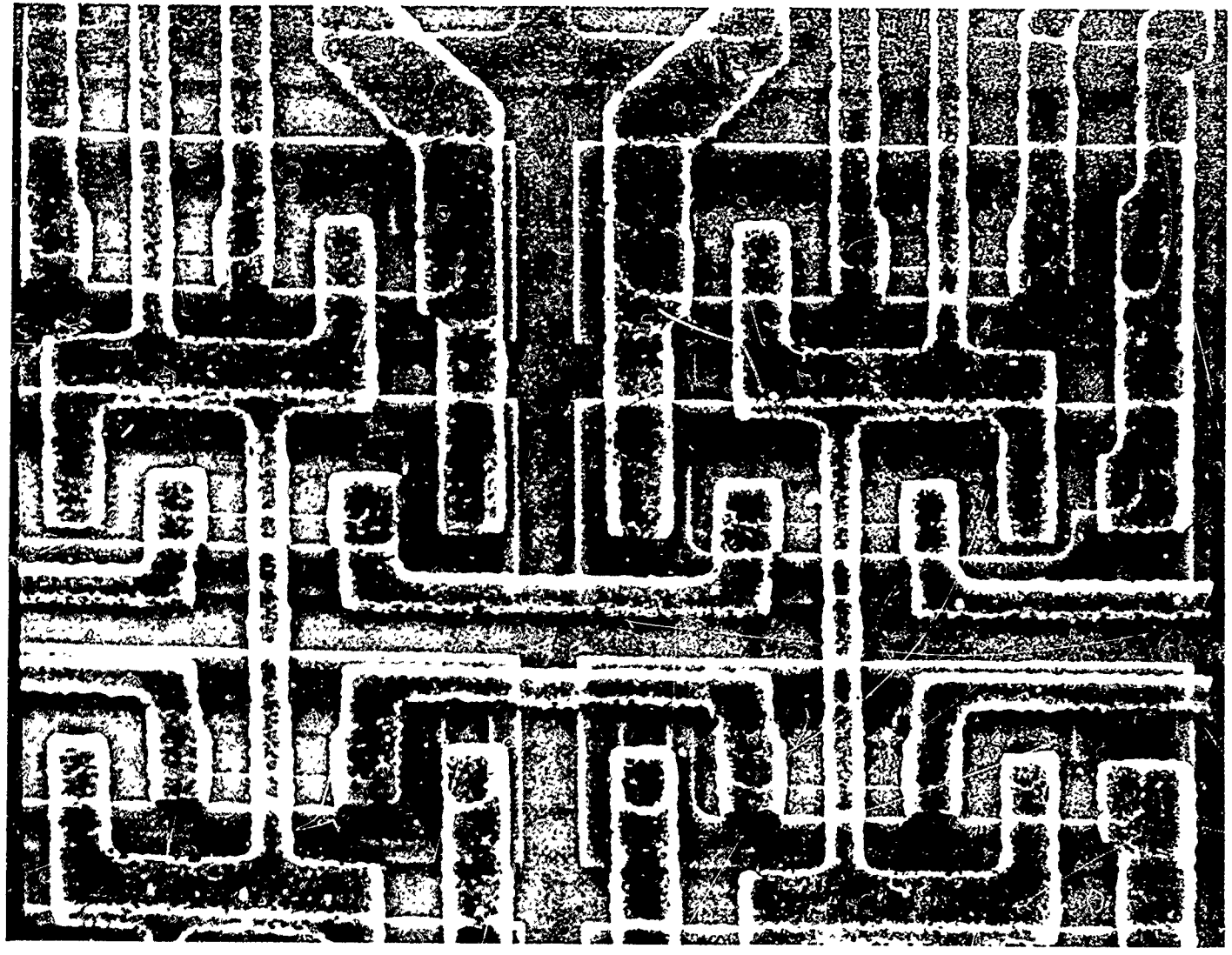


Photo 4-12 SEI Micrograph of Memory Cells. 20 KV, Mag. - 1270X

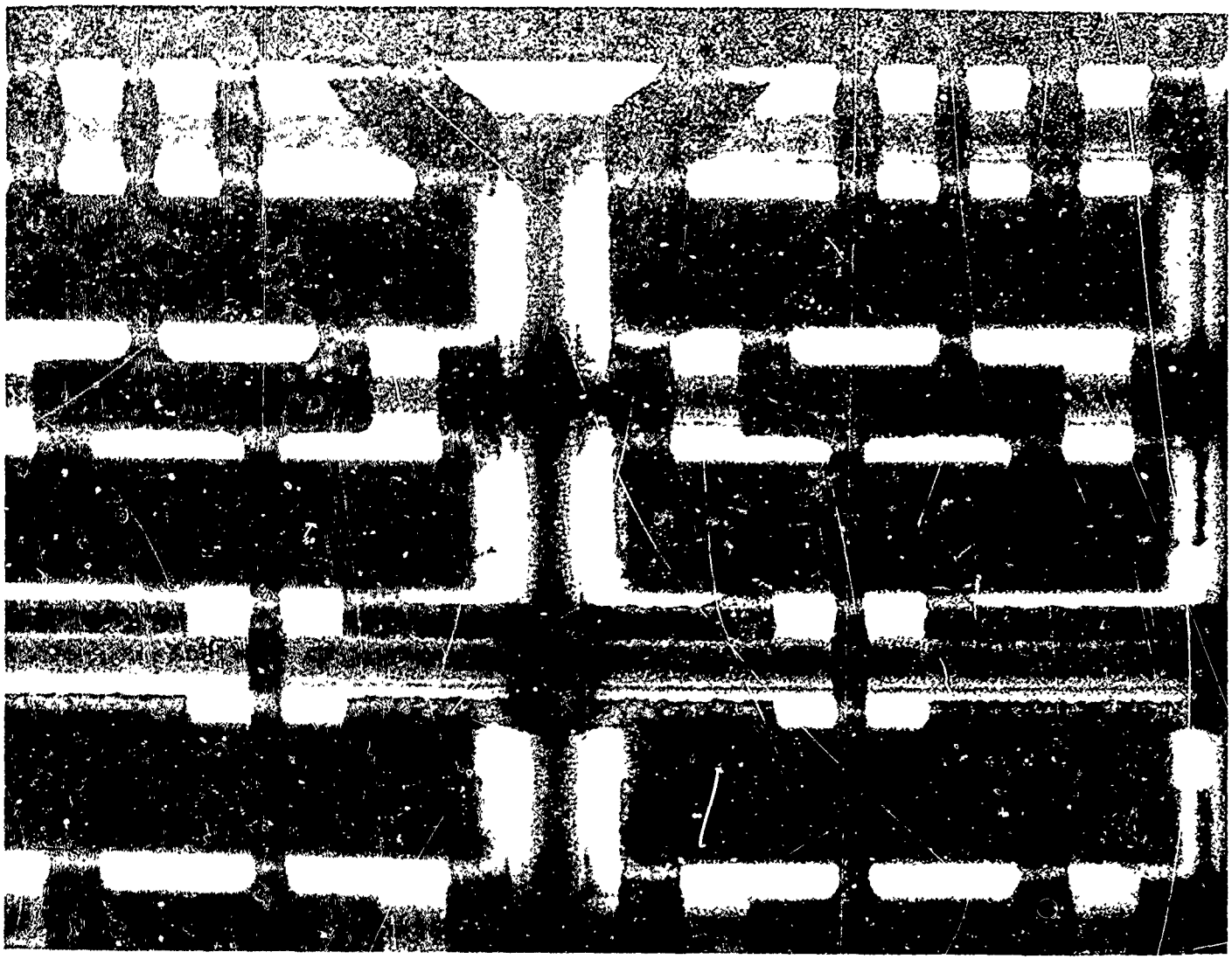


Photo 4-13 EBIC Micrograph of Memory Cells. Pin 16 to SCA, Pin 8 to GND
20 KV, Mag. - 1270X

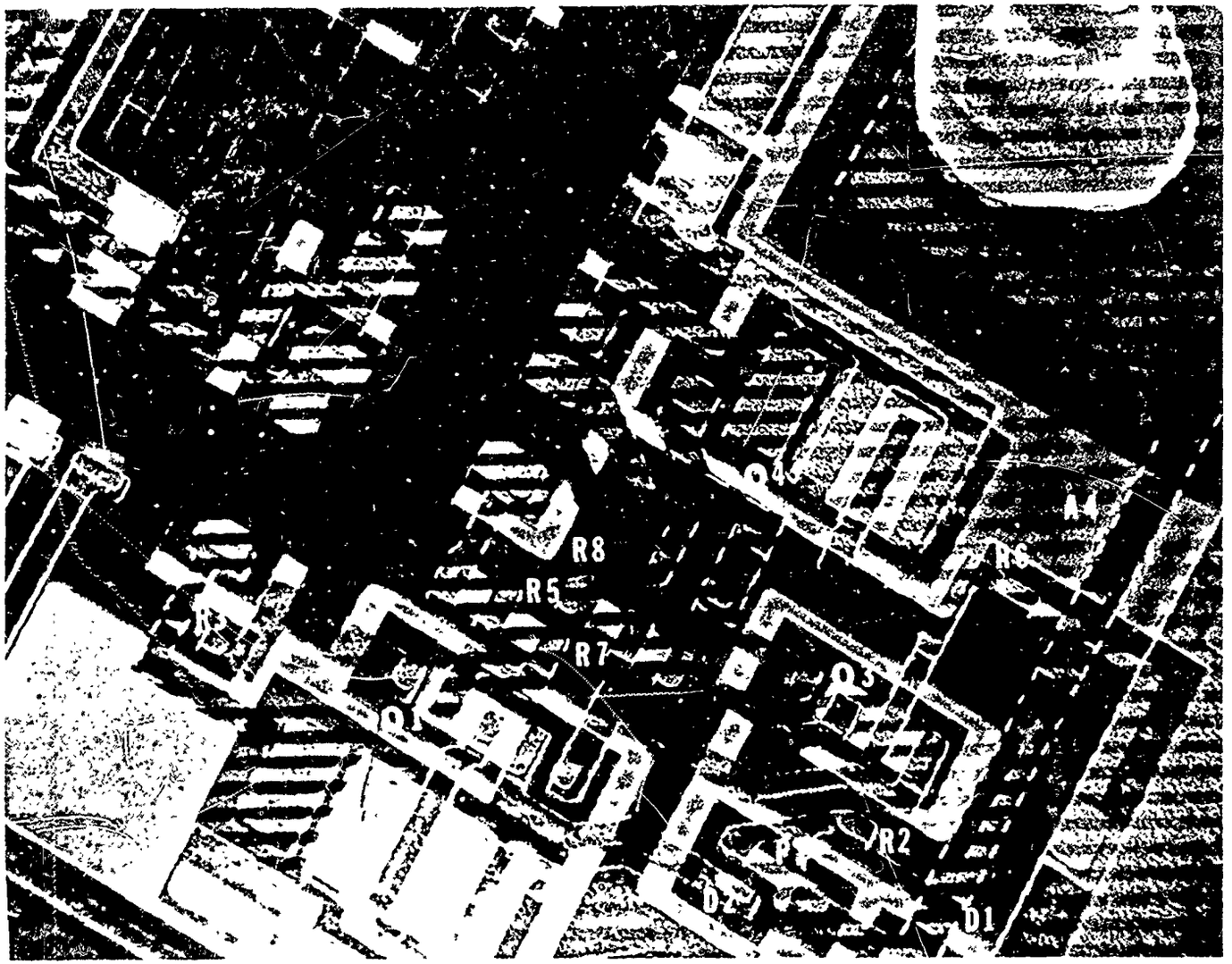


Photo 4-14 Voltage Contrast Micrograph of A4 Column Address Inverter. 5 KV, Mag. - 540X

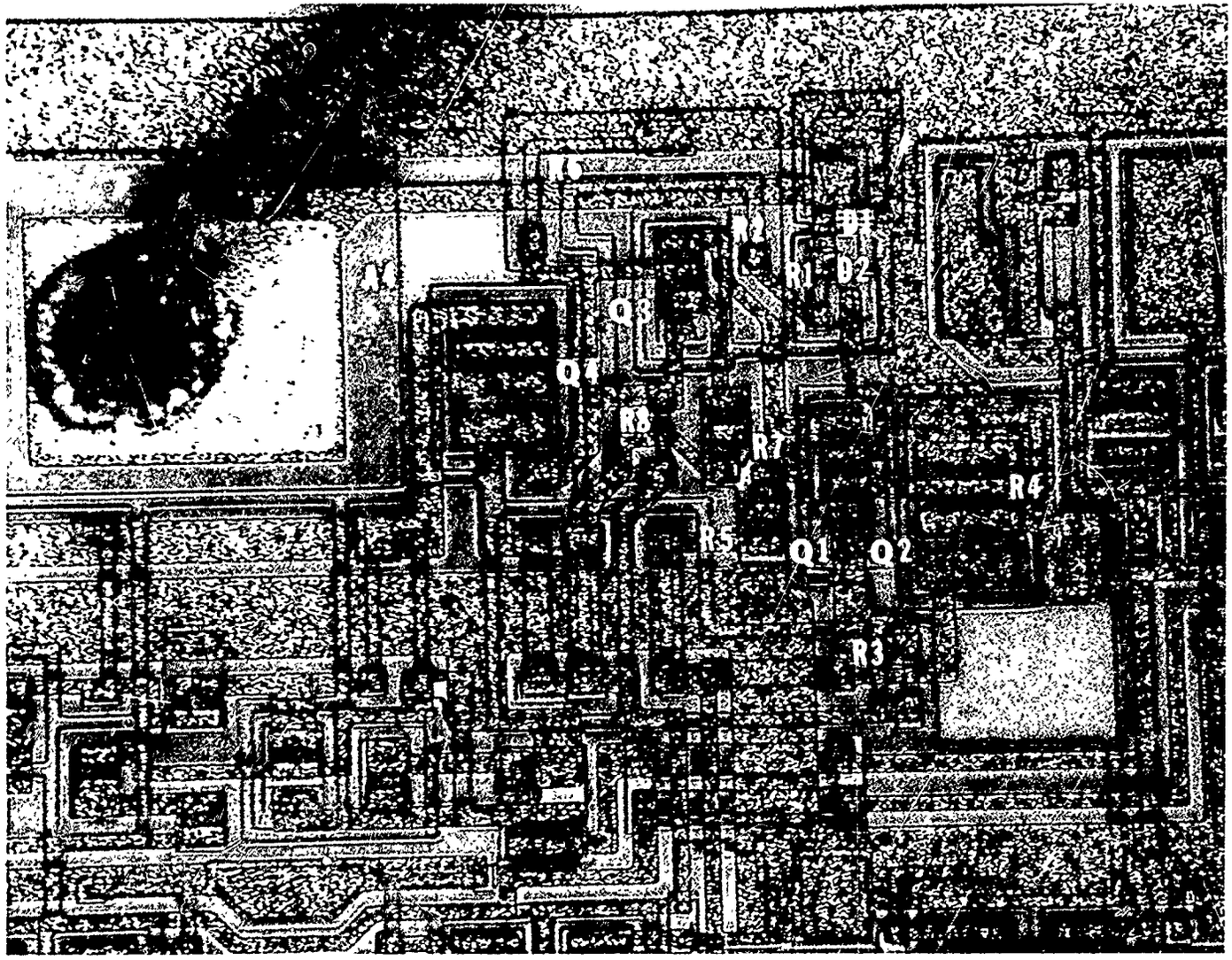


Photo 4-15 Light Photograph of A4 Column Address Inverter. Mag. - 310X

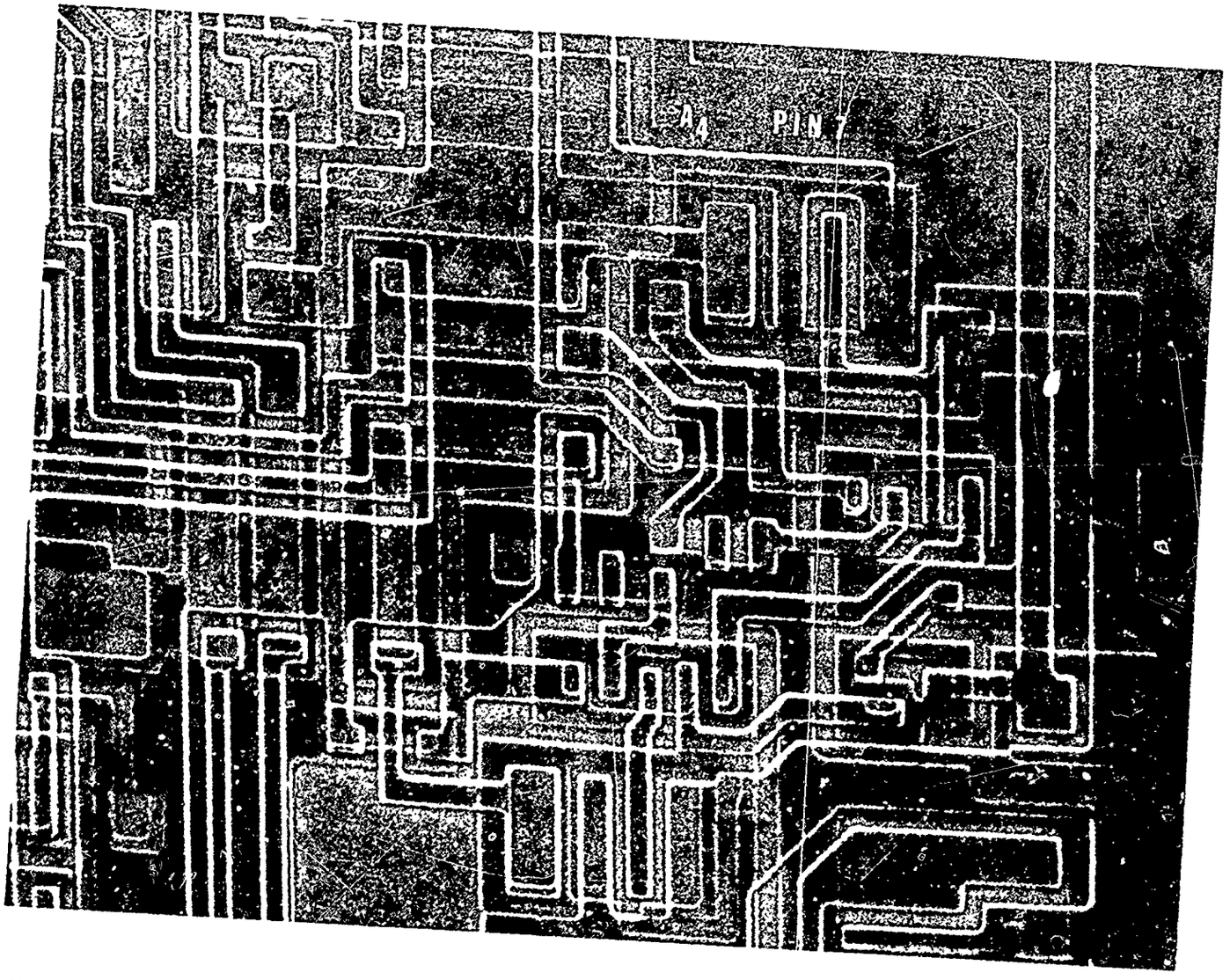


Photo 4-16 SEI Micrograph of A4 Column Address Inverter. 20 Kv, Mag. - 495X

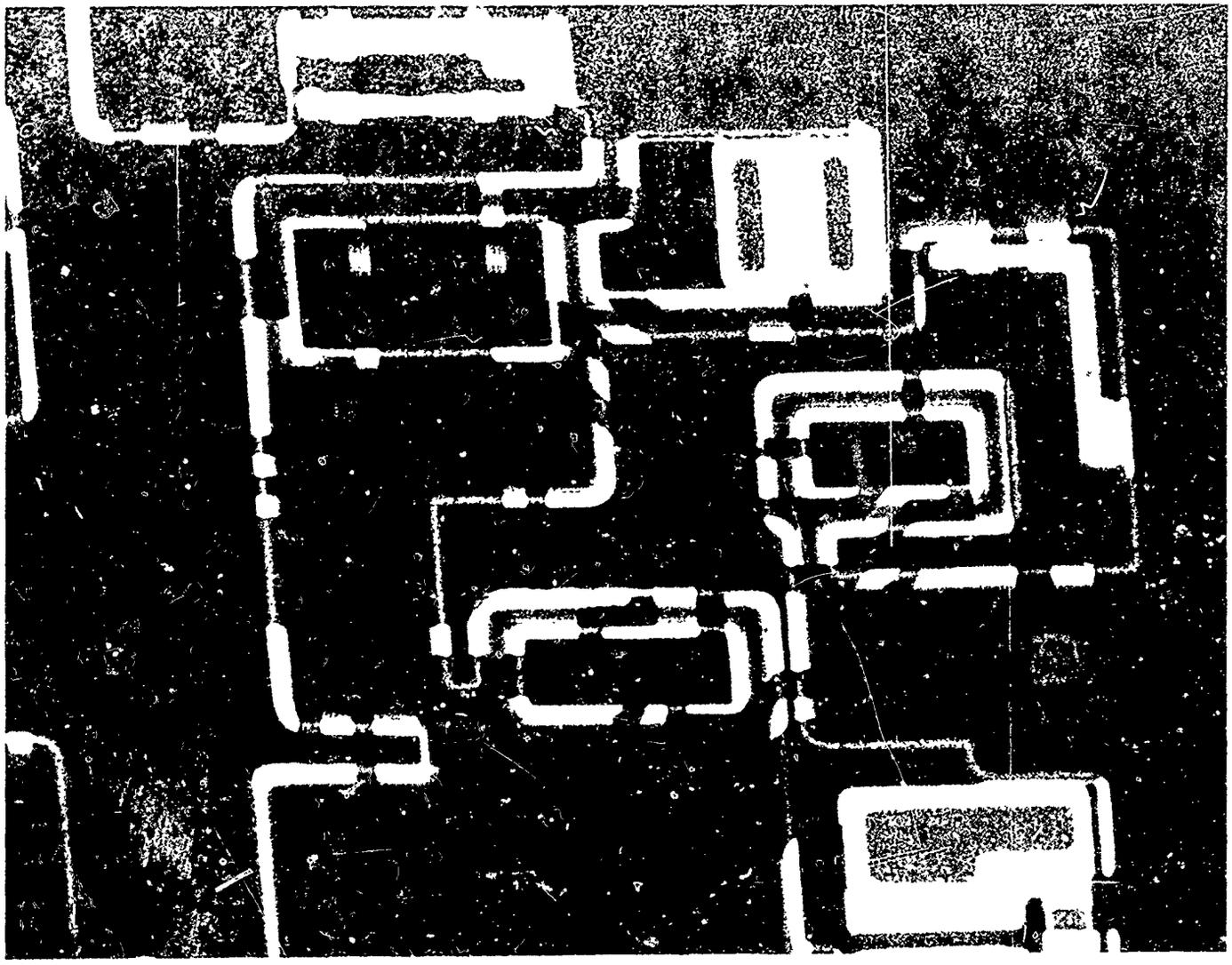


Photo 4-17 EBIC Micrograph of A4 Column Address Inverter. Pin 7 and 16 to SCA, Pin 8 to GND. Mag. - 495X

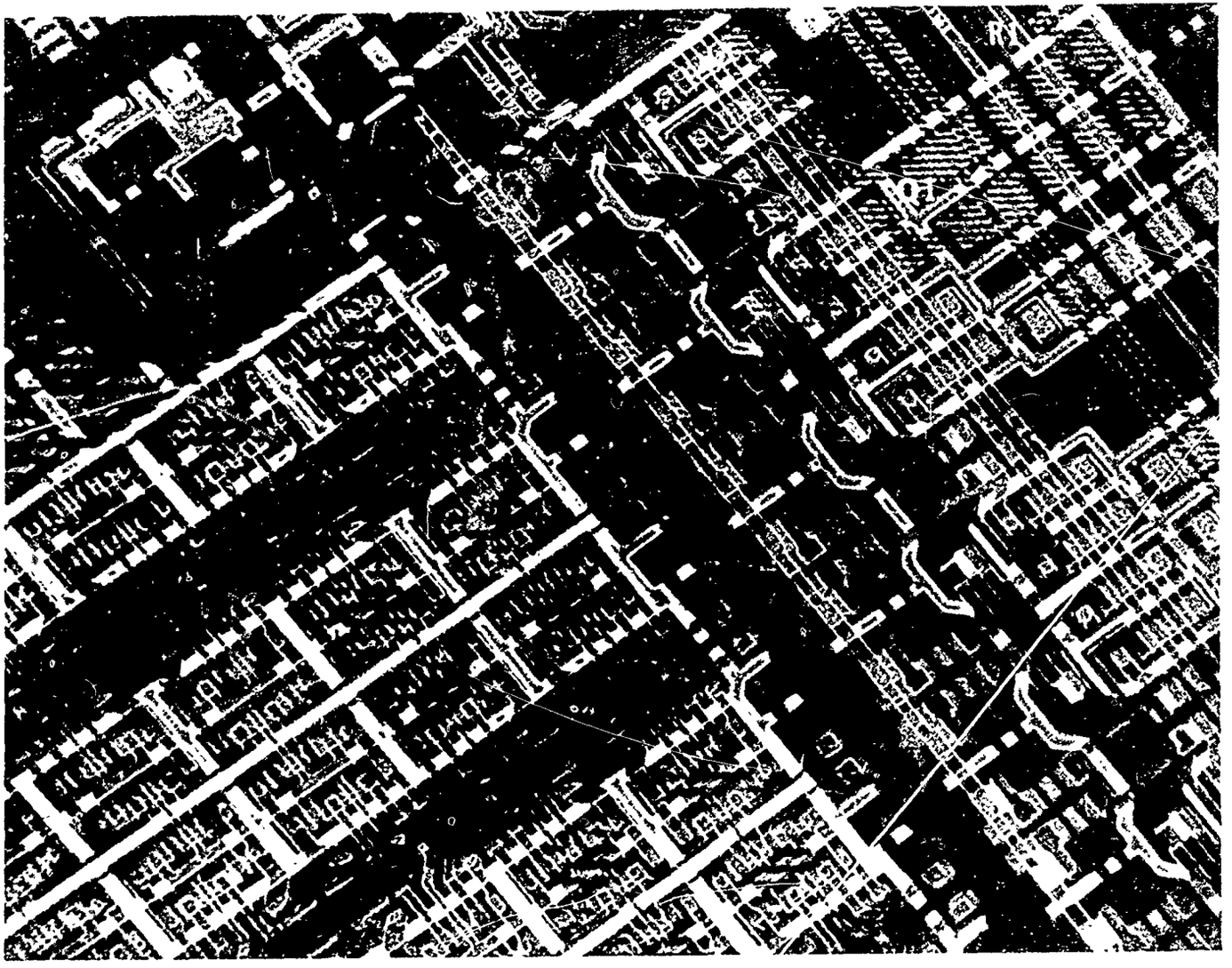


Photo 4-18 Voltage Contrast Micrograph of Column Decode Circuit. 5 KV, Mag. - 310X

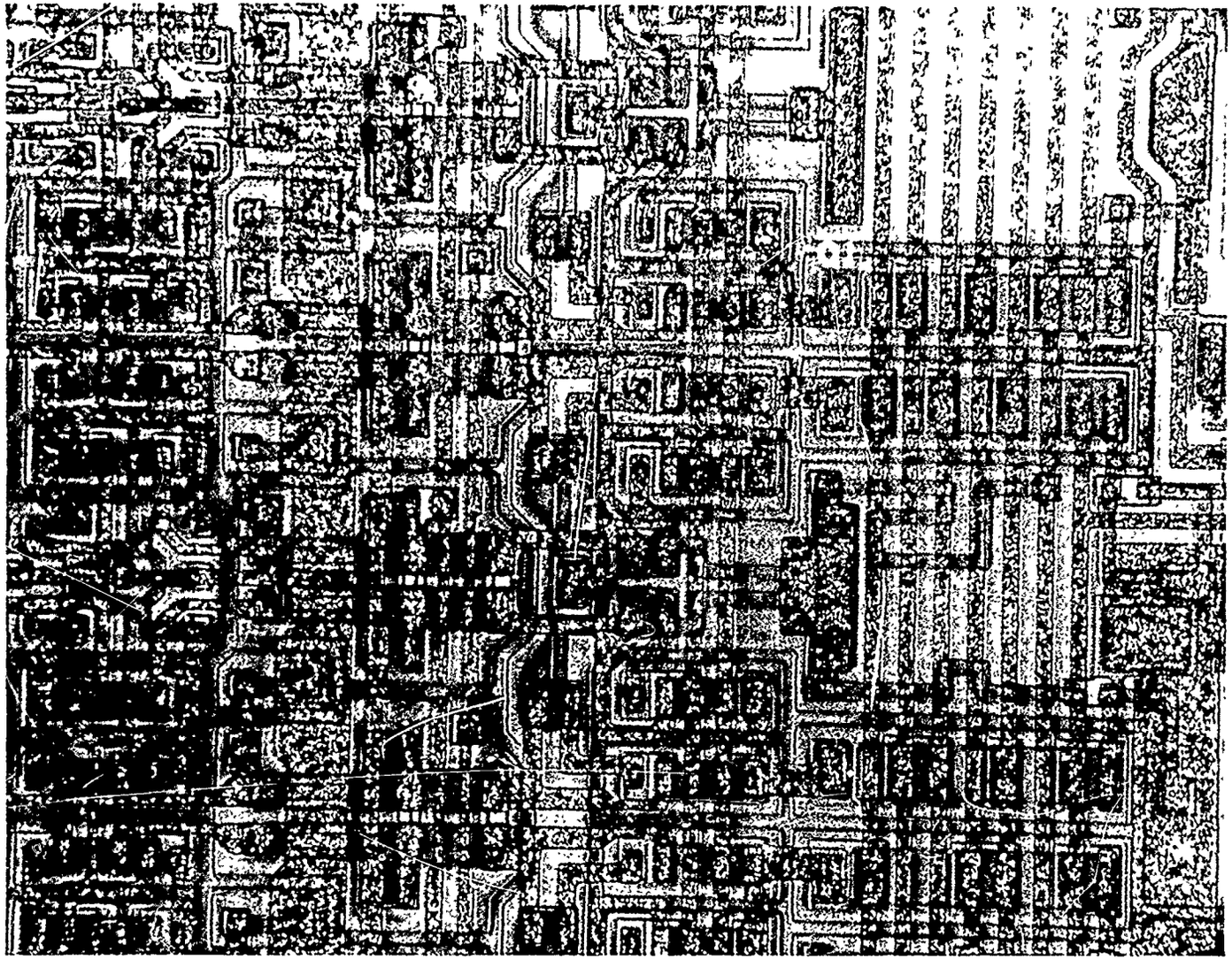


Photo 4-19 Light Photograph of Column Decode Circuit. Mag. - 310X

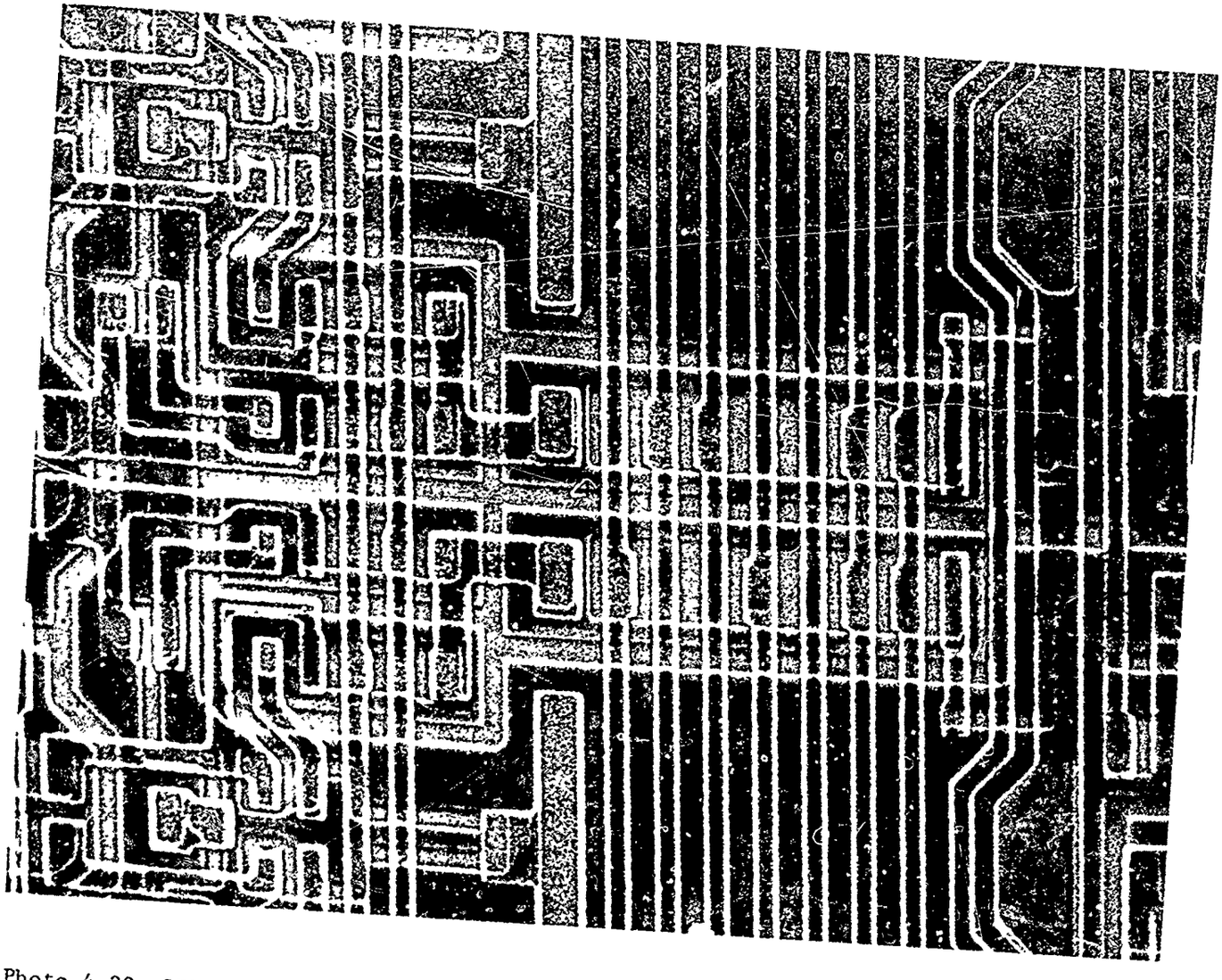


Photo 4-20 SEI Micrograph of Column Decode Circuit. 20 KV, Mag. - 525X

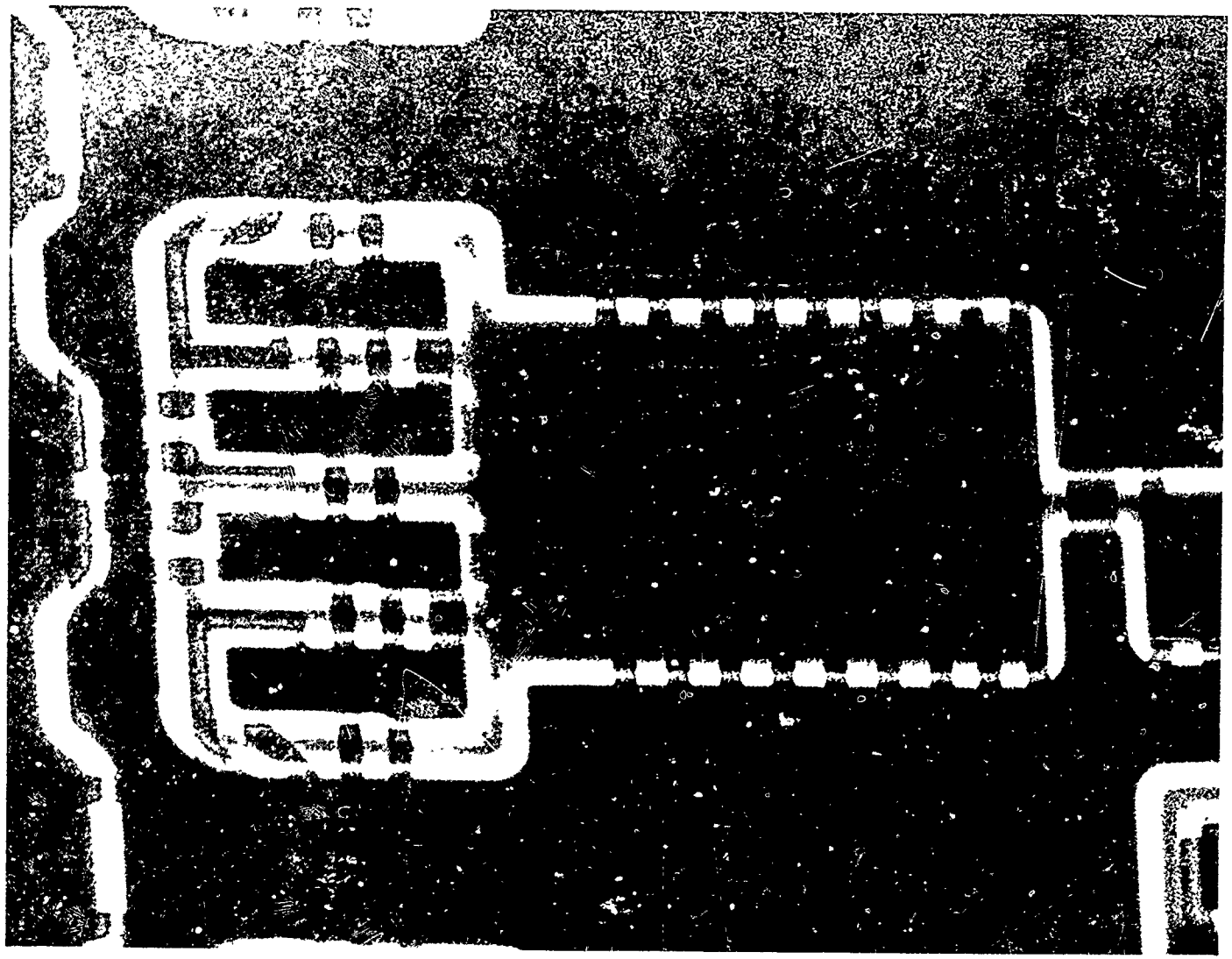


Photo 4-21 EBIC Micrograph of Column Decode Circuit. Pin 16 to SCA, Pin 8 to GND. Mag. - 525X

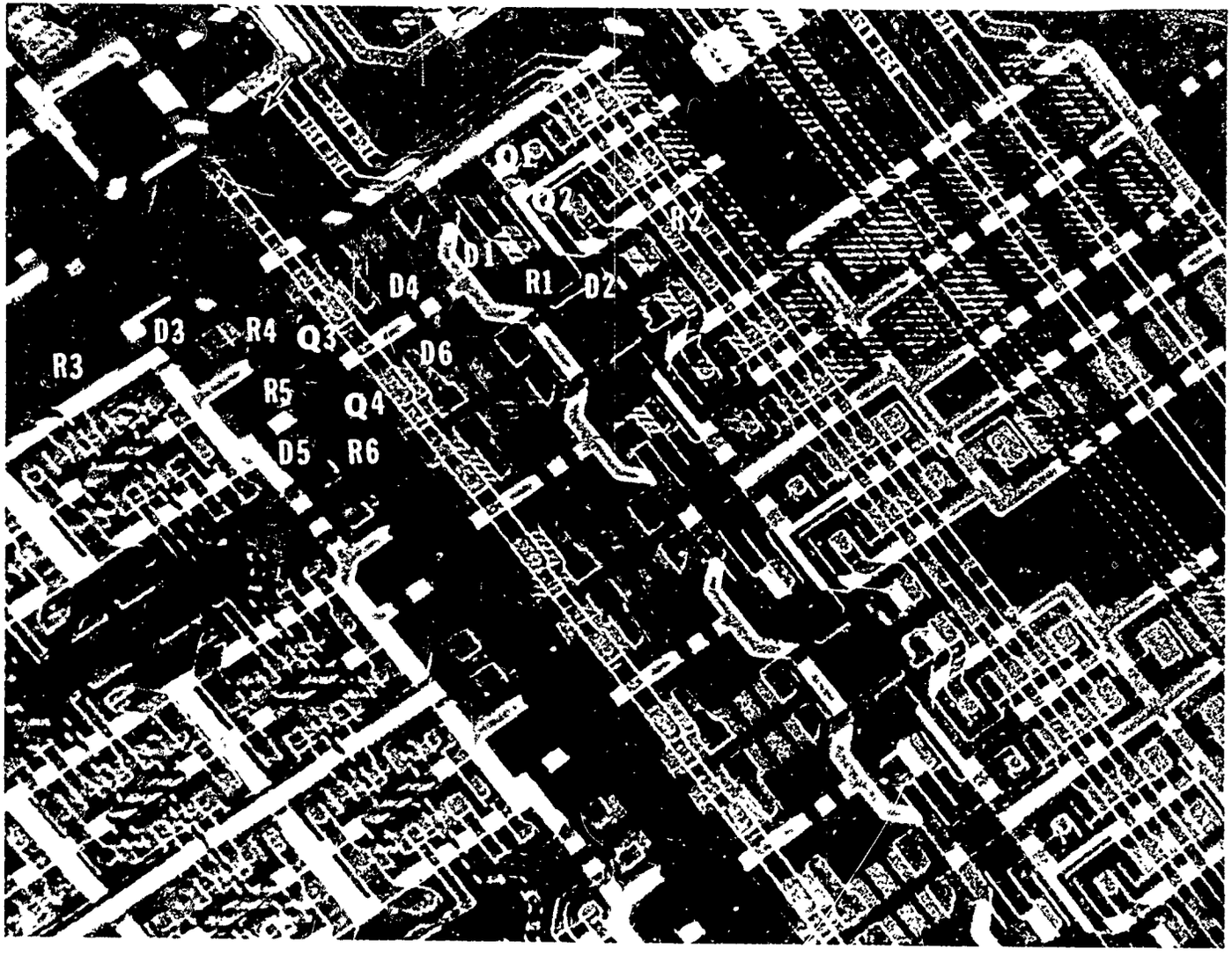


Photo 4-22 Voltage Contrast Micrograph of Sense Amplifier. Arrow Locates a Mask Modification for Two Metal Stripes. 5 KV, Mag. - 300X

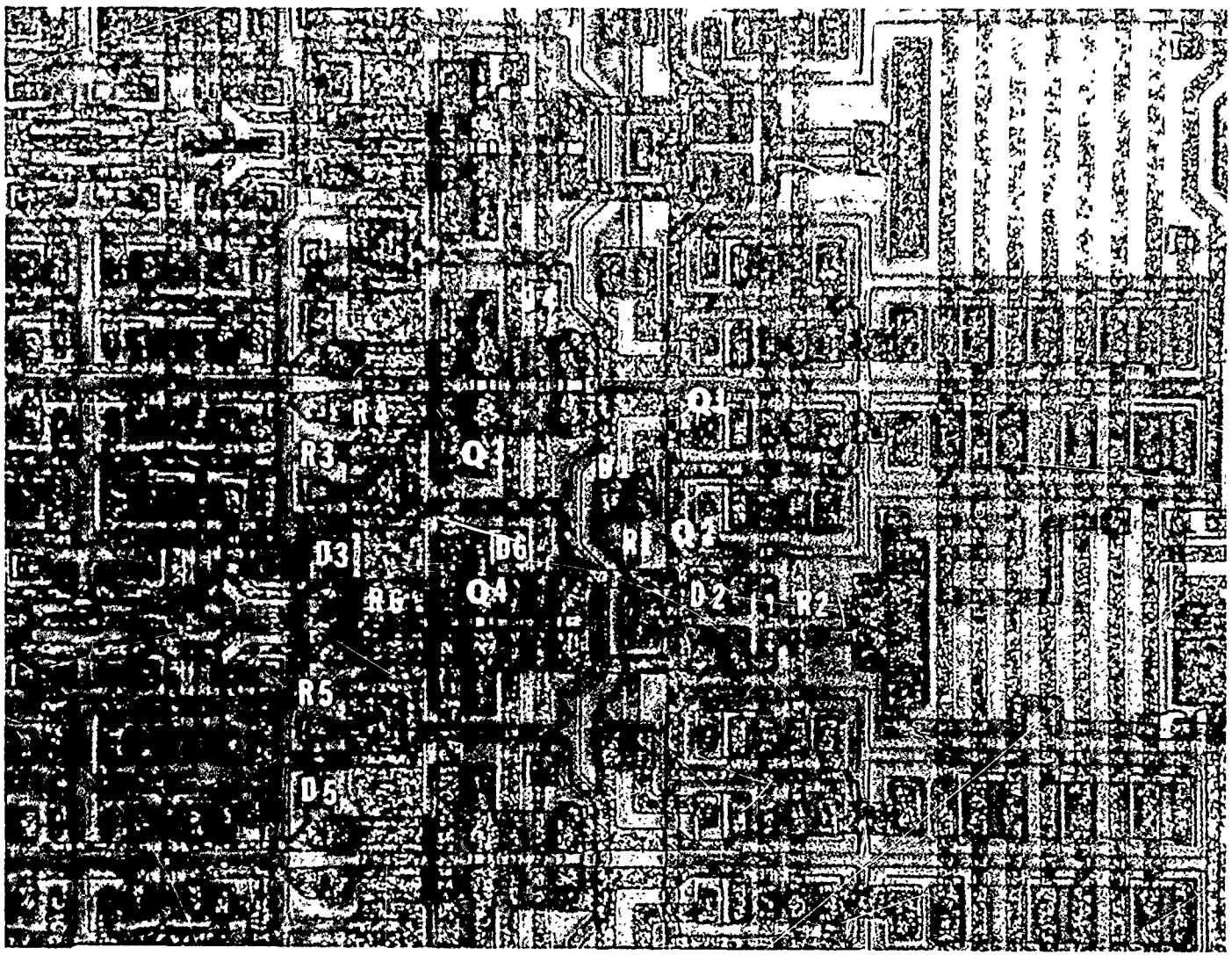
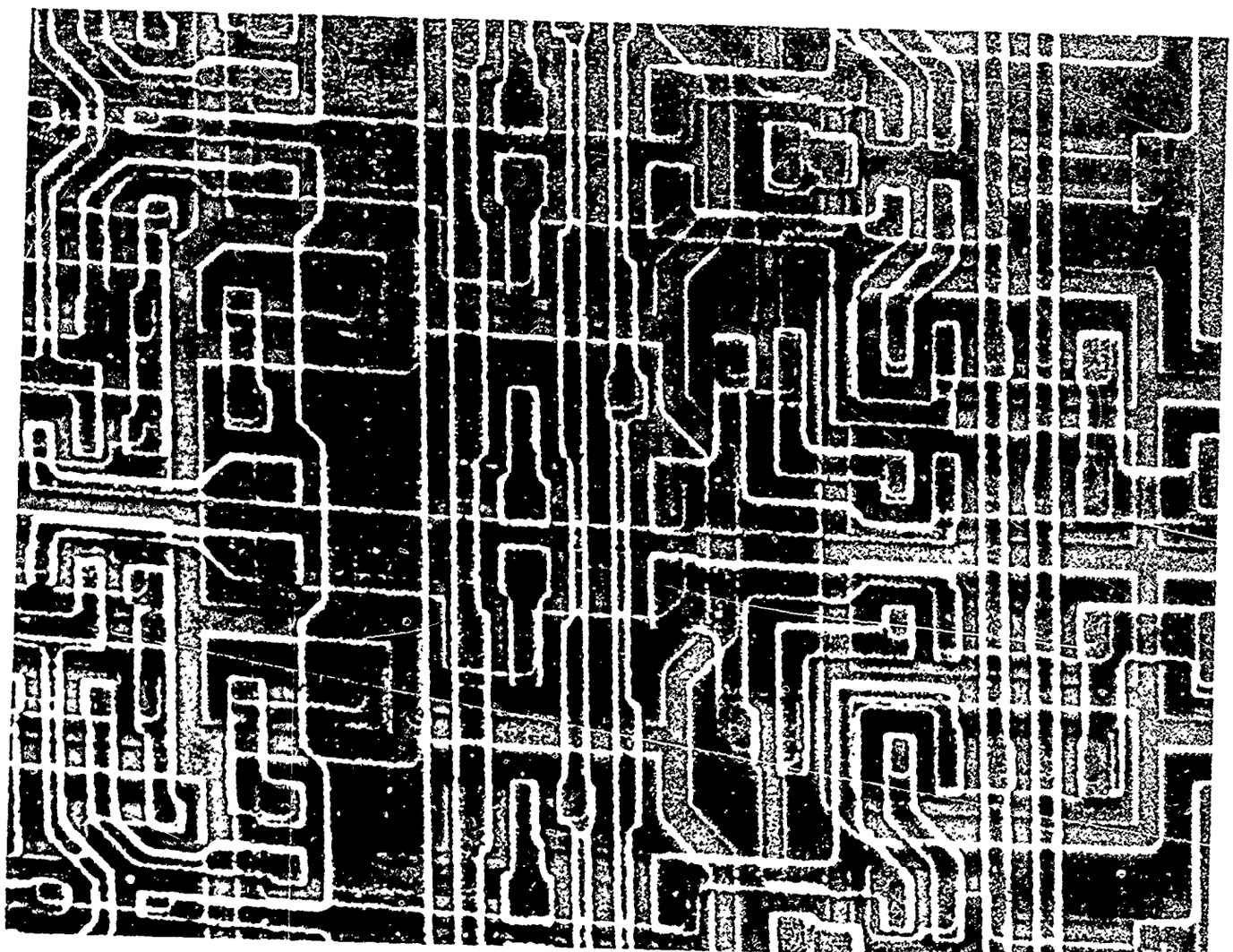


Photo 4-23 Light Photograph of Sense Amplifier. Mag. - 310X



Phot 4-24 SEI Micrograph of Sense Amplifier. 20 KV, Mag. - 635X

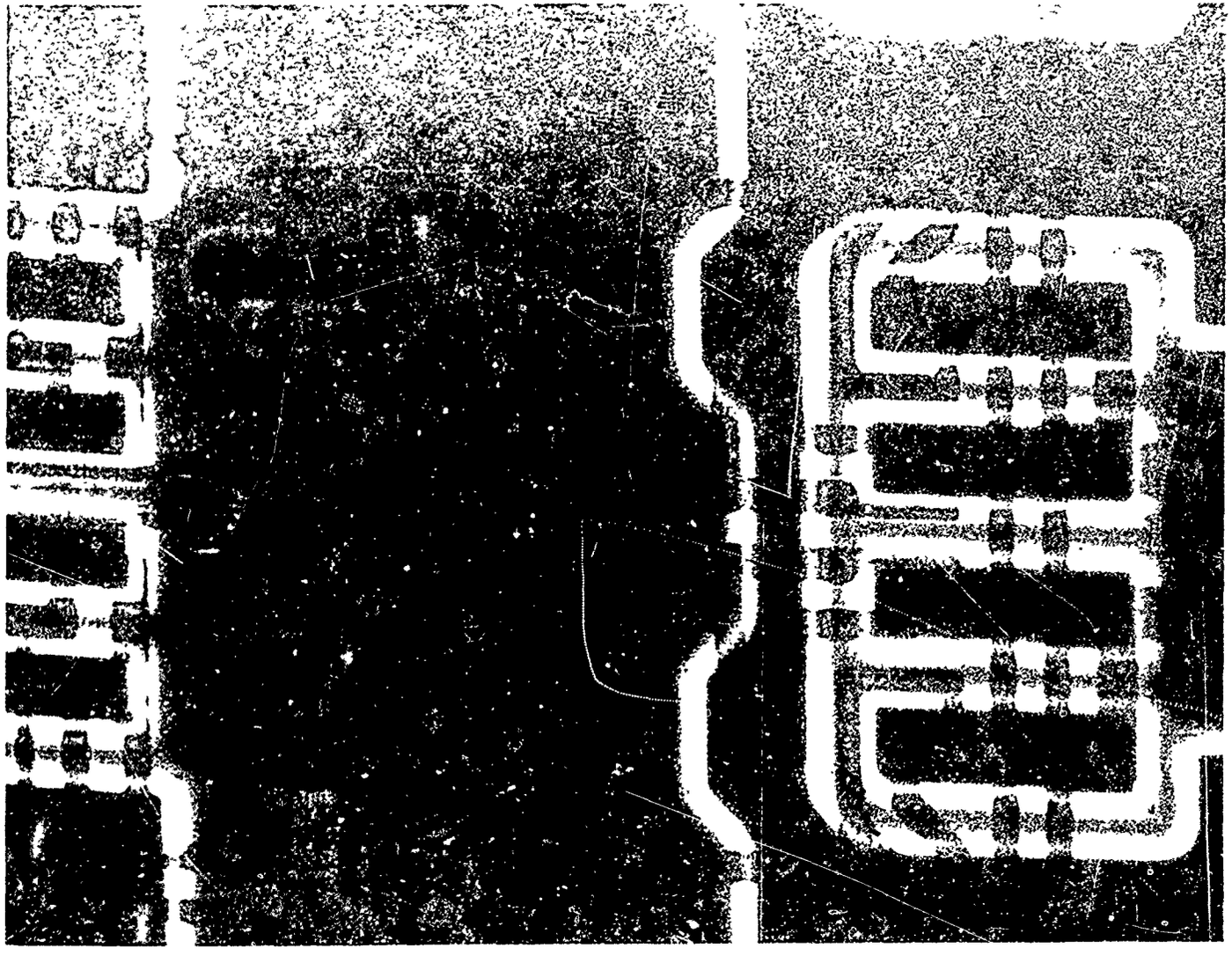


Photo 4-23. EBIC Micrograph of Sense Amplifier. Pin 16 to SCA, Pin 8 to GND, 20 KV, Mag. - 635X

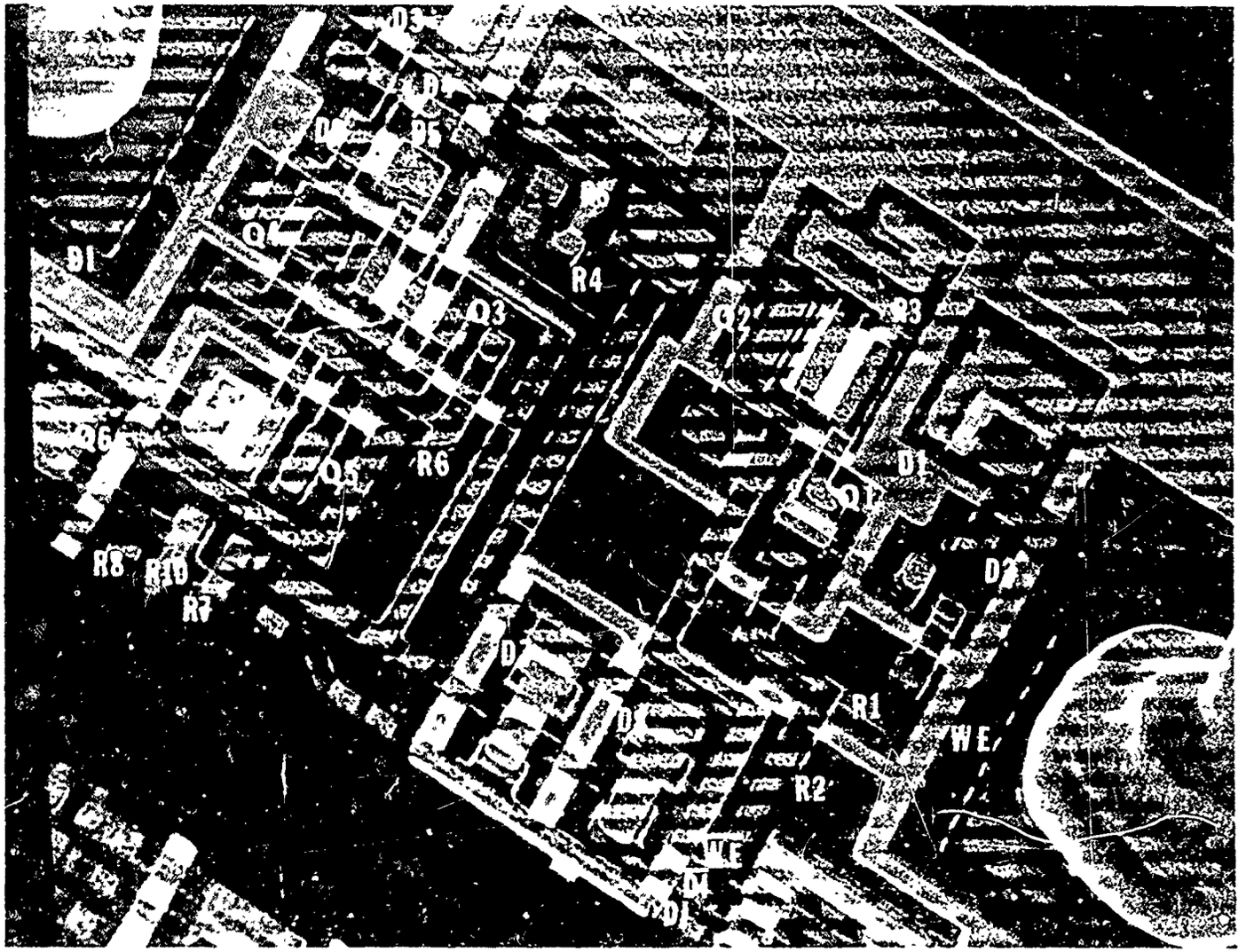


Photo 4-26 Voltage Contrast Micrograph of Data In and Write Enable Circuit. 5 Kv, Mag. - 635X

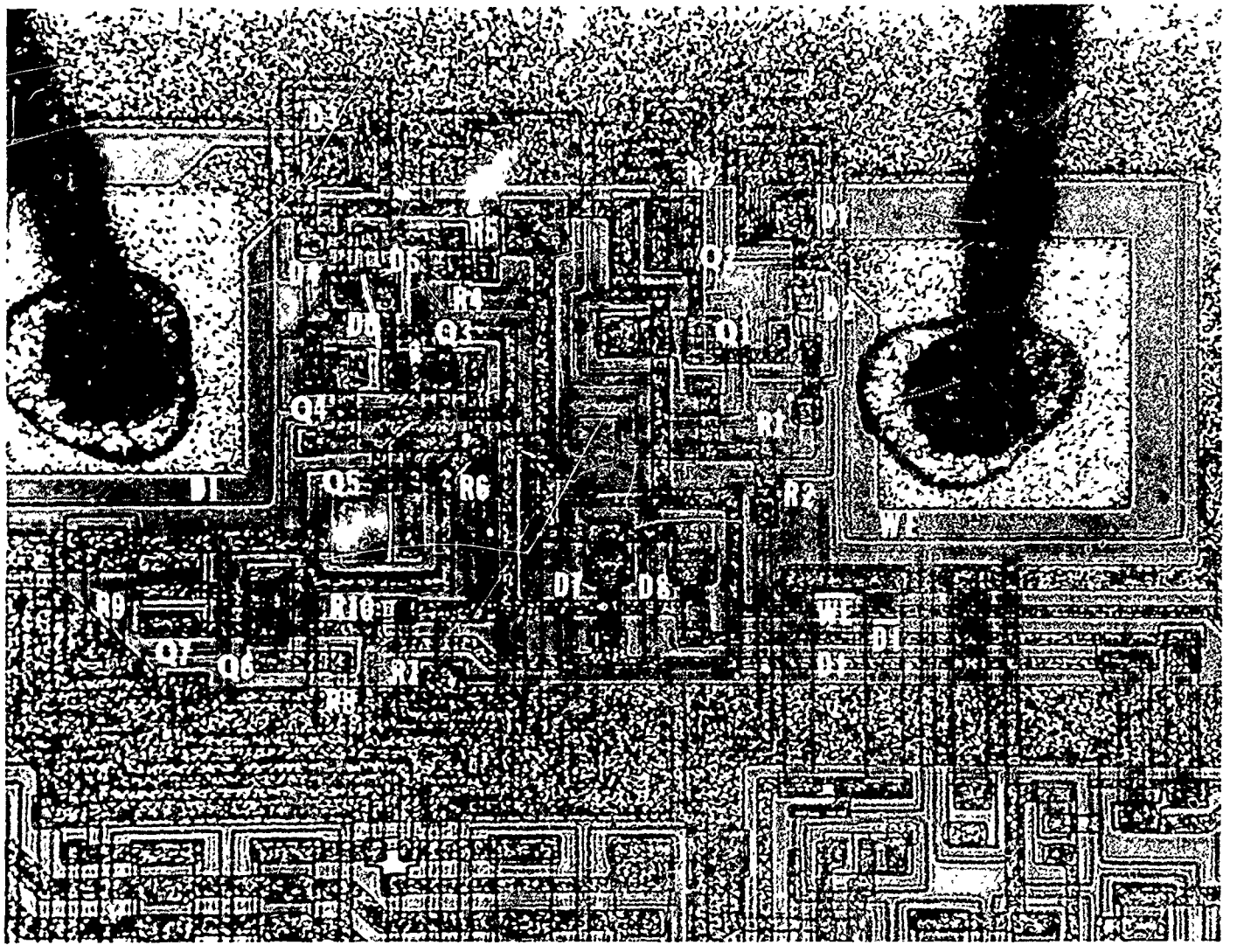


Photo 4-27 Light Photograph of Data Input and Write Enable Circuit, Mag. - 310X

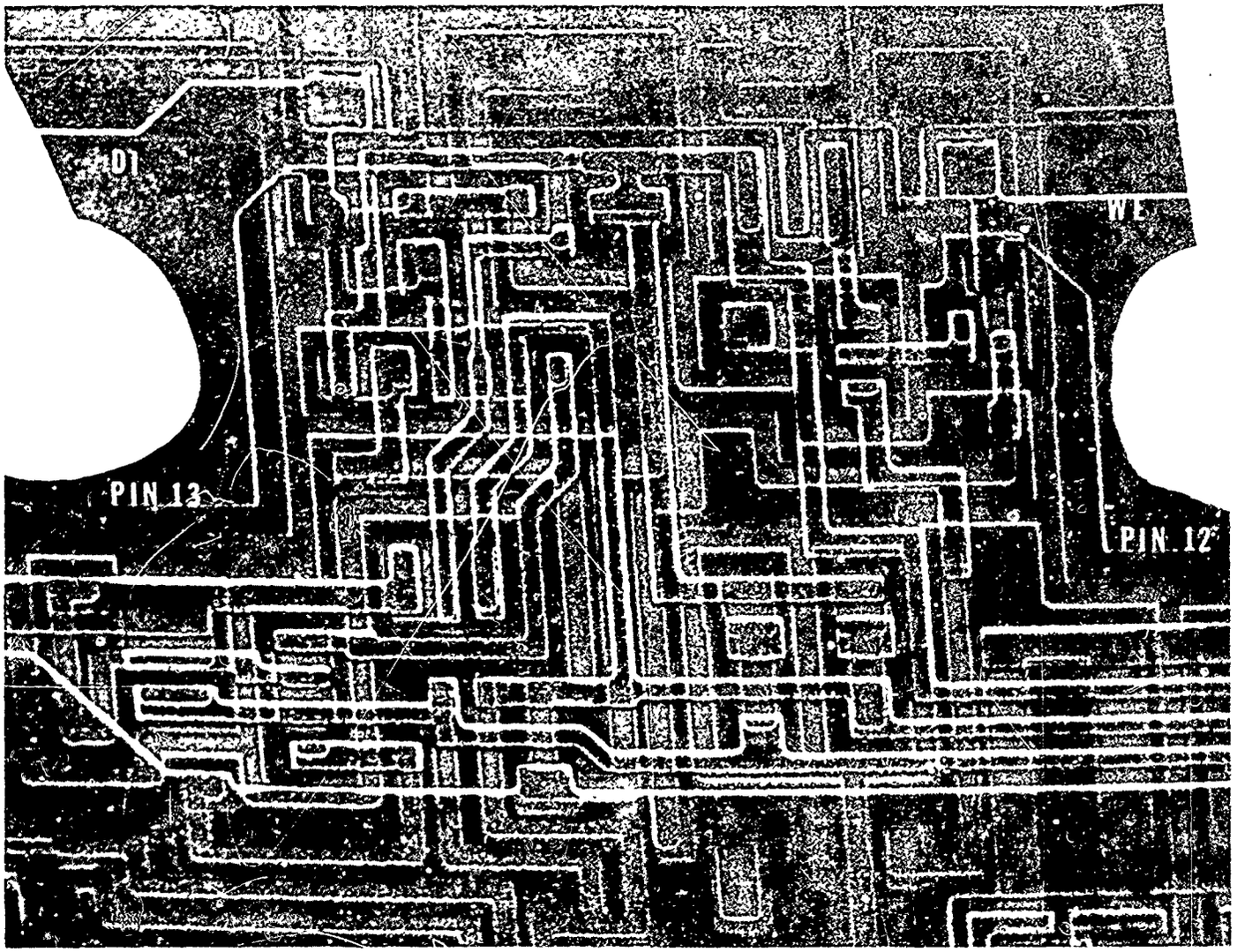


Photo 4-28 SEI Micrograph of Data Input and Write Enable Circuit. 20 KV, Mag. - 480X

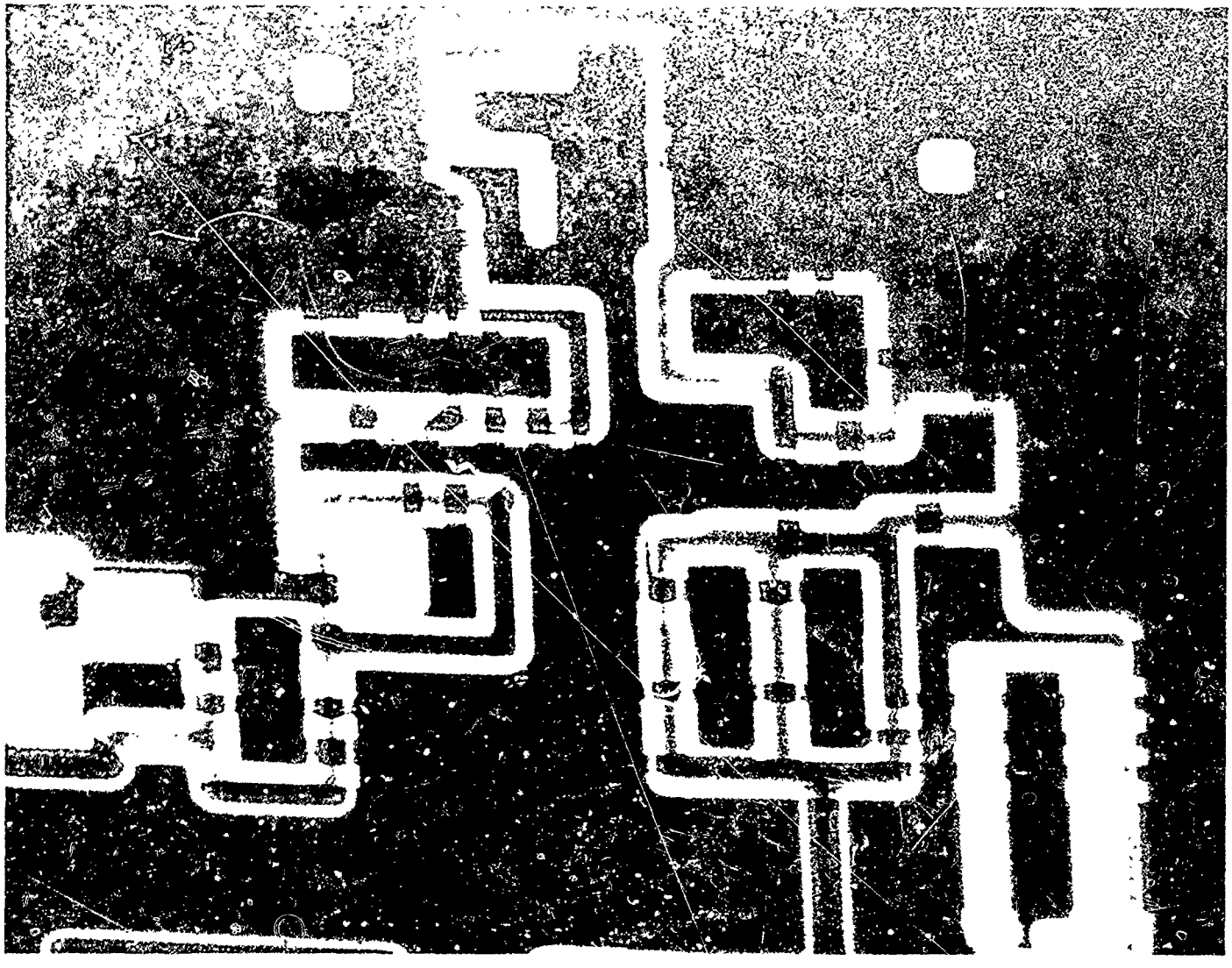


Photo 4-29 EBIC Micrograph of Data Input and Write Enable Circuit. Pins 12, 13 and 16 to SCA, Pin 8 to GND. Mag. - 480X

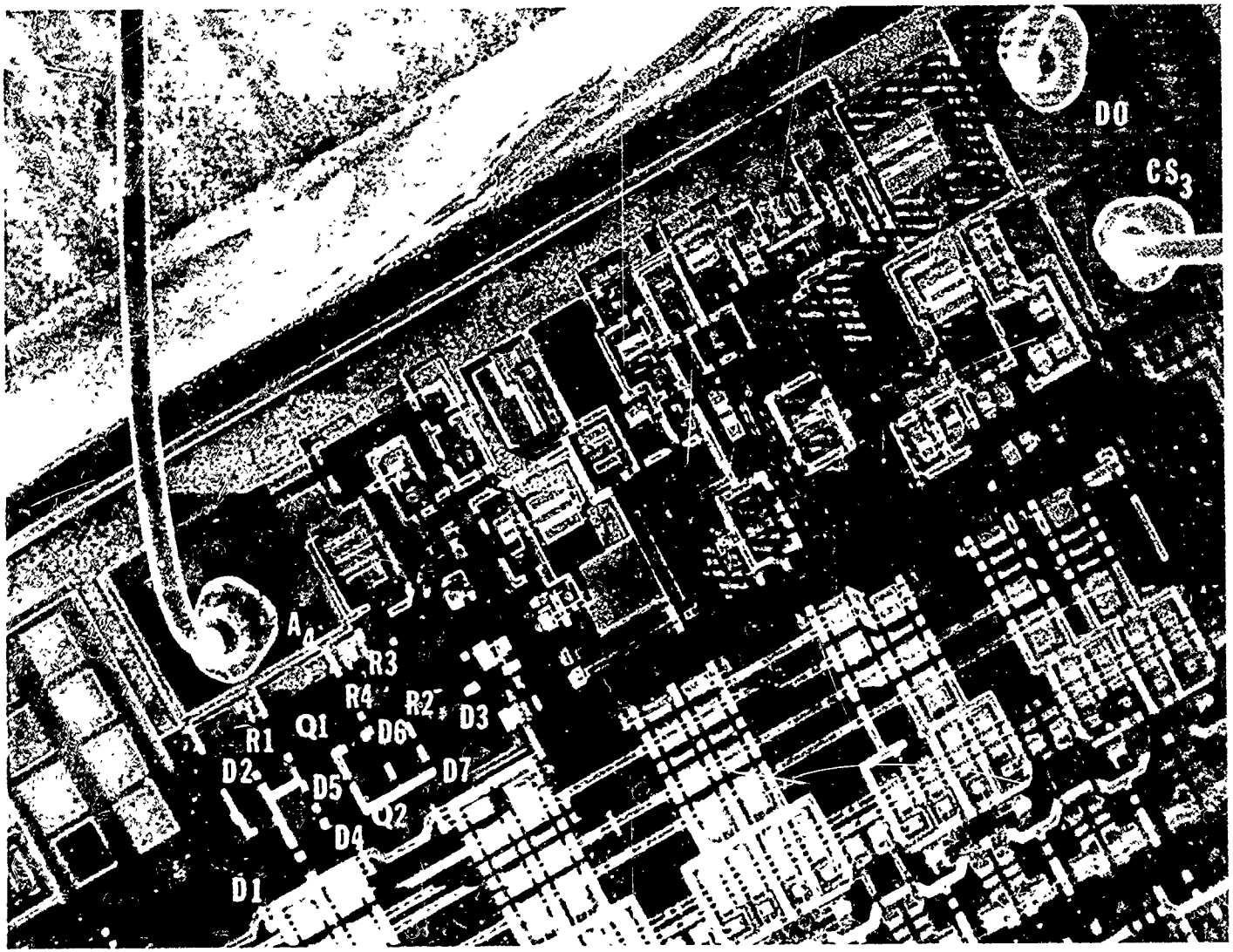


Photo 4-30 Voltage Contrast Micrograph of Sense Amplifier Disriminator. 5 KV, Mag. - 185X

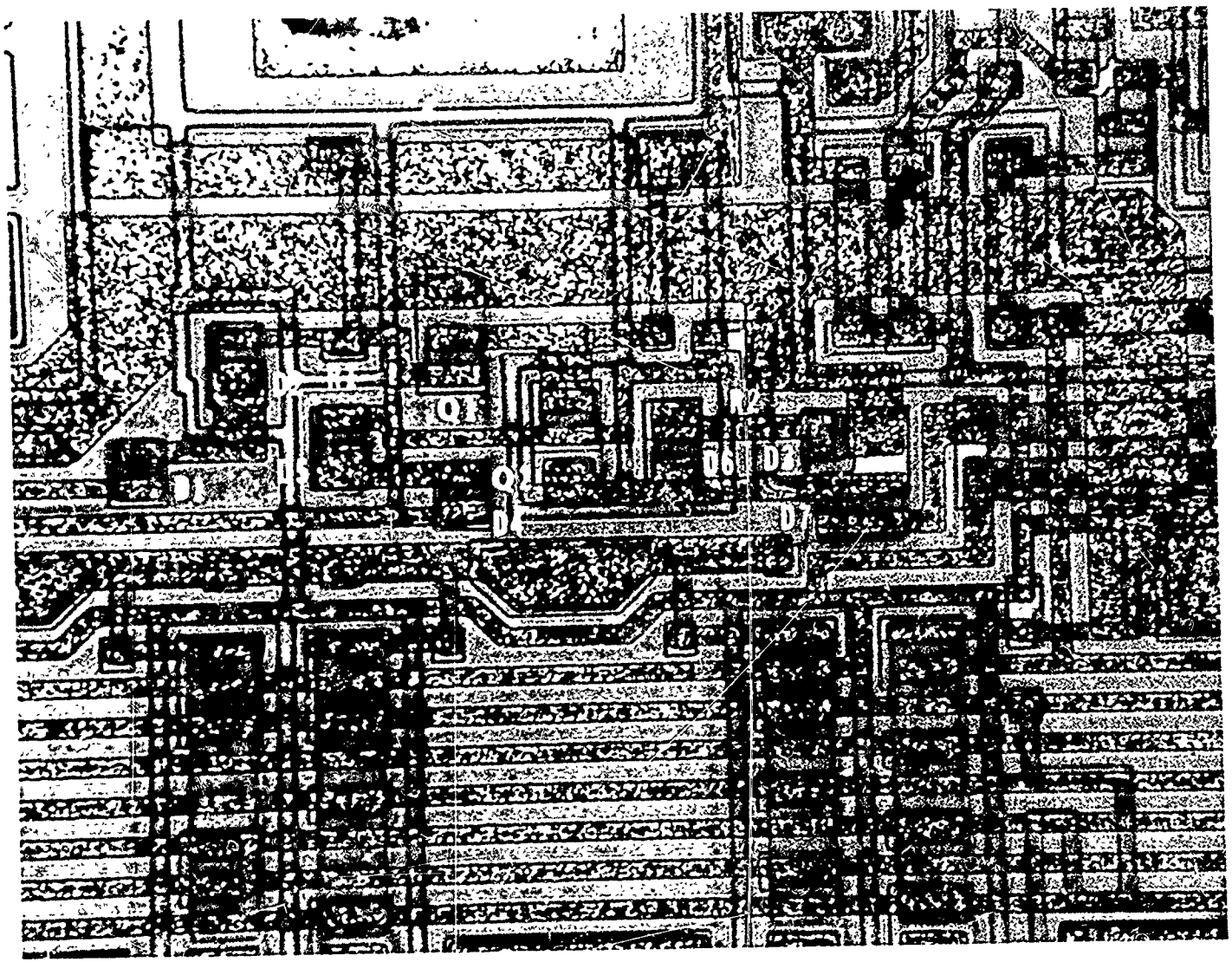


Photo 4-31 Light Photograph of Sense Amplifier Discriminator. Mag. - 365X

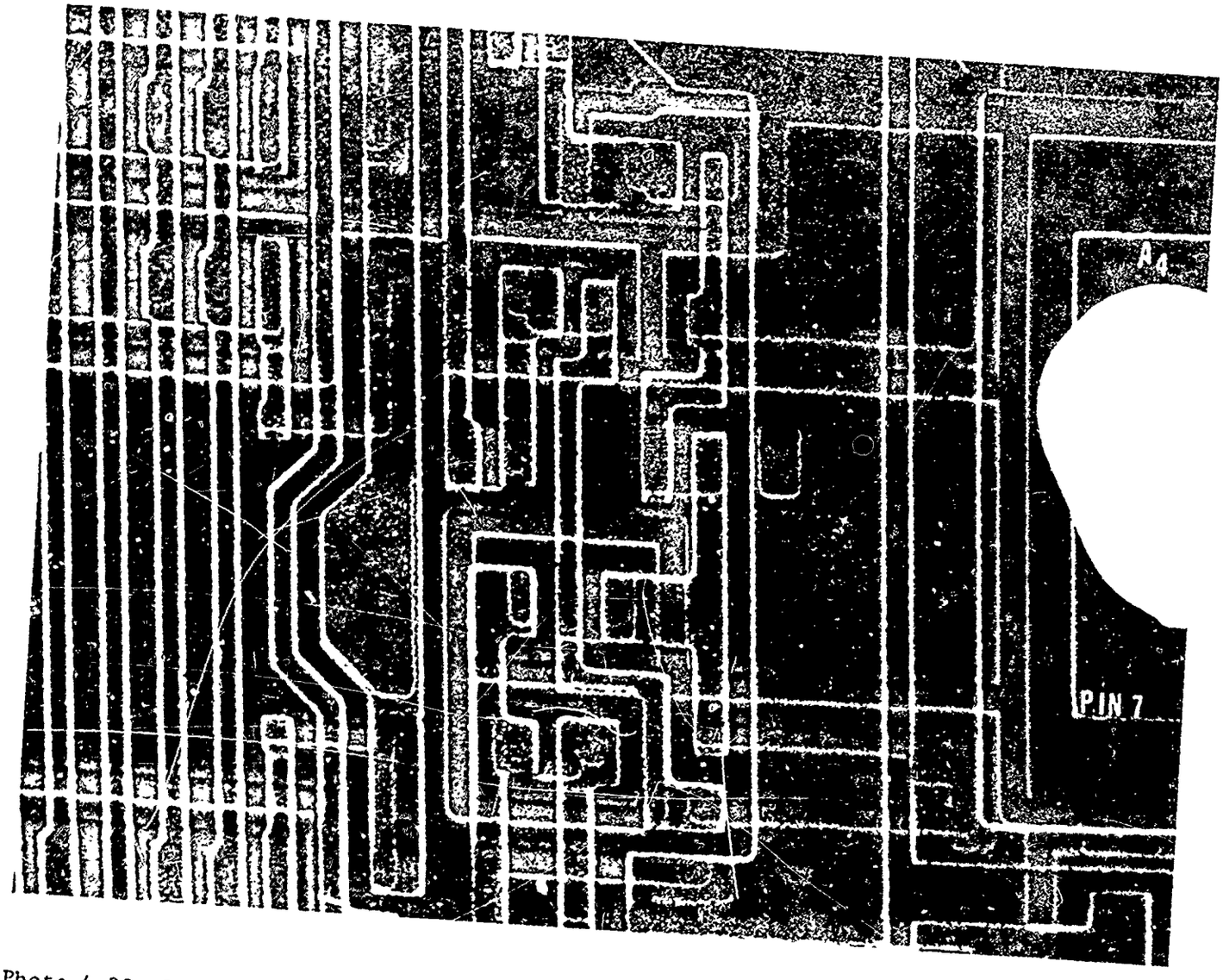


Photo 4-32 SEI Micrograph of Sense Amplifier Dicriminator. 20 KV, Mag. - 620X

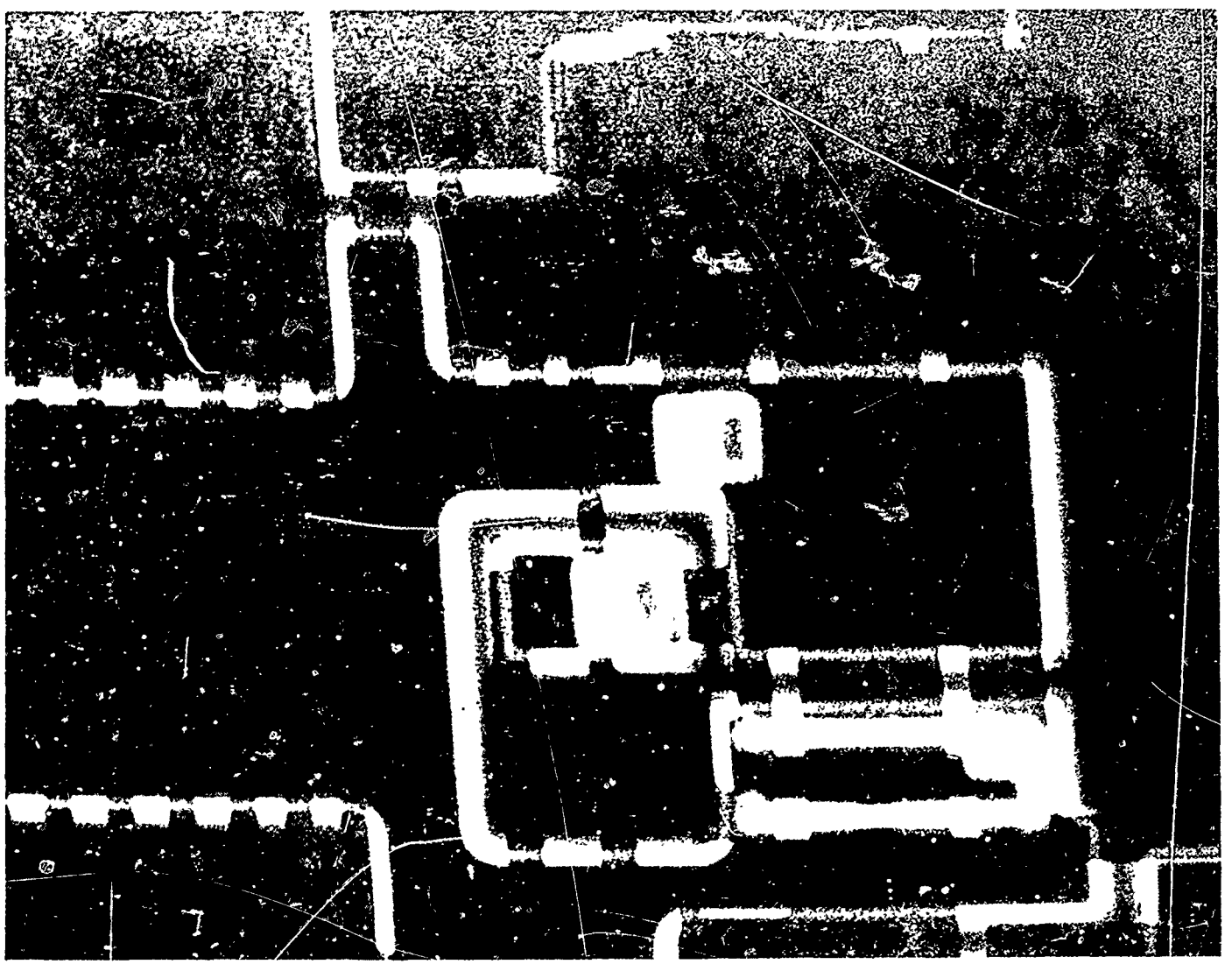


Photo 4-33 EBIC Micrograph of Sense Amplifier Discriminator. Pin 16 to SCA, Pin 8 to GND. 20 KV, Mag. - 620X

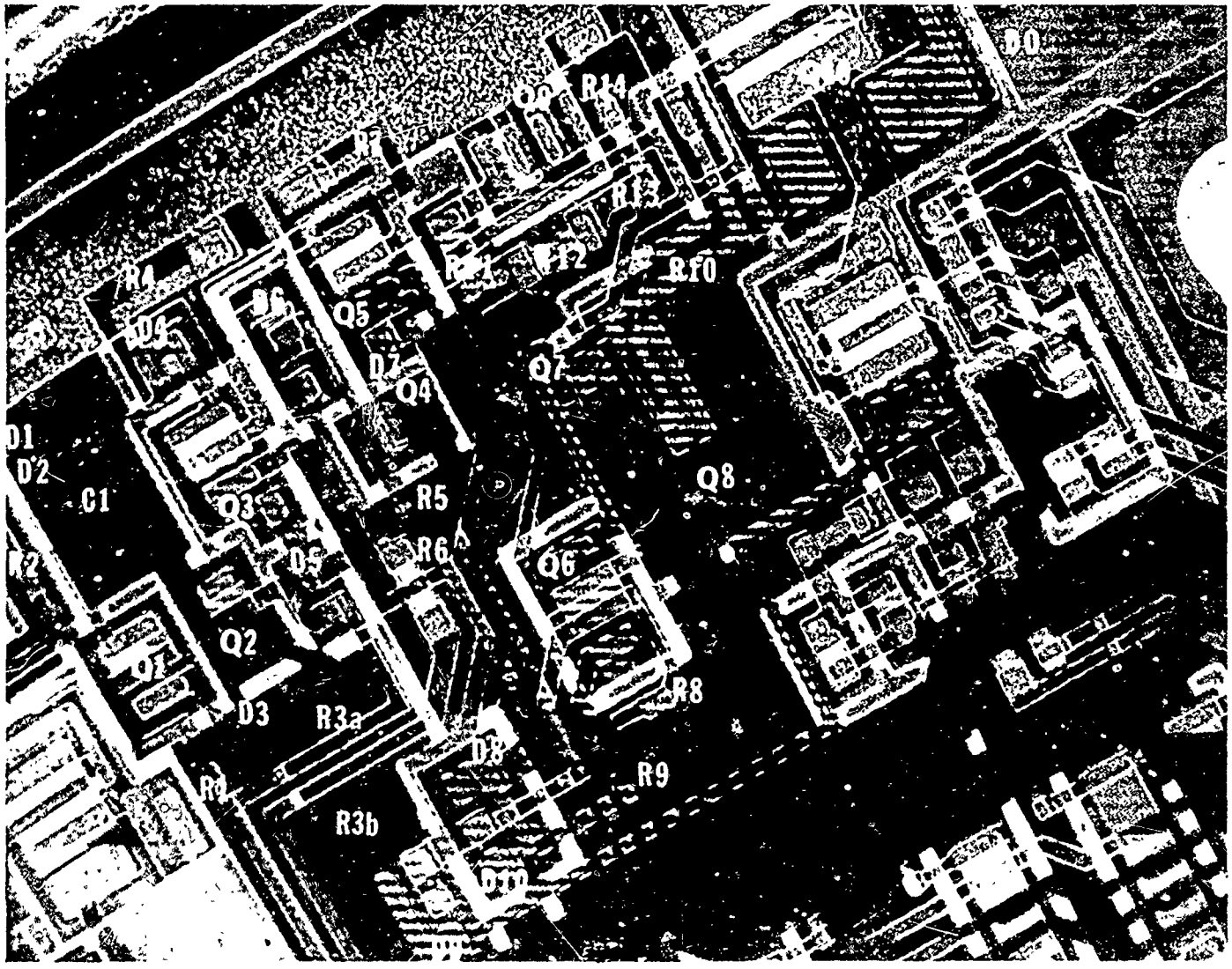


Photo 4- 34 Voltage Contrast Micrograph of Data Output Circuit. 5 KV, Mag. - 385X

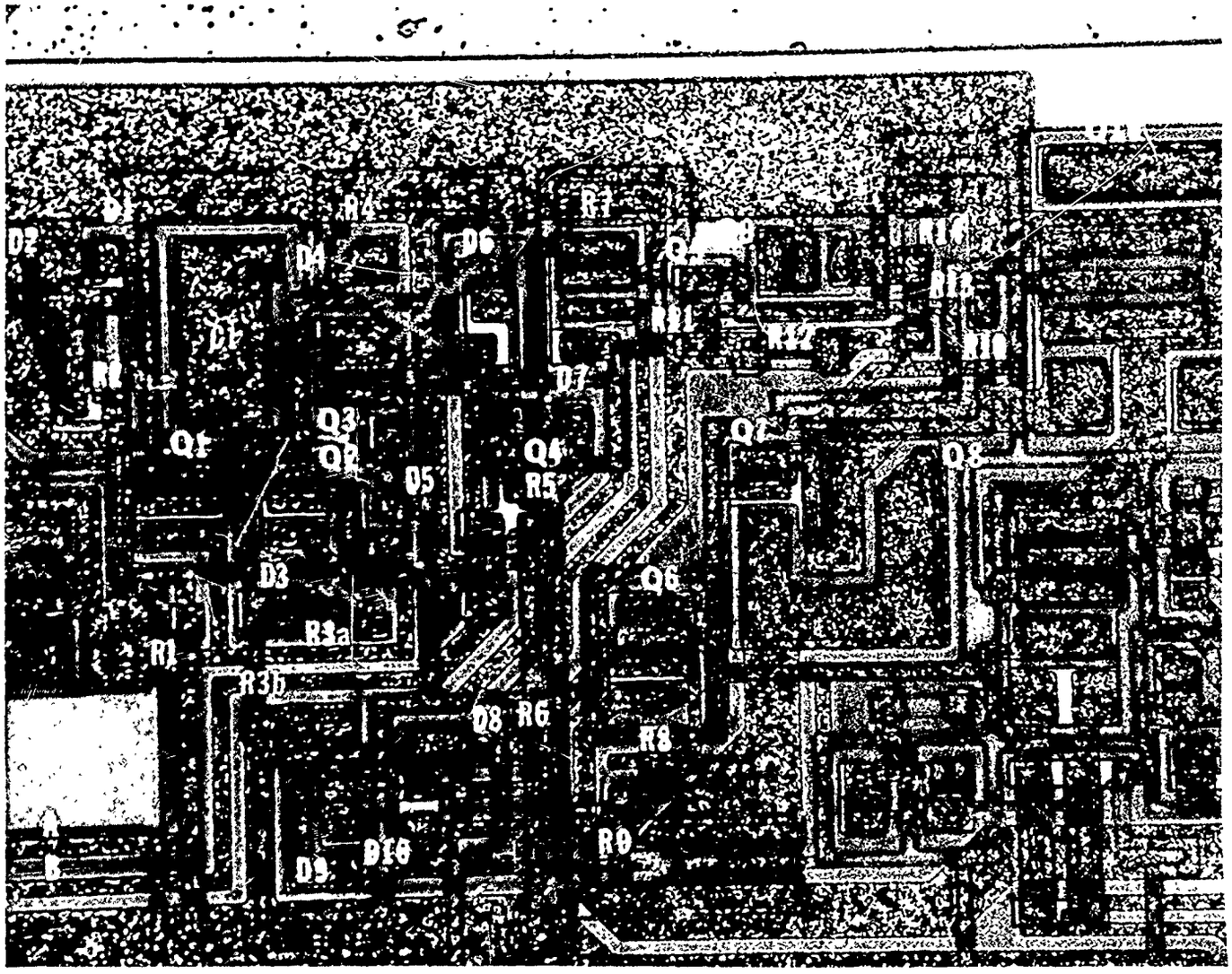


Photo 4-35 Light Photograph of Data Output Circuit. Mag. - 310X

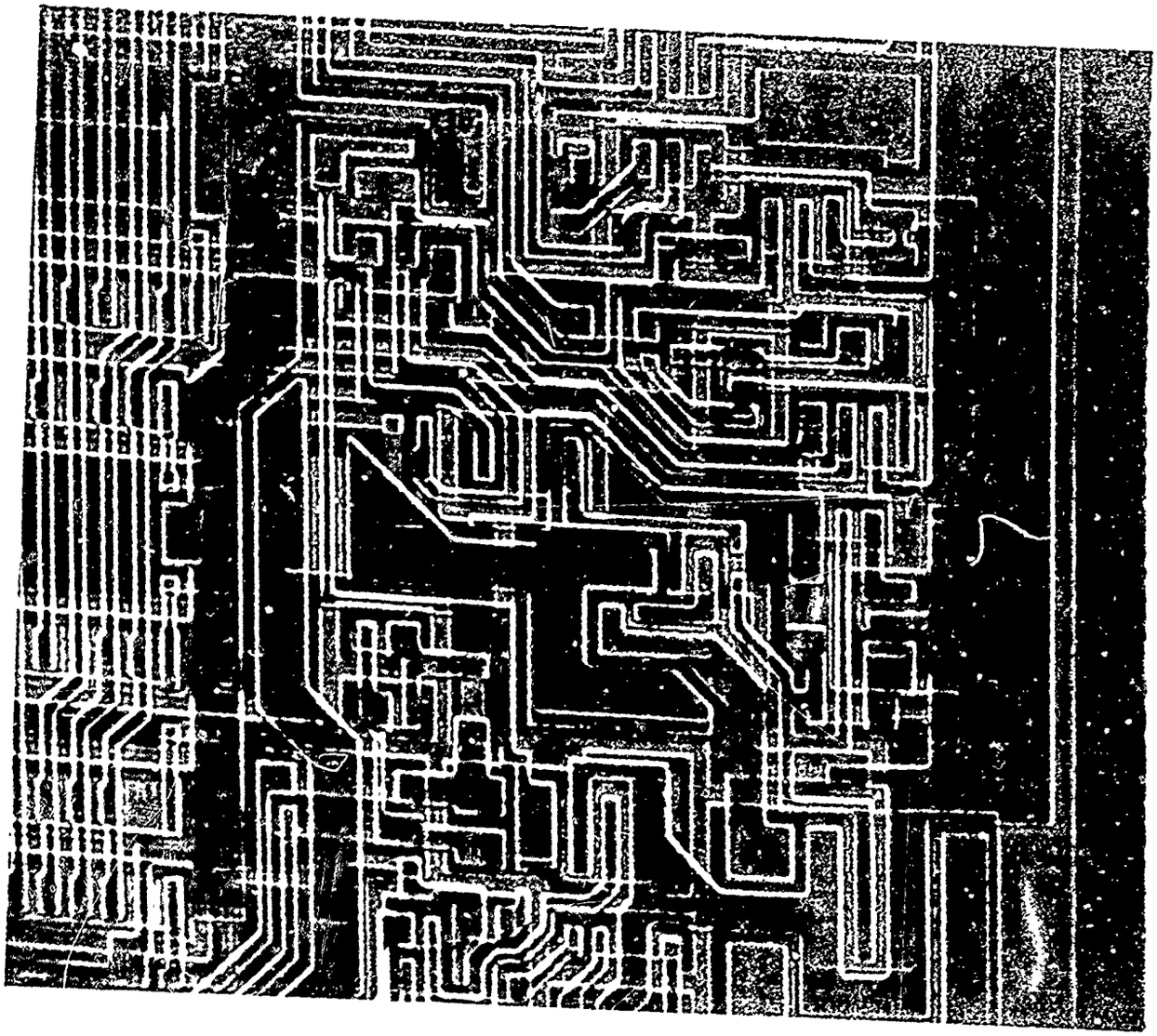


Photo 4-36 SEI Micrograph of Data Output Circuit. 20 KV, Mag. - 310X

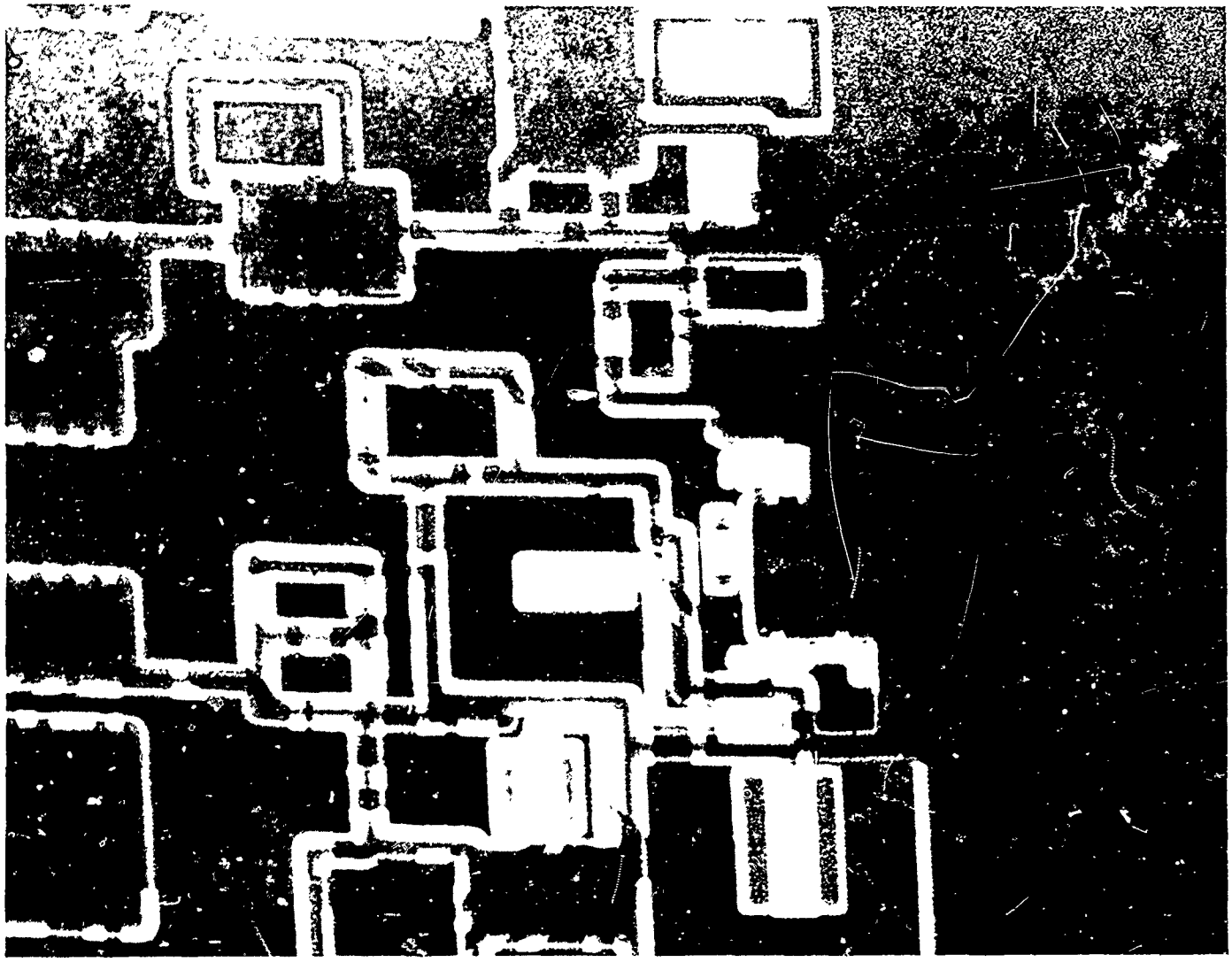


Photo 4-37 EBIC Micrograph of Data Output Circuit. Pin 6 and 16 to SCA, Pin 8 to GND. 20 KV, Mag. ~ 310X

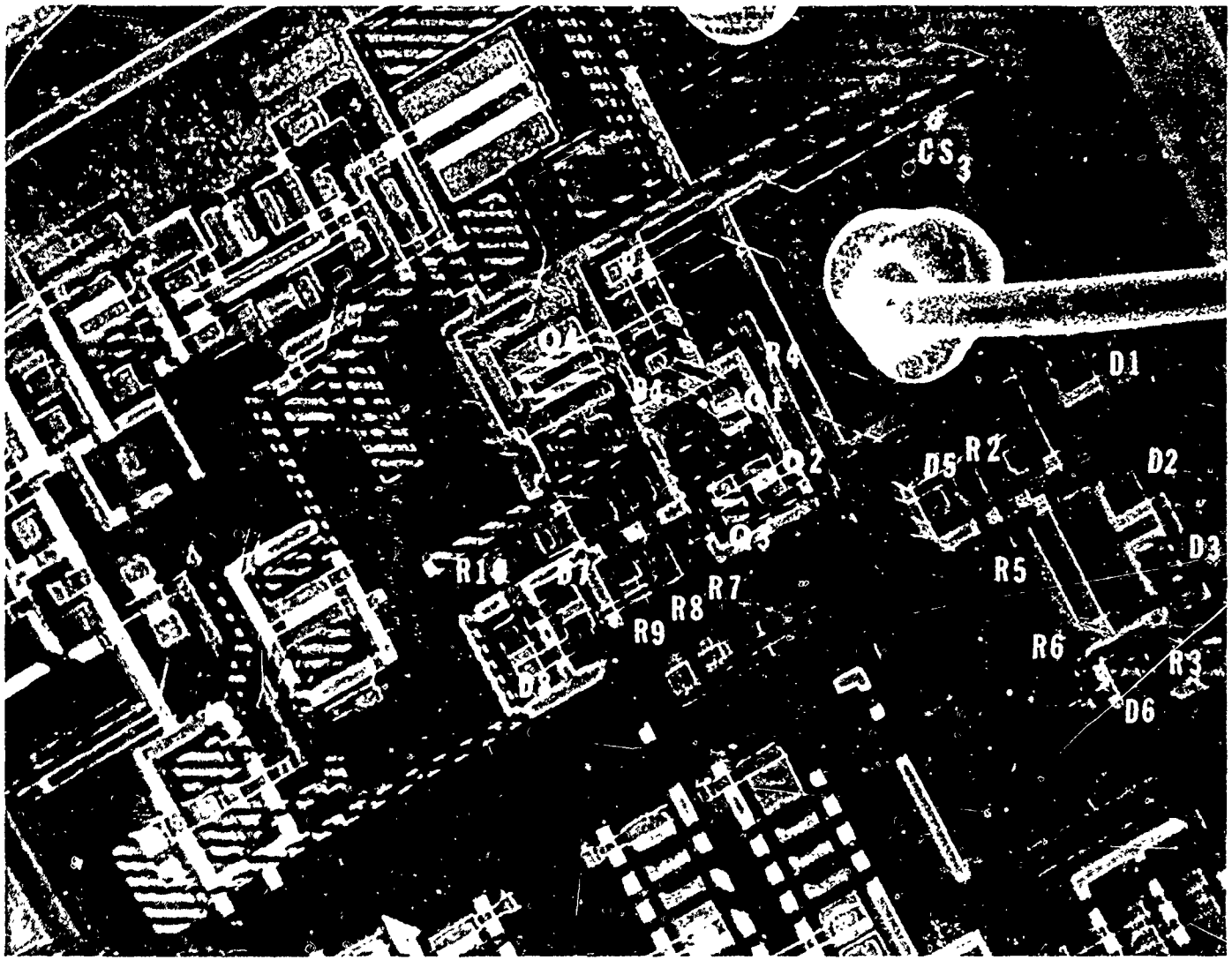


Photo 4-38 Voltage Contrast Micrograph of Chip Select Circuit. 5 KV, Mag. - 340X

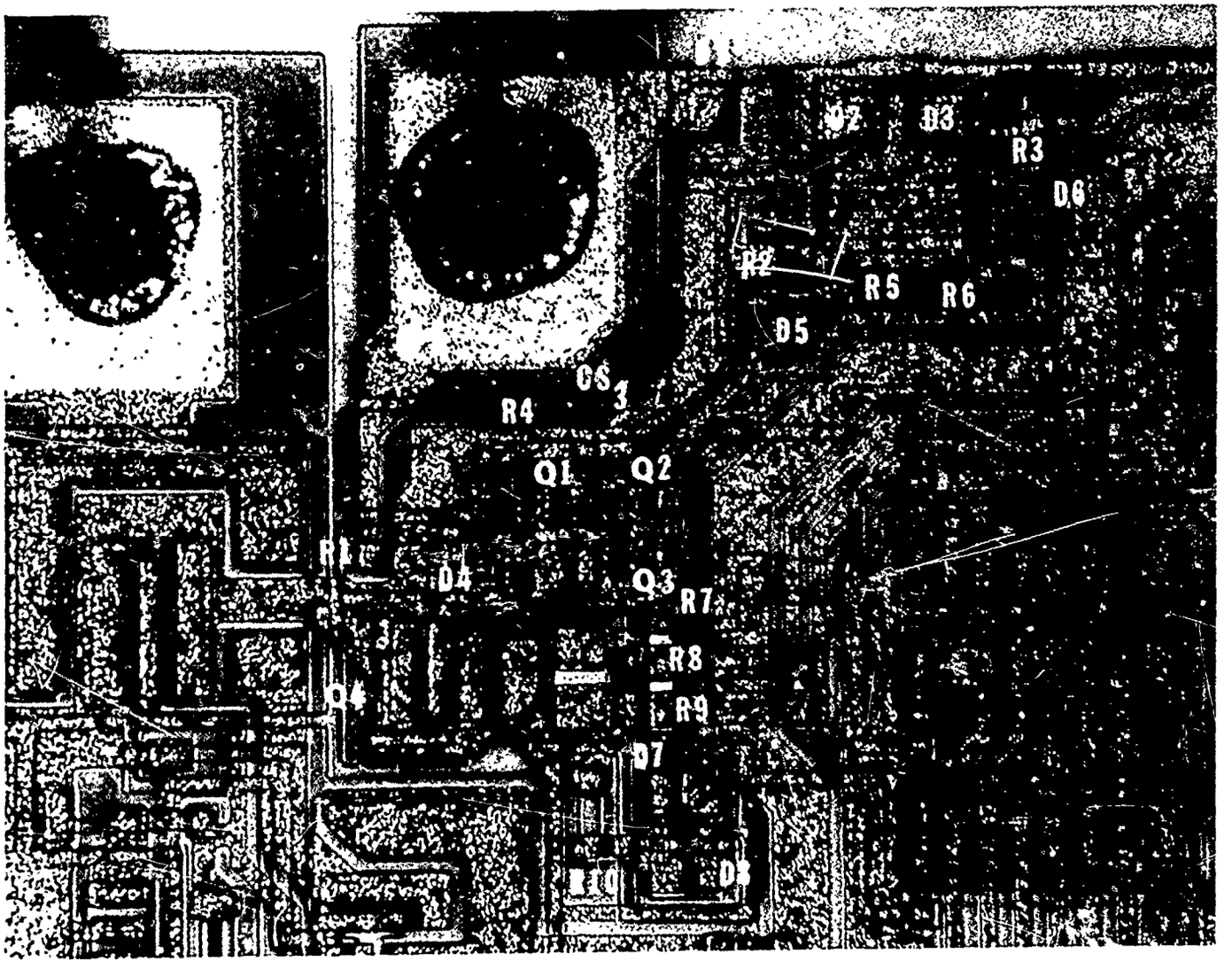


Photo 4-39 Light Photograph of Chip Select Circuit. Mag. - 310X

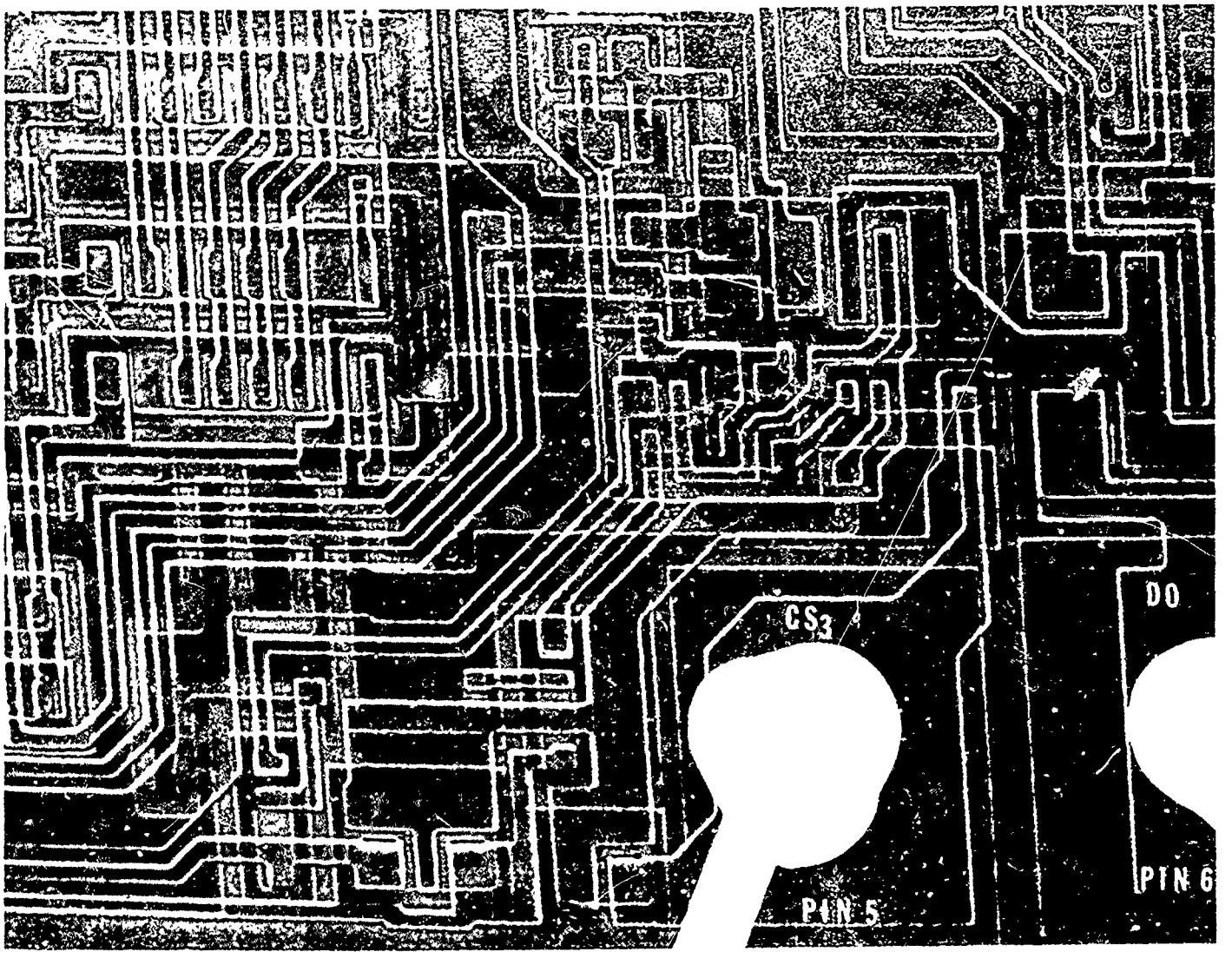


Photo 4-40 SFI Micrograph of Chip Select Circuit. 20 KV, Mag. - 385X

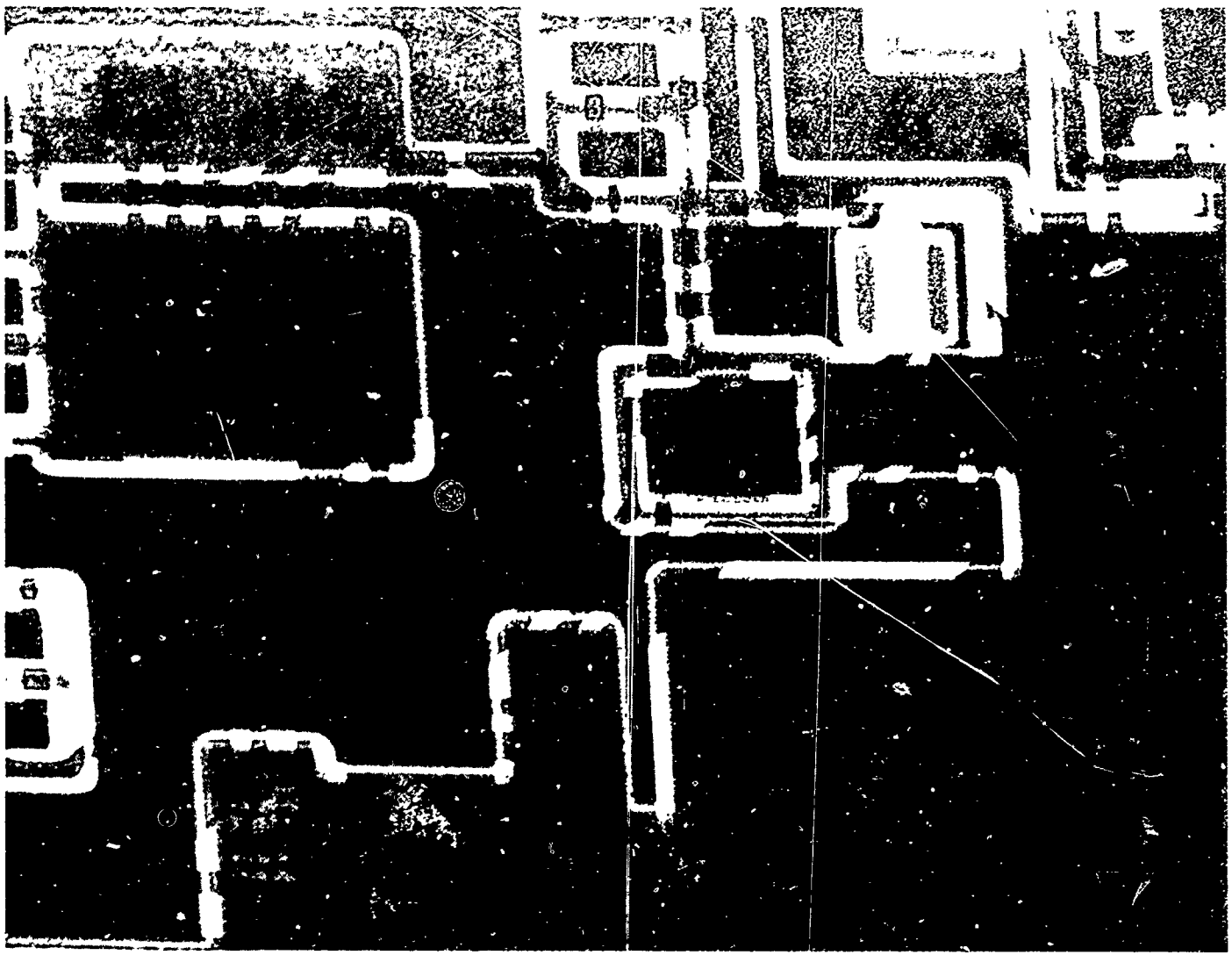


Photo 4-41 EBIC Micrograph of Chip Select Circuit. Pin 16 to SCA, Pin 8 to GND. 20 KV, Mag. - 385X

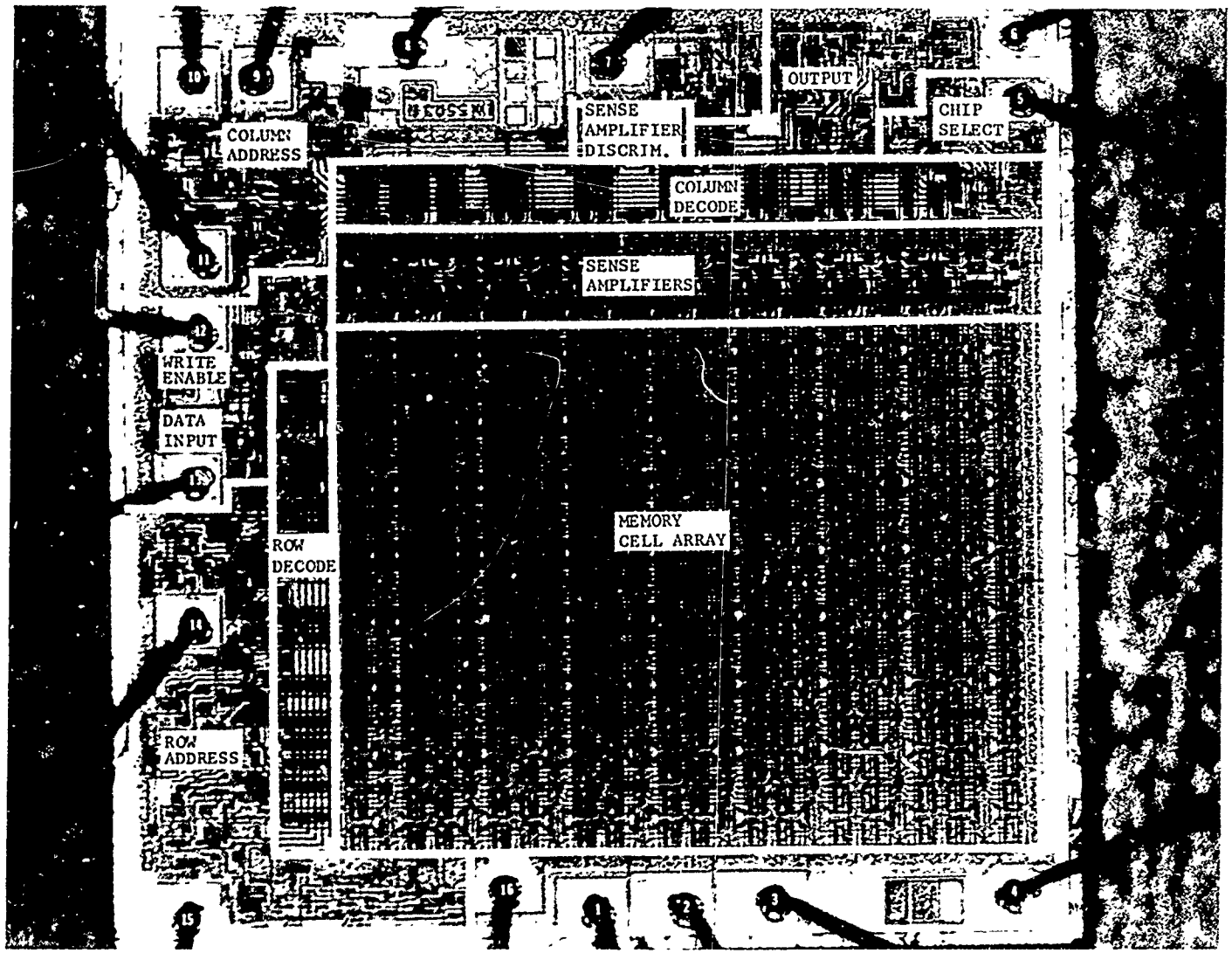


Figure 4-42 Light Photograph of Entire Chip Showing the Functional Block Layout. Mag. - 45X

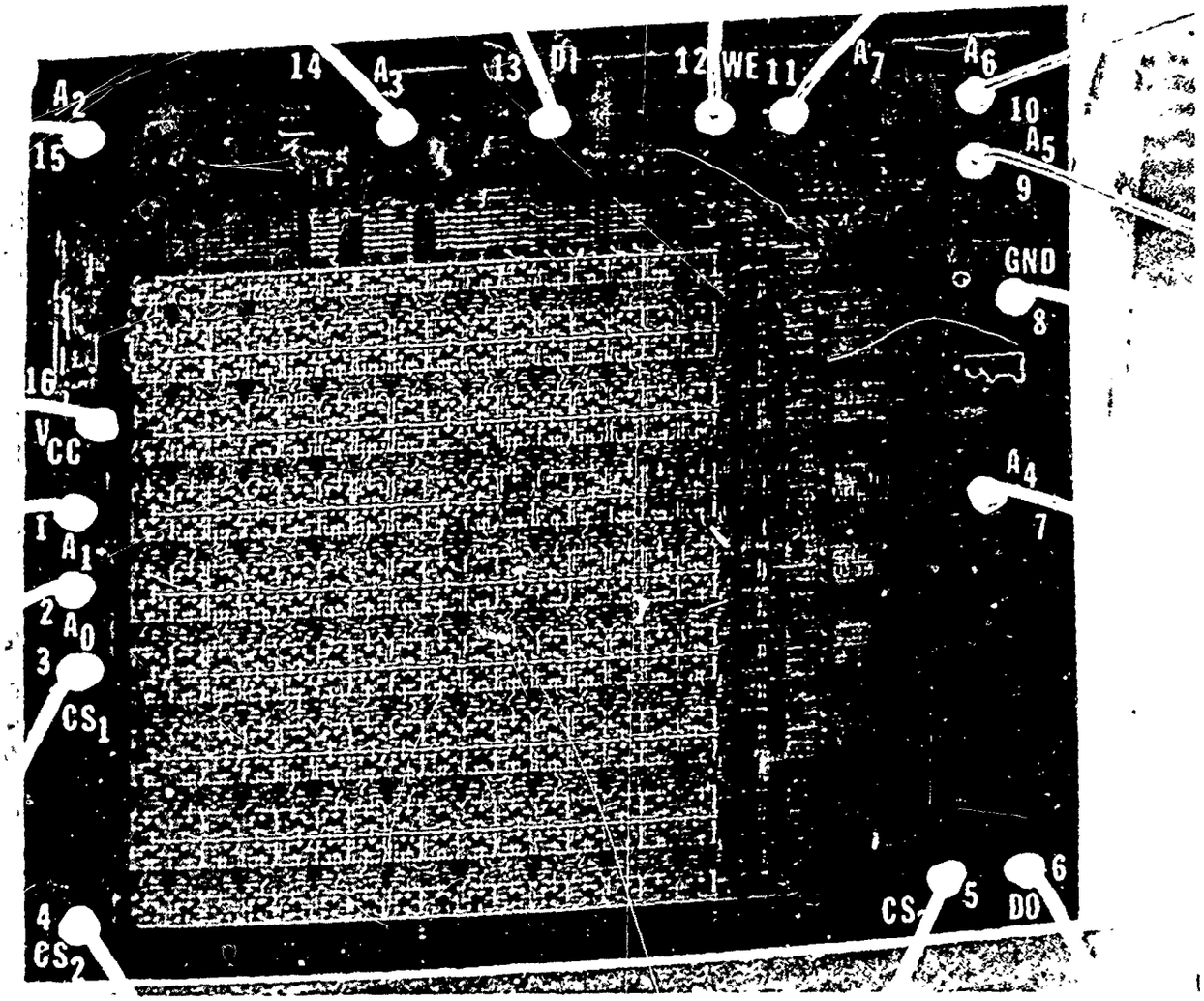


Photo 4-43 SEI Micrograph of Entire Chip. 20 KV, Mag. - 40X

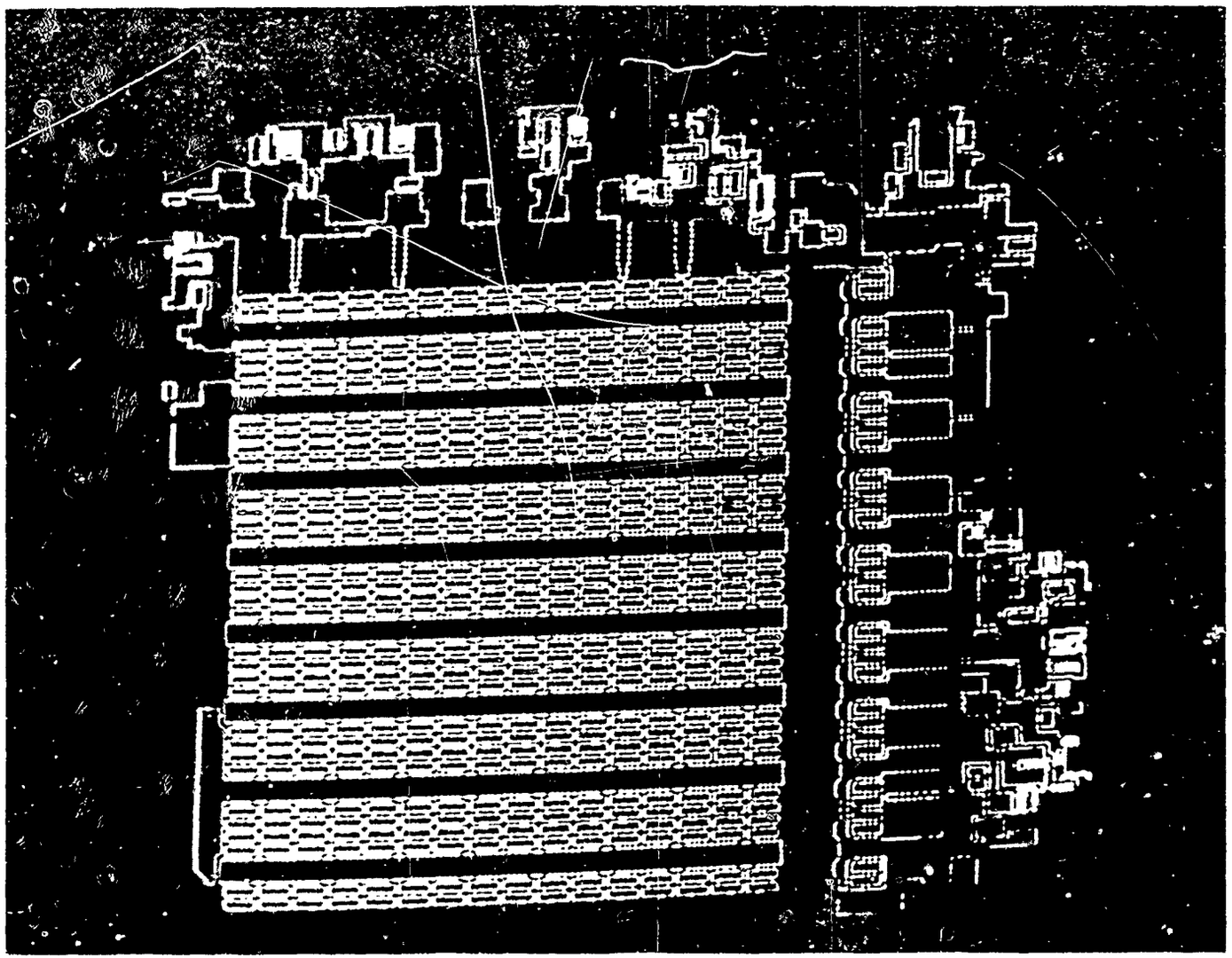


Photo 4-44 EBIC Micrograph of Entire Chip. Pins 12, 13 and 16 to SCA. Pin 8 to GND. 20 KV, Mag. - 40X

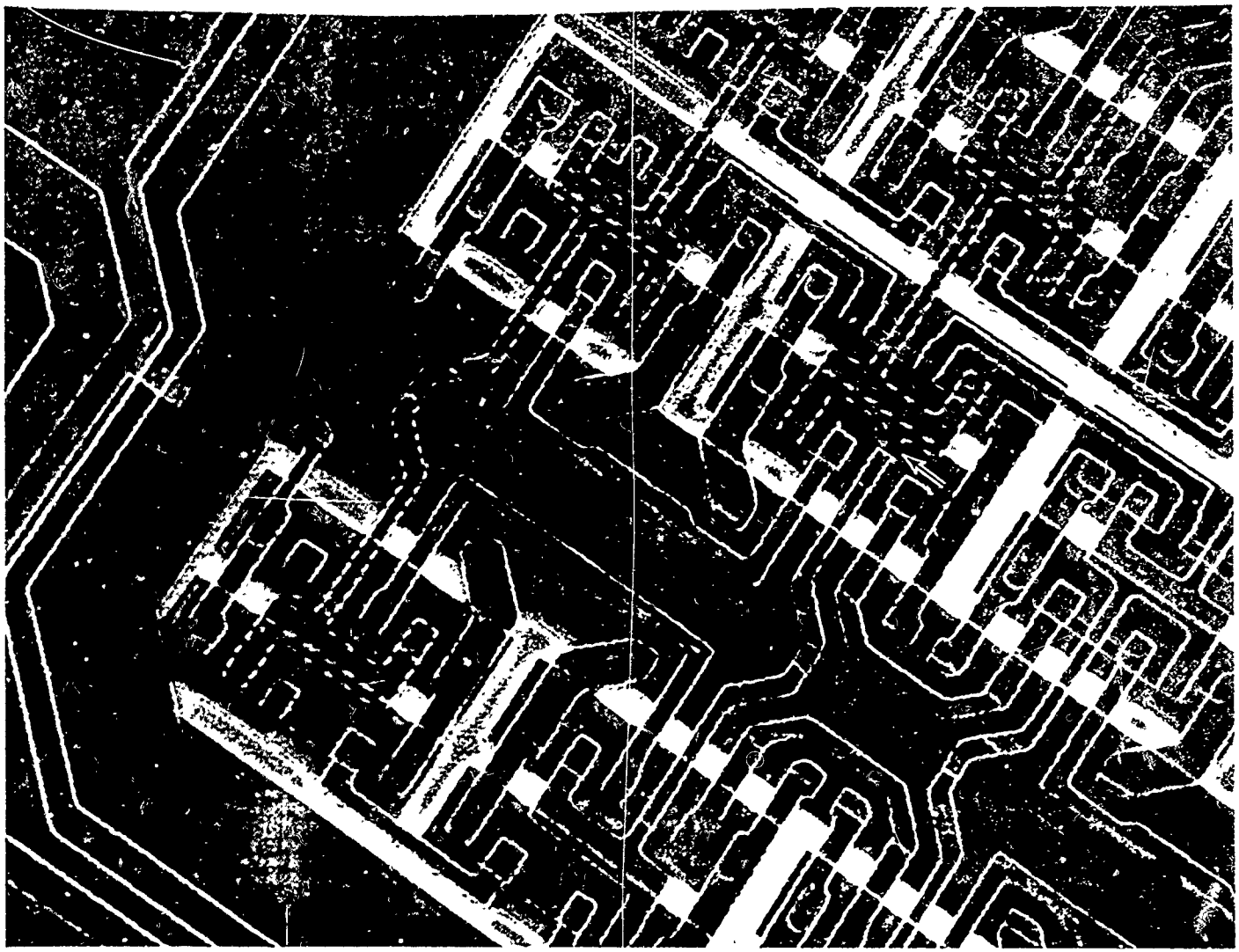


Photo 4-45 Voltage Contrast Micrograph Showing Loss of Row Decode Signal to Word 14 Cell (Arrow). 5 KV, Mag. - 870X

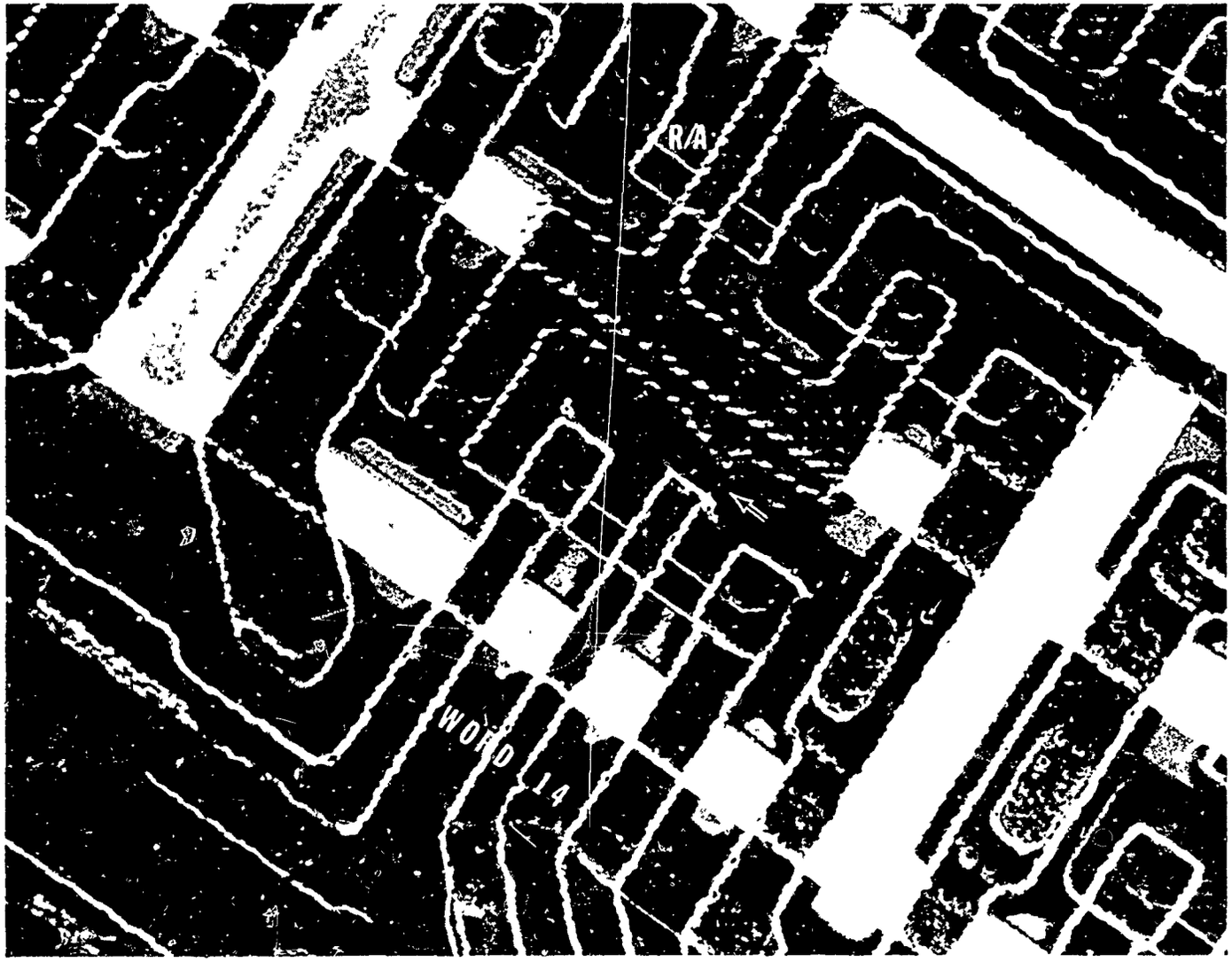


Photo 4-46 Voltage Contrast Micrograph Showing Open in Row Decode Metal Stripe to Word 14 Cell (Arrow). 5 KV, Mag. - 1550X

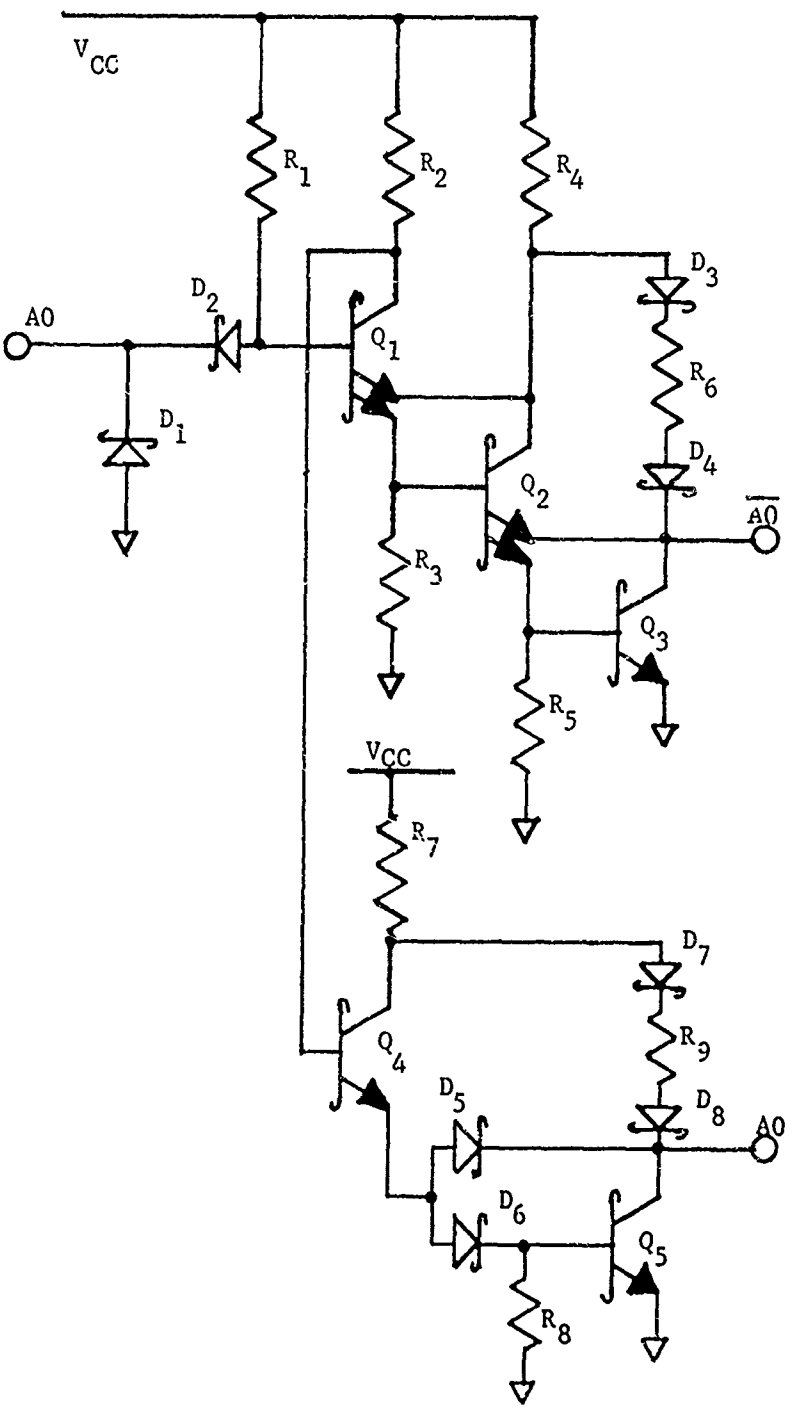


Figure 4-1 Schematic, Row Address Inverter

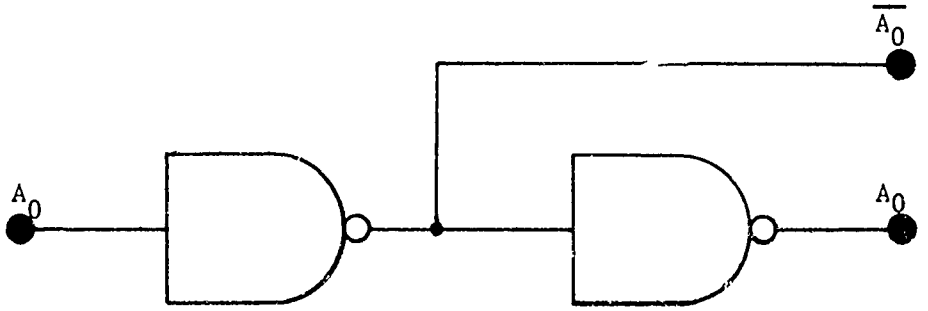


Figure 4-2 Logic Diagram, Row Address Inverter

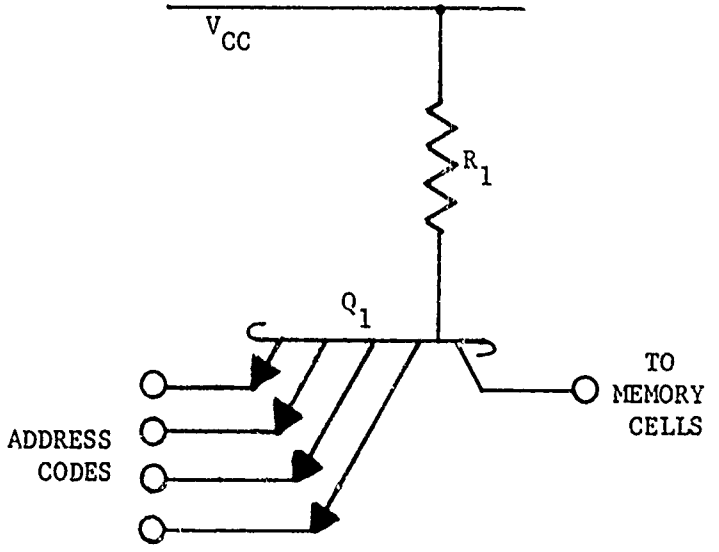


Figure 4-3 Schematic, Row Decoder, 1 of 16

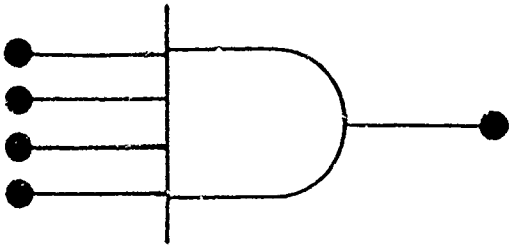


Figure 4-4 Logic Diagram, Row Decoder

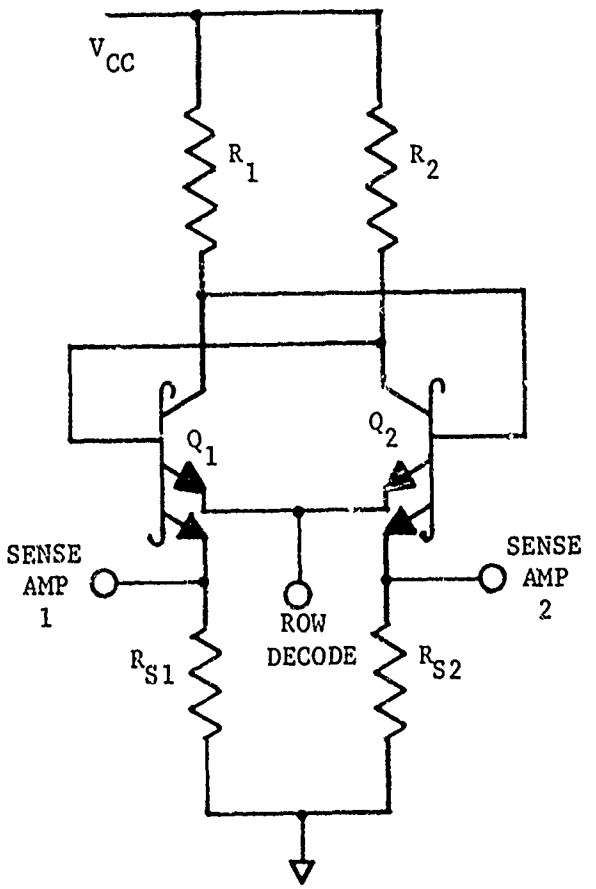


Figure 4-5 Schematic, Memory Cell

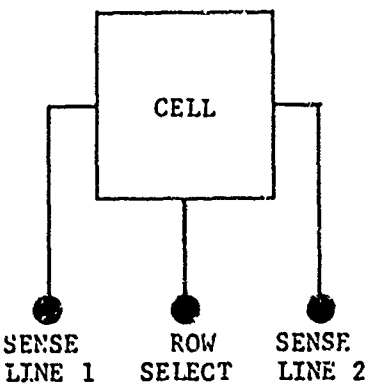


Figure 4-6 Logic Diagram, Memory Cell

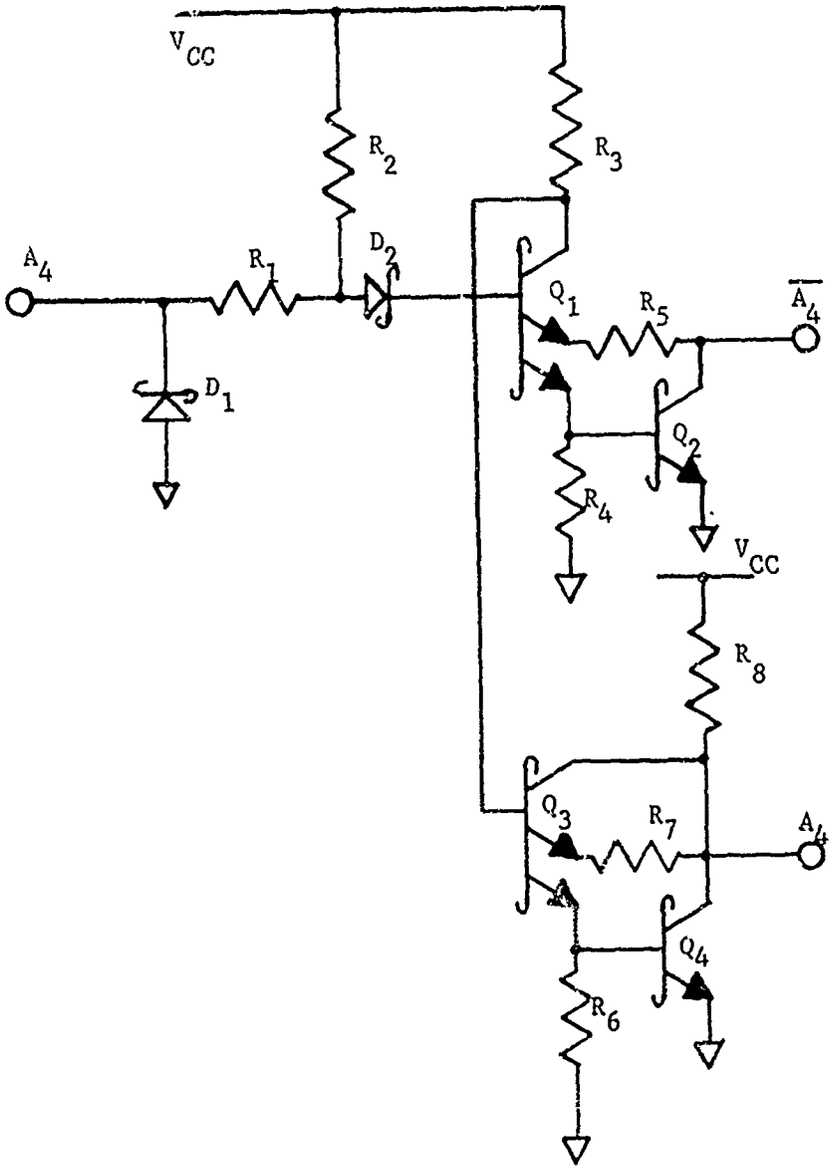


Figure 4-7 Schematic, Column Address Inverter

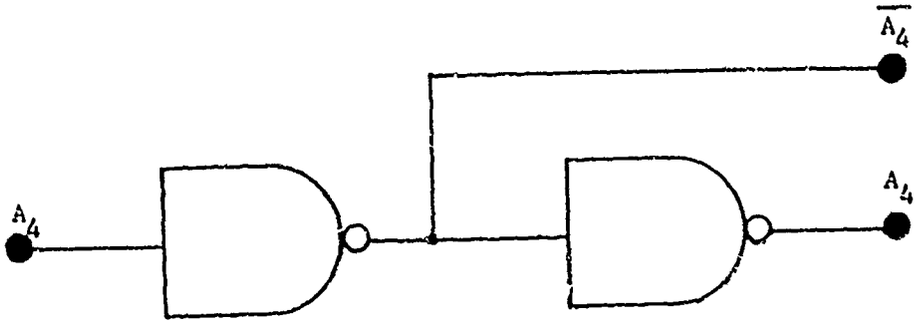


Figure 4-8 Logic Diagram, Column Address Inverter

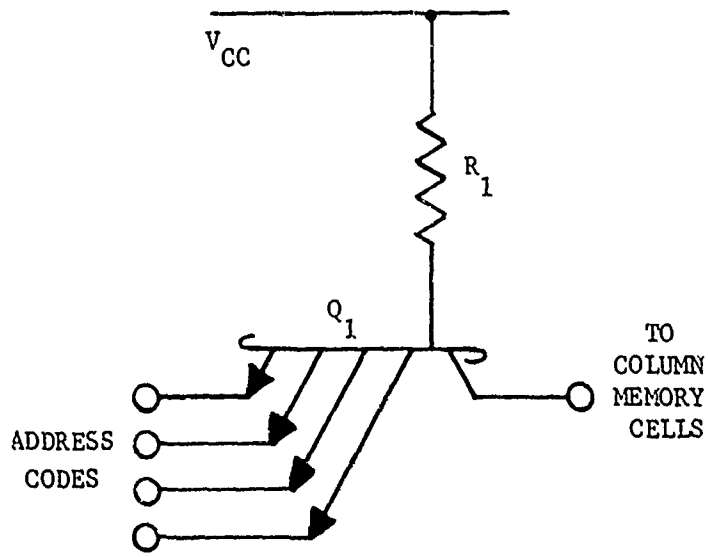


Figure 4-9 Schematic, Column Decode, 1 of 16

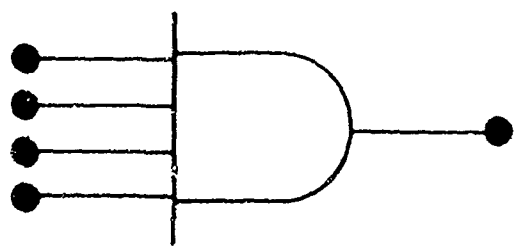


Figure 4-10 Logic Diagram, Column Decode, 1 of 16

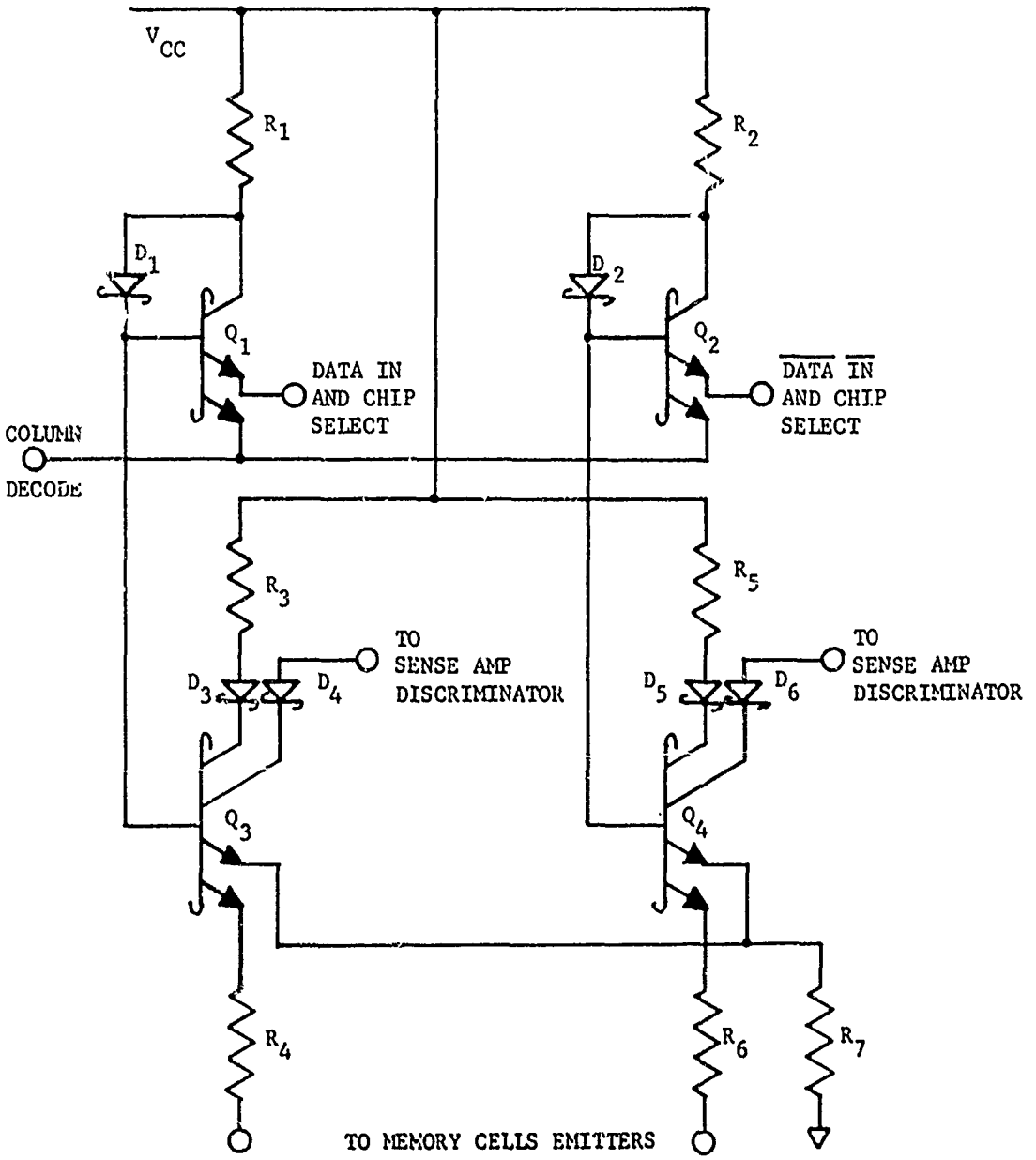


Figure 4-11 Schematic, Sense Amplifier

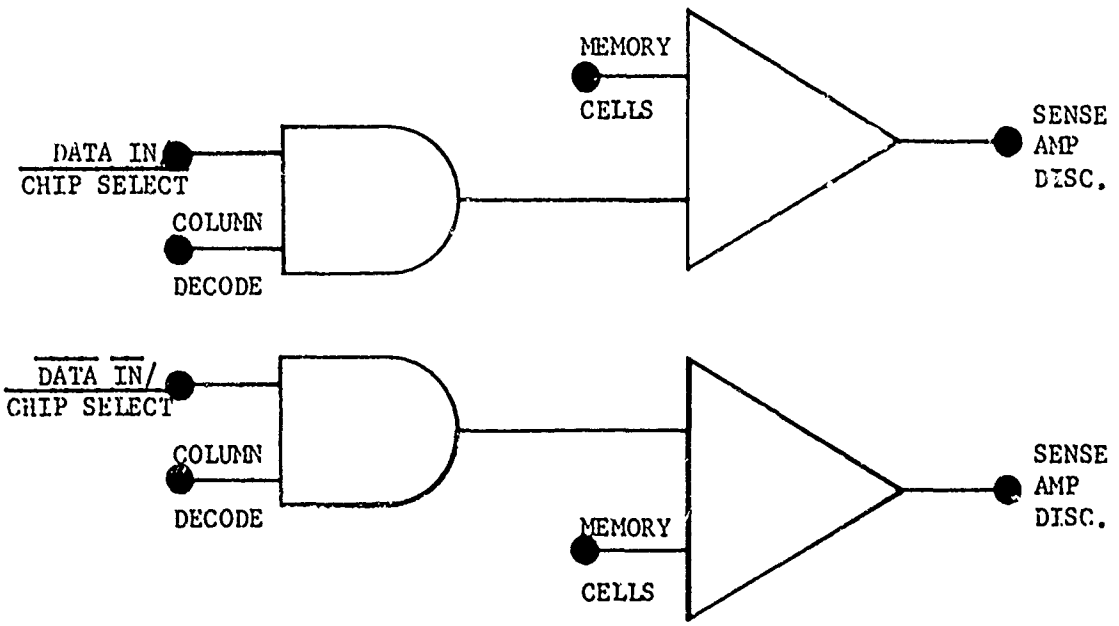


Figure 4-12 Logic Diagram, Sense Amplifier

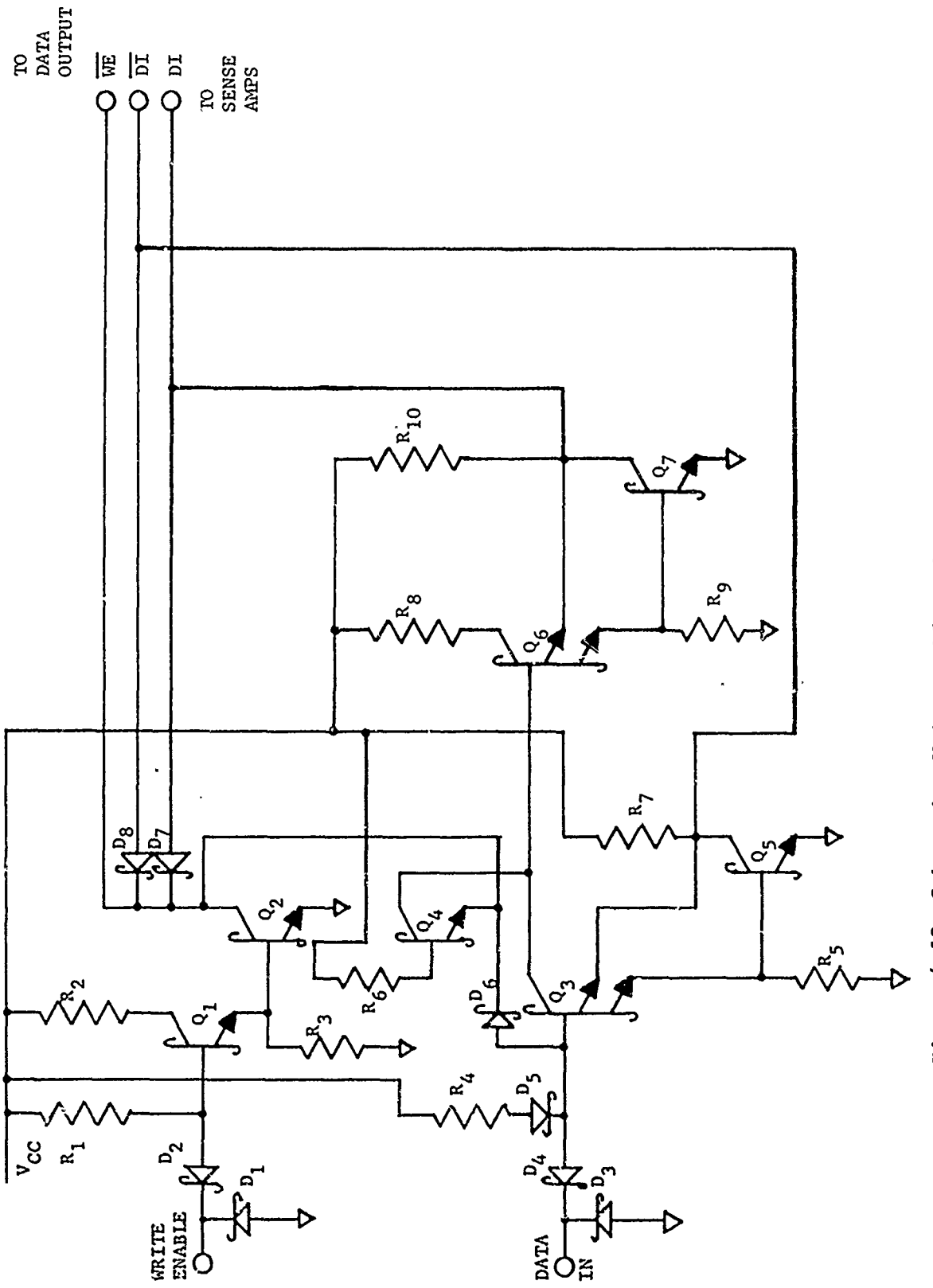


Figure 4-13 Schematic, Write Enable and Data Input Inverter

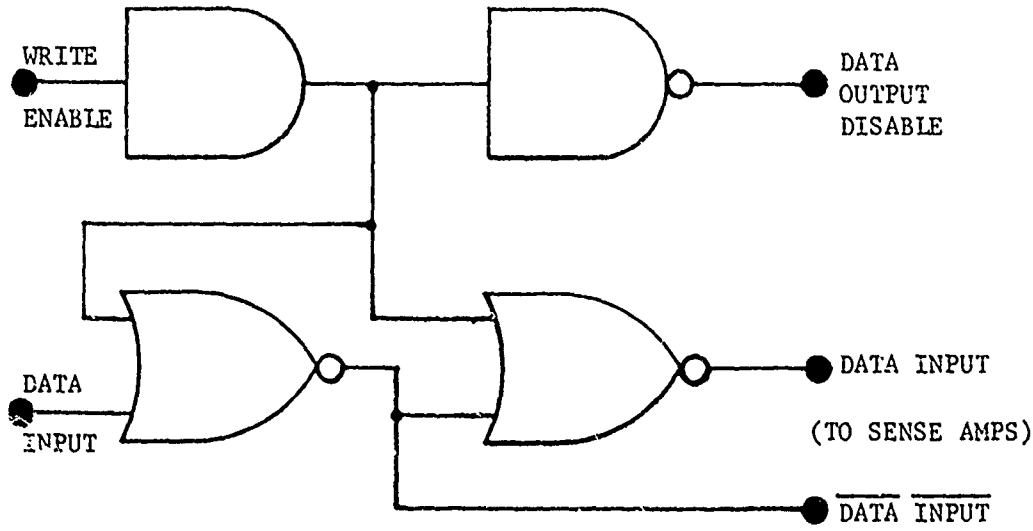


Figure 4-14 Logic Diagram, Write Enable and Data Input Inverter

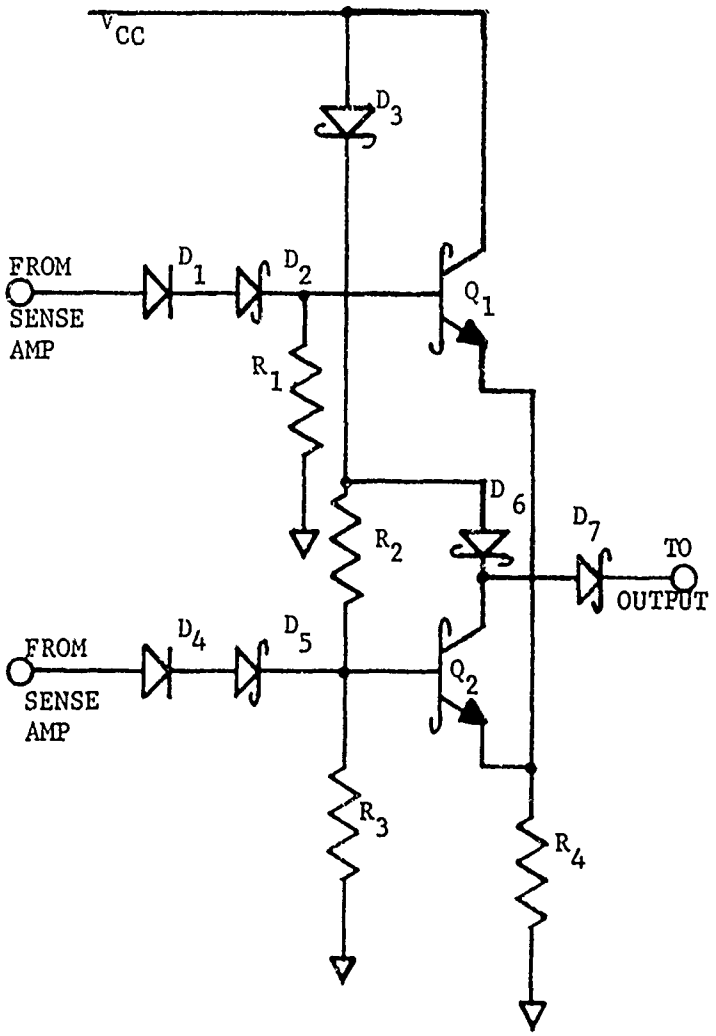


Figure 4-15 Schematic, Sense Amplifier Discriminator

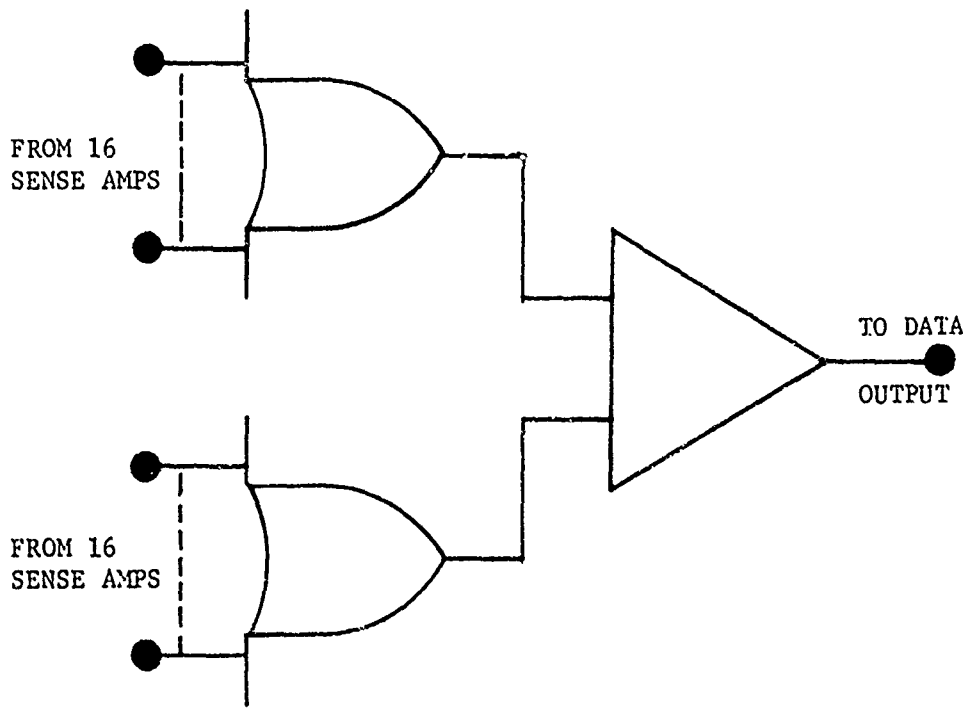


Figure 4-16 Logic Diagram, Sense Amplifier Discriminator

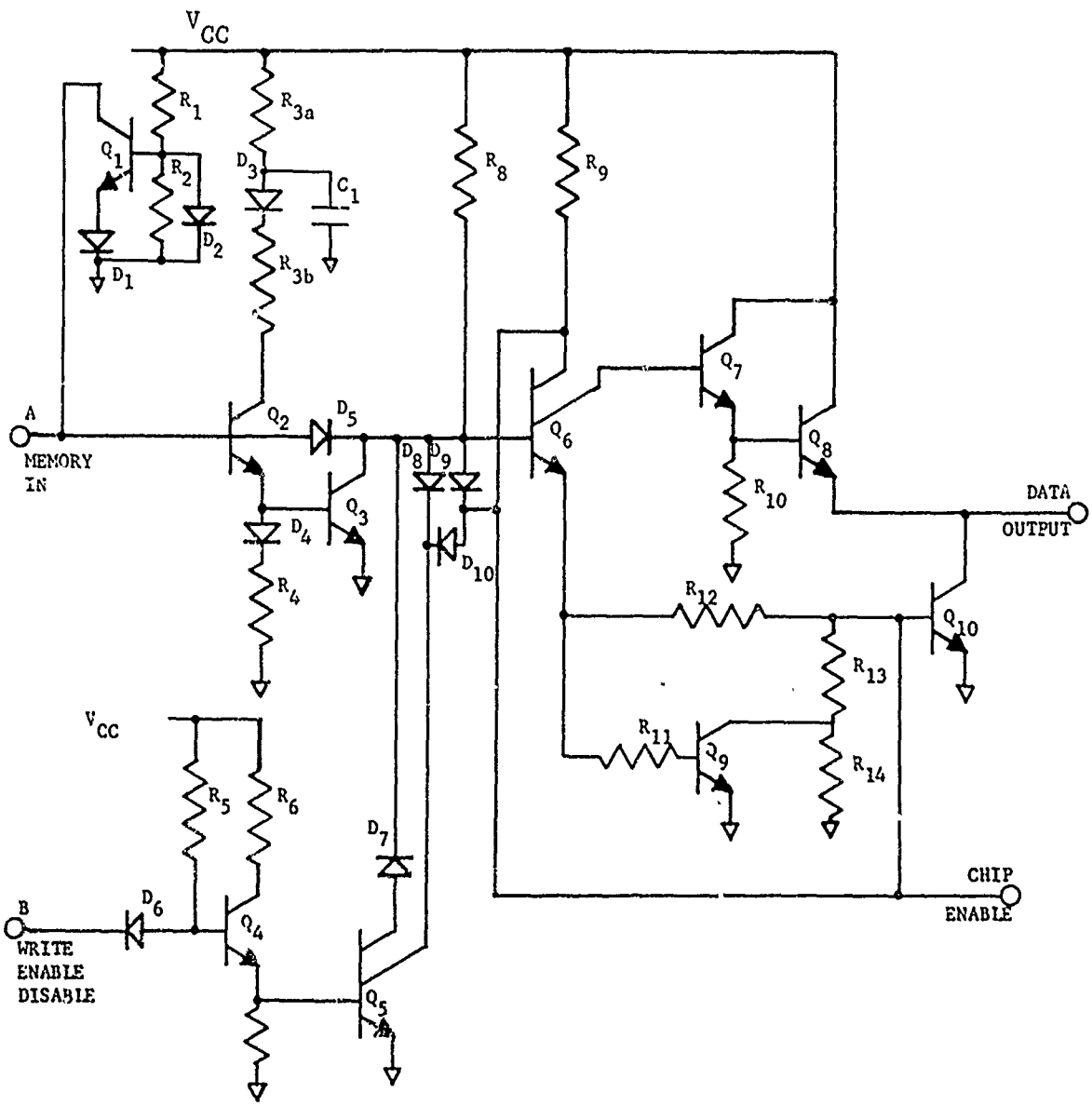


Figure 4-17 Schematic, Data Output

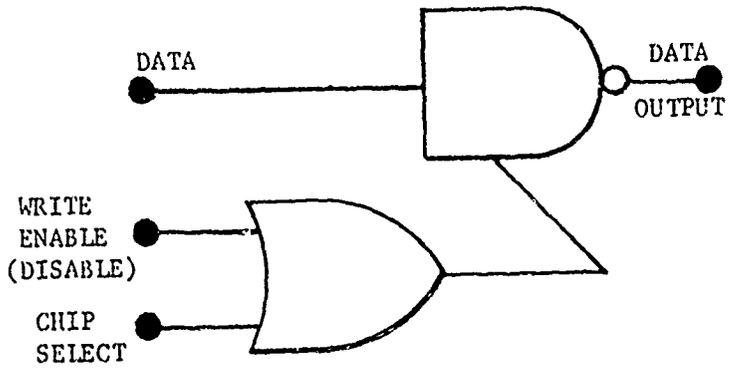


Figure 4-18 Logic Diagram, Data Output Inverter

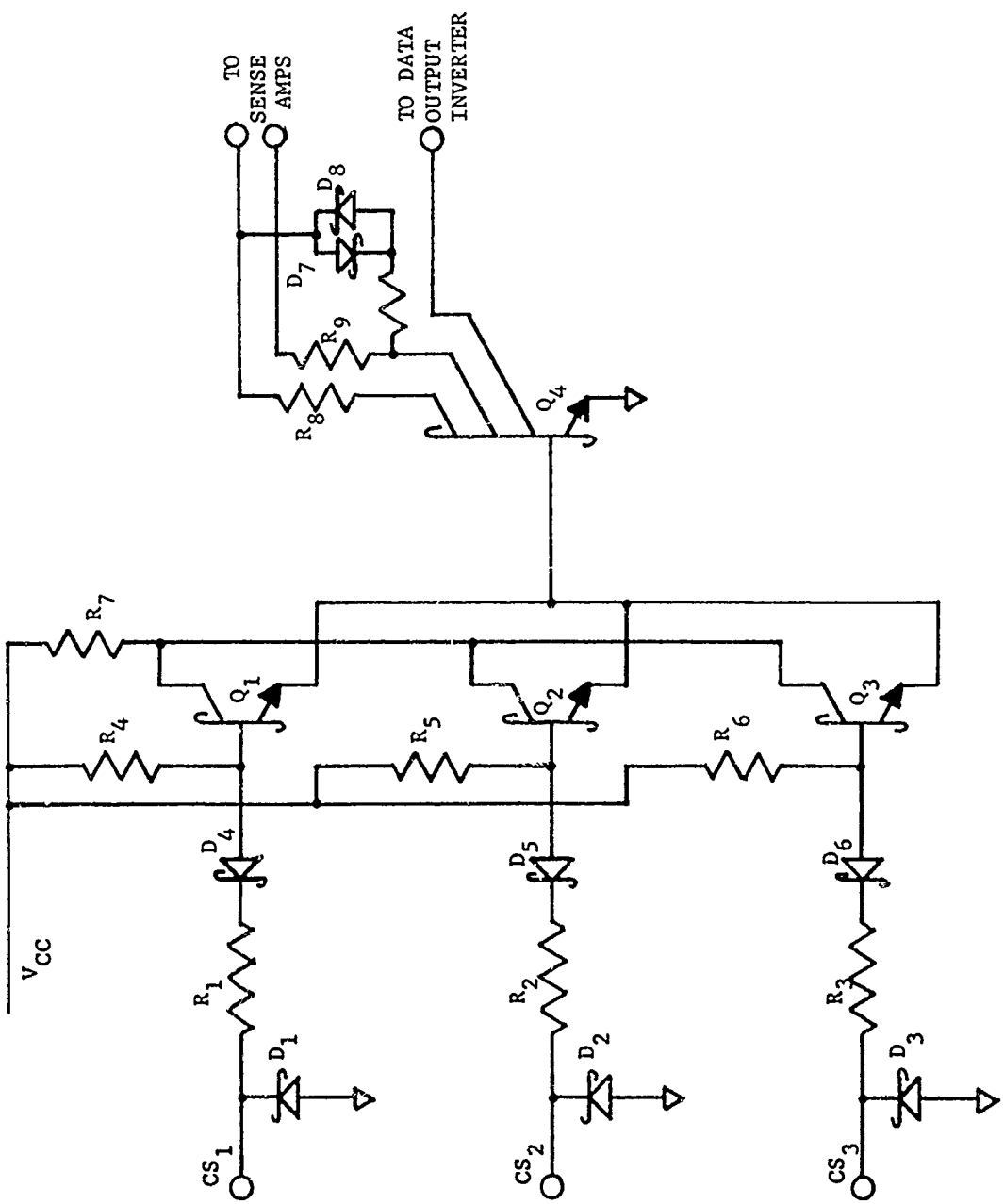


Figure 4-19 Schematic, Chip Select

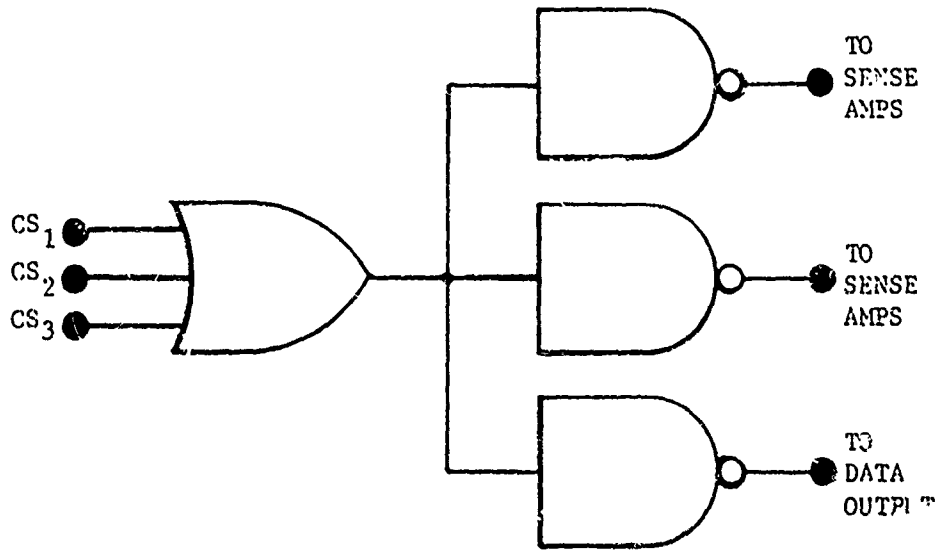


Figure 4-20 Logic Diagram, Chip Select

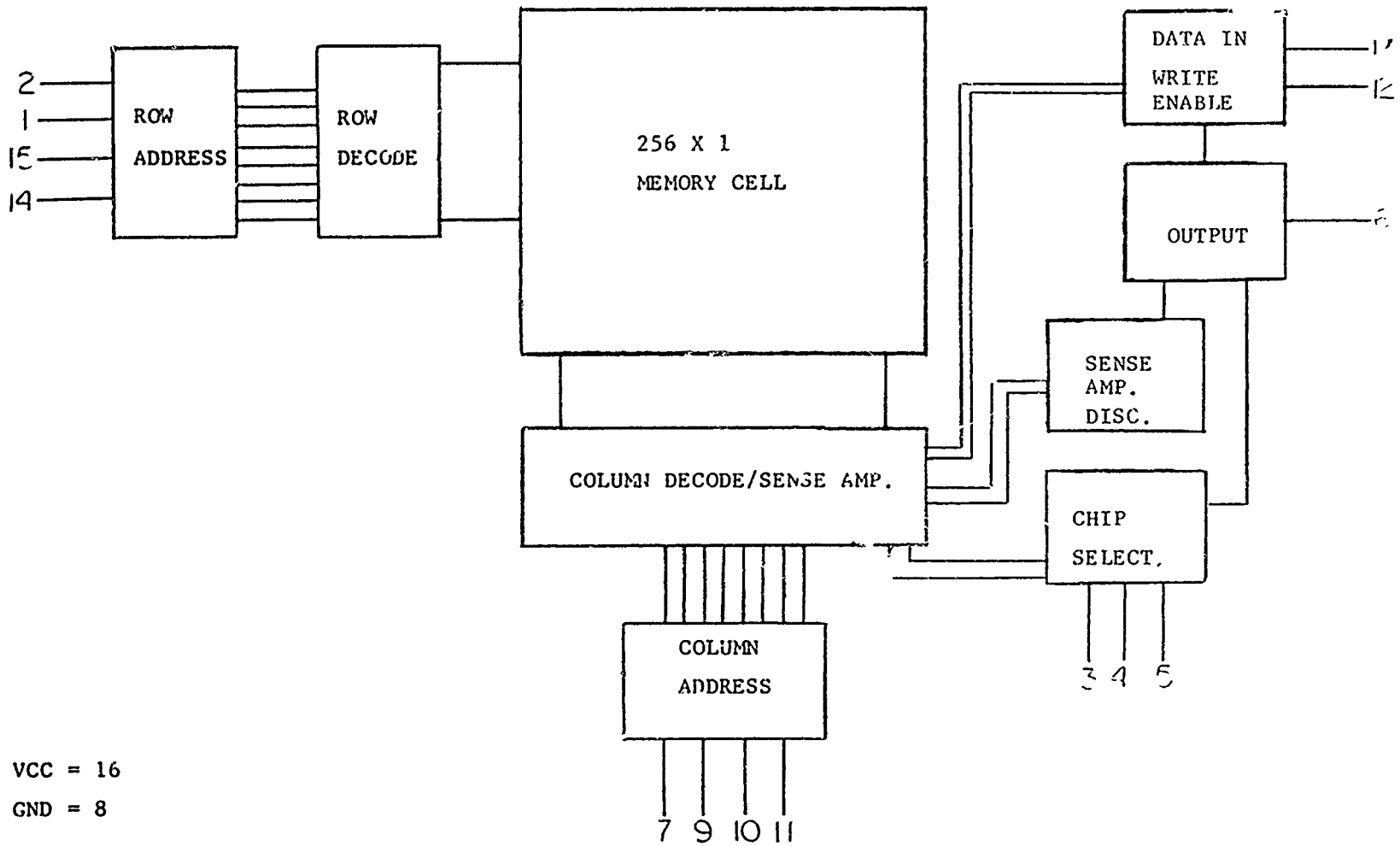


Figure 4-21 Block Diagram

																	ROW DECODE				
																	A3	A2	A1	A0	
																	1	1	1	1	
																	1	1	1	0	
																	1	1	0	1	
																	1	1	0	0	
																	1	0	1	1	
																	1	0	1	0	
																	1	0	0	1	
																	1	0	0	0	
																	0	1	1	1	
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																	0	1	0	0	
																	0	0	1	1	
																	0	0	1	0	
																	0	0	0	1	
																	0	0	0	0	
MSB	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1					A7
COLUMN	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1					A6
DECODE	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1					A5
LSB	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1					A4

Figure 4-22 Bit Map

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