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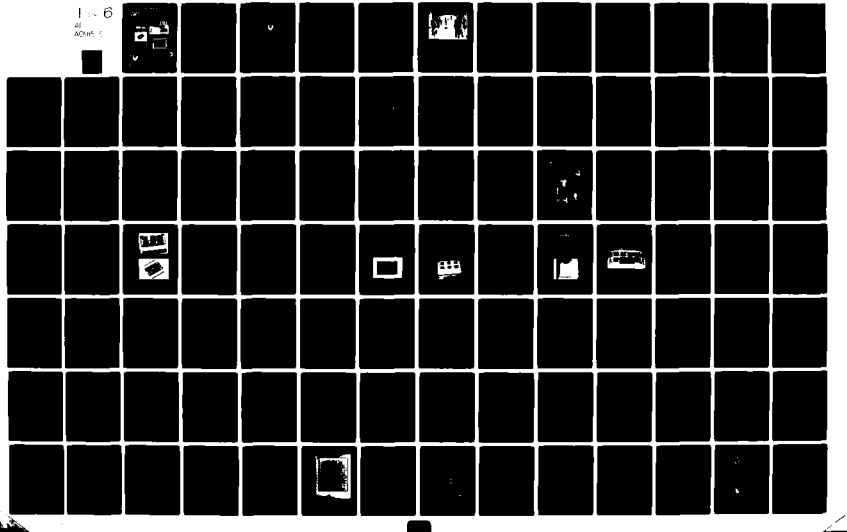

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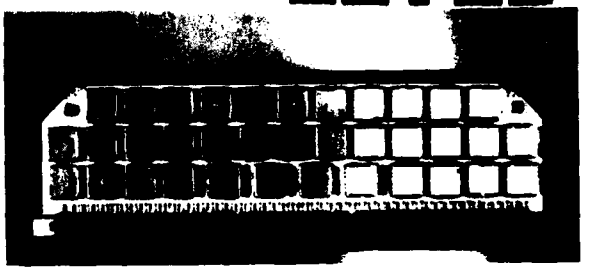

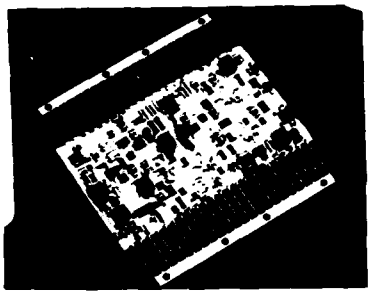

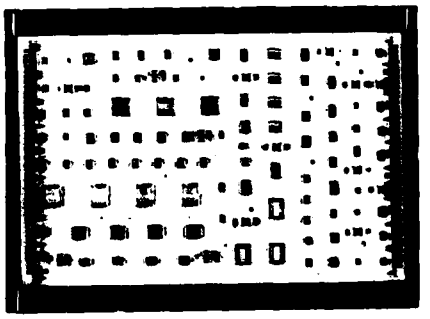

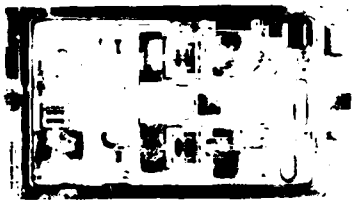

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Symposium was organized by USAERADCOM personnel. Hybrid microcircuits are being applied extensively in government electronics equipment.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
Papers discuss application of hybrid microcircuits in government communications, surveillance and other military electronics equipment. Military use of hybrid microcircuits, past and future were described along with microwave techniques, and progress in film technology and tape processing. Included are papers on advanced processing and manufacturing, new packaging techniques and manufacturing/quality controls.

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## FOREWARD

The Hybrid Microcircuit Symposium in June 1976 emphasized ERADCOM interest in process and quality control, automation and in the application of hybrid microcircuits in Army communication and surveillance equipment. The interim 4 year period has shown hybrid technology progress in these areas and application expansion and evolution into new areas of interest.

The major themes of the '80 ERADCOM Symposium included the increasing interest in higher speed design for circuits with faster operating devices, the growth of the technology as noted by the variety of hybrid microcircuit types for new military applications, the need for efficiency in microwave module manufacturing, and the continuing need for new automated processing, manufacturing and packaging techniques.

The interest by DOD in the development of faster operating devices for high speed data handling is reflected in a number of papers in the Proceedings. As VLSI and DOD supported VHSIC efforts advance toward submicrometer device features for higher speeds, there is a challenge to the hybrid industry for corresponding advancements for device packaging including new approaches for fine line capabilities for high density interconnections, reduction of propagation delays, thermal management of individual devices and provisions for higher pin counts.

The maturity of the technology is noted in a paper which includes an historical review of the basic hybrid fabrication problems encountered and resolved as the hybrid circuit complexity kept pace with the evolution of integrated circuits from SSI to VLSI. The technology growth is exemplified in the paper on the status of copper development toward a viable and practical thick film system. Adaptation of copper based microcircuits for future military applications is important in reducing DOD dependence on high cost precious metals.

Papers related to large tactical display systems, phased array antenna modules, oscillators with high accuracy, computer controlled imaging system for inspection, and computer aided manufacturing indicate areas where the challenge is development of improved automated assembly techniques to bring the product to an economically attractive manufacturing mode or where the techniques or processes must still be demonstrated along a manufacturing line.

The Symposium attracted over 250 attendees from the hybrid microcircuit community representing industry and government. We were gratified by the many positive comments received on the Symposium. The success of the Symposium is due in great part to the excellence of the technical program and to the associated efforts of the speakers, authors, and session chairmen.

On behalf of the USA ERADCOM management and ourselves, we thank all of the Symposium participants.

OWEN P. LAYDEN
Symposium Chairman

ISAAC H. PRATT
Technical Program Chairman

'80 ERADCOM HYBRID MICROCIRCUIT SYMPOSIUM

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# VHSIC - The Next Generation of Military Microelectronics

C. G. Thornton
US Army Electronics Technology & Devices Laboratory, ERADCOM
Fort Monmouth, New Jersey 07703

## Abstract

The VHSIC program is a joint Army/Navy/Air Force program with DOD oversight. Its intent is to develop a new generation of integrated circuits for real time signal processors suitable for deployment in military systems. The VHSIC products are being developed for a number of specific military applications and should cover most of the needs for a wide range of systems. The program objectives include the development of processors with a high gate-speed product in the smallest size and weight packages. Such products will require major advancements in the integrated circuit technology. Higher speed and greater logic density will necessitate also related improvements in electronic packaging. The challenge of new packaging approaches can be met by advancements in the hybrid technology to enhance the utilization of the new high density and high speed integrated circuit technology.

## Introduction

High speed and high throughput signal and data processing are required to meet the needs of military systems in the mid-eighties and beyond. Such systems are required for rapid collection, analysis and dissemination of battlefield information and for effective weapons control through real time signal processors. The development of such capabilities, i.e. processors with circuit density operating at clock speed to perform hundreds of millions (or more) of operations per second, is the basic intent of the Very High Speed Integrated Circuit (VHSIC) program.

Figure 1 indicates how, in the commercial market place, the number of computing elements on the chip has doubled since the early sixties, with the trend probably continuing for the next several years. The result of this tremendous growth in capability is the availability today of commercial microprocessor chips which contain up to 68000 transistor elements, have about 65,800 sq mils of area and about 15,000 gates on one chip. These are substantial advances when compared with whole computers of the early sixties which used only a few thousand gates. For the military, however, a pressing need still exists for more rapid data processing capability. The problems that need solutions for the fielded systems are such that almost unlimited processing speeds in the smallest size and weight packages can be used.

Trends in processing are indicated in Figure 2. Typical system needs are in the range defined by the oval in the center of the figure. This means reaching the 100 million instructions per second (MIPS) range to solve the operational problems of fielded systems. Commercial computers, such as the Cray IS or Cyber 205, which have such a processing capacity, are of a size that would hardly fit into a RPV or a helicopter or even a tank. The Cray consumes kilowatts of power, has kilograms of weight and costs in the millions of

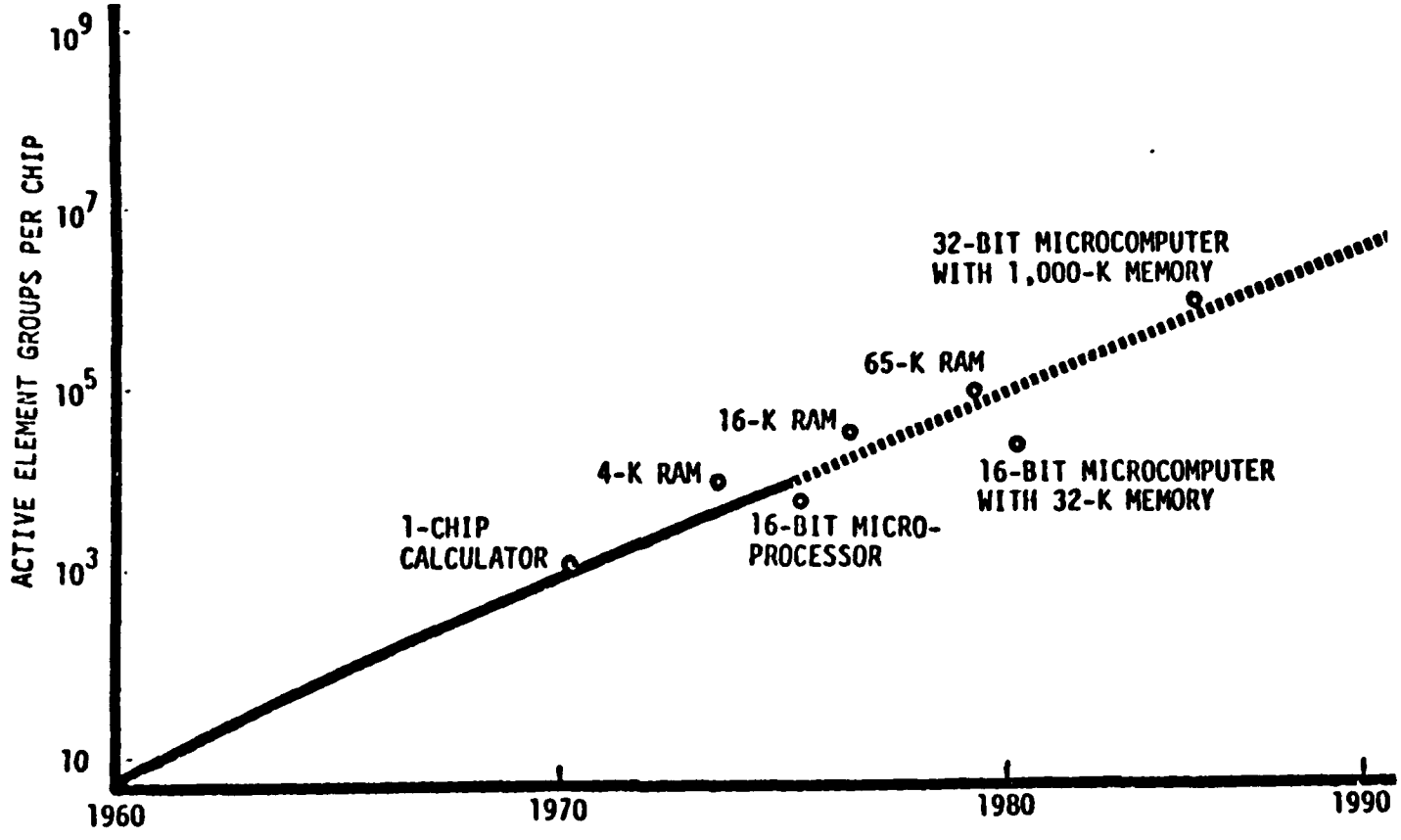


Figure 1. Progress In Integrated Circuit Devices

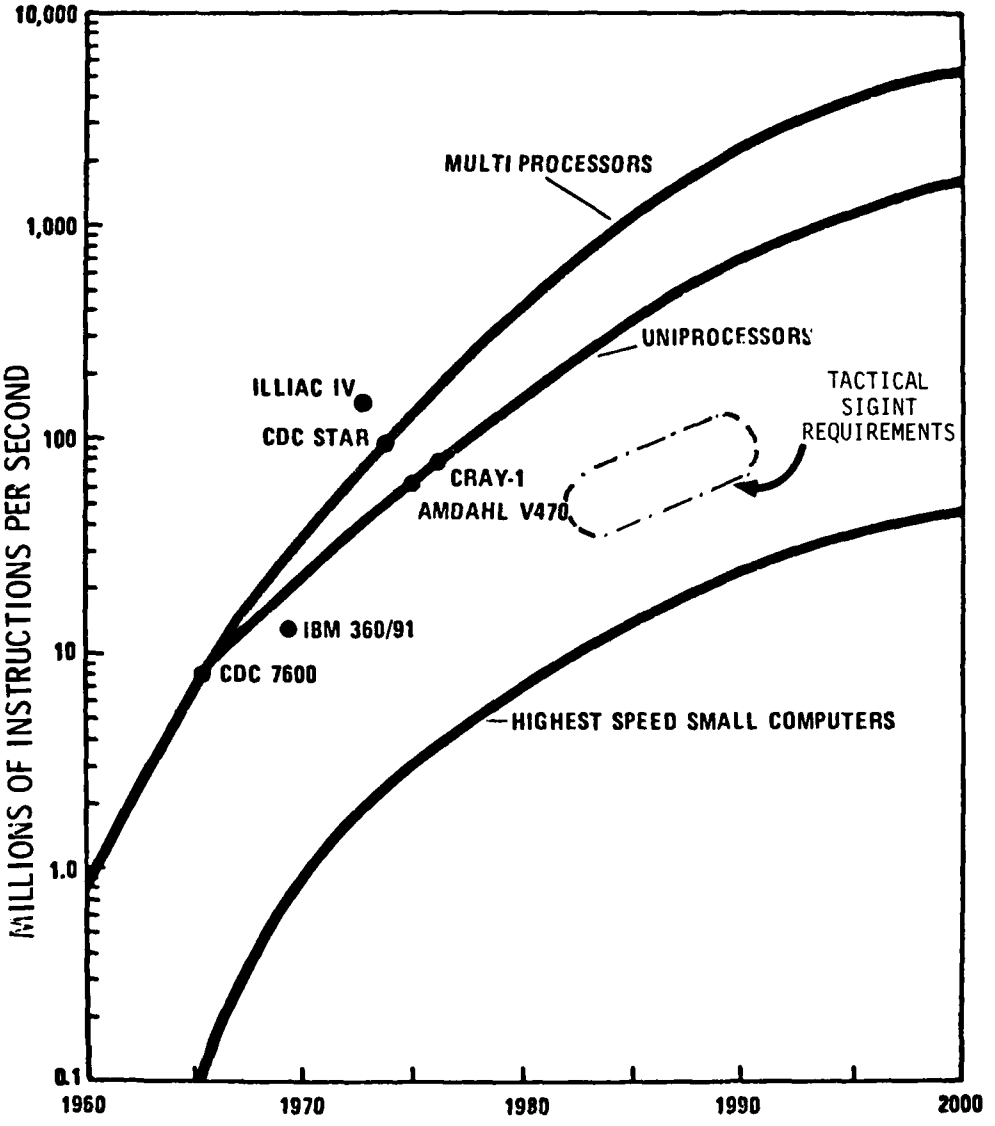


Figure 2. Trends In Processing Speed

dollars. The military needs now the hundred MIPS-and-up capability in some modest size that is associated with a tactical computer.

The VHSIC Program

The VHSIC program is a concerted thrust, involving the military, industrial and scientific communities, to (1) establish and exploit new and very promising plateaus of electronics technology on a highly accelerated basis to provide vastly expanded technological opportunities for design of low-cost, high performance, high reliability equipment, and (2) provide the US Combat Arms with a significantly advanced systems capability in the 1985-1995 time frame to cope with the growing technological threat and the new dynamics of a contemporary war.

The VHSIC program is divided into 4 parts: Phase 0, I, II, and III. Phase 0, now underway, is a Program Definition Phase which entails analyses, partitioning studies, system architecture, chip architecture and design, design layouts and CAD modeling of various weapon systems designed for VHSIC. Phase 0 has nine organizations under contract consisting of from one to six defense electronics/semiconductor/equipment/university companies working together. Approximately $10.4 million of the anticipated $225 million overall VHSIC program is being expended for this feasibility study.

From this Definition Phase, proposals will be obtained that will be used to implement the Phase I portion of the program. Building demonstration systems is the goal of Phase I and the consecutive Phase II. These latter 2 phases will include construction of electronic brassboard systems and provide capabilities for major improvements in system performance by projecting subsystems design concepts to higher performance levels. The state of the art of IC fabrication and design will be extended to sub-micrometer feature sizes during these two phases.

Development of IC's with equivalent clock frequency products in the order of $10^{11}$ gate-hertz/cm$^2$ for Phase I and of $10^{13}$ gate-hertz/cm$^2$ for Phase II will be required to achieve pilot production in 1986 of processors containing 250,000 gates operating at clock speeds of 25MHz. In addition to increasing chip size, the required speed and circuit density necessitate scaling down current circuit configurations by enhancing lithography capability from present 3.0 to 1.25 $\mu$m feature size under Phase I and further extension to submicrometer feature sizes (0.5 to 0.8 $\mu$m) under Phase II.

Phase III consists of VHSIC support programs and is being conducted in parallel with the overall program. Phase III consists of a multiplicity of smaller programs which provide a broad technical base and sources for specific design, manufacturing and test equipment to support the major efforts of Phases I and II. Areas of interest include development of architectural concepts to improve system reliability through fault tolerant or redundant design, concepts of reducing custom fabrication, new IC processing (lithography) techniques and package improvements. The hybrid technology can play

a significant part in this latter area. Approximately 25-30% of the VHSIC effort is budgeted for the Phase III technology support contracts.

Army Systems For VHSIC Implementation

Under the Program Definition Phase approximately 20 different military systems in the categories of communications, radar, missile, acoustic, and electronic warfare, suggested by the three Services, are being addressed by the nine organizations. To insure major impact on military needs, system requirements will drive the technical program developments. Design, architecture and partitioning will directly impact on chip processing and lithography developments for subsystems with diverse applications and for a maximum degree of commonality in each IC design.

The Army suggested a list of four viable applications that were considered most challenging and, as drivers, would insure that VHSIC products evolved would work in the system themselves. If these VHSIC products work in the initial systems, they should cover most of the needs of numerous other military systems that have been analyzed.

One application is the Multi-Mode Fire-And-Forget Missile. An ideal fire-and-forget missile is one that can be fired in the general direction of the battlefield where it will survey the target area, locate and travel to its target, and carry out its function totally on its own. The weapon should have multiple sensors, including thermal, viewing, and millimeter wave, since there are many different countermeasures that can be directed against such a missile. With present packaging constraints, no more than one such sensor can be placed into smaller tactical missiles. Under Phase I, the goal is to determine how much can be incorporated in the given system area while providing a multi-mode capability to allow active and passive sensor elements on a missile. Under Phase II the goal is building a missile which will be totally autonomous in finding its targets and completing the required combat function.

The second area selected was electronic warfare where the monumental problem exists of detecting thousands of targets by sorting and analyzing thousands of signals at millions of pulses per second. The process now uses vans with loads of equipment to do an inadequate job. To do an adequate job, the equipment has to get smaller for mounting in airborne vehicles, be automatic, and interact with weapons systems without going through long complex system chains. Hundreds of MIPS are required in small packages to carry out these functions. The two basic tasks for this area include, therefore, development of a computer capability that will do the job and that will fit into a package that can be used in small vehicles.

The third area is in Communications, one of the weaker links on the battlefield today. Deficiencies of conventional Army communications have become apparent during the past few years in areas relating to real time communications and ECCM. New radio systems must be fully secure and adequately jam-resistant. The radio must interact with hundreds of other radios over tens of kilometers of the battlefield, all netted together in such a way that it

is really one distributed computer system receiving messages and data from one point to another in a totally reliable fashion. Beyond this, each radio may be participating in two or three different kinds of nets (fire control, command and control, ground weapons) which separate from each other. Therefore each radio has to carry out all these functions but do it as if it was several radios incorporated into one, each with its own codes and its own transmission and reception capability. This means literally putting millions of gates into radios, a tremendous problem when we consider the size, weight and power constraints of the Army radios. Here again we have two goals; one is to take all of the known concepts of the Packet Radio System and Position Locating Reporting System and Joint Tactical Information Distribution System (PLRS/JTIDS) and incorporate them in a secure working system with acceptable jam-resistant capability. The second goal is to improve on that performance by a factor of 10 to 100 in terms of the complexity of the codes and the bandwidth required using VHSIC signal processing.

The last application has to do with advanced target acquisition and fire control. The ideal fire control system has a sensor (such as our second generation forward looking infra-red system FLIRS) which scans the battlefield, displays the information relating to multiple targets and other objects of interest, automatically analyzes these items, selects those which are potential targets, prioritizes them, and then directs fire, all without the intervention of the solder. The algorithms exist and these functions can be carried out with large computers today. The problem is that anywhere from 100 to 1000 MIPS could be used to do the job better and more accurately. Fire control has to be done with extreme accuracy because of automatic distinguishing between friend or foe, which means not only identifying a tank but whether it is one of our own. This, of all the applications, will probably bring greater demands than any other. The capability is preferred for a small missile as well as in the tank or helicopter. Therefore there are two goals: One to do the signal processing with a system which can fit into an airborne vehicle such as a helicopter or into a tank, and the second to reduce the size of the system to fit into RPV-sized systems so that the capability can be brought directly into the intense area of the battlefield.

Key Tactical Thrusts

Placing literally hundreds of thousands of gates on a single chip or even on a collection of chips on a high density hybrid substrate creates design problems that transcend anything that a human being had ever hoped to do. A key technical thrust (Table 1) is the ability to structure the architecture and to design that chip so that it is producible, something we simply do not know how to do at the data rates and the processing speeds that we have today. Totally new architectural concepts are needed, hopefully concepts that would allow one circuit to do a multiplicity of functions in many different systems, much as a microprocessor does today. Such functions (Table II) which now require many chips put together are envisioned as being made on single VHSIC chips, with collections of these hopefully being programmable and designed so that they can be used in many different applications. It is recognized that everything cannot be achieved with such a family of chips and therefore

- New system/circuit architecture to permit multiple application and minimize customization.
- Computer aided design and testing of low cost custom VHSIC chips.
- Microfabrication techniques for high density/high speed signal processing devices.
- Develop reliable integrated circuits for military environments.
- VHSIC systems integration.

Table I Key Technical Thrusts

## MULTIPLE APPLICATION INTEGRATED CIRCUITS

| | |
|---|---|
| Viterbi Algorithm | Array Processor |
| Magnituding | Self-Indexing Memory |
| Digital Filtering | Doppler Processing |
| Matrix Multiplication | Linear Predictive Coding |
| Correlator | Transform Encoding |
| Data Sorter | |

Table II Multiplicity of Functions

computer aided designs will be useful at levels well beyond anything that we have today. Designs have advanced from single elements to standard cells and are now rapidly approaching the macro cell designs where whole functions get placed on a chip in sequence and interconnected, and where entire systems can be simu ated.

Approximately 60% of the effort may be expended in the computer design area (Table III). Problems associated with establishing the architectures, designing the devices, developing all the software that is required to design and operate the chips, and finally, the ability to test them to the $10^{11}$ and $10^{13}$ goals indicated above, are about two to four orders of magnitude beyond our present capabilitites in terms of applications to military hardware.

Logistics are a major problem on the battlefield today. We are committing thousands of soldiers simply to maintain the new systems that are presently underway to the battlefield. Hopefully, VHSIC technology, by providing automatic testing and sufficient redundancy, will permit the chips to reconfigure themselves and the system to self-repair. Such features, together with improved reliability and the use of modular concepts (perhaps incorporating with every system that we ship to the battlefield all of those replacement modules that can reasonably be expected to use during its lifetime), will have a major, positive impact on the Army's logistic problem.

Hybrid Packaging Needs

New processes, techniques and equipments will be required to provide for the scaling down of the current configurations to the low micrometer and submicrometer feature sizes required for the higher density and higher speed integrated circuits. Improved lithography equipment including direct electron-beam writing, x-ray system, direct step-on wafer and improved optical projection are being developed. Dry etching and patterning processes including plasma, reactive ion etching and reactive ion milling are replacing wet processing techniques. As the VHSIC chips increase in size and achieve the high circuit density and speed planned, there will be a corresponding demand for improvement in packaging. New approaches will be required to insure that electronic packaging does not become one of the principal factors limiting the utilization of the VHSIC technology. The increasing chip density will result in more pads per chip necessitating an increase in interconnections with the increasing speed necessitating reduction in propagation delays. This will require conductor lines of micrometer dimensions at a very high density necessitating use of photolithographic techniques. In fact, the hybrid technology may have to apply monolithic technology to achieve the fine lines required.

Such techniques, at the narrower linewidths, do not work well on conventional hybrid substrates and therefore the hybrid industry is challenged with coming up with a substrate which will have the capability and the surface on which one can fabricate high densities of lines of narrower dimensions than previously used, in addition to the necessary thermal and mechanical

## LOW COST CUSTOM DESIGN

Computer Aided

- Design
- Architecture
- Software
- Test

} DAST

## SIGNAL PROCESSING THROUGHPUT

Completion of Phase I $10^{11}$ gates x speed (1.25 micrometer)

Completion of Phase II $10^{13}$ gates x speed (0.5 micrometer)

Table III Computer Design Area

characteristics. There will be need for adequate heat dissipation of the thermal load from the chip, proper thermal expansion compatibility between the chip and the substrate, new bonding techniques, provision for increase in pin counts along with the fine line capabilities for high density interconnections between chips, and design control of the interconnections to insure minimum signal degradation as clock speeds increase.

## Conclusions

The Tri-Service VHSIC program is intended to aid DOD in meeting its future objective in high speed, high throughput signal and data processing in support of the requirements for military systems in the mid-eighties and beyond. Major problems in the VHSIC implementation include new architectural concepts, partitioning of functions and provisions for increased testability. To realize the VHSIC potential, solutions must be found to the problems associated with scaling down the IC's including new lithography and etching techniques and equipments. New approaches to packaging are required to keep pace with the new higher density and higher speed integrated circuit technology representing a challenge to the hybrid microcircuit fabricators.

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# 15 YEARS OF HYBRID PRODUCTION - PROBLEMS AND SOLUTIONS

BY

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## ABSTRACT

This paper is intended as a historical review of a variety of problems encountered during the initiation and growth of a hybrid production facility starting in 1964. The solutions to early problems in the area of first electrical test yields are discussed. Data obtained regarding wire bond behavior with various metallurgical systems is presented.

## BACKGROUND

The following background information is presented so that the nature of the facility and its processes can be better understood. The production rate history of the facility has shown fairly steady growth since 1964 with the exception of a severe transient in 1969. This growth expressed as units shipped per month is shown in Figure 1. The total number of hybrids represented in this curve is about 1.5 million.

During this 15 year period the semiconductor components evolved from SSI complexity in 1964, to MSI in 1970, to LSI in 1974, and more recently to VSLI. Hybrid complexity has grown to keep pace. The 1964 hybrid design was a 3/4" x 1" unit with about 50 part numbers with an average die count of 25. There were no suitable cases available in 1964 so the case consisted of the hybrid substrate with a seal area around the perimeter for a solder sealed shaped cover. The 36 exit leads were brought through holes in the ceramic. This hybrid package type is still in use today on a few older programs but is gradually phasing out. A variety of military grade Kovar-glass bead packages were available in the 1970 time frame and these have been used since that time. The size of packages has grown and 2" x 2" hybrids are quite common, with the largest hybrid size reaching 3½" x 3½".

The evolution of fabrication processes at Teledyne during this time period is shown in Figure 2. In 1964 the thick film inks for the screen and fire substrate processes were not capable of producing complex 1" x 3/4" substrates with the 7 mil line width and 7 mil spacing required by the layouts. Therefore, a subtractive thick film process was developed using a solid moly-manganese coating on the ceramic with electroplated gold stripes for the conductor pattern. The gold stripes acted as a resist for the etch process which removed unwanted moly. The need for precision resistors for analogue circuits brought about the development and introduction of an evaporated nichrome-gold thin film substrate process in 1965.

The modern high conductivity noble metal thick film inks became available in 1969 and were capable of 7 mil x 7 mil resolution. A screen and fire thick film process was therefore developed and qualified for military use and went on line in 1970. The emergence and growing use of MSI complexity dice with increasing numbers of bonding pads resulted in a thick film multilayer process being developed simultaneously. This multilayer feature has been used in almost all hybrids since that time.

The first electrical test yield is a very important factor in a hybrid production operation and will be discussed later in this paper. Poor yields in the early years resulted in the development and implementation of a facility to electrically test bare integrated circuit chips. This activity was started in 1966 and has continued to the present time.

A low temperature solder system was developed for component attach and the final form was a silver-tin eutectic solder in a screenable medium. The material is screened on the substrate with a printer which gave accurate placement of the preform and an accurately controlled amount. The dice were pressed into the solder paste positions with a pick and place machine and run through a thermal profile in a conveyor furnace, which fused the solder and attached all dice simultaneously. Organic polymers such as epoxies were avoided initially because of concerns over outgassing. However, a thorough study was completed in 1972 and epoxy was qualified for use on a space program. The data was sufficiently good that all programs were converted.

Ultrasonic aluminum wire bonding was selected for hybrid fabrication at the startup of production and is still the major technology. The choice was motivated in 1964 by the fresh memory in the industry of the purple plague phenomenon. A monometallic weld at the die pad removes this possibility but introduces an intermetallic growth problem at the weld to the gold substrate. However this has been a controllable situation as will be discussed later.

Gold wire thermosonic bond eliminated certain disadvantages of TC bonding by requiring a lower temperature and by providing the ultrasonic scrubbing action to eliminate the problem of minor surface impurities. This process was introduced in 1976 and has progressed to automatic wire bonding for which it is ideally suited.

Cover seal is also a critical hybrid process in providing the suitable inert dry atmosphere necessary for long term reliability. The 1964 hybrid required a solder seal due to its inherent design. The first process attempted was a perimeter sealer. A lead-tin-silver preform was used without flux. The results were erratic with some days providing good yields and some days giving poor yields. No amount of engineer effort appeared to alter this performance and the system was abandoned in favor of an inert atmosphere conveyor furnace in 1967. This gave more consistent results.

The seam welding process was introduced in 1971 and has provided the highest hermeticity yield and the strongest seal of any process investigated. It is the preferred process at this time and new programs all use this approach. The importance of water vapor content was recognized early in the program and vacuum bakeout in the cover seal process was introduced in 1968. This took the form of a two door vacuum oven. The parts entered the front door, dwelled in vacuum at 150°C for 1 hour and then were removed through the other door to the sealing process without exposure to room atmosphere. The water vapor content in the sealing chambers is continuously monitored with suitable equipment.

## FIRST ELECTRICAL TEST YIELD

As mentioned previously, one figure of merit for a hybrid production facility is first electrical test yield. The history of this factor experienced by Teledyne Microelectronics is shown in Figure 3. The very low values in the early years were in general due to lack of experience with hybrid technology and the relatively primitive state of development of the integrated circuits at that time. They were custom SSI devices and were the first epitaxial devices produced by the vendor, the first TTL design, and the lowest power TTL(2.5 milliwatts per gate) produced at that time. An analysis of the specific reasons for the low yields in 1966 revealed the following factors:

1. Electrically defective dice.
2. Dice handling damage.
3. Component errors.
4. Wiring errors.
5. Hybrid handling damage.

The solution to the electrically defective dice was to develop and introduce a 100% production test of bare chips before release to hybrid fabrication. This is described in detail in Reference 1. It basically involved the design of a contact probe to engage the dice pads and a test machine to provide for operator manipulation of the probe assembly. The key features of the probe design were to use blunt contacts to avoid pad damage and exposure of oxide and to provide a controlled burnishing action to break through the oxide coating on the aluminum pads to provide good electrical contact. The probe setup before testing is critical and all probe contacts must touch the die simultaneously, and be centered on the pad area so that no burnish motion goes off the edge. Although it is a manual operation, an average operator can test about 1200 dice per shift and some do considerably more. Initially all dice were tested at 25°C, +125°C, and psuedo cold. However, as semiconductor technology has progressed this is no longer necessary. Mature product lines such as 5400 series and 5400L are sampled on a 1% AQL basis to guard against bad lots. MOS devices are tested only at elevated temperature. 100% testing is only done on complex devices such as memory dice where the need is definite. Also, if yield problems develop at first electrical test due to a die problem, 100% testing can be immediately reinstituted.

The burnish marks on the dice pads due to probing have sometimes been alleged to constitute pad damage that might be deleterious to wire bonds. This question was raised very early in the dice testing activity in relation to hybrids for a NASA space program. Accordingly, a test plan was devised to make several hundred aluminum ultrasonic bonds to probed dice pads, half of which were deliberately made directly on the probe marks and half definitely away from the probe marks. The testing involved destructive pull testing coupled with 150°C thermal exposure and thermal cycling. As with all monometallic welds, the pull strength tended to increase with temperature exposure, but the average pull strength of the bonds made to burnish marks was significantly higher than the others. This might be explained by the burnish action removing surface contaminants such as oxides and exposing purer aluminum for a better bond. There never has been a bond failure related to this.

The die handling damage contribution was caused primarily by the shipping method for bare dice that was prevalent at that time. The only way semiconductor manufacturers would ship integrated circuit dice was many hundreds in a beaker imbedded in paraffin wax. This was a very safe shipping method but the problems at the receiving end in removing from the beaker and totally dewaxing the dice were severe particularly since the dice were not glassivated. Soxhlet extractors were used but dice sticking together would result in thin wax residues that would interfere with wire bonding. The solution was to design and tool a 400 cavity waffle pack using die cast aluminum technology. The cavities were coated with a thin layer of an RTV silicon rubber to protect the dice and an antistatic glass cover completed the cavity. Initially the semiconductor suppliers would not ship in this carrier except at Teledyne risk. Eventually it became accepted and was supplied to all vendors. Dice damage was insignificant particularly after the cavity coating was changed to teflon to avoid silicon particles imbedding in the softer RTV coating. Eventually this waffle pack concept became commercially available in a plastic form and is in standard use today. Another factor in eliminating dice handling damage was the development of a better tip material for vacuum pickup probes and the operator training not to touch the dice with the probe but to cause the dice to be drawn up to the probe.

The solution for component errors had to overcome the problem of the wrong dice in a position or wrong orientation. This was solved by a prekitting scheme that created a nesting fixture made by etching cavities in copper clad P.C. board material. The substrate dice pad artwork was used so the nest cavities were in the exact format of the dice on the substrate. The nest was loaded at a kitting station with the right dice in the right position and in the proper orientation. It was then inspected to verify that this was so. A pick and place machine was designed and built with the feature that once a die was picked from the nest, it automatically was placed in the proper location on the substrate and in the proper orientation. Before entering the process, the substrate was prescreened with tin silver eutectic paste at the dice locations. The pick and place machine seated the

dice in the preform material with the proper gram force and they were held in place by the material until they were passed through a conveyor furnace which completed the process. The proliferation of hybrid part numbers to about 400 in recent years has made this approach too expensive and it is no longer used. Better operator training and more sophisticated line aids now handle the problem.

The solution to the wiring error problem had to overcome the fact that it is difficult for a bonding operator to relate a magnified view of a portion of a hybrid seen through a microscope to a separate overall wiring drawing. At first attempts were made to inject the wiring pattern optically into the microscope, but was unsuccessful. The solution was to place the wiring pattern on the substrate with a permanent material that could not introduce deleterious chemical effects. Since the substrates at that time used molybdenum technology, firing in an oxidizing atmosphere was not permissible. Therefore, an ink was developed based on a borosilicate glass with chromium oxide coloring material which could be fired in a reducing atmosphere. The wiring diagram was stenciled on the substrate producing a 3 mil line wherever a bonding wire was to be placed. This was very successful in reducing wiring errors. With the advent of multilevel thick film technology in 1970 this became unnecessary because the artwork provided a substrate bonding pad immediately adjacent to each die bonding pad and all jumpers were eliminated. For any single level substrate the wiring pattern is still added using a conventional thick film overglaze material. However, in spite of all the above, on the average about 5% of complex hybrids will have a missing wire or a miswire. It is too expensive to detect this with the electrical test of the hybrid so a projection comparator inspection is used. This projects side by side a small area of the substrate just wired and the same area of a known perfectly wired substrate.

Hybrid handling damage is a severe problem. They are difficult to pick up and handle without damaging wire bonds. To solve this for the 1964 hybrid a carrier was developed to grip the external leads and provide a pickup frame so the hybrid is not touched. As package types have proliferated the problems become more varied. Platform packages without side walls present the worst problem. Side wall packages are least troublesome and every effort is made to convince customers to use the side wall platform, or "uniwall" as it is called, if a plug-in design is specified.

The result of all these actions was the increase in first electrical test yield shown in Figure 3.

## WIRE BOND INTEGRITY

The next subject to attract concerted attention was hybrid failures after delivery to the system customer. By 1967 a solid body of data was available and when analyzed yielded the following picture. The data emerged from system integration and system test.

1. The predominant failure mode was wire bonds.
2. There were over 100,000 bonds per system.
3. Esentially all failures were substrate bonds.
4. Systems test involved long temperature exposures and many thermal cycles.

The field experience after systems delivery showed relatively little problem with wire bond failures. This seemed to indicate that the problem was screenable and that Item 4 above might indicate that temperature exposure and thermal cycling might be useful screens. MIL-STD-883 did not exist at this time and only minor screening was being done, such as 168 hours burn-in at 100°C. It was also evident that large samples of bonds would have to be used to determine any effects of screens since the system problem became evident with effectively a 100,000 bond lot. It was also evident that the substrate bonds were the major problem, probably because of their bi-metallic nature.

The first step was to design a substrate test pattern consisting of a series of rectangular stripes that could be wire bonded to form a series circuit with 200 wires and 400 bonds. These were evaluated in lots of 25 substrates and thus 10,000 bonds. At least 10 different lots were used giving total test samples of 100,000 bonds to detect lot to lot differences. The 10,000 bond lots were exposed to the thermal cycling consisting of a sequence of 20 minutes at 150°C, 3 seconds transfer to -65°C, 20 minutes at -65°C, etc., out to 1,000 such cycles. It was found that the cycling produced very few failures as detected by resistance measurements on the substrate unless mechanical shock was introduced at each test time. The resulting data is shown in Figure 4 and is the average of 10 lots of 10,000 bonds each. Incidentally, 20,000 G centrifuge did not produce the detectable failures as did mechanical shock. The first 25 cycles produced most of the failures. The few failures at 600 cycles and beyond were always wire heel breaks caused by fatigue due to thermal expansion differences between the aluminum wire and alumina substrate. As a result of this data, thermal shock followed by mechanical shock was introduced as a 100% screen on all hybrids. The screen used 22 cycles of the thermal cycling sequence to achieve a 12 hour time duration which is easier to manage on a production basis than a time not related to a day or one-half day.

A second series of tests were conducted using 150°C temperature exposure for 1000 hours as the stimulus. Again mechanical shock was found necessary to produce the failures. The results are shown in Figure 5 and indicate that all failures were produced in the first 75 hours. As a result of this data, an exposure of 72 hours to 150°C was introduced on a 100% basis for all hybrids. The 72 hours was chosen because that duration is 3 days and easy to manage in production.

The 1967 screening sequence became:

1. 72 hours at 150°C.
2. 22 thermal cycles, -65°C to +150°C.
3. 5 mechanical shocks 1500 Gs, ½ m/s

The result of these screens was a dramatic reduction in wire bond failures after hybrid shipment. However, attempts to understand the basic reasons for the infant mortality effects shown in Figures 4 and 5 were never successful. Subsequent tests showed that the temperature and thermal cycling screens appeared to be redundant from a wire bond standpoint, since whichever was done first effectively eliminated the failures in the second. However both were retained.

The initial work on thick film substrates in 1969 led to a program to duplicate the tests described above to obtain knowledge of aluminum wire bond behavior on this material. The same test procedures and test substrate patterns were used. The data from thermal cycling is shown in Figure 6. As the test progressed it at first appeared that thick film was the perfect answer to wire bond problems. In fact a pilot run was started on one part number to obtain direct production experience. After 500 thermal cycles the failures began occurring at an increasing rate on the bond samples and the behavior of 150°C test samples showed the same pattern. The actual hybrids that were built started showing electrical failures after a few hundred hours at 150°C even though the bond pull test results were satisfactory. Investigation showed that some bonds were developing fairly high resistance and causing electrical parametric failures of the hybrid. More bond test samples were made and electrical resistance of bonds was monitored during 150°C exposure. The results are shown in Figure 7. The data is difficult to plot because of the wide variation of the resistance change. The increase in resistance can usually be detected by the 100 hour point but bond to bond variation is very large. A current or voltage pulse can restore the original low resistance value, but it soon rises again. Normal bond resistance is in the order of 1 milliohm not including wire resistance. At 500 hours the variation is huge as shown by the spread bar in the curve, but as shown previously, bond strength is not degrading seriously during this 500 hour time frame. Bond cross sections and SEM analysis of the defective bonds were not too conclusive but did seem to indicate some form of intermetallic growth problem. Microcracks could be found with SEM analysis which probably explains the apparent bond resistance increase. Several papers were published during the 1970's on the same basic problem (references 2, 3 and 4). It was intuitively decided to investigate the addition of palladium to the gold ink simply on the basis that it might slow the diffusion of gold into the gold-aluminum intermetallic growth in the bond area. The sample inks were formulated internally simply by mixing various ratios of Alloys Unlimited C7000 composition, which was gold-20% palladium, with Englehard 1560 which was pure gold. Mixtures containing above 5% palladium proved to have unsatisfactory initial bonding performance while very low additions did not have any effect on bond performance. At about 2% palladium content the results were

impressive and aluminum wire bonds could survive 1000 hours at 150°C without resistance growth or bond strength degradation. The same is true for the 1000 thermal cycle test. There was no R & D capability to find exactly what was happening metallurgically, but enough qualification test data was obtained to go to production with the 2% formulation for the top level of the multi-level thick film structures.

The screening and evaluation procedures used for Figures 4, 5 and 6 were no longer valid since they did not produce failures. Therefore, the procedure was changed to do destructive bond pull test on a randomly selected group of bonds on the test sample at every test point. Figure 8 shows such a curve for a bond lot test at 200°C for 1000 hours with the top circuit ink. 200°C is shown since it demonstrates some bond lifts and some wire breaks, which are really heel breaks. At 150°C they would normally all be wire breaks. The shape of the curve was puzzling at first but is clarified by Figure 9 which is the break strength of 1 mil aluminum wire versus time at 150°C. It shows that the wire, which is used in a work hardened condition due to drawing, actually anneals at 150°C. If all the test points in a curve such as Figure 8 were wire breaks it would simply mean that the bond strengths were greater by some unknown amount than the wire in the bond heels. If the test shown in Figure 8 were conducted with normal gold thick film ink, zero bond strengths would occur after several hundred hours.

At first this 2% palladium composition was treated as the only proprietary thing in the factory. However, mixing the formulation for production use became tedious and an attempt was made to buy it. A gold-2% palladium ink was ordered from Englehard and delivered. Analysis showed it did contain 2% palladium as specified but showed no benefits for aluminum wire bonding. After several tries and different lots the attempt was abandoned. This showed that there are more factors involved than simply 2% palladium. Much more recently another attempt was made by ordering the ink from DuPont, with exactly the same results - no effect on aluminum wire bonding. However DuPont became interested in the problem and did the necessary R & D investigation to determine the role of palladium and published the results (reference 5). It appears that the palladium does not enter the gold-aluminum intermetallic reaction and instead is pushed ahead of the growth much as in zone refining, and gradually reaches a concentration that prevents the gold from entering the reaction, thus slowing or stopping it. However, many other factors must be just right for this to happen. Alloy inks suitable for aluminum wire bonding are now commercially available from DuPont as 4119 and from ESL as 8882. They are more complex than simple palladium addition and are semi-fritted perhaps with multiple additions of elements.

As a result of the above studies any contemplated metallurgical changes in the bonding system is studied thoroughly with at least ten 10,000 bond lots using the 150°C and thermal cycle study with pull test curves similar to Figure 8 before introduction to production. The bonds for the test substrates are made by a variety of production personnel on production machines.

In addition a sample is taken from each production substrate lot for bond evaluation before release to stores.

An example dictating the need for caution occurred in 1975 when the first silver-1% platinum inks were evaluated for production use. A preliminary engineering lot of 10,000 bonds produced excellent results both at 150°C for 1000 hours and through 1000 thermal cycles. A small pilot run of an actual hybrid was made to evaluate production performance. However, the results were very poor with both lifting wire bonds and resistive bonds. The performance proved to be related to time between the completion of substrate fabrication and wire bonding. Figure 10 shows the results obtained by storing test substrates for various lengths of time before wire bonding. In each case the substrates were stored wrapped in so-called "silver saver" paper which is supposed to prevent silver tarnish due to sulfur. The results show that beyond 7 days in storage severe degradation occurs in bond performance and evidenced by bond lifts and resistance. The silver-1% platinum was never used in production. The failure mode was somehow related to the tendency of silver to pickup sulfur as shown by electron microprobe analysis which is always present to some extent in room atmospheres.(Reference 6.)

## HYBRID WATER VAPOR CONTENT

There has been increasing concern in recent years regarding water vapor content in hybrid packages. As noted previously, vacuum bake-out integral with the sealing chamber was introduced at Teledyne as early as 1968. Out of the 1.5 million hybrids shipped, only about 2 dozen have experienced failures identified as moisture related. In each case the failure mode was the disappearing nichrome resistor phenomenon which is caused by condensation at the dew point of the package atmosphere. All but 7 of these failures were traced to the inadvertent omission of the proper vacuum bake-out procedure. However customer pressure began mounting through specification requirements to extend the vacuum bake-out from 1 hour to 24 hours. A vacuum bake-out integral with the sealing chamber for this duration does not appear practical for a production operation. Various approaches to evolve equipment designs to allow this were investigated but no viable scheme evolved. The question of a separate bake-out chamber was evaluated. The problem to be considered is that water vapor could reattach to the surfaces during transfer in room air. A concept was explored that envisioned there might be two water vapor problems to contend with. One might be deep seated water in organic materials such as epoxies which might be difficult to remove. The other might be surface adhered and relatively easy to eliminate. The plan was to use a long time duration bake in a separate chamber to remove both surface adhered moisture and deep seated moisture.

This would be followed by a limited transfer time period (5 minutes) to the regular vacuum bake-out system integral with the sealing chamber. Some surface moisture would probably re-adhere during this transfer but the 1 hour vacuum bake-out at 150°C should remove it. An additional concept was that the long term bake-out could be done in any very dry atmosphere such as

nitrogen and per Dalton's Law of Partial Pressures it should be just as effective as vacuum. An experimental program was carried out in 1976 to verify the concepts discussed above. The results are shown in Figure 11. A group of complex hybrids that used epoxy component attach and epoxy substrate to case attach were selected for the test. All were soaked in DI water for 3 minutes to present a worst case water absorption situation, and then were exposed to a brief isopropanol rinse to remove excess water. One unit went directly to cover seal without any type of bake-out. Five units were subjected to a 24 hour 150°C bake-out in a dry nitrogen oven with sufficient flow rate to maintain less than 50 ppm water vapor content. The units were transferred to the vacuum bake-out oven in less than 5 minutes. The results of RGA with mass spectrometer analysis at 100°C is shown in Figure 11. This procedure has been implemented on some programs and results continue to be favorable.

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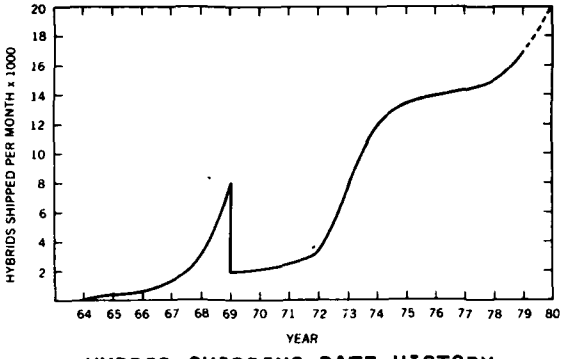
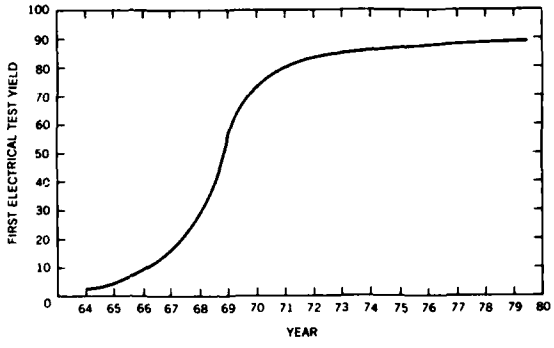


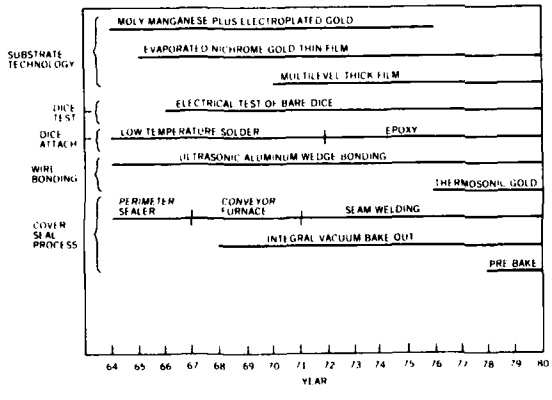

HYBRID SHIPPING RATE HISTORY

FIGURE 1



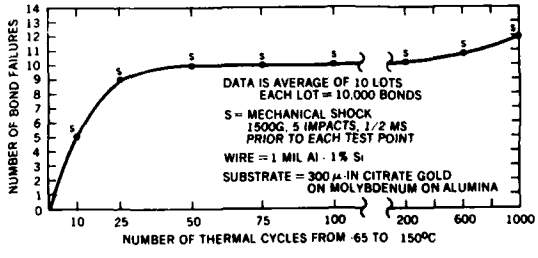

HYBRID YIELD AT
FIRST ELECTRICAL TEST

FIGURE 3



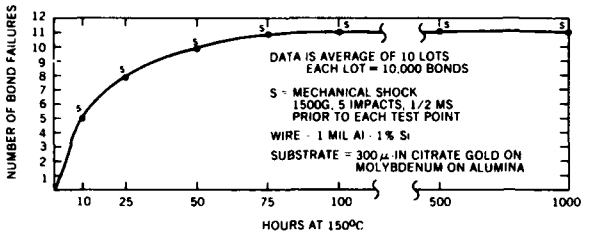

HISTORY OF HYBRID
FABRICATION PROCESSES

FIGURE 2



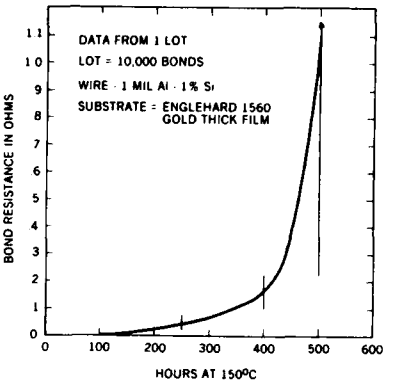

BOND FAILURES PRODUCED BY
THERMAL CYCLING AND
MECHANICAL SHOCK

FIGURE 4



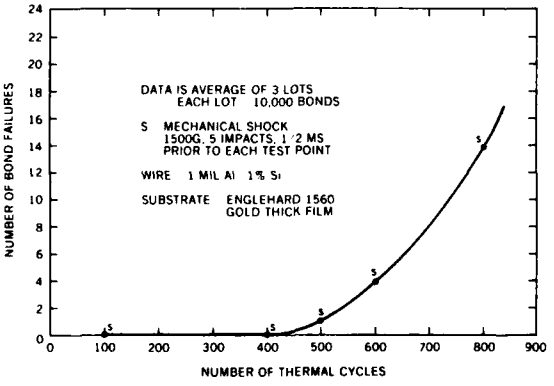

BOND FAILURES PRODUCED BY 150°C EXPOSURE AND MECHANICAL SHOCK

FIGURE 5



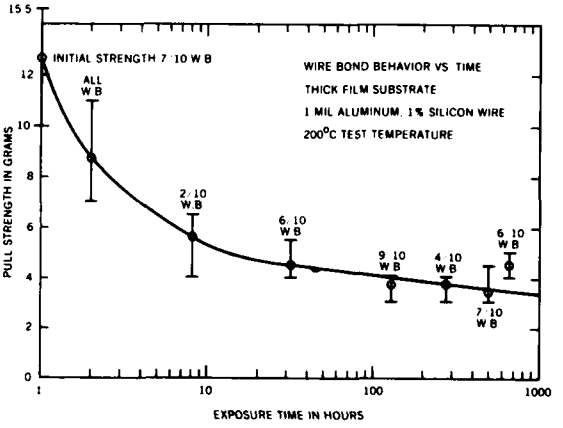

ELECTRICAL RESISTANCE BEHAVIOR OF ALUMINUM BONDS ON THICK FILM GOLD

FIGURE 7



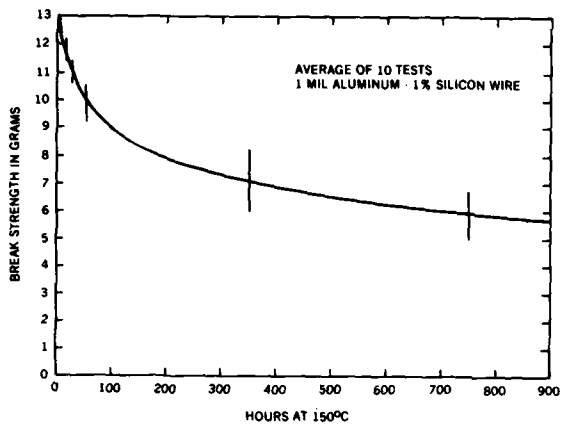

THICK FILM BOND FAILURES DURING THERMAL CYCLING

FIGURE 6



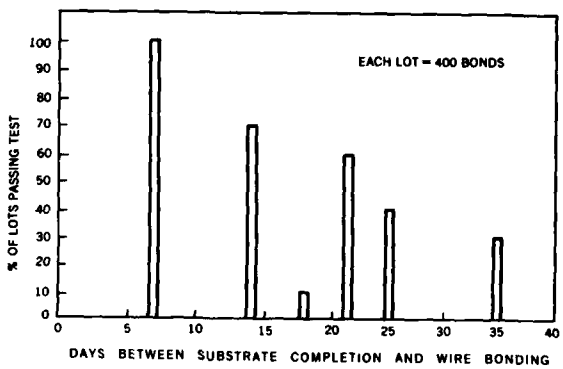

BOND STRENGTH BEHAVIOR OF ALUMINUM BONDS ON GOLD-2% PALLADIUM THICK FILM

FIGURE 8



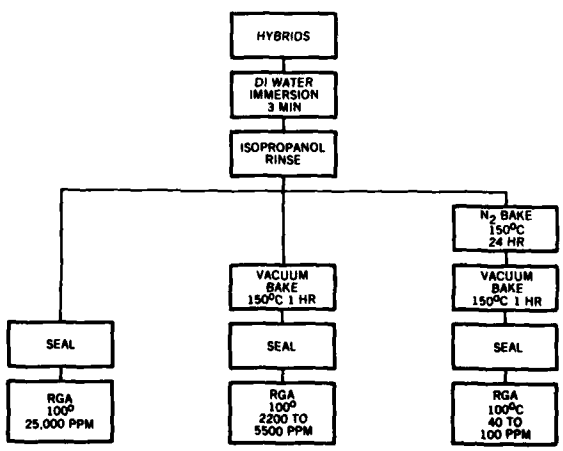

BREAK STRENGTH OF 1 MIL ALUMINUM WIRE ANNEALED AT 150°C

FIGURE 9




BEHAVIOR OF WIRE BONDS ON SILVER-1% PLATINUM THICK FILM

FIGURE 10




EFFECTS OF PRE-BAKE ON WATER VAPOR CONTENT OF HYBRID PACKAGES

FIGURE 11

# HYBRID MICROCIRCUITS IN THE PATRIOT SYSTEM FROM THE DRAWING BOARD TO THE FACTORY

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## ABSTRACT

A set of high density analog and digital hybrid microcircuits developed for the PATRIOT System will be discussed. These hybrids provide architectural building blocks for a wide range of analog and digital functions for aerospace applications. An order of magnitude increase in density and reliability has been achieved over conventional integrated circuit packaging techniques. The analog hybrids use leadless, hermetically sealed active devices which are precursors of todays hermetic chip carriers for IC applications. The digital hybrids (RAYPAKs) were designed using up to 6 beam-leaded, 60 gate TTL arrays attached to a thick film ceramic multilayer interconnection network. They provided high density modules at a time when only Medium Scale Integration (MSI) ICs were available, thereby facilitating high technology insertion, namely the replacement of hybrids by Large Scale Integration (LSI), without requiring system repartitioning at the module level. This paper reviews the various aspects of the hybrid circuit technology employed in the PATRIOT system such as design, reliability, processing and the insertion of technology improvements.

## INTRODUCTION

The PATRIOT Army air defense system is a ground-to-air missile system. It employs a missile with an advanced semiactive radar seeker. On the ground a mobile multimode phase array radar provides a wide range of target acquisition and tracking capabilities under adverse Electronic Countermeasures (ECM) conditions.

This paper covers the various aspects of the hybrid circuit technology used in the PATRIOT ground equipment.

The hybrid circuit technology approach selected fulfills the following requirements:

1) It is based on well proven device concepts and fabrication processes to minimize development risk.

2) It is in the mainstream of technological trends to facilitate second sourcing.

3) It employs a high degree of commonality in manufacturing processes.

4) It permits successful upgrading of the system to more advanced technologies, as these were maturing during the development cycle.

These goals have been realized by using a standard module set of analog and digital modules. The modules make extensive use of hybrid circuits. To increase yield, the analog hybrids use solder attached hermetically sealed leadless active devices on thick film substrates. PATRIOT probably was the first major system to use hermetically sealed transistor devices in leadless packages, a precursor of today's leadless hermetic chip carrier integrated circuit packages.

The digital logic circuits were predominantly beam-leaded, 60 gate Transistor-Transistor Logic (TTL) arrays. This technology corresponds to state-of-the-art semiconductor technology of the early seventies. The 60 gate arrays (chips) were packaged in Multilayer thick film hybrids, each hybrid containing up to six 60-gate arrays. A cover was polymer sealed to the substrate to eliminate the cost of a separate package.

It should be noted that the development span for complex missile systems is in the order of 10 years. Therefore, the original design must be configured to accept technology improvements with minimum design change, especially since semiconductor technology has doubled in performance and integration level every two to three years. As a consequence, the digital hybrid circuits have been made obsolete by more recent monolithic developments toward LSI.

In a technology insertion program, each digital hybrid has been replaced by a customized monolithic 300 gate TTL array in a flatpack. This yields a cost saving to the Government of many million dollars. Due to the initial use of high density hybrid circuits, the design change was restricted to the module level. The newer 300 gate array modules are form, fit and function replaceable with the obsolete RAYPAK hybrid modules.

The ground equipment employs a mobile multiphased-array radar of sophisticated target acquisition and tracking capabilities under adverse ECM conditions. Figure 1 portrays the scheme of operation of the fire control unit and shows the principal functions of each major item.

The PATRIOT ground equipment requires the use of a wide variety of analog and digital subsystems such as transmitters, receivers, filters, beam steering computers, signal processors, control computers, communication systems, etc. To reduce life cycle cost, all these diverse subsystems are based, to a great extent, on a single set of standard modules comprising both digital and analog functions. This module standardization program

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# PATRIOT SYSTEM OPERATION

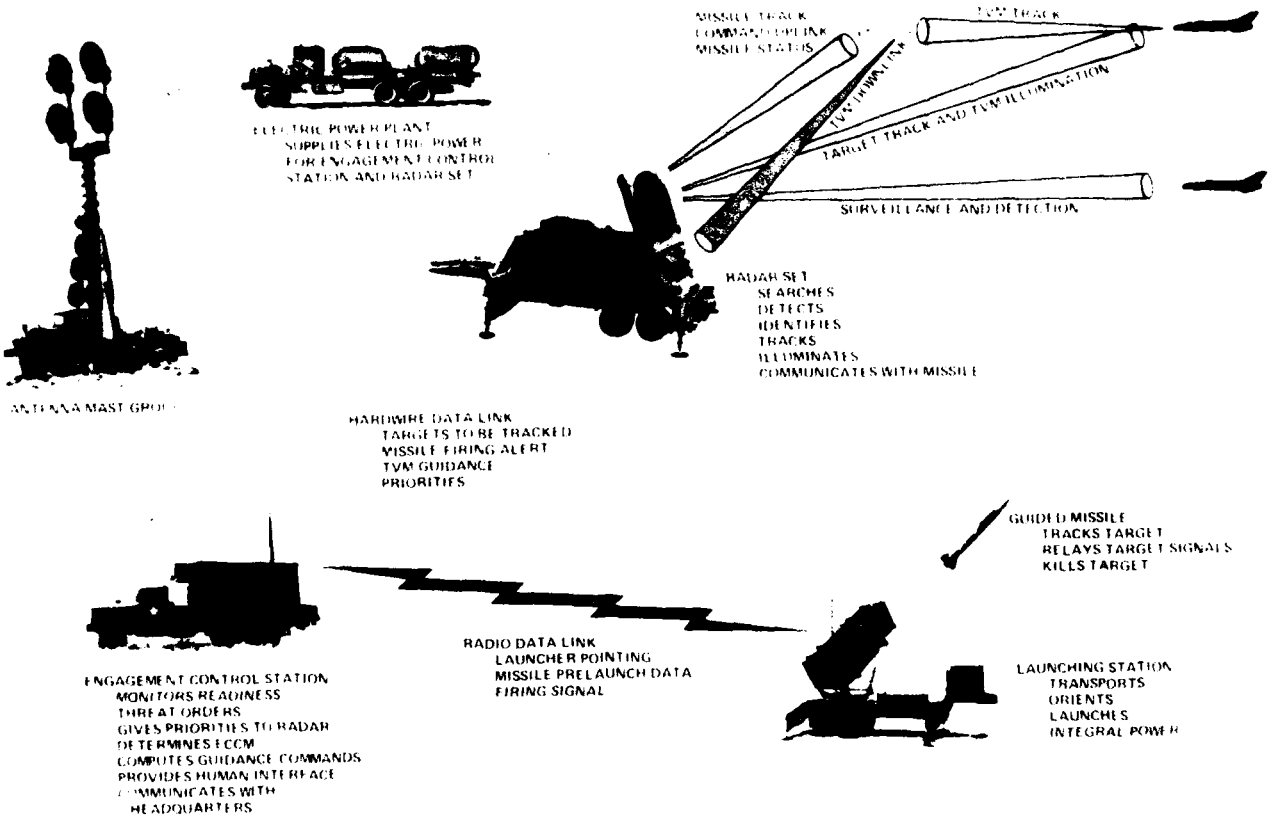


Figure 1 - PATRIOT System Operation

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probably represents a first for a major military system and has been made possible by a number of technical advances:

1) the subsystems have been modularized as much as possible;

2) through implementation in high density microelectronics each standard module represents a subsystem of significant functional capability;

3) the structure of PATRIOT is essentially digital and is thus amenable to a highly regular architecture.

In designing a standard module set, minimum hardware implementation and optimum performance must be somewhat compromised to obtain functions that are widely usable through all the subsystems. Experience at Raytheon has shown, however, that these tradeoffs can be obtained at a very modest penalty (in the order of 10 percent additional hardware and essentially no degradation in performance).

This penalty is far overshadowed by the benefits of functional module commonality which significantly reduces design, manufacturing and life cycle costs.

In addition to standardizing module functions, one single module size and construction serves for all analog modules and a similar one for all digital modules. Mechanically, both digital and analog modules are designed to be mixed on the same chassis without loss of packaging volume due to differences in module size. In addition to standardizing at the module level, standardization was also employed in the design of the hybrid microcircuits that populate the standard modules.

Examples of the hybrid circuit standardization are:

- Limiting the substrate areas to two sizes.
- Locating VCC and ground pins at standard positions.
- Standardizing on a small family of active device types.
- Widening the specification limits of functional analog hybrids to minimize the need for additional functional types.

The manufacturing benefits which accrued from the Standardization Program are as follows:

1) lower unit cost and life cycle costs by creation of a large manufacturing base through commonality of parts;

2) uniformity of manufacturing, test and inspection processes;

3) minimum amount of required tooling;

4) simplified learning process for production workers due to use of standard techniques;

5) use of standard computer-aided automation techniques in design and fabrication.

Naturally, not all the required electronic functions can be satisfied by a single set of standard modules, but Table 1 shows that the utilization is extremely high. Even nonstandard modules use the same construction and form factor as the standard modules.

It is beyond the scope of this paper to discuss in detail the development of the analog and digital standard module set. They are listed in Tables 2 and 3. It should be noted that in the digital set the average gate complexity is 1300 gates, which approximates the complexity of small computers.

Table 1

Significant Standardization Achievements

| | | |
|---|---|---|
| Std. Digital Modules | 22 types | 79 percent of the system's digital module requirements. |
| Std. Analog Module | 22 types | 65 percent of the system's analog module requirements. |

Table 2

Description of

STANDARD DIGITAL MODULES

| Number | Module Function | *Redesigned for 300 Gate Arrays | Quantity Used |
|---|---|---|---|
| 1 | Digital Data Coupler | X | 26 |
| 2 | ADDER | X | 32 |
| 3 | General Purpose Arithmetic | X | 6 |
| 4 | Priority Sequence | X | 6 |
| 5 | Register | X | 8 |
| 6 | D Flip-Flop | | 12 |
| 7 | Registor Shift Barrel | X | 5 |
| 8 | FETCH | X | 9 |
| 9 | Digital Clock Pulse Generator | X | 7 |
| 10 | Word Selector-Delay Line | X | 52 |
| 11 | Input-Output Control | X | 33 |
| 12 | Digital Multiplexer | X | 55 |
| 13 | Scaler Module | X | 7 |
| 14 | Digital Data Receiver/Transmitter | | 90 |
| 15 | Party Line Driver | | 9 |
| 16 | Random Access Memory | | 54 |
| 17 | Monolithic Memory Store-up | | 26 |
| 18 | Monolithic Memory Error Correct | | 2 |
| 19 | Monolithic Memory Control Logic | | 13 |
| 20 | Monolithic Memory Increment-Decrement | | 2 |
| 21 | Monolithic Memory Driver Receiver | | 6 |
| 22 | Power Converter | | 1 |
| | | TOTAL | 461 |

* 3 other non-standard modules-not shown here were redesigned

## PATRIOT ANALOG STANDARDIZATION

PATRIOT Analog standardization uses the building block approach to systems design. Standard analog circuit subfunctions are fabricated in hybrid form. Only two sizes are used to reduce manufacturing and test costs - 1 X (1.15 inches square) and 2 X size (1.15 inches X 2.4 inches). A list of the hybrid functions is shown in Table 3. The hybrid functions have been designed for versatility and compatibility when interconnected on standard analog modules to perform more complex functions. (Table 4).

The module design must satisfy system wide PATRIOT analog applications from low level video and communication signals to high frequency RF receiver signals that require transmission line interconnects. The 164 pin connector, by use of a novel technique, is capable of passing high frequency signals with adequate noise immunity, low VSWR and at 50 Ω impedance. A hexagonal cluster of six ground pins (see Figure 2) surrounds the high frequency signal contact, thus simulating a coaxial line. Figure 3 shows a typical standard analog module. It contains a multilayer PC board, hybrid subfunctions, a frame and the 164 pin connector. The picture illustrates how the two standard size hybrids (1 X, 2 X) mix on the PC board to fully utilize the packaging area. A single analog hybrid circuit is depicted in Figure 4.

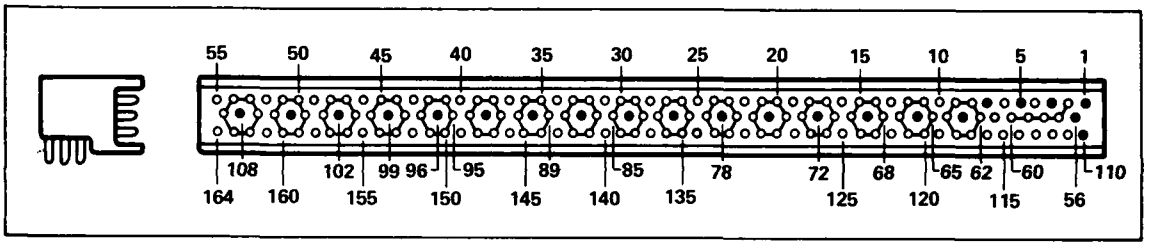



Figure 2 - Schematic of Coaxial Cluster Module Connector

TABLE 3
DESCRIPTION OF
ANALOG HYBRID MICROCIRCUITS

| Description | Key Features |
|---|---|
| 1. Amplifier, RF, Wide Band/8DBM | Basic stage wideband RF, IF amplifier for pulse amplification |
| 2. RF Limiter | 3 stage current limited, emitter coupler clipper |
| 3. RF Electronic Switch | High speed single pole, single throw solid state switch |
| 4. DC Amplifier | Very wideband DC amplifier with low noise & hi slew rate |
| 5. DC Electronic Switch | Single pole/single throw electronic switch |
| 6. High speed electronic switch | Wideband single pole, single throw switch, with match 50 Ω Imp. |
| 7. RF Attenuator-Multi/buffer | RF ladder network and buffer stage controlled by digital input from item 6 |
| 8. RF Attenuator-Multi-stage/ Digital | Enables variable attenuation of RF signals by means of a digital control signal |
| 9. Log amplifier wideband/video | Generates a detected and filtered video output voltage |
| 10. Log Amplifier wideband/RF | Wideband RF amplifier tailored to be used with item 9 |
| 11. Detector RF | A half wave rectifier or peak detector |
| 12. Video Amplifier, Follow-hold/A | Holds instantaneous voltage of an input signal upon receipt of sampling pulse-input amplifier section |
| 13. Video Amplifier, Follow-hold/B | Provides follow & hold for item 12 |
| 14. Integrator-A | Provides transfer function $\frac{Eo}{Ein} = \frac{1}{\tau s}$ |
| 15. Integrator-B | Part of item 15 |
| 16. +20dBm-R.F.Amplifier | 3 stage amplifier-provides necessary gain to meet amplifier power gain requirement |
| 17. RF Attenuator, Volt Var/A | Provides electronically controllable attenuation of RF signals - RF Section |
| 18. RF Attenuator, Volt Var/B | Part of item 17 - Control Section |

TABLE 4
DESCRIPTION OF
STANDARD ANALOG MODULES

| NUMBER | FUNCTION | QUANTITY USED |
|---|---|---|
| 1 | Comparator Detector | 6 |
| 2 | Low Level Mixer | 12 |
| 3 | RF-Divider A | 26 |
| 4 | RF-Divider B | 17 |
| 5 | Wideband Ampl/PWR Divide | 44 |
| 6 | DC Switch | 5 |
| 7 | DC Amplifier/High Level Mixer | 11 |
| 8 | Logarithmic Amplifier | 17 |
| 9 | Wide Band Amplifier | 51 |
| 10 | Amplifier Limiter | 19 |
| 11 | 30 dBm Amplifier | 9 |
| 12 | Hi-Level Mixer | 13 |
| 13 | 20 dBm Amplifier | 38 |
| 14 | Electronic Switch | 26 |
| 15 | RF Divide | 34 |
| 16 | Follow Hold Integral Dump | 5 |
| 17 | Variable Attenuator/Wideband Amplifier | 3 |
| 18 | Wideband Transformer | 28 |
| 19 | RF Switch | 28 |
| 20 | Digital Control Attenuator | 42 |
| 21 | Differential Driver Receiver | 24 |
| 22 | Level Detector | 19 |
| | Total | 477 |

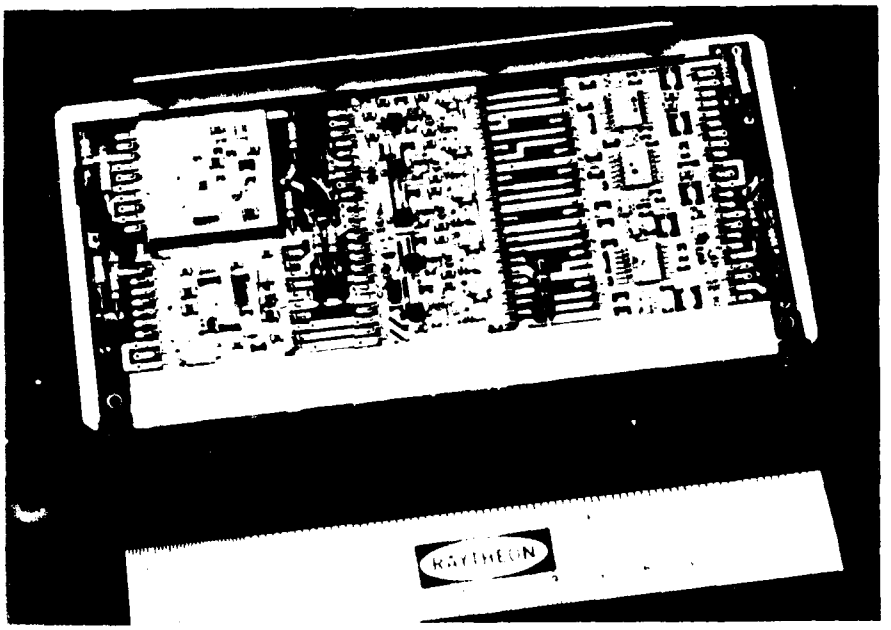



Figure 3 - Standard Analog Module

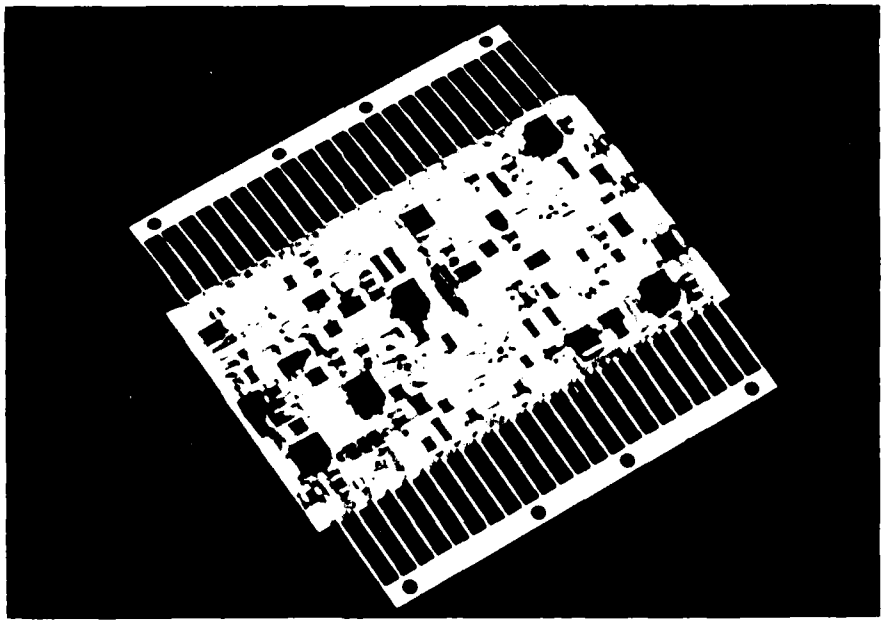


Figure 4 - Standard Analog Hybrid

## ANALOG HYBRID MICROCIRCUIT PACKAGING

The analog hybrids use 96 percent alumina ceramic substrates as a base for the screening and firing of the thick film conductor interconnect and resistor patterns.

Active devices in miniature ceramic packages, chip capacitors, chip conductors and other discrete devices are reflow-soldered to the substrate to complete the assembly.

At the early stages of the PATRIOT Program a decision was made to utilize beam-leaded active devices to improve the reliability and the mean time before failure of the system. To further enhance reliability, all active chip devices are assembled in individual packages to permit screening and burn-in prior to attaching them onto a substrate.

A miniature, leadless, hermetic package was designed to house low power devices with up to four leads or beams (Figure 5). There are two standard packages: a common collector configuration and a common emitter configuration. Both configurations are identical with the exception of the internal metallization. The metallization of both configurations has been designed to accept chip and wire as well as beam-leaded chip sizes up to 0.020 x 0.020 in.$^2$. This permitted the use of readily available chip and

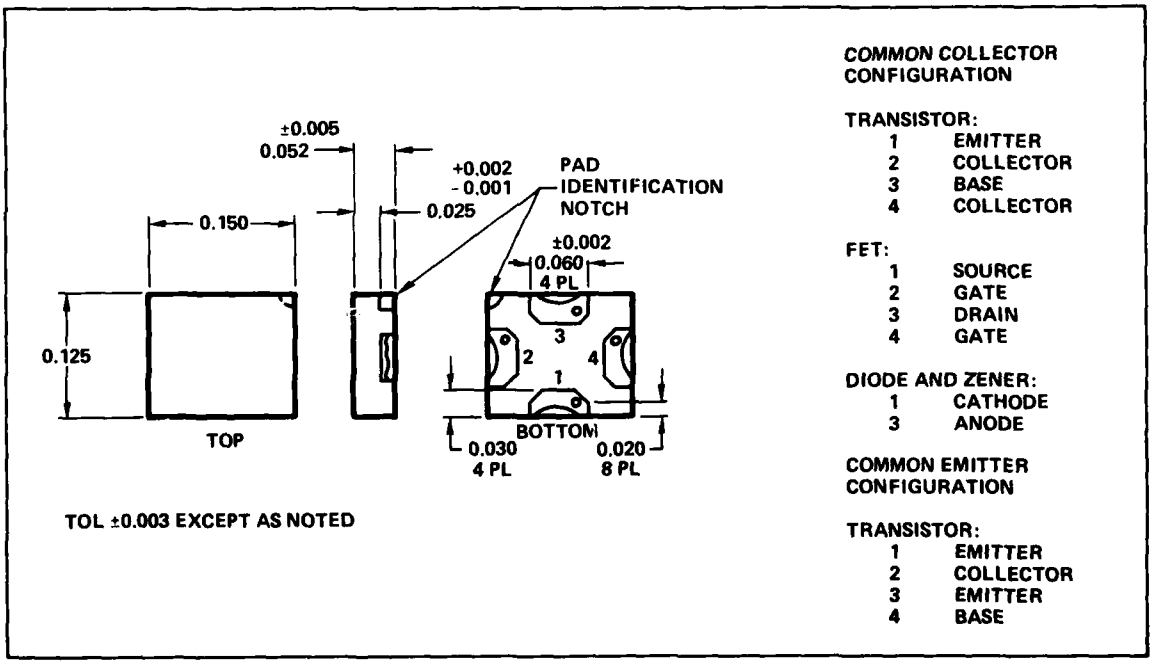



Figure 5 - Low Power Package

wire devices. The isolated lead (common emitter) configuration is used for RF application. The common collector configuration is used to house small-signal field effect transistors (FETs), diodes and common collector transistors with beam leads.

Other packages used are:

1) The TO-91 for medium power application
2) The TO-86 for linear 14-lead devices
3) Miniature stripline packages for high power applications

The active devices in their miniature ceramic packages, chip capacitors, chip inductors, and other discrete devices are reflow-soldered onto the substrate. A plated hard nickel ribbon lead provides the planar interconnection between the substrate and PC board pads. Figure 6 shows the analog hybrid assembly flow process. Environmental protection is provided by a sprayed-on polyurethane conformal coating.

Due to the capability to fully test, screen and burn-in all active devices in individual packages, the hybrid fabrication yield and reliability of these circuits has been extremely high. A reliability review of six widely used analog circuits shows only one failure in many millions of operational hours.

Today, the analog hybrid still represents state-of-the-art technology. The only significant change made is that the beam-leaded devices have been replaced with chip and wire devices to reduce cost and improve availability.

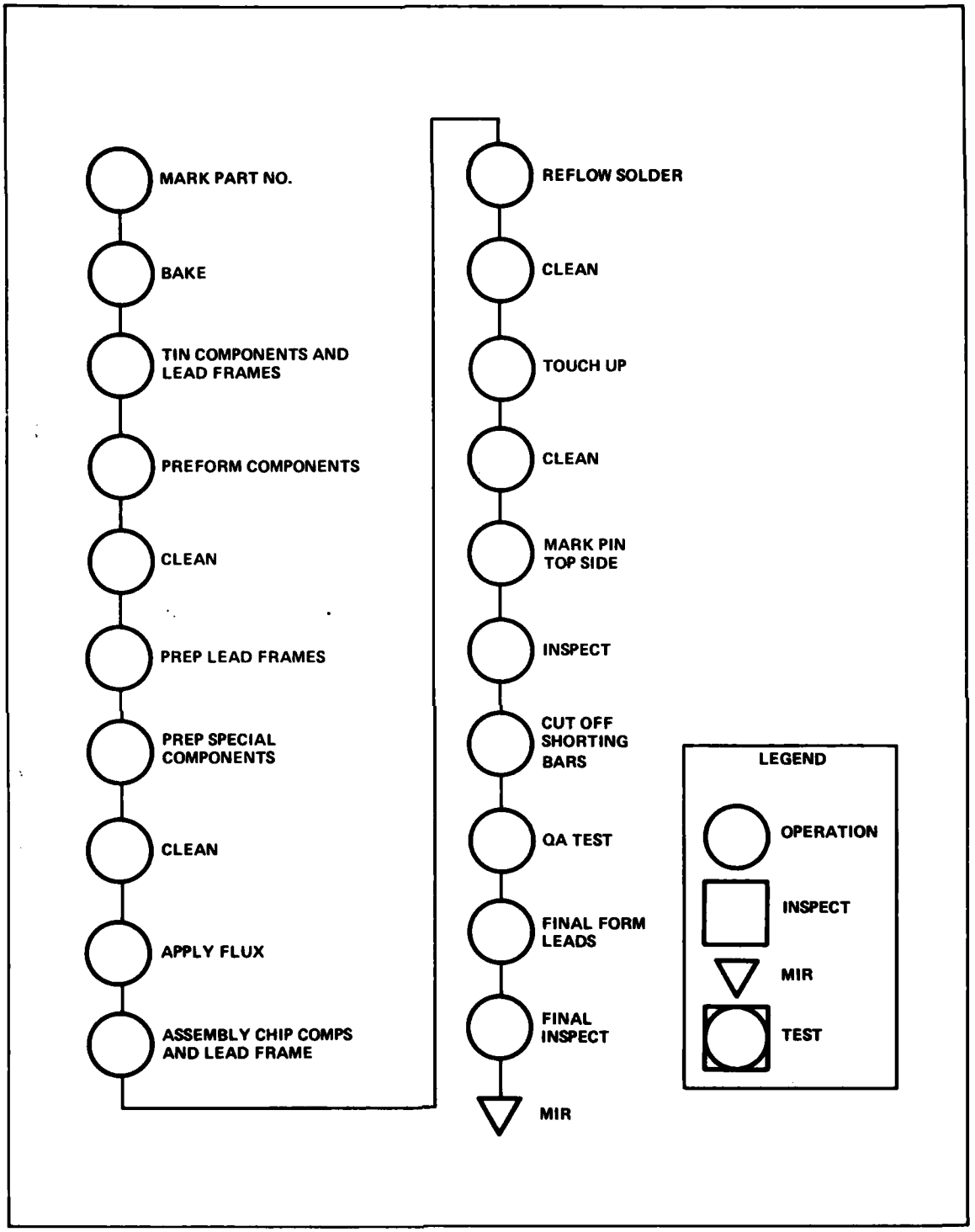



Figure 6 - Assembly Flow Chart Analog-Hybrids

## STANDARD DIGITAL MODULE

### First Design Using MSI Technology

The digital logic is transistor-transistor logic (TTL) which has been selected for its good delay - power product at clock frequencies of 5 to 6 MHz, high noise margin, and good tolerance to changes in load and temperature. The basic building block is a 60-gate general purpose array which can be personalized to any desired logic function solely by a change of the metallization pattern. The chip size is 0.086 x 0.129 in.; 50 beam-leads per chip provide good thermal conductivity for conduction cooling. The basic 60-gate array is shown in Figure 7. Up to six of these arrays are mounted on a multilayer thick film hybrid circuit of RAYPAK construction which is shown in Figure 8.

Figure 9 shows a standard digital module. The module contains up to 1800 gates in a volume of 7 $in.^3$ (6.5 x 3.83 x 0.28 in.) for a circuit density of over 250 gates per cubic inch. Typical as shown, six "RAYPAK" hybrid circuits were mounted on the standard digital module. The RAYPAK contains up to six 60-gate MSI logic arrays.

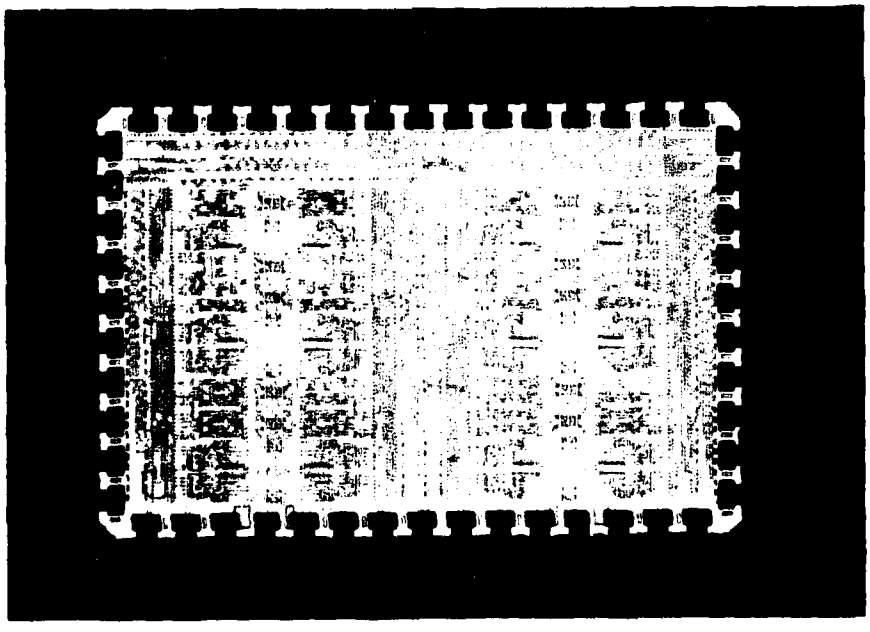
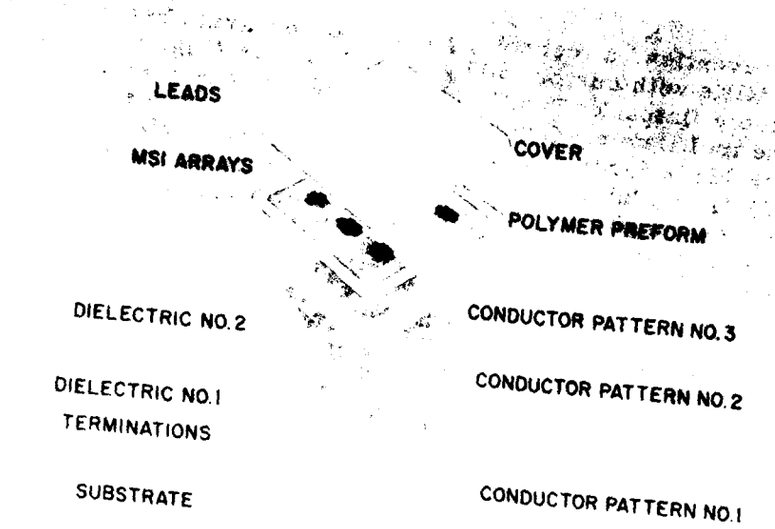


Figure 7 - PATRIOT 60-TTL Array (0.068 x 0.129 in. Dimensions)



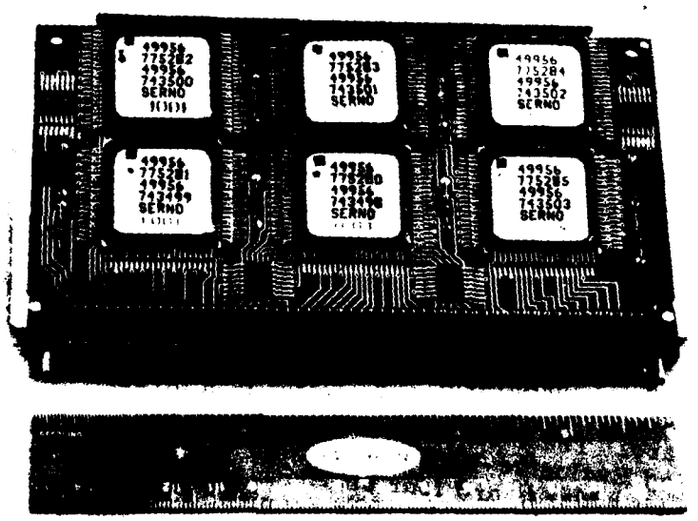



Figure 9 - Standard Digital Module First Design

## 300 GATE ARRAY - TECHNOLOGY INSERTION PROGRAM

In the late seventies, a technology insertion program replaced the obsolete RAYPACKs with custom 300 gate LSI arrays (Figure 10) in a commercially available flatpack (Figure 11) on a one for one basis. The redesign affected only the multilayer PC board design. Each of the new 300-gate array modules (Figure 12) is form, fit and function-interchangeable with its equivalent RAYPAK module. A total of 15 digital modules were redesigned. Only the use of high density hybrid packaging on the original RAYPAK design made this minimal system change possible. Table 2 shows the standard modules that were redesigned.

The new 300 gate array provides higher speed and lower power dissipation. Some of its key features are:

1) Master array which provides a low gate to pin ratio and low-cost custom personalization
2) Schottky TTL at a 5 nsec delay with a gate delay power product of 25 pJ
3) Two layer aluminum metallization system with a total of 64 pads per chip
4) Semiautomatic routing, including an extensive library of an associated technology to package the devices in commercially available flatpacks that feature mainstream IC assembly techniques such as eutectic die bonding, aluminum wire-bonding and lid weldsealing.

The 300-gate array is a universal logic device of 160 $mil^2$ silicon area. It contains 60 drivers capable of interfacing with external circuitry, 120 drivers capable of driving up to 10 internal loads, and 120 expansion elements to be used as logic AND or logic OR expander gates. Circuit diagrams of these three types of gates are shown in Figure 13. Typically, the gates dissipate 5.5 to 6 mW per driver and 1 mW per OR expander. Data on other electrical characteristics are given in Table 5.

## ARRAY PERSONALIZATION

The gates have been arranged in blocks of 12 and 13 elements, and the chip layout has been composed by computer through the stepping or mirroring of these basic blocks. Individual blocks can be interconnected as standard logic functions simply by calling the metallization layout of this function from a computer library. These function include AND/OR and AND/NOR Gates, Exclusive-OR and Exclusive-NOR Gates, Flip-flops, four and eight bit selectors, four bit adders, and four bit Arithmetic Units. The use of a data-base library greatly decreases the time required for the generation of personalized interconnect masks and drastically reduces the possibility of error.

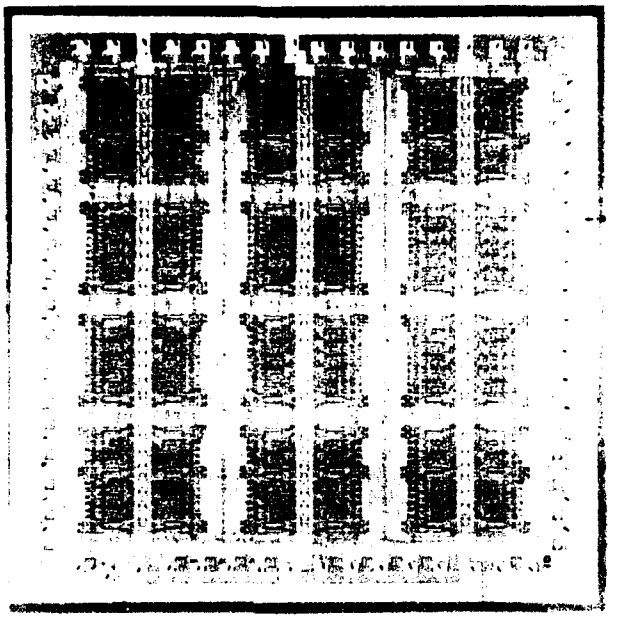


Figure 10 - Custom 300-Gate Array

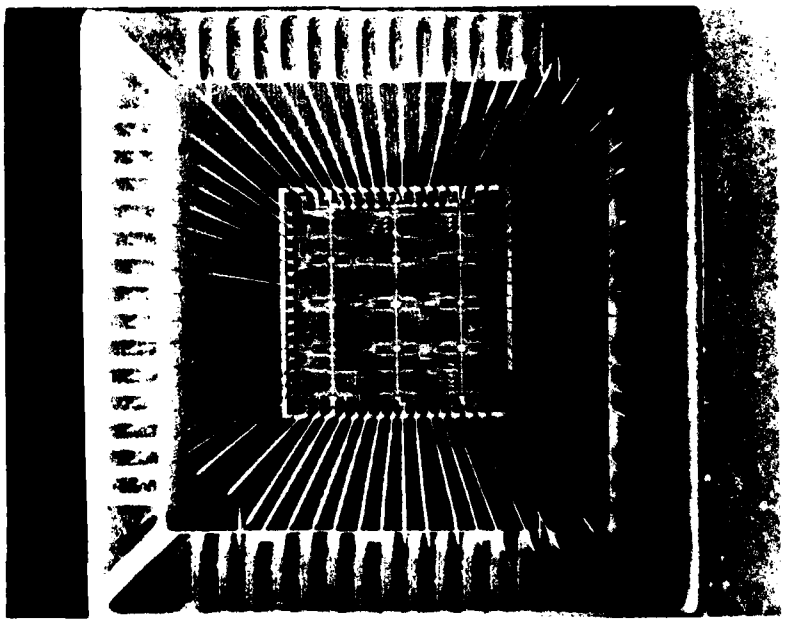


Figure 11 - 300-Gate LSI Array in 64 Lead Flatpack

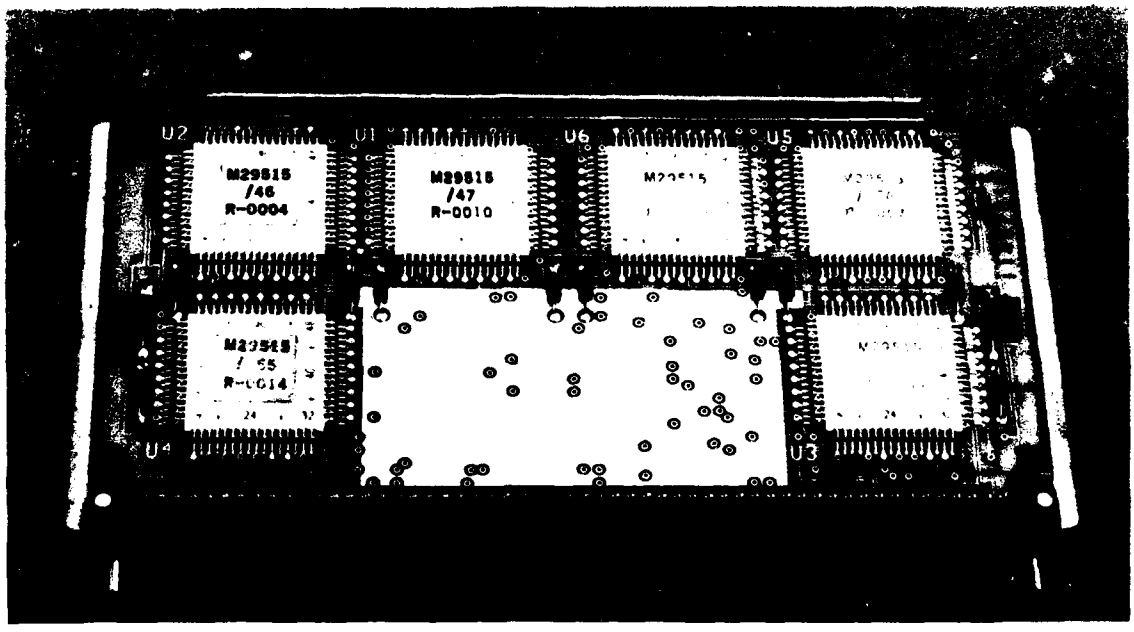



**Figure 12 - 300-Gate Array Digital Module**

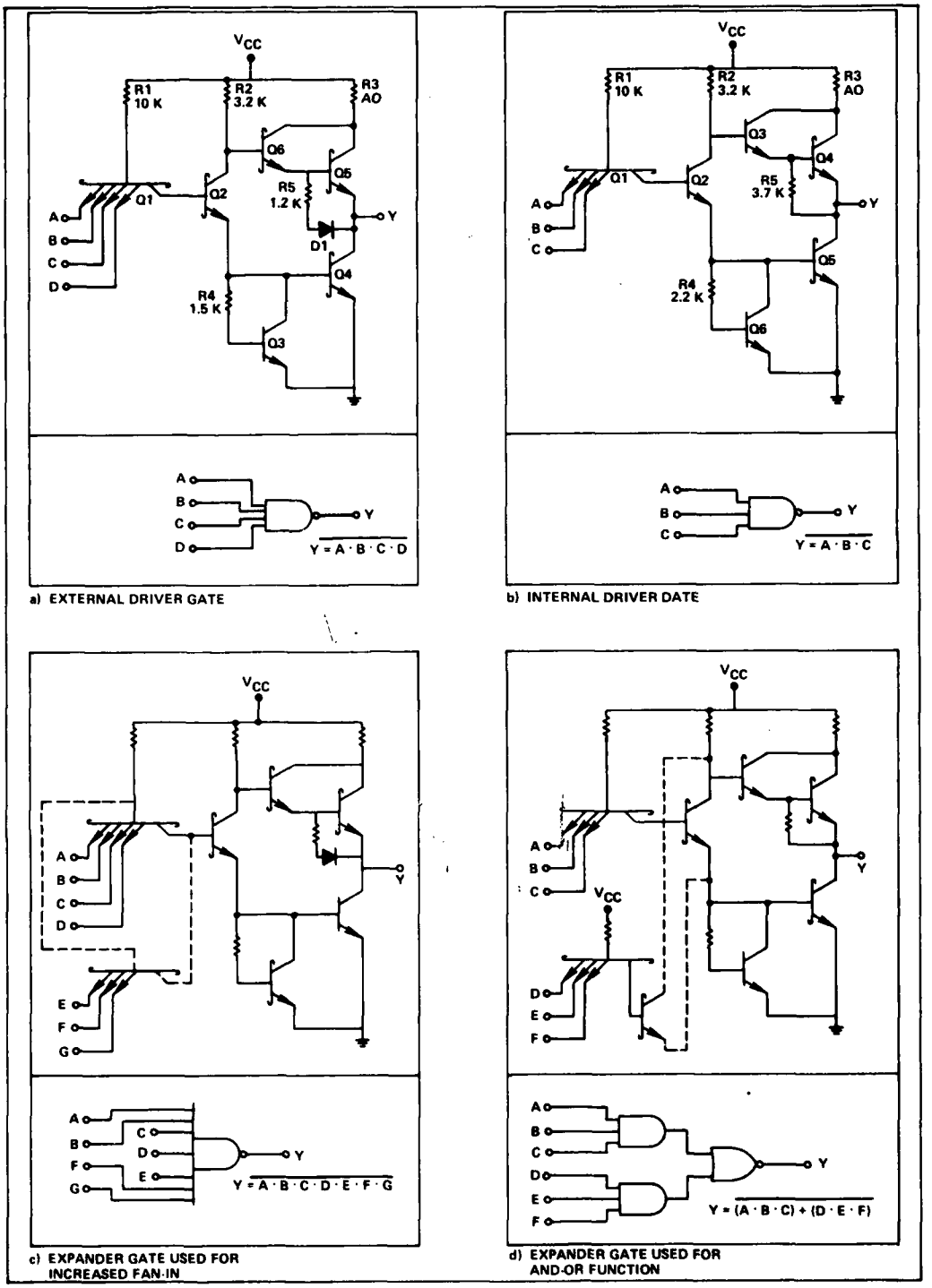



**Figure 13 - Circuit Diagrams of the Gate Elements of the 300-Gate Array**

TABLE 5
ELECTRICAL SPECIFICATION OF THE 300-GATE ARRAY
EXTERNAL GATE OF THE RA-116C AND RA-116M

RECOMMENDED OPERATING CONDITIONS

| | RA-116C | | | RA-116M | | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max | |
| Supply Voltage, Vcc | 4.75 | 5.0 | 5.25 | 4.5 | 5.0 | 5.5 | V |
| Operating free-air temp., $T_A$ | 0 | | 70 | -55 | | +125 | °C |

ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE

| Parameter | | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-Level output | $V_{CC}$ = Min<br>$I_{OH}$ = -0.5 mA<br>$V_{IL}$ = 0.8 V | 2.4 | | | V |
| $V_{OL}$ | Low-level output | $V_{CC}$ = Min<br>$V_{IH}$ = 2.0 V<br>$I_{OL}$ = 14 mA | | | 0.5 | V |
| $I_I$ | Input current at max input voltage | $V_{CC}$ = Max<br>$V_I$ = 5.5 V | | | 1.0 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = Max<br>$V_I$ = 2.4 V | RA-116c | | 60 | µA |
| | | | RA-116M | | 40 | |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = Max<br>$V_I$ = 0.4 V | | -0.4 | -0.6 | mA |
| $I_{CCH}$ | Supply current outputs outputs high (AVE./Ext. Drv. gate) | $V_{CC}$ = 5 V<br>$V_I$ = 0 | | 0.42 | 0.84 | mA |
| $I_{CCL}$ | Supply current outputs low (AVE./Ext. Drv. gate) | $V_{CC}$ = 5 V<br>$V_I$ = 2.4 V | | 1.54 | 2.77 | mA |
| $P_{AVE}$ | Power Dissipation | $V_{CC}$ = 5 V | | 5.0 | | mW |
| $T_{PD}$ | Propagation delay | $V_{CC}$ = 5 V<br>$T_A$ = 25 °C<br>$C_L$ = 15 pF<br>$R_L$ = 1 KΩ | | 5 | 10 | nsec |

The 300-gate array is designed for computer-aided personalization. All wiring channels are situated on a 0.6 mil grid to facilitate routing. Connections are made between metal layers by use of underpasses which can be tapped anywhere along their length. These underpasses are also situated on a 0.6 mil grid.

The desired logic functions are first modelled and verified through computer simulation. The resulting data base serves as the principal input to test software generation and documentation. It also serves as a logic verification of personalization masks.

## BENEFITS

In addition to the improved performance such as higher speed and lower power, the following cost and reliability benefits have been realized by this LSI technology insertion:

1) the packaged 300-gate array is one fifth the cost of the RAYPAK it replaces;

2) the average failure rate for the fifteen 300-gate array module type is predicted to be one half that of the 15 RAYPAK module types that they replace.

## COMPUTER AIDS TO DESIGN

Most analog and digital circuits have been developed with the aid of computerized circuit analysis programs. The use of computer-aids in PATRIOT goes much futher, however, and is practically all-pervading. Without complete design automation, the design and test of devices such as the TTL master arrays and modules in the 1800-gate range would have been impossible.

The entire design automation program comprises four major tasks, namely:

1) System design, logic design and partitioning, using large general-purpose computers, terminals and interactive displays

2) Layout and mask generation which in general depends on computer-controlled high-precision drafting tables, mask generators and interactive displays

3) Test generation and testing at the various device and assembly levels. This phase requires both general purpose computers for test program generation and computer-controlled testers. The latter provide functional, parametric and dynamic tests and such capabilities as data logging and the amplification of environmental stress

4) Reliability predictions at various device, hybrid and module levels such as storage reliability, stress analysis and MTBF predictions utilizing programs on general purpose computers.

## FACTORY TEST EQUIPMENT

While similar or identical processing equipment is used in development and manufacturing, more severe demands are being placed on manufacturing testing from the viewpoint of throughout and simplicity of operation. For this reason, a major effort was required in developing the microcircuit manufacturing test capability for PATRIOT.

The development of microcircuits has outstripped commercially available testers in performance and sophistication. It is for this reason that the Andover plant, based on its HAWK program experience, has developed and built its own test equipment.

All test stations are controlled by a central computer system which provides uniform standards of programming, data logging and data retrieval. In addition, more complex stations are structured as "intelligent terminals" with their own local minicomputer which provides real time local control of test sequences as well as queuing of the data flow to the contral test control system.

It is beyond the scope of this survey article to discuss in detail the design of the various test stations, but Table 6 gives an overview list. It should be noted that the digital tester provides parametric and dynamic test capabilities in addition to functional testing up to a module complexity of about 2000 gates. A continuity/leakage tester assures the integrity of all hybrid substrates before they go into circuit assembly, and two analog testers cover the full range of analog test requirements.

## SUMMARY

This paper has described how microelectronic technology is being used in PATRIOT, a U. S. Army ground-to-air defense system with major new capabilities. Without doubt, microelectronics makes it possible to stay within the bounds of manufacturing cost, reliability and size. Life cycle costs and logistics have been improved by standardization at the electronic module level, and by the use of high density hybrid technologies.

The latter were shown to be instrumental in the successful upgrading of the system from MSI to a more advanced LSI technology with a minimum impact on hardware design, by simple module replacement. Finally, microelectronic fabrication has led to increasingly complex design, processing and assembly technologies. Without design, manufacturing and test automation, the economic and reliable manufacturing of a system as complex as PATRIOT would have been impossible.

TABLE 6
PATRIOT MICROELECTRONICS FACTORY TEST STATIONS

| Test Station | Qty | Description | Performance |
|---|---|---|---|
| Digital Test Station | 2 | Automatically tests high speed Digital Modules | 1. Dynamic Functional Tests<br>2. DC Parametric Tests<br>3. Propagation Delay Tests |
| Pulse Analog Test Station | 1 | Automatically tests Analog/ Digital Chips Substrates, and Modules | 1. Waveform Analysis Tests<br>2. DC Parametric Tests<br>3. AC Parametric Tests |
| Continuity /Leakage Test Station | 1 | Automatically tests Micro-electronic Substrates | 1. Continuity Tests<br>2. Leakage Tests |
| High Frequency Analog Test Station | 2 | Automatically tests Analog Substrates and Modules | 1. Gain Tests<br>2. Phase Tests<br>3. Group Delay Tests<br>4. Intermodulation Distortion Tests<br>5. Dynamic Response Tests<br>6. Noise Figure Test<br>7. Spectrum Analysis Test |
| Semi Automatic Test | | Provides centralized computerized facility in hard-wired support of automatic PATRIOT Test Stations | 1. Supervises the process controller at the test stations<br>2. Maintains a complete library of UUT Programs and software packages<br>3. Collects test data and provides test summaries |

# HYBRID CIRCUIT TECHNOLOGY FOR VHSIC*

By

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## SUMMARY

To achieve high packaging densities and short interconnect lines, military systems often employ for the packaging of digital equipment circuits utilizing a ceramic substrate which connects a number of LSI and VLSI chips. As the density, speed, and I/O complexity of the chips increases, the conventional ceramic hybrid substrate is less suitable as an interconnect medium. With increasing chip I/O complexity, and, hence, interconnect density, the on-chip output driver design must grow in size in order to achieve a lower output impedance to drive the increased capacitance parasitics at faster rates. Not only does the driver size grow, but its associated power dissipation also increases.

Interchip interconnection problems are compounded when emerging VLSI switching times approach the subnanosecond region. For these devices transmission line interconnects are required. Conventional interconnect approaches for very high speed devices rely on PC board based matched impedance interconnects with a reasonably low characteristic impedance (50-70 ohms). These approaches yield a very low interconnect density, and demand on-chip output drivers of relatively high power.

What is really needed for the full realization of VHSIC is a packaging technology that permits the growth in chip I/O complexity, while reducing the on-chip power (and driver size) required to transmit data along the chip interconnects. Despite the desired reduction driver power, a simultaneous reduction in the signal propagation delay between chips is required.

This paper will discuss a solution to these problems based on the interconnection of VHSIC's by means of high-density multilayer thin film substrates. Two different design approaches based on the same technology will

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be considered. For off-chip switching delays in the low nanosecond region, a design focusing on short, narrow lines, yielding low line capacitance with a high interconnect density, is described. For the highest switching speeds, a controlled impedance design with very narrow lines for high $Z_o$ is proposed.

On-going work will be reported for both approaches which utilizes polished sapphire substrates to achieve line widths of a few micrometers. Particular attention will be paid to various power and ground line distribution schemes which minimize coupling to signal lines. Much of this technology is based on well proven monolithic circuit processes.

Such high-density thin film hybrids for the interconnection of VHSIC devices can be packaged in conventional hybrid form. For highest efficiency, however, it is advantageous to stack these hybrids in a high-density, three dimensional configuration. The interconnection of these hybrid substrate stacks will be discussed.

The novel hybrid packaging approaches for VLSI and VHSIC discussed in this paper will be able to achieve a significant overall increase in system performance when compared to conventional packaging techniques.

## Review of LSI/VLSI Circuit Technologies

Over the past several years semiconductor technologies have made significant advances toward dense and extremely complex integrated circuits. This has been achieved through improved lithography, and by utilizing a number of new process technologies as well as circuit design concepts. The applications for these expanding semiconductor technologies have generally been segmented into two main areas consisting of logic and memory. More recently, the microprocessor ($\mu$P) has evolved which combines logic and memory on the same semiconductor chip in order to create total processor functions. This $\mu$P development can be viewed as a natural outgrowth of the rise in chip complexity. In other words, as the potential of including more circuit elements on a single chip became a reality, it was evident that greater performance could be achieved through logic/memory merging rather than having to interface between separate chips, each being dedicated to either memory or logic functions.

In the logic area two major directions are being pursued. These consist of very large scale integration (VLSI), medium speed (1-10 nsec) devices, and very high speed (< 1 nsec) devices with medium-to-large scale integration (MSI to LSI) potential. In the following sections the present and future potential of some of the logic technologies will be explored in some detail in order to better understand the need for hybrid microcircuits for VHSIC technologies. Figure 1 indicates the various technologies being used or explored at present for memory and logic applications. The government funded VHSIC program is providing an accelerated effort directed toward improving the performance of IC technologies in terms of density, power dissipation, and speed. The initial thrust is being directed toward the development of

high density lithographic techniques (E-Beam/X-Ray). It is expected that improvements will be made, not only in density, but also in speed and power through the complete downward scaling of all device features.

With respect to the applicability of the technologies listed in Figure 1, there are a number of technology issues aside from density:

- Speed/power
- Logic/memory compatibility
- Radiation hardness
- Integration potential
- Maturity
- Support systems (packaging)
- Dynamic versus static power

| Logic | | Memory | |
|---|---|---|---|
| Bipolar | FET | Bipolar | FET |
| TTL | NMOS | TTL | NMOS |
| $I^2L$ | PMOS | $I^2L$ | PMOS |
| ECL | CMOS | ECL | CMOS |
| EFL | CMOS/SOS | | CMOS/SOS |
| ISL | SI MESFET | | CCD |
| STL | GaAs MESFET | | SI MESFET |
| | CCD | | FAMOS |
| | | | MNOS |
| Other Technologies | | | |
| Josephson Junction<br>Magnetic Bubble<br>Transferred Electron Devices (TED) | | | |

Figure 1 - Semiconductor Technologies

In the following sections of this paper we will attempt to address some of these issues and show how they impact design approaches for hybrids. One of the issues listed is that of integration potential. As already mentioned, it is expected that significant improvements in density, speed, and power will be made through a complete downward scaling of all device parameters.

## The Impact of Dimensional Scaling on VLSI

It has been predicted and partially demonstrated (References 1, 2, and 3), that tremendous gains in integrated circuit complexity can be achieved through the effective downward scaling of device element sizes and the appropriate adjustment of process parameters. Through this process of scaling, predictions can be made indicating the future evolution of Super VLSI devices; e.g., chips with hundreds of thousands of gates for random logic and/or millions of bits of memory. It is also predicted that these densities will be achieved with an increased speed of operation at little increase in total chip power dissipation. These projections are primarily based on silicon MOS type technologies, but apply also to some bipolar designs as, for instance, $I^2L$. MESFET structures will also benefit from scaling.

As a guide to making density growth predictions for the various MOS type device technologies, charts similar to the one shown in Figure 2 have been developed. This chart indicates some of the performance limiting factors along with those areas that will place increasing demands on process technologies.

The effect of scaling on device performance is shown in Figure 3 for CMOS/SOS logic technology. In this table an expected growth in chip size has been factored together with an anticipated increase in logic gate density. Note, that for gate oxides the scaled thickness for 0.5 μm linewidth is approaching 75 Å. This represents a very ambitious goal if one considers the fact that over the last five to six years gate oxides have only been reduced by a factor of two to three. Again, this does not imply that very thin oxides have not been grown or deposited in the fabrication of novel device structures, but that achieving this for super VLSI devices may be difficult. It is anticipated that the 0.5 μm linewidth resolution will be achieved, reproducibly, before a thin oxide process has matured sufficiently for inclusion in VLSI designs. In fact, MESFET gate structures will probably benefit the most from reduced linewidths.

We can see the tremendous impact that dimensional scaling will have on VLSI circuit technology. A similar evolution must occur in packaging in order to incorporate these devices into a complex military system. Before addressing the problems faced in packaging such devices in a hybrid interconnect structure let us review the expected performance of various circuit technologies.

| | DEVICE/CIRCUIT PARAMETER | SCALING FACTOR | |
|---|---|---|---|
| DEVICES | DEVICE DIMENSION $t_{ox}$, L, W | $1/\eta$ | |
| | DOPING CONCENTRATION N | $\eta$ | |
| | VOLTAGE V | $1/\eta$ | |
| | CURRENT I | $1/\eta$ | |
| | CAPACITANCE A/t | $1/\eta$ | |
| | DELAY TIME/CKT. VC/I OR $1/f_c$ | $1/\eta$ | $P_D\tau_D \rightarrow 1/\eta^3$ |
| | POWER DISSIPATION/CKT. VI OR $CV^2f$ | $1/\eta^2$ | |
| | POWER DENSITY VI/A | 1 | |
| INTERCONNECTS | LINE RESISTANCE, $R_L = \rho L/Wt$ | $\sqrt{\eta}$ | |
| | NORMALIZED VOLTAGE DROP $IR_L/V$ | $\sqrt{\eta}$ | |
| | LINE RESPONSE TIME $R_LC$ | 1 | |
| | LINE CURRENT DENSITY I/A | $\eta$ | |
| | RESULTS FOR VLSI | | |
| | INTEGRATION LEVEL | $\eta^2$ | |
| | POWER/CHIP | 1 + | |

Figure 2 - "MOS" Circuit Performance versus Device Scaling

| Linewidth | 4 μm | 2 μm | 1 μm | 0.5 μm |
|---|---|---|---|---|
| Gate Oxide | 600Å | 300Å | 140-300Å | 75-150Å |
| Maximum Voltage | 8-10 V | 4-5 V | 2 V | 1 V |
| Delay Time/Stage | 0.5 nsec | 0.25 nsec | 0.1 nsec | 0.05 nsec |
| Power Dissipation/ Circuit | 0.08 mW | 0.02 mW | 0.005 mW | 0.002 mW |
| Line Response Time | 0.1 nsec | 0.1 nsec | 0.1 nsec | 0.1 nsec |
| Clock Frequency | 20 MHz | 40 MHz | 80 MHz | 160 MHz |
| Chip Size | 5 x 5 mm | 7 x 7 mm | 9 x 9 mm | 10 x 10 mm |
| No. of Gates per Chip | 3,000 | 10,000 | 40,000 | 100,000 |

Figure 3 - Effects of Scaling on CMOS/SOS Circuit/Device Parameters

Characteristics of VLSI Circuit Families

It can be assumed that the best performance for digital systems will be achieved by selecting and developing those technologies that can yield the highest monolithic integration level. The direction will thus be toward structures having fewer components per gate, smaller signal swings, and reduced parasitic capacitance. Some of the contending circuit families are shown in Figure 4. Their present and expected future characteristics are listed in Figure 5. Naturally, the numbers shown are typical only, and can vary considerably, depending on processing details. The delays include on-chip line delays.

As can be seen, $I^2L$ and CMOS/SOS are especially attractive circuits. $I^2L$ can easily be combined on-chip with powerful bipolar drive circuits. CMOS/SOS, on the other hand, combines low power dissipation with switching speeds below 1 nsec. Short channel bulk NMOS and NMOS on SOS would be close contenders, except for the fact that their higher power dissipation limits the achievable integration level.

For most bipolar manufacturers, $I^2L$ represents a most promising technology. Logic circuits employing $I^2L$ can be readily fabricated to operate over the full military temperature range (-55 to +125°C). An $I^2L$

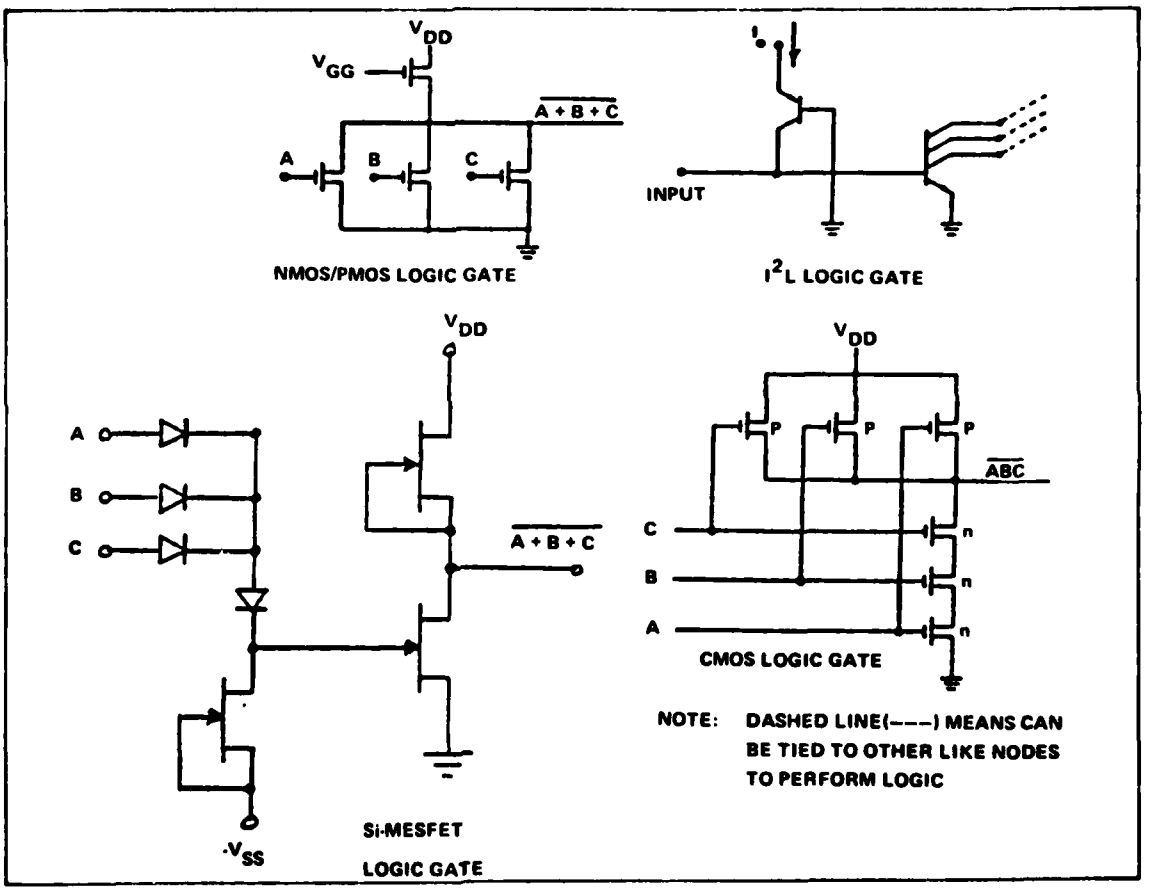



Figure 4 - Circuit Families Suitable for VLSI Implementation

| Circuit Family | | Line Resolution (μm) | Integration Level (Gates/Chip) | Gate Delay (nsec) | Power/ Gate (mW) |
|---|---|---|---|---|---|
| CMOS/SOS | 1980 | 2-4 | 5,000 | 1 | 0.02 |
| | 1983 | 1-2 | 20,000 | 0.5 | 0.005 |
| | 1985 | 0.5-1 | 100,000 | 0.25 | 0.002 |
| NMOS | 1980 | 2-4 | 5,000 | 1 | 0.3 |
| | 1983 | 1-2 | 20,000 | 0.5 | 0.1 |
| | 1985 | 0.5-1 | 50,000 | 0.2 | 0.02 |
| $I^2L$ | 1980 | 2-4 | 8,000 | 5 | 0.05 |
| | 1983 | 1-2 | 30,000 | 3 | 0.03 |
| | 1985 | 0.5-1 | 100,000 | 1 | 0.01 |
| Si MESFET | 1980 | 2-4 | 10,000 | 0.8 | 0.1 |
| | 1983 | 1-2 | 20,000 | 0.4 | 0.05 |
| | 1985 | 0.5-1 | 50,000 | 0.2 | 0.02 |

Figure 5 - Characteristics of VLSI Circuit Families

microcomputer chip set is being offered by one manufacturer that includes a 16-bit single chip microprocessor. The gate speeds of $I^2L$ circuits are expected to decrease to a few nsec with scaling.

Characteristics of Gigahertz Logic Families

Compared to lower speed technologies, few ultra high speed circuit families are evolving as serious contenders, and except for ECL type circuits, most are still in the exploratory or advanced development stage. The important high speed circuit families are shown in Figure 6, and Figure 7 provides a summary of their characteristics. Actually, some of the VLSI circuit families discussed in the last section are candidates in this category also.

The figure provides typical values of various parameters. The gate delays shown represent on-chip values, including capacitive and travel delays as encountered in devices of significant integration level. Off-chip drive power will be significantly higher. Some delays which have been measured on bare gates with a minimum of parasitic loading have been reported in the literature to exhibit considerably shorter switching delays - in the order of

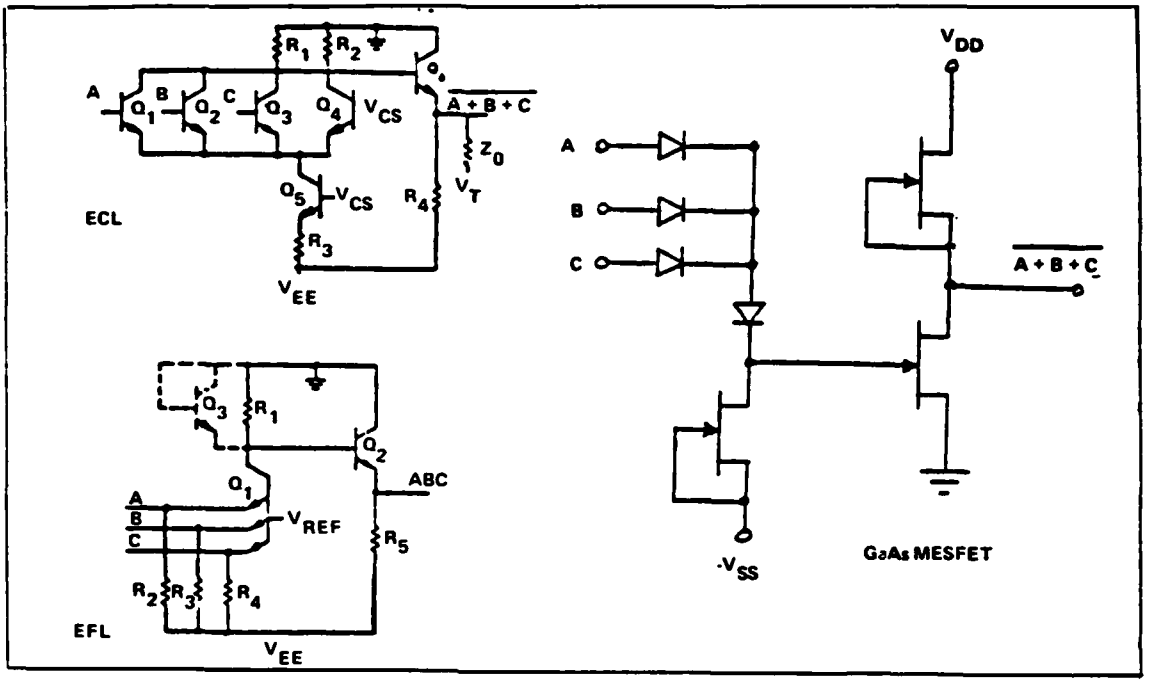



Figure 6 - Circuit Families for Gigahertz Operation

| Circuit Family | | Line Resolution (μm) | Integration Level (Gates/Chip) | Gate Delay (nsec) | Power/ Gate (mW) |
|---|---|---|---|---|---|
| GaAs MESFET | 1980 | 2-4 | 1,000 | 0.2 | 0.25 |
| | 1983 | 1-2 | 5,000 | 0.1 | 0.1 |
| | 1985 | 0.5-1 | 10,000 | 0.05 | 0.05 |
| ECL/EFL | 1980 | 2-4 | 1,000 | 0.5 | 2 |
| | 1983 | 1-2 | 5,000 | 0.3 | 0.5 |
| | 1985 | 0.5-1 | 20,000 | 0.1 | 0.2 |

Figure 7 - Characteristics of High Speed Circuit Families

100 psec for ECL and EFL, and between 20 and 40 psec for GaAs MESFETs. Electron beam-masked MOS circuits have also demonstrated delays close to 100 psec, but this masking technology does not yet represent a high-yield production method for integrated circuits because of the submicron line-widths and registration tolerances used. The near term minimum gate delays will realistically approach 100-300 psec. Such a delay permits 10-20 gate delays per clock cycle which suffices for implementing reasonably conventional architectures in a 250 MHz system.

As mentioned, some of the VLSI circuit families could possibly be considered in this logic class. However, their high output impedance would restrict the speed with which one could come off-chip.

This then leaves for the present as the most serious contenders for ultra-high speed logic the bipolar silicon ECL family and GaAs MESFET circuits. Often a mix of subfamilies provides the optimum performance and integration level.

In comparison to bipolar ECL on silicon, GaAs MESFET technology suffers from a less developed processing technology. GaAs MESFETs can be implemented in two circuit technologies. The faster circuit utilizes separate depletion mode gates and driver/inverters and requires a level shift network (usually one or more Schottky diodes) to adjust input and output levels. The low power GaAs MESFET circuit is based on the use of deep depletion mode MESFETs which are off at zero gate bias and operate in effect as enhancement mode transistors. Here pinch off at zero bias is determined by the offset voltage of the Schottky diode.

GaAs MESFET transistors by themselves switch extremely fast, in the order of 10 psec. Due to the relatively high output impedance, however, the RC time constant of an actual gate extends the gate switching time into the range of the best ECL performance. This high output impedance also represents a problem in driving off-chip interconnection lines.

As a consequence, the ECL circuit family offers at present the best performance in a typical high-speed computer or signal processor environment with its many devices, interconnections and packaging levels. In applications where highest speed is required, but logic complexity is limited, high speed GaAs MESFETs with level shifters offer the best performance. Such applications are IF and RF memories, counters, sequencers and multiplex switches.

## Interconnect Concerns for VHSIC Circuit Technologies

The previous sections have reviewed in some detail the current and future performance of a number of VHSIC circuit technologies. Most of that discussion was devoted to on-chip performance for those technologies considered. The problem now is to focus on chip interconnection systems in a hybrid environment that can provide for the highest interconnect density

consistent with the I/O properties of these various device technologies. In general, chip interconnect systems can be defined as:

- Simple interconnect
- Lumped element interconnect
- Transmission line interconnect

The choice of any one, or a combination, of these general classifications for a hybrid interconnect network is very much dependent on specific device I/O characteristics. Some of these characteristics consist of input impedance, and rise and fall times of signals from the chip output drivers under conditions of minimum load. The ultimate density of a hybrid network is also very much dependent on the specific substrate technology. It would be instructive to explore some of the criteria that can be developed to relate a specific device technology to one or more of these general interconnect classifications. In each case we will be searching for crossover conditions, i. e., simple to lumped and lumped to transmission line.

Simple to Lumped Interconnect Criteria

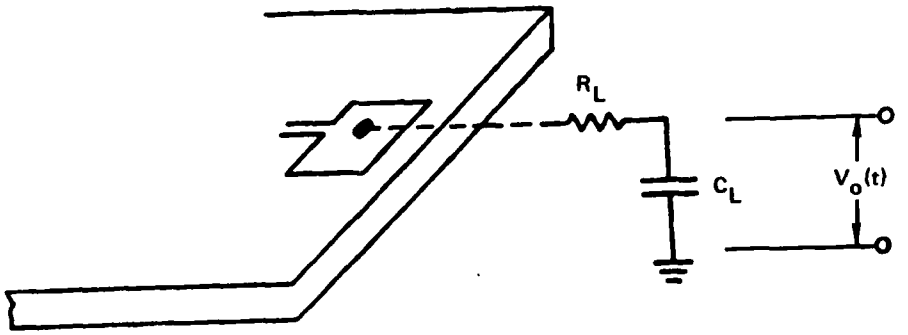
A simple interconnect on a hybrid network is defined as one that would be transparent to line parameters such as $R_L$, $C_L$, $L_L$ and line delay, $\tau_d$. A circuit technology that may satisfy this criteria to a large extent is TTL, where the rise and fall times are in the range of 2-5 nsec, thus limiting clock frequencies to 10 MHz. Let us examine the necessary conditions in more detail.

In its simplest form the interconnect between one chip output to the input of one or more similar chips can be modeled with lumped elements as in Figure 8a.

In this equivalent circuit it is assumed that line inductance is small compared to line capacitance (a more detailed model can include line inductance). It can also be assumed that the input gate resistance on-chip is much larger than $R_L + R_O$. This may not be the case if n is large (a high FAN-IN). Since our goal here is to illustrate the methodology to be employed these simplifications are justified and lead to the circuit shown in Figure 8b.

The chip output voltage is represented by a truncated ramp given by the equation

$$v_c(t) = Ktu(t) - K(t-\tau_r)u(t-\tau_r)$$



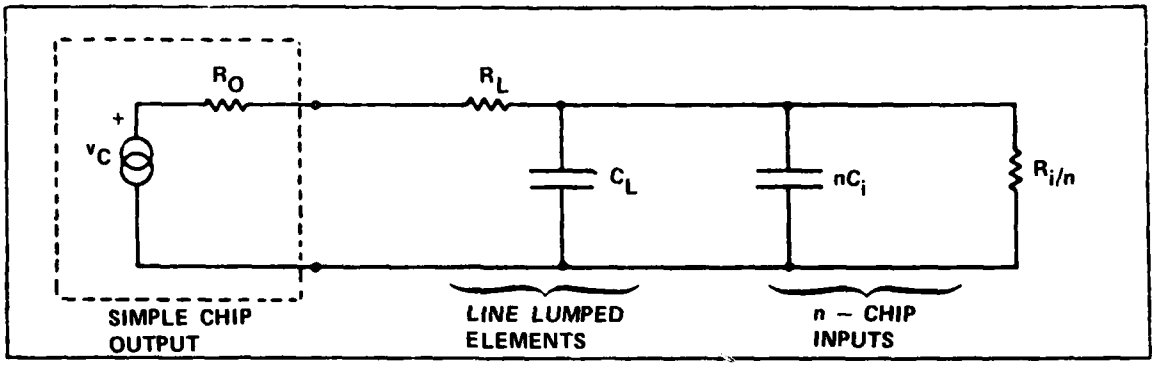




Figure 8a - Lumped Element Model

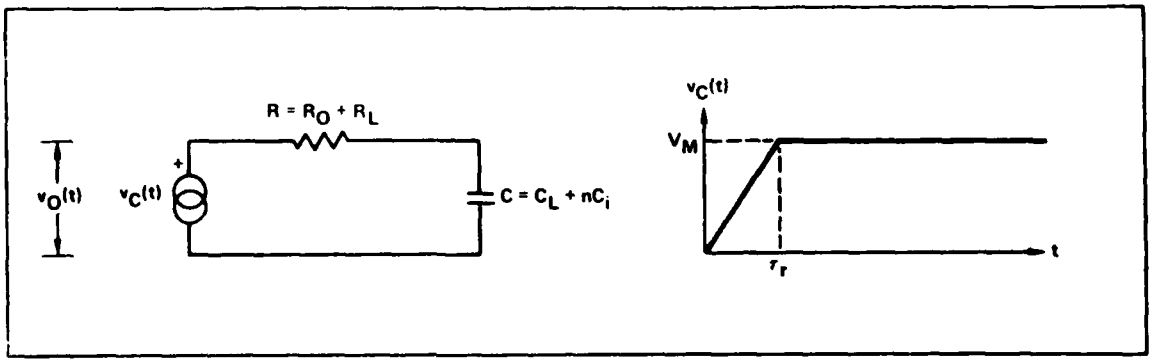



Figure 8b - Simplified Circuit

where,

$$K = \frac{V_M}{\tau_r}$$

$\tau_r \equiv$ equivalent rise time of chip output

$V_M \equiv$ logic "one" level

Using Laplace Transforms,

$$Vc(S) = \frac{K}{s^2} - \frac{K}{s^2} \epsilon^{-\tau s}$$

The output voltage response is now

$$Vo(S) = \frac{K/RC}{S^2\left(S + \frac{1}{RC}\right)} (1-\epsilon^{-\tau s})$$

Solving for the rising portion of the response we have,

$$Vo(t) = Kt - KRC (1-\epsilon^{-t/RC})$$

From this response we see that

$Kt \equiv$ simple interconnect response

$KRC(1-\epsilon^{-t/RC}) \equiv$ lumped element contribution

Therefore, if $RC << \tau_r$ then the simple interconnect model applies.

For TTL output drivers $R_O$ can range from 50 Ω to 200 Ω. If the equivalent line capacitance plus input capacitance is in the range of 10 pF we have

RC = 0.5 nsec to 2 nsec

If $\tau_r$ ranges from 2 nsec to 5 nsec then it is just marginally acceptable to consider the interconnect as simple. Thus, a TTL hybrid will probably consist of a mix of simple and lumped equivalent lines.

Transmission Line Interconnect Criteria

When the interconnect path length is on the order of 1/3 to 1/2 of the rise or fall time of the digital signal, transmission line concepts must be employed. In some cases a matched impedance might even be required for shorter distances. The gate inputs may respond when the incoming digital

signal has reached as little as 20 percent of a rise or fall time. However, in general, it has been adequate to consider 1/3 of a rise or fall time as the dividing point between lumped and transmission line interconnects.

Typically, signal transmission occurs via a TEM mode of propagation. For such a mode the propagation time is given by

$$t_{pd} = 33 \sqrt{\epsilon_r} \text{ psec/cm}$$

where $\epsilon_r$ is the relative dielectric constant. If the dielectric medium is a glass ceramic, for instance a hybrid circuit substrate with a dielectric constant of 8, then the propagation delay time is 93 psec/cm. For any other dielectric medium, the curve shown in Figure 9 may be used to determine the associated propagation delay time.

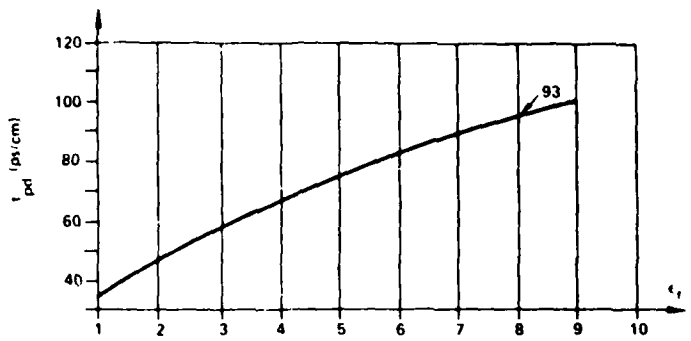



Figure 9 - Propagation Delay Time as a Function of Dielectric Constant

Consider the example of a glass ceramic substrate with $t_{pd}$ of 93 psec/cm and the requirement that transmission line technology be imposed when the propagation delay paths are greater than 1/3 of a single rise or fall time. This translates to rise and fall times of 279 psec for each centimeter of equivalent path length. In terms of a usable figure of merit, when

$$\frac{3 X t_{pd} X L}{t_r \text{ or } t_f} \geq 1$$

then transmission effects must be considered. Again, $t_{pd}$ is the TEM wave propagation time per cm, L is the line path length in cm, and $t_r$ and $t_f$ are rise and fall times. This relationship may also be expressed in the following way, describing a critical path length

$$L_c = \frac{1}{3} \quad \frac{t_r \text{ or } t_f}{t_{pd}}$$

Whenever the actual path length L exceeds the critical path length $L_c$ then transmission line interconnects must be provided.

For the future device technologies rise/fall times are expected to be in the range of 100 to 500 psec. For a propagation delay constant of 93 psec/cm (ceramic), the critical path lengths range from 0.3 cm to 1.79 cm as shown in Figure 10. If a material with a lower dielectric constant is used for signal propagation within a hybrid substrate, the critical path length would be increased. As an example, an organic material such as Kapton/Polyimide ($\epsilon_r = 3.4$) results in an $L_c$ of 0.56 cm for a 100-psec rise or fall time. Figure 10 illustrates the critical path length $L_c$ as a function of the dielectric constant of the propagation medium and the response of high-speed circuits, such as GaAs MESFETs. With rise and fall times in the range of 100 psec, transmission line interconnects are required between all chips on a single substrate.

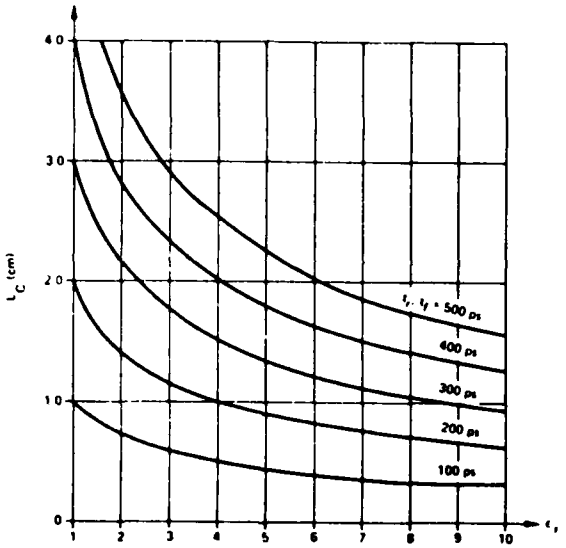



Figure 10 - Critical Path Length ($L_c$) as a Function of Dielectric Constant for Various Logic Gate Response Times

## Interconnect Criteria in Relationship to Hybrid Technologies

In the last section we discussed some elements of the design criteria relative to the logic technology and interconnect properties that permit the classification of hybrid layouts as simple, lumped element, or transmission line structures. In this section we shall examine interconnect criteria in more detail relative to specific hybrid circuit technologies. The parameters unique to all hybrid layouts can be defined as follows:

$C_L$ = Capacitance per unit length

$R_L$ = Resistance per unit length

$L_L$ = Inductance per unit length

$\tau_{pd}$ = Propagation delay per unit length

$C_{CL}$ = Line-to-line coupling per unit length

$C_{CR}$ = Line-to-line crossover capacitance per unit area

In addition to these basic parameters, parasitic elements due to line discontinuities at bond pads, lead inductance (for c/w attach) and vias between lines must be considered.

For the design of transmission line interconnects the parameters listed above are adequate to determine the required transmission properties, such as Zo, attenuation and phase constants, reflection coefficients, and line-to-line isolation. In all cases a combination of microwave and pulse response measurements can be used to experimentally validate any proposed analytical models.

In general, the myriad of hybrid substrate technologies can be grouped into one of three classes.

- Thick film (conductors and dielectrics)
- Laminated (thick film conductors)
- Thin film (conductors and dielectrics)

A brief overview of some specific technologies is shown in Figure 11. Some of the key electrical parameters for these structures will be described in the following sections.

| MULTILAYER HYBRID TECHNOLOGY | DIELECTRIC/$\epsilon_r$ | DIELECTRIC THICKNESS ($\mu$m) | DIELECTRIC PROCESS | METALLIZATION PROCESS | LINEWIDTH MINIMUM ($\mu$m) | LINE IMPEDANCE - Zo (MICROSTRIP) | LINE CAPICITANCE $C_L$ (Pf/cm) |
|---|---|---|---|---|---|---|---|
| SCREENED & FIRED THICKFILM | GLASS/CERAMIC/ 8-10 | 5-50 | SCREEN PRINT OR TAPE | SCREEN PRINT | 100 | 10-50 | 2-10 |
| THIN FILM ON ALUMINA | $SiO_2$/4 | 0.1-10 | SPUTTERED, PYROLITIC | EVAPORATED, SPUTTERED | 12 | 10-100 | 1-10 |
| CERAMIC GREEN TAPE | $Al_2O_3$/8-9 | 100-400 | GREEN SHEET | SCREEN PRINT | 125 | 50-100 | 1-2 |
| POLYIMIDE | KAPTON/3,4 | 25-50 | FILM | LAMINATE, ELECTROPLATE | 25 | 50-100 | 1-2 |
| THIN FILM | SAPPHIRE/10 $Al_2O_3$-TiC | 500 | POLISHED WAFER | EVAPORATED, SPUTTERED | 5 | 100-200 | 0.5-1 |

Figure 11 - Properties of Multilayer Hybrid Interconnections

## Thick Film

In the thick film hybrid technology the interconnect is fabricated by screen printing sequential conductor and dielectric layers onto an alumina ceramic or porcelainized steel substrate. Typical screenable dimensions are 10 mil wide conductors on 20 mil center and 16 x 16 $mil^2$ vias for interconnect feedthroughs through the dielectric. Conductor and dielectric layers are typically 0.5 to 1.2 mils thick.

In some cases, where a higher interconnect density is desired the first layer (and possibly the second layer) of interconnects can be photolithographically masked and etched to produce line widths of 4 mils on an 8 mil grid. However, subsequent layers must be screen printed, yielding line widths in the range of 8 to 10 mils on 16 to 20 mil grids. Thus, the distributed line capacitance for the first (and second) layer may be reduced by a factor of two over those of subsequent layers. This does not normally add any significant electrical performance improvements because in the general x-y routing of signal lines only a portion of a signal path will have narrower line segments.

The distributed line capacitance of a thick film hybrid associated with all signal lines can be simply represented by a "parallel plate" capacitor. Line conductors are typically 0.5 mil thick and the insulating screened dielectrics are typically 1 to 1.2 mil thick, with a relative dielectric constant of 10.

The signal line capacitance is thus given by:

$$C\ell = \frac{\epsilon_I W}{X_I} \text{ f/cm}$$

where

$$\epsilon_I = 10\epsilon_o = 0.885 \text{ pF/cm}$$

$$W = 10 \text{ mils}$$

$$X_I = 1 \text{ mil}$$

thus

$$C_\ell = 8.85 \text{ pF/cm}$$

The signal line resistance is reasonably low, and can be calculated as follows:

$$R_\ell = \frac{\rho}{tw} = \frac{\rho_s}{W} \ \Omega/\text{cm}$$

where

$$\rho s = \frac{\ell}{t} = \text{sheet resistance (ohms/square)} = 3 \text{ mil } \Omega$$

$$W = 10 \text{ mils} = 2.54 \times 10^{-2} \text{cm}$$

thus

$$R_\ell = 0.12 \ \Omega/\text{cm}$$

The capacitance may be reduced somewhat for a 4 mil wide etched layer to approximately 4 pF/cm. However, because of general x-y routing this would translate to a best case of only 6 pF/cm.

In any case, the distributed line capacitance for this structure is very simply related to the line width and dielectric thickness. The distributed resistance is very small and, in most cases, can be neglected. The distributed line inductance for this structure is very low and is simply given by

$$L_\ell = \mu_o \frac{X_I}{W} \text{ h/cm}$$

where

$$\mu_o \equiv \text{dielectric permeability} = 4\pi \times 10^{-9} \text{ h/cm}$$

thus

$$L_\ell = 1.26 \text{ nh/cm}$$

Normally, this inductance can be neglected for routing programs utilizing this technology. In fact, since the inductance is so low this substrate technology, as described, cannot be used for high speed transmission. The equivalent transmission line impedance is given by

$$Z_o = \left(\frac{L}{C}\right)^{1/2} = 12\Omega$$

Another factor to be recognized for this technology is that since the line capacitance is so high, hybrid interconnects must normally always be treated as lumped element loads. Some of the benefits derived using this technology are the minimization of line-to-line coupling and the elimination of line cross-over capacitance. Also, since the line widths are the same as bonding pads, termination discontinuities are minimized.

In some cases for the thick film substrates an attempt is made to reduce the inherently high line capacitance by avoiding the overlap of ground or power planes. Although this results in a reduction of inherent line capacitance, it increases adjacent signal line couplings. Microwave analysis techniques exist to provide coupling predictions.

Laminated Substrates

Laminated substrates using ceramic or polyimide layer stacks can reduce the inherent line capacitance by virtue of a thicker dielectric spacing between layers. As an example, in a laminated ceramic process 92 to 96 percent alumina is cast into a sheet having a thickness controlled from 5 to 40 mils. This cast unfired ceramic tape is die punched into uniform pieces containing via feedthroughs and alignment holes. Each layer is metallized by screen printing. The ceramic sheets are stacked, pressed and fired to produce a monolithic one piece body.

Laminated ceramic interconnects normally have the same 20 mil typical pitch line-density and via feedthrough area limitations described above for the thick film technology. One additional limitation of ceramic is the high camber of over 4 mils per inch in the fired part. For a typical laminated assembly where dielectric thicknesses of 10 mils are used between alternating layers of signal and ground or power planes a distributed capacitance somewhat lower than that for the screened thick film approach can be achieved. Using stripline analysis techniques, a distributed capacitance of 3.5 pF/cm was calculated. This can be reduced somewhat if the dielectric spacing is increased. However, a very thick substrate will be quickly obtained, limiting heat transfer and introducing additional fabrication constraints. As an example, the distributed line capacitance will only be reduced to 2.4 pF/cm if the dielectric layer thickness is doubled.

These capacitance values were calculated using standard stripline equations. For stripline structures the line-to-line coupling capacitance cannot be neglected as was done for the previous thick film structure. A number of microwave analysis techniques exist to quantify this capacitance.

## Thin Film Substrates

A thin film technology can be conceived in which a reasonably high interconnect density can be achieved with an inherently low distributed line capacitance. The characteristics of this technology will be discussed here to show its applicability to the emerging VHSIC technologies.

The configuration proposed for a high density thin film hybrid substrate is shown in Figure 12. Sapphire is shown as the substrate base.

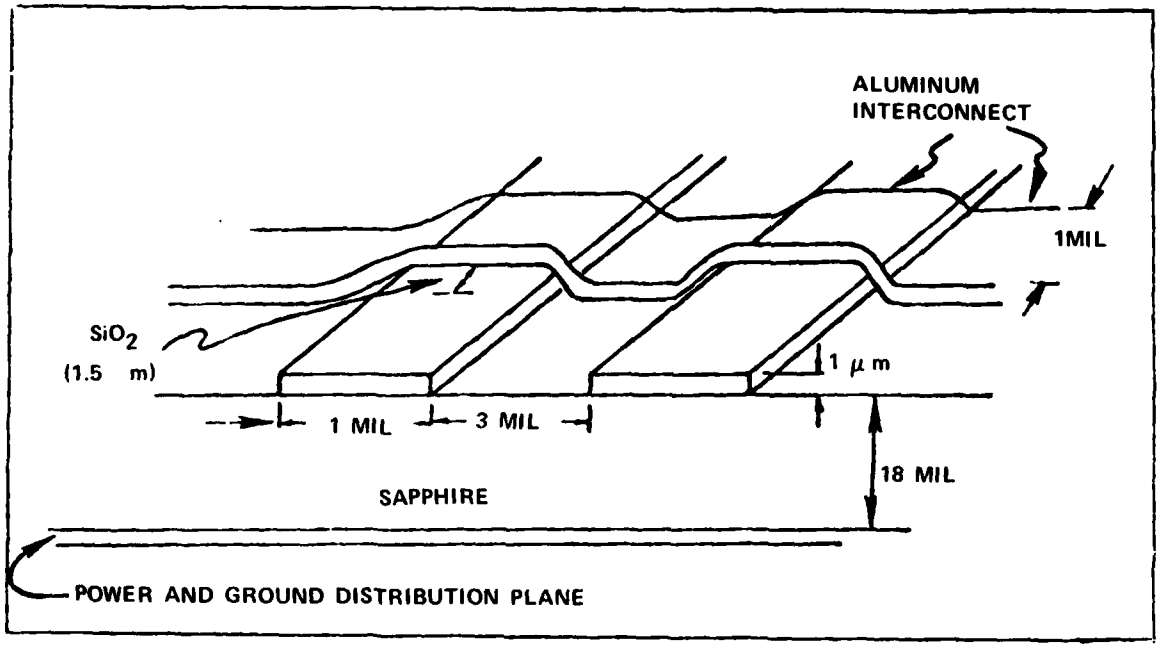



Figure 12 - Illustration of High Density Thin Film Hybrid Substrate

At most, two x-y signal interconnect layers are defined on the top surface of the sapphire substrate. These are 0.5 to 1 mil wide lines on 4 mil centers. Power and ground distribution planes are defined onthe bottom side of the wafer and are brought through the sapphire at selected areas in the vicinity of a chip site.

The technique used to calculate the distributed signal line capacitance for this structure has been described in a previous paper, see Reference (4). The referenced paper considered the use of fine line structure on sapphire for very high speed digital transmission at gigahertz clock rates. For proposed VHSIC technologies operating at frequencies below 200 MHz, controlled impedance transmission is often not required within the limited area defined

on a hybrid. The emphasis here is towards a low line capacitance in order to minimize the physical size and power dissipation of on-chip output drivers.

The calculation of the distributed line capacitance can be accomplished with the aid of Figure 13 and the analysis technique described in Reference (4). In Figure 13, the distributed capacitance contributions shown consist of line to bottom plane, $C_L$, line to line, $C_C$, and line crossovers, $C_{CR}$. $C_L$ and $C_C$ cannot be calculated separately, but can be determined from a set of interdependent potential-charge equations. Such a set of equations is as follows:

$$V_1 = A_{11} Q_1 + A_{12} Q_2 + \ldots\ldots + A_{1n} Q_n$$

$$\vdots$$

$$V_N = A_{n1} Q_1 + A_{n2} Q_2 + \ldots\ldots + A_{nn} Q_n$$

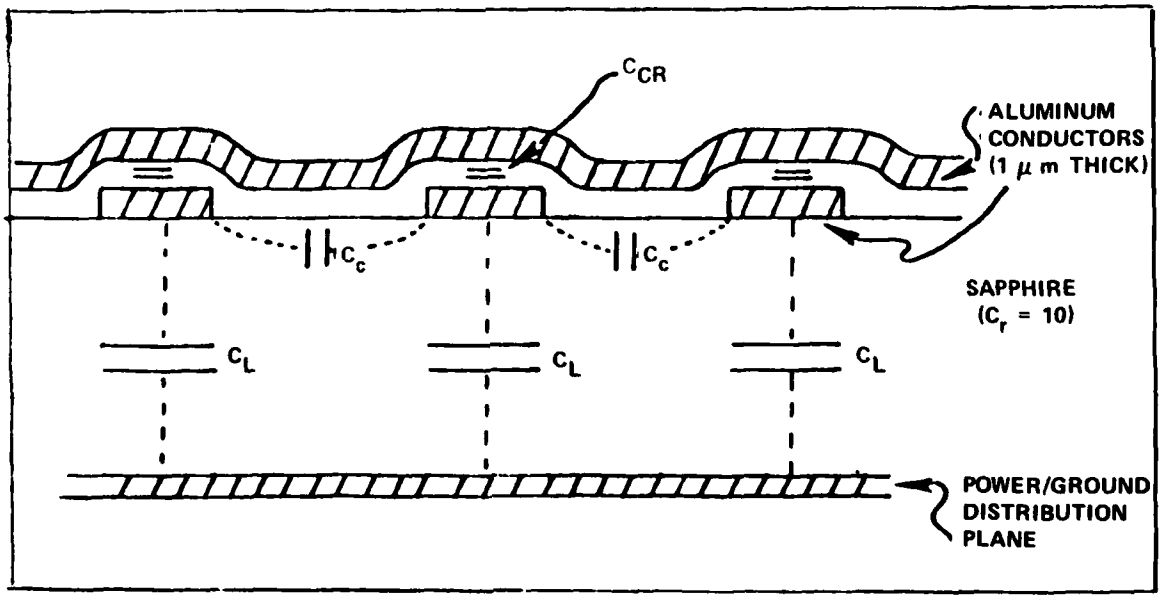



Figure 13 - Distributed Capacitance in Fine Line Interconnection Structure

For the simplest case only one line element would exist. The distributed capacitance for this condition is (Reference (4)).

$$C_D = 0.56 \text{ pF/cm}$$

For two line elements separated by 4 mils the distributed line capacitance is

$$C_D = 0.7 \text{ pF/cm}$$

For three line elements, each separated by 4 mils the distributed line capacitance is

$$C_D = 0.74 \text{ pF/cm}$$

When a number of line elements are in parallel, the distributed line capacitance for one of the elements approaches

$$C_D = 0.76 \text{ pF/cm}$$

To each of these distributed line capacitances must be added the lumped element contributions due to crossovers. For the structures being considered here, each crossover contributes approximately 0.015 pF. For a typical hybrid layout, the average number of crossovers is approximately 20, yielding a total crossover capacitance of 0.3 pF.

Although the capacitance of these fine line structures is much lower than that for the thick film structure, the line resistance is much higher. As indicated in Figure 12, the metal thickness is only 1 μm. For these lines we therefore have

$$R = \frac{\rho}{tw} = 11.2 \ \Omega/\text{cm}$$

where

$\rho = 2.8 \ \mu\Omega\text{-cm}$ (Aluminum)

$t = 1 \ \mu\text{m}$

$W = 25 \ \mu\text{m}$

This combination of line resistance and distributed capacitance represents the load elements for the off-chip output drivers.

Effect of Substrate Technology on Chip Driver Toggle Rate

Consider how the performance of a certain device technology can be influenced by the choice of the hybrid substrate technology. CMOS/SOS is one of the various device technologies being considered for VHSIC. This device technology can be used for very large scale functional logic where a large number of I/O interfaces to the chip are planned. Such chips may have as many as 32-bit wide I/O ports.

The typical output of a simple CMOS/SOS driver is shown in Figure 14. An actual output driver circuit will normally consist of more than one stage in order to minimize the loading effect on the internal logic. However, the simple one-stage output can be analyzed for comparative purposes.

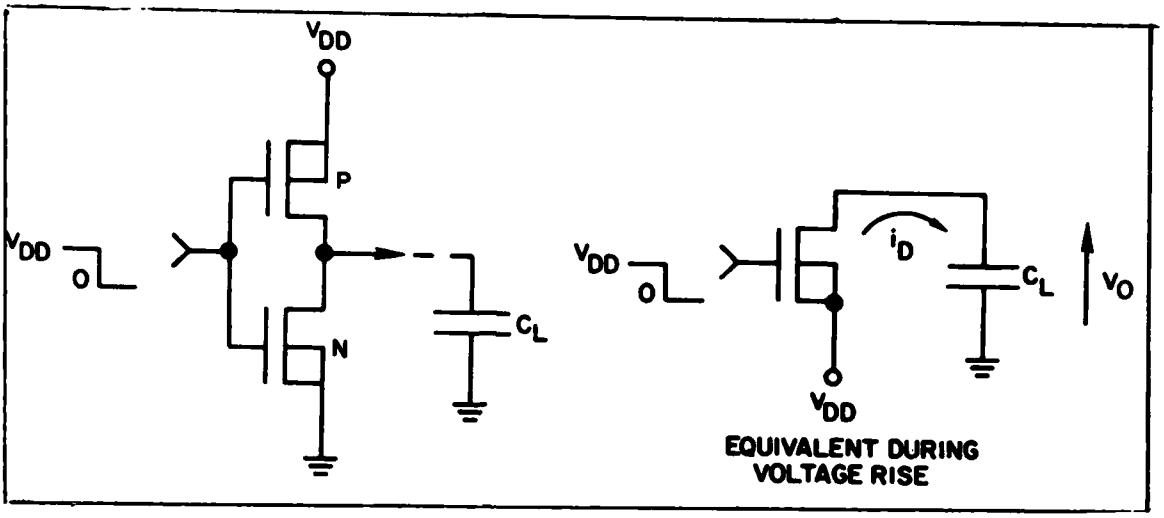



Figure 14 - CMOS/SOS Output Stage

For the single stage we may assume that the input transition from $V_{DD}$ to 0 V occurs rapidly so that the primary charging of the output load capacitance through the p-channel device takes place after the n-channel device is cut off. Thus, the p-channel device conducts primarily in the voltage-saturation condition. Its transient current $i_D$, is given by:

$$i_D = \frac{\mu_p \epsilon_{ox}}{2 x_{ox}} \left(\frac{W}{L}\right)\left(V_G - V_T\right)^2 = C_L \frac{dv_o}{dt}$$

where

$\mu_p$ ≡ p-channel carrier mobility = 200 $cm^2/v\text{-}s$

$\epsilon_{ox}$ ≡ oxide permittivity = $4\epsilon_o$

Xox ≡ gate oxide thickness = 800 Å

$\frac{W}{L}$ ≡ width-to-length ratio

$V_G$ ≡ gate voltage during charging = $V_{DD}$

$V_T$ ≡ p-channel threshold voltage = 1v.

$C_L$ ≡ hybrid load capacitance

Solving for $d\nu_o/dt$ and substituting the above quantities, we have

$$\frac{d\nu_o}{dt} = \frac{4.42 \times 10^{-6}}{C_L} \left(\frac{W}{L}\right)\left(V_{DD}-1\right)^2 \quad v/s$$

For a W/L ratio of 200 and $V_{DD}$ = 10 V we obtain

$$\frac{d\nu_o}{dt} = (7.2 \times 10^{-2})/C_L$$

Referring to the last sections, the load capacitance for thick film hybrid (TFH) was determined to be $C_L$ = 8.85 pF/cm, and for laminated ceramic (LCH) it was $C_L$ = 3.5 pF/cm. The thin film hybrid yielded $C_L$ = 0.76 pF/cm, and $C_{CR}$ = 0.015 pF. For an average of 5 cm run length on a typical hybrid circuit, the peak charging rates for lines with 20 crossovers are:

Thick Film Hybrid - $\frac{d\nu_o}{dt}$ = 1.6 V/ns

Laminated Ceramic Hybrid - $\frac{d\nu_o}{dt}$ = 4.1 V/ns

Thin Film Hybrid - $\frac{d\nu_o}{dt}$ = 17.5 V/ns

A peak charging time constant can be expressed as the reciprocal of these values.

$\tau_{TFH}$ = 0.63 ns/V

$\tau_{LCH}$ = 0.25 ns/V

$\tau_t$ = 0.055 ns/V

Since the complete transition does not occur at this rate, an effective time constant can be approximated by twice these calculated peak values. Therefore,

$(\tau_{TFH})e = 1.26$ ns/V

$(\tau_{LCH})e = 0.5$ ns/V

$(\tau_t)e = 0.11$ ns/V

For a complete transition from 0 to 10 V the switching times are 12.6 ns, 5 ns, and 1.1 ns, respectively, for each hybrid technology.

Assuming a balanced output transistor design, at least two such transition times are required to define an output pulse. Therefore, the maximum toggle rates for this driver are 20 MHz, 50 MHz, and 200 MHz, respectively, depending on the substrate technology.

Influence of Hybrid Technology on Chip I/O Design and Performance

It is generally accepted that chip I/O loading is critical for high impedance technologies such as NMOS and CMOS/SOS. We demonstrated above how the interconnect load capacitance has a significant effect on the ultimate toggle rate of a CMOS/SOS output driver. Let us now reconsider this problem with respect to the influence output loading has on driver power dissipation. We shall show that chip output drivers can be redesigned to be smaller and less power consuming at a fixed clock rate.

In cases where high capacitance loads are anticipated, such as would be experienced for thick film hybrids on PC boards, on-chip output drivers must drive an output load of at least 50 pF. One such driver design for a CMOS/SOS logic chip is shown in Figure 15. It is a three-stage driver that occupies over 100,000 $\mu m^2$ of chip area.

Raytheon has designed, simulated and fabricated the driver shown in Figure 15. Its simulated response is shown in Figure 16. The circuit simulation data agrees reasonably well with the simple calculations presented above. Note that the switching time is 11 nsec and the average power at 5 MHz is 25 mW.

If the same driver had a reduced load of only 5 pF, as would be typically presented by a thin film on sapphire hybrid technology, then the average power at a 5 MHz clock operation would be only 2.2 mW. This can be seen from the logic simulation shown in Figure 17 or simply inferred from the power relation of $P \sim CV^2f$ (C has been reduced by a factor of 10).

Since the rise and fall times of this output driver with a small load are reasonably fast, it is conceivable that the available driver power is excessive. In order to explore this, the original driver design was simplified by eliminating the last stage of the driver design shown in Figure 15. The chip area required by this two stage driver is about one-half that of the original three-stage version. The simulated response of this driver with a

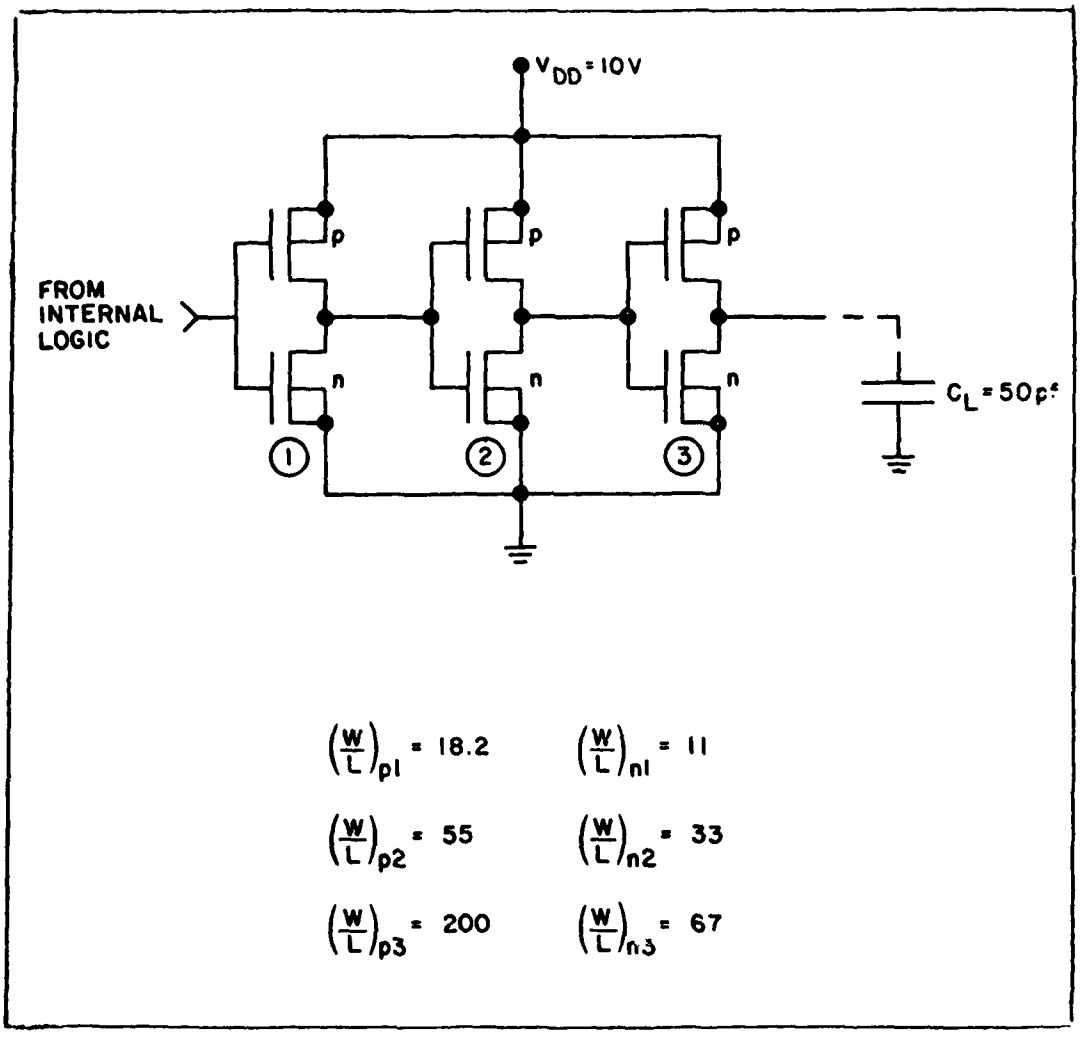



Figure 15 - Electrical Equivalent of Three-Stage CMOS/SOS Output Driver

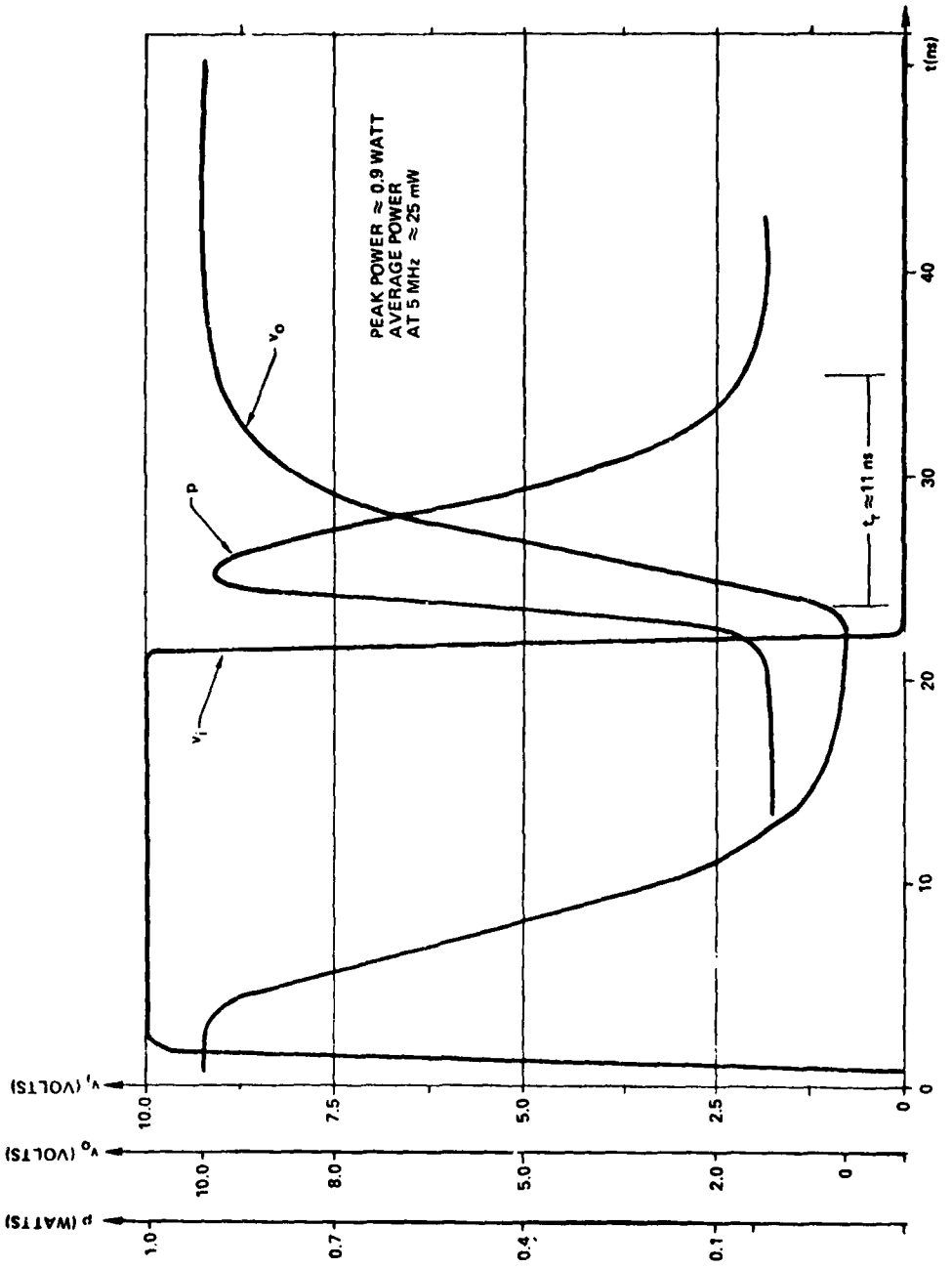



Figure 16 - Computer Simulation of Three-Stage CMOS/SOS Driver: $V_{DD}$ = 10 V, $C_L$ = 50 pF

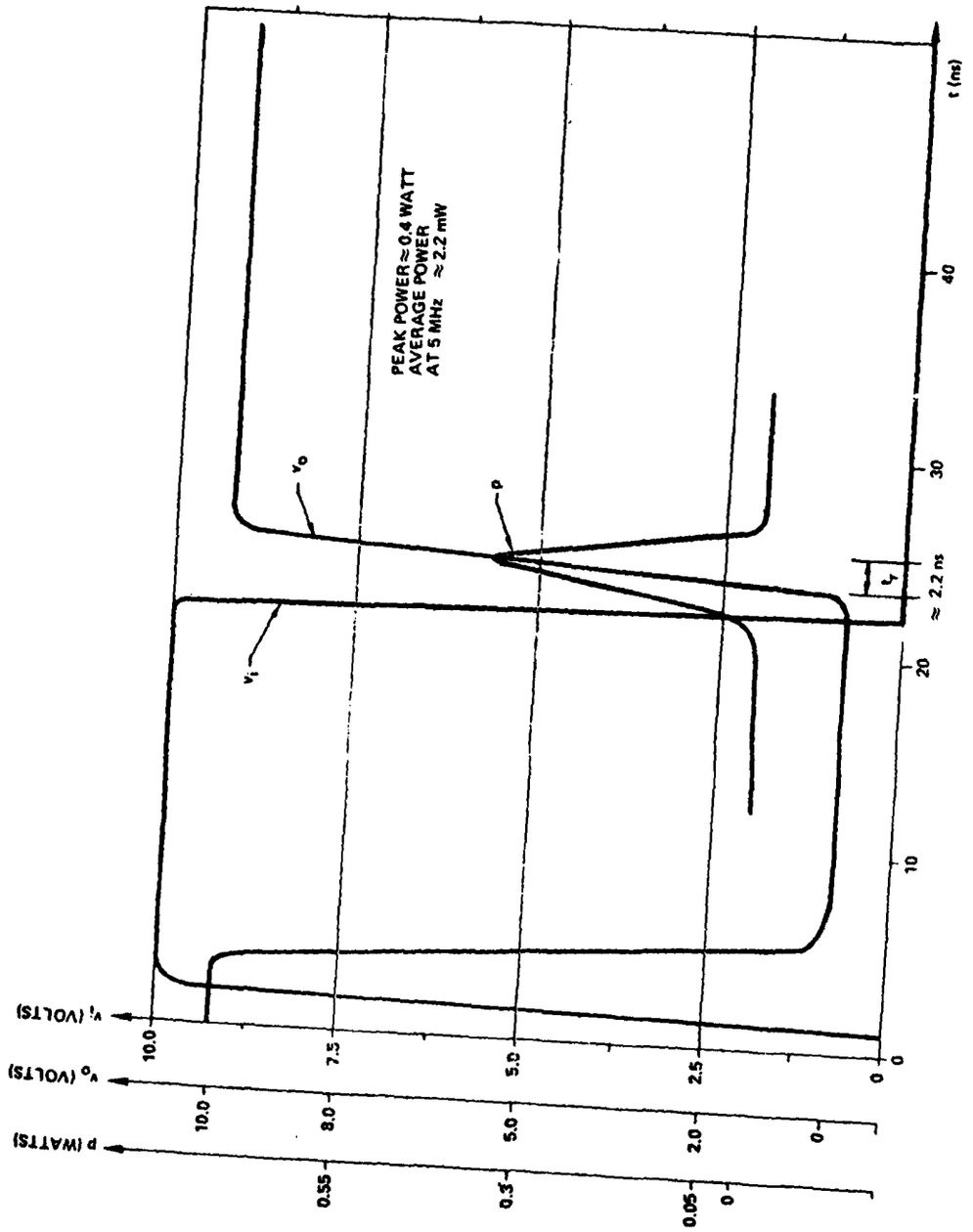



Figure 17 - Computer Simulation of Three-Stage CMOS/SOS Driver: $V_{DD}$ = 10 V, $C_L$ = 5 pF

5 pF load is shown in Figure 18. Note that the average power dissipation now is only 1 mW, and the rise time is approximately 3 nsec compared with 2.2 nsec of the three-stage driver. If we are still only concerned with 5 MHz operation it is conceivable to reduce the power supply level to 5 V. This condition was also simulated, as shown in Figure 19. Note that the rise time was increased to only ~ 6 nsec, but the power dissipation is reduced to 0.25 mW ($\sim CV^2f$).

Therefore, we have been able to drastically improve the design and performance of the original chip output driver through a choice of hybrid technology and design that reduced the off-chip circuit load. The overall result was a reduction of output drive power by a factor of 100, a reduction of driver size by a factor of 2, and a rise time improvement of almost a factor of 2.

Concepts for Higher Level Packaging

As discussed previously, what is needed for the utilization of VHSIC is an integrated packaging approach based on our proposed narrow and short interchip connections of low capacitance. Figure 20 shows a sapphire substrate processed with fine line interconnects assembled into a conventional hybrid package. The hybrid packages are mounted onto a multilayer, transmission line, plug-in printed circuit module, as shown in Figure 21. Obviously, for more stringent future VHSIC applications, this approach suffers because of circuit delays caused by the longer line lengths on the PC board, through connectors and back plane wiring. Also, it is very difficult to achieve a high density transmission line connection with matched impedance connections at the male connector interface to the PC board and the female connector interface to the mother board.

Figure 22 shows a novel approach that dramatically reduces higher level interconnections by stacking sapphire substrates. This packaging concept provides an ideal signal environment for future VHSIC requirements. The devices are mounted on a sapphire substrate which has been previously attached to a glass ceramic board of Fotoceram* on a PC board. Figure 22 shows the use of a rectangular sapphire substrate, while Figure 23 displays a round sapphire wafer. This carrier provides a mounting base for the sapphire substrate as well as for the interconnections between stacked sapphire and carrier board. Conductors on polyimide tape connect the peripheral pads on the sapphire wafer to corresponding pads on the carrier board. From these pads, printed wiring conductors run to peripheral pads located on both sides of the carrier board which are used for interconnections between wafer assemblies. These connections between the various wafers and the external contacts on the module header are made with a connector ring containing resilent conductive or spring loaded metallic contacts.

*Trademark-Corning Glass Company

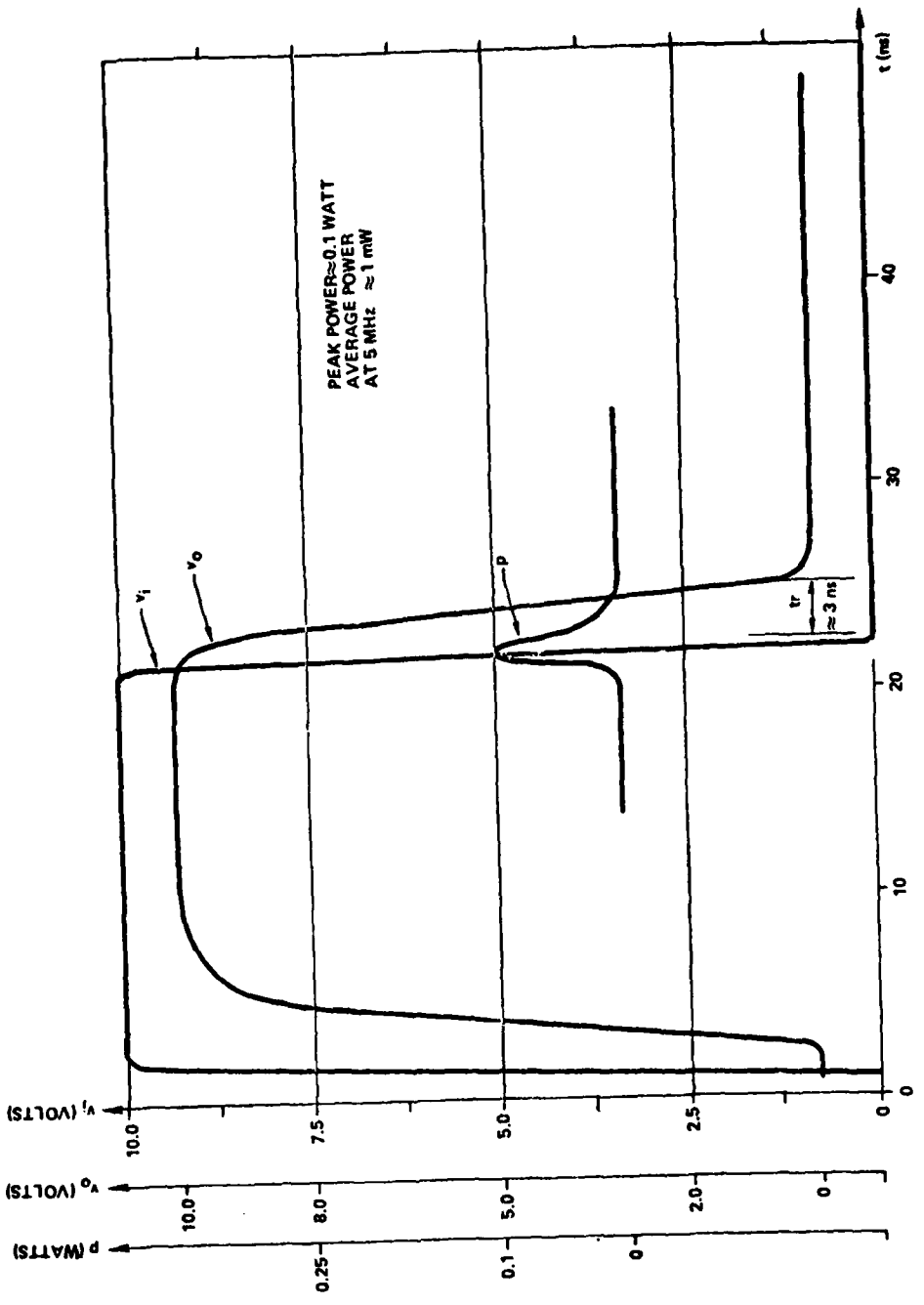



Figure 18 - Computer Simulation of Two-Stage CMOS/SOS Driver
$V_{DD}$ = 10 V, $C_L$ = 5 pF

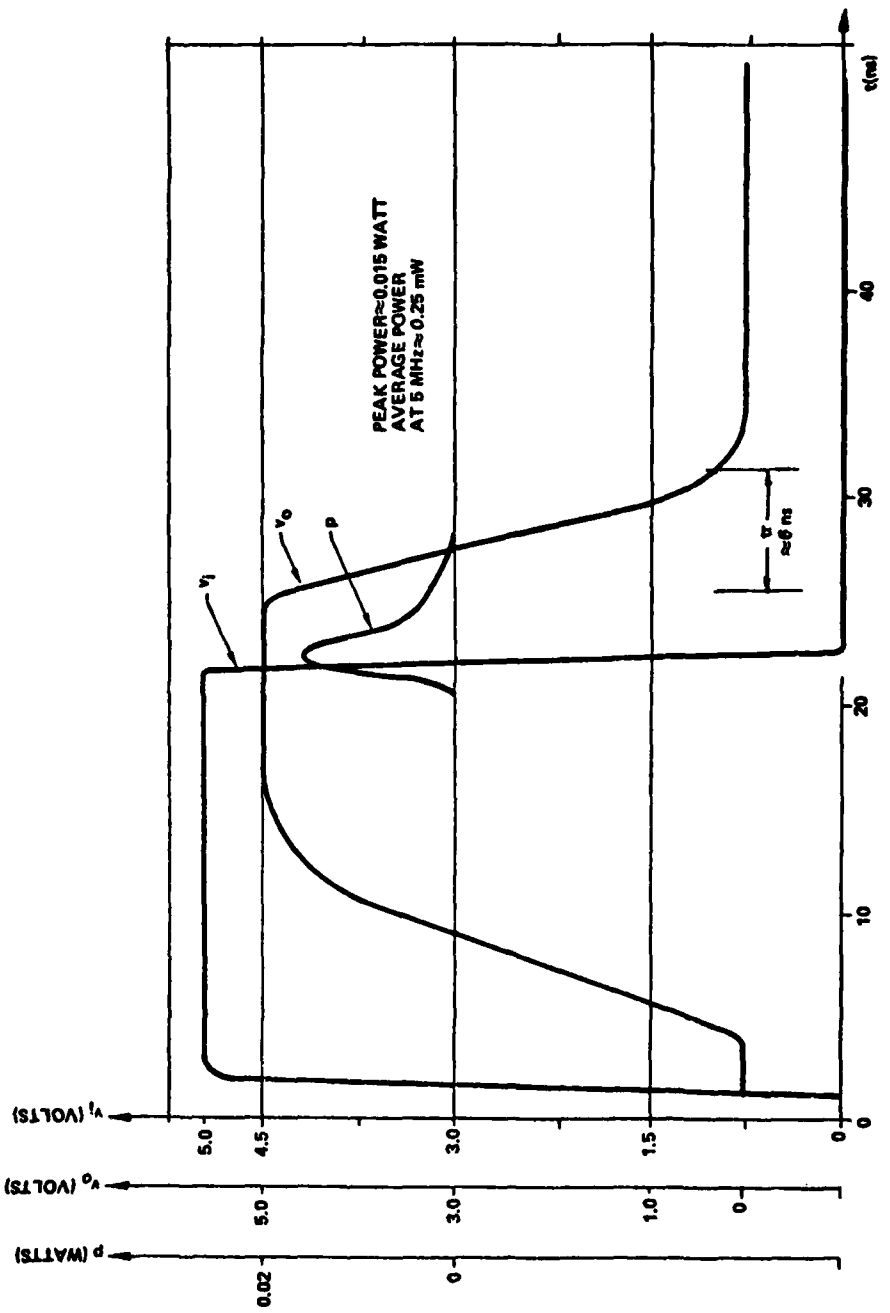



Figure 19 - Computer Simulation of Two-Stage CMOS/SOS Driver: $V_{DD}$ = 5 V, $C_L$ = 5 pF

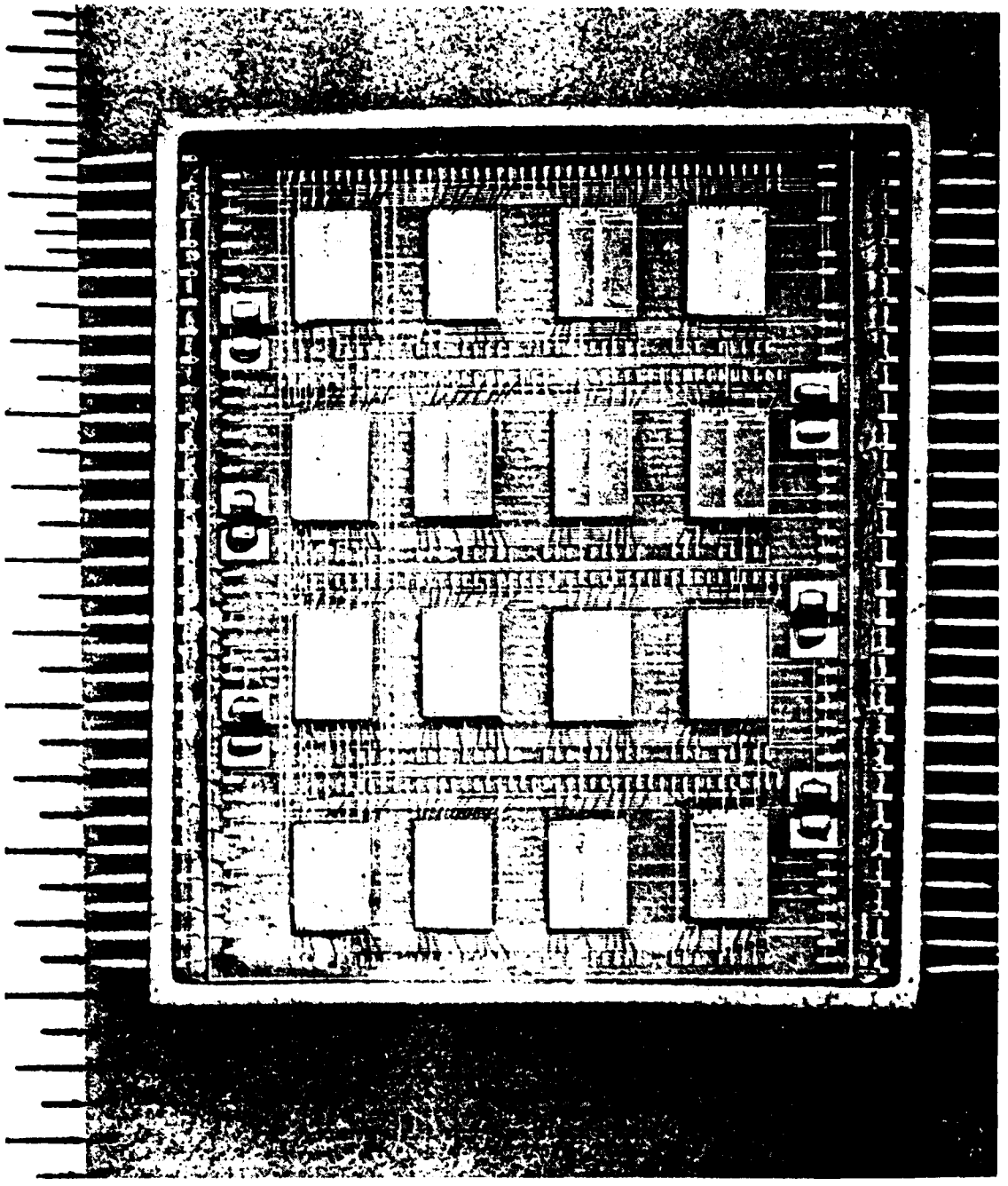


Figure 20 - Example of Thin Film - Two Layer Hybrid

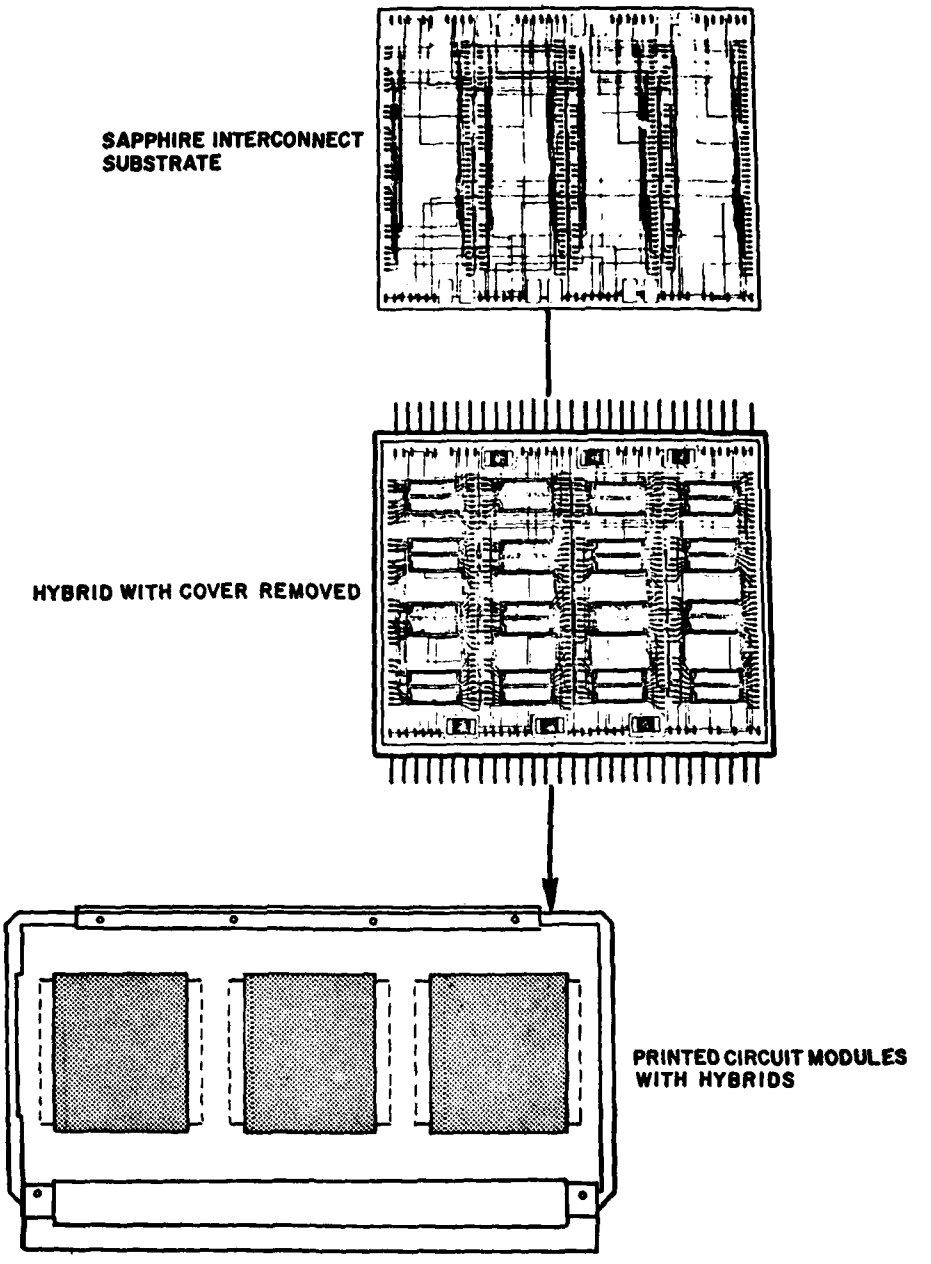



Figure 21 - Plug-In PC Module with Hybrids Containing High Density Two Layer Interconnects on Sapphire

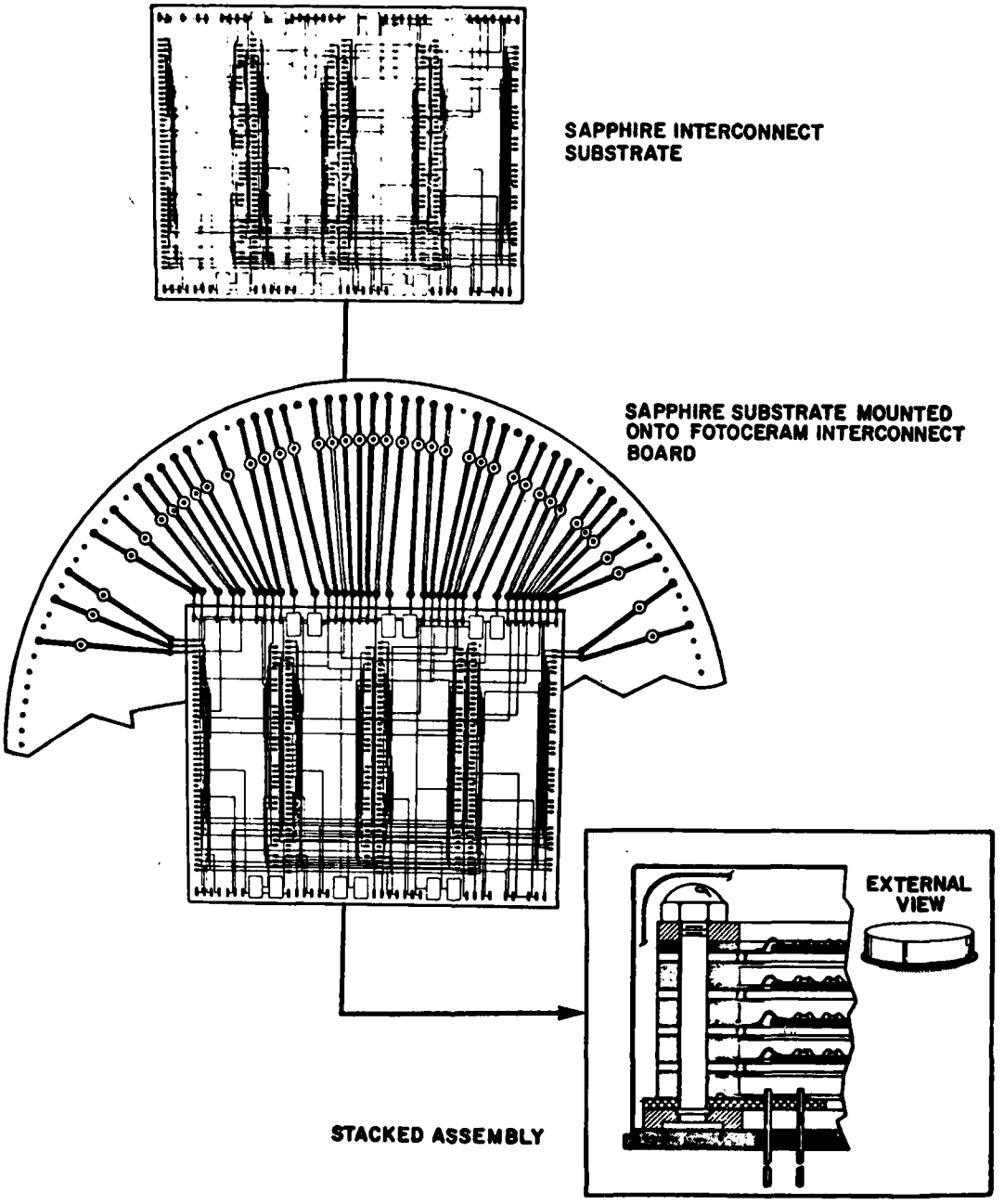



Figure 22 - Stacked Square Sapphire Substrate Approach

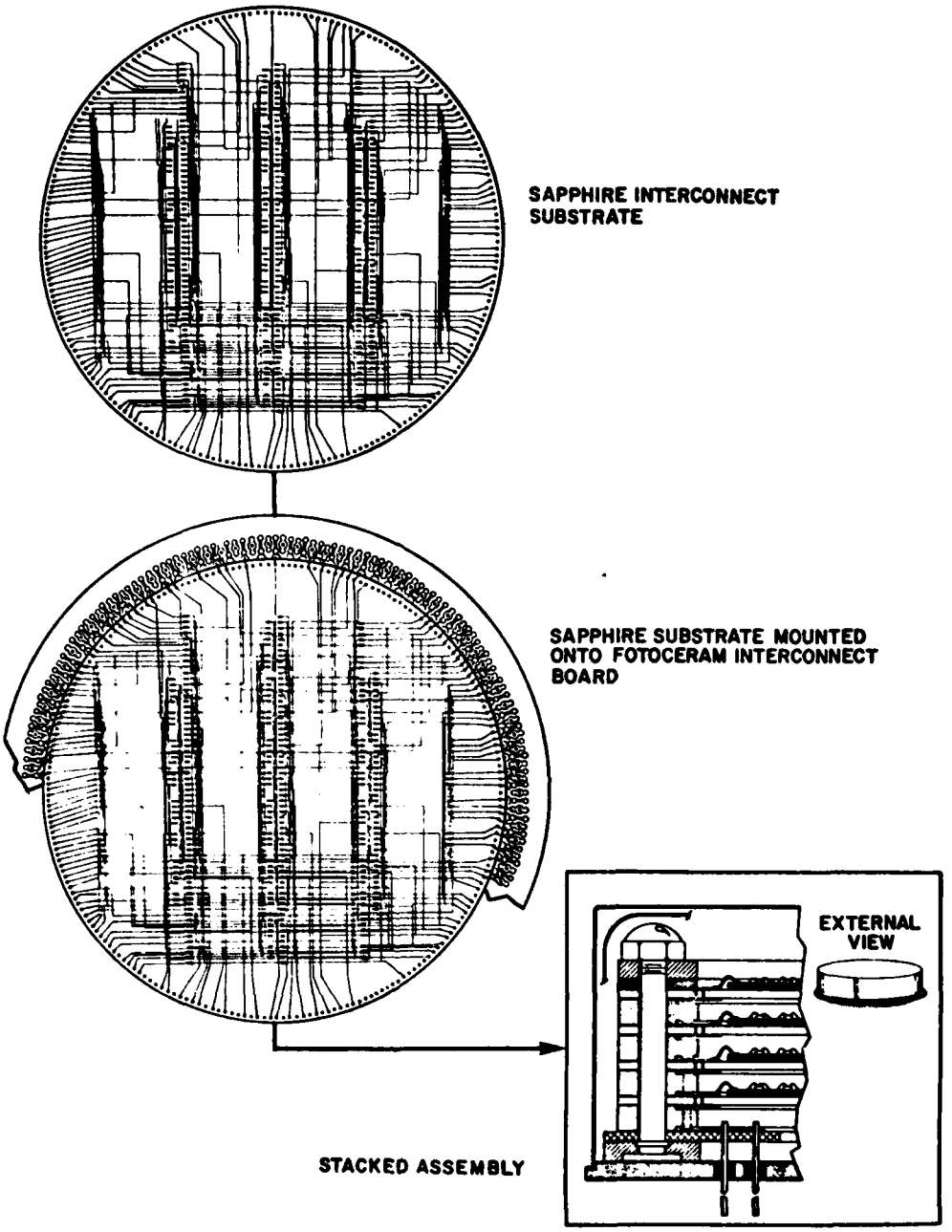



Figure 23 - Stacked Round Sapphire Substrate Approach

Mounting studs are pinned into the header and provide the means for indexing and supporting the wafer assembly. The module can be filled with a specified amount of fluorochemical to provide cooling for the VHSIC devices. The header subassembly is sealed with a gasket seal which provides ease of repair. An alternate method being considered is a weld seal. The entire VHSIC assembly in Figures 22 and 23 is shown with four substrate layers, but substrate layers can be added or removed as needed with minimum impact on the mechanical structure.

The use of a second interconnect carrier provides the option of using a number of smaller rectangular sapphire substrates as a substitute for the single three inch sapphire wafer. Such an implementation might increase assembly yield and facilitate testing, since the number of chips per carrier is reduced. Nonfunctional packaging modules have been build and checked successfully for electrical continuity through the wafer layers.

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# HIGH SPEED DIGITAL PACKAGING

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## ABSTRACT

Packaging digital logic for performance in the 250 MHz to 5 GHz range requires that special techniques be used in the areas of chip packaging, chip interconnection, and thermal management. Investigations in these areas have led to the synthesis of a packaging concept for a high speed digital avionics system. Particular techniques used are coplanar transmission lines, multilayer printed circuit hybrid substrates, ceramic chip carriers, a modular PC board/heatsink, and direct attachment of chip carrier packages to circuit board and heatsink.

## INTRODUCTION

This paper describes a packaging concept for a high speed digital avionics system. The concept represents a synthesis of the results of research into advanced packaging techniques for high speed, high density circuitry. The objectives of the packaging techniques are: to perform at digital logic rates of 200 MHz to 5 GHz, and analog rates up to 18 GHz; to accommodate devices of MSI or greater complexity; and to be versatile, modular, maintainable, reliable, and easily tested. Particular means of implementing these objectives have been the use of impedance matching interconnections, hermetic chip carriers, special materials for high speed circuits, and thermal management techniques for high power densities. The main topics of discussion are hybrid substrate manufacturing techniques, transmission line design, a high density chip carrier package, and a thermal analysis of a PC board module with chip carriers attached.

This paper is a result of the "High Speed Digital Packaging" program performed by TRW Defense and Space Systems Group and sponsored by the Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio under Contract F33615-78-C-1422. The objective of the program is to develop an integrated line replaceable unit level packaging concept optimized for today's state-of-the-art subnanosecond logic devices and faster devices that may become available in the next 10-15 years.

## High Speed Digital Packaging Concept

The design concept for a digital avionics packaging system which was evolved during the first phase of the program is shown in Figure 1.

First, a brief summary of the main components will be given. The half-ATR case in View A contains 16 PC board modules which are inserted from the sides and plug perpendicularly into a vertical mother board in the center of the case. Wire contact connectors, shown in View E, are fastened to the mother board. The modules are composed of a heat exchanger with a PC board bonded to each side, as shown in View C. On the PC boards are leadless chip carriers, attached by reflow soldering. The cross-section of a module in View D shows the heat exchanger core, PC board, solder joints and chip carriers. The PC modules slide into the case on guide rails, View B; are located by guide pins which insert into the connectors; and are locked into place by two screws which mount to the upper and lower air plenums. Cooling is accomplished by forced air which flows into the front of the upper plenum, down through all the modules in parallel, and out the back of the lower plenum.

Now a detailed discussion of the various system elements will be given, starting with the chip carriers, shown mounted on the PC modules in View C. Two sizes of carriers are used: a 1/2 inch x 1/2 inch single chip carrier with 84 pads, and a 1.2 inch x 1.2 inch carrier with 200 pads for up to four chips. Both chip carriers are designed for chip sizes up to .250 inch x .250 inch. A one inch square chip interconnect substrate is used in the larger carrier. This substrate is a multilayer polyimide structure with 6 mil vias, and is fabricated by the sequential lamination process. Both chip carriers have pads on 20 mil centers, which is double the normal density. This allows for shorter interconnect distances between chips, which is essential for high frequency signals.

The carriers are reflow soldered to matching pad patterns on the PC boards, as seen in the cross-section of View D. To improve heat transfer from the chip to the heat sink, there is a checkered metallization pattern plated on the chip carrier beneath the die cavity area. The PC board in this area is kept as thin as possible to present a minimum thermal resistance between the chip carrier and heat sink. To accomplish this, square islands are machined on the heat sink, with recessed channels running between them. These islands are in intimate contact with the PC board layers directly beneath the chip carrier die cavities. At this point there is a one mil layer of polyimide and a one mil layer of adhesive, for a total of two mils of insulation. Conductors can be routed beneath the carrier between these layers. However, most of the PC board conductors are routed in the multilayer matrix between the islands. The channels are deep enough to hold at least six layers of interconnect and wide enough to allow several conductors in parallel.

Each PC board module outline is approximately the size of a Navy standard electronics module: 2.25 inches x 5.62 inches. The PC boards on each face of the module can accommodate 12 of the single chip carriers or three of the four

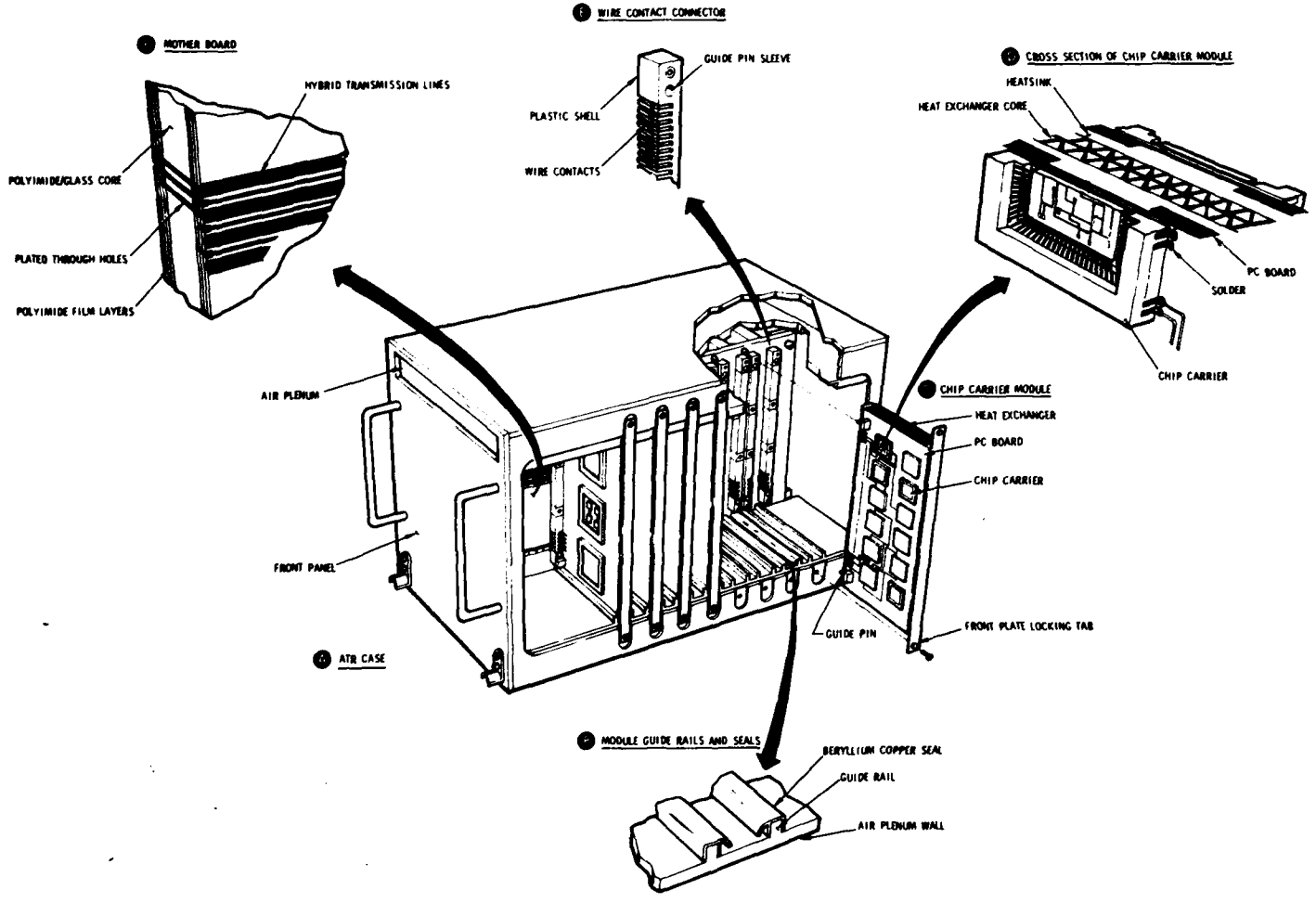


Figure 1. High Speed Digital Avionics Packaging Concept

chip carriers, for a total of 24 chips per module. With a maximum of four watts per chip, there would be 96 watts of total power dissipation per module.

The heat exchanger core is a specially selected copper core which gives optimum performance for a single pass heat exchanger. It is supported by the copper heat sinks and by front and back plates. The entire assembly is brazed together. Included on the heat sink on one side are bosses for the guide pins which locate the module relative to the connectors. To lock the modules into place, the front plate of the module extends upward and downward over the edges of the air plenums to allow it to be fastened with screws. Thus, each module is securely pinned at four corners while the edges are loosely supported by the guide rails, connectors and ATR side panels.

The mother board to module connectors are 90° wire contact connectors as shown in View E. They are screwed into the mother board after being located by means of a guide which mates with a hole on the mother board. The wire contacts are on .050 inch centers, and are supported by an injection molded plastic shell. As many as 75 contacts can be used on each side of the module, for a maximum of 150 I/O's per module. Each contact is a leaf spring which is deflected when the module is inserted between opposing connectors. The contact force is strong enough to prevent it from chattering during standard vibration testing.

The mother board itself is a polyimide multilayer PC board produced by sequential lamination. View F reveals its inner construction. It has a 1/16th inch thick reinforced polyimide core for rigidity. On each side are laminated six copper layers of polyimide film with acrylic adhesive. Hybrid transmission lines are used to control impedance and to minimize signal crosstalk. Connections from one side of the mother board to the other are made with plated through holes whose geometry is controlled to produce a 50 ohm impedance connection.

The mother board is fastened to flanges on the upper and lower air plenums by screws which are located at regular intervals along the length of the board. The guide rails for the modules are also machined into the air plenum. A slot between the rails allows air to flow freely from the plenum into the heat exchanger. Sealing is effected by nylon coated beryllium copper spring stock which is bonded to the guide rails and is deflected by the modules when they are inserted. For ease of insertion the leading edge of the module is chamfered at the point of entry. The air plenums are dip-brazed to a sheetmetal enclosure which is flanged for the removable side covers and front and back panels. On the front panel are mounted three circular connectors for power, ground and signal I/O's and a BNC connector for an 18 GHz analog input signal. Mounting hooks, handles, and an air inlet are the other features.

This concept provides high density circuitry in a modular, easily maintainable package. Individual chip carriers can be easily removed and replaced at a depot maintenance point after the pluggable PC module is removed and replaced in the field. High speed performance is assured by use of controlled impedance and high isolation transmission lines along with minimum discontinuity

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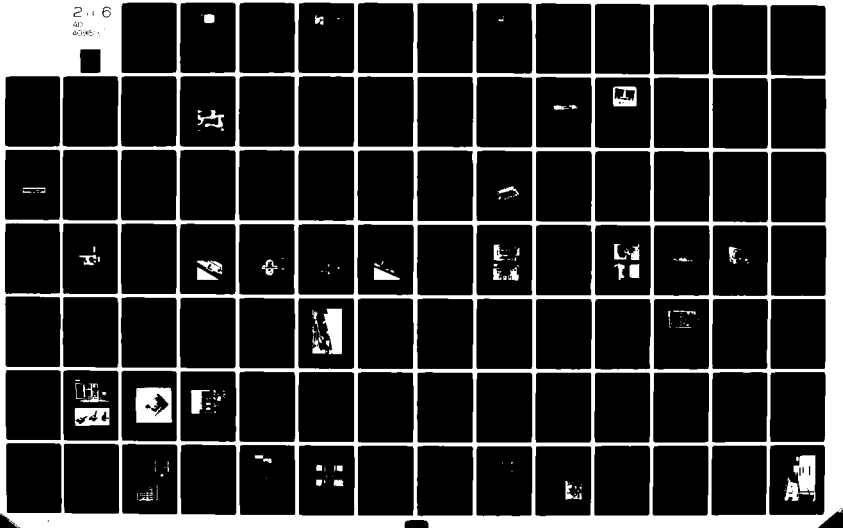


connectors and chip carriers. Reliability is enhanced by a PC module design which optimizes heat transfer from the chip to the cooling air.

The following sections will explain in greater detail the development of certain aspects of this packaging concept.

## Chip Packaging - Hybrid Substrate Techniques

TRW has developed circuitry operating with clock rates of 860 MHz using a polyimide interconnection substrate. This substrate was fabricated utilizing polyimide resin with the printed circuitry produced by the additive plating process. The substrate was manufactured by Pactel Corporation of Newbury Park, California. A photograph of the substrate bonded into a metal plug-in package appears in Figure 2. The primary advantage of this system is that vias can be produced down to 4 mils square.[1] Using conventional multilayer circuit board technology, plated through holes 13 mils in diameter would be the smallest size for vias. The ability to produce vias of 4 mils allows a much higher line density than can be obtained with the conventional multilayer approach. A further advantage is the fact that the vias can be blind, i.e. they do not go completely through the board. The ability to produce blind vias enhances the ability to produce high circuit density substrates since circuit lines can now be routed over or under the blind vias on other circuit layers. Another great advantage of this process is that integral copper posts can be plated up to form thermally conductive heatsinks beneath the chips. These advantages make this process far superior to conventional multilayer circuit boards for high speed interconnections where the requirement for short line lengths dictate the need for high circuit line density.

However, there are certain limitations to this process. The maximum number of conductive layers that can be fabricated is six. Also, the process is limited to polyimide resin. Other materials with lower dielectric constants would, therefore, be excluded from consideration. For example, a polyparabanic acid film manufactured by Exxon Chemical Company under the name of Tradlon has a dielectric constant of 1.6 and would be an ideal candidate for high speed applications. Propagation velocities approaching 80% the speed of light could be achieved with this material as a result of its extremely low dielectric constant.

It was considered prudent to investigate a back-up or alternate design for the interconnect system which would overcome the two limitations just discussed. An attractive alternate appeared to be the sequential lamination method. Figure 3 shows a cross section of a sequentially laminated PC board. The vias only go down to the layers to be connected, rather than going completely through the board as is done in a conventional multilayer circuit board. In this respect, the sequential method is similar to the polyimide/additive process just discussed. The difference is that a completely submerged via can be fabricated with the polyimide/additive processes, whereas in the sequential lamination method one end of the via must always come to the top surface. This limitation is not a serious one. An examination of multilayer boards that have been fabricated in the past reveals that very few

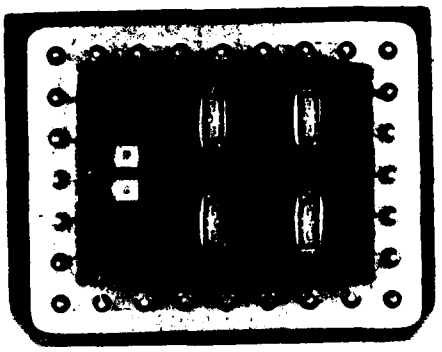


Figure 2

860 MHz Circuit Fabricated by Polyimide/Additive Process

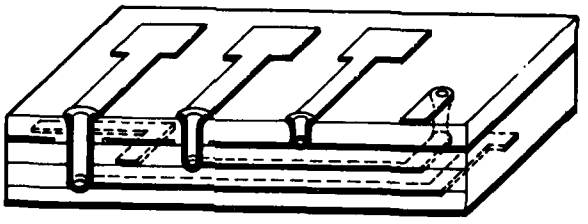


Figure 3

Cross-section of Sequentially Laminated PC Board

completely blind inner layer connections are required. However, it does appear that circuit line density can be slightly higher with the polyimide/ additive process due to the fact that circuit lines can run both under and over completely submerged vias, whereas with the sequential lamination method circuit lines can only run underneath the via since the top of the via must go to the surface. In either case, higher line densities can be obtained with both methods when compared to the plated through hole technique used in the conventional multilayer board fabrication process.

Another important factor in the sequential lamination technique is that only two layers of circuitry are connected at one time. No circuit edge connections are made to the barrel of the plated through hole as is done in conventional multilayer construction. Slight voids and plating irregularities, therefore, would not have a detrimental effect on the integrity of the connection. For this reason, a very reliable connection is made with the plated through hole.

The first experimental attempt of a sequentially laminated substrate was made with glass reinforced polyimide. A .004 inch thick layer of polyimide with 1/2 oz. copper on both sizes was laminated to four single-sided layers of .003 inch polyimide. The adhesive between layers was .003 inch thick glass-supported B-stage polyimide. The finished laminate contained six copper layers and was .033 inch thick. All copper was etched away except for circular pads for the plated-through-holes. These holes were drilled with a .006 inch diameter drill and plazed prior to laminating each additional layer.

A microsection of a typical plated-through-hole is shown in Figure 4. The hole is .033 inch deep, which gives it an aspect ratio of 5.5 to 1. As can be seen, the copper plating in the hole is continuous and consistent. The conclusion can be reached that very small plated through holes are feasible with aspect ratios up to at least 5.5 to 1.

Due to the fact that 6 mil and smaller diameter holes are rather difficult to produce by mechanical drilling, alternate hole drilling methods were examined. The most promising approach to small hole drilling appears to be the laser. Of the many types of lasers available the $CO_2$ type with a wavelength of 10.6 microns appears the best suited for this application. The reason for this suitability is that most dielectric materials are absorbtive at this wavelength and are, therefore, amenable to the laser drilling technique.

Preliminary attempts at laser drilling polyimide have produced .005" diameter holes. However, charring occurred during the drilling procedure. Similar results were achieved with Triazene. It appears that this effect is a property of the material rather than of the process. Further tests have been conducted on various dielectric materials using a 50W, $CO_2$ industrial laser. The minimum beam diameter of this laser is 0.005", although with a collimating attachment the beam diameter could be reduced to 0.0015". Single shot operation was employed with a pulse width of approximately 200μs in duration. The power output was then varied in order to determine the effect of this variable

Figure 4

.006 Inch Diameter PTH Through .033 Inch Thick Polymide Substrate

Figure 5

Laser Drilled .006 Inch Diameter Hole in Closed Cell Tradlon ($\varepsilon$=1.6)

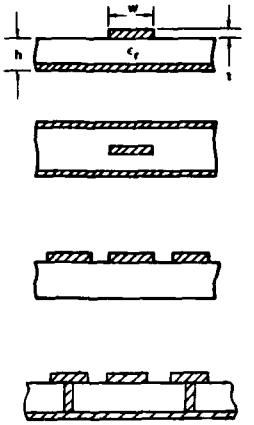



Figure 6

Wiring Geometries for Transmission Lines

on hole size and quality (smoothness). The quality of the hole, as determined by optical microscopy, did not seem to be greatly affected by the output power. However, the hole size decreased as the power decreased. Finally, at the lowest power, 4 watts average, 20 watts peak, hole diameters of between 0.006" and 0.0085" were produced. Figure 5 shows an example of a 6 mil laser drilled hole. The materials used in this investigation were FEP, TFE, Polyimide, Tradlon clear, Tradlon opaque, and Acrylic. The acrylic was included since it is often used as an adhesive when bonding copper to a dielectric material. The results of this investigation were that all the materials could be laser drilled but that polyimide and Triazene charred and would require a cleaning operation before reliable copper plating could be obtained.

Circuit Board Materials

In choosing a material for a high frequency circuit substrate, several requirements must be met. The material should have a low dielectric constant to minimize signal transmission delays, should be readily available in thicknesses down to .001 inch to allow the maximum number of layers for a given plated through hole aspect ratio, should have high heat resistance to withstand soldering and wire bonding, and should be proven amenable to normal printed circuit board manufacturing processes. The materials available include epoxy-glass; glass-reinforced triazine; glass-reinforced and unreinforced polyimide and teflon; and unreinforced clear and opaque Tradlon. Most of these are unsuitable for the following reasons:

- None of the glass reinforced materials are available in .001 inch thicknesses, which puts greater restrictions on the number of layers that can be plated through for a given hole size.
- Teflon film is highly unstable at elevated temperature and is therefore ruled out.
- Tradlon opaque film with a dielectric constant of 1.6 is the most promising of the alternate materials, but is still in the development stage.

Polyimide film is the material of choice due to the following advantages:

- Relatively low dielectric constant
- Readily available to 1 mil thickness
- Proven material for PC board use
- Processing technology is well developed
- Can withstand soldering temperatures

## Transmission Line Design

The physical environment of a high speed logic system has a great effect on the system's performance. For a system of any significant complexity the entire logical function cannot be implemented on a single chip. Some method must be used to move signals between the LSI building blocks. At the signal speeds of interest, the electrical delays associated with the physical distance between active elements can range up to several hundred percent of a clock period. For effective high speed logic design, these delays must be well understood. If possible, they must be exploited as a design tool in future systems.

The three most common geometric configurations for printed circuits are shown in cross-section in Figure 6, along with a fourth type. Microstrip is the term used for a copper strip on the surface of a dielectric sheet separating it from a copper ground plane. Microstrip is relatively easy to manufacture and difficult to analyze. The difficulty arises because of the combination of two dielectrics near the conducting metal.

Stripline is the technique used on interior layers of a multilayer board. It is a metal strip suspended between two ground planes. Analysis of this configuration is much simpler than for the microstrip because the dielectric medium is homogeneous.

The third configuration in common use is called coplanar. The signal line is placed between two surface ground strips. This is similar to the microstrip except that the surrounding ground strips serve to isolate the signal from its neighbors. The coplanar line is useful in cases where more substantial shielding is too cumbersome, such as near a board edge connector. It has not been treated extensively in the literature and requires further research to be well understood.

The last configuration is a modified coplanar line with a ground plane and a "picket fence" configuration of plated through holes connecting the surface ground conductors to the plane. This type of conductor gives superior impedance and isolation control.

It appears that the coplanar and hybrid transmission lines offer the best configurations with which to minimize the discontinuities caused by an intervening connector between the mother and daughter board. Since both ground and signal are on the same surface, discontinuities between the mother and daughter board can be minimized for both signal and ground conductors with the same connector. Microstrip on the other hand, would require a ground on one side of the board and the signal on the other side. This arrangement would negate the possibility of minimizing discontinuities between signal and ground with the same connector configuration because there would be unequal distances between the associated grounds and signals. Stripline would pose an even greater problem than microstrip since three levels of conductors would have to be interconnected.

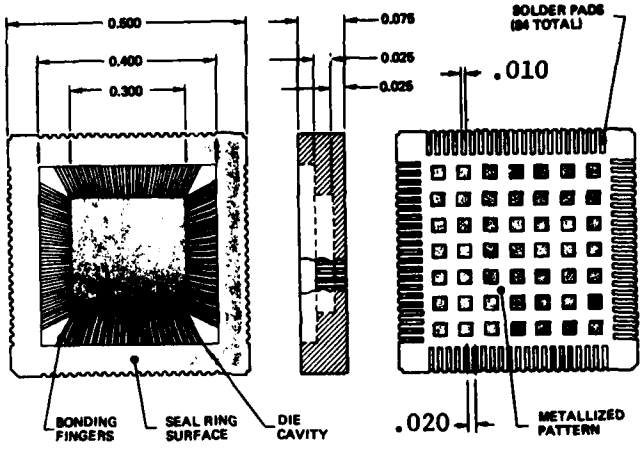
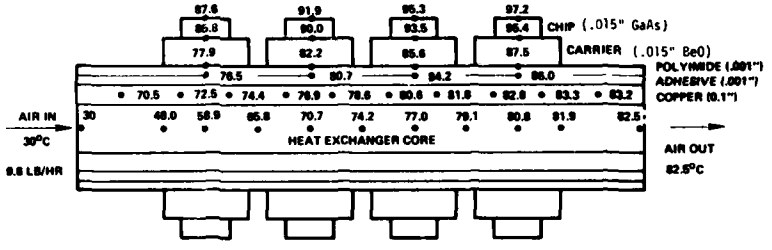



Figure 7

84 Lead Ceramic Chip Carrier With
Leads on .020 Inch Centers




NOTE: TEMPERATURE DISTRIBUTION IS SYMMETRICAL ABOVE AND BELOW HEAT EXCHANGER

Figure 8

Temperature Distribution of Chip Carrier -
PC Board Module

A group of sample substrates were manufactured with hybrid lines on polyimide. The hybrid line spacing was .050 inch between centers on the conductors. It was found that for polyimide in the range of 5 to 80 mils thick, signal conductor widths of 5 mils and greater could yield a characteristic impedance of 50 ohms.

Another test to determine isolation between hybrid lines indicated a 7dB improvement for a 2" length of a hybrid line when compared to the same length of coplanar line.

Chip Carrier Packages

Large multichip carriers are optimum for reducing propagation delay between chips and for providing efficient heat transfer, however, they are expensive to produce and require a custom design for each application. For these reasons a smaller, more versatile chip carrier design was chosen. The goal for the smaller carrier design would be to optimize testability, reliability, maintainability, versatility, and producibility and yet provide satisfactory performance at clock rates up to 5 GHz and at high power dissipation levels.

Maintainability would be improved by virtue of the fact that single chip carriers can be individually replaced when a chip fails. Testability is improved since the chips can be tested individually after they are mounted in the carrier. A large multichip carrier, on the other hand, would require de-lidding to remove a bad chip, thus exposing and possibly damaging the other chips. In addition, leadless single chip carriers can be removed by local heating to melt the solder joints.

Single chip carriers can be even more effective if their lead density is increased. The leadless chip carriers currently available have conductors on .040 inch or .050 inch centers, have die cavity sizes up to .450 inch x. 450 inch, and up to 96 conductors. The lead spacing causes the overall package size to be larger than necessary for the number of leads. If the spacing is reduced from .040 inch to .020 inch, then the package can be half as large, or, twice as many leads can be used on the same size package. The most desirable situation is to make the package as small as possible with the greatest number of leads. It is not feasible to make the lead spacing less than .020 inch for manufacturability reasons.

The die cavity size of a single chip carrier should be large enough for a .250 inch x .250 inch chip, since this is approximately the maximum LSI chip size used today, and is likely to become more common in the future. With this in mind, a chip carrier has been conceived with a 0.300 inch square die cavity with 84 leads on .020 inch centers. The overall package size is .500 inch x .500 inch. This is the minimum overall size that is practical for the die cavity size needed. An illustration of this chip carrier design is presented in Figure 7. Since the conductors through the walls of the chip carrier have uncontrolled impedances, it is necessary to keep their length as short as possible. The lower limit on this length is determined by the minimum practical bonding ledge width plus the minimum seal ring width. These

figures are .025 inch for the bonding ledge and .050 inch for the sealing surface, giving a minimum wall dimension of .075 inch. In order to allow for manufacturing tolerances, a practical wall width is 0.100 inch. Accepting this dimension as a design standard, the overall size of the chip carrier would be determined by the die cavity size.

Leadless chip carriers can be reflow soldered to PC boards. This method minimizes the number of interconnections between chips, since no sockets, leads, or intermediate boards are used for mounting the chip carriers. From the viewpoint of electrical performance, chip carriers soldered directly to PC boards offer the smallest discontinuity.

Mechanically, however, there may be problems with the solder joints failing. Thermally induced stresses, vibration and shock must all be considered. The Air Force Avionics Laboratory (AFAL) has conducted a study of hermetic chip carriers soldered to PC boards. The conclusions reached were that, "leadless hermetic chip carriers can be attached to epoxy-glass, polyimide and triazine PWB's and that such an approach is quite adequate for benign to moderately severe environments if proper process control is observed. Reliability equal to or exceeding that of conventional PWB's used in avionics systems today can be achieved".[2]

The PC board and heat exchanger module concept should reduce mechanical stresses on solder joints due to bending, since the heat exchanger is a very stiff structure and the PC boards are securely bonded to it. The conclusion is that reflow soldering chip carriers to PC boards is feasible from a mechanical stress standpoint, however, further tests should be conducted.

A potential problem in soldering chip carriers with pads on 20 mil centers is that solder bridges may occur. The gaps between pads are only 10 mils wide. In order to determine the solderability of these pads, some chip carrier models were soldered to printed circuit pad patterns. The tests showed that it is feasible to reflow solder chip carriers with pads on 20 mil centers, but that the solder pad thickness must be carefully controlled to assure self-alignment and to prevent shorts.

Thermal Control

The thermal management approach developed is to solder chip carriers to PC boards which are bonded to both sides of a heat exchanger, thus forming a module. An analysis has been performed on a model of such a module to determine the effect on maximum chip temperature of such variables as chip carrier base material and thickness, surface area of the chip carrier base soldered to the PC board, air flow rate through the heat exchanger, and thickness of the PC board.

The analysis was performed on a module which had the following physical components, as shown in Figure 8;

(1) Copper heat exchanger core, 0.2 inches x 2.0 inches x 4.0 inches
(2) Copper heat sink on each side of heat exchanger core, 0.1 inch x 2.0 inches x 4.0 inches
(3) PC board on each side of copper heat sink, .002 inch thick between the heat sink and chip carrier (.001 inch polyimide x .001 inch acrylic adhesive)
(4) Beryllia chip carrier base .015 inch thick soldered to PC board at lead pads only
(5) Gallium Arsenide chip .015 inches x .2 inch x .2 inch, dissipating 4 watts, soldered to chip carrier base

The total power dissipation of the module is 64 watts. As specified in the program's technical requirements, inlet air temperature is 30°C, flow rate is 2.5 lb/min/kw, and maximum pressure drop through the heat exchanger core is 1.5 inches of water.

The thermal analysis was conducted by developing a mathematical model of a section of the module. The temperatures at the node points are shown in Figure 8. The maximum chip temperature expected for this configuration is 97.2°C. This is sufficiently low to give good reliability as far as chip performance is concerned.

## Acknowledgements

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# THICK FILM NON-HERMETIC DIODE PHASE SHIFTERS

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## ABSTRACT

This paper describes a specific application, the microwave phase shifter, for which thick film technology has provided the optimum low cost substrate fabrication technique. The thick film process utilizes conventional screen printing and firing to deposit the signal pattern metallization, substrate vias, and circuit capacitors. A second characteristic of this application is design for reliable operation without need for hermetic package sealing. This is accomplished through use of noble metals for exposed circuit patterns, interconnection ribbons, and device terminations, as well as glass-sealed thick film capacitors.

## INTRODUCTION

The "phased array" radar antenna represents the latest generation of innovations required to meet the military defense needs of the United States. Older style radars with mechanical rotating antennas are unable to track fast-moving targets, such as missiles and artillery shells, due to basic limitations of mechanical systems. Phased array antennas eliminate these limitations by eliminating the mechanical gimbal entirely. The phased array antenna is a flat rectangular assembly, made up of hundreds of individual radiating elements. Directional control over the antenna radar signal is accomplished by controlling the phase of the signals from the individual radiating elements.

The diode phase shifter is one of a number of phase shifter designs; it depends on control over the radar signal by microwave diodes. In the designs discussed in this paper, each module in the diode phase shifter antenna is actually a hybrid microcircuit, containing active components (diodes), and passive components (capacitors), interconnected by ceramic-based conductor networks. Because of the high usage of hybrid microcircuits as phase shifter elements, the cost of these hybrids is an important factor in the cost of the phased array antenna. Hughes Aircraft Company has pioneered the use of thick film, non-hermetic hybrid microcircuits as low-cost phased array elements.

## WHY THICK FILMS?

Historically, thin film techniques have dominated hybrid microstrip applications. The principal reason for this has been the more precise photolithographic pattern definition used in thin film processing. Another important factor has been the relatively high insertion losses of thick film conductors. Since phase shifter designs typically do not require extreme pattern precision however, this does not represent a problem; a new generation of thick film conductors has also removed the second barrier.

Thick film conductors widely used in the late 1960s were usually mixtures of metals and glass. The glass, which was required to adhere the film to the alumina substrate, caused the conductors to exhibit high insertion losses in microstrip applications. The introduction of "reactive bonded" and "mixed-bonded" thick film conductors during the 1970s removed this handicap. This new generation of thick film conductors requires little or no glass for adhesion; their insertion losses are acceptably low for most microstrip applications. Table I lists the measured insertion losses of a representative sample of reactive and mixed-bonded conductors. As indicated, the performance of a number of currently available thick film gold materials was found to equal that of thin film chrome-gold.

Phase shifter designs have two unique requirements which are easily met by thick film processing: metallized substrate vias (holes) and low value capacitors.

## THICK FILM VIA AND CAPACITOR PROCESSING

Typical phase shifter designs contain many precisely located vias which are required to provide circuit connections to the substrate ground plane. These connecting feed-throughs are required to carry high RF currents during antenna operation. Because of the requirement for precise locations, these vias are laser-drilled, which results in somewhat rough walls with sharp feathered edges (Figure 1). Thin film metallizing of such vias, by vacuum or sputter deposition followed by electroplating, is a costly process, in part due to the difficulty in consistently metallizing the sharp edges. Another alternative, use of soldered pins or rivets, is slow and introduces a mechanical component of questionable reliability. Metallization by thick film techniques is, however, easily accomplished. We have found that a platen design which provides individual via vacuum pull-through, coupled with a very slow squeegee speed are necessary to ensure dependable screen printing. Typically, each substrate contains 25 vias, 0.035 inch diameter, in 0.050 inch-thick substrates. Each substrate is given a single via-print stroke; after firing, vias are 100 percent electrically tested at 5 amps to ensure reliability.

TABLE I. INSERTION LOSS OF SOME COMMERCIALLY AVAILABLE THICK FILM CONDUCTORS

| Material | Manufacturer | Type | Insertion Loss at 3 GHz ($dB/cm \times 10^{-3}$) |
|---|---|---|---|
| Gold, Theoretical | -- | -- | 11 |
| Gold, Thin Film (Ref.) | -- | -- | 21 |
| Gold | Electro Oxide | 6990 | 21 |
| Gold | Electro Science Lab | 8880 | 21 |
| Gold | Du Pont | 9260 | 24 |
| Gold | Du Pont | 9791 | 25 |
| Gold | Cermalloy | 4398 | 25 |
| Gold | Plessey | C5750 | 25 |
| Gold | Plessey | C5751 | 25 |
| Gold | Electro Science Lab | 8881 | 30 |
| Gold | Engelhard | A3319 | 35 |
| Gold | Thick Film Systems | 3066 | 36 |
| Platinum-Silver | Engelhard | 3508 | 21 |
| Platinum-Silver | Du Pont | 9770 | 28 |
| Platinum-Silver | Engelhard | A3417 | 30 |
| Platinum-Silver | Plessey | C4710 | 35 |
| Platinum-Silver | Electro Science Lab | 9501A | 36 |
| Silver | Thick Film Systems | 4055 | 22 |
| Silver | Cermalloy | 4570 | 30 |
| Copper | Cermalloy | 7029M | 30 |
| Palladium-Silver | Plessey | LP40-4400 | 91 |

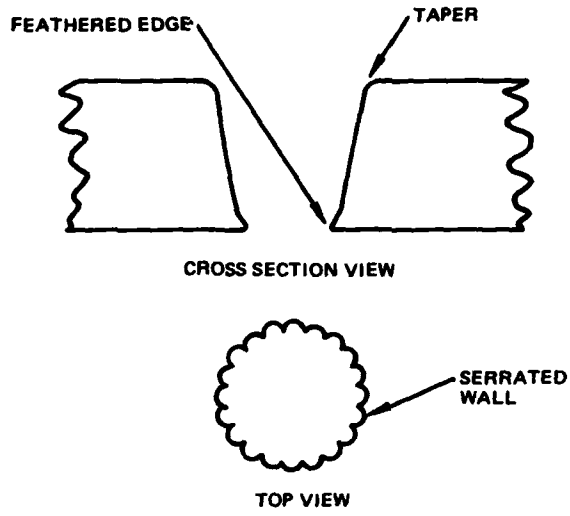


Figure 1. Characteristics of laser-drilled vias.

Numerous (typically 30) low value blocking and bypass capacitors are required for diode phase shifter designs. Although the required capacitance values are not precise, high voltage (100 Vdc) and microwave operation requirements dictate relatively expensive MOS capacitors for designs which utilize discrete components. The thick film process eliminates the need for such discretes, since capacitor dielectric materials are available from many paste suppliers and nothing special is required for screen printing.

## PHASE SHIFTER MANUFACTURE

The phase shifter module manufacturing process flow is given in Figure 2. As-fired, 96 percent $Al_2O_3$ substrates are often used instead of the ground/polished 99.5 percent $Al_2O_3$ widely used in microwave applications. Although the lower purity alumina exhibits somewhat higher (but tolerable) loss, it typically is an order of magnitude lower cost, a distinct advantage for low cost applications.

As indicated in Figure 2, the screen printing process is used to deposit the signal and ground plane conductors, via metal, capacitor dielectric, capacitor termination, and capacitor overglaze. Although seven separate print-and-fire operations are required to complete the substrate definition, routine thick film procedures allow high production rates.

Assembly of the phase shifter is relatively simple compared to most hybrid microcircuits, since it's only active devices are diodes. The diodes are, however, not simple, since they are required to operate at high frequency and

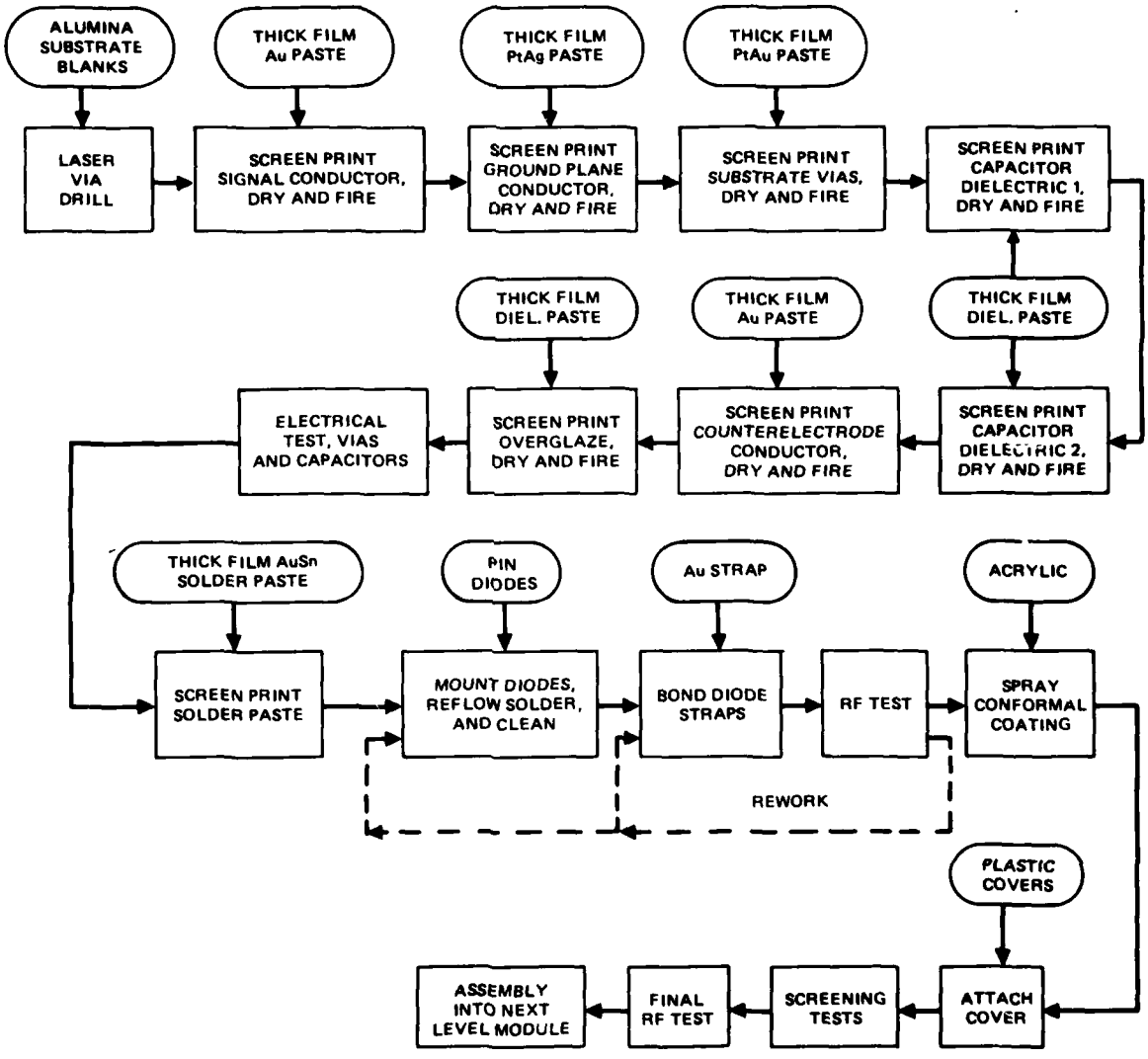


Figure 2. Phase shifter manufacturing process flow.

high voltage. The number of suppliers of acceptable PIN diodes currently is limited. This, coupled with the relatively high cost of the diodes, represents the only serious disadvantage of diode phase shifter technology.

The PIN diodes are gold-backed, a requirement for solder-attachment to the substrate metallization, which is also gold. During the assembly process, 80/20 gold-tin eutectic solder, in thick film paste form, is screen printed on the substrate. Next, the diodes are placed, and the solder reflowed on a heated stage contained in a dry nitrogen atmosphere. After cleaning, the phase shifter is ready for diode interconnection.

Since these phase shifters typically operate in the 2-10 GHz frequency range, the signal path needs to exhibit uniform transmission line behavior throughout. To accomplish this, round wire normally used in hybrid microcircuit interconnection is avoided in favor of flat ribbon. This ribbon, typically 0.001 x 0.020 inch gold, is connected to both the substrate pattern and the PIN diode terminal (also gold material) by welding, using a conventional parallel-gap welder. The exact placement (dress) of this strap is important since it determines both the impedance and signal phase. Figure 3 shows the ribbon interconnection as well as the thick film capacitor and via. As indicated in Figure 2, the phase shifters are then RF tested. Units which fail this test may be easily reworked; this usually involves replacement of a diode, or ribbon re-dress.

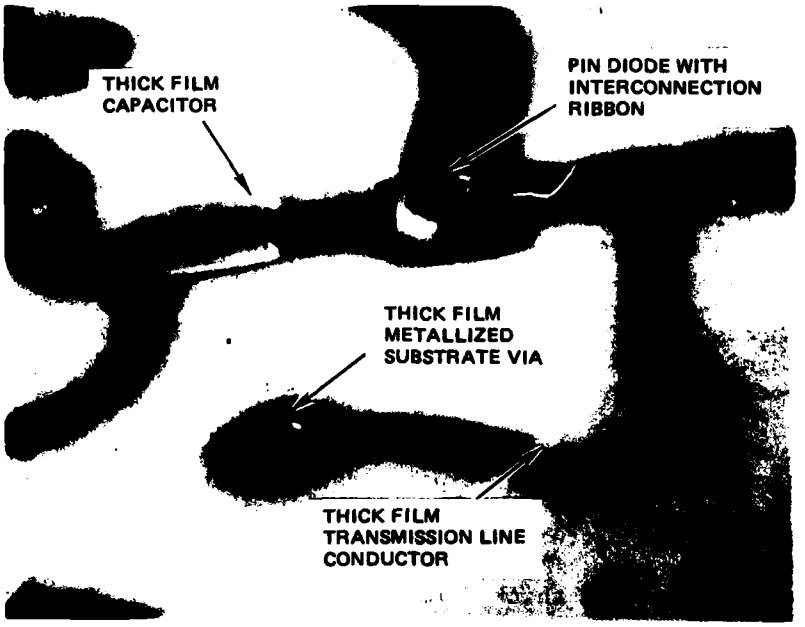


Figure 3. Close-up showing key elements of phase shifter.

Packaging of the phase shifters is relatively simple since hermetic sealing is not required. The circuit is simply given a conformal coating of Acrylic, followed by attachment of an open-sided plastic cover. The thickness of the conformal coating, although not critical, is important since it can affect the impedance of the circuit.

Screen testing of the completed phase shifters consists of temperature cycling (-55°C to +125°C, 10 cycles), followed by burn-in (168 hours at 125°C with 100 volt bias). Although this exposure is relatively severe, the failure rate is very low at final RF test.

## PHASE SHIFTER RELIABILITY

Usage of diode phase shifters ranges from a few hundred to tens of thousands per antenna. Because of this, the phase shifter cost is a critical factor; without low cost phase shifters, phased array antennas are not practical.

Low manufacturing cost has been accomplished on diode phase shifters principally by use of the thick film fabrication process. In addition to this, the high cost of hermetic packaging has been avoided; the question is, has reliability been compromised? In order to answer this question, we need to first look at the relationship between the reliability of the individual phase shifter and the reliability of the antenna.

Unlike many hybrid microelectronic applications, performance of the phased array antenna does not critically depend on each phase shifter. Just as the loss of a single instrument in a large orchestra does not end the concert, the loss of a single phase shifter does not cause failure of the antenna. (The general term applied to this characteristic is "graceful degradation".)

Hermetic packaging of hybrid microcircuits has long been regarded as a requirement for achieving military reliability levels. Although the origin of this myth is obscure, one might reasonably assume that it was fed by evidence of failures in hybrid microcircuits which had originally been built in hermetic packages, but which subsequently lost their seals. We have all seen SEM photos from failure analysts depicting aluminum wires corroded beyond recognition and metal films bridging conductor line gaps by filamentary electromigration.

Reliability in low cost phase shifters has been preserved by <u>designing</u> for non-hermetic packaging. The principal elements of this design are:

- gold substrate pattern metallurgy
- glass-encapsulated thick film capacitors
- gold interconnection ribbon
- silicon-nitride passivated, gold-pad diodes.

Extensive environmental exposure tests have been performed at both the component and antenna levels to ensure high reliability of the modules. Phase shifter tests have included conventional exposure modes such as elevated temperature storage (150°C - 1000 hours), extended high humidity (85 percent R.H., 85°C, 1000 hours), and salt fog, as well as accelerating conditions such as extended bias (100 volts, 1000 hours) and autoclave exposure. The results of these tests indicate that non-hermetic phase shifters not only exhibit acceptable reliability for phased array antenna applications, but in some cases exceed the reliability of hermetic packaged microcircuits.

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# STEPS TO IMPROVE X-BAND PIN DIODE PHASE SHIFTER PERFORMANCE FOR MODULAR ARRAYS

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## ABSTRACT

Use of PIN diode phase shifters makes it possible to design phased array antennas in a modular form, implementing large hybrid integrated circuits in which the digital and microwave circuits are housed in a common package. Adoption of PIN diode phase shifters in the past has been slow, however, due to their inferior performance characteristics. This paper offers several approaches towards improving that performance to levels comparable to presently preferred ferrite phase shifters.

## INTEGRATED ARRAY DESIGN

The many components which go together to make up a phased array antenna using a phase shifter per element comprise the following:

- Phase Shifters
- Drivers
- Radiating Elements
- Aperture
- Structure
- Feed System
- Power Distribution Circuitry

In a conventional approach to array design, the task of interfacing and interconnecting all these components into an assembly which will perform reliably is a sizable task which adds considerably to the cost already prohibitively high because of the repeated parts cost represented in the several hundreds or thousands of elements in the array.

The objective of an integrated array design approach is to incorporate many of the items in the above list into single units manufacturable in a stand-alone assembly process. Meeting this objective would make possible manufacture of large portions of the array in identical units (modules) simultaneously, thus reducing the inherent cost. Specific features of this design approach which contribute to keeping the potential cost low are:

- Minimization of interfaces
- Elimination of connectors
- Use of batch processing
- Minimization of parts count
- Minimization of assembly steps
- Potential for automated manufacturing techniques.

A planar array design illustrating implementation of the integrated design approach is shown in Figure 1. This array is an X-band (9.25 to 9.75 GHz) phased array design being developed for a vehicle mounted Acquisition and Tracking Fire Control Radar.*

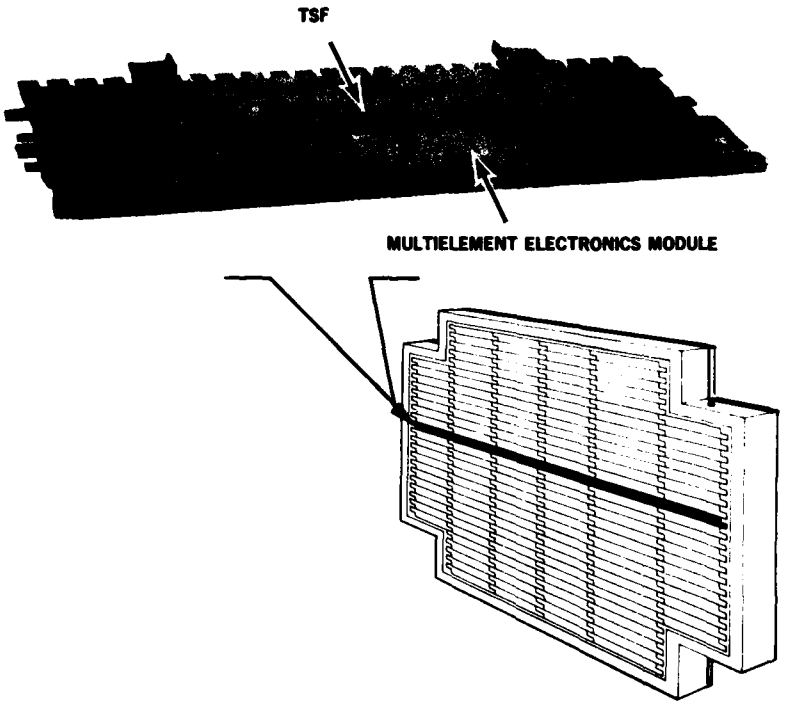



Figure 1. Planar Aperture Design Incorporating Tandem Series Feed between Rows

The multielement electronics module used in this design is pictured in Figure 2. This hybrid circuit incorporates eight four-bit phase shifters, positioned in the module at the array radiating element spacing of 0.7 inch. It also includes the logic and driver circuitry required for commanding with a single 32-bit word all eight phase shifters in the module.

*Contract DAAK-40-79-C-0154, MICOM.

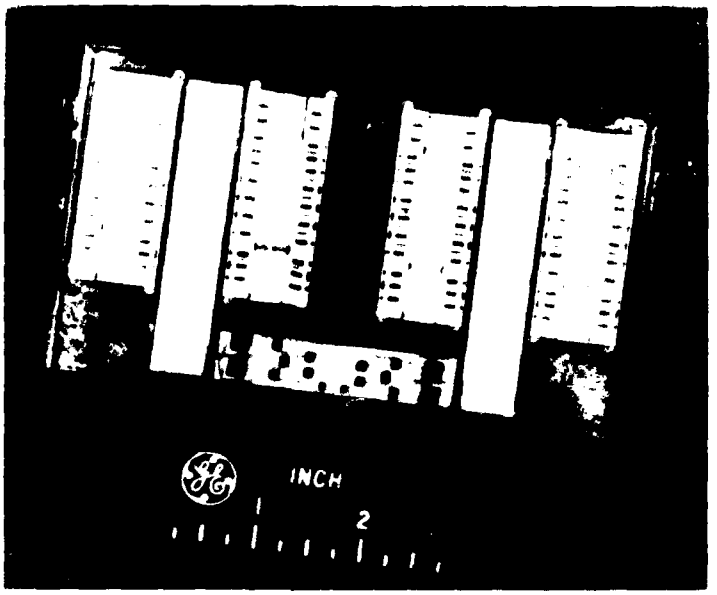



Figure 2. Eight-Element Phased Array Module

The subject of this paper is the performance improvement and configuration of the X-band phase shifters in this type of multielement array module commonly housing the microwave circuitry and its associated control circuitry.

In order to realize the maximum advantage of common packaging of microwave and control circuitry in a single module, PIN diode phase shifters are chosen over their bulk ferrite counterparts which are usually implemented in waveguide, rather than hybrid circuit compatible microstrip on alumina. However, a comparison between performance characteristics of PIN diode phase shifters and those of ferrite phase shifters (Table 1) shows that, historically, systems requiring substantial power levels and low loss performance precluded the use of PIN diode phase shifters. In the past, the usual approach has been to tolerate the cost of ferrite phase shifters and opt for array performance. Such an approach has been proved unaffordable for most anticipated production systems. At the General Electric Company, we have continued to employ the PIN diode phase shifter approach because of the potential cost affordability and have worked toward the objective of diode performance improvement to approach that available from ferrite phase shifters. Table 2 indicates the progress toward this goal over the past ten years.

TABLE 1. COMPARISON OF PERFORMANCE PIN DIODE vs FERRITE PHASE SHIFTERS AT X-BAND BEFORE THIS DEVELOPMENT

| Property | Value | |
|---|---|---|
| | Ferrite Phase Shifter [1] | PIN Diode Phase Shifter [2] |
| Insertion Loss | <1 dB | <3.5 dB |
| Insertion Loss Variation | < ±0.2 dB | < ±0.5 dB |
| Bandwidth | 10% | 6% |
| Power Handling | 10 W Avg [3]<br>20 kW Pk | 2 W Avg<br>1 kW Pk |
| Phase Shift Accuracy | <2° rms | 6.5° rms |
| VSWR | 1.3:1 Max | 1.5:1 Max |
| Switching Speed | 20 μs typical | <1 μs |

Notes: [1] Dual Mode Reciprocal Type

[2] 4-Bit Design

[3] Limited by Resistive Mode suppressor, not ferrite

TABLE 2. PIN DIODE PHASE SHIFTER IMPROVEMENTS ACCOMPLISHED 1970-1980

- Loss Reduced from 3.5 dB to 2 dB
- Bandwidth Increased from 6% to 10%
- Peak Power Capability Increased to 2 kW
- Average Power Capability Increased to 10 Watts
- Hermetic Seal Designed

## PHASE SHIFTER PERFORMANCE LIMITATIONS

Phase shifter characteristics by which the quality of their performance is evaluated include those listed in Table 1. Of all these characteristics, the PIN diode phase shifter at X-band frequencies outperforms the ferrite phase shifter only on switching speed. However, other important considerations combine to strongly favor adoption of diode phase shifters where possible. These include driver complexity, reciprocity, control power, size and weight, and temperature sensitivity.

The extent of performance limitations of PIN diode phase shifters is affected by the transmission line medium in which it is implemented. For example, stripline circuitry in teflon-fiberglass has lower transmission loss than microstrip on alumina. However, because of its small size, its compatibility with hybrid digital circuitry and the facility of using chip and wire diodes, thin-film circuitry on alumina has been chosen for X-band diode phase shifter development.

The remainder of this paper addresses specific circuit and device developments which have been pursued toward improving the performance of this type of phase shifter, particularly at X-band in the frequency range 9 to 10 GHz.

## STEPS TO IMPROVE PERFORMANCE

### INSERTION LOSS

PIN diode phase shifter insertion loss arises from two major contributions. These are the circuit losses of the microwave transmission line and the loss associated with the diode resistances. Careful analysis of these effects serves to indicate where the focus of development will yield the best results. We now proceed to review some of these considerations.

Total line loss includes dielectric loss and conduction loss. For materials used in diode phase shifters, the dielectric loss is overwhelmingly dominated by the conduction loss. Therefore, conduction loss will be the only one considered.

A thin rectangular center conductor cross section shown in Figure 3 is assumed. This center conductor will be the major source of the conductor loss because the ground plane will have a much larger conduction cross section. The conductor is assumed to have a resistance per unit length (r) given by

$$r = \rho/2\delta W \tag{1}$$

where $\rho$ is the conductor resistivity, $\delta$ is the skin depth, and W is the conductor width. The conductor thickness is neglected in this treatment. The center conductor transmission line loss per length $\Delta x$ is given by

$$-i^2 r\,\Delta x = (dP/dx)\,\Delta x \tag{2}$$

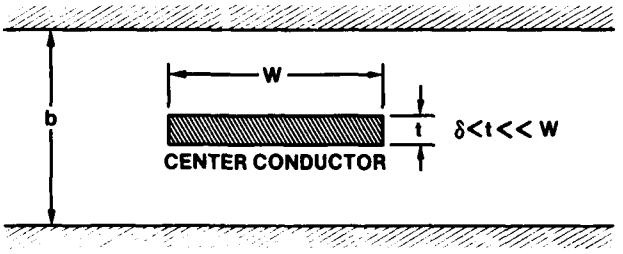



Figure 3. End View of Transmission Line

The power decrement along the line is given by

$$P = (j^2 Z_o) e^{-\alpha x} \tag{3}$$

Applying equations (2) and (3) and taking only first-order terms results in

$$\alpha = r/Z_o \tag{4}$$

Neglecting fringing capacitance for a stripline configuration [4],

$$Z_o = 94.15b/\sqrt{\varepsilon_r}\,W \tag{5}$$

where b is the ground plane spacing and $\varepsilon_r$ is the effective dielectric constant. The skin depth $\delta$ is given by

$$\delta = \sqrt{2\rho/\omega\mu}$$

where $\mu = 4\pi \times 10^{-7}$ h/m

so that from (1)

$$r = \sqrt{\rho\omega\mu}\,/\,(\sqrt{8}\ W) \tag{6}$$

Combining equations (5) and (6) into (4), we obtain the loss factor $\alpha$.

$$\alpha = (\sqrt{\rho\omega\mu\varepsilon_r}\ )\,/\,(\sqrt{8} \cdot 94.15b) \tag{7}$$

Two parameters in equation (7) which the microwave designer has under his control are the ground plane spacing b and the relative dielectric constant $\varepsilon_r$.

Transmission line loss can be minimized according to equation (7) by keeping the effective dielectric constant as low as possible and working with a ground plane spacing b as large as feasible. Several approaches to these objectives have been suggested, including the use of fused silica substrates, teflon fiberglass microstrip, suspended substrate stripline, and air dielectric rectangular coax. These geometries are pictured in Figure 4.

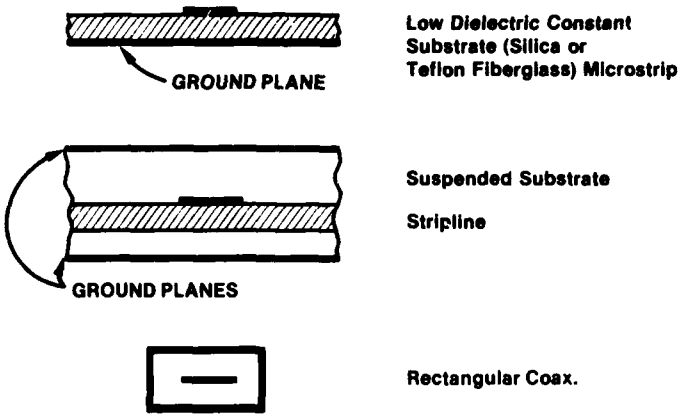



Figure 4. Transmission Line Configurations with Low Effective Dielectric Constant

Such transmission lines must be configured so as to avoid the promotion of spurious waveguide modes. Consequently, lateral circuit dimensions must be kept smaller than waveguide cutoff at the frequencies of interest. The suspended substrate transmission line configuration shown in cross section in Figure 5 is the result of the present development. Characteristic impedance curves are shown for this configuration in Figure 6. The measured transmission loss per unit length for the line is 0.12 dB/$\lambda$ compared to 0.16 dB/$\lambda$ for thin-film microstrip on alumina of 0.025 inch thickness at 50 ohms.

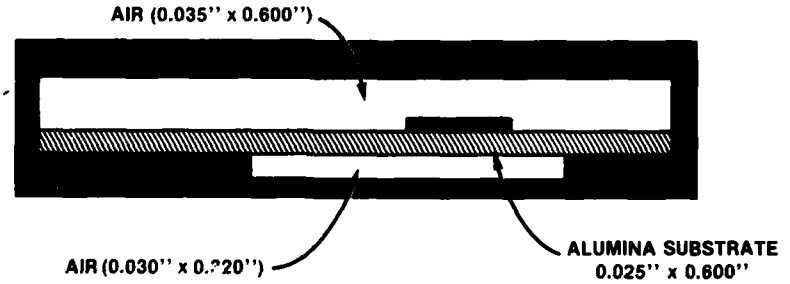



Figure 5. Suspended Substrate Transmission Line Dimensions

Total phase shifter insertion loss for a four-bit phase shifter using identical diodes has been improved from 3.5 dB max in the microstrip design to 2 dB max in the suspended substrate transmission line.

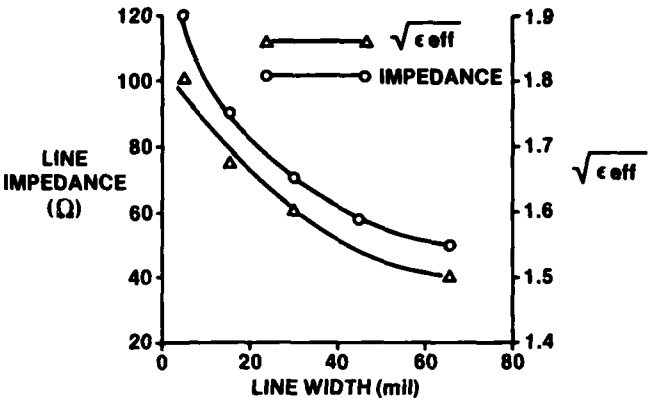



Figure 6. Suspended Substrate Characteristics

LOSS VARIATION

Loss variation between states results in amplitude error in the elements in a phased array which varies as the beam is steered. The cause of the loss variation between states comes from two sources: (1) difference in line lengths involved between the states, and (2) difference in diode resistance between the forward and reverse bias states.

Means of minimizing the first effect include minimizing the circuit loss and designing the bits to use as closely as possible equal circuit lengths in each state. The effect of the diode resistance can be minimized by a judicious choice of circuit characteristic impedance. It has been shown [3] that the ratio $P_D/P_L$ of the power dissipated in the diode to the power in the line is given by

$$(P_D/P_L)_r = KZ_s/R_r Q_d^2 \tag{8}$$

for the reverse bias state and

$$(P_D/P_L)_f = KR_f/Z_s \tag{9}$$

for the forward bias state. In these expressions, $K = 4 \sin(\Delta\phi/2)$, where $\phi$ is the size of the phase shift bit; $Z_s = V_{so}/I_{sc}$, the ratio of the magnitudes of the voltage in the reverse bias state and the current in the forward bias state; $R_r$ is the equivalent series resistance in the reverse bias state; $R_f$ is the series resistance in the forward bias state; and $Q_d$ is the reverse bias diode quality factor given by $Q = 1/R_r\omega C_j$. $C_j$ is the diode reverse bias capacitance and $\omega$ is the angular frequency.

In a loaded line phase shifter employing diodes with reasonably high Q, the ratio $V_{so}/I_{sc}$ is approximately equal to the impedance of the transmission line. Therefore, equations (8) and (9) may be written:

$$(P_D/P_L)_r = KZ_o/R_rQ_d^2 \qquad (8')$$

and

$$(P_D/P_L)_f = KR_f/Z_o \qquad (9')$$

Phase shifters have conventionally been designed in 50-ohm characteristic impedance lines to facilitate matching into available test equipment. In X-band, a representative diode will have parameters listed in Table 3. Using this diode, and equations (8') and (9'), the calculated reverse and forward loss ratios per diode in a 180-degree bit in a 50-ohm system will have the values:

$$(P_D/P_L)_r = 0.027 = 0.12 \text{ dB loss}$$

$$(P_D/P_L)_f = 0.08 = 0.36 \text{ dB loss}$$

TABLE 3. CHARACTERISTICS OF TYPICAL X-BAND PIN DIODE CHIP

| | |
|---|---|
| Capacitance | $C_j = 0.1$ pF |
| Forward Resistance | $R_f = 1$ ohm |
| Reverse Resistance | $R_r = 3$ ohms |
| Quality Factor | $Q_r = 50$ |

The bit design incorporates two diodes so that the total bit losses are 0.24 dB in reverse bias and 0.72 dB in forward bias. Combined with the other bits in a 3- or 4-bit phase shifter, this loss variation between phase states can add up to the order of 1 dB for a complete phase shifter.

The loss variation between states can be minimized by choosing a characteristic impedance different from 50 ohms. Equations (8') and (9') can be used to calculate the characteristic impedance needed to make $(P_D/P_L)_r = (P_D/P_L)_f$:

$$KZ_o/R_rQ_d^2 = KR_f/Z_o$$

giving

$$Z_o = Q_d\sqrt{R_rR_f} \qquad (10)$$

Using the values from Table 3 in equation (10), the correct value of characteristic impedance to equalize insertion loss between states is 87 ohms. In that case, from equation (8') or (9'), the insertion loss of the 180-degree bit will be 0.4 dB.

## POWER HANDLING CAPABILITY

The power handling capability in PIN diode phase shifters is limited mainly by thermal heating and the diodes in the 180-degree bit. Equations (8) and (9) indicate that maximum power is dissipated in the 180-degree bit.

$$\sin \frac{\Delta\phi}{2} = 1$$

Methods which are effective in improving the power handling capability of PIN diode phase shifters include:

1) Minimizing the thermal resistance of the path from the diodes to the ultimate heatsink
2) Configuring the 180-degree bit with smaller multiple subbits (e.g., 4 x $45^{o}$ bits)
3) Minimizing the diode resistance.

## MINIMIZING THERMAL RESISTANCE

To minimize the thermal resistance of the path between the diode and the heatsink requires a knowledge of the thermal resistivities of the materials available to microwave integrated circuit implementation and the ability to calculate the thermal effects of the various geometries involved. Values for thermal resistivity for several materials used in hybrid microwave circuitry are given in Table 4 in $^{o}$C-in./W,

TABLE 4. THERMAL RESISTIVITY OF SEVERAL MATERIALS USED IN HYBRID CIRCUITS

| | $^{o}$C-in./W |
|---|---|
| Alumina | 2.13 |
| Beryllia | 0.24 |
| Aluminum | 0.23 |
| Copper | 0.08 |
| Kovar | 2.22 |
| Epoxy | 33 |
| Silicon | 0.37 |
| Au/Si Eutectic | 0.11 |

Candidate diode geometries include those used in standard microstrip and suspended substrate stripline in either series or shunt configurations. In series configurations, the diode is mounted on the substrate, whereas in the shunt configuration, the diode may be mounted on the chassis for the purpose of effective heatsinking. It is worth noting, however, that shunting the diode to a Kovar chassis for the purpose of good heatsinking is not very effective, because its thermal resistivity is about the same as alumina.

The geometries for the chip, chip attach material, and the substrate thermal path calculations are shown in Figure 7 along with the associated equations. The diode chip is a 0.015 inch square, 0.010 inch in height having an active (heat producing) pad 0.004 inch in diameter. Thermal resistances for the various diode configurations are given in Figure 8.

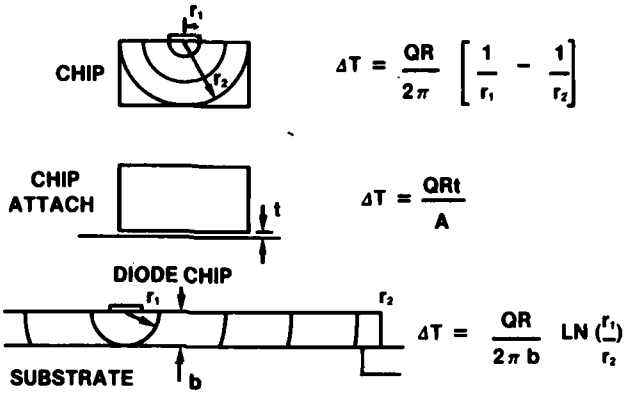



Figure 7. Geometries of Heat Flow

Obviously, the geometry giving least thermal resistance (maximum power handling) is that of shunt microstrip using a copper chassis. For large scale production, required for low cost phased array, this is probably not a cost-effective design, however. Batch fabrication techniques would favor mounting the diodes semi-automatically on the substrates. Here again, alumina is lower cost than beryllia. Consequently, the lowest cost hybrid circuit will have diode thermal resistance somewhere between 60°C and 72°C per watt and the approach of breaking the 180-degree bit into smaller subbits offers a more feasible approach to improving power handling in the phase shifter.

## MULTIPLE SUBBIT DESIGN

Power handling capability of the phase shifter can be increased according to equations (8) and (9) by 4 dB if the 180- and 90-degree bits are configured with multiple 45-degree bits. The penalties paid for adopting this approach are:

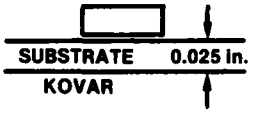
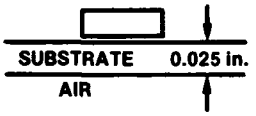
| DIODE GEOMETRY | SYSTEM | DIODE THERMAL RESISTANCE (°C/W) |
|---|---|---|
| | Eutectic Attached Shunt in Microstrip | 30.5 |
| | Epoxy Attached Shunt in Microstrip | 146 |
|   | Eutectic Attached Series in Microstrip Alumina Substrate | 60 |
| | Beryllia Substrate | 34 |
|   | Eutectic Attached Series in Suspended Substrate | |
| | Alumina Substrate | 72 |
| | Beryllia Substrate | 36 |

Figure 8. Thermal Resistance of Diode Geometries

- Increased number of diodes
- Higher control power
- Larger size
- Higher total insertion loss.

The loss penalty paid for using cascaded 45-degree bits for the 90- and 180-degree bits in a complete 4-bit phase shifter is easily calculated. Assuming two diodes per loaded line bit, equation (9') indicates that the expected bit loss will be $2KR_f/Z_o$ where $K = 4 \sin(\Delta\phi/2)$. $R_f$ is the diode forward resistance of 1 ohm, $Z_o$ is the transmission line characteristic impedance 87 ohms. Using these values, the entries in Table 5 are calculated. The first column lists the bit sizes in the phase shifter. The second column lists the loss in each bit when the phase shifter 90- and 180-degree bits are constructed from lossless hybrids. The third column lists the individual bit losses when the 90- and 180-degree bits consist of cascaded 45-degree bits.

Comparison of the cascaded 45-degree bit design with the single bit design shows that cascading 45-degree bits results in a penalty of 0.25 dB loss. However, lossless hybrids have been assumed for the 90- and 180-degree bits. Losses in excess of a quarter dB are common for such hybrids at X-band, indicating that the performance loss may be negligible in going to cascaded subbits.

Cascading subbits results in an increased demand on driver current. In the conventional design, eight diodes are used, whereas in the multiple subbit design, 12 diodes are used, resulting in a 50-percent increase in driver

current requirements. This increase in driver requirement may be recovered by using smaller geometry PIN diodes which reach their limiting value of $R_f$ at lower currents than 50 mA. This approach is feasible because the largest phase shift each diode needs to provide is only 45 degrees.

## MINIMIZATION OF DIODE RESISTANCE

PIN diode forward biased resistance and reverse biased resistance arise from two different but related properties of the device intrinsic layer. The forward current $I_F$ keeps the intrinsic layer filled with electronic charge, making it appear as a low resistance in this state. The value of the low resistance is limited by the injected carrier lifetime $\tau$ which can be related to the ratio of the diffusion length D to the intrinsic layer width W.

Application of the reverse voltage serves to deplete the intrinsic layer of carriers, making the diode appear as a parallel plate capacitor. Diode resistance in this state is a result of depletion layer movement characteristic of a graded doping profile.

TABLE 5. LOSS COMPARISON OF SINGLE BIT TO CASCADED 45-DEGREE BIT DESIGN

| Bit Size (deg) | Single Bit Loss (dB) | Cascaded 45-degree Bit Loss (dB) |
|---|---|---|
| 22.5 | 0.08 | 0.08 |
| 45 | 0.16 | 0.16 |
| 90 | 0.29 | 0.32 |
| 180 | 0.42 | 0.64 |
| Total | 0.95 | 1.20 |
| $(P_D/P_L)_{\Delta\phi} = 2KR_f/Z_o = 8 \sin(\Delta\phi/2) / 87$ | | |

A useful analytic expression for the forward resistance is:

$$R_F = \frac{KW^2}{I_F \tau} \tag{11}$$

where $K = kT/36q$, k is Boltzmann's constant, T is the temperature in degrees Kelvin, and q is the charge of an electron. This equation indicates what must be done to minimize the forward resistance:

- Keep the I-layer width small
- Keep the carrier lifetime high.

The reverse bias resistance can be minimized by providing heavily doped steeply graded p-type and n-type boundaries in the diode.

Diode development which has been undertaken for improvement of phase shifter performance incorporates the following features to minimize series resistance:

- Dedicated high resistivity silicon epitaxy
- Low temperature (<1000°C) semiconductor processing
- Ion implanted p-type junction.

This development had led to a diode improvement over that of Table 3. For example, a 0.23 pF diode with 0.7 ohm forward resistance has a reverse series resistance of a fraction of an ohm. Breakdown voltage of this diode is greater than 150 volts.

## SUMMARY AND CONCLUSIONS

The phase shifter improvement program discussed in this paper is expected to result in an X-band PIN diode four-bit phase shifter having the characteristics given in Table 6.

TABLE 6. PHASE SHIFTER PERFORMANCE OBJECTIVES

| | |
|---|---|
| Frequency of Operation | 9.0 - 10.0 GHz |
| Number of Bits | 5 |
| Insertion Loss | 1.5 dB min, 1.7 dB avg, 1.9 dB max |
| Phase Accuracy | 2 deg rms |
| Peak Power Capability | 2 kW |
| Avg Power Capability | 10 W |
| Size | 0.6" x 3.0" x 0.13" |

Computer aided design is being used to perfect the bits individually and when the measured VSWR of each bit below 1.1:1 is achieved, the bits are then incorporated into the full phase shifter. The phase shifter measured performance to date is given in Figure 9 and 10 for insertion loss and phase shift.

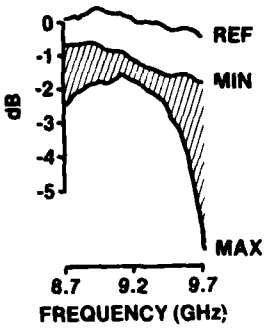



Figure 9.
Insertion Loss Performance of Suspended Substrate Phase Shifter (4-Bit)

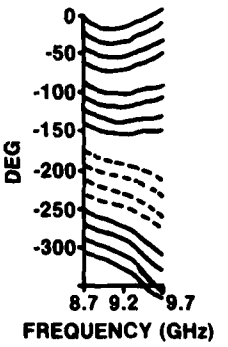



Figure 10.
Phase Shift Performance of X-Band Suspended Substrate Phase Shifter

Work is continuing in order to improve this performance, especially in the characteristic of phase shift accuracy and variation of insertion loss between states. The test fixture for measurement of individual bits and for the full phase shifter is shown in Figure 11 which is a photograph of the suspended substrate transmission line with the top ground plane removed to view the circuitry for the 90-degree bit under development. Eventually the fully developed phase shifter will be incorporated into the eight-phase shifter hybrid module similar to that shown in Figure 1.

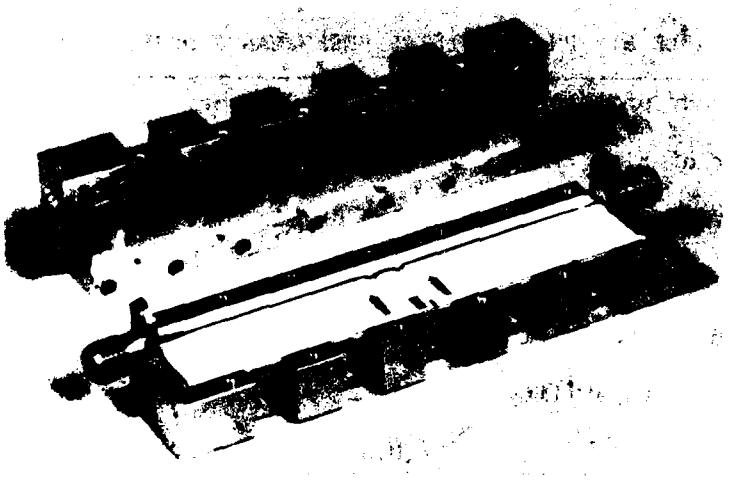


Figure 11. Suspended Substrate 90-degree Bit in Full Size Phase Shifter Housing

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# MICROELECTRONIC CONSIDERATIONS IN MICROSTRIP DESIGNS

BY

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## ABSTRACT

High performance microstrip circuits are normally not mass producible with high yields without considerable emphasis on microelectronic assembly techniques. The proper selection of materials should be based on availability, fabrication methods, and assembly processes, as well as electrical characteristics. For example, a polished alumina substrate has very low microwave losses but it will cause additional processing problems over an as-fired substrate. Therefore, the latter would be the better choice provided the design goals are achieved. Many of the properties of microstrip materials will be discussed along with their processing problems and advantages.

Most microstrip circuit designs require patterns that must terminate at the ground plane. There are several ways that this can be achieved. The commonly used method of drilling holes through the ceramic creates many process and assembly problems while improving the ground connection. The more customary phase, gain and impedance adjustment techniques via pattern layout will also be discussed.

Nearly every microstrip design will use some form of soldering in the assembly operation. The widespread use of soldering is due to ease of implementation. It is difficult to find a replacement for all types of soldering that might be required on a microstrip design. However, the rewards that can be gained with the elimination of any soldering step are well worth the effort. Methods to replace soldering will be discussed, as well as good assembly techniques when soldering is necessary.

Several examples of production microstrip circuits will be presented that demonstrate the advantages gained when microelectronic considerations are part of the overall design.

## INTRODUCTION

The most important aspect of a microstrip circuit is the electrical design, however equally as important is the implementation of that design. This paper will not deal directly with the electrical design but will concentrate on the material and microstrip processing aspects and show how

they effect the electrical design. A major consideration in selection of the material and processing was their effects on being able to produce the microstrip circuit in a production environment. The microstrip substrate system designed at ECI Division, E-Systems will be the vehicle used to demonstrate most of the design considerations recommended.

"The" System

The goal of this section is to describe the microstrip system utilized at ECI. It should be made clear that this system is not the only system or that it is necessarily the best system. However, it has been a well thought out system for ECI's applications and has been coordinated with the fabrication and processing methods used for microstrips.

The metallization system selected was TaN-Mo-Au (Tantalum nitride-molybdenum-gold) for which reasons will be given in the appropriate sections to follow. After investigation of many substrate materials and finishes, an as-fired 3-5 micron finish on high density (99.6%) alumina was chosen as the substrate media.

Substrate Material

The engineer designing microstrip hybrid circuits must demand that he consistently have good substrate material as it plays a vital role in the circuit performance. The electrical properties achievable by the design are directly related to the substrate material's dielectric constant (K) and the thickness. Thus the above parameters must be maintained uniform throughout a single substrate from batch to batch. There are many types of substrate materials in use today which are useful to the microstrip design engineer, some of which are:

1) Alumina (99.6% $Al_2O_3$) - Alumina is the most commonly used material either "as-fired" or polished. The dielectric constant (K) of alumina is found to be in the range of 9.6 to 10.1.

2) Sapphire (99.9% $Al_2O_3$) - Sapphire has a higher K value than alumina, however, it requires sizing and polishing, which can be cost prohibitive.

3) Quartz ($SiO_2$) - Quartz substrates available today are sized and polished to nearly any tolerance desired. This material is frequently used and has a dielectric constant of approximately 4.

4) Ferrite (FeNiCo) - Ferrite materials are used for fabricating special circuit elements such as circulators and is available in various compositions. It requires sizing and polishing for most applications.

5) Beryllium Oxide (BeO) - Beryllium Oxide is used in those circuit designs which require high thermal dissipation The material is available "as-fired", however, special handling is required if the material is to be machined because of the health hazard. The dielectric constant of BeO is 6.5-7.0 and its thermal conductivity is 2.1 watts/cm $^{o}$K at 100$^{o}$C.

The substrate material selected certainly must depend on the circuit application and design, but it also must be compatible with all processing parameters through metallization, photofabrication, assembly and final packaging. Following is a list of substrate material parameters which must be thoroughly considered:

1) Dielectric Properties - Low losses at microwave frequencies require relatively high dielectric constants that are uniform and stable over temperature. Size reduction of circuit elements is an important consideration in today's technology market, thus the material selected is important for this aspect.

2) Dimensional Tolerances - Variations in circuit impedance can be directly associated with substrate thickness tolerance, thus this parameter is of utmost importance. Substrate length and width tolerances are generally satisfactory as supplied, however, they should be investigated for assembly and packaging requirements. Camber tolerance is generally associated with packaging or photolithography and is typically found to be .002" per inch of alumina material.

3) Surface Finish and Surface Defects - Uniform surface finish has high priority as does thickness and dielectric constant. As-fired alumina is available in a 3-5 microinch surface while polishing can achieve a 1-3 microinch surface finish. The cost associated with polished substrates, as well as processing problems encountered due to polishing anomalies (tearouts, etc.) should be weighted carefully. Metallizing of polished substrates requires special consideration for good adhesion and uniform sheet resistivity.

4) Thermal Conductivity - Generally the substrate materials used for microstrip hybrid circuits have good thermal conductivity characteristics, however, special applications require the selection of materials such as Beryllium oxide.

5) Cost - The cost of substrate material for use at microwave frequencies can range from one dollar per square inch to

twenty five dollars or more per square inch. Each of the parameters listed which require tighter tolerances, better surface finish, more sophisticated material or special sizing can drastically increase cost. Therefore the substrate should not be over specified when the design doesn't require it.

6) Processing Compatibility - Listed last is the compatibility of the chosen substrate material with the processing parameters to which it must be exposed to produce the desired circuit. Consideration for all environments expected must be accomplished in order to realistically assess the material compatibility fairly.

Many types of substrate materials have been evaluated and processed at E-Systems, ECI Division over the years of experience in microstrip circuit design and fabrication. Several materials are still used today, however, one substrate material, the as-fired 99.6% alumina, is clearly used more than anything else. The alumina material was chosen because of its consistent electrical and physical properties as shown in Table 1. The remainder of this paper deals with additional design considerations using metallized as-fired alumina as the primary substrate material.

TABLE 1. SUBSTRATE ELECTRICAL AND PHYSICAL PROPERTIES

| Property | Units | Value for 99.6% "as-fired alumina" |
|---|---|---|
| Dielectric Constant | | |
| 1 MHz | — | 9.9 |
| 10 MHz | — | 9.9 |
| 10 GHz | — | 10.0 |
| Loss Factor - 1 MHz | — | 0.002 |
| Volume Resistivity | ohm-cm | $>10^{14}$ |
| Dissipation Factor - 1 MHz | — | 0.0001 |
| Thickness | inch | as specified $\pm$10% or selected |
| Length, Width | inch | $\pm$1% or NLT $\pm$10% |
| Surface Finish | µ-inch CLA | 3-5 |
| Camber | in/in | 0.002 |
| Thermal Conductivity | $cal/cm^2/cm/sec/^oC$ | 0.090 @ 25°C<br>0.050 @ 300°C |
| Thermal Coefficient of Linear Expansion | per °C | $6.3 \times 10^{-6}$ |

## Substrate Metallization System

The metallization system in use at ECI is a sputtered-to-thickness composite of tantalum nitride - molybdenum - gold. The tantalum nitride is RF diode reactively sputtered while the molybdenum and gold are DC magnetron sputtered. All three films are deposited on the substrate during a single pass utilizing a MRC 903 in-line sputtering system. The vacuum system has a load lock capability which allows the main chamber to remain under full vacuum during the loading and unloading of 12 inch square pallets of substrate material.

The substrate metallization system is one of the most important design considerations which must be addressed when designing microstrip circuits. The metallization system chosen for use at ECI came about after years of development efforts and was proven through production. The system must not only have the required electrical properties and be reproducible at a reasonable cost, but must also be compatible with all subsequent processing. Several areas that require consideration are photofabrication; resistor stabilization and trim; substrate hole drilling and sawing; substrate assembly including TC bonding, soldering and epoxy bonding; and packaging. The tantalum nitride resistor film, the molybdenum barrier/adhesive layer, and the high density gold conductor film are briefly discussed below, however there are additional references to the metallization system throughout the paper.

## Tantalum Nitride

Tantalum nitride resistors have been utilized for producing hybrid microcircuits for many years. Those considerations of importance to the microstrip designer are addressed below:

a) Fabrication - The fabrication of tantalum nitride resistors is compatible with subsequent processing and is extremely reproducible.

b) Uniformity - The resistor film uniformity as deposited is better than 5% over a 10" square area.

c) Stability - Tantalum nitride resistors are thermally stabilized (300-450°C) in an oxidizing atmosphere at which time a protective film of tantalum-pentoxide is formed. The tantalum-pentoxide serves as a protective layer against abrasion, moisture, and further chemical attack.

   Long term stability has been experimentally measured to be better than $\pm$ 0.5% (150°C-1000 hours).

d) Thermal Coefficient of Resistance (TCR) - Typical TCR's measured are -50 to -150 ppm/°C. Repeatability of TCR's, run to run, has been better than 5%.

e) Sheet Resistivity - The standard sheet resistivity used at ECI is 100Ω/□ , however tantalum nitride films in the range of 30-250Ω/□ have been used for special applications.

Those tantalum nitride resistors which require very close tolerances are trimmed using a YAG laser system having a 1½-2 mil kerf. As can been seen in Figure 1, a special laser trimmable resistor (trombone design) has been implemented for producing relatively high value resistors. This design requires a small area but is typically capable of adjusting the resistor value as much as 40% of its final value. Power handling capabilities of tantalum nitride resistors are excellent as are their noise characteristics at microwave frequencies. 9

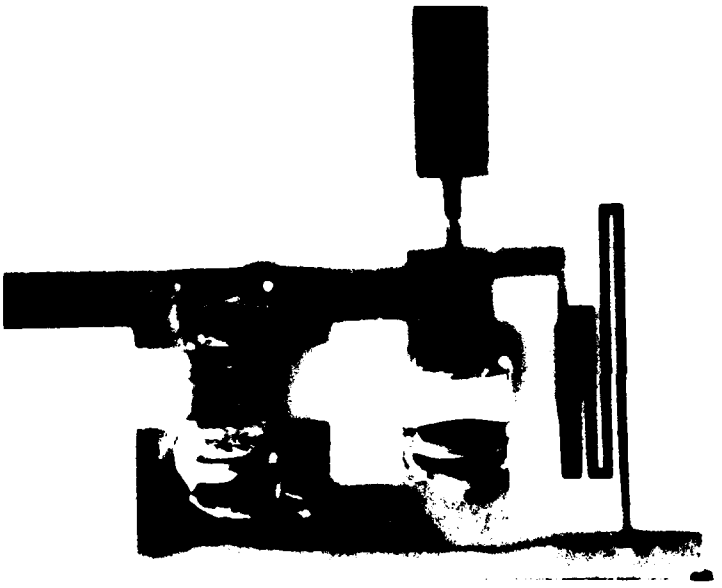

FIGURE 1.0 LASER TRIMABLE RESISTOR

Molybdenum

The second layer, approximately 500-1000 Angstroms in thickness is sputtered molybdenum. This film has a twofold purpose; it is a adhesion layer and diffusion barrier layer between the tantalum nitride and gold conductor. Molybdenum has good adhesion characteristics and has a proven high temperature processing compatibility demonstrated over a number of years at ECI. The molybdenum film is sputtered via a DC planar megnetron.

Gold Conductor

Sputtering is used exclusively to deposit conductor films at ECI. Sput-

tered-to-thickness gold films have been chosen for several important reasons; the high electrical conductivity (99.9% purity), non-oxidizing character, excellent adhesion, film thickness uniformity, bondability (TC bonding, soldering, epoxy, die attach) superior coverage of surface topography, and a low-loss high Q-factor film. The above statement characterizes a conductor film of excellent electrical properties having compatibility with subsequent processing.

Conductor deposition via electroplating was not selected because the films obtainable are not consistent in electrical characteristics or thickness. Plated films do not exhibit the same level of Q-factor consistently as do sputtered films. In addition, the electroplated films previously used in experiments had significant adhesion failures due to blisters when taken to elevated temperatures. Sputtered gold films, however, were consistently uniform in thickness (better than 5%), free of contamination, and compatible with high temperature assembly processing.

ECI utilizes a in-line magnetron sputtering system to deposit gold from a high utilization "inset" target. Gold films of 250-300microinch thickness (3 skin depths at 2 GHz) are DC magnetron sputter-deposited on "as-fired" ceramic in less than 25 minutes.

Artwork Generation

In order to produce microstrip circuits which utilize critical dimensionally superior to that used for other types of hybrid microcircuits, the ECI Division of E-Systems employs a state-of-the-art computer aided design (CAD) system and an integrated circuit photomask system to produce the artwork. After layout of the microstrip circuit using the Computervision CAD system, a pattern generator tape is supplied which is run on an Electromask 251 Combo pattern generator/image repeater system to produce the desired artwork on glass. The Electromask System has the capability through extended software to (a) shrink or expand the circuit design, and (b) bias the line widths as may be required. The availability of this equipment allows for rapid turn-around time for initial layouts and/or modifications when required. In addition each "cell" previously designed can be retrieved for insertion in to subsequent circuit designs as needed.

Design

The initial application for a microstrip circuit at ECI was in 1974 for a bandpass filter operating at S-band frequencies. Several designs were implemented with the best results in the parallel coupled line design. This was due to both a better understanding of the electrical design and the ease at which the design could be implemented. Various types of interdigitated filter designs were only partially successful, because of inadequate design equations for microstrip filters and the lack of know-how to achieve the proper grounding of the elements in microstrip form.

Today the equations for microstrip designs are readily available through

computer programs such as compact, super compact, SNAP [1] and Quad Hybrid [2].

However, the grounding of elements often required in microstrip designs are still left up to the individual designers. Yet the success of the circuit design is often determined on just how well the grounding is achieved. The most successful method employed at ECI has been the wrap-around ground, WAG. This is where the ground plane on the back side of the microstrip substrate wraps around the edges of the substrate and makes contact with the pattern on the circuit side, as shown in Figure 2. This method allows easy conversion from the electrical design to a microstrip design and provides consistent electrical results in production. An alternate method where holes are drilled in the substrate for access to the ground plane should only be used as a last resort. If bond wires or ribbons are used to connect the patterned element to ground, their inductance must be included as part of the electrical design. Even when they are included in the design it is difficult to maintain consistent results in production. Some of the deviations are caused by variations in length of the interconnection by the operator bonding the circuit. Also variations in cross-sectional geometry effect inductance as indicated by the following.

$$L \propto \frac{\text{Length}}{\text{Effective cross sectional area}}$$

Both effects can be minimized by using rectangular ribbon because of the lower inductance per unit length.[3]

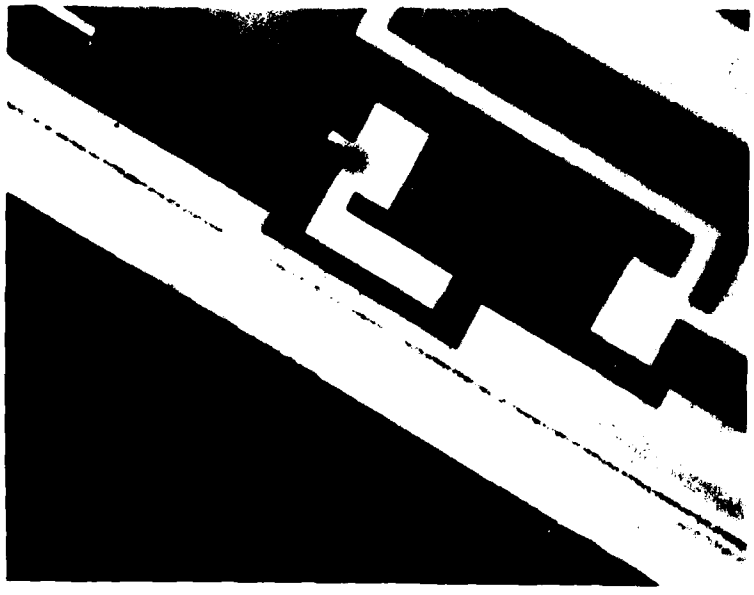

FIGURE 2.0 WRAP-AROUND-GROUND

A third and least acceptable approach is to drill the hole prior to metallization in order to achieve electrical continuity between the ground plane and the circuit side. This method is similar to the WAG at the edges except the hole edges and sides are not well controlled and cause severe adhesion problems with the metallization. The holes also create a non-homogenious surface which causes many problems in photoetching patterns on the major surface. Holes in the substrate also provide areas where high stresses can concentrate to a value exceeding its tensile strength, therefore causing the substrate to crack. High temperature processing (annealing, bonding, and soldering) creates high stress conditions from thermal gradients and mismatch in thermal expansion coefficients. High stress conditions may also occur while the circuit is in the system where a cracked substrate would be a catastrophic failure.

A hole in a substrate is often required to accommodate an electrical component. In this case the peak stress areas can be kept to a minimum through minimization of sharp discontinuities around the hole and where the radius of curvature is maximized. A general rule is that the smoother the discontinuity (physical transition), the lower the peak stress will be under a given condition. Figure 3 is an example of a substrate with a hole required to accommodate an RF packaged transistor. Note that there are smooth radiused edges along the oblong hole without any major flaws. This circuit continues to be successfully produced in large quantities for a phased array antenna system.

FIGURE 3.0 RF TRANSISTOR ASSEMBLY

Holes are drilled in the ceramic using precision drills and diamond core drill bits. Typical hole sizes range from .030" to .150" and are commonly used in both .025" and .050" thick as-fired ceramic. During circuit design and layout, helpful processing aids which precisely mark hole location or size can be made part of the photofabrication artwork. For protection of the remainder of the substrate circuit metallization during hole drilling, the surface is coated with a photoresist having good transparent qualities. The substrate is waxed to a glass surface so that when the drill bit clears the ceramic it does not enter a void, but continues through a similar material. Hole drilling and sawing of ceramic are accomplished under water for lubrication and removal of particles.

Since most microstrip elements are implemented through exact lengths of transmission lines it isn't always convenient or possible to have a grounded element terminate at the edge of the substrate. A novel and unique approach patented at ECI is the application of a tapered transmission line (impedance transformer)[4] to force the termination to occur at the edge of the substrate. Figure 4 shows three grounded quarter wave stubs designed with a stepped transmission line. The utilization of the tapered transmission line has replaced the need for substrate holes in many different microstrip designs. Also shown in Figure 3 is a special ground ring that provides both emitters of the RF transistor with low inductance connections to ground.[5] Various types of low impedance post can be easily designed for special applications but generally they also require undesirable holes in the substrate.

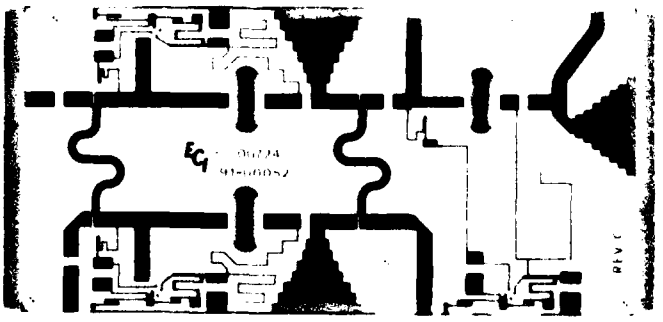

FIGURE 4.0 TAPERED IMPEDANCE TRANSFORMER

## Substrate Photofabrication

There are many design considerations which are associated with the required precision and reproducibility of conductor/resistor pattern delineation. Microstrip circuit characteristics can be drastically altered from that required by the design engineer if parameters such as conductor line width, edge definition, undercutting, and spacing between conductors are not controlled during photofabrication. Many of these parameters can be better controlled if proper adjustments are made in the artwork during the layout stage. Critical line widths must have added compensation to the artwork based on measured undercutting observed from the process and materials to be used to fabricate each individual circuit. Line width tolerances when etching 250-300 microinch thick gold are held to $\pm$ 0.0002 inch typically, however tighter tolerances are achievable through tighter process controls.

The etching of resistors causes some concern in that etching the thick conductor metallization required for microstrip circuits plays a vital role in the ultimate resistor line width. The same artwork line width compensation previosuly mentioned must also be applied to fabricating resistors. When designing low value resistors where their final etched length plays the more important part, artwork compensation associated with undercutting must be taken into account.

Another design technique used to reduce the tolerance requirements on resistor lengths is shown in the following figure. Note that all resistor conductor terminations are the same width as the resistor width. This reduces the tight tolerance requirements on alignment between patterns.

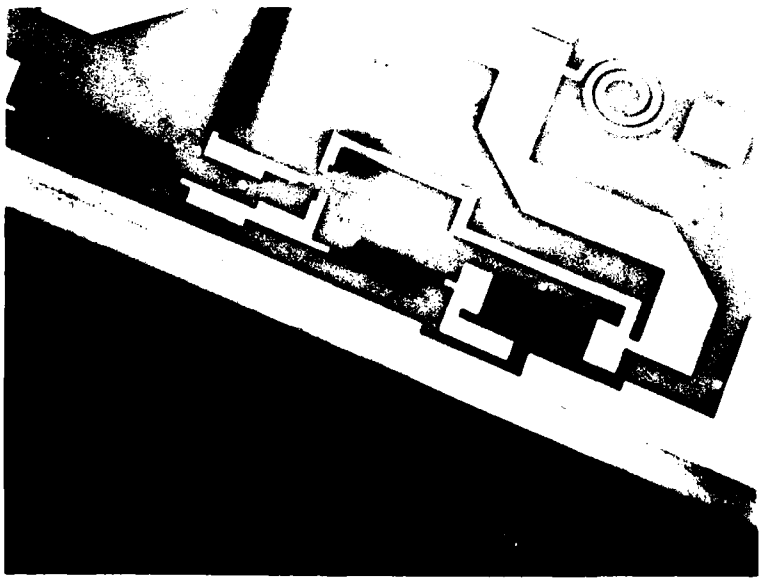

FIGURE - RESISTOR WINDOW PATTERN

Experiments at ECI with substrates having predrilled holes which must remain void of conductor material presented many problems associated with uniform photoresist application and handling. Therefore hole drilling in substrates for component placement is accomplished after all photofabrication has been completed.

The wrap-around-ground employing the use of continuous conductor metallization from the "A" face of the substrate to the "B" face (ground plane) takes full advantage of the sputter coated substrate edges. During the photofabrication procedure it is necessary to coat those edges with photoresist to prevent etching. Considerations worth noting include the fact that the metallization thickness at the substrate edges is somewhat thinner than that on the major surfaces and that due to surface tension effects the applied photoresist tends to draw back from the sharp edges leaving little or no resist at those points. In cases where the circuit design requires exceptional grounding with high reliability, the ceramic substrate edges must be radiused prior to metallization deposition, thus preventing the above mentioned situation. Figure 2 shows a good example of a wrap-around-ground on a .050" thick substrate which has radiused edges.

*Electrical Adjustments*

Most microstrip designs do not require any adjustment to meet electrical specifications because of the excellent reproducibility of etched patterns. But many active devices integrated with microstrip circuits have electrical variations that exceed the fixed properties of input or output matching networks. In most cases the S-parameters of the device could be selected from a generic device to meet the electrical specs of the fixed design. Often this approach will either require a special selected device or a custom device which could be very expensive or possibly not even available. Therefore, it is often wiser to make the circuit adjustable in order to accept a more common device that is available from multiple sources. This type of planning during the design phase of a circuit can prevent serious redesign or schedule problems in production. The need for electrical adjustment commonly shows up in production when your sole source stops producing the "special device" or they lose the magic ingredient. In the past some circuits were not able to be designed this way because S-parameters weren't always available or measured. Also the more recent advent of computer analysis has allowed for the proper selection of S-parameters to a circuit.

Another common reason for adjustment patterns on microstrip circuit is for normalizing the gain or phase of a circuit. One such application is the need for a common gain and phase of each RF module in a phased array antenna system. The gain of the RF module can easily be adjusted several db through adjustment of the biasing resistor on the Low Noise Amplifier (LNA). Actively trimming this resistor with a laser can be achieved but requires elaborate fixturing and test sets. An easier approach can be implemented by segmenting the resistor in the necessary increments. These segments are

jumpered with bond wires during assembly and then removed during testing until the proper gain is obtained. An example of a segmented resistor with gold one mil bond wires is shown in Figure 5. This particular resistor design provides a one db gain adjustment in quarter db steps. The gain of the LNA isn't altered until after it is installed in the RF module so that the total gain of the module is adjusted. The phase of the module was designed to be adjusted through the removal of incremental capacitive pads (Figure 6) attached through low inductance ribbons.[6] The transmission line must be modified to maintain the proper characteristic impedance due to loading effects of the adjustment pads.

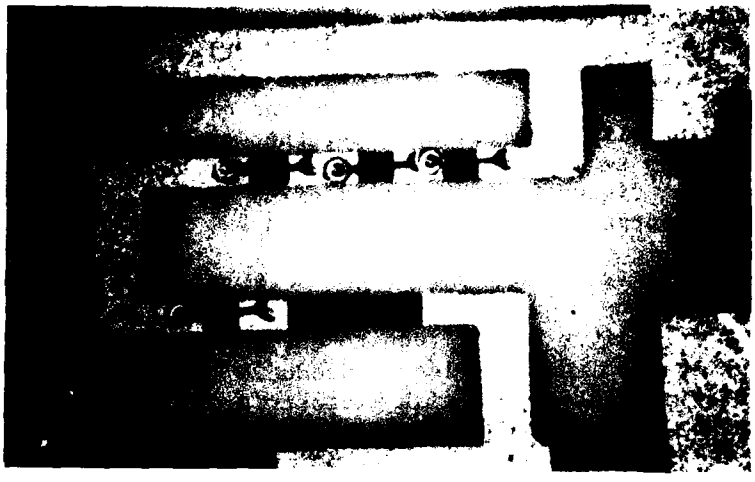

FIGURE 5.0 ADJUSTABLE SEGMENTED RESISTOR

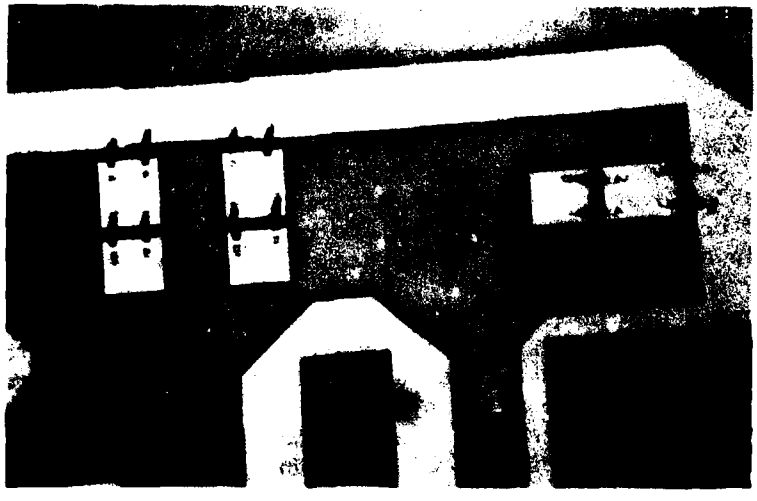

FIGURE 6.0 PHASE ADJUSTMENT PADS

## Assembly Considerations

Both assembly processes and the substrate metallization system must be compatible for successful production circuits. For example, the Mo-Au metallization system mentioned earlier is not compatible for soldering a pallet to the ground plane. The soldering of components to large areas of gold films requires tightly controlled special processes to prevent excessive gold amalgamation. Without these controls the entire gold films can go into solution with the solder causing adhesion problems. Through experience it has been learned that in production one should avoid as many processes as possible that require tight controls or special procedures. For this reason a transitional film has been added to the ground plane. An electroplated copper film is plated over the sputtered gold ground plane which lends itself to a more standard soldering process. The finished bond after soldering has the more desirable shiney finish. This is normally expected by inspection personnel rather than the grainy gold-solder solution obtained when soldering directly to gold. Reworking a copper solder joint normally improves its quality; reworking of a gold solder connection causes further deterioration or failure of adhesion.

Excessive camber in a substrate could cause extra thick solder between the ground plane and the pallet. Since the electrical ground is normally obtained through this solder connection, it could effect the electrical performance of the circuit. General rules of thumb for good electrical grounds when using substrate/pallet mounting are:

1. Have a thin uniform layer of solder between pallet and substrate especially where the RF inputs and outputs are located.

2. Have mounting screws located at or very near the RF inputs and outputs.

3. Make certain pallet and chassis make good contact at the RF input and output.

4. Check all ground interfaces when going from one circuit to the next especially at the RF connections.

Most microstrip circuits will have a mixture of both soldered and metallurically bonded components. Normally the metallization system that is ideal for one is not very compatible for the other. Therefore, an engineering compromise must be made to select the most appropriate film system for the application. As discussed earlier the resistive film must also be considered when making the conductor selection. The most appropriate film system chosen for ECI's applications has been the TaN-Mo-Au system. This system is ideal for either thermocompression or thermosonic bonding. The conductor is ideal for photofabrication along with the TaN resistive film. The outer gold layer is one of the best for being inert and unaffected by

normal environments. Gold also is perfect for high temperature soldering such as gold-tin solder. The main disadvantage with the gold outer layer is the special processing required when soft soldering components to the film. A somewhat extensive effort has been taken to reduce the number of components that require soft soldering to the gold. This has been accomplished through the use of gold beam lead diodes, transistors and capacitors. Examples of beam lead transistors and capacitors are shown in Figures 7 and 8 respectively, a bonded beam lead detector diode is shown in Figure 1.

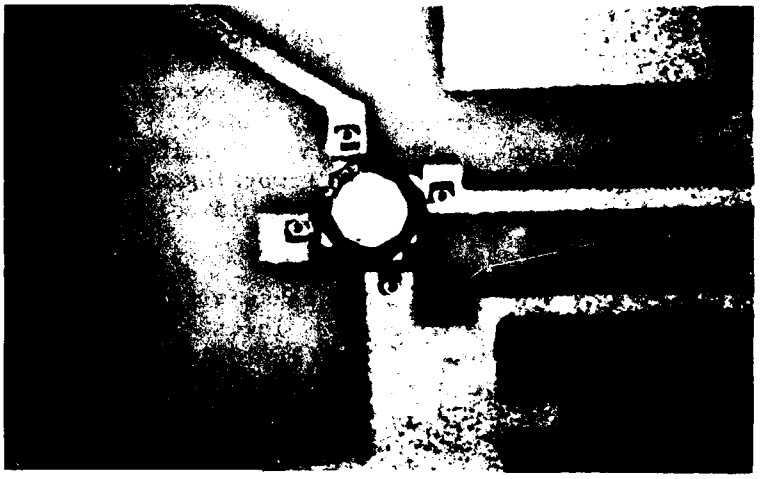

FIGURE 7.0 BONDED BEAM LEAD TRANSISTOR

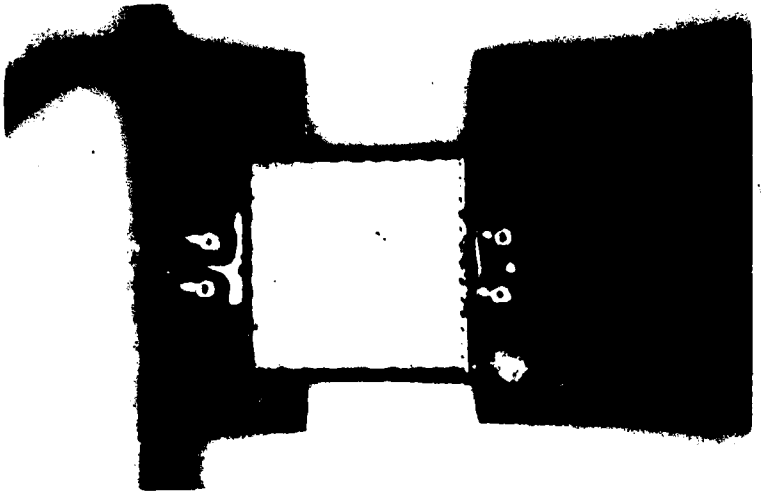

FIGURE 8.0 BONDED BEAM LEAD CAPACITOR

Examples of perfectly soldered ceramic chip and tantalum chip capacitors to gold films are shown in Figures 1 and 9. Even though it is possible to soft solder to gold, the process must be tightly controlled. Some circuits are presently in production that have as many as 16 capacitors and only one solder bond could destroy the circuit and effect productivity. Therefore, the advantages of beam leaded devices are realized in production. Beam leaded devices are also much easier to remove and replace without any deleterious effects. It should be mentioned that beam lead capacitors are normally static sensitive and require special handling. On the other hand porcelain ceramic chip capacitors are very rugged and rarely have failures. Still any unsoldering from gold films is tricky and can frequently be done only once at the same location on the substrate. For these reasons circuits using beam leaded devices have been more successful in the production environment.

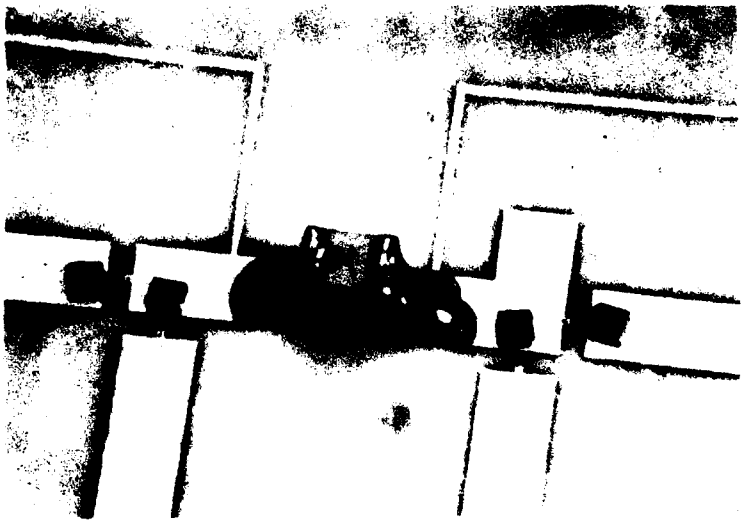

FIGURE 9. SOLDERED CHIP CAPACITOR

There still exist some components that require soft soldering to the substrate. One such device is a packaged RF transistor with planar leads as shown in Figure 3. High potential stresses between the leaded device and the substrate prevent the use of high temperature soldering. Stress relieved leads, limited soft solder and a special soldering process has allowed this circuit to be successfully assembled in production.

High temperature soldering (gold-tin eutectic) has been successfully used in production. It can easily be employed for mounting small discrete devices to gold metallized substrates. Figure 9 shows four of 24 PIN diodes mounted to a common substrate for a dual beam phase shifter. All 24 devices were eutectically bonded at the same time through a reflow soldering process.

The process is so successful that recently a lot of 50 substrates (1200 diodes) were monitored that had zero defects through test.

Another commonly used component that requires special handling is the pedestal mounted diode with existing wire bonds. This device shown mounted in Figure 10, is fragile and difficult to handle. The device is normally used as a grounded shunt diode and, therefore, usually requires a hole in the substrate for mounting. It is recommended that this device be avoided where possible in any volume production circuits because of handling problems.

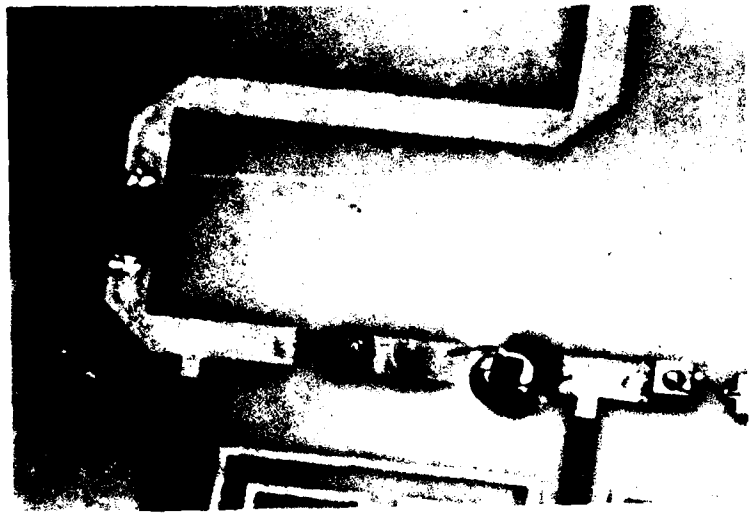

FIGURE 10. PEDESTAL MOUNTED DIODE

## Conclusion

The main idea in the assembly of microstrip circuits is to have both assembly processes and the metallization system as compatible as possible. This will simplify the production processing and reduce the number of special procedures required to produce a finished product.

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# ELECTRONIC COUNTERMEASURES DETECTION USING HYBRID MICROELECTRONIC TECHNIQUES

BY

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## ABSTRACT

The use of hybrid microelectronic circuits in electronic countermeasures (ECM) systems has recently increased, particularly in applications involving microwave detection and logging of signal levels. In this application, hybrid microcircuits offer advantages in unit-to-unit repeatability in power, frequency, and temperature regimes; low weight and volume; and cost, mainly due to active laser trimming techniques. These hybrids typically involve custom hermetic packages, blends of thin and thick film technology, and usage of a variety of semiconductor devices, including beam-lead components. Testing is accomplished by using computer controlled automatic testers.

As an example, many tens of thousands of a particular type are being produced for a state-of-the-art ECM system. Each circuit consists of a broadband single-ended detector followed by a sophisticated DC logarithmic amplifier. These units are all matched over input power levels from -45 dBm to +5 dBm to within 0.75 dBm, over frequency to 1 dBm, and over temperature to 1/3 dBm.

The use of such hybrid microcircuits makes the design of ECM systems requiring hundreds of independent detectors a feasible approach.

## INTRODUCTION

Logarithmic amplifiers have become standard in many microwave systems and ECM equipment. They provide a large dynamic range, low noise, wide bandwidth, and a clean pulse response.

The use of hybrid technology combined with thin film techniques permits such an amplifier to be built in a small package - 7.5 cm x 3.0 cm - (Figure 1) meeting the full requirements of MIL-STD-883B.

Through new manufacturing techniques, it is now possible to fabricate these amplifiers in large quantities, each tracking to very tight specifications. This obviously greatly improves replacement situations when quick repair turnaround is required. Unit tracking also eliminates system recalibration.

Radar arrays can be implemented using this multi-receiver concept. A receiving system covering the entire ECM spectrum could be built using this approach. Figure 2 shows a possible concept. In this system large quantities of receivers are multiplexed in real time to a unified bus system. A microprocessor, along with an A/D converter, is used to poll R.F. intensity at each receiver. Package hermeticity and consistent parameter repeatability from unit to unit ensure reliable operation over the military temperature requirement -55°C to +125°C.

The package offers an ideal solution to system designers as a basic building block to meet a variety of design requirements. Adherence to tight specifications requires new concepts and specialized manufacturing materials and techniques. For example, units must be matched over a wide power input level range from -45 dBm to +5 dBm; all units must track to within .75 dBm. The same situation applies over the frequency spectrum where units are matched to 1 dBm. All parameters also track over temperature to 1/3 dBm.

A block diagram of the units is shown (Figure 3). The hybrid consists of a wideband detector preceding a logarithmic amplifier; the pair acting as an envelope detector with rise time better than 20 nanoseconds. The detector demodulates the pulsed R.F. input fed to the hybrid, and generates the envelope to the logarithmic amplifier. The logarithmic amplifier then provides a pulse whose amplitude is proportional to the input power.

In systems using this multi-amplifier approach in concert with some type of lens arrays, tracking between individual amplifiers is imperative, especially at close range where known signature analyses have to be performed in real time. Deviations or anomalies within the response curve would lead to erroneous interpretation in bearing and distance of target estimation. The logarithmic characteristic of the amplifier-detector combination also alleviates saturation at close range, a problem often encountered with oversensitive receivers.

Real-time estimation of target location also permits generation of R.F. saturation in a concentrated direction. This implementation would be based on a secondary system having transmitting capabilities and whose input would be under control of some microprocessor control.

## DETECTOR CONFIGURATION

The detector is isolated from the amplifier in a separate cavity on the front-end of the amplifier.

Microwave energy is fed through an R.F. connector into a micro-strip configuration whose design provides a 50 ohms termination impedance. A beam-lead diode in concert with a resistor capacitor network provides the required characteristics.

The output of the detector is then fed to the main amplifier through a .030 inch gold ribbon wire. The wire is ultrasonically welded to a glass isolated pin on both sides of the assembly.

## DETECTOR CHARACTERISTICS

Figure 4 shows possible variations in detector characteristics. Since any deviation in detector characteristic is bound to affect the overall performance of the system, some means were established to set linear tracking from unit to unit. Each detector must be electrically characterized over the desired frequency spectrum. The detector is characterized by selecting ten input power levels in the reference curve ranging from -45 dBm to +5 dBm.

The frequency response is then measured at 1/4GHz increments at -17.5 dBm over the total passband.

## AMPLIFIER CHARACTERISTICS

Compensations for detector variations and logarithmic transfer function implementation are made through a network consisting of a number of diodes and a 17-resistor array. As can be seen in Figure 3, each amplifier feeds into this diode function generator. In turn, resistor adjustment can be tailored until the right characteristic is established. It is important to note that, at this point, each array is unique to a given amplifier.

The selection and characteristic of each of the 17 resistors is done dynamically. An algorithm generated by Teledyne is used to control a computer test system. The data thus recovered from the characterization of each detector is recorded onto a magnetic cartridge. Subsequently, this cartridge is brought over to another laser trimming station. From the information retrieved, a resistor network is generated.

This resistor network is epoxy attached onto the main substrate (Figure 1). Electrical connection to the main substrate is made through gold wire. Connections to the output pins are made by gold ribbon wire bonding.

Under computer control, the unit is swept in frequency and power level. The output is then measured from -45 dBm to +5 dBm in 2 dBm increments. The frequency response is then measured at -17.5 dBm across the passband in 1/4GHz increments.

This data is then processed to obtain final trimming information for the amplifier offset and gain. A final algorithm is used to verify that the transfer curve accuracy is within $\pm$ 3/4 dBm from -45 dBm to +5 dBm.

The frequency response is then matched to a standard frequency response and checked to be within $\pm$ 1/3 dBm over the passband. Figure 4 shows three different uncompensated power response characteristics: A, B, C, and D. The

idealized characteristic response is shown in curve D. This is obtained by trimming the resistor-diode network combination.

The test system consists of an H.P. 8925A calculator, frequency synthesizer, pin modulator, attentuators, relay actuators, R.F. power meter, digital voltmeter, and a sample and hold module. Calibration and test programs are fed to the calculator by a cassette. A line printer, a floppy disk, and a cartridge recorder also augment the data logging capability of the system.

During measurements, all peripherals are continuously updated through an IEEE-88 instrumentation bus. A basic diagram of the test set is shown in Figure 5.

## PULSE CHARACTERISTICS

Through software control, the pulse response of the amplifier can be tailored to meet specific requirements. Parameters such as rise time, overshoot, and overall pulse width and shape-factor can be trimmed for, during the overall characterization of the amplifier.

## FABRICATION AND ASSEMBLY

Each unit carries with it its entire history. A traveler sheet accompanies the unit throughout the fabrication cycle. On this traveler, each step of fabrication is identified through a specification number.

Starting with a blank alumina substrate, a gold thick film pattern is deposited using a screen printer. The substrate is then fed into a firing furnace.

Note. at this point, that the use of multilayer circuitry requires several firings. A firing cycle is required for each layer or isolation dielectric. In this instance, a ground plane is screened on a bare alumina $Al_2O_3$ substrate. Connections to the bottom substrate are made through wraparound metallization on the side of the substrate. The firing temperature profile depends on the particular material used; however, temperatures of 850°C are typical. All components, capacitors, transistors, and resistor arrays are mounted on the logarithmic amplifier substrate.

After inspection, the substrate is attached to the case. An epoxy preform is used for that purpose. The unit is then baked, allowing the epoxy to cure. After bonding, the unit is retested, vacuum baked, and sealed. A seam sealer is used for this operation. The main advantage is that the sealing operation is solder free, thus avoiding the use of corrosive flux and related contamination problems.

## PACKAGE INTEGRITY

The mechanical integrity of the package is then tested by submitting the unit to centrifuge, mechanical shocks, and temperature shocks.

## CONCLUSION

As a result of hybridization, the M.T.B.F. (Mean Time Between Failure) of the unit was increased to over 83,000 hours. Improvements in manufacturing costs and higher yields resulted in a cost reduction of over an order of magnitude.

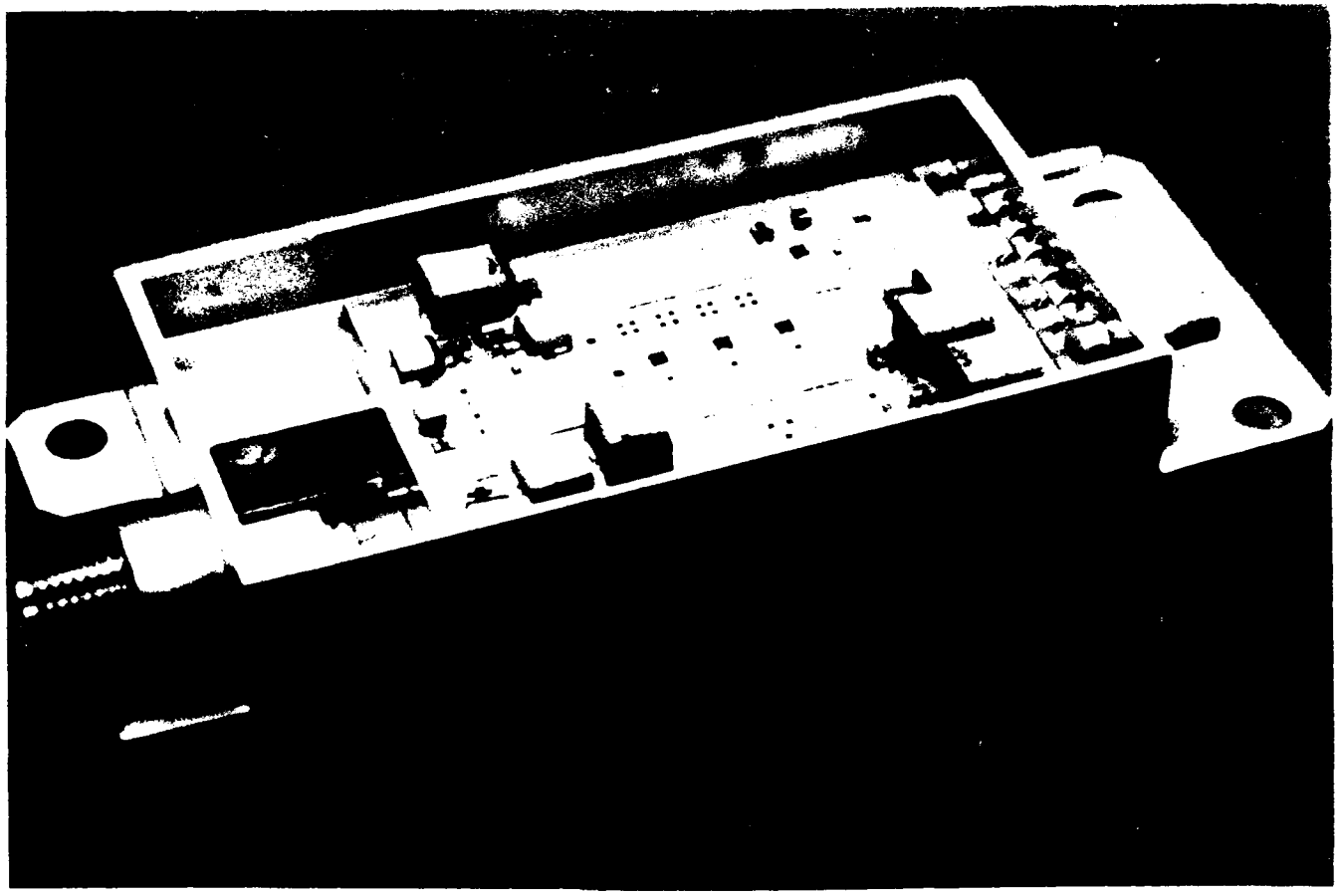


FIGURE 1 - DETECTOR AMPLIFIER OVERALL DIMENSIONS 7.5 CM x 3.0 CM

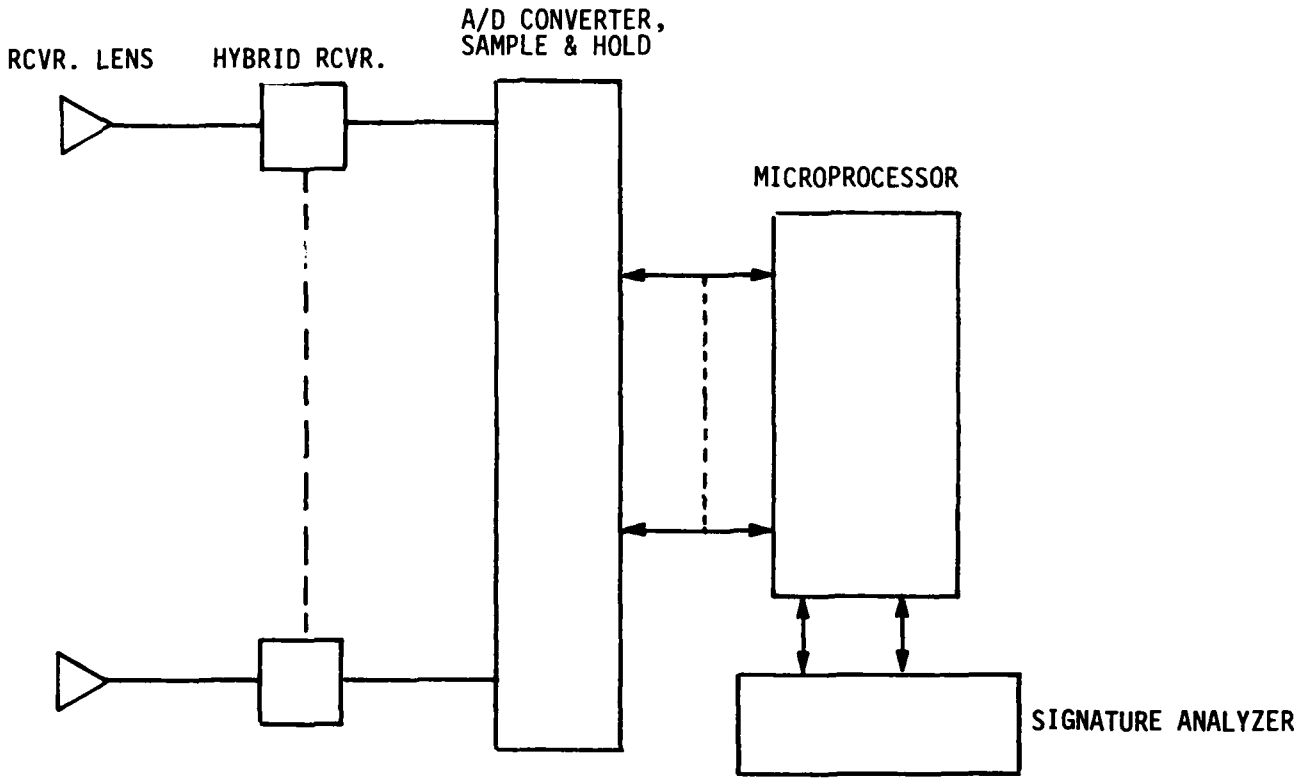



FIGURE 2 - MULTI-RECEIVER ARRAY

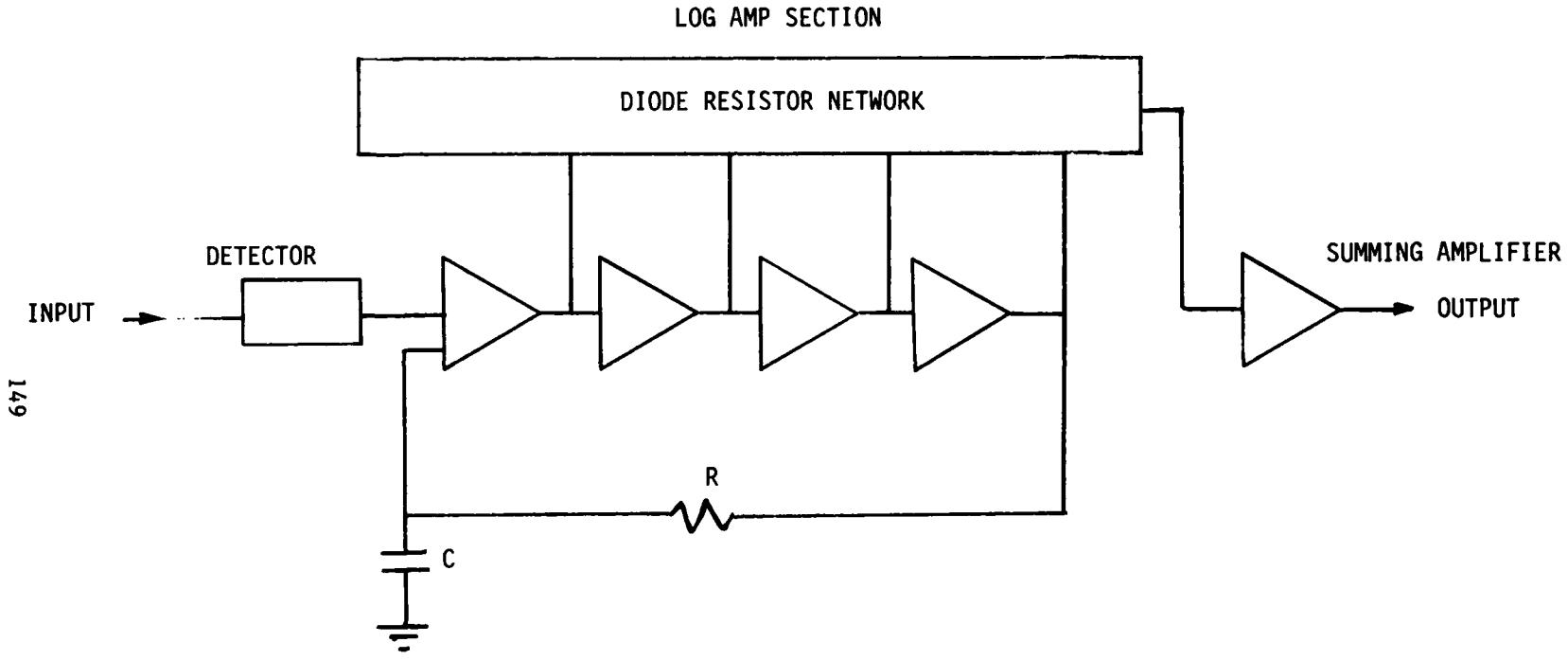



FIGURE 3 - AMPLIFIER DETECTOR BLOCK DIAGRAM

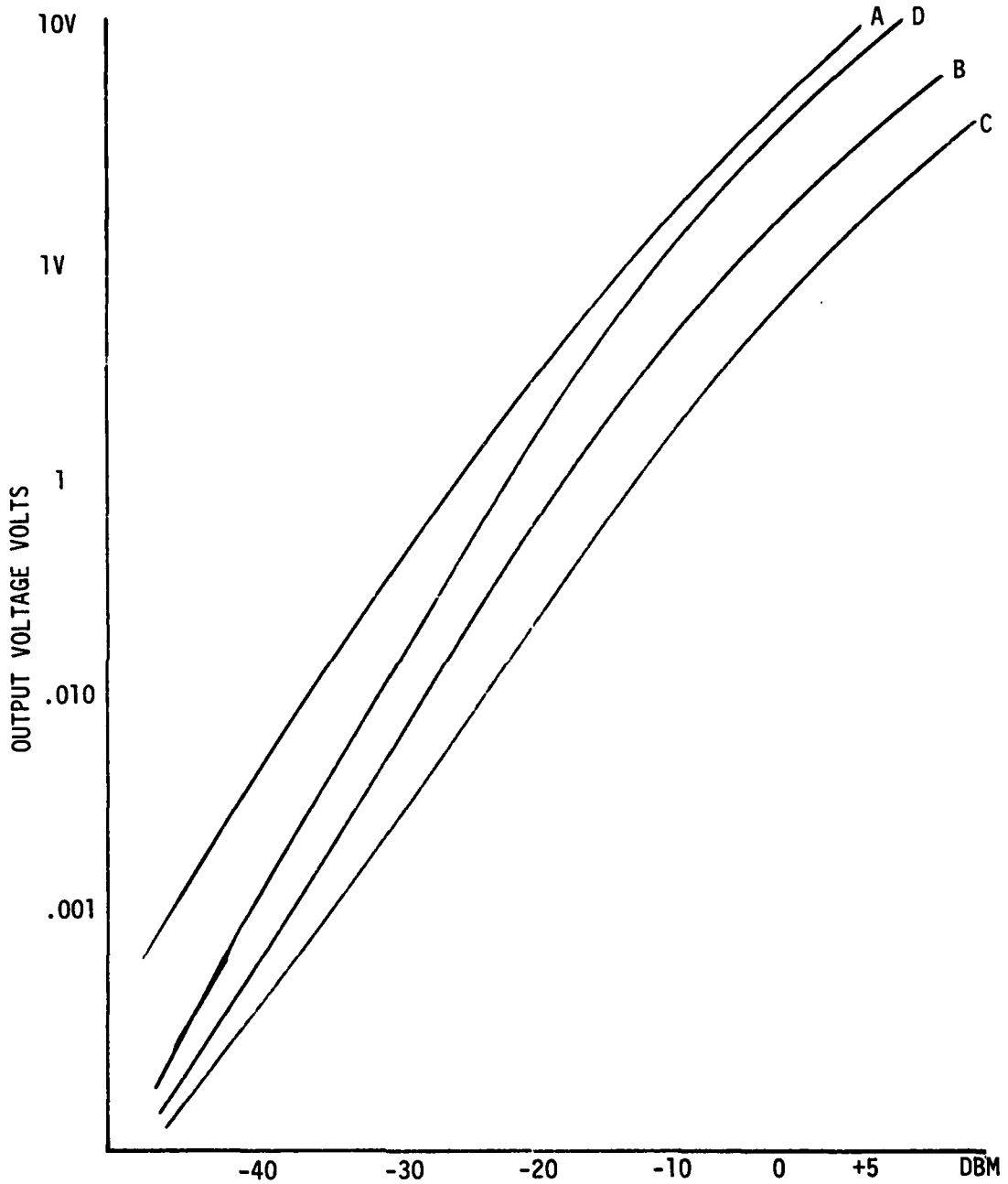
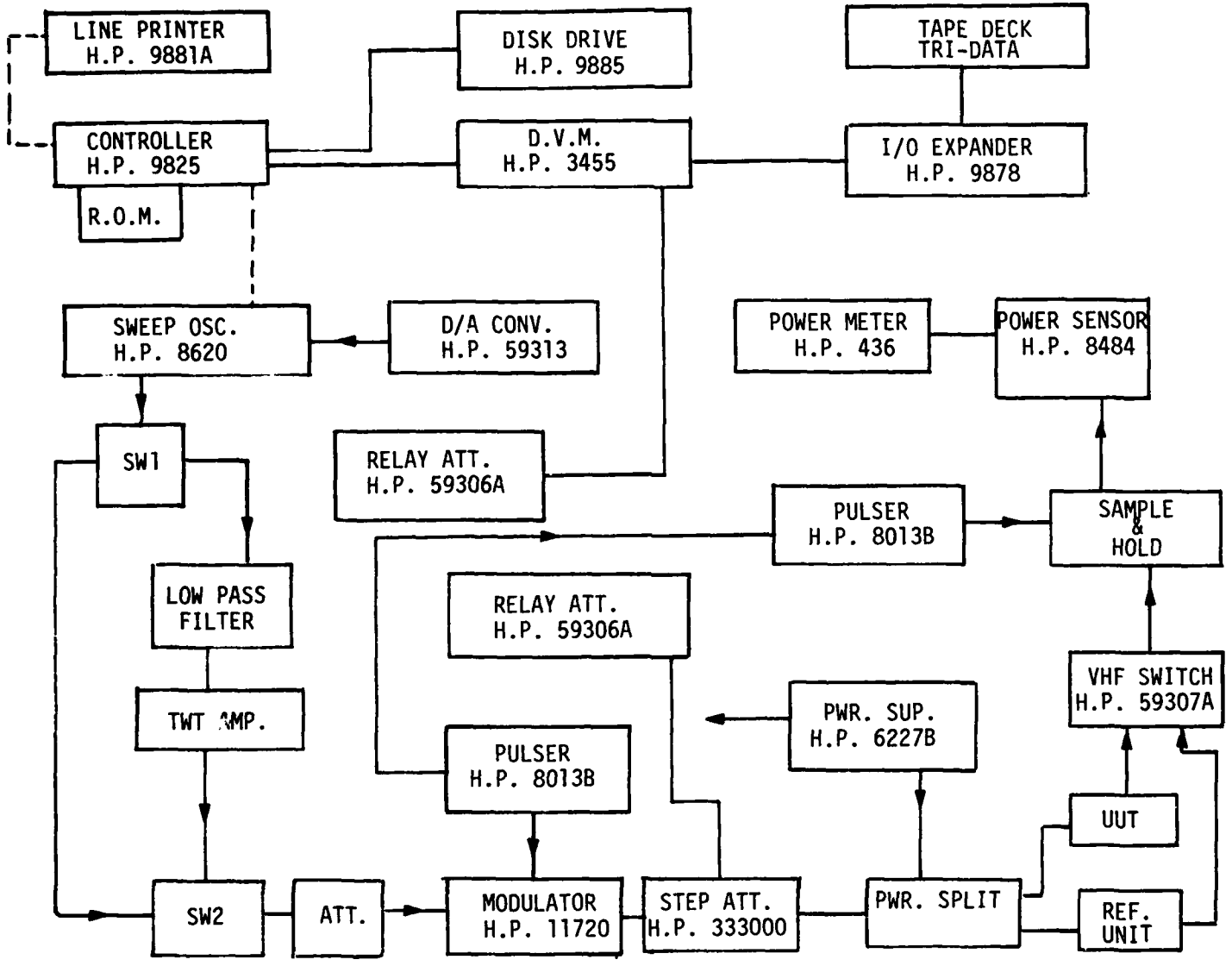



FIGURE 4 - INPUT DETECTOR POWER RESPONSE

FIGURE 5 - TEST SET



# PROGRESS REPORT ON NAVELEX MM & T THICK FILM AND DIRECT BOND COPPER

## 100 W MICROWAVE AMPLIFIER MIC PACKAGE

BY

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## ABSTRACT

This is a progress report on the work being done to improve the producibility and lower costs for the quantity production of 100 W microwave integrated circuits (MIC) modules. The areas identified for improvement were: certain processes peripheral to the basic Direct Bond Copper* (DB Cu) processes, glass seal and lid seal techniques, and testing/tuning. Qualification testing of modules built with these improvements will verify and complete the Manufacturing Methods and Technology (MM&T) program. Other applications of DB Cu in electronic packaging are also illustrated and described.

## INTRODUCTION

In November 1979 at ISHM[1], the author presented a paper entitled "MIC Package Using Thick Film and Direct Bond Copper for 100 W L-Band Power Amplifier" which describes the subject package (See Figures 1, 2, 3, 4 and 5). In September 1979 we were awarded an MM&T contract by NAVELEX (N00039-79-C-0378) for improving the producibility of the MIC in both the fabrication and test/tune areas with the object of reducing costs. The specific areas identified for improvement were:

1. Various peripheral processes related to the DB Cu operations such as:
   - Semi-automated equipment for cleaning and oxidizing copper prior to bonding.
   - Preblanking copper and developing locating fixturing for the substrate ground plane and the copper bonded to the top of the ceramic wall.
   - De-oxidizing all the copper after glass sealing.
   - Testing feed-through pins for continuity.

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* Direct Bond Copper is patented General Electric Company process.

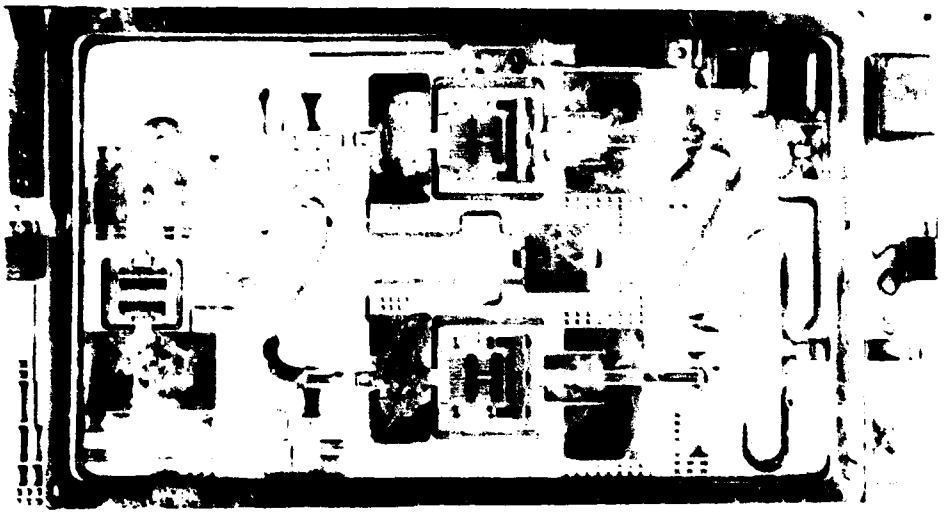


Figure 1. 100 W L-band Amplifier

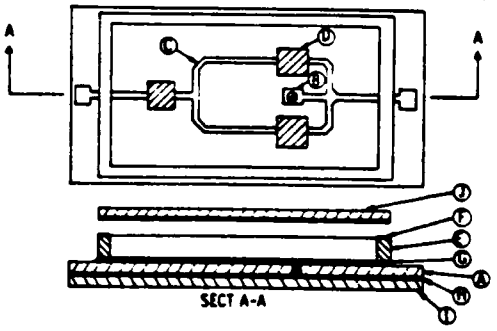



Figure 2. Module Assembly

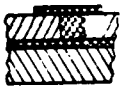


Figure 3. Section Through Ground Pin

Figure 4. Section Through Transistor Carrier

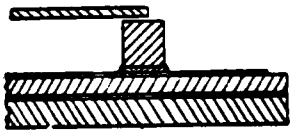


Figure 5. Section Through Wall and Micro Stripline

2. The glass seal between ceramic wall and substrate; change from air firing to nitrogen firing.

3. The F-15 Alloy (Kovar) lid to be changed from solder clad to plain nickel plated Kovar.

4. The manual tuning and testing of the MIC module to be changed to semi-automated tuning and testing.

After incorporating these improvements in the above manufacturing methods, the SOW (Statement of Work) requires the building of 25 electrical working modules using these methods to verify that product has not been compromised by virtue of these changes. Project is scheduled for completion in November 1980 when qualification testing of electrical working modules is completed, test results reported, cost benefits reported and drawings and processes are documented.

## PROGRESS

Progress to date, about 1/2 way in the program, has been good. This indicates that producibility can be significantly improved, resulting in cost savings and enhanced process repeatability for higher yields.

In the area of improving the peripheral DB Cu processes the following has been done:

1. The 10 wet chemical processing operation steps used for cleaning and oxidizing copper prior to bonding are being changed from a laboratory beaker operation to a semiautomated large batch operation. A programmable trolley system will be mounted above the processing tanks to transport and hold a batch of precut copper for cleaning and oxidizing. The tank locations and hold time in each tank will be programmed into the trolley so that the process will always be repeated. Only a part-time operator is required for loading and unloading the basket. Otherwise, all the operations will be performed by the machine without operator attendance. The system has been designed and is now in the process of being built. As a result of implementing this system, it is expected that significant labor costs reduction will be possible, and that more uniform products will be produced.

2. Considerable effort was required to develop the correct blank sizes for the 0.003 in. thick copper sheets used for the ceramic wall and the ground plane. No previous data existed which would have enabled us to predict the correct expansion factor to be applied to the copper blank prior to the DB Cu operation. Many iterations of different-sized etched blanks were used to "home in" on the correct size blanks. Hard blanking dies are now on order for the low cost production of precision blanks. In parallel with the blank size development, locating fixturing was developed to enable the precise locating of the blank with respect to the ceramic features. There

were complications involved in performing this task because of the high temperatures involved in the DB Cu operation (about 1100°C), the affinity of eutectic copper to most common fixturing materials, and the large dimensional tolerances on ceramics. This fixturing problem was most satisfactorily solved and the entire concept of using preblanked copper for the DB Cu process was proven. The labor cost savings realized by implementing this process are significant since it eliminates a long manual operation for hand trimming excess copper after the DB Cu operation to make the copper conform to the ceramic features.

3. The tedius and delicate chemical manual operations presently used for removing copper oxides, which form when making the air-fired glass seal, are to be replaced by a simple hydrogen reducing atmosphere belt furnace operation. Considerable work was done to develop this process. The ideal temperature, mixture of the reducing gas and belt speed had to be established to have the minimum affect on the thick-film copper bond strength and solderability, and on the thick-film copper-compatible resistors. A temperature of 350°C at a belt speed of 1.5 in. per minute with a mixture of 85% nitrogen and 15% hydrogen proved to be satisfactory.

4. An existing automatic continuity test equipment was fixtured for probing feed-through pins for continuity after the DB Cu operation. Labor cost was reduced with this automatic test vs the manual test method, previously used.

In the glass seal area, extensive work has been done in attempting to develop a nitrogen fireable glass to eliminate the oxidizing of copper. All efforts to date have been negative as far as finding a nitrogen fireable glass, but an improved air fireable glass was found. Additional work is being done to develop a better glass seal strength test method. In this connection a finite element model of the MIC package will be made to analyze the stresses within the package including the stress in the glass seal. This information will aid in developing an improved test method to provide a means of improving and evaluating our glass seal process for higher yields and lower costs.

Prior to this study the final lid seal was made with a special Kovar lid nickel plated on the top side and solder clad on the bottom seal side. Extra cost is involved in this approach both in the cost of the material (because of its special nature) and the labor cost associated with preparing the lid for sealing. We have now procured plain Kovar lids which do not require any preparation labor and will be lower in cost. This new approach was made possible now because the mating ceramic wall is now clad with DB Cu and is pretinned prior to final seal. Previously the wall had Moly-Mag refractory metalization with nickel-gold plating, and was dependent on the solder clad lid for the source of solder for making the final seal. Results to date are exceedingly good. The seal yields remain high (95% range), labor cost is reduced, cost of the lid is reduced, and the seam-sealing fixturing and process required only a minor change in power from 750 A to 850 A.

Prior to this study testing and tuning of the completed fully assembled MIC module had evolved into a complex manually performed iterative test and tune

procedure, frequently requiring engineering personnel to perform these tests and analyze the data. Frequently the better part of a day (6 to 8 hours) was required to test one module. A new automatic test station for tuning/testing RF modules and transistor networks has been designed, built and is now implemented (See Figure 6). This station logs data, analyzes and plots the data, instructs test personnel step-by-step through the test and tuning procedure, stores data on floppy disc for complete component traceability and enters data into the main frame computer for module engineering analysis. Early use of this test system has demonstrated that at least 75% labor savings are achieved, and that lower skilled test personnel can perform the test and tuning functions.

Work has not yet started on the final phase of the program, that is, building 25 electrically functioning modules to prove processes and then verification by performing qualification tests.

Having acquainted the reader with DB Cu and its application to the 100 W MIC module, it is opportune to briefly illustrate other applications of this process in electronic packaging. Figure 7 shows a 50 Ω RF stripline load designed to be solder mounted in a hole in a PPO (polyphenylene oxide) stripline. It will be soldered to the ground plane on one side and to the stripline on the other side. The beryllia ceramic is able to rapidly dissipate the heat dumped into the thick film resistor via the DB Cu and onto the stripline copper ground plane. The very high bond strength (20,000 lbs/in.$^2$) of the copper base and leads attached to the beryllia provide extremely reliable connections enabling it to withstand very high power bursts. The present limitation on power appears to be the melting of the solders used to attach the load to the stripline. The cost of producing this two-piece load assembly with DB Cu is significantly reduced as compared to the original four-piece assembly (See Figure 8) which is very important in view of the large number used in each solid-state radar. A similar packaging concept is shown in Figure 9 for a high-power microwave chip carrier, wherein one piece of DB Cu is used for the base, leads, and the chip and network mount.

Figure 10 shows a much larger power hybrid beryllia substrate non-hermetic package with extended DB Cu leads. Figure 11 shows an approach towards using DB Cu for making a weldable integral substrate package (ISP). This design permits welding of a DB Cu lid to DB Cu on top of a hermetic wall using a Nd-YAG laser. Initial work shows promise both in the ease of performing the welds and in the results of environmental tests on the package through temperature cycling and shock tests.

Time does not permit presenting many other novel applications of DB Cu to electronic packaging, but a few words on its salient features with respect to packaging may be of interest. Because of the intimacy of the bond between the copper and the ceramic, the copper yields to the coefficient of expansion of the ceramic without rupturing the bond provided that the proper thickness proportions are not exceeded. This characteristic provides a valuable tool to the designer in matching expansion coefficients of ceramics, silicon and metals. In addition, the copper metal used in the DB Cu process provides excellent electrical and thermal conductivity.

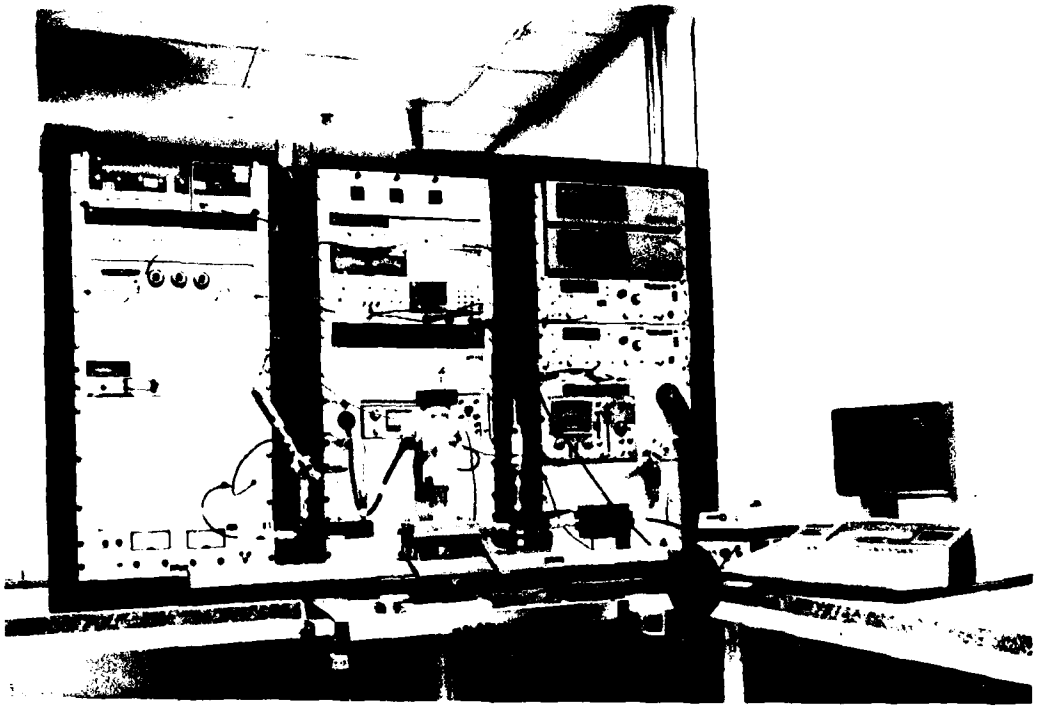


Figure 6. Automatic RF Test Station

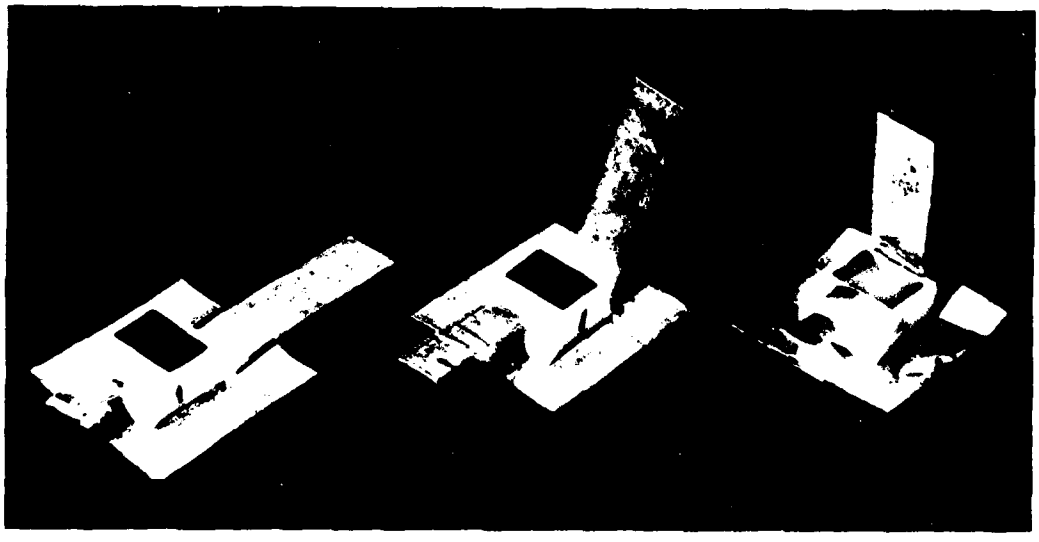


Figure 7. DB Cu Version of 50 Ω Load

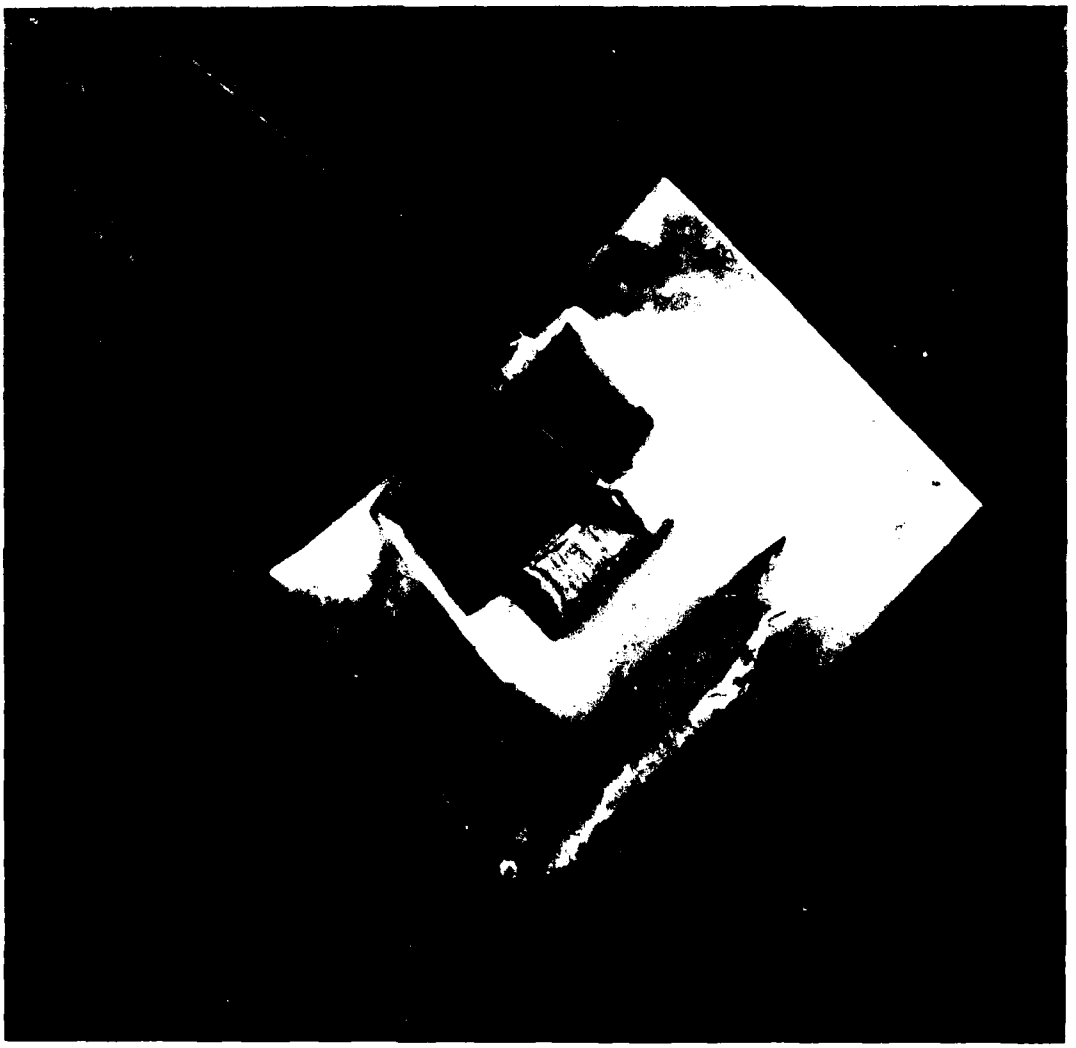


Figure 8. Soldered Version of 50 Ω Load

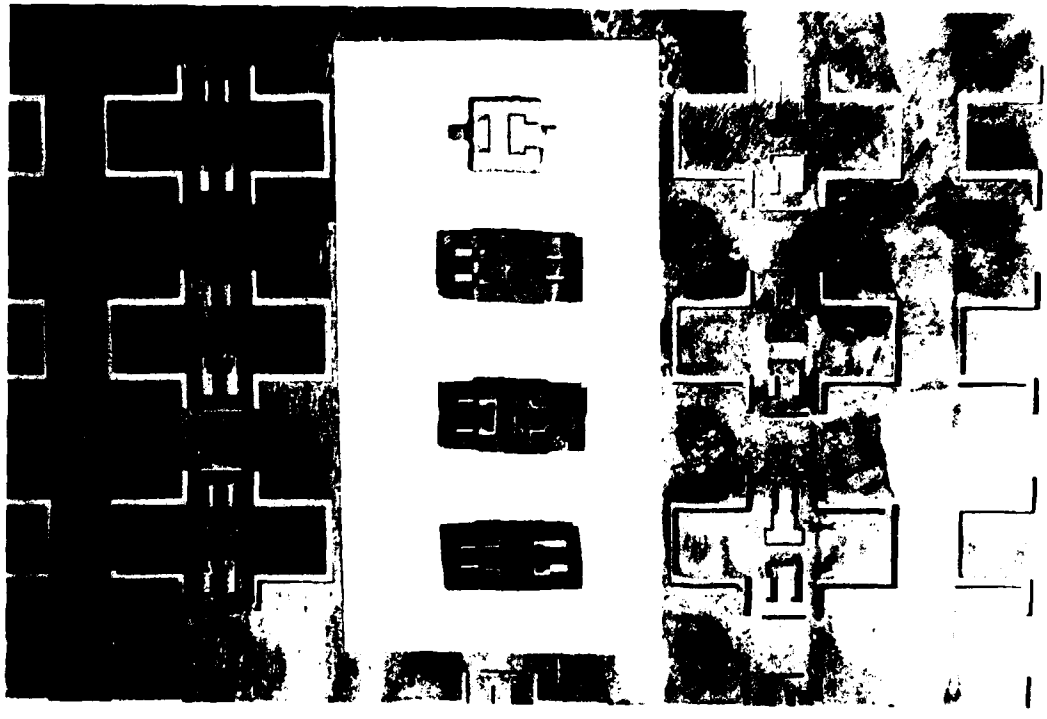
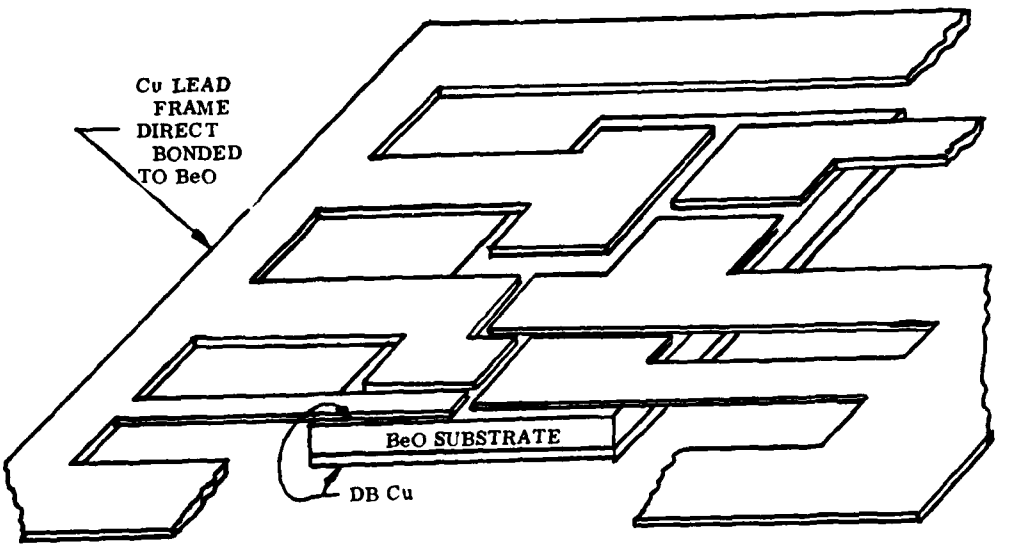
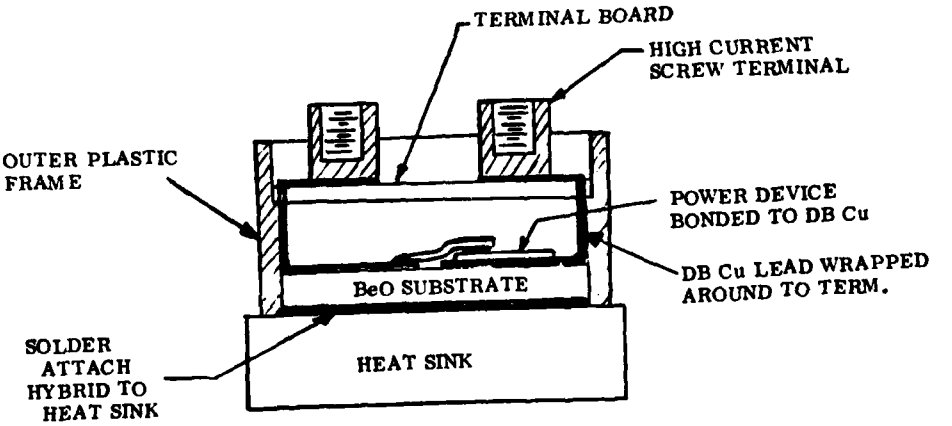


Figure 9. DB Cu RF Transistor Chip Carrier

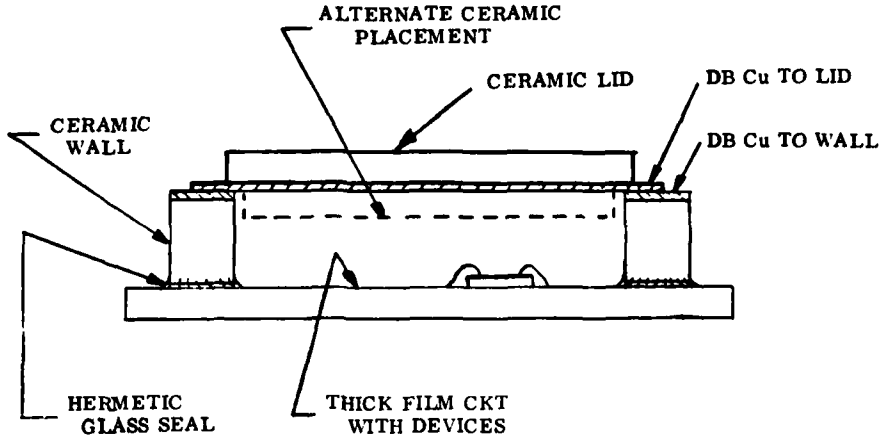


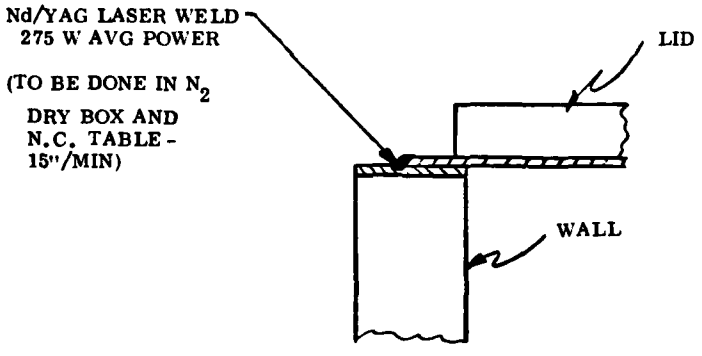

HYBRID SUBSTRATE




HYBRID ASSEMBLY

Figure 10. DB Cu (Integral Leads) High Power Hybrid




BLOW-UP OF Cu TO Cu WELD

Figure 11. ISP-DB Cu Welded Package

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# ULTRA HIGH FREQUENCY CHIP CAPACITORS

BY

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## ABSTRACT

A critical requirement from the hybrid microcircuit industry to develop a high reliability, high frequency chip capacitor in the shortest timeframe has been completed. Single-plate chip capacitors have been designed to offer advanced performance in hybrid microcircuits - namely, to increase the useable frequency range to 36 gigahertz.

Proprietary materials and processes were developed inorder to fabricate this ceramic chip capacitor. Unique ceramic tapes provide a non-porous structure; and impart low loss and excellent stability over an operating range of -55 to +125°C. A nickel-gold electrode system provides a low resistance film with excellent solder or epoxy attachment and wire or ribbon bonding properties. A special pelletizing process provides a micro-chip configuration with uniform, precise, and sharply defined electrodes and edges; and close capacitance tolerances down to $\pm$.01 picofarad.

After manufacturing feasibility was demonstrated, processes were scaled up to establish a manufacturing capability. A total quality system was developed to monitor all incoming materials and in-process and finished products. The reliability of these capacitors has been proven by extensive voltage conditioning and life test programs.

These chip capacitors are used as D.C. blocking, coupling or bypass elements. The key to optimum circuit performance has been the ability to maintain tightly controlled mechanical tolerances, which permits a matching of the capacitor and transmission line widths, and significantly minimizes disturbances and discontinuities.

## INTRODUCTION

The wide use of striplines in this age of circuit minaturization has ultimately resulted in the need for a high reliability, high frequency chip capacitor. M.O.S. capacitor chips were primarily used initially in these microcircuits, where the width of the transmission line was below .050 inches. Catastrophic problems were encountered with the M.O.S. capacitors due to their fragility and the fact that the thin dielectric layer was highly susceptible

to a punch-thru type failure mechanism caused by surface changes. High failure rates near the ninety percent level were noted by many microcircuit manufacturers.

It has not been possible with known devices to accomplish the blocking, coupling or bypass functions without introducing concomitant loss to the circuit, due to (1) the capacitor protruding upward from the board and stripline; (2) size differs from stripline; (3) electrodes were not parallel; and (4) weak or inductive connections.

The unsatisfactory performance of existing capacitive devices resulted in a request from many microcircuit manufacturers to develop an improved device with low losses and one that would readily bond to a transmission line. This paper describes all phases from design thru manufacturing in the new product syndrome of a ceramic chip capacitor.

## DESIGN OBJECTIVES

An ideal transmission line is one where there is no change in geometry along the path of propagation. Any change in geometry along a transmission line will form a discontinuity as shown in Figure I. Discontinuities in transmission lines will launch higher order modes and energy will be stored.

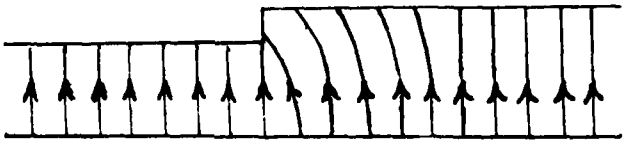


Figure I: Discontinuity on a transmission line

The objectives of this development program were basically threefold, namely, to develop (1) a low loss and stable dielectric material; (2) compatible electrode system; and (3) optimum chip configuration, inorder to minimize discontinuities in the transmission line, and increase the useable frequency range. Figure II shows the basic construction of a ceramic chip capacitor.

Figure II: Chip capacitor construction

## MATERIALS AND PROCESS DEVELOPMENT

A. Dielectric Formulations - Three classes of dielectric materials were investigated; low (NPO), medium and high K materials. Samples of ceramic tapes were prepared using standard ceramic techniques as outlined in Figure IV, Process Flow Chart. A proprietary dielectric formulation, binders and solvent are milled for a specified time. Thin sheets are cast using the doctor blade technique, dried and punched into 1.5 by 3.0 inch plates. Several different firing cycles were developed, since each dielectric material required a different firing cycle, inorder to achieve a non-porous structure that is impervious to moisture and solvents.

Ceramic plates of each composition were electroded, pelletized and evaluated both mechanically and electrically. All ceramic plates had a non-porous structure. The dissipation factor and temperature coefficient data is summarized in Table I for each composition. Compositions 560 and 572, which are low K and NPO type materials, exhibited the lowest loss and best temperature stability over the temperature range of -55 to +125°C.

TABLE I

Dissipation Factor and Temperature Coefficient of Capacitance Data

| Composition Number | Material | Dielectric Constant | DF | TC |
|---|---|---|---|---|
| 560 | Magnesium/Calcium Titanate | 20 | <.001 | 0±15ppm/°C |
| 572 | Barium/Neodymium Titanate | 60 | <.001 | 0±30ppm/°C |
| 612 | Calcium Titanate | 155 | <.002 | N1450ppm/°C |
| 630 | Strontium Titanate | 280 | <.002 | N2400ppm/°C |
| 620 | Barium/Calcium Titanate | 440 | <.004 | N3800ppm/°C |
| 617 | Barium Titanate + Transition Metal | 1000 | <.020 | ±10% |
| 582 | Barium Titanate/Additives | 1500 | <.025 | +15% |
| 589 | Barium Titanate | 4500 | <.025 | ±10% -70% |

B. Electrode System - Two basic metalization systems were investigated, namely, (1) an electroplated gold electrode with a nickel barrier; and (2) a silver electrode. The nickel-gold system was applied to the tape using proprietary plating techniques. The silver electrodes were applied using standard thick film techniques. The gold electrode proved to be superior in all aspects - (1) had lower resistance; (2) more conducive to attachment to the gold transmission line; (3) better resistance to leaching during solder attachment due to the presence of the nickel barrier and (4) more readily bondable with wire or ribbon (a gold

thickness of 100-125 microinches was found to be the optimum thickness for bonding). The silver electrode system exhibited poor performance at high frequencies and appears not to be suitable for today's technology.

C. Pelletizing process investigated consisted of mounting the electroded ceramic plate on a ceramic block with an adhesive material and then dicing the plate using a diamond blade into the desired size. Several waxes and epoxy materials were evaluated to mount the ceramic plates and a two component epoxy system proved to be superior. Different cutting cycles were required due to the varying hardness and strength of the different dielectric materials. An intensive cleaning process was required inorder to remove all traces of the mounting material.

This unique pelletizing process provided a micro-chip with uniform, precise and sharply defined electrodes and ceramic surfaces and a wide range of capacitance values with close tolerances down to $\pm$.01 picofarad. Chip dimensions of .005 inches square have been supplied to customers.

## MANUFACTURING PHASE

After product feasibility was demonstrated, a manufacturing capability was established. A parallel scale-up approach was utilized to provide the capability to produce large quantities of units. Instead of acquiring one larger size piece of equipment to perform an operation, additional smaller systems similar to those used for pilot phase quantities were acquired to perform each operation as outlined in Figure IV, Process Flow Chart.

A quality plan was established to monitor the incoming materials and in-process and final products inorder to maintain conformance to the required quality levels.

## DEVICE PARAMETERS

Table II contains the electrical and mechanical properties measured on these ceramic chip capacitors.

Table II Electrical and Mechanical Properties

| | |
|---|---|
| A. Electrical | |
| Capacitance Range | .02 picofarad - .03 microfarad |
| Insulation Resistance | $>10^6$ megohms |
| Voltage Rating | 50 - 500 WVDC |
| Dielectric Withstanding Voltage | 250% of WVDC |
| Series Resistance | $<$.010 OHMS |

B. Mechanical

| | |
|---|---|
| Size Range | .010" to .500" square |
| Thickness Range | .003" to .150" |
| Hermeticity | non-porous |
| Mechanical Strength | High strength - breaking strength is 10 times greater than M.O.S. chips |

## HIGH RELIABILITY PROGRAM

These parallel plate capacitors have been approved for use in such programs as Intelsat, Insat, TDRSS, DSCS, HARM, PELSS and a variety of F-16 and F-18 associated programs.

Extensive voltage conditioning and life testing has been performed on units with a wide range of capacitance values.

Voltage conditioning testing: Conditions-all units are subjected to a temperature of +125°C with twice the rated voltage applied for a period of 168 hours. After completion of exposure, the dielectric withstanding voltage, insulation resistance, capacitance and dissipation factor are measured. The results are summarized in Table III.

Life testing: Conditions-all units are subjected to a temperature of +125°C with twice the rated voltage for a period of 2000 hours. Measurements of dielectric withstanding voltage, insulation resistance, capacitance and dissipation factor were performed at the completion of 0, 250, 500, 1000 and 2000 hours of exposure.

Table III Voltage Conditioning/Life Test Data

| Test | Number of Tests | Number of Units | Rejected Units | % Defective |
|---|---|---|---|---|
| Voltage Conditioning | 26 | 2358 | 1 | .04 |
| Life Testing | 90 | 7256 | 5 | .07 |

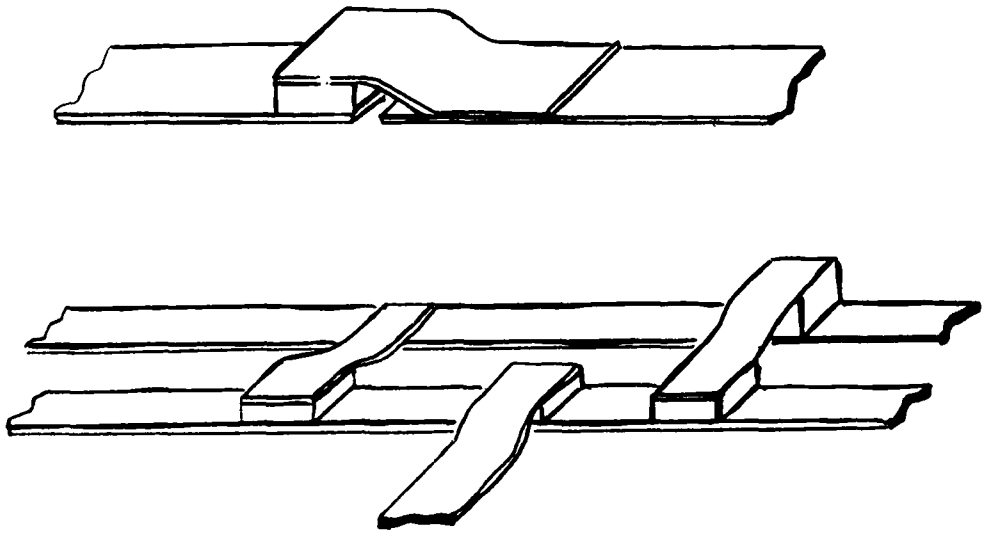
## APPLICATIONS

The three main applications of this chip capacitor are as follows:

A. D.C. blocking - where one side of the circuit is at one D.C. potential and another side at another potential
B. Coupling - capacitive coupling from one line to another - phase shifting one is connected to another by means of a capacitor.
C. Bypassing - to remove spurious or unwanted signals

Figure III shows various techniques for assembling the capacitors.

Figure III: Capacitor Assembly Techniques



## CONCLUSION

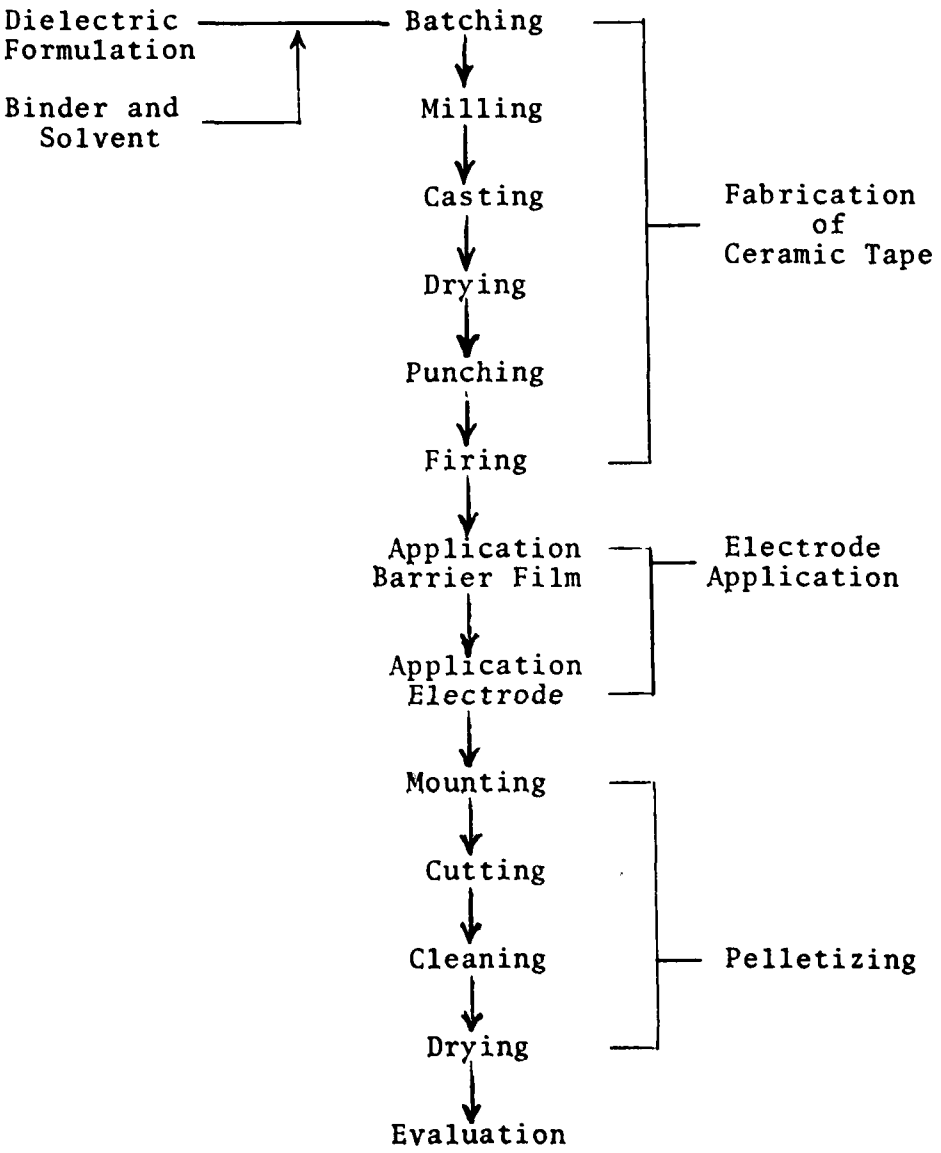
This ultra high frequency chip capacitor provides the design engineer with a high reliability device for applications up to a frequency of 36 gigahertz.

Tight process controls provide the process repeatability to fabricate a consistent, stable, low loss capacitor.

The ability to maintain close mechanical tolerances and provide the optimum configuration significantly minimizes discontinuities in the stripline circuit.

Extensive voltage conditioning and life test data have demonstrated that the capacitor has excellent stability.

Figure IV: Process Flow Chart



# STATUS OF COPPER THICK FILM HYBRIDS

BY

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## ABSTRACT

An understanding of the material and processing relationships is fundamental to the successful application of copper thick film systems. This understanding was obtained through a complete functional study of commercial materials and was expanded to include in-house synthesis of thick film pastes. The culmination of the effort was the definition of a processing window to achieve copper/dielectric multilayer microcircuits. The ability to control the material interactions has led to the successful transfer of copper-based systems from the laboratory to manufacturing.

Environmental stress tests have shown that copper hybrids are more susceptible to corrosion, oxidation and humidity effects than air fireable systems. This behavior has been found to be related in part to the processing of dielectrics in a nitrogen atmosphere which yields a more porous structure. Both material selection and processing conditions contribute to the extent of porosity; it can be reduced by choice of the dielectric glass, vehicle and the refractory/glass ratio. Modified processing procedures involving improved paste drying, infrared heating schedules and $O_2$ doping have promoted optimum vehicle removal with a resultant increase in dielectric density.

Long-term reliability is under investigation to determine the effect of moisture on the insulation properties of multilayer systems. At present, the application of copper thick film systems for use in hostile environments will require protection.

## INTRODUCTION

Microelectronic packages are being employed in a large variety of sophisticated devices and complex systems. Technology forecasts for both military and commercial applications indicate that this use will increase signficantly as new and expanding applications are pursued.

At present, most of the electronic packaging needs are being met successfully with precious metal thick film hybrids. The recent price escalation of precious metals has increased the incentive to identify alternative non-noble metals, e.g., copper, as a direct replacement for noble metal systems. Within the last few years there has been significant progress in both

materials and processing of non-noble systems resulting in copper based compatible material systems (Ref. 1-5).

We will review the present status of copper based thick film systems by examining and comparing the cost/performance character of various metal systems. The material interactions, i.e., blistering, diffusion, delamination and dendrite formation will be discussed along with methods for modifying the material systems and processing conditions to control them. Next, the functional properties and reliability of these systems will be related to material interactions. The result is a compatible high quality copper based multilayer thick film system.

## COPPER BASED HYBRID MICROCIRCUITS

The basic motivation for use of copper based systems as a direct replacement for noble metal systems is due to both cost and performance factors. A cost analysis for a gold and for a copper based multilayer system is shown in Figure 1 (prices as of May 1980). There is a 36 percent savings by use of copper for this example. The cost analysis does include labor, materials such as the dielectric and substrate as well as the $N_2$ for high temperature firing.

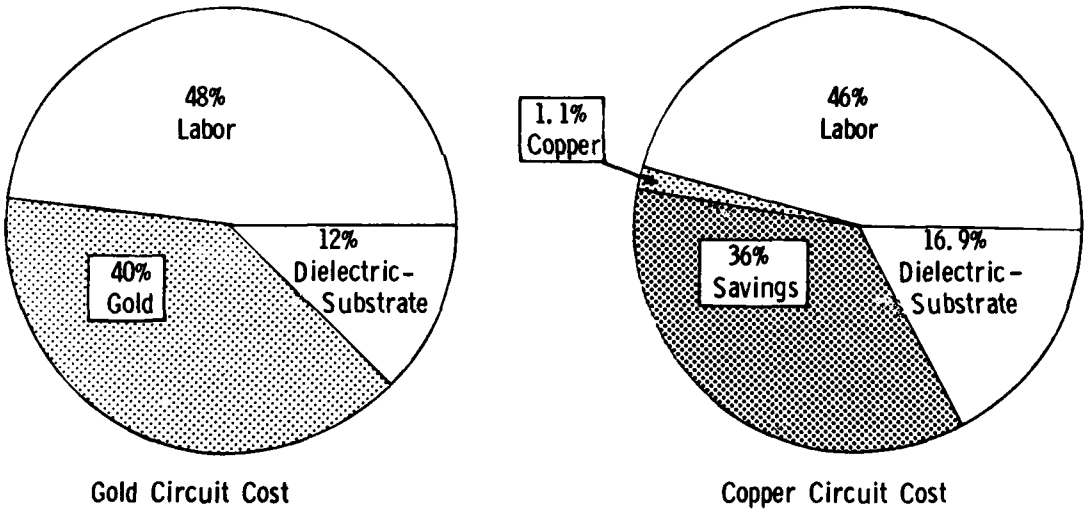



Figure 1. Cost comparison of multilayer gold and copper hybrid circuits.

Functional properties of copper systems may also offer advantages for certain applications. Copper based thick film systems provide very low resistance conductor networks; comparable to gold and better than gold or silver alloys. Adhesion strength is also very high; higher than gold and comparable to gold and silver alloy based systems. The specific properties

of various noble and non-noble systems along with relative thick film paste costs are shown in Table 1.

Table 1. Cost/Performance Comparison of Noble vs Base Metal Systems.

| Conductor Material | Resistivity mΩ/□/mil | Adhesion 2.4 mm sq/pad | Bonding Method | Processing Atmosphere | Cost $/gm |
|---|---|---|---|---|---|
| Au | 1- 2 | 4-5 | S/W | Air | 23 |
| Pt/Au | 20-45 | 6-7 | S/W | Air | 24 |
| Pd/Ag | 7-25 | 8-10 | S/W | Air | < 3 |
| Cu | 1- 2 | 6-8 | S | $N_2$ | < 1 |
| Ni | 30-50 | -- | M | Air | < 1 |
| Al | 16-45 | -- | M | $N_2$ | < 1 |
| W | 3- 5 | -- | M | $H_2$ | < 1 |

S = Solderable
W = Wire Bondable
M = Surface Metallization Required

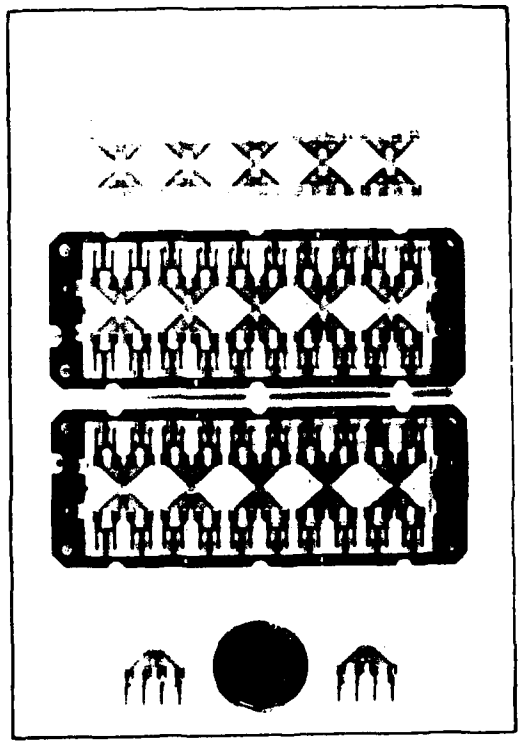
These cost/performance features have led Honeywell and others to investigate copper as a direct replacement for both gold and silver based systems. Two specific products in which this will occur at Honeywell are shown in Figures 2 and 3. Figure 2 shows a copper thick film circuit which is planned for 1980 production in a Honeywell Micro Switch keyboard product line. In this example the copper thick film paste will be replacing a silver-palladium paste. A high density multilayer conductor/dielectric system being used by Honeywell's computer division is shown in Figure 3. In this case the copper will be replacing a gold thick film system which was discussed at the recent Electronics Components Conference (Ref. 6).

The progress made in both materials and processing of copper based systems has provided the opportunity to introduce these new products. Interactions which a few years ago resulted in adverse performance can now be controlled to provide stable multilayer structures. The observations and ultimate control of these interactions are discussed in the next section.

## INTERACTIONS

Copper is a chemically active material even in neutral atmospheres at normal thick film processing temperatures, i.e., $\sim 900^{o}C$ and therefore some material interactions can be expected to occur. Metallographic cross-sections to observe the interactions were prepared and examined. In addition, thick film multilayer structures were subjected to a stress condition, e.g., a pre-oxidation treatment. Then during the entire drying and firing sequence microscopic observations were made and photomicrographs taken to record the condition of the specimen surface at every stage of the process. This provided a pictorial record of the changes during the processing sequence.

Figure 2. Copper thick film circuit used in Micro Switch Hall chip microcircuit.



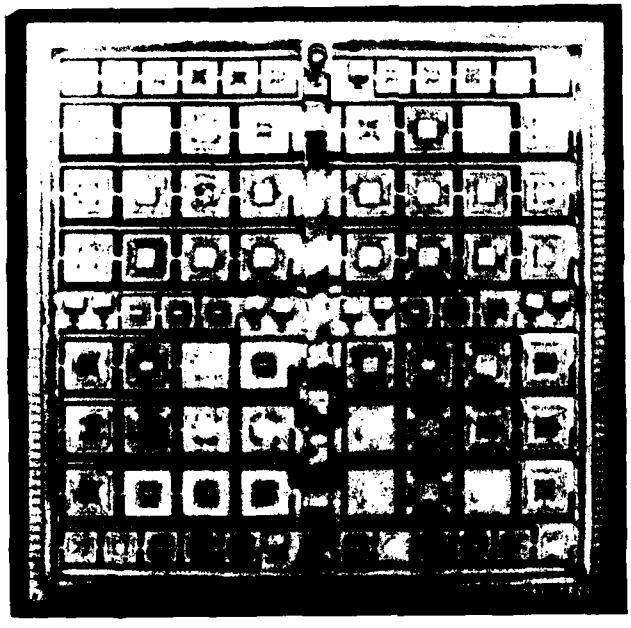


Figure 3. Copper conductor/ dielectric multilayer system for use in Honeywell computer microcircuit.

Typical of the interactions observed are surface oxidation, copper interdiffusion, inner layer delamination, blistering and dendrite formation. Examples of these interactions are illustrated in Figure 4. Composition, processing conditions and environmental stress were all found to contribute to defects noted in this multilayer structure. In the following paragraphs we will discuss breifly each of the interactions and their control.

Diffusion

Diffusion or penetration of copper into the dielectric film was found to be related to the type of glass and glass/refractory ratio in the dielectric. Observations using the microscope hot stage showed that the penetration of copper began suddenly at a specific temperature and progressed so rapidly that it could be observed as it moved into the dielectric. The existence of a temperature threshold and the rapid progress of the penetration are typical of a liquid phase reaction rather than solid state diffusion. The "diffusion" phenomena is therefore an incipient melting effect, and for this reason is strongly dependent upon the presence and the amount of low melting oxides in the dielectric. In no case has diffusion of copper into the high $Al_2O_3$ substrate been observed.

This interaction results in a decrease of the adhesion properties and insulation resistance (dielectric). It is also frequently accompanied by blister formation. The extent of diffusion depends on firing temperature, copper oxide content and composition of the dielectric. The diffusion zone in the dielectric was identified as $Cu_2O$ by cross-polarized light microscopy and confirmed by Auger analysis. The concentration profile was measured using electron beam microprobe analysis. Copper dendrites as shown in Figure 4 also have been observed within the glass phase present in the copper thick film paste.

Blistering

Blistering observed during repetitive firing of multilayer systems has been attributed primarily to material factors such as impurity interactions, non-wetting of surface defects and gas evolution during vehicle burnout. Processing can indirectly affect blistering for example by increasing the $Cu_2O$ content of the thick film structure. The higher the copper oxide content, the greater the tendency for blistering.

Observations were made using the hot stage microscope to determine the temperature at which blistering was initiated, effect of degree of copper pre-oxidation and the relationship of blistering with dielectric composition. The conclusions from these observations were:

- The number and size of blisters in copper pastes increases with copper oxide content of the dried paste.
- The initiation of blistering in copper thick films occurs at much lower temperatures as copper oxide content increases.

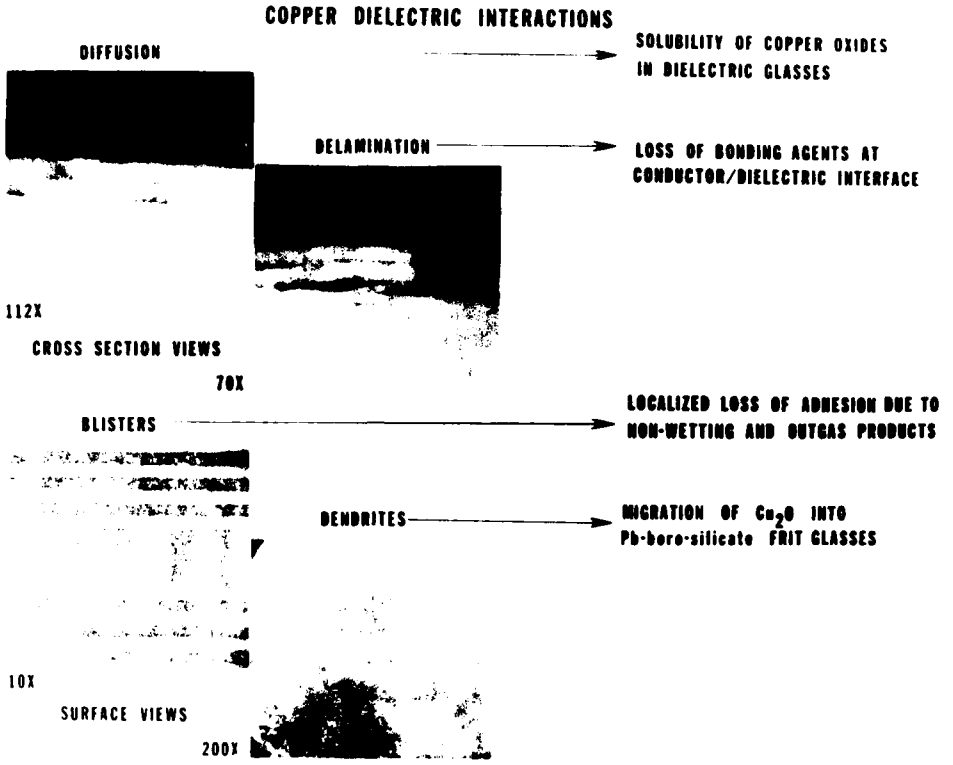



Figure 4. Photomicrograph showing the various interactions between conductor and dielectric.

- Blisters can occur in dielectric films but only at temperatures over 900°C.

In every case the blistering behavior in the systems was accentuated in the hot stage furnace when compared to a similar test in a conveyor furnace. This was especially true for dielectric blisters which were never observed as a result of firing in a conveyor furnace.

Delamination

Separation of conductor and dielectric shown in Figure 4 occurred in our investigations with only a specific set of materials or with unusual processing conditions associated with reducing atmospheres. Introduction of $H_2$ at 100 ppm levels results in a separation of dielectric from inner layer copper which we believe was caused by a reduction of the oxides present during firing. Higher $H_2$ concentrations (1000 ppm) discolored the dielectric films and caused total loss of conductor adhesion. Loss of bonding agents can also occur by improper ventilation of reducing vapors during

vehicle pyrolysis as noted in firing of very thick (greater than 30μm)dielectric films over a prefired conductor layer.

In summary, these observations of diffusion, blistering and delamination indicate that they are composition and processing dependent. Furthermore, the interactions are accelerated by multiple high temperature firings and if not controlled will result in structures as shown in Figure 5.

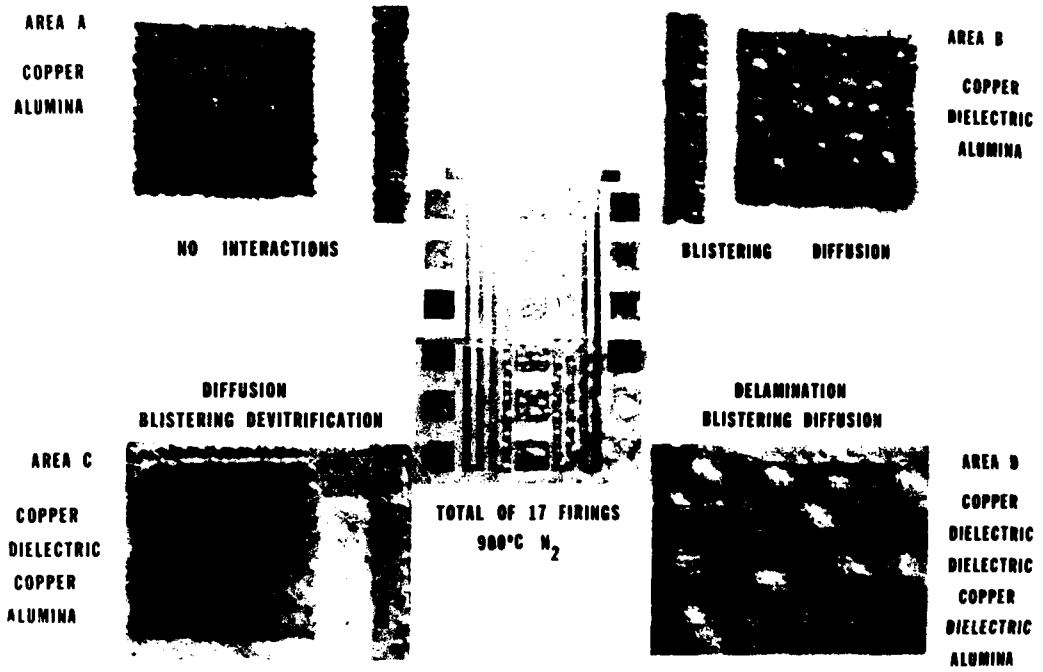



Figure 5. Copper multilayer structure showing effect of adverse interactions.

## FUNCTIONAL PROPERTIES

The electrical and mechanical properties of multilayer structures will deteriorate as a result of the interactions described above. Examples of this behavior are presented in Table 2 for three commercial copper/dielectric systems. The severity of blistering and copper diffusion increases with repetitive firings and is dependent on the material combinations. Decreases in the insulation values tend to track with increased boundary diffusion although these values measured are acceptable from an electrical standpoint. Severe diffusion is always accompanied by blistering and the dielectric loses its structural integrity.

Adhesion measurements on 2.4 mm sq/pad using a DuPont solder pull/peel test showed a decrease in pull strength proportional to increased blistering

Table 2. Compatibility Effects on Copper Hybrid Functional Properties.

| Copper/ Dielectric | 900°C Temp Cycles | Diffusion Boundary (μm) | Insulation Resistance (ohms) | Blister Density | Adhesion Pull/lbs |
|---|---|---|---|---|---|
| DuPont 9923/ DuPont 9949 | 1 | 50 | $1.5 \times 10^{13}$ | None | 8.7 |
| | 3 | 57 | $6.7 \times 10^{11}$ | Few | 8.0 |
| | 6 | 114 | $1.1 \times 10^{10}$ | Severe | 5.6 |
| DuPont 9923/ DuPont 4016 | 1 | 14 | $1.3 \times 10^{11}$ | None | 7.0 |
| | 3 | 43 | $1.4 \times 10^{11}$ | None | 7.0 |
| | 6 | 50 | $2.9 \times 10^{10}$ | Few | 6.3 |
| DuPont 9923/ ESL 4901 | 1 | None | $5.0 \times 10^{12}$ | None | 7.8 |
| | 3 | Slight | $1.0 \times 10^{12}$ | None | 7.6 |
| | 6 | Slight | $1.0 \times 10^{12}$ | Few | 6.8 |

as expected. Dielectrics with high alumina to glass contents (4901) and with different types of glasses, (4016) as compared to (9949), will improve the compatibility behavior.

## PROCESSING WINDOW

The evidence developed in the investigation of the interactions support the validity of a processing window in which all the factors: composition, process parameters and functional properties are brought into balance to provide a compatible system. Early work on paste synthesis (Ref. 3) proposed such a window for dielectrics as shown in Figure 6. Presented in the figure are the compatibility regions for copper films processed on in-house dielectric materials (D-58 through D-63). The processing window defines a narrow zone where acceptable thick film properties were obtained with respect to blistering tendencies, diffusion behavior and insulation properties. Blistering and diffusion are more severe with higher processing temperatures on the glass rich side of the dielectric compositions. High refractory content improves compatibility but leads to more porous dielectrics which are moisture sensitive. These findings show that both material selection and processing controls are essential to process compatible copper thick film hybrids. Recent commercial conductor/dielectric systems support this concept. In addition if multilayer hybrid microcircuits are processed according to the above conditions high quality compatible structures can be obtained. An example is shown in Figure 7. This can be compared to earlier status shown in Figure 5.

## RELIABILITY

The development of compatible material systems now permits us to assess long term reliability. Thermal aging studies and environmental tests were made on experimental microcircuits and on multilayer packages populated with integrated circuits. Results of these studies are summarized briefly below.

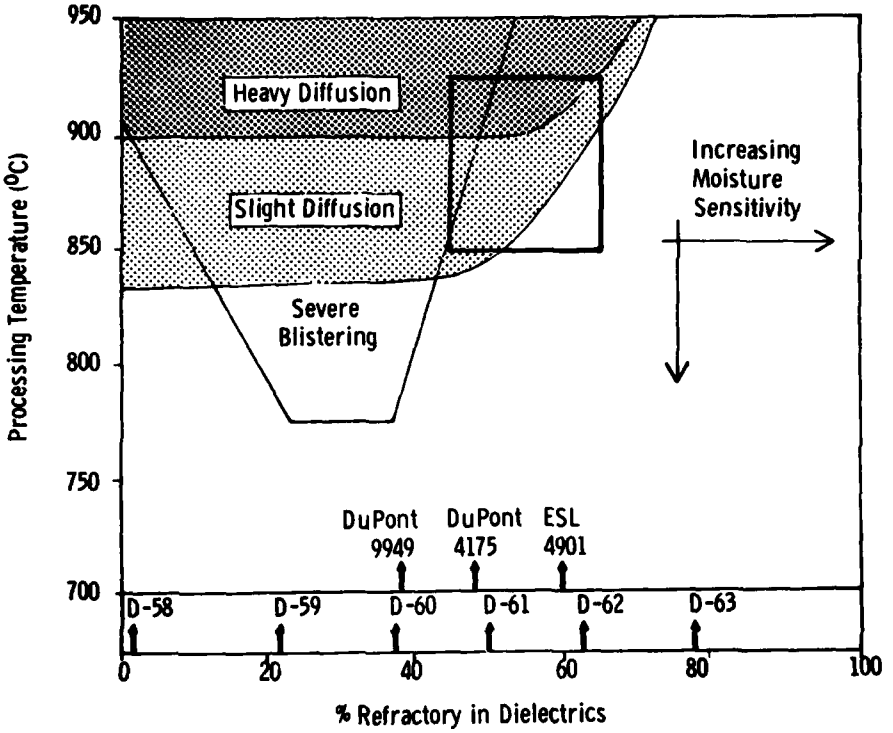



Figure 6. Processing window for compatible copper thick film hybrids.

| | |
|---|---|
| Solderability | Excellent, PbSn solders |
| Solder Leaching | 8 - 10 reflow cycles demonstrated |
| Adhesion (2.4 mm. sq. pad) | |
| Initial | 6 - 8 lbs. |
| Aged (120°C, 2000 hrs.) | 4 - 5 lbs. |
| Thermal Cycle (-55°C to 125°C) | No degradation after 50 cycles |
| Thermal Shock (-50°C to +50°C) | No degradation in bond strengh after 15 cycles |
| Environmental Exposure | |
| Ambient (2000 hrs.) | No degradation in properties |
| <70% RH (2000 hrs.) | No degradation in properties |
| 85°C/85% RH (2000 hrs.) | Reduction in insulation properties |

Electrical and mechanical performance showed little or no degradation in conductor or dielectric properties during ambient operation or after elevated temperature storage when moisture levels were less than 70% RH. Exposure to higher moisture levels such as 85% RH at 85°C or 90% RH at ambient temperatures will rapidly reduce dielectric insulation properties. In situ measurements at high humidity show transient electrical shorts, lower breakdown voltage and increased dissipation properties. All these effects are transient and the properties will recover to their initial value when removed from

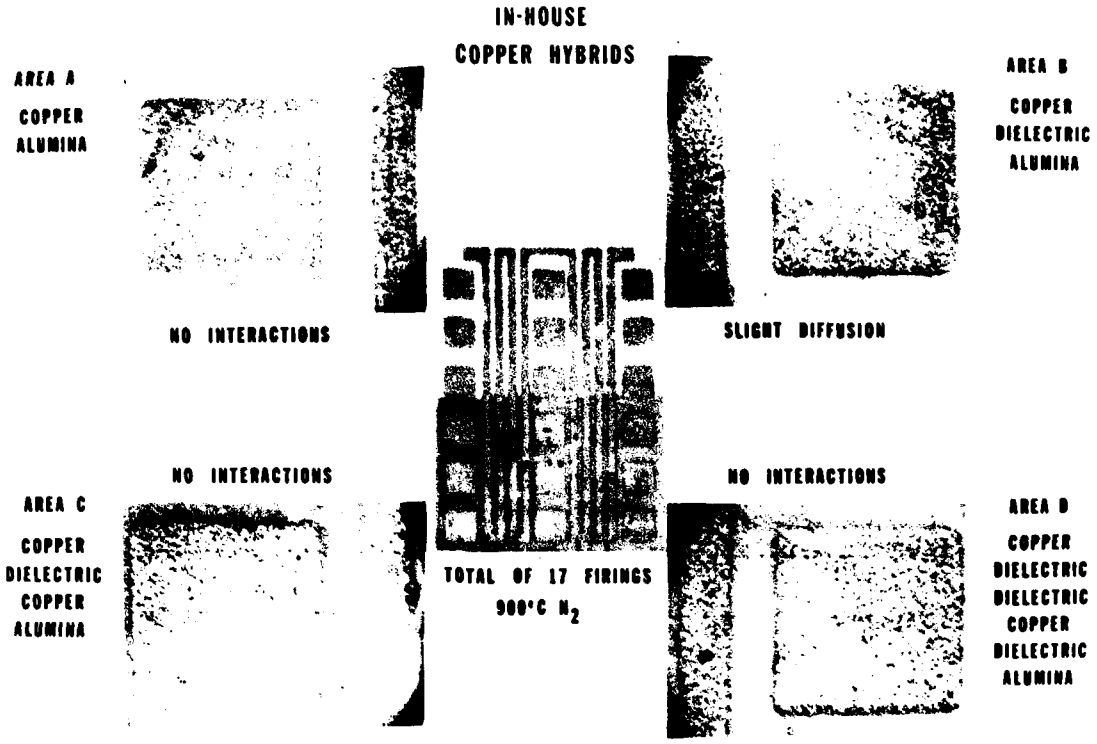



Figure 7. Copper multilayer Structure showing compatible structure.

the high humidity environment. Precious metal systems give a similar response to humidity but to a lesser degree. The extent of moisture sensitivity for copper systems is directly related to the dielectric density with the more porous structures exhibiting the greater change. In summary, solderability, adhesion and thermal behavior of copper hybrids will meet standard system requirements.

## PROCESSING MODIFICATIONS

It is possible to improve as-fired dielectric density by more effective drying and/or firing schedules (Ref 5, 6). Figures 8, 9, and 10 show the structure of the same dielectric processed under three different conditions. Dielectrics fired in air show a very dense structure with a limited amount of porosity (Figure 8). Standard processing in nitrogen will result in a more porous structure as shown in Figure 9. Use of IR drying prior to nitrogen processing improves vehicle removal thereby increasing dielectric density, Figure 10.

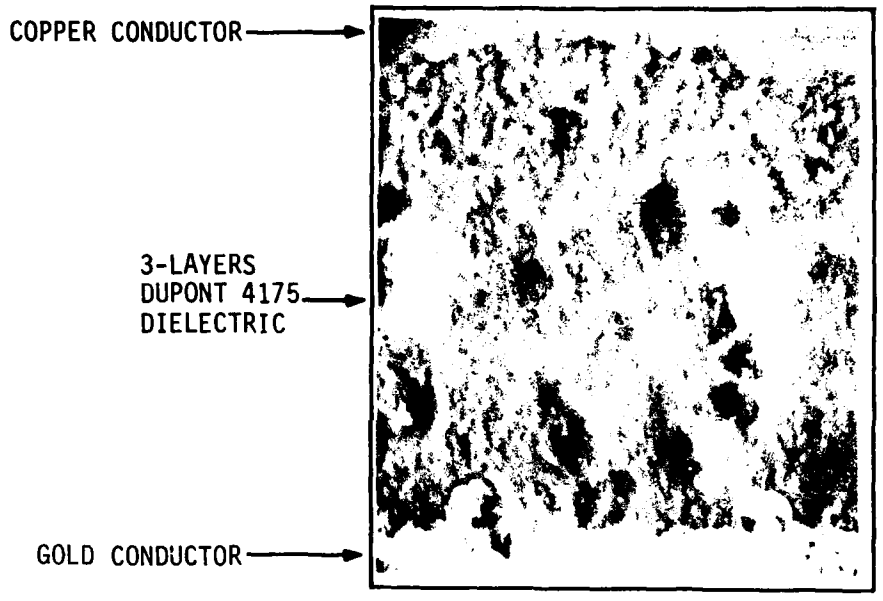



Figure 8. Microstructure of dielectric fired at 900°C in air.
(Magnification 1000X)

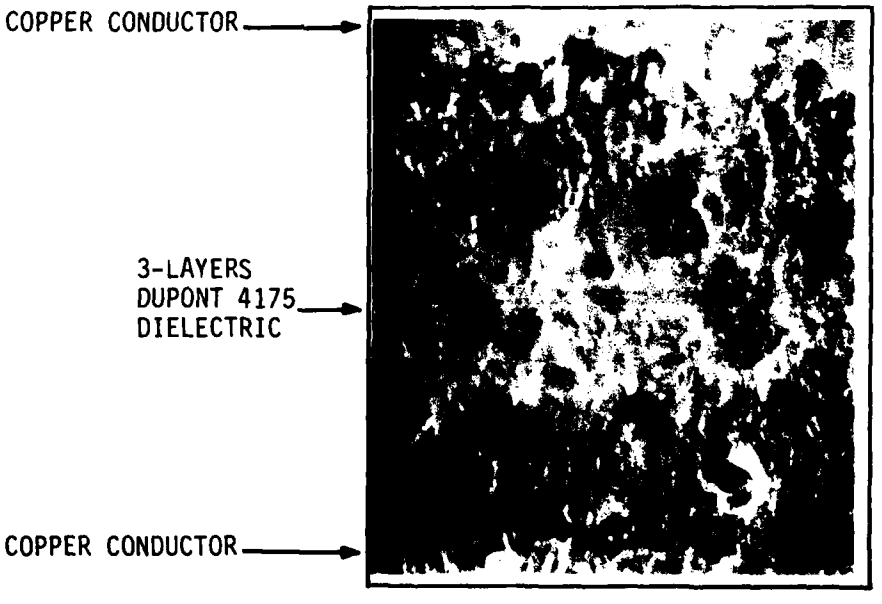



Figure 9. Microstructure of dielectric at 900°C in Nitrogen atmosphere.
(Magnification 1000X)

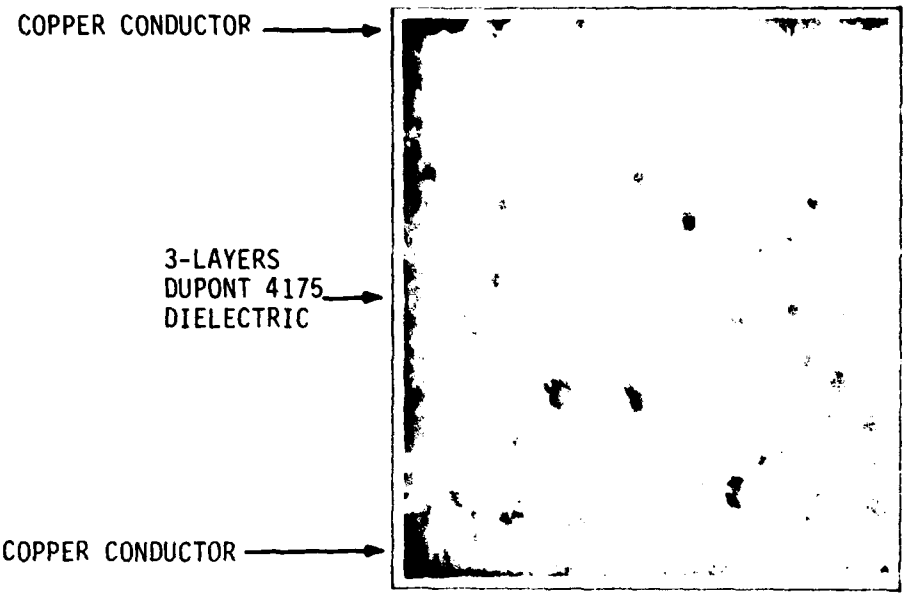



Figure 10. Microstructure of dielectric dried at 300°C using IR furnace prior to being fired at 900°C in nitrogen. (Magnification 1000X)

## CONCLUSIONS

Significant progress has been made in understanding material interactions and processing relationships and has led to the development of compatible copper microcircuits. Specific material and processing steps had to be defined to provide optimum behavior of the conductor and dielectric. This understanding was obtained through a systematic study of both commercial and in-house materials and led to the definition of a processing window. Performance of copper based microcircuits shows that they can be used as a direct replacement for precious metal systems at a substantial savings in cost. Thus, these systems are being introduced into commercial products using vendor materials.

Perhaps the most critical aspect of these systems is the dielectric and its sensitivity to moisture. Protection of multilayer systems from high humidity atmospheres is required for long term reliability. Additional work is underway to measure the extent and type of protection required for application in military systems. This includes both improvements in dielectric density as well as evaluations of protective coatings and hermetic packaging approaches.

A compatible resistor system is required for the full application of copper thick film systems. Resistor development is underway and commercial

resistor pastes are available. Future work will continue with the development of these materials.

## ACKNOWLEDGEMENTS

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3. D. E. Pitkanen, J. P. Cummings and J. A. Sartell,"Material Compatibility and Processing Relationships for Copper Thick Film Hybrids", The International Journal for Hybrid Microelectronics (in press).

4. R. Johnson and D. Kinser, "Examination of the Relationship Between Structure, Adhesion and Conductivity in Copper Thick Film Systems", Proceedings of the 1978 International Microelectronics Symposium, pp. 73-78.

5. J. D. Mitchell, P. C. Donohue, F. K. Patterson, "Processing Techniques for Fabricating Thick Film Copper/Dielectric Multilayer Structures", 1979 Electronics Components Conference.

6. J. Page and D. Webster, "Transitioning from Gold to Copper in a Multilayer System", 1980 Electronics Components Conference.

# HYBRID SUBSTRATES BY COMPUTERIZED WRITING SYSTEM

By

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## ABSTRACT

Since the inception of thick film hybrid technology, substrate circuit patterns have been applied using variations of the art of silk screening. Various other methods of thick film pattern applications have been tried, however, screening has remained the primary method by which thick film pastes are applied to the substrates. ITT Gilfillan has perfected equipment (developed by ITT's Standard Telecommunication Laboratories, Harlow, England) which is an exciting new addition to thick film technology. Referred to as the *Thick Film Writing System* the equipment is not expected to replace screening as a production method of substrate fabrication, but to become a cost saving device for prototype fabrication and development. In addition, it has proven to be economical for production quantities of up to one hundred substrates.

## *INTRODUCTION*

Basically, the *Thick Film Writing System* is a computer-controlled device which applies off-the-shelf thick film pastes through a pen or stylus to a substrate in a programmed pattern. Figure 1 shows the complete system as it is installed in the Microelectronics Laboratory at ITT Gilfillan (ITTG). The block diagram, Figure 2, illustrates interconnections and signal flow between components in the system. As depicted, the system consists of the following components:

1) STL* Writing Head
2) STL* Writing Head Controller
3) Summit 8118 Numerical Controller and Keyboard
4) Summit X-Y Table (6" x 6")
5) Tektronix 4051 Desk Top Graphics Computer
6) Tektronix 4907 File Manager (Disc Drive)
7) Tektronix 4662 Interactive Plotter
8) Line Printer

*Standard Telecommunications Laboratory.

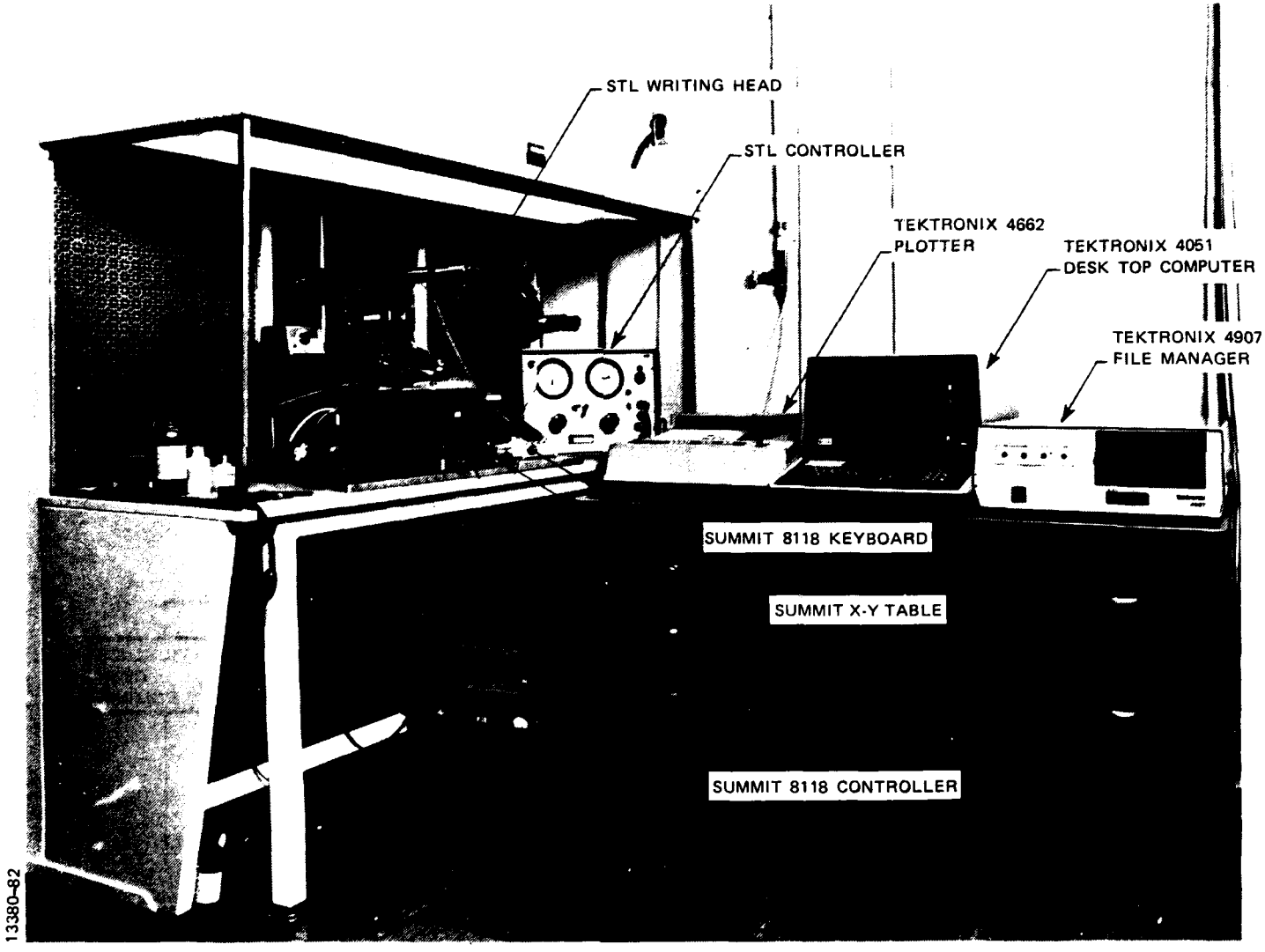


*Figure 1. The Thick Film Writing System*

AD-A091 520 ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND FO--ETC F/G 9/3
PROCEEDINGS OF THE 1980 ERADCOM HYBRID MICROCIRCUIT SYMPOSIUM, --ETC(U)
JUN 80 O P LAYDEN, I H PRATT

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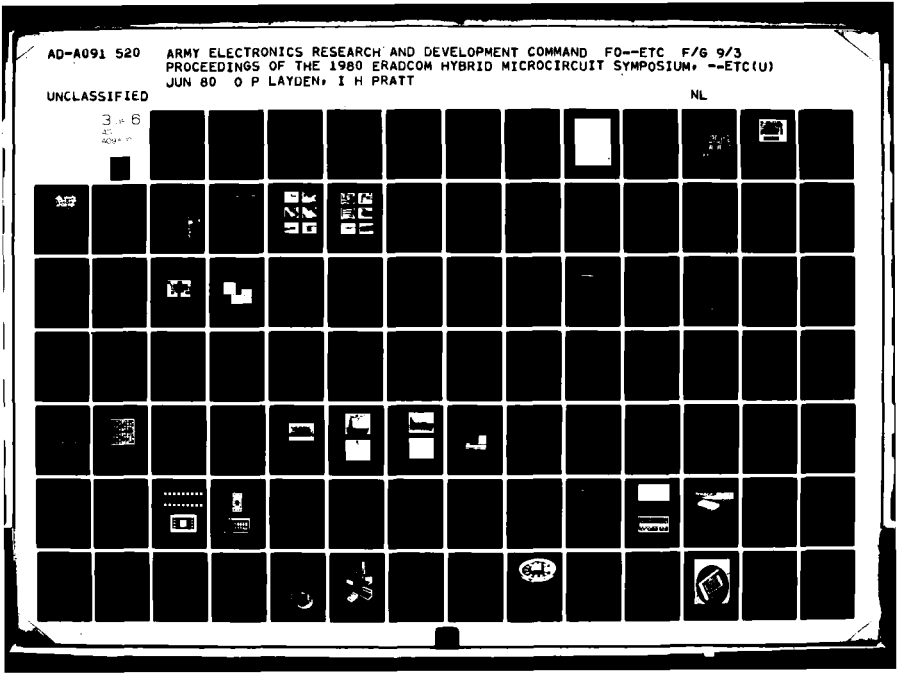

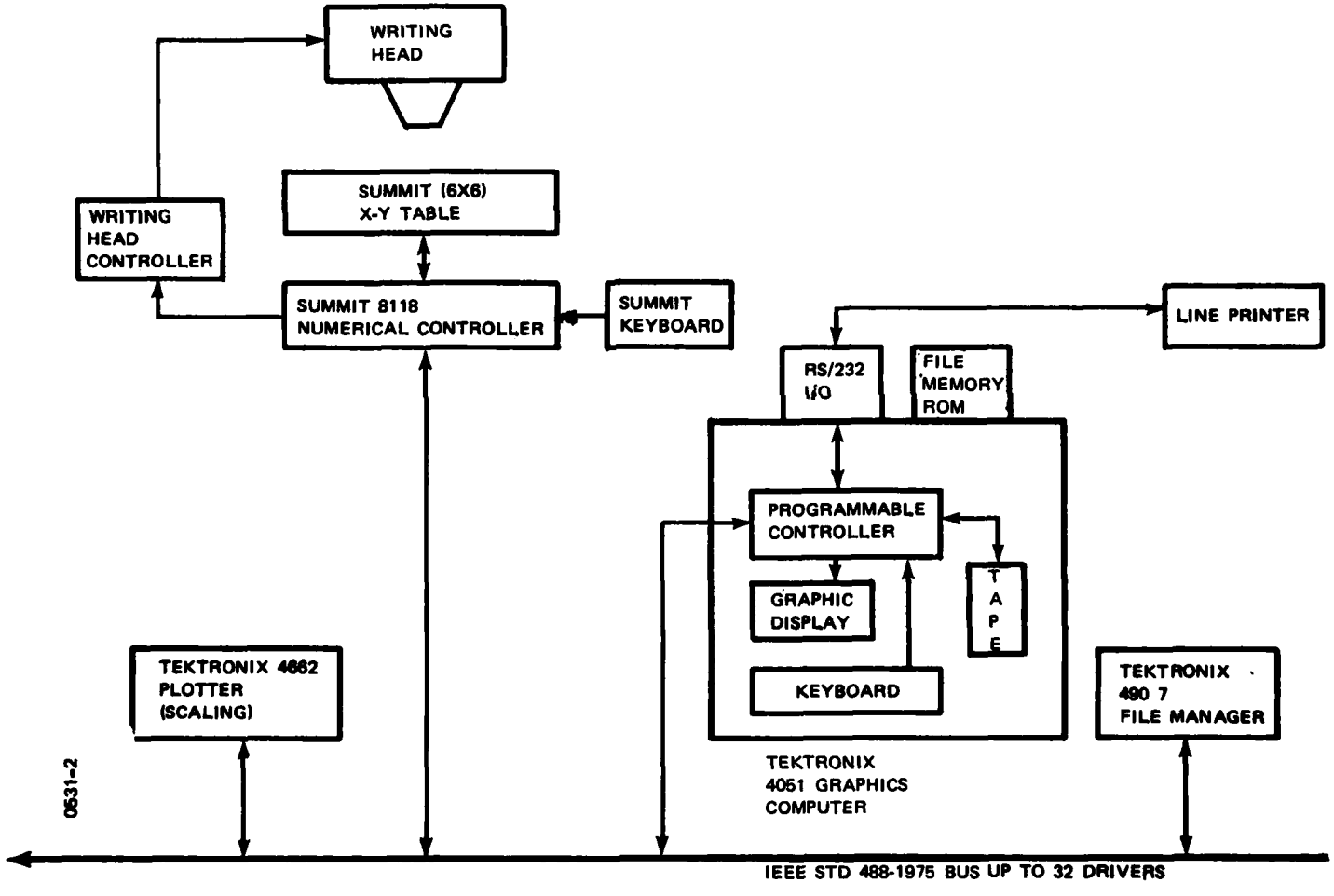


*Figure 2. Block diagram of the computerized thick writing system*

Systems operation is controlled by a software program entered into the Tektronix 4051 processor. The program's modes and/or submodes are as listed:

1) Create (enter required data to fabricate a specified hybrid substrate).
   a) Block
   b) Line
   c) Alphanumeric.
2) Modify (change, delete or add data).
   a) Modify (change, size, shape, stylus direction and location).
   b) Delete
   c) Add.
3) Execute (instructs plotter to make drawings or the writing machine to make substrates).
   a) Plotter (scaled drawings)
   b) Writing System (substrate Fab. 1 to 1).

All data is retained on a separate tape and/or disk and entered on the tape and/or disk as instructed by the system's software.

## DESIGN

During the initial evaluation phase of the Thick Film Writing System a ground rule was adopted such that substrate designs could be fabricated using either the screening process or the writing machine. However, certain basic design rules established for screening were eliminated in order to utilize the capabilities of the writing machine. These design rules are as follows:

1) Use of more than three different resistor pastes.
2) Use of one thickness of dielectric glass paste.
3) Extended length for narrow lines and narrow spaces (less than 5 mils).
4) Experimentally use aspect ratio for rectangular resistors greater than 10 to 1.

In order to properly digitize the layout for data entry into the computer, it is required to divide the substrate pattern into a series of blocks and lines and to properly sequence the data entries. Sequence of blocks and lines is controlled by stylus design and method of paste deposition.

The thick film paste is deposited through the orifice of a pen or stylus. Figure 3 is a drawing of a typical pen as presently constructed. When installed in the writing machine, the diamond-tipped stylus will always be in Quadrant 1 of an X-Y plot, considering that the X-Y axes are perpendicular center lines of the pen orifice as illustrated in Figure 4. The

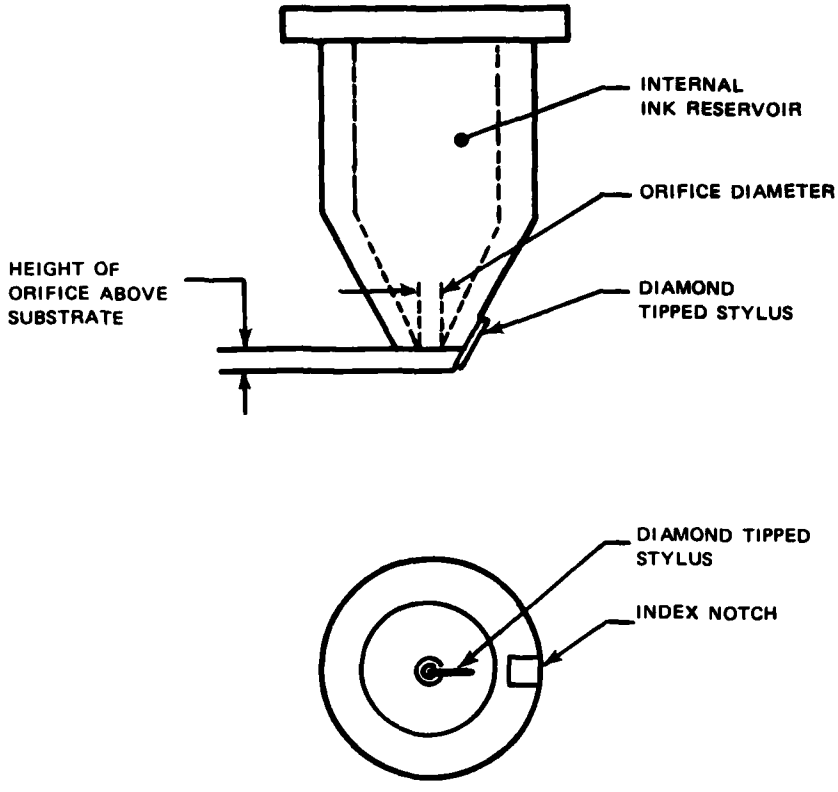


*Figure 3. Writing pen of the thick film writing system*

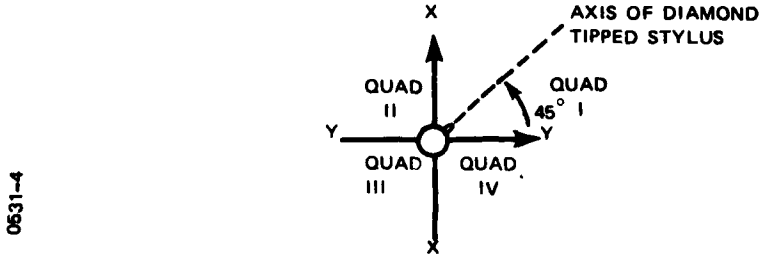


*Figure 4. Location of diamond-tipped stylus in relation to x-y axis*

location of the diamond-tipped stylus is important in determining sequence of blocks and lines which make up the substrate pattern. Also to be considered is the basic line width to be used. Experience has shown that maximum useable line width is 15 mils, however, for maximum efficiency, 5 mils has been adopted as the standard line width. By laying down adjoining 5 mil lines on 5 mil centers, areas of any width and length may be processed. Figure 5 illustrates the technique used to obtain widths greater than 5 mils. 15-mil wide lines are generally used when larger areas such as ground planes are required.

Once the layout is complete, conductor paths are divided into blocks and/or lines for digitizing. After blocking is completed, the blocks and/or lines are numbered to indicate sequence for data entry. Blocks are entered into the computer in the sequence required during processing. Figure 6 is a typical blocking diagram. Separate blocking diagrams are made for conductor paths, dielectric glass, crossovers, each resistor value and resistor encapsulant. Once the blocks and/or lines have been sequenced, the X-Y coordinated data are entered into the form shown in Figure 7. Two sets of X-Y coordinates are required for each entry and, in the case of blocks, a vertical or horizontal instruction must be given.

## COMPUTER PROGRAM

This section is not a description of the software, but rather a discussion of how the software is used. Once the X-Y coordinates are listed, they are entered into the computer. The procedure is started by placing the system program into the computer's memory. The Create mode is initiated and the graphic display will instruct the operator to place the data disk or tape into the equipment. This tape or disk has been formatted to accept three or five hybrids, each hybrid having 10 or 15 layers. (It should be noted that the word, "layer", is not used in the exact sense of a screened layer. The word, "layer", here is considered a section of the tape or disk mark to except a specified number of bytes of information. Conductors and solder patterns for a complex hybrid will normally require two or more tape layers each as compared to a single screen layer.) After placing the data disk or tape into the equipment, the hybrid menu will appear. At this point, the following questions appear on the graphic display.

Next available hybrid?
Name of hybrid?
Width in mils?
Length in mils?
Pitch?

When this set of questions is answered, the layer menu title will appear on the graphic display and will ask:

Next layer available?
Layer name?

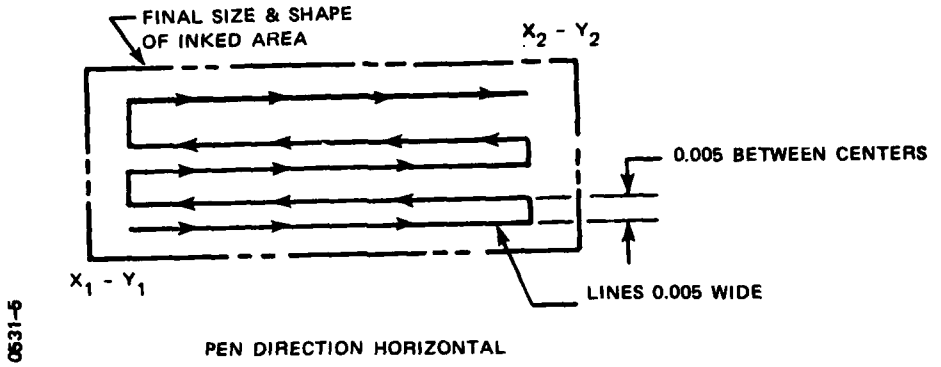


*Figure 5. Serpentine lines used to fabricate wide lines*

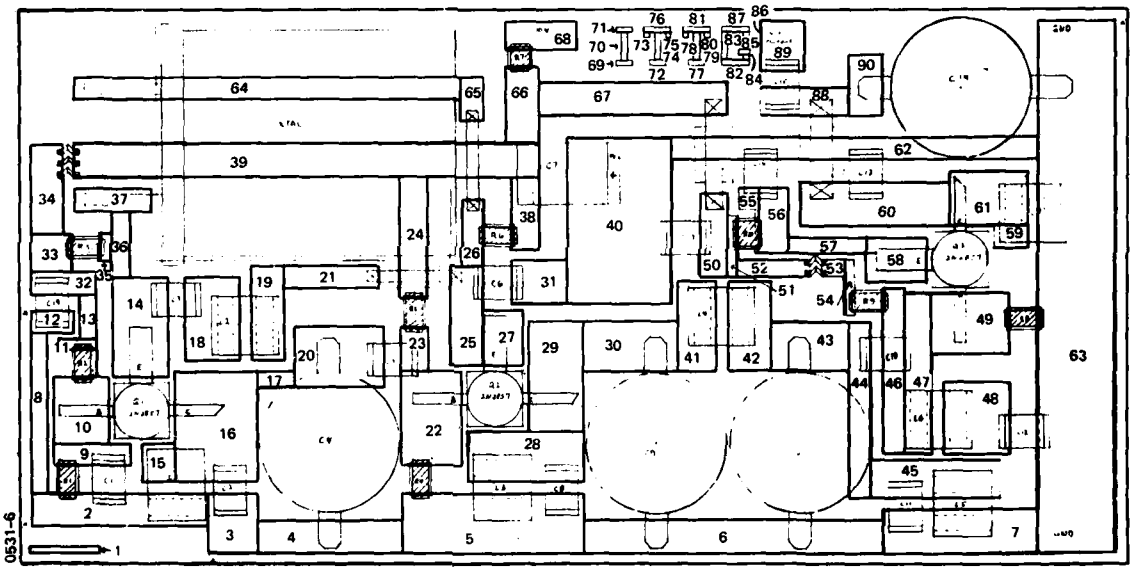


*Figure 6. Blocking digram of conductors*

**HYBRID COORDINATES** P/N MS 1005

TITLE REF Divider No. 2 PREPARED BY M. Shankin DATE 5-22-78

DATA FILE NO. 5 CHECKED BY M. Shankin DATE 5-30-78

HYBRID NO. 1 ENTERED BY M. Shankin DATE 5-30-78

LAYER NO. & NAME 1 Conductor No. 1

PAGE ____ OF ____

| GROUP NO. | BLOCK NO. | DATA | | | | |
|---|---|---|---|---|---|---|
| | | $X_1$ | $Y_1$ | $X_2$ | $Y_2$ | V OR H |
| 1 | 1 | 100 | 1600 | 600 | 1630 | H |
| | 2 | 100 | 1630 | 130 | 1740 | V |
| | 3 | 140 | 1660 | 500 | 1670 | H |
| | 4 | 130 | 1700 | 200 | 1740 | H |
| | 5 | 500 | 1660 | 510 | 1720 | V |
| | 6 | 500 | 1720 | 540 | 1740 | H |
| 2 | 7 | 700 | 1600 | 750 | 1630 | H |
| | 8 | 700 | 1720 | 750 | 1750 | H |
| | 9 | 800 | 1600 | 850 | 1630 | H |
| | 10 | 800 | 1720 | 850 | 1750 | H |
| | 11 | 900 | 1700 | 950 | 1730 | H |
| | 12 | 900 | 1920 | 950 | 9150 | H |
| 3 | 13 | 1000 | 1700 | 1050 | 1730 | H |
| | 14 | 1000 | 1920 | 1050 | 1950 | H |
| | 15 | 10 | 10 | 220 | 185 | H |
| | 16 | 10 | 185 | 245 | 205 | H |
| | 17 | 10 | 205 | 85 | 275 | H |
| | 18 | 95 | 235 | 325 | 265 | H |
| 4 | 19 | 325 | 235 | 420 | 285 | H |
| | 20 | 10 | 275 | 265 | 295 | H |
| | 21 | 125 | 330 | 205 | 360 | H |
| | 22 | 205 | 330 | 290 | 355 | H |
| | 23 | 290 | 315 | 340 | 355 | H |
| | 24 | 10 | 485 | 85 | 575 | V |

REMARKS: Blocks 1 thru 14 Test Blocks

0531-7

*Figure 7. Digitizing form*

At this point, an outline of the substrate will appear on the graphic display with the layer name. The operator will then press the user defined keys asking for block or line. The graphic display will now change showing the substrate outline, the layer name, and will request data entry by asking for:

$X_1$ = ?
$Y_1$ = ?
$X_2$ = ?
$Y_2$ = ?
V or H = ?

Figure 8 shows the graphic display with all entries.

As the data is entered, each block is drawn on the graphic display with sequence number. After entering six sets of coordinates, it is necessary to press the block key to clear for the next set of numbers. The process is repeated until such time as the matrix is filled (used all formatted space) or all required coordinates are entered. The operator then presses the user defined key marked "Layer Complete". This stores the matrix on the data tape or the disk for future use. The computer will then ask if you wish to check entered data. If answer is "Yes" matrix data will appear on screen, if "No" layer menu will appear. This process is then repeated until all required coordinated data for all layers are entered into the computer and stored. When all layers are completed, operator will push user definable key to call up next operation.

If changes are required, the "Modify" key of the user definable keys is pushed. The question asked is then:

Is this a current layer to be modified Y or N?

If the answer is "No", the operator will be asked to place system tape or disk into the system and press Return. This will enter the "Modify" mode program into the computer's memory. The data disk or tape then replaces the system tape or disk and the operator is asked which hybrid and which layer is to be modified. When information is entered through the keyboard, the following is asked:

1) Add?
2) Delete?
3) Modify?
4) Layer complete?

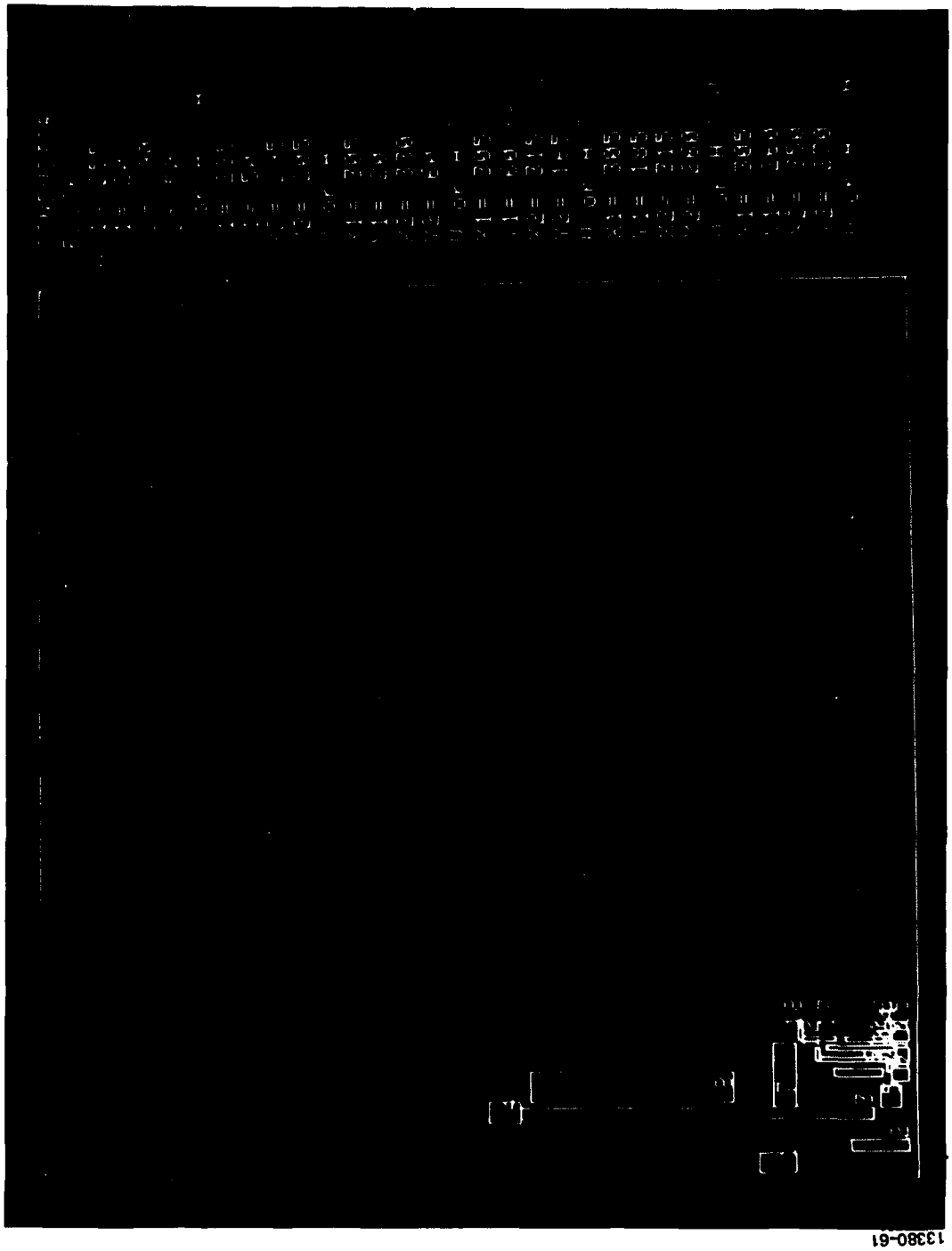


*Figure 8. Graphic display during create mode*

When the appropriate number is entered, the next question asked is:

1) Block?
2) Line?

When answered, the operator will be asked the Block or Line sequence number. If the Delete operation is asked for, the statement "I am deleting" will appear on the graphic display after sequence number is entered. If Add or Modify is requested, the new X-Y coordinate set will be asked for. Upon completion of the layer modification, Layer Complete No. 4 is entered into the computer and the information on the storage device is corrected.

The Plot mode, when placed in the computer memory, will, on command, instruct the plotter to draw the substrate pattern to the desired scale and size within the plotter's capabilities. Figure 9 is a typical substrate plot to check accuracy of inputted data. The plot is usually done in multicolor so as to define each layer. The plot mode can also be used to make final drawings if so desired. With the addition of a "Library of Components", it would be possible to prepare acceptable assembly drawings of the hybrid. The plot mode permits making drawings in outline or serpentine fashion.

The ink mode is the mode used to fabricate the actual substrate. In this mode, the computer instructs the numerical controller as to all actions needed to place pattern on the substrate. Under computer instructions, the X-Y table will be moved until the proper point to start inking is under the stylus. The stylus is dropped and ink starts flowing until specified block is completed. The X-Y table is then instructed to move to the next start position and process is repeated until the layer is completed. Process is then repeated for each layer until substrate pattern is completed. Figure 10 is a typical substrate before components are added.

## CAD COMPATIBILITY

By definition, CAD is being referred to here as the ability to design the hybrid substrate on the computer thereby eliminating the need for board work or for digitizing the completed layout. There has been some argument suggesting that the system, as now constituted, is a form of CAD-CAM and in a sense this is true, but it is not a system that makes the maximum use of CAD capabilities. Of the five writing systems now in use, it is not known if any are used in conjunction with one of the complete CAD systems available; however, studies have shown that with the proper software, the Thick Film Writing System can be controlled by any of the commercially available CAD systems. In fact, it has been determined that the present software system being used could be expanded or used as is if additional software were developed for an in-house CAD system with full design capabilities. There are basically two problems which prohibit this development. Time and money.

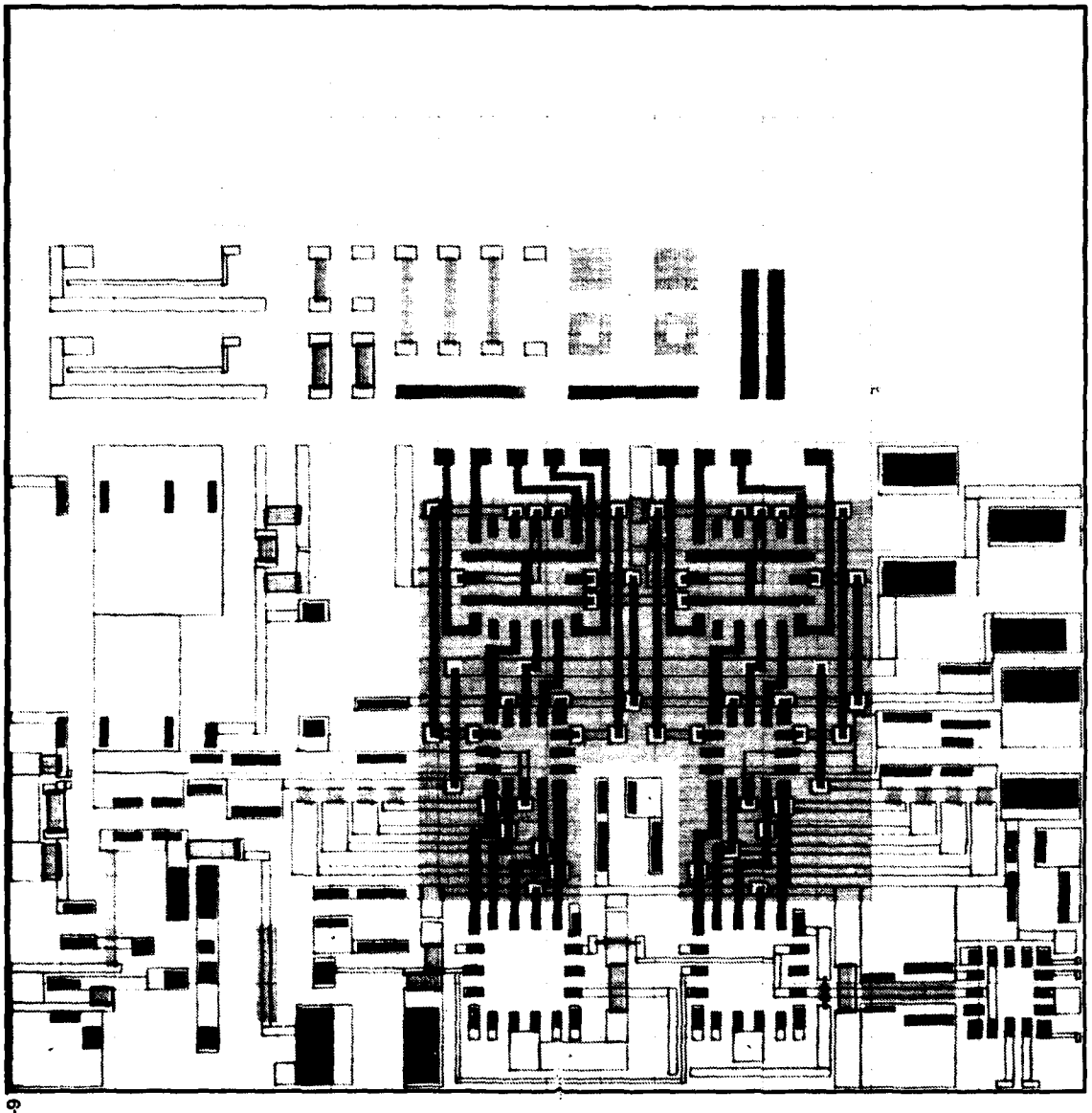

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*Figure 9. Plotter-produced check drawing*

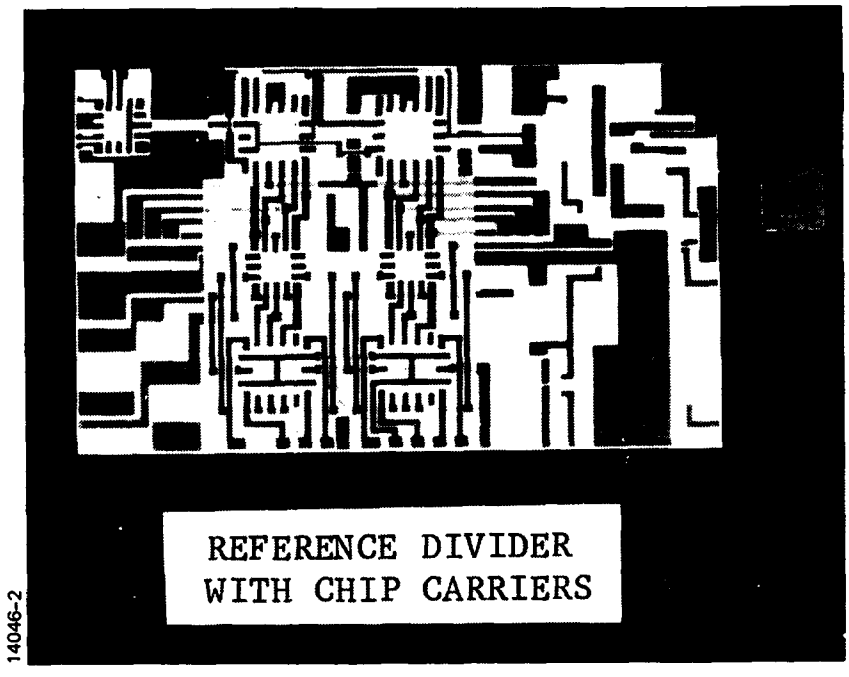


*Figure 10. Substrate*

## ECONOMICS

The beneficial use of any equipment is determined by both its performance capabilities and economic return. It has been established that technically the Thick Film Writing System is a very good tool; its operation is efficient and the resultant product is good. The big question is, and has been, the economics involved. Work to date has proven that for prototype substrates and for small production lots of under 100 substrates of a single type, the cost in labor and time is equal to or less than that for screened substrates.

Table I indicates the estimated dollar savings for prototype generation. As seen from this table, dollar savings can be considerable depending on the amount of prototypes that are made in one year. There is, however, a time saving which can be significantly valuable even though there is no actual labor saving. For example, the prototype of the hybrid integrated circuit, shown in Figure 11, was delivered for test in approximately 60 working hours after completion of the hybrid's layout. (Note: nine screens would have been required if screen techniques had been used.) If the same unit had been screened, it would have taken from six to eight weeks to prepare the tooling, considering time to cut artwork, make photo productions, negatives and screens.

*Table I. Prototype Savings Computerized Writing System* [7]

| | | | |
|---|---|---|---|
| Elimination of Artwork Generation and Inspection | 3 hr/print X $28/hr | = | $ 84.00 |
| Elimination of Photolithographic Preparation and Inspection of Stencil Screens | 2 hr/print X $28/hr | = | $ 56.00 |
| Production, Tooling Eliminated | $100/print | = | $ 100.00 |
| Equipment Preparation Reduction in Time | 1.5 hr/print X $28/hr | = | $ 42.00 |
| Material Savings | 10 gm/print X $16/gm | = | $ 160.00 |
| | PER PRINT SAVINGS | = | $ 442.00 |
| Linear Hybrid Circuit | | | |
| 1 Conductor, 3 Resistor Prints | Savings 4 X $442.00 | = | $ 7,768.00 |
| Digital Hybrid Circuit (Multilayer) | | | |
| 3 Conductor, 5 Dielectric Prints | Savings 8 X $442.00 | = | $ 3,536.00 |
| Program/Company Savings | 15 X $1,768.00 | = | $26,520.00 |
| 15 Linear Circuits | 15 X $1,768.00 | = | $26,520.00 |
| 4 Digital Circuits | 4 X 3536 | = | $14,144.00 |
| | TOTAL SAVINGS | = | $40,664.00 |

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In addition to quick turn-around for prototypes, changes to prototypes are quickly accommodated. As earlier explained, changes are relatively simple to make and, depending on complexity of changes and of the hybrid itself, a new prototype can be made available within eight to twenty-four hours.

Without discussing actual costs, but discussing an actual bid for a hybrid integrated circuit being built for the military, we can compare the cost of screening versus the writing machine fab costs. The hybrid being discussed is fabricated on a two-inch square substrate,

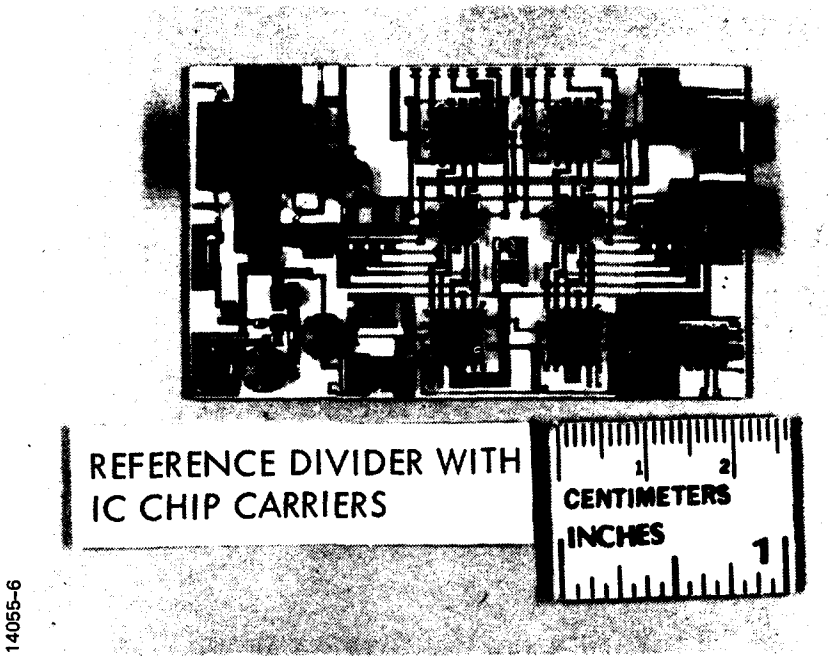



*Figure 11. Assembled hybrid*

has 46 film resistors and 32 add-on components. The purchaser was to supply all material so that the calculations were based on recurring costs only. For very small quantities, the screened device is 843 percent more expensive than the written device. For moderately small quantities or about 25 hybrids, the screened device is 123 percent more expensive than the written device. However, at quantities of 100, the screened device is 6.35 percent less expensive than the written device. The written device cost has been calculated using a single pen and a writing speed of 24 inches per minute. It is possible, with further development, to increase the table speed so that cost crossover point is at 1,000 devices rather than the 100 devices discussed above.

It can be seen that at the present speed of operation, the Thick Film Writing System is a viable tool for fabrication of small quantities of hybrid substrates and a great tool for generation of hybrid prototypes.

## USES OTHER THAN HYBRID SUBSTRATE FABRICATION

There are some further uses for the writing machine other than applying thick film ink patterns to a ceramic substrate. The equipment can be used to apply a photoresist pattern to a copper clad board for printed circuit card development. Photoresist can be applied to mylar to make a photo-positive from which a negative can be made. This negative can then be used for screen fabrication.

## COMPARISON OF SCREENED HYBRIDS TO WRITTEN HYBRIDS

First, comparison will be made between written conductors and screened conductors. Figure 12 shows profilometer traces of both screened conductors[1] and written conductors.[2] Figures 12(a) and 12(b) may be compared as they are both wide conductors. It can be seen that although different scales were used, the average thickness of both traces are similar, however, the noticeable difference is in the flatness of the written conductor. This flatness has helped improve wire bonding. Figures 12(c) and 12(d) are cross sections of narrower conductors. Here we find the written conductor somewhat thinner with a smoother surface. This difference in surface smoothness appears to be due to the fact that when the screen snaps back, the ink on the screen tends to tear away from the ink on the substrate. The written conductor has no such problem as it is applied to the substrate through the stylus much as toothpaste is squeezed from a tube. Figure 15A illustrates the fine edge definition achieved with written conductors. There is little or no feathering and absolutely no scalloping that can occur along the conductor edge as occurs with screened conductors or resistors.

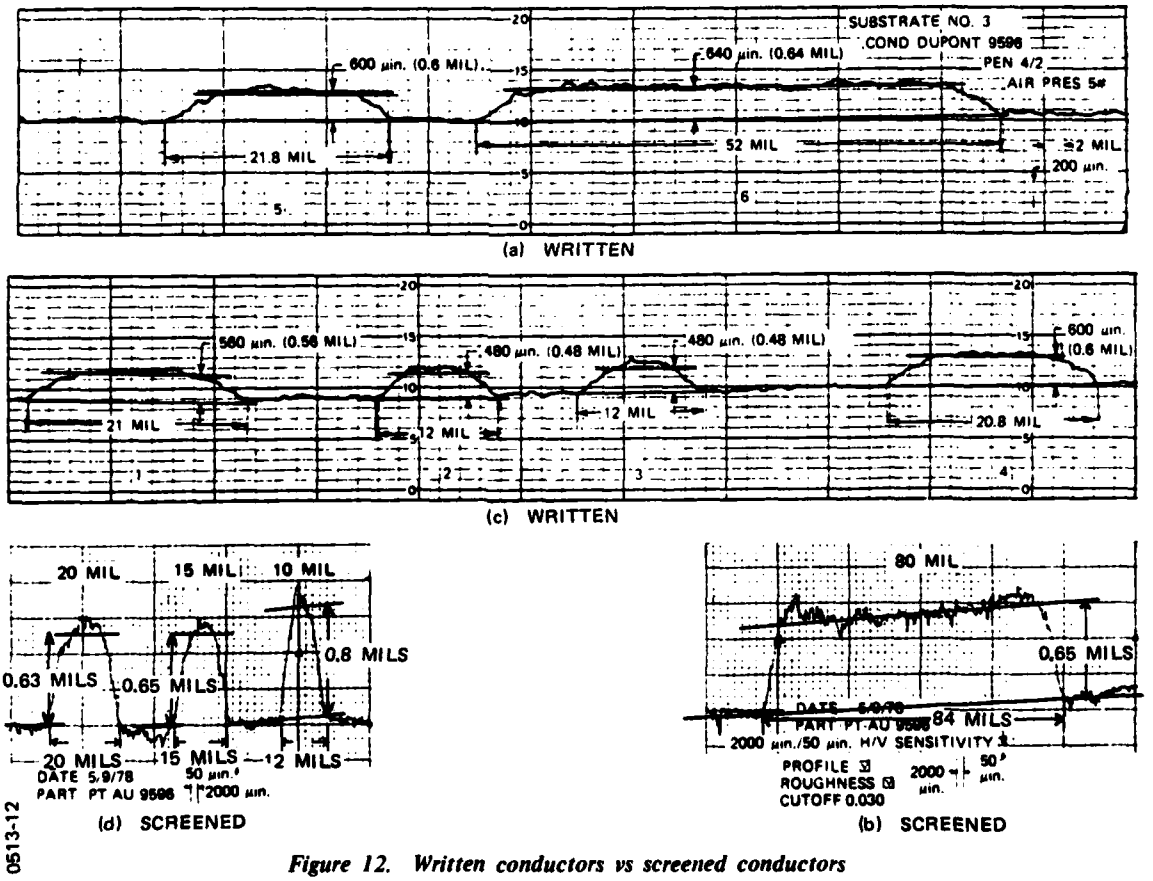



*Figure 12. Written conductors vs screened conductors*

Figure 13[3] shows both profilometer tracers and scanning electron microscope (SEM) photographs of the same areas. It should be noted that the written glass dielectric uses one application of ink as opposed to the double screening of glass normally required and/or used. It can be easily seen from the trace and the photo that written glass is considerably smoother and thinner than the screened glass. Figure 15A also illustrates the smoothness and coverage obtained with a single application of glass by pen. Figure 15B is a SEM photo of screen-applied glass and illustrates the corrugated effect sometimes obtained with screen dielectric glass.

Figure 14 shows the longitudinal traces of both a written resistor[4] and a screened resistor.[5] Figure 14A is the written resistor and illustrates the smooth interface of the resistor and conductor paste. Figure 14B is the screened resistor and shows an uneven peak interface. Unlike the written resistor, which has equal interfaces at each end, the screened resistor is unequal at each end. Figure 15C illustrates the clean square corner of resistor interface, while Figure 15D shows the rounded interface sometimes obtained with screened resistors. Figure 15E is a cross section of a written resistor and illustrates the smooth, even melding of the conductor and resistor pastes at the interface. Figure 15F shows scalloping or sawtoothing of edge definition found on screened resistors and conductors.

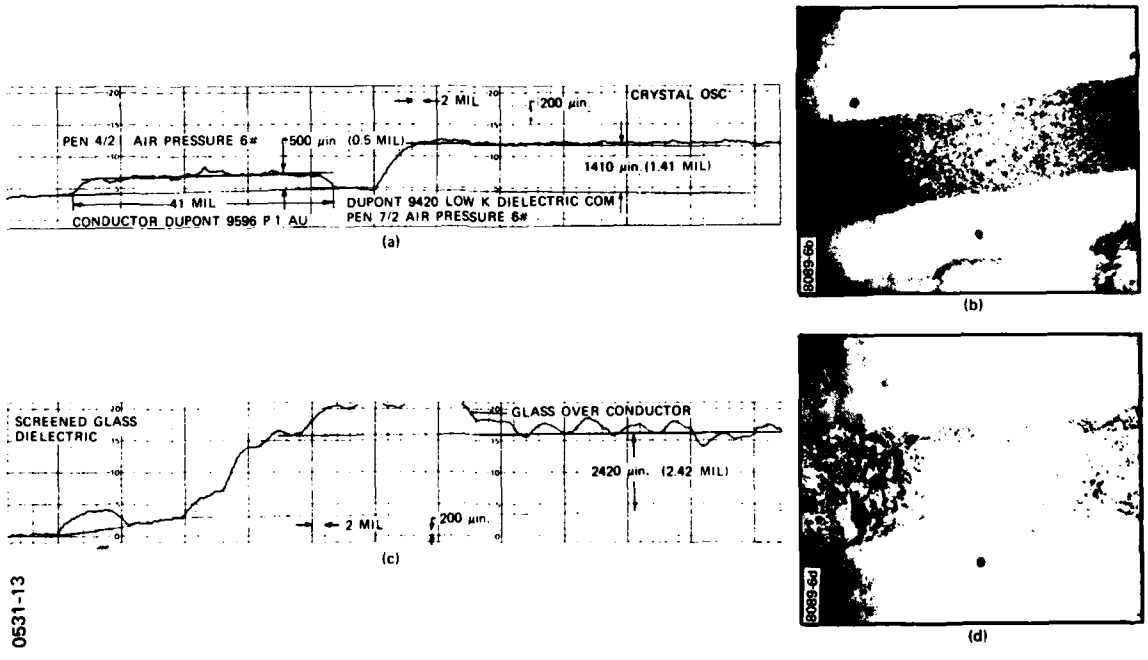
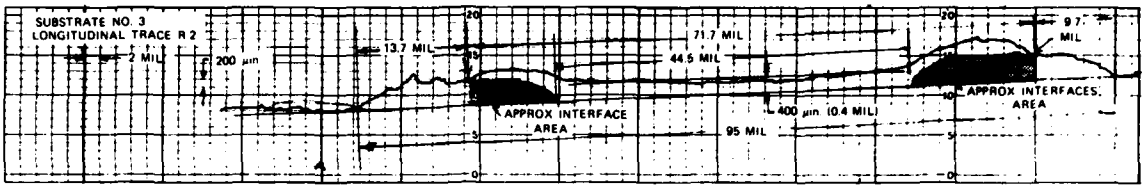
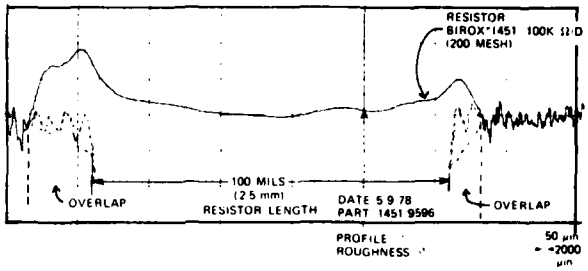



*Figure 13. Written glass vs screened glass*

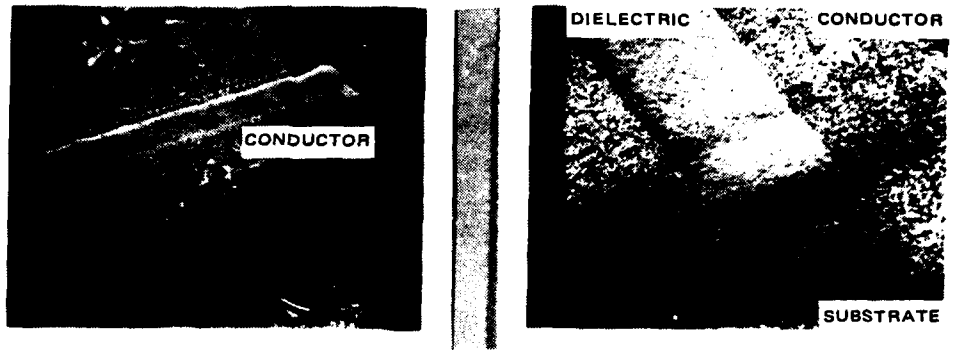



(a) WRITTEN

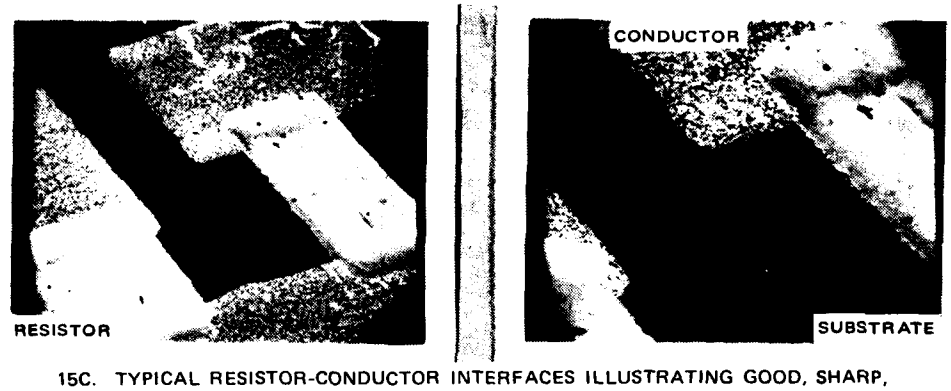



(b) SCREENED

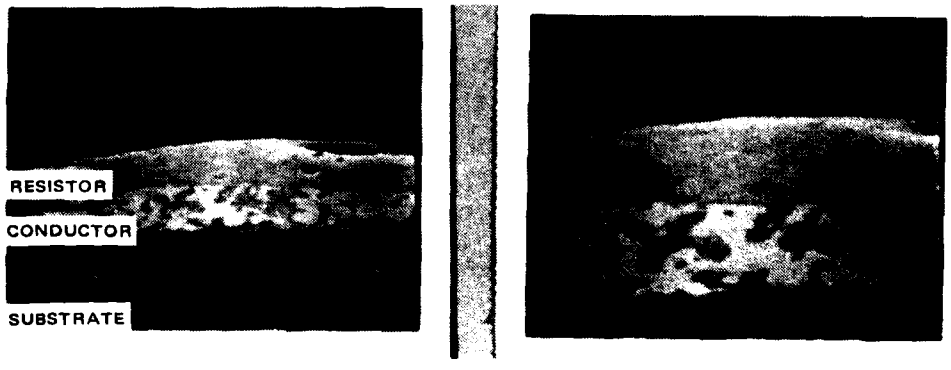
*Figure 14. Written resistor vs screened resistor (longitudinal track)*




15A. TYPICAL CROSSOVER CONFIGURATION DISPLAYING SHARP EDGE DEFINITION AND SMOOTH SURFACES FOR CONDUCTORS AND DIELECTRICS




15C. TYPICAL RESISTOR-CONDUCTOR INTERFACES ILLUSTRATING GOOD, SHARP, SQUARE OVERLAPS




15E. CROSS-SECTION OF RESISTOR-CONDUCTOR-SUBSTRATE INTERFACE

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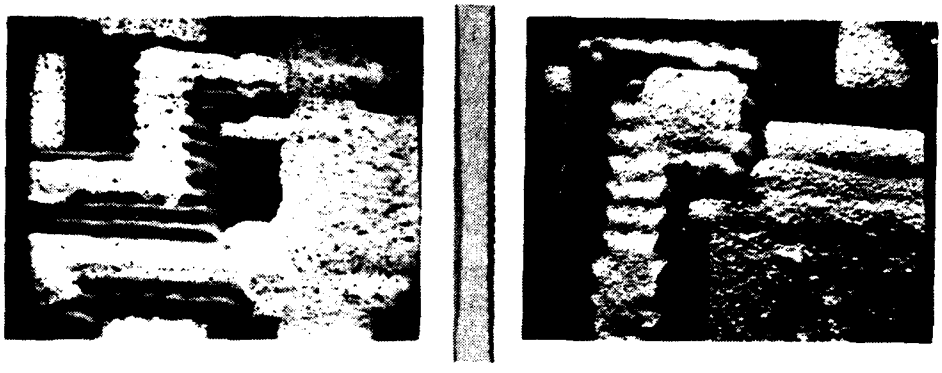
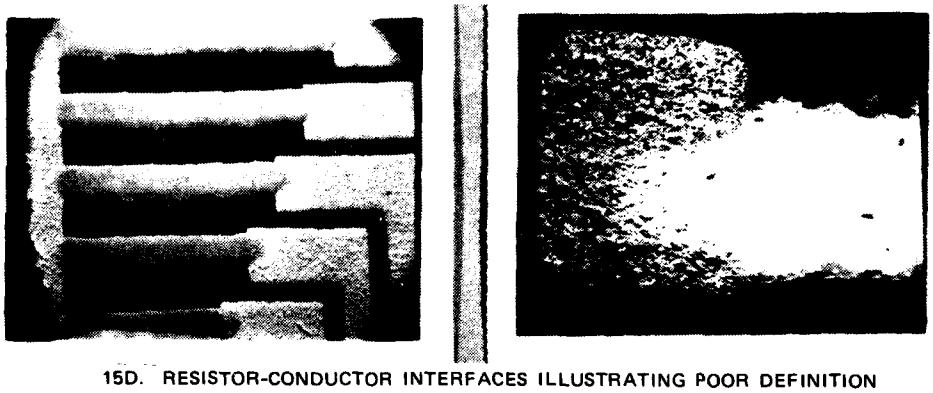
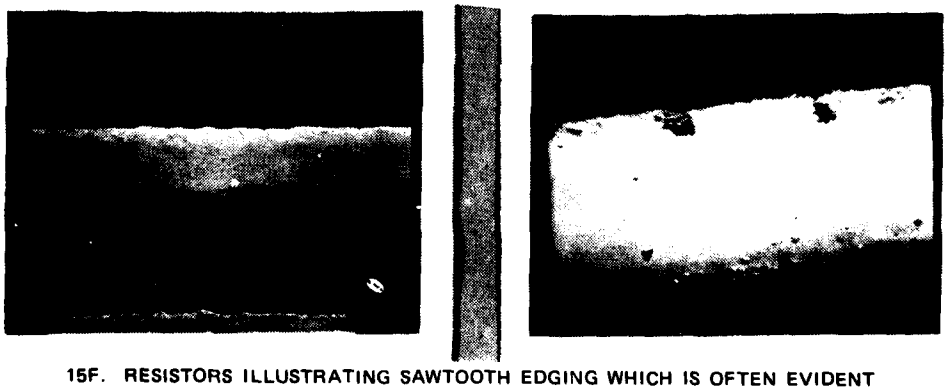
*Figure 15. SEM micrographs of thick film substrates demonstrating topographical characteristics of circuits applied by two different methods.*



15B. TYPICAL CROSSOVER CONFIGURATIONS DISPLAYING CORRUGATED SURFACE AND POOR EDGE DEFINITION



15D. RESISTOR-CONDUCTOR INTERFACES ILLUSTRATING POOR DEFINITION BETWEEN CONDUCTORS AND RESISTORS



15F. RESISTORS ILLUSTRATING SAWTOOTH EDGING WHICH IS OFTEN EVIDENT IN A SCREENED DEVICE

0531-15 (2 of 2)

*Figure 15. SEM micrographs of thick film substrates demonstrating topographical characteristics of circuits applied by two different method. (continued)*

## CONCLUSION

The technical advantages and economic savings involved in the use of the Thick Film Writing System are such that this equipment will make an impact on the hybrid thick film technology in the near future. There will be two areas which will benefit by using the Thick Film Writing Machine. They are:

1) Small quantity High Rel Military Hybrid Fabrication.
2) Prototype fabrication of both commercial and military hybrids.

An on-going Navy manufacturing technology program in the area of computerized thick film printing will do much to hasten the use of the Thick Film Writing Machine.(6)

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3. Op Cit 1
4. Op Cit 1
5. Op Cit 2
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7. Op Cit 6

# FABRICATION AND APPLICATION OF THIN-FILM TRANSISTORS TO DISPLAYS

BY

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## ABSTRACT

A summary of the approach taken at Aerojet to make a monolithic TFT/EL display is given. The type of TFT used and its performance is described. The rationale for using TFTs as pixel switches is discussed.

## INTRODUCTION

The thin-film transistor (TFT) as we know it today was invented in 1962 by Dr. Weimer at RCA. The TFT is a unique kind of transistor in that it can be made on a low-cost substrate such as glass or polymer. As yet, however, there is no product in production using TFTs due to:

- Successes in MOS/FETs,
- Technical problems in reproducibility, and
- Lack of a critical need.

A critical need exists in direct-view electronic displays. The successes in MOS have further accentuated the lack of low-cost, low-power, lightweight, flat-panel displays that are compatible with the new line of CMOS, microprocessors, memories, switching power supplies, etc. The technical problems with TFTs are not significant for the flat-panel display application. The best approach is to keep the TFT circuits simple and dimensions large.

Flat-panel displays have a unique requirement. This is due to the sneak circuits in a matrix-addressed array of picture elements (pixels) which cause one-third-select voltage to be applied across all the non-addressed pixels. Additionally, some display technologies, namely gas discharge and electroluminescence (EL), require a higher operating voltage than is readily available with MOS. Also, flat-panel displays can benefit from memory storage at each pixel. The memory allows for a 100% duty cycle. Without memory, the duty cycle and brightness is inversely proportional to the number of display array rows. The TFT circuit at each pixel can uniquely do all these things. MOS circuits are limited due to their substrate cost and size and low voltage.

A process is being developed to produce TFTs for EL (Thin-Film Electroluminescent) displays under a U. S. Army contract[1] and Aerojet company funds. Present tooling is being used to perfect the fabrication techniques which

allows for a single glass substrate up to 2½" x 5" in size. It is feasible to mosaic four of these together for larger displays. The emphasis is to establish an EL/TFT display; however, other display media could be addressed with the TFTs. Of particular note is liquid crystallinity, electrochromism and electrophoresis.

The contemplated display device is made up of four separate layers called stacks:

- EL Stack includes all those thin-films needed for an EL display,
- Counter-Electrode Stack includes the pixel electrode and a divider capacitor,
- TFT Stack includes all pixel circuit elements except the counter-electrode stack divider capacitor,
- Addressing Stack includes the row and column lines with intermediate dielectric.

The major TFT design considerations are as follows for a display 50 lines X 100 lines or more:

50 X 100 Line Flat-Panel Display

| TFT Advantages | Application to EL | Application to LC and other Non-Emitters |
|---|---|---|
| Switch at Each Pixel | Not Needed, But Advantageous | Mandatory For Matrix Addressing |
| Memory | Advantage For 100% Duty Cycle | Not Needed. Intrinsic Memory |
| High Voltage | Definite Advantage. H.V. Line Driver Only Option | Not Needed at All |
| Large Area | No Advantage | Advantage Over MOS |
| Low Cost | Must Be Lower Than H.V. Line Drivers | Must Be Lower Than Optional MOS Switch |

## THE TFT STACK

This transistor is more sophisticated than that developed by Dr. Weimer,[2.] due to the use of dual gates as shown in Figure 1. Dual gates lead to sharper turn-off characteristics and a higher β coefficient (geometric factor). The pixel circuit uses two TFTs and a capacitor for display memory as shown in Figure 2. The second transistor allows the display median power to be separate from the addressing logic. Memory allows for a 100% duty cycle as noted.

The entire TFT pixel circuit is fabricated on top of the pixel active area defined by a metal electrode called a counter-electrode as shown in the photograph of Figure 3. The TFT pixel circuit is fabricated in one vacuum pumpdown using five metal masks and ten additive depositions.

Fabrication techniques used are as follows:

- Depositions of materials through chemically-etched Kover (TM) metal masks,
- Ball and race aligned tooling set for mask and substrate registration,
- Magnetic pulldown for mask clamping to substrate,
- Tool and mask carousel for in-chamber interchanges, and
- A three-chimney vapor vacuum deposition chamber.

The TFT is a thin-film polycrystalline semiconductor device. The most popular and successful devices use CdSe as the semiconductor which is N type, enhancement mode.[3.4.5.] Typical properties are as shown in Figure 4.

Electrical characteristics are accurately governed by the following equations:[2.]

TFT THEORY

LINEAR $I_{DS} = \beta(V_{DS}(V_G-V_O) - V_{DS}^2/2)$

$G_M = \beta V_{DS}$

SATURATED $I_{DS} = (\beta/2)(V_G-V_O)^2$

$G_M = \beta(V_G-V_O)$

GEOMETRY TERM $\beta = \mu\varepsilon W/TL$

$\mu$ IS SEMI MOBILITY
$\varepsilon$ IS DIELECTRIC CONSTANT
T IS DIELECTRIC THICKNESS
W IS CHANNEL WIDTH
L IS CHANNEL LENGTH

The $\beta$ coefficient is at the designer's control. To improve the TFT, the following requirements can be satisfied with changes in the $\beta$ coefficient and geometry changes:

- Higher Current ($I_{DS}$) requires Higher Gain ($\beta$)
- Higher Transconductance ($g_m$) requires Higher Gain ($\beta$)
- Lower Off-current requires Dual Gates
- Higher Voltage ($V_{DS}$) requires Thicker Dielectric (t)
- Lower Miller Effect requires Reduced Gate-to-Drain Capacitance (caused by Gate and Drain conductor overlap and channel capacitance and ($\varepsilon WL/t$))
- Lower On Resistance ($R_{DS_{ON}}$) requires Higher Gain ($\beta$)

The TFT is a perfectly symmetrical device if the source-to-gate is identical to the drain-to-gate geometry. This is to say the drain and source can be interchanged. The grounded electrode is the source. $I_{DS}$ is the drain-source current as a function of the source voltage and gate voltage. When the TFT is turned off by making the gate slightly negative (-1 volt), the TFT has the electrical characteristics of a diode. When the TFT is turned on, it has the electrical properties of a resistor at approximately one to two K ohms.

## COUNTER-ELECTRODE STACK

The counter-electrode stack contains a capacitor used in series with the EL capacitance for voltage division. The EL requires approximately 300 volts peak-to-peak. It is desirable to address the display with CMOS which is limited to approximately 15 volts peak-to-peak. The TFTs can be made to drive a load above 300 volts but not with sufficient gain for only a 15 volt input signal. One solution for EL display drive is to add a capacitor as shown in Figure 2 and use a capacitor divider circuit. This capacitor is built at each pixel in the counter-electrode stack. The second TFT shorts out the divider capacitor to turn on the pixel. When the divider capacitor is shorted out, the full voltage is applied across the EL thin-film which is electrically equivalent to a capacitor to a first approximation.

## ELECTROLUMINESCENT (EL) STACK

The EL stack is first built on the substrate. The material is ZnS with Mn as the primary activator. The stack is optimized for steep brightness-to-applied voltage performance which has been achieved as shown in Figure 5. High brightness is not important since the duty cycle is 100%. Brightness control is easily achieved with power frequency control. For frequencies below 5KHz the brightness is proportional to frequency.

A display with the EL performance shown in Figure 5 is easily made sunlight readable. Since thin-film ZnS is transparent, the use of a black light-absorbing back layer or a reflecting back layer with front circular polarizer is applicable to achieve sunlight readability.

## ADDRESSING STACK

The addressing stack contains the row and column lines and accommodates the crossovers.

## DISPLAY

The complete display is schematically shown in Figure 6. The process profile for fabricating the display is outlined in Figure 7. Two basic approaches being considered for connecting the TFTs to the EL are monolithic[5]. and sandwich[6]. as summarized in Figure 8. The yield would be improved with the sandwich configuration. The monolithic approach is the most rugged and simplest to make.

The EL is the most efficient light-emitting display except for the cathodoluminescent techniques. The EL panel has a high imaginary power component which cannot be saved when it is supplied along with the display logic. In the approach here the logic and display power are supplied from different sources. Therefore, a resonant circuit can be used to save the imaginary power component.

## SUMMARY

Breadboard device arrays have been fabricated. The process specification steps for making a complete display are being perfected. The pilot plant for the TFT and EL stack is completed. The facilities for the addressing stack and counter-electrode stack are being upgraded.

## ACKNOWLEDGEMENTS

I would like to express my sincere thanks to Mr. I. Reingold, Dr. E. Schlam and Mr. R. M. Miller, of ERADCOM, U. S. Army, for their interest and support; To the Aerojet ElectroSystems Dept. 8211 Staff for their skilled and dedicated work; To Mr. T. B. Odom and Mr. W. J. Helm of Aerojet for their advice and counsel; and to my predecessors, former employees at Aerojet, Dr. G. Cramer and Mr. K. O. Fugate, for their initial work on TFTs and EL displays.

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5. Z. K. Kun, et. al., "Thin-Film Transistor Switching of Thin-Film Electroluminescent Display Elements", SID Pro. Vol. 21, No. 2 (1980).
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## FIGURES


1. Cross Section of Dual Gate TFT
2. Pixel Electrical Circuit for Driving High Voltage EL
3. Planar View of Pixel TFT Circuit
4. Typical Thin Film Transistor Parameters
5. EL Brightness Performance
6. EL/TFT Extrinsic Switching Matrix Addressing Technique
7. Process Profile
8. Methods For Joining TFT's to Display

# Cross Section of Dual Gate TFT

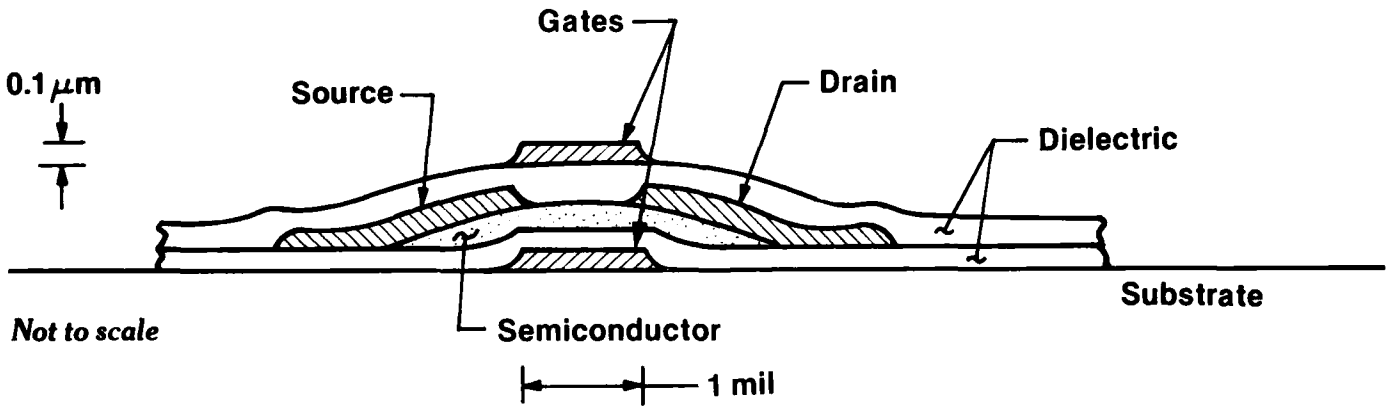




Figure 1.

# Pixel Electrical Circuit for Driving High Voltage EL

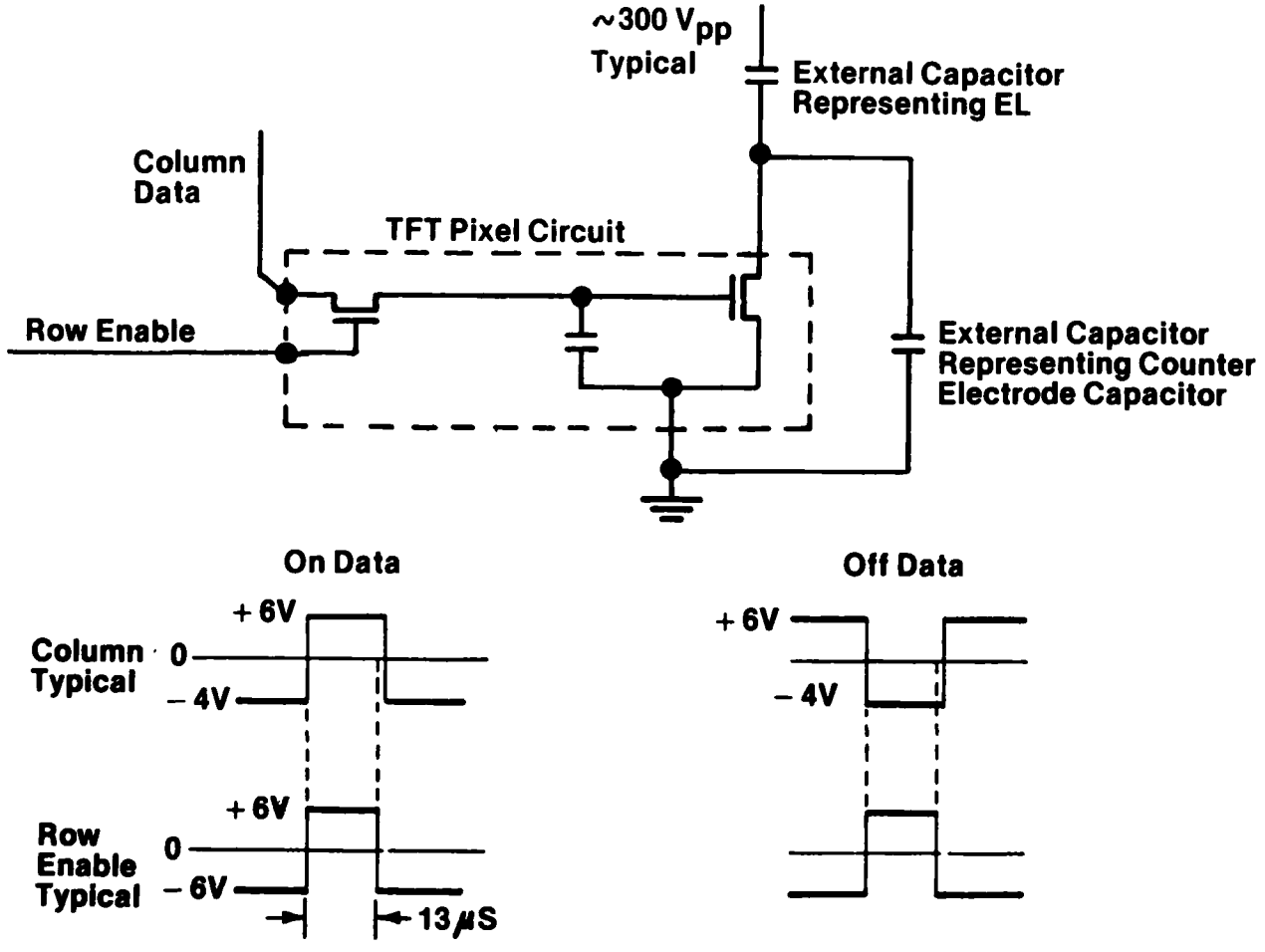


Figure 2.

# Planar View of Pixel TFT Circuit

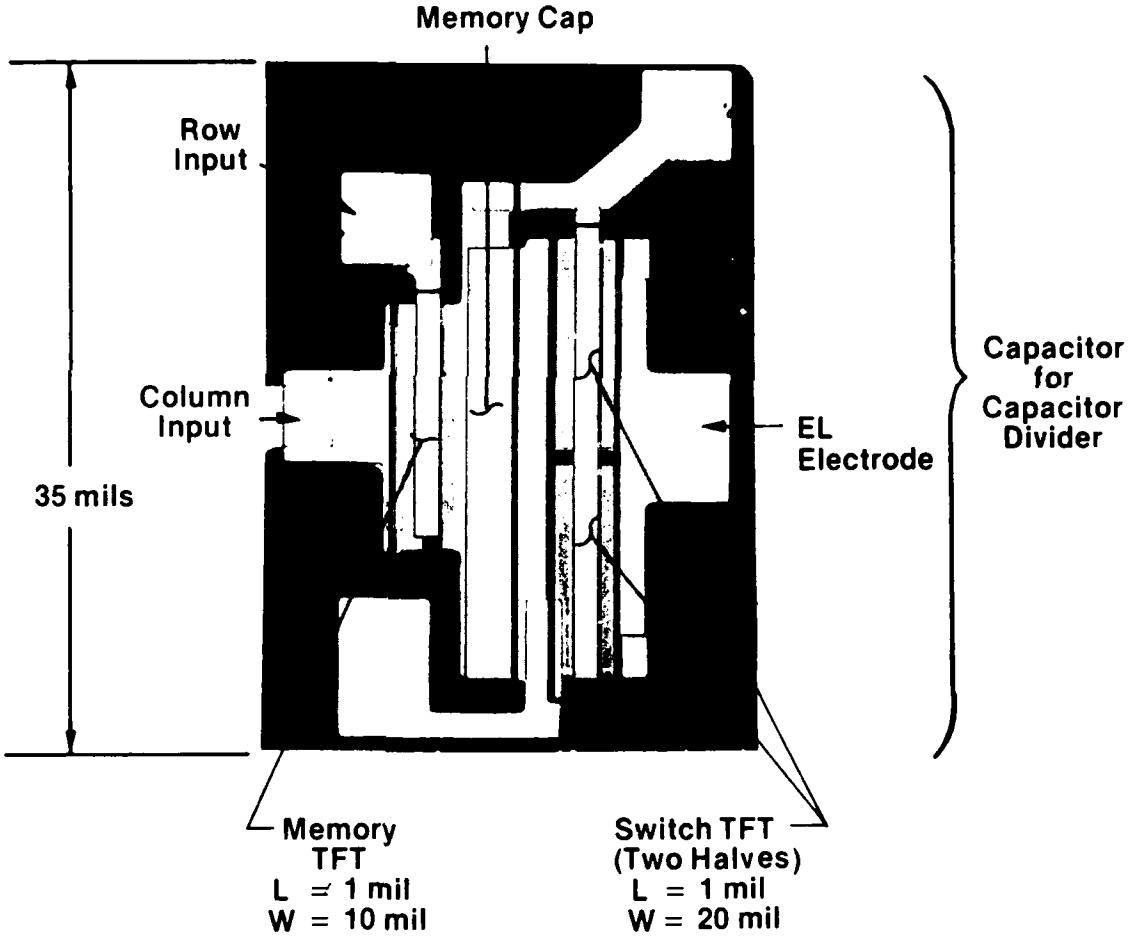


Figure 3.

# Typical Thin Film Transistor Parameters

*Source: Aerojet ElectroSystems Co., Azusa, Ca.*

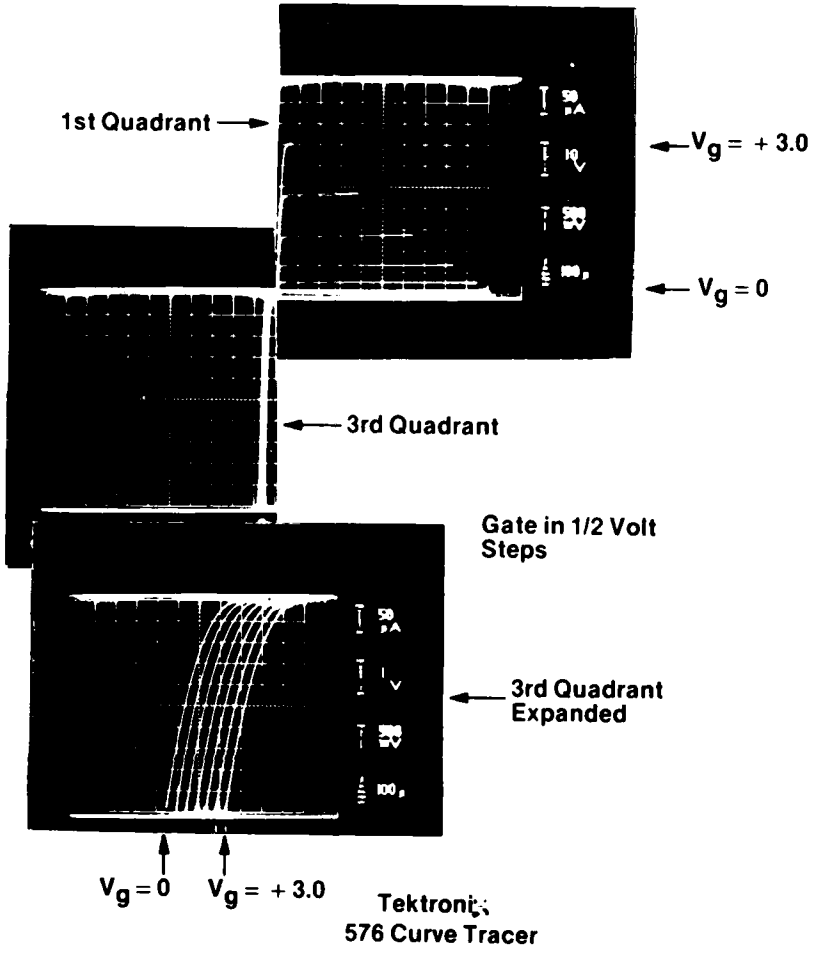


Figure 4.

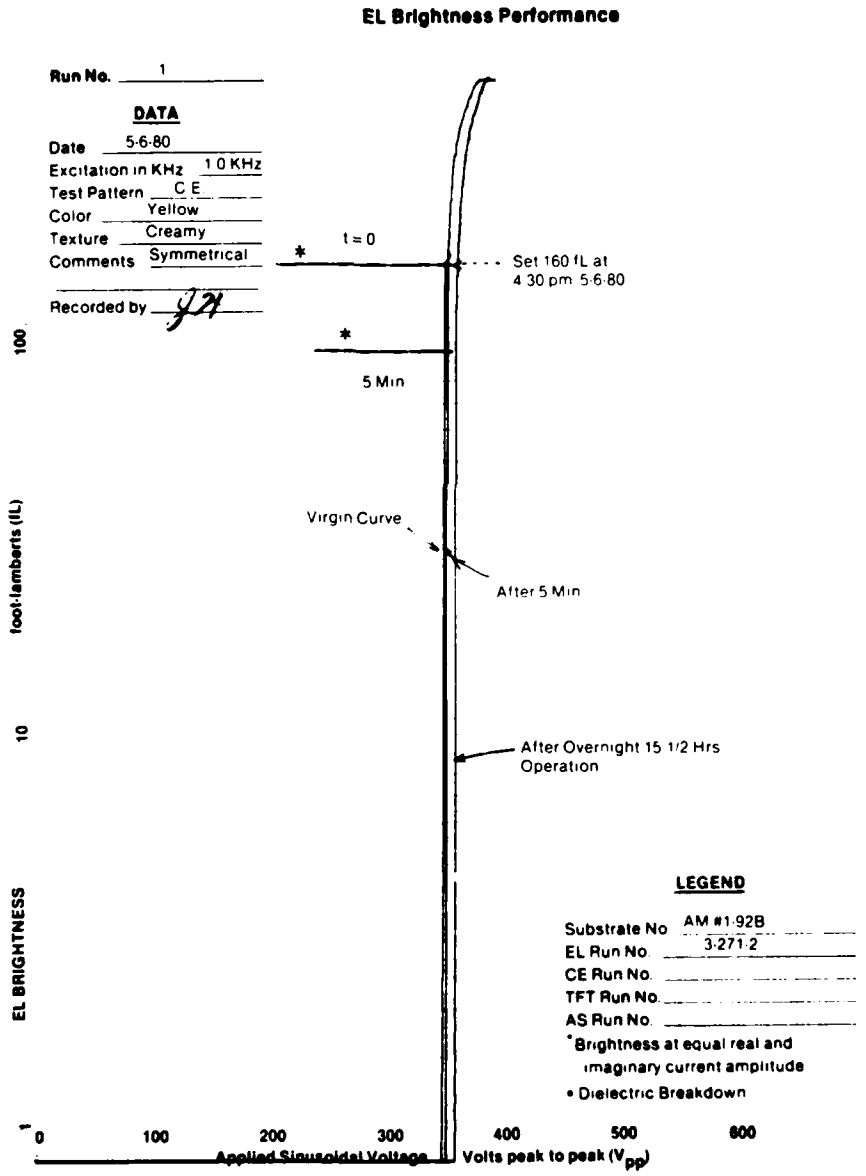
EL Brightness Performance
Run No. 1
DATA
Date 5-6-80
Excitation in KHz 1.0 KHz
Test Pattern C E
Color Yellow
Texture Creamy
Comments Symmetrical
Recorded by
t = 0
Set 160 fL at 4 30 pm 5-6-80
5 Min
Virgin Curve
After 5 Min
After Overnight 15 1/2 Hrs Operation
EL BRIGHTNESS
foot-lamberts (fL)
100
10
1
0
100
200
300
400
500
600
Applied Sinusoidal Voltage
Volts peak to peak ($V_{pp}$)
LEGEND
Substrate No AM #1-92B
EL Run No. 3-271-2
CE Run No.
TFT Run No.
AS Run No.
*Brightness at equal real and imaginary current amplitude
• Dielectric Breakdown

Figure 5.

# EL/TFT Extrinsic Switching Matrix Addressing Technique

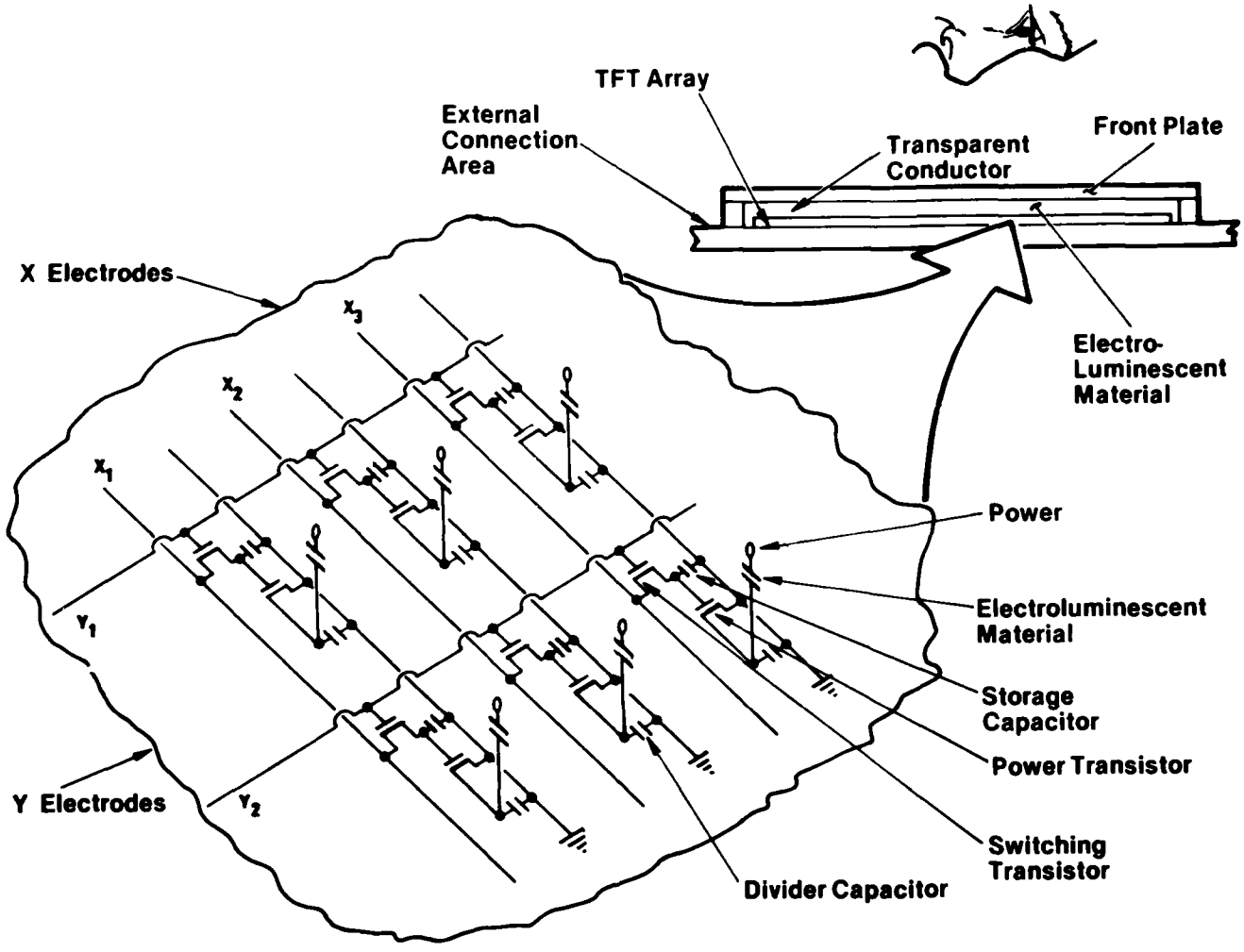


Figure 6.

# Process Profile

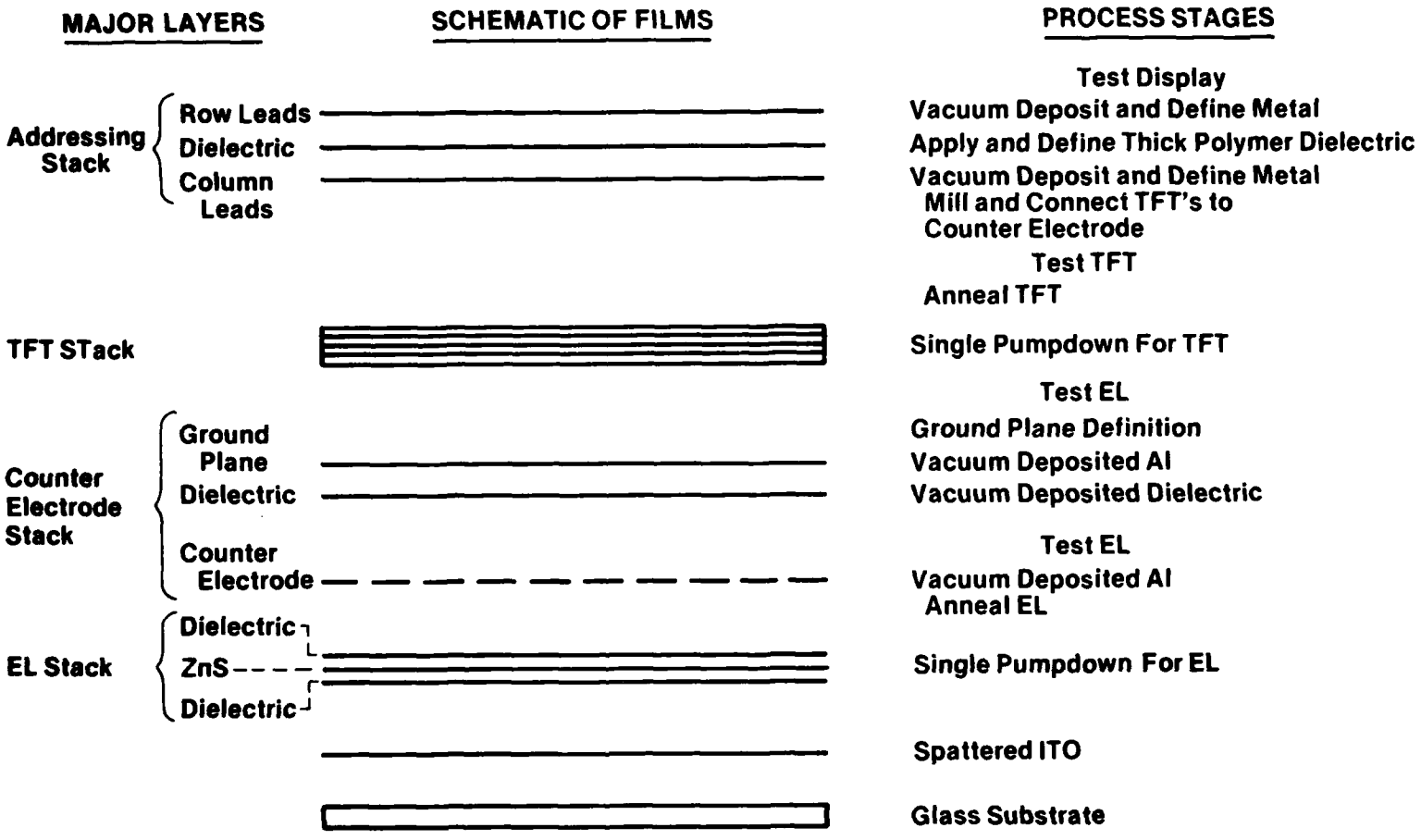


Figure 7.

# Methods For Joining TFT's To Display

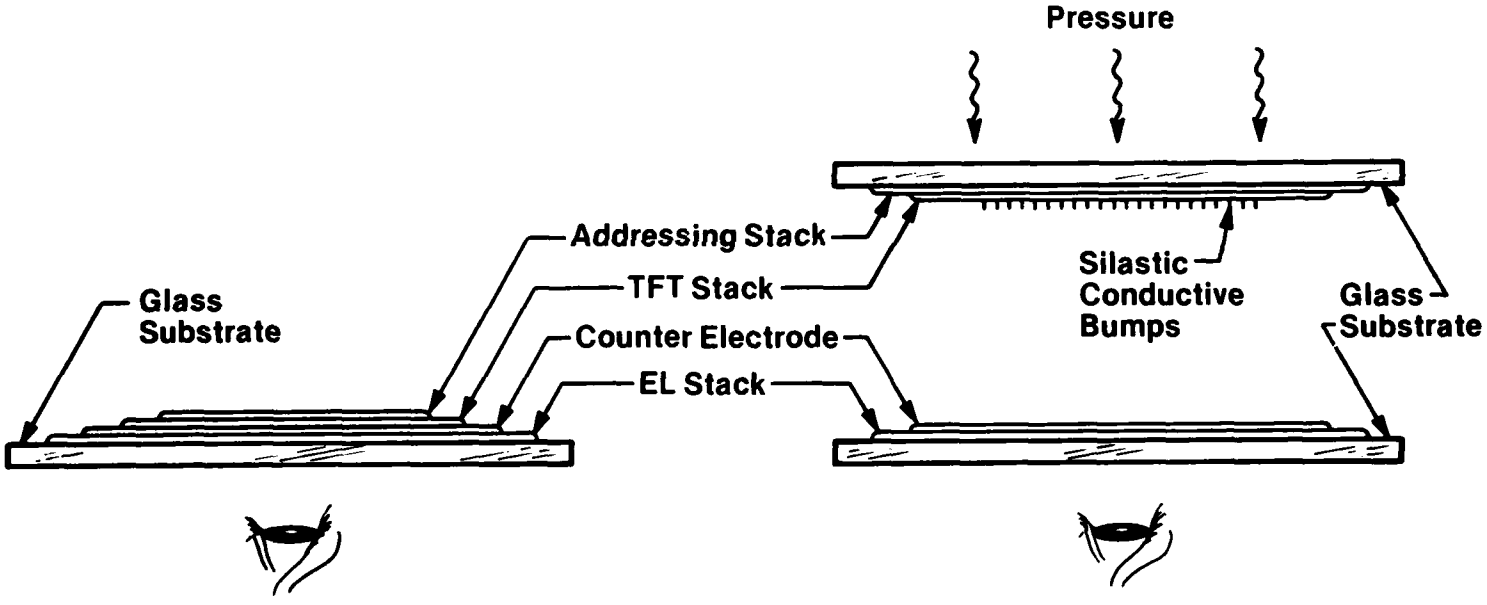


Figure 8.

# HYBRID SUBSTRATES WITH HIGH SHEET RESISTIVITY FILM

BY

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## ABSTRACT

A process for fabricating substrates with a high sheet resistivity film for hybrid circuits applications was established under contract to Naval Avionics Center. These substrates have a 2 to 3 kilo ohm per square cermet resistive layer, covered by a metallic diffusion barrier layer, topped by a thick gold conductive layer suitable for wire bonding. The possibility of patterning these substrates by conventional wet chemical photolithography to a .5 mil resolution was demonstrated. The formulation of the cermet layer, its deposition and annealing process were optimized to achieve a Temperature Coefficient of Resistance (TCR) less than 100 ppm/°C and long term stability.

## INTRODUCTION

Until now, hybrid circuit manufacturers have used mainly Ni-Cr alloys for the resistive film of their thin film substrates. The resistivity of Ni-Cr alloys is not very high, therefore it is difficult to obtain films of over 500 ohms per square on smooth, polished surfaces and over 300 ohms per square on as-fired alumina substrates. Other films are available, such as tantalum nitride whose sheet resistivity is not much higher than that of Ni-Cr alloys.

Microelectronic Technology today, especially in the area of signal processing, tends toward smaller structures and lower power for each circuit element. This implies high values for the resistors. At less than 300 ohms per square, nichrome resistors take up too much substrate area. The purpose of contract #N00163-79-C-0172 from NAC (Indianapolis, IN) is to establish a source of hybrid substrates with a resistive thin film of 2 kΩ to 3 kΩ per square. Such substrates must also have a gold conductive film of 3.8 micrometer (150 microinches) thickness, suitable for wire bonding with both Al and Au wires. A barrier layer can be deposited between the resistive film and the gold. As an overview, Figure 1 shows a schematic cross-sectional view of the layers on a hybrid substrate.

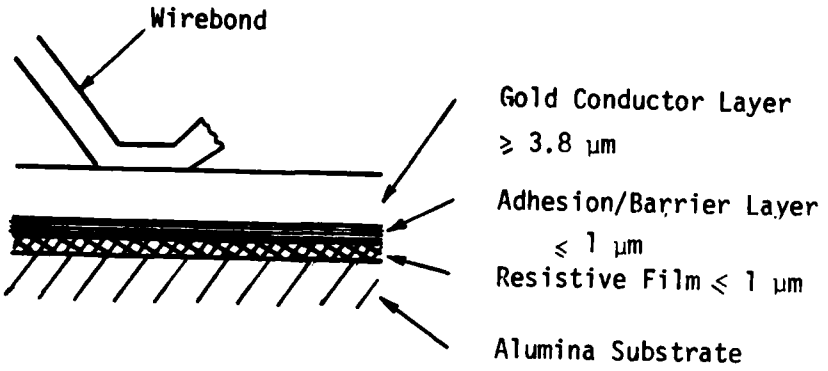


FIGURE 1. SCHEMATIC CROSS-SECTION OF LAYERS

The important specifications such substrates have to meet are:

| | | |
|---|---|---|
| Substrate: | 50.8mm x 76.2mm x 0.635mm | |
| Thickness of layers: | Resistive layer: | Max. 10,000Å |
| | Barrier layer: | Max. 10,000Å |
| | Gold: | Min. 3.8μm |
| Sheet resistivity: | 2 to 3 kΩ per square | |
| Conductivity/Bondability: | Gold conductor: | Less than 10mΩ/square, suitable for wire bonding with Al and Au wire |
| TCR of resistive layer: | Less than 100 ppm/°C in absolute value (positive or negative) | |
| High temperature stability: | Variation of less than .5% for 15 min. at 350°C in air | |
| Load stability: | Variation of less than .5% for 1000 hours at 3.88 watt/cm$^2$ | |
| Long term stability: | Variation of less than .5% for 1000 hours at 125°C | |
| Photodelineation: | Resistive film to be delineated to 12.7μm lines with 25.4μm spacing. | |

## AIM OF PROGRAM

The aim of this Manufacturing Technology Program is to establish a source of such hybrid substrates capable of delivering 250 substrates a month.

## APPROACH

A review of the literature (1 to 14) indicated that the Cr-SiO cermets were the materials with the best chances of meeting all the specifications. Cr-SiO cermets can be deposited by various methods: Vacuum deposition can be used, from two sources (1) (11), or from one source, where the temperature of the source controls the composition of the film (1). Flash-evaporation has been used extensively, too (1)(12)(13). Cr-SiO films can also be deposited by sputtering using a composite target having the desired composition.

Sputtering-Deposition provides good reproducibility of composition of the deposited film since the stoichiometry of the sputtering target is preserved from run to run. It was therefore decided that RF sputtering using commercially available alloy targets was the simplest, most production-adaptable deposition technique for reproducible high sheet resistivity films.

Furthermore, to test the transferability of the process, it was decided, at Hughes Aircraft Company, that the process would be defined in our main engineering facilities in Culver City (CA) and then implemented in one of the production plants, namely, Newport Beach (CA) 50 miles away.

This report covers only the process definition phase of the program.

## EXPERIMENTAL APPARATUS

All samples were prepared using an engineering development sputtering system (Figure 2) utilizing 6 inch diameter commercially prepared sputtering targets. The targets were bonded to aluminum backing plates using conductive epoxy. Water cooling was provided for both the target and the substrate stage. A standard mechanical vacuum pump was used for rough pumping and a 260 liter/sec turbomolecular pump provided high vacuum pumping. An ultimate pressure of $5 \times 10^{-7}$ torr ($6.7 \times 10^{-5}$ pascal) was obtainable as measured by a Bayard-Alpert type ionization gauge. Sputtering pressure measurements were made with a Pirani-type gauge and were recorded without correction for gas type which was ultra-pure argon in all instances.

Initial efforts were carried out by standardizing the power and pressure and varying the deposition time. This method was found to be unreliable. A resistance monitoring capability (Figure 3) was added to facilitate acquisition of repeatable results. At a later time, a shutter was added to allow for sputter cleaning of the target prior to deposition onto the sample substrates. In all cases, a one square monitor was used during depositions giving results directly in ohms per square.

The resistance of the monitor sample was measured with a Triplett meter during deposition and all subsequent measurements were accomplished with a digital ohmmeter. Initially, annealing was carried out on a hot plate with a thermocouple for temperature monitoring. At a later date, an air furnace became available which was then used for all annealing. TCR measurements

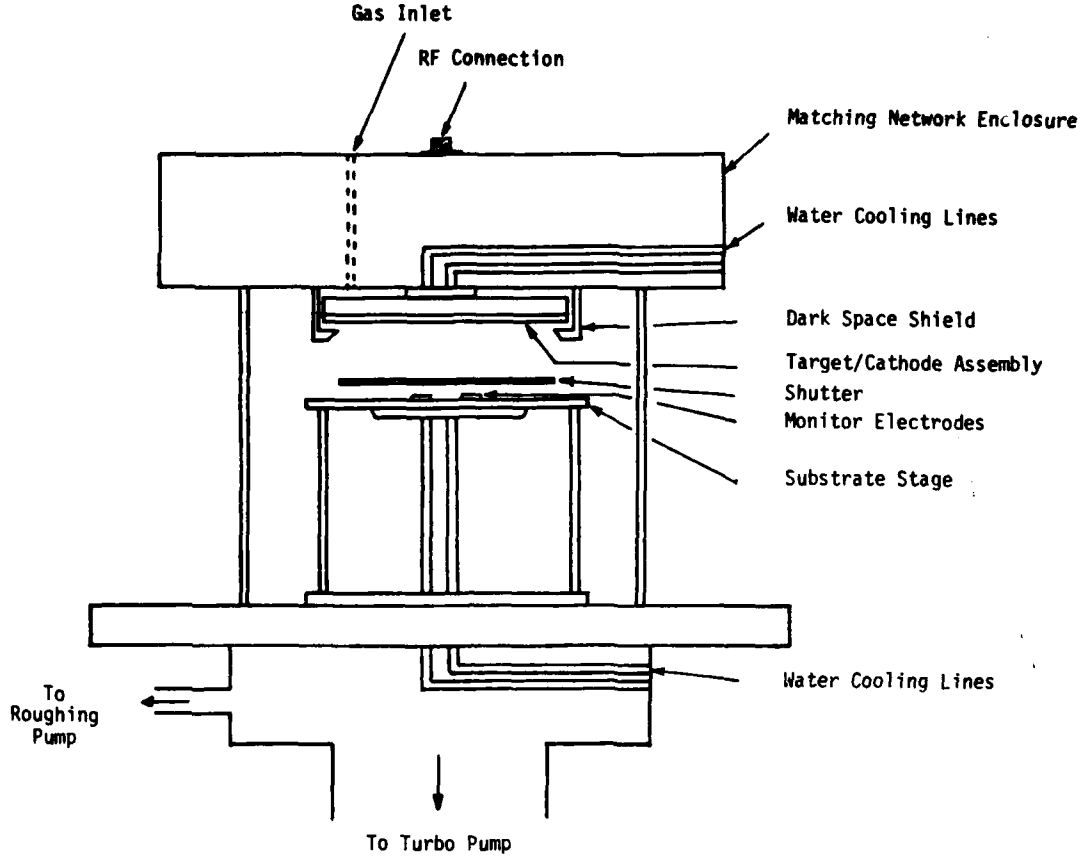


FIGURE 2. SCHEMATIC DIAGRAM OF SPUTTERING SYSTEM

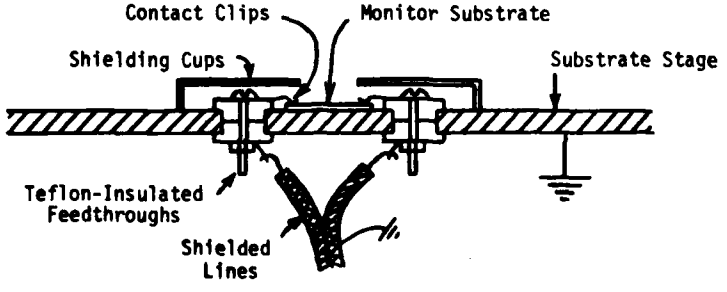


FIGURE 3. RESISTANCE MONITORING SETUP

were made using a hot plate.

Long term (1000 hour) stability tests at elevated temperature (125°C) were performed in an air convection oven. Long term (1000 hour) stability tests under power (3.88w/cm$^2$) were performed on a test fixture in still air.

## EXPERIMENTAL PROCEDURE: DEPOSITION

Substrates were cleaned and loaded onto the substrate stage. The system was evacuated to a pressure usually less than $5 \times 10^{-6}$ torr ($6.7 \times 10^{-4}$ pascal) and then backfilled with ultra-pure argon to a pressure of either $2 \times 10^{-3}$ torr ($2.7 \times 10^{-1}$ pascal) or $3 \times 10^{-3}$ torr ($4.0 \times 10^{-1}$ pascal). The RF power was applied and adjusted within a short time to the desired level for depositions made prior to installation of the shutter. For depositions made subsequent to shutter installation, pre-sputtering of the target for 10 minutes at 1.4w/cm$^2$ and a cathode bias of 2500 volts was performed and the power decreased to the desired level prior to opening the shutter. With resistance monitoring available, deposition continued until the desired value was obtained. The chamber was brought up to ambient pressure, the substrates removed and resistance measurements were made.

The resistance of the substrates was measured prior to annealing. The substrates were then mounted on a fixture sitting on a hot plate. The temperature was brought up to the desired level and held constant for approximately 30 minutes and then cooled to room temperature. Temperature and resistance values were recorded. A second excursion to the same temperature was performed with a fast rise time, no dwell and then cooled.

When an air furnace became available, the resistance of the substrates was measured, annealing was performed in the air furnace already at the desired temperature and then resistance measurements were made again. TCR measurements were carried out with the hot plate fixture.

## EXPERIMENTAL RESULTS

Resistive film depositions were carried out with cermet compositions ranging from 30% chromium to 70% chromium*. Program requirements dictated a maximum film thickness of 10,000Å for a sheet resistance of 2 to 3 k ohms per square. Films composed of 30% and 40% chromium required a thickness in excess of 10,000Å to provide the required sheet resistance thus eliminating these compositions. The cermets containing a higher chrome percentage provided the desired sheet resistance without exceeding a thickness of 10,000Å. Results are summarized in Table 1.

It was found that thickness versus sheet resistivity varied considerably during initial usage of a fresh target. Many hours of sputtering were required

*All Cr and SiO % ratios indicated are weight %.

before a target reached a point of producing repeatable results. This may be due to non-uniformity of composition.

TABLE 1

THICKNESS VERSUS FILM COMPOSITION

| FILM COMPOSITION (WEIGHT %) | THICKNESS (Å) | $R_S$(K OHMS/SQUARE) AS DEPOSITED | RESISTIVITY Ω cm | TCR(PPM/°C) AFTER ANNEAL |
|---|---|---|---|---|
| 30% Cr 70% SiO | 40,000 | 760 | >300 | -4000 |
| 40% Cr 60% SiO | 12,000-19,000 | 2-2.4 | .3 to .45 | -2000 to -1000 |
| 50% Cr 50% SiO | 875- 3,500 | 2.1-2.9 | .025 to .07 | -1000 to-275 |
| 60% Cr 40% SiO | NO DATA | | | |
| 70% Cr 30% SiO | 300- 1,500 | 2.1-2.8 | .008 to .03 | - 400 to -35 |

EXPERIMENTAL RESULTS: ANNEALING

All anneals and TCR measurements were carried out as described earlier. The sheet resistance of an "as deposited" substrate had to be determined in order to provide a value of 2 to 3 k ohms/square after annealing with a TCR of less than 100 ppm/°C. Depositions were performed at various pressures and power levels with anneals at 360°C to 450°C for the early work. Later efforts concentrated on an annealing temperature of 500°C. In all cases, it was observed that there seemed to be a transition value for the sheet resistance. For samples with a higher sheet resistance, annealing caused a drop in value initially followed by a rise if further annealing was applied. Exposure to temperatures less than that at which annealing had been carried out caused little or no change in sheet resistance. Results of the annealing tests are contained in Table 2.

Standardization of the cermet composition on 70% Cr 30% SiO, installation of the resistance monitor and of the shutter for sputter-cleaning of the target before deposition were expected to eliminate any lack of reproducibility in the resistor film properties. One last factor was then found to have a marked influence upon the properties of the resistor film: the residual pressure before backfilling with Argon (the sputtering gas).

Figure 4 shows the resistance of the monitor substrate as a function of the deposition time, for various values of the residual pressure. The RF power was held constant at 110 watts for each deposition. At a higher residual pressure, the data indicates that more time is needed to deposit a layer of the same sheet resistivity. If the deposition rate is constant (constant RF power), this could be interpreted as a different degree of porosity or an increase in oxidation of the resistive film.

The change of the sheet resistivity during annealing must be predictable in order to end up with a 2-3 kΩ per square film. Here again, there is a strong

TABLE 2

ANNEALING RESULTS

| Cr CONTENT WEIGHT % | SPUTTERING PRESSURE $10^{-3}$ TORR | ANNEAL TEMP °C | SOAK TIME (min) | kΩ/□ TRANSITION SHEET RESISTANCE | TCR FOR 2-3kΩ/□ TCR IN PPM/°C | COMMENTS |
|---|---|---|---|---|---|---|
| 30 | 2 | 400 | 30 | Not Determined | Not Determined | 760kΩ/□ , \|TCR\|>3000 |
| 40 | 2 | 400 | 30 | 3.7 | -2000 | |
| | 3 | 400 | 30 | Not Determined | Not Determined | 1.6-2kΩ/□, \|TCR\|>1000 |
| 50 | 2 | 360 | 30 | 3 | -680 to -700 | |
| | 2 | 400 | 30 | 2.9 | -750 to -950 | |
| | 2 | 420 | 30 | >3.4 | -800 to -850 | |
| | 2 | 450 | 30 | 2.5 | -250 to -300 | |
| | 3 | 360 | 30 | 3 | -750 to -950 | |
| | 3 | 400 | 30 | 2.9 | -850 to -900 | |
| | 3 | 450 | 30 | 2.7 | -550 to -600 | |
| 70 | 2 | 450 | 30 | >2.5 | -105 to -400 | |
| | 2 | 500 | 30 | >2.5 | - 30 to - 40 | |
| | 2 | 500 | 60 | | - 15 to - 30 | |

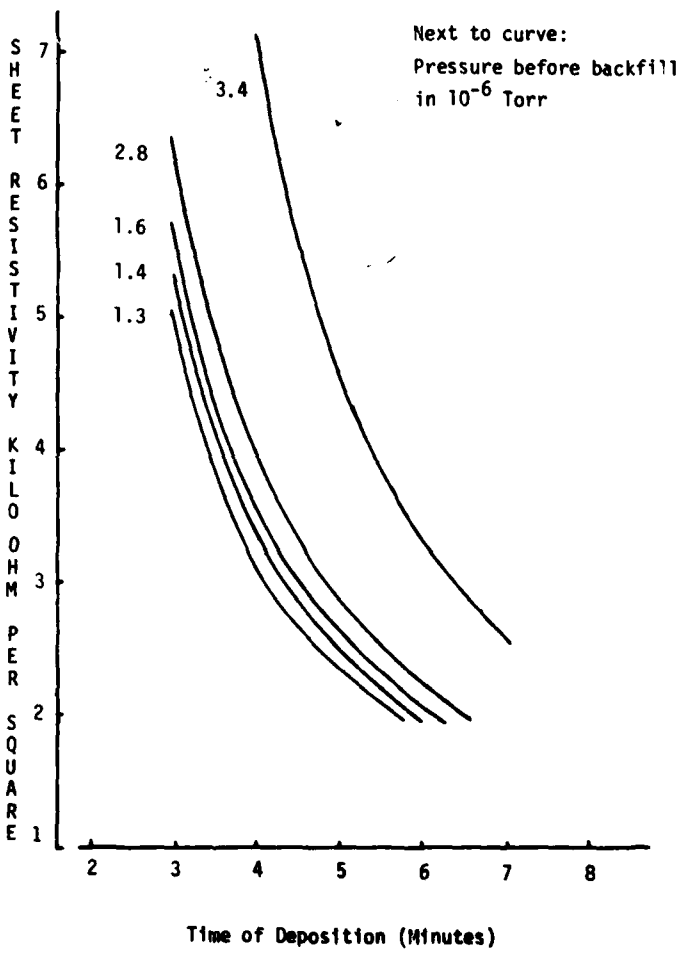


FIGURE 4. SHEET RESISTIVITY VS. DEPOSITION TIME.

but reproducible influence of the residual pressure prior to argon backfill. Figure 5 shows the sheet resistivity of the cermet film as a function of the annealing time at 450°C. It illustrates the following trends: If a film has been sputtered in argon with a large residual pressure, its sheet resistivity will likely go down at first during annealing, to come back up later; if a film has been sputtered in argon with low residual pressure, its sheet resistivity will go up during annealing, right from the onset. This is true for several values of the initial sheet resistivity. This relationship, which may vary from system to system, must be known if a predictable end value for the sheet resistivity is desired.

On the other hand, the temperature coefficient of resistance (TCR) exhibits no definite dependence upon the residual pressure before backfill. Figure 6 shows the variation of the TCR as a function of annealing time at 450°C, for several substrates with 70% Cr 30% SiO cermet films deposited at various values of residual gas pressure. The TCR decreases* during annealing and stays low for a long time before showing a trend upwards, while the sheet resistivity of the samples had gone up considerably, so much so that a sample at 8.2 kΩ per square with a TCR below 100 ppm/°C was produced and another with 12.5 kΩ per square and a TCR of only -130 ppm/°C.

## EXPERIMENTAL RESULTS: STABILITY TEST

Program requirements stipulated a sheet resistance variation of less than ± 0.5% for films subjected to the following conditions:

a. 1000 hours at 125°C
b. 1000 hours at 3.88 watts/cm$^2$
c. 15 minutes at 350°C in still air

Samples were prepared and subjected to the required conditions. Results are summarized in Table 3. It must be noted that the results for requirements c listed above were obtained using a more rigid test condition. All results were obtained by subjecting the samples to an excursion to the annealing temperature which was higher than 350°C.

## EXPERIMENTAL RESULTS: ETCHING

Early efforts to produce a circuit from the cermet films centered around the use of Ni-Cr as an adhesion layer between the cermet and the gold. (The adhesion obtained between the cermet and gold was tenuous at best.) This necessitated etchants which would preferentially etch NiCr and not the cermet. For cermet films containing 50% chromium, it was possible to etch the NiCr using ceric ammonium nitrate-based commercially prepared chromium etchant or ceric sulfate with little or no effect on the cermet resistance. However, these etchants had a pronounced effect on the 70% chromium cermet films and use of NiCr alloys was dropped.

*in absolute value

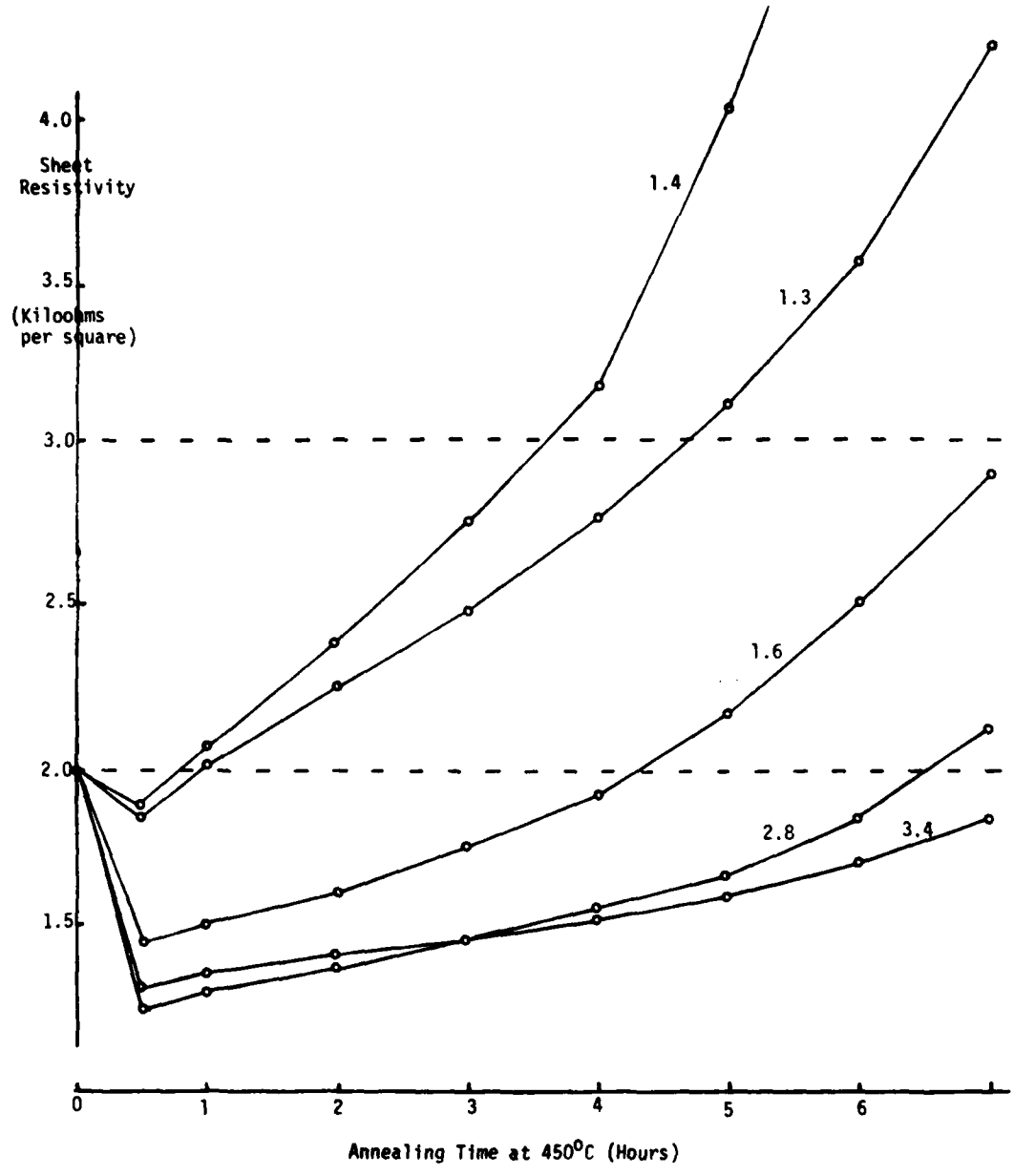


FIGURE 5. SHEET RESISTIVITY VS. ANNEALING TIME FOR 70/30 Cr/SiO

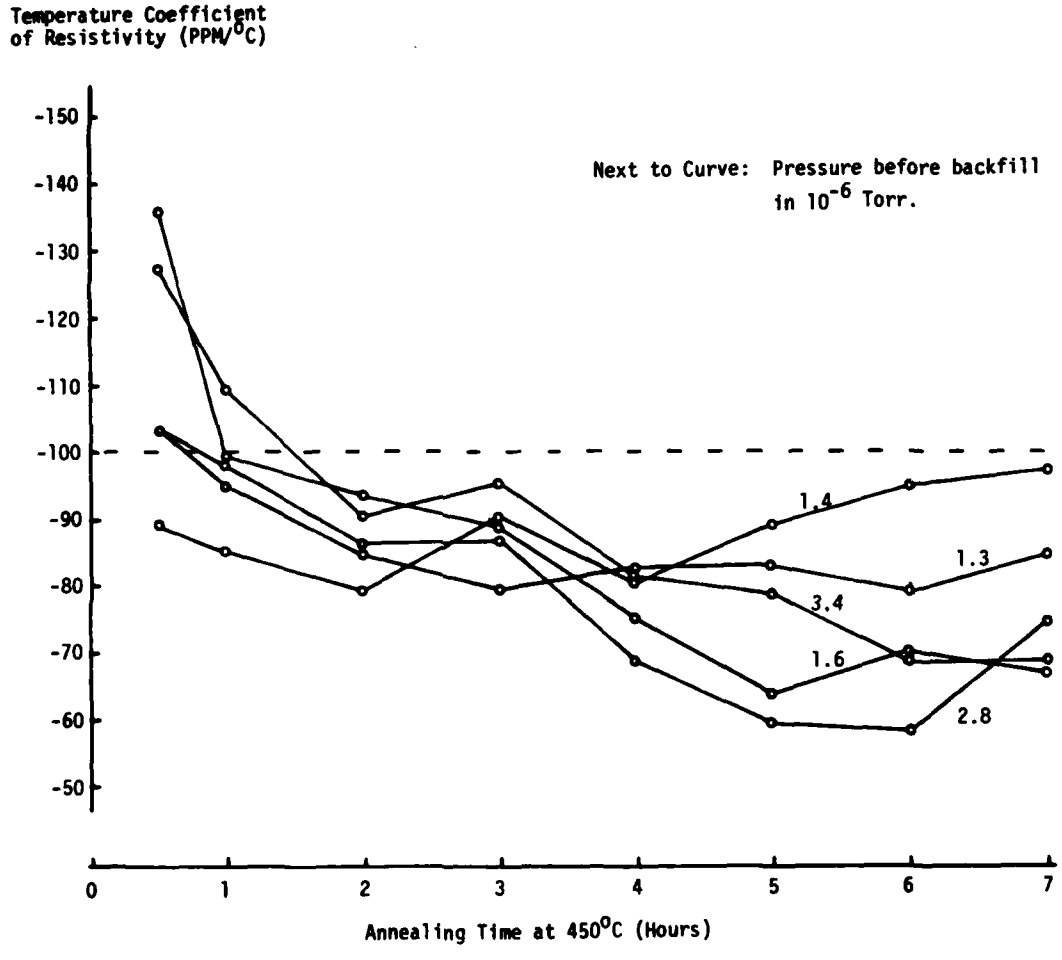


FIGURE 6. TCR VS. ANNEALING TIME FOR 70/30 Cr/SiO

TABLE 3

STABILITY TESTS

| Chromium Content WT. % | 1000 Hr. Temperature Stability Test /Rs-Ri/x100 Ri | | 1000 Hr. Power Stability Test /Rs-Ri/x100 Ri | | 15 Min. 350°C Stability Test /Rs-Ri/x100 Ri | | % Passed | Anneal Temp |
|---|---|---|---|---|---|---|---|---|
| | All Samples | Passed Samples | All Samples | Passed Samples | All Samples | Passed Samples | | |
| 30 | 3.024 | -- | -- | -- | -- | -- | 0 | 420 |
| 40 | .853±1.023 | .149±.131 | -- | -- | -- | -- | 60 | 420 |
| | -- | -- | -- | -- | 9.922±20.512 | 0 | 20 | 420 |
| 50 | .196±.271 | .114±.119 | -- | -- | -- | -- | 89 | 400-450 |
| | -- | -- | 2.039±3.413 | .069±.047 | -- | -- | 67 | 400-420 |
| | -- | -- | -- | -- | -- | .214±.170 | 67 | 400-450 |
| 70 | .311±.112 | .311±.112 | -- | -- | -- | -- | 100 | 450 |
| | -- | -- | .302±.047 | .302±.047 | -- | -- | 100 | 450 |
| | -- | -- | -- | -- | .225±.210 | .225±.210 | 100 | 450 |

Nickel was then investigated for use as both an adhesion layer and a diffusion barrier. Cermet monitor substrates were subjected to a variety of etchants and resistance measurements made after each etchant exposure. Results of these tests are shown in Table 4.

TABLE 4

ETCH RATES OF 70% Cr 30% SiO FILMS

| ETCHANT | TEMPERATURE | RESISTANCE CHANGE IN%* | TIME (MIN) | % PER MIN |
|---|---|---|---|---|
| Chrome Etchant ** | 53°C | 54 | .5 | 108 |
| kI + $I_2$ Gold Etch | 55°C | 3 | 3 | 1 |
| $FeCl_3$ (43°Be') | 56°C | 1.5 | 3 | .5 |
| Aqua Regia | 25°C | 3 | 3 | 1 |

* for 2 to 3 kΩ per square films
** cerric ammonium nitrate + nitric acid

Tests of nickel as a diffusion barrier eliminated it from consideration and palladium was nominated (15). The use of aqua regia as a palladium etchant proved successful.

The gold film was etched using both a cyanide-based commercial etchant and a potassium iodide based commercial etchant. The latter was found to provide shorter etch times with significantly reduced undercutting of the etched lines.

For all circuit patterning, negative photoresist was used. This was necessitated by the etchant used for cermet etching. A mixture of potassium fericyanide and sodium hydroxide provides rapid cermet etching but the presence of sodium hydroxide caused severe breakdown in positive photoresist. Post-baking the negative photoresist at 160°C for 20 minutes was found necessary to prevent lifting of the resist at line edges. Photoresist patterning and etching are carried out in the sequence shown in Table 5.

TABLE 5

ETCHING STEPS FOR RESISTORS/CONDUCTORS PATTERN

1. Apply conductors-only pattern
2. Etch gold in KI + $I_2$ based etchant
3. Etch palladium in aqua regia
4. Apply composite pattern
5. Etch cermet in $K_3(Fe(CN)_6)$ + NaOH etchant

## DIFFUSION BARRIER LAYER

Upon annealing substrates which had the gold condutor layer deposited directly over the cermet film, it became visually evident (by the discoloration of the gold) that the chromium was diffusing through the gold. A bonding test confirmed what was expected: the discolored gold was not bondable. Test substrates were then produced with barrier layers of various kinds. Table 6 gives the results of the bonding tests following annealing of these test substrates. Of the materials tested, only palladium was successful as a diffusion barrier.

TABLE 6

BONDABILITY AFTER ANNEALING

| BARRIER | ANNEALING | REMARKS |
|---|---|---|
| 1000Å Mo + 10,000Å Ni | 450°C 2 hours | Strong discoloration of Au, no bonding possible |
| 20,000Å Ni | 450°C 2 hours | Light discoloration of Au no bonding possible |
| 20,000Å Ni | 450°C ½ hour | Light discoloration of Au bonding possible only after light abrasion of gold (eraser) |
| 3000Å Pd | 450°C 4 hours | No discoloration of Au good bondability with Au wire as well as Al wire |
| 3000Å Pd | 500°C 2 hours | No discoloration of Au good bondability with Au wire as well as Al wire |

## EXPERIMENTAL RESULTS: TCR VALUES FOR FABRICATED RESISTORS

70/30 Cr/SiO cermet was deposited onto a 1" x 1" x .025" AlSiMag 772 substrate which was then metallized with palladium and gold. A test pattern consisting of 16 resistors was fabricated using photolithography and liquid etchants. The test pattern was then annealed in air for 30 minutes at 500°C and then cut to fit a hybrid package. It was mounted in the package and 13 of the 16 resistors were wire bonded to the package leads. The package was then sealed and placed in a fixture which allowed a thermal head to come down around the package for temperature control. The package was taken to each of 8 temperatures and the resistors were measured. TCR's were calculated and averaged at each temperature. The mean value and standard deviation are shown in Figure 7.

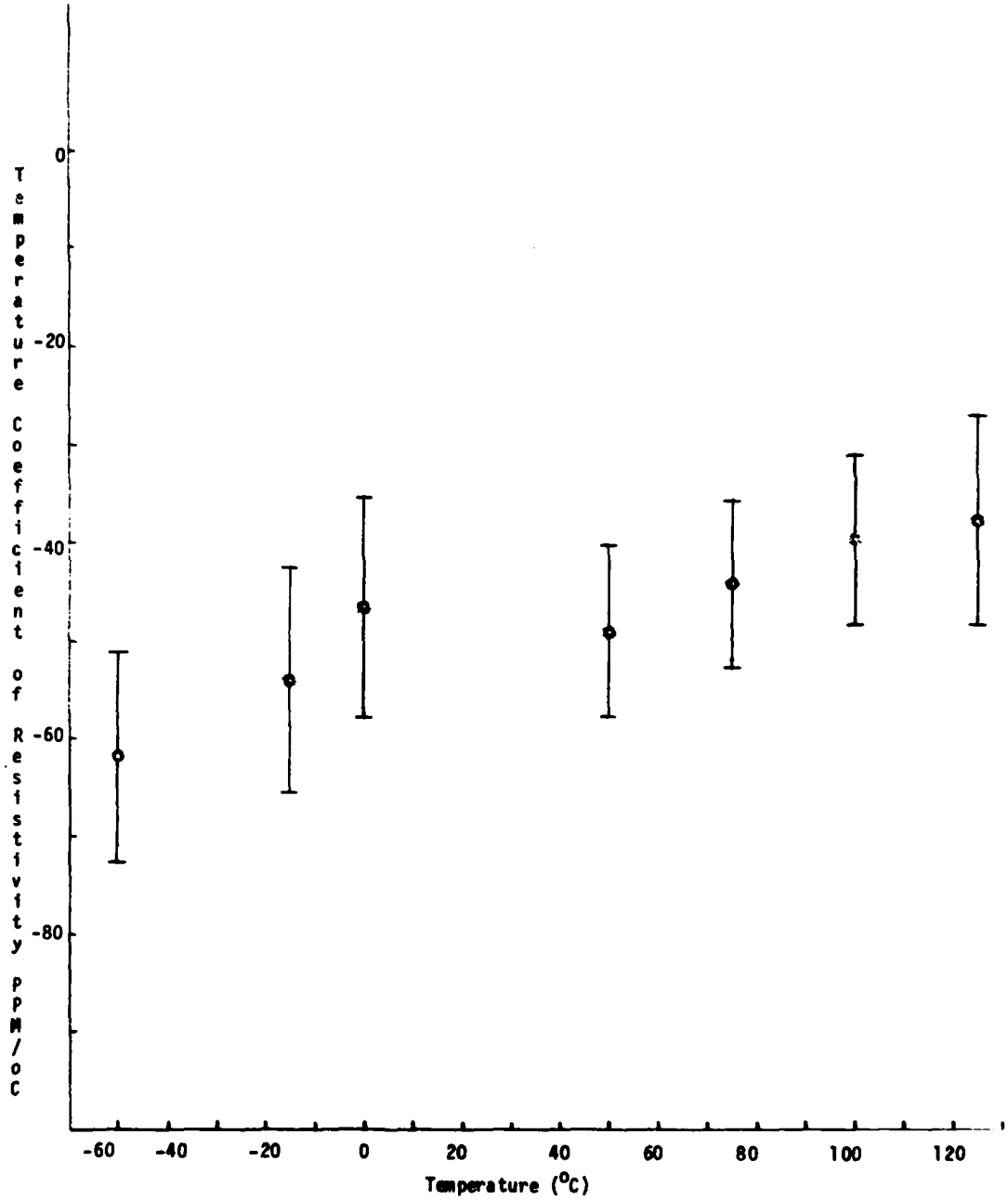


Figure 7. TCR versus Temperature: 70% Cr 30% SiO Resistors

## DISCUSSION OF RESULTS: DEPOSITION

The cermet films, as deposited using RF sputtering, exhibit strong dependency upon deposition parameters. The first of these parameters is substrate temperature. Films deposited at a higher substrate temperature required longer deposition times and exhibited a higher TCR value. It is therefore necessary to impose an upper limit upon the temperature a substrate may reach during the deposition process. This can be accomplished using a water cooled substrate stage and results in films with acceptably low TCR values. The second parameter is related to the residual gas content of the system prior to backfilling with sputtering gas. It was noted that for higher pressures in the vacuum chamber prior to backfill, greater resistance changes took place during film annealing. The use of a setpoint-equipped pressure gauge to initiate backfill with argon at a prescribed pressure can facilitate the control of this parameter.

As is to be expected, strict control must be maintained over the pressure at which sputtering occurs and the power level used for deposition. The former appears to be the more important of the two.

## POST-DEPOSITION PROCESSING

Due to the high temperature required for film annealing, it is necessary to introduce a diffusion barrier between the cermet film and the gold metallization for preservation of wire bondability. Palladium accomplishes this purpose quite successfully and imposes no technical constraints upon the manufacturing process. It is, however, necessary to apply the palladium layer during the same pumpdown as used for the cermet deposition. Exposure of the cermet film to air prior to deposition of the palladium film reduces adhesion between the two films and can cause blistering during the annealing cycle. For this reason, a multiple target sputtering system is a necessity.

Annealing of the films is carried out subsequent to circuit fabrication processes. A temperature of at least 500$^{o}$C is necessary to produce films with TCR's under 100 ppm/$^{o}$C with a reasonably short anneal time. No upper limit on the annealing temperature has been determined.

The most stringent requirement imposed upon circuit processing is the need for a photoresist capable of maintaining its integrity during the cermet etching. The presence of sodium hydroxide as a constitutent of the cermet etchant eliminates most positive photoresists from consideration. Negative photoresist, when post baked at a higher temperature will stand up to the cermet etch.

## TRANSFER OF THE PROCESS FOR THE PRODUCTION PHASE

The manufacturing division in Newport Beach will manufacture the high ohms per square substrates using a VARIAN model 980-2405 RF sputtering apparatus. This apparatus has three 8" diameter targets, a 21" water cooled substrate

table, and two rotating shutter planes. It is fed by a 2 kw 13.56MHz RF power supply.

The plan for the process transfer is as follows:

1. Install all necessary sputtering targets and then, measure the distribution of sheet resistivities across the field of deposition.
2. Fabricate a deposition aperture plate to make the sheet resistivity as uniform as possible.
3. Measure the relationship between residual pressure before argon backfill and the properties of the cermet film.
4. Produce substrates.

## CONCLUSIONS

All work accomplished to date indicates that sputter deposited Cr-SiO films are fully capable of meeting the requirements imposed for use in microcircuit applications. Their use will entail a high degree of process control, ranging from control of the system pressure at which backfill is commenced to the time and temperature at which annealing is accomplished. These process control requirements are well within the capabilities available with present-day instrumentation and should impose no technical constraints upon the manufacturing environment.

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# FLIP TAB PROCESS BROADENS AND IMPROVES TAB TECHNOLOGY

BY

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## ABSTRACT

After tape automated bonding (TAB) at inner lead bonds (ILB) connecting chips to lead frames, the leaded chips are assembled in a flipped or face-down position in making the outer lead bonds (OLB). This process is called flip TAB. Key points in the process and materials used are reported. Results on a calculation of thermal energy dissipation and on aging experiments are presented. Advantages and limitations of the flip TAB process are discussed. The economy and versatility resulted from this process broaden the applicability of TAB. Enhanced reliability using flip TAB process improves TAB technology as a whole.

## INTRODUCTION

Tape automated bonding (TAB) has gradually gained industry-wide acceptance for chip assembly in dual-in-line packages (DIPs) and in hybrids due to its reliability and built-in chip handling and testing potentials. Honeywell Inc. has engaged in nearly all aspects of the development of this technology (Ref. 1 through 6). In the course of this development we found that certain restrictions imposed by the present method of face-up TAB assembly can be improved upon. Workers in this technology area have similar experience. This promoted investigations into alternative TAB structures (Ref. 7). The development of the new face-down or flip TAB process not only obviated the above-mentioned restrictions, but also showed a tremendous potential toward reducing TAB assembly cost and improving the overall reliability of the resulted product.

In this paper, material systems and processes used in flip TAB assembly are described. Calculations on thermal energy dissipation and results on a metallurgical evaluation of outer lead bonds (OLBs) made with flip TAB process are reported. The advantages and limitations of the flip TAB process are then discussed.

Assembly of chips directly on printed circuit boards with the flip TAB process considerably broadens the application of TAB technology. Cost

reduction is an impetus in promoting flip TAB process and improved reliability of resulted products proves that this method of chip assembly is indeed viable.

## FLIP TAB ASSEMBLY

In this section, key process steps as well as material systems using the flip TAB assembly method are described. For applications in multi-chip hybrids, repair procedures can often spell the difference between a practical and a theoretical process. Bond repair and chip replacement are therefore included.

### Key Process Steps

In the flip TAB process, a chip which has been inner lead bonded (ILB), is placed with its active surface down onto a substrate where an epoxy material has been placed on the die bond pad. All the extended leads from this chip are then bonded simultaneously to their respective bonding pads by thermocompression or modified thermocompression bonding. A step by step description is given below.

The leaded chip, either on reel or in an individual 2" x 2" slide carrier, is cut with the lead lengths 3-5 mils longer than the maximum spread of the outer lead bond (OLB) sites. This chip is then placed active face downward onto pre-placed B-stage epoxy material approximately 3-5 mils in thickness. The epoxy must be at a temperature of 120$^{o}$C. For large multi-chip hybrids, it is preferable that all chips be placed within 20 minutes of each other. After a partial cure of the epoxy, thermocompression (TC) bonds are made for all OLBs of each individual die. Figure 1 shows schematically the thermode, die and substrate positions during outer lead bonding. Figure 2 shows flip TABed chips on a multilayer ceramic substrate with gold thick film circuitry.

### Material Systems

Flip TAB procedures can be used in either individual IC packages or on hybrid structures with a variety of metallizations. Because of the relatively low overall processing temperature, printed circuit boards as well as ceramic substrates can utilize flip TAB assembly procedures. Metallization on ceramic substrates can be any of the common thick film or thin film materials. On printed circuit boards flip TAB of chips onto Sn/Pb solder coated copper circuits were successfully made.

To facilitate testing of chips after inner lead bonds, we recommend three layer tape. We used 35 mm polyimide tape laminated with epoxy to 1 ounce copper foils. The etched lead frames are then immersion plated with a tin coating to a thickness of 0.5 to 1 micron.

The epoxy material chip attach is electrically insulating yet thermally conductive in order to provide the mechanical integrity and enhance the heat

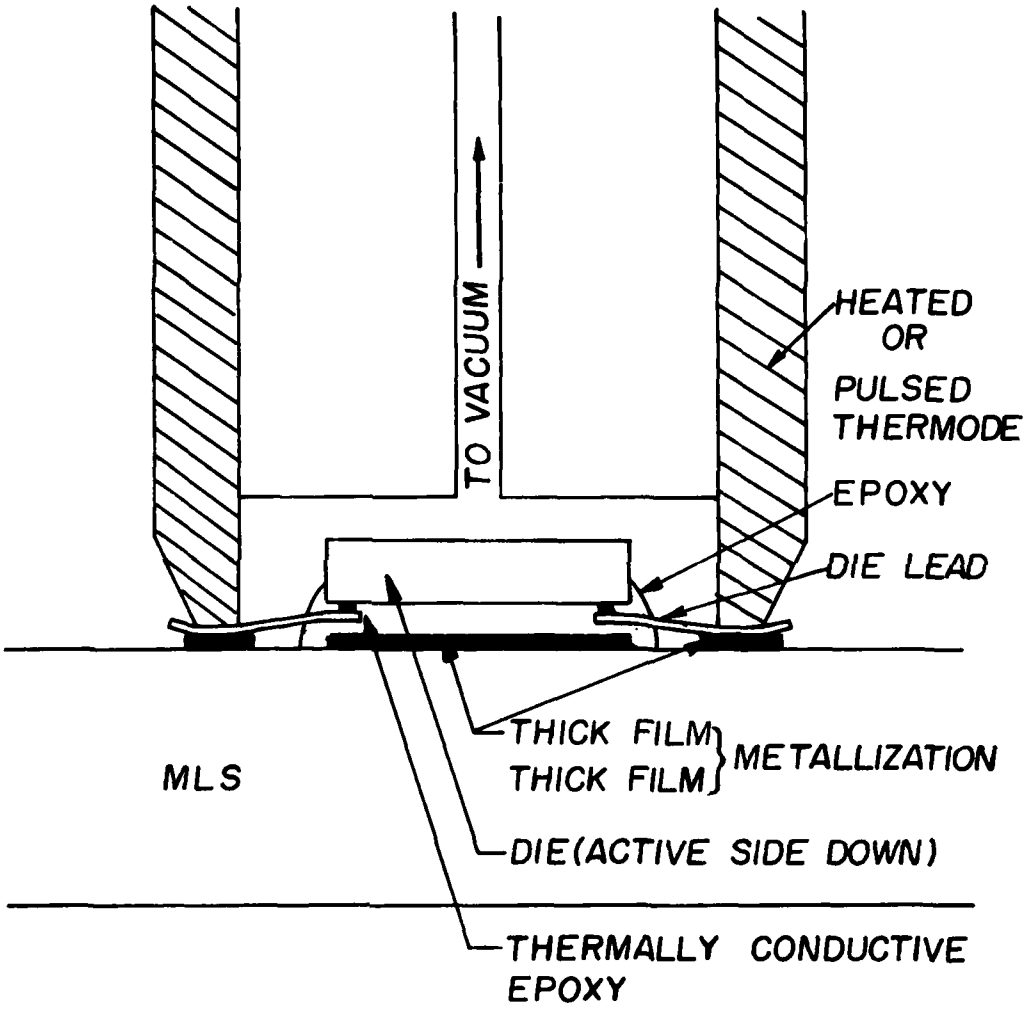


FIG. I: SCHEMATIC DIAGRAM SHOWING THERMODE IN PLACE FOR OUTER LEAD BONDING (OLB) IN FLIP TAB PROCESS.

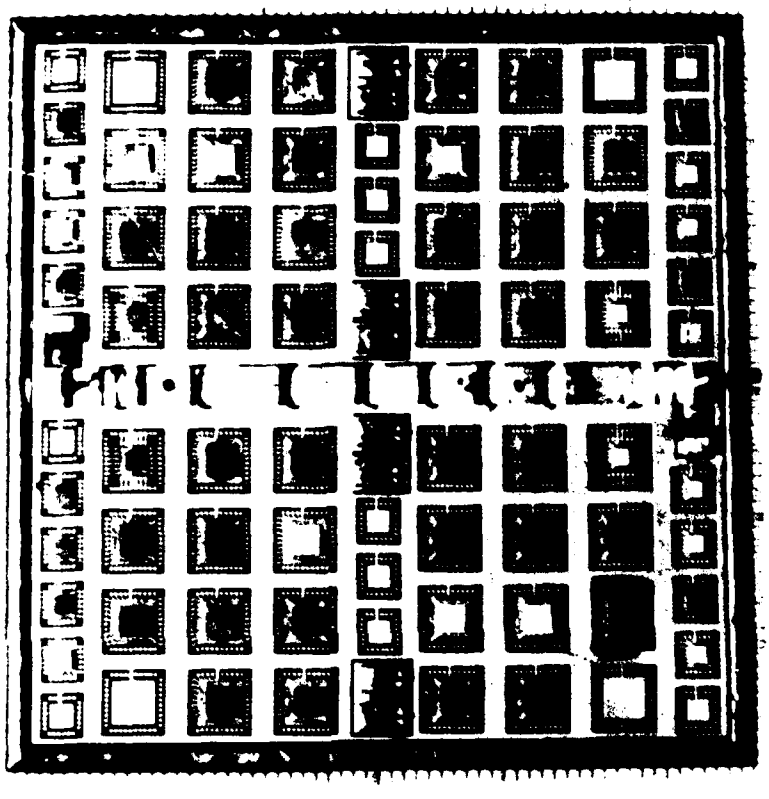

Figure 2. 3" x 3" multilevel substrate populated with flip TABed chips. The active surfaces of these chips are passivated with silicon nitride and protected with polyimide coatings.

dissipation of the assembly. The application of the epoxy can be done with a dispenser, screen printing or through the use of preforms.

Repair Procedures

When used in a multichip hybrid configuration, economic considerations require easy repair procedures for individual open connections or for chip removal and replacement. The following description pertains to TAB bonding to gold thick films on a ceramic substrate. These procedures, with modifications, can be used on copper thick films as well.

For individual open OLBs, a modified pulse tip bonder with a solid capillary bonding tip can be used. The lifted lead is captured between the bonding capillary and the OLB pad and a bond is made. A small Au-Sn preform may be used if the tin on the lead or pad appears oxidized.

For chip replacement, it is necessary to cut the leads from the OLB sites. A hot air gun can then be used to heat the chip and soften the epoxy. When the epoxy is soft, the chip can be pried loose. New epoxy can now be applied, partially cured, and chip replaced by TC bonding on OLB sites using TAB equipment. In this operation, the remains of the old leads at OLB sites need not be cleaned or removed. The leads of the new chip can be bonded over the old leads. This is in effect a tin-to-tin bond which yields lower pull strength (35-40 grams). If desired, however, the old leads can be removed by cutting horizontally at the OLB pad and re-exposing the gold thick film. This is a more desirable repair procedure as it yields 85 to 90 gram bond pull strength.

## FLIP TAB EVALUATION

A number of calculations and experimental tests were carried out to assess the reliability of using flip TAB process for assemblying chips in hybrids. Some of these tests are still in progress at this time. We are reporting here some recent results.

Analysis of Thermal Energy Dissipation

A thermal analysis is made on a worst case situation, i.e., assuming heat dissipation through the leads only (no heat conduction through the epoxy).

Allowing a $10^{o}C$ temperature difference between hybrid substrate and ambient, the power dissipation capacity W, in watts, can be calculated as follows:

$$W = \frac{T_C - T_S - 10}{R_C + R_l}$$

where $T_C$ = chip temperature, $^{o}C$
$T_S$ = substrate temperature, $^{o}C$

$R_c$ = thermal resistance of chip, $^oC$/watt
$R_l$ = thermal resistance of leads, $^oC$/watt

The thermal resistances can be estimated using the following formula:

$$R_c = C \frac{L_c}{K_{Si} A_c}$$

$$K_l = C \frac{L_l}{K_{Cu} A_l}$$

where C = conversion constant to SI units
$L_c$; $L_l$ = thermal path length for chip and lead, respectively
$K_{Si}$; $K_{Cu}$ = thermal conductivity of Si and Cu, respectively at anticipated device operating temperature
$A_c$; $A_l$ = cross-sectional area of chip and leads, respectively, for thermal flow

For a 0.080" x 0.080" x 0.010" chip with 14 copper leads (0.0014" x 0.0035" x 0.075") spaced evenly around the edge of the chip, by substituting the proper dimensional and materials constants into the above formulae, it was found that 500 mw of power can be dissipated. This figure is large enough to permit flip TABing of most logic chips.

Metallurgical Analyses of Flip TABed OLBs

To assess materials compatibility and long term reliability, investigations are undertaken to characterize the metallurgical interactions at the flip TABed OLBs. This report deals with tinned cold rolled copper leads bonded to gold thick film pads on alumina substrates.

To characterize alloy formation and elemental distribution in flip TABed OLBs, it is important first to identify chips with "sound" OLBs. For this purpose, lead pull tests were used to determine bond strength and mode of failure. Lead pulling was performed on a ETP* Model 201 Universal Bond Tester. Under our bonding conditions, typical pull breaking load is around 100 grams with fracture at point-of-pull.

Chips with sound OLBs were then examined in the as-bonded and as-aged conditions. Scanning Electron Microscopic (SEM) examination was made on sectioned specimens. Quantitative determination of tin content in gold was done with energy dispersive analyses of x-rays (EDAX) in conjunction with SEM based on a technique developed and reported previously (Ref. 8, 9).

Figure 3 shows a cross-section of an as-bonded flip TABed OLB at 1000X. Figure 4(a) at 2000X enlarges a portion of this OLB. Figure 4(b) is the corresponding x-ray density map for Sn. By monitoring the $Au_M/Sn_L$ x-ray count ratios at tin-rich regions at the lead/pad interface it is possible to assess the Au-Sn alloy composition. We found that in no case did the tin

* Engineered Technical Products, Inc., Somerville, NJ.

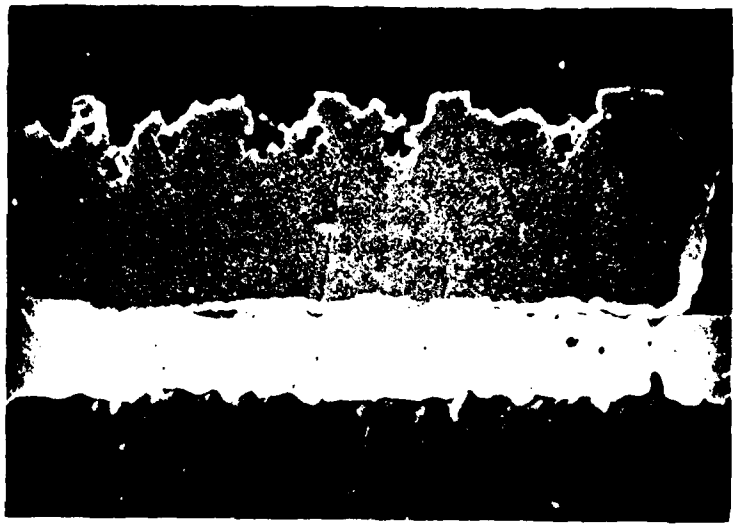

Figure 3. Cross-section of a flip TABed OLB, as bonded, 1000X.

Figure 4(a). Enlargement of a portion of Figure 3, 2000X.

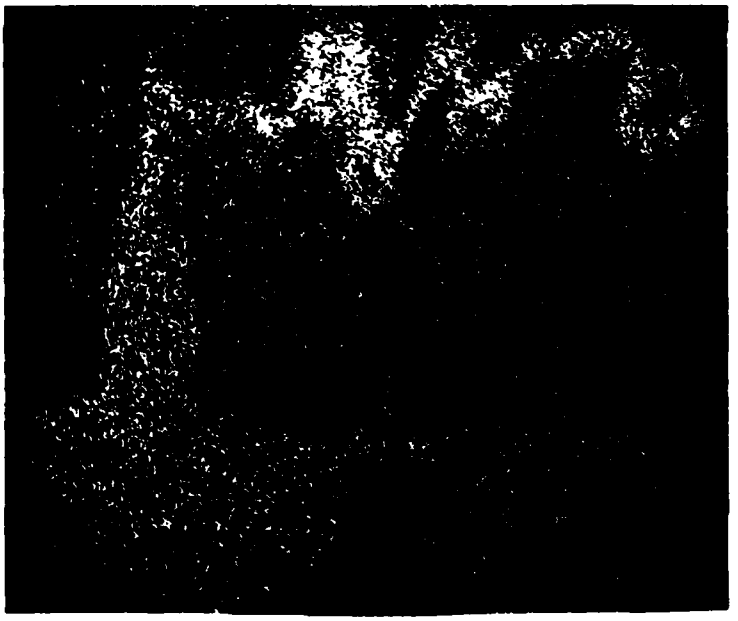

Figure 4(b). X-ray intensity map for Sn of area shown in Figure 4(a).

Figure 5(a). A portion of a flip TABed OLB, aged at 150° C 1000 hrs, 2000X.

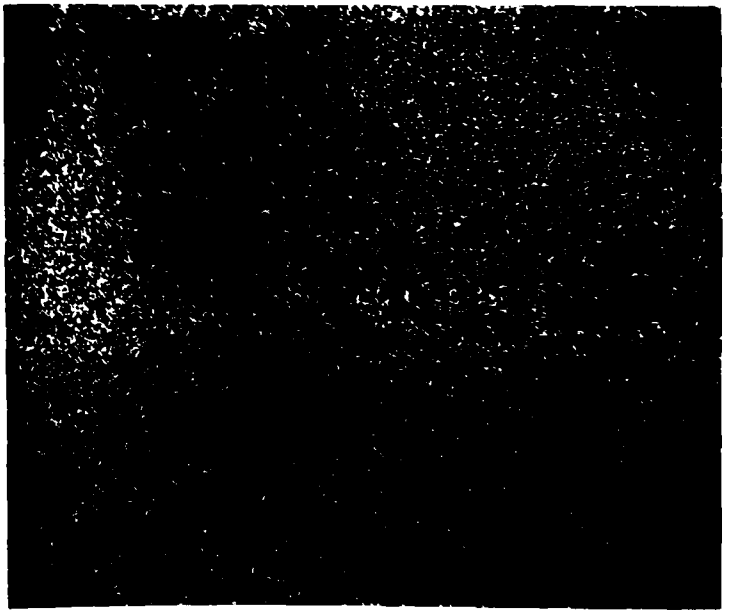

Figure 5(b). X-ray intensity map for Sn of area shown in Figure 5(a).

content exceed ∿ 29 wt% Sn. This means that the OLB formed consisted of alloys near the gold-rich Au-Sn eutectic region with good electrical and mechanical properties. Figure 5(a) is a cross-section of a flip TABed OLB similar to the one shown in Figure 4, but after aging for 1000 hours at 150°C. Figure 5(b) shows the tin distribution as expressed by Sn x-ray density map. One can visualize tin diffusion into the gold thick film qualitatively by comparing Figures 5(b) and 4(b). $Au_M/Sn_L$ x-ray count ratio at tin-rich areas indicated a tin content of ∿ 22 wt% of Sn in Au, a composition with nearly 100% Au-rich Au-Sn eutectic at equilibrium. This assures a metallurgically sound materials system at these bonds.

## ADVANTAGES AND LIMITATIONS OF FLIP TAB PROCESS

The obvious advantages of the flip TAB method of assembly are 1) the elimination of lead forming procedure and 2) the savings in substrate real estate. Using flip TAB, the chip thickness is not critical, and no back metallization is needed. Compared with solder reflow in forming OLBs, flip TAB can be automated more easily. The use of epoxy die attach actually encapsulates the inner lead bonds (ILB), thus strengthening the ILBs and preventing mechanical contact of leads with die edges (as shown in Figure 6).

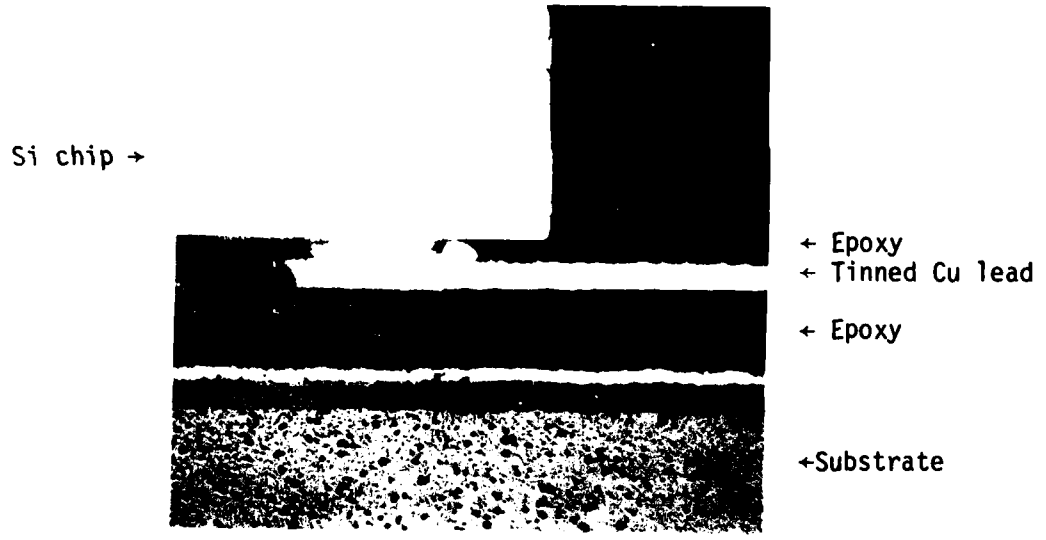


Figure 6. Details at an embedded ILB region, showing epoxy between die edge and lead.

No flux is required for certain OLB material systems (e.g., tinned copper leads bonding to gold thick film pads on ceramic substrates). In metal systems where pretinning of OLB pads is required (e.g., copper circuits on printed circuit boards) no solder dam is needed for strict height control of the solder.

Finally, with flip TAB, it is possible to stack one chip on top of another chip if needed and bonding to P.C. boards are possible.

Flip TAB process has a few limitations, namely, a limited number of chip replacements per site and limited heat dissipation with epoxy die attach. In certain instances, such as in pretinned OLB pads, reapplication of solder can allow a large number of repetitive repair operations to be performed on a given OLB site. The heat dissipation capability is adequate for current chips using the flip TAB assembly method, as in the hybrid shown in Figure 2. With higher powered chips (1.5 watts and up), epoxy die attach alone would not dissipate the heat generated for many MLS assemblies. For P.C. boards, there appear to be some very good alternatives through the use of heat sinks where required.

To summarize, advantages of flip TAB process are:

- No lead forming
- Denser chip population on hybrids possible
- Chip thickness not critical
- No back metal requirement
- Process can be automated
- Mechanical/environmental chip protection afforded
- Inner lead bonds strengthened
- No lead shorts to die
- Fluxless process
- No solder dams needed
- Chips can be stacked
- Chip can be bonded to P.C. boards
- Automatic testing and trouble-shooting of bonded device possible.

Limitations are:

- Limited number of chip changeouts per sites
- Limited heat dissipation capability due to epoxy die attach.

## CONCLUSIONS

Based on our experience with hybrid packages assembled with the flip TAB process and results obtained from various evaluations to date, flip TAB proves to be practical, economical and reliable. We feel that this contributes to improvements in TAB technology as a whole. Direct chip attachment onto printed circuit boards opens up an area hitherto not deemed feasible by TAB technology. Flip TAB process indeed broadens and improves TAB technology.

## ACKNOWLEDGMENT

The thermal analyses was performed by Mr. M. Hubbard.

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# HYBRID TAPE BONDING WITH FAST TURNAROUND, STANDARD CELL, REUSABLE TAPE

by

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## Introduction

Using the tape bonding approach to produce complex hybrids can be uneconomical if the number of hybrids to be produced is small, the number of different chip types to be bonded is large, the tape set up cost is high, and tape lead times excessive. Also, if each chip has a unique outerlead bonding pattern on the substrate, then each chip in the hybrid requires rather expensive dedicated tooling for inner lead bonding, excising, lead forming, and outer lead bonding. If the bumped chip approach is used, then another availability problem is encountered. These disadvantages can offset the inherent tape bonding advantages of high chip density on a substrate and the ability to pretest and characterize chips before they are outer lead bonded.

This paper describes a hybrid tape bonding approach where all of these disadvantages are overcome. The well known "bumped tape" approach is followed to solve the bumped chip availability problem. The procedure described for making artwork to etch strips of bumped tape requires about one day. Etched and plated solid copper tape can be produced in one more day. Chips bonded to these untestable frames are then bonded to a universal test frame which can be used over as many as seven times to accommodate the seven standard cell sizes described. Chips so mounted are then testable. Chip testing, excising, and outer lead bonding from these standard test frames is compatible with manual tooling as well as proposed automatic testers and bonders. Seven sets of hard tooling for bonding, excising, and forming will accommodate any chip up to .320 inch square in .040 inch increments. Seven standard substrate outer lead bonding patterns are presented. Cost comparisons between this approach and conventional tape are made. Size comparisons between the seven standard sizes and various ceramic leadless carriers are made.

## Description

Tape is made in-house with a fast turnaround technique on a standard cell format. The technique allows for part of the tape material to be reused thus reducing some costs. All of the different chip types are tested on the same universal probe tester. The chips are ultimately bonded to standard bonding patterns on a substrate.

## Cost Comparisons

The tape bonding approach to integrated circuit packaging has its own advantages and disadvantages. Applied to hybrids, the main advantages are the

ability to test and characterize the chips before they are mounted on a substrate and the ability to make all the nonstandard chip sizes standard by placing them in a test frame with a standard probe pad layout. The main disadvantages are the poor availability of bumped chips and tape. Tape procurement is usually associated with fairly high set up charges ($3,000 or more), long lead times (6 to 12 weeks), and moderate cost per frame ($.75 per frame in small quantities). What will be described is a technique for producing single layer bumped tape which is ultimately bonded to a universal test frame after it is bonded to a chip. The technique is characterized by very low set up costs (about one man-day per chip type), fast turnaround (about two days to begin laboratory tape production), and a moderate cost per frame (between $1.50 and $2.00 per frame on a laboratory basis).

The tape can be made bumped or unbumped for the same cost. To determine if the approach is appropriate for a given application one must analyze the cost based on how many chips need to be bonded for the particular hybrid run and how important the difference is in tape procurement lead time. In the design of military hybrids it is often the case that the total run of a given hybrid is measured in the hundreds rather than the thousands or tens of thousands. If future trends require more circuitry to be placed in a fixed volume aboard an aircraft, then complex hybrids will be required to meet the volume restraints. Increased complexity requires more thorough testing and characterizing at the chip level to minimize the rework due to chip failure at final assembly. When designing a complex hybrid with many chip types, it is necessary to have a fast tape procurement capability in order to maintain a satisfactory completion schedule. Making the first breadboard hybrid will probably require making small changes in the various tape artworks. It would not be feasible to wait the six or twelve weeks lead time every time a change was needed. Figure 1 shows some cost information indicating the total cost of the frames as a function of the total number needed. The number of frames needed and the lead time required will determine which tape procurement approach is best. A typical break even point for vendor procurement and in-house procurement is about 3000 frames.

## Single Layer Tape Fabrication

The approach used to produce the single layer tape is to spray etch copper foil from both sides in order to form the leads, bumps, sprocket holes, and tape edges in the 35 mm format. The foil must first be protected with photoresist on both sides which is imaged with the appropriate artwork. The artwork used consists of a pair of step and repeat images making up side 1 and side 2 where each feature on side 1 must register with the corresponding feature on side 2 to within several tenths of a mil. The artwork producing cycle begins by taking the actual chip to be bonded and measuring the locations of the bonding pads to produce a 100 to 1 drawing. The bonding pad locations will be represented by artwork spots which are 100 times the size of the photoresist spots which will define the bonding bumps (if bumps are used). This 100 to 1 artwork is then photographically reduced to 25 to 1, and the lead layout is made by hand at this scale. This chip will ultimately fit into one of seven standard cell sizes shown in figure 2. The figure shows

the maximum size a chip may have in a given cell and the locations of the outer lead bonding pads on the substrate. Once the cell size is selected, based on chip size and lead count, a standard format is used to make the lead layout. After this layout is complete it is placed in a 35 mm frame at the 25 to 1 size to form side 1. Side 2 is similar but has the bonding bump spots instead of the lead outlines. These two frames are photographically reduced to 1 to 1 and then step and repeated twenty times to form two strings of images as shown in figure 3. Since they are stepped together, all of the images on side 1 will register with the corresponding images on side 2 to a high degree of accuracy. This artwork can be turned around in less than one day. The final artwork used to image the photoresist is a contact print of the step and repeat master, so many copies of this can be produced at low cost. This final artwork is cut down the middle between the two strings of images and glued together, emulsion facing emulsion, to form an envelope with the frames of side 1 facing the frames of side 2. No expensive alignment is needed. This artwork production cycle represents the total setup requirement for a particular chip type.

Standard Test Frame Concept

After the copper foil is etched using the above described artwork, it can be gold plated and fed into an inner lead bonding machine. Once the chips are bonded to this tape, they are not testable since all leads are shorted as shown in figure 4. In order to make them testable they are bonded to a universal test frame shown in figure 5. The universal test frame is a piece of 35 mm wide polyimide which is four sprocket holes long (.748 inch). It has an array of 64 probe pads which are connected to conductor lines which run to the edges of a square hole in the center of the frame. These copper lines are plated with electroless tin, hence they do not need to be temporarily connected together for plating. Without any temporary connecting lines there is more room for probe pads and chip leads. The leads bonded to the chip are gold plated so that when the single layer tape, with chip, is aligned and bonded to the test frame a gold/tin solder joint is formed between these two copper foils. With pressure still being applied to the gold/tin interface by a manual bonder, the excess gold plated foil is separated by hand thus making the chip testable on the frame. The labor cost required to place the chip on the test frame on a laboratory manual scale and the cost of the polyimide test frame itself are included in the cost information shown in figure 1. The universal test frame is the part of this approach which is reusable.

This one style of test frame can be used for any chip having up to 64 bonding pads and measuring up to .320 inch square. The test frame tape is purchased with a .240 inch (6 mm) hole punched in the center which will accommodate the smallest of seven standard chip cell sizes. The smallest chip size can be a maximum of .080 inch square and have a maximum of four leads (bonding pads) per side. Each standard maximum chip size is .040 inch larger per side than the previous size and has two more leads per side than the previous size. Therefore, the standard chip maximum sizes are: .080, .120, .160, .200, .240, .280, and .320 inch square and they have 4, 6, 8, 10, 12, 14, and 16 leads per side, respectively. It is necessary to have a set of

eight square punches which can be used to excise chips and punch square holes in the center of the universal test frame. These punch sizes are .200, .240, .280, .320, .360, .400, .440 and .480 inch square. Each punch, except the two smallest ones and the largest, will serve two purposes: to excise a chip after its leads are bonded to the test frame, and to enlarge an existing square hole in the test frame thus allowing it to be used over again for the next larger size chip. By enlarging the hole the short stubs left by the last chip are removed. Thus, none of the gold/tin metallurgy stays with the chip. This is illustrated in figure 6. The two smallest punches (.200 and .240) will only be used for excising a chip bonded to .240 or .280 hole and the largest punch can only be used to provide a .480 hole whose chip will ultimately be excised with the .440 punch.

Testing on Standard Test Frames

Once the chip is mounted on the test frame it can be handled conveniently by placing it in a slide frame carrier such as the one shown in figure 5. With a universal probe pad array there would be only one array of probe pins required in the probing test machine. The adoption of a standard probe pattern by the hybrid industry would promote the exchange of mounted chip types. This standardization of probe pad locations would also reduce the number of fixture styles required for burning in chips mounted on the test frames.

Excise Form and Place

The choice of .040 inch as the increment between the standard sizes is based on having 10 mil lines and spaces on the upper (bonding) layer of the substrate. Using lines and spaces less than 10 mils would not reduce the cell sizes since they are determined more by how close to the chip the leads can be formed. The family of standard cells is laid out with the outer edges of the substrate bonding pads located .040 away from the edge of the largest chip that will fit in the particular standard cell. When a chip is excised, the leads overhang the maximum chip size by 60 mils, and when the leads are formed, they are drawn in by 20 mils. The thickness of 20 mils is probably the maximum thickness that a chip plus its mounting adhesive would have. If the chip plus adhesive were less than 20 mils this would result in more lead arching away from the chip when it is pushed down into the adhesive. Figure 6 shows a cross section of the dimensional relationships of a chip mounted to a test frame, the before and after lead forming shape of the leads, and the substrate bonding pad and via locations. The center-to-center spacing of the bonding pads shown in figure 2 is 20 mils, and the nominal size of the bonding pads is 10 mils by 20 mils. Each succeeding size has two more lines and spaces per side so each side grows by 40 mils. The size of each standard cell (area taken up on a substrate) is 100 mils larger than the chip sizes, hence they vary from 180 mils square to 420 mils square. However, if a chip has bonding pads on two opposite sides and not on the other two sides, then a modified outer lead bonding pad layout can be used. Figure 7 shows an integrated circuit chip package where high density is achieved by printing only the outer lead bonding pads which are needed, allowing the chips to be placed closer together than would otherwise be

possible if all of the standard bonding pads were printed. This extra degree of flexibility does not affect, to a signfiicant degree, the amount and kind of hard tooling necessary to bond the standard cell family. The same excising and lead forming tooling is used. The only dedicated tool is the outer lead bonding tip which must have only two bonding rails instead of four.

## Size Comparison with Leadless Chip Carriers

Figure 8 is a graph showing the area efficiency of the TAB standard cells and the leadless carrier packages. It was assumed that there would be 50 mils clearance between adjacent leadless carrier packages. The two leadless carrier families are the 40 mil center and 50 mil center standard configurations developed for the Air Force by RCA and Hughes respectively.[1,2] The area efficiency is defined as the ratio of chip area to cell area; it is the percentage of the substrate area actually occupied by chips. These values are shown for each pin count available in the three approaches.

## Conclusions

It is possible to generate bumped tape artwork with photographic equipment consisting of a reduction camera and a contact print step and repeat machine. This artwork can be produced complete in about one day. This constitutes the entire setup expense for etching short strips of single layer tape. The alignment of a strip of 20 frames of side 1 and 20 frames of side 2 can be done manually with sufficient enough accuracy that bumps and leads register to several tenths of a mil. No special alignment equipment is required. After bonding chips to this single layer tape they can be bonded to a universal test frame making a thermo compression type of gold/tin bond. These test frames can be mounted in 2-inch by 2-inch slides and tested with automatic handling equipment. After chip excising, the frames can be punched to successively larger sizes and reused as many as six more times. The substrate area consumed by the TAB standard cells is about half that consumed by leadless chip carriers.

## Recommendations

The approach presented can be used for preliminary production of bumped tape which can be used until designs are finalized. Tape could be ordered from suppliers for chips with high enough usage to make it economical and long lead times would have minimal impact. TAB standardization should be implemented by the Hybrid Industry for several reasons: a standard probe pattern configuration would promote the exchange of prebonded chips between hybrid manufacturers and would allow the purchaser to conveniently perform his own specific chip tests. A family of standard outer lead bond targets would allow for convenient use of these available tape bonded chips with a minimum of dedicated tooling.

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[2]Report AFML-511-7-4, Manufacturing Technology for Hermetic Chip Carrier Packaging, R. H. Zeien and T. R. Mayhew, RCA Corp.

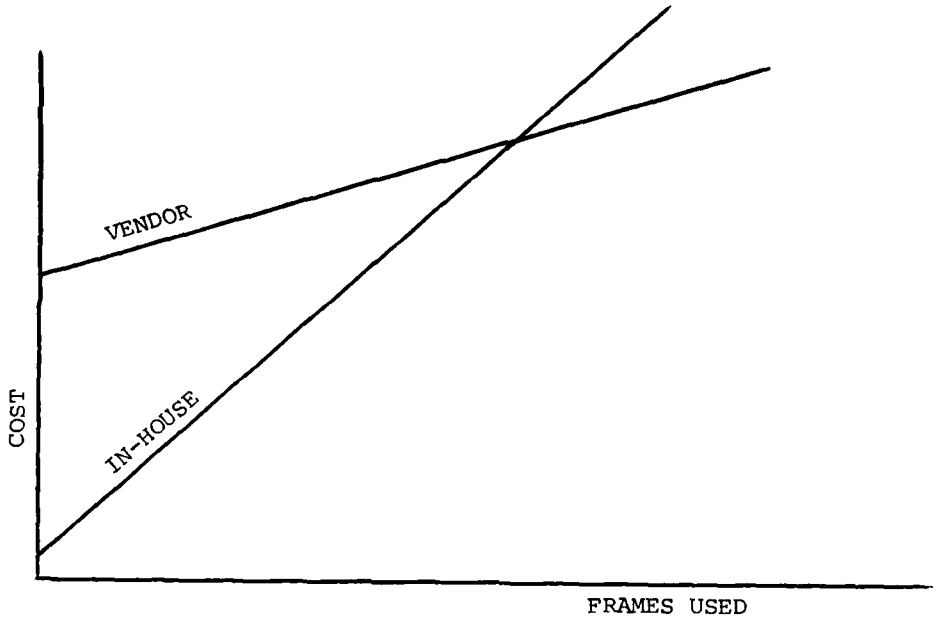
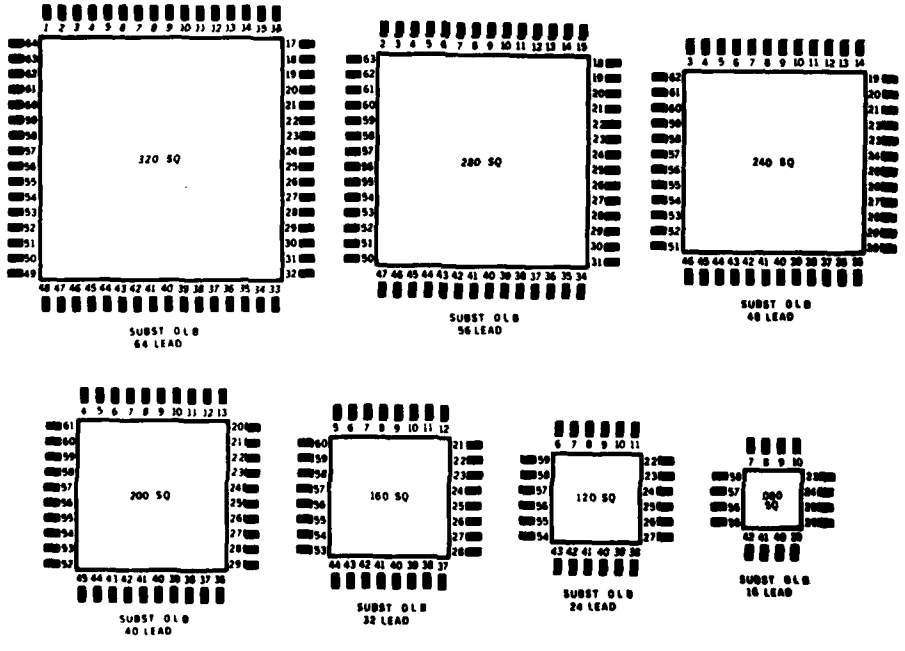



Figure 1. Total Cost of TAB Frames Vs Number of Frames Used




**T.A.B. STD. CELL FAMILY**

Figure 2. Standard Cell Sizes Showing Outer Lead Bonding Pads

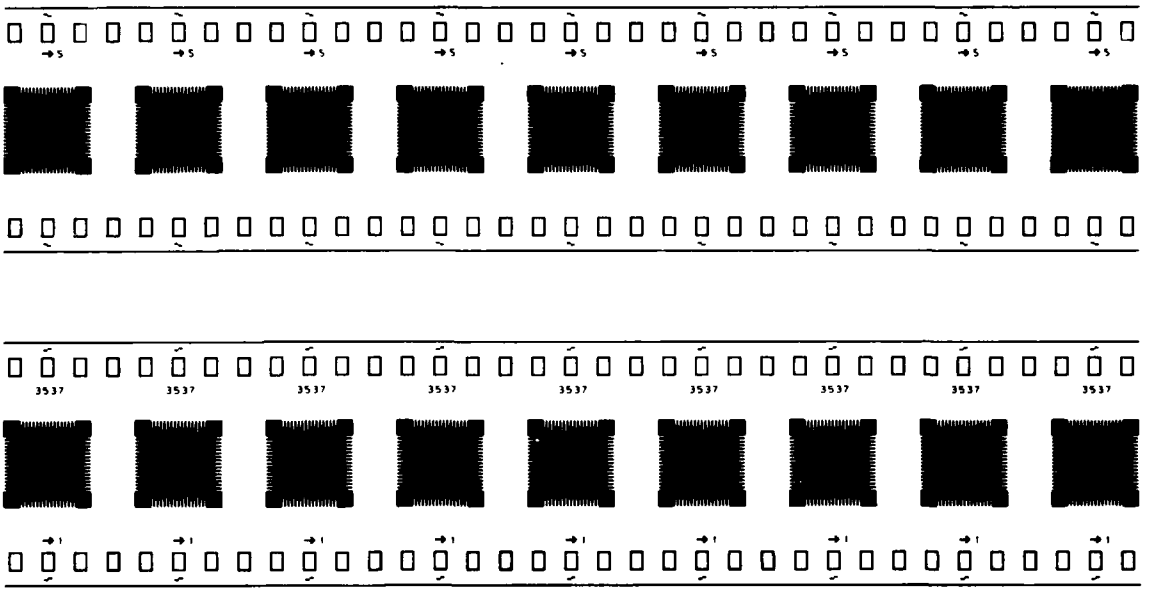



Figure 3. Strings of Images

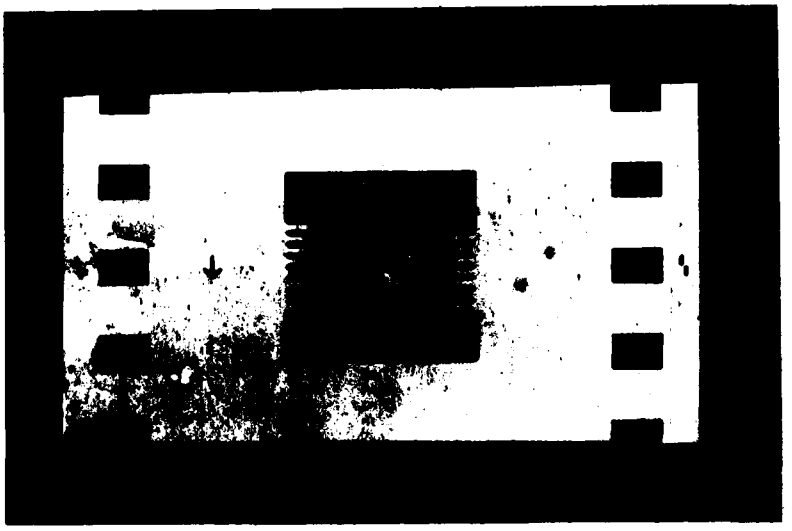


Figure 4. Chip Bonded to Bumped Single Layer Frame

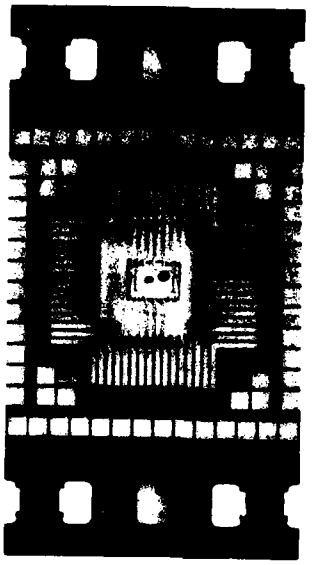


Figure 5. Standard Test Frame Mounted in a 2 x 2 Slide

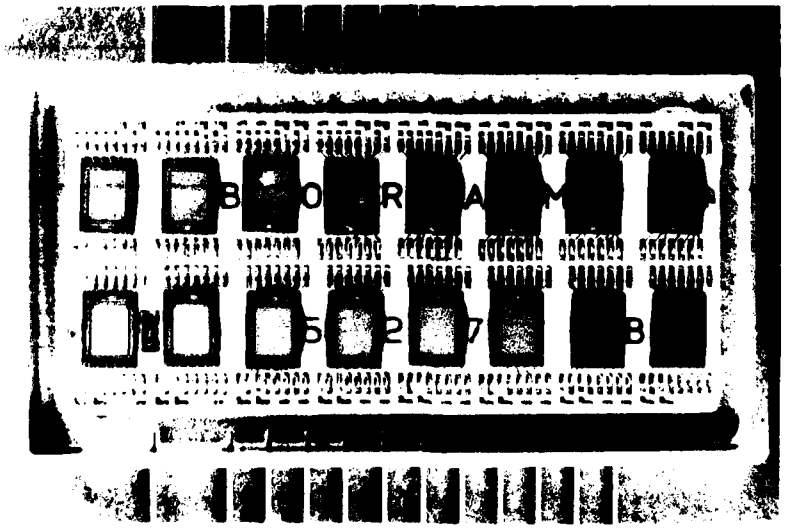


Figure 7. Tape Bonded Hybrid Package

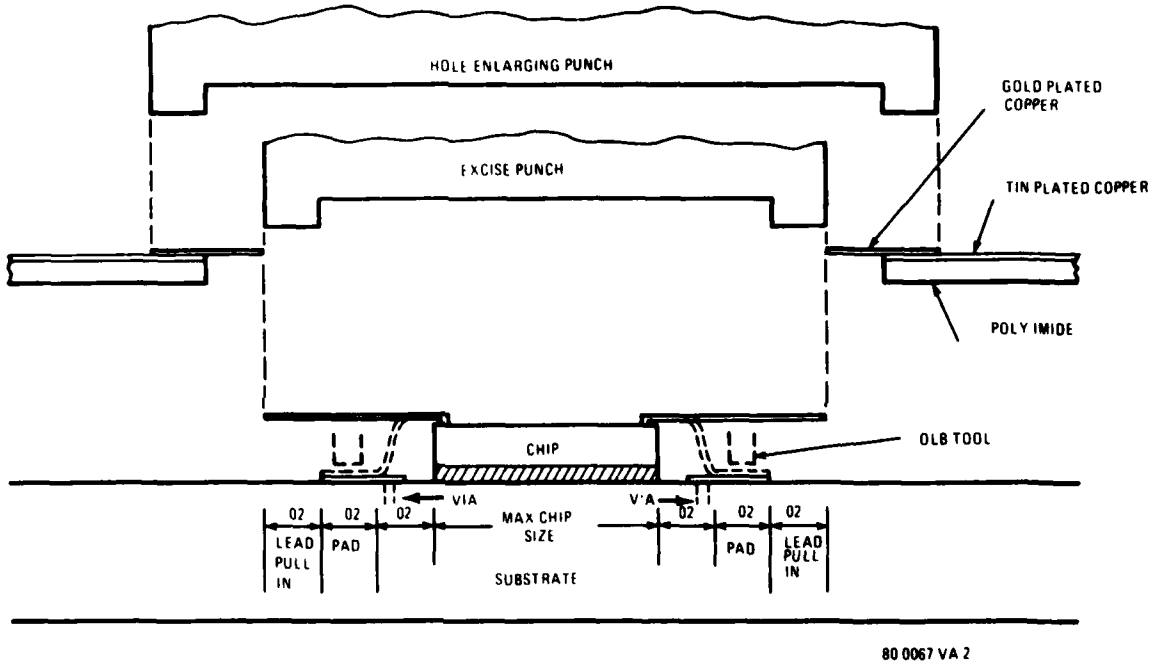



Figure 6. Chip Mounted to Test Frame With Substrate Bonding Pad and Via Locations

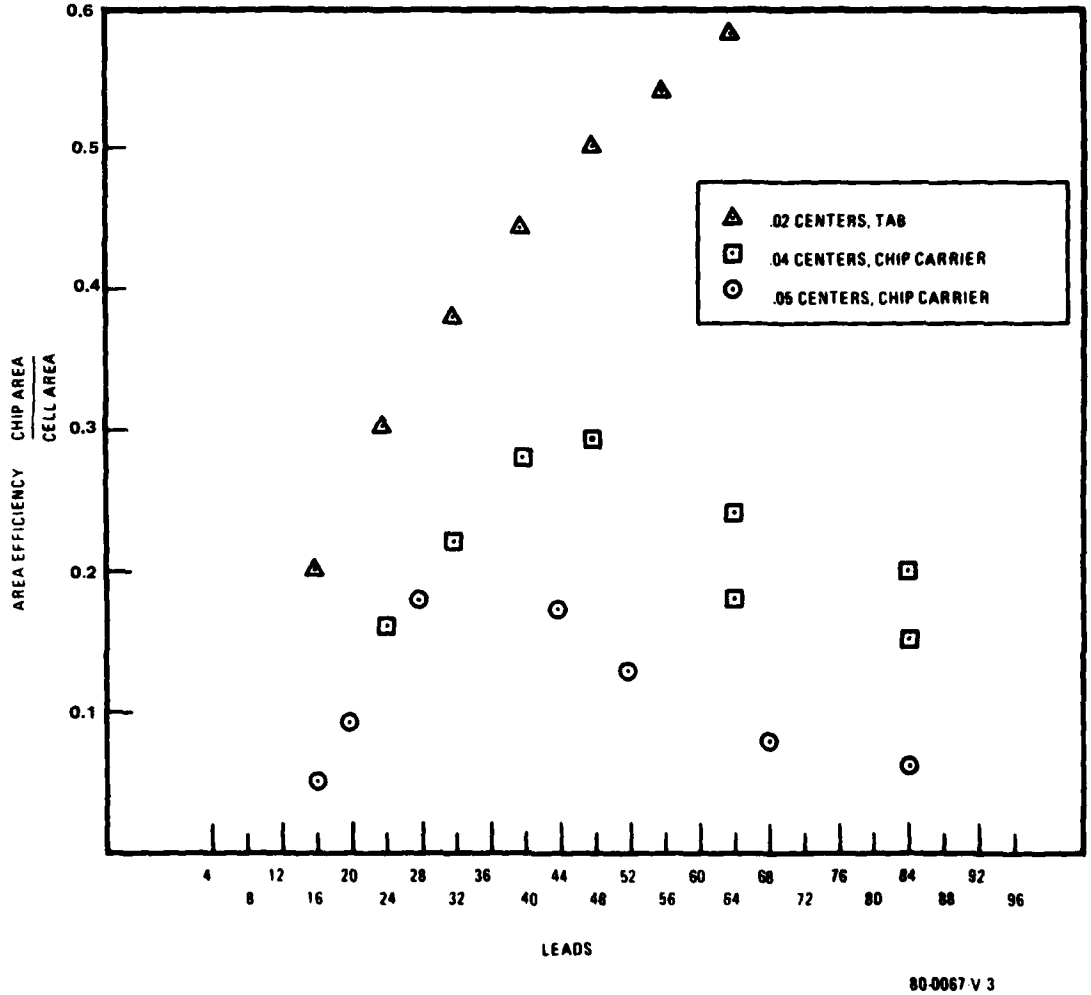



Figure 8. Area Efficiency Vs Lead Count for TAB and Chip Carrier Packaging

# MODULAR TECHNIQUES FOR THE MANUFACTURE OF LARGE TACTICAL DISPLAY SYSTEMS

BY

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## ABSTRACT

Technology surveys, based upon requirements for implementing a large, flat-panel display system, concluded that a modular array of light-emitting diodes (LEDs), was the optimum technology whereby specified display requirements could be satisfied.

The feasibility of such a display was demonstrated by positioning double-doped diodes on a ceramic substrate with a manual pick and place die bonder and using a conductive epoxy as an adhesive. The drive electronics were produced by standard hybrid techniques and were mounted on a printed circuit board attached to the backside of the display surface. While demonstrating product and system feasibility, this approach also identified as cost drivers the LEDs and module interconnect mechanism. In addition, power dissipation, which resulted from the utilization of the Transistor-Transistor Logic ($T^2L$) devices and discrete transistors, was also identified as a system concern.

Further research revealed that single-color (red or green) LEDs emitted the same three colors that the double-doped devices provided for a fraction of the cost, were much more efficient as a light emitter, and thereby required less power. This greater efficiency, coupled with the use of CMOS devices, reduced greatly the power requirement and allowed the mounting of the drive and memory electronics to the back of the LED surface, thus eliminating the connector requirement. Interest now focused on volume producibility and display system surface flatness.

Present efforts include the demonstration of automated means of module production, the investigation and evaluation of leadless hermetic packaging and ring frame enclosure of the drive electronics, low-cost alternatives to gold in plating processes for conductors, and automated testing of modules.

## INTRODUCTION

The critical objective for the tactical map utilized by combat forces is the presentation of timely combat situations for facilitation of command and control decisions. The primary goal, therefore, of a large tactical display system is the integration of a tactical paper map and an electronics display that can provide both the timely presentation and an interactive command and control vehicle for this objective.

In 1969, the US Army Electronics Command, Fort Monmouth, contracted with Litton Data Systems for a study to determine the optimum technology for implementing a large, flat-panel display that would meet these critical and timely objectives.

Initial requirements identified by the Army specified the integration of display and standard Army maps. The technology was to allow the production of a display system that was up to four-feet square at a depth of no greater than six inches. The display was to have the ability to display graphics and alphanumerics in any one of three colors. The graphic characteristics of the display were to be such that on a 1:50,000 scale map the error in graphic map annotations by the display would be no greater than 80 meters.

The study of promising technology indicated that a modular array of light emitting diodes (LEDs) was the optimum technology whereby the display system requirements might be realized. This selection of LEDs was made in part because their technology was maturing and had reached an advanced stage, and also because the solid-state characteristics of the LED were compatible with existing and projected integrated solid-state technology.

## MODULAR DISPLAY FEASIBILITY

Proceeding to demonstrate the feasibility of a modular display concept, Litton Data Systems continued, again under contract to the US Army Electronics Command, to develop a display surface approximately six inches square. The module display surface chosen was nominally 0.72 x 1.44 inches with 16 x 32 display elements on 0.045 inch centers.

The modular approach to a display surface dictated the requirement for modular four-edge abuttability. This allowed the spacing between LEDs to remain the same from one module to the next, as is the spacing between adjacent LEDs within a module. This is illustrated in Figure 1.

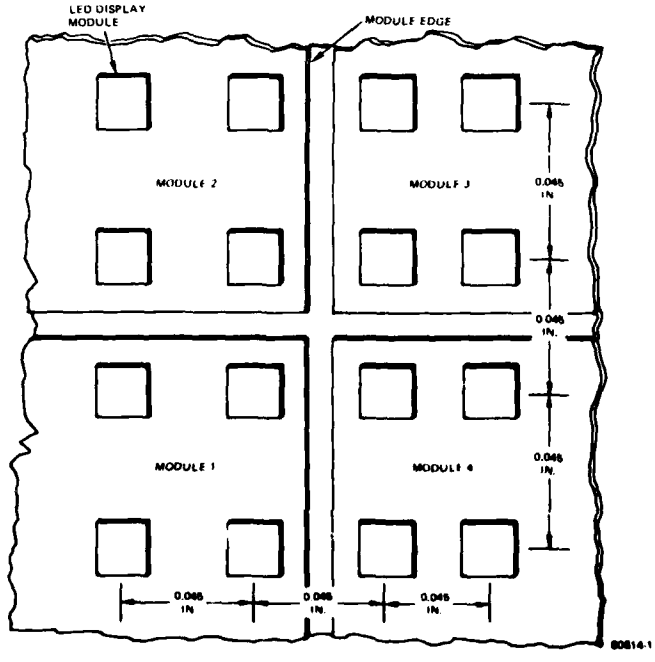


Figure 1

The LEDs chosen for the module were double-doped die and displayed the colors red, green, or amber when the appropriate current was applied.

Upon completion of testing the die for brightness, color, and uniformity of parameters, the LEDs were mounted with an operator-assisted pick and place die bonder, using a silver-filled epoxy as the adhesive. After the LEDs were mounted to a cofired multilayer substrate and wire-bond interconnected, as shown in Figure 2, a clear epoxy resin was molded over the surface to protect the LEDs and wires.

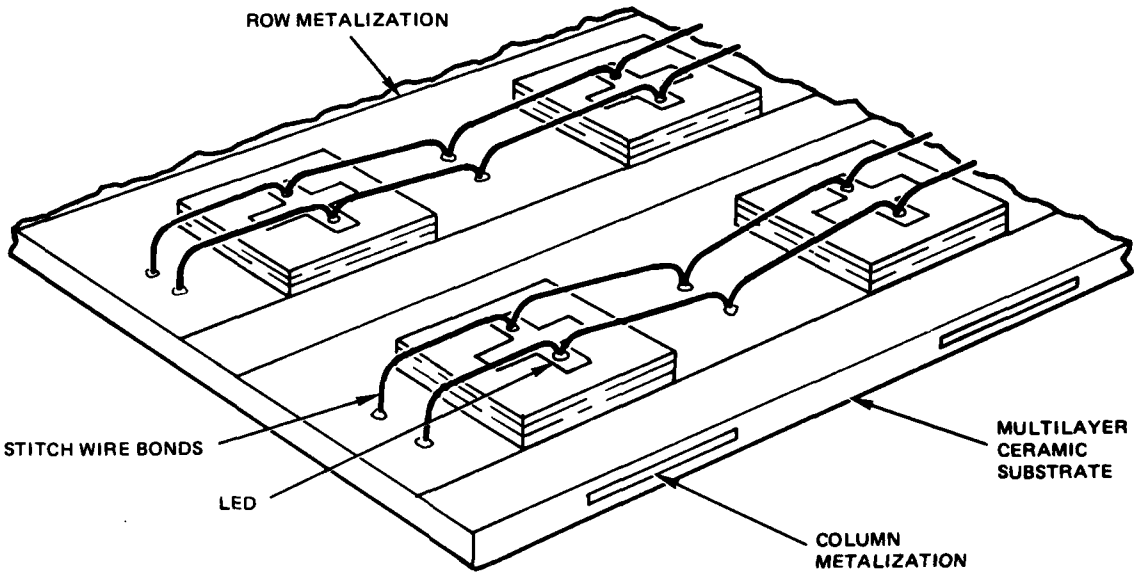


Figure 2

The display row drive, column sink, and memory circuits were produced by standard hybrid circuit techniques in axial lead flat packs. These, in turn, were mounted to a printed circuit board (PCB). Input to the module was accomplished by means of printed connections that mated with a female connector. The outputs from the hybrid electronics interfaced to the display surface by means of a connector mounted at the opposite end of the PCB and allowed the display surface to be connected. The completed assembly is shown in Figure 3.

A fabricated panel utilizing 32 of these modules successfully demonstrated the feasibility of LEDs as an integral component of large panel multicolor display systems.

## PROTOTYPE MODEL

Parameters such as cost, LED efficiency, and module operational efficiency were the key elements for study in the earliest prototype module effort. A series of experiments identified that single-color red and green LEDs, when placed as a red-green pair on a display surface, could be electrically stimulated to give the same three-color effect as the double-doped devices,

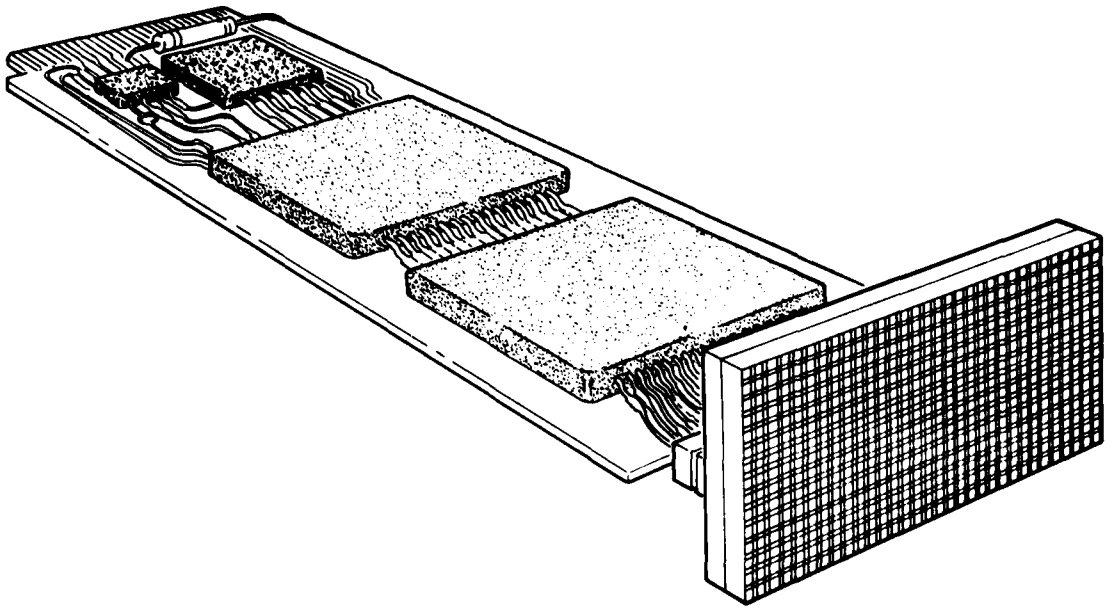


Figure 3 .

provided that the viewing distance was greater than 18 inches. The single-color LEDs were much more efficient than the double-doped devices and also much less expensive. Thus, this greater efficiency, coupled with the use of MOS devices in the addressing circuitry, provided a measure of assault on the parameters viewed as key in directing this technology toward a usable application.

Thermal studies indicated that the achievement of greater efficiency would allow the display and drive to be placed back to back in a single package, thereby eliminating the connector and drastically reducing display panel depth. Further mechanical and electrical considerations pointed to a nominal module size of 1.44 inches by 2.88 inches with 32 x 64 red-green LED pairs on 0.045 inch centers.

The prototype module was fabricated in three basic sections. The row drivers were on a thick film substrate with 32 red outputs and 32 green outputs along one edge, and the necessary inputs via blade pins along the opposite edge, as illustrated in Figure 4. Column sinks were made in a similar fashion.

The LEDs were mounted on a third substrate, which had 64 column strips and 64 (32 each, red and green) row connections on the front surface. These were connected through vias to the rear of the substrate. Traces ran from the vias to the center portion of the back side of this substrate.

LED anodes were mounted on the column strips which formed the Y axis of the display face. They were mounted as 2048 red-green pairs. Again, the die mounting was done with a manual pick and place die bonder, using a silver-filled conductive epoxy as the adhesive.

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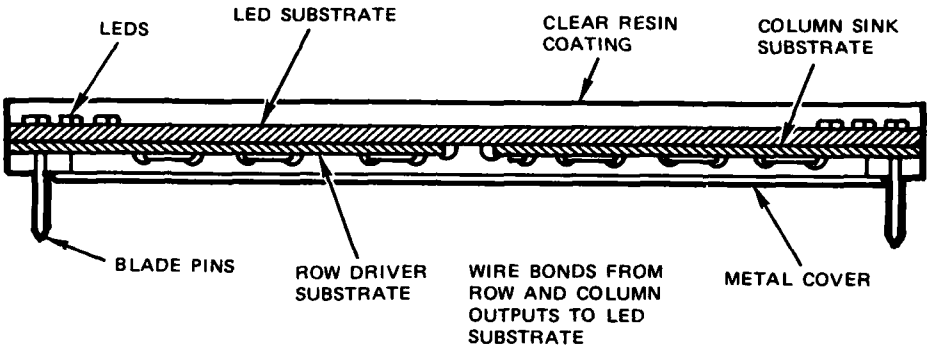
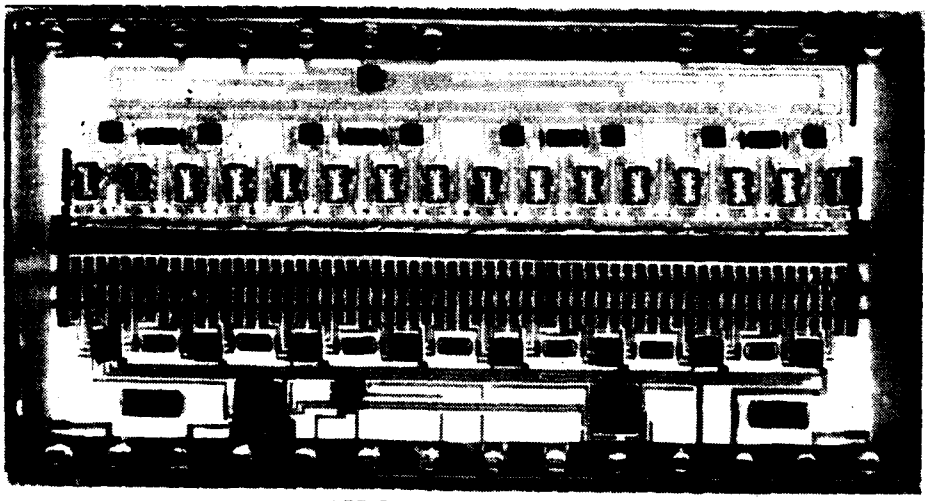
LED DISPLAY–FRONT VIEW



NEG. 641-2CN

LED DISPLAY–REAR VIEW

80614-4

Figure 4

The drive circuits, the array and ring frame that provided a support for a protective cover over the drive circuits, addressing, and memory were adhesive-bonded in an alignment fixture. After the wiring of the drive circuits to the LED array was accomplished and tested the metal protective cover was mounted over the electronic hybrid. A sketch of the module is shown in Figure 5.

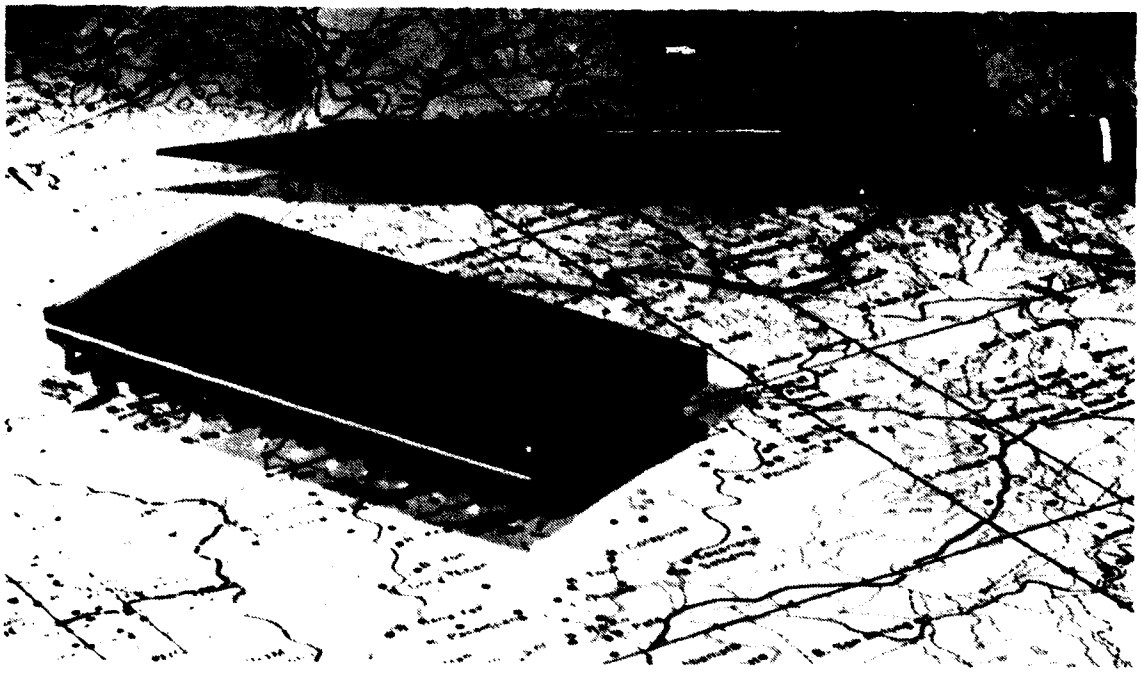


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Figure 5

The blade pins served as both the mechanical and electrical connections to the panel. Each module thus was a complete system, with the LED array, drive, and recirculating refresh memory integrated into one hybrid package. Thus, the modules could be used singly or multiply for construction of panels in any size configuration. Depth, however, would be of less than two inches.

## PRODUCTION MODEL DEVELOPMENT

The LED module is the most important component of a tactical display system and also the largest cost driver. Therefore, in June 1979, the U.S. Army contracted Litton to undertake a producibility study. This study required the identifying and subcontracting of two highly effective production hybrid facilities capable of engineering the display module and providing Litton with several pre-production samples, as well as a firm commitment to meet program cost goals.

Care was taken in defining the requirements and detailing the module envelope to allow the subcontractor as much freedom as possible in defining the hybrid techniques for module fabrication. The electrical block diagram shown in Figure 6 illustrates the basic elements

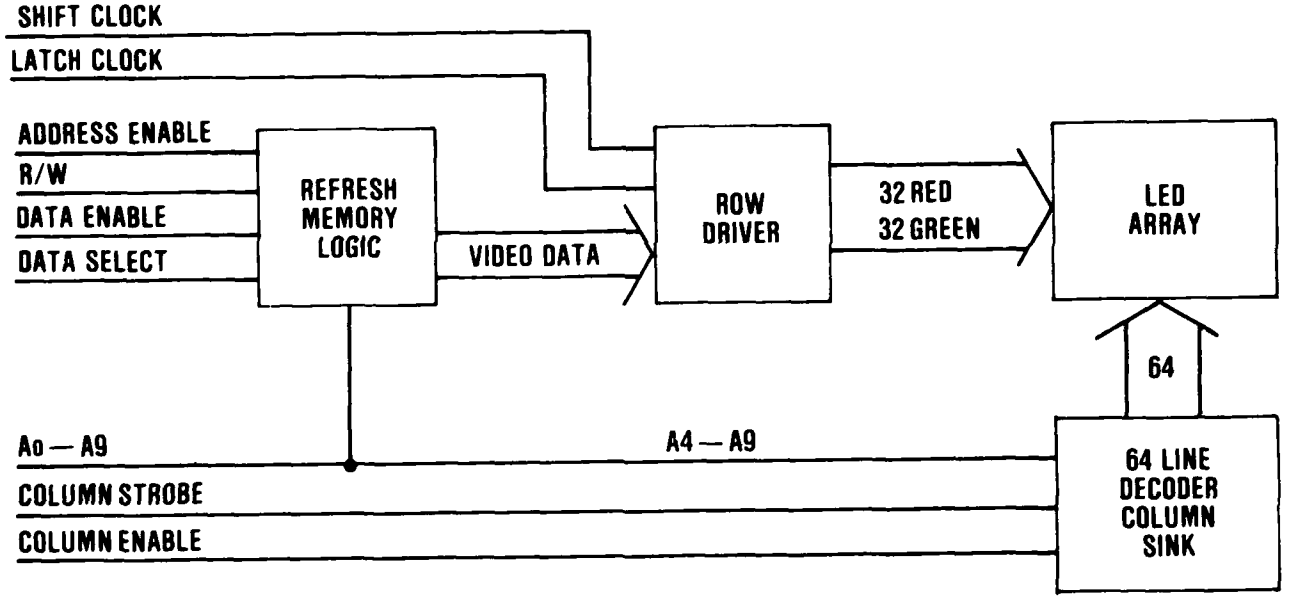
SHIFT CLOCK
LATCH CLOCK
ADDRESS ENABLE
R/W
DATA ENABLE
DATA SELECT
REFRESH MEMORY LOGIC
VIDEO DATA
ROW DRIVER
32 RED
32 GREEN
LED ARRAY
64
A0 — A9
A4 — A9
COLUMN STROBE
COLUMN ENABLE
64 LINE DECODER COLUMN SINK
80614-6

Figure 6

which are packaged in a display module. The electrical operation of the module is quite simple; when information is written into the display, a copy of this information is placed in memory. Each time the displayed information must be refreshed the memory performs this function, thereby not requiring regeneration of information. Whenever information is rewritten, or refreshed, the LED array is addressed in an "X" and "Y" axis with a row driver (the "X" axis) and a column sink (the "Y" axis). This selectively lights the LEDs and displays information.

The hybrid manufacturing approach to a cost-effective LED module shown in Figure 7 separates the LED surface from the electronics and provides separate assemblies that are connected by two short ribbon cables. The module in turn is connected to the system by a short ribbon cable and connector.

The LED surface is produced with an aluminum oxide ($AL_2O_3$) substrate that is ground on six sides to assure both flatness of the LED surface and accuracy of side dimensions. It is then printed using thick film pastes. A screening of conductive epoxy is placed on the surface of the substrate so that gallium arsenide (red LEDs) and gallium phosphide (green LEDs) diodes may be placed automatically with high precision pick and place machines. The epoxy that holds the 4096 LEDs is then cured and the anodes of the LEDs are wire bonded to the surface with automatic wire bonders. After preliminary testing, a reflective overlay which directs the light output is attached and a clear optical epoxy is used to encapsulate the display surface. Electrical testing, as well as grinding and polishing of the surface, are performed, and the completed surface is then cleaned and tested prior to the attachment of flat cables. This makes the front surface ready for final assembly and testing. This process is shown in Figure 8.

The electronics assembly is produced from a family of substrate subassemblies. These subassemblies consist of two aluminum oxide mother boards, which are joined together after four individual chip carriers with hermetic sealing lids are assembled, tested, and placed on the mother boards, as shown previously in Figure 7. A diagram of this process is shown in Figure 9.

The main objective of the separation of electronics into functional packages is to increase throughput of product by allowing easier fault detection and problem isolation during the manufacturing process. A second objective of this technique allows the rework of smaller areas while lowering the risk of damage to neighboring components of other functions.

This approach is being pursued presently and is showing signs of potentially minimizing technical risk and providing the ability to upgrade a particular block function of circuitry without impacting large layout areas.

Figure 10 depicts a second hybrid manufacturing approach to the display module. The figure indicates that the display surface is of the same basic configuration. The basic difference in approach is the manufacturing of the electronics hybrids.

The philosophy of this approach is that the basic functions should be separated. This functional separation may be utilized to great advantage by using available area to optimize heat dissipation to free air, and additionally may decrease the complexity of requirements for a given hybrid substrate fabrication. It will also make interconnection of functions simple and minimize line resistances. The column sink and the row driver/memory hybrid are fabricated

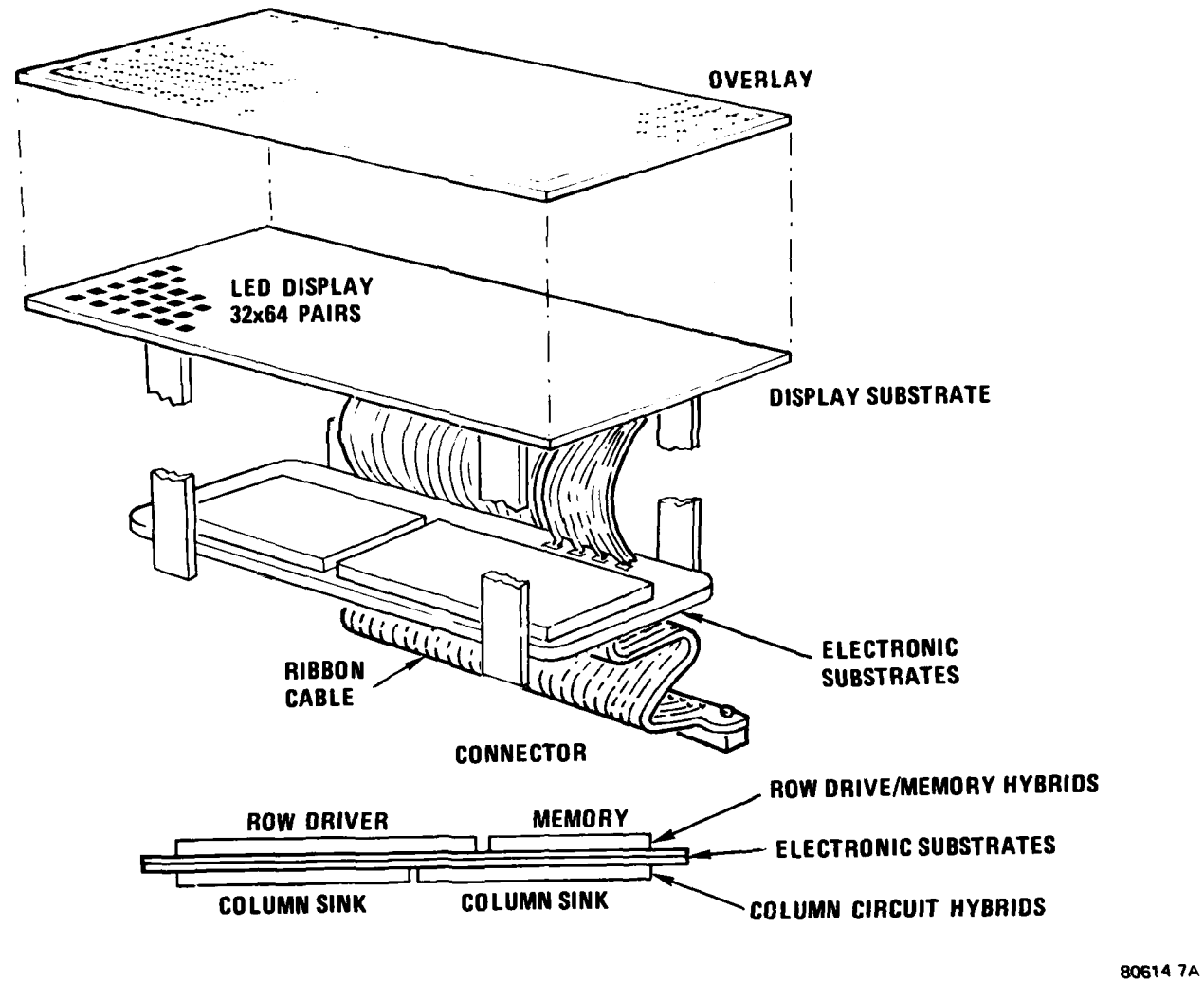
OVERLAY
LED DISPLAY
32x64 PAIRS
DISPLAY SUBSTRATE
ELECTRONIC
SUBSTRATES
RIBBON
CABLE
CONNECTOR
ROW DRIVE/MEMORY HYBRIDS
ROW DRIVER
MEMORY
ELECTRONIC SUBSTRATES
COLUMN SINK
COLUMN SINK
COLUMN CIRCUIT HYBRIDS
80614 7A

Figure 7

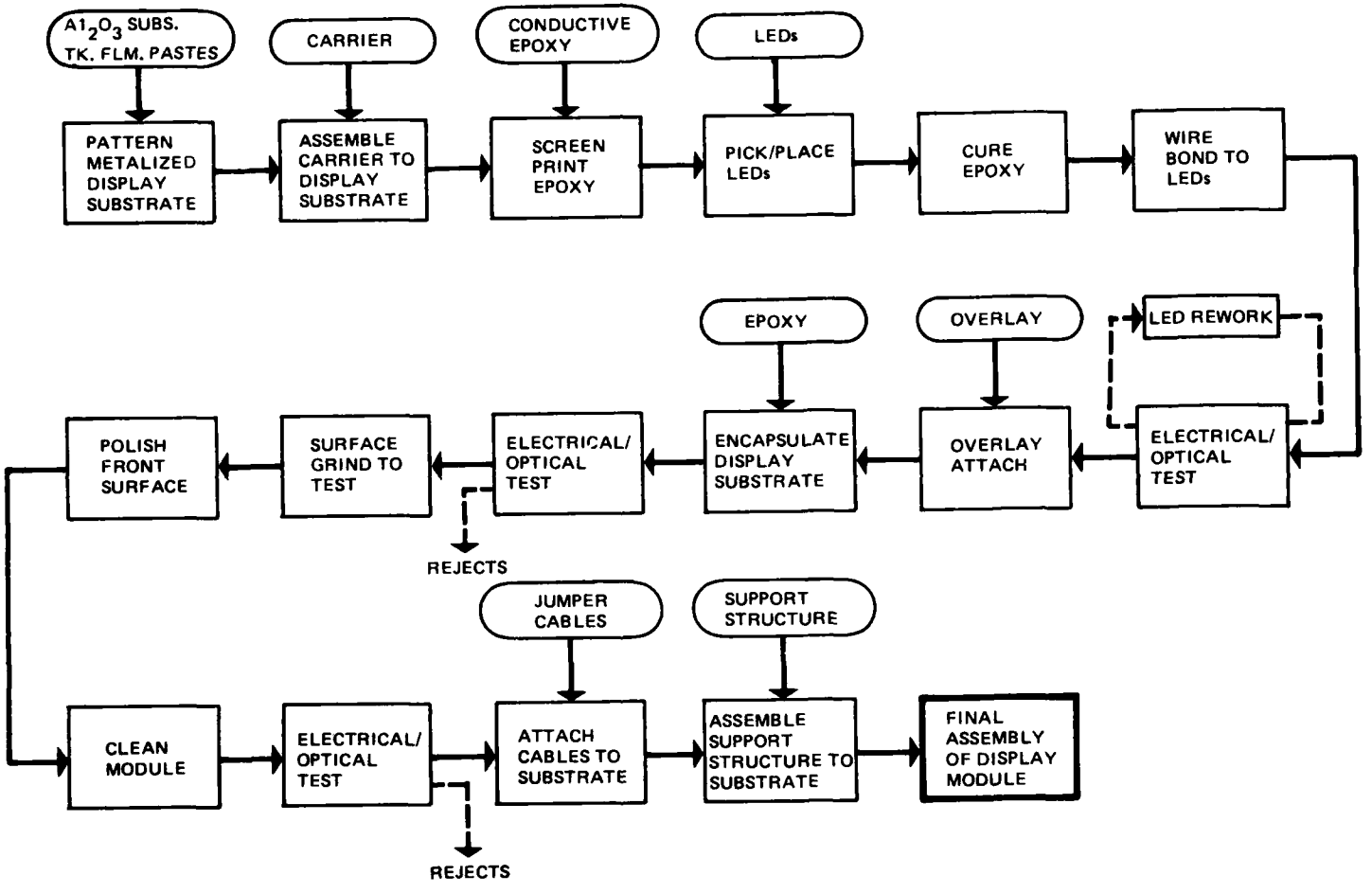
$Al_2O_3$ SUBS. TK. FLM. PASTES
CARRIER
CONDUCTIVE EPOXY
LEDs
PATTERN METALIZED DISPLAY SUBSTRATE
ASSEMBLE CARRIER TO DISPLAY SUBSTRATE
SCREEN PRINT EPOXY
PICK/PLACE LEDs
CURE EPOXY
WIRE BOND TO LEDs
EPOXY
OVERLAY
LED REWORK
POLISH FRONT SURFACE
SURFACE GRIND TO TEST
ELECTRICAL/ OPTICAL TEST
ENCAPSULATE DISPLAY SUBSTRATE
OVERLAY ATTACH
ELECTRICAL/ OPTICAL TEST
REJECTS
JUMPER CABLES
SUPPORT STRUCTURE
CLEAN MODULE
ELECTRICAL/ OPTICAL TEST
ATTACH CABLES TO SUBSTRATE
ASSEMBLE SUPPORT STRUCTURE TO SUBSTRATE
FINAL ASSEMBLY OF DISPLAY MODULE
REJECTS
80614-8

Figure 8

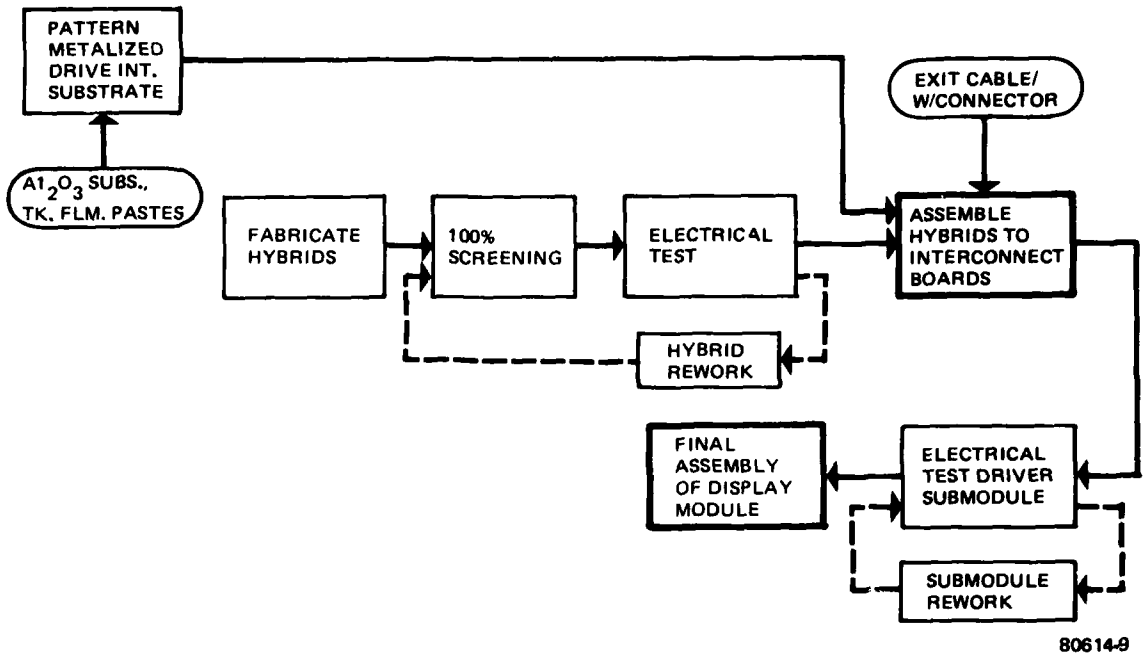


Figure 9

using an aluminum oxide substrate for each with a ring frame mounted on top of each hybrid and surrounding the circuits. This ring frame supports a metal cover which allows for hermetic sealing.

LED modules provide many reasons for automated testing. Among them are the sheer number of modules, and the even larger number of LEDs which have several parameters that must be verified. As a result of these factors, an automated test station has been developed.

The test station views a module to be tested through a fresnel lens. This lens has an optical detector with focused light that may be transformed to an equivalent voltage. This voltage is then fed to a detector which has been preset to indicate the several threshold values that correlate to no light output of an LED, too low an output from an LED, and too high an output. This detection is automatically performed for each LED on the module surface. If there is a problem with a module, the information as to location, nature, and value of deficient parameter is printed. At this point, the operator may stop the test and evaluate the problem, or wait until the complete module has been tested. A block diagram of the basic tester is shown in Figure 11.

## CONCLUSIONS

The technology base of hybrid circuitry has contributed heavily to the success of the LED module presented. The industrial machinery presently being evaluated will further allow practical automation of hybrid fabrication processes, LED surface dice placement and wire bonding, and finished module testing.

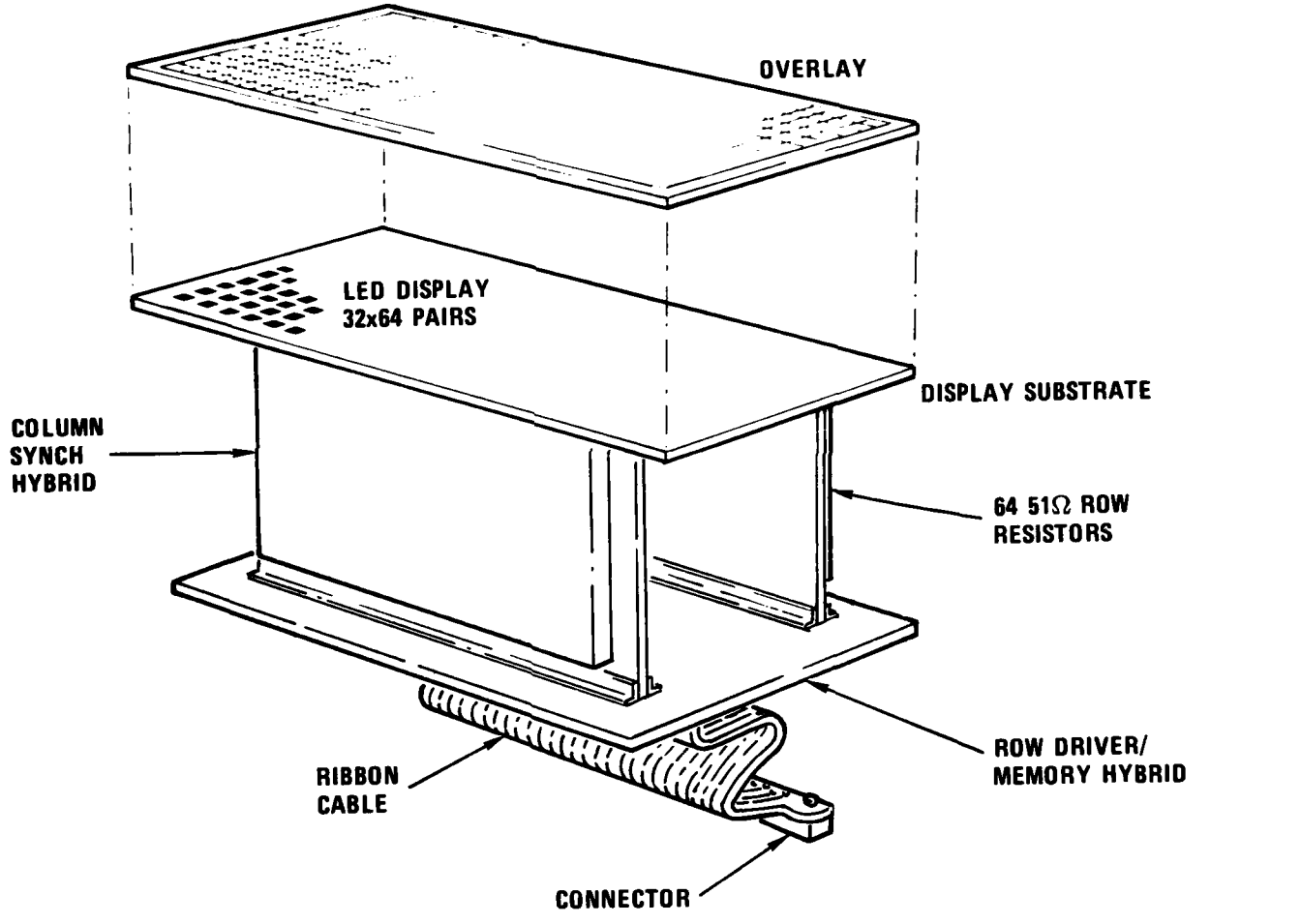
OVERLAY
LED DISPLAY
32x64 PAIRS
DISPLAY SUBSTRATE
COLUMN
SYNCH
HYBRID
64 51Ω ROW
RESISTORS
ROW DRIVER/
MEMORY HYBRID
RIBBON
CABLE
CONNECTOR
80614-5A

Figure 10

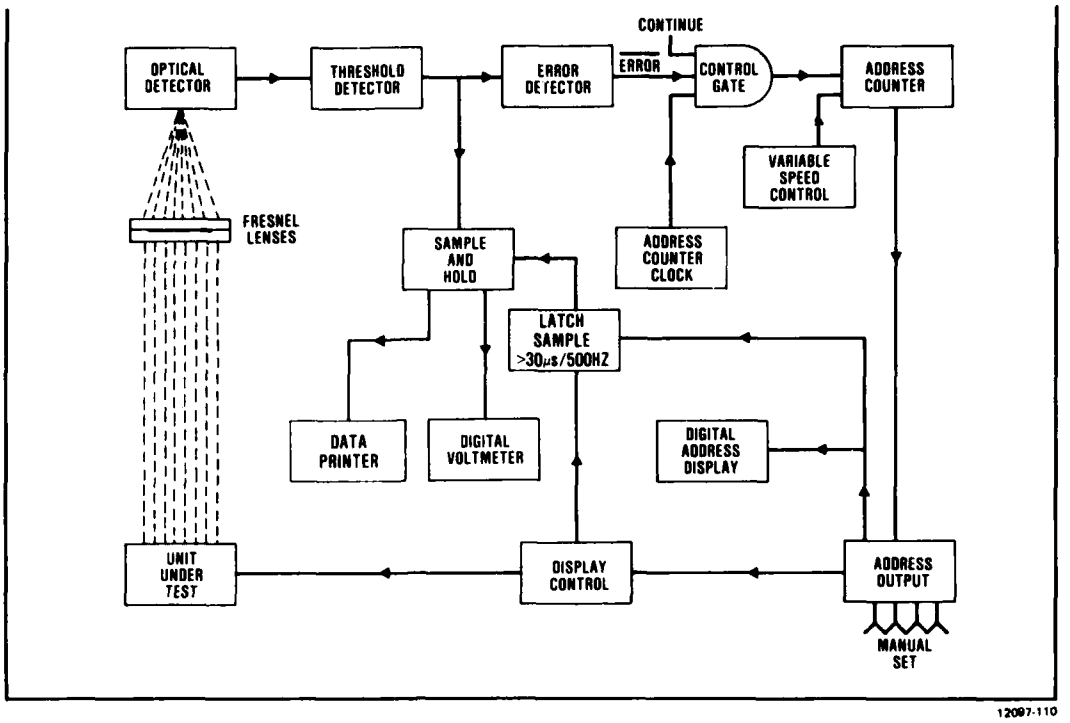


Figure 11

The completed modules described herein will be included in many varied configurations, as depicted in Figures 12 and 13, and will provide the customer with a highly reliable, effective, and cost-appropriate command, control, and communications device.

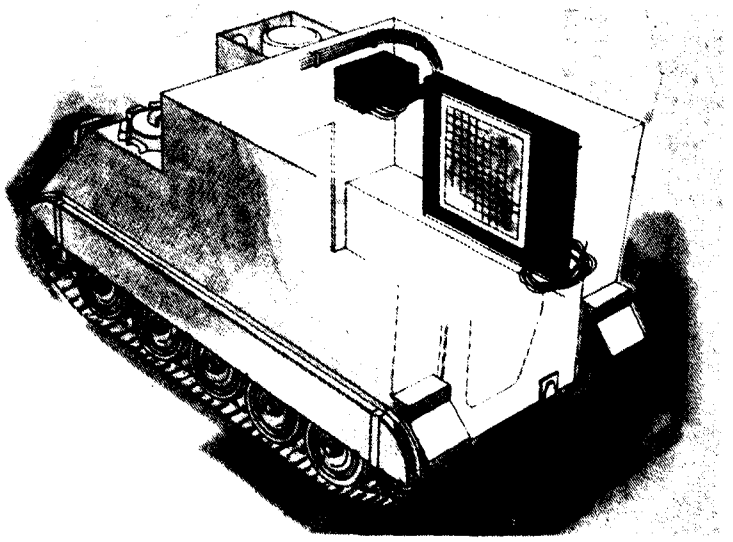

Figure 12

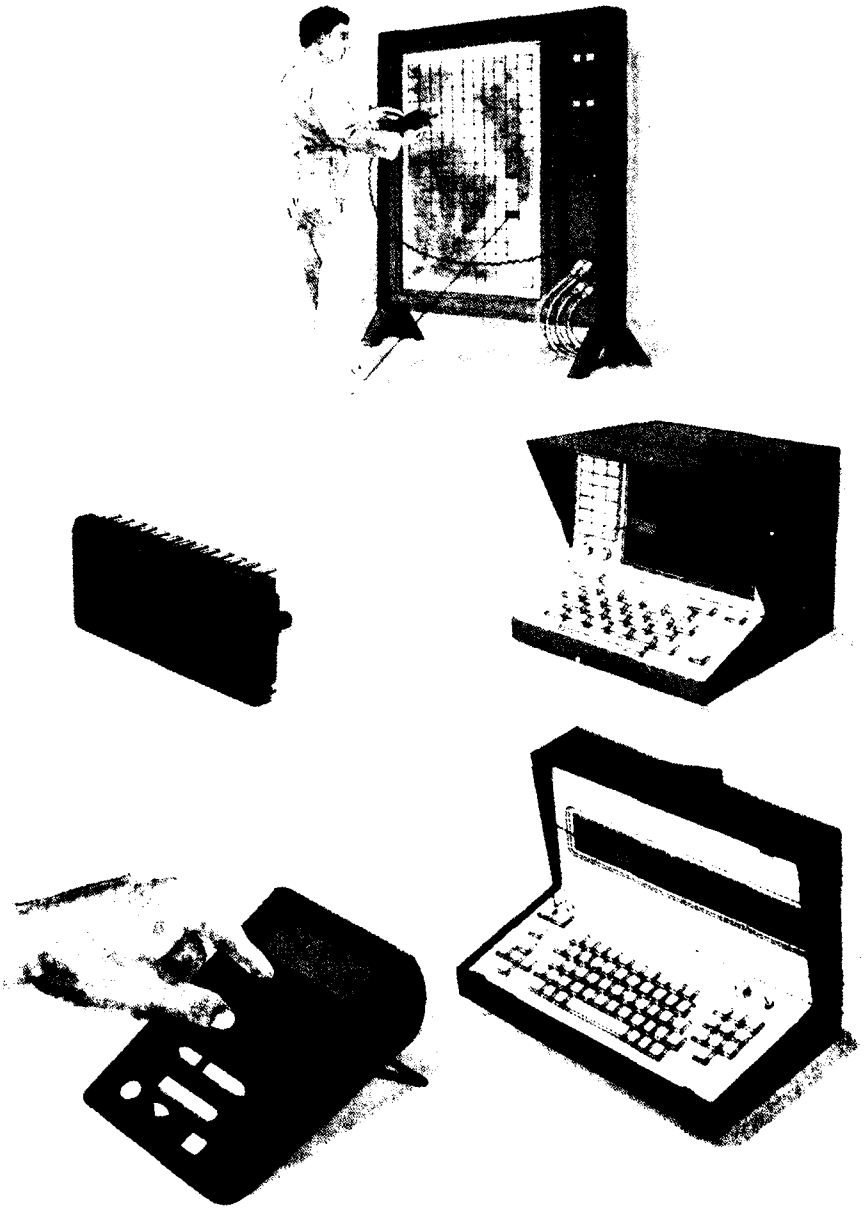

Figure 13

# LARGE OPTICAL HYBRIDS

BY

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## ABSTRACT

The development and fabrication of large optical hybrids combines the usual disciplines of thick and thin film technology with special packaging design for sensor mounting, optical window mounting and custom package configurations. In addition, because there is usually a significant cost associated with the finished circuit, an extremely high emphasis must be placed upon pre-seal screen testing of components and sub-assemblies to avoid unnecessary risk to the hybrid during rework. This is also a driving force for the design and development of repairable packages.

## INTRODUCTION

The requirement to develop and assemble large optical hybrids for aerospace applications is usually due to the need to achieve improved signal-to-noise ratios and to achieve an optimum density of photo sensors in relation to the optics of the system.

This paper will discuss the development and manufacture of two large volume custom hybrids used in optical applications. The first is the Viking PSA (Photo Sensor Array) used on the two Viking Lander Spacecraft which have been taking pictures of the Martian surface since 1976. This hybrid uses twelve sensing diodes to generate color, infra-red and precision black and white imaging. The second hybrid is a precision focal plane array utilizing large (930x60 mils) CCD (Charge Coupled Device) chips. Each chip has 1728 pixels (picture elements) arranged in a 1728x1 linear array. A total of six chips are mounted in the hybrid package to form a 1728x6 array in a focal plane. The array is assembled with precision such that all pixels are coplanar within $\pm$ 15 microns.

These hybrids are custom in the true sense of the word. The requirements, the size, the reliability required, the need for optical windows in the lids, etc., mandated special designs as well as innovative use of materials, assembly techniques, and test approaches. This paper will describe some of the crucial problems encountered and highlight those aspects of the solutions and approaches which may relate more directly with forthcoming military production needs. This will probably be most directly applicable to those uses where large packages are required, where repairability is needed

where epoxies provide ease of fabrication or economic benefit, where precision thermal matching to a large chip is important, where reliability and yield improvement of large area hybrids by means of baby-board mother-board assembly is advantageous, and/or where chip-level burn-in and screening is being considered. Also, this work applies for any requirement to produce a hybrid package with an optical window.

The development of these large-volume hybrids has lead directly to questions indicating that accepted limitations such as rework requirements may need to be revisited for large packages. Also, the usual test requirements for leak testing (bomb pressures, the use of flourinert, etc.) provide unique problems for large hybrids. Our successful use of pre-cap burn-in will be presented.

## VIKING PSA (PHOTO SENSOR ARRAY)

The two Viking Landers sent to Mars in 1976 each employed a pair of facsimile cameras. At the heart of the camera was a large hybrid circuit called the Photo Sensor Array (PSA). The PSA included the optical filters, detectors, amplifiers and multiplexing circuitry to convert the incoming optical image to a voltage level ready for digitizing in the camera electronics. Figure 1 shows the array with the cover removed. Each preamplifier was assembled as an individual hybrid and thoroughly screened tested in a pre-sealed state before mounting on the motherboard substrate. Photodiodes were bonded to small KENNERTIUM blocks with gold-tin solder preforms to establish the desired focal plane height for the detectors. While it is not clearly visible in Figure 1, the optical filters are each epoxy bonded to an aperture/filter holder assembly which locates the apertures directly above each detector at a prescribed distance.

During the development program, several difficult problems were encountered and solved by contributions from technical personnel in the disciplines of electronics, optics, systems engineering, materials engineering and failure analysis. It is pertinent to point out a few of these problems since they serve to illustrate the pitfalls involved with large scale hybrid circuit packaging.

1. Rework and Repairability. Approximately 300 hybrid components and 500 wires were included along with optical components in the PSA. Most of the circuit parameters were difficult to achieve and necessitated chip replacement at various stages including the final un-sealed assembly stage. The original design called for solder or eutectic bonding which was revised to allow gold filled epoxy bonding for chip replacement.

2. Optical Filter Crazing. The normal temperature rate changes produced crazing in the filters. Special assembly and test precautions were implemented to control the temperature rate changes and still provide screen testing effectiveness.

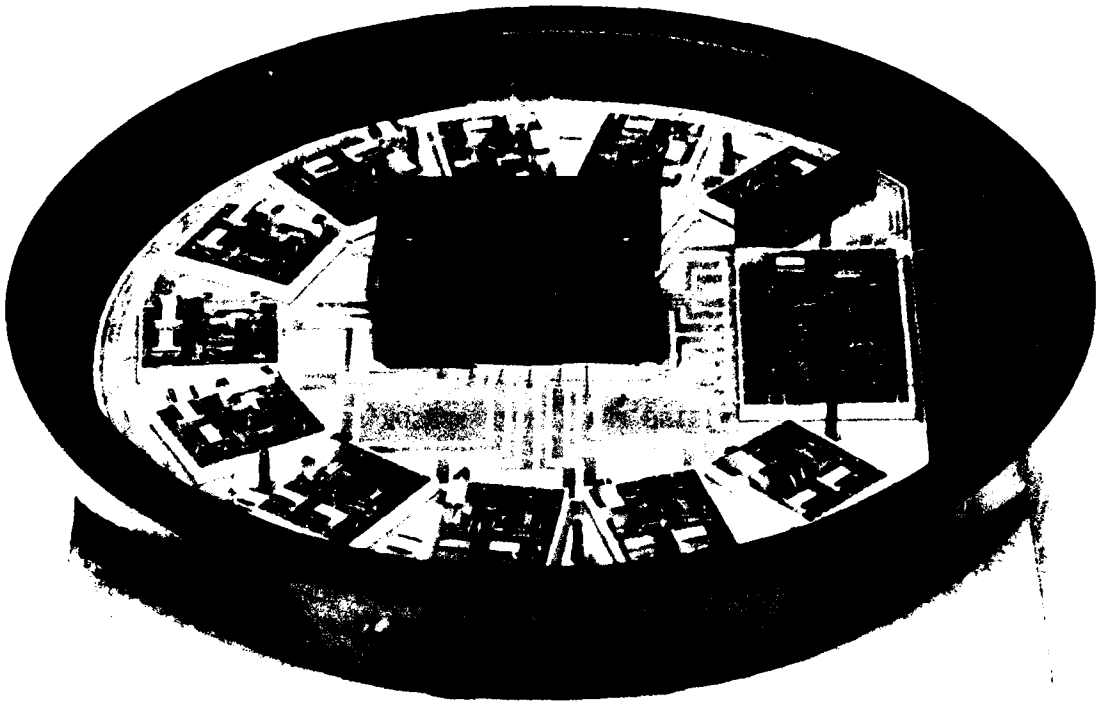

Figure 1 Viking PSA

3. Microphonics. The preamplifiers were extremely high transimpedence amplifiers (700 megohm) and sensitive to wire movement when in proximity with voltage nodes.

4. Window Mounting. The original design used indium solder mounting but due to production problems was finally replaced with a structural adhesive, 3M EC2216. This does not produce a hermetic seal due to the permeability of moisture through epoxy. No failures occurred due to moisture, probably due to the fact that operating temperatures were typically above the moisture dewpoint inside the hybrid.

5. Precision Alignment. The apertures provided on the filter holder and on the cover assembly were kept as small as the optics would allow to minimize stray light effects. This produced a requirement for stringent precision assembly techniques and the need for special tooling. Image vignetting would result from improper location of the diodes with respect to the optical apertures.

6. Leak Testing. Standard hot FLOURINERT gross leak testing was not possible due to the temperature rate limitations. Non-standard helium "sniff" testing and fine leak testing were used effectively.

The PSA used two photodiode aperture sizes etched through the diode metallization exposing the photosensitive junctions. Low resolution imaging used a 4.5 mil aperture and high resolution required a 1.5 mil aperture. The diodes were operated in the unbiased mode with high gain transimpedence amplifiers. Silicon photoresponse from approximately 350 nm to 1100 nm was optically separated into the visible color spectrum of blue, green and red, and the near infrared spectrum defined as IR1, IR2 and IR3 which included wavelengths from about 800 nm to 1100 nm. The amplifiers were trimmed for channel gain to provide equal outputs for each of the six filtered channels. Figure 2 shows the wavelengths of each channel in the optical spectrum. In addition to the filtered channels which used low resolution diodes, there were 4 broadband high resolution channels focused at various distances, a broadband low resolution channel used for survey scanning and a sun calibration channel which had no amplification and was used to study atmospheric extinction in dust storms and at low horizon imaging angles.

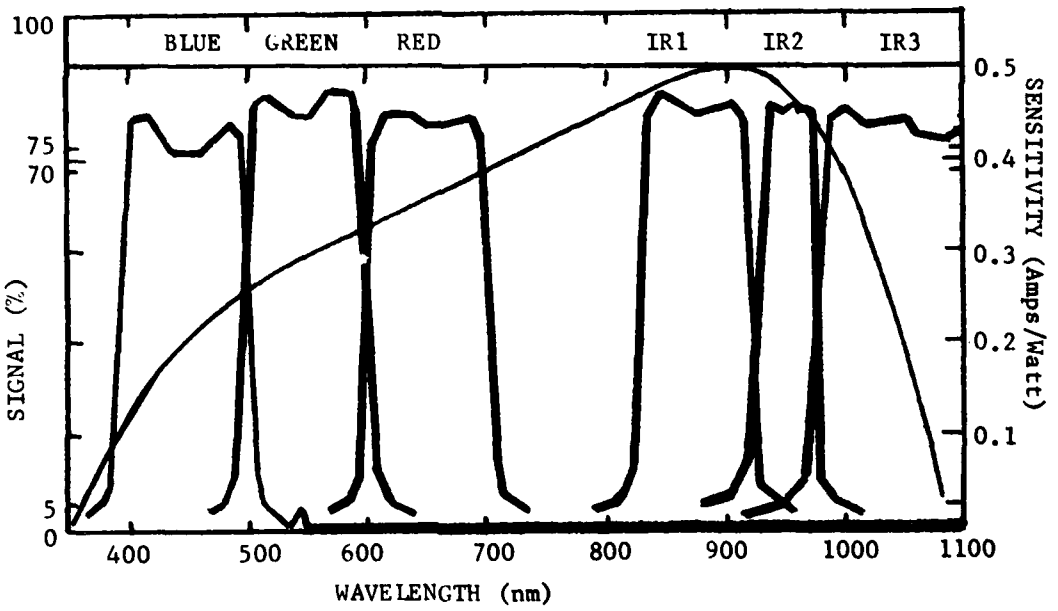


Figure 2 PSA Channel Spectral Response

Photocurrent was required to be as low as a few picoamperes ($10^{-12}$ amps) therefore, the amplifier design used a JFET front-end followed by a monolithic operational amplifier incorporated within the feedback loop. Input leakage current specifications were down to 1 picoampere limits at 25°C. Leakage current, noise, phase margin and gain stability were all critical parameters. In order to produce a reasonable yield, preamplifier parameters were "married" with individual channel gain and stability requirements which proved to be a cost effective compromise over the extremely low yield of preamplifiers when tested against the sub-assembly design specifications.

The custom package was machined from KOVAR and included a bottom stud mount for the camera assembly. The package is 2" in diameter with provisions for a resistance welding lip and mounting holes for discrete barrel feedthru pins. Standard SN-63 lead-tin solder was used to mount the feedthrough pins prior to package leak testing. The precision cover assembly was resistance welded to the package with a standard seam welder. Vacuum bakeout prior to sealing was performed in a special cannister fitted to a residual gas analyzer. The bakeout temperature was maintained at +125°C until all outgassing constituents totalled less than 10 parts per million. The cannister was allowed to cool and backfilled with dry nitrogen. In this manner, the assembly was protected from exposure to the ambient atmosphere and particulate contamination sources while being prepared for sealing in a dry nitrogen atmosphere.

In summary, the Viking PSA program was successful although the development required considerable effort in adapting materials and processes as well as special test and evaluation methods. The device was non-hermetic in that the optical window was mounted with epoxy. At the time (1973) the effects of moisture permeation through epoxy were not as well understood as they are today. Of the 20 arrays built which used thin film resistors in the amplifiers, none failed due to moisture related causes. During this development, serious questions regarding the applicability of MIL-STD-883 test methods for large hybrids were successfully resolved with alternate test methods and environmental stress levels. The experience gained on the Viking PSA program led directly into the Linear Image Sensing Array program discussed next.

## LISA (LINEAR IMAGE SENSING ARRAY)

The LISA is a large optical hybrid array of charge coupled devices (CCD's) designed for extended life operation (10 years). Most of the requirements specified by MIL-M-38510 and the test methods described in MIL-STD-883 apply to the circuit. The LISA has six CCD's mounted in a 1728x6 pixel (picture element) focal plane where all of the 10,368 pixels are required to have precise x and y location coordinates and lie within a best fit plane of $\pm$ 15 microns maximum. A photograph is shown in Figure 3 which depicts the custom package, main substrate and CCD/carrier substrates.

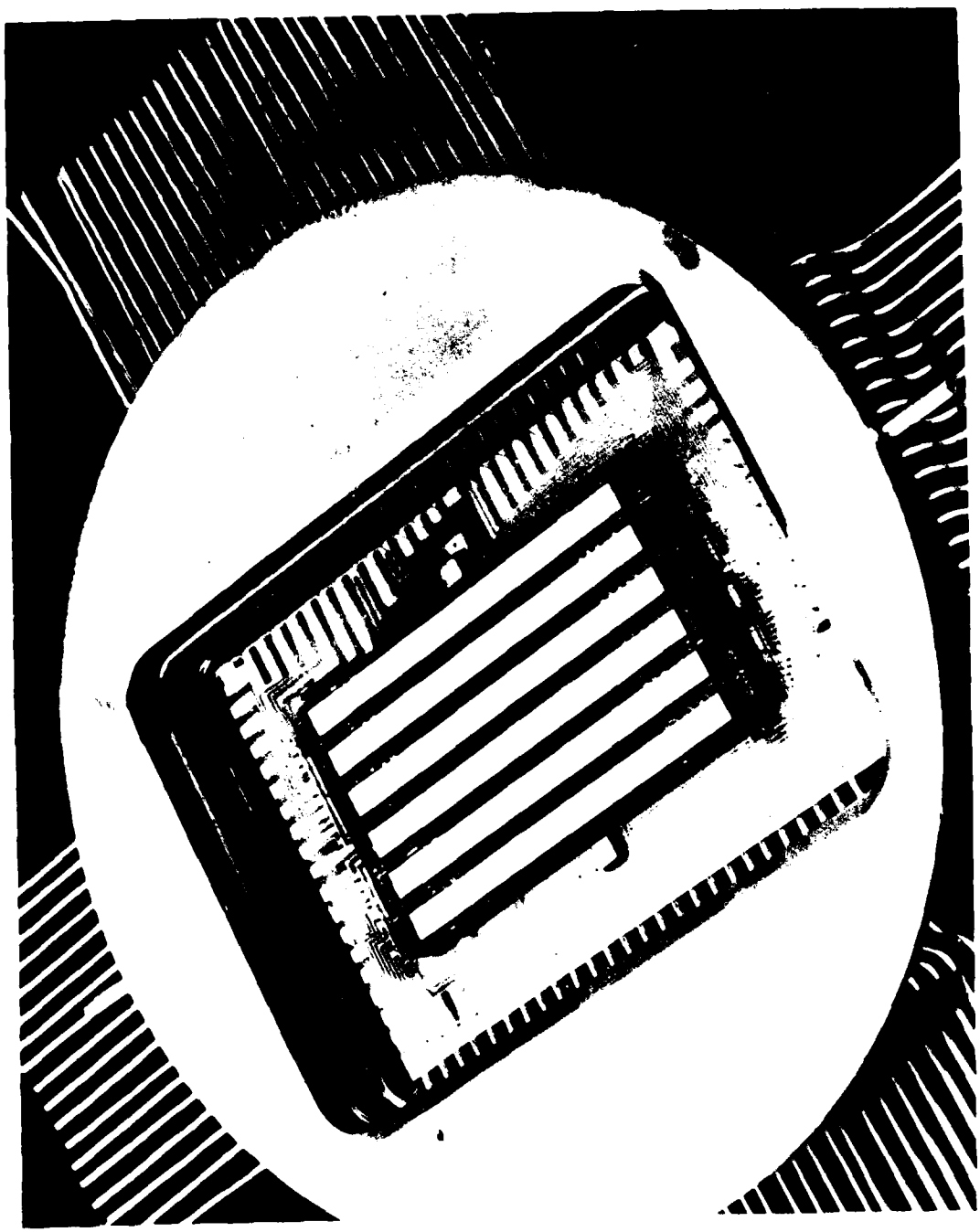

Figure 3 LISA

The nature and the characteristics of the LISA are more readily understood with the following table of summary specifications.

TABLE 1 LISA REQUIREMENTS

| Description | Tolerance |
|---|---|
| Pixel Plane | All pixels coplanar within ± 15 microns. |
| Pixel Position | Trueposition within a 25 micron radius and with lines perpendicular to a reference datum line. |
| Pixel Plane Mounting | Pixel plane to package mounting surface parallel within ± 12.5 microns. |
| Window Mounting | Parallel to pixel plane within 15 arc minutes. |
| Package Mounting Surface | 1.2" x 1.7", flat within .0001". |
| Operating Temperature | Thermo-electrically cooled to -10°C ± 1°C. |
| Storage Temperature | -55°C to +85°C. |
| Internal Temperature Sensors | Accuracy within ± .1°C. |
| Environmental Tests | Temp. Cycle -55°C/+125°C.<br>Burn-in +125°C.<br>Acceleration 5 kg's (eliminated)<br>Mech. Shock<br>Vibration, sine and random<br>Non-destruct wire bond pull<br>Non-destruct substrate bond push |
| Electro-Optical Tests | Pixel Plane Dimensions<br>Responsivity<br>Linearity<br>Noise Equivalent Irradiance<br>Dynamic Range<br>Dark Signal<br>Crosstalk<br>Transfer Efficiency and Trapping Losses |

The packaging design of the LISA was developed around the following:

- o The CCD performance
- o The flatness and stability requirements
- o The thermal requirements
- o The large optical window (1.5" diameter by .125" thickness)
- o The large number of external leads (88)
- o Repairability
- o The intensive reliability requirements

A. CCD PERFORMANCE. Packaging design included mounting the long narrow chip (.93"x.06") on a precision multilayer thin film sapphire carrier substrate. Each CCD chip required intensive electro-optical testing and environmental testing in order to screen for the devices capable of meeting the LISA performance requirements. The Fairchild CCD121 device was selected for the program even though it was designed to be used in commercial page reading equipment. At an early date it was recognized that the CCD121 device was capable of meeting most of the requirements if an effective evaluation and testing program could be implemented. At Fairchild, successful wafer line run qualification tests were completed along with a reasonable wafer level performance probe test program. Devices delivered to Martin Marietta were generally capable of achieving the specifications but required an additional sub-assembly level detailed test program to select the approximate 1 in 5 devices finally used in the LISA.

The LISA requirement calls for pixel lines to be 2.5 millimeters apart. At this distance there is insufficient space between lines to route signal conductors for wirebonding, therefore the decision was made to provide a multilayer thin film carrier substrate which routed the conductors beneath the CCD chip. Additionally, the pixel plane flatness at the LISA was specified at $\pm$ 15 microns. The free curvature of the .9 inch chip was about 50 microns due to built in semiconductor material mismatches. The chip was required to be bonded flat to a flat substrate without damaging any of the conductive layers. A relieved chip surface contacting tool and vacuum chuck was designed which holds the chip flat to within 3 to 5 microns in the uncured gold filled epoxy bond material.

B. FLATNESS AND STABILITY REQUIREMENTS. To a large extent, the pixel plane flatness dictated much of the design and other factors such as thermal paths and assembly tooling and processes were relegated to lower priority.

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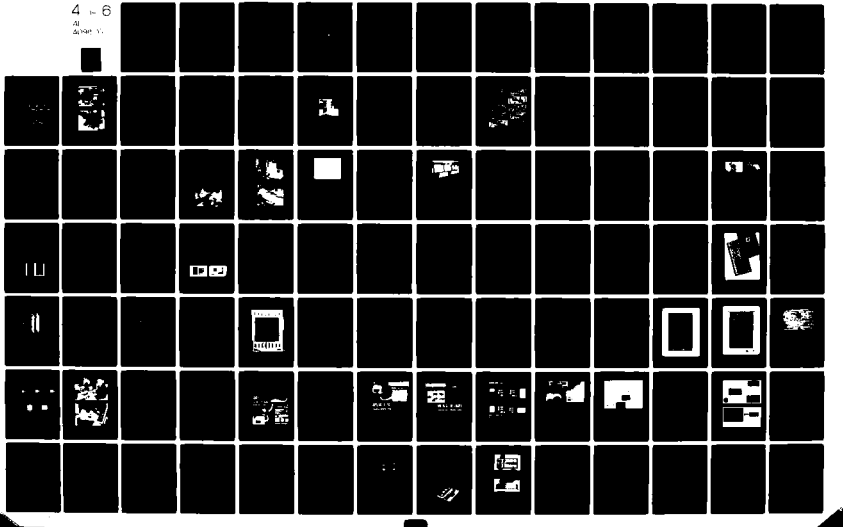

A four layer laminate exists when considering a section of the LISA as shown in Figure 4.

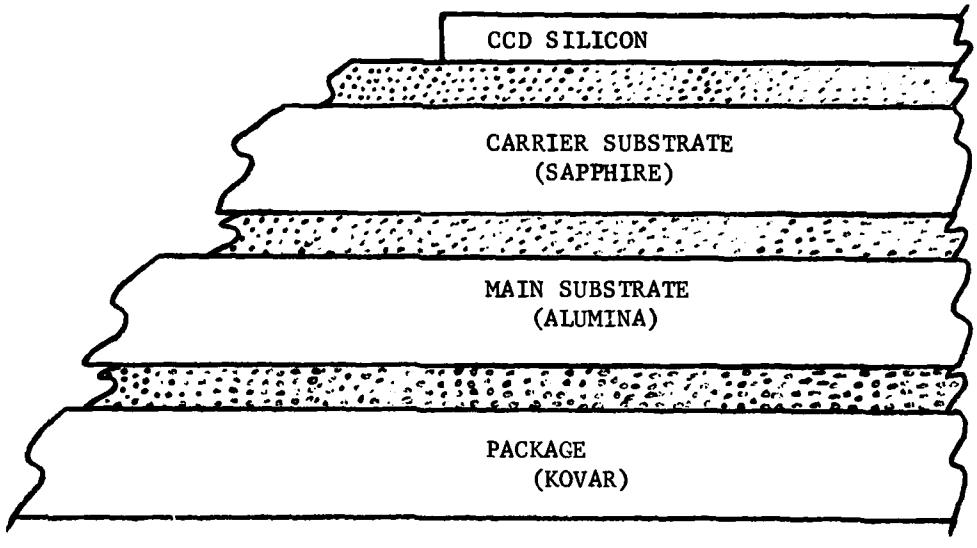


Figure 4 Laminate Structure of LISA

The four materials include two fixed materials, the .008" thick silicon CCD chip and the optional thickness of the KOVAR package base. KOVAR was selected over other materials because of industry experience with glass seal processing. Two other materials, the CCD carrier substrate and the main substrate are optional for thickness and type of material. The thicknesses and material types were chosen after dividing the complex laminate into two "Bimetallic" spring configuration laminates and evaluating the bimetallic spring deflection equation:

$$\frac{1}{\rho} = \frac{(\alpha_2 - \alpha_1)(T - T_0)}{\frac{h}{2} + \frac{2}{h}(E_1 I_1 + E_2 I_2)\left(\frac{1}{E_1 a_1} + \frac{1}{E_2 a_2}\right)} \qquad (1)$$

Where $\rho$ = Radius of curvature

$\alpha$ = Thermal coefficient of expansion

E = Elastic modules

I = Moment of inertia (per unit width)

a = Material thickness

$h = a_1 + a_2$

T = Temperature, $^{o}C$

Figure 5 shows the bimetallic curvature.

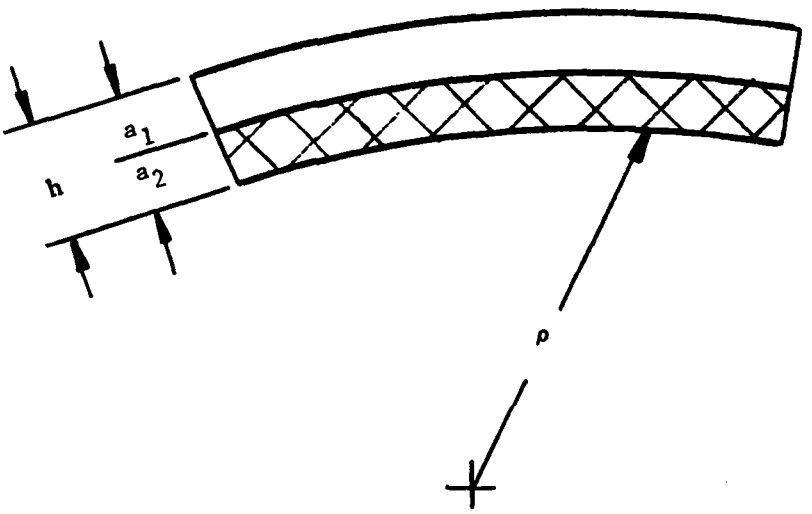


Figure 5 Bimetallic Curvature

The goal was to match the materials and thicknesses to produce minimum curvature over the temperature range and produce a compensating, or opposite curvature between each of the two laminates.

Some of the possible and practical materials are:

| | | |
|---|---|---|
| SILICON | $\alpha = 2.6 \times 10^{-6}/^{o}C$, | $E = 16 \times 10^{6}$ PSI |
| ALUMINA | $\alpha = 6.3 \times 10^{-6}/^{o}C$, | $E = 48 \times 10^{6}$ PSI |
| QUARTZ | $\alpha = 0.5 \times 10^{-6}/^{o}C$, | $E = 10.6 \times 10^{6}$ PSI |
| SAPPHIRE | $\alpha = 5.8 \times 10^{-6}/^{o}C$, | $E = 55 \times 10^{6}$ PSI |
| KOVAR | $\alpha = 4.7 \times 10^{-6}/^{o}C$, | $E = 30 \times 10^{6}$ PSI |

The final selections were:

| | | |
|---|---|---|
| SILICON, | .008" thick | (CCD) |
| SAPPHIRE, | .050" thick | (Carrier Substrate) |
| ALUMINA, | .050" thick | (Main Substrate) |
| KOVAR, | .025" thick | (Package Bottom) |

This produced the following curvature and stresses in the laminated materials. It assumes an unyielding bondline and temperature range of 25°C to -10°C:

CHIP/CARRIER $1/\rho = 16.5 \times 10^{-6}\ \Delta T$

SUBSTRATE/PACKAGE $1/\rho = -26.4 \times 10^{-6}\ \Delta T$

| | | |
|---|---|---|
| $\sigma$ CHIP | = 1464 PSI | At Chip/Carrier Interface |
| $\sigma$ CARRIER | = 1023 PSI | |
| $\sigma$ SUBSTRATE | = 1290 PSI | At Substrate/Package Interface |
| $\sigma$ PACKAGE | = 849 PSI | |

A prototype device was fabricated and tested for flatness and stability. The results from 25°C to -10°C showed less than 1 micron change in flatness for the focal plane over its area of 22.5 mm x 12.5 mm.

C. THERMAL REQUIREMENTS. The assembly of the LISA required the use of epoxy preforms and small copper shims to space the CCD/Carrier assemblies into a best fit focal plane on the main substrate and copper shims to mount the substrate assembly so that the focal plane would be parallel to the package base. The only heat source of significance inside the LISA is the on-chip CCD amplifier which consumes about .2 watts for continuous useage. With the amplifier left on, the pixels nearest the output end will run considerably hotter than pixels farther down the pixel line. The dark signal of the CCD pixels doubles every 8°C. A dilemma exists if one desires minimum dark signal (or dark signal uniformity) and coplanarity of pixels which requires the design previously discussed. To solve this, the amplifier is switched on for just long enough to read out the pixel string for one line. The pixel integration period for the LISA is 80 milliseconds with the line readout time set to 1/6 of the integration period. Although this allows the dark signal to integrate for the full 80 milliseconds, it is affected by the on-chip heat source for only 1/6 of the period. With special pulsing techniques to get the equivalent of zero power dissipation, it was found that pixels nearest the amplifier experience only about a 3°C rise in temperature and this rise is dissipated after about 200 to 300 pixels of the 1728 pixel line length. For this application, the thermal impedence was not critical. The design specification was allowed to be compromised in order to achieve the focal plane flatness and stability.

D. COVER ASSEMBLY DESIGN. The optical window specification called for BK-7 glass with a 10-5 scratch-dig finish and anti-reflection coating on both sides of the glass. The dimensional requirements also called for controls on the wedge angle, thickness tolerance, mounting height from the focal plane and parallelism with the focal plane. The mounting material needed to provide a true hermetic seal with the LISA cover. Of prime importance for the device reliability and ability to withstand the test and operating environments is achieving a good thermal expansion match between the glass and the metal cover for the hybrid. The design which eventually satisfied all the requirements is shown in Figure 6.

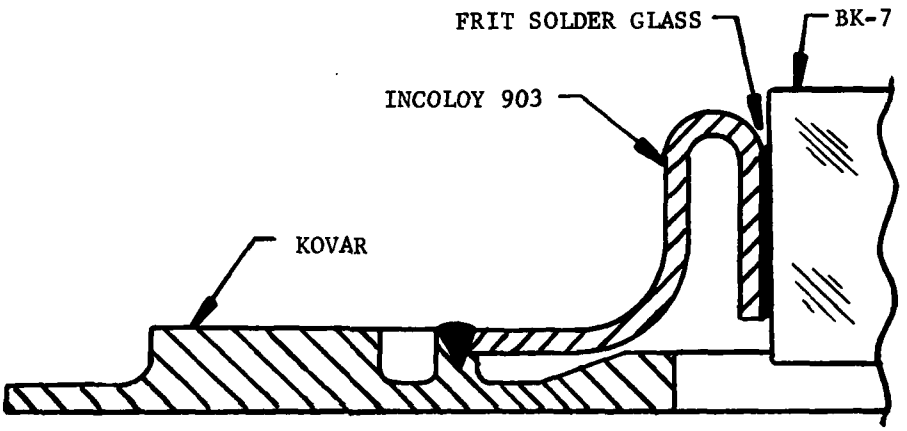


Figure 6 LISA Cover Assembly

The design features a thin expansion ring which is mounted to the window with Schott Solder Glass No. 8463. This material exists in powdered form and is fired in a belt furnace at 450°C. The expansion ring material, Incoloy 903, was selected for its close coefficient of thermal expansion match to BK-7 glass. Under the LISA environments, the frit solder glass bondline is maintained in slight compression.

The assembly procedure and sequence of operations was developed at Martin Marietta for the LISA program and is listed below:

1. Pre-oxidize the expansion ring.
2. Jig mount the BK-7 blank in tooling along with the expansion ring.
3. Successively apply and fire frit solder glass in layers between the vertical edge of the glass and the expansion ring.
4. Grind and polish the window sub-assembly.
5. Vacuum deposit magnesium flouride.
6. Electron beam weld the expansion seal to the KOVAR cover.
7. Gold plate.

The results of the cover assembly development and testing at first uncovered problems in warping and frit seal fractures during the electron beam welding operations. It was found that too much voiding in the frit bond line existed. The process was revised to eliminate the use of a fluid which put the frit into paste form. Also, the application of a few layers of dry powder provided for a minimum of entrapped air bubbles in the molten glass.

Tests were performed to evaluate the resonant frequency, spring constant, resistance to pressure differentials and resistance to temperature cycling. The design was found to be rugged and solved all the design specification problems. For a screen test, all of the cover assemblies are subjected to leak testing, temperature cycling (-55°C to +125°C), bi-directional pressures (±40 psi) and repeat leak testing.

E. CUSTOM PACKAGE DESIGN. The base of the package is rectangular to match the substrate assembly, mate to a thermo-electric cooler and provide 88 pins. The upper flange is round to accept a T.I.G. (Tungsten Inert Gas) weld seal of the cover assembly. No commercially acceptable alternative existed which would provide close enough tolerances for the focal plane dimensions previously discussed. Bar stock KOVAR was first used from which to machine the blank packages but was found to have a high incidence of inclusions resulting in leak test failures. Good success was found with forged sheet stock. The machining operation was first to "rough" out the blanks, anneal to relieve machining stresses and then follow with electron discharge machining (EDM). The resulting package body is sufficiently stress-free to maintain critical tolerances when subjected to copper braze and hard-glass sealing processes.

The leads are pre-assembled into lead frames and fused into the package using standard microelectronics glass seal processing. Experience has shown that this process requires extensive control and in-process inspections in order to achieve reliability with small production quantities.

F. TESTING AND VERIFICATION. This section will not address electro-optical testing in detail other than to call attention to the extensive use of pre-seal temperature cycling and dynamic burn-in for the selection of CCD's and

evaluation of the LISA prior to welding the cover in place. Pre-seal testing was a necessity and has proved extremely successful. Special purged nitrogen enclosures for all sub-assemblies were designed and used for production testing. An on-line computer with specially designed electro-optical interface tooling and precision calibrated light sources were developed for the program. Some key elements of the test program are listed below:

1. Non-destructive wire bond pull testing.
2. Push testing of carrier to substrate bond lines.
3. Mensuration Testing (e.g. the measurement of the precise location of all the pixels).
4. Particulate control (cleaning and inspection for particles exceeding 10 microns size).
5. Vacuum bakeout (as in the Viking PSA program using RGA and sealed cannisters).
6. T.I.G. Welding in a special argon chamber followed by backfill purging with 10% helium and 90% nitrogen through cap-off tubes provided on the LISA.
7. Dry gross leak testing using a "sniff" tester connected to a controlled volume container with the LISA inside.
8. Fine leak testing after pressurized bombing in helium (in addition to the 10% by volume sealed-in helium).

G. REWORK CAPABILITY. It was necessary to develop techniques for replacing individual failed CCD carrier assemblies because of the great expense of a LISA. Since a CCD failure could occur at any level of assembly, the design of the LISA (and its attachment to the next level of assembly) had reworkability as a primary criteria.

The optical window cover assembly can be successfully removed from the LISA be carefully machining away the TIG weld bead attaching it to the LISA package body. A continuous nitrogen purge through the package cap-off tubes has been demonstrated to prevent any machining chips from entering the LISA internal cavity.

Epoxy bonding is used extensively within the LISA and to attach it to the next level of assembly. Experience during the LISA prototype program identified specific epoxy bond lines that were most likely to require rework to replace failed sub-assemblies. The general approach to reworking these bond lines is to heat them until the epoxy is temporarily weakened. While at this temperature, tooling is used to apply mechanical stress to the bond which gradually fails through plastic deformation. Extensive materials and process evaluation was performed to determine epoxies and rework procedures for each bond line. Temperatures and times are carefully controlled so that bond lines not intended to be separated during rework will regain full strength after the unit is returned to room temperature. The ability to perform rework of a completed unit was demonstrated using a design proof test LISA prior to reworking any flight units.

## CONCLUSIONS

The results gained on the two large optical hybrid programs described in this report support the general requirements of MIL-M-38510 and MIL-STD-883. Implementation of the testing, application of de-lidding and rework and compromise to certain fundamental microelectronics specifications must be done with an extreme diligence to proof testing, analysis and qualification testing. The intent of the specifications can usually be met with special test methods, special fixturing and carefully evaluated test levels. The key results, conclusions and recommendations are summarized below:

a. Pre-seal burn-in and temperature cycling was successful in every way. The recommendation for specific useages points to careful analysis and testing of the moisture content and purity of the nitrogen atmosphere prior to implementing these tests.

b. The CCD wafer and chip screening program was successful, however, a higher yield with fewer performance questions could be obtained with more emphasis on matching a wafer functional test to the end item performance requirements. It was thought that this produces too great a burden on the chip manufacturer and that simpler wafer funtional testing would suffice. Experience has shown that detailed application test requirements and improved test tooling would have been more cost effective for both Fairchild and Martin Marietta.

c. The package lead sealing process had too little specification and verification requirements imposed. It is our firm conclusion that a supplier must be selected that has achieved solid production success with production quantities of similar products. Even then, the small custom production lot is likely to get into process trouble. The best approach is to select a proven supplier and specify the operation in considerable detail. In addition, in-process source inspection and process samples should be required.

# A COMPUTER CONTROLLED IMAGING SYSTEM FOR AUTOMATIC HYBRID INSPECTION

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## Abstract

We have shown that an electro-optical system can be used for automatic quality control inspection of thick-film hybrid circuits. This work was supported by the U.S. Army Electronics R&D Command under Contract No. DAAB07-77-C-0585 entitled "Automatic In-Process Microcircuit Evaluation." A high resolution (10,000 Television Lines/Raster Height TVL/H) Return Beam Vidicon (RBV) is used to image an entire 2-inch by 2-inch substrate. The RBV is operated with computer controlled electronic steering and zoom to provide an appropriate level of detail for rapid sequential frame inspection. Video from each frame is compared with that from a referenced image stored on a video disc. Differences are displayed on a color TV monitor and processed by the computer to identify and characterize faults. Various manual and automatic inspection sequences can be programmed readily. This technique can inspect hybrid substrates at rates of 750 per hour, and its efficiency makes 100% inspection an economical method for quality control at high through-put rates. This paper describes the hardware instrumentation and reports functional inspection results achieved using sample hybrid circuits with built-in flaws.

## Introduction

Hybrid devices utilizing standard integrated chips, custom interconnection, and ceramic substrates containing printed conductors and components are finding increased use in military systems where size and weight are critical parameters. Printed circuit components such as resistors and critical interconnections require that close tolerances must be held using a high level of inspection, preferably 100%. Present manual inspection techniques involving microscope evaluation result in operator fatigue and uneconomical production rate inspection. A need exists for more automated methods of in-process inspection to improve yield and assure a high degree of quality control.

This paper describes an Automatic In-Process Microcircuit Evaluation (AIME) system which utilizes a high resolution Return Beam Vidicon (RBV) television camera and storage technique. This system demonstrates the feasibility of automatic, 100% inspection during printing of thick-film conductor lines on hybrid substrates as shown in Figure 1.

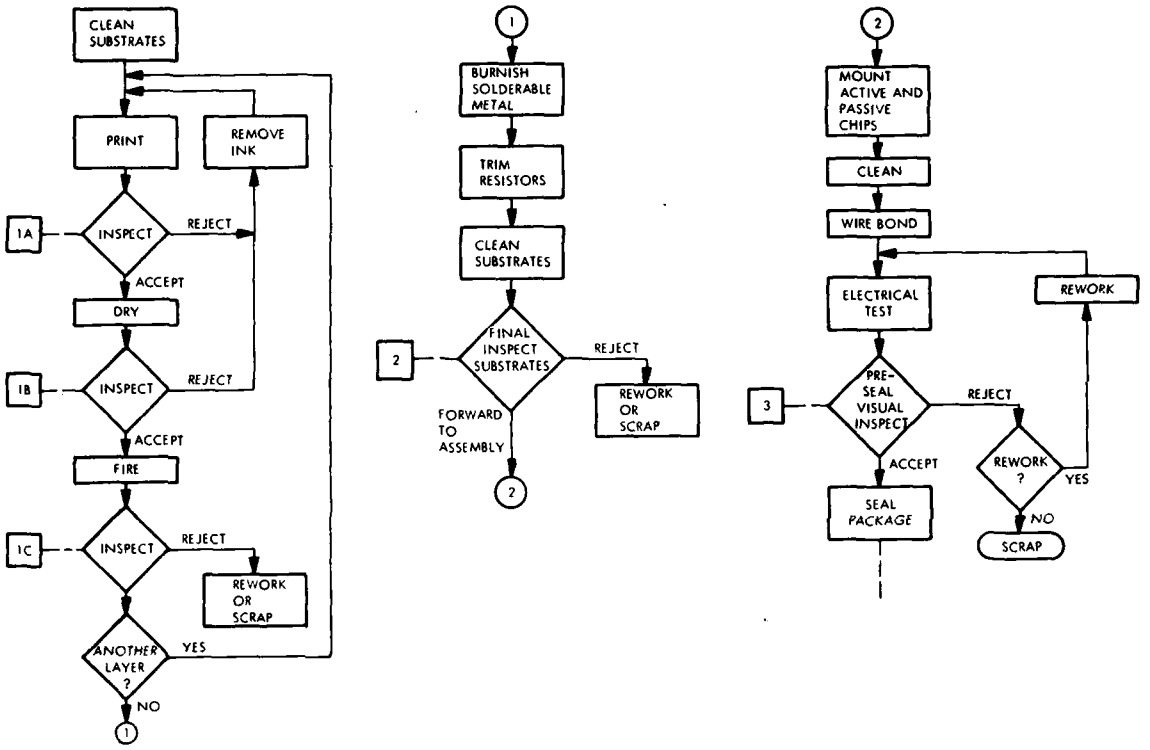


Figure 1. Manufacturing Process Flow with Inspection Points

## Features and Faults of Thick-Film Substrates

To determine the requirements of the RBV camera, it is necessary to evaluate the different kinds of thick-film processing flaws. Figure 2 shows typical defects such as opens, shorts, whiskers between lines, line scratches and smears.

For conditions much worse than in this chart, an out-of-control situation exists with the printing setup. Figure 3 is an illustration of a progressive printing degradation of a single 10-mil line over a series of printing passes on different substrates as the screen gets plugged.

Practical experience indicates that opens in 10-mil lines caused by defective printing will not generally be less than 5 mils. Similarly, short circuits between 10-mil lines separated by 10 mils will be such that the width of the shorting link will range between 5 and 20 mils. Opens due to trapped lint or hair which later vaporize at high temperatures are in the range of 0.5 to 2 mils.

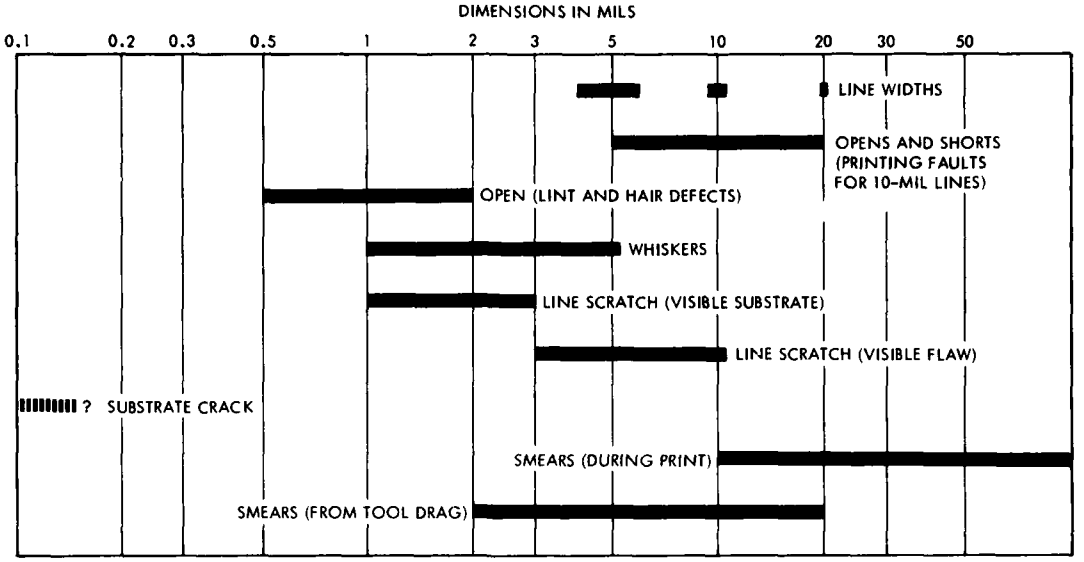


Figure 2. Typical Sizes of Substrate Features/Faults (mils)

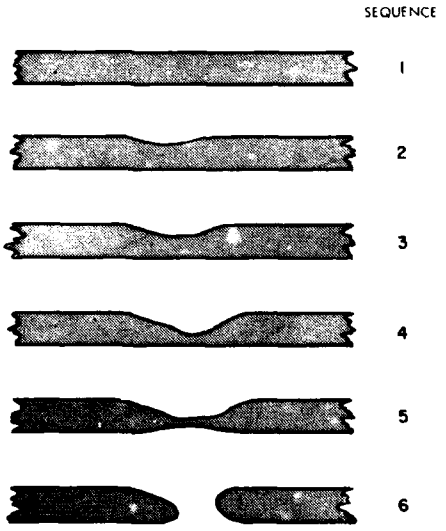


Figure 3. Printing Degradation

## Television Camera Requirements

The heart of the AIME system is the Return Beam Vidicon (RBV) camera. The RBV was chosen as the electro-optical sensor because of its very high resolution over the entire image area. The RBV can provide readout at a continuous rate with a steady-state optical exposure or in near-real time with a discrete input consisting of a shuttered exposure. With discrete input, the information can be read out in a variety of modes, including slow, single-frame scan or fast, multiframe scan. While the shuttered, or discrete input mode of operation has not been utilized to demonstrate basic feasibility, it will be described later as a method for obtaining the required production throughput rates of 750 substrates/hour. The prime features used in the current AIME system are:

- High enough resolution to permit viewing and storing the entire substrate image.
- Large storage capacity with low lateral leakage.
- Use of high-speed computer-controlled electron beam scanning of selected portions of the stored image at zoom ratios suitable for adequate substrate evaluation.
- Operation at standard 525 TVL rates for compatibility with video recorders, displays, etc.

The electron optics of the RBV tube and external magnetic assembly provide outstanding aperture response over the entire sensing layer. Figure 4 includes the sine wave response characteristic or Modulation

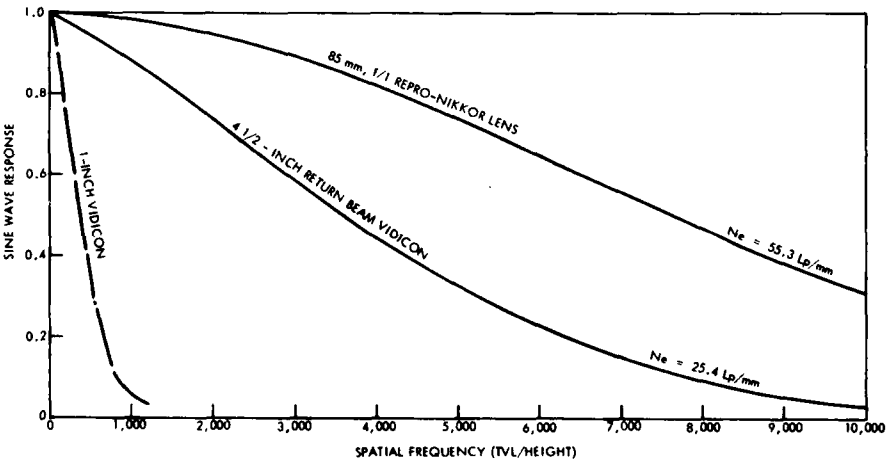


Figure 4. Sine Wave Response

Transfer Function (MTF) of the 4-1/2 inch RBV and also includes, for comparative purposes, the MTF of a standard 1-inch vidicon. The RBV provides approximately ten times the linear (equivalent to 100 times the area) resolution of standard TV sensors. The high resolving power of 100 line pairs/mm (10,000 TVL/RH) has been demonstrated over the entire sensing layer.

Figure 4 also contains a representative MTF for the lens which is used in the system. Note that its performance also is excellent, and this lens/RBV combination permits resolution of fine detail while viewing an entire 2-inch x 2-inch substrate and also provides a sequence of sub-images by means of electron-beam zoom and steering at a standard 525 TVL readout rate.

## Selection of Electronic Magnification

Selection of the electronic zoom ratio must be given careful consideration. High zoom ratio yields greatest image detail, but if excessive, can generate large amounts of superfluous data which slows down the substrate inspection rate.

Analysis of the RBV camera MTF with electronic zoom and video bandwidth filter is depicted in Figure 5. The increase in width of a given line image is shown as a function of zoom ratio.

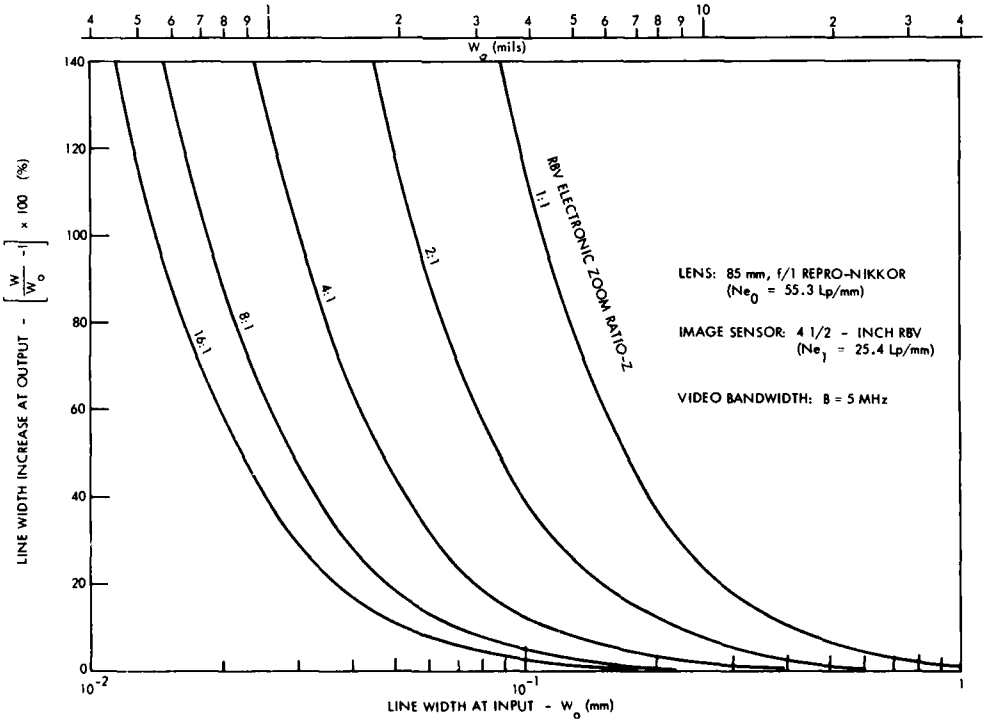


Figure 5. Line Image Fidelity of Video Chain

Examination of image detail population of Figures 2 and 3 and the image fidelity of Figure 5 results in the conclusion that:

- The presence of complete print patterns can be ascertained with full substrate imaging (1:1 zoom).
- Assessment of major faults will require approximately 3:1 zoom.
- Detail examination and classification of minute defects in critical areas will require approximately 10:1 zoom.

Photographs taken from a monitor of a 4-1/2 inch RBV camera imaging a 2" x 2" hybrid substrate with frontal illumination are shown in Figures 6, 7, and 8. These photographs represent zoom ratios of 1:1, 3:1, and 10:1 respectively.

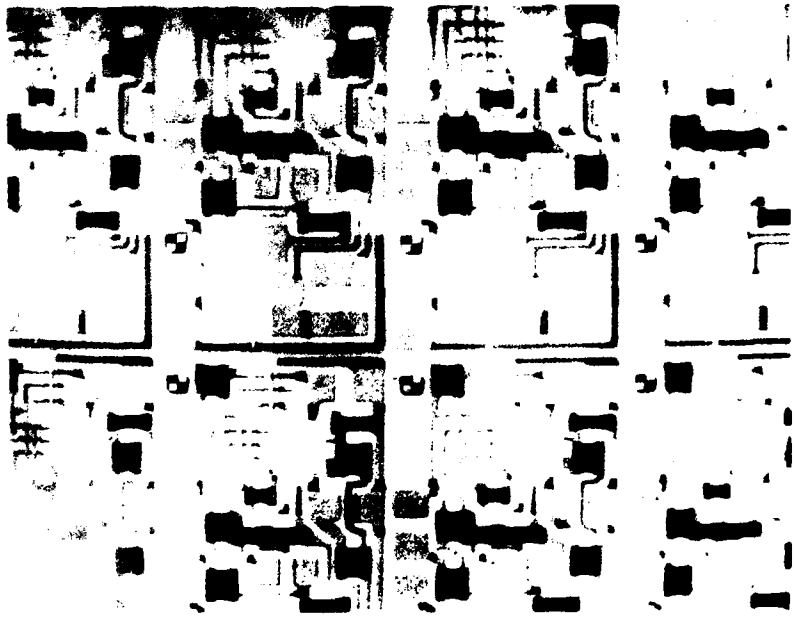

Figure 6. Hybrid Circuit Imaged by RBV - 1:1 Zoom

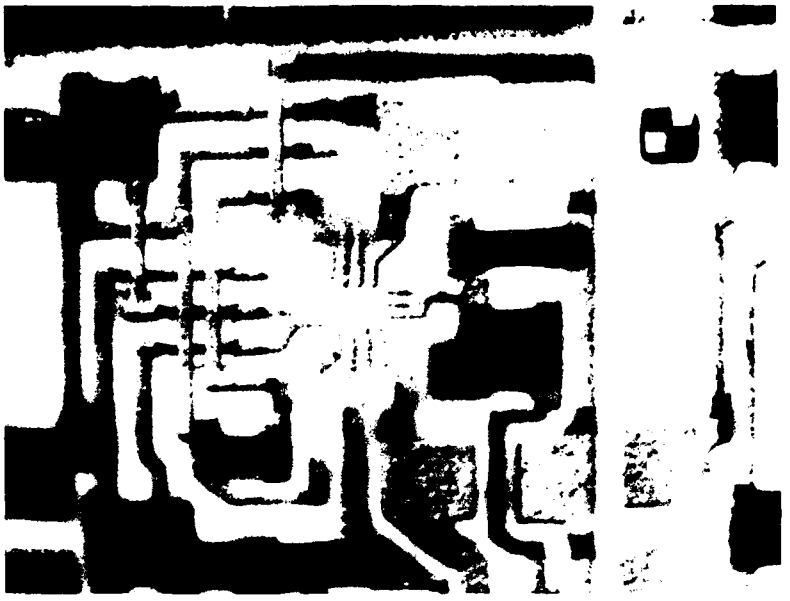

Figure 7. Hybrid Circuit Imaged by RBV - 3:1 Zoom

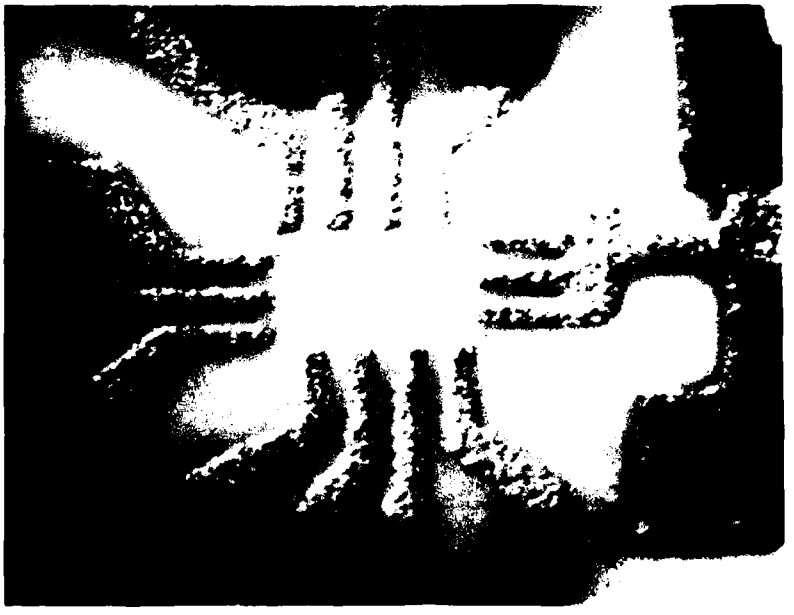

Figure 8. Hybrid Circuit Imaged by RBV - 10:1 Zoom

## System Operation

Figure 9 is a block diagram of the AIME System. The following description explains how the system is set up and used to perform inspections. The first step in the process is to record on the video disc a sequence of frames representing a fault-free substrate. During this recording process the selected zoom ratios, illumination, and sector for each frame are automatically stored in the computer. Then when the recording process is completed, a program is stored in the computer which will automatically perform this same sequence of operations during the inspection process.

With the recording process completed, the system is now prepared to inspect substrates automatically. The substrate to be inspected is placed in the holding fixture, and the inspection program is initiated. The program selects the desired track on the video recorder, and via the time base corrector, supplies this video to the video processor. Simultaneously, and synchronously, live video from the RBV camera is fed to the video processor.

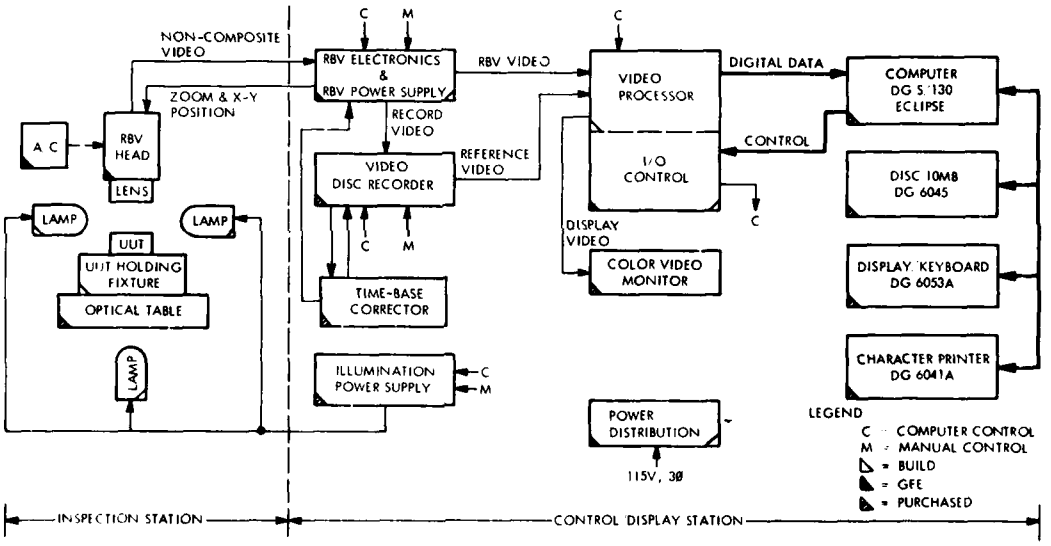


Figure 9. AIME System Block Diagram

The video output of the RBV, representing the unit under test (UUT) image, is compared to the stored reference image in real-time (1/30 sec). The difference data resulting from the comparison represents possible abnormalities. These data are sent to the computer system for final processing and a pass/fail decision. This comparative approach significantly reduces the data processed by the computer, thus maintaining a high inspection rate.

The video processor performs two functions. First, the difference between the RBV video signal and the video disc-recorder signal output is taken, digitized, and fed into the core memory of the AIME system computer. Second, the processor takes the same difference video signal and combines it with the RBV video signal which is then displayed on the color video monitor.

The RBV video signal appears as a black and white image on the monitor. The difference video is directed to the red and green gun-driver circuits. Thus, if the RBV image is wider than the recorded image, the green color-gun output is increased resulting in a highlighting of the greater than normal UUT area. A similar result is obtained if the UUT image is narrower than the recorded image, except now the red color-gun output is increased. If a defect is detected, the operator can observe the color-high-lighted defect on the monitor. When the inspection is complete, the AIME control respositions the RBV beam scan to the next UUT area to be inspected, and repeats the above process until the UUT inspection is completed.

Hybrid pre-cap inspection is performed in a semi-automatic mode with the operator visually observing the monitor and making the pass/fail decisions. For this mode the computer goes through the predetermined inspection steps in sequence, presenting on the monitor a view for the operator so that he can inspect the hybrid. The operator evaluates each view and presses a pass or fail key on the keyboard. This step-by-step process ensures an orderly and thorough inspection of the hybrid without the use of a microscope.

## AIME Software

The AIME System Software consists of the Data General Real-Time-Disc-Operating System (RDOS), the Command Line-Interpreter (CLI), the AIME Run-Time System, and various utility programs.

### Real-Time-Disc-Operating System (RDOS) and CLI

RDOS is a comprehensive and flexible operating system normally used with disc-based NOVA systems.

The Command Line Interpreter (CLI) is a dynamic interface to RDOS via the console and translates the input as commands to the operating system.

### Run-Time System

General. The AIME Run-Time System (ARTS) performs the functions of program generation, and test execution. It is written in a high level language (ALGOL) utilizing structured programming techniques to obtain modularization for ease of maintenance and understanding. Assembly language modules are minimized and used only where necessary for speed or special-purpose programming such as required in image processing.

Program generation can be accomplished either on-line or off-line. On-line program generation allows the user to try various setups for X-Y positions, zoom, illumination, etc. When a specific test setup is decided upon, the system software will remember, on operator command, the exact setup and will place the test setup in sequence with respect to other tests contained in a source file listing.

Test Program Generation. The test program generator is used to create automatic and semi-automatic test programs for substrates and pre-cap hybrids respectively. The operator can activate and control the system from the keyboard. Sectors have been designated for the user in positioning the sub-images on the monitor. The higher the zoom ratio, the greater the number of sectors. Sectors are square in shape and are numbered from left to right and from the top down. When a suitable image is seen on the monitor the operator initiates the following system actions: (1) Interrogation of all system status registers, and storage of the current setup data for the image, (2) the generation of a set of commands and related setup data, which when executed at a later date will result in the exact same setup conditions, (3) indexing and storage of the image on the video disc-recorder, (4) the generation of a MASK of the current image for the automatic test program.

Mask Generation. The mask generator (software module MASKGEN) is used to generate a mask for each reference image operating in the automatic mode. Where an etch boundary exists, the mask consists of a block of '0's with '1's elsewhere. The width of the block of '0's is of sufficient magnitude to mask out offset and registration errors. The resultant mask is read into the computer memory and "AND"ed with the difference video data. The resultant data are then ready for the image processing.

## Image Processing

The image processing algorithm analyzes the masked video difference data to render a pass/fail decision on a substrate. In order to achieve the processing rate of 750 substrates/hour, the following detection scheme has been developed. The 240 thousand bits of masked difference data are divided into a matrix of 930 clusters. Each cluster's density is then examined to determine if a defect exists. The defect's location is then recorded and reported on the line printer for a hard copy.

## Hardware Description

A photograph of the AIME system, shown in Figure 10 consists of two major elements; the Control/Display Station and the Inspection Station. A magnified image of an actual hybrid substrate can be seen on the video display.

## Inspection Station

The inspection station consists of a shrouded structure on an air-suspension optical table as shown in Figure 11. A precision, 3-axis, adjustable holding fixture registers the hybrid susbstrate orthogonally to the RBV optical axis. The RBV is held rigidly to the table and external cooling air is ducted to the assembly to preclude vibrations, and a positive internal shroud pressure maintains a dust free atmosphere.

Two illuminators are located $180^{o}$ apart and the defocused filament is imaged via folding mirrors to provide frontal illumination for pre-cap inspection. A third illuminator, located on the optical table, is provided to produce back lighting for print inspection. Light from this illumination is folded $90^{o}$ by locating a mirror beneath the holding fixture. The

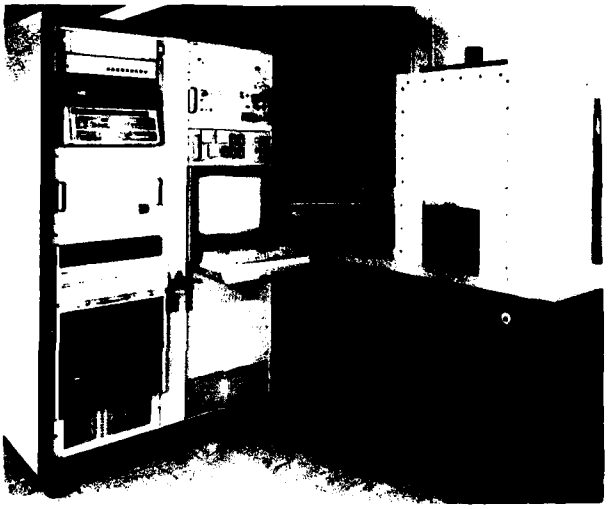

Figure 10. AIME System

hybrid is held in precision alignment against three reference points with a back plane vacuum around the edges, providing a central open area for the back illumination.

## Control/Display Station

The Control/Display Station consists of a double rack assembly. One of the two major functions performed by this station is control of the AIME operating modes. This control is maintained by the computer and associated peripherals.

The remaining elements of the Control/Display station are associated with the RBV and Video Processor. These include the video disc-recorder, sync generator, time-base corrector, color video monitor, and illumination power supplies.

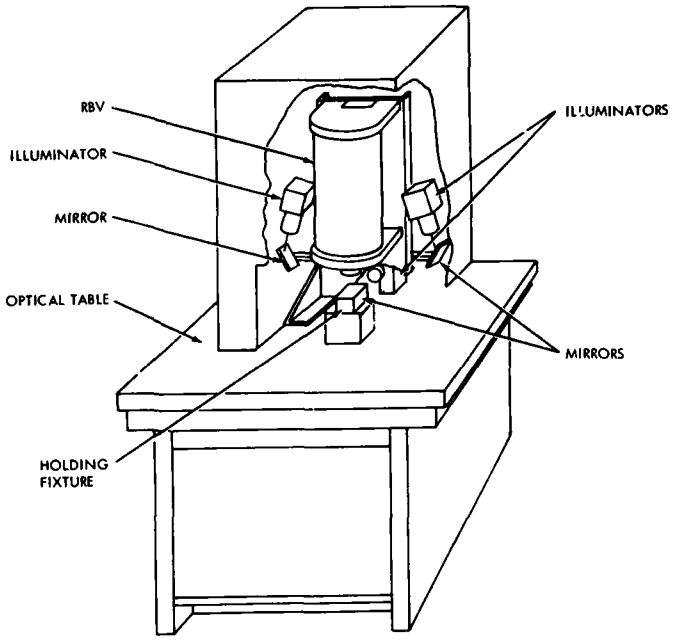


Figure 11. Inspection Station

The AIME system can be controlled either with the computer and associated interface (CPU control), or with controls located on the front panels of the RBV electronics chassis, the video processor chassis, and the video-disc recorder.

## High Speed Inspection Technique

The AIME system described in this paper demonstrated the feasibility of using the high resolution RBV to image an entire substrate and produce sub-images for evaluation by means of electronic zoom and steering. Continuous 525 TVL readout with steady state exposure was used since a standard rate display, time base corrector and video recorder could be used for demonstration. High speed operation for complete substrate evaluation at rates of 750 substrates/hour, however, cannot be achieved with this mode.

The 750 substrate/hour requirement can be achieved by operating the RBV camera in a "Snap Shot" mode. The timing diagram in Figure 12 illustrates the timing sequence using a controlled shutter exposure followed by sequential readout of 33 discrete image areas selected from the stored image on the RBV target. After readout of the entire substrate image in 1.1 sec., the target is then prepared by an erase and prime cycle for the next exposure while a second hybrid UUT is positioned prior to exposure. The entire cycle is completed in 4.8 sec. and is compatible with the data handling rate of the computer for image analysis.

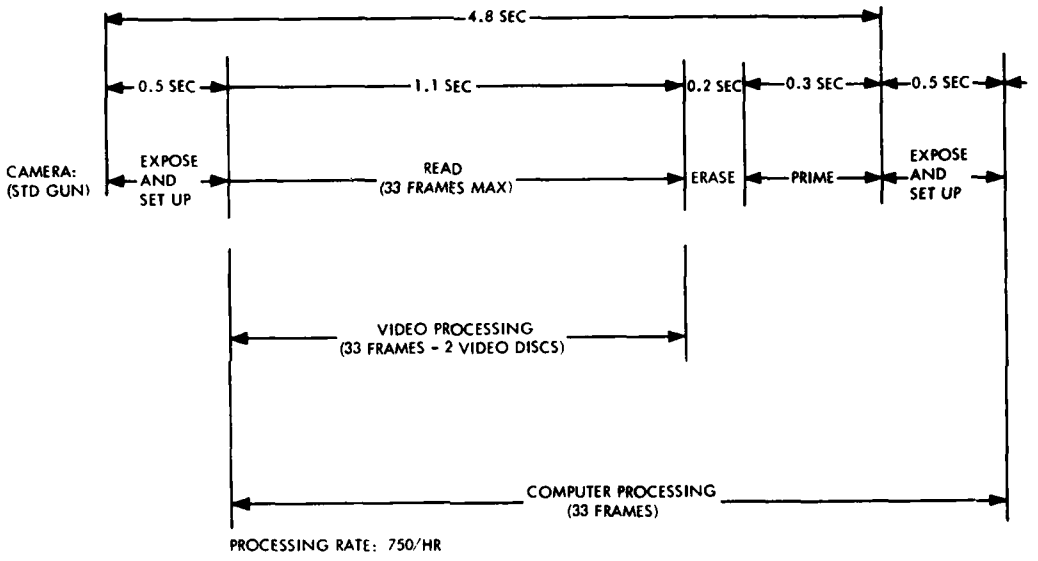


Figure 12. AIME Snap Shot Mode Timing

## Fault Detection

The evaluation of the AIME system capability to detect faults on printed substrates consisted in the testing of twelve (12) substrates containing faults typical of those found in the manufacturing process. The substrate chosen as the evaluation model is shown in Figure 13. Line widths represented are 4, 6, 8, and 10 mils. Faults contained on the twelve (12) defective substrates include breaks in the printed path, excessive ink along a printed path, necking down or narrowing of the printed path and shorts between two printed paths.

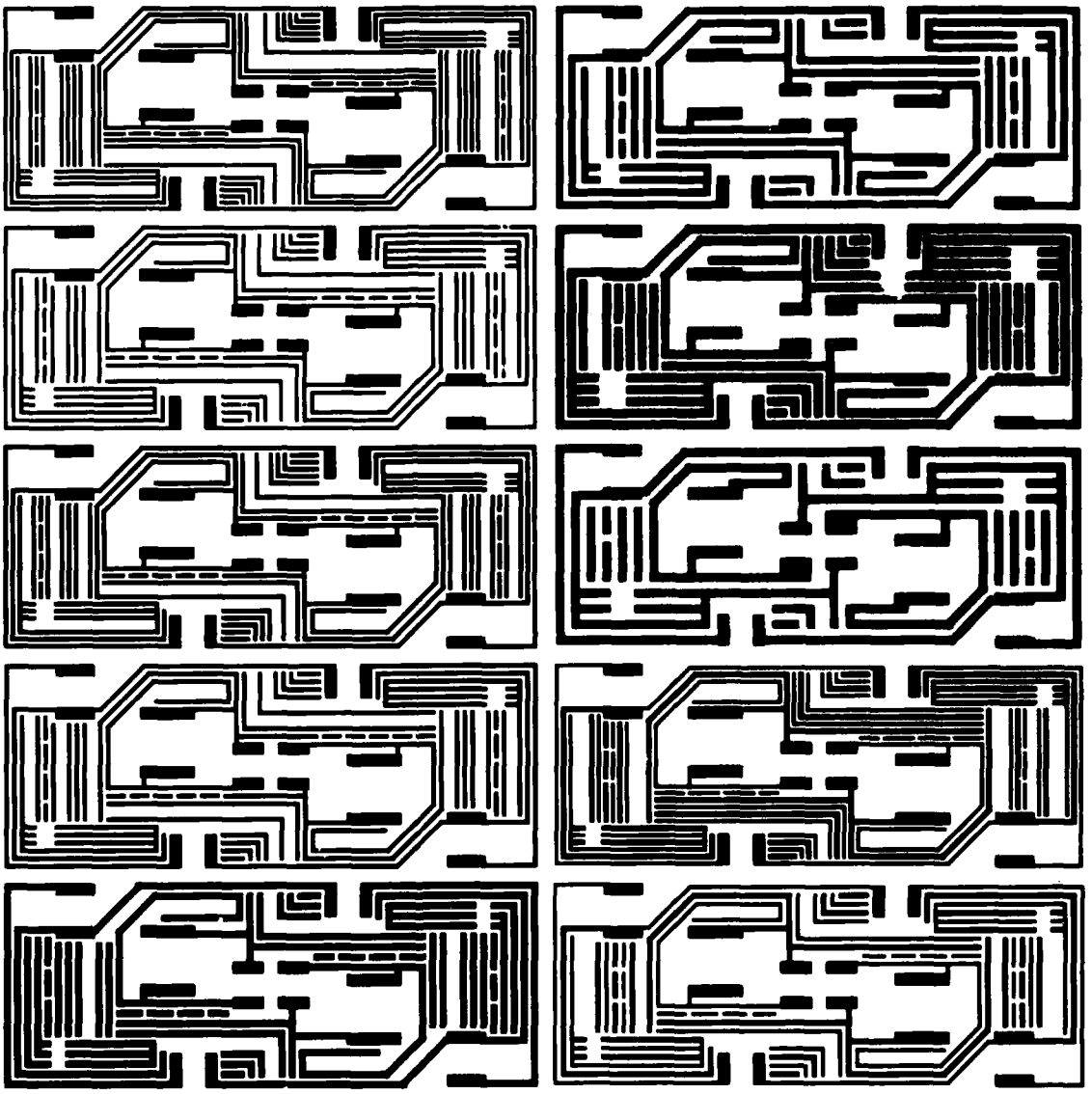

Figure 13. Sample Substrate Used as Evaluation Model

AIME is programmed to automatically test substrates in the zoom 10 mode of image magnification. In this mode of magnification the substrate is recorded or examined in 49 separate sectors. In addition each sector is electronically subdivided and evaluated as a 26 x 30 matrix of subsectors. Should a defect be detected, the row and column of the substrate containing the defect is printed on the AIME printer. In the event of multiple defects within a sector, the largest defect is reported.

At the start of testing, each of the substrates was individually inspected by the test operator using AIME in the manual mode of operation. The defects visually detected by the test operator were then recorded on a printed enlargement of the substrate layout. A defect free "Master" substrate was then recorded by AIME in the automatic mode and a "go-chain" test was made in which the recorded substrate image was compared with the actual "Master" substrate. This test verified the proper operation of AIME.

Each defective substrate was then evaluated by AIME. AIME was programmed to operate in the automatic mode with the verification flag set so that the test operator could confirm the defect detected by AIME. Mechanical realignment of the substrate was performed during the test as required by the test operator to minimize misalignment between the substrate and the "Master" recorded image. The defects detected by AIME were automatically printed on the AIME printer and were also manually recorded by the test operator on data sheets.

Each defect on a substrate was classified as to size. Three size classifications were used; 0-3 mils (small), 3-6 mils (medium), and greater than 6 mils. The defect size was noted on the data sheets. In this manner it was possible to subjectively judge the ability of AIME to detect different sized defects. The results of the AIME demonstration system to detect defects of varying size are summarized in Table 1. These results indicate that overall AIME successfully detected 96.4 percent of the substrate defects. AIME succesfully detected 100 percent of the substrate defects size 3 mils or larger and 81 percent of the substrate defects less than 3 mils. The calculated percentages were determined by the formula.

$$\frac{\text{(Type or Total) Defects Detected}}{\text{Total Number of Defects}} \times 100 = \text{Percent Detected}$$

The total number of defects is the number of defects per substrate less defects in excess of 1 per sector. AIME will detect the largest defect in a sector; therefore, it is inappropriate to include more than one defect per sector in the above calculations.

Table 1. Summary of AIME Data

| Substrate Number | Total Defects | 0-3 Mil Defects | 3-6 Mil Defects | >6 Mil Defects | Total Detected | 0-3 Mil Detected | 3-6 Mil Detected | >6 Mil Detected | Defects Missed |
|---|---|---|---|---|---|---|---|---|---|
| 2A1 | 24 | 5 | 7 | 12 | 24 | 5 | 7 | 12 | 0 |
| 3A1 | 33 | 6 | 14 | 13 | 30 | 3 | 14 | 13 | 3 |
| 3A2 | 26 | 1 | 8 | 17 | 26 | 1 | 6 | 17 | 0 |
| 4A1 | 34 | 2 | 15 | 17 | 34 | 2 | 15 | 17 | 0 |
| 4A2 | 30 | 0 | 13 | 17 | 30 | 0 | 13 | 17 | 0 |
| 5A1 | 19 | 12 | 6 | 1 | 16 | 9 | 6 | 1 | 3 |
| 5A2 | 16 | 10 | 6 | 0 | 15 | 9 | 6 | 0 | 1 |
| 5A1 | 22 | 2 | 10 | 10 | 22 | 2 | 10 | 10 | 0 |
| 6A2 | 20 | 4 | 9 | 7 | 20 | 4 | 9 | 7 | 0 |
| 7A1 | 36 | 11 | 15 | 10 | 35 | 10 | 15 | 10 | 1 |
| 8A1 | 35 | 4 | 13 | 18 | 34 | 3 | 13 | 18 | 1 |
| 8A2 | 36 | 6 | 20 | 10 | 33 | 3 | 20 | 10 | 3 |
| Total | 331 | 63 | 136 | 132 | 319 | 51 | 136 | 132 | 12 |

## Conclusions

Feasibility of a computer controlled high resolution television system for automatic inspection of hybrid substrates has been demonstrated. The following achievements were validated on this program:

- Automatic detection of line widths varying from 3 mils to 10 mils.
- Automatic detection of opens and shorts varying from 1 mil to 10 mils.
- Computer controlled beam steering and raster zoom for high speed processing.
- Video display with color augmentation for visual analysis of substrate faults.

- Hardware functional compatibility demonstrating real-time video comparison technique.

- Validation of software algorithms for automatic program sequence control and fault processing.

Pre-cap inspection of hybrid assemblies utilizing the display has been useful in verifying the location and bonding of chips and the placement of wire bonds. However, integrity of the wire bonding and wire crossover cannot be fully evaluated without a stereoscopic view to provide depth perception.

The results of this program provide the basis for product design of an automatic high speed inspection system using other high resolution, wide format imaging tubes and storage techniques such as digital memories.

## Acknowledgment

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# COMPUTER AIDED MANUFACTURING OF HYBRID MICROCIRCUITS

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## I. INTRODUCTION

The use of hybrid microcircuits in military systems has been growing at an accelerated pace for a long time. When measured by sheer volume, the use of hybrids has grown even more dramatically in the non-military market. The number of hybrid circuits used in watches, toys, and automotive applications is mind-boggling.

Unfortunately, military hybrid circuits have acquired a reputation for high cost. The applications of hybrids in DOD systems would be even more widespread were it not for this fact. It is the purpose of this paper to describe an approach to the hybrid business which is having now and will have in the future a profound effect on the overall cost of hybrid microcircuits - specifically, the application of computer aided techniques to the various aspects of hybrid design - manufacturing - test - inspection operations. Also, we will describe our internal company program for which we have coined the term WICAM - Westinghouse Integrated Computer Aided Management. We will discuss the status of our program at present and show how we intend to achieve the fully integrated system.

Several of the specific improvements we have achieved, and which will further improve with time are:

1). Improved yield.
2). Fewer design errors.
3), Lower labor costs.
4). Improved production control.
5). Improved management through better real-time information.

Today at Westinghouse we are making wide use of numerically controlled or computer controlled equipment in every facet of our hybrid business. However, many of the equipments are manually programmed, and the inputs to the machines are re-entered time after time. As you will see, our ultimate goal is to create a data base during the initial computer aided design, and then to operate our business by computer aided manipulation of that data base. Figure 1 graphically depicts our WICAM concept.

## II. COMPUTER AIDED DESIGN AND MANUFACTURING OF HYBRID CIRCUITS AT WESTINGHOUSE TODAY

### A). Hybrid Design & Artwork Generation.

The mechanical design of hybrids at Westinghouse until recently was done principally by manual methods. Component placement and conductor routing were entirely manual, with several iteractions being required for most circuits, depending on the skill and sophistication of the person doing the layout. The electrical design of digital circuits has been augmented by computer simulation programs for several years. Analog circuit design has been aided through the use of purchased or time-shared computer programs.

At present, there is a concerted effort to design hybrids through CAD as much as the state-of-the-art allows. This is being done using a stand-alone interactive graphics system which has been in use at Westinghouse for several years (Figure 2). The system is being expanded to include design activities other than hybrids. The system provides Westinghouse with powerful analytical as well as design tools and greatly extends the effectiveness of the Engineering Department. The designer is able to create a design from start to finish without ever using pencil and paper. In addition, an engineer is able to enter the fundamentals of a design into the computer, and to have the design refined and embellished by another designer or draftsman. This then frees the principal from detailing considerations and allows his talent to be used in a much more effective way.

### B). Hybrid Substrate Fabrication.

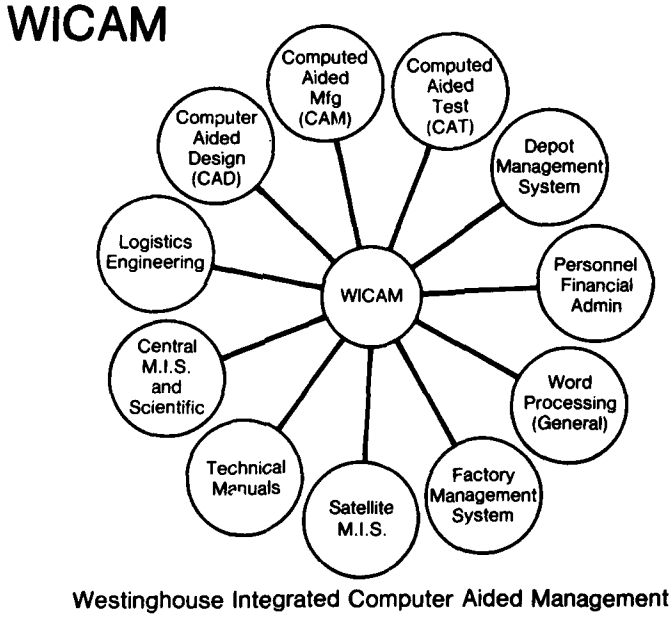
The following NC or computerized equipment is in use today at Westinghouse for hybrid substrate fabrication: a semi-automatic programmable screenprinter, an NC programmed layer for drilling and machining substrates, a computer controlled laser trimmer, a computer controlled two-point probe tester, and a computer controlled multipoint circuit checker. At present, all of these equipments are programmed somewhat laboriously using some sort of human controlled input.

### C). Hybrid Assembly Operations.

Because of the small production lots of many different kinds of hybrids, Westinghouse has not yet implemented automatic package handling and chip mounting. The assemblies are handled one at a time, manually. We are now using an automatic wire bonder, for a particular device, the BORAM memory module, which has potential for high volume. We are presently conducting production feasibility studies of tape automated bonding for this same device using a laboratory bonder (Figure 3). A production tape automated bonder will be received soon. Also, we use an automatic temperature cycling equipment for environmental screening of assembled hybrids. Again, all of these equipments are programmed manually.

D). Test and Inspection.

Figure 4 illustrates a dynamic laser trimmer being used for dynamic test and trim of power regulator hybrids at Westinghouse. We also use automatic digital testers for testing digital hybrids. These testers are the only equipments in our arsenal of NC and CNC equipment whose test programs are generated automatically from the circuit design data. We have been investigating optical video comparators for substrate inspection. We are devoting much effort to development of automatic inspection procedures, but as yet have had not been able to introduce them into production.




Westinghouse Integrated Computer Aided Management

Figure 1

## III. FUTURE COMPUTER AIDED HYBRID MICROCIRCUIT MANUFACTURING

Hybrid microcircuits are becoming increasingly more complex while production costs such as labor, material, facilities, etc. continue to escalate at alarming rates. Both of these factors emphasize the dire need to achieve substantial productivity improvements in order to continue delivering reliable products at affordable prices. At Westinghouse, this need is being addressed by a major Productivity Improvement Program aimed at the development and implementation of a fully Integrated Computer Aided Management (WICAM) system. The key to this system's success is controlled integration because WICAM (Figure 1) encompasses every facet of the Defense and Electronic Systems Center's business. Three of the WICAM functions (Computer Aided Engineering, the Operations Business System, and Factory Automation)are directly related to product delivery and are, therefore, major thrust areas of this Productivity Improvement Program. These functions and their inter-relationships are illustrated in Figure 5.

Computer Aided Engineering efforts (Figure 6) are focused on the development of a comprehensive Interactive Graphics network for product design as well as design analysis. A communications link from the graphics network to a dedicated Engineering host mainframe provides expanded capability to perform more complex design analysis. The host mainframe also provides a convenient repository for storing the product design data base as well as the capability to maintain configuration control of the product design data. Obviously, a number of safeguards must be incorporated into the system to prevent unauthorized access to or modification of the product design data. This is accomplished by means of a multi-level passwork system and write locks on the data.

The Operations Business System (Figure 7) utilizes a second host mainframe dedicated to the functions of Production Planning, Material Management, and Shop Floor Control. This is primarily a management visibility system which contains modules to perform Material Requirements Planning, Inventory Status Monitoring, Factory Scheduling, and Shop Floor Tracking.

Both of the preceding systems are being developed to encompass the needs of the entire product spectrum including, but not limited to, hybrid microcircuits. Factory Automation, the third major thrust area, is being developed using a different philosophy. Many Defense Electronic Factories are typically low volume, high product mix, discrete part, batch manufacturing facilities composed of a number of distinct functions which may be generically categorized into unique commodity groups (i.e., Mechanical Fabrication and Assembly, Printed Wiring Board Fabrication and Assembly, Hybrid Microcircuit Fabrication and Assembly, etc.). There exists a large degree of commonality in the data flow requirements within each commodity group, however, the data formats, data content, and computational capability requirements differ significantly from one commodity group to another. This blend of commonality yet uniqueness has led to the definition of a "standard" computer and communications architecture for Factory Automation Centers which are being

implemented on a commodity group basis. Each commodity group's Factory Automation Center (Figure 8) performs the same basic functions, Process Planning and Process Control. The primary differences between centers are the number of computers installed and the specific process control functions being implemented.

Process Planning, not to be confused with Production Planning, is the basis of all manufacturing and can be equated to a roadmap which shows the specific route that must be followed in order to transform raw materials into finished product. Computer Aided Process Planning (CAPP) minimizes human involvement in the development of these roadmaps by utilizing intelligence that has been captured and incorporated into the planning system. By using decision trees, decision tables, etc.; a series of questions can be asked by a computer with the answers being used for formulate a unique process plan which makes optimum use of available resources. Thus, shop routings can be generaged directly from the product design data base.

The second aspect of factory automation, process control, differs significantly between commodity groups with respect to specific application needs. In general, this is a multi-level hierarchial system with the factory automation processor (top level) augmented by a manufacturing interactive graphics system, being used to transform the product design information into the specific data sets required for control of each automated process (lower level) within a commodity group. Information relative to process performance is automatically captured on an exception reporting basis by the factory automation processor and used for trend analysis, yield analysis, etc. in order to fine tune the various processes for optimum product throughput and yield.

In the hybrid microcircuit area, a number of significant development programs are currently underway which can be categorized as Computer Aided Manufacturing (CAM), Computer Aided Test (CAT), Computer Aided Inspection (CAI), or an integrated composite of CAM-CAT-CAI functions simply called a Process Control System. An example of the latter is a program to develop an automated imaging system for the production of hybrid film masks. This system is centered around a laser artwork generator (LAG) Figure 9, and utilizes automated material handling as well as automated film processing and laser-based inspection equipment to significantly improve process yields and throughput. Further down the road we envision using the LAG to generate thick film circuits directly on the substrates. Other study programs currently in-process include: potential robotics applications for both substrate fabrication and complex assembly operations, an automated material identification and recognition system, automated material movement systems, and advanced data communications concepts for ultra high speed, error-free information exchange.

As stated earlier, the key to success for WICAM is controlled integration and this is particularly true with respect to the three WICAM modules currently being discussed. Controlled integration of Computer Aided Engineering, the Operations Business System, and Factory Automation will permit

real-time information exchange between these modules and this is an absolute necessity to achieve the projected productivity improvements. For example, the moment a product design is complete, the engineer should be able to transmit the design information to the CAPP system and within minutes receive an estimated manufacturing cost (CAPP + work measurement) to compare with his design to cost target. Helpful tips for design modification to reduce manufacturing costs should also be available. Another example: The Operations Business System will permit rescheduling the entire factory on a daily basis. Changes to the master schedules (delivery schedules) daily factory performance (operations completed), material availability and facilities status (equipment availability and capacity) will be available and will depict the current situation in order to use available resources optimally to meet product delivery committments. Finally, the degree of factory automation is increasing at a rapid rate which translates into an ability to manufacture greater product volumes in shorter time spans.. Engineering change activity for our business remains high compared to traditional product transition curves (transferring the design from Engineering to Manufacturing). Combining both factors, Factory Automation plus Engineering change activity, results in a significantly increased scrap or rework rate which is contrary to the product improvement goals. With WICAM, we have the ability to react immediately to design changes and significantly improve our productivity.

In summary, we have described the Westinghouse approach to computer aided manufacturing of hybrids and have described the Westinghouse philosophy and approach to achieving a much higher level of computer integration than we currently enjoy.

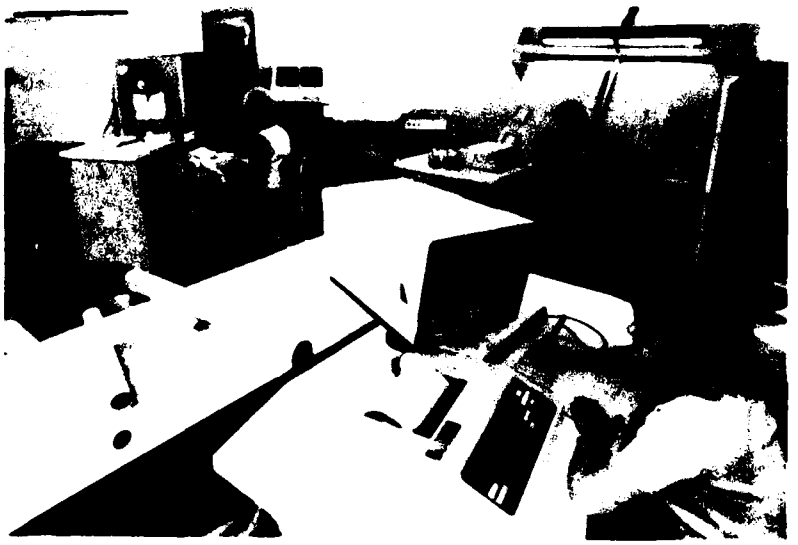


Figure 2

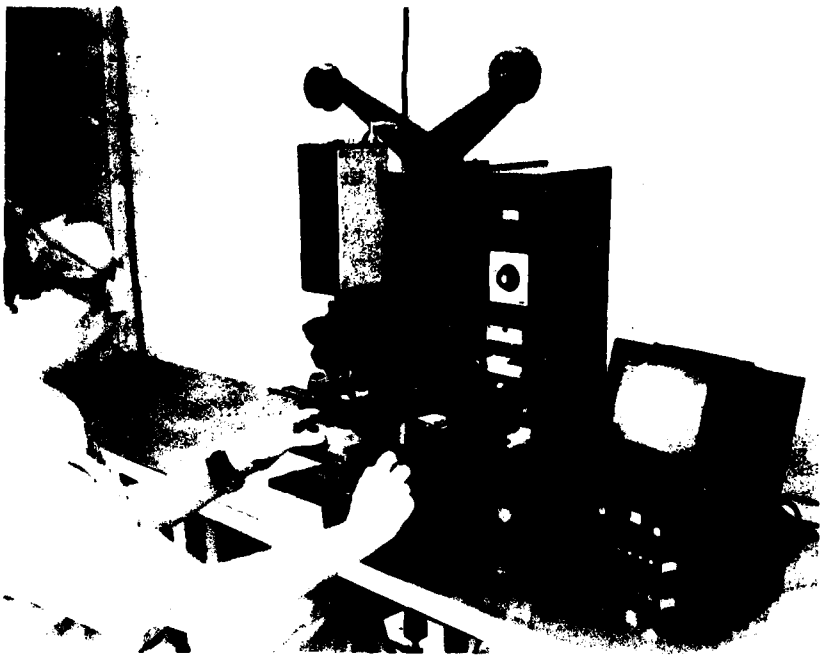


Figure 3

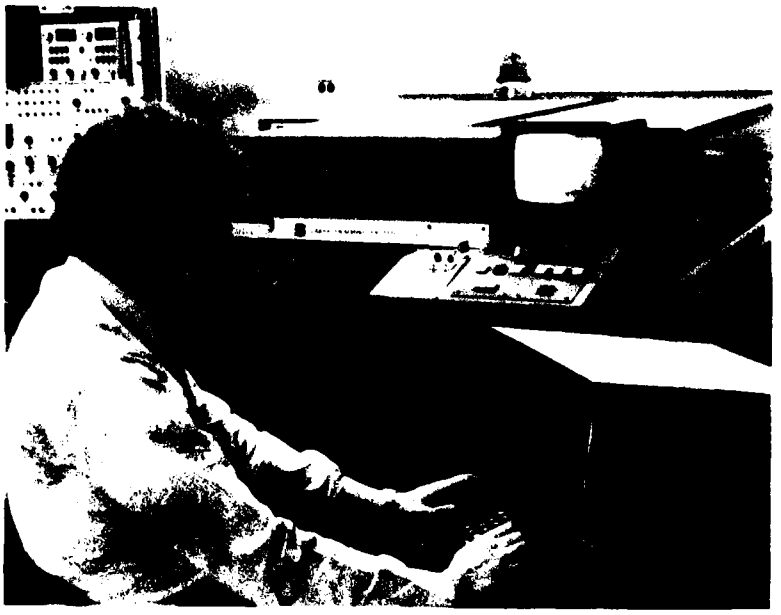


Figure 4

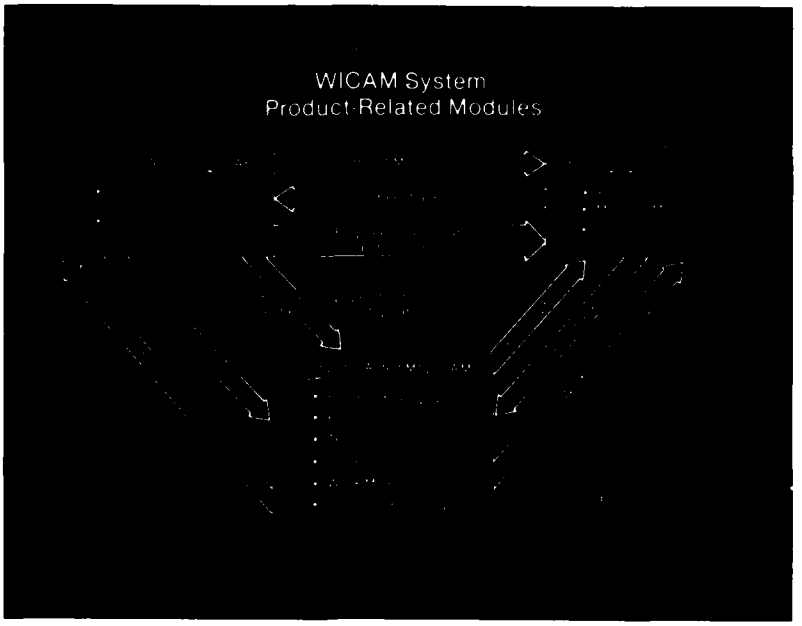



Figure 5

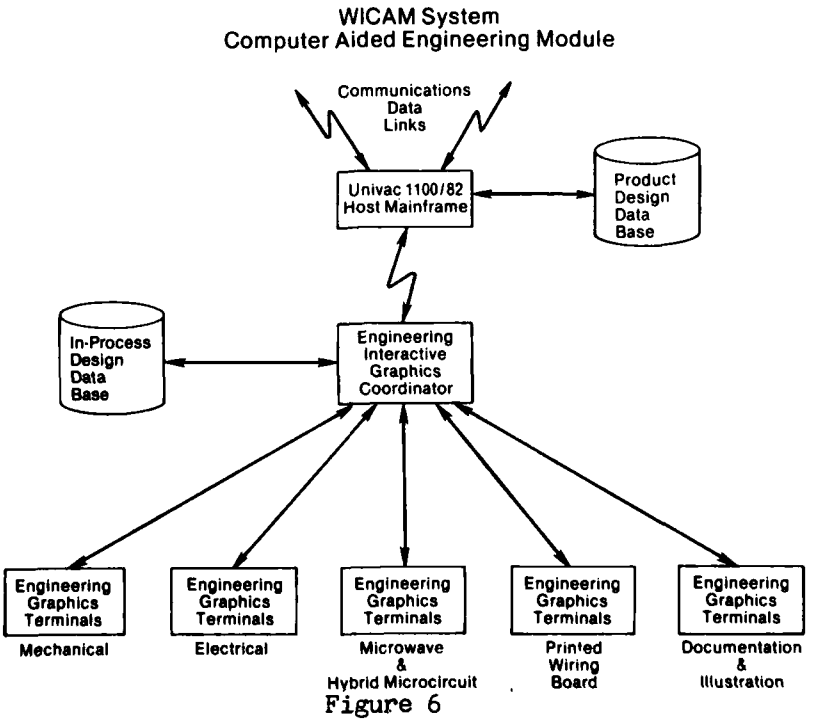



Figure 6

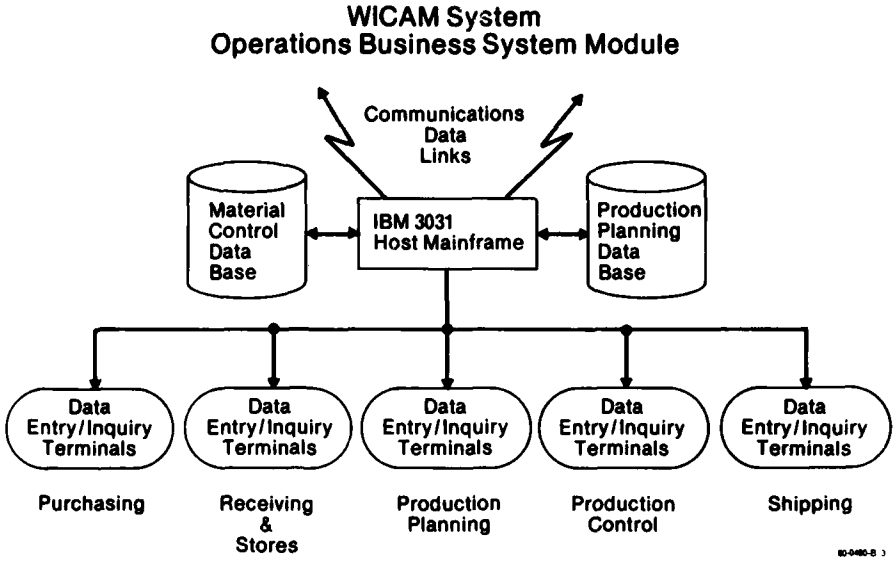



Figure 7

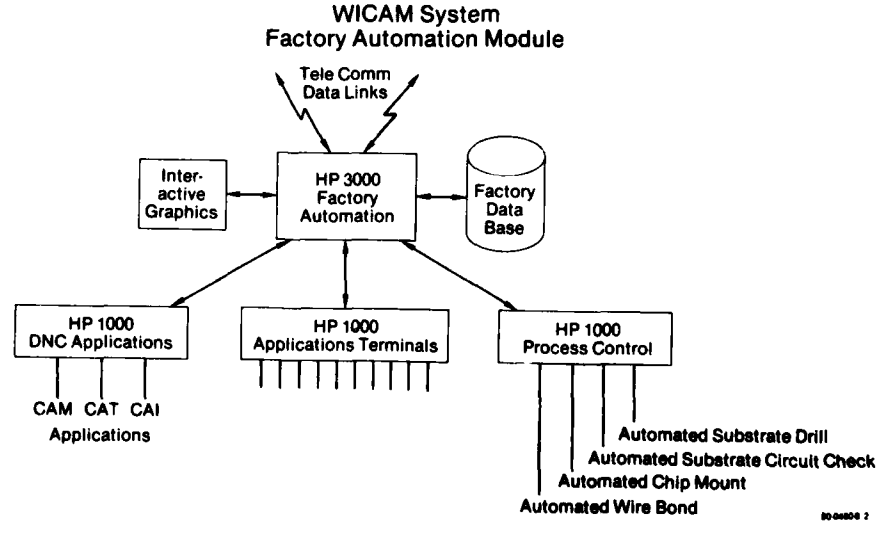



Figure 8

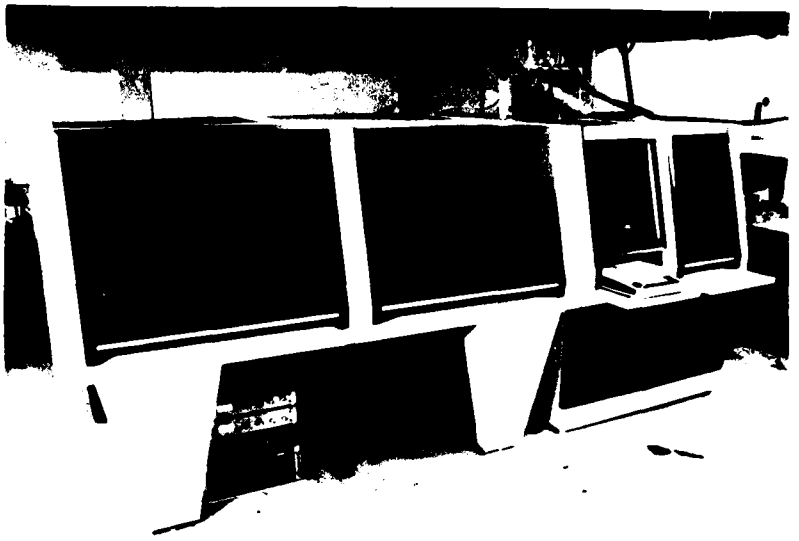


Figure 9

# HYBRID TCVCXO DESIGN AND FABRICATION

BY

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## ABSTRACT

This paper describes the hybrid design, package design, and fabrication of a microcircuit temperature-compensated voltage - controlled crystal oscillator (TCVCXO). The oscillator was required to have high accuracy ($\pm$5 ppm) over a relatively wide temperature range (-40°C to +75°C).

The basic electrical design will be discussed, as well as component selection, hybrid technology selection, and packaging tradeoffs. The fabrication and assembly process flow will be analyzed and will include a discussion of the functional trimming required to obtain the temperature compensation and high accuracy output.

Problems encountered, and the solutions implemented, in the design, fabrication, functional trimming, and packaging of these microcircuits will be addressed.

## TCVCXO FUNCTIONAL DESCRIPTION

There is a need for small stable, accurate, modulated oscillators capable of operating over reasonably wide temperature ranges. The hybrid microcircuit Temperature-Compensated-Voltage Controlled-Crystal Oscillator (TCVCXO) described herein satisfies these requirements. Table I lists the major operational electrical specifications to be met by this circuit module.

As shown in the block diagram of Figure 1, the TCVCXO has six main circuit areas:

1. The voltage regulator provides nine volts to the circuit and must be capable of supplying up to 1 mA of current for external use.

2. The thermometer, which is a buffered forward biased silicon diode, generates a voltage linearly proportional to temperature.

3. The diode function generator transforms the linear voltage-temperature curve of the thermometer into a six segment cubic function that modulates the oscillator and compensates for the expected crystal frequency-temperature variations. Thus the output frequency versus

Table I. TCVCXO Electrical Specifications

| | | |
|---|---|---|
| • | Center Frequency | 21.9375 MHz |
| • | Overall Frequency Tolerance | ±5 ppm |
| • | Temperature Range | $-40^{o}C$ to $+ 75^{o}C$ |
| • | Single Power Supply | +10 Vdc to +16 Vdc (Nominal + 12 Vdc) |
| • | Power Supply Current Drain | 4 mA Max |
| • | Analog Deviation Sensitivity | 500 Hz per Volt ±8% |
| • | Regulated DC Output | 9V ±20 mV |

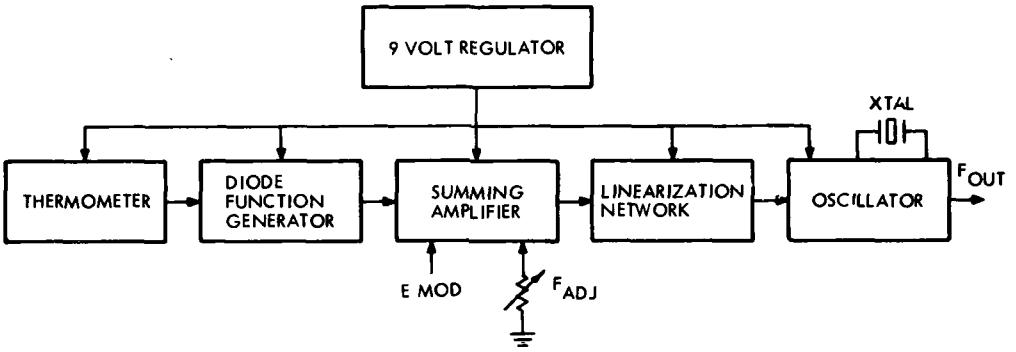


Figure 1. TCVCXO Block Diagram

temperature of the oscillator is kept within its 2 ppm error budget. This is required in order to keep the oscillator within the 5 ppm tolerance for all permitted variations of temperature, supply voltage, load, shock, aging, etc.

4. The oscillator contains a voltage-variable capacitance (varactor diode) in series with the crystal. The output frequency is modulated by varying the voltage applied across the varactor diode.

5. The linearization network compensates for the nonlinear relationship between output frequency and applied voltage and is a diode function generator which produces a two-segment voltage transfer characteristic having a nonlinearity approximately the reverse of the oscillator's frequency/voltage tuning characteristic. Thus, linearization to better than five percent over a deviation range of 100 ppm and better than one percent over a range of 40 ppm is achieved.

6. The summing amplifier accepts the combination of stimuli from the temperature compensation function generator, the analog modulation signal, and a frequency adjust potentiometer that sets the nominal center frequency, and feeds the resultant signal to the oscillator through the linearization network.

The schematic for the TCXCXO is shown in Figure 2. In the version of the system discussed here, the circuit is subdivided into two hybrid modules. The TCFG module contains the thermometer (CR1) and buffer amplifier (U1) and the diode function generator for producing a cubic voltage-temperature curve. The VCXO module contains the summing amplifier (U5), the linearization function generator, the nine volt regulator and the oscillator. The crystal and the frequency adjust potentiometer are mounted external to the VCXO and the entire unit is placed into a shell and encapsulated in potting material.

## HYBRID DESIGN

### Technology

The TCVCXO module required extremely dense hybrid packaging (based on the program defined electrical circuit design and outside mechanical configuration). The circuitry to be packaged included 105 resistors, 10 capacitors, 22 semiconductor devices, a crystal and a potentiometer. The total volume of the required truncated cylinder configuration was less than 0.85 cubic inches, a large percentage of which was unusable due to the irregular shape. The hybrid technology chosen to satisfy these requirements was to use semiconductor dice, chip and wire bonded to a thick film resistor-conductor network.

### Packaging

The module consists of two hermetically-sealed hybrid microcircuits bonded back-to-back, having a crystal and a potentiometer attached externally, and then potted with a low density epoxy into a diallyl phthalate potting shell. The substrate size for each hybrid is 0.90" x 1.515", and hermetic sealing is accomplished by using alumina ceramic corrals and stepped metal lids. Fabricating the corral assembly involves brazing (at about 800$^{o}$C) a metal (Kovar) frame to a metallized ceramic corral so as to render the corral weldable. After brazing, the exposed metal surfaces of the assembly are gold-plated to prevent oxidation during the glass sealing operation. The corral assembly is depicted in Figure 3. This corral assembly is then glass sealed to the thick film network, and a Kovar cover is subsequently seam-sealed to the Kovar frame on the corral. The approach selected for encapsulating the module assembly to the required form factor is to insert the module assembly into a potting shell and back fill the shell with a low density epoxy, so as to meet the weight specification. A completed module in a potting shell is pictured in Figure 4.

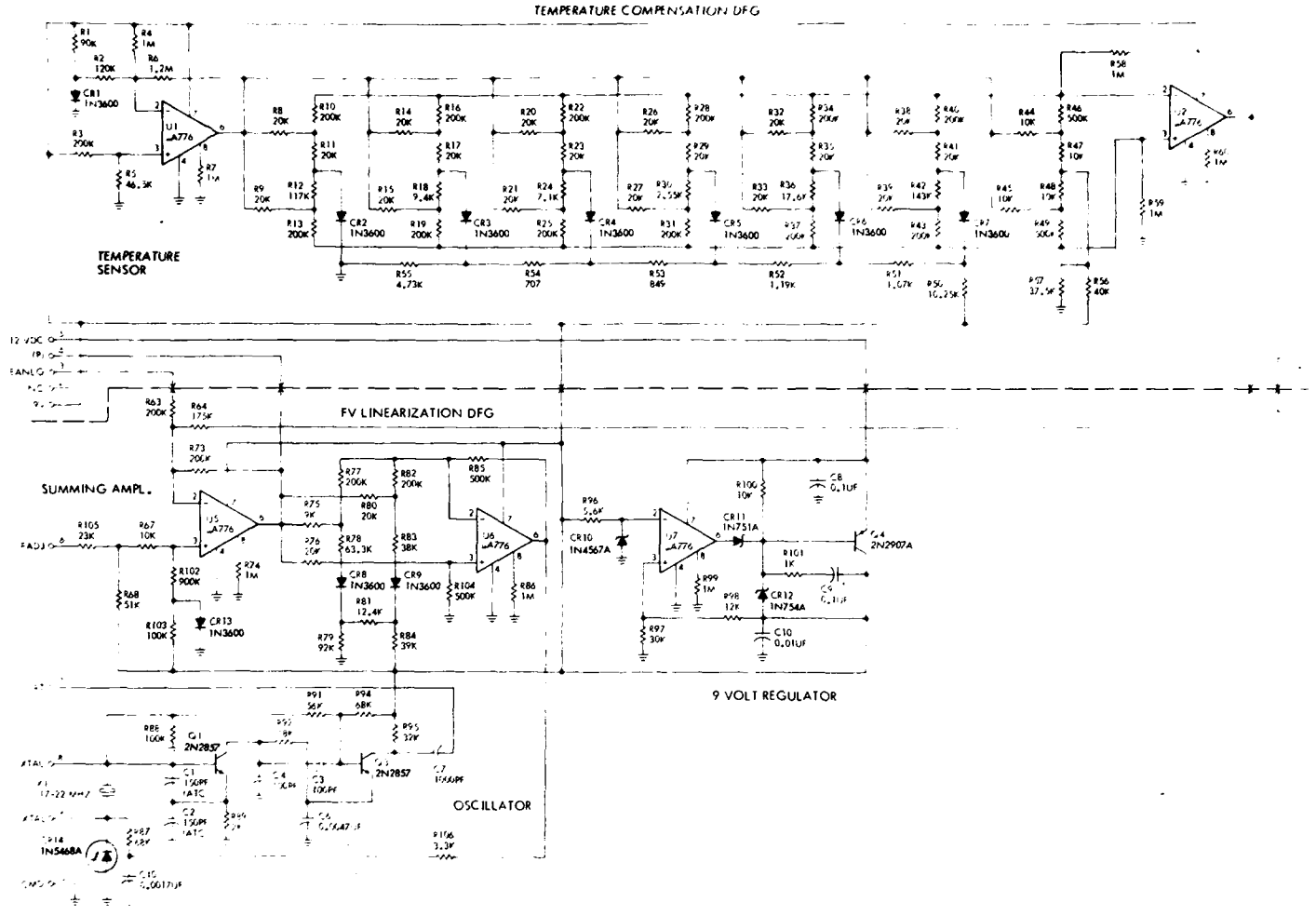


Figure 2. TCVCXO Schematic

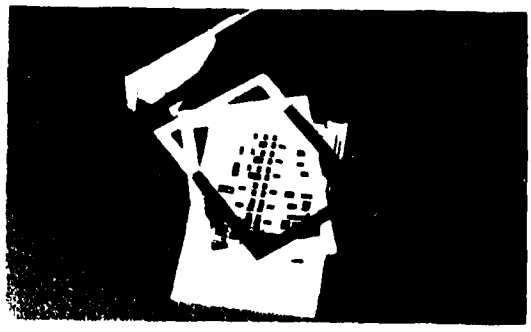

Figure 3. Corral Assembly

Figure 4. Completed Module In Potting Shell

Component Selection

The 105 resistors are all thick film screened resistors, accomplished by the use of four different resistivity pastes on each substrate. The bulk of the resistors are only 0.025" wide due to the density of the layouts. The resistors requiring active trim are somewhat larger to provide adequate trim range, and those requiring a wide trim range are of a top hat configuration.

The semiconductors are used in chip configuration, eutectically die bonded and gold wire-bonded to the network. Some of the diode and transistor devices were initially beam-lead configuration, but were changed to chip and wire due to availability and assembly processing problems. The capacitors were all used in chip form and were mostly ceramic except for a few high-Q porcelain capacitors used in the oscillator section. The TCVCXO was designed to use a new ceramic flatpack crystal which is microcircuit compatible. This flatpack crystal was Government-developed and Government-furnished.

Partitioning

The electrical circuit for the TCVCXO was partitioned into two functional parts, called the voltage-controlled crystal oscillator (or VCXO) section and the temperature-compensated function generator (or TCFG) section. The partitioning is as shown by the dotted line in Figure 2. Each part was fabricated

and tested as a separate hybrid microcircuit. The decision on how to subdivide the overall circuit into subcircuits on several substrates was based on preliminary circuit layouts and on (1) minimizing the amount of connections between substrates, and (2) facilitating functional trimming and testing.

Layout

The layout of the TCFG and VCXO hybrids was a challenge in packaging approximately 140 circuit elements onto two substrates totaling 2.7 square inches, including the area required for corral seal and plug-in "fingers". The total area inside the two corrals was actually only 1.5 square inches, and even that was not totally usable.

An attempt was made to follow preferred design guidelines, however, many compromises were required in order to meet the space requirements. The layouts used four different resistivity pastes (maximum of three is preferred) in order to minimize total resistor area, and utilized smaller resistors than preferred. Some of these compromises figured heavily in later problems relating to resistor trimming, test probe placement, and corral glass overlap onto circuitry. In addition to the serious size constraints, the hybrid layout had to satisfy several known electrical factors:

1. The layout of the oscillator stage of the TCVCXO had to minimize conductor lengths and crossovers in order to reduce stray impedances.

2. The temperature-sensing diode CR1 had to be located as physically close as possible to the crystal in order to achieve proper temperature compensation.

3. To achieve, in manufacture, the exact performance required of the TCVCXO, functional resistor trimming was required. Initially the 105 resistors in the TCVCXO are passively trimmed to a five percent tolerance. There are ten subsequent functional trims involving as many as 19 resistors. Each trim involves adjusting one of a pair of resistors to achieve the desired output value. The required trim range of these resistors is as high as five to one.

4. In the TCFG hybrid design, several ribbon jumpers are necessary for two reasons; one for passive trimming and the other for functional trimming. Although the laser trimming system used is generally capable of trimming individual resistors connected in a closed loop, the TCFG circuit has too complex an array of closed loops for the system to handle. Therefore, some of these loops have to be temporarily broken to allow for passive trimming of the resistors. The other reason for jumpers is that the functional resistor trim procedure requires that certain electrical connections be temporarily

broken to permit injection of test signals or precise measurement of test voltages.

Criteria had to be established for each corral, for minimum corral-to-chip and corral-to-wire distances. The initial layouts placed components and wires too close to the high corral walls. After corrals were attached, it was noted that their glass fillets had extended toward the substrate interior more than anticipated. In some cases, glass had partially covered resistors, making trimming very difficult. Corral tolerances and the associated shift in the glass fillet location also caused VCXO assembly difficulties. In a few areas, wire bond and die bond pads were partially covered by corral glass, making chip attachment and wire bonding a tedious and time-consuming process. The corral height also generated assembly problems. Because of corral dimensions and circuit density, some components had to be mounted extremely close to the inside corral wall, so close that conventional die bonding and wire bonding tools would not clear the wall. To circumvent this problem, bonding tools were ground extremely thin for use in these areas. Thick film networks are shown in Figure 5.

## FABRICATION AND ASSEMBLY

### Thick film Network Fabrication

The networks were fabricated using standard thick film materials and processes and 325 mesh stainless steel screens. Platinum gold conductor material was used for all areas requiring soldering such as chip capacitor pads, wrap-around connection pads, and conductor runs under the corral seal area. Gold was used for all other conductor runs and die and wire bonding pads. Dupont Birox 1400 resistor paste was used for all resistors. Resistors were passive trimmed after corral attach, to eliminate resistor drift problems during the glass corral attach furnace exposure.

Figure 5. Thick Film Resistor-Conductor Networks

## Corral Attach

In attaching the corral assembly to the thick film substrate, first the ceramic bottom surface of the corral assembly is glassivated using a tape transfer process. The glass is then sintered in a furnace at about 500°C, thus fusing the glass to the ceramic corral. The glass is a modified lead-zinc-borate devitrifiable solder glass with a thermal expansion coefficient reasonably well matched to the alumina.

The corral-to-substrate attachment process can be performed in a belt furnace or using a hot plate. Corrals were attached to substrates on a 500°C hot plate with the glass allowed to devitrify for ten minutes. The hot plate process works well and was used in the fabrication of the engineering samples. In production, however, a belt furnace would be used.

## Passive Resistor Trim

All of the 105 resistors are laser trimmed after corral attach to five percent of nominal value. The trimming is performed using custom-designed fixed point probe cards. Extra long probes and a special "elevator" trimming fixture were required in order to make contact to the network with the corral attached. The maximum corral thickness was 0.140". Several resistors required subsequent active trimming which will be discussed in the electrical section. The only problem encountered in passive trimming was the variation of corral location and amount of glass fillet and their effect on the ability to trim the resistors close to the corral.

## Component Assembly

A process flow chart showing the sequence of operations and tests for hybrid and module assembly, beginning with component assembly, is shown in Figure 6.

Component assembly involves die bonding, wire-bonding and soldering of chip capacitors. The height and location tolerance of the corrals caused some assembly problems as mentioned earlier. Ultrasonic ball-bonded gold wire was used for the interconnection of all semiconductor chips. Gold wire was selected over aluminum because of the well-documented reliability problems associated with aluminum wire bonds on most thick film gold materials. Ultrasonic ball bonding was selected over conventional thermo-compression bonding to avoid exposure of the gold-to-aluminum interface on the chips to excessively high temperatures and an attendant "purple plague" intermetallic problem.

The selection of soldering and eutectic die bonding as the processes for attaching chip capacitors and transistor and diode dice, respectively, was made because the use of conductive epoxy was expressly prohibited on this program. Non-conductive epoxy die attach was permitted for the integrated

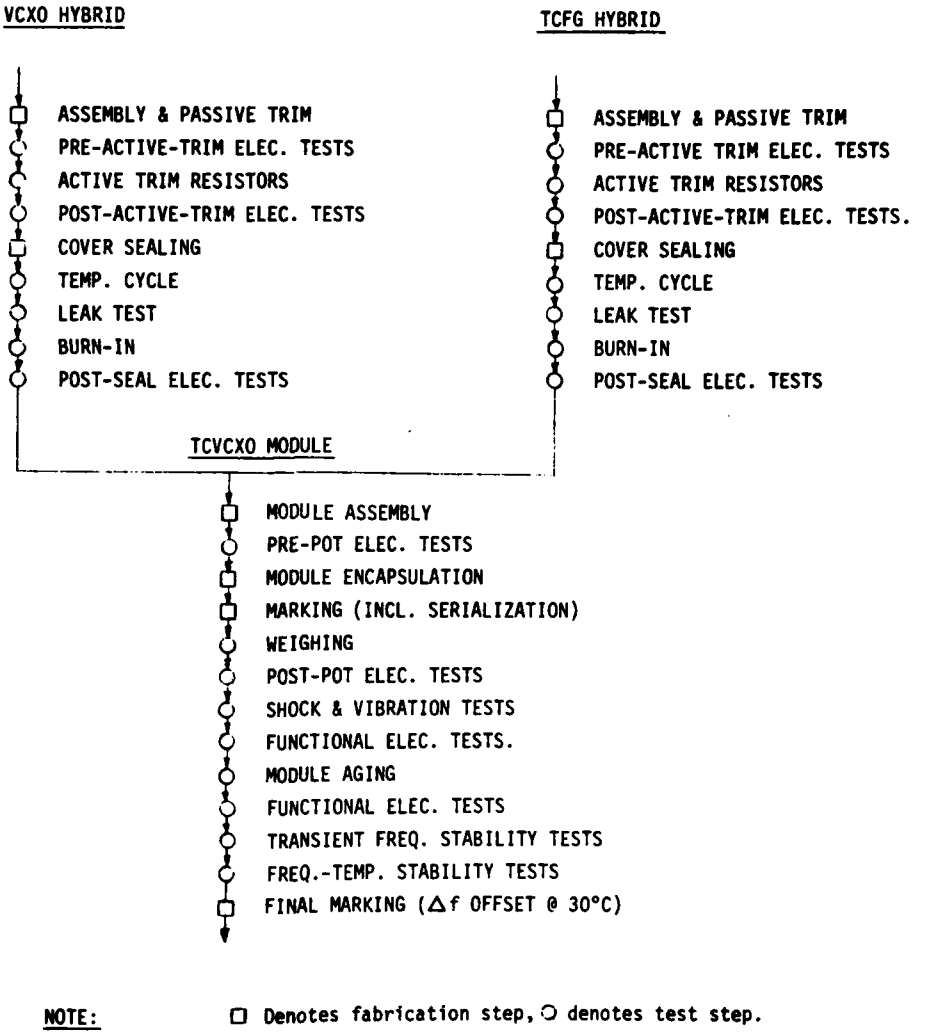


Figure 6. TCVCXO Process Flow

circuit chips where the back of the chip was not required to be electrically attached to the circuit.

Assembled hybrids prior to seal are shown in Figure 7.

## Sealing

The corral assembly and stepped lid were designed for parallel seam welding or soldering. Seam welding turned out to be difficult due to the critical nature of the required welding currents and pressures. Welding currents sufficiently high to effect good cover-to-corral seals would heat and

fracture the corral glass, causing leaks at the corral-to-substrate interface. This was especially true on the shorter of the two corrals.

Parallel seam soldering was therefore used for sealing the hybrids. A preform of 80/20/ Au/Sn was used and a relatively low current setting was adequate to reflow the preform and produce a good seal.

Module Assembly

The two hybrids, after being sealed and tested, are bonded back-to-back using an epoxy preform. The crystal and potentiometer are bonded on top of the hybrid, and the entire unit (Figure 8) is placed in a potting shell and filled with a low density epoxy. The potting shell approach was chosen for two reasons over the alternatives of transfer molding or casting to shape the entire module assembly.

First, the complex external shape of the module is difficult to mold and will cause some yield loss in fabrication. It is more cost effective to incur this loss in an empty potting shell than in a complete, functioning electronic assembly.

Secondly, the module weight specification (30 gms maximum) precludes the use of dense casting or molding resins. The potting shell provides a hard, dense skin for the module that provides handling protection to the assembly and, at the same time, permits the bulk of the encapsulation material to be a low-density foam, thus minimizing weight. The completed module is shown in Figure 4.

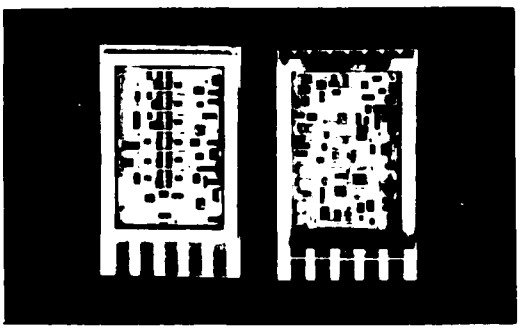

Figure 7. Assembled Hybrids (pre-seal)

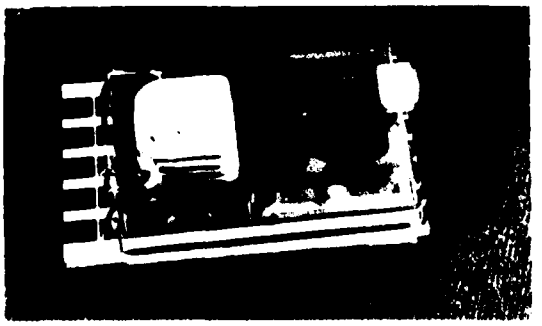

Figure 8. Module Prior to Potting

## ACTIVE TRIMMING

The tight electrical specifications for these modules and the inherent differences between the parameters of each crystal require that each circuit (both VCXO and TCFG) be tailored to the specific crystal used in the oscillator. This is done by functionally trimming the circuits. In addition, active trimming permits the use of other components with looser tolerances than those finally required by the circuit, provided that the circuit parameter in question can be adjusted by trimming. Thus, less expensive components, unmatched components, and looser tolerance circuit sections can be utilized and compensated for permitting a sizeable savings in cost and an improvement in yield and performance. In the majority of active trims for the TCVCXO, the desired output is a function of the ratio of two resistors. This permits the output to be adjusted in either direction allowing recorrection in case of overshoot or parameter drift. Also, this permits the initial target value of the resistors to be their nominal value instead of targeting for a low value as would be necessary if the active trim was unidirectional.

### VCXO Active Trim

In the manufacturing process, prior to laser trim, the crystal is attached to the open VCXO module. Table II shows the active trims that are performed on the VCXO and XTAL combination.

The reference for the voltage regulator is a 6.2 volt $\pm 5\%$ temperature compensated diode and the output voltage of the regulator is primarily dependent on this diode and the ratio of two resistors in the circuit. This ratio is adjusted by laser trimming to produce the required nine volts to its required tolerance.

The voltage-frequency non-linearity that has to be compensated for in active trim is primarily a function of the varactor diode, the crystal, and the capacitance (including stray capacitance) that the oscillator sees. Because the circuit behaves slightly differently with the lid in place and the crystal positioned over the VCXO, a shift in the deviation characteristics is expected and allowed for during trimming.

## TCFG ACTIVE TRIM

A frequency-temperature curve is supplied with each crystal, characterizing its performance over the operating temperature range. The normal passive trim of the TCFG circuit will generate a cubic voltage-temperature function whose shape approximates the frequency-temperature characteristic of the crystal family being used. However, to tailor the function generator to the specific crystal for the particular circuit it is necessary to rotate the curve of the function generator to match the crystal curve. This is accomplised by actively trimming the TCFG. Table III shows the active trims that are performed on the TCFG.

Table II. VCXO Active Trim

| Section | Function | Value | Trim Tolerance |
|---|---|---|---|
| Regulator | Regulated Voltage | 9 Volts | 0.02% |
| Summing Amp | Analog Gain | 1 | 0.5% |
| Summing Amp | Comparator Gain | 1.1 | 0.5% |
| Linearization | Reference Voltage | 1 Volt | 0.1% |
| Linearization | Deviation 1 | 500 Hz/Volt | 0.2% |
| Linearization | Deviation 2 | 500 Hz/Volt | 0.2% |

Table III. TCFG Active Trim

| Section | Function | Value | Trim Tolerance |
|---|---|---|---|
| Thermometer | Gain | 10 | 0.2% |
| Thermometer | Reference | [4.355 + 0.21 ($\Delta$T)] volts | 0.1% |
| Function Generator | Rotation Point | 4.355 volts | 0.05% |
| Function Generator | Compensation | * | 1% |

* One of two selected resistors (R47 and R48) are trimmed to a specified value which is determined by the frequency difference between the upper and lower turning points obtained from a corrected frequency-temperature curve of the crystal assigned to the TCFG being trimmed.

The reference voltage of the thermometer is a function of the characteristics of CR1 and the ambient temperature. During active trim the ambient temperature is monitored by a thermocouple in the trimming fixture which is in intimate thermal contact with the TCFG substrate. The $\Delta T$ of the equation (Table III) is the difference between substrate temperature and 26°C.

The compensation trim ties the TCFG that has been trimmed to a particular crystal. That crystal is also associated with a particular VCXO. These specific parts must be married together at final assembly after sealing the TCFG and VCXO circuits.

## ELECTRICAL TESTING

Production of hybrid devices of the complexity and precision of the TCVCXO requires that the units and their associated components be evaluated at various places in the production cycle to insure high process yields and minimize final module cost. The sequence in which the circuits are electrically tested is shown in Table IV.

Table IV. TCVCXO Electrical Testing

- Device Testing
- Pre-active Trim Electrical Tests (TCFG and VCXO)
- Post-Active Trim Electrical Tests
- Post-Seal Electrical Tests
- Pre-pot Electrical Tests (TCVCXO)
- Post-pot Electrical Tests
- Aging
- Final Electrical Tests

### Device Testing

High volume-high yield production requires that all components introduced into the production flow be adequately screened for compliance with all specification requirements. For the TCVCXO, this screening is especially important for the crystal, and for active components to a lesser degree.

Performance of the crystal within specification limits is all important to the successful building of the TCVCXO. Exact crystal temperature-frequency characteristics are required to determine trim parameters for the TCFG.

All other devices, such as operational amplifiers, diodes, transistors and capacitors, although 100 percent tested by their vendors, must be lot sampled. Standard diodes are checked for opens, shorts and forward voltage drop, while Zeners are checked for reverse voltage characteristic. Varactor diodes are tested for capacitance at rated voltage. Capacitors are sampled for value, transistors for dc characteristics and Beta, and operational amplifiers for dc offset, and gain.

Pre- and Post-Active Trim Testing

The majority of the pre-trim and post-trim functional tests are performed at the laser station itself. The trimming, through its minicomputer and test instruments, can be used to check the significant electrical parameters of the substrate. On the VCXO, for example, these parameters include the output of the nine volt regulator, U6, and the frequency output with known dc control voltages in. If the unit fails to meet expected tolerances, the laser trimmer rejects it. If acceptable, the substrate is trimmed, and finally, retested to active trim tolerances after being allowed to stabilize. The VCXO circuit goes through an extensive testing of its room temperature operating parameters at the laser trim station, which is sufficient to act as both pre-trim and post-trim functional testing. While most of the parameters of the TCFG are checked at the laser trimmer, an additional check to verify the diode function generator curve is performed. A capacity coupled ramp voltage is inserted into the thermometer buffer amplifier to simulate a linear temperature excursion of the circuit. This allows the TCFG to display on an oscilloscope the voltage function of the diode generator. A typical output curve for a good circuit is shown in Figure 9.

Figure 10 shows the equivalent output versus temperature of a TCFG circuit.

Post Seal Testing

The post seal test is a quick go-no-go test to verify that the devices are functional.

Pre-Pot and Post-Pot Testing

Following the post seal tests, the TCFG, VCXO, XTAL and frequency adjust potentiometer are married together and the TCVCXO module undergoes pre-pot testing where it is tested for the parameters of Table V. Following encapsulation, the devices are again subjected to the tests of Table V. The frequency versus temperature and deviation versus temperature tests are accomplished by operating the devices in an oven whose temperature is continuously increasing from $-40^{o}C$ to $+70^{o}C$ at a rate of $1.0^{o}C$ per minute.

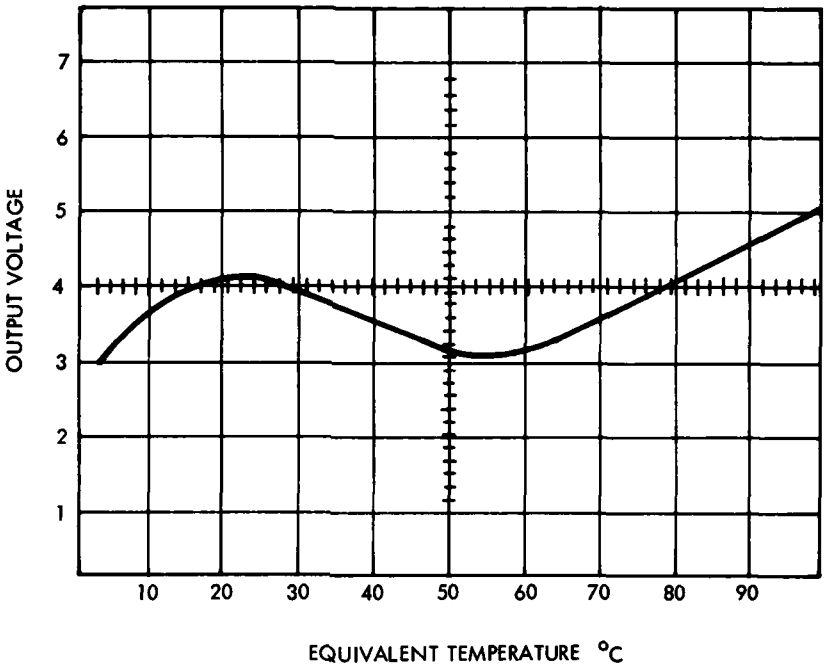


Figure 9. Temperature Simulated TCFG

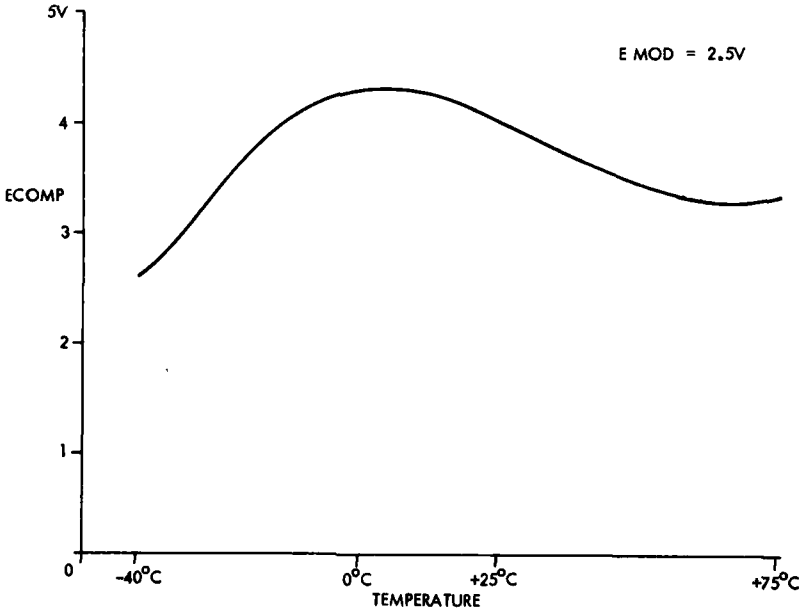


Figure 10. TCFG Output Voltage (ECOMP) Vs. Temperature

Table V. Module Tests

| |
|---|
| • Frequency Adjust Range |
| • Frequency Deviation |
| • Deviation Linearity |
| • Input Impedance |
| • Input Power |
| • Frequency Stability - Versus Supply Voltage<br>- Versus Load |
| • Output Voltage |
| • Regulated Supply Stability - Versus Supply Voltage<br>- Versus Load<br>- Versus Temperature |
| • Modulation Bandwidth |
| • Frequency Versus Temperature |
| • Deviation Versus Temperature |

The modulation input is sequenced between 2.5 volts (center frequency), 3.25 volts (negative deviation), and 1.75 volts (positive deviation) and the output frequency is plotted versus temperature on an X-Y plotter after the input signal is switched. This produces three curves on the plotter as shown in Figure 11.

## Aging

In order to achieve the high order of stability required by these oscillators, the production units will be aged at 60°C for a 14-day stabilization period. Following this period the devices should remain at 60°C and be monitored until the frequency change at 60 $\pm$0.1°C does not exceed $1 \times 10^{-8}$ over a one-week period.

## Final Test

At final test the modules are subjected to the tests of Table V for conformance to the design specifications.

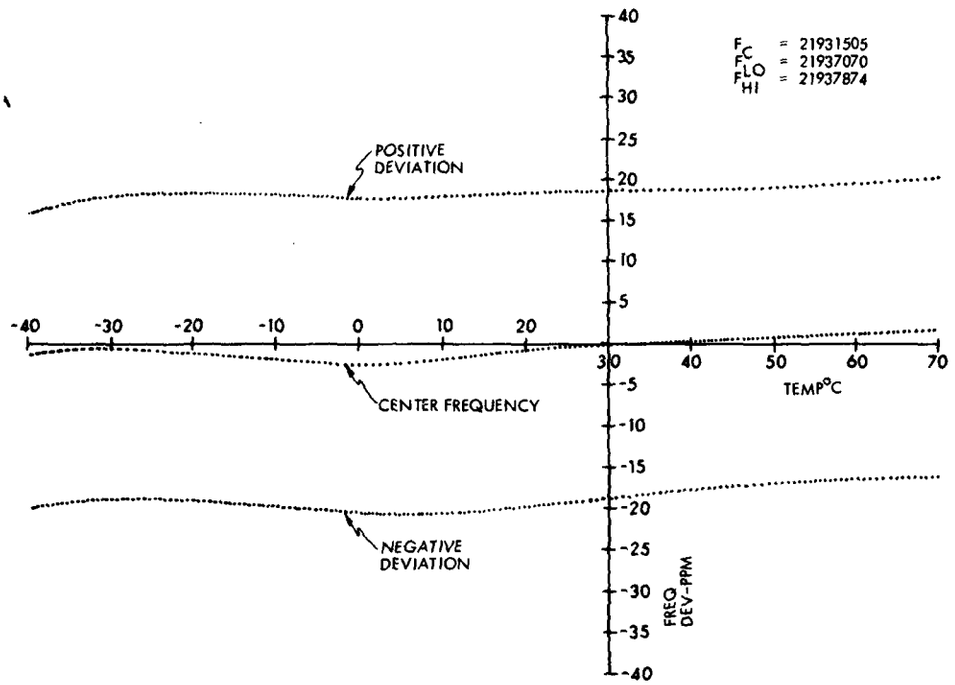


Figure 11. Output Frequency Deviation Vs. Temperature

# LARGE AREA HYBRID DIGITAL ENGINE CONTROL

BY

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## Introduction

The Full Authority Digital Electronic Control (FADEC) for which the hybrid modules to be described have been built, is being developed by the Aircraft Engine Group of General Electric Company. This work was conducted for the Naval Air Propulsion Center under Contract N-00019-76-C-0423 supported by the Naval Air Systems Command. The packaging design, fabrication and test of the hybrid microelectronics used on this program was provided by General Electric Ordnance Systems. As the aircraft engine technology has advanced, the control functions to be performed have become more complex. In order to provide the optimum in engine performance, an on-engine digital computer is the key to effective control. It is that problem to which this program is addressed.

## Goals

The program goals were to package a real time computer, and to control engine output functions using a reliable, lightweight package capable of operating in an on-engine environment. Typical requirements are 40,000 temperature cycles from -55°C to +110°C, acceleration of 30g's, vibration of 40 mil p-p at 60g's as well as resistance to acoustic noise and thermal shock. To meet these challenges, the design uses matching thermal expansion coefficient materials and well-designed compliant members at low stress levels to minimize fatigue and creep.

## Implementation

To implement the computer function in hybrids, several designs were developed using large area (3" x 4.5" and 3" x 2.25") multilayer, refractory metal/alumina substrates. In addition to being large, in area, typical units have a total of 200 to 300 devices such as IC's, resistors and capacitors on a single assembly (Figure 1).

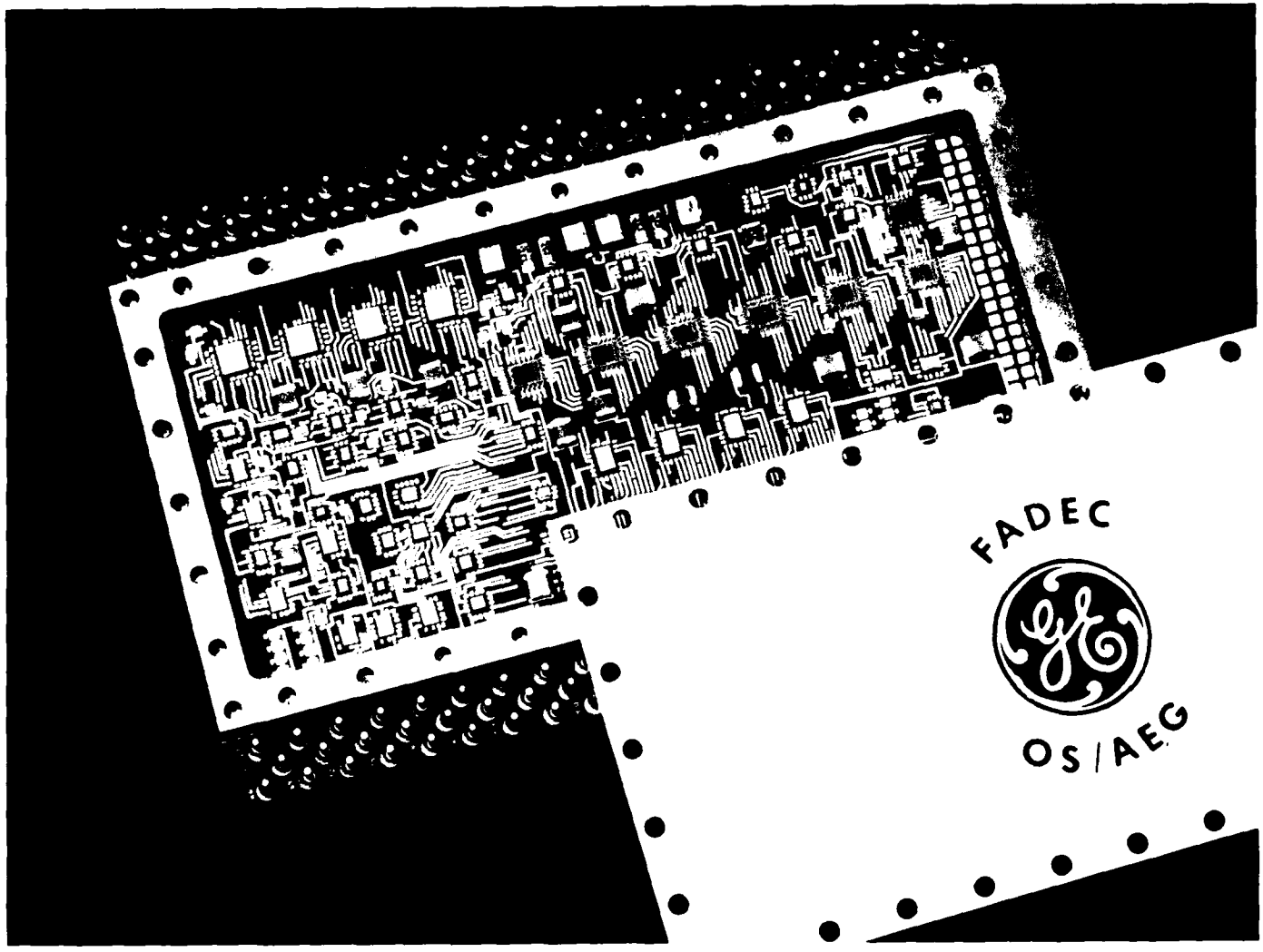


Figure 1. HYBRID MODULE AND COVER

## Packaging

The hybrid package substrate chosen was one utilizing refractory metal/alumina ceramic of six layer construction. For electrical reasons, the first two layers were signal layers followed by power and ground planes, then two additional signal layers (Figure 2).

This material has its vias punched and conductors applied by screening in the "green" or flexible state, with successive layers being aligned, laminated under pressure and fired. The result is a monolithic multilayer ceramic substrate which, because of the initial high temperature firing, is insensitive to the temperature cycle environment.

ASTM Alloy F-15 (Kovar) pins are attached to the substrate using Cu/Ag braze.

In order to minimize residual stresses in the substrate, the kovar ring frame is brazed to the substrate using eutectic Au/Ge. Since the expansion of kovar closely matches that of the alumina at the 356°C eutectic point, stresses are minimal. (Figure 3).

The tungsten metallization on the substrate and the ring frame is Ni and Au plated for device mounting, wire bonding and in the case of the ring frame for protection against corrosion.

Sealing of the hybrid presents something of a dilemma since hermeticity is desirable from the environmental point of view, yet the requirement for repairability is mandatory in a hybrid of this cost and complexity. This problem is faced and solved in high performance vacuum systems by the use of compliant metal seals (gold, aluminum, indium alloy) between specially machined and polished sealing faces. A similar approach was adapted to the particular requirement of on-engine hybrid packages. Here, an electroformed lead seal ring on a copper gasket is compressed between polished gold plated kovar faces. Such seals repeatably provide leak rates less than our measurement threshold ($1 \times 10^{-9}$ atm-cc/sec). Equivalent results are obtained both after thermal cycling, and after opening and resealing the package. This feature is considered to be a highly significant development for this and many other large hybrid applications. (Figure 4).

In order to demonstrate the feasibility and reliability of tape automated bonding of IC's in this environment, a PROM was selected and the capability developed to test, program and mount the device. The tape selected was 3 layer Cu which was Au plated to prevent oxidation during burn-in and for compatibility with mounting metallurgy. Inner leads were attached to the chip using thermocompression bonding while

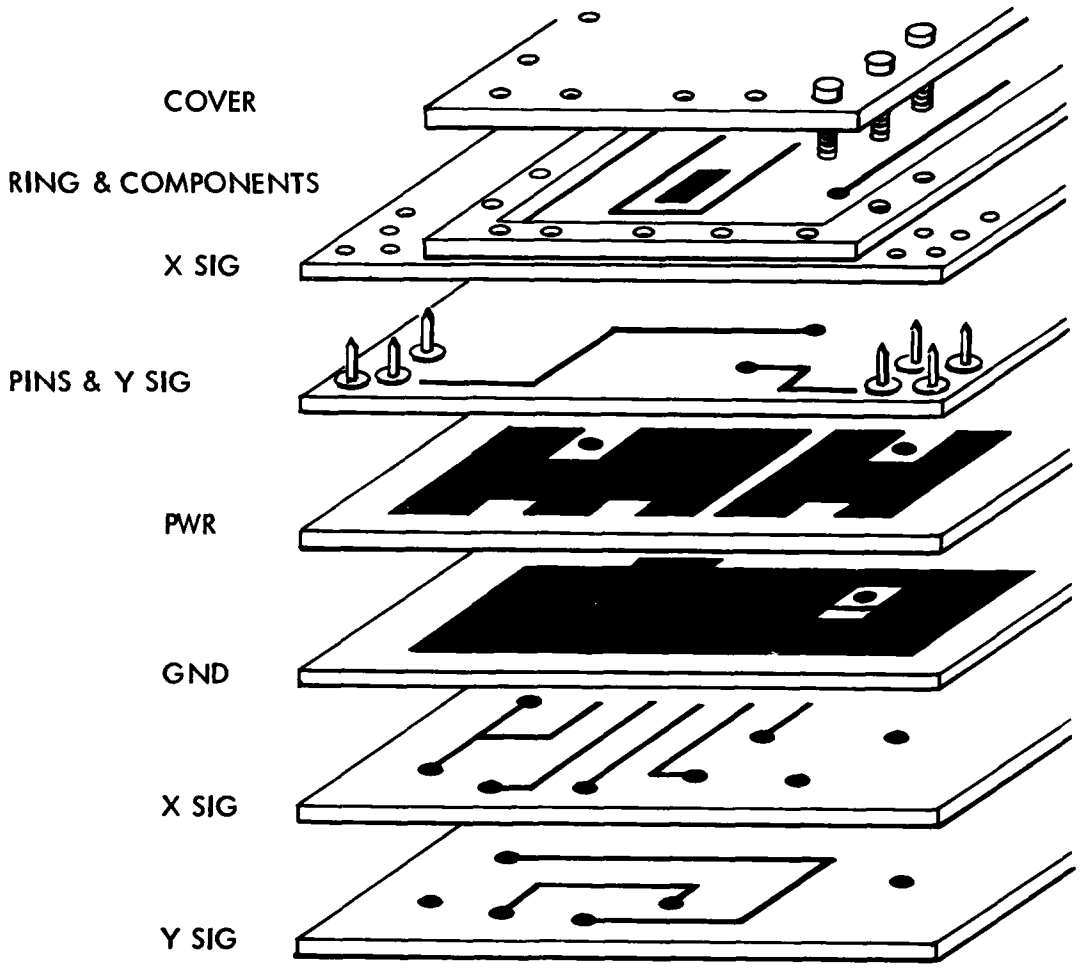


Figure 2. TYPICAL SUBSTRATE CONSTRUCTION.

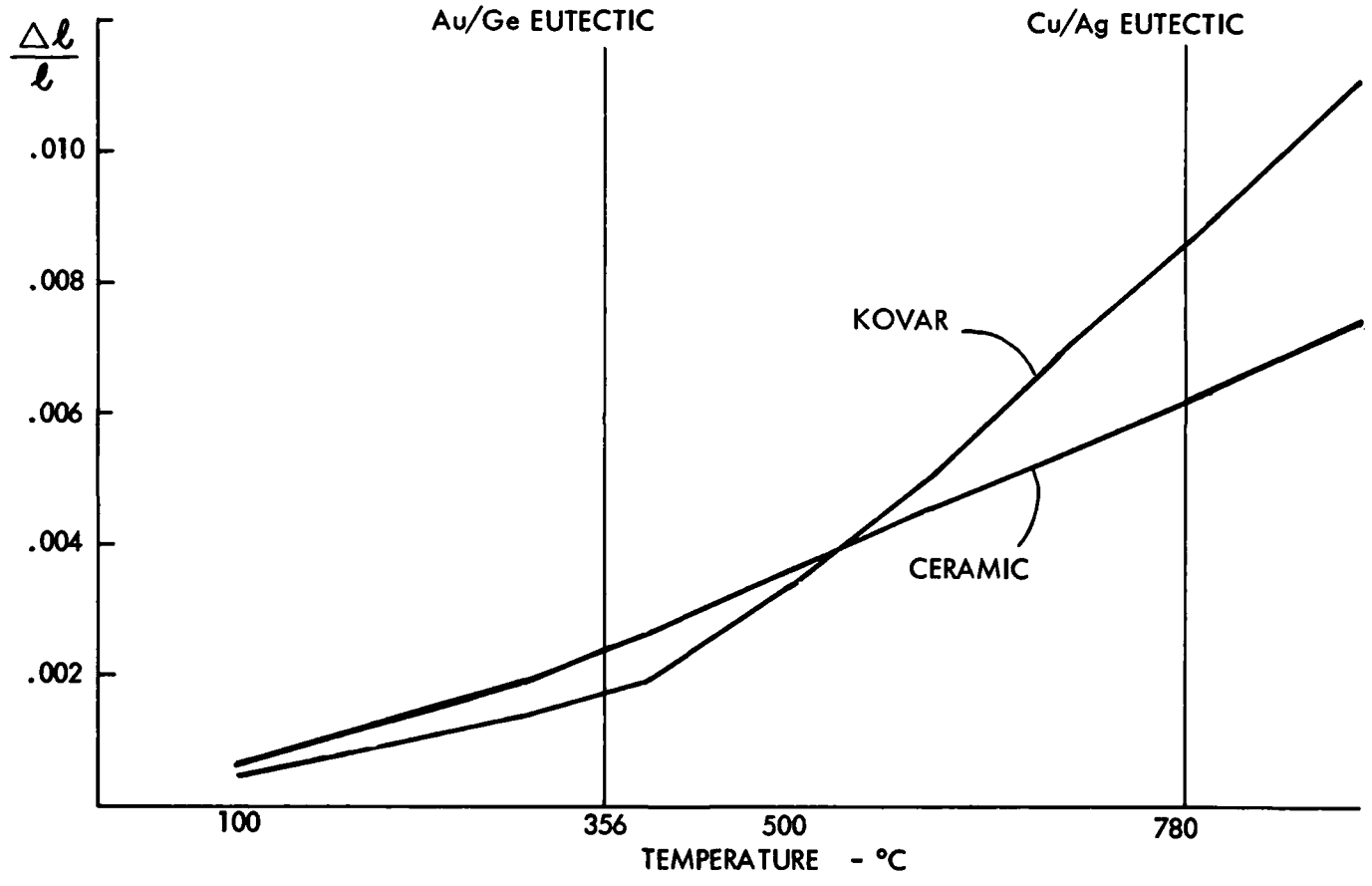


Figure 3. LINEAR EXPANSION OF PACKAGE MATERIALS.

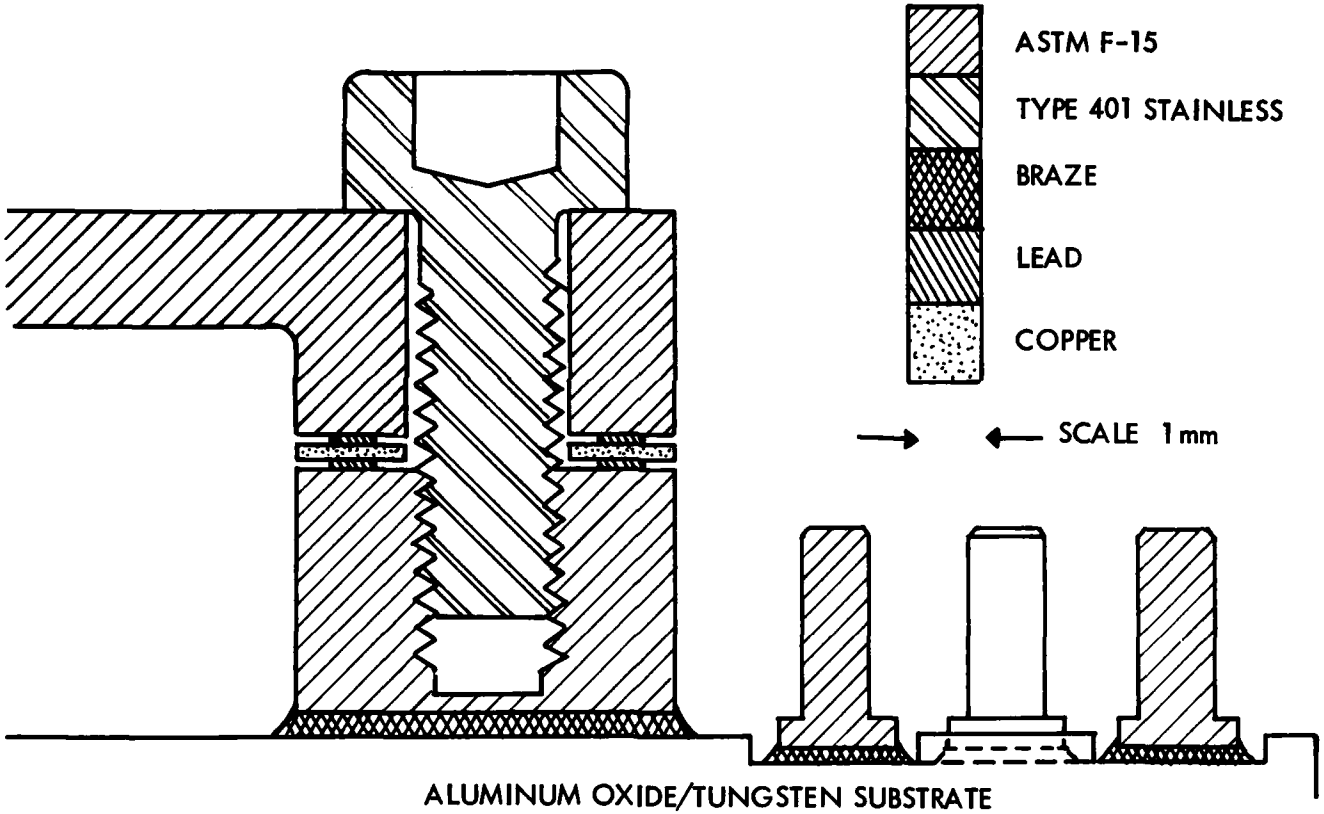


Figure 4. FRAME-PIN-SEAL CROSS SECTION

the chip and outer leads were simultaneously Au/Sn reflowed to the substrate to facilitate repair (Figure 5).

The balance of the IC's are Au/Si eutectic mounted to specially designed Au plated kovar tabs. After electrical testing the tabs are Au/Sn mass reflowed to the substrate. This kovar tab makes it possible to easily remove a single chip during module electrical test and troubleshooting, using locally applied heat. Our experience shows that repairs may be made several times without damage to the chip bonding pad.

## Thermal Design

Thermal considerations are examined using a transient heat transfer computer program and analyzing the IC's considering the maximum power dissipation in each application. Typical $\Delta$ T's to the heatsink mounting are less than 11°C with a maximum of 17°C in the case of power op-amps. The small size of these power chips and their high heat flux led to use of Mo heat spreaders to reduce the $\Delta$ T to acceptable limits for reliability. Infrared imaging of each of the designs, in operation, shows close correlation with the calculated substrate temperature distribution.

Further development work on similar advanced hybrid circuit packaging is continuing at Ordnance Systems.

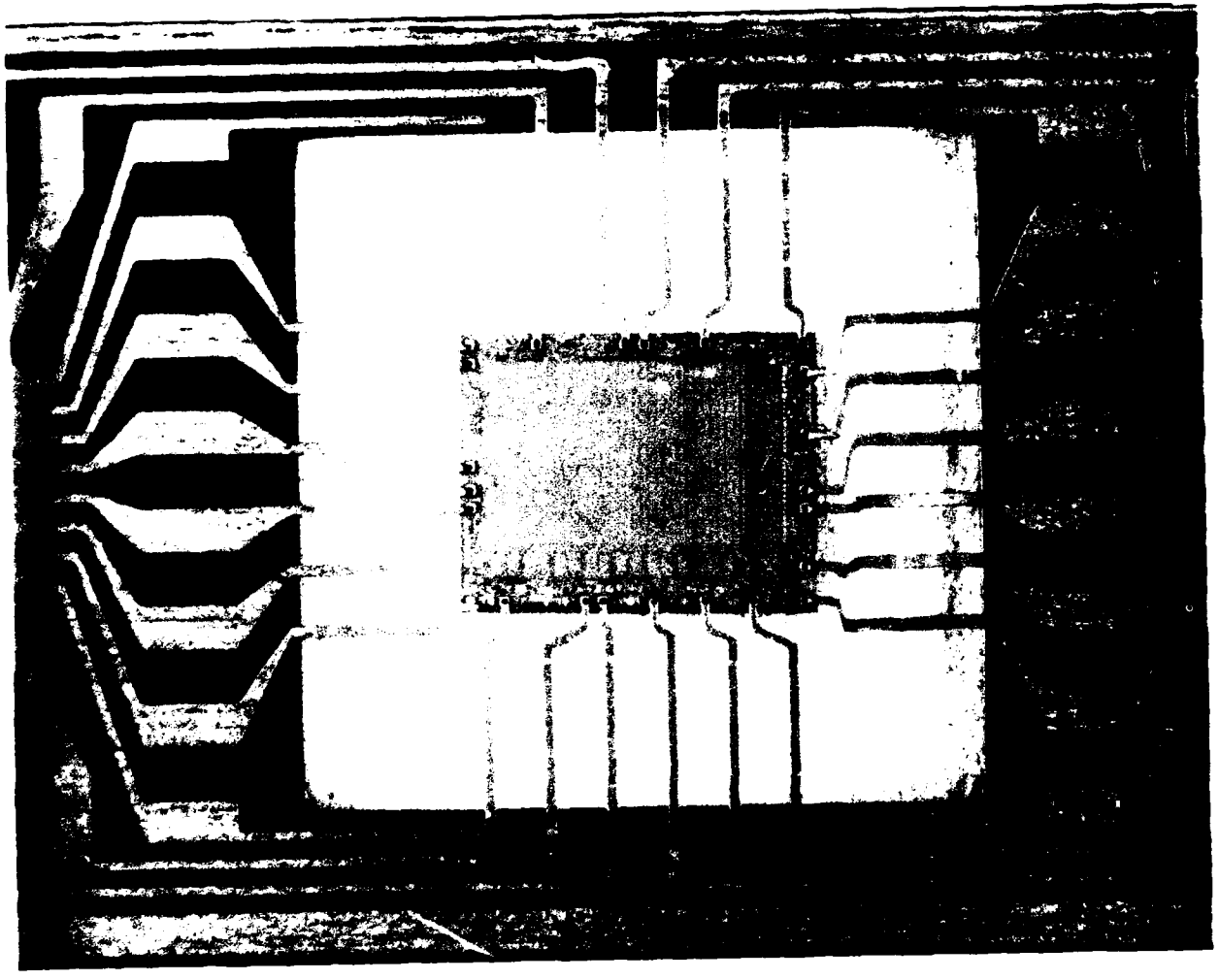

Figure 5. TAB PROM

# Large Area Hybrids Utilized in Lightweight Avionics Systems

by

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## ABSTRACT

Large area hybrids have been found to be a cost effective method of packaging complex digital functions. Contrary to popular opinion, fabrication and test of hybrids containing approximately 100 chips is less costly than trying to package a partitioned design of the function. Also chip failure due to burn-in have not been the problem that many industry personnel believe it to be. The average number of chip failures through all testing including burn-in has been about 5 percent, and this number is being reduced with improved chip screening.

## INTRODUCTION

Many electronic Avionics systems make extensive use of hybrid Technology. ITT Avionics Division is presently using two large area hybrids in several developmental ECM sets. These modules contain 93 and 103 integrated circuits respectively and are shown in figures 1 and 2. In these hybrids, chips are attached to a single 6 square inch substrate which is mounted into a 2-1/2" x 3-1/2" 116 pin plug-in package. One module is the ITT Avionics CX-475 processor which is used 4 times per system and contains SSI, MSI, ROM, PROM, RAM and 2901 microprocessor chips. The other module is a tracker that contains mainly SSI and MSI chips but does contain some memory chips. Over 200 of these hybrids have been made to date. It is presently projected that these hybrids will be in production in 1981 in quantities of between 60 and 150 per month. ITT Avionics has been and will continue to be successful in manufacturing these hybrids because it has developed the following fabrication, assembly and testing techniques which produce high yields and minimize rework.

## VERIFICATION OF CHIP ACCEPTABILITY

When active devices must be procured from IC houses and chip distributors, the following statement is attached to the purchase order:
These semiconductor chip devices shall meet the following requirements:

a) Operating temperature from -55 to +125 degrees C.
b) Meet electrical parameters of vendor's published specs.

c) Visual inspection per MIL-STD-883B, Method 2010.3, Condition B.
d) Shipment in waffle type carriers.
e) All dice within same carrier shall be placed in the carrier in the same orientation.

Die carriers shall be identified with a wafer lot number showing that supplier has performed 100 percent DC probe of wafer(s) and 100 percent visual inspection of individual die.

Although a chip vendor cannot guarantee that all chips will meet this level, he can assure that a very high percentage of chips will perform as MIL-STD-883 Class B devices after packaging. After active devices are received, we totally reinspect all devices visually and do a partial electrical inspection at the chip level or as a packaged device. We do this to further assure that the devices will perform properly when installed in the hybrid circuit. MSI devices, memory and LSI devices are treated differently.

Our most recent experience has shown that over 95 percent of SSI/MSI devices will be functional and fully meet the requirements of MIL-STD-883B after packaging. The device types most often used are the 54 and 54LS Series. Occasionally we find a lot of one device type with parametric, temperature or voltage problems. In order to screen out these lots, a 5 percent sample of each lot can be packaged and characterized. A capability exists to 100 percent probe devices using an Edge Instrument chip probing station connected to an MSI tester. However, at this time we have not found it necessary to do this degree of MSI/SSI chip testing.

ROM and PROM chips have been 100 percent retested at the chip level. Before this retest procedure was established, we often had low yields on ROM and PROM chips. Yields on the 82S215 memory have been as low as 40 percent, although yields average between 65 percent and 70 percent. Since six of these devices are used in each processor, low yields on these devices make heavy rework necessary if we do not retest chips. In the past ROM's and PROM's have been retested by outside organizations. We have just developed an inside test capability by connecting the prober to a PROM burning station. This station can also be used as a chip PROM burner if new microcode is needed for special applications.

RAM chips are tested at high speed using the prober and a dedicated processor controlled test box. The tests given to the RAM are the same tests which the RAM is required to pass when installed in a processor hybrid. The clock rate for this test is 4 MHz, and this test is performed at full voltage at ambient and high temperature. A simulated low temperature test is performed by dropping operating voltage to 4.0 volts. RAM chips are tested because this device type (93L422) also has shown poor yields of below 50 percent. This RAM device has also been procured from a vendor with lot acceptance criteria. A lot is acceptable if 80 percent of the chips are functional at full temperature and voltage after packaging. However, in the past it has been difficult to obtain devices because many lots must be screened to find one that yields 80 percent.

The only LSI device used is a 2901B microprocessor chip. This chip is also prescreened by the vendor to the 80 percent level. Most lots are received where the yield has been claimed to be around 80 percent, and test

experience has shown this to be correct. There have not been delivery problems due to low yielding lots and no attempt has been made to retest this device in chip form.

## SUBSTRATE FABRICATION

We have learned how to be extremely successful in building large area multilayer thick film substrates. Yields on these approach 100 percent, and this yield is obtained through careful inspection. Both processor and tracker circuits require six interconnection layers. Most layers include over 1000 vias, and all metal layers are densely populated with interconnects consisting of 10 mil lines on 20 mil centers. Figures 3 and 4 show typical metal and via layers. Since this multilayer is very dense and complex, ground flat substrates are used to improve yields on lines and vias. The added cost of these substrates (approximately $7 to $15 depending on quantity) is small in comparison with the savings due to reduced rework and inspection during the printing process. All printing is performed using 325 mesh screens. This helps fabrication because metal interconnect layers are printed thin which minimizes surface irregularities on subsequent layers, and vias in dielectric layers are printed with higher resolution. In addition, a thin printing gold is used which further reduces surface irregularities on subsequent layers. The dielectric ink used is extremely thixotropic which improves via resolution. Since 325 mesh screens are used for dielectric printing, three dielectric layers are printed to maintain 2 mil distance between interconnect layers. These three printings and 2 mil spacings have been found to guarantee short free multilayers with the ink systems employed. Before printing, all substrates are fired clean. The printing sequence for processor or tracker fabrication is:

- Print first metal layer
- Print first printing of first dielectric layer
- Print first printing of first via fill layer
- Print second printing of first dielectric layer
- Print second printing of first via filled layer
- Print third printing of first dielectric layer
- Print second metal layer

There are 31 print and fire steps required for a six interconnect layer substrate using the ITT Avionics processing approach. After each substrate is printed and while the substrate is still wet, it is inspected for irregularities. Each dielectric layer is inspected for via size, and if the average via is less than 7 to 8 mils square, the layer is stripped and reprinted. This technique has guard banded the process so that final inspection after printing always shows all vias open. Inspection generally goes fast, but is the limiting factor in manufacturing multilayer structures. In spite of all inspection, a typical 6 layer 2" x 3" multilayer requires less than 4 manhours to manufacture when produced in lots of 50 to 100 pieces. Because of our high degree of success with via printings, it is anticipated that we will eliminate the 100 percent via inspection and substitute a 100 percent electrical continuity test using flying probes.

## SUBSTRATE ASSEMBLY

The assembly processes and procedures have been directed toward the utilization of automatic assembly equipment. The substrate has been fabricated in such a way to assure a very planar chip bonding area. Since the gold used is a thin printing gold, high yields in automatic wire bonding are assured since the gold itself will have few surface irregularities.

After substrate fabrication, substrates are silk screen printed with conductive epoxy for device attachment. Integrated circuits and other chip components are attached using either hand placement (usually when the device is only used once or twice) or by using a manual pick and place machine with a carousel that holds eight die dishes. After all dice are applied, correct placement and positioning is verified using a dual CCTV fixture which allows one to compare the present assembly with a known correct assembly. After verification, die bonding is completed by placing the unit in a hot oven to cure the epoxy. At this point the substrate is ready for wire bonding between chip and pad. Manual wire bonding takes a skilled operator between five and six hours per unit, but an automatic wire bonder is being procured which should reduce this bonding time to less than one hour. One mil gold thermosonically bonded wire is used for all chip to pad bonding. Bonding footprints have been designed in a symmetrical configuration similar to ceramic package footprints as shown in Figure 5, and all wires are bonded whether interconnected to the circuit or not. Because of this, wire bonding diagrams do not have to be closely followed and Product Assurance inspection is simplified. After wire bonding, the substrate is attached to the case using an epoxy preform. A special fixture has been made for each hybrid type which allows one to apply even clamping pressure between substrate and case without damaging chips or wires. Attachment is completed by curing the epoxy and finally I/O wires are bonded between substrate and case. Before submitting the unit to debug test a workmanship inspection is performed by the Product Assurance department, and a sample of each group submitted is verified for correct assembly by comparing to an assembly drawing. The inspection procedure used is MIL-STD-883B, Method 2017.

## HYBRID TEST

Processor hybrids are accepted on the basis of passing a high speed test performed on a dedicated test fixture controlled by a DEC 11V03. This tester and a low speed diagnostic tester also controlled by an 11V03 are additionally used for debug purposes. First, processors are tested at room temperature and nominal voltage with the low speed diagnostic tester. This test is not an operational test, but rather a stimuli/response test. Inputs are set at specific levels and outputs are checked to find if the levels are correct. There are 88 test points on the surface of the hybrid substrate which are connected to a prober via a probe card. The levels of these test points are also monitored by the computer, and if any levels for a given test are wrong, an error message appears which tells an operator where to look for the problem. The low speed tester is shown in Figure 6. The running time for this test is approximately ten minutes.

In the high speed test, the test program allows one to test for ROM/PROM problems, microprocessor problems, control problems and RAM problems almost independently. After it is determined that the ROM/PROM and microprocessor chips are functional, tests are performed to determine if the processor can follow all instructions. The test will automatically halt during or at the end of a failed instruction, and the status of the registers will give clues to what device is not functional. The running time for this test is about one second.

Both high speed and low speed diagnostic tests can be performed at full voltage and full operating temperature. Open testing of hybrids at low temperatures is made possible by using a moisture free nitrogen filled glove box. Figure 7 shows the high speed tester in the glove box. The moisture level in this box is controlled to between 5 to 10 parts per million. The dew point at -65°C is between 10 and 15 parts per million water, and therefore, open testing of hybrids is possible without condensation. The hybrid is cooled by liquid nitrogen flowing through a cold plate, and the temperature can be controlled to -65°C. The processor is generally temperature tested to -30°C since it generates enough heat to stabilize at -25°C in a -55°C environment within one minute of turn on. This is the time required for the system traveling wave tube to warm up. In order to reduce debug costs, hybrids are only tested to the maximum operating temperature that they will see in a system. In most cases this is 105°C case temperature, but one system is being tested to 115°C. Although generally not necessary, the glove box allows for probing inside an open hybrid in order to determine fault location.

The history of the last 40 processors completed shows that the total IC failure rate through burn-in is 5.2 per 93 integrated circuits. Several hybrids were functional at nominal voltage and room temperature without any chip replacement and two required no rework through burn-in and final test. Approximately half of these failures were in MSI/SSI devices and the balance were in microprocessors and memory. Most failures occur at room temperature and high or low voltage. Approximately 15 percent of the failures are high temperature failures. Less than 10 percent of the failures are low temperature failures. Only 3 percent of the failures are in 24 to 48 hour open burn-in and no failures have occurred during 160 hour final burn-in.

Similar test procedures are used for tracker test, but fewer of these circuits have been required, and therefore there is less data. Data shows that a greater number of integrated circuits must be replaced in a tracker, but this has been traced to the fact that exact fault isolation is more difficult in this design.

## PRODUCT ASSURANCE PROVISIONS

When hybrids are fabricated, the progress of each hybrid is tracked with an individual assembly/test traveler. All electrical rework is documented on the back of this traveler. Workmanship and rework is inspected prior to seal per MIL-STD-883B, Test Method 2017. As required by MIL-M-38510, processes are monitored and controlled. Bonders are tested by making periodic destructive pull tests. Non-destructive pull tests are performed on a sample of

wires in all hybrids. We do not follow the non-destructive pull test method set forth in MIL-STD-883B exactly because each hybrid contains over 1800 wires and 20 different chips. We do not believe this test to be cost effective when building large area hybrids. An alternate procedure has been developed which takes advantage of the fact that hybrids are made in groups of 25-50 pieces, contain chips from common IC lots and each hybrid is totally wire bonded on the same machine within a period of hours. In this procedure we non-destruct pull 20 wires on each hybrid from four locations within the hybrid. In a group of 25 to 50 hybrids, wires attached to all chip types are pulled. In the event of failure, 200 wires are pulled, and if failures still occur, then all wires are pulled. It should be noted that we have not failed non-destructive pull tests since inception in 1978.

## SEAL, ENVIRONMENTAL TEST AND AFTER SEAL REWORK

Hybrid cases have been designed for seam sealing, and extra height has been included in the cases to accommodate lapping and resealing in case of seal or electrical failure. Sealing yields have been high (over 90 percent) in these large packages. For high yields, packages must have sealing edges free of nicks and scratches greater than 2-3 mils and Kovar material must be free of inclusions. Although there have been few after seal failures, a procedure has been generated to give high rework yields. In addition to lapping the seal area flat, as done elsewhere in the industry, our rework procedure also contains a method for brush plating the lapped surface with nickel and gold to restore the original surface. During brush plating, the hybrid substrate is protected by a plastic shield, and after plating, the whole assembly is washed in distilled water. It may be noted that this procedure can also be used for rework of hybrids in metal cases solder sealed with gold tin. Hybrids are subjected to the MIL-STD-883B, Method 5008 Screening Tests, which include mechanical shock at the 3000G level, fine and gross leak check, temperature cycling, burn-in and final electrical test. PIND testing has not been performed to date, but we do not expect results of this test to differ drastically from smaller hybrids.

## CONCLUSION

Large area hybrids can be made with today's technology. After three years experience and over 200 parts, we are ready to commit this technology to production. Large area multilayer substrate technology is cost effective and the labor required to fabricate the substrates is competitive with the labor used when fabricating PWB's of similar complexity. The biggest problem that others will encounter when building large area hybrids is that one must change one's views on hybrid test. Testing of large area hybrids is simple providing the proper test equipment is used, the design is made testable and an adequate test program is written. At ITT Avionics, we believe that there is little justification for requiring that large area hybrids must be built with prepackaged, pre-screened, and pre-burned-in active devices in order to get a cost effective product.

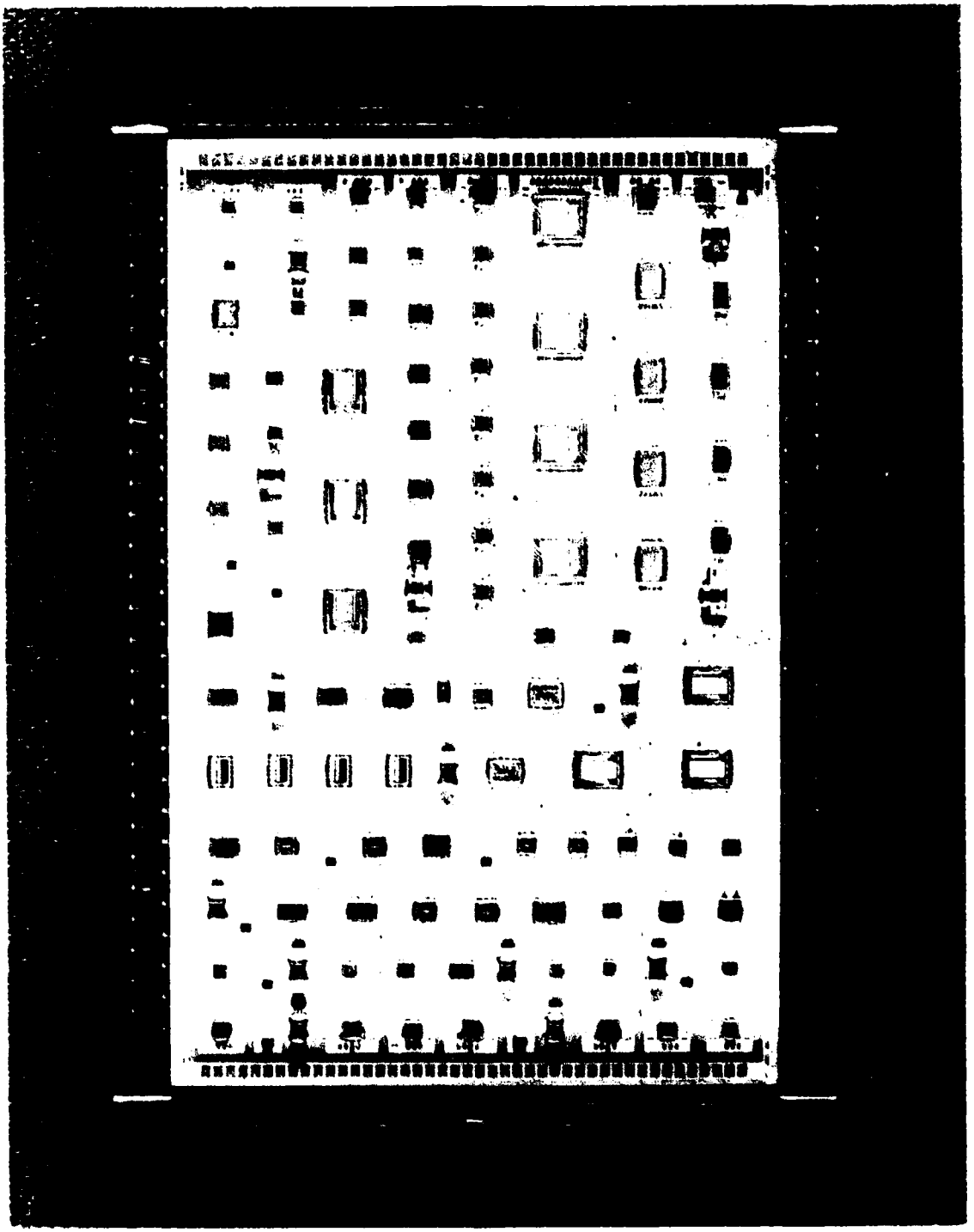

Figure 1. Large Area Processor Hybrid

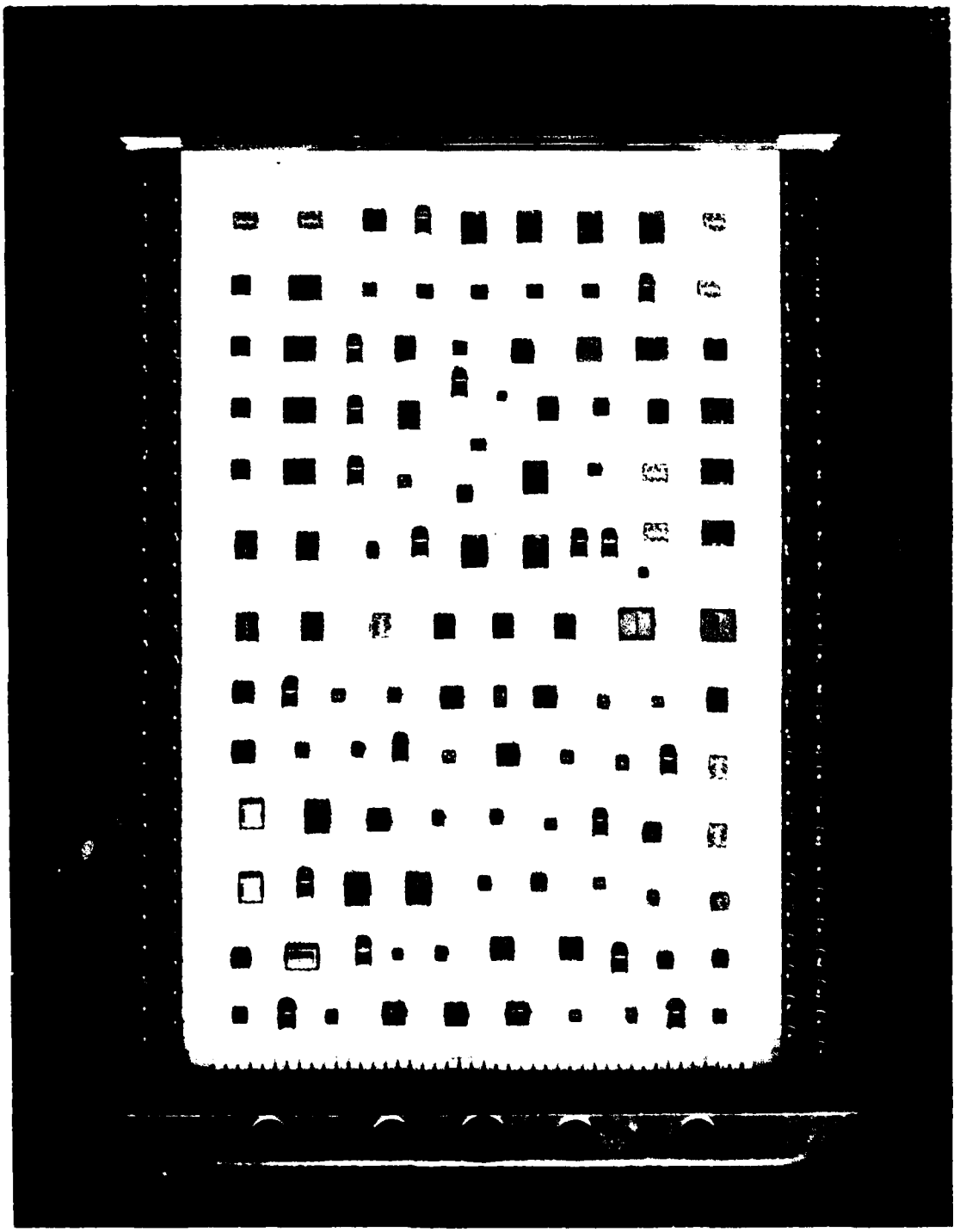

Figure 2. Large Area Tracker Hybrid

Figure 3. Dense Metal Layer

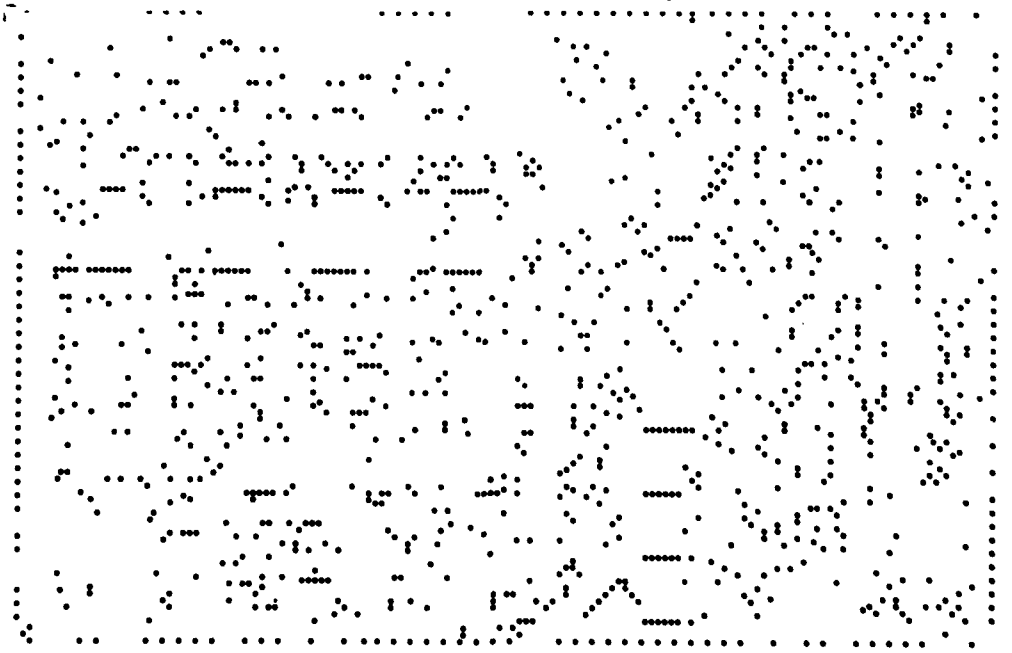

Figure 4. Dense Via Layer

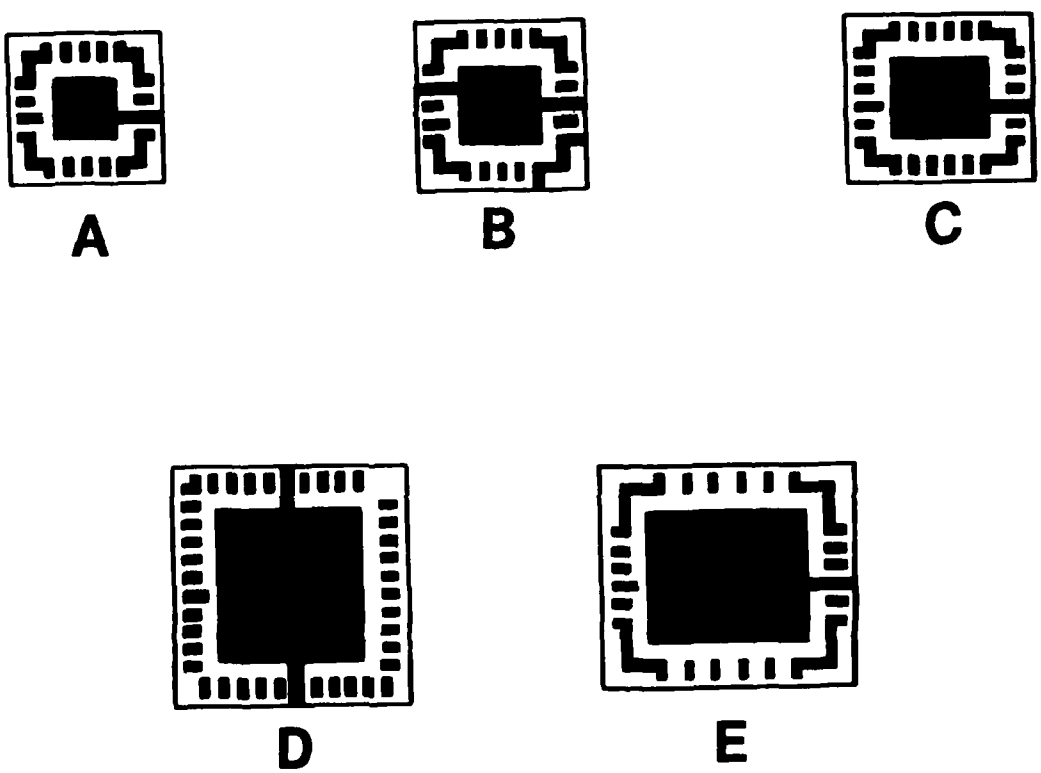


Figure 5. Typical Symmetrical Footprints

Figure 6. Low Speed Test Station

Figure 7. High Speed Cold Test Station

# MNOS BORAM HYBRID MICROCIRCUIT

by

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**Abstract**

A multichip hybrid microcircuit containing 16 Metal-Nitride-Oxide Semiconductor (MNOS) Block-Oriented Random-Access Memory (BORAM) devices is being introduced into military systems. Initial applications are described; and the functional, electrical and mechanical features of the hybrid are presented. Design features to allow the introduction of higher density chips and improved manufacturing technology are explained.

## 1. INTRODUCTION

MNOS is a silicon integrated circuit technology. An MNOS nonmemory transistor performs the same type of functions as a conventional MOS transistor. The physical form of the MNOS device is similar to the MOS device, except that the insulator region is composed of two dielectric layers. The MNOS BORAM nonmemory transistor has 800 angstroms of oxide ($SiO_2$) adjacent to the silicon, and 450 angstroms of nitride ($Si_3N_4$) over the oxide.

In an MNOS memory transistor a region exists where the oxide layer has been made very thin - on the order of 20 angstroms. Given this thin layer, it becomes possible to electrically insert or remove charge from traps in the nitride close to the nitride-oxide interface. When power is removed from the device, what ever charge exists in the insulator will remain for long periods of time.

Both memory and nonmemory transistors are easily fabricated within a single-silicon die, and complex monolithic integrated circuits have become available. One class of MNOS IC's, MNOS BORAM, has been developed specifically for military use. Read-write operation is practical, and the operating temperature range is -55 to 125°C.

This paper describes an MNOS BORAM multichip hybrid microcircuit intended for use in a wide variety of military applications. The microcircuit provides density and cost advantages over alternative forms of packaging. It is configured to fit into an overall plan for orderly growth of the BORAM technology. Changes in chip bit density and improvements in manufacturing technology can be incorporated with almost no impact to memory system designs.

## 2. INITIAL APPLICATIONS

The cost, reliability, power dissipation, environmental limitations, and physical bulk of digital data storage constitutes a major consideration in the implementation of a modern electronic system. This is particularly true in military applications that involve high stress environments, or require emphasis on achievement of some specific attribute such as small size or low power. In several areas, MNOS BORAM shows promise of providing significant advantages over available alternative memory technologies.

### 2.1 Technology Features

The choice of MNOS BORAM for a given application usually keys on one or more of the following features:

- Silicon IC fabrication technology
- Full -55 to 125°C operation
- Nonvolatile data storage
- Data access in tens of microseconds
- Bit density growth potential
- Normal IC voltage interfaces
- Low power operation

Because MNOS is a silicon IC technology it benefits from the enormous cumulative investment in IC fabrication technology, and will share in the gains associated with VHSIC and VLSI advances. MNOS fabrication uses proven materials, processes and equipment. As IC technology achieves finer geometries, MNOS BORAM bit density per chip will increase. Circuit design studies indicate that 256K to 1M-bit chips will emerge.

Of the available nonvolatile memory technologies, MNOS BORAM is most often compared with magnetic bubbles. Bubble data access times are many milliseconds versus tens of microseconds for BORAM. Bubble output signals are millivolts compared to volts for MNOS. MNOS BORAM -55 to 125°C operation, with nonoperating data retention up to 160°C, can not be approached by even the most optimistic projections for magnetic bubbles. In addition, the permanent magnets and field coils associated with bubble devices are not needed for MNOS.

### 2.2 Airborne Recorder Application

The Accident Information Retrieval System (AIRS) being developed by Hamilton Standard for AVRADCOM is an example of one class of application which can benefit from the unique characteristics of MNOS BORAM. AIRS is intended for use on the UH-60A Blackhawk and AH-64 Advanced Attack Helicopters. Variations of AIRS are being considered for use on Air Force and Navy aircraft.

Figure 1 shows the elements of AIRS. Sensors monitor important variables on the aircraft, and this data is constantly examined by a microprocessor system. A history of the last 15 to 30 minutes of the flight is maintained in a solid-state nonvolatile memory formed by one MNOS BORAM hybrid circuit.

Memory is a critical element in AIRS. The system mission is to provide a record which will allow investigation into the cause of an accident. The data must survive in the environment of a crash, and the memory must be capable of reliable operation in the most hostile flight environment.

Crash survivability has been achieved by imbedding the BORAM hybrid circuit in a small lightweight armored module. In December of 1979 the protected memory was qualified per FAA Regulation Part 37-150, Technical Standard Order Authorization T50-C51a. These crash simulation tests included in the following order: 1,000g shock, 5,000-pound crush, penetration (500 pounds behind a small point dropped from 10 feet), 1100°C flame exposure for 30 minutes, and 36-hour salt water submergence.

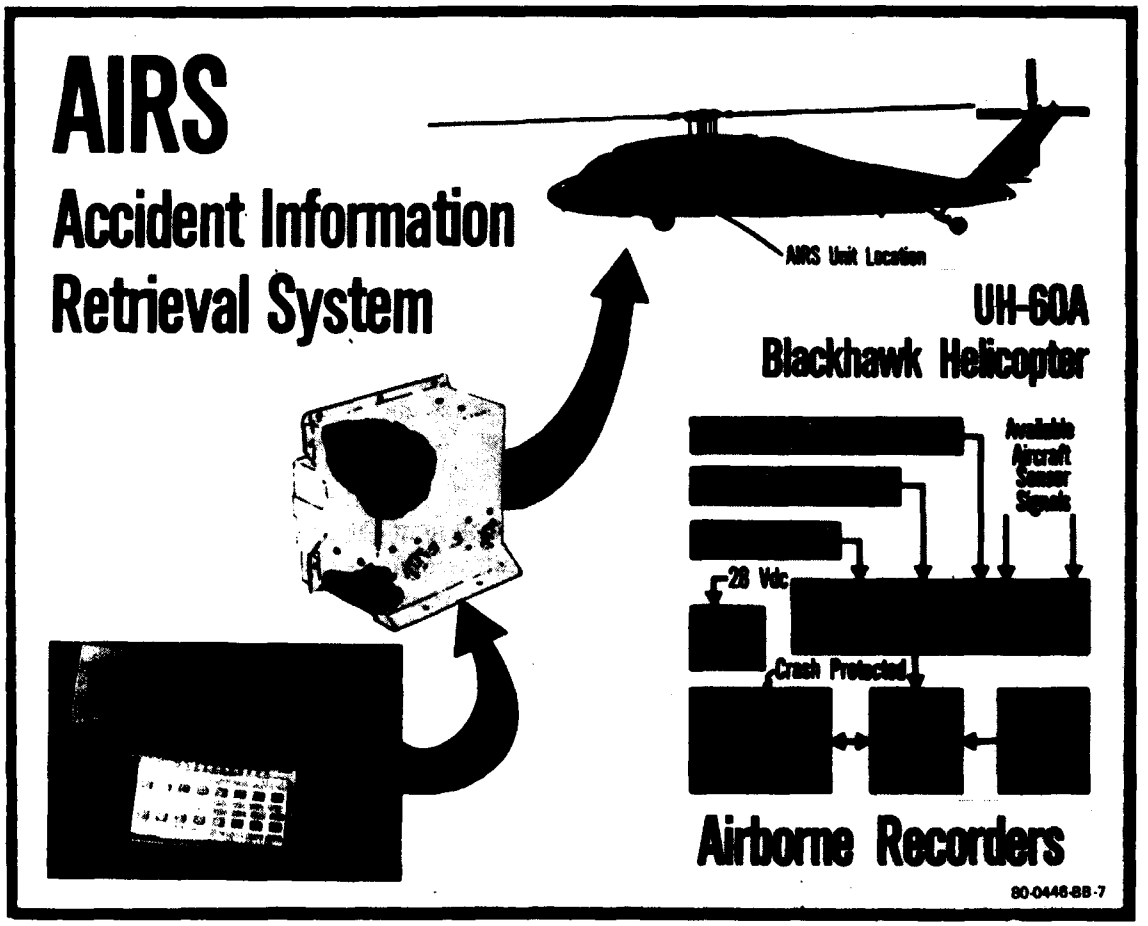


**Figure 1. Accident Information Retrieval System (AIRS)**

Prior to the test sequence the BORAM was loaded with a data pattern. Survival was demonstrated by reading out and checking the pattern after the tests. During the flame test, the cooling provisions in the protective module held the hybrid circuit temperature to 100°C. Other tests at Hamilton Standard showed data was retained after a few hours at 160°C.

For the past few months, the AIRS unit has been undergoing flight tests on a YUH-60A Blackhawk helicopter. Analysis of initial test data has demonstrated the capability of AIRS to reproduce the aircraft flight profile. The memory hybrid circuit has provided reliable operation throughout both the qualification and flight tests.

### 2.3 Program Storage Applications

The storage of computer programs is a requirement common to almost all military electronic systems, and a variety of memory technologies have been used for this purpose. For many systems, MNOS BORAM hybrid circuits can provide a very attractive means of program storage. Figures 2 and 3 illustrate two such applications currently under development.

For an advanced airborne radar an efficient card pair packaging scheme has been established. This particular design uses 8,192-bit BORAM chips in 16 hybrid circuits. The 6.4 × 8.3-inch card pair stores 131,072 words where each word contains 16 bits.

In the Advanced Self-Protection Jammer both the BORAM memory and associated control circuitry are in hybrid microcircuits. The basic configuration consists of three BORAM hybrids and two control and interface hybrids.

Use of the BORAM hybrid provides electrical reprogrammability, high packaging density, wide operating temperature range, low power dissipation and high performance operation in a paging mode.

## 3. PRODUCT PLANNING

Electronic technology is dynamic and continuously growing. The best available semiconductor device of today will be obsolete in a matter of years. Packaging technology is also changing, and significant improvements will be emerging. These forces are desirable, but they complicate the task of product development.

From the viewpoint of both the Government and a private contractor, it is important that a product have a long life time. Functional and economic viability should be maintained for a period sufficient to allow progress down the cost learning curve, and progress toward reliability growth. The product volume must be sufficient to justify significant continued expenditure of engineering talent and capital dollars.

In development of MNOS BORAM the challenge of product growth has been a primary concern. Constraints have been placed on the product configuration to allow change without loss of the benefits of previous investment.

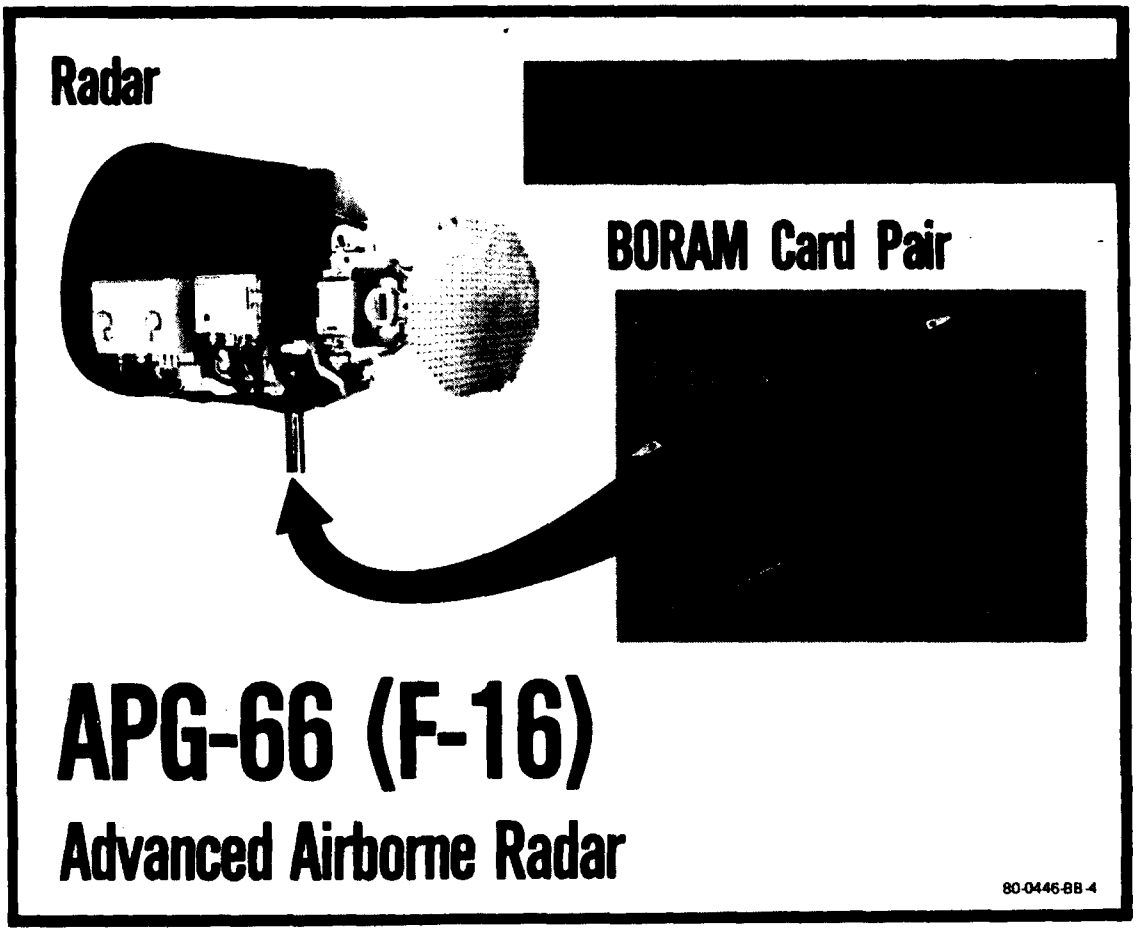


**Figure 2. Airborne Radar Program Storage Application**

### 3.1 Bit Density Growth

The trend toward increased bit density per chip is the most obvious and most important growth factor. To avoid impact to production capability, to circuit configurations, and to system designs a controlled growth plan has been established.

As shown in figure 4, a series of chips called the 6002, 6008, 6032 and 6131 were planned. The bits per chip increase in sequence from 2K to 8K to 32K and then to 131K. All of the devices are pin for pin compatible. A larger device can be used in place of any smaller device. Each chip is of course an evolutionary improvement over the preceding device, and incorporates new features to enhance utility and yield. For example, the 6008 device has lower power dissipation and more relaxed waveform timing requirements than the 6002 chip.

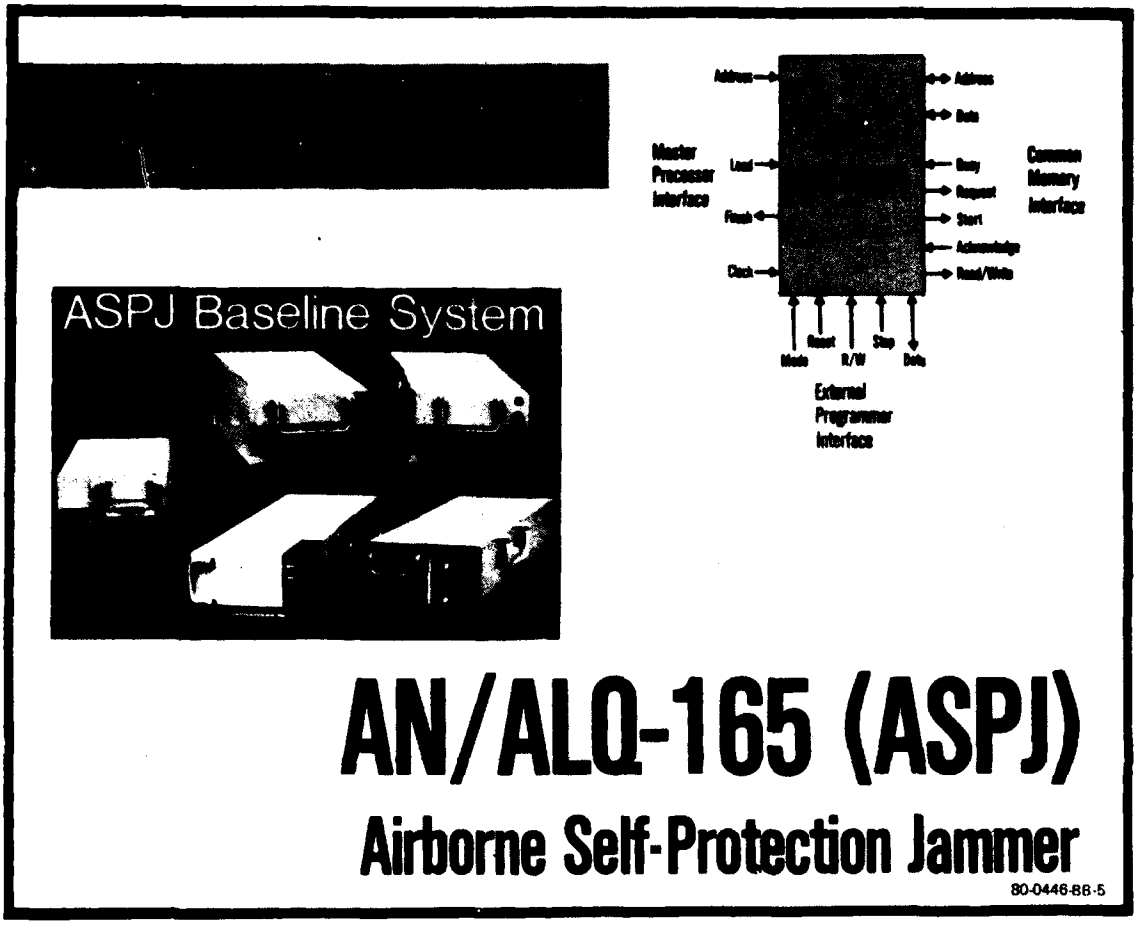


**Figure 3. Advanced Self-Protection Jammer Program Storage Application**

### 3.2 Device Packaging

The MNOS BORAM chips may be placed in any number of different types of packages. Dual in lines, flat packages, leadless carriers and multichip hybrid packages have been employed. While any of these options might be used for a special application, for reasons of density and cost the multichip hybrid approach is the preferred standard. Figure 5 shows the 16-chip BORAM hybrid.

As shown in figure 6, the BORAM hybrid microcircuit was planned to accept any of the 6000 series of chips. The hybrid circuit pin out does not change when it is populated with a different chip. As the product evolves, the pin spacing and signal functions will be maintained. Mechanical improvements will be allowed as long as the pin constraint is held.

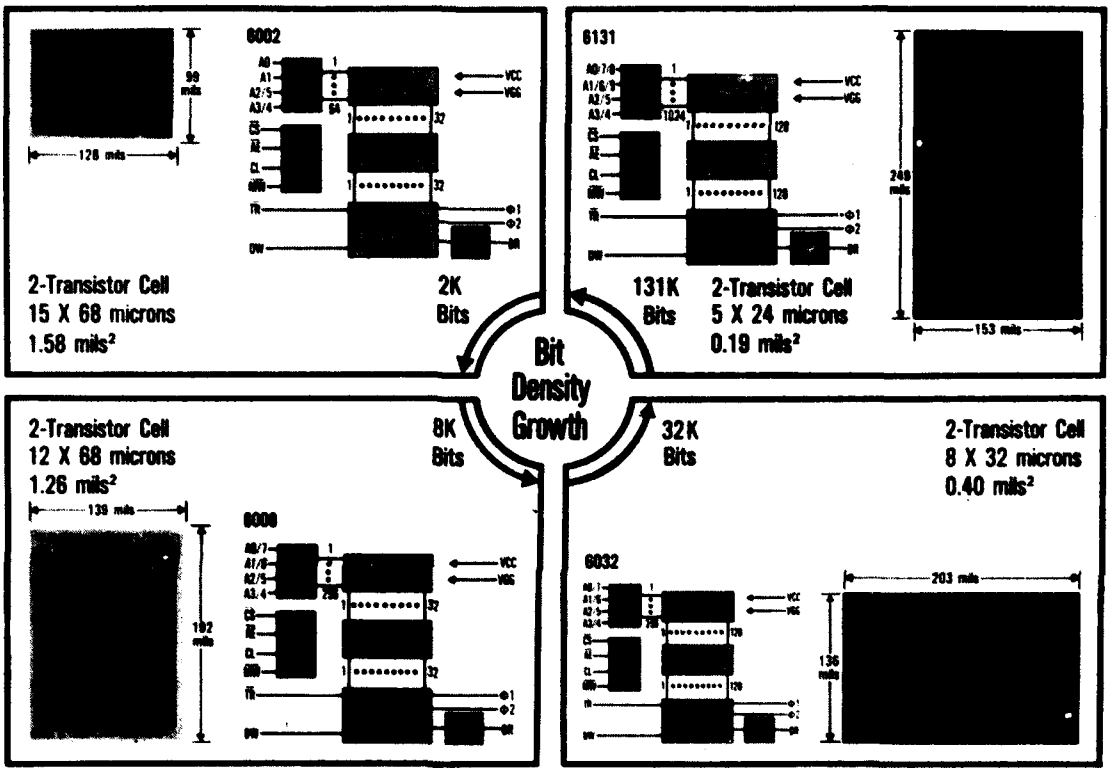


**Figure 4. MNOS BORAM Chip Bit Density Growth Plan**

### 3.3 Packaging Economics

Multichip hybrid microcircuits offer obvious benefits in terms of packaging density, but economic advantages are not so obvious. The MNOS BORAM hybrid was planned to achieve lower production cost per chip than discrete chip packaging. Cost studies were limited to the case of production to military criteria.

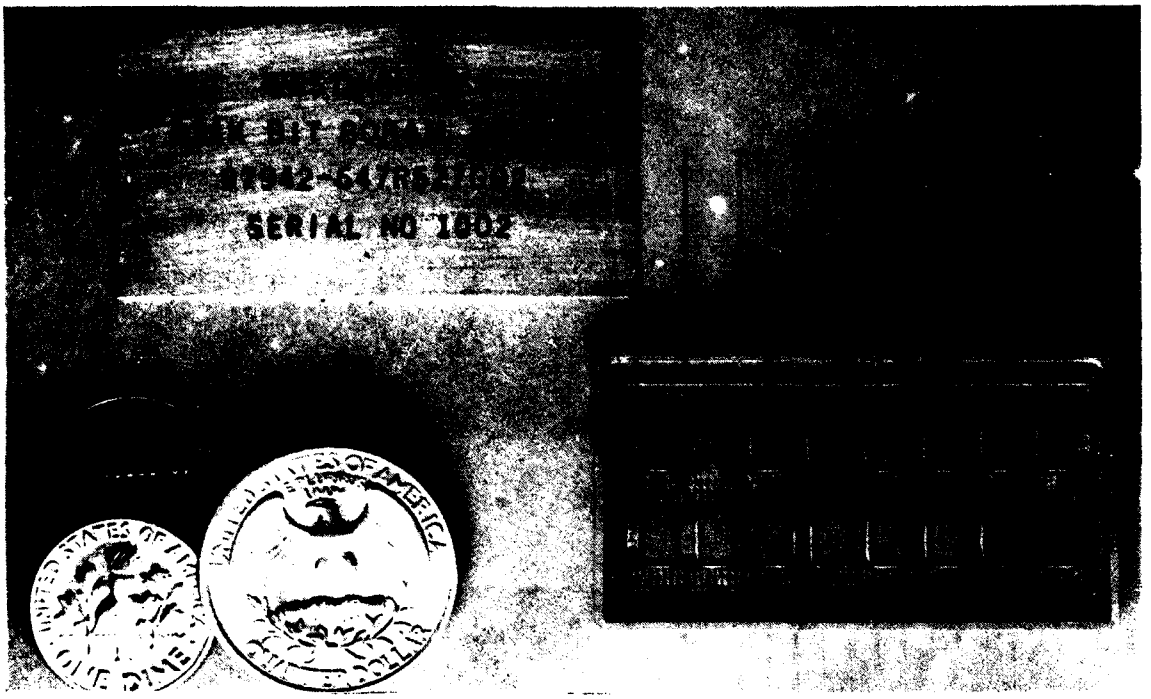


**Figure 5. MNOS BORAM Hybrid Microcircuit**

A simplified comparison of production costs for one hybrid versus 16 discrete packages is presented in figure 7. Hybrid assembly costs exceed the discrete package assembly cost, but given a high degree of automation that difference becomes unimportant. The dominant cost is screening, and this is where a cost advantage exists for the hybrid circuit approach.

The relative factors given for the cost elements will change as the manufacturing technology changes. The advent of tape automated bonding will reduce the hybrid assembly cost and the assembly rework factor. Electrical screening of tape mounted die before hybrid assembly will also reduce the overall screening costs.

### 3.4 Memory Card and System Configurations

Availability of a standard hybrid circuit configuration will avoid system redesign as product growth occurs. Memory card configurations need not be changed at all. Memory system controllers need only vary to accommodate the larger addressing space available with new chips. In most controller designs this means a modification of firmware.

The concept of transparent growth has been demonstrated by the operation of a memory system which can be populated with either 2K chips or 8K chips. In this case, the 2K-bit chip memory card was mechanically identical with the 8K chip memory card. The software instructions to the memory indicated whether a 2K- or 8K-chip card was being accessed.

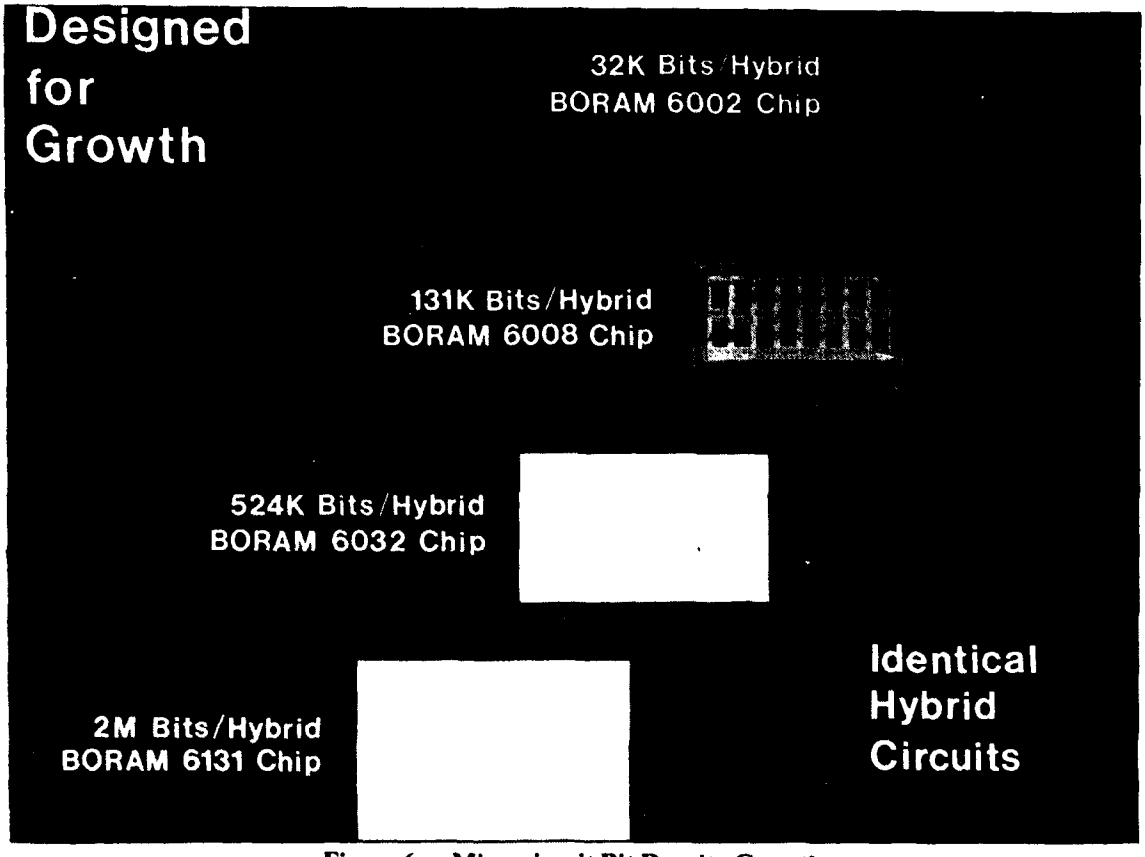


**Figure 6. Microcircuit Bit Density Growth**

## 4. MICROCIRCUIT STRUCTURE

The BORAM hybrid microcircuit has been purposely limited in complexity in order to promote low cost production and flexibility in implementation. The design of any given element in the microcircuit is viewed as being subject to evolutionary improvement. Figure 8 shows the present configuration of substrate, epoxy for substrate attachment, metal package and metal stepped lid.

### 4.1 Substrate Structure

Electrical interconnection and mechanical support of the BORAM monolithic chips is provided by a multilayer ceramic substrate. Figure 9 shows the major features of the present design. The labor required for manufacture was reduced by screening six substrates on a single piece of alumina. After completion of all screening and firing operations the individual substrates were separated by sawing.

The substrate layout allows manual or automatic wirebonding. Also, the pads are configured for tape carrier mounted chips.

Flat Package

$F = 20D+20M+20A+(16+\frac{1}{2}(4))S$

D bare die
M flat pack material
A flat pack assembly
S flat pack screen

Hybrid Package

$H = 20D+m+k_1a+k_2s$

D bare die
m hybrid material
$k_1$ rework factor
a hybrid assembly
$k_2$ rescreen factor
s hybrid screen

Approximations: $m \approx 15M$, $a \approx 18A$,
$s \approx 1.5S$, $k_1 = 1.25$, $k_2 \approx 2$

$$F = 20D + 20M + 20.0A + 18S$$
$$H = 20D + 15M + 22.5A + 3S$$

$$F - H = 5M - 2.5A + 15S$$

The flat package is more expensive in terms of material and screening costs. Screening is the dominate factor. Hybrids require more assembly labor. This difference becomes negligible as the degree of automation is increased.

**Figure 7. Discrete Versus Hybrid Package Economic Comparison**

### 4.2 Wire Bonding

The most labor intensive assembly operation is wire bonding. The BORAM 6000 series chips have 15 pads. Thus 240 wire bonds are needed for the 16 chips in the hybrid. In addition there are 12 substrate to package post bonds, and 32 internal jumper wire bonds.

The jumper wire bonds were included to facilitate circuit analysis and repair during manufacture. As shown in figure 10 most of the signals are common to all 16 chips. The VCC and VGG connections to any individual chip may be removed by lifting a jumper wire. Thus a defective chip may be isolated without disturbing the chip wire bonds.

Wire bonding of the BORAM hybrid was originally a manual operation. An operator would use 0.001 inch gold wire in an ultrasonic bonder to connect each chip. The use of ultrasonics avoided prolonged high temperature exposure during processing.

At a later date, the throughput and reliability of bonding was improved by the introduction of a computer controlled wire bonder. The automatic system consisted of an ultrasonic bonder, a master console, a disk memory, an operator's control pendant, and a power supply.

In the future, tape automated bonding will be employed for the BORAM hybrid. Table 1 shows the approximate facility cost, assembly time and bond strengths of the three bonding approaches.

Tape mounted chips will be electrically tested and burned in prior to insertion into the hybrid. This capability is expected to reduce die replacement to almost zero.

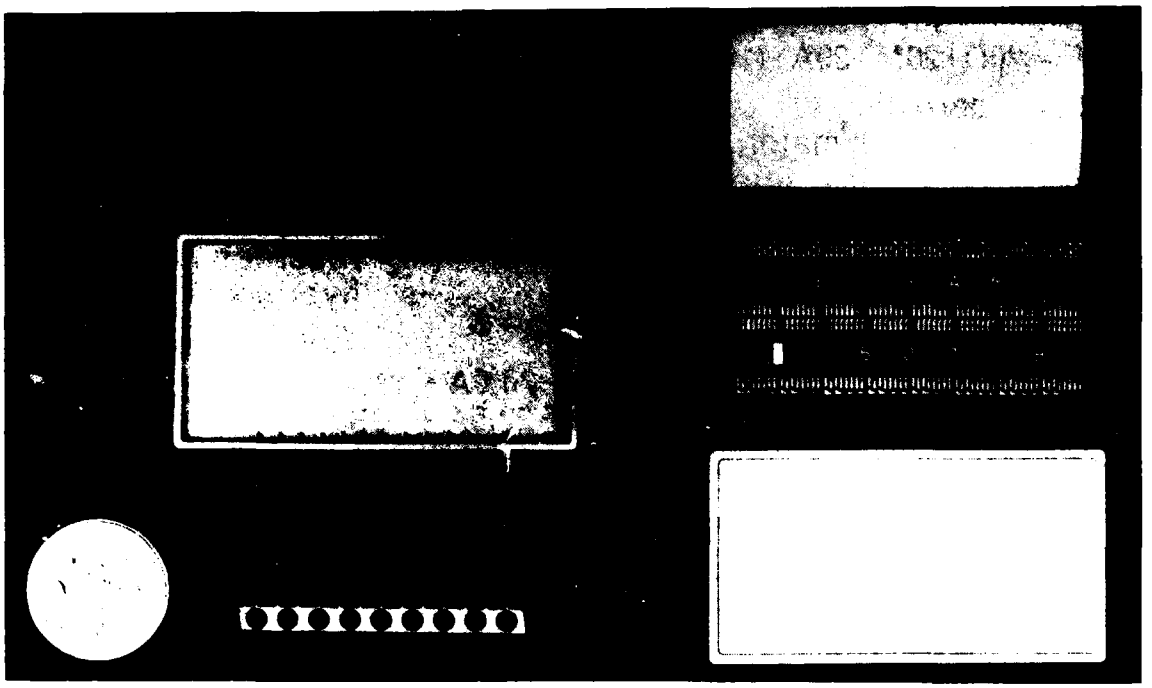

**Figure 8. Elements of the BORAM Hybrid Microcircuit**

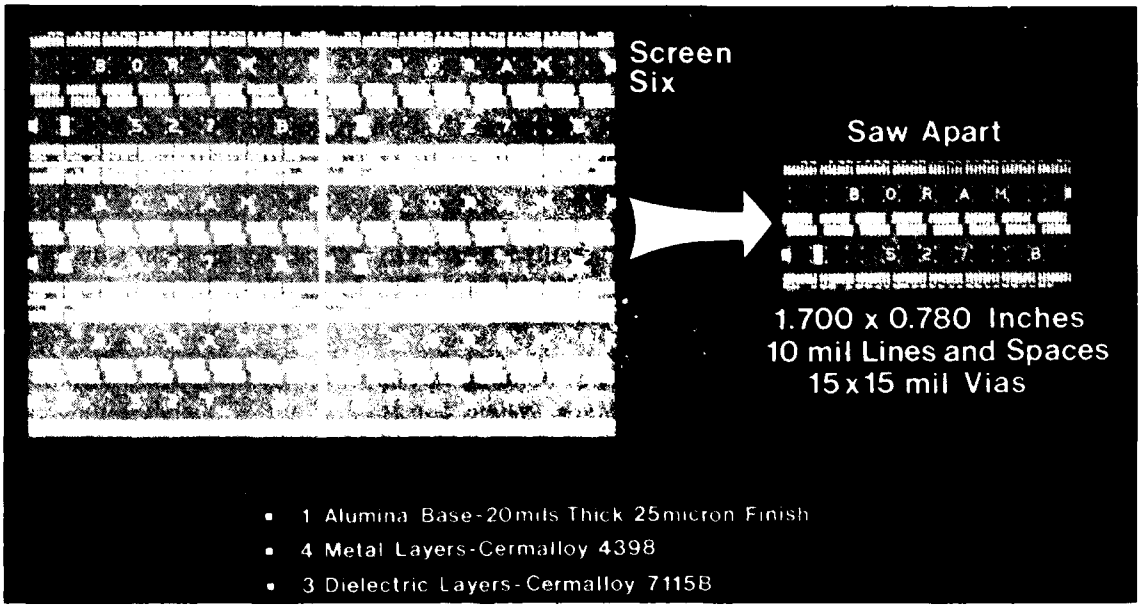


**Figure 9. Multilayer Ceramic Substrate**

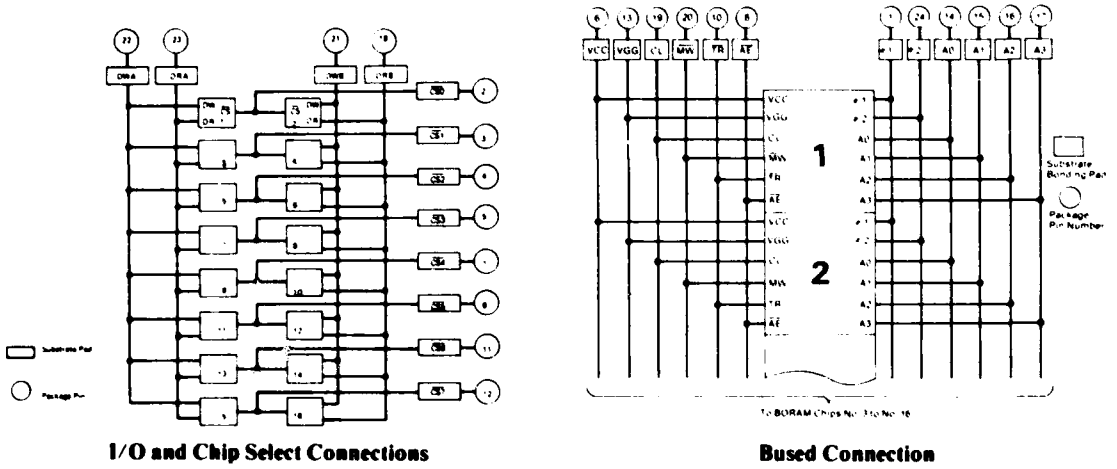


**Figure 10. BORAM Hybrid Circuit Schematic**

**Table 1. Comparison of Bonding Approaches**

| Approach | Cost Minimum Facility | Assembly Time* (Minutes) | Bond Strength (grams) |
|---|---|---|---|
| Manual Wire Bonding | 7-10K | 88 | 10 ± 2 |
| Automatic Wire Bonding | 35-65K | 25 | 10 ± 2 |
| Tape Automated Bonding | 425K | 10 | 50 ± 15 |

*Includes die mount, wire bond, tail pull, 100% pull test and inspection as applicable for each approach.

### 4.3 Microcircuit Package and Lid

The metal case measures 1.036 by 1.925 by 0.120 inches. The 24 leads are on 0.1 inch centers, and the leads are usually formed at a 1.200 spacing. Pin 1 and 2 and pin 23 and 24 are spaced 0.200 inches to provide a keying feature. The circuit board footprint for a tenth inch grid is 1.3 × 2.0 inches.

The package is specified to allow the option of gold coating or nickel coating. The lid may be welded or soldered.

The preferred approach for sealing is welding. A stepped lid provides a reliable seal which increases the package height by a minimal amount. Yields through hermeticity tests approach 100 percent. Of course, the need for an expensive solder preform is eliminated, and the reliability hazzard of solder particles is avoided.

The welded lid opens up the possibility for repairing hybrids without destroying the package. Techniques have been developed for the removal of the lid, and for the successful resealing of the package. This ability to delid, rework and reliably reseal a hybrid opens up new opportunities for improved economics.

## 5. SUMMARY

An economical 1 by 2-inch MNOS BORAM hybrid microcircuit has been developed, and is beginning to be applied in military systems. The hybrid circuit is configured to accept a series of pin compatible memory chips of increasing bit density. Each element of the microcircuit has been planned to allow flexibility in implementation approach and in manufacturing technology. Over the next decade it is expected that the hybrid will be used in significant volume, and that the form of the hybrid will under go evolutionary improvements to maintain economic viability.

## ACKNOWLEDGEMENT

The MNOS BORAM microcircuit development was primarily funded by a US Army Manufacturing Methods project contract DAAB07-76-C-0048. Mr. Herbert Mette of ERADCOM was the technical monitor of that effort. The Westinghouse Electric Corporation performed the development, and has provided significant funding to advance the technology and establish capital facilities. Associated Navy and Air Force contracts have also advanced specific aspects of BORAM development.

# HERMETIC CHIP CARRIER PACKAGING

BY

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## ABSTRACT

An overview of the progress made in bringing the hermetic chip carrier from the development stage to production is presented.

## INTRODUCTION

The multiplicity of technical challenges involved in the development of the hermetic chip carrier have been successfully addressed through a close working relationship with technical personnel in both industry and government. As a result, a significant number of new military designs utilize hermetic chip carriers, thereby achieving performance, reliability, and packing-density goals that would have been impossible to achieve with conventional technology.

## CHIP-CARRIER PACKAGE DEVELOPMENT

The chip carrier is a square, leadless package for integrated circuits. It is made with the same materials and processes that have been used in making high-reliability ceramic DIP's. Fig. 1 shows the typical construction of a three-layer, bottom-contact chip carrier compared with a DIP of the same lead count. The chip carrier is essentially the center portion of the DIP with the two rows of metal leads replaced by the contact pads on all four sides. As with the DIP, screen-printed metallized traces extend from the internal bonding pads to the external contacts.

The chip carriers, developed by 3M Co. of St. Paul, Minn., are now being produced by 3M and Kyocera International, Inc., San Diego, CA. A wide variety of chip-carrier packages are available with input/output counts ranging from 16 to 84 in both rectangular and square formats.

Despite the obvious size, weight, performance, and cost advantages of the ceramic chip-carrier package, its use by manufacturers in the volume production of integrated circuits was slow in gaining acceptance because of the following factors:

- Lack of standardization
- Incompatibility with printed circuit boards
- Unavailability
- High cost
- Unavailability of automatic mounting and insertion equipment

As a result of these concerns, the Air Force Materials Laboratory at Wright-Patterson AFB, Ohio, with support from the Naval Air Systems Command, funded three parallel programs which addressed many of the above issues. The three contractors chosen were Texas Instruments, Hughes, and RCA. Each contractor had essentially the same design goals and objectives, Table I.

In achieving these design goals, the three contractors developed two package outlines having three package styles, Table II. The 50-mil packages are used on printed circuit boards, whereas the 40-mil packages have been optimized for space-critical applications. In these space-critical applications, fine-line board-pattern technology is used, and the 40-mil chip carrier is attached to ceramic boards by means of solder reflow. This application of chip carriers is a viable alternative to wire-bonded chips on hybrid substrates.

As of this writing, the three contractors have met most of their goals:

| | |
|---|---|
| Standardization | - JEDEC standards have been established for 40-mil and 50-mil packages. |
| Manufacturability | - Standardized chip carriers, in addition to test sockets and environmental handlers, are available from package vendors. |
| High Reliabilty | - The chip-carrier approach was chosen by the Jet Propulsion Laboratory for Project Galileo, a Jupiter probe. Several thousand chip carriers are scheduled to be delivered to an equivalent Class S specification. |
| Automation | - Progress is continuing to be made by the three contractors with each taking a somewhat different approach to the development of automated assemblies and test handlers. |
| Technology Dissemination | - There has been an excellent interchange within industry and government of documentation concerning the techniques and processes employed in the manufacture of chip carriers. |

## HYBRID-CIRCUIT APPLICATIONS

Although hybrid packaging provides the advantage of high density with attendant volume and weight reduction, the difficulty of constructing and testing reliable hybrids has increased with the complexity of the chips. It has become more difficult to achieve high yield because of the inability to

adequately screen and test chips and substrates before assembly, and because wire-bonding assembly itself is not always a high-yield process. These problems, which reduce yield and raise costs, are further compounded by the problem of repair after sealing (opening the large hermetic seal, repairing the chip, and then resealing to hermetic condtions). Repair can only be accomplished by skilled people in a special hybrid facility.

In military applications, the major advantage to a hybrid manufacturer in procuring I.C.'s in hermetic chip-carrier packages, as opposed to unpackaged chips, is the level of screening that can be obtained with the chip-carrier packages. Depending upon the application, unpackaged chips are purchased to a specification that includes 100-percent wafer probe, 100-percent visual inspection, and a lot acceptance test. The lot acceptance test consists of packaging a random sample of chips from the lot and subjecting the sample to a series of qualification tests, Table III. If the sample meets the qualification requirements, the remainder of the lot is shipped as unpackaged chips. This procedure works well for mature products because the sample selected truly represents the population, and the fallout from the various qualification tests is minimal. However, in the case of state-of-the-art LSI/VLSI devices, the purchase of unpackaged chips could be very costly to the hybrid manufacturer. The net count of chips per wafer for large LSI devices is relatively low, making it impractical to perform a lot acceptance test, a requirement when selling unpackaged chips. It is in this area of unpackaged chips that the hermetic chip carrier offers a great advantage.

Devices packaged in hermetic chip carriers can be 100-percent subjected to equivalent Class S screening, as is now being done for JPL's Project Galileo, Fig. 2, or equivalent Class B screening, such as that proposed for the devices to be supplied for the Global Positioning System, GPS, receivers, Fig. 3. These devices are all LSI circuits that consume a large amount of area, Table IV. In each case, Project Galileo and GPS, fully screened and tested chips which minimize the amount of rework required by the hybrid manufacturer are being delivered. It is important to recognize that by using the chip-carrier approach, the chip manufacturer can perform a more complete electrical test, thereby enhancing product reliability.

The chip carrier has provided the high-density packaging engineer with an alternative to single-cavity hybrids that comes close to equaling the conventional hybrid packaging density and that also offers an additional advantage of easier tailoring of the size and shape of the ceramic substrate. This latter advantage has been used to tailor hybrid size and shape with chip carriers on ceramic substrates as illustrated by the following designs.

Processing Module For A "Smart" Sensor - Fig. 4

This substrate contains all of the CMOS or CMOS/SOS chips in hermetic chip carriers for A/D conversion and control and all microprocessor functions. Specifically, the chips are:

Microprocessor - CDP1802 or CDP1804
Multiplier - TCS132
A/D Converter
Control logic, Interface - CD4000 Series
I/O Port

Hybrid Memory for AN/UYK-44 or GPS - Fig. 5

This memory was constructed on a double-sided, Navy "Improved Standard Electronic Module," and contains 70 chips. Thirty-two 1k-memory chips plus four control chips are mounted and interconnected by multilayer, thick-film, ceramic substrates on each side of the module.

16-Bit Microprocessor CPU - Fig. 6

The high-speed 16-bit microprocessor was packaged in the JEDEC standardized 84-lead chip carriers with high-speed multiplier chips in 64-lead chip carriers.

## TECHNOLOGY TRANSFER

The transfer of chip-carrier technology from RCA's pilot line to its military-certified production assembly facility in Findlay, Ohio is being supported through additions to the Manufacturing Methods Technology, MMT, program now in progress. Phase I of this MMT add-on will concentrate on the design and development of hermetic chip carriers for rectangularly shaped memories. Phase II will transfer the hermetic chip-carrier technology from development to production with an objective of delivering screened devices to the Global Positioning System Program.

## SUMMARY

In summary, chip-carrier packaging will become the major packaging technology in military systems, and will find increasing application in commercial systems requiring LSI and VLSI technologies.

## ACKNOWLEDGMENT

The authors acknowledge and appreciate the technical contributions of John Bauer, Dan Hampel, and Richard Zeien to this paper.

**Table I · Design Goals**

| | |
|---|---|
| Standardization — | EIA/JEDEC Registration |
| Manufacturability of the Package — | Availability from multiple-package vendors |
| High Reliability — | Ability to meet the screening and conformance testing of Mil-Std-883 methods 5004 and 5005 |
| Automation — | Optimize the package design for automated processing and testing |
| Technology Dissemination — | Make available to industry the technology development to encourage the establishment of multiple sources |

**Table II · Package Development**

| Contractor | I/O Counts | JEDEC Standard Outline | Structure |
|---|---|---|---|
| RCA | 20,24,32,40, 48,64,84 | 40-mil surface mount | Three Layer |
| Hughes | 20,28,44,52, 68,84 | 50-mil surface mount | Three Layer |
| TI | 16,20,28,44 52,68,84 | 50-mil surface mount | Single Layer |

**Table III · Typical Lot Qualification Tests**

| | |
|---|---|
| Initial Electrical | · 25 °C DC, 5% to 10% PDA |
| Burn-In | · 160 hr., 125 °C |
| Post Burn-In Electrical | · 25 °C DC, LTPD 5 or 10 |
| Final Electrical | · − 55 °C, + 125 °C DC<br>+ 25 °C AC<br>3%-5% PDA |
| Life Test | · 1000 hr., 125 °C one time only or periodically |

**Table IV · Typical GPS Receiver Circuits**

| Circuit | Chip Size (in.) | Chip Area ($in^2$) |
|---|---|---|
| General Processing Unit | .205 × .216 | .0443 |
| Controller | .250 × .250 | .0625 |
| Address Select | .175 × .175 | .0306 |
| Register Select | .205 × .205 | .0625 |
| Bus Interrupt | .205 × .205 | .0625 |

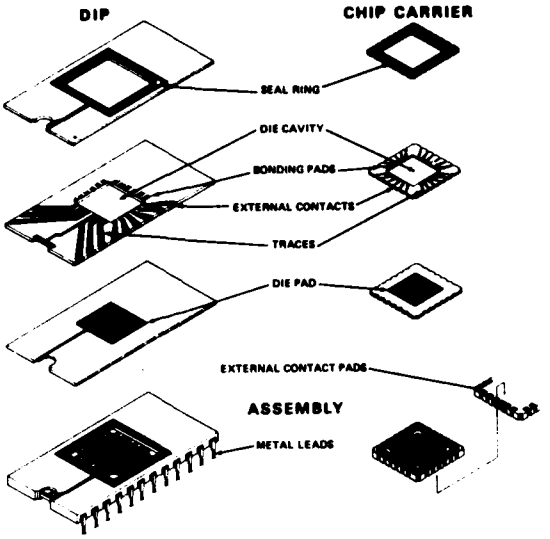


Fig. 1 - Exploded view of chip carrier and DIP.

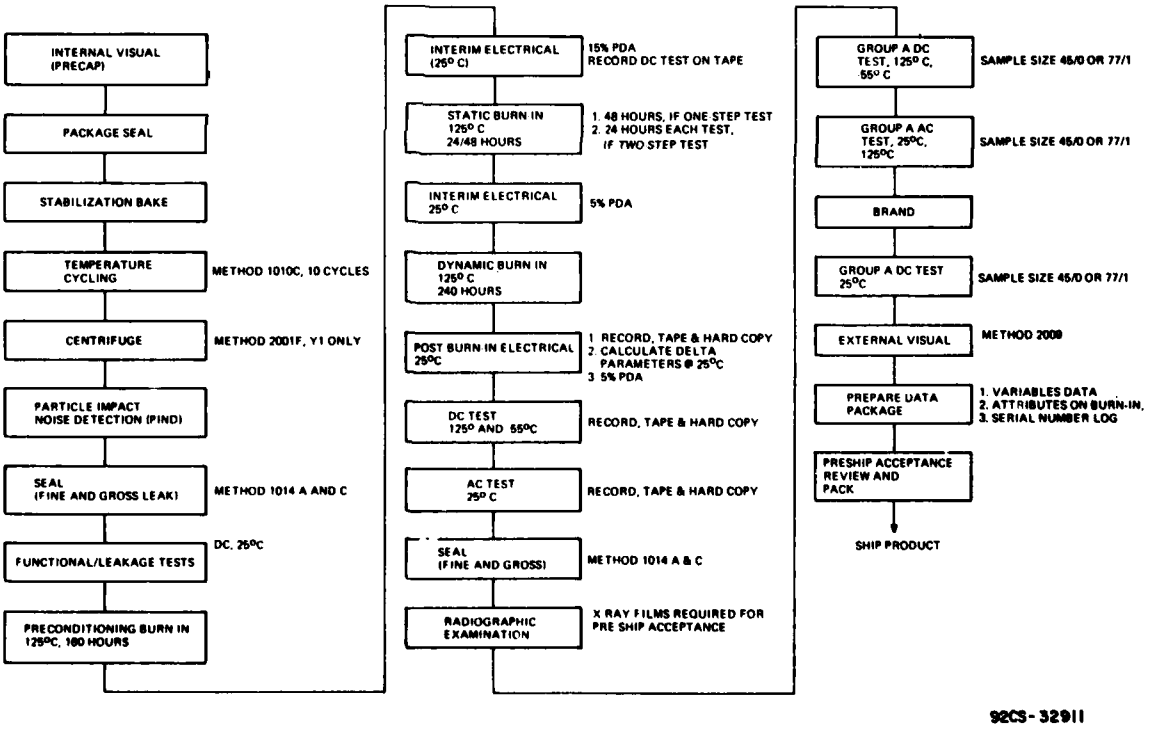


Fig. 2 - Equivalent Class S screen.

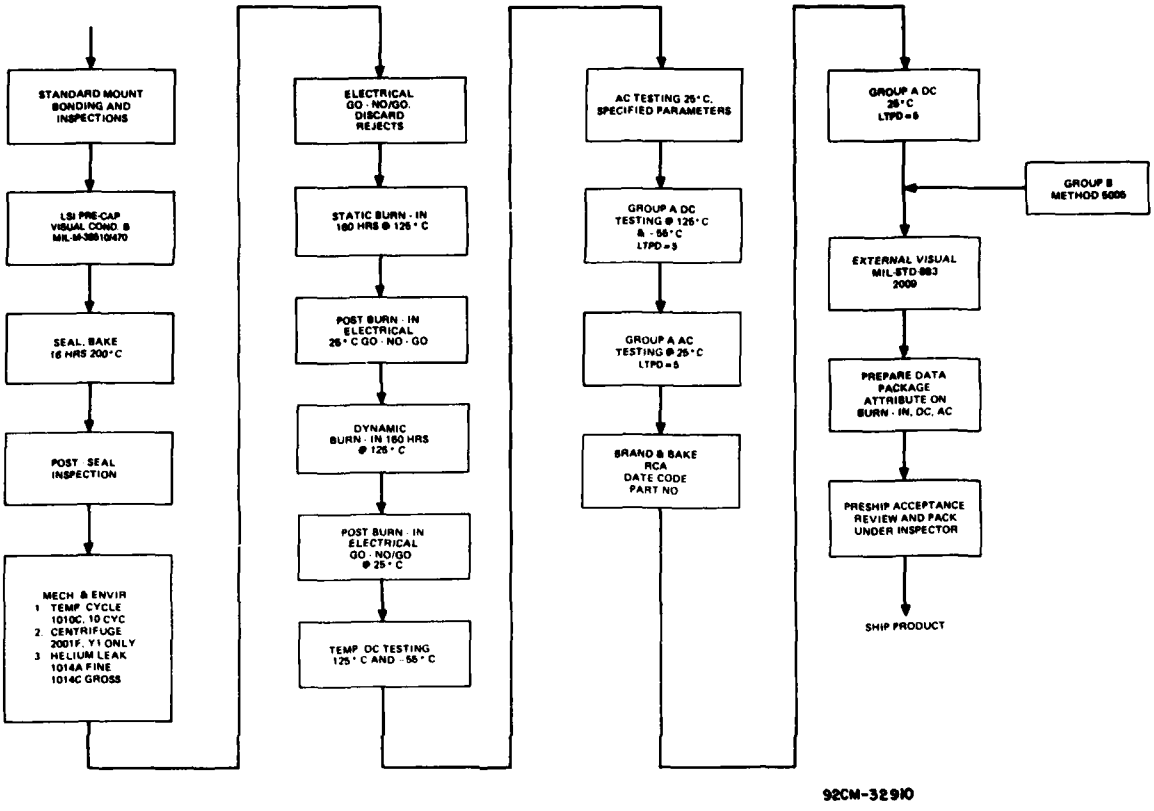


Fig. 3 - Equivalent Class B screen.

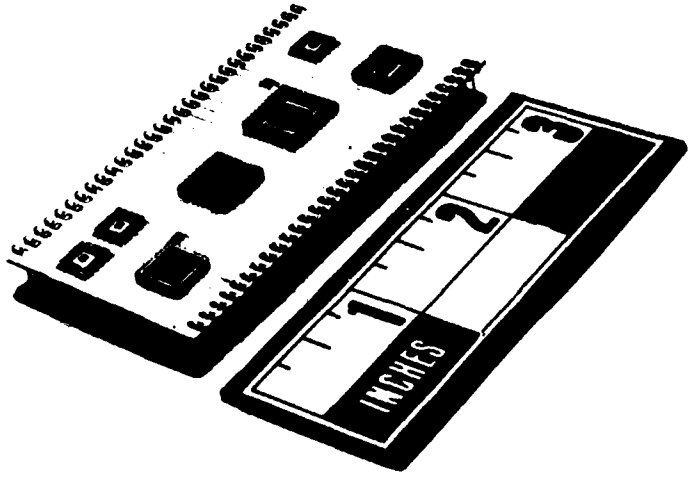


Fig. 4 - Processing module for a "smart" sensor.

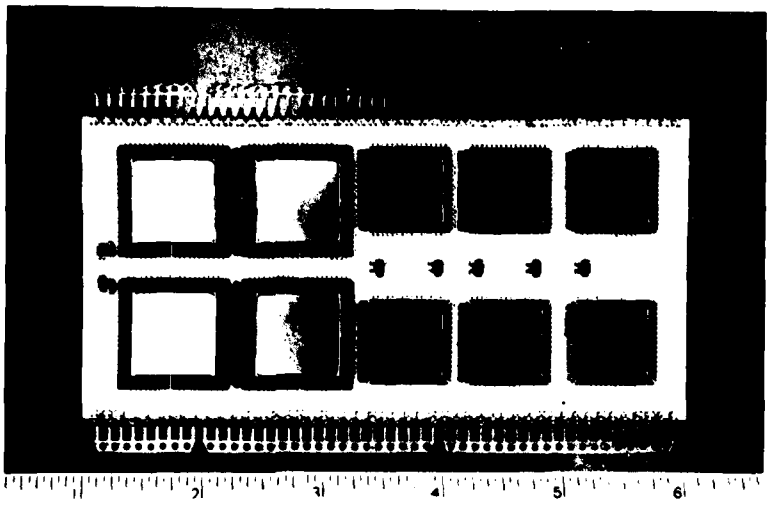

Fig. 5 - 70-chip double-sided hybrid (ISEM).

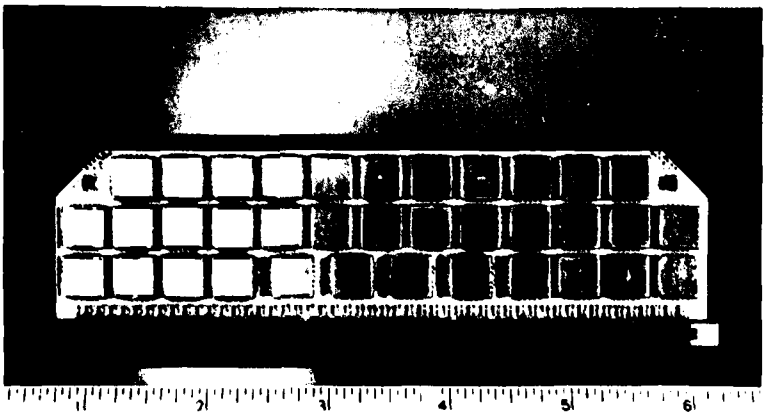

Fig. 6 - 16-bit microprocessor CPU with hardware multiplier.

# RELIABILITY EVALUATION OF PLASTIC ENCAPSULATED HYBRID MICROCIRCUIT DEVELOPED FOR ARMY FUZE APPLICATIONS*

BY:

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## ABSTRACT

A major Army rocket system may incorporate the use of an electronic fuze timer fabricated using two plastic encapsulated hybrid microcircuits and one encapsulated monolithic integrated circuit. The ET&DL at Fort Monmouth, NJ, was tasked with assessing the storage reliability of these devices through accelerated testing and detailed failure analysis to determine failure mechanisms. From this analysis, corrective actions would be proposed which could permit attainment of the desired reliability.

## INTRODUCTION

In an effort to reduce cost, an Army rocket system program considered the use of plastic encapsulated microcircuits in the electronic fuze timer circuit of this missle. The three device types used in the timer circuit are a precision hybrid oscillator, an interface hybrid and an MNOS monolithic memory/timer microcircuit.

These devices were the result of Manufacturing, Methods and Technology (MM&T) Programs managed by the Harry Diamond Laboratories. The objective of these programs was to define manufacturing methods for high volume/low cost devices. A pilot production lot was produced for each contract which demonstrated the contract requirements.

The ET&DL program objective was to obtain qualitative information on the long term storage reliability of each of the three devices. Screens and accelerated environmental tests were devised for this analysis.

## PROGRAM DESCRIPTION

The test program is outlined in the Flow Chart, Figure 1. Device quantities were dictated by availability of MM&T Pilot Line units.

* Project funded by ERADCOM, HDL, Adelphia, MD.

Device Description

a. 10 kHz Hybrid Microcircuit Oscillator - Figure 2 illustrates four stages in the packaging of this unit. Assembly features of this hybrid include:

(1) A tape automated bonded (TAB) amplifier chip. This chip uses aluminum interconnect metallization, passivation of $SiO_2$ and CVD $Si_3N_4$, gold bonding bumps, and eight tin plated copper leads.

(2) The thick-film alumina substrate contains (see Figure 3) the TAB amplifier chip, four chip capacitors, and three thick film resistors.

(3) Component mounting techniques: amplifier chip epoxy mounted using Ablestik 789-3 non-conductive epoxy; capacitors and three external leads attached by solder reflow.

(4) Conformal coating over entire substrate using Dow Corning R6100 silicone junction coating.

(5) Final package assembly: immersion of assembled substrate into a formed metal can with a ground terminal, filled with Hysol ES4128 epoxy encapsulant. The purpose of the metal can is to provide electrical shielding.

b. Interface Hybrid Microcircuit - Figure 4 shows the substrate layout of the interface hybrid. Assembly features are:

(1) The custom monolithic IC chip. Aluminum metallization is used at bonding pads and interconnects. Ball bonded gold wires are used from chip to substrate. There is no passivation over the metallization. The die attachment to the substrate is accomplished using silver-loaded epoxy.

(2) A silicon controlled rectifier (SCR) chip. Die attach using gold-silicon eutectic bonding.

(3) Bonding of leads to substrate is performed using a solder paste and solder reflow. The package is an oversized 14 lead dual in-line configuration, 1.410 cm X 2.172 cm (0.555 in X 0.855 in).

(4) Jumper wires on substrate. Four gold wires are used to connect various substrate conductors.

(5) Encapsulation technique. Hysol Epoxy ES4228 is used as a coating over the IC and SCR chips and the four jumper wires prior to package molding with Dow Corning 307 silicone encapsulant.

c. Memory/Timer - This is an MNOS monolithic microcircuit, with a chip measurement of 0.249 x 0.191 cm (0.098 x 0.075 in), which is packaged in a 16 pin dual in-line plastic package. The encapsulant is Allied 2929B epoxy novalac. The lead frame consists of alloy-42, with selectively gold plated

wirebond areas and solder dipped leads. The chip has aluminum interconnect metallization and bonding pads, plasma deposited silicon nitride passivation, eutectic die bonding and thermal compression gold wire bonds. A photo-micrograph of the chip is shown in Figure 5.

## TEST PROCEDURE

The tests were conducted as outlined in the flow chart in Figure 1. Measurements made at 25°C were repeated at 100°C for the initial end point tests for thermal shock. Testing was conducted and is described in the following sections. A fuze timer test circuit, comprised of a test fixture and a XM36E1 Fuze Setter, was used for functional End Point Tests. Failure criteria was: 1) improper operation of the fuze timer circuit evidenced by erratic, dc or no oscillator output, no pulse output for the interface and memory/timer and/or 2) and error indication in the fuze setter LED display, at either 25°C or 100°C. Functional testing began one hour after removal from test and was completed within four hours.

Burn-in for all devices was performed in accordance with Method 1015.2, MIL-STD-883B, bias life test. Bias was applied to each unit for 168 hours at 125°C. End point measurements were performed at 25°C.

The thermal shock test was conducted in accordance with Method 1011.2, MIL-STD-883B, Test Condition B (-55°C to 125°C). A total of 50 memory/timers, 50 oscillators, and five interfaces were subjected to 30 test cycles. Upon completion of the 30 cycles, 25 timers and 40 oscillators were transferred to the humidity test. The remaining 25 timers, 10 oscillators, and five interfaces were subjected to 300 cycles in 30 cycle increments, and thereafter to a total of 2000 cycles in 100 cycle increments. End point measurements were made at both 25°C and 100°C.

Humidity testing was performed in accordance with the test method developed by ET&DL. A total of 175 timers, 93 oscillators, and 20 interfaces were put on test. End points were measured at approximately 25, 50, 100, 150 and 250 hours and at increasingly longer intervals. End point measurements were made at 25°C.

The end point measurement test circuit is shown in Figure 6. A "Static-Safe" work station was developed for handling the MNOS timer. The work surface was covered with conductive foil and grounded. Test personnel at the work station were equipped with a wrist band in direct contact with the skin and grounded. Figure 7 shows the "Static-Safe" work station including the test fixture which simulates the fuze timer circuit, the XM36E1 Fuze Setter and test meters. The fuze time is manually set using the XM36E1 Fuze Setter and the time is presented by an LED display. A catastrophic failure in the fuze timer circuit or setter will cause the display to indicate error, "E". The end point measurement procedure follows:

a. Memory/Timer

Measurements are made at 25°C. The device under test, DUT, is inserted in the test fixture. Power is switched "ON" and current drain measured (current drain limits are 2.5mA minimum and 11 mA maximum) With power "OFF", fuze setter settings of 178.6 seconds and 4.0 seconds, respectively, are applied to the test fixture. Power is switched "ON" and output waveform observed on an oscilloscope. A typical output waveform is shown in Figure 8. For the thermal shock test, the above measurements are repeated at 100°C.

b. Oscillator

Measurements are made at 25°C. The DUT is inserted in the test fixture. Power is switched "ON" and average current drain measured (current drain limit is 2.7 mA maximum). The output duty cycle and period are measured using an oscilloscope (duty cycle limits are 45 to 50% and period limits are 96 us minimum and 107 us maximum). If the period is marginal, a more precise measurement is made using a HP 5304A Timer/Counter. Typical output waveform is shown in Figure 9. For the thermal shock test, the above measurements are repeated at 100°C.

c. Interface

Measurements are made at 25°C. The DUT is inserted in the test fixture. With power "OFF", a fuze setter setting at 4.0 seconds is applied to the test fixture. Power is switched "ON" and output waveform observed on an oscilloscope. The required output waveform is the same as for the memory/timer. For the thermal shock test, the above measurements are repeated at 100°C.

## TEST RESULTS

Pre- and Post Burn-In:

The following table indicates the number of units tested and the total number of failures for each device type:

| | Units Tested | Failures Pre Burn-In | Failures Post Burn-In |
|---|---|---|---|
| Oscillator | 110 | 5 | 2 |
| Interface | 25 | 0 | 0 |
| Memory/Timer | 200 | 0 | 0 |

a. Thermal Shock:

After completion of the initial 30 cycles of thermal shock, 40 oscillator units and 25 memory/timer units, were removed and placed on the 85°C/85% RH test. The cumulative failures at each readout (in cycles) are shown below:

Thermal Shock Cycles (-55°C to +125°C)

| | Units Tested | 30 | Units Remaining | 60 | 150 | 500 | 600 | 700 | 800 | 900 | 1000 | 1500 | 1600 | 2000 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Oscillator | 50 | 0 | 10 | 0 | 0 | 1 | 2 | 5 | 6 | 7 | 8 | 9 | 10 | |
| Interface | 5 | 3 | 2 | 5 | | | | | | | | | | |
| Memory/Timer | 50 | 0 | 25 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

100% of the oscillators (10/10) failed after 1600 cycles. Total failure of the interface devices (5/5) occurred after only 60 cycles.

b. Steady State Humidity (85°C/85% RH) :

The total number of oscillator and memory/timer devices included 40 and 25 units, respectively, that had received 30 cycles of thermal shock. The cumulative failures for each readout (in hours) are presented below:

| | Units Tested | 87 | 179 | 314 | 428 | 570 | 733 | 897 | 1062 | 1120 | 1222 | 1382 | 1427 | 1582 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Oscillator | 93 | 1 | 4 | 5 | 11 | 12 | 15 | 20 | 30 | | 32 | 34 | | 34 |
| Interface | 20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | | 4 | | | 5 |
| Memory/Timer | 175 | 0 | 0 | 0 | | 1 | | | | 2 | | | 3 | |

Because of the large number of memory/timer devices and the time required to make the electrical measurements, readings were not made at every interval. Many of the failed oscillators were observed to recover after a period of time. This would occur usually after storage at room temperature for 24 hours. The recovery effect is discussed in the next section.

## DISCUSSION OF RESULTS

Test results on the memory/timer device evaluation indicate high quality (evident by zero failure on pre- and post burn-in electrical) and possibly high reliability. At 85°C/85% RH, with the limited amount of data, the median life is predictated to be 100,000 hours. Electrical performance of the first failure varied from normal to partial output pulse, no output pulse, or no output recovery. The second failure occurred after 1120 hours. Output did not recover and the fuze setter displayed an "E" reading. The third failure had no output pulse and the fuze setter displayed an "E" reading.

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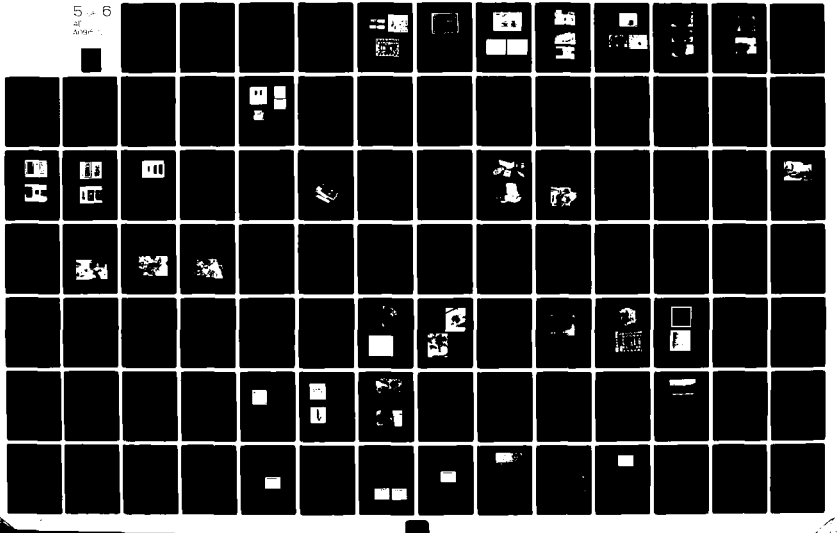


The seven oscillator failures that occurred after pre- and post burn-in electrical is not alarming, assuming the oscillator manufacturer did not perform similar screens. A reject rate of 4.5% after initial electrical and 2% after burn-in are within industry standards.

Device end point measurements were made for thermal shock and humidity tests after a one hour drying period. For many of the oscillator failures, maintained at room temperature, end point tests repeated within 24 hours indicated normal operation. These "restored" devices were returned to the environmental test and failed again on subsequent end point measurements. This failure/recovery cycle usually occurred several times until no recovery was observed.

Tests were conducted to determine the presence of electrical discontinuity in oscillators that passed end point tests at 25°C and failed at 100°C. Resistance measurements between pins for all pin combinations showed either stable or decreasing resistance for a temperature change from 25°C to 100°C.

Interface thermal shock failures included: no fuze setter display, "E" setter display, no output pulse, and/or no recovery of output pulse. The initial humidity failure at 897 hours was a sudden output pulse shift from the normal -21V to -26V at 0.5 seconds. The three additional humidity failures showed no output pulse and an "E" displayed in the fuze setter.

A significant finding was the importance of the 100°C parameter end point measurement following thermal shock. Of the 10 oscillator failures recorded, only 30% failed at room temperature while 70% failed at 100°C.

Preconditioning of the oscillator and memory/timer units with 30 cycles of thermal shock was not significant. Eight of the 32 oscillator humidity failures (23%) had been subjected to the 30 cycles of thermal shock. None of the three memory/timer humidity failures had been preconditioned by thermal shock.

## FAILURE ANALYSIS

a. Procedure:

Standard failure analysis procedures were used in this investigation. Non-destructive electrical and X-ray radiographic techniques were performed prior to removal of encapsulation. Optical microscopy generated the most useful data. The SEM was used when required.

The procedure developed for removal of the device from its package is detailed below.

b. Oscillator:

The metal package was removed by grinding an edge on either side to the epoxy encapsulant. The shield was then pulled from the unit allowing the encapsulated assembly to be removed. Removal of the epoxy encapsulant and silicone junction coating was accomplished by immersion in heated Uresolve Plus solvent for several hours.

c. Interface

The bulk of the silicone encapsulant was removed by an abrasion tool. The remaining encapsulant is removed using the same procedure used with the oscillator.

d. Memory/Timer

A cavity is formed in the epoxy encapsulant above the chip using a Dumat grinding tool. The device is placed on a hot plate. Fuming nitric acid is dropped into the cavity in the package formed by the grinding tool. After several seconds the device is rinsed in acetone. This procedure is repeated until the chip is exposed.

e. Results

Few of the failures studied indicated problems normally experienced with plastic encapsulated devices: open wire after thermal shock; aluminum corrosion following humidity.

Figures 10 through 13 are examples of oscillator failures. Figures 10, 11 and 12 are failures from humidity testing and Figure 13 is a thermal shock failure. Two of the three humidity failures are due to chip capacitor problems. These two failures were the result of a cracked capacitor, C4. The third failure occurred due to fracture of the beam at pad 4 on the micro-circuit chip. These failure modes are not failures usually associated with humidity testing.

The thermal shock failure was again the result of a chip capacitor. Figure 13 shows capacitor C3 separated from the substrate. If this was a poor bond initially, then thermal shock testing could have caused a complete bond fracture to be complete. The result would have been an intermittent failure with temperature, which it was.

Figures 14 and 15 are two interface humidity failures. Figure 14 shows an open jumper wire between two substrate conductors. Figure 15 illustrates an open wire bond at Pad 18 of the microcircuit chip.

A deficiency with the interface hybrid is poor quality control, particularly regarding wire bonds. Figure 16 illustrates three different substrate conductor wire bonds. Figure 16A is a 390X SEM photomicrograph of a typical substrate wire bond. Over pressure by the bonding tool has completely flattened the ball and induced neck-down of the wire. Figures 16B and C show the same type of bond (130X magnification). This time, only part of the flattened bond exists because of the poor placement of the bond on the conductor. These problems could have been eliminated by precap visual inspection.

The one memory/timer unit analyzed failed the humidity test as a result of an open aluminum metallization near the bond pad, Figure 17. Figure 17A is a 110X dark field photomicrograph indicating missing aluminum in the conductor leading from the bonding pad. Under 150X magnification (Figure 17B) a defect in the aluminum at the interface between the silicon nitride passivation and aluminum, indicated by the dash lines, was the probable cause of failure. Moisture entered the package and chemically attacked the narrow aluminum conductor by direct access to the metal through the defect. This failure could have been avoided by precap visual inspection.

## CONCLUSIONS & RECOMMENDATIONS

The completed environmental testing and failure analysis does not indicate a plastic encapsulation related reliability problem. Results for the memory/timer monolithic microcircuit indicate excellent performance on both the thermal shock and 85$^{o}$C/85% RH tests. The median life of the memory/timer device at the accelerated 85$^{o}$C/85% RH test condition is predicted to be 100,000 hours using a Weibull probability plot (Figure 18).

The oscillator and interface failures cannot be attributed to the plastic encapsulation process. Classical failure mechanisms of aluminum corrosion or gold electrochemical reactions of devices tested in high humidity/temperature have not been observed. The problem of initial electrical failure of the oscillator after humidity testing, then recovery after a short drying period, could be classified as a packaging problem. However, improved packaging techniques and materials could possibly eliminate this effect.

Failure mechanisms attributed to the above two hybrid types are associated with assembly techniques and procedures. These include wire bond procedure, circuit layout and the solder reflow process.

The following recommendations are provided based on the tests and failure analysis performed:

a. Major changes in the assembly of the interface hybrid are required. Changes required include: improvement in wire bonding procedure; elimination of four jumper wires; use of standard lead frame assembly; use of accepted molding procedure and materials.

b. The oscillator hybrid requires a package redesign. Packaging should reflect accepted molding procedure and materials. A study should be made to determine the adequacy of solder reflow for component assembly.

c. Procurement of these devices should be by a specification drawing which requires screens, i.e., precap visual and burn-in, and Lot Acceptance Testing.

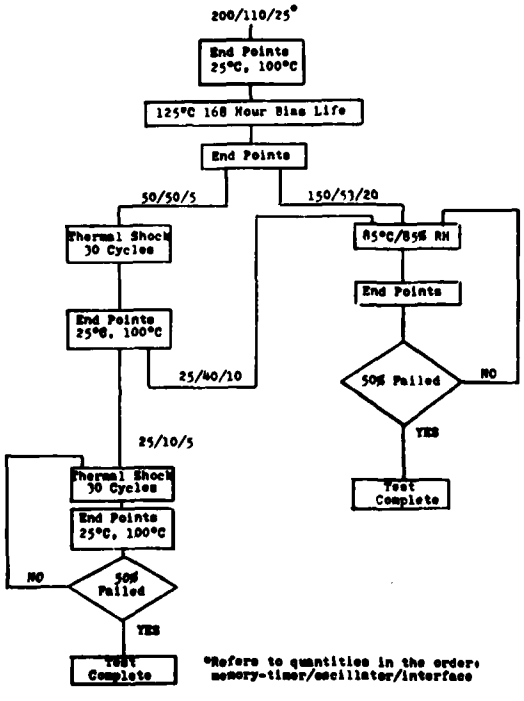



Figure 1. Test Program Flow Chart

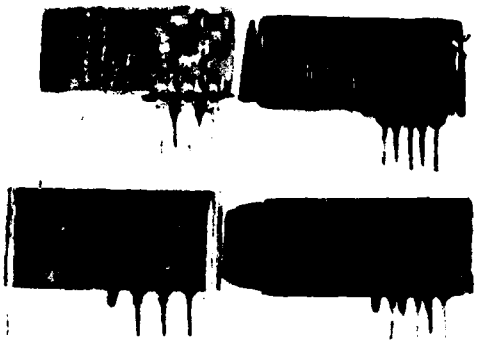


Figure 2. Oscillator Encapsulation Flow

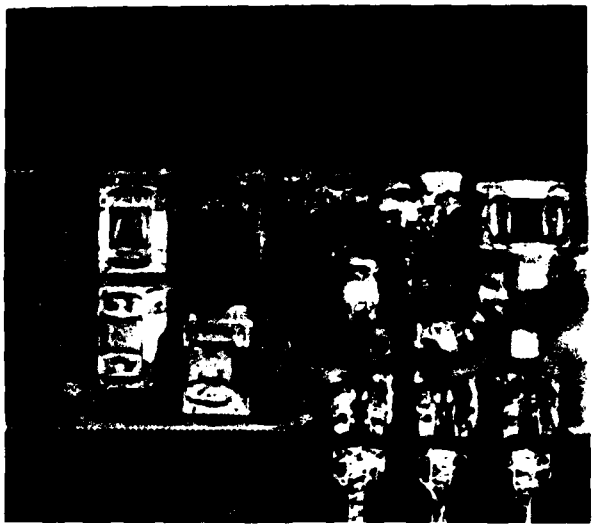


Figure 3. Photomicrograph of Oscillator Substrate

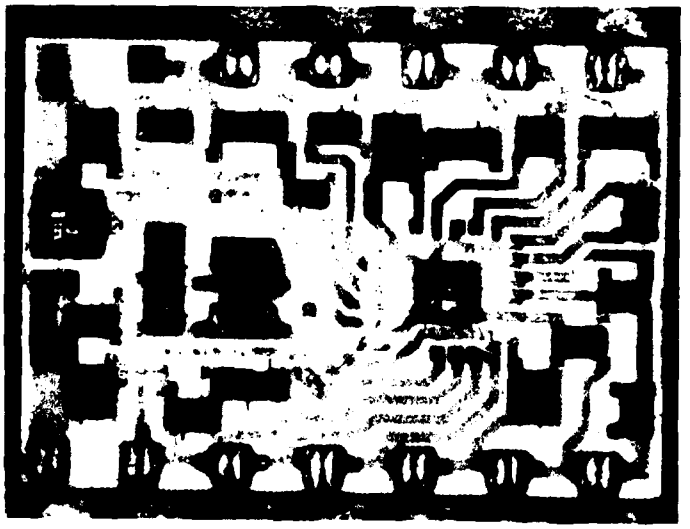


Figure 4. Interface Hybrid Substrate

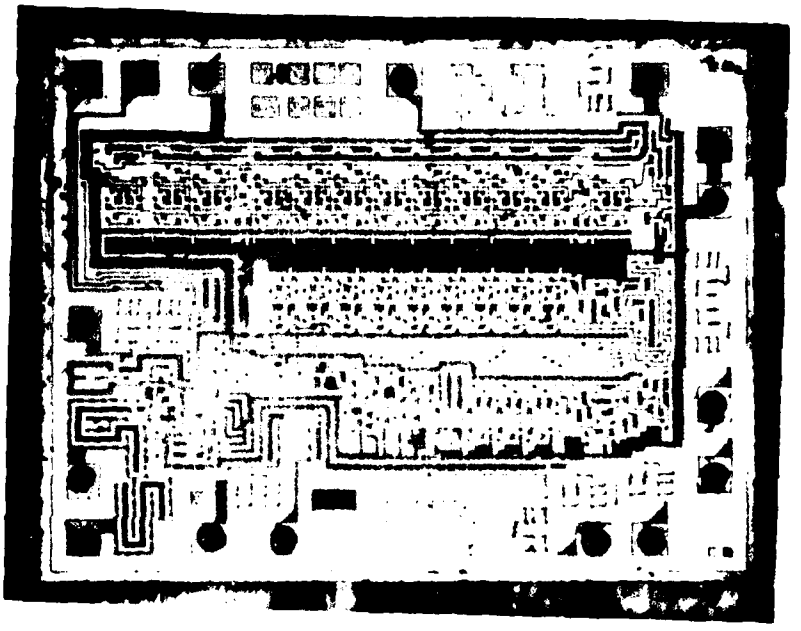


Figure 5. Memory/Timer Monolithic Chip

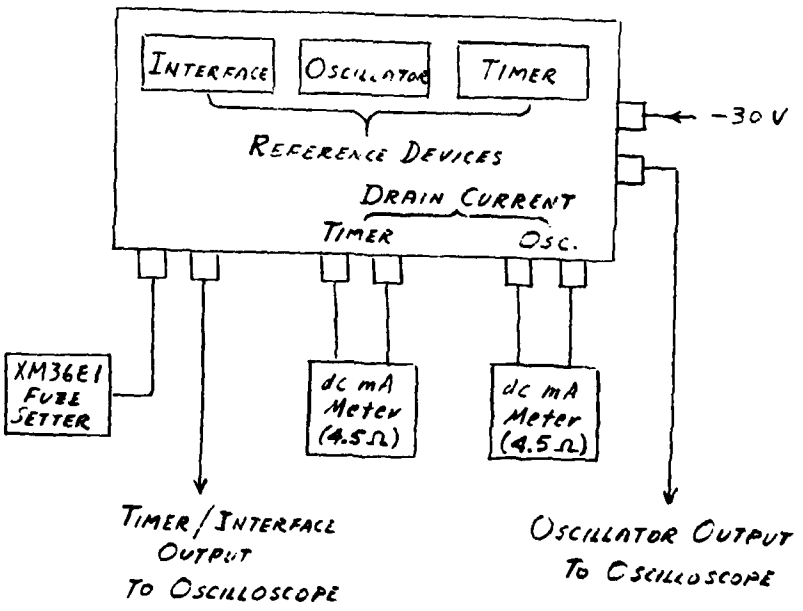



Figure 6. End Point Measurement Test Circuit

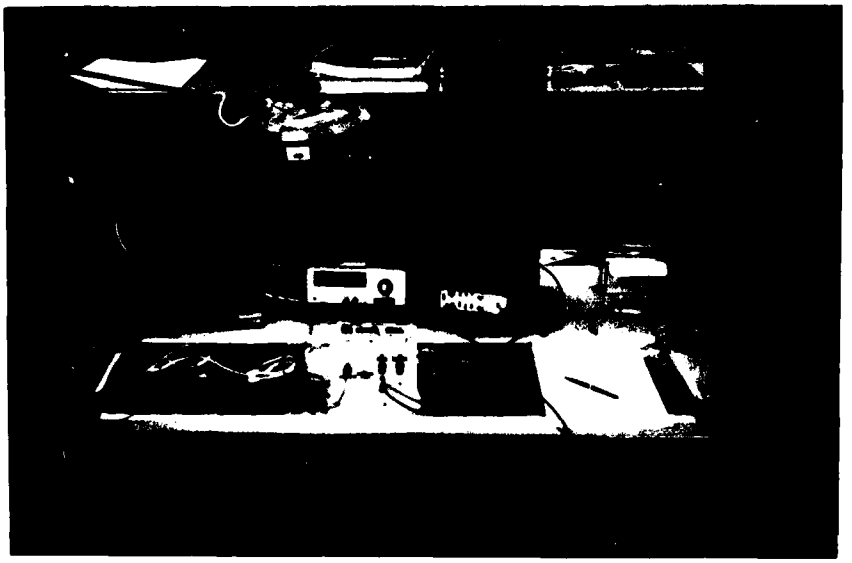


Figure 7. Static-Safe Work Station

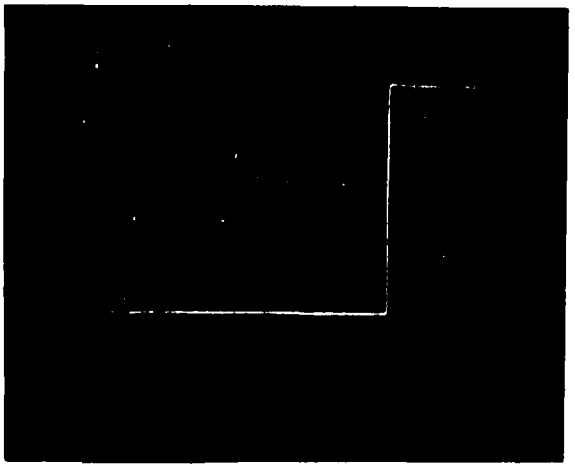


Figure 8. Output Waveform for Timer & Interface (Vertical 5v/div, Horizontal 500ms/div)

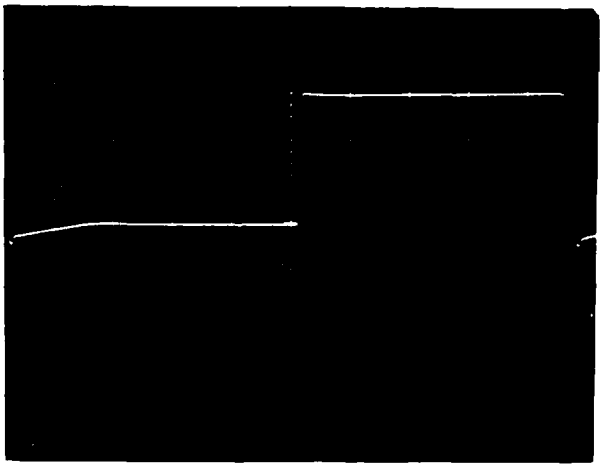
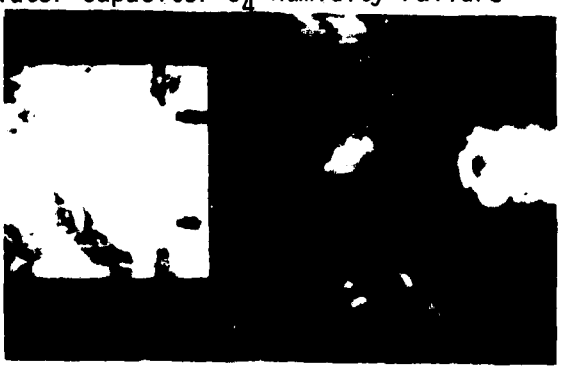


Figure 9. Output Waveform for Oscillator (Vertical 5v/div, Horizontal 10μs/div)

Figure 10. Oscillator Capacitor $C_4$ Humidity Failure

Figure 11. Oscillator Capacitor $C_4$ Humidity Failure



Failure 12. Oscillator Microcircuit Humidity Bond Failure

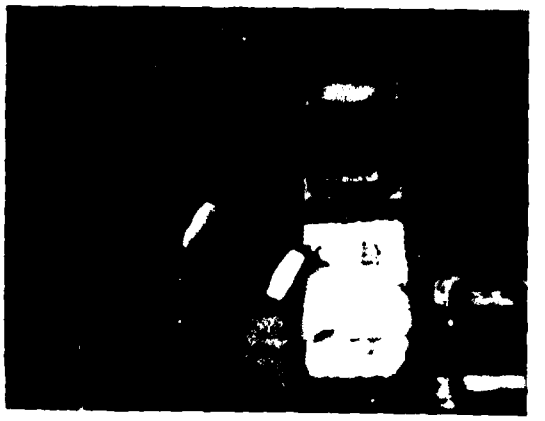


Figure 13. Oscillator Capacitor $C_3$ Thermal Shock Failure

Figure 14. Interface Open Jumper Wire (Humidity Failure)

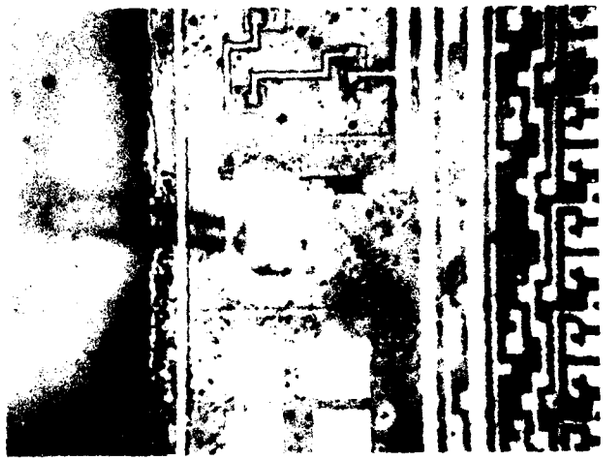
Figure 15. Interface Humidity Chip Wire Bond Failure

(A)

(B)

(C)

Figure 16. Typical Interface Wire Bonds



(A)

(B)

Figure 17. Memory/Timer Humidity Corrosion Failure

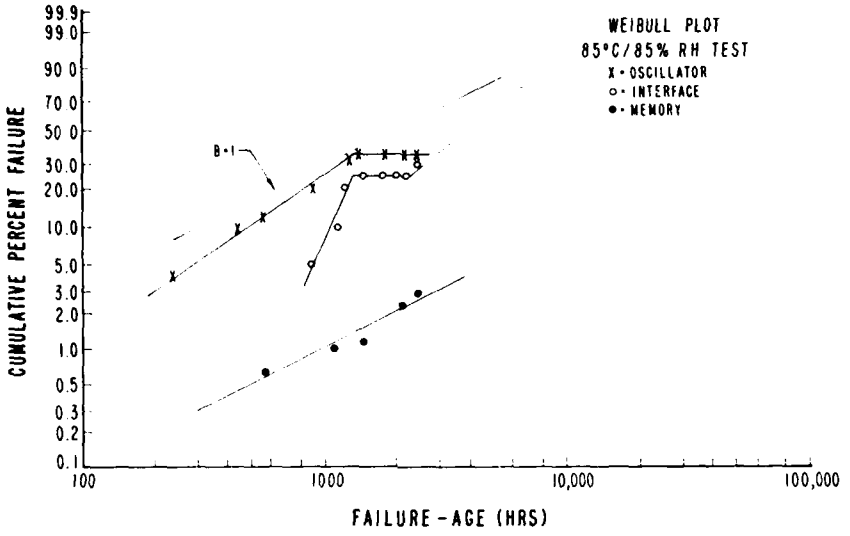



Figure 18. Weibull Humidity Probability Plot

# MICNS HIGH DENSITY PACKAGING USING LEADLESS CHIP CARRIERS, HEAT PIPES AND POLYIMIDE BOARDS

by

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## ABSTRACT

This paper presents details on an IR&D Program resulting in potential improvements in cost, performance, packaging density and weight over flat pack and current leaded chip carrier assembly methods. The benefits are obvious in severe airborne environments as seen by weapons and RPV's as exemplified by Harris' Air Force Precision Location Strike System (PLSS) and the ERADCOM Program on Modular Integrated Communication Navigation System (MICNS).

To meet the Government's challenging requirements, the Aerospace/Avionic Electronics field requires continuous study of new packaging areas. One such area is the ceramic leadless chip carrier which, due to its size and configuration, has become a most effective way to package LSI chips and hybrid circuits. The advantages include significant reduction in printed wiring board area, better electrical performance based on shorter conductors between devices and low assembly costs.

The most common method for mounting chip carriers is to reflow them on a ceramic substrate (co-fire or thick film system) containing a dual-in-line type lead frame, resulting in a leaded carrier package. The substrate is then plugged in and flow or wave soldered to an epoxy glass printed wiring board. Although this method is highly reliable, the high cost of, and the lead time required to obtain the ceramic substrate devices makes it somewhat impractical to design around this method where schedule and cost are primary factors in a program.

A heat dissipation problem results in using leadless chip carriers with more power dissipated in a significantly smaller area. One proposed solution to this problem is the utilization of heat pipes.

Thermal cycling test results (100 cycles -54° C to +125° C) show promise that the leadless chip carrier can be mounted directly on a polyimide type printed wiring board. The IR&D design combines this packaging concept with a flat plate heat pipe.

Another approach is to mount the leadless chip carriers in a larger ceramic substrate containing a high density substrate/motherboard interface connector thus eliminating the glass epoxy daughterboard.

Potential applications for these packaging designs include modems, RF circuits, and any design where high speed, high power and high density are required.

## INTRODUCTION

Ceramic leadless chip carrier (LCC) because of its size and configuration has become the most effective way to package LSI chips and hybrid circuits.

It offers:

- A very efficient use of real estate on the printed wiring board. It occupies about 1/5 the area of a flat pack and 1/9 the area of a dual-in-line package.
- Better electrical performance because of shorter conductors between devices.
- High reliability due to its insensitivity to harsh environments such as high and low temperatures.
- Low assembly costs.

Some of the advantages offered by the leadless chip carrier are lost or restricted because of the interconnect methods used to form functional circuits. In addition, the higher packaging densities realized with LCC's result in higher power dissipated in a smaller area.

Several packaging methods are in use or are being considered to package LCC's by the electronics industry. Among them are:

1. LCC reflow soldered to ceramic substrate (co-fired or thick film systems) containing dual-in-line lead frame. The substrate is plugged in and flow or wave soldered to an epoxy printed wiring board (pwb). The pwb then is plugged into a motherboard (MB) or back panel (LCC/substrate/pwb/MB interface). This packaging approach was used by Harris as early as 1974 and has become the most commonly used packaging method for LCC.
2. Reflow the LCC to glass epoxy pwb. This packaging approach is being used on experimental basis by electronic companies. Its reliability is considered questionable because of the difference in coefficient of linear expansion between the LCC and pwb materials.

3. Porcelain coated steel substrates. A considerable number of companies are investigating the steel core fabricating techniques. Its low cost and ruggedness make it very attractive for high volume consumer products. Its weight, low density packaging as well as its poor electrical performance in certain types of circuits will keep it from airborne equipment applications.

4. Triazine PWB. Initial tests look promising but more tests are needed to establish long term reliability. This material is processed similar to a glass epoxy pwb, but higher temperature and pressure during the laminating process are required. Its availability is limited to one manufacturer in the states and one in Japan.

The study objectives were guided toward the establishment of a low cost, reliable, high density LCC packaging approach capable of surviving the harsh environments imposed by airborne equipment. Two packaging approaches were identified that will meet the study objectives:

- LCC's mounted directly on a polyimide board. The polyimide board was selected based on lower coefficient of thermal expansion, low dielectric constant and material stability in high temperature applications, resulting in longer thermal cycling life and better performance in high speed circuit applications.

- LCC's mounted on a large ceramic substrate containing a high density input/output connector (instead of lead frame). This approach, because the high dielectric constant of the ceramic, is suitable for RF circuit applications.

## Test Samples

A 4.5 inch x 4.78 inch, 8 layer polyimide board was designed to accept seven 48 lead chip carriers (see Figure 1). This size was selected to make the board compatible with the MICNS Program. The design provided a circuit in series with the chip carriers' internal connections to monitor solder joint failures during environmental testing.

Three multilayer polyimide boards were assembled as follows.

a. The first assembly contained seven chip carriers.

b. The second one contained seven chip carriers, a transitron connector and a stiffener across the board for rigidity.

c. The third assembly contained seven chip carriers and a 90 pin AMP minibox connector. This assembly is part of the heat pipe/polyimide board assembly.

d. The fourth sample consisted of a ceramic board 3.84 inches x 4.63 inches x 0.055 inch thick as fired ceramic substrate with 30-48 lead chip carriers and contacts pattern for a 90 pin amp minibox connector screened to one surface.

Three of the chip carriers on assemblies A and B above were wire bonded internally to complete a monitoring circuit used during the testing.

The flat plate heat pipe was designed to fit into the MICNS pwb envelope. Figures 2 and 3 present the heat pipe/polyimide board assembly and heat pipe, respectively. The heat pipe/polyimide board assembly consisted of the heat pipe, heat pipe mounting foot, a resistor board mounted on one side of the heat pipe, and a polyimide board containing chip carriers and a 90 pin AMP minibox connector on the opposite side of the heat pipe board. The resistor board consisted of a polyimide board with 20-2 watt resistors bonded to one side of the board. This board was used as the heat source for the heat pipe temperature test.

## Test Plans and Results

Testing consisted of thermal cycling on a polyimide board to verify solder joint integrity and environmental testing on the heat pipe/polyimide board assembly and ceramic board to verify structural and thermal integrity.

### Thermal Cycling

Two multilayer polyimide boards (Test Samples A and B above) were subjected to a temperature cycling test per MIL-STD-883, Test Condition B. The samples were cycled from -54° C to +125° C for 200 cycles. The test samples' solder joints were thoroughly inspected using a 30x magnification. Solder joint characteristics such as existing defects, solder brightness and any differences between solder joints were noted and identified in a picture or drawing. Solder joint discontinuity was determined by connecting the card to output lines to a resistance bridge and an interrupt circuit that would detect a 100 ns open in the circuit and latch. It would then set off a buzzer which would remain on until shut off thus alerting the operator of a broken solder joint. Test Sample A showed solder joint failures (i.e., discontinuity) at 62 cycles. Test Sample B started to show cracks in the corner of one of the chip carriers after 50 cycles but the test was continued to 200 cycles without catastrophic failure (i.e., the circuit had electrical continuity).

### Environmental Testing

The heat pipe/polyimide board assembly was subjected to temperature, vibration, and shock tests representative of expected responses in airborne applications. The ceramic board was subjected to the same vibration and shock testing to verify structural integrity. The test sequence is presented below:

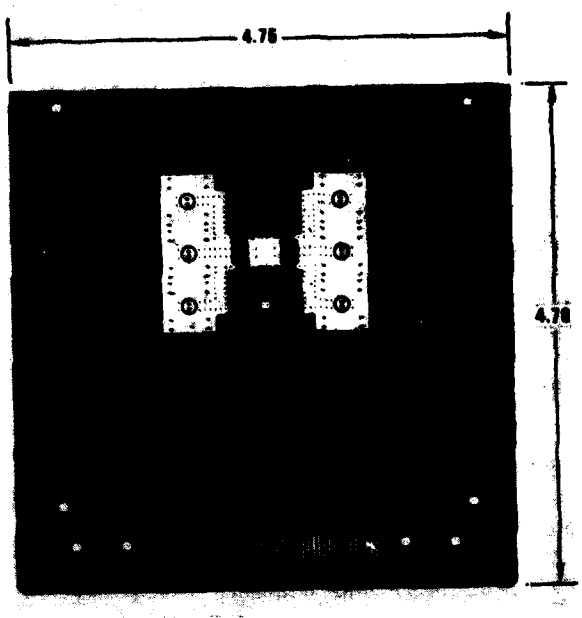


Figure 1. Polyimide LCC Board

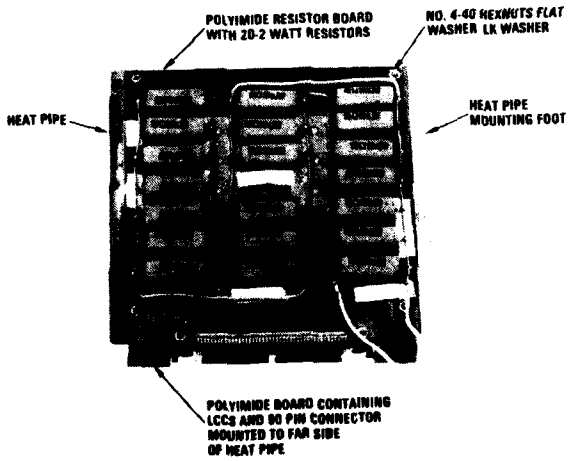


Figure 2. Heat Pipe/Polyimide *Board Assembly*

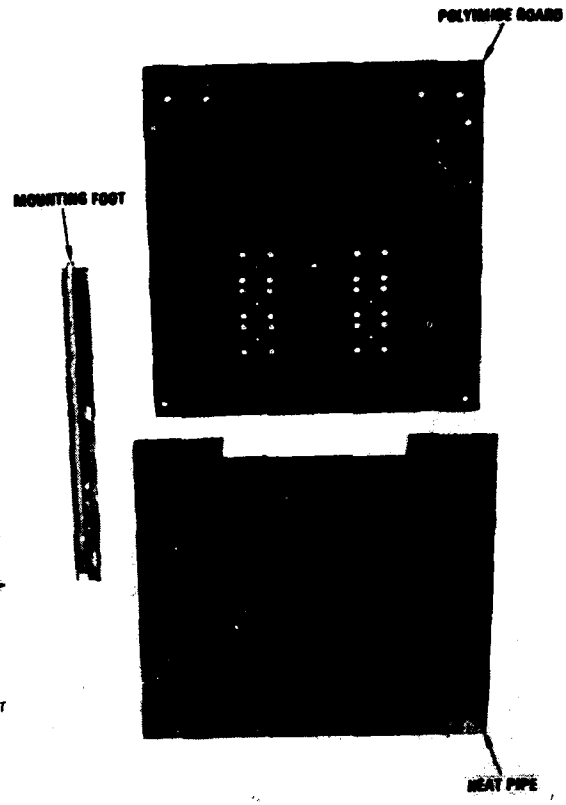


Figure 3. Heat Pipe With Mounting *Foot and Polyimide Board*

1. Electrical test to verify LCC continuity was performed before and after each of the following tests.

2. High (80° C) and low (-15° C) temperature tests to verify heat pipe performance.

3. Vibration test (sine and random) to verify assembly performance.

4. Shock test to verify assembly performance.

5. Repeat high temperature test to check for heat pipe assembly degradation from Tests 2 through 4 above.

Temperature

For the temperature test, the heat pipe/polyimide board assembly was mounted to a cold plate via the mounting foot with the mounting foot vertical. This whole assembly was then placed in a temperature chamber. The temperature chamber and cold plate were separately controlled to either 80° C or -15° C. The assembly was completely surrounded by insulation so as to force the 40 watts of evenly distributed heat dissipation through the condenser section (i.e., mounting foot).

Figure 4 presents the heat pipe test and analysis results along with analysis results for a similar design with a 0.1 inch thick copper heat sink substituted for the heat pipe. The heat pipe only varied 2° C along its length for a 40 watt load. Post vibration testing showed only a 1.3° C or 5.9% thermal gradient degradation from shock and vibration.

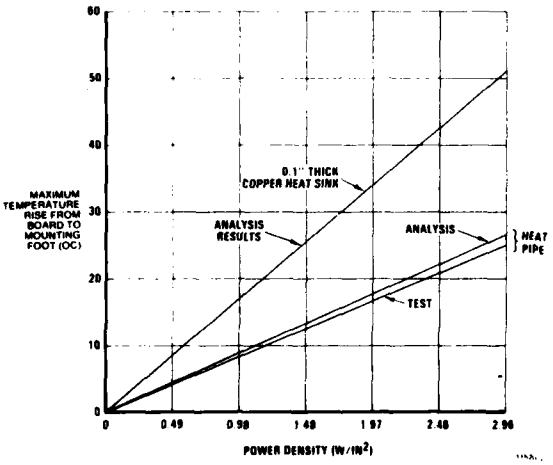


Figure 4. Test and Analysis Comparison

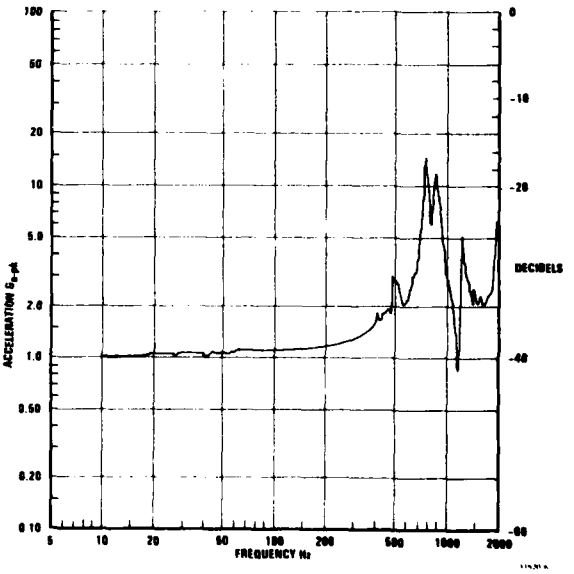


Figure 5. Ceramic Board Response Plot for 1 Gp Sine Input

## Vibration

Sine and random vibration tests were performed on the heat pipe/polyimide board assembly and ceramic board with each mounted in a fixture which was hard mounted to a vibration shaker. The heat pipe/polyimide board assembly mounting interface was completely duplicated, namely - the connector, card guide, thermal foot secured via three #4-40 screws and the end opposite the connector supported by compressed sponge rubber. The ceramic board mounting interface amounted to two card guides, a connector and compressed sponge rubber opposite the connector. Figures 5 and 6 present the heat pipe polyimide board transmissibility plots for the ceramic board and heat pipe assembly, respectively for an input of 1 G peak Sine. Sine and random vibration input levels are presented in Figures 7 and 8, respectively. These levels represent actual application response at the mounting interface. The tests were performed in all three axes with a duration of 1 and 3 hours for sine and random, respectively. Figure 9 presents a comparison of transmissibility for the ceramic board and heat pipe/polyimide board assembly. No failures were observed or measured.

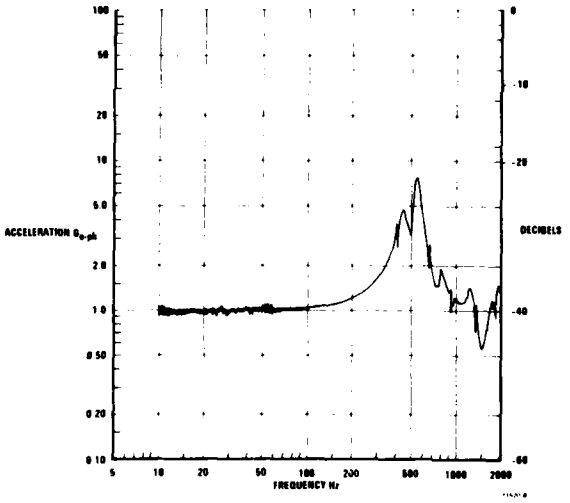

Figure 6. Heat Pipe/Polyimide Assembly Response Plot for 1 Gp Sine Input

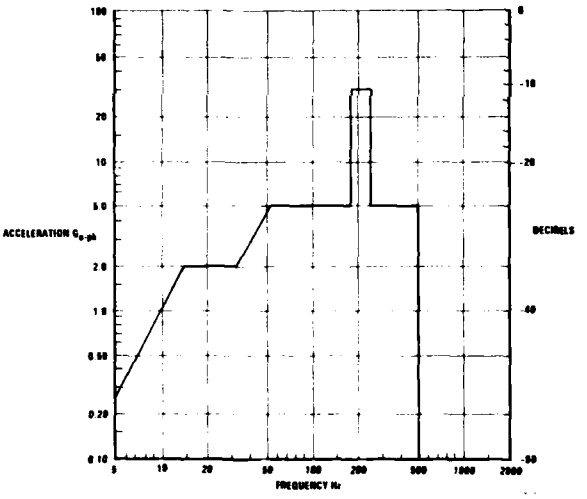

Figure 7. Heat Pipe/Polyimide Assembly Sine Vibration Input

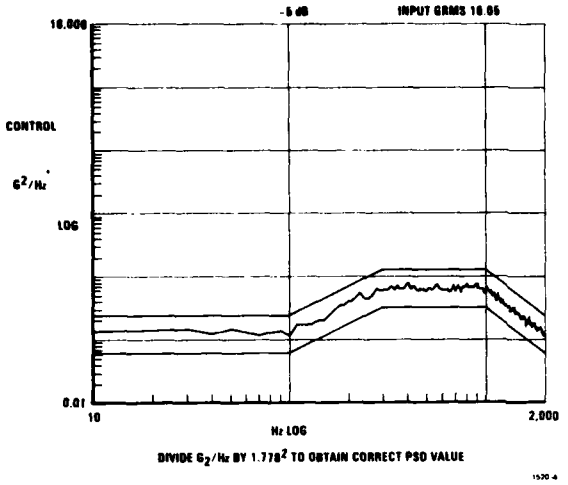


Figure 8. Heat Pipe/Polyimide Assembly Random Vibration Input

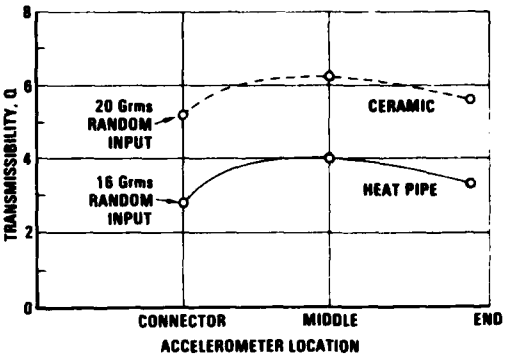


Figure 9. Transmissibility Comparison

## Shock

The heat pipe/polyimide board assembly and ceramic board mounted in their respective fixtures were subjected to shock tests per MIL-STD-810C, Procedure 1, Method 516.2-2, half sine, 15 Gp, 11 ms, three drops per axis, all three axes. No failures were observed or measured.

## Conclusions

The following conclusions were reached as the result of the high density packaging study:

- A ceramic board plugged into a motherboard or back plane can be used to mount LCC's for airborne applications instead of the current method of leaded ceramic module flow soldered to a daughterboard, plugged into the motherboard.
- Polyimide multilayer boards show promise for use in direct mounting of LCC's if properly designed and if the effective coefficient of thermal expansion mismatch is minimized.
- Flat plate heat pipes offer economical solutions to power dissipation problems difficult or impractical to solve by other means.
- The heat pipe/polyimide assembly resulted in significant vibration damping thereby providing lower response levels and longer component life.

# COST AND PERFORMANCE EFFECTIVE HYBRID PACKAGING APPROACH FOR MILITARY AND COMMERCIAL APPLICATIONS

BY

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## ABSTRACT

A ceramic packaging technique is described where electrical interconnections between components are integrated into the package for multilayer hybrid circuit application. The package construction is first explained followed by quality, cost, process and electrical performance benefits. Finally, examples of hybrid products that were realized in both conventional packaging and the method described in this paper are shown for comparison and improvements in performance.

## REVIEW OF EXISTING TECHNIQUES

Among the more popular packaging technologies in use for hybrid integrated circuits are metal platform packages, metal sidewall, metal or ceramic flat pack and ceramic cavity packages. Due mostly to increasing metal (gold and Kovar) cost, the packaging cost using the above techniques is rapidly becoming a higher percentage of the total device cost, especially when integrated circuit (IC) prices are decreasing. Most of the existing packages require a substrate, using gold metal system, especially for high reliability applications. The substrate area is directly proportional to circuit size and complexity since the difficulty factor in going higher than two or three metallization layers is significant with thick film processing techniques resulting in lower yield and increased cost. Further, the packages require two-step mount and multilevel wirebond operations. The proposed packaging technique described in this paper will yield a much improved cost savings, electrical performance and assembly ease for military and commercial applications.

## SLAM PACKAGE DESCRIPTION

The Slam package is a multilayer laminated ceramic package with circuit interconnections and lead connections integrated within the package. As a result, a separate substrate insert with circuit patterns (used in conventional packaging) is not required. Each layer is made from 10-30 mil "tapes", or plates in the green (unfired) ceramic state with metallization patterns of

tungsten or moly-manganese screened on using conventional thick film techniques. Up to nine tape layers are possible. Interconnection between layers is made using punched holes or "vias" through which metal paste is drawn through under vacuum (Fig. 1). All the vias are punched at the same time on the plate using a metal die. In the green state (unfired), the ceramic is flexible, soft and easy to work with. Various layers with patterns are stacked in order, pressed and co-fired at very high temperatures (above 1200°C). The ceramic shrinks about 20% when it is fired and hardening takes place. This presents no alignment problem however, since all the layers shrink at the same rate.

The Slam package can also be constructed using screened ceramic dielectric (instead of tapes) up to six levels. This can also be combined with tape construction, with the screened layers on the uppermost tape for process compatibility reasons.

Leads are attached using conventional side braze techniques using silver-copper alloy as braze material. More circuit area can be gained with fixed pin spacing if the pins are bottom brazed such that the package width is much larger than the pin row spacing. After the package has been fired and pins are attached, the package is electroplated with nickel and gold on the pins and on areas on the top layer where conductors and pads have been left exposed with no dielectric.

The lid is made of the same ceramic material and is generally punched into the shape of a sidewall cap deep enough for components and bond wires.

## SLAM PACKAGE ADVANTAGES

The benefits derived from this package technique is discussed in four categories: 1) mechanical and processing, 2) quality and reliability, 3) cost and 4) electrical performance.

## MECHANICAL AND PROCESSING

Fewer assembly processing steps are needed since there is no substrate insert. Thus, substrate attach, cure, and visual inspection are eliminated. Since the connection to the pins is integrated into the package, the number of bond wires is reduced by the number of leads. In addition, the different bond levels in the hybrid is reduced from three to two. (Only chip and package levels are needed. The post or pin level is eliminated). This facilitates automation in wirebonding, where multi-levels and/or bond level range is limited. Chip carriers can also be used in this package or mixed with chip and wire assembly techniques. Although much work has been done to improve thick film gold bondability, it is our experience that significant problems still exist such as weak bond strength and integrity, gold thickness, open circuits, bridging, poor reliability and life test failures. These problems tend to be lot dependent on thick film processes and systems. In the ceramic package metallization, the wire bonding is very consistent and less sensitive to bond settings and operating condition. This is some-

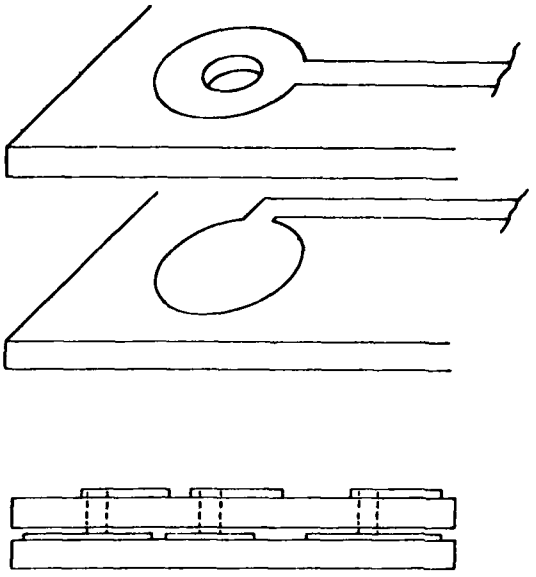

Figure 1. Interconnections between tape layers.

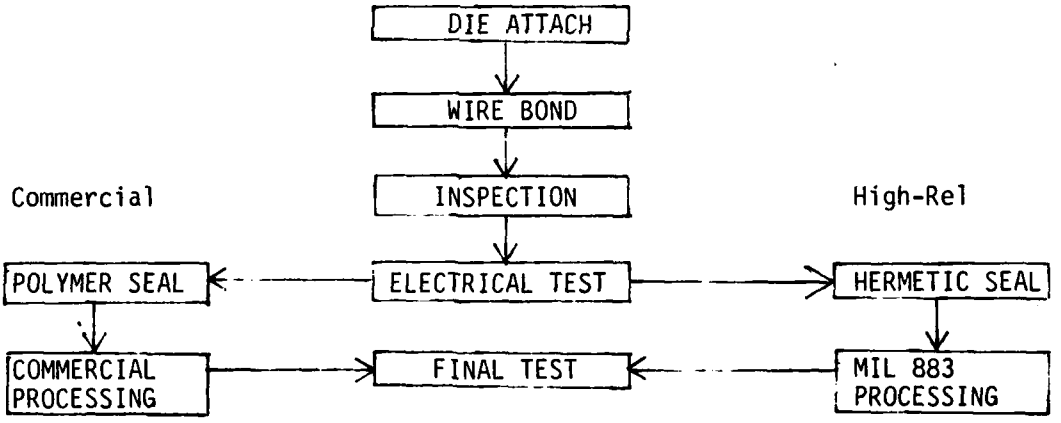


Figure 2. Assembly Flow Diagram

what attributed to excellent adhesion of tungsten conductor to alumina and controlled gold plating processes.

Because there is no cavity, the Slam package can be epoxy screened for die attach. IC dice can be eutectically mounted as well. Package designs can be constrained to side-brazed pin types by increasing the number of layers. This facilitates automation in that the package outlines fits standard IC holding chucks for assembly and handlers for testing. Devices can be loaded into tubes for automatic loading and unloading.

Polymer or solder reflow sealing of these packages is a batch process rather than individual manual operation given to each package as in brazing and welding of metal packages. The overall result is that there is a higher throughput rate for assembly processing using the ceramic package.

The flow diagram (in figure 2 ) shows similarity in hybrid assembly processes. It should be noted that most of the assembly processes are identical prior to sealing of the devices for both commercial and high reliability applications. Special processing and environmental screening of hybrids are done depending upon the end product specifications.

## QUALITY AND RELIABILITY

With fewer bond wires (due to package lead interconnections) there is lower probability of a bond failure. As stated above, bond integrity is much better than thick film gold, with consistently higher pull strength and narrow distribution about the mean due to tightly controlled metallization/ plating processes. There is virtually no chance of shorting of conductors with 10-30 mil tape separation between layers rather than the 2 mils of thick film dielectric that is prone to pin holes. If there were an open circuit it would be easily observed in color differences between the gold and the tungsten in non-plated areas.

The package construction outlined above is of the same process as standard monolithic sidebraze packages that are widely accepted by industry and military specifications. Package qualification by similarity is therefore possible. Hermeticity is inherent to the package since most of the conductors are buried deep inside the ceramic and leads are attached by braze techniques. Metal packages also suffer from potential leaks at the glass to metal interfaces around each post. Since the ceramic package is compact in outline and less weight compared to metal packages, it can withstand higher level of environmental stresses such as centrifuge and mechanical shock, etc. The Slam package technique is also less sensitive to higher process temperatures (eutectic attach, reflow sealing). Elimination of the substrate and associated interface to the package results in better thermal conductivity from chip junction to ambient environment. Thus, IC junction temperatures are lower and hence, reliability is improved.

## COST

Being an advantage in every other respect, the elimination of a substrate is also a cost advantage as there is one less component in the device. The substrate savings becomes more significant when the amount of gold reduction is considered. The package is electroplated with gold after the dielectric is in place, exposing only the minimum area of die attach and bond pad areas. The metallization on thick film substrates is gold on all layers regardless of dielectric covering. Cost is usually proportional to package size since the area defines the number of units per plate. The Slam package can reduce the size by using more layers at an incremental cost with smaller area for each layer. The elimination of many processing steps, such as substrate attach and visual inspection, fewer bond wires, and an increase in the throughput rate results in lower manufacturing costs.

## ELECTRICAL ADVANTAGES

With direct connection to the pins there is lower series resistance especially important on device outputs, input power supplies, and ground connections where transient currents can cause voltage errors. The Slam package can minimize this problem using Kelvin connections with the force line contacting the pin on one layer and the sense line on another (the bottom layer for best results to sense as close to the external circuit as possible). Similarly ground returns can be split on different layers to reduce current modulation effects. Many precision circuits that normally would require separate force and sense pins and several ground pins have been designed with fewer pins in smaller package outlines. Crosstalk and noise are minimized by partitioning the circuit (for example, analog and digital functions) into different layers separated by up to 30 mils rather than the typical 2 mil separation created by thick film dielectric isolation. Individual layers also greatly improve dynamic performance since capacitance from one layer metallization to that of the next layer is inversely proportional to separation. Dynamic performance is further improved by the negligible dielectric absorption of the ceramic. Low noise circuits can be designed by isolating sensitive areas on separate layers away from other noise sources within the device.

From the elimination of post bonds, and the improvement in bond integrity stated above, there is less bond resistance change with stresses from processing and environmental conditions. In some circuits even very small series resistance can be significant if large constant currents are flowing, which appears as an error or offset voltage. This error cannot be compensated, by an active trim for example, if the resistance changes. The Slam package makes device accuracy much less sensitive to any bond resistance changes.

The improvement in thermal conductivity from the absence of a substrate and interface as pointed out previously for better reliability, is also an advantage for electrical reasons. There is less effect from self heating that often limits settling time by long thermal tails. Accuracy is not as

much affected by output load current. Higher operating temperature range can be achieved with lower junction temperatures. It is usually the high temperatures that limit accuracy in as much as drift errors increase much more rapidly, at least for bipolar integrated circuits.

## DISADVANTAGES

There are some trade-offs to be made using Slam package techniques, but they are few and minor. Each package needs separate tooling and this cost is higher than the cost for thick film substrates and screens. Another drawback is longer lead time than thick film fabrication. Multi-level packages are more difficult to design, check out and hence, are prone to errors. However, these errors can be minimized with experience, and/or using computer automated design. Another limitation is that deposition of thick film resistors on the metal system is not possible due to process difficulties.

## EXAMPLES

Several products were designed in both a conventional hybrid assembly (either thin film substrate on metal platform or thick film substrate on ceramic cavity package) and the Slam package. In each case there was a performance increase and size reduction in the Slam package.

## A/D CONVERTERS

A 12 bit analog to digital converter required a .900" wide conventional packaging with two layers to meet the performance and isolation requirements. The same design was implemented in a Slam package having the same number of layers with reduced width to .600". (Figure 3 ). The device speed improved from 4 to 3us with negligible crosstalk between digital and analog sections. Figure 4 shows similar comparison between conventional and slam package design. It should be noted that the commercial and hermetic packages differ only by the addition of a seal ring on the top metallization.

## AMPLIFIERS

Figures 5 & 6 show the comparison of high gain amplifiers in thick film and slam package version. A tenfold improvement in the dynamic response from 400 to 40 us settling time achieved by translating same layout pattern. This is due to low capacitance effects of the package.

## PRECISION VOLTAGE REFERENCE

Using Kelvin sensing and proper ground schemes on different layers, a low TC reference (Figure 7 ) was achieved in Slam with the following specifications:

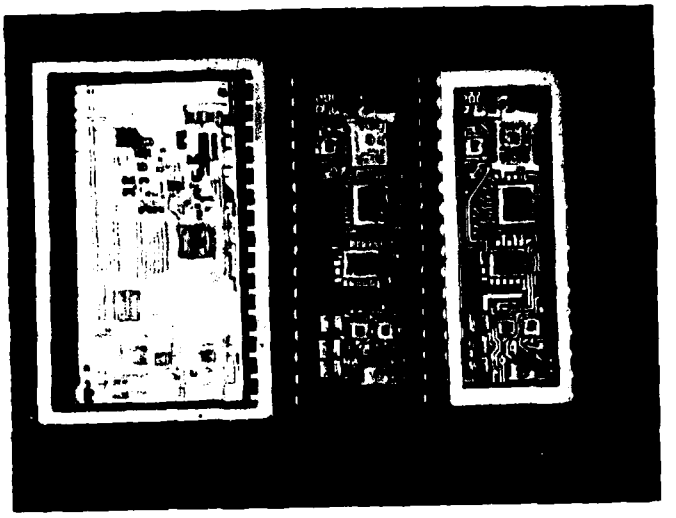

Figure 3. High speed analog to digital converter.

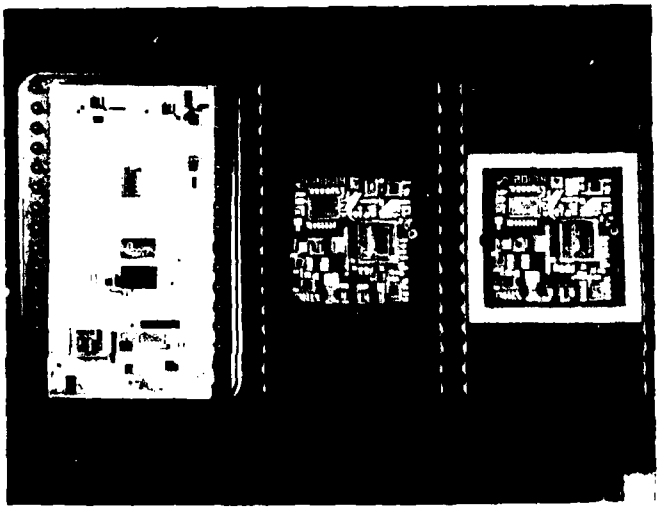

Figure 4. Medium speed converter.

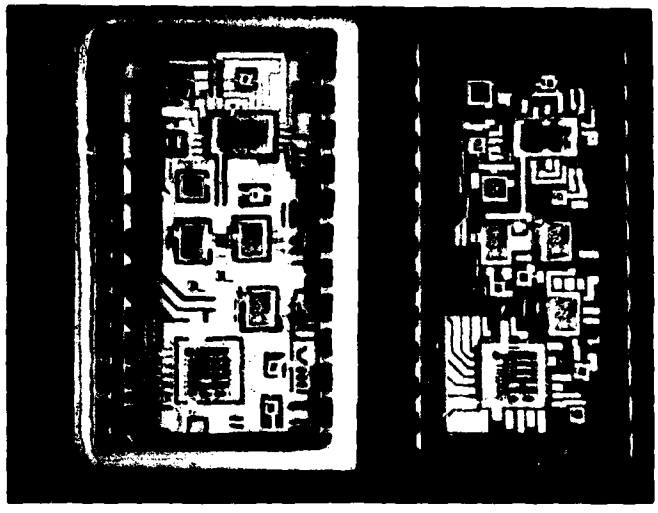

Figure 5. High gain instrumentation amplifier

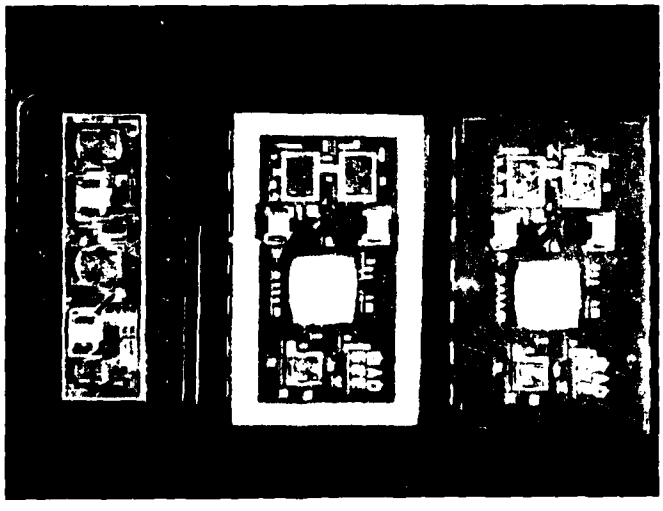

Figure 6. Instrumentation amplifier

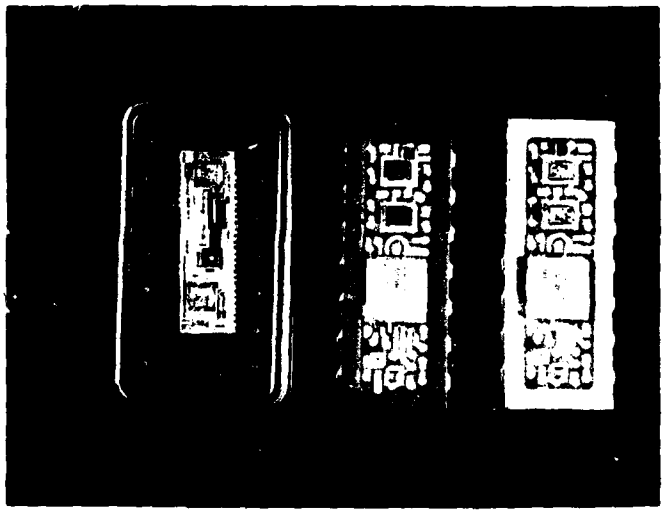

Figure 7. Precision voltage reference.

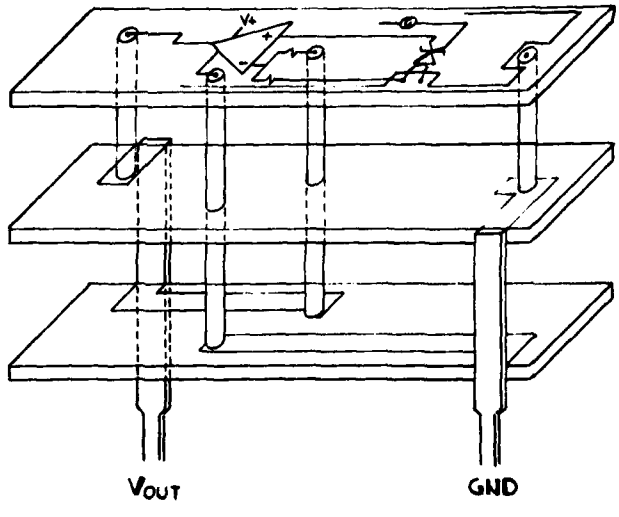


Figure 8. Exploded view of slam package reference device.

| | |
|---|---|
| Error from nominal value (25°C) | 1mV |
| Temperature coefficient (0-70°C) | 1ppm/°C |
| PSRR | 80db |
| Load regulation | 50uV/mA |

An exploded view of the critical conductors in the three level package are shown in figure 8.

## CONCLUSION

It has been shown that using the Slam technique, hybrid microcircuit performance and reliability are improved by careful package layout design with lower cost and less manufacturing requirements. The ability to design hybrid devices in three dimensions provides much more flexibility in the choice of pin-outs, outline and circuit complexity. The reliability of the units are improved due to less weight, better thermal gradient, ability to withstand higher environmental stress levels and fewer wire bonds.

## ACKNOWLEDGMENTS

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# REDUCING THE COST OF HYBRID MANUFACTURING THROUGH INNOVATIVE OPERATOR TRAINING

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## Abstract

Operator training is a subject that has long been neglected by many hybrid manufacturers. However, inadequate training is the major cause of defective work in most assembly operations. Obviously, reduction in the amount of defective work will lead to increased yield and greater throughput, resulting in cost savings. An effective means of operator training which can be used in almost any manufacturing environment is presented in this paper. This method utilizes a combination of audio-visual techniques and active trainee involvement, providing a self-paced performance based training program which in itself is more cost-effective than conventional training methods. In addition, the more thorough training provided by the new techniques as well as the availability of the programs for future operator reference, produce improved assembly yields and throughput.

## Introduction

Once designs are finalized and the manufacturing cycle begins, an often overlooked but extremely important aspect to keeping the production line running smoothly is operator training. Whether the manufacturing process is simple or complex, the manufacturing operators need to be trained in performing their tasks. This training must be done in the least expensive manner which will assure an adequate skill level. Depending on the size of the production area and the complexity of the tasks to be performed, this operator training may take various forms. For a small number of operators with relatively simple tasks, training may consist simply of verbal instructions given by a supervisor or other operator, followed by a few minutes of

*Mr. Leven was formerly with Westinghouse Defense & Electronic Systems Center, where the work described herein was performed.

practice. In large production operations with complex tasks, training may consist of a rigorous schooling complete with audio-visual aids, training instructors, and testing for certification. In between these two extremes lies the vast majority of production lines for which it is not apparent that a formal training program would be cost effective.

This paper discusses how we prepared and utilized a series of audio-visual training programs for operators in one such production area - the Westinghouse Hybrid Microwave Module Assembly Area, in which custom hybrid microelectronic modules are produced in medium volume for military radar and communications systems. The methods and techniques discussed yielded a 30% reduction in training time and can be applied in any manufacturing environment.

A hybrid microwave module, as differentiated from an integrated circuit chip and wire hybrid, utilizes packaged, hermetically sealed transistors and integrated circuits and other devices which are soldered to thick film ceramic substrates. These substrates are assembled into a module, which is then sealed using a gasket covered lid. These modules range in size from 1 x 2 inches to 12 x 18 inches, and due to the relatively small quantities, are assembled using hand soldering techniques. Figure 1 shows a typical Westinghouse hybrid microwave module.

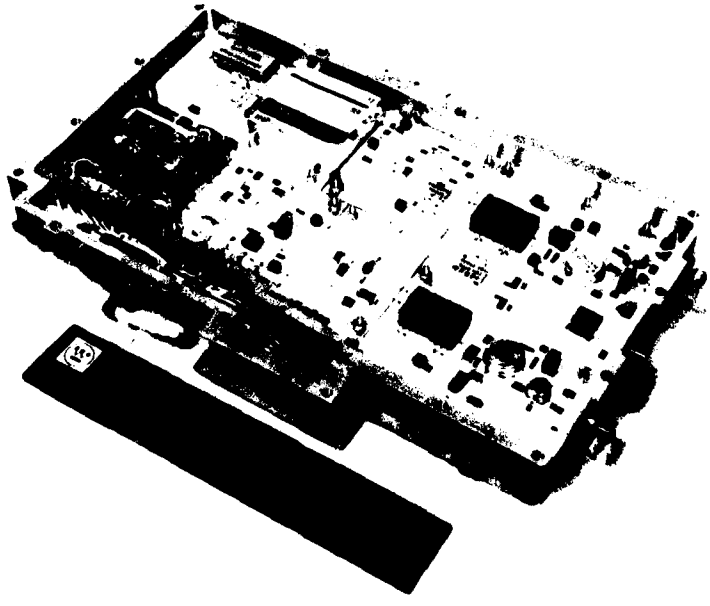

Figure 1. A typical Westinghouse Hybrid Microwave Module

The operations required to correctly assemble these modules are very delicate and require a high degree of training. Since the work is done in a clean room environment, the operations involved include cleanliness and proper handling of parts. Specific operations include component preparation and lead bending, soldering of various shapes and styles of leads and parts to both ceramic and printed circuit substrates, soldering of substrates to carriers, and attaching substrates to housings with adhesive. Lidding and delidding procedures as well as requirements for adhesive supports must also be learned. In addition, mechanical assembly operations, thorough cleaning, documentation, and repair and rework procedures are all tasks which must be performed by all hybrid operators.

## Reasons for Emphasis on Training

Obviously, operators in our Hybrid Microwave Module Area need to be trained. But the subject of operator training received critical attention due to the following reasons:

- o High Product Cost. By the time a module is completed, it represents a large investment in component parts and labor. Any mistakes during assembly will jeopardize the unit's performance or reliability, causing expensive rework or scrappage.
- o Wide Range of Operator-Dependent Skills. Due to the complexity of the hybrid assemblies, each operator must be able to perform a large number of very complex skills. The successful assembly of a module requires a high degree of dexterity by these operators, with most of the operations being performed under a microscope, resulting in a highly operator-dependent process.
- o Low Volume and Long Assembly Time. The relatively low production rates and length of time required for assembly result in operators going back to operations after an absence of weeks or even months. This results in the need for retraining after the initial training and certification.
- o Operator Turnover. Even though the hybrid workforce is relatively small, advancement policies and mobility requirements based on union-management contractual agreements mean that new operators are constantly coming into the area. Additionally, reductions in workforce, sometimes in other areas of the plant, cause operators who have not worked in hybrids for some time to re-enter the area. These operators require retraining.
- o Need for Consistency. Due to the highly technical nature of the tasks to be performed, training needs to be consistent from operator to operator. This consistency is also preferred by our employee unions, so that adequate training will be available for all operators.

For a number of years operator training in the hybrid area consisted of one insructor who personally trained small groups of operators in the

basic hybrid procedures during a two week training course. In addition to training the Microwave Module operators, she also trained all the other hybrid operators, including those involved in chip mounting, wire bonding, cleaning, and packaging. Working from her own notes, the instructor usually taught about 40% of the microwave module operations during the 2-week course. The rest of the tasks were learned from the more experienced operators.

Due to the fact that the instructor was very competent, our former hybrid training methods were well intentioned and provided an acceptable means of training for a period of time. However, the training was inconsistent since the instructor relied on her own notes and memory. It was not comprehensive, nor was it rigorously reviewed by supervisors, Quality Control engineers, or Process engineers. The training was not geared to operators' individual learning rates because trainees progressed as a class. This class structure also restricted instructor efficiency since only one subject at a time could be taught.

## Audio-Visual Approach

Last year, Westinghouse developed a new training program for the Hybrid Microwave Module Assembly Area. Our objectives in preparing these new training programs were to provide consistent, comprehensive, self-paced, performance-based training in the most cost effective manner. After an extensive search, the audio visual training medium that we found to be the most effective was the Sound-on-Slide* delivery system manufactured by 3M Corporation. This equipment permitted us to create training programs at Westinghouse which would be of modular construction and allow completely self-paced individualized instruction. The system offers simplicity of program preparation and update, and equipment operation, making it ideal for use in a factory environment.

## Synchronization Problems Eliminated

The key feature of the Sound-on-Slide delivery system is the enlarged plastic slide frame. Figure 2 shows how a standard 2 inch x 2 inch 35 mm slide is physically clipped to the plastic frame which contains a rotating magnetic recording disk. These frames are then inserted in either straight 36-frame trays or circular 40-frame trays. Separation of the sound from the visual, or loss of synchronization, is not possible unless the 35 mm slide is intentionally removed from the frame. The equipment available to make use of this feature is shown in Figure 3, and includes a projector which operates similarly to a standard 35 mm slide projector.

*R Sound-on-Slide is a registered Trade Mark of 3M Corporation.

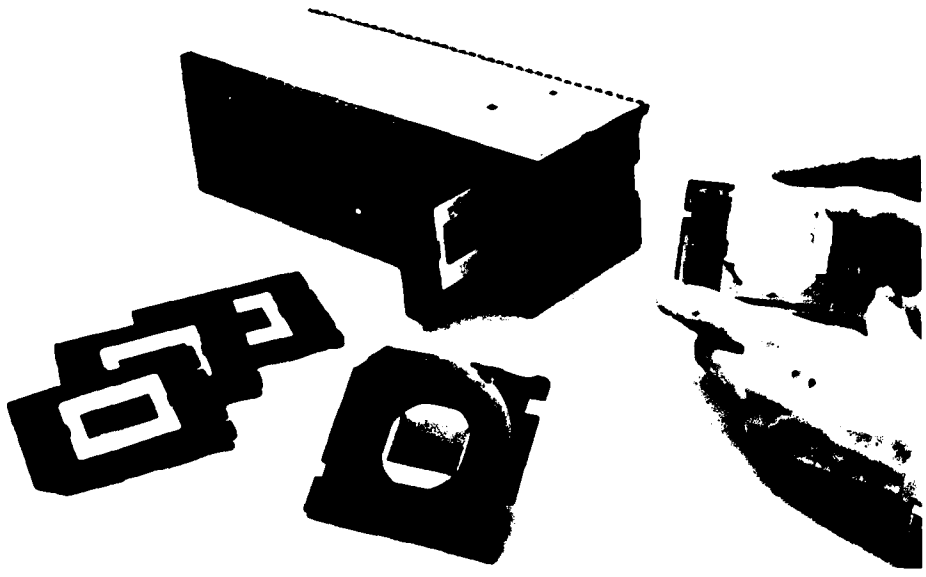

Figure 2. The Sound-on-Slide delivery system features a 35 mm slide which is physically clipped to a plastic frame containing a rotating magnetic recording disk.

Figure 3. Sound-on-Slide equipment includes the projector, a detachable rear screen, headphones, and a Responder for interacting with the training program.

The advantages of the Sound-on-Slide delivery system over conventional audio-visual systems are as follows:

- o Synchronization between audio and visuals cannot be lost.
- o Visuals are standard 35 mm slides.
- o Recording of the verbal instructions is as easy as speaking into a microphone, and can be accomplished one frame at a time directly onto the slide frames, eliminating complex editing, timing, and re-recording. See Figure 4.
- o Revisions, corrections, changes in the order of procedures, or excerpting portions of programs for other uses are all simple to accomplish. Only the affected frames need be re-recorded or have visuals changed. No matter how long or short the revisions are, the synchronization of the remainder of the program is completely unaffected.
- o Portable equipment can easily be set up at the operators' work station for individualized training, or used classroom style for a group presentation.
- o Operator involvement stems from the ability of the equipment to advance slides automatically while a set of instructions is given, and then to wait until the operator completes some work or activity before continuing the program. In addition, the Forward, Reverse, and Instant Replay controls allow the operator to travel back and forth through the program at will to be sure of understanding the material.

Figure 4. Visuals are prepared using a standard 35mm camera.

- o Responder allows the asking of mulitple choice questions of the trainee. Only if the correct answer button is pressed will the program continue. This is another feature which keeps the operators actively involved in the learning process, as opposed to simply watching a film or video-tape.

These advantages convinced us that the Sound-on-Slide equipment was the best equipment available to help us meet our training goals in the Hybrid Microwave Module Assembly Area.

## Training Techniques and Psychology

In performance-based, task oriented, self-paced, individualized skills training, the training psychology and methods are just as important as the technical content. Westinghouse used a series of training techniques designed to put the trainee at ease and have her become actively involved in the learning process. The first step in relaxing the operators was the use of a non-professional narrator. The person chosen to narrate the programs was the hybrid area instructor, who spoke the script in her own dialect. A professional narrator would have been too unfamiliar with the material to do an effective job.

At the outset of each training program the trainee is told the objectives of the lesson, as well as how the lesson relates to the importance of her job and the other lessons of the series. Then the trainee is both shown and told what tools, equipment, and supplies she needs to obtain before proceeding with the lesson. The program stops at this point and waits until the trainee has gathered all the necessary items.

Each frame of instruction gives the trainee some new information or tells her to do something specific. The program always stops and waits for the trainee to perform the required actions before going on to the next step. Operations which must be performed in a time sequence are broken into blocks of instruction which may be several frames long. The trainee is encouraged to review the steps several times before attempting the actions on her own. And most important, the trainee is never addressed in a condescending manner. The program always assumes the trainee will be able to easily master the technique with proper instruction and sufficient practice. Accordingly, words of encouragement are used throughout.

In skills training, showing the trainee how to do something, and letting her practice are not enough. The trainee must be given all the evaluation criteria which will be used to judge her work. In this way, she can determine when she has mastered one technique and is ready to go on to the next. This method is true self-paced instruction. Of course, the instructor is always present during training for consultation.

Multiple choice questions are used in the training programs to help the trainee learn the technical requirements and evaluation criteria. Generally, these questions offer the trainee some information, and then solicit some additional related information. The questions, which are answered by use of the Responder, help reinforce process requirements which may not show up in the trainee's finished sample work, such as hot plate temperatures, etc. In all cases, the answers to the questions are explained fully in the following frame, as an added means of reinforcement.

These techniques, when incorporated into the training programs, make the trainee an active part of the learning process, rather than a passive observer. This active participation is one of the best ways to teach such detailed skills using audio-visual techniques.

## Training Program Development

The first step is an analysis of the functions within the area to determine which procedures will be trained. Order of training is also critical because it establishes the prerequisites.

As a result of our task analysis, the operations of the Microwave Module Assembly Area were broken down into two basic groups. The first was "entry level training", which all incoming operators received. These programs included:

- Handling and cleanliness
- Paperwork
- Lead forming by special equipment
- Chip component to substrate soldering
- Round lead component to substrate soldering
- Flat lead component to substrate soldering
- Cleaning
- Application of adhesive to substrates
- Assembly of printed circuit or soft substrates
- Documentation and inspection control tags.

The second group of programs is referred to as "as needed" training. These programs were given to operators as they were required to perform certain additional operations. This group of operations included:

- Substrate to package adhesive mount
- Substrate to carrier soldering
- Module sealing
- Module mechanical assembly
- Adhesive application to modules
- Repair and rework procedures.

The next step in the process is to find dedicated program writers. These may be in-house personnel or outside consultants, and need not have any knowledge of the subject matter to be trained. In our case, Westinghouse hired an outside consultant firm, Northrop Services, Inc., to write the hybrid training programs, since sufficient personnel were not available internally.

Regardless of who is writing the programs, subject matter experts must be identified. We identified subject matter experts from among all the following disciplines:

- Manufacturing Engineering
- Quality Control Engineering
- Operator Supervision
- Industrial Engineering
- Experienced Operators.

The program writers read the existing Westinghouse process specifications so that they would have an understanding of the process. They then observed previously trained operators performing the functions, accompanied by engineers who were able to discuss the important points of the process. The program writers then described the process as they saw it in an outline form which was reviewed for approval by Manufacturing and Quality Control engineers.

Scripting was the next phase of program development. The program script was written, taking into account all of the training psychology and process information. As part of the scripting phase, a storyboard of the training program was prepared, identifying the visuals to be used. The scripts and storyboards were also approved by Manufacturing and Quality Control engineers, as well as by the area supervisors and selected experienced operators.

Once the script and storyboard were approved, preparation of the visuals began. The Microwave Module Training programs, due to the size of the project, required the photographing of about 1200 visuals. This effort required the constant close cooperation of the Photographic Department; the Technical Publications Department, which added graphics to some of the slides; the Assembly area operators and supervisors who were preparing the samples; and, of course, the program writers and subject matter experts. The majority of the visuals were 35 mm color slides with some graphics added where necessary. The photography was done using actual operators, as shown in Figure 5.

Recording of the scripts was done concurrently with the photography. The area instructor recorded most of the programs, one script at a time, with the help of the program writers, directly onto the Sound-on-Slide frames. Usually, the narrator needed to read the script only once prior to recording, since she was completely familiar with the material.

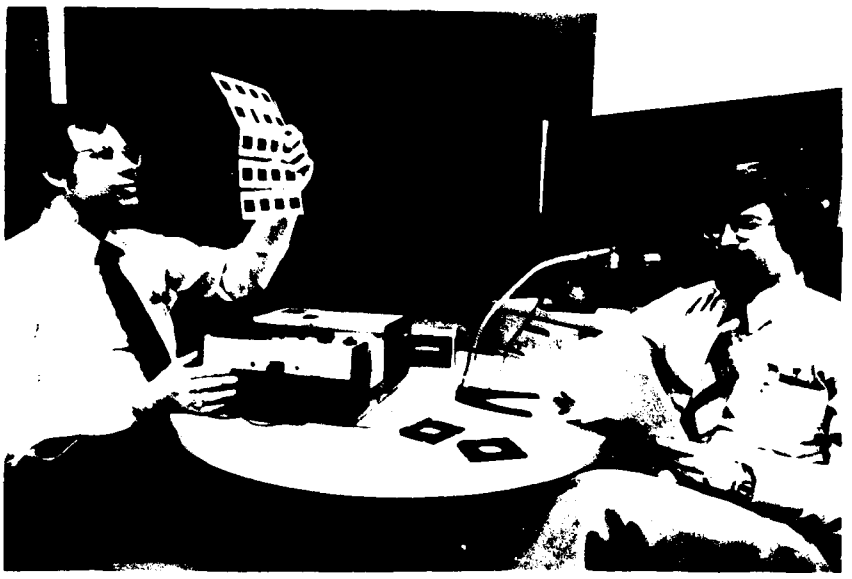

Figure 5. Steve Leven records one of the Microwave Module Assembly Area training programs as Sheldon Schwartz assists by operating the recorder and checking the visuals.

The need for review and approval cycles cannot be over-emphasized. In addition to the approval of the process outlines and scripts, the recorded program was reviewed by a small group of Manufacturing and Quality engineers, area supervisors, program writers, the instructor, and several key operators who were intimately familiar with the process. Any errors or omissions were readily identified and these corrections were then made to the program by addition or correction of some of the script and/or some of the visuals.

The finished program was then reviewed by the same group again, after which it was ready for release to the instructor for actual use.

## Coordination of Training Program Development Effort

It is important to understand that since the creation of these audio visual training programs takes some time from everybody concerned with production in a given area, including the Manufacturing and Quality engineers, area supervisors, instructors, management, and even the operators themselves in preparing samples, continuous support is extremely important. One person must be identified as the final technical authority ultimately responsible for the technical information within the program. In our case

it was one of the Process engineers. In addition, we identified one individual to coordinate the various in-plant services to insure success. These services included Purchasing, photography, graphics, Security, Industrial Relations, Manufacturing, Manufacturing engineering, Quality Control engineering and office services.

## Student Workbooks

After the hybrid programs were developed, a student workbook was assembled to complement the training programs. The material for the workbook was easy to prepare because the information came directly from the program, which was technicaly correct and well organized. The workbook consisted of separate worksheets for each program containing:

- Title
- Objective
- Equipment and Materials
- Process Summary
- Helpful Diagrams.

Although the programs were technically complete, we felt that the trainee still required additional information to help support the learning process. The workbook also contains a section on terminology, actual Westinghouse process specifications for reference, Safety Rules and a copy of those questions that appeared in the program.

The workbook allows the trainees to make their own notes and provides them with an organized set of training material after they leave the training environment and get out into the "real world". The workbook also contains the "nice-to-know" information that might have confused the student during training.

## Program Upkeep

Having spent the time and money necessary to create an advanced audio visual training program, it is imperative that the program be continuously updated to insure that it doesn't quickly become obsolete, especially in a high technology area. Any change in a process must be coordinated through those responsible for maintaining the validity of the training program so that as a process evolves, the required changes will be made in the training program, thus keeping it current.

To insure that our training programs are kept up to date, we established rigorous configuration procedures. The script, and a master set of slides for all programs are stored in a central location. Revision letters are assigned to each program upon release to the functional area. We assembled a list of all process specifications and documents that were

required in preparing each training program. Any changes to these documents are carefully reviewed by the training group, consulting with the appropriate Manufacturing Engineer, for impact on the training program. New slides are made when required, and only the frames to be changed are renarrated. As changes in the programs are made, the program revision level is upgraded. A current listing of program revision levels is published monthly.

Initially there were some concerns that we would be constantly revising the programs; however, to date only approximately 5% of the frames have been changed, with most of these changes due to improvements and clarifications rather than due to changes in Westinghouse process specifications.

## Program Use

After each training program was completed, it was released to the area supervisor so that he could present it to his existing group of operators. This group review, as shown in Figure 6, helped show the operators that the effort they underwent in preparing samples for the program were not wasted. Their review of the program corrected any misconceptions they may have had about some of the operations they were performing, or that they may have been performing incorrectly. This review generated more feedback for the program writers, and frequently indicated that there was still some information lacking or incorrect in the program.

Figure 6. The existing group of operators, led by their supervisor, reviews a Sound-on-Slide training program.

Several copies of the programs were then released to the instructor to use in training new employees. The actual training session consisted of a small group of 5 or 6 new employes with the instructor present. Each trainee was seated at a work station with a microscope and with a Sound-on-Slide equipment set-up, as shown in Figure 7. Each trainee was first instructed on how to use the Sound-on-Slide equipment, and then began with the Basic Operations program. The instructor checked the progress of each student frequently as she progressed on individual programs at her own pace.

After our first set of trainees used the Sound-on-Slide programs we decided to provide the next class of trainees with actual samples of acceptable and rejectable parts that they could compare for themselves under a microscope. Even though the program photography was excellent, actual parts were found to be very helpful to the trainees in confirming the accept-reject criteria in their own minds. These parts helped the operators to judge for themselves whether or not their work would meet the process requirements.

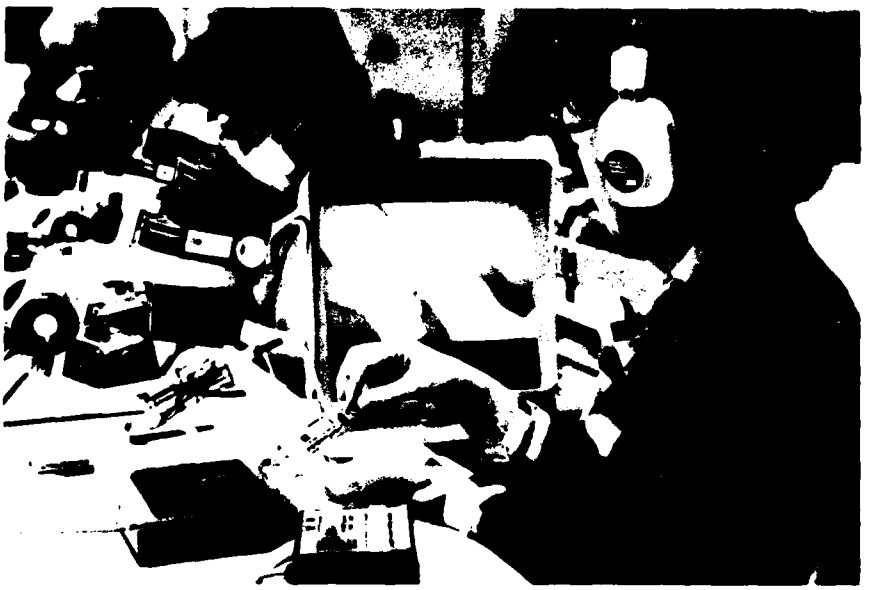

Figure 7. A new trainee learns Microwave Module Assembly techniques at her work station.

## Results

This training method now provides consistent delivery of information from class to class and student to student. The instructor can now also spend more time with those students who have difficulty, while allowing the other students who perform the operations correctly to go on to more advanced work. Typically the training session that lasted two weeks and covered 40% of the assembly operations now is completed in 7 working days covering about 75% of the operations. The first group of operators to achieve certification using Sound-on-Slide training assembled their test substrates with zero defects. The remaining 25% of the operations, which fall into the "as needed" category, are given to the operators, via Sound-on-Slide techniques, when they are going to be working on new processes. Frequently, operators use the Sound-on-Slide programs at their work stations individually or in small groups to refresh themselves on specific procedures and on new information, as shown in Figure 8.

Copies of all the programs are available in the immediate vicinity of the production line so that any operator can, with the permission of the supervisor, review a program. We have found that most operators prefer to review a Sound-on-Slide program rather than go back to a source document such as a Westinghouse process specification.

Figure 8. A group of operators gathers around the Sound-on-Slide equipment to review and discuss some techniques.

## Program Production Cost and Scheduling

A typical Sound-on-Slide training program consists of approximately 50 frames of information. For estimating purposes we allowed up to 2 hours for each frame to gather information and to write and edit the script. Some programs took longer due to the complexity of the technical material. Non-technical programs, such as on how to fill out paperwork, usually took between 1 to 1-1/2 hours per frame because the material was much less technical.

We also allowed another hour per frame for review sessions, final changes and time to record the audio track. Actual time to produce the audio track was usually the least expensive part of producing a program. Getting the words right took most of the time. On the average each frame usually took about 1 minute to record. A fifty frame program was completed in about 1 hour using a non-professional in-house narrator who was reasonably familiar with the subject material. Material that was well documented in our company procedures or process specifications usually took less time to organize. The more subjective the material, the more time it took to reach agreement between the subject matter experts on correct procedures.

In most cases we found that some delays in gathering information, due to such occurrences as subject experts not being available, changes to the process, etc., are unavoidable. During the production phase, delays can occur in taking pictures because the samples have not been prepared. We normally allowed for these problems since they never seem to go away, no matter how well we schedule and plan. On the average it takes 6-10 weeks to produce a finished, highly technical program.

Expensive equipment exists for taking photomicrographs, but none was available to us during production of the visuals. In order to show the microscopic parts as the operators would see them, we encountered significant difficulties in preparing the visuals. With some minor modifications of available photographic equipment we developed an adapter to attach a 35 mm single lens reflex camera to any stereo zoom microscope on the production line. One eyepiece on the microscope is used for setup while the other holds the camera.

As it turned out, our adapter produced very acceptable slides and prints. The visuals that the operators viewed during training were very close to what they would see if they were looking at the actual part through a microscope. The quality of the visuals was a major factor in the success of our programs.

Since the adapter was portable, we were able to go out to the production area and photograph defects, partial operations, good parts, etc. Based on the evaluation from the trainees, using real parts and equipment from production definitely made the programs relevant.

Because of the commonality of some technical subjects, the cost of producing additional programs has been reduced. Existing information from prior programs can now be used for future programs. Approximately 10-20% of our slides can be duplicated and used in other programs, thereby, reducing the cost of producing new visuals.

## Additional Benefits

An unexpected benefit of the Sound-on-Slide training programs has been improved communications between our functional groups. Traditionally in most manufacturing organizations there have always been various points of disagreement between Design, Manufacturing and Quality engineering. Because we spent a considerable amount of time during the scripting phase to carefully analyze our process and procedures, we now have a convenient form of communication. The development process for these Sound-on-Slide programs has helped us reach agreement on many subjective concepts.

Inspectors now view our training programs with the Manufacturing operators and any disagreements as to interpretation are discussed and ironed out. Because our programs are directed to operators, the technical terms are omitted, and shop terms that are commonly used are explained in clear and simple language. The simple language goes a long way toward conveying the highly technical information to the trainee.

Since information for each training program is based on Westinghouse procedures, new engineers in the Hybrid area have been brought up to speed faster than if they had to sit at a desk and read all the required specifications. New engineers are more productive sooner with the assistance of Sound-on-Slide training programs.

Our programs are also available to the Indusrial Engineering group for review for potential method improvements because the subject matter is presented in a step-by-step manner. Our programs save the engineer from starting from scratch with process familiarization each time.

Although the programs are geared to the manufacturing operator, we have started to make training programs for the inspectors. In the manufacturing programs we instruct the operator on how to make the hybrid; for the inspectors we train them on how to inspect it. The common thread through both programs is the accept-reject criteria. Now both the operator and the inspector can be trained to the same level of quality.

Because of the overwhelming success of the Hybrid Microwave Module Assembly Area programs, we have started 19 additional programs in the Hybrid Packaging area, including such detailed operations as mounting of substrates into packages, sealing of hybrids, and leak testing. In addition, we have started 18 programs for the Printed Circuit Assembly Area.

## Conclusion

We at the Westinghouse Defense and Electronic Systems Center have found the preparation of detailed training programs to be most encouraging. Interest and support is continually growing, and the programs have resulted in reduced rework, improved operator proficiency, higher productivity, and a more comfortable employee-management dialogue. With all these bottom line advantages we are expanding the implementation of the Sound-on-Slide approach to training to other areas in the factory with great expectations.

# QUALITY ASSURANCE PROCEDURES FOR HYBRID MICROCIRCUITS

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## ABSTRACT

This paper will report on the status of a contract (F30602-79-C-0181) with Rome Air Development Center on Quality Assurance Procedures for Hybrid Microcircuits. The contract runs for two years and is scheduled for completion 30 June 1981. The purpose of the contract is to generate a complete package of documentation for hybrid microelectronics that will contain information for both users and manufacturers.

## INTRODUCTION

As a result of a contract with Rome Air Development Center there will be significant changes to the present military specifications relating to the manufacturing and testing of hybrid microcircuits. In addition to updating MIL-M-38510 and Appendix G (Hybrid Microcircuit Procurement Procedures) of MIL-M-38510 and such MIL-STD-883 test methods as 2009 (External Visual) 2017 (Internal Visual-Hybrid), and 5008 (Test Procedures for Hybrid and Multichip Microcircuits), several new documents will be generated. The modifications will include both addition of S level and microwave hybrid requirements as well as changes to the present B level. The new documents will include:

Line Certification Handbook
Fabrication Process and Material Qualification
Design Guidelines Handbook
Applications Guidelines

The Line Certification Handbook along with its companion document, Fabrication Process and Material Qualification will contain the most significant new material.

The purpose of these documents is to provide a uniform method of approving hybrid manufacturing lines for both B and S level products. They will detail:

a. The documentation required for material and process controls
b. Specific areas of concern that should be considered in a line evaluation
c. Qualification test procedures
d. Sample sizes and frequency of testing

These documents are not intended to direct or select the use of any particular material or process but only to standardize on the minimum testing required to qualify a process or material and the documentation required to assure that the qualified process or material will continue to generate satisfactory product.

## GENERAL PHILOSOPHY

The present documents such as Appendix G of MIL-M-38510 and Test Methods 2017 and 5008 of MIL-STD-883 are in the process of being updated for circulation to the Government and industry for comments and coordination. The philosophy used for the changes to the present documentation as well as for the new documents is to move testing requirements earlier in the manufacturing process so that reliability can be improved and costs reduced. Details of some of the proposed changes will highlight this philosophy. The reliability physics approach will be used to define the requirements recommended for the complete documentation package for hybrid microelectronics.

## CHANGES TO 2017

The proposed version of test method 2017 will include the addi- of S level and microwave criteria. Also many new definitions have been added and some changed. One of the major changes is to redefine multilayer to mean several layers of conductors separated by layers of insulation (presently defined as multilevel). The term multilevel has been eliminated and a new definition,composite metalization, has been added to define conductors that consist of several layers of metal in contact with each other. Included in this definition would be items like nichrome/gold and tantalum/gold thin film systems.

The scratch criteria on substrates for Level B has been modified to allow a scratch to completely cross a conductor if less than 25 percent (by width) of the underlying material is exposed. That is, substrate or underlying dielectric for thick film and underlying composite metal for thin film substrates.

All clearances between "non common voltage" conducting surfaces has been increased to 1.0 mil. This was done so that PIND testing requirements could be relaxed in other portions of the documentation package.

The section on resistor trimming has been changed to allow some trimming into the conductor area and treats serpentine resistors as a special case.

The build up of solder and organics for both chip and substrate attachments has been modified based on how close the material comes to a "non common voltage" point rather than any specific height criteria.

Because of the difficulty in visually inspecting substrate attachment,a note has been added to test method 2017 to allow radiographic,centrifuge or drop shock to satisfy the substrate attachment criteria.

The present methods 2010 and 2017 do not protect against wires coming close to,or touching the uninsulated edge of a silicon die. The requirement for a 1.0 mil clearance in this area has been added to test method 2017.

A requirement has been added to allow for a 10 mil clearance from the bottom of the lid to the highest component in the hybrid microcircuit. Recent information shows that for large hybrids and thin lids, 10 mils will not be enough under worst case environmental conditions. A note to this effect also has been included.

The foreign material criteria has been altered based on experience with the 20psig removal method. Small unattached particles tend to remain in place even when the force of the gas blow is enough to flatten the interconnect wires.

## CHANGES TO 5008

The proposed changes to test method 5008 will be more extensive than for test method 2017. Class S criteria will be included in the new version. Periodic tests for die and substrate attachment quality have been added to assure that the attachment processes are under control.

The 100 percent mechanical shock or centrifuge testing has been reduced from 3Kg to 1.5Kg for mechanical shock and from 10Kg to 5Kg for centrifuge. This was possible by adding periodical sampling at higher levels. The philosophy used here and for several other sample tests is to stress the parts at several levels. One level defines a minimum acceptable level. Passing that level would allow production to continue even though the next level of stress resulted in a failure.Failing the second level would,however, require some corrective action since the second level has been set well within good processing capabilities. The higher levels of centrifuge may require a stiffening block to be firmly attached to the bottom of the hybrid to prevent damage to the part as a result of "oilcanning". Adhesives such as Eastman 910 have been used successfully to attach a one eight inch thick aluminum block to a 1" x 2" hybrid bottom. The hybrid was then run to a level of 20Kg on a centrifuge with no failures.

Lot jeopardy for Group B PIND testing has been removed as a result of the increased spacings required in the proposed version of 2017. Since a particle of 1.0 mil or larger would be required to cause a failure,and since the PIND testing for particles of this size becomes more efficient, the requirements for loose particles can be reduced.

Minimal requirements for 100 percent testing of passive components has been instituted.Reviews of hybrid failures showed that most passive component failures could have been screened out with simple 100% testing.

One of the major changes is in the area of Group C testing.The standard electrical life testing has been supplemented with some mechanical testing. The mechanical testing (electrical rejects or fully processed dummy samples can be used) is a modified destructive physical analysis which serves as a minimal check on wire bonding,chip and substrate attachment,loose particle problems,SEM evaluation of metalization and moisture content.

By adding the mechanical testing to Group C,all tests presently in Group D that could not be performed by the package manufacturer have been removed from Group D testing. This could allow the package manufacturer to complete all testing for Group D.

## FUTURE EFFORTS

In the remaining year of the contract revisions to MIL-M-38510, and the new documents will be completed. Much of the efforts on the Line Certification Handbook, the Fabrication Process and Material Qualification Document, the Design Guidelines Handbook and Applications Guidelines will utilize completed and on going DOD contractual efforts in these areas and will include extensive interface with military hybrid manufacturers. Back-up data for much of the material has been gathered and recommendations for testing programs will be made where no data is presently available.

# EFFECTS OF PROCESSING CONTAMINANTS ON HYBRID MICROCIRCUIT RELIABILITY

BY

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## INTRODUCTION

The manufacture of high reliability hybrid microcircuits requires that both the integrated circuit and the package be resistant to environmental attack. Moisture in the environment has been found to cause a signficant number of device failures by means of corrosion of the Al conductor metallization. Such attack is promoted by the presence of active contaminant ions, which may originate in the processes used in manufacture. The materials used in construction of hybrid packages also have been found to be susceptible to environmental attack.

It is clear that acceptable levels of reliability of chip and package will be obtained only if suitable means of control of, or protection from, both moisture and contaminant ions can be provided. In order to develop adequate means of protection, the mechanism of the corrosion process and its causes must be understood, and the sources of corrodant agents must be identified. Accordingly, a program was undertaken in which failure analysis provided information on the nature of the corrosion process, a model of the process was proposed, confirmation of the model was obtained by means of radioactive tracer techniques and the results of this work were applied to both integrated circuit chips and hybrid packages.

## EXPERIMENTAL

### Failure Analysis - Silicon Devices

An analysis of the failures during environmental exposure of integrated circuit chips was conducted to identify the failure mechanism. A group of bipolar logic circuit wafers, passivated with silica glass (Silox), was followed through the entire processing sequence, and samples were withdrawn after each step in the process sequence. After microscopic examination, these samples were exposed to an $85^{o}C/85\%$ Relative Humidity environment for various lengths of time. No electrical bias was applied. After environmental exposure the samples were examined by means of optical and scanning electron microscopy and were then analyzed by EDAX (energy dispersive analysis by x-rays) as well as Auger/ESCA spectroscopy.

Optical microscopy provided a means of examining large areas and assisted in the identification of the corrosion product. SEM examination provided

higher resolution, better depth of field and the capability of analysis (EDAX) for elements of atomic numbers greater than 11. The Auger and ESCA spectroscopy were used for surface analysis and depth profiling of the composition.

Observations on Chip Failures

Failures occurred primarily by means of corrosion of the Al metallization with the point of initiation in every case at a defect in the passivation, usually at a step, corner or other geometric feature of the circuit (Figure 1). The chemical reaction which results in the formation of hydrated $Al_2O_3$ is accompanied by a large increase in volume placing the Silox under stress as shown in Figure 1, taken with polarized light.

As attack progresses, the stress becomes large enough to cause the Silox to crack (Figure 2), with the cracks moving most rapidly along steps or geometric features which constitute points of stress concentration, planes of weakness or areas of poor glass coverage.

When the change in volume of the corrosion product underneath the Silox becomes sufficiently large, complete glass fracturing takes place, (Figure 3) exposing the corrosion product. Under extreme conditions the hydrated $Al_2O_3$ was actually extruded out of an opening in the passivation layer (Figure 4), indicating a very high pressure buildup.

X-ray techniques were used to identify the corrosion product. It was found to be hydrated $Al_2O_3$ and in every case contained a large amount of $Cl^-$ ions.

## MODEL FOR ENVIRONMENTAL ATTACK OF Al CONDUCTORS

Proposed Model

On the basis of the observations cited above, we can propose the following model:

Discontinuities in the Silox passivation layer provide access of the ambient atmosphere to the Al conductor. The presence of moisture in the air provides $H^+$ ions. The Al can then corrode according to the following reactions:[1]

$$2\ Al + 6\ H^+ \rightarrow 2\ Al^{+++} + 3\ H_2 \qquad (1)$$

$$2\ Al^{+++} + 3\ H_2O \rightarrow 2\ Al\ (OH)_3 + 3\ H_2 \qquad (2)$$

The aluminum hydroxide so formed is hygroscopic and can absorb up to 6 molecules of water to become $Al(OH)_3 \cdot 6\ H_2O$.

Chloride ions have the effect of accelerating the attack of Al.[2] Once the $Cl^-$ ions have penetrated the surface oxide, the following reaction takes place:[3]

$$Al + 4\ Cl^- \rightarrow Al(Cl)_4^- + 3e \quad (3)$$

and in the presence of moisture, the $Al(Cl)_4^-$ can react with the available water:

$$2\ Al\ (Cl)_4^- + 6\ H_2O \rightarrow 2\ Al(OH)_3 + 6\ H^+ + 8\ Cl^- \quad (4)$$

This reaction liberates $Cl^-$ ions which are available to continue the attack on the Al.

The discontinuities in the Silox can be pinholes, porosity at steps, cracks or mechanical damage resulting from handling. Since step coverage is generally poor with Silox, this is the most frequently observed location of attack.

The $Al(OH)_3$ produced occupies a much larger volume than the Al consumed, and subsequent absorption of water increases the volume further. This stresses the Silox, finally causing cracking and exposing more of the structure to the atmosphere.

From the chemical equations it can be seen that moisture alone can corrode Al, but the reactions consume the corroding agent therefore the reactions tend to snuff themselves out. When both moisture and $Cl^-$ ions are present, however, the reaction continually liberates $Cl^-$ ions and thus leads to catastrophic failure. This model for the corrosion of Al on passivated integrated circuit chips is shown schematically in Figure 5.

Confirmation of the Corrosion Model

With evidence that $Cl^-$ ions were the contaminant primarily responsible for corrosion, we first sought the source of the ions in the wafer processing sequence. Using reagents tagged with $Cl^{36}$ (a mild $\beta$ emitter) in the various wafer processing steps, it was possible to determine the amount of $Cl^{36}$ (and thus the amount of reagent) retained after each stage of the process sequence.

It was found the $Cl^{36}$ was retained in substantial quantities after the wafer was subjected to a mild $HNO_3/HCl$ etch, Table 1. Subsequent rinsing in hot and cold distilled water did not remove the $Cl^{36}$, indicating it had penetrated the passivation layer and was held within or under the Silox. Only by removal of the Silox itself could the $Cl^{36}$ be removed.

To determine the location of the $Cl^{36}$ on the wafer surface, a wafer, contaminated by $Cl^{36}$ in the etch described above, was counted and autoradiographs were made. The autoradiograph in Figure 6 show the locations of significant $Cl^{36}$ contamination. This wafer section was then exposed to the 85°C/85% R.H. environment. After a very short time (< 8 hrs) local corrosion attack was noted, (Figure 7) and the locations of corrosive attack showed a one-to-one correspondence with the $Cl^{36}$ concentrations on the autoradiograph. This established clearly the cause and effect relationship between $Cl^-$ ions and accelerated Al corrosion.

Table 1. Chlorine Retained after Processing. Values are Obtained from Radioactivity Counts.

| Sample | Micrograms Cl Retained after $HCl-HNO_3$ Etch | Micrograms Cl Retained after HF-Acetic Acid (Stage B) |
|---|---|---|
| 1 | 0.09 | $1.5 \times 10^{-4}$ |
| 2 | 0.07 | $1.8 \times 10^{-4}$ |
| 3 | 0.05 | $3.6 \times 10^{-4}$ |
| 4 | 0.10 | $2.2 \times 10^{-4}$ |
| 5 | 0.08 | $3.6 \times 10^{-4}$ |
| 6 | 0.08 | Not etched |

## ACTIONS TAKEN TO IMPROVE ENVIRONMENTAL RESISTANCE

Since the corrosion model as confirmed involves:

- Passivation defects
- Penetration by moisture
- Contaminant ions

as necessary conditions for rapid corrosive attack, two specific actions were taken to prevent corrosion failures:

1. Silox, which inherently gives poor step coverage, was replaced by silicon nitride, which has been found to provide superior step coverage. This drastically reduced the access of moisture and the number of points at which corrosion could initiate. In addition, because of the excellent adhesion of the silicon nitride to the device surfaces, it was found that even where corrosion did initiate (Figure 8) it was contained, being almost nodular in character and showing no tendency to propagate along edges or steps. The corrosion product was chemically like that produced on Silox passivated chips.

2. The wafer processes were examined for potential sources of chlorides. Those process steps or process reagents which could result in the release of chloride ions were eliminated where possible and in those cases where elimination was not practicable steps were taken to tie up the chloride ions chemically to minimize their corrosive effects.

The two actions described above reduced $Cl^-$ related corrosive failures to a marked degree, increasing the resistance to environmental exposure by more than two orders of magnitude. This type of $Cl^-$ ion attack is no longer considered a significant cause of failures.

## HYBRID PACKAGE

In the assembly of hybrid packages, a number of cleaning processes are included, often employing chlorinated solvents. Since we know chlorine is present in some form, we decided to use the radioactive tracer techniques described above to determine the amount of $Cl^-$ ion retention as a function of the assembly and cleaning processes. This was done for two common cleaning solvents, DuPont TMS Freon and methylene chloride (dichloromethane).

### Experimental - DuPont TMS Freon

The hybrid package used in this investigation was a multilayer, multichip thick film package based on an $Al_2O_3$ substrate. Substrates were taken from four stages of the assembly process:

- Bare $Al_2O_3$ substrate
- Substrate processed through top metallization
- Substrate with chips attached
- Substrate with chips attached, coated with a silicone gel.

The cleaning solvent was DuPont TMS Freon innoculated with HCl tagged with $Cl^{36}$ (radioactive). The concentration was 0.2 N and the ratio of $Cl^{35}$ to $Cl^{36}$ was 3.5 to 1.

All four samples were processed as follows:

1. Count Radioactivity (Background Determination)
2. 20 Minute Immersion in $Cl^{36}$ Tagged TMS
3. Air Dry 24 Hours at 25°C
4. Count Radioactivity (Column A, Table 2)
5. 15 Minutes Rinse, Untagged TMS
6. Count Radioactivity (Column B, Table 2)
7. Air Dry 48 Hours at 25°C
8. Count Radioactivity (Column C, Table 2)
9. $H_2O$ Wash, 3 Times - 15 Minutes at 25°C
10. Air Dry 2 Hours at 25°C
11. Count Radioactivity (Column D, Table 2)

The radioactivity of the samples was determined in a modified windowless gas flow counter. Counts were made in the four quadrants of the package and in total represented about 88 percent of the substrate area.

The results obtained are summarized in Table 2. The values listed are micrograms of total ($Cl^{35}$ + $Cl^{36}$) chloride ion retained on the substrate. After immersion all the substrates retained measurable amounts of chloride with the retention an order of magnitude higher on those substrates on which chips were attached.

As seen in the table, the use of a second rinse in untagged TMS Freon does not reduce the $Cl^-$ ion retention, but a series of water rinses reduces

Table 2. Results of Cleaning Tests Using TMS Tagged with $Cl^{36}$ Expressed in Micrograms of Chlorine.

| Sample | A After 24 Hrs Air Dry | B After TMS Freon Rinse | C After 48 Hrs Air Dry | D After Triple $H_2O$ Rinse |
|---|---|---|---|---|
| Bare Substrate | 0.06 | 0.08 | 0.04 | 0 |
| After Top Metallization | 0.04 | 0.05 | 0.04 | 0 |
| After Chips Attached | 0.66 | 0.73 | 0.72 | 0.39 |
| Coated with Silicone Gel | 0.24 | 0.23 | 0.22 | 0.17 |

$Cl^-$ ion retention essentially to zero for the unpopulated substrates. The water rinses slightly reduce $Cl^-$ ion retention on substrates with chips attached, but a rather high concentration remains firmly attached.

The difference in behavior between the populated substrates and the bare or metallized substrates suggests that different mechanisms are involved. The effectiveness of rinsing in either TMS or water in cleaning the bare and the metallized substrates indicates simple adsorption had occurred. The relative difficulty of removal of chloride from the populated boards may be related either to much greater probability of entrapment under chips, leads, etc. or a reaction between the $Cl^-$ ions and the solder or the lead materials. In both cases, retention would be expected to be high.

Experimental - Methylene Chloride Solvent

A set of similar experiments was run using methylene chloride tagged with $Cl^{36}$ (one microcurie $Cl^{36}$ per ml methylene chloride). The substrates were:

1. Bare $Al_2O_3$ substrates
2. Substrates plus gold metallization
3. Solder added
4. Riser added
5. Completed substrate, chips not attached
6. Completed substrate, chips attached.

After immersion in the radioactive methylene chloride, the activity on the substrates was counted. Since substantial evaporation was observed, a second set of data were obtained after a 24 hour drying cycle at 25°C. These data are listed in Table 3.

The amounts of $Cl^{36}$ retained were in every case much less for methylene chloride than for TMS Freon, usually an order of magnitude less after a 24 hour drying cycle. In addition, the rinsing procedures used for TMS Freon were much more extensive. A direct quantitative comparison should be avoided, however, since different chemical species were involved.

Table 3. Chloride ion retention on substrates after cleaning in activated methylene chloride.

| | Retained Cl in Micrograms | |
|---|---|---|
| | Immediately after Cleaning in Methylene Chloride | After 24 hours at 25°C |
| Bare Substrate | .02 | .001 |
| Substrate and Gold | .009 | .004 |
| Solder Added | .02 | .005 |
| Riser Added | .03 | .02 |
| Complete - No Chips | .05 | .03 |
| Complete, Chip Attached | .03 | .03 |

Since evaporation was such an important factor in the case of the bare, the metallized and the solder coated substrates, an evaporation experiment was run to determine the time needed for evaporation to be complete. Table 4 summarizes the results of that experiment and shows that evaporation is essentially complete after 50 minutes drying time.

Table 4. Radiation Counts After Cleaning a Metallized Substrate *in Activated ($Cl^{36}$) Methylene Chloride and Drying at* 25°C.

| Time | Counts/Minute |
|---|---|
| 0 | 289 |
| 10 | 261 |
| 20 | 256 |
| 30 | 250 |
| 40 | 239 |
| 50 | 235 |

Autoradiography

Since it was clear that the completed packages retained an appreciable amount of chloride ions, we wished to determine the locations or distribution of the retained chloride ions. Therefore autoradiographs were made of the completed packages using $Cl^{36}$ tagged methylene chloride.

A micropackage with chips attached was put through a cleaning sequence in $Cl^{36}$-tagged methylene chloride and given a final rinse in distilled water. An optical photograph of this package is shown in Figure 9a while the

autoradiograph of the package is shown in Figure 9b. In order to get the film close to the surface of the package, the film was cut into two sections to avoid the large Cu bus. On the radiograph, white spots are areas of higher $Cl^{36}$ concentration (e.g., arrows); the dark areas are those with little or no $Cl^{36}$. There is a gradual increase in density from left to right which is an experimental artifact.

It is clear that the I-C chips are almost completely free of $Cl^{36}$ while the areas around the chips retain considerable $Cl^{36}$. This is not surprising since these areas offer sites for entrapment under leads or in the somewhat porous dielectric. The Cu power decal retains a small amount of $Cl^{36}$ as do the unpopulated chip sites across the top row of the radiograph. These results indicate the need for a rinsing action sufficiently vigorous to clean out inaccessible areas of packages such as found under leads to remove all except chemically bonded Cl.

## SUMMARY

This work has made clear the role of $Cl^-$ ions in the corrosion of Al metallization, has provided a model for the corrosion process and has pointed to several corrective measures. It also has made it clear that Silox is not a satisfactory passivation layer because of inadequate step coverage. Silicon nitride has been proved to be superior. The development of a radioactive tracer technique was an essential part of the work.

The extension of the radiotracer study to the hybrid package has provided an extremely sensitive method of evaluating cleaning solution effectiveness, with respect to $Cl^-$ ions. Finally, the autoradiographic technique has disclosed the location of the retained $Cl^-$ ions and indicates that entrapment is a primary cause of $Cl^-$ retention.

## ACKNOWLEDGMENTS

The authors wish to thank Honeywell Inc for the opportunity to do this work and publish the results and to thank R. I. George and L. J. Hallgren for their assistance in the experimental work.

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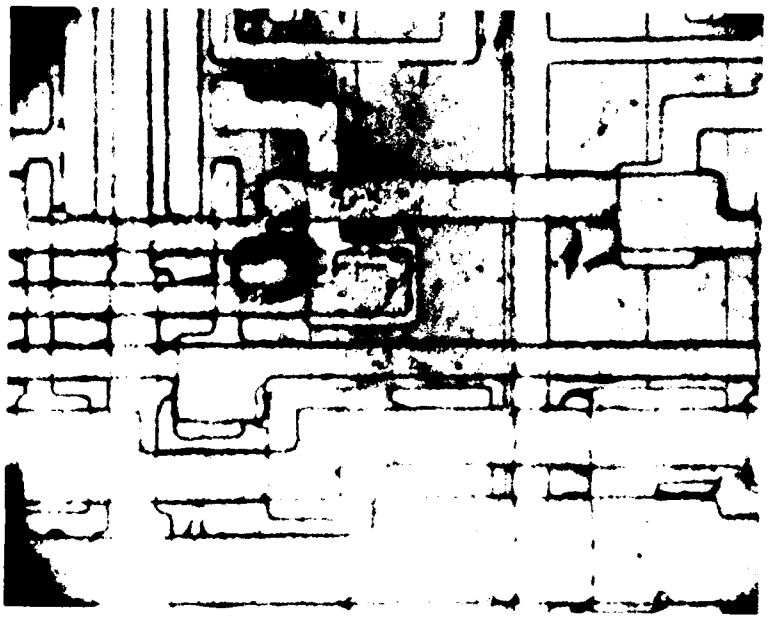


Figure 1. Integrated circuit chip after 8 hours at 85°C/85% RH showing initial point of environmental attack X400

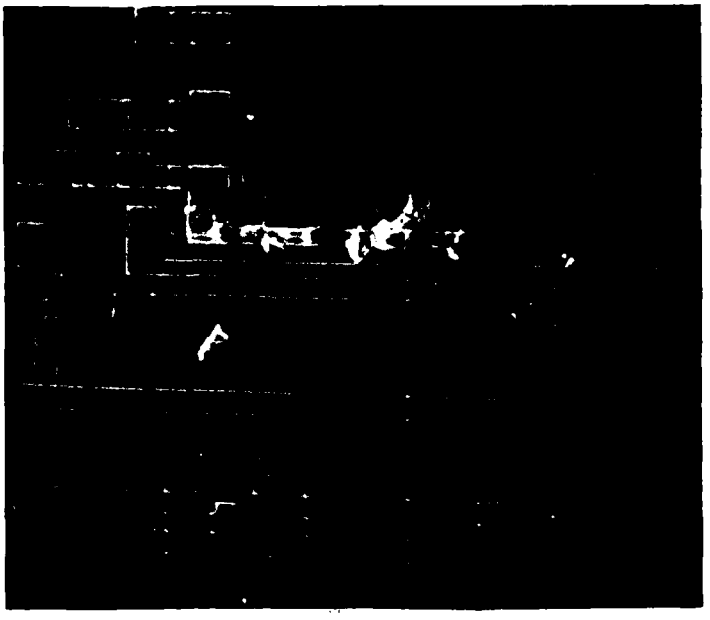


Figure 2. Early stage of Al corrosion showing Silox cracking along edge of conductor. X160

Figure 3. Advanced stage of Al corrosion, showing fractured Silox and exposed corrosion product. X1600

Figure 4. Extreme conditions of Al attack showing corrosion product extruded out through cracks in Silox. X1700

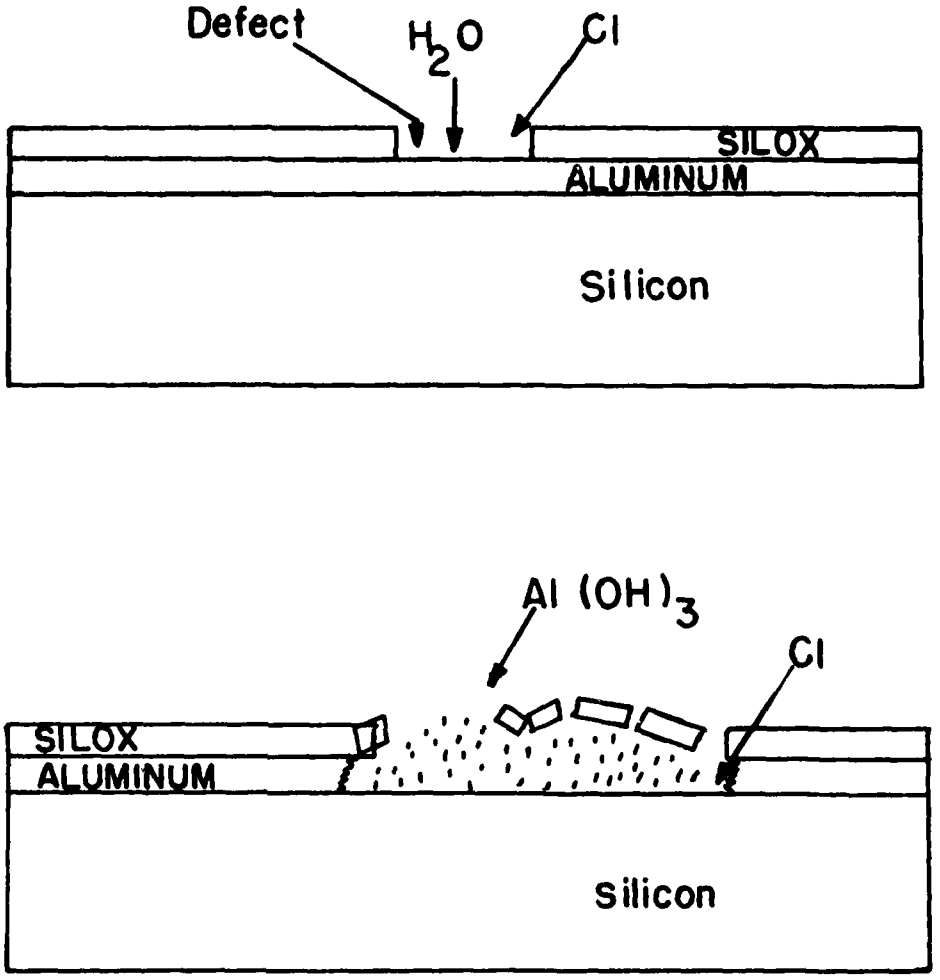



Figure 5. Proposed model for corrosion of integrated circuit passivated with Silox. Upper portion shows point of attack; lower portion illustrates advanced stages.

Figure 6. Autoradiograph of Si wafer showing "hot spots" after exposure to radioactive HCl.

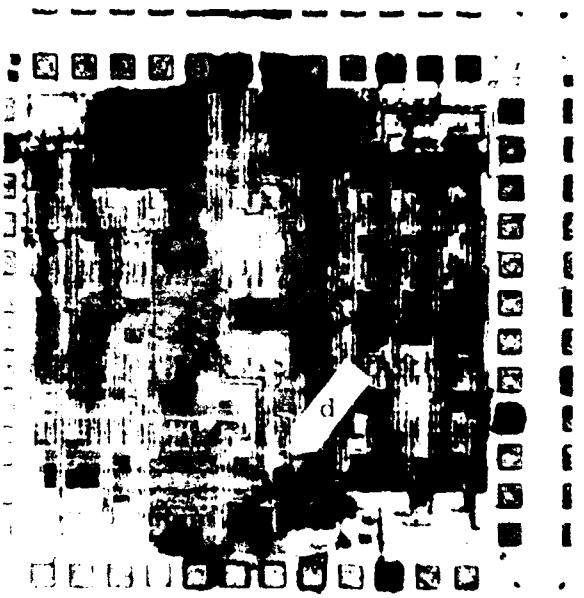


Figure 7. Local attack on wafer previously exposed to radioactive HCl.

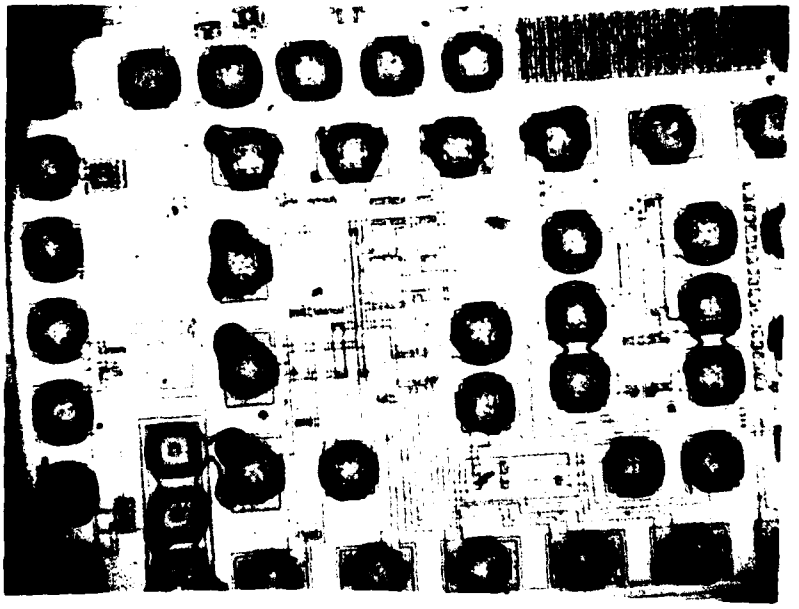
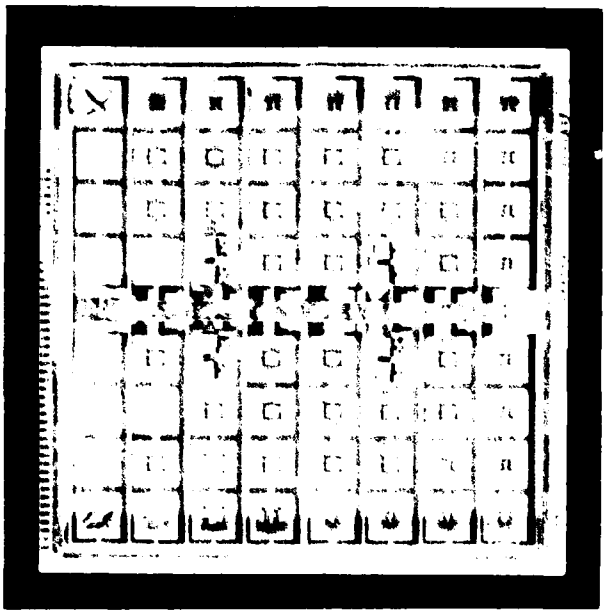
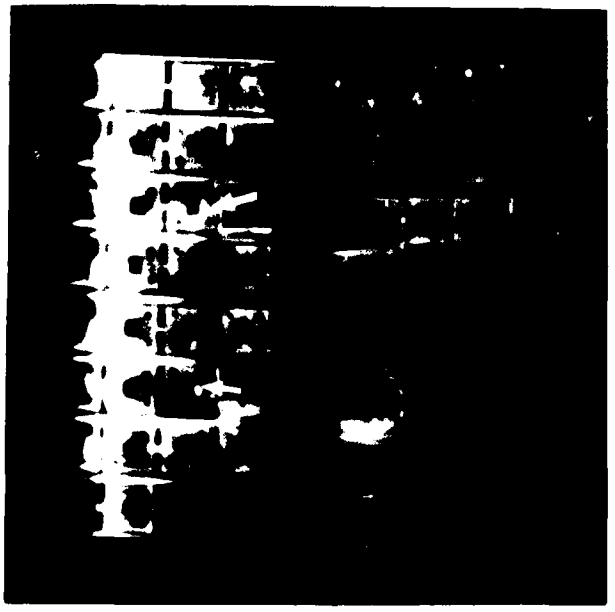


Figure 8. Integrated circuit chip passivated with Silicon nitride, showing a contained or "nodular" mode of attack.



a



b

Figure 9. Optical photograph and autoradiograph of multi-chip package showing concentrations of $Cl^{36}$ (arrows). Dark-to-light gradation is an experimental artifact.

# QUALITY ASSURANCE OF HYBRID CIRCUITS

BY

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## ABSTRACT

This report is based upon the development of specifications for the performance, test, manufacture, and acceptance requirements for two specific military hybrid integrated circuits (STINGER & PATRIOT). In general MIL-STD 883, MIL-STD-750, and MIL-M-38510 give specifications for testing, inspection, and performance standards for all microelectronic components. But it is necessary to develop a unique MIL-SPEC for each hybrid system based upon the system environment and performance characteristics.

Since the beginning of the Microelectronic field the General MIL-STDS have been a constantly evolving system. The hybrid field was still in it's infancy during the initial design stages of the STINGER & PATRIOT hybrids. New techniques, materials, processes, and testing were constantly on the horizon. It was necessary to develop a complete device specification for these hybrids and as a necessity these specifications had to change with the frontiers of hybrid design.

The results of these efforts have been published as MIL-F-48370 (STINGER) and MIL- S-63256 (PATRIOT). The hybrids from these two systems repre sent different technologies (STINGER uses discrete thin film chips and PATRIOT uses fired on components). The body of this report outlines the development of these specifications, the problems encountered and how they were solved. The paper discusses the new technologies used in these hybrids which weren't addressed in the current MIL-STD's and the changes which were necessary to handle these new technologies. As a result, we feel that this method of developing a tailored MIL-SPEC for each new hybrid (system) insures a more reliable and controllable component.

## INTRODUCTION

Failure caused by manufacturing defects must be anticipated and prevented. Careful visual inspection before package sealing plays an important role in detecting and screening such defects. In large hybrid circuits it is

relatively easy for the inspector to overlook small defects; accordingly environmental and electrical stress testing is necessary to complement the visual inspection and to further insure against marginal conditions that would jeopardize long term reliability. Specifying exact requirements for the visual acceptance and defining stress conditions that will assure high confidence levels of reliability under the expected operating conditions in the system are the task of the QA engineer.

In this presentation we will give two examples (hybrids of the STINGER and PATRIOT S&A) and show how specifications were developed. In general MIL-STD 883, Section 2017 describes the visual inspection of hybrids and was followed as closely as possible and each applicable criterion was documented with illustrations. In addition specific problems that were unique to the particular manufacturer and his technique were examined. For example the different manufacturers of the STINGER and the PATRIOT hybrid utilized different manufacturing techniques for the resistors-thick film (PATRIOT) versus thin film resistors (STINGER)-and a special effort was made to identify and characterize all potential failure producing conditions.

To assist the manufacturer in supplying high quality products special restrictions and/or requirements for the fabrication process were worked out to prevent the occurrence of marginal conditions. A good example of this is the rework procedure. Replacement of chips, rebonding of wires, resealing, etc., were limited to a reasonable number of rework times. Ideally, we would like to eliminate rework because each intrusion into the finished product can introduce additional defects in the surrounding area and the condition of the reworked area (i.e., film thickness underneath the chips ) cannot be guaranteed. With todays increasing use of LSI's in hybrids and the impossibility of electrical function testing of these LSI's before build-in, such a rigorous restriction (no rework) is impractical from both a cost and yield viewpoint. Therefore a compromise has to be reached.

## DISCUSSION

The purpose of the MIL-STD is to establish a uniform procedure for inspecting and testing microelectronic devices and circuits so they meet the high quality requirements necessary for military applications. The intention is to cover all possible test methods and make it applicable to "all" types of devices.

From the above it is obvious that with the rapid development in new device techniques, the completeness of the MIL-STD becomes outdated. New techniques (i.e.,tape automated bonding) and their deficiencies are not covered and the consumer must be aware of this lack of inspection and test criteria. If the user relies on the completeness of the MIL-STDs and its applicability to all types of devices, then this can cause problems.

On the other hand, the attempted universality of the MIL-STDs re-

sults in a multitude of criteria which are not specific to one particular device type. Therefore it is necessary for the user to screen and select the small percentage of inspection criteria which are applicable to the particular hybrid.

In the case of the STINGER and PATRIOT hybrids a new approach was utilized. After having selected the manufacturer, which identified the manufacturing techniques used, those criteria from MIL-STD 883 and 750 which addressed acceptance standards for those techniques were extracted. Then in collaboration with the manufacturer, defects that were common to his procedures were collected and documented with illustrations, using either light or electron microscopy. In this process of close collaboration during which the manufacturing facilities were accessible to us, microscopic analysis often disclosed defects which had not been addressed in the MIL-SPECs. It must be mentioned at this point that the manufacturer who is experienced with military requirements normally develops his own inspection standards to insure product quality. These are directed towards problems unique to his product.

A tailored device standard was thus generated combining the applicable criteria of MIL-STDs 883 and 750 with the manufacturer's inspection standards. This specific device STD was complemented by visual aids generated from manufactuer/contractor samples to illustrate the rejection criteria.

After having established this base for device quality, continuous observation of the process development was necessary to identify any problem areas requiring changes and any desirable extension of the established standard. Additional reject criteria were added and special restrictions imposed (e.g., the rework restriction and the unique specifications for the overbonding that was later deleted). It is emphasized that even the specific device standards are not necessarily final; depending on new development, new manufacturing equipment and/or techniques or other problems, alterations become necessary.

A. Rework

1. The area of hybrid rework is one that requires a clarification and interaction between the customer and the producer. The producer would like to be allowed unlimited rework and refer to it as a standard part of his manufacturing process. The high reliability user must limit the amount of rework but as the complexity of hybrids increase the need for more rework, becomes evident. At ARRADCOM the decision of limiting the amount of rework was based on the fact that any rework operation on a completed or a semi-finished hybrid item, presents a risk of degrading the performance of that item.

2. Initially, rework of the STINGER Hybrid package seal was allowed but complete delidding for the purpose of rework of the interior was not allowed. It is now our feeling that delidding/rework/resealing be allowed as long as it is a well defined procedure with good quality control and screening of the devices afterward to insure the reliability of the devices. Experience in-

dicated that the cleaning and scrubbing of a pad for component attachment could only be guaranteed successful two times. Therefore replacement of active or passive elements or die was limited to two.[4] It was also realized that total die replacement was impractical therefore, no more than 10% replacement of the total elements or die was allowed. Determining the number of rebonds permitted requires interaction with the producer. The producer would like in most cases to be able to replace or repair wires as he sees fit. But based upon experience as the number of rebond attempts increases the overall reliability of the finished product decreases. Thus, rebonding was limited to a maximum of 10% of the total number of bonds.

3. In conclusion, rework is a very strenuous and difficult task to define, but to reduce the consumer risk, specific limits must be established. It is our suggestion and it has been our practice to negotiate these with the producer. The STINGER MIL-STD left a great deal to be desired in this area. Our second attempt, we hope is better which defines the rework for PATRIOT hybrid (MIL-S-63256).

PATRIOT Rework

Rebonding and Element Replacement for Hybrid Microcircuits - Unless otherwise specified, rebonding and replacement of attached elements in hybrid microcircuits shall be permitted with the following limitations :

No scratched, open or discontinuous metallization paths or conductor patterns shall be repaired by bridging with or the addition of bonding wire or ribbon.

No more than one rebond attempt shall be permitted at any pad or post and no rebonds shall be made directly over an area where metallization of intended wire bond areas has been lifted.

The total number of rebond attempts per hybrid (exclusive of total element replacement) shall be limited to a maximum of 10% of the total number of bonds in the hybrid microcircuits. The 10% limit on rebonds may be interpreted as the nearest whole number to the 10% value. A bond shall be defined as a wire to post or wire to pad bond (i.e. for a 14 lead wire-bonded package there are 28 bonds). Bondoffs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically off the plated post or if they contain a non-typical number of wedge marks. The initial bond attempt need not be visible. The replacement of one wire bonded at the end or an unsuccessful bond attempt at one end of the wire counts as one rebond: a replacement of a wire bonded at both ends, or an unsuccessful bond attempt of a wire already bonded at the other end counts as two rebonds. A ball bond on top of a ball is not permissable.

Replacement of active or passive elements or dice shall be limited to a

maximum of 10% of the component with a further limit of two replacements of each element or die. Rebonding of wires to substrate pad or package post done to effect element replacement shall not be counted against the rebond limitations of 3.1.1.1.

Regardless of the number of allowable rebonds or element replacements, all rebonding or element replacement of the hybrid must be accomplished in no more than three recycles of any single hybrid for rework after initial electrical test.

Since this criteria has not been tried, it may require some additional modifications, but we feel it is a good starting point and each time we refine this process it will be reflected in our other documents. In summary, it is important that rework be defined and negotiated between the user and the producer, and it is clearly understood that each time a repair to a hybrid is made, it is considered rework and be counted as such. Some latitude and exceptions to any rework criteria must be considered on a reasonable and rational basis by both parties.

B. Internal Visual Inspection

During the early engineering development phase of the STINGER hybrids the contractor encountered several novel visual faults which were not addressed in either MIL-STD 883 or MIL-STD 750. Also, many questions arose as to the correct interpretation of certain visual rejection criteria described verbally in the MIL-STDs. Therefore, it was felt that in order to eliminate these ambiguities a photographic book illustrating the visual rejection criteria be developed. Added to this book were many new visual rejection criteria not included in the MIL-STDs.

The resulting visual criteria was intended to accomplish several objectives. The first objective was to clarify the interpretive descriptions in the general MIL-STDs with photographs illustrating the fault. Secondly, it was intended to improve and standardize the quality of the hybrids by better defining the visual criteria of MIL-STD 883. Finally, the visual criteria in the general MIL SPECS covers all types of devices and processes whereas a particular hybrid would require only a subset of the general MIL-SPEC criteria. Therefore, it was necessary to tailor the general MIL-SPEC's visual criteria by including only the criteria pertaining to the particular hybrid. These objectives were accomplished with the development of the photographic visual inspection procedure.

The final visual inspection criteria was accummulated from three sources; 1) MIL-STD 883 Method 2017, 2) MIL-STD 750 Method 2072, 3) Manufacturers of various hybrid components. The first step was assembling the visual criteria pertinent to the STINGER hybrids. This was accomplished by extracting from MIL-STDs 883 & 750 only those criteria applicable. Then new criteria were added which weren't addressed in the MIL-STDs. To accomplish

this the visual reject criteria was requested from several hybrid component manufacturers. Once this information was assembled in the proper format components were examined to find good illustrative examples of each rejection criterion. The following paragraphs explain some of the new criteria which had to be included in these specifications.

An example of an unnecessary inspection criterion is in MIL-STD 750B Section 2072 Part 3.1.1.1 which states the rejection criteria for metallization scratches for Discrete Semiconductor Devices. Four of the five criteria do not apply to the discrete devices used on the STINGER Hybrids. Shown below is this section on metallization scratches with the one part pertinent to the STINGER Hybrids in capital letters.

3.1.1.1 Metallization scratches (see figure 2072-1). A scratch is defined as any tearing defect that disturbs the original surface of the metal.

(a) For die with 10 or less interconnecting paths-A scratch that exposes oxide anywhere along its length and leaves less than 50 percent of the original metal width undisturbed. An interconnecting path is defined as the region of metallization between the bonding pad and the pre ohmic window cut.

(b) For die greater than 10 interconnecting paths (and are not low noise or power devices) - A scratch that exposes oxide anywhere along its length and leaves less than 50 percent of the original metal width undisturbed, in 10 percent or more of the interconnecting paths.

(c) FOR DIE WITH NO INTERCONNECTING PATHS- A SCRATCH THAT GOES COMPLETELY ACROSS ANY METALLIZATION PATH AND EXPOSES THE UNDERLYING SURFACE SUCH THAT 50 PERCENT OR MORE OF THE CONTACT AREA IS ISOLATED FROM THE BONDING PAD.

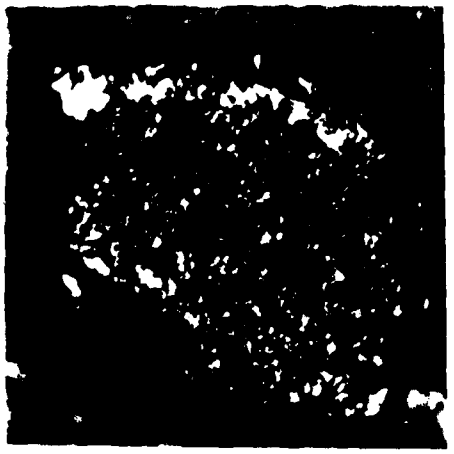
(d) For die with 10 or less interconnecting paths- A scratch which goes completely through the metallization on the contact window and isolates more than 50 percent of the design contact window area from the interconnecting metallization.

(e) For die with greater than 10 interconnecting paths (and are not low noise or power devices ) - A scratch which goes completely through the metallization on the contact window and isolates more than 50 percent of the design contact window area from the interconnecting metallization on 10 percent or more of the interconnecting paths.

For an on-line inspection it would be very time consuming for an inspector to have to continually scan through all this verbiage. Therefore, the inspection procedure for the STINGER hybrids contains only this pertinent part (3.1.1.1C).

Another area in which MIL-STD 883 needed some supplement was visual rejection criteria for discrete thin film resistors. Neither MIL-STD 883 nor MIL-STD 750 addressed thin film resistors thoroughly. Therefore, by canvassing the thin film resistor industry a more complete set of rejection criteria of these components was compiled.(5)

A unique fault of the STINGER discrete thin film resistors concerns the chip bottom (Photo 1).



40.1.4.5 A crack or chip in the backside of a die which leaves less than 75% of area or, a crack or chip under a bonding pad.

Photo 1

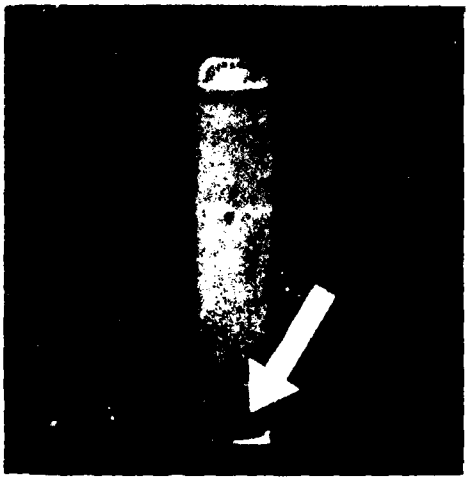
Many of the resistors used on the STINGER are Back-Contact Resistors (where one contact end of the resistor is the gold conductor on the bottom of the chip). These resistors are scribed and cut from the wafer by the manufacturer and shipped to the contractor as individual parts. Apparently during the scribing and breaking operation some of the chips have the gold backing partially torn off. Since these are back contact resistors, this can cause failure due to poor electrical contact. It might also be the cause of poor physical attachment, because the backside is not completely flush with the substrate during bonding. This inspection requires a special jig to turn the resistor over and examine the backside. It can be performed either at incoming inspection or just prior to attachment.

The visual acceptance criteria for the ceramic chip capacitors was also expanded beyond MIL-STD 883.(6) Several new criteria were added and some good illustrative examples of all criteria were found. One particularly obvious problem would be "missing metallization exceeding more than 10% of each surface" illustrated in photo 2.

40.2.4 Missing metallization exceeding more than 10% of each surface.

Photo 2.

Another valuable criteria is "Pad dimension not within minimum and maximum values specified" illustrated in photo 3. Both of these faults are not addressed in the MIL-STDs.



40.2.5 Pad dimension not within minimum and maximum values specified.

Photo 3.

Another major addition was to the bonding criteria. The STINGER hybrids used a "compound" which was not included in MIL-STD 883. The "compound" wire bond is a thermosonic ball bond on top of a stiched wire illustrated in photo 4.

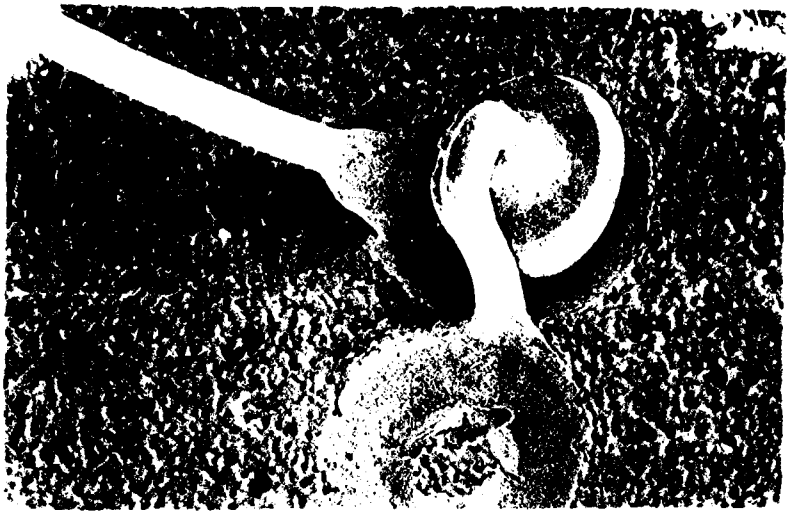


Photo 4.

This type of bond was initially allowed because the contractor said it was necessary to meet pull requirements. Therefore a set of visual acceptance criteria was developed for it. Then the contractor purchased some new automatic bonding equipment and demonstrated they could meet the pull forces by using only the stitch bond. After the stitch bond was tested to assure it's reliability the ball overbond was eliminated. Also, stitch bond visual reject criteria were developed since this bond is not addressed in section 2017 of MIL-STD 883. Photo 5 illustrates stitch bond.

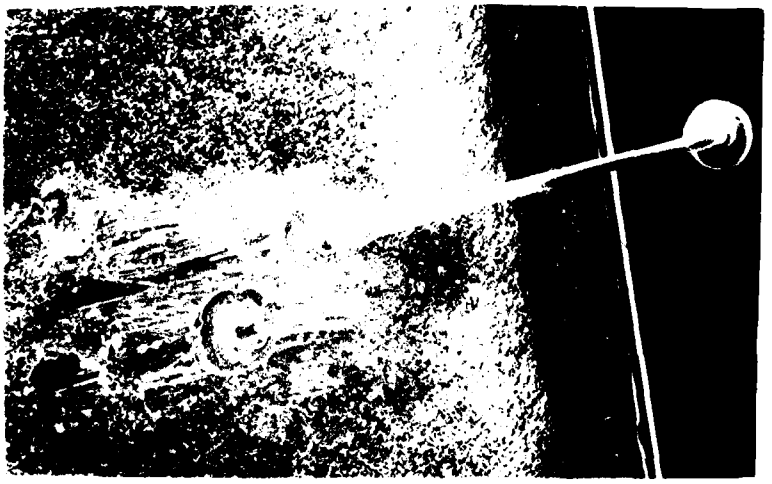


Photo 5.

Results:

A. Visual Inspection Criteria

1. Weed out defective inexpensive components early.

2. Present a clear, concise photographic book illustrating rejection criteria.

3. Standardize pre-cap visual inspection criteria.

B. Rework

1. Some amount of rework must be permitted.

2. All types of repair must be considered rework.

3. Rework limits need to be defined by mutual agreement between user and manufacturer.

4. Need to allow flexibility in rework limits in the form of case by case waivers.

Conclusions:

The development of unique specifications is an effective means of controlling the quality of High Reliability Hybrids. Also, it is felt that the photographic visual inspection criteria definitely enhance the effectiveness of this inspection procedure. Finally, rework is an area which needs to be defined with each hybrid manufacturer.

REFERENCES

1. MIL-STD-883A, Method 2017, "Internal Visual (Hybrid)", Method 2010, "Internal Visual (Monolithic)", 15 Nov 74.

2. MIL-STD-750B, Method 2072, "Internal Visual (Pre-Cap) Inspection", 20 Dec 71.

3. MIL-M-38510D, 31 Aug 77.

4. Herring S. et al, Magnavox Corp., Ft. Wayne, IN, Personal Communication.

5. Puri N., Semi-Films Tech., Personal Communication.

6. Soltis R, N., Vitramon, Personal Communication.

# ELECTRICALLY CONDUCTIVE EPOXIES
# HOW RELIABLE ARE THEY?

by

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## ABSTRACT

Although not widely reported, several hybrid manufacturers have experienced electrical resistance problems when attempting to attach semiconductor devices to gold interconnect patterns on alumina substrates with silver-filled conductive epoxies. Electrical failures due to this problem have been reported at all stages of the hybrid circuit's fabrication and use. These electrical resistance problems may generally be characterized as either a higher than expected linear or nonlinear resistance.

This paper reports upon an investigation of these problems. Failure modes are identified and characterized with regard to time-to-failure, current-voltage relationships, reaction to stresses such as current, voltage, temperature and time. Theories for the physics of the failure mechanisms are advanced, based on empirical data including SEM photographs of sectional samples and thermal aging test results. Failure mechanisms were found to be related to die backside metalization system, die size, and epoxy handling.

## INTRODUCTION

As the number of components in hybrid microelectronic circuits has grown from less than ten to 1000 or more, the time required for die attach and the likelihood and difficulty of repair have also risen. For example, in the case of hybrids with fifty or more dice, the time required for die attach will be on the order of one hour. If eutectic die attach is used, substrate temperatures will be approximately 350°C for this period of time. This can have a detrimental effect on many components such as resistors where accurate tolerances and tight temperature coefficients are required. Also, many integrated circuit performance characteristics, most notably FET input op amp offset voltage, may be altered by this time and temperature exposure. Although most IC manufacturers are willing to guarantee device performance after a 1 to 5 minute exposure to eutectic attach temperatures, few if any are willing to guarantee performance after exposures of 1 to 2 hours. Many presentations have been made which show the declining hybrid yield as a result of increasing complexity. The problem of repairing eutectically attached devices in these circuits is most difficult. Typically a thermal-mechanical removal technique is used, which involves heating the entire package to near the gold-silicon eutectic temperature, and then localized heating is applied to the defective die location, first to remove the die and secondly to replace

it. The problem arises from the fact that the metallic package acts to prevent localized heating from the bottom. Often this is overcome by impinging a heated gas from the top which is directed to the defective die location. The inability to achieve this localized heating often results in damage to adjacent components such as gold flow shorts or nonexpanded contact transistors and diodes, resistor and capacitor value shifts, and integrated circuit performance degradation.

In order to overcome these problems, it was decided to establish an epoxy die bonding process. Three epoxies were selected very early in the program, based upon cost, application method, and experience accumulated throughout the industry. These epoxies are categorized below.

| Epoxy | Filler Material | Filler % by Weight | Classification | Time to Cure @ 150°C | $T_g$ (°C) |
|---|---|---|---|---|---|
| A | Silver (V9) | 70 | 100% Solids Single Component | 65 min. | 58 - 78 |
| B | Silver (Larger Platelets than A) | 50 | 100% Solids Single Component | 65 min. | 58 - 78 |
| C | $Al_2O_3$ | 70 | 100% Solids Single Component | 55 min. | 140 |

Several steps were taken to arrive at a capability for epoxy bonding semiconductor devices, ceramic capacitors, and other components to metalized ceramic substrates. These evaluations consisted of epoxy application methods, repair process, layout criteria, bleedout, mechanical strength, thermal resistance, epoxy seam thickness, and electrical resistance. This paper discusses the electrical resistance evaluation and its results.

## BACKGROUND

In order to obtain a reliable ohmic connection between two conductor surfaces, two conditions are required. The first condition is that the surfaces must be clean and free from insulating films or oxides, and the second condition is that there must be sufficient force holding the two conductors together to overcome any forces which might tend to pull them apart, such as vibration or thermal expansion/contraction.

If, on the other hand, one desires to obtain a reliable ohmic contact between a conductor and a semiconductor, these two conditions may not suffice. It can be shown [1] that, if the semiconductor surface has been polished or

etched, the resulting contact will very likely be a rectifying junction which follows the general diode equation:

$$I = I_S(e^{\frac{qV}{nKT}} - 1)$$

where

A = empirically determined number

I = current

$I_S$ = reverse saturation current

q = charge of an electron

V = voltage

K = Boltzmann's constant

T = temperature

This will be true if the work function of the metal $\phi_M$* is greater than the work function $\phi_S$ for an n-type contact and $\phi_S$ is greater than $\phi_M$ for a p-type contact.

If an n-type semiconductor with gold vacuum deposited onto a smooth polished surface, such as an NPN transistor which has been back-etched, is considered, it is seen that an undesirable n-type contact will result. However, if this gold is sintered or alloyed into the semiconductor, the effect will be to increase the reverse saturation current due to the gold acting as a "getter" in the semiconductor and thereby reducing the minority carrier lifetime. Thus, in effect, an ohmic contact is the result.

In the photomicrograph of a sectioned epoxy bonded semiconductor shown in Figure 1, one can see that there are four contacts which must have reliable ohmic characteristics. These are depicted in Table 1.

Several people [2,3,4,5] have reported on problems experienced with the semiconductor-gold contact. Most state that the gold must be properly sintered. This contention is supported by the previous analysis and by experiment as is shown later in this paper. Problems with the chip backing gold and the epoxy silver contact have been reported. Svitak and Williams [6] found no electrical problems with silver-filled epoxy when used to bond gold-plated, 0.016 in. x 0.018 in., nickel block to a gold-plated nickel header

* The work function of a material is the minimum amount of energy that, when supplied to an electron, will effect the emission of an electron from the material.

Figure 1. Epoxy Die Attach Section - SEM Photograph

TABLE 1. CONTACT INTERFACES FOR SILVER-FILLED EPOXY ATTACHED GOLD-BACKED SEMICONDUCTOR

| |
|---|
| SEMICONDUCTOR |
| \| |
| GOLD (Chip Backing) |
| \| |
| SILVER |
| \| |
| SILVER |
| \| |
| GOLD (Substrate) |

even after 10,000 hours at 150°C. In fact, a decrease in resistance was noted. However, when they performed the same storage test on the same size gold-backed silicon samples, a 67-percent reduction in shear strength was experienced. Failure analysis revealed chip separation at the adhesive bond line. It is conjectured that if these silicon samples had been used for the electrical test, an increase in resistance would have resulted.

Similar mechanical shear strength versus thermal aging tests were performed by Mitchell and Berg [7] except that aluminum strips were used rather than semiconductor to metal. They showed that the adhesive strength of bonded joints falls rapidly at temperatures above 100°C, indicating that relatively small applied stresses at high temperature could degrade the bond integrity. Mitchell and Berg did not experience any significant decrease in strength after 150°C storage.

The bulk resistivity of the epoxy has been evaluated by several authors [6,7,10] and has been found in almost all cases to meet the vendors' data sheet specifications even after extended storage. Svitak and Williams [6] showed that only at temperatures approaching 300°C did the bulk resistance behave erratically.

An equation for voltage drop as a function of current density for the epoxy was derived as follows:

$$R = \frac{R_s L}{A}$$

where

R = resistance

$R_s$ = resistivity

L = length

A = area

and V = IR

$$V = \frac{I}{A} \times RA = \frac{I}{A} \times R_s L$$

Plots were made of voltage drop V versus current density with the resistivity times the epoxy thickness ($R_s L$) held constant. Figures 2 and 3 represent these plots for epoxy A and epoxy B, respectively. The resistivities were determined using a glass slide onto which two strips of adhesive tape are placed 0.1 inch apart. Epoxy is applied between these two strips and leveled using a razor blade. The tape is removed and the epoxy cured at 150°C for one hour. The resistance is then measured by using a four-point probe method with a one-inch spacing. Based on this, the resistivity of epoxy A was determined to be 0.0002 Ω-cm and epoxy B was determined to be 0.0005 Ω-cm. It can be seen that the voltage drop contribution of the epoxy is less than a millivolt for even the highest current density and largest seam thickness.

Eisenmann and Halyard [3] suggest the fluctuating contact resistance observed in epoxy attached devices results from differences in the thermal expansion rate of the epoxy resin and filler. They suggest that this problem will be observed at current densities on the order of 300 to 400 A/in.$^2$. This theory is refuted, I think, by percolation theory*[8]. The volume per-

* Percolation theory predicts a critical percent by volume of conductor within an insulating matrix below which the probability of conduction is zero.

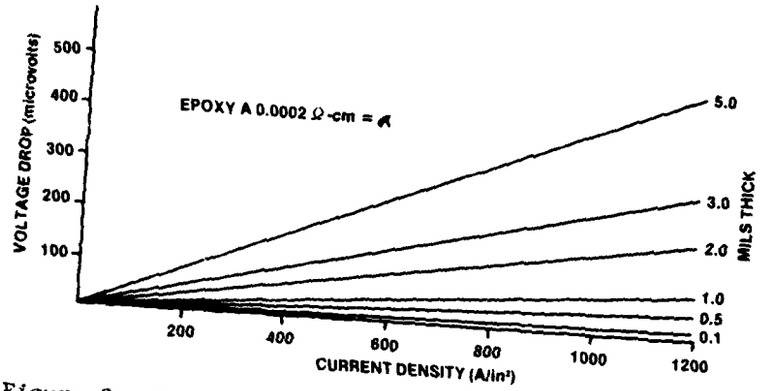


Figure 2. Epoxy Voltage Drop versus Current Density

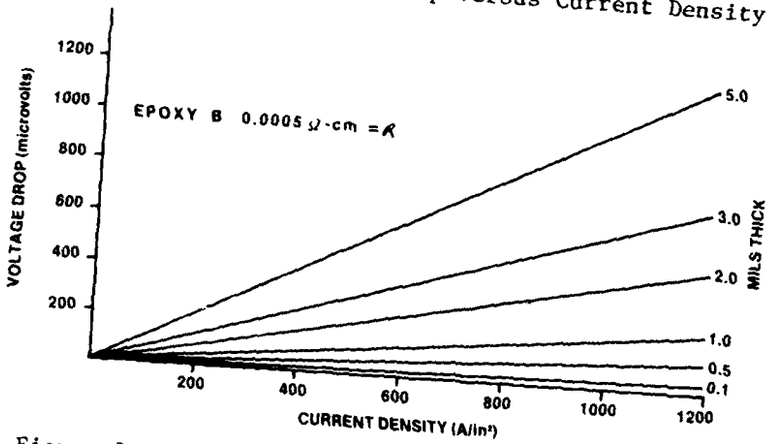


Figure 3. Epoxy Voltage Drop versus Current Density

cent of conductor in epoxy required to initiate conduction has generally been reported as a minimum of 20 to 30 percent, with a dependence of particle size and surface area. Smaller size and large relative surface areas give the lowest resistances. Since the expansion and contraction of the epoxy resin is not large enough to appreciably affect the percent volume of conductor, it does not seem reasonable that this would cause significant resistance fluctuations.

Lovinger [9] has shown that the reason for nonconduction of epoxy filled with V9 silver is that the epoxy is coated with a fatty acid salt of copper to promote dispersion. Temperatures of 100°C and greater cause the removal of this organic insulator by decarboxylation, followed by vaporization of the parent hydrocarbons. One could infer from this that if the epoxy could be cured at room temperature, it would be nonconductive.

Based on this background, die backside metalization appears to affect the contact resistance, the bulk resistivity of the epoxy appears to be more than

adequate, and no data could be found on the effects of substrate gold and die size. Three experiments were conducted.

## EXPERIMENTAL

In order to evaluate the effects of gold backing, a special test vehicle was devised using silicon wafers and a diode mask set. However, instead of diffusing a p-type anode as would be done if one were creating a diode, an $N^+$ region was diffused, as would be done for the emitter of an NPN transistor. Aluminum was then deposited and alloyed for the top contact. The resulting test sample is shown in Figure 4.

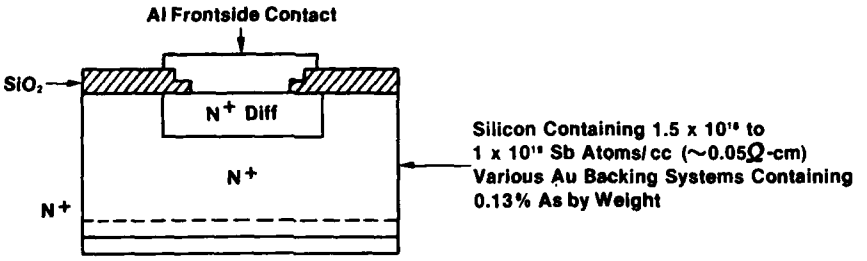


Figure 4. Semiconductor Test Vehicle

The back contact for each of two wafers was then prepared in the following five ways, following an HF etch:

1) No gold
2) Gold vacuum deposited but not alloyed
3) Gold vacuum deposited and properly alloyed
4) Gold vacuum deposited and heavily alloyed (fast withdrawal from sintering oven)
5) NiCr, Ni, Au vacuum deposited but not alloyed

These substrates were then scribed and broken into 0.016 in. square dice.

### EXPERIMENT No. 1

As the test vehicle, a thin-film substrate (Figure 5) was used to attach 120 dice divided into 12 columns of 10 dice each, connected in series. On each substrate, six columns were attached using epoxy A, 70% by weight, silver-filled conductive epoxy, and six columns were eutectically attached using a gold-germanium preform. (Eutectic attach was completed prior to epoxy attach.)

Ten test circuits were fabricated in this manner. Cure schedules for the epoxy were as follows:

| Number of Circuits | Time | Temperature | Circuit Numbers |
|---|---|---|---|
| 2 | 1 hr | 150°C | 1, 2 |
| 2 | 1/2 hr | 150°C | 3, 4 |
| 2 | 1 hr | 125°C | 5, 6 |
| 2 | 1/2 hr | 175°C | 7, 8 |
| 2 | 1/2 hr | 200°C | 9, 10 |

Also, one circuit was fabricated using a eutectic attach with no preform and one circuit was fabricated using a eutectic attach with a gold-germanium-arsenic preform.

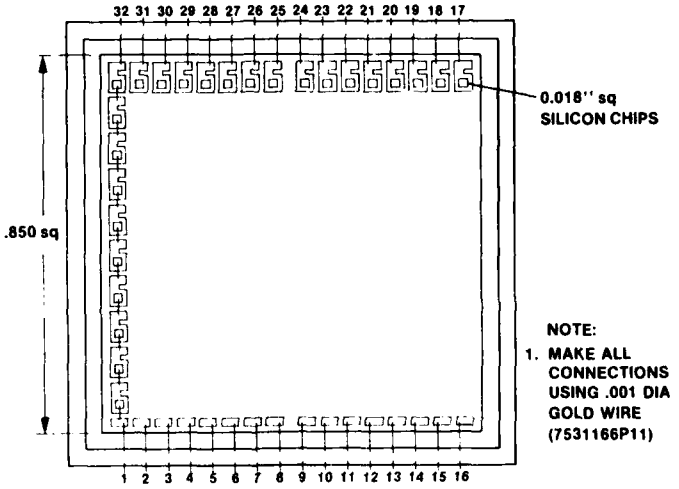


Figure 5. Epoxy Die Attach Process Test Pattern

The following is a breakdown by column of the die gold backing and attach method:

| Column Number | Description of Die Backing | Attach Method |
|---|---|---|
| 1 | Plain Silicon, No Gold | Eutectic |
| 2 | Arsenic-Gold, No Alloying | Eutectic |
| 3 | Arsenic-Gold, Proper Alloying | Eutectic |
| 4 | Arsenic-Gold, Overalloyed | Eutectic |
| 5 | NiCr-Ni-Au, No Alloying | Eutectic |
| 6 | Gold-Plated Kovar | Eutectic |
| 7 | Plain Silicon, No Gold | Epoxy |

| Column Number | Description of Die Backing | Attach Method |
|---|---|---|
| 8 | Arsenic-Gold, No Alloying | Epoxy |
| 9 | Arsenic-Gold, Proper Alloying | Epoxy |
| 10 | Arsenic-Gold, Overalloyed | Epoxy |
| 11 | NiCr-Ni-Au, No Alloying | Epoxy |
| 12 | Gold-Plated Kovar | Epoxy |

Silicon contained $1.5 \times 10^{18}$ to $1 \times 10^{19}$ Sb atoms/cc
Gold backing contained 0.13% As by weight

The test sequence is depicted in Figure 6.

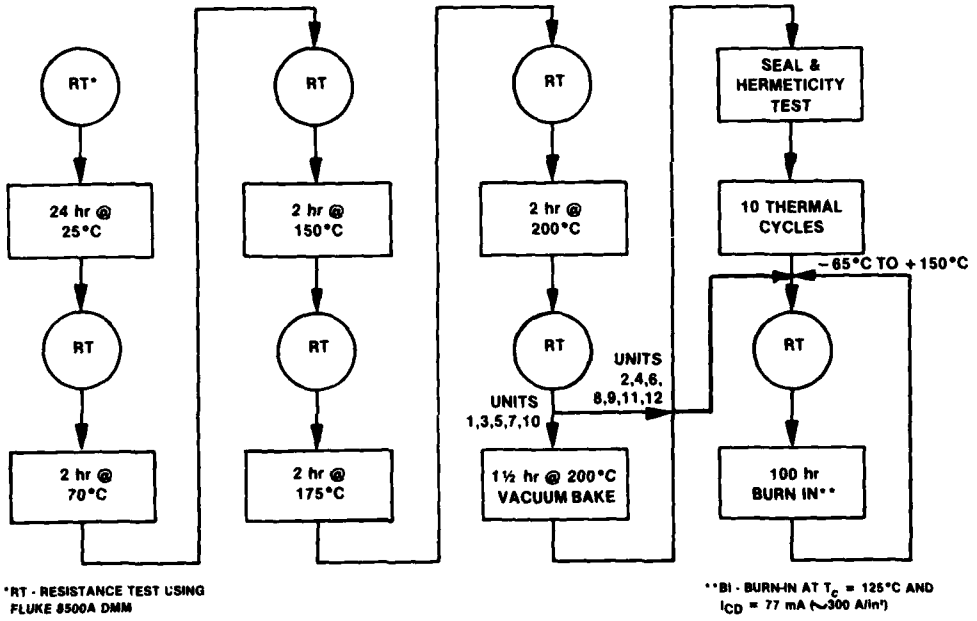


Figure 6. Experiment No. 1 Test Sequence

EXPERIMENT No. 2

One thick-film and one thin-film circuit were fabricated using all properly sintered dice. The configuration was the same as the previous experiment with six columns of properly sintered dice attached with epoxy A and six columns of properly sintered dice attached eutectically (no preform was used). The epoxy cure was one hour at 150°C. The eutectic attach was completed prior to the epoxy attach. Both circuits were subjected to the test sequence shown in Figure 7.

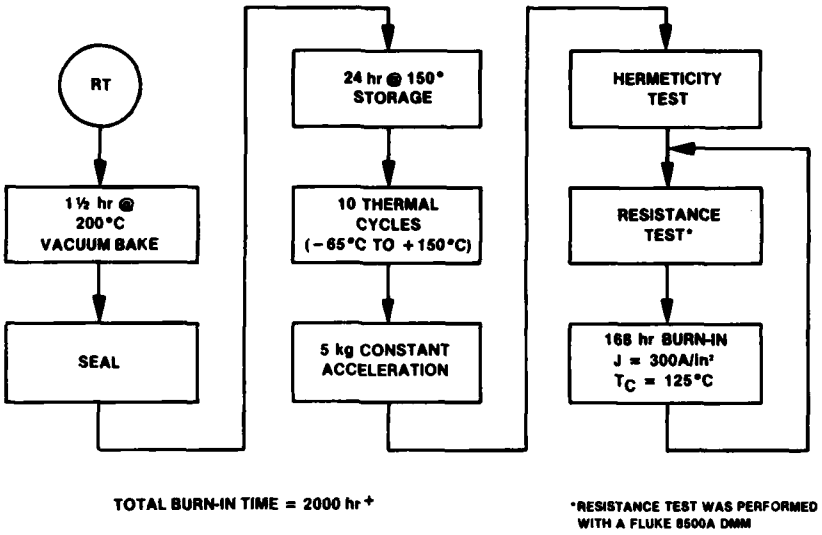


Figure 7. Experiment No. 2 Test Sequence

EXPERIMENT No. 3

This experiment was designed to evaluate the electrical resistance contribution of conductive epoxy to the collector circuit of larger power transistors. The transistors evaluated were 0.120 inch square NPNs with properly sintered gold backing. Ten each of these dice were attached to a thin-film substrate using two adhesives - epoxy A and epoxy B. Both epoxy based adhesives were cured for one hour at 150°C. The screening sequence is given in Figure 8. The forward voltage drop of the base-collector diode was measured at a current of 250 mA on a Tektronix 576 Curve Tracer in accordance with the test method recommended by Barton and Harriot [10].

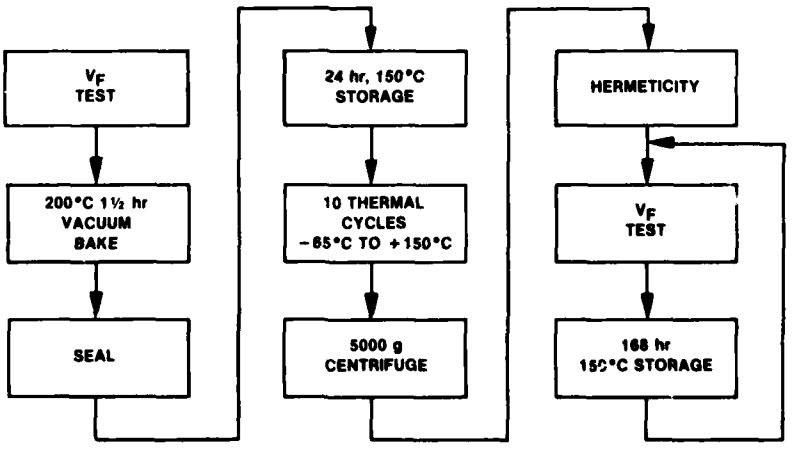


Figure 8. Power Transistor Test Sequence

## DISCUSSION OF RESULTS

### EXPERIMENT No. 1

The intent of this experiment was to determine the effect of semiconductor metalization backing system on the electrical resistance of the epoxy die attach. The final resistance measurements of all samples are given in Table 2. A one-gram nondestructive wire bond pull test was performed and all lifted wires were replaced prior to these readings. An analysis of the results for each die backing system follows.

#### Silicon, No Gold Backing

When attached with silver-filled epoxy, these units exhibited a nonlinear I-V (current-voltage) characteristic immediately after die attach (see Figure 9). There was no noticeable effect on this contact resistance due to high temperature exposure or life test. The units which were exposed to seal and thermal cycle did exhibit a quivering I-V curve in the forward breakdown region after life test. It is not known when the quivering curve first appeared. A typical I-V characteristic curve is shown in Figure 9. It is believed that this nonlinear I-V curve is a result of a metal-semiconductor rectifying contact as outlined in the Background section of this paper. It must be noted that similar rectifying contacts (these contacts had a lower $I_S$ compared to epoxy) were achieved even with eutectic attaches unless an arsenic doped gold-germanium preform was used.

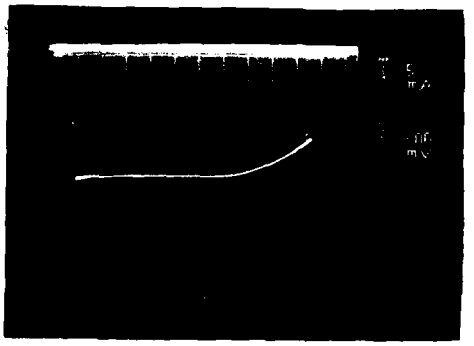

Figure 9. I-V Curve for Non-Gold-Backed Die Silver-Filled Epoxy Attach

#### Unsintered - Doped Gold Backing

These samples exhibited some very unusual characteristics when attached with silver-filled epoxy. All of the samples cured at 150°C and below exhibited nonlinear I-V characteristics similar to those of the non-gold-backed case except with lower $I_S$. However, samples cured at 175°C exhibited about half the resistance of samples cured at 150°C and samples cured at 200°C appeared nearly ohmic initially. After the 175°C and 200°C two-hour exposures of the test sequences, all of these samples appeared nearly ohmic.

TABLE 2. FINAL RESISTANCE MEASUREMENTS* (ohms)

| Seal/Thermal Cycle | | | Yes | No | Yes | No | Yes | No | Yes | No | No | Yes | No | No |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Eutectic Preform | | | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | Au-Ge | None | As-Au-Ge |
| Epoxy Cure (°C/hr) | | | 150/1 | 150/1 | 150/½ | 150/½ | 125/1 | 125/1 | 175/½ | 175/½ | 200/½ | 200/½ | 150/1 | |
| Unit Number | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| Backing | Attach | Col. No. | | | | | | | | | | | | |
| Si | U | 1 | 251 | 379 | 210 | 242 | 205 | 172 | 268 | 223 | 400 | 207 | 586 | 6.6 |
| | P | 7 | 840K | 600K | 780K | 815K | 400K | 760K | 700K | 790K | 1M | 70K | 700K | - |
| Au Not Sintered | U | 2 | 25 | 26 | 10 | 13 | 12 | 12 | 20 | 17 | 13 | 21 | 7 | 7.9 |
| | P | 8 | 60K | 180K | 200K | 100K | 100K | 300K | 100K | 80K | 100K | 100K | 200K | - |
| Au Properly Sintered | U | 3 | 36 | 93 | 55 | 23 | 18 | 121 | 81 | 41 | 65 | 73 | 8 | 8.1 |
| | P | 9 | 10 | 10 | 37 | 8 | 8 | 9 | 10 | 9 | 9 | 9 | 10 | - |
| Au Over-sintered | U | 4 | 41 | 121 | 64 | 67 | 31 | 53 | 86 | 120 | 27 | 41 | 18 | 6.8 |
| | P | 10 | 49 | 8 | 40 | 8 | 73 | 8 | 90 | 8 | 8 | 37 | 8 | - |
| NiCr-Ni-Au | U | 5 | 24 | 56 | 30 | 29 | 23 | 39 | 85 | 21 | 26 | 40 | 1.3K | 7.2 |
| | P | 11 | 10K | 7K | 10K | 6K | 371 | 10K | 6K | 8K | 10K | 10K | 6K | - |
| Au Plated Kovar | U | 6 | 0.7 | 0.7 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | - | 1.1 |
| | P | 12 | 0.9 | 0.7 | 0.8 | 0.9 | 0.9 | 1.4 | 0.9 | 0.8 | 0.8 | 0.8 | 0.9 | - |

Note: U- Eutectic
P - Epoxy

* All wires were prestressed at 1 gm and all defective wire bonds were replaced. Resistance measured using Fluke 8500A DMM

All of the unsintered - doped gold backing samples which were epoxy attached reverted to a high resistance state during the life test. Figure 10 depicts these results graphically for the 150°C one-hour cure and the 200°C half-hour cure. The initial nonlinear I-V characteristic for those samples cured at 150°C and below is thought to be due to the metal semiconductor rectifying contact identified earlier. The fact that a 200°C exposure causes this contact to become ohmic may be due to some microsintering at the gold-silicon junction which is reversed by the application of an electrical bias at elevated temperature. Figure 11 depicts the range of I-V characteristics for these samples after life test.

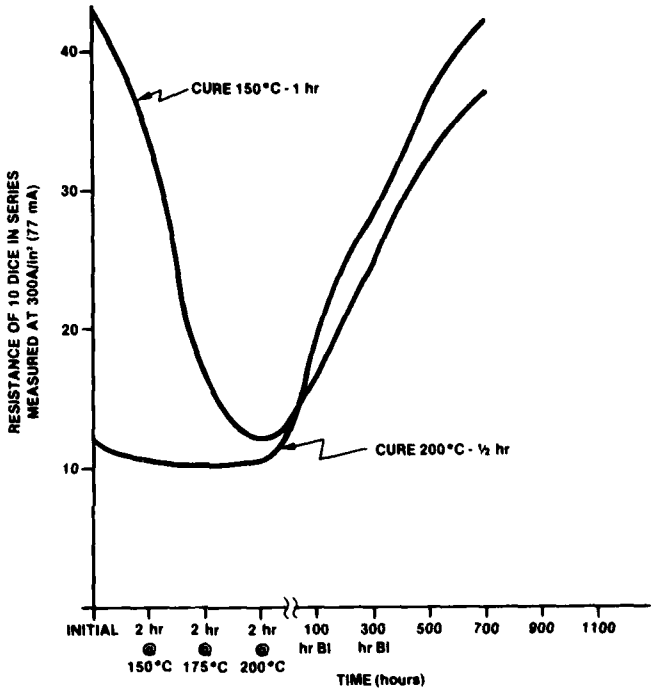


Figure 10. Unsintered Samples - Resistance at 77 mA vs Exposure

Figure 11. I-V Characteristics of Unsintered Gold-Backed Silicon Die with Silver-Filled Epoxy Attach

Again the eutectic attach with Au-Ge preform produced unsatisfactory results. Only with a eutectic attach using no preform or using an arsenic-doped Au-Ge preform were the results satisfactory.

Properly Sintered Gold Backing

All of these samples produced reliable low resistance ohmic contacts (see Figure 12) when epoxy attached except for one. This failure upon analysis was determined to be due to one die of the 110 samples. Its resistance was approximately 30 ohms and was sensitive to probe pressure. The first increase in resistance in this die was noted after approximately 700 hours of life test. The I-V characteristic was nearly linear and showed some jitter on the curve tracer. It is believed that the most likely cause of this failure was a loss of adhesion between the epoxy and the chip but unfortunately the sample was destroyed during a potting and sectioning step prior to a scanning electron microscope (SEM) analysis.

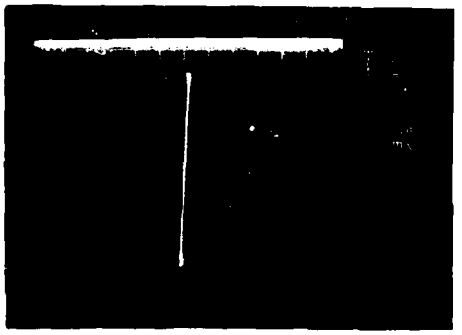

Figure 12. I-V Characteristic for Properly Sintered Gold-Backed Die with Silver-Filled Epoxy Attach

An estimate of the effective resistivity may be obtained by assuming an average bond seam thickness and assuming that the eutectically attached die either without preform or with the arsenic-doped preform represents the resistance of the die and gold runs. The average bond line thickness was estimated to be 0.0001 inch based on SEM photographs such as Figure 13.

$$R_s = \frac{RA}{L} = \frac{1.2\Omega \times (0.016 \text{ in.})^2 \times 2.54 \text{ cm}}{0.0001 \text{ in.} \times 10 \text{ dice in.}} = 0.780 \ \Omega\text{-cm}$$

The reason for this value being so much higher than the vendor's published 0.0001 Ω-cm value is not clear. Although it was observed that the silver-filler density was lower in the bond seam than in the fillet around the chip, this was not a great enough difference to explain the higher resistivity. Therefore, it is assumed that interface resistances account for this difference.

Again, the eutectic die attach did not produce acceptable results when the Au-Ge preform was used but low resistance ohmic contacts were obtained with no preform and with the arsenic-doped preform.

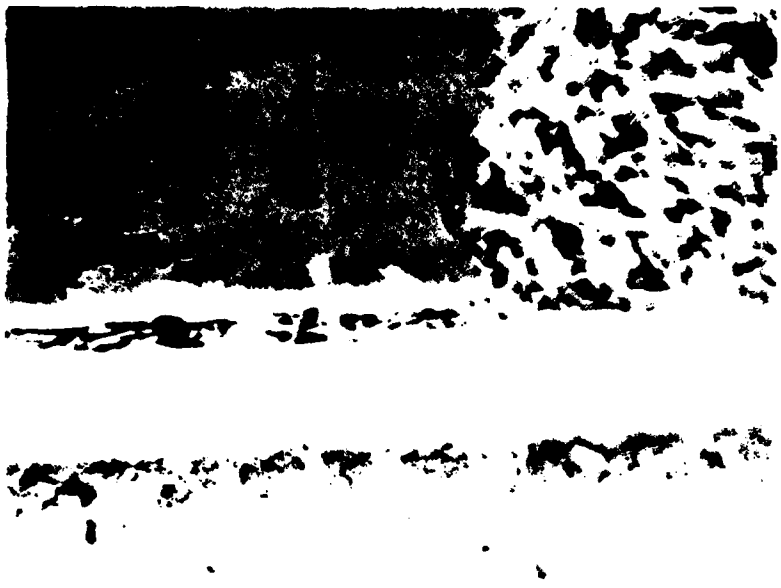

Figure 13. Section of Epoxy Attached 0.016-inch Square Die

Heavily Sintered Gold Backing

The results with epoxy attach again were very interesting. All of the samples which were sealed and subjected to thermal cycle developed higher than expected resistance for the ten series connected dice while the samples which were not sealed and subjected to thermal cycle maintained low resistance ohmic contacts. A plot of the average resistance of these samples vs. time is shown in Figure 14. The pattern for the failed samples was an initial increase of 2 to 3 ohms followed by quivering scope trace of 20 to 30 ohms, and finally a distinct 20 to 50 ohm increase.

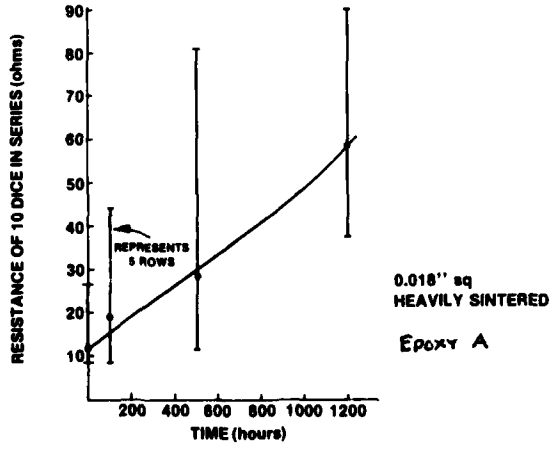


Figure 14. Die Resistance of Ten Dice in Series vs. Time

In order to analyze the failures, unit No. 10 had its cover removed and each chip in row 10 was probed for resistance at 10 mA. The results are shown in Figure 15. Die numbers 2, 3, and 9 exhibited high resistance. This circuit was then potted and sectioned. It can be seen from Figure 16 that the increase in resistance is due to lack of adhesion between the epoxy and the chip back side. One would expect better adhesion to these chips than the properly sintered dice due to the increased presence of silicon oxide on the die back side of the heavily sintered devices. One possible explanation is that the gold acts as a cushion for stresses. The heavily sintered parts have a much harder back surface and therefore more stress may be generated at the epoxy-chip interface.

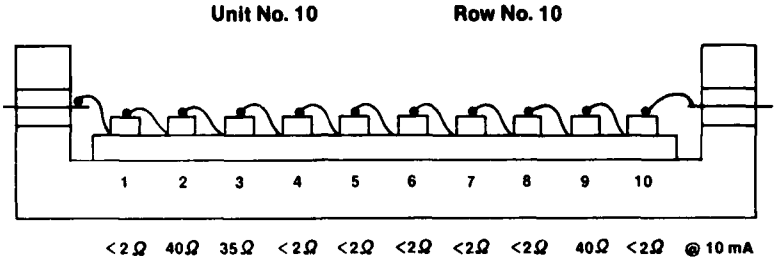


Figure 15. Heavily Sintered Die

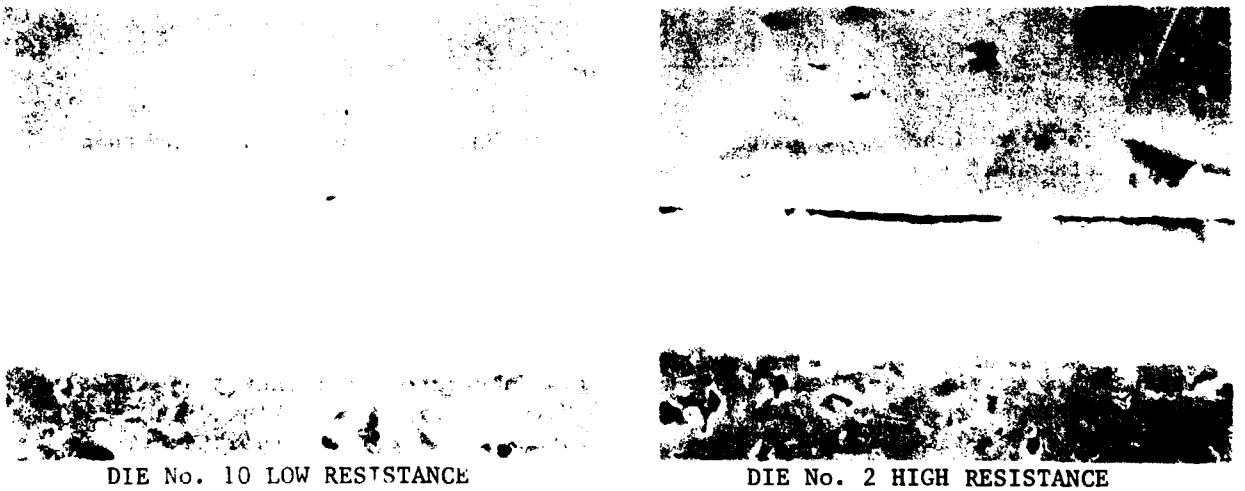


Figure 16. SEM Photos

The eutectic attach again did not produce low resistance contacts except in the case where an arsenic-doped Au-Ge preform was used.

Barrier Metal (NiCr-Ni) and Unsintered Gold

This produced results similar to the non-gold-backed devices except that $I_S$ was higher once W was lower (see Figure 17). These characteristics were not affected by the high temperature exposure, thermal cycle, or life test.

Eutectic attach with arsenic-doped gold-germanium preforms was successful. All others produced higher than desired resistances.

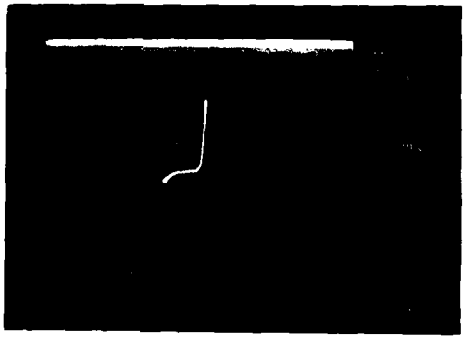

Figure 17. I-V Characteristic for NiCr-Ni-Au Backed Die Attached with Silver-Filled Epoxy

Gold-Plated Kovar

These devices produced low resistance, reliable, ohmic contacts for all attach methods. If the same method of calculating epoxy bulk resistance is employed as was used earlier, we see that the epoxy resistivity is

$$R = \frac{0.08\Omega \times 0.016 \text{ in.} \times 0.016 \text{ in.} \times 2.54 \text{ cm}}{0.0001 \text{ in.} \times 10 \qquad \text{in.}} = 0.056\ \Omega\text{-cm}$$

This is 10 to 1 better than the silicon chips but still 500 to 1 worse than the data sheet value.

Table 3 summarizes the results of Experiment 1.

EXPERIMENT No. 2

The intent of this experiment was to determine the effect of thick-film substrate metalization versus the thin-film substrate metalization used in the previous experiment. The results of this experiment are listed in Table 4. The thick-film circuit had two dice which exhibited high resistance, one in row 4 and one in row 5. These high resistance values did not appear until after the 1000-hour point.

The thin-film circuit, however, had all high resistance bonds at the end of the experiment. Some of these bonds appeared very early in the experiment. Failure analysis revealed a complete loss of adhesion. The die could easily be removed with tweezers at room temperature. Extensive resin bleedout was noted with the resin being brown in color.

It is felt that this sample received excessive heat after the epoxy attach. It is possible that a eutectic repair was attempted after the epoxy die

TABLE 3. SUMMARY OF ELECTRICAL BACK SIDE RESISTANCE AS A FUNCTION OF CHIP BACKING AND ATTACH METHOD ON 0.016 in. SQUARE N-TYPE SILICON CHIPS

| Chip Backing | Epoxy | Eutectic | Au-Ge Eutectic | Au-Ge-As Eutectic |
|---|---|---|---|---|
| Silicon Backed | Nonohmic | Nonohmic | Nonohmic | Acceptable* |
| As Doped Au Unsintered | Nonohmic | Acceptable* | $\sim 1\Omega$ | Acceptable* |
| As Doped Au Proper Sintering | Acceptable* | Acceptable* | $3 - 20\Omega$ | Acceptable* |
| As Doped Au Heavily Sintered | Acceptable* w/o Thermal Cycle 1-80 ohms with Thermal Cycle | $\sim 1\Omega$ | $3 - 20\Omega$ | Acceptable* |
| NiCr-Ni-Au Unsintered | Nonohmic | Nonohmic | $1 - 8\Omega$ | Acceptable* |
| Gold-Plated Kovar Tabs | Acceptable* | — | Acceptable* | Acceptable* |

* Average contact resistance of less than $0.3\Omega$

attach, or that an oven runaway occurred. The high resistance eutectic failures at the $2000^{+}$ hour point were due to wire bond high resistance. This further supports the overheating theory since none of the thick-film wire bonds failed. The conclusion was that the substrate metalization had negligible effect on the contact resistance.

EXPERIMENT No. 3

The intent of this experiment was to determine the effects of die size on the electrical resistance of conductive epoxy attached dice. It would be nice to say that this experiment was designed through some insight or wisdom. Unfortunately, no. Failures on the factory floor for power dice $V_{CE\ SAT}$ after burn-in provided the impetus for this experiment. The dice were checked for proper gold backing and were found acceptable. Also it was noticed that transistors with dimensions of 0.06 inch square and smaller did not have any problems but dice 0.08 inch square and larger did. A plot of the base-collector voltage versus time at $150^{\circ}C$ is given in Figure 18. It can be seen that the trend is an increase from an initial value to a maximum value after the first few hundred hours and then a decrease to a steady state value which is somewhat higher than the initial value. It was noted that a large current applied for a short period of time could correct this problem temporarily, but after a few more hours of exposure, it would reappear.

TABLE 4. NORMAL SINTERING LIFE TEST

| | | Initial | 2 hr Room | 2 hr 100°C | 250 hr 125°C | 418 hr 125°C | 686 hr 125°C | 734 hr 125°C | 754 hr 125°C | 894 hr 125°C | 1126 hr 125°C | 1846 hr 125°C | 2000+ hr 125°C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THIN FILM | | | | | | | | | | | | | |
| 1A | 1 | 7.01 | 7.39 | 7.49 | 7.10 | 7.20 | 7.25 | 7.37 | 7.29 | 7.44 | 7.5 | 7.8 | 26 |
| Eu | 2 | 8.41 | 8.81 | 8.95 | 8.57 | 8.71 | 8.77 | 8.58 | 8.56 | 8.73 | 8.87 | 10.1 | 32 |
| | 3 | 8.57 | 8.96 | 9.10 | 8.73 | 8.90 | 8.96 | 8.79 | 8.79 | 9.18 | 9.28 | 9.7 | 28 |
| | 4 | 8.01 | 8.40 | 8.58 | 8.26 | 8.35 | 8.40 | 8.25 | 8.25 | 8.60 | 8.59 | 8.8 | 27 |
| | 5 | 8.23 | 8.61 | 8.81 | 8.48 | 8.57 | 8.64 | 8.49 | 8.68 | 8.84 | 8.87 | 9.2 | 26 |
| | 6 | 8.09 | 8.48 | 8.66 | 8.32 | 8.45 | 8.48 | 8.39 | 8.38 | 8.77 | 8.78 | 9.1 | 34 |
| Ep | 7 | 9.40 | 10.0 | 11.9 | 26.2 | 36.5 | 24.8 | 11.9 | 13.4 | 50.6 | 39.0 | 27.5 | 116 |
| | 8 | 8.49 | 8.95 | 25.7 | 9.53 | 10.1 | 10.5 | 10.6 | 27.( | 14.0 | 30.1 | 23.5 | 127 |
| | 9 | 8.49 | 8.90 | 9.19 | 23.8 | 24.1 | 10.8 | 23.4 | 23.5 | 24.5 | 12.3 | 27.0 | 190 |
| | 10 | 11.25 | 10.9 | 25.4 | 23.8 | 11.4 | 12.8 | 10.9 | 28.4 | 44.5 | 37.0 | 45.5 | 121 |
| | 11 | 8.64 | 9.12 | 9.33 | 10.25 | 10.3 | 10.2 | 10.4 | 47.5 | 41.0 | 17.8 | 26.2 | 183 |
| | 12 | 8.75 | 9.16 | 12.7 | 11.22 | 11.4 | 24.7 | 24.0 | 33.3 | 48.8 | 53.8 | 37.1 | 115 |
| THICK FILM | | | | | | | | | | | | | |
| 2A | 1 | 8.80 | 8.84 | 8.94 | 8.52 | 8.56 | 8.62 | 8.57 | 8.51 | 8.61 | 8.77 | 9.18 | 10.5 |
| Ep | 2 | 8.69 | 8.73 | 8.83 | 8.44 | 8.53 | 8.57 | 8.54 | 8.57 | 8.84 | 9.38 | 10.4 | 9.77 |
| | 3 | 8.56 | 8.58 | 8.66 | 8.23 | 8.30 | 8.35 | 8.30 | 8.34 | 8.42 | 8.55 | 9.0 | 10.1 |
| | 4 | 8.69 | 8.74 | 9.09 | 8.86 | 9.66 | 9.77 | 9.64 | 8.96 | 9.23 | 24.0 | 11.3 | 12.3 |
| | 5 | 8.56 | 8.60 | 8.70 | 8.51 | 9.77 | 8.83 | 9.90 | 8.88 | 8.96 | 22.7 | 24.5 | 21.7 |
| | 6 | 8.52 | 8.55 | 8.61 | 8.22 | 8.25 | 8.31 | 8.25 | 8.26 | 8.34 | 8.49 | 9.46 | 10.4 |
| Eu | 7 | 8.22 | 8.26 | 8.30 | 7.84 | 7.58 | 7.66 | 7.70 | 7.48 | 7.77 | 7.79 | 7.82 | 8.3 |
| | 8 | 8.27 | 8.30 | 8.34 | 7.96 | 8.00 | 8.06 | 8.01 | 7.96 | 8.04 | 8.12 | 8.25 | 8.37 |
| | 9 | 8.22 | 8.26 | 8.92 | 7.88 | 7.94 | 8.01 | 7.95 | 7.91 | 7.97 | 8.05 | 8.22 | 8.36 |
| | 10 | 8.18 | 8.23 | 8.24 | 7.84 | 7.90 | 7.97 | 7.92 | 7.88 | 7.96 | 8.04 | 8.23 | 8.40 |
| | 11 | 8.38 | 8.43 | 8.44 | 8.05 | 8.10 | 8.17 | 8.12 | 8.08 | 8.16 | 8.25 | 8.42 | 8.57 |
| 8 dice | 12 | 6.92 | 6.96 | 6.96 | 6.60 | 6.64 | 6.70 | 6.65 | 6.61 | 6.68 | 6.75 | 6.88 | 6.77 |

Resistance value of 10 series vertical resistors in ohms at 300 A/in.$^2$

Eu - Eutectic Ep - Epoxy

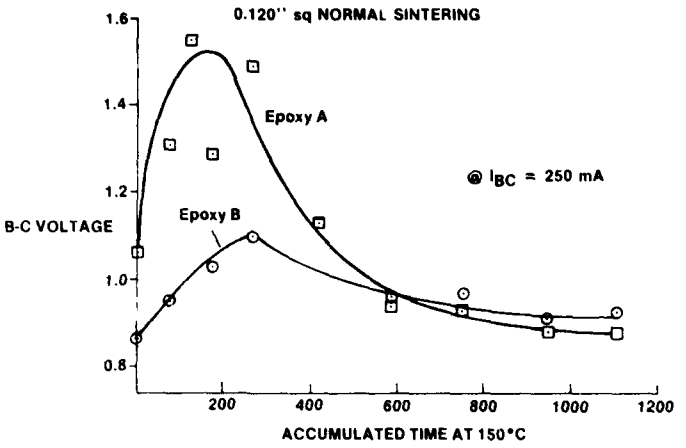


Figure 18. Average B-C Voltage for Ten Dice vs. Time

The physics of this failure mechanism is unknown. One theory which might explain this phenomenon is that the larger transistors may not allow the gases given off during cure toward the center of the epoxy bond to escape to the atmosphere. During high temperature exposure, these gases may diffuse to the surface and build up enough pressure to reduce the contact pressure and cause an increase in resistance. As time passes, these gases may then continue to diffuse until they reach the outside atmosphere, thereby reducing the pressure buildup and increasing the contact pressure, resulting in a lower resistance. This is a fairly recent development and we are continuing to evaluate it.

## SUMMARY AND CONCLUSIONS

- Properly sintered and doped gold-backed silicon dice may be reliably attached with silver-filled conductive epoxy to gold metalization on alumina substrates.

- Semiconductor dice which either have no gold backing, unsintered gold backing, or gold backing with an unsintered barrier metal between the semiconductor and gold produce nonohmic contacts when attached with silver-filled epoxy due to the metal-semiconductor rectifying junction formed at the semiconductor-junction interface.

- Semiconductor dice which have heavily sintered gold back side metalization produce a higher than expected electrical resistance when attached with silver-filled conductive epoxy if exposed to ten thermal cycles from -65°C to +150°C. This is due to a loss of cohesion between the epoxy and semiconductor back side metalization. It is theorized that the harder back surface of the heavily sintered samples produces increased stresses on the joint during thermal cycles.

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- Small gold-plated Kovar tabs produce reliable ohmic contacts when attached with silver-filled conductive epoxy to alumina substrates with gold metalization.

- Silicon transistors 0.08 inch square and larger, when attached with silver-filled conductive epoxy, exhibit an initial increase in contact resistance which peaks after a few hundred hours of high temperature exposure and then declines to a value near the initial value. This may be due to a pressure buildup of trapped gases which gradually diffuse to the atmosphere.

- Both thin-film and thick-film substrate metalization systems are acceptable for silver-filled epoxy die attach.

- A current density of 300 A/in.$^2$ did not in and of itself produce an erratic contact resistance.

These results are depicted in set theory format in Figure 19. In order to put this in proper perspective, it must be noted that none of these subsets produced acceptable results when eutectically attached using a gold-germanium preform. The acceptable subsets were limited to no sinter and proper sinter when eutectic attach without preform was used. Only the eutectic attach with a doped preform produced acceptable results for all subsets. Also, it should be noted that the problems of eutectically attached large transistors are well documented.

In summary, then, it appears that it is possible, if the previously mentioned limitations are overcome, to use silver-filled epoxy to obtain a reliable ohmic contact when attaching semiconductor devices to gold metalization patterns on alumina substrates.

The methods of overcoming these limitations are not the best, however. The large dice are in most cases eutectically attached to a gold-plated metal tab and this subassembly is then epoxy-attached to the substrate which allows the collector contact to be wired. This, although very reliable, adds to the cost. The back side metalization system is somewhat more difficult to control. This may be attempted by a statement on the component drawing to the effect that the back side metalization must be properly doped and sintered with no barrier metal present. At incoming inspection, the die may be attached back side up and scratched with a sharp instrument followed by a visual inspection. This is a fairly good method of detecting the non-gold-backed and unsintered cases but the determination between proper sintering and heavy sintering is subjective and the barrier metal case would probably go undetected.

At least two areas of further work are suggested. The first is to extend the range of the epoxy into heavily sintered and larger dice. The second is to evaluate the epoxy bonded hybrid qualification procedures in light of these results.

# Summary

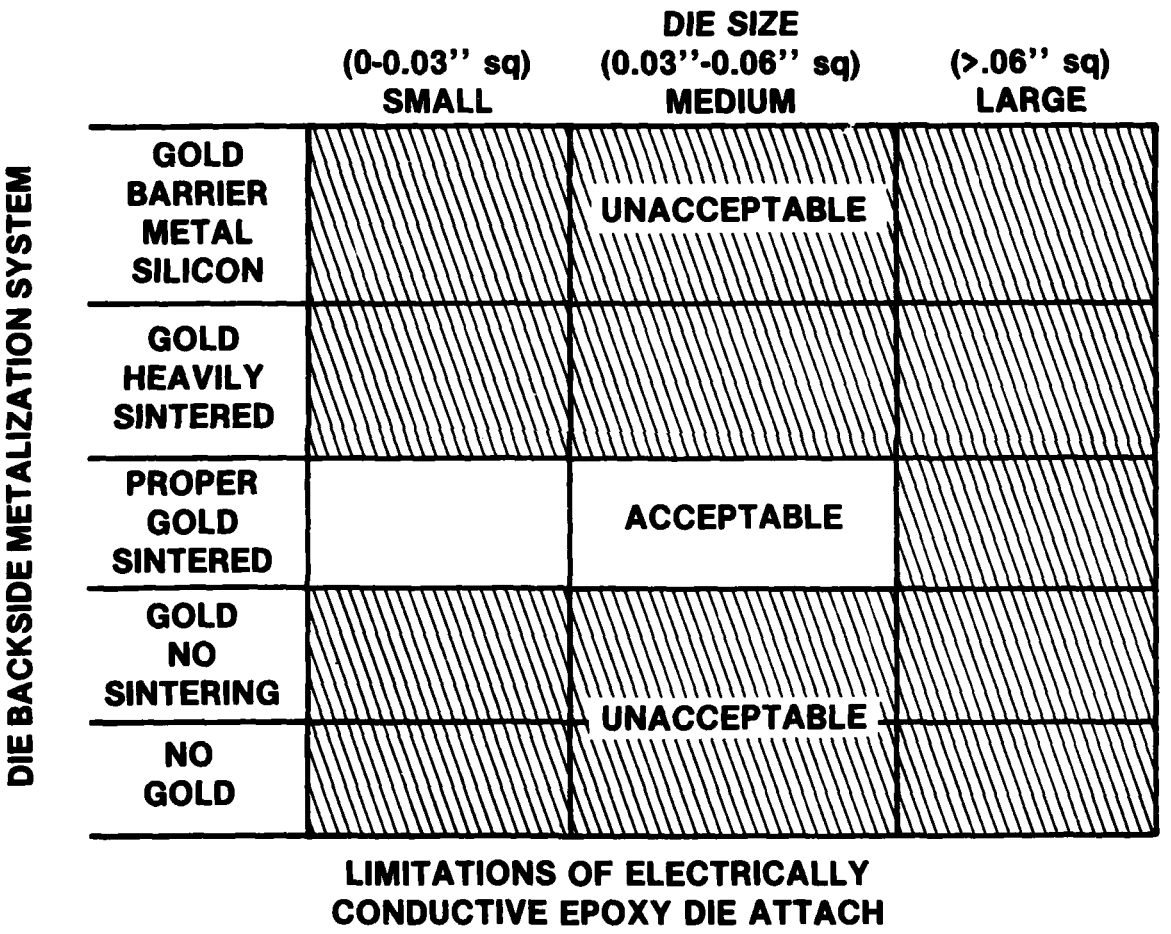


Figure 19.

## ACKNOWLEDGEMENT

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# PRELIMINARY INVESTIGATION OF POTENTIAL BERYLLIUM EXPOSURE WHILE LASER TRIMMING RESISTORS ON BERYLLIA SUBSTRATES

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## ABSTRACT

With the ever increasing use of beryllia substrates in the electronics industry, and laser trimming of resistors on these substrates, the question of potential personal exposure to beryllium must be addressed. Beryllium, when inhaled, has the potential to cause adverse health effects if exposure concentration is excessive.

This paper reports the results of a preliminary air sampling survey in the work area of an Electro Scientific Industries Model 25, YAG laser while trimming thick film resistors on beryllia. Substrates trimmed during this survey were one inch square 99.5% BeO and printed with DuPont thick film resistive materials. Numerous air samples were taken in varying proximities to the trimming site, some as close as four inches from the beam impaction point. Additional samples were taken of general air conditions and the operator's breathing zone area. The laser operator wore a personal type lapel sampler during all trimming operations. Air samples were taken during the trimming of 599 substrates. This is the equivalent of several thousand substrates when the test procedure is considered. Of all samples taken, only two showed any detectable beryllium and both of these are well below the allowable limit.

## INTRODUCTION

Beryllium oxide is a ceramic material used in electronics primarily for the combination of electrical isolation and unique thermal conductivity.

Beryllium and its compounds are a group of the many industrial materials which are potentially hazardous. However, beryllium is not a new material. It has been produced commercially for over fifty years. For thirty odd years its toxicity has been known and successfully controlled. As in any industry, the key to a good safety record depends on two factors:

Operating personnel being well informed and management ensuring that proper precautions are taken to prevent potential accidents. This paper

is intended to help you make an informed decision about Beryllia Ceramics.

## BACKGROUND

During the 1930's European literature citing cases of illness supected of being caused by beryllium went unnoticed in the United States.[1] In the early 1940's Dr. Van Ordstrand of the Cleveland Clinic reported cases of acute chemical pneumonia as a result of exposures to soluble compounds of beryllium. Dermal irritations of a less serious nature were also observed from exposure to the same soluble salt compounds.[2]

In 1946 a chronic lung disorder found among many fluorescent tube workers in Massachusetts was described in the literature by Doctors Hardy and Tabershaw.[3] Cases of acute and chronic disease continued to appear in the late 1940's. Finally, the United States Atomic Energy Commission, the principle consumer of beryllium metal became concerned and conducted studies to determine the nature and extent of beryllium toxicity and to establish industrial hygiene standards.

Out of these studies of 1949 came three recommended standards:

1. To control the acute chemical pneumonia problems, an in-plant maximum of 25 micrograms of beryllium per cubic meter of air was suggested.

2. To control the chronic disease in-plant, an average concentration of 2 micrograms of beryllium per cubic meter of air over an 8-hour day was recommended.

3. To protect the outplant population, a level of 0.01 micrograms per cubic meter of air averaged monthly was recommended for the immediate area surrounding the beryllium plant.

The first two of these recommendations was eventually adopted by the American National Standards Institute and by the American Conference of Governmental Industrial Hygienists and incorporated as a consensus standard by OSHA. The third was established as an outplant standard by the United States Environmental Protection Agency. Although the standard for acute disease and for the EPA outplant have legal status they are really only of historic significance. There has been no non-occupational case of beryllium disease as a result of exposure since the 1940's and the acute disease which is only found in beryllium producer plants has not been seen in the past decade.

The only significant concern with the toxicity of beryllium is with the chronic form of the disease, i.e., berylliosis. In this disease the thin membrane tissues of the lung wall are thickened by inflamation and impede the flow of gases between the lung and the circulatory system. The disease cannot be cured but it can be controlled. Under medical management, such as steroid medication, the patient can maintain a relatively normal regimen.

Most importantly, however, the disease is preventable.

The occurrence of berylliosis requires these factors:

1. Exposure to a sufficiently large concentration of airborne beryllium to cause an adverse effect.

2. Beryllium must be of a respirable size.

3. The exposed individual must be a hypersensitive reactor to beryllium.

Berylliosis is now accepted by medical opinion to be a disease of delayed immunological response. In layman's language, an individual must be "allergic" to beryllium to contract the disease.

Although there are no good studies of the frequency of beryllium hypersensitivity, the experience in the beryllium and fluorescent lamp industries, where large numbers of employees were massively exposed before the toxicity of beryllium was recognized, indicate only about 1% of those exposed ever came down with berylliosis.

There is no way to predetermine beryllium sensitivity. We cannot recognize the 1% so we must protect 100% of the working population.

Beryllium, beryllium alloys, and beryllia are completely safe in their solid form. *Only when each form is further processed* is there any danger of toxicity. Airborne particles in excess of about 10 microns in size do not penetrate the upper respiratory tract and enter the alveolar area of the lung.

They are filtered out by the nose hair and the cilia-mucous action of the bronchial tube, swallowed and excreted through the gastrointestinal tract without affect. In order for beryllium to cause berylliosis the particles must penetrate to the alveolar sacks of the lung. These particles (less than 10 microns in size) are invisible and their presence determined only by air sampling.

No one can say with any certainty where the divided line lies between safe and unsafe concentration of beryllium. The A.E.C. recommended levels, which have become the standards, had a safety factor but whether this factor is 10 or 100 we just don't know. What we do know is that there has never been a case of berylliosis when the exposure was at or even near the 2 micrograms per cubic meter level.

At Brush Wellman, the world's primary producer of beryllium products, we handle and re-handle tons of beryllium compounds per month. Most of these are in the particulate form, the form potentially most hazardous. Despite this difficult task we have had only one case of berylliosis among the Elmore plant workers first employed after the initial shakedown period of that plant, being around 1962. That single case was due to an equipment

malfunction in which the worker was exposed to massive quantities of powdered beryllium. We have also had one other accidental exposure at another plant which resulted in berylliosis. Thus we have had a total of two cases with exposures since 1960.

## EXPERIMENTAL PROCEDURES

This presentation will describe the results of a preliminary investigation of the potential beryllium exposure while laser trimming resistors on beryllia substrates. The trimming equipment was an Electro Scientific Industries Model 25 (Figure 1 and 2) operated in a laboratory environment. Air samples were taken in varying proximities to the trimming site. Locations are shown in Figures 3 and 4. Site samples ($S_4$ Figure 4) were taken four inches from the beam impaction point. This was the closest possible point for filter placement due to physical and operational restrictions. Additional samples were taken of the general air conditions and of the breathing zone conditions of the operator. The general air, breathing zone, and site samples were taken only while the laser trimming operation was in progress. The laser operator wore a personal type lapel sampler during all trimming operations. The lapel samples were taken over the entire trimming period and not turned off during the change of one run to the next.

The substrates trimmed during this survey were one by one inch square beryllia printed with DuPont thick film resistive materials in their image "33" pattern. (See Figure 5). Additional one by one inch beryllia substrates were coated totally on one side with the same resistive material except for a very small border at all edges (Figure 6). The solid printed substrates were used to simulate a production type operation by making sixteen (16) continuous cuts fully traversing the substrate. In this way, the cut length per unit time approximated the true situation found in industrial production shops. The Electro Scientific Industries Model 25 laser was tuned at 3 kilohertz, 1.3 watts, and a trim speed of 10 millimeters per second (0.4 inches per second). This is the normal operational setting for trimming resistors on alumina. When trimming alumina within these parameters, a kerf will be cut in the substrate approximately five (5) microns deep.

## RESULTS

Air samples were taken during the trimming of 599 substrates. This is the equivalent of approximately 2,500 substrates when taking into account that over 37% of these were of the solid printed pattern. Of all samples taken only two showed any detectable beryllium. See Table I for the results. The limit of detection is $8.0 \times 10^{-12}$ g beryllium for the "Graphite Furnace AA" method used in this study.

The two (2) detectable samples were taken at the same location ($S_3$ Figure 4) on different runs. Concentrations of these two samples were 0.04 micrograms per cubic meter and 0.30 micrograms per cubic meter. These numbers represent 2% and 15% respectively of the permissible occupational limit of 2 micrograms per cubic meter time weighted average. These samples

also represent 0.16% and 1.2% of the occupational limit of 25 micrograms per cubic meter for short term exposures of 15 minutes or less.

The detectable samples were taken at the lower right edge of the enclosing hood. At this location there exists an outward air movement of 200 feet per minute which passes over the substrate being trimmed before exiting the hood. The origin of the air is from a cooling fan in the main housing of the laser circuitry. Although the samples are very low they do show presence of some beryllium in the atmosphere of beryllium trimming operations. Wipe samples taken of these substrates before and after trimming do show a very small increase in the concentration of surface beryllium. (Table 2). Wipe samples taken of the substrate stage table used for holding substrates while laser trimming showed no detectable beryllium.

TABLE I

AIR SAMPLES

| Sample | Location | Average Microgram Be/M$^3$ |
|---|---|---|
| L.P. | Operator Lapel | N.D. |
| B.Z. | Operator Breathing Zone | N.D. |
| G.A. | General Area (6-8 ft. from laser) | N.D. |
| Site 1 | Lower Left Edge of Laser Hood | N.D. |
| Site 2 | Center of Laser Hood (at lower edge) | N.D. |
| Site 3 | Lower Right Edge of Laser Hood | 0.17 |
| Site 4 | 4 Inches Above Trimming Point on Lense Arm | N.D. |

TABLE II

WIPE SAMPLES

Average Micrograms Be/Piece

| Before | After |
|---|---|
| 0.49 | 0.58 |

Photo micrographs of laser trimmed substrates were taken to determine the geometry of the trim patterns. While trimming, the laser cuts into the alumina substrates but beryllia showed no signs of laser penetration. See Figures 6, 7, 8 and 9. Resistor stability was semi-quantitatively tested by heating to 425°C for 19 minutes. In the case of alumina substrates, this test shows resistor drift if the kerf does not penetrate the substrates.

The resistors on beryllia show stability. Although a more thorough high temperature drift study is required, the inability of the laser to cut into the beryllia under normal trim settings offers no adverse effect of stability. To determine the effectiveness of other trimmers, similar studies will have to be made.

## CONCLUSIONS

This test indicates atmospheric concentrations of beryllium in the area of laser trimming thick film resistors were well below the occupational limit with the stated laser power settings. Because of its high thermal conductivity or other properties, beryllia has the ability to resist substrate deformation at beam powers necessary to make clean kerfs in the resistive material. There is an extremely small amount of beryllia removed during laser trimming operations. In this sampling survey, there was no contamination of the surrounding area or equipment.

Preliminary high temperature resistor stability tests indicate that trimming into the substrate may not be necessary with beryllia as is the case with other substrate materials. In operations where high powered lasers are used and the potential for beryllium liberation increases, it would be advisable to use local exhaust ventilation and test for airborne beryllium.

## ACKNOWLEDGEMENT

Printing, firing and all laser trimming were performed by E. I. DuPont De Nemours & Company (Inc), Electronic Material Division. We extend our thanks for the help and counsel of Nelson Arnold and Rene E. Cote and their staff for help with this investigation.

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2. Van Ordstrand, Huhges and DeNardi, Chemical Pneumonia in Workers Extracting Beryllium Oxide, 10 Cleveland Clinic Quart. 10 (1943).

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Figure 1. E.S.I. Model 25 Y.A.G. Laser

Figure 2. Beam Arm and Monitoring Circuitry (MD. 25 E.S.I. Laser)

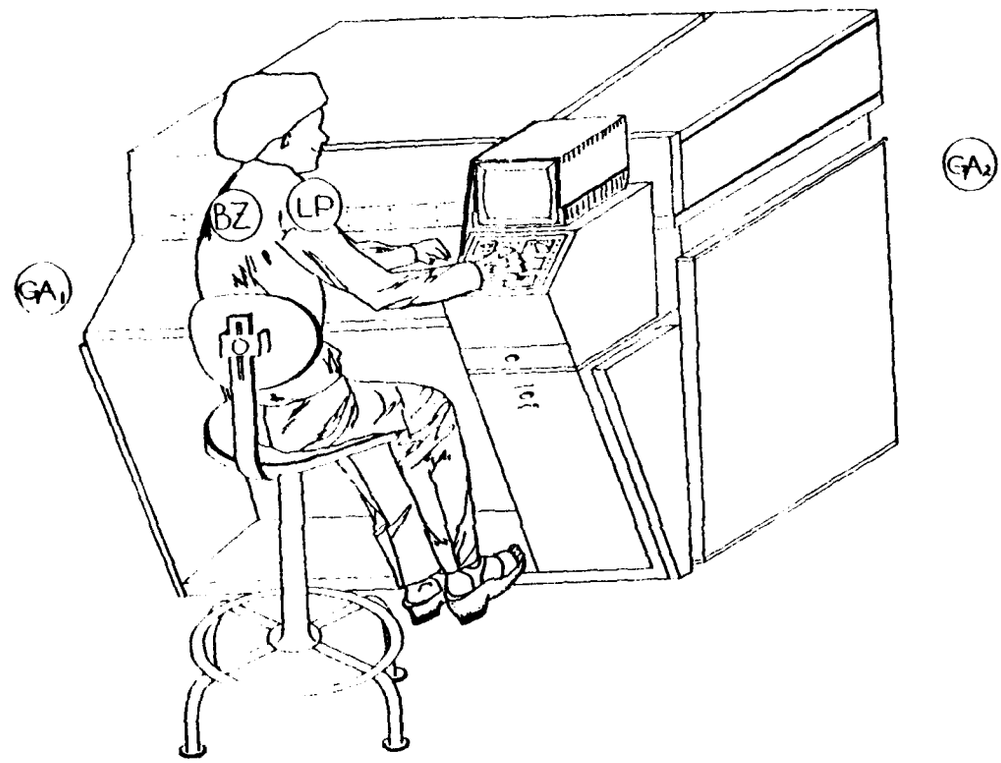



Figure 3. Sampling Locator

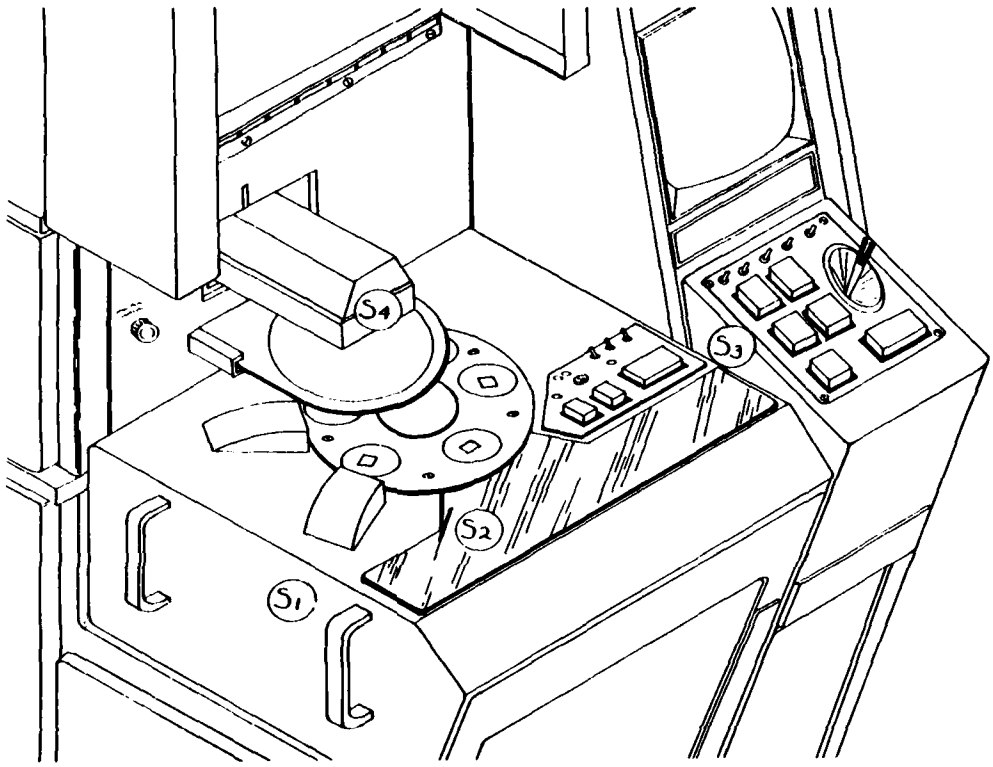
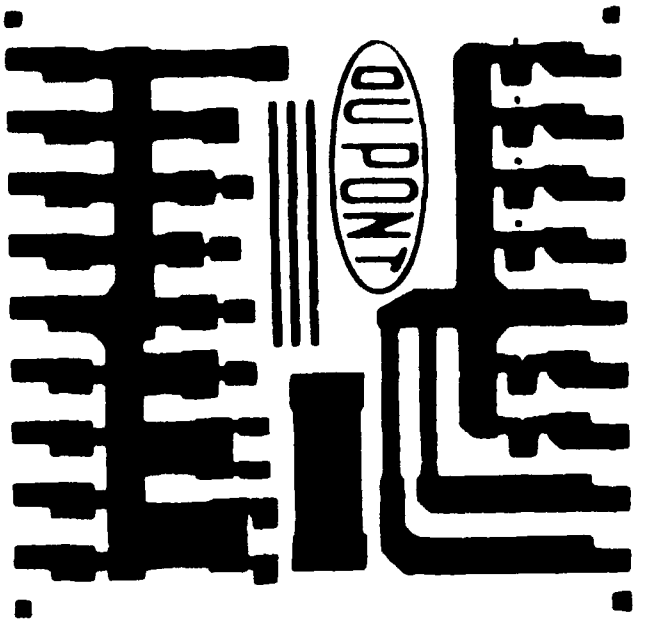



Figure 4. Sampling Locator



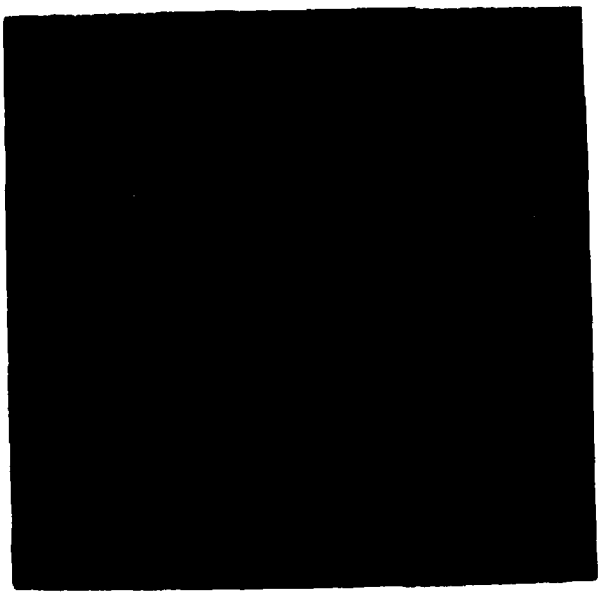



Figure 5. DuPont "33" Pattern and Solid Coated Substrate

Figure 6. Electron micrograph of BeO substrate coated with DuPont resistive material. The substrate was cut in half and stood on end to show geometry of the kerf.

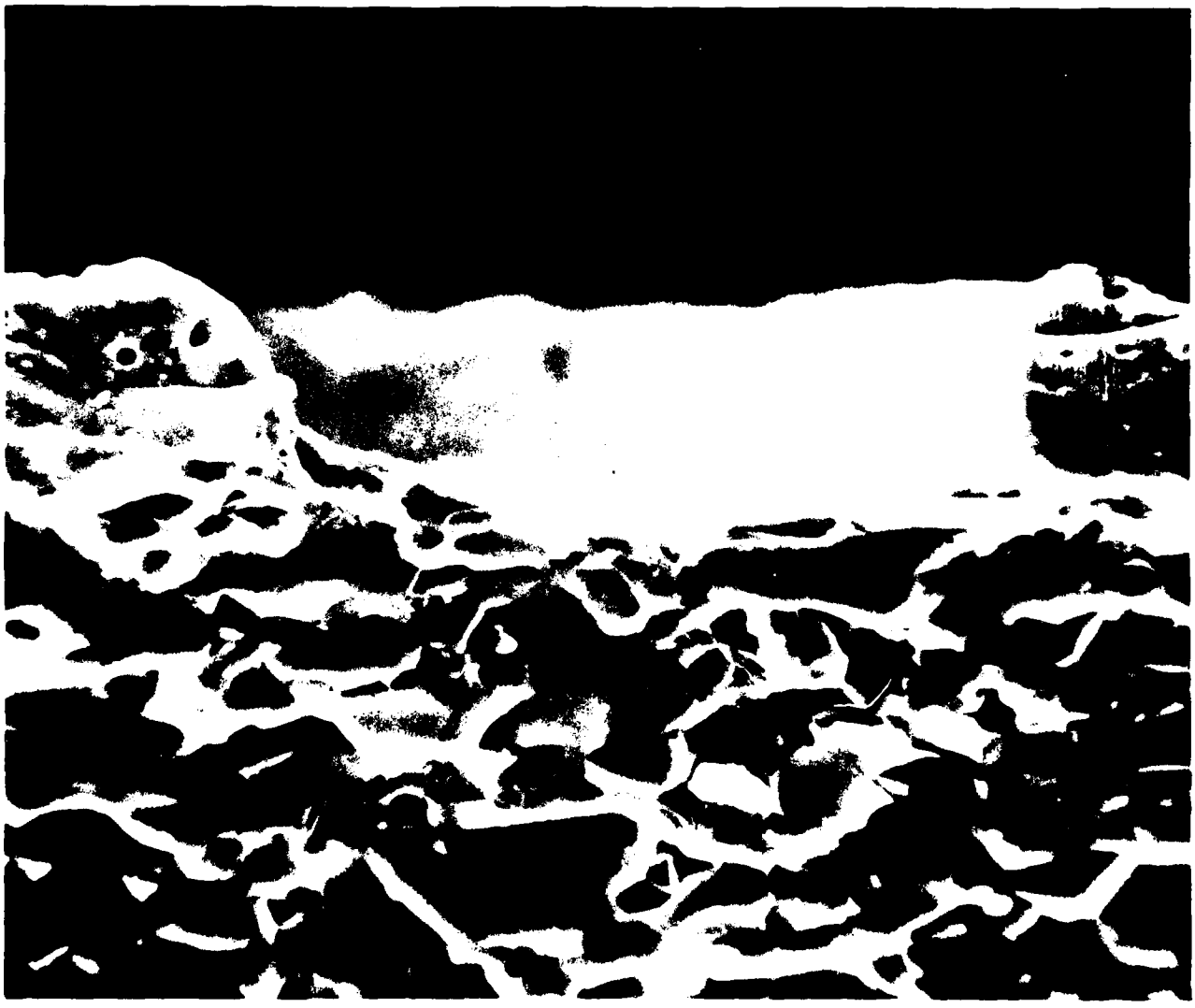


Figure 7. Electron micrograph of $AlO_x$ substrate coated with DuPont resistive material. The substrate was cut in half and stood on end to show geometry of the kerf.

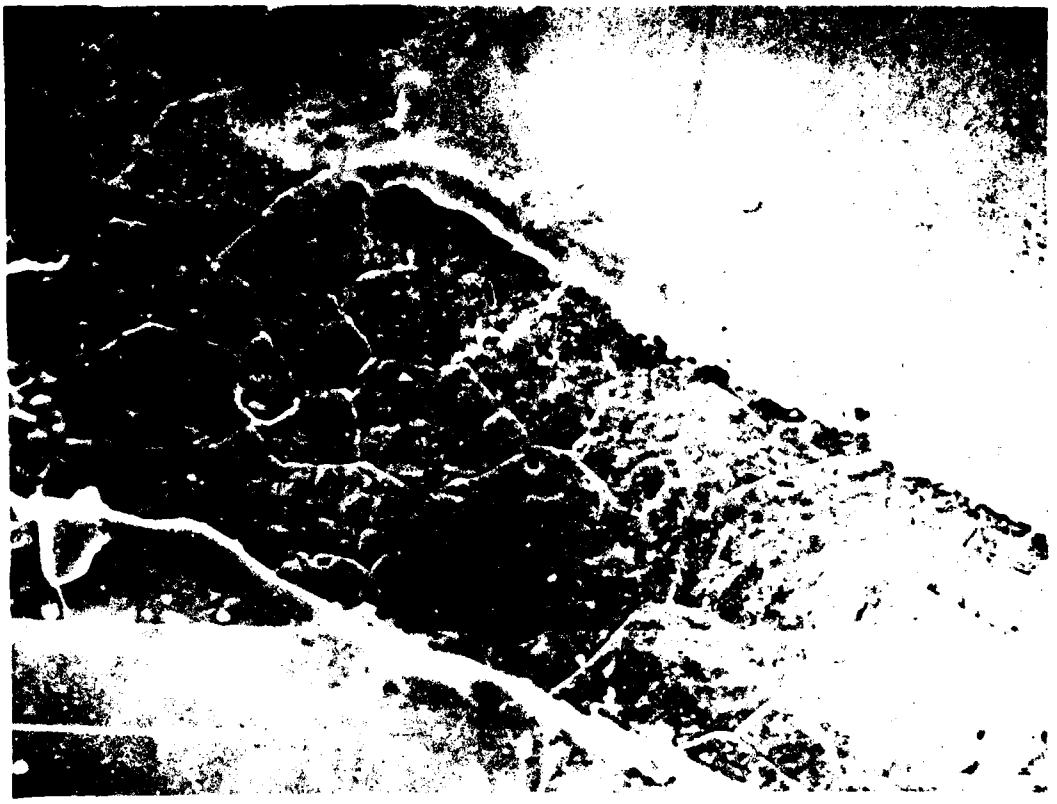


Figure 8. Electron micrograph of BeO substrate. View shows edge of resistive material at point where trimming was started or stopped.

Figure 9. Electron micrograph of $AlO_x$ substrate. View shows edge of resistive material at point where trimming was started or stopped.