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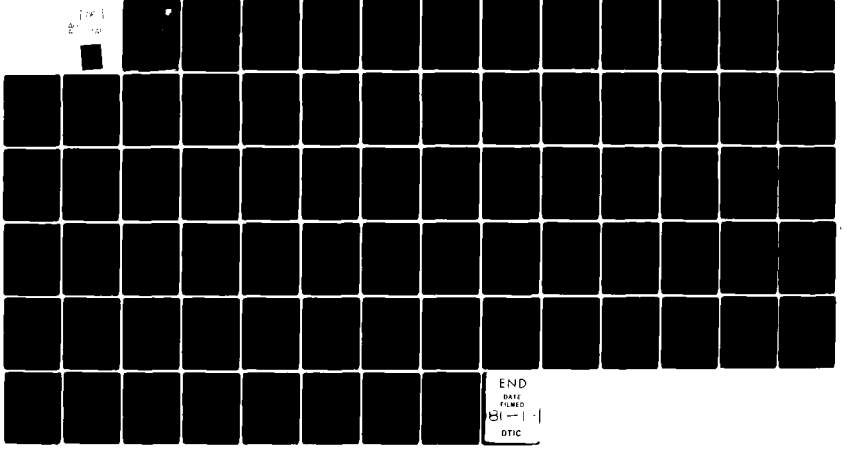

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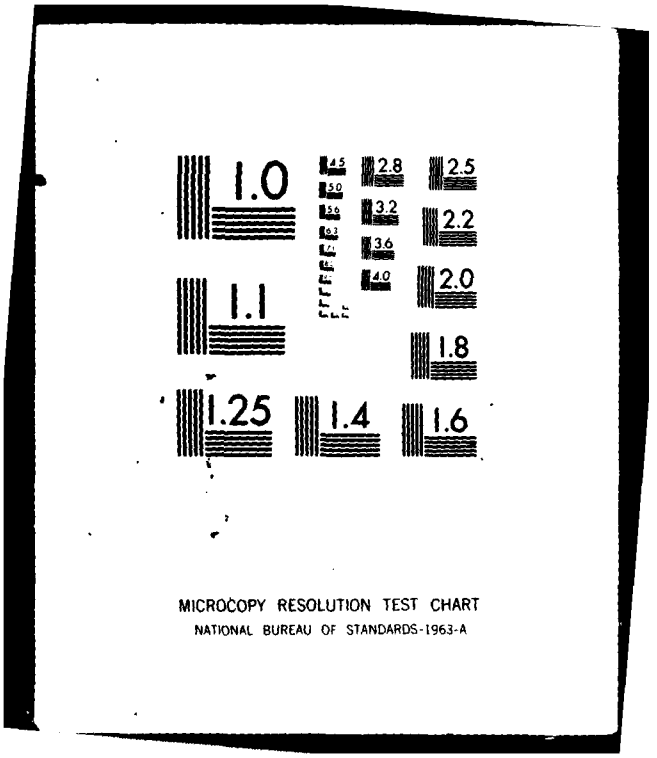

RADC-TR-80-257
Final Technical Report
August 1980

LEVEL II

PERFORMANCE DEGRADATION OF A 7400 TTL NAND GATE DUE TO SINUSOIDAL INTERFERENCE

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This effort was funded by the Laboratory Director's Fund

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The investigation reported herein addresses the problem of electromagnetic susceptibility of digital circuits. Of particular interest is the desire to obtain electromagnetic interference (EMI) performance curves for digital circuits. This report describes an effort devoted to the electromagnetic susceptibility of a single integrated circuit 7400 TTL NAND gate. The investigation was carried out by means of a computer simulation using the computer program SPICE (Simulation

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Program with Integrated Circuit Emphasis). The report concentrates on the special case of sinusoidal interference inject at various circuit nodes. Under appropriate conditions the gate voltages and currents were observed to suffer severe waveform distortion. The computer simulation revealed that the sinusoidal interference could cause the propagation delays and the rise and fall times of the output waveforms to increase significantly.

CONTENTS

1. INTRODUCTION

A typical Air Force system includes a wide variety of electronic equipments. Each equipment is likely to have several ports by which electromagnetic energy is either transmitted and/or received. Ports that generate electromagnetic energy are referred to as emitter ports while those that receive electromagnetic energy are referred to as receptor ports. Electromagnetic interference (EMI) is said to occur at a receptor port when undesired signals degrade receptor performance to an unacceptable level. The RADC Intrasystem Analysis Program (IAP) is concerned with the problem of insuring electromagnetic compatibility (EMC) between the various equipments within a system.

One of the most difficult problems associated with the IAP is specification of criteria under which undesired signals do, in fact, constitute interference to a receptor. Needed are EMI performance curves for each receptor which relate degradation in receptor performance to significant parameters of the undesired signals. Such performance curves are available for most communications, radar, and navigation receivers. However, relatively little work has been done on EMI performance curves for other types of receptors.

Of particular concern is the electromagnetic susceptibility of electronic equipments utilizing digital circuits. Recent breakthroughs in integrated circuit and microprocessor technologies have produced a rapid expansion in the use of digital circuits. Nevertheless, relatively little attention has been devoted to their electromagnetic

susceptibility. Specifically, EMI performance curves for digital circuits are unavailable. In fact, even though sophisticated digital equipments employing thousands of digital circuits are commonplace, the effect of undesired signals on even a simple logic gate is not clearly understood. Therefore, in the work reported herein, it was decided to investigate the electromagnetic susceptibility of a single integrated circuit 7400 TTL NAND gate.

The investigation was carried out by means of a computer simulation using the computer program SPICE (Simulation Program with Integrated Circuit Emphasis). Because of the small physical dimensions associated with the integrated circuit chip, it was assumed that the most probable mechanism for interfering signals to enter the NAND gate was due to electric and/or magnetic fields coupling onto the long wires attached to the chip. Consequently, interference sources were impressed on the gate's input, output, power line, and ground connections.

This report concentrates on the special case of sinusoidal interference in series with the gate output. Under appropriate conditions the gate voltages and currents were observed to suffer severe waveform distortion. This is in contrast to a previous experimental study [1], performed by McDonnell Douglas Astronautics Company, which monitored only dc voltage offsets. Our computer simulation revealed that the sinusoidal interference could cause the propagation delays and the rise and fall times of the output waveforms to increase significantly (as much as ten times in some cases). Also, instead of experiencing a simple dc offset, the output waveform can fluctuate between the

HIGH and LOW states. Large variations in the power supply current were also noted.

In order to describe the waveform distortions, it is convenient to distinguish between transient and steady-state effects. The transient effects apply to the leading and falling edges where the waveform attempts to switch from one state to another. On the other hand, the steady-state effects pertain to the periodic portion where the waveform tries to maintain a constant output. Various waveform parameters are defined in order to describe these effects. These parameters are then plotted as a function of the amplitude and frequency of the sinusoidal interferer.

2. CIRCUIT SCHEMATIC AND OPERATION OF 7400 TTL NAND GATE

The schematic diagram of the 7400 TTL NAND gate, as specified by the manufacturer, is shown in Fig. 1a. Observe that the circuit contains 5 transistors and 3 diodes. In actuality, the two input transistors T_{11} and T_{12} comprise a single dual emitter transistor with a common collector. The diagram includes the node numbers used in the SPICE simulation. Note that node 8 is the gate output.

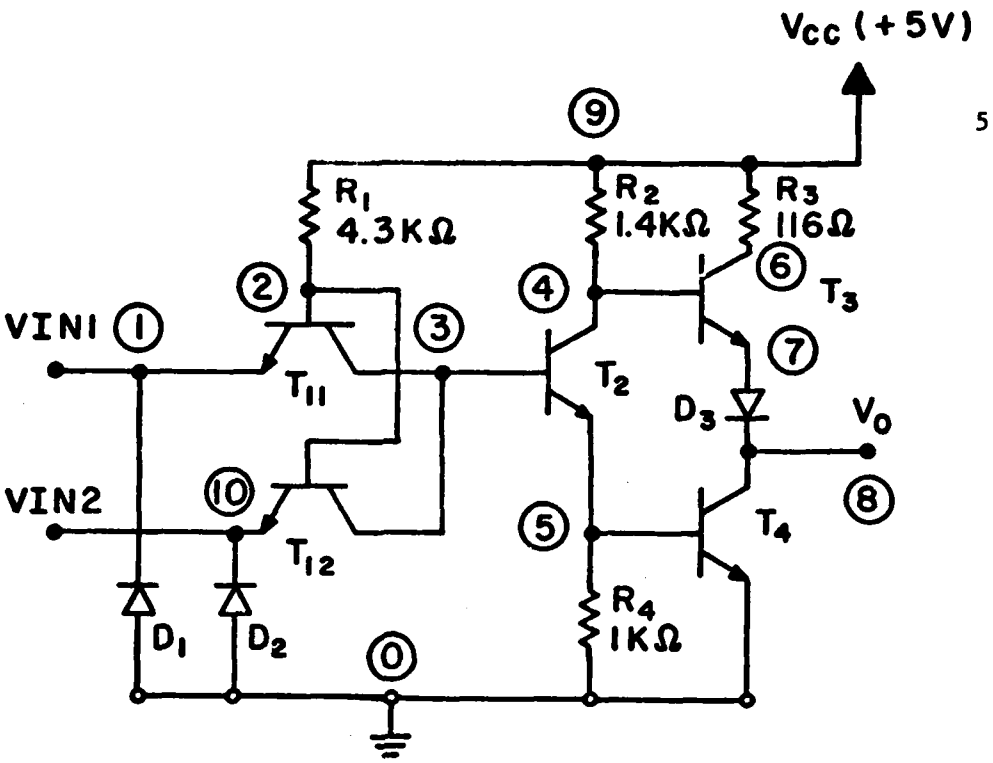
The NAND gate for the two-input case is symbolized as shown in Fig. 1b. The truth table, given in Table 1, demonstrates that the output is LOW (0) if and only if both inputs are HIGH (1).

Table 1

Truth Table for NAND Gate

VIN 1	VIN 2	V_0
0	0	1
0	1	1
1	0	1
1	1	0

According to the manufacturer, an input voltage must exceed 2 volts if it is to be interpreted as HIGH and must be below 0.8 volts if it is to be interpreted as LOW. Similarly, the output must exceed 2.4 volts if it is to be considered HIGH and must be below 0.4 volts if it is to be considered LOW. Typical values for the output voltages are 3.4 volts in the HIGH state and 0.2 volts in the LOW state. These levels are summarized in Table 2.



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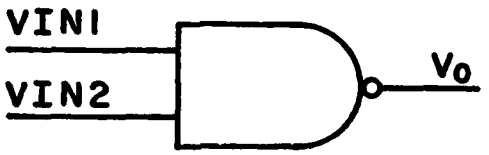


(b)

Fig. 1. a) Schematic diagram of 7400 TTL NAND gate.
b) Schematic symbol.

Table 2

Typical Voltage Levels for the NAND Gate

V_{IH}	= 2V	Min.	
V_{IL}	= 0.8V	Max.	
V_{OH}	= 2.4V	Min.	(3.4V TYP.)
V_{OL}	= 0.4V	Max.	(0.2V TYP.)

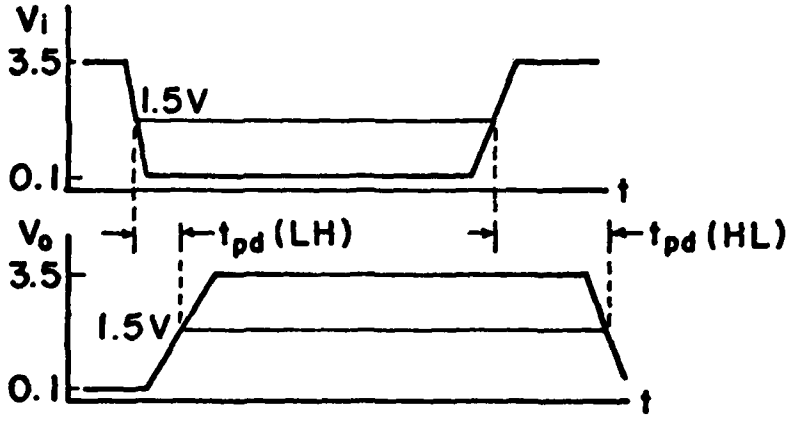
Also of use in describing typical operation of the NAND gate are the propagation delay time and the rise and fall times. Figures 2a and 2b illustrate their definitions, as taken from the manufacturer's handbook. Nominal values for t_r and t_f are 8 nanoseconds and 5 nanoseconds, respectively, while nominal values for $t_{pd}(LH)$ and $t_{pd}(HL)$ are 11 nanoseconds and 7 nanoseconds, respectively. These values are summarized in Table 3.

Table 3

Typical Values for Rise, Fall, and Propagation Delay Times

t_r	= 8 nS
t_f	= 5 nS
$t_{pd}(LH)$	= 11 nS
$t_{pd}(HL)$	= 7 nS

As an example of the type of information supplied by the manufacturer, two manufacturer's data sheets with typical electrical and switching characteristics are shown in Figures 3 and 4. In Figure 3, the column which pertains to the 7400 NAND gate is labeled DM 54/74 (00, 04, 10, 20, 30) while in Figure 4 the pertinent row is labeled 00, 10.



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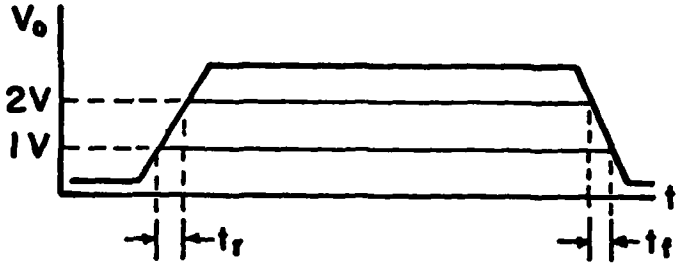


(b)

Fig. 2. a) Propagation delay time.
b) Rise and fall time.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS			DM54/74 00, 04 10, 20, 30			DM54H/74H H00, H04 H10, H20, H30			DM54L/74L L00, L04 L10, L20, L30			DM54LS/74LS LS00 LS04, LS10 LS20, LS30			DM74S S00, S04 S10 S20 S30, S133			UNITS
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.7		N.A		V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA																	V
			I_I = −12 mA				−1.5			−1.5			N.A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						400			−500			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		N/A			V
				DM74	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			N/A	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4		N/A		V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5		0.5		
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			0.1						1	mA
			V_I = 7V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			50			10							μA
			V_I = 2.7V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V										−0.18							mA
			V_I = 0.4V	LS30												−0.4				
				Others			−1.6			−2						−0.36				
			V_I = 0.5V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−40		−100	−3		−15	−30		−130			N.A	mA
				DM74	−18		−55	−40		−100	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) National Semiconductor temporarily reserves the right to ship DM54/DM74LS00, LS04, LS10, LS20, LS30 devices which have a minimum I_{OS} = 6.0 mA.

Fig. 3. Typical electrical characteristics supplied by manufacturer.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
00, 10	C_L = 15 pF, R_L = 400Ω		11	22		7	15
04, 20			12	22		8	15
30			13	22		8	15
H00	C_L = 25 pF, R_L = 280Ω		5.9	10		6.2	10
H04			6	10		6.5	10
H10			5.9	10		6.3	10
H20			6	10		7	10
H30			6.8	10		8.9	12
L00, L04 L10, L20	C_L = 50 pF, R_L = 4 kΩ		35	60		31	60
L30			35	60		70	100
LS00, LS04 LS10, LS20	C_L = 15 pF, R_L = 2 kΩ		9	15		10	15
LS30			9	15		15	20
S00, S04	C_L = 15 pF, R_L = 280Ω	2	3	4.5	2	3	5
S10, S20	C_L = 50 pF, R_L = 280Ω		4.5	7		5	8
S30, S133	C_L = 15 pF, R_L = 280Ω	2	4	6	2	4.5	7
	C_L = 50 pF, R_L = 280Ω		5.5	8		6.5	10

Fig. 4. Typical switching characteristics supplied by manufacturer.

3. MODELING OF 7400 NAND GATE USING THE SPICE COMPUTER PROGRAM

The susceptibility of the 7400 NAND gate was investigated using the SPICE computer program in its transient mode of operation. This required a detailed circuit modeling of the 7400 NAND gate. As shown in Fig. 1a, typical resistor values are provided by the manufacturer. However, circuit models for the transistors and diodes are not supplied. Fortunately, the SPICE computer program does contain stored circuit models for both the bipolar junction transistor (BJT) and the semiconductor diode. Typical parameter values, for use in the models, are also found in the SPICE User's Manual [2].

Another source which was useful in the circuit modeling was the McDonnell Douglas study [1] previously cited. To explain the dc voltage effects which they had measured, they developed a modified transistor model. This was exercised using the SPICE computer program in its dc mode of operation. They modeled a 7400 NAND gate and listed the numerical values used for the dc parameters of the 5 transistors and 3 diodes of Fig. 1a. Note that capacitive parameters were not specified since their dc analysis required only resistive components.

Our approach was to begin with the parameter values specified by McDonnell Douglas. For those parameters not specified by McDonnell Douglas, typical values taken from the SPICE User's Manual were used. The circuit was then exercised with the SPICE program and certain parameter values were adjusted in an attempt to achieve circuit performance as close as possible to the manufacturer's specifications. This resulted in 3 parameters having values different from those of

McDonnell Douglas and 2 parameter values differing from typical SPICE values.

The SPICE transistor model is shown in Fig. 5. It is based upon the integral charge control model of Gummel and Poon. The 27 parameters required by the model are listed in Table 4 along with their typical SPICE values.*

The SPICE diode model is shown in Fig. 6. This model makes use of 11 parameters. These are listed in Table 5 along with their typical SPICE values.

Table 5

SPICE Diode Model Parameters

Symbol	Parameter Name	Units	Typical Values
I_S	Saturation current	amps	1.0E-14
r_s	Ohmic resistance	ohms	10
n	Emission coefficient	-	1.0
τ_t	Transit time	sec	0.1 nS
C_{jo}	Zero-bias junction capacitance	farad	2 pF
ϕ_B	Junction potential	volts	0.6
m	Grading coefficient	-	0.5
ϵ_g	Energy gap	eV	1.11 SI 0.69 SBD 0.67 GE
P_T	Saturation current temperature exponent	-	3.0 JN 2.0 SBD
K_f	Flicker-noise coefficient	-	0
a_f	Flicker-noise exponent	-	1

*Table 4 appears on page 12.

Table 4

SPICE BJT Model Parameters

Symbol	Parameter Name	Units	Typical Value
B_F	Ideal forward current-gain coefficient	-	100
B_R	Ideal reverse current-gain coefficient	-	0.1
I_S	Saturation current	amps	1.0E-16
r_b	Base ohmic resistance	ohms	100
r_c	Collector ohmic resistance	ohms	10
r_e	Emitter ohmic resistance	ohms	1
V_A	Forward Early voltage	volts	200
V_B	Reverse Early voltage	volts	200
I_K	Forward Knee current	amps	10mA
C_2	Forward nonideal base current coefficient	-	1000
n_{EL}	Nonideal b-e emission coefficient	-	2.0
I_{KR}	Reverse knee current	amps	100mA
C_4	Reverse nonideal base current coefficient	-	1.0
n_{CL}	Nonideal b-c emission coefficient	-	2.0
τ_F	Forward transit time	sec	0.1nS
τ_R	Reverse transit time	sec	10 nS
C_{CS}	Collector-substrate capacitance	farads	2 pF
C_{je}	Zero-bias b-e junction capacitance	farads	2 pF
e	B-E junction potential	volts	0.7
m_e	B-E junction grading coefficient	-	0.33
C_{jc}	Zero-bias b-c junction capacitance	farads	1 pF
ϕ_C	B-C junction potential	volts	0.5
m_c	B-C junction grading coefficient	-	0.33
ε_g	Energy gap	eV	1.11 SI 0.67 GE
p_T	Saturation current temperature exponent	-	
K_f	Flicker-noise coefficient	-	6.6E-16 NPN 6.3E-13 PNP
a_f	Flicker-noise exponent	-	1.0 NPN 1.5 PNP

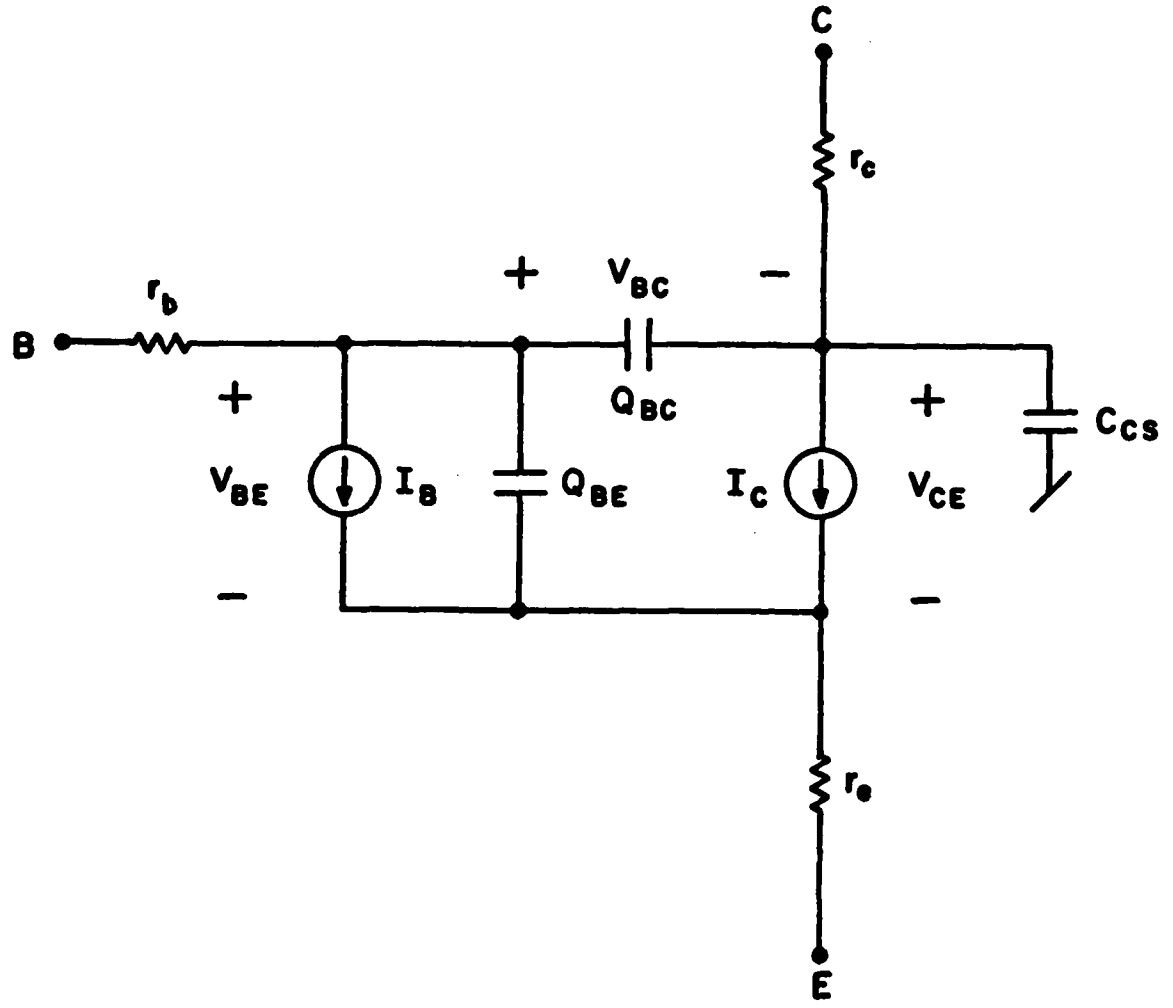


Fig. 5. The SPICE BJT Model.

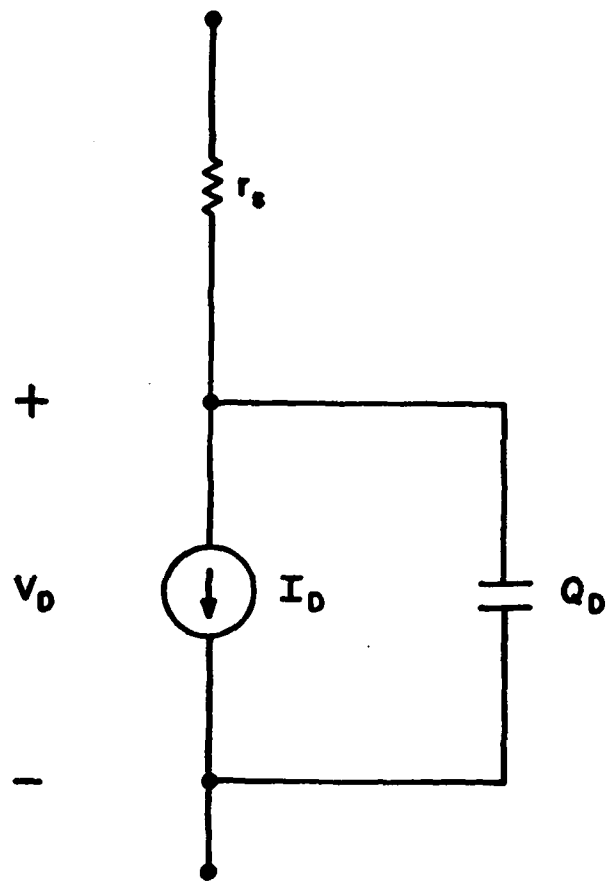


Fig. 6. The SPICE semiconductor diode model.

The diode and transistor parameter values used by McDonnell Douglas in their dc computer simulation of the 7400 NAND gate are presented in Table 6.

Table 6

McDonnell Douglas Diode and Transistor Parameter Values

Diode Parameters

Name	Parameter Description	DIN	D3
RS	Ohmic resistance (Ω)	60	30
IS	Saturation current (pA)	100	5

Transistor Parameters

Name	Parameter Description	T1	T2	T3	T4
BF	Forward Bets (βF)	.316	19.8	17.2	21.7
BR	Reverse Beta (βR)	.0024	.060	.082	.106
RB	Base Ohmic Resistance (Ω)	68.	75.	70.	80.
IS	Saturation current (pA)	.5	3.	8.	20.
AF[a]	Forward alpha (αF)	.24	.952	.945	.956
AR[a]	Reverse alpha (αR)	.0024	.057	.076	.0956
IES[a]	Emitter diode sat.curr (pA)	2.	3.	8.	20.
ICS[a]	Collector diode sat. current (pA)	200.	50.	100.	200.

[a]Parameter used in modified Ebers-Moll model.

The final transistor and diode parameter values used in our computer simulation are noted in Table 7. As indicated by the asterisk, all parameter values not listed are the typical SPICE values. Those parameter values with the superscript 2 were obtained by "fine tuning" in order to achieve typical circuit performance once it was determined that neither the McDonnell Douglas or SPICE values would yield typical operation of the NAND gate.

Table 7

Semiconductor Parameter Values Used*

Transistor Parameters

Parameter \ Device No.	T_{11} & T_{12}	T_2	T_3	T_4
B_f	0.316^1	19.8^1	17.2^1	21.7^1
B_r	0.02^2	0.06^1	0.082^1	0.106^1
r_b	$68\Omega^1$	$75\Omega^1$	$70\Omega^1$	$80\Omega^1$
τ_F	$0.39nS^2$	$0.39nS^2$	$0.39nS^2$	$0.39nS^2$

Diode Parameters

Parameters \ Device No.	D_1, D_2	D_3
I_S	$1 \times 10^{-16}A^2$	$1 \times 10^{-16}A^2$
r_S	$60\Omega^1$	$30\Omega^1$

Sources: 1 McDonnell Douglas
2 Syracuse University

*All parameter values not listed are the typical SPICE values.

The justification and effect of using parameter values different from those of McDonnell Douglas and SPICE are given in Table 8. All of the parameter values finally decided upon are considered to be reasonable.

Table 8

Justification and Effect of Parameter Changes

Parameters differing from McDonnell Douglas

Parameter	Change From	To	Justification	Effect
$B_r(T_1)$	0.0024	0.02	More typical to TTL input transistor (see Ref. 3).	Current levels closer to manufacturer's specification
I_S(transistors)	10^{-12}A	10^{-16}A	Typical SPICE value	Rise/fall times, propagation delays and voltage levels closer to manufacturer's specifications
I_S(Diodes)	10^{-12}A	10^{-16}A	More reasonable value	Voltage and current levels closer to manufacturer's specifications

Parameters differing from typical SPICE values

Parameter	Change From	To	Justification	Effect
τ_F	0.1nS	0.39nS	More appropriate for a switching transistor	Gives more reasonable base-emitter capacitance
I_S (Diodes)	10^{-14}A	10^{-16}A	More reasonable value	Voltage and current levels closer to manufacturer's specifications.

Using the parameter values specified in Table 7, a computer run was made without interference to determine how well the simulated NAND gate approached typical behavior. The results are summarized in Table 9. Observe that all signal parameter values of the output waveform are either close to the typical values or well within the manufacturer's specifications.

Table 9

Comparison of Simulated NAND Gate Behavior to Manufacturer's Specifications

Signal Parameter	Computer Simulation Result	Manufacturer's Specifications	
		Typical	Extreme
V_{OH}	3.59V	3.4V	2.4V Min
V_{OL}	0.2V	0.2V	0.4V Max
$t_{pd}(HL)$	13nS	7nS	15nS Max
$t_{pd}(LH)$	17nS	11nS	22nS Max
t_f	4nS	5nS	
t_r	4nS	8nS	
I_{OH}	-57μA	-140μA	-400μA Max
I_{OL}	9.2mA	10mA	16mA Max
I_{IH} @ 3.4V	5μA	14μA	-400μA Max @ 2.4
I_{IL} @ 0.2V	-0.92mA	-1mA	-1.6mA Max @ 0.4V

Parameter values are for 10 fan-out loading.

4. LOADING OF 7400 NAND GATE AND LOCATION OF INTERFERENCE SOURCES

In contrast to McDonnell Douglas who loaded their gate with a fixed resistor in order to approximate a fan-out of 10 gates, we loaded our gate with a second 7400 NAND gate which was impedance scaled so as to also simulate a fan-out of 10 gates. The impedance scaling was accomplished by using the model of the first gate with all resistance values divided by 10, all capacitance values multiplied by 10 and all saturation currents multiplied by 10. This resulted in the currents of the second gate being increased by a factor of 10 while the time constants (i.e., RC products) and voltages (i.e.,RI products) of the second gate remained unchanged from those of the first gate.

By loading the first gate with a second gate, we have more accurately modeled a typical circuit configuration. The time-variant and nonlinear nature of the load is taken into account as the second gate is caused to switch states. In addition, interference applied at the output of the first gate is also injected into the second gate. This more accurately depicts what is apt to happen in practice. Finally, by observing the output of the second gate, it is possible to determine whether waveform distortion in the output of the first gate is severe enough to cause undesired state changes in the output of the second gate. A fan-out of 10 gates was used because manufacturer's specifications are often given in terms of this type of loading. Also,

it was anticipated (and subsequently confirmed) that the first gate is more susceptible to EMI when loaded with a fan-out of 10 as opposed to a fan-out of 1.

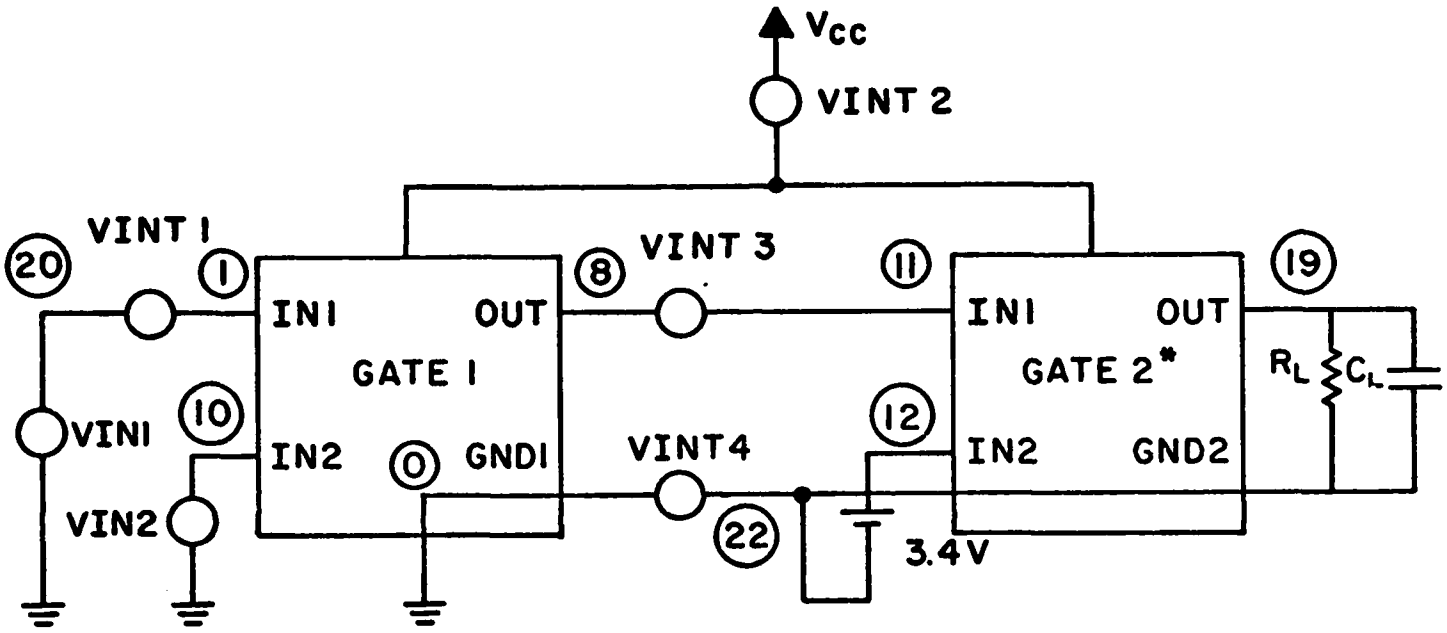
The entire system simulated by the SPICE program is shown in Fig. 7. For convenience, the second gate was loaded by the parallel combination of a fixed resistor and capacitor to ground. In order to simulate a fan-out of 10 gates, R_L and C_L were set equal to 400 ohms and 15 pF, respectively. In addition, VIN2 of the second gate (node 12) was maintained at the HIGH voltage level of 3.4 volts. The truth table for the two gates of Fig. 7 is given in Table 10. V(1) and V(10) denote the two inputs of the first gate. V(8) denotes the output of the first gate while V(19) denotes the output of the second gate. With VIN2 of the second gate (node 12) held HIGH, note that the output of the second gate changes state whenever the output of the first gate changes state.

Table 10

Truth Table for Two Gates of Fig. 7

V(1)	V(10)	V(8)	V(19)
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

The network topology of gate 2 is identical to that of gate 1 as given in Fig. 1a. However, the component values of gate 2 differ from those of gate 1 because of the impedance scaling mentioned



VINT1 - Interference on input of gate 1

VINT2 - Interference on power line common to both gates

VINT3 - Interference on output of gate 1 (series connection)

VINT4 - Interference on ground common to both gates

*The gate 2 parameters were impedance scaled so as to simulate a 10 fan-out loading of gate 1.

Fig. 7. Complete system simulated by the SPICE program.

previously. The complete schematic for the two cascaded gates is shown in Fig. 8. The corresponding node, device, and resistor numbers for the two gates are listed in Table 11.

Table 11

Numbering Correspondence between Gates 1 and 2

Node number correspondence

Node Numbers Gate 1	2	3	4	5	6	7
Node Numbers Gate 2	13	14	15	16	17	18

Device number correspondence

Device Numbers Gate 1	T_{11}	T_{12}	T_2	T_3	T_4	D_1	D_2	D_3
Device Numbers Gate 2	T_{51}	T_{52}	T_6	T_7	T_8	D_4	D_5	D_6

Resistor number correspondence

Resistor Numbers Gate 1	R_1	R_2	R_3	R_4
Resistor Numbers Gate 2	R_5	R_6	R_7	R_8

The sinusoidal interference was injected into the system of Fig. 7 while the first gate was being driven by the two inputs shown in Fig. 9. Observe that these inputs exercise all four combinations of the system truth table given in Table 10. As shown in Fig. 7, interference sources were impressed on the first gate's input and output terminals and on the power line and ground connections common to both gates. The various interference sources were injected one at a time. Those not in use were deactivated by constraining their voltages to be zero.

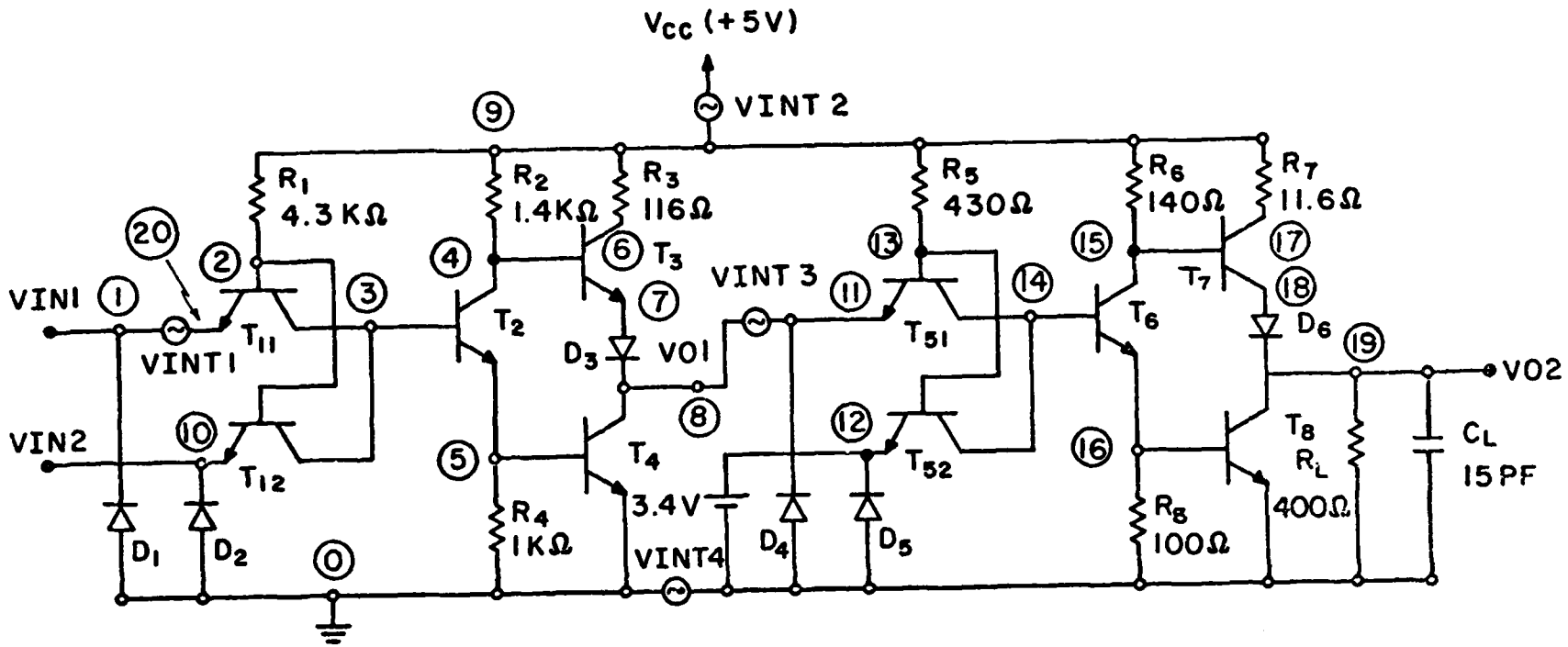
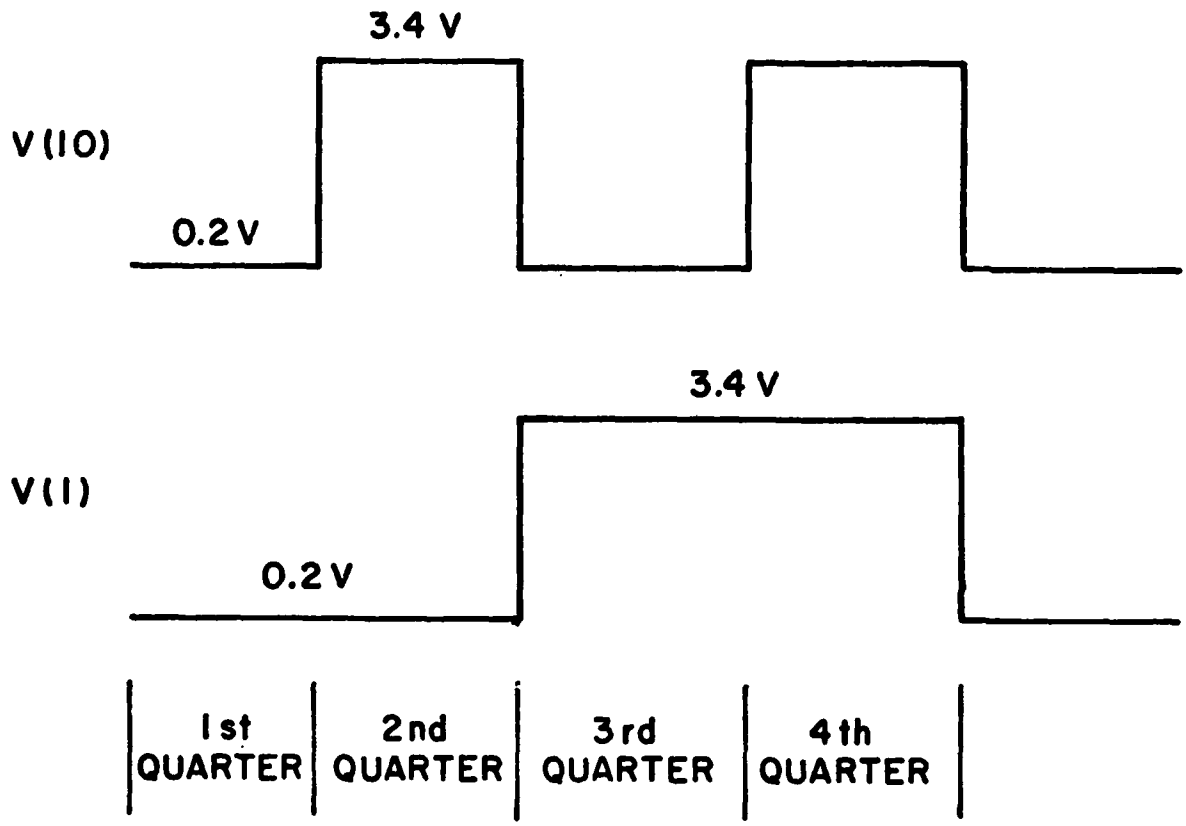


Fig. 8. Complete schematic of the two NAND gates.



*The input rise/fall times were set equal to 5nS for computer simulation.

*The pulse widths were allowed to vary depending upon the interference frequency.

Fig. 9. Input waveforms used to drive the first gate while sinusoidal interference was injected into the system of Fig. 7.

Depending upon the point at which the interference was injected, it was discovered that the system was most susceptible to sinusoidal interference during certain quarters of the input, as defined in Fig. 9. For example, the fourth quarter was found to be most critical when the interference was applied either in series with the output of gate 1 (VINT 3) or in the ground line (VINT 4). As shown in Fig. 10, a 1 MHz sinusoidal interferer of amplitude 3V did not cause any noticeable interference on the output of gate 2 during the first three quarters but did result in fluctuations between the HIGH and LOW states during the fourth quarter. Similarly, when the same interference was applied to the input of gate 1 (VINT 1), the system was observed to be susceptible during the second and fourth quarters, as shown in Fig. 11. Finally, with a 1 MHz interferer of amplitude 5V injected into the power line (VINT 2), the system was found to be susceptible during the first three quarters but not in the fourth. This is illustrated in Fig. 12. Although severe fluctuations did occur on the output of gate 2 during the fourth quarter, the system is not considered to be susceptible during this quarter since the output did not fall below 2V (i.e., did not change states).

It was also discovered that the system is most susceptible to sinusoidal interference applied in series with the output of gate 1 (VINT 3) as opposed to interference injected into the input of gate 1 (VINT 1), the power line (VINT 2), and the ground line (VINT 4). This is illustrated in Fig. 13 where the minimum interference amplitude required to cause the steady-state portion of the gate 2 output to

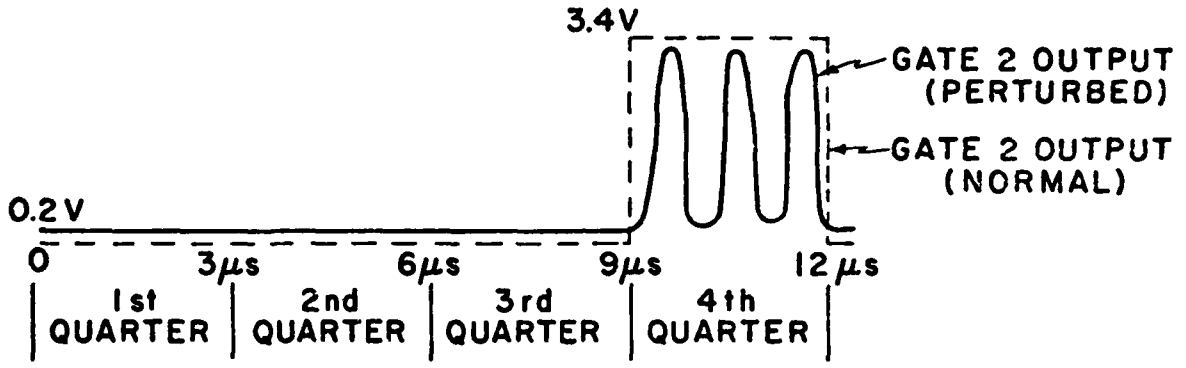


Fig. 10. Output of gate 2 with a 1 MHz sinusoidal interferer of amplitude 3V applied either in series with the output of gate 1 (VINT 3) or in the ground line (VINT 4).

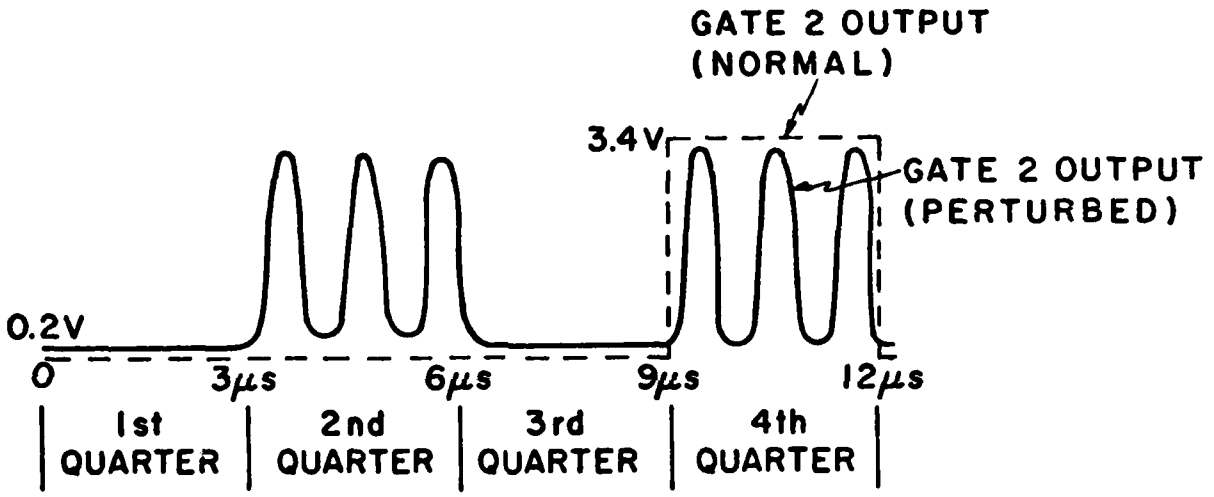


Fig. 11. Output of gate 2 with a 1 MHz sinusoidal interferer of amplitude 3V applied to the input of gate 1 (VINT 1).

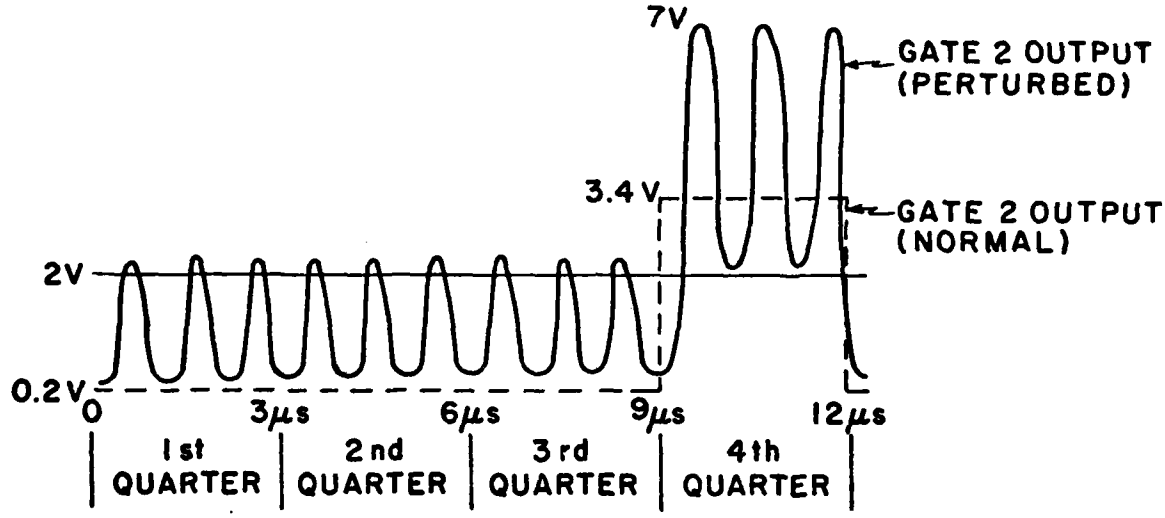


Fig. 12. Output of gate 2 with a 1 MHz sinusoidal interferer of amplitude 5V injected into the power line (VINT 2).

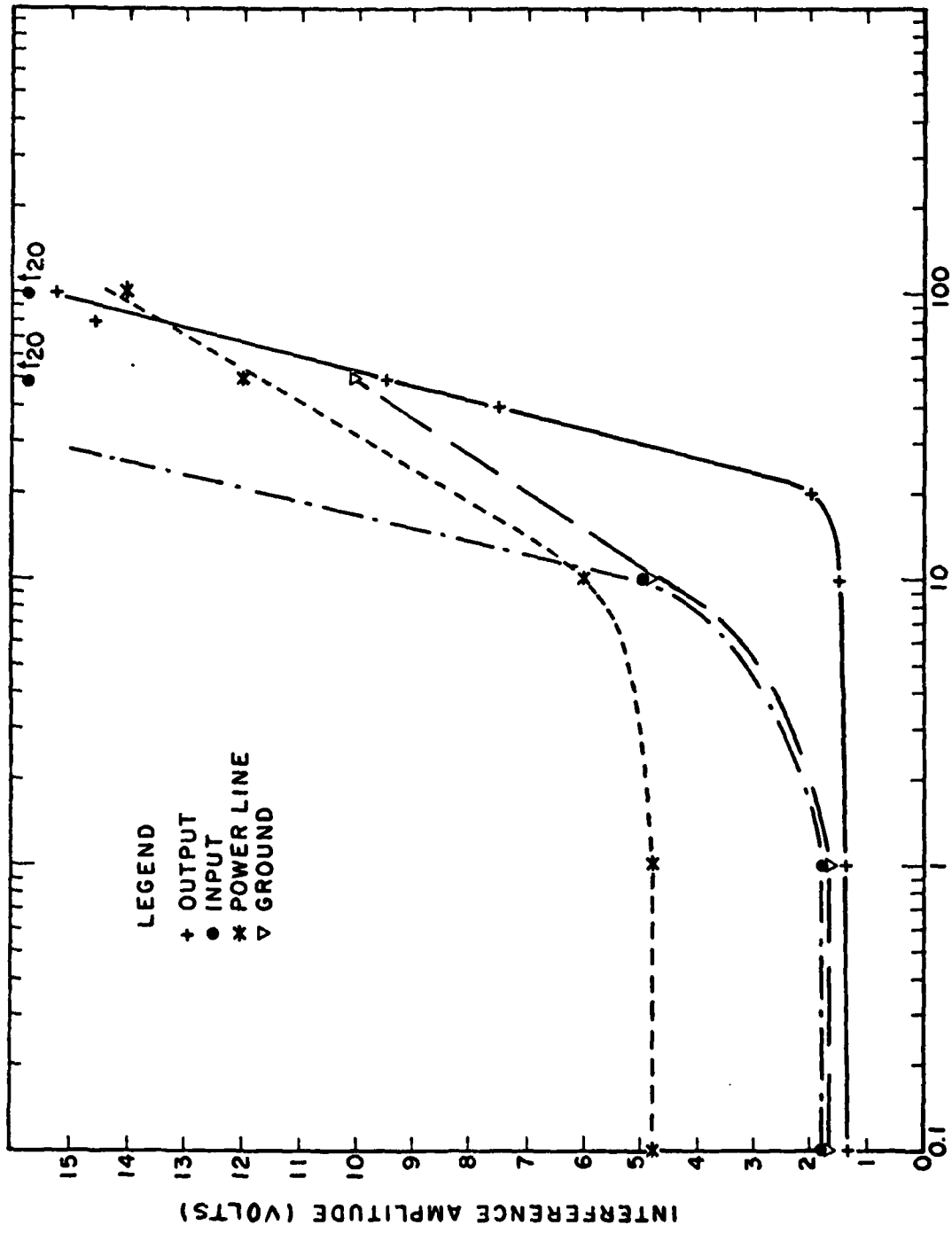


Fig. 13. Minimum interference amplitude required to cause the steady-state portion of the gate 2 output to change state.

change state is plotted as a function of the interference frequency. Consistent with the previous discussion of susceptible input quarters, the four curves in Fig. 13 pertain to the following susceptible quarters: (1) output of gate 1 - fourth quarter, (2) input of gate 1 - second quarter, (3) power line - first quarter, and (4) ground line - fourth quarter. The curve for sinusoidal interference inserted in series with the output of gate 1 displays not only the largest susceptibility but also the broadest bandwidth. It is pertinent to point out that McDonnell Douglas also found the NAND gate to be most susceptible to RF interference entering the gate output [1].

Consequently, in the remainder of this report, results are presented only for the case of sinusoidal interference applied in series with the output of gate 1 (VINT 3). Recall that the system is most susceptible to this interference during the fourth quarter of the input. In order to examine the effect of interference during the switching mode while reducing the running time of the simulation, only the end of the third quarter to the steady-state portion of the fourth quarter was simulated on the computer. Typical behavior of the two gates during this interval without interference is illustrated in Fig. 14.

As a final check that the NAND gates, in the absence of interference, were functioning properly during the computer simulation, the voltage levels at all the nodes of Fig. 8 were examined during the third quarter (i.e. V(8) HIGH, V(19) LOW) and the fourth quarter (i.e. V(8) LOW, V(19) HIGH). These voltages are tabulated in Table 12.

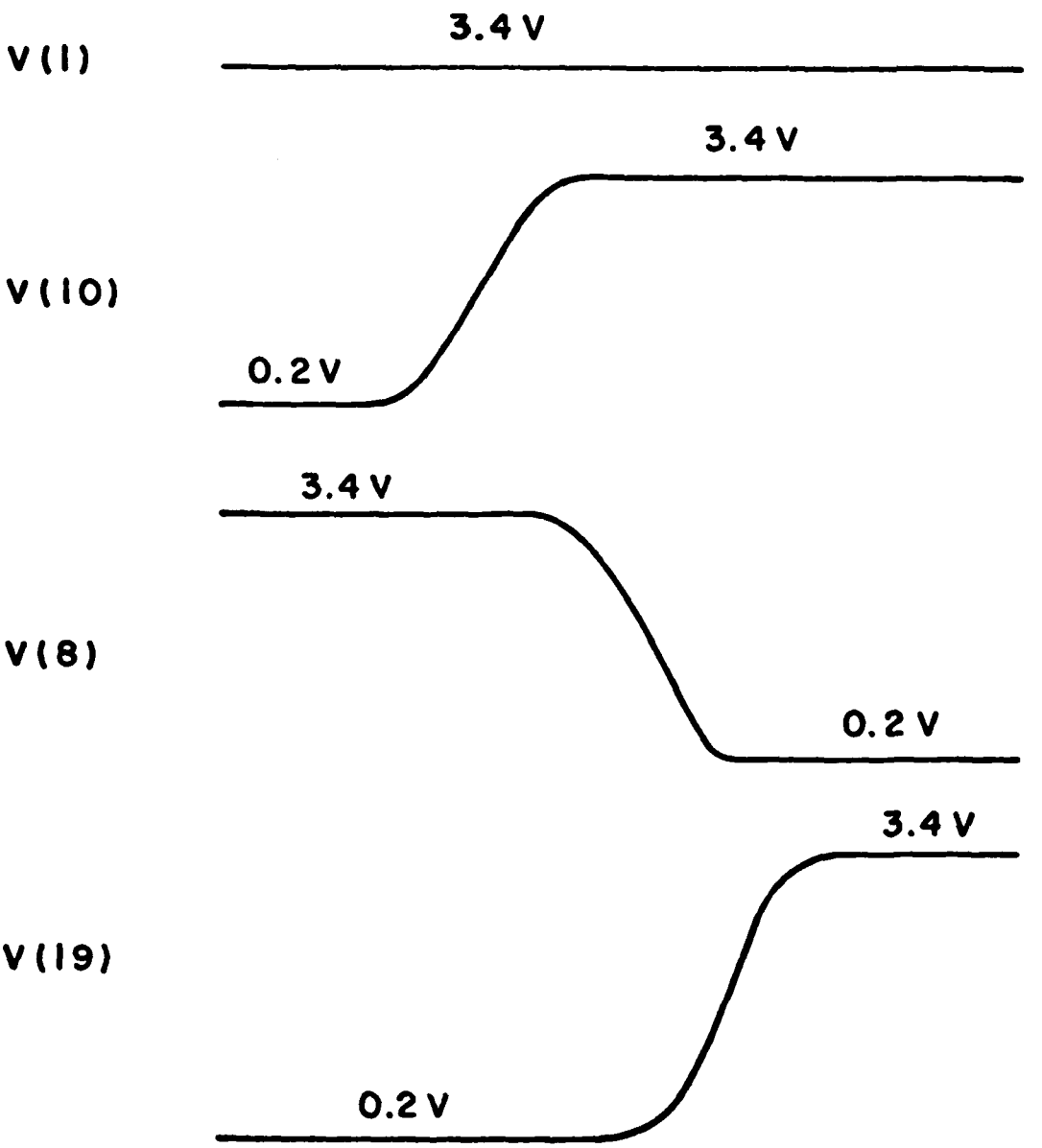


Fig. 14. Typical behavior of the two gates during the transition from the third to fourth quarters without interference.

All of these voltages conform to typical values. In addition, the current levels, timing sequences, and time delays all agreed with those of a properly functioning circuit.

Table 12

Node Voltages for Third and Fourth Quarters

Node Number	Third Quarter Voltages (Volts)	Fourth Quarter Voltages (Volts)
20	0.2	3.4
10	0.2	3.4
2	0.9494	2.545
3	0.3022	1.882
4	4.993	1.188
5	0.0011	1.032
6	4.993	5.0
7	4.292	0.7338
8 , 11	3.589	0.2118
13	2.501	0.9993
14	1.838	0.3594
15	1.143	4.935
16	0.9878	0.0001
17	5.000	4.907
18	0.6151	4.163
19	0.0629	3.368

5. REPRESENTATIVE OUTPUT WAVEFORMS WITH SINUSOIDAL INTERFERENCE INJECTED IN SERIES WITH THE OUTPUT OF GATE 1

With the inputs of gate 1 chosen so as to transition from the third to fourth quarters (see Fig.14), a sinusoidal interferer, VINT3, was inserted in series with the output of gate 1 as shown in Fig. 7. (The other interference sources in Fig. 7 were deactivated by setting their voltages equal to zero.) The amplitude and frequency of the interferer were varied from 0.5 to 20 Volts and from 0.1 to 200 MHz, respectively.

For certain amplitude and frequency combinations of the interferer, severe distortion was observed in the output waveforms of gates 1 and 2. The purpose of the simulation was to investigate the susceptibility of the first gate. (The second gate acts merely as a load for the first gate.) However, looking at only the distorted output of the first gate, it is not clear to what extent upset will be caused in a following gate. For this reason, attention is focused on the output of gate 2. Recall from Fig.14 that the second gate output ideally should have a smooth transition from the LOW to HIGH states. In this section representative output waveforms for gate 2 are presented.

The case for which the amplitude and frequency of the interferer are 10 Volts and 100 MHz, respectively, is shown in Fig. 15. Observe that there is a slower than normal transition from the LOW state to the HIGH state. However, once the output has achieved the HIGH state, the waveform remains in the HIGH state even though it

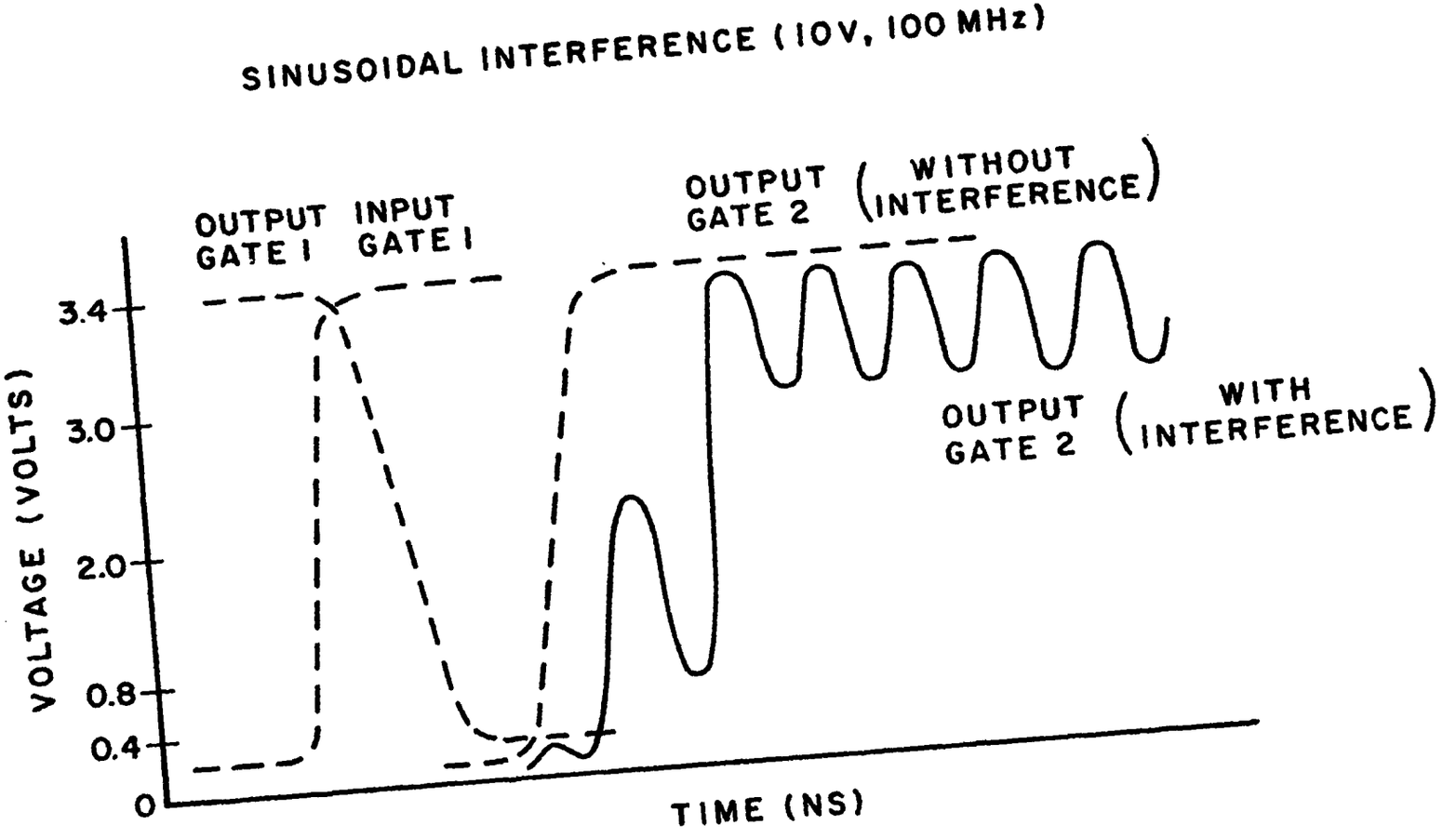


Fig. 15. Output of gate 2 remains in HIGH state.

undergoes noticeable oscillation. If the output is sampled while it is in the HIGH state, no logic errors are likely to occur.

In Fig. 16 the amplitude of the interferer is maintained at 10 Volts. However, the frequency is reduced to 70 MHz. The transition from the LOW to HIGH states takes even longer than before. In addition, the fluctuations in the HIGH state are more severe. In fact, in the steady-state the ouput periodically enters the UNDEFINED area which extends between 0.8 and 2 Volts. If the output is sampled while it is in the UNDEFINED area, a logic error may result.

The frequency of the interferer is reduced to 50 MHz in Fig. 17 while the amplitude is again set at 10 Volts. An even longer transition period ensues. Now the output, which should remain HIGH, periodically drops to the LOW state which extends below 0.8 Volts. Obviously, if the output is sampled while it is in the LOW state, a logic error will result.

In those applications where the output of gate 2 would be differentiated in order to provide a triggering pulse for another stage, the distortion in the leading edge of the responses shown in Figs. 15, 16, and 17 could also cause the generation of logic errors.

A very interesting case is depicted in Fig. 18. Here the amplitude of the interferer is 20 Volts while its frequency is 100 MHz. Now the output of gate 2 never makes the transition from the LOW state to the HIGH state. This will result in a logic error irrespective of the time at which the output is sampled.

Calcomp plots for the cases illustrated by the sketches shown in Figures 14-18 are presented in Appendix A.

In some situations it may be desirable to model the interference as

being inserted in parallel, as opposed to in series, with the output of gate 1. Several runs were made with the interference source connected from the output of gate 1 to ground. A large capacitor was placed in series with the source so as not to upset the dc behavior of the gate. Results similar to those presented in Figs. 15 through 18 were observed.

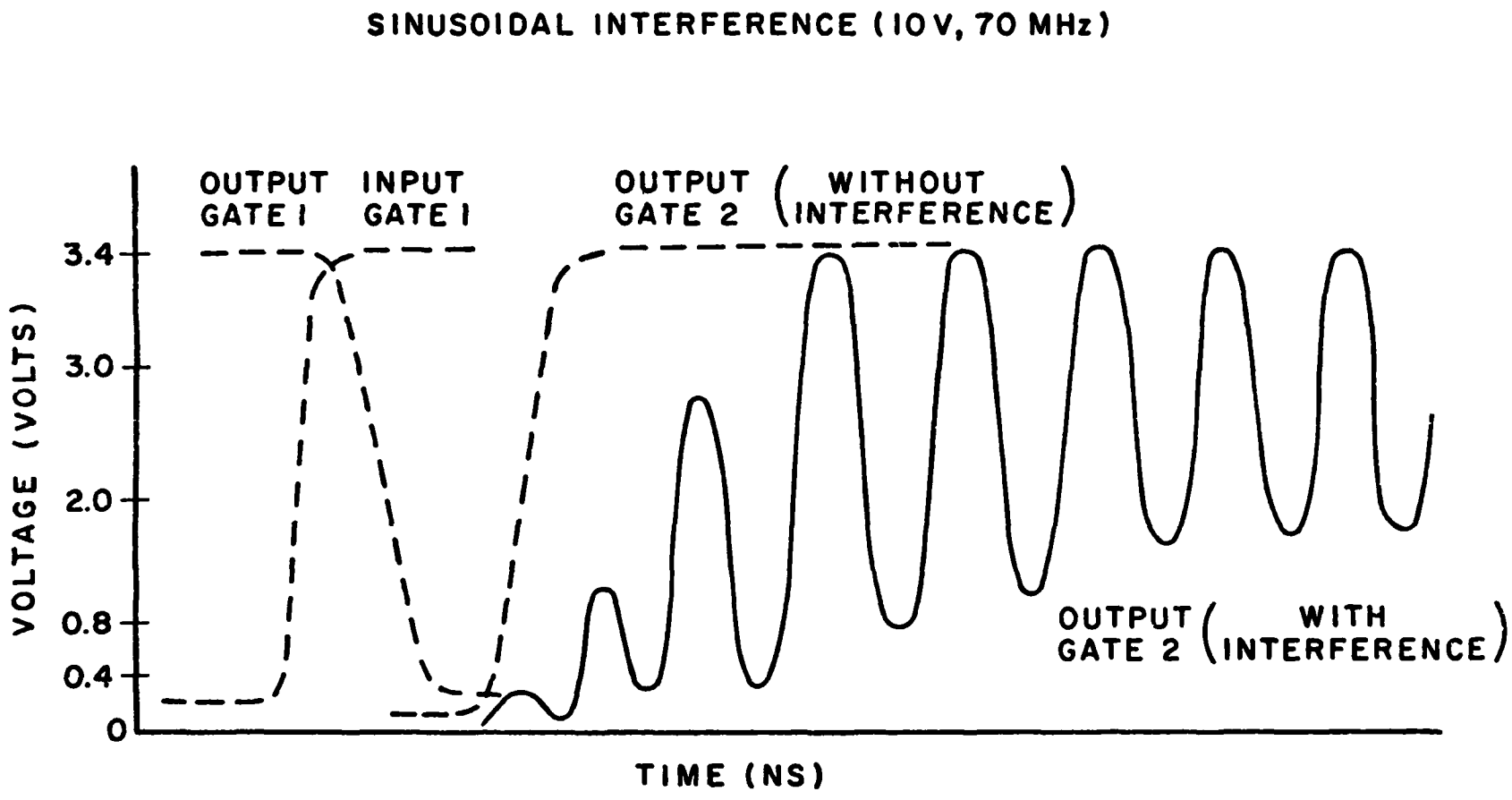


Fig. 16. Output of gate 2 enters UNDEFINED area.

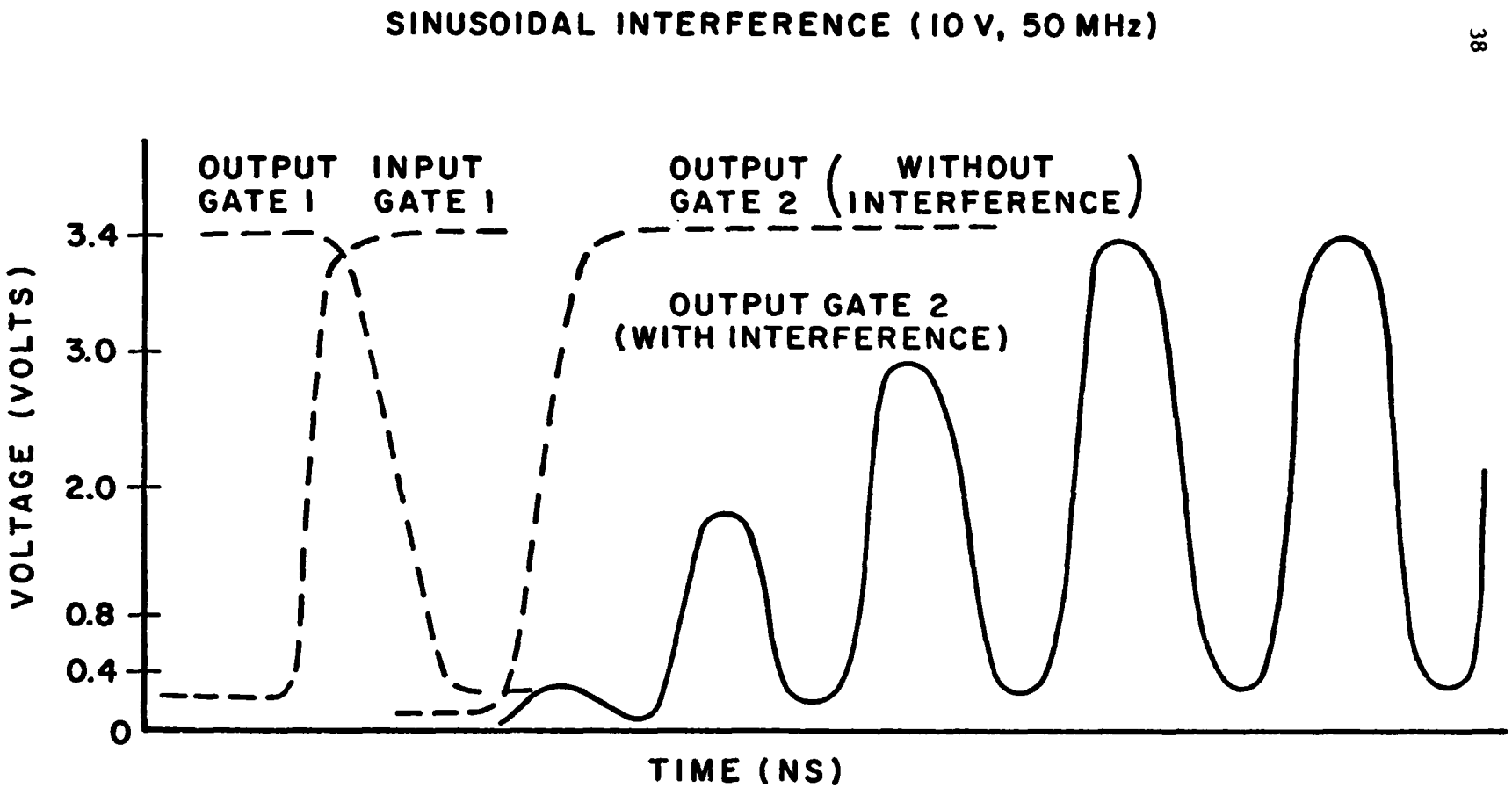


Fig. 17. Output of gate 2 drops to the LOW state.

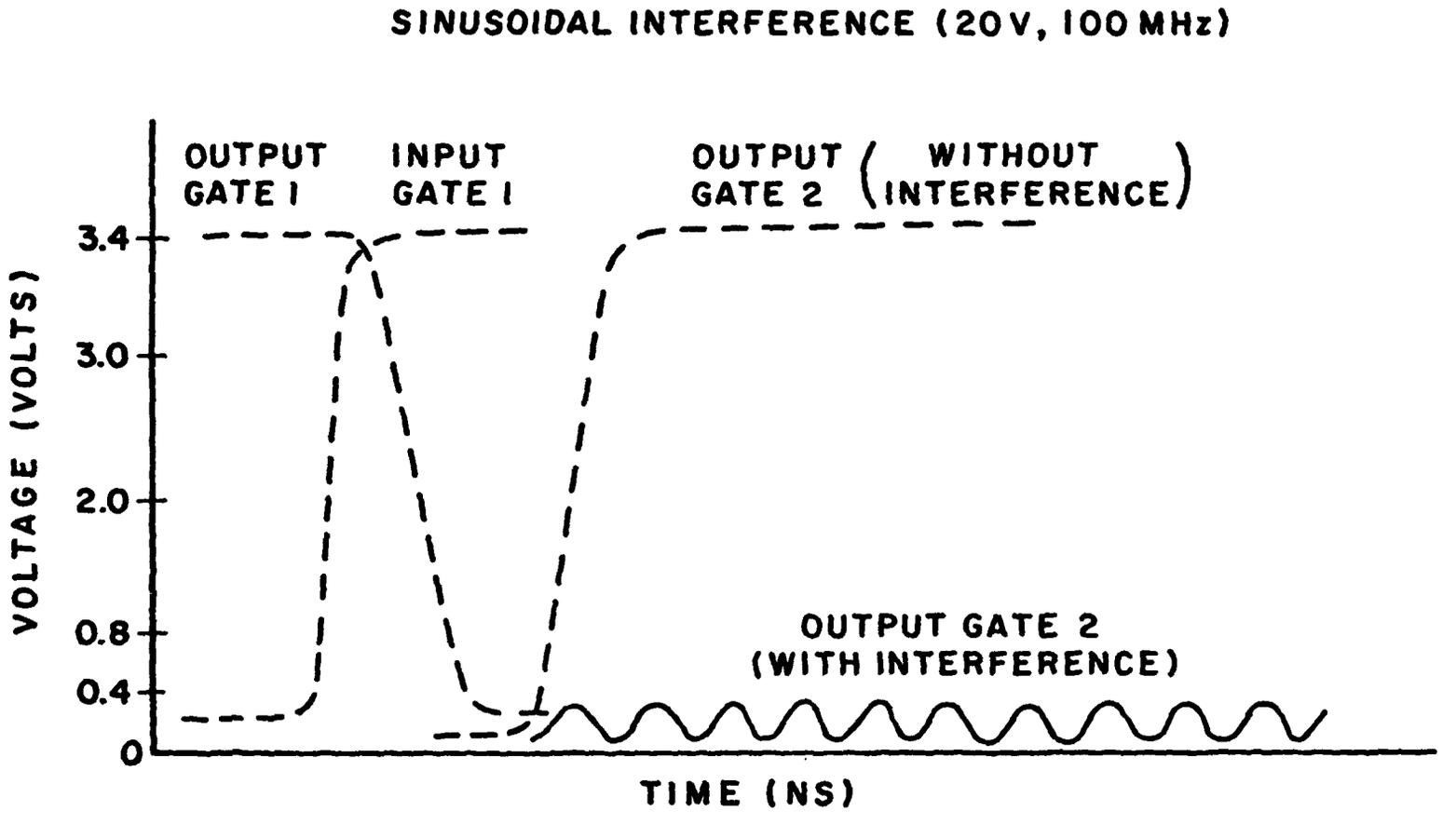


Fig. 18. Output of gate 2 remains in the LOW state.

6. DEFINITIONS OF WAVEFORM PARAMETERS FOR DESCRIBING INTERFERENCE EFFECTS.

In order to describe the waveform distortions illustrated in Section 5, it is convenient to distinguish between steady-state and transient effects. The steady-state effects pertain to the periodic portion of the waveform as it tries to maintain a constant output in the HIGH state. The transient effects apply to the leading edge of the waveform where it attempts to switch from the LOW to HIGH state. Various waveform parameters are defined in this section in order to describe these effects. These parameters are then plotted in Section 7 as a function of the amplitude and frequency of the sinusoidal interferer.

We first define the steady-state parameters. Because the interference is periodic, the fluctuations in the output of gate 2 eventually become periodic. The steady-state parameters are defined with respect to the periodic portion of the output.

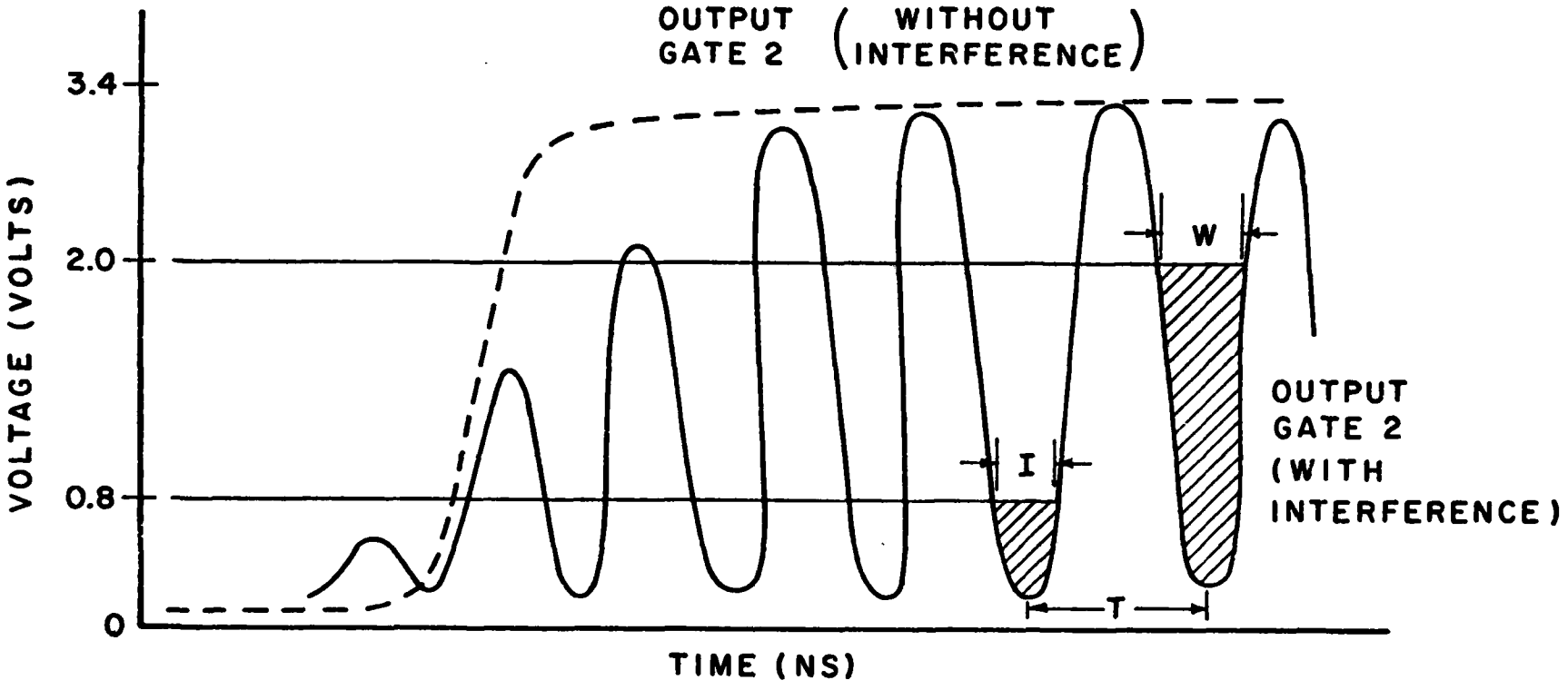
Consider one period of the steady-state output as shown in Fig. 19. Let

$$T = \frac{1}{f}$$

denote the period where f is the frequency of the interferer. During this period let the time spent in the LOW state be denoted by I. The ERRONEOUS state duty cycle is defined by

$$D_1 = \frac{I}{T} .$$

Note that D_1 gives the fraction of a period the waveform resides in



$$\text{ERRONEOUS STATE DUTY CYCLE} = D_1 = \frac{I}{T}$$

$$\text{UNDEFINED AREA DUTY CYCLE} = D_2 = \frac{W}{T}$$

Fig. 19. Definition of ERRONEOUS state and UNDEFINED area duty cycles.

the LOW state. Similarly, let the time during one period spent in the UNDEFINED area or below be denoted by W. The UNDEFINED area duty cycle is defined by

$$D_2 = \frac{W}{T}.$$

Note that D_2 gives the fraction of a period the waveform resides in or below the UNDEFINED area.

Two additional parameters for describing the steady-state portion of the output are the steady-state mean voltage and the steady-state r.m.s. deviation. Denote the steady-state portion of the output waveform by $v_o(t)$. The steady-state mean voltage is defined to be

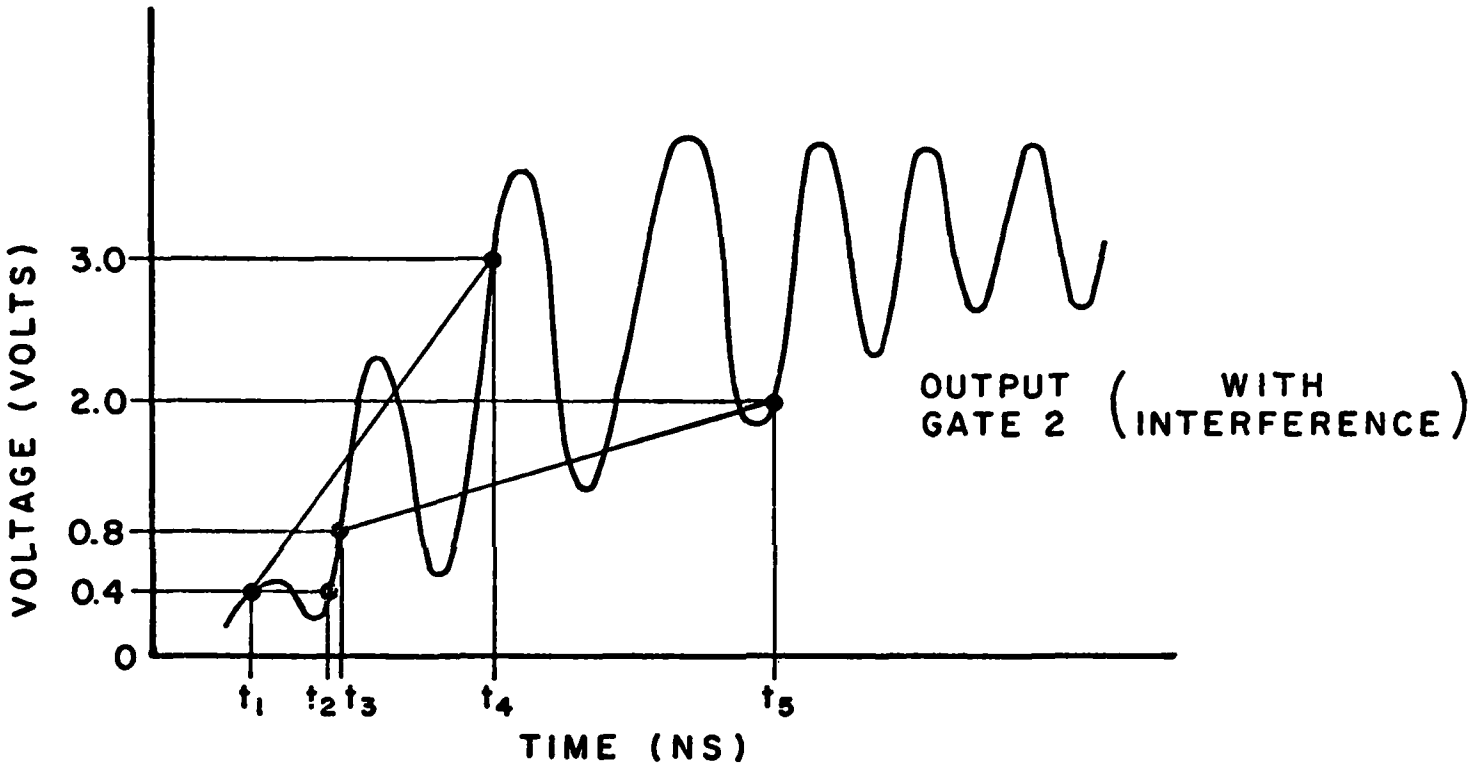
$$A = \frac{1}{T} \int_0^T v_o(t)dt$$

where the average is over one period of the steady-state portion of the output. Obviously, the steady-state mean voltage gives the mean value of the output in the steady-state. The steady-state r.m.s. deviation is defined to be

$$\sigma = [\frac{1}{T} \int_0^T [v_o(t) - A]^2 dt]^{1/2}.$$

Once again, the average is over one period of the steady-state portion of the output. The steady-state r.m.s. deviation is a measure of the size of the fluctuations about the steady-state mean voltage.

The transient waveform parameters are now defined. A typical distorted output is shown in Fig. 20. The time instants t_1, t_2, t_3



t_1 = first time waveform equals 0.4V

t_2 = last time waveform equals 0.4V before reaching 3.0V for the first time.

t_3 = first time waveform equals 0.8V (defined only when steady-state portion of the waveform does not drop below 2.0V).

t_4 = first time waveform equals 3.0V.

t_5 = Last time waveform equals 2.0V (defined only when steady-state portion of the waveform does not drop below 2.0V).

Fig. 20. Definitions of rise time and state transition time.

t_4 and t_5 are defined and illustrated in the figure. The rise time is defined to be

$$t_r = t_4 - t_1.$$

Typical values for the undistorted output voltage are 3.4 Volts in the HIGH state and 0.2 Volts in the LOW state. By defining the rise time with respect to the 3.0 and 0.4 Volt levels, we are using the approximate 90% and 10% values of the HIGH voltage.

The state transition time is defined to be

$$t_s = t_5 - t_3.$$

This definition applies only when there has been a clear transition from the LOW to HIGH states (i.e., when the steady-state portion of the waveform does not drop below 2.0 Volts which is the minimum voltage guaranteed to be recognized as a HIGH voltage by a succeeding gate). The time instant t_3 is defined relative to 0.8 Volts because this is the maximum voltage guaranteed to be recognized as a LOW voltage by a succeeding gate. Observe that for time less than t_3 the waveform is in a recognizable LOW state while for time greater than t_5 the waveform is in a recognizable HIGH state.

The excess propagation delay time is defined in Fig. 21. As shown in Fig. 2a, when there is no waveform distortion, the propagation delay times are defined in terms of the approximate 50% points of the leading and trailing edges. In Fig. 21 the input to gate 1 and the outputs from gates 1 and 2 which would apply if there was no interference are shown in dashed lines to serve as reference waveforms. For the reference waveforms the conventional propagation delay times

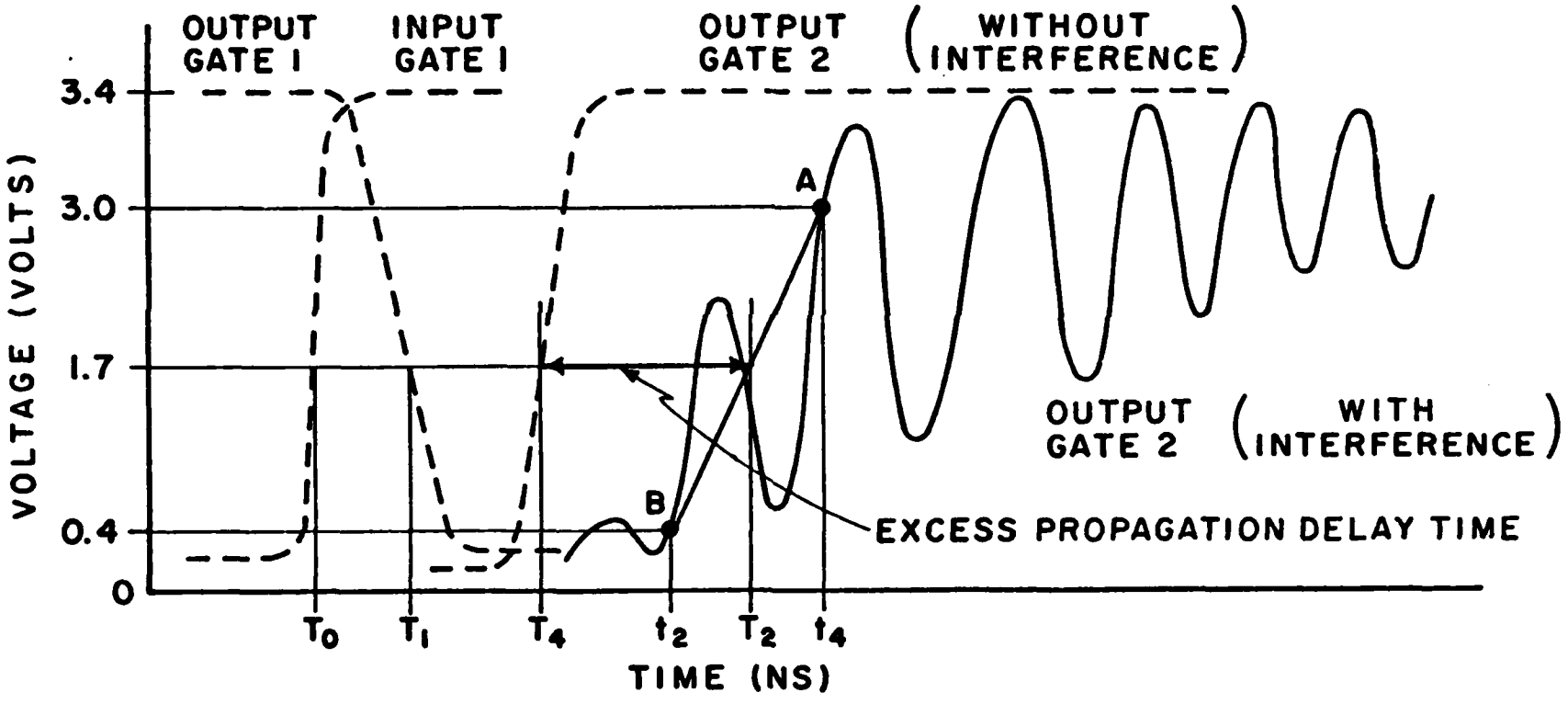


Fig. 21. Definition of excess propagation delay time.

are given by

$$t_{pd}(HL) = T_1 - T_0 \qquad \text{(first gate)}$$

and

$$t_{pd}(LH) = T_4 - T_1. \qquad \text{(second gate)}$$

With interference the output of gate 2 may be heavily distorted. To assist in determining an excess propagation delay time, the straight line AB is drawn between the points A and B, as shown in Fig. 21. The time instants t_2 and t_4 are defined in Fig. 20. t_2 is the last time the waveform equals 0.4 Volts before reaching 3.0 Volts for the first time and t_4 is the first time the waveform equals 3.0 Volts. T_2 is defined to be the time instant at which the straight line AB reaches the 50% point of the unperturbed gate 2 output. The excess propagation delay time is then defined to be

$$t_{epd}(LH) = T_2 - T_4 = T_2 - T_0 - (T_1-T_0) - (T_4-T_1)$$

$$= T_2 - T_0 - t_{pd}(HL) - t_{pd}(LH).$$

7. RESULTS OF COMPUTER SIMULATION

As illustrated in Section 5, the output waveform of gate 2 can be severely distorted when sinusoidal interference is inserted in series with the output of gate 1. Several waveform parameters were defined in Section 6 to assist in describing the interference effects. The results of our computer simulation are now summarized in terms of these waveform parameters. A sample program is shown in Appendix B.

The UNDEFINED area duty cycle and the ERRONEOUS state duty cycle of the gate 2 output are plotted, as a function of interference frequency with the interferer amplitude as a parameter, in Figures 22 and 23, respectively. For a constant frequency the duty cycles are seen to increase with increasing amplitude of the interferer. An interesting phenomenon is the "resonance effect" which is observed for frequencies between 30 and 100 MHz. Also, as was implied by Fig. 18, a duty cycle of 1.0 is possible for sufficiently strong interferers.

The steady-state mean voltage and the steady-state r.m.s. deviation of the gate 1 output are plotted in Figures 24 and 25, respectively. The gate 1 output is chosen in order to compare with the steady-state dc results from the McDonnell Douglas study [1]. Although an exact comparison is not possible because McDonnell Douglas injected the interference in parallel with the gate 1 output where we inserted the interference in series with the gate 1 output, the general trends of the results are identical. Without interference the gate 1 output

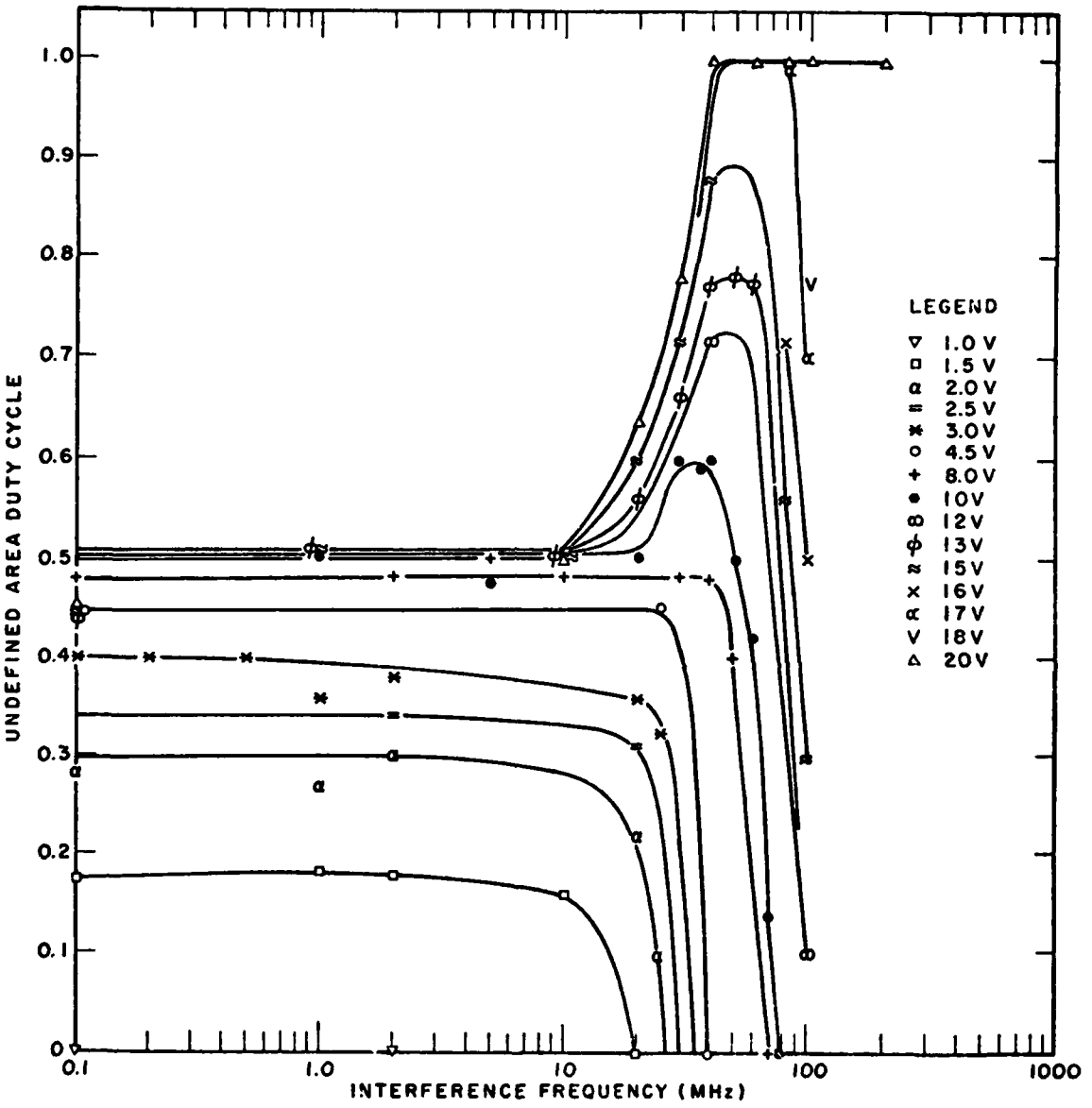


Fig. 22. UNDEFINED area duty cycle for gate 2 output.

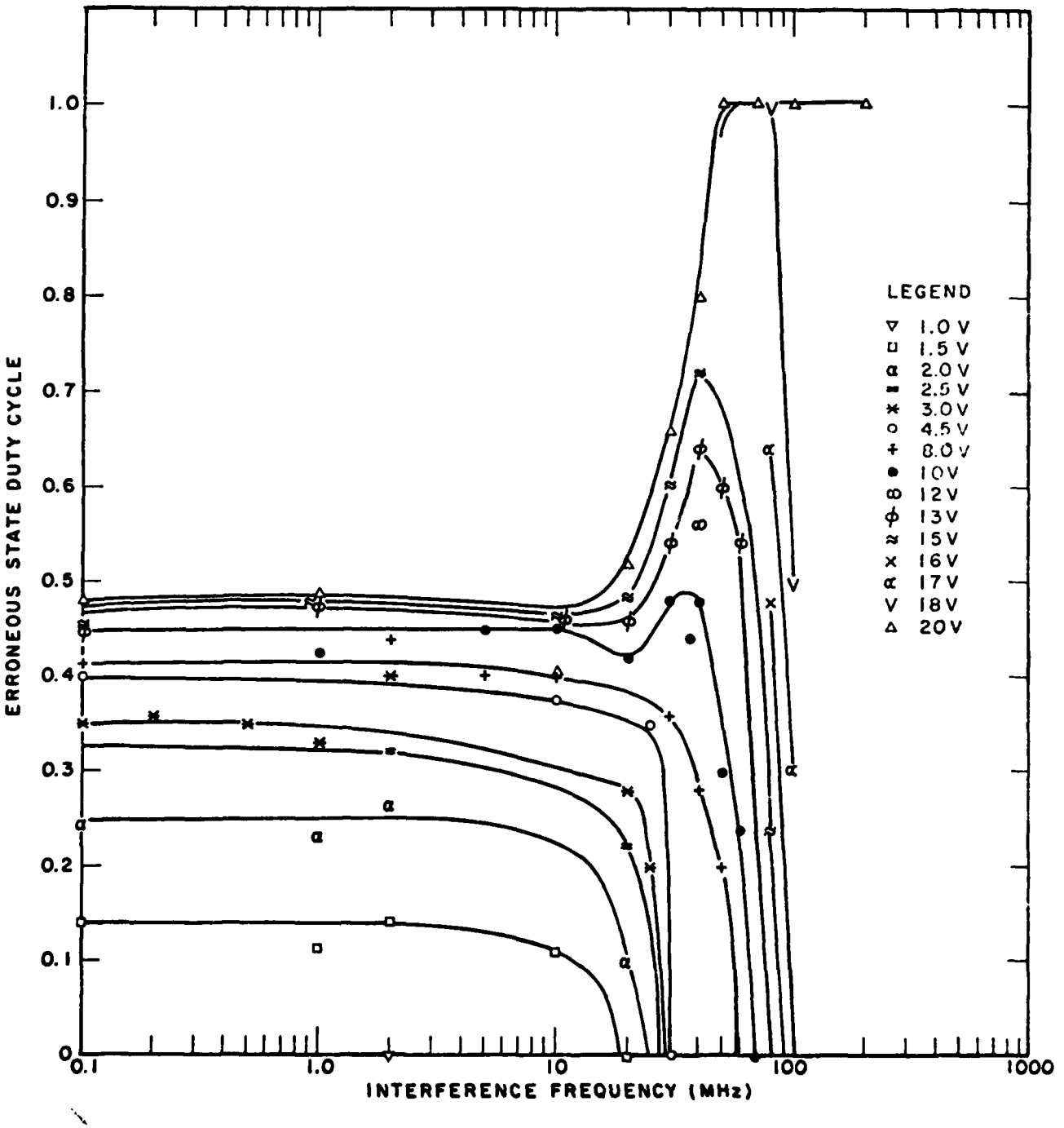


Fig. 23. ERRONEOUS state duty cycle for gate 2 output.

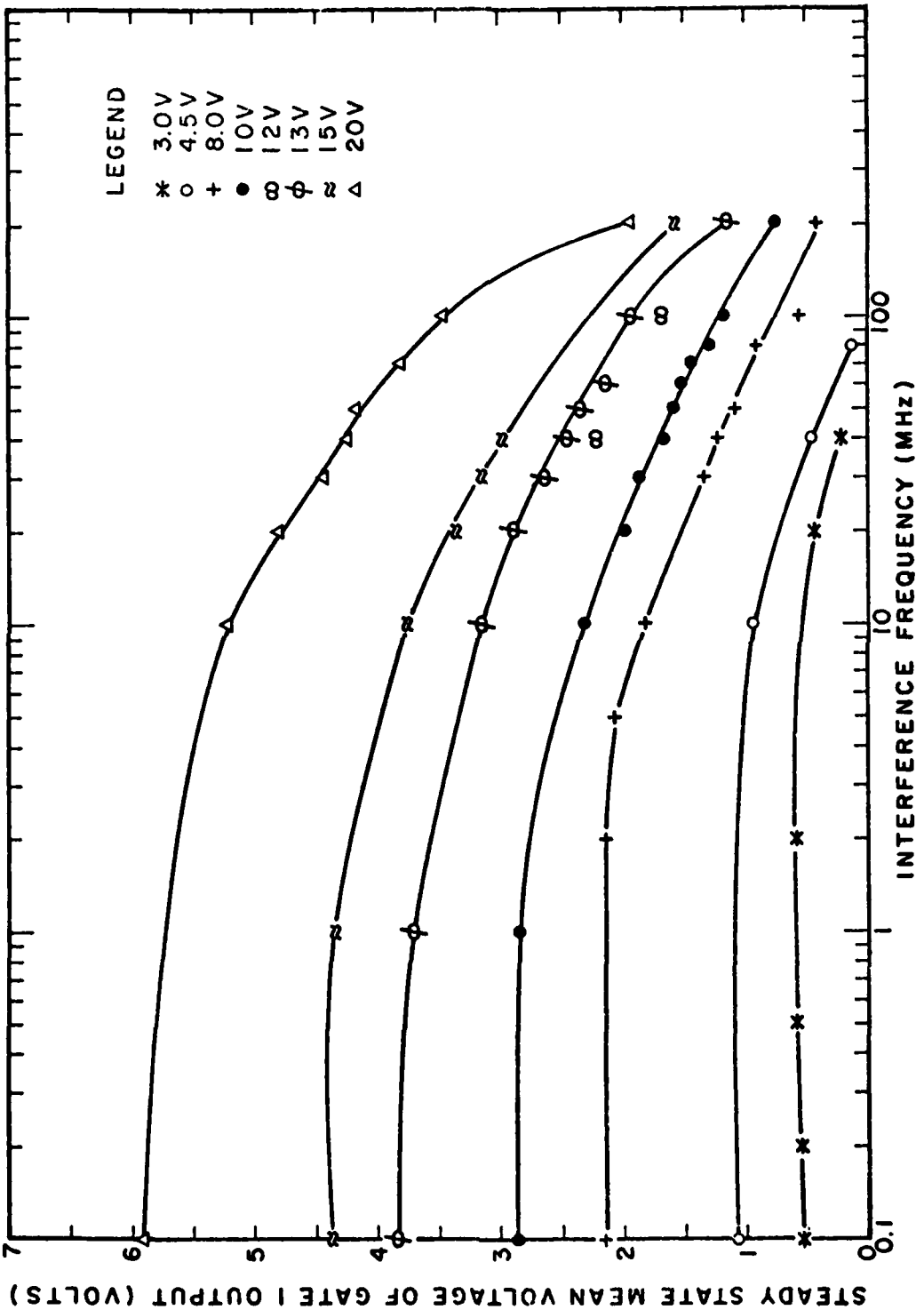


Fig. 24. Steady-state mean voltage of the gate 1 output.

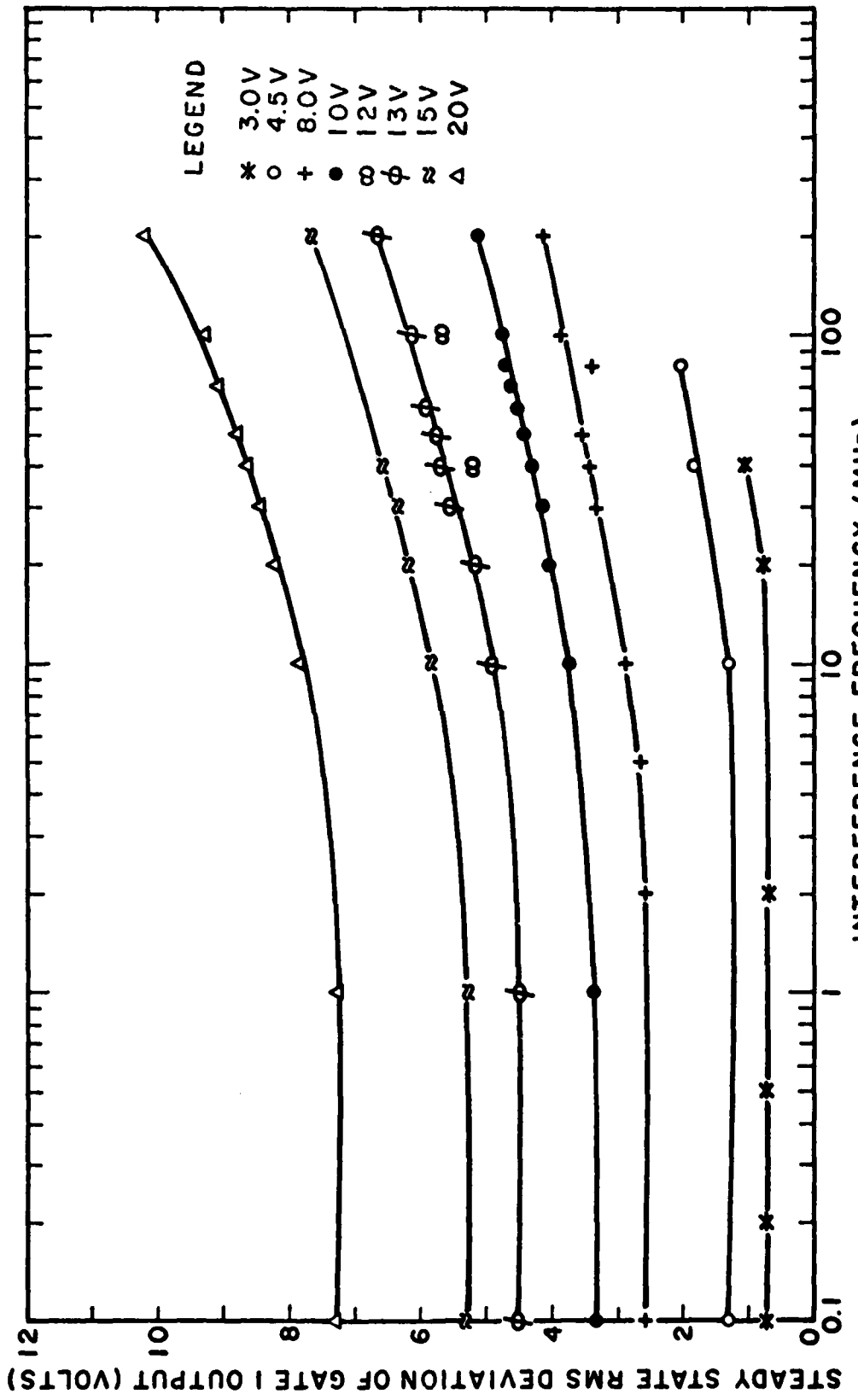


Fig. 25. Steady-state r.m.s. deviation of the gate 1 output.

should remain LOW in the steady-state. It is interesting to note that, in some cases, even when the steady-state dc value of gate 1 increased to levels greater than 2.0 volts, gate 2 did not recognize the waveform as a HIGH voltage input due to the fluctuations in the waveform.

The steady-state mean voltage and the steady-state r.m.s. deviation of the gate 2 output are plotted in Figures 26 and 27, respectively. Observe that a "resonance effect" is seen in Fig. 26 that does not appear for the gate 1 output curves shown in Fig. 24. Also, by comparing Fig. 27 with Fig. 25, it is seen that the steady-state r.m.s. deviation of the gate 2 output is much less dependent on amplitude than is that of the gate 1 output.

The rise time and excess propagation delay time of the gate 2 output are plotted in Figures 28 and 29, respectively. The plots are functions of the interference frequency with interference amplitude as a parameter. Observe that, for large enough amplitudes and for frequencies in the range of 30 to 100 MHz, the "resonance effect" is seen once again. Rise times and excess propagation delay times in excess of 100 nanoseconds apply during this "resonance" phenomenon. These values are an order of magnitude larger than the typical values without interference.

It should be pointed out that the sinusoidal interference distorts the trailing edge of the gate 2 output in a manner different from its effect on the leading edge. Therefore, a plot of the fall time differs from the rise time plot of Fig. 28. The effect of the phase of the interfering signal on the rise and delay times was also

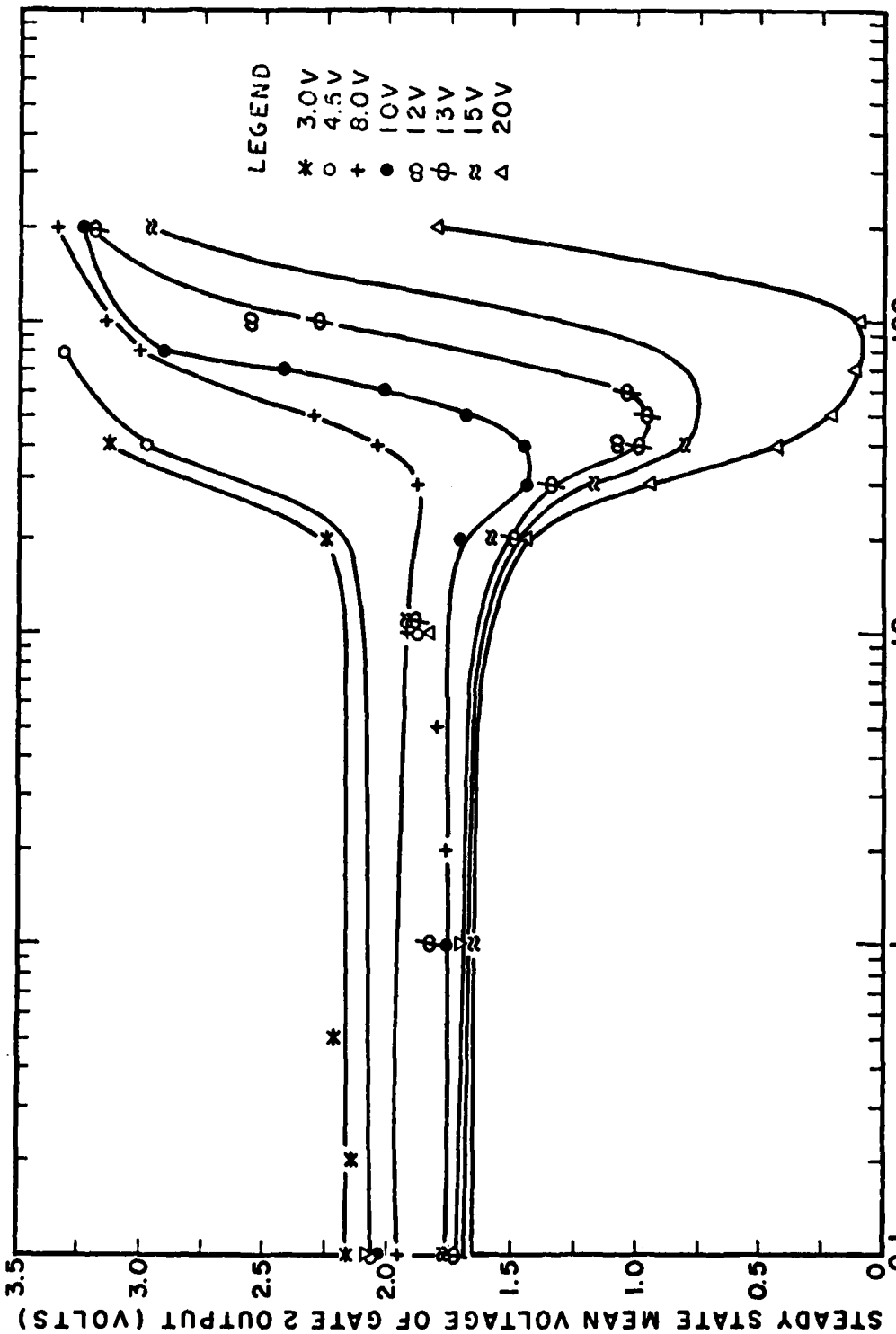


Fig. 26. Steady-state mean voltage of the gate 2 output.

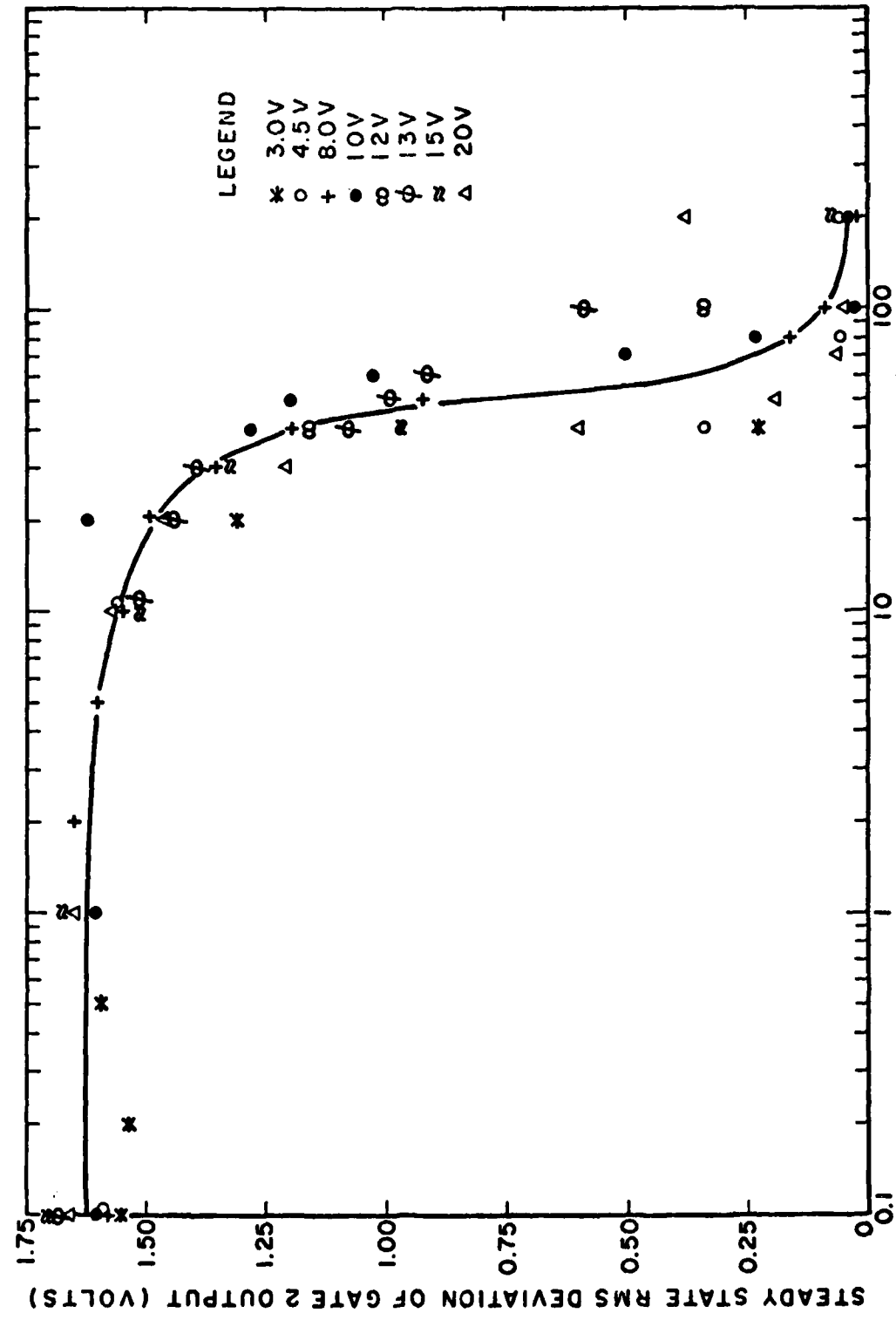


Fig. 27. Steady-state r.m.s. deviation of the gate 2 output.

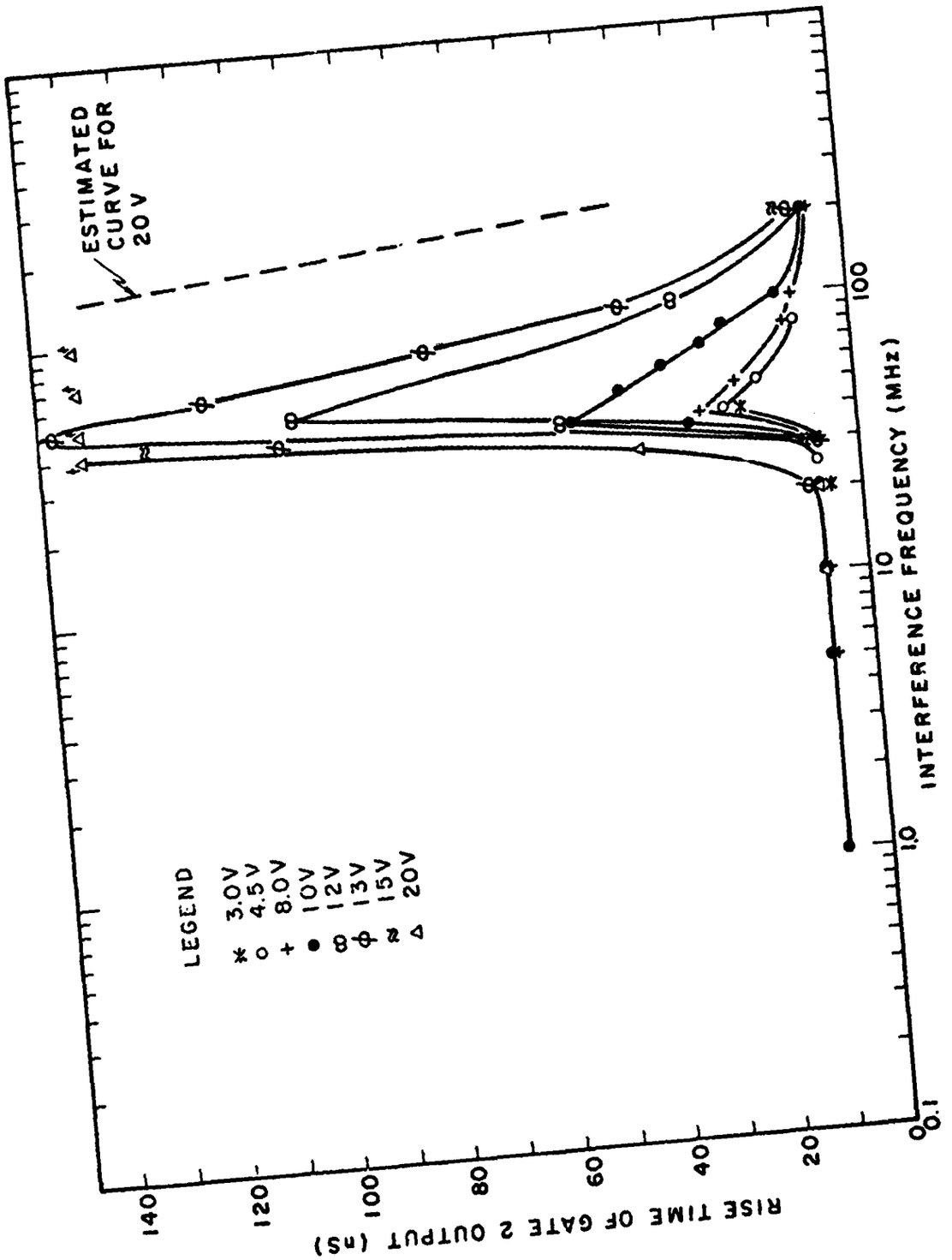


Fig. 28. Rise time of gate 2 output.

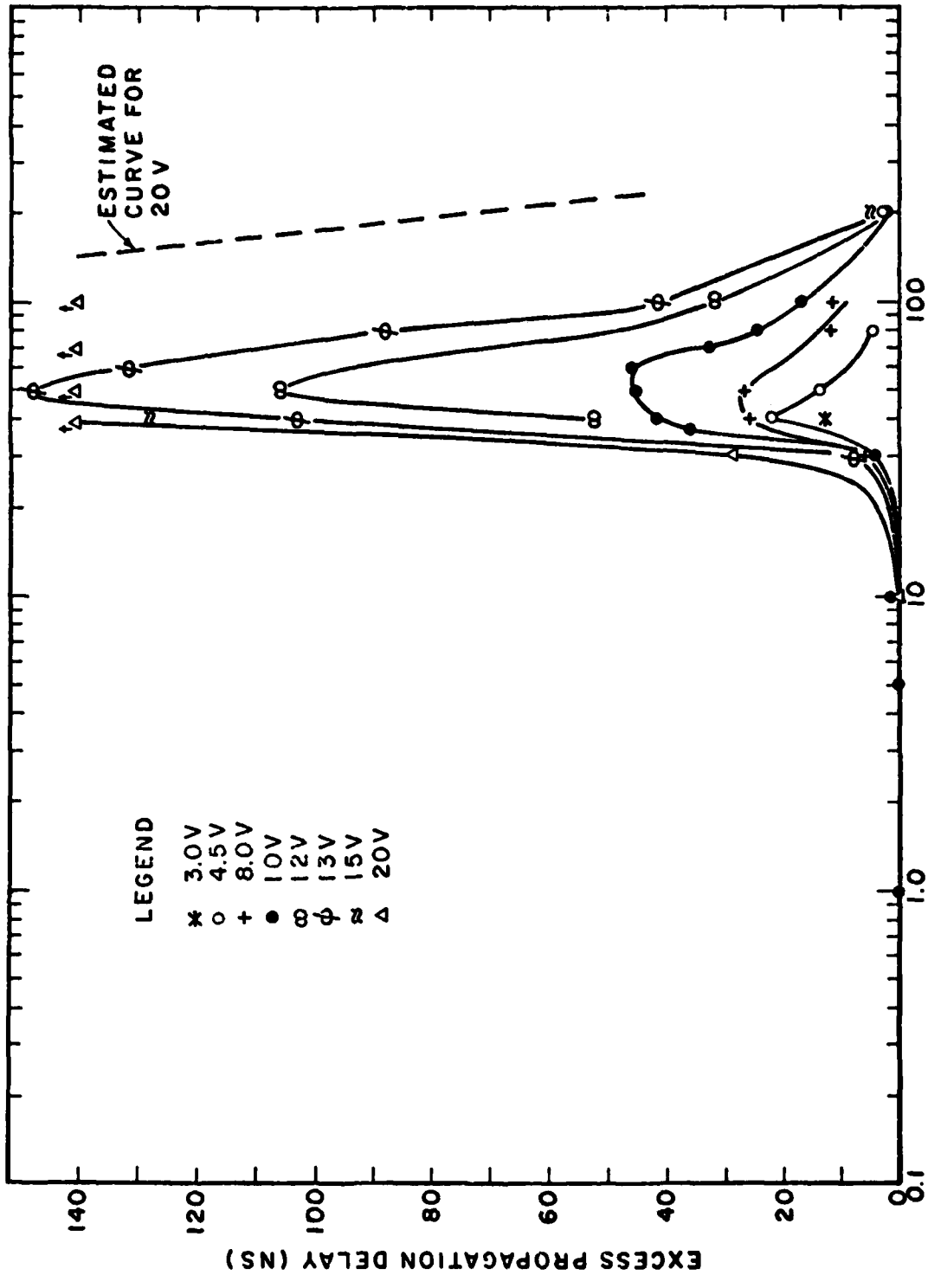


Fig. 29. Excess propagation delay time of gate 2 output.

investigated. It was determined that the phase had no noticeable effect on the rise time but did introduce changes in the delay time by an amount as large as one period of the interfering signal.

The average power supply current is plotted in Fig. 30. Notice that the average current drain on the power supply may increase significantly in the "resonance" region which, once again, extends from 30 to 100 MHz.

Some state transition times are tabulated in Table 13 for various cases where a clear transition was made from LOW to HIGH states. As with the rise time and excess propagation delay time, values of the state transition time can be relatively large compared to typical rise and propagation delay times.

Finally, a calculation was made of the average power delivered by the interference source. This was accomplished by first multiplying the instantaneous voltage and instantaneous current of the interference source, in order to obtain the instantaneous power delivered by the source, and then averaging the result. The average delivered powers for interference amplitudes of 0.5V and 20V were 1.4 mW and 540 mW, respectively. This range corresponds to the same range of absorbed power measured by McDonnell Douglas in their experimental study [1].

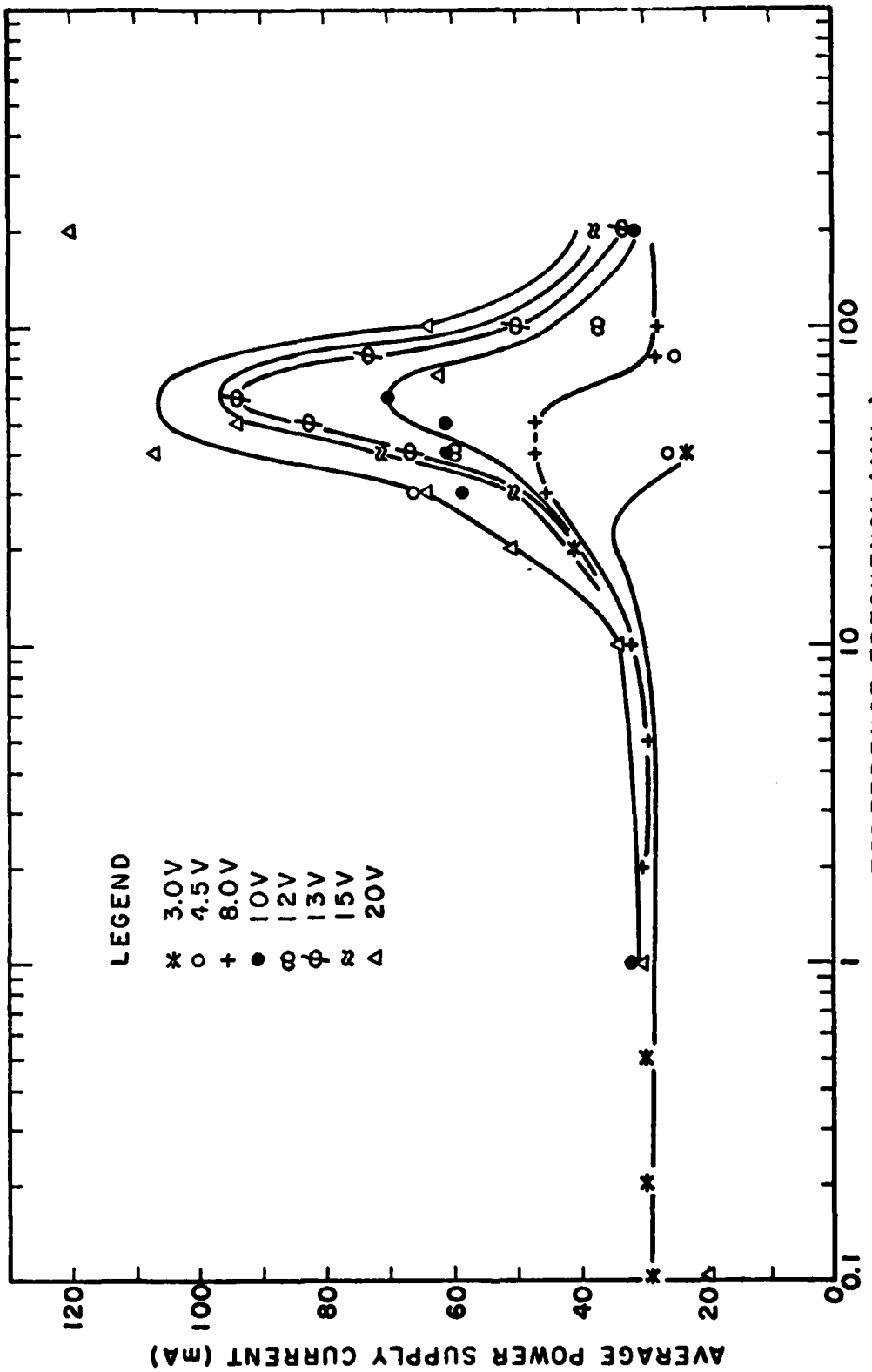


Fig. 30. Average power supply current.

Table 13

State Transition Time for Gate 2 Output

Interference Amplitude (V)	Interference Frequency (MHz)	State Transition Time (nS)
3	40	37
4.5	40	66
4.5	50	14
4.5	80	8
8	80	11
8	100	3
8	200	3
10	80	35
10	100	17
10	200	3
13	200	4
15	200	7

8. SUMMARY AND SUGGESTIONS FOR FUTURE WORK

This work has emphasized EMI upset in an integrated circuit 7400 TTL NAND gate due to sinusoidal interference injected in series with the gate output. Severe waveform distortions, capable of causing serious logic errors, were observed through computer simulation of the digital circuits involved. These results are in sharp contrast to the pure dc offsets reported by McDonnell Douglas [1]. We conclude that RF interference can pose a serious threat to the successful operation of digital circuits.

The work reported herein is merely a small step forward towards understanding interference effects in digital equipments. As far as the 7400 TTL NAND gate is concerned, it is desirable to study in greater depth the consequences of interference in the power line and ground connections. Also, other interference waveforms, such as pulses and spiked transients, should be investigated.

The 7400 TTL NAND gate represents merely a single technology and a single type of digital circuit. Other types of technologies, such as ECL, CMOS, and IIL, need to be studied. Also, the commonality between the NAND gate and other logic circuits, such as OR, AND, and NOT gates, should be pursued.

It would be highly desirable to model the various logic gates in terms of circuits containing considerably fewer semiconductor devices. This may be possible using the macromodel concept which has been successful in generating relatively simple circuit models for

operational amplifiers. Once simpler models have been devised, it would be desirable to combine them in an effort to model more complicated combinations of logic circuits. In this way, it may be possible to arrive at EMI performance curves for relatively sophisticated digital equipments.

Finally, all of the above should be supplemented by an experimental effort in order to validate analytical and computer simulation results.

REFERENCES

1. "Integrated Circuit Electromagnetic Susceptibility Handbook," Report MDC E 1929, 1 August 1978, McDonnell-Douglas Company.

2. "User's Guide for SPICE," Electronic Research Laboratory, College of Engineering, University of California, Berkeley.

3. "Digital Integrated Electronics," H. Taub and D. Schilling, (McGraw-Hill, 1977).

APPENDIX A: CALCOMP PLOTS OF REPRESENTATIVE OUTPUT WAVEFORMS

The Calcomp plots corresponding to the waveforms sketched in Figures 14-18 are presented in Figures A.1 - A.5. However, as defined in Fig. 9, the transition from the fourth to first quarters is shown in addition to the transition from the third to fourth quarters. In Fig. A.1 the two inputs to gate 1, the output of gate 1, and the output of gate 2 are plotted while in Figures A.2 - A.5 only the two inputs to gate 1 and the output of gate 2 are plotted.

As indicated on the plots, the vertical voltage scale is multiplied by 10^{-1} while the horizontal time scale is multiplied by 10^{-8}. The sketches shown in Figures 14-18 are seen to capture the essential features of the Calcomp plots. In addition, it is seen that the leading edge of the gate 2 output, corresponding to the transition from the third to fourth quarters, differs markedly from the trailing edge of the gate 2 output, corresponding to the transition from the fourth to first quarters.

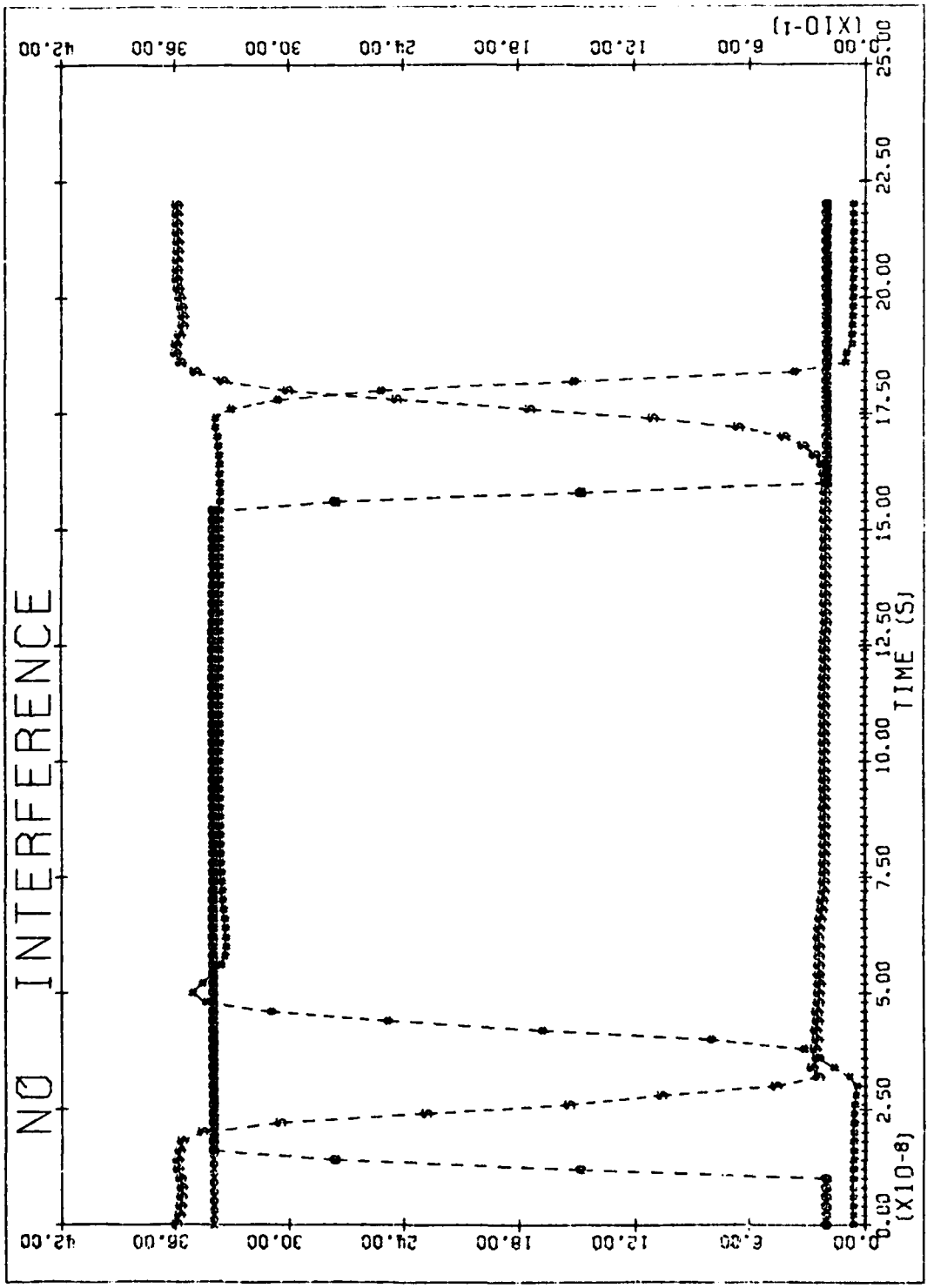


Fig. A.1. Typical behavior of the two gates without interference.

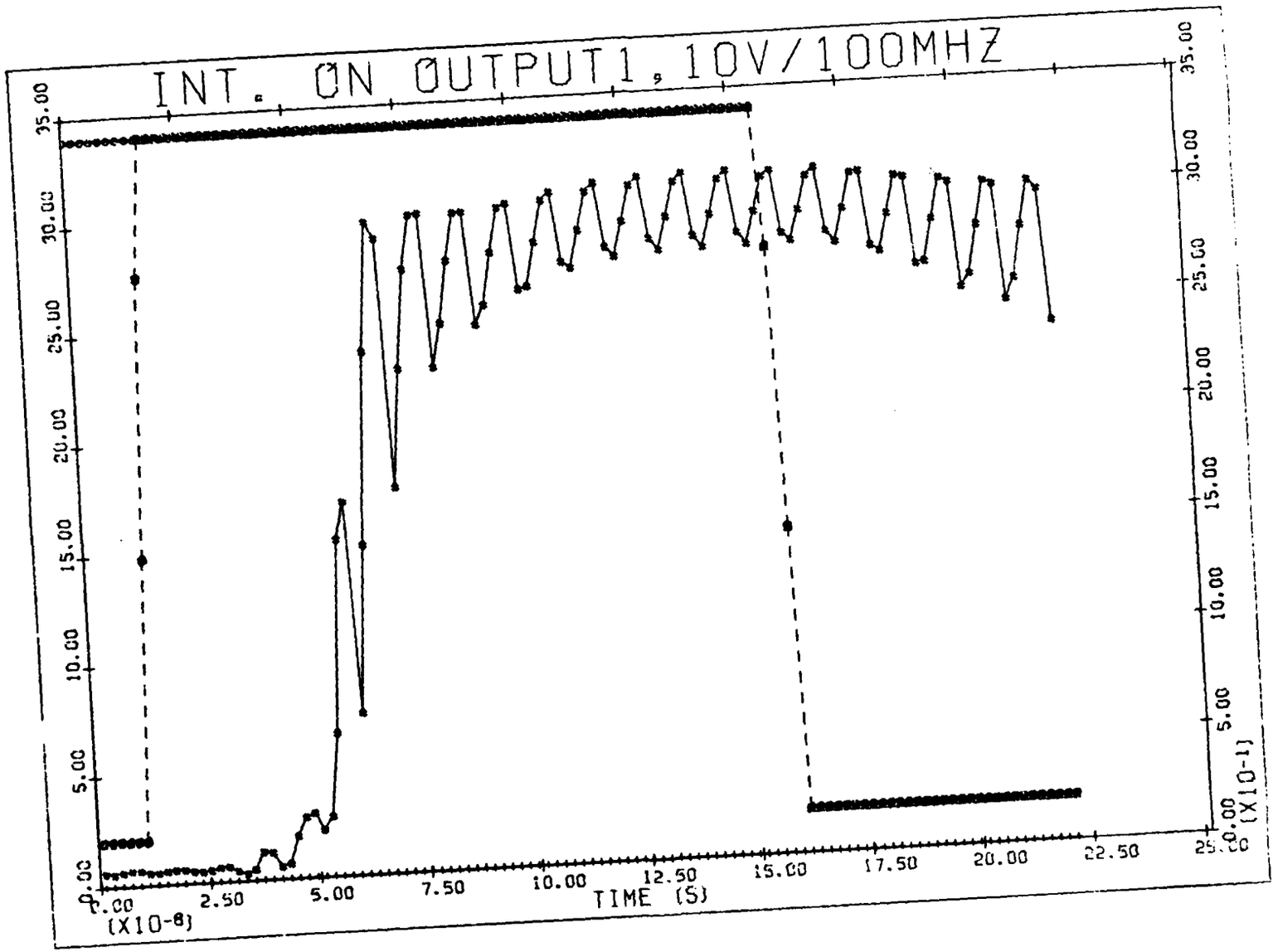


Fig. A.2. Output of gate 2 remains in HIGH state.

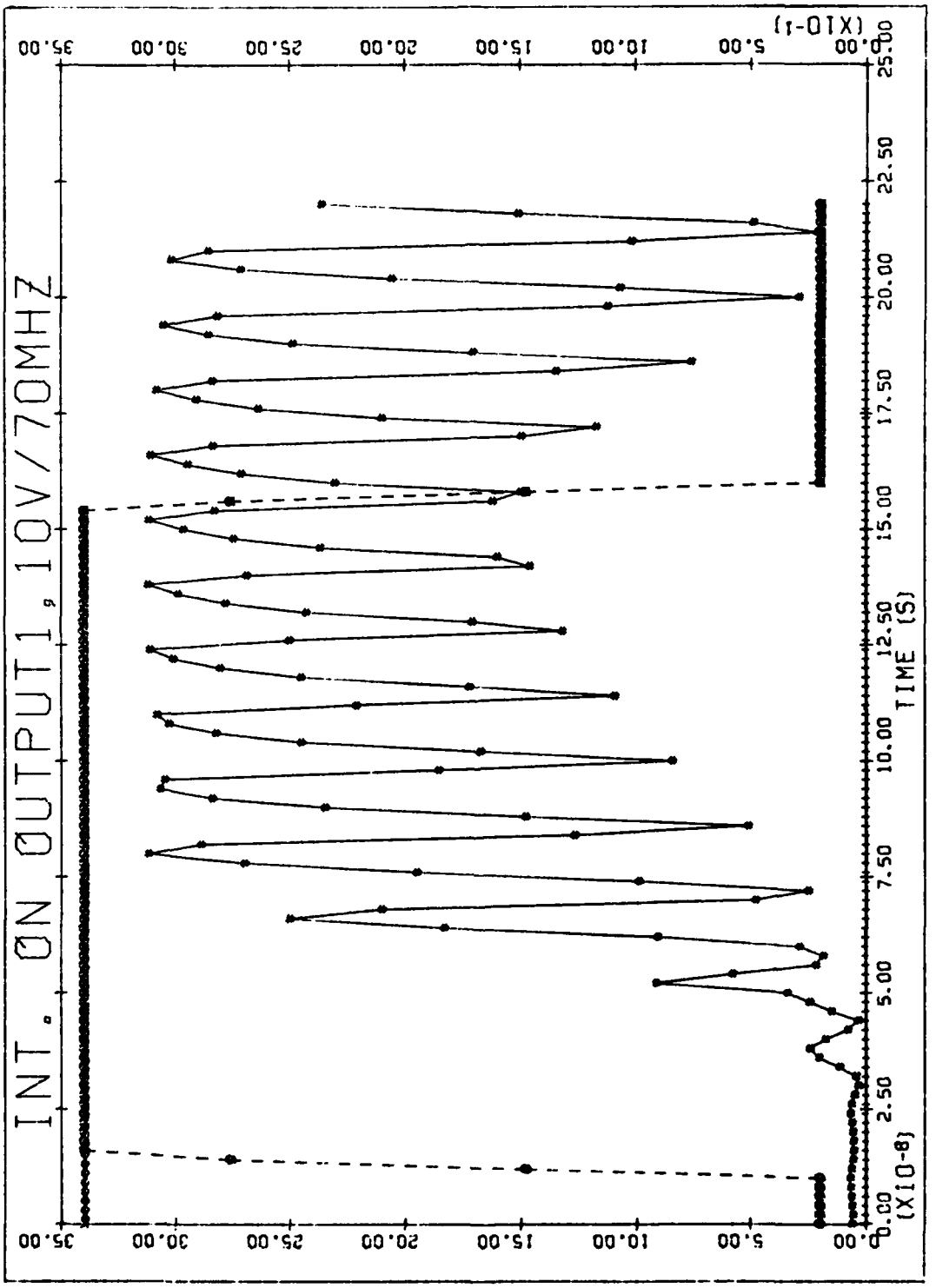


Fig. A.3. Output of gate 2 enters UNDEFINED area.

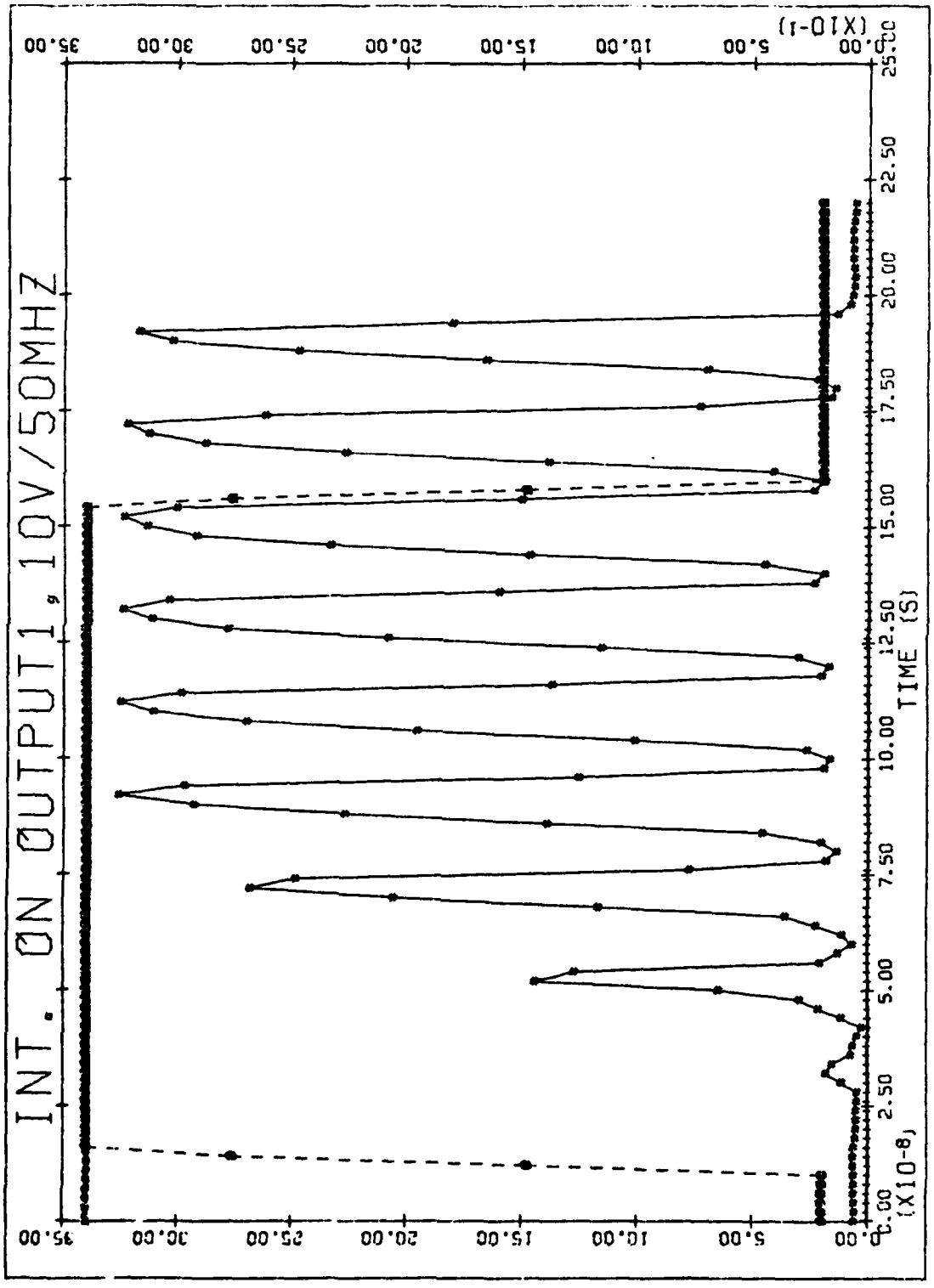


Fig. A.4. Output of gate 2 drops to the LOW state.

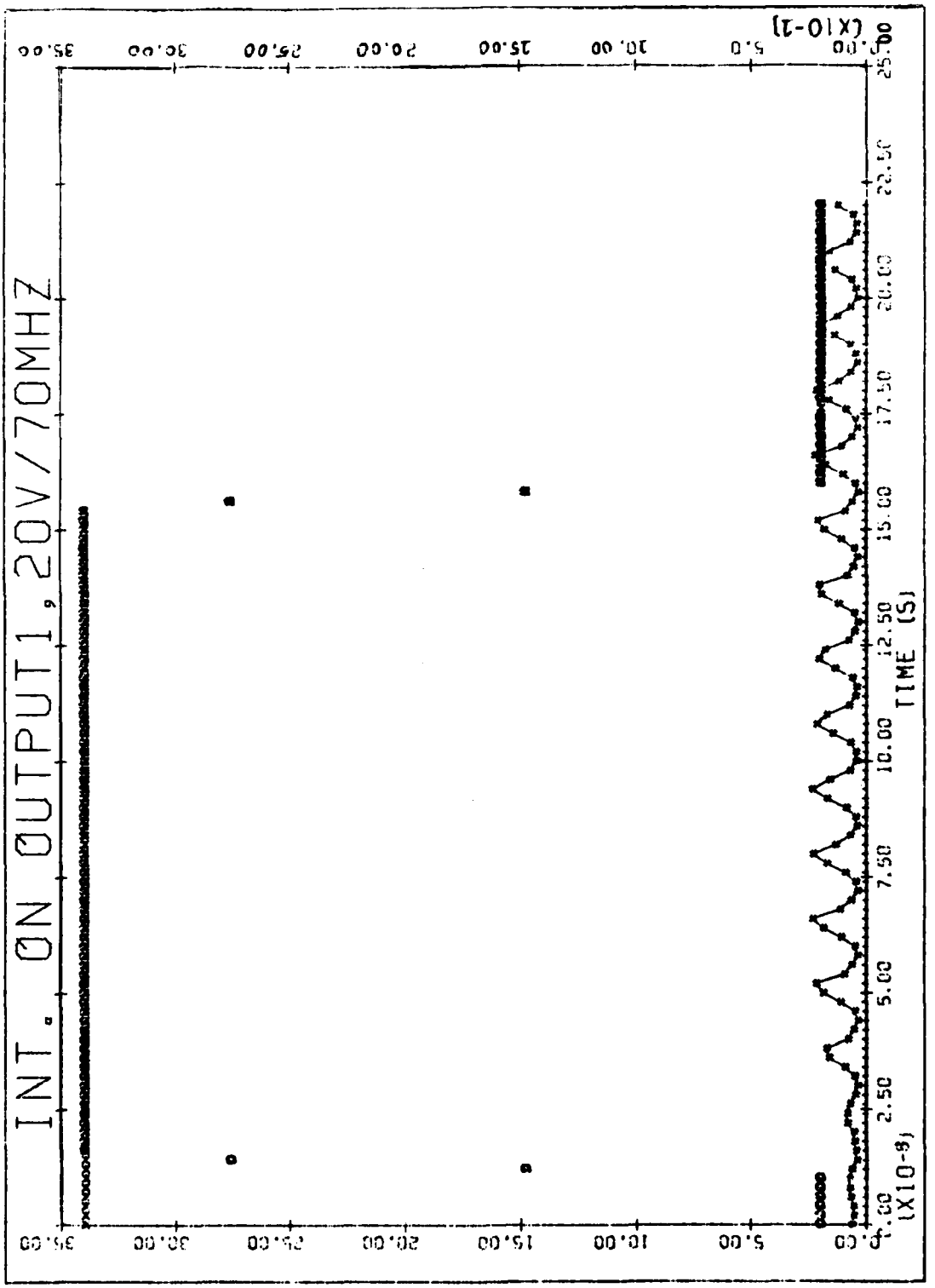


Fig. A.5. Output of gate 2 remains in the LOW state.

APPENDIX B: SAMPLE SPICE COMPUTER PROGRAM

```
1)TRANSIENT ANALYSIS OF NAND GATE
2)*
3)* RESISTORS
4)R1 2 9 4.38K
5)R2 9 4 1.43K
6)R3 9 6 0.116K
7)R4 5 0 1.03K
8)* DIODES
9)DIN1 0 1 STAN
10)DIN2 0 10 STAN
11)D3 7 8 DIO3
12)* TRANSISTORS
13)Q11 3 2 1 TR1
14)Q12 3 2 10 TR1
15)Q2 4 3 5 TR2
16)Q3 6 4 7 TR3
17)Q4 8 5 0 TR4
18)* DESCRIPTION OF LOAD STAGE
19)* RESISTORS
20)R5 9 13 0.438K
21)R6 9 15 0.143K
22)R7 9 17 0.0116K
23)R8 16 22 0.106K
24)* DIODES
25)DIN4 22 11 STANL
26)DIN5 22 12 STANL
27)D6 18 19 DIO3L
28)*TRANSISTORS
29)Q51 14 13 11 TR1L
30)Q52 14 13 12 TR1L
31)Q6 15 14 16 TR2L
32)Q7 17 15 18 TR3L
33)Q8 19 16 22 TR4L
34)* LOAD RESISTOR AND CAPACITOR FOR LOAD STAGE WITH FAN_OUT = 10
35)* WITH LOAD TIED TO GROUND
36)* LOAD RESISTOR
37)RLL 23 22 0.4K
38)* LOAD CAPACITOR
39)CLL 23 22 15PF
40)* MODEL CARDS FOR DIODES AND TRANSISTORS OF FIRST STAGE
41).MODEL STAN D(RS=600HMS TT=0.1NS CJO=2PF PB=0.6V BV=40V IS=1E-16)
42).MODEL DIO3 D(RS=300HMS TT=0.1NS CJO=2PF PB=0.6V BV=40V IS=1E-16)
43).MODEL TR1 NPN(BF=0.316 BR=0.02 RB=680HMS TF=0.39NS TR=100NS RC=100HMS
44)+RE=10MH VA=200V C2=1000 C4=1 CCS=2PF CJE=1PF PE=0.7V ME=0.33
45)+CJC=0.5PF PC=0.5V MC=0.33 KF=6.6E-16)
46).MODEL TR2 NPN(BF=19.8 BR=0.06 RB=750HMS TF=0.39NS TR=100NS
47)+RE=10HM VA=200V VB=200V C2=1000 C4=1 CCS=2PF CJE=2PF PE=0.7V ME=0.33
48)+CJC=1PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-16)
49).MODEL TR3 NPN(BF=17.2 BR=0.082 RB=700HMS RC=100HMS TF=0.39NS TR=100NS
50)+RE=100HM VA=200V C2=1000 C4=1 CCS=2PF CJE=2PF PE=0.7V ME=0.33
51)+CJC=1PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-16)
52).MODEL TR4 NPN(BF=21.7 BR=0.106 RB=800HMS RC=100HMS TF=0.39NS TR=100NS
53)+RE=10HM VA5200V VB=200V C2=1000 C4=1 CCS=2PF CJE=2PF PE=0.7V ME=0.33
54)+CJC=1PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-16)
```

```
55)* MODEL CARDS FOR DIODES AND TRANSISTORS OF LOAD STAGE
56).MODEL STANL D(RS=600HMS TT=0.1NS CJO=20PF PB=0.6V BV=40V IS=1E-15
57)+IBV=0.01)
58).MODEL DIO3L D(RS=30HMS TT=0.1NS CJO=20PF PB=0.6V BV=40V IS=1E-15
59)+IBV=0.01)
60).MODEL TR1L NPN(BF=0.316 BR=0.02 RB=6.80HMS TF=0.39NS TR=100NS RC=10HM
61)+RE=0.10HM VA=200V VB=200V C2=1000 C4=1 CCS=20PF CJE=10PF PE=0.7V
62)+ME=0.33 CJC=5PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-15)
63).MODEL TR2L NPN(BF=19.8 BR=0.06 RB=7.50HMS RC=10HM TF=0.39NS TR=100NS
64)+RE=0.10HM VA=200V VB=200V C2=1000 C4=1 CCS=20PF CJE=20PF PE=0.7V
65)+ME=0.33 CJC=10PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-15)
66).MODEL TR3L NPN(BF=17.2 BR=0.082 RB=70HMS RC=10HM TF=0.39NS TR=100NS
67)+RE=0.10HM VA=200V VB=200V C2=1000 C4=1 CCS=20PF CJE=20PF PE=0.7V
68)+ME=0.33 CJC=10PF PC=0.5V MC=0.33 KF=6.6E-16 IS=1E-15)
69).MODEL TR4L NPN(BF=21.7 BR=0.106 RB=80HMS RC=10HM TF=0.39NS TR=100NS
70)+RE=0.10HM VA=200V C2=1000 C4=1 CCS=20PF CJE=20PF PE=0.7V
71)+ME=0.33 CJC=10PF PC=0.5V MC=0.33 KF=6.6E+16 IS=1E-15)
72)* VOLTAGE SOURCES
73)VIN1 20 0 PULSE(3.4 0.2 155NS 5NS 5NS 290NS)
74)VIN2 10 0 PULSE(0.2 3.4 10NS 5NS 5NS 140NS)
75)VCC 21 0 DC 5
76)VPLUS 12 22 DC 3.4
77)* INTERFERENCE SOURCES
78)VINT1 1 20 DC 0
79)VINT2 9 21 DC 0
80)VINT3 8 11 SIN(0.0 10V 100MEGHZ 0.0 0.0)
81)VINT4 0 22 DC 0
82)VINT5 19 23 DC 0
83)* OUTPUT PROCEDURE
84).TRAN  1NS 150NS
85).OPTIONS LIMPTS=10000 LIMTIM=4 RELTOL=0.1 NOMOD NOPAGE
86).PLOT TRAN V(1,20) V(8,11) V(9,21) (-20,20) V(20) V(10) V(8) V(19) V(11)
87).PLOT TRAN V(1) V(2) V(3) V(4) V(5) V(6) V(7) V(9)
88).PLOT TRAN V(13) V(14) V(15) V(16) V(17) V(18)
89).PLOT TRAN I(VIN1) I(VIN2) I(VINT3) I(VCC) I(VPLUS) I(VINT4) I(VINT5)
90).PRINT TRAN V(20) V(10) V(8) V(1,20) V(8,11) V(9,21) V(19) V(11)
91).PRINT TRAN V(1) V(2) V(3) V(4) V(5) V(6) V(7) V(9)
92).PRINT TRAN V(13) V(14) V(15) V(16) V(17) V(18)
93).PRINT TRAN I(VIN1) I(VIN2) I(VINT3) I(VCC) I(VPLUS) I(VINT4) I(VINT5)
94).END
```

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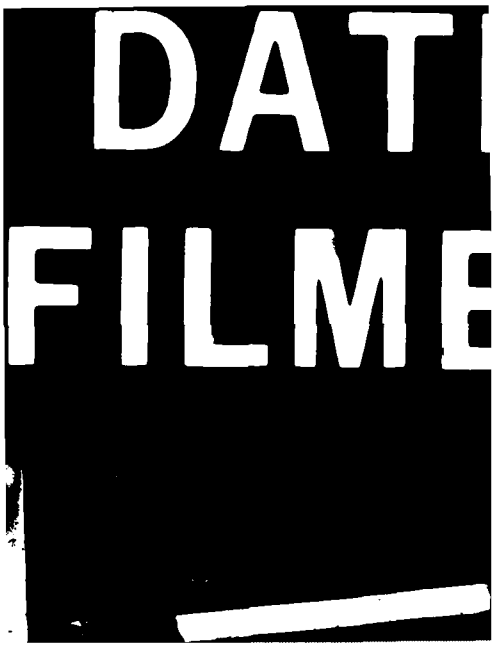
DAT
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