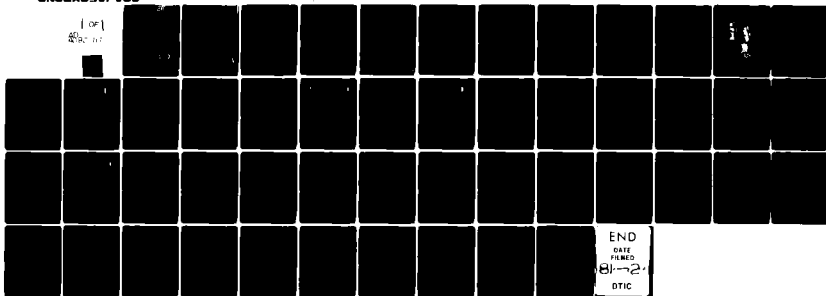


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TEN-BIT RESOLUTION PCM ENCODER

(Falling Sphere Experiment)

Richard F. Buck
Electronics Laboratory - D.E.T.A.
Officer of Engineering Research
Oklahoma State University
Stillwater, Oklahoma 74078

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unit are covered; the report is written to serve as a technical manual for the equipment, and also covers an associated test set.

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SUMMARY

The OSU Model C40BE02 ten-bit PCM encoder was developed to improve data resolution obtainable from the Accumetrics ten-inch falling sphere, used by AFGL to measure atmospheric density. Design objectives included minimal size, weight, and power consumption, with the ability to withstand the anticipated environment for the instrument within which the component is to be installed.

The serial PCM output is in bi-phase level form; one minor frame consists of sixteen ten-bit words at a data rate of 20 kilobits per second. Fifteen analog data words can be accommodated with bipolar levels of -5 to +5 volts dc. To permit transmission of housekeeping monitor data, a major frame length of eight minor frames is used. An internal multiplexer for seven slowly varying analog monitors within the 0 to +5vdc range subcommutates data into a selected word within the minor frame. Primary data words are sampled at a rate of 125 samples per second; housekeeping data is transmitted at a rate of approximately 16 samples per second.

Use of CMOS logic throughout and incorporation of a dc-to-dc inverter power supply within the coder permitted development of a unit with power demand of only 60 milliamperes at $+28 \pm 4$ volts dc which weighs only 385 grams and occupies 305 cubic centimeters, approximately the volume of the earlier unit which it replaces. Wire-wrap construction and plug-in logic elements are used to facilitate maintenance.

To assist in initial adjustment and testing of the coder, an associated test-set (OSU Model C40BC01) was also designed and built in conjunction with the prototype system.

This report is written to serve as a technical manual, to be used with the equipment. Details of the circuit design, theory of operation, adjustment and test procedures, and a complete parts list for both coder and test-set are included. An evaluation of the tests performed on the prototype unit is also included for reference.

LIST OF CONTRIBUTORS

The following staff members (listed alphabetically) from the Oklahoma State University Electronics Laboratory (Division of Engineering, Technology, and Architecture) contributed to the work described in this report:

Richard F. Buck	Darrell L. Haston
Joseph M. Cooper	L. Orion Schmitt
Donald G. Dale	Rosalee I. Stafford
Tom B. Gwin	Jerry R. Waughtal
Claude M. Gwinn	Joe B. Zinn

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1.0 INTRODUCTION

1.1 The OSU model C40BE02 16-channel PCM encoder was developed specifically for use with the Accumetrics Falling Sphere 3-axis accelerometer. The coder generates a series of pulse-code modulated (PCM) words with 10-bit resolution (approximately 10 mv per bit), and is used to provide a PCM telemetry signal, from the 10" diameter falling sphere instrument to the ground receiving system. The instrument is used to obtain atmospheric density data by measurements of deceleration (due to drag forces) on a smooth balanced sphere as it falls back to the earth's surface, after ejection from a rocket vehicle. A sensitive 3-axis piezo-electric accelerometer within the sphere senses forces and, through charge amplifiers, provides four separate scale-factor output signals from the X and Y axes (transverse in fall) and 3 separate scale factor signals from the Z axis (longitudinal in fall). Additional signals are developed within this sphere for indication of nutation of the sphere, and for various housekeeping functions. Analog signals from the 3-axis accelerometer instrument are converted to 10-bit digital form and suitably formatted for transmission by the coder. The PCM wave train is then used to frequency modulate an S-band transmitter located within the sphere. The composite telemetry signal is radiated from a special flush-mounted S-band antenna array on the surface of the sphere, received by the ground receiving system, and the PCM data recovered from the demodulated carrier frequency. The PCM wave train so recovered is then decoded, to retrieve the original data transmitted.

1.2 The PCM wave train from the coder has the following characteristics:

Format: Biphase-Level Code (an NRZ-Level signal is also developed by the coder and may be used as an alternate transmission form).

Bit Rate: 20.00 Kilobits per second

Word Length: 10 bits; encoded most significant bit first.

Frame Length: Minor frame of 16 words (15 data words plus synchronization)

Subcommutation Capability: 7 analog housekeeping signals maximum, in 0 to +5v data range.

Minor Frame Synchronization Code: 110 111 000 0 (standard 10-bit Barker code). (For maximum reliability in ground station synchronization, the minor frame synchronizing code is inverted in alternate frames, thus appearing as 001 000 111 1 every other frame.)

Major Frame Length: 8 minor frames of 16 words each.

Subframe Synchronization: Equivalent to -5.1v; subframe sync word
000 000 000 0.

The analog to digital converter used within this sphere coder is operated in a bipolar mode, and sensing is such that a -5.00v analog input signal generates a bit stream of 10 consecutive zeros; +5.00v input generates a word of 10 consecutive 1's.

If the subcomm capability is utilized, advantage is taken of the fact that all housekeeping monitors are in the range of 0 to +5v data span and the sub-frame synchronization word is equivalent to a -5v input signal, thus enabling simple synchronization of the subcommutator by choice of a synchronizing pattern which can never appear within the subcommutated data format.

1.3 Normal data assignments within the PCM formats are as follows:

<u>Word</u>	<u>Data</u>
0	Frame synchronization (alternate frame inversion; 10-bit Barker code) (110 111 000 0/001 000 111 1)
1	Low gain X-channel
2	Mid-low gain X-channel
3	Mid-high gain X-channel
4	High-gain X-channel
5	Low-gain X-channel
6	Mid-low gain Y-channel
7	Mid-high gain Y-channel
8	High-gain Y-channel
9	Low-gain Z-channel
10	Mid-gain Z-channel
11	High-gain Z-channel
12	Unassigned Spare Word
13	Nutation Signal
14	Sphere Voltage Monitor
15	Housekeeping Monitor

Words 12, 14 and 15 may be used for housekeeping monitors in applications where little housekeeping data is required. If additional housekeeping functions are present, the subcommutated data frame may conveniently be inserted in the position of word 15 by appropriate jumpers on the input data connector to permit a total of 9 monitors (words 12, 14, and seven sub-commutated monitors on word 15).

1.4 Physical characteristics: the complete sphere encoder, including an internal dc-to-dc power conversion system, is enclosed within a rectangular

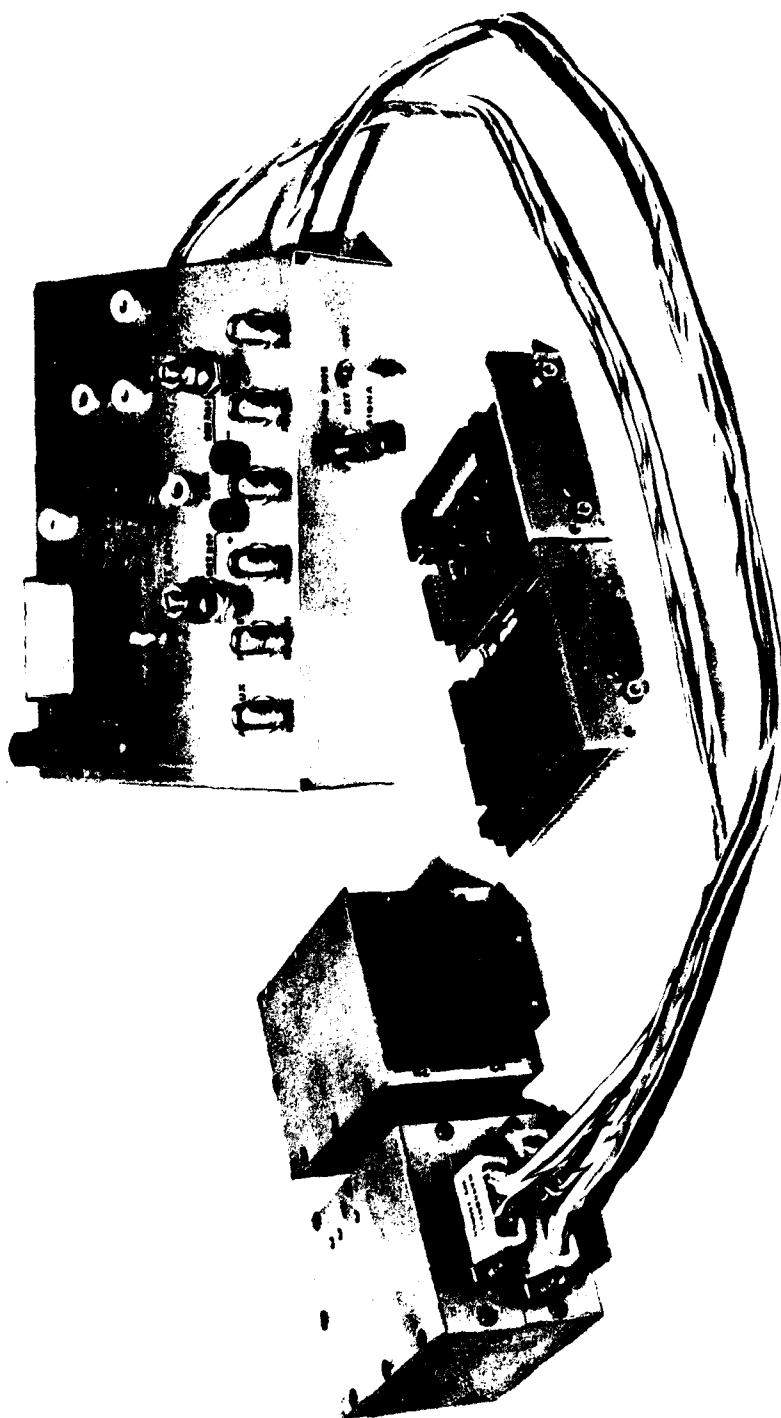


Figure 1. 10-Bit Coder (and Associated Test Set)

case with dimensions of 8.89 centimeters ($3\frac{1}{2}$ ") long by 6.35 centimeters ($2\frac{1}{2}$ ") wide by 5.4 centimeters ($2\frac{1}{8}$ ") high, exclusive of mating connectors and mounting flange. Physical mounting is accomplished by means of four 4-40 mounting screws through the external flange, which has dimensions of 11.43 cm ($4\frac{1}{2}$ ") long by 6.35 cm ($2\frac{1}{2}$ ") wide. Mounting screw holes are in a rectangular pattern, with dimensions of 9.906 cm (3.9") by 2.159 cm (.85"). A photograph of the completed unit is shown in Figure 1. Two connectors are provided across the smaller face (end) of the instrument. Input data signals (15 main signals plus 7 subcommutated signals) are applied to S0101, a Cannon DB-25P connector, requiring a DB-25S as a mating connector. (The data connector also incorporates single ground on pin 17 and the mixed analog subcommutation output signal on pin 25.) An analog signal in the range of 0 to +5v, indicating condition of the batteries supplying power to the instrument, is provided on pin 16. Primary data assignments are to pins 1 through 15, for data words 1 through 15 respectively. Input data to subcommutated monitors 1 through 7 are applied on pins 18 through 24. Total weight is 385 grams.

A second connector, S0102, a Cannon DA-15P connector (mating connector DA-15S), is provided for DC power input to the system, and also carries the PCM output wave train signal on two end pins. (The second connector also supplies a series of monitor points for use in set-up and evaluation of the coder; it should be noted that these pins are provided only for test purposes and should not be connected when the coder is installed in the instrument for flight.)

1.5 The decoder has been designed for normal operation over the range of environmental conditions anticipated as possible for the rocket payload installation proposed. Specifications may be summarized as follows:

<u>Parameter</u>	<u>Limits</u>
Altitude	Unlimited
Temperature	0° to +65°C
Vibration	0 to 10 g's, 20 to 2000 cycles, all 3 axes
Shock	20g peak, all 3 axes
Voltage	+28v; $\pm$ 5v dc
Current Requirement	60 ma nominal
Input voltage data limits:	Main words -5.00 to +5.00v dc
Subcommutator	0 to +5.00v dc

2.0 GENERAL DESCRIPTION OF CODER CIRCUITRY

Reference should be made to Figure 2, the block diagram (OSU B40BE01), for a generalized explanation of electronic circuitry required within the PCM coder.

2.1 The timing system for the coder is derived from an internal CMOS clock oscillator. The basic clock frequency is 320 KHz; this is successively divided down to provide the bit clock rate of 20.00 KHz, the word clock rate of 2.00 KHz, the minor frame clock rate of 125 Hz, and the subcommutated frame rate of 15.625 major frames per second. All necessary timing signals for the remainder of the unit are derived from some combination of these clocking signals. Countdown is done by a CMOS dual binary counter, with appropriate feedback where required for non-binary division ratios.

2.2 Input data is multiplexed by two cascaded 8-line input analog multiplex chips. These are alternately enabled with every 8th word, and each multiplex chip uses the 1, 2, and 4 address lines to progressively sequence through the 16 words of the minor frame. The multiplexed analog signal, switched at the minor frame word rate, is then fed through an operational amplifier (as a buffering circuit) to the analog-to-digital converter.

A third 8-line input analog multiplex chip is enabled constantly and switched at minor frame rate (125 HZ) by the 1, 2, and 4 subcomm frame counter outputs to permit a sequence of 8 minor frames - this permits slowly varying housekeeping signals to be multiplexed into the data stream. Seven such inputs are provided; the last remaining input to the subcomm multiplexer is internally saturated at the negative end to generate an output word from the analog-to-digital converter of 10 consecutive zeros, for use as the frame synchronizing signal for the subcommutator.

2.3 Multiplexed data, after passing through the analog buffer stage, is fed as the analog input signal to a 12-bit analog-to-digital converter. Only the 10 most significant bits from this 12-bit converter are used for the digital output signal. The analog signal is multiplexed so as to switch data input at the end of each word. A convert command is generated during the time of the 3rd bit within each word, and used to initiate a conversion within the analog-to-digital converter unit. (This permits the multiplexed analog signal to settle to a steady state value between transitions.) A time interval of approximately 600 microseconds is required for conversion to all 12 possible bits. At the end of the conversion cycle, the binary value is held on 12 parallel output

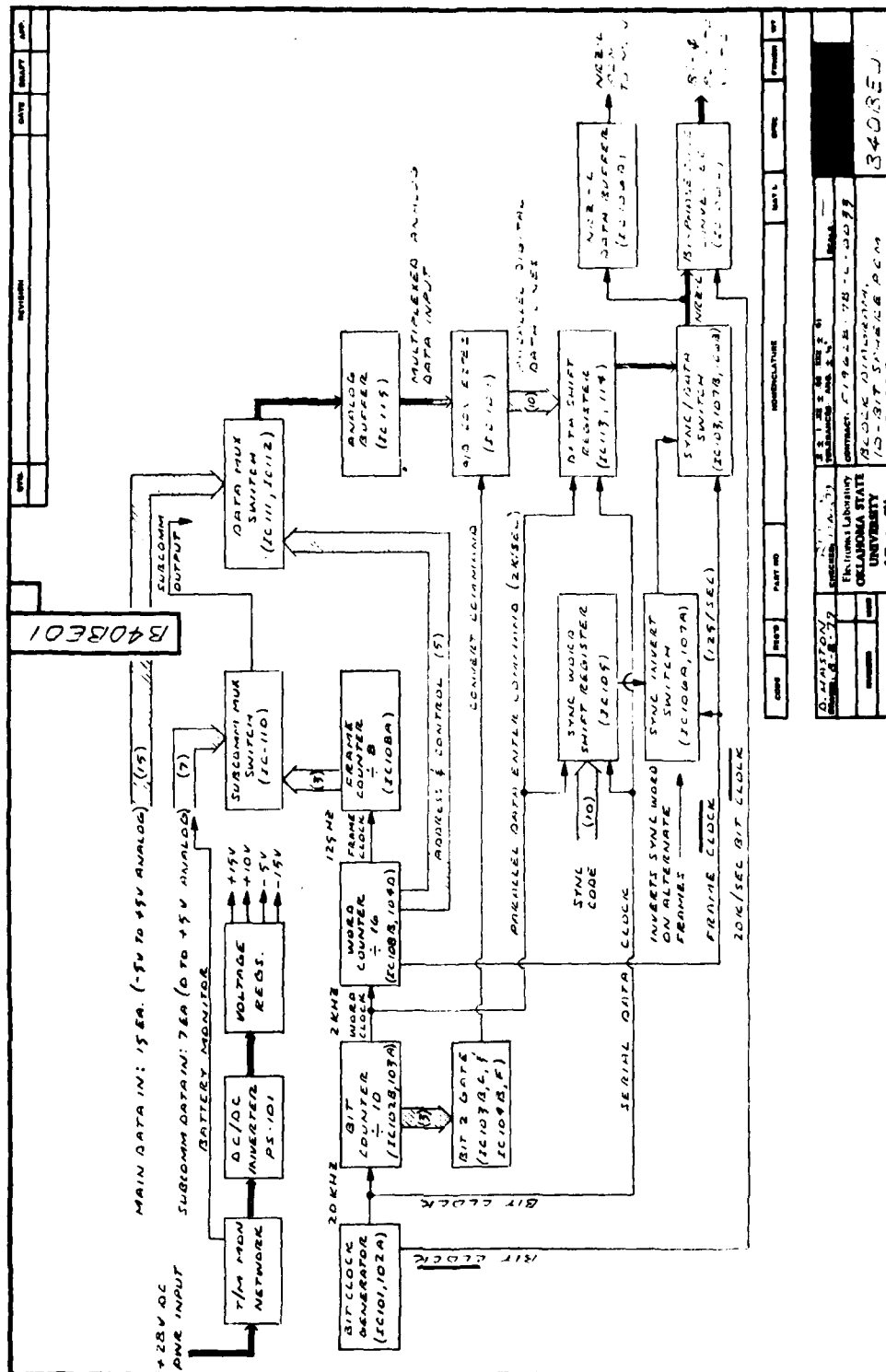


Figure 2. Block Diagram, 10-Bit Sphere Encoder

data lines until receipt of the next convert command, at which time output lines are reset to 0 and the conversion process is repeated. Since conversion starts 150 microseconds after the start of each word and requires approximately 300 microseconds for conversion, a full conversion procession is normally completed approximately 50 microseconds prior to use in the digital data stream.

2.4 Synchronization of the digital data into the desired data stream is accomplished by entering data into an array of shift registers at the end of each word. "Parallel enter" commands at the end of each word then transfer data from the sync word generator and the analog-to-digital converter into the shift registers. A serial data clock (at 20 KHz bit rate) then clocks the stored data from the shift registers into the output data stream in NRZ-L code.

The synchronizing word is generated (in NRZ-L code) at the word rate (2 KHz) by IC105. It is inverted on alternate frames such that it changes from 110 111 000 0 to 001 000 111 1, and it is clocked out once per frame.

Since the A-to-D converter signal is presented with an input voltage of greater than -5v once per minor frame rate, a sequence of 0's is generated, corresponding to the 16th word of each sequence. The sync/data switch gate circuitry is enabled for 1 word, once per frame, at the proper time to insert the desired synchronizing word in the position occupied by all 0's (at word 16) to the data shift register output. Since the synchronizing word is inverted in alternate frames, this results in a string of 15 data words followed by a normal synchronizing word, then 15 data words, followed by an inverted synchronizing word, then 15 data words again. The output signal of the sync/data switch is then a 16-word NRZ-Level data stream, containing the digital equivalent of all analog input words and the Barker-coded synchronizing word, which is inverted in alternate minor frames.

2.5 The NRZ-Level signal is available as a monitor for ease in checking system operation. The NRZ-Level signal is also mixed with the out-of-phase bit clock signal in the code converter, IC106C, in such a way as to reverse the second half of each bit, thus resulting in the conventional sense Biphase-Level PCM wave train out to the transmitter.

A passive RC network on the output of the biphase code converter is used for premodulation filtering, in order to optimize bandwidth required for transmission of the data stream over the telemetry link.

For applications where a narrower band transmission is desired, it is possible to transfer the premodulation filter and deviation control network

from the biphase code converter output to the NRZ-Level data buffer output, resulting in NRZ-Level modulation for the associated transmitter. This feature is provided for convenience in PCM/FM/FM modulation, when it is desired to transmit sphere data on a standard IRIG voltage-controlled oscillator, in combination with other data on the same transmitter.

2.6 All required operating voltages for the unit are generated internally by use of a dc-to-dc converter. Raw 28v battery power is fed into this converter and generates positive and negative 15v output levels, balanced to ground, at a capability of approximately 30 ma per side. The +15v supply is also dropped to +10v level for the major logic supply within the unit. The -15v signal is similarly dropped to a regulated level of -5.1v, for use as an "overranging reference" signal to the data multiplex chips.

The input 28v line to the dc-to-dc converter is also used to generate a battery monitor for telemetry, showing the status of the bus applying power to the falling sphere instrument. An offset zener regulator and voltage divider are provided such that a telemetry voltage of 0 to +5v span is provided for nominal input swings of plus 23 to plus 33 volts dc bus voltage.

3.0 THEORY OF OPERATION

The schematic diagram of the circuitry used for the 10-bit sphere encoder is shown in Figure 3 (OSU C40BE02), to which reference should be made during the explanation which follows. All CMOS logic is used throughout, in order to reduce power drain to the minimum from the battery source supplying common power to the instrument, telemetry, trajectory equipment, and encoder.

3.1 Basic timing for the entire unit is provided from a crystal-controlled CMOS oscillator, IC101. The HS-400 oscillator generates a 50% duty cycle square-wave timing waveform at a fundamental frequency of 320 KHz. In order to reduce this high frequency clock signal to the desired bit rate of 20 Kbt per second, one-half of IC102 (a CD4520B dual 4-stage binary counter) is used to divide the basic crystal frequency by a factor of 16. IC102A is constantly enabled (by application of +10v to pin 2) and thus advances as a ripple counter on the positive-going transition of each cycle of the basic crystal clock. Successive divisions of 2, 4, 8 and 16 result, with the output signal a 20 KHz per second square wave, taken from pin 6. Since the full division of 16 is desired in this 4-stage counter, no reset is required and pin 7 is grounded to permit the full count of 16. The output signal is a square wave at a fundamental frequency of 20 KHz per second. The signal is used directly with its normal phase as a clock signal to other portions of the circuit and, after inversion in IC104A, is also provided as an anticlock signal for code conversion elsewhere in the circuit.

The 20 KHz signal from IC102A is further divided to provide the word clock (2 KHz) by IC102B, the other half of the same CD4520B counter chip. This chip is similarly enabled on pin 10, permitting it to advance on the positive-going transitions, applied as clock signals to pin 9. Output signals are thus available at successive stages of the binary counter at normal rates of $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, and $\frac{1}{16}$ of the input clock rate. However, since division by 10 is desired, the output signals on pins 12 and 14 (division by 2 and by 8 of the input frequency) are combined in one section of IC103A, a quad 2-input AND gate, type CD4081B. An output signal is achieved from this gate only at the time at which both the 2 and 8 counts are positive-going, thus resulting in an output reset signal on every 10th pulse. This reset signal is applied back as a reset gate to pin 15, thus clearing the second half of the counter to zero and starting the next word count. The output word clock from pin 3 (at the reset gate) is also used as the clocking signal to the frame counter, and as a parallel entry signal to all shift registers, thus entering parallel data

into the shift registers at the end of each word. The word clock frequency is 2 KHz per second.

The 2 KHz word clock signal is used as input to IC108, a second dual 4-bit binary counter, type CD4520B. The first section (IC108B) of this binary counter operates to count successive words, dividing by a factor of 16 to provide the main frame clock rate of 125 Hz. Outputs from the 1, 2, and 4 division sections are used as addresses to the associated minor frame multiplexer; the output from the last stage (at a frequency of 125 Hz) is used both as an enabling gate to the multiplexer section and as the input clock to the next counter, IC108A, providing synchronization at subcommutator rates of 8 minor frames per major frame. Since the full possible count of 16 is desired in the IC108B portion of the counter, no reset is necessary and reset pin 7 is grounded.

Frame clock pulses from pin 6 of the minor frame counter are applied as input clocking signals to the 2nd half of IC108A, where they are counted down to provide 8 minor frames per major frame for the timing signal. Because a negative transition from pin 6 of IC108B occurs at the end of each minor frame, pin 9 is grounded and IC108A then advances on each such negative transition. Since the subcomm rate is only 1/8th that of minor frame rate, this counter is reset by returning the output of the 8th stage (pin 14) to "reset" pin 15, thus recycling the counter on every 8th minor frame. Output lines from 1, 2, and 4 division sections of this counter are taken as the address lines to the subcommutator multiplexer, IC110.

3.2 Input analog signal multiplexing is accomplished by a series of 3 identical 8-input multiplexing chips, type HI-1818A. Two of these chips, IC111 and IC112, serve to combine the 15 desired analog input signals into a single time multiplexed train. (The 16th position is returned to a negative 5.1v reference, in order to provide a blank input for later insertion of the frame synchronizing pulse.) The HI-1818A multiplex chip is enabled by a low signal on pin 3 and advance in sequence with addresses on A, B, and C (pins 16, 1, and 4 respectively), where all three logic 0's serve as reset, and each logic 1 serves as an advance address. The output at pin 6 from main frame word counter IC108B is a logic 0, at ground potential for the first 8 words, then transfers to a logic 1 (approximately +9.5v) for the next following 8 words. Use of this signal as the "enable" signal for IC111 permits successive advances at the outputs of IC108B to transfer the input signals desired for

words 1 through 8 of the main frame through the desired sequence during the time pin 3 is held at ground potential.

The same signal which is used as the enabling signal to IC111 is inverted by IC104D (one section of hex inverter chip, type 74C901). The inverted signal is applied as an enable pulse to IC112, and holds it in the "disabled" mode for the first 8 words, then enables it to advance in sequence for words 9 through 15 and for the timing interval for the synchronizing pulse, as the same address lines for A, B, C are successively applied to pins 16, 1, and 4. The time sequential analog signals from pin 12 of IC111 and IC112 are parallel connected and returned to ground through R107, a 470 Kohm resistor, to prevent floating output lines from the CMOS multiplexer. The resulting analog signal, consisting of successive signals for words 1 through 15 plus the frame sync interval, appears across R107 and is used as the input signal to IC115, a type MC1741S operational-amplifier, connected as a voltage follower with unity gain.

Multiplex power is provided from the $\pm 15\text{v}$ supply buses, and the logic reference voltage on pin 2 is provided from the $+10\text{v}$ bus of power supply. In order to protect the multiplexer chips against excessive high level input signals during the "power off" condition, a steering diode, CR104, is used in the power supply section to isolate the $+15\text{v}$ bus on pin 14.

The multiplexed signal is applied to the non-inverting input, pin 3 of IC115, and the output at pin 6 of the operational amp is returned directly to the inverting input, pin 2, in order to establish the desired unity gain condition. The buffered analog multiplexed output signal is also taken as an "analog multiplex monitor" through R109, a 10K isolation resistor, to pin 6 of S0102 as a convenience in observing proper operation of the multiplex signal. The buffered analog signal from pin 6 is also taken as the input analog signal to pin 26 of the analog-to-digital converter, IC109.

Housekeeping subcommutation is available through use of a third HA-1818A multiplex chip, IC110. This chip has its "enable" bus energized continuously, since only 8 signals are to be time-multiplexed at the subcommutation rate. Address lines for this 3rd multiplex chip are enabled at frame rate (rather than word rate) by taking 1, 2, and 4 addresses from IC108A of the subcommutator frame counter. The first seven input signals serve to multiplex housekeeping signals at minor frame rate from seven different housekeeping monitors; the last input is again returned to a -5.1v reference to provide 10 successive zeros as the frame synchronization pulse at the end of each subcommutation

cycle. The time multiplexed signal is taken from output pin 12, to pin 25 of S0101, for use elsewhere as desired. For proper operation of the unit, the subcommutated output signal from pin 25 of S0101 should be jumpered back to one of the unused main frame words; normally word 15 (pin 15 of S0101) would be chosen for this purpose. As in the case of the main frame subcommutator, diode steering is used on the +15v bus to prevent potential damage of IC110 by application of excessive voltage input data words at times when the coder is not energized.

3.3 Conversion of the time multiplexed analog signal wave train to the desired digital form is accomplished in IC109, a Datel ADC-H12-BGC analog-to-digital converter.

Conversion of each piece of analog input data is desired once per word; in order to achieve conversion of the analog voltage of the proper time, a "conversion command" pulse must be applied to pin 21 of IC109 to start conversion. In order to enable the analog signal to settle to a steady-state value after time-multiplexing, a slight delay is desired for this conversion command. IC103B and C and IC104B and F are used to derive a "convert command" signal at the desired time with respect to the word clock pulse in the following manner: The "divide-by-2" timing signal is used as one input, to pin 6 of AND gate 1103B. The second input signal to this gate is provided by the wave form from the "divide-by-4" output, inverted by IC104F and applied to pin 5. Since the gate passes signals during the portion of time when both signals are positive, the output at pin 4 of IC103B is a positive going signal commencing at the start of bit 2 and terminating at the end of bit (3)? of each successive word in the main frame. This signal is taken as one of the inputs to IC103B, on pin 13. The second input signal to IC103C is obtained by inverting the "1's" address through IC104B. AND gate 103C then provides a "convert command" signal one bit (50 microsec) in time duration, commencing at the start of bit 3 and ending at the end of bit 3. This "convert" signal fills the necessary criteria of a positive-going pulse a minimum of 50 microsec wide as the "start" signal to the analog-to-digital converter.

At the end of the "start" signal, the analog-to-digital converter starts conversion by the successive approximation technique, beginning with the most significant bit. Internal clocking within IC109 establishes one conversion each 25 microsec; the full 12 bits of conversion are thus possible within 300 microseconds following the trailing edge of the start signal. At the end of the 12th conversion, the analog-to-digital converter commands itself into the "off"

mode. Internal latches provide a parallel line 12-bit binary-valued signal on pins 2 through 13. Zero volts indicates logic "0"; +10v indicates logic "1" for these output lines. Although the converter has been disabled at the end of the 12th conversion (by the "End Of Conversion" command on pin 16, fed back to "Mode" control pin 17), the output lines are held at the latched values resulting from the conversion process. Only the 10 most significant bits (pins 2 through 11) are utilized in this converter. These signals will remain present as parallel lines on the output until the "start" pulse is received, 1 word later.

The analog-to-digital converter is provided with both "zero" adjust and "gain" adjust potentiometers, R106 and R104 respectively, in order to permit adjustment of the converter sensitivity to the desired range. Note that, since no balance control is supplied to the voltage follower, IC115, any residual zero offset at the output of the voltage follower (nominally approximately 3.5 mv in level) is compensated for by "zero" adjust pot, R106.

The analog-to-digital converter is placed in the desired mode of operation (-5v to +5v bipolar input) by applying input data to pin 26 and jumpering pins 24 and 25 together to set the desired scale factor.

Note that, in this portion of the circuit, each word is converted from analog to digital form during the time that the analog multiplexer is dwelling on the desired input signal; the converted digital signal at the output of IC109 is then held and transferred to the associated data shift register at the next following word clock pulse, to be clocked through as digital data, delayed one word time interval with respect to the input analog signal.

Use of the positive-going narrow pulse of the word clock line from pin 3 of IC103A as a "parallel enter" signal transfers all 10 parallel digital output lines into the data shift register, IC113 and IC114. The shift register is made up of two 8-bit parallel in/serial output static shift registers, type CD4021B. Since only 10 bits of data are actually involved per word, the remaining 6 bits of IC113 have been grounded. Normally these would clock out as zeros, but the application of the "parallel enter" pulse at the end of each ten serial clock pulses simply re-enters the next following word to the shift register assembly. Data entered by the word clock pulse is then transferred out as a serial data stream by the bit clock signal, applied to pin 10 of each shift register. The Q8 output from pin 3 of IC113 is used as serial input to pin 11 of IC114, in order to add the desired two least significant bits to the serial transfer process during each word of the wave train. The output signal from Q8 then consists of 16 consecutive 10-bit digital words, clocked out most significant

bit first in each word, on pin 3. The first 15 words of this sequence consist of the 15 desired input signals, while the 16th word will be clocked out as a string of 10 successive zeros (by virtue of the fact the -5.1v reference to pin 5 of IC112 has insured saturation in the negative direction of the a-to-d converter) during the time interval desired for the synchronizing pulse. The digital wave train from pin 3 or IC114 is then taken as the serial data train to the sync/data switch.

3.4 Synchronization of the wave train is automatically accomplished by derivation of all desired timing signals from a common clock reference. The frame synchronization word is generated by IC105, another CD4021B (8-stage, parallel in/serial out static shift register). Parallel input lines are hardwired to +10v (logic 1) and ground (logic 0) so as to generate the desired synchronizing word of 110 111 000 0. As only an 8-bit shift register is used, advantage is taken of the fact that the parallel-entered sync word is clocked out, followed by a string of zeros, until a new sync word is reentered. The 8-bit content of the register is then clocked out, followed by 2 zeros, before the next following "parallel enter" pulse on pin 9 sets the sync word into the shift register once again. Serial data out is taken at bit clock frequency from pin 3 of IC114.

In order to improve noise immunity of the system, a scheme of inverting alternate minor frame synchronizing pulses has been employed within this unit. Timing for frame inversion is accomplished from the frame clock signal derived from IC104D. This signal, which is a square wave at minor frame frequency of 125 per second, is used to trigger IC107A, a CD4013P type D-toggle, to reverse the state at the Q_1 output, pin 1 of this toggle, with each successive minor frame. The Q_1 signal then consists of 16 words at "0" reference, followed by 16 words at logic "1" reference (+9.5v). The series of sync words from IC105 (the sync word generator) is applied to pin 1 of IC106, a quad 2-input exclusive OR gate, type CD4070B. A timing signal from the sync inversion gate, IC107A, is applied to the opposite input, pin 2. Since characteristics of IC106A are such that signal is passed through only when one input is at "0" and the other at logic "1", for the first 16 sync words, the output of pin 3 is identical to that provided from the sync word generator. The next following 16 are inverted in phase, providing the 1's complement synchronizing word. The input signal to sync data gate IC103D is then 16 consecutive normal sync words, followed by 16 consecutive inverted sync words.

3.5 The synchronizing signal is inserted in the proper position in the serial data train by gating through only one word of each group of 16. To accomplish this, the second section of IC107E is used as a "data switch" gate. This type D-toggle is driven by the frame anti-clock signal on pin 11 and is reset by the "word 1" address signal from main frame word counter, IC108B. The result is a positive-going square wave to pin 9 of dual input AND gate IC103D, only 1 word in duration, immediately following each transition from normal to inverted polarity for the sync word train. The output at pin 10 of IC103 then consists of a normal sync word, followed by 15 words of 0's; then an inverted sync word, followed by 15 more words of 0's.

The synchronizing signal is applied to pin 5 of "exclusive OR" gate IC106B. The data wave train derived from pin 3 of IC114 is applied to the opposite input on pin 6. Timing is such that, while pin 6 is held low for 10 consecutive 0's by the reference voltage in the analog multiplexed wave train, the desired polarity of synchronizing word is present on pin 5. Conversely, during the interval of time when digital data words are present on pin 6, there are 15 words of 0's on pin 5 of IC106. Because of the characteristics of the exclusive OR gate, the output wave train consists of mixed synchronizing and data words on pin 4, in NRZ-Level format.

The NRZ-Level wave train from pin 4 of IC106B is fed to pin 9 of IC106C and to pin 12 of IC106D. IC106D has its second input (on pin 13) grounded, resulting in a non-inverting buffer configuration and providing NRZ-Level PCM signals as the output from pin 11. This NRZ-Level monitor signal is taken through isolation resistor R118 to pin 7 of S0102 as a monitor signal.

In order to convert the NRZ-Level code to the desired Biphase Level format, the NRZ-Level train on pin 9 of IC106C is mixed with an inverted bit clock signal as input to pin 8, so as to insert a "0" following each "1" of the NRZ-Level train, and a "1" following each "0" of the NRZ-Level train, to provide the desired Biphase Level output code. The anti bit-clock signal is delayed by C102 to compensate for delays which occur within the sync data gate and shift register clocking portion of the circuit, so as to provide the desired time relationship in the biphase code converter.

The DC component of the output wave train is removed by C103, a blocking capacitor. A passive network consisting of R103, C104, and R102 is used to integrate the Biphase-Level code to act as a premodulation filter, reducing bandwidth requirements for radio transmission of the pulse modulated wave train.

A 10K ohm potentiometer, R102, is used for deviation control and permits adjustment of the desired biphasic level signal from 0 to ± 2 v maximum amplitude with respect to ground. Adjustment of this level provides an adjustment for deviation of the associated frequency modulated telemetry transmitter.

3.6 In order to permit operation from a single input power bus at a nominal voltage of +28v dc, PS101 (a dc-to-dc inverter) is used as a power supply. This unit (MIL Electronics Model PD815) operates on raw +29v input level to provide regulated output signals at ± 15 v with respect to common ground at 30 ma per side. The power supply incorporates a down-regulator such that operation of the system is essentially independent of input voltage for bus input levels about approximately +22v dc.

A secondary logic voltage is supplied as a nominal value of +10v with respect to ground, and a reference of -5.1v with respect to ground, are both provided by simple zener down-regulators. The +10v supply is obtained by dropping power through R112 to zener diode CR102. The value of R112 has been chosen to provide the desired bus current of approximately 15 ma and still retain approximately 3 ma of zener current. The storage capacitor C111, a 10 microfarad tantalytic capacitor, is provided in parallel with the zener to permit supply of the surge current demanded by the analog-to-digital converter during the period of each convert command signal.

The -15v supply is also reduced to a level of -5.1v by dropping resistor R113 and zener diode CR103. The -5.1v reference is used only as an input signal to word 16 of the main frame multiplexer and word 8 of the subcomm multiplexer, in order to insure that an analog signal which will saturate the analog-to-digital converter in the -5v direction is present at the time of desired synchronization.

All output voltage buses (+15, -15, +10, and -5.1v) are also brought through 10K isolation resistors to monitor pins on S0102, to permit external voltmeter checks of power supply operation.

The input bus voltage to the power supply is also offset by CR101, a nominal 23v positive zener, which effectively subtracts a fixed voltage from the input supply line. The difference between this zener reference and the supply line is then divided 2:1 by R111 and R110, filtered for hash and ripple,

and taken to pin 16 of S0101 as a conditioned battery monitor, for use within the telemetry subsystem as a monitor of battery condition. Parameters are so chosen as to permit monitor of the supply bus voltage power over a region of +23 to +33v dc input.

Note that monitors of all timing signals (bit clock, word clock, frame synchroniziation) and all voltage levels (+15, -15, +10, -5.1v), as well as an analog monitor of the multiplexed input to the analog-to-digital converter, are all brought to S0102 through 10K isolation resistors. In addition, the NRZ-Level coded signal from IC106D (pin 11) is brought to this same plug for convenience in observing system operation on a test oscilloscope.

3.7 As an alternate mode of operation, in the event it is desired to modulate a voltage-controlled oscillator rather than the raw telemetry transmitter, modulation can be provided through use of the NRZ-Level signal (instead of the Biphase-Level signal) as the primary output of the system. In order to change the modulation signal on pin 8 of S0102, it is only necessary to interchange the leads from pins 10 and 11 of chip IC104. Interchanging these two leads will provide the desired premodulation and deviation control on the NRZ-Level signal, while substituting the 10K isolation resistor as a monitor point on the Biphase-Level signal to pin 7 of S0102.

4.0 TEST AND SET UP OF ENCODER

In order to facilitate tests of each completed coder and to facilitate set up and evaluation of coder performance, an auxiliary coder test set (schematic diagram as shown in Figure 5) has been provided.

4.1 The test box is designed to provide the required operation and controls for the associated encoder from an external (variable) dc input source. It also brings out monitor points from the coder to permit voltmeter checks of the power supply output voltages, provides a measurement of coder input current, and generates a predetermined sequence of reference analog input signals for use as test signals while performing coder setup and evaluation tests. In addition, oscilloscope monitor points are provided for the Biphase-Level coded output signal, the NRZ-Level coded monitor signal, the analog multiplex monitor, and timing signals at bit, word, and frame rate. For initial set-up of the analog-to-digital converter "gain" and "zero" adjust controls, an auxiliary input jack is provided to transfer "word 1" to a precision external reference source. A toggle switch permits selection of the normal test voltage for "word 1", or use of the external calibration source.

In order to simplify operation of the test box, a PD815 dc-to-dc inverter is used to generate a set of semi-regulated input analog data signals for both main frame and subcommutator data word inputs. Normal $\pm 15\text{v}$ outputs from this power supply are down-regulated to reference levels of $\pm 6.8\text{v}$ with respect to ground, then adjusted to precision levels of $+5.00\text{v}$ and -5.00v by "reference adjust" potentiometers. The $\pm$ reference signals are also brought to a rotary selector switch, which permits use of an external voltmeter to monitor: the raw input supply voltage, all power supply voltages from the coder, the two reference voltages from the test set, and the coder "Battery Monitor" voltage.

Two captive cables, approximately 2 feet in length, are prewired to the test box to mate with S0101 (data input) and S0102 (power and monitor) plugs of the coder under test. (Ref: Figure 1, showing unit connected.)

When used in the internal test mode, the sequence of analog signals which should appear on the coder "analog multiplex monitor" will be as follows, for words 1 through 15:

Word 1	-5v	Word 6	-0.5v	Word 11	+4v
Word 2	-4v	Word 7	+0.5v	Word 12	0v
Word 3	-3v	Word 8	+1v	Word 13	+5v
Word 4	-2v	Word 9	+2v	Word 14	Battery Monitor
Word 5	-1v	Word 10	+3v	Word 15	Subcomm (Housekeeping)

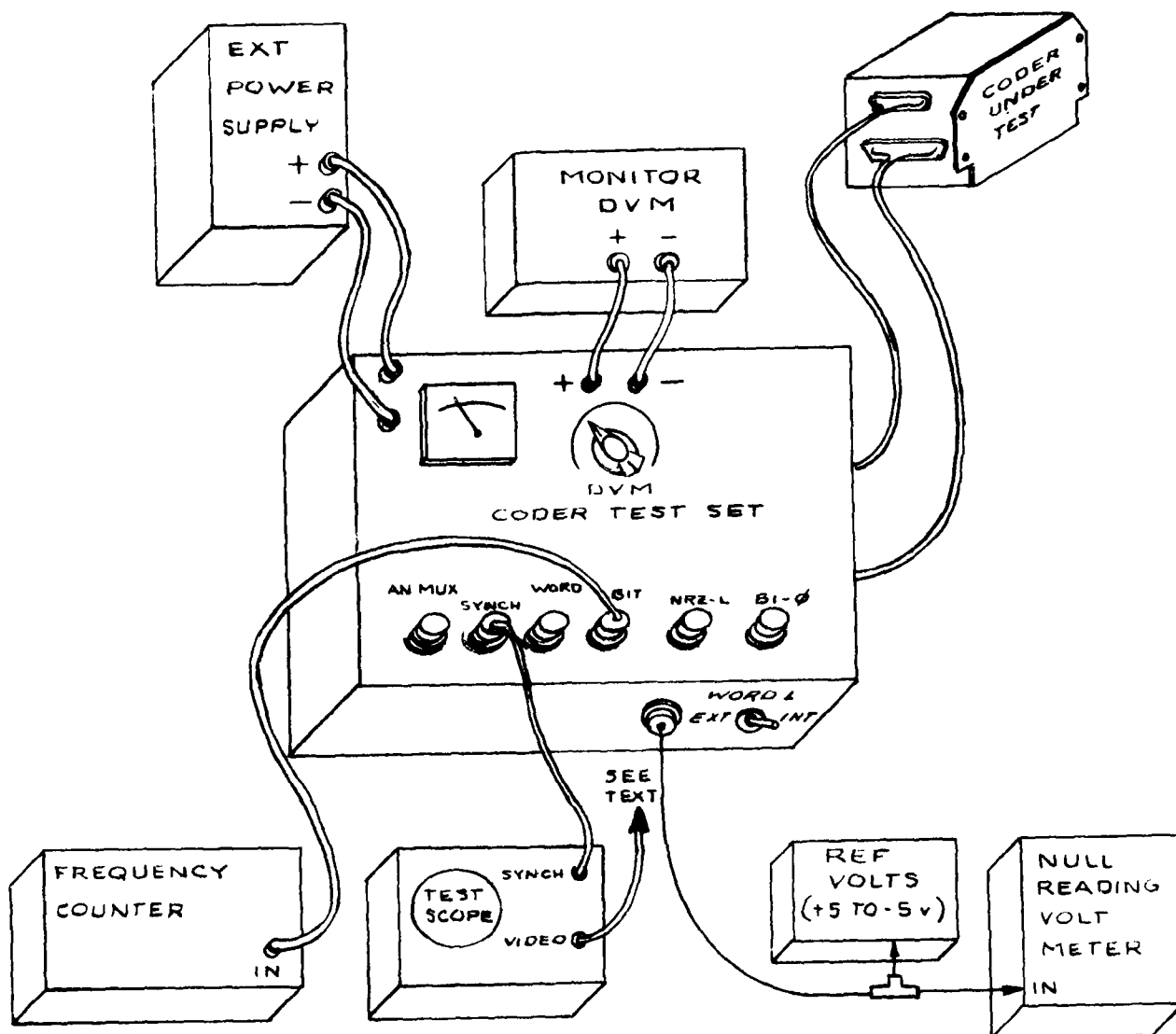


Figure 6. Coder Test Set up

The housekeeping subcommutator is wired so as to present the battery monitor signal on subcommutated input number 1, followed by a sequence of +5, +4, +3, +2, and +1, and +.5v signals. This test harness is so wired to insert the subcommutated wave train as the input to word 15. Word 12 serves as a reference signal, at signal ground potential.

4.2 The test set up required for initial evaluation of coder performance is as shown in Figure 6. Equipment required (in addition to the special coder test set) is as follows:

- a. Nominal +28v dc power supply, adjustable over region of 22 to 34 volts in level, with output current capability of at least 150 ma.
- b. External voltmeter monitor (preferably a digital voltmeter) with capability of zero to +35v dc measurement range.
- c. External low noise reference source of precision voltage, with noise level of no more than 2 mv, and adjustable dc reference values from -5 to +5v dc.
- d. Precision null-reading voltmeter, preferably with resolution of the order of 100 microvolts dc minimum.
- e. Test oscilloscope, sweep speeds of 1 microsec/div to 10 millisec/div.
- f. Counter, 100 Hz to 500 KHz range.

4.3 For initial set up of each individual coder prior to formal test evaluation, the following procedure should be followed: (Set up should be made with the nominal external power supply input voltage of 28 volts, at normal room temperature of approximately 25°C.)

4.3.1 With the system turned on but coder current "off", set the voltmeter selector to the "+ and - Ref" positions. With the adjustments provided on the coder test set, adjust for voltages of +5.00 and -5.00 volts respectively.

4.3.2 Turn the "coder current" switch to the "on" position and record both the input voltage (as displayed on the digital voltmeter) and the current to the coder on the test data sheet (Figure 7).

4.3.3 Record the bit frequency from the counter.

4.3.4 With the scope synchronized as shown (vertical input as shown in detail A,) observe the "analog multiplex monitor" waveform and verify that it is in accord with that shown on test sheet 1. Vary input voltage and note that word 14 varies in accord with changes.

4.3.5 Verify proper synchronization pattern by the following procedure:

- (a) With video input to the scope on test point C; set sweep for two word length (1 millisec).

TEST DATA SHEET-OSU C40BE02 (10 Bit Coder) S/N _____

Initial Set-up:

Temperature = _____ °C

Input Volts = _____ v Coder Current = _____ ma

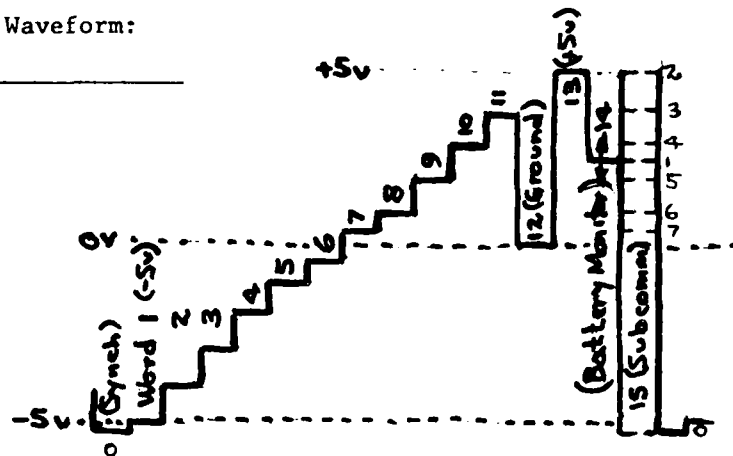
Bit Frequency = _____ bits/sec

Test Set Voltages:

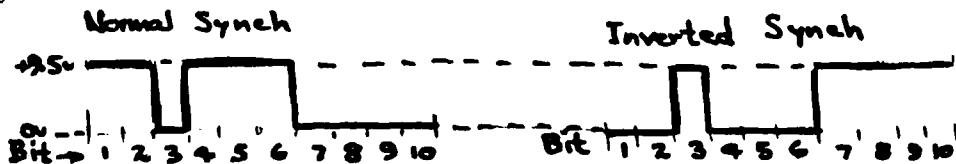
+15v = _____ v
 +10v = _____ v
 -5.1v = _____ v
 -15v = _____ v
 +5v Ref = _____ v
 -5v Ref = _____ v

Analog Mux Waveform:

Checked _____



Synch Word Check:



Scope Synch (-) _____ Checked

Scope Synch (+) _____ Checked

Bi-Phase Conversion _____ checked

Deviation Control Set (+2v) _____ v set

Battery Monitor Calibration:

In =	24v	25v	26v	27v	28v	29v
Mon =	_____	_____	_____	_____	_____	_____
In =	30v	31v	32v	33v	34v	
Mon =	_____	_____	_____	_____	_____	

Date _____

By _____

Figure 7. Coder Test Data, Sheet 1

(b) Move scope to point E and verify the synchronizing pattern in NRZ-Level waveform is in accord with that shown, with the scope set to trigger from negative synchronization.

(c) Readjust sync to positive synchronization and note that the alternate sync inversion is occurring, as shown by the inverted waveform on Figure 7. Waveforms will be seen on the left side of the screen, in the grouping corresponding to the first word displayed.

4.3.6 With the scope in the same configuration (two words sweep length and synchronization from frame sync), observe the appearance of the word in the right-hand side of the scope screen, corresponding to the second word displayed. (This will be word 1 in the data assignment.) Flip the "word 1 signal" switch to the "external" position and, with 0v from the reference supply, adjust the "0" control on top of the decoder to give a pattern flickering between a logic 1 followed by nine 0's, and a logic 0 followed by nine 1's (This effectively sets the "0" point at the half-bit decision point for the coder being used, and establishes the reference for data input voltages in the following checks.)

4.3.7 Readjust the reference voltage source to +5v and adjust coder "gain" control for a sequence of all 10 bits at the logic 1 level. (Caution should be exercised in this setting not to turn the control too far, as the coder will saturate at 10 consecutive 1's.) Adjustment should be made to where the least significant bit has just gone to a solid "one" indication, with no flicker in the 0 level.

4.3.8 Move the scope to point F and verify that proper biphas level code conversion has occurred, as indicated by a succession of alternating half bit width "ones" and "zeros" for the second word position. Adjust the "deviation" control to provide a 4v peak-to-peak biphas level wavetrain on the modulation output (F of Figure 6).

4.3.9 Calibrate the "Battery Monitor" circuit by the following procedure:

(a) Switch the "external VM" monitor to the "Battery Monitor" position. Note the "Battery Monitor" voltage for +28v dc "In".

(b) Either by switching the external VM back and forth between "In" and "Battery Monitor", or by use of a separate digital meter on the "In" test point, measure the "Battery Monitor" volts as a function of the "Input" voltage for a range of +24 to +34 volts. Record the data on the test sheet in the space provided.

TEST DATA SHEET-OSU C40BE02 (10-Bit Coder) S/N _____

Coder Conversion Tests:

Temperature = _____ °C

Bit Frequency (Bits/sec) _____

Coder Current (ma) _____

Ext DVM Power Supply Tests:

Input Volts:

	(28v)	(24v)	(32v)
+15v P.S. (volts)	_____	_____	_____
+10v P.S. (")	_____	_____	_____
-5.1v P.S. (")	_____	_____	_____
-15v P.S. (")	_____	_____	_____
+5v Ref (")	_____	_____	_____
-5v Ref (")	_____	_____	_____

Digital Conversion Tests:

Input Condition =	+28v	+24v	+32v
Digital Test Word	Null Voltmeter	Input for	Test Pattern
111 111 101 1 (+4.9609v) $\Delta V =$	_____	_____	_____
110 000 010 0 (+2.5440v) $\Delta V =$	_____	_____	_____
100 000 001 0 (+0.0204v) $\Delta V =$	_____	_____	_____
001 111 101 1 (-2.5440v) $\Delta V =$	_____	_____	_____
000 000 010 0 (-4.9609v) $\Delta V =$	_____	_____	_____
Max Bit Error (+) =	_____	bits (@ 9.77mv/bit)	
Max Bit Error (-) =	_____	" (" / ")	

Worst Case Conditions: _____

Notes: _____

Tested by: _____

Date: _____

Figure 8. Coder Test Data, Sheet 2

4.4 Testing under variable conditions may now be done. For this purpose the test data sheet shown in Figure 8 should be employed, and data recorded as requested. Initial setting should be made at +28v applied voltage and 25°C (room temperature) conditions.

4.4.1 Record the bit frequency as shown on the counter, coder current, and all operating voltages (by dialing the external digital voltmeter through the entire sequence of switch positions available on the coder test set).

4.4.2 With the scope adjusted as described in paragraph 4.3.5, move the scope input to point D of Figure 6 and adjust the sweep control for 2 bits per horizontal division on scope. (This should establish "word 2" position as extending from the center line on the scope reticle to the right-hand edge, for one word of 10-bit length.) Move scope vertical input back to E of Figure 6.

4.4.3 Still operating in the word 1 "External Signal" mode, adjust the reference voltage to give each of the 5 selected test patterns of Figure 8 on the test digital waveform. Record the null voltmeter reading shown for each of the 5 conditions, when the pattern desired is established on the NRZ-L waveform on the scope. These dc voltages should be compared with the theoretical voltage (shown in parenthesis under each bit pattern) and the difference between the actual voltage and the theoretical voltage recorded in the proper spot on the test sheet.

4.5 In order to verify acceptability of operation under varying input voltage conditions, repeat the entire procedure outlined under 4.4 for input voltages of +24v and +32v supply voltage. (The test sheet will provide a place to record this information as well.)

4.6 In order to verify acceptability under extremes of temperature conditions, the system should be reset to 28v, placed in the temperature chamber, and allowed to stabilize for at least 30 minutes at a temperature of -20°C. Data should be recorded again on the test sheet for this new temperature, by following the procedures outlined in 4.4 and 4.5. This should verify proper operation at -20°C for minimum and maximum supply voltages.

4.7 Change temperature of the test chamber to +65°C and allow unit to soak for 30 minutes at this temperature, then record all parameters (as outlined in 4.4 and 4.5) for the same 3 input voltages. This should verify operation at +65°C for minimum and maximum supply voltages.

4.8 In the event that an appropriate PCM decoder is available for performing the above checks, it may prove more convenient to feed the serial data

wave train into a PCM decoder (from scope monitor point F of Figure 6) and use the decoder digital light display to verify digital coding, in preference to reading the raw NRZ-L wave forms from the face of the scope. It is possible to accommodate the alternate sync inversion on a PCM decoder not equipped for the "alternate sync" mode of operation by programming decoder to accept 2 full frames of data as the indicated format. To do this, the PCM decoder should be set for the biphas-level mode of operation, with the bit rate at 20 Kbits. Formatting should be for a frame of 32 words of 10-bit length; the synchronization pattern should be set as 110 111 000 0. (Note that this is the normal Barker code without inversion.)

4.8.1 The inverted sync code can then be checked, as it will appear in the data stream as word 16, inverted to show the pattern of 001 000 111 1, for the test of 4.3.5.

4.8.2 Verification of proper bit patterns and null meter voltage readings for word 1 (as described in 4.3.6) may be done by dialing in word 1 and observing each of the five selected bit patterns from the digital display of the PCM coder.

4.8.3 In the normal coder test set mode, word 15 will contain subcommutated information. Proper operation may also be checked by programming the decoder for an 8 minor frame subcomm within the main frame, in word 15 position. The subcomm synchronization word should be selected as 000 000 000 0. Subcommutated voltages will present the battery monitor signal as subcomm word number 1, followed by a sequence of approximately +5, +4, +3, +2, +1 and +0.5 volt signals for words 2 through 7.

4.8.4 The test set also supplies a predetermined sequence of voltages for all minor frame words, 1 thru 14. (The sequence of analog voltages supplied was listed in 4.1 of this section.)

4.8.5 The battery monitor circuit can be calibrated by reading the digital word displayed in the word 14 position while varying the input supply voltage. Record the word 14 digital value as a function of the input supply voltage (as shown on the external digital voltmeter monitor) while the external supply voltage is varied over limits of 24 to 34 volts dc.

5.0 ASSOCIATED DRAWINGS

The following OSU drawings describe the 10-bit resolution sphere PCM coder and associated test set. Where drawings have been reproduced as a portion of this manual, the figure number used herein is listed.

Coder Drawings			
Drawing Number	Title	Figure	Page
B40BE01	Block Diagram	2	10
C40BE02	Logic Diagram (Schematic)	3	14
B40BE03	Envelope Drawing (Mounting)		
B40BE04	Mechanical Assembly Drawing		
B40BE05-2	End Plates (Connector Mount)		
A40BE06	Base Plate		
B40BE07-2	Side Plates		
B40BE08	Back Plate		
A40BE09	Top Plate		
D40BE10	Detail, Board A (Logic & ADC)		
D40BE11	Detail, Board B (Power Supply & Multiplexer)		
B40BE12	Waveforms	4	16
Test Set Drawings			
C40BC01	Schematic & Board Detail	5	26
C40BC02	Assembly		
C40BC03	Chassis Detail		

6.0 COMPOSITE PARTS LIST, 10-BIT CODER AND TEST SET

A complete parts list of all electrical components used in both the C40BE02 model of the 10-bit sphere encoder and the associated model C40BC01 test set follows. Parts have been listed in alphanumeric order, following the reference code designations used as identifiers on the schematic diagram for each unit.

The lists include the manufacturer and the manufacturer's part number, as well as a description of each part and the usage within the circuit.

10-BIT CODER PARTS LIST (C40BE02 CIRCUIT)

Reference Code	Part	Description	Use	Manufacturer
C101	CW15C103K	0.01uFd 50v Monolythic Capacitor	Decoupling	Centralab
C102	CW15C472K	0.0047uFd 50v "	Delay Compensation	"
C103	CY20C104M	0.1uFd 50v "	Signal Coupling	"
C104	MTPI06M035P1A	10uFd 35v Tantalytic	Filtering, +10v Bus	Mallory
C105	CY30C105M	1.0uFd 50v Monolythic	Decoupling, Battery Monitor	Centralab
C106	CK06BX105K	1.0uFd 50v "	Filtering, +28v In	Mallory
C107	Same as C106	"	" , +15v Out	"
C108	Same as C106	"	" , -15v Out	"
C109	CW15C102K	0.001uFd 50v Monolythic	Signal Shaping	Centralab
C110	Same as C102	"	Signal Coupling	"
C111	Same as C104	"	Filtering, +10v Out	Mallory
CR101	1N723A	23v Zener Diode	Battery Monitor Offset	Texas Instru.
CR102	1N758A	10v " "	+10v Regulator	Int'l Rectifier
CR103	1N751A	5.1v " "	-5.1v "	" "
CR104	1N483	100 ma 70 PIV Diode	Steering Diode, +15v	Texas Instru.
IC101	HS-400(320 KHz)	CMOS Crystal Oscillator	Clock Base	Northern Eng'g Labs
IC102	CD4520B	CMOS Dual Binary Counter	Bit Clock Divider	RCA
IC103	CD4081B	CMOS Quad 2-In And Gate	Logic Gating	RCA
IC104	HD74C901N	CMOS Hex Inverter	Signal Inversion	Harris Semicond.
IC105	CD4021B	CMOS 8-bit PISO Shift Register	Synch Generator	RCA
IC106	CD4070B	CMOS Quad 2-In Exclusive Or Gate	Logic Gate & Switch	RCA
IC107	CD4013B	CMOS Dual "D" Flip Flop	Gate Generator	RCA
IC108	CD4520B	Same as IC102	Word & Frame Counter	RCA
IC109	HC12-BGC	CMOS 12-Bit A/D Converter	An to Dig Conversion	RCA
IC110	HI-1818A	8-Chan Analog Multiplex Switch	Subcomm Multiplexer	Datel
IC111	HI-1818A	Same as IC110	Data Multiplexer	Harris Semicond.
IC112	HI-1818A	Same as IC110	" "	" "
IC113	CD4021B	Same as IC105	Data Shift Register	RCA
IC114	CD4021B	Same as IC105	" "	RCA
IC115	MC1741SCP	Fast Operational Amplifier	Voltage Follower	Motorola
IC116	LDP16-01-103G	8-Section 10K + 2% 1/8 watt Resistor	Monitor Isolation	Dale
(RA-RH)				
PS101	PD-815	DC/DC Inverter (28v to +15v 300MA)	Power Supply	MIL Electronics
R101	RC-07	10K + 5% 1/4 watt Resistor	Monitor Isolation	Ohmite
R102	3262H-W1-103	10K Variable Resistor	Deviation Adjust	Bourns
R103	RC-07	Same as R101	Shaping Network	Ohmite

10-BIT CODER PARTS LIST (C40BE02 CIRCUIT) (CONT'D)

Reference Code	Part	Description	Use	Manufacturer
R104	3262H-W1-103	Same as R102	Converter Gain Adjust	Bourns
R105	RC-07	Selected (Nom 1M ohm $\pm$ 5% $\frac{1}{4}$ watt) Resistor	Converter Gain Set	Ohmite
R106	3262H-W1-103	Same as R102	Converter Zero Adjust	Bourns
R107	RC-07	470K $\pm$ 5% $\frac{1}{4}$ watt Resistor	Multiplexer Output Return	Ohmite
R108	RC-07	Same as R101	Monitor Isolation	Ohmite
R109	Deleted - Not used in this system			
R110	RC-07	3.3K $\pm$ 5% $\frac{1}{4}$ watt Resistor	Battery Monitor Divider	Ohmite
R111	RC-07	Same as R110	" "	Ohmite
R112	RC-07	270 ohm $\pm$ 5% $\frac{1}{4}$ watt Resistor	+10v P.S. Dropping	Ohmite
R113	RC-07	1K ohm $\pm$ 5% $\frac{1}{4}$ watt Resistor	-5.1v " "	Ohmite
S0101	DB-25P	25-Pin Male Connector, Chassis Mount	Signal Input	Cannon
S0102	DA-15P	15-Pin Male Connector, Chassis Mount	Power & Monitor	Cannon
No Number	508AG10F	8-Pin Dip Socket, Wire-wrap	Chip Socket	Augat
"	514AG10F	14-Pin Dip Socket, Wire-wrap	Chip Socket	Augat
"	516AG10F	16-Pin Dip Socket, Wire-wrap	Chip Socket	Augat
"	102-16-AA-B	16-Pin Dip Socket, Wire-wrap	Chip Socket	Garry

*Cut two lengthwise, use in line for IC109;
other three used for IC105-113-114, end-to-end.

CODER TEST SET PARTS LIST (C40BC01 CIRCUIT)

Reference Code	Part	Description	Use	Manufacturer
CI01	162D335X9010	3.3ufd 10v Tantalytic Capacitors	+5v Ref. Filter	Sprague
CI02	162D335X9010	Same as CI01	-5v Ref. Filter	Sprague
CR101	1N754A	6.8v Zener Diode	+5v Ref. Power Supply	Motorola
CR102	1N754A	Same as CR101	-5v Ref. Power Supply	Motorola
JS101	DF30R	5-way Binding Post, Red	+28v Input	Superior
JS102	DF30B	" " " " , Black	Power Ground	Superior
JS103	UG-625/U	BNC Jack, Chassis Mount	Word 1 Input	Amphenol
JS104	UG-625/U	Same as JS103	BiPhase Level Out	"
JS105	UG-625/U	" " "	NRZ-L Monitor	"
JS106	UG-625/U	" " "	An Mux Monitor	"
JS107	UG-625/U	" " "	Bit Clock Monitor	"
JS108	UG-625/U	" " "	Word Clock Monitor	"
JS109	UG-625/U	" " "	Frame Synch Monitor	"
MI01	MS-1T	100 MA DC Meter	Coder Current Monitor	Honeywell
PL101	DB-25S	25-Pin Female Connector (Cable)	Signal Input	Cannon
PL102	DA-15S	15-Pin Female Connector (Cable)	Power & Monitor Input	Cannon
PS101	PD-815	DC/DC Inverter, +28v to +15v 30 MA	Power Supply	MIL Electronics
R101	RC-20	2.2K + 5% 1/2 watt Resistor	+Ref. P.S. Dropping	Ohmite
R102	RC-07	560 ohm + 5% 1/4 watt Resistor	+Ref. P.S. Decoupling	Ohmite
R103	RC-20	Same as R101	-Ref. P.S. Dropping	Ohmite
R104	RC-07	Same as R102	-Ref. P.S. Decoupling	Ohmite
R105	RA20NA5D501A	500 ohm 1/2 watt Variable Resistor	+Ref. P.S. Adjust	Centralab
R106	RA20NA5D501A	Same as R105	-Ref. P.S. Adjust	Centralab
R107	RC-07	470 ohm + 5% 1/4 watt Resistor	Signal Voltage Divider	Ohmite
R108	RC-07	Same as R107	"	"
R109	RC-07	Same as R107	"	"
R110	RC-07	Same as R107	"	"
R111	RC-07	220 ohm + 5% 1/4 watt Resistor	"	"
R112	RC-07	240 ohm + 5% 1/4 watt Resistor	"	"
R113	RC-07	Same as R107	"	"
R114	RC-07	Same as R107	"	"
R115	RC-07	Same as R107	"	"
R116	RC-07	Same as R107	"	"
R117	RC-07	Same as R111	"	"
R118	RC-07	Same as R112	"	"

CODER TEST SET PARTS LIST (C40BC01 CIRCUIT) (CONT'D)

Reference Code	Part	Description	Use	Manufacturer
S101	MTB-106D	SPDT Toggle Switch	Coder On	Alco
S102	PA-2001	1 pole 9-position Rotary Switch	Ext. VM Select	Centralab
S103	MTB-106D	Same as S101	Work 1 Select	Alco
TP101	256 (White)	Banana Jack Test Point	Ext - VTVM Monitor	H. H. Smith
TP102	256 (Black)	Same as TP101	Ext - VTVM Monitor	H. H. Smith
TP103	256 (Red)	Same as TP101	Input Monitor	H. H. Smith
TP104	256 (Orange)	Same as TP101	+15v Monitor	H. H. Smith
TP105	256 (Yellow)	Same as TP101	+10v Monitor	H. H. Smith
TP106	256 (Gray)	Same as TP101	-5.1v Monitor	H. H. Smith
TP107	256 (Blue)	Same as TP101	-15v Monitor	H. H. Smith
TP108	256 (Tan)	Same as TP101	Monitor Common	H. H. Smith
TP109	256 (Brown)	Same as TP101	-5v Ref. Monitor	H. H. Smith
TP110	256 (Green)	Same as TP101	+5v Ref. Monitor	H. H. Smith
No Number	AC-402	5"x7"x2" Aluminum Chassis	Test Box	Bud

7.0 EVALUATION OF PROTOTYPE SYSTEM

Following completion of the prototype model of the C40BE02 PCM encoder and the associated C40BC01 test set, the system was adjusted and tested in accord with the procedure described in Section 4.0 of this report.

Initial adjustment was made by the procedure described in paragraph 4.3 and results are shown on the following Test Data Sheet 1.

The initial set-up data was followed by testing under conditions of varying input supply voltage, following the procedure described in paragraphs 4.4 and 4.5. Test results under ambient temperature conditions are as presented on the attached Test Data Sheet 2.

Final testing of the unit was for operation under temperature extremes of -20°C and $+65^{\circ}\text{C}$, for the entire range of input supply voltage anticipated. The procedures described in paragraphs 4.6 and 4.7 were followed for these tests, and test data is as recorded on the final completed copies of Test Data Sheet No. 2 at the end of this report.

The results of the tests indicate that the prototype version of this equipment satisfied the design objectives, and the prototype will be delivered to AFGL for qualification testing prior to use in scheduled experiments. Two production versions of the same component are presently under construction for later use in the ongoing measurement program.

TEST DATA SHEET-OSU C40BE02 (10 Bit Coder) S/N PROTO

Initial Set-up:

Temperature = 25 °C

Input Volts = 28.0 v Coder Current = 63 ma

Bit Frequency = 20,000 bits/sec

Test Set Voltages:

+15v = +14.50 v

+10v = +10.12 v

-5.1v = -5.08 v

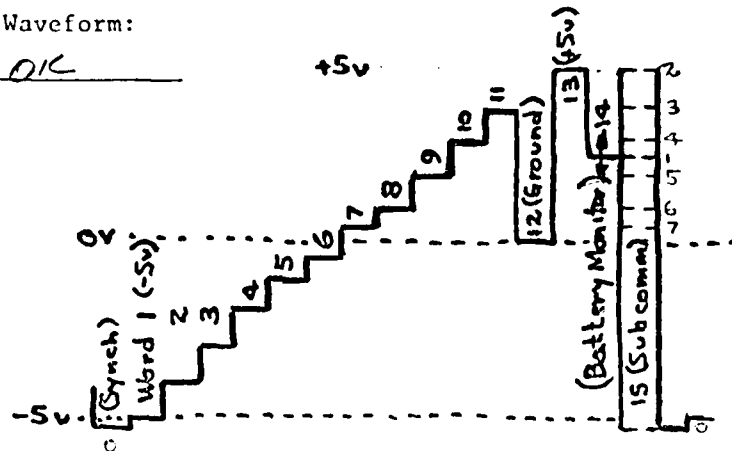
-15v = -15.16 v

+5v Ref = +5.00 v

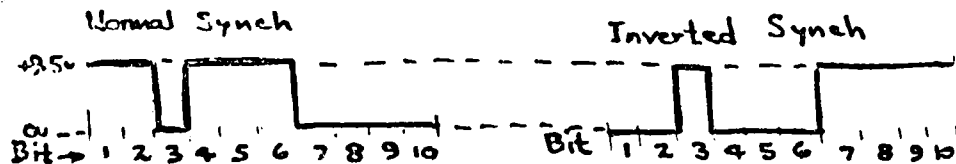
-5v Ref = -5.00 v

Analog Mux Waveform:

Checked OK



Synch Word Check:



Scope Synch (-) OK Checked

Scope Synch (+) OK Checked

Bi-Phase Conversion OK checked

Deviation Control Set (+2v) ±2 v set

Battery Monitor Calibration:

In =	24v	25v	26v	27v	28v	29v
Mon =	<u>0.00v</u>	<u>.123v</u>	<u>.603v</u>	<u>1.071v</u>	<u>1.57v</u>	<u>2.07v</u>
In =	30v	31v	32v	33v	34v	
Mon =	<u>2.55v</u>	<u>3.03v</u>	<u>3.51v</u>	<u>4.00v</u>	<u>4.49v</u>	

Date 2/28/80
By LS

TEST DATA SHEET-OSU C40BE02 (10-Bit Coder) S/N PR070

Coder Conversion Tests:

Temperature = 25 °C

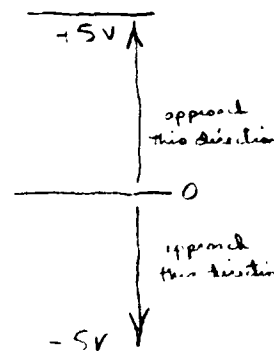
Bit Frequency (Bits/sec) 20000 20000 20000
 Coder Current (ma) 63ma 64ma 64ma

Ext DVM Power Supply Tests:

Input Volts:	<u>+28.0v</u> (28v)	<u>+24.0v</u> (24v)	<u>+32.0v</u> (32v)
+15v P.S. (volts)	<u>+14.50v</u>	<u>+14.49v</u>	<u>+14.49v</u>
+10v P.S. (")	<u>+10.12v</u>	<u>+10.12v</u>	<u>+10.12v</u>
-5.1v P.S. (")	<u>-5.08v</u>	<u>-5.08v</u>	<u>-5.08v</u>
-15v P.S. (")	<u>-15.15v</u>	<u>-15.16v</u>	<u>-15.16v</u>
+5v Ref (")	<u>+5.00v</u>	<u>+5.00v</u>	<u>+5.00v</u>
-5v Ref (")	<u>-5.00v</u>	<u>-5.00v</u>	<u>-5.00v</u>

Digital Conversion Tests: +5v and 0v pot set. (-1.9945v to get all 0's out)
 Input Condition = +28v +24v +5.0000v to get all 1's on +32v

Digital Test Word	Null Voltmeter	Input for	Test Pattern
111 111 101 1 (+4.9609v)	<u>4.9581v</u> $\Delta V = -0.0028v$	<u>4.9581v</u> -0.0027	<u>4.9581v</u> $-0.0027v$
110 000 010 0 (+2.5440v)	<u>2.5442v</u> $\Delta V = -0.0022v$	<u>2.5442v</u> -0.0022	<u>2.5442v</u> $-0.0022v$
100 000 001 0 (+0.0204v)	<u>0.0218v</u> $\Delta V = -0.0014v$	<u>0.0216v</u> -0.0014	<u>0.0217v</u> $-0.0014v$
001 111 101 1 (-2.5440v)	<u>-2.5425v</u> $\Delta V = +0.0015v$	<u>-2.5425v</u> $+0.0015$	<u>-2.5425v</u> $+0.0015v$
000 000 010 0 (-4.9609v)	<u>-4.9636v</u> $\Delta V = -0.0027v$	<u>-4.9636v</u> -0.0027	<u>-4.9630v</u> $-0.0027v$
Max Bit Error (+)	= +0.004 bits (@ 9.77mv/bit)		
Max Bit Error (-)	= -0.004 " (" / ")		

Worst Case Conditions: NoneSPECIAL TEST: None

Notes: _____

Tested by: LSDate: 2/28/80

TEST DATA SHEET-OSU C40BE02 (10 Bit Coder) S/N PROTO

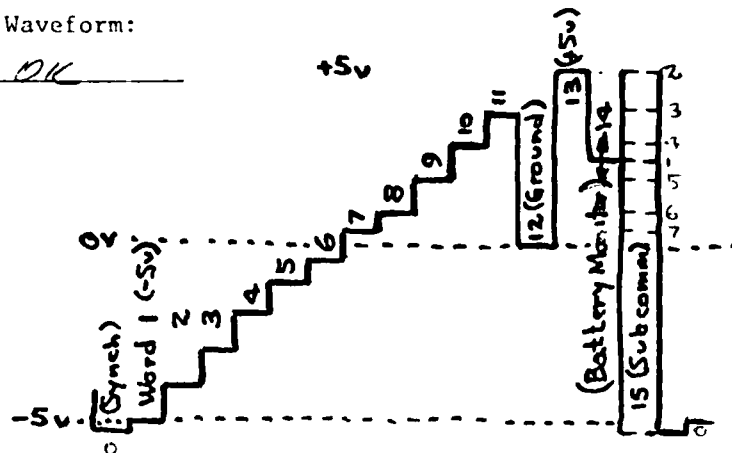
Initial Set-up: Temperature = -20 °C
 Input Volts = 28.0 v Coder Current = 62.0 ma
 Bit Frequency = 20,000 bits/sec

Test Set Voltages:

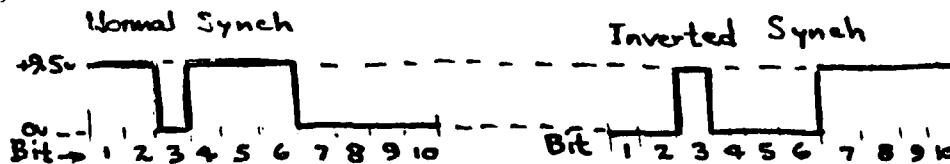
+15v = +14.28 v
 +10v = +9.78 v
 -5.1v = -5.11 v
 -15v = -15.05 v
 +5v Ref = +5.00 v
 -5v Ref = -5.00 v

Analog Mux Waveform:

Checked OK



Synch Word Check:



Scope Synch (-) OK Checked Scope Synch (+) OK Checked

Bi-Phase Conversion OK checked

Deviation Control Set (+2v) ±2.0 v set OK

Battery Monitor Calibration:

In =	24v	25v	26v	27v	28v	29v
Mon =	<u>.103v</u>	<u>.630v</u>	<u>1.108v</u>	<u>1.62v</u>	<u>2.10v</u>	<u>2.60v</u>
In =	30v	31v	32v	33v	34v	
Mon =	<u>3.11v</u>	<u>3.57v</u>	<u>4.06v</u>	<u>4.54v</u>	<u>5.02v</u>	

Date 2/27/80
 By S

Temperature = -20°C

Ext DVM Power Supply Tests:

Digital Conversion Tests:

at 31000
on 10/28/80

Worst Case Conditions: - 2.50 gms. @ 1000 rpm

SUPPLY VOLTA 25

Notes: A/D 5/10/1992 ADD 4/15 12 NAME

SUMMER ADMS + 1/2 RIT

LOW TEMPERATURE CORROSION

Tested by: 5

Date: 2/29/80

TEST DATA SHEET-OSU C40BE02 (10 Bit Coder) S/N PROTO

Initial Set-up:

Temperature = +65 °C

Input Volts = 28.0 v Coder Current = 63.0 ma

Bit Frequency = 20,000 bits/sec

Test Set Voltages:

+15v = +14.55 v

+10v = +10.23 v

-5.1v = -5.07 v

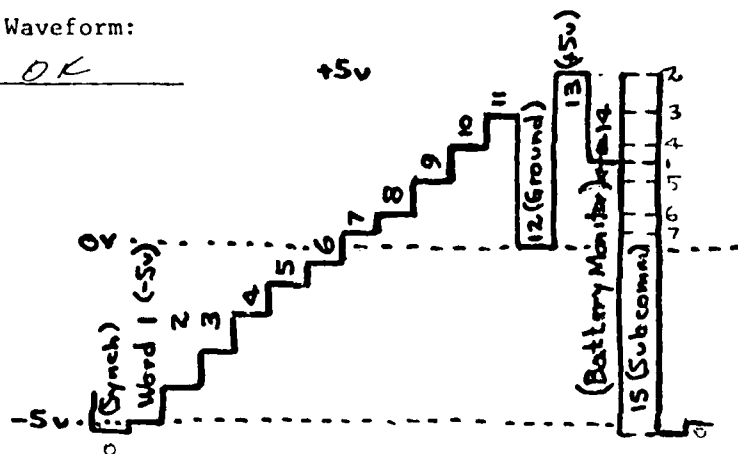
-15v = -15.18 v

+5v Ref = 5.00 v

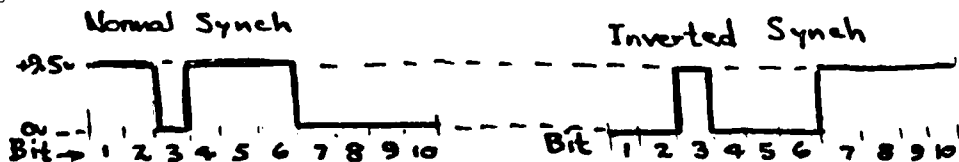
-5v Ref = -5.00 v

Analog Mux Waveform:

Checked OK



Synch Word Check:



Scope Synch (-) OK Checked

Scope Synch (+) OK Checked

Bi-Phase Conversion OK checked

Deviation Control Set (+2v) ±2 v set (Bi-φ L code out - OPEN output.)

Battery Monitor Calibration:

In =	24v	25v	26v	27v	28v	29v
Mon =	.000v	.000v	.443v	.908v	1.403v	1.90 v
In =	30v	31v	32v	33v	34v	
Mon =	2.36v	2.85v	3.33v	3.83v	4.31v	

Date 2/29/80
By S

TEST DATA SHEET-OSU C40BE02 (10-Bit Coder) S/N PR000

Coder Conversion Tests:

Temperature = 65 °C

Bit Frequency (Bits/sec)	<u>20000</u>	<u>20000</u>	<u>20000</u>
Coder Current (ma)	<u>64ma</u>	<u>65ma</u>	<u>64.5ma</u>

Ext DVM Power Supply Tests:

Input Volts:	<u>28.0v</u>	<u>24.0v</u>	<u>32.0v</u>
	(28v)	(24v)	(32v)
+15v P.S. (volts)	<u>+14.55v</u>	<u>+14.55v</u>	<u>+14.56v</u>
+10v P.S. (")	<u>+10.23v</u>	<u>+10.23v</u>	<u>+10.23v</u>
-5.1v P.S. (")	<u>-5.07v</u>	<u>-5.07v</u>	<u>-5.07v</u>
-15v P.S. (")	<u>-15.18v</u>	<u>-15.19v</u>	<u>-15.20v</u>
+5v Ref (")	<u>+5.00v</u>	<u>+5.00v</u>	<u>+5.00v</u>
-5v Ref (")	<u>-5.00v</u>	<u>-5.00v</u>	<u>-5.00v</u>

Digital Conversion Tests:

Input Condition =	+28v	+24v	+32v
Digital Test Word	Null Voltmeter	Input for	Test Pattern
111 111 101 1	<u>4.9587v</u>	<u>4.9587v</u>	<u>4.9587v</u>
(+4.9609v) $\Delta V =$	<u>-.0022</u>	<u>-.0022</u>	<u>-.0022</u>
110 000 010 0	<u>2.5438v</u>	<u>2.5438v</u>	<u>2.5438v</u>
(+2.5440v) $\Delta V =$	<u>-.0002</u>	<u>-.0002</u>	<u>-.0002</u>
100 000 001 0	<u>.01995v</u>	<u>.01995v</u>	<u>.01995v</u>
(+0.0204v) $\Delta V =$	<u>-.0004</u>	<u>-.0004</u>	<u>-.0004</u>
001 111 101 1	<u>2.5446v</u>	<u>2.5446v</u>	<u>2.5446v</u>
(-2.5440v) $\Delta V =$	<u>+.0006</u>	<u>+.0006</u>	<u>+.0006</u>
000 000 010 0	<u>4.9595v</u>	<u>4.9596v</u>	<u>4.9594</u>
(-4.9609v) $\Delta V =$	<u>+.0004</u>	<u>+.0003</u>	<u>+.0005</u>
Max Bit Error (+) =	<u>+0.2</u>	bits (@ 9.77mv/bit)	
Max Bit Error (-) =	<u>-0.5</u>	" (" / ")	

Worst Case Conditions: NEAR REFERENCE

Notes: BALANCE SCITING APPEARS TO
SHIFT SLIGHTLY AT HIGH TEMPERATURE
CONDITION

Tested by: 5Date: 2/29/80

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