RADC-TR-80-354
Final Technical Report
November 1980

DESIGN CONSIDERATIONS FOR PHASED ARRAY MODULES

University College London

John R. Forrest
J. Austin
A. A. de Salles
J. G. Schoenenberger

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-80-354 has been reviewed and is approved for publication

APPROVED: Sheldon B. Herskovitz

SHELDON B. HERSKOVITZ
Project Engineer

APPROVED: Allan C. Schell

ALLAN C. SCHELL
Chief, Electromagnetic Sciences Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (EECT) Hanscom AFB MA 01731. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

19 REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: RADC-TR-80-354	2. GOVT ACCESSION NO.: AD-A093499	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): DESIGN CONSIDERATIONS FOR PHASED ARRAY MODULES	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, 1 Mar 77 — 30 Sep 79
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): John R. Forrest, A. A. deSalles, J. J. Austin, J. G. Schoenenberger	8. CONTRACT OR GRANT NUMBER(s): AFOSR-77-3238
9. PERFORMING ORGANIZATION NAME AND ADDRESS: University College London, Electronic & Electrical Engineering Dept, Torrington Place London WC1E 7JE, UK	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61102F, 2305J423
11. CONTROLLING OFFICE NAME AND ADDRESS: Deputy for Electronic Technology (RADC/EECT), Hanscom AFB MA 01731	12. REPORT DATE: November 1980
	13. NUMBER OF PAGES: 418
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Same	15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Sheldon B. Herskovitz (RADC/EECT)

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Active phased array radar, radar transmit/receive modules, intermediate frequency phase shifters, phase locked loop control of microwave sources, microwave integrated circuit radar modules, Computer Programs, Software.

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The report describes work carried out on the design of X-Band (10GHz) transmit/receive modules for use in active phased array radar. A heterodyne phase locked loop is used to synchronize the r.f. source in each module to a common reference. Beam steering for an array of modules is accomplished by phase shifting the intermediate frequency reference to each module, thus avoiding the use of microwave phase shifters. An eight element array of modules was constructed and beam steered (Cont'd)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

405010

Item 20 (Cont'd)

radiation patterns are given in the report. A particularly simple digital control and monitoring system for the i.f. phase shifters is described. Finally, the design and construction of the modules in microwave integrated circuit form with 10W pulsed Gunn diodes is described.

Evaluation

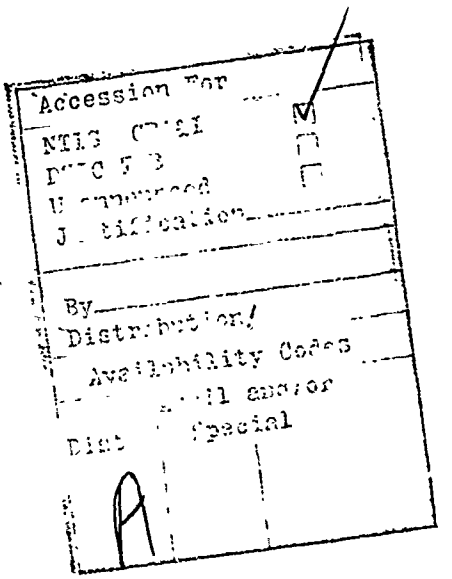
1. This is the Final Report on the contract covering the period 1 March 1977 to 30 September 1979. The object of this research was to design X-band (10 GHz) transmit/receive modules for use in active phased array radars. In particular, the modules employed a heterodyne phase locked loop technique for synchronizing array elements. Beam steering was accomplished by phase shifting the intermediate frequency reference to each module. The technique therefore eliminated the use of costly and less efficient microwave phase shifters.

2. The design and construction particulars of an eight-element array of modules are given in this report. Measured radiation patterns are detailed.

3. This report is an extremely comprehensive document detailing the traditional approach to phased array applications, status of available solid state microwave generators, synchronizing techniques, array design, phased-locked loop concepts, and overall design criteria. The thoroughness of this report gives it a value far beyond that of a mere documentation of a contractual effort.

Sheldon B. Herskovitz

SHELDON B. HERSKOVITZ
Project Engineer



ABSTRACT

The electronically steered active phased array combines, for radar applications, the advantages of electronic beam scanning with the advantages of solid state microwave power generation. Despite their attractions, however, as a result of their high cost, few of these arrays have in fact been built.

The work described in this report is based on the investigation of novel approaches to the design of elements for active arrays, particular regard being given to the element cost. Emphasis has been given to element design based on the use of synchronized oscillators, as opposed to the more common approach using amplifiers. The use of both injection locking and phase locked loop synchronization of oscillators are considered.

Following a review of the current powers and efficiencies obtainable from microwave semiconductor devices, analyses of the steady-state and transient characteristics of phase locked loops and injection locked sources are given, with reference to the effect of these characteristics on array performance.

Various element designs based on the use of injection locking or the phase locked loop are described and the latter shown to be generally more attractive. Of particular interest are the designs based on the heterodyne phase locked loop, since these permit beam-steering on both transmission and reception to be achieved using only intermediate frequency phase shifters; microwave phase shifters are thus avoided.

Results obtained with a small experimental X-Band active array of eight elements based on the heterodyne phase-locked loop are described. Beam steering with simple control from a PROM controller using a novel design of intermediate frequency phase shifter has also been demonstrated. Finally, the integration of the element design into m.i.c. form with unpackaged active devices is described, being the first stage in a full development programme.

CONTENTS

ACKNOWLEDGEMENTS

A large part of the work described in this report represents research submitted by J.Austin to the University of London in regard to requirements for the Ph.D degree.

Financial support of the project by the United States Air Force, Office of Scientific Research, is gratefully acknowledged and particular thanks are extended to Col. R. Lopina, Major D. Fairfull and Captain R. Ray (during their tour of duty at European Office of Aerospace Research and Development, London) together with Mr. S.B. Herskovitz and colleagues at Rome Air Development Centre, Hanscom AFB, Mass.

Additional financial support was obtained from Plessey Electronic Systems Ltd. and the U.K. Science Research Council, to which organisations grateful acknowledgement is made.

For encouragement and useful discussions, thanks are due to Professor A.L.Cullen, Professor K.Milne and Dr. R.E.Hayes. Finally, acknowledgement is gratefully made to Drs. M.Brinson and L.Parsons of the Polytechnic of North London for assistance in construction of the thick film microwave integrated circuit modules, and to Mr. A.D. Williams of U.C.L. for construction and testing of the modules and array.

ABBREVIATIONS

CW	Continuous Wave
FET	Field Effect Transistor
FM	Frequency Modulation
FMCW	Frequency Modulated Continuous Wave
HPLL	Heterodyne Phase-Locked Loop
IF	Intermediate Frequency
LSA	Limited Space-Charge Accumulation
MIC	Microwave Integrated Circuit
PLL	Phase Locked Loop
PSD	Phase Sensitive Detector
RF	Radio Frequency (Microwave Frequency)
SAW	Surface Acoustic Wave
VCO	Voltage Controlled Oscillator

Introduction

The concept of the active phased array antenna, in which a solid state source of microwave power is provided at each element of a phased array, is particularly attractive for many radar applications. The advantages associated with electronic beam steering, as opposed to the mechanical scanning of conventional radars, are well established : the flexibility afforded by the phased array enables it to perform the functions that would typically require several independent, mechanically steered radars.

The use of solid state sources for the generation of the transmitted power, instead of the conventional vacuum tube, has additional advantages, particularly with regard to the increased reliability and also with respect to the reduced size, weight, and power supply voltages. Although the reliability of individual solid state devices is far in excess of that of vacuum tubes, the large number of elements that will typically be used in an array antenna increases the statistical likelihood of failures ; these failures will however, give rise to only a ' graceful degradation ' of the array performance with time as some of the element sources fail.

The active array is a particularly suitable vehicle for the introduction of solid state sources for generation of the transmitted signal. The power available from individual solid state microwave devices is very much less than that available from typical vacuum tube transmitters, and at present, it would appear very unlikely that any individual solid state device capable of generating these power levels will appear. Clearly, high power levels may be achieved by operating many solid state devices in parallel, and the construct-

ion of a high power vacuum tube replacement consisting of a complex power combining circuit and a large number of solid state devices, is conceivable. The active array approach is far more attractive however, since the power summation in this case simply occurs in space.

Noting the advantages described above, serious interest in active arrays began in the 1960s when solid state devices producing significant microwave powers began to appear. The MERA[1] program was an ambitious early example of an active array, using in this case transistor element sources followed by varactor multipliers. Despite general acceptance of their desirability, and the considerable effort expended on their development, very few active arrays have in fact advanced beyond the demonstration model stage; the reason for this can be quite clearly attributed to their very high cost in comparison to conventional radars. This has limited their use in practice to a relatively small number of fairly sophisticated military applications.

In this light, the work descibed in this report has had the objective of investigating novel approaches to the design of modular, transmit and receive, active element circuits, with particular regard being given to the use of locked oscillator element sources, as opposed to the more common amplifier approach.

Since a wide range of topics have been considered in the course of this work, a brief description of the contents and relative position in the work of each of the following chapters is given below.

Chapter 2 serves as a more detailed introduction to the background of active arrays. Initially the characteristics and applications of phased arrays in general are discussed, and the techniques that have been devised for reducing the cost of passive element arrays (i.e. phased arrays driven by a single source) are reviewed. The active array concept is then discussed in more detail and the available approaches for effecting any simplification or cost reduction are highlighted. The previous work at U.C.L. on active arrays is also described. Finally, the characteristics of PIN and ferrite phase shifters are reviewed for comparison with phasing techniques described in subsequent chapters.

As a first consideration for active element design, a review is initially given in Chapter 3 of the power and efficiency that may be obtained from the major existing solid state microwave sources. This serves to indicate first the most suitable chioce of solid state device at any particular frequency, and secondly to indicate the level of radiated power that can realistically be achieved from an active array with a given number of elements. Transistor sources (bipolar and FET), avalanche devices (Impatt and Trapatt) and transferred electron devices (Gunn and LSA) are considered. Also briefly mentioned in this chapter are recent developments being made in the field of FET low-noise preamplifiers.

When the solid state source used in each element of an active array takes the form of an oscillator, synchronisation of the oscillator to a common reference signal for the array will be required in order to form a coherent output. In Chapter 4 the two means of oscillator phase locking, represented by injection locking and the phase-locked

loop are described. An analysis is given in each case of the steady -state and transient performance that may be obtained, and the relative merits of these forms of oscillator locking are compared. Since previous work at University College London has looked in detail at the characteristics of injection locked oscillators, particular attention has been given here to the phase-locked loop analysis.

In Chapter 5 several basic aspects which influence the details of practical element designs are considered. Specifically, the implication on the element design of the desire to provide tapering of the aperture distribution for radiation pattern sidelobe control is considered ; an assessment is made of the required amplitude and phase accuracy to realise a given sidelobe level ; and the effect on reception of various element receiving configurations is considered.

Active element designs based on the use of injection locking for the synchronisation of the element source are described in Chapter 6. Several element circuits are considered and specific points related to their performance are examined.

In Chapter 7 various element designs based on the use of the phase-locked loop are described. Particular attention is given to elements based on the heterodyne form of the phase-locked loop, since these are particularly attractive in allowing beam-steering on both transmission and reception to be achieved with only intermediate frequency phase shifters. The cost and loss associated with conventional microwave phase shifters may be avoided in these designs. Various circuit configurations are examined, and two in particular are presented as being particularly attractive.

In Chapter 8 a novel form of digital intermediate frequency phase shifter is described, which is particularly suitable for use in conjunction with the element designs of Chapter 7. The phase shifter uses a harmonically locked phase-locked loop to provide a higher level of phase accuracy than is available for most intermediate frequency phase shifters.

An experimental four element active array demonstrating the use of the element designs based on the heterodyne phase-locked loop is described in Chapter 9. Details of the element construction, and measured broadside and steered radiation patterns produced by the array are presented.

In Chapter 10, the extension of the array to eight elements and the inclusion of a simple digital beam controller based on stored phase shifter codes in a programmable read-only memory (PROM) is described. Again, measured broadside and steered beam radiation patterns are presented.

Chapter 11 presents the design of a microwave integrated circuit (m.i.c.) version of the prototype array element previously developed. This allows investigation of a higher power output microwave source and some insight into the feasibility of the element for mass production.

Finally, in Chapter 12, conclusions are drawn regarding this approach to active element design and its future application areas.

CHAPTER 2

PHASED ARRAY ANTENNAS

2.0 Introduction

2.1 Characteristics and Applications of Phased Arrays

2.2 Passive Element Arrays

- 2.2.1 Frequency Scanning
- 2.2.2 Array Thinning and Techniques for Grating Lobe Suppression
- 2.2.3 Optical Feeds

2.3 Active Element Arrays

- 2.3.1 Previous Work on Active Arrays at University College London

2.4 Microwave Phase Shifters for Array Antennas

- 2.4.1 Ferrite Phase Shifters
- 2.4.2 PIN Phase Shifters
- 2.4.3 Other Phase Shifter Types

2.0 Introduction

The purpose of this chapter is to review the advantages, applications and limitations of phased array antennas as a background to the work described in subsequent chapters on active arrays. Initially a review is given of the desirable properties that have led to the development of phased arrays, the main factor influencing their cost, and techniques adopted for cost reduction in conventional, passive element arrays. The active array concept, in which each array element is associated with an individual source of RF power, is then discussed and previous work in the field considered. Finally the characteristics of PIN and ferrite phase shifters, which have previously played a dominant role in electronic scanning, are described for comparison with phasing techniques presented in later chapters.

2.1 Characteristics and Applications of Phased Array Antennas

The principal feature of the phased array antenna is its ability to electronically vary its aperture phase distribution, resulting in inertialess and very rapid control of the main beam direction and shape. The advantages of this have long been recognised and considerable effort has been devoted to the development of the phased array[2], initially and still primarily for military radar applications.

Electronic beam steering has obvious advantages arising from the replacement of the conventional rotating radar antenna with a fixed system. The avoidance of the need to physically move large and heavy antenna structures, has alone promoted the phased array for the long range surveillance radars operating at UHF or low microwave frequencies

for which very large apertures are used. More often however, it is the increased beam agility that is the principal desirable feature ; electronically variable phase shifters, normally introducing digital phase increments allow repositioning of the beam in any direction within microseconds.

It is notable that the main advantage of beam agility is in the target tracking mode and not the surveillance mode of operation. The rate of rotation of a surveillance beam is basically limited by the time required to receive radar returns from targets at the maximum range ; this rate of scan is achievable mechanically in most circumstances. The update time (or data rate) for target tracking with a mechanically rotated antenna is simply the time required for the antenna to complete a revolution, typically 1 - 10 seconds, depending on the beamwidth and maximum range. For fast moving targets this will usually be inadequate and thus several additional independent tracking radars will be required for multiple target tracking. The inertialess beam positioning of the phased array, however, allows the directions containing targets of interest to be examined at any time during the surveillance sweep with a frequency that may be adaptively controlled according to the interest in that target. Many targets may be simultaneously tracked and the relative proportion of time allocated to tracking, surveillance or high data rate surveillance in particular directions, can be varied at will. It is this multifunction capability, allowing the phased array to perform the functions that would require several mechanically scanned radars, that is the main attraction of the phased array. Additionally, there is also the possibility of multiple beam formation from a single aperture, the lack of scanning modulation and the inherent flexibility of the aperture layout (conformal arrays).

The primary application for phased arrays is in the radar field, both monostatic and bistatic[3] but other applications include scanning beam microwave landing systems, satellite communication antennas, and inertialess motion compensation for aircraft and ship communication antennas.

Despite the notable advantages of phased arrays and the considerable development effort expended on detailed analysis of their design and operation, very few have advanced beyond the prototype or demonstration model stage. The reason for this can be fairly simply attributed to cost ; the very high cost of design, manufacture and operation has mainly limited the application of fully-phased arrays i.e. two dimensional arrays with electronic scanning in two planes) to sophisticated, high performance radars for which they are the only effective technical solution. At a lower level of complexity and cost, arrays with electronic scanning in only one plane have seen more use, although these clearly do not have the advantages of fully agile beam types. One notable application of single plane scanning has been to provide electronic elevation scanning for mechanically rotated antennas, thus enabling three dimension pencil beam operation to be achieved.

Apart from the operational and maintenance cost of phased arrays, three areas representing particularly high expenditure, can be identified, the first two of which are in the province of the antenna designer :

1) The array elements, particularly the phase shifters. Although the cost of one element alone may not be particularly high, since hundreds or thousands of elements are typically used in an array, the element cost clearly takes on considerable importance. The

microwave phase shifter (e.g. a PIN or ferrite type) often represents a large part of the element cost.

2) The distribution/combining network. If a single microwave source is employed to generate the transmitter power, a low loss distribution network, often constructed in waveguide, will be required to feed the array elements. The construction complexity of a waveguide feed will introduce considerable expense.

3) The beam steering and control computer. As computational costs are decreasing the relative expense of this is being reduced, but nevertheless fairly sophisticated processing is required to control a high performance, automated, multi-function radar.

2.2 Passive Element Arrays

The majority of phased array development effort in the past has been devoted to arrays in which the microwave energy is developed in a single source such as a magnetron before being distributed to the array phase shifters and radiating elements. Such an array may be termed a ' passive element array ' or simply a ' passive array ' in comparison to the ' active array ' in which microwave power generation is accomplished additionally within the array elements. Passive arrays have previously been favoured since the power available from solid state microwave sources has in the past been insufficient for most radar applications and it is generally inconvenient to incorporate distributed power generation from vacuum tube sources due to their size, weight, and power supply requirements.

Many ingenious techniques have been developed to reduce the cost of passive arrays, either by reducing the number of elements and phase shifters or by avoiding a complex feed network. To compare the ap-

plicability of these techniques to active arrays, the more important ones are briefly summarized below.

2.2.1 Frequency Scanning

Frequency scanning represents a simple and relatively widely used method of electronic scanning and avoids the expense both of phase shifters and a complex feed network. The array elements, which for a linear array could typically take the form of waveguide slots, or for a two dimensional array, slotted waveguide columns, are usually separated in a series feed by a distance giving a fixed time delay Δt between them. The angular deviation Θ of the main beam from the broadside direction is then given by

$$\Theta = \sin^{-1} \frac{\lambda . \Delta t}{d} \left(f - \frac{n}{\Delta t} \right) \qquad \ldots\ldots 2.1$$

where λ is the free space wavelength

d is the inter-element spacing

f is the frequency

and n is an integer

The rate of change of the beam pointing direction with frequency is clearly dependent upon the inter-element delay Δt. A slow-wave or serpentine feed structure is normally adopted for use with frequency scanned arrays to enhance the rate of scan with frequency compared to that for a simple waveguide series feed.

The use of frequency scanning for two dimensional beam steering in a planar array has been proposed[4] . s widely different rates of scan with frequency are used to obtain a beam that scans rapidly and

repeatedly in one plane, whilst simultaneously scanning relatively slowly in the other. The constraints imposed by limitations on the bandwidth and the delay that may conveniently be incorporated between elements, make this approach unattractive however. A relatively inexpensive technique for providing electronic beam steering in two dimensions with a planar array is to combine frequency scanning in one plane with phase scanning in the other ; a relatively small number of phase shifters are employed in this arrangement to introduce a phase gradient between the frequency scanned columns or rows.

One fundamental limitation of frequency scanning for military applications, is the direct relationship between the beam-pointing direction and the frequency ; the fact that the frequency of the transmission in any direction is always predictable makes such a radar susceptible to jamming.

2.2.2 Array Thinning and Techniques for Grating Lobe Suppression

A reduction in the total number of array elements while maintaining the same aperture dimensions serves to reduce both the cost of the element array and the distribution network. The immediate problem that arises with thinned arrays however is that of grating lobes ; if the number of equally spaced elements in a given aperture area is reduced simply by increasing the spacing between them, grating lobes (undesired secondary lobes with the same amplitude as the main beam) will start to appear at large scan angles. Two techniques for reducing the effects of grating lobes in thinned arrays are described below.

Random Thinning

In the random thinning technique[5], an array with the conventional approximately half-wavelength spacing is initially considered. Elements are then removed from the array at random until the desired number of elements remains. Although there will clearly be many inter-element spacings in the array greater than one half-wavelength, the lack of periodicity in the positioning of these prevents the formation of distinct grating lobes, the energy associated with the normal grating lobe being now widely distributed in angle and giving rise to a general increase in the sidelobe level. It is of interest to note, as described in more detail in Chapter 5, that density tapering, a variation of the random thinning technique, may also be used to effectively provide an amplitude taper across the aperture[6] for sidelobe control.

Grating Lobe Suppression Via the Element Pattern

The pattern multiplication theorem states that the array radiation pattern is the product of the array factor and the element factor. Grating lobes in the array factor of an array with uniform wide inter-element spacing may be tolerated if adequate suppression may be obtained at these angles via the element pattern. The element aperture is generally of insufficient size to provide adequate suppression, but two techniques have been proposed for increasing this. Belcher[7] developed a method of tapering the walls between waveguide radiating elements down to a series of posts at the aperture. The effect of this is to provide an effective element aperture extending over several conventional elements, therefore providing a greater rate of cut-off of the element pattern. Hazeltine Inc.

have developed a technique for their COMPACT array, designed for scanning beam microwave landing systems, in which every element is coupled to all others by a series of couplers and amplitude weights in the feed network. The effective element aperture is in this case of the same size as the array itself. For a restriction on scan angle of $\pm 20^{\circ}$ for example, only 15 elements and phase shifters are typically required for a 2° beamwidth array.

One other technique related to element thinning, that reflects the high cost of microwave phase shifters, is that of phase shifter thinning. This technique, described by Cheng[8], reduces only the number of phase shifters (whilst maintaining a filled aperture) by using a single phase shifter to drive several neighbouring elements. Random distribution of the co-phased blocks of elements is used to avoid excessive sidelobe degradation.

2.2.3 Optical Feeds

The cost of the feed network for a phased array can be significantly reduced by the use of an optical feed approach, in which the microwave energy is distributed to the array elements via free-space transmission. Each array element receives part of the energy radiated by the primary feed, and after the application of appropriate phasing, the energy is re-radiated. Optically fed systems using both transmission through the array (i.e. use a phase shifter lens) and reflection from the array have been developed.[9]

2.3 Active Arrays

In the active array a microwave source, either amplifier or locked

oscillator, is included within each element so that final amplification of the transmitted signal is provided at this point. One advantage is apparent in that the feed network loss is less critical when final amplification occurs at the aperture, but the principal reason for the development of the active array concept is that it is a particularly convenient way of introducing solid state sources for the generation of transmitter power. The power available from single solid state microwave sources is insufficient for most radar applications and equivalent power to that of microwave tubes can only be obtained by combining the powers of many individual sources, operated in parallel. Although it may be possible, using many sources and a complex power combining circuit, to produce a direct solid state replacement for a vacuum tube source, the distribution of solid state sources in the elements of an active array is far more convenient ; summation of the individual power then simply occurs in space.

The advantages of the use of solid state sources over the use of vacuum tubes include reduced size and weight, reduced power supply voltage and increased reliability. Although the reliability of individual solid state sources will be far in excess of that of vacuum tubes, the large number of solid state sources used will increase the statistical likelihood of some failures. However, the active array will only suffer a relatively slow ' graceful degradation ' of performance compared with the disabling failures that occur for vacuum tubes. Consider as an example a planar array of 100 x 100 elements, which for half-wavelength inter-element spacing and uniform illumination will produce a pencil beam of beamwidth $\sim 1^{\circ}$. Assuming a mean time to failure of 10^{6} hrs for the individual devices (an estimated value for Gunn or Impatt devices), and

assuming for simplicity that the probability of failure is constant with time, it may be seen that 1 element source will fail every 100 hours. One percent of the devices in the array will have failed after 10^4 hrs ; ten percent of the devices will have failed after 10^5 hrs. It is probably at around the 10% failure level that the effect on the array perfo:mance will be becoming significant.

The limitation on the application of active arrays is again that of high cost, particularly that of the array elements, and again only a small number of these arrays have in fact been built. A notable large example is the U.S.A.F's Pave Paws radar [11]. The techniques available for reducing cost for active arrays are, however, somewhat restricted. Frequency scanning may still be employed to avoid the expense of phase shifters, but the bandwidth that may be used for this is now restricted by the solid state source ; where locked oscillator element sources are used, for example, the frequency must clearly remain within the range for which lock can occur, and in practice may be even further restricted due to the possibility of phase errors between elements. This is described in more detail in Chapter 4.

The thinning and wide element spacing techniques are not always applicable to active arrays ; in a passive array the power transmitted from a thinned or widespaced array is the same as that of a filled aperture, since the feed is rearranged to apply all the power into the remaining elements. In an active array in which the element output power is limited to a certain peak value by the solid state source, a reduction in the number of elements will produce a similar reduction in radiated power.

Accepting that a reduction in the number of elements is not always practical, it is clear that the element cost is of paramount importance, and it has therefore been to the reduction of active element cost that much of the work at U.C.L. on active arrays has been aimed.

2.3.1 Previous Work on Active Arrays at University College London

With the background described above, previous work at U.C.L. focussed principally on the investigation of novel techniques for reducing phase shifter costs in active arrays , the phase shifter typically representing a large proportion of the overall element cost. Arrays for transmission only were considered in this initial work.

A reduction (by a factor of 2 for a linear array and 4 for a planar array) in the number of conventional microwave phase shifters required in a transmitting array was obtained with the interpolation locking technique[12] . This was achieved by making use of the mutually coupled signal from alternate elements in an array to injection lock the oscillators of intermediate elements. Since the phase of the mutually coupled signal has the mean phase of the neighbouring elements (which is exactly that required on the intermediate element output) no direct locking signal or phase shifter is required for these elements.

The other technique previously investigated avoided the use of conventional microwave phase shifters entirely by using the harmonically locked phase shifting principle initially proposed by Cullen[13]. Though it is normal to synchronise an injection locked oscillator to a reference signal which is close in frequency to the free running frequency of the oscillator, a similar locking can be obtained if

the reference is close to a harmonic of the free-running frequency. However, since each cycle of an nth harmonic frequency corresponds to 1/nth of a cycle of the fundamental, and each harmonic cycle is identical as regards the locking process, the fundamental output of a harmonically locked oscillator may be synchronised at a series of phase positions, each separated by exactly $2\pi/n$ radians. By providing control of the phase position at which the oscillator is locked, a digital phase shifter with phase increment $2\pi/n$ radians may be formed. The use of this technique for synchronising and phase shifting the element sources in an active array was described by Al-Ani, Cullen and Forrest[14].

In a similar context, the objective of the work described in this thesis has been the investigation of low cost active element designs for both transmission and reception, with again particular consideration being given to the use of locked oscillator element sources, as opposed to the relatively well established amplifier approach.

2.4 Microwave Phase Shifters

Noting the importance of the phase shifting function in any active element design, a brief review of the characteristics of established microwave phase shifting devices is given below. Initially the basic desired phase shifter characteristics may be summarised as follows :

1) Low insertion loss. Loss introduced by phase shifters at the array apertures reduces the radiated power and increases the noise figure on reception.

2) Reciprocal operation. To avoid the necessity of phase shifter switching between transmission and reception, reciprocal phase shifters are preferred.

3) Rapid switching time. The switching time should clearly be short for rapid beam steering but particularly so if non-reciprocal phase shifters are used since the switching time in this case will influence the minimum range.

4) Drive Power. Drive power should be low to minimise power supply requirements and to avoid cooling problems, particularly for mobile and airborne applications.

5) Minimum phase increment and phase error. The minimum phase increment required for a digital phase shifter will be related both to the array size and the desired sidelobe level. The approach for determining the required level of quantisation is discussed further in Chapter 5. The bit number N of a phase shifter is given by

$$\frac{360}{2^N} = \varphi_{inc}$$

where φ_{inc} is minimum phase increment.

6) Low cost. As previously indicated, the phase shifter cost can be of particular importance.

At present two phase shifter types are predominantly used for electronic scanning, using two widely different approaches. The ferrite phase shifter uses the interaction with the bulk medium over an extended region of propagation to effect a phase shift. In contrast the PIN diode of a semiconductor phase shifter acts essentially at a point, providing a switching function.

2.4.1 Ferrite Phase Shifters

Phase shifting with ferrite devices is achieved using the change in permeability which occurs with application of a magnetic biasing field. The magnetic properties of ferrite are due to the spinning motion of the electrons within the material, which form tiny magnetic dipoles. When placed in a magnetic field the dipoles tend to align themselves with the direction of the applied field. If an r.f. magnetic field whose directional is orthogonal to the dc magnetic field is applied, the magnetic moments experience a torque which causes them to precess about the applied d.c. field. The permeability, which is related to the gyroscopic frequency, can be changed by adjusting the static magnetic field. Non-latching phase shifters use a constantly driven external coil to provide a fully variable magnetic field. Latching devices use the remnant magnetisation left in the material by a pulsed coil.

Three configurations have been found to be of practical interest :

1) The Reggia-Spencer Phase Shifter

This phase shifter, the form of which is sketched in Fig. 2.1, is a reciprocal non-latching type, consisting of a ferrite rod supported inside a standard waveguide section, with a solenoid wound around the waveguide to apply a longitudinal magnetic field. Despite its basic simplicity this type has seen little use in the phased array application. The main drawbacks of the design are a) the high level of drive power required, arising partly from the fact that a DC holding current must be applied to the coil to maintain the magnetic field and partly from eddy current losses in the waveguide walls; b) the long switching time required (typically $>100\mu s$) to change the magnetic field via the external coil.

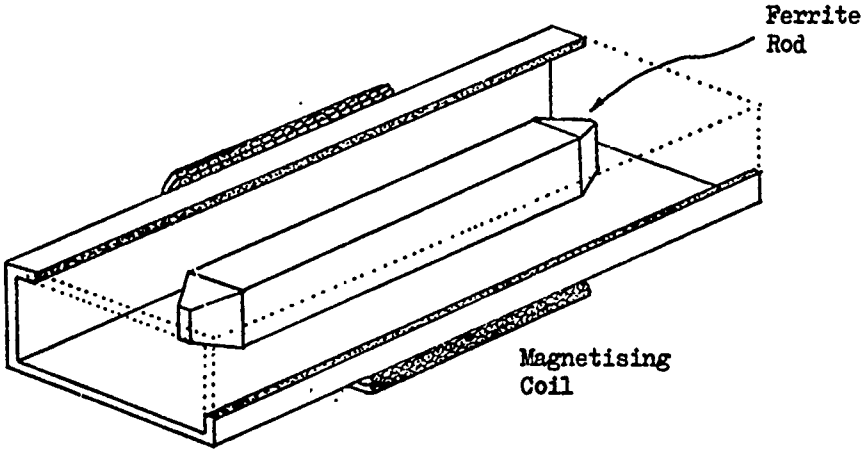


Fig. 2.1 The Reggia-Spencer Ferrite Phase Shifter

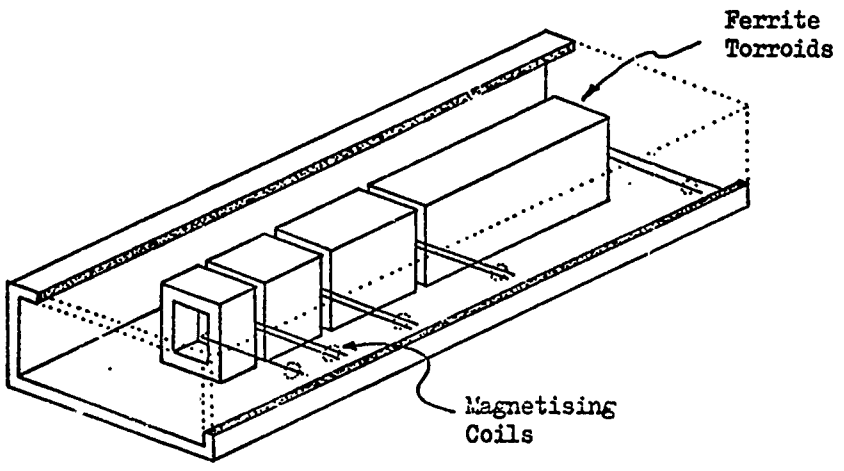


Fig. 2.2 The Waveguide Torroidal Ferrite Phase Shifter

2) The Toroidal Phase Shifter

The toroidal configuration, which is by far the most widely used, produces a non-reciprocal, latching device. Ferrite toroids of length proportional to the amount of phase shift to be introduced by each section are threaded with wires to which the magnetising pulse currents are applied. A waveguide form of the phase shifter is shown in Fig. 2.2, although microwave integrated circuit realisations more suited to active array elements are also possible[9] In addition to ferrite loss, loss can be easily introduced in this design by the generation of higher order modes in the guide ; in practice it is common to introduce a resistive sheet into the guide to suppress these[2] ; typically losses of $\lesssim$1dB are then obtained. One of the main attractions of the torroidal design is high switching speed, which is typically 2 - 5μs, although times down to 1μs are quoted. This is considerably faster than that available with other ferrite designs.

The required drive power of latching devices is normally quoted in terms of the switching energy and the repetition rate ; the energy required to switch the ferrite toroid between oppositely magnetised states is expressed in terms of the hysteresis loop area . Typically the required switching energy for a 4 bit, C band device with all bits changing simultaneously is$\sim$1mJ (Electromagnetic Sciences Inc., Data Sheet 7306). Assuming a switching rate determined by a radar pulse repetition interval of 100μs, an average driver power of 2W will be required. It may be noted that this level of power can create cooling problems in large arrays ; for instance a 100 x 100 element array will dissipate 20KW of drive power.

The well known temperature dependence of ferrite phase shifters can be distinctly improved using the flux drive approach[2] in which the ferrite is switched around only a minor hysteresis loop, the ferrite not being driven into the temperature sensitive saturated regions in either state. Quoted temperature ranges of -10° to $+60^{\circ}C$ are then obtained.

The frequency range of toroidal phase shifters extends up to 30GHz with power handling typically up to tens of KW. Bandwidths typically between 3 and 10% are obtained in practice.

3) The Dual Mode Phase Shifter

The dual mode phase shifter uses a Faraday rotator in conjunction with a ferrite quarter-wave plate at each end to realize a reciprocal device considerably faster than the Reggia-Spencer design. Recent designs employ a small square waveguide completely filled with ferrite ; in practice the waveguide wall is simply plated on the ferrite bar. The reported results indicate that the performance of this design is only slightly inferior to that of the toroidal with regard to loss and bandwidth.

2.4.2 PIN Phase Shifters

The PIN diode in diode phase shifters is essentially used as a switch, either to switch between alternative electrical paths or to switch the reflection coefficient of line terminations. An advantage of PIN phase shifters is that all types are reciprocal and generally provide faster switching speeds than ferrites. The principal PIN phase shifter types are :[15]

1) Hybrid Coupled.

This arrangement, one section of which is shown in Fig. 2.3, uses a 3dB quadrature hybrid coupler for each phase bit, and is now the most widely used. A signal appearing at port 1 is split with equal amplitudes but quadrature phase between ports 3 and 4. For the 180° phase bit, PIN diodes placed at these outputs provide essentially an open circuited or short circuited termination, with the result that the reflected signal appears at port 2 with either 0° or 180° phase shift. Smaller phase steps are obtained from the 180° bit by the transformed switch method[16], the PIN diode now being coupled to the hybrid via an ideal transformer of appropriate transformation ratio and $\frac{1}{8}$ wavelength of transmission line. A phase shifter of the required bit number is then formed by placing several sections with the appropriate phase increment, e.g. $22\frac{1}{2}^{\circ}$, 45°, 90° and 180°, in series.

The phase shifter insertion loss, typically 1 - 2dB for a 4 bit device, has two components. The lower limit of the insertion loss that may be obtained results from the non-ideal switching characteristics of the PIN diode ; the diode does not appear either as an ideal open circuit or an ideal short circuit in its two states. For equal dissipation in the diode under forward and reverse bias (for the same diode mismatch in the two states) Stark[2] gives an approximate expression for the minimum loss of a single bit (providing phase shift $\Delta\varphi$) as

$$\text{Insertion loss (dB)} = \frac{17.27\, f}{f_c} \sin\left(\frac{\Delta\varphi}{2}\right) \qquad ..2.2$$

where f is the operating frequency

and f_c is the diode cut-off frequency.

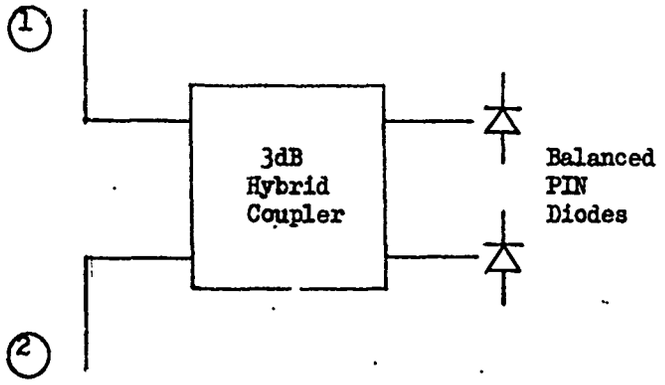


Fig. 2.3 A Hybrid Coupled Phase Shifter Section

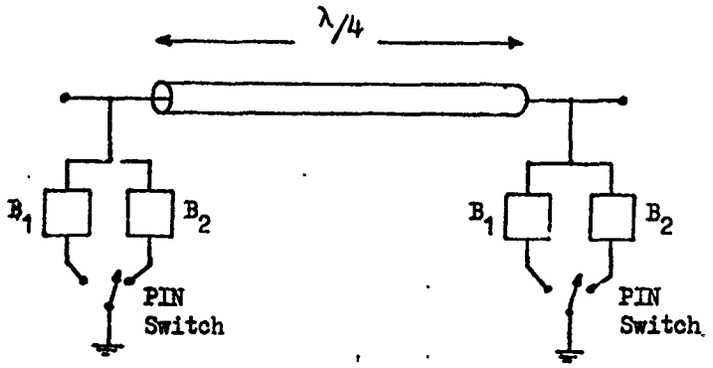


Fig. 2.4 A Loaded Line Phase Shifter Section

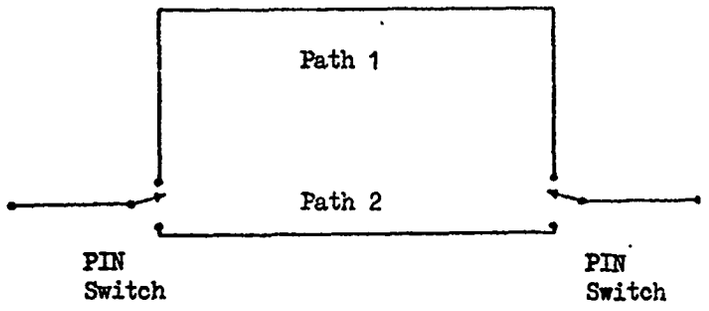


Fig. 2.5 A Switch Line Phase Shifter Section

Taking for example f = 10GHz and a typical cut-off frequency of 300GHz, the minimum insertion loss of a four bit phase shifter (180^{o}, 90^{o}, 45^{o} and 22.5^{o} steps) is $\sim$1.4dB. The other component of the insertion loss is simply that due to circuit losses, which for the TEM modes commonly used, is typically $\sim$ 0.5dB, giving, for the example, an overall insertion loss of $\sim$ 1.9dB.

The bandwidth of the hybrid coupled design is basically restricted by the bandwidth of the transformers used ; typically 10% bandwidths are obtained in practice. Phase shifting speeds are strongly dependent on the required power handling capability; for low power applications (approximately $<$ 1W) switching times down to $\sim$ 50ns can be achieved; for higher powers switching times $\sim$ 1μs are more often obtained. Only two diodes per bit are required for this design.

2) Loaded Line

The loaded line configuration, shown in Fig. 2.4 uses switched loading susceptances spaced a quarter wavelength apart along a transmission line. This arrangement is chosen since the symmetric shunt susceptances (or series reactances) will have mutually cancelling reflections providing their normalised susceptances (or reactances) are small compared with unity. The loading susceptances are switched between capacitative and inductive states to achieve the phase shift, however, due to the restriction on magnitude of susceptance, only a limited phase increment, e.g. 45^{o}, may be obtained from each section for good VSWR.

Many sections are thus required to form a complete phase shifter, leading to higher losses and cost than the hybrid coupled type.

The attraction of this configuration, however, is in power handling capability since many diodes are now used to share the phase shifting task.

3) Switched Line.

The most obvious means of obtaining phase shift is to switch between different electrical paths , the change in electrical length therefore providing the phase shift. Each phase shifter section, shown in Fig. 2.5 now uses four diodes per bit, and is theoretically capable of twice the power capacity of the hybrid coupled circuit since no voltage doubling by reflection is produced. This configuration may be used to provide true time delay steering as opposed to the usual 0 - 360° phase steering.

For most applications except those requiring high power handling capability, the hybrid coupled arrangement is usually preferred since the minimum number of diodes are required and the insertion loss is low.

A comparison of typical performance of PIN and ferrite phase shifters is given in tables 2.1 and 2.2. In general terms, PIN diode phase shifters have advantage in

switching speed and driver complexity

reciprocal operation

temperature insensitive phase shift

lower size, weight and cost.

Ferrite phase shifters have advantage in

higher power handling capability

lower insertion loss

lower VSWR

	Toroidal	Reggia-Spencer
Insertion loss	1.0 dB	1.0 dB
Switching time	1-3 μs	0.1 - 1.0 ms
Drive power	2 watts at 1,000 pps	18 watts at 300 pps
Phase error	10^{o} rms	10^{o} rms
Transmitted power	75 kW peak; 400 watts average	100 kW peak; 600 watts average

Table 2.1 Typical Characteristics of Ferrite Phase Shifters

Insertion loss	1.0 - 2.0 dB
Transmitted power	10 kW peak; 200 watts average
Switching time	50 ns to 2μs
Drive power, including losses in drivers	1.0 - 2.5 watts

Table 2.2 Typical Characteristics of PIN Phase Shifters

2.4.3 Other Phase Shifter Types

Other electronically variable phase shifters of little importance for this application, include gaseous discharge types (variable dielectric constant), the TWT and variable capacitance types (varactors). One other type of some potential for the future is that based on the microwave FET. There is at present work going on in several establishments, e.g. Siemens at Munich and Lincoln Labs. of M.I.T. aimed at producing fully integrated, if not monolithic, FET front ends which for the active array application could include an oscillator, phase shifter low noise receiving amplifier and downconverting mixer. Phase shifters based on the use of FETs acting as switches in combination with miniature lumped element realisations of the hybrid coupler have thus also been receiving attention recently(17,18,19).

CHAPTER 3

SOLID STATE MICROWAVE GENERATORS FOR ACTIVE ARRAYS

SOLID STATE MICROWAVE GENERATORS FOR ACTIVE ARRAYS

3.0 Introduction

The major existing solid state devices that may be used for microwave power generation in an active array are reviewed in this chapter, with the aim of indicating the most suitable choice at different frequencies and showing the level of transmitted power that may be realistically achieved. The characteristics of bipolar transistors, FET, Impatt, Gunn, LSA and Trapatt devices are briefly reviewed and a graphical presentation is given of the power level and frequency range that may be achieved with each of these. The mechanism of operation of the various devices is not described here, since such a description for all the devices considered would inevitably be lengthy and since these already exist in many texts[20].

Solid state device powers are continually being updated, and therefore it has not been attempted to present exact current figures but rather to show the approximate relative power levels at present being achieved with the various devices. A comparison of device performance is made in the chapter summary.

The characteristics of obvious importance are peak power, mean power, efficiency and reliability. In most cases information on reliability is only available for specific devices used in military or communication equipment (terrestrial and satellite) but in general, the devices exhibiting the highest reliability are bipolar transistors, Impatts and Gunns (domain mode transferred electron devices) where mean lifetimes of 10^5 hours are quoted

for the latter devices.[21] The general reliability of FETs has yet to be fully established but it is notable that some FET amplifiers have been adopted for use in satellite communication systems. Where reliability is of particular importance it is usually necessary to operate devices at power levels considerably below their maximum output, since the liftime of a device is strongly dependant on its temperature. When device temperatures are excessively high, the diffusion of the contact metals into the semiconductor material represents a common source of failure.

The highest mean power that may be obtained in pulsed mode can be approximated by the power levels obtained for CW operation, since the same limitation, usually that of thermal dissipation, similarly affects both of these quantities. The difference between highest mean and CW powers that can arise in practice, results from the use of slightly different device structures to optimise the pulse performance, usually at the expense of thermal design.

Some features of the variation of the device powers with frequency, shown in Figs. 3.1 - 3.5, are worthy of mention at this stage. For most of the devices, the LSA being the notable exception, the operating frequency directly influences some aspect of the physical size of the device, for instance the length of the drift region in Gunn and Impatt diodes. Since the maximum electric field strength that may be applied to a device is limited finally by breakdown, this can lead to an inverse relationship between the maximum applied voltage and the frequency of operation, and thus a $1/f^2$ relationship between maximum power output and frequency, f being the frequency. Clearly the reduced thermal capacity of smaller higher frequency devices will lead to a reduction of the pulse power obtainable with

frequency (assuming equal pulse lengths), but in addition the state of development of device heat sinking technology plays a large part in determining the relationship between power and frequency here. The relationship between maximum output power and frequency for the thermally limited case is therefore less predictable.

Radar range performance is equally dependent on the noise figure of the receiver used as on the level of transmitted power and therefore current developments in low noise FET preamplifiers are also considered.

3.1 Transistors

Bipolar Transistors

Bipolar transistors at present dominate the field of solid state power generation from audio frequencies to 4GHz. Although Trapatt and LSA devices are capable of generating higher peak powers at the low microwave frequencies, the well established advantages of bipolar transistors have led to their nearly exclusive use in UHF, L band (1-2GHz) and S band (2-4GHz) communications and solid state radar developments. The principal advantages are

a) Well understood device/circuit interaction. This leads to well established, reproducible circuit design.

b) Relatively high peak and mean power. The powers typically available from bipolar transistors in pulsed and CW modes are shown in Fig. 3.1. It is noticeable that there is only a relatively small increase in peak power under pulse conditions. This indicates that it is a voltage rather than a thermal restriction which limits the peak output power. Much of the development of high power pulsed bipolars has in fact been due to military sponsored programmes aimed

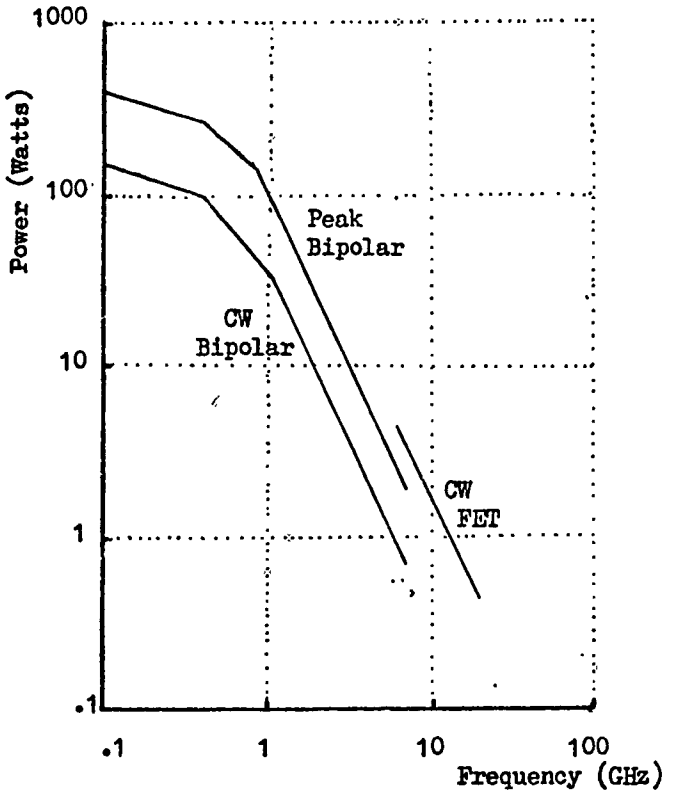


Fig. 3.1. Power Levels Obtained from Bipolar and FET Microwave Transistors

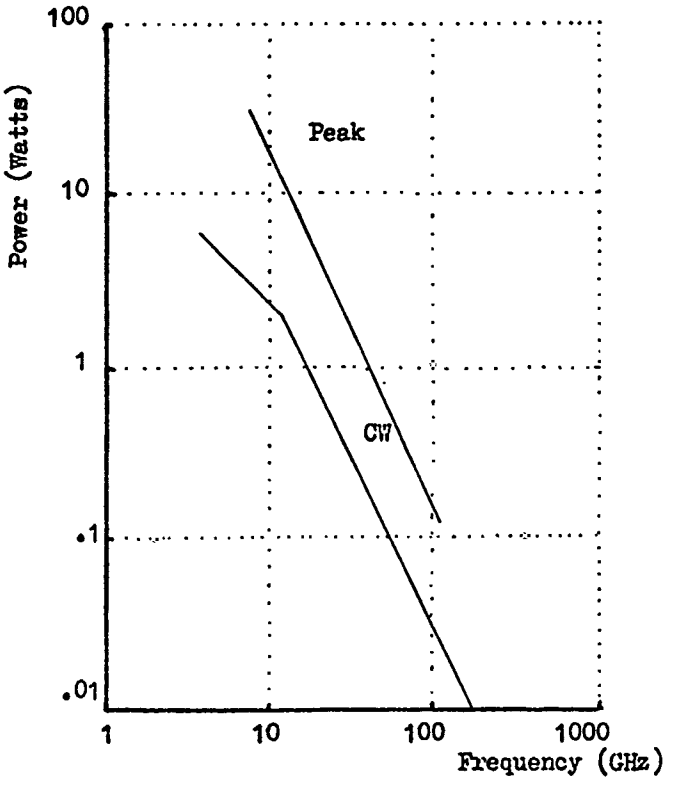


Fig. 3.2. Power Levels Obtained from Impatt Devices

at producing suitable devices for UHF and L band active phased array radars. Using several devices in parallel with a combining circuit, modular active array elements producing several hundred Watts with pulse lengths up to several ms have been produced at UHF and L band frequencies. The USAF Pave Paws active array radar for example produces 440W peak power per element module at 430MHz from 4 parallel devices, with pulse lengths up to 16 ms[11] for very long range surveillance. Pulse compression is used to improve the range resolution here.

c) Efficiency. The efficiency of bipolar transistors, typically 40 - 50%, compares well with that of microwave vacuum tubes and is significantly higher than that of most other solid state devices, with the possible exception of the Trapatt and FET.

The frequency range of bipolar transistors extends to X band (8 - 12GHz) with CW power approaching 1W at 8GHz. Before the development of avalanche and transferred-electron devices, considerable effort was devoted to varactor frequency multipliers for use with bipolar sources to generate power at frequencies above a few GHz. This technique was used in the early MERA X band active phased array in which at 2.25GHz signal amplified by bipolar transistors, was multiplied by 4 to give a radiated output at 9GHz, with 50% conversion efficiency.[9] Given a $1/f^2$ relationship between power and frequency, where f is the frequency, higher output powers can often be obtained from a lower frequency source plus a multiplier, despite multiplier loss, than from direct generation at the required frequency with the same device. The $1/f^2$ relationship reduces the available power at 6dB/octave, whilst a x2 multiplier normally introduces much lower attenuation; typically 3dB for x4 at the low microwave frequencies but increasing with frequency above this.

This relationship can be more clearly seen considering a generalised device of length l and carrier velocity v_c, with load resistance R. The output power P is

$$P = \frac{V^2}{R} \qquad \ldots\ldots\ldots 3.1$$

where V is the voltage existing across the device. In terms of the electric field strength E we have

$$V = E.l \qquad \ldots\ldots\ldots 3.2$$

and also

$$v_c = 1/\tau_t \qquad \ldots\ldots\ldots 3.3$$

where τ_t is the transit time of carriers across the device. Thus

$$P = \frac{E^2 v^2 \tau_t^2}{R} \qquad \ldots\ldots\ldots 3.4$$

Since the transit time will be approximately related to the frequency of operation f by

$$\tau_t = \frac{1}{2f} \qquad \ldots\ldots\ldots 3.5$$

we have

$$P = \frac{E^2 v_c^2}{8Rf^2} \qquad \ldots\ldots\ldots 3.6$$

The output power will be a maximum when

$$E = E_b$$

and $$v_c = v_{cs}$$

where E_b is the breakdown field and v_{cs} is the saturated carrier velocity.

Thus

$$P_{max} = \frac{E_b v_{cs}^2}{8Rf^2} \quad \ldots\ldots\ldots \quad 3.7$$

or

$$P_{max} \cdot f^2 = \text{a constant} \quad \ldots\ldots\ldots \quad 3.8$$

This relationship is commonly found with microwave semiconductors.

Where voltage breakdown is not the primary problem, heat generated within the device, resulting from the limited efficiency of microwave semiconductors, provides the restriction on power output. The use of multipliers however, considerably increases the circuit complexity, resulting in higher cost and reduced reliability, and in addition they may provide only a restricted bandwidth. Their use is therefore not usually preferred where alternative sources exist giving direct generation at the required frequency. Multipliers can, of course, be used in conjunction with any solid state source.

Field Effect Transistors

Microwave power GaAs FETs are a relatively new addition to the microwave solid state field and are at present experiencing rapid development, the usual form being the gallium arsenide Schottky junction device (MESFET). FET performance now surpasses that of bipolar devices at X band and above, with possible operation to 20GHz i.e. approximately an octave above the frequency limit of bipolars. CW results presently reported are shown in Fig. 3.1. Few results for pulsed operation are available at this time, but a large increase in peak power for pulsed mode would not be expected since voltage breakdown rather than thermal considerations are likely to limit the

device power. Increases in power to 10W or more CW at 10GHz are confidently predicted,[22] which, combined with high efficiency (~ 30%) and simplicity of fabrication, makes this device appear attractive for the future. Present costs, reflecting development expenses, are naturally relatively high.

One other aspect giving further potential to the FET is its versatility. FETs can be used for power amplification, low noise amplification, mixing (dual gate FETs) and also as switches for phase shifters as mentioned in Chapter 2. These are exactly the functions required for an active array element and there would obviously be advantage in using one device technology to achieve them all, ideally in a monolithic form. Related developments in this area are being made by Philips[19] but full integration of such an element is at present some way off. Device yield alone will probably be a limiting problem here.

3.2 Avalanche Devices

Impatts

Impatt devices presently provide the highest CW powers available above ~ 5GHz although it seems likely that FETs will soon reduce this lead. Impatts are made with a variety of doping structures in both silicon and gallium arsenide, the latter providing the highest efficiencies and by a small margin the highest powers. The efficiency of silicon devices is typically 10 - 16%, that of GaAs types 20 - 35%. Silicon devices are now tending to be restricted to the higher frequency (> 20 GHz) applications, producing directly generated power at frequencies up to 200GHz. Present power levels are shown in Fig.

3.2. Powers of several watts are available from CW devices at 10GHz with pulse powers reaching 30W at this frequency. Double drift structures, i.e. structures with a drift region on either side of the p-n or Schottky avalanche junction, are being adopted to increase power and efficiency.

Resulting from their use as communications link amplifiers, considerable attention has been given to the subject of Impatt reliability and mean lifetimes of 10^7 hrs have been predicted for devices run below their maximum output [21]

Trapatts

Trapatts, like Impatts are essentially simple two terminal avalanche diodes offering relatively high power and efficiency, particularly in this case, for pulsed operation. Although Trapatts are not, as yet, commercially available, very encouraging results have been obtained from laboratory devices and some are now being tested in military systems. Trapatts, which at present are nearly all fabricated in silicon, have been operated from 400MHz to 12GHz but their main area of application is to pulsed sources in the approximate range 1 - 5GHz, where they compete with pulsed bipolar transistors. Current power levels are shown in Fig. 3.3. Pulse powers up to 200W have been achieved from single devices using narrow pulse widths ($\sim$ 0.5 μs) in the 3 - 4GHz range, with 80W for longer 10 μs pulse widths [21]. Pulse powers over 1KW have been obtained at 1.9GHz by combining the outputs of several devices [21].

Efficiencies of the order of 30% are typically obtained, but higher levels up to 60% have been theoretically predicted. Despite out-

standing ılse performance, the CW powers of Trapatts are low, reflecting diff· ulties of heat sinking the device, higher CW power usually being ot ıined from bipolar transistors.

A disa/ antage of the Trapatt, which previously led to serious doubts about ıe usefulness of the device as a practical source, is the compl· ity of the microwave circuit design required to achieve correct opera ion. A matching circuit is required, often realised with an iris or slug tuned coaxial line, that acts as a band pass filter to the esired fundamental output, but reflects harmonics in the output back to the diode to initiate the next cycle in the oscillation. Previously, the characteristics of individual devices had to be determined to produce the necessary circuit design. This problem, along with that of leading edge jitter is now being overcome and present oscillator circuits allow field replacement of the diode given a 10% match in capacitance[19] . Device reliability is also being improved.

A characteristic of this device is that the conventional method of electronic tuning microwave oscillators with varactor diodes is not suitable for Trapatt circuits due to the need to maintain the necessary matching conditions at the fundamental output and at the harmonics, however, electronic tuning of 70MHz at 2GHz has been reported by applying a magnetic field to a ferrite substrate upon which the resonant circuit is formed[23] .

3.3 Transferred Electron Devices

GaAs Gunn devices (i.e. domain mode transferred electron devices) at present dominate the field of low to medium power generation in the 4 - 40GHz band, due to their low voltage requirements, and low

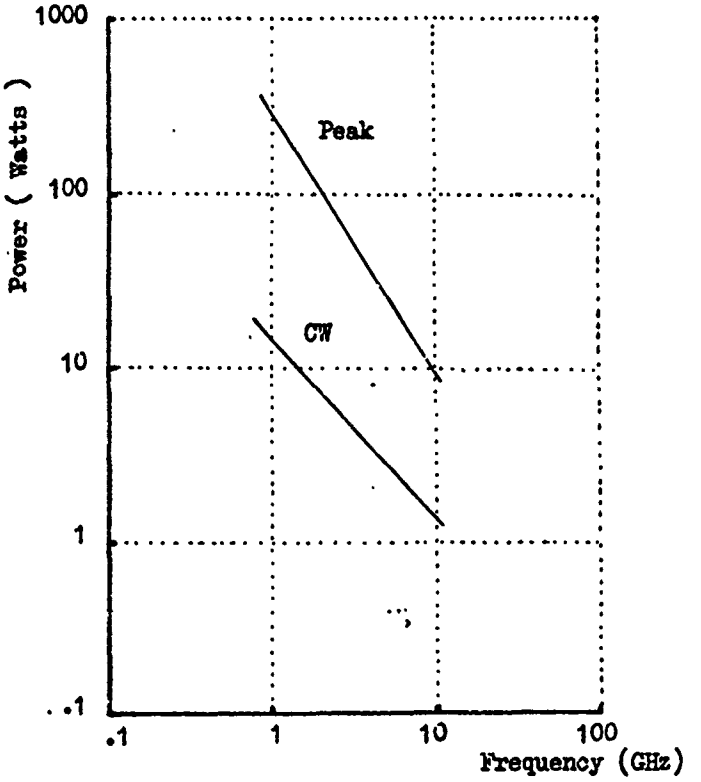


Fig. 3.3 Power Levels Obtained from Trapatt Devices

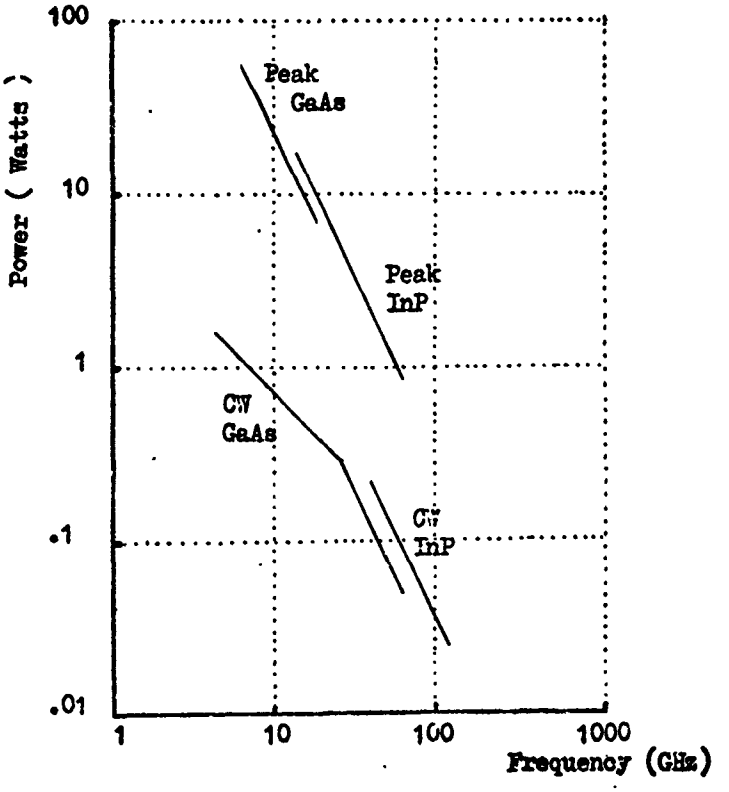


Fig. 3.4 Power Levels Obtained from Gunn Devices

noise (at least with respect to the main contender - Impatts). These advantageous characteristics usually outweigh the disadvantage of low efficiency, which is typically below 7%. The power levels achieved with higher power GaAs devices are shown in Fig. 3.4. CW powers of $\sim$ 1W are achieved at 10GHz, this being about the same as that of GaAs FETs and slightly less than that available from Impatts. In pulsed mode Gunn devices offer peak power levels at $\sim$ 10GHz which are only surpassed by LSA mode devices. For 5 μs pulse length and 0.01 duty cycle, 30W peak at 10GHz is reliably achieved from GaAs with 8% efficiency. Best current results at this frequency are at the 60W level[19].

Recent developments in InP[24,25] indicate that increased power and efficiency may be obtainable from devices fabricated in this material. Pulse powers of up to 21W peak with 15% efficiency have been achieved at 15GHz with 0.5 μs pulse length and 0.001 duty cycle. Mean powers of 1.5W at 1 μs pulse length and 0.1 duty cycle have also been achieved at this frequency. Since InP devices also exhibit a lower frequency sensitivity with temperature, yielding lower chirp (inter-pulse frequency change) of pulsed sources, it appears that this material will see increased use in future devices. The reduced scattering time of InP makes it particularly attractive for higher frequency ($>$ 10GHz) applications.

LSA Mode Devices

Transferred electron diodes operated in LSA (Limited Space-charge Accumulation) mode offer the highest pulse powers obtainable from microwave solid state devices. Although these are still below the maximum pulse powers of vacuum tubes by a factor of 10^3 to 10^4, they

represent the closest approach to a solid state vacuum tube replacement. The power levels that have been achieved are shown in Fig. 3.5. For sub-μs pulse lengths and duty cycles typically 0.001 or less, peak power up to 1KW at 8GHz has been achieved. Lower power operation with longer pulse widths or increased duty cycle is also possible. LSA devices are usually operated in pulsed mode at low duty cycle as a result of difficulties of heat-sinking the relatively large device. The problem of heat dissipation limits the mean power to no more than that obtainable from Gunn or Impatt devices and it is for this reason that CW LSA devices are uncommon. Efficiencies are typically around 20%.

The development of LSA devices has been hampered by problems in the design of the optimum bias pulse required to initiate LSA mode operation; initial operation in the Gunn (domain) mode can lead to device failure at high power level due to voltage breakdown. Poor reliability due to this effect remains a problem at present, but in other respects the device is attractive for pulse radar applications.

3.4 FET Preamplifiers

Whilst considering solid state microwave power sources for active arrays it is useful also to consider the subject of solid state microwave receiving preamplifiers, since within limits, radar range performance can be improved equally well by reducing the receiver noise figure as by increasing the transmitted power. Low noise solid state amplifiers can be used to provide distributed preamplification on reception (i.e. a preamplifier within each array element) in the same way that the power generation is distributed on transmission. The advantage of this is that the loss of the array power combining

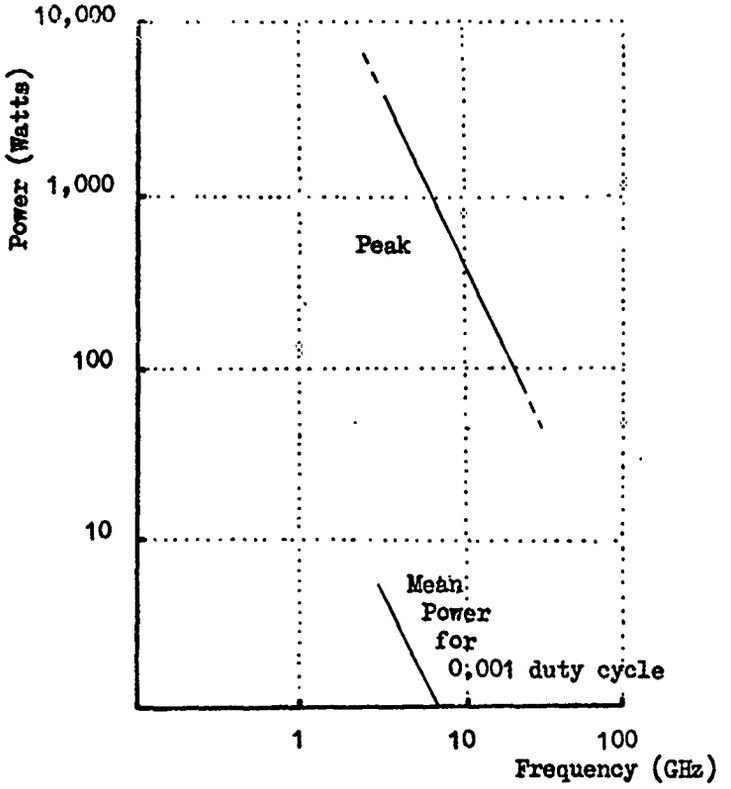


Fig. 3.5 Power Levels Obtained from LSA Mode Transferred Electron Devices

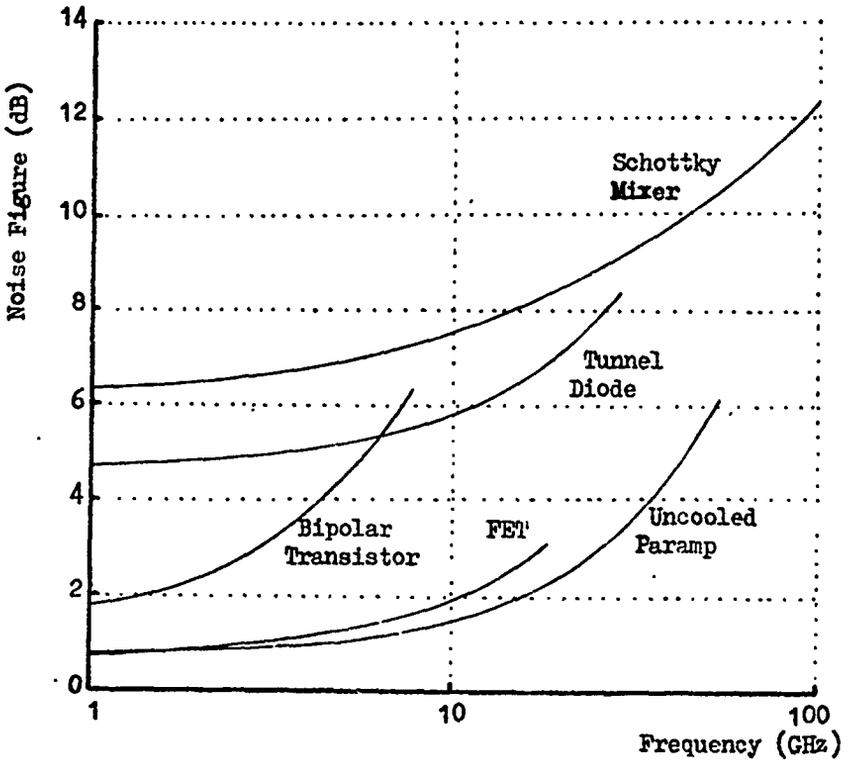


Fig. 3.6 Comparison of Front-End Component Noise Figures

network does not, in this case, significantly degrade the receiver noise figure. The received signal may also be downconverted to an intermediate frequency within the elements in which case the power combing task is made considerably easier. Previously, low noise bipolar transistors and tunnel diode amplifiers have been used to provide preamplification within each element, (parametric amplifiers are considered too costly for this application) however, microwave low noise GaAs FET amplifiers have been developed in recent years which offer significantly lower noise figures in the 1 - 20GHz range. A comparison is given in Fig. 3.6 of the approximate variation of noise figure with frequency, of FETs, bipolar transistor, tunnel diodes, parametric amplifiers and Schottky diode mixers. It may be seen that FETs provide noise figures comparable to those of parametric amplifiers at the lower frequencies of this range.

A recent addition to microwave semiconductor devices which may call for a re-appraisal of the usual preamplifier-mixer configuration is the dual-gate microwave FET. This device may be used to provide both low noise mixing and amplification, and although still in quite an early stage of development, a noise figure of 4dB with conversion gain of 4dB has been obtained at 12GHz [19]. This device therefore has promise for future receiver front-ends.

3.5 Summary and Conclusions

Graphs summarizing the peak and CW powers obtained from the various solid state sources are shown in Figs. 3.7 and 3.8. For pulsed operation, the results of LSA mode devices are outstanding in terms of peak (but not mean) power; however, this device type is also the least well developed since reliable operation has been difficult to

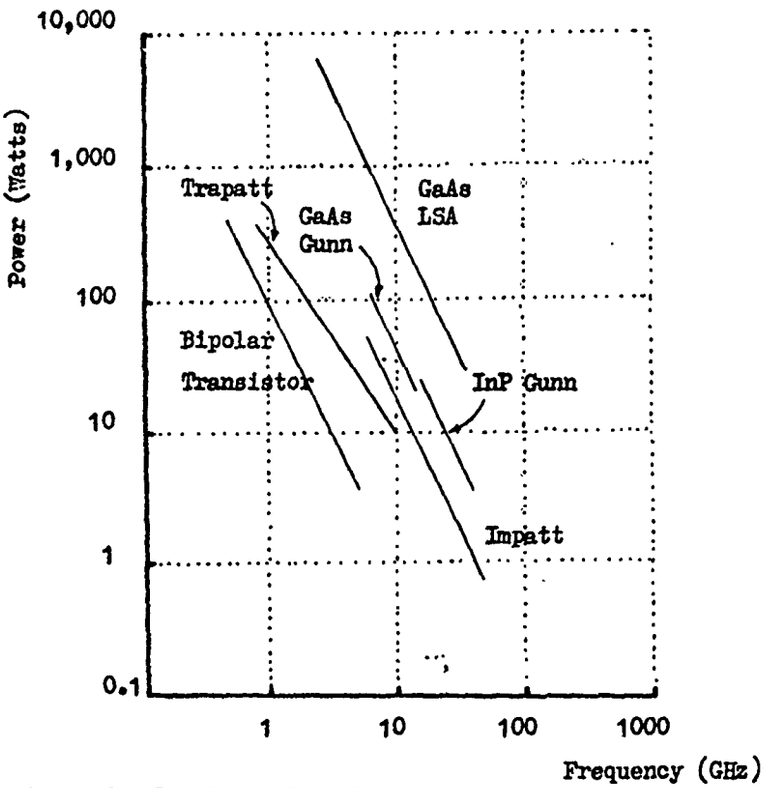


Fig. 3.7 Comparison of Solid State Peak Power Capabilities

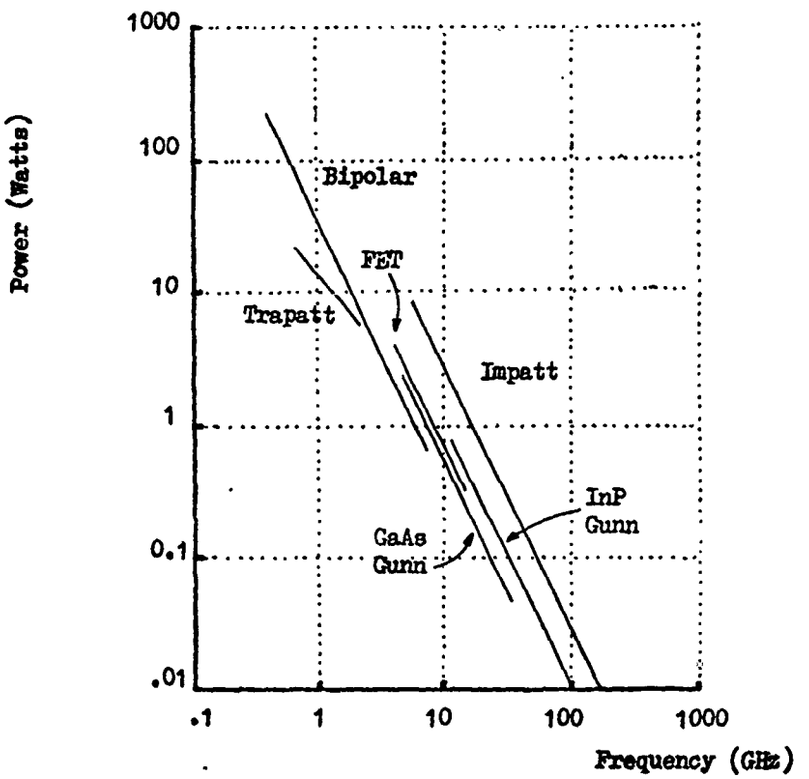


Fig. 3.8 Comparison of Solid State CW Power Capabilities

achieve.

Trapatt devices offer higher peak powers than bipolar transistors but the Trapatt has suffered in the past from a lack of clear understanding of the required matching circuit design; however, this situation is markedly improving. Above 5GHz both Impatt and Gunn devices exist, Gunn diodes typically offering higher peak power and lower voltages, whilst Impatts typically provide higher mean power and efficiency. The efficiency and mean power of Gunn devices is improving however, with the use of InP material.

Results for CW operation, shown in Fig. 3.8 show much closer grouping than the pulsed mode results, reflecting similarities between the various devices in the problems of heat dissipation. Bipolar transistors offer the highest powers in the lower end of the microwave frequency range, giving way to Impatts at frequencies about $\sim$ 5GHz. FETs at present produce CW powers at approximately the same level as Gunn devices, although it is likely that FET CW powers will increase to surpass those of Gunns and Impatts within the next few years. Above 20GHz Impatts are the main source of power; however InP Gunn devices may compete for this position in the future as InP material technology becomes established.

Fig. 3.9 shows a comparison of device efficiencies, the levels shown representing ' good ' results. Both bipolar and field effect transistors exhibit fairly high efficiencies below 10GHz. It is likely that FET efficiency will increase to the 40 - 50% range as the device design is further refined. Trapatt efficiency can extend to the 50 - 60% range but results at around the 30% level are much more commonly obtained. Around 10GHz Impatts can provide efficiencies between

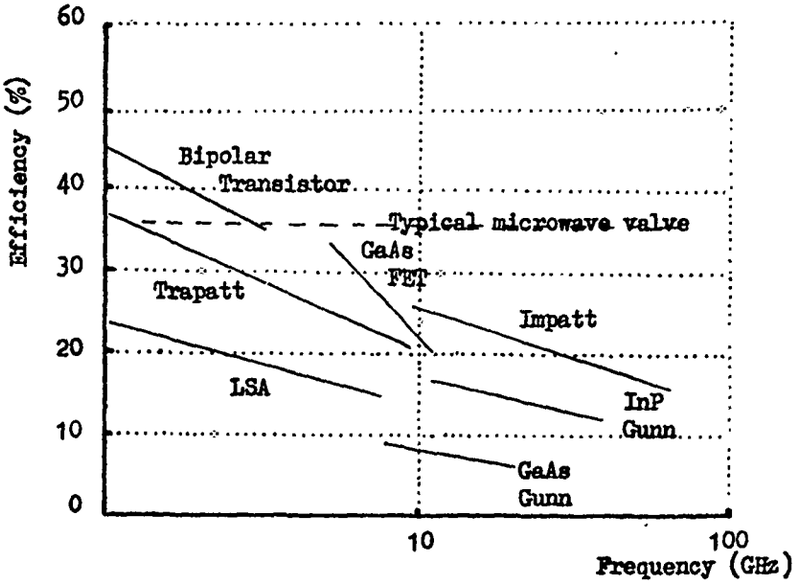


Fig. 3.9 Comparison of Solid State Efficiencies

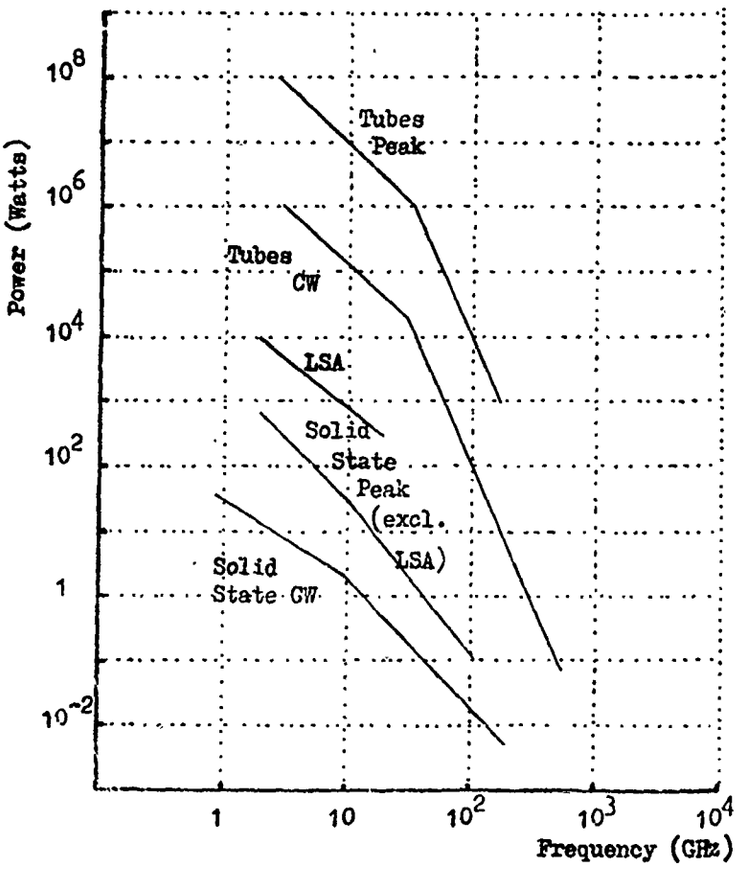


Fig. 3.10 Comparison of the Output Powers of Solid State Devices and Vacuum Tubes

10 and 30% depending on the structure and material, but over most of this range this is normally greater than that of Gunn devices, which provide the lowest efficiency.

It must be borne in mind when considering the choice of the solid state generators for use in an active array, that the probability of detecting a target in radar systems is related to the mean rather than the peak radiated power, the modulation imposed upon the transmission such as those of pulsed or FMCW modes being unimportant in this respect. The limited peak powers obtainable from solid state devices result in highest mean powers being obtained when operated CW or at high duty cycle. If mean radiated power were the only consideration, a CW transmission using bipolar transistors for frequencies below 5GHz and Impatts for frequencies above 5GHz would probably be chosen. For future systems the CW FET would appear attractive in the 5 - 15GHz range. All of these devices exhibit relatively high power, efficiency and reliability.

In practice, however, CW modulations are not favoured. Except in the case of bistatic or multistatic radar configurations [3] the use of modulated CW transmissions is restricted by direct leakage that will inevitably exist between the transmitter and the receiver. Techniques such as adaptive cancellation can be used to reduce the leakage level but the range performance obtained with CW radars is generally inferior to that obtained when conventional pulsed transmissions are used. Nevertheless, in simple radar applications where long range performance is not required, e.g. trawler or small boat radars, a CW transmission can be considered. This approach is at present receiving attention at the Philips Research Laboratories : a solid state FMCW small boat radar is being developed in which a Fast-Fourier Transform

processor is used to decode the received signals to provide range information[26].

The conventional low duty cycle, high peak power mode of operation, which is usually the cost-effective solution for use with vacuum tube transmitters is not well suited, however, to solid state device. With the exception of LSA and Trapatt devices (these unfortunately also being the least well understood), the mean power obtainable from solid state devices is significantly lower when operated with short pulses ($\lesssim 1\,\mu s$) and low duty cycle ($\sim 0.1\%$), than for operation CW or at high duty cycle. The compromise that is usually adopted for active arrays is to retain the pulsed mode of operation for which no leakage problem exists and for which receiver signal processing is relatively simple, but with the use of long pulses ranging from a few μs to many ms so that the improved solid state mean power capabilities at higher duty cycle can be used. The pulse length used is obviously restricted in practice by the minimum range requirement. The maximum pulse length τ_{max} for a desired minimum range R_{min} is given by

$$\tau_{max} = \frac{2 R_{min}}{c}$$

where c is the velocity of RF propagation.

Radar range resolution can be maintained at a desired level, despite the use of long pulses by the adoption of pulse compression techniques. Pulse compression involves the superposition of a coding on the long transmitted pulse and subsequent processing of the received echo to obtain the range resolution of a narrow pulse.

The technique can be explained in simple terms considering initially

the generation of a long pulse from a narrow one. A narrow pulse contains a large number of frequency components with a precise phase relationship between them. If these relationships are altered in a phase distorting (coding) filter a longer expanded pulse will be produced. An example of this is found in the response of a dispersive SAW delay line to a narrow input pulse; a longer pulse with inter-pulse frequency variation is produced at the output. The expanded pulse is then transmitted, and the received target echoes are applied to a filter with a complimentary response to the coding filter. The original phase relationships are here re-established and a narrow pulse is produced; it is this which then determines the range resolution, despite the length of the transmitted pulse.

Both linear FM and digital phase codes are used in practical pulse compression systems, the linear FM coding being the more common. Signal bandwidths between 1 and 10MHz are typical.

The optimum device choice for use with a pulse compression transmission is less clear than that for a CW transmission and will depend to a large extent on the range coverage required and thus on the pulse length used. For short pulse lengths (1 - 10 μs) the Trapatt and Pulsed Gunn devices offer the highest peak powers below and above 5GHz respectively. Although the reliability and understanding of the LSA device may improve in the future, it is not at present at an adequate stage of development for practical use. For longer pulse lengths than $\sim 10\mu$s, where long range performance is of more importance than short range, bipolar transistors below 5GHz, and Impatts and FETs above this frequency would probably be chosen.

It is interesting that high peak power (> 1MW) vacuum tube driven

radars also adopt the pulse compression technique, showing that cost considerations favour an increase in duty cycle rather than an increase in peak power at this level.

Fig. 3.10, from a similar plot by Nergaard[27] shows the peak and CW powers obtained from individual vacuum tubes and solid state devices. The results for pulse LSA devices are shown separately. The CW powers, approximating the best mean powers that may be achieved, show vacuum tubes to have a factor of 10^5 or more advantage in the common 1 - 10GHz radar bands. Ideally, equivalent performance could therefore be achieved from an active array of 10^5 elements each containing a single device, or from a lower number of elements if several devices are operated in parallel in each element. Although very large solid state active arrays have been built, the cost of these is prohibitively high except for a small number of specialised military applications. A more reasonable range of application for active arrays will probably be in smaller systems of up to a few hundred elements, where reliability, small size and weight, and reduced power supply requirements will be particularly important features, such as in mobile and airborne equipments. Example applications in the military field include battlefield, fire control and ship missile-defence radar. In the non-military field, aircraft weather radar, requiring typically a few KWs pulse power, could be a suitable application.

CHAPTER 4

SYNCHRONISATION OF SOLID STATE SOURCES

4.0 Introduction

The purpose of this chapter is to examine the injection locking and phase-locked loop forms of oscillator synchronisation in order to predict the behaviour of sources thus synchronised in the active array.

Previous active array element designs have in the main employed the amplifier configuration for the element solid state source, the reason for this being the predictability of amplifier behaviour and familiarity with the amplifier concept. The phase error introduced by the amplifier, an important feature for the control of sidelobes, is composed of two components: that due to the basic group delay and that introduced for signals of different frequency across the quoted bandwidth, e.g. $\pm 45^{\circ}$ at the 3dB points of a simple resonant cavity. The main disadvantage of the amplifier for active elements is the limited gain available from solid state microwave sources; typically this only 6 - 10dB. To avoid the need for a relatively high level input to each element, which for a large array could only be generated by a vacuum tube source, several stages of amplification will be required within each element, leading to high cost and complexity. The work described in this thesis has focussed on the use of synchronised oscillator element sources which have the potential of higher gain per stage and thus simpler element design.

The features of synchronised oscillators that must be considered are:

1) the magnitude of the steady state phase error between the input and output signals introduced by the locking process

2) the transient response and time required for the phase

error to settle within an acceptable margin of the steady state value

3) where long pulses are used, the response to modulations imposed on the input signal to increase the transmitted bandwidth

4) the effect of locking on the noise output of the oscillator. This is considered only briefly.

It should be noted that it is the phase error between array elements that is important for sidelobe control and phase errors introduced by the locking process that are identical between elements are not a problem. In practice the phase errors introduced will not be the same, but possible phase differences between elements can be minimised by ensuring that the maximum phase error on the output of any element is within acceptable margins. For example, if the maximum output phase error introduced under the most adverse circumstances is $\pm 10^{\circ}$, the worst case spurious phase difference between elements will be 20°. Since the phase error introduced (for instance by temperature drift of the free running frequency) is often similar for all elements, the probable phase difference between elements may be $< 5^{\circ}$. Typical requirements for a locked source could be a maximum phase error of $\pm 10^{\circ}$ and a minimum time to acquire lock of 100ns for a 1 μs pulse length.

For both injection locking and the phase-locked loop method of locking both steady state and transient behaviour of locked sources are examined. The important aspect of phase-locked loop stability and its effect on performance is examined and the heterodyne loop, used heavily in subsequent element designs, is presented. Since the characteristics of injection locked microwave sources are fairly well established a relatively simple model is adopted for this. More

attention is given to the description of the phase-locked loop.

4.1 Injection Locking

The injection locking technique for synchronising non-linear oscillators has previously received much attention and detailed models have been developed for predicting performance[28]. In previous work at University College London, Al-Ani[29] and Darbandi[30] in particular have considered the application of injection locking to active arrays, via the harmonic locking and the interpolation locking techniques. In light of the previous detailed work, only a relatively simple model for injection locking is adopted here, but this nevertheless serves well to indicate the nature of the performance that may be obtained with injection locked sources.

Neglecting voltage dependent susceptance and frequency dependent effects, the behaviour of a circulator coupled injection locked oscillator is described by[28]

$$\frac{d\varphi_e}{dt} = \Delta\omega - \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}}\sin\varphi_e \qquad \ldots\ldots\ldots\ 4.1$$

where φ_e, the phase error, is the phase of the oscillator output measured with respect to the locking signal

ω_0 is the oscillator free running angular frequency

$\Delta\omega = \omega_1 - \omega_0$, is the difference between the locking signal angular frequency ω_1, and the free running angular frequency ω_0

Q is the oscillator locking Q factor ($\approx$ loaded Q)

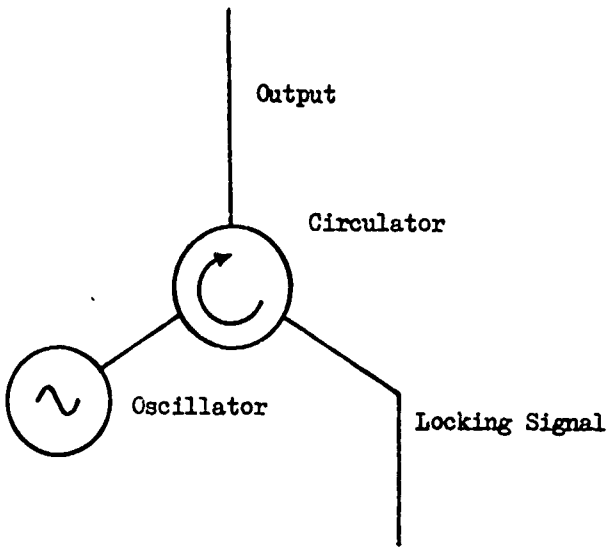


Fig. 4.1 A Circulator Coupled Injection Locked Oscillator

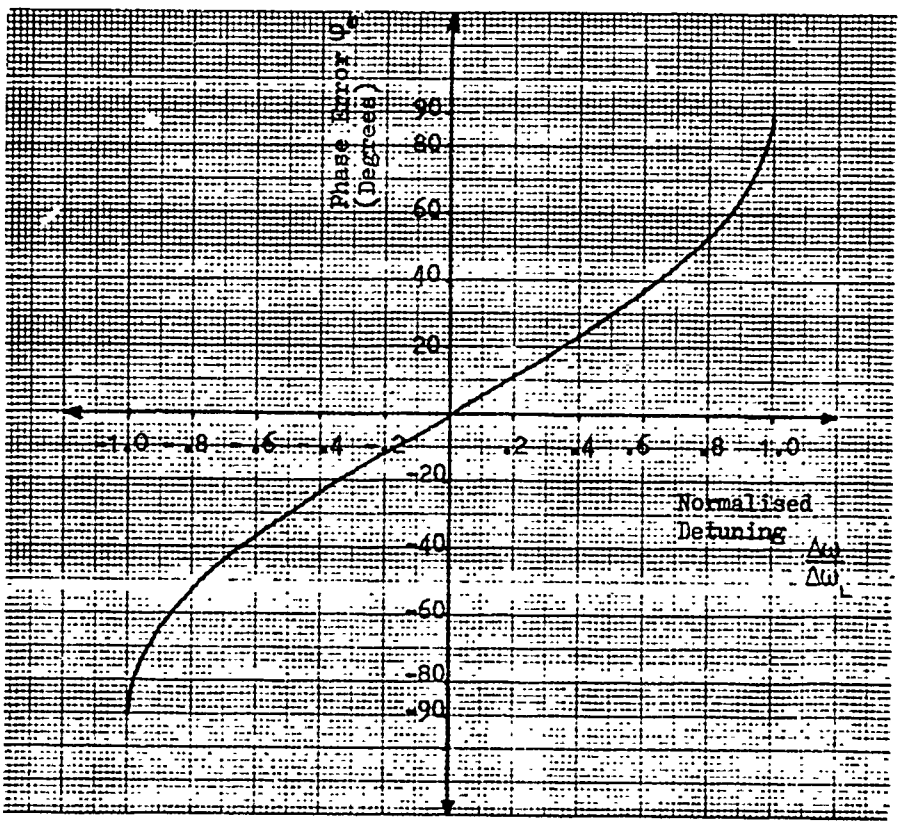


Fig. 4.2 Variation of Phase Error with Detuning

P_1 is the injected signal power

P_2 is the measured output power

This expression is valid when the assumption can be made that the oscillator output voltage is not significantly changed by the presence of the locking signal i.e. $P_2 \gg P_1$. In practice this condition is satisfied for locking gains of 10dB or more, and since this is the range for which injection locking can offer higher gain than that of a typical single stage amplifier (typically $\sim$ 6dB gain) its use here is justified.

The steady state response when lock has been achieved is given by Eqn. 4.1 with

$$\frac{d\varphi_e}{dt} = 0$$

thus

$$\Delta\omega = \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}}\sin\varphi_e \qquad \ldots\ldots\ldots 4.2$$

A restriction on the detuning $\Delta\omega$ is apparent since

$$-1 \leqslant \sin\varphi_e \leqslant +1$$

and hence a locking range $\Delta\omega_L$ can be defined such that

$$\Delta\omega_L = \left|(\Delta\omega)_{max}\right|$$

$$= \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}} \qquad \ldots\ldots\ldots 4.3$$

It may be noted that this quantity can take only +ve values and represents half the frequency range over which lock can occur.

The synchronisation range $\Delta\omega_s$, being the range of frequency for which the oscillator can be synchronised to the locking signal is given by

$$\Delta\omega_s = 2\,\Delta\omega_L = \frac{2\omega_0}{Q}\sqrt{\frac{P_1}{P_2}} \qquad \ldots\ldots\ldots 4.4$$

It may be noted immediately that this is inversely related to Q and locking gain.

The variation in phase error with detuning is obtained from Eqn. 4.2.

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega . Q}{\omega_0}\sqrt{\frac{P_2}{P_1}}\right) \qquad \ldots\ldots\ldots 4.5$$

$$= \sin^{-1}\left(\frac{\Delta\omega}{\Delta\omega_L}\right) \qquad \ldots\ldots\ldots 4.6$$

and the form of this relationship is shown in Fig. 4.2. To obtain low values of steady state phase error in the presence of drift of the free running frequency due to temperature, aging etc., it is clear that high values of locking range should be used.

Transient Performance

The transient response of an injection locked oscillator is obtained from integration of Eqn. 4.1. This has previously been carried out by White and Jones [31] and their result is simply quoted below. (Solution of a similar equation derived from the phase locked loop is given in more detail in section 4.2.3.)

White and Jones's solution is

$$\varphi_e(t) = 2 \tan^{-1}\left(A_1 + \frac{A_1^2 - 1}{A_1\left[\pm \exp(B\,[t-t_0]) - 1\right]}\right) \qquad \ldots\ldots 4.7$$

where $A_1 = \tan\left[\frac{\varphi_e}{2}\right]$

$B = \sqrt{(\Delta\omega_L)^2 - (\Delta\omega)^2}$

t_0 = a constant related to the initial conditions at the start of the transient.

To find, in addition, the frequency transient of the oscillator output let the oscillator output voltage v_2 be expressed in terms of the free running frequency ω_0

$$v_2 = V_2 \sin(\omega_0 t + \varphi_2(t)) \qquad \ldots\ldots\ldots 4.8$$

It is convenient to also express the locking signal voltage v_1 in terms of the oscillator free running frequency :

$$v_1 = V_1 \sin(\omega_0 t + \varphi_1(t)) \qquad \ldots\ldots\ldots 4.9$$

The instantaneous phase error between the input and output is therefore

$$\varphi_e(t) = \varphi_1(t) - \varphi_2(t) \qquad \ldots\ldots\ldots 4.10$$

Hence

$$\frac{d\varphi_e}{dt} = \frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt} \qquad \ldots\ldots\ldots 4.11$$

Substituting in Eqn. 4.1

$$\frac{d\varphi_2}{dt} + \Delta\omega = \frac{d\varphi_1}{dt} + \Delta\omega_L \sin\varphi_e \qquad \ldots\ldots\ldots 4.12$$

Let the instantaneous oscillator output frequency be ω_2 thus

$$\omega_2 = \omega_0 + \frac{d\varphi_2}{dt} \qquad \ldots\ldots\ldots 4.13$$

Similarly let the instantaneous input frequency be ω_1

$$\omega_1 = \omega_0 + \frac{d\varphi_1}{dt} \qquad \ldots\ldots\ldots 4.14$$

Substituting in Eqn. 4.12 gives

$$\omega_2 - \omega_1 + \Delta\omega = \sin\varphi_e \qquad \ldots\ldots\ldots 4.15$$

and since

$$\Delta\omega = \omega_1 - \omega_0 \qquad \ldots\ldots\ldots 4.16$$

we obtain

$$\frac{\omega_2(t) - \omega_0}{\Delta\omega_L} = \sin\varphi_e \qquad \ldots\ldots\ldots 4.17$$

To evaluate Eqn. 4.6 and 4.17 a value of t_0 would normally be chosen to give φ_e equal to the initial value for any particular transient. The form of these expressions can best be illustrated however, by

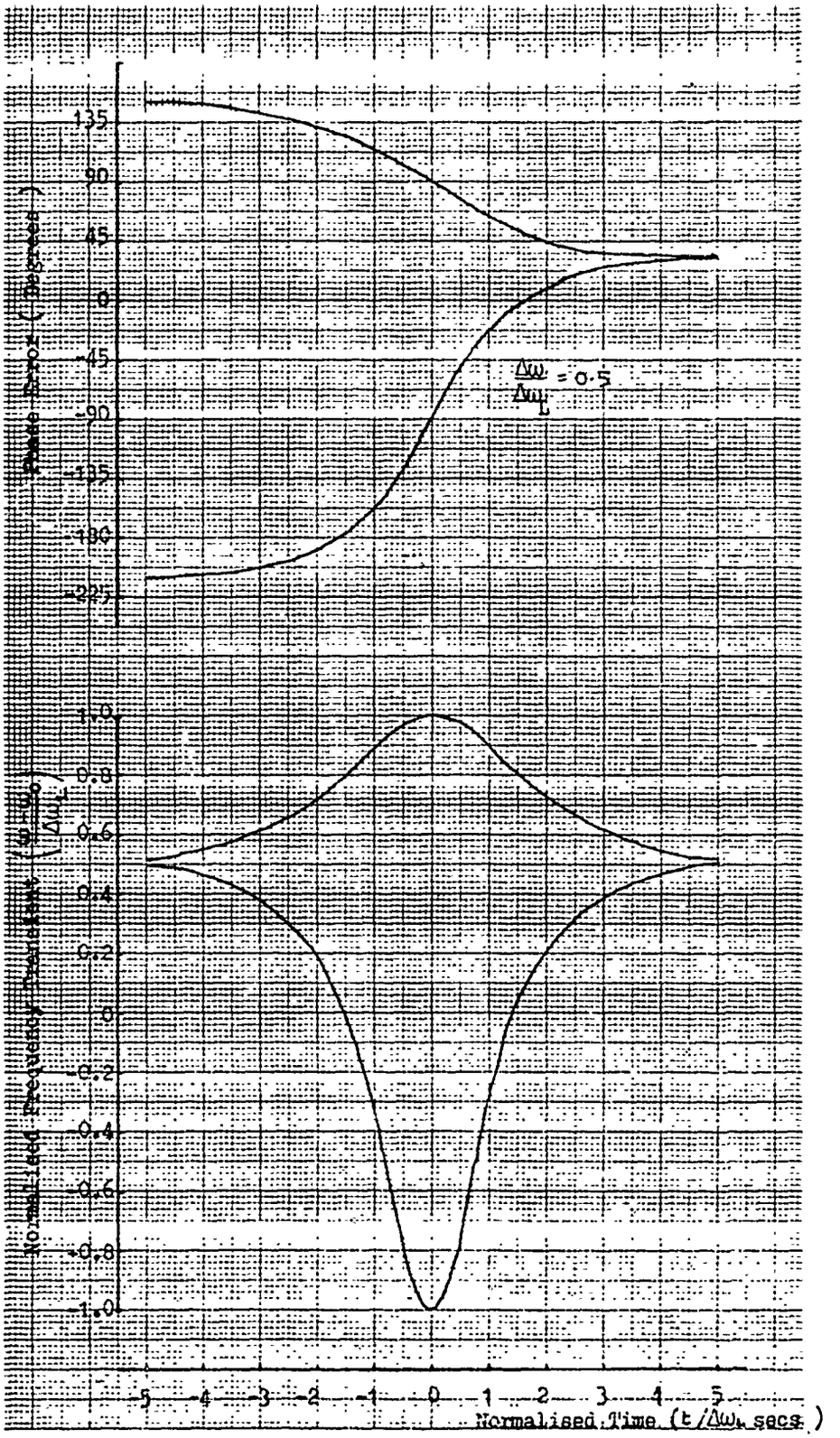


Fig. 4.3 Transient Response of an Injection Locked Oscillator with $\Delta\omega/\Delta\omega_L = 0.5$

taking a value of t_0 giving symmetrical plots against time as shown in Fig. 4.3. This choice of t_0 does not affect the shape of the curves but only the relative position on the time axis. Fig. 4.3 shows the phase and frequency transients for the case $\Delta\omega/\Delta\omega_L = 0.5$. The transient for a given initial value of phase error may be obtained by entering the curve at this value of φ_e and following the transient for increasing time. It may be seen that apart from initial values of phase error very close to the unstable equilibrium position, most transients are essentially over in a time $t = 10/\Delta\omega_L$ secs. (This approximation is examined in more detail for the similar transient of the first order phase-locked loop in section 4.2.3). A more exact transient analysis of injection locking including voltage dependent susceptance is given by Takayama[32] but the form of response is not significantly different.

Acquisition Behaviour of Pulsed Injection Locked Sources

It might be expected that the behaviour of pulsed sources during acquisition would be described by Eqn. 4.6 with essentially random initial values of phase error. In this case, the acquisition time, being the time required to ensure the phase error is within a few degrees of the final value for most initial conditions would be given by $10/\Delta\omega_L$. This is indeed found to be correct for cases in which the locking signal is also pulsed and applied to the oscillator slightly after the oscillator is switched on. However, for the more usual case in which the locking signal is either continuous or applied before energisation of the oscillator, it is found that the acquisition time is much less than this value. This is explained by considering the build up of oscillation when the oscillator is switched on.

When the energising bias pulse is applied, oscillation within the resonant cavity is normally initiated by noise, leading to random pulse-to-pulse initial phase. When a locking signal is present, however, this will itself initiate oscillation and furthermore, during the initial part of the exponential build up of oscillation the locking gain P_2/P_1 will be very low, leading to large locking range and thus rapid synchronisation. The acquisition time for this case has not been measured but is estimated to be less than one tenth of that for random initial conditions.

Practical pulse microwave sources exhibit a change of free running frequency during the pulse (chirp) due to heating effects. It would not be expected that this would have any significant effect upon the acquisition transient since the change in frequency is typically small during the period of acquisition. The effect on the phase error after acquisition may be obtained by considering the equivalent frequency variation applied to the input signal. For small phase error (which would in practice be required from a locked active array source)

$$\sin \varphi_e \approx \varphi_e$$

and Eqn. 4.1 simplifies to

$$\frac{d\varphi_e}{dt} = \Delta\omega - \Delta\omega_L \cdot \varphi_e \qquad \text{.....4.18}$$

Interpreting the detuning $\Delta\omega$ as a frequency shift from ω_0 on the locking signal we have

$$\Delta\omega = \frac{d\varphi_1}{dt}$$

Thus

$$\frac{d\varphi_e}{dt} = \frac{d\varphi_1}{dt} - \Delta\omega_L.\varphi_e \qquad \text{.....4.19}$$

Transforming into the frequency domain, using operational notation

$$s\,\Phi_e(s) = s\,\Phi_1(s) - \Delta\omega_L.\Phi_e(s) \qquad \text{.....4.20}$$

where $\Phi_e(s)$ and $\Phi_1(s)$ are the Laplace transforms of $\varphi_e(t)$ and $\varphi_1(t)$ respectively.

Hence

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s}{s + \Delta\omega_L} \qquad \text{.....4.21}$$

Representing linear pulsed oscillator chirp by a linear variation of the input frequency of P rad/s^2 we can write

$$\Phi_1(s) = \frac{P}{s^3} \qquad \text{.....4.22}$$

assuming zero phase error initially.

Thus

$$\Phi_e(s) = \frac{P}{s^2(s + \Delta\omega_L)} \qquad \text{.....4.23}$$

giving

$$\varphi_e(t) = \frac{Pt}{\Delta\omega_L} - \frac{P}{(\Delta\omega_L)^2}\,(1 - \exp(-\Delta\omega_L.t)) \qquad \text{.....4.24}$$

After the initial transient the response to a linear frequency change therefore contains a constant tracking error $P/(\Delta\omega_L)^2$ and a term linearly increasing with time corresponding to the detuning existing at time t. With increasing time this term can cause operation outside the linear region, for which a phase error of the form sin $(Pt/\Delta\omega_L)$ would be expected, and eventually cause loss of lock. Taking for illustration typical values used experimentally,

$$\Delta\omega_L = 1.98 \times 10^8 \text{ rad/s for a 10GHz oscillator}$$

with $Q_1 = 100$

$$\frac{P_2}{P_1} = 10$$

$$P = 3.14 \times 10^{13} \text{ rad/s}^2 \ (5\text{MHz}/\mu\text{s})$$

The constant term is seen to be small :

$$\frac{P}{(\Delta\omega_L)^2} = 0.8 \times 10^{-4} \text{ rad}$$

The linearly increasing term produces a phase error

$$\frac{Pt}{\Delta\omega_L} = 0.16 \text{ rad}/\mu\text{s}$$

It may be seen that this is the more serious source of error for the rates of change of frequency typically encountered.

Response to Pulse Compression Modulations

Since many solid state sources are limited in peak power, it is com-

mon to use relatively long transmitted pulses to increase the average radiated power, in combination with modulated transmissions and pulse compression to maintain adequate range resolution. Pulse compression modulations applied to the transmitted signal usually take the form of coded phase-shift keying (PSK) or linear frequency modulation[9] ; transmitted bandwidths between 1 and 10MHz are typical.

The response of injection locked oscillators to phase shift keyed locking signals has been examined by Mackey[33] . He concluded, that when the period of the modulation is long compared with the locked oscillator response time, the output would essentially follow the input modulation; when the period of modulation is of the order of the locked oscillator response time the oscillator would be unable to reproduce the modulation. This result is fairly obvious in consideration of the previous transient analysis since the locked oscillator will require a finite time to re-establish lock after each input phase discontinuity. An approximate maximum PSK period of $10/\Delta\omega_L$ is therefore predicted although in practice lower rates would have to be used in order to avoid distortion of the modulation spectrum.

The response to linear variation of the locking signal was established in Eqn. 4.24. Since the rate of frequency change P will usually be small (e.g. 2MHz/ μs) in comparison with $(\Delta\omega_L)^2$, the constant tracking phase error may be ignored. A limitation on transmitted bandwidth will be imposed by the maximum acceptable variation in phase error during the pulse, φ_{e1} . Within the linear range this will be

$$\varphi_{e1} = \frac{P\tau}{\Delta\omega_L} \text{ rad} \qquad \text{.....4.25}$$

where τ is the pulse length. If a maximum phase error variation of 10° is specified the maximum angular frequency change $P\tau$ for the example previously considered with $\Delta\omega_L = 1.98 \times 10^8$ rad/s is 3.45×10^7 rad/s.

Noise Response

Solid state microwave oscillators such as Impatt and Gunn sources are generally noisy, and the usual situation encountered is that of a ' quiet ' locking signal synchronising a ' noisy ' source. The effect of injection locking on the oscillator noise output has been considered by several authors[34,35]. It is found that AM noise accompanying the desired oscillator output is unaffected by locking, but FM noise (which is usually greater) is significantly suppressed close to the carrier. The FM noise suppression is described by the equation[36]

$$\Delta f_{rms} = \sqrt{\frac{(\Delta f_r)^2 + (\Delta f_0)^2 \left(\frac{2\pi f_m}{\Delta\omega_L}\right)^2}{1 + \left(\frac{2\pi f_m}{\Delta\omega_L}\right)^2}} \qquad \ldots 4.26$$

where Δf_{rms} is the noise deviation of the injection locked oscillator

Δf_0 is the noise deviation of the unlocked (free-running) oscillator

Δf_r is the noise deviation of a low noise locking signal

f_m is the modulation frequency.

Basically this states that close to the carrier the FM noise deviation of the locked oscillator is that of the reference signal, whilst further from the carrier it reverts to that of the free running oscillator. The FM noise deviation has increased to $\sqrt{2}$ times Δf_r at a modulation frequency f_m' given by

$$f_m' \approx \frac{\Delta f_r}{\Delta f_0} \times \frac{\Delta \omega_L}{2\pi} \qquad \ldots\ldots\ldots 4.27$$

and thus to provide suppression of the FM noise over a wide bandwidth a large value of $\Delta\omega_L$ should again be used.

Summary

The phase error introduced by injection locking due to detuning caused by temperature induced frequency drift, aging, chirp or linear FM is given by Eqn. 4.6 :

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{\Delta\omega_L}\right)$$

and to minimise possible phase error a large value of locking range is therefore desirable. This is also required to minimise the loop transient response time, approximated to $10/\Delta\omega_L$, although it was noted that the acquisition time for pulsed sources in which the locking signal is initially present is much less than this.

The locking range is given by

$$\Delta\omega_L = \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}}$$

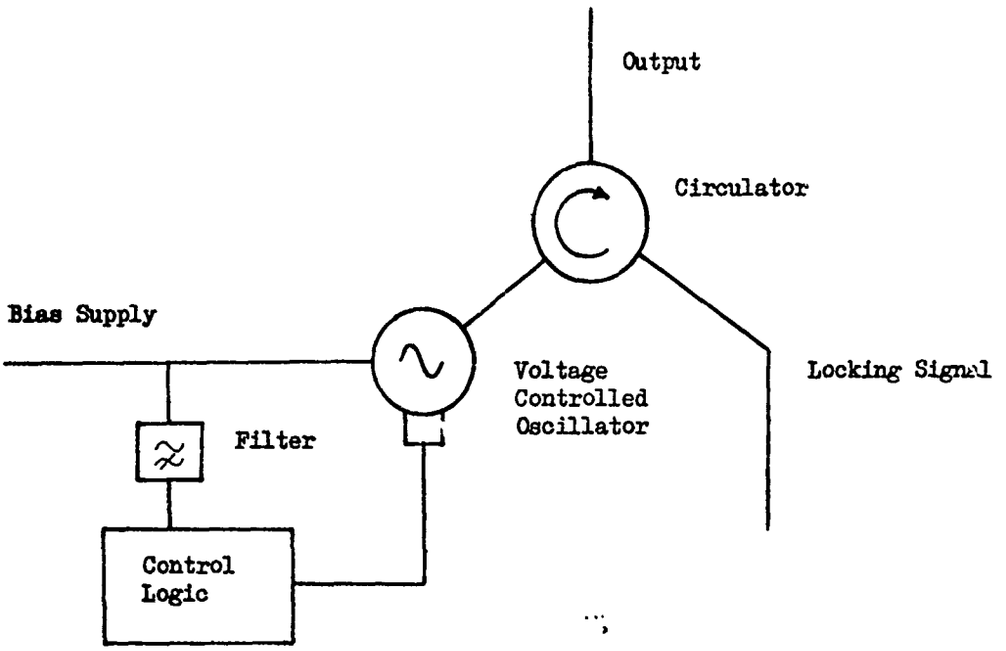


Fig. 4.4 Circuit to Reduce Insertion Phase Due to Ulbricht and Marx

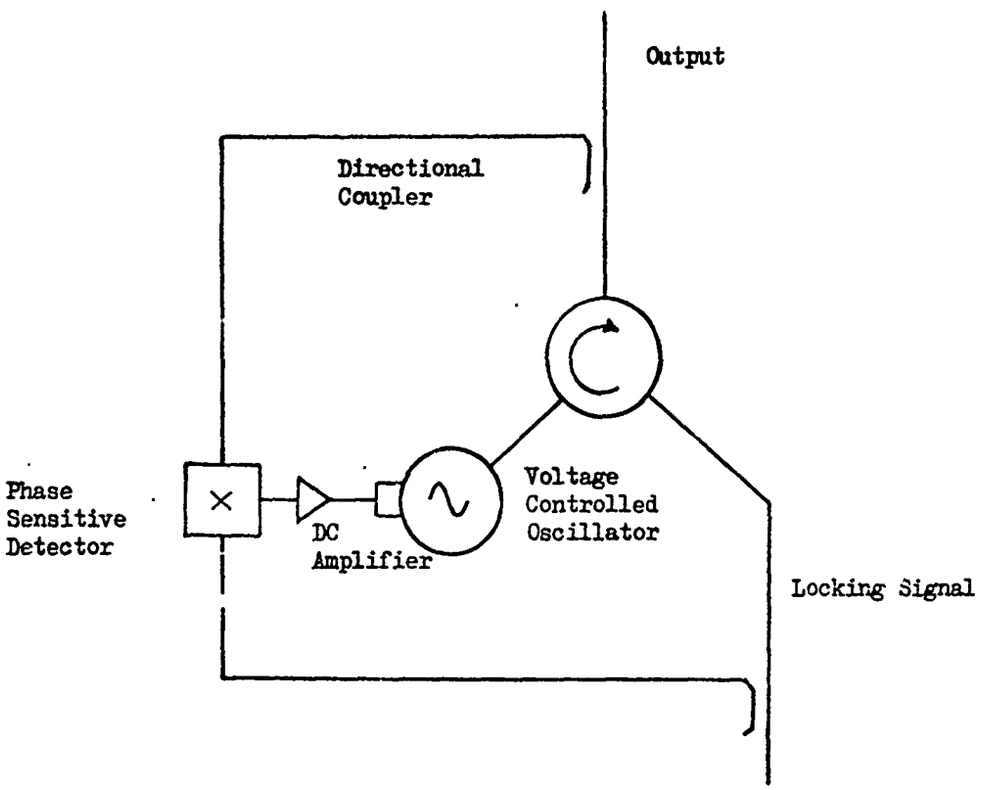


Fig. 4.5 Circuit to Reduce Insertion Phase Due to Mackey

and for a given free running frequency can be increased only by reducing either the Q or the locking gain. A reduction in Q will not, however, necessarily improve phase error due to temperature drift, chirp etc. since the detuning produced by these effects is inversely related to Q. This then leaves the locking gain as the principal source of control over the locking range and thus in general high values of locking gain cannot be used for straightforward injection locking. Typical gains are limited to $\sim$ 10dB.

Recognising this limitation, two techniques have been put forward, which, with the penalty of some added complexity, allow higher gain to be achieved whilst maintaining low phase error. Both involve the addition of voltage controlled tuning to the locked oscillator with which the detuning between the input frequency and the oscillator free running frequency is minimised.

Ulbricht and Marx [37] have suggested an essentially open loop technique for reducing detuning, using no additional microwave components, as shown in Fig. 4.4. At regular intervals the logic control circuitry varies the free running frequency of the injection locked voltage controlled oscillator (VCO) until the extremities of the locking range are found. These are sensed by the presence on the oscillator bias supply line of the downconverted beat frequency when the oscillator is unlocked. The varactor voltage is subsequently reset to the mid value between the unlock positions, therefore ensuring small long term detuning. The technique suffers mainly from the fact that it is essentially restricted to CW operation.

A closed loop technique has been suggested by Mackey [33] as shown in Fig. 4.5. A comparison is here made of the input and output phase

of the locked oscillator. In the event of a phase error being present, a feedback signal is generated which changes the free running frequency such that the detuning and phase error are reduced to low level. When a wideband feedback path is employed this system can reduce phase error due to pulsed oscillator chirp in addition to that due to ambient temperature frequency drift.

4.2 The Phase-Locked Loop

The phase-locked loop represents the alternative to injection locking for oscillator synchronisation, assuming an electronically tunable source. Since many aspects govern the choice of the optimum loop design the description given in this section has been broken down under separate headings to consider some of these independently. Initially the established general description of the phase-locked loop is given ; subsequently the relevant behaviour of both first and second order loops is examined. In section 4.2.6 the constraints imposed by loop instability are examined and the restriction on first and second order loop behaviour is summarized in 4.2.8. In 4.2.9 the heterodyne form of phase-locked loop, much used in Chapter 7, is described. Experimental results with phase-locked loops containing pulsed sources are presented in 4.2.11 and conclusions regarding the relative merits of injection locking, the first and second order phase-locked loops are drawn in section 4.3.

Only sinusoidal phase-sensitive detectors, represented in practice by passive mixers, have been considered in the analysis.

4.2.1 Phase Locked Loop Fundamentals

A representation of a microwave phase-locked loop (PLL) is shown in Fig. 4.6. A sample of the voltage controlled oscillator (VCO) output is compared with a reference locking signal in a phase sensitive detector (PSD) ; the resulting error signal is fed back via an amplifier and filter to the control terminal of the VCO to complete the loop. The phase sensitive detector, which produces a voltage which is a function of the difference in phase between the inputs is simply realised in practice using the difference frequency output of a balanced mixer. Practical mixers also produce a sum frequency term however and a low pass filter will, in general, be required at the mixer output to suppress this component. However, since the sum frequency is usually very much higher than the difference frequency, it is normally assumed that any filtering required to remove this component may be neglected in the analysis.

Ideal synchronism with no phase error is achieved when the steady state error voltage is zero, which for the case of a mixer PSD requires a static phase difference between the inputs of 90°. This factor may conveniently be included in the analysis by defining the input waveform to the PSD in terms of sine and cosine waves, as shown in Fig. 4.6.

The following definitions are used :

K_1 is the PSD gain (volts/radian) in the linear (small phase error) region for input signals

$$v_1(t) = V_1 \sin (\omega_0 t + \varphi_1(t))$$

and $$v_2(t) = V_2 \cos (\omega_0 t + \varphi_2(t))$$

K_2 is the VCO tuning sensitivity (rads/v.s) which is assumed to be linear.

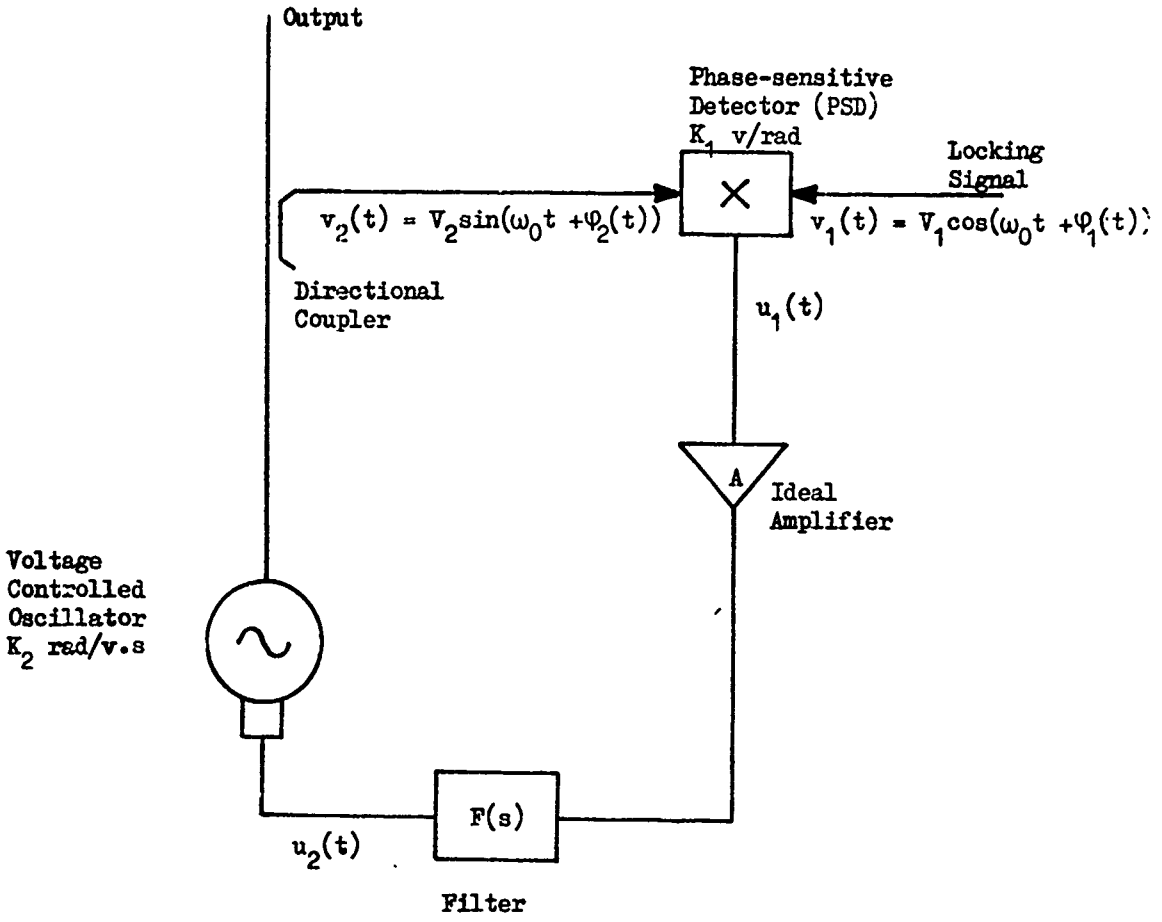


Fig. 4.6 The Basic Phase-Locked Loop

ω_0 is the free running frequency of the VCO.

A is the voltage gain of an ideal amplifier.

F(s) is the transfer function of the filter (this may include the frequency response of a practical amplifier).

$u_1(t)$ is the PSD output voltage (volts).

$u_2(t)$ is the voltage applied to the VCO control terminal (volts).

With reference to Fig. 4.6, the VCO output voltage applied to the PSD may be expressed

$$v_2(t) = V_2 \cos(\omega_0 t + \varphi_2(t)) \qquad \ldots\ldots\ldots 4.28$$

where ω_0 is the free running frequency of the oscillator, and $\varphi_2(t)$ represents the VCO output phase variation with time. Assuming a Linear VCO tuning characteristic of sensitivity K_2 rad/v.s, the deviation of the VCO frequency from the free running value is

$$\frac{d\varphi_2(t)}{dt} = K_2 u_2(t) \qquad \ldots\ldots\ldots 4.29$$

where $u_2(t)$ is the voltage applied to the frequency control terminal.

It is convenient to also express the input locking signal voltage in terms of the VCO free running frequency, thus

$$v_1(t) = V_1 \sin(\omega_0 t + \varphi_1(t)) \qquad \ldots\ldots\ldots 4.30$$

where $\varphi_1(t)$ represents the possible input phase variation with time.

The output of the sinusoidal phase sensitive detector is then

$$u_1(t) = K_1 \sin\left(\varphi_1(t) - \varphi_2(t)\right) \qquad \ldots\ldots\ldots 4.31$$

where K_1 is the PSD gain in v/rad for the given input voltages V_0 and V_1. The sign of K_1 for any particular mixer PSD with a given phase relationship between the inputs is dependent on the sense of diode connection. The characteristics of mixer PSDs are considered in section 4.2.11 but it may be noted here that when operated in the saturated region, K_1 is essentially independent of the input signal voltages.

After the ideal amplifier and the filter (in which can be included the frequency response of practical amplifiers) we have

$$u_2(t) = A\, u_1(t) * f(t)$$

where $f(t)$ is the impulse response of the filter and * denotes convolution. Substituting for $u_1(t)$ from 4.31 we obtain

$$u_2(t) = AK_1\left\{\sin\left(\varphi_1(t) - \varphi_2(t)\right) * f(t)\right\} \qquad \ldots\ldots\ldots 4.32$$

and from Eqn. 4.29

$$\frac{d\varphi_2(t)}{dt} = AK_1K_2\left\{\sin\left(\varphi_1(t) - \varphi_2(t)\right) * f(t)\right\} \qquad \ldots\ldots\ldots 4.33$$

which is the generalised time domain equation of the loop.

Replacing AK_1K_2 by K , and the phase error $(\varphi_1 - \varphi_2)$ by φ_e ,

Eqn, 4.33 becomes

$$\frac{d\varphi_2(t)}{dt} = K \sin(\varphi_e(t)) * f(t) \qquad \text{.....4.34}$$

It may be noted that K has the dimensions of frequency. The magnitude of K represents the DC gain around the loop when a passive filter with unity DC gain is used.

Analysis of PLL behaviour is considerably simplified when the phase error is such that

$$\sin \varphi_e \approx \varphi_e$$

in which case Eqn. 4.34 becomes

$$\frac{d\varphi_2(t)}{dt} = K(\varphi_e(t) * f(t)) \qquad \text{.....4.35}$$

which is the linearised equation of the PLL.
Transformation of Eqn. 4.35 into the frequency domain, using operational notation gives

$$s\Phi_2(s) = K(\Phi_e(s).F(s)) \qquad \text{.....4.36}$$

where $\Phi_2(s)$ and $\Phi_e(s)$ are the transforms of $\varphi_2(t)$ and $\varphi_e(t)$ respectively and F(s) is the filter transfer function.
Eqn. 4.36 may be rewritten :

$$s\Phi_2(s) = K(\Phi_1(s) - \Phi_2(s)).F(s) \qquad \text{.....4.37}$$

from which the loop transfer function H(s) may be obtained

$$H(s) = \frac{\Phi_2(s)}{\Phi_1(s)} = \frac{KF(s)}{s + KF(s)} \qquad \text{.....4.38}$$

Similarly the error function 1 - H(s) is given by

$$1 - H(s) = \frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s}{s + KF(s)} \qquad \text{.....4.39}$$

It should be noted that Eqns. 4.38 and 4.39 are valid only for the limited range of φ_e for which the linearising approximation $\sin \varphi_e \approx \varphi_e$ may be made. Also due to the definition of the PSD inputs in terms of sine and cosine, a zero value of φ_e in fact represents a phase difference of $\frac{\pi}{2}$ rads between the VCO output and the locking signal.

4.2.2 Phase-Locked Loop Classification

Following the usual convention for servo control loops and depending upon the form of the filter transfer function F(s), phase locked loops are classified according to their ' order ' and ' type ' since these terms conveniently indicate the form of the transient and steady state response of the loop respectively[38] .

The order of a loop is given by the highest power of s in the denominator of the loop transfer function H(s) given in Eqn. 4.38. A first order loop, for example, will be obtained if F(s) = 1, and from a knowledge of servo control loops of this order a transient response consisting of simple exponential terms may be expected. A second order loop will be obtained from filter types

$$F(s) = \frac{1}{1 + s\tau_1} \quad , \quad \frac{1 + s\tau_2}{1 + s\tau_1} \quad \text{and} \quad \frac{1 + s\tau_2}{s\tau_1}$$

for which a transient described additionally in terms of a natural resonant frequency and damping factor may be expected.

The type of a loop is given by the number of poles in the open loop transfer function G(s) where

$$G(s) = \frac{AK_1K_2F(s)}{s}$$

and indicates for which input conditions a zero steady state phase error would be expected. A type one loop gives a zero steady state phase error for a phase step input ; a type two loop gives additionally a zero steady state error for a frequency step input ; a type three loop gives additionally a zero steady state error for a frequency ramp input. It may be noted that all PLLs are of at least type one since the VCO itself acts as an integrator, relating the output phase to the integral of the control voltage.

4.2.3 The First Order Loop

Although the first order loop will subsequently be shown to be less attractive than the second order for the synchronisation of practical sources a detailed description of its behaviour is given here since it is indicative of second order loop behaviour for which analysis is less straight-forward. Furthermore a direct comparison can be made between the behaviour of a first order loop and that of injection locking, since the two cases are described by similar equations.

A first order loop (which is necessarily of type one) is formed when there is no filter in the loop, i.e. when $F(s) = 1$, and the PSD output after amplification is applied directly to the voltage control terminal of the VCO.

For this case

$$u_2 = Au_1 = AK \sin \varphi_e \qquad \ldots\ldots\ldots 4.40$$

and Eqn. 4.34 becomes

$$\frac{d\varphi_2}{dt} = K \sin\varphi_e(t) \qquad \ldots\ldots\ldots 4.41$$

Since $\varphi_2 = \varphi_1 - \varphi_e$ Eqn. 4.41 may be written

$$\frac{d\varphi_e}{dt} = \frac{d\varphi_1(t)}{dt} - K \sin\varphi_e(t) \qquad \ldots\ldots\ldots 4.42$$

A C.W. locking signal of frequency $\omega_1 = \omega_0 + \Delta\omega$ is obtained when

$$\varphi_1(t) = \Delta\omega.t + \theta_1 \qquad \ldots\ldots\ldots 4.43$$

where θ_1 is the locking signal phase.

Differentiating Eqn. 4,43 gives

$$\frac{d\varphi_1(t)}{dt} = \Delta\omega \qquad \ldots\ldots\ldots 4.44$$

and substituting this in Eqn. 4.42 we obtain

$$\frac{d\varphi_e(t)}{dt} = \Delta\omega - K \sin\varphi_e(t) \qquad \ldots\ldots\ldots 4.45$$

In the steady state, assuming the VCO is locked to the synchronising signal, $\frac{d\varphi_e}{dt} = 0$ and Eqn. 4.45 becomes

$$\Delta\omega = K \sin\varphi_e \qquad \ldots\ldots.4.46$$

A locking range $\Delta\omega_L$ may be defined as the magnitude of the maximum detuning of the VCO for which the loop will remain locked, and is obtained by noting that

$$\left|\sin\varphi_e\right| \leqslant 1$$

Thus

$$\Delta\omega_L = K = AK_1K_2$$

A synchronization range $\Delta\omega_s$ being the range of frequency over which the VCO can be synchronized to the locking signal, is also defined such that

$$\Delta\omega_s = 2\Delta\omega_L = 2K \qquad \ldots\ldots.4.47$$

It may be noted that Eqn. 4.45 is of similar form to Eqn. 4.1 for injection locking. The behaviour of a first order loop and an injection locked oscillator are in fact very similar, but an important advantage of the PLL is that the locking range is not directly related to the input or output power (assuming a PSD operating under saturated conditions) and may be independently controlled via the amplifier gain A ; by implication the locking range and locking gain (output power/locking power) of the PLL may be independently specified.

From Eqn. 4.46 the steady state phase error introduced by the loop (neglecting the $\frac{\pi}{2}$ radian due to the use of a mixer PSD) is given

by

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{AK_1K_2}\right) \qquad \text{.....4.48}$$

the form of which is the same as that of Fig. 4.2 for injection locking.

Transient Behaviour

The transient response of a first order loop, indicating the behaviour during capture of the VCO by the locking signal or after a sudden phase shift applied to the locking signal, can be obtained from Eqn. 4.45

$$\frac{d\varphi_e}{dt} = \Delta\omega - K \sin\varphi_e(t)$$

Thus

$$\int dt = \int \frac{1}{\Delta\omega - K \sin\varphi_e}\, d\varphi_e \qquad \text{.....4.49}$$

which yields upon integration

$$t-t_0 = \frac{2}{\sqrt{(\Delta\omega)^2 - K^2}} \tan^{-1}\left[\frac{\Delta\omega.\tan(\varphi_e/2) - K}{\sqrt{(\Delta\omega)^2 - K^2}}\right] \qquad \text{.....4.50}$$

when $(\Delta\omega)^2 > K^2$ where t_0 is an integration constant.

This case, representing an injected signal outside the locking range gives

$$\varphi_e(t) = 2\tan^{-1}\left[\frac{\sqrt{(\Delta\omega)^2 - K^2}\,\tan\left[\frac{(t-t_0)\sqrt{(\Delta\omega)^2 - K^2}}{2}\right] + K}{\Delta\omega}\right] \qquad \text{...4.51}$$

As t varies, $\varphi_e(t)$ will vary periodically with period

$$T = \frac{2\pi}{\sqrt{(\Delta\omega)^2 - K^2}} \qquad \ldots\ldots 4.52$$

and thus there will be no steady state solution. Eqn. 4.36 then describes the beat phenomenon associated with first order loops (or injection locked oscillators) when driven by a signal outside the locking range.

Integration of Eqn. 4.49 also gives

$$t - t_0 = \frac{-2}{\sqrt{K^2 - (\Delta\omega)^2}} \tanh^{-1}\left[\frac{\Delta\omega \cdot \tan\left(\frac{\varphi_e}{2}\right) - K}{\sqrt{K^2 - (\Delta\omega)^2}}\right] \qquad \ldots\ldots\ldots 4.53$$

when $K^2 > (\Delta\omega)^2$ and $\left|\Delta\omega \tan\left(\frac{\varphi_e}{2}\right) - K\right| < \sqrt{K^2 - (\Delta\omega)^2}$

and

$$t - t_0 = \frac{-2}{\sqrt{K^2 - (\Delta\omega)^2}} \operatorname{ctnh}^{-1}\left[\frac{\Delta\omega \cdot \tan\left(\frac{\varphi_e}{2}\right) - K}{\sqrt{K^2 - (\Delta\omega)^2}}\right] \qquad \ldots\ldots\ldots 4.54$$

when $K^2 > (\Delta\omega)^2$ and $\left|\Delta\omega \tan\left(\frac{\varphi_e}{2}\right) - K\right| > \sqrt{K^2 - (\Delta\omega)^2}$

The conditions $\left|\Delta\omega \tan\left(\frac{\varphi_e}{2}\right) - K\right| < \sqrt{K^2 - (\Delta\omega)^2}$ and $\left|\Delta\omega \tan\left(\frac{\varphi_e}{2}\right) - K\right| > \sqrt{K^2 - (\Delta\omega)^2}$ correspond to initial values of phase error above and below the steady state value and give rise to transients with phase error either increasing or decreasing with time. The different phase paths are demorstrated subsequently in Fig. 4.8.

Taking first the case for $\left|\Delta\omega \tan\left(\frac{\varphi_e}{2}\right) - K\right| > \sqrt{K^2 - (\Delta\omega)^2}$
Eqn. 4.54 gives

$$\text{ctnh}\left[-\frac{(t-t_0)\sqrt{K^2-(\Delta\omega)^2}}{2}\right] = \frac{\Delta\omega.\tan\left(\frac{\varphi_e}{2}\right) - K}{\sqrt{K^2-(\Delta\omega)^2}} \qquad \ldots\ldots 4.55$$

Making use of the relation

$$\text{ctnhx} = \frac{\exp(2x)+1}{\exp(2x)-1}$$

yields

$$\varphi_e(t) = 2\tan^{-1}\left[\frac{K\left[\exp\left((t-t_0)\sqrt{K^2-(\Delta\omega)^2}\right)-1\right]-\sqrt{K^2-(\Delta\omega)^2}\left[\exp\left((t-t_0)\sqrt{K^2-(\Delta\omega)^2}\right)+1\right]}{\Delta\omega\left[\exp\left((t-t_0)\sqrt{K^2-(\Delta\omega)^2}\right)-1\right]}\right]$$

$\ldots\ldots\ldots\ldots 4.56$

Although the integration constant t_0 would normally be chosen to give φ_e equal to the initial value at the start of the transient for any particular case, the form of the first order loop transient is most conveniently illustrated by taking t_0 such as to give $\varphi_e = \pi/2$ rads at $t = 0$, since then the expression given by Eqn. 4.56 is skew-symmetric about $t = 0$. Similarly for the case

$$\left|\Delta\omega.\tan\left(\frac{\varphi_e}{2}\right) - K\right| < \sqrt{K^2-(\Delta\omega)^2}$$

φ_e will equal $-\frac{\pi}{2}$ rads with this value of t_0.

Thus taking

$$\exp\left(-t_0\sqrt{K^2-(\Delta\omega)^2}\right) = \frac{K-\Delta\omega+\sqrt{K^2-(\Delta\omega)^2}}{K-\Delta\omega-\sqrt{K^2-(\Delta\omega)^2}} = C \qquad \ldots\ldots\ldots 4.57$$

say

$$\varphi_e(t) = 2\tan^{-1}\left[\frac{K\left[C\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)-1\right]-\sqrt{K^2-(\Delta\omega)^2}\left[C\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)+1\right]}{\Delta\omega\left[C\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)-1\right]}\right] \quad \ldots\ldots 4.58$$

which reduces to

$$\varphi_e(t) = 2\tan^{-1}\left[\frac{\frac{K-\sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega}\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)+1}{\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)+\frac{K-\sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega}}\right] \quad \ldots\ldots 4.59$$

Secondly, when $\left|\Delta\omega.\tan\left(\frac{\varphi_e}{2}\right)-K\right| < \sqrt{K^2-(\Delta\omega)^2}$

we have from Eqn. 4.53

$$\tanh\left[\frac{-(t-t_0)\sqrt{K^2-(\Delta\omega)^2}}{2}\right] = \frac{\dot{\Delta\omega}.\tan\left(\frac{\varphi_e}{2}\right)-K}{\sqrt{K^2-(\Delta\omega)^2}} \quad \ldots\ldots 4.60$$

from which is obtained, similarly

$$\varphi_e(t) = 2\tan^{-1}\left[\frac{\frac{K-\sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega}\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)-1}{\exp\left(\sqrt{K^2-(\Delta\omega)^2}t\right)-\frac{K-\sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega}}\right] \quad \ldots 4.61$$

The frequency transient of the VCC may be simply obtained from the above expressions, since ω_2, the VCO output frequency is given by

$$\omega_2(t) = \omega_0 + K_2u_2(t) \quad \ldots\ldots 4.62$$

$$\text{therefore } \omega_2(t) = \omega_0 + AK_1K_2\sin\varphi_e(t) \quad \ldots\ldots 4.63$$

Thus

$$\frac{\omega_2(t)-\omega_0}{K} = \sin\varphi_e(t) \quad \ldots\ldots 4.64$$

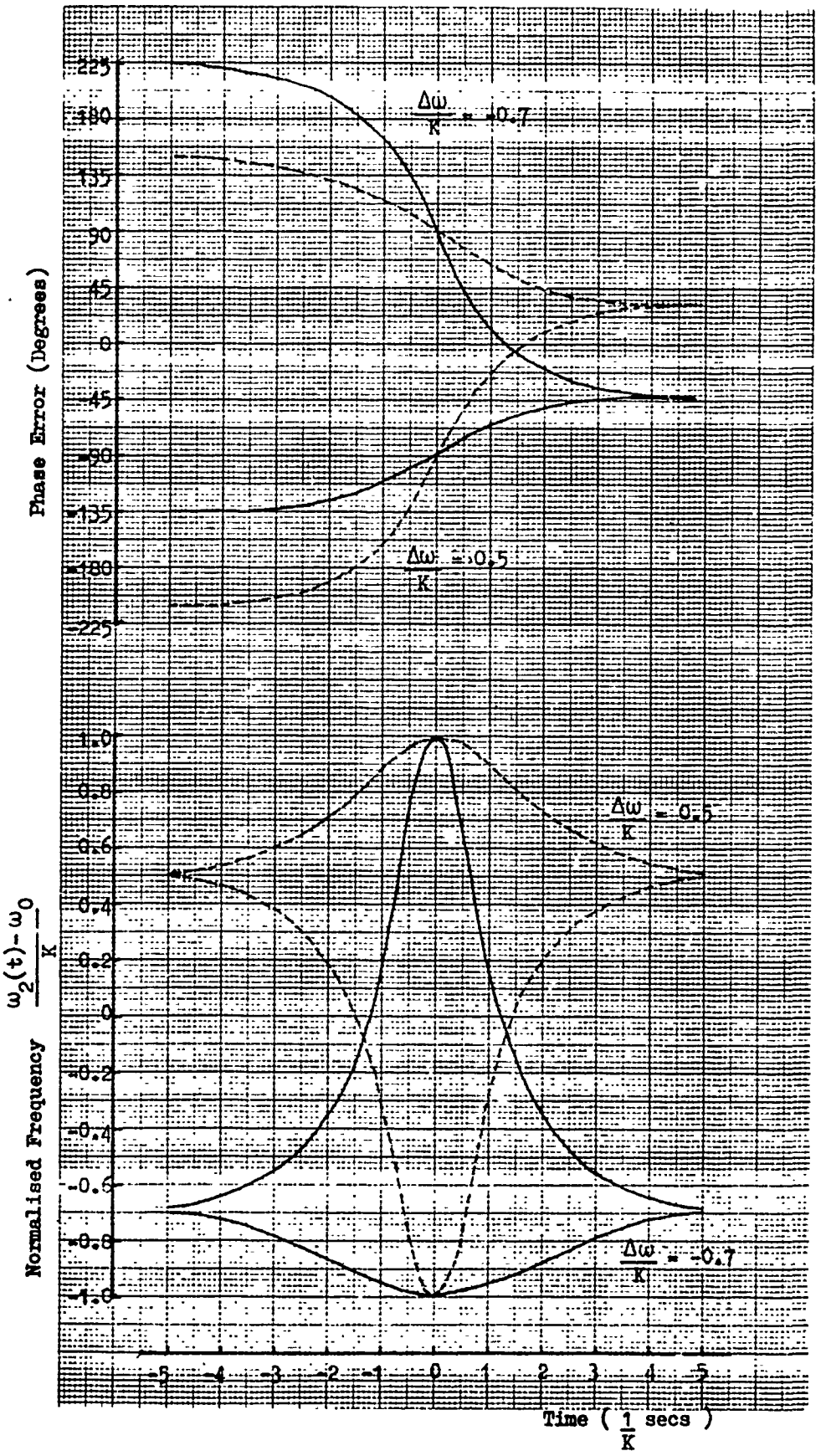


Fig. 4.7 Phase and Frequency Transients of a First Order Loop

The variation of $\varphi_e(t)$ and $\frac{\omega_2(t)-\omega_0}{K}$ with time (normalised to units of $1/K$ secs) is shown in Fig. 4.7 for two values of detuning, $\Delta\omega/K = 0.5$ and -0.7. Note that the time scale is normalised to give a symmetric plot around $t = 0$ as previously described. The transient is of the same form as that given for injection locking in Fig. 4.5 as may be expected since similar differential equations describe the injection locking and the first order loop.

As before, the transient response, which could be due either to a sudden phase shift applied to the locking signal, or to the sudden energization of a pulsed VCO, is determined by taking the point on the phase transient corresponding to the initial value of phase error and hence following the transient for increasing time. Similarly the frequency transient is entered at the point on the time scale corresponding to the initial value of phase error.

The asymptotic values of phase and frequency appearing at large negative values of t correspond to an initial phase close to the unstable equilibrium position and it may be seen that the time required for the loop to reach the stable locking condition may be relatively long for this case. The stable and unstable equilibrium positions related to the PSD output are shown in Fig. 4.8, from which the significance of the two solutions of Eqns. 4.59 and 4.61, corresponding to movement in different directions from the unstable equilibrium position, may be seen. The stable locking position will be located on the PSD slope yielding negative feedback around the loop.

The steady state phase error, obtained from either Eqn. 4.59 or 4.61, when $t \to \infty$ is given by

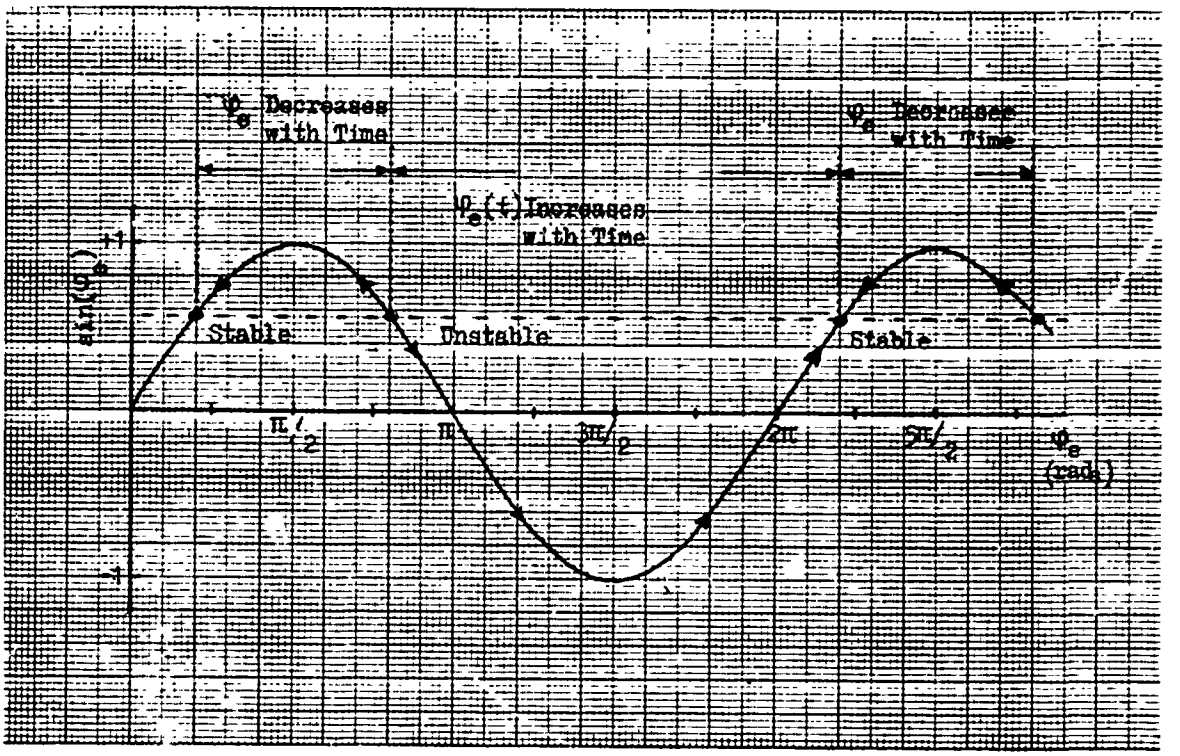


Fig. 4.8 Phase Sensitive Detector Characteristic

$$\varphi_e(\infty) = 2\tan^{-1}\left[\frac{K - \sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega}\right] \qquad \ldots\ldots.4.65$$

$$\text{therefore } \tan\frac{\varphi_e(\infty)}{2} = \frac{K - \sqrt{K^2-(\Delta\omega)^2}}{\Delta\omega} \qquad \ldots\ldots\ldots4.66$$

for which, using $\tan(\frac{x}{2}) = \dfrac{1 - \cos x}{\sin x}$

$$\sin\varphi_e(\infty) = \frac{\Delta\omega}{K}$$

$$\text{and } \varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

as previously established in Eqn. 4.48.

Considering first the effect of the transient behaviour on the response of ideal pulsed VCOs, the phase transient for a representative case of $\Delta\omega/K = 0.5$ is shown in more detail in Fig. 4.9. Bearing in mind that the initial phase state of a pulsed VCO will be random, all phases being equally likely, it is of interest to examine the statistical distribution of the time required for the PLL to achieve lock. It may be seen from Fig. 4.9 that the phase error has been reduced to less than $\pm 3^\circ$ of the final value by a time $+\frac{4}{K}$ secs, and taking this value as the point at which the capture transient may be considered to be complete (since phase errors of $\pm 3^\circ$ will produce a radiation pattern with a reasonably low sidelobe level) the statistical distribution of capture times for random initial phases may be obtained. Fig. 4.10(a) shows the percentage of initial starting phases which result in capture times within each time interval i.e.

$$0 < Kt < 1 \;,\quad 1 < Kt < 2 \quad \text{etc.}$$

on the horizontal axis. It may be seen that approximately half (54%) of capture times will be of duration $3 < Kt < 5$.

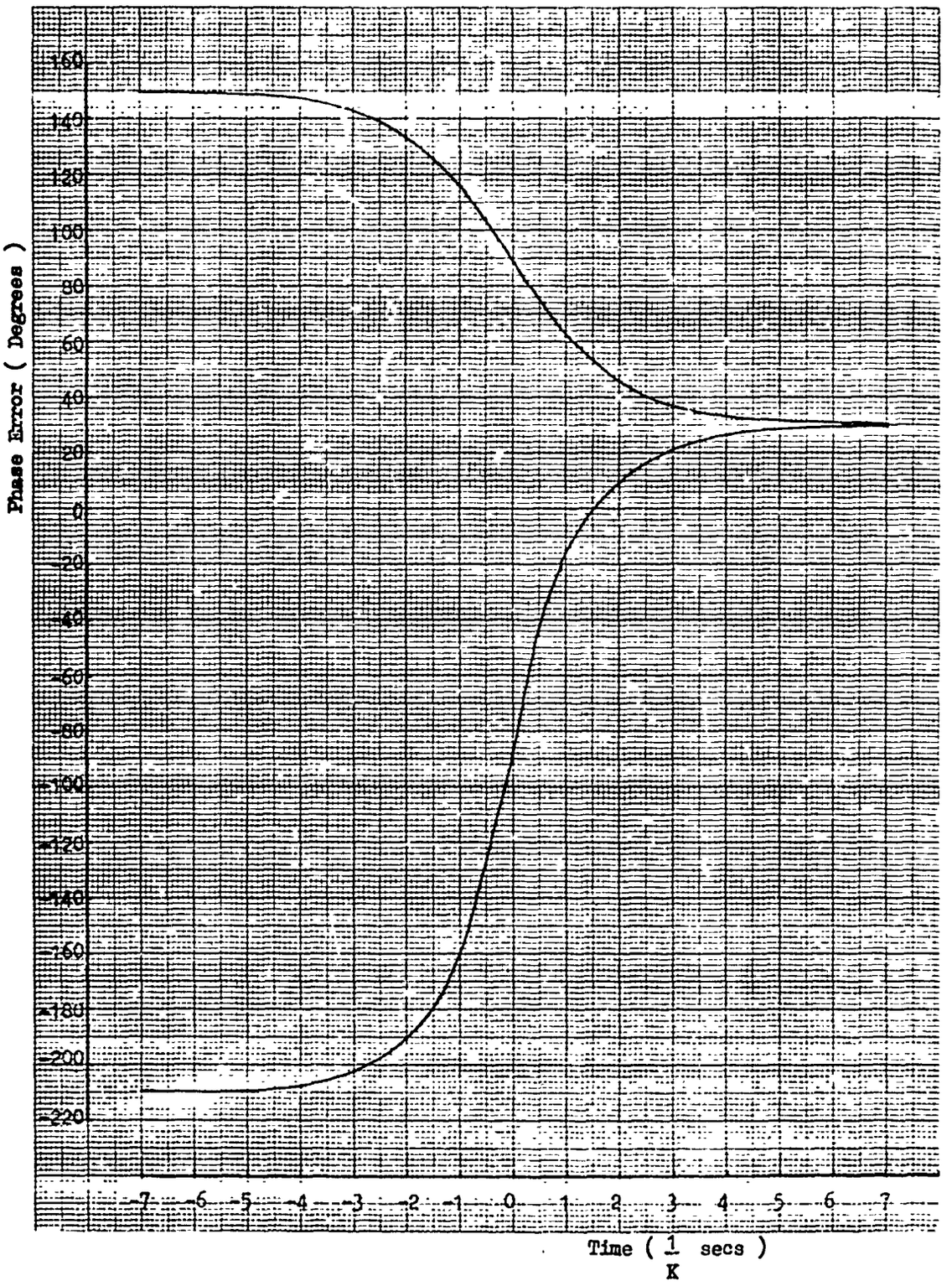


Fig. 4.9 First Order Loop Phase Transient for $\frac{\Delta\omega}{K} = 0.5$

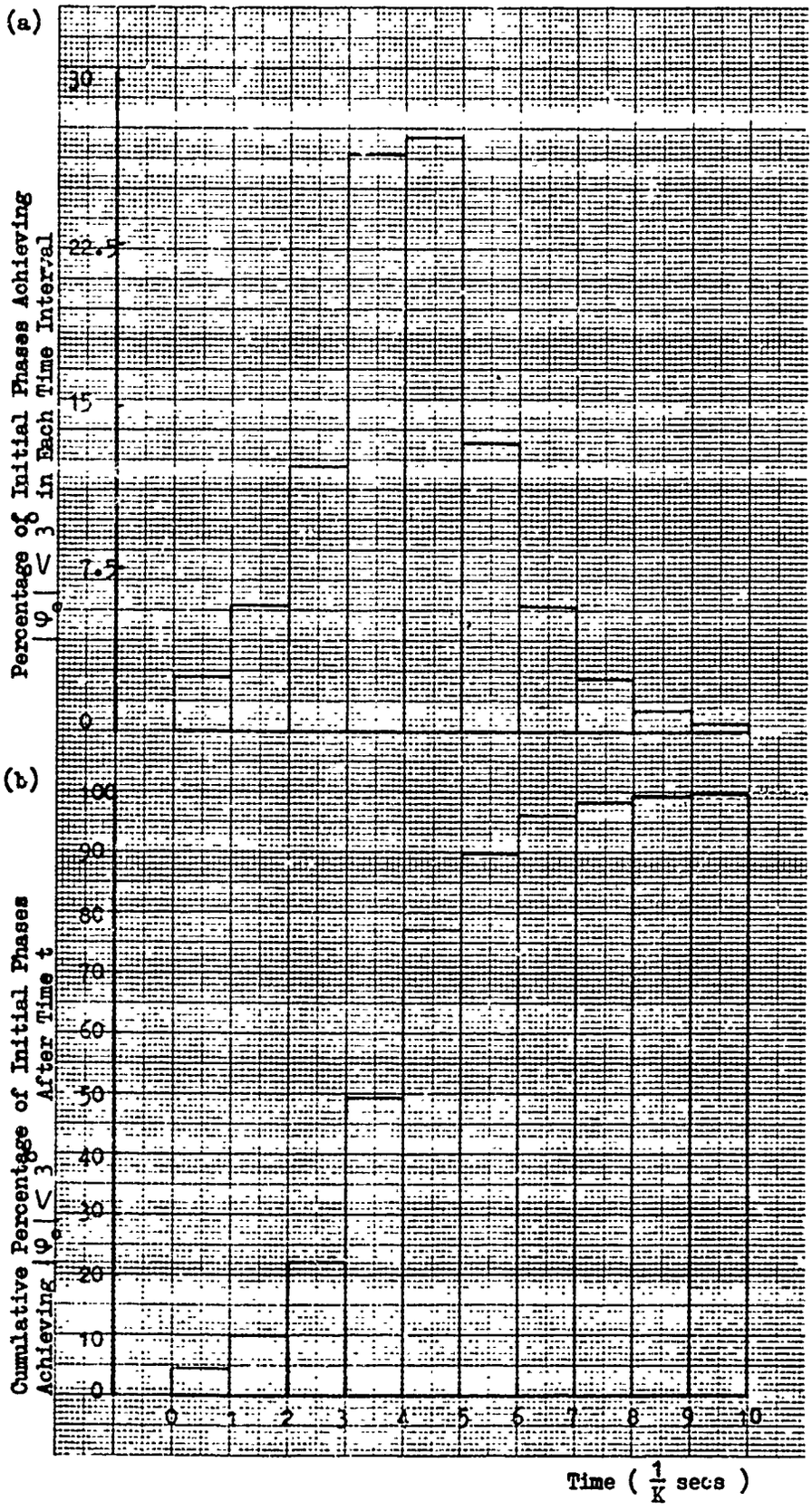


Fig. 4.10 **First Order Loop Acquisition Time**

The cumulative percentage of initial starting phases having achieved lock after time t is shown in Fig. 4.10(b). Ninety percent of transients may be seen to be over after $t = \frac{6}{K}$ secs ($\approx$ 1/locking range in HZ) and 99.7% over after $t = \frac{10}{K}$ secs., the remaining 0.3% being due to initial phases very close to the unstable equilibrium value. Thus for illustration, assuming $\Delta\omega/K = 0.5$ in all cases and random initial starting phases, 3 of an array of 1000 pulsed VCOs so locked would have $|\varphi_e| > 3^\circ$ after $t = \frac{10}{K}$ secs.

The figures given in Fig. 4.10(a) and (b) are for the case $\Delta\omega/K = 0.5$ but in light of the time constant of exponential terms in Eqns. 4.59 and 4.61, it would be expected that capture time will be related to detuning $\Delta\omega$. The variation with normalised detuning of time required for 95% of possible initial phases to achieve $|\varphi_e| < 3^\circ$ is given in Fig. 4.11 from which it may be seen that for $\Delta\omega/K$ up to 0.9, most initial phase conditions will have achieved the steady state value in

$$t = \frac{10}{K} \text{ secs} \qquad \ldots\ldots\ldots 4.67$$

Transient Response Including Linear Frequency Chirp

The locking transient of practical pulsed sources may be complicated by a temperature induced change in free running frequency (chirp) during the pulse. If a linear frequency change is assumed (as may be seen to be approximately the case for the pulsed varactor tuned Gunn oscillators used in subsequent experiments) of slope P rad/s^2, the VCO output phase $\varphi_2(t)$ becomes

$$\varphi_2(t) = \int (u_2 K_2 + P.t)\, dt \qquad \ldots\ldots\ldots 4.68$$

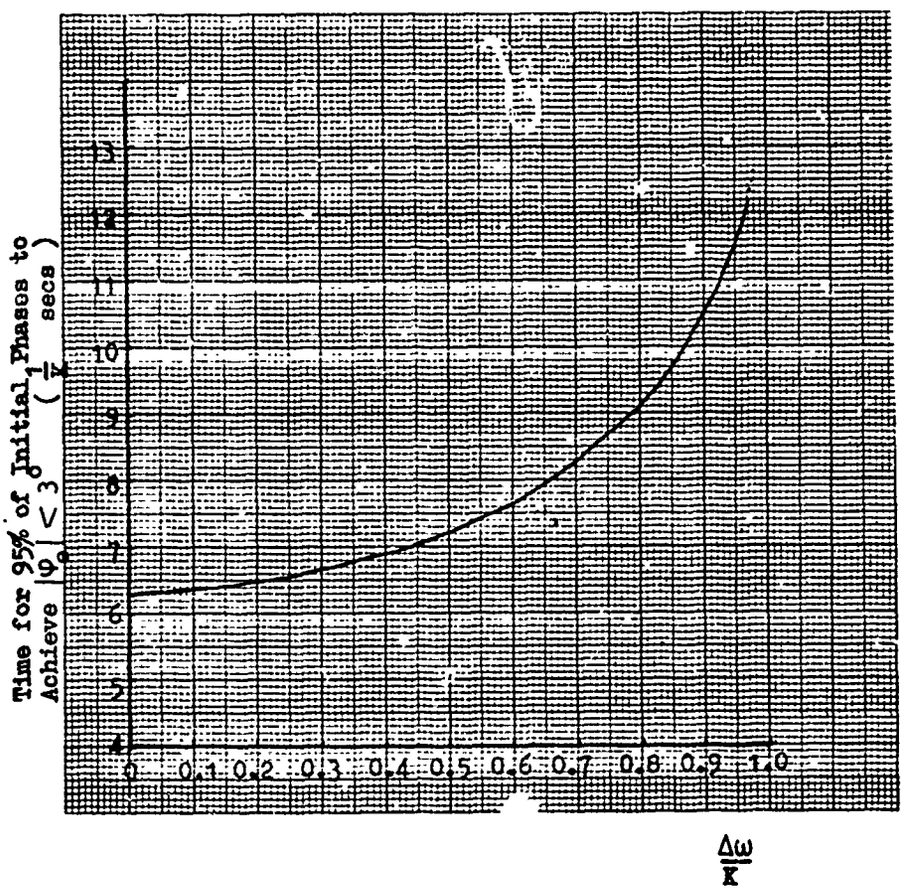


Fig. 4.11 Variation of Acquisition Time with Detuning

Eqn. 4.45 then becomes

$$\frac{d\varphi_e(t)}{dt} = \Delta\omega - Pt - K \sin\varphi_e(t) \qquad \text{.....4.69}$$

which is not of easily integrable form.

It would be expected that the effect on the loop transient would be small however if the change in free running angular frequency during the transient is small in relation to the locking range. Fig. 4.12 shows a chirp slope of 5MHz/μs (a typical value obtained experimentally from a 150mW pulsed Gunn oscillator at 10.5GHz) plotted against an ideal frequency transient for a typical loop with

$$K = \Delta\omega_L = 2\pi.10^7 \text{ rad/s}$$

Little change in the form of the frequency transient would be expected in this case although one minor effect will be to reduce the small number of relatively long transients, since the change in free running frequency will ensure disturbance of initial locking conditions close to the unstable equilibrium position.

The form of the subsequent response of the loop to the frequency chirp may be illustrated by linear theory, for cases in which the linearising approximation $\sin\varphi_e \approx \varphi_e$ can be made. A frequency ramp applied to the VCO free running frequency may be seen to be equivalent to a frequency ramp applied to the input locking signal. If the equivalent slope of the input frequency is P rad/s^2 from t = 0 and assuming zero initial detuning the locking signal phase $\varphi_0(t)$ may be expressed as $\Phi_0(s) = \frac{P}{s^3}$ in operational notation.

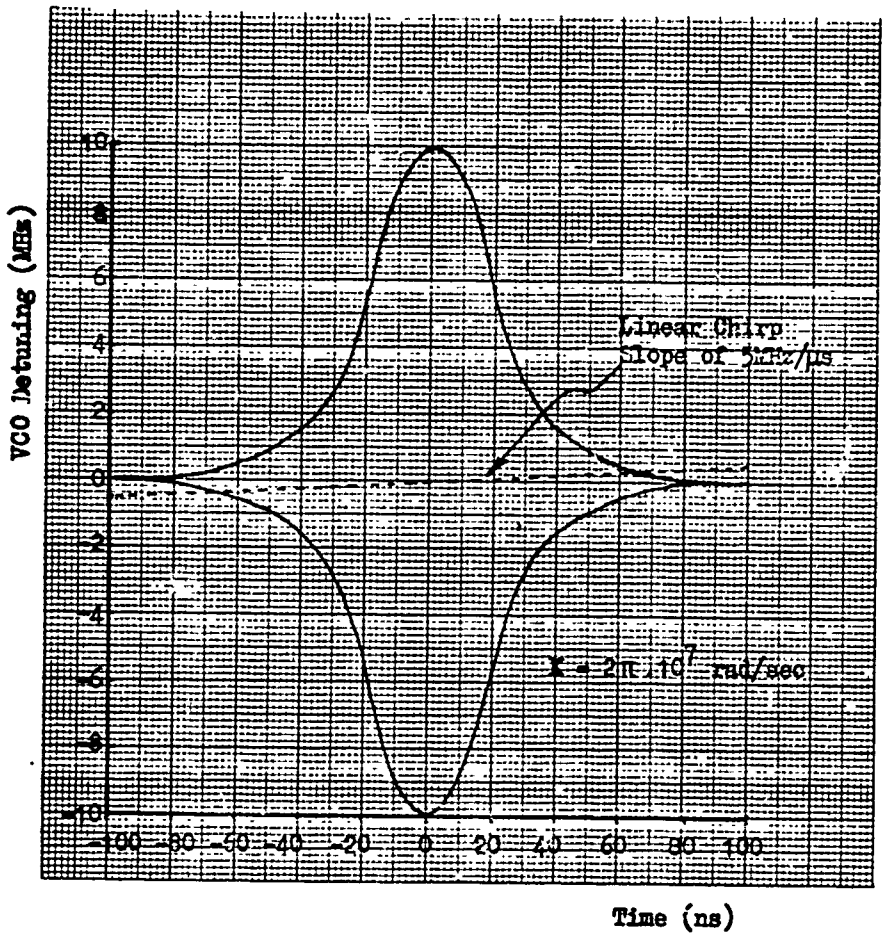


Fig. 4.12 First Order Loop Frequency Transient ($\Delta\omega = 0$)

From Eqn. 4.39

$$\Phi_e(s) = \frac{s}{s + K}\,\Phi_0(s)$$

$$= \frac{P}{s^2(s + K)}$$

from which

$$\varphi_e(t) = \frac{Pt}{K} - \frac{P}{K^2}\left(1 - \exp(-Kt)\right) \qquad \ldots\ldots 4.70$$

Ignoring the transient component, which may for this case be assumed to be included in the loop capture transient, the steady state phase error may be seen to consist of a constant tracking error - P/K^2 and a term increasing linearly with time Pt/K corresponding to the ' steady state ' error for the detuning existing at time t. Using the values given previously for Fig. 4.12 the tracking error may be seen to be relatively small in practice :

$$-\frac{P}{K^2} = -7.96 \times 10^{-3}\,\text{rad}$$

when

$$P = 3.14 \times 10^{13}\,\text{rad/s}^2 \quad (5\text{MHz}/\mu\text{s})$$

and $$K = 2\pi.10^7\,\text{rad/s}$$

As t increases, the linearly varying component of the phase error may drive the loop into the nonlinear region, for which a phase error of the form $\sin^{-1}\left(\frac{Pt}{K}\right)$ may be expected, and eventually if a phase error of $\pm 90^\circ$ is reached the loop will fall out of lock. From the example an error of 30° would be expected after 1μs, which would,

in practice, be unacceptably high. Ideally a value of loop gain K much greater than P.t would clearly be chosen to reduce the error, but it is subsequently shown that practical values of K for the first order loop are restricted due to loop instability.

A more exact description of the behaviour of the loop under chirp conditions may be obtained from solution of Eqn. 4.69 using the phase plane technique described in section 4.2.4.

Response to Pulse Compression Modulations

Modulations applied via the locking signal for the purpose of increasing the transmitted signal bandwidth, as described previously for injection locking, commonly take the form of phase shift keying or linear frequency modulation. Typically transmitter bandwidths between 1MHz and 10MHz are required.

In light of previous analysis of the loop transient behaviour, it may be seen that a phase shift keyed locking signal would give rise to a transient described by Eqn. 4.49 at each discontinuity of the input phase. The time for the loop to re-establish the equilibrium condition may be approximated by $\frac{10}{K}$ secs, and this time then represents the minimum period of the modulation. The maximum PSK frequency will therefore be $\frac{K}{10}$ Hz, although it should be noted that at such rates the loop transient will result in significant spectral degradation.

In particular for the case of zero frequency detuning, as may be seen from Fig. 4.8, sudden 180° phase shifts applied to the locking signal will transfer the loop exactly to the unstable equilibrium position, resulting in maximum distortion. In addition to the waveform distortion, inevitable differences in the transient between

elements will degrade the array radiation pattern during this time. PSK modulation will therefore only be suitable when the period $\frac{10}{K}$ is short relative to the modulation period and pulse length.

The loop response to a linear FM applied to the locking signal, previously established for a linear PSD in Eqn. 4.70 shows that the phase error contains a constant tracking error which is typically small, and a term linearly increasing with time due to the progressive detuning of the VCO. The maximum frequency deviation that may be applied will therefore be limited by the maximum acceptable phase error, where the phase error φ_e is given for the sinusoidal PSD by

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

Thus to ensure low phase error between elements the maximum value of the detuning $\Delta\omega$ must be small compared with K.

Summary of the First Order Loop Behaviour

It may be seen that the behaviour of the first order phase locked loop is very similar to that of injection locking in both steady state and transient phase error. The phase error due to detuning between the locking signal and the VCO free running frequency (which may be caused either through temperature drift, aging , pulsed VCO chirp or intentional linear FM applied to the locking signal) is given by Eqn. 4.48

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

The acquisition time, being the time required to ensure the steady state value of phase error has been reached for the majority of initial phase conditions, is given by Eqn. 4.67

$$t = \frac{10}{K} \text{ secs}$$

It is desirable to minimise both of these quantities in practice and since they are both inversely related to the loop gain $K = AK_1K_2$, theoretically this may simply be achieved by increasing the amplifier gain A to a sufficiently high level. (In comparison, the equivalent quantities in injection locking may only be minimised at the expense of locking gain.) However, as will be shown in section 4.2.6 loop instability due to signal delay around the loop limits the magnitude of the loop gain in realisable loops, such that typically the locking range of the first order loop is limited to some tens of MHz and this will, in general, be insufficient to ensure adequately low phase error when microwave VCOs are used. It is shown in the following section however, that the inclusion of suitable loop filtering permits the inclusion of further amplification in the PLL and a subsequent reduction of phase error to adequately low level.

A further description of the practical performance that may be achieved with the first order loop is given in section 4.2.8.

4.2.4 Second Order Loops

The second order loop overcomes the first order loop limitation on locking range, by providing high loop gain at low frequency, to yield low steady state phase error, whilst reducing the gain at high frequency to maintain stability.

The three filter types giving rise to second order loops are described by

$$F(s) = \frac{1}{1 + s\tau_1}, \quad F(s) = \frac{1+ s\tau_2}{1+ s\tau_1} \quad \text{and} \quad F(s) = \frac{1+ s\tau_2}{s\tau_1}$$

the frequency responses and possible circuit realisations of which are shown in Fig. 4.13.

In practice the simple 'lag' filter with transfer function

$$F(s) = \frac{1}{1 + s\tau_1}$$

shown in Fig. 4.13(a) would not be suitable since its use often leads to instability. As described in more detail in section 4.2.6 the high frequency phase shift introduced by this filter, when added to the -90° due to the integrating action of the VCO, will approach -180°. Although the phase shift in an ideal loop would not reach -180°, the inevitable spurious phase shifts present in practical loops commonly result in oscillation.

The addition of a ' lead ' term resulting in a filter transfer function

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1}$$

reduces the tendency to instability by reducing the filter insertion phase to zero degrees at high frequency. This response is obtained from the passive filter of Fig. 4.13(b). These filter transfer

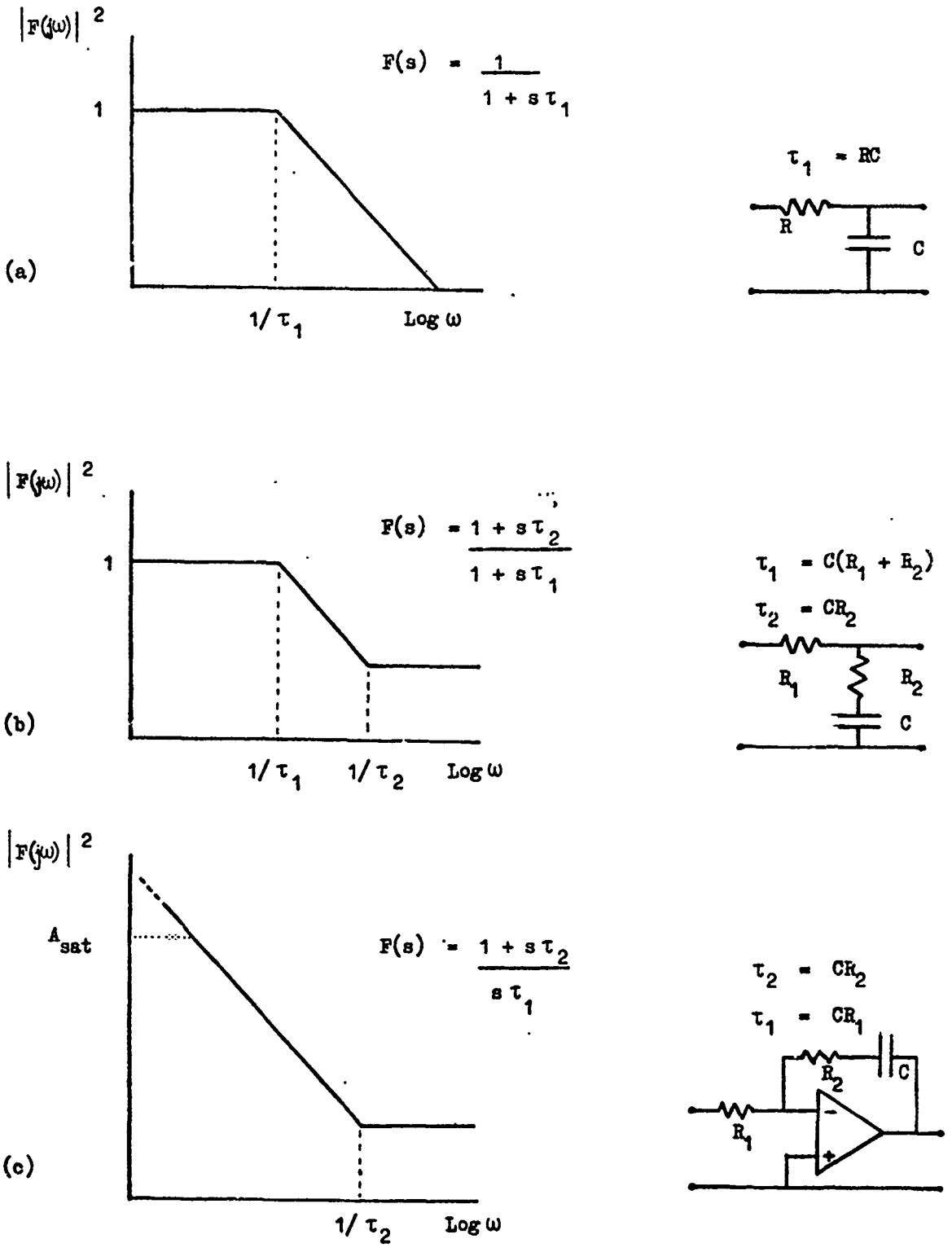


Fig. 4.13 Frequency Responses of Second Order Loop Filters

functions result in second order, type one loops.

The transfer function

$$F(s) = \frac{1 + s\tau_2}{s\tau_1}$$

yielding a type two second order loop, is produced by an ideal integrator plus a phase ' lead ' network. Although the integration function can be approached with a high gain operational amplifier, the gain of practical amplifiers will inevitably saturate at some value (as indicated by the dotted curve in Fig. 4.13(c) and the response in practice will be equivalent to that obtained from an ideal amplifier of frequency independent gain A_{sat} followed by the passive filter of Fig. 4.31(b), i.e.

$$F(s) = A_{sat}\left(\frac{1 + s\tau_2}{1 + s\tau_1}\right)$$

where τ_1 is now the period corresponding to the angular frequency at which saturation occurs. Since the gain A_{sat} may for convenience be considered to be included in the gain of the ideal loop amplifier, second order loop analysis may therefore be simply confined in practice to second order type one loops with filter transfer functions of the form

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1} \qquad \text{.....4.71}$$

Derivation of the General Time Domain Equation

With reference to Fig. 4.6, the combined transfer function of the ideal amplifier and filter using Eqn. 4.71 may be written

$$\frac{U_2(s)}{U_1(s)} = \frac{A(1 + s\tau_2)}{(1 + s\tau_1)} \qquad \text{.....4.72}$$

The time domain equation relating u_1 and u_2 is then

$$\tau_1 \frac{du_2}{dt} + u_2 = A\left[u_1 + \tau_2 \frac{du_1}{dt}\right] \qquad \text{.....4.73}$$

We have from Eqn. 4.31

$$u_1(t) = K_1 \sin\left(\varphi_1(t) - \varphi_2(t)\right) \qquad \text{.....4.74}$$

and thus

$$\frac{du_1}{dt} = K_1 \cos\left[\varphi_1(t) - \varphi_2(t)\right]\left(\frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt}\right) \qquad \text{.....4.75}$$

From Eqn. 4.29

$$\frac{d\varphi_2(t)}{dt} = K_2 u_2(t)$$

Differentiating again gives

$$\frac{d^2\varphi_2}{dt^2} = K_2 \frac{du_2}{dt} \qquad \text{.....4.76}$$

Substituting Eqns. 4.74, 4.75 and 4.76 into Eqn. 4.73 yields

$$\tau_1 \frac{d^2\varphi_2}{dt^2} + \frac{d\varphi_2}{dt} = AK_1K_2\sin\left[\varphi_1(t) - \varphi_2(t)\right] + AK_1K_2\tau_2\cos\left[\varphi_1(t) - \varphi_2(t)\right]\left(\frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt}\right) \quad \ldots\ldots 4.77$$

which is the generalised time domain quotation for a second order loop with lag/lead filter.

We have previously defined the phase error φ_e as $\varphi_e = \varphi_1 - \varphi_2$ hence

$$\frac{d\varphi_e}{dt} = \frac{d\varphi_1}{dt} - \frac{d\varphi_2}{dt} \quad \ldots\ldots 4.78$$

When the locking signal frequency is constant $\frac{d\varphi_1}{dt}$ is a constant and thus from Eqn. 4.78

$$\frac{d^2\varphi_e}{dt^2} = -\frac{d^2\varphi_2}{dt^2}$$

Substituting, Eqn. 4.77 then becomes

$$\frac{d\varphi_1}{dt} = \tau_1\frac{d^2\varphi_e}{dt^2} + \frac{d\varphi_e}{dt}\left[1 + K\tau_2\cos\varphi_e(t)\right] + K\sin\varphi_e(t) \quad \ldots\ldots 4.79$$

where $K = AK_1K_2$ as before.

A check on Eqn. 4.79 can be made by equating τ_1 and τ_2 to zero

since then $F(s) = 1$ and a first order loop should be obtained.

Eqn. 4.79 with $\tau_1 = \tau_2 = 0$ gives

$$\frac{d\varphi_1}{dt} = \frac{d\varphi_e}{dt} + K\sin\varphi_e(t)$$

and since $\frac{d\varphi_1}{dt} = \Delta\omega$

$$\frac{d\varphi_e}{dt} = \Delta\omega - K\sin\varphi_e(t)$$

which is the same as Eqn. 4.45.

The steady state response of the second order loop for a constant locking signal frequency is obtained directly from Eqn. 4.79 with

$$\frac{d^2\varphi_e}{dt^2} = \frac{d\varphi_e}{dt} = 0$$

for which the assumption is made that lock is achieved.

Hence

$$\frac{d\varphi_1}{dt} = K\sin\varphi_e$$

therefore $\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$ 4.80

The locking range $\Delta\omega_L$ is obtained by noting the restriction

$$\left|\sin\varphi_e\right| \leq 1$$

giving $\Delta\omega_L = K$ 4.81

Similarly the synchronisation range $\Delta\omega_s$ is

$$\Delta\omega_s = 2K \qquad \text{.....4.82}$$

The expressions of Eqn. 4.80 and 4.82 may be seen to be the same as those obtained for the first order loop in Eqn. 4.48 and 4.47.

As before, the transient response of the loop is of interest for predicting the loop behaviour when a pulsed VCO is used, or when modulation is applied to the locking signal. An exact solution to Eqn. 4.79 is not available however, since this is a second order nonlinear differential equation, analytically insoluble; nevertheless the form of the transient may be obtained indirectly. The more precise indirect method of analysis, described subsequently, uses the phase plane approach, but a good deal of insight into second order transient behaviour may also be obtained from physical reasoning and the results previously established for first order loop.

With reference to Fig. 4.14 in which the amplitude response of the type one second order loop filter is again shown, it may be seen that at high frequency, the filter is simply an attenuator of voltage ' gain ' τ_2/τ_1. This is established as follows :

we have

$$F(j\omega) = \frac{1 + j\omega\tau_2}{1 + j\omega\tau_1}$$

Hence

$$\left|F(j\omega)\right| = \sqrt{\frac{1 + \omega^2\tau_2^2}{1 + \omega^2\tau_1^2}}$$

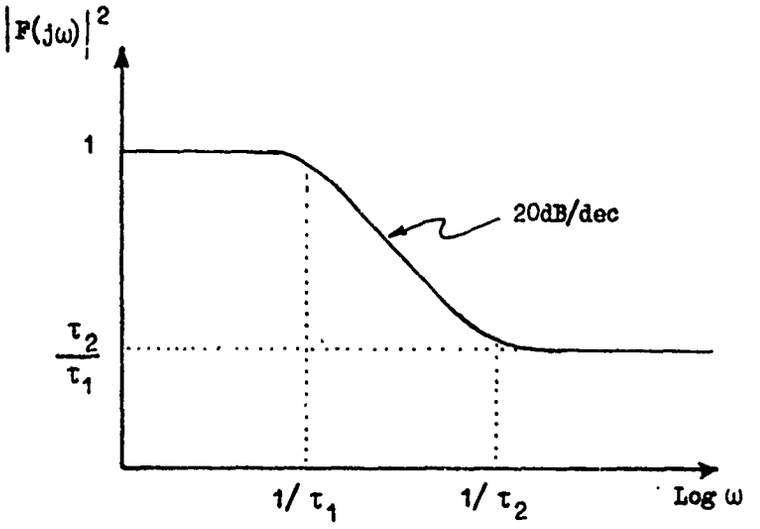


Fig. 4.14 First Order, Type one Loop Filter Response

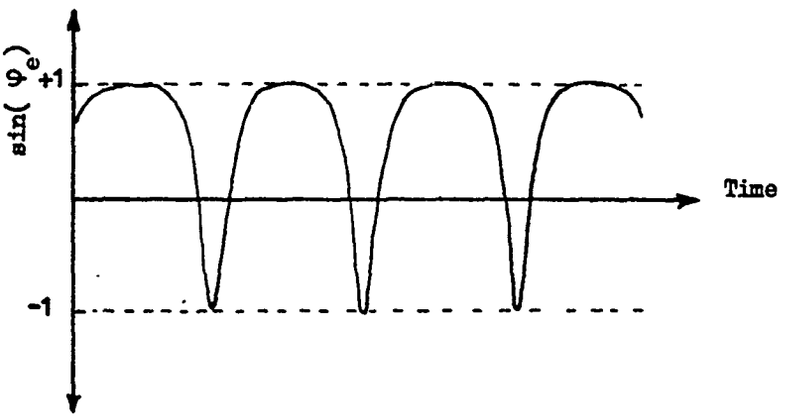


Fig 4.15 PSD Output Waveform for $\Delta\omega > K$

When ω is large

$$|F(j\omega)| \rightarrow \sqrt{\frac{\omega^2\tau_2^2}{\omega^2\tau_1^2}} = \frac{\tau_2}{\tau_1} \qquad \text{.....4.83}$$

When a large detuning exists between the VCO free running frequency and the locking signal a high difference frequency will be present in the loop and the gain of the loop will thus be reduced by the factor τ_2/τ_1 from the low frequency value. Under these conditions, assuming that the detuning is such that immediate lock of the VCO is not possible, the loop will appear to be a first order loop of reduced gain, driven with a synchronising signal outside the locking range. The behaviour for this situation was established in Eqn. 4.51 and an illustration of the PSD output for this case is shown in Fig. 4.15. It may be noted that this waveform is asymmetric, due to modulation of the VCO by the difference frequency, and contains a DC component. Fig. 4.14 however, shows the loop filter to have higher ' gain ' (unity) at DC and thus the DC component of the PSD output will cause the VCO frequency to move, relatively slowly, towards that of the locking signal. The asymmetry of the PSD output is always such as to produce a DC component tending to reduce the difference frequency. This phenomenon of second order loops, in which the difference frequency of an unlocked loop gradually diminishes, is known as ' pull-in ' ; the VCO during this period is said to be ' skipping cycles '. If the difference frequency is reduced to a point approaching that at which lock can occur as predicted by first order theory, from Eqn. 4.52 the beat frequency present in the loop will be reduced. The loss introduced by the filter will, however, then also reduce, leading to greater VCO modulation. This in turn will lead to a further reduction of beat frequency and so on, and

the loop will rapidly become locked. A second order, type two loop with an ideal integrator will ' pull-in ' for any initial detuning ; the more realistic case represented by the second order, type one loop has a finite ' pull-in ' range. Approximate values for the ' pull-in ' range and time to acquire lock via ' pull-in ' are given by Blanchard(39) .

Since rapid synchronisation is required for a pulsed active array source, the pull-in form of locking transient will in general be unacceptably slow and a locking transient without cycle skipping will be required.

The range of initial difference frequencies over which capture without cycle skipping is obtained, defined here as the capture range $\Delta\omega_c$, cannot be exactly specified unless the initial phase difference is also known. However, an approximate value for any initial phase is simply given by the synchronisation range for a first order loop with loop gain equal to that existing at high frequency. Thus using the result established in Eqn. 4.47

$$\Delta\omega_c \approx 2 \cdot \frac{K\tau_2}{\tau_1} \qquad \text{.....4.84}$$

This approximation will be valid when

$$\left| \frac{K\tau_2}{\tau_1} \right| > \frac{1}{\tau_2} \qquad \text{.....4.85}$$

i.e. when $\Delta\omega_L$ for the equivalent first order loop is within the ' flat ' high frequency region of the filter response. This condition will usually be necessary to ensure stability.

To summarize the points made thus far, the synchronisation range of the second order loop can be represented as shown in Fig. 4.16. The synchronisation range within which the VCO, once locked, can track the locking signal, is

$$\Delta\omega_s = 2K$$

Within the synchronisation range, the capture range, approximated by

$$\Delta\omega_c = 2.\frac{K\tau_2}{\tau_1} \quad \text{rad/s}$$

gives the range of initial difference frequency for which the acquisition transient is relatively short and does not include ' cycle skipping '. Outside this range the VCO skips cycles during a relatively long pull-in phase before lock occurs. The range of frequency over which the loop can pull in to lock is given by Blanchard[39]. Since acquisition involving pull-in is not of practical interest, the discussion of the acquisition behaviour can now be limited to initial frequency differences within the capture range.

Phase Plane Analysis

Phase plane analysis is essentially a graphical method of solving differential equations and has been developed principally for the analysis of control systems. The application of the technique to PLLs is well described by Klapper and Frankle[40] and Viterbi[41] and the essential features are given below.

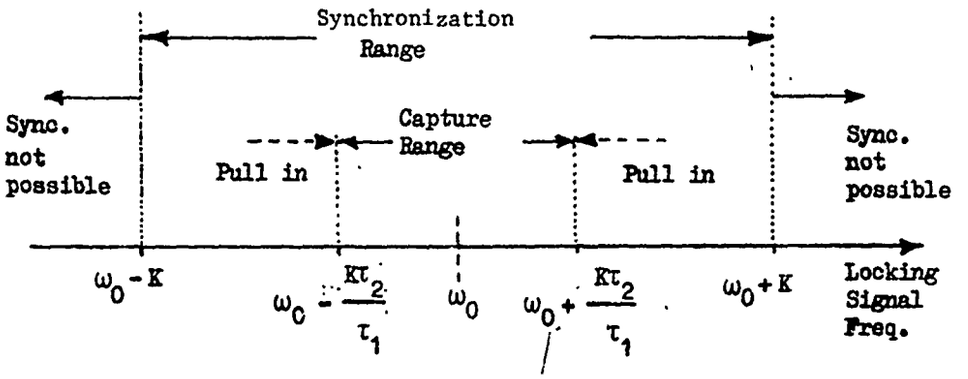


Fig. 4.16 Second Order Loop Synchronization and Capture Range

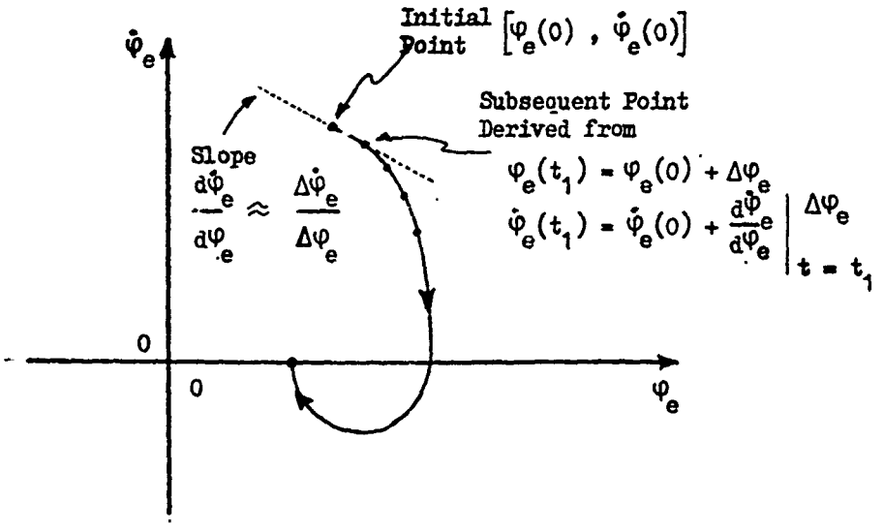


Fig. 4.17 Graphical Construction of Phase Plane Portrait

A plot is made of $\frac{d\varphi_e}{dt}$ against φ_e (hence the description phase plane analysis as shown in Fig. 4.17. For convenience the notation $\dot{\varphi}_e = \frac{d\varphi_e}{dt}$ is used here.

The plot is started by evaluating $\dot{\varphi}_e(t)$ at $t = 0$ from a known initial condition $\varphi_e(0)$. Thus we have the first point $\left[\dot{\varphi}_e(0),\ \varphi_e(0)\right]$. Subsequent points on the plot are found by noting that the slope at $\left[\dot{\varphi}_e(0),\ \varphi_e(0)\right]$ is

$$\left.\frac{d\dot{\varphi}_e}{d\varphi_e}\right|_{t=0} \approx \left.\frac{\Delta\dot{\varphi}_e}{\Delta\varphi_e}\right|_{t\neq 0} \qquad \text{..... 4.86}$$

and therefore the next point is approximately

$$\varphi_e(t_1) = \varphi_e(0) + \Delta\varphi_e \qquad \text{..... 4.87}$$

$$\dot{\varphi}_e(t_1) \approx \left(\left.\frac{d\dot{\varphi}_e}{d\varphi_e}\right|_{t=0} \times \Delta\varphi_e\right) + \dot{\varphi}_e(0) \qquad \text{.....4.88}$$

Similarly at this point the slope is again calculated and the plot is thus continued. A small value of $\Delta\varphi_e$ between points is used to ensure accuracy.

The time interval between evaluations is calculated by noting that

$$\frac{\Delta\varphi_e}{\Delta t} \approx \dot{\varphi}_e(t_1) \qquad \text{.....4.89}$$

Thus

$$\Delta t = \frac{\Delta\varphi_e}{\dot{\varphi}_e(t_1)} \qquad \text{.....4.90}$$

and

$$t_1 = \Delta t \qquad \text{..... 4.91}$$

By noting the time interval at each evaluation, the variation of φ_e with t can therefore be established.

An obvious difficulty arises in the computation of the plot from the fact that $d\dot{\varphi}_e/d\varphi_e \rightarrow \infty$ when $\dot{\varphi}_e \rightarrow 0$ as shown in Fig. 4.17. However the problem can be avoided by reducing $\Delta\varphi_e$ as the φ_e axis is approached ($\Delta\varphi_e$ was reduced from 0.5° to 0.01° in practice) and by arranging for the plot to ' jump over ' the axis when $d\dot{\varphi}_e/d\varphi_e$ is sufficiently large.

To evaluate the slope of the phase plane plot at each point we need an expression for $\dfrac{d\dot{\varphi}_e}{d\varphi_e}$

From Eqn. 4.79 we have

$$\tau_1 \frac{d^2\varphi_e}{dt^2} + (1 + K\tau_2\cos\varphi_e)\frac{d\varphi_e}{dt} + K\sin\varphi_e = \Delta\omega$$

Dividing each term by $\tau_1\dot{\varphi}_e$ we obtain

$$\frac{\ddot{\varphi}_e}{\dot{\varphi}_e} + \frac{1 + K\tau_2\cos\varphi_e}{\tau_1} + \frac{K\sin\varphi_e}{\tau_1\dot{\varphi}_e} = \frac{\Delta\omega}{\tau_1\dot{\varphi}_e} \qquad \text{.....4.92}$$

where $\ddot{\varphi}_e = \dfrac{d^2\varphi_e}{dt^2}$

Noting that

$$\ddot{\varphi}_e = \frac{d}{dt}(\dot{\varphi}_e) = \frac{d}{d\varphi_e}(\dot{\varphi}_e).\dot{\varphi}_e$$

we have

$$\ddot{\varphi}_e = \frac{d\dot{\varphi}_e}{d\varphi_e}.\dot{\varphi}_e \qquad \text{.....4.93}$$

and thus from Eqn. 4.92

$$\frac{d\dot{\varphi}_e}{d\varphi_e} = \frac{\Delta\omega - K\sin\varphi_e}{\tau_1\dot{\varphi}_e} - \frac{1 + K\tau_2\cos\varphi_e}{\tau_1} \qquad \text{.....4.94}$$

which is of the required form.

The initial value for $\dot{\varphi}_e$ at the start of the plot, given any initial φ_e, is taken from that pertaining to a first order loop with gain equal to the high frequency gain of the second order loop, i.e.

$$\dot{\varphi}_e = \Delta\omega - K\frac{\tau_2}{\tau_1}\sin\varphi_e$$

Several series of computations were made using phase plane analysis to establish the nature of the capture transient of the second order type one loop. The FORTRAN program used for this is given in Appendix 1. Results for a representative case of practical interest are shown in Fig. 4.18 in which we have

$$\Delta\omega = 6\pi.10^6 \text{ rad/s}$$
$$K = 2\pi.10^8 \text{ rad/s}$$
$$\tau_1 = 1/10\pi.10^5 \text{ sec}$$
$$\tau_2 = 1/10\pi.10^6 \text{ sec}$$

i.e. the filter roll-off frequencies are 500KHz and 5MHz.

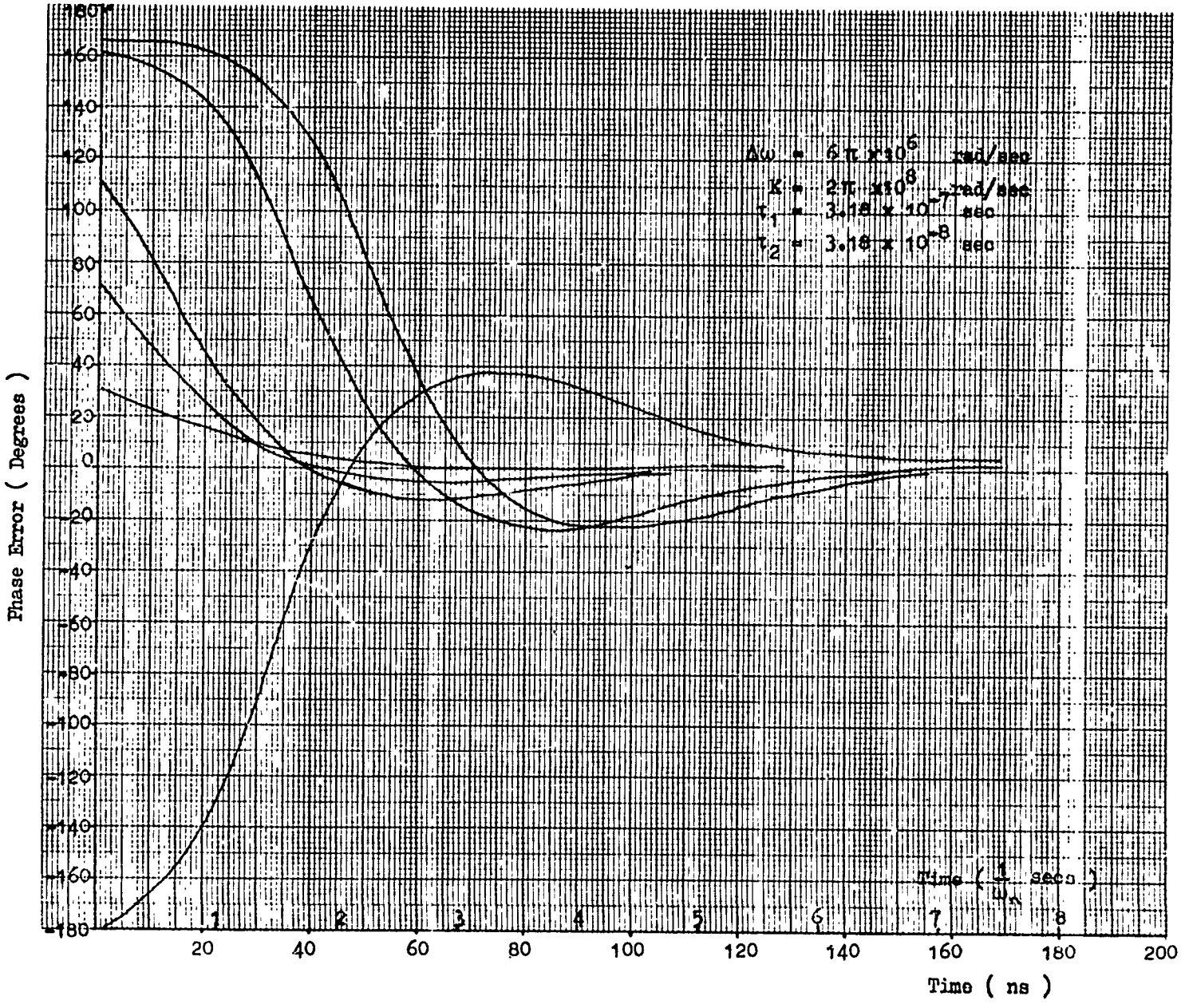


Fig. 4.18 Phase Transient Derived from Phase-Plane Analysis

It may be seen from the figure that after ~ 20ns the transients are all decreasing towards the final value. The subsequent overshoot, characteristic of a slightly underdamped second order system may be seen to decay in exponential fashion to the steady state value. The meaning of the scale marked in units of $1/\omega_n$ secs is explained shortly.

The theoretical value of steady state phase error is, from Eqn. 4.80

$$\varphi_e(\infty) = 1.7^\circ$$

and the locking range for this case is

$$\Delta\omega_L = K = 2\pi.10^8 \text{rad/s}$$

Since phase plane analysis does not yield a general solution to Eqn. 4.79 it will be necessary to examine all the possible capture transients for each individual second order loop in order to predict the time required for the majority of possible initial conditions to achieve the steady state phase error.

A general approximation can be obtained however, from the linearised theory of the loop which can also be applied to the nonlinear analysis.

Linear Theory of the Second Order Loop

When the linearising approximation $\sin\varphi_e \approx \varphi_e$ can be made, the error function of a PLL in operational notation is

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s}{s + KF(s)}$$

Using

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1}$$

gives

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s(1 + s\tau_1)}{s(1 + s\tau_1) + K(1 + s\tau_2)}$$

$$= \frac{s^2 + s/\tau_1}{s^2 + s(1 + K\tau_2)/\tau_1 + K/\tau_1} \qquad \ldots 4.95$$

It is common to form an analogy between Eqn. 4.95 and the equivalent expression for generalised second order servo loops. The denominator of the generalised transfer and error function is usually formulated in terms of the natural resonant frequency ω_n and damping coefficient ζ as

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad \ldots\ldots\ldots 4.96$$

By analogy

$$\omega_n^2 = \frac{K}{\tau_1} \text{ and } 2\zeta\omega_n = (1 + K\tau_2)/\tau_1$$

$$\text{Therefore} \quad \omega_n = \sqrt{\frac{K}{\tau_1}} \text{ and } \zeta = \frac{1}{2} \frac{(1 + K\tau_2)}{\sqrt{K\tau_1}} \qquad \ldots\ldots\ldots 4.97$$

Thus Eqn. 4.95 becomes

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s^2 + \frac{\omega_n^2}{K} s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \ldots\ldots\ldots 4.98$$

The acquisition transient for the case of zero initial phase error can be represented by a frequency step input with $\Phi_1(s) = \frac{\Delta\omega}{s^2}$

Thus

$$\Phi_e(s) = \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2} + \frac{\omega_n^2}{K} \frac{\Delta\omega}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad \ldots\ldots 4.99$$

From which, taking the inverse transform

$$\varphi_e(t) = \frac{\Delta\omega}{K} + \frac{\Delta\omega}{\omega_n} \exp(-\zeta\omega_n t)$$

$$\times \left(\frac{1 - \zeta\omega_n/K}{\sqrt{\zeta^2 - 1}} \sinh \omega_n \sqrt{\zeta^2 - 1}\, t - \frac{\omega_n}{K} \cosh \omega_n \sqrt{\zeta^2 - 1}\, t \right) \quad \ldots 4.100$$

when $\zeta > 1$

$$= \frac{\Delta\omega}{K} + \frac{\Delta\omega}{\omega_n} \exp(-\omega_n t) \left(\omega_n t - \frac{\omega_n^2}{K} t - \frac{\omega_n}{K} \right) \quad \ldots\ldots 4.101$$

when $\zeta = 1$

$$= \frac{\Delta\omega}{K} + \frac{\Delta\omega}{\omega_n} \exp(-\zeta\omega_n t)$$

$$\times \left(\frac{1 - \zeta\omega_n/K}{\sqrt{1 - \zeta^2}} \sin \omega_n \sqrt{1 - \zeta^2}\, t - \frac{\omega_n}{K} \cos \omega_n \sqrt{1 - \zeta^2}\, t \right) \quad \ldots 4.102$$

when $\zeta < 1$

It may be noted immediately that these equations contain an exponentially decaying factor with time constant $1/\omega_n\zeta$, in terms of which the capture transient may be described. Also since

$$\zeta\omega_n = \frac{1 + K\tau_2}{2\tau_1}$$

it may be seen that two time constants are involved in the transient. Since we will normally ensure that $\frac{1}{\tau_1} < \frac{K\tau_2}{\tau_1}$ the longer time constant will be τ_1 and this then indicates the approximate time at which the phase error will be reaching the final value.

Taking the same values of K, $\Delta\omega$, τ_1 and τ_2 used previously we have

$$\omega_n = \sqrt{\frac{K}{\tau_1}} = 4.44 \times 10^7 \text{ rad/s}$$

and $\zeta = 0.743$

The transient of Eqn. 4.102 is shown in Fig. 4.19 which also shows for comparison the equivalent transient for a first order loop with loop gain equal to the high frequency gain of the second order loop i.e. $K_{1st\ order} = 2\pi.10^7 \text{ rad/s}$. It may be seen that the transient of the second order loop initially follows that of the first order, however after $t \approx 1/\omega_n$ the error starts to decrease towards the steady state value.

It may be shown, as demonstrated in the example of Fig. 4.19 that for initial phases within $\pm 30^\circ$, the phase error is within a small fraction (i.e. less than a few degrees) of the final value in a time $t = 6/\omega_n$ secs when $\zeta \sim 1$. Since $\pm 30^\circ$ represents the approximate linear range of a sinusoidal PSD, this time may therefore also be applied to the nonlinear acquisition transient once the phase error

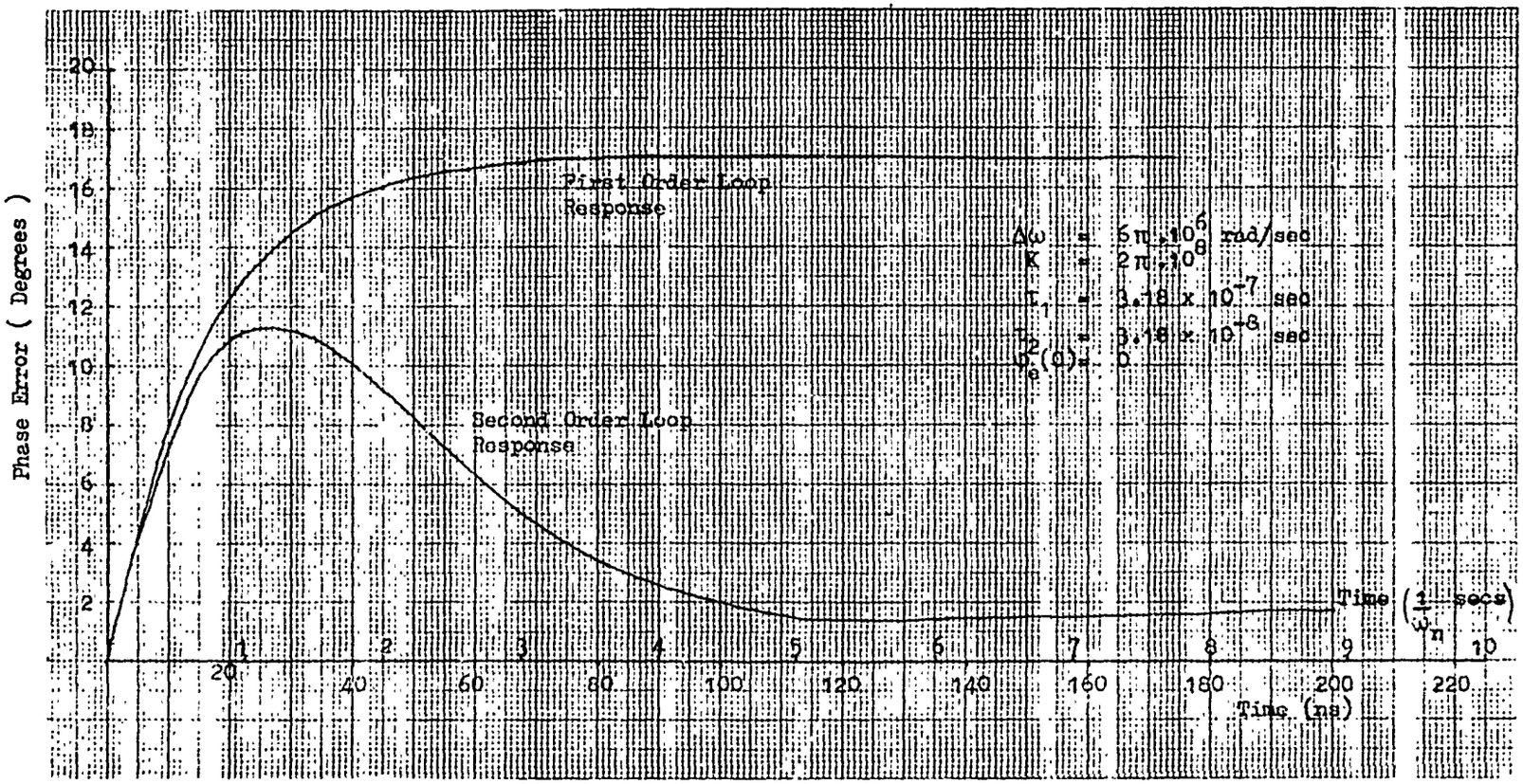


Fig. 4.19 Second Order Loop Phase Transient, Linear PSD

is reduced to the linear region. Allowing, with reference to Fig. 4.18, an additional $4/\omega_n$ secs for the reduction of worst case initial conditions to the linear region gives an approximate time to ensure acquisition of

$$t = \frac{10}{\omega_n} \text{ secs} \qquad \text{.....4.103}$$

This time, although less well specified than that for a first order loop, may be used as a general approximation of the acquisition time and from the time scale given in terms of $1/\omega_n$ it may be seen to be valid for the case represented in Fig. 4.18.

Transient Response Including Linear Frequency Chirp

When chirp of practical pulse oscillators is taken into account, presuming a linear change of frequency through the pulse of slope P rad/s^2 from t = 0, Eqn. 4.29 becomes

$$\frac{d\varphi_2}{dt} = u_2(t)K + P.t$$

and Eqn. 4.79 thus becomes

$$\tau_1 \frac{d^2\varphi_1}{dt^2} + \frac{d\varphi_1}{dt} - P(t + \tau_1) = \tau_1 \frac{d^2\varphi_e}{dt^2} + \frac{d\varphi_e}{dt}\left[1 + K\tau_2\cos\varphi_e\right] + K\sin\varphi_e \qquad \text{.....4.104}$$

When the locking signal is constant, $\frac{d^2\varphi_e}{dt^2} = 0$ and hence

$$\frac{d\varphi_1}{dt} - P(t + \tau_1) = \tau_1 \frac{d^2\varphi_e}{dt^2} + \frac{d\varphi_e}{dt}\left[1 + K\tau_2\cos\varphi_e\right] + K\sin\varphi_e \qquad \text{....4.105}$$

As before, this equation is analytically intractable, but following the approach previously adopted for the first order loop, the linearised equation may be used to indicate the form of the loop response to linear oscillator chirp after the acquisition transient. The linearised error function of the loop is

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s^2 + \frac{\omega_n^2}{K} s}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

and representing the VCO chirp by an equivalent linear variation of the locking signal frequency, the case of a linear chirp slope P rad/s^2 applied at t = 0 with zero initial detuning is given by

$$\Phi_1(s) = \frac{P}{s^3} \qquad \text{.....4.106}$$

Thus

$$\Phi_e(s) = \frac{P}{s^2 + 2\zeta\omega_n s + \omega_n^2} + \frac{P\omega_n^2/K}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad \text{...4.107}$$

Ignoring the transient terms in the solution, which, including an exponential factor $\exp(-\zeta\omega_n t)$ may be assumed to be small after the capture transient, the subsequent response is given by

$$\varphi_e(t) = \frac{P}{\omega_n^2}\left(1 - \frac{2\zeta\omega_n}{K}\right) + \frac{Pt}{K} \qquad \text{...4.108}$$

This may be seen to contain a constant ' tracking ' error and term linearly increasing with time. Taking, for example, the values previously used to obtain Fig. 4.18

i.e. $\omega_n = 4.44 \times 10^7 \text{rad/s}$

$\zeta = 0.743$

$K = 2\pi.10^8 \text{rad/s}$

with $P = 2\pi.5.10^{12}$rad/s (i.e. chirp of 5MHz/μs) a tracking error of 1.426×10^{-2}rad is obtained. The term linearly increasing with time is of the same form as that previously obtained for the first order loop and represents the ' steady state ' phase error for the detuning existing at time t. In the example a phase error of 5×10^{-2}rads is obtained after 1μs.

Response to Pulse Compression Modulations

Consider, as before, phase shift keyed and linear FM modulations applied to the locking signal to increase the transmitted bandwidth.

The form of response of the second order loop to PSK modulation will be similar to that of the first order in that at each phase discontinuity of the input signal, the loop will take a finite time, approximated now by $10/\omega_n$ secs, in which to re-establish the steady state output phase. The finite loop response time will therefore degrade the modulating waveform and also the radiation pattern during the transient. The period $10/\omega_n$ must be therefore short in comparison with the period of the modulation.

The response to linear FM modulation is the same as that given above for a linear frequency chirp. As for the first order loop the limitation on the input frequency variation is determined principally by the phase error introduced by the detuning $\Delta\omega$, when the tracking

error may be ignored, where

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

However, since K for the second order loop will normally be significantly greater than that which may be used in a first order loop, the restriction on the maximum value of $\Delta\omega$ is reduced.

The maximum transmitted bandwidth normally required is 10MHz. It may be seen that taking the value of K previously used ($2\pi.10^8$rad/s) the phase error introduced during the pulse by a linear frequency change of this value is acceptably low, 5.7^o, within the linear range of the PSD.

Summary of the Second Order Loop Behaviour

The second order loop analysis is simplified by taking only the lag-lead filter transfer function to be of practical interest. The use of this filter, shown in Fig. 4.14 overcomes the restriction on loop gain encountered for the first order loop by providing high gain at low frequency, whilst reducing the gain at high frequency to maintain stability.

The phase error due to detuning between the locking signal and the VCO free running frequency (which may be caused by temperature drift, aging , pulsed VCO chirp or intentional linear FM) is given by

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

which is the same expression as obtained for the first order loop. It should be noted, however, that higher values of loop gain K will in general be used in the second order loop, leading to lower phase error.

In addition to the normal capture transient, the second order loop also exhibits a pull-in response in which an oscillator with initial detuning outside the capture range becomes locked via a cycle skipping transient. Acquisition within the capture range, of more interest for rapid synchronisation of pulsed active array sources, may be analysed in specific cases using the phase plane approach to solve the non-linear differential equation. A more general approach using the linearised equation however gives an approximate time to ensure acquisition of

$$t = \frac{10}{\omega_n} \text{ secs}$$

4.2.5 Higher Order Loops

Phase-locked loops of order greater than two are of little interest for the active array application, since even in the ideal case, when no spurious phase shift is introduced into the loop, extreme care must be taken in their design and operation to avoid instability. In practice, when the effects of loop delay are included stable operation is usually only achieved at the expense of the loop capture range and transient performance.

4.2.6 Phase-Locked Loop Stability and the Effect of Loop Delay

Stability of Ideal Loops

The stability of PLLs can be established by means of root locus analysis [42] in which the location in the complex s plane of the poles of H(s) are determined as the loop gain varies. If, for certain values of K, the root locus cuts the imaginary axis and passes into the right hand half-plane, the loop will be unstable for these values. An alternative method of assessing loop stability utilises the Bode diagram to examine the gain of the open loop transfer function when its phase reaches 180° and since this is more illuminating as to the cause of and possible solution to loop instability, it is to be preferred here. Thus plots are made of the magnitude and phase of the openloop transfer function G(s) against frequency. The linearised open loop transfer function of an ideal loop (no amplifier delay, flat amplifier gain) containing a filter with transfer function F(s) is given by

$$G(s) = \frac{AK_1K_2F(s)}{s} \qquad \text{.....4.109}$$

where the denominator represents the integrating action of the VCO. The linearised transfer function is used in stability analysis since the ' gain ' of the PSD in v/rad is greatest in the linear region and hence loop instability will appear in this region first.

The Ideal First Order Loop

A first order loop has no filter and thus $F(s) = 1$. With $s = j\omega$,

Eqn. 4.109 for this case becomes

$$G(j\omega) = \frac{AK_1K_2}{j\omega} \qquad \text{.....4.110}$$

for which

$$\left|G(j\omega)\right| = \frac{AK_1K_2}{\omega} = \frac{K}{\omega} \qquad \text{.....4.111}$$

and

$$\text{Arg}(G(j\omega)) = \tan^{-1}(-\infty) = -\frac{\pi}{2} \text{ rad} \qquad \text{.....4.112}$$

The plots of $\left|G(j\omega)\right|$ and $\text{Arg}(G(j\omega))$ against $\log(\omega)$ are shown in Fig. 4.20 and it may be seen that this loop is unconditionally stable with phase margin (i.e. the difference in phase from 180° at the unity gain frequency) of 90°. It may be noted that the unity gain frequency, given by Eqn. 4.111 as $\omega = K$, also defines the locking range since from Eqn. 4.47 $\Delta\omega_L = K$. For the ideal first order loop K is unrestricted by loop instability. In practice, of course, this loop cannot exist since any practical loop amplifier will introduce delay and eventually a high frequency gain roll-off at some point.

The Ideal Second Order Loop

The ideal second order type two loop results from the use of a flat-gain amplifier with no delay, followed by a passive second order loop filter . The filter transfer function containing only a ' lag term is given by

$$F(s) = \frac{1}{1 + s\tau_1}$$

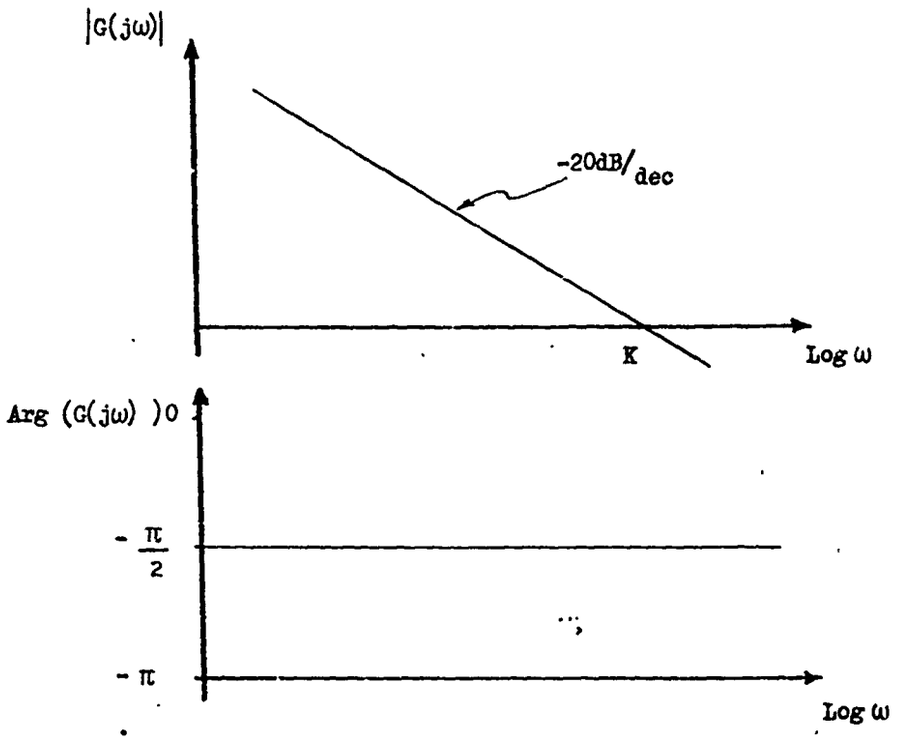


Fig. 4.20 Bode Plot for the First Order Loop

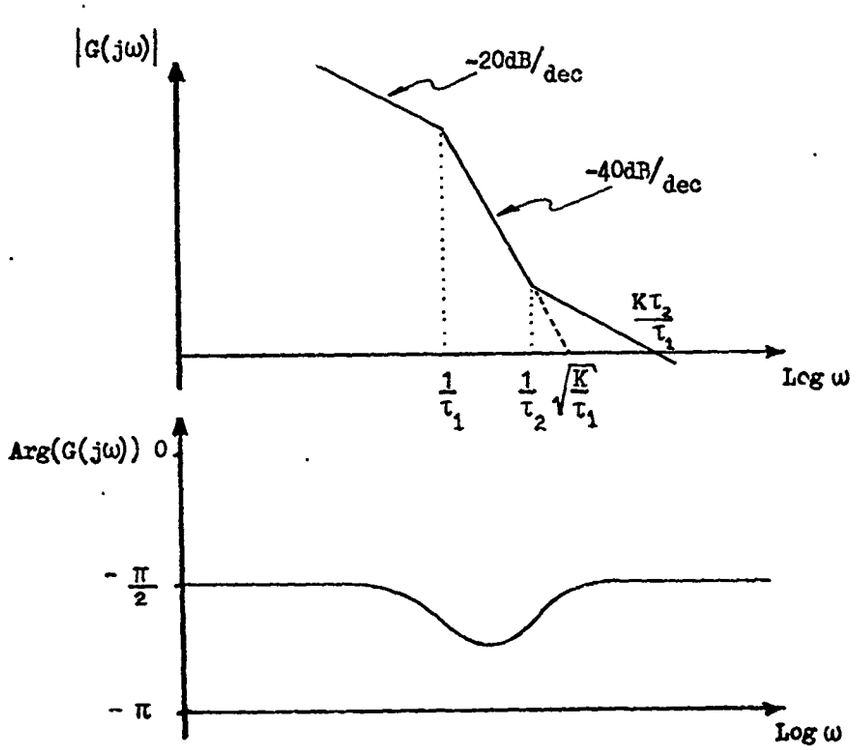


Fig. 4.21 Bode Plot for the Second Order, Type One Loop

and in this case $G(j\omega)$ becomes

$$G(j\omega) = \frac{K}{j\omega(1+ j\omega\tau_1)} \qquad \text{.....4.113}$$

from which it may be seen that at high frequency the phase shift around the loop tends to - 180°. In practice any delay or additional spurious phase shift in the loop can result in instability, and hence loops with this simple lag filter attract little attention.

The ' lag-lead ' filter transfer function

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1}$$

as previously noted is of much more interest. An ideal loop containing this filter response gives

$$G(j\omega) = \frac{K(1+ j\omega\tau_2)}{j\omega(1+ j\omega\tau_1)} \qquad \text{..... ....4.114}$$

therefore

$$|G(j\omega)| = \frac{K}{\omega}\sqrt{\frac{1 + \omega^2\tau_2^2}{1 + \omega^2\tau_1^2}} \qquad \text{.....4.115}$$

and

$$\text{Arg}(G(j\omega)) = \tan^{-1}\left(\frac{1 + \omega^2\tau_1\tau_2}{\omega(\tau_1 - \tau_2)}\right) \qquad \text{..... 4.116}$$

The Bode diagram for this case is shown in Fig. 4.21 and it may be seen that the phase characteristic approaches -180° during the region of rapid amplitude fall, but recovers at high frequency tc give a

phase margin of 90^{o}.

The Effect of Delay on Loop Stability

All realisable PLLs will exhibit a finite delay time around the loop, introduced either by the loop components or simply by the physical length of the loop. That due to the loop length may obviously be reduced by giving careful consideration to layout and in practice it is often the amplifier that is the main contributor to the delay. The type SL541C amplifier used in the experimental work for example has typical delay of ~ 6 ns. When a delay τ_d is included in the loop, the open loop transfer function G(s) becomes

$$G(s) = \frac{AK_1K_2F(s)\exp(-s\tau_d)}{s} \qquad \text{.....4.117}$$

For a first order loop including delay this becomes when $s = j\omega$

$$G(j\omega) = \frac{K\exp(-j\omega\tau_d)}{j\omega} \qquad \text{.....4.118}$$

from which we obtain

$$|G(j\omega)| = \frac{K}{\omega} \qquad \text{.....4.119}$$

$$\text{Arg}(G(j\omega)) = \tan^{-1}(\cot\omega\tau_d) = -\frac{\pi}{2} - \omega\tau_d \qquad \text{.....4.120}$$

It may be noted that

$$\text{Arg}(G(j\omega)) = -\pi$$

when

$$\omega\tau_d = \frac{\pi}{2} \text{ rad}$$

i.e. $$\omega = \frac{\pi}{2\tau_d} \text{ rad/s} \qquad \ldots\ldots\ldots 4.121$$

Thus taking for example the approximate value of τ_d for the SL541C amplifier i.e. τ_d = 6 ns, the 180° phase shift frequency is 2.6×10^8 rad/s (41.67 MHz) and this then is also the maximum value of open loop unity gain frequency and locking range that can be obtained from a first order loop containing this amplifier. In practice other spurious phase shifts and additional delay due to the loop length will combine to further reduce the locking range that may be obtained. It should be noted that amplifiers with lower values of insertion delay can be used to provide larger bandwidths.

The second order open loop transfer function including delay is

$$G(j\omega) = \frac{K(1+ j\omega\tau_2)}{j\omega(1 + j\omega\tau_1)} \exp(-j\omega\tau_d) \qquad \ldots\ldots 4.122$$

where

$$F(j\omega) = \frac{1 + j\omega\tau_2}{1 + j\omega\tau_1}$$

In this case

$$|G(j\omega)| = \frac{K}{\omega}\sqrt{\frac{1 + \omega^2\tau_2^2}{1 + \omega^2\tau_1^2}} \qquad \ldots\ldots 4.123$$

and

$$\text{Arg}(G(j\omega)) = \tan^{-1}\left[\frac{(1+\omega^2\tau_1\tau_2)\cos\omega\tau_d - \omega(\tau_1-\tau_2)\sin\omega\tau_d}{\omega(\tau_1-\tau_2)\cos\omega\tau_d + (1+\omega^2\tau_1\tau_2)\sin\omega\tau_d}\right]$$

...4.124

The Bode diagram describing Eqn. 4.123 and 4.124 is shown in Fig. 4.22. The dashed curve shows the phase shift due to the delay alone i.e. the first order loop response. It may be seen from the diagram that care must now be taken in the choice of τ_1 and τ_2 to ensure that the phase characteristic does not reach -180° at the dip in phase corresponding to the region of rapid gain fall-off in the amplitude response. The maximum frequency at which the phase characteristic can reach -180° can be seen to be that due to the delay alone and thus the maximum bandwidth (= capture range) of the second order loop is restricted to the same value as that for a first order loop. The advantage of the second order loop becomes apparent, however, when considering the loop gain at lower frequencies, since it is this which determines steady state phase error.

The Effect of Delay on Loop Performance

In addition to its effect on loop stability, delay will also influence the transfer function and transient performance of the loop. Since the effect of delay can be neglected at low frequency it is clear that the steady state response of the loop will be unaffected. The behaviour involving the wideband response of the loop will be modified, but since loops will not in general be designed to operate close to instability (i.e. the open loop unit gain frequency will be designed to be significantly less than the maximum value determined above) it would not be expected that the behaviour would be radically different from that given in sections 4.2.3 and 4.2.4. It should be

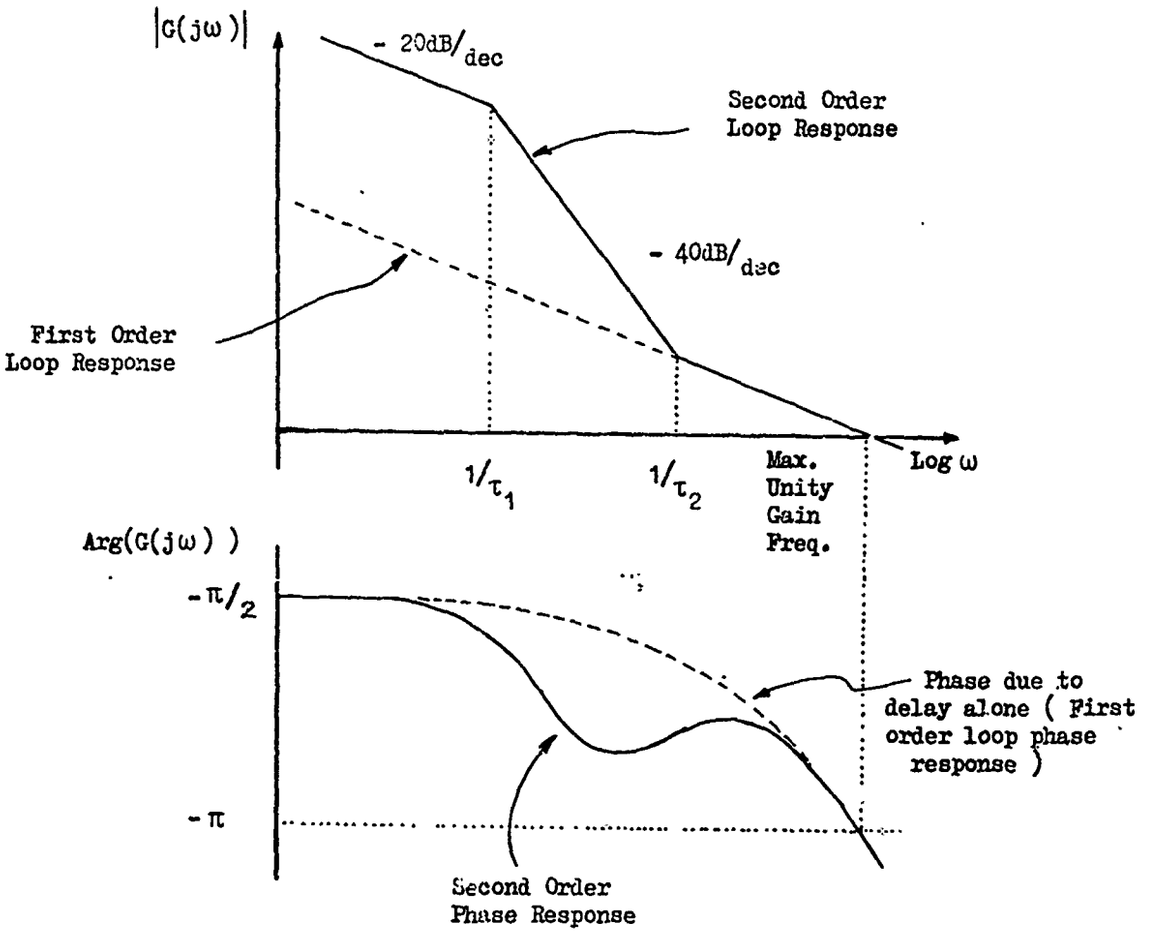


Fig. 4.22 Bode Diagram for First and Second Order Loops Including Delay

noted, however, that if an exact description of the loop transient performance is required, the modified equations including delay should be used in the loop analysis. These are developed below simply for reference.

Consider then a delay τ_d introduced by the loop amplifier. Following the derivation of the loop equations previously given in section 4.2.1 the output of the PSD is

$$u_1(t) = K_1 \sin(\varphi_1(t) - \varphi_2(t))$$

For a first order loop the filter is omitted and the output of the amplifier is

$$u_2(t) = AK_1 \sin\left[\varphi_1(t - \tau_d) - \varphi_2(t - \tau_d)\right] \qquad \text{.....4.125}$$

Since $\dfrac{d\varphi_2(t)}{dt} = K_2 u_2(t)$

we have

$$\frac{d\varphi_2(t)}{dt} = K \sin\left[\varphi_1(t - \tau_d) - \varphi_2(t - \tau_d)\right] \qquad \text{.....4.126}$$

which is the loop differential equation including delay. In the linear region of the PSD, this simplifies to

$$\frac{d\varphi_2(t)}{dt} = K\left[\varphi_1(t - \tau_d) - \varphi_2(t - \tau_d)\right] \qquad \text{.....4.127}$$

Transforming into the frequency domain this becomes

$$\Phi_2(s) = \left[\Phi_1(s)\exp(-s\tau_d) - \Phi_2(s)\exp(-s\tau_d)\right] K$$

and the loop transfer function is then

$$H(s) = \frac{\Phi_2(s)}{\Phi_1(s)} = \frac{K\exp(-s\tau_d)}{s + K\exp(-s\tau_d)} \qquad \ldots\ldots 4.128$$

The equivalent time domain equation for other loops is

$$\frac{d\varphi_2}{dt} = K\sin\left[\varphi_1(t-\tau_d) - \varphi_2(t-\tau_d)\right] * f(t) \qquad \ldots\ldots 4.129$$

where, as previously, f(t) is the impulse response of the filter and * denotes convolution. The transfer function, similarly, is

$$H(s) = \frac{\Phi_2(s)}{\Phi_1(s)} = \frac{KF(s)\exp(-s\tau_d)}{s + KF(s)\exp(-s\tau_d)} \qquad \ldots\ldots\ldots 4.130$$

4.2.7 Noise Performance

A detailed analysis of the noise performance of the PLL is given elsewhere [66], but several points indicative of the form of the noise performance are considered in the following.

It was previously noted in the discussion of the noise performance of injection locked oscillators that solid state microwave oscillators usually exhibit a high level of output noise power relative to an upconverted signal from a stable low frequency source. Thus the expected situation will again be that of a ' quiet ' locking signal synchronising a ' noisy ' VCO.

Amplitude Modulated Noise

A PLL with ideal PSD in which the output voltage is only related to the phase of the inputs will be unaffected by AM noise; the AM noise output of the VCO will be the same as that of the unlocked oscillator; AM noise present on the locking signal will have no effect on the VCO output. Practical mixer PSDs are, however, based on a multiplication of the input signal for their operation, and the mixer output power at the desired difference frequency will be a function of the input signal powers. AM noise present at the mixer inputs will therefore produce variations in the PSD characteristic K_1 (volts/rad) and thus lead via Eqn. 4.48 to a varying phase error. In general therefore, although the inherent AM noise of the VCO will be essentially unaffected by the PLL, for frequency components within the loop bandwidth, given approximately by the locking range for a first order loop and by the capture range for a second order loop, there will be some degree of AM to FM conversion resulting from AM noise components appearing at the PSD. AM noise sidebands present on the locking signal will produce FM noise sidebands at equivalent frequencies on the VCO output; AM noise sidebands existing on the VCO output will produce correlated FM sidebands at the same ' modulation ' frequencies. The AM- FM conversion may be minimized, and in practice brought down to low levels, by operating diode mixer PSDs in the saturated region, i.e. with input power levels greater than a few mWs, for which the variation in output voltage with input power is small. The variation of PSD output power with the input signal level is described further in section 4.2.11.

Frequency Modulated Noise

The effect of the PLL on the FM noise characteristics of the VCO can be obtained from the following simple argument.

If initially the case of a ' quiet ' VCO and a locking signal accompanied by FM noise is considered, it would be expected that each component of the input noise spectrum, at frequency f_m from the centre frequency, will modulate the VCO such that the input and output components of the noise at modulating frequency f_m, will be related by the loop transfer function, i.e. slowly varying components of the noise will be reproduced on the VCO output, whilst high frequency components of the noise will be outside the loop bandwidth and will only appear in attenuated form.

If the same noise spectrum is now considered to be present on the VCO output, with the locking signal now ' quiet ', it may be seen that without feedback around the loop the same magnitude of output voltage as before will be obtained from the PSD. However, when the loop is closed it may be considered in a simple approximation that this voltage will produce VCO modulation that will cancel (since the loop has negative feedback) the original components of the noise signal. The degree of cancellation is then given by the error function of the loop, which for a linear phase detector is

$$\frac{\Phi_e(s)}{\Phi_1(s)} = \frac{s}{s + KF(s)}$$

ignoring loop delay. The form of this is shown in Fig. 4.23, from which it would be expected that nearly complete cancellation of the

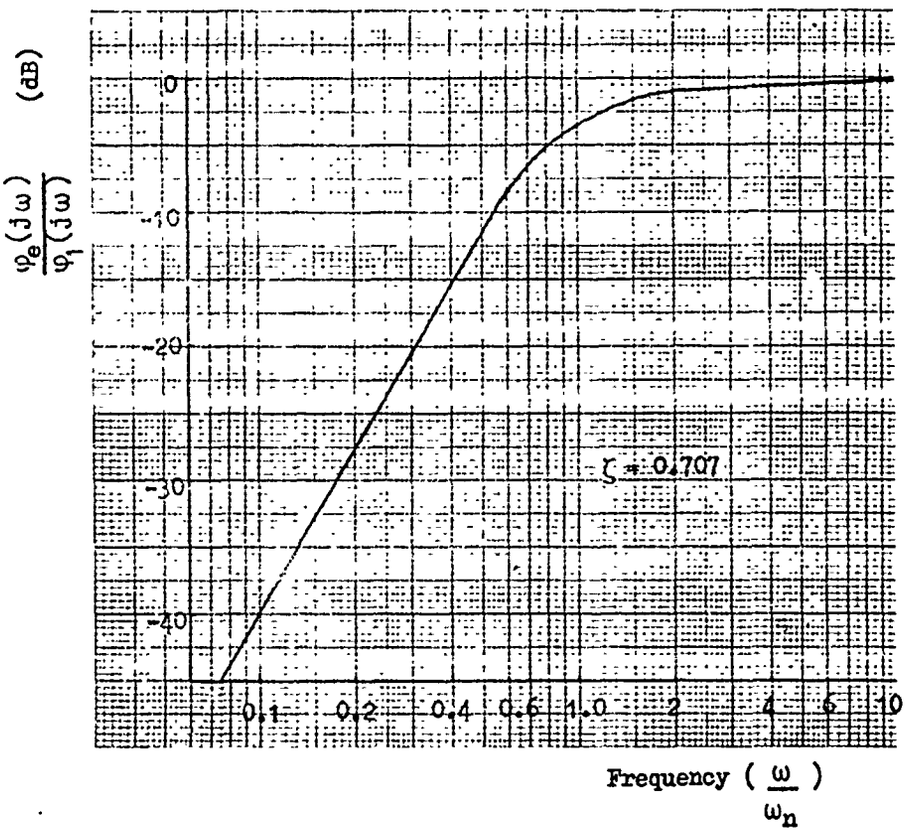


Fig. 4.23 Error Function for a Second Order Loop.

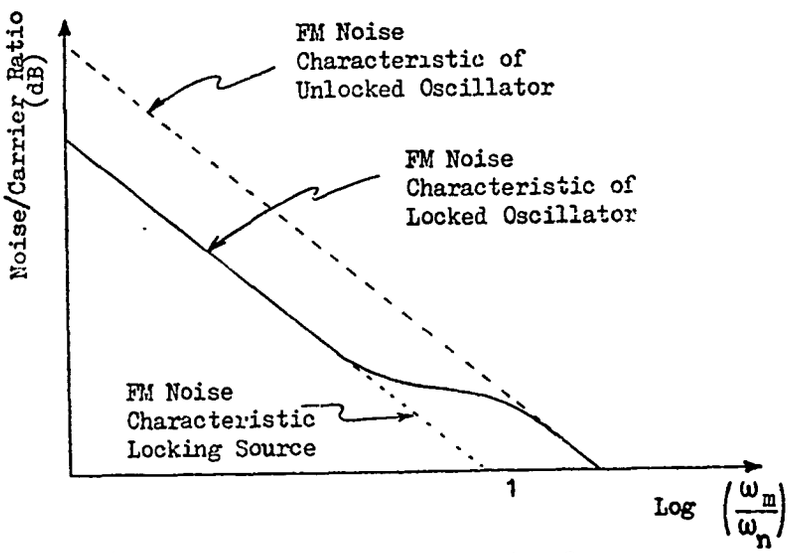


Fig. 4.24 Generalised FM Noise Characteristic of Locked Oscillator

FM noise will occur for the slowly varying components, whilst those at modulation frequencies $> \omega_n$ will be unaffected by the loop.

The form of the relationship between FM noise sideband power level and the ' modulation ' frequency will thus be similar to that shown in Fig. 4.24. At frequencies close to the carrier the FM noise level will closely follow that of the reference source, whilst for frequencies greater than ω_n the noise level will be essentially that of the unlocked oscillator. This result is similar to that obtained for injection locking, as described by Eqn. 4.26.

Additional Sources of Noise within the Loop

As described above, in the absence of additional sources of noise, the VCO will take on the FM noise characteristics of the locking source close to the carrier. Noise voltages introduced within the loop by practical PSDs and loop amplifiers will however produce an additional frequency modulation on the VCO output. Resulting from the loop negative feedback, any noise voltage introduced by the PSD or loop amplifier appearing at the VCO frequency control terminal will produce a phase error on the output, with sign and amplitude that will restore the voltage applied to the VCO to the original level required to maintain lock. If the noise voltage referred to the PSD output is $+ \delta u_1$, from Eqn. 4.31 the additional phase error produced on the VCO output, within the PSD linear range will be

$$\varphi_e = -\frac{\delta u_1}{K_1} \qquad \text{.....4.131}$$

The FM noise output of the VCO may thus be greater than that predicted

from the above argument, however, it may be noted that the additional FM noise so produced on the individual outputs of an array of locked oscillators will not be correlated, and as discussed in Chapter 5, will not therefore be transmitted with the full gain of the array. A more detailed analysis of the effect of noise voltages appearing within the loop is given by Blanchard[39].

4.2.8 Comparison of the First and Second Order Loops

It was noted in sections 4.2.3 and 4.2.4 that a phase error introduced by the PLL by detuning $\Delta\omega$ between the locking signal and the free running frequency of the VCO, caused by temperature drift, aging, pulsed VCO chirp or intentional linear FM is given by

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{K}\right)$$

To ensure low phase error it is therefore desirable to use a high value of loop gain $K = K_1K_2A$. However, as shown in section 4.2.6, the maximum value of open loop unity gain frequency is limited in practical loops in which delay is present. If ω_π is the angular frequency giving 180° phase shift around the loop, the maximum value of K for stable operation with the first order loop is given by

$$K = \omega_\pi \qquad \text{.....4.132}$$

It may be noted, refering to its introduction at Eqn. 4.34, that the dimensions of K are sec^{-1}. Similarly for the second order loop we have, when $\frac{1}{\tau_2} < \omega_\pi$

$$K \frac{\tau_2}{\tau_1} \approx \omega_\pi \qquad \text{..... 4.133}$$

giving

$$K \approx \omega_\pi \frac{\tau_1}{\tau_2} \qquad \text{.....4.134}$$

and since we may choose $\frac{\tau_1}{\tau_2} >> 1$

it may be seen that higher values of K, and thus lower phase errors may be obtained with the second order loop.

Using the above restriction on high frequency loop gain it may be seen that the capture range for both first and second order loops is limited to a maximum of ω_π

The acquisition time, being the time required to ensure that the VCO is within a few degrees of the steady state value for the great majority of initial phases is given, for the first order loop by

$$t = \frac{10}{K}$$

and for the second order loop by

$$t = \frac{10}{\omega_n}$$

where ω_n, the loop natural resonant frequency, was defined in Eqn. 4.97.

Acquisition times short compared with the pulse lengths typically

used in active array radar (1 - 20μs) may be achieved for both first and second order loops in practice, and since phase errors are significantly less for the latter, the second order loop is to be preferred.

Where it is desired to modulate the transmitted pulse for the application of pulse compression techniques, linear FM appears to be the most suitable modulation since the high loop gain will ensure low variation of phase error through the pulse; a phase shift keyed modulation will be distorted by the loop transient at each phase discontinuity.

Summarizing the relative performance of the second order PLL with that of injection locking, it was previously shown that a large locking range, and thus low phase errors were only obtainable with injection locking at the expense of locking gain; several stages of injection locked amplification may, in practice , be required. The PLL offers potentially high gain within a single stage since the locking range is not directly related to locking gain when a saturated PSD is used. Furthermore particularly low values of phase error may be achieved with the second order loop.

The relative performance that can be obtained from injection locking, the first order and the second order PLL is illustrated by the following example. A voltage controlled oscillator of similar characteristics to that used experimentally (a varactor tuned Gunn oscillator) is considered, with :

free running frequency = 10GHz

locking Q factor = 100

tuning sensitivity K_2 = $2\pi.10^7$ rads/v.s

A PSD operated in the saturated region is assumed with typical gain K_1 of 0.3 v/rad. The internal delay of a typical loop amplifier is assumed to be 4ns.

Table 4.1 shows the locking characteristics for the three cases (given for convenience in terms of frequency (Hz)) assuming :

(a) a minimum locking gain of 10dB is required when the oscillator is injection locked, yielding a locking range from Eqn. 4.3 of 1.98×10^8 rad/s.

(b) the amplifier gain in the case of the phase locked loop is taken as the maximum value determined by Eqns. 4.132 and 4.134. In practice this would be reduced by a safety margin to ensure stability.

(c) the PLL acquisition times are the approximate values obtained ignoring loop delay.

Phase Error Comparison

It may be seen from the table that for either injection locking or the 1st order loop, close control of the detuning will be required to constrain the phase error in the presence of temperature change, frequency chirp etc. Temperature drift of the free running frequency alone (typically 0.5 MHz/^{o}C for the oscillator under consideration) may produce serious phase error, although it must be noted that it is the differential phase error between array antenna elements that is of importance; temperature drift will tend to produce similar phase errors in all elements. The second order loop produces significantly lower phase error for a given detuning and restrictions on drift of the free running frequency will thus be considerably less severe. Similarly the within-pulse variation of phase error

	FIRST ORDER PLL	INJECTION LOCKING $\frac{Pout}{Pin}$ = 10dB	SECOND ORDER PLL
LOCKING RANGE $\frac{\Delta\omega_L}{2\pi}$	62.5MHz	31.5MHz	625MHz
CAPTURE RANGE $\frac{\Delta\omega_e}{2\pi}$	62.5MHz	31.5MHz	$\sim$ 62.5MHz
SYNCHRONISATION RANGE $\frac{\Delta\omega_s}{2\pi}$	125MHz	63MHz	1250MHz
ACQUISITION TIME	25.6ns	$\sim$ 5ns (estimate)	63.6ns
MAX. DETUNING FOR $\lvert\varphi_e\rvert < 10^\circ$	$\pm$ 10.8MHz	$\pm$ 5.46MHz	$\pm$ 108MHz
PHASE ERROR VARIATION WITHIN 5MHz CHIRP OR LINEAR FM (LINEAR PSD)	4.6°	9.1°	0.46°

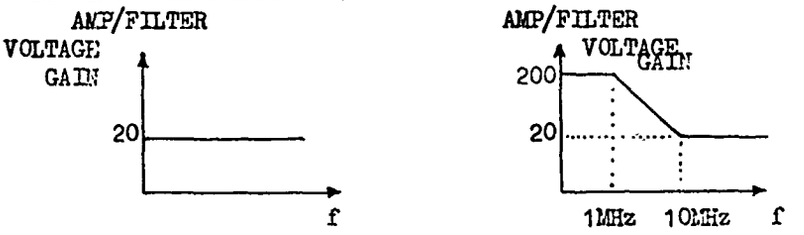


Table 4.1 Comparison of Locking Behaviour of Injection Locking and First and Second Order PLLs

due to chirp or linear FM is significantly reduced with the second order loop.

Acquisition Comparison

As previously described in section 4.1, injection locking acquisition times are significantly less than that predicted by simple theory based on the transient solution to Eqn. 4.1. An estimated acquisition time equal to the inverse of the locking range $\Delta\omega_L$ is given in the table. The acquisition time for the second order loop is longer than that for the first order, but this represents the time required to establish a significantly lower phase error. The phase error will be reduced to that of the first order loop in a time significantly less than that shown.

The acquisition time must be short relative to the pulse length; typically, acquisition in just under 100ns will be adequate for a 1μs pulse. Since pulse lengths used in solid state radar are relatively long (typically 1 - 20μs) it may be seen that the acquisition performance in all three cases is adequate. The effect of the phase transient during the acquisition time on the array radiated output is discussed further in Chapter 5.

4.2.9 The Heterodyne Loop

A configuration of the PLL of particular interest for subsequent active element design is shown in Fig. 4.25. The sample of the VCO output is here heterodyned to a lower frequency before being applied to the PSD, such that lock is achieved when the downconverted signal and locking signal applied to the PSD are of the same frequency. The VCO may thus be synchronised to either the sum or difference of the input frequencies, although in practice care is taken to ensure that the VCO can lock to only one of these to avoid ambiguity (for instance by restricting the VCO tuning range).

The equivalence of the operation of the heterodyne loop with that of the simpler loop previously considered is simply demonstrated in the following. The signal obtained at the output of the bandpass filter centred on the angular frequency $(\omega_2 - \omega_3)$ following the downconverting mixer is

$$v_4(t) = V_4 \sin\left[(\omega_2 - \omega_3)t + \varphi_2 - \varphi_3\right] \qquad \text{.....4.135}$$

The output of the PSD to which this signal is applied, along with the second locking signal

$$v_5(t) = V_5 \cos(\omega_5 t + \varphi_5)$$

is given by

$$u_1(t) = K_1 \sin\left[(\omega_2 - \omega_3 - \omega_5)t + \varphi_2 - \varphi_3 - \varphi_5\right] \qquad \text{.....4.136}$$

where K_1 is the PSD gain in v/rad. If the loop filter impulse

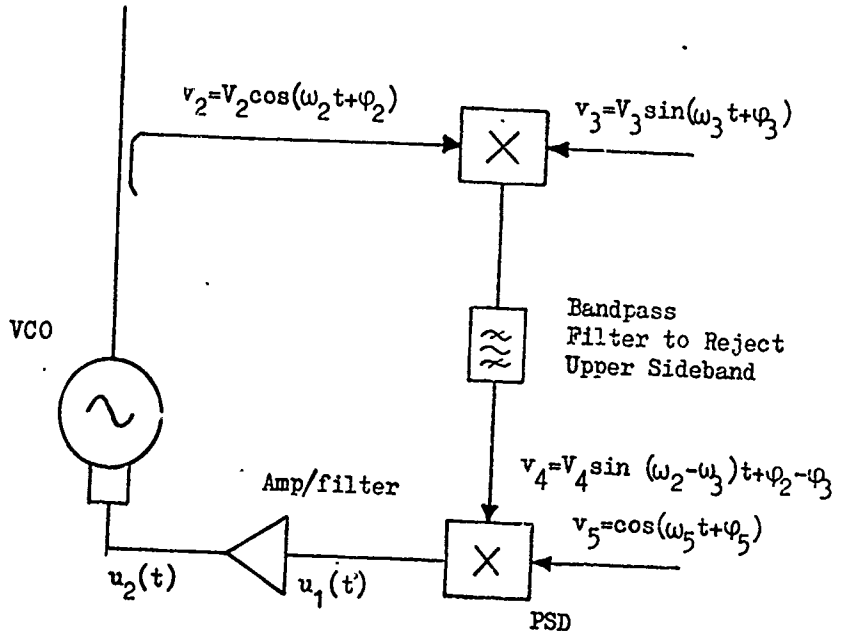


Fig. 4.25 The Heterodyne Loop

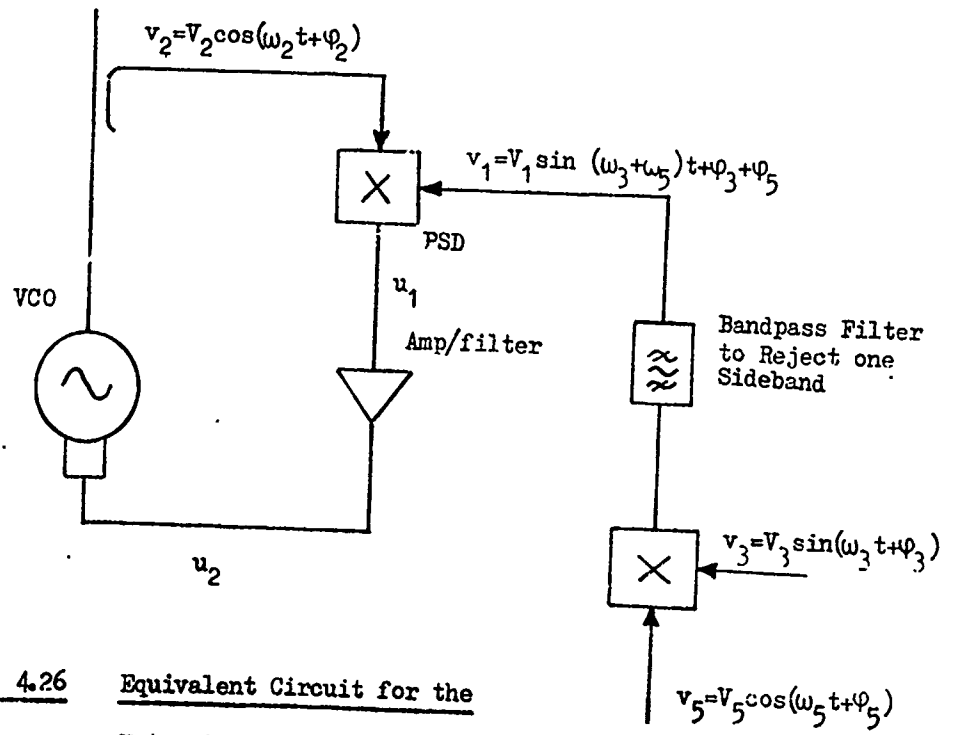


Fig. 4.26 Equivalent Circuit for the Heterodyne Loop

response is f(t) we have, in line with the previous analysis

$$u_2(t) = u_1(t) * f(t) \qquad \ldots\ldots\ldots 4.137$$

and also

$$\frac{d\varphi_1(t)}{dt} = K_2 u_2 \qquad \ldots\ldots\ldots 4.138$$

Eqns. 4.136, 4.137 and 4.138 are similar, however, to those obtained from the circuit of Fig. 4.26 containing a conventional PLL. For this circuit the signal $v_1(t)$ applied to the PSD is

$$v_1(t) = V_1 \sin\left[(\omega_3 + \omega_5)t + \varphi_3 + \varphi_5\right] \qquad \ldots\ldots\ldots 4.139$$

and the phase detector output is

$$u_1(t) = K_1 \sin\left[(\omega_2 - \omega_3 - \omega_5)t + \varphi_2 - \varphi_3 - \varphi_5\right] \qquad \ldots\ldots 4.140$$

assuming the same PSD sensitivity K_1.
As before we have

$$u_2(t) = u_1(t) * f(t) \qquad \ldots\ldots 4.141$$

and

$$\frac{d\varphi_1}{dt} = K_2 u_2(t) \qquad \ldots\ldots 4.142$$

Since the circuits of Figs. 4.25 and 4.26 are described by the same equations, their performance will be equivalent, and thus the theory

previously derived for the conventional PLL may also be applied to the heterodyne loop.

The attraction of the heterodyne loop results from the fact that the VCO output phase is determined by the phase of both input signals, irrespective of their frequencies. If ω_3 is a microwave and ω_5 an intermediate frequency, the phase of the microwave output may therefore be simply controlled via the intermediate frequency input. This feature is used in subsequent active element designs to avoid the conventional microwave phase shifter, which often represents a large part of the element cost.

It may be noted that for VCO synchronisation to the sum of the input frequencies, a phase shift $+\varphi$ on the i.f. input will produce a shift $+\varphi$ on the VCO output. However, with synchronisation to the difference frequency a sign change will be introduced in the downconversion of the feedback signal, resulting in an output phase change $-\varphi$ for an input shift of $+\varphi$.

Several factors influence the choice of value of intermediate frequency ω_5 to be used in conjunction with the heterodyne loop.

1) As mentioned above, the heterodyne loop (HPLL) allows phase shifting of the microwave output to be achieved via an i.f. phase shifter placed in the i.f. input to the loop. However even at i.f., phase shifter and distribution network design and construction are simplified at lower frequencies. In this respect a low i.f. is therefore preferable.

2) The heterodyne loop may theoretically be locked with an output frequency equal to either the sum or difference of the input

frequencies. To avoid ambiguity it will therefore be necessary to constrain the tuning range of the VCO in practice to ensure that lock to only one of these frequencies is possible. A value of i.f. must therefore be chosen that will give sufficient separation of the sum and difference frequencies for this to be achieved.

3) Practical mixer PSDs inevitably have some degree of leakage of the input frequencies present on the output. In order to avoid modulating the VCO output at the i.f. frequency, a value of i.f. outside the pass-band of practical loop amplifiers and filters will therefore be chosen.

In practice the constraints given by 2) and 3) above result in a choice of i.f. of the order of 100MHz. In the experimental work subsequently described using HPLLs, an i.f. of 60MHz was generally employed since particularly large loop bandwidths were not used.

Finally in this section it must be noted that for stable operation, care must be taken to avoid the introduction of extra delay around the loop with the additional downconversion of the HPLL.

4.2.10 Phase Locked Loop Components

A brief discussion is given of some of the characteristics and limitations of practical VCOs and PSDs.

Voltage Controlled Oscillators

With the exception of magnetic tuning e.g. YIG tuned oscillators for which tuning rates are low (typically modulation frequencies only up to 1MHz are used) electronic tuning of solid state sources

is usually achieved with varactors. The varactor introduces a variable reactance into the source resonant circuit, producing electronic control of the resonant frequency. An approximate equivalent circuit for a diode oscillator is given in Fig. 4.27. The tuning bandwidth that may be obtained depends upon the maximum change in varactor capacitance with voltage, the degree of coupling between the varactor and the cavity, and the loaded Q factor, Q_L, of the cavity. An approximate expression for the tuning range is(43)

$$\Delta f \approx \frac{(C_{jmax} - C_{jo})V^2\pi f^2}{Q_L P_T} \qquad \ldots\ldots\ldots 4.143$$

where Δf is the tuning range in Hz

C_{jmax} is the varactor junction capacitance at breakdown

C_{jo} is the varactor junction capacitance at zero bias

V is the RF voltage swing at the varactor junction

f is the operating frequency

Q_L is loaded Q factor

and P_T is the total power dissipated in the varactor and circuit elements.

To obtain a large tuning range for the PLL application, it would therefore be expected that a varactor with large capacitance variation and low loss, tightly coupled to the cavity to increase V, and a low Q_L cavity would be used. In practice, however, there are several restrictions :

(a) one of the reasons for requiring a large PLL locking range is that practical solid state oscillators are subject to drift of the free running frequency. The magnitude of the drift is ,

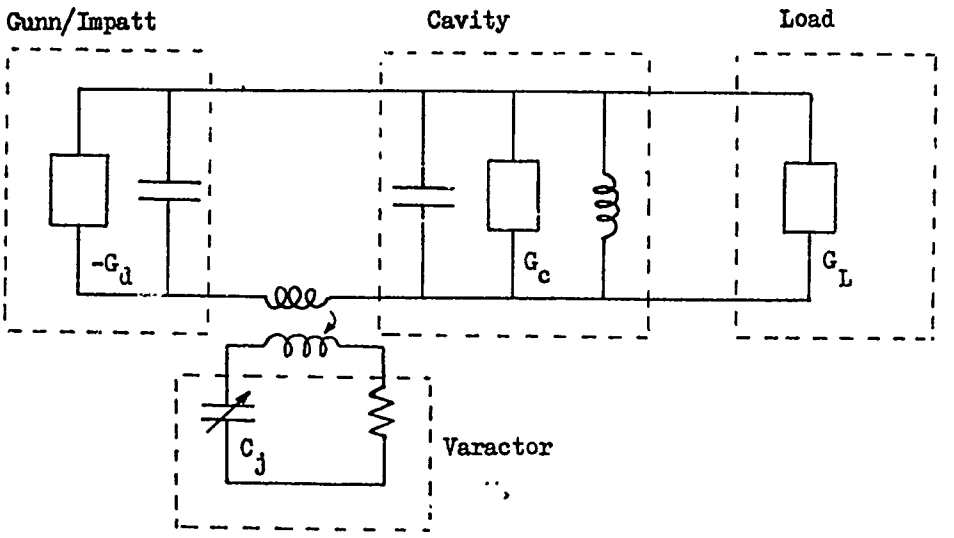


Fig. 4.27 Simple Equivalent Circuit for a Varactor Tuned Oscillator

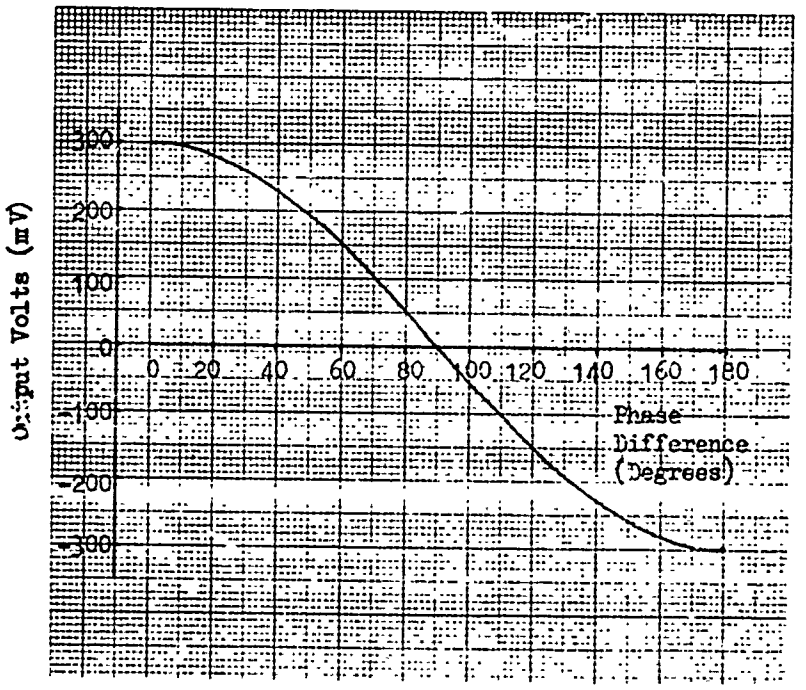


Fig. 4.28 PSD Characteristic

however, inversely related to the Q_L of the oscillator cavity and thus there is little to be gained by reducing this quantity. In fact if an adequate PLL locking range can be achieved, it is preferable to use a high Q_L to reduce drift and chirp.

(b) under higher power operation (e.g. tens of Watts) the RF voltage swing at the varactor can cause large rectified currents to flow at zero bias. The range of bias voltage and hence the tuning range is therefore restricted at higher power levels.

At low power (e.g. less than a few hundred mWs.) tuning bandwidths of 10% may be readily obtained. At higher power tuning ranges of some tens of MHz has been quoted for a 10W pulsed Gunn source. Transistor sources in which the resonant circuit voltage is less than that of the output may be expected to provide higher tuning ranges for higher power operation.

The variation in the VCO frequency is approximately proportional to the square root of the bias voltage. The VCO tuning sensitivity K_1 previously considered to be linear in the PLL analysis is therefore non-linear in this case. However, when the loop bandwidth, given by the capture range, is small in comparison to the VCO tuning range the deviation from linearity within this bandwidth is small over most of the tuning characteristic.

One other characteristic to be mentioned regarding practical VCOs is ' post tuning drift ', which is a relatively slow drift in frequency of an unlocked VCO after the application of a sudden voltage step to the varactor. Typically the post tuning drift extends up to several ms after the application of the tuning voltage before the output frequency settles to a steady value. The primary reason

for this effect is a thermal one[44]; a significant retuning of the oscillator to a frequency producing a different oscillator output power will change the thermal dissipation in both the oscillator generating diode or transistor and the varactor. The frequency thus subsequently changes until a thermal equilibrium is re-established.

Post tuning drift has not been considered in the previous transient analysis of PLL behaviour since the thermally induced frequency change of a pulsed oscillator has been already described in the context of chirp, and within-pulse frequency changes that may be applied for pulse compression are not in practice sufficiently great to markedly alter the thermal dissipation.

Phase Sensitive Detectors

Fig. 4.28 shows a quoted[45] DC output voltage against relative phase for a double-balanced mixer PSD with both input signal levels equal to 5mW. As previously noted the output voltage is zero when the input signals are in quadrature. The slope of the characteristic within the ' linear region ' (i.e. $90 \pm 30^{\circ}$) is

$$K_1 = \frac{150\text{mV}}{30^{\circ}} \times \frac{360}{2\pi} = 0.286 \text{ V/rad}$$

The DC offset voltage, which is simply due to rectification and is not dependent on phase, is quoted as 1mV. This offset, the magnitude of which is related to the input powers, produces a constant frequency offset on the VCO which can subsequently result in a fixed phase error on the output. However it was previously noted that the tuning range of practical VCOs is not linear, and it will be necessary in practice

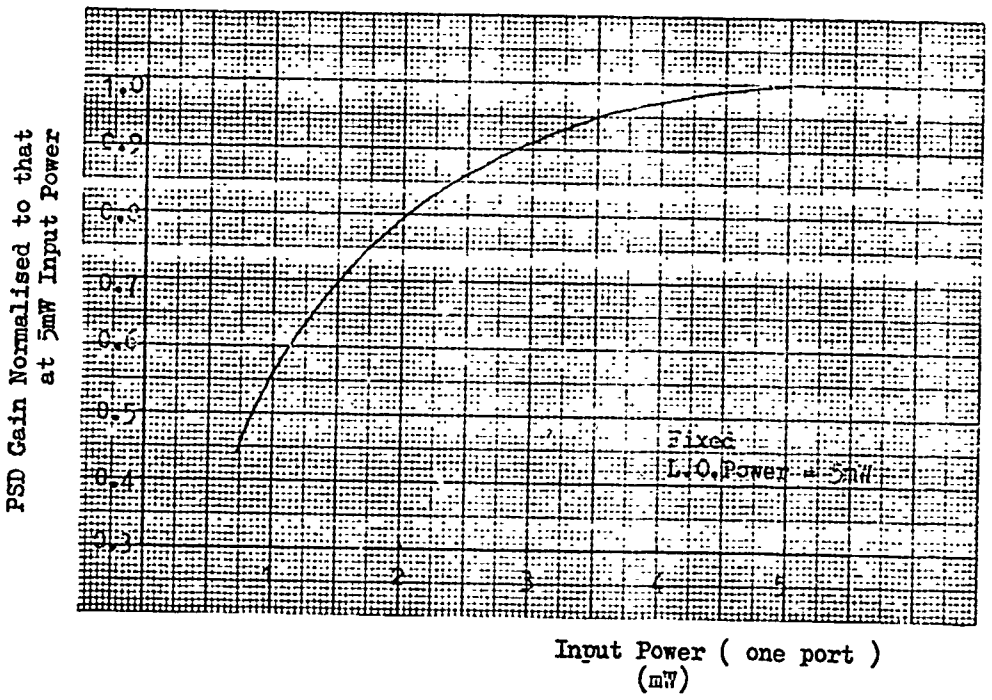


Fig. 4.29 PSD Gain Variation With Input Power of One Port.

to apply a standing voltage to the varactor of the VCO to bias it into a linear part of its tuning range. The standing varactor voltage will then determine the desired free-running frequency. The offset voltage of practical PSDs may therefore be included in the standing bias voltage.

PSDs are normally operated with input powers sufficient to drive the mixer into the ' saturated ' region. This provides a relatively high value for K_1 and also provides some rejection of AM - FM noise conversion. The variation of K_1 with power of one input, with the other fixed at 5mW, is shown in Fig. 4.29. The PSD gain is shown normalised to that obtained with both input powers at 5mW. This characteristic was obtained experimentally from a type EM36A X band mixer (Lorch Devices Inc.) at 10.4GHz. It may be seen that with both input powers ~5mW, there is little variation of K_1 for small changes of input level. It is therefore advisable to operate the PSD at this power level.

4.2.11 Experimental Results

Experiments were conducted with the aim of demonstrating the application of the theory to the synchronisation of practical microwave sources. In particular it was desired to check the validity of the acquisition time approximations, the use of the second order loop to reduce phase error, and the operation of the heterodyne loop. Attention was not given to the provision of particularly large loop bandwidth.

The VCO used in the experiments was a varactor tuned, waveguide Gunn oscillator (AEI type DA8825G) designed for CW operation and

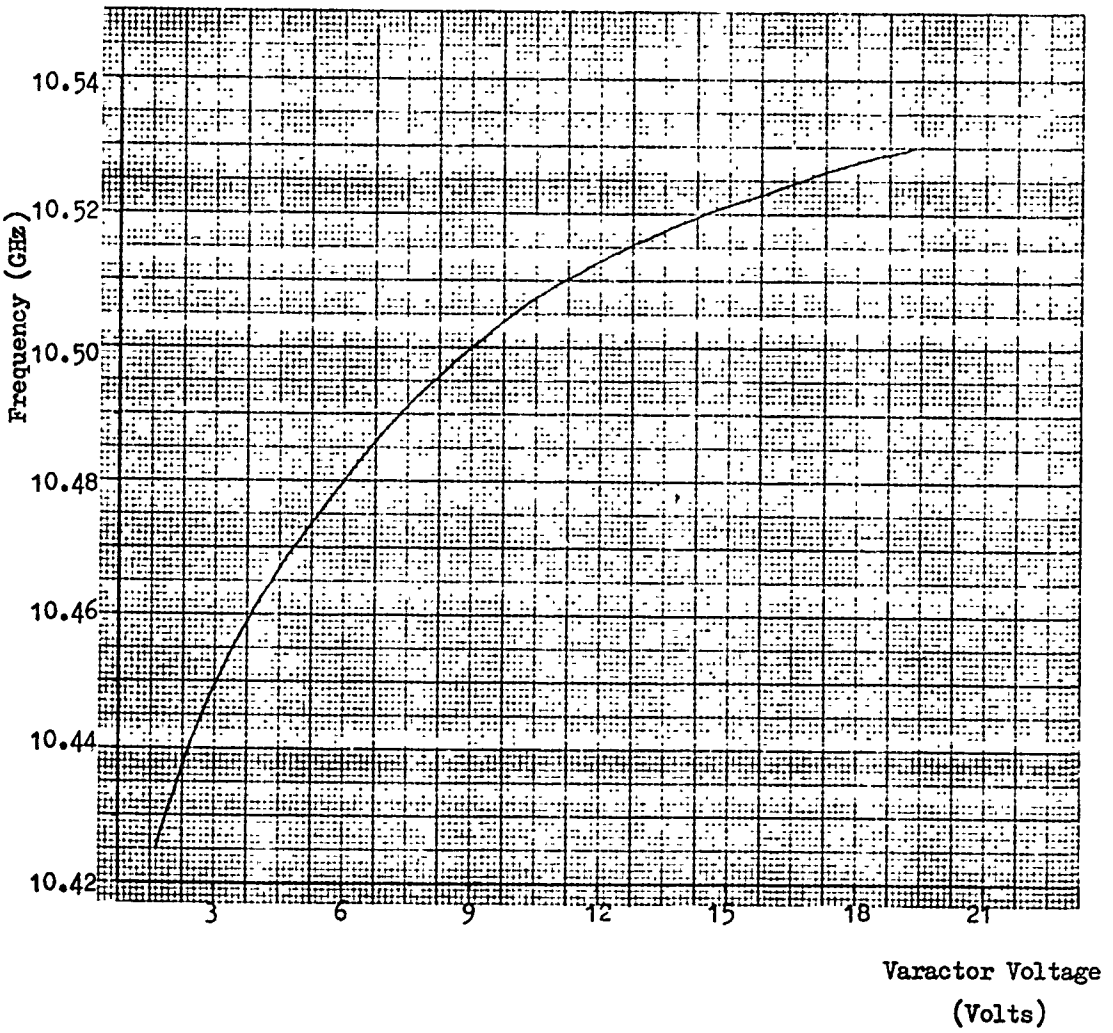


Fig. 4.30 Varactor Tuning Characteristic

for a Type DA8825G Oscillator

producing 150mW CW at 10.5GHz. The CW electronic tuning range was approximately 130MHz for a varactor bias voltage range of 1.5 - 20V. The tuning characteristic for one oscillator is shown in Fig. 4.30.

A heterodyne PLL was set up as shown in Fig. 4.31 with locking signal frequencies chosen to allow synchronisation of the VCO to the sum frequency. Following the PSD a wideband operational amplifier (type SL 541C) was used to provide both amplification and filtering; the figure shows an amplifier configuration producing a second order loop. To avoid the more severe tuning non-linearity at low values of varactor bias voltage a fixed offset voltage of $\sim$6V was applied to the varactor, about which the loop feedback voltage would vary. With an offset voltage applied, approximately linear tuning of 8MHz/v was obtained over some tens of MHz. For CW operation advantage was taken of the high input impedance of the varactor ($\sim$ 1MΩ) and the low output impedance ($\sim$ several Ωs) of the amplifier to avoid a DC level shifting circuit. (Ideally the operational amplifier would be used to provide a DC level shift but the output voltage swing of the SL541C was insufficient for this purpose.) With $R_5 \gg R_4$ little of the amplifier output voltage is dropped across R_5 ; with $R_4 \gg R_0$, where R_0 is the amplifier output impedance, little of the offset voltage appears at the amplifier output. For pulsed operation the amplifier may simply be capacitively coupled to the varactor.

Initial experiments were confined to CW operation of the VCO. With R_3 and C_1 removed, R_1 and R_2 were chosen to provide an amplifier voltage gain of 10, resulting in a first order loop. The VCO was locked to the sum of input frequencies 10.38GHz and 100MHz. The locking range was measured to be $\approx$ 7MHz, in agreement with that

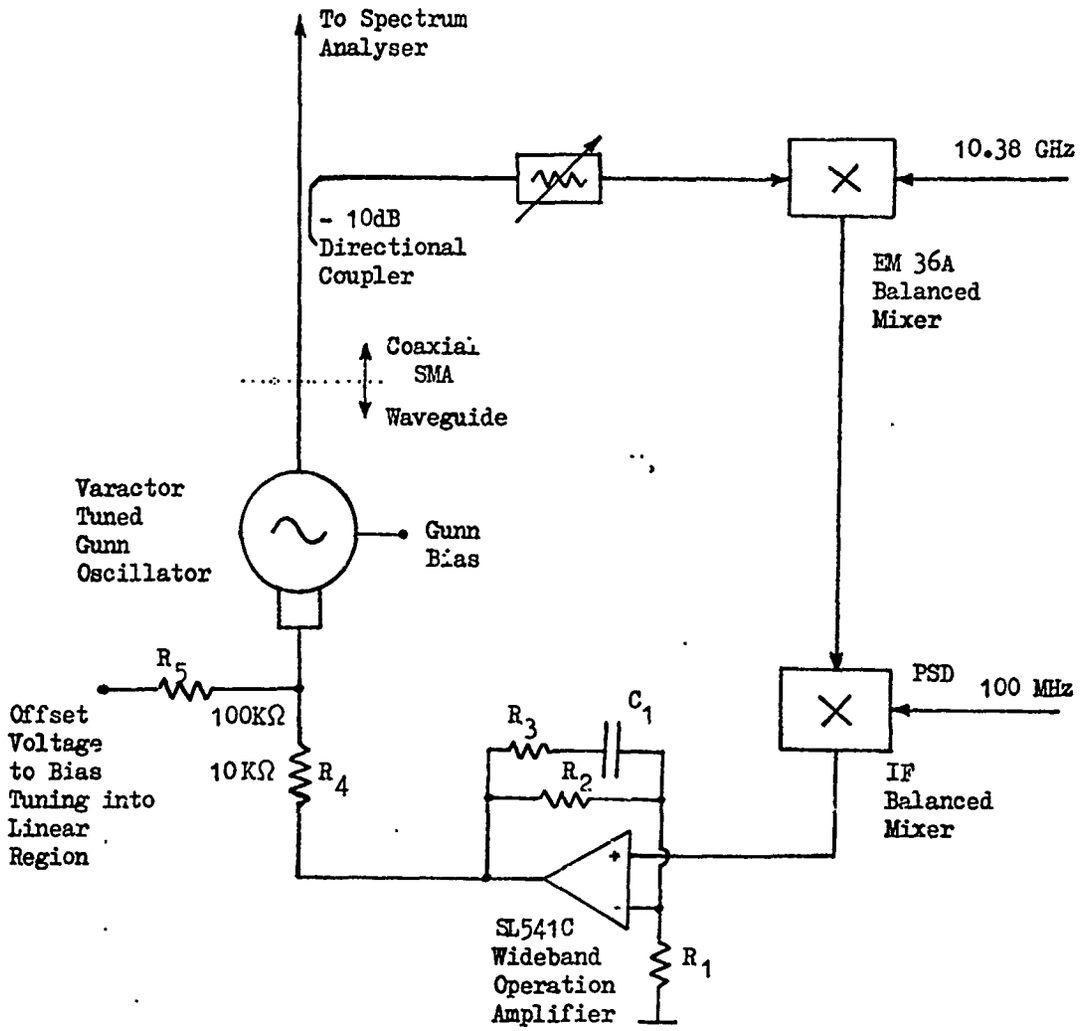


Fig. 4.31 Experimental Heterodyne Phase-Locked Loop

predicted theoretically from Eqn. 4.47 (7.2MHz) using a measured PSD gain K_1 = 0.1 v/rad and taking the combined voltage gain of the amplifier and offset circuit as x 9. Increasing the amplifier gain, locking ranges (i.e. half the synchronisation range) up to 20MHz were obtained before loop instability at 22MHz occurred. The instability frequency due to delay alone (estimated to be 6ns for the SL541C amplifier and 2ns for the loop length) was 31MHz ; the additional phase shift producing the lower instability frequency was found on investigation to be introduced by high frequency gain roll-off in the SL541C amplifier and the varactor feed. Since large loop bandwidths were not required for the demonstration of the basic loop behaviour, the amplifier gain was simply reduced to keep the loop bandwidth less than 10MHz for subsequent experiments. Under this condition the open loop gain was reduced below unity at a frequency significantly less than that at which the gain roll-off commenced. The loop behaviour would then be expected to be similar to that of the first or second order loop with ideal amplifier.

The acquisition behaviour of the first order loop was measured using the arrangement shown in Fig. 4.32 in which the output of the locked VCO is compared in a further PSD with a CW signal derived from the locking signals via a single-sideband modulator. For pulsed operation the VCO was retuned to 10.6GHz, at which frequency the same tuning sensitivity as previously used (8MHz/v) was obtained. The output of the PSD comparing the CW reference signal with the pulsed VCO output is shown in Fig. 4.33. The initial shift in DC level due to rectification of the VCO pulse is followed by many superimposed transients corresponding to random initial phase conditions. It may be seen that most transients are over in 100ns although a few, not

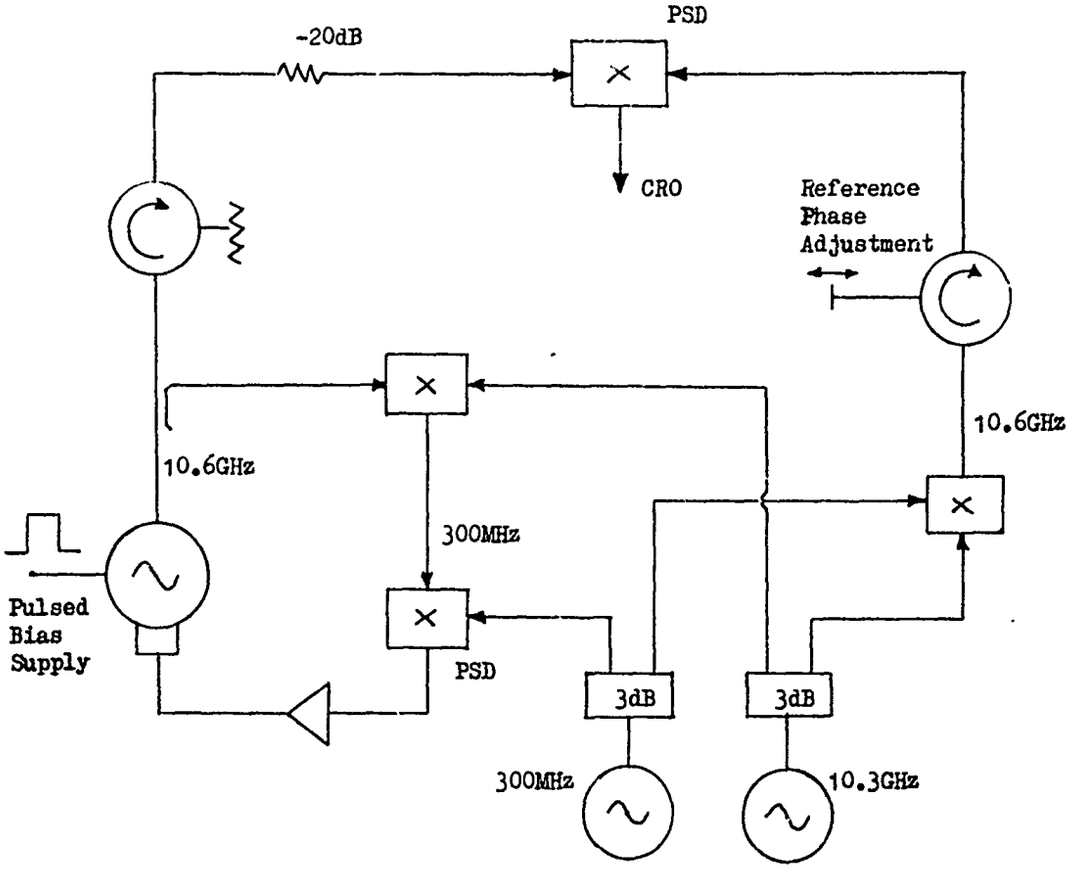


Fig. 4.32 Arrangement for Measurement of Capture Time

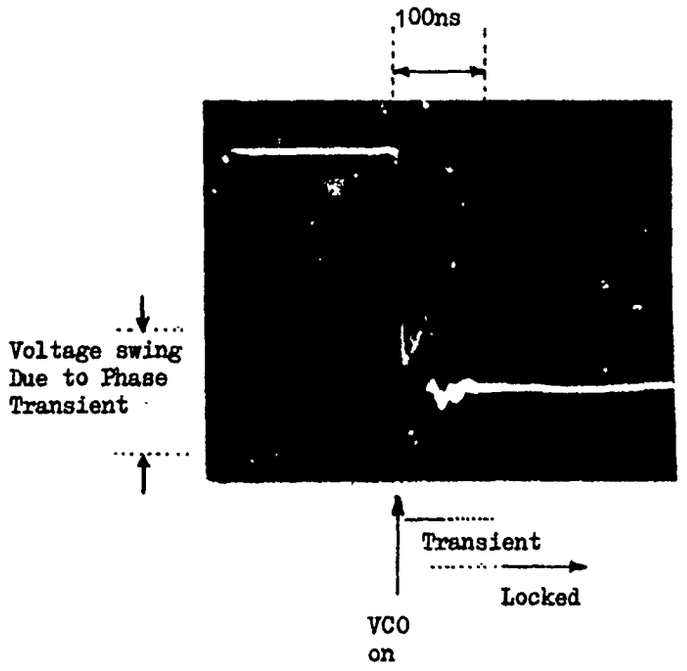


Fig. 4.33 Oscilloscope Trace of Phase Transient

evident in the photograph, extend to 200ns. This is in agreement with the approximation $\frac{10}{K}$ which in this case, for a locking range of 4.7×10^7 rad/s (7.5MHz) gives

$$\frac{10}{K} = 212\text{ns}$$

The deviations in the phase once lock has been achieved are due to ringing of the Gunn diode pulsed supply and chirp.

The loop PSD output may also be used to indicate the capture transient and phase error of the VCO. When the PSD output voltage is zero there is no phase error between the input and output which as previously defined implies the PSD inputs are, in fact, in phase quadrature. At the voltage extremities a $\pm 90^\circ$ phase error exists.

Fig. 4.34(a) shows, in the upper trace, the PSD output voltage (many superimposed transients) for a pulsed first order loop with locking range 3.8×10^7 rad/s (6MHz). The lower trace shows, as a time reference, the pulsed bias supply to the Gunn diode.

To best illustrate the effect of phase errors, the detuning was set to give a locking signal frequency at the edge of the locking range, i.e. $\Delta\omega \approx 6$MHz. It may be seen that the loop initially locks with a large phase error $\approx 90^\circ$ in ~ 200ns; subsequently chirp reduces the detuning and thus also the phase error during the pulse.

Fig. 4.34(b) shows the PSD output voltage for a pulsed second order loop operated within the capture range with

$$R_1 = 100\Omega$$

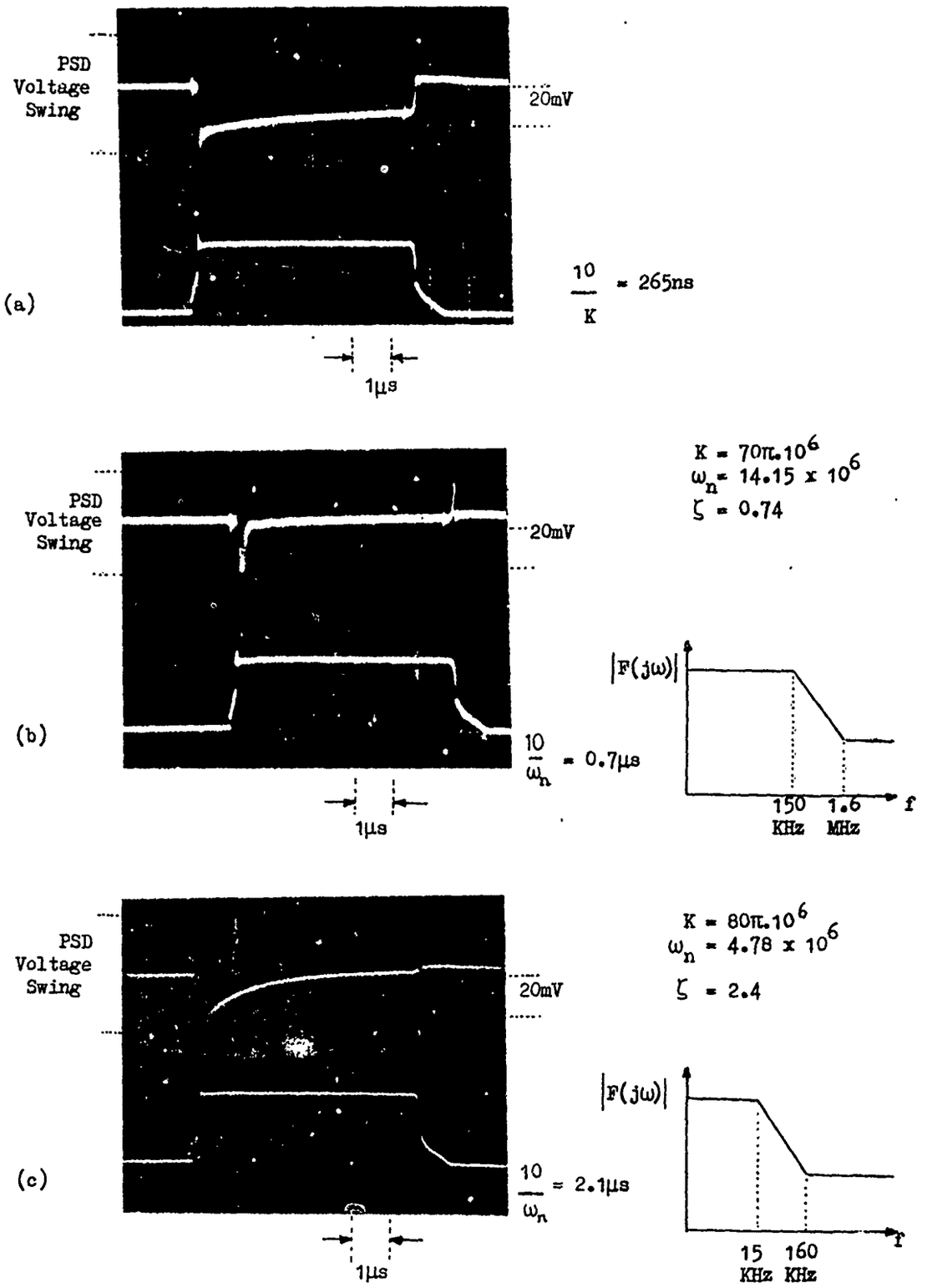


Fig. 4.34 PSD Output Voltage for Pulsed First and Second Order PLLs

$R_2 = 11K\Omega$

$R_3 = 1K\Omega$

$C_1 = 100pF$

The initial detuning was again set at the edge of the capture range to clearly show the phase error transient. It may be seen that after a brief initial period in which the capture transient resembles that of a first order loop with a large phase error, the phase error rapidly drops to a low level. The slight slope on the trace, once a low phase error has been achieved, is due to coupling between the two oscilloscope inputs as may be seen by comparing the trace levels before and after the pulse when there is no PSD output. The theoretical approximate acquisition time for this case is $\sim 0.7\mu s$ to ensure capture, with most transients over in $< 350ns$. This may be seen to agree with the observed transients.

To show more clearly the reduction of phase error with time of the second order loop, C_1 above was changed to 1000pF. The reduction of phase error from the original high value at the start of the pulse is now clearly seen, although in practice such a slow transient would be undesirable. The quantity $\frac{10}{\omega_n}$ for this case is $2.1\mu s$. although since $\zeta \not\approx 1$ $(= 2.4)$ this approximation is less exact for this loop.

The acquisition behaviour of first and second order loops was thus found to be in approximate agreement with the theoretical prediction. The photographs of Fig. 4.34 clearly show the advantage of the second order loop over the first order for reducing both the absolute phase error and the change in phase error resulting from chirp.

4.3 Conclusions

In view of the length of this chapter, a review of the main features in the preceeding analysis of injection locked oscillators and PLLs is given in this section, in addition to conclusions on the applicability of these techniques to active array elements.

4.3.1 Injection Locked Sources

The locking range of an injection locked oscillator, defined by Eqn. 4.3 as half the range of frequency $\Delta\omega_s$ over which synchronisation can occur, is obtained from the differential equation Eqn. 4.1 by applying the conditions

$$\frac{d\varphi_e}{dt} = 0 \quad \text{and} \quad -1 \leqslant \sin\varphi_e \leqslant 1$$

giving

$$\Delta\omega_L = \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}} \qquad \ldots(4.3)$$

The synchronisation range is thus

$$\Delta\omega_s = 2\Delta\omega_L = \frac{2\omega_0}{Q}\sqrt{\frac{P_1}{P_2}} \qquad \ldots(4.4)$$

The relationship between the steady state phase error introduced by the locking process and the detuning $\Delta\omega$ between the locking signal and the free running frequency was given by Eqn. 4.6 as

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{\Delta\omega_L}\right) \qquad \ldots\ldots(4.6)$$

In the region for which phase errors are small, differentiating gives the rate of change phase error with detuning as

$$\frac{d\varphi_e}{d(\Delta\omega)} = \frac{1}{\Delta\omega_L} \qquad \ldots\ldots\ldots 4.144$$

It was previously noted that the phase error predicted from Eqn. 4.6 will have little effect on the array radiation pattern if all the array elements exhibit the same phase error. There will, however, inevitably be a spread in the values of free-running frequency for a practical array of solid state sources due to variations in the device and circuit parameters and thus a spread in the value of phase error introduced by the locked oscillators. The effect on the radiation pattern of random deviations from the desired array phase distribution is discussed in Chapter 5. From Eqn. 4.6, the variation in the phase error resulting from a given spread in values of detuning can clearly be minimised by adopting a large value of $\Delta\omega_L$ for the locked oscillators. This therefore implies, with reference to Eqn. 4.3, the use of low locking gain.

Taking the values previously used in the example presented in Table 4.1, i.e. a locking Q of 100, a free running frequency of 10GHz and locking gain of 10, Eqn. 4.144 predicts a rate of change of phase error with detuning of 1.8°/MHz. If it is then desired to restrict the spread of phase error on the array due to the locked oscillators to within $\pm 10^{\circ}$, the spread of oscillator detuning must not exceed $\pm$ 5MHz. This may be difficult to achieve in practice. The restriction on the spread of detuning can be eased by using lower oscillator Q since this will yield a greater value of $\Delta\omega_L$ for a given locking gain but care must be taken when adopting this approach that the variations in detuning resulting from differences in chirp and frequency drift

with temperature are not simply increased in proportion.

The synchronisation of pulsed injection locked oscillators where the locking signal is present during the build up of oscillations in the cavity is very rapid, as previously described in section 4.1. The acquisition time in this case is estimated to be less than $1/\Delta\omega_L$ secs.

In conclusion the attractive features of injection locking of simplicity, high possible locking gain and rapid synchronisation when pulsed, are offset by the problem of maintaining the difference in phase error between elements within acceptable levels. Typically, locking gains only of the order of 10dB may be used and even at this level it may be necessary, in practice, to adopt additional techniques to minimise the spread of detuning, such as choosing only closely matched sources, temperature stabilisation of the array or the use of feedback circuits as shown in Figs. 4.4 and 4.5.

4.3.2 Phase Locked Loops

Despite the additional components and apparent complexity compared with a straightforward circulator coupled injection locked oscillator, the PLL offers several distinctly attractive features. First the locking gain and the locking range may be independently specified for the PLL; high values of locking gain can then be achieved simultaneously with large locking range. This cannot be achieved with an injection locked oscillator. Secondly, access to the components in the feedback path permits direct tailoring of the loop transfer function, providing in the second order loop, a compromise between the need, on the one hand, to maintain low phase errors and on the

other to ensure stability. Thirdly, use of the heterodyne phase-lock loop configuration provides a means whereby phase shifting of the microwave output may be achieved with only I.F. phase control. The microwave phase shifter conventionally used for electronic beam steering can then be replaced with an I.F. type. The characteristics of first and second order PLLs are reviewed in the following.

The First Order Loop

The analysis for the first order loop followed a similar pattern to that of injection locking. The locking range and synchronisation range of the first order loop were given in Eqn. 4.47 as

$$\Delta\omega_L = K = AK_1K_2$$

and $$\Delta\omega_s = 2\Delta\omega_L = 2AK_1K_2 \qquad \ldots\ldots(4.47)$$

where K_1 is the PSD gain in V/rad, K_2 is the VCO tuning sensitivity in rad/V.s and A is the frequency independent voltage gain of an ideal loop amplifier

The relationship between detuning and phase error was obtained in Eqn. 4.48

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{AK_1K_2}\right) \qquad \ldots\ldots(4.48)$$

and the equivalent expression to Eqn. 4.144 is then

$$\frac{d\varphi_e}{d(\Delta\omega)} = \frac{1}{AK_1K_2} \qquad \ldots\ldots 4.145$$

It may be noticed immediately that neither the input nor output power appear directly in this expression. With input powers to the PSD sufficient to drive it into the saturated region (~5mW) K_1 is essentially constant and the locking gain of the loop may then be specified independently of $\Delta\omega_L$. Since the locking signal power required is only ~5mW it is possible that the reference power for the whole array may be derived from a single solid state source.

To minimise the variation in phase error introduced in an array of PLL elements for a given variation in the values of detuning it is clear from Eqn. 4.48 that as for the injection locked case, a large value of locking range $\Delta\omega_L$ should be used. This implies, for a given K_1 and K_2, the use of a large value of voltage gain A. However, as shown in section 4.2.6, the delay τ_d that will inevitably exist in practical loops limits the amount of gain that may be included in the loop without instability. From Eqn. 4.121, the open loop gain of a first order loop must be reduced to unity at an angular frequency less than

$$\omega = \frac{\pi}{2\tau_d} \text{ rad/s} \qquad \text{.....(4.121)}$$

This is then the maximum value of locking range $\Delta\omega_L$ for stable operation. In practical loops where the delay introduced by the physical length around the loop may be neglected, the delay is primarily introduced by the loop amplifier. The SL541C amplifier used in the experimental work has a delay of approximately 6ns for which the maximum value of locking range by Eqn. 4.121 is 41.7MHz. Operational amplifiers with delays down to 4ns are commercially available, and this value of delay has been used to calculate the figures in the example performance of the first order loop in Table 4.1. Taking

this value of delay to calculate the maximum value of AK_1K_2, Eqn. 4.145 gives a rate of change of phase error with detuning of 0.9°/MHz for small phase error. If, as before, it is desired to restrict the variation of phase shift introduced by the PLLs to within $\pm 10^\circ$, the values of detuning are in this case restricted to be within $\pm$ 11MHz. Practically this may again be difficult to achieve for 10GHz oscillators without close control of the array environment.

Larger values of locking range and thus a greater permissible spread in values of detuning may be achieved using amplifiers with lower group delay; it is estimated that a suitable amplifier with delay down to 1 or 2ns could be constructed, but it must be noted that the use of such wideband amplifiers can usually be avoided using a second order loop.

The effect producing the very rapid synchronisation of pulsed injection locked oscillators, i.e. the presence of the locking signal during the growth of oscillations in the cavity, does not exist in the PLL; the acquisition time for the first order loop is obtained from solution of Eqn. 4.45 for various initial phase conditions. The time required for the phase error to be within a few degrees of the steady state value for the great majority of initial values of phase error was given by Eqn. 4.67 as

$$t = \frac{10}{K} = \frac{10}{AK_1K_2} \text{ sec} \qquad \text{.....(4.67)}$$

The Second Order Loop

The second order loop overcomes the first order loop restriction

on locking range by the use of a loop filter response providing high loop gain at low frequencies to yield a large locking range, whilst providing a reduced gain at high frequencies to maintain stability. It was shown in section 4.2.4 that only one of the filter transfer functions giving rise to a second order loop need be considered in practice: this is the lag/lead transfer function

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1}$$

The locking and synchronisation range of the second order loop were given by Eqn. 4.81 and 4.82

$$\Delta\omega_L = K = A_L K_1 K_2 \qquad \ldots(4.81)$$

$$\Delta\omega_s = 2K = 2A_L K_1 K_2 \qquad \ldots(4.82)$$

These are clearly of the same form as those for the first order loop, but the voltage gain A_L now used is that existing at low frequencies. The phase error versus detuning relation is similarly

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{A_L K_1 K_2}\right) \qquad \ldots(4.80)$$

and the rate of change of phase error with detuning is now

$$\frac{d\varphi_e}{d(\Delta\omega_L)} = \frac{1}{A_L K_1 K_2} \qquad \ldots\ldots\ldots 4.146$$

for small errors.

The examples given in Table 4.1 serve well to show the advantage of the second order loop over the first order. In the example, the high frequency loop gain in both cases is taken to be the maximum stable value with an amplifier of 4ns delay. The low frequency gain for the second order loop is however ten times greater here than the first order, yielding by Eqn. 4.146 a rate of change of phase error with detuning of 0.09°/MHz for low phase errors i.e. one tenth of that for the first order loop. The criterion of maintaining the variation of phase error to within $\pm 10^{\circ}$ now yields a maximum permissible frequency variation of $\pm$ 110MHz, which should be easily achieved.

The acquisition time of the second order loop for damping coefficients of the order of unity was given by Eqn. 4.103 as

$$t \doteq \frac{10}{\omega_n} \qquad \ldots\ldots(4.103)$$

where ω_n is the loop natural resonant frequency given in Eqn. 4.97. From the example in Table 4.1 and the experimental results, it may be seen that acquisition times short compared to the 1 - 20μs pulse lengths typically used in active arrays, may be readily obtained with practically realizable loop bandwidths.

In conclusion the PLL has the advantage of offering a locking gain that is not directly related to locking range. Although more components are required in the PLL than in an injection locked oscillator, the high potential gain may enable one PLL ' stage ' to replace several stages of injection locked gain. The second order PLL can provide low values of phase error despite the limitation on loop bandwidth imposed by the delay that is present in practical loops.

Acquisition times short compared with the pulse lengths typically used may be readily achieved. Use of the second order PLL is, therefore generally the most attractive means of oscillator synchronisation, but in addition, use of the heterodyne loop configuration may be used to reduce phase shifting cost. Phase control of the microwave output may be achieved in this case via a phase shifter in the intermediate frequency input to the loop.

CHAPTER 5

GENERAL ASPECTS OF ANTENNAS INFLUENCING ACTIVE ARRAY ELEMENT DESIGN

5.0 Introduction

5.1 Techniques for Sidelobe Level Control in Active Array Antennas

5.2 The Effect of Element Amplitude and Phase Errors on the Radiation Pattern

5.2.1 Fixed Distribution Errors

5.2.2 Time Varying Errors

5.3 Receiving Array Signal to Noise Ratios

5.0 Introduction

Several general aspects of active array antennas relating to sidelobe level control, the effect of element random errors, and array receiving signal to noise ratios for various array configurations are discussed in this chapter. Since the results and techniques described are mainly well established, the discussion aims principally to present a review of some of the antenna considerations influencing active array design.

5.1 Techniques for Sidelobe Level Control in Active Array Antennas

Control of radiation pattern sidelobe levels is of particular importance for radar antennas. A low sidelobe level is desirable to minimise the illumination of targets in, and the reception of target returns from, directions outside the radiation pattern main beam; radar echoes received via the sidelobes will appear as false targets. A low sidelobe level is also desirable to minimise the reception of interfering signals, particularly deliberate ' jamming ' signals, via the sidelobes. Since the power of radar returns varies as the inverse fourth power of target range, whilst jamming signals suffer only inverse square law attenuation, jamming signals are often received at a sufficiently high power level that the detection of targets can be severely restricted or completely prohibited when the jamming source is within the radiation pattern main beam. Although little can be done to counter the loss of sensitivity in the direction of the jammer, the reception of significant jamming power also via the sidelobes can lead to loss of sensitivity in other

directions. A low sidelobe level is therefore desirable to effectively suppress signals received via the antenna sidelobes with respect to those received via the main beam.

For civil radar applications sidelobe levels between -20 and -30dB are often acceptable; for military applications a lower level, down to-40dB or less, is often desired to offset the effects of jamming.

The design of an antenna to produce a radiation pattern with a specified maximum sidelobe level is basically a question of ascertaining the aperture amplitude and phase distribution corresponding to an acceptable pattern. For a line source (i.e. a continuous linear antenna) of length a, the far-field electric field intensity $E(\theta)$ assuming $a \gg \lambda$ is given by

$$E(\theta) = \int_{-\frac{a}{2}}^{\frac{a}{2}} A(z)\exp\left(\frac{j2\pi z\sin\theta}{\lambda}\right)dz \qquad \ldots\ldots 5.1$$

where θ is the angle measured away from broadside in the plane of the antenna

z is distance along the antenna with reference to its centre

λ is the wavelength

and $A(z)$ is the excitation at distance z.

$A(z)$, the aperture distribution, may be complex, representing both the amplitude and phase distributions, i.e.

$$A(z) = \left|A(z)\right|.\exp(j\Psi(z)) \qquad \ldots\ldots\ldots 5.2$$

where $\left|A(z)\right|$ is the amplitude distribution and $\Psi(z)$ is the phase distribution.

Distribution Type	Relative Gain	Half-Power Beamwidth (deg.)	Intensity of 1st Sidelobe (dB below max. intensity)
Uniform	1	$51\lambda/a$	13.2
Cosine	0.81	$69\lambda/a$	23
Cosine^2	0.667	$83\lambda/a$	32
Triangular	0.75	$73\lambda/a$	26.4
Circular	0.865	$58.5\lambda/a$	17.6

Table 5.1 Comparison of Some Aperture Distributions

In the case of an array antenna, the far-field electric field intensity reduces to a finite summation of the contributions from the individual element radiators. For a linear array of isotropic radiators, the far-field electric field intensity is given by

$$E(\theta) = \sum_{n=0}^{N-1} A_n \exp\left(j \frac{2\pi n d . \sin\theta}{\lambda}\right) \qquad \ldots\ldots 5.3$$

where A_n is the complex excitation of element n

d is the inter-element spacing (assumed constant)

and N is the number of array elements.

It is well known that amplitude distribution tailoring can be used to provide sidelobe level control in both reflector and array antennas. Table 5.1 shows the effect on the peak sidelobe level of half-power beamwidth of various amplitude tapers. The application of such tapers in the case of a reflector or passive array antenna is straightforward : taper may be applied via the feed radiation pattern and geometry in the case of the reflector and via a weighted power distribution network in the case of the passive array. For both of these the reciprocal nature of the antenna will yield the same radiation pattern on both transmission and reception.

The application of amplitude taper to active arrays calls for further thought regarding the best way in which this may be implimented. First, active array elements will inevitably contain non-reciprocal devices or switches to change the signal path on transmit and receive, since the element amplifiers used to generate the transmitter power will be non reciprocal. This means that it will be possible to apply

independent tapers on transmission and reception ; for example, the taper on reception could be applied at IF, after downconversion to IF within each element. Secondly, manufacture of an active array will be considerably simplified if identical elements can be produced, rather than a number of elements containing devices of different output power. Consideration must then be given to methods of achieving the desired amplitude distribution on transmission, whilst making best use of the available solid state microwave power.

One arrangement, equivalent to that of the passive array, which could be used where the element solid state generators are configured as amplifiers, is to simply apply the desired taper in the distribution network as for a passive array. On transmission the element amplifiers, all providing the same gain, will reproduce the tapered distribution across the array. On reception, the same or possibly a different taper could be used, with the distribution network perhaps also acting as a power combiner. The disadvantages with this arrangement are :

1) The element amplifiers away from the array centre will be operated with a power output considerably below their maximum. Since it was shown in Chapter 3 that the powers available from solid state microwave devices are somewhat restricted, it will usually be desirable to operate all the devices in an active array at as high a power level as possible, consistant with constraints imposed by reliability considerations.

2) This arrangement clearly is not suitable for locked oscillator element sources since the output powers of identical oscillators will be the same for all elements.

An alternative arrangement, suitable when either amplifiers or oscill-

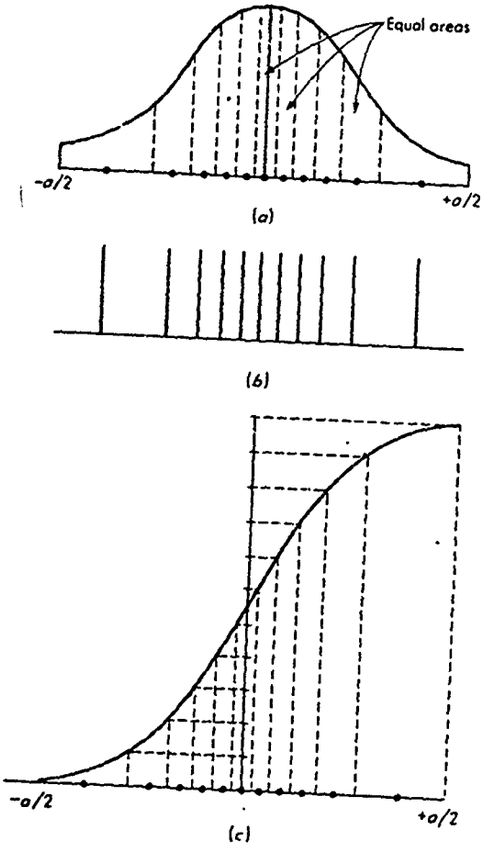


Figure 5.2 Deterministic Density Taper

(a) Model Current Density Function (Amplitude Taper) Divided into 11 Equal Areas

(b) Location of Density Tapered Elements

(c) Cumulative Current Distribution

(After Skolnik[6])

ators are used, is simply to accept a uniform amplitude distribution from identical, equally spaced elements on transmission, yielding a relatively high peak sidelobe level (- 13dB) and concentrates on providing a high degree of sidelobe suppression via the receiving radiation pattern, which as previously mentioned, may be formed using an independent amplitude distribution. In cases where false target returns and illumination of clutter outside the main beam are not limiting problems, this approach will probably be acceptable since it is the level of the receiving pattern sidelobes alone which affects the radar system performance in the presence of jamming.

A further alternative arrangement giving sidelobe level control on both transmission and reception, uses the technique of ' density tapering ' in which unequal spacing of equally excited elements is used to effectively provide a tapered distribution. Array design using this technique may be carried out via either a deterministic or a statistical approach.

Figure 5.2, after Skolnik[6] , shows the basis of the deterministic approach. A model continuous distribution yielding a radiation pattern similar to the desired one is initially chosen. The location of equally excited, unequally spaced elements in the array is determined by dividing the area under the model distribution into equal areas, as shown in (a). The relative positions of the array elements are then taken from the centres of the intervals defined by the equal areas. Fig. 5.2(b) shows the relative positions of the elements and (c) shows the positions relative to the cumulative current distribution.

It would be expected that the radiation pattern produced by a density

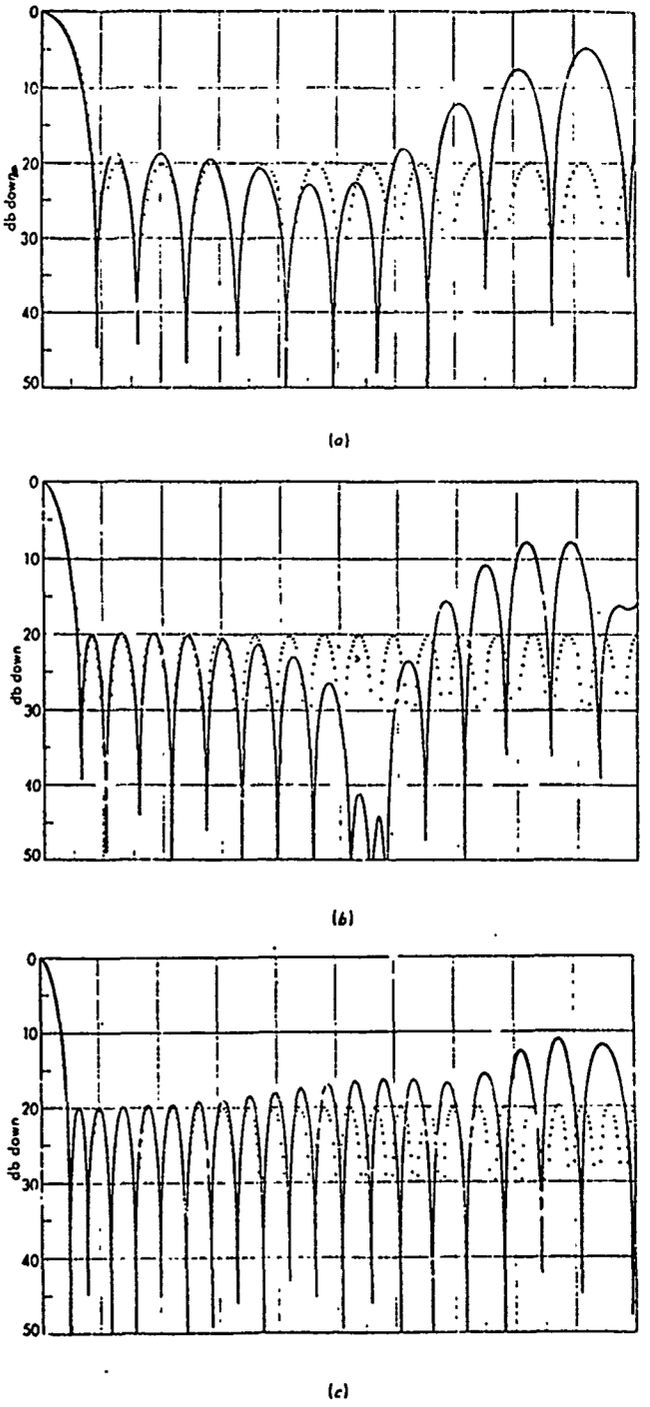


Fig. 5.3 Comparison of Density-Tapered Array Pattern (Solid Curve) and the Model Amplitude-Tapered Array Pattern (Dotted Curve), (a) 12 Elements; (b) 18 Elements; (c) 24 Elements (After Skolnik [6])

tapered array would follow the pattern of the model in the vicinity of the main beam and close-in sidelobes, and deviate at larger angles. This is indeed found to be the case as shown in Fig. 5.3, given by Skolnik[6] . Fig. 5.3 (a), (b) and (c) shows the array factors for a 20 wavelength aperture containing 12, 18 and 24 elements, respectively. The array factor of the model distribution, a Taylor distribution [46] designed to produce an equal -20dB sidelobe level is also shown in the dotted curves. The plots cover, in each case, the angular region over which the density tapered array pattern initially follows, and then starts to deviate from, the pattern of the model distribution. Although values for the horizontal axes are not given in the reference, the figure serves well to show that increasing the number of elements improves the fit between the patterns. The number of elements that may be included in a density tapered array is limited, in practice, by the minimum element spacing ($\sim\lambda/2$). This may arise either from the physical size of the element or from the increase in mutual coupling as the separation is reduced.

Defining the degree of thinning as the percentage of elements removed from a half-wave-length spaced array of the same dimensions, the 24 element array has 41 percent thinning. The closest spacing between adjacent elements is 0.52 wavelengths. In practice the far-out sidelobes, which deviate from the desired pattern of the model illumination, can be suppressed by the element factor and therefore it is possible to obtain consistantly low sidelobes throughout the visible region.

The statistical approach to density tapered array design follows similar lines. Here, the model illumination function is used to determine the probability of whether or not an element should be located at a specific aperture point. Elements are located pseudo-

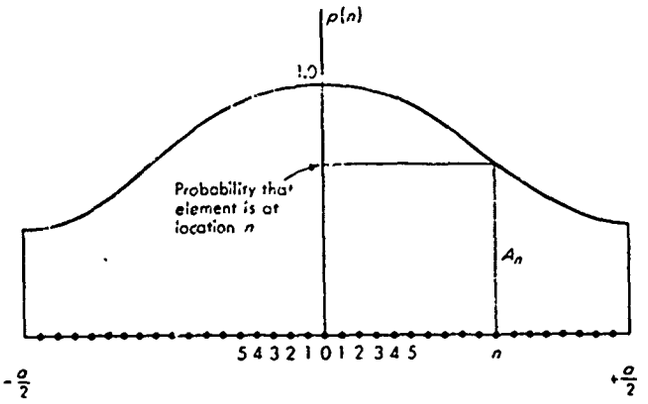


Fig. 5.4 Model Aperture Illumination used to Determine Placement of Elements in Statistical Density-Taper Method of Designing Unequally Spaced Arrays (After Skolnik[6])

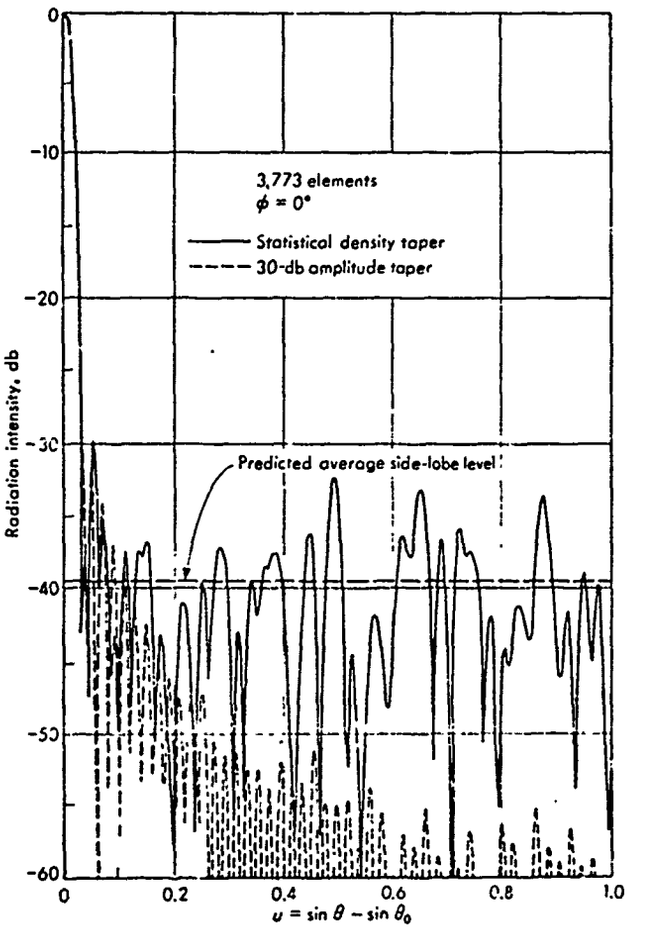


Fig. 5.5 Statistical Density-Taper Radiation Pattern Designed with a 30 dB Taylor Distribution as the Model (After Skolnik[6])

randomly rather than in a definite manner as in the deterministic approach, but they are not uniformly random because their probability density function is tapered. Their average density, computed statistically, follows the form of the model illumination function, since the tapered weighting of the probability density functions makes the placing of an element near the aperture centre more likely than elsewhere. The method is termed a statistical density taper since the radiation pattern can only be specified beforehand in statistical terms.

Fig. 5.4, also from Skolnik[6], illustrates the procedure for designing a statistical density tapered array. The curve representing the model amplitude distribution is used here to define the probability of an element existing at each of the positions that would be occupied in a filled array with half-wavelength spacing. The probability of occupancy of the central element position is unity. Fig. 5.5 shows the calculated pattern of a statistical density tapered array and of the model distribution for a 50 wavelength diameter circular array with -30dB peak sidelobe level. Although it can be seen that the density tapered sidelobe level is significantly greater than the ideal one after the first few sidelobes, the advantage of the statistical approach is illustrated in that the sidelobe energy for larger angles is fairly evenly distributed, and does not build up to consistantly high peak values. Fig. 5.6 shows the element locations in the planar array, the pattern of which is shown in Fig. 5.5. This array contains 3773 elements compared with 7800 if the array were filled, indicating a thinning factor about 50 percent.

The design of an active array with elements of equal transmitting output power will therefore probably take one of two forms :

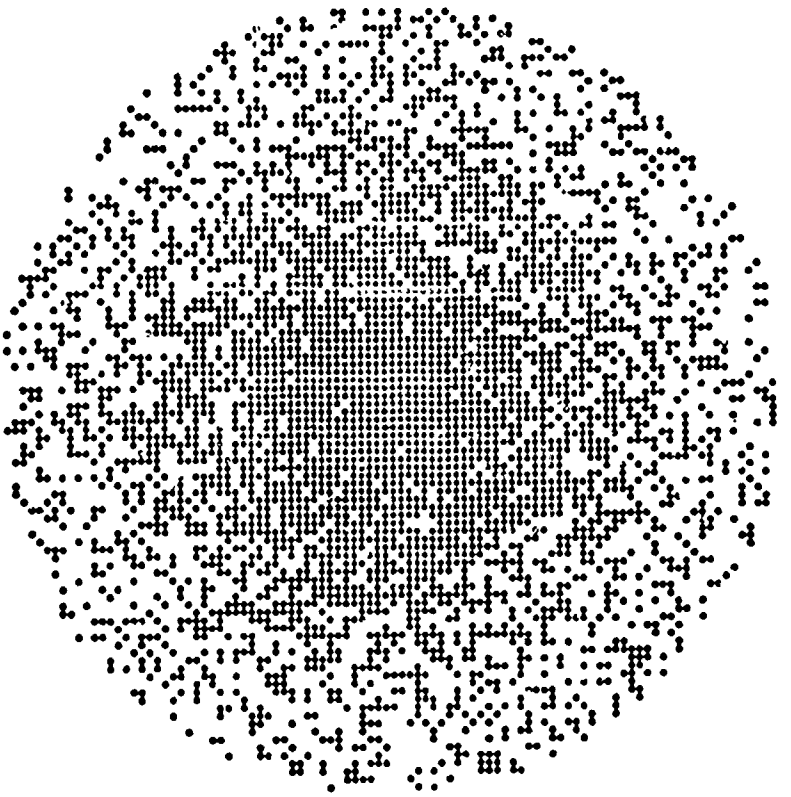


Fig. 5.6 Locations of the Elements Determined Statistically for the -30 dB Density Taper Array the Pattern of which is shown in Fig. 5.5
(After Skolnik[6])

1) An array of equal element spacing of approximately half-wavelength, providing uniform distribution on transmission and a separate tapered distribution on reception. Lower receiving sidelobes should, in general, be available from a filled aperture than from a density tapered array.

2) A density tapered array providing sidelobe control on both transmission and reception. For a given number of elements, the aperture dimensions will be larger in this case than for a half-wavelength spaced array, and thus a narrower beamwidth would be expected. The statistical method of density tapered array design has the advantage of producing a sidelobe structure with a uniform mean value in the region where the pattern differs from that of the model. This technique is however only generally applicable to large arrays where there are enough ' samples ' to ensure statistical regularity. Skolnik[6] suggests that this approach is limited to arrays containing more than 100 elements, the deterministic approach providing better results with smaller arrays. A further discussion of density tapering is given by Steinburg[5].

5.2 The Effect of Element Amplitude and Phase Errors on the Radiation Pattern.

5.2.1 Fixed Distribution Errors

Random amplitude and phase errors on the element outputs of an array antenna impose a practical limitation on the degree of sidelobe suppression that may be obtained from the use of tapered distributions, and clearly a similar limitation will also exist for density tapered arrays. The additional complexity that is introduced by the use of active elements in an array may in general be considered to present

a more exacting task than for the passive array when it is desired to meet a given amplitude or phase tolerance. Conversely the additional degrees of freedom afforded by amplitude and phase adjustments that could be provided in each element may be considered to ease the tolerancing problem, although from the point of view of manufacturing cost this approach may carry an economic penalty. The analysis given below, following the approach of Gladman[47], seeks to indicate the limitation on the sidelobe level that may be achieved in the presence of a given level of random amplitude and phase errors.

Taking for simplicity the case of an array of N evenly spaced elements the far-field electric field intensity in the presence of errors is given by

$$E(U) = \sum_{n=0}^{N-1} A_n(1 + \Delta_n)\exp(j\delta_n)\exp(jnU) \qquad \ldots\ldots 5.4$$

where Δ_n is the amplitude error on the nth element

δ_n is the phase error on the nth element

A_n represents the element excitation, as before

$$U = \frac{2\pi d \sin\theta}{\lambda} \qquad \ldots\ldots 5.5$$

where d is the inter-element spacing

θ is the angle of interest, measured from broadside.

If the amplitude and phase errors are small $\exp(j\delta_n) \approx 1 + j\delta_n$

and Eqn. 5.4 may be written

$$E(U) = \sum_{n=0}^{N-1} A_n \exp(jnU) + \sum_{n=0}^{N-1} A_n \Delta_n \exp(jnU)$$

$$+ j \sum_{n=0}^{N-1} A_n \delta_n \exp(jnU) \qquad \ldots\ldots 5.6$$

The first term represents the unperturbed pattern, the second and the third terms being the ' error patterns ' due to the amplitude and phase errors respectively.

The radiated power is proportional to $E(U)E^*(U)$ and the radiated power within one period of the variable U is therefore proportional to

$$\int_{-\pi}^{\pi} P(U)dU = \int_{-\pi}^{\pi} E(U)E^*(U)dU \qquad \ldots\ldots 5.7$$

where $E^*(U)$ is the complex conjugate of $E(U)$.

Thus

$$\int_{-\pi}^{\pi} P(U)dU = 2\pi \sum_{n=0}^{N-1} |A_n|^2 + 4\pi \sum_{n=0}^{N-1} |A_n|^2 \Delta_n$$

$$+ 2\pi \sum_{n=0}^{N-1} |A_n|^2 \Delta_n^2 + 2\pi \sum_{n=0}^{N-1} |A_n|^2 \delta_n^2 \qquad \ldots\ldots 5.8$$

The first term on the right hand side represents the power in the unperturbed pattern whilst the remaining terms result from the amplitude and phase errors existing on the array. Assuming that the sum of the weighted amplitude errors given by the second term on the

right hand side is zero, the mean power in one period of U-space is:

$$\overline{P(U)} = \sum_{n=0}^{N-1} |A_n|^2 (1 + \overline{\Delta^2} + \overline{\delta^2}) \qquad \ldots\ldots 5.9$$

where

$$\overline{\Delta^2} = \frac{\sum_{n=0}^{N-1} |A_n|^2 \Delta_n^2}{\sum_{n=0}^{N-1} |A_n|^2} \qquad \ldots\ldots 5.10$$

is the power weighted mean square amplitude error, and

$$\overline{\delta^2} = \frac{\sum_{n=0}^{N-1} |A_n|^2 \delta_n^2}{\sum_{n=0}^{N-1} |A_n|^2} \qquad \ldots\ldots 5.11$$

is the power weighted mean square phase error.

The main beam power density of the unperturbed pattern $P_0(0)$ may be expressed as $G_0\overline{P_0(U)}$, where G_0 is the gain, and $\overline{P_0(U)}$ is the average power density of the undisturbed pattern.

The average power density of the pattern including errors, relative to that of the main beam in the undisturbed pattern is

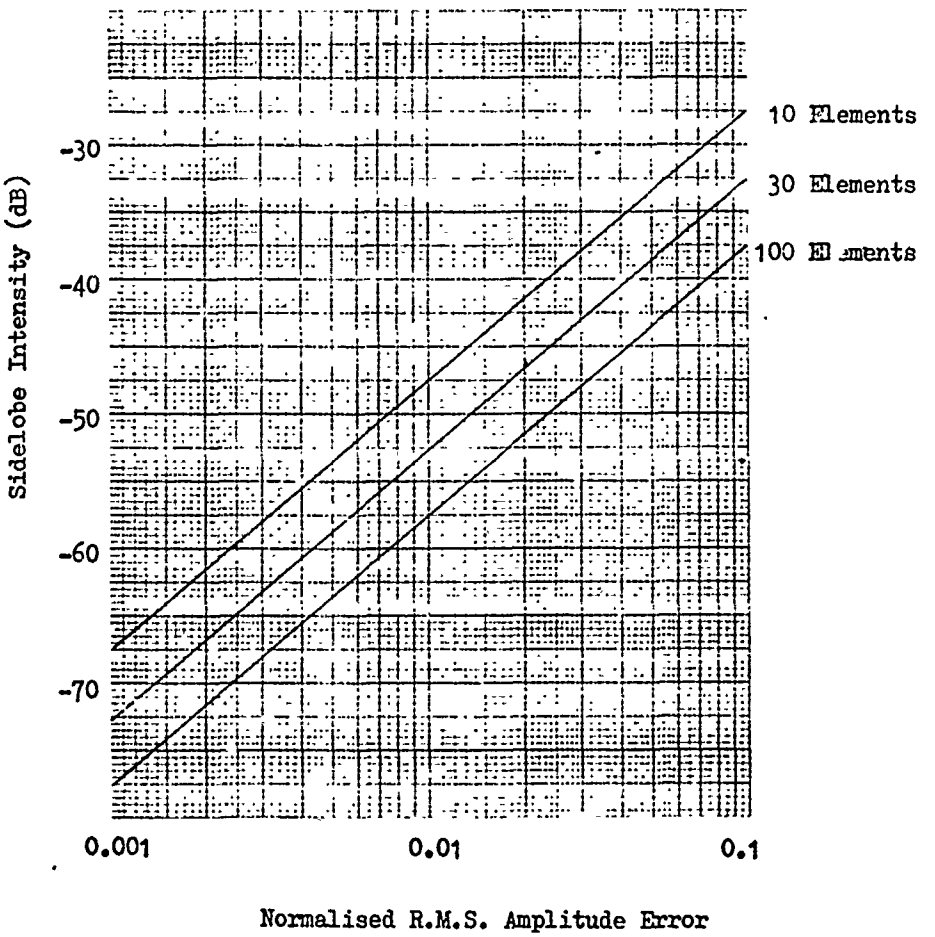


Fig. 5.7 Sidelobe Levels Resulting from Random Amplitude Errors. (After Gladman[47])

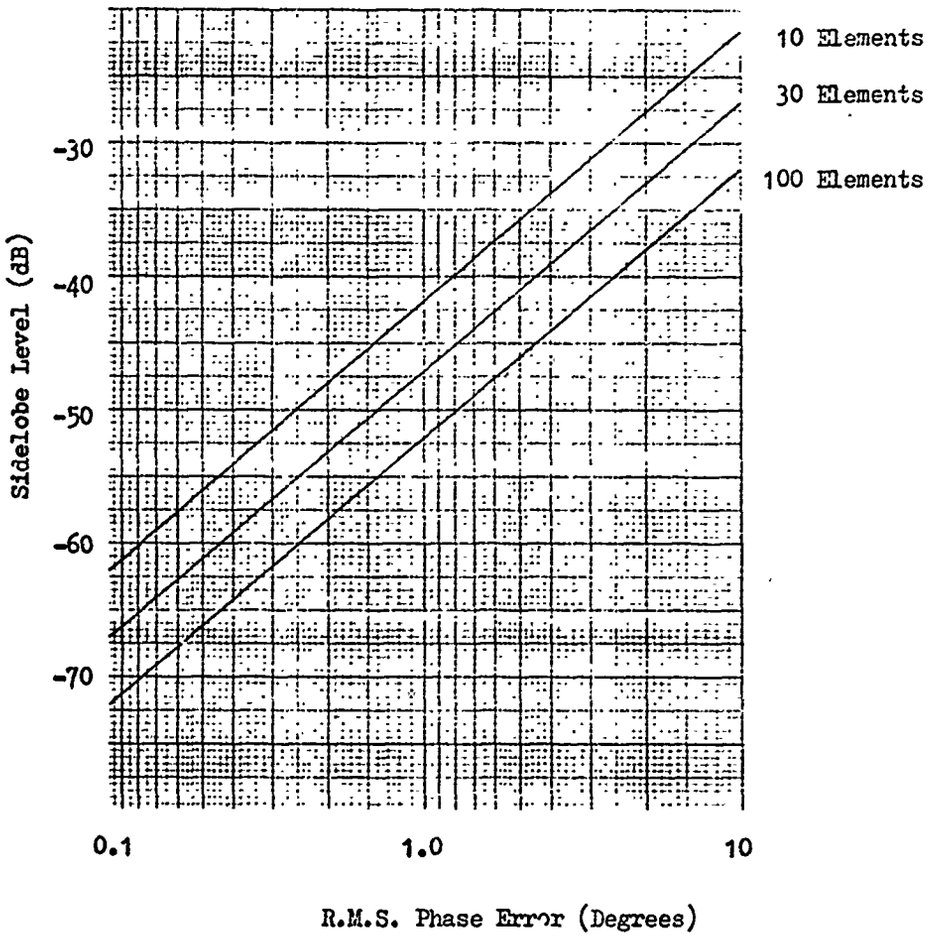


Fig. 5.8 Sidelobe Levels Resulting from Random Phase Errors. (After Gladman[47])

$$\frac{\overline{P(u)}}{P_0(0)} = \frac{1}{G_0} + \frac{\overline{\Delta^2}}{G_0} + \frac{\overline{\delta^2}}{G_0} \qquad \ldots\ldots 5.12$$

The first term is the average power density of the unperturbed pattern relative to the main beam density. The second and third terms are the power densities resulting from the amplitude and phase errors respectively. Since the gain G_0 will be proportional to the number of elements N in the array, it may be seen that the level of the contribution to the pattern from the amplitude and phase errors will also be related to the array size. Figs. 5.7 and 5.8, after Gladman[47], show the mean peak sidelobe level due to amplitude and phase errors respectively, for arrays of 10, 30 and 100 elements of equal half-wavelength spacing, where the errors are superimposed on initially uniform amplitude and phase distributions. A factor of two, derived empirically, has been assumed between the mean error level and the mean peak level shown in the Figures. Although the plots give the results specifically for the uniformly illuminated case, Gladman indicates that in practice they may also be used as a guide to the required tolerancing on tapered distribution arrays, if the curves are raised approximately by 1.5dB. The plots may then be used to assess the approximate degree of manufacturing accuracy required, and the amount of permissible phase error introduced by phase locking, if this is randomly distributed to ensure the pattern sidelobe level is below a specified value. In a similar context, they may also be used to indicate the minimum bit size of digital phase shifters for an array of given size when the errors introduced by the phase shifter quantisation are randomised.

5.2.2 Time Varying Errors

Time varying errors on the aperture distribution can arise in two cases :

1) phase errors introduced by the locking phase transient of pulsed phase-locked element sources

2) amplitude and phase errors due to time varying signal components such as additive amplifier noise that are present throughout the transmission.

Response to the Phase Locking Transient.

As described in Chapter 4, during an initial period in the synchronisation of pulsed phase-locked loops, and also to some extent for pulsed injection locked oscillators, the output is not fully coherent with the input locking signal but exhibits a phase/frequency transient before reaching the steady state locked condition. The array radiation pattern during this period will not therefore be the same as that calculated simply on the basis of the steady state phase distribution and may be expected to change significantly with time.

Referring the phase of the nth element output φ_n to a convenient phase reference on the locking signal, the radiation pattern of an equally spaced array of N elements at time t after the application of the supply voltage may be expressed as :

$$E(U,t) = \sum_{n=1}^{N-1} |A_n| \exp(j\varphi_n(t))\exp(jnU) \qquad \text{.....5.13}$$

where $|A_n|$ is the excitation amplitude at the nth element, assumed constant during the pulse. (Oscillation growth times are assumed to be so rapid in comparison to the pulse length that they may be ignored.)

and $\varphi_n(t)$ is the phase of the nth element at time t. A time varying phase indicates the existance of a frequency difference between the element output and the reference.

It was previously noted in Chapter 4 that the initial phase of pulsed oscillators is essentially random where the oscillation is initiated by random noise processes. At the instant following the application of the supply voltage a random phase distribution will therefore exist on the array. A full analysis of the dynamic characteristics of the radiation pattern would therefore initially assume a random phase distribution, calculate the subsequent variation of the phase of each element output with time (for instance using phase plane analysis), and then use these phase values to compute the radiation pattern at each instant of time. Calculation of the far-field phase in each direction

$$\mathrm{Arg}(E(U,t))$$

and its rate of change, will provide information on the spectral content of the signal transmitted in each direction. Repeating the computation for many random initial conditions will indicate the time average response.

A detailed analysis of the form described has not been carried out in the work covered by this thesis; however the transient radiation pattern and the associated ' spectral splash ' during the synchronisation of pulsed PLLs are of interest for determining the details of the transmitted pulse shape and spectrum, and this analysis should

be considered in future work.

Some of the basic features of the response may be obtained without a detailed treatment, using simple reasoning. When the array consists of a large number of elements, the initial uniform amplitude, random phase distribution may be expected to produce an array factor which will not exhibit significant gain in any direction but will approximately follow the level of the average pattern. In practice where directive elements are used, the initial pattern will simply be the element pattern. With increasing time, as numbers of the element sources reach the steady state output phase, the increasing coherent addition of the element outputs will result in growth of the desired radiation pattern main beam and the suppression of the radiated power in other directions. The array radiation pattern may thus in general be expected to change with time from a shape governed by the element to that of the usual narrow beam associated with a coherently excited array. The growth of the main lobe may be expected to follow the cumulative curve of the percentage of elements reaching the steady state output phase with time shown in Fig. 4. Typically, the main beam will be formed in 100ns using loop bandwidths of the order of 10MHz.

It was shown in Chapter 4 that the frequency transient of pulsed, first order PLLs could extend to the edges of the locking range, and for second order loops to a limit set approximately by the loop unity gain frequency. It may therefore be expected that during the radiation pattern transient period, spectral components at all frequencies within these limits will be radiated by the array, with a spatial distribution determined principally by the element pattern. As the main lobe of the desired pattern forms, both the spectral spread and

the spatial spread of the transmission will be reduced.

The principal effects of the PLL locking transient on the transmitting radiation pattern will therefore be :

1) The pulse transmitted in the desired direction will have a ' rounded ' leading edge when compared to the output of a single element, corresponding to growth of the main beam. If the growth time is short compared to the pulse length, the energy lost from the main beam will have little effect.

2) During the transient, the array will briefly radiate a range of frequencies over a wide angle. Of particular interest from a further detailed analysis would be information on the level of radiated spectral components which, when reflected, could be confused with doppler shifted returns from moving targets.

Response to Noise Components in the Output Waveforms

Time varying AM and FM noise components of the array element outputs may be considered as varying amplitude and phase errors, and it is of interest to note that in an active array these components can be radiated with a significantly different directional characteristic than that of a passive array. A full analysis of this effect has been given by Iglehart [48]; however a simplified qualitive analysis as given below is sufficient to indicate the basic characteristics.

In a passive array with equal path lengths from a single generator to the array elements, the far-field electric field intensity at time t, including errors, may be written in a similar form to that used in Eqn. 5.4 :

$$E(U,t) = \sum_{n=0}^{N-1} A_n(1 + \Delta(t))\exp(j\delta(t))\exp(jnU) \qquad \ldots\ldots\ldots 5.14$$

where $\Delta(t)$ and $\delta(t)$ represent the amplitude and phase deviations due to noise components at time t. Since these will be the same for all elements in the array, neglecting any noise introduced in the feed, this becomes

$$E(U,t) = (1 + \Delta(t))\exp(j\delta(t)) \sum_{n=0}^{N-1} A_n \exp(jnU) \qquad \ldots\ldots 5.15$$

and thus the directional characteristics of the array are unchanged. The modulating noise components simply appear unchanged on the far-field signal.

For an active array of phase locked element sources, consider first the amplitude modulated noise terms. It was noted in Chapter 4 that AM noise present on the locking signal of a phase locked loop would in practice have little effect on the output noise level. This will also be true for injection locked oscillators when the locking signal is much smaller than the output, i.e. for large values of locking gain. The AM noise on the outputs in this case will therefore be simply that due to the individual oscillators alone and no correlation would be expected between elements. The far-field electric field strength including AM noise terms will then be

$$E(U,t) = \sum_{n=0}^{N-1} A_n(1 + \Delta(t))\exp(jnU) \qquad \ldots\ldots 5.16$$

where $\Delta_n(t)$ is the amplitude deviation on the nth element at time t. Since the Δ_n will be randomly distributed it will not in general be possible to predict the pattern shape exactly at a given time but on an instantaneous basis an analysis similar to that of 5.2.1 could be used. As the noise signal from each element is also randomly changing with time, it is clear that the time averaged pattern due to the AM noise would be evenly distributed with angle if the array elements were isotropic. Where directive elements are used the time averaged pattern will follow that of the element.

The response to FM noise is less straightforward. Referring again to the results of Chapter 4, it was found that the FM noise output of a locked oscillator could be approximately divided into two regions. Within a bandwidth given by Eqn. 4 for injection locking, and by plus or minus the open loop unity gain frequency for a phase locked loop, the FM noise output takes on the character of the locking source and the inherent FM noise is supressed. Outside this bandwidth the FM noise character is independent of the locking signal and is at the level of an unlocked oscillator. The noise components in these two regions will be radiated with significantly different spatial distributions.

FM noise components in the former range of frequency will be the same for all elements and thus, following the result of Eqn. 5.15 it may be seen that these will be radiated with the conventional narrow beam array pattern. The noise components will then appear unchanged on the far-field.

FM noise components in the latter range, which are due to the inherent oscillator noise, will not be correlated between elements and thus

will produce a random distribution. Following the previous arguments, these terms will be radiated according to the element pattern.

In summary, the only noise components that will be radiated with the full gain of the array will be those present on the reference locking signal since these will appear coherently on all element outputs. Both AM and FM noise generated within the element sources will be uncorrelated between elements and thus will be radiated with only the element pattern gain. This result is of particular interest for active array radar in which it is desired to provide moving target indication (MTI) since it indicates that the noise accompanying the main beam transmission will be determined primarily by the locking source. This can then be chosen to have a low output noise level. The noise level of the element sources is only of secondary importance and thus this need not be a major consideration in the choice of suitable solid state devices for an active array.

5.3 Receiving Array Signal to Noise Ratios

Two basic receiving circuit configurations may be adopted with arrays, in which receiver pre-amplification is provided either in distributed form within the array elements or at a single point following the combining circuit. The advantages of particular configurations such as amplification and down-conversion to i.f. within each element are discussed further in Chapters 6 and 7, but at this point it is of interest to compare the signal to noise ratios obtained in the two basic cases, primarily with the aim of determining, in the case of distributed amplification, the relationship between the element

S/N ratio and the overall S/N ratio.

In the following analysis an expression for the receiver signal to noise ratio is obtained for both passive and active receiving arrays, with and without amplitude tapers. Three important features of the analysis may be noted at this stage:

1) The power associated with the sum of coherent in-phase signal currents i_{s1}, i_{s2}, i_{s3}, ... is proportional to $(i_{s1}+ i_{s2}+ i_{s3}+...)^2$; the power associated with the sum of random noise currents i_{n1}, i_{n2}, i_{n3}, . . . is proportional to $(i_{n1}^2+ i_{n2}^2+ i_{n3}^2+.....)$.

2) An N element array is assumed in which the element impedance is Z_0. The combining network is followed by a transformer giving an output impedance also equal to Z_0.

3) A noise free antenna and a lossless combining circuit are assumed in order to identify the effects of amplifier noise alone.

A Passive Array Without Amplitude Taper

Passive elements are assumed here with a single amplifier following the combining circuit.

Let the signal current in each of the elements be

$$i_s \qquad (Z = Z_0)$$

The total signal current at the combiner output, assuming in-phase addition, is then

$$Ni_s \qquad (Z = Z_0/N)$$

After transformation back to impedance Z_0 the total signal current is

$$\sqrt{N}\, i_s \qquad (Z = Z_0)$$

After an amplifier with current gain A, the total signal current becomes

$$A\sqrt{N}\, i_s \qquad (Z = Z_0)$$

Let the amplifier noise output current be

$$i_n \qquad (Z = Z_0)$$

The signal to noise ratio is thus

$$\left(\frac{S}{N}\right)_1 = \frac{\left(A\sqrt{N}\, i_s\right)^2}{i_n^2} \qquad \ldots\ldots 5.17$$

which is the same as that for a reflector antenna of the same effective area.

An Active Array Without Taper

Again let the received signal current at the element be

$$i_s \qquad (Z = Z_0)$$

After amplification within the element with the same current gain as before, the element output signal current is

$$Ai_s \qquad (Z = Z_0)$$

At the output of the combining network the total signal current will be

$$NAi_s \qquad (Z + Z_0/N)$$

After transformation to impedance Z_0 this becomes

$$\sqrt{N}\, Ai_s \qquad (Z = Z_0)$$

Let the output noise current of each element amplifier be i_n, as before.

At the combiner output the total noise power will be proportional to

$$Ni_n^2 \qquad (Z = Z_0/N)$$

After transformation to impedance Z_0, the noise power is proportional to

$$i_n^2 \qquad (Z = Z_0)$$

The signal to noise ratio is thus

$$\left(\frac{S}{N}\right)_2 = \frac{\left(\sqrt{N}\,Ai_s\right)^2}{i_n^2} \qquad \ldots\ldots 5.18$$

It may be seen that the signal to noise ratios given by Eqns 5.17 and 5.18 are the same. Thus ideally the same performance will be obtained if a given amplifier is used either after the combining circuit in a passive array, or in each element in an active array. In practice, combining circuit losses will always degrade the passive array performance.

It remains to establish whether this equivalence also exists in the case of amplitude tapered arrays in which tapering is achieved

1) by transformer weighting for both active and passive arrays,
2) by transformer weighting in the passive array and by alternative weighting in the active array.

A Passive Array With Amplitude Taper

Amplitude tapering can be applied using an ideal transformer to scale the signal current to the desired value in each element. Since no loss is involved in the transformation, no additional noise terms are introduced. Let weighting terms x_m be applied to the element output currents ; the signal current output of the nth element will

be $x_n i_s$.

Again let the received element signal current be

$$i_s \qquad (Z = Z_0)$$

At the combiner output the total signal current will now be

$$i_s \sum_1^N x_n \qquad (Z = Z_0/\sum(x^2))$$

After transformation back to impedance Z_0 the total signal current becomes

$$i_s \sqrt{\frac{(\sum x_n)^2}{\sum(x_n)^2}} \qquad (Z = Z_0)$$

After amplification with current gain A, this becomes

$$Ai_s \sqrt{\frac{(\sum x_n)^2}{\sum(x_n)^2}} \qquad (Z = Z_0)$$

Let the noise output of the amplifier as before, be

$$i_n \qquad (Z = Z_0)$$

The signal to noise ratio is thus

$$\left(\frac{S}{N}\right)_3 = \frac{A^2 i_s^2 (\sum x_n)^2}{i_n^2 \sum(x_n)^2} \qquad \ldots\ldots 5.19$$

An Active Array with Amplitude Taper Using Transformer Weighting

Again let the element signal current be

$$i_s \qquad (Z = Z_0)$$

After the element amplifier this becomes

$$Ai_s \qquad (Z = Z_0)$$

At the combiner output the total amplifier signal voltage is

$$Ai_s \sum_{n=1}^{N} x_n \qquad (Z = Z_0 / \sum(x_n^2))$$

After transformation back to impedance Z_0, this becomes

$$Ai_s \sqrt{\frac{(\sum x_n)^2}{\sum (x_n)^2}} \qquad (Z = Z_0)$$

Let the amplifier output noise current be

$$i_n \qquad (Z = Z_0)$$

At the combiner output the total noise output <u>power</u> will be proportional to

$$i_n^2 \sum(x_n^2) \qquad (Z = Z_0 / \sum(x_n^2))$$

After transformation to impedance Z_0, the noise output power is proportional to

$$i_n^2 \qquad (Z_0 = Z_0)$$

The signal to noise ratio is thus

$$\left(\frac{S}{N}\right)_4 = \frac{A^2 i_s^2 (\sum x_n)^2}{i_n^2 \sum (x_n)^2} \qquad \text{.....5.20}$$

The signal to noise ratios of Eqn. 5.19 and 5.20 may be seen to be equal.

An Active Array with Amplitude Taper Using Attenuative Weighting

Attenuative weighting can be used to provide amplitude tapering in active arrays since the element amplifier determines the signal to noise ratio existing at the element.

Let the element signal current, as before, be

$$i_s \qquad (Z = Z_0)$$

After the element amplifier of current gain A, we have

$$Ai_s \qquad (Z = Z_0)$$

At the combiner the total signal current is

$$Ai_s \sum x_n \qquad (Z = Z_0/N)$$

After transformation to impedance Z_0 this becomes

$$Ai_s \sqrt{\frac{(\sum x)^2}{N}} \qquad (Z = Z_0)$$

Let the element amplifier noise output current be

$$i_n \qquad (Z = Z_0)$$

At the combiner output the total noise <u>power</u> will be proportional to

$$i_n^2 \sum (x_n)^2 \qquad (Z = Z_0/N)$$

After transformation to impedance Z_0, the total noise power is proportional to

$$\frac{i_n^2 \sum (x_n)^2}{N} \qquad (Z = Z_0)$$

The signal to noise ratio in this case is therefore

$$\frac{A^2 i_s^2 (\sum x)^2}{i_n^2 \sum (x_n)^2} \qquad \text{.....5.21}$$

The signal to noise ratios of Eqn. 5.19, 5.20 and 5.21 may all be seen to be equal. An equivalence in performance therefore exists in all three cases, whether a given amplifier type is included in each element, or singly after the combining network.

In an array with active transmitting elements, the weight of argument will usually be in favour of distributed amplification since :

1) Loss in the subsequent combining network is then not critical and a low cost design may be used. Low loss waveguide combiners may be required in a passive receiving array.

2) The additional complexity of providing amplification within the element on reception will not be great where circuitry already exists in each element for transmission.

3) This arrangement is particularly suitable where it is desired to downconvert the received signal to i.f. within each element. This allows array beamforming and signal processing to be performed at convenient frequencies. Amplification could be provided at r.f. or i.f.

CHAPTER 6

ACTIVE ELEMENTS BASED ON INJECTION LOCKING

6.0 Introduction

The characteristics of several possible active element designs based on the use of injection locked element sources are described in this chapter. In each case one or more stages of gain, provided by an injection locked oscillator, are used to amplify the reference signal within the element before transmission. On reception the signals received by the elements of the array may be combined either at the received microwave frequency, or at an intermediate frequency following downconversion within each element. Elements based on these two approaches are considered in sections 6.1 and 6.2 respectively. Experimental results are presented for one design of interest in which the local oscillator signal for downconversion to intermediate frequency of the element received signal is derived from the output of the element source.

The characteristics of injection locked oscillators, which clearly have a strong influence on the overall element characteristics, were summarized in section 4 of Chapter 4.

6.0.1 General Considerations Influencing Active Element Design

It was previously noted in Chapter 2 that the active array concept has been successfully demonstrated in several practical radar systems, a notable example being the U.S.A.F. Pave Paws radar, which is based on an array containing active elements . The technical feasibility of the technique has therefore been clearly demonstrated, but the very high cost of active phased arrays compared to that of conventional, mechanically rotated reflector antennas has neverthe-

less severely limited their acceptance.

In this light, the previous work on active arrays at University College London, described by Al-Ani et al [14] and Forrest et al [12], was principally aimed at the investigation of techniques for reducing the cost, particularly that associated with the element phase shifters, in active transmitting arrays. The techniques investigated, i.e. the harmonic locking and interpolation locking techniques, were previously described in Chapter 2. In a similar vein, a great many of the factors influencing the choice of possible element circuits in this and the next chapter are based on considerations regarding the element cost. Since many elements may be used in a practical array, the element cost clearly has a strong bearing on that of the complete array.

Two initial points related to cost restrict the types of element design considered :

1) For the conventional monostatic radar application, the elements should function in both transmission and reception modes to avoid a requirement for separate transmitting and receiving arrays. In addition to the extra size and weight associated with a second, receiving array, the expense of duplicating components such as the element phase shifters makes the separate array approach unattractive. Furthermore, if the total antenna dimensions are restricted, higher gain on transmission and greater effective receiving area on reception may be obtained from a single transmit-and-receive antenna than from separate antennas covering the same total area.

2) The use of identical, modular elements is clearly to be preferred since this not only minimizes the element cost, by permitting mass-

production techniques to be employed in manufacture, but also considerably simplifies the task of maintenance in the event of element failures. It was noted in Chapter 5 than an effective amplitude taper may still be applied to an array where identical elements are used, by means of the density tapering technique.

The basic element types of interest are therefore those of modular design that may be used in both transmission and reception modes.

The characteristics of PIN and ferrite microwave phase shifters were described in Chapter 2 and ideally the use of these components, which in addition to their high cost and loss consume significant drive power, would be avoided. Both the harmonic locking technique described by Al-Ani et al[14] and the heterodyne PLL may be used to achieve this end; element designs based on the heterodyne PLL are described in Chapter 7 ; the use of microwave harmonic locking is discussed in section 6.2.2. Where PIN or ferrite phase shifters are used, particular attention must be given to the best way in which these may be included in the element, with particular regard to their cost (i.e. by avoiding a very low insertion loss requirement) and the effect of their loss.

The preferred form of construction for the elements of practical arrays will, in general, be based on microwave integrated circuits (MICs). MIC construction has distinct advantages over a waveguide approach in size, weight and cost (at least in quantity production).

The use of MIC construction for the array feed network (or networks) however, must be taken into account in the element design. The use of waveguide feed networks will, in general, not be preferred, since

for large arrays these may exhibit both high weight and cost. When MIC feed networks are used, however, consideration must be given to the greater loss that may be encountered (typically 2 - 4dB). Since final amplification takes place within the elements on transmission, feed network loss will not be of first importance here ; on reception the use of MIC feed networks will generally call for preamplification of the received signals within the elements in order to prevent degradation of the receiver noise figure.

6.1 Active Elements for use with Microwave Combining Networks

6.1.1 Design without Element Preamplification

An element based on injection locking with no preamplification or downconversion of the received signal within the element represents the simplest case considered, although this is not likely to be the most attractive in practice. Such an element is shown in Fig. 6.1. The feed network in this case is used both for distribution of the reference locking signal on transmission, and for combination of the signals received by the array elements on reception. A transmit/receive (T/R) switch would be placed at the input to the feed network to isolate the receiver during transmission. The circulator shown in Fig. 6.1 serves both to separate the input and output signals of the injection locked oscillator on transmission, and to decouple the inactive oscillator from the signal path on reception. The element phase shifter, which must be a microwave type (e.g. PIN or ferrite), may be placed either in the feed to the element aperture, or the input to the element from the distribution/combining network. The advantage of the latter position is that the phase shifter loss (typically 1 - 3dB) does not reduce the output power of the element

on transmission, whilst on reception the effect of the loss is the same in either position. It may be seen that in either position, the phase shifter action on transmission and reception is reciprocal, assuming a reciprocal phase shifter is used. By the antenna reciprocity theorem, a single phase setting will thus serve to form a beam in the same direction on both transmission and reception. This result is of interest for comparison with that for subsequent elements where the sign of the phase shift must be changed between transmission and reception.

The attractive feature of this element is its overall simplicity ; very few components are required compared to the other elements considered. The main drawback, however, results from the losses that are present on reception. The combined loss on reception, of the circulator (typically $\sim$ 1dB), the phase shifter (typ. $\sim$ 1dB for ferrite types ; 1 - 3dB for PINs), and the combining network (typ. 2 - 4dB for an MIC network), will severely degrade the receiver noise figure. It was noted previously that the gain that may be obtained from injection locked sources will typically be limited to values of the order of 10dB. To provide higher element gain several stages of injection locked oscillator gain may be required. The loss on reception due to the circulators will then be greater than that mentioned above. The best possible receiver noise figure, assuming an ideal, noise free receiver following the combining network, will be numerically equal to the sum of these losses. It must be noted that if several injection locked oscillator stages are used, the phase errors introduced by the oscillators will be compounded.

A further possible disadvantage of this element is that amplitude

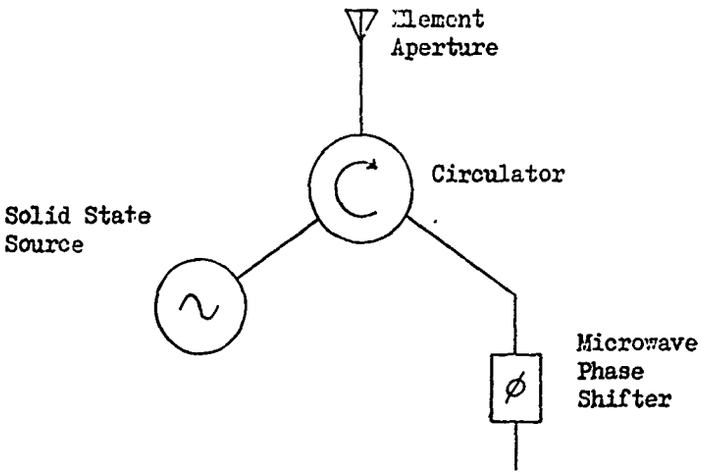


Fig. 6.1 A Simple Element Circuit with no Preamplification on Reception

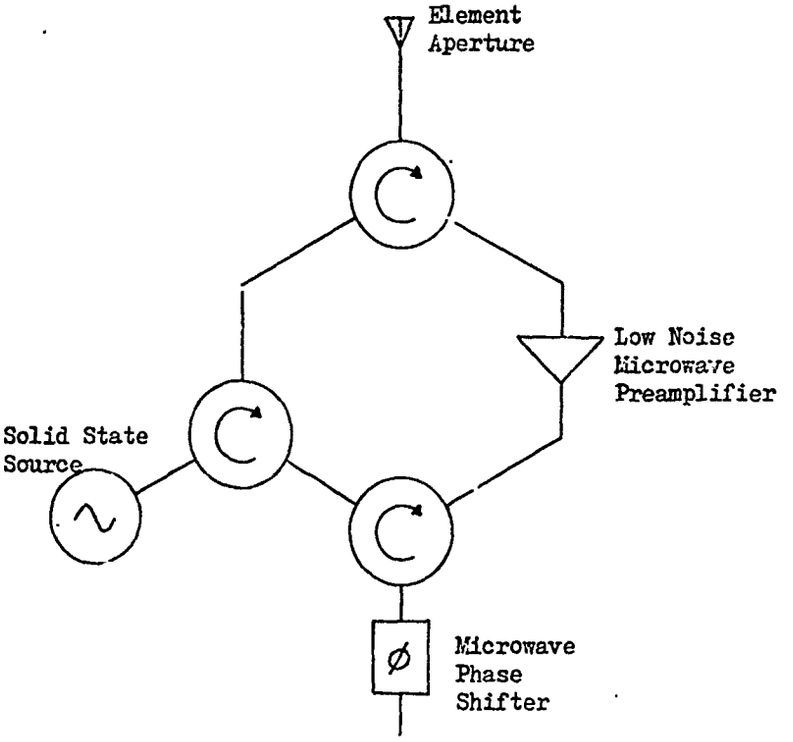


Fig. 6.2 Element Circuit Including Preamplification on Reception

taper on reception can only be applied via the feed network (i.e. attenuative weighting cannot be used here without further degrading the receiver noise figure). Since the feed network is also used on transmission, however, an equal amplitude taper would be produced on the locking signal distributed to the array. This would be undesirable if equal element output powers were used. Density tapering must therefore be used to provide aperture distribution weighting with this element design.

6.1.2 Design with Element Preamplification

The drawbacks associated with the element of Fig. 6.1 can be overcome by the inclusion of low noise preamplification within the element as shown in Fig. 6.2. In practice the preamplifier could take the form of a low noise FET amplifier as described in Chapter 3. Two circulators are now used to separate the transmitted and received signals within the element. On transmission the injection locked oscillator amplifies the pulsed reference signal applied to the element ; on reception the preamplifier provides low noise amplification of the received signal close to the element aperture. As before, a single array feed network is used for both transmission and reception. The microwave phase shifter may again be placed in two possible positions, i.e. in the feed to the element aperture or in the input to the element from the distribution/combining network. The latter position is now clearly to be preferred since in this position the phase shifter insertion loss will neither reduce the transmitted output power nor significantly degrade the receiver signal to noise ratio.

Where the preamplifier gain is sufficient to overcome the effects

of subsequent losses, the element noise figure is essentially determined by the circulator loss and the preamplifier noise figure. The value of preamplifier gain required to overcome the influence of subsequent loss on the element noise figure may be determined using Frii's formula for cascaded networks

$$F_{tot} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \frac{F_4-1}{G_1G_2G_3} + \text{etc} \qquad \ldots\ldots 6.1$$

where F_1, F_2, F_3,
G_1, G_2, G_3,
are the noise figures and gains (or losses) respectively, of the first, second, third, etc. networks
and F_{tot} is the overall noise figure.

In this case the first and second terms of Eqn. 6.1 represent the contributions from the circulator loss and the preamplifier. The third and subsequent terms represent the contributions to the overall noise figure of the components following the preamplifier. It may be seen that the magnitude of these is inversely related to the preamplifier gain G_2. A value of G_2 is thus chosen to reduce the values of these terms to negligible levels.

It may be noted that since losses following the preamplifier are no longer of first importance, an MIC feed network may now be used without difficulty. In addition, relaxation of the phase shifter insertion loss requirement will permit lower cost designs to be used.

The separate signal paths within the element on transmission and reception allow the use of independent aperture distributions in the two modes. The most suitable case for an active array when density tapering is not employed, as noted in Chapter 5, is the use of a

uniform distribution on transmission and a separate, tapered distribution on reception. With a feed network providing a uniform distribution, a taper may conveniently be applied on reception using variations in the gain of the element preamplifiers. This is the equivalent of attenuative weighting, i.e. where weights are applied by means of different attenuators following equal gain amplifiers.

One final point to be mentioned regarding this element is that for certain output power levels, protection of the receiving preamplifier may be required. Typically, the maximum peak power that may be applied to a microwave preamplifier is ~100mW. If the major component of the signal appearing at the preamplifier during transmission is due to leakage in the reverse direction around the circulator at the element output, (typically -20dB relative to the input power) the maximum source output power before a power limiter is required is 10W. For greater source powers, a limiter (e.g. PIN or varactor) would be required to precede the preamplifier. Alternatively a PIN T/R switch, providing typically ~60dB isolation when in the ' off ' state, could be used to replace the circulator at the element aperture ; however, this would require an additional control input to the element.

6.2 Elements for Use with Intermediate Frequency Combining Networks

Downconversion of the received signals to an intermediate frequency within each element has several advantages. First, the need for a microwave combining network is avoided ; losses of an i.f. combining network should be less than those of a microwave network, although clearly consideration must now be given to the conversion loss intro-

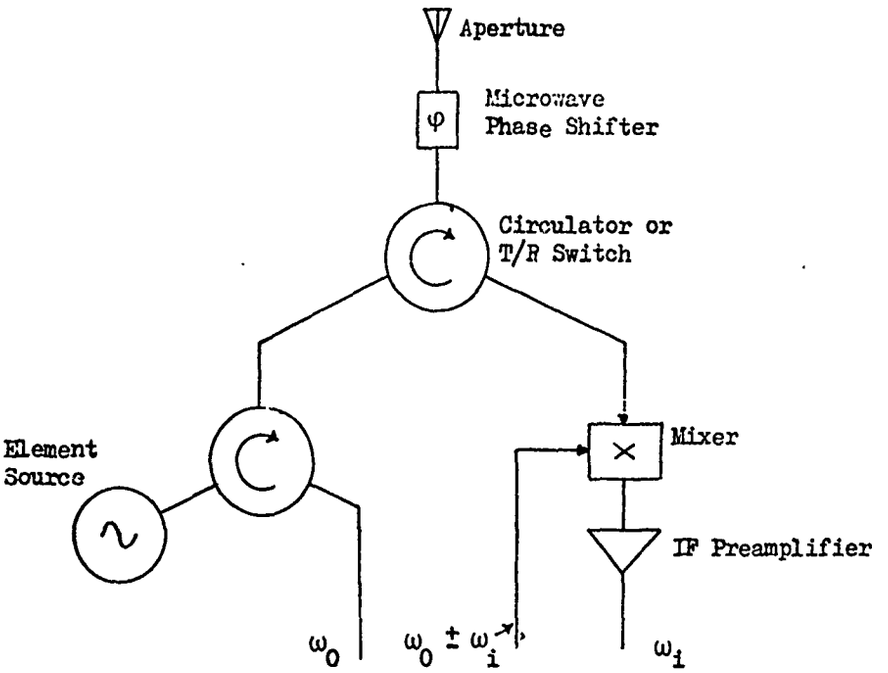


Fig. 6.3 Initial Element Including Frequency Down-Conversion On Reception

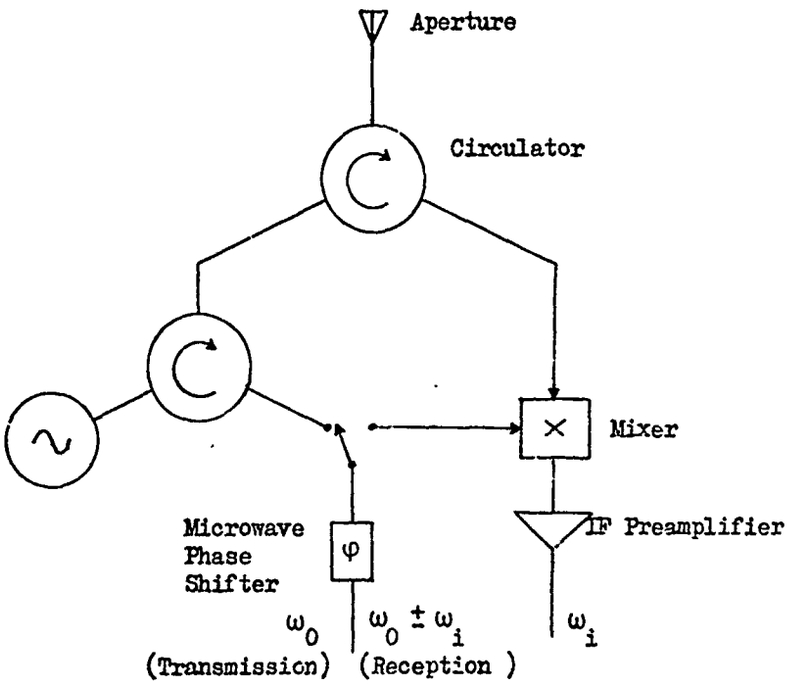


Fig. 6.4 Simplified Element Including Frequency Down-Conversion on Reception

duced by the frequency translation. Secondly, the amplitude and phase errors introduced by an i.f. combining network should, in general, be less than those for a microwave network. This results, to a large extent, from the smaller fraction of a wavelength represented by a given physical manufacturing tolerance. Also, individual adjustment of the amplitude and phase of the element outputs may be more conveniently applied at intermediate frequency. Lower receiving sidelobes should, therefore, be attainable with this arrangement. Thirdly, the use of i.f. combining networks is particularly suitable, from the viewpoint of both cost and losses, where it is desired to form several receiving beams. These may include both sum and difference patterns for monopulse tracking and possibly additional independent beams for passive tracking of active targets (e.g. jamming sources).

The intermediate frequency chosen for the element output on reception will be a compromise between the desire, on the one hand to use a low frequency to simplify the combining network construction, and on the other, to avoid the situation of the received signal bandwidth being a large percentage of the intermediate frequency value. Typically, an i.f. $\sim$60MHz may be used.

6.2.1 Design with a Single Injection Locked Oscillator Stage

The most straightforward modification including frequency translation to i.f. of the received signal within the element is shown in Fig. 6.3. A mixer is now included after the circulator or T/R switch. An additional microwave input to the element carries the local oscillator signal, with angular frequency $\omega_0 \pm \omega_i$, where ω_0 is the locking signal frequency and ω_i is the frequency of the element i.f. output. Since the only part of the circuit common to both transmitted and

received signals is the feed to the element aperture, the element microwave phase shifter is placed in this position. It may be noted, using antenna reciprocity, that as before, a single phase setting will produce the same beam pointing direction on both transmission and reception, assuming a reciprocal phase shifter is used.

Dependent upon the mixer conversion loss, the inclusion of a microwave preamplifier may be necessary if a low receiver noise figure is required. Preamplification may be necessary particularly where passive diode mixers (noise figure and loss typically ~ 8dB) are used. However, as mentioned in Chapter 3, it should be noted that FET mixers can provide noise figures (presently 3 - 4dB noise figure with several dB gain at 12GHz) for which preamplification may not be necessary. For simplicity microwave preamplifiers have not, therefore, been shown in the subsequent elements, although it must be noted that these may be required where passive mixers are used.

Two obvious improvements can be made in the circuit shown in Fig. 6.3. Firstly, it is clearly undesirable to provide two separate microwave distribution networks for the reference, locking signal and for the local oscillator signal. In the pulsed mode of operation, these signals are not required simultaneously and thus a single distribution network may be used for both signals. Secondly, it is undesirable to position the phase shifter in the element aperture feed, since its loss will both reduce the transmitted power and increase the receiver noise figure. Since a single distribution network is again used, the phase shifter may again be placed in the input to the element, as shown in Fig. 6.4.

On transmission, in the circuit of Fig. 6.4, the switch is used to

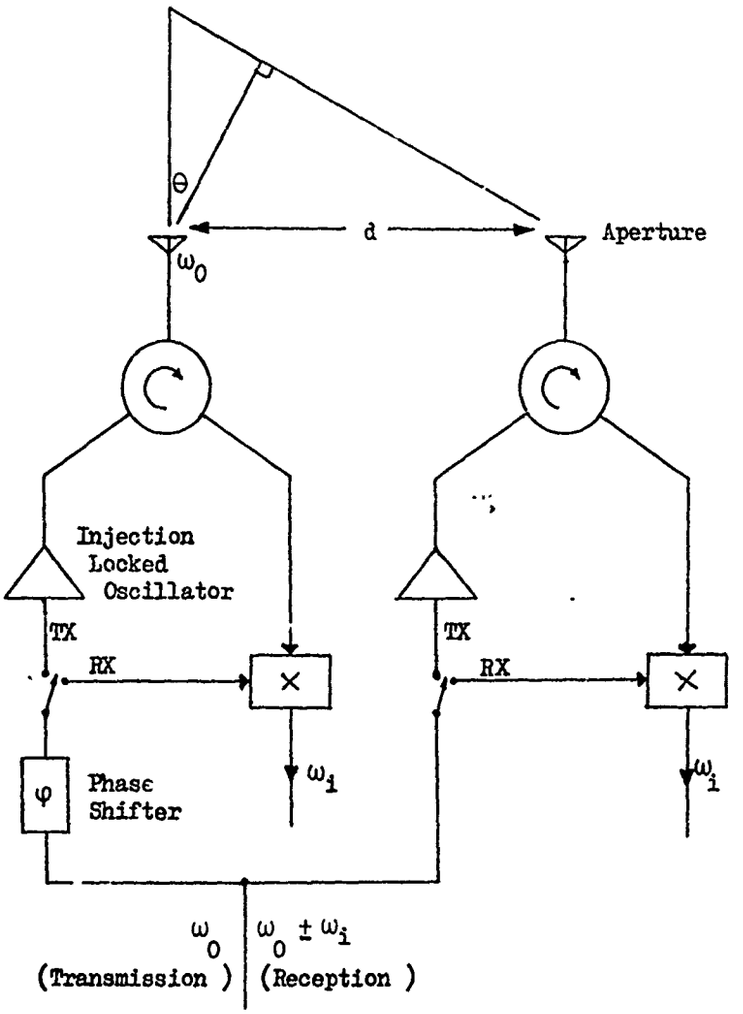


Fig. 6.5 A Two Element Array for Demonstration of the Phase Reversal Requirement Between Transmission and Reception

apply the locking signal distributed to the array, at angular frequency ω_0, to the oscillator for the period of the pulse length. Subsequently, on reception, the element oscillator is inactive and the switch is used to apply the distributed signal, now at frequency $\omega_0 \pm \omega_i$, where ω_i is the intermediate frequency, to the mixer local-oscillator input. When the loss of reference signal and local oscillator power is acceptable, the use of a passive network such as a directional coupler or power splitter may be preferred to the switch, since this will avoid the additional input to the element required for the switch control.

One slight disadvantage of this element circuit is that a phase change is required between transmission and reception to produce the same beam-pointing angle in the two cases. This is demonstrated in the following analysis.

Consider the two element array shown in Fig. 6.5. The injection locked oscillators are simply represented here as amplifiers since they do not influence this aspect of the element operation. Consider a relative phase shift $+\varphi_t$ applied to the left hand element on transmission. The injection locked oscillators will amplify the input signals at frequency ω_0, and neglecting any phase error introduced by the oscillators, the amplified signals will be transmitted with in-phase addition in a direction Θ given by

$$\Theta = \sin^{-1}\left[\frac{\lambda\varphi_t}{2\pi d}\right] \qquad \ldots\ldots 6.2$$

where Θ is the angle measured clockwise from the broadside position

λ is the wavelength

d is the inter-element spacing.

On reception we wish to find the value of phase shift that must now be applied to the left hand element to form the receive beam in the same direction, when the local oscillator frequency is (a) greater than the transmitted frequency ω_0 (i.e. $\omega_0 + \omega_i$), (b) less than the transmitted frequency (i.e. $\omega_0 - \omega_i$).

Consider a relative phase shift $+\varphi_r$ applied to the local oscillator signal of the left hand element on reception. Taking the phase of the signal received in the right hand element as the phase reference, the signals received from direction θ in the left and right hand elements may be expressed as

$$A\sin\left(\omega_0 t - \frac{2\pi d\sin\theta}{\lambda}\right) \quad \text{and} \quad A\sin(\omega_0 t)$$

respectively, where A represents the amplitude of the received signal voltages. Taking first the case (a), where the local oscillator frequency is greater than the transmitted frequency, the voltages after downconversion are

$$KA\sin\left(\omega_i t + \varphi_r + \frac{2\pi d\sin\theta}{\lambda}\right) \quad \text{and} \quad KA\sin(\omega_i t)$$

in the left and right hand elements respectively, where the factor K represents the conversion loss. It may be seen that these voltages are in phase when

$$\varphi_r + \frac{2\pi d\sin\theta}{\lambda} = 0 \qquad \ldots 6.3$$

Substituting for Θ from Eqn. 6.2 we obtain

$$\varphi_r = -\varphi_t \qquad \text{.. 6.4}$$

Secondly, taking the case (b) where the local oscillator frequency is less than the transmitted frequency, the element voltages after downconversion are

$$KA\sin(\omega_i t - \frac{2\pi d\sin\Theta}{\lambda} - \varphi_r) \quad \text{and} \quad KA\sin(\omega_i t)$$

in the left and right hand elements respectively. It may be seen that these voltages are in phase when

$$-\frac{2\pi d\sin\Theta}{\lambda} - \varphi_r = 0$$

giving, as before

$$\varphi_r = -\varphi_t \qquad \text{..... 6.5}$$

Thus in either case, the sign of the phase shift must be reversed between transmission and reception to maintain the same beam-pointing direction.

The addition of another mixer to the element circuit could be used to provide a fixed change of sign of the local oscillator signal phase (i.e. spectrum inversion); however, the expense and complexity of this would not be justified, since the only effect of the sign reversal requirement is to impose a minimum range restriction corresponding to the phase shifter switching time. As described

in Chapter 2, typical switching times for PIN and ferrite phase shifters are 50ns - 2μs and 1 - 5μs respectively. Taking the minimum pulse width as twice the switching time τ_s, the minimum range R_{min} is given by

$$R_{min} = \tau_s c \qquad \text{.....6.6}$$

where c is the velocity of propagation, 3×10^8m/s. Taking a typical value of τ_s as 1μs, R_{min} is 300m.

It must be borne ir mind that ferrite phase shifters, which generally exhibit longer switching times, are often non-reciprocal. Since phase switching between transmission and reception will then be required for any of the element circuits, the same minimum range restriction will apply in all the cases considered.

6.2.2 Design with Several Injection Locked Oscillator Stages

As previously noted, the limited gain available from single injection locked oscillator stages may result in more than one stage being required in an element circuit, particularly if it is desired to use solid state sources to generate the array locking and local oscillator signals. With respect to the circuit shown in Fig. 6.4, an additional locked oscillator following that shown could clearly be included with no change to the element operation, although consideration would have to be given to their combined phase error. If only particularly low levels of locking and local oscillator signal power were available, however, it is of interest to consider an element in which the local oscillator signal is also amplified within each element, as shown in Fig. 6.6. The first locked oscillator in this element serves to amplify both the local oscillator signal and the

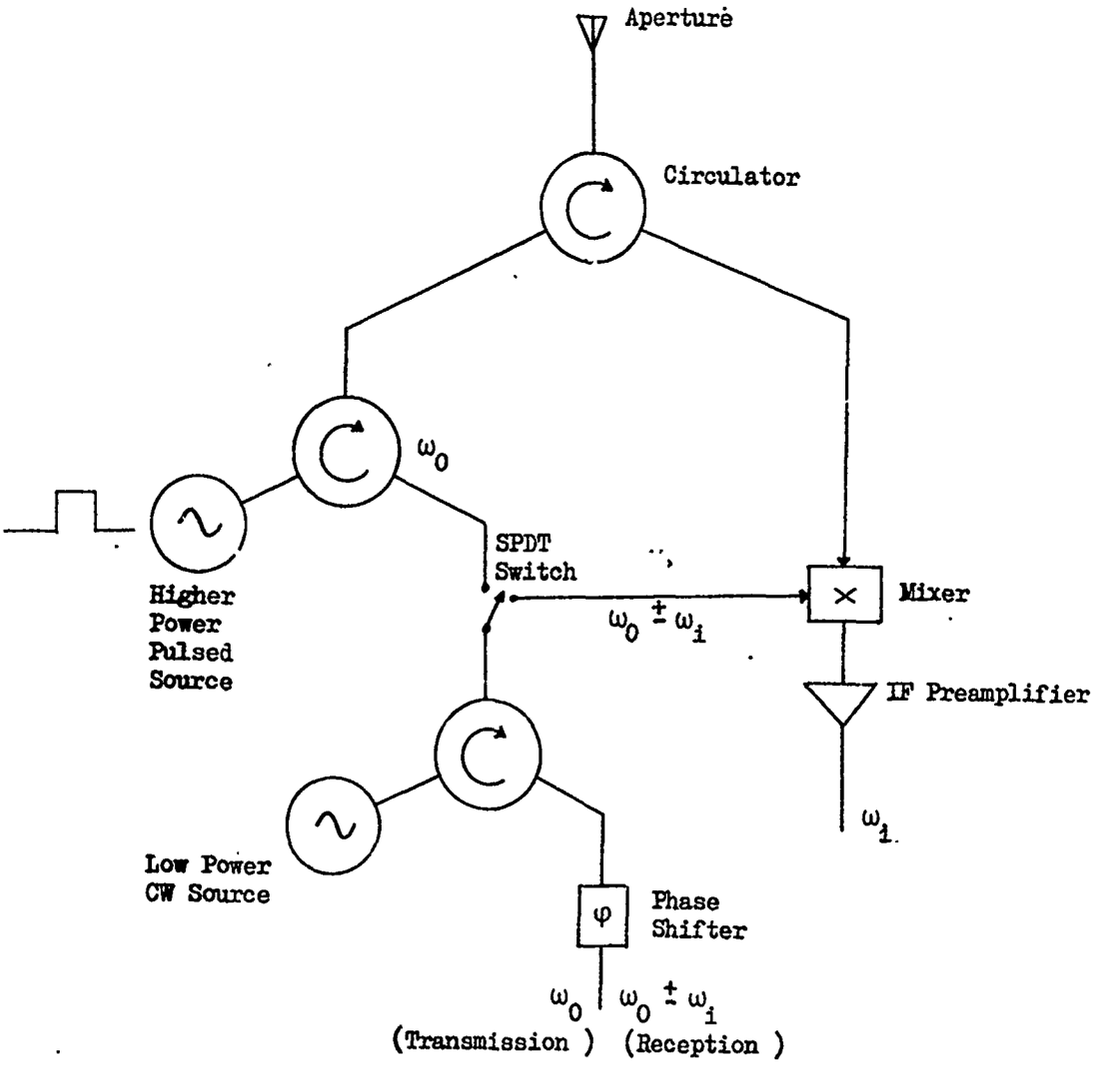


Fig. 6.6 Element Providing Amplification of Both the Local Oscillator and Transmitter Signals

signal for transmission, and thus operates continuously. The second oscillator which is operated on transmission only is a higher power pulsed source.

Three aspects require consideration in this design.

1) The minimum range of the radar will be dependent on the time required for the element to switch from transmission to reception modes. In addition to the phase shifter switching time, the time required for the locked oscillator to change frequency must now also be considered.

2) Consideration must now be given to the additional noise introduced on the local oscillator signal by the locked oscillator.

3) Phase errors introduced by the locked oscillator will now have an effect on both transmission and reception.

Minimum Range Restrictions due to the Locked Oscillator Response Time

The time required for an injection locked oscillator to respond to a sudden change of frequency of the locking signal may be obtained from the theory for the acquisition transient previously described in Chapter 4. For the case in which the locking signal is applied after steady state oscillations are established, the approximate worst case acquisition time, corresponding to an initial phase error close to the unstable equilibrium position, was given in Chapter 4 as

$$t = \frac{10}{\Delta\omega_L}$$

where $\Delta\omega_L$ is the locking range (i.e. half the synchronisation

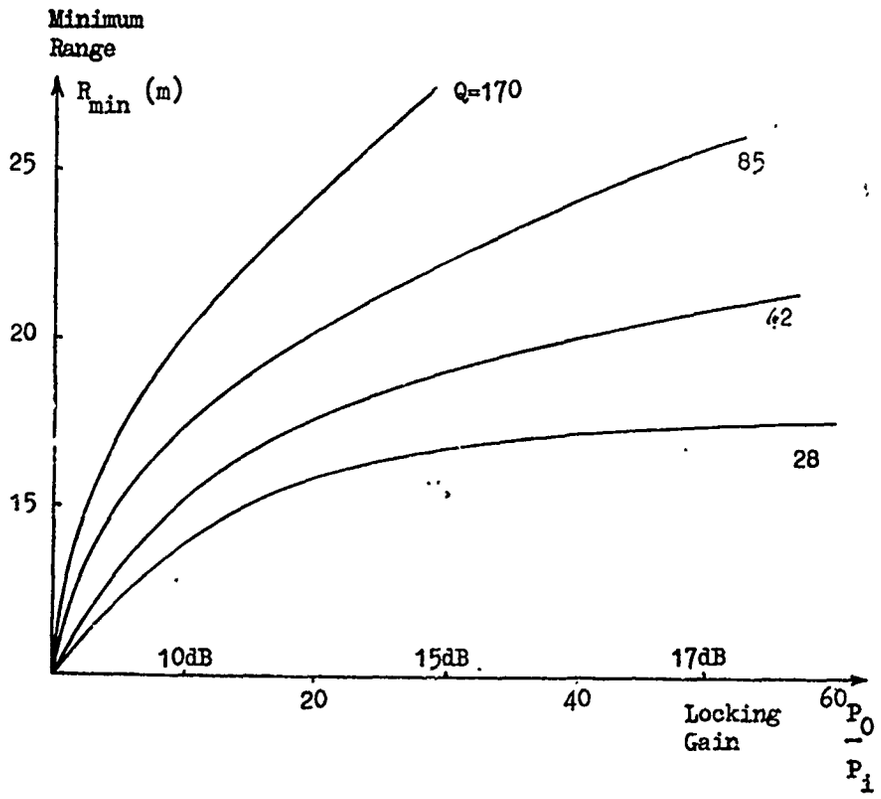


Fig. 6.7 Variation of Minimum Range due to the Locked Oscillator Response Time

range). The reference locking signal and the local oscillator signal for the array will, in general, be derived from separate switched sources, and assuming rapid switching, the form of the locked oscillator transient will be the same as that for acquisition. Taking a worst case time for the oscillator to relock to the locking or local oscillator signal as $10/\Delta\omega_L$, and assuming the minimum pulse length is twice this value, the minimum range, using Eqn. 6.6 is given by

$$R_{min} = \frac{10c}{\Delta\omega_L} \qquad \ldots\ldots 6.7$$

From Eqn. 4.3

$$\Delta\omega_L = \frac{\omega_0}{Q}\sqrt{\frac{P_1}{P_2}}$$

Hence Eqn. 6.7 becomes

$$R_{min} = \frac{30.10^8.Q}{\omega_0}\sqrt{\frac{P_2}{P_1}} \qquad \ldots\ldots 6.8$$

The variation of minimum range with locking gain for various values of Q is shown in Fig. 6.7. Noting that values of locking gain greater than ~10dB cannot be used (a) since the oscillator locking range must be large enough to contain both the transmission and local oscillator frequencies and (b) to restrict the variation of phase error between elements, it may be seen from the figure that the restriction on the minimum range due to the locked oscillator response time is much less than that due to typical phase shifter switching times.

The Effect of the Locked Oscillator Noise on Reception

The AM and FM noise levels on the output of an injection locked oscillator are given by (34) , (49)

$$\left(\frac{N}{C}\right)_{SSB}^{AM} \approx \frac{kTBN_0/2P_2}{1 + (Q\,\omega_m/\omega)^2} \qquad \ldots 6.9$$

$$\approx \frac{kTBN_0}{2P_2} \quad \text{for } \omega_m \ll \frac{\omega}{Q} \qquad \ldots 6.10$$

and

$$\left(\frac{N}{C}\right)_{SSB}^{FM} \frac{(\Delta\omega_r)^2 + \Delta\omega_0(\omega_m/\Delta\omega_L)^2}{2\left[1 + (\omega_m/\Delta\omega_L)^2\right]\omega_m^2} \qquad \ldots\ldots 6.11$$

where $\Delta\omega_0 = \frac{\omega_0}{Q}\sqrt{\frac{kTBN_0}{P_2}}$ ..6.12

and where $\left(\frac{N}{C}\right)_{SSB}$ is the single-sideband noise power to carrier power ratio

$kTBN_0$ is the noise output of the free running oscillator in bandwidth B

k is Boltzmann's constant

T is the ambient temperature

N_0 is the oscillator noise measure

ω_m is angular frequency of interest measured with respect to the oscillator frequency

$\Delta\omega_r$ and $\Delta\omega_0$ are the r.m.s. frequency deriviations of the reference source and of the unlocked oscillator

P_2 is the oscillator output power

and $\Delta\omega_L$ is the locking range.

Since these levels for typical solid state sources will often be greater than those present on a local oscillator signal derived from a low noise (e.g. crystal controlled) source the effect of the increased noise level must be considered.

It may be noted initially that the FM noise present on the local oscillator input to the mixer will not alone give a downconverted noise output. In simple terms it may be considered that only a single frequency is present at any instant and mixing with itself (with no delay) will only produce DC and harmonic terms. FM noise present on the local oscillator signal will, however, produce equivalent FM noise sidebands on the downconverted received signal. If low frequency components of the FM noise produce pulse to pulse phase variations on the downconverted signal, it is clear that these may be confused with those produced by target motion. It is therefore desirable to minimise the FM noise within the range of possible Doppler shifts. As previously noted in Chapter 4, when $\omega_m \leqslant \Delta\omega_L$, Eqn. 6.11 reduces to

$$\left(\frac{N}{C}\right)_{SSB}^{FM} \approx \frac{(\Delta\omega_r)^2}{2\omega_m^2} \qquad \ldots\ldots 6.13$$

Thus for $\omega_m \ll \Delta\omega_L$ the locked oscillator takes on the FM noise character of the locking source, which may then be designed to be of a low level.

AM noise terms present on the oscillator output <u>will</u> produce a downconverted signal at the desired intermediate frequency due to rectification. The downconverted noise level may be minimized by the use of a balanced mixer which will typically produce a downconverted noise power 20dB below the input noise power in a given

bandwidth. The downconverted noise power will appear on the element output in addition to that predicted by the receiver noise figure and thus may necessitate an increase in the gain of a possible preamplifier to preserve the desired element signal to noise ratio. Taking typical figures for a 10GHz Gunn oscillator with noise measure of 35dB, output power of 10mW and locking Q ($\approx$ loaded Q) of 100, Eqn. 6.9 gives the AM noise to carrier ratio in 1KHz bandwidth at frequency 60MHz from the carrier as $\approx$ -120dB. Assuming 20dB loss is introduced by a balanced mixer this gives a downconverted noise power at the mixer output of -130dBm in 1KHz bandwidth. This must then be compared to the noise power at this point derived from the conventional noise figure calculations to determine the value of preamplifier gain required.

Two final points regarding the effects on noise require comment. First, the AM noise outputs of the array locked oscillators will not exhibit any correlation from element to element and thus in the combiner the downconverted noise powers will add only in r.m.s. fashion, as described in Chapter 5. Secondly, if a power splitter or directional coupler is used to replace the switch in Fig. 6.6, consideration must also be given to the AM noise entering the mixer via the leakage path around the circulator. The use of a T/R switch would clearly avoid the problem.

Phase Errors Introduced by the Locked Oscillator

As previously described, the values of phase error within the linear region ($\sin\varphi_e \approx \varphi_e$) Eqn. 4.144 may be used to find the permissible spread in values of oscillator free running frequency given a maximum acceptable value of variation in phase error between

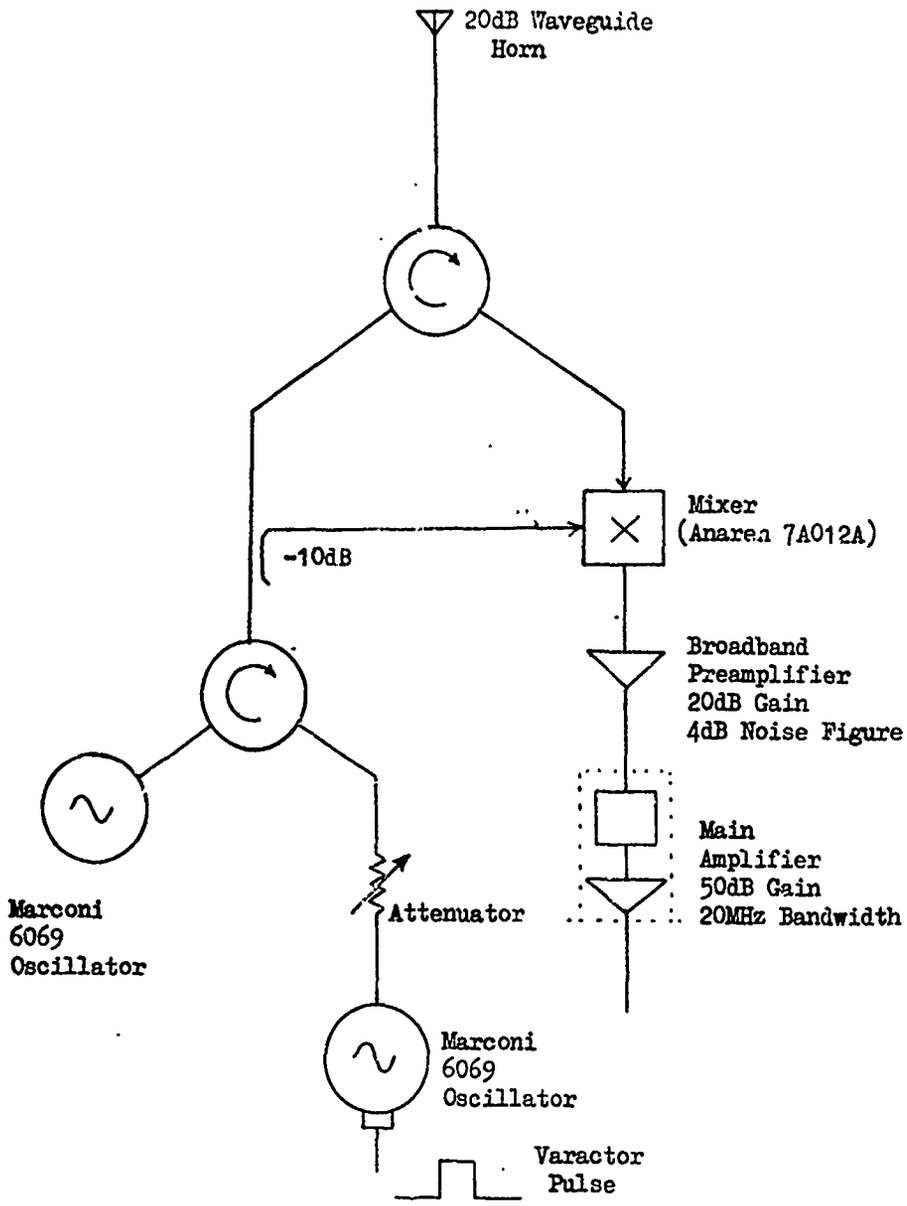


Fig. 6.8 Experimental Element Circuit

elements. The first locked oscillator in the circuit of Fig. 6.6 must be able to lock to both the transmitted and the local oscillator frequencies and phase error will be introduced onto both of these signals. As long as the phase errors in both cases are within the linear region, however, Eqn. 4.144 may still be applied. It may be noted that the absolute values of phase error introduced on transmission and reception may be significantly different (e.g. 20 - 30°) but if the errors are the same for all elements there will be no effect on the array radiation pattern.

Since the rate of change of phase error with detuning $\Delta\omega$ increases rapidly outside the linear region, it is clear that a large value of locking range should be used for the first oscillator to bring both the locking frequencies into the linear phase error region. From Eqn. 4.3 this implies the use of both low locking gain and low Q for this oscillator.

Experiments Justifying the Minimum Pulse Width Relation

Some simple experiments were carried out with a single element to demonstrate the feasibility of the design shown in Fig. 6.6.

The element circuit used is shown in Fig. 6.8. For simplicity the second, pulsed oscillator was omitted from the circuit, as was a microwave preamplifier preceeding the passive mixer, since the principal desire was to examine only the behaviour of the first locked oscillator with the frequency switched locking signal. Again for simplicity, a directional coupler was used instead of a switch to couple some of the locked oscillator output power to the mixer local oscillator input. The element thus radiated continuously in this

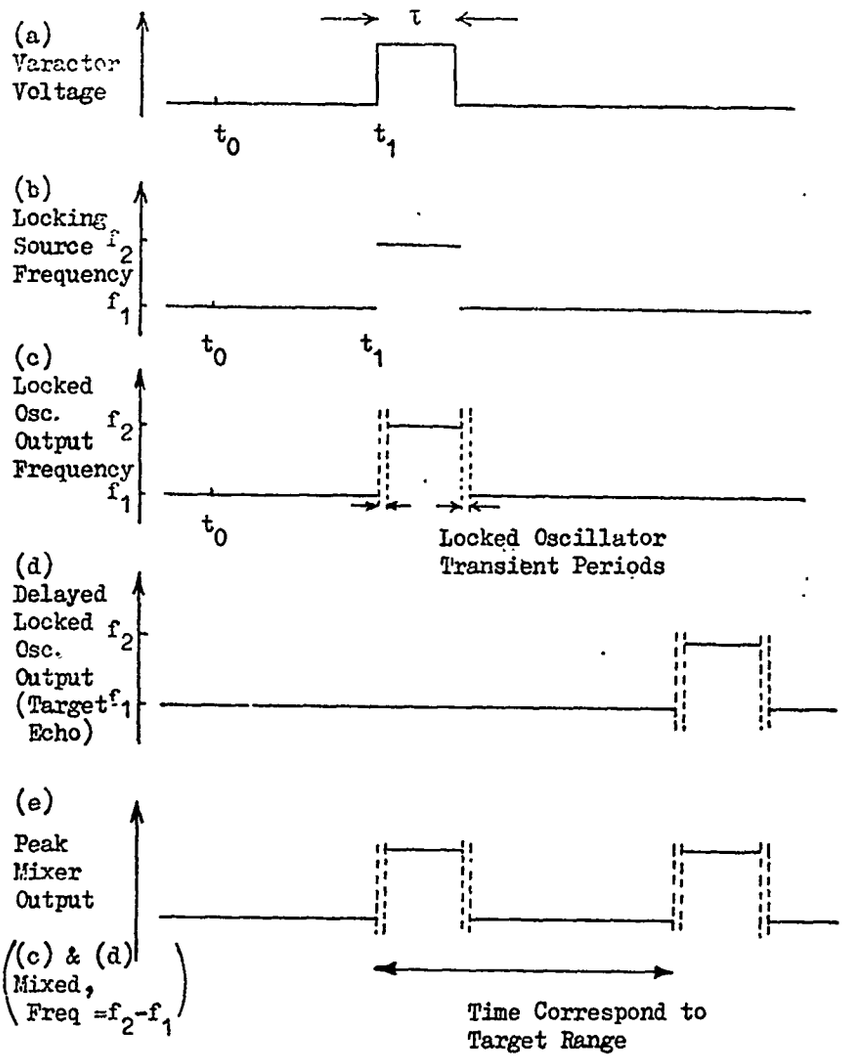
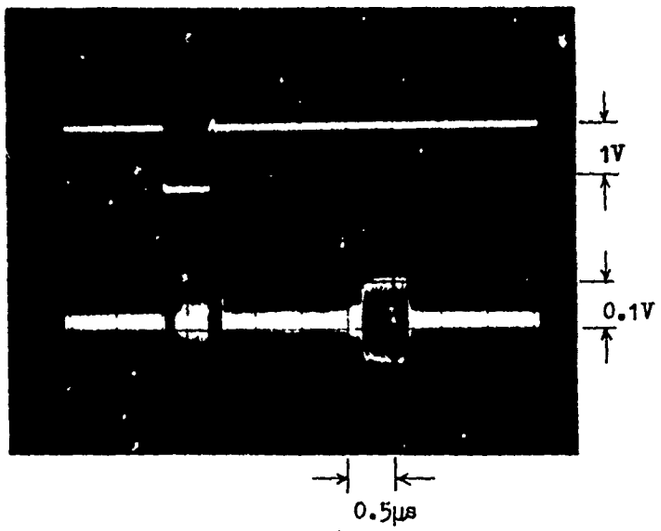


Fig. 6.9 Description of the Experimental Circuit Operation

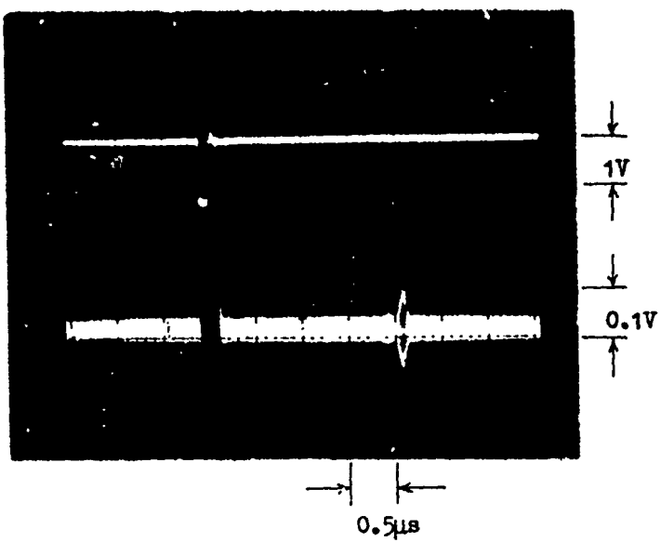
case.

The locking source took the form of a 10mW varactor tuned Gunn oscillator (Marconi type 6069) in these simple experiments. A pulse applied to the varactor of this oscillator was used to change the locking signal frequency between transmission and reception. The same oscillator type was also used as the element source, providing 10mW output power at a frequency $\sim$ 10GHz.

The operation of the experimental circuit may be most simply explained with reference to Fig. 6.9. At time t_0 the locking source varactor voltage shown in (a) is low. The locking signal frequency (b) is f_1 and assuming this is within the synchronisation range of the locked oscillator, the output frequency of this oscillator (c) will also be f_1. A signal at this frequency is thus radiated and also applied to the mixer local oscillator input. Assuming no target echoes at frequencies other than f_1 are received at this time, there will be no mixer output at the I.F. frequency other than noise. At time t_1 a pulse of duration τ is applied to the locking source varactor, with amplitude resulting in a change of the locking signal frequency to f_2. With a maximum response time given approximately by $10/\Delta\omega_L$, the locked oscillator will follow the step change in frequency, assuming f_2 is also within the oscillator synchronisation range. With the local oscillator frequency at f_2 an IF output at frequency $f_2 - f_1$ will be produced for approximately the pulse length τ due to target returns of the signal previously radiated for a long period at f_1. At the end of the pulse the locking signal and locked oscillator frequencies return to value f_1, and mixer IF output pulses will then be produced at any subsequent time corresponding to round trip delays to possible targets, of the radiated pulse of frequency f_2.



(a) 0.5μs Pulse Length



(b) 100ns Pulse Length

Fig. 6.10 Locking Source Varactor Voltage and Element IF Output for 0.5μs and 100ns Pulse Lengths

The IF output will then be as shown in Fig. 6.9 (e).

In the experimental element f_1 = 9.836GHz. A value of f_2 was chosen to give an intermediate frequency of 60MHz, suitable for use with the available IF amplifiers, i.e. f_2 = 9.896 GHz. With the element oscillator locking Q of 170, a low value of locking gain was required to give a synchronisation range large enough to encompass both frequencies. A locking gain of 5dB was used, yielding a synchronisation range of $\approx$ 64MHz for an output power of 10mW and a locking power of 3.1mW. It may be noted that in a practical array with MIC elements, oscillator Qs much less than 170 would be used (e.g. typically 10 - 20), thereby providing considerably higher values of gain for the same synchronisation range. The maximum oscillator response time, approximated by $10/\Delta\omega_L$ (N.B. $\Delta\omega_L = \Delta\omega_s/2$) was $\approx$ 50ns.

Assuming a noise measure N_0 of 35dB for the Gunn oscillator, and ambient temperature T of 273°K the AM noise to carrier ratio at 60MHz from the carrier with the rather larger receiver bandwidth of 20MHz was calculated from Eqn. 6.9 to be - 79dB. With respect to 1W, the AM noise power in this bandwidth is - 99dBW. In the experimental circuit, in which a single-balanced mixer was used (Anaren type 7A0128) the AM noise accompanying the leakage in the reverse direction around the circulator would have produced a higher level of downconverted noise than that present on the local oscillator signal, since there was no suppression of noise on the ' signal ' input to this mixer. For a circulator leakage level of - 20dB relative to the transmitted power, the AM noise power due to the locked oscillator, appearing at the mixer input was - 119dBW in 20MHz bandwidth. This was of the same order as that referred to this point after calculation of the usual receiver noise figure. Taking a mixer noise figure and gain

of 8dB and .155 respectively, a preamplifier noise figure and gain of 4dB and 20dB respectively, and a main amplifier noise figure and gain of 10dB and 50dB respectively, gives an overall noise figure of 13.5dB. The noise power referred to the input is then - 117.5dBW.

The experimental results obtained with the element are shown in Fig. 6.10(a) and (b). The photographs show radar operation of the single element against a building target at a range of 300m. In both cases the upper trace shows the voltage pulse applied to the varactor of the locking source, producing a frequency step of 60MHz on the locking line. The lower traces show the element IF outputs, which are similar to that sketched in Fig. 6.9(e). The expected 60MHz pulsed output at approximately 2μs delay may be clearly seen. The pulse length used in the upper photograph is 0.5μs; in the lower photograph the pulse length is reduced to 100ns, demonstrating that operation down to pulse lengths equal to twice the locked oscillator maximum response time (50ns) may be achieved. Taking the measured value of signal return loss of - 80dB (path loss + reflection loss) the S/N ratio calculated on the basis of the above noise theory should be 17.5dB. This is in reasonable agreement with the measured value of 15dB.

Application of the Harmonic Locking Technique

Finally in this section, the use of the harmonic locking technique to the design of Fig. 6.6 must be mentioned. The harmonic locking technique was described in Chapter 2 and is based on the fact that the output phase of an oscillator injection locked to a signal at the nth harmonic of the output fundamental frequency may take one of n possible values with respect to a fixed phase reference. The harmonically locked oscillator may therefore be used as a digital

phase shifter when the phase position of the output can be controlled.

The use of microwave harmonic locking in an active transmitting array was described by Al-Ani et al[14]. On transmission the use of harmonic locking is straightforward ; the harmonically locked oscillator simply replaces the conventionally locked element source, the locking signal now being at the nth harmonic of the element output. On reception a harmonically locked oscillator clearly cannot be included in the signal path, and thus to provide reception phase shifting, the phase shifts present on a harmonically locked oscillator output must be induced on the received signal via a mixing process.

The element design shown in Fig. 6.6 is particularly suitable for the use of harmonic locking. The harmonically locked oscillator now replaces the first locked oscillator and the phase shifter. The element locking signal will now be at the nth harmonic of the transmitter frequency on transmission and at the nth harmonic of the desired local oscillator frequency on reception.

Phase switching times of $\sim$ 40ns have been reported [29] from a harmonically locked oscillator thus no increase in the minimum range would be expected from the use of this technique.

Although attractive in that the conventional microwave phase shifter is avoided, the harmonic locking technique suffers from two drawbacks : (1) immediately after switch-on or after a disturbance, the output phase state of the oscillator will be unknown. It will therefore be necessary either to monitor the oscillator output phase continually, or periodically relock the oscillator at its

fundamental frequency to re-establish a known phase state. (2) the size of the phase increment produced by an injection locked oscillator is given by 360/n degrees, where n is the harmonic number. To provide 3 bit phase shifting (45° increments) will require locking to the 8 harmonic ; to provide 4 bit phase shifting will require locking to the 16th harmonic. If 4 bit phase control is required in a 10GHz array, a reference signal at 160GHz will need to be distributed to the array. This would clearly be very difficult and thus the harmonic locking technique applied directly at microwave frequency will generally be only applicable to low microwave frequency arrays.

6.3 Conclusions

Injection locking represents a simple and straightforward means of oscillator synchronisation. Its main drawback stems from the level of phase error that will be introduced by the inevitable spread in the values of free running frequency that will exist in an array of sources. To minimize the variation in phase between elements only low values of locking gain (of the order of that obtainable from single stage microwave amplifiers) can be used. Higher gains may be obtained only when particular care is taken to reduce the spread of detuning e.g. by temperature stabilisation of the array, or the use of feedback techniques such as that shown in Figs. 4.4 and 4.5.

Of the element designs considered in this Chapter, that of Fig. 6.2 is the most attractive where a microwave combining network is used, and that of Fig. 6.4 the most attractive for an IF combining network. Although the sign of the phase shift must be reversed between

transmission and reception in this design, this is not seen as a disabling problem.

In all the designs microwave phase shifters are required, although it was noted that the harmonic locking phase shifting technique could be adopted with the circuit of Fig. 6.6 for relatively low microwave frequency applications.

The circuit of Fig. 6.6 is suitable for the special case where the locking signal and local oscillator inputs to the element are both at low level and require amplification within the element. The experimental results, some of which are also described in reference (50) , have demonstrated the feasibility of this approach for a single 10GHz element.

CHAPTER 7

ACTIVE ELEMENTS BASED ON THE PHASE-LOCKED LOOP

7.0 Introduction

In contrast with the last chapter, in which element designs based on the use of injection locked element sources were described, in this chapter attention is given to elements based on the use of phase-locked loops. The points raised in section 6.0.1, however, concerning the general approach to the active element design, also apply to this chapter.

Elements can be formed using either a straightforward PLL with a single input, or with a heterodyne loop ; however those based on the latter have the attraction of offering IF control of the element phase and thus these are given more attention. A number of element designs based on the HPLL are possible and these are described in turn. The relative merits of the designs are considered in the chapter summary.

Reference is made to the summary at the end of Chapter 4 for a review of the characteristics of phase-locked loops.

7.1 Active Elements based on the Simple PLL with Single Input

The simple PLL in which there is only a single microwave locking signal input may, in most cases, be used as a direct replacement for the injection locked oscillator in the designs considered in the last chapter. Only the circuit of Fig. 6.1 is unsuitable, since the single circulator in this case was used both to decouple the input and output signals of the locked oscillator and also to isolate the inactive oscillator from the received signal path on reception. The use of the simple PLL in the two circuits of most interest in

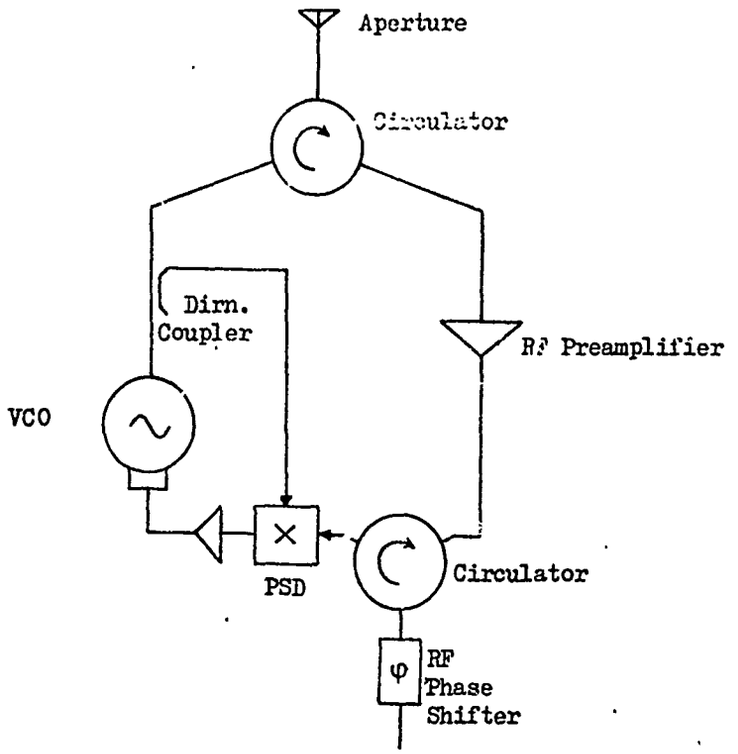


Fig. 7.1 Application of the Simple Phase-Locked Loop to Replace the Injection Locked Oscillator in the Circuit of Fig. 6.2.

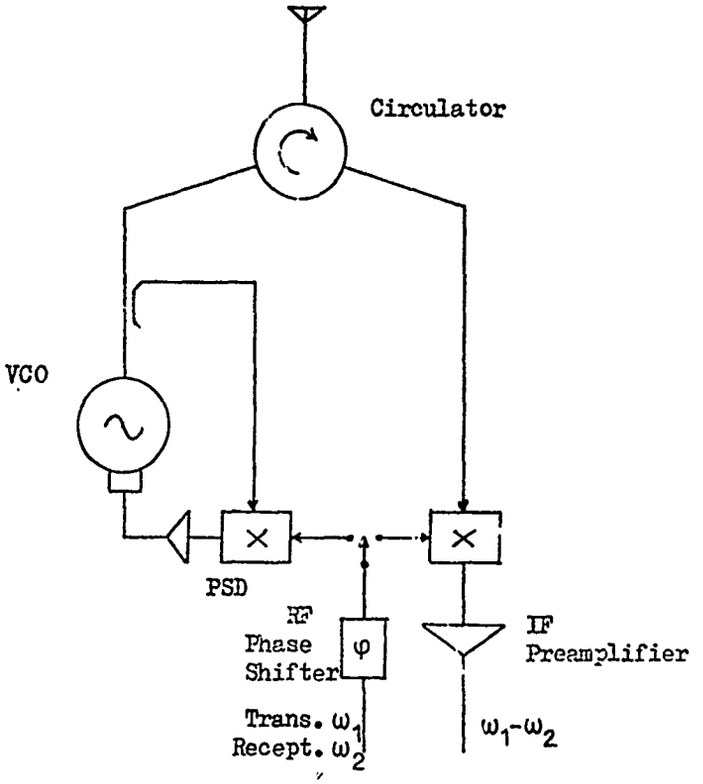


Fig. 7.2 Application of the Simple Phase-Locked Loop to Replace the Injection Locked Oscillator in the Circuit of Fig. 6.4

Chapter 6 is shown in Figs. 7.1 and 7.2. A directional coupler is used in these designs to sample a fraction of the VCO output for the loop feedback signal. The maximum coupled power required is only of the order of a few mW where passive diode mixers are used, and this will generally be only a very small fraction of the total VCO output (e.g. tens of Watts). The reference signal power required at each element will similarly be of the order of a few mW.

Clearly, the factors considered in Chapter 6 with regard to these circuits, concerning losses, and frequency and phase switching between transmission and reception also apply when PLLs are used. The main advantages of the use of PLLs in these cases are related to the higher locking gain that may be used, and the lower variation in element phase due to differences in the source free-running frequencies. The designs are still restricted to use with microwave phase shifters however, and the designs described in the following sections based on the heterodyne PLL are generally more attractive.

7.2 Active Elements Based on the Heterodyne Phase-Locked Loop

The attraction of the HPLL lies in its ability to provide phase control of the microwave VCO output simply via the phase of the IF input ; phase shifts applied to the IF reference input transfer directly (though with a possible change of sign) to the microwave output. An IF phase shifter is thus used to replace the conventional microwave type for electronic beam steering in the following element designs.

There are several advantages in the use of IF phase shifters.

1) The high cost of PIN and ferrite microwave phase shifters was previously noted in Chapter 2, and is demonstrated by the very small

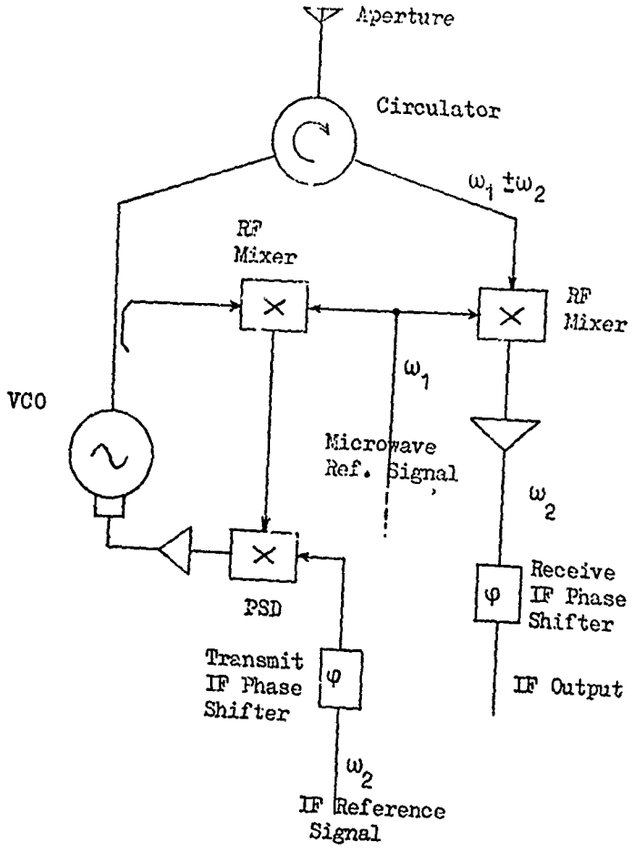


Fig. 7.3 Element Design with Separate IF Phase Shifters on Transmission and Reception

number of phased arrays, active and passive, that have reached a production stage of development. IF phase shifters, which are often based on low frequency implementations of the hybrid coupled phase shifter described in Chapter 2, will in general be simpler to manufacture and hence be less expensive than microwave types. A novel IF phase shifter, particularly suited for use in these elements and which should also be of relatively low cost is described in Chapter 8.

2) Lower amplitude and phase tolerances should be obtainable with an IF approach. It was shown in Chapter 5 that the radiation pattern sidelobe level of an array is related to the level of amplitude and phase errors existing on the elements. A lower sidelobe level may then be possible with IF phase shifters.

3) The drive power required for IF phase shifters should generally be significantly less than that required for RF types.

In all the designs considered, the use of an IF combining network has been assumed. The advantages of this were discussed in section 6.2, but an additional factor influencing the decision in this case is that an IF feed network must be provided on transmission for the distribution of the IF reference signal to the elements ; in many cases it will be possible to use a single network to also act as an IF combining network on reception.

7.2.1 Element Designs with Separate Signal Paths for the Downconversion of the Loop Feedback and Received Signals

In these designs the HPLL circuit is isolated from the received signal path. Separate RF mixers are used to downconvert the loop feedback and the received signals to IF.

Design with Separate Phase Shifters for Transmission and Reception

A first approach to the inclusion of a HPLL in a transmit and receive, active element could take the form shown in Fig. 7.3. The HPLL is used to synchronise the VCO to the sum or difference of the two reference input frequencies at ω_1 and ω_2. Since it is undesirable that two possible locking conditions should exist simultaneously, the tuning range of the VCO is restricted in practice to cover only one of these. The required power of each of the reference signal inputs to the element is of the order of a few mW. An IF phase shifter, placed in the IF input to the element, is used to provide phase control of the VCO output for beam steering.

On reception, a separate mixer, preamplifier and phase shifter are included in the element. Where passive mixers are used, microwave preamplification may again be required, but for simplicity this is again not shown. The microwave reference locking signal is now conveniently used also as a local oscillator signal for reception with no change of frequency required. The downconverted IF output of the element is then at the same frequency as the IF reference signal.

Since amplification is provided within the element on transmission and reception, feed network losses, both RF and IF, will not be of first importance here.

Design with a Single Phase Shifter and IF Feed Network.

Since, in the pulsed mode of operation, the separate phase shifters and feed networks shown in Fig. 7.3 are not used simultaneously, a clear reduction in the circuit complexity and cost can be achieved

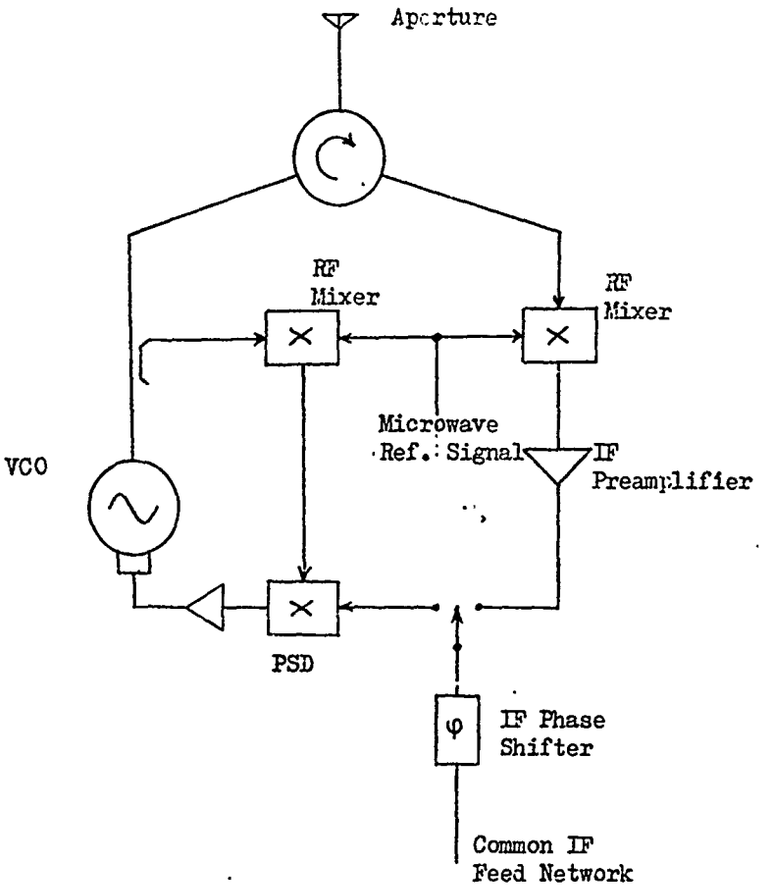


Fig. 7.4 Element Design with a Single IF Phase Shifter and Feed Network Used on Both Transmission and Reception

by using a single phase shifter and feed network for both transmission and reception. This circuit is shown in Fig. 7.4. The switch is used to apply the phase shifted IF reference signal to the HPLL on transmission, and connects the element IF output to the phase shifter and summing network on reception.

The performance of this element will clearly be very similar to that of Fig. 7.3, except that a minimum range restriction may now be present associated with the switch transient time. It is clearly of interest to ascertain whether the phase shifter setting must also be changed between transmission and reception since the switching time required for this can also effect the minimum range. The analysis below follows the same lines as that given in Chapter 6, section 6.2.1.

Consider the two element array shown in Fig. 7.5 where θ, the steering angle, is measured clockwise from the broadside direction. With reference to Chapter 4 it was previously noted that with the VCO of a HPLL synchronised to the sum of the microwave and IF input frequencies, a phase shift $+\varphi$ applied to the IF input will result in a phase shift $+\varphi$ on the VCO output ; with the VCO synchronised to the difference of the input frequencies, a phase shift $+\varphi$ applied to the IF input will result in a phase shift $-\varphi$ on the VCO output. Taking first the case for sum frequency synchronisation, consider a phase shift $+\varphi_T$ applied to the IF input of the left hand element on transmission. The VCO output of the left hand element at frequency $\omega_1 + \omega_2$ will similarly be phase shifted by $+\varphi_T$, resulting in in-phase addition of the element outputs (ignoring any phase errors present in the elements) in a direction

$$\theta = \sin^{-1}\left(\frac{\varphi_T \lambda}{2\pi d}\right) \qquad ..7.1$$

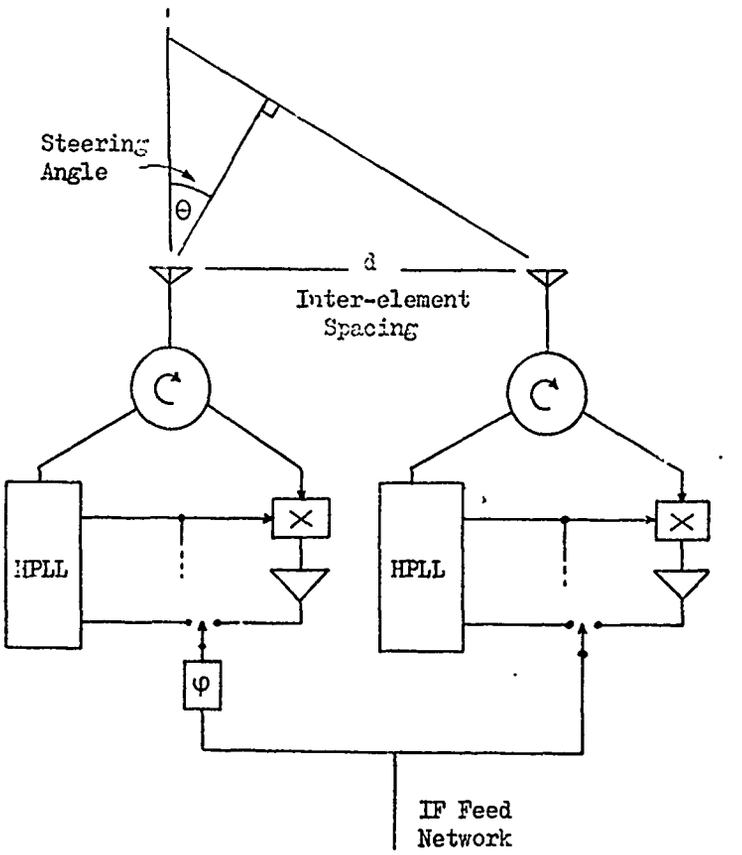


Fig. 7.5 A Two Element Array Used to Determine Beam Steering Angles

where λ is the free space wavelength

and d is the interelement spacing.

We now wish to find the phase shift φ_R that must be applied to the left hand element to give the same beam pointing direction on reception. Taking the phase of the signal received in the right hand element as a reference, the signals received at frequency $\omega_1 + \omega_2$ from direction θ in the left and right hand elements respectively are

$$A \sin\left[(\omega_1 + \omega_2)t - \frac{2\pi d \sin\theta}{\lambda}\right] \text{ and } A \sin\left[(\omega_1 + \omega_2)t\right]$$

where A represents the signal amplitudes.

After mixing with a local oscillator signal at frequency ω_1 with an assumed zero phase, the downconverted and amplified signals within the elements, now at frequency ω_2 are

$$AK \sin\left[\omega_2 t - \frac{2\pi d \sin\theta}{\lambda}\right] \text{ and } AK\sin(\omega_2 t)$$

in the left and right hand elements respectively. The factor K represents the overall mixer/amplifier gain. After phase shift $+\varphi_R$ is applied to the left hand element output we have

$$AK \sin\left[\omega_2 t - \frac{2\pi d \sin\theta}{\lambda} + \varphi_R\right] \text{ and } AK\sin(\omega_2 t)$$

These signals are in-phase when

$$-\frac{2\pi d \sin\theta}{\lambda} + \varphi_R = 0 \qquad \ldots\ 7.2$$

i.e. $$\varphi_R = \frac{2\pi d \sin\theta}{\lambda} = \varphi_T \qquad ..7.3$$

Thus no change of sign is required between transmission and reception in this case to maintain the same beam-pointing direction.

Taking secondly the case for difference frequency synchronisation, a phase shift $+\varphi_T$ applied to the IF input of the left hand element on transmission, will produce on the VCO output a phase shift $-\varphi_T$. The VCO outputs will be in-phase in a direction θ given by

$$\theta = \sin^{-1}\left(\frac{-\varphi_T\lambda}{2\pi d}\right)$$

$$= -\sin^{-1}\left(\frac{\varphi_T\lambda}{2\pi d}\right) \qquad \ldots 7.4$$

i.e. in a direction exactly opposite broadside from that obtained before.

We wish now to find again the phase shift that must be applied to the left hand element to produce the same beam-pointing direction on reception. Following the same procedure as before, the signals received from direction θ given in Eqn. 7.4 in the left and right hand elements respectively are

$$A\sin\left[(\omega_1 - \omega_2)t - \frac{2\pi d\sin\theta}{\lambda}\right] \quad \text{and} \quad A\sin\left[(\omega_1 + \omega_2)t\right]$$

where again the phase is referred to that of the signal received in the right hand element.

After downconversion and amplification we obtain in the left and right elements respectively

$$AK\sin\left[\omega_2 t + \frac{2\pi d\sin\theta}{\lambda}\right] \quad \text{and} \quad AK\sin(\omega_2 t)$$

After phase shift $+\varphi_R$ is applied to the signal in the left hand element we obtain

$$AK\sin\left[\omega_2 t + \frac{2\pi d\sin\theta}{\lambda} + \varphi_R\right] \text{ and } AK\sin(\omega_2 t)$$

These signals are in phase when

$$\varphi_R + \frac{2\pi d\sin\theta}{\lambda} = 0$$

$$\text{i.e.} \quad \varphi_R = \frac{-2\pi d\sin\theta}{\lambda} = \varphi_T \qquad \ldots.7.5$$

Thus as before, no phase shifter switching is required between transmission and reception. The only limitation on the minimum range due to the array elements is thus the switch transient time, which could typically be down to a few tens of ns.

Design with the Phase Shift Induced on the Received Signal by Mixing

This design, the last of the three element circuits considered in this section, is applicable

a) where it is desired to avoid the use of a switch (+ associated drivers) within the element, or more important

b) where it is desired to use a uni-directional phase shifter, in particular the harmonically locked PLL phase shifter described in Chapter 8.

The element circuit for this case is shown in Fig. 7.6. On transmission the VCO is synchronised to the sum or difference of the input signals, as before. On reception the signal after downconversion and amplification is simply mixed with the phase shifted IF reference signal, producing the desired phase shift on the output at the.

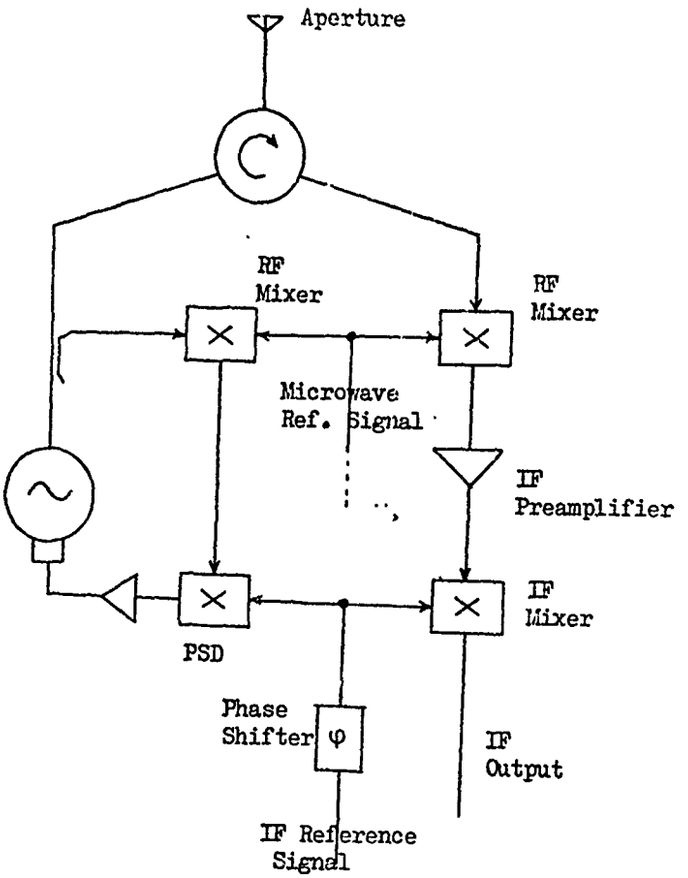


Fig. 7.6 Element Design with the Phase Shift Introduced on Reception by Mixing

sum of the mixer input frequencies.

Two aspects require attention in this design. First it is necessary to establish the phase shift that must be applied to maintain the same beam-pointing direction on transmission and reception. Secondly the level of undesired mixer products must be considered.

A full analysis of phase shifts required on transmission and reception can be avoided by noting the similarity between this circuit and the last one considered, shown in Fig. 7.4. Since the only difference between these circuits lies in the use of a second mixer the result previously obtained i.e. that no change of phase is required between transmission and reception for either sum or difference frequency synchronisation, will also be true for this circuit if no change of sign is introduced by the second mixer. This will clearly be the case when the sum frequency mixer output is taken as the element output since the output phase is simply the sum of the two input signal phases.

The most straightforward operation of the circuit will be when the RF and IF reference signal frequencies remain the same for both transmission and reception. For RF and IF reference frequencies ω_1 and ω_2 respectively the downconverted signal on reception, neglecting any Doppler shifts, will be ω_2 and hence the sum frequency output of the second mixer will be $2\omega_2$. Since practical mixers, in addition to the desired mixing products, also generate harmonics of the input signals, care must be taken in this case that the signal output of the mixer at $2\omega_2$ is not obscured by the second harmonic of the local oscillator signal also generated by the mixer.

To prevent this the amplifier preceding the second mixer must provide sufficient gain to amplify the minimum detectable signal in the element to a level at the output greater than that due to local oscillator second harmonic generation. To illustrate the magnitude of gain typically required, consider an element with simply an RF mixer (i.e. no microwave preamplification) of 8dB noise figure and - 8dB gain, followed by an IF amplifier of noise figure 2dB and gain G, followed by the IF mixer again with 8dB noise figure and - 8dB gain.

It is assumed that the minimum detectable signal in the element is equal to the element noise level in the receiver bandwidth, taken in this case as 10MHz. (It may be noted that for an array of elemen the minimum detectable signal at the element stage is in fact less than the element noise level due to coherent addition of the signal powers and the incoherent addition of the noise powers. This fact is ignored, however, in this simple calculation).

The overall noise figure of the element F, from Friis's formula is

$$F = 6.3 + \frac{0.585}{0.158} + \frac{5.3}{0.158G} \qquad \ldots.7.6$$

$$= 10 + \frac{33.5}{G}$$

The effective noise power at the input is given by

$$kTB$$

where k is Boltzmann's constant

B is the bandwidth

and T is the equivalent noise temperature at the input

$= (F-1).290^{\circ}K$

At the second mixer output the noise power is

$$.025GkTB$$

$$= 10^{-16}(9F + 33.5) \text{ Watts}$$

in 10MHz bandwidth.

Experimental measurements have demonstrated that suppression of the local oscillator second harmonic output of up to 60dB may be achieved with balanced mixers i.e. the second harmonic output power is 60dB below the local oscillator input power.

Assuming a typical local oscillator power of 5mW and 60dB suppression the second harmonic power at the output is 5×10^{-9}W. This is equal to the output noise power when

$$(9G + 33.5)\ 10^{-16} = 5 \times 10^{-9}$$

Thus the required gain in this case is

$$G = 5.5 \times 10^{6}$$

$$= 67.4\text{dB}$$

It will clearly be undesirable to include such high levels of amplification within each array element. This can be simply avoided however, by providing a slight frequency change of the RF input on reception, so that the output signal and local oscillator harmonic frequencies are no longer coincident. The gain required will then be simply that necessary (e.g. 20dB) to prevent significant degradation of the element noise figure by the mixer losses.

It may be noted that a particularly useful feature of this design is that the operating frequency of the phase shifter may be maintained at a fixed value. The frequency change between transmission and reception mentioned above, and also the linear change of frequency required on transmission for FM pulse compression, may both be applied via the RF reference signal. The IF reference frequency (i.e. the phase shifter operating frequency) may thus be maintained at a fixed value for transmission and reception. Since the phase shifter may be set up for single frequency operation, lower-phase variations between elements should be achievable with this design compared to one in which broadband phase shifting is required. In the circuit of Fig. 7.4 for instance, the IF phase shifter on reception must operate over a range of received frequencies, e.g. 10MHz where FM pulse compression is used. If an IF of 100MHz is chosen this represents a requirement for a consistent phase shift over a 10% bandwidth, which may be difficult to achieve in practice.

Both of the circuits of Fig. 7.4 and 7.6 are thus of interest. The circuit of Fig. 7.4 has the advantage of simplicity and requires only a single IF feed network. Its disadvantages are that switching is required within the element between transmission and reception, and that a wide bandwidth phase shifter may be required. The circuit of Fig. 7.6 has the advantages of permitting a uni-directional phase shifter, such as that described in Chapter 8, to be used, and also permits the phase shifter to be operated at a single frequency. Its disadvantages are the need to change the reference frequency between transmission and reception in order to avoid the leakage problem ; the loss introduced in the element by the additional mixer and the use of two feed networks, although in practice a single network

with suitable filtering to separate the IF reference and the received signals would probably be used.

7.2.2 Element Designs with a Common Signal Path for the Downconversion of the Loop Feedback and the Received Signals

With the aim of reducing the number of components required in the element, and thus the element cost, it is of interest to examine techniques for further simplifying the designs previously considered. It may be noted in each of the three previous designs, that in pulsed operation, the RF mixer used to down-convert the loop feedback signal is inactive on reception ; similarly the RF mixer used to down-convert the received signals is inactive on transmission. Element designs can thus be considered in which a single RF mixer is used to perform both functions. A number of circuits using this approach are possible, as described below. One aspect of all these circuits is that mutually coupled signals between the array elements can influence the HPLL performance on transmission. This aspect is examined in Section 7.3.

Design with Separate Transmit and Receive Phase Shifters

A first approach to an element using only a single RF mixer is shown in Fig. 7.7. This is essentially a simplification of the circuit of Fig. 7.3. On transmission the RF and IF reference inputs are present as before. The feed-back fraction of the VCO output, previously provided by a directional coupler, is now provided by the leakage in the reverse direction around the circulator, thus a usually undesirable feature of practical circulators is used here to advantage. The leakage power is typically one hundredth of

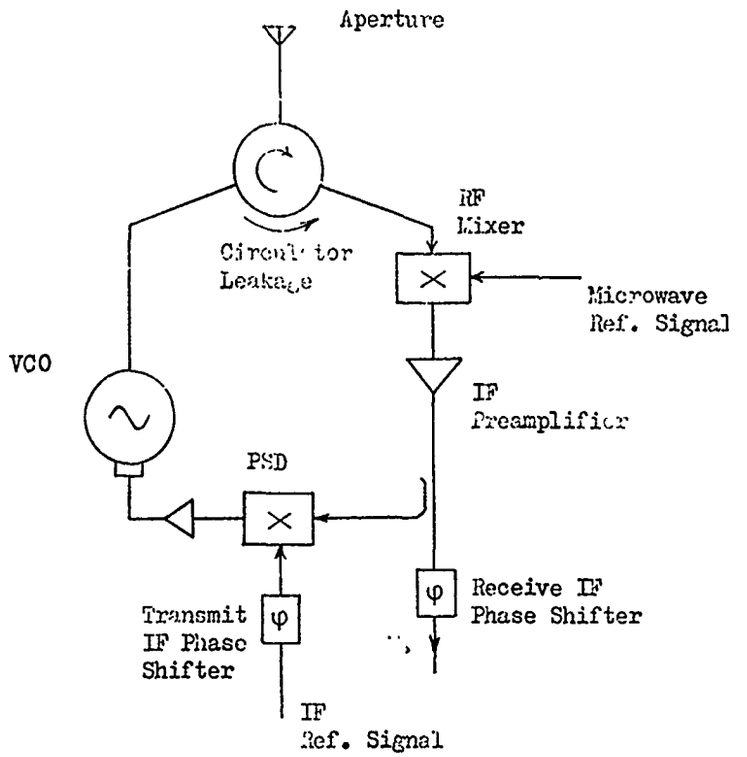


Fig. 7.7 Element Design with Separate Phase Shifters for Transmission and Reception

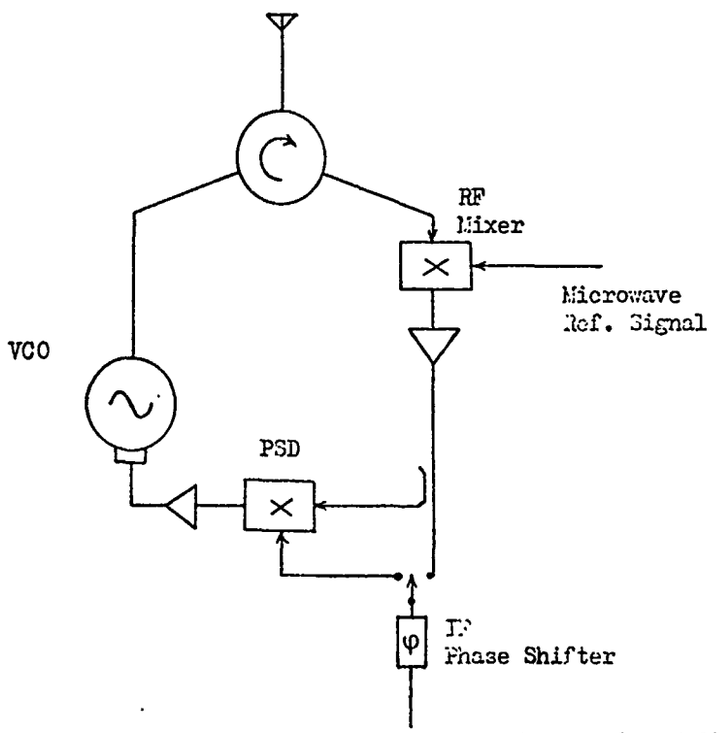


Fig. 7.8 Element Design with a Single IF Feed Network and Phase Shifter Used on both Transmission and Reception

that passed in the forward direction (i.e. - 20dB relative to forward power). The reflection from passive element apertures (e.g. dipoles, or open ended waveguides) may in fact be at a similar power level and thus the signal appearing at RF mixer on transmission will be a combination of these components. This feed-back signal is then downconverted to IF and subsequently applied to the phase sensitive detector along with the phase shifted IF reference signal. Thus the loop is completed and the VCO can be locked to the sum or the difference of the input signals as before. An IF directional coupler is used to apply some of the downconverted feedback signal to the PSD since this is a simple passive component ; a SPDT switch could alternatively be used in this position when it is desired to maximise the feedback signal applied to the PSD in order to increase the locking range. Also, it may be necessary to remove (via a switching arrangement) the amplifier from the down - converted signal path on transmission,a) to avoid the introduction of the amplifier group delay into the HPLL, since this will reduce the available loop bandwidth as described in Chapter 4, and b) to avoid the recovery time often required for amplifiers operated under saturated output conditions before normal operation is re-established. Typical recovery times measured experimentally with a type SL550 integrated circuit IF amplifier were of the order of several μs. The presence of an amplifier recovery time can set an additional constraint on the minimum radar range.

On reception the VCO is inoperative and the reception path, consisting of the downconverting mixer, amplifier and reception phase shifter, is the same as that for Fig. 7.3 neglecting the directional coupler (or SPDT switch, if this is used instead).

Design with a Single Phase Shifter and IF Feed Network Used on Both Transmission and Reception

A clear reduction in the element cost and complexity can be made by using a single phase shifter and IF feed network for both transmission and reception. This circuit is shown in Fig. 7.8 and is analogous to that given in Fig. 7.4. On transmission the switch applies the phase shifted IF reference signal to the PSD to lock the element VCO ; on reception the switch connects the amplifier IF output to the element phase shifter and IF combining network. It may be noted comparing Figs. 7.4 and 7.8 that the phase relationships between the reference inputs and the VCO output on transmission are the same in the two cases. Similarly the relationship between the reference signal phases and the IF output is the same on reception. The result previously established for Fig. 7.4 therefore also applies to this design i.e. no change of sign of the phase shift is required to produce the same beam-pointing direction on transmission and reception, for either synchronisation to the sum or difference of the reference input frequencies. The beam-pointing direction in these two cases is still on either side of the broadside direction, however, as before.

Design with a Single Phase Shifter Contained Within the HPLL

A further circuit variation, for which no direct counterpart was considered in the section on circuits containing separate RF mixers, is shown in Fig. 7.9. The single IF phase shifter, still used on both transmission and reception, is now placed in a position such that it is within the HPLL on transmission. On reception the signal path, including downconverting mixer, amplifier and phase shifter

is the same as the last element.

The loop response to the application of a phase shift in this case may be illustrated by a qualitative description of the loop behaviour. When the VCO is locked at a fixed frequency equal to the sum, or difference of the two reference frequencies, by definition a certain fixed value of voltage will exist at the VCO frequency control terminal. By implication a fixed phase relationship will therefore exist at the PSD between the IF reference input and the downconverted feedback signal. If a phase shift $+\varphi$ is applied to the downconverted feedback signal within the loop, then in order to remain locked, the VCO must change its output phase by an amount that will produce an equal and opposite phase shift on the downconverted feedback signal. This will then re-establish the required phase relationship at the PSD. When the VCO is synchronised to the sum of the input signals, the VCO output frequency is greater than that of the RF reference and the downconverted feedback phase is directly proportional (i.e. with no change of sign) to the VCO phase. Thus a phase shift $-\varphi$ introduced in the loop in this case will result in a phase lead $+\varphi$ appearing on the VCO output.

It was demonstrated in the analysis with sum frequency synchronisation for the circuit of Fig. 7.4 however, that the same phase shift must be applied to the downconverted received signal as is applied to the VCO output signal to give the same beam-pointing direction. This will clearly not occur in this design without a change of sign of the phase shift applied between transmission and reception. This result may also be shown to exist for the case of synchronisation to the difference of the reference frequencies.

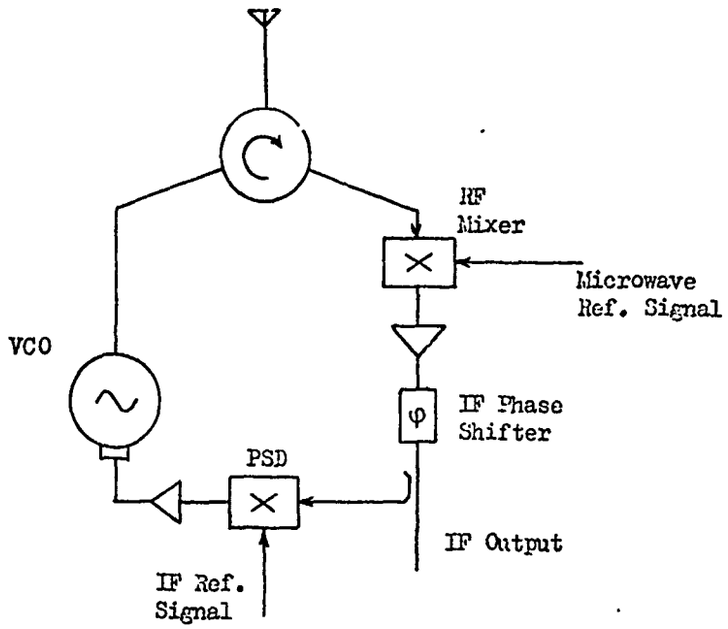


Fig. 7.9 Element Design with the Phase Shifter Contained within the Heterodyne Phase-Locked Loop

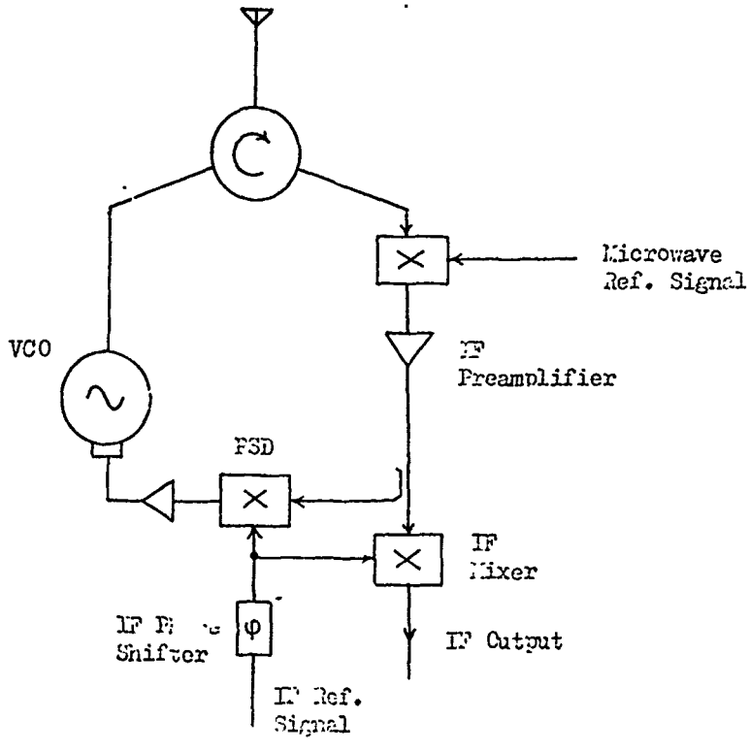


Fig. 7.10 Element Design with the Phase Shift Introduced on Reception by Mixing

Since a change of sign of phase shift is required in this element between transmission and reception, and in addition any phase shifter group delay will reduce the available loop bandwidth, this design is considered to be less attractive than that in Fig. 7.8.

Design Using Two IF Mixers where Phase Shifts are Induced on the Received Signals by Mixing

The advantages of inducing the required phase shift on the received signals by mixing the downconverted signals with the phase shifted IF reference was described in the last section. A uni-directional phase shifter may be used and, in addition, single frequency operation of the phase shifter is possible. The use of this approach is shown in Fig. 7.10. This circuit is the equivalent to that shown in Fig. 7.6 where two RF mixers were used, and the same phase relationship will exist i.e. when the sum frequency product of the right hand IF mixer is used, there is no requirement for a change in the phase shifter setting between transmission and reception. Also in common with the circuit of Fig. 7.6 it may be noted that when the reference signal frequencies are the same on transmission and reception, the received signal may be obscured by the second harmonic of the IF reference signal generated by the IF mixer. As before, this problem may be simply overcome by changing one of the reference signal frequencies on reception (preferably the RF reference, since a single operating frequency can then be maintained for the IF phase shifter) ; the IF reference signal second harmonic and the received signal output frequency will then not be coincident.

Alternatively, to avoid the frequency change on reception, a fixed frequency offset could be applied to the IF reference within the

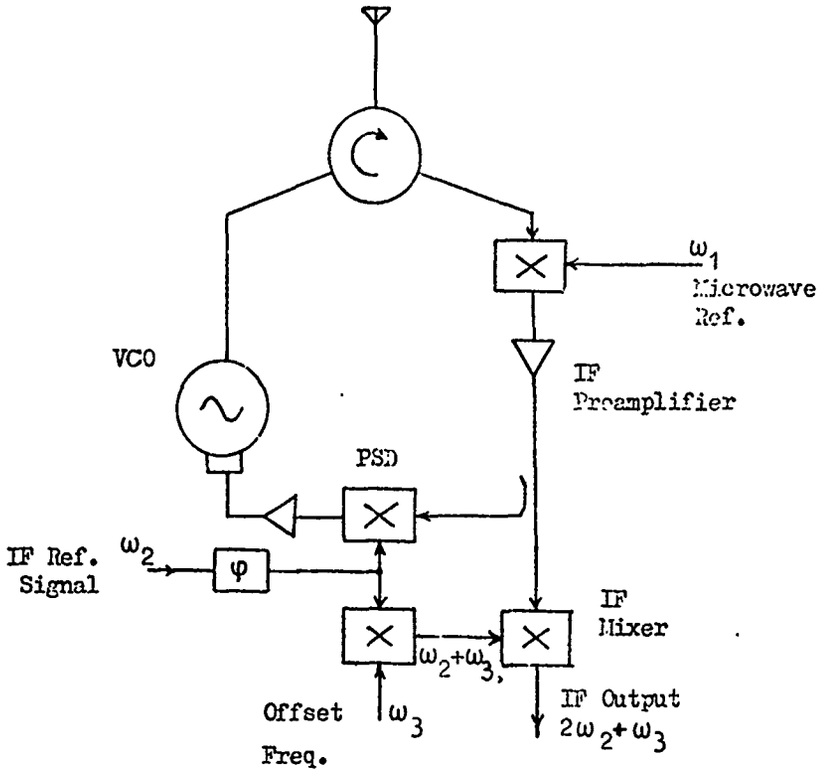


Fig. 7.11 Element Design with Frequency Offset

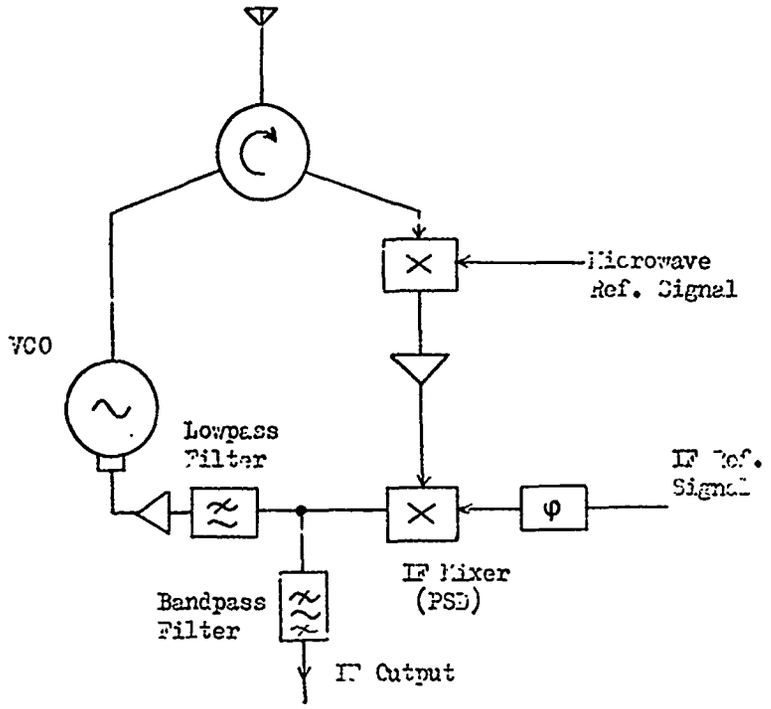


Fig. 7.12 Element Design Using a Single IF Mixer

element. This is shown in Fig. 7.11. The frequency of the signal now mixed with the downconverted received signal is the sum of the IF locking signal frequency and the offset frequency. In general it is not felt that the additional element complexity of this arrangement would be justified however ; a change of RF reference signal frequency on reception being considered less expensive to implement.

Design Using a Single IF Mixer, where Phase Shifts are Induced on the Received Signal by Mixing

Finally in this section, it may be noted that the design of Fig. 7.10 may be further simplified by using a single IF mixer, to function both as a PSD on transmission, (in which case the difference frequency mixer output is used), and as a conventional mixer on reception (in which case the sum frequency output is used). This circuit is shown in Fig. 7.12. Filters are now used to separate the sum and difference outputs of the mixer on transmission and reception. Again a reference signal frequency change will be required on reception with this circuit to avoid the second harmonic leakage problem.

The most attractive circuits of this section are those of Figs. 7.8 and 7.12, since these represent the simplest designs. The circuit of Fig. 7.12 has the advantage that a single phase shifter operating frequency can be used. This circuit was therefore chosen to experimentally demonstrate the practicability of including the received signal path within an HPLL on transmission.

The experimental arrangement used is shown in Fig. 7.13. No limiter or RF amplifier was used in these simple experiments. The VCO was a varactor tunable, waveguide Gunn oscillator (MEC type DA 8825C) which was basically designed for CW operation. In pulsed mode of operation however, a peak power of 150mW at 10.52GHz was obtained for 1μsec pulse lengths and 10KHz pulse repetition frequency. This oscillator type was also used for the experiments on the HPLL described in Chapter 4. The pulsed output was radiated via a circulator and 20dB waveguide horn antenna. The circulator leakage level was - 20dB, producing at the RF mixer input a leakage power of 1.5mW during the pulse. Following the RF mixer (Lorch type 36A) the downconverted signals were amplified in a 40dB gain, 2dB noise figure, integrated circuit amplifier (Plessey type SL550) before being applied to the IF mixer (Hewlett-Packard type 10534A), along with a 60MHz IF reference signal. At the mixer output, filters were used to direct low frequency outputs back to the VCO varactor, via an SL541C high speed, operational amplifier, whilst the output at the sum frequency was applied, via further amplification and filtering (8MHz bandwidth) to an oscilloscope. For simplicity in these experiments the IF amplifier following the RF mixer was not disconnected on transmission, and a recovery time of $\sim$ 1μs was required after the pulse, before normal low noise operation was re-established. To examine the problem of the leakage of the IF reference signal second harmonic from the IF mixer, the reference signal frequencies were not changed between transmission and reception. The second harmonic leakage and the received signal output of the IF mixer were thus both at 120MHz.

The 120MHz output obtained with the antenna pointed at building targets is shown in the upper trace in Fig. 7.14 ; the lower trace

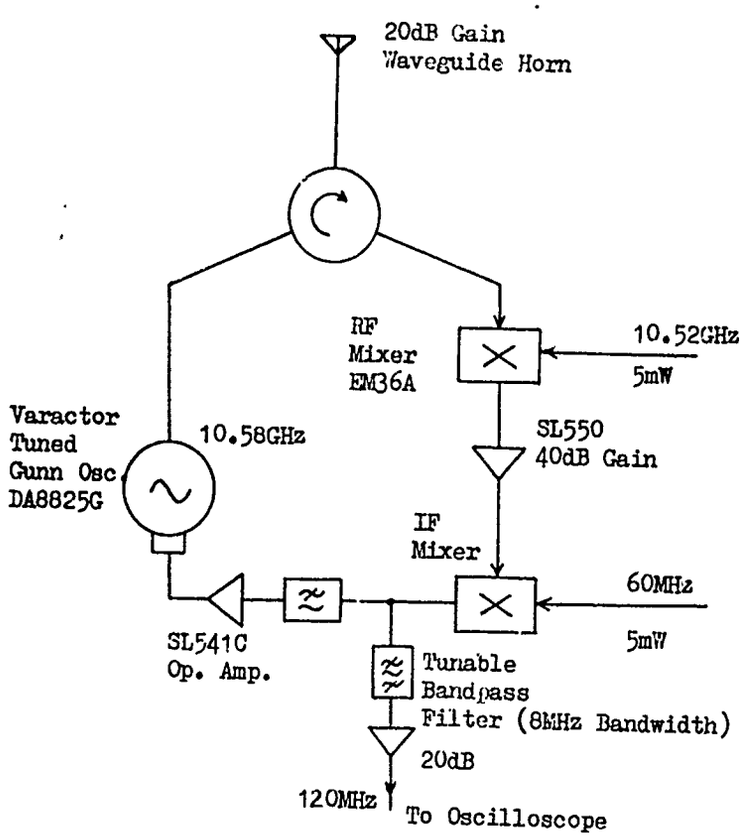


Fig. 7.13 Experimental Circuit

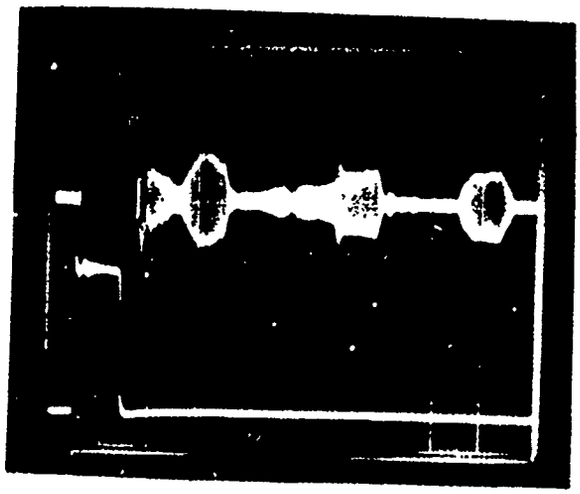


Fig. 7.14 Oscilloscope Trace

Upper Trace : Element IF Output at 120MHz

Lower Trace : Pulsed Bias Supply to VCO

shows the bias pulse applied to the VCO. For the first target, for which the round trip delay time is $\sim 2\mu s$, a received signal power 70dB less than the transmitted power was obtained. The theoretical S/N ratio on this target return, that would be obtained without the second harmonic leakage, is 47dB, assuming 8dB noise figure and - 8dB gain for the circulator/RF mixer combination, 2dB noise figure and 40dB gain for the IF amplifier and 8dB noise figure and - 8dB gain for the IF mixer. Due to the second harmonic leakage however, the measured value was only 16.8dB, in agreement with that predicted theoretically (18.5dB) taking into account the measured mixer second harmonic leakage of - 50dB with respect to a 5mW input power at 60MHz. With no leakage signal, i.e. with the IF amplifier output at 60MHz applied directly to the oscilloscope after an 8MHz bandwidth filter, building targets at ranges up to 5Km range were detected.

7.3 The Effect of Mutual Coupling in the Simplified Element Design Based on the Heterodyne Phase-Locked Loop

In the simplified HPLL element designs described in section 7.2.2, in which a single RF mixer is used both on transmission and reception, consideration must be given to the effect on the element behaviour of the mutually coupled signals between array elements. Clearly the usual mutual coupling effect will exist, i,e, a current in any one array element aperture will produce currents in the neighbouring element apertures, the overall effect of which is to produce a modification in the element radiation pattern when the element is in the array environment. However, for these elements, the total mutually coupled signal entering the element on transmission will now be applied to the RF mixer along with the desired feedback signal

from the VCO. The total phase at this point will thus be that of the composite signal. Since the loop can only lock with a specific phase of the signal applied to the RF mixer (producing a specific PSD output voltage) it may be seen that in general, the effect of mutually coupled signal will be to produce a change of the VCO output phase, that will re-establish the necessary phase value of the composite signal at the RF mixer.

The situation is quite complicated from an analytic point of view. The phase of the radiated output of any one element in the array will influence the output phase of the neighbouring elements. The subsequent changes in their output phases will, in turn, influence the phase of the first element, and the phases of the elements further along the array. All the array elements will therefore interact with each other, although since mutual coupling dimishes rapidly with distance, it would be expected that the influence of any one element will only extend over the few nearest neighbours. Clearly, when the level of the mutually coupled signal appearing at the element RF mixer is small in comparison to the desired feedback signal, (i.e. the leakage in the reverse direction around the circulator) the effect on the element output will be small ; the behaviour in this case will be similar to that of the elements described in section 7.2.1 in which the HPLL is isolated from the mutually coupled signal. For higher levels of mutual coupling, where the mutually coupled signal appearing at the RF mixer is approaching the level of the circulator leakage, it would be expected that the elements at the centre of the array will behave much as desired (since the mutual coupling environment here is constant and most of the effects of mutual coupling will be self-balancing) ; for elements near the array edges however, deviations from the desired phase distribution would be expected. When the mutually coupled signal

at the RF mixer is greater than the circulator leakage, conditions can arise in which the PLL can no longer offset the phase change introduced in the loop by the mutual coupling, and the expected behaviour becomes unclear.

Since the levels of mutual coupling typically encountered between array elements is of the order of typical circulator leakage levels, the effects of this must be considered. An analysis based on an iterative approach is given below, after a brief description of the analysis usually carried out for array elements where the mutual coupling does not affect the phase of the element source.

The Effect of Mutual Coupling Where the Coupled Signal does not Affect the Phase of the Element Source

In this case, the analysis of mutual coupling effects may be obtained with reference to the equivalent element circuit shown in Fig. 7.15. The element voltage source itself is assumed to be independent of mutual coupling, however, the mutual coupling does have an effect on the amplitude and phase of the element current and thus on the radiation pattern. The mutually coupled signal voltage at the nth element due to current I_m in the mth element is $Z_{nm}I_m$ where Z_{nm} is the mutual impedance. The impedance Z_{nn}, defined as the self impedance, would normally be equated to the source impedance Z_{gn} if no mutual coupling were present.

No electrical length is included between the generator and the aperture in Fig. 7.15 but this can be taken into account simply by an appropriate phase shift on e_n. For voltage balance

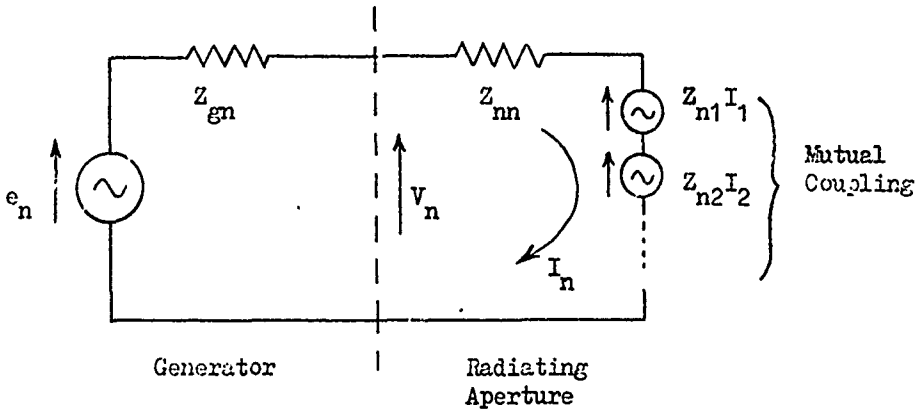


Fig. 7.15 Equivalent Circuit of an Array Element Where the Mutual Coupling Does Not Affect the Phase of the Element Source

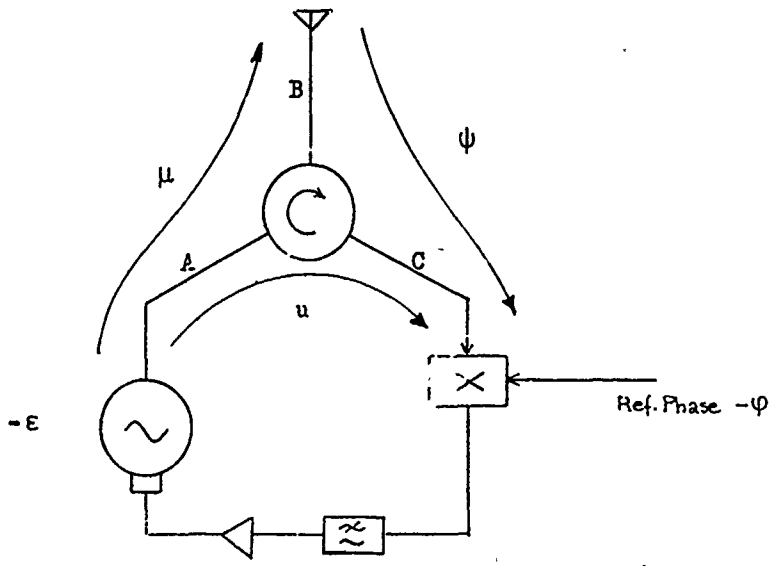


Fig. 7.16 Simplified Active Element Circuit Defining the Electrical Path Lengths

$$e_n - Z_{gn}I_n - Z_{nn}I_n - \sum_{\substack{m=1 \\ (m\neq n)}}^{N} Z_{mn}I_m = 0 \qquad \ldots 7.7$$

or, in a matrix representation

$$\left[e\right] = \left[Z\right]\left[I\right] \qquad \ldots 7.8$$

where

$$Z = \begin{bmatrix} Z_{g1} + Z_{11} & Z_{12} & \cdots & Z_{1N} \\ Z_{21} & Z_{g2} + Z_{22} & & \\ Z_{31} & \vdots & & \\ \vdots & & & \\ \vdots & & \ddots & \\ Z_{N1} & & & Z_{gN} + Z_{NN} \end{bmatrix} \qquad \ldots 7.9$$

Thus, given the voltages of the element sources, the element currents may be obtained from

$$\left[I\right] = \left[Z\right]^{-1}\left[e\right] \qquad \ldots 7.10$$

Taking these values of the array element currents, the array radiation pattern in the presence of mutual coupling can therefore be calculated.

<u>The Effect of Mutual Coupling in the Element Designs Where the Coupled Signal Affects the Phase of the Element Source</u>

The evaluation of the aperture current in these cases is less straightforward. The mutually coupled signal again arrives at each aperture and influences the element current through the effective aperture impedance. Instead of being absorbed, however, the coupled signal

appears, along with the PLL feedback signal, at the element RF mixer and thus affects the phase of the feedback signal and hence the phase of the VCO output.

Consider the simplified element based on a PLL shown in Fig. 7.16. A straightforward PLL with RF phasing (i.e. not a heterodyne PLL) is used here for simplicity.

Assuming the loop is locked, let the oscillator phase be $-\varepsilon$, so that the open-circuit source voltage may be represented (neglecting $\exp(j\omega t)$ time dependence) by

$$e_n = e_{no}\exp(-j\varepsilon) \qquad ..7.11$$

This voltage is twice the voltage measured across the load when the oscillator is delivering power into a matched load. Assuming phase shift μ is introduced by the path length to the element aperture, the source voltage referred to this point is of the form

$$\tfrac{1}{2}e_{no}\exp(-j(\varepsilon+\mu)) \qquad ..7.12$$

Two separate signals arrive at the signal port of the mixer :
1) a fraction of the oscillator output due to the leakage in the reverse direction around the circulator. This signal is of the form

$$\tfrac{1}{2}e_{no}f_R\exp(-j(u+\varepsilon))$$

where f_R represents the amplitude of the typically small fraction of the oscillator output passed by the circulator in the reverse direction ; and u is the phase lag introduced by the path length from

the source to the mixer.

2) a signal from the element aperture, due partly to the mismatch of the antenna element, and partly due to mutual coupling. The voltage at the aperture due to the forward wave, as previously noted, is of the form

$$(e_n)_{aperture} = \tfrac{1}{2} e_{no} \exp(-j(\varepsilon+\mu)) \qquad \ldots\ldots 7.13$$

With a complex reflection coefficient ρ, the reflected wave is

$$\tfrac{1}{2} \rho e_{no} \exp(-j(\varepsilon+\mu)) \qquad \ldots 7.14$$

The reflection coefficient ρ must be calculated from the radiation impedance Z_{rad}, which is obtained through

$$Z_{rad}\Big|_{\text{nth element}} = \left(\frac{e_n}{I_n}\right)_{aperture} - Z_{gn}$$

Assuming a phase lag Ψ is introduced by the path length from the aperture to the mixer, this signal referred to the mixer input is

$$\tfrac{1}{2} \rho e_{no} \exp(-j(\varepsilon+\psi+\mu)) \qquad \ldots\ldots 7.15$$

The net signal arriving at the signal port of the mixer is thus

$$\tfrac{1}{2} e_{no} f_R \exp(-j(u+\varepsilon)) + \tfrac{1}{2} \rho e_{no} \exp(-j(\mu+\varepsilon+\psi)) \qquad \ldots 7.16$$

Let this be of the form $A\exp(-jX)$. Assuming a local oscillator signal $V_1 \exp(-j\varphi)$, the DC output of the mixer will be of the form $\pm B\cos(\varphi - X)$, the sign depending on the sense of the diode connection in the mixer.

As a first step in the procedure for calculating the output phase, no mutual coupling and a perfectly matched antenna are assumed. The voltage at the signal input to the mixer is thus due to the circulator leakage alone and this will then determine the VCC output phase. Thus

$$\chi = \varepsilon + u$$

When the loop is locked, assuming for simplicity no detuning between the locking signal and the VCO free-running frequency, the inputs to the mixer will be in phase quadrature, since this condition will produce zero PSD output voltage. Assuming that the stable locking condition occurs with the feedback signal lagging the input signal by $\frac{\pi}{2}$ rad.,

$$-\chi + \frac{\pi}{2} = -\varphi$$

i.e. $$-\varepsilon - u + \frac{\pi}{2} = -\varphi$$

and thus

$$\varepsilon = \frac{\pi}{2} - u + \varphi \qquad \ldots 7.17$$

This then gives the initial value for ε. Taking this value of ε, the source phase referred to the aperture may be used to find the element currents & reflection coefficients. A new value ε' of the source phase is then obtained taking into account the leakage and mutual coupling signals as a vector sum,

$$\varepsilon' = \varepsilon + \frac{\pi}{2} + \varphi - \chi$$

The process is then repeated until convergence occurs, whereupon all element currents are determined and the array radiation pattern can be calculated using Eqn. 5.3 . A similar procedure applies to steered beams by repeating the above calculations with the appropriate value of reference phase φ applied to each element.

Bearing in mind the tedious algebra involved in the inversion of complex matrices and iterative calculations, such a procedure is most easily carried out by digital computation. The FORTRAN program used and an explanatory flow chart is given in Appendix 2.

The effect of mutual coupling in this element design may be minimised in an interesting manner by analogy with the technique of interpolation locking[12] . If the electrical path length between circulator and antenna in each element can be chosen at will, then the mutually coupled signal (including that reflected from any additional antenna mismatch) can be adjusted to arrive at the mixer input with exactly the same phase as the desired leakage signal around the circulator. The mutually coupled signals thus exactly aid the desired leakage and no phase error is introduced by mutual coupling. In general, except in the centre of a large array, the element path lengths will differ from element to element, due to asymmetries in coupling, in order to achieve this condition. The required element lengths may easily be calculated in the computer program and a routine to make both signal components arriving at the mixer have equal phase is inserted at statement [75]. It is obvious that this equi-phase condition can only apply for one phase distribution across the array and the obvious phase distribution to choose for setting up the adjustment is the broadside beam position. As the element reference phases are changed, however, to produce an approximately linear

phase variation across the array for a steered beam, the mutual coupling signal received at any element also changes in phase by approximately the same amount and the equi-phase condition for leakage and mutually coupled signals at the mixer still approximately applies. This path length adjustment technique is therefore worthwhile in such element designs.

The programme was used to compute the radiation patterns of a four element array, similar to that described in Chapter 9, using open-ended waveguide apertures. An element pattern, as given by Silver[51] was used in the computations ; values of mutual coupling, measured experimentally by Darbandi[30], were used since these also showed agreement with theoretical calculations based on the work of Rhodes[52]. Since the mutual coupling effects are very strong in an E plane array of open-ended waveguide elements, 10dB attenuation was introduced in each element feed to reduce to mutually coupled power in the experimental array to a level approximately 10dB less than that of the circulator leakage. This was simulated in the program. The computed radiation patterns are shown in Figs. 7.17, 7.18, 7.19, 7.20, these are compared in Chap' 9 with those given in section 9.2 for the experimental array.

The computer program has been written in general form and can be extended to a linear array of any number of elements if appropriate values of mutual coupling are provided. In general the computations indicated for both the four element array and larger arrays, that with mutually coupled powers less than, or even of the same order, as the circulator leakage signal, the radiation patterns will follow those which would be expected from a straightforward array in which the source phases are not influenced by mutual coupling. When the

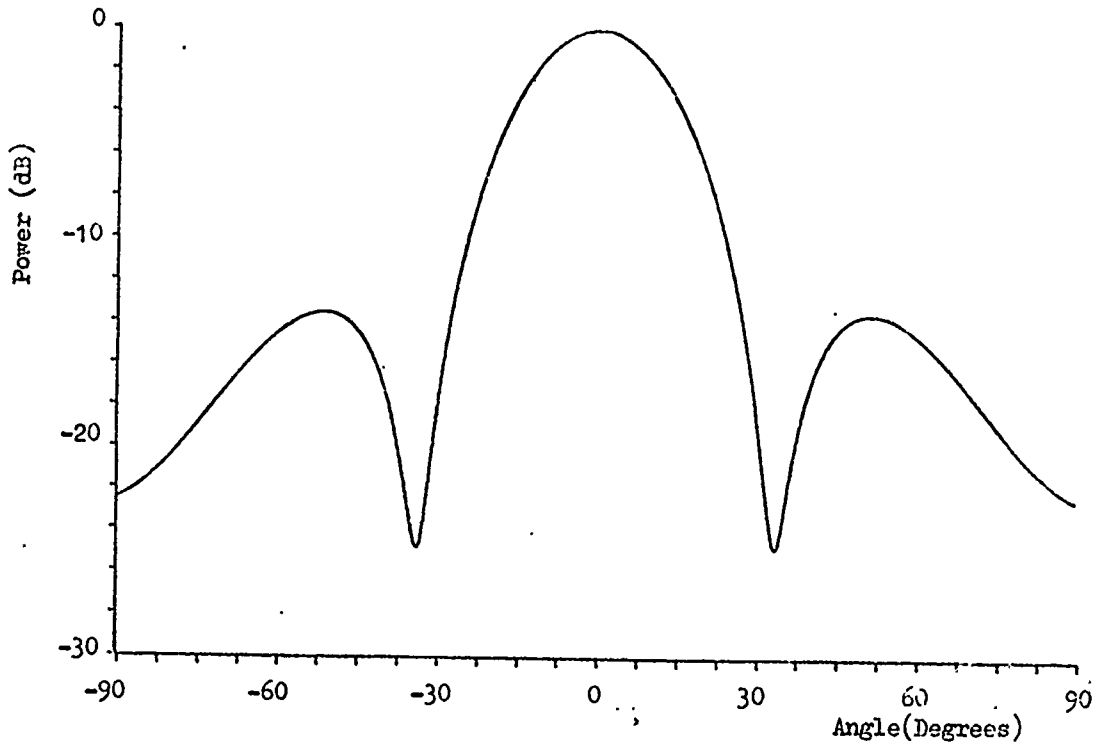


Fig. 7.17 Computed Four Element Array Pattern

Phase Settings : 0°, 0°, 0°, 0°

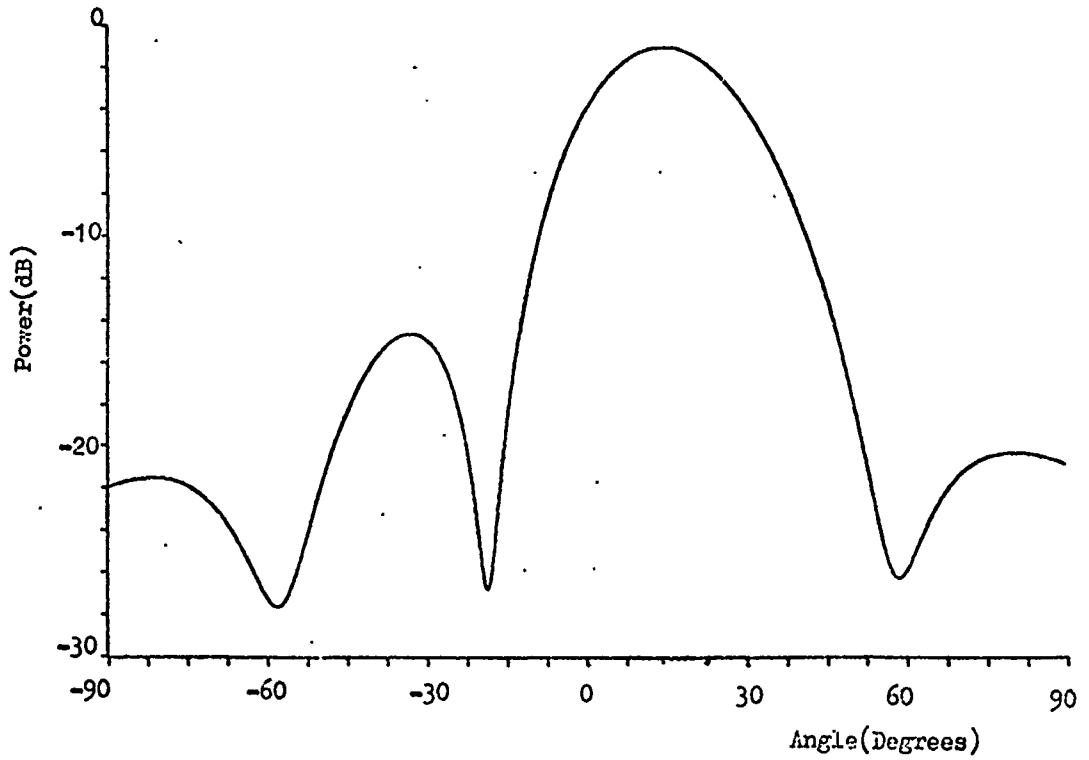


Fig. 7.18 Computed Four Element Array Pattern

Phase Settings : 135° , 90°, 45°, 0°

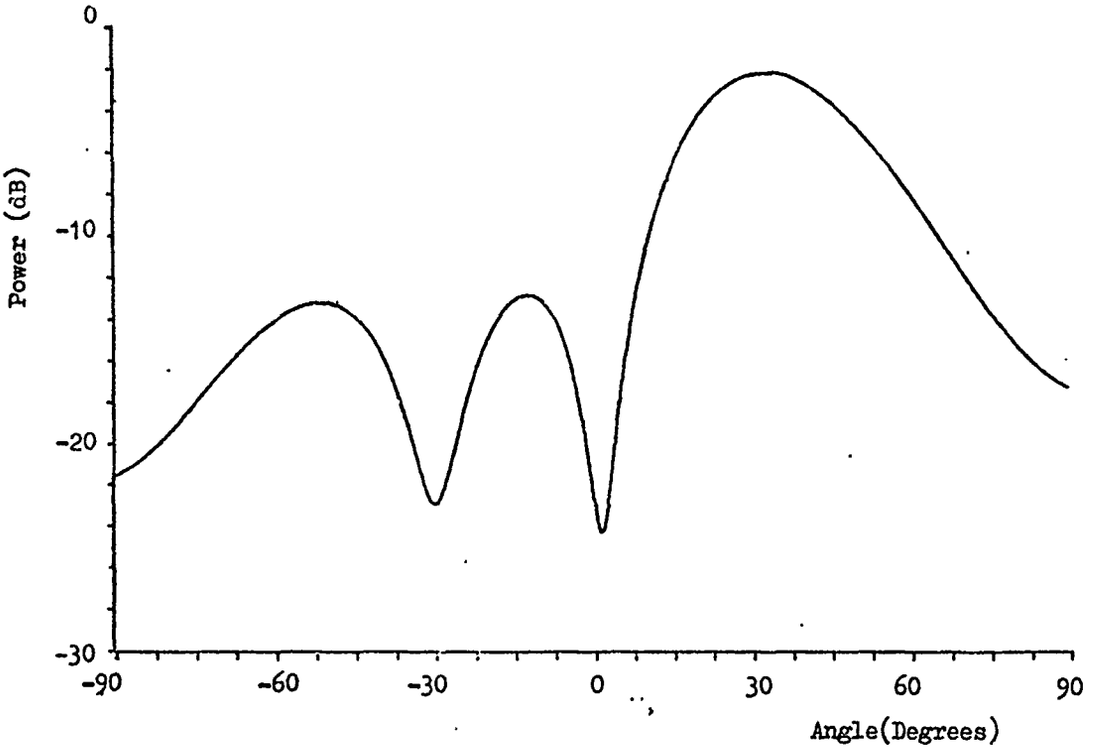


Fig. 7.19 Computed Four Element Array Pattern

Phase Settings : 270°, 180°, 90°, 0°

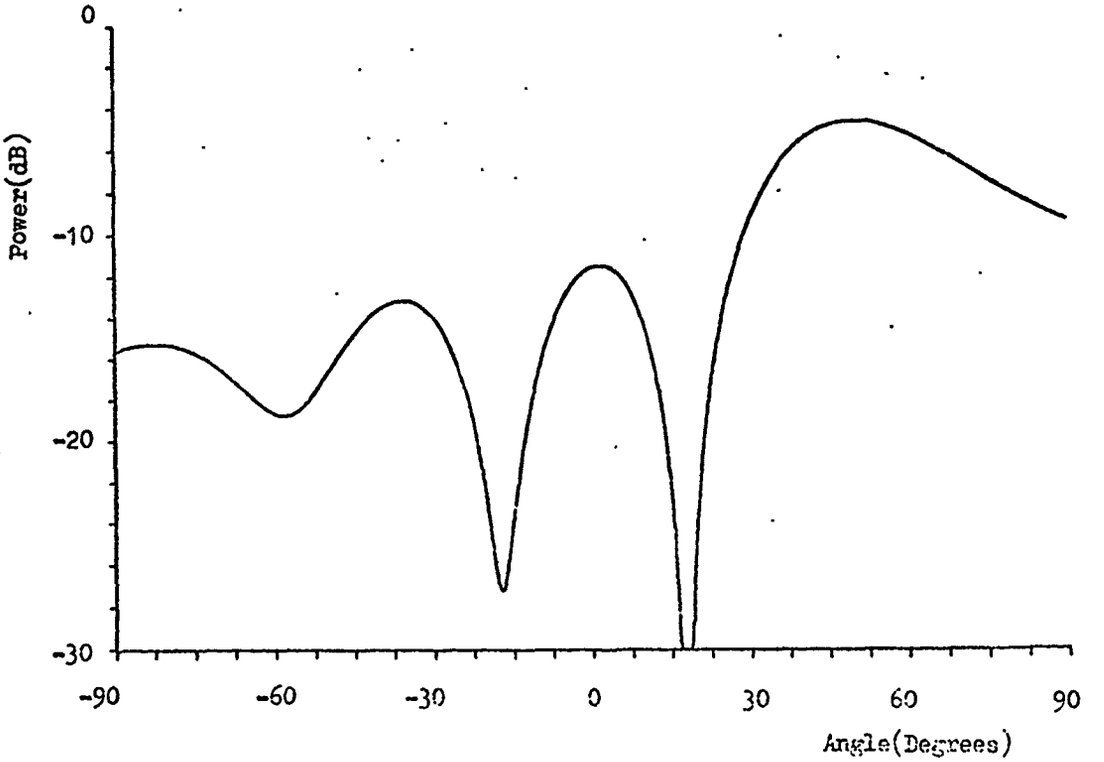


Fig. 7.20 Computed Four Element Array Pattern

Phase Settings : 45°, 270°, 135°, 0°.

mutually coupled signal is significantly larger than the circulator leakage, however, it was typically found that although a beam could be formed in the broadside direction, any attempt to steer it resulted in non-convergence of the program, thus indicating instability in the array. Particular consideration must therefore be given, in the use of these element designs, to the level of mutual coupling existing between elements.

7.4 Generation of the Microwave Reference Signal Within the Elements

Finally in this Chapter, it may be noted that one slight disadvantage of all the elements based on the HPLL is that both an IF and an RF reference signal must be distributed to the array elements. Consideration could be given, in some of the designs, to the use of optical feed techniques for simplifying the distribution of the RF reference signal, however an alternative, more attractive approach is to generate the RF reference signal actually within the element ; in this case the only microwave components in the radar will be those in the array elements. The use of this approach in the design of Fig. 7.12 is illustrated in Fig. 7.21. Since the RF reference power required with a PLL is low, a harmonic generator may be used to generate the RF power directly from the IF reference ; a filter preceding the RF mixer is used to select the desired harmonic. A varactor multiplier would provide a much higher conversion efficiency than a comb line (harmonic) generator, however, the simplicity of the latter is particularly attractive. One limitation of the comb line generator, however, is that it may be difficult to generate sufficient power to drive the mixer ($>$ 0dBm) at harmonics above approximately the tenth ; manufacturers quoted results (Omniyig Inc.) indicate that

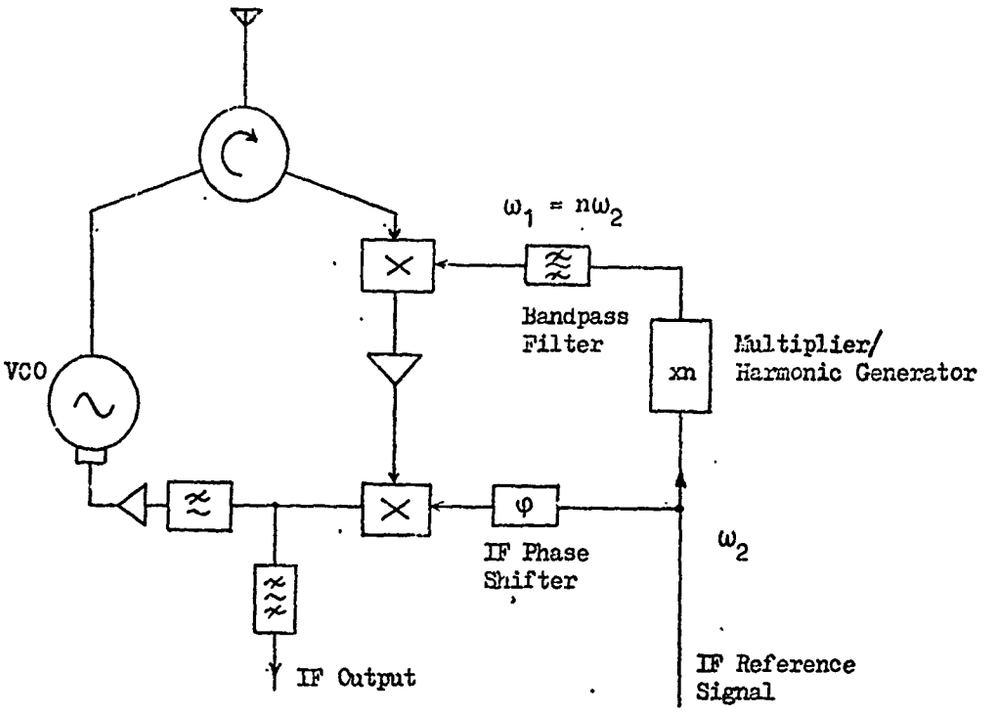


Fig. 7.21 Active Element Using Harmonic Generation to Generate the Microwave Reference Signal Within the Element

a maximum output power of + 1dBm at 2GHz may be achieved from a step recovery diode generator (type CG111) with input power of + 23dBm at 200MHz. The frequency difference between the RF and IF for which a comb generator may be used is therefore limited.

With regard to this limitation, it may be noted at this stage that the harmonically locked PLL IF phase shifter described in Chapter 8 requires an input locking signal at typically the 8th or 16th harmonic of its output frequency. The output of the phase shifter is applied to the IF input of the HPLL, and when this frequency is, for example, 100MHz, a phase shifter locking signal at 800MHz or 1600MHz will be required. Taking this signal as the input to the comb generator, it may be seen that the generation of the microwave reference input to the HPLL will be considerably eased.

A general point regarding the harmonic generation of the RF reference within the element is that careful control of phase errors on the IF input will be required since a phase error φ on the IF input will become an error $n\varphi$ on the microwave signal, n being the appropriate harmonic number. Also since the two reference frequencies will now be related, it will no longer be possible to provide an invarient phase shifter operating frequency when it is desired to use FM pulse compression, frequency hopping or a frequency change between transmission and reception. However the change of IF signal frequency required to produce a change $\Delta\omega$ on the microwave reference signal will only be $\Delta\omega/n$, so that often a narrow band of operating frequencies will still be maintained.

7.5 Conclusions

A number of different active element designs based on the use of the PLL have been described in this chapter. In section 7.1 two designs using the simple PLL with a single locking signal input were described; these circuits are essentially the same as two of the circuits described in Chapter 6, with a VCO, synchronised by the PLL, now replacing the injection locked oscillator. Although the use of the PLL in these elements offers distinct advantages in terms of both locking gain and phase error, they are nevertheless still restricted to use with RF phase shifters and are not considered as attractive as those based on use of the HPLL.

The HPLL is particularly attractive for synchronising solid state sources in active array elements ; the HPLL offers the high possible locking gain and low phase errors obtainable with conventional loops, and in addition, permits phasing of the microwave output to be achieved via an IF phase shifter. The usual microwave phase shifter required for electronic beam steering can then be replaced by an IF type. The advantages of this are that IF phase shifters should basically be more accurate, less expensive and require less drive power than microwave types. Additionally the RF phase shifter insertion loss is avoided in this arrangement.

In section 7.2.1 element designs based on a fairly straightforward implementation of the HPLL were described ; the HPLL circuit and the circuit for downconverting the received signals were separated in these designs. The two circuits of most interest in this section were those of Figs. 7.4 and 7.6 ; the circuit of Fig. 7.4 had the advantage of simplicity, but had the disadvantage that the phase

shifter may be required to operate over a large percentage bandwidth. This problem was overcome in the circuit of Fig. 7.6 in which the phase shift on reception was induced on the received signal by mixing ; in this circuit a single phase shifter operating frequency could be used, indicating that more accurate phase control and thus lower sidelobes should be available with this arrangement. This design is also particularly suitable for use with the harmonically locked PLL phase shifter described in Chapter 8.

Noting that a single RF mixer could be used to downconvert both the VCO feedback signal on transmission, and the target returns on reception, several simplified circuits based on the use of a single RF mixer were described in section 7.2.2. Of these circuits, that of Fig. 7.12 is considered to be of the most interest. This circuit has a minimum of components and thus should represent the design of lowest cost; both the RF mixer and the IF mixer are used for dual purpose in this design. Again the phase shift on reception is induced on the received signal by mixing, and thus a single phase shifter operating frequency may be used.

The active element designs that are considered to be of most interest are therefore those of Figs 7.6 and 7.12. Although the simplicity of the circuit of Fig. 7.12 is attractive, the choice between these in practice will depend on :

1) the level of mutual coupling. As described in section 7.3 the mutually coupled signal should not be significantly greater than the desired leakage signal around the circulator when the circuit of Fig. 7.12 is used. In the design of Fig. 7.6 the circulator isolation and the coupler directivity will prevent any significant amount of mutually coupled signal from reaching the loop RF mixer.

2) The relative cost of manufacture, of a) the additional RF and IF mixer for the circuit of Fig. 7.6 and b) the switching circuitry to remove the IF amplifier from the loop on transmission in the circuit of Fig. 7.12

CHAPTER 8

A PRECISE DIGITAL PHASE SHIFTER USING A HARMONICALLY LOCKED PHASE-LOCKED LOOP

8.0 Introduction

The principle of phase shifting with a harmonically locked oscillator was initially suggested by Cullen[13] and is based on the fact that an oscillator locked to a signal at the nth harmonic of its fundamental output frequency, can take any one of n possible output phases with respect to a fixed reference. The n possible phase positions are separated by exactly 360/n degrees. By controlling the phase position at which the oscillator is locked, by means of an external signal, an accurate digital phase shifter may be formed.

The technique has been previously applied to phase shifting at microwave frequencies, of the element sources in an active transmitting array[14], with the aim of avoiding the use of conventional PIN or ferrite microwave phase shifters. This was previously described in Chapter 2. Its accuracy and basic simplicity are also attractive, however, for the IF phase shifting required with the elements based on the HPLL described in the last chapter. In this case the IF input signal to each element PSD will be obtained from a harmonically locked oscillator, the IF reference signal distributed to the array elements now being at the harmonic frequency. The use of a harmonically locked oscillator in the element design of Fig. 7.11, for example is shown in Fig. 8.1.

The application of the technique at IF has the advantage that many of the problems that limited the application of the technique at RF may be overcome. In particular the typical harmonic frequencies used (e.g. 8th or 16th harmonic of a 60MHz fundamental frequency) are still in the frequency range for which signals can be easily generated and distributed to an array:this is clearly not the case for 8th or

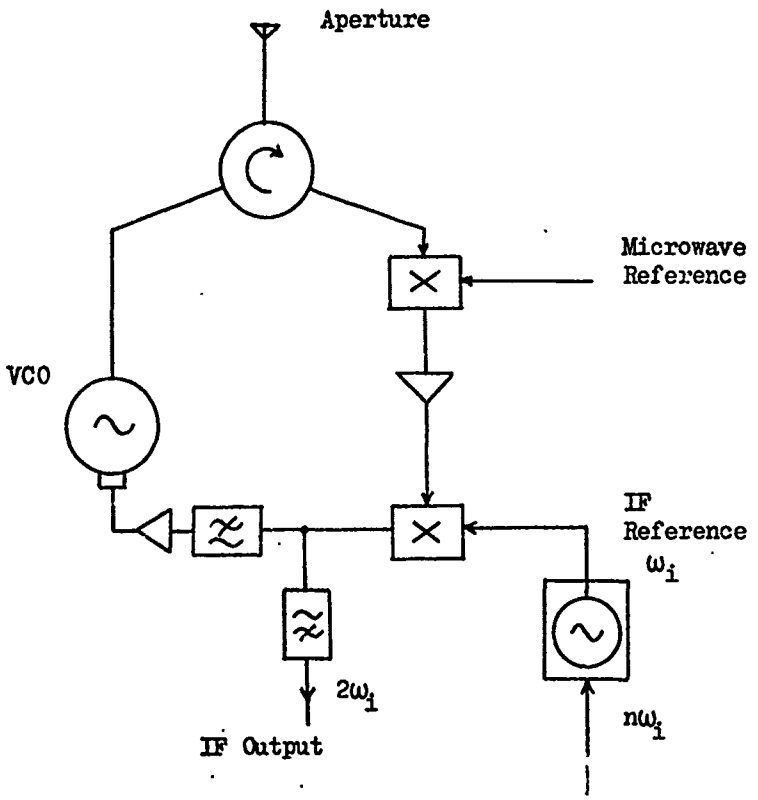


Fig. 8.1 Active Array Element Incorporating a Harmonically Locked Oscillator for IF Phase Shifting

16th harmonic locking of microwave sources, at anything but the lowest microwave frequencies. Also, the problem previously encountered, associated with the unknown phase state of the oscillator after switch-on, may now be solved at reasonable cost, by providing circuitry for the continuous measurement of the phase of oscillator output.

The previous applications of the harmonic locking phase shift technique, being at RF in the active transmitting array[14] , and at IF in a microwave Q factor measurement system[53] , have both used injection locked sources. However, from the comparison between injection locked oscillators and phase-locked loops given in Chapter 4, improved performance in terms of the steady state phase error between the element IF oscillators may be expected from the use of a phase-locked loop. A description of a harmonically locked, PLL phase shifter is thus given below.

8.1 Theory of the Harmonically Locked Phase-Locked Loop

The basic harmonically locked PLL is shown in Fig. 8.2. In all previous PLLs considered in the present work the fraction of the VCO output constituting the feedback signal has been at the VCO output fundamental frequency. In this case the nth harmonic content of the VCO output, at angular frequency $n\omega$ where ω is the VCO fundamental frequency, is now used as the feedback signal. The loop can now lock when the reference signal angular frequency ω_1 is close to $n\omega$ and within the loop locking range, which is defined below. When synchronisation has occured, both inputs to the PSD will be at angular frequency ω_1 and a DC output will be obtained from the PSD. The VCO fundamental output frequency will be ω_1/n.

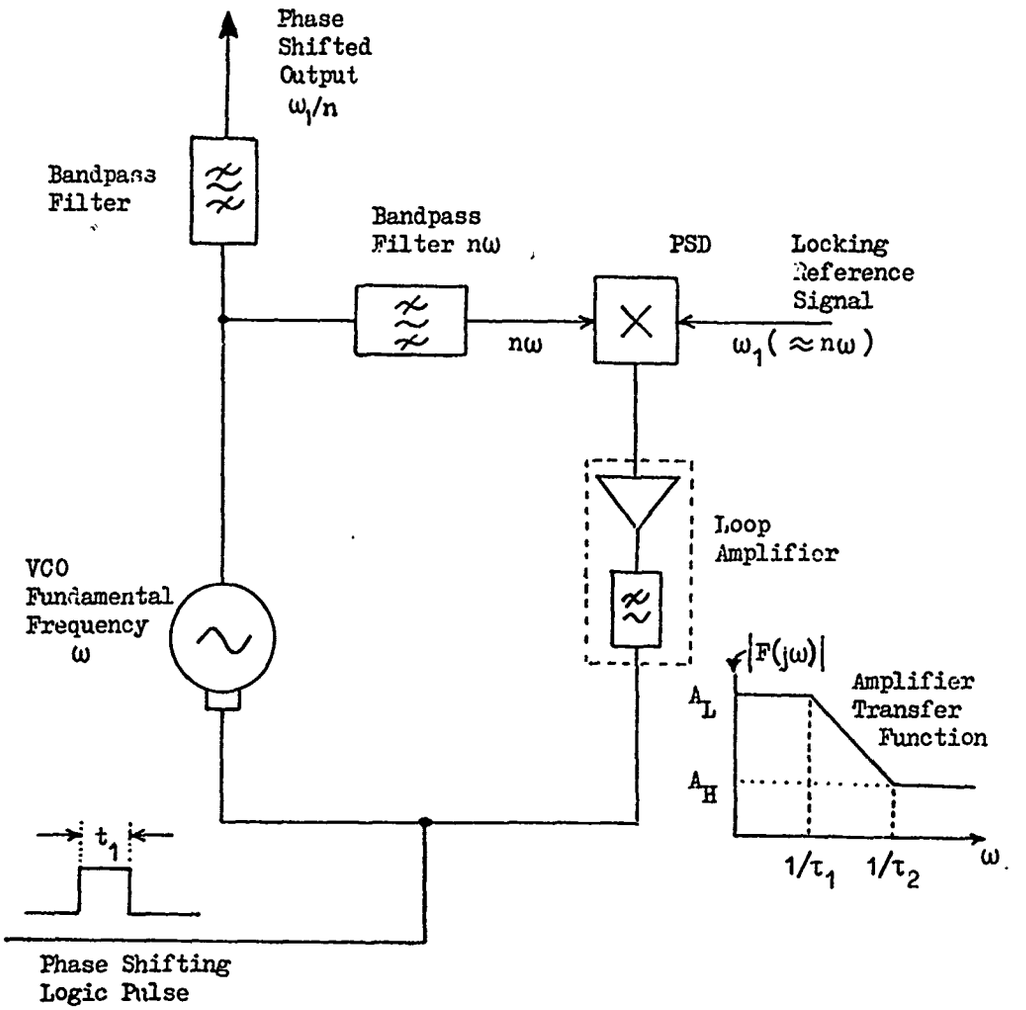


Fig. 8.2 A Harmonically Locked, Phase-Locked Loop

An alternative form of the harmonically locked PLL, which can be used when the VCO output has little harmonic content, once again returns to the use of VCO fundamental output as the feedback input to the PSD, but uses the mixer non-linearity to generate the required harmonic. The subsequent mixing between the harmonic of the VCO output generated by the mixer and the input reference signal then produces the required feedback voltage to the VCO. Again, when synchronisation is achieved, the harmonic generated within the mixer and the reference signal input have the same frequency ω_1 and the VCO fundamental frequency will again be ω_1/n.

Given the same feedback signal amplitude to the VCO, the performance in the two cases will clearly be equivalent ; however, with the use of the mixer to generate harmonics, the loop locking range becomes dependent on the non-linearity of the particular mixer used, and thus this approach is not preferred. In the harmonically locked PLL phase shifter subsequently described, a tunable, digital ECL oscillator was used as the VCO, producing an approximately square wave output ; in this case it was only necessary to filter the required harmonic from the VCO output.

Assuming that the required harmonic $n\omega$ is present in the VCO output, and ignoring for the moment the VCO output at frequencies other than $n\omega$, the loop can be simply considered as a conventional, fundamentally locked loop, operating at frequency $n\omega$. The VCO free running frequency is assumed to be $n\omega_0$ (where ω_0 is the free running frequency of the true fundamental output) and the tuning sensitivity is nK_2 rad/V.s where K_2 is the tuning sensitivity at the true fundamental output. The theory previously derived for PLLs locked at fundamental

frequency may therefore now be applied.

It was shown in Chapter 4 that a second order PLL has the advantage of permitting large values of loop gain to be used at low frequencies, thus providing low steady state phase errors, whilst reduced gain may be used at high frequencies to ensure stability. This loop type is therefore adopted here ; a filter transfer function producing a second order loop is shown for the loop filter in Fig. 8.2.

From Eqn. 4.81 the locking range (at the harmonic frequency) is given by

$$\Delta\omega_L = K$$
$$= A_1 K_1 (nK_2) \qquad \ldots.8.1$$

where A_L is the combined low frequency gain of the amplifier and filter

K_1 is the PSD gain in V/rad for the particular input signal amplitude used. It may be noted that in this case the harmonic output power of the VCO may not be sufficient to drive the PSD into the saturated region, in which case K_1 will be strongly dependent on the harmonic power, as described in section 4.2.10.

The steady state phase error arising from a detuning $\Delta\omega$ between the input signal at frequency ω_1 and the VCO free running frequency $n\omega_0$ (where ω_0 is the free running frequency at the true fundamental) is

$$\varphi_e = \sin^{-1}\left(\frac{\Delta\omega}{\Delta\omega_L}\right)$$
$$= \sin^{-1}\left(\frac{\omega_1 - n\omega_0}{nA_L K_1 K_2}\right) \qquad \ldots.8.2$$

Clearly, by providing a large value of low frequency amplifier gain A_L, low phase errors may be obtained.

The apparent locking range $\Delta\omega_L'$ appearing at the VCO true fundamental output frequency is 1/nth of that given by Eqn. 8.1, i.e.

$$\Delta\omega_L' = \frac{A_L K_1 n K_2}{n} = A_L K_1 K_2 \qquad \ldots\ldots 8.3$$

Similarly the phase error φ_e' appearing at the true fundamental frequency is 1/nth of that given by Eqn. 8.2, i.e.

$$\varphi_e' = \frac{1}{n} \sin^{-1}\left(\frac{\Delta\omega}{\Delta\omega_L}\right) \qquad \ldots 8.4$$

The steady state phase error at the fundamental frequency therefore varies between $\pm \frac{90}{n}$ degrees at either extreme of the locking range.

Fig. 8.3, reproduced from Fig. 4.8, shows the PSD output voltage variation with the phase error between the reference signal at frequency ω_1 and the VCO output at the harmonic. It may be seen that an identical PSD output voltage is obtained, and thus an identical locking condition exists, for any 2π radian change of phase of the VCO output at the harmonic. A change of 2π radians of the harmonic output corresponds, however, to a phase change of only $2\pi/n$ radians at the true fundamental frequency, and thus there are n distinct phase states of the VCO fundamental output for which lock can occur, each separated by <u>exactly</u> $2\pi/n$ radians. The harmonically locked PLL may therefore be used as a digital phase shifter if the phase position at which the VCO is locked can be controlled.

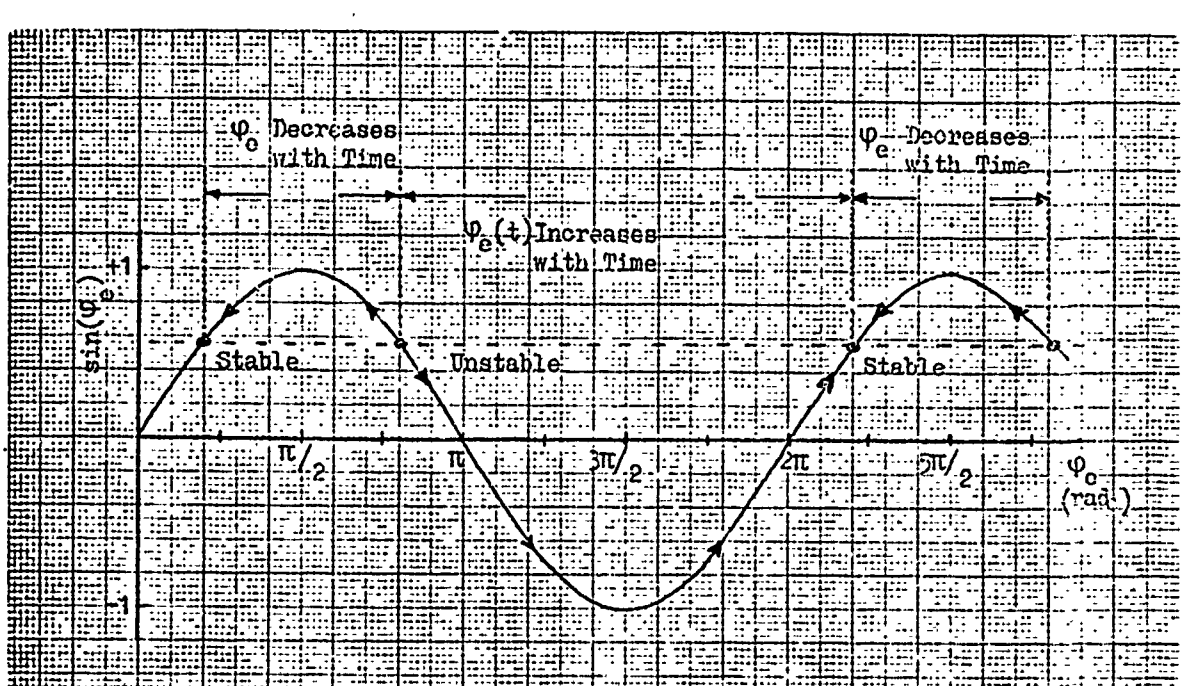


Fig. 8.3 Phase Sensitive Detector Characteristic

Phase control may be achieved in practice by the application of a voltage pulse to the VCO as illustrated diagramatically in Fig. 8.2. If the VCO frequency is increased by amount $\delta\omega$ for the period of the pulse t_1 the relative phase will be advanced by an amount $\delta\omega.t_1$. The phase error, defined as the difference between the locking signal phase and the phase of the VCO output at the harmonic, will thus experience a similar phase change but with opposite sign. From Fig. 8.3, it may be seen that if at the end of the pulse the phase error is changed to a value less than that of the previous unstable equilibrium, but still greater than that of the preceding unstable equilibrium, the loop will relock the VCO to the stable locking position with a phase change of magnitude exactly equal to 2πrad. At the VCO fundamental frequency this will correspond to a phase advance of exactly $2\pi/n$ rad. The range of the product $\delta\omega.t_1$ for which this phase advance will occur may be seen to be

$$(\pi + 2\varphi_{e0}) \leqslant \delta\omega.t_1 \leqslant (3\pi + 2\varphi_{e0}) \qquad \ldots\ldots 8.5$$

where φ_{e0} is the initial deviation of the steady state phase error for the zero error position (0, 2π, 4π rad. etc.). When large values of amplifier gain A are used, φ_{e0} will typically be small and Eqn. 8.5 will simplify to

$$\pi \leqslant \delta\omega.t_1 \leqslant 3\pi \qquad \ldots 8.6$$

A phase lag may similarly be obtained by applying a voltage pulse to the VCO that will cause the VCO frequency to decrease such that phase is ' lost ' relative to the locking source. In this case the product of the frequency change $\delta\omega$ and the pulse length t_1 that will result in a phase lag $2\pi/n$ rad on the output will be

$$(\pi - 2\varphi_{e0}) \leqslant \delta\omega . t_1 \leqslant (3\pi - 2\varphi_{e0}) \qquad \ldots\ldots 8.6$$

which again for small φ_{e0} becomes

$$\pi \leqslant \delta\omega . t_1 \leqslant 3\pi \qquad \ldots 8.7$$

The corresponding frequency change on the fundamental output during the pulse is $\delta\omega/n$.

The time required to implement a phase shift may clearly be reduced by using a short pulse width in conjunction with a large frequency change, but finally, the phase shifting speed will be limited by the time required for the loop to re-lock the oscillator after the pulse. The worst case condition will be when the phase error at the end of the pulse is at a value close to an unstable equilibrium position. It was shown in Chapter 4 that the approximate time for the loop to re-lock in this case was $10/\omega_n$ sec. where ω_n is the loop natural angular resonant frequency. From Eqn. 4.97

$$\omega_n = \sqrt{\frac{K}{\tau_1}} = \sqrt{\frac{nK_1K_2A}{\tau_1}} \qquad \ldots 8.3$$

where $1/\tau_1$ is the frequency associated with the filter roll-off from the low frequency value, as shown in Fig. 8.2. The steady state phase error given in Eqn. 8.2 will typically be established in a time t_s given by

$$t_s = \tau_1$$

8.2 Phase Measurement Technique

It was previously noted that the phase of fundamental output of a harmonically locked PLL immediately after switch-on will be unknown. This problem can be simply overcome by providing measurement of the phase state at the PLL output. This may be achieved in practice with the arrangement shown in Fig. 8.4. A fraction of the fundamental output of the PLL phase shifter is applied to two PSDs (mixers) along with a signal at the same frequency, derived (e.g. via a digital divider) from the reference input of the PLL. In one signal path a fixed 90° phase shift is introduced, as shown.

Since the inputs to the PSDs are at the same frequency a DC voltage will appear at the outputs, proportional to the phase difference between the PSD inputs. The variation of the output voltage of one PSD with the phase difference between the signal derived from the reference input and the PLL output will be of the form of Fig. 8.3, for a sinusoidal PSD. It will not be possible to determine the phase state of the PLL from measurement of the output voltage of one of the PSDs alone however, since there are two phase positions that can yield the same PSD output. By the use of two PSDs and the 90° phase offset however, voltage measurements can unambiguously indicate the phase state. An example of the variation of the two PSD outputs with phase difference is shown in Fig. 8.5. Consider the case, for illustration, of 8th harmonic locking, producing phase increments of 45°. By placing comparators on the first PSD output with voltage thresholds as shown, it will be possible to unambiguously determine when the PLL output phase is at $+ 90^{\circ}$ or $- 90^{\circ}$, but there will be ambiguity between the $+ 45^{\circ}$ and $+ 135^{\circ}$ positions, the 0 and 180° positions and the $- 45^{\circ}$ and $- 135^{\circ}$ positions. By noting in addition

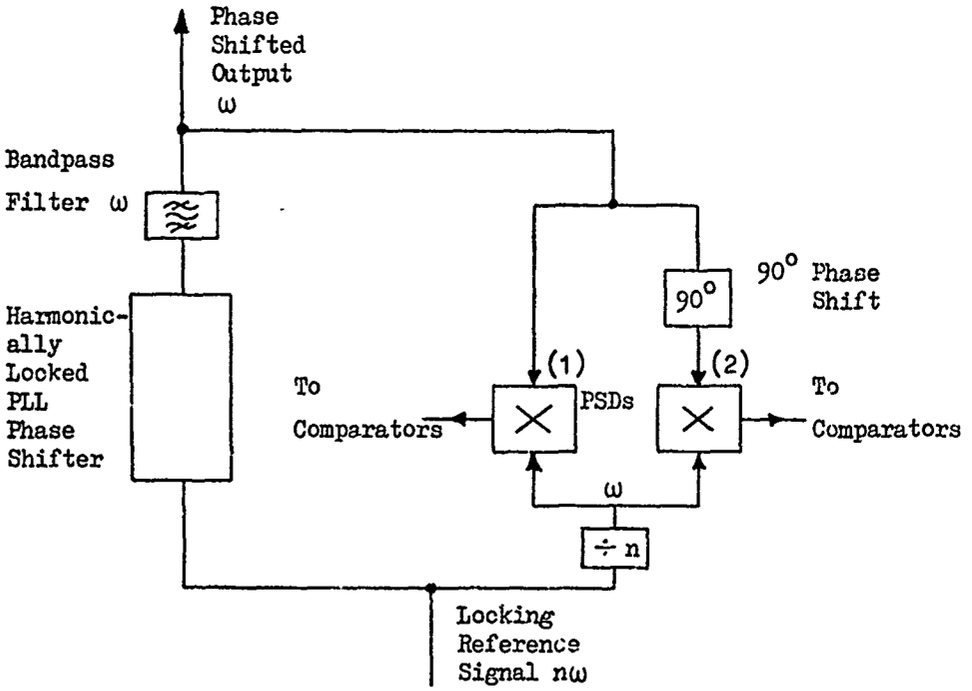


Fig. 8.4 Arrangement for Measurement of Phase Shifter Phase State

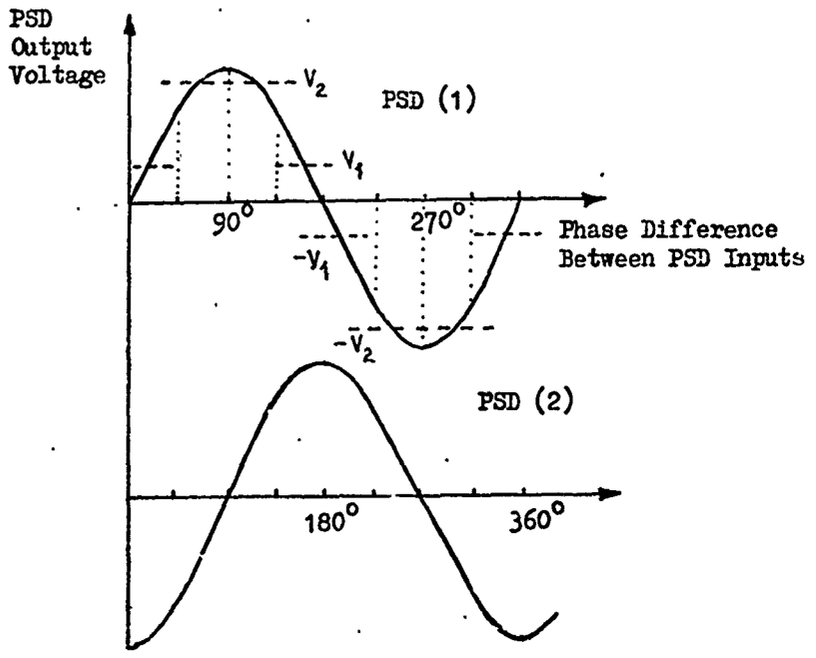


Fig. 8.5 PSD Output Characteristics & Comparator Levels for Phase Measurement

the sign of the second PSD output, using another comparator (or comparators), these ambiguities may be resolved.

The phase measurement, in addition to indicating the initial phase position after switch-on, may also be used a) for phase shifter fault indication and b) to control the phase shifter setting ; instead of applying a previously determined number of phase shifting control pulses to the loop to produce a required phase setting, the phase shifter is placed in a control loop that repeatedly applies pulses until the comparator outputs indicate the desired output phase has been reached.

8.3 Experimental Results

The basic circuit used to demonstrate phase shifting with a harmonically locked PLL is shown in Fig. 8.6. Locking to the eighth harmonic was chosen for the experiments since this enabled the circuit to be constructed using readily available equipment and components, whilst also providing reasonably small phase increments : 45° (i.e. 3 bit phase control).

The VCO used was a digital, integrated circuit, ECL oscillator (type SP1648B) to which a resonant circuit could be added externally to determine the frequency of oscillation. Varactors were included in the resonant circuit to provide voltage tuning. The tuning characteristic of the oscillator is sketched in Fig. 8.7. Since the desired IF reference frequency for the experimental array was 60MHz, a fixed offset voltage was applied to the varactor to produce a free running frequency of this value. The loop feedback signal then varied the varactor voltage around the fixed value. It may be seen that over

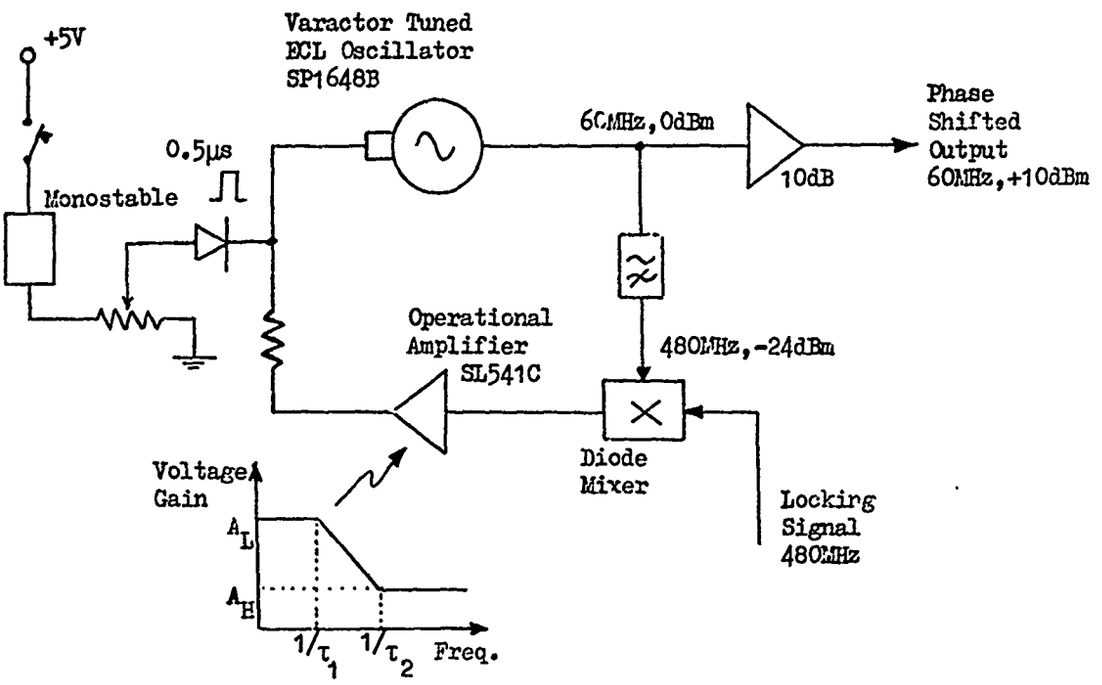


Fig. 8.6 Experimental Harmonically Locked Phase Shifter Circuit

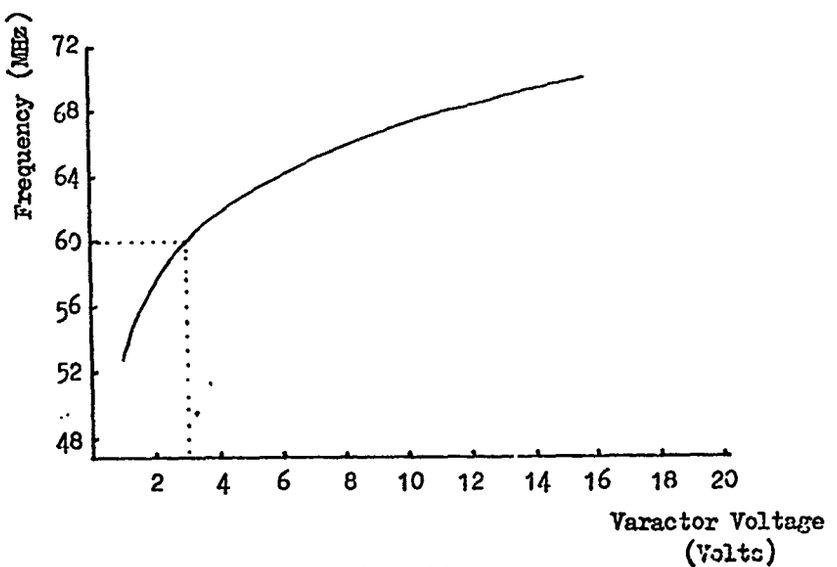


Fig. 8.7 VCO Tuning Characteristic

a frequency range ± 2MHz the tuning characteristic was approximately linear. The tuning sensitivity at 60MHz was measured to be 2.86MHz/V. The VCO output power at 60MHz was ~ 1mW, but since a higher level than this was required to drive both the active element PSD and the two possible additional mixers for measurement of the output phase, a discrete component 60MHz amplifier was included in the output, providing 10dB gain at the desired output frequency and some degree of filtering of the harmonics.

The eighth harmonic output of the VCO, of frequency ~ 480MHz and amplitude ~ - 24dBm for the particular VCO used, was simply high-pass filtered to remove the 60MHz fundamental before being applied to the PSD, along with the reference input at 480MHz. The PSD used was a passive diode mixer (type CM1) for printed circuit board mounting, with input frequency range 0.1 - 1000MHz. The measured value of the PSD gain K_1 V/rad for the particular powers used was 11.4 mV/rad. A wideband operational amplifier (type SL541C) was used to provide both amplification and filtering of the PSD output with effective transfer function as shown. The value of gain at angular frequencies less than $1/\tau_1$ was in fact limited by the open loop gain of the amplifier (70dB) in this case. The amplifier transfer function characteristics were :

A_L ,	the low frequency voltage gain	= 3162
A_H ,	the high frequency voltage gain	= 6.8
$1/\tau_1$,	the angular frequency associated with the gain roll-off from the low frequency value	= 1.7×10^3 rad/s
$1/\tau_2$,	the angular frequency associated with the transition to the flat high frequency gain region	= 6.7×10^5 rad/s

The VCO varactor was fed from the amplifier output through an impedance of several KΩ, but since the varactor impedance (reverse biased diode) was much greater than this, the voltage drop was negligible. The phase shifting control pulses were simply generated from a TTL monostable multivibrator (type 74121) and applied to the varactor via a potentiometer and diode. The use of a simple TTL compatible circuit for the generation of the phase shifting pulses was felt to be particularly desirable from the point of view of interfacing the phase shifters with a beam-steering computer. The diode was included to act as a switch ; when the monostable voltage was low the diode was reverse biased and the monostable was thus effectively isolated from the varactor ; when the monostable voltage increased during the phase shifting pulse to a value greater than that previously existing on the varactor, the diode turned 'on' thus applying the voltage pulse to the varactor. The potential divider action of the impedance following the amplifier, and the pulse source impedance, effectively disconnected the loop during this time. Taking the measured value of the VCO tuning sensitivity as 2.86MHz/V, Equation 8.6 predicts a required change of voltage at the varactor during the 0.5μs pulse as being of the order of 0.1V, for a 45° phase shift. This was found to be in close agreement with that obtained. Clearly, since the characteristics of the phase shifting pulse are determined by the product of the frequency shift and the pulse length, a shorter pulse length and a larger voltage pulse at the varactor could have been used.

The steady state phase error predicted from Eqn. 8.2 between the reference signal and the VCO output at the 8th harmonic, for a detuning of 1MHz at the fundamental frequency (8MHz at the 8th harmonic) is 0.55°. On the fundamental output at 60MHz, this

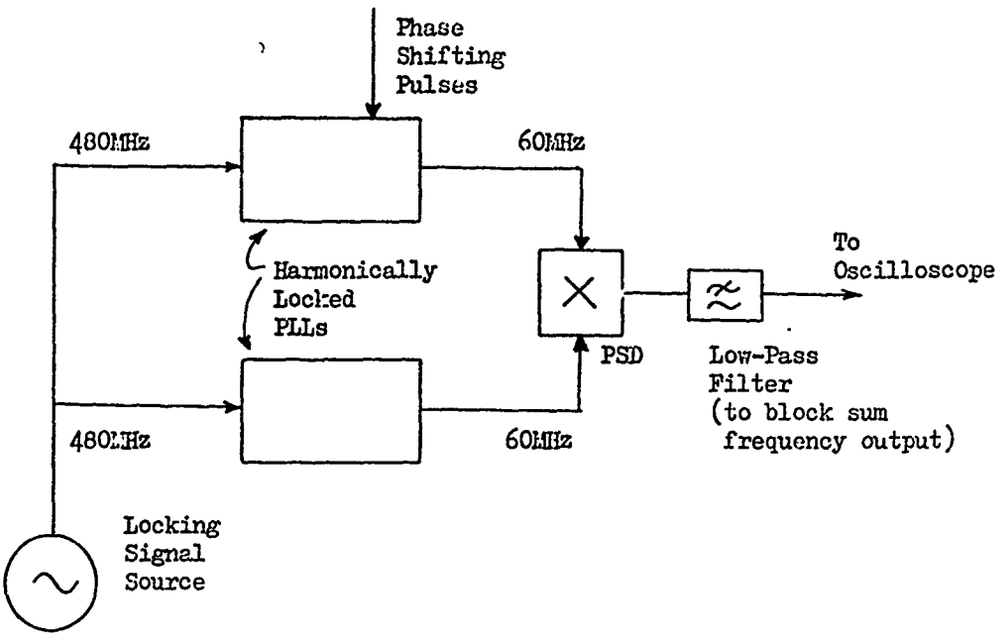
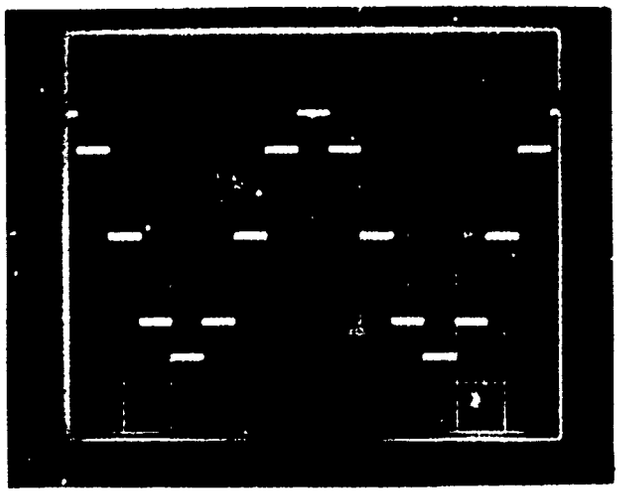
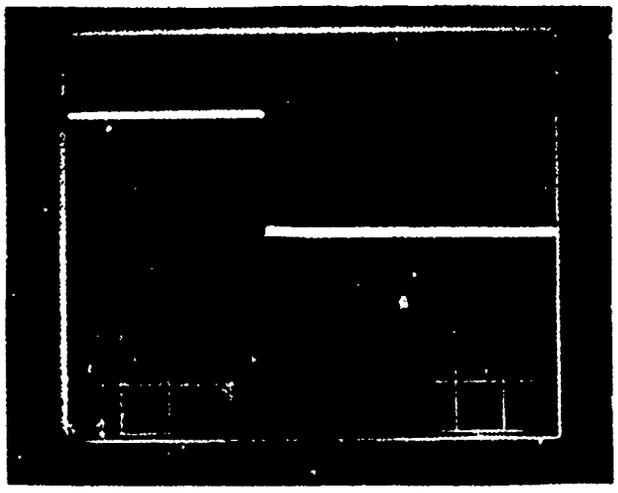


Fig. 8.8 Experimental Arrangement for Demonstrating Phase Shifts



10ms

Fig. 8.9 Phase Sensitive Detector Output Showing Successive 45° Phase Increments



..... 0°

..... 45°

20μs

Fig. 8.10 Detail of Phase Transient During Switching Between 0° and 45° Positions

corresponds to a phase error of 0.07° on all the phase positions, the phase increment between phase positions still being exactly 45°. This example clearly illustrates that low phase errors may be achieved with the PLL ; in fact a lower phase error than that given could easily be obtained with the use of an amplifier providing higher DC gain.

The natural resonant frequency of the loop ω_n in this case was, from Eqn. 8.8, $\approx 3.10^6$ rad/s. Thus the theoretical worst case time for the loop to relock after the application of a phase shifting pulse was

$$\frac{10}{\omega_n} = 3.37\ \mu s$$

although in most cases a significantly shorter time would be obtained. The phase error on the 60MHz output, being typically reduced to a few degrees after several μs, is further reduced to the low value given above in an approximate time

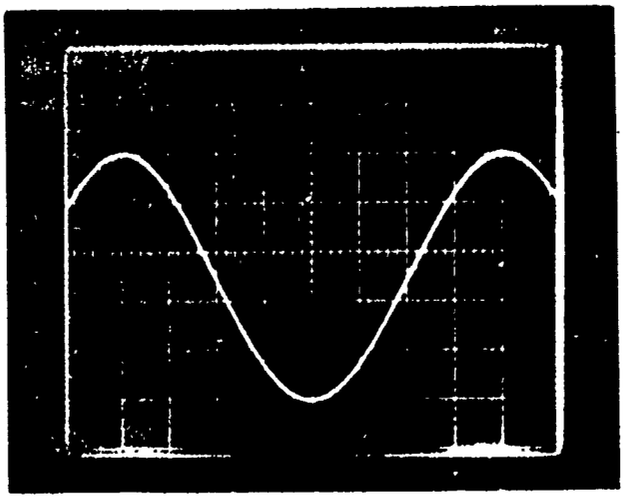
$$\tau_1 = 0.6ms$$

Several points relating to these times are worthy of note :

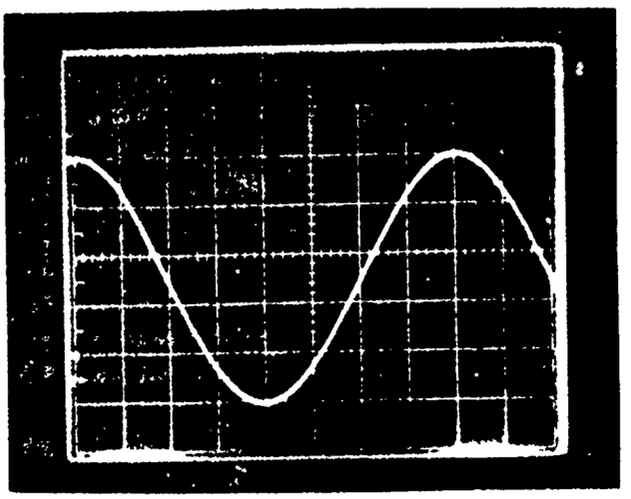
1) Although the time given by $\tau_1 = 0.6ms$ appears long, this is the time required to achieve a very low value of phase error. Phase errors are reduced to a few degrees (in many cases an adequate level) in a few μs.

2) By optimising the loop design a reduction of an order of magnitude in these times should be possible.

3) Care has been taken in the element designs of Chapter 7 to avoid a requirement for phase shifter resetting between transmission and reception. A relatively long delay, corresponding to changes in the beam-pointing direction, will therefore exist between phase shifter



a) Phase Shifter Output in the 0^{o} Reference State



b) Phase Shifter Output in the 45^{o} Phase Position

Fig. 8.11 60Hz Output Signal from Harmonically Locked PLL Phase Shifter

resetting.

To demonstrate phase shifting with the harmonically locked PLL, two identical loops were arranged as shown in Fig. 8.8 (In fact four such loops were constructed, for use in the four element array described in the next chapter). With the monostable of one phase shifter successively triggered, yielding successive phase shifts of 45° on one output, a voltage appeared on the output of the PSD comparing the phase of the two outputs, as shown in Fig. 8.9. It may be seen from the Figure that as successive phase shifts of 45° were applied, the PSD output voltage varied sinusoidally, as expected. To examine the phase shifting time, the scale of display of Fig. 8.9 was expanded to show a single phase transition. This is shown in Fig. 8.10. It may be noted that the pulse length used to implement the phase shift in this case was 0.5 μs, thus the phase shifting time was determined to a large extent by the time required for the loop to relock. It can be seen from Fig. 8.10 that a phase shift is indeed accomplished within a 3μs period, as predicted. Although not clearly seen in the photograph, the predicted relatively slow subsequent reduction in the phase error to a low level was also observed.

To illustrate the accuracy of the phase increments of 45°, one of the harmonically locked loops was now used to synchronise the time base of a wide band oscilloscope. The output of the other loop was displayed on the oscilloscope. The displayed waveforms before and after a 45° phase shift are shown in Fig. 8.11(a) and (b). Careful examination of the plots indicated that the phase increment was certainly within $\pm 2^{\circ}$ of 45°, this being the limit of accuracy of measurement.

Finally, phase measurement circuitry as described in section 8.2 was applied to the output of one phase shifter to check that correct indication of the phase state could be achieved. The second phase shifter was now used to provide the coherent 60MHz reference signal for the two measurement PSDs. The two PSDs, the comparators and the subsequent decoding logic circuit used are shown in Fig. 8.12. The eight LEDs appearing on the right hand side of the Figure were used as indicators. As the phase position was now successively changed the 8 LEDs were successively illuminated in turn as desired.

8.4 Conclusions

It has been demonstrated, both theoretically and experimentally that the harmonically locked PLL can be used for phase shifting in the same way as the harmonically locked, injection-locked oscillators previously reported. Indeed the PLL has the advantage that both low relative phase errors (i.e. the phase errors between phase positions) and absolute phase errors can be achieved. A 60MHz phase shifter suitable for use with the active elements based on the HPLL has been demonstrated experimentally, and a phase measurement circuit for determining the output phase has also been shown to operate successfully. Phase shifting times of the order of a few μs have been obtained, although a reduction in this time by an order of magnitude should be possible with optimisation of the loop components and transfer function. Some of the results presented are also described in reference (54).

As a general point, it may be noted that the harmonic locking phase shifting technique may be applied at any frequency. Direct harmonic locking of active element PLLs or HPLLs (for instance via the IF

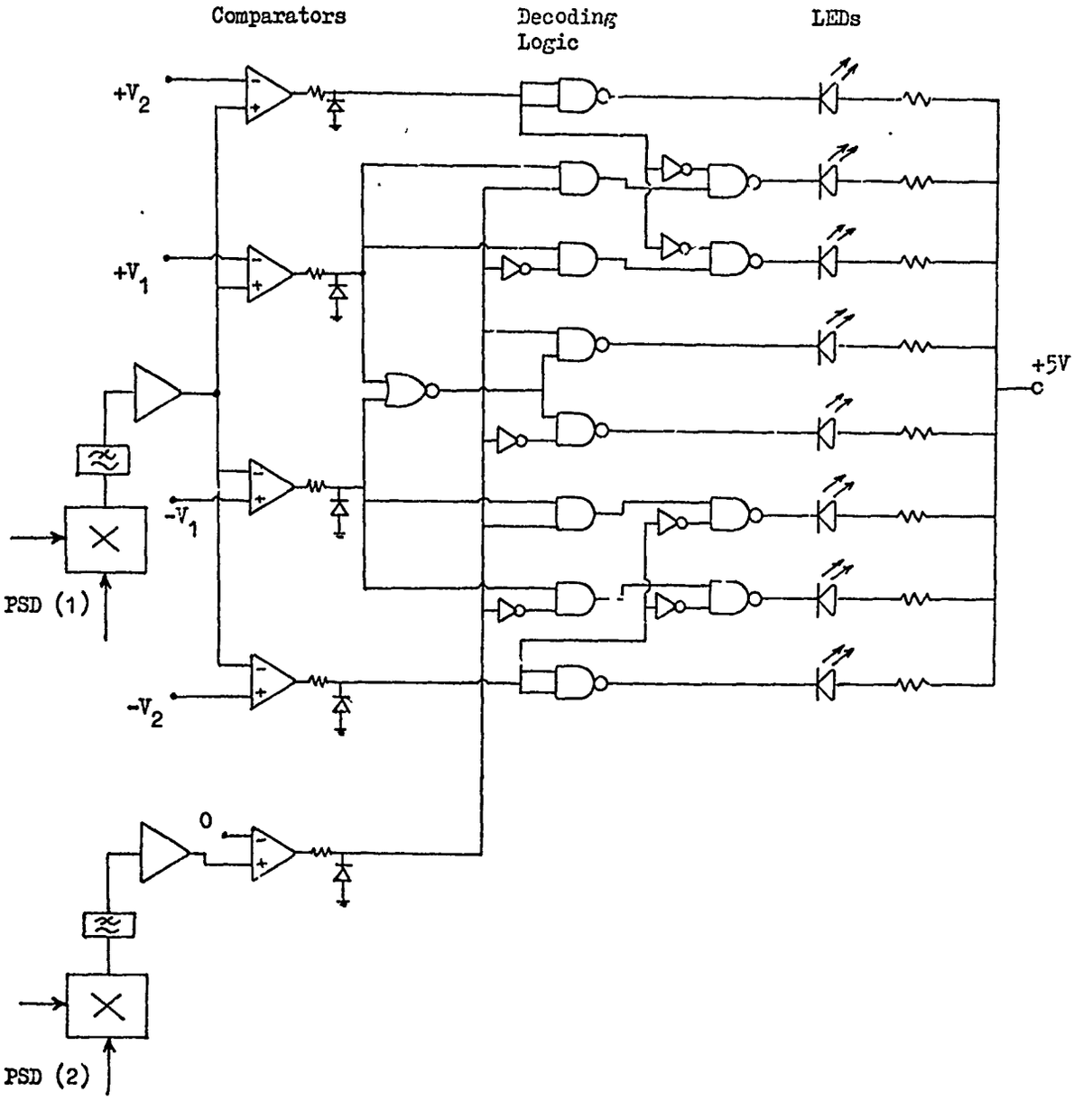


Fig. 8.12 Circuit for Determining the Phase State from the PSD Outputs

input in this case) could be considered for a transmit-only array. For low frequency phase shifting applications, integrated circuit PLLs could conveniently be used to reduce the circuit complexity.

CHAPTER 9

An Experimental Four Element Active Array

9.0 Introduction

9.1 Design and Construction of the Experimental Elements

9.2 Measurement Technique and Experimental Results

9.0 Introduction

The experimental active array was constructed principally with the aim of demonstrating that the element designs based on the heterodyne phase-locked loop can indeed provide electronic beam steering using only IF phase control. It was also desired to demonstrate the use of IF phase shifters using the harmonically locked PLL phase shifting technique. A small array was therefore constructed using the element designs considered to be of most interest in Chapter 7 (i.e. the designs of Figs. 7.6 and 7.12) and the beam-forming and beam-steering properties of the array were examined.

9.1 Design and Construction of the Experimental Elements

To maintain the maximum flexibility for the investigation of various element configurations, the experimental elements were constructed using discrete components (i.e. discrete directional couplers, circulators, mixers etc.) as opposed to a more compact but less easily varied approach using microwave integrated circuits. A limitation on the number of components that were available however, restricted the size of the array to only four elements, but nevertheless this number, though not ideal in that none of the elements in an array of this size has the same mutual coupling environment, was found to be sufficient to clearly demonstrate beam steering.

Since it was desired to examine the performance of arrays of both the element designs of Fig. 7.6 and 7.12, for simplicity the element IF circuitry was designed to work with either design. The experimental circuit corresponding to the design of Fig. 7.6 is shown in Fig. 9.1. For this case the switch shown was kept always in position (1). The

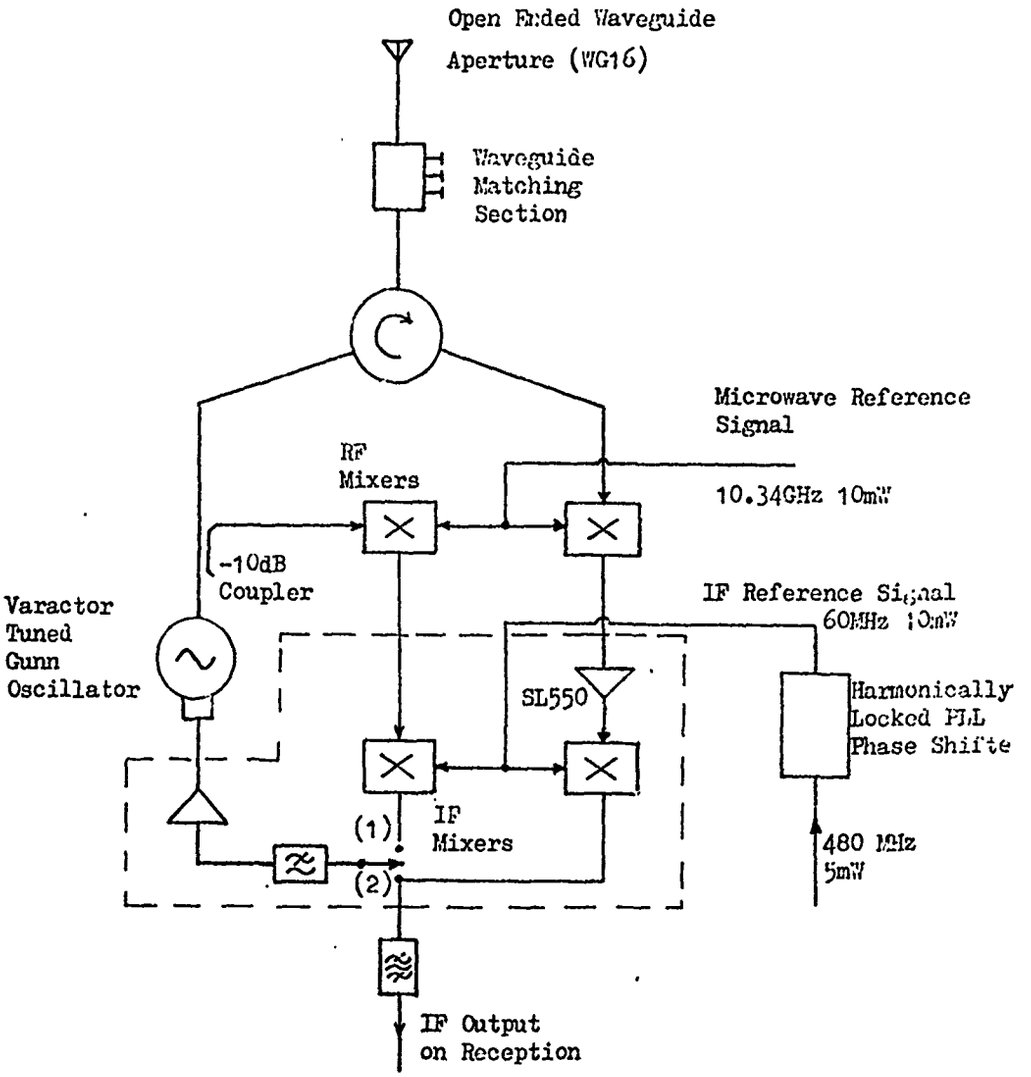


Fig. 9.1 Detail of the Experimental Element Circuit Configuration

VCOs used were waveguide varactor tuned Gunn oscillators (AEI type DA8825G) producing $\sim$150mW at a frequency $\sim$ 10.46GHz; this oscillator type was previously used for the PLL transient experiments described in Chapter 4. A directional coupler was used to take a sample of the VCO output, which after downconversion in an RF mixer (Lorch type EM36A), was applied to a PSD (Cimarron type CM1 printed circuit board mixer) along with the IF reference input at 60MHz. The PSD output voltage was amplified in a high speed operational amplifier (Plessey type SL541C) with transfer function producing a second order loop, before being applied to the VCO varactor to close the loop. A fixed bias voltage was also applied to the varactor to bias the VCO into the linear tuning range using the circuit previously shown in Fig. 4.31.

The VCO was synchronised to the sum of the input reference frequencies at 10.34GHz and 60MHz. With VCO tuning sensitivity $\sim 2\pi.10^6$rad/V.s, PSD gain of 0.1 V/rad and a loop amplifier low frequency gain of 100, the theoretical locking range of the loop was $\sim$100MHz; however due to the rather low voltage swing ($\pm$ 3V) of the operational amplifiers used the locking range was in practice limited to $\sim$ 30MHz (i.e. a synchronisation range of 60MHz). Within this range, the predicted phase error introduced by the loop for a 1MHz frequency difference between the sum of the locking signal frequencies and the free running frequency was $\sim 0.6^o$.

The IF reference signal for each element was derived from a harmonically locked PLL phase shifter of the same design as that described in Chapter 8. Eight harmonic locking was used to provide phase increments of 45^o.

After the directional coupler, the VCO output was applied, via a

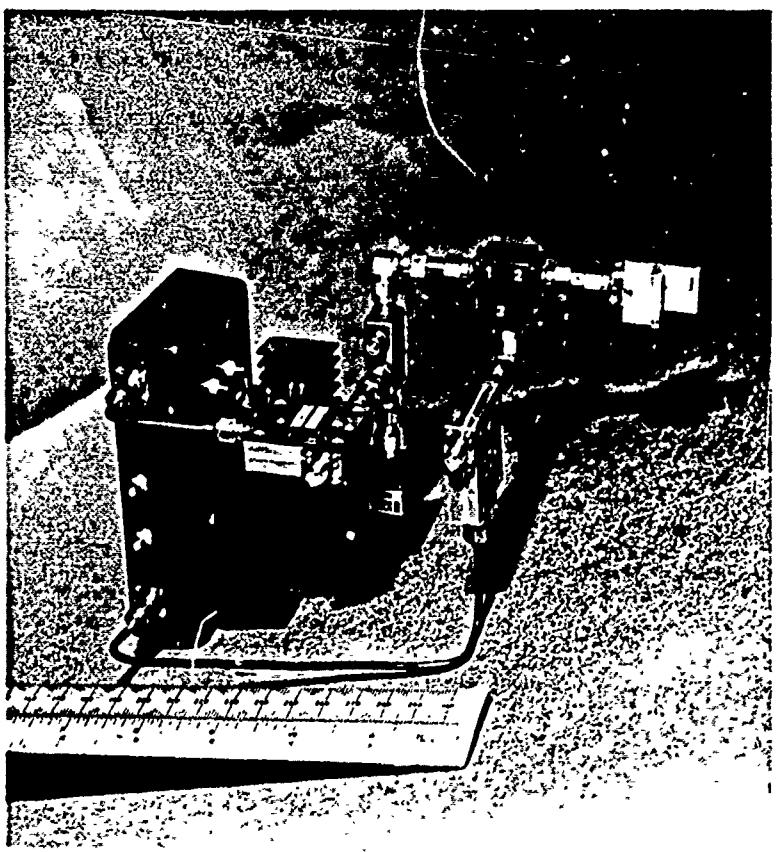


Fig. 9.2 Experimental Element Corresponding to the Design of Fig. 7.6

circulator, to the element aperture. Open ended waveguide apertures were used (WG16) since the characteristics of these had been previously well established by Darbandi[30]. The apertures were matched at the operating frequency (10.4GHz) by means of a 3-screw tuner; matching was carried out with the element isolated, i.e. not in the array environment.

In the reception path, shown on the right hand side of Fig. 9.1, the downconverting mixer (Lorch type EM36A) was followed by a low noise amplifier (Plessey type SL550). The variable gain control of this amplifier was used to equalise the output signals of the array elements for the reception radiation pattern measurements. The element output was taken as the sum frequency output of the subsequent mixer.

The physical form of this element (not including the phase shifter) is shown in Fig. 9.2. All the IF and DC circuitry shown within the dashed line in Fig. 9.1, was contained on a single printed circuit board. The box holding this was then attached directly to the waveguide Gunn oscillator to make the loop length as short as possible, since any delay present in the loop reduces the bandwidth that may be used, as described in Chapter 4. The box containing the IF circuitry, attached to the waveguide Gunn oscillator and its associated heat sinks, may be seen on the left hand side in Fig. 9.2. The lower semi-rigid cable input to the IF circuitry box comes directly from the receiving RF mixer, which follows the circulator separating the transmitted and received signals. The upper semi-rigid cable input comes directly from the RF mixer which downconverts the sample of the oscillator output provided by the directional coupler. For the purpose of illustration a microstrip dipole

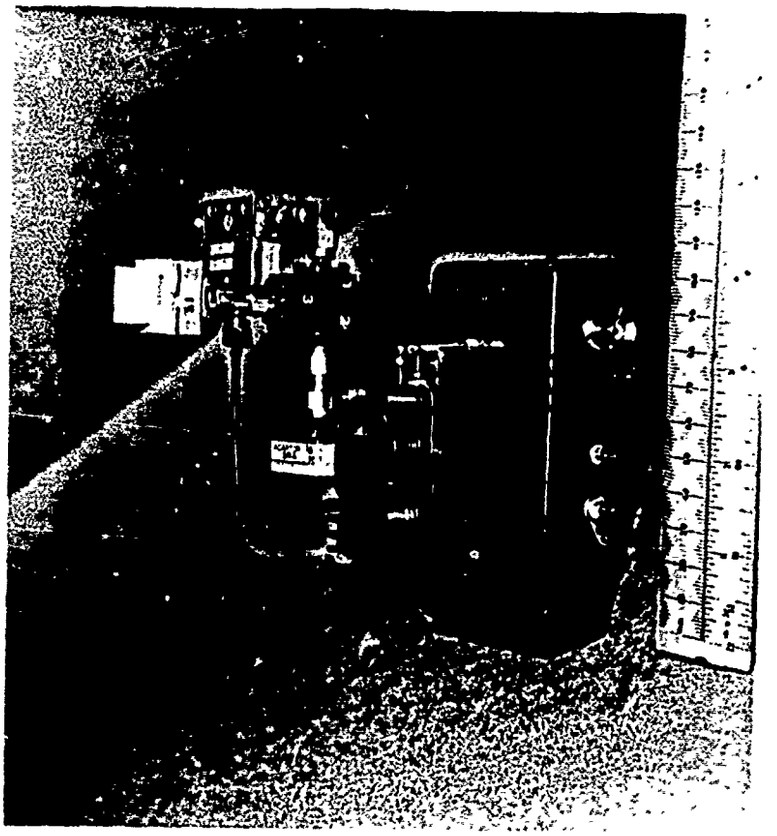


Fig. 9.3 Front View of the Experimental Element Corresponding to the Design of Fig. 7.12

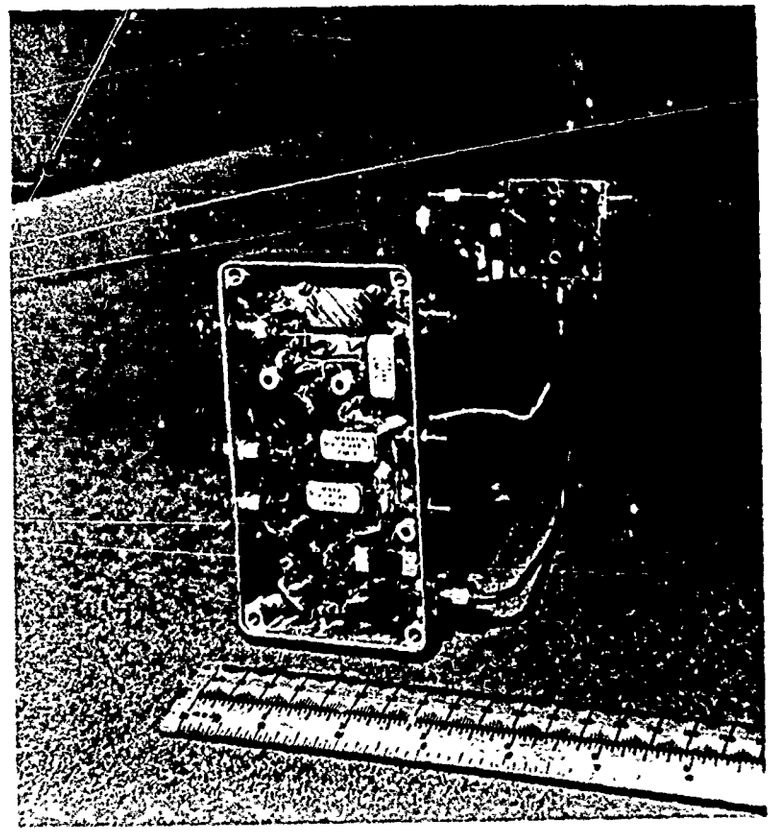


Fig. 9.4 Rear View of the Experimental Element Corresponding to the Design of Fig. 7.12

antenna is shown for the element aperture ; in practice transformation into waveguide occurred at this point, with a ~ 30cm waveguide section preceding an open-ended waveguide aperture.

A change in the circuit configuration to form an element corresponding to the design of Fig. 7.12 was easily achieved. With reference to Fig. 9.1 it may be seen that this design may be obtained simply by removing the directional coupler and the associated RF mixer, and changing the switch to position (2). The realisation of this design is shown in Figs. 9.3 and 9.4. In Fig. 9.3 a front view of the element is given, showing the arrangement of the circulator and single mixer. In practice a line stretcher was included between the circulator and the aperture to provide the path length adjustment described in Chapter 7 for minimising the effects of mutual coupling. Also, for the purpose of setting up the required path length, a directional coupler was placed before the RF mixer in the elements actually used in the experiments, to provide monitoring of the power at this point. Fig. 9.4 provides a rear view of the element and shows the circuitry associated with the operational amplifier, the variable gain (20 - 40dB gain) low noise amplifier and the mixers.

9.2 Measurement Technique and Experimental Results

Taking first the element corresponding to the design of Fig. 7.6, the open ended waveguide apertures of four elements were brought together to form an E-plane array with the waveguide broad walls in direct contact. The inter-element spacing was 1.3cm., corresponding to 0.45λ at 10.4GHz. A flat sheet of microwave absorbing foam brought up to the plane of the apertures was used to overcome

reflections from the array supporting structure.

The microwave reference signal at frequency 10.34GHz was distributed to the array elements via a 4 way power divider ; a line stretcher was included at each output of the power divider to provide fine phase adjustment of the element RF inputs. The IF inputs to the elements were derived from four independent PLL phase shifters, all locked at 8th harmonic. For these simple experiments, each phase shifter was controlled by means of a push-button which triggered the monostable multivibrator in the circuit described in Chapter 8. Use of the push button advanced the output phase by one increment of 45°; larger phase shifts were obtained by repeating this operation.

The array was mounted on a stepper-motor driven turntable. An analogue voltage proportional to angle was derived from the stepper motor controller via a pulse counting technique ; this voltage was then used to drive the horizontal axis of an X - Y plotter on which the radiations patterns were recorded. A repositioning accuracy of $\sim 1^{\circ}$ was obtained from the turntable.

The array and turntable were positioned in an anechoic corner, the walls of which were covered by microwave absorbing material (Plessey type AF40). A 20dB gain horn placed in the corner was used to receive the radiated signal, which was then applied to a microwave spectrum analyser (AIL-Tech type 707). The distance to the horn was 140cm, which was significantly larger than the minimum required for far-field measurements given by $2D^2/\lambda$ where D is the overall array length. The value of this quantity for the experimental array was 19cm with D taken as 5.2cm.

The spectrum analyser was used to provide the function of a detector and logarithmic amplifier. With the analyser tuned to the received signal frequency and the scan rate turned to zero, the video output obtained was applied to the vertical axis of the X - Y plotter to give a logarithmic plot. The calibrated attenuator of the analyser was used to define the vertical scale on the plots.

CW transmissions were used to obtain the radiation patterns since the oscillators used in the experimental array contained Gunn diodes optimised for CW operation and difficulty was experienced in equalising their output powers and free running frequencies when pulsed. In general, however, diodes optimised for pulsed operation would be used in the active elements previously described.

As the initial step in the measurement of the transmission radiation pattern the element CW output powers were equalised to within 0.5dB by means of the Gunn bias supply voltages. Frequency variations resulting from changes in the bias voltage were overcome by retuning the oscillators via the standing voltage applied to the varactor. With the array positioned with the receiving horn in the broadside direction, the IF phase shifters were initially used to broadly maximise the received power. The line stretchers in the RF reference inputs to the elements were then used to provide fine phase control to finally maximise the broadside power and to match the sidelobe powers and null depths of the radiation pattern obtained. From this starting position, steered beams were obtained by simply applying phase gradients across the array with the digital IF phase shifters. The measured radiation patterns with this array are shown in Figs. 9.5 to 9.13 ; in each case the phase shifts introduced to steer the beam away from the broadside beam position are shown. Fig. 9.5

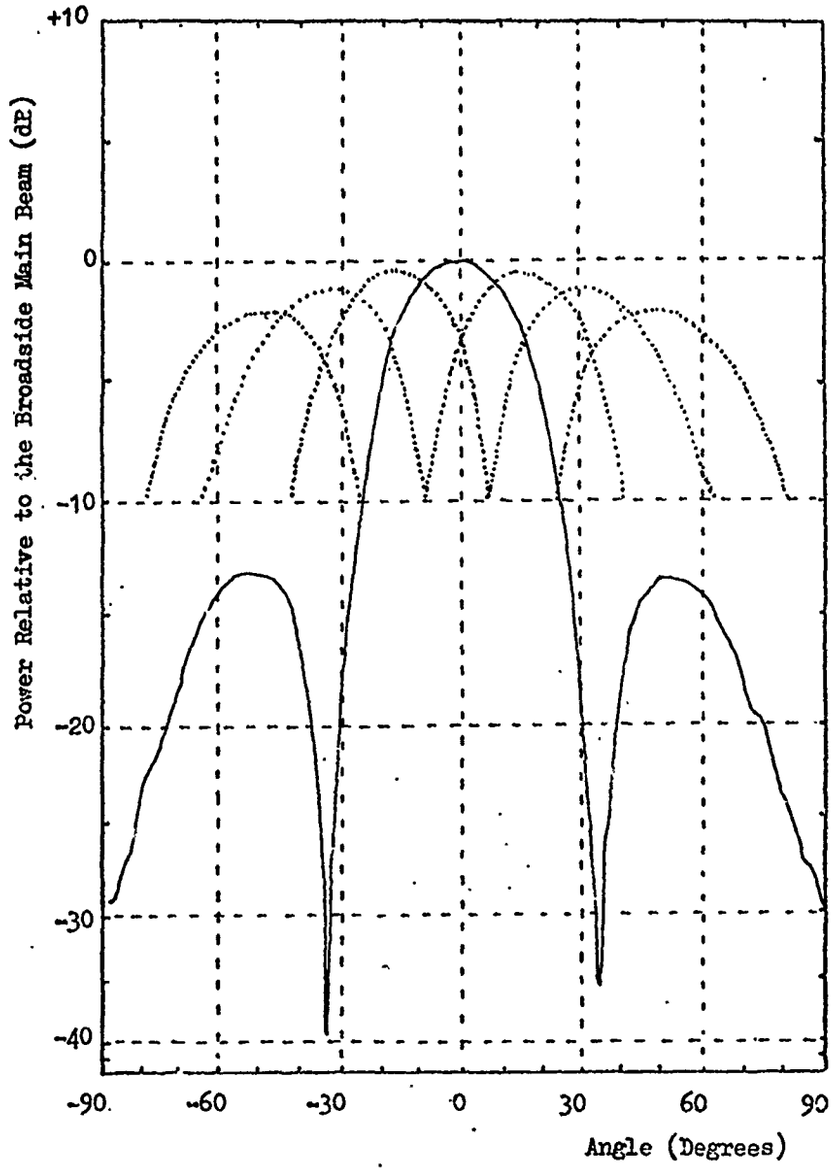


Fig. 9.5 Measured Broadside Radiation Pattern and Peaks of Steered Beams Using the Element Design of Fig. 7.6

shows the broadside pattern and for comparison the peaks of the steered beams. The broadside pattern agrees closely with that which would be expected from theory for a uniformly illuminated array of this size. The theoretical angles from broadside of the first nulls, given by

$$\pm 2\sin^{-1}\left[\frac{\lambda}{Nd}\right]$$

where N is the number of elements and d is the inter-element spacing, are $\pm 33.748^{\circ}$, the experimentally obtained values may be seen to be in close agreement. The sidelobe level at -13dB is also in agreement with that expected.

Figs. 9.6 to 9.12, demonstrating that beam steering was successfully obtained, show the steered patterns obtained with 'linear' phase distributions on the array, i.e. with equal phase increments between elements. It may be seen that, as desired, the basic pattern shape is maintained in the steered patterns. The reduction in the peak of the main beam with increasing scan angle was found to correspond to the average of the element patterns, these having slight differences due to the different mutual coupling situations. That the element amplitudes and phases were well matched is demonstrated by the symmetry and the depth of the broadside null, of the pattern of Fig. 9.13.

For measurement of the transmission radiation patterns of an array with elements corresponding to the design of Fig. 7.12 using a single RF mixer, the same open-ended waveguide apertures were used. The element configuration was altered to the basic form shown in Fig. 9.3, but including in addition the line stretcher in the aper-

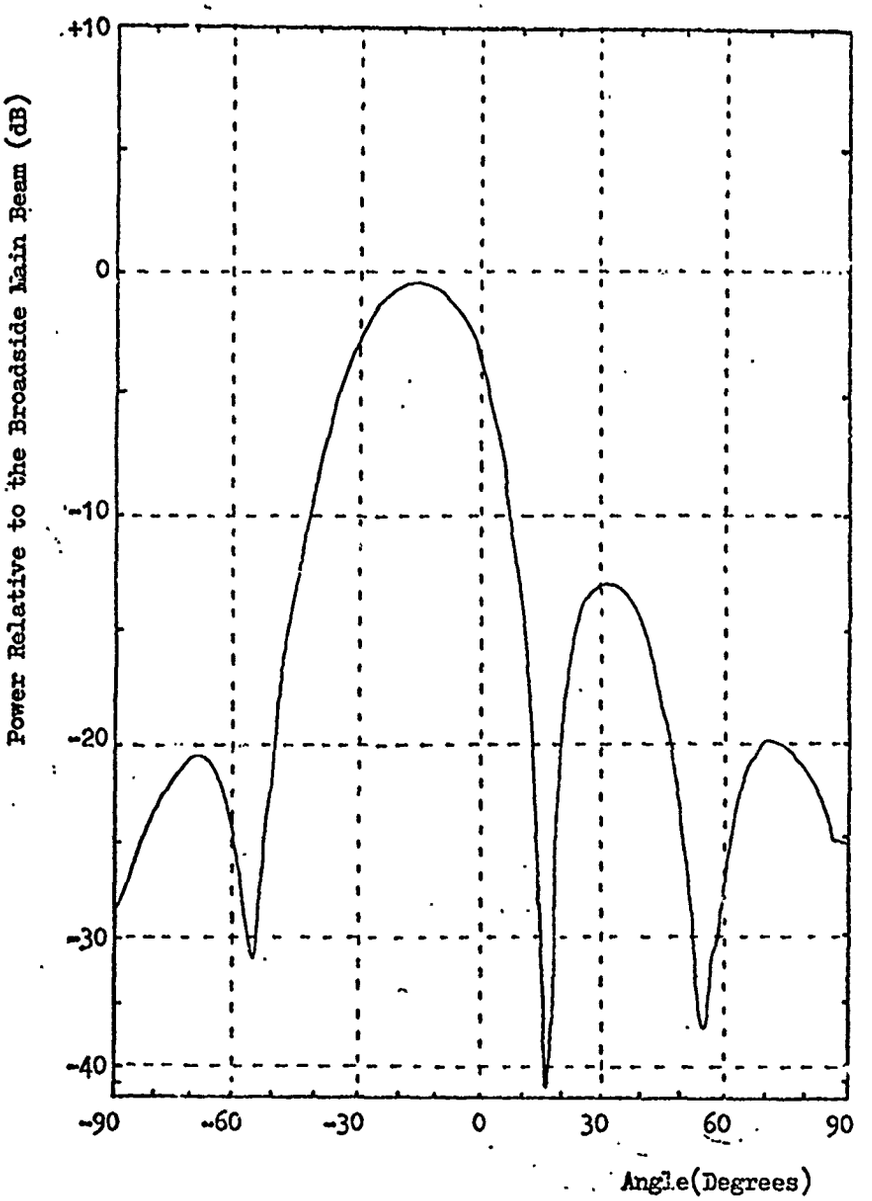


Fig. 9.6 Steered Transmission Radiation Pattern

Phase Settings : 0°, 45°, 90°, 135°

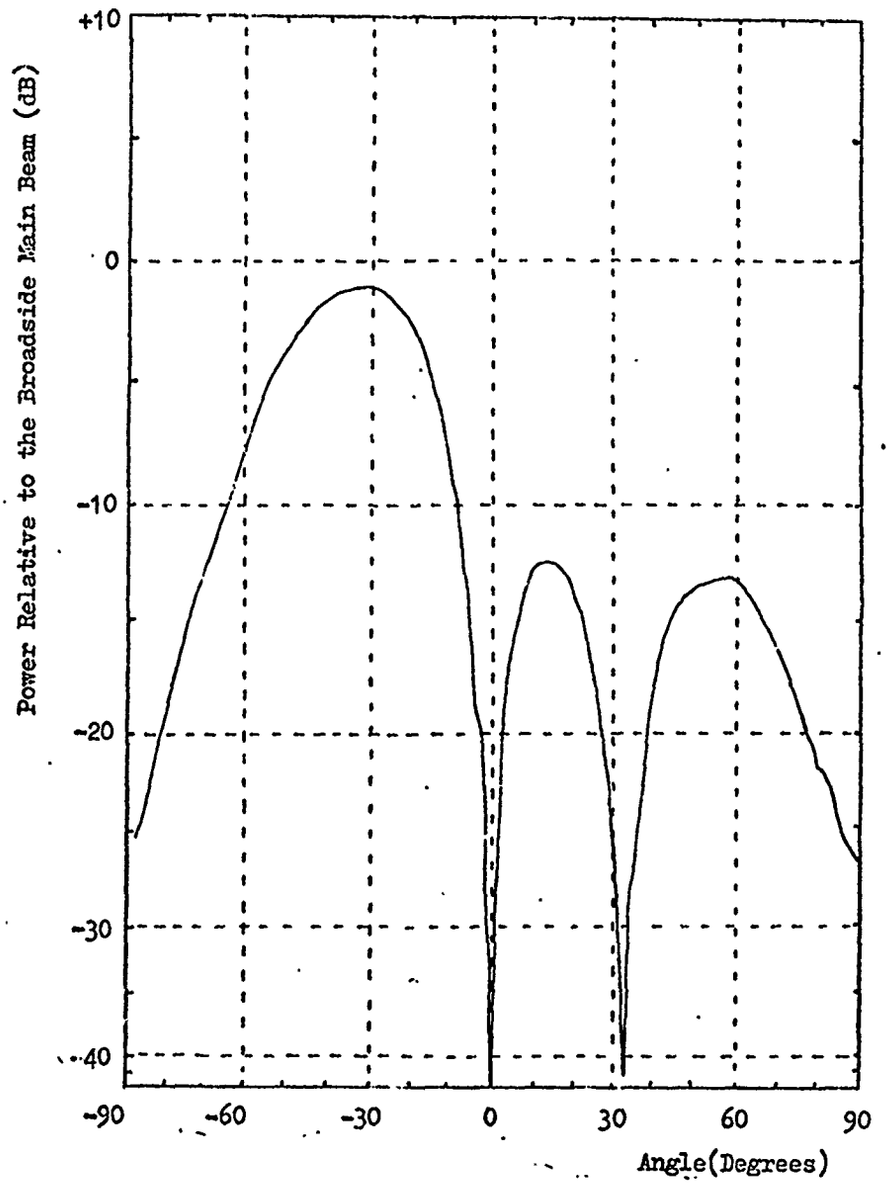


Fig. 9.7 Steered Transmission Radiation Pattern

Phase Settings : 0°, 90°, 180°, 270°

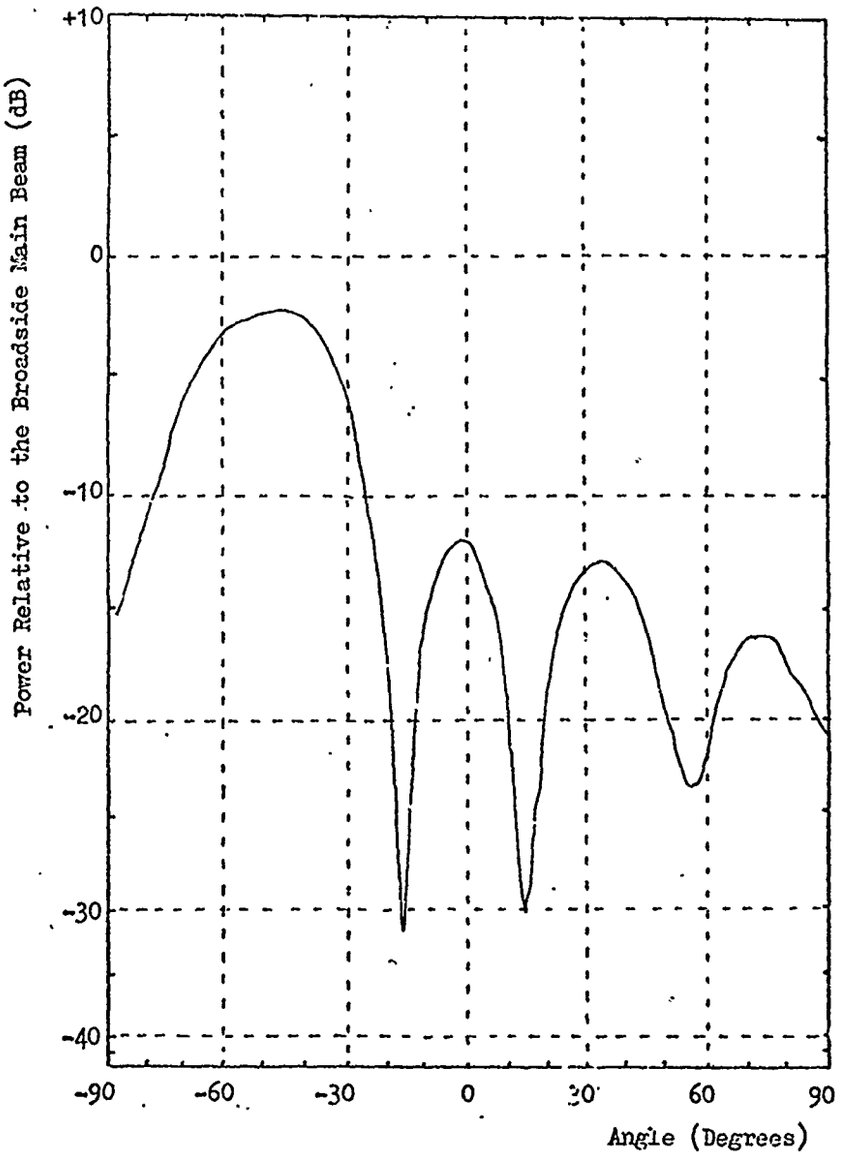


Fig. 9.8 Steered Transmission Radiation Pattern

Phase Settings : 0°, 135°, 270°, 45°

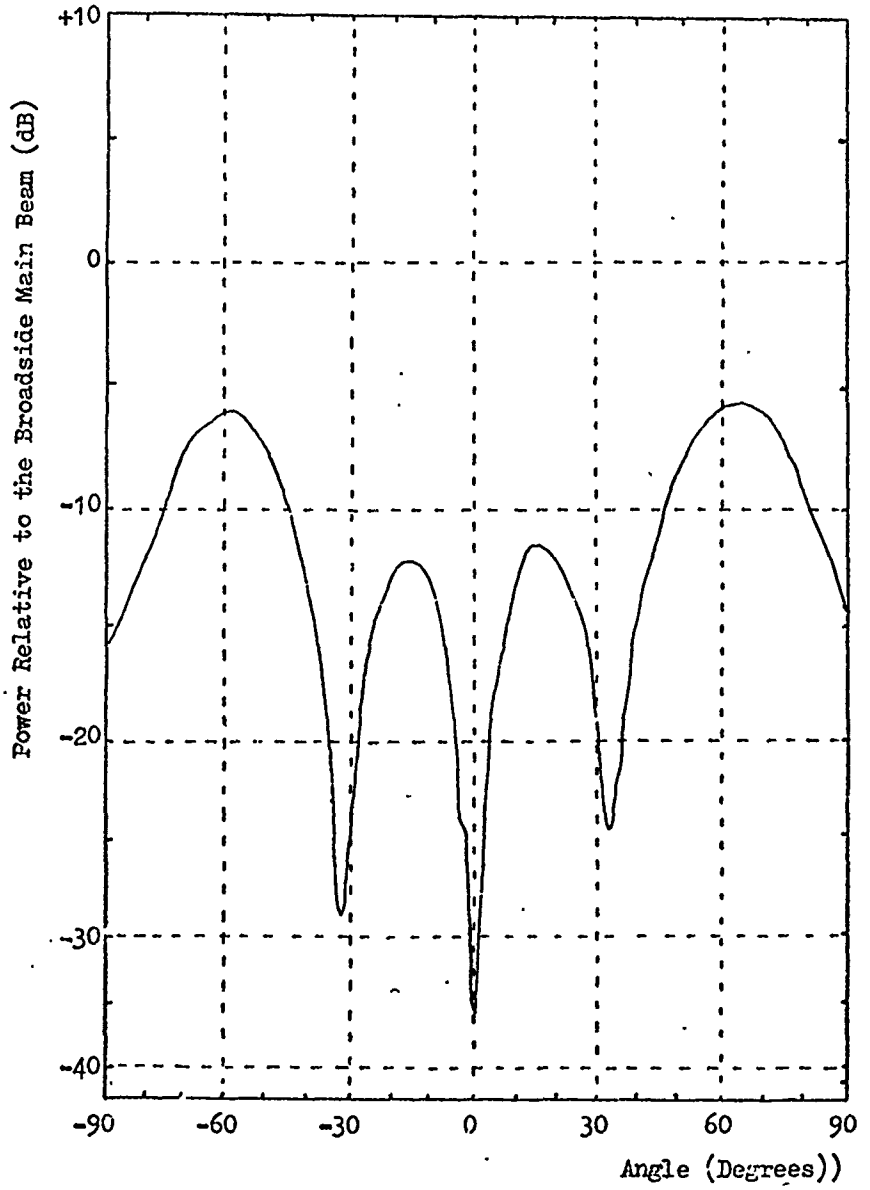


Fig. 9.9 Steered Transmission Radiation Pattern

Phase Settings : 0^{o}, 180^{o}, 180^{o}, 180^{o}

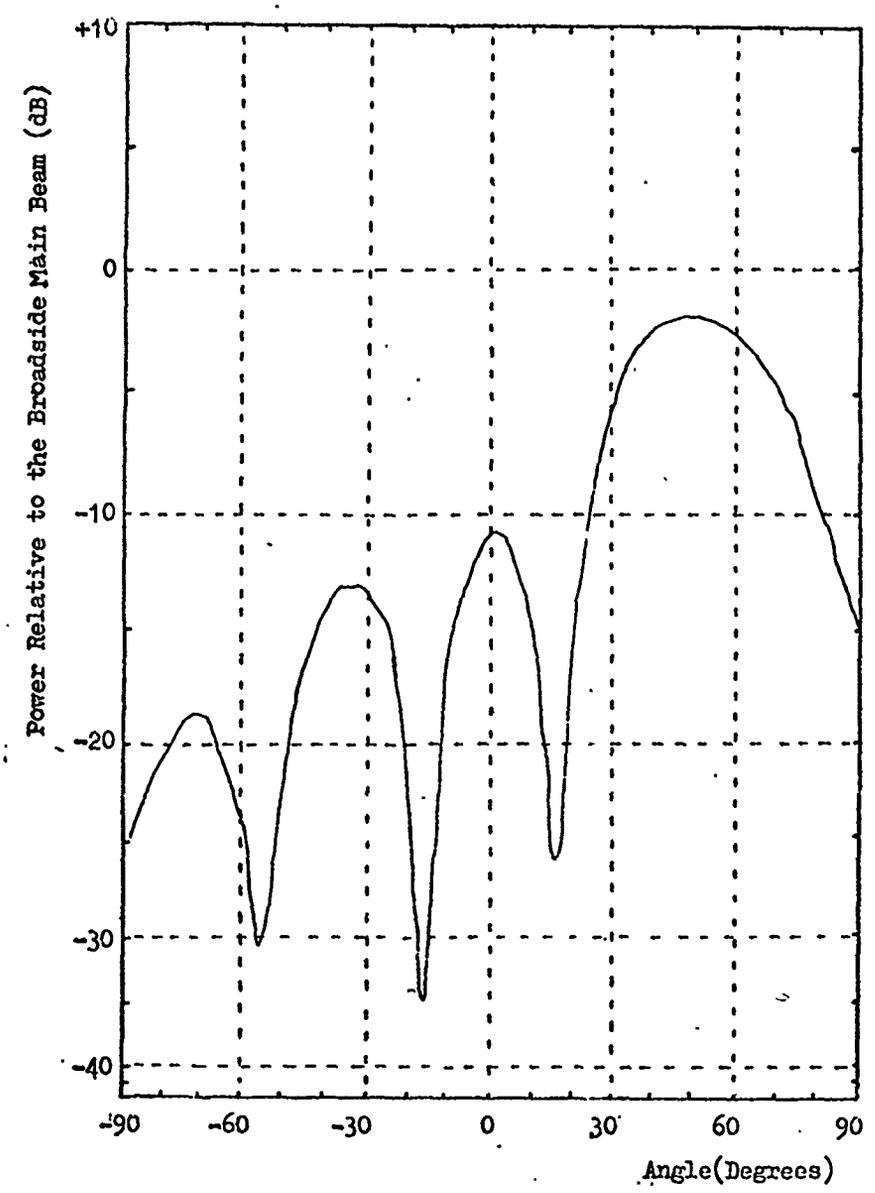


Fig. 9.10 Steered Transmission Radiation Pattern

Phase Settings : 0^{o}, 225^{o}, 90^{o}, 315^{o}

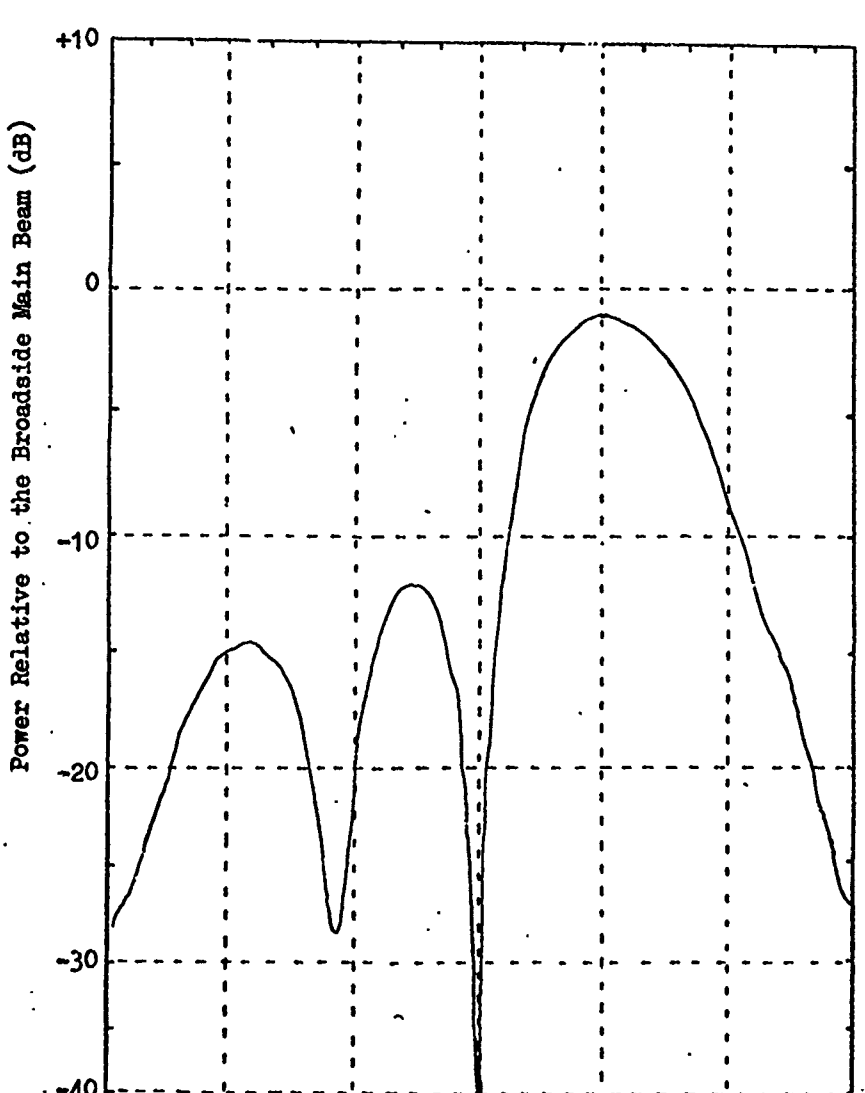


Fig. 9.11 Steered Transmission Radiation Pattern

Phase Settings : 0°, 270°, 180°, 90°

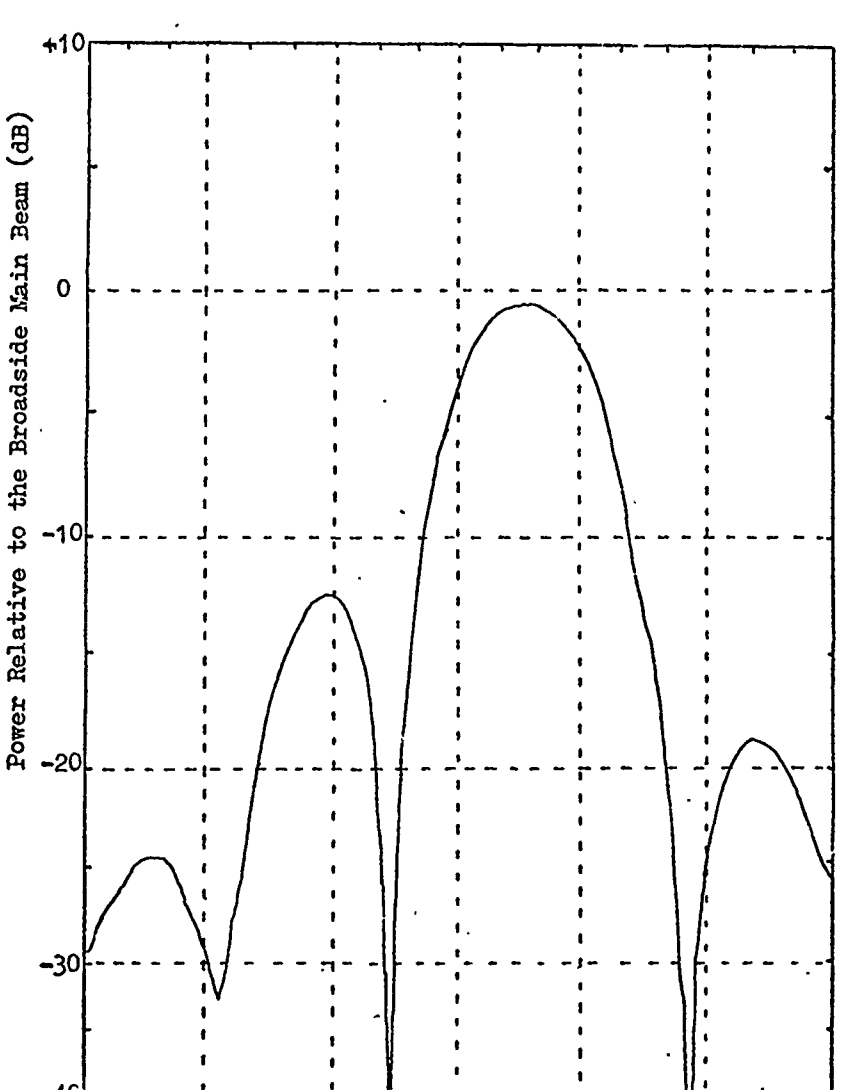


Fig. 9.12 Steered Transmission Radiation Pattern

Phase Settings : 0°, 315°, 270°, 225°

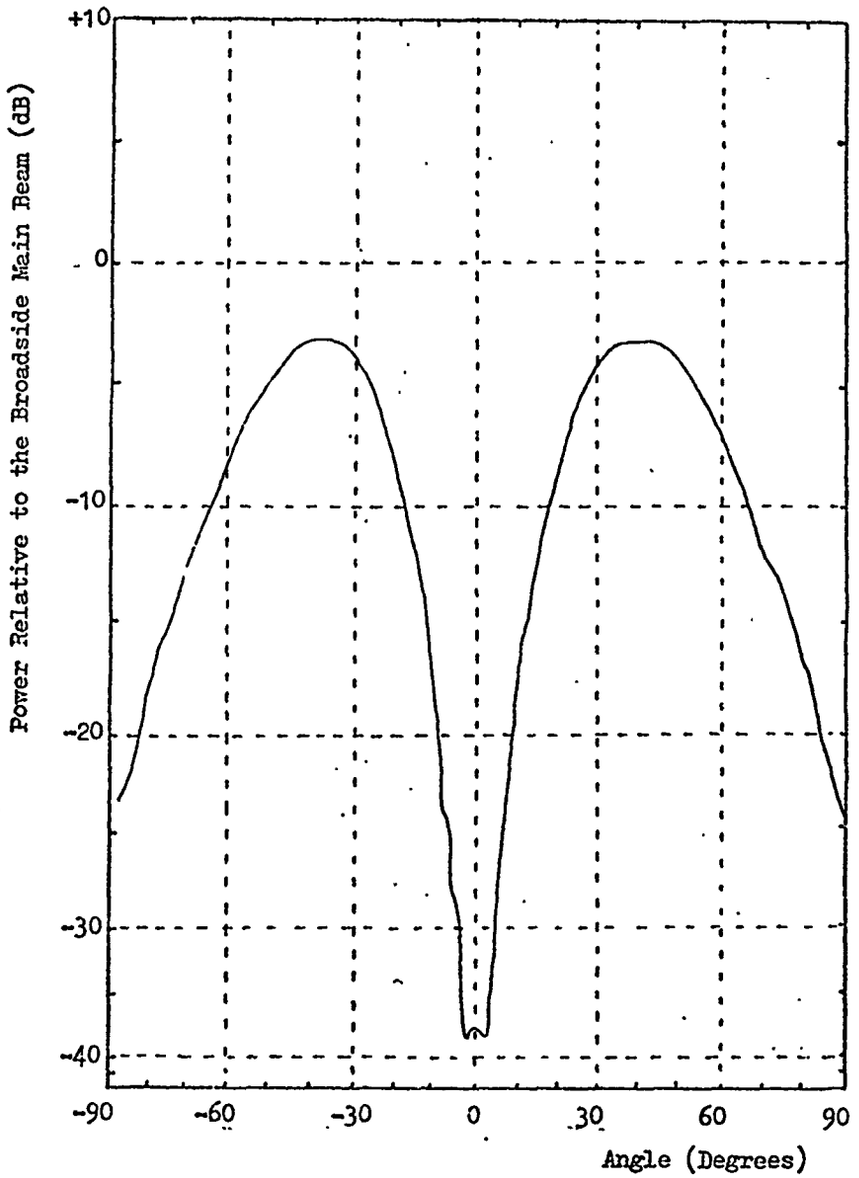


Fig. 9.13 Radiation Pattern Illustrating the Amplitude and Phase Match between Elements

Phase Settings : 0^{o}, 180^{o}, 180^{o}, 0^{o}

ture feed and the direction coupler preceding the mixer, for minimising the mutual coupling effects. The measured circulator leakage in the reverse direction was $\approx$20dB. The level of mutual coupling for E-plane open ended waveguides is known to be particularly high however, and in practice a level of $\approx$ -10dB between adjacent elements was found to exist. The mutually coupled signal was therefore the dominant term in the combined signal appearing at the signal input of the RF mixer.

Previous computer simulation described in Chapter 7 using the program in Appendix 2 for the case of a strongly dominant mutually coupled signal failed to produce a conclusive result ; although the aperture feed length adjustment procedure in the program successfully produced a broadside beam, any attempt to steer the beam resulted in the program being unable to converge on a solution. It was found in the experimental results for this situation that the element VCOs could not be locked to the reference signals with this level of mutually coupled power. The 'noisy' spectrum obtained at the receiver indicated the presence of instability in the array. Since the effective feedback path includes several of the neighbouring elements in this situation, it may be expected simply on the grounds of the increased loop delay alone that this arrangement would be more prone to instability. This aspect of the work requires further investigation.

As a means of demonstrating the performance of this element design under conditions of lower mutual coupling, 10dB attenuators were included in the aperture feeds of the four elements. This had the effect of reducing the transmitted power by 10dB and the mutually coupled power appearing at the signal port of the RF mixer by 20dB. The mutually coupled power at the RF mixer was now typically 10dB

less than that due to the circulator leakage. It was found in this case that the VCOs could be locked to the reference signals without difficulty.

The precedure used for setting up the broadside radiation pattern was as follows :

1) The broadside beam was roughly maximised with the IF phase shifters
2) The line stretcher in the element feed was adjusted to maximise the power into the RF mixer (the power at this point was monitored via directional couplers)
3) Steps 1) and 2) were repeated until no noticeable improvement occurred.
4) The line stretchers in the RF reference inputs were then used to provide fine phase control to give the best pattern shape.

The measured broadside radiation pattern and the peaks of the steered patterns are shown in Fig. 9.14. It may be seen that the broadside pattern exhibits deep nulls and is comparable to the pattern of Fig. 9.5. For the broadside case however, adjustment of the input phases was used to offset any phase errors introduced by the mutual coupling : for the pattern steered away from broadside with the IF phase shifters, it would be expected that phase errors would be introduced by the mutual coupling. Evidence of this may be seen in the steered patterns shown in Figs. 9.15, 9.16 and 9.17. In comparison with the plots of Figs. 9.6, 9.7, 9.8 it may be seen that some degradation of the pattern shape has occurred and the nulls are no longer as deep. However, the pattern shape in general remains similar to that previously obtained as may be expected since the level of the 'effective' mutually coupled signal appearing at the RF mixer is relatively small compared to the circulator leakage.

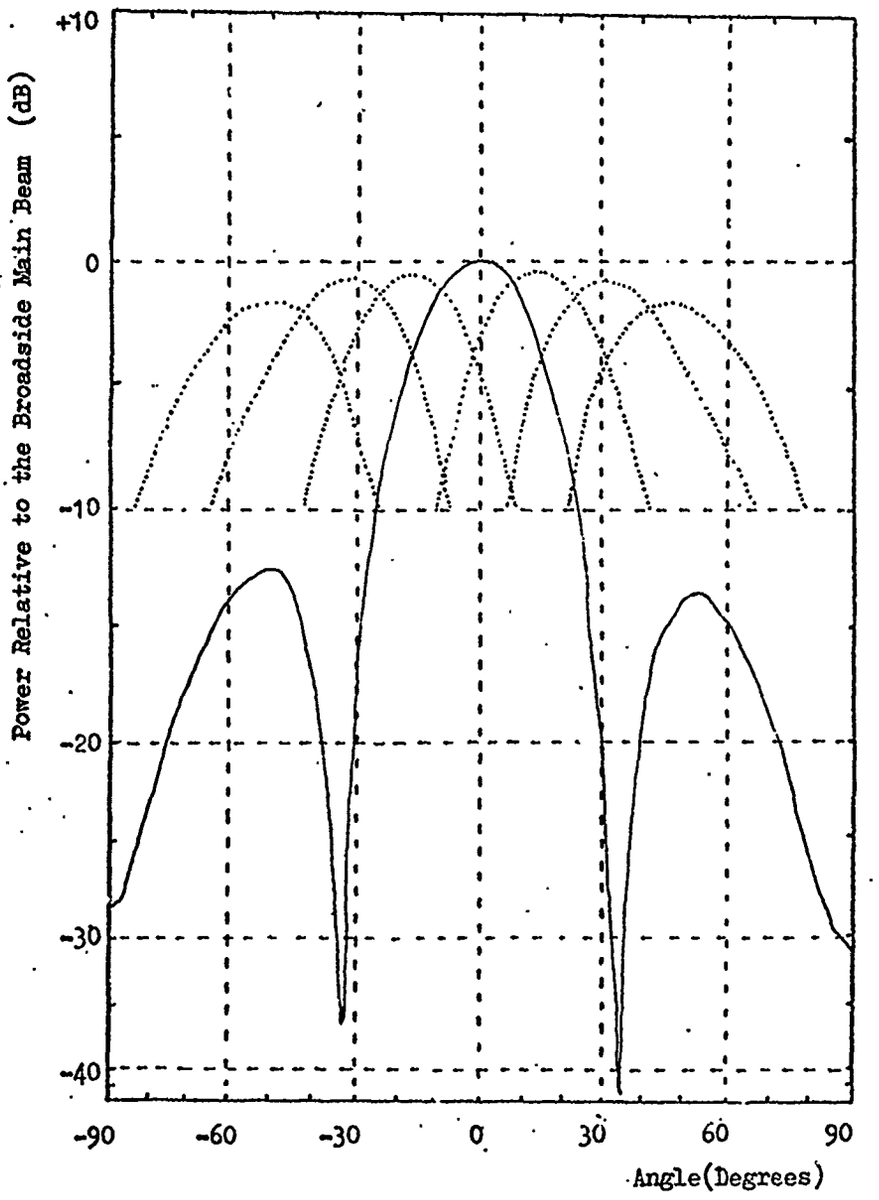


Fig. 9.14 Broadside Radiation Pattern and Peaks of Steered Beams Using the Element Design of Fig. 7.12

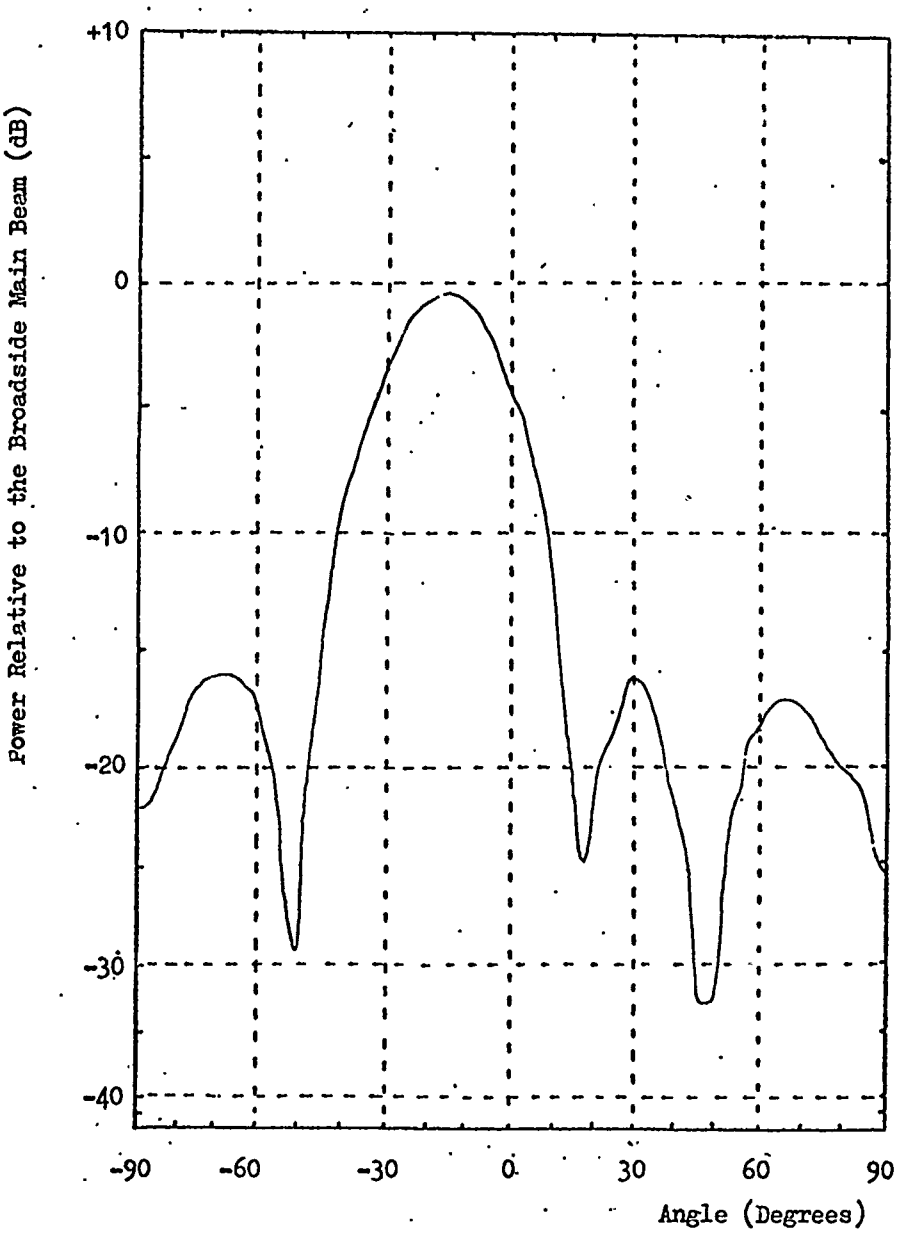


Fig. 9.15 Steered Transmission Radiation Pattern

Phase Settings: 0°, 45°, 90°, 135°

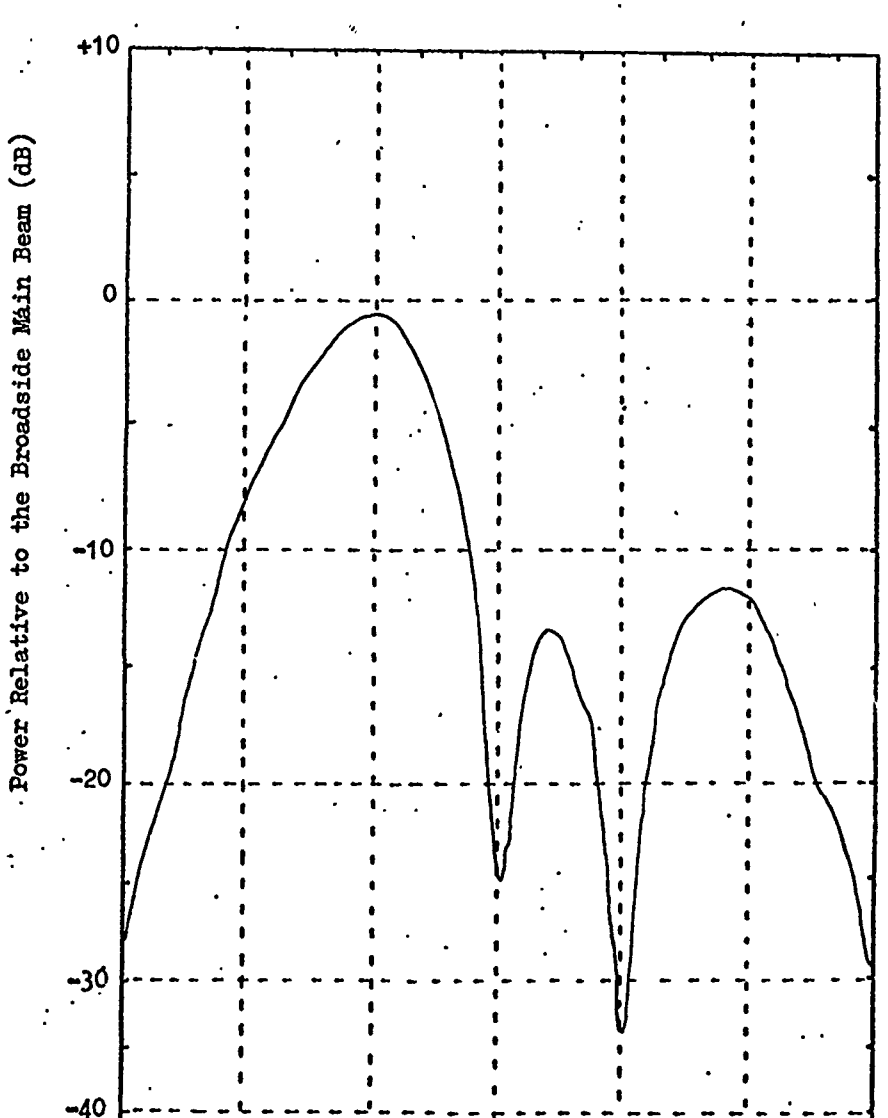


Fig. 9.16 Steered Transmission Radiation Pattern

Phase Settings: 0°, 90°, 180°, 270°

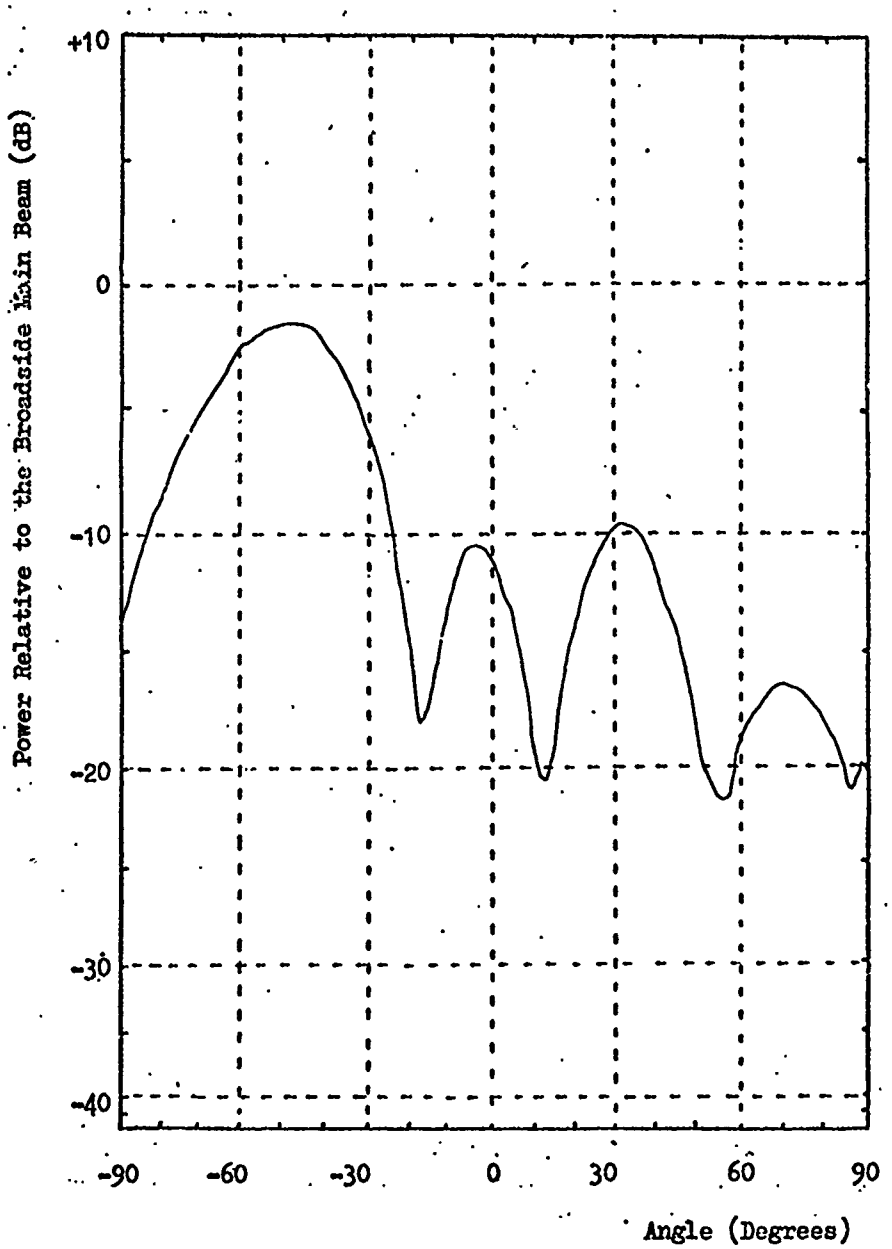


Fig. 9.17 Steered Transmission Radiation Pattern

Phase Settings: $0^{\circ}, 135^{\circ}, 270^{\circ}, 45^{\circ}$

Comparing the measured broadside pattern of Fig. 9.14 with the computed broadside pattern for a four element array including the 10dB attenuators shown previously in Fig. 7.17, two slight differences may be noted. First, the pattern level at $\pm$ 90° is greater in the computed pattern ; this corresponds to a difference between the element pattern used in the program and that obtained experimentally ; the flat sheet of microwave absorber surrounding and in the plane of the experimental open ended waveguide apertures, produced a low level of radiation at $\pm$ 90°. Secondly, the nulls of the experimental pattern are lower than those computed. This results from an unintentional difference in the setting up procedure for the two arrays ; in the program, adjustment is made only to maximise the sum of the circulator leakage and the mutual coupling at the mixer input ; in the experimental array the final adjustment was applied to the reference input phases to obtain the best pattern shape. Noting that the computed steered patterns were steered in the opposite direction to those measured experimentally, broad agreement in the pattern shapes may be seen between the patterns of Figs. 7.18, 7.19, and 7.20 and those of Figs. 9.16, 9.16 and 9.17. The difference between the patterns are again probably due to the different setting up procedures used.

Finally, measurements were taken of the radiation patterns produced on reception to demonstrate the indirect phasing approach in which phase shifts are applied indirectly by mixing the received signal with the phase shifted IF reference signal. The received signal path which may be seen from Fig. 9.1 to be common for both element designs, consisted of downconversion of the signal received by the open-ended waveguide aperture, amplification ($\sim$25 dB gain) in a variable gain low noise amplifier and then mixing with the IF reference signal. The element output at the sum frequency of the IF mixer inputs was

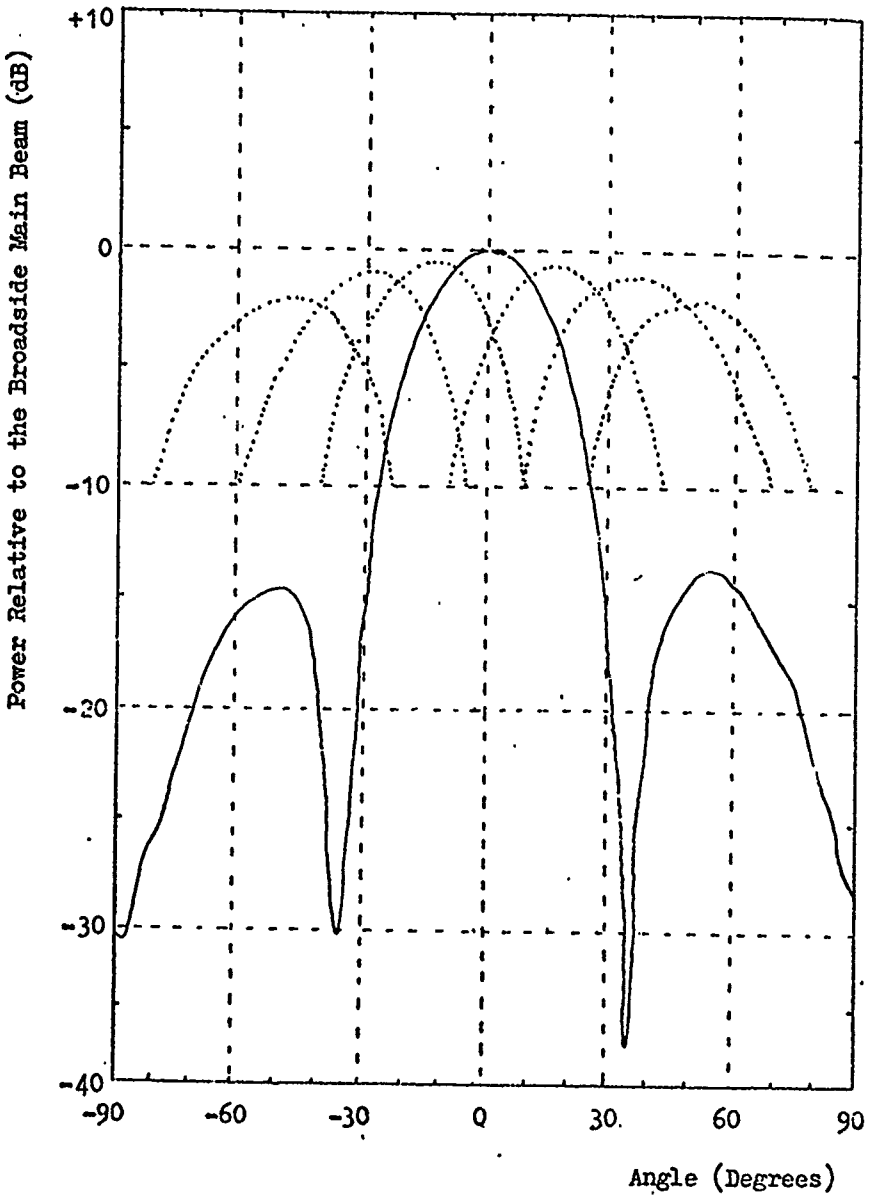


Fig. 9.18 Broadside Radiation Pattern and Peaks of the Steered Beams on Reception

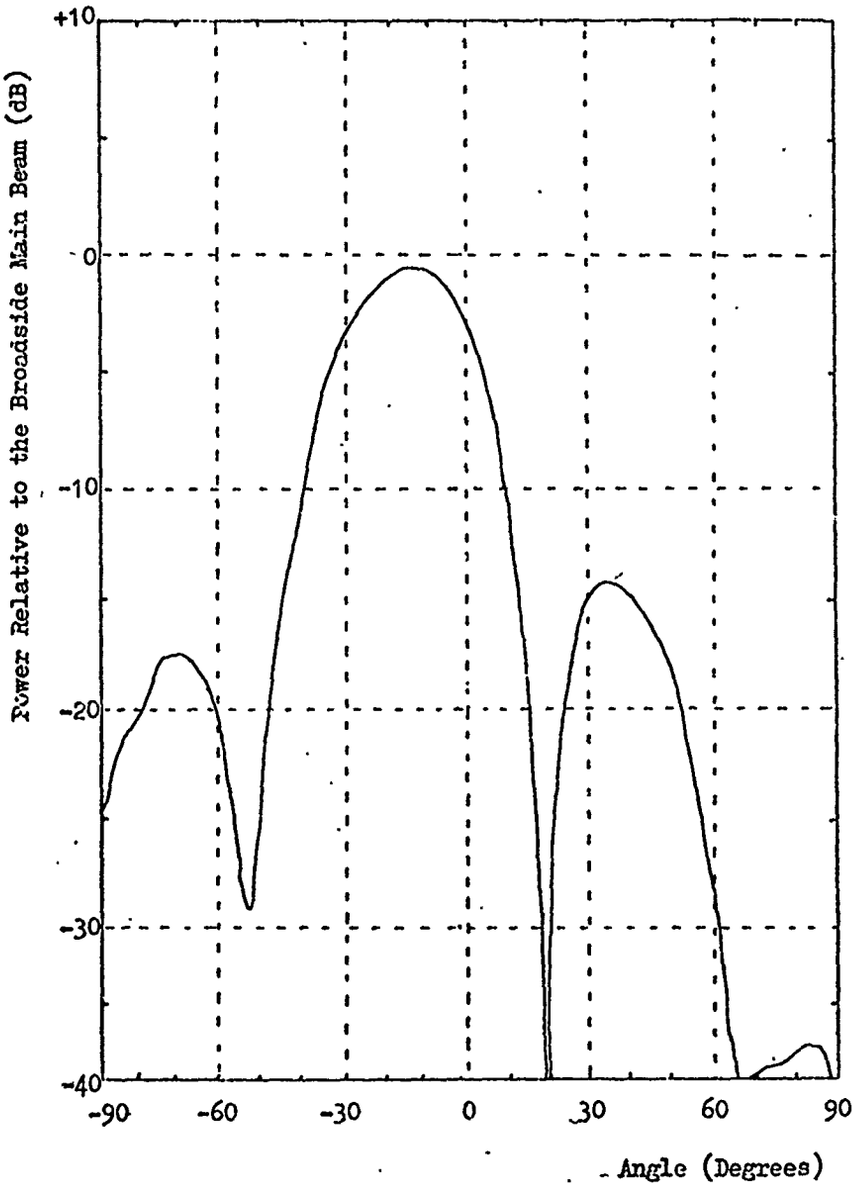


Fig. 9.19 Steered Reception Radiation Pattern

Phase Settings : 0°, 45°, 90°, 135°

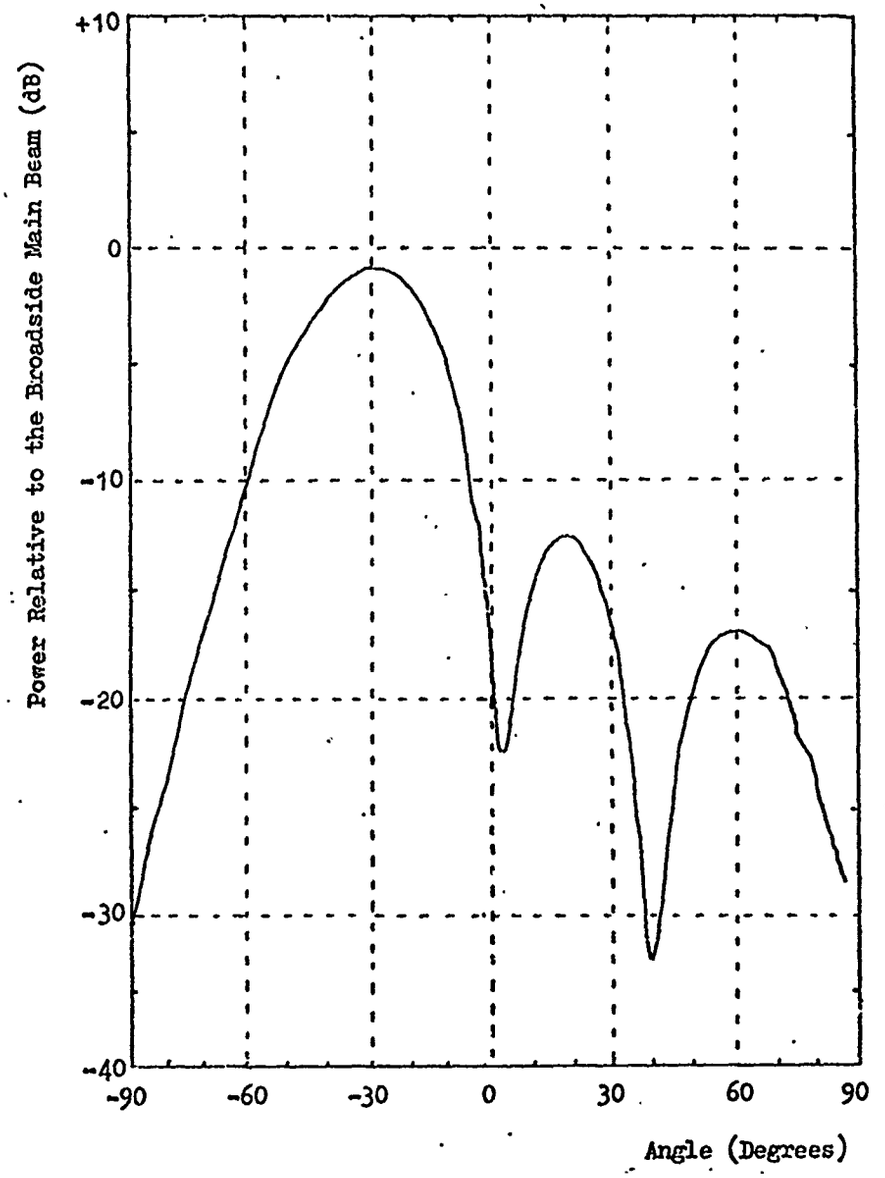


Fig. 9.20 Steered Reception Radiation Pattern

Phase Settings : 0°, 90°, 180°, 270°

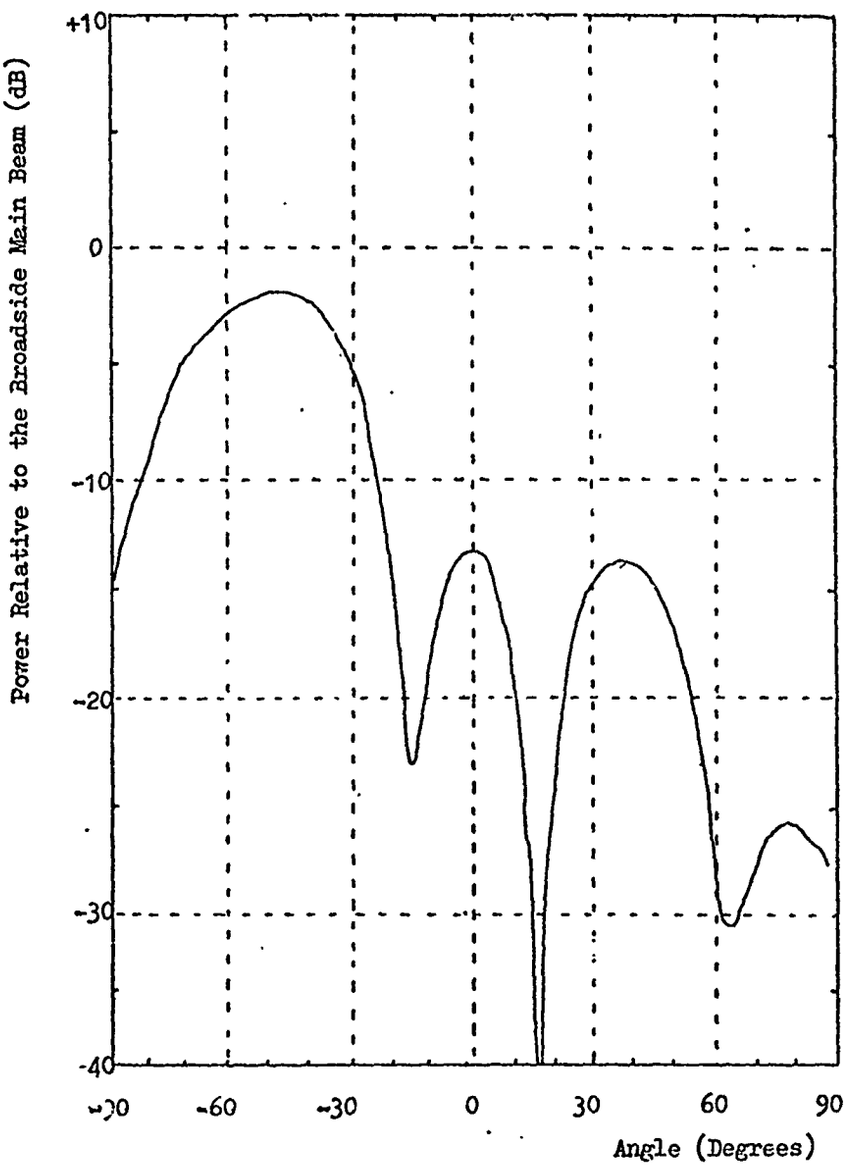


Fig. 9.21 Steered Reception Radiation Pattern

Phase Settings : 0°, 135°, 270°, 45°

applied to a 50-500MHz 4-way power combiner (Merrimac). The combined power was then applied to a spectrum analyser, as before, to provide detection and logarithmic amplification. The waveguide horn in the anechoic corner which was previously used for reception was now used to transmit a CW signal at 10.4GHz With the IF reference signal at 60MHz, an RF reference signal at 10.328GHz was chosen to give an element output at 132MHz.

Initially the element output powers were equalised by positioning the array with the transmitting horn in the broadside position. Examining the element outputs at 132MHz in turn with the spectrum analyser, the variable gain amplifiers were used to equalise the output powers. With the array in the same position, the output phases were equalised by maximising the output of the combining network by adjustment of the line stretchers in the RF reference inputs to the elements.

The broadside reception pattern and the peaks of the steered reception main beams are shown in Fig. 9.18. Three steered patterns are shown in Figs. 9.19, 9.20 and 9.21. It may be seen that these patterns are very similar to those produced on transmission, as may be expected on the basis of reciprocity.

CHAPTER 10

AN EXPERIMENTAL EIGHT ELEMENT ACTIVE ARRAY WITH PROGRAMMABLE BEAM STEERING CONTROLLER

10.0 Introduction

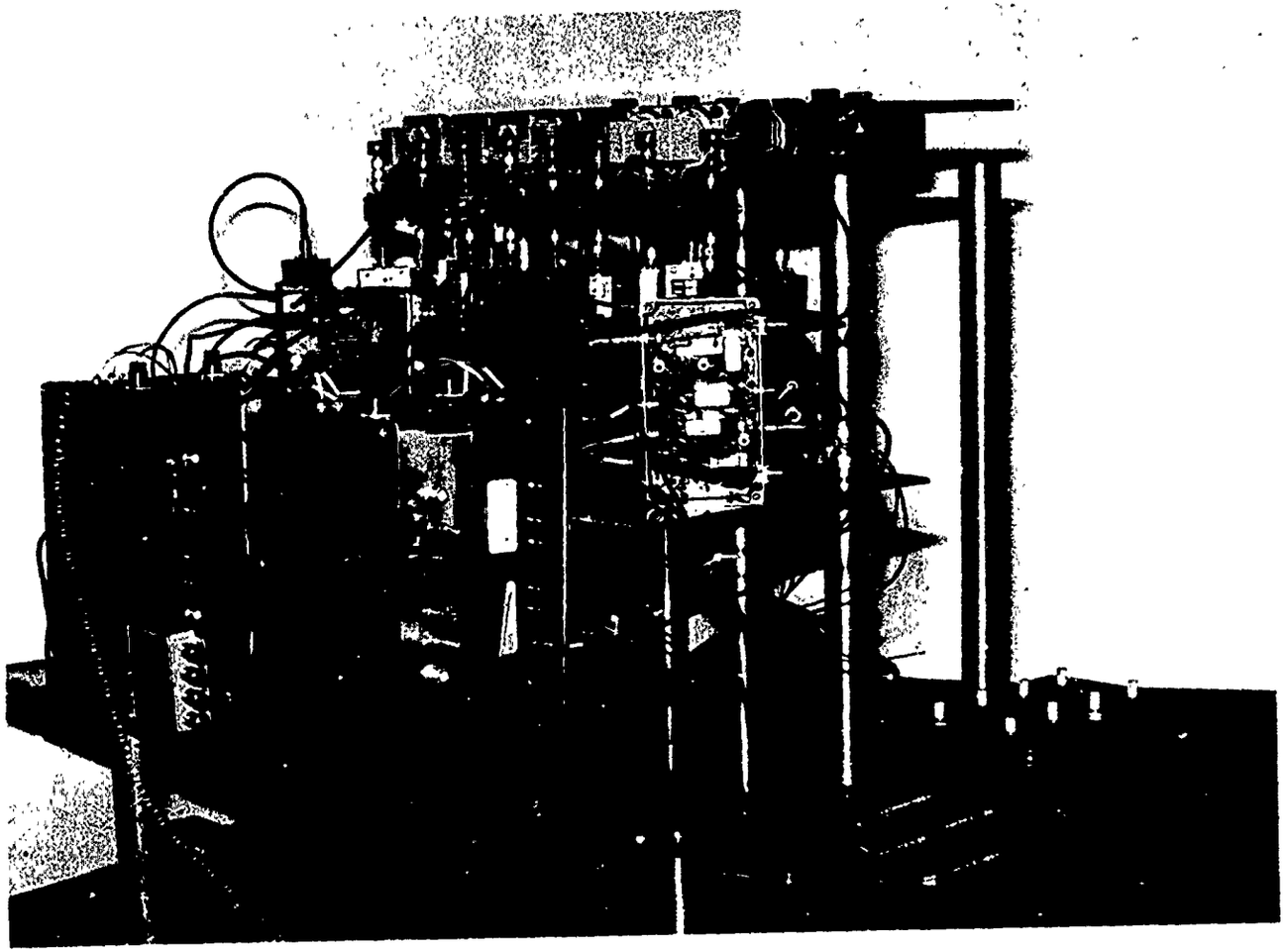
A four element array provides a rather large beamwidth and also presents a highly non-uniform situation for each array element in regard to mutual coupling. With eight elements, the central array element is now more closely in the environment of a very large array. Also, with eight elements, the phase steering commands are now sufficiently complex that some form of controller is required and this allows different philosophies for beam steering control to be investigated.

10.1 Eight Element Array

A further four elements of the type described in Chapter 9 were constructed [55]. These were assembled with the original four to form an eight element E-plane array, the broad walls of each waveguide radiating element being in direct contact with the neighbouring element. A photograph of the array is shown in Fig. 10.1.

10.2 Beam Steering Controller

A block diagram of the control unit is shown in Fig. 10.2. Each element IF stage incorporates a phase detector to measure uniquely the phase state of the element with respect to the 60kHz signal derived from the 480kHz array reference. The output of the phase detector in each element is routed to a column of LED display lights, each LED corresponding to a particular phase state. For the 8 elements with 8 possible phase states (0°, 45°, 90°..... 315°), a matrix display of 8 X 8 LED's was used. The measured phase state is also coded into a 3-bit binary word which is presented to a comparator



Photograph of Complete Eight Element Array

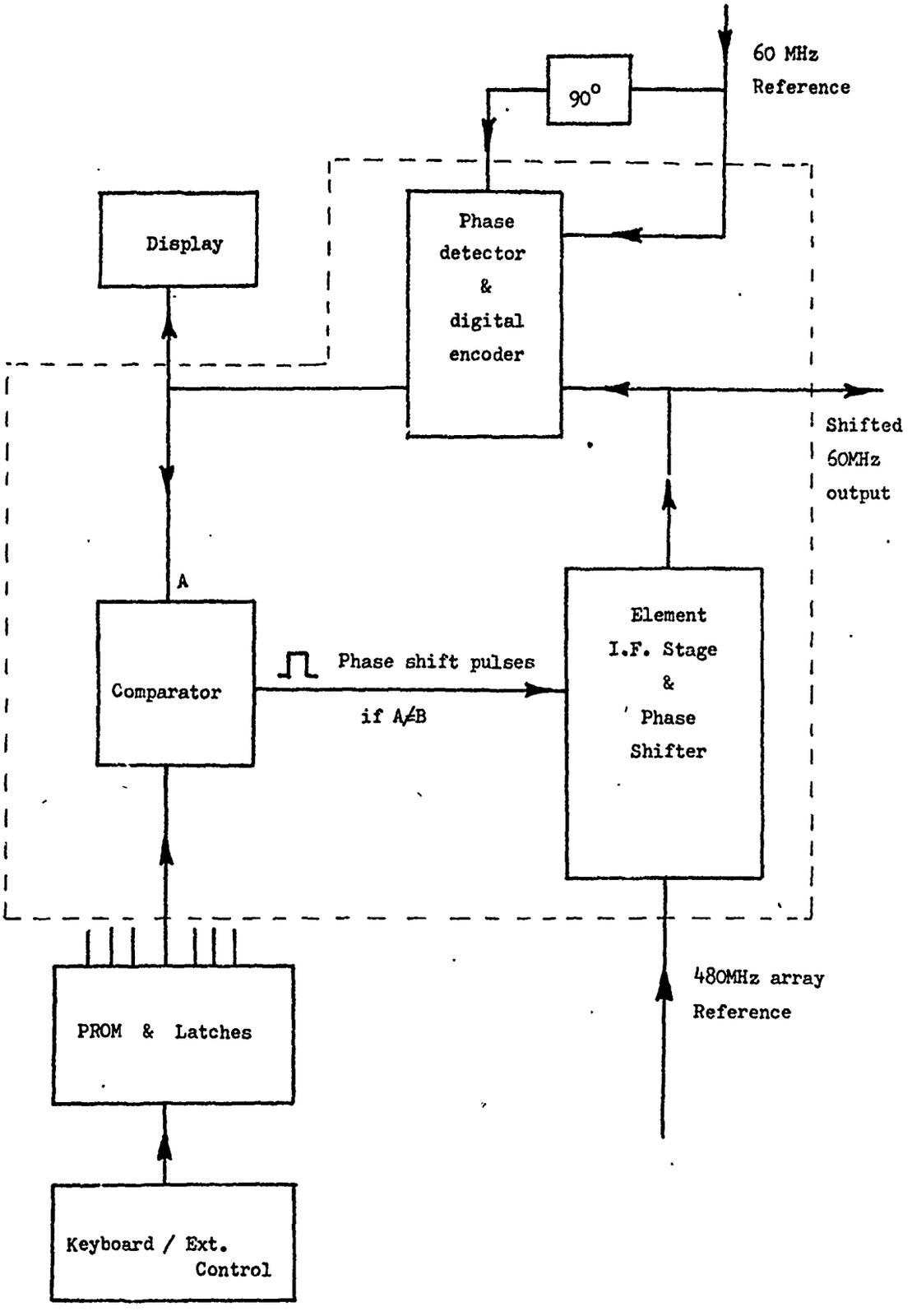


Fig. 10.2 Array Beam Steering Controller - Block Diagram

(input "A" in Fig. 10.2). If the phase word is not the same as that presented at the other input to the comparator (input "B" in Fig. 10.2), then phase shift pulses are applied to the element phase shifter from the comparator. The word presented at input "B" on the comparator is the required phase state of the element concerned, which is obtained from a PROM acting as a look-up table for phase states required to produce particular beam positions.

To access a particular beam position, a 3-digit number is entered on a conventional keypad; this is automatically converted to a binary address for the PROM. The PROM (Intel 1702A-2) is ultra-violet erasable in case reprogramming is needed; it is presently organised as 256 words of 8 bits. For each beam position 8 words are used to provide the 8 required phase states. Only the three least significant bits of each word are used, allowing space for expansion to 4 or 5-bit phase shifting if required. With the present PROM, 32 beam positions may be accommodated. The complete real cycle time for the PROM is 8μs after which the required phase data are presented to the comparators via latches (56). If the phase words at the comparator inputs are not the same on the leading edge of the phase detect strobe pulse, a phase shift pulse is applied to the phase shifter; 3μs after the phase shift pulse, the comparator output is strobed again, the process repeating as necessary until all the phase words are matched, whereupon shift pulses are inhibited.

The maximum number of phase bits any element might need to be advanced is 7 (i.e. 315°). At present this takes 35μs, giving a total phase shift time, for beam steering to a new position, of 43μs at absolute maximum; all elements are phase shifted in parallel mode since sequential shifting of elements would take an excessive time.

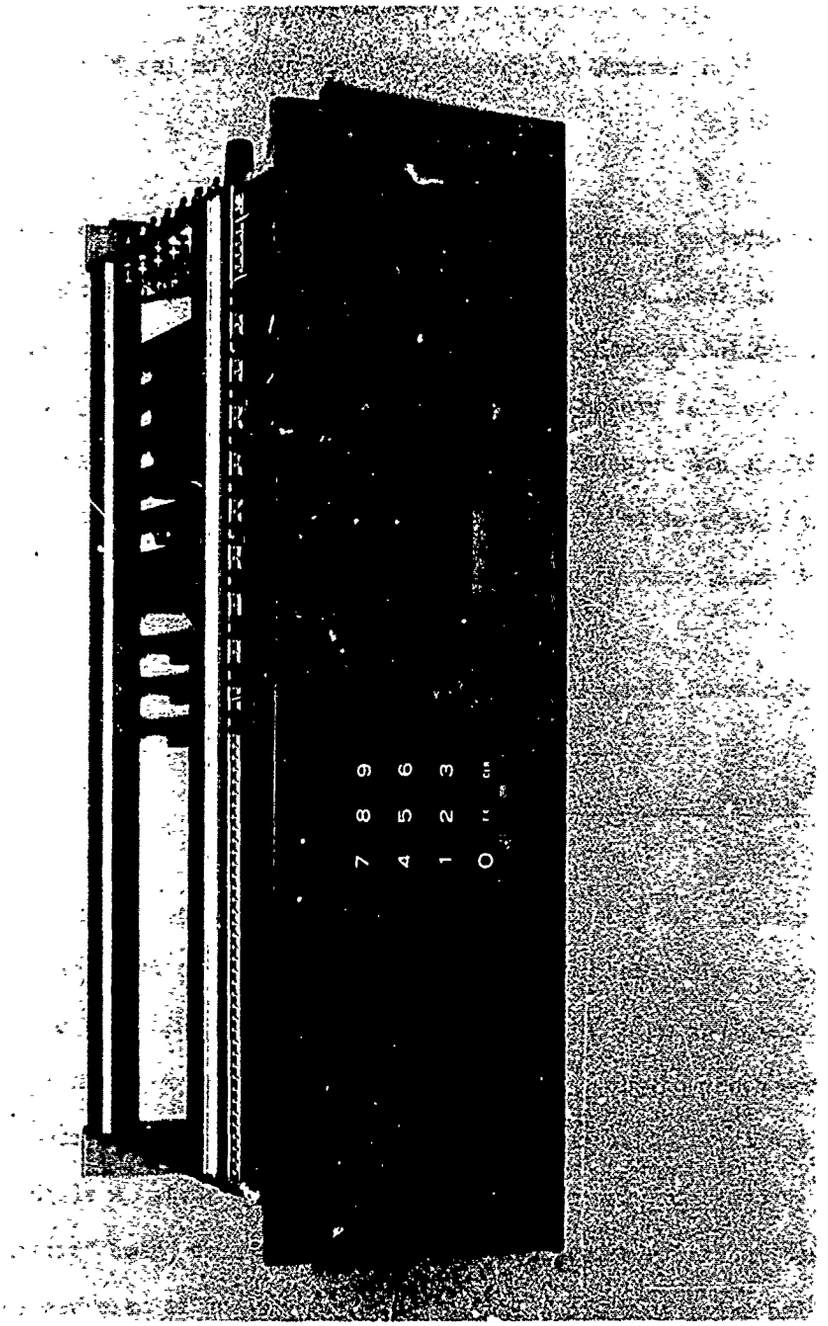


Fig. 10.3 Photograph of the Beam Steering Controller

The time for beam repositioning could be reduced from the 43μs maximum to 5μs maximum if Schottky TTL were used for the PROM and other circuits.

If the number of phase shift pulses to any element is more than 7, a fault has occurred within the element. By counting the number of pulses applied to each element, indication of phase shift malfunction is obtained. At present, a failure indication is given if 15 or more pulses are sequentially applied to a given element. With this "present phase state" feedback path, the system cannot produce incorrect phase state without error indication being given.

A photograph of the controller is shown in Fig. 10.3.

10.3 Measured Radiation Patterns

Using exactly the same measurement system and technique as given in Chapter 9, radiation patterns were plotted for a wide range of beam positions programmed into the controller. All elements were set to the same power output, giving a uniform illumination function to the array aperture. A steered beam pattern, for small beam steering angle is compared with the broadside beam in Fig. 10.4. A slight increase in sidelobe level is seen due to the coarse phase "staircase" along the array aperture. In Fig. 10.5 comparison is made between broadside and strongly-steered beams. It is pleasing to note that in this steered beam case the sidelobe level remains close to the -13dB theoretical for the uniformly illuminated aperture.

In all cases tested, very good agreement is obtained between computed and experimentally measured radiation patterns indicating that the

array behaviour is well-characterised and that accurate phase control is being achieved.

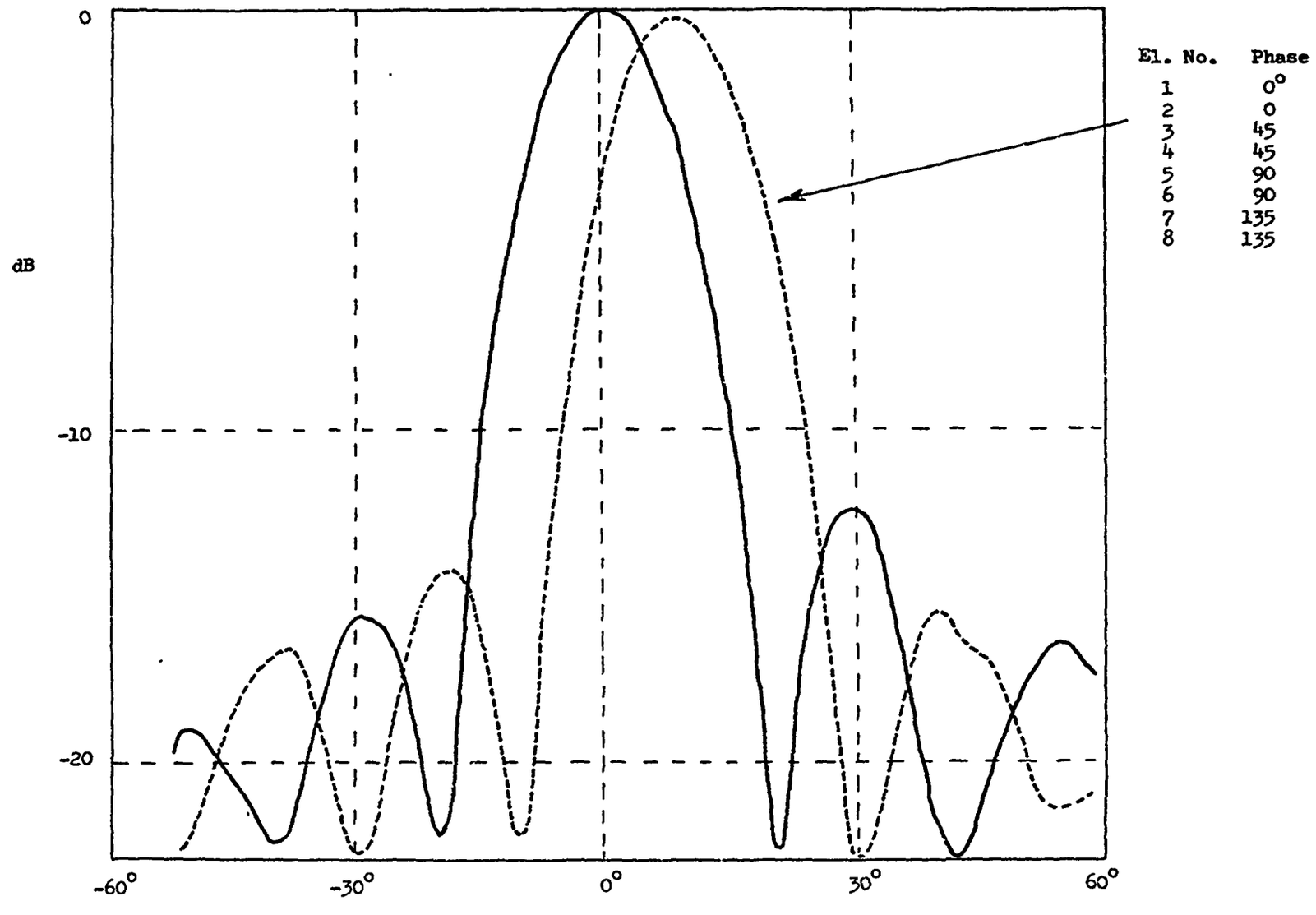


Fig. 10.4 Antenna Radiation Patterns, Broadside and Steered Beam

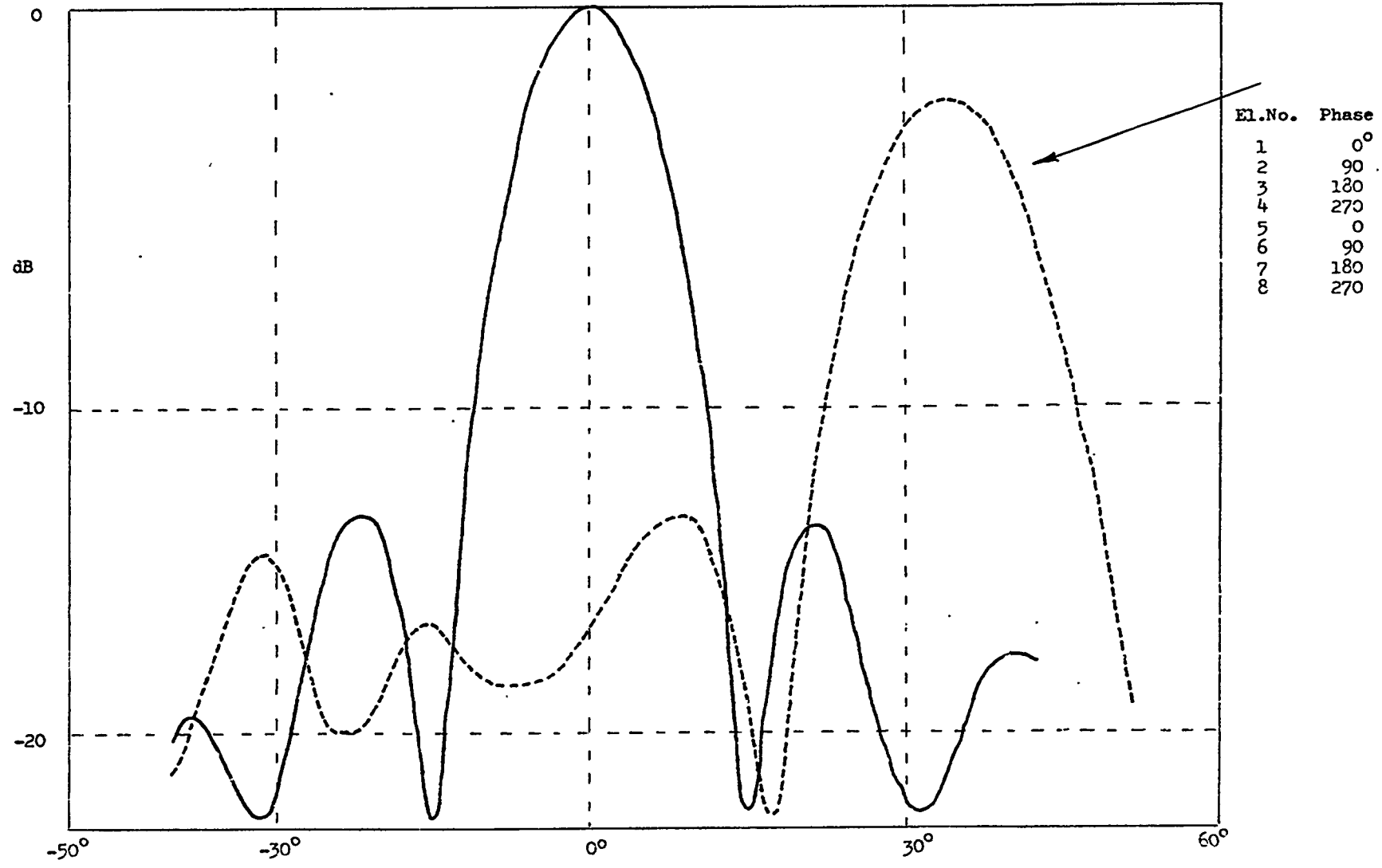


Fig. 10.5 Antenna Radiation Patterns, Broadside and Steered Beam

CHAPTER 11

MICROWAVE INTEGRATED CIRCUIT ARRAY ELEMENT DESIGN

11.0 Introduction

In order to demonstrate the viability of the array element design given in Chapter 10 as regards quantity production, a microwave integrated circuit (m.i.c.) version of higher output power has been constructed. Such a procedure is the next step in the evolution from a "breadboard" prototype to a fully engineered production version. Though the basic design is tested in the "breadboard" stage, new problems can arise in the transfer of that design from discrete components to an integrated circuit.

The m.i.c. allows very considerable cost reduction, particularly in quantity production, since the packaging of individual component parts is eliminated. This is particularly true of the active device providing the source of microwave power, where packaging and RF test comprise the major part of the device cost. For this reason, it was decided to use unpackaged microwave semiconductor devices (RF source, mixer diodes, etc.) in the m.i.c. element.

A choice also has to be made between various forms of m.i.c. construction, microstrip and stripline being the most common. Stripline has the advantage of lower r.f. power losses since it is an almost fully enclosed structure; however, this very aspect makes it a more difficult structure in which to incorporate microwave semiconductor devices and perform tuning adjustments. For these two reasons, if the m.i.c. is reasonably compact with short line lengths, it is generally preferable to make use of the microstrip configuration. Microstrip has therefore been chosen in the present work.

The remaining choice lies between thick and thin film technology for the formation of the microstrip lines and circuit elements. For higher microwave frequencies (X-Band and above) the normal choice is thin film technology because of the lower losses associated with the homogeneous and well-defined conductor layer. However, thin film technology requires high standards of circuit fabrication in regard to cleanliness and complex plant; it is therefore not so amenable to mass-production. Thick film circuits, by contrast, do not require vacuum processing, complex equipment or high standards of cleanliness. Once the circuit design is defined, circuits can be mass-produced easily and at low cost. Recent work at the Royal Signals and Radar Establishment, Malvern, U.K. has shown that thick film techniques can be used with success up to frequencies in excess of 16GHz, so it was decided in the present work to use this form of circuit construction.

From the outset, therefore, circuits were fabricated by the standard thick film screening process. After circuit design, a positive mask (10X scale) was drawn and photo-reduced on to the photoresist material coating of 400-mesh stainless steel screens. Fritless inks (palladium - silver for development work - Electroscience 9990, gold for final circuits - Electroscience 8880) in conjunction with alumina substrates (3M Co., type 838 Alsimag). Typical loss for test sections of 50Ω microstrip transmission line was 0.25dB per wavelength at a frequency of 10GHz.

11.1 Overall Circuit Configuration

As mentioned in Section 7.2.2, element designs with a common path for the loop feedback signal and for the received signal can suffer

from phase errors due to mutual coupling between array elements in the transmit mode of operation. The design of Fig. 7.6, with separate RF and IF mixers in transmit and receive channels was therefore chosen to ensure satisfactory operation even in high mutual coupling environments.

To demonstrate higher RF power operation than the several hundred milliwatt level of the modules described in Chapters 9 and 10, it was decided to use a pulsed Gunn diode (Plessey Co. Ltd.) of nominal 10 W RF output power rating (1μs pulse, 0.1 % duty cycle) at 10GHz. With this level of output power, circulator reverse leakage ($\approx$ - 20dB) or antenna mismatch can result in destructive levels of power reaching the receive section mixer. A limiter diode was therefore added before the mixer to limit the maximum mixer input power to lower than + 20dBm.

For ease of integration with the m.i.c. construction the radiating element was chosen to be a conventional microstrip dipole with arms on opposite sides of a small alumina substrate and a balun to match the dipole to 50Ω microstrip line.

In other ways, the module circuit design followed the practice outlined earlier, except that a design frequency of 9.4GHz was chosen, consistent with common military radar frequency allocations.

11.2 Individual Circuit Element Design

This section describes the design and development of the various circuit components. Each component was first built and tested on a separate alumina substrate before the design was transferred to

the complete module.

11.2.1 Gunn Diode Matching Circuit

The optimum matching impedance for the pulsed Gunn diode is not known exactly, but is in the region of 2Ω. The device itself also has capacitive properties associated with the semiconductor chip mounted on a goldplated copper block, or manual. The gold bonding tab from the diode has inductive properties and is designed to resonate with the chip capacitance in the region of the normal operating frequency. Thus, the circuit requirement for optimum device operation is a transformer to present a 2Ω real impedance to the diode when terminated with the standard 50Ω load. The impedance transformation provided by the transformer, together with the bond wire inductance and chip capacitance determine the operating frequency; this frequency may therefore be set by minor mechanical adjustments to the circuit or to the transformer design.

The transformation ratio from 50Ω to 2Ω is large. For broad-band applications, this would be accomplished with a multi-section transformer. In the present case however, bandwidth is not of great importance and the transformation can just be accomplished with a single-stage quarter wave transformer without violating the restriction that the characteristic impedance of the quarter-wave section must not be so low that the microstrip line width can exceed half a guide wavelength.

Using the standard m.i.c. design equations [57], it is found that the quarter-wave section should have characteristic impedance $Z_o = 13\Omega$ which implies a line width to substrate thickness ratio

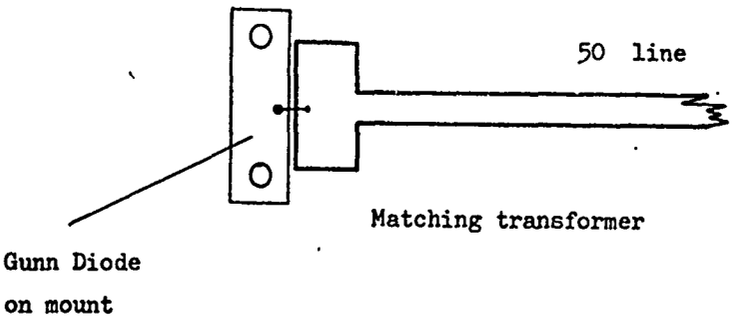


Fig. 11.1 Gunn Diode and Matching Circuit

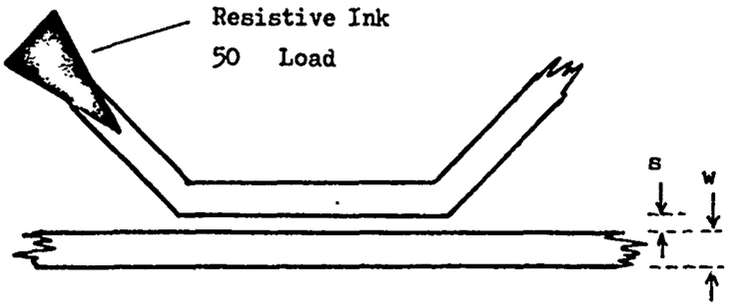


Fig. 11.2 Microstrip Directional Coupler

w/h = 7.92 on alumina. For 0.025 (0.63 mm) thickness alumina, therefore, w = 5.03mm. Compensating the end effect capacitance of the transformer section, the length of the quarter wave line, l_t, becomes ($\sqrt{\varepsilon_{eff}}$ = 2.62, f_o = 9.4GHz) approximately 8.5 mm. A drawing of the transformer is given in Fig. 11.1.

With a quarter-wave transformer of this design in thick film format, positioned so that the low impedance side was at the edge of an alumina substrate and the 50Ω output line terminated in a coaxial matched load at the other side of the substrate, pulsed r.f. output power in the region of 3-5W was obtained. The pulse length was 0.5μs at 2KHz PRF and the diode pulse bias supply was 35V at 3A. In the free-running mode, without phase locked loop control, the frequency chirp was approximately 60MHz, a high value resulting from the low Q-factor of the microstrip oscillator circuit.

11.2.2 Varactor Tuning Circuit

In order to control the free-running frequency of the Gunn diode electronically, as required by the phase locked loop control scheme, it was necessary to couple a varactor to the Gunn oscillator; as in the waveguide cavity oscillators used previously, this alters the load susceptance seen by the Gunn diode and thus changes the output frequency of oscillation. There are several ways of coupling the varactor to the Gunn diode, but a method which allows DC isolation and hence ease of independent biasing of varactor and Gunn is the use of a parallel-line, quarter-wave directional coupler (Fig. 11.2). This follows very standard design procedure[58] which may be implemented using a pocket calculator. The value of coupling required is a function of the tuning range over which the VCO must operate

and a simple theoretical expression for this tuning range has been derived by Hewitt[59].

In the present case, since no frequency agility for the module transmitted output frequency is being considered, the varactor need only tune the Gunn oscillator over a frequency range sufficient to encompass the natural frequency chirp of the oscillator due to diode heating during the pulse and also any drifts in free-running oscillator frequency over the operational temperature range. In view of the 60MHz chirp observed earlier, together with allowance for ambient temperature induced frequency drifts, a minimum frequency tuning range of 100MHz for varactor control is indicated. From the theory of Hewitt, this then implies coupling of the varactor to the Gunn diode with a 10dB coupler. It is worth noting that very little benefit would be obtained by increasing the coupling further as the r.f. power then incident on the varactor is rectified to produce significant DC voltages which reduce the varactor operating range.

For the 10dB coupler on 0.025" alumina substrate, the following design values were used : even-mode impedance, $Z_{oe} = 69.4\Omega$; odd-mode impedance, $Z_{oo} = 36.0\Omega$; $\sqrt{\varepsilon_{eff}} = 2.51$; normalised line separation, $s/h = 0.24$ implying $s = 0.15$ mm ; normalised line width $w/h = 0.82$, implying $w = 0.52$ mm ; quarter wave section length at $f_o = 9.4$ GHz, $l = c/4f_o\sqrt{\varepsilon_{eff}} = 3.14$ mm.

The 50Ω load on the fourth arm of the coupler was provided by a 50Ω tapered restive film, also fabricated in thick film technology with 10Ω/square resistive ink. (Electroscience 3911); such loads presented better than 1.2 VSWR.

11.2.3 Coupler for Loop Signal

The same method of coupler design was used for the coupler to provide a sample of the Gunn oscillator output for the phase locked loop. The coupling value here was chosen as 20dB so that, even with maximum possible output of 10W from a Gunn diode, the signal entering the loop HF mixer would not exceed the 100mW damage level. For this coupler, the design values were : $Z_{oe} = 55.3\Omega$; $Z_{oo} = 45.2\Omega$; $\sqrt{\varepsilon_{eff}} = 2.48$; $s/h = 1.13$, implying $s = 0.72$ mm ; $w/h = 1.06$, implying $w = 0.67$ mm ; $l = 3,18$ mm.

Again, the resistive load on the fourth arm of the coupler was fabricated in thick-film technology. The performance of this coupler, to give a typical test example, independently assessed, is given in Fig. 11.3.

11.2.4. Band-pass Filter

In order to provide d.c. blocking between the Gunn diode and the module output as well as to eliminate any harmonic or spurious signals, a band-pass filter was provided in the output line before the circulator. A maximally-flat response with one element in the low-pass prototype was chosen, the design being for 9.4GHz centre frequency, 10% bandwidth and 50Ω terminating impedances.

Following the treatment of Matthaei[60], the even and odd mode impedances were calculated for the coupled lines and from standard design curves[61], the width and line spacing of the half-wave resonator section was calculated. The design values used were : $s/h = 0.38$, implying $s = 0.24$ mm ; $w/h = 0.82$, implying $w = 0.52$ mm ; $\varepsilon_{eff} = 6.61$; half-wave section length, end corrected, $l = 5.76$ mm. A computer

Fig. 11.3 Microstrip Directional Coupler Performance

Fig. 11.4 Band-pass Filter Performance

program for the design, written in FORTRAN, is given in Appendix 4.

Measurements on a test filter using a 1" x 1" substrate with OSM microwave connectors are shown in Fig. 11.4. At the design frequency the insertion loss is in the region of 1dB, some 0.5dB of which may be accounted for by the connectors.

11.2.5 Circulator

A ferrite circulator was employed to separate transmitted and received signals in the module. The design procedures used were based on the well-known Bosma theory[62], which allows calculation of the circulator dimensions from given ferrite material parameters. A triangular shape has been adopted for the central conductor pattern in order to achieve maximum possible bandwidth. Quarter-wave transformer sections allow matching of the three lines to the low impedance central region.

For under-resonance operation, assuming that only the dominant mode has significant amplitude, the radius of the magnetised ferrite region under the central conductor pattern is given by :

$$R = \frac{1.84\lambda_o}{2\pi\sqrt{\varepsilon_{eff}\,\mu_{eff}}} \qquad \ldots\ldots\ldots 11.1$$

where λ_o is the free space wavelength at the centre band operating frequency f_o

$$\mu_{eff} = \frac{\mu^2 - K^2}{\mu} \qquad \ldots\ldots\ldots 11.2$$

where μ and K are the parameters of the ferrite permeability tensor. Now $\mu = 1$ and $K = -\omega_m/\omega_o$ with $\omega_m = 2\pi\gamma$ (the "$4\pi M_s$" saturation magnetisation) $\gamma = 28$GHz/Tesla (the gyromagnetic ratio) and $\omega_o = 2\pi f_o$.

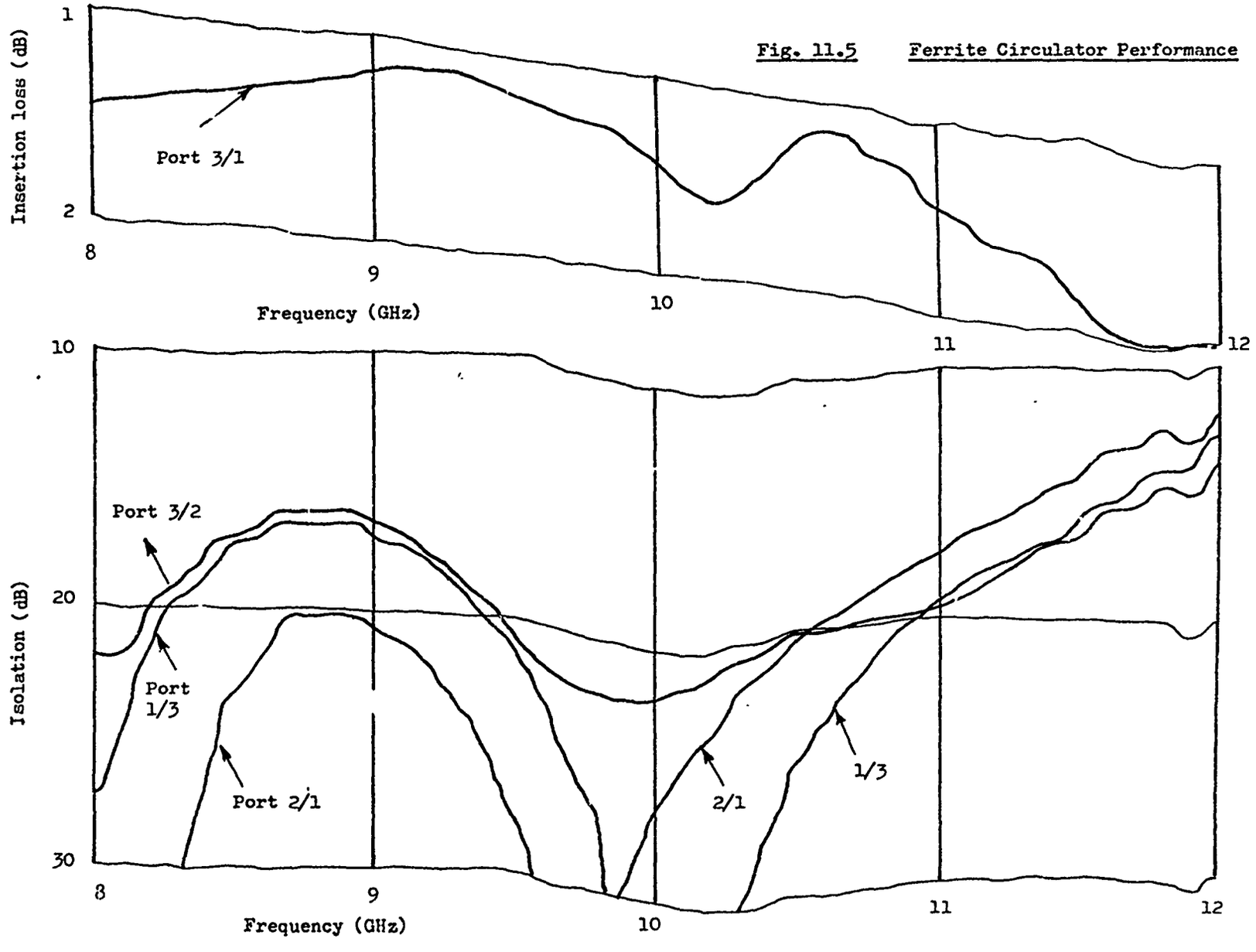


Fig. 11.5 Ferrite Circulator Performance

The ferrite substrate thickness was chosen as 0.025" for compatibility with the alumina substrates and also as a compromise between keeping the microstrip line width as large as possible (w/h constant) and keeping the substrate thin to avoid higher order mode propagation. A Transtech TTI-2500 ferrite with $4\pi M_s$ = 2500 gauss (0.25 Tesla), loss tangent $\tan\delta < 0.00025$ and relative permutivity $\varepsilon_r = 12.9$ was chosen. Quarter wave transformers of line width 0.73 mm and length 3.0 mm provided the matching at each port. The circulator magnet was made from Magnadur 330 material (Mullard Ltd.), magnetised to yield a flux density of approximately 2200 gauss, some 10% less than the saturation value. The full circulator design computer program is given in Appendix 3.

Typical performance characteristics for this circulator design, using a 1" x 1" substrate and mounted in a test jig with OSM connectors, are shown in Fig. 11.5. The insertion loss is just over 1dB, some 0.5dB of which is due to the connectors. The isolation is better than 20dB in the design bandwidth.

11.2.6 Balanced Mixer

A balanced mixer design was chosen to provide good isolation between the signal and the local oscillator inputs as well as to provide suppression of local oscillator a.m. noise. The same design was used for down-conversion in the loop on the transmit side and also for the mixer on the receive side.

The 3dB splitting action required in balanced mixers was provided by a branch line coupler rather than a hybrid ring or rat-race coupler; this latter coupler has non-adjacent output arms, requiring a bridge

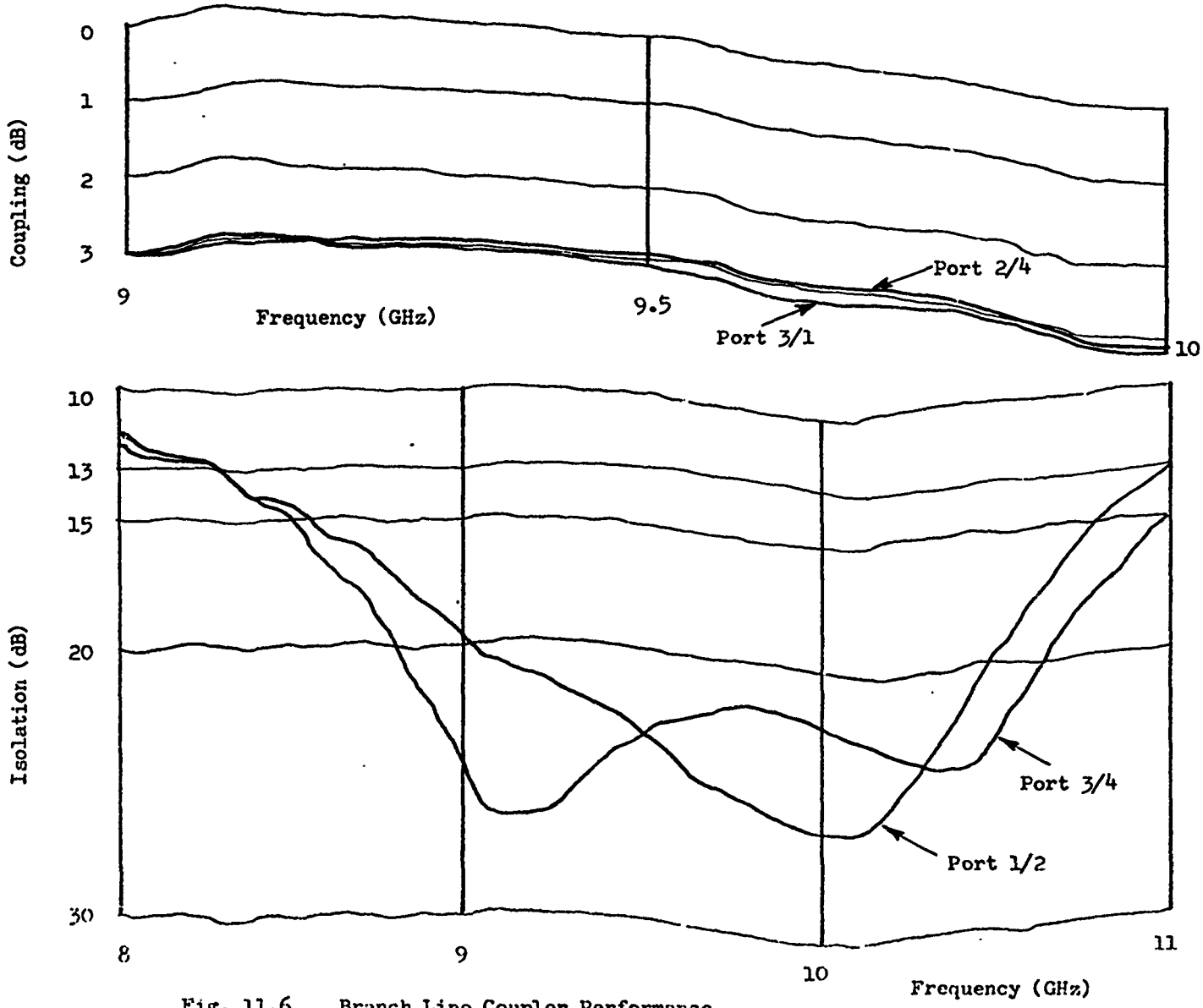


Fig. 11.6 Branch Line Coupler Performance

over one input conductor and this is inconvenient. A standard design[63], taking into account T-junction discontinuity effects was used.

This design of coupler provided a measured power split of very close to 3dB and better than 20dB isolation. Detailed performance curves are shown in Fig. 11.6.

The mixer diodes fed from the output ports of the branch line coupler were GaAs Schottky barrier devices (AEI Type DC 130M), obtained as a matched pair. The noise figure quoted is 6.0dB, the conversion loss 4.5dB, the IF impedance 400Ω, the VSWR 2:1 and the peak burn-out level 400mW. Quarter-wave lines of high impedance from the two coupler RF output ports to ground were provided as a DC return for the diodes.

Low pass filters following the diodes were used to select the 60MHz IF signal and provide good rejection to RF signals. A seven element design was chosen with cut-off at 5GHz. Insertion loss for frequencies below 1GHz was less than 0.5dB, while from 8 to 10GHz the insertion loss was 23dB.

An overall conversion loss of 6dB was obtained for the mixer; the noise figure has not at present been measured.

11.2.7 Dipole Antenna

Though at present separate from the module and connected with an OSM connector, the antenna was constructed also in m.i.c. form on alumina substrate, permitting easy integration with the rest of the module if required.

A 0.025" thick alumina substrate was again used ; quarter wavelength dipole arms were formed, one on each side of the substrate. A balun section performed the matched transition to the imbalanced conventional 50Ω microstrip line and ground plane. A similar form of antenna has been used by Wasse and Denison[64].

11.2.8 Miscellaneous Components

A 3dB power divider to divide the r.f. reference signal between local oscillator ports of the two r.f. mixers was constructed using the design procedure given by Wenzel[65]. It comprises essentially only a quarter-wave transformer section to match one 50Ω line to two parallel 50Ω lines, but some slight correction for the line section discontinuities is necessary.

In order to protect the receive side r.f. mixer from large signals due to antenna mismatch or any form of leakage during the transmit pulse, a Si PIN diode limiter (Alpha type 176-001) was inserted at the junction of the circulator and receiver substrates just before the receive side mixer. This limiter has a quoted insertion loss of 0.1dB with a maximum leakage of 100mW, well below the damage level of the mixers. Protection is provided against input signals of 2W CW or 100W (1μs) pulse.

The remaining microwave circuiting in the module comprised bias lines for the Gunn diode and varactor. These were fabricated using fine (0.001") wire, a quarter wavelength long in air above the substrate. An RF short circuit termination was provided by a 10pF chip capacitor at the end of the wire away from the device.

11.3 Module Layout and Mechanical Construction

The whole module, as shown in the photograph (Fig. 11.7), is assembled in a machined aluminium box. Three substrates are used for convenience of assembly in development work though all the module could be on one substrate if a ferrite insert were provided for the circulator.

The phase locked loop circuitry, exactly as given in Chapters 4 and 9, was assembled on a printed-circuit board mounted in a recess on the underside of the module; this facilitated short connections between the m.i.c. substrates and the loop components without need for external interfaces.

Further development work is proceeding to improve the module output power by means of improved matching of the Gunn diode to the load. The achieved performance at present is as follows :

Output Power	5W, 1μs pulse, 2kHz PRF
Varactor Control Range	70MHz
I.F. Output	120MHz
Loop I.F.	60MHz
I.F. reference frequency	60MHz , + 5dBm
R.F. reference frequency	9.4 GHz, + 5dBm
Loop Settling Time	**100ns**

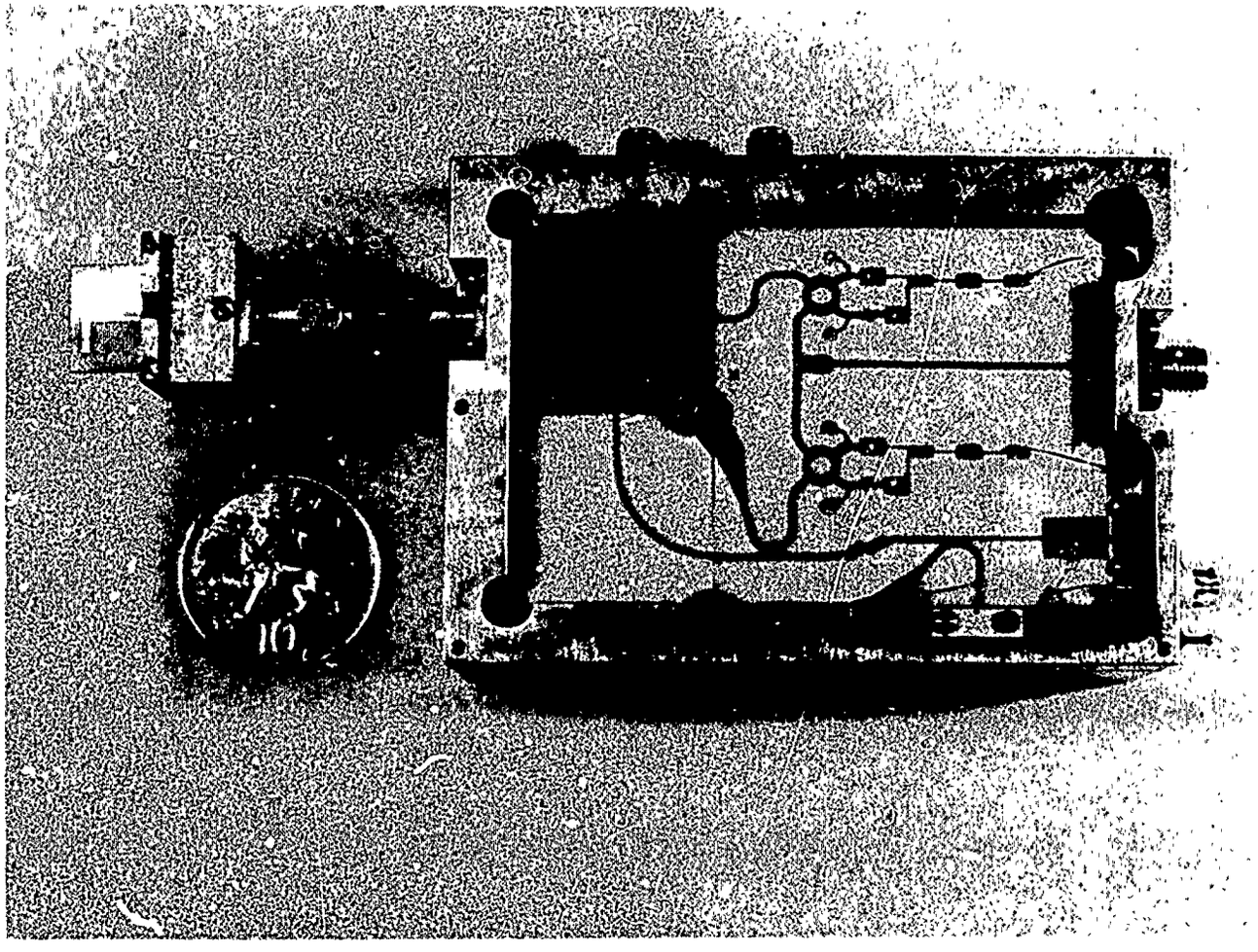


Fig. 11.7 Photograph of the M.I.C. Module

CHAPTER 12

CONCLUSIONS

Conclusions

The review given in Chapter 3 of the powers at present available from microwave solid state devices shows that generation of the power levels typically required for radar can now realistically be achieved with the active array approach, particularly at the lower microwave frequencies. The principal attraction of solid state microwave power generation is its high reliability in relation to that of vacuum tubes, and since both the reliability and the powers available from solid state sources will almost inevitably continue to improve as device technology progresses, it would appear likely that interest in active arrays will continue to grow.

Clearly the obvious approach to the design of active array elements is that based on the use of amplifiers ; however, the cost and complexity associated with the use of multiple stages of gain within the element (often required since typical microwave amplifier gains are $\sim$6dB) and the cost of microwave phase shifting, has proved to be a severe problem. The work described in the preceding chapters has thus concentrated on the investigation of possible approaches based on phase-locked oscillators.

The characteristics of both forms of phase locking, i.e. injection locking and phase-locked loop synchronisation, were examined in Chapter 4. It was concluded that despite the attractive simplicity and high possible locking gain of injection locked sources, the phase error introduced by the locking process would usually limit the locking gain that could be used in practice to a level less than 10dB. The phase-locked loop alternatively was found to offer an attractive combination of properties. It was shown that by the use

of the second order loop transfer function, low phase errors could be achieved in addition to the use of high values of locking gain. furthermore, it was shown that using the heterodyne form of the phase-locked loop the microwave phase shifter usually required for beam-steering could be replaced with an intermediate frequency type.

Following considerations of the influence of the overall array properties on active element design in Chapter 5, possible designs based on injection locking were considered in Chapter 6. It was found however, that due to the restriction on locking gain, little advantage over the use of amplifiers in these designs could be achieved ; microwave phase shifters were still generally required for beam steering.

In Chapter 7, element designs based on the phase-locked loop were considered. A number of possible designs using the heterodyne phase-locked loop were described and two considered to be of particular interest were shown in Figs. 7.6 and 7.12. Since it was recognised that mutual coupling could introduce phase errors in the design of Fig. 7.12 a program to simulate the behaviour of an array of these elements under various mutual coupling conditions was developed. For large arrays the program indicated that the behaviour of the array was fairly insensitive to mutual coupling over a large range of values, however, it remains for further work to determine a guiding value for the maximum mutual coupling level that should exist using this element, when a given sidelobe level is required. It may be noted that the other element design of interest is essentially unaffected by mutual coupling.

Although any IF phase shifter could be used in the elements described

in Chapter 7, a novel digital design based on a harmonically-locked phase-locked loop was described in Chapter 8. The main attractions of this design are the high phase accuracy and the simple control requirements.

In Chapters 9 and 10, the results obtained with four and eight element arrays were presented. The experiments basically demonstrated that beam steering on both transmission and reception may indeed be achieved using only IF phase shifters with the heterodyne loop. Moreover, it was shown that the system lends itself very readily to a simple and direct interface with a TTL based digital beam steering controller or computer.

Finally in Chapter 11, the realisation of the element design in microwave integrated circuit module form with several watts of pulse output power was described; this demonstrates the viability of the design for quantity production as would be required in a large array.

APPENDIX 1

FORTRAN Computer Program to Calculate the Acquisition Phase Transient of a Second Order, Type One Phase-Locked Loop.

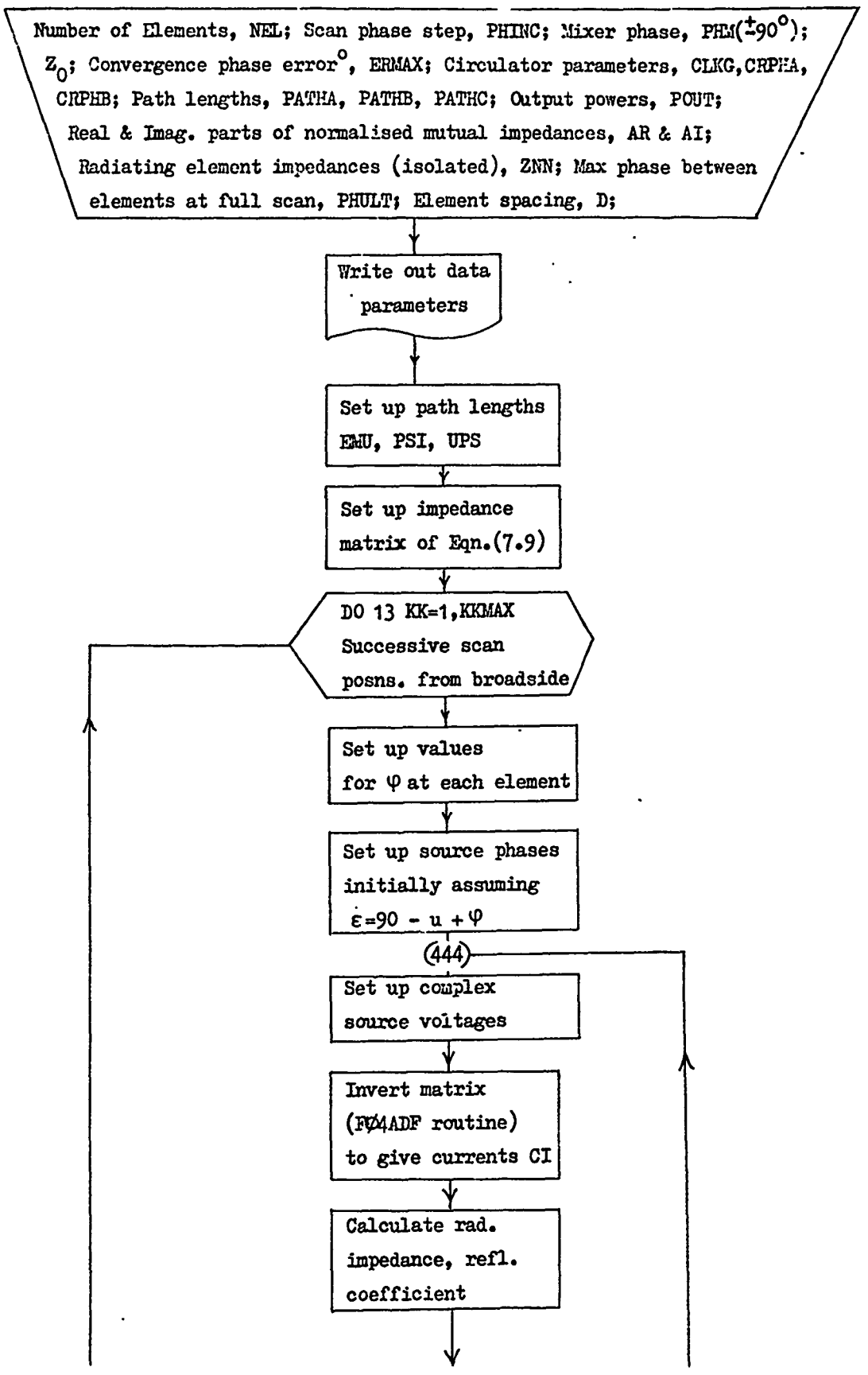
```
C
C                PHASE PLANE ANALYSIS OF A SECOND ORDER TYPE ONE
C                PHASE LOCKED LOOP.        THE INITIAL     RATE OF CHANGE
C                OF PHASE  FOR A GIVEN PHASE IS TAKEN FROM THE FIRST
C                ORDER CASE
C
C
C     THE INPUT VOLTAGE IS SIN,  THE OUTPUT VOLTAGE IS COS
C
      REAL  K
      INTEGER  COUNT,COUNTM
      READ(5,1) AERROF,K,DELPHI,TAUONE,TAUTWO,COUNTM
C   THESE VALUES ARE ENTERED IN RADIAN FORM
    1 FORMAT(2F10.4,F10.4,2F10.4,I1)
      WRITE(6,83)AERROF,K,DELPHI
   83 FORMAT(1H1,10X,'OFFSET RAD FREQ = ',F10.4,5X,'K (LOOP GAIN) = ',
     1E10.4,5X,'PHASE INC (RADS) = ',F15.6,/)
      WRITE (6,87) TAUONE,TAUTWO
   87 FORMAT(1H0,10X,'TAUONE = 'F10.4,10X,'TAUTWO = ',E10.4,/)
      COUNT=0
      J=0
   64 CONTINUE
      READ(5,18)PHITC
   18 FORMAT(F10.4)
      TIME=0.
C SET PHI TO THE INITIAL CONDITION
      PHI=PHITC
    3 COUNT=COUNT+1
      IF(COUNT.GT.COUNTM) GO TO 200
      DO 80 I=1,900
C   USE THE FIRST ORDER LOOP EXPRESSION FOR THE FIRST VALUE OF PHIDOT
      IF(I.EQ.1) PHIDOT=AERROF-(K*SIN(PHI)*(TAUTWO/TAUONE))
C   IF PHIDOT IS POSITIVE, THE PHASE INC MUST BE NEGATIVE AND VICE VERSA
      DPHIS=DELPHI
      IF(PHIDOT.LE.0.) DPHIS=0.-DELPHI
C THE FOLLOWING CARDS DECREASE THE PHASE STEP NEAR PHIDOT=0 TO AVOID ERRORS
      IF((PHIDOT.LT.0.0).AND.(PHIDOT.GT.0.-5.*10.**6)) DPHIS=0.0-DELPHI
     1 /60.
      IF((PHIDOT.GT.0.0).AND.(PHIDOT.LT.5.*10.**6)) DPHIS=DELPHI/60.
C EVALUATE PHIDOT
      R=(AERROF-K*SIN(PHI))/(TAUONE*PHIDOT)
      S=(1.+K*TAUTWO*COS(PHI))/TAUONE
      PHIDOT=R-S
C  CALCULATE THE NEW PHI
      PHI=PHI+DPHIS
C  EVALUATE PHI IN DEGREES
      PHID=(PHI*360.)/(2.*3.142)
CEVALUATE THE NEW PHIDOT
      PHIDOT=PHIDOT+PHIDTF*DPHIS
C  TO SKIP ACROSS ZERO WHEN PHIDOT IS SMALL
      IF((PHIDOT.GT.0.0).AND.(PHIDOT.LT.3.*10.**5)) GO TO 152
      GO TO 153
  152 PHIDOT=0.0-3.*10.**5
      WRITE(6,8)
    8 FORMAT(1H ,10X,'SKIPPED DOWN')
```

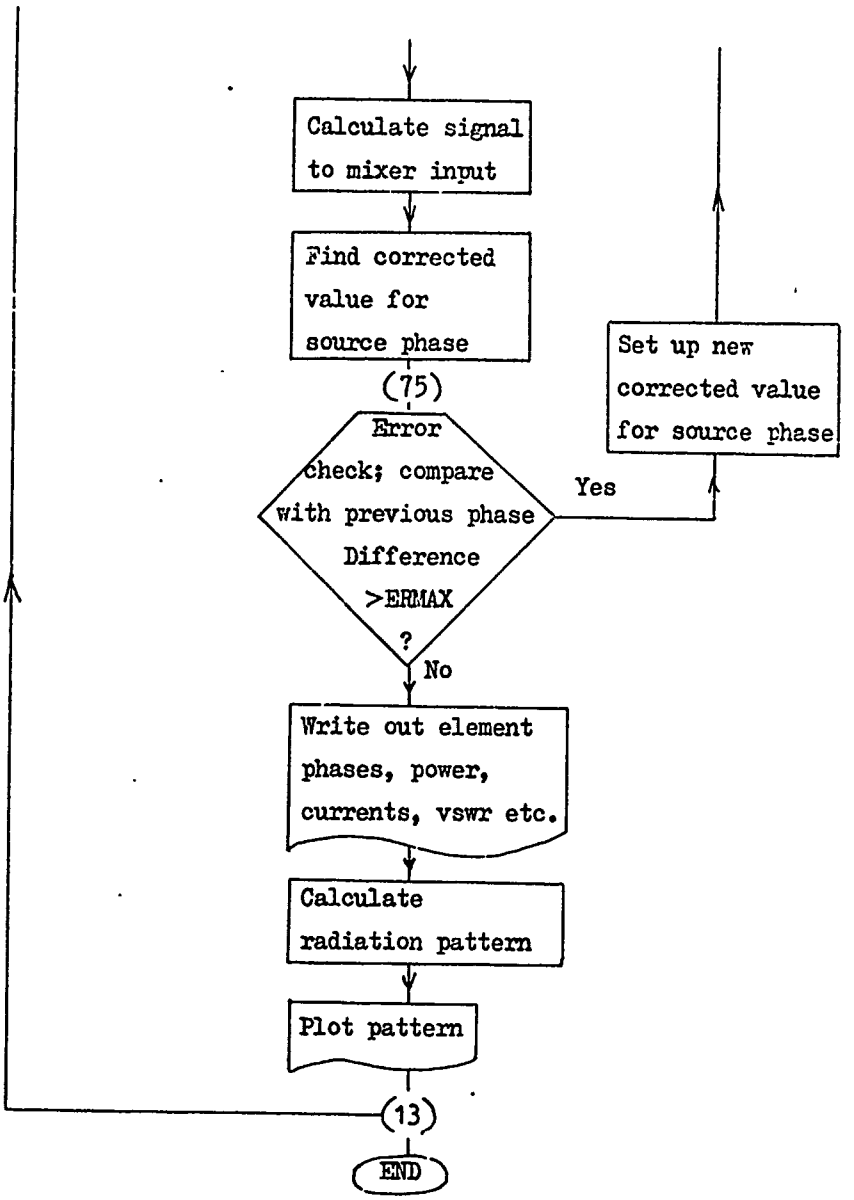
```
      GO TO 79
  153 IF((PHIDOT.LT.0.0).AND.(PHIDOT.GT.0.-3.*10.**5)) GO TO 155
      GO TO 157
  155 PHIDOT=3.*10.**5
      WRITE(6,7)
    7 FORMAT(1H ,10X,'SKIPPED UP')
      GO TO 79
  157 CONTINUE
C  CALCTHE TIME STEP INVOLVED IN THE EVALUATUION OF THE NEW PHIDOT
      DELTIM=ABS(DPHIS)/ABS(PHIDOT)
      TIME=TIME+DELTIM
      A=SIN(PHI)
      IF(I.EQ.1) GO TO 28
      J=J+1
      IF(J.EQ.3) GO TO 73
      GO TO 79
   73 J=0
      GO TO 33
   28 WRITE(6,12)
   12 FORMAT(1H1,10X,'TIME',15X,'PHI IN DEGREES',10X,'PHIDOT',20X,
     R'SIN(PHI)',10X,'PHIDIF',10X,'I',/)
   33 WRITE(6,13) TIME,PHID,PHIDOT,A ,PHIDIF,I
   13 FORMAT(1H ,10X,E12.4,10X,F10.4,10X,E12.4,10X,F10.4,10X,E12.4,
     R6X,I4)
   79 CONTINUE
   80 CONTINUE
      GO TO 64
  200 CONTINUE
      STOP
      END
```

APPENDIX 2

FORTRAN Computer Program to Calculate the Radiation Pattern, Including the Effects of Mutual Coupling, for an Array Using the Element Designs of Section 7.2.2.

Flow Chart


Number of Elements, NEL; Scan phase step, PHINC; Mixer phase, PHM(±90°); Z_0; Convergence phase error°, ERMAX; Circulator parameters, CLKG, CRPHA, CRPHB; Path lengths, PATHA, PATHB, PATHC; Output powers, POUT; Real & Imag. parts of normalised mutual impedances, AR & AI; Radiating element impedances (isolated), ZNN; Max phase between elements at full scan, PHULT; Element spacing, D;
Write out data parameters
Set up path lengths EMU, PSI, UPS
Set up impedance matrix of Eqn.(7.9)
DO 13 KK=1,KKMAX Successive scan posns. from broadside
Set up values for φ at each element
Set up source phases initially assuming ε=90 - u + φ
(444)
Set up complex source voltages
Invert matrix (F04ADF routine) to give currents CI
Calculate rad. impedance, refl. coefficient


Calculate signal to mixer input
Find corrected value for source phase
(75)
Error check; compare with previous phase Difference >ERMAX ?
Yes
Set up new corrected value for source phase
No
Write out element phases, power, currents, vswr etc.
Calculate radiation pattern
Plot pattern
(13)
END

```
      REAL*8 ARSP
      COMPLEX CMPLX,CIS,RHO,ARHO,ZRAD,ZNS,VT,VAC,VBC,VM,ZOC
      COMPLEX ZIN,ZC,ZD,V,VL,CI,ZOD,EOPS,EPSI,ELMD,ZC,ZA,VA,VB,ZMN
      DIMENSION CI(4,1),V(4,1),VB(4,1),Z(4,4),VA(4,1),VC(4,1)
     1 ,ZC(4,4),ZA(4,4),ZB(4,4),REF(4),POUT(4),CIPH(4)
     2 ,AR(5),AI(5),ARSP(4),CIS(4),PHI(4),ZRAD(4),RHO(4),VSWR(4)
     3 ,ZIN(4),ZNS(4),EPS(4),VT(4),VM(4),VAC(4),VBC(4)
     4 ,THETA(541),PEL(541),A(10,541,2),IXAX(5),IYAX(5),IZAX(5)
     5 ,CIMOD(4)
      DATA IXAX/'ANGL','E (D','EGRE','ES) ','    '/
      DATA IYAX/'POWE','R IN',' DB ','    ','    '/
      DATA IZAX/'    ','    ','    ','    ','    '/
      WRITE(6,111)
  111 FORMAT(1H0,'PHASE LOCKED LOOP TRANSMITTING ELEMENT ARRAY PROGRAM'
     1 ,/,' ANALYSIS OF MUTUAL COUPLING EFFECTS')
      CALL PLOTS(300)
      NEL=4
      NELM=NEL-1
      WRITE(6,112) NEL
  112 FORMAT(1H0,'NUMBER OF ELEMENTS',I3)
      D=0.45
      WRITE(6,113) D
  113 FORMAT(1H ,'ELEMENT SPACING',F6.2,' WAVELENGTHS')
      PHINC=45.0
      PHULT=135.0
      KKMAX=PHULT/PHINC+1.5
      PI=3.14159
      PHM=90.
      RADDG=PI/180.
      ZO=50.
      ERMAX=5.0
      WRITE(6,114) ERMAX
  114 FORMAT(1H ,'MAXIMUM PHASE ERROR IN CONVERGED SOLUTION= ',F3.1,
     1 ' DEGREES')
      ELERR=3.0
      ZOC=CMPLX(ZO,0.0)
      ZOD=ZOC
C ATDB IS THE VALUE OF ANY ATTENUATOR (IN DB) INSERTED BETWEEN
C CIRCULATOR AND ANTENNA ELEMENT TO REDUCE MUTUAL COUPLING EFFECTS IN
C SINGLE MIXER DESIGN
      ATDB=-10.0
      ATT=10.0**(ATDB/20.0)
      READ(5,100) CLKG,CKPHA,CKPHB,PATHA,PATHB,PATHC
  100 FORMAT(6F10.4)
      WRITE(6,99) CLKG,CKPHA,CKPHB,PATHA,PATHB,PATHC
   99 FORMAT(1H0,'CIRCULATOR LEAKAGE(DB)=',F6.1,/,' CIRCULATOR INSERTION
     2 PHASE BETWEEN ADJACENT PORTS,FORWARD(DEG)=',F6.1,/,' CIRCULATOR I
     3NSERTION PHASE BETWEEN ADJACENT PORTS,REVERSE(DEG)=',F6.1,/,' ELEC
     4TRICAL PATH FROM OSCILLATOR TO CIRCULATOR(DEG)=',F6.1,/,' ELECTRIC
     5AL PATH FROM CIRCULATOR TO ANTENNA(DEG)=',F6.1,/,' ELECTRICAL PATH
     6 FROM CIRCULATOR TO MIXER(DEG)=',F6.1)
      READ(5,101) PLOT
      READ(5,101) AR
      READ(5,101) AI
```

```
  101 FORMAT(6F10.4)
      READ(5,110) ZIN
  110 FORMAT(2D10.4)
      WRITE(6,119)
  119 FORMAT(1H ,'ELEMENT NUMBER',10X,'IMPEDANCE',12X,'REFLECTION COEFFI
     1CIENT',7X,'VSWR',/,17X,'REAL PART',5X,'IMAG PART',5X,'REAL PART',
     2 5X,'IMAG PART')
      DO 30 I=1,NEL
      ZNS(I)=ZIN(I)
      ZNSR=REAL(ZNS(I))
      ZNSI=AIMAG(ZNS(I))
      ARHO=(ZNS(I)-Z00)/(ZNS(I)+Z00)
      RHOR=REAL(ARHO)
      RHOI=AIMAG(ARHO)
      RHOM=SQRT(RHOR**2+RHOI**2)
      SWR=(1+RHOM)/(1-RHOM)
      WRITE(6,120) I,ZNSR,ZNSI,ARHO,SWR
   30 CONTINUE
  120 FORMAT(7X,I3,7X,F10.4,3X,F10.4,4X,F10.4,4X,F10.4,5X,F6.4)
      WRITE(6,121) PHM
  121 FORMAT(2H0,'SIGNAL INPUT TO MIXER LAGS REFERENCE INPUT BY ',F6.1,
     2 ' DEGREES FOR ZERO D.C. OUTPUT')
      F=10.**(CL*6/20.)
      WRITE(6,103)
      DO 10 I=1,NELM
      WRITE(6,102) AR(I),AI(I)
   10 CONTINUE
  103 FORMAT(2H0,'MUTUAL IMPEDANCE DATA VALUES')
  102 FORMAT(1H ,'REAL PART=',F7.3,5X,'IMAGINARY PART=',F7.3)
C SET UP IMPEDANCE MATRIX
      DO 20 J=1,NELM
      DO 25 K=1,NELM
      L=J+K
      IF(L.GT.NEL) GO TO 25
      AR2=AR(K)*ZO
      AI2=AI(K)*ZO
      Z(J,L)=CMPLX(AR2,AI2)
      Z(L,J)=Z(J,L)
   25 CONTINUE
      Z(J,J)=Z00+ZIN(J)
   20 CONTINUE
      Z(NEL,NEL)=Z00+ZIN(NEL)
C IMPEDANCE MATRIX SET UP
C SET UP THE PLOT PARAMETERS
      NP=361
      DO 62 J=1,NP
      THETA(J)=(-90.+FLOAT(J-1)*180./FLOAT(NP))*RADDG
C ELEMENT PATTERN ACCORDING TO SILVER
      AA=1.+0.707*COS(THETA(J))
      UUPS=0.5*PI*SIN(THETA(J))
      IF(J.EQ.(NP/2+1)) GO TO 63
      PEL(J)=(AA*SIN(UUPS)/UUPS)**2
      GO TO 62
   63 PEL(J)=AA**2
```

```
   32 CONTINUE
C SET UP ELECTRICAL LENGTHS
   75 PHD=PATHA+PATHB+CLPHA
      PSI=PATHC+PATHD+CLPHA
      DPS=PATHA+PATHC+CLPHB
      DPSR=DPS*RADCO
      PSIR=PSI*RADCO
      ENDR=END*RADCO
      CD=COS(DPSR)
      CP=COS(PSIR)
      SI=-SIN(DPSR)
      SJ=-SIN(PSIR)
      CE=COS(ENDR)
      SE=-SIN(ENDR)
      EDPS=CMPLX(CD,SI)
      EPSI=CMPLX(CP,SJ)
      EEND=CMPLX(CE,SE)
      PARN=1.E-6
      DO 15 KK=1,NRMAX
      JK=0
      DO 14 I=1,NEL
C SET UP COMPLEX VOLTAGE SOURCES
      PHI(I)=PHINC*FLOAT((KK-1)*(I-1))
      EPS(I)=PHM+PHI(I)-DPS
   14 CONTINUE
  444 DO 17 I=1,NEL
      EPS(I)=PRINV(EPS(I))
      ED=2.*SQRT(POUT(I)*ZO)
      ER=ED*COS(EPS(I)*RADCO)
      EI=-ED*SIN(EPS(I)*RADCO)
      VTR=ER/2.
      VTI=EI/2.
      VT(I)=CMPLX(VTR,VTI)
      V(I,1)=CMPLX(ER,EI)*EEND
C THIS IS THE SOURCE VOLTAGE REFERRED TO THE APERTURE NOW
   17 CONTINUE
C TRANSFER VALUES OF Z AND V TO WORKING ARRAYS
      DO 23 J=1,NEL
      XEF(J)=EPS(J)
      VB(J,1)=V(J,1)
      DO 24 K=1,NEL
      ZB(J,K)=Z(J,K)
   24 CONTINUE
   23 CONTINUE
      IND=0
C INVERT MATRIX TO GIVE CURRENTS
      CALL FO44DF(ZB,NEL,VB,NEL,NEL,1,CI,NEL,WKSP,II)
      JK=JK+1
      IF(II.NE.0) WRITE(6,105) II
  105 FORMAT(1H0,'UNSUCCESSFUL MATRIX INVERSION CODE IS 0; CODE IS ',I2)
      DO 22 J=1,NEL
      ERADT(J)=REAL(VI(J,1))/CI(J,1)-ZO
      XR(J)=(ERADT(J)-ZO)/(ERADT(J)+ZO)
      RORGO=CABS(XR(J))
```

```
      VSWR(J)=(1+ROMOD)/(1-ROMOD)
   21 CONTINUE
C EVALUATE RESULTANT COUPLED SIGNAL
      DO 12 I=1,NEL
      VAC(I)=VT(I)*EDPS**F
      VACR=REAL(VAC(I))
      VACI=AIMAG(VAC(I))
      VACPH=TANSP(VACR,VACI)
      VBC(I)=VT(I)*ELENG*RHO(I)*EPSI-ATT**2
      VBCR=REAL(VBC(I))
      VBCI=AIMAG(VBC(I))
      VBCPH=TANSP(VBCR,VBCI)
      WRITE(6,123) VACPH,VBCPH
      IF(I.EQ.(NEL/2).AND.KK.EQ.1) GO TO 75
      GO TO 74
   75 ADJ=VACPH-VBCPH
C THIS ADJUSTS THE ELEMENT LENGTH IN BROADSIDE POSITION FOR INTERPOLAT-
C ION LOCKING EFFECT
   72 PATHB=PATHB-ADJ/2.
   74 CONTINUE
   12 CONTINUE
      IF(ABS(ADJ).GT.ELERR) GO TO 73
  123 FORMAT(1H ,E12.4,5X,E12.4)
      DO 77 I=1,NEL
      VM(I)=VAC(I)+VBC(I)
      VMR=REAL(VM(I))
      VMI=AIMAG(VM(I))
      WRITE(6,125) EPS(I)
      EPS(I)=EPS(I)+PHI(I)+PHM+TANSP(VMR,VMI)
      EPS(I)=PRINV(EPS(I))
  125 FORMAT(1H ,E12.4)
      WRITE(6,125) EPS(I)
      ERR=ABS(EPS(I)-REF(I))
      IF(ERR.GT.ERMAX) IND=1
   77 CONTINUE
      IF(IND.EQ.1.AND.KK.NE.1) GO TO 444
      DO 80 J=1,NEL
      EPSN=-EPS(J)
      WRITE(6,115) J,RHO(J),VSWR(J),POUT(J),EPSN
  115 FORMAT(1H ,'ELEMENT NUMBER',I2,'  REFLECTION COEFFICIENT',E12.5,3X
     2,E12.5,'  VSWR',E12.5,3X,'SOURCE POWER ',E10.3,3X,'PHASE ',F6.1)
   80 CONTINUE
      DO 81 J=1,NEL
      WRITE(6,105) J,VAC(J),VBC(J)
  105 FORMAT(1H ,'ELEMENT NUMBER ',I3,' LEAKAGE SIGNAL ',E12.5,3X,
     1 E12.5,' REFLECTED SIGNAL ',E12.5,3X,E12.5)
   81 CONTINUE
      WRITE(6,110)
      DO 15 L=1,NEL
      CIS(L)=CI(L,1)
      CISR=REAL(CIS(L))
      CISI=AIMAG(CIS(L))
      CIPH(L)=TANSP(CISR,CISI)
      VMR=REAL(VM(L))
```

```
      VMI=AIMAG(VM(L))
      VMMOD=SQRT(VMR**2+VMI**2)
      VMPH=ATAN2(VMI,VMR)
      CIMOD(L)=SQRT(CISR**2+CISI**2)
      PHII=PHASV(VI-PHI(L))
      CERR=PHASV(PHII-CIPH(L)+CIPH(1))
      WRITE(6,107) L,PHII,CIMOD(L),CIPH(L),CERR,VM(L),VMMOD,VMPH
   15 CONTINUE
  107 FORMAT(2X,I2,9X,F6.1,9X,E10.3,8X,F6.1,9X,F6.1,6X,E10.3,3X,F10.3,
     * 5X,E10.3,5X,F6.1)
  110 FORMAT(1H0,'EL. NUM',5X,'REF PHASE',5X,'EL. CURRENT MODULUS',6X,'P
     1HASE',5X,'CURRENT ERROR',9X,'COMPLEX COUPLED VOLTAGE',7X,'MODULUS'
     2,6X,'PHASE')
C CALCULATE THE RADIATION PATTERN
      DO 84 J=1,NP
      RP=0.0
      AIP=0.0
      DO 85 I=1,NEL
      APSI=2.*PI*D*SIN(THETA(J))*FLOAT(I)
      APHI=APSI+CIPH(I)*RADCO
      RP=RP+CIMOD(I)*COS(APHI)
      AIP=AIP+CIMOD(I)*SIN(APHI)
   85 CONTINUE
      A(KK,J,2)=(RP**2+AIP**2)*PEL(J)
      IF(KK.GT.1) GO TO 84
      IF(A(KK,J,2).GT.PARN) PARN=A(KK,J,2)
C THIS SETS A NORMALISATION FACTOR WITH BROADSIDE BEAM MAXIMUM AS REFERENCE
   84 CONTINUE
      NNT=0
      DO 86 J=1,NP
      NNT=NNT+1
      A(KK,J,2)=10.*ALOG10(A(KK,J,2)/PARN)
      A(KK,J,1)=THETA(J)/RADCO
      IF(NNT.NE.10) GO TO 87
      WRITE(6,124) A(KK,J,1),A(KK,J,2)
  124 FORMAT(1H ,E10.5,5X,E12.5)
      NNT=0
   87 CONTINUE
   86 CONTINUE
   13 CONTINUE
C NOW CALL THE PLOT ROUTINE
      CALL PLTSU(NP,NKKAA,5.,5.,2.,15.,0.,-90.,7.5,1AAX,20,-30.,1.,
     1 1YAX,-20,12AX,20,0.5)
      CALL PLOT(0.0,0.0,2000)
      STOP
      END
```

```
      SUBROUTINE PLT3D(A,N,NC,XO,YO,XP,YP,THET,XS,XINC,IXAX,NCX,YS,
     1 YINC,IYAX,NCY,IZAX,NCZ,ZOFF)
      DIMENSION A(10,N,2),IXAX(5),IYAX(5),IZAX(5),B(541,2)
C FORREST'S FANCY PHILOMORPH
      RADCO=3.14159/180.
C WORK OUT Z-AXIS PARAMETERS
      CS=COS(THET*RADCO)
      SS=SIN(THET*RADCO)
      ZL=20.
      XSP=XP/FLOAT(N-1)
      L=ZOFF*CS/XSP
      XSC=1./XINC
      YSC=1./YINC
      XSS=XS
      YSS=YS
      DO 9001 I=1,NC
C SET UP ORIGIN
      IF(I.EQ.1) CALL PLOT(XO,YO,-3)
C DRAW X-AXIS AND TITLE
      CALL AXIS(0.,0.,XP,0.,XS,XINC,IXAX,NCX)
      CALL PLOT(0.,0.,3)
C DRAW Y-AXIS AND TITLE
      CALL AXIS(0.,0.,YP,90.,YS,YINC,IYAX,NCY)
      CALL PLOT(0.,0.,3)
      DO 9010 K=1,N
      B(K,2)=0.0
 9010 CONTINUE
      DO 9008 J=1,N
      IF(A(I,J,2).LT.YSS) A(I,J,2)=YSS
      X=(A(I,J,1)-XSS)*XSC
      Y=(A(I,J,2)-YSS)*YSC
      B(J,1)=X
      NL=J+L
 9006 CALL PLOT(X,Y,2)
      B(J,2)=Y
 9007 CONTINUE
 9008 CONTINUE
      CALL PLOT(0.,0.,3)
      CALL PLOT(0.0,0.0,999)
 9001 CONTINUE
      RETURN
      END
```

```
      FUNCTION PRINV(X)
      XX=X
      IF(ABS(XX).LE.360.0) GO TO 3001
      N=XX/360.
      XX=XX-FLOAT(N)*360.
3001  IF(XX.GT.180.) XX=XX-360.
      IF(XX.LT.-180.) XX=360.+XX
      PRINV=XX
      RETURN
      END
```

```
      FUNCTION TANSP(BR,BIM)
      IF(BR.EQ.0.0.AND.BIM.GT.0.0) GO TO 4001
      IF(BR.EQ.0.0.AND.BIM.LT.0.0) GO TO 4002
      A=ATAN(BIM/BR)*180./3.14159
      IF(BIM.GT.0.0.AND.BR.LT.0.0) A=A+180.
      IF(BIM.LT.0.0.AND.BR.LT.0.0) A=A-180.
      GO TO 4003
4001  A=90.
      GO TO 4003
4002  A=-90.
4003  TANSP=A
      RETURN
      END
```

APPENDIX 3

FORTRAN COMPUTER PROGRAM FOR CIRCULATOR DESIGN

```
      READ(2,11) F1,F2
   11 FORMAT(2F8.2)
      READ(2,12) MS,IE
   12 FORMAT(2F8.2)
      F0 = (F1 + F2)/ 2.
      FM = 2.8 * MS
      IF (FM - F1) 1,2,2
    2 WRITE(3,13)
   13 FORMAT(1H ,' UNUSEFUL MATERIAL, TAKE SMALLER MS')
      GO TO 9
    1 IF (F2 - 4100.) 3,3,4
    3 H = 1.5
      GO TO 5
    4 H = 0.365
    5 D1 = 0.172 * 3. * 10. ** 5./(F0 + 0.5)
      W  = 0.94 * H
      E = 3.12
      XL = 3. * 10. ** 5./(F0 * 4. * E)
      D2 = D1 + W * SQRT(3.)
      D3 = 2. * XL + D1
      WRITE(3,14) D1,D2, D3,W,XL,H
   14 FORMAT(6F8.3)
    9 STOP
      END
```

APPENDIX 4

FORTRAN COMPUTER PROGRAM FOR INTERDIGITAL FILTERS

1ST PART - EVEN AND ODD-MODE IMPEDANCES

```
C       DESIGN OF AN INTERDIGITAL BAND-PASS FILTER IN MICROSTRIP LINE
        REAL J
        DIMENSION A(10),G(20),J(20),Z1(20),Z2(20)
        INTEGER P
        AL = 0.1 , BPR = (F2-F1)/F0
        N = 1
        F1 = 9.025
        F2 = 9.975
        F0 = (F1 + F2)/2.
        PI = 3.1416
C       COMPUTING THE 'G' PARAMETERS FOR THE PROTOTYPE
        L = K - 1
        T = AL/17.37
        Q = EXP(T)
        U1 =A LOG((Q + 1./Q)/(Q - 1./Q))
        T = U1/(2. * N)
        Q = EXP(T)
        U2 = (Q - 1./Q)/2.
        A(1) = SIN(PI/(2. * N))
        G(1) = 2. * A(1)/U2
        K = 0
        DO 1 K = 2,N
        A(K) = SIN((2. * K-1.) * PI/(2. * N))
        L = K - 1
        B = U2 ** 2. + (SIN(L * PI/N)) **2.
        G(K) = 4. * A(K) * A(L)/(B * G(L))
      1 CONTINUE
        AN = FLOAT(N)
        LI = IFIX(AN/2.)
        F = AN/(2. * FLOAT(LI))
        M = N + 1
        IF (F - 1) 2,2,3
      3 G(M) = 1.
        GO TO 10.
      2 T = U1/4.
        Q = EXP(T)
```

```
      G(N) = ((Q + 1./Q)/(Q - 1./Q)) **2.
   10 DO 11  K = 1,M
      Y0 = 0.02
   11 CONTINUE
C     CALCULATING THE IMPEDANCES
      G(0) = 1.
      J(0) = SQRT(PI * BPR/ (2. * G(0) * G(1)))
      J(N) = SQRT(PI * BPR/ (2. * G(N) * G(M)))
      P = N - 1
      DO 4 I = 1,P
      L = I + 1
      J(I) = PI * BPR/(2 * SQRT(G(I) * G(L)))
    4 CONTINUE
      DO 5 I = 0,N
      Z1(I) = (1 + J(I) + J(I) **2.)/Y0
      Z2(I) = (1 - J(I) + J(I) ** 2.)/Y0
      WRITE(6,30) J,Z1(I),I,Z2(I)
    5 CONTINUE
   30 FORMAT(2X,'ZOE',I2,'=',F9.4,2X,'OHMS',14X,'ZOO',I2,'=',F9.4,2X,'OHMS')
      WRITE(6,31)
   31 FORMAT(2X,'INTRODUCE NEW DATA')
      STOP
      END
```

2ND PART - PHYSICAL DIMENSIONS

```
      ER = 9.8
      H = 0.635
      FO = 9.5
      WH =
      SH =
      W = WH * H
      S = SH * H
      XLO = 299.776/ FO
      EP = 5.3 + 4.3/SQRT(1. + 10. * H/W)
      BO = 0.0645 * ALOG(100. * W/H)
```

```
      XLR = XL0/(4. * SQRT(EP)) - B0 * H
      WRITE(3,36) I,XLR,W
   36 FORMAT(2X,'LENGTH AND WIDTH(MM) OF',I2,'RESONATOR:',2F9.4)
      WRITE(6,37) I,S
   37 FORMAT(I2,5X,'SPACING(MM)',3X,F9.2)
      STOP
      END
```

REFERENCES

1. Brookner, E. (Ed) — Radar Technology. Artech House, 1977.

2. Stark, L. — Microwave Theory of Phased-Array Antennas - A Review. Proc. I.E.E.E., Vol. 62, No. 12, Dec. 1974.

3. Milne, K. — Principles and Concepts of Multistatic Surveillance Radars. Intl. Conf. 'Radar '77'. I.E.E. Conf. Publ. 155.

4. Croney, J. — Doubly Dispersive Frequency Scanning Antenna (for Two Plane Scanning). Microwave Journal, July 1963.

5. Steinberg, B.D. — Principles of Aperture and Array System Design. J.Wiley, 1976.

6. Colin and Zucker (Eds) — Antenna Theory (Parts 1 and 2) . McGraw Hill, 1969.

7. Brown, J. and Beltcher, W.R. — The Reduction of Grating Lobes in Phased Arrays. Intl. Conf. 'Radar Present and Future' Oct.'73, I.E.E. Conf. Publ.No. 105.

8. Cheng, D.K. and Goto, N. — Phase-Shifter Thinning and Sidelobe Reduction for Large Phased Arrays. I.E.E.E. Transactions, Vol. AP-24, No. 2, March 1976.

9. Skolnik, M.I. (Ed) — Radar Handbook, McGraw Hill, 1970.

10. Burgess, J.S. — Recent Advances in Radar Technology. Intl. Conf. 'Radar '77'. I.E.E. Conf. Publ. 155.

11. Hoft, D.J. — Devices and Techniques for all Solid State Radars. Eascon '76 Record, Sept. 1976.

12. Forrest, J.R. Darbandi, A. and Cullen, A.L. — Interpolation Locking : A New Technique For Active Array Antennas. I.E.E. Journal, Electronic Circuits and Systems, Vol. 1, No. 1, Sept. 1976

13. Cullen, A.L. — New Technique for Digital Phase-Shift Control. Electronic Letters, Vol.5, No. 7, April 1969.

14. Al-Ani, A.H., Cullen, A.L. and Forrest, J.R. — A Phase-Locking Method for Beam Steering in Active Array Antennas. I.E.E.E. Transactions. MTT-22, June 1974.

15. White, J.F. — Diode Phase Shifters for Array Antennas. I.E.E.E. Transactions, MTT. 22, No. 6 June 1974.

16. Burns, R.W. and Stark, L. — PIN Diodes Advance High-Power Phase Shifting. Microwaves, Vol. 11, pp.38-48, 1965

17. Lewis, E.T. — Monolithic Realizations of Lumped Element Matching Networks and a Lumped Element Phase Shifter with FET Switching. Raytheon Company Report.

18. Forrest, J.R. and Austin, J. — Report on Technical Visit to the U.S.A. U.C.L. Internal Memorandum, Jan. 1978.

19. Forrest, J.R. and Austin, J. — Technology Assessment of Microwave Semiconductor Devices. January 1978. Survey carried out under Grant No. AFOSR-77-3444 for the U.S. AirForce Office of Scientific Research.

20. Carrol, J.E. — Hot Electron Microwave Generators. Arnold, 1970.

21. Cohen, E.D. — Trapatts and Impatts - State of the Art and Applications. Microwave Journal, February 1977.

22. Pitzalis, O. Jnr. — Status of Power Transistors - Bipolar and Field Effect. Microwave Journal, February 1977.

23. Newton, B.H. — A Tuneable S-Band Trapatt Oscillator - Preliminary Results. Paper presented at I.E.E. Colloquium on Microwave Tuneable Oscillators, November 1977.

24. Rees, H.D. and Gray, K.W. — Indium Phosphide : a Semiconductor for Microwave Devices. I.E.E. Journal SSED, 1, 1-8, September 1976.

25. Irving, L.D., Pattison, J.E., Braddock, P.W. and Gray, K.W. — Improved Mean Power and Long Pulse Width Operation of InP TEOs in J Band. Electronic Letters.

26. Lindop, R.W. — A Fast Fourier Transform Processor Using Shift Registers. Mullard Research Laboratories Annual Review, 1975.

27. Nergaard, L.S. — Tubes and/or Solid State Devices for Power Generation. Microwave Journal, April 1970.

28. Kurokawa, K. — Injection Locking of Microwave Solid State Oscillators. Proc. I.E.E.E., Vol. 61, No. 10, Oct.1973

29. Al-Ani, A.H. — A Beam Steered Active Array Using a Harmonic-Locking Phase Shift Technique. PhD. Thesis Univ. of London, 1973.

30. Darbandi, A. — An Interpolation Locking Technique for Steerable Active Phased Array Antennas. PhD. Thesis, Univ. of London 1976.

31. White, T.M. and Jones, W.B. — Frequency Transients in Synchronized Oscillators. I.E.E.E. Trans. on Circuit Theory, June, 1964.

32. Takayama, Y. — Dynamic Behaviour of Nonlinear Power Amplifiers in Stable and Injection-Locked Modes. I.E.E.E. Trans., MTT-20, No. 9, Sept. 1972.

33. Mackey, R.C. — Injection Locking of Klystron Oscillators. IRE Trans. Microwave Theory and Techniques, July, 1962.

34. Hines, M.E., Collinet, J.C. and Ondria, J.G. — FM Noise Suppression of an Injection Phase-Locked Oscillator. I.E.E.E. Trans. MTT-16 , Sept., 1968.

35. Kurokawa, K. — Noise in Synchronized Oscillators. I.E.E.E. Trans. MTT-16, April 1968.

36. — Microwave Power Generation and Amplification Using Impatt Diodes. Hewlett Packard Application Note 935.

37. Ulbricht, J. and Marx, B. — Stabilization of a Phase Shifting Injection Locked Oscillator Module for Phased Array Application. ntz. Bd. 30 (1977) Heft 7.

38. Kroupa, V.F. — Frequency Synthesis Theory, Design and Applications. Griffin, 1973.

39. Blanchard, A. — Phase Locked Techniques - Application to Coherent Receiver Design. J.Wiley and Sons, 1976.

40. Klapper and Frankle — Phase-Locked and Frequency Feedback Systems. Academic Press, 1972.

41. Viterbi, A.J. — Acquisition and Tracking Behaviour of Phase-Locked Loops. Jet Propulsion Labs. External Public. No.673, July, 1959

42. Gardner, F.M. — Phaselock Techniques. J.Wiley and Sons, 1966.

43. Myers, F.A. — Gunn Effect Technology (Part 3). Microwave Systems News, Oct/Nov. 1975.

44. Shipow, A. — Let's Clear up the Confusion on PTD. Micro Systems News, April 1977.

45. — Data Sheet, Model CM-1 Double -Balanced Mixer, Vari-l Co., Inc.

46. Jasik, H. (Ed) — Antenna Engineering Handbook McGraw Hill, 1961

47. Gladman, B.R. — A Theoretical Study of Low Sidelobe Antenna Arrays. PhD. Thesis, London University, 1975.

48. Iglehart, S.C. — Noise and Spectral Properties of Active Phased Arrays I.E.E.E. Trans. Vol. AES-11, No.6, Nov. 1975

49. Kurokawa, K. — An Introduction to the Theory of Microwave Circuits. Academic Press, New York. 1969

50. Austin, J. and Forrest, J.R. — Low Cost Active Array Module Design for Transmit and Receive Operation. Conf. Proc. Fifth European Microwave Conf. Hamburg, 1975.

51. Silver, S. — Microwave Antenna Theory and Design. McGraw Hill, 1948.

52. Rhodes, D.R. — Synthesis of Planar Antenna Sources. Oxford University Press, 1974.

53. Cullen, A.L. Davies, J.A. and Williams, A.D. — A Precise Injection Locked l.F. Phase Shifting Technique and its Application to Microwave Q-Factor Measurement. Proc. Conf. Precision Electromagnetic Measurements, Boulder, Colorado, July, 1976.

54. Austin, J. and Forrest, J.R. — A Precise Digital Phase Shifter Using a Phase-Locked Loop. Electronics Letters, Vol. 14, No. 8, April, 1978.

55. Austin, J.
Forrest, J.R.
Schoenenberger, J.G.
and Williams, A.D.
An Active Phased Array incorporating Phase Locked Loops
Proc. Int. Conf. 'Military Microwaves' 1978, p. 331. (Reprinted in M.S.N., 9, 1, p.84)

56. Austin, J.
Forrest, J.R.,
Schoenenberger, J.G.
Progress Report No. 2. (May 78)
USAF - AFOSR Grant 77-3238
Scanned Active Array Radar

57. Hammerstad, E.O.
Equations for Microstrip Circuit Design
Proc, 5th European Microwave Conf., Hamburg 1975, p. 268.

58. Reisch, F.E.
Designing Coupled Lines with a Pocket Calculator
Microwaves, June 78, p. 88.

59. Hewitt, S.J.
Fundamental Limits on Varactor-tuned Oscillators.
Internal Note, Plessey Co. Ltd.

60. Matthaei, G.L.
Young, L. and
Jones, E.M.T.
Microwave Filter Impedance Matching Networks and Coupling Structures
McGraw Hill, NewYork

61. Ros, A.E.
Design Charts for Inhomogeneous Coupled Microstrip Lines.
IEEE Trans. MTT-26, 394, June 1978

62. Bosma, H.
On Stripline Y-circulation at UHF
IEEE Trans. MTT-11, Jan. 64, p. 61.

63. Vogel, R.W.
Effects of the T-junction Discontinuity on the Design of Microstrip Directional Couples.
IEEE Trans. MTT-20, Mar. 73, p. 145.

64. Wasse, M.P. and
Denison, E.
An Array of Pulsed X-Band Microstrip Gunn Diode Transmitters with Temperature Stabilisation.
IEEE Trans. MTT-19, July 72, p. 616.

65. Menzel, W.
Design of Microstrip Power Dividers with Simple Geometry.
Electronics Letters, 25 Nov. 76, p. 639.

66. Austin, J.
Forrest, J.R.
and Williams, A.D.
Noise Analysis of the Phase Locked Loop.
UCL Internal Report, Oct. 79

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (PJs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.